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Enhancement of Thermoelectric Properties of ALD Synthesized PbTe and PbSe by Phonon Engineering

Xin Chen
Old Dominion University

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**ENHANCEMENT OF THERMOELECTRIC PROPERTIES OF ALD SYNTHESIZED
PbTe AND PbSe BY PHONON ENGINEERING**

by

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ABSTRACT

ENHANCEMENT OF THERMOELECTRIC PROPERTIES OF ALD SYNTHESIZED PbTe AND PbSe BY PHONON ENGINEERING

Xin Chen

Old Dominion University, 2017

Director: Dr. Helmut Baumgart

Thermoelectrics is a green renewable energy technology that plays an important role in power generation due to its potential in generating electricity out of waste heat. The main challenge for the development of thermoelectrics is its low conversion efficiency. One key strategy to improve conversion efficiency is focused on reducing the thermal conductivity of thermoelectric materials. In this thesis, the novel phononic engineering concept was implemented by conformal ALD deposition of PbTe, PbSe thermoelectric films, and PbTe/PbSe nanolaminates on patterned silicon substrates in order to improve the thermoelectric performance of the thermoelectric films. The silicon substrates were lithographically patterned with a mask into porous templates with a regular or staggered pore arrangement and alternatively into stripe and trench patterns. The effect of nano-patterning on the Seebeck coefficient, electrical conductivity, and thermal conductivity of the thermoelectric films was studied experimentally. The results indicate that usage of porous Si templates simultaneously enhances the Seebeck coefficient and reduces thermal conductivity. A ZT enhancement was achieved in porous ALD PbTe/PbSe nanolaminates by a factor of up to three at a temperature of 500 K. Therefore, the novel concept and engineering approach of phonon engineering has been successfully rendered. For the case of stripe patterning nano-structures, the simulation results indicate a ZT enhancement was expected in the structures with a mesa stripe width of less than 2 μm and a trench depth larger than 500 nm. For in-plane ZT characterization, a lab-on-a-chip based platform was applied to measure the in-plane Seebeck coefficient, electrical

conductivity and thermal conductivity quasi-simultaneously. All of the ALD PbTe and PbSe thin film samples exhibit super low in-plane thermal conductivity κ , which is attributed to grain boundary scattering occurring in polycrystalline ALD PbTe and PbSe films. In addition, we extended our investigation to the thermoelectric properties of hybrid Surface Anchored Metal-Organic-Framework (SURMOF) thin films. TCNQ loaded MOF films exhibit a higher Seebeck coefficient and super low thermal conductivity κ in the temperature range of 290 ~ 350 K, which render MOF films a promising thermoelectric material for thermoelectric applications around room temperature and a potentially inexpensive alternative hybrid organic-inorganic thermoelectric materials.

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This thesis is dedicated to my family and relatives.

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CHAPTER 1

1. INTRODUCTION

1.1 Introduction to Thermoelectrics

Energy consumption is an important issue getting significant attention from the entire world. Energy resources including solar, nuclear, hydroelectric, wind, geothermal, natural gas, coal, biomass, and petroleum, are being used for residential, industrial, commercial and transportation purposes. Vast quantities of data for the US in 2016 are displayed in Figure 1 representing the energy flow chart depicting energy resources and their actual use. The total amount of heat energy wasted in the US is about 66.4 quadrillion BTU/year, equivalent to a loss of \$6B/year. Heat is one of the most commonly released by-products wasted into surroundings - automobiles, plants, factories - all involve heat waste. Harvesting even 20% of that heat waste is comparable to adding 10-30 nuclear power plants at no cost. Solar energy, wind energy, bio energy and hydroelectric energy are some of the prominent renewable energy sources in today's world. Thermoelectric energy conversion (TEC) is another green renewable energy that is characterized by a zero emission and maintenance technology to harvest electricity out of waste heat. Thermoelectric materials have attracted much attention for their potential in the conversion of waste heat to electricity and consequently could be used for heating and cooling systems.

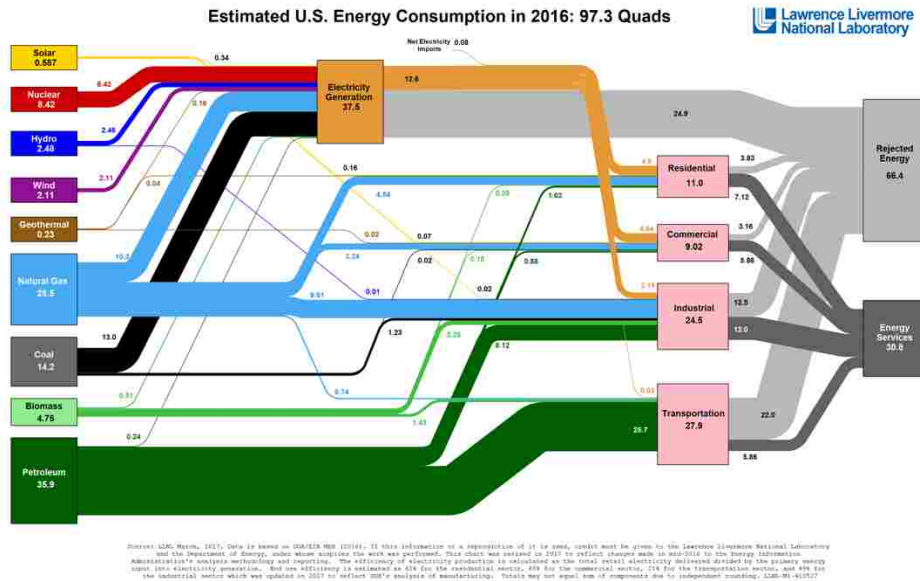


Figure 1. Energy flow chart depicting resources and their use represents vast quantities of data in USA in the year of 2016 (<https://flowcharts.llnl.gov/commodities/energy>).

Thermoelectrics originated in the year 1821, when German scientist Thomas Johann Seebeck first observed that a magnetic needle was deflected if two similar conducting materials in a closed loop were maintained at different temperatures. This phenomenon was found in a larger number of materials, including semiconductors. At first, Seebeck incorrectly considered it to be a magnetic polarization effect. After subsequent studies, Hans Christian Oersted, a Danish scientist, predicted that the reason behind the needle deflection was the flow of electric current. When current flows, a voltage difference was generated which is given by,

$$\Delta V = \int_{T_1}^{T_2} S dT \quad (1)$$

where S is the Seebeck coefficient [1]. Earliest efforts had been made to generate electrical power using thermocouples with the efficiency of 3%, which was comparable to the best steam engines at that time [2].

Thirteen years later, a French physicist, Jean Peltier, discovered a temperature change across the junction of two dissimilar conducting materials when a current passed through them. This is the reverse effect of the Seebeck effect and was named the Peltier effect. The heat is absorbed or released at the junction depending on the direction of current flow. The ratio of I to q defines the Peltier coefficient, given by:

$$\Pi = \frac{I}{q} \quad (2)$$

where Π is the Peltier coefficient and I is the current.

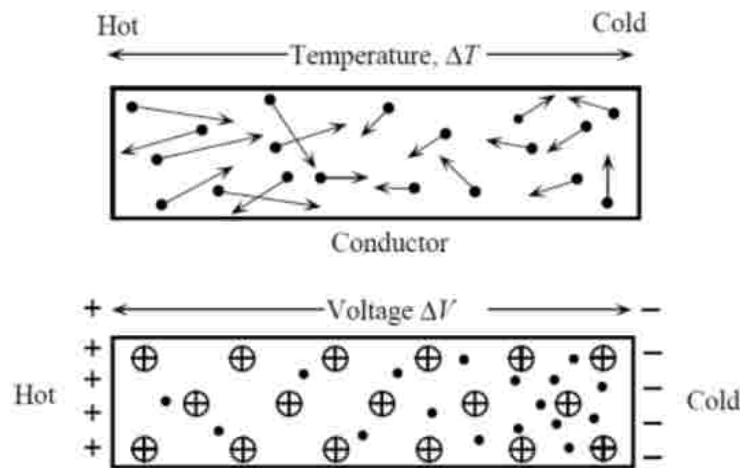


Figure 2. Representation of moving electrons (upper one) and moving carriers (bottom) on the conductor [3]

These two effects determine the thermoelectric property of any material. For the case of the Seebeck effect, the temperature gradient results in more excess charge carriers on the hot side than on the cold side due to thermal heat excitation of charge carriers. Due to the concentration gradient, the charge carriers (electrons or holes) then diffuse from the hot side to the cold side,

thereby creating an accumulation of the charge carriers (electrons or holes) on the cold end and opposite charge carriers (holes or electrons) on the hot end of a thermoelectric generator [3]. This builds the voltage difference between the hot and cold sides for current to flow, which is illustrated in Figure 2. The Seebeck effect provides the principle for a thermoelectrical generator. The schematic diagram for thermoelectrical generators consisting of two dissimilar semiconductors (p-type and n-type), which are also called TE legs, is shown in Figure 3 (a). When the two junctions of two TE legs experience a temperature gradient, the heat source excites more electrons (majority carriers) in the n-type semiconductor and more holes in the p-type semiconductor on the hot side. The diffusion of electrons under the influence of the concentration gradient in the n-type leg and holes in the p-type leg from the hot side to the cold side results in a voltage difference between the two ends of the generator. The Peltier effect explains the mechanism of a thermoelectrical cooler. A practical thermoelectric cooler typically contains two dissimilar p-type and n-type semiconductors that are connected electrically in series and thermally in parallel. Figure 3 (b) displays the schematic diagram of the thermoelectrical cooler. When a current is applied in the closed loop consisting of two dissimilar p-type and n-type TE legs, electrons in the n-type TE leg move from one side to the other side opposite of the current direction, while holes move along the current direction. Illustrated by the schema in Figure 3 (b), both electrons and holes are moved away from top junctions dragging along heat, which leads to the cooling of the top junction and temperature rising at the bottom junction. Energy is released or absorbed when the charge carriers move from one end to the other depending on the average energies of the charge carriers. The reversal of current direction shown in Figure 3 (b) leads to a temperature increase in the top junction and cooling of the bottom junction.

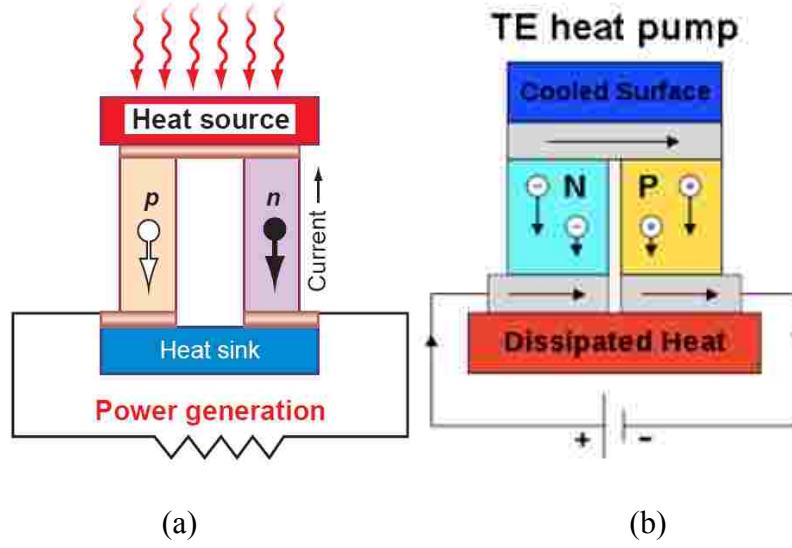


Figure 3. Schematic diagram of Seebeck effect and Peltier effect.

As a green renewable energy technology, thermoelectrics plays an important role in recovering energy from waste heat due to its potential in converting heat into electricity. Thermoelectrics has been applied in TE power generators to use electricity generated from waste heat as a power source for automobiles or even spacecraft and satellites and in the thermoelectrical cooler taking advantage of its small size, flexible shape, portability and long lifetime. The challenge for current state-of-the-art TE devices is the low conversion efficiency, which is true for all green renewable techniques. The efficiency of a thermoelectric device is expressed as:

$$\eta = \frac{T_H - T_C}{T_H} \left[\frac{(1 + ZT)^{\frac{1}{2}} - 1}{(1 + ZT)^{\frac{1}{2}} + \left(\frac{T_C}{T_H}\right)} \right] \quad (3)$$

where T_C and T_H indicate the temperature of the cold and hot sides. The conversion efficiency η is determined by the dimensionless thermoelectric Figure of Merit ZT ,

$$ZT = S^2 \sigma T / (\kappa_e + \kappa_L) \quad (4)$$

where S is the Seebeck coefficient, σ is the electrical conductivity, T is the temperature in Kelvin, κ_e is the thermal conductivity due to electrons, and κ_L is lattice thermal conductivity due to phonons

[1]. This Figure of Merit was first formulated in 1909 by the German scientist Edmund Altenkirch [4] as $Z = S^2\sigma/(\kappa_e + \kappa_L)$ and was later popularized by A. Ioffe [5] in the 1950s as a dimensionless Figure of Merit by multiplying Z with T .

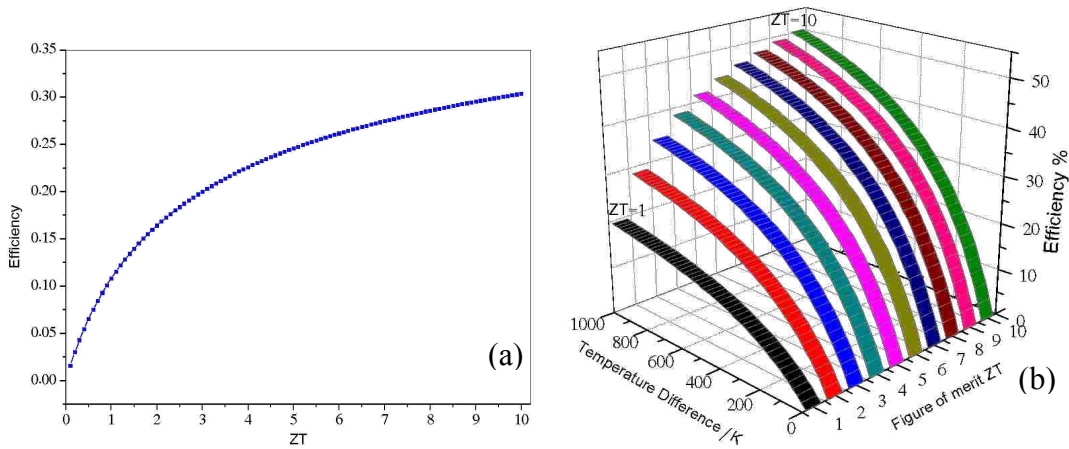


Figure 4. Simulation results of (a) the dependence of TE efficiency on ZT ; (b) the dependence of TE efficiency on Figure of Merit (ZT) and Temperature difference.

Figure 4 shows the simulation result for the dependence of the conversion efficiency η on ZT and temperature difference. This graph demonstrates a clear trend: the higher the Figure of Merit ZT , the higher the conversion efficiency η would be. For current state-of-the-art TE devices, the Figure of Merit ZT value is usually around one, which translates into a conversion efficiency that is usually no higher than 5%. For large-scale practical applications, it is critical to synthesize better TE materials with a higher Figure of Merit ZT in order to promote attractive conversion efficiencies for TE devices.

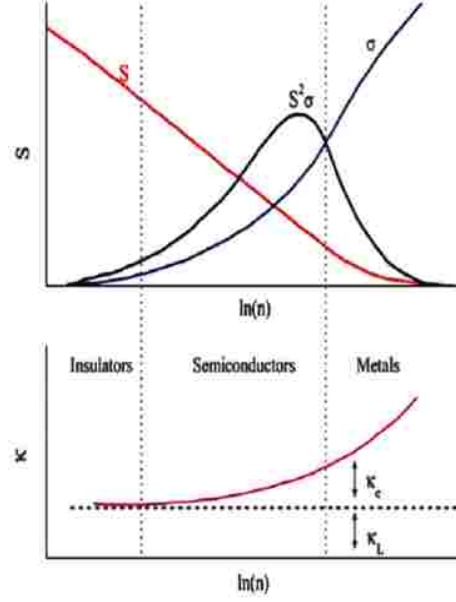


Figure 5. *The relationship of Seebeck coefficient, electrical conductivity and thermal conductivity on the carrier concentrations for a bulk material [6].*

To increase the ZT value, it is not sufficient to simply increase the Seebeck coefficient (S) and the electrical conductivity (σ) and to decrease the thermal conductivity (κ_e and κ_L), since these parameters are correlated to each other in a complex way. The Seebeck coefficient can be expressed by

$$S = \frac{8\pi^2 k_B^2}{3eh^2} m^* T \left(\frac{\pi}{3n}\right)^3 \quad (5)$$

where k_B is Boltzmann constant, m^* is effective mass, h is plank constant, and n is carrier density. The Seebeck coefficient is inversely proportional to the density of charge carriers. An increase of the Seebeck coefficient S leads to a reduction of electrical conductivity, σ , while enhancement of electrical conductivity σ results in an increase of thermal conductivity κ_e as illustrated by Figure 5. A high Seebeck coefficient usually is found in semiconductor or insulator materials with lower carrier density. While high electrical conductivity is typically observed in metals, the maximized

power factor ($S^2\sigma$) can be found in highly doped semiconductors with a carrier concentration of $10^{19} \sim 10^{21} \text{ cm}^{-3}$ [7]. Since κ is inversely proportional to ZT , low thermal conductivity is the other essential requirement for high ZT TE materials. The thermal conductivity of TE materials consists of two components: the electronic thermal conductivity κ_e , which results from heat carrying charge carriers (electrons or holes), and the lattice thermal conductivity κ_L , which results from lattice vibrations through crystal lattices. The Wiedemann-Franz law provides the relationship between electrical conductivity and electronic thermal conductivity κ_e , which is described by:

$$\kappa_e = L_0\sigma T \quad (6)$$

Where L_0 is the Lorentz number with a value of $2.44 \times 10^{-8} \text{ W}\cdot\Omega/\text{K}^2$. This law provides the ratio of the electrical component of thermal conductivity and the electrical conductivity in relation to the product of Lorentz number (L) and temperature (T) [8]. This law is applicable at high temperatures and at low temperatures whereas it fails at intermediate temperatures. In metals and highly doped semiconductors, this ratio is almost a constant at a given temperature. However, in semiconductors, this ratio is much greater which makes it more suitable for thermoelectric applications. The electronic thermal conductivity is proportional to the electrical conductivity. However, it may not be feasible to achieve high ZT by reducing the electronic thermal conductivity because the reduction in electrical conductivity will inversely affect the electrical conductivity and will ultimately decrease the power factor. The lattice thermal conductivity κ_L describes the thermal conductivity due to heat transfer by way of elastic vibrations of lattices, which is defined by:

$$\kappa_L = \frac{1}{3} C_v v_s \lambda_{ph} \quad (7)$$

Where C_v is heat capacity, v_s is sound velocity, and λ_{ph} is the mean free path of phonons. The lattice thermal conductivity is the only parameter that is independent of the Seebeck coefficient,

the electrical conductivity or the electronic thermal conductivity. Therefore, reduction in lattice thermal conductivity is a feasible and effective approach to enhance ZT.

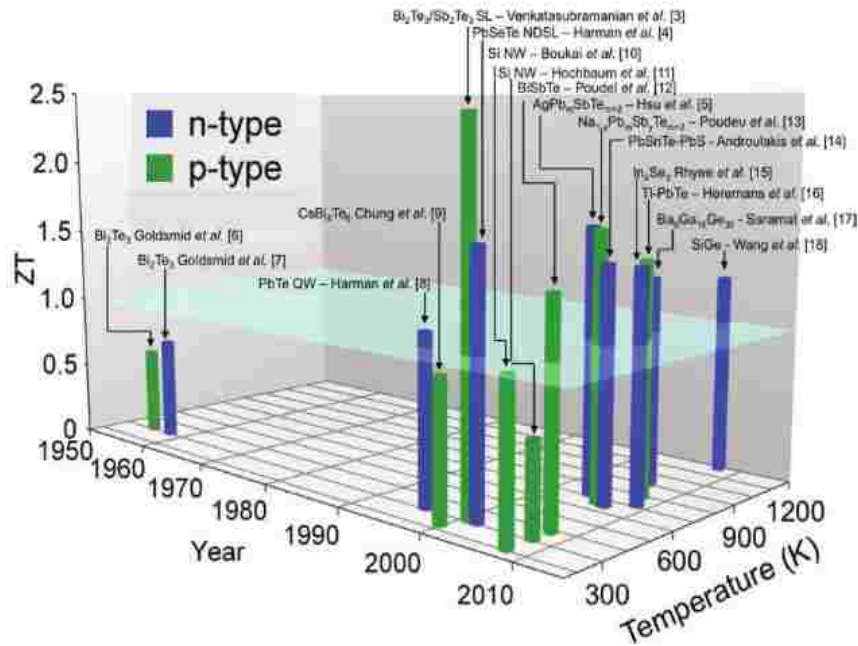


Figure 6. Major milestones achieved for ZT as a function of both year and temperature [9]. p-type Bi_2Te_3 [10], n-type Bi_2Te_3 [11], GeSi [12], $\text{Pb}_{1-x}\text{Eu}_x\text{Te}/\text{PbTe}$ quantum well [13], CsBi_4Te_6 [14], p-type $\text{Bi}_2\text{Te}_3/\text{Sb}_2\text{Te}_3$ SL [15], n-type $\text{Bi}_2\text{Te}_3/\text{Bi}_2\text{Te}_{2.83}\text{Se}_{0.17}$ SL [16], n-type $(\text{Bi,Sb})_2(\text{Se,Te})_3$ Quantum Dot SL [16], $\text{AgPb}_m\text{SbTe}_{2+m}$ ($m = 10, 18$) [17], $\text{Na}_{0.95}\text{Pb}_{20}\text{SbTe}_{22}$ [18], $\text{Ba}_8\text{Ga}_{16}\text{Ge}_{30}$ [19], Si nanowire [20] [21], Zn_4Sb_3 [22], $\text{Pb}_{1-x}\text{Sn}_x\text{Te}/\text{PbS}$ ($x = 0.08$) [23], Ti doped PbTe [24], Na doped $\text{PbTe}_{0.85}\text{Se}_{0.15}$ [25]

For the development of thermoelectrics, bismuth telluride (Bi_2Te_3), lead chalcogenides like lead telluride (PbTe) and silicon germanium (SiGe) bulk materials are the first generation TE materials mainly working in an optimal way at room temperature, intermediate temperature range and high temperature [26], respectively. Figure 6 shows major milestones achieved for ZT as a

function of both year and temperature. Great progress has been made in recent years. Most R&D efforts have achieved a ZT value of 1 during the last two decades. The highest ZT reported in $\text{Bi}_2\text{Te}_3/\text{Sb}_2\text{Te}$ superlattices is 2.4 [15]. The periodicity of the superlattice was controlled and optimized to modulate the transport of electrons and phonons in $\text{Bi}_2\text{Te}_3/\text{Sb}_2\text{Te}$ superlattices. Despite such a singular high achievement, progress in TE materials still has been limited to practical applications. To enhance the TE conversion efficiency, researchers are focused on two main directions: increasing the power factor ($S^2\sigma$), and decreasing the thermal conductivity κ .

1.2 The Phonon Glass Electron Crystal

The Phonon Glass Electron Crystal (PGEC) is one of the most popular approaches applied for the enhancement of ZT. PGEC stands for an ideal hypothetical material that possesses the low thermal conductivity of glass and high electrical conductivity of crystals and was first proposed by G. A. Slack et al. [27]. It provides a strategy of ZT enhancement by optimizing the thermal and electrical conductivity of TE materials. Generally, the electrical conductivity of semiconductors can be improved by doping the materials to n-type or p-type. The enhanced charge carrier density results in an improvement in electrical conductivity. Regarding thermal conductivity, thermal transport in crystalline dielectric solids or amorphous glasses is accomplished by lattice vibrations and interactions of phonons. The phonons are the quantum description of a collective vibration of a lattice consisting of atoms or molecules. The lifetime of electrons is zero in most non-metallic materials, indicating electrons have no contribution to heat transport. Therefore, the electronic thermal conductivity was not taken into consideration in this case. The wavelength of phonons in crystalline solids is distributed over a broad range. First principle calculations reveal that the long-wavelength phonons contribute 95% to the total thermal conductivity in bulk materials. The

existence of defects, voids and interface boundaries in the crystals acts as scattering centers to block heat transfer through phonons, which leads to a reduction of thermal conductivity. Therefore, the PGEC idea suggests that an ideal TE material can be realized in a cage-like “open structured” compound as a host crystal, and inside of which heavy mass atoms were trapped acting as scattering centers of phonons to reduce thermal conductivity. These PGEC materials were observed experimentally in skutterudite and intermetallic clathrates.

A Skutterudite is a cubic crystal structure with $Im\bar{3}$ space group. This structure was typically in the family of $(Co, Ni, Fe, Ir, Rh)(P, Sb, As)_3$, containing voids with large unit cells [28]. It has been reported that the thermal conductivity of Skutterudite structures can be altered by inserting rare earth elements into the host structure. The infiltrated heavy rare earth atoms act as scattering sites generating large scale local anharmonic lattice vibrations. As a result, the thermal conductivity decreases due to lattice vibrations, while little effect on the electrical conductivity has been seen. This renders skutterudites an ideal model of TE material. The phonon propagation can be suppressed up to 58% resulting from the lattice phonon scattering caused by the large mass of inserted rare earth atoms [29].

Intermetallic clathrates are another candidate for the PGEC structure; they consist of a nano-caged structure working in the same way as skutterudites. It was also realized by inserting guest molecules into the host cage. The off-center oscillations of guest atoms inside the voids, which is also called “rattling” or “rattler”, suppress heat flow and thereby reduce the thermal conductivity of the materials to values as low as ~ 2 W/Km [30, 31]. In contrast, the electrons can move freely and undisturbed along the crystalline structure of the host materials. The intermetallic clathrate is typically formed by Zintl compounds with cage frameworks of Si, Ge, and Sn, and buried cationic guests [32, 33]. The non-stoichiometric clathrate generates charge carriers and

thereby behaves like semiconductors. The carrier density can be modulated in a range of 10^{-19} to 10^{-20} per cm^3 , resulting in a decent electrical conductivity and a simultaneously high Seebeck coefficient [33, 34].

Reduction of thermal conductivity is key for enhancement of ZT. The lattice thermal conductivity of each material is limited by the mean free path of the phonons resulting from atomic substitution and nano-structures in alloys [31, 35]. It is reported that every material has its well-defined minimum lattice thermal conductivity. The lowest lattice thermal conductivity can be reached when the characteristic length scale is the mean free path of phonons is equal or approaching their wavelength [31, 35]. Slack et al. have pointed out that the lowest thermal conductivity of heavy element semiconductors will be in the range of $0.1 \sim 0.5$ W/mK at room temperature, and PbTe can exhibit thermal conductivity as low as 0.25 W/mK, for instance [33, 36].

The limitation in thermal conductivity of TE materials predicts the highest possible ZT values of TE materials and the ultimate performance of TE devices. Figure 7 displays the calculated ZT values as a function of carrier concentration in the PGEC model at three different temperatures. The closer the lattice thermal conductivity of the PGEC materials is to their minimum thermal conductivity, the higher possible values of ZT can be reached within all the temperature ranges in the doping level of $10^{-17} \sim 10^{-18} \text{ cm}^{-3}$. In Figure 7c the highest theoretical ZT of 4 can be achieved at 300K when the lattice thermal conductivity is reduced to the minimum value.

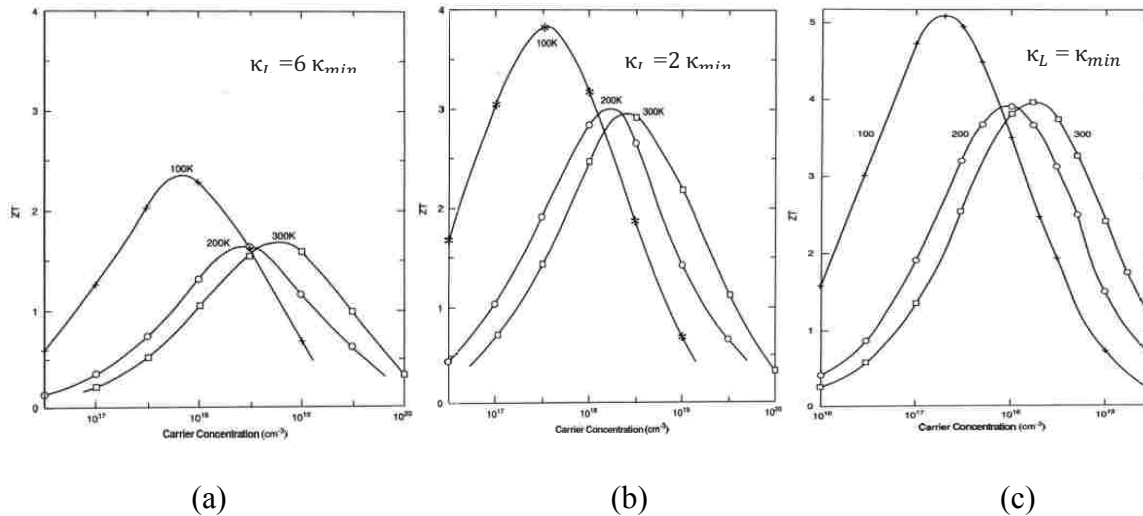


Figure 7. The calculated ZT as a function of carrier concentration for (a) $\kappa_L = 6\kappa_{min}$, (b) $\kappa_L = 2\kappa_{min}$, (c) $\kappa_L = \kappa_{min}$ at three different temperatures 100 K, 200 K, and 300 K [1].

By the 1950s, there were several semiconductor compounds with narrow bandgap that had been identified as TE candidates, such as PbTe, PbSe, Sb₂Te₃, Bi₂Te₃, and related heavy element compounds. The related ternary and quaternary compounds are usually prepared by alloying, which possesses a ZT value of around 1 for thermoelectric generator and cooler applications. The enhanced ZT results from the reduction of lattice thermal conductivity due to enhanced phonon scattering caused by the mass difference without affecting electrical conductivity significantly [37]. The alloys are typically exhibiting thermal conductivity in the range of 5 ~ 10 W/mK at room temperature and have their well-defined lowest possible thermal conductivity [33, 38], which is also called an alloy limit. In the Rayleigh scattering regime, the scattering cross-section σ ($\sigma \sim b^6/\lambda^4$) is proportional to the size of the scatter particles (b) and inversely proportional to the phonon wavelength (λ). The size of the scattering particles in alloys is around 1 Å, which indicates that phonons with shorter wavelength would be scattered more effectively than the phonons with

mid or longer wavelength. The scattering of phonons with mid and long wavelength becomes essential to further decrease the lattice thermal conductivity.

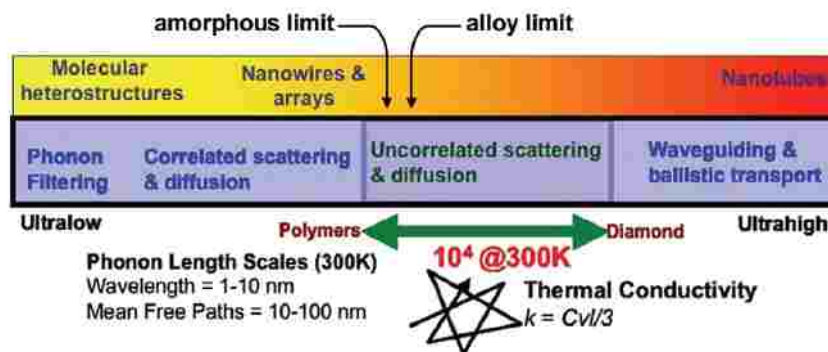


Figure 8. Schematic diagram illustrating various approaches to reduce the thermal conductivity of materials [38].

Figure 8 illustrates various ways to expand the limit of thermal conductivity. By introducing nano-particles, nano-sized polycrystallines, and numerous interfaces into bulk TE materials, such nanostructures covering a range of length scales from 5 nm ~ 10 μ m can effectively scatter the phonons in a broad range of mean free paths and thereby reduce the lattice thermal conductivity breaking the alloy limit. For instance, it is reported that the compacted 30 ~ 50 nm-thick $\text{Bi}_{0.5}\text{Sb}_{1.5}\text{Te}_3$ nano-platelets fabricated by the hydrothermal method exhibit a low thermal conductivity of 0.37 W/mK at 295 K, which is much lower than the thermal conductivity of parent bulk compounds (1.5~2.4 W/mK), and yields a ZT value of 0.93 at 295 K [39]. Three years later, a joint research group from South Korea and the US reported on the same alloy of $\text{Bi}_{0.5}\text{Sb}_{1.5}\text{Te}_3$, which was fabricated by using melted telluride to fuse bismuth, antimony, telluride granules, exhibiting a high ZT of 1.86 at 320 K [36]. The granule size varied from 10 nm to 20 nm. The dense dislocation arrays generated at grain boundaries in the $\text{Bi}_{0.5}\text{Sb}_{1.5}\text{Te}_3$ alloy played a significant

role in scattering the phonons with mid-wavelength, resulting in a lower thermal conductivity of 0.33 W/mK at 320 K.

1.3 Nanostructuring

Nanostructuring is another proven approach to beat the alloy limit. In principle all low dimensional nano-structures, including two-dimensional quantum well or superlattices, one-dimensional nano-wire or nano-tube, and zero-dimensional quantum dots, confine the motion of electrons in one or more dimensions, which decouples the dependence between the Seebeck coefficient S , the electrical conductivity σ and thermal conductivity κ , and make it possible to enhance power the factor product of $S^2\sigma$ and reduces κ somewhat independently [40] [40]. This is attributed to the difference in the density of states of low dimensional materials and bulk materials. Figure 9 shows the density of states of semiconductors as a function of energy for 3-D material and low dimensional materials. As the dimensionality decreased from 3-D to 0-D, the dependence of density of states on the energy changed from continual in 3-D structures to step-like in 2-D structures and pulse-like in 1-D structures, and to discrete in 0-D structures. The electron confinement effect in low dimensional structures increased the density of states near the Fermi level and thereby enhanced the electrical conductivity since it is directly proportional to the density of states [41] under the assumption of energy independent electron scattering.

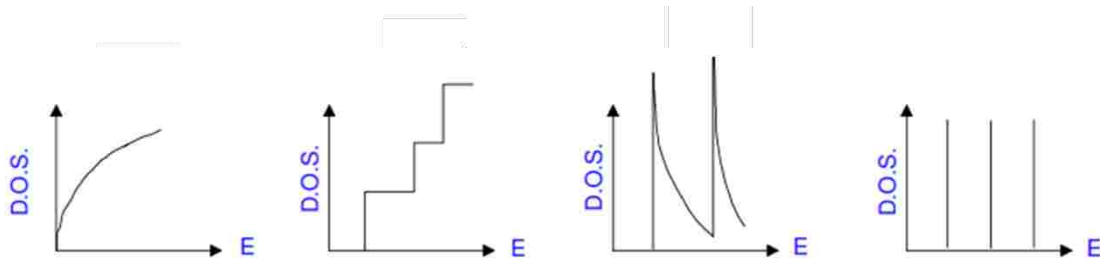


Figure 9. *Electronic density of states as a function of energy for (a) 3-D bulk semiconductors, (b) 2-D quantum well or superlattices structures, (c) 1-D nano-wire or nano-tube structures, and (d) 0-D quantum dots structures [41].*

Most recently, novel innovative research approaches focused on low dimensional nanostructures [9], including quantum wells [15], quantum dots [42], and superlattices [16], in order to improve the Figure of Merit ZT . P-type $\text{Bi}_2\text{Te}_3/\text{Sb}_2\text{Te}_3$ superlattices were found to exhibit the highest reported ZT value of 2.4 at room temperature with the lowest thermal conductivity of 0.22 W/mK by adjusting the period of superlattice to around 6 nm to control the transport of phonons and electrons in the superlattice [15]. Caylor and co-workers reported enhanced $ZT = 1.75$ at 425 K using $\text{PbTe}/\text{PbTe}_{0.75}\text{Se}_{0.25}$ quantum well structure with Se doping at 25% [43]. For 1-D nanowire structures so far, Bi based nanowires have been extensively investigated due to their properties at the transition between semi metal to semiconductor resulting from the size effect [40]. These nanowires are often synthesized using porous anodic aluminum oxide (AAO) or quartz (SiO_2) templates. Bi nanowires with diameters ranging from 9~15 nm have been reported with a factor of two more times enhancement in thermoelectric power $S^2\sigma$ in the 100~300K. An enormous ZT enhancement was observed at a low temperature (~150K), which benefited from the reduction of the thermal conductivity. Herman and co-workers proposed a lead chalcogenide based quantum dot superlattice system, $\text{PbTe}/\text{PbSeTe}$, embedding PbSe quantum dots in the PbTe

matrix, which achieved a ZT as high as 1.6 at 300K with low thermal conductivity of 0.33 W/mK [16]. In addition, other quantum dots systems such as $\text{AgPb}_m\text{SbTe}_{20-m}$, also known under the acronym LAST-18 [17], NaPbmSeTe_{20-m} known under the acronym SALT-20 [18], and $(\text{Pb}_{0.95}\text{Sn}_{0.05}\text{Te})_{0.92}(\text{PbS})_{0.08}$ [23] were reported to achieve ZT values as high as 1.7 (at 700 K), 1.6 (at 675 K), and 1.5 at 650 K, respectively.

Low dimensional nanostructures help to improve ZT because the quantum confinement effect increases the density of states near the Fermi level and consequently increases the thermal power factor ($S^2\sigma$). Additionally, the quantum confinement effect contributes to decoupling the inter-dependence relationship between electrical and thermal properties, resulting in increasing electrical conductivity while reducing thermal conductivity quasi-independently. On the other hand, numerous interfaces in the lower dimensional structures result in enhanced phonon scattering, and consequently, in a reduction of thermal conductivity and improved ZT values. The latter is the dominant cause of ZT enhancement [40]. Figure 10 displays the scattering mechanism of phonons and electron transport within TE materials. Since the mean free path of electrons is much smaller than that of phonons, the phonons could be scattered more efficiently than electrons. Meanwhile, the phonons with a short wavelength can easily be scattered by atomic defects, while the phonons with mid or long wavelength could be scattered by nano-particles and boundary interfaces. By wisely selecting the dimension of nano-structuring, the phonon scattering would be enhanced efficiently while the transportation of electrons would not suffer.

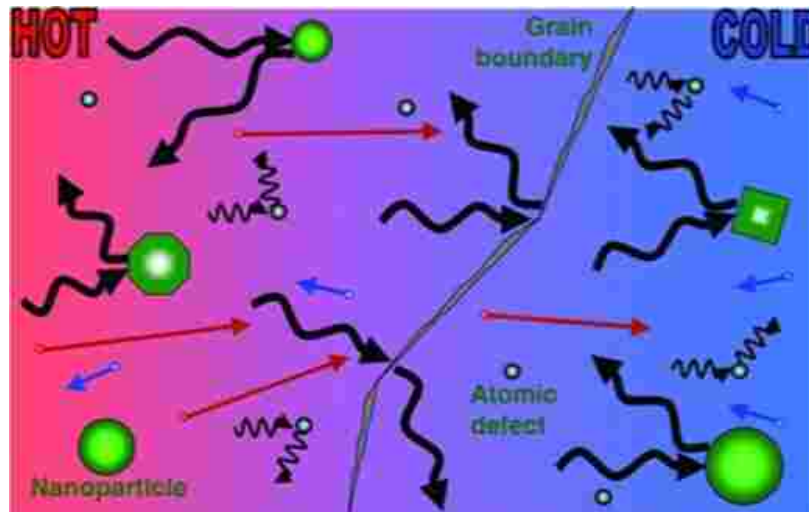


Figure 10. Phonon scattering mechanism and electrons transport within TE material. [37]

1.4 Phonon Engineering

Phonons

At the present time, it is generally known that reduction in lattice thermal conductivity caused by phonon scattering is a powerful strategy to enhance TE efficiency. In order to apply phonon engineering advantageously it is essential to have a sound understanding of the phonon scattering mechanism. Phonons are a quantum mechanical description of the vibration of elements in solids or some liquids, in which the atoms or molecules uniformly oscillate around their equilibrium position and interact with the neighbor atoms [44]. In this physical model phonons are considered as quasi-particles, possessing wave-like properties as in classic physics and particle-like quantum properties. In the lattice of crystalline solids composed of N atoms, the displacement of atoms from their equilibrium positions and the interactions between neighboring atoms lead to a wave propagation of atoms' elastic vibrations, as shown in Figure 11. The displacement of the atoms from their oscillating centers determines the amplitude of the lattice wave, and the amplitude of the lattice wave is higher at elevated temperatures. The wavelength of the phonon propagation

is defined as twice the equilibrium separations between atoms, which is marked in Figure 11. Phonon vibrations of different frequency and wavelength co-exist in a solid.

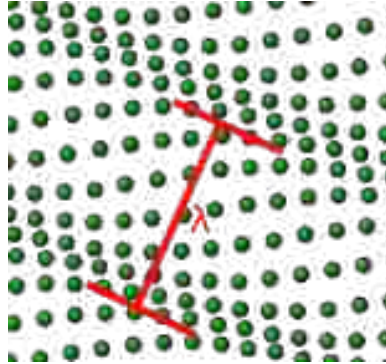


Figure 11. *Schematic depiction of phonon propagation through a crystal lattice*
(<https://en.wikipedia.org/wiki/Phonon>).

Considering the case of the lattice wave propagating along x-direction, i.e. the direction of wave vector k , the displacement of atoms can be either parallel along k or perpendicular to the direction of k . Therefore, there are three polarized modes for each wave vector, including one longitudinal mode in which the atoms oscillate along the direction parallel to k (eg. x-direction), and two transverse modes that the atoms vibrate perpendicular to the k (eg. y and z-directions) [45]. The phonons in a solid are classified into acoustic phonons and optical phonons. Acoustic phonons are coherent vibrations of atoms around the equilibrium position with two modes of LA (longitudinal acoustic) and TA (transverse acoustic), which typically disperse in the long wavelength range and contribute 95% of thermal conductivity in semiconductors [46, 47]. In contrast, the optical phonons usually disperse in short wavelength range and occur in compounds with two or more different atom species. Optical phonons are excited by infrared radiation. Ions with positive and negative charge are moving in opposite direction in an applied electric field. In

a crystal composed of the number of atoms $N \geq 2$, there are three acoustic modes, and $(N-1) * 3$ optical modes in total [48].

Phonon Scattering Mechanisms

In general, thermal conductivity of materials can be reduced by suppressing the propagation of phonons. The mechanism of phonon scattering consists of Umklapp phonon-phonon scattering, phonon-impurity scattering, phonon-electron scattering and phonon-boundary scattering [49]. When there is more than one phonon scattering mechanism occurring in a solid, which is the case when both impurities and boundaries are present in a solid, the total effect of phonon scattering can be expressed by Matthiessen's rule in terms of the relaxation rate:

$$\frac{1}{\tau} = \frac{1}{\tau_U} + \frac{1}{\tau_{impurities}} + \frac{1}{\tau_{ph-e}} + \frac{1}{\tau_B} \quad (8)$$

Where τ is the real average scattering time, τ_U , $\tau_{impurities}$, τ_{ph-e} , and τ_B are scattering time caused by Umklapp scattering, phonon-impurity scattering, phonon-electron scattering and phonon-boundary scattering, respectively.

Umklapp scattering is a phonon-phonon interaction involving three phonons. Two incoming phonons with wave vector of k_1 and k_2 shown in Figure 12 (a) combine during the scattering process and generate the third phonon with a wave vector of k_3 with conserved phonon momentum of the former two phonons in another Brillouin zone. The scattering time of Umklapp scattering is defined by:

$$\frac{1}{\tau_U} = 2\gamma^2 \frac{k_B T}{\mu V_0} \frac{\omega^2}{\omega_D} \quad (9)$$

Where γ is the Grüneisen parameter, ω is the phonon frequency, ω_D is the Debye frequency that defines the maximum possible vibration frequency of the atoms in a crystal, V_0 is the volume per

atom, and μ is the shear modulus. Umklapp scattering dominates at high temperature in low defect materials [50]. The relaxation time of Umklapp scattering τ_U is proportional to ω^{-2} , and Umklapp scattering dominates at high frequency.

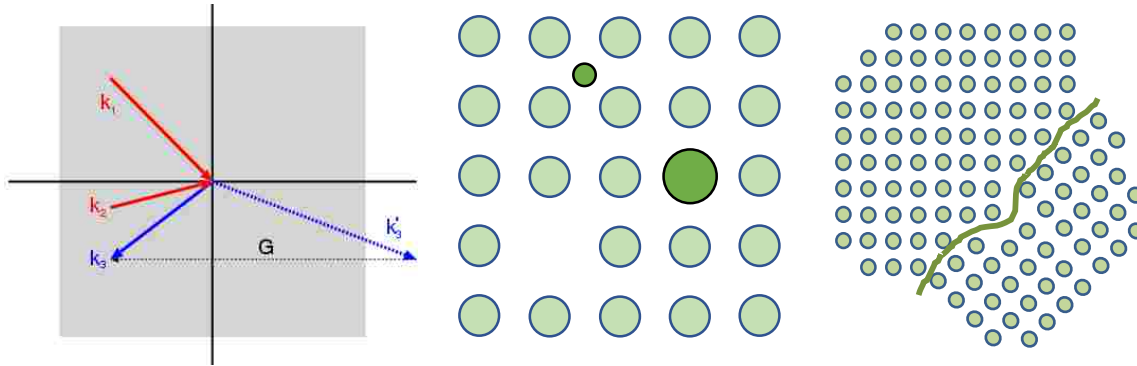


Figure 12. Schematic diagram illustrating the scattering mechanism of (a) Umklapp scattering [51], (b) impurities or defect scattering [52], and (c) phonon-boundary scattering [53].

Impurities or defect scattering is caused by random site disorder, such as vacancies, dislocations or substituted atoms, which create mass differences at lattice sites [54]. The thermal conductivity depends on the concentration of impurities or defects in the impurities or defect scattering dominated phonon scattering [55]. The relaxation time is defined by:

$$\frac{1}{\tau_{Im}} = \frac{V_0 \Gamma \omega^4}{4\pi v_g^3} \quad (10)$$

Where V_0 is the volume per atom, Γ is a measure of the impurity scattering strength, and v_g is the velocity depending on the phonon dispersive curve. The relaxation time of defect scattering is proportional to ω^{-4} , and is strongly affected by high frequency phonons [56].

Phonon-boundary scattering is an important mechanism in low dimensional nanostructures, including thin films, superlattice, nanowire, and nano-composites. The boundaries and interfaces play a significant role in scattering phonons with relative long wavelength, and

hence reduce the lattice thermal conductivity of materials. The phonons are scattered by interfaces when the characteristic length scale is no longer than the mean free path of the phonons. The relaxation time of phonon-boundary scattering τ_B is defined as:

$$\frac{1}{\tau_B} = \frac{V}{D}(1 - p) \quad (11)$$

where V is the volume per atom, D is the dimension of the system, and p is the boundary specular parameter. When $p = 1$, the phonons experience perfect specular boundary scattering, and the relaxation time τ_B is approaching infinity ∞ . Hence, the boundary scattering doesn't affect thermal transport. A value of p equaling 0 indicates the interfaces are really rough and phonons scatter more diffusively. In this case the relaxation time τ_B becomes a constant V/D , which is also known as the Casimir limit [57]. The phonon-boundary scattering mechanism only affects the phonons with a mean free path longer than the characteristic defect length, and has little dependence on phonon frequency.

These three phonon scattering mechanisms mentioned above co-exist in the materials simultaneously. Figure 13 plots the frequency dependence of the relaxation time for the three phonon scattering mechanisms together. We can see the relaxation time of the boundary scattering has little frequency dependence. Both Umklapp scattering and Impurity defect scattering depend on the phonon frequency, and the impurities defect scattering exhibits a stronger frequency dependence. Therefore, the total effective relaxation time τ is plotted as a black dot line in Figure 13. In addition, only Umklapp scattering is temperature dependent. At low temperature, Umklapp scattering can be neglected. Therefore, the boundary scattering dominates at low phonon frequencies, while defect scattering dominates at high phonon frequencies.

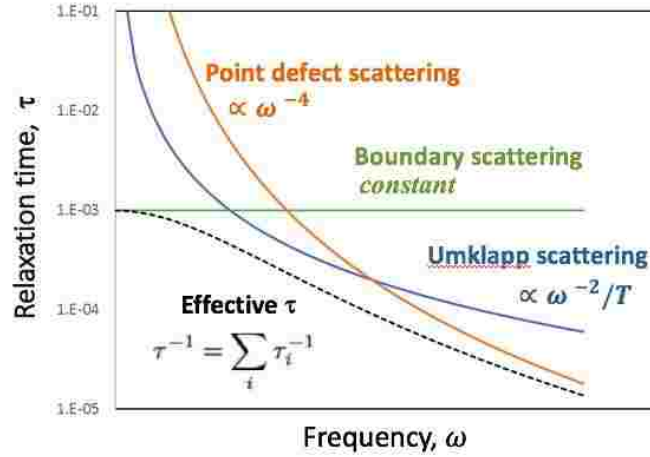


Figure 13. The relationship between the relaxation time of the three different scattering mechanisms and the frequency of phonons [58].

Phononic Crystal Structures

Very recently, researchers focused their attention on phononic crystal (PnC) nanostructures in thermoelectric materials. The thermal conductivity of PnC samples is lower compared to non-patterned thermoelectric samples due to phonon-boundary scattering [59-62]. Work from the University of Tokyo has produced a 2-D phononic crystal nanostructure using single crystalline or poly crystalline silicon membranes. Figure 14b shows experimental results for the thermal conductivity of PnC made from a single crystalline Si and polycrystalline Si membrane as a function of the radius of pores. 2-D PnCs made from polycrystalline Si exhibit lower thermal conductivity, which is attributed to grain boundaries scattering of thermal phonons with relatively short MFP, and periodic patterns scattering phonons with relatively longer MFPs. In addition, the geometric arrangement of pores plays a role in the reduction of thermal conductivity [63, 64]. Porous silicon template substrates and thin porous Si membranes are a relatively novel and versatile material with tunable properties related to their porosity and porous geometry. The thermal conductivity of porous templates is tunable by modulating the porous configuration

(staggered or aligned) [63], the geometrical shape of the pores (circular or square or triangular) [65] and the periodicity [66]. Figure 14c displays the dependence of thermal conductivity of porous Si on the shape and arrangement of pores. It has been proven by theoretical and experimental work that phonon-boundary scattering in porous materials contributes significantly in reducing phonon thermal conductivity up to two orders of magnitude compared to bulk materials [65]. Therefore, the phonon-boundary engineering tuning thermal transport in nanostructured materials is a powerful approach to develop high-efficiency thermoelectrical materials.

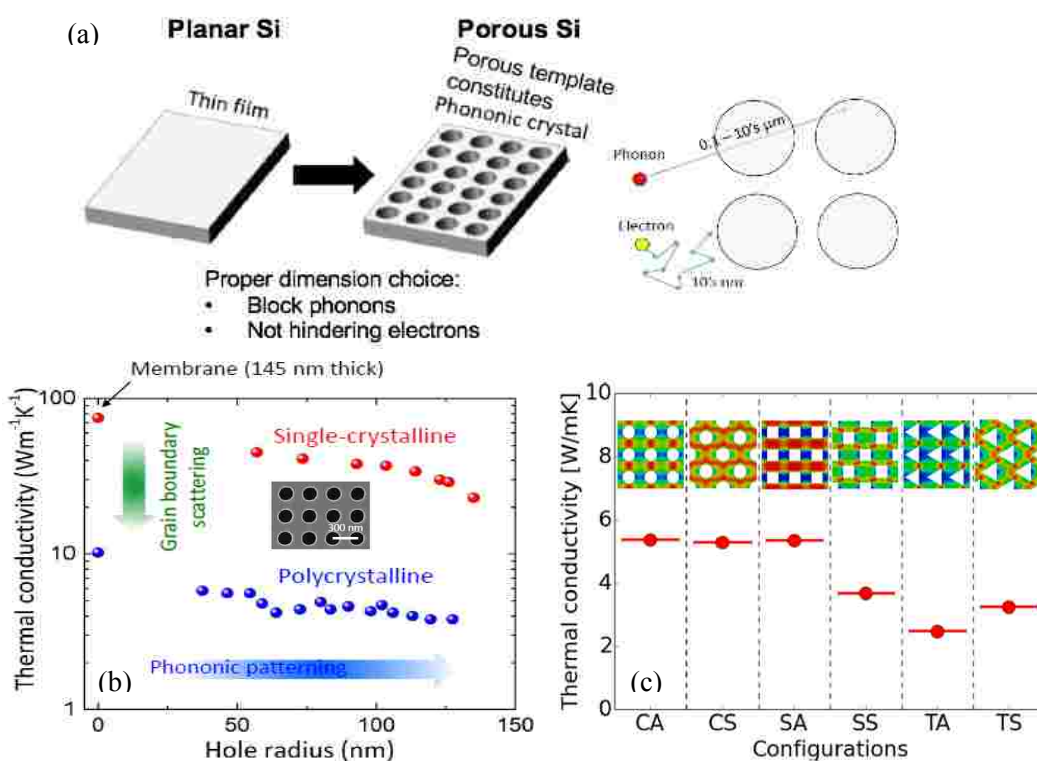


Figure 14. (a) Schematic illustration of the concept of Phononic Engineering by proper choice of the dimension scale of nano-structuring to block phonon while not hindering electrons. (b) Thermal conductivity of PnC vs. the radius of the holes. The inserted image is a schematic diagram of PnC with hole-center distance of 300 nm [67]. (c) Theoretical simulation of the dependence of thermal conductivity on the configurations of variously shaped pores [65].

1.5 Dissertation Objectives

Motivated by phonon-boundary engineering, we hypothesize that depositing conformal thermoelectric films on nano-patterned substrates will contribute to improved ZT values of such TE materials. Figure 15 illustrates the idea of improving the thermoelectric performance of conventional TE material (PbTe and PbSe) by using a nano-structuring and phonon engineering approach and thin films instead of bulk material. The main idea and the physics behind the concept of phonon engineering stems from the fact that the mean free path of electrons lies in the 10s of nm range, while the mean free path of phonons is orders of magnitude larger in the range of 0.1 - 10s μm . Therefore, through proper choice of the dimension scale of nano-structuring, one can block the phonon transport with certain structures like micro-pores, while not hindering the electron transport as illustrated in the schematic of Figure 14a. Adopting a two-pronged approach, the Si substrates were patterned either into stripes or alternatively into porous templates with different dimensions to investigate the effect of patterned substrates and the dimension of the patterns on the thermoelectric properties of the TE films. The deposited thermoelectric film thicknesses were controlled in relation to the mean free path of phonons in the TE films to confine the thermal transport along the in-plane horizontal direction. By depositing thin TE films or 2-D nanolaminate structures on a nano-patterned substrate, the numerous interfaces and boundaries that were introduced could scatter phonons more effectively, resulting in a reduction of thermal conductivity and consequently improving the Figure of Merit ZT.

The main objective of this thesis is to address the challenge of low conversion efficiency of thermoelectric materials with a novel phonon engineering approach in order to improve TE

properties of lead chalcogenide (PbTe and PbSe) by employing atomic layer deposition (ALD) technology to conformally deposit PbTe/PbSe nanolaminate films on nano-patterned Si substrates. Specific objectives of the study are detailed below.

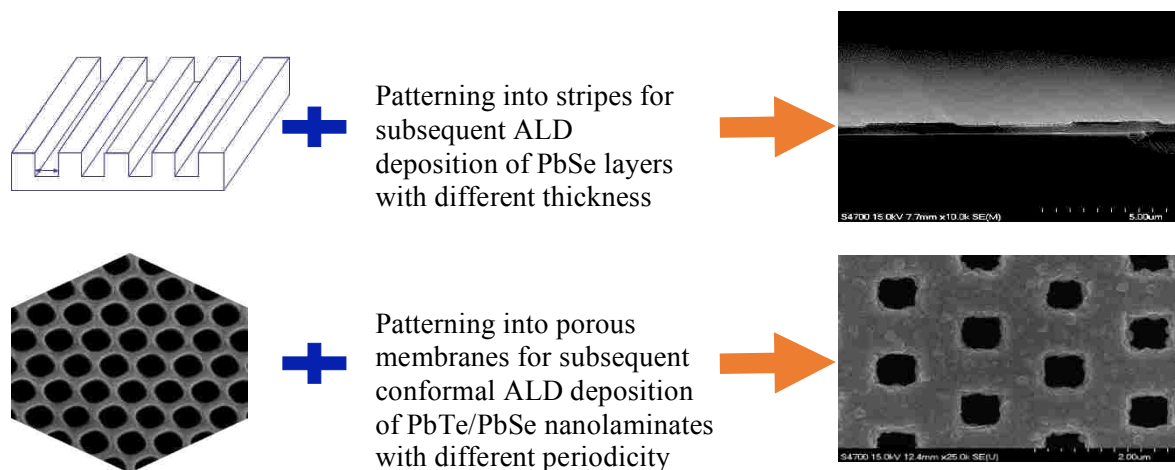


Figure 15. *Schematic diagram of nano-patterning of thermoelectrical PbSe/ PbTe materials for phonon-scattering engineering.*

Objective 1: Synthesis of PbTe/PbSe Nanolaminates film using ALD technology.

ALD technology was first applied for the synthesis of PbTe/PbSe nanolaminate structures in our work. ALD is a competitive technique to deposit thin films due to its advantages of precise thickness control, lower deposition temperature and uniform and absolutely conformal deposition on any complex patterned substrate morphology. Both ALD synthesized PbTe and PbSe films exhibit polycrystalline structure with granular film morphology. The polycrystalline nature of these thermoelectric films provides a sufficient number of grain boundaries to scatter phonons, which exactly meets our requirements. The preliminary results indicate the growth of PbTe and PbSe films by ALD and follow the Volmer-Webber island growth mode. However, the grains are

isolated in random size and orientation, and do not fuse together no matter how many ALD cycles were repeated. Achieving uniform and complete coverage of the sample surface with the ALD films would be the crucial first step to fabricate nanolaminate thermoelectric structures. The isolated granular surface morphology of ALD PbTe and PbSe results from the fact that atom-to-surface reactions dominate in ALD growth of PbTe and PbSe. By pre-treating the substrates with saturated OH⁻ hydroxyl termination and optimizing the growth conditions to enhance the chemisorption of the Se and Te precursors on the substrate, the initially isolated nucleated PbSe islands finally coalesce and combine tightly into a continuous TE PbTe and PbSe film.

Objective 2: To enhance TE properties by increasing the Power Factor and Figure of Merit ZT for PbTe/PbSe nanolaminates by applying porous silicon templates as substrates for the ALD deposited nanolaminate films.

Based on phonon boundary engineering, it is hypothesized that PbTe/PbSe nanolaminates grown conformally on porous silicon membranes would enhance the Seebeck coefficients of the thermoelectric film due to lower thermal conductivity κ in the porous structures. We set out to render this hypothetical concept into practice with a series of critical experiments for proof of concept. The dimension, scale and geometric arrangement and shape of the pores play an important role in determining the thermal conductivity of the film. The following series of experimental and simulation work was performed and is listed below:

- Patterning the silicon substrate into stripe patterns by etching thermal oxide hard mask on silicon wafers in KOH solution following photolithography patterning with a stripe mask.
- ALD Synthesis of PbTe, PbSe thin films, and PbTe/PbSe thermoelectric nanolaminates on nano-patterned silicon templates. The film thickness or the thickness of each layer in the

nanolaminates was controlled in the range of 10~20 nm comparable to the average mean free path of phonons in PbTe and PbSe films, in order to enhance phonon-boundary scattering.

- Physical characterization of surface morphology, crystal structure, and elemental composition with FESEM, AFM, XRD and EDS.
- Thermoelectric characterization to investigate the Seebeck coefficient, electrical conductivity, Hall Effect and thermal conductivity of the samples.
- Perform theoretical simulation of thermal conductivity dependence of the lead chalcogenide nanolaminates on the thickness of the wall of porous silicon templates, and the width/depth of stripe patterns.

The detailed experimental procedures and results for objectives 1 and 2 are discussed in chapter 3.

Objective 3: In-plane ZT measurements of PbTe/PbSe thin films deposited by Atomic Layer Deposition.

For anisotropic materials, the thermoelectric properties along vertical direction (perpendicular to the surface) and in-plane direction (parallel to the surface) are generally different. It is essential to measure all of the parameters (Seebeck coefficient, electrical conductivity and thermal conductivity) in the same direction to calculate the Figure of Merit ZT correctly. The maximum benefits of phonon engineering by nano-structuring thin thermoelectric films can only be achieved in the in-plane direction because space limitations in the vertical direction hardly leave room for nano-structuring. In this thesis, a lab-on-a-chip based thermoelectric test platform was applied to perform all in-plane ZT characterization of PbTe, PbSe thin films and double-layer

PbTe/PbSe films. The Seebeck coefficient, electrical conductivity and thermal conductivity of the films were measured quasi-simultaneously for one single thermoelectric film deposited on the ZT test chip. The thermoelectric properties of single-layer PbTe, PbSe thin film and double-layer PbTe/PbSe film were measured and discussed in chapter 4.

Finally, as an exercise in future outlook the investigation of phononic engineering in semiconductor TE materials on nano-patterned structures, was extended to the thermoelectric properties of novel hybrid Metal-Organic-Framework (MOF) HKUST -1 films. The experimental results are discussed in chapter 5. The guest molecule infiltrated MOF film structure is similar to the clathrate structure. In analogy to the clathrates, the loaded guest molecules inside the porous MOF framework enable off-center oscillations, which are known as “rattling” or “rattler”, suppress the heat flow, and thereby reduce the thermal conductivity of the materials. The results indicate that TCNQ loaded HKUST-1 MOF films are potentially promising candidates for thermoelectric applications.

CHAPTER 2

2. EXPERIMENTAL SETUP INSTRUMENTS

This chapter describes the technique used for thermoelectric thin film deposition, and the scientific instruments used for measuring the thermoelectric properties of thermoelectric films.

2.1 Atomic Layer Deposition

In this thesis, nano-structured PbTe/PbSe films were deposited in a conformal fashion in order to mimic the nano-structured contours of the Si substrates, and the resulting thermoelectric properties were investigated. PbTe and PbSe are popular thermoelectric materials for intermediate temperature thermoelectric applications due to their high Figure of Merit (ZT), good chemical stability, low vapor pressure and high melting point. PbTe and PbSe films have been deposited by different techniques, such as pulsed laser deposition (PLD) [47], metal-organic chemical vapor deposition (MO-CVD) [68], magnetron sputtering [69], molecular beam epitaxy (MBE) [70] and electrical-chemical atomic layer deposition (ALD) [71]. Thermal ALD is considered to be a novel, innovative and competitive method to synthesize PbTe/PbSe nanolaminate structures [72]. For this thesis thermal ALD was the film deposition technology of choice because only ALD technology affords absolute conformal thin film deposition, which is a key requirement for this study. No other film deposition technique is able to follow any nano-structured substrate morphology in a conformal fashion.

Atomic Layer Deposition (ALD) is a surface saturating self-limiting chemical reaction that occurs in each ALD monolayer deposition cycle. ALD technology can precisely control the film layer thickness, stoichiometry, composition, uniformity, and produce sharp interfaces. ALD also

can be used to deposit conformal films onto very complex 3-D structures and on the inside of cavities and negative slope surfaces. It is also possible to generate reproducible and well-defined nanolaminate structures, which is exactly what was intended for the deposition thermoelectric films on patterned substrates.

The mechanism of ALD is mainly based on alternate pulsing of precursor gaseous vapors onto the substrate and subsequent chemisorption and surface reaction of reactants [73]. In the ALD system, the precursor gas molecules are injected onto the substrate separately. They fill the reaction chamber independently step by step. The principle of ALD is illustrated as follows, taking the synthesis of Al_2O_3 as an example. The commonly used precursors for ALD Al_2O_3 synthesis are trimethylaluminum (TMA) and H_2O , which were first used as early as the late 1980s [73]. The surface chemistry of the Al_2O_3 ALD process can be described by the reactions (12) and (13):



where the asterisks denote the surface species [73].

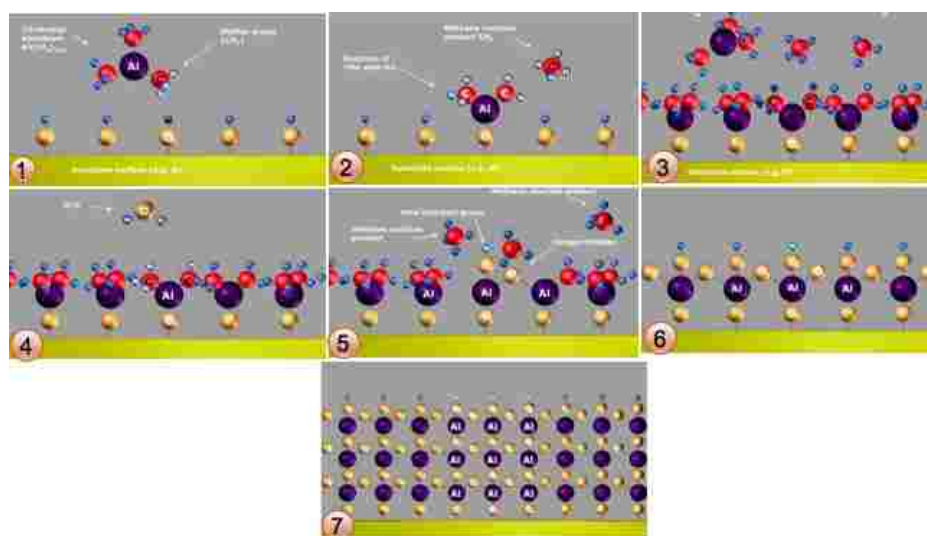


Figure 16. Schematic representation of the process of ALD layer by layer growth of Al_2O_3 [74].

Figure 16 clearly shows the individual steps of ALD Al_2O_3 growth utilizing water and TMA as ALD precursors. In step one, the substrate is exposed to the water vapor, forming a saturated hydroxyl terminated layer on the substrate surface. After formation of a monolayer, the excess water vapor is pumped away. Then the second precursor, TMA, is injected into the chamber. TMA reacts with the absorbed hydroxyl groups, producing methane as the reaction by-product. TMA does not react with itself; TMA will continuously react with hydroxyl groups until every available surface is passivated and then it is self-terminated. This ensures perfect uniformity of ALD deposited films, and the excess TMA will be pumped away together with the methane reaction by-product by purging nitrogen gas. After the TMA and methane reaction by-product is pumped away, water vapor is pulsed into the reaction chamber. Water vapor reacts with the dangling methyl groups on the new surface forming Al-O-Al bridges and hydroxyl surface groups. After the completed reaction, the surface is passivated with the Al-OH group, waiting for the next TMA pulse cycles. Methane was the by-product and will be pumped out from the chamber. Excess water vapor does not react with the hydroxyl surface groups, again causing perfect passivation to one atomic layer. One TMA vapor pulse and one water vapor pulse form one ALD cycle. This ALD cycle process can be repeated n times to obtain the desired thickness of the deposited films. The final film thickness is obtained from depositing n-times one monolayer.

For the ALD growth of PbTe/PbSe films, lead bis(2,2,6,6-tetramethyl-3,5-heptanedionato) ($\text{Pb}(\text{C}_{11}\text{H}_{19}\text{O}_2)_2$), (trimethylsilyl) telluride ($(\text{Me}_3\text{Si})_2\text{Te}$) and (trimethylsilyl) selenide ($(\text{Me}_3\text{Si})_2\text{Se}$) were employed as the chemical ALD precursors for lead, tellurium and selenium, respectively. The surface chemistry of the PbTe/PbSe ALD process can be described by reactions (14) and (15):





The solid lead precursor was volatilized at a temperature of 170 °C with 0.5 s pulse time; the liquid Te precursor required heating to 42 °C with 0.03 s pulse time, and the liquid Se precursor was kept at room temperature with a 0.03 s pulse time. 20 sccm inert N₂ was used as a carrier gas to transport the chemical precursors into the ALD reaction chamber. The ALD growth temperature of the PbTe and PbSe films was 150 °C. The chamber base pressure was kept at 30 mTorr. The substrates were pretreated with 10 wt% HF for 1 min to remove the native oxide layer. After rinsing in flowing DI water for 5 min, the substrates were then dipped into H₂O₂/H₂SO₄ (volume ratio: 1:4) mixed solution for 5 min to achieve a saturated hydroxyl OH⁻ terminated surface on the substrate, which provided the nucleation sites in order to promote the surface chemisorption of the ALD telluride and selenide thin films. The substrates were then rinsed in flowing DI water for 5 min and blow-dried with nitrogen gas. All the chemicals were obtained from Sigma Aldrich and were used without further purification.

2.2 Seebeck Coefficient Measurements

The Seebeck effect utilizes temperature differences between different conductors or semiconductors to generate a voltage, which in turn is used to generate electricity [26]. The Seebeck coefficient is an intrinsic materials property that describes the voltage (ΔV) developing from a given temperature difference (ΔT) in a thermoelectric material, ($S = \Delta V / \Delta T$). The Seebeck coefficient is an intrinsic property of thermoelectrical materials that has no special relationship with the sample dimension or geometry for homogeneous materials. However, the Seebeck coefficient is dependent on the measurement position for inhomogeneous materials. As

mentioned in chapter 1, in n-type thermoelectric materials, the electrons move from the hot side to the colder side. The resulting charge transfer develops an electric field between the two sides of the sample, which leaves the positive charge on the hotter side. On the other hand, in p-type thermoelectrical materials, the holes move from the hot side to the cold side, leaving the negative charge on the hotter side. Therefore, based on the definition of the Seebeck coefficient, it is positive for p-type materials, while it is negative for n-type materials [75].

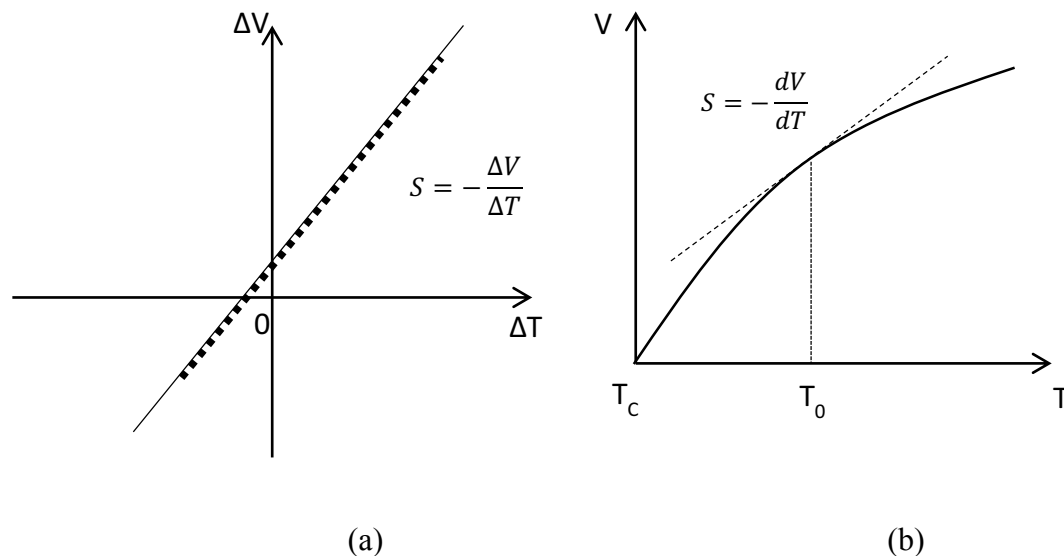


Figure 17. Illustration of the two basic Seebeck coefficient measurement methods based on (a) differential and (b) integral method [76].

To measure the Seebeck coefficient, there are two basic techniques: the integral and the differential methods [76]. In the integral method, one end of the sample is usually held at a fixed temperature (generally room temperature or 273K), while the other end of the sample is varied through the temperature range of interest. The temperature range is usually large, and the dependence of the Seebeck coefficient on temperature is nonlinear, as shown in Figure 17. The

Seebeck coefficient at the selected temperature is defined as the derivative of the voltage-temperature curve. This method is normally applied for long metal wire materials and assumes the temperature between the thermocouple junction and the sample is reached at thermal equilibrium with no delay between the voltage and temperature measurements [76].

$$S = -\frac{dV}{dT} \quad (16)$$

In the differential method, a small temperature gradient that is near the temperature of interest is applied across the sample to generate the Seebeck voltage. Therefore, the Seebeck coefficient is given by $S = -\frac{\Delta V}{\Delta T}$. The value of temperature difference is kept small to obtain accurate measurement. Several data points of varying temperature difference are collected, and the Seebeck coefficient is given by the slope of the Seebeck voltage with the temperature difference.

Seebeck coefficient measurements of thermoelectric films can be performed principally in two directions: in the horizontal in-plane direction and in the vertical direction perpendicular to the film surface. The thermoelectrical properties along these two directions are usually different due to crystal lattices structure and anisotropy [15]. Using the superlattices structure as an example, in the vertical direction of superlattices, electrons and phonons may experience much stronger interface scattering compared to the horizontal direction. In addition, the thermionic emission process may improve thermoelectric energy conversion efficiency along the cross-sectional direction [77]. For the case of thin films and when the thermoelectric material is fully isotropic, the Seebeck coefficient in the vertical direction can be indirectly measured by measuring in the horizontal in-plane direction, which is easier to accomplish experimentally. For bulk materials and superlattice structured samples, the cross-sectional measurement of the Seebeck coefficient is usually applied. For thin films with high isotropy, Seebeck coefficient measurement in the horizontal direction is commonly applied.

Seebeck coefficient measurement in horizontal direction

In this thesis work, the Seebeck coefficients of TE films in the horizontal direction were measured using an MMR Seebeck measurement system. The sample under test and a reference sample (made of constantan) were mounted symmetrically on a Seebeck stage in the MMR Seebeck system and were then contacted with leads, as shown in the right-top image in Figure 18 (b). The heater insert on top of the test stage was computer controlled to heat up the temperature of the hot side, while the cold side was attached to the MMR solid-state refrigerator. These two sides were thermally isolated as shown in the bottom image in Figure 18 (b). There are two pairs of thermocouples on the MMR Seebeck stage; one consists of copper with the sample under test, and the other one is copper with constantan. The Seebeck coefficient was measured differentially by applying a small temperature gradient between the heater and the MMR refrigerator. The voltage response of a particular temperature gradient of the sample under test and of the reference sample were recorded as V_1 and V_2 . Since the temperature differences between the two sides of the sample and the reference sample were the same, the Seebeck coefficient of the sample can be calculated as:

$$S_1 = S_{ref} \left[\frac{V_1(P)}{V_2(P)} \right] \quad (17)$$

where P is a specific heating power setting, S_1 and S_{ref} are Seebeck coefficient of the sample under test and the reference sample. To eliminate equipment error and voltage offset, the calculation of the Seebeck coefficient of the sample is modified by collecting the voltage response at two different heater power settings (P_1 and P_2), using the following equation:

$$S = S_{Ref} \left[\frac{V_1(P_1) - V_1(P_2)}{V_2(P_1) - V_2(P_2)} \right] \quad (18)$$

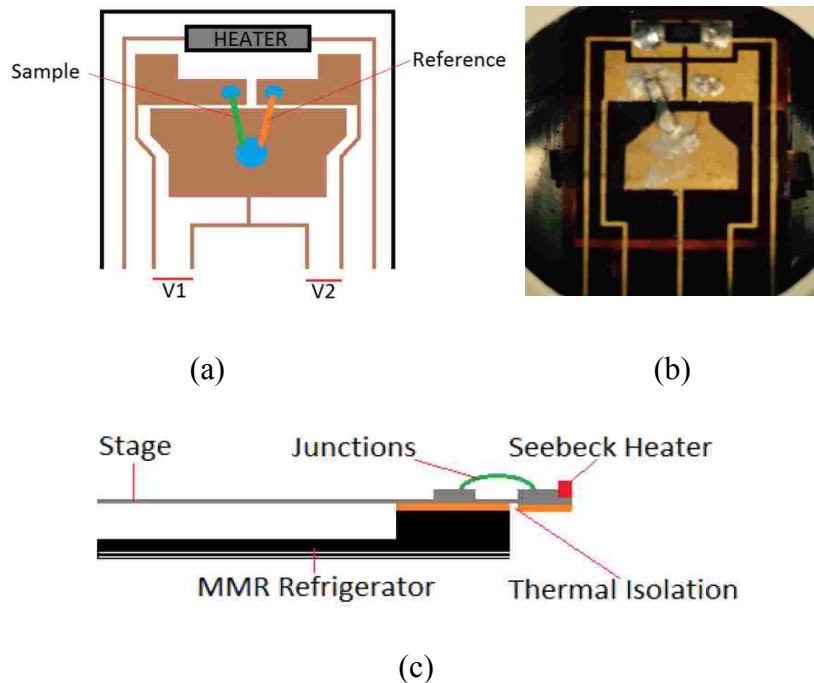


Figure 18. (a) Schematic top view of Seebeck stage in MMR Seebeck measurement system; (b) Real photographic image of symmetrically mounted DUT sample and reference sample on the stage; (c) Cross-sectional image of Seebeck stage attached with MMR refrigerator. Copyright of Figure (a) and (c) from WWW.MMR-TECH.COM.

For the Seebeck measurements, the ALD thermoelectric sample was cleaved into a small sized rectangle with a 1 mm width and a 5 mm length. Since lead chalcogenide is easily oxidized in air at room temperature, the surface lead oxide layer inhibited Ohmic contacts and instead Schottky diode type exponential I-V behavior between electrodes and the sample was observed. The presence of a surface lead oxide on our PbTe and PbSe thermoelectric samples therefore affects the Seebeck measurements. In order to achieve good Ohmic contacts, the PbTe and PbSe samples were pre-treated by two methods: (a) hydrogen reduction and (b) mechanical scratching of the two ends of the sample. Following these two treatments, the best Ohmic contacts were

achieved by the latter method and by sputter coating Au contact pads on the two ends of the sample. The thickness of the Au contact pads is around 100 nm. Afterwards, the thermoelectric ALD samples with the sputtered electrodes were mounted on the MMR Seebeck stage and contacted with silver paste, as indicated in Figure 18 (b).

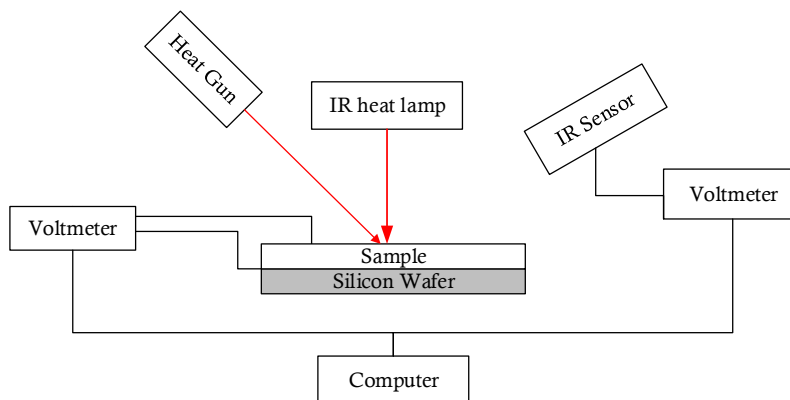


Figure 19. Schematic diagram of the experimental set-up for measuring Seebeck coefficient in vertical direction.

Seebeck coefficient measurement in vertical direction

The Seebeck coefficient in the vertical direction of the samples was measured at MicroXact, Inc. Figure 19 displays a schematic diagram of the set-up used to measure the Seebeck effect in the vertical direction. There are two heat sources: a heat gun and an infrared heat lamp. The temperature at the surface of the sample was measured at a 10 Hz rate with an OS136-1-K infrared temperature sensor available from Omega. The temperature sensor supplied a voltage measured with a Keithley 2100 digital multimeter and recorded by LabVIEW on a laptop. A Keithley 2182a nanovoltmeter was used to measure the thermoelectric response of the sample to

the applied heat with the results being recorded on the computer through LabVIEW. Gold contact pads have been evaporated onto the sample allowing for multiple measurement points.

2.3 Hall Effect Measurements

An Ecopia Hall Effect Measurement System was used to detect electrical conductivity of the sample based on the Van der Pauw method. During test, the current was introduced through one side, and the voltage response from the opposite side was recorded to calculate sheet resistance. For the hall coefficient measurements, a magnetic field was applied, introducing a diagonal current to measure the diagonal voltage response to calculate the sheet carrier density. Figure 20 shows the schematic diagram for the principle of resistivity and Hall coefficient measurements.

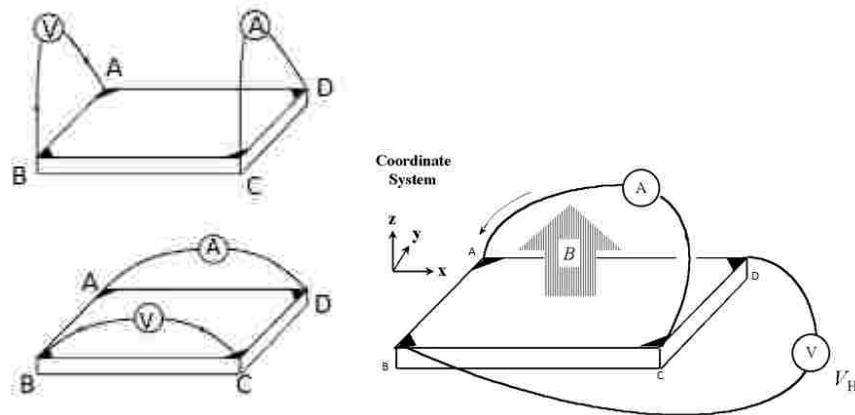


Figure 20. *Schematic diagram of the Van der Pauw contact method for Hall Effect measurements [78].*

There are four point contacts marked as A, B, C, and D. During testing, a current was

introduced flowing along DC edge (I_{DC}), the voltage across AB side (V_{AB}) is measured to calculate resistance $R_{DC, BA}$ by $R_{DCBA} = V_{AB}/I_{DC}$, which is considered as resistance along the y-direction (R_y). For precise measurements, the reciprocal resistance R_{ABCD} is calculated by $R_{BADC} = V_{DC}/I_{AB}$ to average the result. After measuring the resistance along the x-direction R_x , the sheet resistance of the sample with arbitrary shapes can be determined by Eq. 19.

$$\begin{aligned}
 e^{-\pi R_y/R_s} + e^{-\pi R_x/R_s} &= 1 \\
 R_y &= (R_{DCBA} + R_{BADC})/2 \\
 R_x &= (R_{DABC} + R_{BCDA})/2
 \end{aligned} \tag{19}$$

For the Hall coefficient measurements, two sets of measurements were conducted. One is under a magnetic field in positive z-direction, and the other one is under negative z-direction magnetic field. For each set, the diagonal voltage response under diagonal current input was recorded. Once we get sheet resistance and sheet carrier density, we can calculate carrier density, mobility and electrical conductivity of the film as long as we know the thickness of the film.

$$\begin{aligned}
 V_{AC} &= V_{AC,P} - V_{AC,N} \\
 V_{BD} &= V_{BD,P} - V_{BD,N} \\
 V_{CA} &= V_{CA,P} - V_{CA,N} \\
 V_{DB} &= V_{DB,P} - V_{DB,N}
 \end{aligned} \tag{20}$$

$$V_H = \frac{V_{AC} + V_{BD} + V_{CA} + V_{DB}}{8} \tag{21}$$

$$n_s = \frac{IB}{q|V_H|} \tag{22}$$

Where R_s is sheet resistivity, n_s is sheet carrier density, V_H is the Hall voltage, I is the input current, and B is the magnetic field.

All the electrical properties measurements were performed with an Ecopia Hall effect measurement system (HMS-5300) using the Van der Pauw sample configuration. The Hall system is equipped with a 0.55 T permanent magnet, and variable temperature test is available from 80 K to 550 K. Liquid nitrogen was used to cool down the system to the desired initial test temperature. In the experiment, square-shaped $1\text{ cm} \times 1\text{ cm}$ samples were prepared for the measurements. The four electrical contacts are either soldered InSn or sputtered Au on the four corners with size of less than $1 \times 1\text{ mm}^2$. For the Au contacts, the size of Au pads is generally less than $1 \times 1\text{ mm}^2$ in area and with a thickness of 100 nm. Figure 21 displays a photographic image of the Hall measurement stage and another image of a sample with the four sputtered Au contacts.

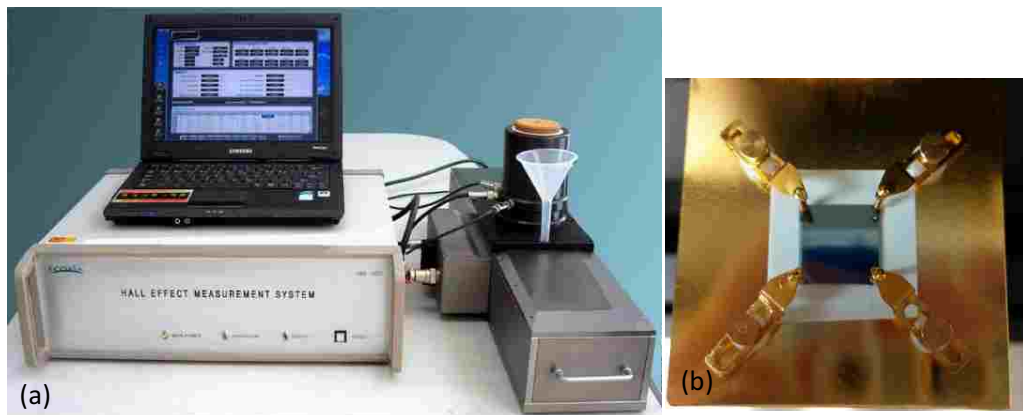


Figure 21. (a) Photographic image of the Ecopia Hall measurement system. (b) The Hall measurement stage mounted with a sample using Van der Pauw contact configuration.

2.4 Thermal Conductivity Measurements

In-plane direction measurement

The 3-Omega technique is the most commonly used method to accurately measure the in-plane thermal properties of thin film materials, which can also be used to measure the thermal

diffusivity and effusivity of materials directly. Figure 22 illustrates the principle of the 3ω method for thermal conductivity measurements. Generally, an alternating current at angular frequency 1ω is applied through a metal line, creating Joule heating at 2ω . The periodic heating generates a temperature wave that spreads through the surrounding material, which is oscillated at 2ω but delayed in phase ϕ (i.e., the phase lag). This relationship is shown as the temperature equation in Figure 22. The oscillation amplitude of the temperature wave at the heating source is dependent on the properties of the material. The Resistance oscillates at 2ω and causes a voltage oscillation at 3ω . The 3ω voltage amplitude is directly measurable and provides information on the thermal environment of the heater.

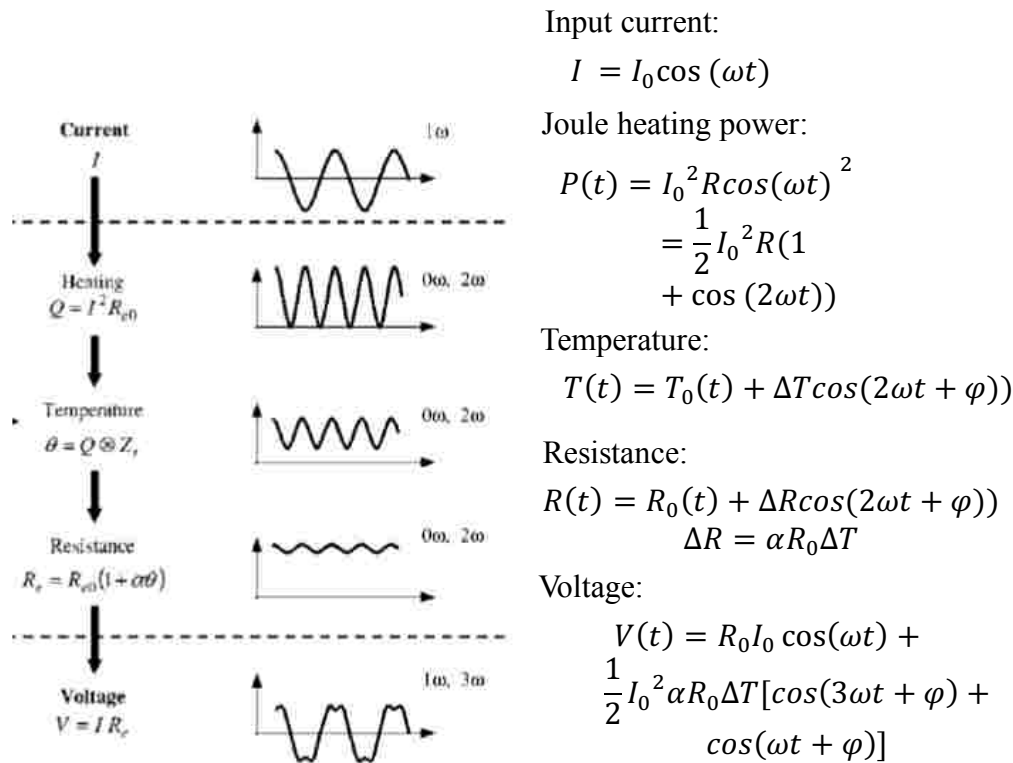


Figure 22. Principle of 3ω method for in-plane thermal conductivity measurement of films [79].

Vertical direction thermal conductivity measurement

The vertical direction Thermal conductivity is measured based on the Time Domain Thermo-reflectance (TDTR) technique. TDTR is a time transient, non-contact, optical thermometry technique that utilizes a pump-probe experimental configuration that uses a femtosecond (fs) laser system [80]. The principle behind this technique is that once a thin film material is heated up by a pump laser pulse, the change in the reflectance of the surface can be utilized to derive the thermal properties. The reflectivity is measured as a function of time, and the data received can be matched to a model with coefficients that correspond to thermal properties. The schematic diagram of thermoelectrical conductivity measurement is shown in Figure 23.

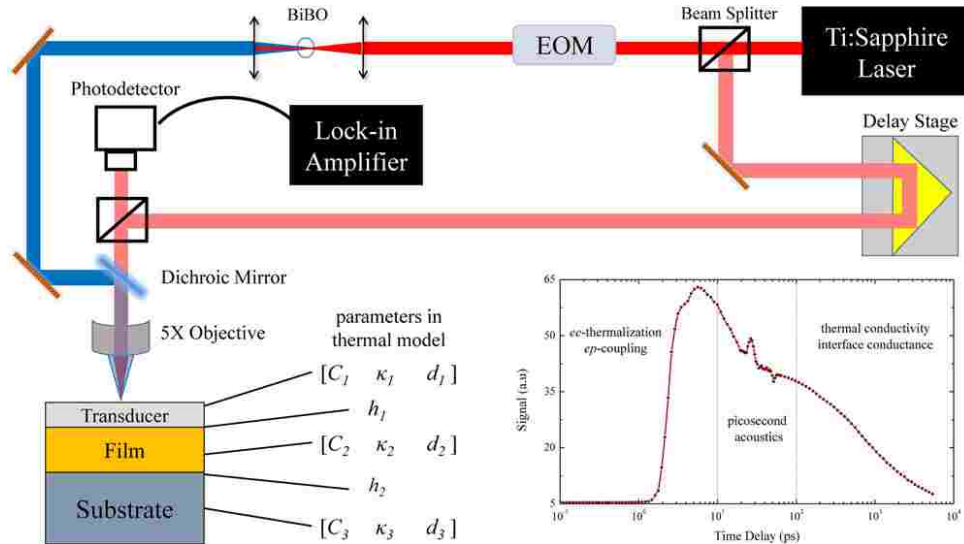


Figure 23. Schematic diagram of thermoelectrical conductivity measurement [81].

For the TDTR measurements, 83 nm \pm 3 nm of aluminum was deposited on top of the ALD thermoelectric nanolaminate samples by electron beam evaporation, acting as a transducer to transduce the optical energy from the TDTR laser pulses into thermal energy, and the temporal

decay of which was subsequently measured. A Ti-Sapphire femtosecond Spectra Physics Tsunami oscillator that emits ~ 100 fs pulses at a repetition rate of 80 MHz with a wavelength centered at ~ 800 nm (FWHM of 10.5 nm) was used as a laser source. The pulse was split into two beams: pump and probe beam by a half-wave plate followed by a polarizing beam splitter leading to a cross-polarized pump and probe beam. The Pump beam heats the surface of the thermoelectric thin film samples and the reflectivity of the aluminum changes linearly with the surface temperature. The Time delayed probe beam hits the sample at same spot and monitors the change in reflection. The probe beam is mechanically delayed in time by a translational mechanical delay stage up to 6 ns. The reflected intensity from the probe is measured by a balanced photodetector. The pump and probe spot sizes were focused down to $1/e^2$ radii of $14 \mu\text{m}$ and $7 \mu\text{m}$, respectively. A lock-in amplifier demodulates the signal and provides amplitude and phase data in the form of a thermal decay curve. The decay curves are fitted with a heat conduction model to obtain the thermal properties of the material.

CHAPTER 3

3. NANOSTRUCTURED PbTe/PbSe FILMS

The experimental implementation of our novel phonon engineering concept by nanostructuring of ALD PbTe/PbSe thin films to enhance the thermoelectric properties is described in this chapter. The ALD synthesis of PbTe/PbSe nanolaminate layers was performed in absolute conformal fashion on the inside walls of the pores of nano-structured porous Si templates replicating the porous template morphology. The PbTe/PbSe films, nanostructured by the template replication method, were subsequently benchmarked against identical ALD planar non-structured thermoelectric films deposited on planar Si substrates instead.

Physical analysis and surface characterization of the ALD thin film samples has been performed with FE-SEM, XRD, and AFM. The thermoelectric characterization was performed in the horizontal in-plane direction with Seebeck coefficient measurements, and electrical conductivity measurements of the ALD PbTe/PbSe nanolaminate structures. However, due to the experimental constraints, the thermal conductivity can only be measured in the vertical direction through the film thickness by the TDTR method as explained in the schematic of Figure 23. In addition, in the second approach the effect of stripe patterned silicon substrates on the thermoelectric properties of conformal ALD PbTe/PbSe films was investigated and is discussed in this chapter.

3.1 Conformal ALD PbTe/PbSe Nanolaminate Deposition on Porous Si Templates

Multiple layered PbTe/PbSe nanolaminates were fabricated by alternately depositing PbTe and PbSe layers first on regular planar bulk silicon wafers, and second for direct comparison and benchmarking also inside the myriad pores of porous silicon templates using thermal ALD technology. The ALD film deposition recipe and the experimental conditions for ALD deposition was described in detail in chapter 2. PbTe/PbSe nanolaminates with film thickness of roughly 10 nm for each PbTe and PbSe layer were prepared, and the evaluation is described in the following section.

Surface Characterization

The crystal structure of the synthesized ALD films was analyzed by X-ray Diffraction (XRD). Figure 24 displays the XRD plot of 1000 ALD cycles of PbTe, 1000 ALD cycles of PbSe, and double layer PbTe/PbSe (10 nm / 10 nm) nanolaminate structure grown at 150 °C. The experimentally obtained diffraction peaks for PbTe and PbSe can be indexed into the cubic structure of the PbTe phase [space group: $Fm\bar{3}m(225)$] and PbSe phase [space group: $Fm\bar{3}m(225)$], which is consistent with the NIST X-ray data files PDF 78-1904 and PDF 06-0354, respectively. The highest peak in the XRD pattern indicates preferential growth of PbTe and PbSe along the (200) crystal direction, resulting from the lowest surface energy in comparison with other orientations. The lattice constant of PbTe and PbSe can be calculated by two formulas based on Bragg's law: $\lambda = 2d\sin\theta$, and $a^2 = (h^2 + k^2 + l^2)d^2$. The three letters h, k, and l are Miller indices, and a, d, λ and θ are lattice constant, interspace between two adjacent planes, and X-ray wavelength and incident angle of the X-ray, respectively. For (200) crystallographic direction, the lattice constants of PbTe and PbSe are 6.397 Å and 6.159 Å, which are compatible with reported

values 6.438 Å and 6.128 Å, respectively. The lattice mismatch between PbTe and PbSe corresponds to $\Delta \frac{a}{a} = 3.8\%$, exhibiting a slight lattice mismatch.

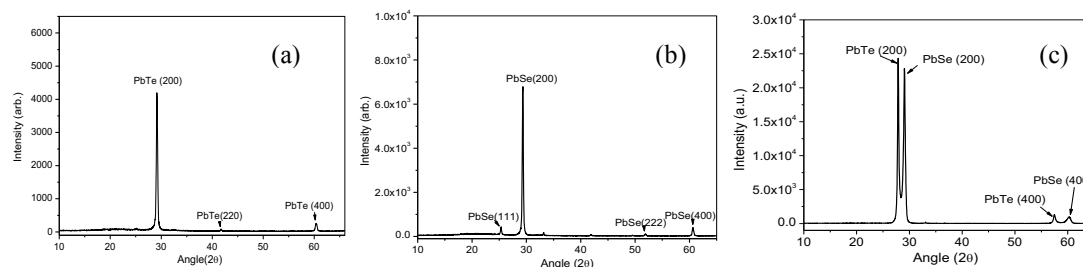


Figure 24. XRD plot of (a) 1000 ALD cycles of PbTe, (b) 1000 ALD cycles of PbSe, and (c) double layer PbTe/PbSe (10 nm/ 10 nm) nanolaminate deposited at 150 °C.

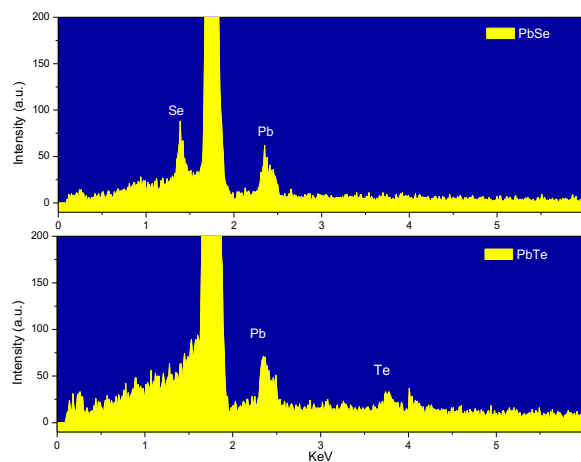


Figure 25. Energy dispersive X-ray Spectroscopy analysis (EDS) of PbSe film deposited with 1000 ALD cycles and of PbTe samples grown with 1000 ALD deposition cycles.

The composition and stoichiometry of the samples were observed by energy dispersive X-ray spectroscopy analysis (EDS), as shown in Figure 25. The result from EDS reveals the chemical element composition in PbTe and PbSe films grown at 150 °C with 1000 ALD deposition cycles.

Table 1 lists the element compositions in PbTe and PbSe samples. Both PbTe and PbSe are slightly non-stoichiometric being Pb rich, which indicates the PbTe and PbSe films are n-type semiconductors and electrons are the charge carriers [16]. This was further corroborated by subsequent Seebeck coefficient measurements. The strongest peak at 1.8 KeV identifies the Si substrate.

Table I

The composition of lead, tellurium and selenide in PbTe and PbSe films.

| Samples | Pb (Weight %) | Te (Se) (Weight %) | Pb (Atom %) | Te (Se) (Atom %) |
|--------------------------|------------------|-----------------------|----------------|---------------------|
| PbTe (1000cys-170 °C) | 6.53±1.61 | 1.98±0.22 | 0.86±0.21 | 0.42±0.05 |
| PbSe (1000cys-170 °C) | 12.07±0.81 | 3.68±0.26 | 1.88±0.13 | 1.5±0.1 |

Our previous research reported the ALD growth of PbTe and PbSe follows the Volmer-Weber island growth mode[82]. Figure 26a displays the surface morphology of PbTe films on planar silicon wafers without any pre-treatment grown with 1000 ALD deposition cycles. The nucleated PbTe islands are isolated and exhibit random size and orientation, which is also can be seen in TEM cross-section images in Figure 27 (a) and (b), nucleating in a Volmer-Weber type of island growth mode.

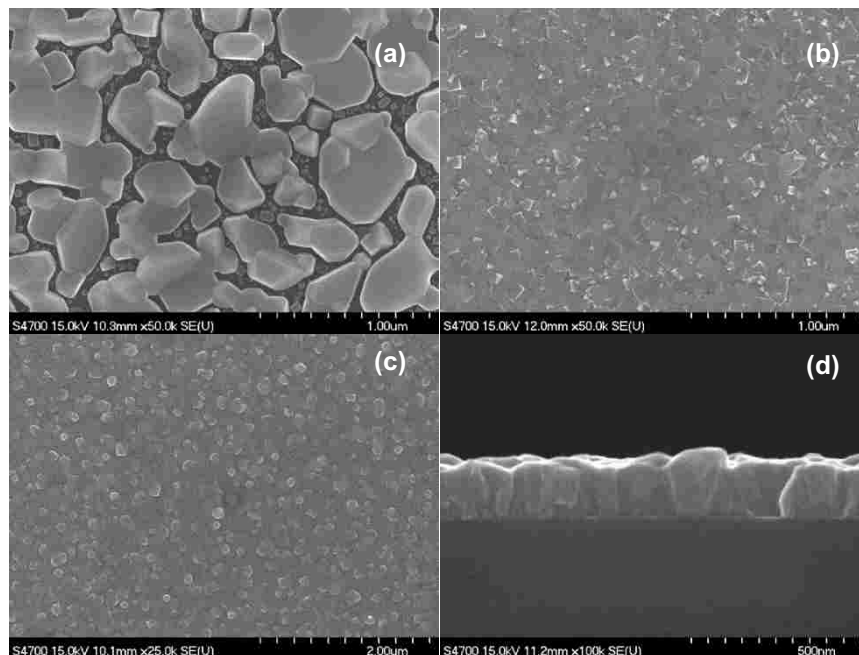


Figure 26. FE-SEM micrographs of (a) 1000 ALD deposition cycles of PbTe film without pre-treating the Si substrate, (b) 1000 ALD deposition cycles of PbSe film grown on hydroxyl OH terminated Si substrate, (c) PbTe/PbSe (10/10 nm) nanolaminates, (d) Cross-section image of PbTe/PbSe (10/10 nm) nanolaminates.

To achieve complete coverage, we pre-treated substrates as described in the experimental section in order to add hydroxyl termination (OH^-) on the surface of the silicon substrate to enhance chemisorption of the Te and Se chemical precursors. Complete and conformal surface coverage with PbSe films of pre-treated silicon wafers was achieved starting at a thickness of 1000 ALD deposition cycles and above, which is displayed in Figure 26b. The initially isolated nucleated PbSe islands finally coalesce and combine tightly into a continuous TE film, which is required for practical device applications. Figure 26c shows the surface morphology of a nanolaminate composite structure consisting of 9 bi-layers of PbTe/PbSe (each of 10/10 nm) synthesized at 150 °C on pre-treated planar bulk silicon substrates. The FE-SEM micrographs exhibit complete

surface coverage of the planar silicon wafer with granular PbTe/PbSe nanolaminate layers. The ALD growth of the PbTe and PbSe films still follows the Volmer-Weber island growth mode but with increasing film thickness the isolated nucleated islands coalesce together, which can be seen clearly in the SEM cross-sectional image of the PbTe/PbSe nanolaminate structure in Figure 26d and TEM cross-sectional image shown as in Figure 27c. This may be attributed to the saturated nucleation sites on the surface of the pre-treated Si substrate. The thickness of the entire thermoelectric nanolaminate structure is about 200 nm.

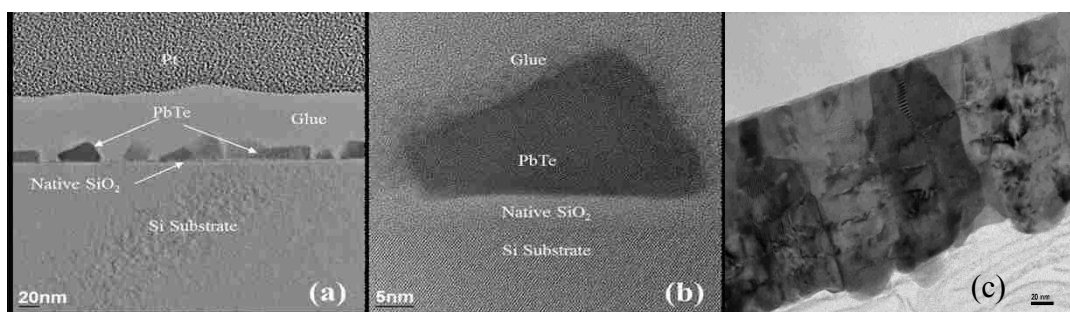


Figure 27. (a) TEM cross-sectional images of (a) (b) ALD deposited PbTe film of 700 ALD cycles grown at 170 °C on Si substrate highlighting the cubic PbTe crystallites in the initial nucleation phase [83], and (c) featuring thicker PbTe/PbSe (10/10 nm) nanolaminate layers when all the initial nuclei have finally coalesced into continuous compact layers grown on a Si substrate at 150 °C.

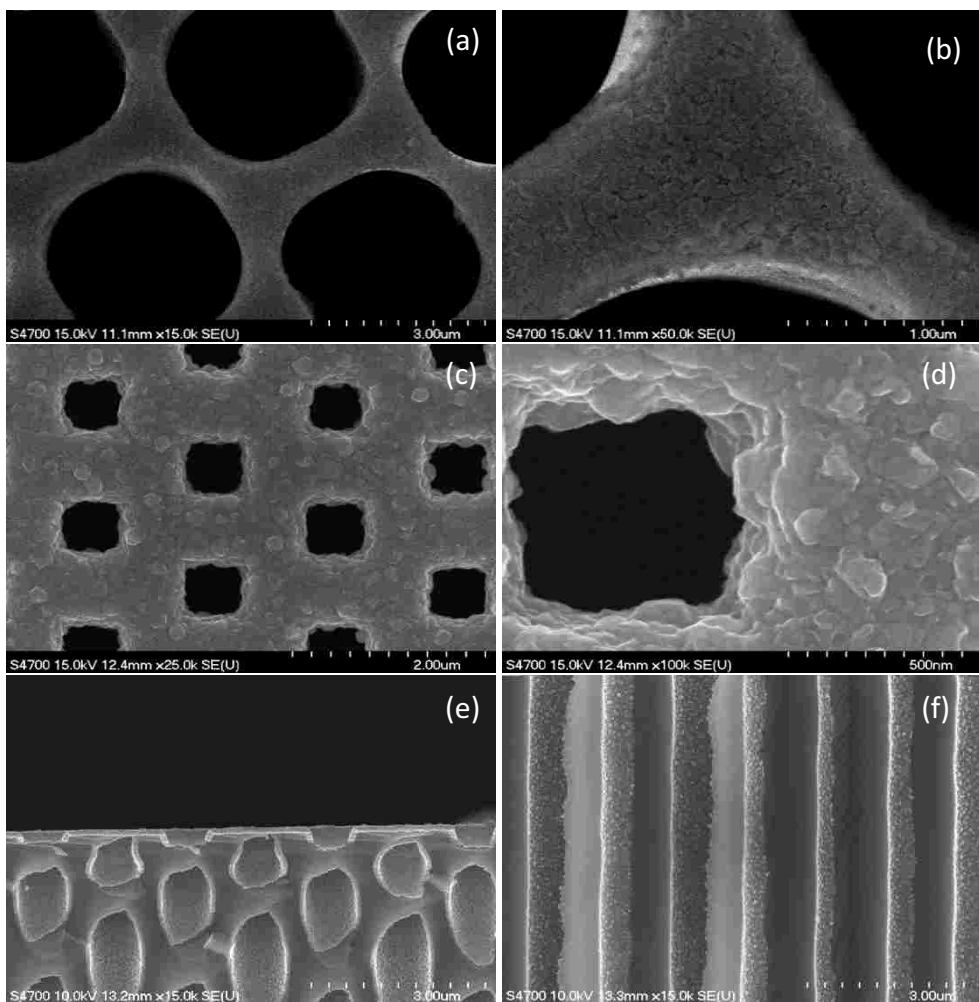


Figure 28. FE-SEM images of PbTe/PbSe (10/10 nm) nanolaminates grown on porous Si substrate with pore size of 3 μm . (a) at 15k magnification (b) at higher magnification of 50k (c) The misaligned staggered square pores are 700 nm x 700 nm and are horizontally spaced 1.72 μm apart, and 0.6 μm vertically apart. FE-SEM images and of PbTe/PbSe (10/10 nm) grown on porous Si templates. (d) FE-SEM images of PbTe/PbSe (10/10 nm) nanolaminates deposited at 150 $^{\circ}\text{C}$ on porous Si substrate. (e) and (f) are cross-sectional images of PbTe/PbSe nanolaminates with period of 10 nm.

The FE-SEM micrographs of the PbTe/PbSe (10nm/10nm) nanolaminate structure grown on microporous Si membranes at 150 °C are illustrated in Figure 28. There are two kinds of porous Si substrates with different pore sizes used for the phonon engineering experiments. One porous template contains misaligned round square pores with a 600 nm-thick pore wall and pore diameter of 3 μm. The other variety of Si porous templates contains misaligned square pores with smaller pore size, characterized by an almost square pore size of 700 nm, with pore walls of 700 nm, and the pores are horizontally spaced 1.72 μm apart and 0.6 μm vertically apart. Figure 28 (a) and (b) shows the FE-SEM images of double layer PbTe/PbSe (10/10 nm) nanolaminates grown on porous Si templates with larger misaligned staggered round square pores. In contrast, Figure 28 (c) and (d) displays FE-SEM images of PbTe/PbSe (10/10 nm) nanolaminates deposited on porous Si templates with considerably smaller misaligned, staggered square pores. The cross-sectional images of PbTe/PbSe nanolaminates grown on the misaligned staggered square porous Si substrate with period of 10 nm are shown in Figure 28 (e) and (f). The ALD PbTe/PbSe films cover both planar Si and porous Si templates completely, conformally and uniformly, and coat absolutely conformal the inside of the porous Si walls. The average grain size of the ALD PbTe/ PbSe films is $\sim 108 \pm 10$ nm. Figure 26 demonstrates complete coverage of the inside pore walls with ALD PbTe/PbSe nanolaminate films. In this micrograph, the top surface of the pore sidewalls is imaged. This further highlights the significant advantage of ALD technology for coatings of complex 3-D surface morphologies and high aspect ratio pores in porous templates. Figure 29 illustrates a 3-D AFM image of the PbTe/PbSe (10nm/10nm) nanolaminate structure grown at 150 °C on a planar Si test substrate. The surface roughness is 11.37 nm, which indicates that a relatively smooth surface was achieved.

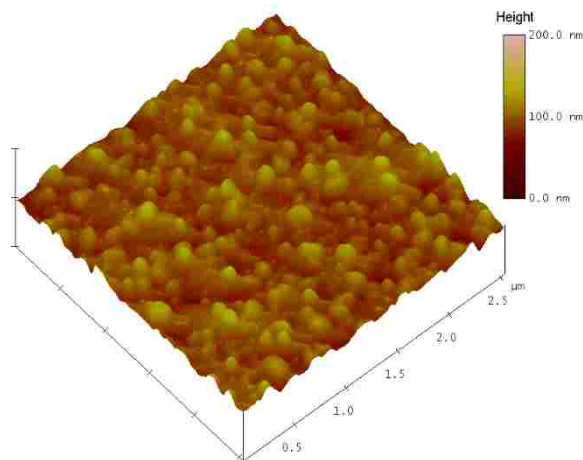


Figure 29. *AFM images of PbTe/PbSe (10/10 nm) nanolaminates deposited at 150 °C on a planar silicon substrate.*

To illustrate the effect of the micro-porous silicon template on the thermoelectric properties, we measured the Seebeck coefficient, the electrical conductivity, and the thermal conductivity for PbTe/PbSe nanolaminates grown by ALD on both bulk silicon wafers and micro-porous silicon templates.

Seebeck Coefficient Measurements

The Seebeck coefficient in the horizontal direction was measured by an MMR Seebeck measurement system. The measurements were conducted over a temperature range from 300 K to 500 K and then back-traced from 500 K to 300 K. The same measurement sequence was repeated again overnight.

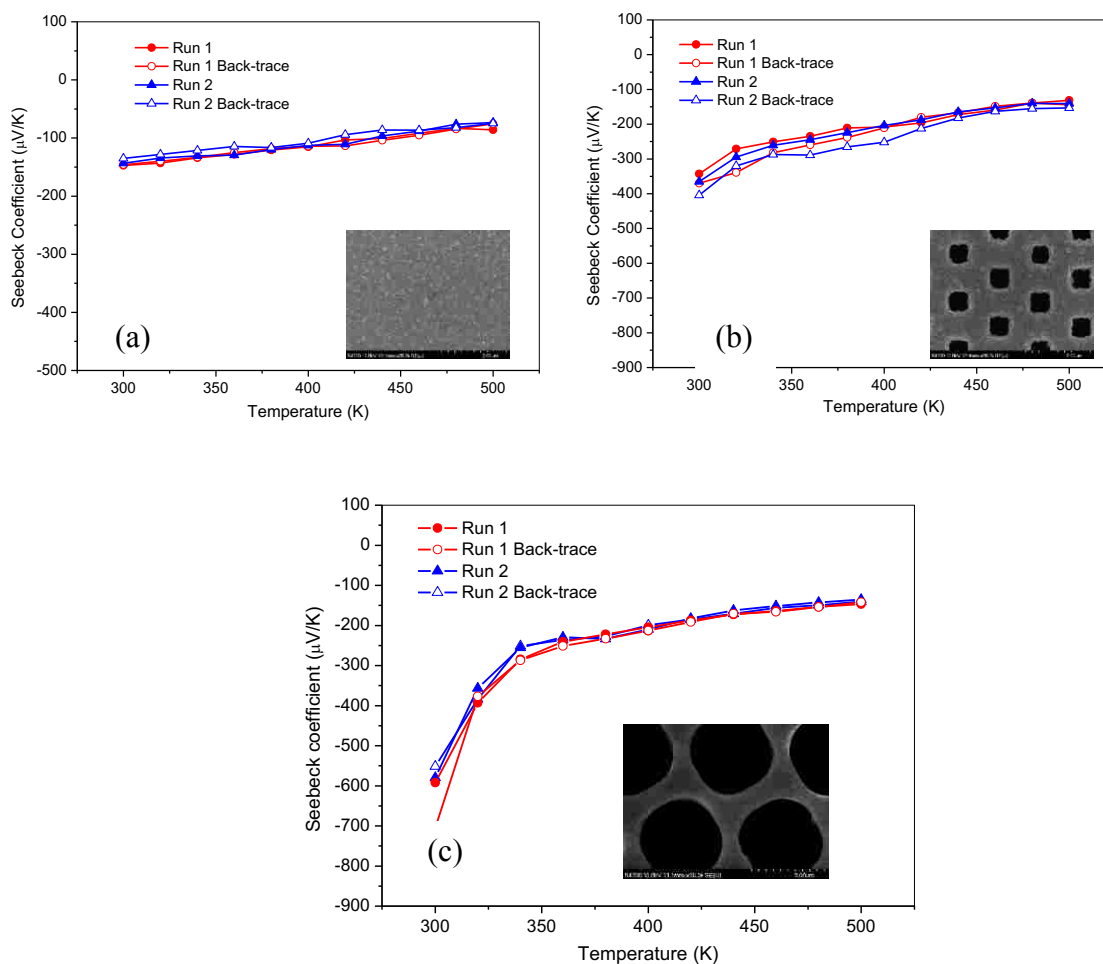


Figure 30. Plot of Seebeck coefficient as a function of temperature of 9 bi-layers of ALD PbTe/PbSe (10/10 nm) nanolaminates deposited on (a) planar Si substrate and (b) microporous silicon template with small square shaped pores (c) porous silicon template with thinner pore wall and larger pore diameter measured by MMR Seebeck measurement system. The measurements were conducted in the temperature range of 300 ~500 K.

Figure 30 (a) displays the temperature dependence of the Seebeck coefficient for PbTe/PbSe nanolaminates grown on planar silicon wafers. The maximum value of $143.016 \pm 5.500 \mu\text{V/K}$ for the Seebeck coefficient of the PbTe/PbSe film on planar Si substrates was found at 300 K. As the temperature increases from 300 K to 500 K, the Seebeck coefficient decreases

almost linearly. The negative value of the Seebeck coefficient indicates electrons are the majority carriers in the PbTe/PbSe nanolaminates. On the other hand, the measured Seebeck coefficients of the thermoelectric ALD nanolaminates deposited on micro-porous silicon templates are shown in Figure 30 (b) and (c). The Seebeck coefficient of the sample synthesized on a micro-porous silicon template exhibits a similar temperature dependence compared to the sample deposited on a regular planar silicon substrate. The Seebeck coefficient decreases steadily from 300 K to 500 K. The maximum value of the negative Seebeck coefficient is $-370.556 \pm 37.750 \mu\text{V/K}$ at 300 K. The sample grown on the porous silicon template with thinner pore walls and larger pore diameter exhibits even higher Seebeck coefficients around $-574.239 \pm 20.790 \mu\text{V/K}$ at 300 K. The dependence of the Seebeck coefficient on temperature exhibits good agreement for both up-trace and down-trace measurements over the temperature range as well as high reproducibility. The negative value of the measured Seebeck coefficient is indicative of n-type material for the PbTe/PbSe nanolaminates.

It is noteworthy that the in-plane Seebeck coefficient for our PbTe/PbSe nanolaminate structure measured in porous Si membranes is about 2.5 times larger compared to the value obtained for planar bulk Si substrates. The enhanced Seebeck value is attributed to the presence of the regular array of etched out pores, which provides an additional periodic structuring of the nanolaminate composite sample, while the high porosity of the porous Si template simultaneously reduces simultaneously the thermal conductivity with more air than Si remaining in the template structure.

The Seebeck coefficient of all the thermoelectric ALD samples under test reaches a maximum value around room temperature. Our measured temperature dependence of the Seebeck coefficient is different from the reported value in reference [84], where the maximum Seebeck

coefficient occurs at 560 K. One reason for the discrepancy may be different thermoelectric film properties due to different deposition techniques. It is believed that the maximum Seebeck coefficient occurs when intrinsic conduction begins. However, our non-doped PbTe and PbSe films evidently have lower carrier concentration than the doped films in the literature, which consequently results in the onset of intrinsic conduction at a lower temperature [85].

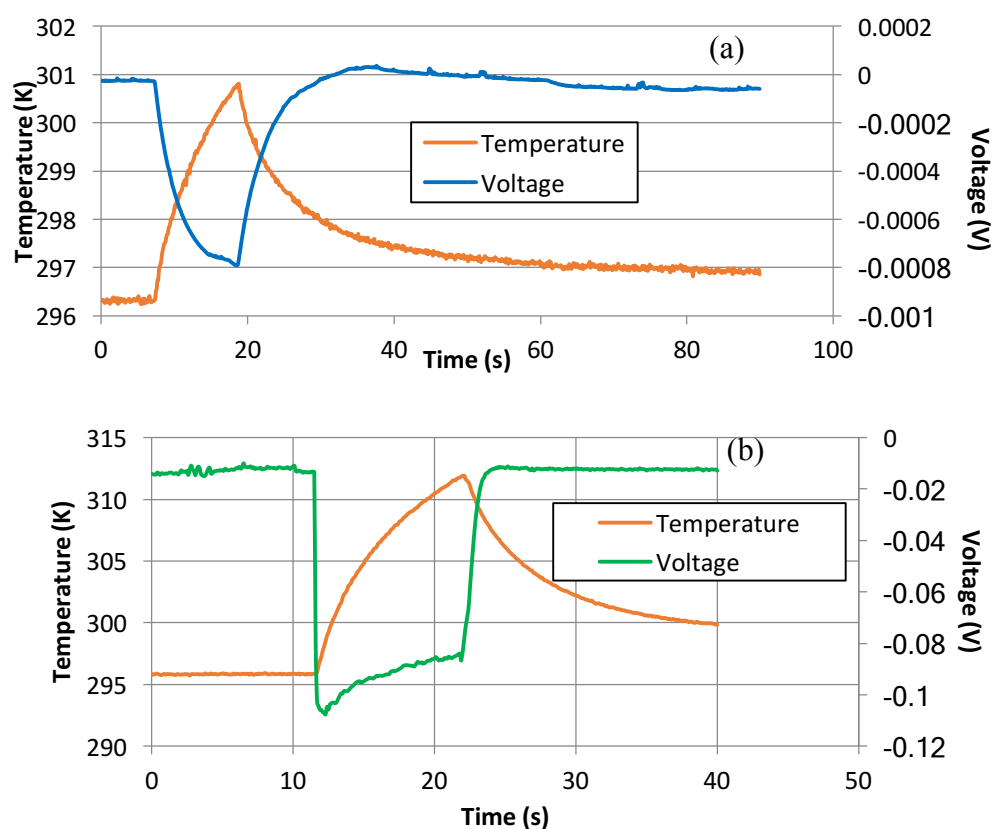


Figure 31. Voltage and temperature response to infrared heat pulse at room temperature for PbTe/PbSe (10 / 10 nm) (a) grown on planar Si substrates and (b) on porous Si templates.

For the Seebeck coefficient measurements in the direction vertical to the surface, our collaborator at MicroXact, Inc. measured similar trends and found that the PbTe/PbSe

nanolaminate structure grown on micro-porous silicon membranes exhibits even higher Seebeck coefficients with values of $78670 \pm 15540 \mu\text{V/K}$ in the vertical direction compared with the thermoelectric nanolaminate structure grown on a planar bulk silicon wafer ($250 \pm 27 \mu\text{V/K}$) [86], as shown in Figure 31.

This porous Si membrane is fabricated by removing the Si from the backside with KOH etching until the pores are reached from the backside. From the results of our Seebeck measurements in both the horizontal and vertical directions, the low dimensional ALD thermoelectric nanolaminate structures synthesized inside the pores of porous silicon membranes exhibit higher Seebeck coefficients than previously reported values. This indicates that the added periodic surface structuring and the dimensions of the pore diameter and pore walls resulting from the photo-lithographically defined regular pore pattern of the porous Si membrane constitutes another crucial parameter to aid in further improving the Seebeck coefficient of TE materials. This is attributed to the lower thermal conductivity κ in porous Si membrane structures. The porous silicon membrane we used exhibits a staggered square porous configuration, which theoretically yields the lowest thermal conductivity compared to other porous configuration arrangements [65]. This is further confirmed in our thermal conductivity measurements, which is discussed in detail in later sections. Since the temperature gradient is the driving force for charge carriers moving from the hot side to the cold side, such a temperature gradient will be more lasting in a material with lower thermal conductivity, so that more charged carriers accumulate on the cold side leading to a larger voltage difference between the two sides, resulting in a larger Seebeck coefficient.

Electrical Conductivity Measurements

The electrical properties of the PbTe/PbSe nanolaminates structure grown on porous Si templates and planar Si substrates were measured with the Ecopia Hall measurement system. The measurements were conducted over the temperature range from 320 K to 500 K, with a permanent magnetic field of 0.55 Tesla. Figure 32 (a) plots the temperature dependence of the electrical conductivity for the thermoelectric ALD nanolaminates with a layer periodicity of 10 nm grown on planar Si wafers and porous Si templates. As the temperature increases from 320 K to 500 K, the electrical conductivity of both samples increases, exhibiting a classic semiconductor thermal behavior. The increased electrical conductivity is attributed to the fact that the carrier concentration increases at higher temperature, as shown in Figure 32 (b), and thermally generated carriers contribute to electrical conduction at high temperature. This is true for both planar substrates and porous patterned templates. The electrical resistance decreases exponentially with temperature. In addition, the nano-patterned thermoelectric ALD nanolaminates exhibit a lower electrical conductivity compared to non-patterned nanolaminates, which is similar to reported literature work [87]. The reduction in electrical conductivity in patterned samples is attributed to the electron scattering by the sidewall of the pores.

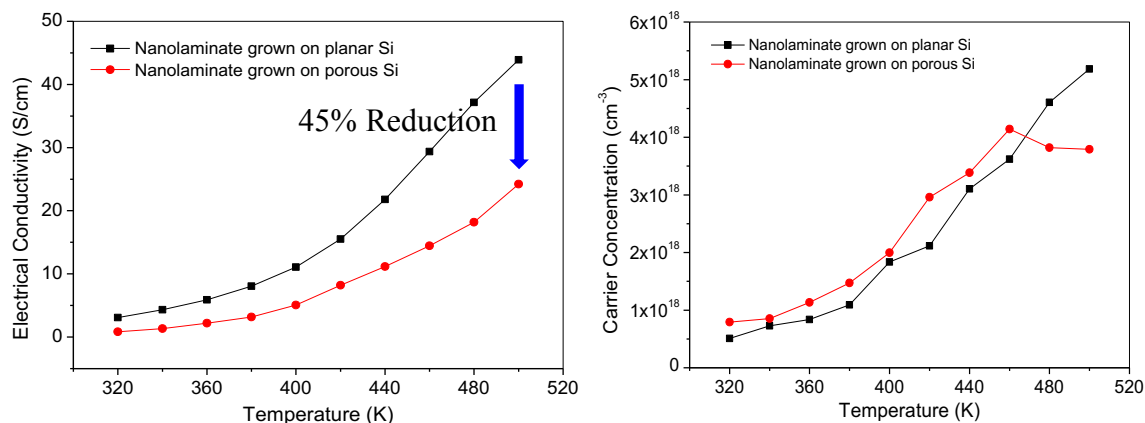


Figure 32. Plot of (a) electrical conductivity and (b) carrier concentration of the PbTe/PbSe (10/10 nm) nanolaminates grown on planar Si substrates (in black line) and porous Si templates (in red line) as a function of temperature.

Thermal Conductivity Measurements

In this dissertation work, the time domain thermo-reflectance (TDTR) method was applied to measure the vertical cross-plane thermal conductivity of a series of PbTe/PbSe nanolaminates with different layer periodicity. The PbTe/PbSe thermoelectric nanolaminates with 20 ALD cycles, 60 ALD cycles and 100 ALD deposition cycles per layer, which correspond to a thickness of 2 nm, 6 nm, and 10 nm per layer, were grown on planar silicon substrates and porous silicon templates by ALD technology. The total thickness of these three samples were 220 nm, 180 nm, and 175 nm, respectively.

Figure 33 displays the thermal conductivity of the PbTe/PbSe nanolaminates with three different layer periodicities grown on planar and porous Si substrates. In addition, the thermal conductivity values for single layers of PbTe, PbSe films grown on planar and porous Si substrates are also included in this plot. The graph demonstrates that the porous samples exhibit a lower thermal conductivity by nearly a factor of two compared to the planar samples. For all three planar

nanolaminates samples, thermal conductivity is around $1.3 \text{ Wm}^{-1}\text{K}^{-1}$, which is almost half that of PbTe and PbSe bulk materials ($\sim 2.5 \text{ Wm}^{-1}\text{K}^{-1}$). The reduced thermal conductivity can be attributed to the enhanced phonon-boundary scattering due to the introduced period boundaries within the nanolaminates. Surprisingly, the thermal conductivity of the nanolaminates didn't show much dependence on layer periodicity, which remains a constant for both porous and planar samples.

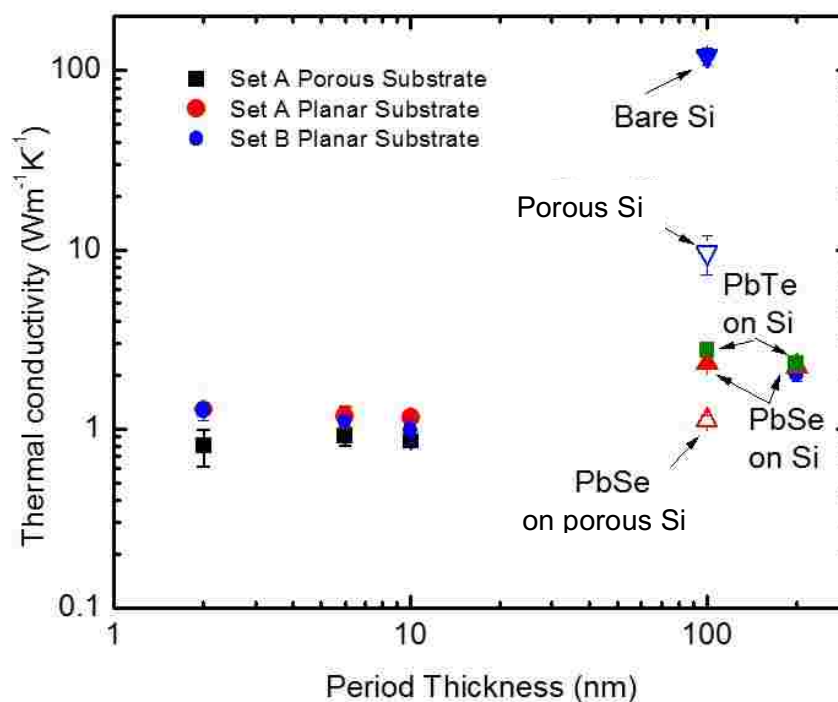


Figure 33. Thermal conductivity of the PbTe/PbSe nanolaminates with different layer periodicity grown on planar Si substrates and porous silicon templates, which is plotted on log-log scale.

In addition, the simulation result shown in Figure 34 indicates that the effective thermal conductivity of the ALD films conformally grown on porous Si templates will further decrease as the width of pore walls decrease [86]. The reason can be attributed to the fact that when the dimension of the substrate is further reduced approaching the nanometer range, the acoustic

phonons which have relatively longer mean free path (MFP) can be strongly scattered, and meanwhile the optical phonons with relatively shorter MFP will start to be scattered as well to further reduce thermal conductivity of the film.

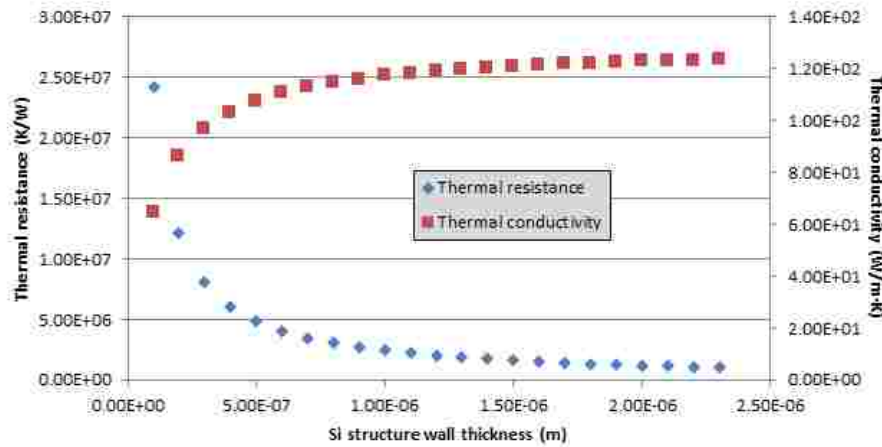


Figure 34. Simulation results of effective thermal conductivity of 100 nm thick PbTe/PbSe nanolaminate film on a porous Si substrate as a function of Si wall width [86].

The Figure of Merit ZT ($S^2\sigma T/\kappa$) of the ALD PbTe/PbSe nanolaminates can be calculated from our measured values of the Seebeck coefficient, electrical conductivity and thermal conductivity. In the study, there are two approximations applied to calculate the Figure of Merit ZT . First, since the Seebeck coefficient and electrical conductivity were measured along the horizontal in-plane direction while the thermal conductivity measured by the TDTR method was measured along the vertical direction instead, we assume the thermal conductivity of the nanolaminates is isotropic. This is an incorrect oversimplification. It is clearly apparent that in the case of porous substrates, there are many more interfaces and boundaries in the horizontal in-plane direction compared to the vertical direction. For this reason, the phonon scattering is expected to

be massively increased in the horizontal in-plane direction, where thousands of pores will be encountered resulting in even lower thermal conductivity. Therefore, using the oversimplifying approximation of isotropic thermal conductivity of the nanolaminates will underestimate the calculated ZT values and thus only strengthen our conclusions. Another approximation is the assumption that the thermal conductivity of the planar and porous thermoelectric nanolaminates is constant over the measured temperature range. For ZT calculation, the thermal conductivity values used for planar and porous PbTe/PbSe nanolaminates (10/10 nm) are $1.2 \text{ Wm}^{-1}\text{K}^{-1}$ and $0.8 \text{ Wm}^{-1}\text{K}^{-1}$, respectively. Figure 35 plots the ZT value for the PbTe/PbSe nanolaminates grown on planar and porous Si substrates as a function of temperature. It can be clearly seen that the porous sample has a higher ZT value than the planar sample. The ZT value of the nano-structured porous sample was enhanced by a factor of up to three at 500 K.

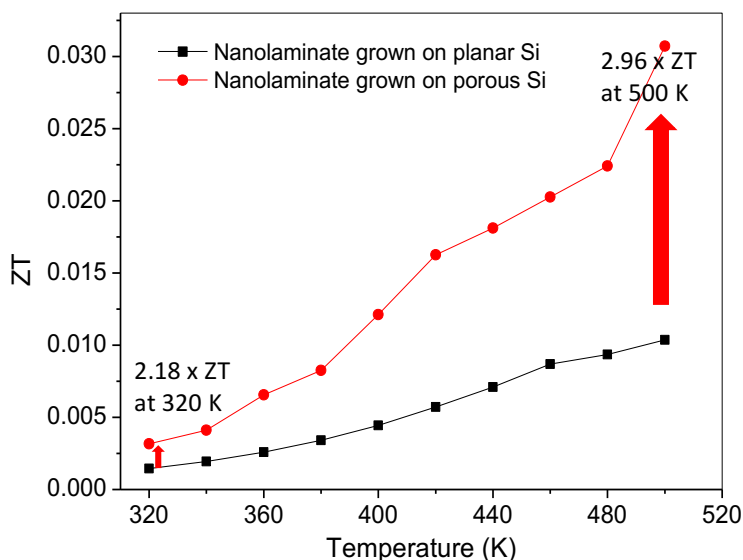


Figure 35. Plot of calculated ZT as a function of temperature for ALD PbTe/PbSe nanolaminates (10/10 nm) grown on planar and porous Si substrates using our measured values of the Seebeck coefficient, the electrical conductivity and the thermal conductivity.

3.2 PbTe/PbSe Films on Stripe-Patterned Si Substrates

In this section, the thermoelectric properties of ALD PbTe/PbSe films grown on stripe-patterned Si substrates were investigated experimentally and theoretically.

Fabrication of Stripe Patterned Si Substrates

The stripe patterned Si substrates were fabricated by wet etching thermal oxidized silicon wafers after photolithographic pattern transfer from a mask. Figure 36 shows the schematic diagram for the process steps to fabricate stripes of varying widths by photolithography with a mask aligner. The 484 nm-thick thermal SiO₂ layer was used as a hard mask and pre-treated by ultra-sonic cleaning in acetone, rinsing with DI water, and dried using nitrogen gas flow at room temperature. The pre-treated oxidized Si substrates were then placed into a furnace at 200 °C for 15 min to dehydrate under nitrogen atmosphere. Hexamethyldisilazane (HMDS) acted as a surface promotor on the substrate surface before spin-coating photoresist to enhance photoresist adhesion to SiO₂/Si substrate by forming a strong bond with the oxide surface. MIR-701 photoresist was spin-coated on the HMDS covered substrate at a spin speed of 4000 rpm, which yields a ~ 0.9 μm-thick resist film. After soft baking on a hot plate at 90 °C for 1 min, the sample was exposed under UV light with intensity of 2.55 mW/cm² for 1 min in hard contact mode, and followed by post exposure baking at 110 °C for 1 min. MIF 300 was used as developer and diluted by DI water with a dilution ratio of 2:1. The developing time was about 65 sec. After post baking on a hot plate at 100 °C for 10 min, the oxide hard mask was etched in buffered oxide etching (BOE) solution for 10 min. The etching rate of thermal SiO₂ in BOE solution is 17.7 nm/min. Finally, the pattern was trench etched into the Si substrate using a 30% KOH solution for

1 min achieving a trench depth of 700 nm. The remaining photoresist will be removed by diluted KOH solution; therefore, there is still patterned SiO_2 remaining acting as an isolating hard mask.

To investigate the effect of the dimension of the stripe patterns on the thermoelectric properties of the thin PbTe/PbSe films, patterns with width of 1 μm , 2 μm , and 4 μm were fabricated.

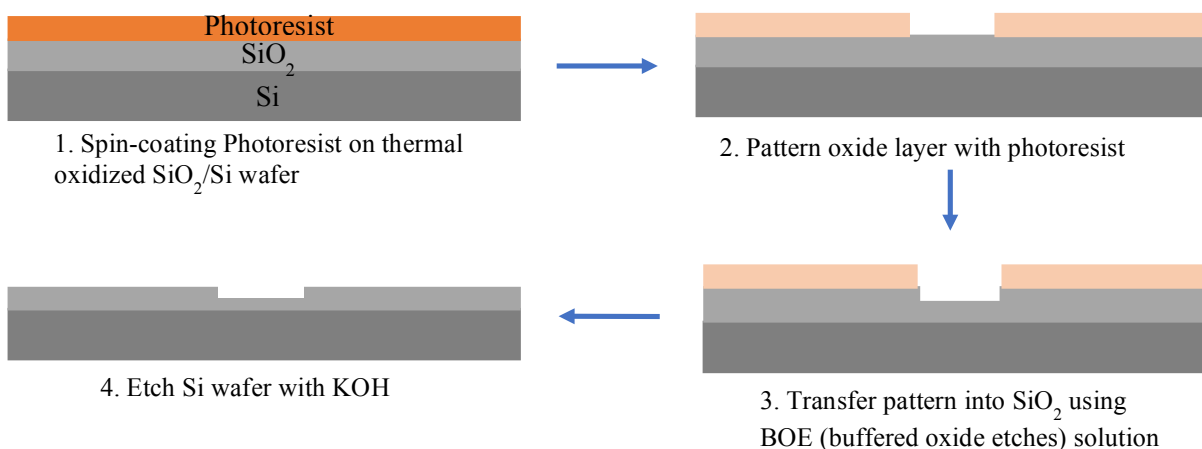


Figure 36. Schematic diagram of the process flow for the fabrication of stripe patterned substrates.

Surface Characterization

ALD technology was applied for the conformal deposition of PbTe and PbSe thin films on the stripe patterned substrates. The thickness of the ALD deposited films was controlled in the range of 25 nm ~ 50 nm, which is comparable to the average mean free path of phonons [88], aiming to enhance phonon scattering to reduce thermal conductivity. Figure 37 displays the FE-SEM micrographs of the surface morphology of ALD synthesized PbSe of ~ 50 nm on stripe and trench patterned Si substrates. The height of the stripe is around 100 nm. The width of the stripe is 1 μm , 2 μm , and 4 μm , respectively and the trench depth is 100 nm. The granular surface

morphology reveals Volmer Webber island growth resulting in polycrystalline ALD PbSe films. During ALD deposition the initial nucleated islands coalesce together forming a very good complete film coverage even in the corner of the stripe pattern.

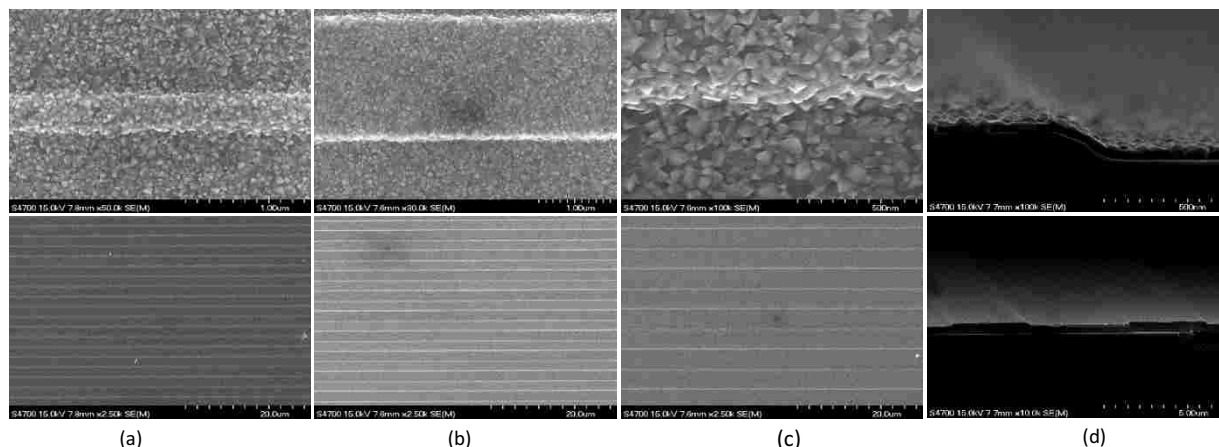


Figure 37. FE-SEM images of an ALD PbSe film on (a) $1\mu\text{m}$, (b) $2\mu\text{m}$, (c) $4\mu\text{m}$ patterned Si substrate, (d) cross-sectional images of PbSe film grown on $2\mu\text{m}$ wide stripe patterned Si substrate with trench depth of 100nm .

The Seebeck coefficient of these ALD PbSe films grown on stripe patterned Si substrate were measured in the temperature range of 300 K to 500 K using an MMR Seebeck measurement system. Figure 38 (a) plots the Seebeck coefficient as a function of temperature of ALD PbSe films grown on $1\mu\text{m}$, $2\mu\text{m}$ wide stripe patterned Si substrates benchmarked against planar SiO_2 covered Si wafers. In all three cases, the Seebeck coefficient of the PbSe film decreases as temperature increases from 300 K to 500 K. The maximum negative Seebeck coefficient occurs at room temperature around $-175\mu\text{V/K}$. The width of the stripe pattern has a measurable influence on the Seebeck coefficient of ALD PbSe films in the horizontal in-plane direction at high temperature. Our photolithography equipment available at the university limited us to $1\mu\text{m}$ wide stripe pattern

as the smallest width that could be resolved by our photolithography. However, in order to experimentally realize significantly improved thermoelectric properties based on phonon engineering principles, further reduction of the stripe width to submicron regime (~ 100 nm) would be required. This could be achieved with better state-of-the-art photolithography equipment or by E-beam lithography, but this was unavailable during the course of this study. Figure 38 (b) reveals an improvement of the Seebeck coefficient of PbSe films as a function of reduced thickness. The reduction of PbSe film thickness from 50 nm to 25 nm exhibits a clear improvement of the Seebeck coefficient, which can be attributed to thermal transport confinement along the film coating direction (vertical direction to the film surface).

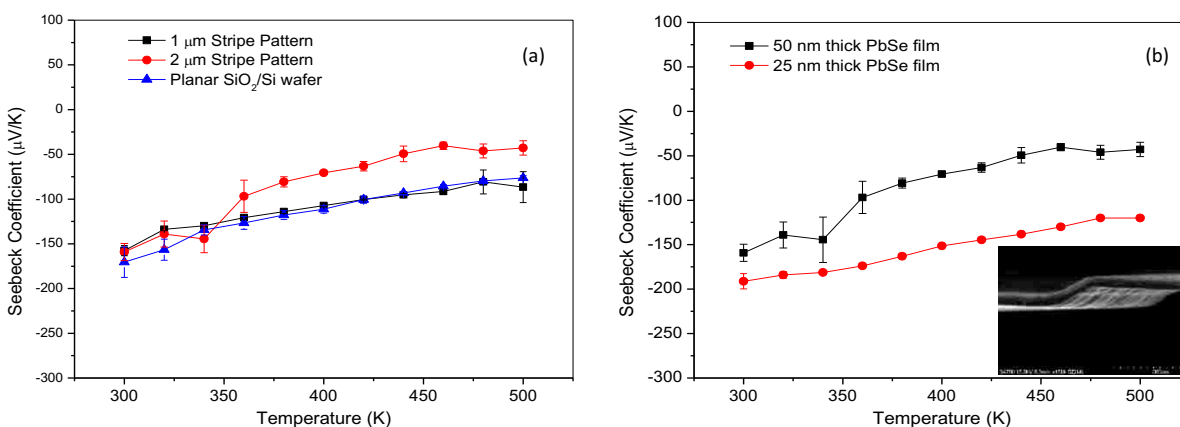


Figure 38. (a) Plot of Seebeck coefficient versus temperature of ALD PbSe films with thickness of 50 nm grown on stripe patterned Si substrate with width of 1 μm and 2 μm and compared to planar SiO_2/Si wafer over temperature range of 300 K \sim 500 K in horizontal in-plane direction by MMR Seebeck Measurement System. (b) Seebeck coefficient as a function of PbSe film thickness ranging between 50 nm and 25 nm grown on 2 μm wide stripe patterned Si substrate over a temperature range between 300 K \sim 500 K.

COMSOL Simulations of effective thermal conductivity of PbSe (100 nm) films

Because equipment limitations confined the experimentally achievable stripe width to 1 μm as the smallest dimension and shallow trench depths, the effect of consecutively smaller submicron stripe widths and varying trench depths had to be investigated by numerical simulation. A numerical simulation of the thermoelectric properties of a single stripe patterned TE element composed of a thin conformal PbTe film on a stripe patterned silicon substrate was developed using the finite element analysis software COMSOL 5.1 Multiphysics. The heat transfer in the single TE leg module was calculated using the equation of classic heat transfer in solids, which is defined by:

$$\rho C_p \frac{\partial T}{\partial t} + \rho C_p \mu \cdot \nabla T = \nabla \cdot q + Q \quad (23)$$

$$q = -k\nabla T \quad (24)$$

Where ρ is the density, C_p is the heat capacity at a temperature T , μ is the velocity field, κ is thermal conductivity, q is heat flux that is defined using Fourier's law, and Q is heat source [89]. To simplify the calculation, there are several assumptions in the simulation. For the heat transfer module, only heat diffusion was considered in our case. Furthermore, all the outer surfaces are assumed thermally isolated except for the front and back ends where the temperature difference is applied. Since the simulation assumes only vacuum environment, the heat convection between the solid and surrounding air, air flow and pressure are neglected. In spite of the simplifying assumption this simulation model still provides practical valuable insight for the thermoelectric devices because minimizing the heat loss caused by heat convection is a desirable objective. Additionally, the simplified model uses the classic heat transfer model, which eliminates the size effect in the nano scaled structures, whereby the heat transfer would follow a ballistic transport

model. However, the size effect will further decrease the thermal conductivity of nano-patterned films, which will be explained later.

The thermoelectric analysis used a coefficient form partial differential equation. Coupled with the heat transport equation Eq. 23 and the continuity of electric current density equation Eq. 25, as well as the constitutive equations of thermoelectrics Eq. 26-27, the thermoelectric field equations for temperature T and electrical potential V in a steady state can be expressed by Eq. 27 and 28:

$$\nabla \cdot \left(\vec{j} + \frac{\partial \vec{D}}{\partial t} \right) = 0 \quad (25)$$

$$\vec{q} = \Pi \cdot \vec{j} - \kappa \cdot \nabla T \quad (26)$$

$$\vec{j} = \sigma \cdot (-\nabla V - S \cdot \nabla T) \quad (27)$$

$$-\nabla(\sigma S^2 T + \kappa) \nabla T - \nabla(\sigma S T \nabla V) = \sigma((\nabla V)^2 + S \nabla T \nabla V) \quad (28)$$

$$\nabla(\sigma S \nabla T) + \nabla(\sigma \nabla V) = 0 \quad (29)$$

Where \vec{j} is electric current density vector, \vec{D} is the electric flux density vector ($\vec{D} = \epsilon \vec{E}$), V is the electrical potential, σ is the electrical conductivity, κ is the thermal conductivity, Π is the Peltier coefficient ($\Pi = ST$). Considering the case of non-time-varying magnetic fields, the electrical field is non-rotational and $\vec{E} = -\nabla V$.

COMSOL-Multiphysics allows the implementation of common arbitrary partial differential equations (PDEs) of the field variables u on one to three dimensional regions Ω . A coefficient form PDE application model was defined as Eq. (30)-(32) [90].

$$c_a \frac{\partial^2 u}{\partial t^2} + d_a \frac{\partial u}{\partial t} + \nabla \cdot (-c \nabla u - a u + \gamma) + \beta \cdot \nabla u + a u = f \quad (30)$$

$$n \cdot (-c \nabla u - a u + \gamma) + q u = g - h^T u \quad (31)$$

$$hu = r \quad (32)$$

Then the thermoelectric field equations Eq. (28) (29) can be transformed into the coefficient form. The vector field variable \vec{u} , the coefficient c , and the coefficient f are can be expressed in the following equations Eq. 33 to Eq. 35. The other parameters in the set of Eq. (29)-(31) are zero for static state calculation.

$$\vec{u} = \begin{pmatrix} T \\ V \end{pmatrix} \quad (33)$$

$$c = \begin{pmatrix} \lambda + \sigma S^2 T & \sigma S T \\ \sigma S & \sigma \end{pmatrix} \quad (34)$$

$$f = \begin{pmatrix} \sigma \left((\vec{\nabla} V)^2 + S \vec{\nabla} T \vec{\nabla} V \right) \\ 0 \end{pmatrix} \quad (35)$$

The dimension of the single stripe patterned TE element was set as $10 \mu\text{m} \times 10 \mu\text{m} \times 50 \mu\text{m}$, and the 100 nm-thick PbSe film coating was modeled on top of the stripe patterned SiO_2 substrate. The thermoelectric ALD film coating covered the surface and trenches of the patterned Si substrate uniformly and in a conformal fashion. The width of the stripe patterns was varied from 0.1 to $1 \mu\text{m}$, and the trench depth of the stripe patterns was varied from 1 to $10 \mu\text{m}$, to investigate the effective thermal conductivity and generated thermoelectric voltage of the PbTe film on the stripe patterned SiO_2 substrate as a function of the width and trench depth of the stripe patterns. Tetrahedral mesh was chosen for both thin film and the substrate, as shown in Figure 39, with the maximum element size of 1.77×10^{-6} m, a minimum element size of 5.05×10^{-7} m, a maximum element growth rate of 1.45, a curvature factor of 0.5, and a resolution of narrow regions of 0.5. Several important parameters for the PbTe film and SiO_2 substrate, including Seebeck coefficient, electrical conductivity, thermal conductivity, heat capacity and density, are temperature dependent and taken from the COMSOL Multiphysics database and reported literature articles. Table II below presents those parameters at a given temperature of 293 K. A p-type PbSe film was applied in the

simulation. The front and back ends of the test element are set as cold and hot side, respectively. The Dirichlet boundary condition was defined for the temperature of the hot and cold sides. The front cold surface was set as electric ground potential. All the other surfaces are thermally isolated. Therefore, the thermoelectric voltage was generated strictly based on the established temperature gradient.

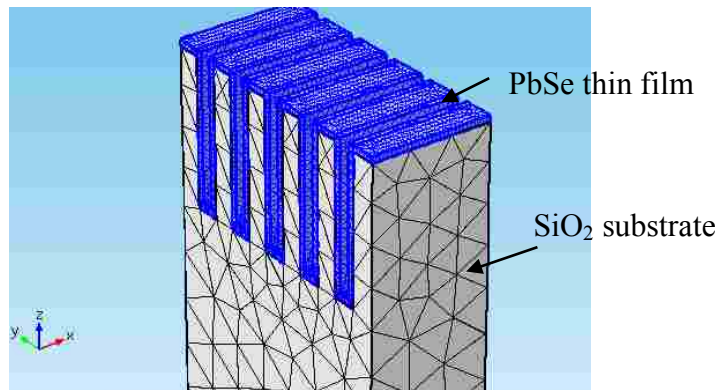


Figure 39. Details of the mesh density distribution over the test element that was used in the model.

TABLE II

Thermoelectric properties for TE materials and substrate at 293 K

| Sample | Seebeck Coefficient S [$\mu\text{V}/\text{K}$] | Electrical Conductivity σ [S/m] | Thermal conductivity κ [W/mK] | Heat Capacity C_p [J/kgK] | Density P [kg/m^3] |
|------------------|---|---|---|--|---|
| PbTe | 187 | 6.1×10^3 | 1.46 | 151 | 8160 |
| SiO ₂ | / | 1×10^{13} | 1.4 | 730 | 2200 |
| Si | 86 | 1.2 | 130 | 700 | 2329 |
| Cu | 6.5 | 5.9×10^8 | 350 | 385 | 8700 |

Figure 40 demonstrates the temperature profile along the surface of the thin film coating, comparing the temperature distribution of thin thermoelectric layer along the y axis at two different

trench widths of 5 μm and 0.5 μm . The temperature gradient is steeper in the narrower patterned test sample, indicating smaller thermal conductivity. The effective thermal conductivity of the stripe patterned samples can be calculated based on equation $q = -\kappa \frac{dT}{dx} \approx \kappa_{\text{eff}} (T_{\text{hot}} - T_{\text{cold}}) / \Delta x$, where q is heat flux, T_{cold} and T_{hot} is the temperature of cold side and hot side, respectively, which are extracted from the simulation. The temperature at the hot front side and cold back side of the test structure can be extracted from the software.

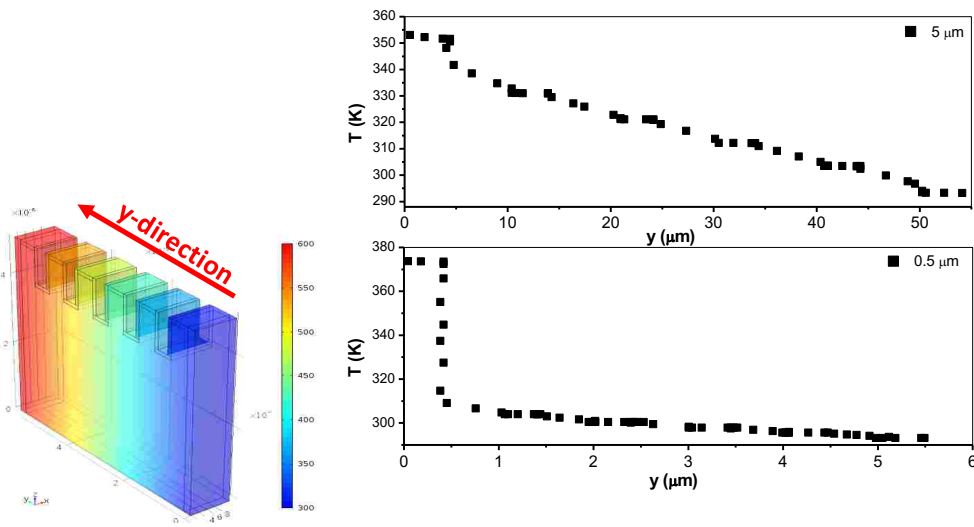


Figure 40. (a) The PbSe thin film coating of 100 nm was modeled on the patterned SiO_2 substrate. The width and depth of the stripe patterns along y-direction was varied from 10 μm to 0.5 μm . (b) Temperature profile of 100 nm PbSe film on stripe patterned SiO_2 substrate. The width of the stripes is 5 μm and the trench depth is 0.5 μm . The heat flux is maintained at a constant value of 10^6 W/m^2 at the front face of the module.

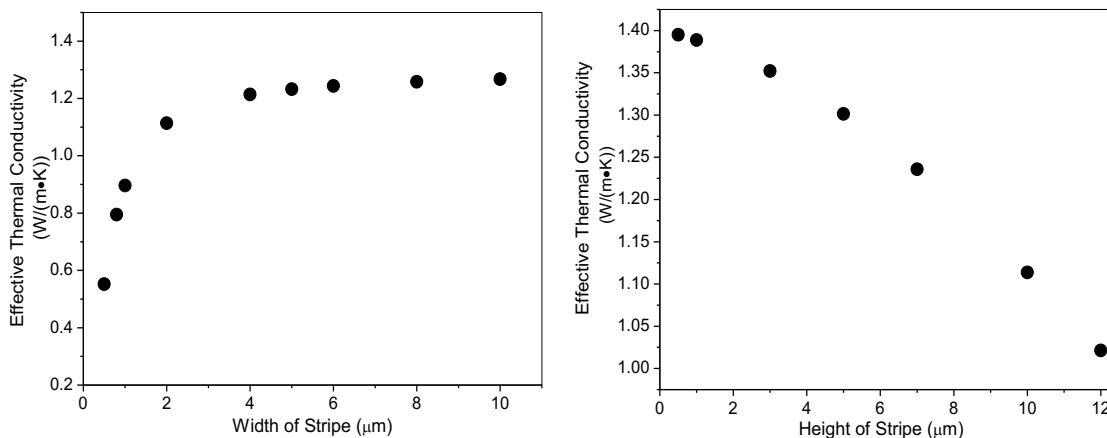


Figure 41. (a) Theoretical effective thermal conductivity of PbSe (100 nm) film coating deposited on stripe patterned SiO₂ templates as a function of stripe width (b) as a function of the height of the stripes.

Figure 41 (a) displays the dependence of the effective thermal conductivity on the width of the stripe pattern, which is varied from 0.5 μm to 10 μm. In Figure 40a the height of the stripe patterns was kept constant at 2 μm. As the width of the stripes decrease from 10 μm to 0.5 μm, the effective thermal conductivity also decreased. This could be explained by the reduction in materials in the stripe patterned structure, the increasing etched-out trenches introduce more film substrate boundaries which contribute more to scatter phonons, hindering the heat transport. The effect of the height of the stripes on the effective thermal conductivity is shown in Figure 41 (b). In this case the width of the stripe was kept constant at 2 μm. Initially when the height of the stripe pattern varies only from 0 to 0.5 μm and to 1 μm, such a stripe height has little to negligible effect on the effective thermal conductivity. However, when the height of the stripe increases further, the effective thermal conductivity dropped immediately in a steady fashion. Because of technical issues with isotropic KOH wet etching, the stripe height (or trench depth) of our experimentally fabricated stripe patterns is limited to only 50~100 nm. This shallow stripe height is located in the

upper left of Figure 40 (b), where the effective thermal conductivity does not start to drop yet. The limitation to shallow stripe heights of only 50~100 nm explains why our experimentally fabricated stripe patterns did not influence the Seebeck coefficient of the samples as much as expected. Nevertheless, the simulations provide accurate insights and predictions how the dimension of the stripe width and height affects the heat transfer inside the test structure. The COMSOL simulation indicate that narrower and deeper stripe patterns are the best strategy to apply in thermoelectric films in order to reduce the effective thermal conductivity and consequently to improve ZT. In order to optimize the geometric dimensions of the stripe patterns for thermoelectrics application its influence on electron transport has to be investigated as well. The maximum thermoelectric voltage difference observed between the hot and cold side was found to be 0.0599 V for a stripe pattern width of 1 μm , as shown in Figure 42.

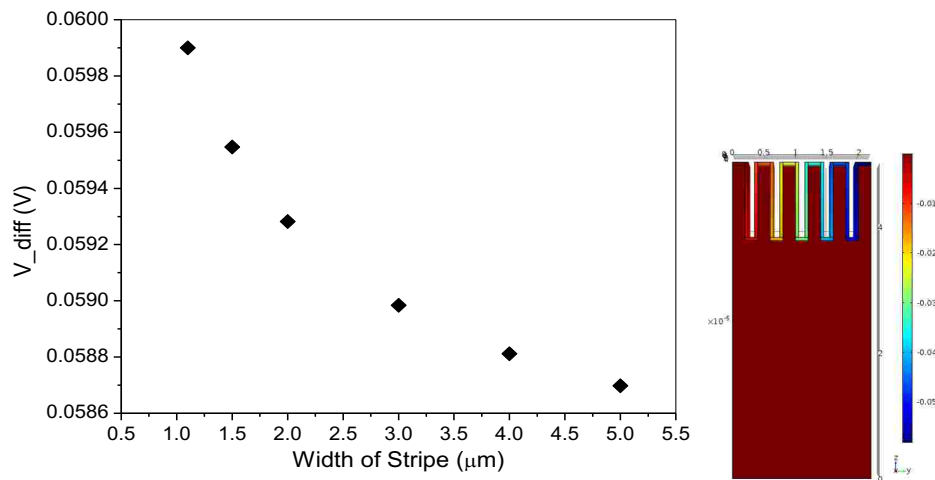


Figure 42. *Plot of the relationship between thermoelectric voltage difference and the width of stripe patterns.*

3.3 Summary

In this chapter, the phonon engineering concept was experimentally implemented by ALD depositing PbTe/PbSe thin films on nano-patterned substrates, aiming to enhance phonon scattering to reduce thermal conductivity. The PbTe/PbSe nanolaminate structures were deposited by ALD technology on regular planar silicon wafers and benchmarked against identical PbTe/PbSe nanolaminate coatings synthesized inside nano-scaled periodic porous Si templates. The first time use of nano-scaled porous Si templates and thermoelectric ALD coatings increased the Seebeck coefficient by a factor of three. As an added benefit, the use of porous nanolaminates simultaneously lowered the thermal conductivity by a factor of two compared to the case of planar thermoelectric nanolaminate films. The enhanced Seebeck value is attributed to the presence of the regular array of etched out pores, which provides an additional periodic structuring of the nanolaminate composite sample, while the high porosity of the porous Si templates simultaneously reduces the thermal conductivity. On the other hand, the presence of the pore walls can also scatter electrons to some degree, resulting in a small reduction in the electrical conductivity. Consequently, the Figure of Merit ZT value for the porous thermoelectric nanolaminates was enhanced by a factor of up to three at 500 K. These results demonstrate that the novel concept and fresh engineering approach of phonon engineering in nano-scaled thermoelectric films was successfully rendered to practice. For the stripe patterned structure, the COMSOL simulations further demonstrate that a significant ZT enhancement can be realized in the structure with stripe width less than $2\ \mu\text{m}$ and stripe height (or trench depth) larger than 500 nm.

CHAPTER 4

4. IN-PLANE ZT MEASUREMENTS USING LAB-ON-A-CHIP TEST DEVICES

The properties of nano-scaled thermoelectric materials are usually very different from bulk materials of the same substance because of the size effect. The confinement of electrons and phonon transport has been successfully applied for enhancing the electrical properties of low dimensional materials, including quantum wells, superlattices, nanowires, and quantum dots. For anisotropic materials, there is a discrepancy in their properties along the horizontal in-plane direction (parallel to the surface) or vertical direction (perpendicular to the surface), since the charge carriers and phonons experience different scattering effects along these two directions. Taking the example of 2-D superlattices or quantum well structures, phonon scattering is more pronounced along the vertical direction compared to the phonon scattering along the horizontal direction because of numerous interfaces in the vertical direction. ZT calculations will only be correct if all parameters are measured in the same direction. Ideally, all thermoelectric measurements should be performed at only one sample within one run in order to avoid errors due to different sample compositions, different sample geometries, such as size or thickness, and different heat profiles. The ZT test chip in a lab-on-a-chip setting was reported by V. License et al. [79] for in-plane ZT measurements, with which the Seebeck coefficient S , the electric conductivity σ and the thermal conductivity κ of thermoelectric thin films can be measured quasi-simultaneously for one single deposited film.

This chapter provides the results obtained by applying the Linseis lab-on-a-chip based thermoelectric test platform to perform horizontal in-plane ZT characterizations of ALD PbTe,

PbSe thin films and double-layer PbTe/PbSe films. The thermoelectric films were deposited by Atomic Layer Deposition (ALD) on the sample deposition area of the test chip. The Seebeck coefficient, the electrical conductivity, and the thermal conductivity of the films were measured quasi-simultaneously in the horizontal in-plane direction. Figure 44a shows a photographic image of the commercial Linseis thermoelectric test system and Figure 44b provides a close-up of the measurement chamber and the test chip stage. All the important thermoelectric parameters were measured in the temperature range of 300 K to 380 K with a 1 Tesla magnet field. A thin Al_2O_3 protection layer was applied to avoid oxidation and degradation of PbTe/PbSe films.

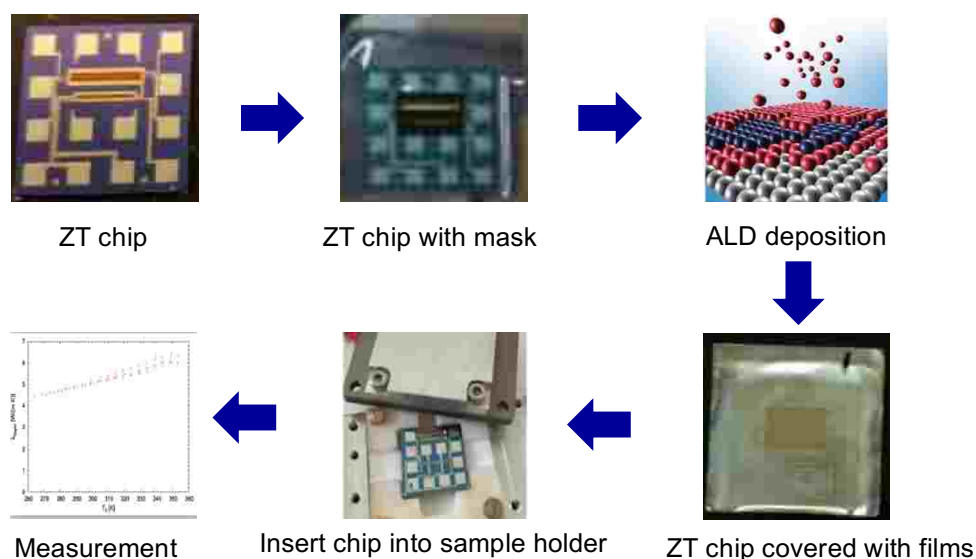


Figure 43. Schematic of the process flow of sample preparation for thermoelectric ZT test chip measurements [79].



Figure 44. (a) View of the Linseis thermoelectric measurement System and b) close-up of the sample stage in the measurement chamber.

4.1 Sample Preparation and Measurement Setup

Figure 43 shows the process flow of sample preparation. The test chip was fabricated by pre-structuring thermoelectric test circuits on a Si (100) wafer, acting as substrate for thermoelectric material deposition. The pre-structured thermoelectric test chip consists of two measurement parts, one is based on the Völklein geometry for thermal conductivity measurements utilizing a membrane structure [91], and the other part is based on a four-point Van der Pauw geometry for measuring various electrical properties and the Seebeck coefficient of thin films. The detailed configuration of the ZT test chip is displayed in Figure 45. The Seebeck coefficient is measured using a Pt resistance thermometer passivated by an ALD (Atomic Layer Deposited) 30 nm Al_2O_3 top layer and is located on the surface of the larger 100 nm thick Si_3N_4 test membranes. The ALD Al_2O_3 passivation layer covers the entire test chip. The contact pads are subsequently opened up by masking and wet chemical etching. An organic pre-structured shadow mask was

used for low temperature (below 150 °C) film deposition. In case higher film deposition temperatures (higher than 150 °C) are required a metal shadow mask can be used instead. In principle, several film deposition techniques can be applied, including thermal evaporation, sputtering, Molecule Beam Epitaxy (MBE), Chemical Vapor Deposition (CVD) or Atomic Layer Deposition (ALD). Then the key thermoelectric parameters of the deposited TE film can be measured on the ZT test chip in the temperature range from 120 to 450 K in a higher vacuum of 10^{-7} torr [79].

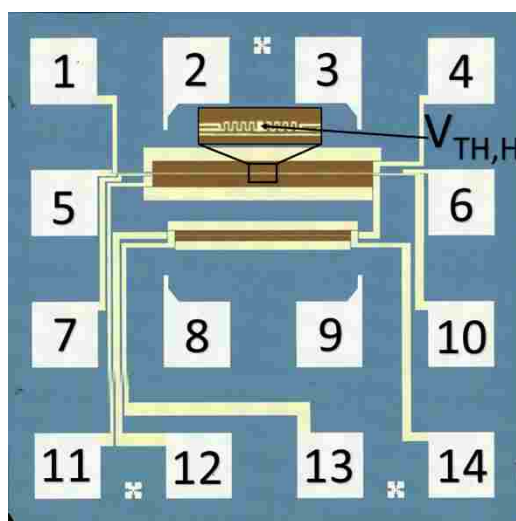


Figure 45. The configuration and layout of the electrical circuits and contact pads of the ZT test device structures [79].

The PbTe, PbSe, and double-layer PbTe/PbSe films were deposited on the ZT test chip by ALD, covering the entire testing structure marked with the red square in Figure 45. Lead bis(2,2,6,6-tetramethyl-3,5-heptanedionato) ($\text{Pb}(\text{C}_{11}\text{H}_{19}\text{O}_2)_2$), (trimethylsilyl) telluride ($(\text{Me}_3\text{Si})_2\text{Te}$) and (trimethylsilyl) selenide ($(\text{Me}_3\text{Si})_2\text{Se}$) were employed as the chemical ALD precursors for lead, tellurium and selenium, respectively. Thermal ALD with a cross-flow reactor

from Cambridge Nanotech was applied for the ALD deposition. 20 sccm inert N₂ gas was used as a carrier gas to transport the chemical precursors into the ALD reaction chamber. The growth temperature of PbTe and PbSe was 150 °C. The solid lead precursor was volatilized at a temperature of 170 °C with 0.5 s pulse time, the liquid Te precursor required heating to 45 °C with 0.03 s pulse time, and the liquid Se precursor was kept at room temperature with 0.03 s pulse time. The Pb precursor and Se precursor were introduced into ALD chamber alternatively for ALD growth of PbSe (PbTe) films. The chamber base pressure was kept at 30 mTorr. The growth rate for ALD growth of PbTe and PbSe films at 150 °C were about 0.48 Å/cycle and 0.73 Å/cycle, respectively. The ALD growth of PbSe exhibits a higher growth rate than that of PbTe ALD film, which may be attributed to the higher reactivity of the Se precursor compared to the Te precursor.

In this study, a PbTe film of 2000 ALD deposition cycles, a PbSe of 2000 deposition cycles, a double layer of PbTe/PbSe (2000 / 1400 ALD deposition cycles), and a PbSe film of 2000 ALD deposition cycles covered with a 25nm-thick Al₂O₃ passivation layer were fabricated and characterized. The measured thickness of the four tested samples is 96.24 nm, 146.40 nm, 132.46 nm, and 111.23 nm, respectively.

Table III

The thickness of PbTe, PbSe, PbTe/PbSe, and PbSe/Al₂O₃ films.

| Samples | PbTe (2000 cycles) | PbSe (2000 cycles) | PbTe/PbSe (2000/1400 cycles) | PbSe/ Al ₂ O ₃ (2000/250 cycles) |
|----------------|-----------------------|-----------------------|---------------------------------|---|
| Thickness (nm) | 96.24 ± 3.15 | 146.40 ± 3.81 | 132.46 ± 11.33 | 111.23 ± 7.51 |

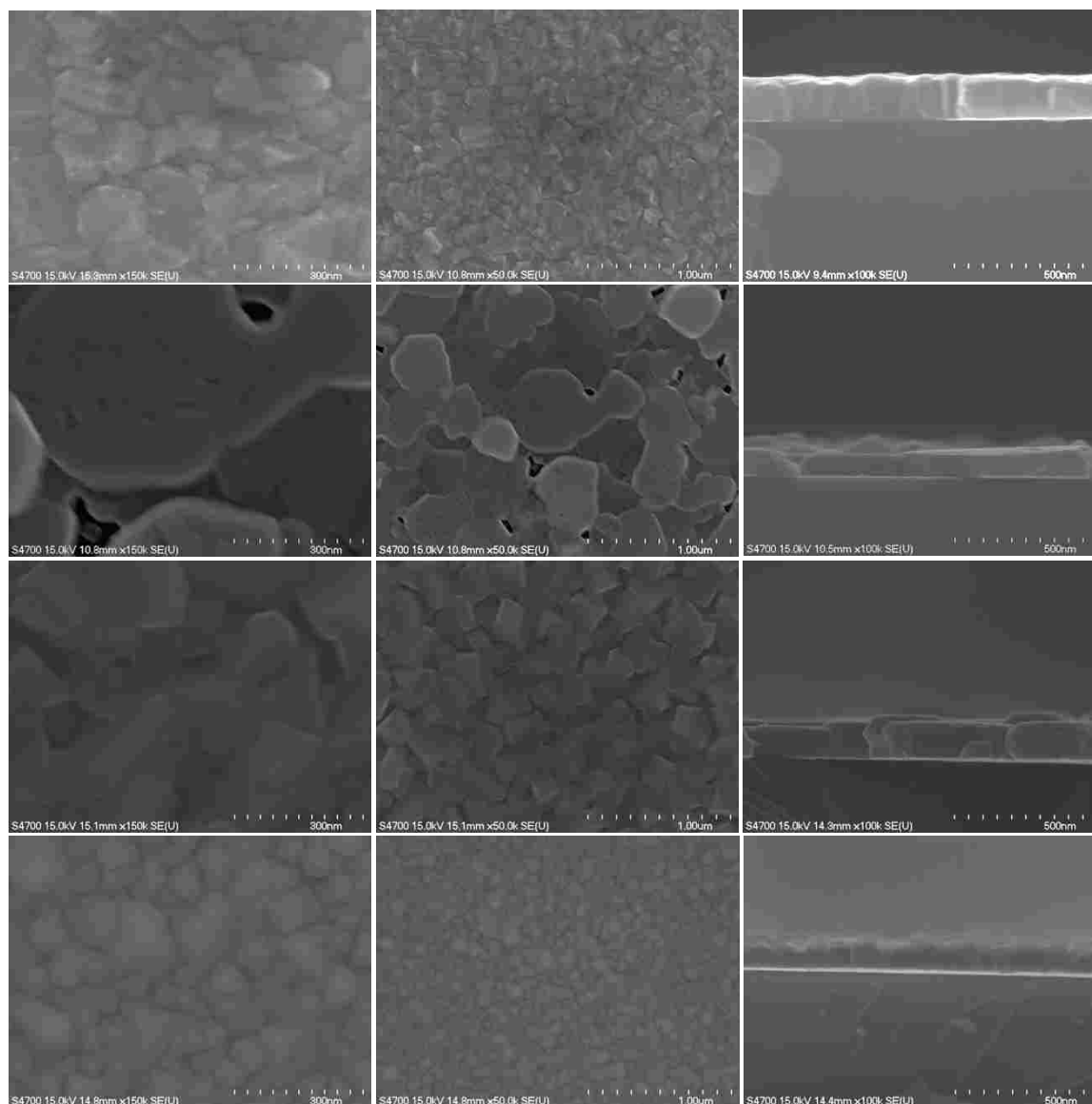


Figure 46. FE-SEM micrographs of surface morphology of (a) a PbSe film with 2000 ALD deposition cycles, (b) a PbTe film with 2000 ALD deposition cycles, (c) a double-layer PbTe/PbSe (with 2000/1400 ALD cycles), and (d) a PbSe film with 2000 ALD deposition cycles covered with 250 cycles of Al_2O_3 passivation layer.

The FE-SEM micrographs of the surface morphology of the samples are shown in Figure 46. It can be clearly seen that both the ALD growth of PbTe and PbSe follow Volmer-Webber

island growth mode, and the PbTe and PbSe grains combine together forming completely closed and compact tight films. The grain size of PbSe is ranged randomly from 30 nm to 150 nm. It was observed that the PbSe grain size is considerably smaller than the grain size of PbTe that is around hundreds of nanometers.

4.2 Results and Discussions

Electrical Conductivity

The electrical properties are measured based on Van der Pauw four contacts technique, using needle contacts of 2, 3, 8 and 9, as marked in Figure 45. The current was introduced in between contacts 2 and 3, then measured induced voltage between contacts 8 and 9. The resistivity of the film was determined by

$$\rho = \frac{V_{23} * W * t}{I_{89} * L} \quad (36)$$

Where W is the width of the sample, L is the distance between contacts 8 and 9, t is the thickness of the sample. The measurements under reversed current and voltage were taken to reduce error by taking averaged current and voltage.

Figure 47 plots the temperature dependence of electrical conductivity of planar single-layer PbTe, PbSe films and double-layer PbTe/PbSe films, and in addition PbSe films protected with a 25 nm-thick Al₂O₃ passivation layer on top. For the planar single-layer PbTe and PbSe films, the electrical conductivity of the films increases with rising temperature over the temperature range from 280 ~ 370 K. The planar PbTe films possess the higher electrical conductivity over the whole measured temperature range. The maximum electrical conductivity for PbTe film was 195.98 S/m at 370 K. The measured value is lower than reported literature values, which can be attributed to the intrinsic growth of ALD PbTe and PbSe films which are not doped. The resulting low charge

carrier density leads to poor conductive films. Impurity doping is the way to improve the electrical conductivity.

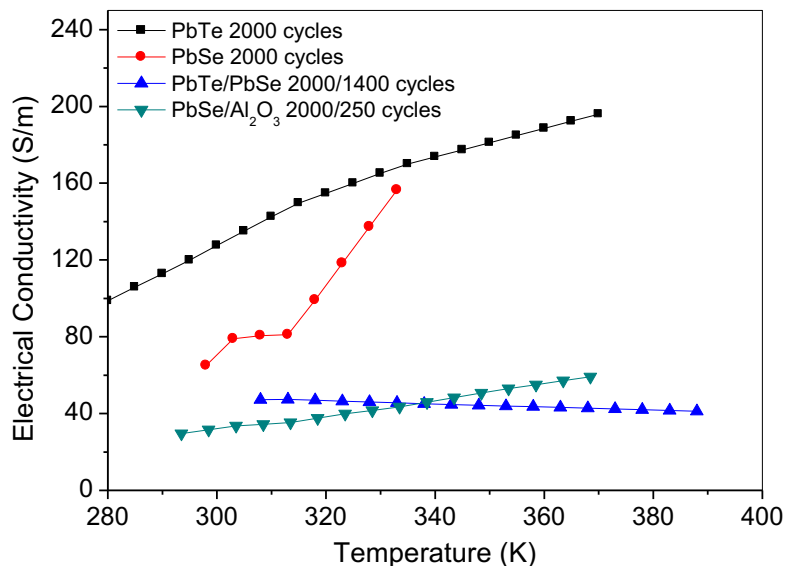


Figure 47. Plot of Electrical conductivity versus temperature of planar PbTe films (2000 ALD cycles), PbSe films (2000 ALD cycles), double-layer PbTe/PbSe (2000/1400 ALD cycles) films, and for comparison PbSe films covered with Al₂O₃ passivation top layer.

The temperature dependence of electrical conductivity for both planar single-layer PbSe and PbTe films exhibit pure semiconductor behavior (the electrical conductivity of the film increases as temperature arises) because the increased temperature provides more energy to excite more electrons across the band gap to the conduction band. Therefore, the electrical conductivity is rising with increasing temperature. In contrast to the single layer ALD films, the electrical conductivity of the double-layer PbTe/PbSe film reveals the opposite temperature dependence, decreasing electrical conductivity, which exhibits metallic properties. This interesting result indicates that there is a conductive layer on the surface of the double-layer films, which is similar

to the behavior of topological insulators. But further investigations are needed to ascertain that the temperature dependence of the electrical conductivity in nanolaminate PbTe/PbSe layers exhibits topological-insulator-like property. Since the existence of a conductive surface is not a unique property solely for topological insulators, the symmetry of the band structure of the layered ALD thin film needs to be studied to ascertain if double or multi-layer PbTe/PbSe films are potential candidates for topological insulators. Comparing the electrical conductivity of PbSe films against PbSe covered with an Al₂O₃ passivation layer, there is no benefit to be seen in the data of Figure 47. Instead, the deposition of an ALD Al₂O₃ top passivation layer does little to prevent the TE layer from degradation; rather, it decreases the electrical conductivity of the films. The reduced electrical conductivity after applying an Al₂O₃ passivation layer is attributed to the oxidation of PbSe when a water pulse is introduced, which is required for the growth of ALD Al₂O₃.

Seebeck Coefficient

For the in-plane Seebeck coefficient measurements, a Hall-bar test device configuration was applied. A Pt resistance thermometer was used to measure the temperature of the hot side. The resistance was measured using contact pads 1, 4, 5, and 6 shown in Figure 45. The temperature gradient was applied along the y-direction. A sample contact $V_{TH,H}$ was pre-coated on the surface of the Si₃N₄ membrane and passivated by a 30 nm-thick ALD Al₂O₃ layer, which was close to the heating stripe, as shown in Figure 43. The contact $V_{TH,H}$ was electrically connected with contact pad 1 to measure the thermoelectric induced voltage $V_{TH,H}$. Contact pad 8 is the cold contact used to observe the voltage potential at the cold side $V_{TH,C}$, which was placed on the silicon substrate heat sink that is always maintained at room temperature. During the measurement, the electrical

current was introduced to the heating strip in between the contact pads 7 and 10 to generate a temperature gradient along the y-direction. The Seebeck coefficient was defined by the equation

$$S - S_{Pt} = -\frac{V_{th}}{\Delta T} = -\frac{V_{TH,H} - V_{TH,C}}{T_H - T_C} \quad (37)$$

Where S_{Pt} is the Seebeck coefficient of the Pt contacts, T_H and T_C is temperature of the hot side and cold Si heat sink. The temperature is measured by an inserted thermocouple underneath the ZT test chip [79]. The temperature dependence of the horizontal in-plane Seebeck coefficient of the planar thermoelectric ALD films was measured over the temperature range of 300 ~370 K.

Figure 48 plots the Seebeck coefficient of planar single-layer PbTe films and double-layer PbTe/PbSe films as function of temperature. The positive Seebeck coefficient value indicates the both PbTe film and double-layer PbTe/PbSe film with PbTe termination were p-type TE materials. The Seebeck coefficient of PbTe films increased slightly as temperature increased and reached a maximum value of 458.76 $\mu\text{V/K}$ at 320 K, exhibiting extrinsic conduction behaviour. Beyond the maximum the positive Seebeck coefficient of PbTe decreased as the temperature was further increased, indicating onset of intrinsic conduction. For the double-layer PbTe/PbSe film, the Seebeck coefficient decreased as the temperature increased from 300 K to 370 K, with a maximum Seebeck coefficient of 441.71 $\mu\text{V/K}$ at 303 K. It is believed that the maximum Seebeck coefficient occurs at the temperature when intrinsic conduction begins, and the onset of intrinsic conduction is lower in thermoelectric materials with lower charge carrier density. The maximum Seebeck coefficient for PbTe/PbSe film occurred at a lower temperature of 303 K or lower. That finding can be explained by the lower carrier density in the double-layer TE film, which is also confirmed in the electrical conductivity measurements.

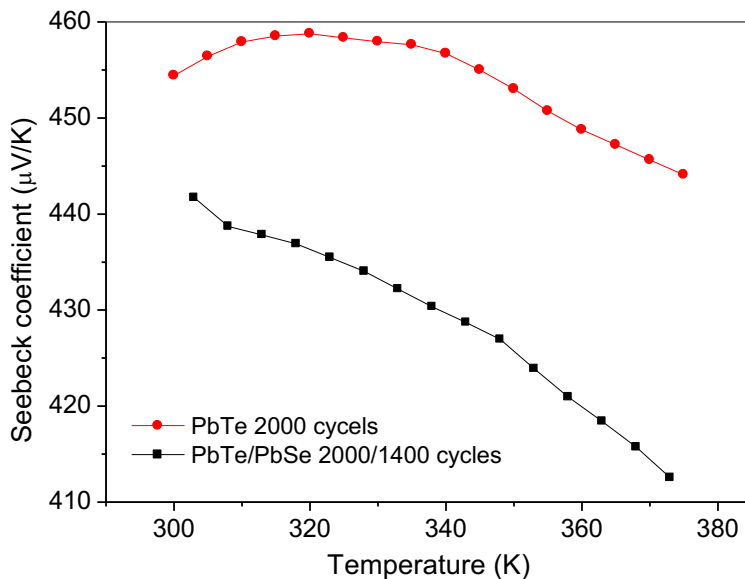


Figure 48. Plot of the Seebeck coefficient of planar PbTe film with 2000 ALD deposition cycles and of a planar double-layer PbTe/PbSe film (with 2000/1400 ALD cycles) as a function of temperature.

The Power Factor ($PF = \sigma S^2$) calculated from the measured single parameters (S and σ) was plotted as a function of temperature, and is displayed in Figure 49. The power factor value of planar PbTe films increases as a function of increasing temperature. The maximum power factor value at 370 K was $38.45 \mu\text{W}/(\text{mK}^2)$. For comparison, the power factor of double PbTe/PbSe nanolaminate films is much lower than the PbTe films, with a maximum value of $9.09 \mu\text{W}/(\text{mK}^2)$. The power factor of the nanolaminate films decreased as a function of rising temperature. The temperature dependence of the power factor is firmly related to that of the electrical conductivity of the films.

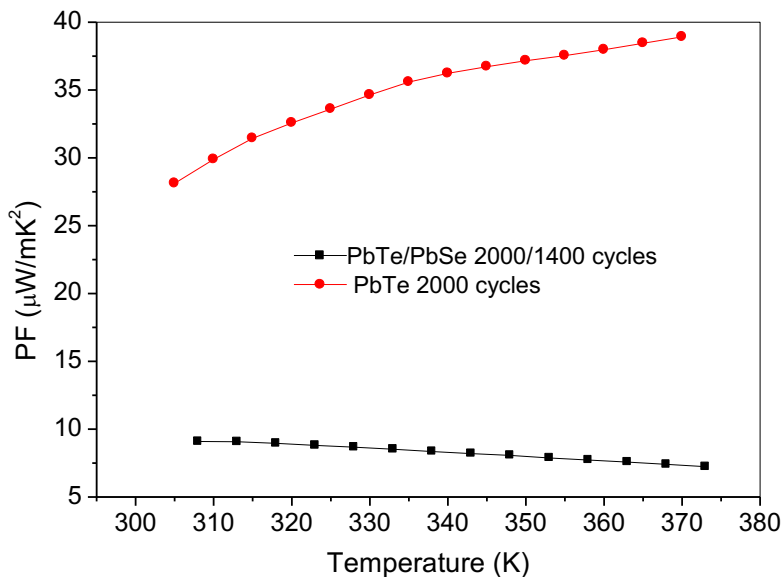


Figure 49. Plot of the calculated power factor $S^2\sigma$ for the planar PbTe film and PbTe/PbSe film in the temperature range between 300 K and 370 K using the data extracted from the Seebeck coefficient and electrical conductivity results.

Horizontal in-plane Thermal Conductivity

During this dissertation work, the horizontal in-plane thermal conductivity could only be measured with the ZT test chip. The thermal conductivity measurement was based on the Völklein configuration, which consists of two heating strips with different dimensions. The heating strips are connected in a 4-point probe configuration with contact pads 7, 10, 11, 12, 13, and 14, which are used as heater and sensor in the meantime. Figure 48 displays the configuration of electrical circuit contact pads of the ZT test chip and the cross-sectional schematic diagram of the suspended silicon nitride part utilized for the thermal conductivity measurements. The metal strip heater was pre-structured and fabricated on the surface of the suspended Si_3N_4 membrane, and was passivated by a thin ALD Al_2O_3 layer needed for separating the films from the heater. The thermoelectric films under test were ALD deposited on the top of the suspended Si_3N_4 membrane setup.

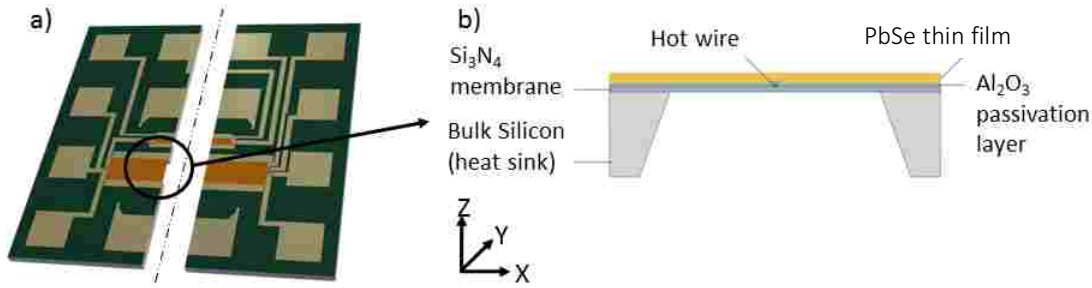


Figure 50. (a) Top view of the Electrical circuits and contact pad configuration of the ZT test chip, (b) Cross-sectional schematic of the ZT chip explaining the Si_3N_4 membrane test device for the thermal conductivity measurements [79].

For the thermal conductivity measurements, we start the procedure with the measurement of the resistance of the hot wire with a very small current to avoid Joule heating. The measured resistance is used to calculate temperature T_1 . Subsequently, a larger current was applied to the heating strip, producing heat because of Joule heating. Since the resistance of the hot wire and the applied current has been measured and thus is known, the heating power can be directly calculated. Heat flows through the membrane and the thermoelectric sample and penetrates the Si bulk substrate at the ends of the Si_3N_4 membrane, which acts as heat sink. For the next round the resistance of the much hotter heated wire with the larger applied current was measured again. The measured resistance can be used for the calculation of temperature T_2 . Therefore, the total thermal conductance G of the test device including the thermoelectric films is given by the ratio of the heating power W_h and the change of temperature of the metal strip before and after heating according to Eq. 38. The thermal conductivity κ_s of the thermoelectric film can be calculated by Eq. 39, where κ is the thermal conductivity of the entire membrane system (Si_3N_4 membrane and the thermoelectric sample), and κ_m is the thermal conductivity of Si_3N_4 membrane, t and t_m are

the thickness of the entire membrane system and the Si_3N_4 membrane, respectively.

$$G = \frac{W_h}{T_2 - T_1} \quad (38)$$

$$\kappa_s = \frac{\kappa t - \kappa_m t_m}{t_s} \quad (39)$$

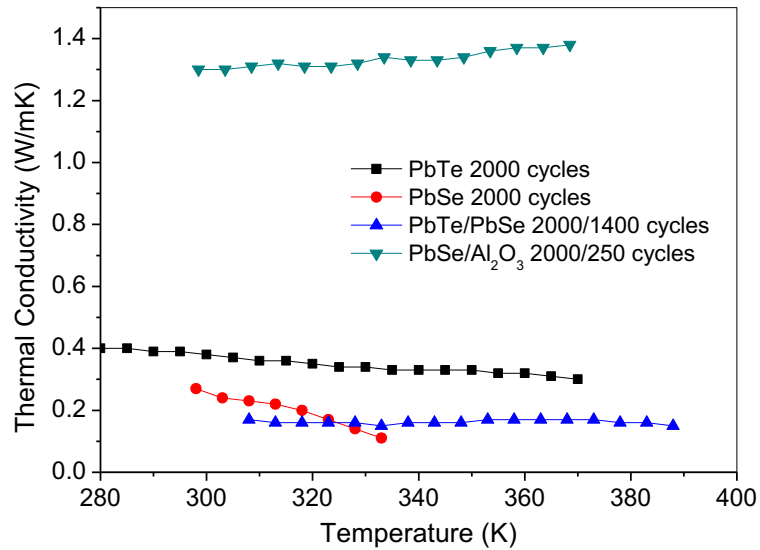


Figure 51. Plot of measured horizontal in-plane thermal conductivity for the planar PbTe films (2000 ALD deposition cycles), PbSe films (2000 ALD cycles), nanolaminate PbTe/PbSe films (2000/1400 ALD cycles) film and the PbSe film with Al_2O_3 passivation cap (2000/250 ALD cycles) as a function of temperature between 290 K and 370 K.

Figure 51 shows the horizontal in-plane thermal conductivity of the planar PbTe films with 2000 ALD deposition cycles, the PbSe films (2000 ALD cycles), and the PbTe/PbSe (2000/1400 ALD cycles) films plus the PbSe with an ALD Al_2O_3 passivation cap (2000/250 ALD cycles) measured in the temperature range of 290 ~ 370 K. It is significant to note that all the thermoelectric samples except for PbSe film with Al_2O_3 passivation cap exhibit extremely low

horizontal in-plane thermal conductivity (less than 0.4 W/(mK)) over the entire measured temperature range. As the temperature increases from 290 K to 370 K, the thermal conductivity of ALD PbTe films and the nanolaminate PbTe/PbSe films slightly decreases, while the thermal conductivity of the ALD PbSe films shows a more significant reduction. For the ALD PbTe film, the horizontal thermal conductivity decreases from 0.48 to 0.3 W/(mK) as the temperature increases from 180 to 370 K, as shown in Figure 51. The thermal conductivity of the ALD PbSe films is lower within the range of 0.27 W/(mK) (at 298 K) and 0.11 W/(mK) (at 333 K). The XRD and FESEM results clearly prove that the ALD deposited PbTe and PbSe films have a polycrystalline structure. The initially random nucleated PbTe and PbSe grains eventually coalesce together forming completely compact films. The grain boundaries along the in-plane direction can be clearly seen in high magnitude FE-SEM images. In comparison to the vertical measurement direction through the polycrystalline thermoelectric film, the horizontal in-plane thermal conductivity measurement configuration encounters orders of magnitude more grain boundaries. The increased grain boundary-phonon scattering encountered in the horizontal in-plane direction results in the demonstrated lower thermal conductivity. Since the grain size of ALD PbSe films is smaller compared to ALD PbTe films, the concomitant higher grain boundary density leads to stronger grain boundary-phonon scattering in the ALD PbSe films. This grain boundary density difference contributes to the lower thermal conductivity of ALD PbSe samples compared to the ALD PbTe samples. The double-layer ALD PbTe/PbSe samples exhibit even lower horizontal thermal conductivity than the PbTe and PbSe films. The PbTe/PbSe sample consists of 1400 ALD deposition cycles of PbSe on the bottom layer and 2000 ALD deposition cycles of PbTe on the top of PbSe, and corresponding thicknesses of two layers are ~38 nm and 100 nm, respectively. The thickness of the first layer of PbSe is low enough to cause the size effect [88] that constraints the

phonon transport along the vertical z-direction. On the other hand, the smaller grain size of the ALD PbSe layer is distributed over the range of ~ 30 nm and ~ 150 nm. Therefore, the increased grain boundary scattering along horizontal in-plane direction encountering higher grain boundary density plus the additional phonon scattering from the interface between the two ALD layers ultimately results in the lower measured thermal conductivity in double-layer PbTe/PbSe films.

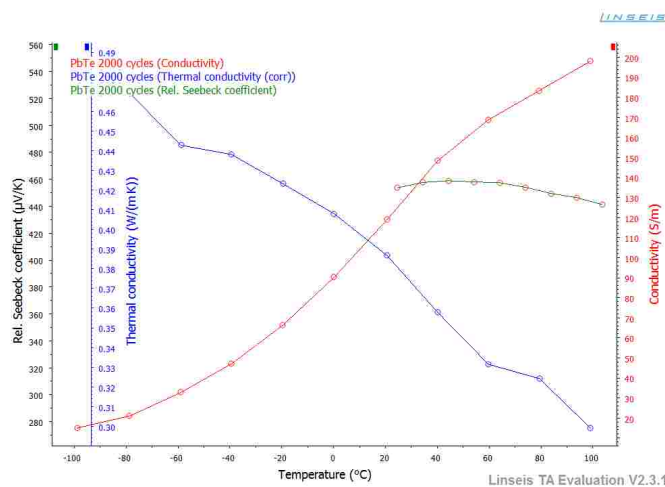


Figure 52. Plot of Electrical conductivity, Seebeck coefficient and thermal conductivity as a function of temperature of a planar ALD PbTe film with 2000 ALD deposition cycles measured in the temperature range from 180 K to 370 K.

Finally, the plot of Figure of Merit ZT as a function of temperature is shown in Figure 53. The ZT value was calculated from the measured horizontal in-plane Seebeck coefficient, the electrical conductivity and the thermal conductivity for non-structured planar thermoelectric films. The ZT of the ALD PbTe sample is higher than ZT of the ALD PbTe/PbSe films, and increases as temperature increases, with to a maximum value of 0.048 at 373 K. The relatively low ZT value results directly from the low electrical conductivity of the films, because our ALD thermoelectric

films were not doped for this study.

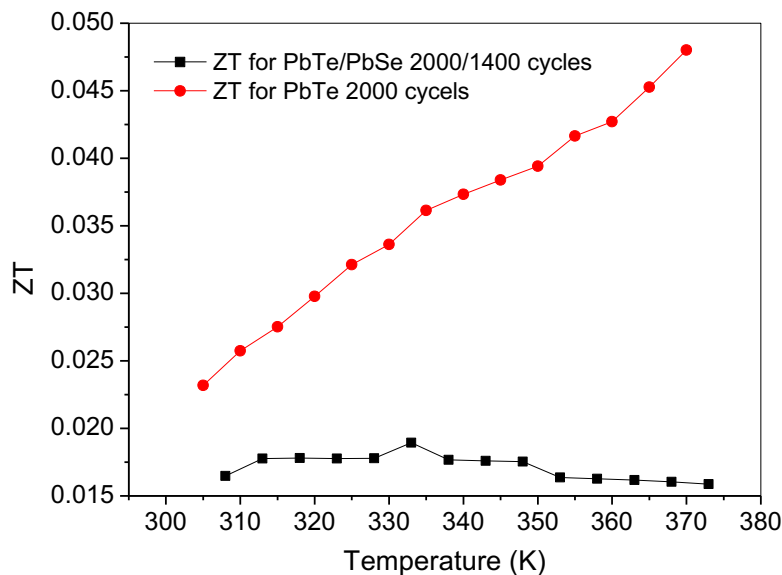


Figure 53. Plot of Calculated ZT values versus temperature for planar $PbTe$ films with 2000 ALD deposition cycles and $PbTe/PbSe$ film with 2000/1400 ALD cycles) using measured horizontal Seebeck coefficient, electrical conductivity and thermal conductivity.

The plot in Figure 54 compares the calculated ZT values for our non-structured planar $PbTe/PbSe$ samples, where all measurements were performed in the horizontal in-plane direction with the Linseis lab-on-a-chip test system to the ZT values for the ALD nanolaminates grown on planar and porous Si, where the thermal conductivity measurements were constrained to the vertical direction only by the TDTR method. It is evident that the ZT values calculated from all thermoelectric parameters measured in the horizontal in-plane direction are considerably higher than the ZT values calculated from separately measured all three parameters. As outlined previously, for the polycrystalline ALD $PbTe/PbSe$ films, the horizontal in-plane measurements with the Linseis test chip device of about 10 mm length encounters many orders of magnitude

more grain boundaries and interfaces along in-plane direction compared to the vertical direction, which corresponds only to the tenths of nanometer film thickness. This huge number of grain boundaries encountered in the horizontal 10 mm test device stretch are dramatically more effective in scattering phonons and blocking phonon transport, which yields a much lower thermal conductivity in the horizontal in-plane direction. Furthermore, it is important to point out that the ZT values in nano-structured porous samples are seriously underestimated because experimental constraints of TDTR method allowed only vertical thermal conductivity measurements. Also, the in-plane thermal conductivity is much lower than vertical thermal conductivity.

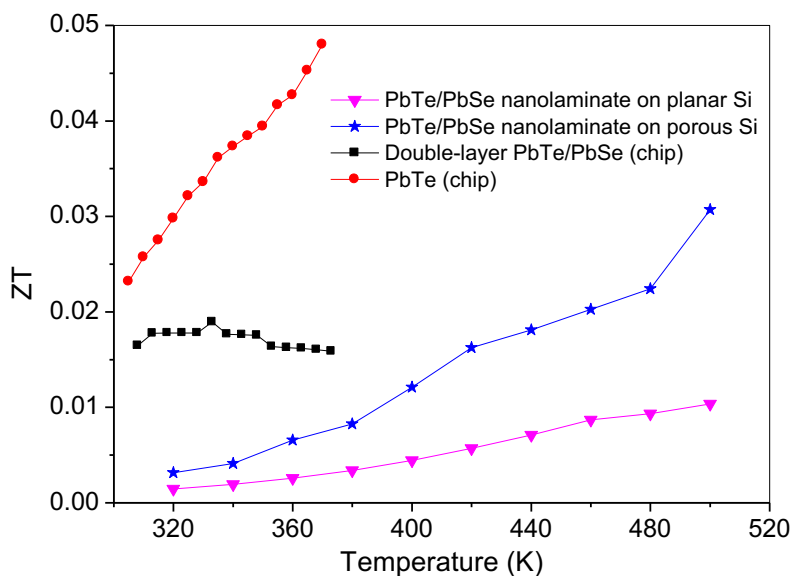


Figure 54. Comparison of ZT values for horizontal in-plane measurements with lab-on-a-chip test devices on non-structured planar ALD PbTe films benchmarked against ALD PbTe/PbSe nanolaminates on porous templates and planar Si substrates, where the thermal conductivity could only be determined in the vertical direction by the TDTR method.

TABLE IV

Comparison of the thermoelectric properties of our ALD PbTe/PbSe samples with literature reported values of PbTe/PbSe based nanostructures.

| Structure | Materials | Thermal Conductivity κ (W/mK) | Electrical Conductivity σ (S/cm) | Seebeck coefficient S (μ V/K) |
|---|---|--------------------------------------|---|--------------------------------------|
| Quantum Wells | PbTe/PbTe _{0.75} Se _{0.25} [43] | 0.5 | \ | -208 |
| Quantum Dots | PbTe/PbSe QDSLs [16] | 0.33 | 585.8 | -219 |
| Quantum Dots | (Pb _{0.95} Sn _{0.05} Te) _{0.92} (PbS) _{0.08} [23] | 0.4 | 6000 | -100 |
| Planar NL | PbTe/PbSe | 1.15 | 45 | -143.01 |
| Porous NL | PbTe/PbSe | 0.83 | 22 | -370.56 |
| Polycrystalline (all in-plane) | PbTe | 0.38 | 1.27 | 454.4 |
| Double-layer polycrystalline (all in-plane) | PbTe/PbSe | 0.17 | 0.47 | 438.71 |

Table IV shows the thermoelectric properties of our ALD PbTe/PbSe samples compared to the state-of-the-art thermoelectric properties for PbTe/PbSe based nanostructures reported in the literature. The thermal conductivity of our double-layer ALD PbTe/PbSe sample beats the lowest thermal conductivity reported in PbTe/PbSe quantum dots superlattice structures. For the ALD PbTe/PbSe nanolaminates grown on porous Si templates, the thermal conductivity in the horizontal in-plane direction is expected to be considerably lower. However, the TDTR method unfortunately allows only vertical measurements. At the present time, there is no experimental way to exfoliate and transfer the porous membrane onto the fragile thin Si₃N₄ based thermal conductivity test membrane of the Linseis ZT test chip. For this reason, we cannot measure the horizontal in-plane thermal conductivity of the most important porous thermoelectric samples by the test chip

platform. It is an unresolved experimental challenge to import porous Si templates onto the Linseis ZT test chip platform because the suspended fragile Si_3N_4 membrane is easily broken. Resolution of this issue would require a complete redesign of the Linseis thermal conductivity test device into a mechanically more robust structure. Regrettably these experimental constraints prevented the horizontal in-plane measurements of the thermal conductivity in porous patterned polycrystalline ALD PbTe/PbSe films, where the largest benefit in decreasing thermal conductivity is expected. The same argument holds for maximizing phonon scattering on pore boundary walls because only in the horizontal in-plane direction many more nano-pores will be encountered in comparison to the tiny vertical direction of the film thickness. Nevertheless, the experimental results indicate the both the grain boundaries from the polycrystalline ALD PbTe/PbSe films and the porous patterned structure do contribute to the reduction of thermal conductivity. In addition, our nano-structured ALD thermoelectric samples also exhibit higher Seebeck coefficients compared to other reported PbTe/PbSe based nanostructures, which can be attributed much lower thermal conductivity in our case. The electrical conductivity of our ALD synthesized samples is lower compared to reported values. This can easily be explained by the fact that our ALD thermoelectric samples are non-doped intrinsic samples. The electrical conductivity of our ALD PbTe/PbSe film can be improved by doping, but the doping level should be optimized to obtain a relatively higher Seebeck coefficient and lower thermal conductivity.

4.3 Summary

In this chapter, a lab-on-a-chip based thermoelectric test platform was applied in order to enable horizontal in-plane measurements of all key thermoelectric parameters like the Seebeck coefficient, the electrical conductivity and the thermal conductivity of thermoelectric films quasi-

simultaneously. Experimental constraints prevent transfer of porous templates to the test chip platform. Therefore, only single-layer non-structured planar ALD PbTe, planar ALD PbSe thin films and double-layer planar ALD PbTe/PbSe films were measured using the thermoelectric test chip platform. The Seebeck coefficient of both non-structured planar ALD PbTe films and ALD PbTe/PbSe films provided high values in the temperature range of 300 K~ 370 K. The maximum Seebeck coefficient was 458.76 $\mu\text{V/K}$ at 320 K for PbTe, and 441.71 $\mu\text{V/K}$ at 303 K. The discrepancy on the temperature dependence of the Seebeck coefficient for these two samples results from the lower carrier density in the PbTe/PbSe sample, which was further confirmed through electrical conductivity measurement. The temperature dependence of the electrical conductivity for single-layer PbTe and PbSe films exhibits pure semiconductor property, where the electrical conductivity increases as the temperature is increasing. Interestingly, the electrical conductivity of the ALD double-layer PbTe/PbSe films shows a reverse temperature dependence, indicating metallic behavior. Further investigations are needed to ascertain if PbTe/PbSe samples are potential candidates for topological insulators. For the thermal conductivity measurements, both ALD PbTe and PbSe samples exhibit very low horizontal in-plane thermal conductivity. The low thermal conductivity is attributed to massive grain boundary scattering occurring in the polycrystalline ALD PbTe and PbSe films. In the double-layer PbTe/PbSe film, the thin PbSe layer with the thickness lower than MFP of phonons enhances phonon scattering and plays an important role in further reducing thermal conductivity of the film. The highest ZT value of non-structured planar ALD PbTe films without any doping was 0.038 at 370 K. The full potential of phonon engineering in porous structured polycrystalline ALD thermoelectric films could not be measured because the fragile membrane of the ZT test chip platform does not allow transfer of the porous Si template. Therefore, we cannot measure the horizontal in-plane thermal conductivity in porous

thermoelectric samples, where the largest benefit in thermal conductivity reduction is expected. In conclusion, the vast potential of decreasing thermal conductivity in nano-structured thermoelectric ALD films by phonon engineering has been demonstrated. This fresh novel engineering approach highlights new possibilities for significant improvement of the thermoelectric Figure of Merit ZT when thermoelectric materials are structured on the length scale of the mean free path of phonons, thereby efficiently blocking phonon transport while hardly hindering charge carrier transport.

CHAPTER 5

5. CONCLUSION AND FUTURE WORK OUTLOOK

5.1 Conclusions

Thermoelectrics is a green renewable energy technology that plays an important role in power generation and power conservation due to its potential in generating electricity out of waste heat. But the practical application for thermoelectrics has been limited by its low conversion efficiency. Decreasing thermal conductivity is a key strategy for improving thermoelectric conversion efficiency. This can be achieved in thermoelectric materials in PGEC structures, low dimensional nanostructures, or phononic crystal structures. Those structures consist of numerous voids, rattlers, defects, dislocations, interfaces and grain boundaries, which effectively enhance phonon scattering thereby reducing the thermal conductivity and consequently improving the thermoelectric Figure of Merit ZT . In this thesis, the phononic engineering concept was implemented by ALD deposition of PbTe, PbSe films, and PbTe/PbSe nanolaminates on nano-patterned silicon substrates to improve thermoelectric performance of the thermoelectric films.

In chapter 2, the techniques used for thermoelectric film deposition and film characterization were introduced. Atomic Layer Deposition was applied for PbTe/PbSe synthesis on planar Si wafers and porous Si membranes and lithographically patterned Si substrates. ALD has the critical advantage of being able to deposit conformal films onto very complex 3-D structures and on the inside of cavities and negative slope surfaces, which has been confirmed in the ALD PbTe/PbSe nanolaminates films grown on patterned Si substrates. The film exhibits a uniform coverage on both the surface and sidewall of patterned substrates. The Seebeck coefficient in the horizontal in-plane direction and vertical direction was measured with an MMR Seebeck

Measurement System and an IR Seebeck Characterization System, respectively. For the characterization of the electrical properties, an Ecopia Hall Measurement System was used for in-plane electrical conductivity measurement. The TDTR method was used to measurement the thermal conductivity along vertical direction through the thermoelectric film thickness.

In chapter 3, the thermoelectric properties of the PbTe/PbSe nanolaminates grown on planar silicon wafers and the identical PbTe/PbSe nanolaminates grown on porous silicon templates were investigated and discussed. The results indicate the usage of porous Si templates enhances the Figure of Merit ZT by a factor of up to three at 500 K. This is attributed to the presence of the etched-out pores, which provide an additional periodic structuring of the nanolaminate composite sample to scatter phonons, increasing the Seebeck coefficient and reducing the thermal conductivity simultaneously. There is a small effect from the periodic structures also scattering charge carriers, resulting in a small reduction in the electrical conductivity of the porous samples. Since the mean free path of charge carriers is much smaller (10s nm scale) compared to the mean free path of phonons (0.1 ~ 10s μm scale), there is only a small price to pay in carrier scattering. From the stripe patterned samples, a significant reduction in thermal conductivity occurs when the width of the stripe patterns is less than 2 μm while the trench depth of the stripe patterns should be in excess of more than 500 nm. The generated thermoelectric voltage increases as the width of the stripe patterns decreases. The decreased thermal conductivity results from the enhanced phonon-boundary scattering due to the presence of periodic patterns as the size of patterns is approaching the mean free path of phonons. The increased thermoelectric voltage can be attributed to the increased thermal gradient since less Si conducts heat as the size of patterns is decreasing. This work demonstrated the feasibility of applying Nano-patterned TE elements into TE devices for an improved performance.

In chapter 4, a lab-on-a-chip based platform was applied for horizontal in-plane measurements of all critical thermoelectric parameters like the Seebeck coefficient S , the electrical conductivity κ and the thermal conductivity σ of thin films quasi-simultaneously. ALD Single-layer PbTe, PbSe thin film and double-layer PbTe/PbSe film were measured using the thermoelectric test chip. All the ALD samples exhibit high Seebeck coefficients of over 400 $\mu\text{V/K}$. The temperature dependence of the electrical conductivity for single-layer PbTe and PbSe films exhibits the pure semiconductor behavior. In contrast, the electrical conductivity of double-layer PbTe/PbSe films showed a reverse temperature dependence, indicating metallic property. Further investigations are needed to ascertain if ALD nanolaminate PbTe/PbSe samples are potential candidates for topological insulators. For the thermal conductivity measurements, all ALD planar PbTe and PbSe samples exhibit extremely low horizontal in-plane thermal conductivity. The low thermal conductivity is attributed to grain boundary scattering dominantly occurring in polycrystalline ALD PbTe and PbSe films. In the double-layer PbTe/PbSe film, the thin PbSe layer with the thickness lower than the mean free path (MFP) of phonons enhances phonon scattering and plays an important role in further reducing the thermal conductivity of the film. The highest ZT value of non-structured planar ALD PbTe films without any doping was 0.038 at 370 K. In conclusion, the vast potential of decreasing thermal conductivity in nano-structured thermoelectric ALD films by phonon engineering has been demonstrated and rendered to practice. This novel engineering approach highlights new possibilities for significant improvements of the thermoelectric Figure of Merit ZT.

As part of outlook and future work, the thermoelectric properties and application potential of non-traditional hybrid organic-inorganic Metal-Organic Framework (MOF) films were investigated.

5.2 Outlook for Metal-Organic-Framework (MOF) Films

Bulk MOF films are designed as scaffold-like compounds that consist of metal ions connected by organic ligands, forming highly ordered porous structures. These bulk MOF frameworks were initially designed for gas storage due to high storage capacity inside the porous MOF bulk material [92]. Initially their applications for electrical devices were very limited resulting from their electrically insulating characteristics. However, the electrical properties of bulk host MOFs can be modulated by infiltrating guest molecules (metal clusters) inside the porous MOF framework. This renders MOF materials a novel and promising material for microelectronic devices, sensors, and thermoelectrics [93-96].

Metal-organic frameworks are formed by connecting organic linkers via inorganic metal (or metal/oxo) clusters [97]. Due to their crystallinity, their thermal stability of typically up to 250°C and their open porous framework structure, this class of solids is highly adjustable and possesses interesting tailorable properties. For example, the size of the pores within MOFs has been reported to be highly tunable [98], and pore widths up to 10 nm [99] have been reported, yielding porous solids with extremely low densities. For the time being, bulk MOF powders constitute the de-facto standard modification of MOF materials. The typical product of the most commonly applied solvothermal synthesis method yields crystalline powders containing MOF crystallites with a widespread size distribution up to the mm range. Determining the electrical properties and behavior of this class of porous microcrystalline powder materials with conventional methods for powders is very difficult at best but is facilitated by using high quality and monolithic thin films of MOFs instead, which recently have been grown successfully by quasi-liquid phase epitaxy (LPE) [100]. Such monolithic and oriented MOF thin films are referred to as

surface-anchored metal-organic frameworks (SURMOFs). The superior elastic and mechanical properties of SURMOF films have already been reported for single layered materials as well as in multilayered architectures [101, 102].

Therefore, highly oriented SURMOF films offer a clear advantage in this context and lend themselves more easily to electrical characterization measurements. A number of different techniques and methods are currently known for preparing polycrystalline MOF coatings [103]. In addition, the deposition of MOF [104] materials have been described for the fabrication of electrical and microelectronic devices [105]. It is rather obvious that the electrical properties of porous MOFs/SURMOFs change when guest molecules are loaded into the pores of the framework. The first studies of this type were reported by Dragässer et al. [106], for the case of loading ferrocene inside monolithic HKUST-1 (acronym for Hong Kong University of Science & Technology) SURMOF thin films. Later, Talin et al. found that after loading TCNQ (Tetracyanoquinodimethane) molecules into the framework of HKUST-1, the electrical conductivity increased over six orders of magnitude with values up to 7 S m^{-1} in air [107]. The first models suggest that the conductivity arises from redox-active TCNQ guest molecules linking the copper paddlewheels within the open pores of HKUST-1. Charge transport between the TCNQ guests has been recently described and theoretically investigated by a second order process [108]. In this experimental study, it was also pointed out that inconsistencies exist between the electron-conducting mechanism proposed by the authors and the positive sign of the experimentally determined Seebeck-coefficient [109], which actually points to a hole-conducting mechanism instead [108].

In this work, the electrical properties of pristine (non-loaded) HKUST-1 and TCNQ loaded HKUST-1 SURMOF films were measured by Hall-Effect measurements. The MOF thin films

were grown on pretreated Si and SiO₂ non-conductive substrates using liquid phase epitaxy (LPE) in conjunction with a spray process already reported in our previous studies [104]. This process yields film thicknesses in the range of \approx 40-100 nm, depending on the number of spraying cycles used [110]. SURMOF films were characterized using X-ray diffraction and IRRAS measurements. Morphological studies through scanning electron microscope (SEM) cross-sectional measurements have been applied to check for continuity, homogeneity and compactness of the monolithic SURMOF thin films, as well as to detect possible meso/macro porosity within the epitaxial grown SURMOF coatings. Recently, a number of alternative procedures have been developed for the fabrication of MOF thin films, including dipping, spin-coating as well as electrochemical techniques. However, it has been difficult to achieve high quality oriented MOF thin films with low defect density using the above-described methods. In contrast, it is possible to grow SURMOF thin films of high morphological quality and low surface roughness by employing the controlled process of liquid phase epitaxy (LPE) on functionalized Au/Si substrates, as schematically shown in Figure 55b. Excellent quality polycrystalline HKUST-1 thin MOF films can be achieved on modified silicon and SiO₂ glass substrates, which is the essential prerequisite for enabling good electrical contacts and horizontal/planar conductivity measurements in order to obtain reproducible electrical measurement results. SURMOF films synthesized from other metal-organic framework systems have been studied in previous works with regard to their mechanical, optical/photonic [111], magnetic [112], or electrical [106] behavior, which are key properties for the desired functionality.

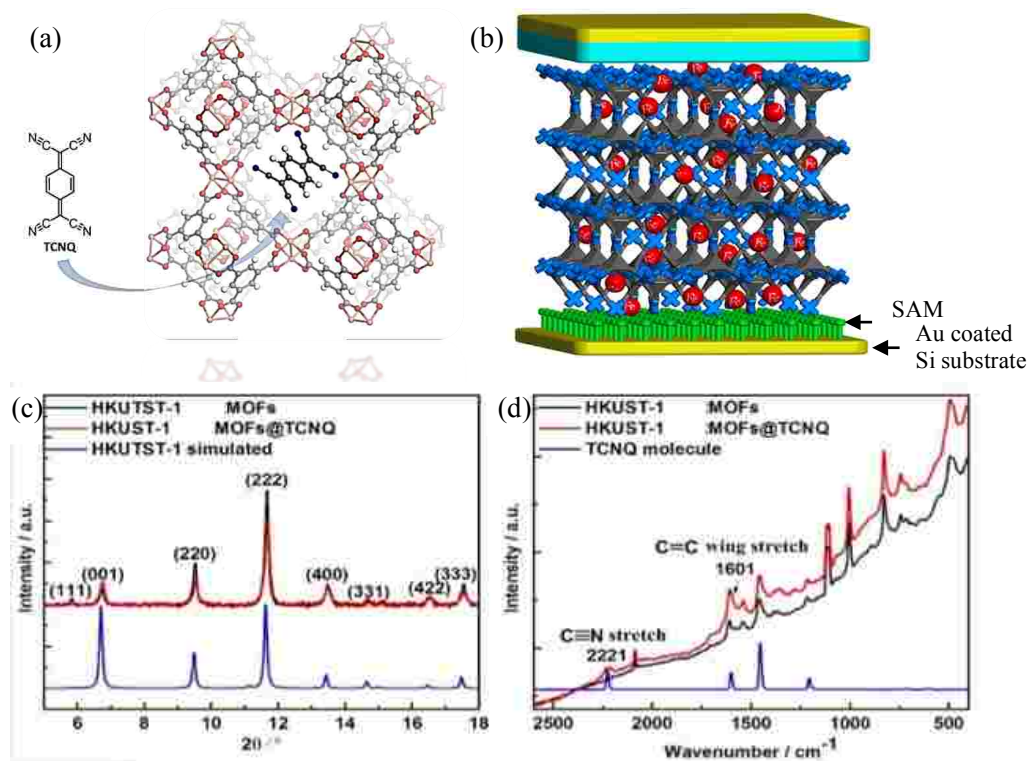


Figure 55. (a) Schematic illustration of the structure of HKUST-1 MOFs infiltrated with TCNQ (TCNQ, tetracyanoquinodimethane) in the pores. (b) Schematic diagram of HKUST-1 SURMOF grown on surface functionalized SAM layer [96]. (c) X-ray diffraction (XRD) patterns of pristine HKUST-1 SURMOFs and the HKUST-1 SURMOFs loaded with TCNQ [113]. (d) Raman spectrum of pristine HKUST-1 SURMOFs and the HKUST-1 SURMOFs loaded with TCNQ [113].

HKUST-1 MOF films are constructed from Cu^{++} dimers and benzene-tricarboxylate (BTC) units which form a crystalline, 3-D porous structure with a pore diameter of 1.2 nm, where the available pores allow the loading or storage of guest molecules for example TCNQ inside the MOF structure (see Figure 55 (a)). HKUST-1 MOF films used in this study were grown on plasma-treated silicon, quartz and glass substrates by LPE spray method [102], in which the metal-containing solution [1 mmol Copper (II) Acetate $\text{Cu}(\text{OAc})_2$] and the linker solution [0.1 mmol

BTC] are sprayed subsequently on the pretreated Si and quartz (SiO_2) substrate. For this study, the standard spray procedure was modified by omitting the rinsing process with pure ethanol in order to achieve random polycrystalline, non-orientated MOF films, which are required for horizontal/planar conductivity Hall Effect measurements. In contrast, highly oriented HKUST-1 thin films on functionalized Si/Au substrates have been used for resistive switching between two electrodes using aligned MOF pores for charge transport in the vertical direction [108].

The crystalline nature of the resulting HKUST-1 SURMOF films was verified by X-ray diffraction (XRD), and the resulting diffraction pattern is displayed in Figure 55 (b) (black curve). The XRD data clearly demonstrate the presence of polycrystalline HKUST-1 MOF films with random orientation of the individual crystallites. The experimental XRD data compare well with the simulated HKUST-1 MOF powder diffraction pattern. The loading of TCNQ into the HKUST-1 MOFs was carried out by a liquid-phase procedure, where the as-synthesized MOF thin film was first activated at 60 °C for 4 h to remove any remaining solvent stored in the pores of the MOF material. Subsequently, the samples were immersed in an ethanoic TCNQ solution (2mM) for 72 h at room temperature. Finally, the sample was rinsed using pure ethanol to remove the TCNQ molecules adsorbed on the surface. To ascertain the successful loading of TCNQ molecules, Raman spectra of the sample before and after loading as well as the drop cast TCNQ molecule on a gold covered substrate were recorded and are displayed in Figure 55 (c). The Raman spectra recorded after loading provide a clear signature of the TCNQ molecules, such as the peak at 2221 cm^{-1} and 1601 cm^{-1} wavenumbers. These signals were assigned to the C and N triple bond stretch and C and C double bond wing stretch, respectively. The other Raman-bands related to the HKUST MOF framework showed no changes after loading, which suggests that the infiltration with TCNQ did not change or deteriorate the HKUST-1 MOF host structure. XRD data received from the

sample after loading with TCNQ provided additional evidence that the thin films are still crystalline. The slight change of relative intensity is attributed to the form factor change after loading the guest molecule into the porous crystal structure. All chemical precursors used in this work are commercially available from Sigma Aldrich, and the silicon substrates were received from Silchem Handelsgesellschaft GmbH, Germany.

The desired film thickness can be adjusted using a number of distinct LPE spray cycles; e.g., 15, 25, 30 and 45 spray cycles for HKUST-1 result in a total thickness of ~40, ~60, ~70 and ~100 nm (see Figure 54, SEM cross-sections for further details). After the epitaxial growth of the SURMOF films, all samples were characterized using X-ray diffraction (XRD) with a D8-Advance Bruker AXS diffractometer with Cu K α radiation ($\lambda = 1.5418\text{\AA}$) in $\theta/2\theta$ geometry equipped with a position sensitive detector. XRD data have been recorded for all samples before and after loading with TCNQ molecules. Morphological studies were performed using cross-sectional images with a Hitachi S 4700 FE-SEM operated at 5 kV for SURMOF films on silicon substrates on an Al-SEM cross-section holder. Cu₃(BTC)₂ (BTC: benzene tricarboxylate) MOF films known as HKUST-1 MOF films were studied in this thesis. Liquid phase epitaxy (LPE) spray method was applied to grow HKUST-1 MOF films. We found that the MOF films grown on SAM surface functionalized gold coated silicon substrates and quartz result in oriented SURMOF films, while MOFs grown on non-treated thermally oxidized SiO₂/Si substrates gives rise to random polycrystalline MOF films. The tetracyano-quinodimethane (TCNQ) guest molecules were infiltrated into the MOFs to modulate the electrical properties of the film.

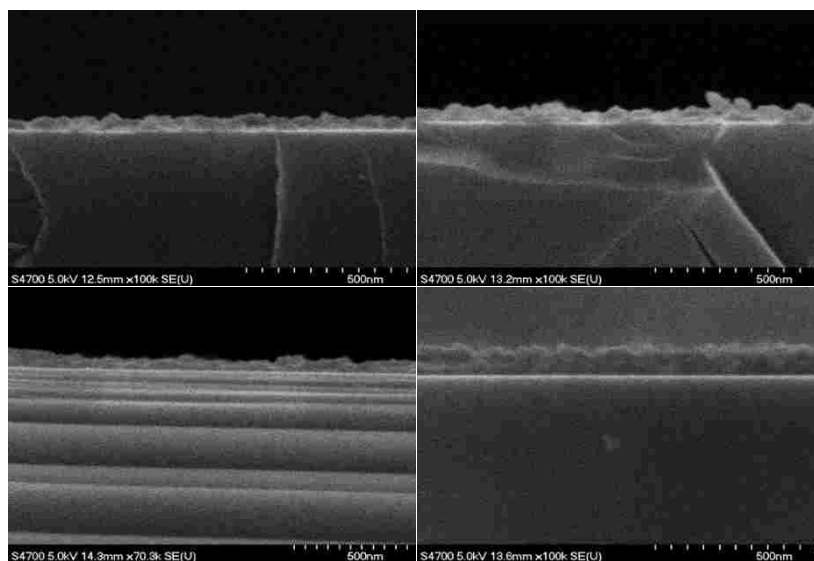


Figure 56. FE-SEM cross-sectional micrographs of MOF films with thickness of (a) 40 nm, (b) 60 nm, (c) 70 nm, and (d) 100 nm.

The Seebeck coefficient, electrical conductivity and thermal conductivity of both oriented SURMOF films and random polycrystalline MOF films were measured to investigate the thermoelectrical properties of the MOFs film.

Seebeck coefficient

The Seebeck coefficient of both 200 nm-thick random polycrystalline MOF films infiltrated with TCNQ and for comparison 100 nm-thick highly orientated SURMOF films with TCNQ loading were investigated in the temperature range of 290 K ~350 K. Figure 57 (a) plots the temperature dependence of the measured Seebeck coefficient of quasi-epitaxial highly oriented SURMOF films with and without (pristine) TCNQ infiltration. In both cases for pristine and loaded MOFs, the horizontal Seebeck coefficient of highly oriented SURMOF films is hardly measurable fluctuating around 0 $\mu\text{V}/\text{K}$ and in the noise level over the entire temperature testing range from

295 K to 350 K. In sharp contrast, the measured horizontal Seebeck coefficient is fairly high over the temperature range between 290 K and 350 K for random polycrystalline MOF films grown on thermal oxidized Si substrates with thick 484 nm SiO₂, which were either TCNQ loaded or pristine. The maximum measured Seebeck coefficient of TCNQ loaded polycrystalline MOFs with film thickness of 200 nm and TCNQ infiltration was 422.32 $\mu\text{V/K}$ at 350 K, see Figure 57 (b). This can be attributed to the fact that SURMOF films grown on SAM functionalized gold coated Si substrates exhibit a strong preferential orientation along the (001) direction [114] and have demonstrated good charge carrier transport only through the vertical direction with surface top contacts and backside contacts [96], while no carrier transport takes place in the horizontal direction parallel to the surface. However, all MOF films grown directly on thermally oxidized Si substrates without the use of SAM functionalized Au layers turned out into random polycrystalline MOF films. The isotropic nature of these random polycrystalline MOF films enabled charge carrier transport via all directions. For this reason, the measured horizontal Seebeck coefficient of highly oriented SURMOF films parallel to the surface was negligibly small around 0 $\mu\text{V/K}$, while the Seebeck coefficient of random oriented polycrystalline MOF films measured fairly high values. The measured high positive Seebeck coefficient of polycrystalline MOF films indicates the MOF films are p-type, so that the majority charge carriers are holes, which is consistent with reported work [109].

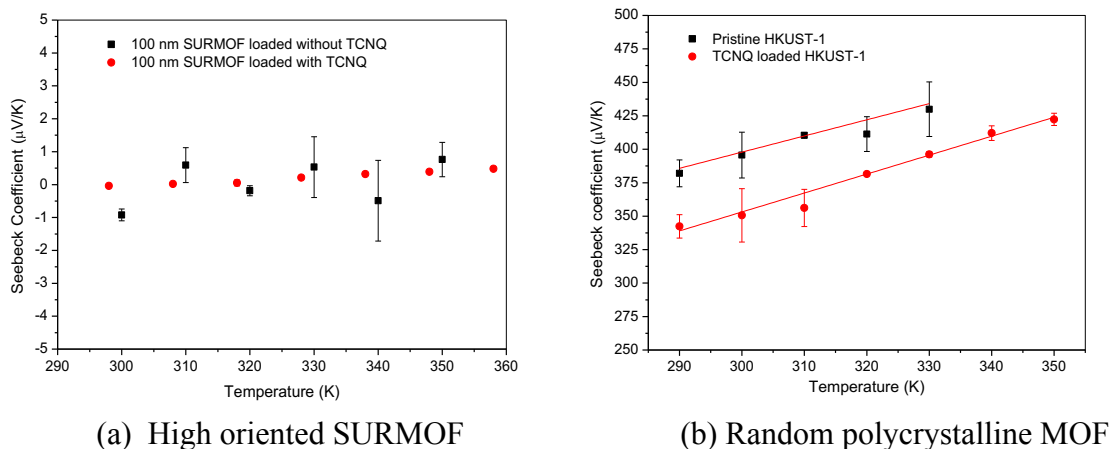


Figure 57. (a) Seebeck coefficient measurements as function of temperature of LPE highly oriented HKUST-1 films with a thickness of 100 nm, which were prepared with and without TCNQ loading. (b) Seebeck coefficient measurements of LPE polycrystalline HKUST-1 thin film with a thickness of 200 nm, which were prepared with and without TCNQ loading.

The positive Seebeck coefficient of TCNQ loaded MOF films increases linearly from 342.39 $\mu\text{V/K}$ to 422.32 $\mu\text{V/K}$ as the temperature rises from 290 K to 350 K. This may be attributed to the fact that thermal activation generates more holes contributing to the Seebeck coefficient as the temperature is increasing. A maximum Seebeck coefficient would be expected at higher temperature where intrinsic transport behavior starts to dominate. The temperature dependence of the Seebeck coefficient of the pristine MOF film exhibits the same slope and tendency over the temperature range between 290 K and 330 K, where the Seebeck graph of the pristine MOF film appears parallel, shifted to higher values by approximately 50 $\mu\text{V/K}$. These measurements establish that the temperature dependent Seebeck coefficient of the pristine non-infiltrated MOF films is higher compared to the TCNQ loaded MOF films. This can be understood as follows. The Seebeck coefficient S is inversely related to electrical conductivity σ by the relationship from

Eq. 5 $S = \frac{8\pi^2 k_B^2}{3eh^2} m^* T \left(\frac{\pi}{3n}\right)^{\frac{2}{3}}$ and $\sigma = ne\mu$, where n is carrier density, μ is the carrier mobility, k_B is the Boltzmann constant, h is the Planck's constant, m^* is the effective mass of the charge carrier, T is the temperature and e is the electron carrier charge [37]. This relationship of decreasing Seebeck coefficient as a function of increasing charge carrier density has also been illustrated in Figure 5. Therefore, the fact that TCNQ loading effectively enhances the electrical conductivity of isotropic polycrystalline MOF films has to result in a lower Seebeck coefficient, while at the same time the lower electrical conductivity and lower carrier density of pristine polycrystalline MOF films has to result in higher Seebeck coefficients, which was observed in the plot of Figure 57 (b) [107].

Electrical Conductivity

To investigate the electrical properties of MOFs, the I-V-characteristic curves of oriented MOFs grown on quartz and polycrystalline MOFs grown on thermal oxide SiO₂/Si wafer was measured with an Ecopia HMS-5300 Hall Effect Measurement System. Figure 58 shows the schematic sample stage pre-structured with four bottom Au contacts, and the Hall Measurement stage mounted with an actual MOF sample. Figure 59 displays the I-V curves of polycrystalline MOF films with and without TCNQ infiltration. The measurements demonstrate that the TCNQ loading results in a measurable I-V curve, while the pristine non-loaded MOF films exhibit really poor conductivity. For comparison and in stark contrast, the I-V curve of highly oriented MOF films grown on quartz shown in Figure 60 reveal that TCNQ loading has no influence on improving horizontal electrical conduction in highly oriented MOF films. Both TCNQ loaded and pristine MOF films show a negligibly tiny current in the voltage range from -10 V to 10 V. This results further demonstrates that these highly oriented MOF films exhibit a large electrical anisotropy

with no charge carrier transport in horizontal direction parallel to the sample surface, but only carrier transport in the vertical direction, where switching effects have been reported [96].

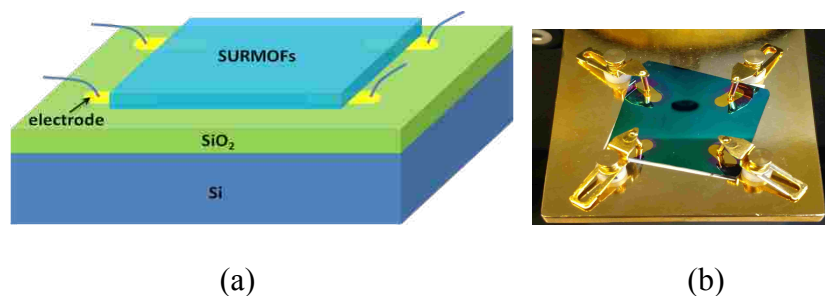


Figure 58. (a) Schematic of the MOF samples with four bottom contacts. (b) Hall Effect measurement stage with square MOF sample with sputtered Au bottom contacts in the four corners for a Van der Pauw configuration.

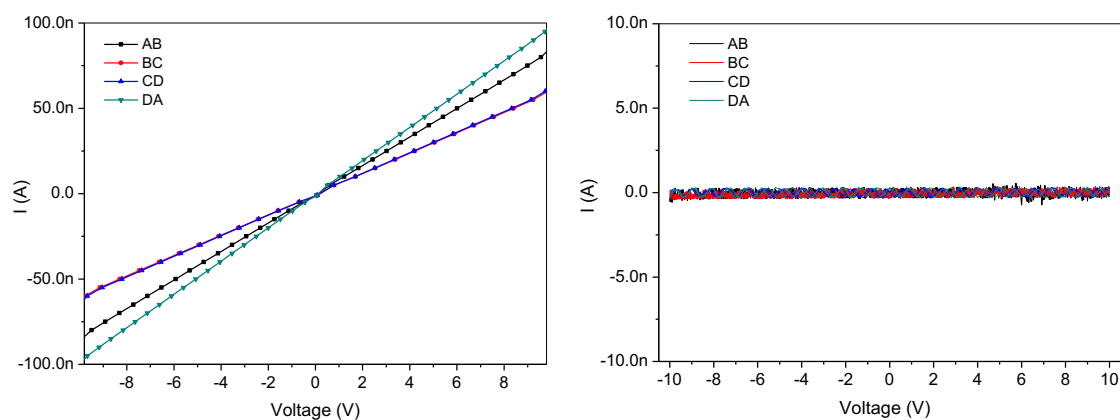


Figure 59. (a) *I-V* characteristic of TCNQ loaded polycrystalline MOF films grown on glass. (b) *I-V* characteristic of pristine random polycrystalline MOF film grown on glass. Infiltration with TCNQ molecules greatly improves the electrical conductivity of polycrystalline MOF films. The MOF films grown on glass produce random polycrystalline films that allow the majority charge carrier –hole transport through any directions.

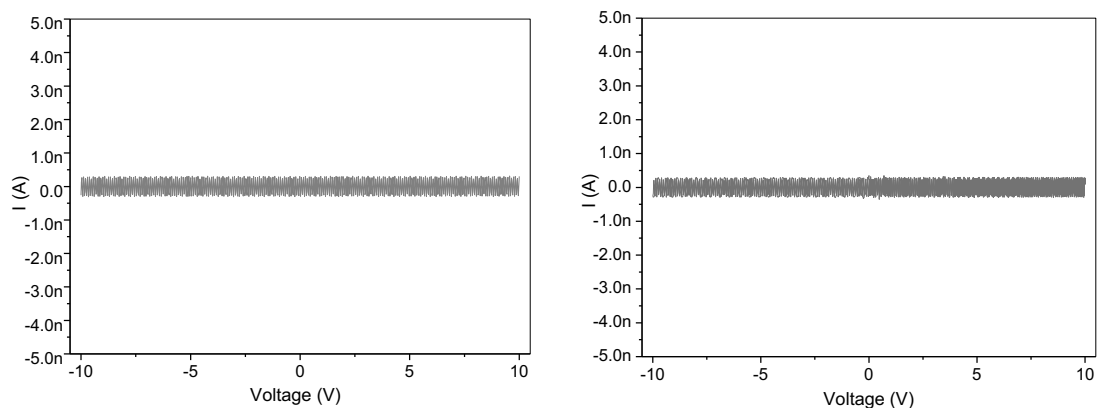


Figure 60. (a) *I-V* characteristics of highly oriented pristine MOF films grown on surface functionalized quartz. (b) *I-V* characteristic of highly oriented MOF films grown on functionalized quartz and loaded with TCNQ.

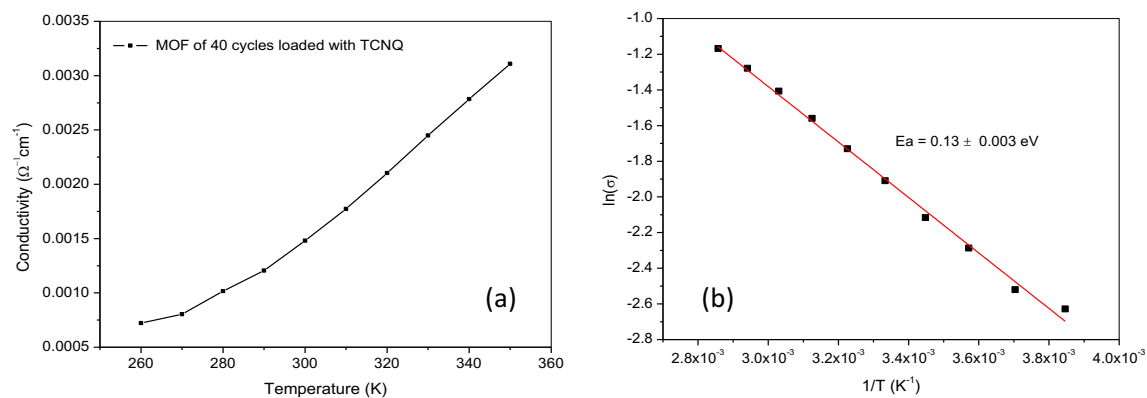


Figure 61. (a) Temperature dependence of electrical conductivity of TCNQ loaded polycrystalline MOF film grown on insulating glass substrates. (b) Arrhenius plot of $\ln(\sigma(T))$ versus T^{-1} .

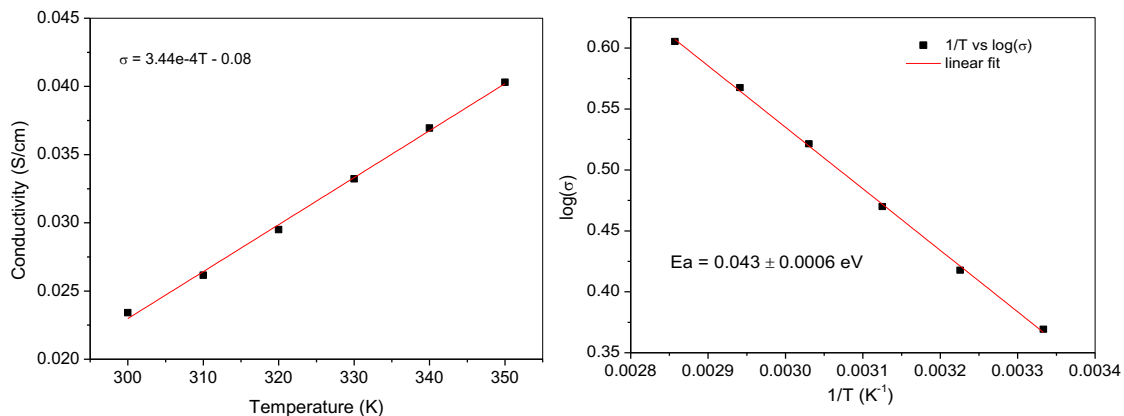


Figure 62. (a) Temperature dependence of electrical conductivity of TCNQ loaded MOF grown on thick SiO₂ covered Si substrates. (b) Arrhenius plot of $\ln(\sigma(T))$ versus T^{-1} .

Figure 61 plots the temperature dependence of the electrical conductivity of random polycrystalline MOF films of ~130 nm thickness grown on glass substrates in the temperature range of 260 ~ 350 K and measured with an Ecopia HMS-5300 measurement system. As the temperature is increasing, the electrical conductivity also increases, which results from thermal activation generating more charge carriers. The red line is linear fit that could represent a thermally activated process with activation energy of 0.13 eV. The electrical conductivity over the temperature range of 260 ~350 K of polycrystalline MOF films with ~40 nm thickness grown on thick thermal SiO₂ covered Si substrates with bottom Au contacts is plotted in Figure 62. The red line is linear fit that could represent a thermally activated process with activation energy of 0.043 eV. The slope of the Arrhenius plot can be seen as E_a/k , where E_a represents activation energy, and k is Boltzmann constant. A low activation energy generally leads to a high charge density and hence high electrical conductivity. The E_a of MOF films grown on thick SiO₂ covered Si substrates is smaller compared to the MOF films grown on soda lime glasses, indicating the MOF films grown on SiO₂/Si substrates exhibit a higher electrical conductivity. This can be attributed to the

difference between relatively loosely stacked and more porous bulk MOF materials grown on glass versus compact and dense MOF films grown on the SiO₂/Si substrates. The investigations on Metal-Organic-Framework (MOF) films indicate polycrystalline TCNQ loaded MOFs is a promising TE material at low temperature range.

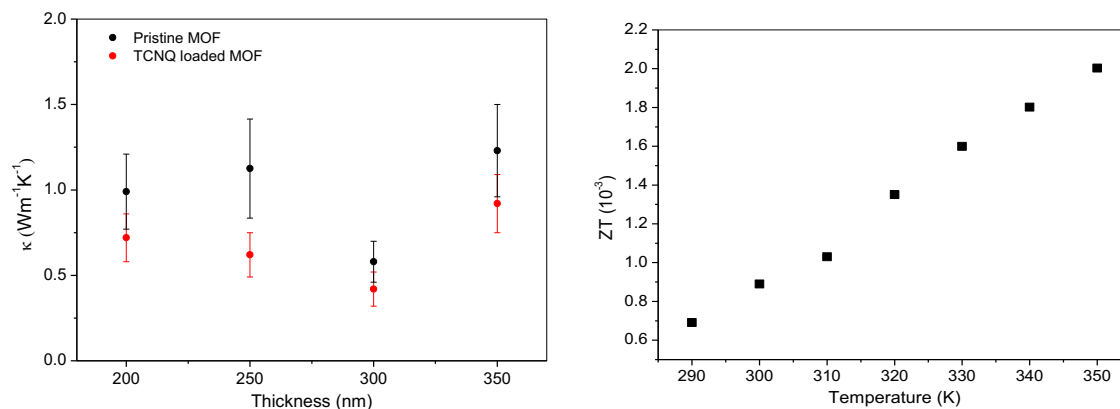


Figure 63. (a) Plot of Thermal Conductivity versus temperature of pristine and TCNQ loaded polycrystalline MOF films with different thicknesses. (b) plot of calculated thermoelectric Figure of Merit ZT as a function of temperature obtained from the measured Seebeck coefficient, electrical conductivity and thermal conductivity.

Figure 63 (a) compares the thermal conductivity of pristine and TCNQ loaded polycrystalline MOF films. The TCNQ loading results in great enhancement of the electrical conductivity and surprisingly also results in a concurrent reduction of thermal conductivity. The electrical conductivity of the MOF film increases as the temperature rises, which is resulting from enhanced mobility and increased hole generation at higher temperature. These results demonstrate that the presence of infiltrated TCNQ molecules in the MOF pores introduces Einstein modes that can scatter framework phonons. This is known as the “rattling” mechanism in the literature on

Skutterudites and Clathrates. It is believed that the weakly interacting guest molecules entrapped in the host cages introduce Einstein modes that can scatter phonons.

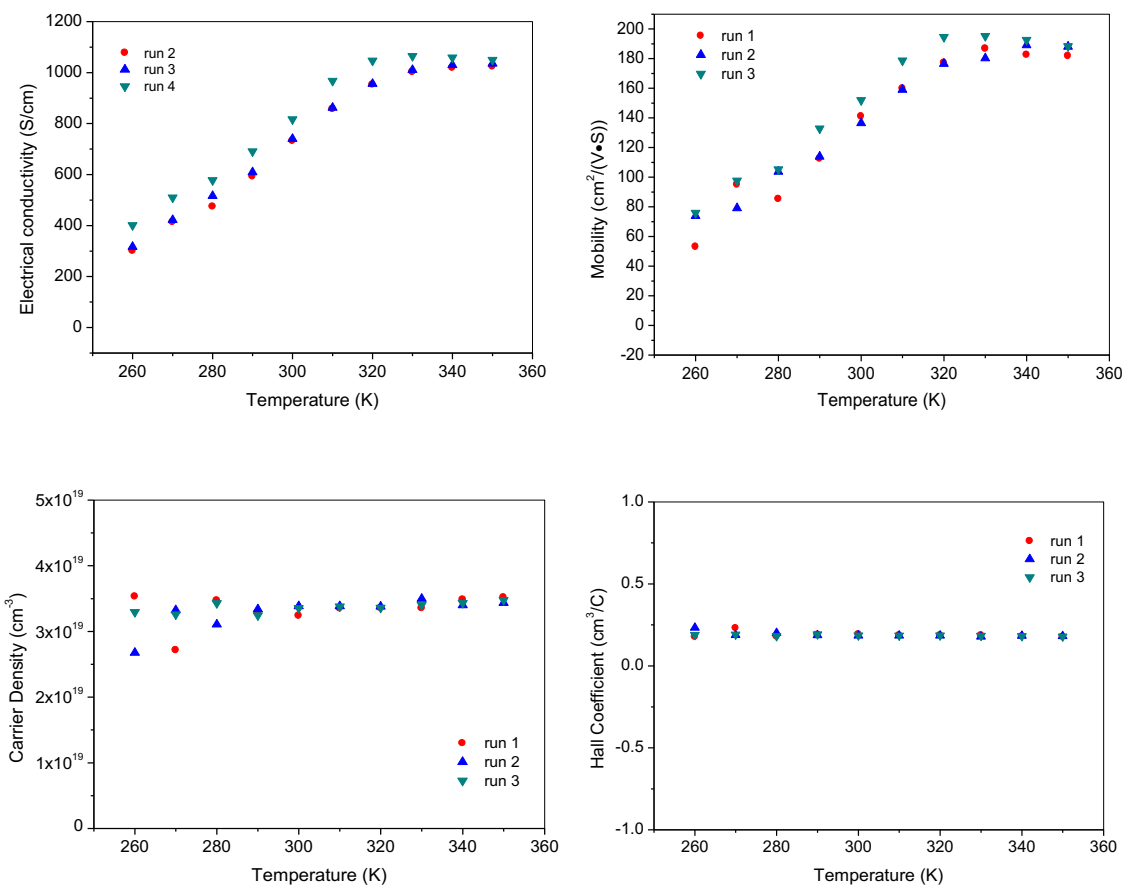


Figure 64. Plotting the temperature dependence of (a) the electrical conductivity (b) the Hall mobility, (c) the carrier density, and (d) the Hall coefficient of TCNQ loaded polycrystalline MOF films grown of ~ 40 nm grown on thick SiO_2 covered Si substrates using Au bottom contacts.

Figure 63 (b) displays the Figure of Merit ZT for TCNQ loaded MOF films as a function of temperature. The highest ZT is about 2.1×10^{-3} , which is fairly low for practical TE applications. The low ZT is mainly attributed to the low electrical conductivity of the current MOF films. The conclusion from these values is straightforward: Further measures have to be taken to improve the

electrical conductivity of MOF films in order to obtain useful ZT number for potential future TE applications of MOFs. TCNQ loaded MOF films exhibit higher Seebeck coefficient and extremely low thermal conductivity κ in the temperature range of 290 ~ 350 K, which render MOF films a promising TE material for TE applications around room temperature and a potentially inexpensive alternative hybrid organic-inorganic thermoelectric material.

5.3 Future Work

In this dissertation work, the phonon engineering concept was implemented to reduce thermal conductivity and enhance the Figure of Merit ZT of thermoelectric thin films. Porous membranes and stripe patterned Si substrates were applied as substrates for conformal ALD thermoelectric film deposition. The utilization of porous Si templates enhances the ZT of PbTe/PbSe nanolaminates by a factor of three, which demonstrates the feasibility of improving thermoelectric conversion efficiency by applying porous substrates. However, the maximum ZT value for the porous nanolaminates was 0.03 at 500 K, which is quite small for practical thermoelectrical application. One reason for the small ZT is low electrical conductivity, caused by non-doped intrinsic PbTe and PbSe films and materials degradation after deposition. Doping is a popular approach to improve the electrical conductivity. Impurity doping and electrical activation with Atomic Layer Deposition can be achieved by post-annealing at a higher temperature. Na and Bi are commonly used for p-type and n-type doping of PbTe and PbSe material. In general, doping PbTe/PbSe samples is considered a challenge. Since PbTe and PbSe films are easily oxidized and degraded at high temperatures, post-annealing with flowing nitrogen gas atmosphere cannot avoid

oxidation and degradation of the PbTe and PbSe samples from experimental experience. A high vacuum furnace may be required to achieve doped PbTe/PbSe films with high quality.

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