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Experimental Super High Frequency Rectifier And DC To DC Converter For Application In Space Solar Power

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EXPERIMENTAL SUPER HIGH FREQUENCY RECTIFIER AND DC TO DC CONVERTER FOR APPLICATION IN SPACE SOLAR POWER

by

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This thesis, submitted by Robert C. Bernaciak in partial fulfillment of the requirements for the Degree of Master of Science from the University of North Dakota, has been read by the Faculty Advisory Committee under whom the work has been done and is hereby approved.

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Robert C. Bernaciak
08 December 2016

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Dedicated to my wife Thyra, my father Pete,
My mother Carol and my sister Erin.

ABSTRACT

Due to the continuous rise in the global energy demands, new sources of fuel and energy need to be explored. One area of research that is currently underdeveloped is the study and application of space solar power. Space solar power (SSP) is a broad topic that covers the idea of capturing and transmitting renewable solar energy from space to earth. There has been lots of research in the area of SSP, but there are yet any test platforms operating in space continuously to gather data for supporting the commercialization of SSP. This research document looks at the design of the sub assembly level of components while keeping in mind the end application of SSP. The most innovative idea of this research work to be implemented is adding a DC to DC converter to a rectenna array to regulate the output so that the output may be used in a constant charging application. A rectenna is a rectifying antenna used to convert microwave energy into a DC output. The process used in the following work developed a rectifier that has been shown to work through simulations and a buck/boost converter to regulate the output voltage from the rectifier. Simulations using the developed rectifier produced more than 1.8V DC when excited by two 6V peak to peak 5.8GHz sine waves. The sine waves were out of phase by 180^{o}. The filter on the designed rectifier was able to reject re-radiation of the 2^{nd} and 3^{rd} harmonics of the 5.8 GHz input signal by more than 25 dB and 22 dB, respectively. The efficiency of the designed rectifier is unknown due to the simulations not having a current output for a power calculation and the assembled prototypes did not produce any measurable results. The efficiency of the buck/boost

converter has been measured to be 80% efficient and up to 95% efficient, depending on the input voltage and the load requirements.

I. INTRODUCTION

The demand for renewable energy does not appear to be slowing down anytime soon. The desire for more renewable energy has led to a continuous study and investigation of space solar power (SSP). SSP is the idea or concept in which solar energy is harvested by satellites in space and then the energy can be wirelessly transmitted to the surface of the earth using microwaves. The transmission of wireless power via microwaves can be used in numerous applications including powering other satellites (Figure 1), space missions or space travel, used on Earth (Figure 2), and many other applications [1].

Figure 1: Image of a wireless power transmitting and receiving satellite [1]

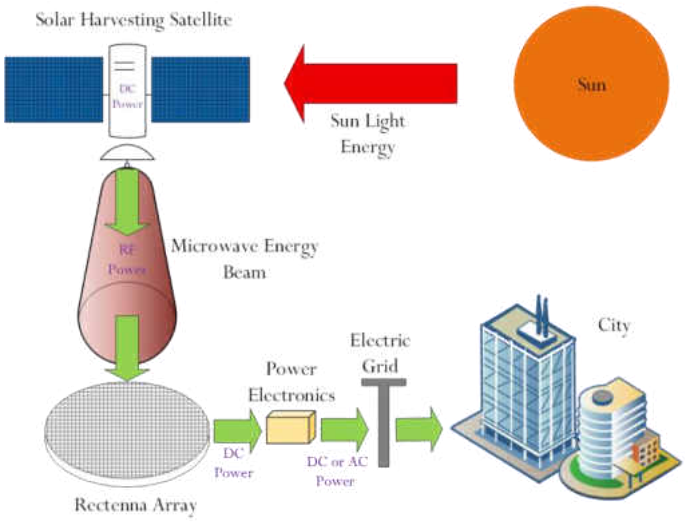

Figure 2: Grid tied overview of space solar power [1]

In recent years, there have been numerous researchers and institutions working to advance the systems of SSP so that they could one day be used commercially for microwave wireless power transmission (MWPT) systems. The technology that is being improved for MWPT are the power receiving antenna arrays, rectifiers, and receiving antenna arrays, which will improve the end-to-end system of MWPT systems. MWPT is often received by an integrated microwave antenna and a DC rectifier on a single substrate. The union of the antenna and rectifier into a single design is called a rectenna. Rectennas and their arrays are by no means a novel idea due to the amount of research conducted on them in the past and the current numerous ongoing studies around the world. The general layout of a rectenna can be seen in Figure 3, which was obtained from [2]. The following sections will discuss the approach, design and testing of a single rectifier to be used in conjunction with an antenna developed by another member of the research team.

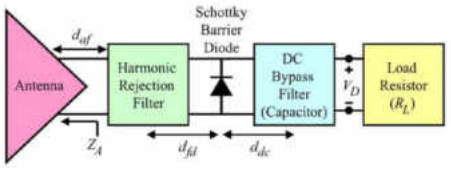

Figure 3: Block diagram of a rectenna [2].

a. State-of-the-Art:

Wireless power transmission (WPT) has been experimented with all the way back to 1879 when David Edward Hughes became the inventor of the crystal radio. People to follow Hughes' work with WPT included Heinrich Hertz with his work on electromagnetic wave propagation and Nikola Tesla with his work on wireless power transmission towers or commonly known as Tesla Coils or his large-scale project of the Tesla Towers. Modern WPT has been forever improved through the inventions of two devices conceived around 1940 by the Klystron tube and the magnetron [2].

The most relevant modern history of WPT began with the works of William Brown of the Raytheon Company. In 1971 the Raytheon Corporation conducted a full-scale experiment of a MWPT system for beam collection and rectification resulting in an efficiency of 82.4% at 2.446GHz [2]. The 82.4% system efficiency achieved by Raytheon was measured from the beam collection to the output of the rectification. Since then, the current state-of-the-art radio frequency (RF) to direct current (DC) rectifiers operating at Super High Frequencies (SHF), 3GHz-30GHz, have achieved efficiencies up to 60% at 10GHz [3]. The measured 60% efficiency includes the losses of the antenna, not just the rectifier [3]. When comparing different designs, one has to keep in mind the type of subsystems that are included in the efficiency calculations and the frequency at which the results are obtained. If two tests do not have the same system included

in the efficiency calculations or the same operating frequency, then the two tests cannot be directly compared.

One system that has seen several improvements is the RF-to-DC conversion. This subsystem has been achieving efficiencies greater than 82% since at least 1974. In 1974 Brown and other Raytheon colleagues achieved a RF to DC conversion efficiency of 82.4% with a 2.446GHz signal [2]. The 1974 testing by Brown was technically not a small-scale test, but the measured results of a full-scale experiment on the specific portion of the system directly pertinent to the state-of-the-art for this paper. On the larger scale side of MWPT, a test in 1975 was conducted by a collaboration between Brown at Raytheon, NASA, and the Jet Propulsion laboratory (JPL). The 1975 testing was completed with a one mile distance between the transmission antenna and the receiving rectenna. The first MWPT experiment in space was the International Space Year – Microwave Energy Transmission in Space (ISY-METS). ISY-METS transferred energy from one rocket to another while in space. The experiment used microstrip antennas on the transmitting rocket and two different rectennas on the rocket that received the antennas [2].

In 1998 James McSpaden developed a rectifier that used a printed dipole antenna and a Silicon Schottky diode to achieve a RF-to-DC conversion efficiency of 82% [4]. Since then several new techniques for designing rectennas have been developed. In 2000 Texas A&M researchers developed a RF-to-DC converter that utilizes a circularly polarized pair of antennas with improved Schottky diodes. The Texas A&M researchers achieved an efficiency of 82% with a 5.8 GHz signal

[2]. The improved Schottky diodes have lower parasitic capacitances with allow the diodes to be faster and thus more efficient when changing between conducting and blocking modes.

Although the 2008 experiment conducted by John Makins is not a feat of engineering for its efficiency, it is a feat of engineering in overcoming regulations and budgetary constraints for the distance tested. In 2008 Mankins transmitted using an antenna array on Maui, HI, and received the power on the Island of Hawaii, HI (The big island). His power received was less than $1/1000^{th}$ of 1%. However, his impressive distance traveled was 148km (91miles). Mankins budget for the experiment was less than a million dollars restricting the size of his transmitting and receiving arrays. Mankins accomplished this with the collaboration of researchers at Texas A&M University (TX, USA) and Kobe University (Kobe, Japan) [2].

The operating frequency (center frequency) of 5.8GHz is most often chosen as a compromise in transmission and reception system size, the ability of the microwave energy to travel through the atmosphere with minor attenuation losses and the ability to transmit long distances. The higher the frequency the less efficient a system will be in the rectification process. The efficiency loss is due to the electrical parts not operating as efficiently due to parasitic effects of capacitance and resistance that are internal to the diodes and capacitors used in rectifiers. However, the increased frequency gives a longer transmission distance because it takes longer for the beam of transmitted power to spread out and leads to a reduction in the size of the MWPT system [3].

Previous rectifier designs used in MWPT developments have focused on half wave rectifiers. Half wave rectifiers decrease the number of parts needed, compared to full wave

rectifier designs, thus simplifying the design [2]. Half wave rectifiers are also commonly used since there is a nominal gain in efficiency when compared to a full wave rectifier in the SHF range [5, 6]. These designs often have a single diode to convert the energy. As shown in Figure 3, typical topology for a SHF rectifier is an input filter, a single shunt diode and an output capacitor to short the remaining RF energy [2, 5]. The typical MWPT rectifier design is shown in Figure 4 (a), and can be compared to a charge pump topology using multiple diodes in Figure 4 (b). A charge pump is a half wave rectifier that continuously multiplies the voltage output relative to the input voltage received. Another common name for a charge pump is a voltage doubler. The charge pump is often used in extremely low power designs, such as Radio Frequency Identification (RFID) applications [5].

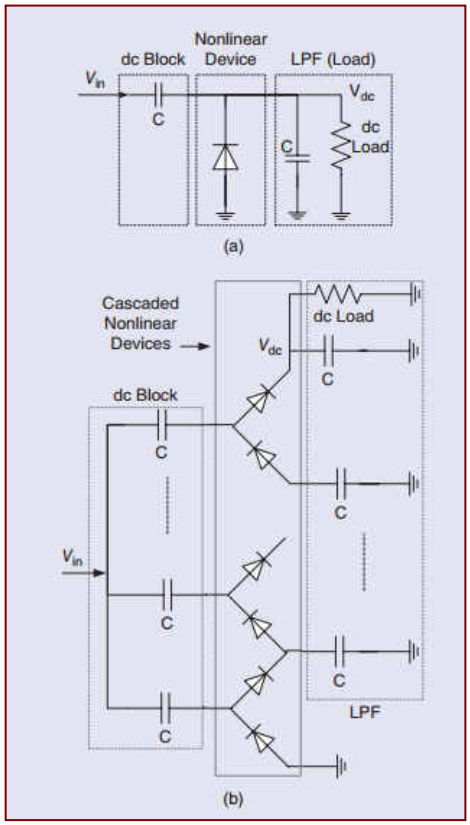

Figure 4: RF-DC converters: (a) single diode detector, (b) a charge pump [5].

The most common method to connect the rectifiers and antennas in rectennas is by using Co-Planar Strips (CPSs). CPSs are typically impedance matched to the diode and the antenna to maintain the highest power transfer to the load [7]. Impedance matching means that each component has the same impedance so that the power received is divided equally among all parts of the system. Previous research has focused on increasing the rectification efficiency. This has been done by using a fixed load connected directly to the output of the rectifier.

Previous designs have not yet leveraged the advantages from recent discoveries to build a scale model for a specific business case, such as Space Solar Powered Satellite (SSPS) energy utility. In 2009 there was a public release stating that Solaren Corporation would launch and begin selling energy using a Space Solar Power (SSP) system to transmit MWP by the year 2016 [8]. Since the Solaren public announcement in 2009, there has been no indication through public releases to judge if the company will indeed be able to make their intended goal of production starting in 2016. Other researchers, such as Susumu Sasaki of the Japan Aerospace Exploration Agency, have suggested that a commercialized version of SSP system would be viable by the year 2030 or later [9].

b. Research Problem:

To advance a technology into the production stage of a life cycle one transition that needs to be made is from the technology development process (TDP) to the product development process (PDP). From the state-of-the-art it can be seen that several entities are looking into not just the TDP of MWPT, but they are also looking into the PDP of MWPT. The ongoing research to design space solar power systems (SSPSs) could one day be the future electrical energy source

for Earth. To stay current with product development, research entities should also be looking at the system level incorporation of the MWPT technologies. In order for MWPT to be a commercially viable option, the design of rectennas and their Power Management and Distribution (PMAD) systems are essential to meeting an adequate end-to-end efficiency.

The following section will discuss a development process used to produce subsystem prototypes of the Rectifier, rectenna filter, and power converter; which are intended to be able to test the proof of concept of a full scale rectenna array design. The full scale rectenna array and PMAD design should eventually lead to the production and testing of an orbiting spacecraft. Due to the lack of funding towards SSPSs and the complexity of testing a full-scale system, the subsystems of a commercially viable MWPT system need to be dissected and improved towards a better overall efficiency [2].

To break apart the MWPT system into manageable pieces, only a portion of the power receiving spacecraft, such as the receiving satellite seen in Figure 1, will be discussed. This research work will focus on the power conversion (rectenna), regulation (rectenna array), and its management (PMAD) onboard a receiving satellite. Those three things will begin immediately after the power has been received by the antennas that are located on the power receiving satellite as shown in Figure 1. The power converter will be a rectifier that will connect to the antenna and form a rectenna. For simplicity, the power regulation will be considered a sub set of the power management system. The power regulation and power management will be referred to as the PMAD system. The parts being designed can be seen in the green blocks in Figure 5.

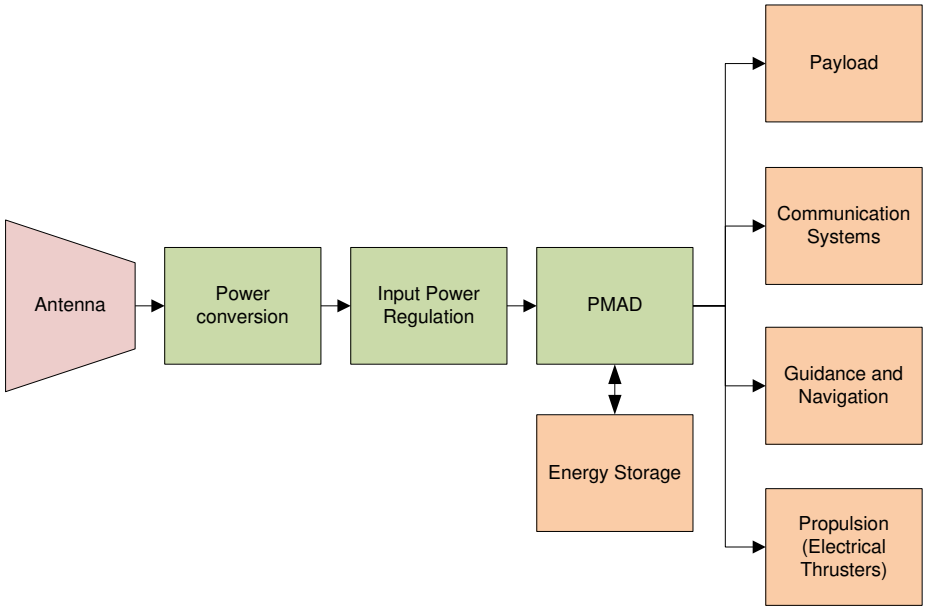

Figure 5: MWPT receiving satellite power flowchart

c. Methodology:

To conduct the proposed work, the following tasks were performed.

Task 1: Conduct a literature review to understand previous work on MWPT systems. In order to design an efficient rectifier and its associated PMAD for the MWPT system, further investigation into the characteristics and performance of previous designs is necessary. This investigation exercise would help in a thorough understanding of the previous MWPT designs. The advantages of each previous designs can then be leveraged for the optimal design of the new MWPT system proposed. The design goal of the rectifier was to have an efficiency of 70%. An additional understanding of Schottky Diodes needed to be obtained. An initial literature search revealed that numerous researchers point to using them in their rectifier designs [2, 5].

Task 2: Design and verify the rectifier circuit. Several rectifying topologies were researched to determine the best conversion efficiency. Rectifier topologies that were

investigated are single shunt diode [2, 4, 5], dual diodes [10], full wave rectifiers [6], and charge pumps [11]. Since the larger picture of this project was to create a rectenna, a coplanar strip was investigated as the transmission and filtering method for each of the aforementioned rectifier circuits.

After researching each rectifier topology, the design that meets the needs of the SSPS system best was chosen. The chosen topology was simulated in the software package CST Studio Suite [12]. Through design analysis and results from simulations, the selected rectifier topology was tuned to a frequency of 5.8 GHz. This frequency has an accumulated history, has less regulation by the FCC, and has the necessary properties of propagation through the atmosphere for transmission to earth [2]. The Federal Communication Commission (FCC) has deregulated the center frequencies for 2.45 GHz, 5.8 GHz, 24.125 GHz and many other center frequencies for Industrial, Scientific, and Medical (ISM) use and research. These ISM band frequencies are unregulated so that armatures and corporations can use these RF bands for private or public communication between devices. Some devices that operate in these bands are microwave ovens, cordless phones, Wireless LANs (Wifi and Bluetooth), and many other applications. Simulation and design iterations will produce the expected efficiency of the chosen topology and would aid in the design of the harmonic rejection filter as will be covered in Chapter “II”, Section “b”, Sub-section “iii”. As stated earlier, the efficiency goal of the rectification process was set at 70%. After simulation studies were completed and the appropriate rectifier design was selected and finalized, the physical rectifier circuit was fabricated and tested for its efficiency.

The amount of output power from the rectifier depends on the power received from the transmitting antenna. Previous research work suggests that the rectenna array receives a power

irradiance of about 25mW/cm^2 at the center and about 1mW/cm^2 at the outer edges of the array [13]. The size of the rectenna array will be 30 cm by 30 cm as determined by the area of the surface of the application aboard a one unit (1U) class CubeSat. More description of the 1U CubeSat will be provided in the Sub-section "d" of this Chapter. The size of the rectenna array will greatly impact the rectifier design and the PMAD system. An example of a rectenna array design is shown in Figure 6.

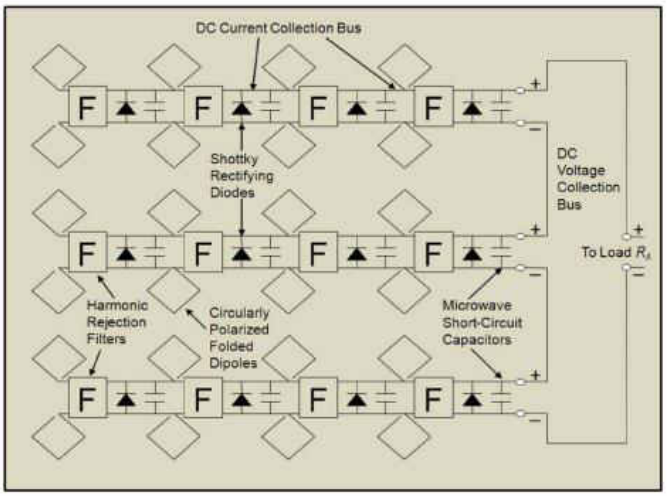

Figure 6: An Array of 12 individual rectennas [2].

Task 3: Design and verify the PMAD system. The last design aspect of this work focused on the PMAD system. A buck/boost converter design was the primary candidate for the PMAD design of this work. The efficiency of the PMAD power transfer capability was expected to be above 85%.

Task 4: Perform research on how to design an array of rectennas. This process was similar to designing an array of photovoltaic panels to be regulated by a charge controller. Using the output of the rectennas, the PMAD was designed to maintain a constant voltage level on the

load side of the rectenna array. The constant voltage from the designed PMAD, allow multiple rectenna arrays to be combined in parallel as shown in Figure 6. In Figure 6, the PMAD will be placed where "To load R_L" is shown and the load will be connected to the output of the PMAD.

d. System Application and Design Constraints

Throughout the design process of this work the goal will be to design the rectifier and PMAD as if they were going to be used in space, by attempting to use space qualified parts and materials to maintain a sense of authenticity for the designated application on SSPSs. The PMAD system described is intended to be implemented on an experimental satellite that will test the viability of MWPT in a scaled test in outer space.

The satellite mentioned in this design is receiving the MWPT. The proposed initial space application is aboard a 1 Unit (1U) CubeSat. The CubeSat class of satellites are frequently used by universities due to the lowered build and launch costs [14]. The MWPT system will be installed on a 1U satellite. The 1U satellite is a constrained payload so that it would be economically feasible for Universities to send payloads to space. The constraints that a 1U platform provides are a total mass of 1.33 kg and a maximum outer dimensions of 10 cm x 10 cm x 10 cm.

The system was designed as if it is incorporating a Clyde Space CubeSat Standalone battery [15]. The output voltage of the battery should be 9V to ensure a voltage over the 8.2V end of charge voltage benchmark of the Clyde Space battery so the system could successfully charge the battery [16]. The Clyde Space battery has numerous conditions for charging and discharging current rates, but a maximum charge current of 1.875A is recommended [16]. Designing a separate DC to DC converter is a little impractical in the design of the system since

the Clyde Space CubeSat Standalone battery can come equipped with a DC to DC converter and does not need to be designed from scratch [16]. The converter incorporated with the Clyde Space battery would be space qualified, unlike the circuit that will be described later. However, obtaining one of these batteries and converters for the purpose of testing is impractical due to the high cost of the battery [15]. This testing is also the first known case in which a DC converter would be incorporated in a MWPT system, making the risk of damage to the expensive DC converter and battery module an unnecessary risk. Since obtaining a Clyde battery would not be possible, a DC to DC converter will be designed and tested with a load to simulate the characteristics of the Clyde battery. The load will be implemented using a fixed resistor load during the testing of the system.

Future calculations and simulations will need to be done on the thermal properties of space and the components in space temperatures. Parts will be chosen to be operational from at least -55oC to 125oC. This temperature range should give the best results for the anticipated harsh environment of space. The temperature range also coincides with the automotive grading of the AECQ-200 standards for parts, making parts for this temperature range widely available and at a reduced cost compared to custom parts.

II. SYSTEM DESIGN

The system design will consider application and design constrains already set in place. The complete system is divided into 4 subsystems; antenna design, rectifier design, rectenna array design, and the DC to DC converter. This research work will only cover the rectifier and DC to DC converter designs. The rectifier design will be comprised of three separate pieces. The rectifier will include a Harmonic Rejection Filter (HRF), rectifying diode(s), and a DC bypass filter. The block diagram of the whole system can be seen in Figure 7. The rectenna array design can be viewed in Figure 6. The following sections will describe each block of Figure 7 in more detail.

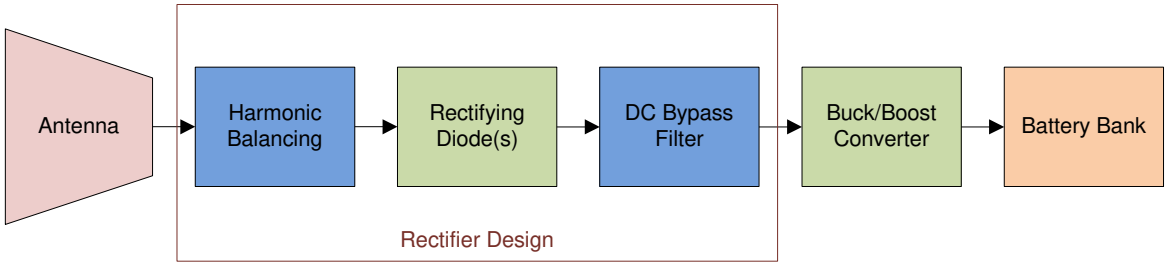

Figure 7: Block diagram of the MWPT system

a. Antenna Design

The design of the antenna used in this design was completed by another member of the research team, a colleague at the University of North Dakota. The results of the antenna are important to note since all of the pieces of the MWPT system need to be designed to match each other. The antenna was designed to match a 100Ω transmission line. The reasoning for matching to the 100Ω will be described in Chapter "III". The antenna design is not a part of this thesis work.

b. Rectifier Design

As stated, part of this research work is focused on the rectifier design component of the MWPT system. The general design process for the RF rectifier system, was based on the process laid out in [2]. The RF rectifier design process is as follows:

1. Select a Schottky diode
2. Decide on a Schottky diode configuration
3. Design the transmission lines, HRF and load to match the impedance of the chosen diode
4. Tune out the reactance of the impedance of the chosen diode
5. Select a DC bypass capacitor

Design steps are explained in the following subsections.

i. Diode Selection

The primary device in RF rectifiers is the Schottky diode [2, 4, 5, 7, 10, 17, 18]. The Schottky diode is used due to its low forward voltage and the reduced amount of time it takes the diode to start and stop conducting. Both of these properties leads to improved efficiency. The aforementioned properties are due to the physics of the materials that make up the diodes. The Schottky diode consists of a metal contact and an N-doped silicon substrate as seen in Figure 8. In Schottky diodes P-doped silicon does not exist, despite most other diodes [19]. The lack of P-doped silicon means that there are no minority carrier build-ups; the diode stops conducting as soon as voltage is in reversed biased [5, 20]. The lack of a minority carrier and the presence of a majority carrier junction means that there is a lower barrier voltage, which allows some Schottky

diodes to begin conducting at about 0.3 Volts in comparison to a standard diode conducting at 0.7 Volts. The turn on voltage is the minimum voltage potential across the diode in which the diode will become forward biased and begins to conduct [19]. This reduced turn-on voltage is quite important to the rectifier efficiency since rectifiers are normally dealing with low input voltages. The higher the turn-on voltage, the less power rectified and the more power consumed by the diode. All of the above properties make Schottky diodes a suitable and a common choice in rectifiers operating at high frequencies such as 5.8GHz.

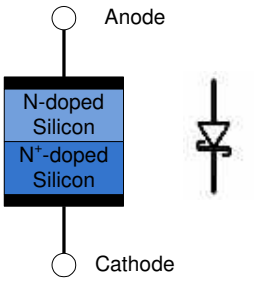

Figure 8: Internal material and symbolic view of a Schottky diode.

An added design challenge when using or considering Schottky diodes is their nonlinear properties. Schottky diodes are nonlinear due to the way they are designed. The interaction between the insulator and the internal metal wires of the diode causes the nonlinearity [5]. A description of how a nonlinear device works is presented by Boaventura [5] "when fed with an RF input signal, the nonlinear device produces several spectral components at the output: DC, fundamental frequency, harmonics of the fundamental, and intermodulation mixing products (if the input signal is modulated)." A nonlinear device has been proven to be quite effective and efficient in rectification for applications of MWPT as described in [2, 4, 17].

Schottky Diode Selection

When searching for a diode, it is important to keep in mind that there are no "ideal diodes" on the market, unlike in most of the analysis done in simple circuit theory. There were two types of diodes incorporated into the design analysis process of the rectifier in this work. The BAT17 and MA4E1317 diodes were chosen. The BAT17 was initially chosen due to the low turn on voltage of ≈ 0.3V. However, the BAT17 is limited by a breakdown voltage of 4V. Upon a deeper investigation of the part it was also noted that the part was recommended for use in mixer applications in the Very High Frequency (VHF) and Ultra High Frequency (UHF) [21] circuits. VHF frequency band is defined from 30 MHz to 300 MHz and UHF frequency band is defined as 300 MHz to 3 GHz. Neither of which are overlapping the SHF operating range. The BAT17 is recommended for use in the lower bands due to its relatively large junction capacitance of 0.55pF [21]. In comparison, the MA4E1317 has a maximum operating frequency of 80 GHz and a much lower junction capacitance of 0.02pF. Junction capacitance is the parasitic capacitance that negatively impacts the operating frequency of diodes. While exploring the potential efficiency and preforming impedance calculations of the BAT17; the MA4E1317 was used as a control to compare the results and compare the results to previous works, since it had been used in [10, 17, 18]. A selection between the two diodes was made that will be explained in Chapter "III". The calculations preformed to determine the impedance of a diode are as follows [2, 4].

$$Z_D = \frac{\pi R_s}{D + jE} \tag{1}$$

where,

$$D = \cos\theta_{on}\left(\frac{\theta_{on}}{cos\theta_{on}} - sin\theta_{on}\right) \tag{2}$$

$$\text{E}= \omega R_s(C_j\sqrt{\frac{V_{bi}}{V_{bi}+V_D}})(\frac{\pi-\theta_{on}}{cos\theta_{on}} + sin\theta_{on}) \quad (3)$$

and θ_{on} is found by solving equation (4)

$$tan\theta_{on} - \theta_{on} = \frac{\pi R_s}{R_L(1+\frac{V_{bi}}{V_D})}. \quad (4)$$

The junction capacitance C_j in (3) is defined as

$$C_j = C_{jo}\sqrt{\frac{V_{bi}}{V_{bi}+|V_D|}}. \quad (5)$$

The variables and parameters used in the diode calculation can be seen in Table 1 along with a description of each variable. The datasheet of Schottky diodes provide these parameter definitions as: R_s is the diode series resistance; C_{jo} is the zero-bias junction capacitance; V_{bi} is the built-in turn on voltage; V_D is set at the operating voltage and is also called the voltage across the diode, which should be ½ of the breakdown voltage (V_{br}) [4, 17]. The maximum of V_D should be about ½ of V_{br} so that the diode will not be put into an avalanche breakdown mode. Derating of the V_D, diode voltage, is also a good idea if the part being used has a wide tolerance between the minimum and typical V_{br}. However, the efficiency of the diode will increase as the rectifier increases V_D closer to V_{br}. It should be noted the closer the diode is operated to V_{br}, the more likely the diode will be saturated and burned out. The load resistance R_L is the projected load of the system. The θ_{on} variable is the forward-bias turn-on angle of the Schottky diode [4, 17]. The forward-bias turn-on angle must be calculated using equation (4). θ_{on} can be viewed in relation to other independent variables of the diode and the rectification signal in Figure 9.

Variable	Description
Z_D	Complex impedance of the diode
R_s	Series resistance of the diode
θ_{on}	Forward-bias turn-on angle of the Schottky diode
C_j	Junction capacitance
V_{bi}	Built-in turn on voltage (forward voltage)
V_D	Voltage across the diode (operating voltage)
R_L	Load resistance
C_{jo}	Zero-bias junction capacitance
V_{br}	Breakdown voltage

Table 1: Quick reference description of the variables used to calculate the diode impedance.

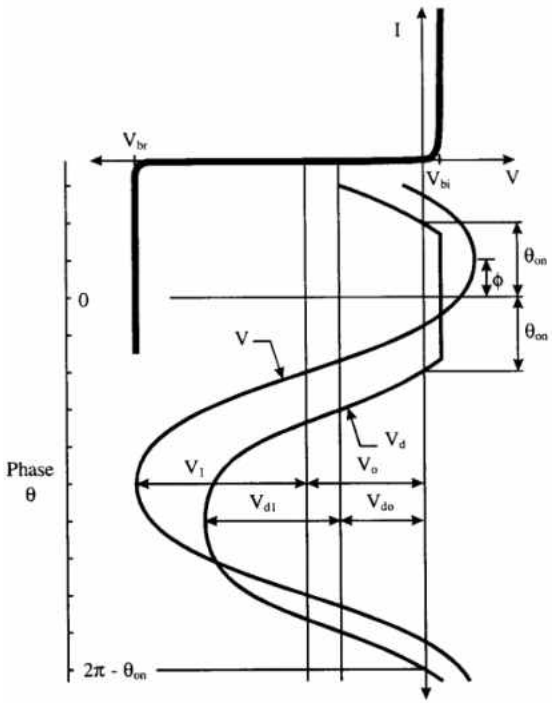

Figure 9: The rectification cycle of the shunt diode is represented by the input fundamental and overlaid on the diode Current-Voltage curve. This model assumes that there are no losses due to the harmonics and $\theta = \omega t - \varphi$ [4].

The diode efficiency is also used to assist in comparing diodes. The calculated efficiency for a can be found by [4, 17]

$$\eta_d = \frac{1}{1+A+B+C} \tag{6}$$

where,

$$A = \frac{R_L}{\pi R_s}\left(1+\frac{V_{bi}}{V_D}\right)^2\left[\theta_{on}\left(1+\frac{1}{2\,(\cos\theta_{on})^2}\right)-\frac{3}{2}\tan\theta_{on}\right] \tag{7}$$

$$B = \frac{R_s R_L {C_j}^2 \omega^2}{2\pi}\left(1+\frac{V_{bi}}{V_D}\right)\left(\frac{\pi-\theta_{on}}{(\cos\theta_{on})^2}+\tan\theta_{on}\right) \tag{8}$$

and

$$C = \frac{R_L}{\pi R_s}\left(1+\frac{V_{bi}}{V_D}\right)\frac{V_{bi}}{V_D}(\tan\theta_{on}-\theta_{on}). \tag{9}$$

The diode efficiency calculations do not include the effects of the harmonics created by the non-linear operation of the Schottky diode. If the harmonics effects were accounted for in the calculations, the diode efficiency would be higher than the values calculated using the equations (6-9). Many of the parameters and variables used in the diode efficiency calculation are the same as in the diode impedance. All variables used in the diode efficiency calculation are listed with a description in Table 2. The efficiency of the Schottky diodes will approach 100% if the junction voltage (V_j) (forward voltage drop) of the diodes is much lower than the breakdown voltage (V_{br}) [3]. For example, a V_j of 0.8V is much lower than a V_{br} of 60V. Also, the lower the C_j, the lower the breakdown voltage. Typically, as the C_j decreases, R_s increases [3]. While an increase in C_j reduces the diode efficiency. Also as C_j decreases, the speed at which the diode can switch between conducting and not conducting increases [3]. Since a highly efficient design requires V_{br} to be high, and a diode that can conduct as fast as possible, a compromise needs to be made

between the diode characteristics while selecting a diode. If the power input across the diode increases above saturation, the diodes will burn out and stop working.

Variable	Description
η_d	Efficiency of the diode, excluding effects of harmonics of the diode
R_L	Load resistance
R_s	Series resistance of the diode
V_{bi}	Built-in turn on voltage (forward voltage)
V_D	Voltage across the diode (operating voltage)
θ_{on}	Forward-bias turn-on angle of the Schottky diode
C_j	Junction capacitance
ω	Operating frequency

Table 2: Quick reference description of the variables used to calculate the diode efficiency.

Rectifier Topology

The two most prominent configurations of a rectifier are a single shunt diode and a Dual diode configuration, as seen in Figure 10. While operating at 5.8GHz, a single shunt diode configuration can achieve the highest overall efficiency (up to 82% [2, 4, 17]). Previous works have achieved efficiency higher than 80% in the power range from 50mW-130mW for a single element test [4, 17]. A single element is the composition of a pair of antennas, HRF, rectifying diode(s) and a DC bypass capacitor, as seen in Figure 10. In Figure 10, the section labeled BPF is the HRF. The rectifying diodes in Figure 10 are at the location shown by the exploded bubble of the "Dual Diodes". The DC bypass capacitor is in the middle of the CPS section and the symbol for the capacitor is shown by the legend on the right side of the image. The critical flaw of the single shunt diode is that the voltage output is low. Higher output voltages are important for all applications that require more than microwatts of power. For this application, the increased voltage is important so that less energy is wasted in order for the output voltage regulation to be closer to the battery or load voltage requirements. The increased voltage of the single element

will lower the efficiency when compared to a single shunt diode topology [10]. However, the dual diodes will allow for an increased efficiency when interconnecting array elements. The importance of the voltage per rectenna will be discussed further in Section "c" of this Chapter. The voltages of the single shunt diode and the dual diode are compared in Figure 11 based on the results of [10]. However, the dual diode configuration has achieved a maximum RF to DC conversion efficiency of only 76% [10].

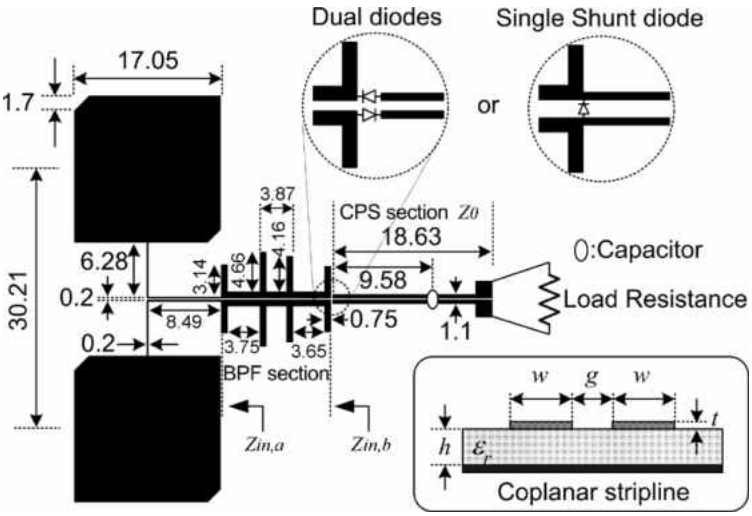

Figure 10: Layout of the previous dual-diode rectenna design, single shunt diode rectenna, and CPS. All dimensions are in millimeters [10].

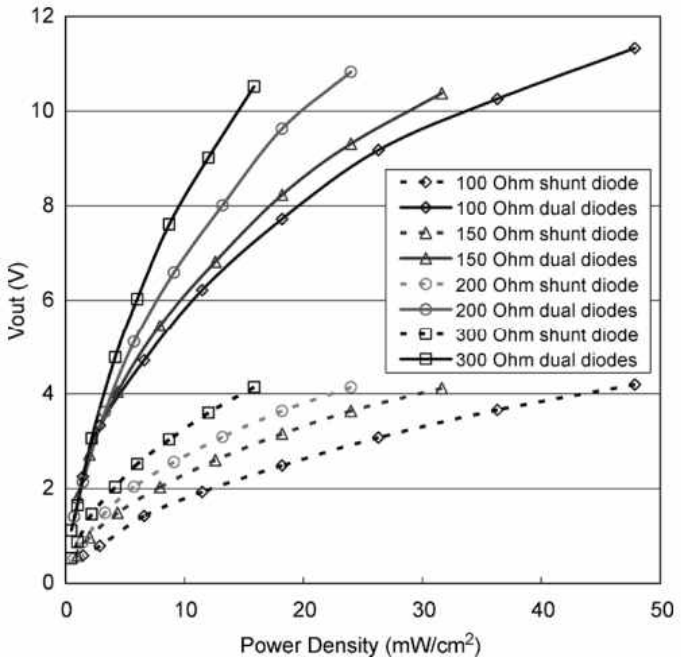

Figure 11: Measured DC output voltages of the dual-diode and single shunt diode rectennas [10].

The diode efficiency of dual diodes can be obtained for the BAT17 and the MA4E1317 by the substitution stated by Ren in [10]. The substitution replaces R_L and R_s in equations (7) - (9) of this work. To approximate the dual diode efficiency, substitute all instances of R_L in equations (7) - (9) with $(R_L + R_D)$ [10]. R_D is the diode resistance or the real portion of Z_D found in (1). Then all instances of R_s in equations (7) - (9) should be substituted by $(R_s + R_L)$ [10]. As a result of this substitution. Equations (7) - (9) will be changed to:

$$A = \frac{(R_L+R_D)}{\pi(R_s+R_L)}\left(1+\frac{V_{bi}}{V_D}\right)^2\left[\theta_{on}\left(1+\frac{1}{2\,(\cos\theta_{on})^2}\right)-\frac{3}{2}\tan\theta_{on}\right] \qquad (10)$$

$$B = \frac{(R_s+R_L)(R_L+R_D){C_j}^2\omega^2}{2\pi}\left(1+\frac{V_{bi}}{V_D}\right)\left(\frac{\pi-\theta_{on}}{(\cos\theta_{on})^2}+\tan\theta_{on}\right) \qquad (11)$$

and

$$C = \frac{(R_L+R_D)}{\pi(R_s+R_L)}\left(1+\frac{V_{bi}}{V_D}\right)\frac{V_{bi}}{V_D}(\tan\theta_{on} - \theta_{on}). \quad (12)$$

The most significant advantage of the dual diode configuration is that it will have two to three times the voltage of the single shunt diode configuration, as seen in Figure 11 [10]. Figure 3 shows the rectenna layout for a single diode configuration. If a dual diode were to be chosen, it would look like the dual diode balloon in the top center of the image seen in Figure 10. The dual diodes used in [10] was a brand-new idea and topology design in research [10]. Previous designs have used multiple diodes in their rectification process [11, 22, 23]. Previous designs using multiple diodes are more closely related to charge pumps, as seen in Figure 4 (b) [11]. Charge pumps are typically used for much lower power devices such as RFID tags and produce only microwatts of power [11]. All of the filtering blocks in Figure 3 allow more RF power to be retained and converted into DC.

ii. Diode Matching to Coplanar Strips

One of the most important factors in the rectifier design, is ensuring the transmission lines are matched properly to the impedance characteristics of the chosen diode. If the transmission lines are not matched properly, there will be a loss in efficiency. The impedance of the Schottky diode needs to be first calculated by using calculations in equations (1) - (4). Once the impedance calculation is completed, a graph of the diode impedance versus the load resistance can be created. The Diode impedance should match to the circuit should be made with the real impedance and not the complex portion of the impedance [2]. The complex impedance should be matched to the antenna's complex impedance so that it is tuned out and the power can be transmitted as efficiently as possible. If the antenna, HRF and diodes are not matched

impedances, the efficiency of the system will suffer. The use for the complex portion of the diode impedance will be discussed later in this Section under Sub-section “iv”. The efficiency calculations using equations (6) - (9) are used to find the efficiency of the Schottky diode. To choose an impedance for matching the coplanar strips to the diode, both the impedance and efficiency graphs should be consulted. The matched impedance should allow the diode to operate near the highest possible diode efficiency. However, choosing high load impedance will result in a low output current. A compromise between output current and the efficiency needs to be made. This is to maximize the power transfer of the system to achieve greater power transfer efficiency.

iii. Harmonic Rejection Filter

The HRF prevents the reradiating of RF energy at frequencies other than the center frequency. The filter does this by allowing the 5.8GHz signal received by the antennas to pass, but will not allow the various harmonic frequencies 2*f*, 3*f*, 4*f*, etc. (where *f* is the fundamental frequency) to be returned to the antenna. The harmonic frequencies are created by the nonlinear operation of the Schottky diode.

There are several types of filters that could be used to achieve these results. First is a High Pass Filter (HPF) which allows only high frequency signals to pass through. Second is a Low Pass Filter (LPF) which allows only low frequency signals to pass through. Next is a Band Pass Filter (BPF) which is a combination of a HPF and a LPF so that only a specific band of frequencies is allowed to pass through the filter. Next is a Band Stop Filter (BSF) which is a combination of a HPF and a LPF so that only a specific band of frequencies is prevented from passing through the filter.

The HRF in this work can represented as a combination of a Band Stop Filter (BSF) and a Band Pass Filter (BPF), since the center frequency of 5.8GHz is allowed to pass and the 2nd and 3rd harmonics are rejected. This work could have also been completed by using a low pass filter. The type of filter is intended to be a maximally flat filter so that the frequencies between the areas of interest have a nearly constant amplitude attenuation. The initial filter design chosen was based on the filter used in [10], which can be seen noted by the "BPF" in Figure 10.

The rectenna filter in [10] was used in this work as an initial starting point due to simplistic design and ease of optimization using the software package from Computer Simulation Technology (CST) [12]. It is important that the impedance of the HRF to be matched to the real impedance of the diode(s) to maximize the rectification efficiency [2]. The design and layout of the rectifier circuit can be seen in Figure 12. The label "La" and the items below and to the right are the optimized filter and rectifier. "La" is the length "a" of the first coplanar strip (CPS). A CPS is two parallel transmission lines separated by an air gap and a dielectric constant between the lines and a ground plane. The thin blue lines in Figure 12 are representations of the electrical connections between the blocks. The "T" looking block is a junction that allows the filter stub, "L1" to be connected to the CPSs on either side of the "T". The design continues like this until it reaches the SPICE representations of the diodes. Since the design is symmetrical between the top and bottom halves of the filter and rectifier, "La" does not need the Prime of "La" below the strip of "La". Inside the simulation, CST accounts for the dielectric constant, width length and height of each transmission line, along with the gap between the transmission lines and the ground plane. The SPICE Models for the diodes are based on the parameters found in the diode datasheet and then entered into a text file and uploaded to CST through a SPICE model. Once the

filter design from [10] was imported to CST it was optimized to meet the author's specific goals for the filter seen in goals 0 through 7, as seen in Table 3. The design parameters for Figure 12 are located in Appendix G. The impedance line diagram of Figure 12 is also located in Appendix G.

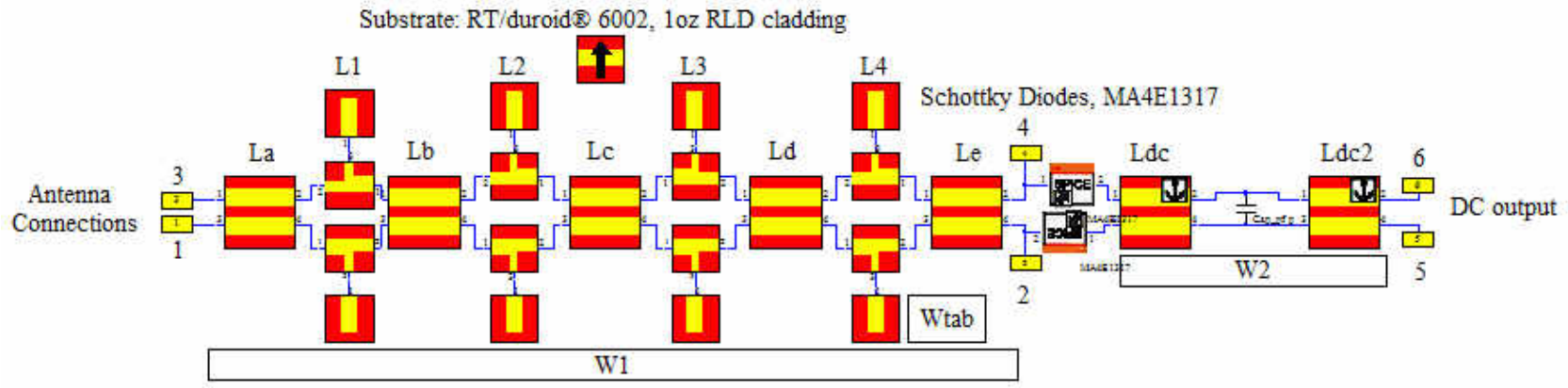

Figure 12: Layout of Harmonic Rejection Filter (HRF) with Dual Diode design. The red and yellow blocks are representations of CPS. The spice blocks to the right of the Ports "2" and "4" are links to spice file representations of the diode MA4E1317 [12].

Description	Operator	Target	Frequency (GHz)	Weight of Goal
S_{11}	Min	0	5.8	1
S_{33}	Min	0	5.8	1
S_{12}	Max	1	5.8	1
S_{34}	Max	1	5.8	1
S_{12}	Min	0	11.6	1
S_{34}	Min	0	11.6	1
S_{12}	Min	0	17.4	1
S_{34}	Min	0	17.4	1

Table 3: Goals for optimization of harmonic rejection filter.

In Table 3, a target value of 0 represents that the signal at the specified frequency will not be allowed to pass, a target value of 1 represents that the signal at the specified frequency will be allowed to pass. In Figure 12, each yellow box represents a port. S_{ij} is the S parameter between ports i and j.

iv. DC Bypass Capacitor

The DC bypass filter acts as a short for the high frequency harmonics and allows the DC power to pass onto the load. The complex portion of the diode impedance will be tuned out by the reactive size of the bypass capacitor [2]. The distance between diode and the bypass capacitor, d_{dc}, can be viewed in Figure 3. The length d_{dc} is decided through experimentation, as shown by previous researchers [17, 18]. If a dual diode topology is chosen, then the complex impedance of the two diodes can be assumed to be canceled out since the diodes will not be acting like the single shunt diode [10]. The size of the capacitor is a difficult choice. The capacitor should be large enough to remove the ripple from the rectifying process, but small enough so that the capacitor can fully recharge to the input voltage so that no voltage is dropped across the

capacitor. Ripple, or voltage ripple is unwanted radiation of an AC signal or noise on an output intended to be a DC output signal.

v. Half-wave Versus Full-wave Rectifying

The consideration for using a half-wave rectifier versus a full-wave rectifier was determined on two terms. First reason is the reduction of parts and thus a reduction in building cost [5]. Second reason is that the difference between conversion efficiency of half- and full-wave rectifiers at SHF (5.8GHz) is extremely small based on the comments of [5, 6]. The largest benefit that a full-wave rectifier has over a half-wave rectifier is that the full-wave rectifier can divide the input power across more diodes than a half-wave rectifier. When the power is divided in the full-wave rectifier the rectifier can operate at higher power levels before the diodes reach their breakdown ratings [6]. With a full wave rectifier, there will also be a smaller output voltage ripple on the end of the rectenna. However, the full-wave rectifier requires a higher operating voltage range due to the increased number of diodes. The full-wave rectifier system power conversion efficiency at lower input power levels will be much lower when compared to a half-wave rectifier due to the voltage drop across the extra diodes. Meaning the small signal conversion of a full wave rectifier is potentially worse or marginally better than the half-wave rectifier when efficiency is the most important factor in compare to smooth DC voltage.

c. Rectenna Array Design

The goal in designing the rectenna array is to capture and convert the most power possible for the given area. The area will be constrained by the size of the satellite. In this case the spacecraft will be 10cm × 10cm × 10cm. The size of the array will be 30cm × 30cm built of

nine separate 10cm × 10cm panels arranged in a 3×3 panel square, similar to Figure 13. The array will need to balance the spacing of the rectenna elements close enough to fit as many rectennas on the array surface as possible, but also far enough away from each other so each element can absorb the optimal amount of energy.

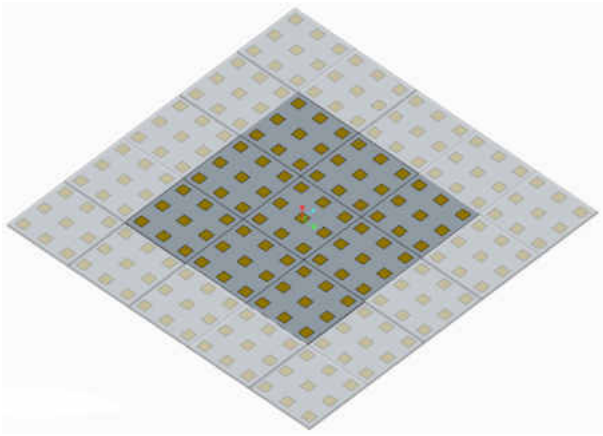

Figure 13: Image of the receiving satellite with a 4x4 panel area or a 3x3 panel area [1] [12].

Like any other portion of the RF to DC conversion process, the design of the rectenna array can make or break the efficiency of the system. The rectenna array can be made more or less efficient by how elements are inter-connected. An element consists of two antennas and the rectifier, as seen in the dashed boxed in Figure 14 (A). There are two basic ways to connect elements into an array, series and parallel as seen in Figure 14 (B) and (C) [10, 24]. A third method, cascaded, can be implemented by using series and parallel to connect elements into an array, as seen in Figure 14 [10]. In [10] results were published on all three interconnection methods using the dual diodes seen in Figure 10 instead of the shunt diode method shown in Figure 14. The experiment results described in [10] discovered that the cascaded array produced a greater voltage and had a better efficiency than any other connection method. In [10, 24] the efficiency of array elements in series and parallel connections were studied, and found that elements

connected in parallel produced more power than those elements connected in series. It was also noted that elements in an array generally produce equal or less power than the sum of the power generated by the elements individually [24]. The ability to have fewer rectennas in series will increase the overall system efficiency. This is because it has been shown that rectennas cascaded in parallel are more efficient than their counter parts connected in series [10, 24].

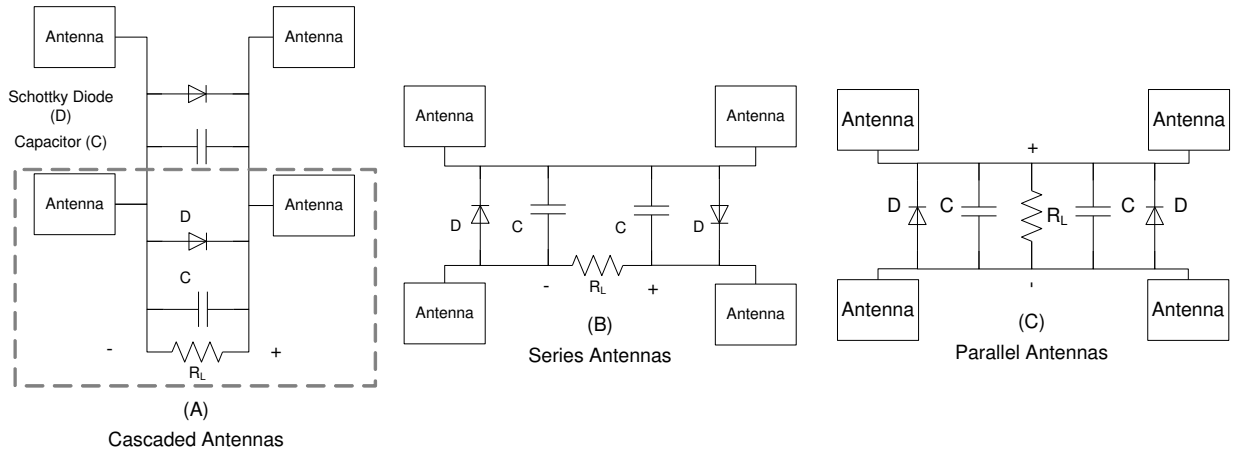

Figure 14: (A) Cascaded Antennas, (B) Series Antennas, and (B) Parallel antennas

d. DC-to-DC Converter

The DC-to-DC converter is a transition between the rectenna arrays and the batteries onboard the satellite, as seen in Figure 16. The purpose of the DC-to-DC converter is to regulate the energy gathered from the rectenna array and use it to charge a battery bank. The type of DC-to-DC converter chosen for this work will be a buck/boost converter. A buck/boost converter is a combination of a buck converter and a boost converter. The buck converter can regulate input voltages at or above a desired output voltage, thus reducing or bucking the input voltage. A boost converter can regulate input voltages at or below a desired output voltage, thus increasing or boosting the voltage. The combination of a buck and boost converter into a single design is highly

advantageous for an application with a large input voltage range. The buck/boost converter was also chosen since the designs are familiar to the author from previous projects that have been completed.

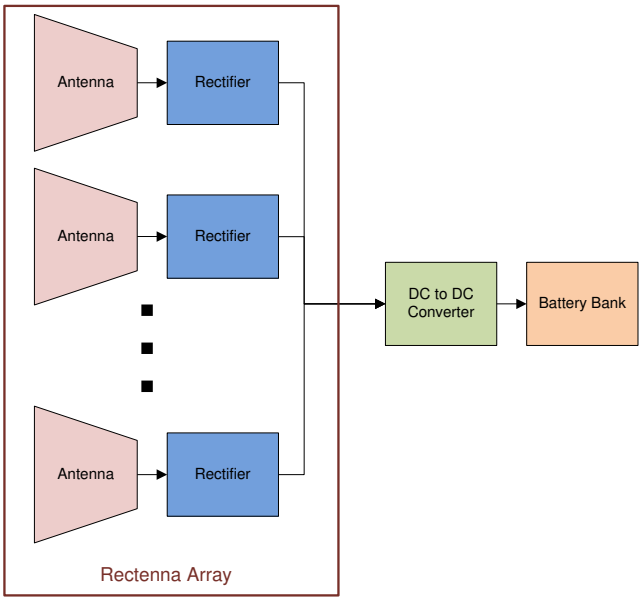

Figure 15: Block diagram showing the position of the DC-to-DC converter.

The most important reasons for having a DC-to-DC converter is to regulate the input voltage and protect the batteries, improve the system design for use on multiple spacecraft, and assist the rectenna array to be designed for the greatest power reception.

The DC-to-DC converter will allow the battery to be charged while the satellite is not in the optimal power density. This will protect the batteries from being over and under charged. This will be a result of the buck/boost converter's ability to increase the voltage received high enough to charge a battery or decrease the voltage received so the battery does not over charge. In a more advanced design, the buck/boost converter could be replaced by a charge controller. The converter will maximize the amount of energy that can be stored in the batteries when the

satellite is coming into and out of the primary RF beam by allowing the battery to begin charging at lower input powers. This ability will allow the batteries to be charged effectively for a longer amount of time.

The properties of the converter will also allow the rectenna array to be used on multiple receiving satellites that receive different power densities. The multiple power densities may happen due to different orbiting elevations and relative closeness to the transmitting spacecraft.

If a DC-to-DC converter was not used in the design, and the same rectenna array design was used on two satellites, which received different power densities, the array would produce different output voltages and would have different efficiencies. Without a DC-to-DC converter and by using the same rectenna array for multiple power densities, the system could produce a voltage, which could damage the battery bank or other circuitry in the system. On the contrary, the satellite may produce a low voltage situation, in which the system may not maintain its operation as expected or it may never turn on.

To show how a converter would assist in the optimal rectenna array design an example is given:

Presume that the transmitting power beam cannot be changed, and the rectenna array was designed without a DC-to-DC converter to produce an output of 8 volts to charge a battery bank and the power irradiance of the array is 10mW/cm^2. The 10mW/cm^2 is chosen because it is located near the midpoint of the 0.1-20mW/cm^2 expected operating range of the receiving satellite being designed. Also, presume that the number of rectenna elements in an array is fixed at eight elements, for ease of calculation. Based on the results from [10] and those shown in

Figure 11 a single shunt diode could produce about 2V [10]. This would require the array to have a sub-array of two cascaded elements and four sub-arrays in series to produce the required voltage for a charging, 8V. If the satellite shifted position and the power irradiance increased to 20mW/cm^2, the output voltage could then be 12V. The four extra volts above the charging voltage could cause damage or diminish the lifespan of the battery bank.

If a DC-to-DC converter is added to the example system design, then the dual diode array can have all eight elements cascaded because the DC-to-DC converter would maintain the battery charging voltage at 8V even if the input fluctuates, based on the results from Figure 11 [10]. However, for the single shunt diode array example, there could be four elements cascaded into a sub-array and two sub-arrays could be connected in parallel to increase the efficiency of the rectenna array over adding elements in series. The reduction of antennas in series is important because studies have shown that more power can be produced in an array if elements are cascaded or are in parallel compared to elements being tied in series [5, 10, 24]. The new design would also include all of the other mentioned benefits of a DC-to-DC converter.

The downsides of adding a DC-to-DC converter are the additional losses in system efficiency and an increase in system cost and complexity. The advantages of a converter are an expanded operating voltage range for operation of a load or battery charging, an increase in array efficiency achieved by more cascaded and parallel rectennas, a common design can be used on multiple receiving satellites without needing an array redesign. It is important to note that every DC-to-DC converter is different and has different efficiency curves. However, DC-to-DC converters easily achieve efficiencies above 85% [25, 26].

The design criteria for selecting and designing the DC-to-DC converter are:

1. Buck/boost converter
2. Acceptable range of Vin, ~ $4V<V_{in}<30V$
3. $V_{out} = 9V$
4. Maximum $I_{out} \geq 2A$

i. Converter Design analysis

Much of the design analysis for the converter can be found in the datasheets [27] or application notes [28] produced by DC-to-DC converter manufacturers. Beyond the calculations found in the converter datasheet, the two most important parameters for the converter is the tolerances of the resistors to ensure that a resistor does not cause the output of the converter to be changed; and the maximum power consumed by each resistor.

When using resistors in any design it is importance to check that their variance in manufacturing will not impact the design. The easiest way to show the variance is to look the feedback resistor divider used by most converters to set the output voltage of the DC converter. This is done by checking the minimum and maximum voltage output based on the divider network. The following equations assume that the divider network looks like Figure 16.

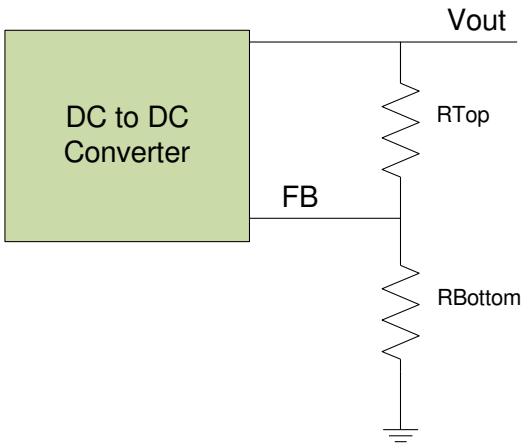

Figure 16: DC converter feedback resistor divider network.

The starting equation for the resistor divider is as follows,

$$V_{FB\_desired} = V_{out} \frac{R_{Bottom}}{R_{Top}+R_{Bottom}}. \quad (13)$$

Solving equation (13) for R_{Bottom} creates the following equation,

$$R_{Bottom} = \left(\frac{V_{out}}{V_{FB\_desired}} - 1\right) * R_{Top}. \quad (14)$$

$V_{FB\_desired}$ is the nominal voltage on net FB in Figure 16 in which the converter will attempt to maintain in order to regulate the output voltage (V_{out}). Equation (14) assumes that the value V_{out} has been specified by the application description, along with the value of $V_{FB\_desired}$ which should be specified in the DC converter datasheet or application note. Since the value of the two resistors are still unknown, a second equation, equation (15), will be used to substitute into equation (14) in order to find the resistor values. Since the converter is attempting to achieve the highest possible efficiency, the sum of R_{Top} and R_{Bottom} should be very high. It is recommended that the sum of the two resistors meet exceed 1 MΩ, as:

$$R_{Top} + R_{Bottom} >= 1M\Omega. \quad (15)$$

Now that the values of the resistors are known, the Resistor tolerance needs to be specified and the minimum and maximum resistance for both resistors need to be calculated as seen by the following equations for the resistor minimum and maximum,

$$R_{XXXX\_min} = R_{XXXX}\left(1 - \frac{Tol_R}{100}\right) \tag{16}$$

and

$$R_{XXXX\_max} = R_{XXXX}\left(1 + \frac{Tol_R}{100}\right). \tag{17}$$

The new minimum and maximum output voltage is checked to ensure that the resistor tolerances will not impact the output voltage significantly, as seen in the following two equations

$$V_{out\_max} = V_{FB\_desired}\frac{R_{Top\_max} + R_{Bottom\_min}}{R_{Bottom\_min}} \tag{18}$$

and

$$V_{out\_min} = V_{FB\_desired}\frac{R_{Top\_min} + R_{Bottom\_max}}{R_{Bottom\_max}}. \tag{19}$$

The power requirements can now be checked for the two resistors using $P_R = \frac{V^2}{R}$. The following equations are implemented in the divider network shown in Figure 16,

$$P_{R\_Bottom} = \frac{\left(\frac{V_{\max\_out} * R_{Top\_min}}{R_{Bottom\_max} + R_{Top\_min}}\right)^2}{R_{Bottom\_max}} \tag{20}$$

$$P_{R\_Top} = \frac{\left(\frac{V_{\max\_out} * R_{Bottom\_min}}{R_{Top\_max} + R_{Bottom\_min}}\right)^2}{R_{Top\_max}}. \tag{21}$$

In equations (20) - (21) the value of $V_{\max\_out}$ is not the same value of V_{out_max} calculated in (18). The value $V_{\max\_out}$ is the specified maximum voltage the load of the converter will possibly see. $V_{\max\_out}$ should be about 5-10% higher than the typical value of V_{out}. The following check should be completed and passed,

$$V_{out\_max} < V_{\max\_out} \tag{22}$$

The minimum value of the inductance and the output ripple current calculations were obtained from the application note by Green [28]. The minimum inductance value is a crucial step in designing a monolithic buck/boost converter. The minimum inductance needed is first determined by calculating the minimum inductances for the buck mode and boost mode with

$$L_{Min\_Buck} > \frac{V_{out}*(V_{in\_max}-V_{out})}{K_{ind}*F_{sw}*V_{in\_max}*I_{out}} \tag{23}$$

and,

$$L_{Min\_Boost} > \frac{{V_{in\_min}}^2*(V_{out}-V_{in\_min})}{K_{ind}*F_{sw}*I_{out}*{V_{out}}^2}. \tag{24}$$

The maximum inductance between L_{Min_Buck} and L_{Min_Boost} is then chosen as the converter's overall minimum inductance (L_{Min}), as seen by

$$L_{Min} = max[L_{Min\_Boost}, L_{Min\_Boost}]. \tag{25}$$

The following are an explanation of the parameters used in (23) and (24). V_{out} is the typical output value of the converter. V_{in_max} is the maximum possible input voltage that the converter could anticipate. K_{ind} is a constant to reflect the output current ripple. This value can

be approximated to be between 0.2 and 0.4 ($20\% < K_{ind} < 40\%$). F_{sw} represents the chosen switching frequency. I_{out} is the anticipated load current of the converter. V_{in_min} is the minimum input voltage in which the converter will operate.

e. Substrate and PCB Materials

Substrate and Printed Circuit Board (PCB) are two similar terms used in the RF community and industrial and commercial electronics industries, respectively, and therefore, mean the same in this document.

i. Rectifier Substrate Material

The material Rogers RT/duroid® 6002 has been chosen for this work due to its low outgassing properties. The outgassing properties are important to reduce the probability that harmful vapors will be released and condense on the inner surfaces of the satellite [29]. One ounce copper cladding of the material was chosen for better heat dissipation properties. The antenna part of the rectenna will absorb more RF energy as the copper thickness increases. The substrate has a 0.06 inch (1.524 mm) thickness and two layers of copper.

ii. Buck/Boost Converter PCB Material

Thinner materials may be easier to work with for better heat dissipation characteristics and placing electrical pathways (vias) between the layers of copper. Additional heat dissipation can be achieved by increasing the thickness of the copper on the layers of the PCB. Standard copper thicknesses are typically 0.5 oz. /sqft (1/2 oz.) and 1 oz. /sqft (1 oz.). Specialty thickness of copper can range up to 20 oz. /sqft, usually in 1oz increments, depending on the insulation

material type [30]. Having more layers of copper would only be necessary as the circuitry complexity increases, which would require more traces between components.

III. PROTOTYPE DESIGN

a. Rectenna Design

The rectenna design was simulated using the CST software. The substrate that the rectenna was simulated on was the Rogers RT/duroid® 6002 material described in Chapter "II". The simulated rectifier for the rectenna can be viewed in Figure 12. The Antenna and rectifier were designed and optimized separately. Once achieving quality results for both, they were combined and then re-optimized to ensure the antenna and the HRF are properly tuned to 5.8GHz. The rectenna was also optimized for antenna spacing. As noted in Chapter "II", another member of the research team designed the antenna portion of the rectenna system.

The rectifier was optimized separately from the antenna by using the specifications shown in Table 3. Figure 17 shows a copy of the design in Figure 12. The function of each transmission line stub of the HRF was determined by removing one stub at a time to see what changed in the S-parameter results. The stubs can be seen as (L1) - (L4) in Figure 17. The first stub (L1) was used to match the Impedance of the HRF to the transmission lines of the antenna. The second stub (L2) prevents 17.4GHz from reflecting back to the antenna. The third stub (L3) assists the fourth stub (L4) in preventing 11.6GHz from reflecting back to the antenna. Stubs two through four all allow the 5.8GHz signal to pass. Without the stubs two through four, 5.8GHz signals would be blocked by the filter. Through trial and error, it was discovered that an additional goal was needed in Table 3 to achieve a DC output value at S_{56}. The additional goal to achieve the desired

output is to find the point at which S_{56} has a minimum value with a target of “0” at the frequency of “0” and the weight of “1”. This final weight can be higher since the desired output at S5 and S6 in Figure 12 should have no DC component between them. S5 is the yellow box on the right side of Figure 12 with “5” inside of it and “5” below it. S6 is the yellow box on the right side of Figure 12 with “6” inside of it and “6” above it. Final design parameters for a Rectifier and filter can be viewed in Appendix G. Appendix G represents a design without the stubs added for using SMA connectors to test the design.

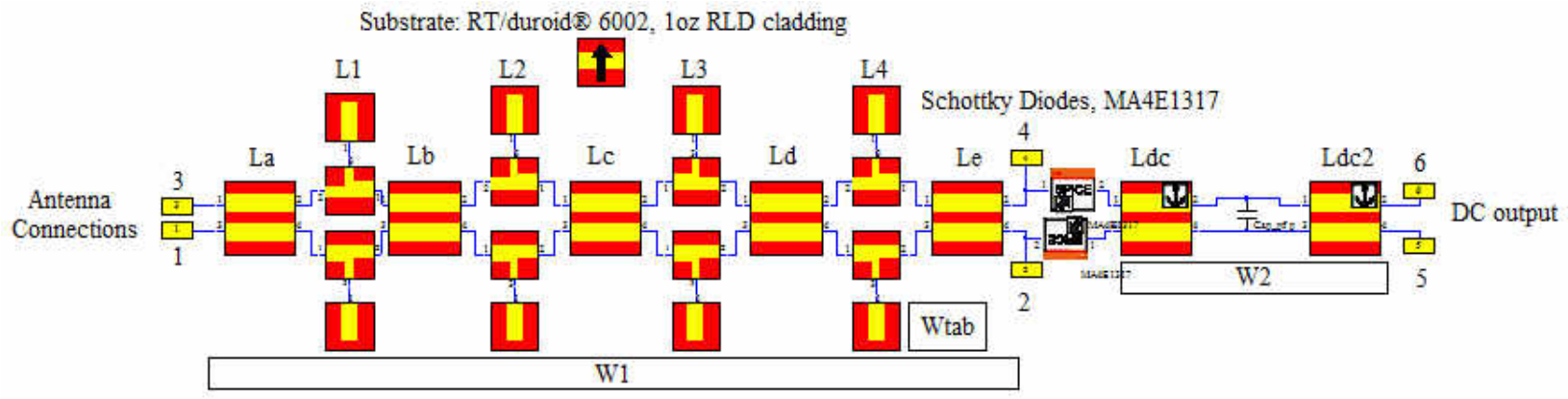

Figure 17: Layout of Harmonic Rejection Filter (HRF) with Dual Diode design. The red and yellow blocks are representations of CPS. The spice blocks to the right of the Ports "2" and "4" are links to spice file representations of the diode MA4E1317 [12].

i. Diode Analysis

The calculations used in the diode analysis were those is equations (1)-(9) using the parameters from the respective datasheets [21, 27]. The calculations and plots used in the diode analysis were completed using the MATLAB software package [31]. The script for the diode calculations is presented in Appendix C. The calculated impedance from the BAT17 can be viewed in Figure 18. The MA4E1317 impedance served as a control to ensure the BAT17 calculations were correct. The MA4E1317 impedance values were approximately the same as those found in [17]. The impedance of the MA4E1317 can be seen in Figure 19. After the efficiency calculations were completed for both the BAT17 and MA4E1317, it was quite clear that the MA4E1317 was a better diode for this application than the BAT17. To view the results, compare Figure 20 to Figure 21.

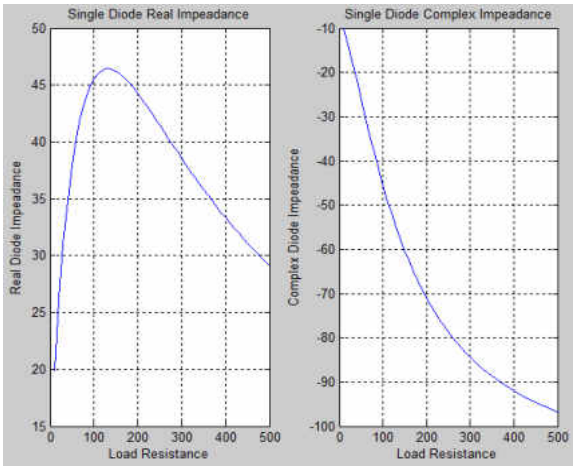

Figure 18: BAT17 single diode calculated impedance.

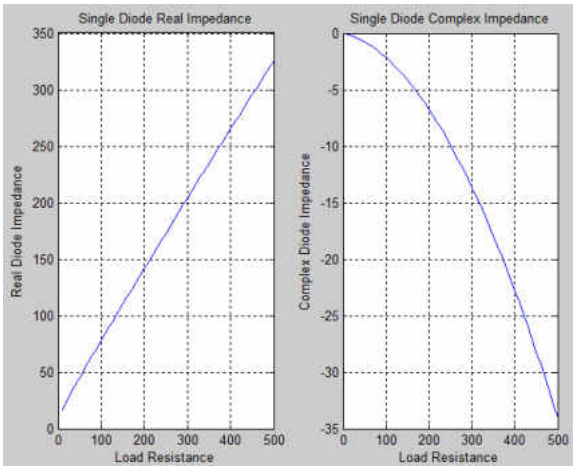

Figure 19: MA4E1317 single diode calculated impedance.

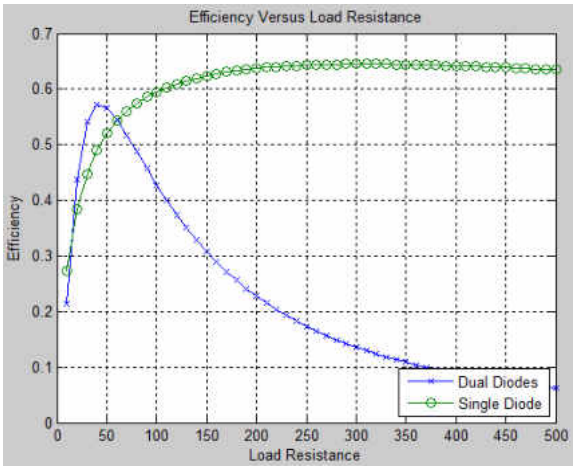

Figure 20: BAT17 calculated single and dual diode efficiency.

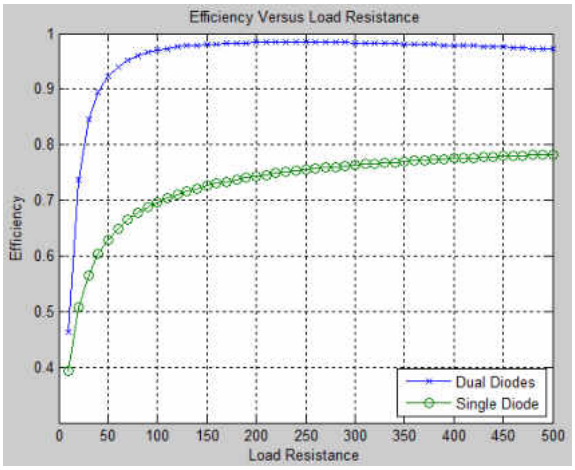

Figure 21: MA4E1317 calculated single and dual diode efficiency.

By using the efficiency calculations provided in [4] a good comparison was made between the BAT17 and MA4E1317. Upon reviewing the results of the efficiency graphs in Figure 20 and Figure 21, the decision to only continue with the MA4E1317 was made.

Once the diode was chosen the rectifier was chosen to match to 100 Ω. 100 Ω was chosen to match the diode impedance when there is a load resistance R_L of 135 Ω, as seen in Figure 19. The antenna design will also match the 100 Ω to maintain the maximum power transfer to the load. The widths of the HRF traces and the length d_{dc} were calculated and optimized by CST with an initial trace width of 0.75 mm and a d_{dc} length of 0.0 mm.

The decision to choose a single shunt diode or dual diodes was based on the results of previous data shown in Figure 11 and Figure 21. Figure 11 shows that the output voltage of the dual diodes can exceed twice the voltage of the single shunt diode topology. Figure 21 shows that the diode model for the MA4E1317 predicts the dual diodes to be more efficient than the single shunt diode.

b. Rectenna Array Design

The prototype will use the results of [10, 24] to guide the array design. The primary goal will be to incorporate as many elements into a cascaded array. The next step used will be putting sub-arrays of cascaded elements in parallel. The proposed design will be to combine the rectennas on each 10 cm x 10 cm panel. Then to cascade 3 of the 10 cm × 10 cm panels. The satellite will have a total of 3 sections, each section with 3 panels. The tree panels in a section will be connected via the cascaded method shown in Figure 14. All three sections on the satellite will be placed in series and then connected to a single DC-to-DC converter. Placing rectennas in series may be the least efficient, but if the antennas are placed in series the voltage to the DC converter will be higher and thus more efficient to regulate through the DC converter. This design would be very similar to the image in Figure 6. A satellite with a 3 x 3 array of panels can be viewed in Figure 1 and Figure 13. The proposed design needs to be reassessed once the hardware of a single element has been built and tested. The proposed design is an educated guess as to the most efficient interconnection method of the proposed design.

The elements on each panel will be cascaded to produce the most voltage per panel, so that more panels may be connected in parallel to each converter. Figure 22 shows that with a power irradiance of 10mW/cm^2 and two cascaded elements 18V can be produced. Since the receiving craft will be designed to receive a wide range of input power, the voltage near 1mW/cm^2 and 10mW/cm^2 are also important. Based on Figure 22, 1mW/cm^2 and 10mW/cm^2 will produce 10V and 18V, respectively [10]. The range of 10 to 20V will be more than acceptable for the chosen DC to DC converter.

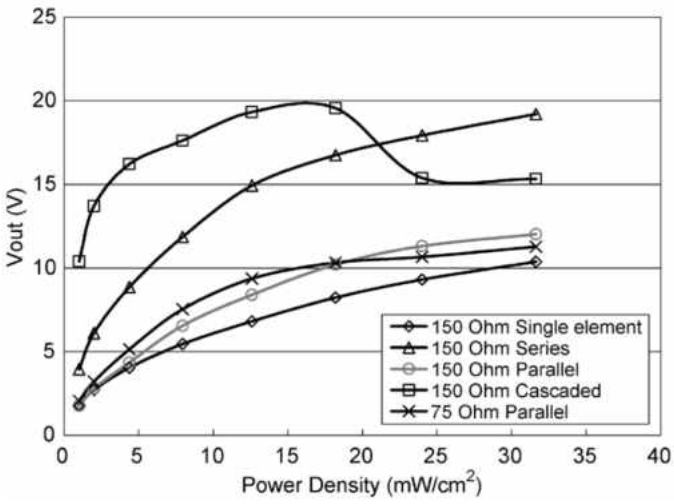

Figure 22: Measured DC output voltage of the rectenna array [10].

c. DC-to-DC Converter

Since the application for this design is for space, an attempt was made to find space-qualified parts for testing. The application also desires the most efficient parts. The consideration of different voltage regulator topologies was limited to a monolithic buck/boost converter due to the potential for wide ranges of inputs and the desire for a highly efficient design. The buck/boost converter TSP63060-EP produced by Texas Instruments was chosen. The TSP63060-EP is not specifically qualified for space, but has a high reliability rating in combination with an operating temperature of –55°C to 125°C [26]. Upon further review of the datasheet, it was noted that the part had a maximum output voltage of 8V, which was not high enough for the maximum charged voltage of the Clyde Space battery [16, 26]. Another round of searching was done to find a replacement part with a wider range of input and output voltages and a qualified rating. LTC3115MP-1 by Linear Technology (LT) was found. The part is not a high reliability or space qualified part, but it is made from a military grade plastic. The LT part has an adjustable output

voltage from 3V to 40V [25]. The LTC3115MP-1 is compared to the design specifications of this work in Table 4.

	Design Requirement	LTC3115-1
V_{in}	4V< V_{in} <20V	3V< V_{in} <40V
V_{out}	9V	3V< V_{out} <40V
I_{out} (Max)	2A	2.25A

Table 4: List of DC to DC Converter design constraints with the capabilities of the chosen part for the design.

The calculations necessary to design the buck/boost converter using the chosen LTC3115MP-1 part were completed by using equations (10)-(19) in addition to calculations found in [25], [28] and [31]. All of the calculations used to design the circuit involving the LTC3115MP-1 were completed using a script created in MATLAB, which is provided in Appendix A. The results of the calculations and the scripts are given in Appendix B. The converter with all of the designed supporting components can be seen in Figure 23. The components selected based on MATLAB code in Appendix A and the results from appendix A are shown in Appendix B. The results from LTSPICE and MATLAB simulations for each supporting component associated with the converter are listed in Table 5. The LTC3115MP-1 datasheet gave directions on ensuring that the Voltage Compensation (VC) network was designed properly.

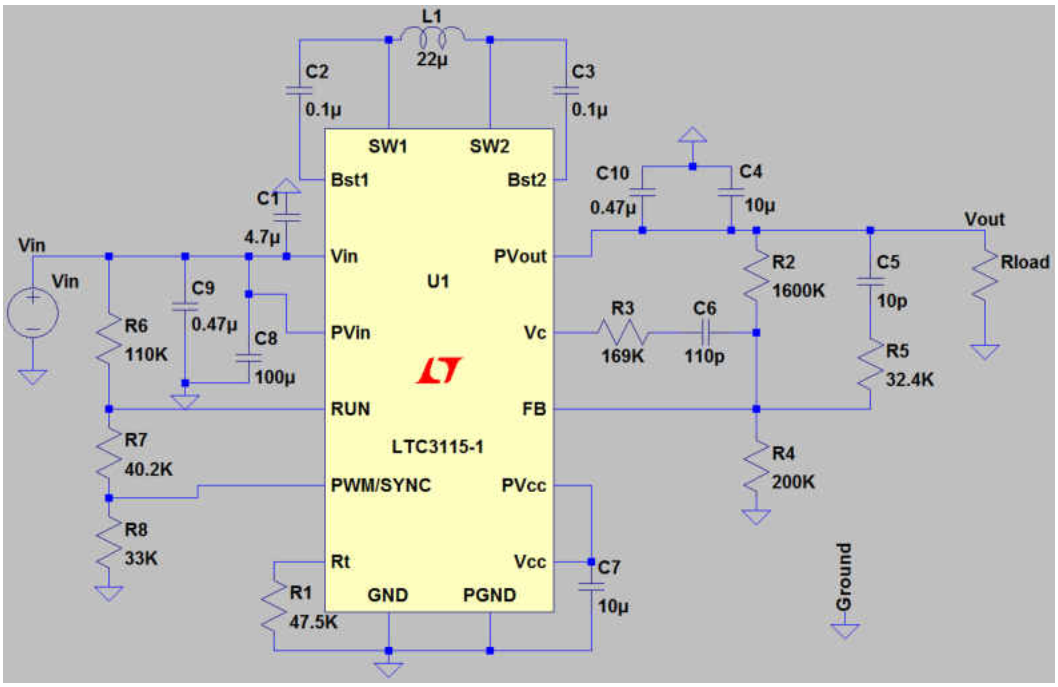

Figure 23: LTC3115-1 DC to DC buck/boost converter laid out in LTSPICE [36].

Component Name	Value	Units
R1	47.5	kΩ
R2	1.60	MΩ
R3	169	kΩ
R4	200	kΩ
R5	32.4	kΩ
R6	110	kΩ
R7	40.2	kΩ
R8	33	kΩ
L1	22	µH
C1	4.7	µF
C2	0.1	µF
C3	0.1	µF
C4	10	µF
C5	10	pF
C6	110	pF
C7	10	µF
C8	100	µF
C9	0.47	µF
C10	0.47	µF

Table 5: List of components and component values for LTC3115-1 buck/boost converter.

The design of voltage compensation network is one of the most difficult sections of the DC converter design. Generally, a Bode plot is helpful in ensuring that the gain of the DC converter during Buck mode will be a fixed value. A type III VC network was chosen and designed to provide an optimized output voltage transient [25].

To design the VC network a simulation is needed to find the Bode plot. In Figure 24, a sample bode plot can be seen with the gain and phase separated out [25]. In Figure 24, the gain does not have specific values to be looking for like the phase does. Reference [25] is a great resource that explains step-by-step instructions of how to analyze and choose values based on a bode plot. The LTSPICE simulation test setup used to find the Bode plot for this work can be viewed in Figure 25. The final result of the design was a -180 degree phase margin and a -5dB crossover frequency. The goal of the design was to achieve a -180 degree phase margin and a 0dB crossover frequency based on the recommendations from the converter datasheet [25]. The final results were approximated with the calculation results in Appendix B. Then the calculations were plugged into the LTSpice Simulation to verify and refine the result. The values chosen also took into account commercially available parts to expedite the design process time. Further schematics, test results and additional reading can be found in Appendix E.

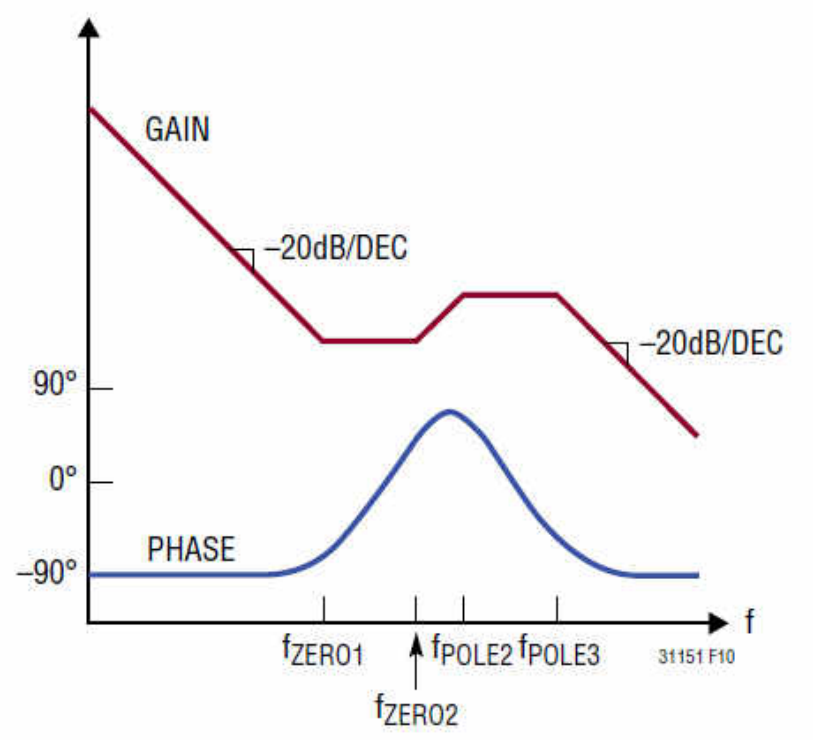

Figure 24: Bode plot example from the LT31151 DC-to-DC converter data sheet [25].

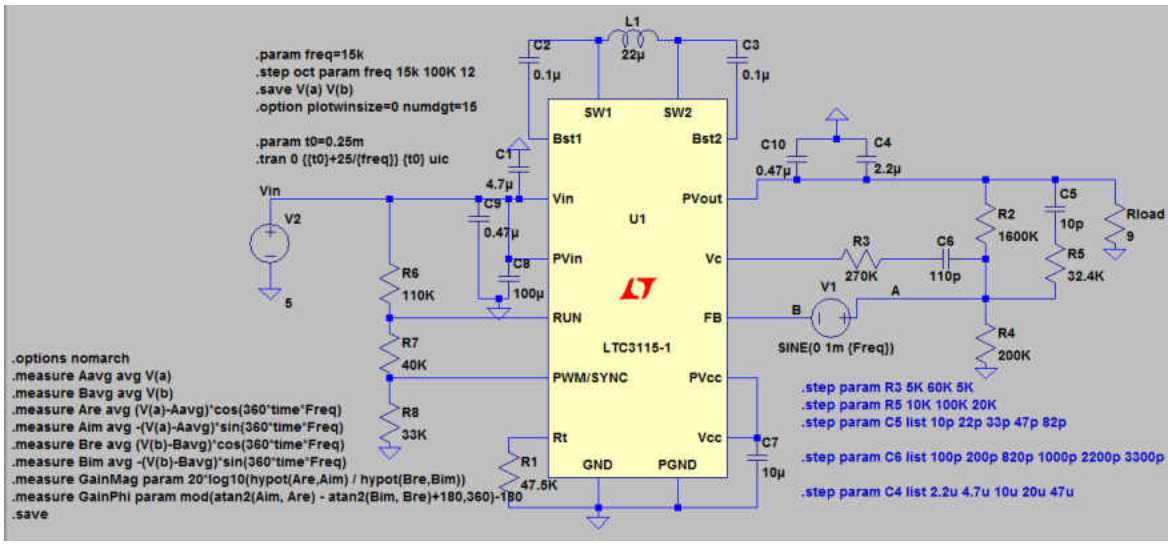

Figure 25: DC-to-DC converter and test set up used to determine the Bode plot using LTSPICE [36].

IV. PROTOTYPE MANUFACTURING & TESTING

The prototypes produced consisted of three different subsystems. The first prototype was the complete rectifier. The second prototype was the filter used in the rectifier design. The filter was manufactured independently in order to characterize its S-Parameters. The third prototype was the DC-to-DC buck/boost converter. The following describes how each prototype was manufactured and tested. The methods described below do not include the procedures used in design simulations.

a. Rectifier Manufacturing

The rectifier was manufactured based on the proposed design that was simulated, using Rogers Duroid 6002 0.006'' 1oz copper substrate. The rectifier PCB was manufactured in house by using the etching process with Ferric Chloride. The metal was preserved on the substrate by transferring tonner to the areas where copper was to remain. A permanent marker was used to fix any areas where the toner did not transfer properly. The permanent marker was also used to black out the ground plane on the reverse side of the rectifier. After the etching process was complete, it was very clear that the permanent marker was not enough to repel the Ferric Chloride from the ground plane as seen in Figure 26 (a). To ensure a proper ground plane is on the rectifier a layer of 1oz copper tape was applied to the ground plane as seen in Figure 26 (b).

3.5mm SMA connectors were soldered to the rectifier ports. Attaching the Schottky diodes was a challenge due to their size. The decision to use a conductive epoxy on the diodes was made based on a lack of previous experience with solder paste, the cost effectiveness of obtaining sample conductive epoxy, and the fact that previous designs had successfully used conductive epoxy [10]. The silver epoxy AA-DUCT-904 from Atom Adhesives [32] was selected due to multiple reasons such as: cost effectiveness, syringe application, and a one-part solution that could be cured using heat.

(a) (b)

Figure 26: a) Image of the deteriorated ground plane on the rectifier b) Image of the ground plane with the attached copper tape

Due to the small surface area needed to secure the diodes, the epoxy did not cure properly. Customer service at Atomic Adhesives determined that the product AA-DUCT-904 did not have enough hardener in the product to cure properly for the small application area. The diodes were then secured by another cold solder material, AA-DUCT-905, sent by Atomic Adhesives. The diodes and epoxy area can be seen to the left of the arrow placed in Figure 27.

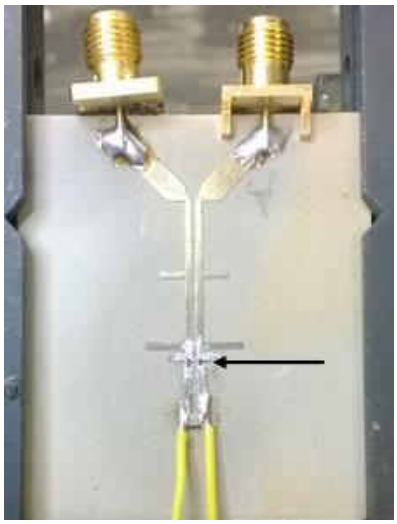

Figure 27: Image of the rectifier prototype. The arrow indicates the diodes that were placed on the board.

b. Rectifier Filter Manufacturing

The rectifier filter board was etched using the same process as the rectifier. However, when etching the filter, the ground plane was preserved much better. The ground plane was preserved by printing a square of toner and applying that to the ground plane. A permanent marker was used to fill in the holes where the toner did not transfer properly. On top of the toner coated ground plane a white shipping label was placed to ensure a more durable coating to prevent copper removal. The extra precautions on the ground plane were successful in keeping the integrity of the ground plane.

c. DC-to DC-Converter Manufacturing

The DC buck/boost converter was laid out for PCB manufacturing using Ultiboard software by National Instruments [33]. The layout can be seen in Figure 28. The PCB board is a two-layer FR4 material. The copper on each layer of this board is 1oz/sqft copper or approximately 35µm in thickness. The material selected for the DC converter was based purely

on cost. The decision to use FR4 instead of a space qualified material should not impact the testing procedure or results of the circuit, unless the space qualified material had better heat dissipation properties. For actual applications, a space qualified board material would be used that could allow vias. The most critical part in choosing a board material for the specified space application design would be for the board to have good heat dissipation qualities. Before sending the design to fabrication, four copies of the layout were placed on a single board to be produced in order to save on the manufacturing cost. The design sent out for manufacturing can be seen in Figure 29. The PCB for the DC-to-DC converter was manufactured by Advanced Circuits [34]. The manufactured PCB can be seen in Figure 31. The only issue with the production of the DC converter was that the ground tab under U1 did not contain a keep out for the solder mask, so before assembly the solder mask was removed by scrapping the material off. A fully populated DC converter can be viewed in Figure 32.

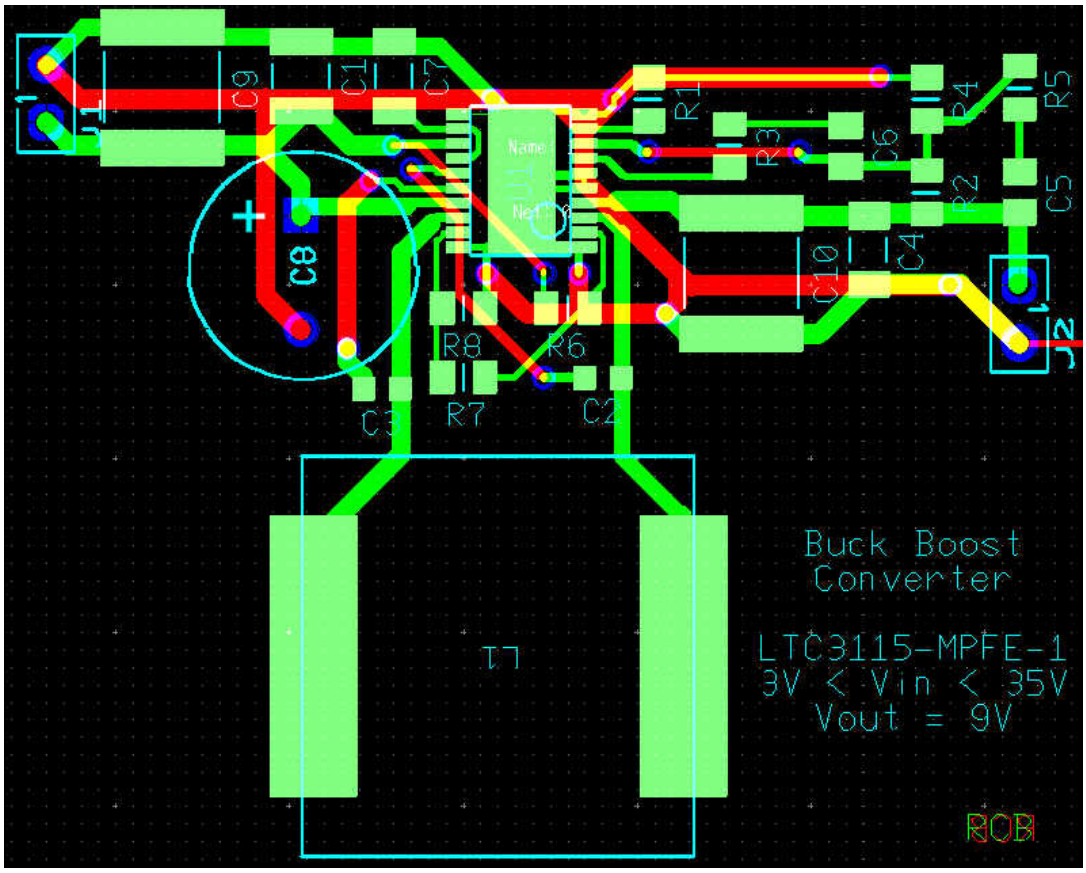

Figure 28: Single converter lay out. Approximate size: 2'' wide x 1.7'' high. Copper Top is green and the copper bottom is colored red. The bottom also has a ground plane to assist with heat dissipation, not shown.

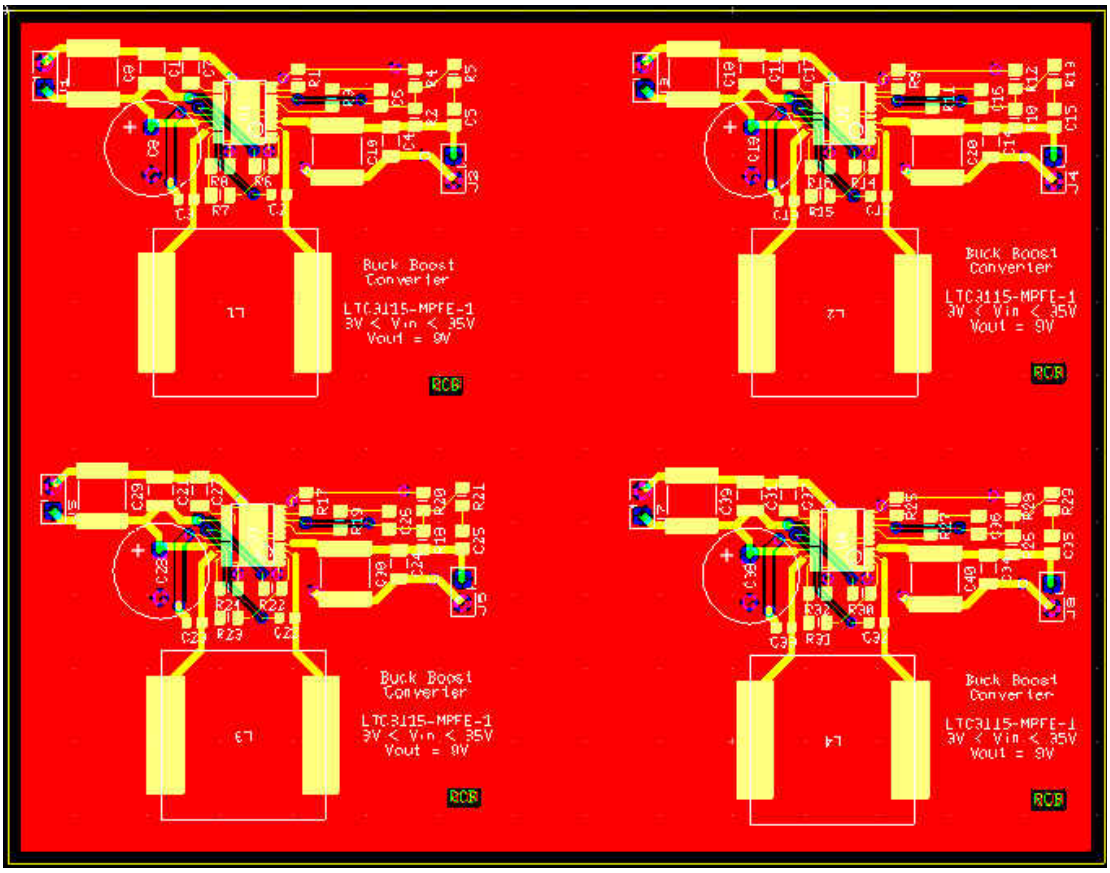

Figure 29: Array of 4 converters placed on a single PCB. Approximate size: 4.5" wide x 3.5" high. Copper Top is green and the copper bottom is colored red. The bottom also has a ground plane, shown here, to assist with heat dissipation.

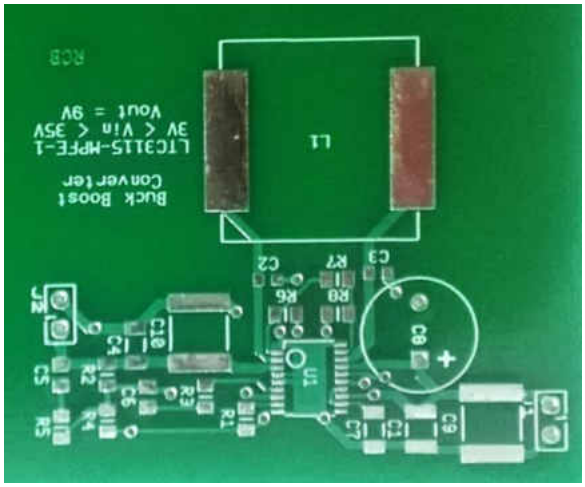

Figure 30: Image of a single DC converter PCB produced by Advanced Circuits.

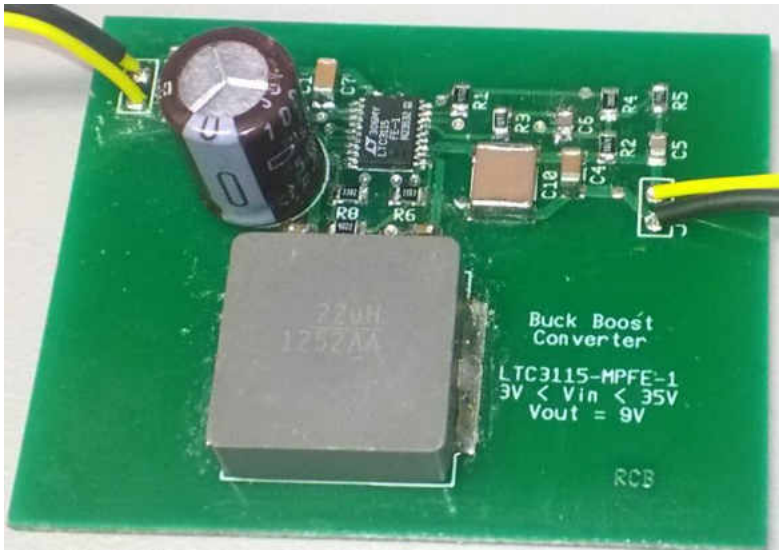

Figure 31: Image of a single DC-DC buck/boost converter PCB the author populated by hand.

d. Rectifier Testing

Testing the rectifier was attempted to show the proof of concept. The test set-up can be seen in Figure 33. The process for testing the rectifier is as follows:

1. Obtain the following: a signal generator capable of generating a signal frequency, equal or greater than 6GHz, one SMA male to male cable, oscilloscope with appropriate probe.
2. Connect the signal generator to one side of the SMA cables and the other end of the SMA cable to one SMA port of the rectifier, as seen in Figure 27.
3. Properly connect the oscilloscope to the probe chosen and then connect the signal end of the probe to the rectifier output, one of the wires protruding from the substrate in Figure 27. Connect the ground on the probe to the ground plane of the rectifier.
4. Turn on the signal generator and keep the signal to the rectifier turned off while adjusting the settings of the signal generator.
5. Turn on the oscilloscope and adjust the settings to see the rectifier output.

6. Set the frequency of the signal generator to 5.8GHz and the power output equal to +10dBm. Turn on the signal to the rectifier and record the results.
7. Repeat step 5 by increasing the power output of the signal generator in steps of 0.5 dBm until the oscilloscope detects that the rectifier is producing a DC output voltage.

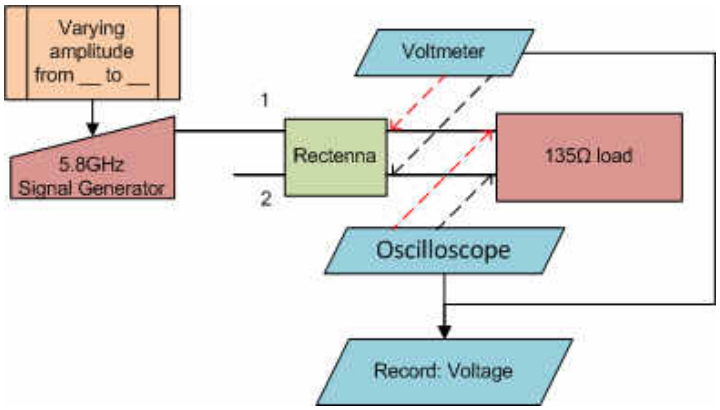

Figure 32: Test setup for rectifier. A single port was tested at a time since the signal generator used only had a single RF output.

e. Rectifier Filter Testing

Testing of the individual filter in the rectifier was carried to show the simulated S-Parameter results were realistic. Fig. 34 show the test setup for the rectifier filter. The rectifier tested can be seen in Figure 35. The process for testing the rectifier filter is as follows:

1. Obtain the following: a network analyzer that has a band width above 20GHz to be able to see the 3rd harmonic of the fundamental frequency (17.4GHz), two (2) SMA male to male cables, and three (3) 50Ω terminators.
2. Calibrate the network analyzer for a single port device.
3. Connect the network analyzer to one end of a cable and the other end of the cable to the filter port 1.

4. Terminate the remaining ports with the 50Ω terminators (ports 2-4).
5. Measure and record the results of the S-Parameters on the network analyzer. Be sure to export the data and properly label it for use later.
6. Repeat steps 3-5 for ports 2-4.
7. Calibrate the network analyzer for a dual port device.
8. Connect the network analyzer to one end of a cable and the other end of the cable to the filter port 1. Connect a second cable to port 2 and the other end of the second cable to the network analyzer.
9. Terminate the remaining ports with the 50Ω terminators (ports 3 and 4).
10. Measure and record the results of the S-Parameters on the network analyzer. Be sure to export the data and properly label it for use later.
11. Repeat steps 8-10 for the following connections: port 3 and 4, port 1 and 4, and port 2 and 3.

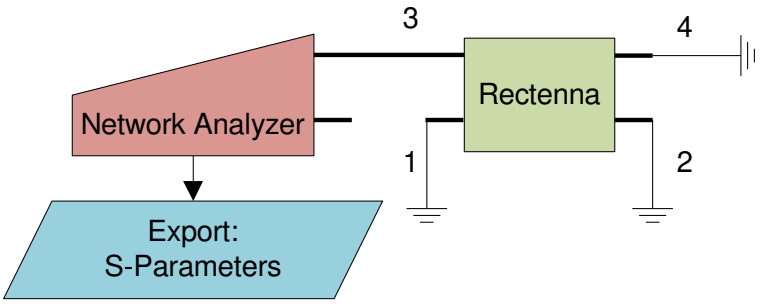

Figure 33: Test setup for the testing of the rectifier filter. The network analyzer has 2 ports to be able to test the S_{12} parameter and other combinations listed in step 11 of the testing.

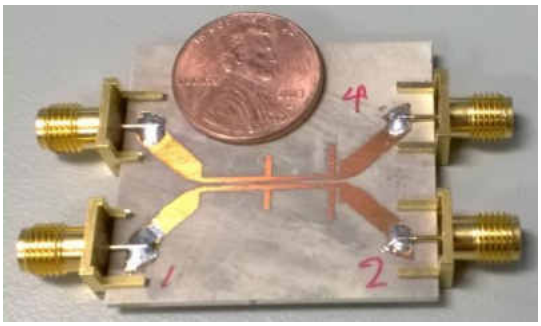

Figure 34: Filter only design. The port nearest to the penny is port 3.

f. DC-to-DC Converter Testing

The testing of the converter provides an efficiency curve for various power inputs and loads. The test setup used for the testing of the converter can be seen in Figure 36. This information can be used in future to further optimize the rectenna and rectenna array design. Note this testing can be dangerous if the proper load resistors are not used. All resistors for this testing should be able to individually handle at least 50W.

1. Obtain the following: DC power source capable of outputs from 0V to 40V and a maximum current of greater than 2.5A, wire leads to connect the DC converter and power supply, various power resistors to be able to vary the load of converter (recommended resistances are 18Ω, 9Ω, 4.5Ω, and 4Ω in order to correspond with the following load currents 0.5A, 1A, 2A, and 2.25A), an Oscilloscope or digital multi-meter, and proper probes to connect the oscilloscope to the converter.
2. Connect the positive and ground leads on the converter to the corresponding connections on the DC power supply.
3. Connect a probe across the output of the converter.

4. Connect the 18Ω resistor to the output of the converter.
5. Vary the input voltage from 2V to 38V. Record the input voltage and current, output resistor, the output voltage and output current of the converter.
6. Repeat steps 4 and 5 with the following resistors 9Ω, 4.5Ω, and 4Ω.
7. Use the data collected to create efficiency graphs for each load resistor.

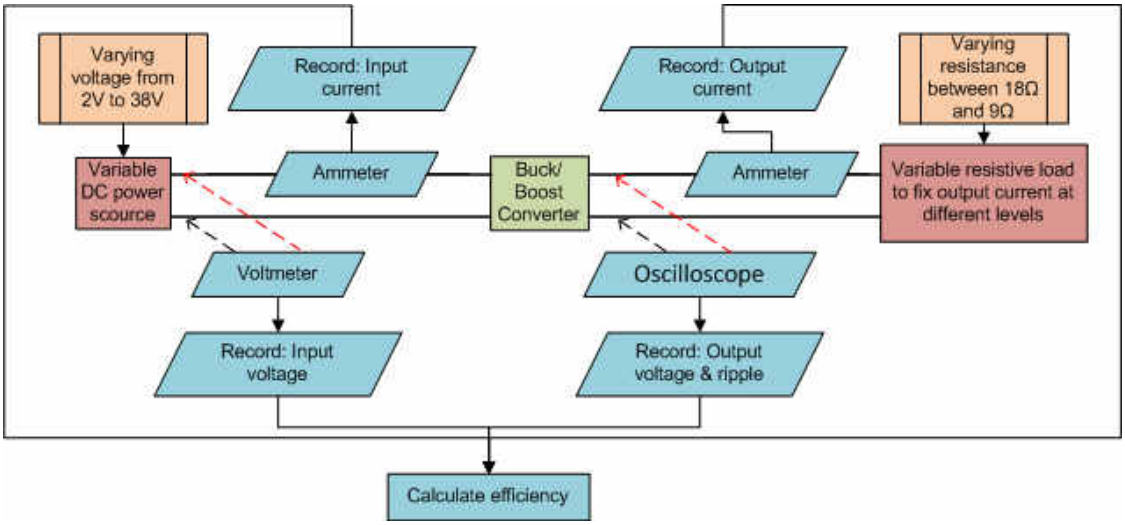

Figure 35: Test setup of the buck/boost converter.

g. Testing Setup Notes

The test setup did not excite both ports of the filter rectifier at the same time due to the lack of necessary equipment. To excite both ports of the rectifier and rectify a signal, two signal generators would have been needed to be 180° out of phase for the maximum efficiency of the rectifier. The network analyzer used was Agilent Technologies E5071C 300kHz-25GHz model. The signal generator used was ANRITSU MD3692C. The oscilloscope used was a Tektronix TDS 2002B with AK220 60MHz probes. The limit of 60MHz bandwidth should not be an issue for measuring

the rectifier output since the output should be purely DC. The cables used were SMA male-to-male PCA9125-12 cable.

When testing the DC converter, a current probe for an oscilloscope was not used in the testing and verification due to the lack of equipment in the laboratory. It is recommended to use a current probe to assist in detecting any flaws in the design of the DC converter and the feedback loop for the converter. An oscilloscope is recommended for measuring the output voltage of the DC converter instead of a multi-meter due to the ability to more easily view and measure any output voltage ripple.

VI. RESULTS

Looking at the spectral density of the rectifier one is able to see how the energy is transformed and converted from high frequency into DC energy. Figure 37 below shows the simulation test setup that was used and where the test points were located.

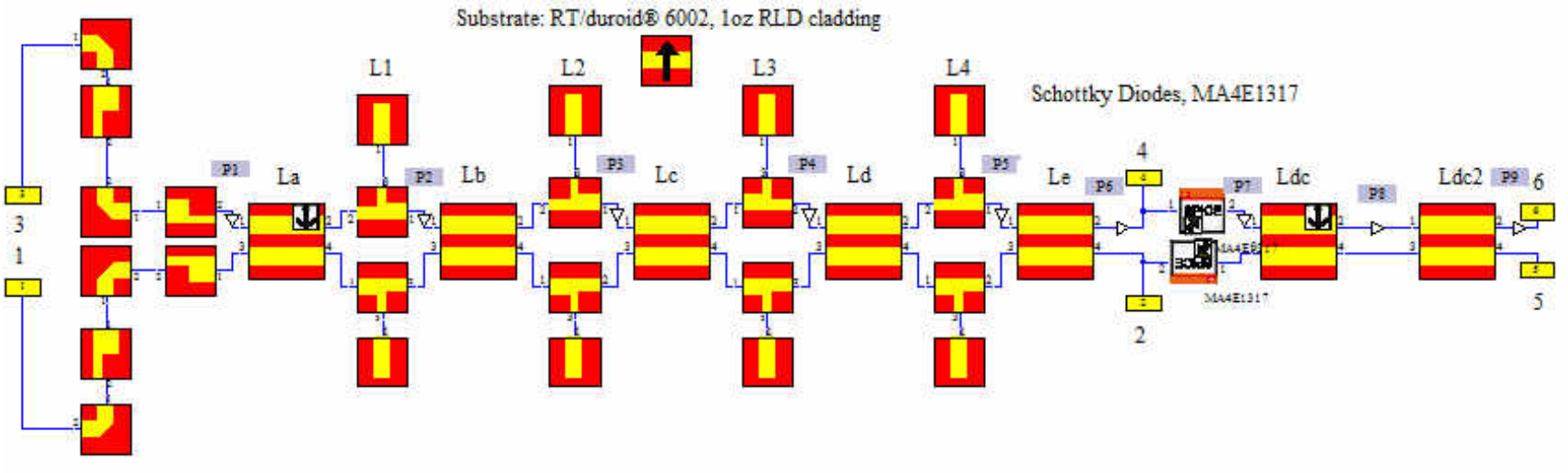

Figure 36: Rectifier layout showing the test points used in the spectral density testing. Each gray box has an increasing probe number starting at the left of Length A or La.

The quantities on the following graphs are not nearly important as the qualitative explanation of how the energy is converted into DC. It is also important to note that the simulation was unable to show the energy density at a frequency of 0Hz or the DC values. Figures 38 to 47 are for the energy in only one half of the rectifier (the energy between Port 3 and R_{Load}), in order to get the correct values everything should be doubled in magnitude. As seen in Figure 38, the overall energy density is mostly centered about 5.8 GHz, 11.6GHz and 17.4 GHz in the order of decreasing energy density. In Figure 38 the graph shows the initial energy in the rectifier injected to the circuit through Port 3. The following graphs, Figures 38 to 47, show points along the circuit and take snapshots of the energy spectral density. At point 1 (P1) the energy can be seen to be centered and is the densest at 5.8GHz, as seen in Figure 39. This is logical since the source had a center frequency of 5.8GHz and P1 was right before the filter designed to capture and harvest the energy from 5.8GHz to DC (0Hz).

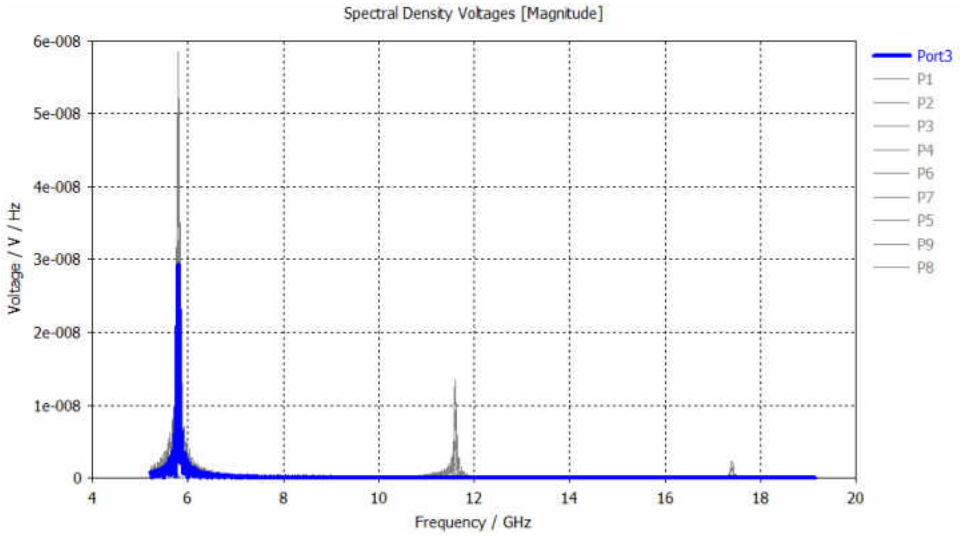

Figure 37: Port 3

Table 6 shows the values of the spectral energy density of Figure 37 through Figure 46 at 5.8 GHz, 11.6 GHz and 17.4 GHz. The values shown are multiplied by 10^{-8}. The units are V / V / Hz.

Spectral energy density of rectifier			
Location	5.8 GHz	11.6 GHz	17.4 GHz
Port 3	3	0	0
P1	5.8	0.95	0
P2	3.2	0.15	0.05
P3	4.8	0.4	0.15
P4	5	0.9	0.2
P5	4.9	1.25	0.15
P6	4.25	1.25	0.15
P7	0	0	0
P8	0	0	0
P9	0	0	0

Table 6: Spectral energy density of Figure 37 through Figure 46. The values shown are multiplied by 10^{-8}. The units of the values above are V / V / Hz.

At point 1 (P1) in Figure 39, the energy is increased due to the harmonic reflections from the diodes. The energy will continue to increase or decrease depending on which points the harmonics are being reflected back to the diodes. At this point the energy is has the most density at the primary frequency of 5.8GHz. At this point the energy is the greatest along the rectifier. A small portion of the energy is centered on the second harmonic of 11.6GHz.

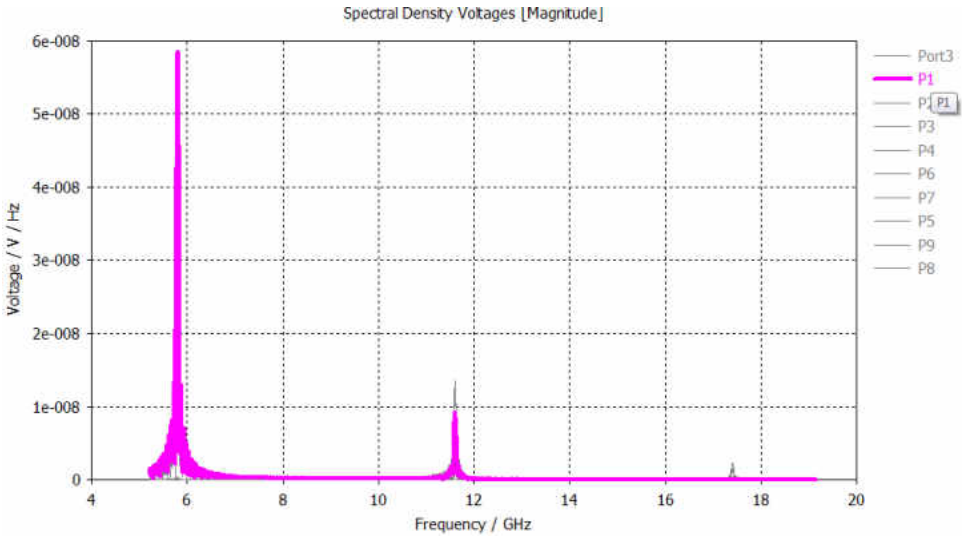

Figure 38: Point 1 (P1)

At point 2 (P2) in Figure 40, the energy is the densest at the primary frequency of 5.8GHz. A small portion of the energy is centered on the second harmonic of 11.6GHz. It appears that a tiny portion of the energy can be seen centered on the third harmonic of 17.4GHz.

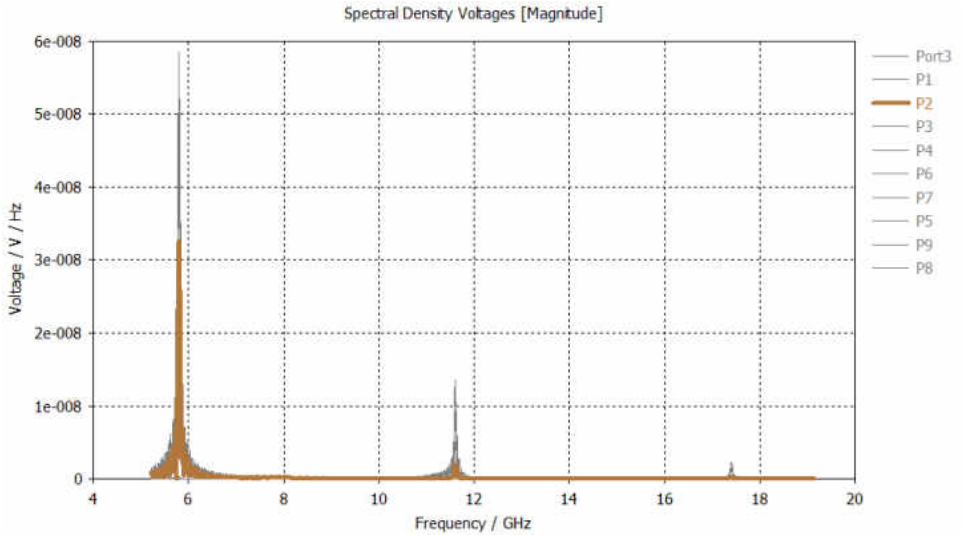

Figure 39: Point 2 (P2)

At point 3 (P3) in Figure 41, again the energy is the densest at the primary frequency of 5.8GHz. A small portion of the energy is centered on the second harmonic of 11.6GHz. It appears that a tiny portion of the energy can be seen centered on the third harmonic of 17.4GHz.

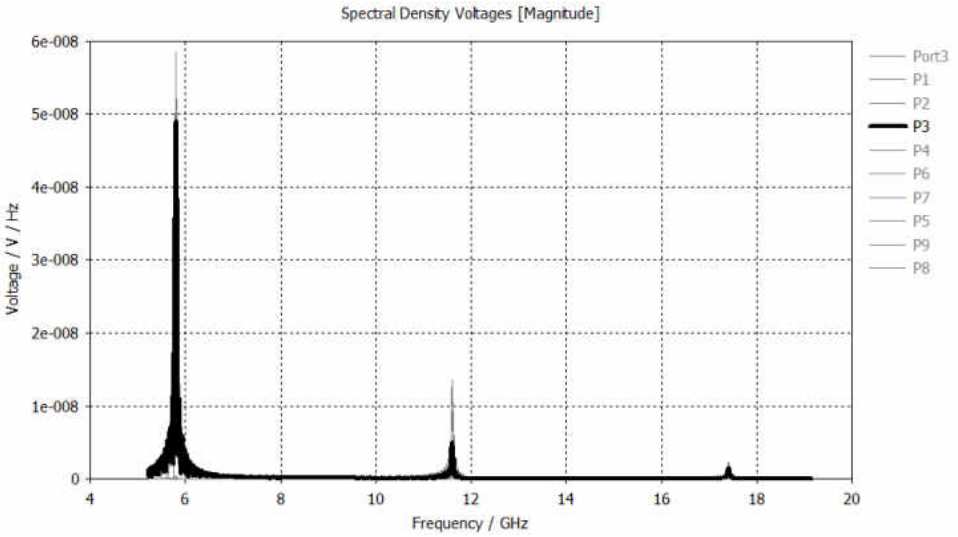

Figure 40: Point 3 (P3)

At point 4 (P4) in Figure 42, again the energy is maximum at the primary frequency of 5.8GHz. The small portion of the energy centered on the second harmonic of 11.6GHz will continue to increase. The third harmonic of 17.4GHz has the greatest density at this point along the rectifier.

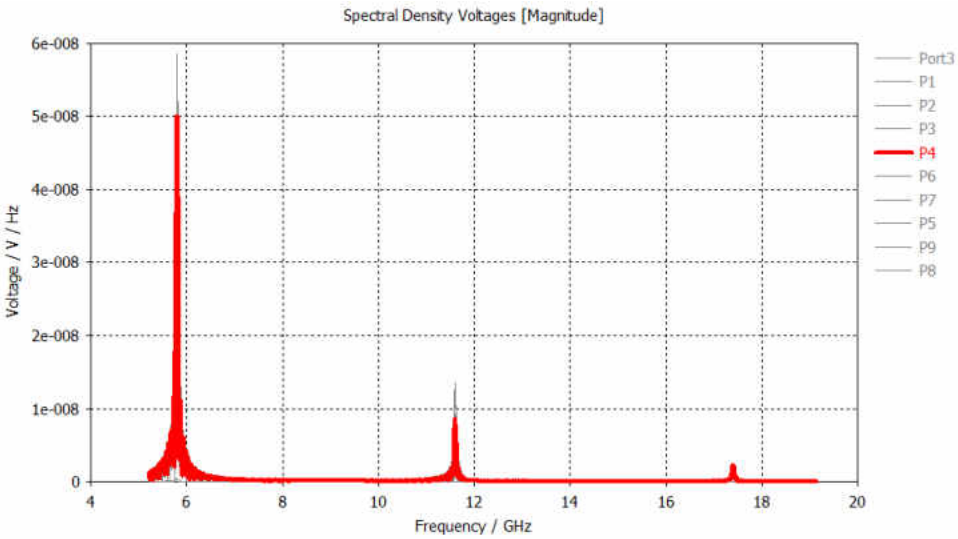

Figure 41: Point 4 (P4)

At point 5 (P5) in Figure 43, again the energy is maximum at the primary frequency of 5.8GHz. The small portion of the energy centered on the second harmonic of 11.6GHz is at the greatest density along the rectifier. The energy of the third harmonic at 17.4GHz is again reduced.

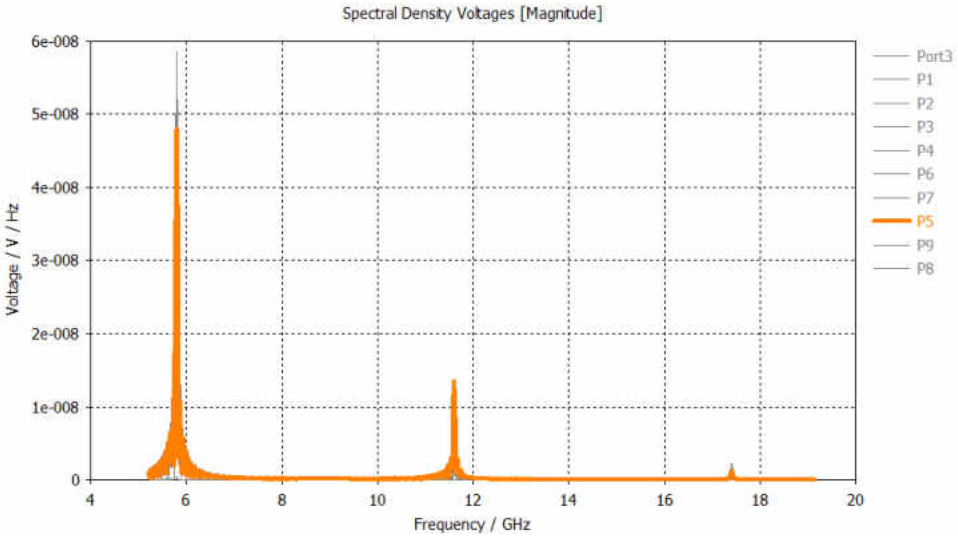

Figure 42: Point 5 (P5)

At point 6 (P6) in Figure 44, again the energy is mostly around at the primary frequency of 5.8GHz. The small portion of the energy centered on the second harmonic of 11.6GHz is at the greatest density along the rectifier. The energy of the third harmonic at 17.4GHz is again reduced.

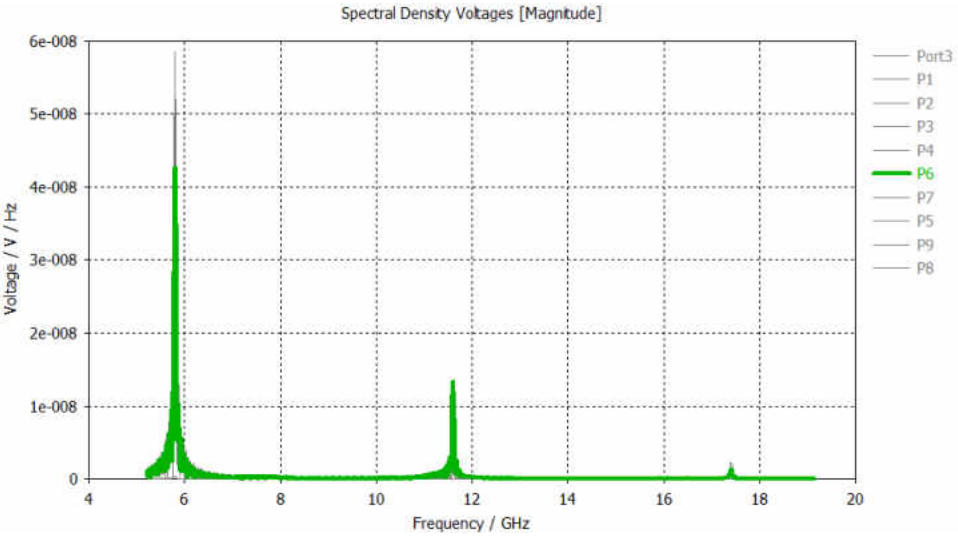

Figure 43: Point 6 (P6)

Point 7 (P7) in Figure 45, is the first point after the rectifying diodes. If the diodes rectify all of the energy, then all of the density should be shown at a Frequency of 0 Hz. 0 Hz is not shown on this graph, but all frequencies shown have no energy density which suggests that all of the energy was rectified.

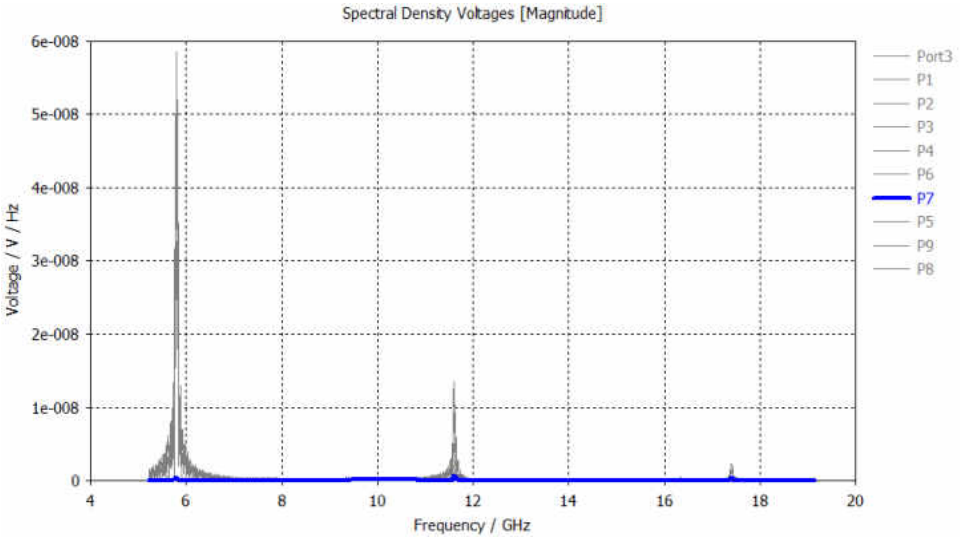

Figure 44: Point 7 (P7)

At point 8 (P8) in Figure 46 and point 9 (P9) in Figure 47 are also after the rectifying diodes and show that there is no microwave energy was allowed to pass.

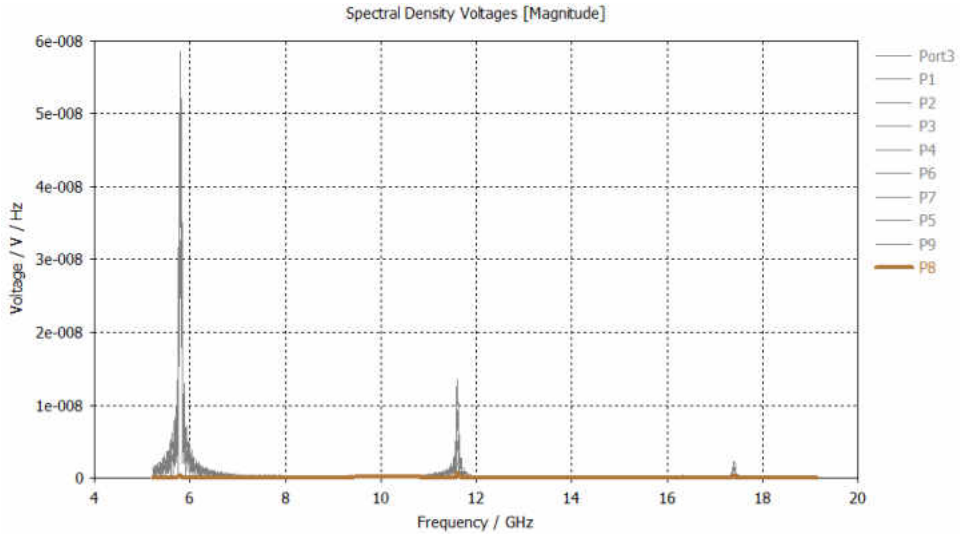

Figure 45: Point 8 (P8)

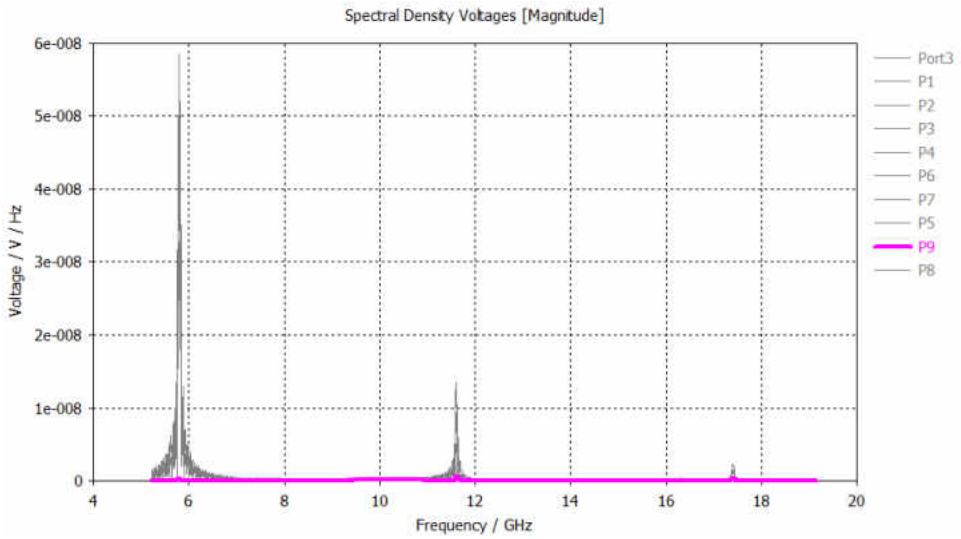

Figure 46: Point 9 (P9)

a. Rectifier Filter

The Filter only design cannot be used to compare or show any voltages. The design can only be used to show the S-Parameters of the filter used in the Rectifier prototype. When viewing the results, one has to remember that the design is not optimal due to the impedance transformers that needed to be added for testing.

The simulated filter results are shown in Figures 48-53. The S_{11} is an exact replica of the S_{33}. The results of S_{12}: S_{21}; and S_{34}: S_{43} are all copies of each other as well. In general, the measured results achieved similar results to the simulated results in terms of dB attenuation. However, every filtering dip in dB resulted in a frequency shift. In Figures 48-53, The dB measures the change in power. The positive means a gain in power output relative to the input power and the negatives represent a loss in power output compared to the input power.

The simulated results for S_{11}, shown in Figure 48, at 5.8GHz could have been improved for the initial design to prevent reradiating energy. This improvement would have resulted in a

center frequency of 5.8GHz. The actual results show a frequency shift at the desired center point of 6.3GHz to 4.9GHz. No other frequency was necessary to be passed or filtered out on S_{33}.

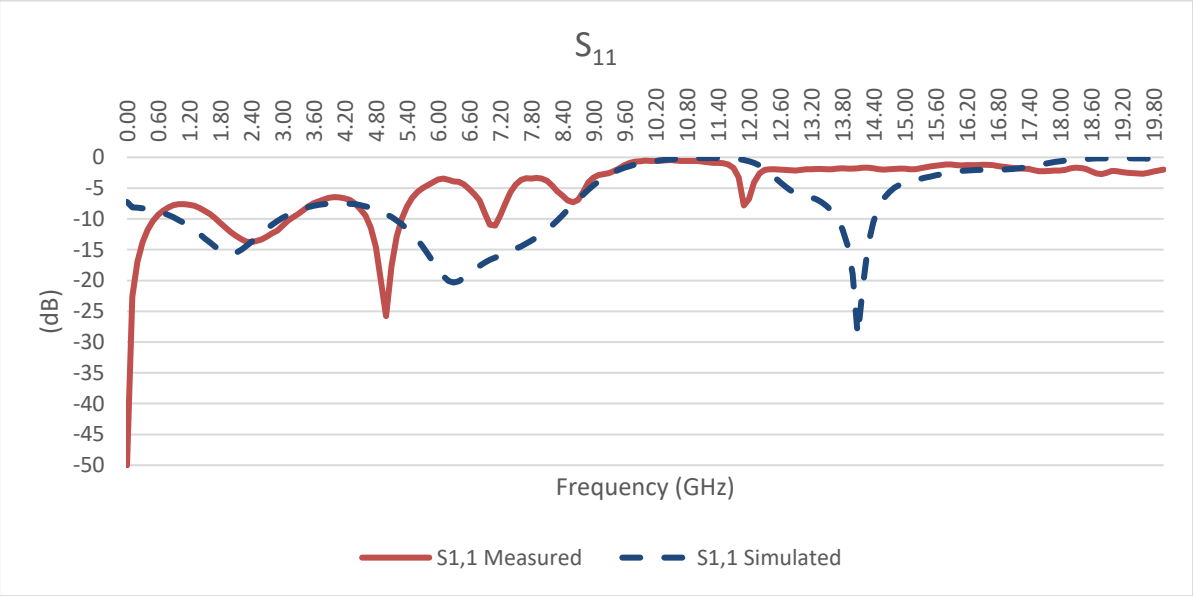

Figure 47: Measured and simulated S_{11} parameters of the filter only prototype.

The results from the S_{33}, shown in Figure 49, match those from S_{11} quite well, suggesting that there is good symmetry in the design between the two halves of the filter.

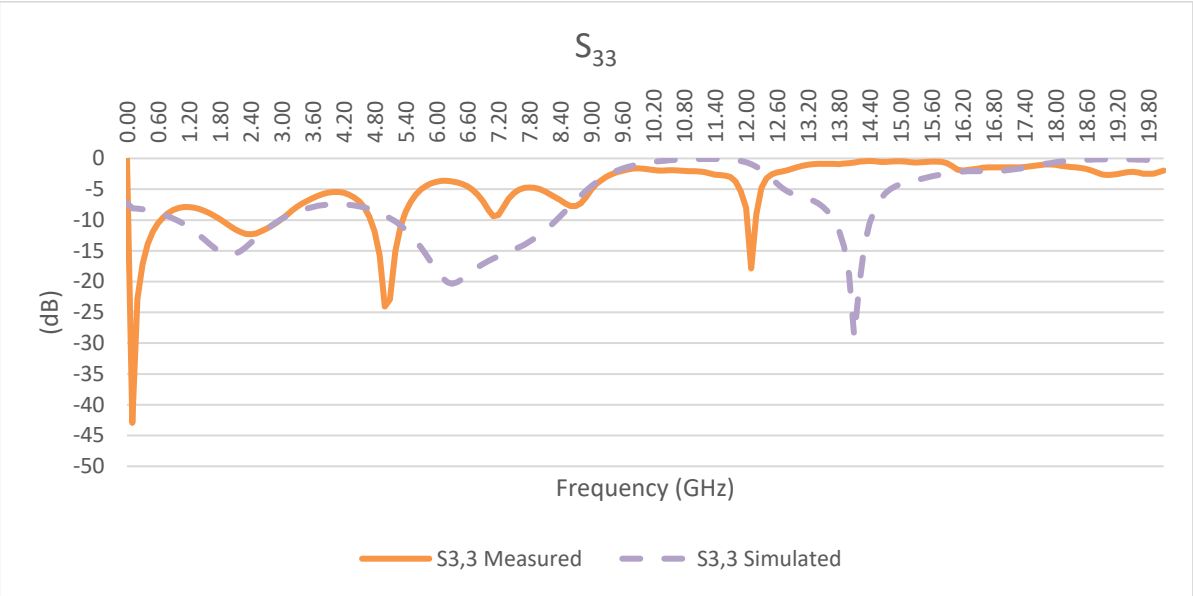

Figure 48: Measured and simulated S_{33} parameters of the filter only prototype.

The simulated results for S_{12}, shown in Figure 50, have very defined frequencies that were to be filtered out at 11.6GHz and 17.4GHz. The measured results follow the simulated results until the first harmonic is to be filtered out. The simulation shows that the first harmonic is centered at 11.6GHz, but the measured results show band stop centered at 10.8GHz. The simulation and measured results do not match between the first and second stop frequencies either. The second stop band for the measured and simulated results are at 16.2GHz and 17.4GHz, respectively.

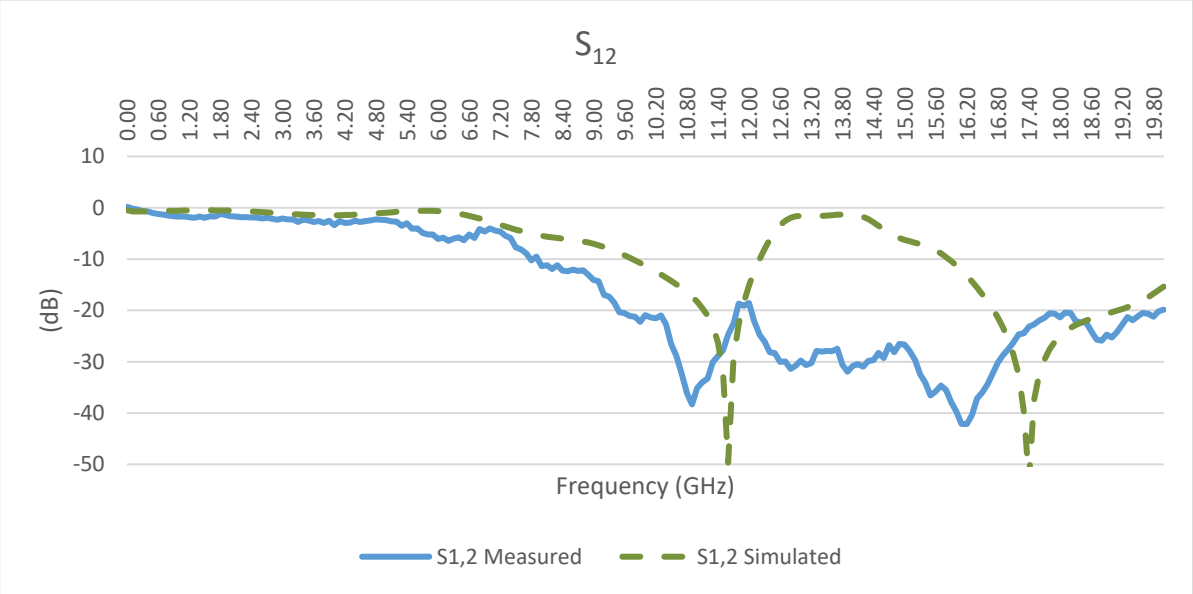

Figure 49: Measured and simulated S_{12} parameters of the filter only prototype.

The results from the S_{34}, shown in Figure 51, match those from S_{12} quite well, suggesting that there is good symmetry in the design between the two halves of the filter.

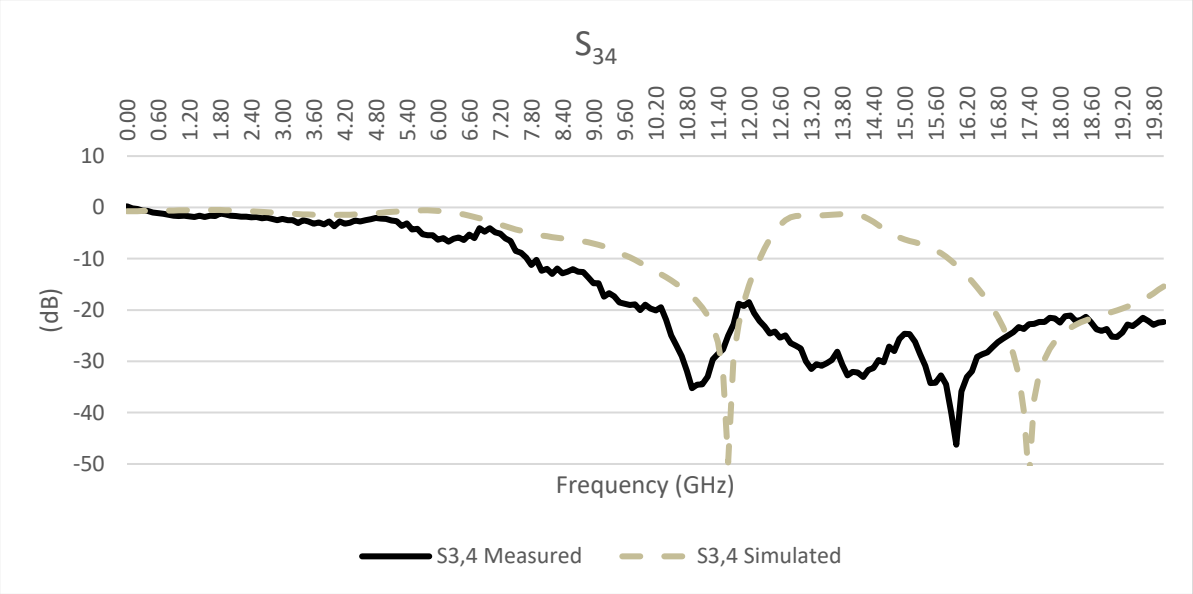

Figure 50: Measured and simulated S_{34} parameters of the filter only prototype.

The simulated results for S_{14}, shown in Figure 52, show that the frequencies of 0Hz, 11.6 and 17.4GHz should be filtered out. The simulated and measured results look similar around 0Hz. The measured results do not match the undesired frequencies of 11.6GHz and 17.4GHz. Instead the measured results filter out around 9.6GHz and 12.8GHz are the minimum.

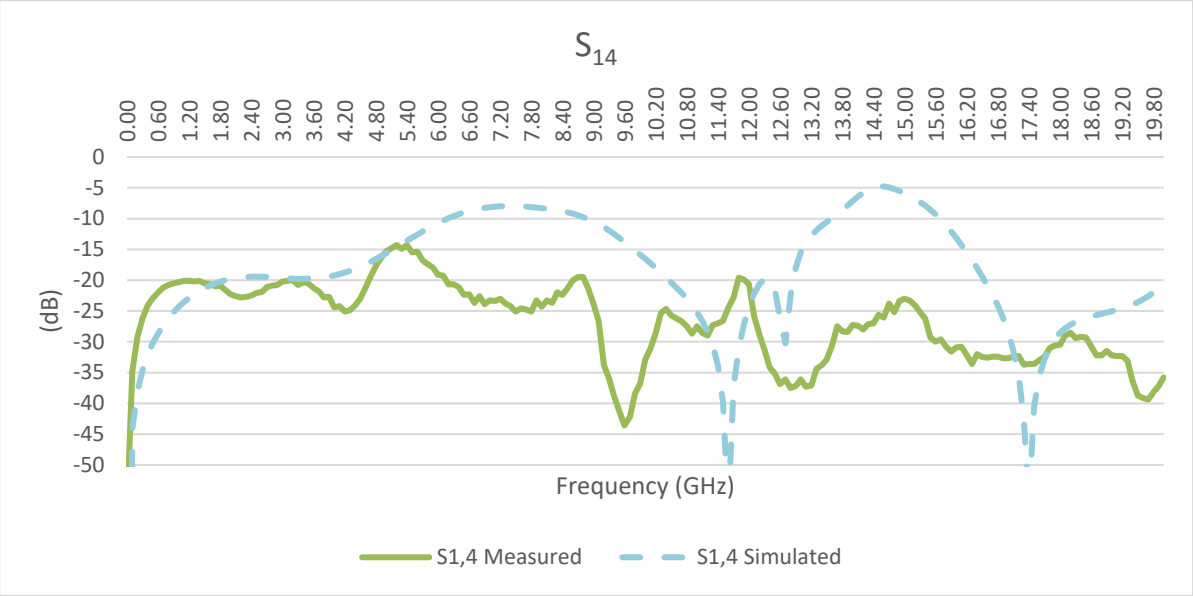

Figure 51: Measured and simulated S_{14} parameters of the filter only prototype.

The results from the S_{32}, shown in Figure 53, match those from S_{14} in the general shape. There are a few more filtered out frequencies than required, and the trend of the attenuation at many frequencies is noticeably different. This suggests that there is less uniformity between two halves of the filter.

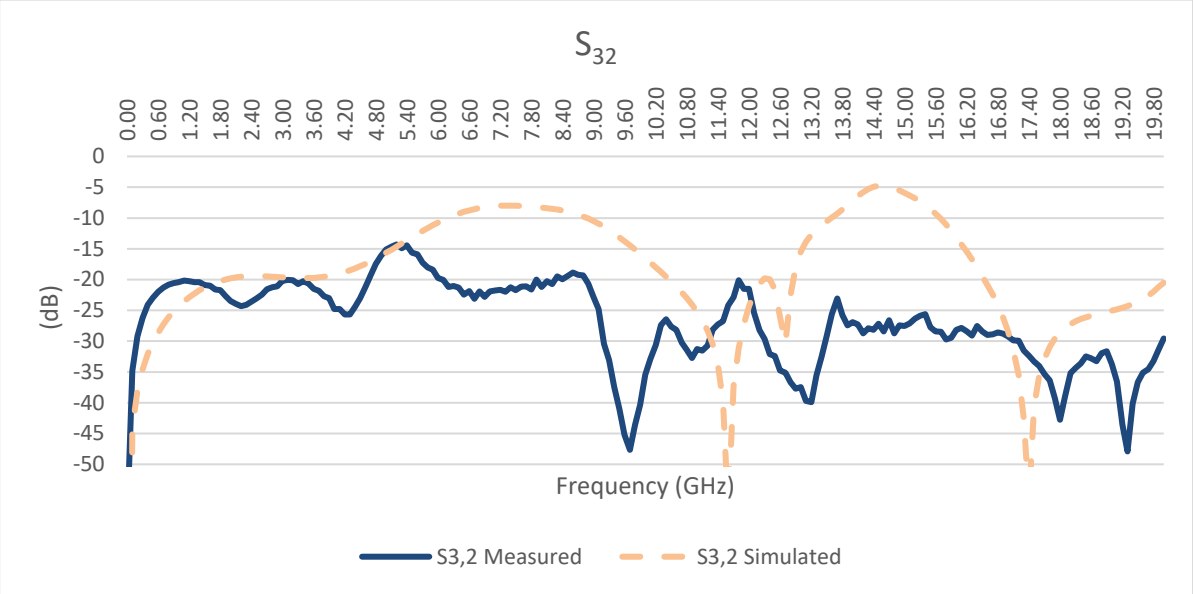

Figure 52: Measured and simulated S_{32} parameters of the filter only prototype.

When comparing the simulated and the measured results, they are quite similar.

b. Rectifier Results

i. Simulation results

Through simulation it was learned that the signals that would need to be passed through the rectifiers would need to be 180° out of phase. This confirms what other researchers have used as well for a dual diode rectifier [10]. This can be seen in the differences between Figures 54 and 55. In Figures 54 and 55, the source of the two signals are placed on Port 1 and Port 3. These two ports correspond to "1" and "3" in Figure 12. In Figures 54 and 55, P1 and P2 are probes that were placed on the output of the simulated rectifier as seen on the right side of Figure 56. In Figure 56 the signal sources were subjected to the rectifier at "1" and "3". The "R_{load}" for the simulation was 135Ω. The 135Ω load was determined in the diode analysis, using Figure 19. The signals were generated using a 5.8GHz transient signal with an amplitude of 6V. In Figure 56 the signal sourced at "1" was given a time delay of 0.086207ns. The time delay was calculated

to be the delay in which a signal needed to achieve 180^{o} phase shift. The time delay was needed since CST software would only accept a time delay of one signal relative to the other, and not just a phase difference between two signals.

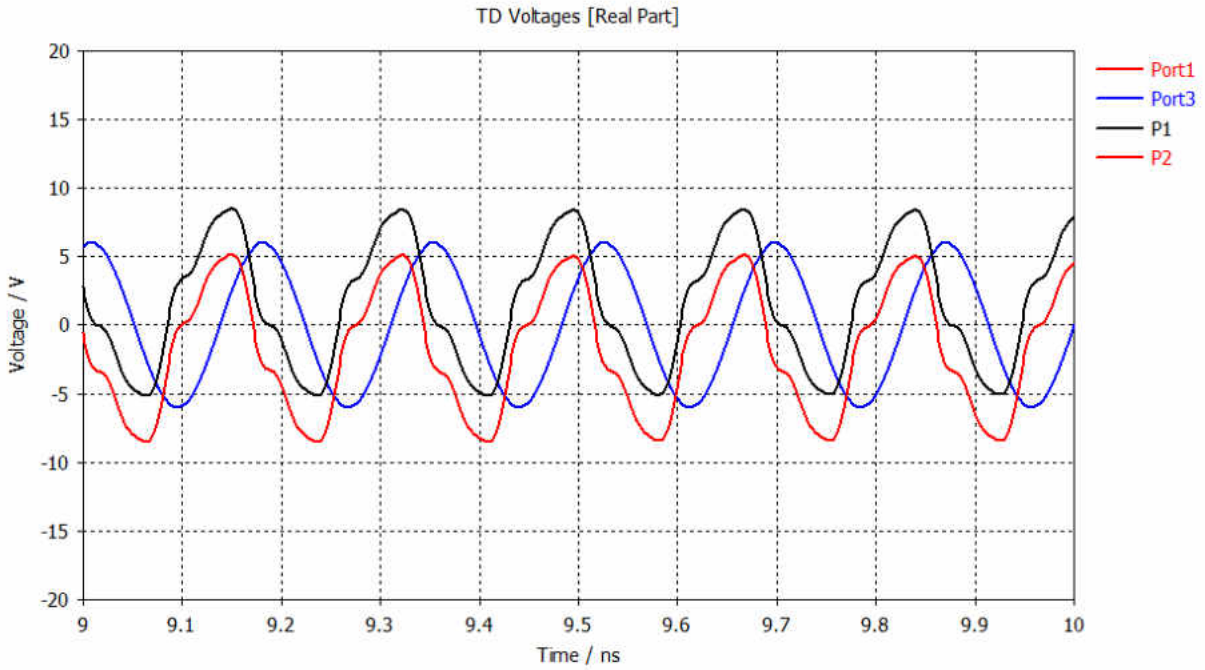

Figure 53: When inputs are in phase (dual diode configuration) [12].

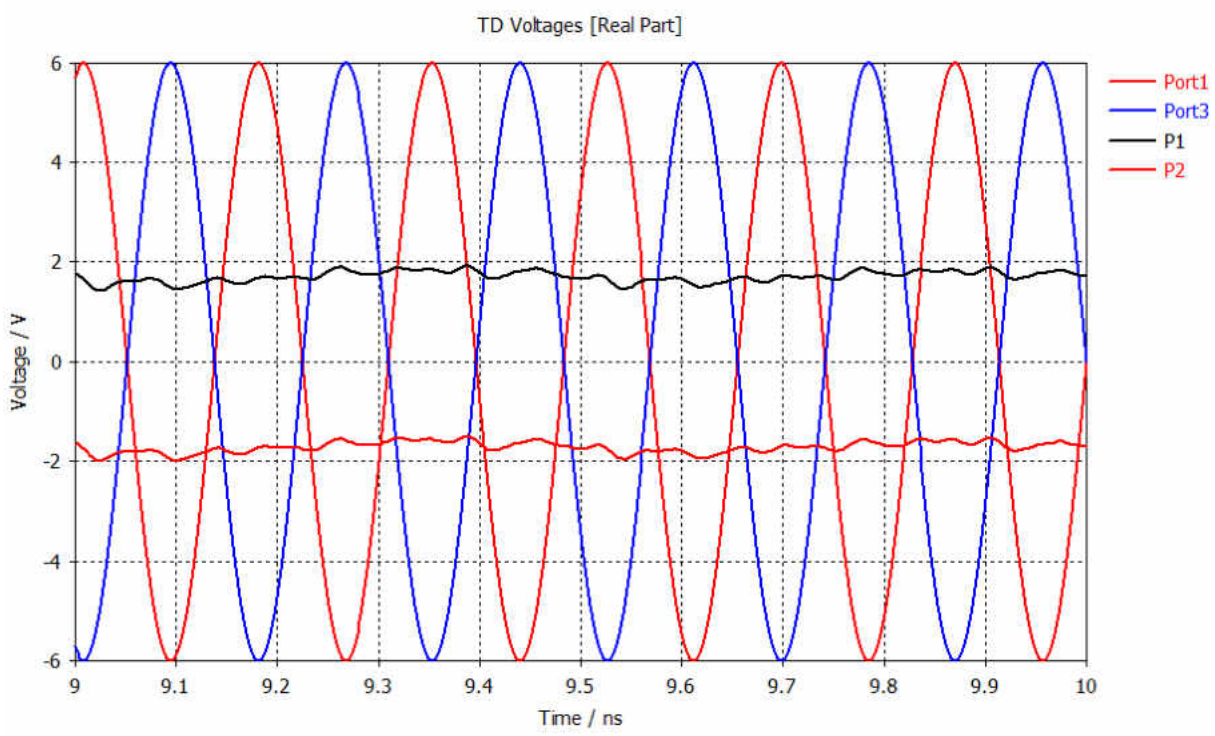

Figure 54: When inputs have phase shift of 180° (dual diode configuration) [12] (Delay = 0.086207ns).

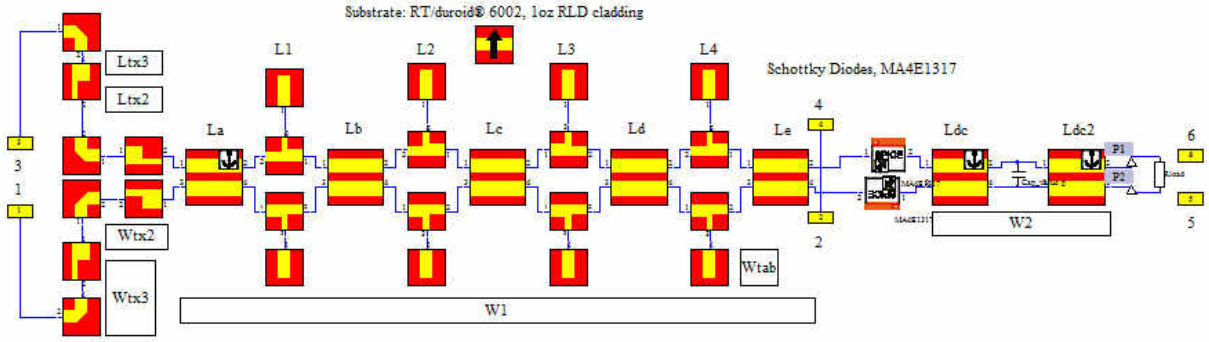

Figure 55: Rectifier simulation used for Rectification simulation [12].

In Figure 57 the same dimensions as the prototype built for laboratory testing was simulated to see what the theoretical results would be. With additional filtering capacitance, the DC output voltage would be about 2.4V with a 3V amplitude signal as the input.

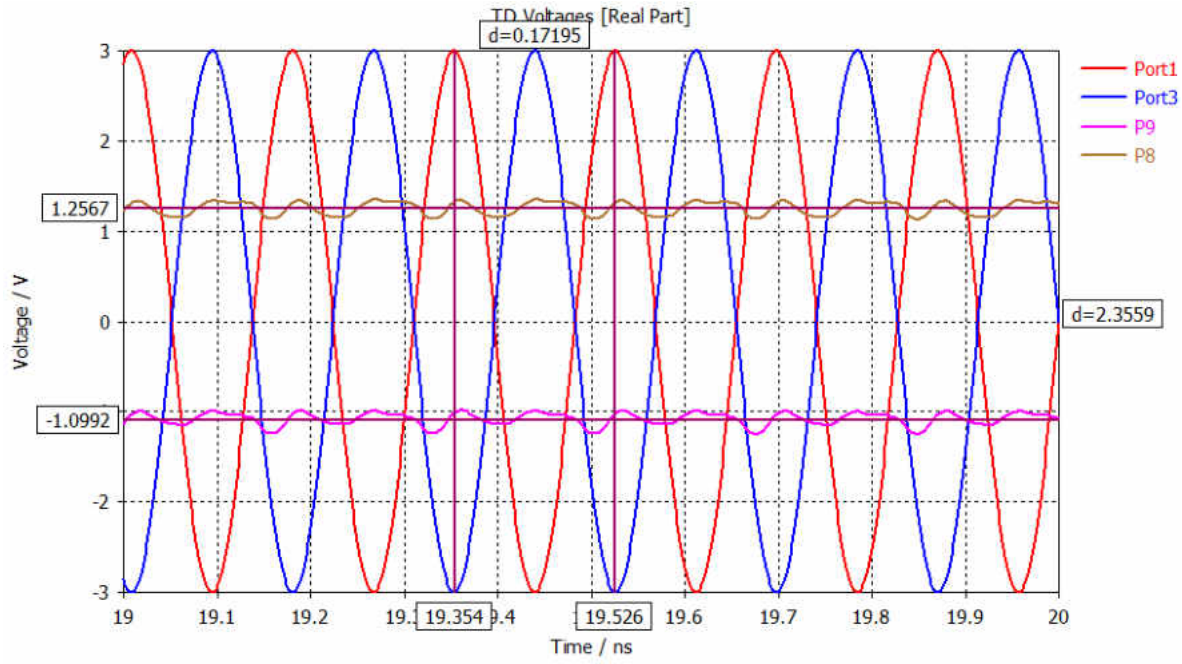

Figure 56: Rectifier simulation of the prototype built for laboratory measurements.

ii. Prototype Measurement Results

Using the hardware manufactured with the ferric chloride produced no results. After analyzing the testing results, only static could be viewed in the results for the prototype measured in the lab. Upon further investigation of the issue, it was discovered that side 1, as seen in Figure 58 by the number "1" written on the substrate of the rectifier, had a large amount of resistance across the diode when biased. The increased resistance is likely to be an internal defect since no other measured diode had similar results. The resistance across side 2, as seen in Figure 58, read as "no load" when the resistance was measured, as expected. The leads of the multi-meter that were used read 0.94Ω when measured.

The rectifier was not tested with two signal generators at 180° out of phase due to a lack of availability and cost of additional testing equipment required.

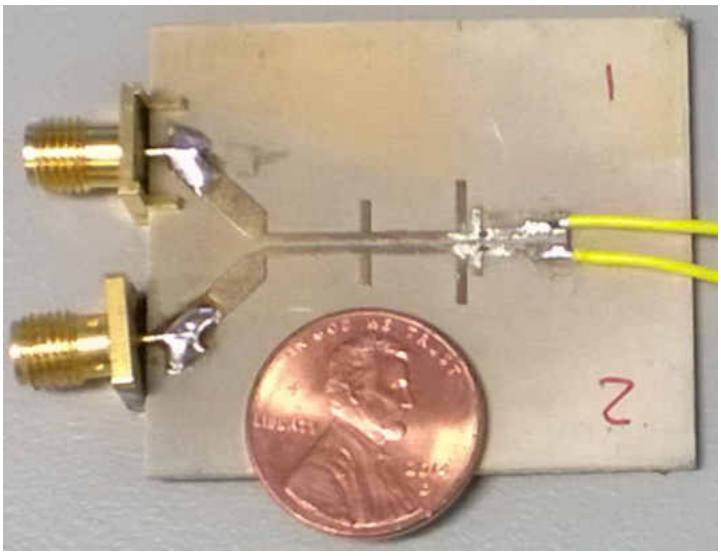

Figure 57: Image of the rectifier prototype in relation to a penny.

Due to the lack of results from the rectifier prototype in Figure 58, a second rectifier was built in an attempt to obtain results. Figure 59 shows the second rectifier tested. The second testing of the rectifier used only one half of the rectifier design in order to attempt to reduce the complexity of the rectifier. In the second rectifier, some parts of the copper on the ground trace was removed during the etching process. Copper traces were added in an effort to make the ground trace a continuous ground path. The second rectifier used the same test plan as the initial rectifier test. The second prototype rectifier did not produce any measurable results like the first attempt.

Figure 58: Image of the second attempt at the prototype rectifier.

Upon testing the second rectifier the results from testing were the same as the initial rectifier. In an attempt to obtain any results from a rectifier, a third rectifier was built. The third rectifier was used in order to detect rectification. The third rectifier did not have any harmonic filter to suppress the harmonic oscillations created by the Schottky diodes. The third rectifier can be seen in Figure 60.

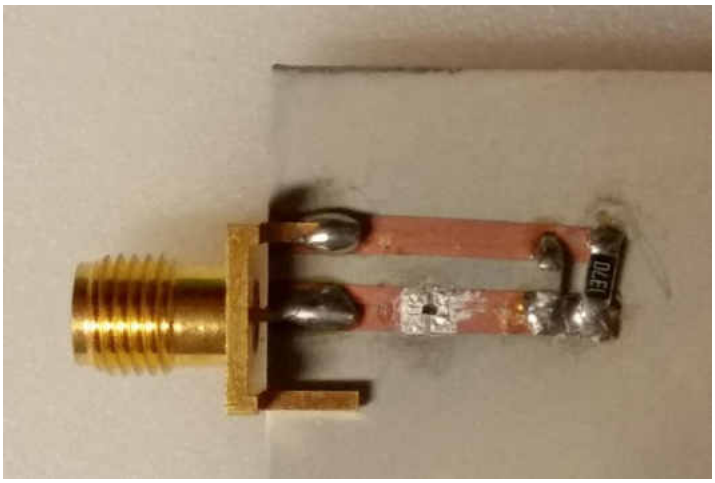

Figure 59: Image of the third attempt at the prototype rectifier.

A third attempt to receive results was done using just a diode placed on a copper trace attached with the same silver epoxy. The diode was again placed in series with the signal

generator output to see if the issue was with the rectifier filter. This third attempt was a quick project and did not involve exact measurements on the trace widths. This rectifier attempt also did not produce any measurable results.

c. DC-to-DC Converter

The efficiency curves for the LTC3115-1 buck/boost converter can be viewed in Figure 61 with the output loads of 0.5A and 1A. The converter efficiency ranged from 80% to 95% efficient for the 0.5A load. The manufacturer does not provide example efficiency curves with a wide input range and an output voltage of 9V. The converter efficiency ranged from 60% to 93.5% efficient for the 1A load. The converter was designed to turn on at 3.03V, so there is no efficiency for the 2V input voltage. The converter was not stable for the input voltage range of 3-6V for the 1A load. The instability can be seen in the graph of the output voltage ripple, Figure 62. The output voltage ripple is very high from 5V–8V due to the converter attempting to shut down so the voltage across the output capacitor is oscillating about 1V–2V. This was due to thermal issues, which is described in further detail in the conclusions. As a result of the thermal issues, recording any results from 2V–5V was impossible with a load of 1A or greater. For the same thermal issues, the converter was also unstable while testing at a load of 2A and 2.25A, this prevented any results to be gathered at any voltages range for loads greater than 1A. Figure 63 shows the measured results of the voltage ripple at two different loads. Figure 63 shows that the converter has a difficulty of maintaining a constant voltage near the transition point between the buck and boost converter. Since the LTC3115 does not have an external input for the transition between the buck and boost modes, the exact transition or hysteresis of the transition is not known. The Converter

handles this operation internally based on the input voltage, output voltage, feedback line and the voltage compensation network.

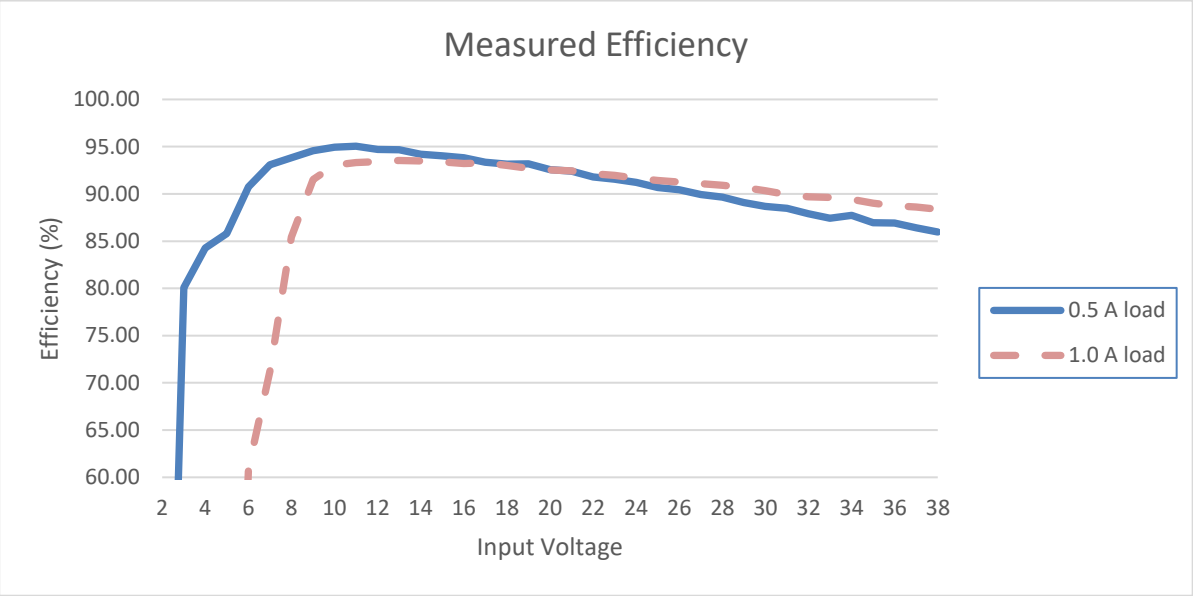

Figure 60: Measured efficiency of the LTC3115-1 buck/boost converter.

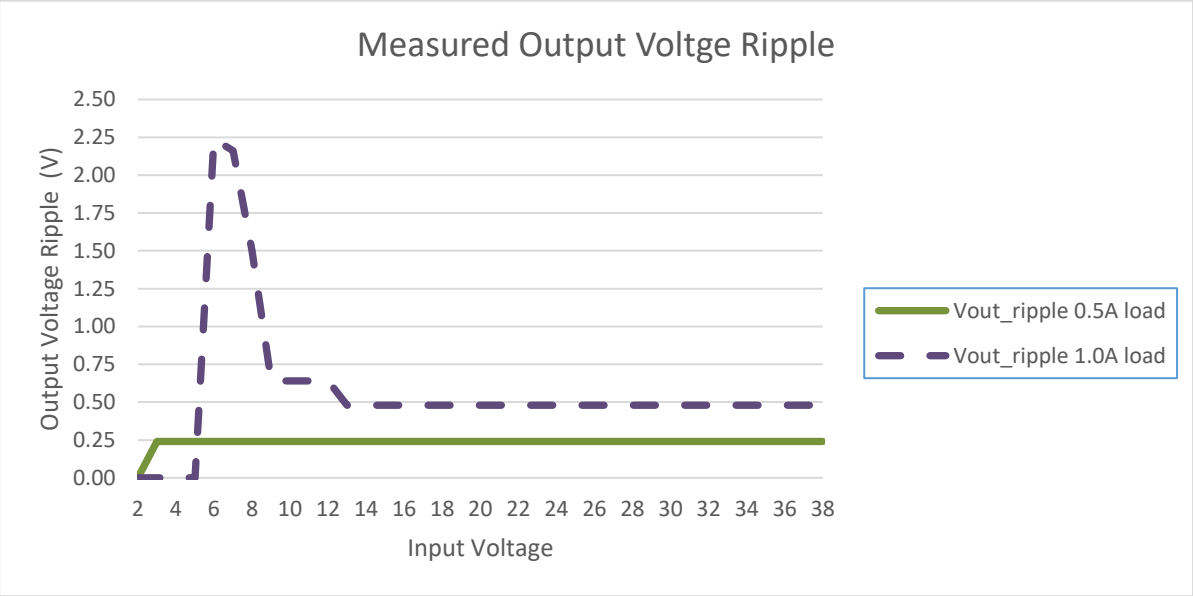

Figure 61: Measured voltage ripple on the output of the LTC3115-1 buck/boost converter.

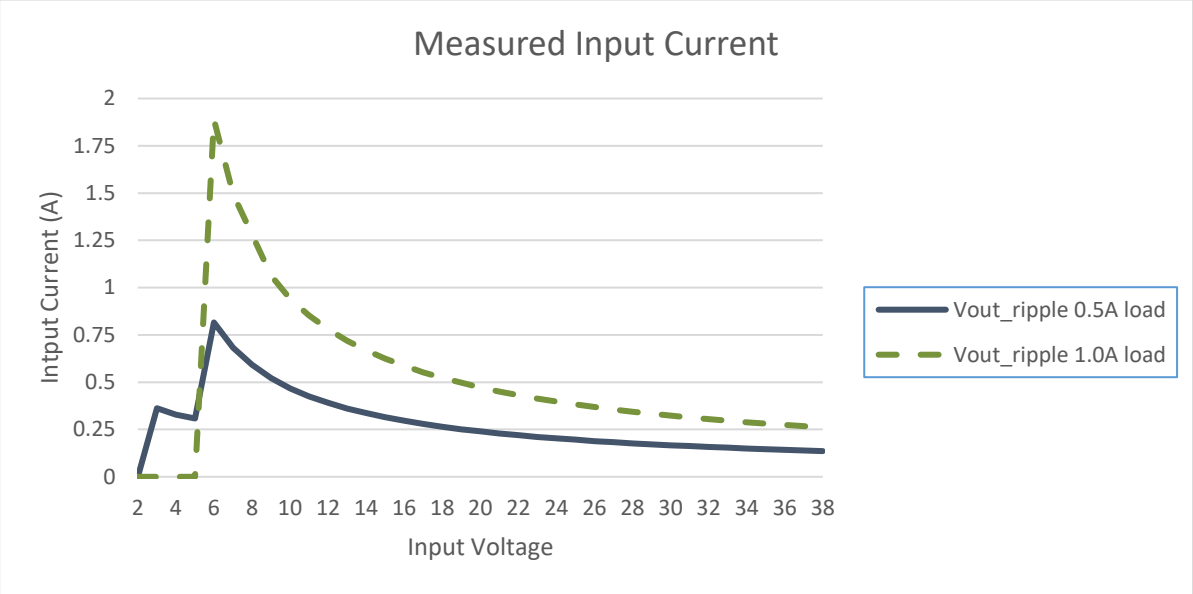

Figure 62: Measured input current on the output of the LTC3115-1 buck/boost converter.

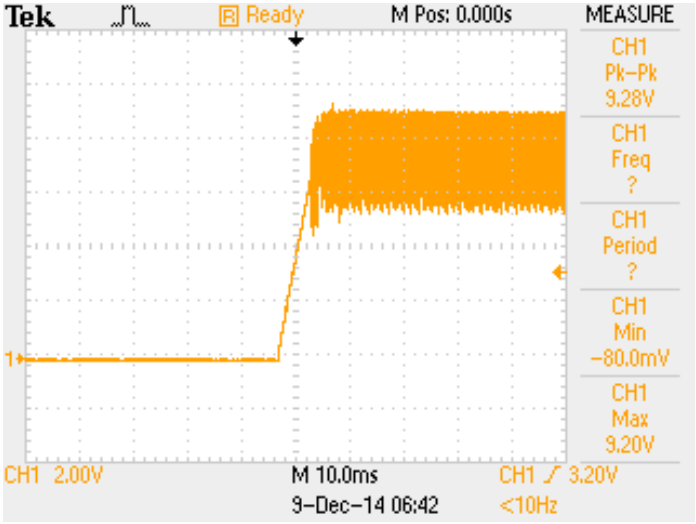

Figure 63: Oscilloscope's capture of an instance of the thermal shutdown and zoomed into the leading edge of the output voltage waveform. The converter was operating with an input voltage of 14V and a load current of 1A.

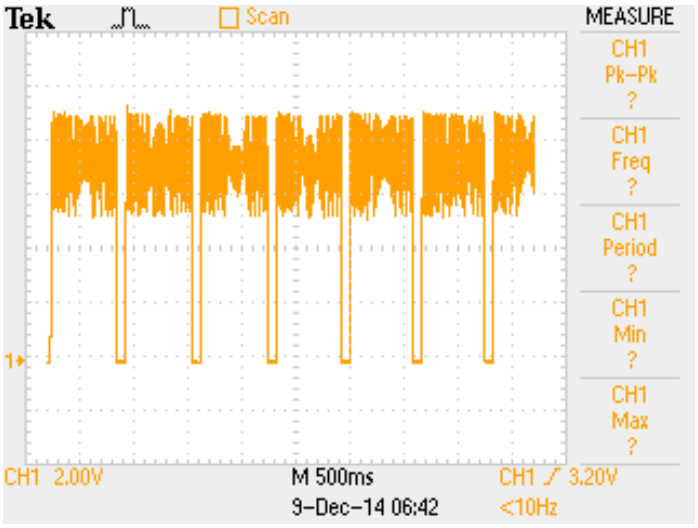

Figure 64: Oscilloscope's capture of an instance of the thermal shutdown and zoomed to show multiple periods of the output voltage waveform. The converter was operating with an input voltage of 14V and a load current of 1A.

The output voltage ripple of the 0.5A load was constant at 240mV peak-to-peak. Across all input voltages and output current levels, the converter was designed to have less than a +/- 5% change in output voltage. Assuming the output voltage is centered at 9V, the maximum ripple could be 900mV peak to peak and the output voltage would still be within the design criteria. The output voltage ripple of the 1A load was not constant throughout the input voltage range. The output voltage ripple was about 640mV peak-to-peak with an input of 9V. The ripple increased as the input voltage was reduced and at an input of 6V the ripple was 2.24V peak-to-peak. This was caused by the instability of the converter due to the thermal characteristics of the PCB. The output voltage ripple was about 480mV peak to peak with an input of greater than 9V and a load of 1A.

The measured current and voltage results of the two loads can be viewed in Figures 66 and 67, respectively. On Figures 66 and 67, a slight change in the ramp rate can be seen from three to 5V. This same ramp rate can be seen in the efficiency graph in Figure 61. This ramp rate

change is due to a setting on the LCT3115 called burst mode. In burst mode, the converter attempts to increase the efficiency of the device during light load conditions. In Figure 61 this is quite evident by the efficiencies measured at 3V to 5V input not matching the ramp rate after 5V. The measured data recorded from the testing of the LTC3115-1 buck/boost converter can be viewed in Tables 5 and 6 of Appendix F.

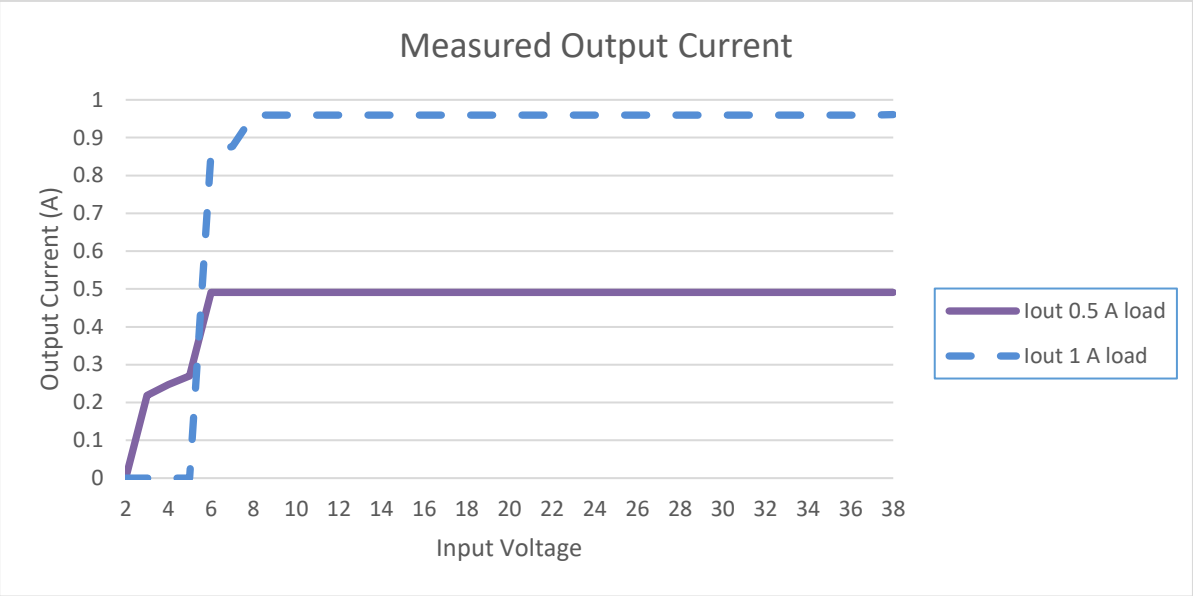

Figure 65: Measured output current of the LTC3115-1 buck/boost converter.

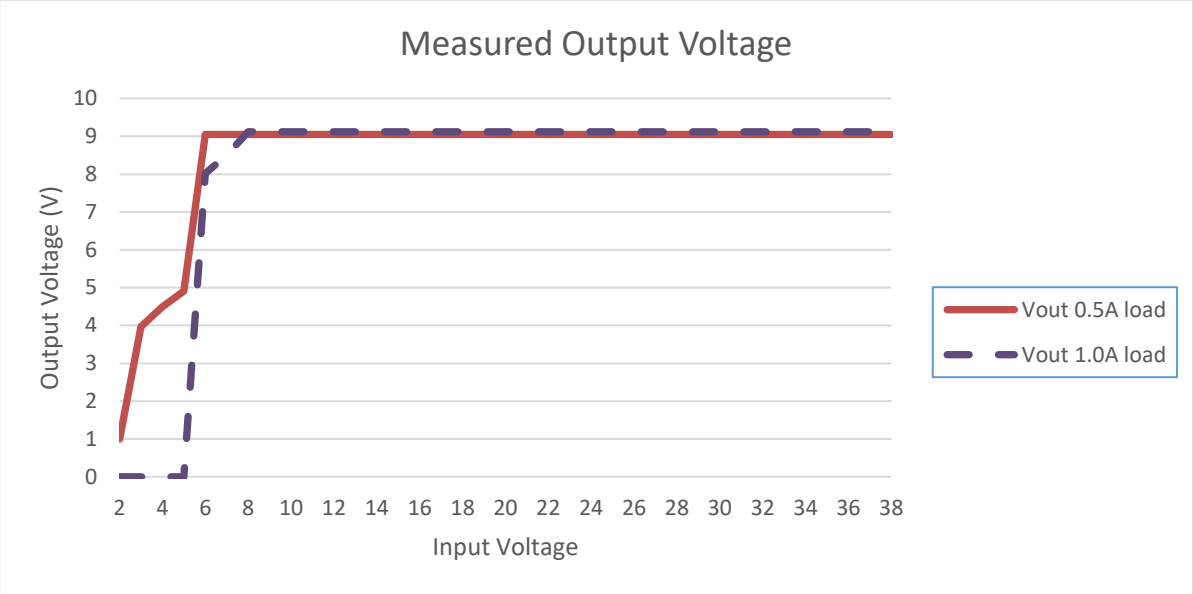

Figure 66: Measured output voltage of the LTC3115-1 buck/boost converter.

Fig. 68 show the voltage ripple values during the steady-state of the ripple. The images taken can be seen in Figures 68 and 69. The non-steady-state ripple areas are times in which the output voltage was being shut down due to thermal issues, images of this region can be seen in Figures 64 and 65. These images also show that the V_{out} average stayed very close to 9V, which was highly typical of the converter while it was loaded. When the converter was unloaded, the output would rise to about 9.2V. The nominal voltage ripple of the 0.5A load and 1A load can be seen in Figures 65 and 68, respectively.

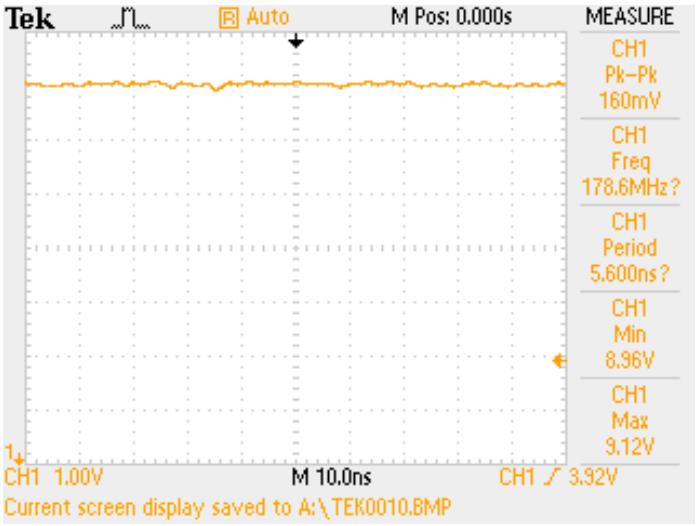

Figure 67: DC output showing the minimal output voltage ripple, the image shows 160mV peak to peak ripple, but the average was 240mV. V_{in} was 14V and I_{out} was 0.5A.

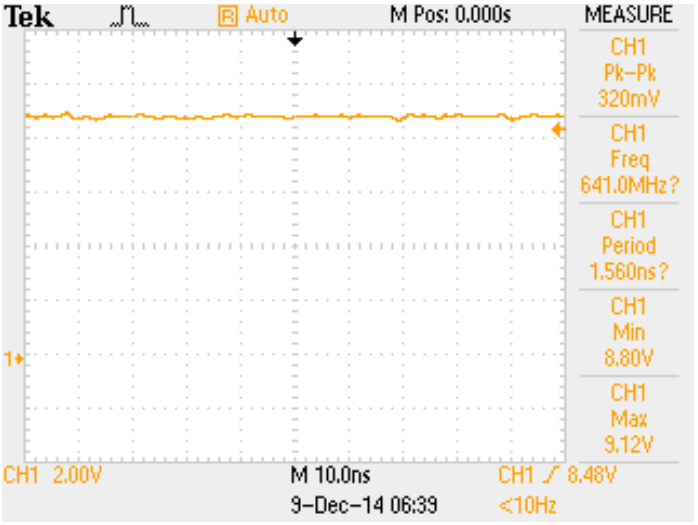

Figure 68: DC output showing the minimal output voltage ripple, the image shows 160mV peak to peak ripple, but the average was 480mV. V_{in} was 14V and I_{out} was 1.0A.

VII. CONCLUSIONS

The process of designing, analyzing and prototyping a rectenna and its array should not be underestimated in difficulty. The knowledge needed to complete a rectenna design is a large time and resource investment. Though this project of designing and building a rectenna, rectenna array and DC converter has not all been successfully completed, foundational knowledge to do so has been obtained.

The concept of building a rectenna is not a new idea, but the idea to attach a DC-to-DC converter to a SHF rectifier is quite new. The process of integrating DC converters into the rectenna and rectenna arrays design in the future will become a normal practice. The lack of a long-term space experiment of MWPT, the practicality, cost effectiveness and safety of the satellite, all provide reasons as to why a DC convertor should be employed on-board for future MWPT test experiments that are carried out on space or on the Earth. Integrating the DC converter should be done at the system level of the rectenna array. The efficiency breakdown of the rectenna array system should be done piece by piece so that it can be compared with previous and future works. The efficiency should be broken down in the following categories: single element rectenna, rectenna array, DC converter, and rectenna array system.

a. Review of Methodology

The following will discuss the success of each task laid out in the methodology.

Task 1: complete a literature review to understand previous work on MWPT systems. Through the literature review, it was discovered that many researchers had attempted new reception techniques to increase the efficiency of MWPT systems. Some researchers focused on the topology of the diodes used in rectification, design of the arrays, the HRFs, and many more ideas not presented here. The literature review failed to produce prior work that integrated a MWPT into a long-term space experiment to serve as a proof of concept for SSP. Prior works have conducted MWPT experiments in space. However, no prior work mentions the thought of integrating the improved rectennas with a receiving spacecraft. The present work is about system integration, especially the idea of using a DC converter after the output of the rectifier to regulate the voltage for a load specified application. The lack of any mention about system integration of rectennas with a regulator for charging applications in the literature was surprising.

Task 2: design and verify the rectifier circuit. Several rectifying topologies were considered to determine the best conversion efficiency. Rectification process efficiency goal was set at 70%. The design of the rectifiers was a challenge and a struggle. The design of the rectifier and filter was an easy process once it was understood how to use the CST software [12] effectively. The testing of the rectifiers was quick, other than the struggle to understand why there were no measured results. The rectifying process conversion efficiency was tested, but achieved no results due to no functioning rectifiers.

Task 3: involved the design of the PMAD or regulator. This task was completed and improved with added input to the design after the first version of the buck/boost controller was built and tested. The improvements are discussed later in this Chapter.

Task 4: focused on designing the rectenna array. The design of the array was not fully completed. This was due to the unknown voltage and power outputs of the individual rectennas. A sample array was designed using the assumptions from a reference by Strassner and Chang [2], which uses a similar rectenna design.

b. Simulation Results

Simulation results are not always a perfect representation of reality. However, when testing experiments with real components there are many variables that will impact the experiments. Simulations are meant to predict the results of the actual experiment. While the simulation results of the rectifier were not perfect, they appeared to be capable of delivering measurable results. The filter results, as seen in Figures 48 – 53, appeared to be satisfactory. For results to be satisfactory the results should match the design rules seen in Table 3. In Table 3, a target value of 0 represents that the signal at the specified frequency will not be allowed to pass. In Table 3, a target value of 1 means that the signal at the specified frequency will be allowed to pass. So, when the design rule specifies that a signal frequency should not be passed through a point, in Figures 48 – 53 the graph at that point should be as low as possible. Then when the design rule specifies that a signal frequency should be passed through a point, in Figures 48 – 53 the graph at that point should be close to 0 dB.

The rectifier simulation results of CST Design Studio software did not show conversion efficiencies in the 90% range, but it is believed, with more time and experimentation, that a better conversion efficiency could be achieved. The simulated input and output of the rectifier can be seen in Figure 55. The simulation results could not produce an efficiency sine the

measurements did not include a current waveform and the power input was not known. The rectifier simulation results were constrained because the filter had to be designed so that it could be tested. The two features designed for testing that are the most noticeable are the 2 stubs that the SMA connectors are directly attached to in Figure 58. In Figure 12, the blocks above the box shown as “W” is the actual filter and rectifier and the rest was added in order to be able to test the prototypes. If the filter design was designed without these testing stubs and the stubs were added to the rectifier after simulations were complete, then the rectifier performance would be even worse in simulations and in measured results.

c. Prototype Results

The ferric chloride etchings of the rectifier and filter only designs were meant to provide a proof of concept. Since the manufacturing of the filter was a proof of concept, the frequency shift of the filtered results from the expected 5.8GHz to the measured results around 5GHz were pleasing. This experiment is the first time the author has had with SHF devices and their manufacturing. The author does not see significance in the lack of results. The lack of results is believed by the author to be a result of manufacturing errors and loose tolerances. It is believed that if the prototypes were manufactured professionally, then better results would have been obtained. However, due to cost and lead-time the prototypes were made in house and manually. These conclusions are based on the fact that the filter showed reasonable results but none of the rectifiers gave measurable results. The author also believes that this design is still valid since a similar design was used and published by Chang et al. [10]. The lessons learned from building these prototypes by hand and the experiences from testing the prototypes at the University of North Dakota provided invaluable knowledge that will be used in future designs. The importance

of the converter testing is a great step and can be used to design a more efficient rectenna array. This is believed as a result of prior researchers being able to produce novel rectenna designs, but prior researchers have seldom suggested the idea to regulate and contain the captured energy into a storage device.

i. Rectifier

The three different rectifier prototypes can be considered a failure since they did not produce any results.

Possible reasons that caused the lack of results from the rectifier:

Manufacturing Defects, each prototype was traced out by hand and then covered in ink to prevent the etching process and then etched away by the ferric chloride solution. The prototypes took several days and multiple tries to get the diodes cured properly without shorting around the diodes due to excess conductive epoxy.

Manufacturing Accuracies, other manufacturing defects on all three versions of prototypes included mismatching of the sizes of the copper traces due to the simple fact the prototypes were etched and produced by hand.

Diode Misplacement, the lack of results from the rectifier may also be due to inadequate bonding of the diode to the copper. Even with extreme caution and checking the conductivity of the first rectifier, one of the diodes did not fully block the signal of a digital multi-meter when reverse biased.

Testing Procedure, another possible reason in which the rectifier did not produce results could be that the testing method was flawed in some way. This could be due to testing a single side of the rectifier at a time and not having 2 input sources to the rectifier. This could be accomplished by a Signal Phase shifter and power splitter or it could be accomplished by utilizing 2 antennas attached to the rectifier.

Testing Features of the Rectifier, the SMA connector and the attachment point were not simulated and could be a source of the testing results failure. This could be causing an additional Resistive, Inductive, and Capacitive (RLC) network that is impacting the performance of the rectifier.

ii. Rectifier Filter

The design was optimized before the impedance transformers were added. The S-parameter results from a single filter could have been optimized much better to obtain better results. However, this may not have been a great advantage since the filter would then not be an exact copy of the filter used in the rectifier prototype. The results were quite close to the simulated results. The error of the frequency shift is likely caused by 2 driving factors:

- The un simulated parts of the filter design that were used in testing, such as the SMA connectors and the stubs used to attach them.
- Manufacturing inaccuracies of the filter due to production method

iii. DC-to-DC Converter

The efficiency results of the converter were within the anticipated range. The converter even met and exceeded the capability of 95% efficiency stated on the datasheet [25]. The aspect

of the converter testing that was unexpected and surprising was the significance of the thermal properties of the PCB. The thermal properties of the converter design were not expected to become an issue until the converter was loaded to about 2 Amps; since the LTC3115-1 datasheet says that the current output limit is 2.25A [25]. However, the thermal properties of the converter were barely able to handle a load of 1A. Thermal issues probably negatively impacted the efficiency of the converter when loaded at 0.5A and input voltages above 18V.

The efficiency of the 1A load current and high voltage input of the 0.5A load current should be improved with additional heat dissipation properties which is best described by the LTC3115-1 datasheet [25]: “Careful consideration must be given to the thermal environment of the Integrated Circuit (IC) in order to optimize efficiency and ensure that the LTC3115-1 is able to provide its full-rated output current.” More consideration should have been placed on the thermal properties to improve the converter efficiency. The efficiency of the converter system could also be increased if the input to output voltage ratios were approximately one [25].

The output voltage ripple was satisfactory for the 0.5A load. The output voltage ripple was unsatisfactory for the 1A load while the chip was boosting (when the input voltage is below 10V). The ripple voltage above 9V was within the anticipated tolerance of 0.5V. The ripple could have been reduced with a higher output capacitance. However, the Thermal issues of the PCB design still would have limited the output voltage regulation. High thermal parts were attempted to be used where feasible, meaning most parts were rated above 75^{o}C. While some were rated over 100^{o}C. The Industry standard of the thermal properties for FR4 is greater than 125^{o}C.

Upon testing the converter again once the thermal issues have been corrected, one will be able to then decide if the output capacitor needs to be increased or if an additional filter needs to be placed in series with the DC output.

One cause of the poor performance was determined not to be the burst mode operation. In one of the converters the PWM pin was tied to V_{cc} so that the burst mode would not operate. This actually caused the converter to preform worse. The modified converter actually began its thermal shutdown at an input of 8V, where it was previously shutting down around 6V. Additionally, the burst mode would not impact the output and drive the output into a light load condition until the input was 3.89V at which the converter would attempt to operate in a light load condition. If the converter was in the burst mode and the load resistance was low enough so that the current demand of the output exceeded the capabilities of the burst mode, then the thermal shutdown condition could be an issue due to overdriving the converter.

The performance of the DC-to-DC converter could be drastically improved with a PCB redesign. Things that should be addressed in the redesign are the thermal properties. Increasing the thermal dissipation of the buck/boost converter will allow it to handle additional currents above 1A. To fix the thermal properties in the next revision of the PCB, the ground pad for the LTC3115-1 buck/boost converter should be made up of as many vias as possible. The vias should connect the ground pad to the ground plane on the bottom side of the board. Additional ground spaces should be placed on the topside of the board as well to create additional heat dissipation capabilities. A proposed redesign should look like Figures 70-72. If ideas proposed above, do not fix the thermal shut down issues then a physical heat sink should be attached to the copper top

and copper bottom layers just above the LT DC converter. If a heat sink just connected to the copper planes near the converter does not work, then a heat sink should be attached to the top of the LT DC converter device with thermal paste between the heat sink and the converter for maximum surface contact between the converter and the heat sink.

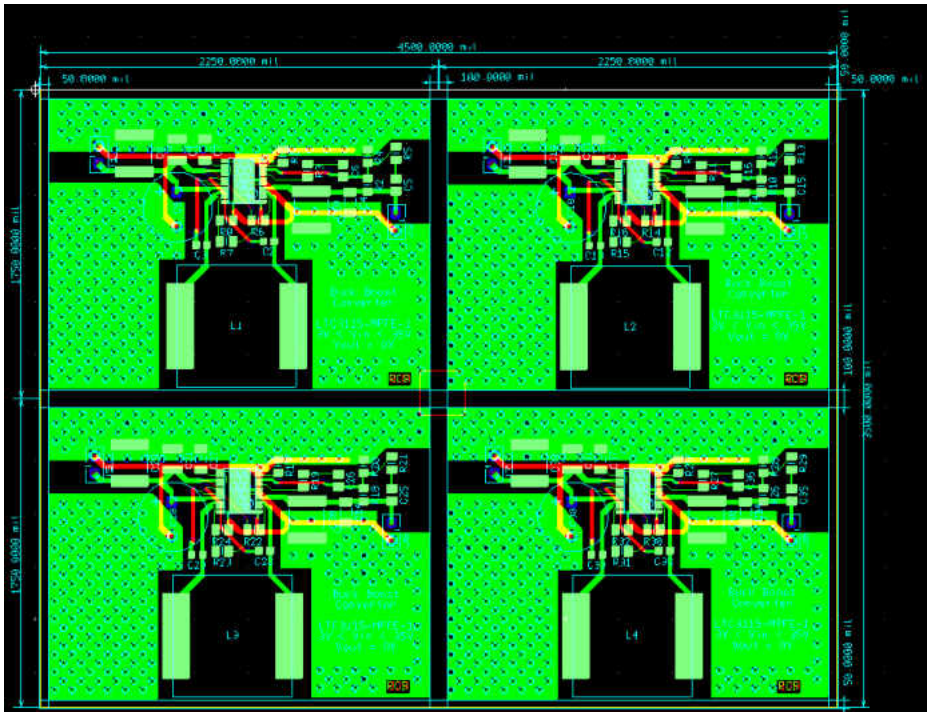

Figure 69: Revised DC converter PCB showing four converters on a single PCB. The ground plane is not shown to allow for more detail on the copper top and the on the copper bottom.

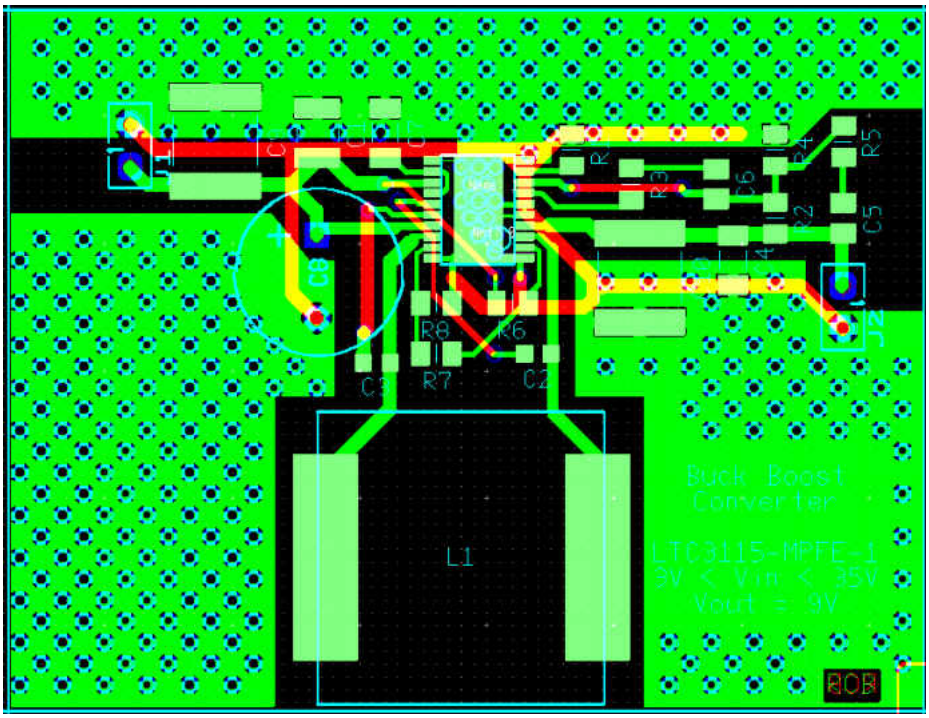

Figure 70: Revised DC converter PCB showing a single converter. The ground plane is not shown to allow for more detail on the copper top and the on the copper bottom.

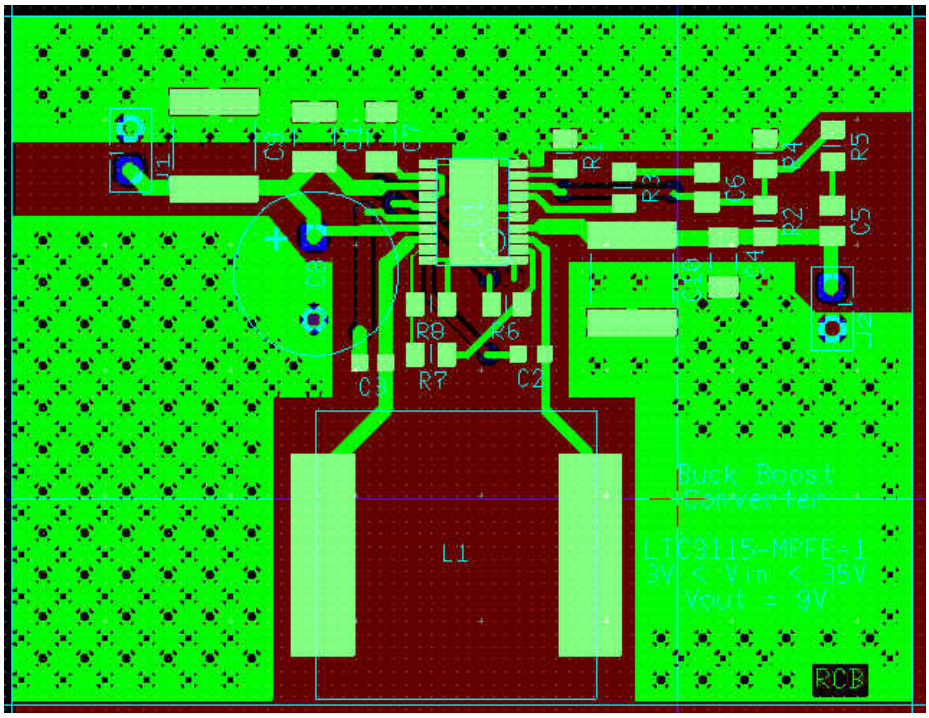

Figure 71: Revised DC converter PCB showing a single converter. The ground plane is shown as the dark red color to show how it would cover the entire underside of the PCB.

d. Future Research Areas

There is a great need and vast number of topics to continue the research on space solar power and microwave power transmission. Some of the areas that have been discussed and are open to further research include, but are not limited to, the rectifier design, the rectenna array design, the DC-to-DC converter, and space qualified parts and materials.

i. Rectifier Design

A study should be completed to investigate more available Schottky diodes on the market to determine if there is a better alternative to the MA4E1317 diode. A study should be conducted on using two capacitors on the output of the diodes of the rectifier. The two capacitors should have different capacitance values in order to filter out different frequencies. The one closer to the load should have a larger capacitance, between 100pF and 330pF. This capacitor would short out many more of the lower frequency components of the rectified output. In general, as the capacitance value of the filter capacitor, the output voltage ripple will decrease. This capacitor should not be too large since as the capacitance increases, the less the capacitor will fully charge. If the capacitor is not able to charge fully, then the output voltage will drop. The capacitor closer to the diodes should be between 1pF and 10pF to respond to the high frequency components that make it through the diodes in the rectification process. By having these two capacitors, design may allow for more energy to be converted, due to less energy remaining in the form of an oscillating voltage.

ii. Rectenna Array Design

A complete rectenna array design study should be conducted in the future. The study should extend the knowledge of the work presented in [10, 18, 24]. To expand the previous works mentioned, the scope of work should include part or all of the following suggestions.

All suggestions are to use a fixed amount of area, preferably incorporating three or more rectenna elements contained in the specified area, to compare system efficiencies. The first suggestion is to compare the efficiency of combining rectenna elements on a single substrate using shunt diode and the three different interconnection methods of series, parallel and cascaded. These results should also be compared to the results of a single element to show the inefficiencies of array interconnection. The results of this suggestion should be found to be comparable to the results found by Sinohara and Matsumoto in [24] and Ren and Chang in [10]. The second suggestion is to implement the first suggestion using the dual diode rectifier topology. These results should be comparable to those found by Ren and Chang in [10]. The last suggestion is to compare a shunt and dual diode design by creating a 6+ element rectenna array using the knowledge gained from the previous two experiments by using the most optimal rectenna array design and then integrate the rectenna array with a DC-to DC-converter. The information gained in the third suggestion will be completely novel to the MWPT and SSP fields. The experience gained will be used to determine if the dual diode rectenna array combined with the DC converter can be more efficient than the shunt diode rectenna array combined with a DC converter.

iii. DC-to-DC Converter

Future designs should evaluate and implement an input voltage clamp. The input voltage clamp would act like a clipper circuit so that the input voltage cannot exceed the maximum voltage capability of the DC-to-DC converter. This clamp would be necessary on an energy receiving satellite to protect against a stronger than designed for 5.8GHz signal beam

The clamp should be set at 90%-95% of the rated maximum voltage of the converter. In the instance of the LTC3115-1, the input clamp would be recommended to be set at 35V to 38V. Typical voltage clamps use Zener diodes.

iv. Space-Qualified Materials

In a future experiment the same process should be completed with only space-qualified parts. The space-qualified parts should include everything from the converter PCB material to the SMT parts and the type of solder used. A space-hardened equivalent of every part may not be a possibility. One part that may not have an equivalent is the Schottky diode, MA4E1317.

In a future design the MSK5055RH switching voltage regulator by the M.S. Kennedy Corporation should be researched and implemented [35]. This part is completely space qualified so it provides a realistic judgment of the space application capabilities. This part meets the needs in the requirements for the DC-to-DC converter (I_{out}>2A, 3V<V_{in}<30V, and V_{out}=9V). This part is not directly limited by the load current, since the switching path does not contain the load current pass through the device. The efficiency of the MSK5055RH ranges from 76% to 93% depending on the load current [35]. This part should be researched in a future design due to the more complex circuitry that is needed to operate the converter.

APPENDICIES

Appendix A

MATLAB script used in determining values for the DC to DC converter

```
%Calculations for the Buck/Boost converter
%Device calculated for LTC3115-1
%Original Author: Robert Bernaciak 22-May-14

%Modifications Tracker
%Person             Date        Modifications made
%Robert Bernaciak   19-June-14   Mod tracker added
%Robert Bernaciak   09-July-14   added calculations to the
compensation
%   voltage loop

clc;clear all;

%prefixes to convert to specific units
milli=1/1000;    %unit to convert in and out of milli Watts/Volts/Amps
micro=1/1000000;    %unit to convert in and out of micro
Watts/Volts/Amps
pico=micro^2;       %unit to convert in and out of micro
Watts/Volts/Amps
Kilo=1000;      %unit to convert in and out of kilo Watts/Volts/Amps
Mega=1000000;   %unit to convert in and out of Mega Watts/Volts/Amps

%Fixed global values
Vin_max=40;     %(V) max input voltage
Vin_min=3;    %(V) also the set value for the Run Pin to go low
Vout=9;         %(V) voltage desired at output
Vout_min=Vout*(1-0.05); %(V) minimum allowable voltage output
%   (change in 5% allowed)
Vout_max=Vout*(1+0.05); %(V) maximum allowable voltage output
%   (change in 5% allowed)
Iout_max=2.25;  %(A) max output current of the device
Iout_typ=1.875; %(A) based on recommendation in Clyde user manual
Vburst_mode=Vin_min*1.25;   %(V) set the chip into burst mode 25%
above
%   the Vin_min
Vrun_set_point=1.21;   %(V) desired voltage for the Run to go low
Vsync_set_point=0.7;   %(V) point at which the Sync pin will turn on
burst
%   mode
R6R7R8=180*Kilo;    %(Ohms) value of R6+R7+R8 should be set relatively
%   high to reduce power loss through the resistors
Irun_typ=3*micro;   %(A) given by the datasheet
Check=0;        %used to count all of the passing checks
tLow=100*milli*micro;   %(ns) time taken from graphs in LTC3115-1
datasheet
```

```
Cap_V_derating=50; %(given in %) this value is the recommended useable
%   amount of the rated voltage
resistor_tol=1; %(given in %) tolerance of the resistors for the
design



%Find the RLoad for the Clyde Space battery
RLoad=Vout/Iout_typ;%(Ohms), found by taking the output voltage/ the
%   recommended output current by Clyde Space



%%%%%% Selection of R1 %%%%%%
%Calculate the resistor to set switching frequency
R1=47500;   %(Ohms) used to set switching frequency
R1_ptc_min=R1*(1-resistor_tol/100);
R1_ptc_max=R1*(1+resistor_tol/100);
Fsw=35.7/(R1/Kilo)*Mega; %(Hz) switching frequency
Fsw_min=35.7/(R1_ptc_max/Kilo)*Mega;    %(Hz) Min switching frequency
Fsw_max=35.7/(R1_ptc_min/Kilo)*Mega;    %(Hz) Max switching frequency

%power of R1 is purely a guess since there is no RT current or voltage
%   output given in the datasheet
Pr1=Vin_max^2/R1_ptc_min/milli;  %(mW)34.0245

%%%%%% Selection of R6, R7, R8 %%%%%%
%Calculate the resistors for the Divider network of Run and SYNC pins

%R8=Vrun_set_point/Vin_min*(R6+R7)/(1-Vrun_set_point/Vin_min)
%coefficients for R8 =k*(R6+R7)
kR8=(Vsync_set_point/Vburst_mode)/(1-Vsync_set_point/Vburst_mode);

%R6=Vrun_set_point/Vin_min*(R7+R8)/(1-Vrun_set_point/Vin_min)
%coefficients for R6 =k*(R7+R8)
kR6=((Vin_min/Vrun_set_point)-1);

%build matrix to solve for R6, R7 and R8
Acoeff=[1 1 1; kR8 kR8 -1; -1 kR6 kR6]; %3x3 matrix of coefficients
Bsol=[R6R7R8;0;0];%matrix of the results to the system of equations
Resistors678=Acoeff^-1*Bsol;
R6=Resistors678(1); %(Ohms) resistance value of R6
R7=Resistors678(2); %(Ohms) resistance value of R7
R8=Resistors678(3); %(Ohms) resistance value of R8

fprintf('\nCalculated values for R6-R8\n');
fprintf('R6 = %10.3f KOhms \n',R6/Kilo);
fprintf('R7 = %10.3f KOhms \n',R7/Kilo);
fprintf('R8 = %10.3f KOhms \n\n',R8/Kilo);
```

```
%pick the values since it is unlikely that there will be the exact
part
%   desired
% fprintf('Select the values of R6-R8 with the closest available
values \n');
%     R6_pick=input('Enter a value for R6 in KOhms:  ')*Kilo;
%     R7_pick=input('Enter a value for R7 in KOhms:  ')*Kilo;
%     R8_pick=input('Enter a value for R8 in KOhms:  ')*Kilo;
%     fprintf('\n\n');

%once you have bought your parts, place those values in here,
uncomment
%   these three lines, and comment out the above 5 lines of code
R6_pick=110*Kilo; %(ohms)
R7_pick=40.2*Kilo; %(ohms)
R8_pick=33*Kilo; %(ohms)

R6R7R8_pick=R6_pick+R7_pick+R8_pick;% calculate the picked total
resistance

%recalculate the Shutdown voltage and the voltage when the Burst mode
turns
%   on
Vshutdown=Vrun_set_point*(R6R7R8_pick/(R7_pick+R8_pick));
Vburst=Vsync_set_point*(R6R7R8_pick/(R8_pick));



counter1=1;% preallocate for the max number of iterations of the while
loop
if R6_pick~=R6 || R7_pick~=R7 || R8_pick~=R8
    str='N';    %set the value so that the loop will be executed
else
    str='Y';
end

while str~='Y' && counter1 <= 10
if counter1>=2
    clc     %clear the screen and reprint everything
end

fprintf('%21s|| %7s\n','Designed', 'Actual');
fprintf('R6 = %10.2f KOhms|| %7.2f KOhms\n',R6/Kilo,R6_pick/Kilo);
fprintf('R7 = %10.2f KOhms|| %7.2f KOhms\n',R7/Kilo,R7_pick/Kilo);
fprintf('R8 = %10.2f KOhms|| %7.2f KOhms\n',R8/Kilo,R8_pick/Kilo);

fprintf('\n\n')
fprintf('Cumulative Resistance of R6 + R7 + R8:\n')
fprintf(' Designed = %4.2f KOhms\n',R6R7R8/Kilo);
fprintf(' Actual   = %4.2f KOhms\n\n',R6R7R8_pick/Kilo);
```

```
fprintf('Voltage at which the chip will shutdown:\n')
fprintf(' Designed = %4.2f Volts\n',Vin_min);
fprintf(' Actual   = %4.2f Volts\n\n',Vshutdown);

fprintf('Voltage at which the chip will go into burst mode:\n')
fprintf(' Designed = %4.2f Volts\n',Vburst_mode);
fprintf(' Actual   = %4.2f Volts\n\n',Vburst);

str=input(' Are these differences acceptable? Y/N: ', 's');

if str=='N'
    R6_pick=input('Enter a new value for R6 in KOhms:  ')*Kilo;
    R7_pick=input('Enter a new value for R7 in KOhms:  ')*Kilo;
    R8_pick=input('Enter a new value for R8 in KOhms:  ')*Kilo;
    R6R7R8_pick=R6_pick+R7_pick+R8_pick;% calculate picked total
resistance

    %recalculate the Shutdown voltage and the voltage when the Burst
mode
    %   turns on
    Vshutdown=Vrun_set_point*(R6R7R8_pick/(R7_pick+R8_pick));
    Vburst=Vsync_set_point*(R6R7R8_pick/(R8_pick));

elseif str=='Y' || isempty(str)
    str='Y';
    clc % clear screen print the burst mode results and the shutdown

    fprintf('Voltage at which the chip will go into burst mode:\n')
    fprintf(' Designed = %4.2f Volts\n',Vburst_mode);
    fprintf(' Actual   = %4.2f Volts\n\n',Vburst);
    fprintf('Voltage at which the chip will shutdown:\n')
    fprintf(' Designed = %4.2f Volts\n',Vin_min);
    fprintf(' Actual   = %4.2f Volts\n',Vshutdown);

end

counter1=counter1+1;
end

%values of the minimal resistance for a 1% resistors, assists in worst
case
%   scenarios, use worst case from now on
%min
R6_ptc_min=R6_pick*(1-resistor_tol/100);
R7_ptc_min=R7_pick*(1-resistor_tol/100);
R8_ptc_min=R8_pick*(1-resistor_tol/100);
R6R7R8_ptc_min=R6R7R8_pick*(1-resistor_tol/100);
%max
```

```
R6_ptc_max=R6_pick*(1+resistor_tol/100);
R7_ptc_max=R7_pick*(1+resistor_tol/100);
R8_ptc_max=R8_pick*(1+resistor_tol/100);
R6R7R8_pct_max=R6R7R8_pick*(1+resistor_tol/100);

%calculate current of R6-R8
Ir7=Vin_max./R6R7R8_ptc_min; %(A) use worst case, including resistors
Ir8=Ir7;    %(mA)
Pr7=Ir7.^2*R7_ptc_max/milli;   %(mW) Max power dissipation through R7
Pr8=Ir8.^2*R8_ptc_max/milli;   %(mW) Max power dissipation through R8

%the run pin may draw an extra amount of current
Vrun_max=Vin_max*(R7+R8)./(R6R7R8_pick);   %(V) resistor ratio will be
the same
%   if used max or min
Irun_max=(Vrun_max-5)/(5*Mega);     %(A) Max sync current into Run Pin
Pr6=(Ir7+Irun_max).^2*R6_ptc_max/milli;     %(mW) Max power
dissipation
%   through R6




%the level at which the chip will turn off after being enabled
%   calculation is taken from LTC3115-1 datasheet
Vhyst=R6_pick*0.5*micro+(R6R7R8_pick)/(R7_pick+R8_pick)*0.1; %(V) the
0.5uA
%   is taken from the typical sync current into the Run pin
Vturn_off=Vin_min-Vhyst;


%%%%%% Selection of L1 %%%%%%
%selection of inductor value and requirements

%From page 3 of TI application note:
%   http://www.ti.com/lit/an/slva535a/slva535a.pdf
Kind=0.4;   %used as an approximate guess of the current ripple at
%   the output

%buck Inductor minimums
Lbuck_min1=Vout*(Vin_max-Vout)/(Kind*Fsw*Vin_max*Iout_max);  %(H)
Kind=0.2;
Lbuck_min2=Vout*(Vin_max-Vout)/(Kind*Fsw*Vin_max*Iout_max);  %(H)
%Boost Inductor minimums
Lboost_min1=Vin_min^2*(Vout-Vin_min)/(Kind*Fsw*Iout_max*Vout);   %(H)
Kind=0.4;
Lboost_min2=Vin_min^2*(Vout-Vin_min)/(Kind*Fsw*Iout_max*Vout);   %(H)

L1_min=max([Lbuck_min1, Lbuck_min2, Lboost_min1, Lboost_min2])/micro;
%   only for viewing the result
```

```
L1_pick=22*micro;    %(H) pick a value for L1
RL1=22.3*milli;      %(Ohms) retrieved from the actual inductor picked
%http://www.digikey.com/product-detail/en/IHLP6767GZER220M5A/541-1716-
2-ND/4071407

if L1_pick > L1_min*micro
    Check=Check+1;
else
    display('Warning L1 is not picked properly');
end

%calculations from LTC3115-1 datasheet
Iripple_buck=(Vout/L1_pick)*((Vin_max-Vout)/Vin_max)*(1/Fsw-tLow);
%(A)
Iripple_boost=(Vin_min/L1_pick)*((Vout-Vin_min)/Vout)*(1/Fsw-tLow);
%(A)
%check the output ripple guess

if Iripple_boost/Iout_typ<0.21% added 0.01 on for an error and the
    %   additional 1% will not be an issue
    Check=Check+1;
else
    disp('Warning Boost ripple current does not meet the assumption
for Kind used in picking L1');
end
if Iripple_buck/Iout_typ<0.21% added 0.01 on for an error and the
additional
    %   1% will not be an issue
    Check=Check+1;
else
    disp('Warning Buck ripple current does not meet the assumption for
Kind used in picking L1');
end



%%%%%% Selection of C1, C8 %%%%%%
%selection of input capacitors
C1=4.7*micro; %(F) datasheet recommends C1>0.1uF
C8=100*micro; %(F) datasheet recommends 47uF<=C1<=100uF, 100uF chosen
%   because of the long leads

%Minimum Input cap requirements
C1C8_rated_V=100; %(V) voltage rating of the used in picking L1
Derated_C1C8_V= C1C8_rated_V*Cap_V_derating/100; %Assume cap can only
be
%   used to 80% of voltage limit for spikes and degrading
    if Derated_C1C8_V > Vin_max
        Check=Check+1;
    else
```

```
        disp('Warning Rated voltage of the input capacitor needs to be
higher');
    end

%%%%%% Selection of C2, C3 %%%%%%
%selection of switching capacitors
C2=0.1*micro;   %(F) based on recommendation from LTC3115-1 datasheet
C3=0.1*micro;   %(F) based on recommendation from LTC3115-1 datasheet

%%%%%% Selection of C7 %%%%%%
%selection of switching capacitors
%based on recommendation from LTC3115-1 datasheet
C7=10*micro;   %(F) datasheet recommends a value greater than 4.7uF



%%%%%% Selection of C4 %%%%%%
%selection of output capacitor(s)

%datasheet recommends having C4>10uF
NumCout=1;    %Number of output capacitors
C4=NumCout*10*micro; %(F) 10uF chosen so that a SMT cap can be used
ESR_C4=1; %(Ohms) selected based on typical values for ceramic X7R cap
at
%   10uF
%http://ds.murata.co.jp/software/simsurfing/en-us/#

%Calculate the expected output ripple voltages, this does not include
the
%   ripple across the ESR of the output cap(s)
Vbuck_ripple=Iout_typ*tLow/C4;
Vboost_ripple=Iout_typ/(Fsw*C4)*(Vout-Vin_min+tLow*Fsw*Vin_min)/Vout;
Vmax_ripple=max([Vbuck_ripple, Vboost_ripple]);

%Minimum Input cap requirements
C4_rated_V=25; %(V) voltage rating of the used in picking L1
Derated_C4_V= C4_rated_V*Cap_V_derating/100; %Assume cap can only be
used
%   to 80% of voltage limit for spikes and degrading
    if Derated_C4_V > Vout_max
        Check=Check+1;
    else
        disp('Warning Rated voltage of the input capacitor needs to be
higher');
    end



%%%%%% Selection of R2, R4 %%%%%%
%selection of Feedback resistors
```

```
%Pick R4 to set the compensation of the FB and R2
%1.6M and 200k are the first numbers to be found by manufacturers so
they
%   were chosen
R2=1.6*Mega;    %(Ohms) LTC 3115-1 recommended to be 1MOhm or larger
R4=R2/8;        %(Ohms)

%min
R4_ptc_min=R4*(1-resistor_tol/100);
R2_ptc_min=R2*(1-resistor_tol/100);
%max
R4_ptc_max=R4*(1+resistor_tol/100);
R2_ptc_max=R2*(1+resistor_tol/100);

Vr2=Vout_max*R2_ptc_min/(R2_ptc_min+R4_ptc_min);%(V), max voltage
across R2
Vr4=Vout_max*R4_ptc_max/(R2_ptc_min+R4_ptc_max);%(V), max voltage
across R4
Pr2=(Vr2^2)/R2_ptc_min/micro;  %(uW)  max power consumed by R2
Pr4=(Vr4^2)/R4_ptc_max/micro;  %(uW)  max power consumed by R4 8.0992

%check Vout min and max based on resistor error
Vout_calc_min=(R2_ptc_min+R4_ptc_max)/R4_ptc_max*1;  %(v) the 1 is the
1v
%   nominal value set point for FB pin
Vout_calc_max=(R2_ptc_max+R4_ptc_min)/R4_ptc_min*1;

%check Vout error due to FB resistor error plus the ripple voltages
    if Vout_max>Vout_calc_max+Vmax_ripple
        Check=Check+1;
    else
        disp('Warning Vout maximum is outside of specified
tolerance');
    end

    if Vout_min<Vout_calc_min-Vmax_ripple
        Check=Check+1;
    else
        disp('Warning Vout minimum is outside of specified
tolerance');
    end


%%%%%% Selection of R3, R5, C5, C6  %%%%%%
%selection of Compensation network
%Compensation network calculations
%calculations are taken from the LTC3115-1 datasheet
```

```
Fcrossover=58.685*Kilo; %(Hz) point at which the phase of the gain
crosses the -180 degrees
Target_Gain=5.22;%(dB)
Desired_Gain=-1*Target_Gain; %() used to achieve 0dB at Fcenter
Fzeros=Fcrossover/7; %(Hz) approximate frequency of the zeros
Fpoles=Fcrossover*7; %(Hz) approximate frequency of the poles
C6=50/(exp(Desired_Gain/20)*2*pi*Fcrossover*R2); %(F)
R3=1/(2*pi*C6*Fzeros);
C5=1/(2*pi*R2*Fzeros);
R5=1/(2*pi*C5*Fpoles);
Cpole=1/(2*pi*R3*Fpoles);   % will not be placed

%values picked based on part availability
C5_pick=10*pico;
C6_pick=110*pico;
R3_pick=169*Kilo;
R5_pick=32.4*Kilo;

%   actual values
Desired_Gain_pick=20*log(50/(2*pi*Fcrossover*R2*C6_pick));
Fzero1=1/(2*pi*R3_pick*C6_pick);              %(Hz)
Fzero2=1/(2*pi*(R2+R5_pick)*C5_pick);         %(Hz)
Fpole2=(C6+Cpole)/(2*pi*R3_pick*C6_pick*Cpole);  %(Hz)
Fpole3=1/(2*pi*R5_pick*C5_pick);              %(Hz)

%%%%%% Selection of C9, C10  %%%%%%
%C9 and C10 will be used to filter out any high frequency ripple in
%the input and output, respectively.
C9=4.7*micro;    %(Farad)
C10=4.7*micro;   %(Farad)

fprintf('\n');
fprintf('Feedback loop characteristics\n');
fprintf('%21s|| %7s\n','Designed', 'Actual');
fprintf('R3 = %10.2f KOhms|| %7.2f KOhms\n',R3/Kilo,R3_pick/Kilo);
fprintf('R5 = %10.2f KOhms|| %7.2f KOhms\n',R5/Kilo,R5_pick/Kilo);
fprintf('C5 = %10.2f pF   || %7.2f pF\n',C5/pico,C5_pick/pico);
fprintf('C6 = %10.2f pF   || %7.2f pF\n',C6/pico,C6_pick/pico);
fprintf('gain = %10.2f dB || %7.2f
dB\n',Desired_Gain,Desired_Gain_pick);

%%%%%%%%print out all of the results
fprintf('\n\n');
fprintf('%18s   %7s %7s \n','Design Requirement','Value','Units');
fprintf('%18s = %7.2f %7s \n','C1_rated_V',C1C8_rated_V,'Volts');
fprintf('%18s = %7.2f %7s \n','C4_rated_V',C4_rated_V,'Volts');
fprintf('%18s = %7.2f %7s \n','C8_rated_V',C1C8_rated_V,'Volts');
fprintf('%18s = %7.2f %7s \n','Switching Freq',Fsw/Kilo,'KHz');
fprintf('%18s = %7.2f %7s \n','L1 Resistance',RL1/milli,'mOhms');
fprintf('%18s = %7.2f %7s \n','Resistor tol',resistor_tol,'%');
```

```
fprintf('%18s = %7.2f %7s \n','RLoad',RLoad,'Ohms');

fprintf('\n');
fprintf('%15s \n','Maximum Power');
fprintf('%15s = %7.2f %7s \n','Derated 0805',((1/8)/2)/milli,'mW');
fprintf('%15s = %7.2f %7s \n','Derated 1206',((1/4)/2)/milli,'mW');
fprintf('%15s = %7.2f %7s \n','PR1',Pr1,'mW');
fprintf('%15s = %7.2f %7s \n','PR2',Pr2,'mW');
fprintf('%15s = %7.2f %7s \n','PR4',Pr4,'mW');
fprintf('%15s = %7.2f %7s \n','PR6',Pr6,'mW');
fprintf('%15s = %7.2f %7s \n','PR7',Pr7,'mW');
fprintf('%15s = %7.2f %7s \n','PR8',Pr8,'mW');

fprintf('\n');
fprintf('%15s   %7s %7s \n','Component','Value','Units');

fprintf('%15s \n','Resistor');
fprintf('%15s = %7.2f %7s \n','R1',R1/Kilo,'KOhms');
fprintf('%15s = %7.2f %7s \n','R2',R2/Mega,'MOhms');
fprintf('%15s = %7.2f %7s \n','R3',R3_pick/Kilo,'KOhms');
fprintf('%15s = %7.2f %7s \n','R4',R4/Kilo,'KOhms');
fprintf('%15s = %7.2f %7s \n','R5',R5_pick/Kilo,'KOhms');
fprintf('%15s = %7.2f %7s \n','R6',R6_pick/Kilo,'KOhms');
fprintf('%15s = %7.2f %7s \n','R7',R7_pick/Kilo,'KOhms');
fprintf('%15s = %7.2f %7s \n','R8',R8_pick/Kilo,'KOhms');

fprintf('%15s \n','Inductor');
fprintf('%15s = %7.2f %7s \n','Minimum of L1',L1_min,'uH');
fprintf('%15s = %7.2f %7s \n','L1',L1_pick/micro,'uH');


fprintf('%15s \n','Capacitor');
fprintf('%15s = %7.2f %7s \n','C1',C1/micro,'uF');
fprintf('%15s = %7.2f %7s \n','C2',C2/micro,'uF');
fprintf('%15s = %7.2f %7s \n','C3',C3/micro,'uF');
fprintf('%15s = %7.2f %7s \n','C4',C4/micro,'uF');
fprintf('%15s = %7.2f %7s \n','C5',C5_pick/pico,'pF');
fprintf('%15s = %7.2f %7s \n','C6',C6_pick/pico,'pF');
fprintf('%15s = %7.2f %7s \n','C7',C7/micro,'uF');
fprintf('%15s = %7.2f %7s \n','C8',C8/micro,'uF');
fprintf('%15s = %7.2f %7s \n','C9',C9/micro,'uF');
fprintf('%15s = %7.2f %7s \n','C10',C10/micro,'uF');
```

Appendix B

Results from MATLAB script used in determining values for the DC to DC converter

```
Voltage at which the chip will go into burst mode:
 Designed = 3.75 Volts
 Actual   = 3.89 Volts

Voltage at which the chip will shutdown:
 Designed = 3.00 Volts
 Actual   = 3.03 Volts

Feedback loop characteristics
             Designed||  Actual
R3 =      172.54 KOhms||  169.00 KOhms
R5 =       32.65 KOhms||   32.40 KOhms
C5 =       11.87 pF   ||   10.00 pF
C6 =      110.03 pF   ||  110.00 pF
gain =       -5.22 dB ||   -5.22 dB


Design Requirement      Value   Units
        C1_rated_V =  100.00   Volts
        C4_rated_V =   25.00   Volts
        C8_rated_V =  100.00   Volts
    Switching Freq =  751.58     KHz
     L1 Resistance =   22.30   mOhms
      Resistor tol =    1.00       %
             RLoad =    4.80    Ohms

  Maximum Power
   Derated 0805 =   62.50      mW
   Derated 1206 =  125.00      mW
            PR1 =   34.02      mW
            PR2 =   44.55      mW
            PR4 =    5.66      mW
            PR6 =    5.51      mW
            PR7 =    1.97      mW
            PR8 =    1.62      mW
```

Component		Value	Units
Resistor			
R1	=	47.50	KOhms
R2	=	1.60	MOhms
R3	=	169.00	KOhms
R4	=	200.00	KOhms
R5	=	32.40	KOhms
R6	=	110.00	KOhms
R7	=	40.20	KOhms
R8	=	33.00	KOhms
Inductor			
Minimum of L1	=	20.62	uH
L1	=	22.00	uH
Capacitor			
C1	=	4.70	uF
C2	=	0.10	uF
C3	=	0.10	uF
C4	=	10.00	uF
C5	=	10.00	pF
C6	=	110.00	pF
C7	=	10.00	uF
C8	=	100.00	uF
C9	=	0.47	uF
C10	=	0.47	uF

Appendix C

MATLAB script used to calculate the diode and impedance calculations with a fixed input diode voltage and a variable load resistor.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%
%This is to calculate the parameters surrounding the dual diode
selection
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%
%Original Author: Robert Bernaciak 22-May-14
%Copyright 2014, All Rights Reserved

%Modifications Tracker
%Person             Date        Modifications made
%Robert Bernaciak   19-June-14  Mod tracker added
%Robert Bernaciak   08-July-14  Added Single diode calculations to
this file and
%   reorganized the plots, fixed dual diode efficiency and impedance

%This file is intended to calculate Impedance and Efficiency for the
%   Schottky Diodes used in the rectenna

clear all
clc

%%MA4E1317%% RB prefer this over Bat17
Freq=5.8*10^9;  %operating frequency of 5.8GHz
Rseries=4;      %Ohms, from Datasheet
Rload=10:10:500;      %Ohms, user specified
Vbi=0.7;        %Volts, barrier voltage of the diode, from Datasheet
Vbmax=7;         %Volts, max continuous reverse bias voltage, from
Datasheet
Cj0=0.02*10^-12;   %Zero-bias junction capacitance, from Datasheet
%Do not edit items below
Vd=Vbmax/2;      %Volts, Voltage across the diode(not to be more than
1/2 breakdown voltage)
w=2*pi*Freq;    %Angular Freq



%%Bat17%%
% Freq=5.8*10^9;  %operating frequency of 5.8GHz
% Rseries=8;      %Ohms
% Rload=10:10:500;      %Ohms
% Vbi=0.45;        %Volts, barrier voltage of the diode
% Vbmax=4;         %Volts, max continuous reverse bias voltage
% Cj0=0.55*10^-12;   %Zero-bias junction capacitance, From Infineon
datasheet
% %Do not edit items below
```

```
% Vd=Vbmax/2;      %Volts, Voltage across the diode(not Rec'd to be
more than 1/2 breakdown voltage)
% w=2*pi*Freq;    %Angular Freq


iRload=length(Rload);
Ktheta=zeros(1,iRload);
for n=1:iRload
Ktheta(n)=pi*Rseries/(Rload(1,n)*(1+Vbi/Vd));
end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%     FIND ThetaOn
%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%

Kout=zeros(1,1);      %preallocate the output constant
stepsize1=10^5;       %used to set number of values in theta and the
error size
stepsize2=stepsize1;
theta=linspace(-pi,pi,stepsize1);%create vector of theta
Ktemp=tan(theta)-theta;

ThetaOnR=zeros(1,iRload); %preallocate the size of the ThetaOn

for m=1:iRload
count=1;
count2=count;
stp=1;
stop_me=0;
while stp~=0 || stop_me<10
    stop_me=stop_me+1;
    for n=1:length(Ktemp)
        if (Ktemp(n)*Ktheta(m)>0)
            if(((Ktemp(n)-Ktheta(m))<(1/stepsize2)) && ((Ktemp(n)-
Ktheta(m))>(-1/stepsize2)))
                Kout(1,count)=Ktemp(n);
                Kout(2,count)=n;
                count=count+1;
                ThetaOnR(m)=theta(n);    %ThetaOn in Radians
                stp=0;
            elseif Ktemp(n)==Ktheta>0
                ThetaOnR(m)=theta(n);
                stp=0;
                break
            end
        end
    end
    stepsize2=stepsize2/1.5;
```

```
end
stepsize2=stepsize1;
end

ThetaOnD=ThetaOnR*180/(2*pi); %ThetaOn in Degrees
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%     FIND Zd
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%
% equations from Strassner/Chang 2002

Cj=Cj0*sqrt(Vbi/(Vbi+Vd));    %junction capacitance
%calculating Zd for the diode
D_Single=ThetaOnR-cos(ThetaOnR).*sin(ThetaOnR);
E_Single=w*Rseries*Cj*((pi-ThetaOnR)./cos(ThetaOnR)+sin(ThetaOnR));
Zd_Single=pi*Rseries./(D_Single+1i.*E_Single);
ZdReal_Single=real(Zd_Single);
ZdComplex_Single=imag(Zd_Single);

%not correct since Ren did not suggest using the substitutions for
this calculation
%calculating Zd for dual diodes
D_Dual=ThetaOnR-cos(ThetaOnR).*sin(ThetaOnR);
E_Dual=w.*(Rseries+Rload).*Cj.*((pi-
ThetaOnR)./cos(ThetaOnR)+sin(ThetaOnR));
Zd_Dual=pi*(Rseries+Rload)./(D_Dual+1i.*E_Dual);
ZdReal_Dual=real(Zd_Dual);
ZdComplex_Dual=imag(Zd_Dual);

%Real impedance
figure(1)
subplot(1,2,1)
plot(Rload, ZdReal_Single)
title('Single Diode Real Impedance')
ylabel('Real Diode Impedance')
xlabel('Load Resistance')
grid ON
%Complex impedance
subplot(1,2,2)
plot(Rload, ZdComplex_Single)
title('Single Diode Complex Impedance')
ylabel('Complex Diode Impedance')
xlabel('Load Resistance')
grid ON
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%     FIND Nd
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
```

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%
%Equations are from McSpaden et al. 1998, equation is same as the one
used in Strassner/ Chang 2002

%Single Diode Efficiency
A_Single=Rload./(pi.*Rseries).*(1+Vbi./Vd)^2.*(ThetaOnR.*(1+1./(2*(cos
(ThetaOnR)).^2))-3/2.*tan(ThetaOnR));
B_Single=Rseries.*Rload*Cj^2*w^2./(2*pi).*(1+Vbi./Vd).*((pi-
ThetaOnR)./((cos(ThetaOnR)).^2)+tan(ThetaOnR));
C_Single=Rload./(pi*Rseries).*(1+Vbi./Vd).*(Vbi./Vd).*(tan(ThetaOnR)-
ThetaOnR);
Nd_Single=1./(1+A_Single+B_Single+C_Single);
% Dual Diodes Efficiency
A_Dual=(Rload+ZdReal_Single)./(pi.*(Rseries+Rload)).*(1+Vbi./Vd)^2.*(T
hetaOnR.*(1+1./(2*cos(ThetaOnR).^2))-3./2.*tan(ThetaOnR));
B_Dual=(Rseries+Rload).*(Rload+ZdReal_Single)*Cj^2*w^2./(2*pi).*(1+Vbi
./Vd).*((pi-ThetaOnR)./((cos(ThetaOnR).^2))+tan(ThetaOnR));
C_Dual=(Rload+ZdReal_Single)./(pi*(Rseries+Rload)).*(1+Vbi./Vd).*(Vbi.
/Vd).*(tan(ThetaOnR)-ThetaOnR);
Nd_Dual=1./(1+A_Dual+B_Dual+C_Dual);

figure(2)
plot(Rload, Nd_Dual,'-x', Rload, Nd_Single,'-o')
title('Efficiency Versus Load Resistance')
ylabel('Efficiency')
xlabel('Load Resistance')
legend('Dual Diodes','Single Diode','Location','SouthEast')
grid ON
```

Appendix D

MATLAB script used to calculate the diode and impedance calculations with a variable input diode voltage and fixed load resistor.

```
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%
%This is to calculate the parameters surrounding the dual diode
selection
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%
%Original Author: Robert Bernaciak 22-May-14
%Copyright 2014, All Rights Reserved

%Modifications Tracker
%Person             Date        Modifications made
%Robert Bernaciak   19-June-14  Mod tracker added
%Robert Bernaciak   08-July-14  Added Single diode calculations to
this file and
%   reorganized the plots, fixed dual diode efficiency and impedance

%This file is intended to calculate Impedance and Efficiency for the
%   Schottky Diodes used in the rectenna

clear all; clc;

%%MA4E1317%% RB prefer this over Bat17
Freq=5.8*10^9;  %operating frequency of 5.8GHz
Rseries=4;      %Ohms, from Datasheet
Rload=135;      %Ohms, user specified
Vbi=0.7;        %Volts, barrier voltage of the diode, from Datasheet
Vbmax=7;         %Volts, max continuous  reverse bias voltage, from
Datasheet
Cj0=0.02*10^-12;   %Zero-bias junction capacitance, from Datasheet
%Do not edit items below
%Vd=Vbmax/2;      %Volts, Voltage across the diode(not to be more than
1/2 breakdown voltage)
Vd=0.1:0.1:Vbmax;     %used to vary the input power
w=2*pi*Freq;    %Angular Freq

%%Bat17%%
% Freq=5.8*10^9;  %operating frequency of 5.8GHz
% Rseries=8;      %Ohms
% Rload=10:10:500;      %Ohms
% Vbi=0.45;         %Volts, barrier voltage of the diode
% Vbmax=4;          %Volts, max continuous  reverse bias voltage
% Cj0=0.55*10^-12;   %Zero-bias junction capacitance, From Infineon
datasheet
% %Do not edit items below
```

```
% Vd=Vbmax/2;      %Volts, Voltage across the diode(not Rec'd to be
more than 1/2 breakdown voltage)
% w=2*pi*Freq;    %Angular Freq

iVd=length(Vd);
Ktheta=zeros(1,iVd);
for n=1:iVd
Ktheta(n)=pi*Rseries./(Rload*(1+Vbi/Vd(1,n)));
end
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%     FIND ThetaOn
%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%
KthetaMax=max(abs(Ktheta));
Kout=zeros(1,1);      %preallocate the output constant
stepsize1=10^7;       %used to set number of values in theta and the
error size
stepsize2=stepsize1;
theta=linspace(-pi,pi,stepsize1);%create vector of theta
Ktemp=tan(theta)-theta;

ThetaOnR=zeros(1,iVd); %preallocate the size of the ThetaOn

for m=1:iVd
count=1;
count2=count;
stp=1;
stop_me=0;
while stp~=0 && stop_me<75
    stop_me=stop_me+1;
    for n=1:length(Ktemp)
        if (Ktemp(n)*Ktheta(m)>0)
            if(((Ktemp(n)-Ktheta(m))<(1/stepsize2)) && ((Ktemp(n)-
Ktheta(m))>(-1/stepsize2)))
                Kout(1,count)=Ktemp(n);
                Kout(2,count)=n;
                count=count+1;
                ThetaOnR(m)=theta(n);   %ThetaOn in Radians
                stp=0;
            elseif Ktemp(n)==Ktheta>0
                ThetaOnR(m)=theta(n);
                stp=0;
                break
            end
        end
    end
    stepsize2=stepsize2/1.5;
end
stepsize2=stepsize1;
```

```
end

ThetaOnD=ThetaOnR*180/(2*pi); %ThetaOn in Degrees
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%     FIND Zd
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%
% equations from Strassner/Chang 2002

Cj=Cj0.*sqrt(Vbi./(Vbi+Vd));    %junction capacitance
%calculating Zd for the diode
D_Single=ThetaOnR-cos(ThetaOnR).*sin(ThetaOnR);
E_Single=w*Rseries.*Cj.*((pi-ThetaOnR)./cos(ThetaOnR)+sin(ThetaOnR));
Zd_Single=pi*Rseries./(D_Single+1i.*E_Single);
ZdReal_Single=real(Zd_Single);
ZdComplex_Single=imag(Zd_Single);

%not correct since Ren did not suggest using the substitutions for
this calculation
%calculating Zd for dual diodes
D_Dual=ThetaOnR-cos(ThetaOnR).*sin(ThetaOnR);
E_Dual=w.*(Rseries+Rload).*Cj.*((pi-
ThetaOnR)./cos(ThetaOnR)+sin(ThetaOnR));
Zd_Dual=pi*(Rseries+Rload)./(D_Dual+1i.*E_Dual);
ZdReal_Dual=real(Zd_Dual);
ZdComplex_Dual=imag(Zd_Dual);

%Real impedance
figure(1)
subplot(1,2,1)
plot(Vd, ZdReal_Single)
title('Single Diode Real Impedance with RLoad=135Ohms')
ylabel('Real Diode Impedance')
xlabel('Vd')
grid ON
%Complex impedance
subplot(1,2,2)
plot(Vd, ZdComplex_Single)
title('Single Diode Complex Impedance')
ylabel('Complex Diode Impedance')
xlabel('Vd')
grid ON
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%     FIND Nd
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
%%%%
```

```
%Equations are from McSpaden et al. 1998, equation  is same as the one
used in Strassner/ Chang 2002

%Single Diode Efficiency
A_Single=Rload./(pi.*Rseries).*(1+Vbi./Vd).^2.*(ThetaOnR.*(1+1./(2*(co
s(ThetaOnR)).^2))-3/2.*tan(ThetaOnR));
B_Single=Rseries.*Rload*Cj.^2*w^2./(2*pi).*(1+Vbi./Vd).*((pi-
ThetaOnR)./((cos(ThetaOnR)).^2)+tan(ThetaOnR));
C_Single=Rload./(pi*Rseries).*(1+Vbi./Vd).*(Vbi./Vd).*(tan(ThetaOnR)-
ThetaOnR);
Nd_Single=1./(1+A_Single+B_Single+C_Single);
% Dual Diodes Efficiency
A_Dual=(Rload+ZdReal_Single)./(pi.*(Rseries+Rload)).*(1+Vbi./Vd).^2.*(
ThetaOnR.*(1+1./(2*cos(ThetaOnR).^2))-3./2.*tan(ThetaOnR));
B_Dual=(Rseries+Rload).*(Rload+ZdReal_Single).*Cj.^2.*w^2./(2*pi).*(1+
Vbi./Vd).*((pi-ThetaOnR)./((cos(ThetaOnR).^2))+tan(ThetaOnR));
C_Dual=(Rload+ZdReal_Single)./(pi*(Rseries+Rload)).*(1+Vbi./Vd).*(Vbi.
/Vd).*(tan(ThetaOnR)-ThetaOnR);
Nd_Dual=1./(1+A_Dual+B_Dual+C_Dual);

figure(2)
plot(Vd, Nd_Dual,'-x', Vd, Nd_Single,'-o')
title('Efficiency Versus Vd with RLoad=135Ohms')
ylabel('Efficiency')
xlabel('Vd')
legend('Dual Diodes','Single Diode','Location','SouthEast')
grid ON

Pin=(Vd.^2./(1*Rload));

figure(3)
plot(Pin, Nd_Dual,'-x', Pin, Nd_Single,'-o')
title('Input Power Versus Efficiency with Rload=135Ohms')
ylabel('Efficiency')
xlabel('Input Power (W)')
legend('Dual Diodes','Single Diode','Location','SouthEast')
grid ON
display('Calculations Complete')
```

Appendix E

Code to run frequency response analysis in LTSPICE, and an image of the program ready to be run for a simulation.

```
.param freq=15k
.step oct param freq 15k 100K 12
.save V(a) V(b)
.option plotwinsize=0 numdgt=15
.param t0=0.25m
.tran 0 {{t0}+25/{freq}} {t0} uic
.options nomarch
.measure Aavg avg V(a)
.measure Bavg avg V(b)
.measure Are avg (V(a)-Aavg)*cos(360*time*Freq)
.measure Aim avg -(V(a)-Aavg)*sin(360*time*Freq)
.measure Bre avg (V(b)-Bavg)*cos(360*time*Freq)
.measure Bim avg -(V(b)-Bavg)*sin(360*time*Freq)
.measure GainMag param 20*log10(hypot(Are,Aim) / hypot(Bre,Bim))
.measure GainPhi param mod(atan2(Aim, Are) - atan2(Bim, Bre)+180,360)-180
.save
```

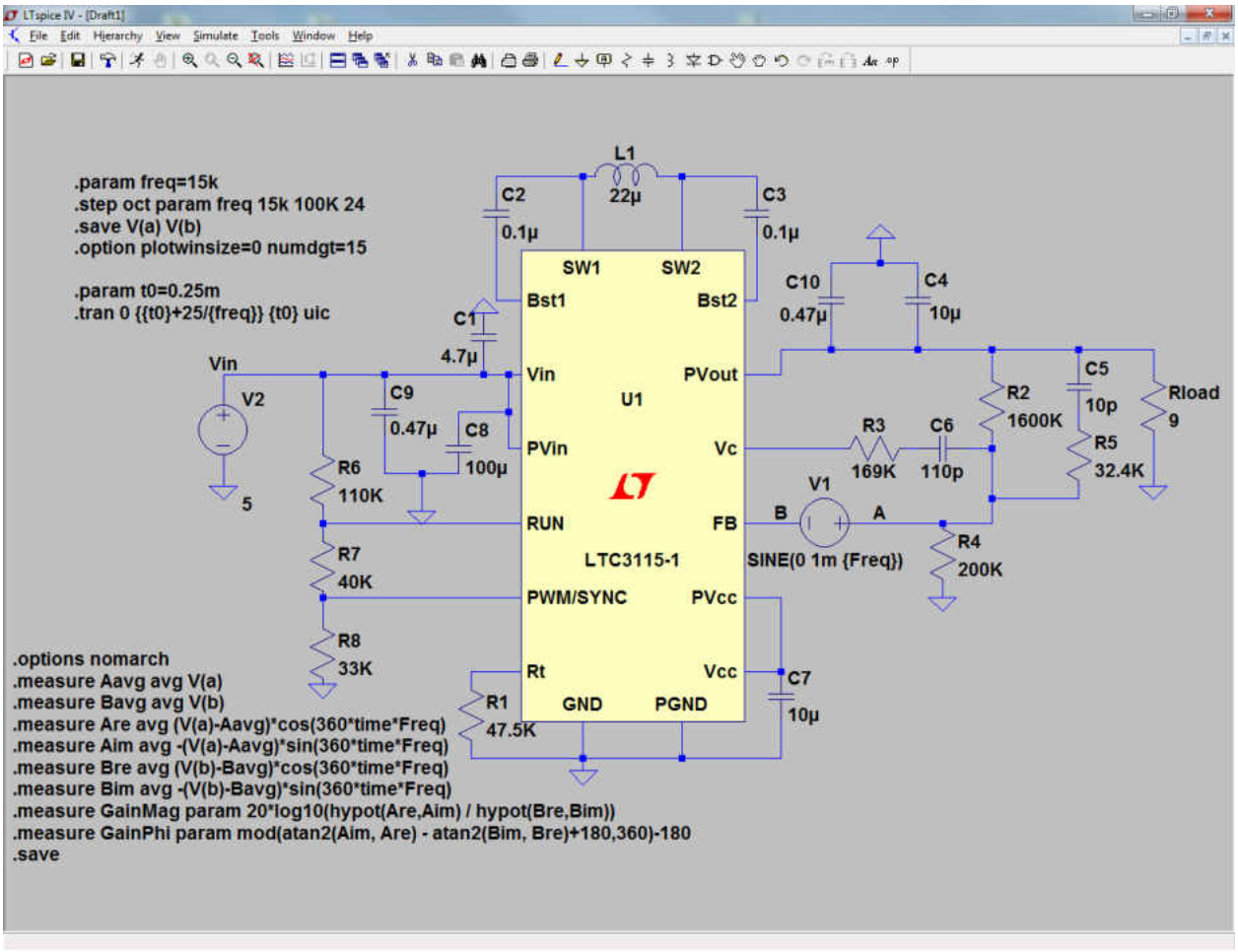

Figure 72: Final VC Test setup with the chosen values.

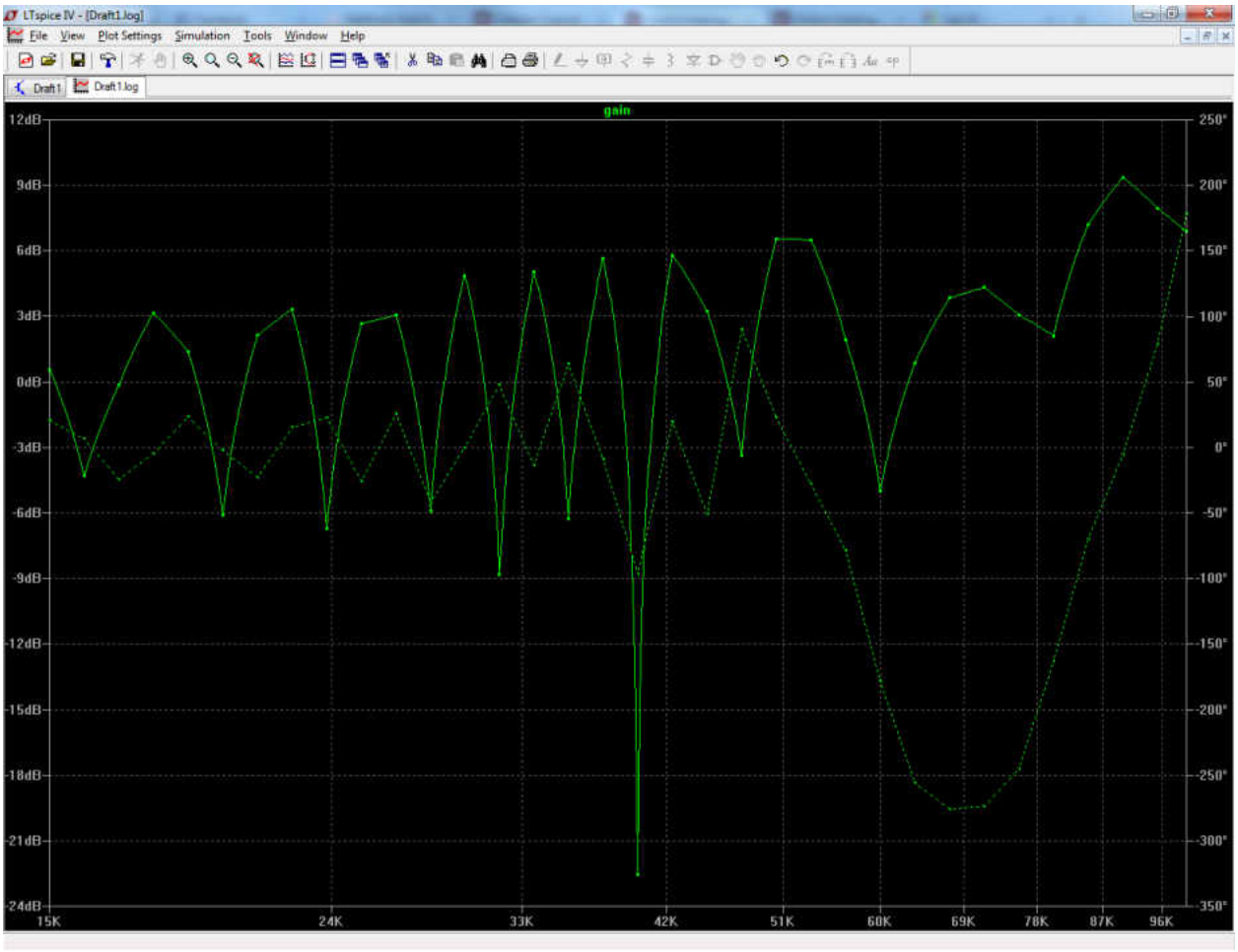

Figure 73: Final VC Test results with the chosen values.

Additional information can be found at: http://cds.linear.com/docs/en/lt-journal/LTJournal-V23N3-05-di-LTspice-GabinoAlonso.pdf or http://www.linear.com/solutions/4672

Appendix F

Measured results from the testing of the LTC3115-1 buck/boost converter.

Rload	18Ω	Iout	Iout 0.5 A load	Pout	4.5W
Vin	I_in	Vout	Iout measured	Efficeincy (%)	Vout_ripple
2	0	1	0	0.00	0.00
3	0.362	3.97	0.219	80.06	0.24
4	0.329	4.49	0.247	84.27	0.24
5	0.309	4.91	0.27	85.81	0.24
6	0.816	9.05	0.491	90.76	0.24
7	0.682	9.05	0.491	93.08	0.24
8	0.592	9.05	0.491	93.82	0.24
9	0.522	9.05	0.491	94.58	0.24
10	0.468	9.05	0.491	94.95	0.24
11	0.425	9.05	0.491	95.05	0.24
12	0.391	9.05	0.491	94.70	0.24
13	0.361	9.05	0.491	94.68	0.24
14	0.337	9.05	0.491	94.18	0.24
15	0.315	9.05	0.491	94.04	0.24
16	0.296	9.05	0.491	93.82	0.24
17	0.28	9.05	0.491	93.35	0.24
18	0.265	9.05	0.491	93.16	0.24
19	0.251	9.05	0.491	93.18	0.24
20	0.24	9.05	0.491	92.57	0.24
21	0.229	9.05	0.491	92.40	0.24
22	0.22	9.05	0.491	91.81	0.24
23	0.211	9.05	0.491	91.56	0.24
24	0.203	9.05	0.491	91.21	0.24
25	0.196	9.05	0.491	90.68	0.24
26	0.189	9.05	0.491	90.43	0.24
27	0.183	9.05	0.491	89.93	0.24
28	0.177	9.05	0.491	89.66	0.24
29	0.172	9.05	0.491	89.08	0.24
30	0.167	9.05	0.491	88.69	0.24
31	0.162	9.05	0.491	88.48	0.24
32	0.158	9.05	0.491	87.89	0.24
33	0.154	9.05	0.491	87.44	0.24
34	0.149	9.05	0.491	87.71	0.24
35	0.146	9.05	0.491	86.96	0.24
36	0.142	9.05	0.491	86.92	0.24
37	0.139	9.05	0.491	86.40	0.24
38	0.136	9.05	0.491	85.98	0.24

Table 7: Measured data from testing the LTC3115-1 at 0.5A load.

Rload	9Ω	Iout	Iout 1 A load	Pout	9W
Vin	I_in	Vout	Iout measured	Efficeincy (%)	Vout_ripple
2	0	0	0	0.00	0.00
3	0	0	0	0.00	0.00
4	0	0	0	0.00	0.00
5	0	0	0	0.00	0.00
6	1.889	8.02	0.861	60.92	2.24
7	1.495	8.5	0.877	71.23	2.16
8	1.281	9.12	0.96	85.43	1.50
9	1.063	9.12	0.96	91.51	0.64
10	0.941	9.12	0.96	93.04	0.64
11	0.853	9.12	0.96	93.31	0.64
12	0.781	9.12	0.96	93.42	0.64
13	0.72	9.12	0.96	93.54	0.48
14	0.669	9.12	0.96	93.48	0.48
15	0.625	9.12	0.96	93.39	0.48
16	0.587	9.12	0.96	93.22	0.48
17	0.552	9.12	0.96	93.30	0.48
18	0.523	9.12	0.96	93.00	0.48
19	0.497	9.12	0.96	92.72	0.48
20	0.473	9.12	0.96	92.55	0.48
21	0.451	9.12	0.96	92.44	0.48
22	0.432	9.12	0.96	92.12	0.48
23	0.414	9.12	0.96	91.95	0.48
24	0.398	9.12	0.96	91.66	0.48
25	0.383	9.12	0.96	91.44	0.48
26	0.369	9.12	0.96	91.26	0.48
27	0.356	9.12	0.96	91.09	0.48
28	0.344	9.12	0.96	90.90	0.48
29	0.333	9.12	0.96	90.66	0.48
30	0.323	9.12	0.96	90.35	0.48
31	0.314	9.12	0.96	89.94	0.48
32	0.305	9.12	0.96	89.70	0.48
33	0.296	9.12	0.96	89.63	0.48
34	0.288	9.12	0.96	89.41	0.48
35	0.281	9.12	0.96	89.02	0.48
36	0.274	9.12	0.96	88.76	0.48
37	0.267	9.12	0.96	88.62	0.48
38	0.261	9.12	0.961	88.37	0.48

Table 8: Measured data from testing the LTC3115-1 at 1.0A load.

Appendix G

Final parameters and design impedances from the simulations in CST

Parameter List

Name	Value	Description
Cap_pf	213.44672358391	213.44672358391
Epsilon	2.94	
fo	5.8*10^9	Center freq.
Gnd_Roughness	0.0004	in mm
H_Cu	0.03302	Thickness of 1oz Copper
H_Sub	1.524	Hieght of Substrate
L1	0.80184934061904	Length of L1
L2	2.5607082994162	Length of L2
L3	3.2856944459518	Length of L3
L4	4.2209605097765	Length of L4
La	0.18826627288123	Length of La
lam	51.7	Wavelength
Lb	3.7945795133895	Length of Lb
Lc	1.9984998520041	Length of Lc
Ld	2.3350738386475	Length of Ld
Le	0.11586939491109	Length of Le
Lt1	La+Lb+Lc+Ld+Le+5*Wta	distance for layout of L_dc
Lt2	Lt1+0.5*L_dc+0.5*L_dc2	Layout position of L_dc2
Ltotal	Lt2+0.5*L_dc2	total length of the rectifier
L_dc	0.2000363646705	Length from diode to cap
L_dc2	7.9995579361477	Length from cap to load
L_Gap_diode	0.127	gap between the pads of the diode selected
Rho	0.0000001	for Gnd plate and cps
Rload	135	
TanDelta	0.0012	Dissipation factor (typical value)
W1	1.04520762463803	Width of w1 microstrip lines(1.045207624638
W2	W1	Width of w2 microstrip lines
Wgap	0.4	Distance btw CPS
Wtab	0.81452621979081	Thickness of the Stub(0.833105837029)

Figure 74: Final parameters of the CST simulation showing a design without stubs used for SMA attachment during testing.

	Z_o = 107.98 Z_{in}=-j123.3	Z_o = 107.98 Z_{in}=-j20.55	Z_o = 107.98 Z_{in}=-j75.83	Z_o = 107.98 Z_{in}=j337.9
Z_o = 122.905	Z_o = 122.905	Z_o = 122.905	Z_o = 122.905	Z_o = 122.905
	Z_{in}=-j123.3 Z_o = 107.98	Z_{in}=-j20.55 Z_o = 107.98	Z_{in}=-j75.83 Z_o = 107.98	Z_{in}=j337.9 Z_o = 107.98

Figure 75: Impedance line diagram of the final rectifier parameter results including Z_o and Z_{in} of the stubs. The antenna inputs are on the left of the figure and the load would be on the right.

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