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Wideband Wilkinson Power Divider For Uav Phased Array Radar

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WIDEBAND WILKINSON POWER DIVIDER FOR UAV PHASED ARRAY RADAR

by

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This thesis, submitted by Jonathan Musselwhite in partial fulfillment of the requirements for the Degree of Master of Science from the University of North Dakota, has been read by the Faculty Advisory Committee under whom the work has been done, and is hereby approved.

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This thesis is being submitted by the appointed advisory committee as having met all of the requirements of the Graduate School at the University of North Dakota and is hereby approved.

_____
Wayne Swisher, Dean of the Graduate School

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PERMISSION

Title: Wideband Wilkinson Power Divider for UAV Phased Array Radar

Department: Electrical Engineering

Degree: Master of Science

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Date 07/25/2012

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This work is dedicated to my mother and father who have always supported my endeavors and sacrificed themselves to provide me the opportunities to push myself to new limits. Throughout this research, they have been a constant support with a listening ear, sympathetic understanding, and encouraging words. I definitely would not have been able to do this without their support.

ABSTRACT

The purpose of this project is to design a wideband Wilkinson power divider as part of an active phased array radar system for use in Unmanned Aerial Vehicle (UAV) applications. In order to comply with the entire system, the power divider was restricted in size, operating frequency, and bandwidth. The proposed power divider was integrated into a 10 GHz phased array system for future development in a transmitting and receiving system.

The Wilkinson power divider was designed to provide 2 GHz bandwidth centered at 10 GHz. In order to provide the bandwidth, a 4-stage Wilkinson power divider was designed and fabricated. It was then tested thoroughly to provide Printed Circuit Board (PCB) characteristics for integration within the system. Port isolation, phase error, and PCB power losses were found for the power divider and recorded to provide better integration into the radar system. The experimental results compared well with the simulated models created in the design phase.

The final modularly designed phased array radar consisted of a Vivaldi antenna array, phase shifter and amplifier module, and control module. The focus of the work presented is the Wilkinson power divider that was designed to meet stringent design requirements for space, operating frequency, and phase error. The result is a fabricated

Wilkinson power divider that met all the requirements and the module functions within the phased array system.

CHAPTER 1

INTRODUCTION

1.1 Unmanned Aircraft Systems' Barrier for Entry in the National Airspace System

The commercialization of Unmanned Aircraft Systems (UAS) applications for use in the U.S. National Airspace System (NAS) are being stifled by the strict safety regulations imposed by the Federal Aviation Administration (FAA). These regulations are to provide safety in commercial airspace for both those in the air and on the ground. One of the primary concerns with Unmanned Aerial Vehicles (UAVs) is the communication between aircrafts and the procedure to avoid airborne collisions.

In addition to the communication and avoidance of other aircrafts, a non-cooperative method is necessary to provide collision avoidance from non-responsive aircrafts, birds, gliders, power lines, buildings, hot air balloons, and any other type of airborne structure that would possibly not have the ability to properly communicate with the UAV. Until both cooperative and non-cooperative sense and avoid method can be integrated into UAVs, they will not be available for commercial use in the NAS.

1.2 Cooperative Sense and Avoid Using Automatic Dependent Surveillance-Broadcast

Research done at the University of North Dakota (UND) has produced a system that uses an Automatic Dependent Surveillance-Broadcast (ADS-B) for sense and avoid

[1]. The designed system uses the communication between different aircraft's ADS-B units to provide the UAV a procedure for proper FAA avoidance maneuvers.

While this system provides a UAV with proper FAA regulation collision avoidance techniques [2], it does not take into consideration old aircrafts or crop dusters that do not have ADS-B units on them. There are also other obstacles within the NAS that could prove to be harmful to the aircraft such as birds, power lines, etc. Because of these factors, it is necessary to complement a sense and avoid system such as UND's Unmanned Aircraft Systems Engineering (UASE) ADS-B payload with a non-cooperative sense and avoid application [3].

1.3 Phased Array Radar UAS for Non-Cooperative Sense and Avoidance

A potential solution for non-cooperative sense and avoid applications is a small-scale phased array radar for UAS platforms. Using multiple antennas in an array, the signal can be shifted using a phase shifter which will alter the antenna array radiation direction. The alterations in the array radiation can be controlled through the phase shifters to create a sweeping motion. This phased array antenna can be integrated into a radar [4].

These phased arrays radars have lower costs and smaller size as opposed to mechanically driven radar designs. Additionally, the deterioration of the mechanical radar system is decreased due to the reduction in moving parts. The phased array radar can provide a non-cooperative sense and avoid solution for UAVs that includes higher efficiency, lower costs, and a smaller size.

1.4 Laserlith Corporation and Private Corporation Involvement

Laserlith Corporation instituted a program to create and manufacture Electronically Steered Antenna Arrays (ESAs) with the cooperation of the Army Research Laboratory and the Air Force Research Laboratory. The Wilkinson power divider of this research work was designed with the intention of integration with the Laserlith Corporation's phase shifters. These phase shifters utilize new MEMS technology designed by Laserlith that provides higher efficiency with lower power consumption. Laserlith's MEMS based phase shifters will provide a much quicker phase change which increases the radar's sweeping speed. Currently, these phase shifters have not been provided for integration and the system of this study uses commercial off-the-shelf hardware instead. The final goal is to have the Laserlith Corporation's phase shifters replacing the off-the-shelf mounted phase shifters in the full phased array radar of this research work.

1.5 Prior Work

Previous work on this project has been done by others with the creation of a 2.4 GHz tracking array with printed dipole antennas and commercial off-the-shelf products. Research on tracking a video signal from an in-flight UAV payload provided a base concept for the design of our system [5]. Using this concept, a C-band 5.8 GHz tracking phased array has been developed and characterized. This system provided a proof of concept for phased array sense and avoid applications (Figure 1).

Figure 1: 5.8 GHz Phase Array Proof of Concept System

The phased array radar system when integrated into a small-scale Unmanned Aerial System (UAS) provides multiple commercial and military applications. Another proposed application is the tracking of targets located on the horizon. Would provide a method for self defense for ships against low altitude attacks [6]. In order to aid the radar's field of view on a Naval ship, a low power radar system can be placed on an in-flight UAV. The aircraft could find low altitude targets that were out of the ship's mounted radar range. This tracking capability can be applied to multiple other applications within the commercial sector.

In addition to the previous Naval research, prior studies at the UASE program at UND in the area of sense and avoid technology also prompted the research and design of a non-cooperative sense and avoid platform [1]. A linear array was designed,

manufactured, and integrated into UAV's wing structure with antenna elements [7]. This work led to the initial concept of creating a phased array sense and avoid system that is wing-mounted on the UND UASE Super Hauler (shown in Figure 2).

Figure 2: UND UASE Super Hauler

The Wilkinson power divider design of this thesis was intended to be eventually integrated into the phased array sense and avoid system. In coordination with the UASE program at UND, a small-scale payload system that operates at 10 GHz has been designed to perform tracking and radar applications. This system consists of a Radio Frequency (RF) source, a power divider, phase shifting module, amplifiers, and antenna elements [8]. Figure 3 displays the design for the 10 GHz phased array system. The system is comprised of four separate modules, the power divider board, amplification and phase shifter board, control board, and antenna array. This thesis focuses on the design of a 10 GHz Wilkinson power divider board with a 2 GHz bandwidth centered at 10 GHz. A power divider board with a wide bandwidth that integrates into the system is to be designed and fabricated. The board has multiple constraints for integration into the system. The size of the board along with the distance between each output port, the

operating frequency bandwidth, and the power loss with the anticipated phase error are critical to the design of the power divider module.

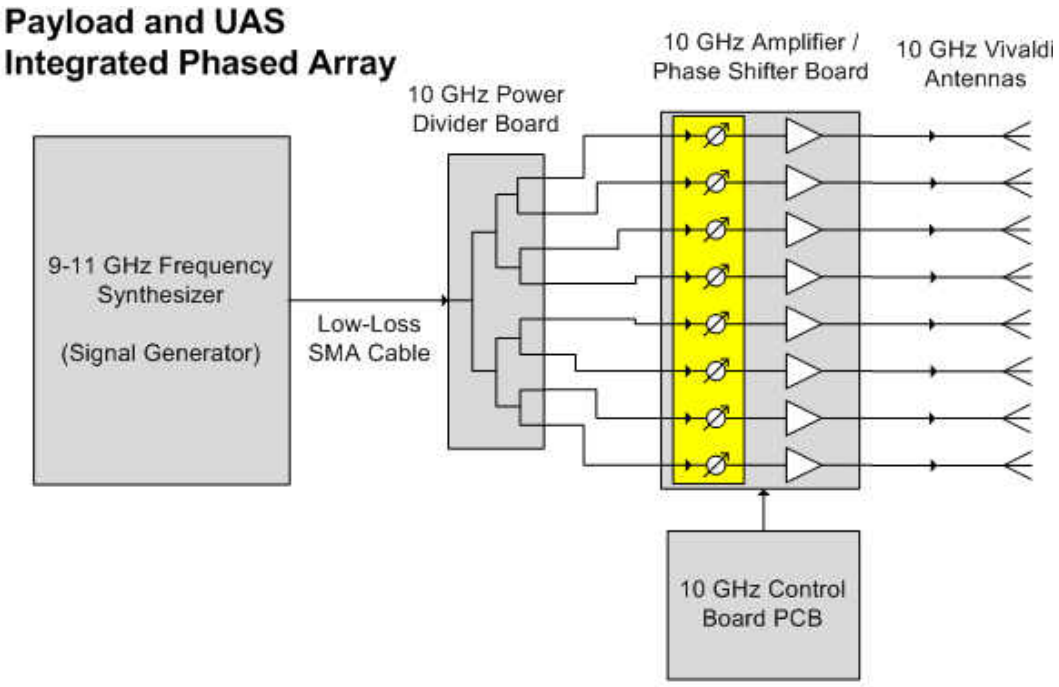

Figure 3: 10 GHz Phased Array Block Diagram

Work has been performed by D. Hajicek in creating a phased array control module and phase shifter with amplifier module [9]. Through digital phase shifting modules with a fixed number of phase shifting states, a simple control system was created to control the array steering performance. The quantization that comes with fixed states was lessened by using high resolution phase shifter. Therefore, a more precise control with the array steering was provided that reduced degradation of the phase control [10].

As shown in Figure 3, steering is achieved by the phase shifting module. This is the basic principle of a phase array system. The details of the design of a 10 GHz wideband Vivaldi antenna elements is provided by J. Alme [11].

1.6 Review of Literature

Prior literature was reviewed to provide a better understanding of the research and to also ensure that this thesis was pertinent to research within the realm of Wilkinson power dividers. The papers covered efficacy and designs of Wilkinson power dividers. Many of the readings were on the Wilkinson design and potential design modifications.

E. Wilkinson first created the design of a power divider which was named after his work [12]. His findings offered a basic design for the N-way power divider. This design was modified by S. Cohn who provided a basic design for a multi-stage N-way power divider [13]. He was the first to propose using Chebyshev polynomials to roughly determine the size of the isolation resistors.

Recent research has been performed by J. Cooper who modeled multiple Wilkinson power dividers to create a complex reflection coefficient detector [14]. By using five Wilkinson power dividers, he was able to implement the detector on a much smaller scale. D. Harty also provides recent research within the design of Wilkinson power dividers. His work provides a novel design of a wideband Wilkinson power divider for a ribcage-dipole array [15].

Chapter 2 further explores the work of others in the design of power dividers specifically the Wilkinson power divider and its design methodology. The Wilkinson power divider provides large bandwidth to a system with multiple designs.

1.7 Work Performed

The tasks performed and discussed in this thesis are the design and testing of a wideband Wilkinson Power Divider for the X-band frequency. This module is integrated into a phased array system that is mounted on a small-scale UAV which is being operated by the UASE Laboratory at UND.

Chapter 2 provides the evolution of the power divider and the theory for designing a Wilkinson power divider. The methodology of designing the wideband Wilkinson power divider for UAV application is covered within Chapter 3. The results from simulation and testing are provided in Chapter 4. Chapter 5 presents the conclusions which will briefly sum up the research performed and covers the suggested future work on the project.

CHAPTER 2

WILKINSON POWER DIVIDER PRINCIPLES

2.1. Introduction

The Wilkinson power divider is a variation of power dividers that uses a microstrip design and allows for the low loss division of a signal N-ways. This section with look into the evolution of the power divider into the Wilkinson design and will discuss the theory behind the design of the power divider.

2.2. Definitions

Before further delving into power divider in general and the Wilkinson power divider in particular, several definitions should be expressed to avoid confusion. The scattering parameters, which is also called the S-parameters, describe the behavior of networks, such as dividers and couplers. S-parameters are provided in an $M\ x\ M$ matrix for an M-port network. A general description of a single S-parameter is given in Equation 2.1 where *i* is the row number and *j* is the column number.

$$S_{ij} = \frac{b_i}{a_j} \tag{2.1}$$

b_i is the voltage leaving *i* port and a_j is the incident voltage at *j* port.

Throughout the theory, the reflection coefficient will be used in the evaluation of the power dividers. The reflection coefficient is commonly given as Equation 2.2

$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2.2}$$

where Z_L is the load impedance and Z_0 is the line characteristic impedance. The reflection coefficient is used to provide the anticipated reflection of the signal back towards the source from the load. When *i=j* in the S-parameters, the resulting parameter provides the reflection coefficient for the network.

Quarterwave impedance transformers are used in the design of the Wilkinson power divider and are a length of transmission line which is exactly a quarter of a wavelength long. In the design of the power divider, these types of impedance transformers were used. For the transformer, the impedance is found by Equation 2.3.

$$Z_T = \sqrt{(Z_i Z_L)} \quad , \quad Z_i = \frac{Z_T^2}{Z_L} \tag{2.3}$$

Where Z_T is the transformer line impedance, Z_i is the input impedance which is typically used as the characteristic impedance or Z_0, and Z_L is the load impedance.

For a planar design, microstrip lines may be used to form a transformer. When designing a microstrip line, it is important to decrease the losses that sharp corners create. In order to perform this, the angles can be mitered or chamfered. Figure 4 provides a visual representation of how to calculate the required chamfer for the angle [16].

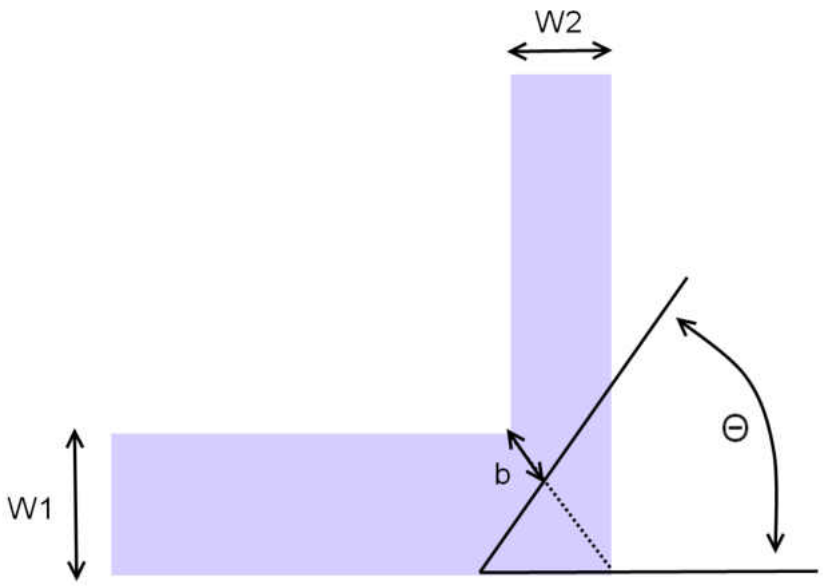

Figure 4: Mitering Right Angles

Using the variables found in Figure 4, Equations 2.4 – 2.5 will provide the values needed to successfully chamfer the angle and reduce losses.

$$\theta = \tan^{-1}\left(\frac{W_1}{W_2}\right) \tag{2.4}$$

$$b = 0.4\sqrt{(W_1^2 + W_2^2)} \tag{2.5}$$

Where *W* is the width of each microstrip line entering the right angle. Figure 4 shows which width is attributed to which transmission line.

2.3. Power Divider History

Power dividers were first discovered in the Massachusetts Institute of Technology (MIT) Radiation Laboratory back in the 1940s. During several experiments, waveguide couplers and power dividers were characterized and invented [17]. The T-junction power divider from the research of this thesis provides a power division for a 3-

port network. This 3-port design can be repeated multiple times to provide an N-way division.

The T-junction power divider is a simple three-port network typically with two outputs and one input, but the reverse can be also be applied for power combining. Figure 5 provides a visual representation of power division and combination [18].

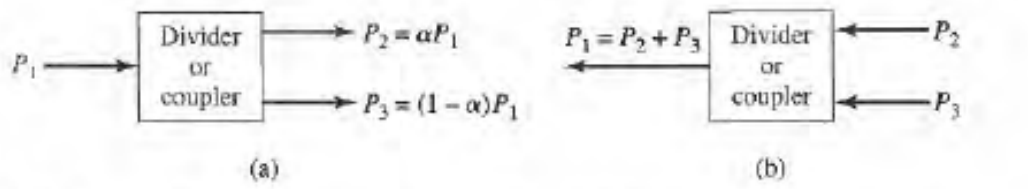

Figure 5: Basic Concept for (a) Power division, (b) Power Combining [18]

α is the ratio of the first output power to input power. The equation representation of the α parameter in Figure 5 is given in Equation 2.6.

$$\alpha = \frac{P_3}{P_1} \tag{2.6}$$

The scattering matrix for this 3-port network has nine independent elements (Equation 2.7):

$$[S] = \begin{bmatrix} S_{11}S_{12}S_{13} \\ S_{21}S_{22}S_{23} \\ S_{31}S_{32}S_{33} \end{bmatrix} \tag{2.7}$$

Ideally, a power divider would be lossless, reciprocal, and matched at all ports. In order to create a lossless three-port with no anisotropic materials, the scattering matrix must be not only unitary and reciprocal but also symmetric which would provide the following matrix (Equation 2.8) [19].

$$[S] = \begin{bmatrix} 0 & S_{12}S_{13} \\ S_{12} & 0 & S_{23} \\ S_{13}S_{23} & 0 \end{bmatrix} \tag{2.8}$$

The matrix should meet the following conditions (Unitary):

$$\sum_{k=1}^{N} S_{ki}S_{kj}^{*} = 1, \quad \text{for } i = j \tag{2.9}$$

$$\sum_{k=1}^{N} S_{ki}S_{kj}^{*} = 0, \quad \text{for } i \neq j \tag{2.10}$$

If these conditions are expanded with the reciprocal matrix shown in Equation 2.7, the following conditions are created (Equations 2.11-2.16):

$$|S_{12}|^2 + |S_{13}|^2 = 1 \tag{2.11}$$

$$|S_{12}|^2 + |S_{23}|^2 = 1 \tag{2.12}$$

$$|S_{13}|^2 + |S_{23}|^2 = 1 \tag{2.13}$$

$$S_{13}^{*}S_{23} = 0 \tag{2.14}$$

$$S_{23}^{*}S_{12} = 0 \tag{2.15}$$

$$S_{12}^{*}S_{13} = 0 \tag{2.16}$$

where $|S_{ij}|$ is the magnitude of S_{ij}. Analyzing these conditions, there is a direct conflict between the equations. In order to satisfy Equations 2.14-2.16, there must be at least two zero valued parameters which would conflict with Equations 2.11-2.13. Thus, it is apparent that it is impossible to make a lossless and reciprocal 3-port network that is matched at all ports. However, if one of these conditions is neglected, then the other two can be met [18].

Because of this compromise, there are three commonly used passive three-port power dividers: the T-junction, resistive, and Wilkinson dividers. Each design brings a

specific compromise which in turn provides distinct advantages and disadvantages to each.

The T-junction is a versatile yet simple three-port power divider. Sacrificing matching, this network provides a lossless system aside from transmission line loss. Figure 6 provides a transmission line model of the T-junction.

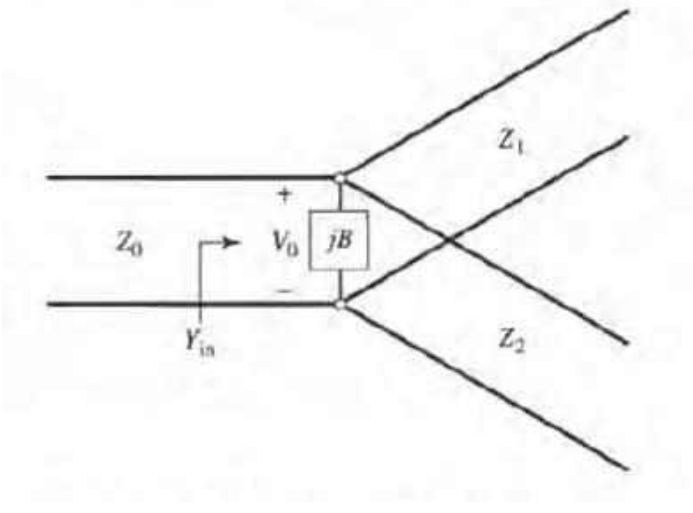

Figure 6: Transmission Line Model of T-Junction Divider [18]

Stored energy from fringing fields and discontinuity at higher order modes at the junction create stored energy or lumped susceptance, *B*, which is the imaginary part of the admittance.

The resistive power divider provides the ability to match all the ports while sacrifices isolation and uses lossy lumped-element resistors. Figure 7 displays a resistive power divider that uses lumped-element resistors.

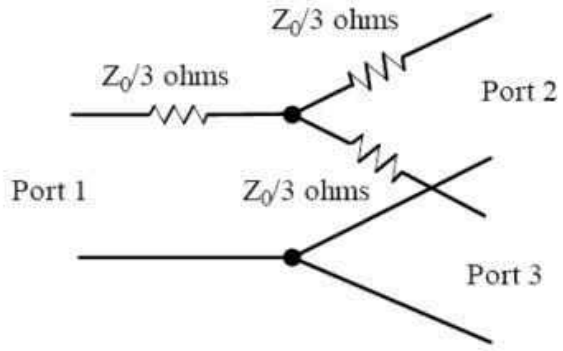

Figure 7: Resistive Power Divider [19]

The input power into the divider is given in Equation 2.17. Additionally, the output power are equal and given in Equation 2.18.

$$P_{in} = \frac{1}{2}\frac{V_1^2}{Z_0} \tag{2.17}$$

$$P_2 = P_3 = \frac{1}{2}\frac{(\frac{V_1}{2})^2}{Z_0} = \frac{1}{8}\frac{V_1^2}{Z_0} = \frac{1}{4}P_{in} \tag{2.18}$$

where V_1 is the voltage at port 1. This equation shows that the two output powers are a quarter of the input power and have dissipated the input power by half. This is a large loss of power through the network and is a large disadvantage of the resistive power dividers [18].

The final passive three-port power divider is the Wilkinson power divider. Discovered in 1960 by Ernest Wilkinson, the Wilkinson power divider is treated as a lossless network that uses a resistor to match the ports [12]. It uses quarter-wavelength transformers to match the output ports to the input port. Figure 8 shows a Wilkinson power divider in microstrip form and its transmission line model where Z_0 is the characteristic impedance.

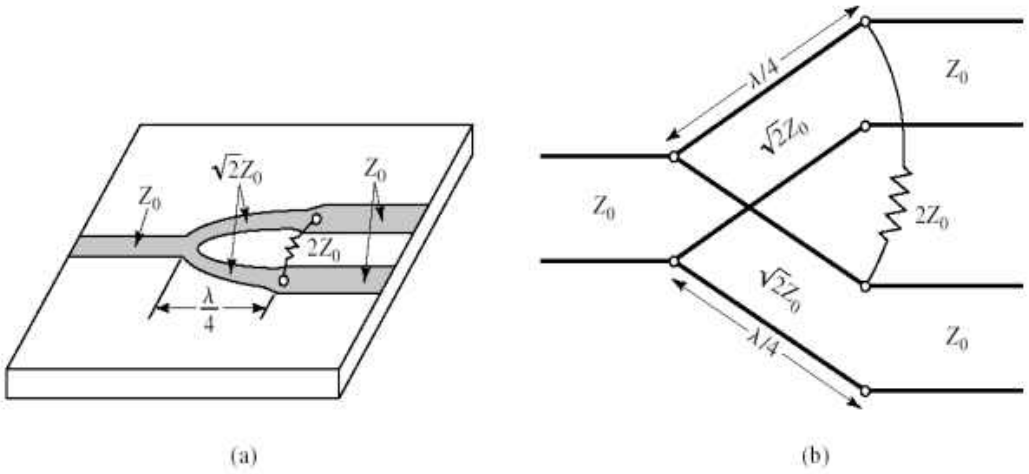

Figure 8: The Wilkinson Power Divider: (a) An Equal-Split Wilkinson Power Divider in Microstrip Form, (b) Equivalent Transmission Line Circuit [18].

When the network is matched at all ports, the Wilkinson divider has all three network characteristics: low loss, reciprocal, and matched. It is impossible to achieve all three characteristics but the Wilkinson power divider uses lossless quarterwave impedance transformers and each division has an inherent -3dB loss, due to dividing the power by a factor of 2. The Wilkinson power divider is lossless when the output ports are matched and balanced but when there is a reflected wave, the Wilkinson will have lossy characteristics. Because of this, the Wilkinson power divider provides the best results for passive power dividers. The following table provides a brief summary of the three passive power dividers.

Table 1: Passive power dividers

Power Divider	Lossless	Matched Ports	Reciprocal
T-junction	Yes	No	Yes
Resistive	No	Yes	Yes
Wilkinson	Lossy only for reflected wave	Yes	Yes

2.4. Design Procedure

The Wilkinson power divider's lossless quarterwave impedance transformers have a characteristic impedance of $\sqrt{2}Z_0$ to match the ports and a lumped resistor of $2Z_0$ to assist with isolation. These attributes allow for a high isolation between the two output ports [12].

In order to analyze the S-parameter matrix for the Wilkinson power divider, the even-odd mode analysis must be performed [18]. Using superposition, the network can be split into two symmetrical modes, even and odd. The transmission line model of the network is normalized to the character impedance, Z_0. The circuit is as shown in the Figure 9.

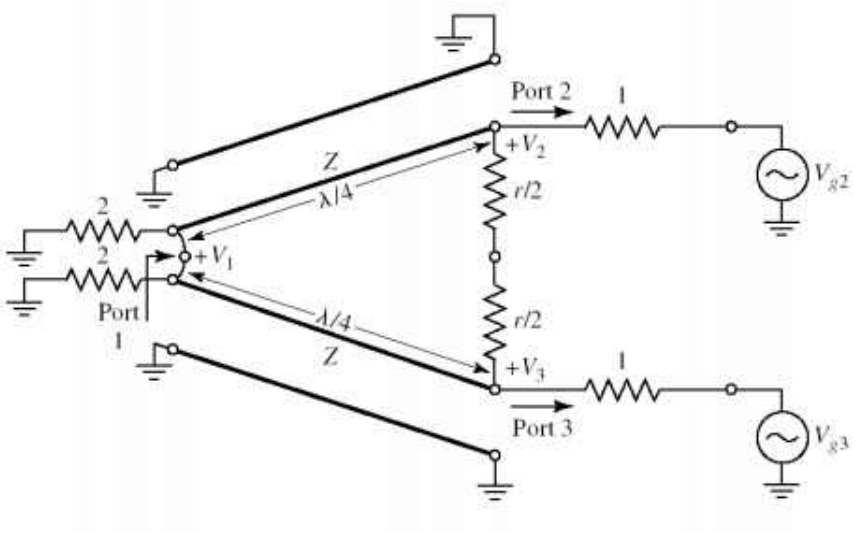

Figure 9: The Wilkinson Power Divider Model in Normalized and Symmetric Form. [18]

In order to provide symmetry the single input resistor whose value is 1 after normalization is split into two parallel resistors which have the value of 2. Additionally, the quarterwave transformer normalized impedance is *Z* and the normalized resistor value is *r* as shown in Figure 9.

The even and odd modes are defined as (Figure 9):

$$V_{g2}^{e} = V_{g3}^{e} = 2V_0, \text{ for even mode} \tag{2.19}$$

$$V_{g2}^{o} = -V_{g3}^{o} = 2V_0, \text{ for odd mode} \tag{2.20}$$

Using superposition, it is found that $V_{g2} = V_{g2}^{0} + V_{g2}^{e} = 4V_0$ and $V_{g3} = 0$. Taking these two values the S parameters can be derived. Because of the short circuit at Port 1, current does not flow between the parallel resistors. The circuit can then be split and treated as two separate modes, even and odd [18].

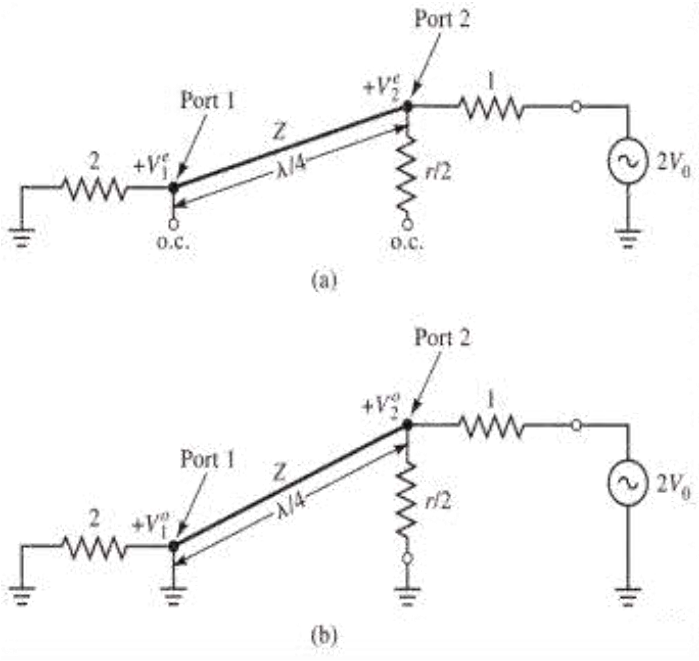

Figure 10: Bisection of Wilkinson Power Divider: (a) Even-Mode Excitation, (b) Odd-Mode Excitation [17].

Looking toward the ground from Port 2 in Figure 10a and applying the values $Z_L = 2$ and $Z_T = Z$ into Equation 2.3, the even-mode has an input impedance of

$$Z_{in}^{e} = \frac{Z^2}{2} \tag{2.21}$$

where Z_{in}^{e} is equal to 1 for matched condition. The ports are matched when the normalized line impedance, *Z* in Equation 2.21, is equal to $\sqrt{2}$ and thus Z_{in}^{e} becomes equal to 1. The transmission line voltage for the network is found to be:

$$V(x) = V^{+}(e^{-j\beta x} + \Gamma e^{j\beta x}) \tag{2.22}$$

where Γ is the reflection coefficient and β is the phase constant and is equal to $\frac{2\pi}{\lambda}$ for lossless line. Assuming *x* = 0 at port 1 and *x* = -λ/4 at port 2 where λ is the wavelength of the transmission line, the port voltages are found to be, where $\beta x = \frac{2\pi}{\lambda}\,\frac{\lambda}{4} = \frac{\pi}{2}$:

$$V_2^{e} = V\left(-\frac{\lambda}{4}\right) = jV^{+}(1-\Gamma) = V_0 \tag{2.23}$$

$$V_1^e = V(0) = V^+(1+\Gamma) = jV_0\frac{\Gamma+1}{\Gamma-1} \tag{2.24}$$

The reflection coefficient is observed at Port 1 in Figure 10a. The values found for Z_0 and Z_L are substituted into Equation 2.2 which gives the reflection coefficient as:

$$\Gamma = \frac{2-\sqrt{2}}{2+\sqrt{2}} \tag{2.25}$$

Thus

$$V_1^e = -jV_0\sqrt{2} \tag{2.26}$$

The odd-mode shown in Figure 10b has an input impedance of

$$Z_{in} = \frac{1}{2}(\sqrt{2})^2 = 1 \tag{2.27}$$

when matched. The voltages of the odd-mode branch are $V_2^o = V_0$ and $V_1^o = 0$.

Figure 11a is the resulting circuit when Port 2 and 3 are matched. Looking at the circuit, it is noted that $V_2^0 = V_3^0$ thus there will be no current flow through the normalized resistor therefore it can be removed as shown in Figure 11b. The input impedance at Port 1 can now be found as

$$Z_{in}^0 = \frac{(\sqrt{2})^2}{2} = 1 \tag{2.28}$$

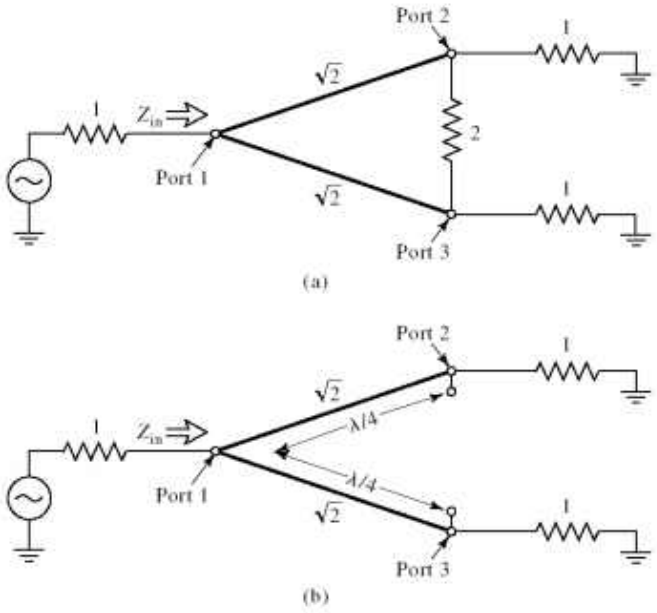

Figure 11: Analysis of the Wilkinson Divider To Find S11: (a) Terminated Wilkinson Divider, (b) Bisection of the Circuit in (a) [17].

Taking the results found through the even-odd mode analysis, the following S parameters can be derived.

$$S_{11} = 0 \tag{2.29}$$

$$S_{22} = S_{33} = 0 \tag{2.30}$$

$$S_{12} = S_{21} = \frac{V_1^e + V_1^o}{V_2^e + V_2^o} = -j/\sqrt{2} \tag{2.31}$$

$$S_{13} = S_{31} = -j/\sqrt{2} \tag{2.32}$$

$$S_{23} = S_{32} = 0 \tag{2.33}$$

These parameters explain the nature of the Wilkinson power divider. When the network is driven by port 1 with the ports matched, the resistor does not dissipate any power, thus the network is a lossless network. The resistor only dissipates reflected power from ports 2 and 3 [17]. The resulting S-parameter matrix is given as:

$$[S] = -\frac{j}{\sqrt{2}}\begin{bmatrix} 0 & 1 & 1 \\ 1 & 0 & 0 \\ 1 & 0 & 0 \end{bmatrix} \tag{2.34}$$

2.5. Coupling and Isolation

The Wilkinson power divider has multiple measurement parameter values that help quantify the efficiency of the network. Equations 2.35-2.37 give the return loss at Input Port 1 and Output Port 2 ($RL_1[dB]$ and $RL_2[dB]$), coupling between Ports 1 and 2 ($CP_{12}[dB]$), and the isolation between Ports 2 and 3 ($IL_{23}[dB]$), respectively [15][20].

$$RL_1[dB] = -20\ log|S_{11}| \quad , \ RL_2[dB] = -20\ log|S_{22}| \tag{2.35}$$

$$CP_{12}[dB] = -20\ log|S_{12}| \tag{2.36}$$

$$IL_{23}[dB] = -20\ log|S_{23}| \tag{2.37}$$

It is important to note that the return loss is the absolute dB measurement of the reflection coefficient since $\Gamma = S_{11} = S_{22}$. These measurements are typically determined through simulation or testing of a power divider on a vector network analyzer. Using a simulator, an example of a graphical representation of these measurements are shown in the Figure 12.

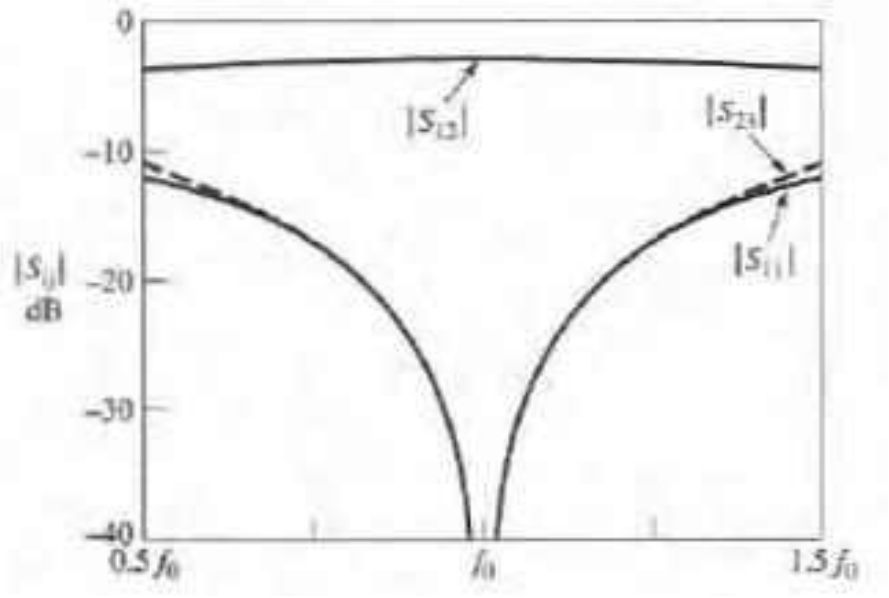

Figure 12: Power Divider Characteristics Example [17]

In Figure 12, the characteristics of the power divider are shown in dB scale. Each line is identified and is measured across an operating frequency, f_0. The coupling between Ports 1 and 2, S_{12}, is close to -3 dB which is the inherent power loss with each division. Additionally, the return loss and the isolation between the output ports, have a drop at the operating frequency.

2.6. Straight Split and Circular Split

Single stage planar Wilkinson power dividers have two commonly used designs: straight split and circular split designs (Figure 13). The circular Wilkinson power divider is smaller in size than the straight Wilkinson power divider. In Chapter 3 a sample design of both single stage, single split models will be given and the simulated results will be discussed [21].

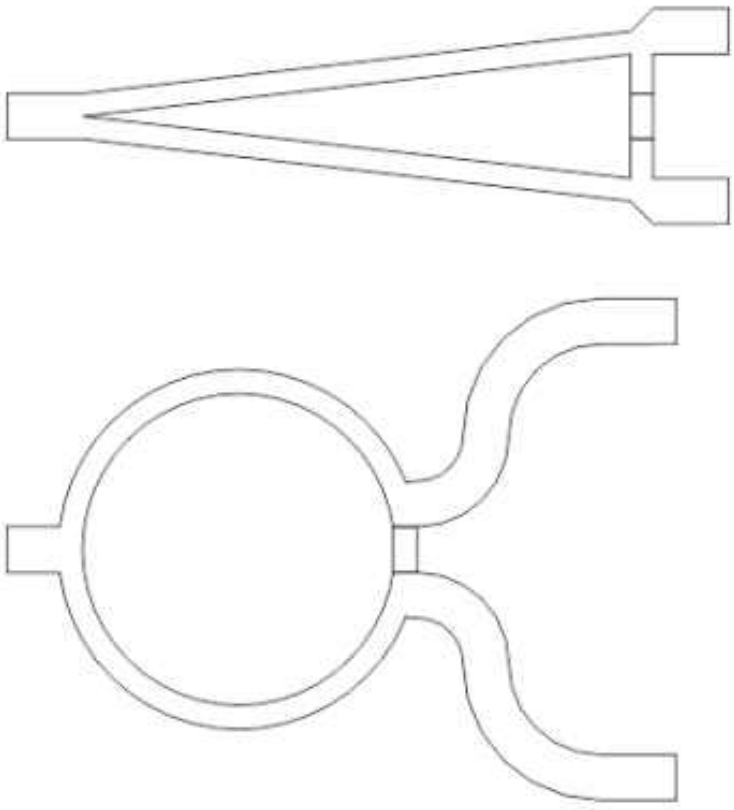

Figure 13: Straight and Circular Wilkinson Power Divider [15]

2.7. Multistage Wilkinson Power Divider

Adding multiple stages of quarter wavelength transformers within the network allows for a larger bandwidth of operation. The bandwidth can be increased to include over a decade of frequency which allows for a wide use of components [22]. In order to design a multistage Wilkinson, the even-odd method is again utilized but instead of a single stage, multiple stages are observed [13].

A general schematic for an N-stage Wilkinson power divider is given in Figure 14.

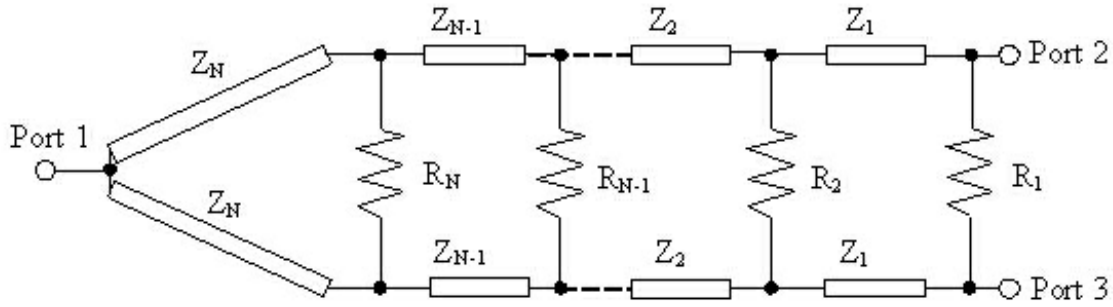

Figure 14: Multistage Wilkinson Power Divider Schematic [13]

As with the single stage divider, the even mode is created by assuming that Ports 2 and 3 are in-phase thus negating the voltage across the isolation resistors which allows for the resistors to be ignored. The odd mode has the excitations 180˚ out of phase and a virtual ground is placed across the axis of symmetry. The even and odd segments for analysis are as follows respectively:

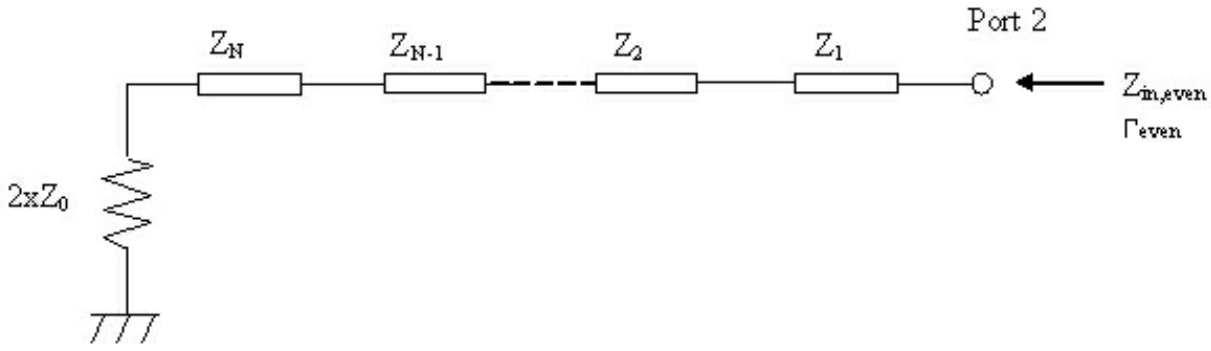

Figure 15: Even Mode Multistage Wilkinson [13]

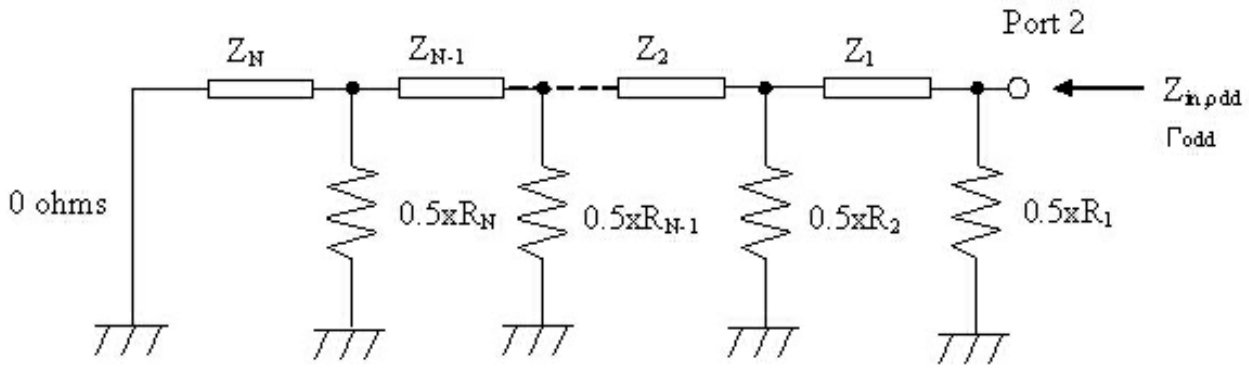

Figure 16: Odd Mode Multistage Wilkinson [13]

Note that in the odd mode, the resistors are halved.

From the even-odd mode, the reflection coefficients can be calculated, but first the impedance from the input must be defined using the transformer equation [23]. For a lossless case and looking towards the ground from Port 2, the input impedance is found as:

$$Z_{in} = \frac{Z_L + jZ_0 \tan(\beta l)}{Z_0 + jZ_L \tan(\beta l)} \tag{2.38}$$

where Z_{in} is the input impedance, Z_L is the inductive impedance, Z_0 is the line impedance, l is the length, and β is the phase constant.

Using Equation 2.2, the reflection coefficient for port 1, S_{11}, is found to be the same as the even-mode reflection coefficient while the reflection coefficients for ports 2 and 3, S_{22} and S_{33} respectively, are averaged between the even and odd mode reflection coefficients [13].

$$\Gamma_2 = \Gamma_3 = \frac{(\Gamma_{even} + \Gamma_{odd})}{2} \tag{2.39}$$

If it is assumed that the network is lossless to provide ease of design before optimization, the transmission coefficient between the input port and the output ports can be calculated using the reflection coefficients. The isolation between the output ports is half of the difference between the two modes' reflection coefficients.

$$|t_{21}| = |t_{31}| = \sqrt{\frac{1}{2}(1 - \Gamma_e)^2} \tag{2.40}$$

$$t_{23} = \frac{(\Gamma_{even} - \Gamma_{odd})}{2} \tag{2.41}$$

where *t* is the transmission coefficient with the subscripts representing the network ports.

The input reflection coefficient was solved using Chebyshev polynomials. The coefficient is not a function of the isolation resistors which means that it is a function of line impedances [23].

2.8. Design Considerations

There are several considerations that were necessary to contemplate while looking into the design of the power divider. The system that was being integrated into required the divider to operate over 10 GHz. Additionally, the system was to be utilized by UAVs which requires size constraints to be considered during the modeling.

The X-band was chosen as an operating frequency. There were three main reasons the X-band was chosen. First, the previous system modules were designed for this band. Secondly, commercial off-the-shelf phase shifters were most readily available

within this frequency band. Lastly, the X-band frequency provides an inherent small form-factor that the wavelengths can accommodate.

Working at a high frequency brought several other considerations that were necessary during development. The selection of the substrate material was critical to the successful operation of the system. Further discussions on the design considerations will be in Chapter 3.

2.9. The System Overview

The phased array radar system consists of several modules that must be integrated successfully together. This requires understanding of their operation at the design stage and careful calibration at the implementation stage. The system consists of a power divider, phase shifter module, control PCB, and a Vivaldi antenna array. This system must be small enough to easily fit into the UASE Super Hauler. The following section discusses the phased array radar principles.

2.10. Phase Array Radar Principles

In a phased array system a signal is generated at the system's operating frequency. This frequency goes through a power divider to provide N number outputs that match the number of array elements. After the division, the signals are sent through a transmit module. The module delays each signal which in principle "phase shifts" the signals. After the phase shift, the signal is amplified then sent to the array of antennas. The following figure provides a general overview of the process.

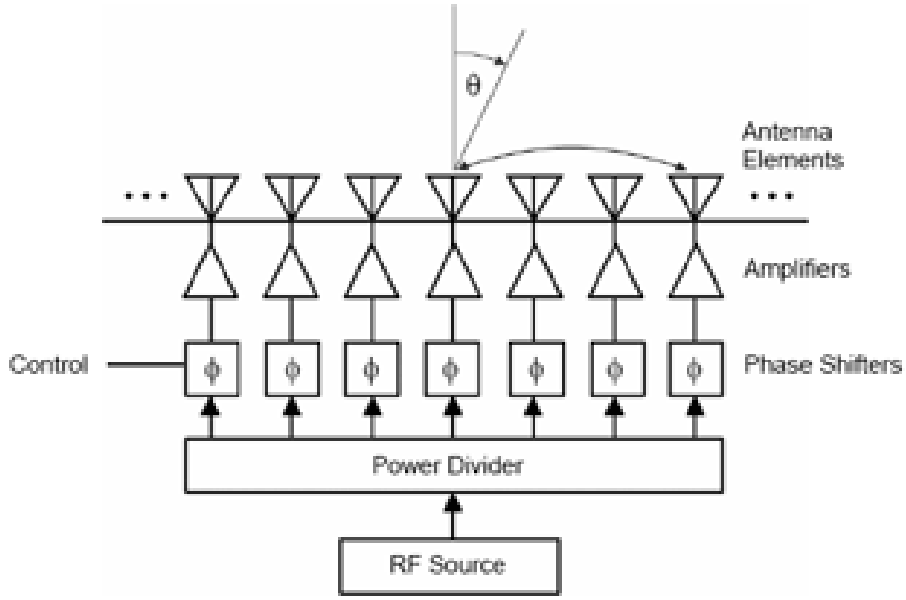

Figure 17: Phased Array Block Diagram [24]

The phased array radar system should also receive the back scatter signals from objects of interest. Figure 17 shows the transmitting section of the phased array antenna system. A receiving module and data processing component need to be integrated into the entire system to create fully functional phased array radar.

Figure 18 further details the antenna array radiation pattern when phase shifters are utilized.

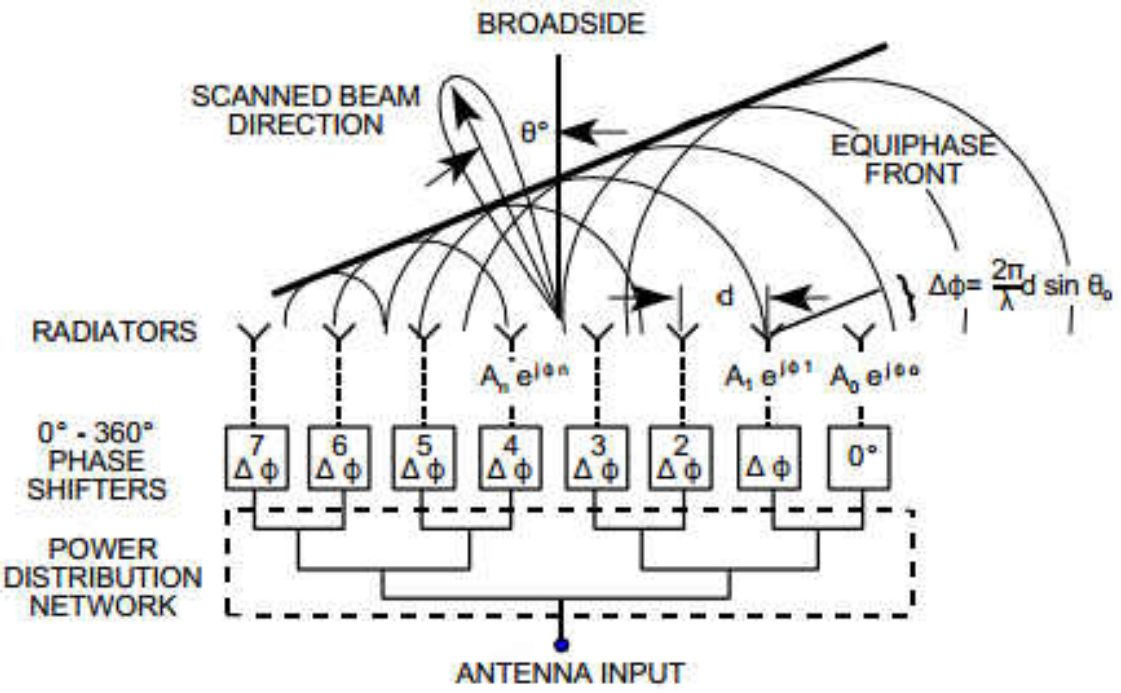

Figure 18: Phased Array Steering [25]

In Figure 18, the broadside angle is at $\theta = 0$ and scanned beam is at $\theta = \theta_0$. If the antennas in the array are equally spaced and their pointing radiation patter are to the same direction, the following equations can be used to calculate the steering angle (Θ_0) and differential phase shift ($\Delta\varphi$), respectively:

$$\Theta_0 = \sin^{-1}\left(\frac{\Delta\varphi\lambda}{2\pi d}\right) = \sin^{-1}\left(\frac{\Delta\varphi}{\beta d}\right) \tag{2.40}$$

$$\Delta\varphi = \frac{2\pi}{\lambda} \cdot \sin(\Theta_0) \tag{2.41}$$

In which λ is the operating frequency, *d* is the distance between each antenna element, Θ_0 is the steering angle, and $\Delta\varphi$ is the differential phase shift for a uniform array of isotropic elements. The achievable scan angle can be found as a function of the differential phase shift if the operating frequency is constant [27].

The proposed system is using digital phase shifters which allow for a rapid state change in the phase shifters, thus providing quick scanning capabilities. Because of the speed of scanning capability, phase array systems are an extremely viable design for radar applications.

CHAPTER 3

METHODOLOGY

3.1. Phased Array Radar Requirements

As mentioned in Chapter 2, the system was designed to operate at 10 GHz or the X-band frequency with a bandwidth of 2 GHz. Working at a high frequency poses several design constraints that have to be taken into account, specifically the choice of a substrate material. Thick substrates with a low dielectric constant are the ideal choice because they are more efficient, but the disadvantage is that the wavelength is larger for low permittivity substrate. Because of this disadvantage, substrates with a high dielectric constant are preferred when size is limited [17][27]. The substrate that was chosen for the Wilkinson power divider was Rogers RT/duroid 6006/6010LM [28]. The high dielectric constant of 10.2 of this substrate provided the ability to shrink the circuit size with a low loss tangent of 0.0023 at 10 GHz. These two factors provide a good substrate material to create a power divider with small dimensions.

The size of the system must be small enough to easily integrate into the UAV. Originally, the system was required to fit inside the payload cavity of the UND UASE's Super Hauler. The bay is approximately 21" x 11" x 12" and can carry approximately 30 pounds.

Figure 19 shows the payload bay with a payload attached at the bottom through quarter-turn locks.

Figure 19: UND UASE Super Hauler Payload Bay

Since it was not possible to scan the beam to angles in front of the airplane without interference with the fuselage and engine, one solution was dropping the system lower than the plane but this risks damaging the system on take off and landings. A better solution was to place the system inside the wing ribs. This caused more restrictions on the size. The cross-section of the wing provided approximately two inches in the thicker section of the wing and around six inches between each rib. The system can be connected with cables that run through the unused hole in the ribs. Figure 20 shows the wing cross-section with the available space.

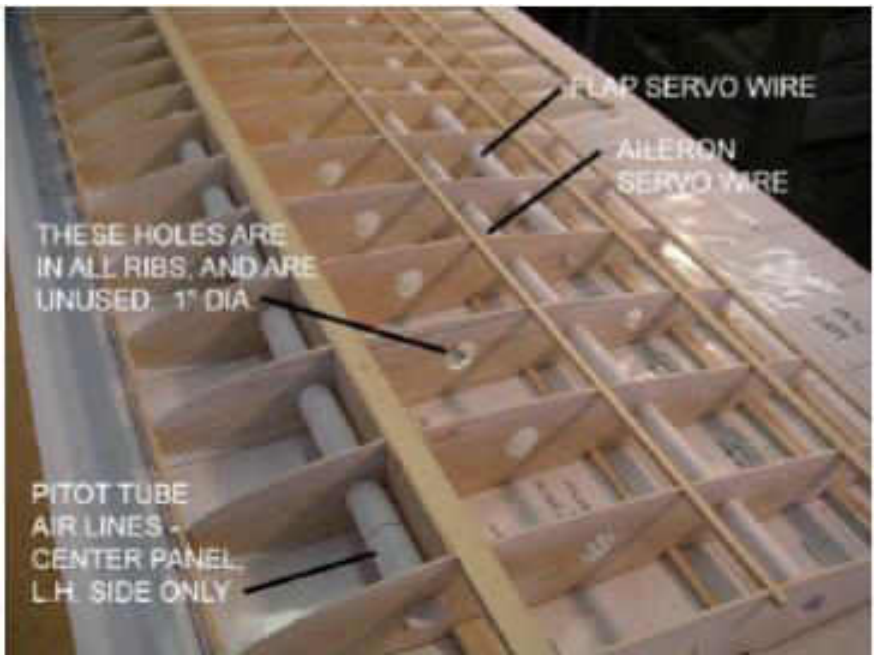

Figure 20: UND UASE Super Hauler Wing Cross-Section [29]

Modifying the wing embedded system; the final system design included a wing mounted pod that would hangs below the wing. The system would still will be attached by cables that are dispersed through the unused hole in the wing's rib but it has less restricted forward looking orientation through the pod. The dimensions of the pod are slightly larger than the wing and the system was designed with the size constraints within the wing, thus it provided ease of transition to the pod design (Figure 21).

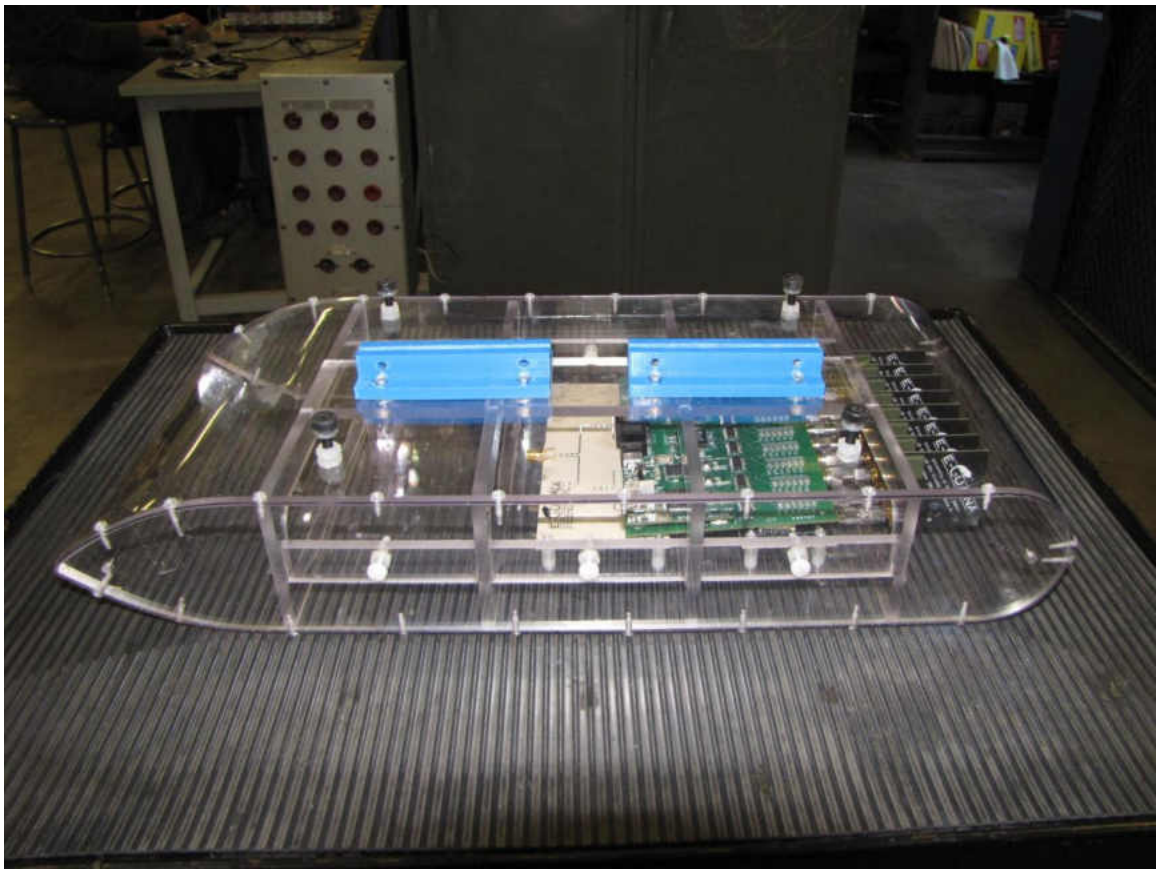

Figure 21: Wing Pod for Phased Array System

3.2. Power Divider Requirements

The desired power divider for integration into the phased array system needs a bandwidth of 2 GHz that is centered at 10 GHz. A single signal needs to be received and a balanced, in-phase 8-way output needs to be produced.

In order to reduce losses of the system and still keep it modular, the Wilkinson power divider must have the ability to directly connect to the phase shifter board. This required the exact spacing of the output ports at a half wave of the operating frequency, or 590 mils. Eight female SMA connectors on the power divider must align perfectly with the eight female connectors on the phase shifter board. A Federal Custom

Cable component with male SMA connectors on both sides and a machined metal sleeve in between them were used to connect the two boards (Figure 22). A torque wrench is used to tighten the connectors to exactly 8 in/lb.

Figure 22: Male to Male SMA Connector

The board width was less than six inches with this design requirement which fits into the size constraints placed on the system by the pod. Additionally, because the operating frequency was high the components had a small size and the entire board was less than half an inch in height.

3.3. Wilkinson Power Divider Variables

The Wilkinson power dividers were designed based on the theory discussed in Chapter 2. Using Equations 2.21 – 2.30, values for each quarterwave impedance transformer were calculated. Agilent Technologies' AppCAD software (Figure 23) was used to find the dimensions of the microstrip [30]. These were used to create a model of the power divider in Ansoft's HFSS software [31]. This software is uses a full-wave analysis to simulate the microwave components taking into account the characteristics

of the substrate material such as the dielectric constant and the thickness of the substrate.

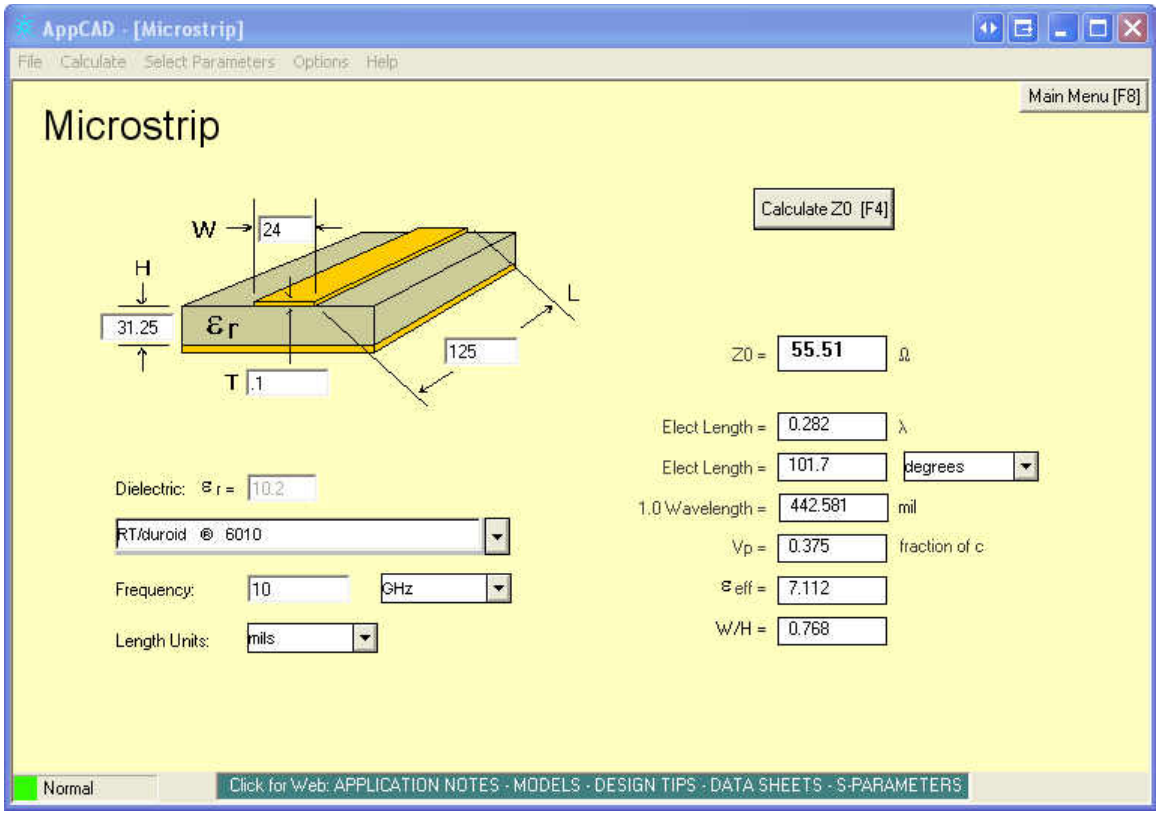

Figure 23: Agilent Technologies AppCAD [30]

Upon designing the multistage Wilkinson power divider, Chevyshev polynomials [17] were used to find the isolation resistors values and the impedance necessary for the quarterwave transformers. These values were imput into the AppCAD software which provided the dimensions for each stage of the transformers. These were then used for setting up a simulation modeled in HFSS.

3.4. Simulation Results

Simulations were performed in Ansoft's HFSS [31]. The power dividers were created on a 31.25 mil Rogers 6010 substrate. A microstrip line was designed given a

Perfect E characteristic which means that the E-field is normal to the selected plane. An infinite ground was considered. An analysis was done at 10 GHz operating frequency with a fast mode frequency sweep across 5-15 GHz to provide extra data beyond the required 2 GHz for analysis. This provided further information on the network's frequency bandwidth.

A circular single split Wilkinson power divider is modeled with the widths and lengths calculated through AppCad software. The width and length results were recorded as variables for the model. By creating variables, the model could easily be modified without having to completely redefine the model. Table 2 provides the values for each dimension as shown in Figure 24.

Table 2: Circular Single Split Variables

In_strip_width (1)	27.5 mil
In_strip_legnth (2)	138 mil
Circle_strip_length (3)	113 mil
Circle_strip_width (4)	14 mil
Circle_slot_width (5)	27.5 mil
Out_strip_width (6)	27.5 mil

Taking these variables, a model was created within the HFSS simulating software. Figure 24 shows how each variables are used in the creation of the model. The numbers next each variable in Table 2 can be found in Figure 24. The entire model is shown in Figure 25.

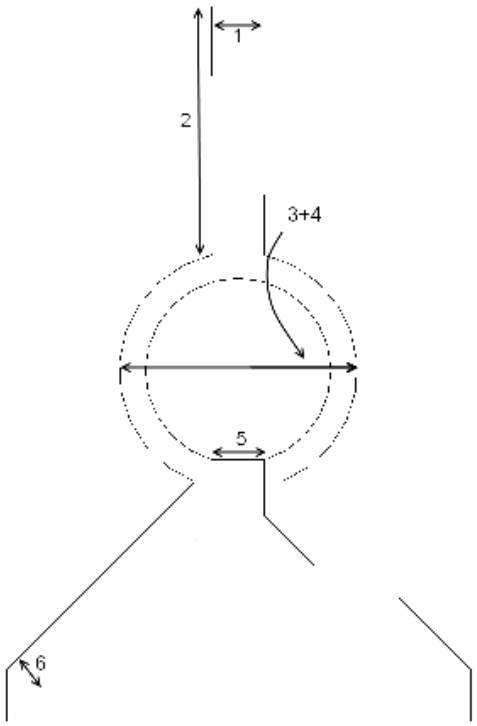

Figure 24: Circular Wilkinson Power Divider with Variables

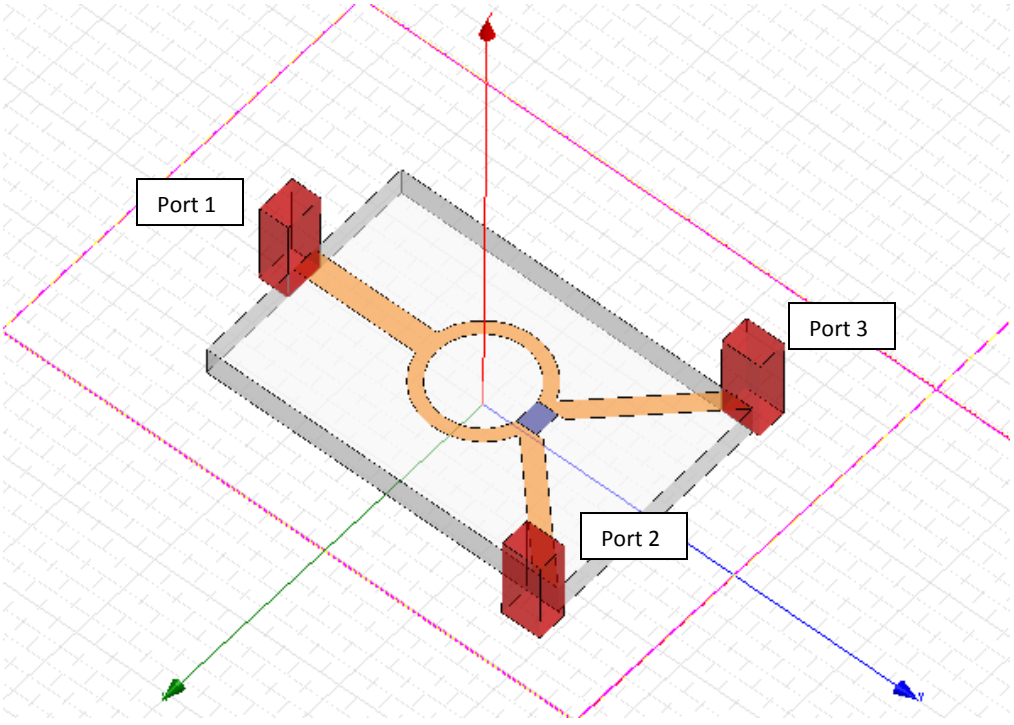

Figure 25: Circular Single Split Wilkinson

Figure 25 shows the substrate, the designed microstrip Wilkinson power divider, the isolator resistor is the gray box, the three boxes that represent port locations, and is surrounded by a box that imitates network surrounding air shown in Figure 25. The Cartesian coordinates are the three arrows pointing out from the center of the figure.

The circular single split was then tested across the desired frequency spectrum to find the return loss and power loss. The results are depicted in Figure 26.

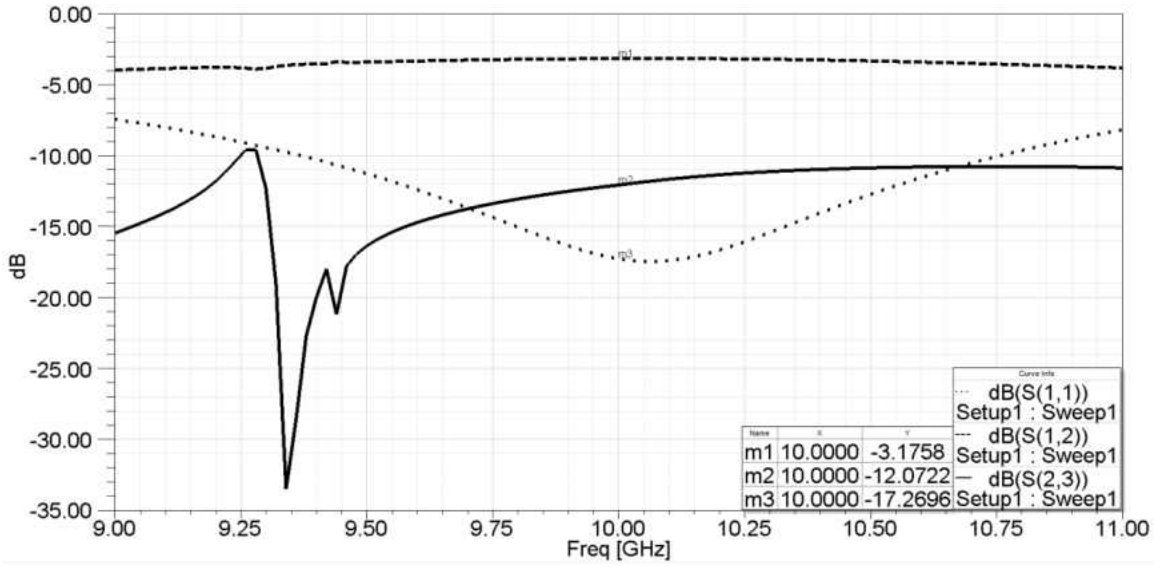

Figure 26: Circular Single Split Wilkinson Results

The circular single split Wilkinson power divider provided a low return loss (m3) of -17.27 dB at 10 GHz frequency which translates into a working power divider (dotted line in Figure 25). The threshold for reflection coefficient (m2) for this system is -9 dB thus the operating bandwidth for this power divider is approximately 1.5 GHz centered around 10.1 GHz. The power loss (m1) across the network is given by the dashed line and is measured as -3.1758. Taking into account the 3 dB division, the power loss is 0.176 dB. Finally, this network does not have the desired -25 dB measurement for isolation between Port 2 and Port 3.

Following the same procedure as the circular single split, a straight single split Wilkinson power divider was also modeled. Taking the values for the impedance quarterwave transformers, the following width and length values were derived with the AppCAD software.

Table 3: Straight Single Split Variables

In_strip_width (1)	27.5 mil
In_strip_legnth (2)	50 mil
Straight_strip_length (3)	301 mil
Straight_strip_width (4)	14 mil
Out_strip_width (5)	27.5 mil

These values are then set within the HFSS software and the straight single Wilkinson split is modeled. Figure 27 shows the use of the variables in the modeling of the Wilkinson power divider. The variables are numbered within Table 3. The final design is shown in Figure 28.

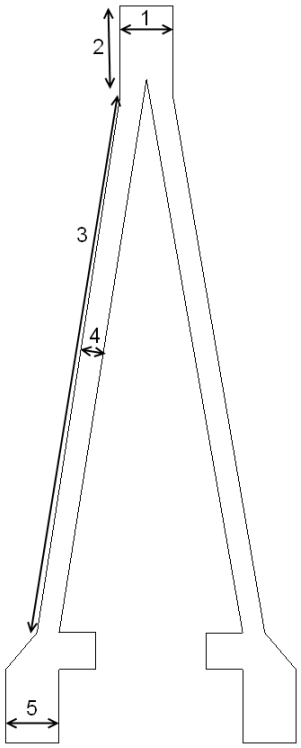

Figure 27: Straight Wilkinson Power Divider Variables

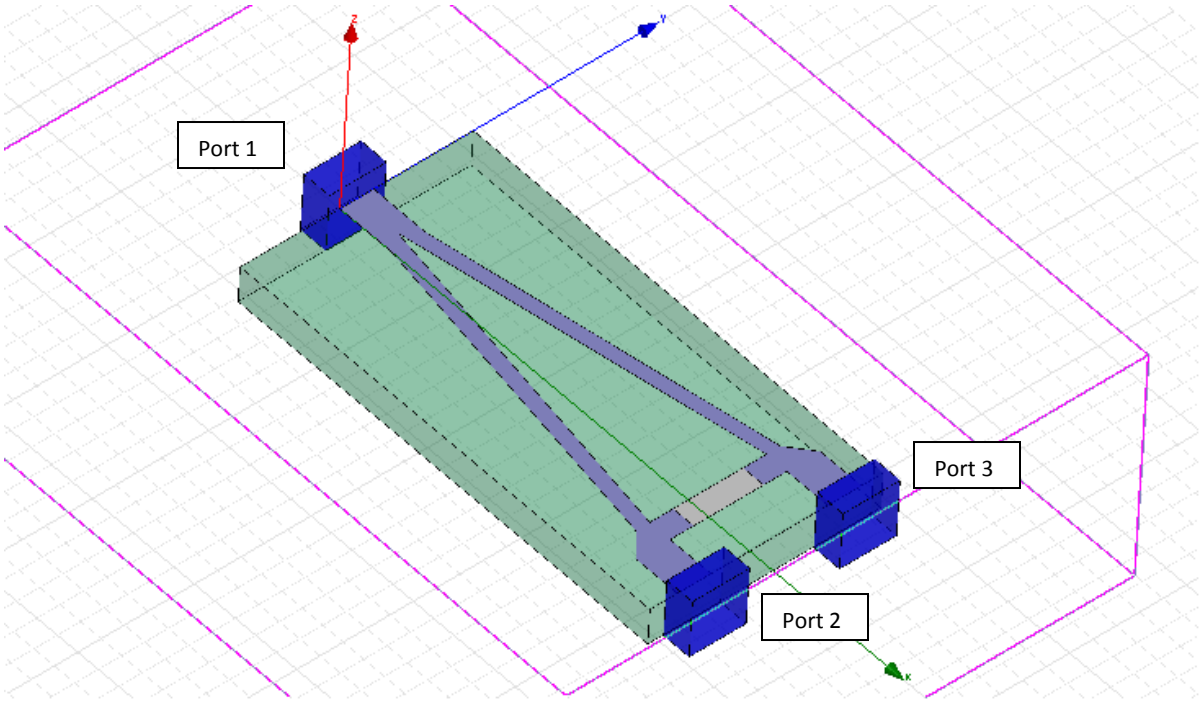

Figure 28: Straight Single Split Wilkinson

Following the same frequency sweep and analysis setup, the straight split is analyzed. In Figure 29, the results are provided. The center frequency has shifted by 0.75 GHz but the operating bandwidth has increased from 1.25 GHz to approximately 2 GHz for that the acceptable reflection coefficient of -9dB. The power loss through the network has increased to 0.46 dB and more importantly, the isolation between ports is reduced to only -5.67 dB.

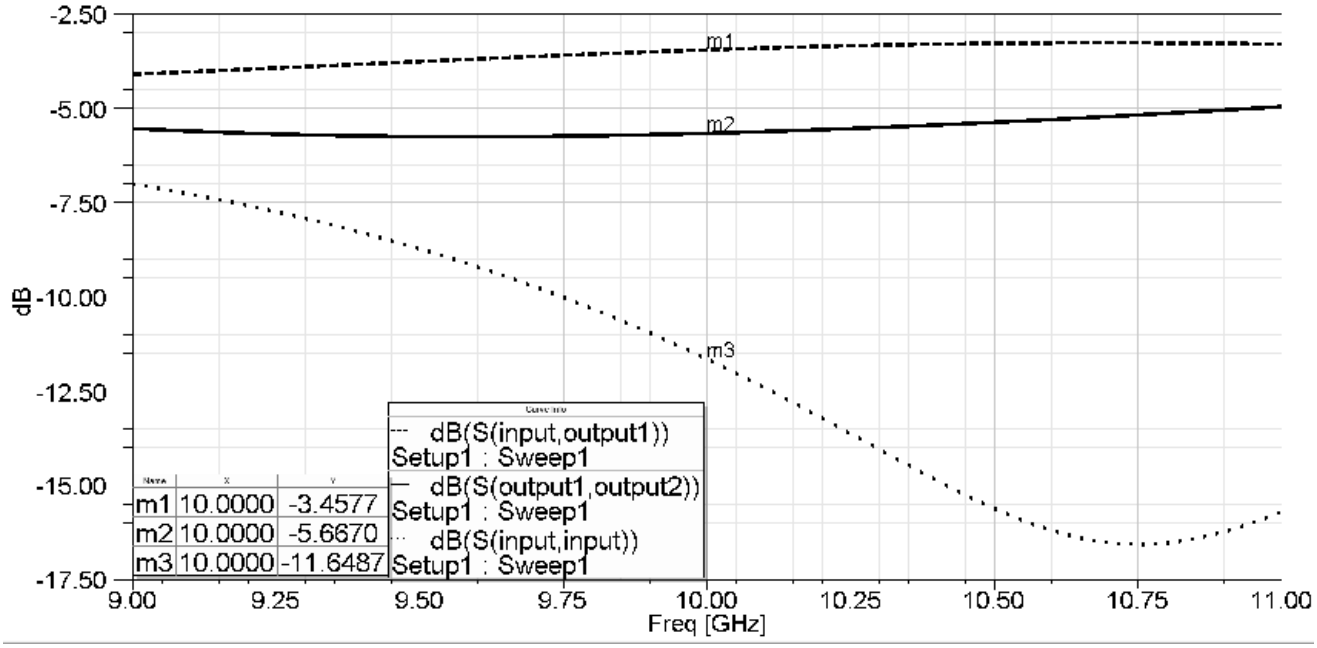

Figure 29: Straight Single Split Wilkinson Results

Both the circular and straight divisions provide an operating power divider across the desired frequency. They also are extremely close to providing the required bandwidth for the system. The straight Wilkinson power divider has larger power loss across the board compared to the circular design. Both designs do not meet the required -25 dB port isolation (m2). Better matching with the isolator resistor would provide better isolation between both output ports. Table 4 provides a comparison of the two designs.

Table 4: Circular and Straight Wilkinson Comparison

	Requirements	Circular Division	Straight Division
Center Frequency	10 GHz	10.1 GHz	10.75 GHz
Bandwidth	2 GHz	1.5 GHz	2 GHz
Power Loss at 10 GHz (for single split)	0.4 dB	0.176 dB	0.46 dB
Port Isolation at 10 GHz	-25 dB	-12.07 dB	-5.67 dB

In both the single stage divisions the required distance of 590 mils between output ports are not met. Additionally, the bandwidth can be increased by increasing the number of stages. Therefore, a multistage Wilkinson power divider was designed. These factors were taken into account in the multistage single split design.

Using Chebyshev polynomials, the following values are found for the isolation resistors and the quarterwave transformers of the multistage power divider design. Note that the Isolation Resistor 1 and Transformer 1 are the closest ones to the output ports.

Table 5: Multistage Power Divider Values

Isolation Resistor 1	1010 Ω
Isolation Resistor 2	143 Ω
Isolation Resistor 3	143 Ω
Isolation Resistor 4	72.5 Ω
Line Impedance for Transformer 1	52.59 Ω
Line Impedance for Transformer 2	62.51 Ω
Line Impedance for Transformer 3	79.98 Ω
Line Impedance for Transformer 4	95.07 Ω

The isolation resistors were modeled within the HFSS software. The quarterwave transformer dimensions were found using AppCad software. Due to the small wavelengths at high frequencies, the values are quite small so the closest round integer was used for the dimensions. Table 6 provides the dimensions found for the transformers with T_width_1 being the transformer closest to the output ports.

Table 6: Multistage Quarterwave Transformer's Line Widths

T_width_1	24 mil
T_width_2	16 mil
T_width_3	8 mil
T_width_4	4 mil

These values were utilized to build a model of the power divider in HFSS, with the center of the output ports being 590 mils apart. In order to avoid the losses that come with sharp edges, a Matlab microstrip chamfer program was used to derive values from Equations 2.4 – 2.5. The resulting design is shown in Figure 30.

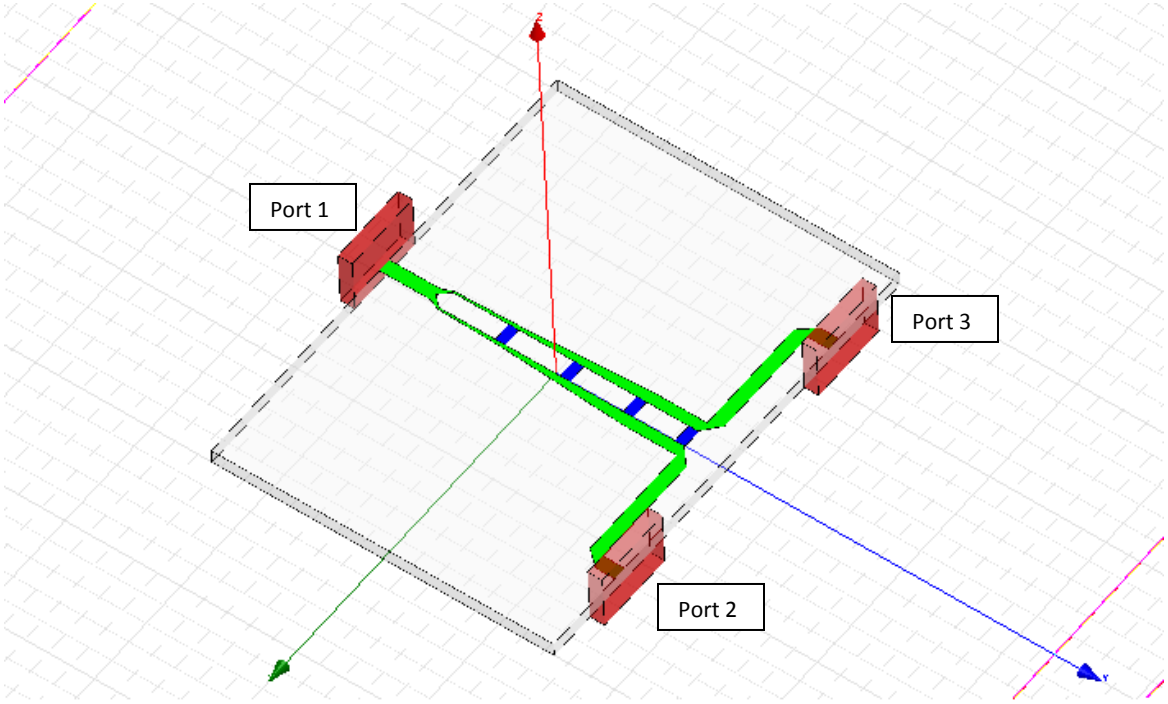

Figure 30: Multisection Single Split Wilkinson

The results from the simulation are provided in Figure 31.

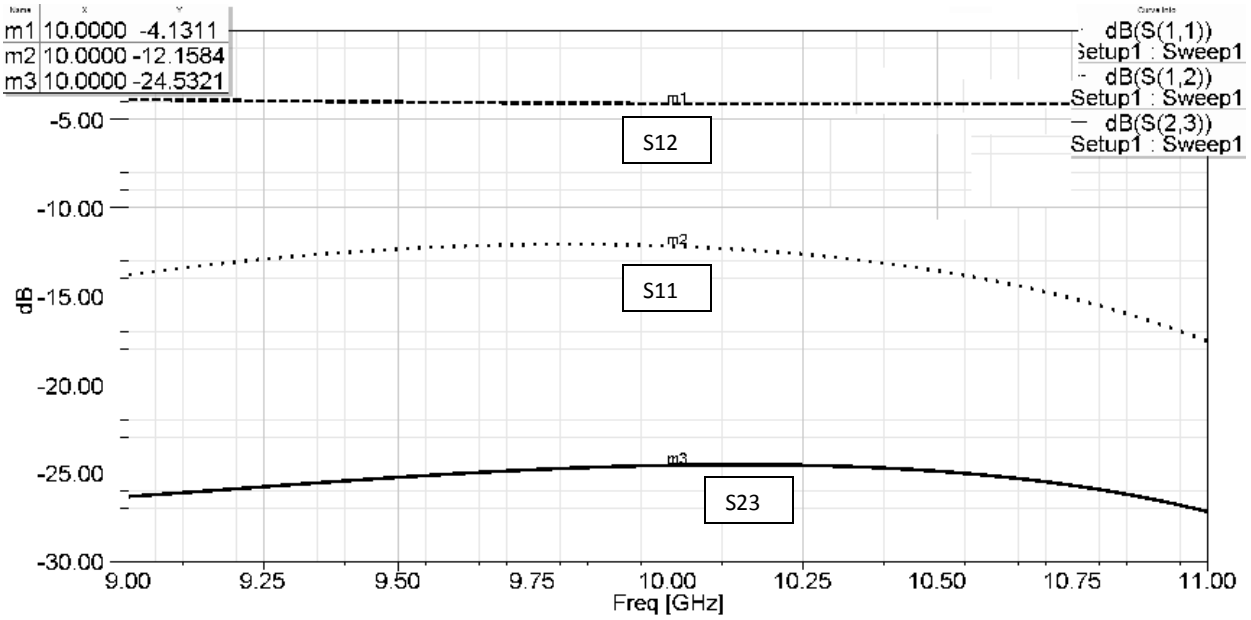

Figure 31: Multisection Single Split Wilkinson Simulation Results

The results from the multisection single division Wilkinson power divider show that the power divider has an operating bandwidth from 9-11 GHz. The reflection coefficient (m2) at Port 1 is -12.16 dB at 10 GHz which is acceptable under the -9 dB threshold. The power loss (m1) from the network is 1.1 dB at 10 GHz which is anticipated with the higher bandwidth. For a single split, commercial power dividers typically have approximately 0.4 dB loss through the network which is the desired power loss. The multistage power divider is the furthest measurement from that value. The port isolation (m3) is not at the desired -25 dB measurement but is extremely close and much better than both single stage power dividers. Because of the narrow analysis of the 9 – 11 GHz frequency sweep, the multistage power divider analysis frequency sweep is increased. Figure 32 shows the results.

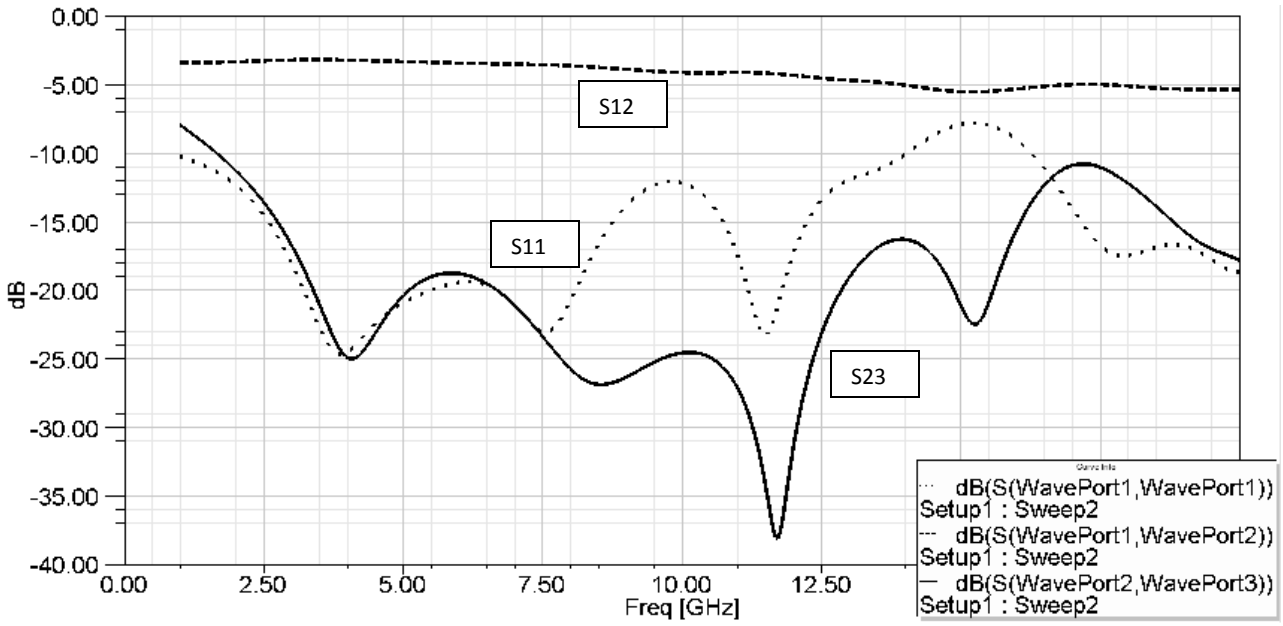

Figure 32: 20 GHz Frequency Sweep Multistage Wilkinson Power Divider

This larger frequency sweep provides more information on the network's performance. The bandwidth of the multistage power divider is over 10 GHz operating from 1 – 14 GHz. There are also visible dips and humps on the reflection coefficient (dotted line) which is a consequence of increasing the stages. To increase bandwidth of the system, the power loss of the network is increased. The low frequencies within the bandwidth have the lowest loss at 0.2 dB loss, and for high frequencies the power loss reaches 2 dB. Finally the port isolation is much better than the single split power dividers across the entire frequency span and it is optimal at 11.5 GHz with -37 dB value.

This design meets two major requirements of the power divider, bandwidth across the desired operating frequency and output ports distanced 590 mils apart. Also, the isolation is extremely close to the requirement. This design is cascaded to provide a corporate feed network. The resulting model can be seen in Figure 33.

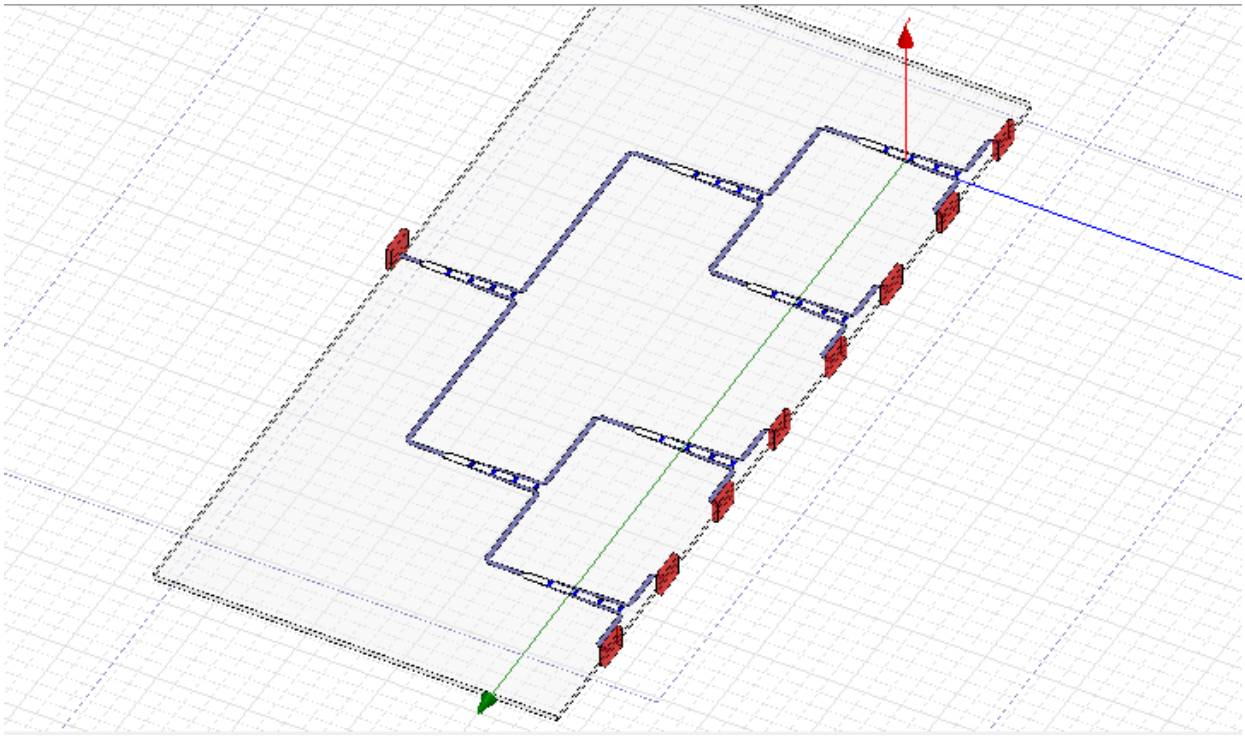

Figure 33: Multistage 8-split Wilkinson Power Divider

The simulation results are given in Figure 34.

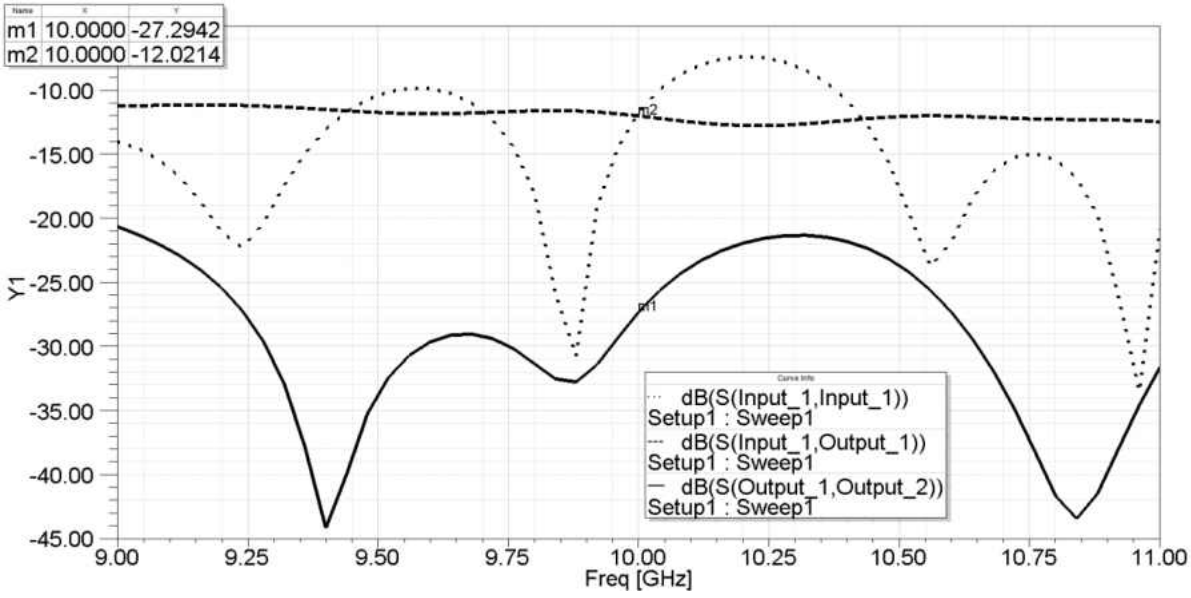

Figure 34: Multistage 8-way Wilkinson Power Divider Simulation Results

The return loss (m2) at 10 GHz is underneath the -9 dB threshold at -12.02 dB with the return loss remaining under the threshold at lower frequencies but a large

hump immediately after 10 GHz breaks this limit. While the return loss (m2) is acceptable, the dip at 9.85 GHz would be best the desired operating frequency of 10 GHz. The power loss across the board is just above -3 dB loss at 10 GHz with the loss varying approximately ±1 dB across the frequency sweep. Finally, Figure 34 shows the port isolation (m1) at -27.3 dB at 10 GHz.

Further simulation provides a larger frequency sweep and better analysis. Figure 35 gives the results.

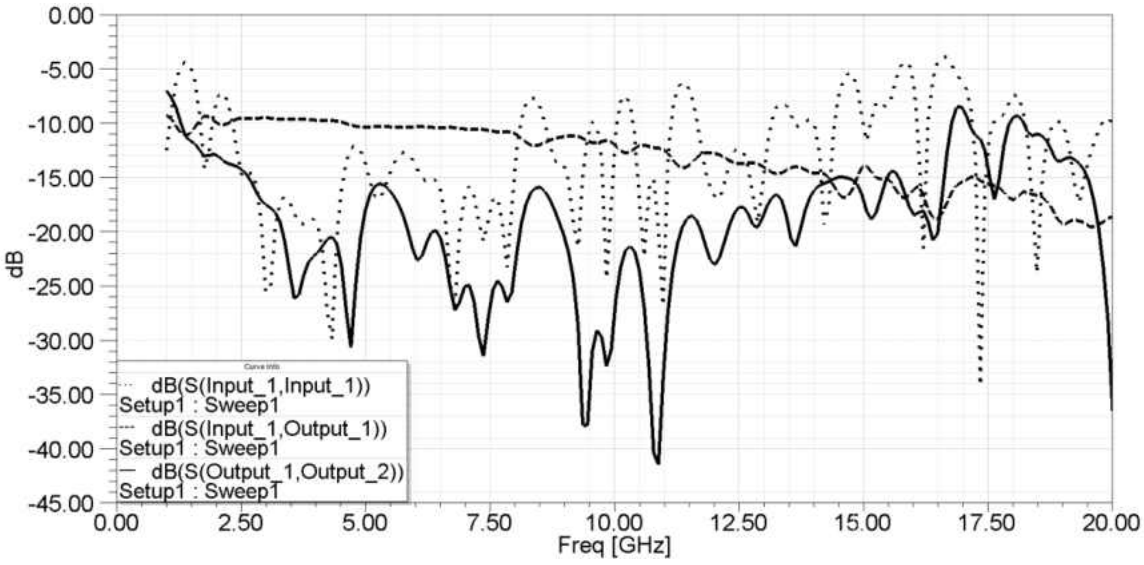

Figure 35: Large Frequency Sweep 8-way Wilkinson Power Divider Simulation Results

There is approximately 1.5 GHz operating bandwidth that includes but is not centered at 10 GHz. From 2.25 – 8.25 GHz there is a large operating bandwidth but this is not including the required frequency. The power loss of the network continually increases as the frequency increases. It ranges from 2 dB to 3 dB loss over the 1.5 GHz bandwidth (note that there is an inherent 9 dB loss from the power divider). Finally, the port isolation is performing as required from 9.2 – 10.1 GHz with large dips and humps

across the entire frequency span. It particularly gets worse at higher frequencies. Table 7 provides an analysis of the simulation compared to the requirements. The power loss and port isolation are taken across the operating bandwidth from 8.5 – 10.1 GHz.

Table 7: Multistage 8-way Power Divider Simulation Analysis

	Requirements	Simulation
Operating Frequency	10 GHz	9.9 GHz
Bandwidth	2 GHz	1.5 GHz
Power Loss	2 dB	2 dB – 3dB
Port Isolation	-25 dB	-17dB – -37 dB

3.5. Fabrication

Due to time constraints for system testing, the simulated multistage Wilkinson power divider was fabricated. CadSoft's Easy Applicable Graphical Layout Editor (EAGLE) was used to draw the PCB layout. Side mounted SMA female connectors were placed at the ports with vias placed in the soldering pads to provide better adhesion with the SMA to the PCB copper [32]. Additionally, the isolation resistors were attached to a soldering pad. RC0402 surface mounted lumped resistors were used because of their small size (0.039" x 0.020" x 0.016"). Because the desired isolator values are not standard, the standard resistors with closest resistances were used [33]. The PCB for the power divider is shown in Figure 36.

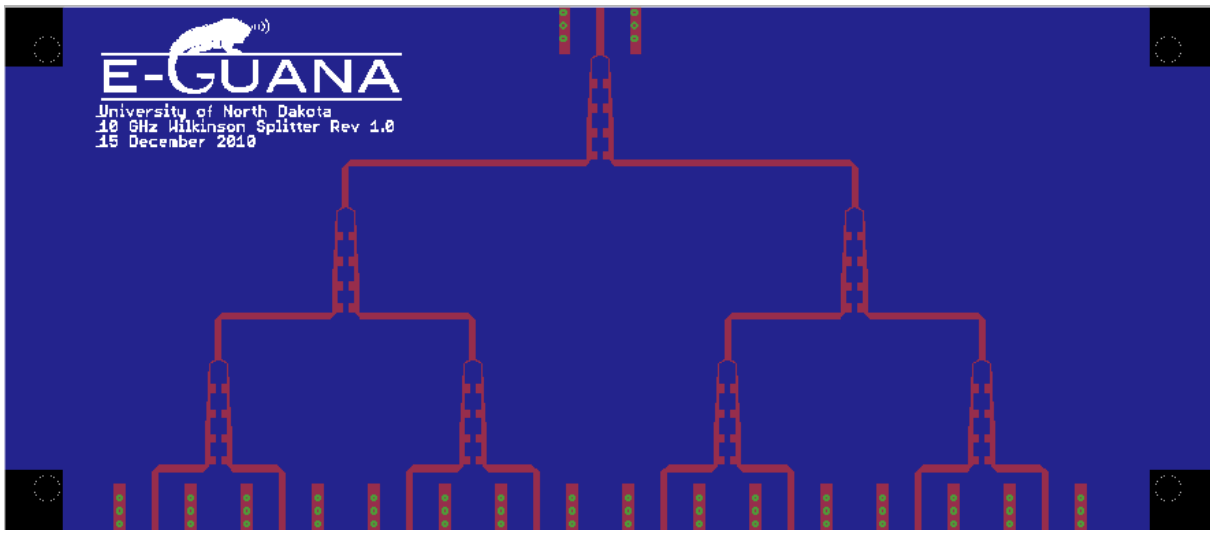

Figure 36: EAGLE Wilkinson Design

EAGLE produces Gerber design files were sent to Advanced Circuits for fabrication [32]. Once the board and components were received, the resistors were placed on the PCB. A board stencil was not purchased to provide guidance when applying the solder so the resistors and solder were placed carefully by hand with the aid of a microscope. Once the resistors were place, the board was put in a controlled oven to solder the resistors into place. After the resistors were set, the SMA connectors were placed by hand taking caution on centering the probe on the microstrip. The final fabricated board can be seen in Figure 37. The output ports are also numbered with the furthest to the left being labeled Output Port 1. This port numbering will be used in Chapter 4 while discussing the results.

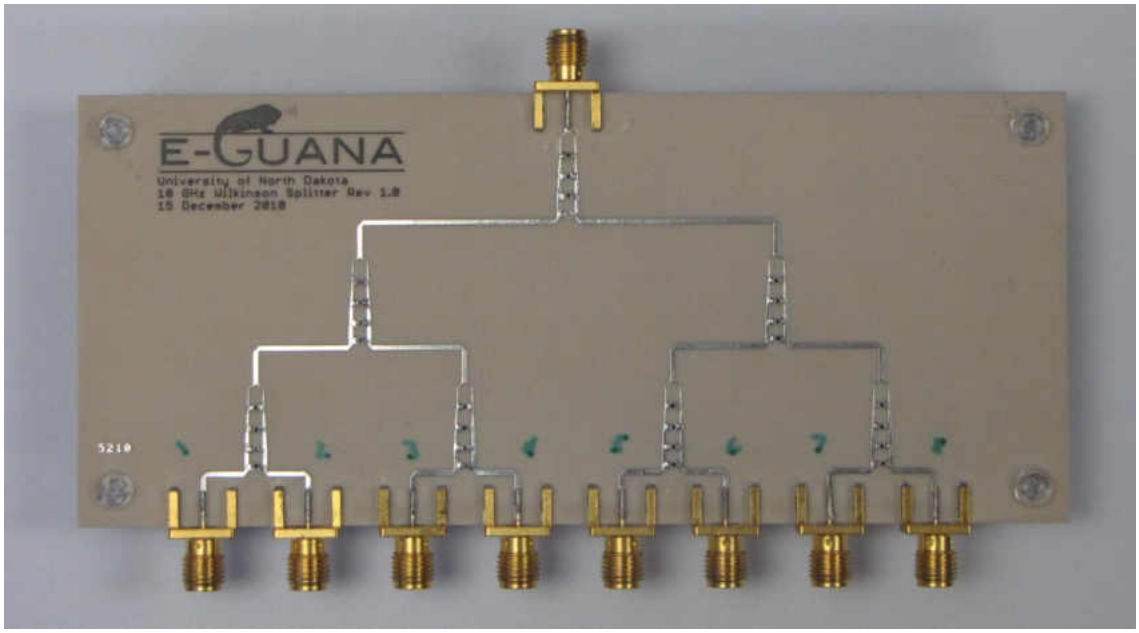

Figure 37: Final Fabricated Wilkinson Power Divider

CHAPTER 4

RESULTS

4.1 Introduction

After the simulation and fabrication of the power divider, the network was tested. The simulation and experimental testing results are compared in this chapter to provide insight into the power divider.

4.2 Measurement Result

The fabricated Wilkinson power divider was tested with Rohde & Schwarz's VZA-40 Vector Network Analyzer (VNA). In order to ensure accurate results, the VNA was calibrated using a Rohde and Schwarz ZV-Z54 Calibration Unit. Figure 38 shows the calibration setup.

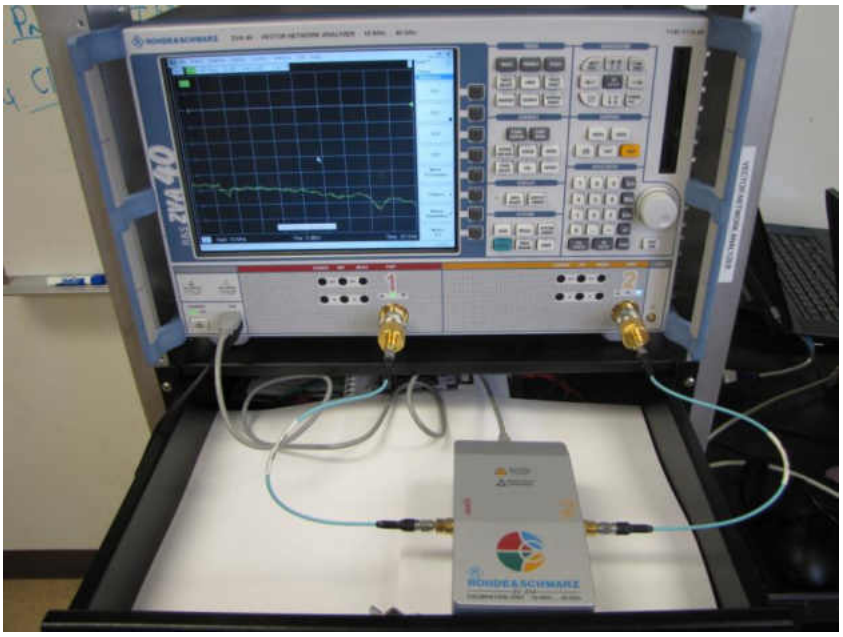

Figure 38: VNA Calibration Setup with ZV-Z54

After the unit was calibrated, using the same connectors and cables, the Wilkinson power divider was attached to the VNA. In order to test for a balanced load across each port, the VNA was set to have a 50Ω termination at the ports and 7 SMA-50Ω terminators were placed at the unmeasured output ports (Figure 39).

Figure 39: SMA-50Ω Terminator

The terminators were alternated to cover all output ports whenever one port was attached to the VNA. The measured reflection coefficient (S11) for each output port was processed using Matlab (Appendix B) and then were plotted. Figure 40 provides the resulting plot.

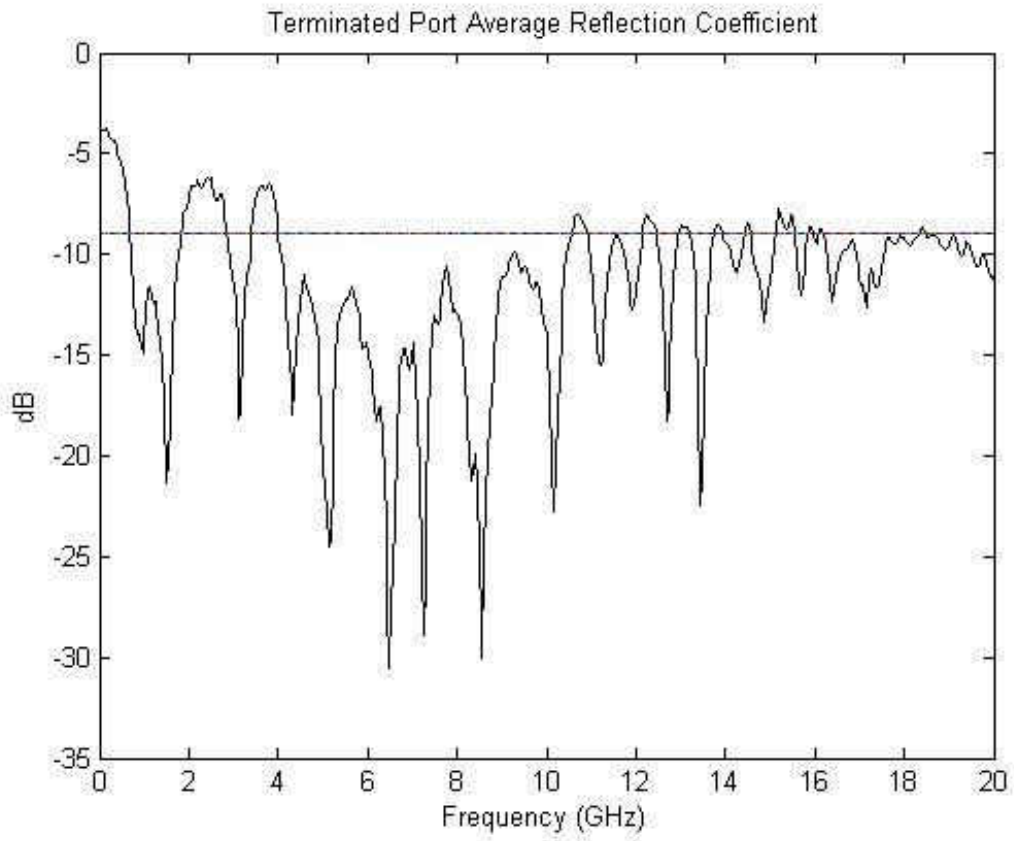

Figure 40: Average Reflection Coefficient of Network

The -9 dB threshold is plotted along with the average reflection coefficient for the network. This provides a visible representation for the operating bandwidth. At high and much low frequency bands the reflection coefficient was less than the threshold. The power divider has a 6.5 GHz bandwidth from 4 GHz to 10.5 GHz. The bandwidth is

not centered at the desired 10 GHz. Figure 41 provides the network's reflection coefficient across the operating bandwidth.

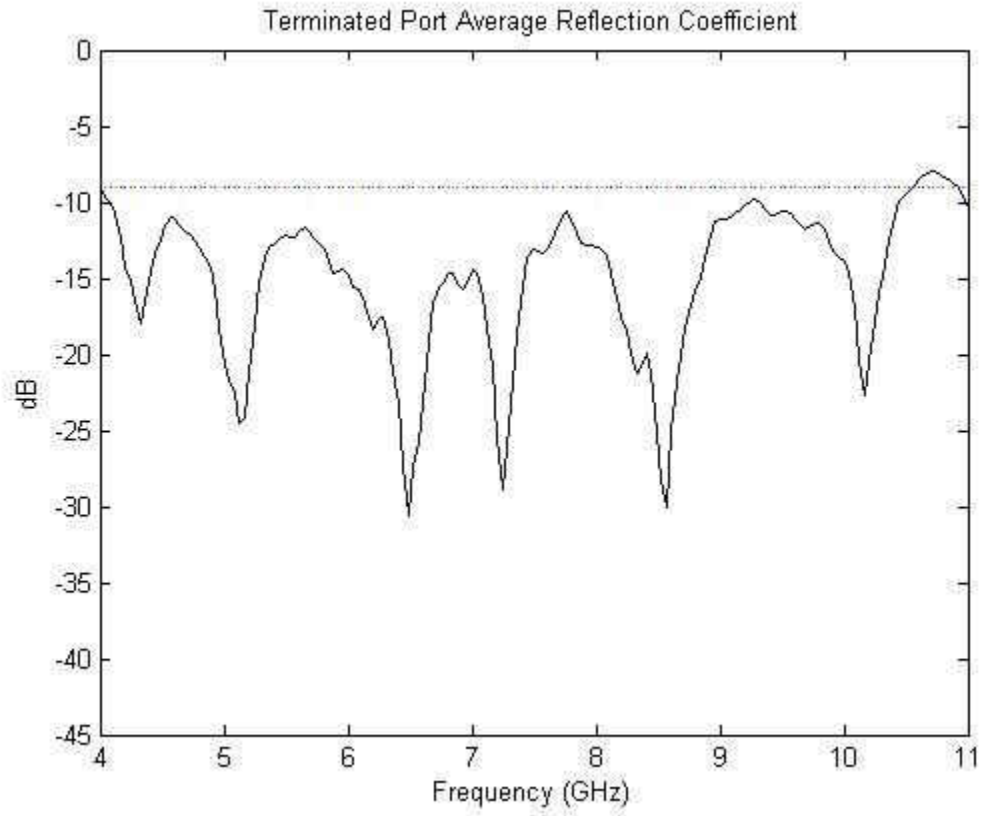

Figure 41: Average Reflection Coefficient Bandwidth (Terminated Ports)

Figure 41 better shows the bandwidth. There are multiple dips in the return loss which is a product of the design of the multistage power divider. For each stage, a dip wf created for a specific frequency. There is a dip of -25 dB reflection coefficient at approximately 10.1 GHz which is offset from the desired 10 GHz. Additionally, while the bandwidth is more than the required 2 GHz, it is not centered at 10 GHz.

The same process was followed to measure the reflection coefficient (S11) while the antennas were attached. A fabricated brace was used to provide stability to the

antennas and to ensure the linearity of the array during testing. It was noticed that occasional interference due to radiation of the antennas cause inaccuracies within the measurements. Figure 42 shows the set-up used for phased antenna array testing. Figure 43 shows the average measurement results from each port.

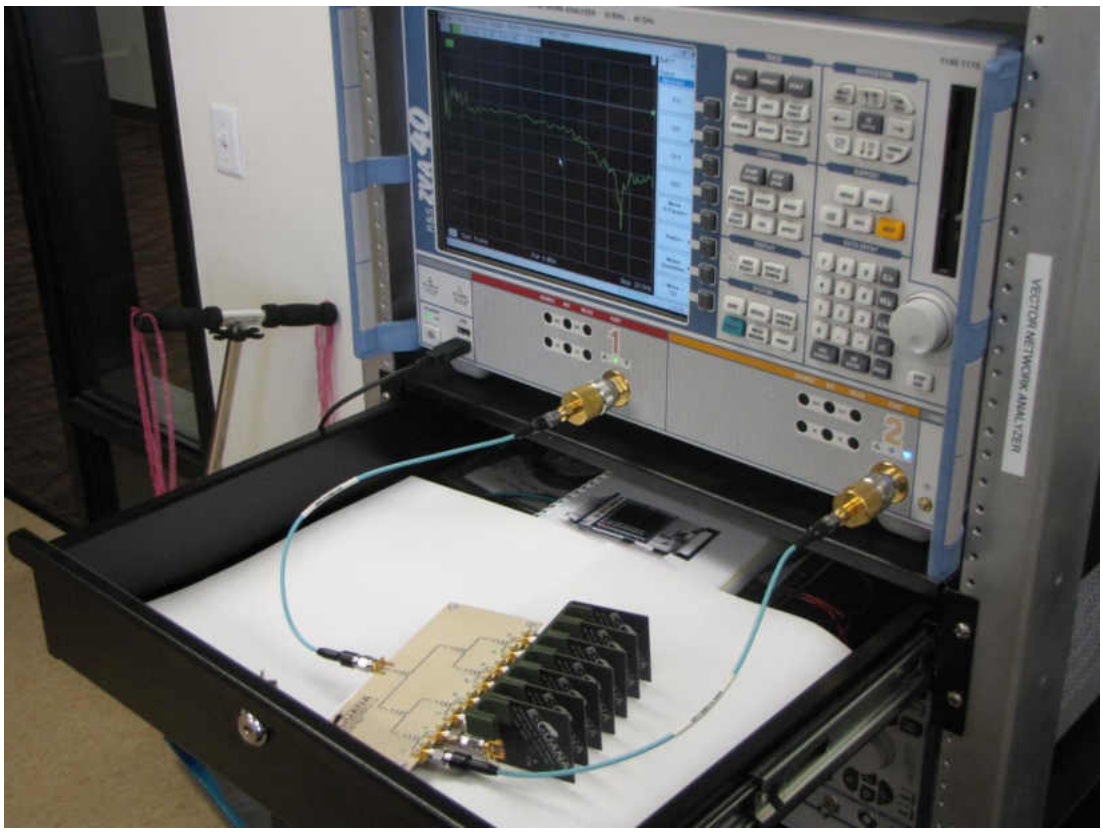

Figure 42: Wilkinson Power Divider with Vivaldi Antenna Test Set-up

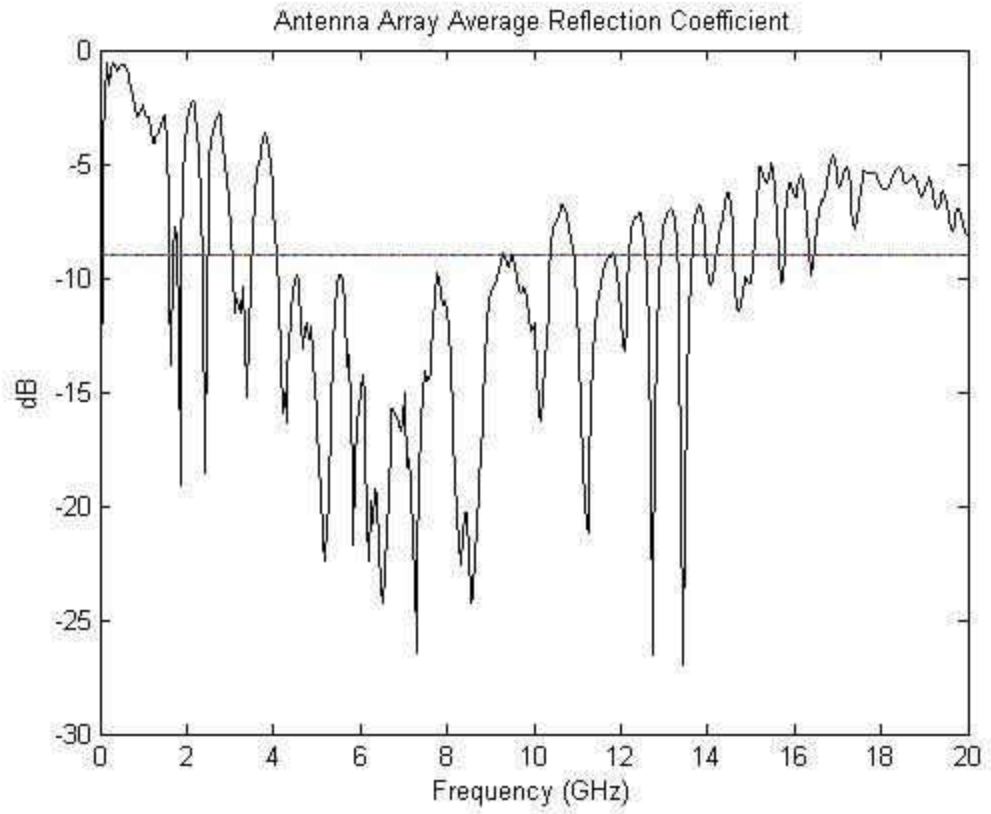

Figure 43: Average Reflection Coefficient for the Combination of Power Divider and Antenna Array

Much like the average reflection coefficient with terminated ports, the operating frequency bandwidth is also 6.5 GHz starting at 4 GHz. Even though the ports are terminated with antennas, their radiation causes more noise to be introduced to the network. A comparison of the terminated and antenna array average reflection coefficient measurements across the 6.5 GHz bandwidth is given in Figure 44.

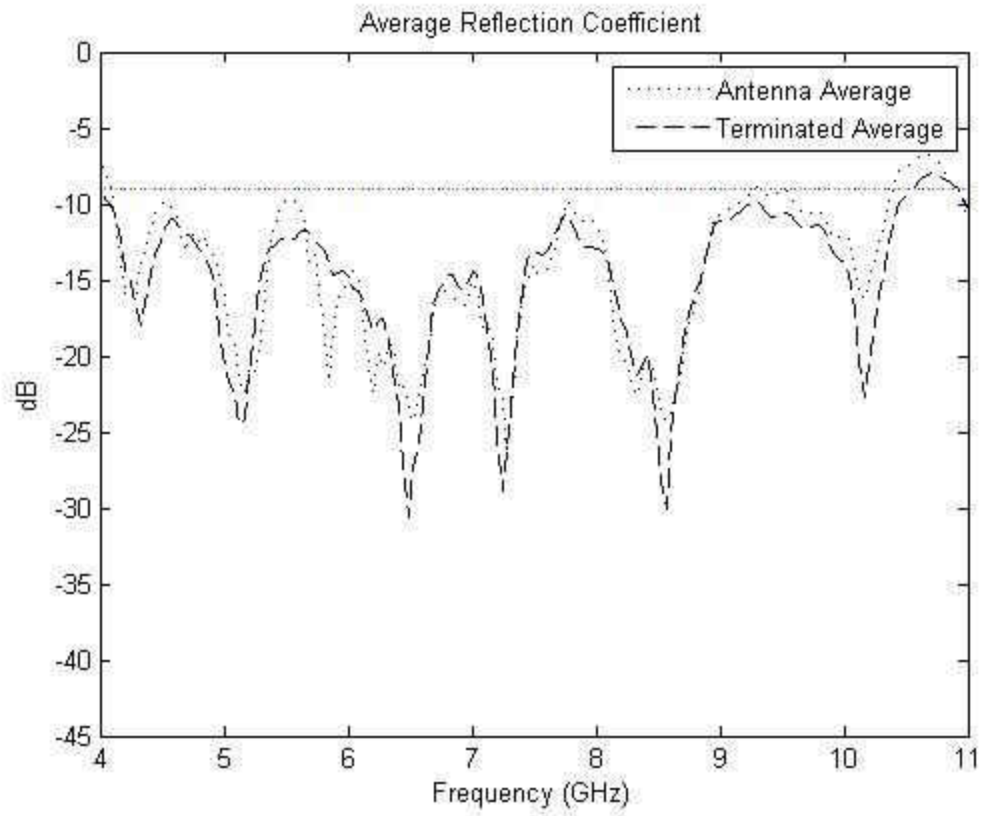

Figure 44: Terminated and Antenna Array Average Return Loss

The noise in the antenna array return loss is noticeable when compared to the terminated ports. The antenna array does not have as severe dips throughout the bandwidth and also comes close to breaking the threshold several times.

During testing, several inaccuracies were observed. During the testing of the antenna array, the cable interfered with the radiation of several antennas in the array which affected the return loss during the measurement. There are also inaccuracies created by the bend in the cables connecting the network to the VNA. Care was taken in keeping the same position but the slightest alteration in the cable's bend could affect up to -3dB change across the measurements. A torque wrench was used to apply an equal

torque of 8 in/lb to each port but it was noticed that the antenna SMA connectors often came loose. Additionally, each SMA connector on the network was placed individually by hand. Slight inaccuracies could occur based off the differences between each probe placement.

4.3 Port Isolation

The isolation between ports is measured using the VNA. The desired measurement for port isolation is any value lower than -25 dB. Figure 45 depicts the isolation between Output Port 1 and all other ports over the 6.5 GHz operating bandwidth of the network. The isolation for all the Output Ports are provided in Appendix A.

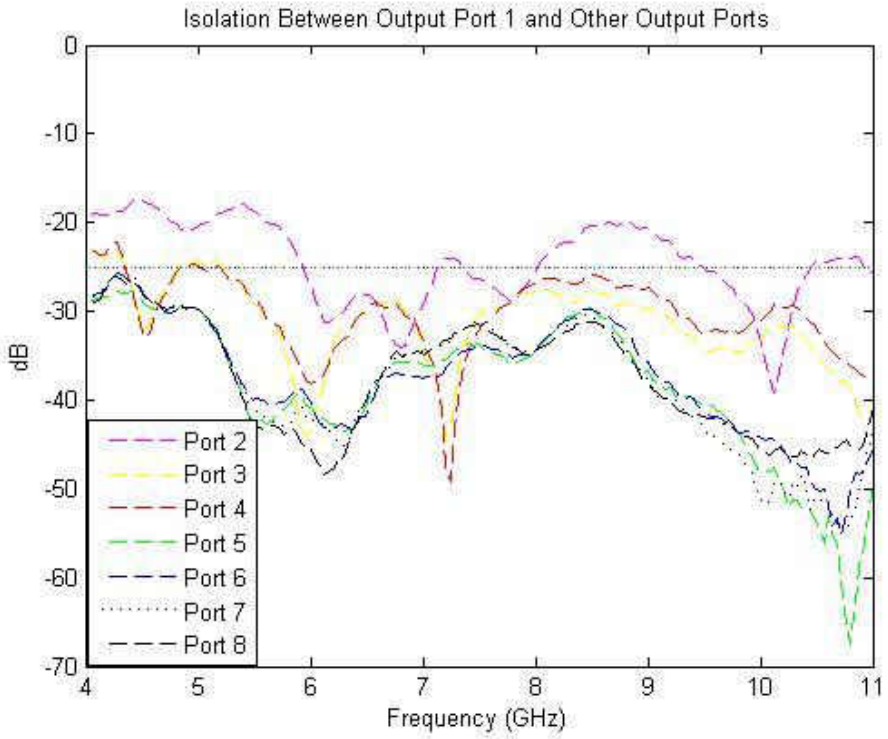

Figure 45: Output Port 1 Isolation Open Port

Figure 45 displays that most of the output ports are well underneath the required -25 dB threshold. Output Port 2 which is located closest to Output Port 1 is often breaking the desired threshold. A better way to explain why the isolation between these two ports is not meeting the required value over the bandwidth is to trace the path from Output Port 1 to Output Port 2. There is only a single power division with four isolator resistors. The other output ports have multiple divisions and resistors to provide better isolation. Note that at 4 GHz, Output Port 3 and 4 are above the desired measurement. These two ports are the next closest ports to Output Port 1 and will act this way because of the design of the power divider.

A potential inaccuracy in the isolation could be the human error when soldering the resistors to the network. Care was taken in soldering but due to the resistor's size, they could be slightly off their pad. Also, when acquiring the resistors, the theoretical resistance value could not be met with the standard resistors on the market so the next highest standard resistor was used. Plots for other ports can be found in Appendix A.

4.4 Phase and Power Error

The VNA produces a signal that is sent through the network. The initial signal is then compared to the received signal (the one that went through the network). The data was processed using Matlab and plotted to find the average phase error for each output port across the power divider's operating bandwidth. Data was acquired through the same method for testing the reflection coefficient. The phase for matched

terminated port, antenna terminated port, and open circuit port were then graphed. Figure 46 shows the matched terminated phase across all eight ports.

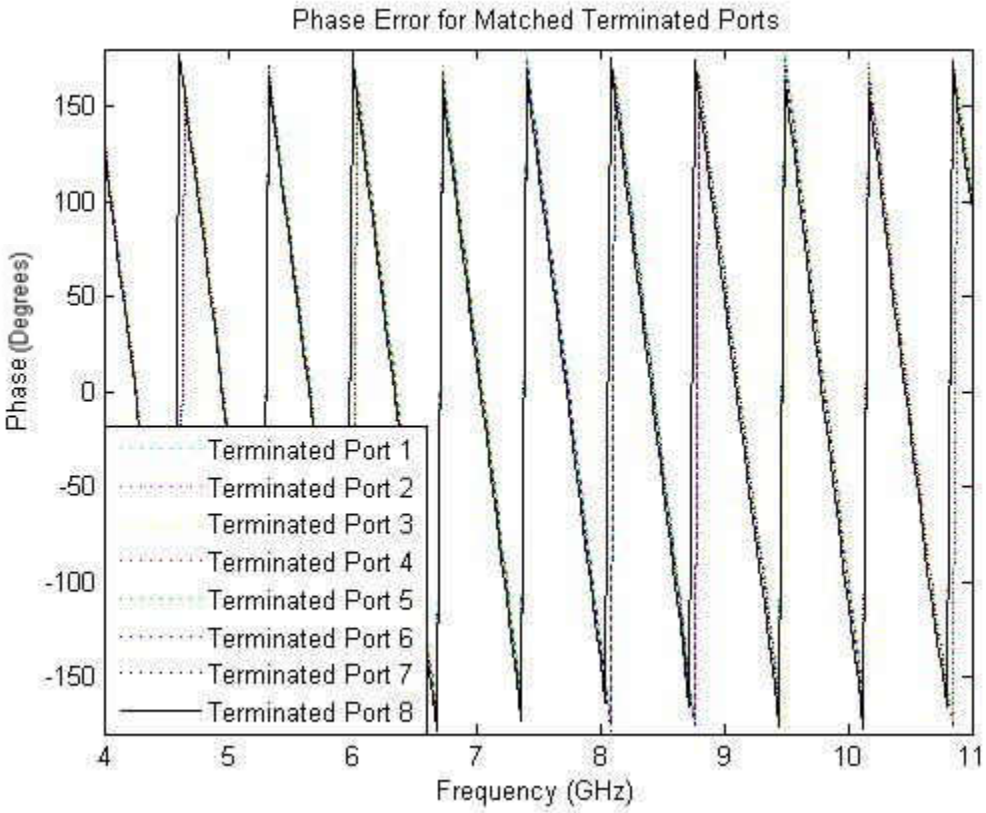

Figure 46: Phase Across Matched Terminated Output Ports

Looking at the graph of each output port's phase does not provide enough information on the differences between the phases. The phase measurement of the antenna array and open circuit ports look similar to Figure 46. As mentioned, there are differences between the output port signals. In order to better analyze the difference in phase at the output ports, the error for Output Port 3 and Output Port 8 were plotted for visual effect with a 2 GHz bandwidth (Figure 47).

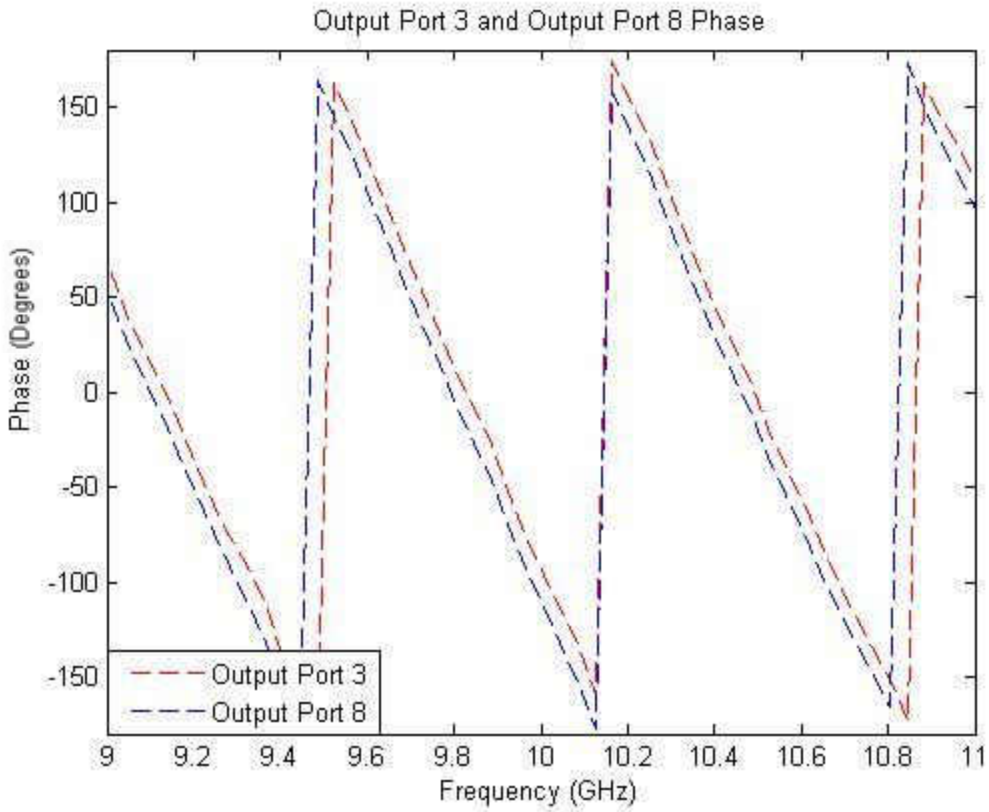

Figure 47: Port 3 and 8 Phase with Matched Terminator

It is apparent that these two ports have a phase difference. This difference shows the phase difference between the two ports. Because the system was designed to keep provide each output signal in the same phase, this difference is the phase error. The error was calculated in Matlab with the phase shift angles values plotted (Figure 48). This plot proves that the absolute value of error increases with frequency. Also the occurance of this error is more at a higher frequency band. Note that the phase error is minimal across 4 GHz to 12 GHz with a single outlying spike.

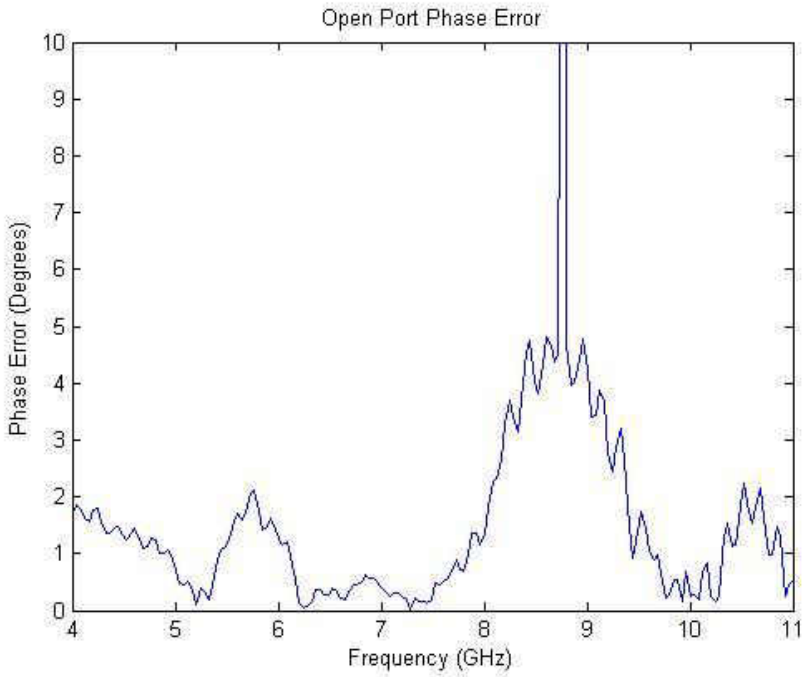

Figure 48: Open Port Phase Error Between Output Port 3 and Output Port 8

The phase error at 10 GHz is 0.4˚ with a single outlier in phase error at 8.8 GHz. This large error would provide massive error within the entire system if it was to operate at 8.8 GHz. The phase differences between port 1 and all other outputs are calculated then the mean is found to provide a single port average. The majority of the error happens at frequencies higher than 12 GHz which is out of the design frequency band. Figure 49 provides the phase error for Output Port 1 across the 6.5 GHz operating bandwidth of the power divider.

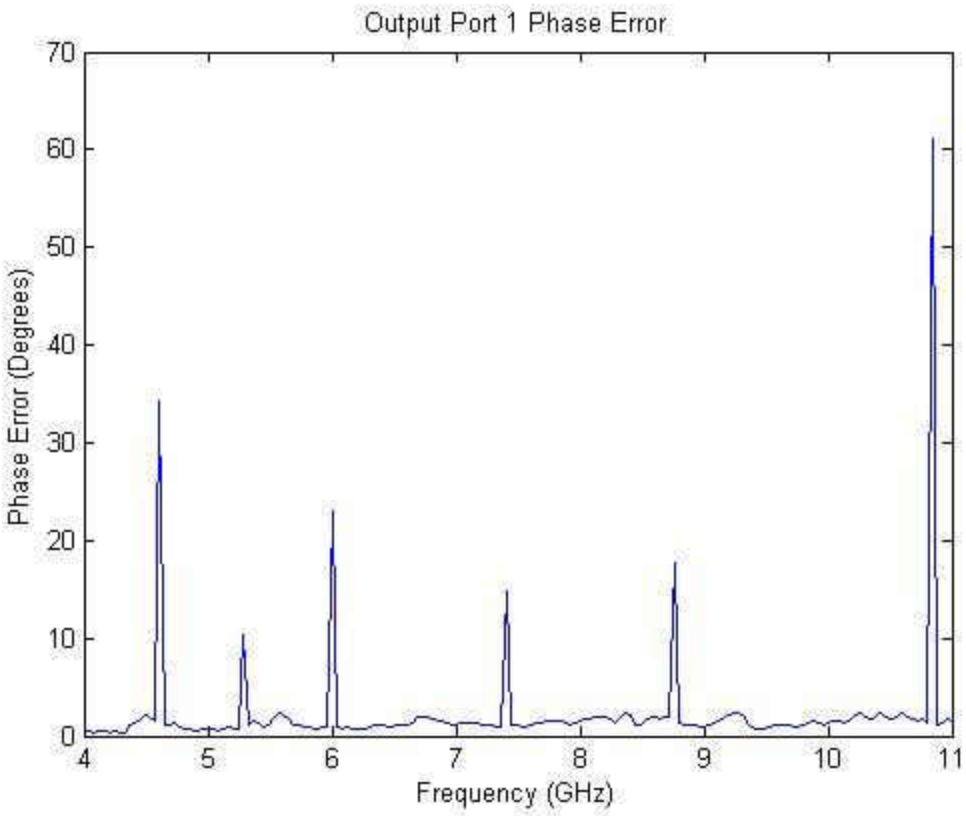

Figure 49: Output Port 1 Average Phase Error

The phase error is below the required phase error across most of the 6.5 GHz operating bandwidth but there are multiple outliers that would render the network nonfunctional. The large phase errors would not provide the necessary accuracy in the antenna array broadside radiation.

Taking the phase error for each port and applying the error into a Matlab program that calculates the array factor for the antenna array, Figure 50 was created to show the ideal array factor and the anticipated array factor including the phase error.

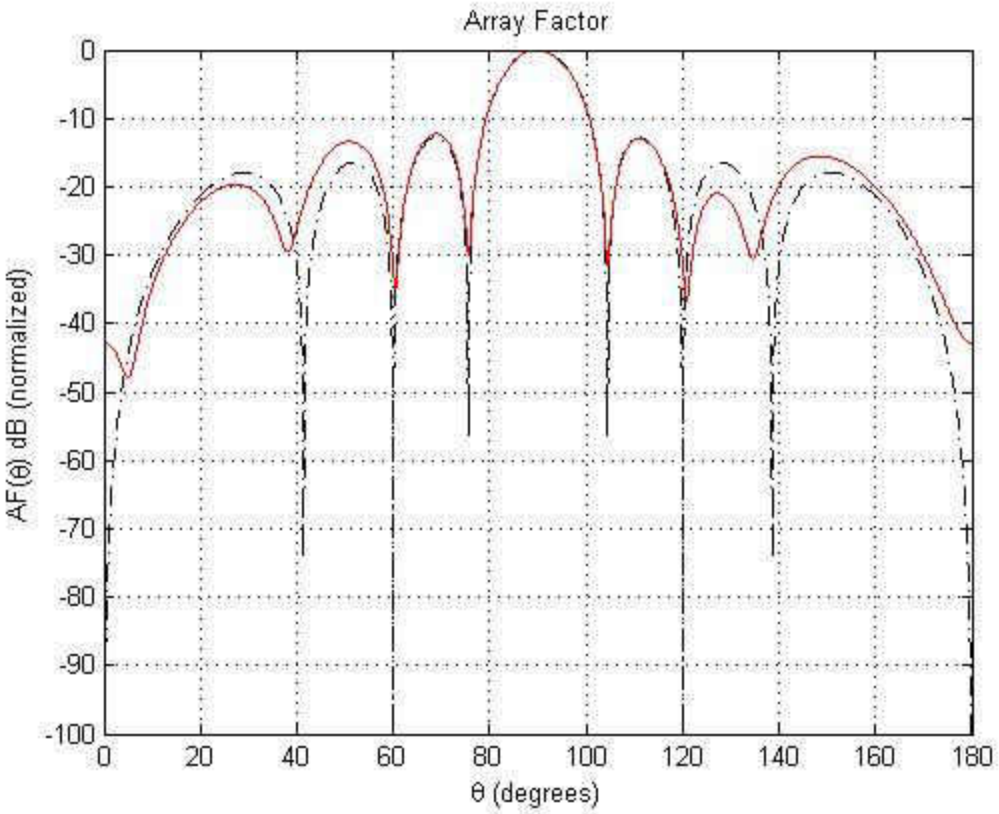

Figure 50: 90 Degree Radiation Array Factor

The figure shows the array factor for a 90˚ radiation array. The solid red line shows the array factor with the phase error included while the dashed line provides the ideal array factor without any error. The two are closely aligned but the side lobes do start to diverge. The array factor divergence is prominent at the side lobes because of the phase error of each element affecting the radiation.

To measure the power loss of the network, the VNA provides the S21 scattering parameter which measures the loss between the VNA Port 1 and the VNA Port 2.Port 1 of the VNA is attached to the input of the network while port 2 is attached to the desired network output for measurement. The S21 is measured with three different

types of port terminations: matched terminator, antenna array, and open circuit. The S21 provides the occurred losses across the board. The power loss for each power division is -3 dB and with three sections for each port a total power loss will be 9dB in an ideal condition. The difference between the measured power loss and the actual network power loss is the measured value subtracted by the anticipated power loss from the power divider. Figures 50-52 provide the S21 for each termination and Figure 53 compares the three terminations for Output Port 1.

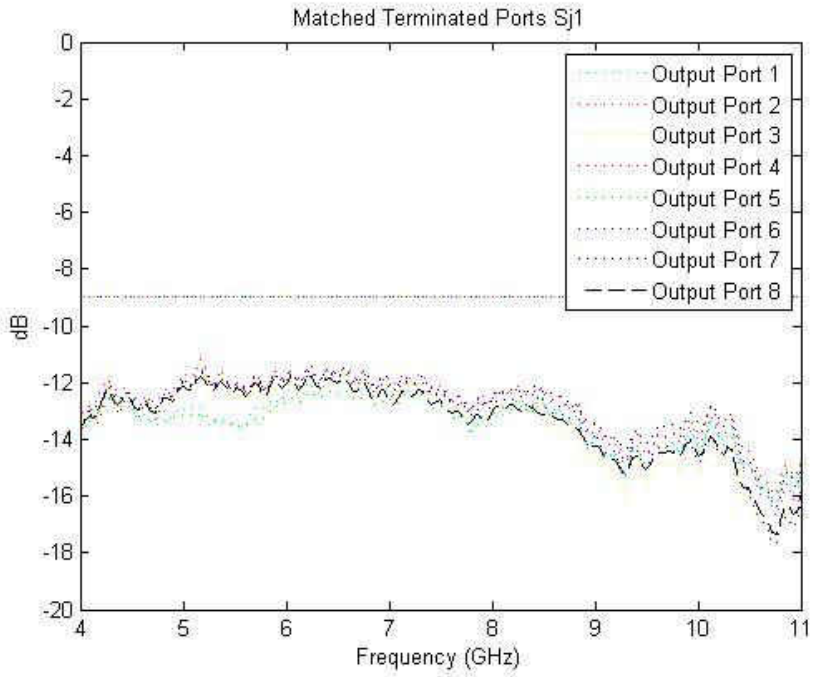

Figure 51: Measured S21 Between Input and Balanced Output Ports

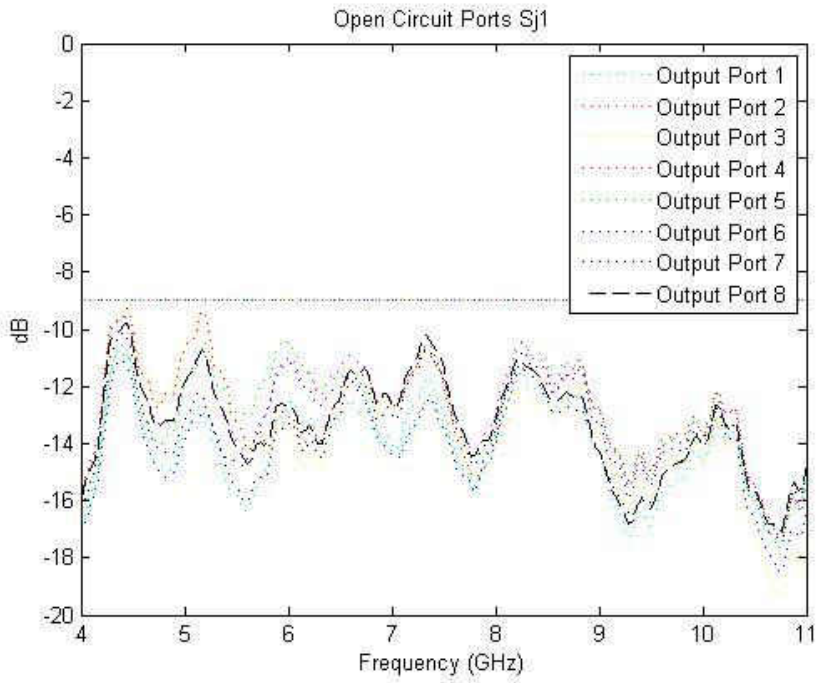

Figure 52: Measured S21 Between Input and Unbalanced Open Output Ports

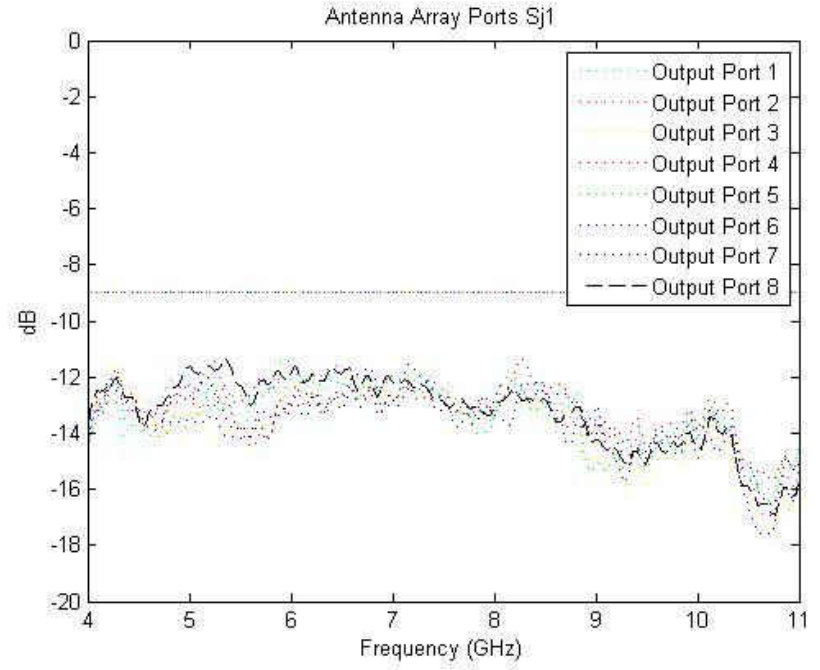

Figure 53: Meaured S21 Between Input and Unbalanced Antenna Output Ports

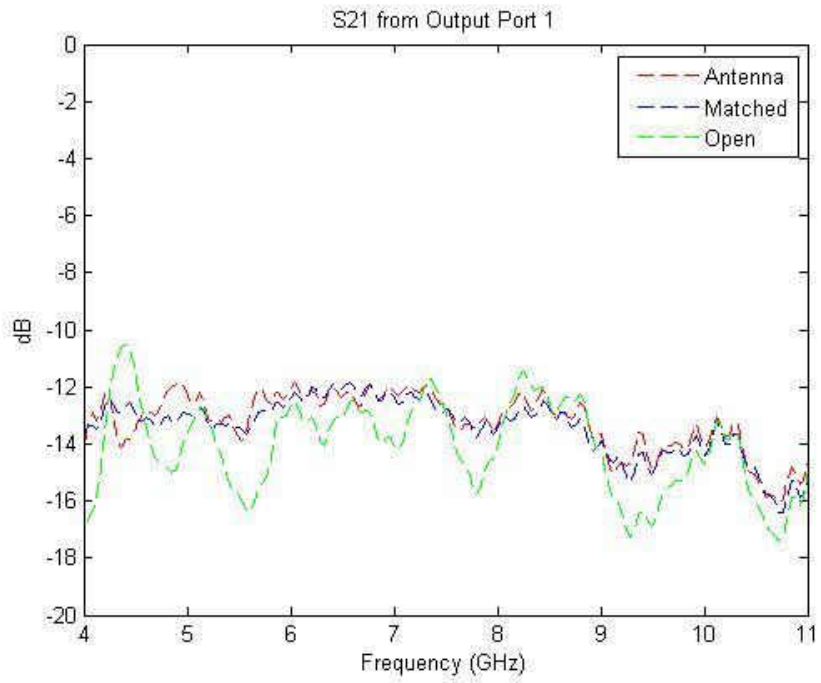

Figure 54: Measured S21 at Output Port 1

The power loss when each output port except the measured one is attached to a 50Ω terminator provides the best and less noisy results. The 50Ω antenna elements also provide similar results but are slightly more noisy. The open circuit is the noisiest of all three with a loss of up to 9 dB. Figure 53 compares the three terminations. The average power loss for the open circuit is 5.4 dB, matched termination is 4.2, and the antenna array is 4.3. Commercial products typically have losses of approximately 2 dB which is the threshold for power loss. The matched termination is the closest to this desired loss.

Multiple factors could have affected the losses across the board. The change in the angle of cable bend affects the results slightly. Additionally, the design of the network has the tapered quarterwave transformers to provide smoother transition between stages which could have added the losses. The biggest contribution to the loss

though is from the transmission line. Coupling also affects the power loss. A more unique design that negates the coupling can provide better results. While the results are not equal or better than the desired power loss, 4.3 dB loss is an acceptable power loss with the feed network when integrated with the entire system.

4.5 Board Integration With The System

The Wilkinson power divider was integrated into the 10 GHz phased array system. The output ports' distance matched precisely with the phase shifter module's inputs and they were connected smoothly with the Male-Male SMA connectors. Figure 54 shows the entire integrated system without the control module and Figure 55 displays the entire system with the control board.

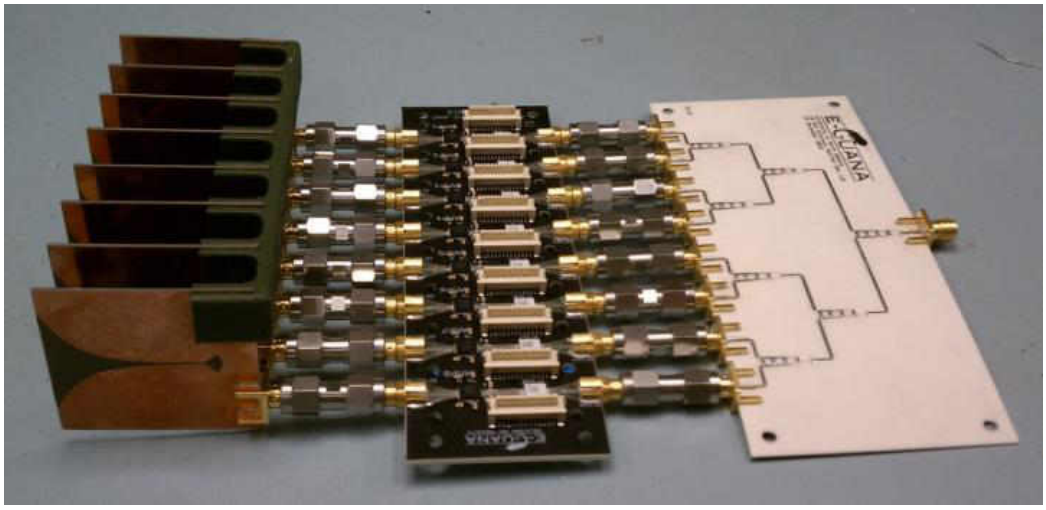

Figure 55: 10 GHz Phased Array System Without Control Board

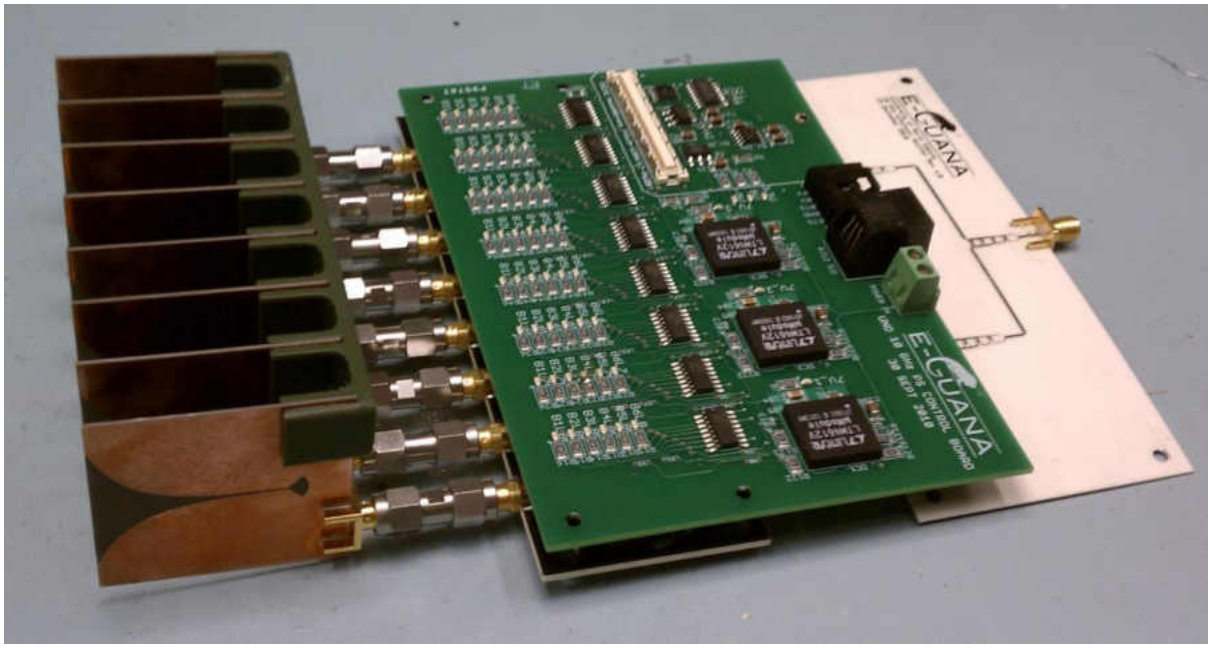

Figure 56: 10 GHz Phased Array System With Control Board

The Wilkinson power divider, while not ideal, operated properly within the system but the full system itself is unable to operate due to the power amplifier issues on the phase shifter board. Due to the amplifier's failure, only a small amount of RF energy is transmitted which renders steering impossible.

4.6 Comparison of Measured and Simulated Results

There are obvious differences in the measurements from the simulated power divider and the fabricated network. Table 8 provides a comparison between the two.

Table 8: Comparison of Measured and Simulated Results

	Simulation	Experiment
Closest Reflection Coefficient Dip	9.9 GHz	10.1 GHz
Bandwidth	1.5 GHz	6.5 GHz
Power Loss	2 dB – 3dB	2.8 – 8.8 dB
Port Isolation	-17dB – -37 dB	-18 – -68 dB

The closest dip in the reflection coefficient, thus better functionality for the network, are both not at 10 GHz. Even though both operate at this frequency based on the reflection coefficient threshold of the network, 10 GHz is not the center frequency nor an optimal operating frequency. The fabricated power divider shows a much wider operating bandwidth than the simulation. Both results were not centered at 10 GHz with this frequency being located towards the upper frequency in the bandwidth. The power loss and port isolation were measured across the operating bandwidth of 6.5 GHz. The measured results from the power divider has more power loss than the simulated results as it was is expected with the increase in bandwidth. Power is sacrificed in order to achieve a larger bandwidth. Lastly, the port isolation is much better with the fabricated Wilkinson. This could come from the higher impedance isolation resistors used on the fabricated PCB.

CHAPTER 5

CONCLUSION

5.1 Final Assessment

At the beginning of this research, a wideband power divider was to be designed and fabricated to function within the developing phased array radar system for UAV non-cooperative sense and avoid application. The Wilkinson power divider was designed to meet certain requirements with space, operating frequency, and phase error. Table 9 lists the requirements obtained values for the fabricated system.

Table 9: Design Requirements

	Required	Fabricated
Size	6”x 3” x 2” with output ports spaced 590 mils	5.6” x 2.43” x 0.314” with output ports 590 mil apart
Closest Reflection Coefficient Dip	10 GHz	10.1 GHz
Operating Bandwidth	2 GHz with 10 GHz at the center	6.5 GHz with 7.25 GHz at the center
Phase Error	3.5˚	0.1˚ – 61˚ with 0.4˚ phase error at 10 GHz
Power Loss	2 dB	2.8 – 8.8 dB
Port Isolation	-25 dB	-18 – -68 dB

The fabricated system did not meet all the requirements in Table 9 but did perform better than requirements in terms of bandwidth and phase error. The two requirements that were not met are the bandwidth is not centered at 10 GHz and the power loss. Also, the network works within the phased array antenna system.

The power loss and center frequency can be improved to provide the system a better power divider. If the bandwidth of the network is decreased, the power loss can be minimized. With a smaller bandwidth, there would be less necessary stages which would also allow for the operating frequency to be center in the reflection coefficient.

Another consideration for the power divider is the design of multistage Wilkinson. The proposed design for a multistage circular Wilkinson power divider is given in Figure 57.

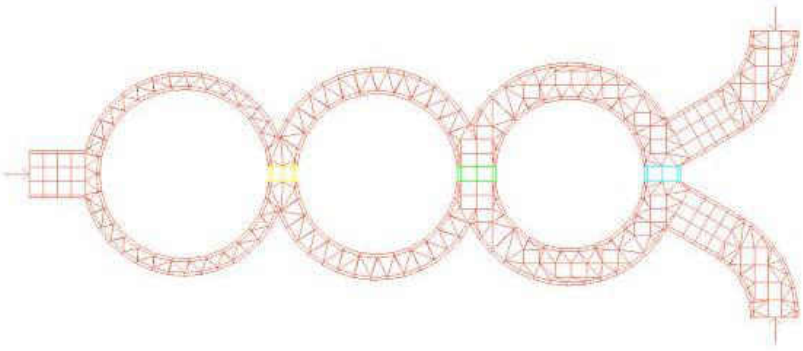

Figure 57: Proposed Multistage Circular Wilkinson Power Divider [34]

In this design, the coupling that happens between the parallel lines in this model would be reduced which would increase performance. The biggest concern though was the output distance which would also have to be considered during this design and is the reason that the circular power divider was not used.

5.2 Future Considerations

Field testing of the system will be the next step within the phased array system design. Unfortunately, the phase shifter board is not working and needs to be redesigned and fabricated to fix the 10 W amplifiers. Also, the Wilkinson power divider can be further optimized to provide better transmission. Finally, a reception module should be designed to receive a signal and turn the current transmission system into a fully operational phased radar system.

APPENDICES

APPENDIX A

WILKINSON SPLIT VNA RESULTS

The Wilkinson splitter was tested using Rhode and Schwatz Vector Network Anaylzer and the data was interpreted through Matlab software. Three different loads were tested on the divider. The 10 GHz Vivaldi antenna array was attached to the unused output ports with the VNA port 2 being attached to the desired network output port for measurement. The 50Ω port terminators were attached during the testing for matched output ports. Another round tested all the ports open circuit except for the output port that is being measured. These measurements were discussed in Chapter 4. The following graphs show the difference in measurement for each port based on the type of port termination.

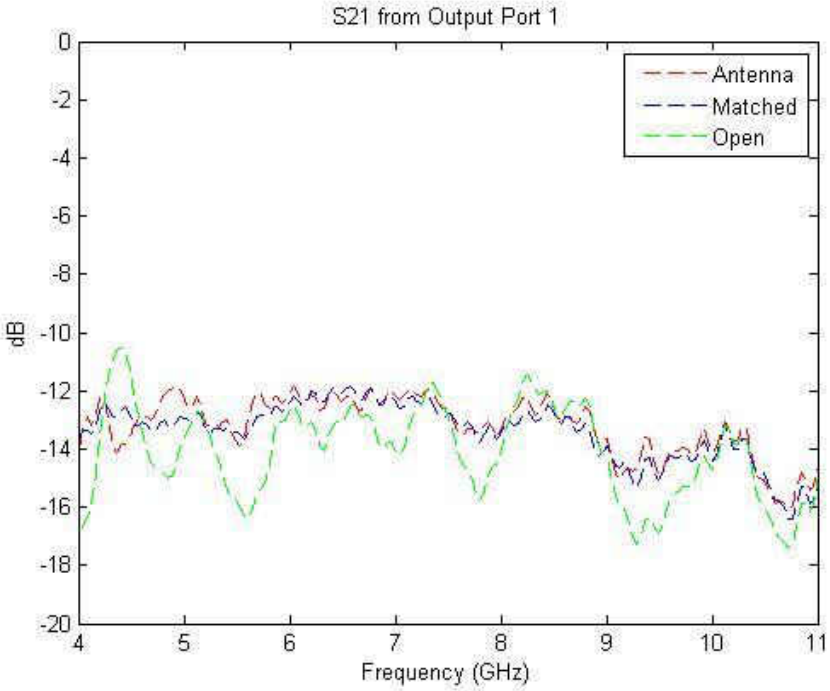

Figure 58: S21 Output Port 1

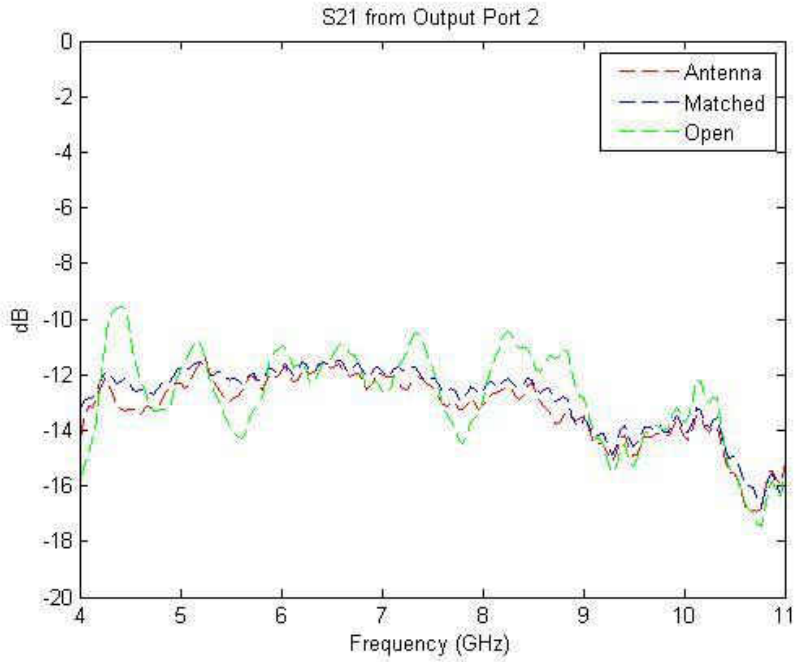

Figure 59: S21 from Output Port 2

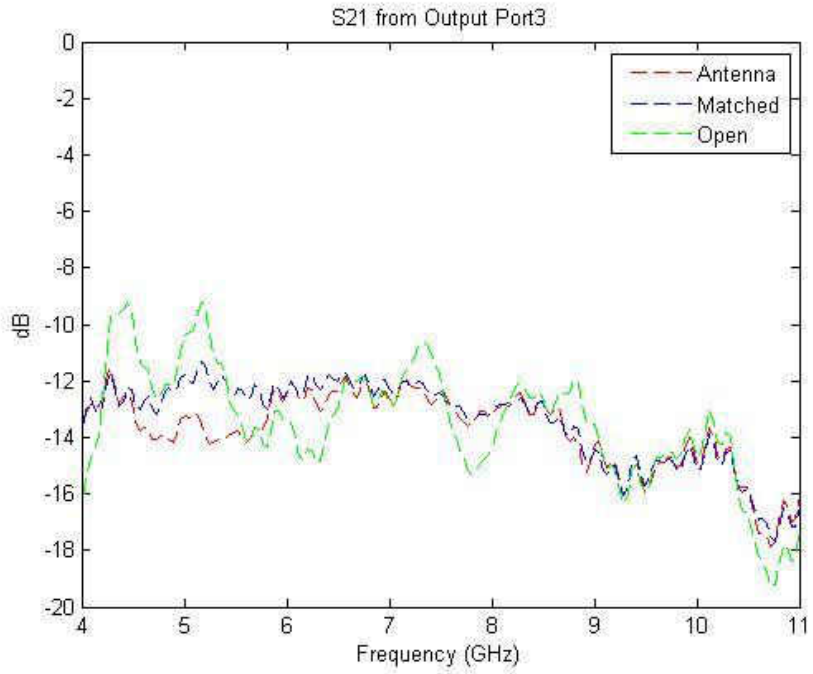

Figure 60: S21 from Output Port 3

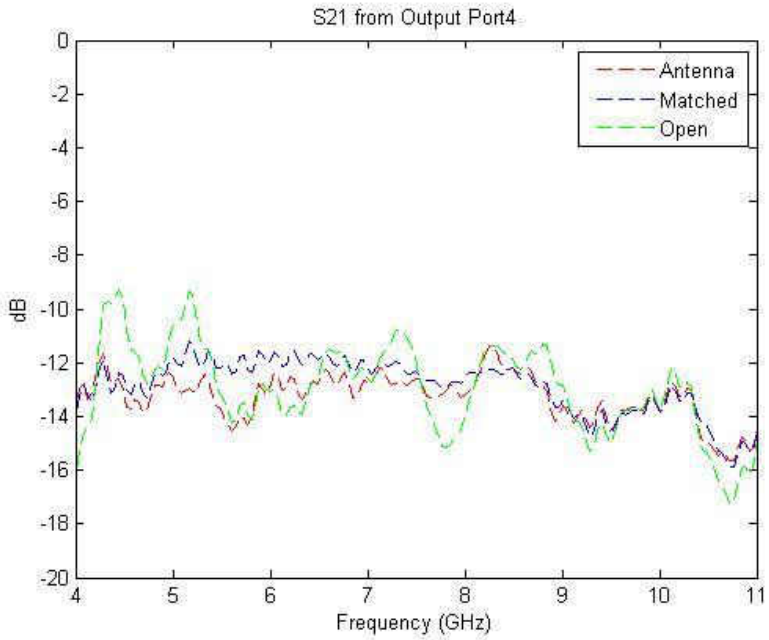

Figure 61: S21 from Output Port 4

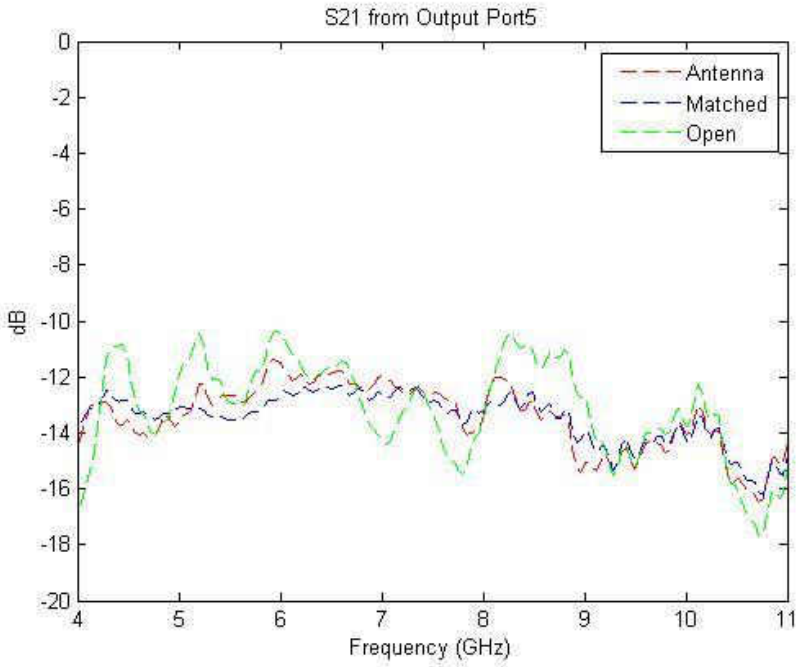

Figure 62: S21 from Output Port 5

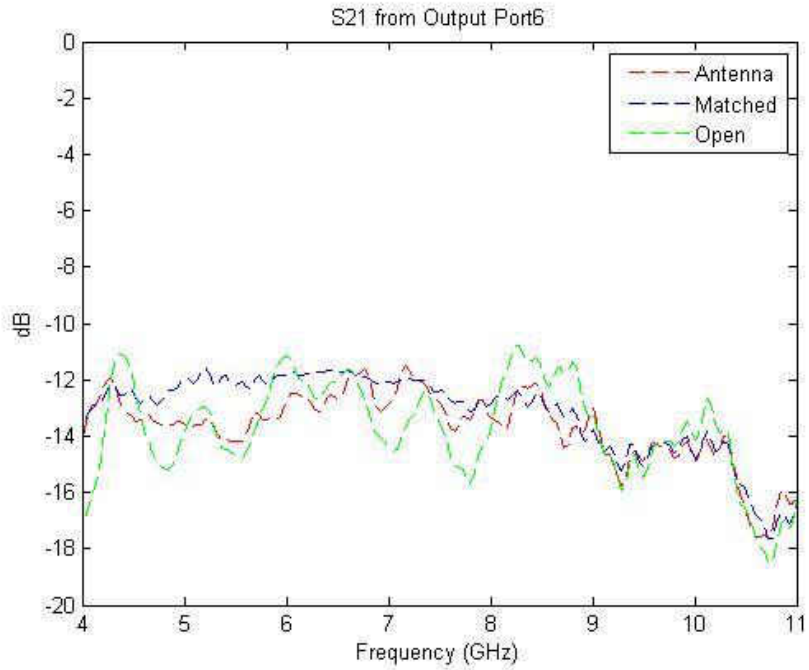

Figure 63: S21 from Output Port 6

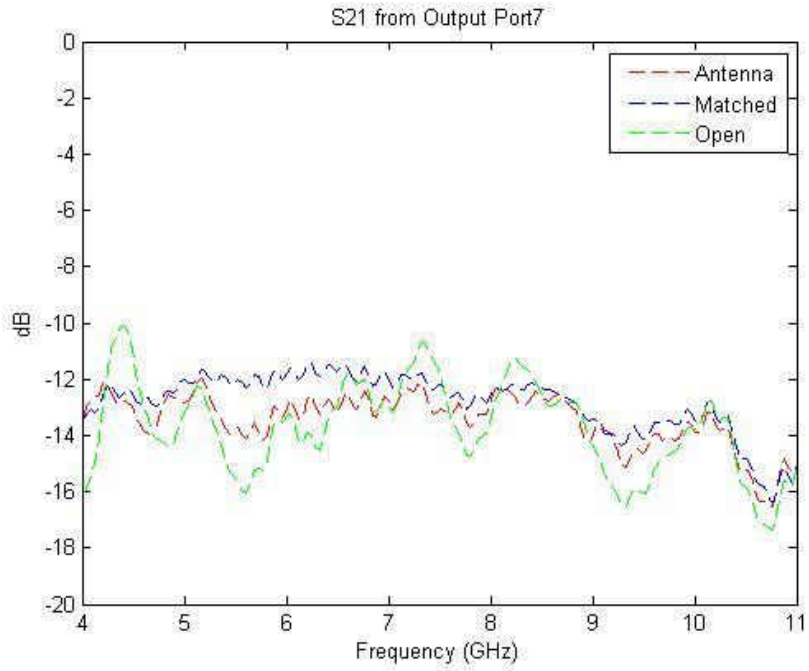

Figure 64: S21 from Output Port 7

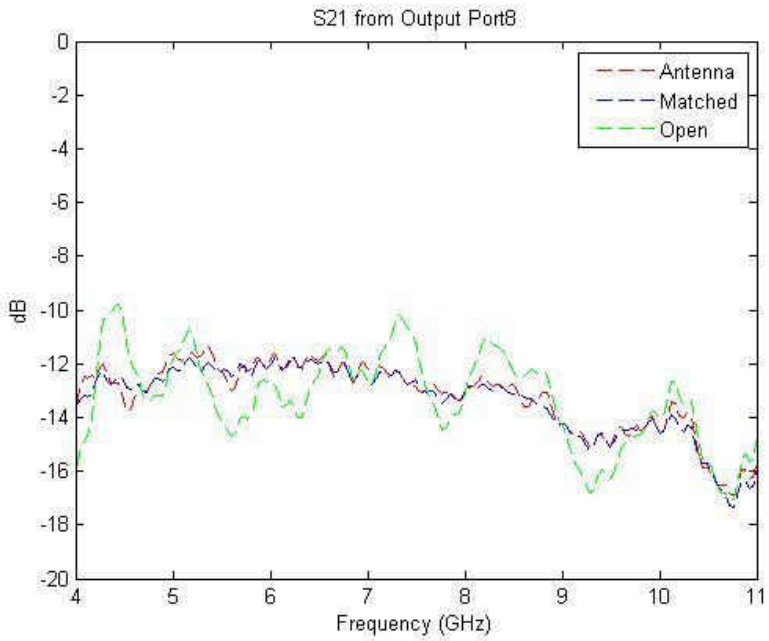

Figure 65: S21 from Output Port 8

The measured isolation at each port is given in Figures 64-71. Note that the partnered ports (Port 1 and 2, 3 and 4, etc.) have the lowest loss which signifies that those ports are not as isolated as the other output ports. While -20dB is not meeting the desired result, most of the other ports are averaging -37 dB isolation which shows that they are well isolated from each other.

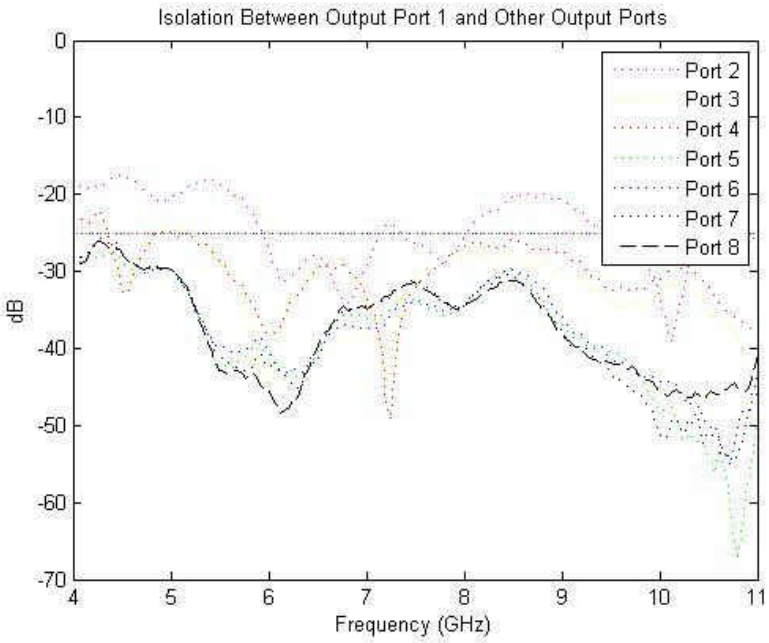

Figure 66: Isolation Between Port 1 and Output Ports

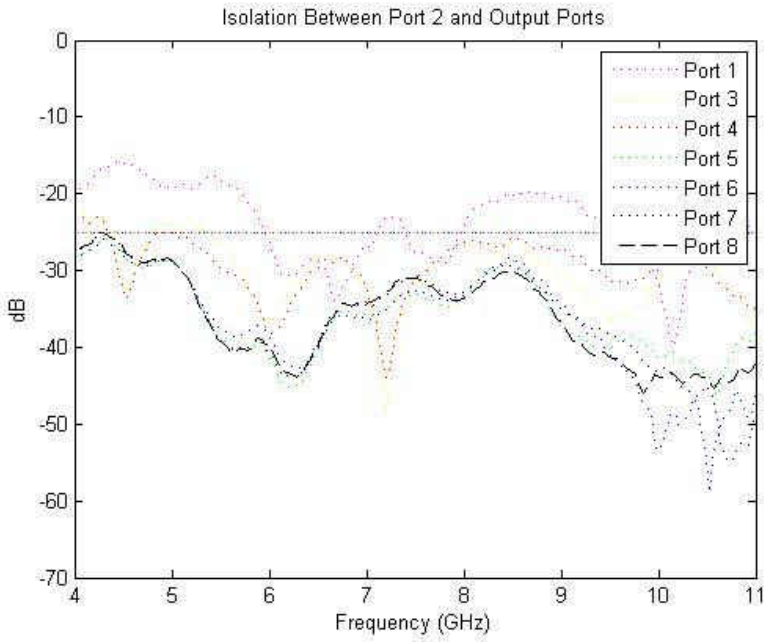

Figure 67: Isolation Between Port 2 and Output Ports

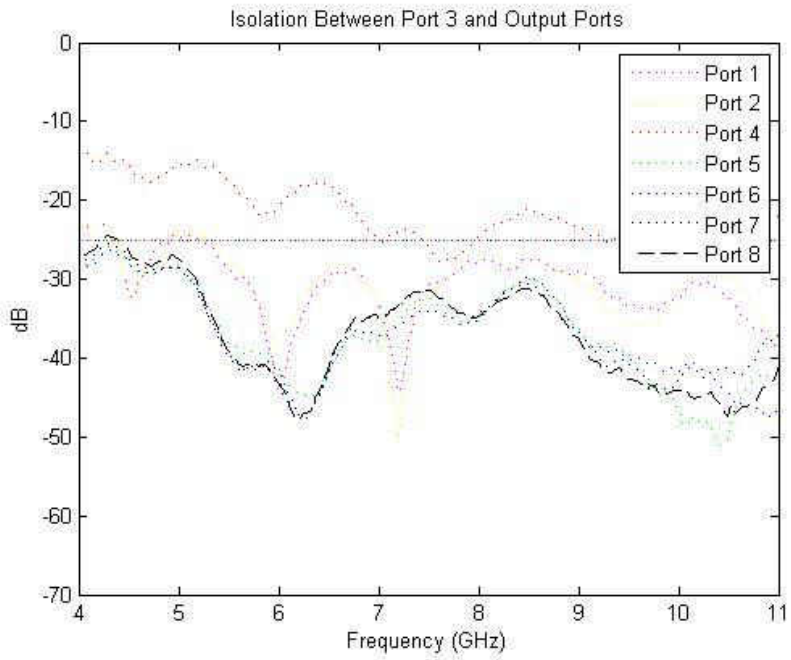

Figure 68: Isolation Between Port 3 and Output Ports

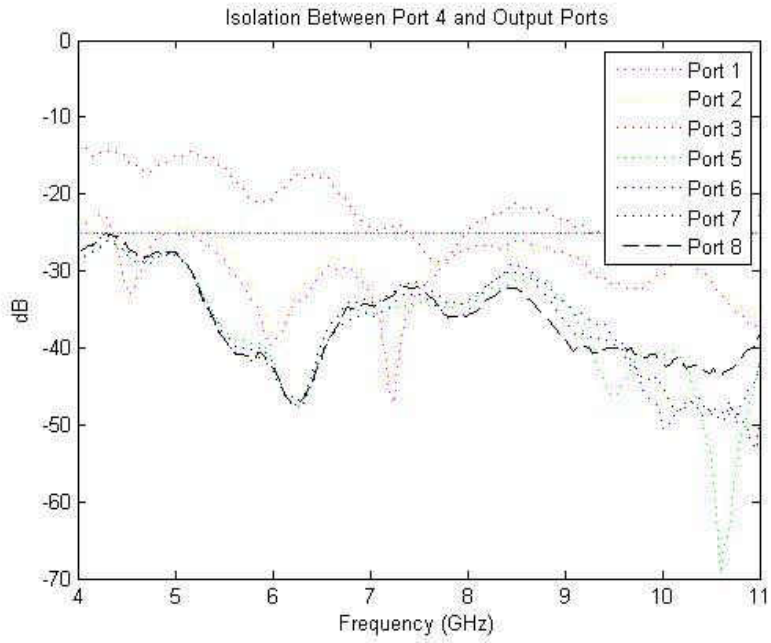

Figure 69: Isolation Between Port 4 and Output Ports

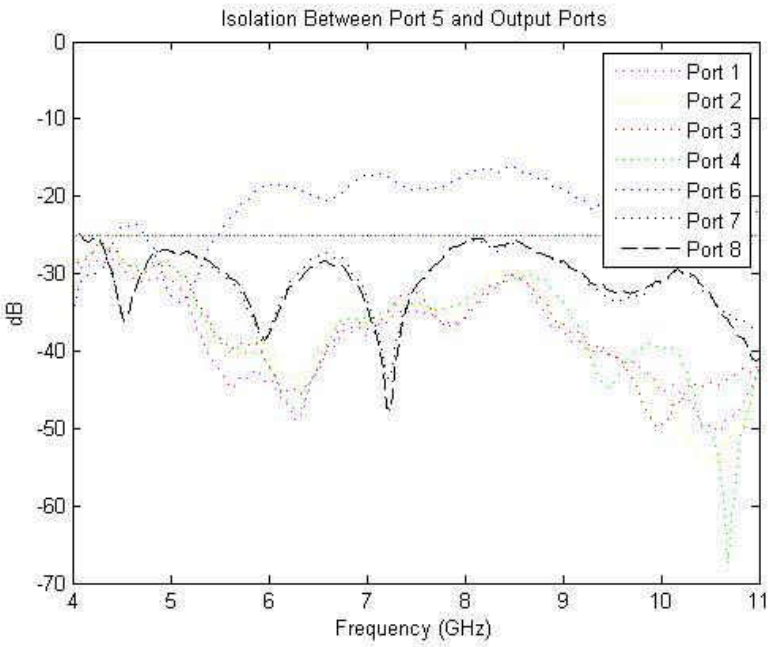

Figure 70: Isolation Between Port 5 and Output Ports

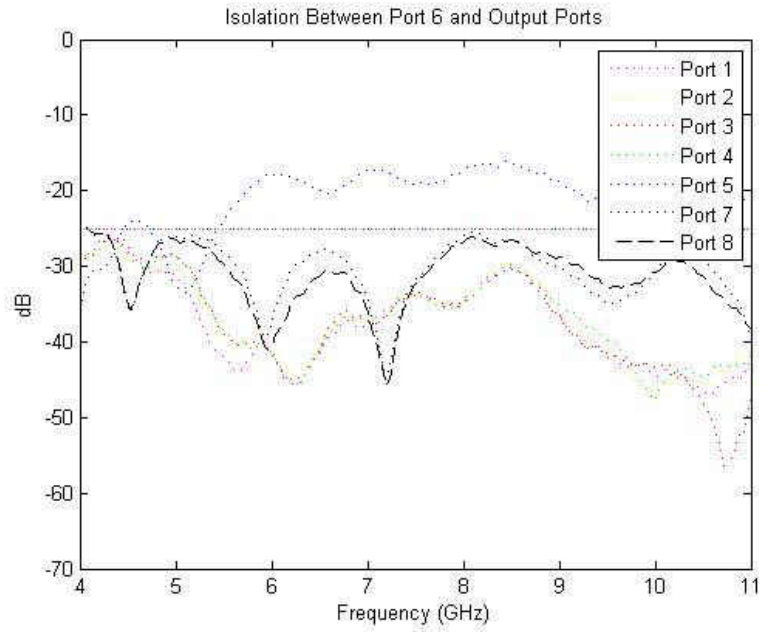

Figure 71: Isolation Between Port 6 and Output Ports

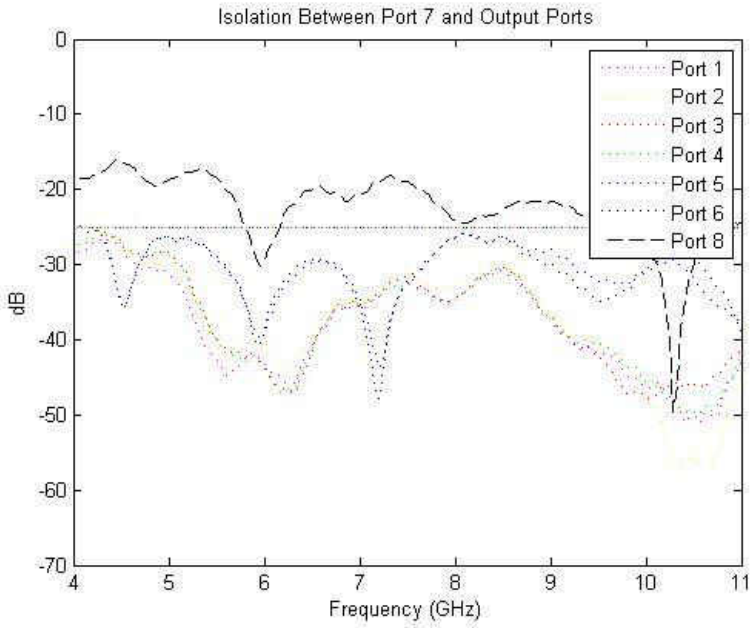

Figure 72: Isolation Between Port 7 and Output Ports

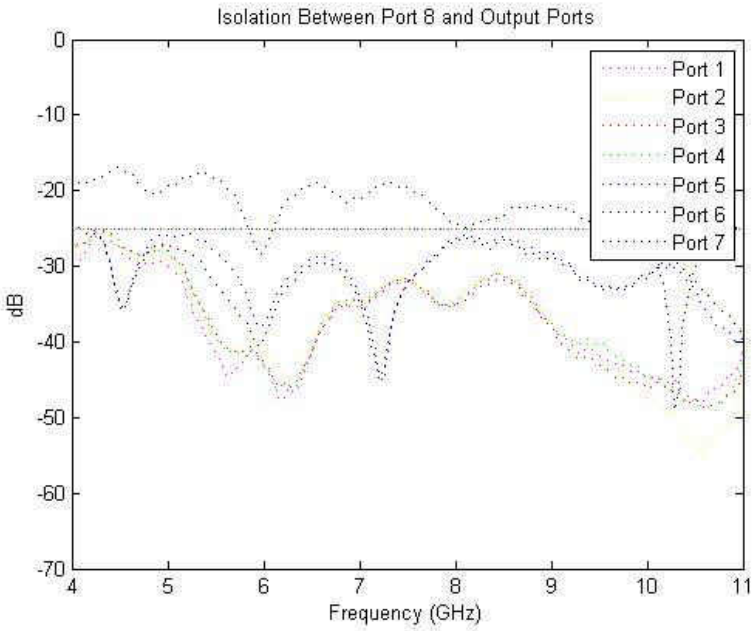

Figure 73: Isolation Between Port 8 and Output Ports

The phase errors for the Wilkinson power divider was also calculated through Matlab with the data that the VNA provided. The following graphs are the average phase error at each port measured between 4 -11 GHz.

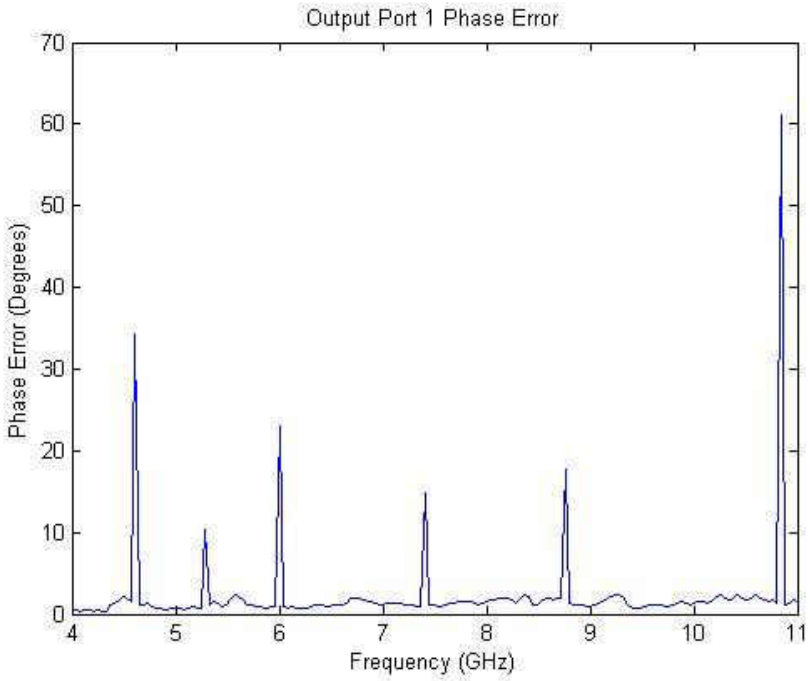

Figure 74: Output Port 1 Phase Error

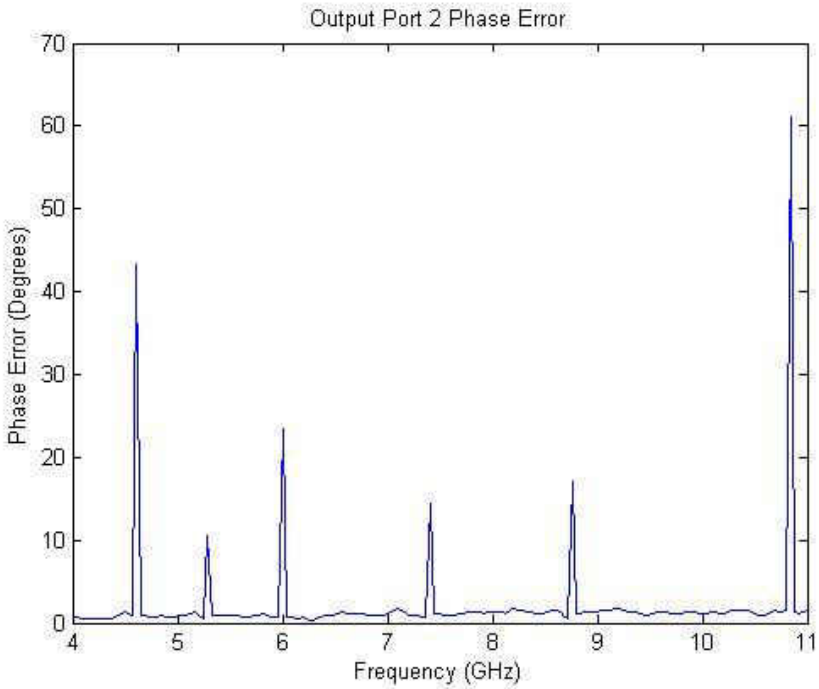

Figure 75: Ouput Port 2 Phase Error

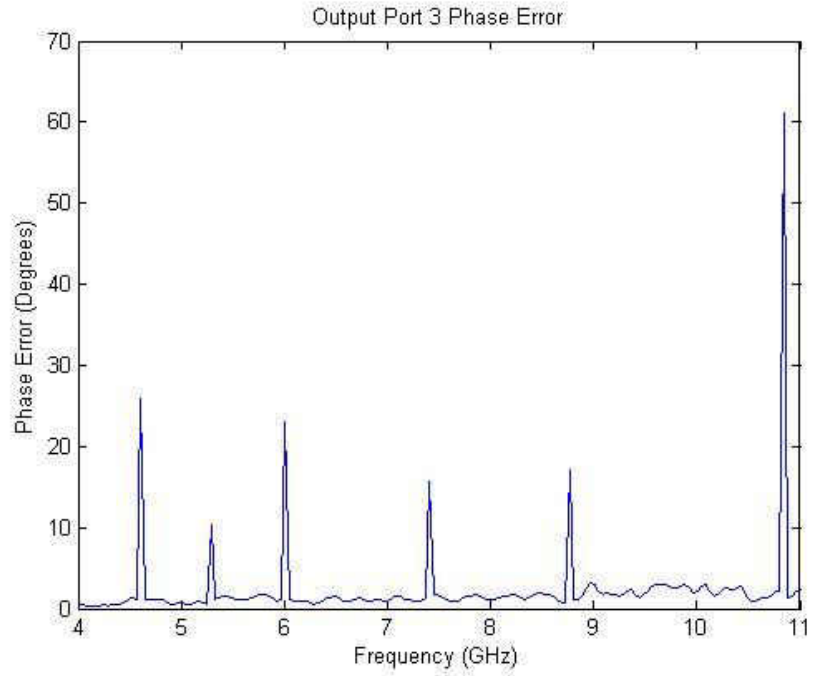

Figure 76: Output Port 3 Phase Error

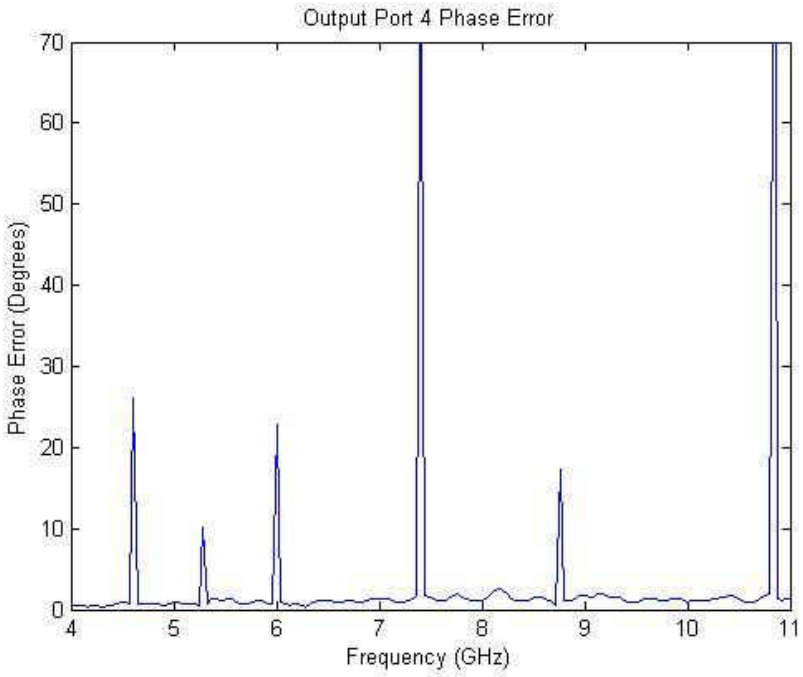

Figure 77: Output Port 4 Phase Error

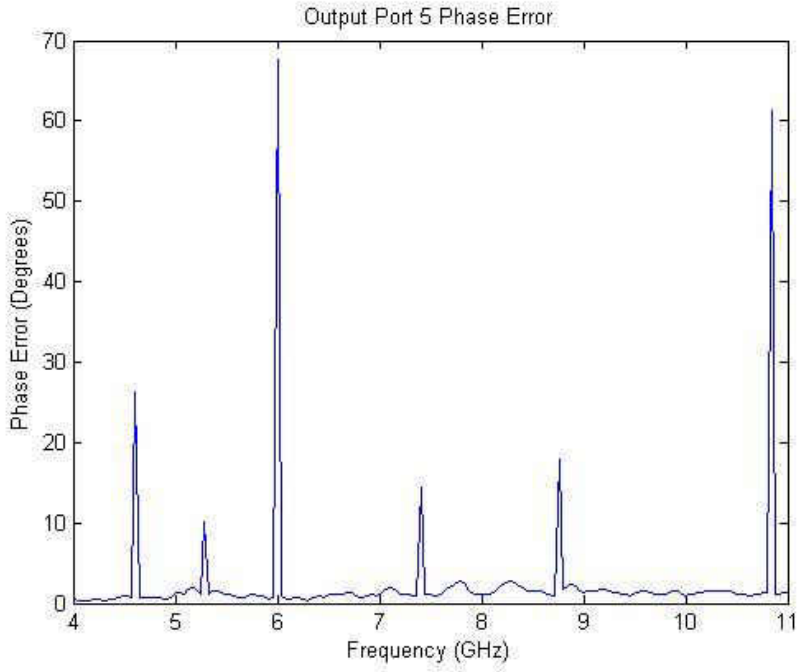

Figure 78: Output Port 5 Phase Error

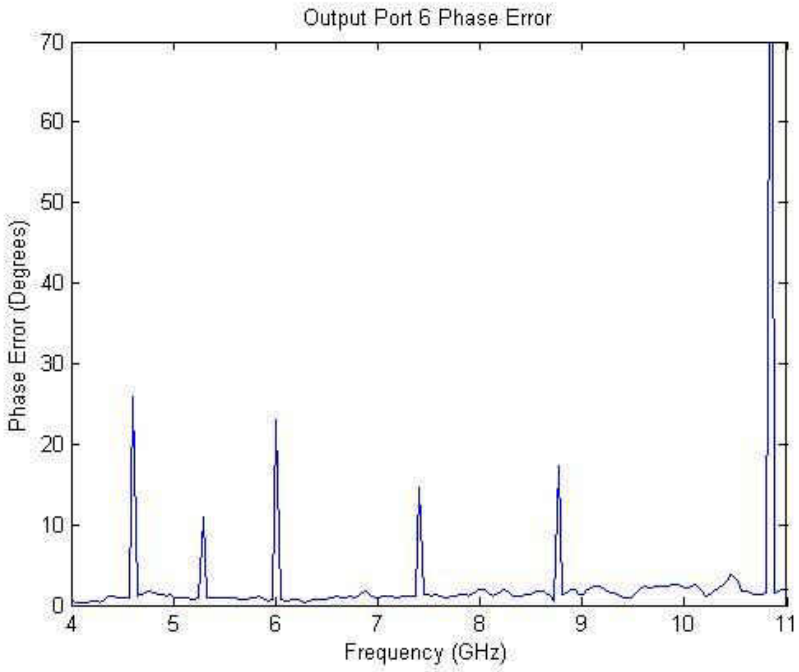

Figure 79: Output Port 6 Phase Error

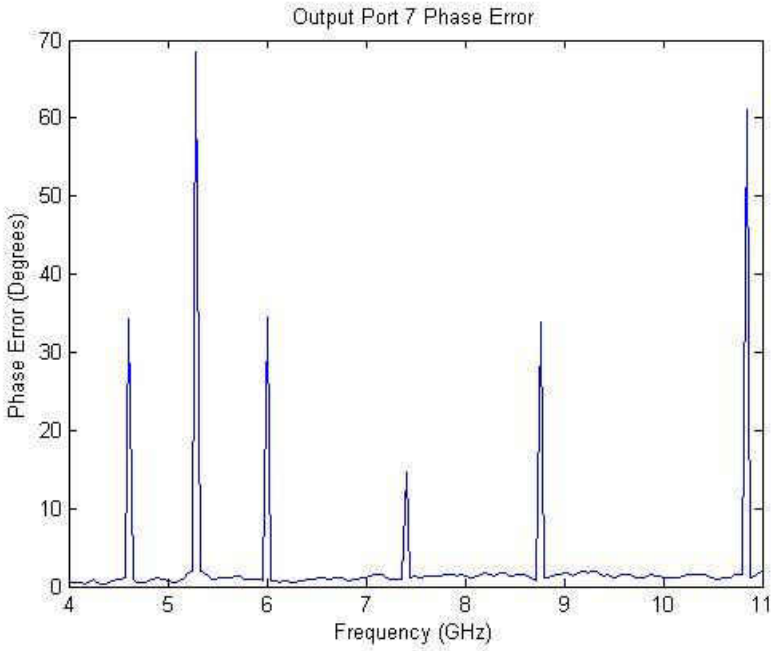

Figure 80: Output Port 7 Phase Error

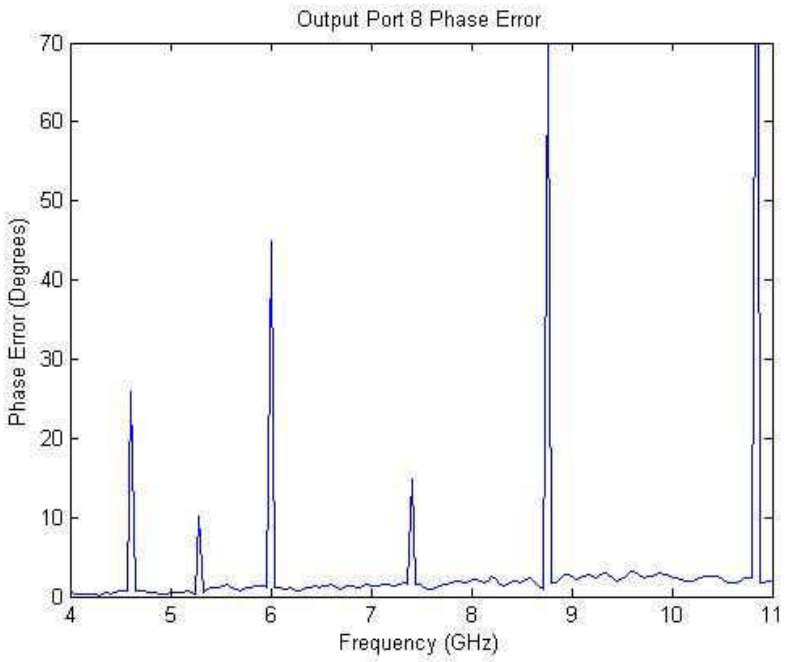

Figure 81: Output Port 8 Phase Error

APPENDIX B

MATLAB CODE

TRANSMISSION LINE MITERING

```
%% Mitering Transmission Lines
% University of North Dakota
% EGUANA

% For background on the calculations and formulas see the pages 170-176
% in Planar Microwave Engineering by Lee

%Clear the workspace
clear all;
close all;


%% Input the transmissio line widths
w1 = 12;    %Width of transmission line
w2 = 29;    %Width of transitioned to line


%% Calculate the dimensions for the bend
%Use trigonometry to calculate miter lengths
theta = atan(w1/w2);    %Angle of the chamfer relative to x axis
c = sqrt(w1^2+w2^2);
b = 0.4*c;    %Distance between corner and chamfer

%Calculations for w1
phi = asin(w1/c);
alpha = pi - theta - phi;
a = sin(alpha)*(c-b)/sin(phi);

%Calculations for w2
beta = pi/2 - phi;
ro = pi/2 - theta;
psi = pi - alpha;
d = sin(psi)*(c-b)/sin(beta);

%Determine the new lengths of the mitered sides
dif1 = round(a);    %Decrease in the outside w1 tline lengths
dif2 = round(d);    %Decrease in the outside w2 tline lengths
length = w1*5;  %Declare side length for illustration
out1 = length - dif1;
in1 = length - w1;
```

```
out2 = length - dif2;
in2 = length - w2;

%Create lines defining the mitered transmission line
x = [0,0,w2,w2,w2-dif1,-in1,-in1,0];
y = [0,in2,in2,dif2-w1,-w1,-w1,0,0];


%% Plot the mitered transmission line
figure(1)
plot(x,y,'-b')
hold on;
axis([-in1-w1 w2+in1 -w1*2 in2+w1])
title('Modeling a Mitered T-Line (mils)')
xlabel('Horizontal Dimensions (mils)')
ylabel('Vertical Dimensions (mils)')
text(-75,30,'(0,0)')
text(w2-dif1-30,-w1-25,['dx = ',num2str(w2-dif1),' , dy = ',num2str(-
w1)])
text(w2+25,dif2-w1,['dx = ',num2str(w2),' , dy = ',num2str(dif2-w1)])
text(-in1+20,-w1/2,['w1 = ',num2str(w1)])
text(w2+20,in2,['w2 = ', num2str(w2)])
set(figure(1),'WindowStyle','docked')
```

VNA Plots

```
%% Import .dat files into values
%Take the data files and turn them into 501x3 matrices for analysis
%Input to Output are without terminators or antennas
%Terminator have 50 ohm terminators on the outputs for a matched result
%Antennas have the 10GHz Vivaldi antennas attached at the end

% open('input to output1.dat')
% open('input to output2.dat')
% open('input to output3.dat')
% open('input to output4.dat')
% open('input to output5.dat')
% open('input to output6.dat')
% open('input to output7.dat')
% open('input to output8.dat')
% open('antenna1.dat')
% open('antenna2.dat')
% open('antenna3.dat')
% open('antenna4.dat')
% open('antenna5.dat')
% open('antenna6.dat')
% open('antenna7.dat')
% open('antenna8.dat')
% open('terminator1.dat')
% open('terminator2.dat')
% open('terminator3.dat')
```

```
% open('terminator4.dat')
% open('terminator5.dat')
% open('terminator6.dat')
% open('terminator7.dat')
% open('terminator8.dat')

%% Format the files to hold decimal places

format longE;
inputToOutput1;
format longE;
inputToOutput2;
format longE;
inputToOutput3;
format longE;
inputToOutput4;
format longE;
inputToOutput5;
format longE;
inputToOutput6;
format longE;
inputToOutput7;
format longE;
inputToOutput8;
format longE;
antenna1;
format longE;
antenna2;
format longE;
antenna3;
format longE;
antenna4;
format longE;
antenna5;
format longE;
antenna6;
format longE;
antenna7;
format longE;
antenna8;
format longE;
terminator1;
format longE;
terminator2;
format longE;
terminator3;
format longE;
terminator4;
format longE;
terminator5;
format longE;
terminator6;
format longE;
terminator7;
format longE;
terminator8;
```

```
%% Plot the S21 from unmatched ports

x = inputToOutput1(:,1);
y1 = inputToOutput1(:,2);
y2 = inputToOutput2(:,2);
y3 = inputToOutput3(:,2);
y4 = inputToOutput4(:,2);
y5 = inputToOutput5(:,2);
y6 = inputToOutput6(:,2);
y7 = inputToOutput7(:,2);
y8 = inputToOutput8(:,2);

figure(1)
plot(x,y1,'c',x,y2,'m',x,y3,'y',x,y4,'r',x,y5,'g',x,y6,'b',x,y7,'w',x,y
8,'k');
hold on

xlabel('Frequency');
ylabel('dB');
title('Empty Port(Unmatched) S21');
legend('Empty Port 1','Empty Port 2','Empty Port 3','Empty Port
4','Empty Port 5','Empty Port 6','Empty Port 7','Empty Port 8')
whitebg([.75,.75,.75])
set(gcf,'Color',[1,1,1])

%% Plot the S21 from matched ports with 50 ohm terminators

x = inputToOutput1(:,1);
t1 = terminator1(:,2);
t2 = terminator2(:,2);
t3 = terminator3(:,2);
t4 = terminator4(:,2);
t5 = terminator5(:,2);
t6 = terminator6(:,2);
t7 = terminator7(:,2);
t8 = terminator8(:,2);

figure(2)
plot(x,t1,'c',x,t2,'m',x,t3,'y',x,t4,'r',x,t5,'g',x,t6,'b',x,t7,'w',x,t
8,'k');
hold on

xlabel('Frequency');
ylabel('dB');
title('Terminated Ports (Matched) S21');
legend('Terminator Port 1','Terminator Port 2','Terminator Port
3','Terminator Port 4','Terminator Port 5','Terminator Port
6','Terminator Port 7','Terminator Port 8')
whitebg([.75,.75,.75])
set(gcf,'Color',[1,1,1])

%% Plot the S21 from unmatched ports with 50 ohm antennas

x = inputToOutput1(:,1);
```

```
a1 = antenna1(:,2);
a2 = antenna2(:,2);
a3 = antenna3(:,2);
a4 = antenna4(:,2);
a5 = antenna5(:,2);
a6 = antenna6(:,2);
a7 = antenna7(:,2);
a8 = antenna8(:,2);

figure(3)
plot(x,a1,'c',x,a2,'m',x,a3,'y',x,a4,'r',x,a5,'g',x,a6,'b',x,a7,'w',x,a
8,'k');
hold on

xlabel('Frequency');
ylabel('dB');
title('Antenna Ports (Matched) S21');
legend('Output Port 1','Output Port 2','Output Port 3','Output Port
4','Output Port 5','Output Port 6','Output Port 7','Output Port 8')
whitebg([.75,.75,.75])
set(gcf,'Color',[1,1,1])

%% Plot the S21 from Output port1 (antenna,unmatched,terminator)

x = inputToOutput1(:,1);
p1 = antenna1(:,2);
p2 = terminator1(:,2);
p3 = inputToOutput1(:,2);

figure(4)
plot(x,p1,'r--',x,p2,'b--',x,p3,'g--');
hold on

xlabel('Frequency');
ylabel('dB');
title('S21 from Output Port1');
legend('Antenna','Terminator','Empty')
whitebg([.75,.75,.75])
set(gcf,'Color',[1,1,1])

%Repeat 7 more times for each port comparison
```

PHASE ERROR CALCULATIONS

```
%% Phase Error for Open Ports

x = inputToOutput1(:,1);
p1 = inputToOutput1(:,3);
p2 = inputToOutput2(:,3);
p3 = inputToOutput3(:,3);
p4 = inputToOutput4(:,3);
p5 = inputToOutput5(:,3);
p6 = inputToOutput6(:,3);
p7 = inputToOutput7(:,3);
p8 = inputToOutput8(:,3);
```

```
figure (12)
plot(x,p1,'c',x,p2,'m',x,p3,'y',x,p4,'r',x,p5,'g',x,p6,'b',x,p7,'w',x,p
8,'k');
hold on
legend('Open Port 1','Open Port 2','Open Port 3','Open Port 4','Open
Port 5','Open Port 6','Open Port 7','Open Port 8')

xlabel('Frequency');
ylabel('Phase');
title('Phase Error for Open Ports');
whitebg([.75,.75,.75])
set(gcf,'Color',[1,1,1])

%% Phase Error for Antenna

x = inputToOutput1(:,1);
q1 = antenna1(:,3);
q2 = antenna2(:,3);
q3 = antenna3(:,3);
q4 = antenna4(:,3);
q5 = antenna5(:,3);
q6 = antenna6(:,3);
q7 = antenna7(:,3);
q8 = antenna8(:,3);

figure (13)
plot(x,q1,'c',x,q2,'m',x,q3,'y',x,q4,'r',x,q5,'g',x,q6,'b',x,q7,'w',x,q
8,'k');
hold on
legend('Antenna Port 1','Antenna Port 2','Antenna Port 3','Antenna Port
4','Antenna Port 5','Antenna Port 6','Antenna Port 7','Antenna Port 8')

xlabel('Frequency');
ylabel('Phase');
title('Phase Error for Antenna Ports');
whitebg([.75,.75,.75])
set(gcf,'Color',[1,1,1])

%% Phase Error for Terminated Ports

x = inputToOutput1(:,1);
r1 = terminator1(:,3);
r2 = terminator2(:,3);
r3 = terminator3(:,3);
r4 = terminator4(:,3);
r5 = terminator5(:,3);
r6 = terminator6(:,3);
r7 = terminator7(:,3);
r8 = terminator8(:,3);

figure (14)
plot(x,r1,'c',x,r2,'m',x,r3,'y',x,r4,'r',x,r5,'g',x,r6,'b',x,r7,'w',x,r
8,'k');
hold on
```

```
legend('Terminated Port 1','Terminated Port 2','Terminated Port
3','Terminated Port 4','Terminated Port 5','Terminated Port
6','Terminated Port 7','Terminated Port 8')

xlabel('Frequency');
ylabel('Phase');
title('Phase Error for Terminated Ports');
whitebg([.75,.75,.75])
set(gcf,'Color',[1,1,1])

%% Output 3 Output 8  Comparison

x = inputToOutput1(:,1);
s1 = terminator3(:,3);
s2 = terminator8(:,3);

figure(15)
plot(x,s1,'r',x,s2,'b');
hold on
axis([9000000000,11000000000,-inf,inf])
xlabel('Frequency');
ylabel('Phase');
title('Phase Error for Port3 and Port8');
whitebg([1, 1, 1])
set(gcf,'Color',[1,1,1])

%% Open Port Phase Error (Worst)

p3 = inputToOutput3(:,3);
p8 = inputToOutput8(:,3);
f1 = inputToOutput1(:,1);

for i = 1:501
    lambda = (3*10^8)/f1(i,1);
    k=(2*pi)/lambda;
    p_s=k*(p3(i,1) - p8(i,1));
    error_o(i) = abs(p_s/(180*pi));
end

error_ave_oworst = mean(error_o)
figure(1)
plot(f1,error_o)
xlabel('Frequency')
ylabel('Phase Error (Degrees)')
title('Open Port Phase Error')

%% Terminated Port Phase Error (Worst)

q3 = terminator3(:,3);
q8 = terminator8(:,3);
f1 = inputToOutput1(:,1);

for i = 1:501
```

```
    lambda = (3*10^8)/f1(i,1);
    k=(2*pi)/lambda;
    p_s=k*(q3(i,1) - q8(i,1));
    error_t(i) = abs(p_s/(180*pi));
end

error_ave_tworst = mean(error_t)
figure(2)
plot(f1,error_t)
xlabel('Frequency')
ylabel('Phase Error (Degrees)')
title('Terminated Port Phase Error')
axis([9000000000,11000000000,0,5])
%% Antenna Port Phase Error (Worst)

r3 = antenna3(:,3);
r8 = antenna8(:,3);
f1 = inputToOutput1(:,1);

for i = 1:501
    lambda = (3*10^8)/f1(i,1);
    k=(2*pi)/lambda;
    p_s=k*(r3(i,1) - r8(i,1));
    error_a(i) = abs(p_s/(180*pi));
end

error_ave_aworst = mean(error_a)
figure(3)
plot(f1,error_a)
xlabel('Frequency')
ylabel('Phase Error (Degrees)')
title('Antenna Port Phase Error')
axis([9000000000,11000000000,0,5])

%% Open Port Phase Error (Best)

p3 = inputToOutput1(:,3);
p8 = inputToOutput5(:,3);
f1 = inputToOutput1(:,1);

for i = 1:501
    lambda = (3*10^8)/f1(i,1);
    k=(2*pi)/lambda;
    p_s=k*(p3(i,1) - p8(i,1));
    error_o(i) = abs(p_s/(180*pi));
end

error_ave_obest = mean(error_o)
figure(4)
plot(f1,error_o)
xlabel('Frequency')
ylabel('Phase Error (Degrees)')
title('Open Port Phase Error')
axis([9000000000,11000000000,0,5])
%% Terminated Port Phase Error (Best)
```

```
q3 = terminator1(:,3);
q8 = terminator5(:,3);
f1 = inputToOutput1(:,1);

for i = 1:501
    lambda = (3*10^8)/f1(i,1);
    k=(2*pi)/lambda;
    p_s=k*(q3(i,1) - q8(i,1));
    error_t(i) = abs(p_s/(180*pi));
end

error_ave_tbest = mean(error_t)
figure(5)
plot(f1,error_t)
xlabel('Frequency')
ylabel('Phase Error (Degrees)')
title('Terminated Port Phase Error')
axis([9000000000,11000000000,0,5])
%% Antenna Port Phase Error (Best)

r3 = antenna1(:,3);
r8 = antenna5(:,3);
f1 = inputToOutput1(:,1);

for i = 1:501
    lambda = (3*10^8)/f1(i,1);
    k=(2*pi)/lambda;
    p_s=k*(r3(i,1) - r8(i,1));
    error_a(i) = abs(p_s/(180*pi));
end

error_ave_abest = mean(error_a)
figure(6)
plot(f1,error_a)
xlabel('Frequency')
ylabel('Phase Error (Degrees)')
title('Antenna Port Phase Error')
axis([9000000000,11000000000,0,5])

%% Antenna Average Phase Error for Port 1

a1 = antenna1(:,3);
a2 = antenna2(:,3);
a3 = antenna3(:,3);
a4 = antenna4(:,3);
a5 = antenna5(:,3);
a6 = antenna6(:,3);
a7 = antenna7(:,3);
a8 = antenna8(:,3);
f1 = inputToOutput1(:,1);

for i = 1:501
    lambda = (3*10^8)/f1(i,1);
    k=(2*pi)/lambda;
```

```
    p_s=k*(a1(i,1) - a2(i,1));
    error_2(i) = abs(p_s/(180*pi));
end
for i = 1:501
    lambda = (3*10^8)/f1(i,1);
    k=(2*pi)/lambda;
    p_s=k*(a1(i,1) - a3(i,1));
    error_3(i) = abs(p_s/(180*pi));
end
for i = 1:501
    lambda = (3*10^8)/f1(i,1);
    k=(2*pi)/lambda;
    p_s=k*(a1(i,1) - a4(i,1));
    error_3(i) = abs(p_s/(180*pi));
end
for i = 1:501
    lambda = (3*10^8)/f1(i,1);
    k=(2*pi)/lambda;
    p_s=k*(a1(i,1) - a5(i,1));
    error_4(i) = abs(p_s/(180*pi));
end
for i = 1:501
    lambda = (3*10^8)/f1(i,1);
    k=(2*pi)/lambda;
    p_s=k*(a1(i,1) - a6(i,1));
    error_5(i) = abs(p_s/(180*pi));
end
for i = 1:501
    lambda = (3*10^8)/f1(i,1);
    k=(2*pi)/lambda;
    p_s=k*(a1(i,1) - a7(i,1));
    error_6(i) = abs(p_s/(180*pi));
end
for i = 1:501
    lambda = (3*10^8)/f1(i,1);
    k=(2*pi)/lambda;
    p_s=k*(a1(i,1) - a8(i,1));
    error_7(i) = abs(p_s/(180*pi));
end
for i = 1:501
    lambda = (3*10^8)/f1(i,1);
    k = (2*pi)/lambda;
    p_s=k*(a1(i,1) - a2(i,1));
    error_8(i) = abs(p_s/(180*pi));
    end

  error_total =
error_2+error_3+error_4+error_5+error_6+error_7+error_8;
  error_avg_port1= mean(error_total)/7
```

ISOLATION PLOT

```
%% Isolation Plot Port 1
```

```
format longE;
Isolation12;
format longE;
Isolation13;
format longE;
Isolation14;
format longE;
Isolation15;
format longE;
Isolation16;
format longE;
Isolation17;
format longE;
Isolation18;

x = Terminator1(:,1);
i12 = Isolation12(:,2);
i13 = Isolation13(:,2);
i14 = Isolation14(:,2);
i15 = Isolation15(:,2);
i16 = Isolation16(:,2);
i17 = Isolation17(:,2);
i18 = Isolation18(:,2);

figure(1)
plot(x,i12,'m',x,i13,'y',x,i14,'r',x,i15,'g',x,i16,'b',x,i17,'w',x,i18,
'k');
hold on

xlabel('Frequency');
ylabel('dB');
title('Isolation Between Port 1 and Output Ports');
legend('Port 2','Port 3','Port 4','Port 5','Port 6','Port 7','Port 8')
whitebg([.75,.75,.75])
set(gcf,'Color',[1,1,1])

% Repeat 7 more times to get each plot.
```

S11 PLOT

```
%% Terminator

format longE;
Terminator1;
format longE;
Terminator2;
format longE;
Terminator3;
format longE;
Terminator4;
format longE;
Terminator5;
format longE;
Terminator6;
```

```
format longE;
Terminator7;
format longE;
Terminator8;

x = Terminator1(:,1);
t1 = Terminator1(:,2);
t2 = Terminator2(:,2);
t3 = Terminator3(:,2);
t4 = Terminator4(:,2);
t5 = Terminator5(:,2);
t6 = Terminator6(:,2);
t7 = Terminator7(:,2);
t8 = Terminator8(:,2);

figure(1)
plot(x,t1,'c',x,t2,'m',x,t3,'y',x,t4,'r',x,t5,'g',x,t6,'b',x,t7,'w',x,t
8,'k');
hold on

xlabel('Frequency');
ylabel('dB');
title('Terminated Ports (Matched) S11');
legend('Terminator Port 1','Terminator Port 2','Terminator Port
3','Terminator Port 4','Terminator Port 5','Terminator Port
6','Terminator Port 7','Terminator Port 8')
whitebg([.75,.75,.75])
set(gcf,'Color',[1,1,1])

%Repeat for the antenna
```

ARRAY FACTOR CODE

```
%% Inputs

rad = pi/180;
N = 8;
d = .5;
theta_0 = input('Enter beam direction (degrees): ');
error = input('Enter the error type: amplitude: (a), phase: (pn,pu),
failure: (f) ','s');
for i = 1:N
    a(i) = 1;
end
theta_0 = theta_0 * rad;

%% Constants

k = 2 * pi;
t_min = 0;
d_t = .1;
t_max = 180;

for i = 1:20
   [AF(i,:), AFe(i,:), ae(i,:)] = ...
```

```
       OddArray(N, d, k, a, theta_0, error, t_min, d_t, t_max, rad);
   normAF(i,:) = abs(AF(i,:)) ./ max(abs(AF(i,:)));
   logAF(i,:) = 20 .* log10(normAF(i,:));

   normAFe(i,:) = abs(AFe(i,:)) ./ max(abs(AFe(i,:)));
   logAFe(i,:) = 20 .* log10(normAFe(i,:));
end

theta = t_min:d_t:t_max;
for i = 1:20
    UnormAF(i,:) = normAF(i,:) .* conj(normAF(i,:));% .* conj(normAF);
    DAFdB(i) = Dirsym(UnormAF(i,:), d_t, rad);

    UnormAFe(i,:) = normAFe(i,:) .* conj(normAFe(i,:));
    DAFedB(i) = Dirsym(UnormAFe(i,:), d_t, rad);

    [R_max(i) loc_AFe(i)] = max(logAFe(i,:));
    center(i) = (loc_AFe(i) * d_t) - d_t;

    iter = 0;
    while (logAFe(i,loc_AFe(i) + iter) >= -3)
        iter = iter + 1;
    end
    HPBWr = (loc_AFe(i) + iter) * d_t;
    iter = 0;
    while (logAFe(i,loc_AFe(i) - iter) >= -3)
        iter = iter + 1;
    end
    HPBW1 = (loc_AFe(i) - iter) * d_t;
    AFe_HPBW(i) = HPBWr - HPBW1;

    iter = 0;
    n = 1;
    while (loc_AFe(i) + iter) < (length(logAFe(i,:))-1)
        iter = iter + 1;
        if (logAFe(i,loc_AFe(i) + iter - 1) < logAFe(i,loc_AFe(i) +
iter)) ...
                && (logAFe(i,loc_AFe(i) + iter + 1) <
logAFe(i,loc_AFe(i) + iter))
            AFe_SLLr_loc(i,n) = (loc_AFe(i) + iter - 1) * d_t;
            AFe_SLLr(i,n) = logAFe(i,loc_AFe(i) + iter);
            n = n + 1;
        end
    end

    iter = 0;
    n = 1;
    while (loc_AFe(i) - iter) > 2
        iter = iter + 1;
        if (logAFe(i,loc_AFe(i) - iter - 1) < logAFe(i,loc_AFe(i) -
iter)) ...
                && (logAFe(i,loc_AFe(i) - iter - 1) <
logAFe(i,loc_AFe(i) - iter))
            AFe_SLLl_loc(i,n) = (loc_AFe(i) - iter - 1) * d_t;
            AFe_SLLl(i,n) = logAFe(i,loc_AFe(i) - iter);
```

```
            n = n + 1;
        end
    end
end

Pointerror = center
HP = AFe_HPBW
Directivity = DAFedB

for i = 1:20
    [RightSLL(i) r_max] = max(AFe_SLLr(i,:));
    if RightSLL(i) == 0
        AFe_SLLr(i,r_max) = -100;
        [RightSLL(i) r_max] = max(AFe_SLLr(i,:));
        if RightSLL(i) == 0
            AFe_SLLr(i,r_max) = -100;
            [RightSLL(i) r_max] = max(AFe_SLLr(i,:));
            if RightSLL(i) == 0
                AFe_SLLr(i,r_max) = -100;
                [RightSLL(i) r_max] = max(AFe_SLLr(i,:));
                if RightSLL(i) == 0
                    AFe_SLLr(i,r_max) = -100;
                    [RightSLL(i) r_max] = max(AFe_SLLr(i,:));
                end
            end
        end
    end

    RightLoc(i) = AFe_SLLr_loc(i,r_max);

    [LeftSLL(i) l_max] = max(AFe_SLLl(i,:));
    if LeftSLL(i) == 0
        AFe_SLLl(i,l_max) = -100;
        [LeftSLL(i) l_max] = max(AFe_SLLl(i,:));
        if LeftSLL(i) == 0
            AFe_SLLl(i,l_max) = -100;
            [LeftSLL(i) l_max] = max(AFe_SLLl(i,:));
            if LeftSLL(i) == 0
                AFe_SLLl(i,l_max) = -100;
                [LeftSLL(i) l_max] = max(AFe_SLLl(i,:));
                if LeftSLL(i) == 0
                    AFe_SLLl(i,l_max) = -100;
                    [LeftSLL(i) l_max] = max(AFe_SLLl(i,:));
                end
            end
        end
    end

    LeftLoc(i) = AFe_SLLl_loc(i,l_max);
end

RightSLL = RightSLL
RightLoc = RightLoc
LeftSLL = LeftSLL
LeftLoc = LeftLoc
```

```
figure(1);
plot(theta,logAF(1,:),'k-.',theta,logAFe(2,:),'r-');
grid on;
title('Array Factor');
xlabel('\theta (degrees)');
ylabel('AF(\theta) dB (normalized)');
axis([0,180,-100,0])
set(gcf,'Color',[1,1,1])
```

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