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Fast Transients in Non-Volatile Resistive Memories (RRAM) Using Tantalum Pentoxide as Solid Electrolyte

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FAST TRANSIENTS IN NON-VOLATILE RESISTIVE MEMORIES (RRAM) USING TANTALUM PENTOXIDE AS SOLID ELECTROLYTE

by

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ABSTRACT

FAST TRANSIENTS IN NON-VOLATILE RESISTIVE MEMORIES (RRAM) USING TANTALUM PENTOXIDE AS SOLID ELECTROLYTE

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Old Dominion University, 2013
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The semiconductor electronics industry has followed Moore's law austerely since 1965 fueling the microelectronics revolution and major technological advancements. Over the recent decades, the semiconductor industry has proven to be very successful, particularly by scaling the geometry of devices ever smaller. The device scaling has been very effective in boosting productivity yielding astonishing integration levels while simultaneously dramatically dropping the price per bit. However, the future of device scaling remains unclear. It is certain that device scaling will face severe reliability, cost and energy issues in the future. Therefore, there is a need to identify alternative technology platforms. Reconfigurable devices are considered as one of the key alternatives.

However, the widespread aggressive acceptance of reconfigurable devices in the semiconductor industry faces many different challenges. One of the major challenges is the size of the switching matrix. One solution to overcome this challenge is to replace the present SRAM (Static Random Access Memory) switch with a non-volatile resistive memory switch. Some of the advantages of these switches are low cost, CMOS compatibility and simple structure.

Given such advantages, it is essential to elucidate the working principle as well as the reliability issues. Since these non-volatile resistive switch devices are new to the semiconductor electronics industry, it is crucially important to explore novel structures for improved device architectures and to develop adequate measurement techniques to inspect and characterize these novel resistive switch devices. In this thesis, novel structures of RRAM devices with constricted electrode area close to the size of a single conducting filament of around 10 nm have been explored to improve device performance. Also, new measurement setups have been developed and proprietary test circuits have been designed, built and tested in order to acquire accurate and reliable data to investigate device performance. Some of the notable achievements of the developed measurement setups are measurement capability of switching transient with accuracy of 4 ns, high resistance measurements up to 1.6 GΩ, accurate endurance test within 1 ms/cycle and limiting current during SET to < 20 μA without noticeable overshoot within 500 ps.

To my parents Pradeep Das Shrestha and Chandu Shrestha and to my life partner

Pusker Raj Regmi

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CHAPTER 1

INTRODUCTION

1.1 Background

Recently resistive switches have gained much attention and popularity in the field of memory technology [1-5]. These two terminal devices are excellent candidates for non-volatile memories due to their simplicity, small size and low cost [6]. Due to similar reasons mentioned for memory devices, these devices also have the potential to work as high performance switches for interconnect architectures [7].

These two terminal devices switch from a high resistance to a low resistance state by applying voltage across the two electrodes of a Metal-insulator-Metal structure. These structures can change their resistance state from high (R_{OFF}) to low (R_{ON}) depending on the voltage applied. Some of these devices can switch their state from R_{OFF} to R_{ON} and vice versa with the same voltage polarity, and consequently, they are named unipolar switches. The other kind of resistive switches are able to switch their state only by reversing the voltage polarity and therefore are known as bipolar switches. This dissertation is investigating bipolar switches with a Cu/Ta_2O_5/Pt stack, where Ta_2O_5 serves as the solid electrolyte.

In a very simple scenario, switching in bipolar resistive devices is attributed to the migration of metal ions, which either form a metal conductive filament or dissolve it by diffusion of the ions depending on the polarity of the externally applied electric field. A solid electrolyte is sandwiched between two metal electrodes as shown in Figure 1. One

of the metal electrodes is inert and the other electrode oxidizes quickly to form the required metal ions. These ions are made to migrate from the oxidizing metal electrode towards the inert metal by applying an appropriate voltage to form a dendritic metal filament. The two metal electrodes are shortened when the growing metal filament reaches the other inert electrodes. This causes the device to change its state to low resistance. This is termed the SET process. When the reverse voltage is applied, the ions diffuse in the opposite direction and move away from the inert metal electrode. This will lead to the dissolution and break-up of the conducting metal filament and thus changing to the high resistance state. This is termed the RESET process. Since the voltage applied to change the state from one to the other is reversed, it is a bipolar switch.

An example of Banno et al is used to explain the working of the $Pt/Ta_2O_5/Cu$ device stack. The Ta_2O_5 solid electrolyte is sandwiched between the Pt and Cu electrodes [8]. Here the Pt electrode serves as the inert electrode and the Cu electrode provides the ions to form the metal filament. When a positive voltage is applied at the Cu electrode, an electro-chemical reaction takes place at the interface between the Cu and Ta_2O_5 to form positive Cu^+ ions. Because of the applied electric field between the two electrodes, the Cu^+ ions migrate towards the negatively charged Pt electrode. At the Pt electrode, these Cu^+ ions are reduced to form Cu precipitates. These Cu precipitates now start to grow directionally from the Pt electrode along the electric field lines to form a dendritic filament that eventually touches the Cu electrode to form a low resistance Cu bridge between the two electrodes (termed SET). When a reverse polarity is applied; i.e. when negative voltage is applied to the Cu electrode, the diffused Cu^+ ions in the electrolyte move towards the negative Cu electrode dissolving and breaking up the existing metal

filament short between the two electrodes. This results in the high resistance state (termed RESET).

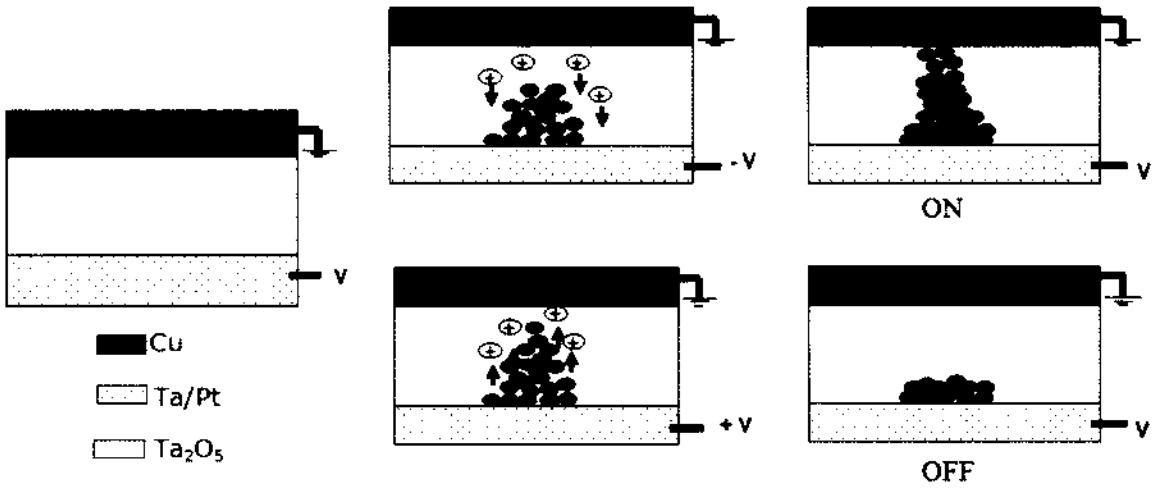


Figure 1. Formation and dissolution of a conductive metal filament in a nano-crossbar switch fabricated with solid electrolytes.

These low and high resistance states can be seen by applying voltages lower than the RESET and SET voltages of the switch. Therefore, the sensing of the state is non-destructive. The low resistance state is retained until the metal filament has been dissolved and broken; i.e. when the RESET voltage is applied. The same is true for the high resistance state. Therefore, the resistance state acquired by the device is non-volatile. This constitutes a significant advantage of resistive switches in comparison to conventional memory devices like DRAMs.

1.2 Motivation

From the above discussions it is clear that resistive switches are simple in structure, and furthermore CMOS compatible and non-volatile. All of these advantages render resistive switches plausible candidates for future memory device technologies and interconnect switches for reconfigurable devices. The following section provides an overview of the present status of the existing memory technologies and reconfigurable device technology. The need for novel technology approaches in the field of resistive switches is discussed.

Memory Devices

The memory industry has come a long way from the early magnetic and mechanical memory devices to the prevalent solid-state storage device. The modern Solid-State Devices (SSDs) are preferred due to significant advantages like size, noiseless, reduced cost, higher speed, improved reliability etc. SSDs can be divided primarily into volatile and non-volatile memories. Volatile memories lose all stored information when the system power is turned off, whereas non-volatile memories do not lose their information. Non-volatility is always a desirable advantage as these memories do not require another memory to store the data.

Flash Memory

Flash memory is a non-volatile memory. It gained much attention and became a game changer in the SSD [9]. Thus far, the biggest advantage of flash memory has been its small size. Flash memory consists of a single transistor cell with a double gate as shown in Figure 2. The memory state of flash memory is defined by the voltage shift due to the

charge stored in the floating gate. Flash memory can have relatively high density, therefore it is compact and inexpensive to fabricate [10]. Most of the time flash memory is used as a data storage device due to its slow operating speed 1 ms and 0.1 ms for write and read respectively [11].

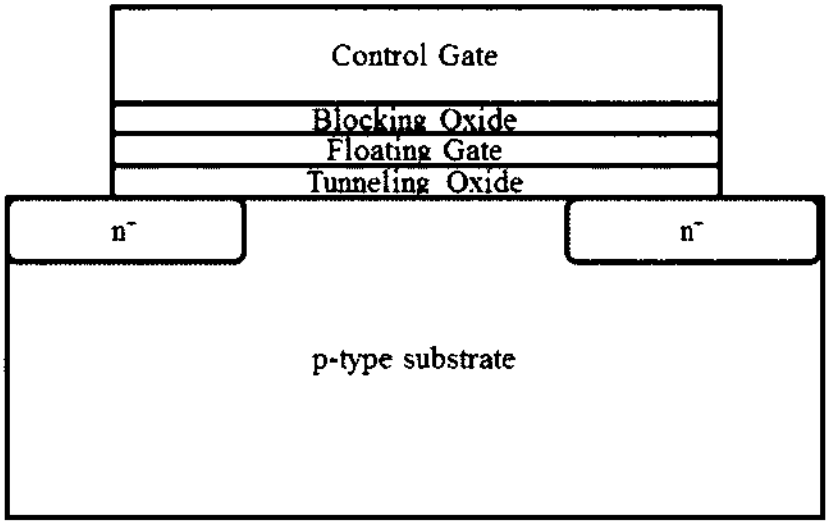


Figure 2. Schematic depiction of a Floating Gate (FG) flash memory [10].

However, some critical issues may work against it in the future due to device scaling. As the device size decreases so does the charge in the floating gate. This lowers the threshold voltage shift margin, making it less reliable. The next significant issue is the power. It is always desirable to decrease the operating voltage of the device. But for flash memory there is a limit up to which this can be done due to reliability issues like bit error, retention time [12] and low operating speed [13].

Dynamic Random Access Memory (DRAM)

The Dynamic Random Access Memory (DRAM) is a volatile memory that consists of one capacitor and one transistor memory cell. A schematic of a 1-transistor- 1-capacitor (1T-1C) DRAM cell is shown in Figure 3. The memory states for a DRAM cell are represented by two charge storage levels of the storage capacitor. DRAMs gained popularity due to its simple structure and fast write/read time of tens of nanoseconds.

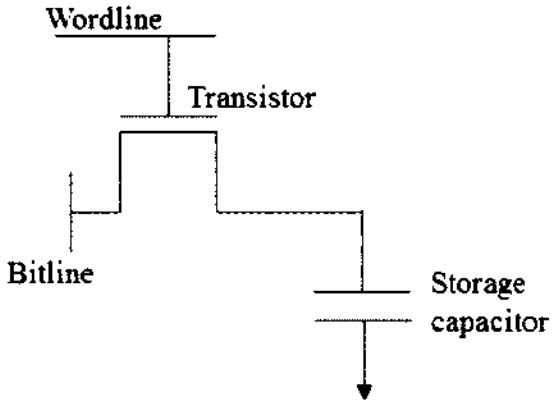


Figure 3. Schematic of a 1T-1C DRAM cell [14].

DRAM memory cells have the advantage of very fast access but they suffer from high refresh rates and poor scalability. In DRAM cells, the digital memory data bits are stored as electrical charge in the capacitor. However, the charge in the capacitor leaks due to leakage currents, which causes the stored data to be lost. Therefore the electrical charge in the storage capacitor has to be refreshed to its original level every 5-10 ms. DRAM operation requires an external circuitry block to refresh the DRAM cells. This DRAM refresh circuitry design requirement comes with a huge area and power loss. The poor scalability of DRAM cells is due to the capacitor. The storage capacitor should have the

capacity to hold a sufficient charge for sensing the charge state during the read and write cycles. Therefore, the size of the transistor can be readily decreased but it is much more difficult to decrease the size of the capacitor because of the need to maintain a critical minimum capacitor charge.

From the above discussions, it can be deduced that the conventional memory technology will reach the scalability limits in the near future. Therefore, it is critically important to research and develop novel memory device technologies to ensure a smooth transition to successor technologies when the current conventional memory technologies have reached their physical limits. There are various emerging memories such as MRAM (Magnetic RAM), PCM (Phase Change Memory) and RRAM (Resistive RAM or resistive switches) that are being explored as replacement and successor technologies to the above-mentioned conventional memories. Among these newly emerging memories, RRAM seems to be a very promising technology [11, 15, 16].

Reconfigurable Devices

So far, the microelectronics industry has used device scaling for many decades to achieve the expectations of "Moore's Law" [17]. In addition, device scaling according to Dennard's scaling theory is holding true in achieving high operating speed and high efficiency. Device scaling for relentless productivity increase has been used so aggressively in the semiconductor industry that the utilization of the devices for better performance has been ignored. The devices fabricated so far have not been used to their full potential. If the efficiency of the devices can be increased with same scaling factor, the industry will be able to delay the inevitable demise of Moore's Law. Researchers [7, 18] have suggested that appropriate architectures can be used to obtain faster and more

efficient systems with the same devices. Presently system designers are kept busy exploring such architectures for better performance without making changes at the device level. Reconfigurable devices are one of the tools that the system designers use to solve the architectural intricacies. Reconfigurable devices have the remarkable ability to adapt to usage. This characteristic can be employed advantageously to modify the devices according to the application with the least energy and time consumption. This can be viewed as the backbone to amplify efficiency.

One example of such use of reconfigurable devices is the partition of the embedded system [18]. In this case, the embedded system is partitioned into software and hardware tasks. The hardware code is capable of performing a task in a single clock cycle which otherwise would require several clock cycles due to the large set of instructions in the software. The codes that are most often used are identified and converted into the hardware codes. Doing so increases the speed of the task performed and simultaneously decreases the energy consumption. For instance, the microprocessor consumes significantly more power to perform a small task than when the same task is being performed by the hardware code. In addition, more energy is needed to power the microprocessor and all tasks that need to be executed at the software level take more time. Therefore, keeping the microprocessor in a standby mode, while the tasks are being performed by the hardware code, saves time as well as energy.

Another area that is going to benefit from reconfigurable devices is the device reliability. As mentioned earlier, the reliability of the devices becomes questionable with massive and aggressive scaling of solid-state devices (SSDs). This leads to more energy consumption, and increased effort and cost to obtain reliable devices. This fundamental

problem can be avoided by using less reliable devices but with better performance [19]. At first glance, this may not sound intuitive or logical, but this is precisely what the appropriate use of reconfigurable devices can achieve. This astonishing task can be performed by rerouting the data signals from the defective paths. The key is capitalizing on the ability of reconfigurable devices to rearrange according to the requirements. It should be noted that the part of the system that checks for the errors should be very reliable and in parallel to other methods such as redundancy, which should be used for errorless performance.

These examples suggest that reconfigurable devices are poised to play a very important role in the future of microelectronics for the semiconductor industry. Until recently, there were technological challenges and difficulties that prevented reconfigurable devices from being widely used. Some of these challenges are:

- Increased application design complexity
- Limited applications
- Compilation time
- Device cost

The most important challenge would be the limited application. If the potential applications are limited, then there is no incentive in undertaking a big effort to develop a new separate system to achieve better performance. The reasons for such limited applications are slow clock frequency due to the routing delays, size and fast computations. The root cause for all these technical problems is the switching matrix that controls the routes of the signals.

Let us take an example of a Field Programmable Gate Array (FPGA) shown in Figure 4 [20]. An FPGA has two important blocks, namely, the configurable logic block (CLB) and the switching block. The picture shown here is a simple representation of the embedded system. This is quite misleading as the switching blocks are very large compared to the CLBs and account for 70% of the total area [7]. The actual picture of a single switch is shown in Figure 4 b). A single switch consists of a six-transistor SRAM (Static Random Access Memory) cell with a pass transistor and memory to keep the state non-volatile.

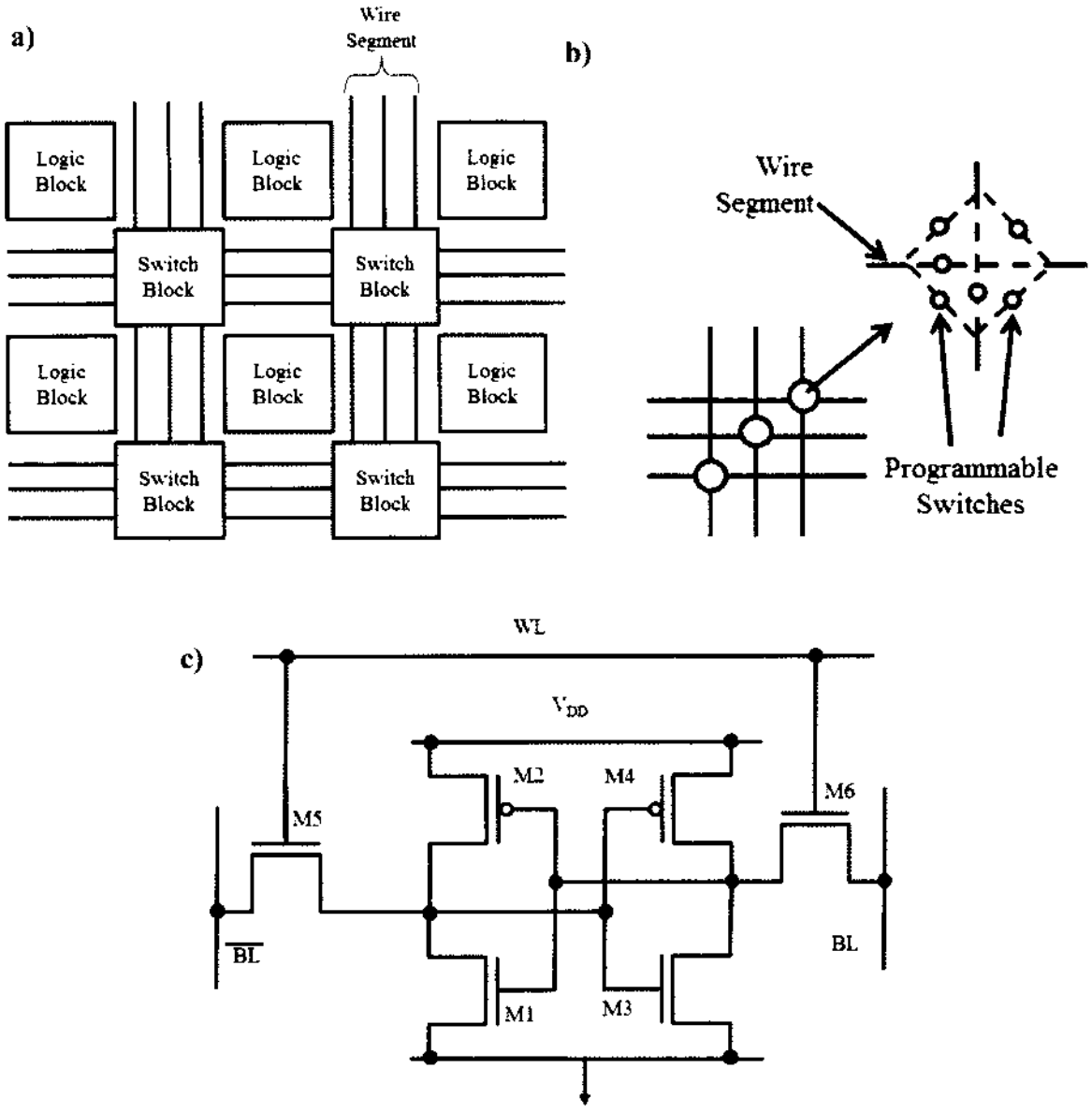


Figure 4. a) Simple schematic representation of logic blocks and switching blocks, b) Each intersection consists of number of programmable switches, c) example of a conventional 6 transistor SRAM cell for each switch.

Two important effects and consequences of using SRAMs are; 1) the high ON resistance and 2) the long lengths of interconnects due to the large area. Therefore, the RC delay of the circuit is very high. To minimize this delay, the use of switches is minimized as much

as possible. One way to do this is by increasing the granularity of the architecture i.e. the size of the logic block is increased instead of the switching block, so that most of the operation can be performed by a single logic block. This limits the application of such systems as the utilization is low i.e. more energy is required to perform minor operations due to the large grain size. Therefore, the design of the FPGA requires calculation of the optimum point where the utilization and the RC delay congregate. Because of such large RC delays, the clock frequency of the system cannot go very high and is compromised instead. This again limits the application, as slow clock frequency might not be desirable to the vast number of applications.

It is therefore clear that the switch size is the major challenge that prevents the wide use of reconfigurable devices [7]. This problem can be solved by employing a nano-crossbar two terminal switches architecture that significantly brings down the size of the switches in the switching matrix. It should be noted that since these switches can be fabricated by stacking the electrode and solid electrolyte along with the crossing interconnect system; this architecture can reduce the switch to almost miniscule size.

Basic Objectives of a High Performance Switch

The overriding objective for a high performance switch is to obtain a high endurance, long retention time, high R_{ON}/R_{OFF} ratio, low On resistance and size comparable to the interconnect. All of this can be controlled if the working mechanism of the new switch device is well understood.

- High R_{OFF}: The off resistance should be as high as >1 GΩ to insure that no signal is being passed from one block to the other.

- Low R_{ON}: The R_{ON} is expected to be below 1 kΩ to beat the input resistance of the present SRAM switch to decrease the routing delays.
- Size comparable to interconnect: The size is expected to be around the size of interconnect for ease of fabrication and to prevent any extra area of Si being required.
- SET/RESET time: The switching time should be aimed to <100 μs.
- Current retention time: Contrary to the conventional memory devices, where the signals are used for switching and sensing, for switch purposes only the devices should be able to handle current flow through it for longer timeframes. The reason for this is that the current has to flow through the switch in order to complete the circuit. The current that can be flowing through the switch without changing the state of the switch is aimed to be > 200 μA.
- High endurance: High endurance is important because it is being aimed to build a reconfigurable device capable of rerouting and checking the reliability of the devices. Therefore, the reconfigurable device should be in good position to be switched for a very large number of switching cycles. As a rule of thumb, a start value can be taken to be 10^4 cycles.

1.3 Literature Review

Materials

Numerous materials such as CuS, SiO_2, Ag-Ge-Se,Ge-S, TaO_x, TaSiO, HfO_2 [21-30] have been investigated for solid electrolyte switching, where one electrode is inert and

the other oxidizable. In all the above-mentioned solid electrolytes systems either Cu or Ag is used as the oxidizing electrode. These devices are bipolar in nature, thus the switching is attributed to the mobile metal ions in the electrolyte forming conducting metal filaments. The use of SiO_2 does seem very tempting due to its well proven compatibility with CMOS processing [22] and SiO_2 being the most widely used and best understood insulating material. The endurance achieved with SiO_2 is also very high and can reach 10^7. Though the endurance and CMOS compatibility is excellent, the R_{ON} and R_{OFF} distribution does not seem very convincing. Most of the results of these devices lack the controllability of the voltage used for switching. In the case of CuS solid electrolyte, the switching voltage is below +/- 0.2V[31]. On the other hand, Ta_2O_5 shows very promising results with controllable switching voltage and better distribution of R_{ON} and R_{OFF} and good endurance [25].

Resistive Switches with Ta_2O_5

Ta_2O_5 has been extensively studied for the past four decades resulting in efficacies in multiple areas of the semiconductor industry [32]. Early research on the material was due to its high antireflective index and its use as antireflective coating for solar cells and as interference filters for optical devices [33, 34]. It has also been extensively investigated as a dielectric candidate for the DRAM capacitor cell[81, 82] and as gate dielectrics [35] due to its high dielectric property (k=25). Recently, it has gained popularity in the field of resistive switches as well. Ta_2O_5 as well as its sub-oxides that have been investigated show promising results.

Banno et al has analyzed a Cu/Ta_2O_5 device in detail [36] and published many measurements investigating retention time, endurance time and repeatability. The device

is a lot more stable and consistent for AC signals. The devices are made to switch at lower current as required by the ITRS (*International Technology Roadmap for Semiconductors*) [37]. Lowering the current leads to a higher R_{ON} of 800 Ω. However, this is still better than the (1k-2k) resistance of conventional SRAM [38].

Thus far, the switching characteristics of the device seem to be very promising though the actual working principle of the device has yet to be discerned. Sakamoto et al suggested that the conducting filament formed in the solid electrolyte is a discontinuous metal filament.[24] He is proposing that the conduction is not solely due to the metal precipitates alone because the filament is comprised of metal islands in the insulator [25]. The variability in resistance values obtained for each switching cycle is attributed to the lengths of the electrolyte gaps between the metal islands forming the discontinuous metal filament. His hypothesis has yet to explain how the metal ions can be reduced spontaneously in the middle of the solid electrolyte far removed from the inert metal electrode.

A large amount of scientific literature on resistive memory suggests the possibility of more than one mechanism operating in the same materials system. One paper proposes conduction in Ta_2O_5 solid electrolyte due to Cu interstitials and shows that there is less contribution from oxygen vacancies [39], whereas the majority of the literature papers suggest oxygen vacancies or metal diffusion to be responsible for forming the conductive metal filament bridges [40-46] in solid electrolyte systems.

Crossbar switching devices fabricated with Tantalum Pentoxide (Ta_2O_5) and its sub-oxide have been shown to exhibit high switching endurance. Endurance as high as 10^{10} cycles has been reported for TaO_x device with low R_{OFF}/R_{ON} ratio of 15 [47].

Issues Related to Resistive Switches

Most of the researchers in the resistive switches field are more concerned about the non-uniformity in device performance. In the vast literature on resistive switches, it is clearly mentioned that these devices suffer device-to-device as well as cycle-to-cycle non uniformity in switching characteristics [4, 48-60]. The affected device parameters are OFF resistance, ON resistance, switching times, switching voltages and forming voltages. Variability in these parameters is attributed to random filament formation, non-uniform annihilation of filament and current overshoot. Many efforts have been made by researchers to understand the switching mechanism [50] to improve performance. The biggest issue here is the complete lack of a precise understanding of the switching mechanism of these devices.

Switching Mechanisms

Various switching mechanisms of resistive switches have been addressed in the literature. Most commonly discussed are formation mechanisms of the conductive metal filament [22, 38, 61-65] and the aligning of oxygen vacancies [66-69]. Other mechanisms such as redox reactions at the metal and oxide interface [70], conduction due to metal interstitials [39] and thermochemical [71, 72] reactions are also discussed. It has been shown, that in a material system more than one mechanism might be responsible for switching [39]. More often metal ion migration due to electrochemical effects is thought to be the dominant mechanism in materials systems involving oxidizing metals such as Cu and Ag.

Random Filament Formation

It has been shown that the conduction in a two terminal crossbar switching device with solid electrolytes takes place through a localized filament of a few nm in size [73], where the position of the filament is random. Therefore, the variability of the device parameters are attributed to this randomness of filament location [4, 48-60]. This random formation of the conductive path has been well depicted by Guo et al [64]. To minimize the variability in device performance due to random conduction paths several techniques have been considered. Some of these optimization techniques are introducing interfacial layers[28, 74, 75] and doping of the insulating electrolyte layer [44, 48, 55, 76].

Non-uniform Annihilation of Filament

It is not solely the formation of the filament, which is random. However, the annihilation or dissolution of the formed metal filament is equally non-uniform and random. It is very difficult to estimate the exact spot in a conducting filament at which the rupture takes place [38, 49]. There is no guarantee that the filament will break at the same spot for every switching cycle [77]. Based on the experimental data this is highly unlikely. Some of the measurable effects of this non-uniformity are: 1) variation in the off resistance and 2) variation in switching time for the next cycle.

The time of dissolution of the metal filament depends on the diffusivity of the particular electrolyte being used [78, 79]. Therefore, multiple layers of electrolyte with different diffusivity can be used in order to aid localization and to reduce the variability of the metal filament formation and dissolution process. The filament dissolves sooner when the electrolyte has higher diffusivity. Therefore, the point of metal filament dissolution can be controlled by controlling the placing of the electrolyte layer with the higher

diffusivity. Sakamoto et al [77] have shown much better uniformity is achieved by placing the higher diffusivity electrolyte layer closer to the inert electrode. Other techniques that have been explored to improve the uniformity of the process is by switching partially broken filaments [49]. This approach does improve the uniformity of switching and OFF resistance values but at the cost of a lower ON and OFF resistance ratio.

Current Overshoot

It is important to limit the current through the device during SET operation. Otherwise, the high current through the tiny conductive filament may prove to be detrimental to the device. Therefore, a current compliance is applied during SET. Typically, current compliance is achieved using 1T1R (1-Transistor 1- Resistor), 1D1R (1 Diode 1 Resistor), 1R (1 Resistor) RRAM configurations or a conventional parametric analyzer [51, 61, 80, 81]. With a simple parameter analyzer, the current can be limited reasonably well below the set current compliance but still suffers from an initial current overshoot. This detrimental current overshoot occurs during the finite settling time required for the parametric analyzer to achieve the current compliance [81-83]. Even more rudimentary compliance circuits consisting of a diode [51] or single resistor [82, 83] also show current overshoot due to inherent parasitic capacitance. It has been shown that the increased reliability of these devices is linked to better control over the current overshoot during SET process [80, 81, 84]. This high current overshoot during SET is also cited as the primary cause of high RESET current [81].

1.4 Thesis Objective and Overview

Due to its remarkable potential to replace the present memory devices and the high performance switches, a tremendous number of research papers has been published on resistive memories. Despite such effort, resistive memory has not made its way to the production. For production, tighter distribution of device performance and high energy efficiency of device is very crucial. The primary objective of this thesis is therefore to improve the device performance, where the wide distribution of the device performance and high RESET current are the key issues. Wide distribution is attributed to the random filament formation and annihilation as well as the current overshoot during SET. High power consumption due to the high RESET current is attributed to the current overshoot during SET. Given below are some of the key techniques discussed in the thesis that were used to improve and understand the overall device performance:

- A novel structure with minimal size (≈10 nm) close to the size of the conducting filament was fabricated to eliminate the random filament formation. Various novel fabrication techniques were developed to achieve the desired structure.
- To better understand the switching mechanism electrical measurement setup capable of transient measurements during switching was developed, an endurance measurement setup with precise transient measurement along with accurate high resistance measurement was also developed.
    - To obtain better control over the current overshoot an innovative current compliance circuit was developed.

CHAPTER 2

DEVICE FABRICATION

As mentioned in the previous section, large numbers of materials systems have been tested for resistive switches. For this thesis research, the Ta_2O_5 and Cu system are chosen due the promising results mentioned in section 1.3.

The crossbar switch devices for this study have been fabricated in the state-of-the-art "Center for Nano-scale Science and Technology" research facility inside NIST. A number of fabrication tools and fabrication techniques have been used to achieve improved device performance. During fabrication, the individual process steps were kept as simple as possible. A large number of required fabrication techniques and clean room processes did not exist at this facility and had to be developed for this crossbar switch device study. Some newly developed device processes achieved superb outcome whereas others had to be left out due to the process complexities and time constraints. Ample numbers of clean room inspection tools were also used to inspect and to characterize each individual process step during device fabrication, as well during process development.

2.1 Fabrication Tools

Deposition

Sputtering has been used as deposition techniques for most of the films during device fabrication. During sputter deposition many parameters such as substrate bias, chamber pressure, substrate temperature, sputtering energy, gas flow in the chamber etc. can be modulated. These parameters can be changed accordingly to achieve desirable film characteristics [85]. For this reason, sputtering technique was chosen to deposit most of

the films used in the device. The bottom Pt electrode along with the Ta adhesion layer, Ta_2O_5 and the Cu top electrode were all sputtered deposited. E-beam evaporation was used to deposit the Cr hard mask. For excellent conformal step coverage during Si_3N_4 spacer deposition, Plasma Enhanced Chemical Vapor Deposition (PECVD) was used [86]. Si_3N_4 was used as a spacer and insulator that defines the device area.

Etching

Parallel plate diode reactive ion etching (RIE) and inductively coupled plasma (ICP) etching were used to etch Si_3N_4 and the Cr hard mask. RIE is also used to remove resist (Descum). O_2 plasma descum process was used to etch and remove photoresist. RIE is a simple plasma-etching tool where the anisotropy depends on factors like chamber pressure during deposition, power and etching gas. The ICP etcher was used for higher etch rates and anisotropy along with low voltage bias [86].

Patterning

For large structures, photolithography was used (<1 μm). Nano-imprint was considered at one point to obtain small devices <100 nm, but this approach was abandoned due to the complexities in the process. Larger patterns obtained by photolithography were reduced to achieve features below 1 μm using self-aligned spacer techniques.

Photolithography

Photolithography was used to achieve >1 μm resist patterns. The resist patterns were used for either etch or lift off to obtain the thin film patterns. LOR 3A (Lift Off Resist) with positive photoresist S1813 was used for lift off. This is a two-layer lift off process as shown in Figure 5 (http://microlab.berkeley.edu/labmanual/chap1/1.3.html#_ MOD _18).

The top layer is a positive tone photoresist and the bottom layer is a lift off resist that dissolves in the developer. During the developing steps, only the exposed area of the top resist is removed thus making way for the developer to get to the bottom LOR layer. This creates an undercut below the upper resist pattern. When a thin layer is deposited on the pattern, it is not continuous due to the discontinuous bi-layer pattern. These voids provide a path for the resist removal to lift off the resist and to achieve a clean pattern (Figure 5). Since a discontinuous film is expected for clean lift off, it should be noted that the thickness of the metal to be lifted off should not exceed 70% of the thickness of the bottom LOR 3A resist. In order to obtain a clean pattern with a thickness of 200 nm, the LOR resist thickness should be above 300 nm. The LOR 3A resist is therefore spun on the substrate at 3000 rpm to achieve the thickness of about 300 nm.

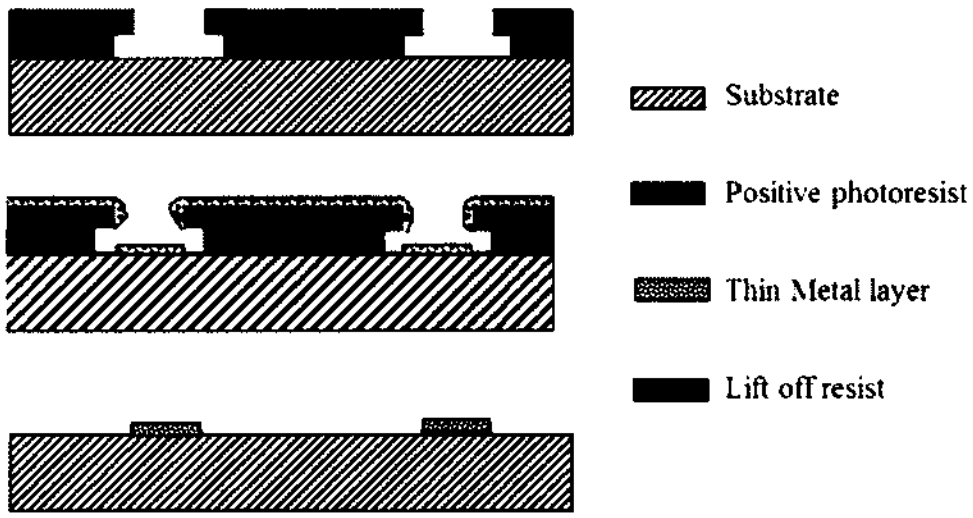


Figure 5. Formation of voids during deposition of thin film makes it easy for the photoresist remover to get into the thin film for clean lift off.

Nano-imprint

Nano-imprint was explored to achieve smaller devices. Nano imprint is a lithography technique capable of patterning nano-structures with sizes comparable to 25 nm with 70 nm pitch on a large area with low cost and high throughput [87]. A mold with specifically designed nano-structures is used to imprint these structures on to the resist. This is accomplished by heating the resist to its glass transition temperature during imprint. The resist becomes much less viscous causing it to easily take the form of the mold. A simple schematic of a nano-imprint process flow is depicted in Figure 6 a). Formation of such a structure is shown in Figure 6 b). It can be seen from the image that there is a residual resist of 120 nm left in the compressed area.

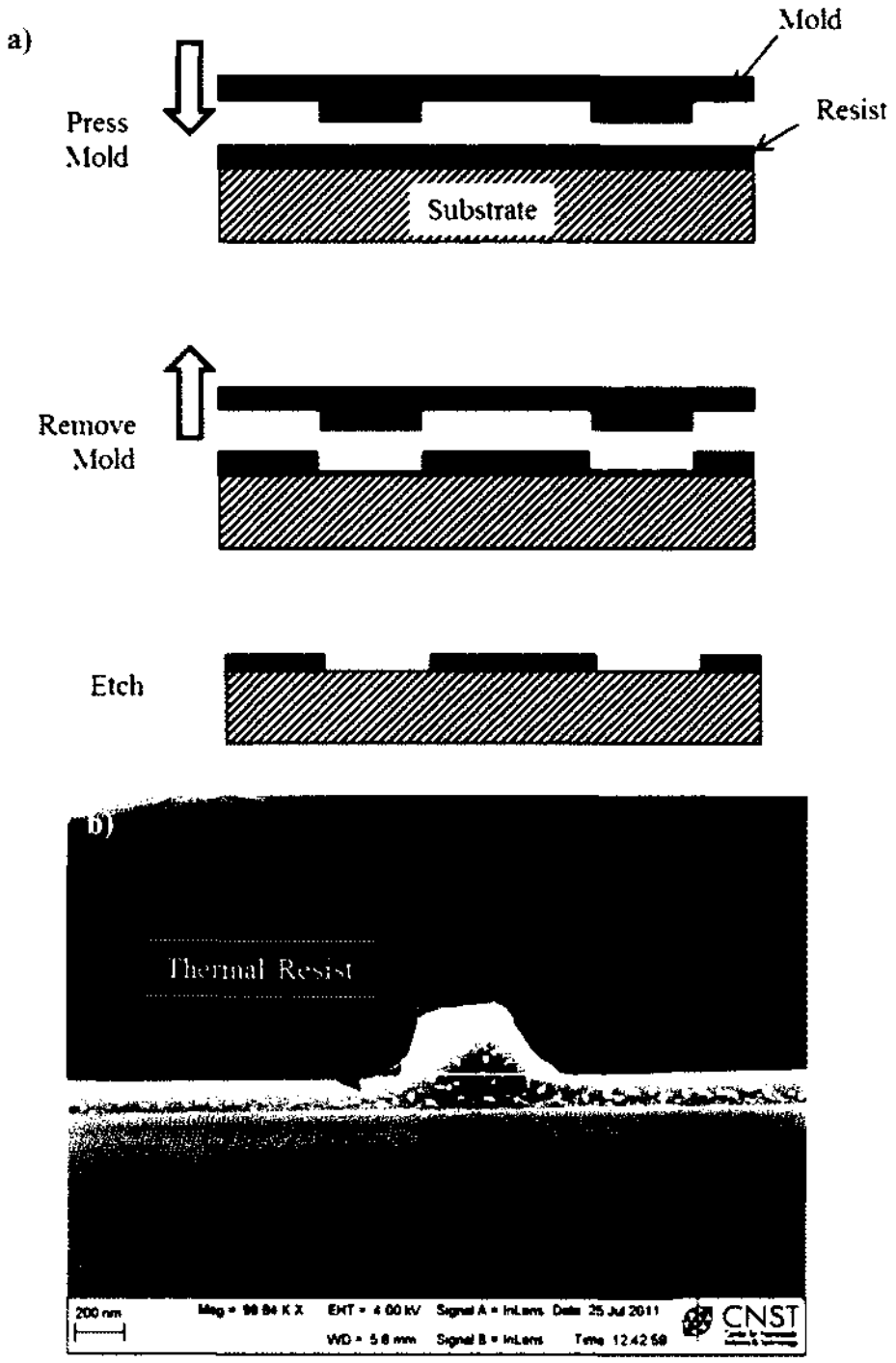


Figure 6. a) Integrated Nanoimprint process flow [88] and b) SEM image of formation of nano-structure after nano imprint.

RIE Oxygen plasma (O_2) ashing was used to remove this residual resist. The details of the RIE etch recipe and the outcome of the resist etching are shown in Figure 7. The power used for the plasma ashing etching process was optimized to achieve good anisotropy, as well as to avoid any energy transfer to the resist. The energy transfer leads to heating of the resist, which needs to be avoided in order to prevent resist deformation. The resist used for nano-imprint technology is heat sensitive and, therefore, has a tendency to deform at higher temperatures.

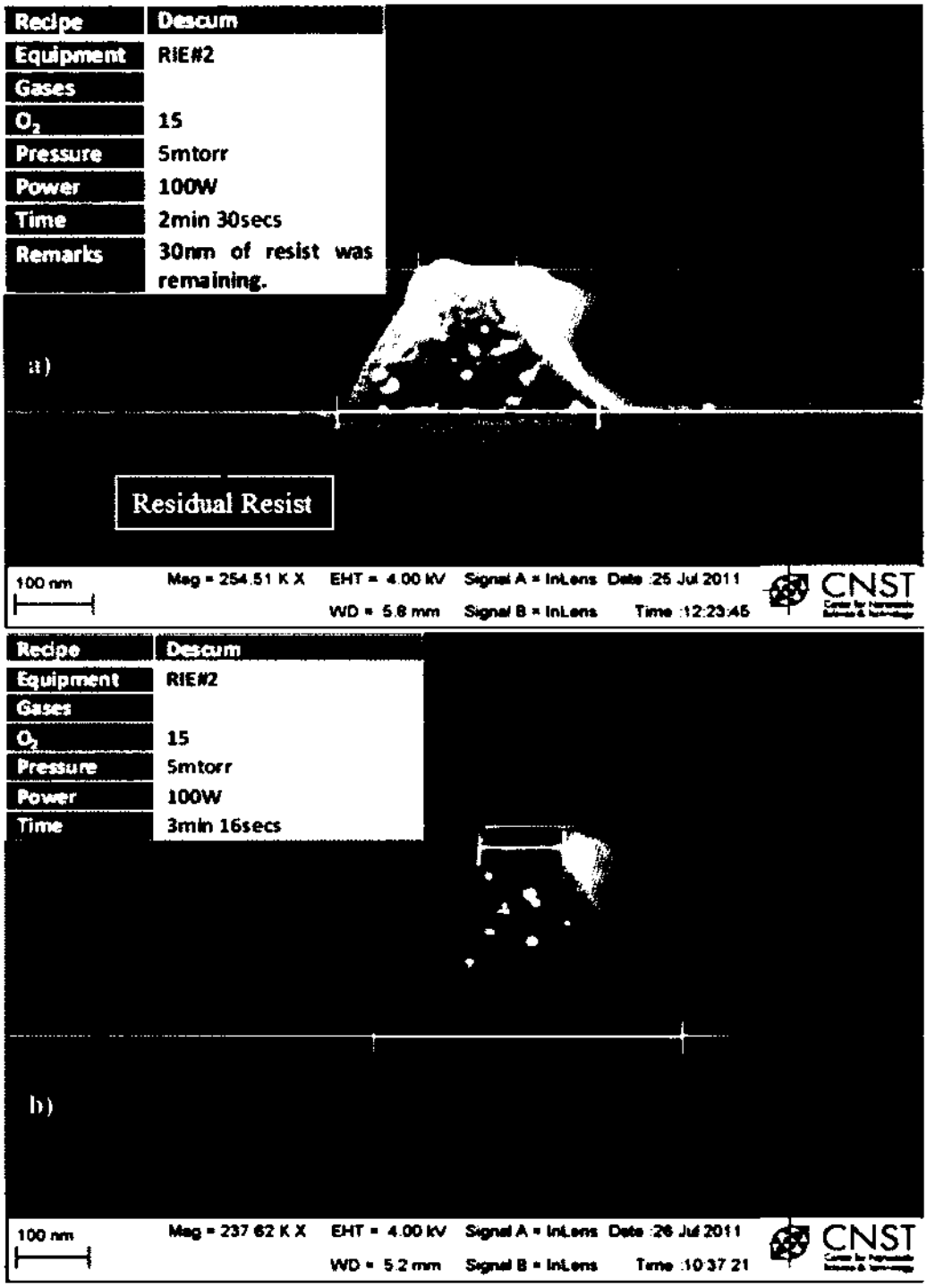


Figure 7. Oxygen plasma RIE recipes used to remove the residual resist from the pattern SEM images a) with and b) without residual resist .

Mold Preparation

Due to the unavailability of a nano-imprint mold with nano-holes at NIST, a nano-imprint mold with nano-pillars was fabricated. Silicon was used as the mold material.

Si Etching

Si etching with good anisotropic profile is required for mold preparation. Fluorine chemistry was first attempted using RIE. Based on Gogolides et al [89], SF_6 and CHF_3 chemistry was used. A gas ratio of 50:50 and 80 W, 160 W and 200 W powers was used to test the recipe. The details of the etch process are given in Table 1(Appendix). The etch profile obtained at each power setting is shown in Figure 8. It can be clearly seen that the 160 W and 200 W etch recipe achieves a better profile compared to the 80 W etch recipe. The DC bias increases with the power, which gives rise to more energetic ions normal to the DC bias. Therefore, these energetic ions provide the horizontal surface with significantly more energy compared to the vertical sidewalls. Therefore, the recipe with higher power shows better anisotropy. The 200 W etch recipe was chosen for the best etch profile.

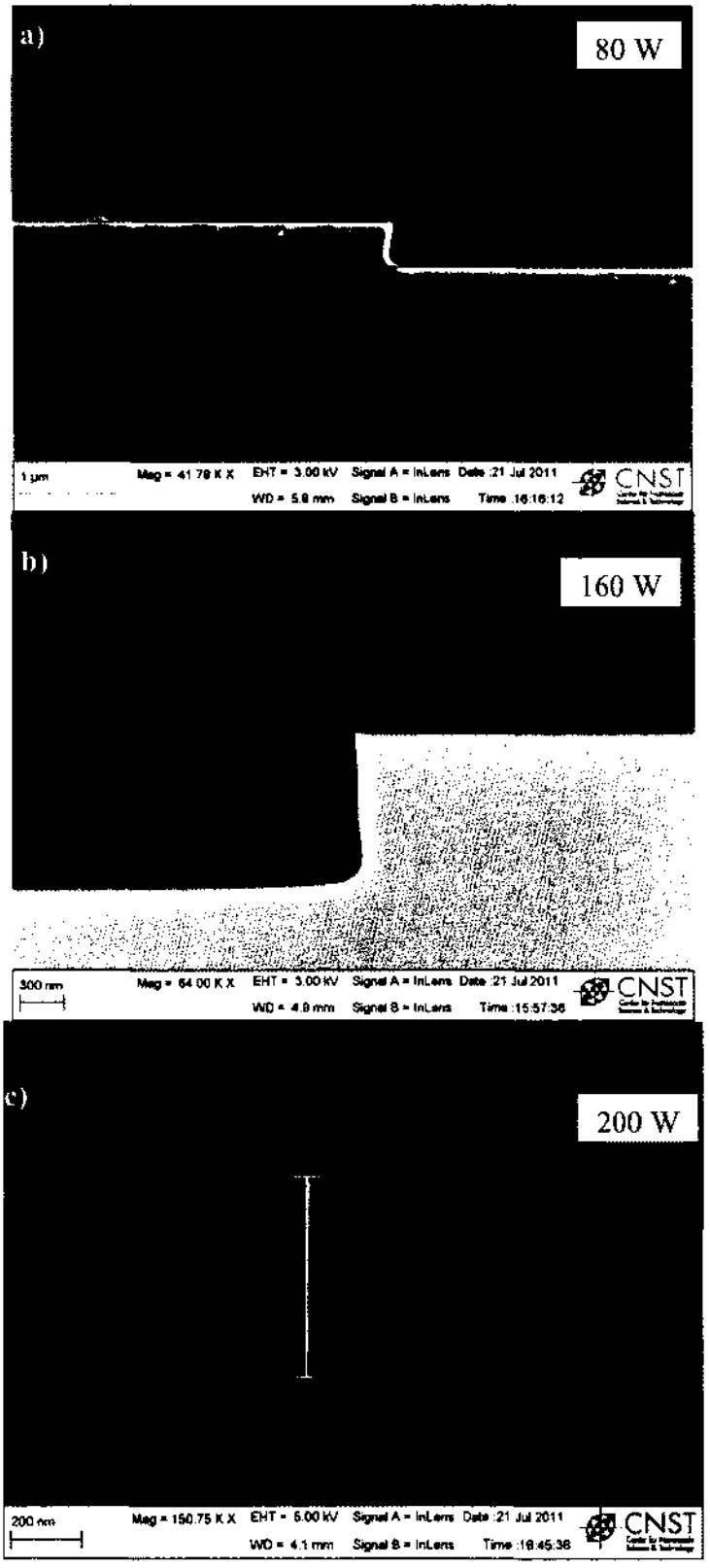


Figure 8. Cross-sectional SEM micrographs showing RIE Etch profile as a function of varying RIE power.

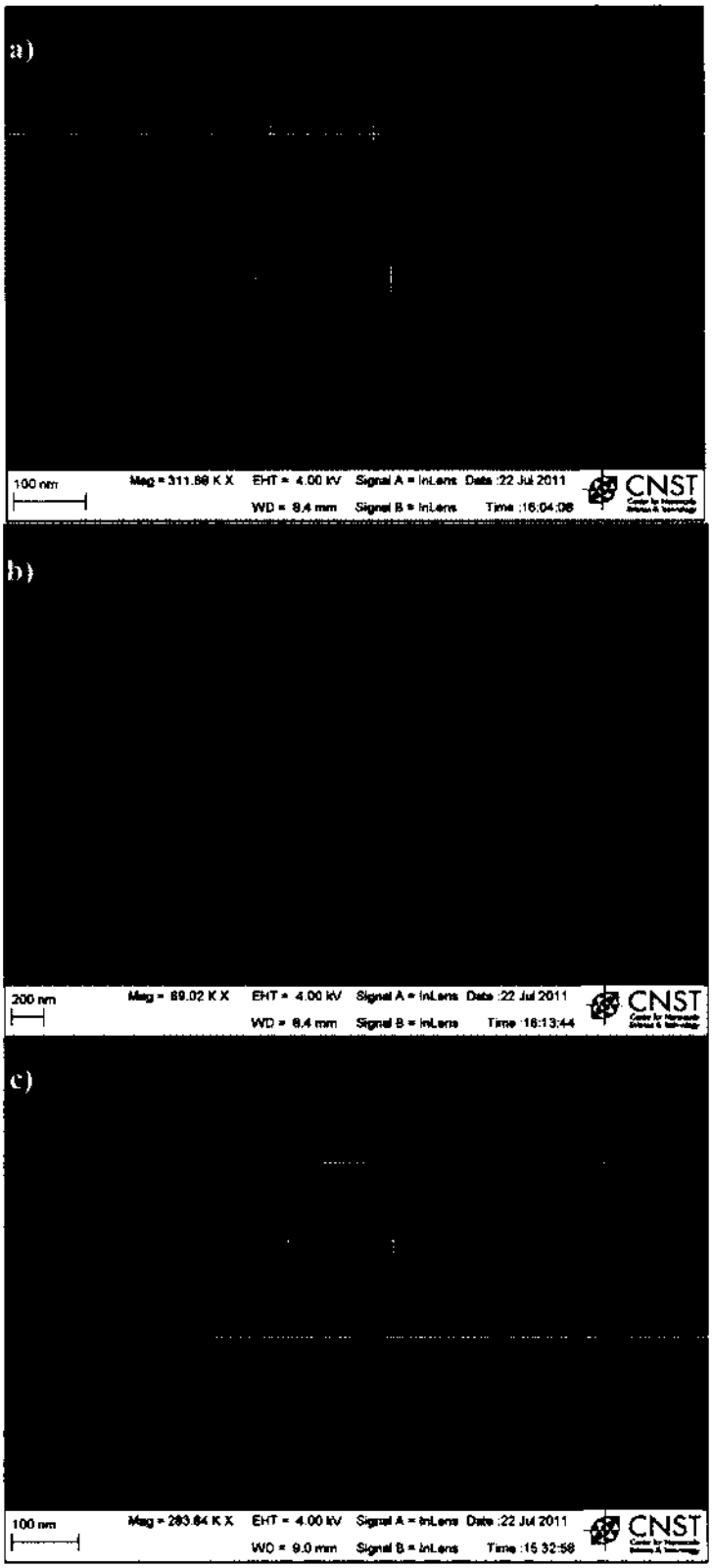


Figure 9. SEM micrograph showing Fabrication of Si nano-wires using 200 W power for Si etch recipe.

Patterns obtained following the etching process are shown in Figure 9. The nano-pillars using the imprints are vertical. The nano-pillars are tapered at the top and have a wide foot as demonstrated in Figure 9. In addition, the heights of the nano-pillars are not the same for pillars with dissimilar diameters. The shape of the resist causes this. From previous sections (Figure 7), it is clear that the shape of the resist mask is trapezoidal. The angle of the trapezoid depends on the size of the structure. The slope is much steeper for smaller structures (Figure 10) causing the smaller nano-structure to be eroded sooner by RIE processing.

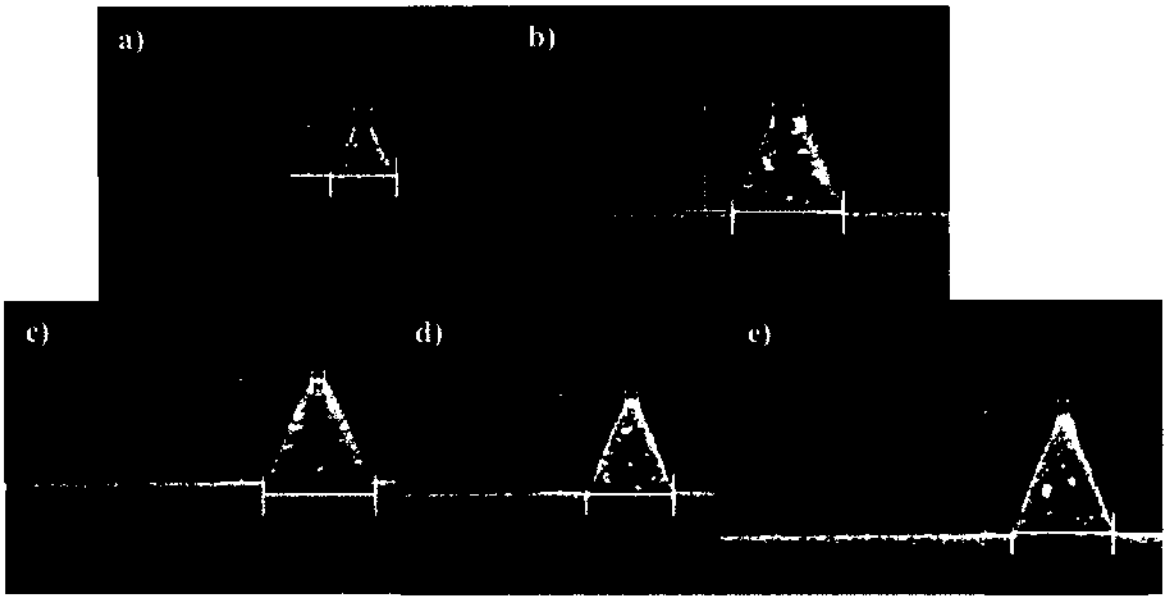


Figure 10. Cross-sectional SEM micrographs of resist patterns obtained from nano-imprint technology. The size of each thermal resist structure is different. The size is decreasing from a) to e).

In order to limit the dependence of the etched Si pattern on the resist mask it was necessary to improve the selectivity of Si to resist. To improve the selectivity of Si over resist, the lower power of 80 W was used to etch Si. The result of the Si etching with

lower power is shown in Figure 11. The SEM cross-sectional results suggest that the chosen etch recipe is not as anisotropic as expected. Therefore, the idea of decreasing the power was abandoned in favor of a hard mask.

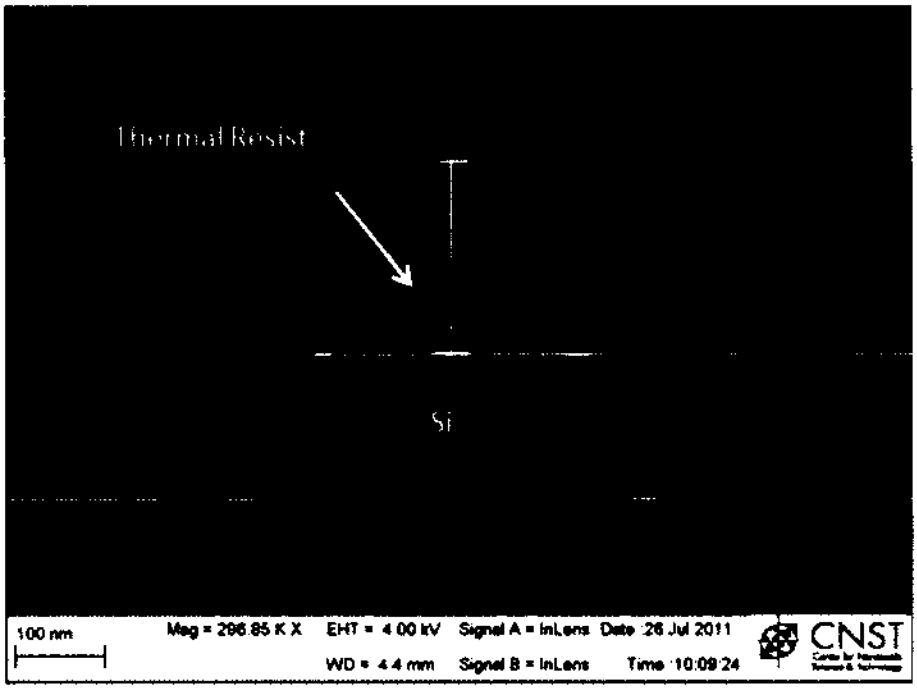


Figure 11. SEM cross-sectional micrograph highlighting the result of Si etching using 80 W lower RIE power.

PECVD SiO_2 was explored as hard mask. The details of the recipe used for deposition and etching along with the final outcome are shown in Figure 12.

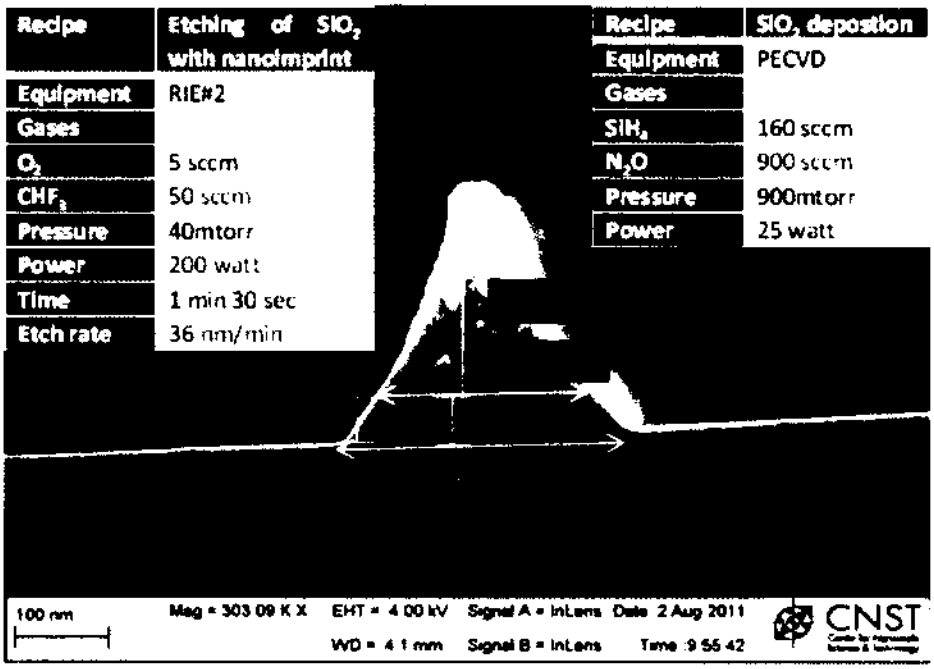


Figure 12. SEM cross-section delineating the result of SiO_2 etching using a nano-imprint resist mask with details of etching and deposition recipes.

Since the selectivity of the PECVD SiO_2 hard mask with the resist was unsatisfactory and the resist profile was not vertical, the underlying etch profile was getting worse. For the above case Figure 12, 50 nm of SiO_2 hard mask was used. Complete etching of the 50 nm thick oxide hard mask was leading to 50 nm of horizontal over cut. To reduce the over cut, the thickness of the SiO_2 hard mask had to be reduced. For the case of such a thin PECVD SiO_2 hard mask, a recipe with very high selectivity between Si and SiO_2 was required.

Because of time constraints and the unforeseen process complexities involved in making the mold and anticipating further difficulties during the nano-via formation, a decision was reached not to pursue nano-imprint technology further for this study. Critical process complexities identified while using nano-imprint technology are:

- Thermal resist is very vulnerable to heat. Therefore, extra care has to be taken while using it as a mask to etch the layer below it.
- The thickness of the thermal resist is very thin, in the order of 100 nm. This renders it highly questionable to use as mask for various layers that need to be etched. To achieve better etch depth selectivity with the same resist thickness; a hard mask has to be used instead.
- Mask alignment is not possible for nano-imprint. Therefore, the layer that needs the nano-imprint technique has to be the first layer for the device fabrication. In our device configuration, this will not be practical for further processing.

Inspection

Profilometer, ellipsometer and reflectometer were used to accurately determine the thickness of thin films utilized for device processing. For metals and material whose composition is not definite, a profilometer was used. For thin films deposited on various stacks of layers, SEM (Scanning Electron Microscopy) was used to measure the film thickness.

SEM microscopy was also used to carefully characterize all the processing steps during device fabrication. Test and Control samples undergoing the same fabrication process as the actual device were imaged by SEM in order to inspect all critical process steps. The test and control samples were cleaved for SEM cross-sectional imaging. The control samples were patterned with dense holes and lines as depicted in Figure 13. The dense lines will surely be cleaved revealing the structure of layers that have been deposited and RIE etched. The cross-section of the line provides a measure about the structure that is being formed but may not give the exact picture the device fabrication. The actual device

structure might be different from the test structure being formed on a circular structure, which is similar to the device structure. The dense dots were included in the control samples. The spacing of the dots is such that there is a high probability of cleaving through one of the dots.

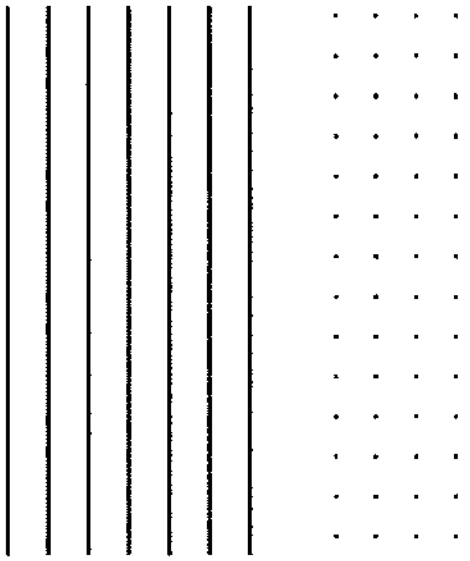


Figure 13. Dense lines and dots patterned as test structures for SEM inspection of spacer technique.

To check the final actual device structure of a complete device, one of the crossbar switch devices was milled using Focused Ion Beam (FIB) to reveal the cross-section. The cross-section of the completed device was then imaged and characterized using high-resolution SEM microscopy.

2.2 Fabrication of Devices Larger than >1 μm Diameter

A schematic layout of the array of device structures designed and fabricated is shown in Figure 14. The array consists of a crossbar structure where the active switching devices

are located at the cross points of the intersection of the top and bottom metal line electrodes. Each individual switching device in the array can be probed via metal pads of 100 μm x 100 μm at the ends of each crossbar. The bottom Pt layer was first patterned by lift off technique. Next, the blanket insulator of Si_3N_4 was patterned over the bottom electrode as in Figure 14. Holes were etched on the blanket Si_3N_4 layer at the point where the crossbars will intersect. These define the active device area. This allows the size of the active area to be independent of the top and bottom electrode. Subsequently, the Ta_2O_5 electrolyte layer and the top Cu electrode were deposited to form the completed device as shown (Figure 14).

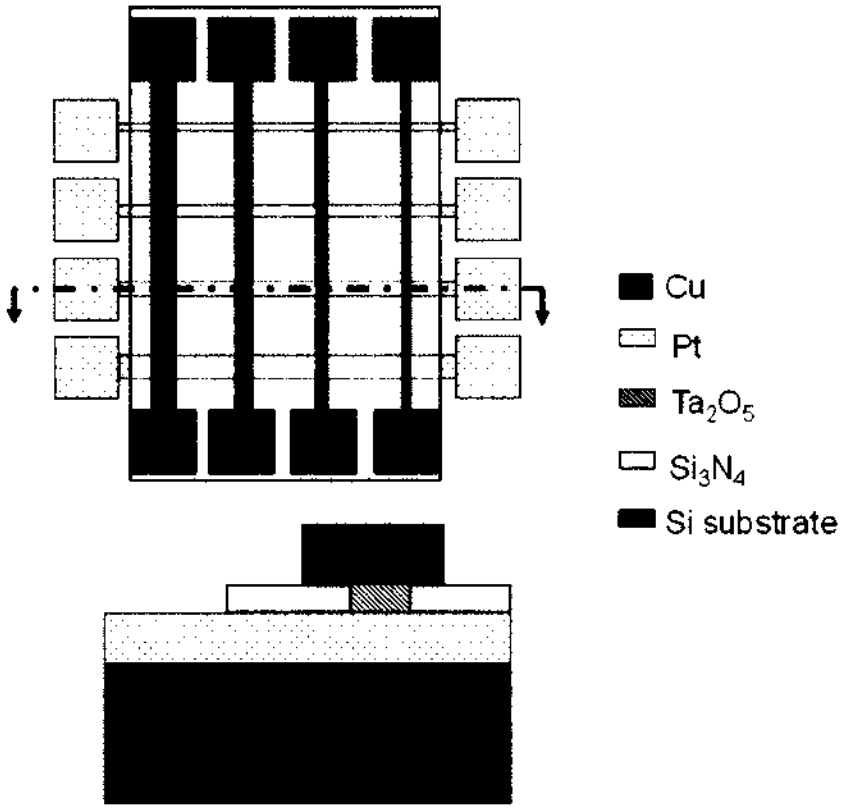


Figure 14. Schematic layout of the final array containing different and varying device sizes using the catalogue mask in Figure 15.

Mask design

The mask was designed with four patterns for four layers. The first layer is the bottom inert Pt electrode, the second layer is the blanket oxide, the third layer contains the solid electrolyte via points and the last layer is for the top Cu electrode. All these layers are designed in the same mask using the catalog mask layout shown in Figure 15. The sizes of the metal electrode lines vary from 1 μm to 30 μm. The via points are of sizes ranging from 1μm x1μm to 20μm x 20μm. There are at least 100 sets of each device after the complete fabrication. For reliability testing, the mask was specifically designed to fabricate a large number of devices in a single processing run. According to the experimental requirement, certain layers can be skipped. For example Layer 3: Via can be skipped completely. In this case, the solid electrolyte can be used as the blanket oxide. The difference here is the device's size, which will be limited by the top and bottom metal electrode line size. Devices smaller than 5 μm x 5 μm will be very difficult to test due to high electrode resistance.

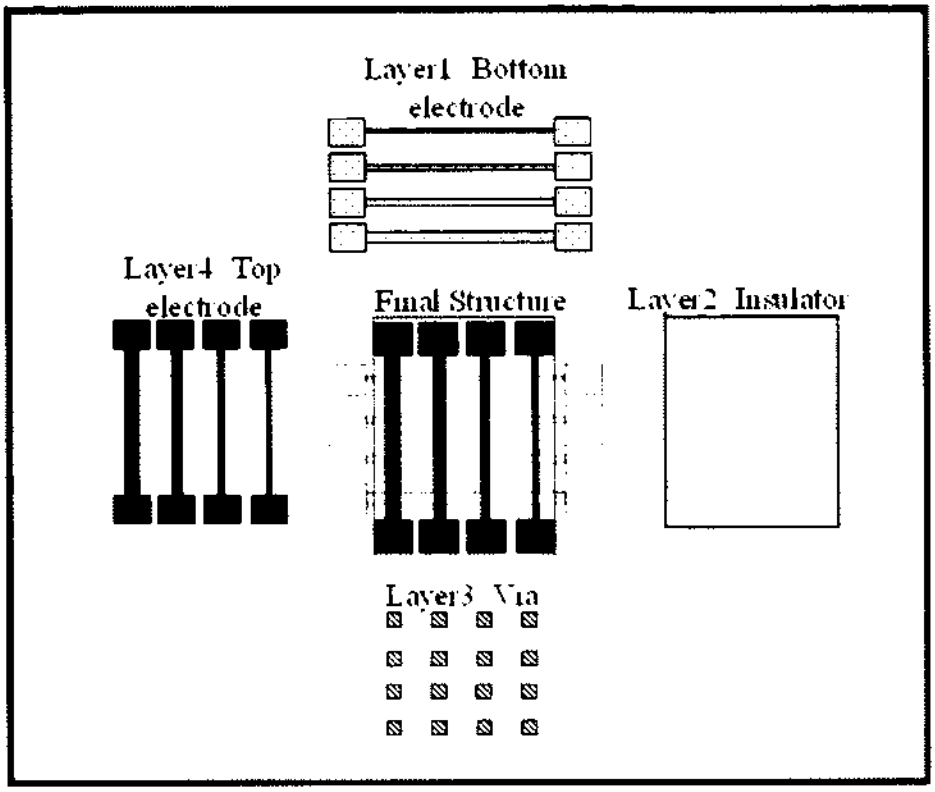


Figure 15. Catalog mask layout used to accommodate four layers in single mask for a device array.

Fabrication Procedures

Platinum Deposition

Platinum (Pt) was sputtered to serve as the bottom electrode. Since the adhesion of Pt to either Si or SiO2 is very poor [90] approximately 40 nm of Ta was deposited prior to Pt deposition given in Table 6 as an adhesion layer. Finally, 150 nm of Pt was deposited with the experimental conditions listed in Table 7.

Tantalum Pentoxide (Ta_2O_5) Deposition

Ta_2O_5 was also sputtered using a commercial Ta_2O_5 target. The thickness of the Ta_2O_5 electrolyte layer is 16 nm. The experimental details of the Ta_2O_5 sputter deposition are given in Table 8. The stoichiometry test for the Ta_2O_5 was not accomplished, but according to the literature, the sputtered Tantalum Pentoxide films are oxygen deficient [91, 92].

Copper (Cu) Deposition

In this study, Cu was always patterned as the top electrode for all switching devices. This process flow was designed to avoid the use of developer (MF-319) with Cu, because Cu reacts with this developer. Initially, the Cu metal electrode was deposited with a very low deposition rate of 1.8 Å/sec. However, the Cu films deposited under these slow growth conditions oxidized very fast indicating poor quality. Realizing this deposition rate of Cu was then increased almost ten times to 16 Å/s to reduce oxygen incorporation during Cu deposition. This change in the deposition rate improved the quality of the Cu film but resulted in poor adhesion to the underlying Ta_2O_5 electrolyte layer. In order to improve the adhesion substrate, RF bias was then added during deposition [85]. The optimum recipe for a decent quality Cu metal electrode with good adhesion is given in Table 11.

Silicon Nitride (Si_3N_4) Deposition and Etching

PECVD Si_3N_4 was deposited as the insulator that defines the device area as depicted in Figure 14. The recipe for PECVD Si_3N_4 deposition is given in Table 14. The recipe given in Table 3 was used to anisotropically etch the Si_3N_4 in an RIE tool. Anisotropic etching is desirable to replicate the via size in the mask.

Sample A

The schematic layout of sample A is shown in Figure 16 (a). The array structure is obtained by using Layer 1, Layer 2 and Layer 4 shown in Figure 15. Layer 1 was used to pattern the bottom Pt inert electrode on a Si substrate. The bottom electrode was obtained by lifting off 120 nm of sputtered Pt. The deposition rate of the Pt was about 1.7 Å/sec. A Ta layer of 20 nm was used for better Pt adhesion. Microposit 1165 was used to lift off Pt at a temperature of 78 °C. Layer 2 was used to pattern the Ta_2O_5 solid electrolyte layer. The Ta_2O_5 layer was sputtered with 300-watt RF sputter power at 5 mTorr with 50 sccm of Ar flow. The deposition rate was 1 Å/sec and the targeted Ta_2O_5 thickness used was 16 nm. Micoposit remover 1165 was used to lift off the Ta_2O_5 at a temperature of 78 °C. Layer 4 was used for the top Cu metal electrode. The 150 nm of Cu was sputtered at a rate of 1.8 Å/Sec. Microposit 1165 was used at room temperature to lift off Cu.

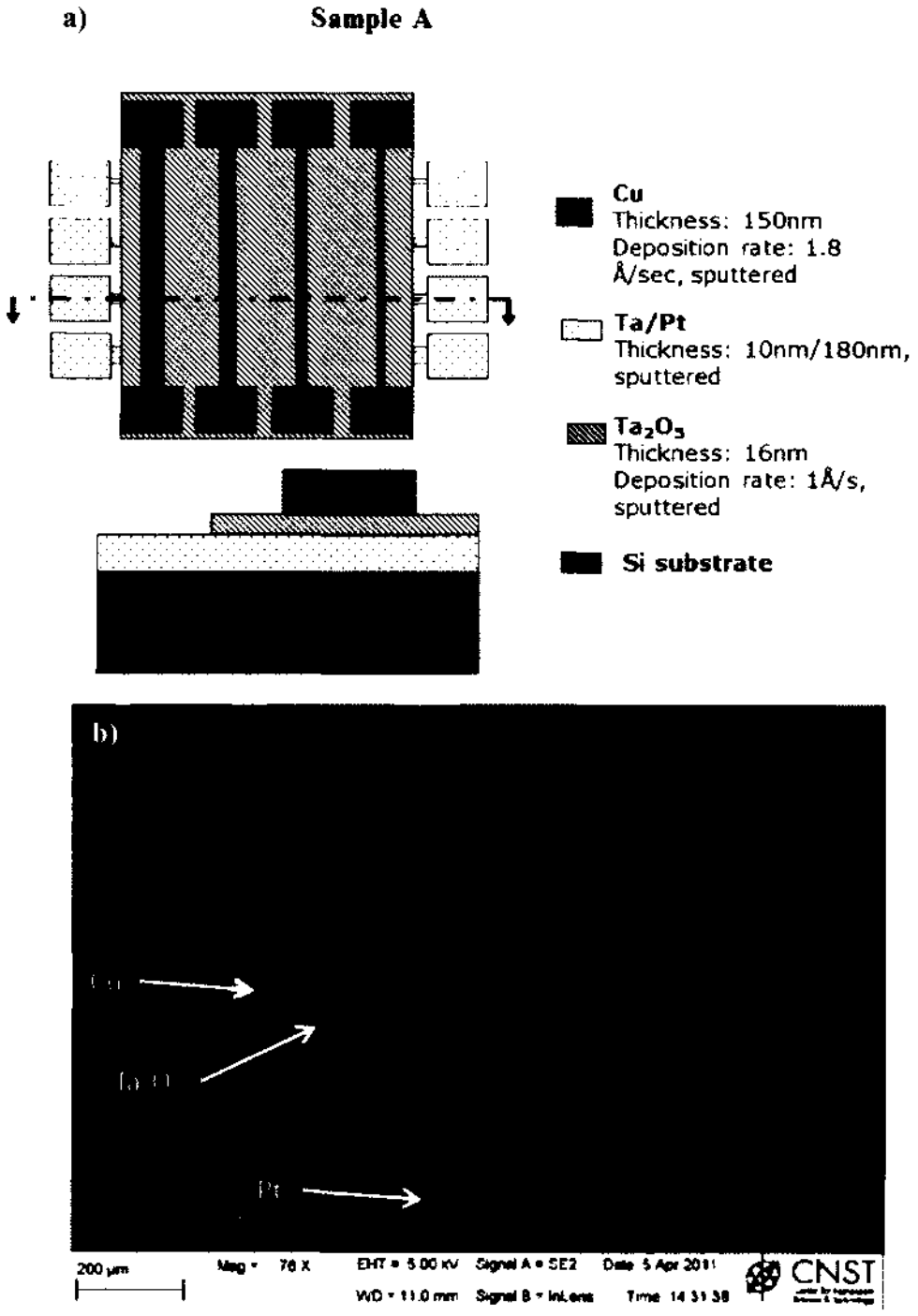


Figure 16. a) Schematic layout of sample A and b) SEM micrograph of the fully processed and completed device array of sample A.

2.3 Fabrication of $Pt/Ta_2O_5/Cu$ Device with Localized Cu-ion Implantation

Non-volatile resistive memories have gained much popularity in the past few years due to their simple structure, low cost and high scalability [50]. Despite all of these advantages, these devices still suffer from poor distribution of R_{ON} and R_{OFF} and controllability. This poor controllability and distribution is attributed to the random formation of the metal filament that provides a conductive path through the solid electrolyte in the devices. Significant research has been performed to improve the distribution and controllability of the metal filament [92]. There are a few groups that have been able to show tighter R_{ON} and R_{OFF} distribution by selective doping of the solid electrolyte layer in the MIM structure [48, 55]. The doping process, in these cases, has been accomplished either by diffusion doping or by blanket ion implantation. Better control of the formation and rupture (dissolution) of the conductive path around the dopants is suggested to be the reason for improvement of the distribution. This suggests that the distribution of the R_{ON} and R_{OFF} can be improved by controlling the path and the location at which the formation and the rupture of the conductive filament takes place. To further improve the control of the conductive paths, the doped region should be as close to the site of a single filament as possible. The best way to achieve such a structure for a $Pt/Ta_2O_5/Cu$ device stack is by implanting Cu ions a few nm deep into Ta_2O_5 solid electrolyte keeping the area of the implant closer to the filament site.

To implant the Cu ions into selected extremely small areas, a pattern that opens such a small hole for the Cu ion implantation and will mask the reminder of the Ta_2O_5 has to be designed and fabricated. A schematic of such a structure is shown in Figure 17 a). Once the Cu ion implantation has been completed, the masking layer can be removed to deposit

Cu top electrode. Although the Cu top electrode area is large, the active device area, where the filament formation and switching takes place, is solely determined by the area of the Cu ion implantion as illustrated schematically in Figure 17 b).

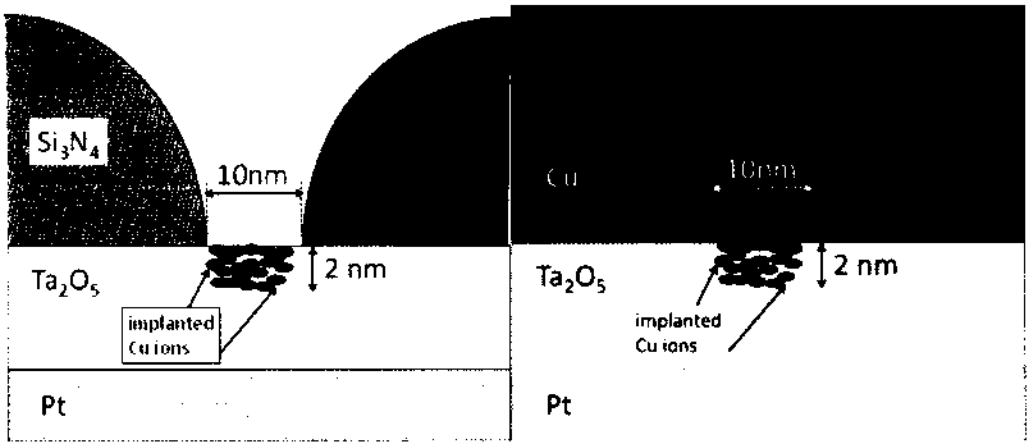


Figure 17. a) Desired structure for Cu ion implantation and b) complete device after the removal of the Si_3N_4 and top Cu deposition.

For this device, the Cu ion has to be implanted with an implant energy as low as possible, in order not to damage the underlying Ta_2O_5 solid electrolyte with implant damage. The Cu ions should be implanted just 2 nm into the thin Ta_2O_5 solid electrolyte layer of 16 nm thickness. The cost of such a metal ion implant is very high due to the low dose and low energy requirements. Along with the high cost issue, significantly more processing time and developing effort would be required in order to achieve the structure shown in Figure 17 a). Particularly the requirement to achieve the absolutely smallest implant openings aim for 10 nm diameter brings this task to the cutting edge of technically feasible possibilities with today's cleanroom technology. Therefore, the Cu ion implantation approach was abandoned for this dissertation study. Instead, an alternative strategy was pursued to achieve the same objective by reducing the size of the device to the size of a single filament.

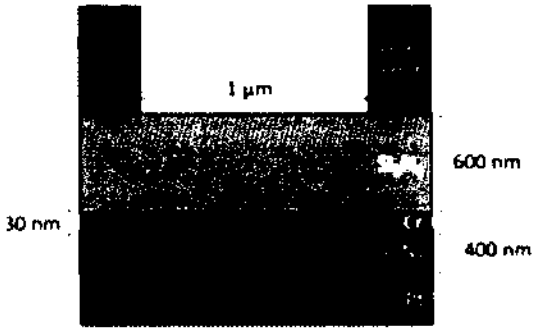
2.4 Fabrication of Devices with Less than <100 nm Diameter

Resistive switches with solid electrolytes suffer from poor distribution of R_{ON} and R_{OFF} and controllability attributed to the random formation of the conductive filament in the devices. Beck et al showed that the distribution of R_{ON} and R_{OFF} improves with the decreasing size of the active area [4]. This is attributed to fewer random dendritic conductive metal filaments in a smaller area. The size of such metal filaments formed has been shown to be only a few tens of nm [93]. In order to achieve the maximum possible tighter distribution of R_{ON} and R_{OFF}, a strategy to reduce the active device area to the size of a single filament would be ideal. For this reason, the targeted active area of the device was shrunk to 10 nm x 10 nm. Such a device area reduction will trigger filament formation in that particular point and prevent random formation of the dendritic metal filaments in other parts of the device due to deliberate space limitations.

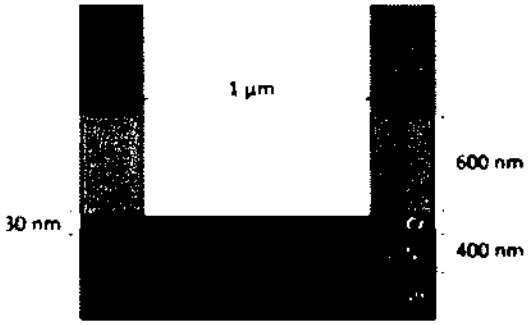
The similar mask shown in Figure 15 was used to fabricate devices with less than <100 nm size. The difference in this case is that the size of the via is either 1 μm x 1 μm or 2 μm x 2 μm, in stark contrast to the previous mask, where the much larger via sizes ranged from 1 μm x 1μm to 20 μm x 20 μm . In order to achieve much smaller active device areas, the vias formed in Layer 3 were further reduced in size using the specific spacer techniques discussed in the following section. A double spacer technique was first explored. This technique can be used to fabricate devices in the range of 100 nm. However, this technique is very difficult to control when aiming to achieve device structures below that size. Since the target size of the shrink device was 10 nm, a multiple spacer technique was used to shrink the size of the via with better dimensional control.

Double Spacer Technique

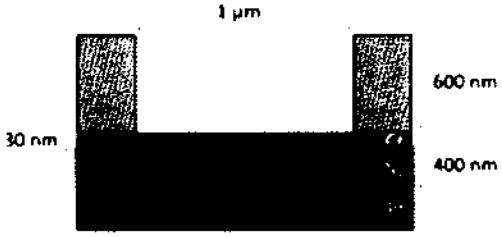
Initially, the first layer for the double spacer technique was patterned using a contact aligner. Then the double spacer layers were all self-aligned. PECVD Si_3N_4 was used for a spacer. The smallest size achieved by the contact alignment was approximately ≈1 μm. This size was then reduced to less than 500 nm by using the first spacer. The first spacer was used to create a via of 500 nm or less. These vias were created by using Chromium as the hard mask. The complete integrated process flow of the double spacer technique developed for this crossbar switch device study is shown in Figure 18.



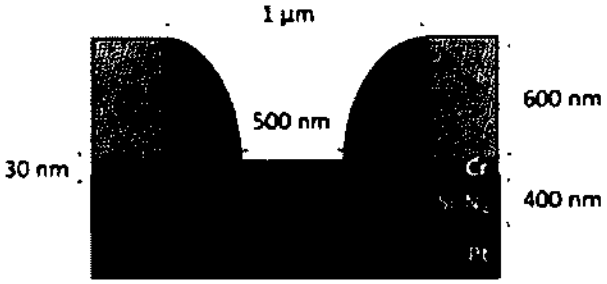
a) Patterning using photolithography



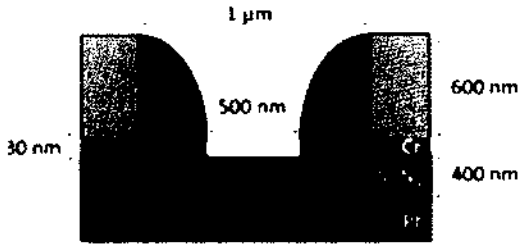
b) Anisotropic etching of Si_3N_4



c) Removal of photo resist

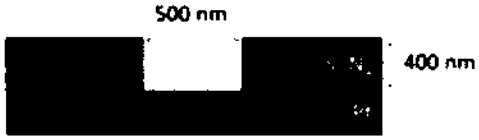


d) Formation of first spacer

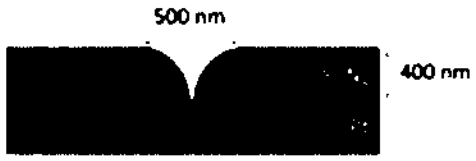


e) Cr anisotropic etching of Cr hard mask

f) Anisotropic etching of bottom layer with reduces size



g) Removal of Cr layer



h) Formation of second spacer

Figure 18. Integrated Process flow developed for the double spacer process.

Si_3N_4 Deposition

Si_3N_4 was used as spacer material. Si_3N_4 was also used as the insulator between the top and bottom electrode because it forms a good diffusion barrier and exhibits excellent resistance to Cu diffusion. The spacer material has to be extremely conformal to achieve the desirable output. Therefore, the Plasma Enhanced Chemical Vapor Deposition (PECVD) technique was chosen to deposit spacers. During PECVD processing, the adsorbed material on the substrate are energetic species. This leads to three important aspects during PECVD deposition. The first is that these energetic species, which are primarily radicals, tend to stick to the substrate more easily due to their high reactivity. The second is the energy with which the species are adsorbed is high in the case of the PECVD. This allows the species to move around easily and rearrange laterally on the sample surface. The third is that the adsorbed film is continuously being subjected to high-energy ion bombardment. All of these aspects are key to uniform and conformal coating. The resulting conformal coating of Si_3N_4 in a trench using the newly developed recipe listed in Table 11 is shown in Figure 19.

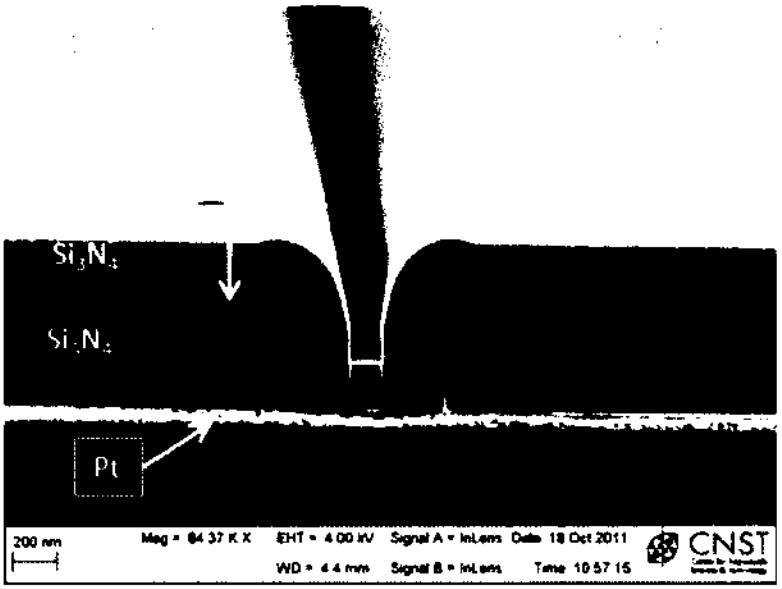


Figure 19. Cross-sectional SEM micrograph providing proof of conformal coating of Si_3N_4 using PECVD technique.

Dry Etching of Si_3N_4

Dry etching can be isotropic as well as anisotropic. During the fabrication of the crossbar switching devices, anisotropy is important. Therefore, dry etching recipes with extremely anistropic etching were explored. Anisotropy in dry plasma etching is achieved in the presence of either one or both of the following techniques [94],

- High energy ion bombardment

  The high-energy ions attracted to the substrate hit horizontal substrate surface normally. The energy of the ion hitting the substrate surface normally is much higher than the ions hitting the vertical sidewall, which leads to anisotropic etching.

- Polymer formation on the vertical side wall

  During RIE etching, polymers form in the chamber by design due to the chemical reaction of the etching gasses. If formed in significant amounts, these polymers

reaction by-products will coat all substrate surfaces evenly. Since the horizontal part of the surface is bombarded with high-energy ions, these polymer reaction by-products were easily and completely removed from the horizontal substrate surfaces. In contrast, the vertical sidewalls of the device pattern are not susceptible to these high-energy ions during etching. Consequently, there is a significant build-up of these polymers on the vertical sidewalls of the patterned device structure. This polymer build-up on the vertical walls acts as a hard mask and protects the vertical side walls from etch attack, thus ensuring anisotropic etch attack

Usually both of these methods are employed to achieve high anisotropy.

Micro-masking Effects during Anisotropic Etching of the Si_3N_4 Spacer Material

For the formation of a good spacer, perfect anistropic etching is required. A conformal deposition will provide a structure as shown in Figure 20 a). Following an anisotropic etch step of the deposited Si_3N_4 film, the final spacer structure should look like Figure 20 b).

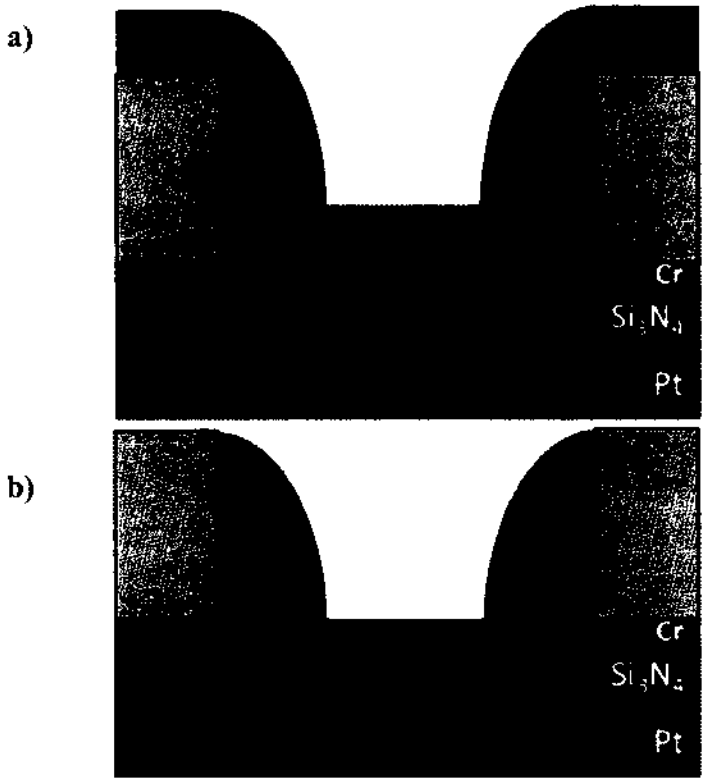


Figure 20. a) Schematic representation of Si_3N_4 spacer formation before and b) after anisotropic etching.

The details of the etch recipe used for the Anisotropic RIE etching of the Si_3N_4 spacer structure is provided in Table 3. The resulting cross-sectional profile of the Si_3N_4 is anisotropic and clean until it etches all the way up to the underlying Cr layer. The experimental challenge with this recipe is that the DC bias is above 400 V because this is the sputtering voltage for Cr. Once the underlying Cr is exposed at the conclusion of the Si_3N_4 spacer etch, the bias with voltage above 400 V will sputter Cr off. These sputtered Cr metal particles land on the surface of the material being etched. Due to the high etch selectivity between the Si_3N_4 and Cr and high anisotropy these Cr particles will micro-mask the underlying Si_3N_4 forming nano-grass [95]. An example of the SEM micrograph

is shown in Figure 21 (b). In order to avoid the micro-masking effect due to the sputtering residue of Cr, an ICP etcher was used. The advantage of using an ICP etcher is that the average ion bombarding energy is independent of the ion flux. Thus, the ion bombardment energy can be lowered independently to avoid sputtering erosion of the bottom Cr layer without compromising the anisotropy and the etch rate of the Si_3N_4 spacer structure [96]. The final optimized result of the Si_3N_4 spacer etching process using the ICP etcher is documented in Figure 21 (c). The problem caused by micro-masking effect has been resolved by changing the etching from the RIE to the ICP etch tool.

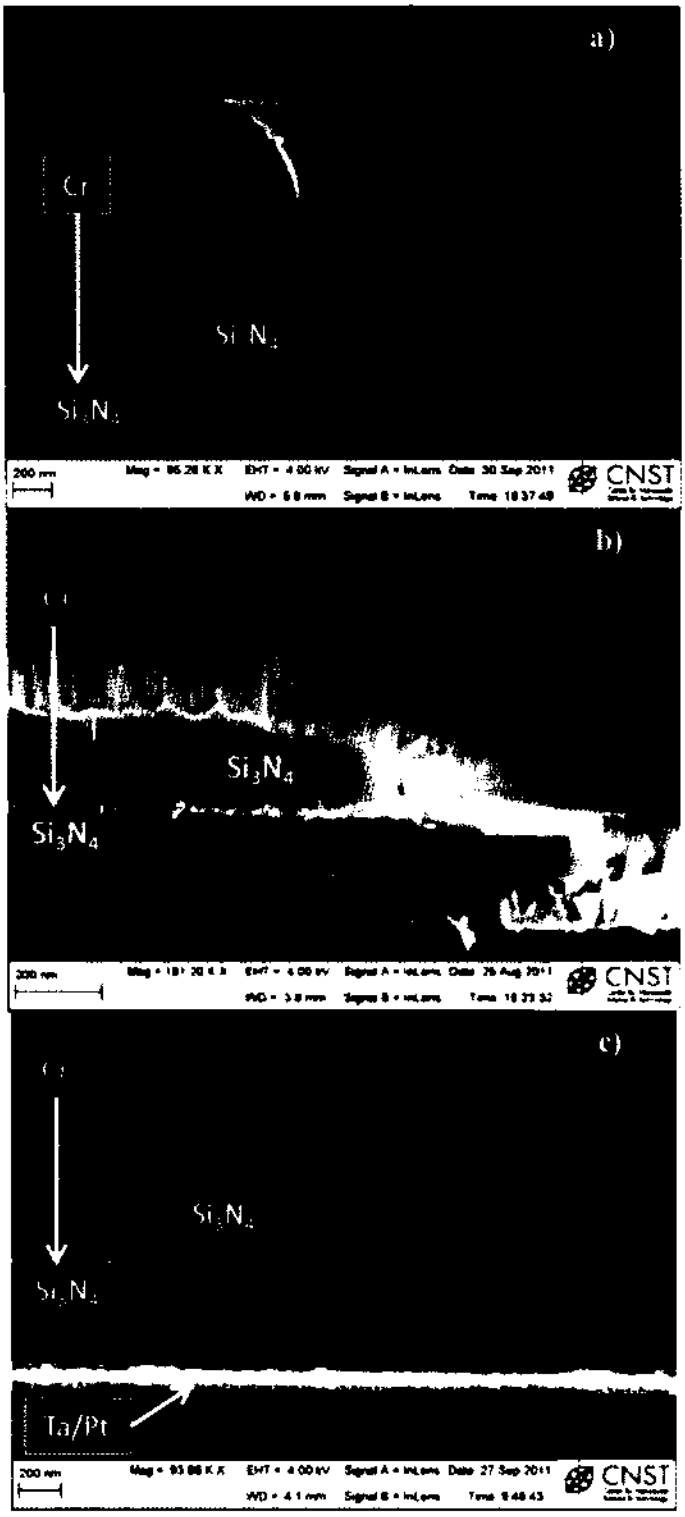


Figure 21. SEM micrographs documenting the cross-sectional profile of a) conformal deposition of the Si_3N_4 spacer layer before etching, b) nano-grass formation due to the micro-masking effect caused by the sputtering of Cr and c) ideal Si_3N_4 spacer etch result using the ICP tool to prevent the micro-masking effect.

Once the spacer is formed successfully the Cr layer is etched to form the hard mask, which will enable the pattern transfer to the underlying Si_3N_4 by further etch processing as depicted in Figure 18 e). Once the patterns are formed in the Cr hard mask, the bottom Si_3N_4 layer is etched to form the necessary step for the next spacer as shown in Figure 22.

Figure 22. Schematic showing pattern transfer using the Cr hard mask a) before and b) after Si_3N_4 etching for next spacer.

At the completion of this step, the Cr hard mask is very difficult to remove without residue. The Cr residue from an incomplete hard mask removal then micro-masks the layer underneath during etching, which results in the formation of nano-grass as documented in Figure 23 a). To prevent the formation of the detrimental nano-grass etch residue, the Cr hard mask is over etched by 50% instead of the standard 12% over etching used under normal circumstances. This over-etching strategy does help but leaves an etch undercut in the Cr and leaves residues close to the edges. For comparison, the etching results of the Si_3N_4 using 12% and 50% over-etching of the Cr hard mask are shown in Figure 23 a) and b).

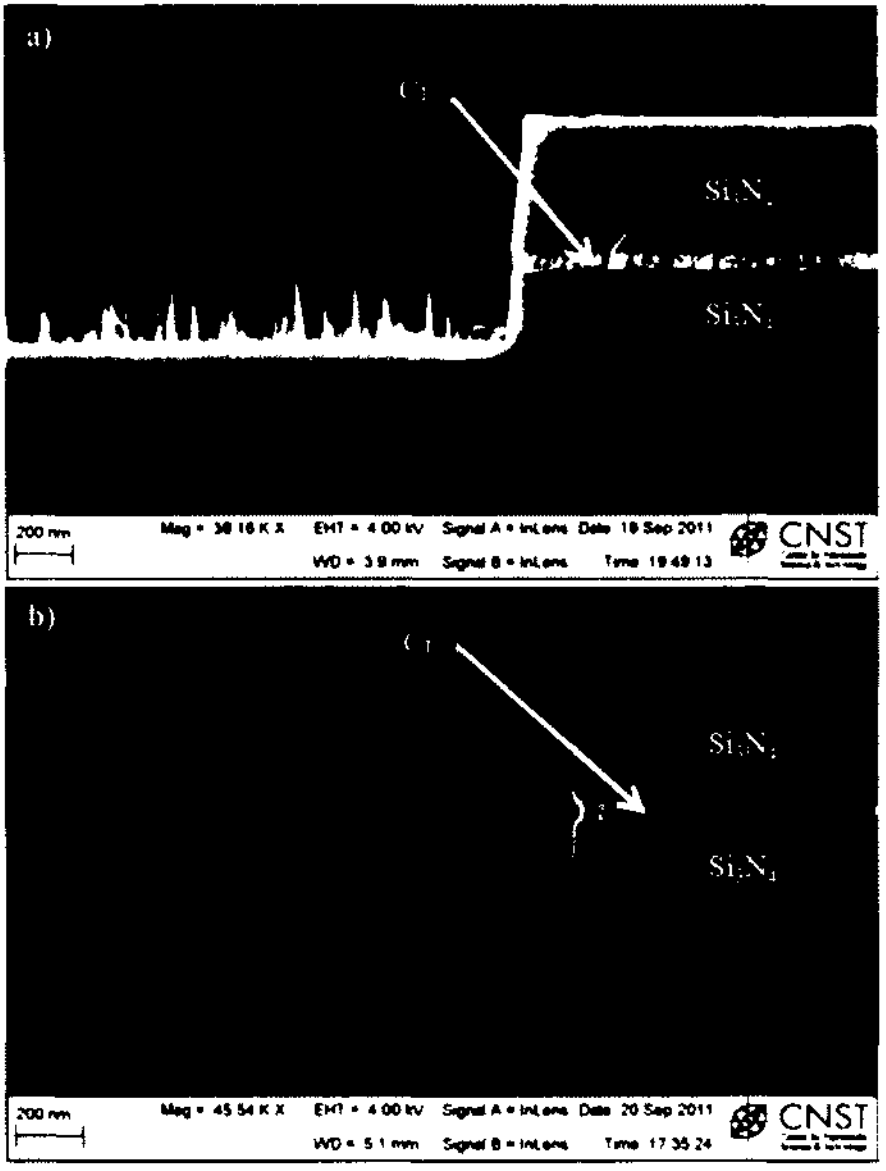


Figure 23. SEM cross-sectional profiles showing the Si_2N_4 etch with a) 12% over-etching of the Cr hard mask and b) 50% over etching of Cr.

To further improve the Cr profile and to remove the nano-grass structure obtained after the Si_3N_4 etching with 12% Cr over-etching, the device structure is dipped into HF for 1 min. The etch rate of PECVD Si_3N_4 in 2% HF solution is about 10 nm/min. Using this wet chemical etch process the nano-grass is safely removed with little damage to the etch

profile. Figure 24 documents the SEM images of the resulting etch profiles, before and after the 2% HF dip.

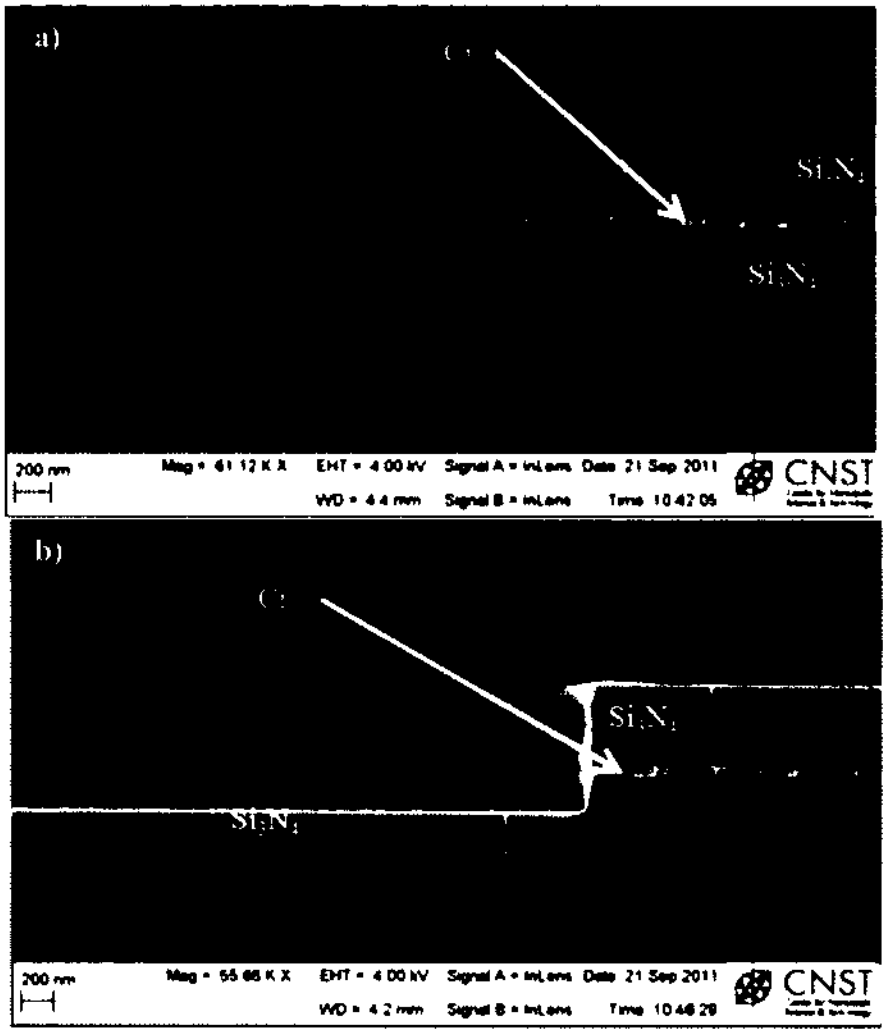


Figure 24. SEM micrographs of cross-sectional profiles of S_3N_4 etching with a) 12% over etching of Cr and b) after 1 min 2% HF dip to remove nano grass.

The first spacer formation on the 1 μm structure is shown in Figure 21 and the subsequent formation of the smaller via obtained after step (g) in Figure 18 is shown in Figure 25.

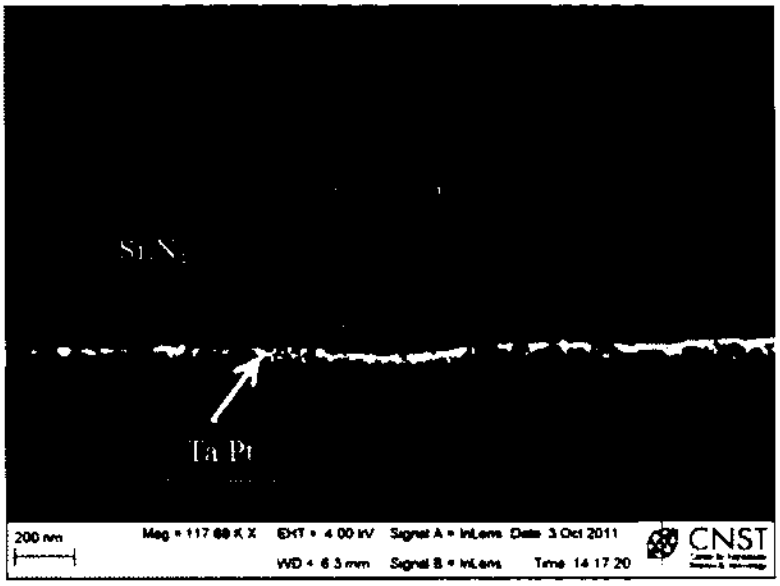


Figure 25. Cross sectional SSEM images of via obtained after the first spacer.

Process Development for Second Spacer Layer

Prior to the fabrication of the second spacers, the Ta_2O_5 electrolyte layer was deposited by sputter technique. The process details of the deposition of the Ta_2O_5 are given in Table 8. For the second spacer layer, similar processes were used that have already been developed for the first spacer layer. The difference between the formation of the first and the second Si_3N_4 spacer layer is primarily the aspect ratio of the via to be filled. The opening of the via for the second spacer had been designed for a much smaller size in the range of 500 nm – 200 nm. The aspect ratio for the second spacer layer is in the range of 2 to 1 when taking the height to be 400 nm, while it is 0.6 – 0.5 for first spacer (Figure 18 b).

Figure 26 a) shows uniform PECVD Si_3N_4 deposition but as the aspect ratio increases and the thickness of the spacer layer increases the deposition is no longer uniform as

demonstrated in Figure 26 b). Although PECVD yields very good film conformity, for this case and this mask Si_3N_4 layer overhanging can be seen due to limited surface migration. Such undesirable film overhang will pinch off the via opening and eventually close the via at the top. Therefore, the step height for the second Si_3N_4 spacer had to be optimized. The step height was around 400 nm for the first device generation. In order to subsequently insure better control on the via size the step height was reduced to 250 nm. Another process problem related to the high aspect ratio of the via is the sputtering of the Ta_2O_5 solid electrolyte. Due to the high aspect ratio, the sputtered Ta_2O_5 cannot be deposited uniformly at the bottom of the via step.

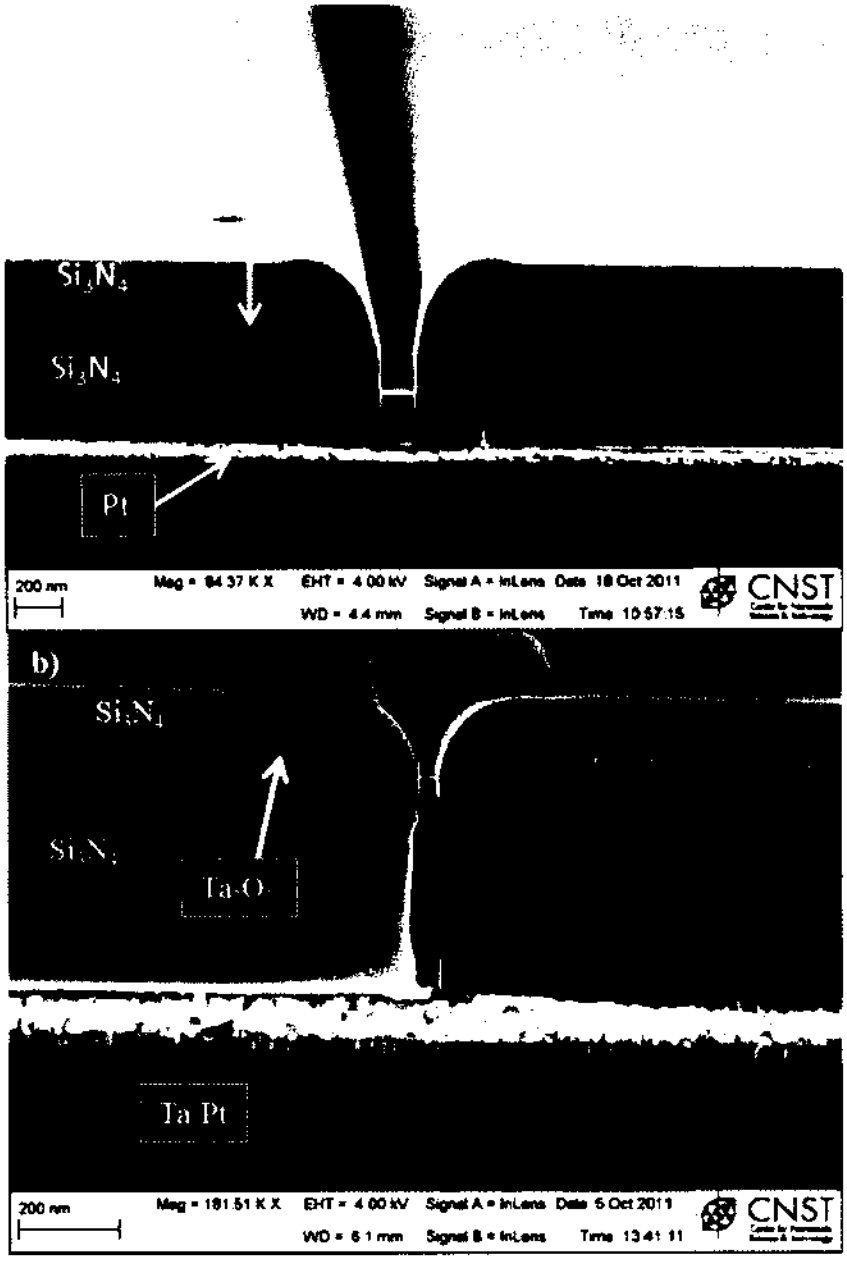


Figure 26. PECVD of Si_3N_4 spacer layer showing a) conformal deposition and b) over hanging due to high aspect ratio.

The solution to this process challenge was re-sizing of the via step height. Once the step height for the second spacer was sufficiently decreased, the film overhanging at the via opening was eliminated and finally the Ta_2O_5 solid electrolyte layer could be uniformly

sputtered. When employing this optimized process flow, the smallest via sizes obtained using the double spacer layers was around 35 nm measured at the via bottom. The SEM image of Figure 27 highlights the best result featuring the smallest via size obtained.

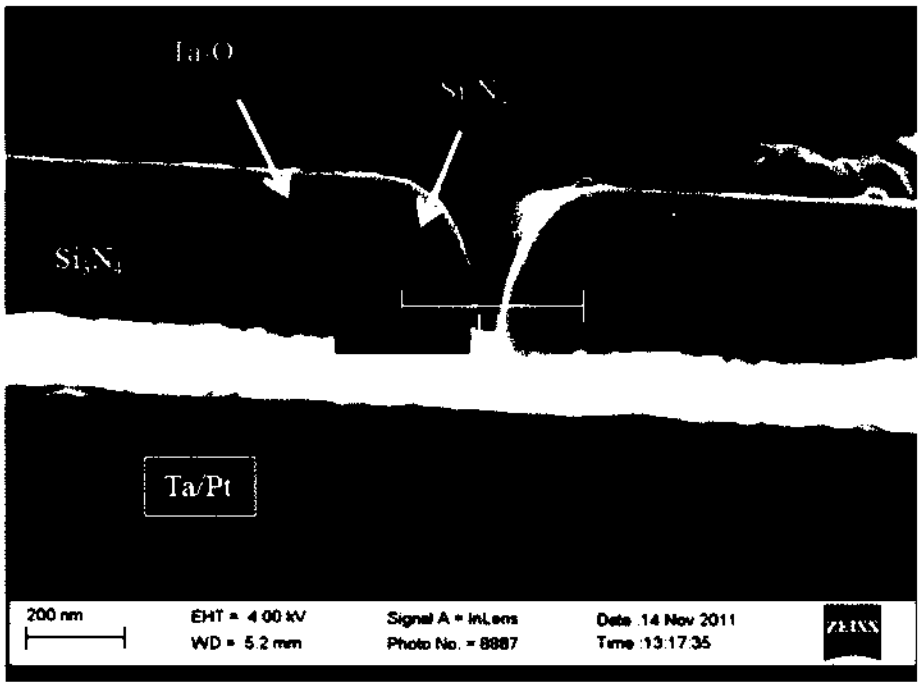


Figure 27. SEM micrograph showing the profile of the Second spacer layer with a reduced step height of 250 nm and with a via bottom opening of 35 nm, which represents the best result.

Following successful process optimization to achieve the smallest via from the second spacer, the excess Si_3N_4 was dry-etched in such a way that a very thin sacrificial layer of Si_3N_4 is remaining over the Ta_2O_5 electrolyte layer. This precaution will avoid any damage to the underlying Ta_2O_5 layer due to the plasma etching. For high selectivity between Si_3N_4 and Ta_2O_5, this sacrificial protective residual film is later removed by wet etching in a hot Phosphoric acid bath. The next challenge is to deposit metallic Cu by sputter technique overlaying this structure to finally form the oxidizable top electrode.

Cross-sectional images after the Cu deposition are displayed in Figure 28. It can be clearly seen from the SEM images that the larger vias in Figure 28 a) have a uniform Cu layer deposited over the Ta_2O_5 solid electrolyte layer. However, for smaller vias, Figure 28 b) demonstrates that the sputter deposited Cu layer did not reach and could not contact the Ta_2O_5 electrolyte at the bottom of the narrow via opening.

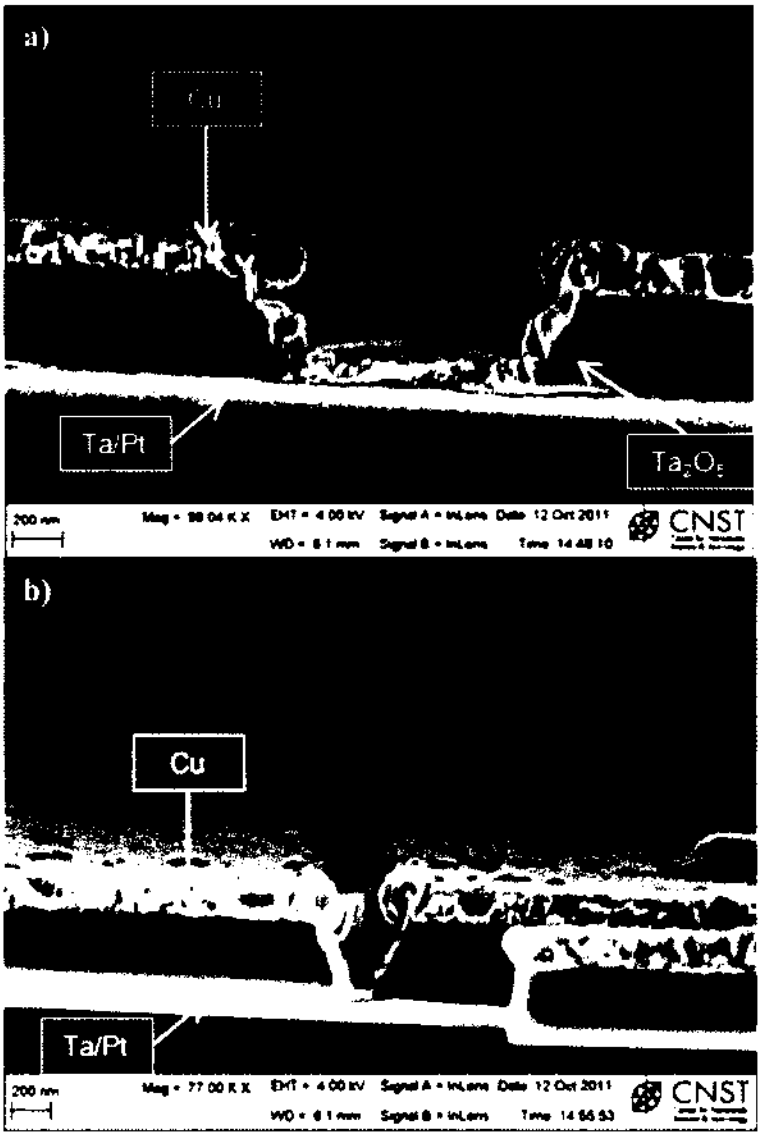


Figure 28. Cross-sectional SEM images of the device structure highlighting the uniformity of the Cu metal deposition a) for the case of larger via sizes and b) the unsuccessful case for much narrower vias.

The images of Figure 28 a) and b) suggest that the aspect ratio of the vias prior to the Cu deposition has to be decreased and optimized. The size of the via bottom opening is critical in the quest for the smallest device and therefore should be kept as small as possible. Keeping this objective in mind, the only parameter that can be changed to decrease the aspect ratio is the step height. Decreasing the step height comes at the expense of less control over the final opening after the second spacer. Since the desired via size is in the range of few tens of nm, final control of the via opening is very important. Therefore, the only solution to improve the Cu deposition and the via size control is to develop a three spacer layer technology. The SEM cross-section of Figure 29 demonstrates a best in class example of what can be achieved using the double spacer technique highlighting an actual device with size of $\approx$ 250 nm.

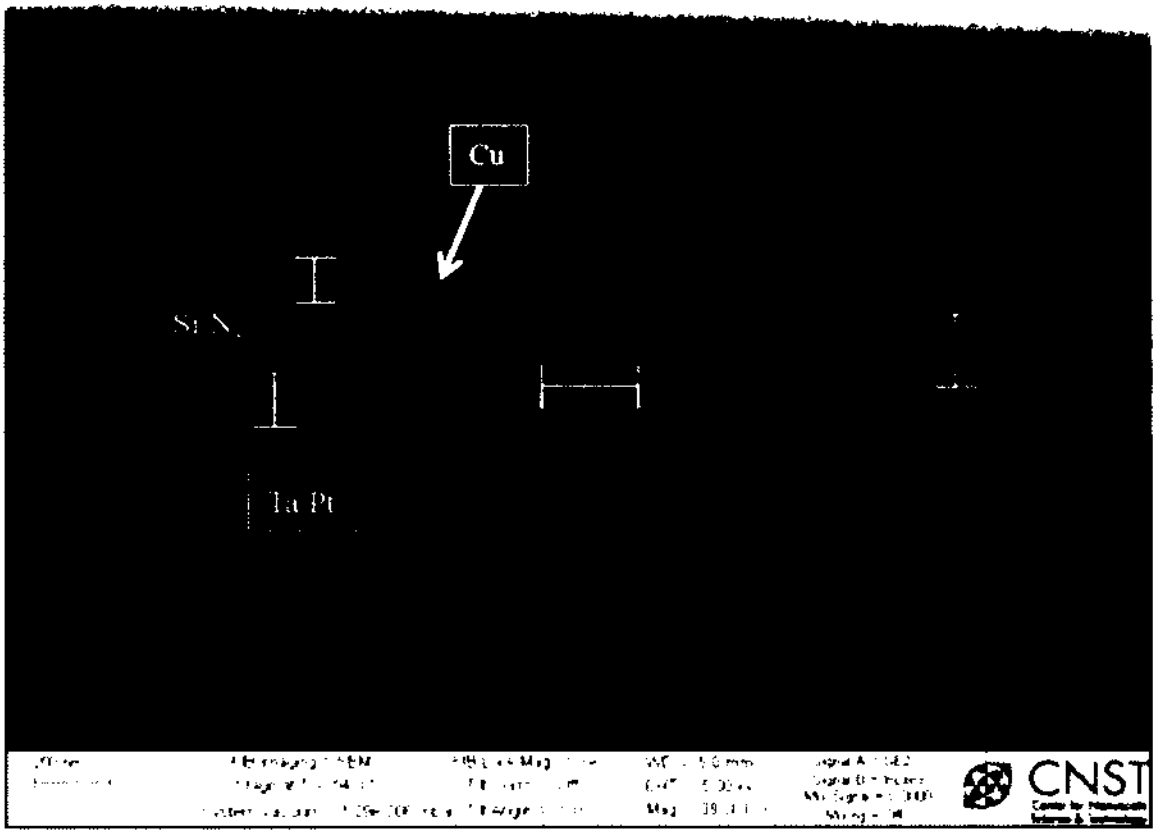


Figure 29. SEM of cross-section of typical device achieved using the double spacer technology. The cross-section was visible after milling with FIB technique.

Development of Multiple Spacer Technology

As explained in the earlier section, the analysis of the experimental results led to the conclusion that the development of a three spacer layer technology is necessary in the quest to achieve the minimum device size based on the tool capability of the NIST clean room. A new step height of 50 nm was used for the third spacer in order to achieve more uniform Cu deposition and better control of the via size. The size of the via bottom opening after the second spacer was kept around 100 nm. A full schematic of the complete integrated process flow is given in Figure 30.

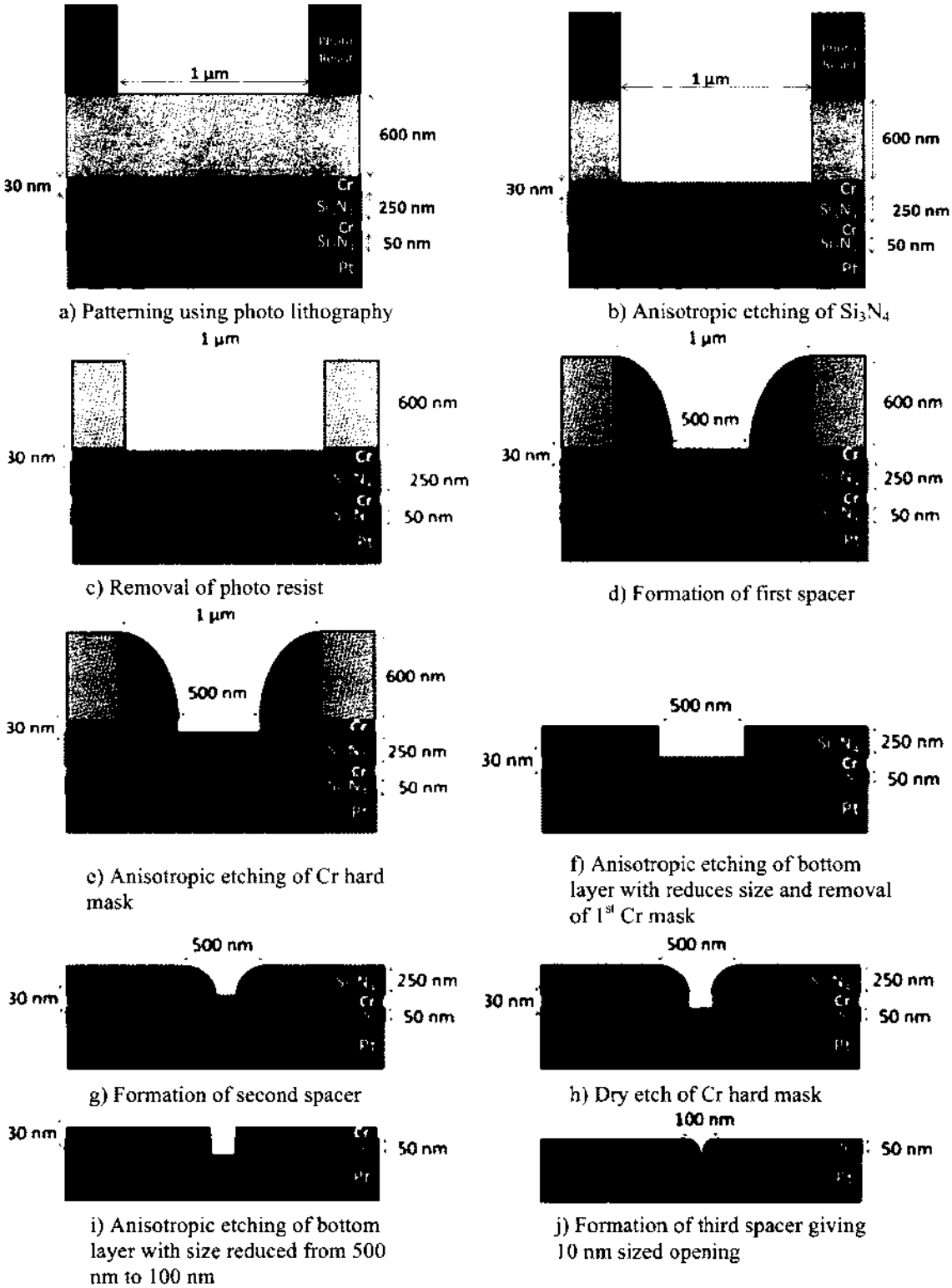


Figure 30. Simple schematic representation of the integrated processes flow involved in three layer spacer technology to achieve nm sized via openings, which ultimately define the minimum device size achievable.

All the process steps used for the three-layer spacer technique are similar and follow the double spacer technique until step (e) of Figure 30. Removal of the top Cr hard mask layer after the first spacer, without affecting the bottom Cr, was a challenge involving the following process steps from step e) to f). As depicted in Figure 31, resist etch back was used to remove the top Cr without affecting the bottom Cr. A thin resist layer is first coated over the wafer using spin coating. Such a spin coating process naturally collects thicker resist inside the vias compared to the flat surface parts of the Si substrate wafer. The resist is then etched just enough to uncover the top flat surface layer. If the etching process is well controlled, the via holes that started with much thicker resist will still be covered with resist that has only been slightly eroded. That remaining resist inside the vias acts as the protective mask for the bottom Cr. Once this was achieved, the top Cr layer was wet etched. The resist is then removed using 1165 sonication to achieve the final structure (Figure 31 e). Good control of resist etch and resist thickness are important to achieve the necessary outcome for minimizing the final device dimensions.

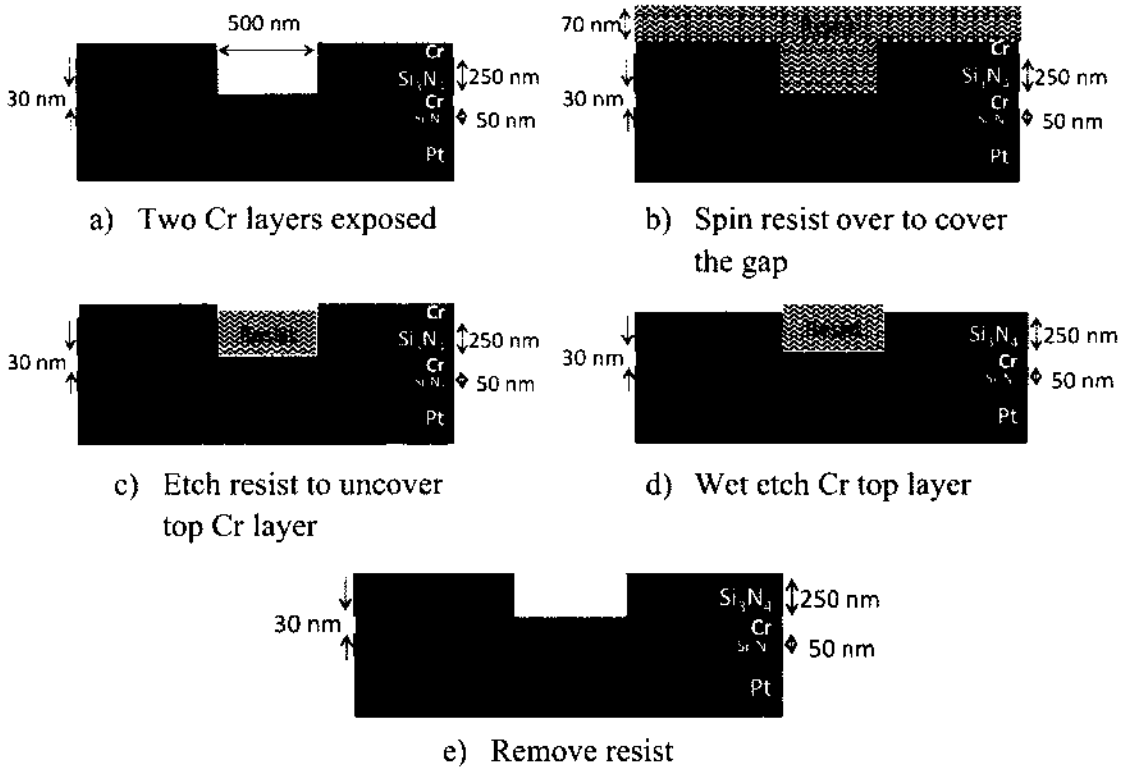


Figure 31. Schematic integrated Process flow to remove top Cr layer without affecting bottom Cr.

Loading effect

The term loading effect is the effect where the etch rate depends on the area of the surface of a patterned wafer to be etched [97, 98]. During the etching of the resist process flow shown in Figure 31, the etch rate of the resist changes dramatically from step b) to step c). The root cause for this lies in the fact that the etch reaction in c) is much less compared to b). If the reactive species remain in the RIE chamber long enough then they etch the smaller areas faster compared to the larger patterned areas that have to be etched. For this reason, the thickness of the resist is kept as thin as possible to achieve better control over the etch time.

Resist Spinning

S1813 was chosen for the resist etch back due to its compatibility with the Cr wet etchant. S1813 achieves a resist thickness of around 1.2 μm at 4000 rpm during spin-on. However, this resist coating is too thick and prevents a good control during plasma etching. Therefore, S1813 was thinned to achieve a thinner resist coating during spin-on. A commercial thinner Type P was used to thin the S1813 resist. A ratio of 1 part of S1813 and 5 parts of Thinner Type P was used and the resist was spun-on at 6000 rpm. The resulting thickness of the resist coating ranges from 60 nm – 70 nm. As expected, the via holes were covered with a thicker 143 nm resist because the resist is stuck in the via holes and accumulates in the vias during the spin-on process. The SEM images are shown in Figure 32.

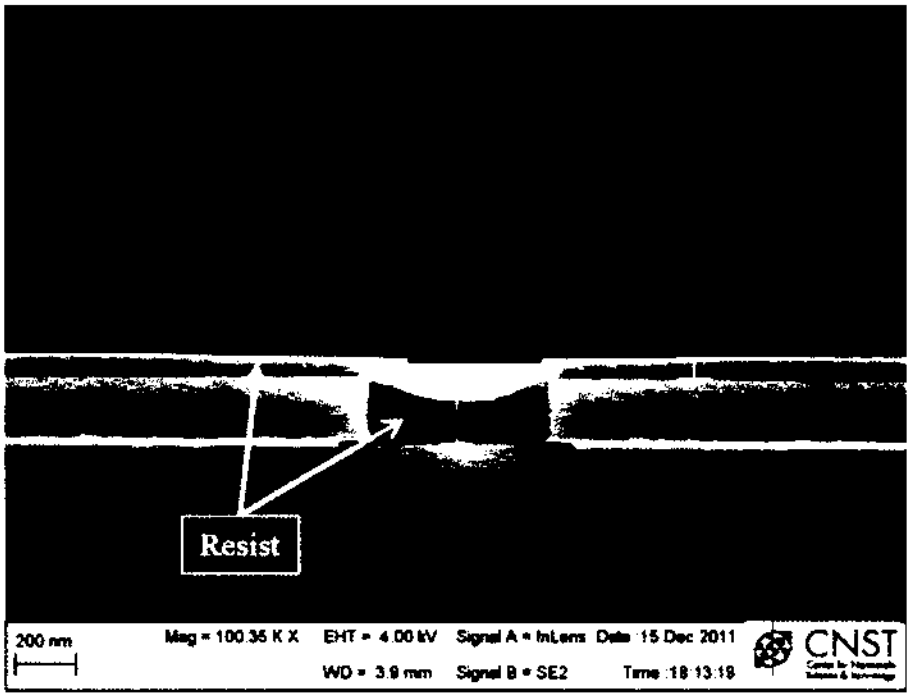


Figure 32. SEM cross-sectional images of via holes revealing a much thicker accumulated resist in the vias compared to the flat surface following the spin-on resist coating process.

Etch-back with Descum Process

The resist Descum process explained in Table 5 is then used to etch the resist. SEM cross-sectional images providing proof of the remaining resist are shown in Figure 33.

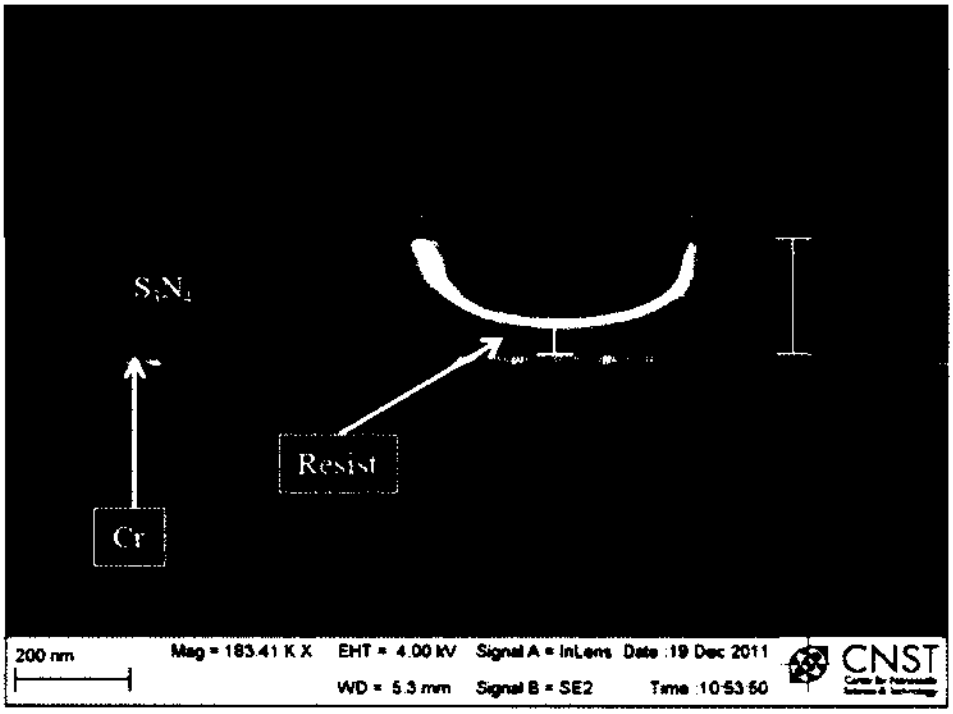


Figure 33. SEM cross-sectional images of via with resist after 3 min 20 sec etch.

Once the top Cr was exposed without exposing the bottom Cr, the top Cr hard mask layer was wet etched. Figure 34 documents the integrity of the Cr hard mask before and after the Cr wet etch. The top Cr hard mask is removed without affecting the integrity of the bottom Cr layer. The presence of notches on the top and the bottom of the via opening can be seen in Figure 34 a). These notches occur at the edges of the interface between the Cr and Si_3N_4 layer. The observed notches are attributed to the potential difference in the Si_3N_4 and Cr surface layers [99-101]. The longer the over etching proceeds, the more

prominent are the observed notches. For this reason, the over-etching time was kept as short as possible.

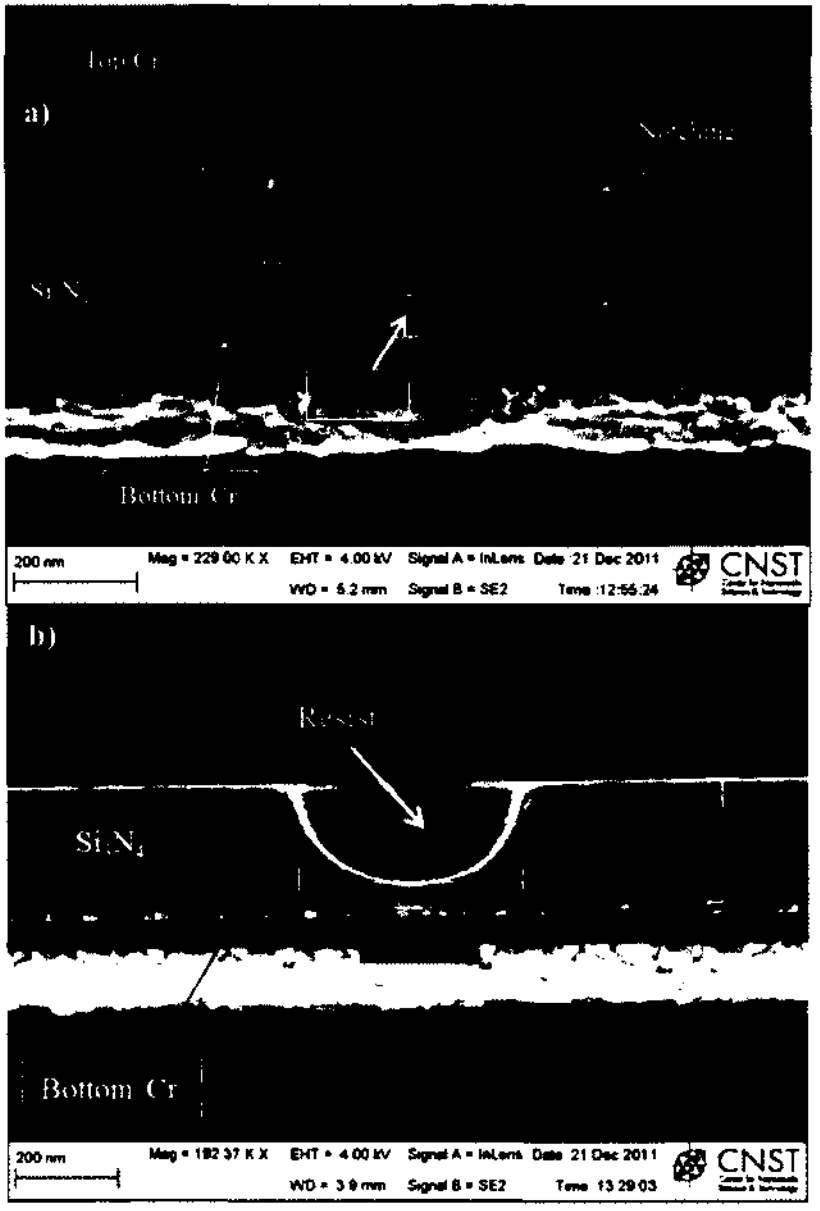


Figure 34. SEM images revealing removal of the top Cr hard mask layer without affecting the bottom Cr layer using accumulated thick resist in the bottom as protective layer for the bottom Cr layer.

Once the bottom Cr layer is exposed, similar processes mentioned in double spacer technique is used to complete the device.

Sample W: Novel Device Structure Promoting a Single Filament Formation by Constricting the Cu Electrode Area

Figure 35 shows a Schematic cross-section through the crossbar switch device and SEM images of the actual device W fabricated with the multiple spacer technique. Figure 35 b) shows the cross section of an actual device from a control sample used to check the process flow. Finally, Figure 35 c) is the SEM image of an actual device revealing the surface morphology of the fine-grained polycrystalline sputtered Cu metal electrode as the last layer on the top.

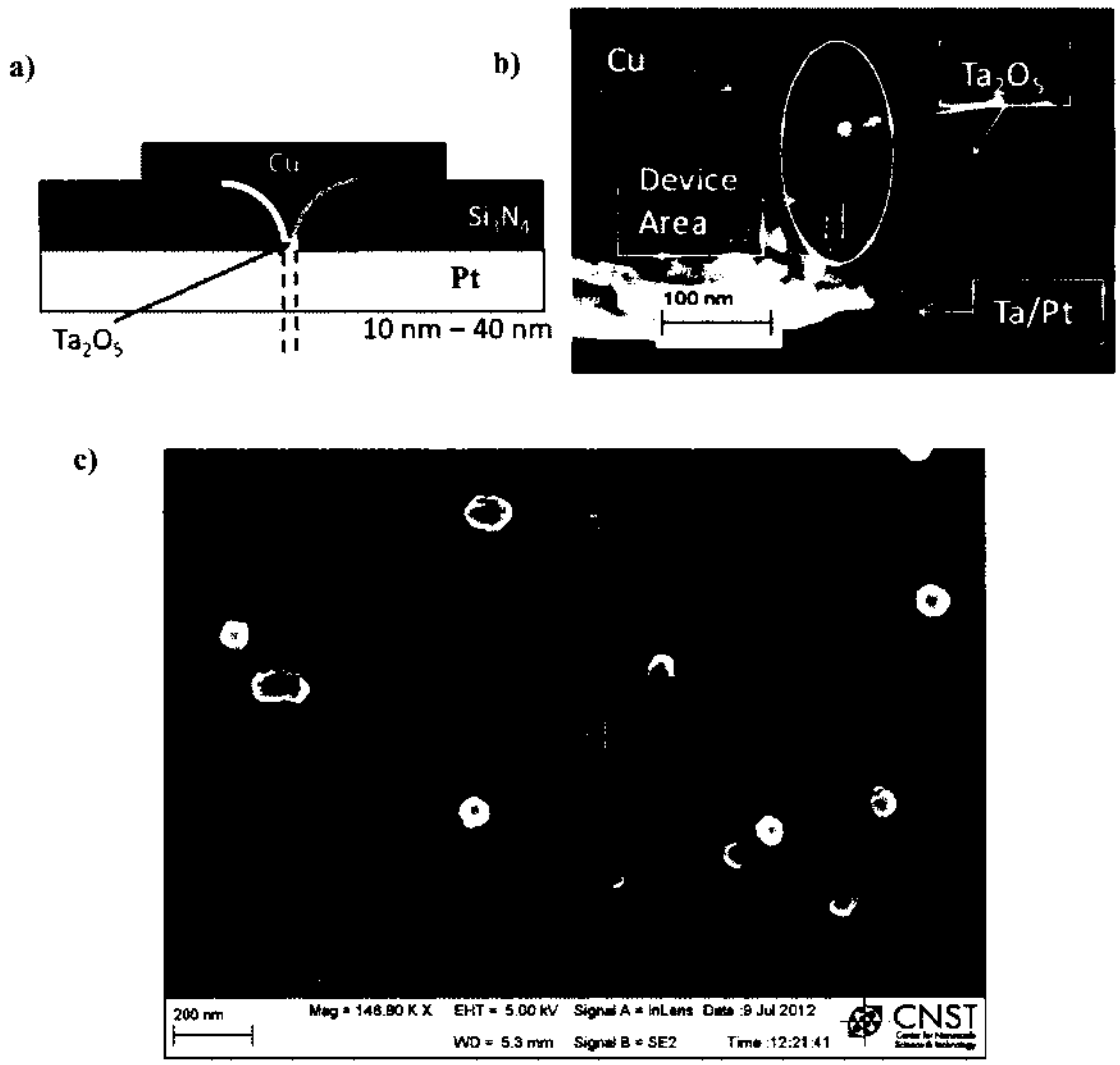


Figure 35. a) Schematic cross-section of a device following the process flow of the sample W fabricated , b) SEM cross-section micrograph of the actual device fabricate d with process flow of sample W and c) SEM top view revealing the polycrystalline nature of the sputtered oxidizable Cu top electrode.

The device W was fabricated with the objective of improving the switching uniformity by significantly reducing the number of potential metal filament formation sites. This was accomplished by considerably constricting the Cu area. This new mask design, with restricted Cu area, reduces the possibility of many new random sites for filament formation during every new device cycling or every device. Figure 36 explains the

experimental approach and shows a schematic model for the formation of multiple random metal filament sites for the case of large Cu electrode areas and the case of a restricted Cu electrode area promoting the desired single filament formation site.

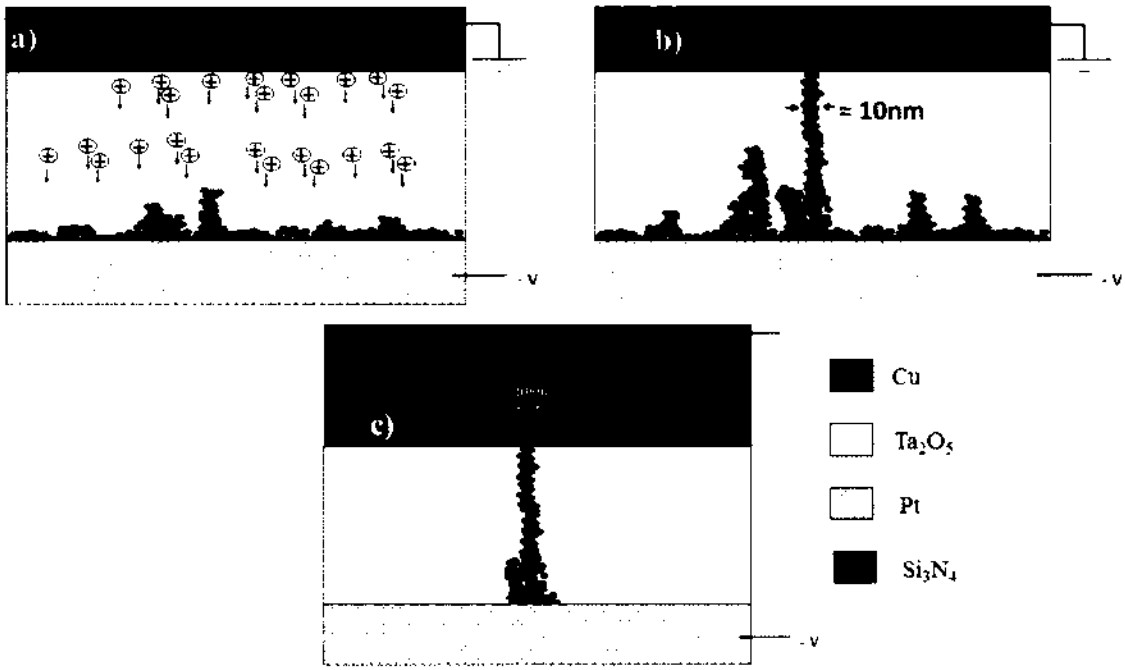


Figure 36. Schematic model showing a) current of Cu^+ ions flowing towards the Pt electrode in presence of negative voltage on the Pt electrode and dendritic Cu filaments starting to form at numerous sites for the case of a large Cu electrode area, b) formation of an electric short by only one single fastest growing conductive Cu filament and c) the model case of a restricted Cu electrode area promoting the desired single filament formation site using device X.

Sample X: Advanced Design to Restrict Cu Nucleation Sites for a More Accurate Control of the Single Metal Filament Size and Location by Constricting the Pt Electrode Area

Although the design of device W has severely constricted the Cu electrode area, this by itself does not guarantee less filament nucleation sites. This is because the Cu filaments nucleate by a reduction process and start to build up from the Pt electrode side (Figure 36), which still maintains a relatively large area. In the case of the specific process flow

explained in Figure 35, the device ends up with a limited area through which the Cu ions can enter the Ta_2O_5 solid electrolyte. However, as demonstrated in Figure 36, that particular device design strategy is still vulnerable to multiple random nucleation sites of the Cu filaments anywhere on the large are of the bottom Pt electrode. In order to remove this last possibility for metal filament nucleation site variability more advanced device architecture was designed with a new mask set. With this new strategy in mind, another new set of devices was fabricated with the schematic structure shown in Figure 37, where the point at which the Cu filament starts to nucleate is fixed. Previously published work has provided experimental evidence that the Cu metal filament is the thinnest closer to the inert Pt electrode[76]. Thus in principle, the point at which the filament breaks during RESET, which equals the thinnest path can be fixed and controlled. The technique of breaking the metal filament closer to the inert electrode showing uniform switching has been successfully demonstrated by Sakamoto et al [77].

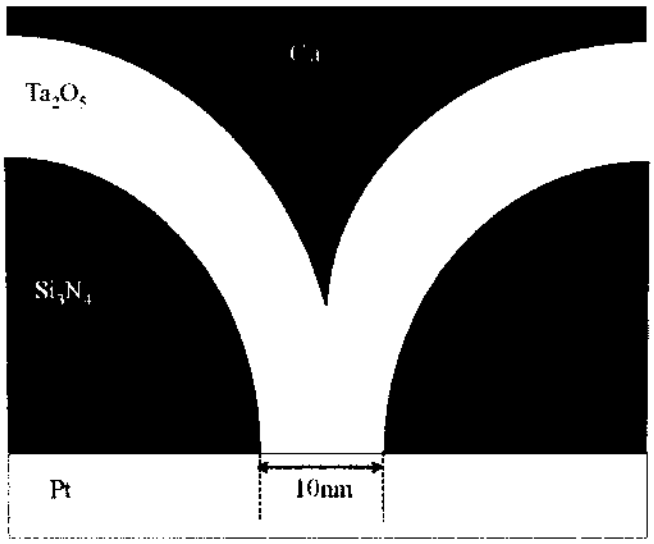


Figure 37. Schematic of device X design providing in addition to restricted Cu area also a minimum Pt electrode area in order to restrict and fix the nucleation site for the Cu filament.

CHAPTER 3

EXPERIMENTAL SETUP FOR ELECTRICAL MEASUREMENTS

Different measurements setups mentioned in this chapter are used for a variety of analysis purposes. Some are designed to overcome the shortcomings of previous measurement techniques, whereas others are designed to achieve a better understanding of the crossbar-switching device with Ta_2O_5 solid electrolyte. This chapter describes the measurement setup and highlights the significant novel aspects of the measurements. The objectives and aspirations behind the design of these setups are explained in detail in chapter 4.

3.1 Parameter Analyzer

Every time a new device was completed, preliminary tests were performed with a regular parameter analyzer. The Agilent B1500A parameter analyzer was used in each test. The noise level of the analyzer is in the range of femto Amperes (fA). Therefore, a useful analytic tool provides accurate measurements of very low currents during the OFF state of the device.

It is important to note that, based on Ta_2O_5 solid electrolyte and Cu and Pt electrodes, an initial "forming" process is required to start the switching process in these non-volatile crossbar switch devices. Initially, high voltage is required to switch the device (Figure 38). Current compliance has to be provided every time the device is switched from OFF to ON state in order to limit the current through the device when the device switches to a low resistance state. Otherwise, the high current would be detrimental to the filament and

may damage the device. After the initial forming process, the voltage is swept from negative to positive voltage and then swept back to the negative voltage to complete one switching cycle. A typical voltage sweep for a device of size 10 μm x 10 μm is shown in Figure 39. Here the voltage is swept from -1 V to +1 V. Note that the voltage for switching ON and OFF is less than the voltage required for the initial forming process.

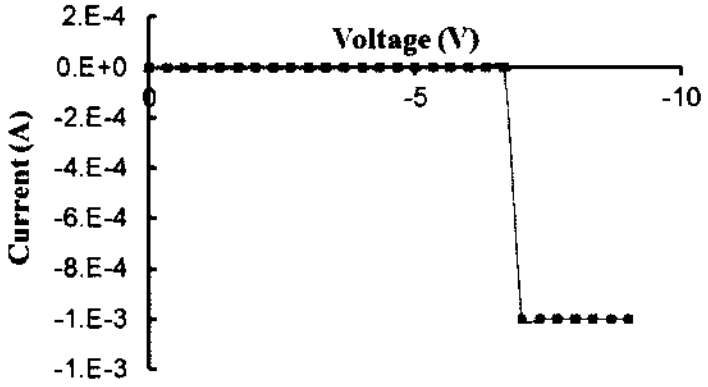


Figure 38. Typical Forming process for sample A, with device size of 15 μmx15 μm requiring initially much higher voltage to start the switching cycle.

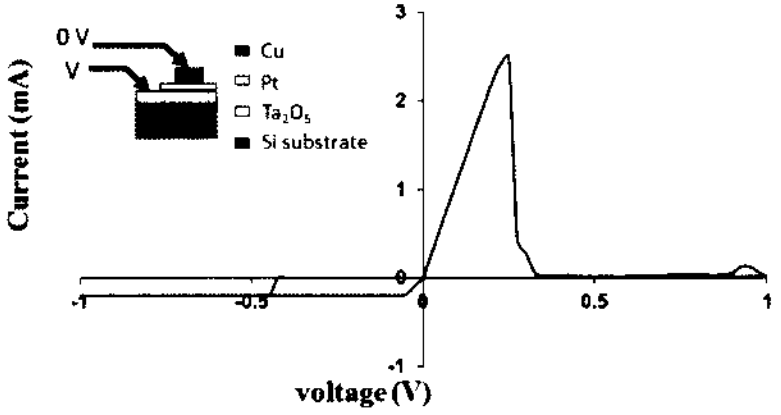


Figure 39. Voltage sweep with ON at current compliance of 200 μA. (inset: schematic of the device structure and the probes).

Next, the resistance was measured after each SET and RESET. A short program was written for the Agilent B1500A parameter analyzer to repeatedly perform these tasks. The program consists of five input variables: the number of cycles, the maximum positive voltage, the minimum positive voltage, the ON current compliance and the OFF current compliance. Once these inputs are entered, the program sweeps from 0V to the maximum negative voltage with current compliance for ON state (SET). The resistance of this ON state is measured from 0V to 100 mV. The device is then "RESET" (switched OFF) by sweeping the voltage from 0V to the maximum positive voltage. Again, the resistance of this state was measured from 0V to 100. This process was repeated from the beginning until it reaches the specified input number of cycles.

Figure 40 shows the set of measurements performed on large devices with 15μm x 15μm size for 600 cycles. These measurements provide very precise resistance values; however, the drawback is that these measurements are very time consuming. Each set of measurements with SET, measuring resistance ON resistance (R_{ON}), RESET and measuring OFF resistance (R_{OFF}) takes about 3 min. This means significant time is needed to obtain the data for a large number of switching cycles, which are important for reliability assessments and lifetime tests.

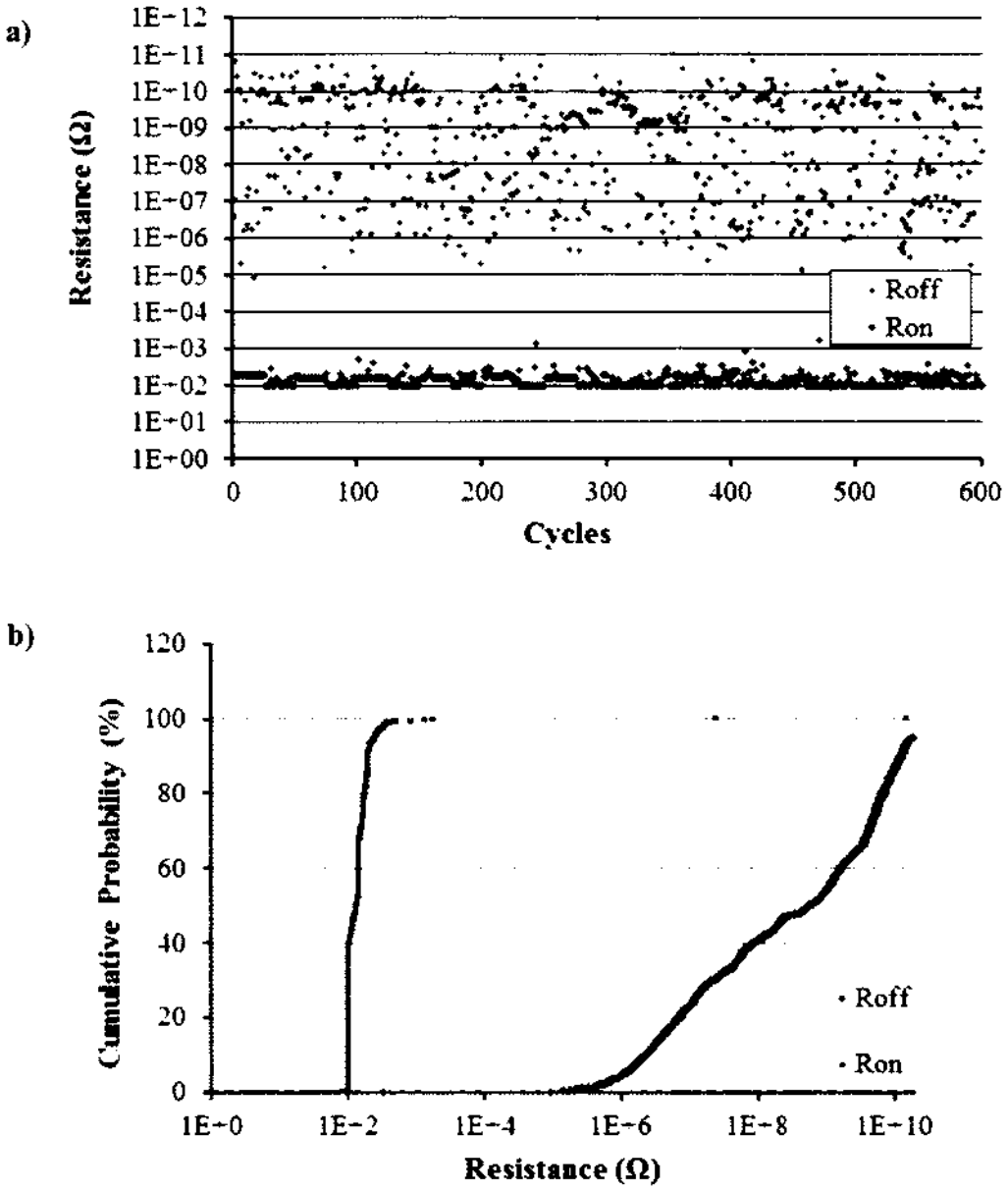


Figure 40. Measured resistance values obtained for 600 cycles of switching devices with 15μ x 15μm size a) distribution of R_{on} and R_{off} vs. the number of switching cycles b) cumulative probability for the Distribution of Ron and Roff.

3.2 Pulse Switching

In order to perform fast measurements, the HP 4556 pulse generator was used with 7 ns rise/fall time. A Lecroy wave-guide was used to measure the signal. A small resistance of 300 Ω was used in series with the device to obtain the current through the circuit. Figure 41 shows details of the special circuit, which was custom designed and built for this thesis work. This circuit was placed in series with the device to provide current compliance during the endurance test using voltage pulse. This custom tailored circuit consists of a rectifying diode that allows high current only in one particular direction through the device. In this case, only high positive current passes through during RESET. The current compliance circuit limits the negative current for SET. According to the resistance values used in the circuit shown in Figure 41, 200 μA is the maximum current flowing through the device for a negative voltage applied. A 50 Ω resistor was also added across the input to match impedance. The points V1 and V2 in the schematic of Figure 41 are fed to the oscilloscope along with the input.

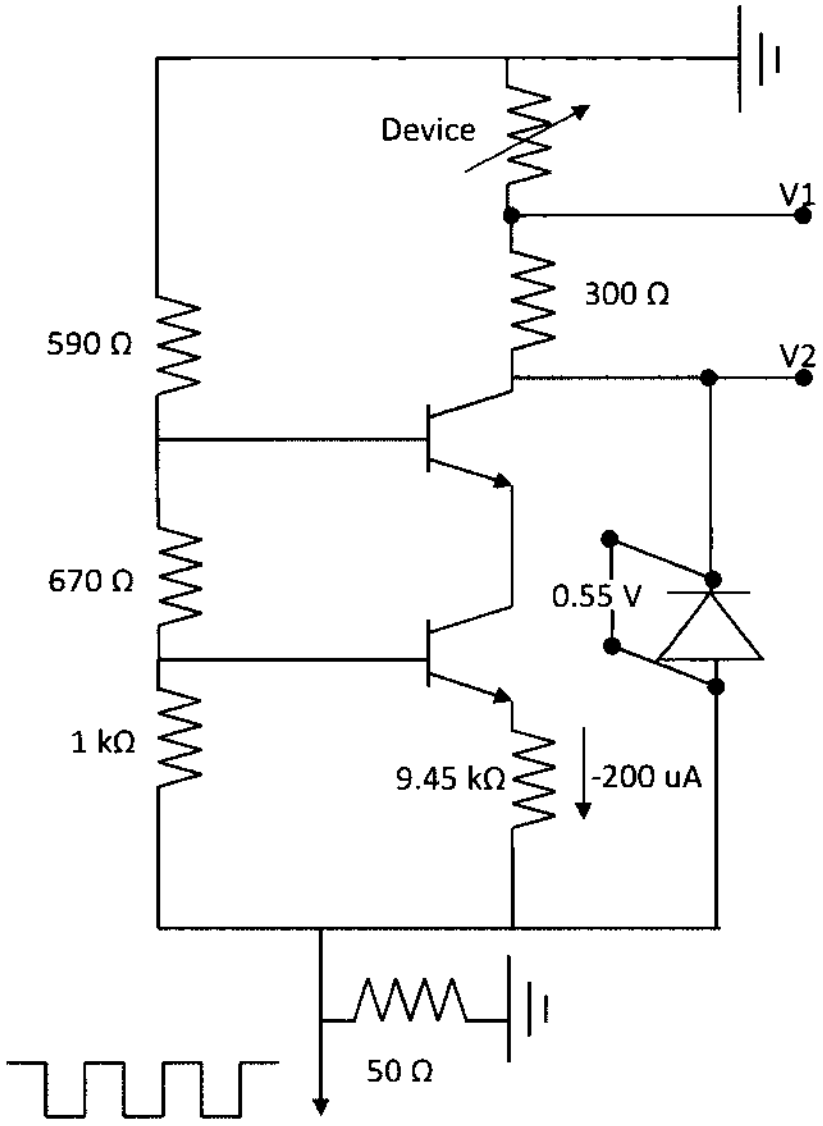


Figure 41. Custom designed Circuit used for current compliance and current measurement through the device.

Data obtained from the oscilloscope was then used to calculate the current flowing through the device. LabView was used to analyze the data and to obtain the R_{ON} and R_{OFF} values for each switching cycle. Figure 42 shows the R_{ON} and R_{OFF} values obtained with a 1kHz signal while using V_{ON} = -6V and V_{OFF} = 4V. The data shows the presence of switching at the signal rate of 1 kHz. However, the careful analysis of this measurement

setup revealed the following technical issues. The problem with this system is that high speed in the range of nano seconds (ns) is not possible due to the presence of slow devices such as the Bipolar Junction Transistor (BJT) and the diode, in the custom circuit. The other important point is that the R_{OFF} obtained in the data is not very accurate. This occurs because the current flowing through the device during the OFF state is very low. Therefore, the voltage obtained is very small. Furthermore, the 8-bit resolution of the oscilloscope is not sufficient to obtain the highest accuracy. The lowest voltage that the oscilloscope would be able to detect with a reasonable accuracy is around 15 mV. With this voltage across a 300 Ω resistor, the highest resistance the oscilloscope can detect is around 100 kΩ. For this reason, the R_{OFF} values displayed in Figure 42 are limited by the measurement setup and equipment.

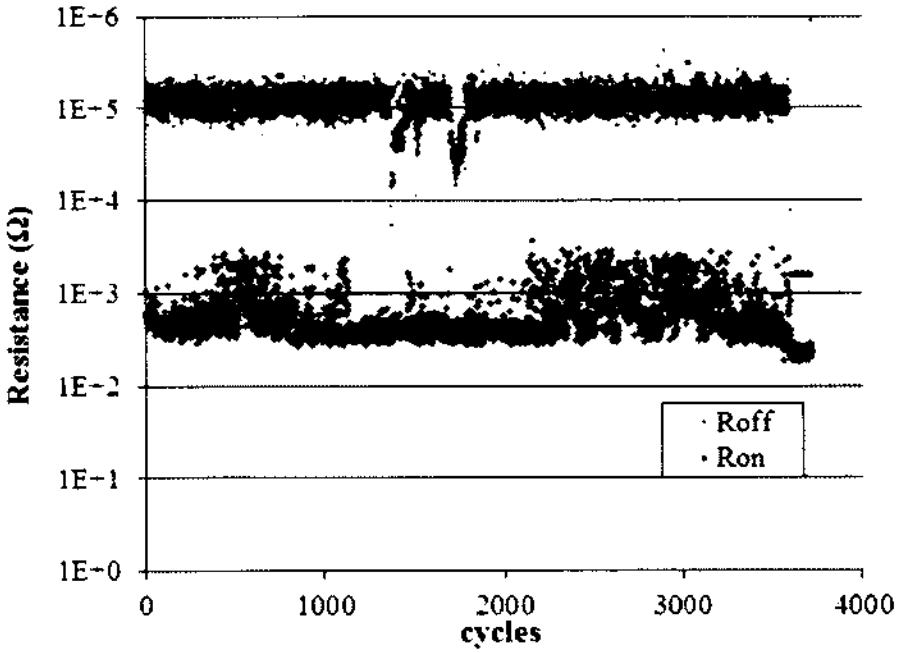


Figure 42. Resistance Data obtained by pulsing 1 kHz signal with low = -6V and high = 4V.

Due to problems like low speed and accuracy, new measurement techniques and approaches are explored.

3.3 Fast I-V Setup for Transient Measurements

This new measurement setup was primarily designed to measure the transients during the switching of a device. There are mainly two components for this fast I-V setup for transient measurements. First is the fast and simple current compliance circuit that limits the current through the device during SET for stable switching. Second is the fast amplifier that is capable of following and amplifying the transient signal. The amplifier

allows current to voltage measurement with well-defined terminal potential to the device under test (DUT).

New Circuit Design to Limit Current through the Device

For this technique, a resistor with high resistance and a diode is taken to limit the current. The schematic in Figure 43 shows a diode and a resistor of a fixed size. The concept here is to limit the current during SET and then to let higher current flow through the device during RESET. Since the device is a bipolar switch, a diode is used to block current though the device in only one direction and let the current through in the reverse direction. The current with negative polarity is forced through a 5 kΩ resistor so that the current is limited by the large resistance. For positive voltages, the current preferentially flows through the diode following the least resistance path. This allows the current to be high for the positive voltage and low for the negative voltage. The diode used in this circuit is a Schottky diode with a fast recovery time. These components are placed on a Printed Circuit Board (PCB). The PCB was physically placed very close to the probe that goes to the Pt electrode.

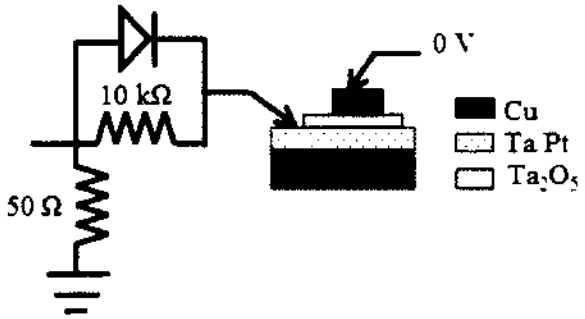


Figure 43. Schematic of the Current limiting circuit.

High Speed Amplifier for Transient Measurements

For many applications, the switching speed is an important performance factor and many researchers have reported fast switching in various material systems [49, 70, 102, 103]. Even though high-speed measurements can easily be plagued by artifacts, few authors have explicitly discussed the details of their measurement techniques. Resistive switching devices operate by changing resistance from high (R_{OFF}) to low (R_{ON}) values in response to the applied voltage [29, 31]. Fast switching from one state to the other is an important clue to the underlying mechanism. Reliable measurements of the details of the transient response during switching are therefore crucial for a better understanding of the switching mechanisms.

The most common source of artifacts in high-speed measurements is the transmission line effect that distorts the signal when there is an impedance discontinuity. The best strategy is to avoid the transmission line effect altogether. For our test configuration, the circuit is built on a small board with the probe needle directly attached to the input end as shown in Figure 44. The total distance from the device under test (DUT) to the inverting input of the high-speed operational amplifier (opamp) is less than 3 cm. At such short length, the transmission line effect is negligible for rise times as short as 0.8 ns [104, 105]. This brute force approach is the simplest way to assure signal integrity, while at the same time this design provides a well-defined terminal potential for the device under test. This approach can be extended to faster rise times; with a change to a shorter distance from the probe tip to the amplifier. However, distances shorter than 1 cm will make the current test

configuration more difficult. Thus the practical experimental limit is about 0.2 ns rise time or slightly over 1 GHz.

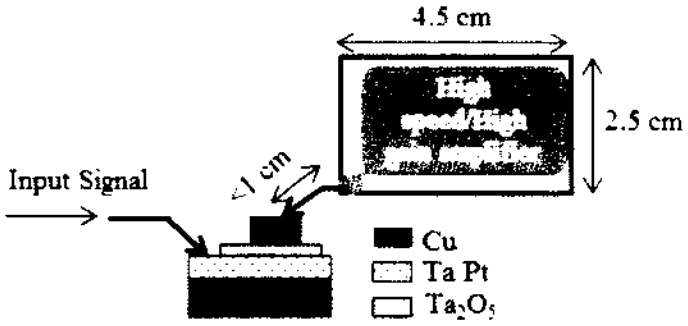


Figure 44. Schematic of test configuration showing the final position, the overall size and the setup of the custom circuit designed.

The configuration of a current feedback opamp with a bandwidth of 1.7 GHz has been chosen, along with the proper bypass methodology for power supplies to support high-speed operation of the amplifier in order to ensure that the high-speed amplifiers will have performance matching. The bypass is accomplished by a set of three capacitors connected as close as possible to each power pin. The capacitor values are such that low impedance is achieved over a wide bandwidth. The circuit layout ensures that the signal path of the fastest signal is as short as possible. The output of the amplifier is carefully compensated (amplifier output impedance + external resistor in series) to achieve 50 Ω total output impedance, ensuring signal integrity all the way to the high-speed oscilloscope. A simplified schematic setup for the custom-built high speed amplifier is shown in Figure 45.

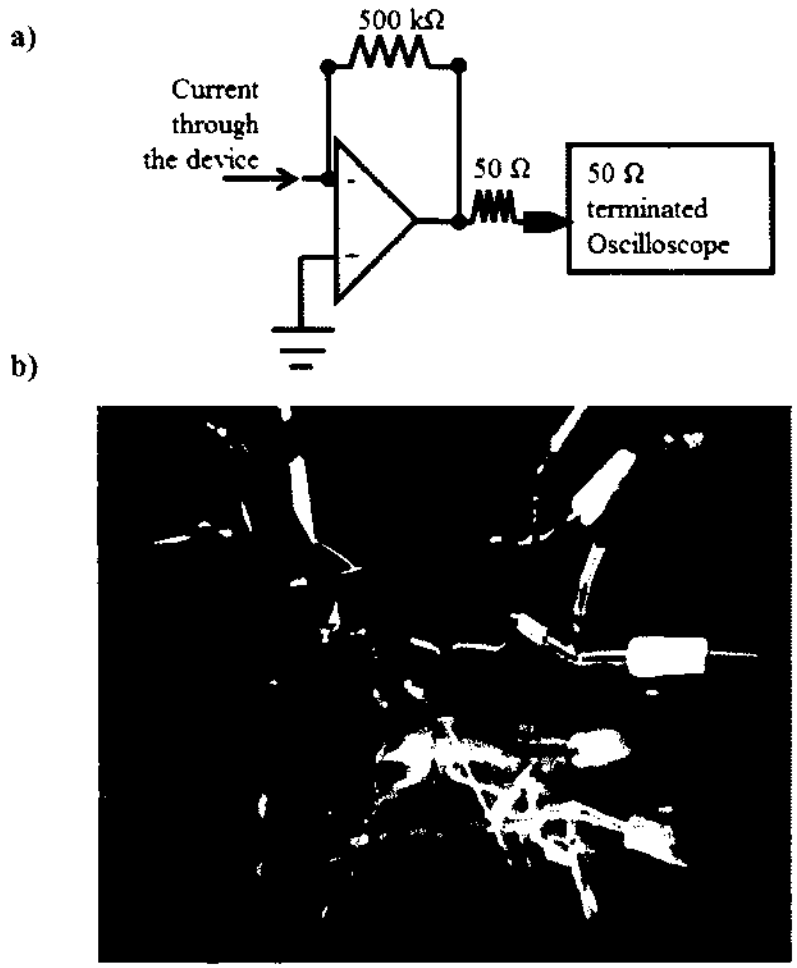


Figure 45. a) Schematic of high speed amplifier for high speed measurements and b) image of the actual amplifier setup.

The input signal applied to the device and the output of the high speed amplifier are then measured from the oscilloscope. A representative example of such a data set is presented in Figure 46. "Input" is the input voltage applied to the device. Since the negative voltage on the Cu electrode switches the device ON (SET), negative voltage is labeled V_{ON}. Positive voltage switches the device OFF (RESET), thus V_{OFF}. "Output" is the output from the high speed amplifier. This data is used to check the switching transients, calculate R_{ON} and R_{OFF} and switching time of the device. The switching time is the time

taken by device to switch its state after the application of the voltage (V_{ON} or V_{OFF}). Switching times are shown in Figure 46 (t_{ON} and t_{OFF}). A LabView program was formulated to achieve the switching time using the data obtained from the oscilloscope.

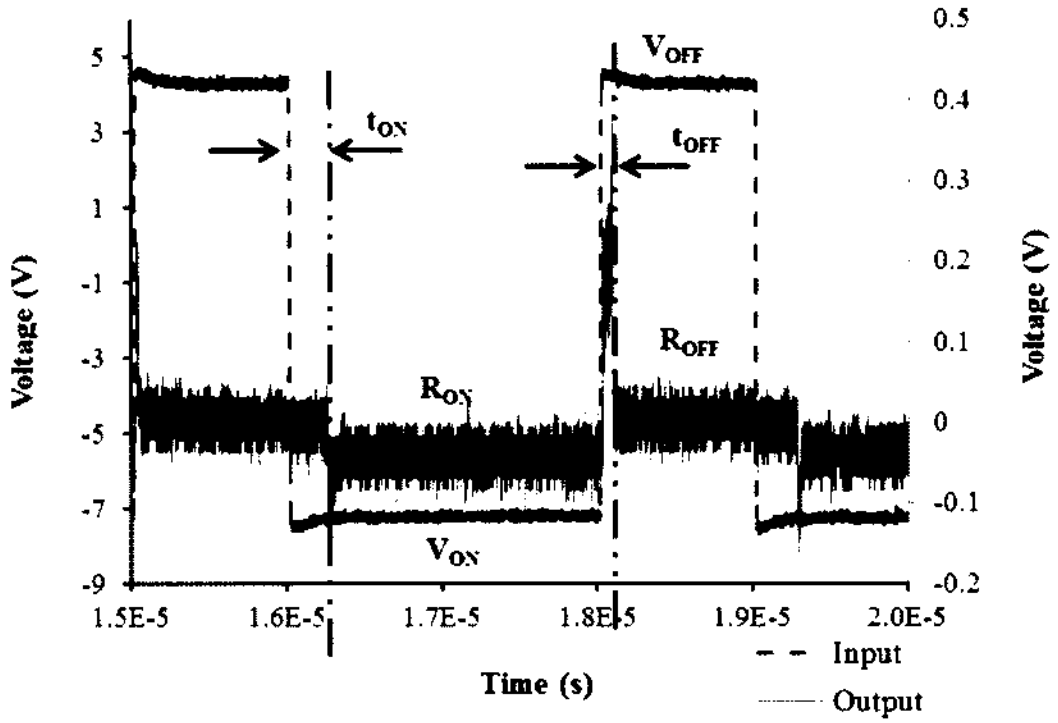


Figure 46. Output of a high speed amplifier along with measured input signal to the device.

This provides a similar situation to the setup in 3.2, where the accuracy of the R_{OFF} value is limited by the measurement setup.

3.4 Fast Endurance Test Measurement Setup

For high-performance switch applications, the desirable property is low R_{ON} (<1 kΩ) and high R_{OFF} (>1 GΩ) [7]. Although this significant resistance difference can be accurately measured with various instruments by changing the sensitivity manually, doing so would

be tedious and time consuming. Since it is very important to study the cycling endurance of the devices, an optimized way to collect cycling data at high speed is highly desirable. The vast difference in resistance value with ratios in excess of $>10^4$ renders the accurate and fast measurement a technical challenge.

To achieve accurate measurements of transient response and ON/OFF resistance in rapid cycling, a novel custom designed circuit was developed for the characterization of resistive switches. The objective is to characterize the non-volatile crossbar switch fabricated with Ta_2O_5 solid electrolyte at 1,000 cycles per second without sacrificing details and accuracy.

The basic approach of the design for the high speed endurance test circuit is schematically shown in Figure 47. The concept consists of three important components: a high speed amplifier, a high gain amplifier and a high-speed electronic single pole double throw (e-SPDT) switch. As shown in Figure 47, the current through the device is switched electronically between the paths, depending on the need to perform transient measurements (and low resistance measurements) or alternatively to perform high resistance measurements. The current during SET/RESET (write) and ON state (sense R_{ON}) is directed to a high speed amplifier and the current during OFF state (sense R_{OFF}) is directed to a high gain amplifier. A single cycle consists of SET, sense R_{ON}, RESET, sense R_{OFF}.

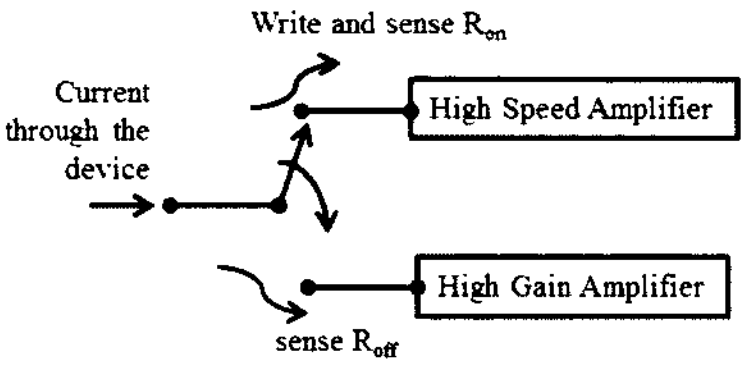


Figure 47. Basic schematic concept of high speed endurance test circuit.

High Speed Measurements

The high speed measurement setup for this high speed endurance test circuit is the same as that explained in section 3.3.

High Resistance Measurements

For the high resistance measurements, an opamp with very low noise and a decent gain bandwidth product was chosen. The high gain amplifier consists of a two stage amplifier to improve the speed. The gain of the first stage can be varied from 10^5 to 10^3 using various feedback resistors selectable by a mechanical switch. The second stage has a fixed gain of 10^2. The maximum total gain of the circuit is $5x10^7$ V/A. A simplified setup for the high gain amplifier is shown in Figure 48. With this gain, the lowest current that can be measured is 62.5 pA. That implies with this current, the largest R_{OFF} that can be measured with a target sense voltage of 50mV is 1.6 GΩ with a settling time of 100 μs.

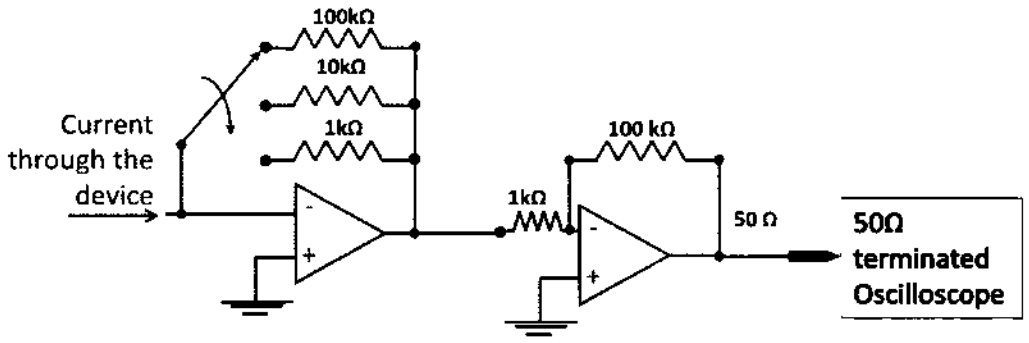


Figure 48. Schematic concept of high gain amplifier for high resistance measurements.

Current Compliance Circuit

The input probe configuration consists of the simple current compliance explained in section 3.3. Details of the probe setup along with resistance values are shown in Figure 49.

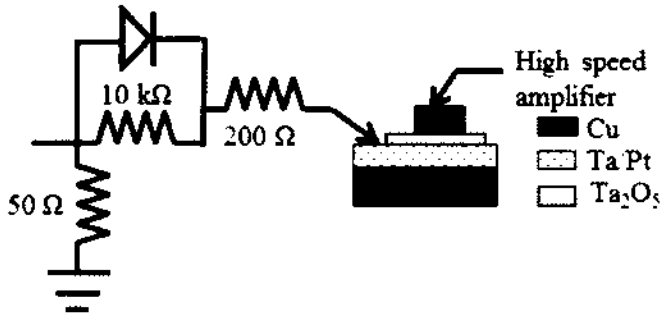


Figure 49. Detailed schematic of the probe setup used to apply voltage to the device.

Input Signal

The input signal to the device is illustrated in Figure 50. It has two main components, namely switching (writing) and sensing. The switching component consists of a high voltage pulse with short pulse width (500 ns in this initial demonstration (Figure 51)). The sense component consists of a low voltage pulse with longer pulse width (500 μs in

this demonstration case (Figure 51)), which is designed to allow the two stage amplifier described earlier to sense the current accurately. The low sense voltage also helps to reduce any stress on the device during the sense measurement. The pulse sequence of Figure 50 is produced by a programmable pulse generator. An electronic switch directs the switching transient and the sense signal following the SET to the high speed amplifier. The sense signal following the RESET is directed to the high gain and low noise amplifier. Thus, there are two separate output channels of this measurement setup: one from the high speed amplifier and the other from the high gain amplifier.

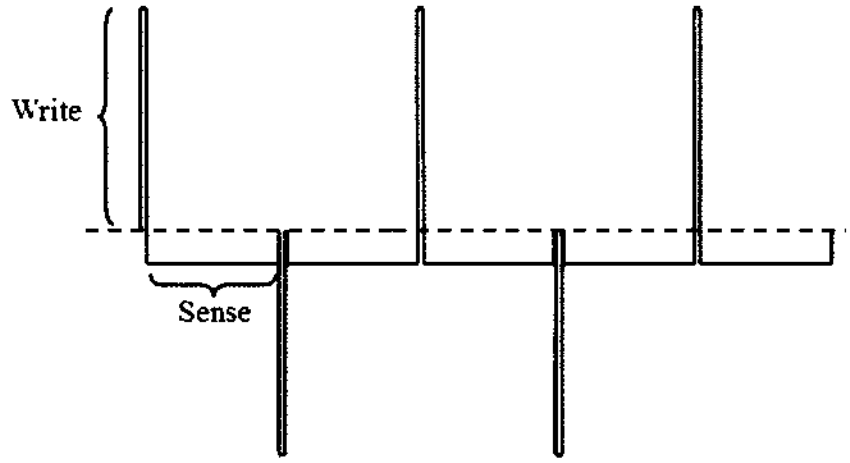


Figure 50. Input signal to the device with two distinct components for write and sense signals.

Electronic Switch

The circuit should be operated such that the high current is measured by the high speed amplifier and the low current is measured by the high gain amplifier. During SET and RESET, the current through the device should be measured by the high speed amplifier. Since the current is high for low resistance, sense for R_{ON} should also be measured by the

high speed amplifier. The only time the high gain amplifier should be used is during the high resistance measurement. The high-speed electronic single pole double throw (e-SPDT) switch mentioned earlier is responsible for switching the signal path from the high-speed amplifier to the high-gain amplifier and vice versa. The switch has one input, two outputs (S1 and S2) and one control line. The input of the switch is transferred to either one of the outputs depending on the electrical signal at the control line. Positive voltage above 2.4 V sends the input signal through S1, while maintaining S2 at ground. Similarly, when the voltage at the control line is below 0.4 V, the path of input is through S2 while S1 is ground. The path, which the e-SPDT switch will switch to, should depend on the input signal. Therefore, a pulse signal to the control line of the e-SPDT should be synchronized with the input signal. An example of such a signal is shown in Figure 51. It shows two pulses, one pulse to the control line of the switch (Switch) and another pulse fed to the device (Input). "Switch" is synchronized to "Input" such that high allows the signal through the device to the high gain amplifier. In the case of Figure 51, it is the sense signal after V_{OFF} (RESET), which is the high resistance state. Similarly, both the write signals (SET and RESET) and the sense signal after V_{ON} (SET) flow through the high speed amplifier.

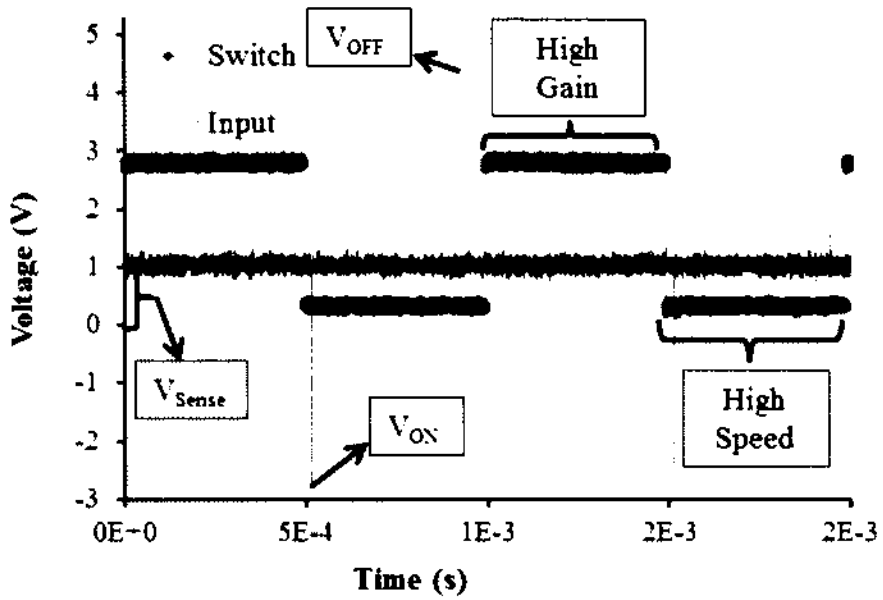


Figure 51. Oscilloscope measurement showing input voltage to the device (Input) and to the switch (Switch).

Once everything is positioned (Figure 52) the measurements are performed following the programed sequence. There are four signals that are measured: a) Input signal to the device (Input), b) Input signal to the control line of the switch (Switch), c) Output of the high gain amplifier (High Gain) and d) Output of the high speed amplifier (High Speed). One such measurement is shown in Figure 53. The current through the device (measured by High Gain) preceding V_{ON} is very small indicating high R_{OFF}. After the V_{ON} pulse, the current is measured using the high speed amplifier output. The output of the "High Speed" following the V_{ON} pulse is high indicating switching ON of the device. In Figure 53 it can be seen that the "High Gain" is always low indicating high resistance after V_{OFF}. "High Speed" after V_{ON} pulse is always high indicating low resistance after V_{ON}. These measurements were taken to calculate the R_{ON} and R_{OFF} values. It is noteworthy that the

low and high resistances were measured by two different amplifiers within 1 ms. Thus accurate R_{ON} and R_{OFF} values for a single cycle can be obtained within 1 ms.

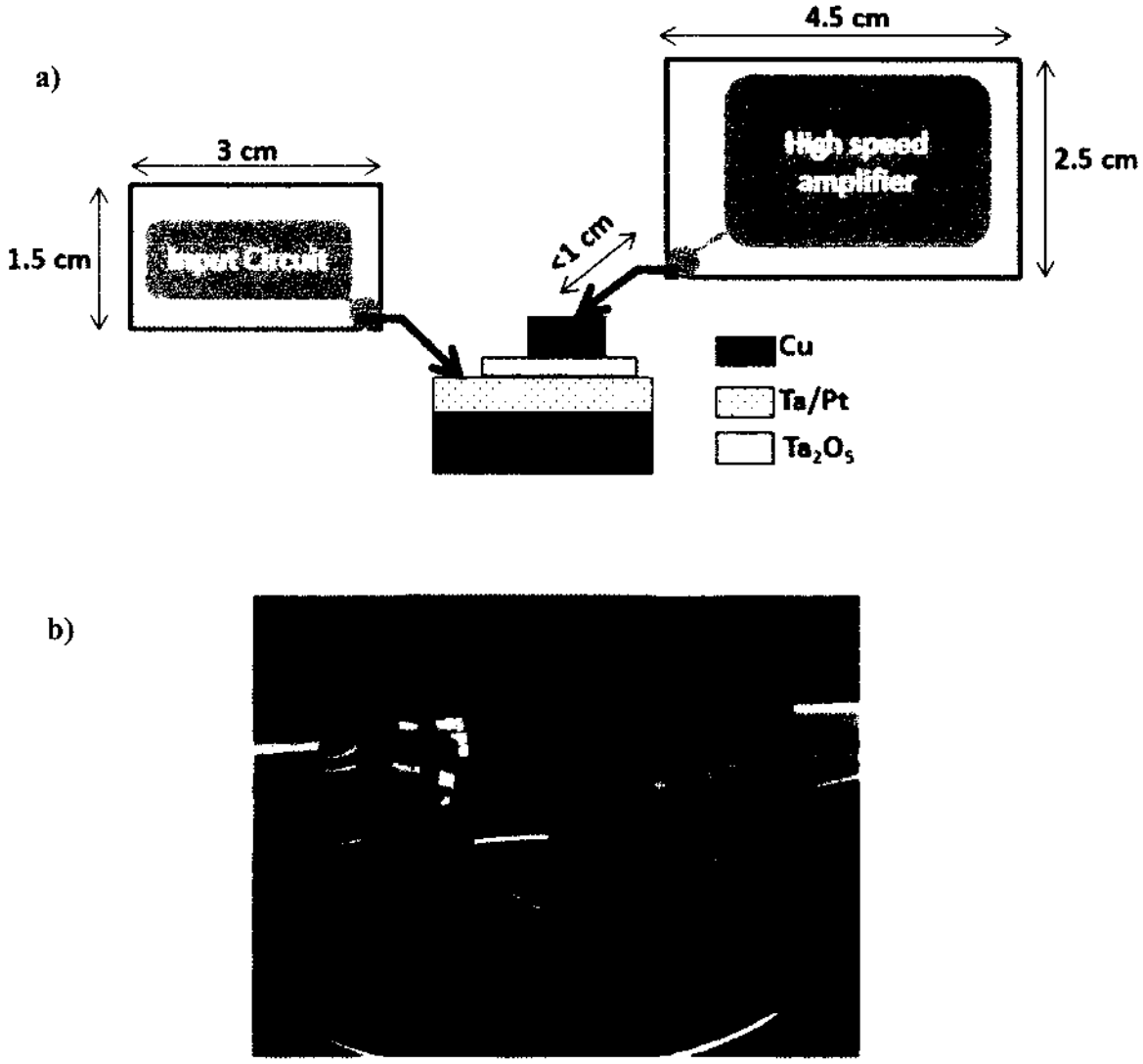


Figure 52. a) Schematic of the Fast Endurance Test Measurement setup showing the size and placement of the circuits and the probe needles b) photographic image showing the actual setup of the probes built for measurement.

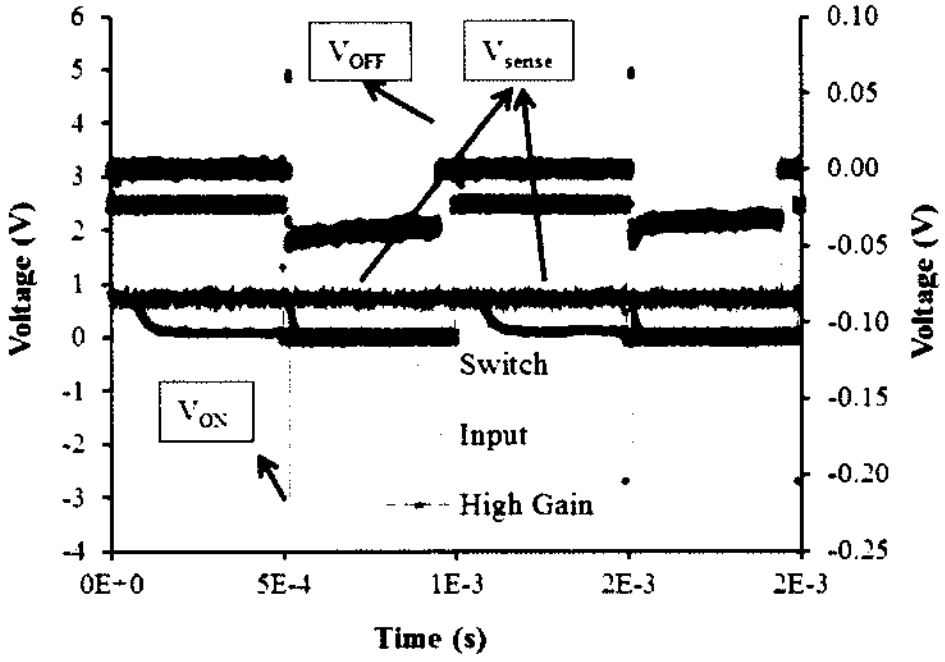


Figure 53. Output voltages measured at different time frames.

3.5 Endurance Measurement Setup with Current Compliance Circuit

As previously mentioned in the literature review section (1.3), the resistive switch community has been battling the "current overshoot" problem for a long time. The current overshoot is especially high and detrimental for devices with higher R_{ON}/R_{OFF} ratios. As shown in Figure 40, the $Pt/Ta_2O_5/Cu$ non-volatile crossbar switching devices in this study exhibit a high R_{ON}/R_{OFF} ratio. In order to enable reliable testing of these devices, it is important to find a solution to this overshoot problem. To meet this objective, another new custom circuit was designed to achieve as low current overshoot as possible.

The basic conceptual idea of the designed circuit is shown in Figure 54; a "Sensing Resistor" in series with the Device under Test (DUT) is used to monitor the current. The

voltage across the "Sensing Resistor" is amplified and applied to the other terminal of the DUT. The amplification factor is chosen such that when the DUT is in high resistance state, the voltage applied to the other terminal is low enough that the voltage across the DUT is not affected. However, when the DUT resistance drops, the voltage drop across the DUT is essentially zero.

Although this cancellation scheme is very fast, it is not instantaneous. To suppress the very early transient, an inductor is placed in series with the DUT to slow down the change just enough for the circuit to be effective while still maintaining a fast response. The combination of the inductor and the "feed forward" circuit completely eliminates the current overshoot. The proper combination of the "sensing resistor" value and the amplification factor allows the current compliance to be set to any value needed.

A diode is placed in the "feed forward" circuit such that the current is limited only for the negative input voltage. Thus, the circuit will limit the current during SET and allow high current during RESET.

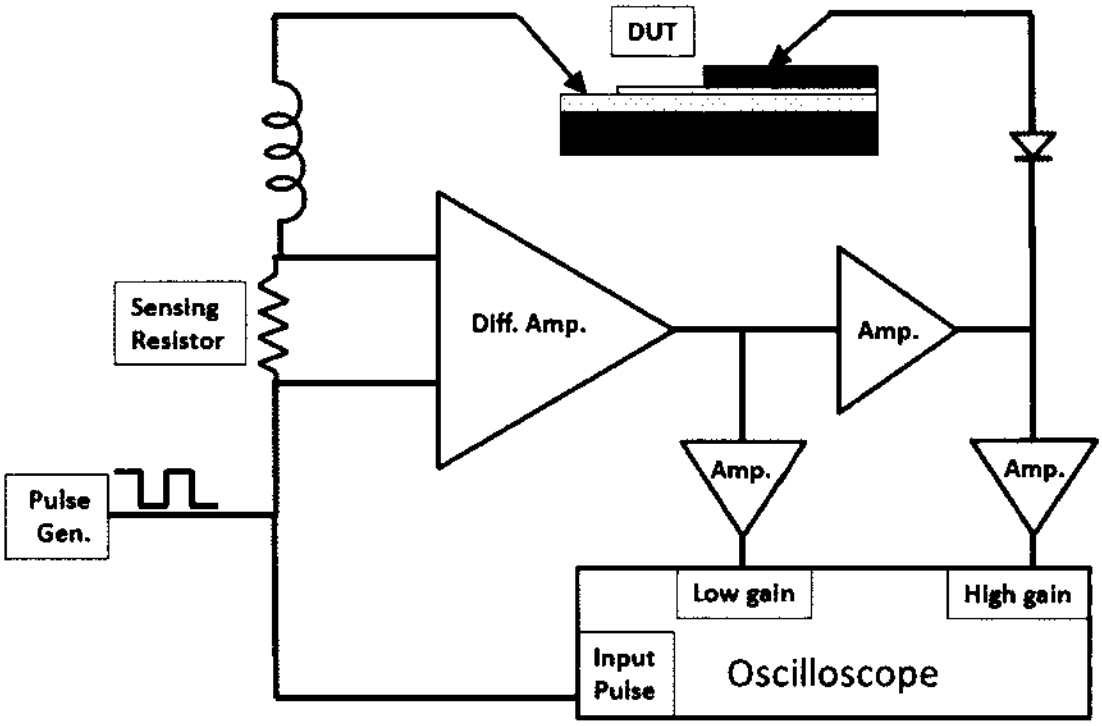


Figure 54. Basic schematic concept of the current compliance circuit.

As shown in Figure 54, this special circuit has built-in ports to monitor the current through buffer amplifiers. The channel designated as "Low Gain" has a gain of 8.4×10^3 V/A to monitor the low resistance state. The channel "High Gain" has a gain of 44.2×10^3 V/A to monitor the high resistance state. The compliance circuit needs to be as close to the device as possible to minimize noise and any measurement artifacts (Figure 55). To accomplish that, the whole circuit is put together on a very compact surface mount PCB and the probe tip for measurement setup is mounted directly on the circuit board.

Figure 55. Photograph of the actual Measurement setup along with the device under test.

CHAPTER 4

RESULTS AND DISCUSSIONS

This chapter covers the measurements obtained by using the various special experimental setups mentioned in chapter 3. The results and the analysis of the data are then discussed in detail. The anomalies during SET and RESET from one cycle to another and one device to another have been investigated. During the measurements, it was also found that the device switching depends heavily on the specific measurement setups. The analysis and discussion in this chapter provide a better understanding of why these different measurement circuits were developed for this study.

4.1 Transient Measurements

In order to study the transient current voltage properties of the device, the high speed current amplifier, described in the earlier section, is used to SET the device. A voltage pulse of -3 V/1 μs was used. The transient response of the device during the set process is shown in Figure 56 a). It can be seen that the current peaks before it reaches a stable R_{ON} state. To eliminate the possibility that this peak is the current spike due to the parasitic capacitance in the circuit, the same measurement on the identical device was measured while it is in its ON state as shown in Figure 56 b). The absence of a current spike proves that the spike seen in Figure 56 a) is a real device switching phenomenon. The nature and origin of the current peak during switching is discussed in a later section.

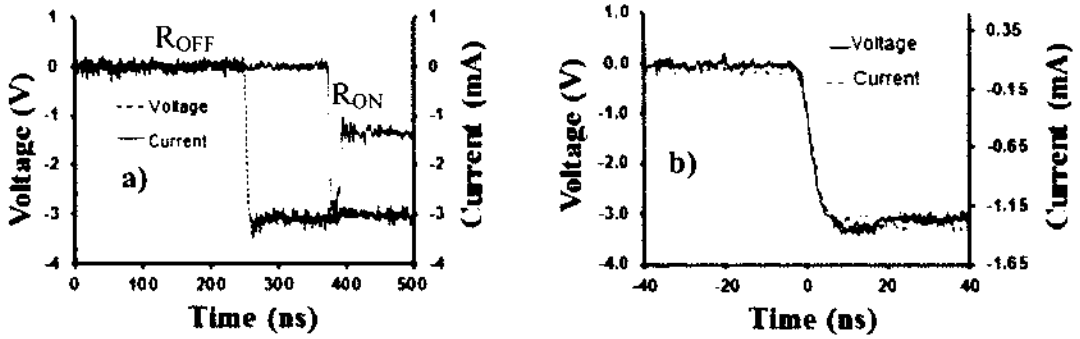


Figure 56. a) Applied voltage and current vs. time illustrating the high speed capabilities of our custom measurement circuit. The Current measurement error is about ± 0.5 mA and the voltage error is about 0.25 V. b) Transient current response during switching event from high to low resistance state. The Current error for this measurement is about ± 0.5 mA and for voltage the error is about ±0.25 V.

This circuit was further used to obtain accurate SET and RESET switching time of the device. The data shown in Figure 56 b) reveal that the amplifier setup can follow a 4 ns rise and fall time without any problem. This result suggests that the switching time obtained from the data is accurate within the range of few ns. Data obtained by analyzing 150 cycles are depicted in Figure 57.

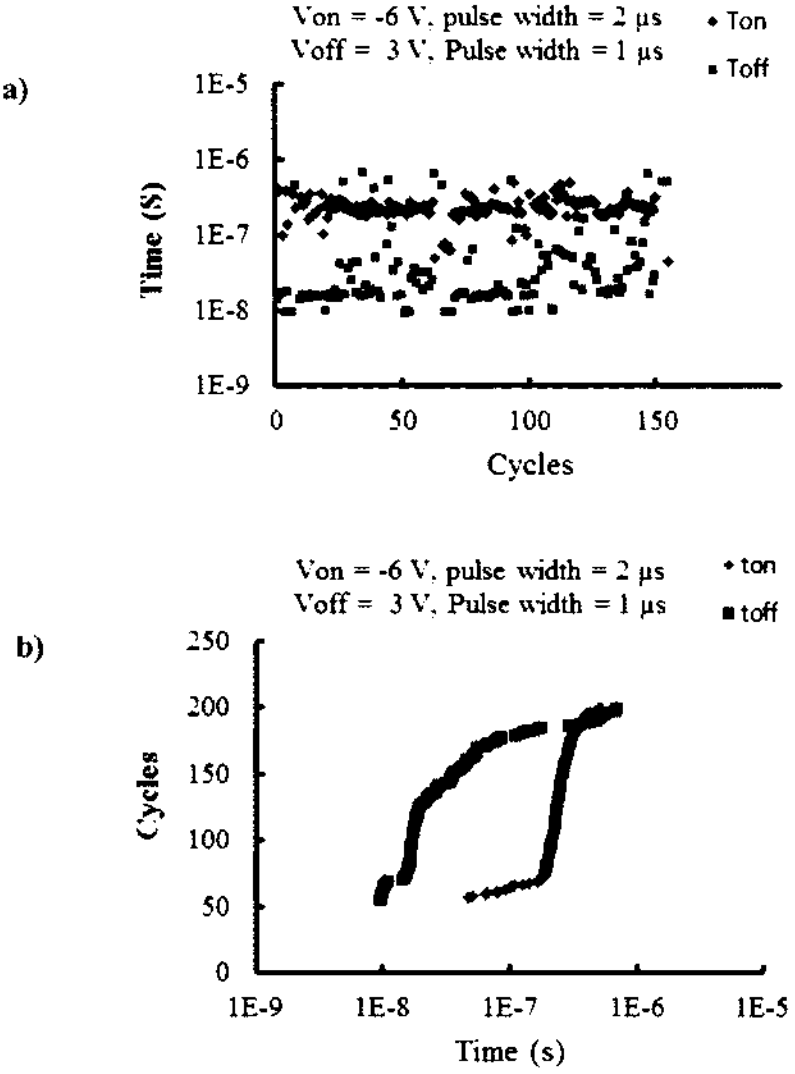


Figure 57. a) Switching time achieved for Sample W and b) distribution of switching time for 200 cycles.

The same high speed circuit was again used to analyze the endurance of the device. Consecutive ON and OFF voltages are applied to the device (V_{ON} = -6 V/500 ns, V_{OFF}= 2.5 V/500 ns). The current with labels R_{OFF} and R_{ON} was used to calculate the values for R_{ON} and R_{OFF}. The data obtained for 60,000 cycles are shown in Figure 58. The values of R_{OFF} obtained in Figure 58 are limited by the low gain of the high speed circuit. These results clearly demonstrate the necessity of the high gain circuit for the sensing purpose.

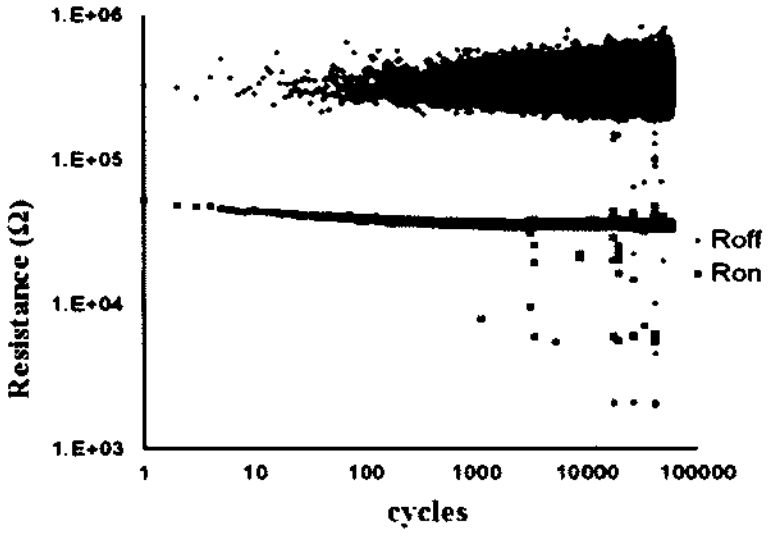


Figure 58. Data obtained from switching the memristive device for up to 60000 switching cycles using a high speed amplifier for Sample A.

This transient measurement revealed the presence of a peak during SET, which is otherwise not detectable by other slow measurement techniques. This transient measurement is also capable of obtaining fast switching times in the range of a few nano seconds (ns). The only measurement that is not accurate using this measurement setup is the value of R_{OFF}.

4.2 High Speed Endurance Test Circuit

To mend the shortcoming of the previous measurement technique and to achieve accurate R_{OFF} values along with the accurate transient, the improved newly designed switching measurement circuit discussed in section 3.4 was used. The Data shown in Figure 59 was obtained by using the complete high speed/high gain circuit mentioned in section 3.4 and Figure 47. Values of R_{ON} were obtained using the output from the high speed circuit, capable of measuring high current. R_{OFF} was obtained from the output of the high gain circuit.

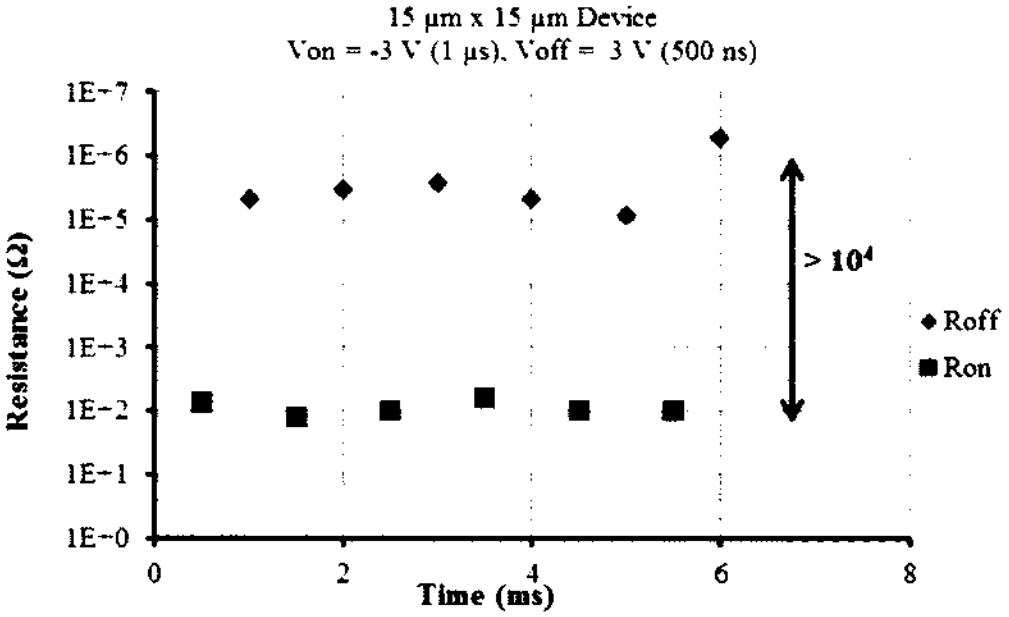


Figure 59. Data obtained by using the specially designed high speed/ high gain circuit. R_{on} was obtained from the output of the high speed circuit and R_{off} from the high gain circuit (Sample A).

For the particular data shown in Figure 59, a voltage of -3 V with a pulse width of 1μs was used to switch the device ON and subsequently a voltage of 3 V with a pulse width of 500 ns was used to switch the device OFF. In between each of the switching states, a sense voltage of 750 mV with pulse width of 500 μs was used to sense the state of the device. It is apparent from Figure 59 that a huge difference in the resistance values can be measured within the short time frame of 1 ms. The data suggests that the basic endurance requirement of 10^5 switching cycles for the high performance switch can be measured within a few minutes by using this novel technique.

This custom circuit is therefore capable of measuring current transients during switching. This circuit can also measure very low currents through the high resistance state of the

device up to 1.6 GΩ. High speed cycling for accurate endurance can therefore be achieved simultaneously.

4.3 Ohmic and Non-Ohmic ON State Characteristics

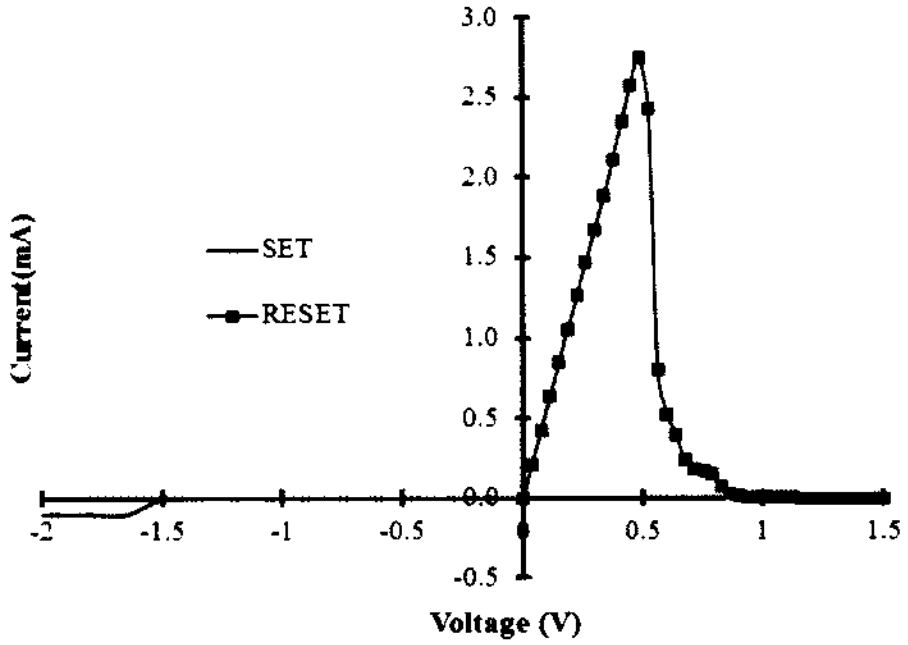


Figure 60. SET and RESET sweep of a device with structure similar to the one shown in Figure 35.

Typical SET and RESET sweeps are shown in Figure 60. The voltage is applied on the bottom Pt electrode and the top Cu electrode is grounded. The voltage was swept across the device using a conventional parametric analyzer. The device was SET at -1.5 V by using a current compliance of 100 μA. RESET was achieved by using a positive voltage sweep without current compliance. Typically, RESET was observed at ~0.5 V with a rather large RESET current of 2.75 mA. As is shown, these devices result in nominal switching consistent with literature values [8, 36].

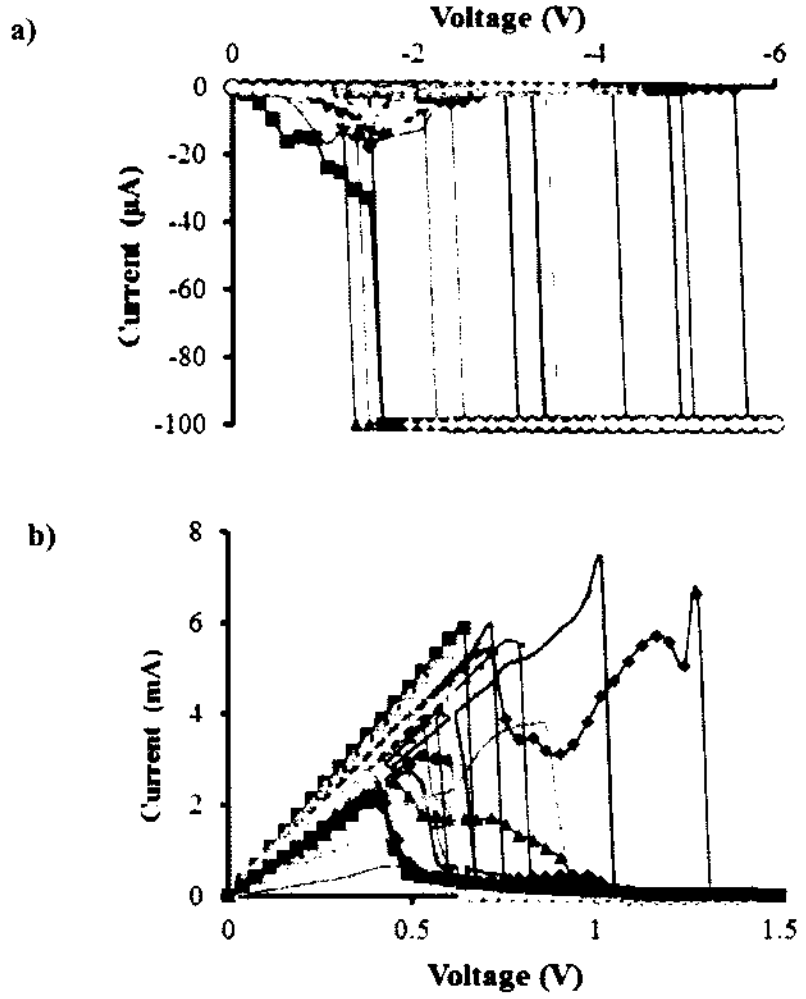


Figure 61. 20 cycles of a) SET and b) RESET characteristics of devices fabricated using the multiple spacer technique (Sample W).

In Figure 61 a) and b) 20 cycles of SET and RESET are displayed. One can see that the devices switch ON and OFF but the variability in the switching is very high. Different cycles have a different SET voltage and a different OFF voltage. The ON and OFF resistances change frequently as well. One of the most intriguing data is the variation in the characteristics of the ON state. The devices were cycled through SET and RESET numerous times. Figure 62 illustrates four of these characteristic cycles, which prove

most instructive. Figure 62 a) shows the SET process with current compliance of 150 μA. Figure 62 b) shows the RESET process for the same cycles displayed in Figure 62 a) (nominally referred to as cycles W, X, Y, and Z). An examination of RESET for cycles W, X and Y revealed linear current voltage relationships (Ohmic). However, cycle Z exhibits a non-ohmic RESET. This is more easily observed in subsequent resistance plots during ON state (Figure 62 c). This further confirms and proves that the SET resistances of cycle W, X and Y are indeed ohmic while the SET resistance of cycle Z is not ohmic.

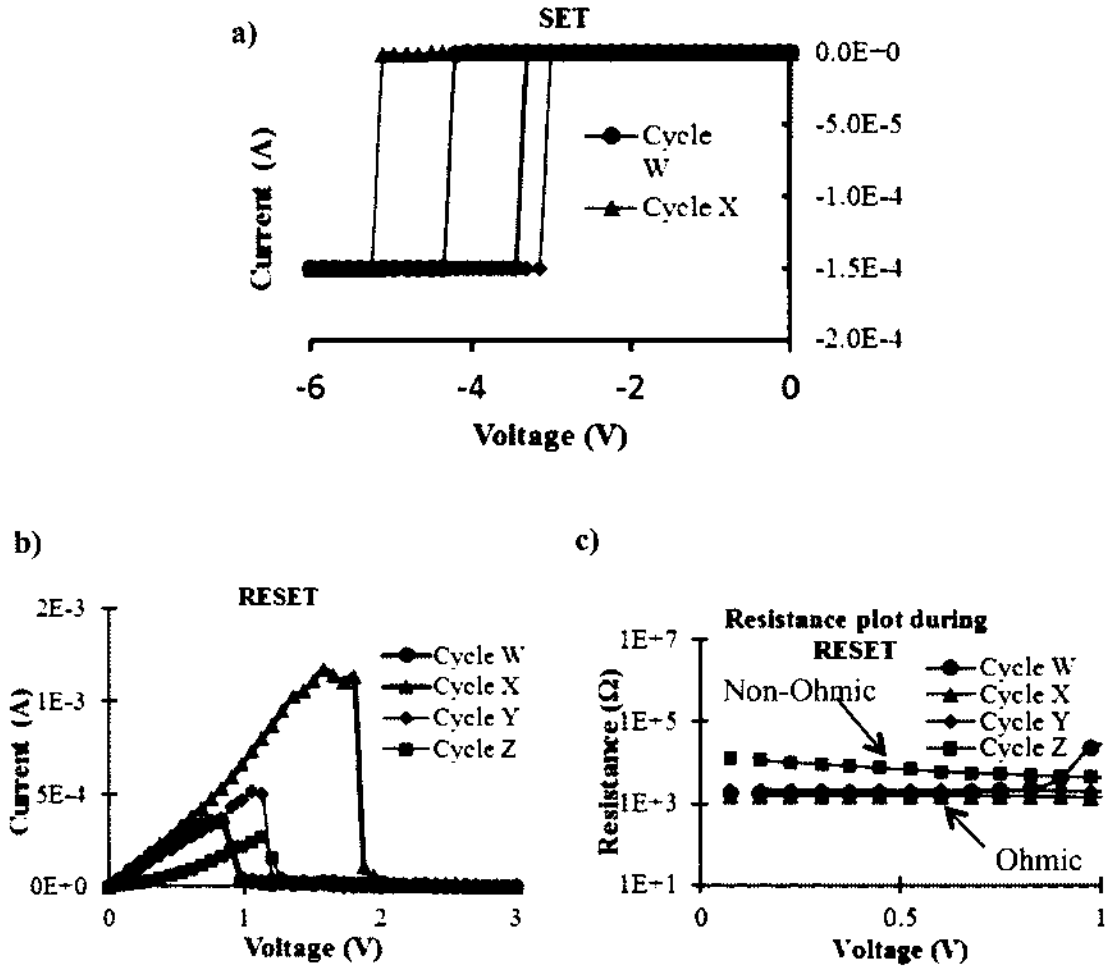


Figure 62. a) SET sweep, b) Current plot during RESET and c) Resistance plot during RESET.

Similar Non-Ohmic states are repeatedly obtained when the devices undergo a partial, or incomplete, RESET. Figure 63 shows one such instance where a partial breaking of the filament takes place in the "First Sweep". When a "Second Sweep" is performed on the same device immediately after the "First Sweep," the resistance plot suddenly displays Non-Ohmic conduction. The device further switches to a higher resistance level when a higher voltage is applied.

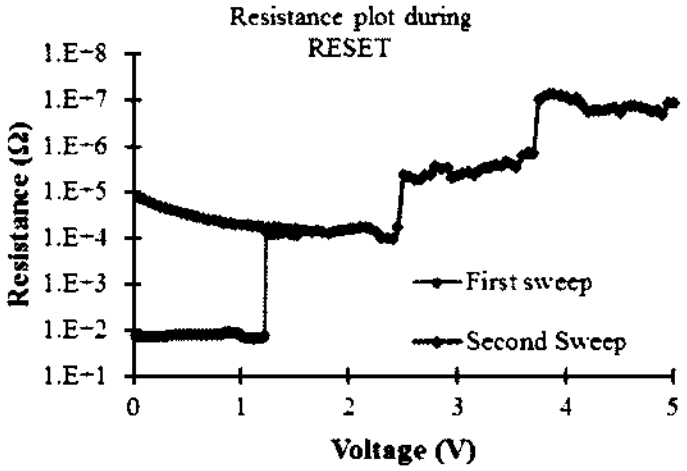


Figure 63. Resistance voltage plot of RESET sweep.

The similarities between the "Second Sweep" in Figure 63 and in Figure 62 c) suggest similar mechanisms of Non-Ohmic conduction within the voltage range of 1 V. The only difference between the first case (Figure 62) and the second case (Figure 63) stems from the fact that the polarities of the voltage sweep applied before obtaining the Non-Ohmic states are opposite. The Non-Ohmic Cycle "Z" of Figure 62 c) is obtained after SET sweep, which is negative in polarity. However, the Non-Ohmic "Second Sweep" Figure 63 is observed after the "First Sweep" which is positive. Therefore, the trigger that causes

the Non-Ohmic conduction does not depend on polarity. Joule heating, which is not polarity dependent, has been claimed to be the primary reason for the filament dissolution [50]. In the case of RESET one can see the current getting high enough to cause joule heating. However, in the case of SET, the current is being limited to a fixed low value. So why would Joule heating sporadically occur?

This raises the question of how much one can rely on the current-voltage plot. It is a known fact that the current compliance of a parametric analyzer has a finite response time, during which the device is subjected to an unregulated high current. This current overshoot is not captured by the slower measurements supported by the parametric analyzer but may be the source of the joule heating which triggers the dissolution of the metal filament during SET. Using a high speed amplifier, current overshoot is also observed for a simple compliance circuit comprised of a current limiting resistor and a diode [51] (section 4.1). Similarly, the overshoot has also been reported in compliance circuits as simple as a series resistance due to the parasitic capacitance [82, 83].

4.4 Current Compliance Circuit

Proof of Current Overshoot Due to Compliance Circuit

Figure 56 a) shows a peak in the current during the SET process before the current stabilizes to a fixed value. This current peak shown in the plotted data of Figure 56 a) is not a measurement artifact as in Figure 56 b). In fact, it shows that the current measurement perfectly follows the input voltage curve without any distortion up to pulse rise time of 4 ns. Therefore, the peak has to be a real device switching phenomena.

Using a spice model for the measurement setup and the current limiting circuit, it is confirmed that the observed peak is due to the capacitance associated with the current

limiting circuitry and the capacitance associated with the device itself. The circuit used for the spice simulation is shown in Figure 64 b) along with the simulation output in Figure 64 c).

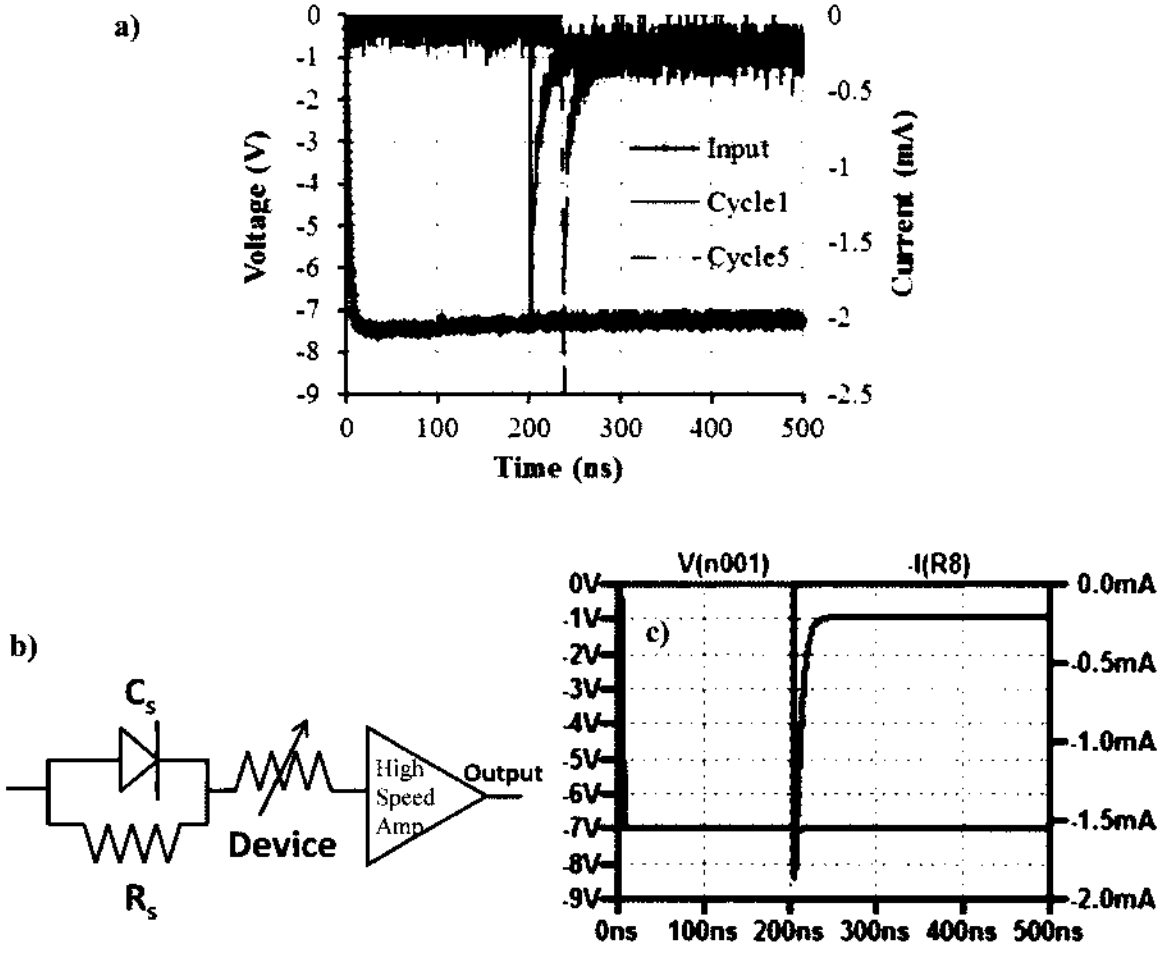


Figure 64. a) Measured applied voltage and current through the device during SET operation using the current limiting circuit in Figure 43 and the high speed amplifier (Figure 45) b) circuit component used to simulate current through the device and c) results obtained from SPICE simulation.

Why is current overshoot a problem?

From section 4.3, the ON state and the following OFF state depend significantly on the current flowing during the SET process. This overshoot seen in Figure 64 plays a vital role in device performance. This current overshoot may lead to premature breaking of the filament during SET or may lead to high RESET current during RESET. This high RESET current then gives rise to joule heating within the device. Figure 65 shows the effects of heating due to multiple SET-RESET cycles. Figure 65 a) shows a virgin device which has not gone through device switching. Figure 65 b) and c) shows the heating effects because of numerous switching cycles. Similar results were observed and attributed to joule heating during switching [106, 107]. Therefore, reliable current control during SET process is important for a good control over the ON and OFF state of a device.

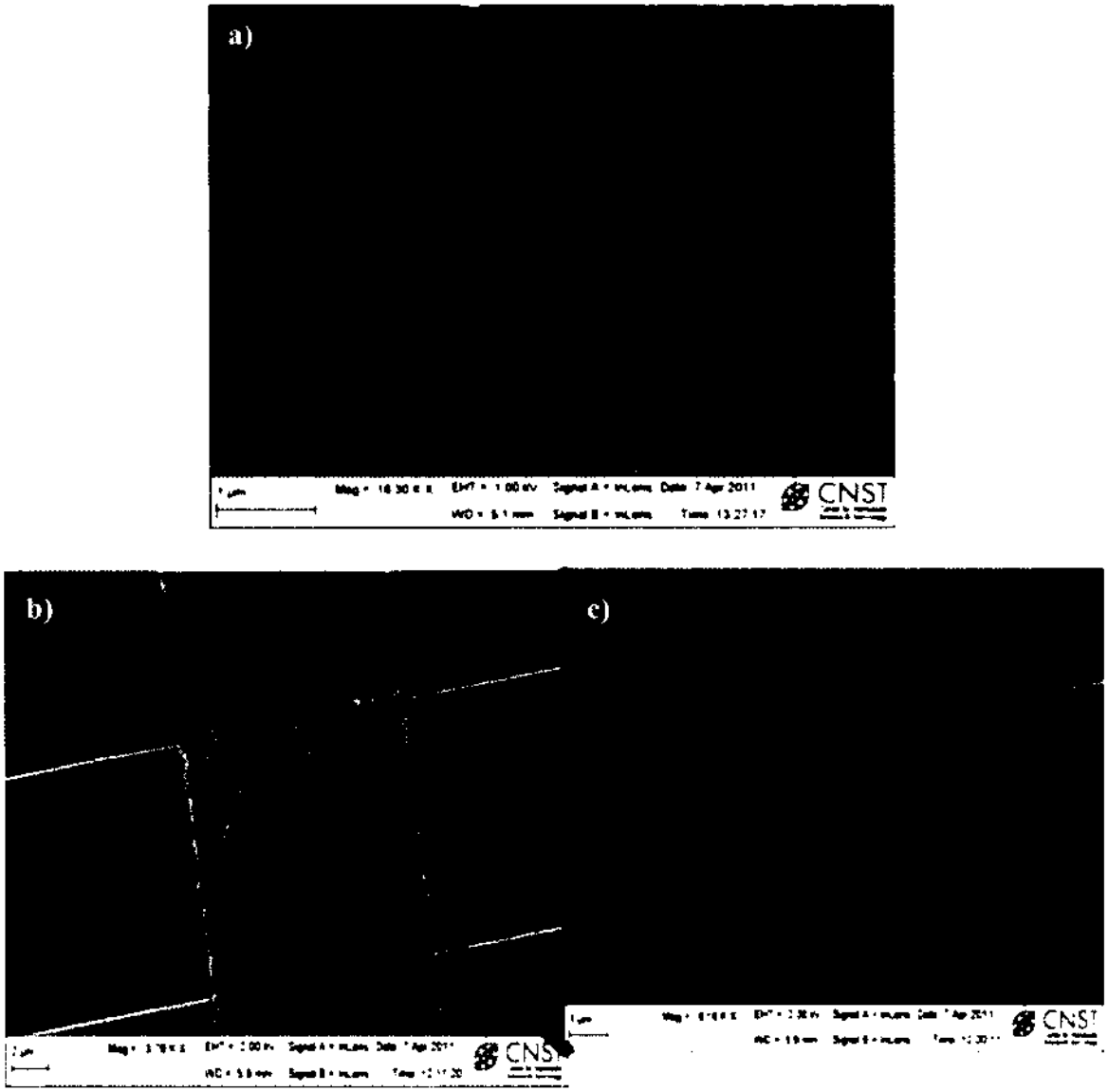


Figure 65. SEM planar view images of a representative cross bar switching device after multiple SET and RESET cycles (Device A).

In order to gain good control over the current compliance, the circuit described in section 3.5 is put together on a surface mount PCB board. Figure 66 plots the output of the "Low Gain" amplifier shown in Figure 54. The device switches ON with a current compliance given by ~74 mV in the "Low Gain" amplifier output. With the gain of 3.7×10^3 V/A, the current through the device is ~20 μA. The inset shows another SET process with 2×10^9

samples/s. This example shows successful control of current compliance with no significant overshoot within the limit of the measurement, which is 500 ps.

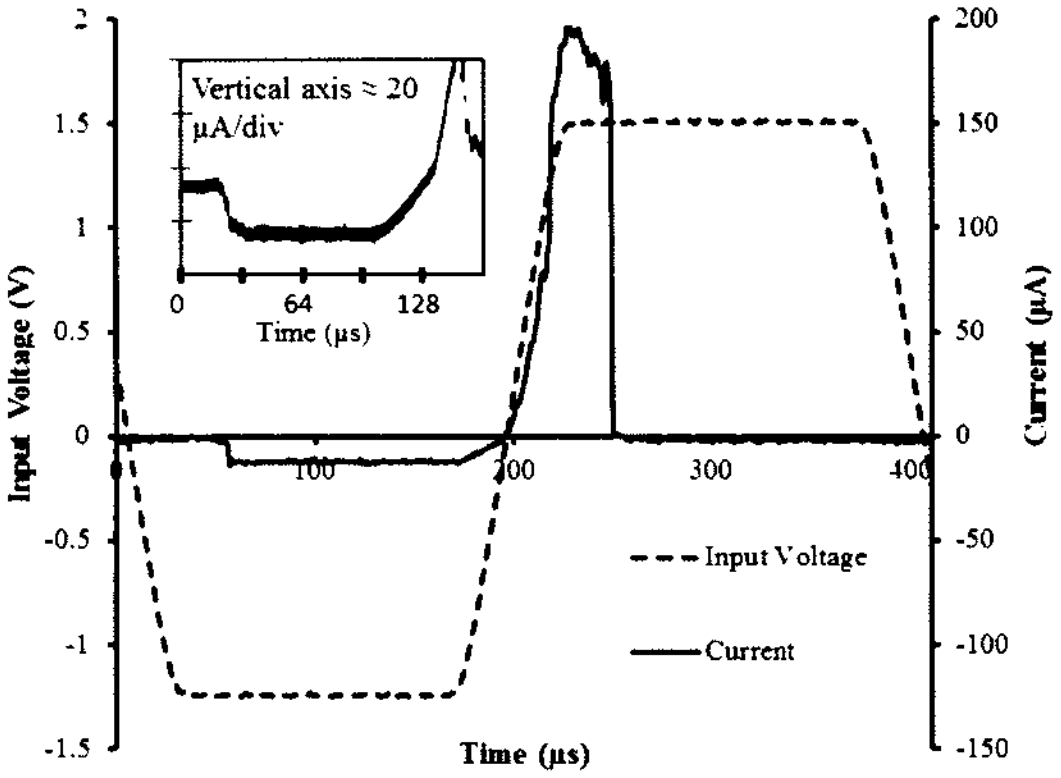


Figure 66. Plot of Input Voltage and current measurement obtained from the "Low Gain" amplifier shown in Figure 47. The Inset shows the amplifier output during SET operation with a higher sampling number of $2x10^9$ samples/s. The device was SET using -1.25 V and RESET using 1.5 V.

In order to verify the operation of the circuit, Spice simulations have been performed. The Current through the device is simulated using the models of the components used to build the compliance circuit. The simulated current is shown in Figure 67 a) and the experimental measurement obtained is given in Figure 67 b). The excellent correlation between the data simulated with the Spice model and the actual experimental measurements displayed in Figure 67 assures good reliability of the circuit.

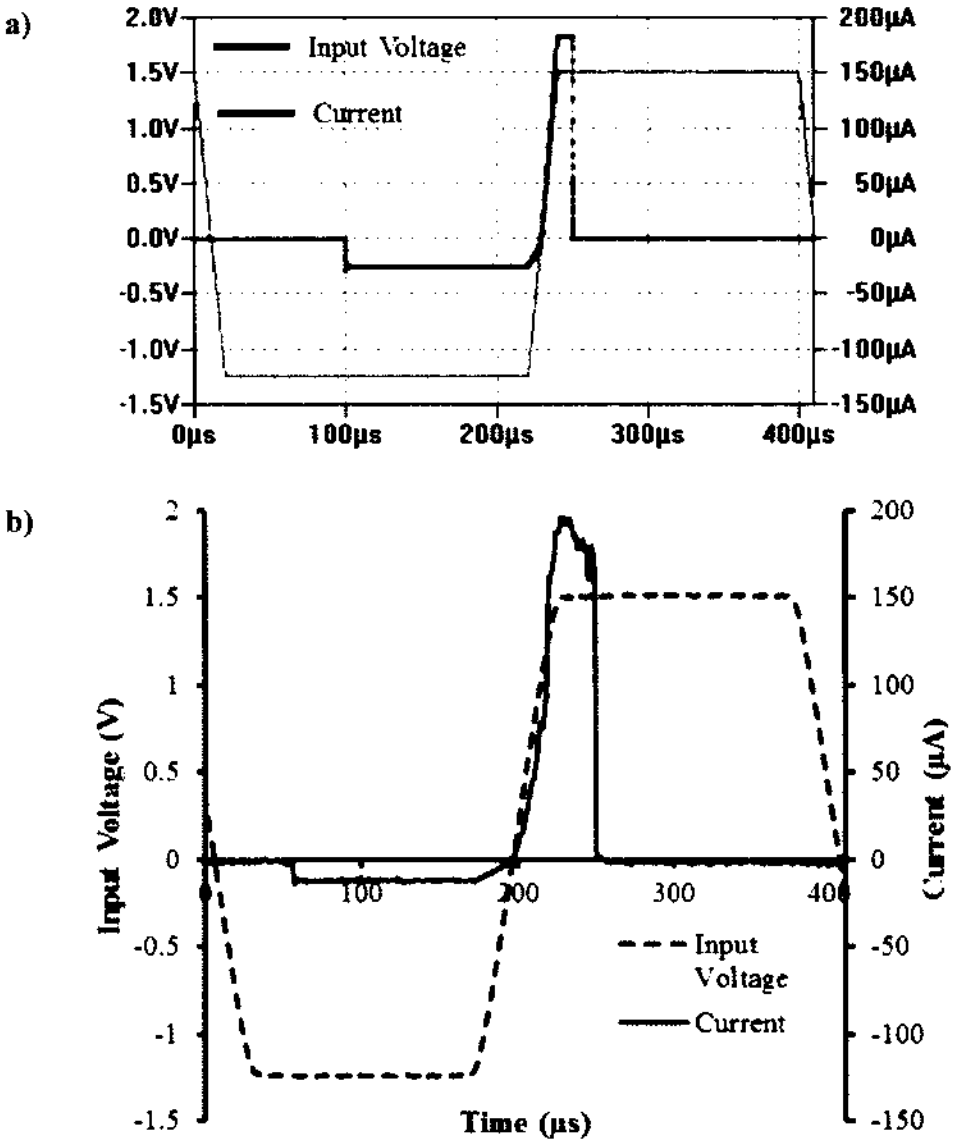


Figure 67. a) Simulated current and b) Measured current through the device during switching using current compliance circuit.

Figure 68 a) and b) plot the achieved SET and RESET current respectively for Sample W with the structure shown in Figure 35. Figure 68 a) clearly indicates that the RESET current is below 40 µA for 10 cycles. This is significant compared to the RESET current of the devices being SET by using a parameter analyzer shown in Figure 60. The

resistance data versus cycles in Figure 68 b) further prove that the R_{ON} and R_{OFF} ratio is more than 10^4 with such a small SET and RESET current.

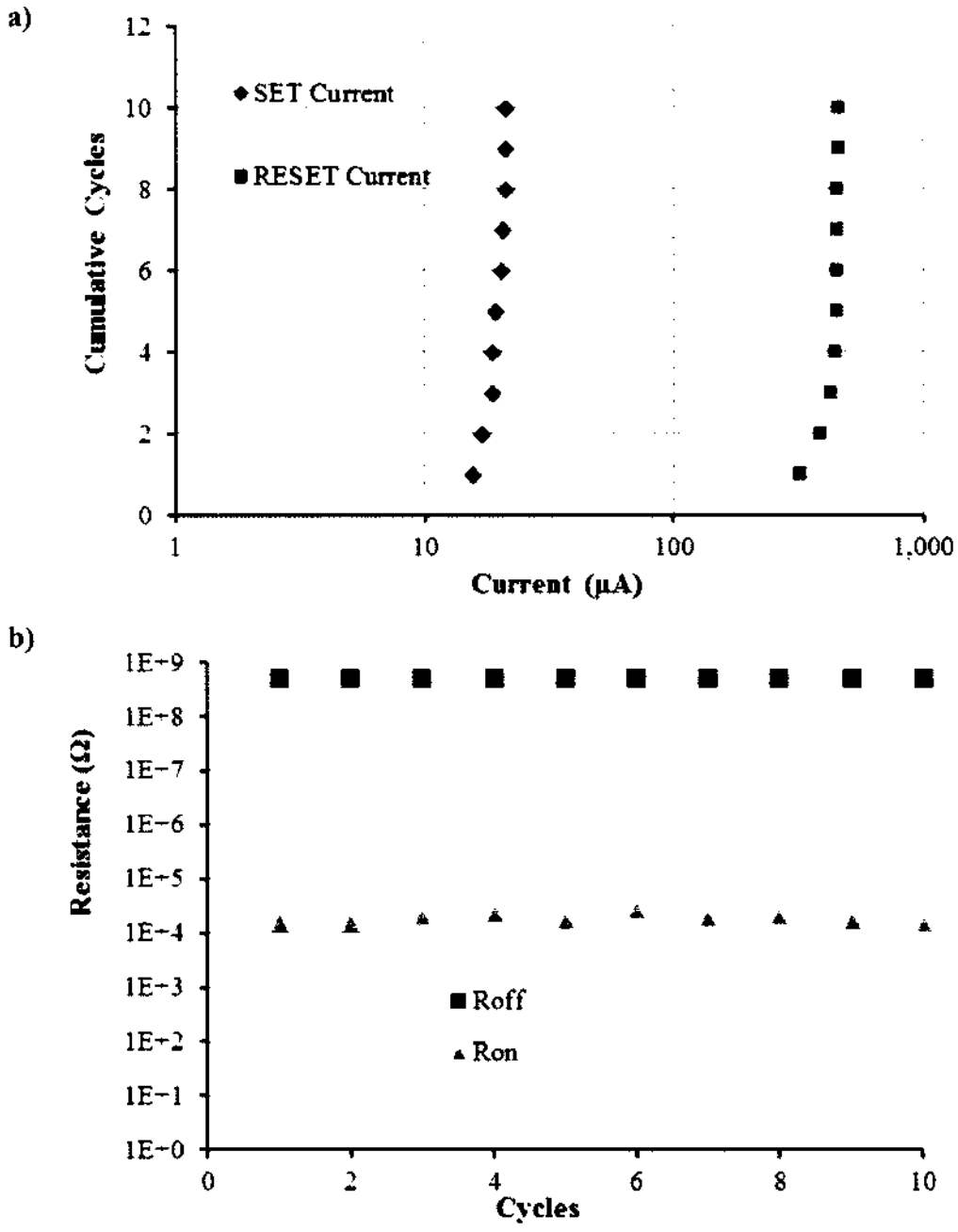


Figure 68. a) Plot of SET and RESET current distribution and b) R_{ON} and R_{OFF} for 10 cycles using the current compliance circuit (Device W).

To improve the variations in the ON state characteristics and to lower the RESET current, the current overshoot during SET has to be minimized significantly. Thus the circuit delivers current control within 20 μA with no overshoot within the range of 500 ps. The RESET current for devices were less than <40 μA, which is much lower compared to the RESET current achieved by using the current compliance of a conventional parameter analyzer (200 μA to 2 mA). In addition a high R_{ON}/R_{OFF} ratio of greater than $>10^4$ is also attained. Although the number of cycles presented is few, the data does suggest that the external current compliance circuit has the potential to improve the performance of resistive switches.

4.5 Discussions on Devices with Constricted Cu Area (Device W)

The SET current, the RESET current, R_{ON} and R_{OFF} measurements using the novel current compliance circuit for the Device W (with constricted Cu area) are shown in Figure 68 a) and b). Figure 68 a) clearly shows that the RESET current (< 200 μA) is still an order of magnitude higher than the SET current (> 20 μA). Ideally, it is preferred to have a lower RESET current to minimize the power consumption of the device. The device has one filament as illustrated in Figure 36 c) but is the filament uniform? When we closely look at the structure shown in Figure 36 we can see that the potential nucleation sites for the Cu metal filament at the Pt inert electrode are still plenty because of the large Pt electrode area. For this reason during the initial switching cycles the filament will have a structure shown in Figure 69 a), but after few cycles the filament might widen at the inert Pt electrode as shown in Figure 69 b). Therefore, there is a huge possibility of variability in the filament size from cycle to cycle. This growing expansion

of the filament size may be the reason behind the higher RESET current. The thicker the filament the larger will be the power required to disrupt and to dissolve it. One of the best solutions for this problem is restricting the Cu nucleation sites at the Pt inert electrode. This can be achieved by constricting the Pt inert electrode area in the device.

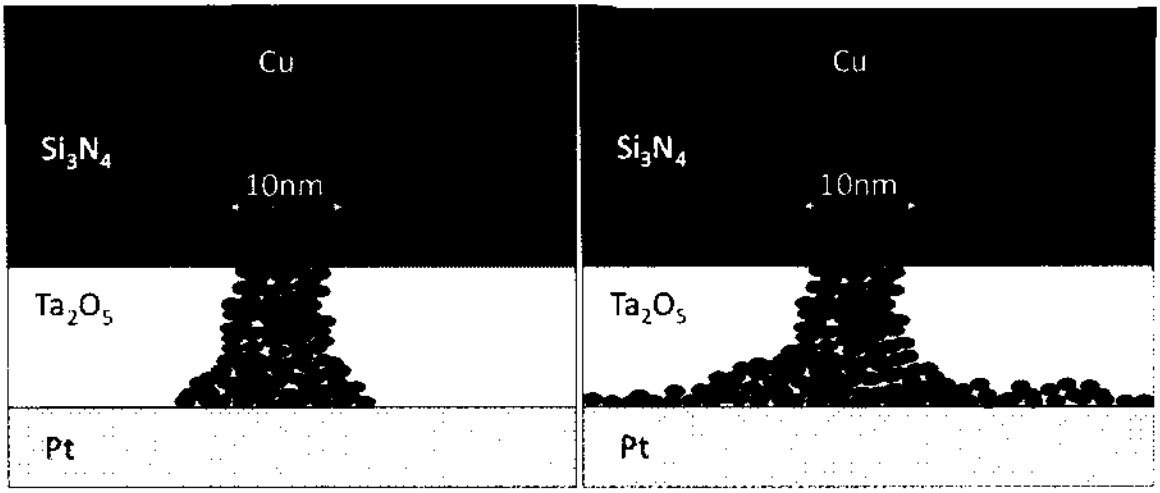


Figure 69. Plausible filament shape after a) few cycles and b) numerous cycles of SET and RESET.

4.6 Discussions on Devices with Constricted Pt Area (Device X)

The next device was fabricated with a constricted inert Pt electrode area to minimize the Cu nucleation sites on the Pt electrode. The multiple spacer technique, developed for Device W, was used to make the devices (Figure 70) where the SET and RESET current distribution is plotted Figure 71 a). In this case, the Cu ions have only a very limited area to nucleate which will considerably narrow the sites for metal filament formation.

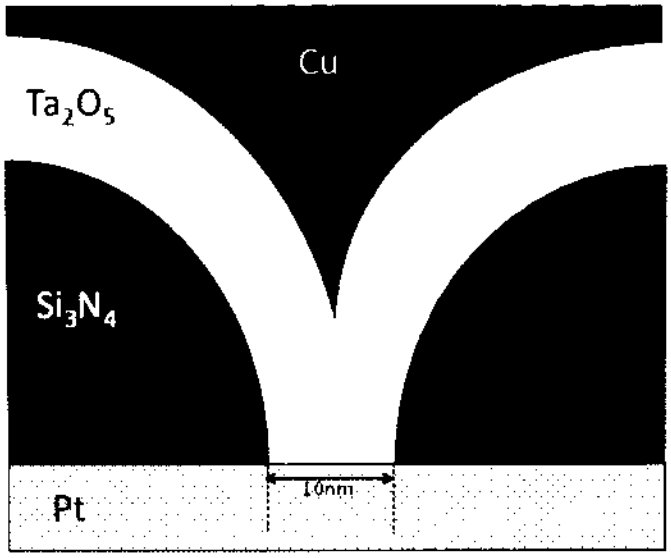


Figure 70. Schematic of fabricated device with constricted Pt area (Device X).

The current compliance circuit was used to measure the SET current, the RESET current, and R_{ON} and R_{OFF}. The results are displayed in Figure 71. The RESET current for Device X has values 50 μA to 130 μA. The RESET currents are low but the distribution is very poor. Similarly, the R_{ON} values show lot of variation from cycle to cycle. These are the preliminary results showing 15 cycles. These variations within 15 cycles suggest that the structure is not as ideal as expected. However, in the future more switching cycling tests are required for better statistics.

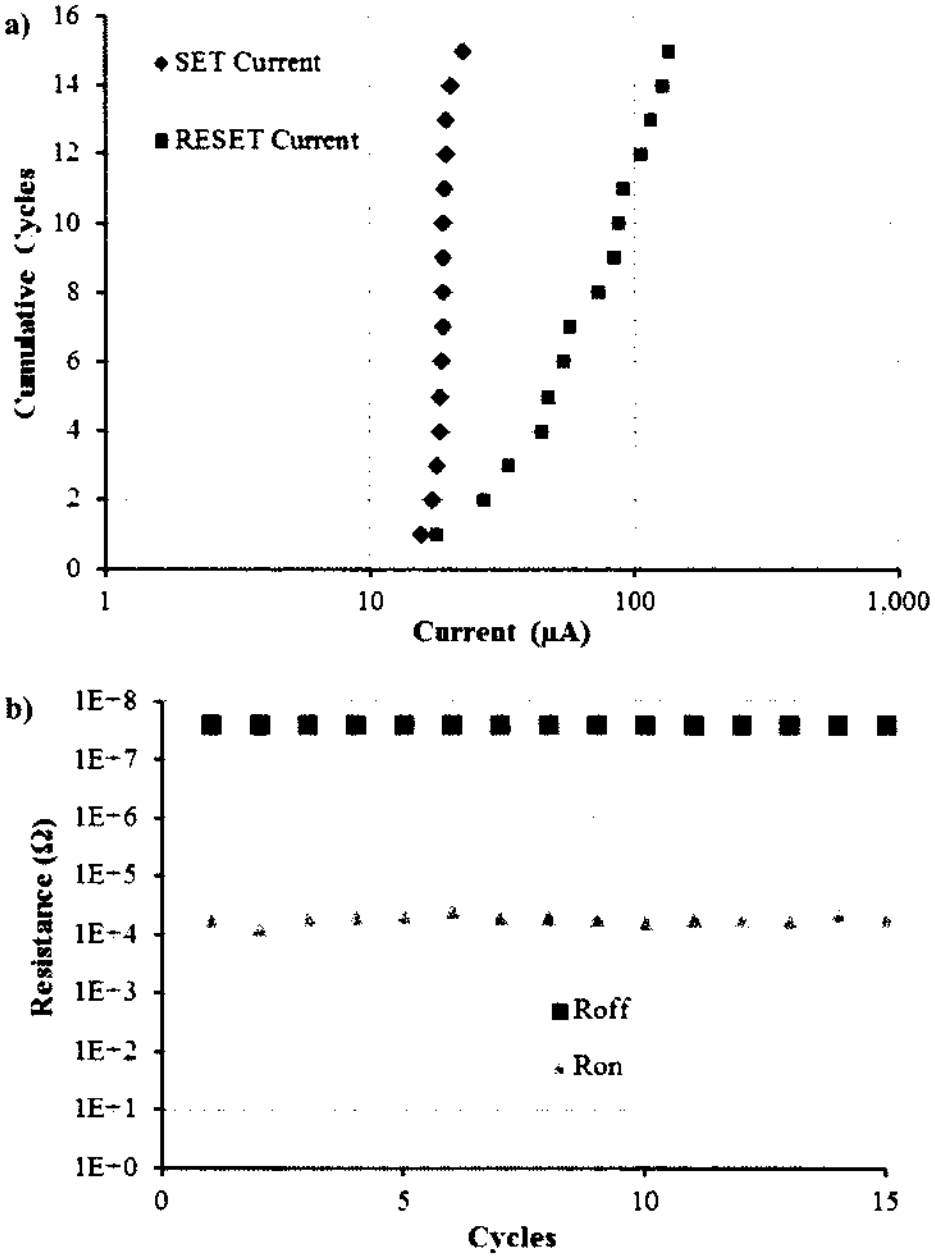


Figure 71. a) Plot of SET and RESET current distribution and b) R_{ON} and R_{OFF} for 15 cycles using the current compliance circuit (Device X).

There are two distinct problems with the structure. The first one is that the thickness of the Ta_2O_5 solid electrolyte layer in the active device region is very difficult to control. This is because the exposed area is 10 nm in diameter and the target thickness of Ta_2O_5 is

16 nm. During Ta_2O_5 deposition it is deposited to the sidewalls of the spacer formed. In such case, there is a possibility of these films deposited on the sidewall to close up the active device area as the film deposited is 16 nm and the hole to be covered is 10 nm. This was not considered during the fabrication of Device X. The second problem is, according to literature reports there is a very high probability that the filament is the thinnest closer to the Cu electrode as shown in Figure 72. This will lead to the non-uniform annihilation of filament discussed in chapter 1, section 1.3. This leads to the variations in RESET current and the resistance values.

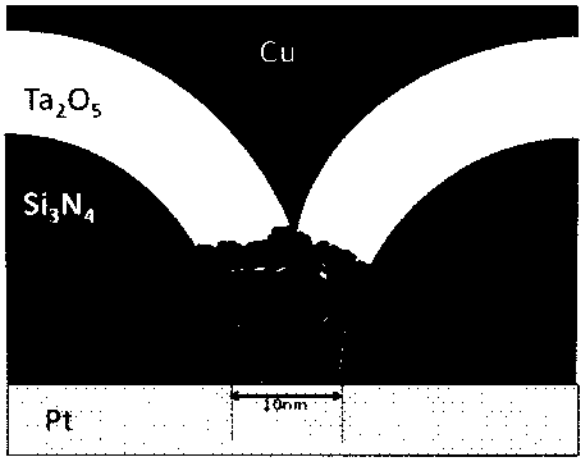


Figure 72. Probable shape of the filament formation for Device X shown in Figure 70.

The structure shown in Figure 70 is fabricated to achieve a device with constricted Pt electrode area with the existing double spacer technique. The ideal structure would rather be the one shown in Figure 73 a) to achieve uniform filament as shown in Figure 73 b). Nevertheless, this device configuration could not be pursued, because our developed integrated fabrication process flow always starts with the Cu deposition first for this structure. An entire new set of process steps will have to be developed to fabricate this

device, as Cu is not as inert as Pt. Therefore, a lot of deposition, wet etch and dry etch recipes will have to be investigated to check the compatibility of the recipes with Cu. That additional cost and process development time was beyond the means of this dissertation project.

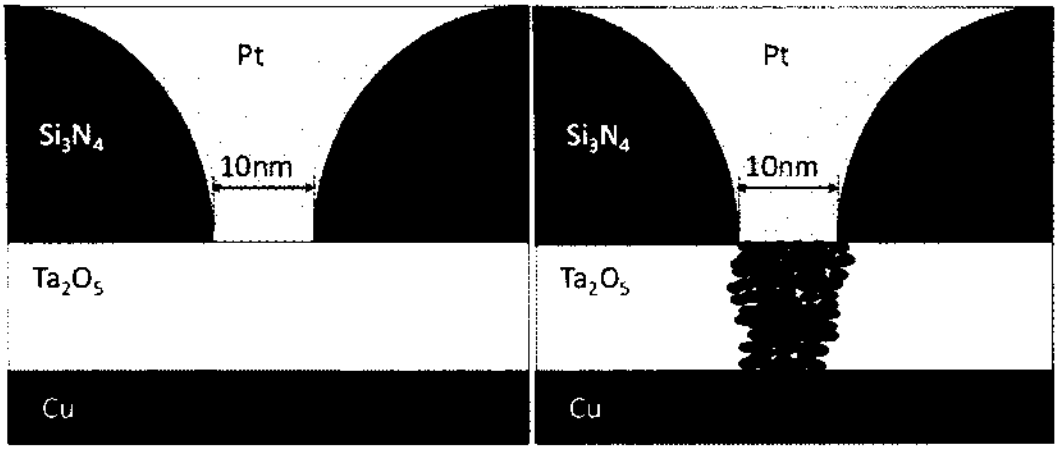


Figure 73. Ideal a) structure and b) single filament formation with restricted Cu nucleation site and annihilation site closer to the Cu electrode.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1 Conclusions

Resistive switching memory (RRAM) cells are among the most promising emerging non-volatile memories. They have tremendous potential to meet future needs by offering a successor technology that could replace the present memory device technology, as well as high performances switches in reconfigurable devices. Resistive switching memories are conceptually simple, low cost and CMOS compatible. Thus, a considerable amount of effort is being put into investigating of these devices. Despite having such advantages, RRAM devices are far from production due to issues like wide distribution of device performance and high RESET current. This thesis explored various methods to extract details of the device switching by designing novel measurement setups. Along with the measurements setups, novel device structures to minimize the random filament formation were also explored.

The outcome of the thesis can therefore be split into two distinct parts: the measurement setups and the fabrication of devices.

Design of Novel Electrical Measurement Setups

At the present time, all reliability tests of the resistive switching memories reported in the literature were performed by either using a slow parameter analyzer or by using pulsed signals without cycle to cycle information of the device outputs. In order to achieve a better reliability technique, a unique novel endurance test circuit was custom designed

and developed as part of the experimental work of this dissertation. This novel custom endurance test circuit was capable of measuring switching transients, ON and OFF resistances from cycle to cycle. The switching transients were measured with an accuracy of 4 ns. Low R_{ON} of less than 1 kΩ and high R_{OFF} up to 1.6 GΩ could be measured within 1 ms. During the measurement test stage it was realized that the variability in the device output was very large from cycle to cycle. Literature review suggests two major reasons for the detected variability: the current overshoot during SET process and the random metal filament formation and dissolution during switching. In this dissertation work, both of these factors challenging the technology were carefully analyzed and novel approaches to their solutions were explored in detail and successfully implemented.

The presence of the current overshoot was first investigated thoroughly. For this purpose, a special high speed circuit was designed and built. The transients during the switching of the RRAM devices were measured and compared with the simulated results using SPICE models. The results verified the presence of the current overshoot during SET. The current compliance circuits being used for the SET process were the primary significant contributors of the current overshoot. For this reason, a current compliance circuit capable of low current overshoot was developed in order to offer a solution. The developed current compliance circuit was capable of limiting the current through the device at the range of 20 μA without any overshoot within the resolution of 500 ps. The results showed significant change in the RESET current due to the elimination of the current overshoot. This constitutes a respectable achievement and success as the high RESET current in the range of few mA (high RESET power) is a major concern for the memory industry.

The results mentioned in the earlier sections confirm that during this work a powerful set of tools were designed to understand and control RRAM devices.

- No such endurance test circuit with capability of measuring transients (with accuracy of 4 ns) and high R_{OFF}/R_{ON} ratio ($>10^6$) together has been designed or shown [108-110]. The biggest advantage of this circuit was its ability to check the reliability of cycle within 1 ms. Since the variation in device performance is from cycle to cycle, this is a very useful tool to track the details of each cycles to understand the reason behind the variations.
- Current overshoot during SET could be controlled within 20 μA without any evidence of overshoot within 500 ps. By doing so the RESET current of devices were brought down to few hundreds of μA. Low SET current down to few μA has been obtained in literature, but all of the devices presenting such low SET current have high R_{ON} [111, 112]. However, for high performance switches low R_{ON} is desirable. The RESET current value in the range of few hundred of μA is a huge accomplishment compared to few mA for devices with low R_{ON}.

Design and Fabrication of Novel Device Structure

In order to address and to solve the technology challenge in the form of random filament formation and dissolution, special device structures with active device area close to the filament size were designed and fabricated. Two different structures one with the constricted Cu electrode area and the other with the constricted Pt area, were fabricated and tested. Both of these devices were investigated using the novel custom designed current compliance circuit. The results showed better results compared to the previous much larger devices that did not constrict the potential nucleation sites for the metal

filament. Both of the devices showed good switching characteristics in terms of high R_{OFF}/R_{ON} ratio and low RESET and SET current. The results also suggested that there is room for improvement in device structure to pursue this successful avenue by further optimization.

5.2 Future Work

The results discussed in chapter 4 (in the results and discussion section) show that the three custom designed circuits and the measurement setups that have been developed can be used successfully as tools to explore the working mechanism and the reliability of non-volatile resistive switches. During the course of this study, a large number of different devices with varying structures were fabricated and measured. Each of the devices showed promising results but the difference in the output due to device structure could not be deduced due to the insufficient number of data points. Device reliability studies require larger test series and amounts of collected data over much longer time periods. There are a few fabrications and data mining that have begun but are not completed; two of which are mentioned here after.

Data Analysis

LabView was used as a tool to analyze the significant amount of data. The program used so far to obtain the key parameters of the device performance can be improved. Two aspects of the program that have to be improved are efficiency and user friendliness.

The data obtained from the experiments constitute a mine of information. It is therefore critically important to be able to analyze the data accurately. The results shown (**Figure 74**) here are just few examples of how the data can be used to extract the important

information. Tremendous improvement in the code is required in order to achieve the most accurate and reliable information from the data.

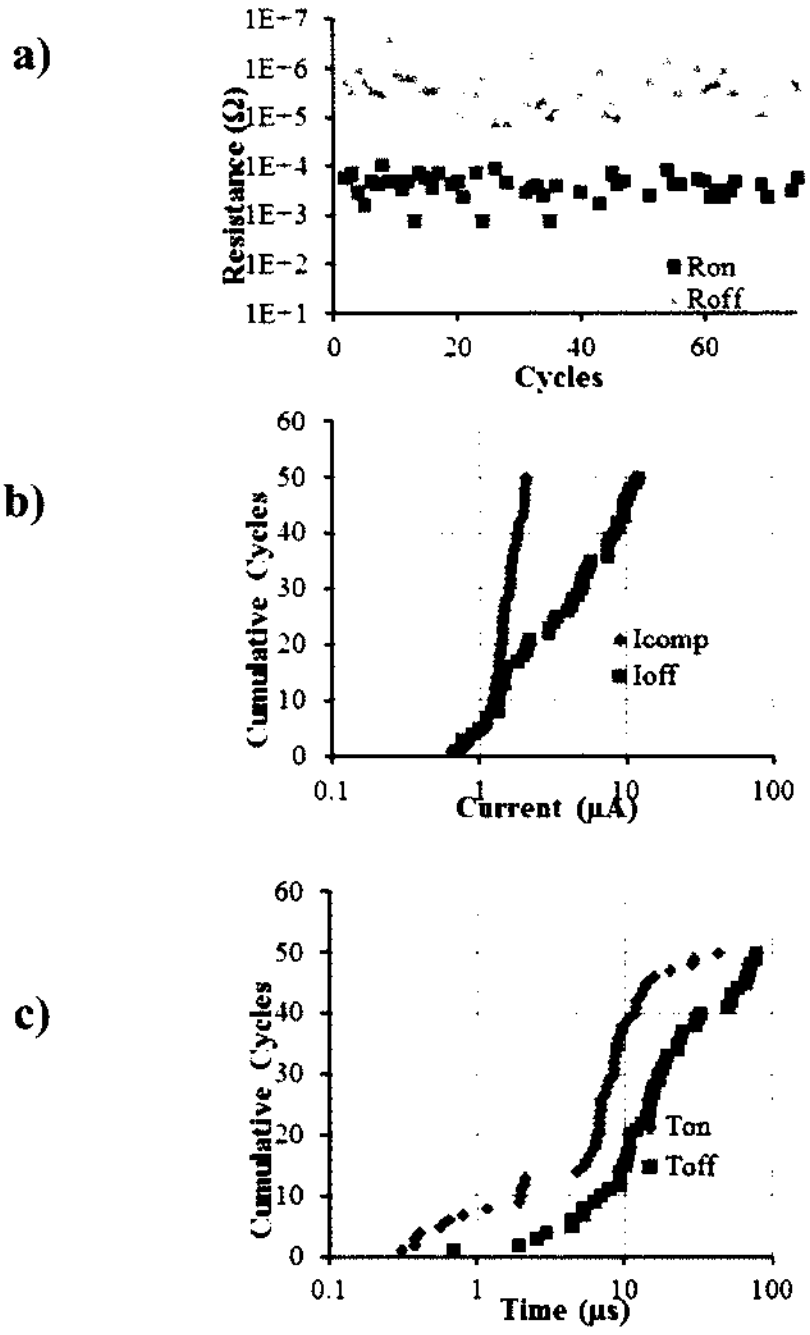


Figure 74. Data for sample X showing a) R_{ON} and R_{OFF} values obtained for sample X. b) current compliance of each cycle (Icomp) and RESET current (Ioff) and c) time to switch ON (Ton) and time to switch OFF (Toff).

Replacement of Pt with CMOS Compatible Electrodes

Present device use Pt as the inert bottom electrode. Pt being a very stable noble metal is a good candidate for the initial fundamental research phase but when it comes to CMOS processing, it is not a desirable electrode because it is very difficult to RIE etch Pt causing the patterning to be very complicated. The first metal that is being tested as an alternative is Tungsten (W) as Ta_2O_5-W has been known to work well with electrodes other than Cu [113].

RF sputtering is used for W deposition (Table 15) and it is found that the device would SET and RESET at a very high voltage. Once the device RESET, it would never SET again. On further investigation, it is found that the bottom W electrode has very high resistance leading to large voltage drop across the electrode compared to the device when the device is ON (at low resistance state). The high off voltage would then lead to high heat generation leading to the breaking of the electrode instead of the filament in the solid electrolyte. Therefore, deposition of low resistivity tungsten deposition was carried out.

To improve the resistivity, the tungsten recipe with higher deposition rate of tungsten was explored. For this, the RF sputter deposition of W is abandoned. DC sputter deposition is attempted to improve the deposition rate (Table 16).

To achieve the maximum possible deposition rate, the voltage at which the deposition is done has to be high. To achieve this, Ar pressure is decreased. The set of experiments performed and results are shown in Table 17. The experiments are performed on a substrate with patterned resist (Table 18). This is done to achieve the closest possible results to the actual process during lift off of W.

Replacing Sputter Deposition of the Tantalum Pentoxide Solid Electrolyte with Atomic Layer Deposition (ALD) Technology

For better film thickness uniformity and better conformity, ALD [114] technology would be useful to explore as an alternative to the sputtered Ta_2O_5 layer. ALD has excellent properties like conformal self-limiting deposition over large areas. It is superior to many deposition techniques when it comes to control of the film thickness and composition of the film deposited. It is comparatively a slow process but it is useful for depositions where small thicknesses are required with the highest accuracy. For the $Pt/Ta_2O_5/Cu$ device stack, a target thickness of 16 nm Ta_2O_5 solid electrolyte is deposited using sputtered Ta_2O_5. For superior control over this Ta_2O_5 thickness, an ALD deposition process would be the preferred method. Along with the film, non-uniformity sputtered films also suffer from Ar gas incorporation into the sputtered layer during deposition. Sputter technique offers flexible parameters to be changed during deposition for better control over the film. Nevertheless, for the same reason it is an extremely complicated system. Any change in one of the parameters may lead to a completely different film.

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APPENDIX

Details of Fabrication Procedures

Lithography

AZ5214

1. Clean : DI rinse, nitrogen dry
2. Dehydration bake : if cleaned with DI water
3. Prime : optional not done in our case
4. Coat: 4000 rpm (1.15 μm thick coat)
5. Soft bake: 110 °C for 1 min
6. Expose: vac. Exposure dose = 56 mJ/cm^2 (λ = 405 nm)
7. PEB(Post exposure bake): 115 C for 120 sec
8. Flood exposure without mask, dose = 375 mJ/cm^2
9. Develop: MF319, 60-90 sec (60 sec worked just fine)

LOR 3A lift-off resist

1. Clean wafer
2. Coat: LOR-3A , 3000 rpm for 40 sec(300 nm thick)
3. Bake: 200 °C for 5 min
4. S1813 coat: Spin coat at 4000 rpm for 45 sec (1.2 micron)
5. Soft bake: 115 °C for 1 min
6. Expose: vac. Exposure, dose = 110 mJ/cm^2
7. Develop: MF 319 for 1 min and 30 sec
8. Bake: 115 °C for 1 min

S1813

1. Clean wafer
2. S1813 coat: Spin coat at 4000 rpm for 45 sec (1.2 micron)
3. Soft bake: 115 °C for 1 min
4. Expose: vac. Exposure, dose = 110 mJ/cm^2
5. Develop: MF 319 for 1 min
6. Bake: 115 °C for 1 min

Etching Recipes

Table 1. Recipe for anisotropic etching of Si.

Recipe	Anisotropic etching of Si		
Equipment	**RIE#2**	**RIE#2**	**RIE#2**
Gases			
SF_6	**25 sccm**	**25 sccm**	**25 sccm**
CHF_3	25 sccm	25 sccm	25 sccm
Pressure	**10mtorr**	**10mtorr**	**10mtorr**
Power	80 watt	160 watt	200 watt
Time	**5 min**	**10 min**	**5 min**
Etch rate	96.6 nm/min	107.6 nm/min	113 nm/min
Remarks	**This was done to test the recipe for 80W. 66nm**	**This was done to test the recipe. S1813 used as the mask**	**This was done to test the recipe for 200W to get better anisotropy**

Table 2. Recipe for anisotropic etching of Si_3N_4 in an ICP etcher.

Recipe	Anisotropic etching of $SiON/Si_3N_4$
Equipment	**ICP etcher**
Gases	
SF_6	**10 sccm**
CHF_3	90 sccm
Pressure	**15 mtorr**
RF Power	25 W
ICP Power	**2000 W**
DC Bias	125 V
Remarks	

Table 3. Recipe for anisotropic etching of Si_3N_4 in RIE.

Recipe	Anisotropic etching of Si_3N_4
Equipment	**RIE**
Gases	
O_2	**5 sccm**
CHF_3	50 sccm
Pressure	**40 mtorr**
Power	200 W
Dc bias	**420 V**

Table 4. Recipe for Cr etching in ICP etcher.

Recipe	Cr etch
Equipment	**ICP etcher**
Gases	
He	**42 sccm**
Cl_2	50 sccm
O_2	**8 sccm**
Pressure	12 mtorr
RF Power	**6 W**
ICP Power	1200 W
DC Bias	**55 V**
Etch rate	30 nm/min
Remarks	

Table 5. Recipe for descum.

Recipe	Descum
Equipment	**RIE#1**
Gases	
O_2	**30 sccm**
Pressure	600 mtorr
Power	**100 W**
Bias	90 V
Etch rate	**20 nm/min**
Remarks	

Deposition Recipes

Table 6. Recipe for sputtered Ta deposition.

Recipe	Ta deposition
Equipment	**Sputter**
Base pressure	$3x10^{-6}$ torr
Ar flow	**50 sccm**
Pre-sputter	60 sec
Deposition pressure	**4.8 mtorr**
RF power	300 W
DC bias	**351 V**
Deposition rate	
Remarks	**Adhesion layer between Pt and SiO_2**

Table 7. Recipe for sputtered Pt deposition.

Recipe	Pt deposition
Equipment	**Sputter**
Base pressure	$3x10^{-6}$ torr
Ar flow	**35 sccm**
Pre-sputter	60sec
Deposition pressure	**4.25 mtorr**
DC Amp	0.25 A
DC bias	**349 V**
Deposition rate	≈2 Å/sec
Remarks	

Table 8. Recipe for sputtered Ta_2O_5 deposition

Recipe	Ta_2O_5 deposition
Equipment	**Sputter**
Base pressure	$3x10^{-6}$ torr
Ar flow	**50 sccm**
Pre-sputter	60 sec
Deposition pressure	**3.8 mtorr**
RF power	300 W
DC bias	**207 V – 147 V**
Deposition rate	1 Å/sec
Remarks	

Table 9. Recipe for sputtered Cu deposition (dep. rate = 1.8 Å/s)

Recipe	Cu deposition
Equipment	**Sputter**
Base pressure	$3x10^{-6}$ torr
Ar flow	**35 sccm**
Pre-sputter	20 sec
Deposition pressure	**4.18 mtorr**
CD current	0.25 A
DC bias	
RF substrate bias	
Deposition rate	**1.8 Å/s**
Remarks	

Table 10. Recipe for sputtered Cu deposition (dep. rate = 16 Å/s)

Recipe	Cu deposition
Equipment	**Sputter**
Base pressure	$3x10^{-6}$ torr
Ar flow	**35 sccm**
Pre-sputter	20 sec
Deposition pressure	**4.18 mtorr**
CD current	1.25 A
DC bias	**386 V**

Table 11. Recipe for sputtered Cu deposition with substrate bias.

Recipe	Cu deposition
Equipment	**Sputter**
Base pressure	$3x10^{-6}$ torr
Ar flow	**35 sccm**
Pre-sputter	20 sec
Deposition pressure	**4.18 mtorr**
CD current	1.25 A
DC bias	**386 V**
RF substrate bias	5 W/ 78 V
Deposition rate	
Remarks	RF bias added to improve adhesion

Table 12. Recipe for Cr deposition with ebeam.

Recipe	Cr deposition
Equipment	**ebeam**
Base pressure	$3x10^{-6}$ torr
Deposition rate	**1.5 Å/sec**
Remarks	

Table 13. Recipe for sputtered Cr deposition.

Recipe	Cr deposition
Equipment	**Sputter**
Base pressure	$3x10^{-6}$ torr
Ar flow	
Deposition pressure	
RF power	
DC bias	
Deposition rate	**1.5 Å/sec**
Remarks	

Table 14. Recipe for PECVD Si_3N_4 deposition.

Recipe	Conformal PECVD Si_3N_4 Deposition
Equipment	**PECVD**
Gases	
SiH_4	**160 sccm**
N_2	150 sccm
NH_3	**5**
Pressure	900 mtorr
Power	**50 watt**
Temperature	300 °C
Average dep. rate	**11-15 nm/min**
DC bias	5-7 V

Table 15. RF sputter deposition of W.

Recipe	W deposition
Equipment	**Sputter**
Base pressure	$3x10^{-6}$ torr
Ar flow	**35 sccm**
Deposition pressure	3.8 mtorr
RF power	**500 W**
DC bias	
Deposition rate	**1.7 Å/sec**
Remarks	

Table 16. DC sputter deposition of W.

Recipe	W deposition
Equipment	**Sputter**
Base pressure	$3x10^{-6}$ torr
Ar flow	**35 sccm**
Pre-sputter	
Deposition pressure	**2.4 mtorr**
DC Amp	1.5 A
DC bias	
Deposition rate	≈7.2 Å/sec
Resistivity	**20 μΩ.cm**

Table 17. Experiments to achieve low resistivity W.

SN	Pre-sputter SCCM	Sputter sccm	Start pressure torr	DC current set Amp	DC voltage V	DC power	Deposition pressure mtorr	Deposition rate Å/sec	Resistivity Ω.m	Remarks
1	5	5	$3x10^{-6}$	1.25	460	578	0.744	3.8	$8x10^{-7}$	X20 more than the bulk
2	1	1	$3x10^{-6}$	1.25	600	--		---		No plasma
3	3	3	$3x10^{-6}$	1.25	600	---		---		No plasma
4	4	4	$3x10^{-6}$	1.25	600	---	$1.23x10^{-3}$	---		No plasma
5	5	4	$3x10^{-6}$	1.25						Pre-sputtering went fine but the plasma could not sustain the 4 sccm sputter
6	5	5	$1.74x10^{-6}$	1.5	470	714	0.773	4.48	$2.13x10^{-7}$	X4 more than bulk and x2 more than thin film sputtered W

Table 18. List of recipes explored for sputter W with resist.

SN	Pre-sputter SCCM	Sputter sccm	Start pressure torr	DC current set Amp	DC voltage V	DC power	Deposition pressure mtorr	Deposition rate Å/sec	Resistivity Ohm.m	Remarks
1	5	5	$3x10^{-6}$	1.25	460-464	578-582	0.738	4.2	$11x10^{-7}$ /$15.51x10^{-7}$	100 secs/ very stable
2	5	5	$3x10^{-6}$	1.25	460	578	0.744	3.8	$8x10^{-7}$	X20 more than the bulk
3	5	5	$8.74x10^{-7}$	1.25	458-468	574-588	0.728-0.785	4.6	$3.5x10^{-7}$	Lift of fine/ did not run after 300 secs
4	5	5	$8.95x10^{-7}$	1.5	458-471	693-712	0.767-0.791	5.5	$3.5x10^{-7}$ /$2.56x10^{-7}$	100secsx2/ 1 min gap/ stable/ lift off fine
5	5	5	$2.8x10^{-6}$	1.5	475-484	748-731	0.854-0.874	5	$7x10^{-7}$	Did not run after 250 secs/affects resist
6	5	5	$1.74x10^{-6}$	1.5	470	714	0.773	4.48	$2.13x10^{-7}$	X4 more than bulk and x2 more than thin film sputtered W Not stable stops after 300secs

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EDUCATION

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AWARDS

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Outstanding PhD Researcher Award 2010, Department of Electrical and Computer Engineering, Old Dominion University

2nd place, Poster competition organized by American Vacuum Society (AVS), Mid-Atlantic Chapter, 2010

3rd place, Poster competition organized by AVS, Mid-Atlantic Chapter, 2009
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EXPERIENCE

National Institute of Standard and Technology, Department of Commerce, Gaithersburg, Maryland
Guest Researcher *May 2010- Present*

- Fabrication of Nano-cross bar switch for reconfigurable devices using solid-electrolyte
- High-speed measurements of resistive switching devices
- Fabrication and measurements of capacitors and MOSFETs using deposited oxide on SiC
- Fabrication of NEMs structures with Nano-pores for DNA sequencing
- Micro-ESR probe tip fabrication

Old Dominion University, Dept. of Electrical and computer Engineering, Applied Research Center, Jefferson Lab, Newport News, Virginia
Graduate Research Assistant *January 2007-Present*

- Processing and Electrical measurements of ALD (Atomic Layer Deposition) High-k Dielectrics
- Processing and electrical measurements of Solid-electrolyte Switch

Graduate Teaching Assistant — *January 2010-May 2010*
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1. P. Shrestha, A. Ochia, K. P. Cheung, J. P. Campbell, H. Baumgart, and G. Harris, Electrochemical and Solid-State Letters, vol. 15, pp. H173-H17(2012)
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Seminar PRESENTATIONS

1. Z. Chbili, P. Shrestha, L. Yu, C. Vaz, J.-H. Kim and K. P. Cheung, "Sputter-Deposited Oxide on SiC", 17th Annual SiC MOS workshop, 2012.
2. P. Shrestha, "Non-Volatile Resistive Memory for High Performance Switches", Seminar 2012, Electrical and Computer Engineering, Old Dominion University.

POSTER PRESENTATIONS

1. P. Shrestha, K.P. Cheung, H. Baumgart, "Switching Characteristics of Nano-crossbar Pt/Ta_2O_5/Cu Stack", AVS mid Atlantic Meeting, 2011.
2. P. Shrestha, D. Gu, H. Baumgart, G. Namkoong, T. Abdel-Fattah, "ALD Synthesis of Nested Coaxial Multiple Walled Nanotubes by Template Replication", AVS mid Atlantic Meeting, 2010.
3. P. Shrestha, C. Ndoye, W. H. Anderson, D. A. Elliott, J. D. Thomas, H. Baumgart, D. Gu, "Electrical Properties of MOS Capacitors with High-k Dielectric HfO_2 Gate Insulator Using ALD", AVS mid Atlantic Meeting, 2009.