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Congestion-aware wireless network-on-chip for high-speed communication

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ABSTRACT

The design of system-on-chip (SoC) requires the complex integration between a multi-number of cores on a single chip. To establish the effective communication between multiple cores there aremore challenging issues on designing the network-on-chip (NoC) architectures. The proposed system deals with the utilization of on-chip antennas for the wireless communication between the long distance cores to minimize the latency and power. In this proposed work, we have designed high-speed wireless NoC (WiNoC) for on-chip communication. This high-speed WiNoC has been achieved by designing a congestion measure unit, which monitors and measures the congestion in the input data and establishes the effective wireless communication between the output channels and routers. The designed architecture is synthesized and implemented by using Altera Quartus II, where the SoC is designed using Qsys builder. The proposed WiNoC shows better performance parameters like throughput, latency and power than the conventional NoC.

KEYWORDS

Network-on-chip; network routing; integrated circuit design; system-on-chip; wireless NoC

1. Introduction

In emerging on-chip communication technology, net work-on-chip (NoC) has emerged as the communication architecture of complex system-on-chip (SoC) since it has to overcome the problem of reliability, power and speed, which requires high efficiency in bus architecture [1]. By increasing the number of cores of a chip based on the requirement, the NoC architecture faces the communication problem with the distant cores in terms of reliability [2]. As per the International Technology for Roadmap for Semiconductors (ITRS) [3], the wired communication between the cores does not satisfy the interconnection in terms of performance and reliability and a recent research was established as an integrated chip antenna for inter- and intra-chip communication [4]. However, the operating frequency of this silicon-integrated antenna has an energy dissipation problem to establish the communication between the cores. On the other hand, the communication between the distant IP cores causes more latency and power consumption. Since the implementation, it is clear that the performance of the conventional NoC retains the improvement in integrated circuits (IC) performance. This problem initiated the opportunities for the investigation into wireless NoC (WiNoC). This wireless communication technology is suitable to solve the latency and power dissipation issues from the conventional technology, which also eliminates the complexity of interconnection.

In this paper, the design of high-speed WiNoC architecture has been proposed to avoid the traffic between the data transmissions. The performance of speed and power of wireless links has been analysed by the utilisztion of cycle simulation. Recently, more number of WiNoCs have been proposed by integrating the on-chip antennas and transceivers to enable the intra-chip wireless interconnection [5,6]. The dedicated WiNoC architecture and the network calculus were designed to enable the wireless link operations. On-chip WiNoC between the cores of SoC is illustrated in Figure 1. The wireless link receives the data from different cores and assigns the topology to establish the communication between the cores.

This WiNoC link enables the multi-hop communication between the different nodes and reduces the hop counts in communication. Currently, the single-hop communication improves the performance of the wireless communication. In conventional WiNoC topology, the channel allocation has been designed with separate bandwidth to send the data. Hence, the proposed WiNoC architecture uses an energy-efficient wireless transceiver to improve the link utilization statistics [7]. The implementation of on-chip wireless communication links leads to significant savings in latency, even considering the overhead of wireless transceivers [8]. In our proposed method, the interconnection of WiNoC architecture considers the adaptability, channel numbers and wireless links.

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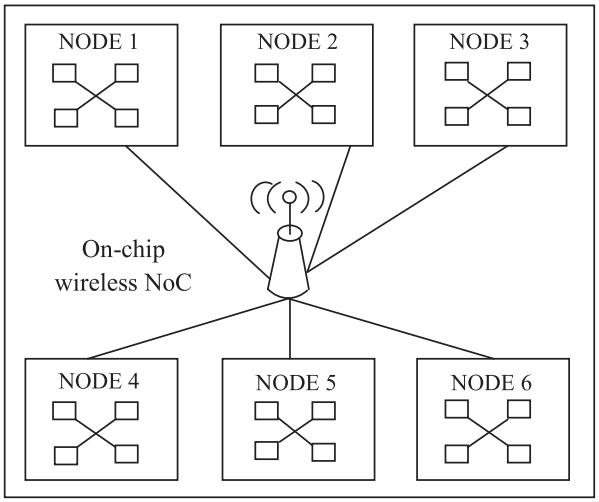

Figure 1. Illustration of WiNoC in multi-core SoC.

Organization of the proposed work is as follows:

- proposed WiNoC design between distant-range links
- design and placement of wireless antenna
- congestion-free wireless link.

2. Proposed WiNoC design between distant-range links

In wired NoC, the embedded cores communicate with switches and wired links. The data transfer between this multi-hop communication leads to high energy dissipation and latency. To overcome this problem, we proposed a low-power, high-speed, long-distance wireless link between the cores in SoC chip. The following section focuses on the design of NoC architecture of WiNoC.

2.1. Proposed network architecture

The proposed method also focuses on the location facility problem [9]. The problem with this method is channel allocation for different data. The objective of this proposed method is to reduce congestion to improve the communication facility. In this proposed work, the antennas are placed in the corner of each subnet. The main idea to place the antenna is the consideration of the demand level of processing elements. The reconfigurable routing method is implemented in this paper to transmit the data in all directions. In this routing method, the data are transmitted from the source to destination by identifying the neighbour nodes. The long-distance nodes placed in any direction establish the communication and implementation of the routing algorithm with respect to nodes, as shown in Figure 3. The data transmission between the nodes is established using a reconfigurable routing algorithm. The distance measured between the nodes, processing elements and antenna identified by utilizing the network parameter is shown in Figure 2. The distance between each node and antenna is calculated and stored as input models in matrix formats by defining the distance between the communication points. Figure 2 shows the pseudocode for the proposed wireless routing algorithm for the reconfigurable topology. By considering the source and destination nodes as input, return the selected data as an output through the channel. By considering the X and Y dimension, label the routing direction with N_x and N_y. If both N_x and N_y values are zero, the output data are transmitted with the minimal diagonal channel path, and X Y channels are further candidates. If $|N_x| - |N_y| \geq 2$, the output data passes through the diagonal channel with a non-minimal path. If N_x is non-zero and N_y is zero, the X channel will be selected as network selector (NS), when $|N_x| \geq 2$, the two diagonal channel will be available to transmit the data. If N_x is zero and N_y is non-zero, the Y channel will be selected. If both of these two offsets are zero, the packet data will be in the destination router, and the data are transmitted to its local processor via L output port, where L represents the eternal channel of the port.

In minimal routing, the packet data are considered in the rectangular (REC (s, d)), defined by the source nodes (S_x, S_y) and the destination nodes (D_x, D_y). That means the routers residing in (REC (s, d)) will establish the communication between routers for transmitting the packet data. In the proposed reconfigurable routing different channel paths are provided for routing to establish the communication, but it uses only three of the channels ($X-$, $T+$ and $C-$) for output. Assigning higher priority based on the congestion between the links and the output channel selection is based on the NS state. Initially, the short-range communication channels are provided with high priority. The channels in NS will be divided into two sets based on the communication channel and the channel path. The short-range channels have been given higher priority to direct packets of destination nodes more quickly. If the operation path has high priority and the channels are free, the packet could bypass the congested area and proceed with its destination, if more than one packet competes for the same output channel.

3. Design and placement of wireless antenna

In our proposed WiNoC, carbon nanotube antennas are used to establish the communication between the nodes. This antenna was implemented using multiband sources of Frequency Division Multiplexing (FDM) to communicate and transfer different frequencies of the same channel. The highly directional gain of this antenna helps to create directed channels between the source and destination. The placement of this link depends on the chip parameter like the number of cores, number of short- and long-range link and the

Algorithm

Input: Source node (S_x ,S_y) and destination node (D_x ,D_y)

Output: Selected output

```
1.  {
2.  N_x = D_x − S_x , N_y = D_y − S_y ; NS = Ø
3.  if N_x≠ 0 and N_y > 0
4.  {
5.  N_s = {T+, X−, Y+}
6.  if |N_x| − |N_y| >= 2NS = NS U{c−}
7.  }
8.  if N_x ≠ 0 and N_y < 0
9.  NS = {C−, X−, Y−}
10. {
11. if |N_x| − |N_y| >= 2NS = NS U{T+}
12. }
13. if N_x == 0 and N_y ≠ 0
14. {
15. if N_y > 0NS = {Y+}
16. else NS = {Y−}
17. }
18. if N_x ≠ 0 and N_y == 0
19. {
20. NS={X-}
21. if |N_x| >= 2NS = NS U{T+, C−}
22. }
23. if N_x == 0 and N_y == 0NS = {L};
24. return select (NS)
25. }
```

Figure 2. Proposed routing algorithm pseudo-code.

traffic distribution. To place wireless links is to minimize the number of hop counts in the communication network and to optimize the traffic interactions between the cores.

This antenna was placed based on the annealing methodology to configure faster than the conventional search method. The routing method implemented here is a combination of reconfigurable routing for the nodes, where the communication between cores takes place, as shown in Figure 3. The structure of the wireless router and its interconnection between wireless link I is shown in Figure 4. Each wireless router has five input ports, five output ports, a router arbitrator and a congestion measure unit with the traffic and arbitration controller. This congestion measure unit measures each congestion information from the from

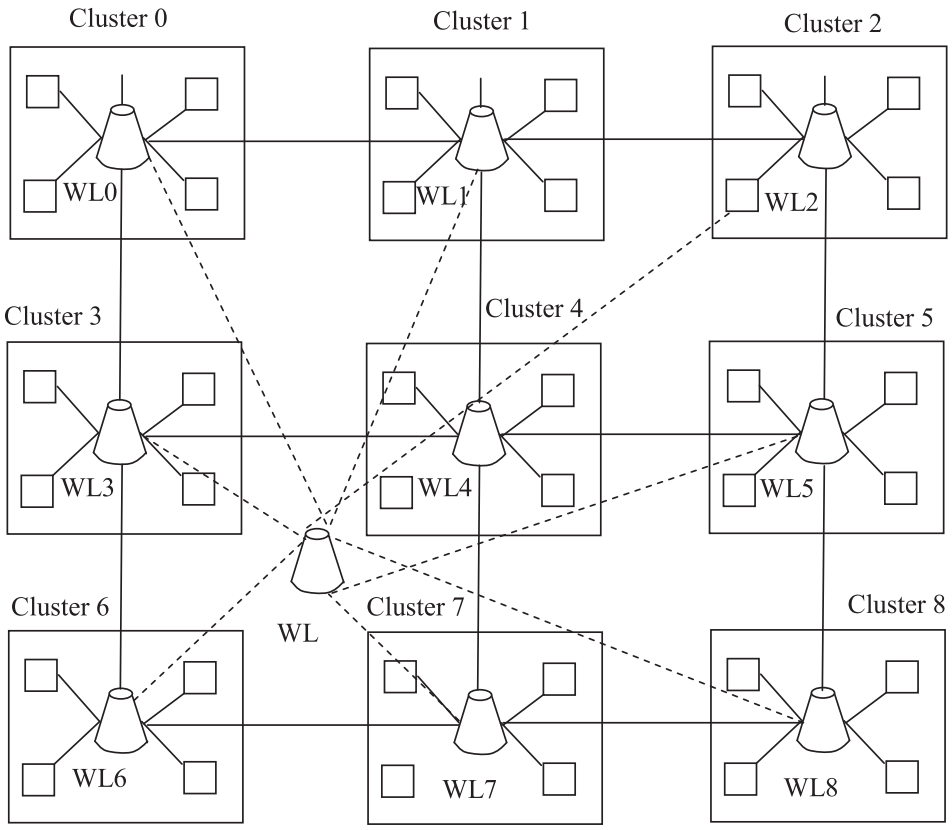

Figure 3. Wireless link establishment between cores.

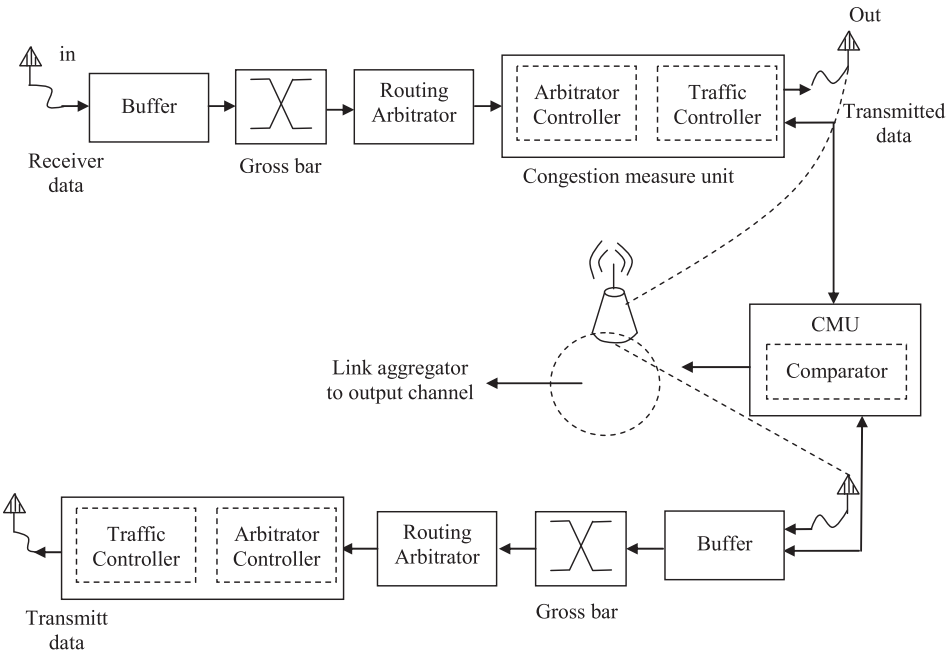

Figure 4. Wireless router architecture and its link establishment.

the receiver unit and transmits to the global congestion measure unit. The global congestion measure unit has a comparator unit, which compares the congestion data to link aggregator to establish the communication or to transmit the output data. Each port of this implementation gets connected in the wireless medium.

The congestion measure unit transmits the output data by the sub-channel division based on the Frequency Division Multiple Access (FDMA) technique, as explained in [10]. The same operation was carried out on the receiver side of the output channel. As shown in the architecture all the transmitter and receiver links are connected with link aggregator in the wireless link and

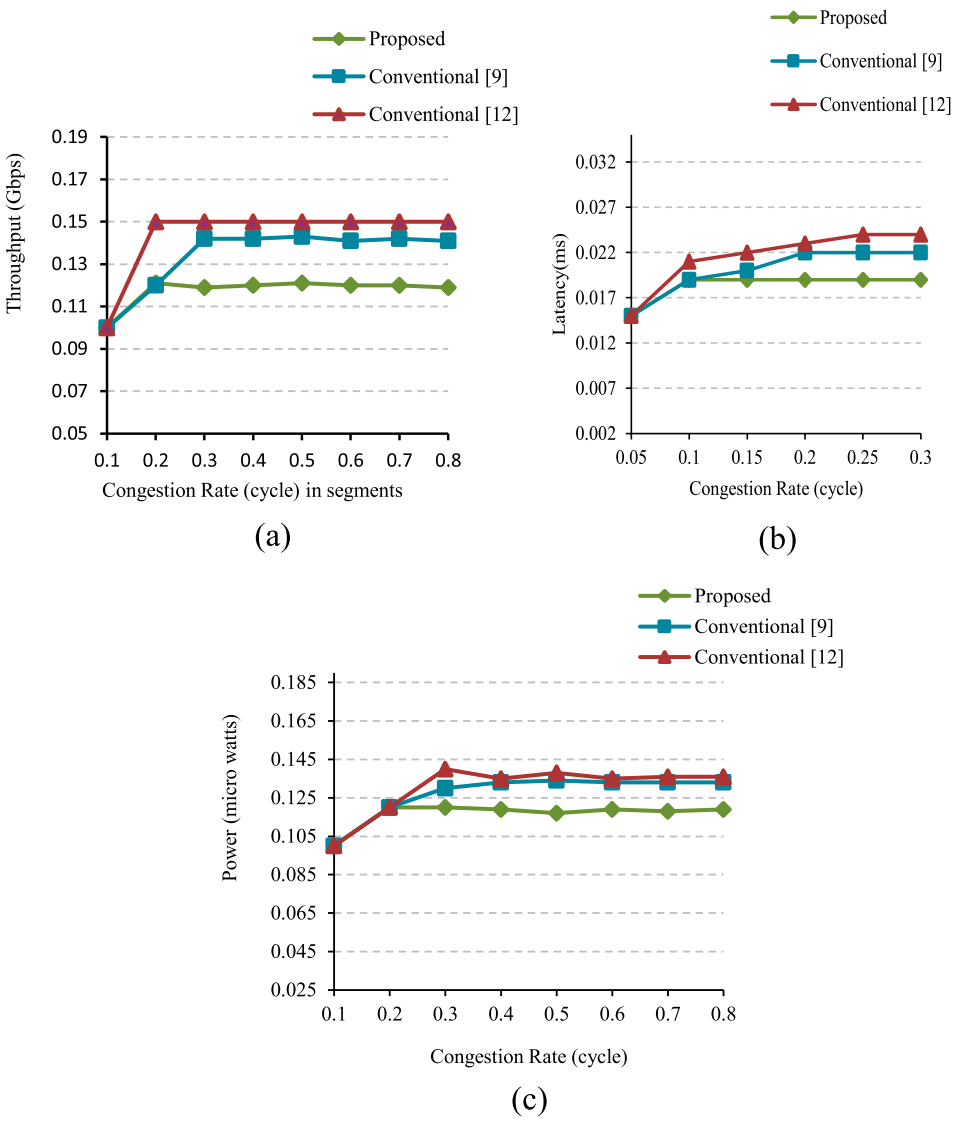

Figure 5. The comparison of (a) throughput (b) latency (c) power of conventional method with the proposed method.

the data are transmitted and received simultaneously between the transmitter and receiver.

4. Congestion-free wireless link

The performance of the WiNoC in on-chip communication deals with the effective design and transfer of data, as shown in Figure 4. This effective data transfer is achieved by avoiding the congestion between the wireless links. In general, congestion occurs when the sequence of packets is waiting to transfer from the channel, hence packets are blocked indefinitely. In WiNoC, resources are shared among different packets; if there is no cyclic channel dependency on the network [11], the congestion will never occur. To deal with the congestion issue, WiNoC routing schemes are designed with the effective mechanism. The buffers are designed to store and bypass the congested path. The routers embedded in the routing algorithm are to provide the flexible routing arbitration algorithm to relax the network traffic by coordinating the input pairs with a wireless router. The congestion measure unit measures the information by inspecting the input ports in the router [12,13]. This congestion measurement is based on the clock-by-clock cycle and the received information is sent to the nearby routers used for the next clock cycle. The global congestion unit provides the faster links to reduce the transmission time by exchanging the congestion information. In this global congestion measure unit, comparator block is used with a buffer. Instead of sharing the information, this comparator compares the resource utilization by inspecting the elements. By analysing the information about wireless transmitter and receiver buffers, the link aggregator will enable the link. Once the information is compared, then the packets resume the communication between the wireless routers [14,15]. The algorithm shows congestion detection mechanism and routing performance.

5. Experimental results and set-up

To evaluate its performance, the proposed wireless communication is simulated in Ansys High Frequency

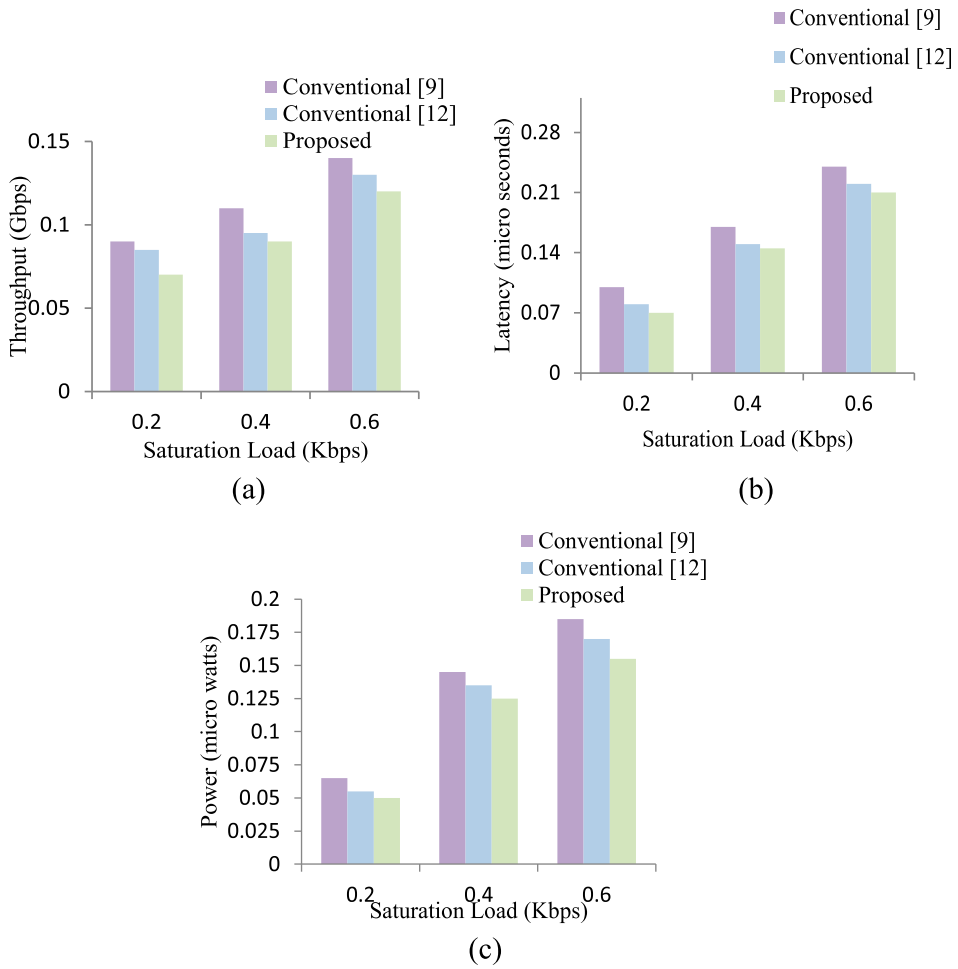

Figure 6. Comparison of (a) throughput (b) latency (C) power for different saturation loads.

Structured Simulator (HFSS) [16,17]. Here, we investigated on a wide range of WiNoC configurations. Both the conventional and proposed WiNoC topologies are investigated and summarized in Figure 5. This WiNoC simulator has a traffic controller located in a congestion measure unit, which enables product application and synthetic traffic patterns. In the synthetic pattern, WiNoC is designed with the injection and distribution function. The packets are injected into the wireless router from the transmitter antenna by the injection pattern, based on the level 0 or 1 model. Level 0 model indicates the channel is free and level 1 indicates the channel is full.

Latency, throughput and power are the essential and fundamental performance evaluation metrics in the core integration. The congestion measure unit keeps tracking the transmission data and monitors the throughput, latency and power in different traffic loads. Saturation load is analysed, where throughput is no longer growing. This congestion load is calculated based on the load and our results of the saturation loads are compared with the conventional method, as shown in Figure 6. The implementation results show that the improvement in throughput is about 15%, which is achieved by incorporating parallel buffers. This implementation results show that the proposed WiNoC outperforms in long-distance wireless communication. By incorporating a congestion measure unit, the load is efficiently monitored and the routing operation is implemented by alternative links. All the above implementation methods show effective optimization of the parameters such as latency, throughput and power.

The NoC interconnection is designed using the Altera Qsys builder to solve the communication problem between the cores, such as how the transaction takes place between the nodes in the SoC. The implementation of Qsys includes the core, where the designers use the core to implement a SoC in less time using the Qsys integration method.

6. Conclusion

To exploit the advances in NoC, high-speed and low-power WiNoC has been proposed to manage the traffic and establish the wireless communication between the routers. The proposed WiNoC improves not only the parameters, but also the reliable communication between the routers. We have compared our proposed WiNoC with conventional NoC. And our proposed WiNoC outperforms in terms of throughput, latency and power for different traffic and saturation loads.

With the congestion measure unit, the wireless link was employed between the routers. Moreover, the theoretical justification for pseudocode was given for the wireless link establishment of the congestion-free and different saturation-load conditions. Implementation results show that the proposed WiNoC can provide better performance and better reliability than the conventional NoC.

Disclosure statement

No potential conflict of interest was reported by the authors.

References

[1] Kodi A, Sarathy A, Louri A. Design of adaptive communication channel buffers for low-power area-efficient network-on-chip architecture. Proceedings of the 3rd ACM/IEEE Symposium on Architecture for Networking and Communications Systems; 2007. ACM.

[2] Ogras UY, Marculescu R. It's a small world after all: NoC performance optimisation via long-range link insertion. IEEE Trans Very Large Scale Integr (VLSI) Syst. 2006;14(7):693–706.

[3] Schaller RR. Technological innovation in the semiconductor industry: a case study of the International Technology Roadmap for Semiconductors (ITRS) [dissertation]. George Mason University.

[4] Yordanov H, Russer P. Wireless inter-chip and intra-chip communication. 2009 European Microwave Conference, EuMC; 2009. IEEE.

[5] Chang MF, Roychowdhury VP, Zhang L, et al. RF/wire less interconnect for inter-and intra-chip communications. Proc IEEE. 2001;89(4):456–466.

[6] Mahmoud SF, AlAjmi AR. Characteristics of a new carbon nanotube antenna structure with enhanced radiation in the sub-terahertz range. IEEE Trans Nanotechnol. 2012;11(3):640–646.

[7] DiTomaso D, Kodi A, Matolak D, et al. Energy-efficient adaptive wireless NoCs architecture. 2013 Seventh IEEE/ACM International Symposium on Networks-on-Chip (NoCS); 2013. p. 1–8.

[8] Wang AY, Sodini CG. On the energy efficiency of wireless transceivers. 2006 IEEE International Conference on Communications, ICC'06, Vol. 8; 2006. p. 3783–3788.

[9] An Y, Zeng B, Zhang Y, et al. Reliable p-median facility location problem: two-stage robust models and algorithms. Transp Res B Methodol. 2014;64:54–72.

[10] Wong IC, Oteri O, McCoy W. Optimal resource allocation in uplink SC-FDMA systems, wireless Communications. IEEE Trans. 2009;8(5):2161–2165.

[11] Hoseiny Farahabady M, Sarbazi-Azad H. The recursive transpose-connected cycles (RTCC) interconnection network for multiprocessors. Proceedings of the 2005 ACM Symposium on Applied Computing; 2005. p. 734–738.

[12] Wang C, Bagherzadeh N. Design and evaluation of a high throughput QoS-aware and congestion-aware router architecture for network-on-chip. Euromicro International Conference on Parallel, Distributed and Network-Based Processing; 2014. IEEE. p. 457–464.

[13] Ouyang Y, Li Z, Xing K, et al. Design of low-power WiNoC with congestion-aware wireless node. J Circuits Syst Comput. 2018;27(09):1850148.

[14] Chidella KK, Asaduzzaman A. A novel wireless net work-on-chip architecture with distributed directories for faster execution and minimal energy. Comput Electr Eng. 2018;65:18–31.

[15] Kumar JCR, Kanagaraj M. Enhanced TACIT algorithm based on Charl's table for secure routing in NoC architecture. J Comput Theor Nanosci. 2017;14(12):5680–5685.

[16] Ravenstahl M, Kopp M. Application brief: ANSYS HFSS for ECAD; 2013.

[17] Oberg J, Robino F. A NoC system generator for the sea-of-cores era. Proceedings of the 8th FPGAWorld Conference; 2011. ACM.