Contents lists available at ScienceDirect





Electric Power Systems Research

journal homepage: www.elsevier.com/locate/epsr

Control strategy of transfer branch for reducing peak value of DCCB breaking current

control strategy.



Zhenhao Wang, Zhaojing Hou*, Long Cheng, Wei Wang, Guoqing Li

Department of Electrical Engineering, Northeast Electric Power University, Jilin 132012, China

ARTICLE INFO	A B S T R A C T
Keywords: High-voltage DCCB Transfer branch Fault current Breaking strategy	A high-voltage DC circuit breaker is one of the key equipment that constructs the DC power grid. Therefore, reducing the peak value of the breaking current and shortening the fault removal time are the main research directions for its performance optimization. This paper first analyzes the basic topology and the traditional breaking strategy of a hybrid high-voltage DC circuit breaker with forced current commutation. Then, the theoretical analysis of the fault current, voltage, and the relationship between the withstand voltage level of the fast mechanical switch and the exit time of the transfer branch, is conducted. A new breaking strategy is proposed, which can effectively reduce the peak value of the breaking current by turning off the transfer branch step by step. When a fast mechanical switch reaches the corresponding withstand voltage level, it sends the OFF signals to each sub-module of the transfer branch; thus, the energy consumption of the DC circuit breaker is reduced and the fault removal time is shortened. Finally, the PSCAD/EMTDC simulation platform is used to build

1. Introduction

In order to alleviate the global energy crisis, a variety of distributed renewable clean energy is connected to the grid through the Voltage Source Converter based High-Voltage Direct Current (VSC-HVDC) transmission system. VSC-HVDC has received widespread attention and experienced rapid development [1–5]. Compared with the traditional AC power grid, the VSC-HVDC has the characteristics of low damping. Namely, after a fault occurs at the same time scale, the fault current in VSC-HVDC develops more rapidly, and the influence range widens [6,7]. When only the AC side breaker is used to prevent a DC fault, the multi-terminal or mesh system without a fault area will be affected [8,9]. Therefore, in order to adapt to the future development trend of a large-capacity high-voltage VSC-HVDC, and ensure safe and reliable operation of the multi-terminal and mesh systems, a high-voltage DC circuit breaker (DCCB) that can quickly isolate the DC line faults and improve its key performance is urgently needed.

The DCCB can be divided into three main types, which are mechanical DCCB, solid-state DCCB, and hybrid DCCB. The hybrid DCCB combines the advantages of the first two. It has the advantages of small on-state loss, strong arc extinguishing ability, fast breaking speed, and reliable operation [10–15]. Hybrid DCCB is the essential building block for selective protection and thus system stability in VSC-HVDC [16]. Therefore, it has a good application prospect [8]. In 2012, company ABB proposed a typical hybrid DCCB based on the parallel principle of power electronic switch groups and fast mechanical switches, and conducted the prototype test of 80 kV/2.6 kA in the same year. The breaking time of this prototype is 5 ms, and the peak value of breaking current is 9 kA [17–19].

the test system, which verified the effectiveness of current limiting and other functions of the proposed breaking

At present, the research on hybrid DCCB mainly focuses on its faultbreaking time, the peak value of the fault current, current-limiting capability and total energy consumption during the breaking process. The demand for optimization of its performance can be improved in both the topology and the control strategy. A novel topology for current limiting DCCB is proposed in [20]. The topology can flexibly select the number of inductive branches. With the increase of the number, the effect of current restriction increases. A rapid fault detecting method and a pre-transferring strategy based on the cascaded full-bridge DCCB topology were proposed in [21], thereby reducing the breaking time of a CB. [22] proposed an high-voltage DCCB with no on-state loss and features bi-directional interruption, which can provide similar performance to classical hybrid high-voltage DCCB at relatively lower costs. For a typical hybrid DCCB, the control strategy can be taken as a research object to achieve the purpose of limiting current. A short-duration DC fault current limiting model is introduced in [8]. It limits the failure current to a constant value greater than the rated current after

https://doi.org/10.1016/j.epsr.2020.106832

Received 14 February 2020; Received in revised form 29 July 2020; Accepted 18 August 2020 Available online 25 August 2020 0378-7796/ © 2020 Elsevier B.V. All rights reserved.

^{*} Corresponding author. *E-mail address:* elainehou0306@163.com (Z. Hou).

the failure current drops, which provides an advantage for reclosing. In [23], a sequential switching strategy for hybrid DCCB is proposed to improve transients during DC fault interruption in multi-terminal high voltage direct current grids. In [24], a breaking and simulation method of arresters based on step-by-step operating was proposed to solve the problem of long action time of a fast mechanical switch. However, the existing control strategies for typical topologies cannot well limit the rise rate of the fault current, and thus cannot effectively reduce the total energy consumption.

In order to overcome the problems mentioned above, this paper proposes a step-by-step exit strategy of a transfer branch, which is beneficial to reduce the peak value of the breaking current of a hybrid DCCB. The paper begins by introducing the advantages of hybrid DCCB, its topology, and its traditional operation during breaking. Then, the method of step-by-step opening the solid-state insulated-gate bipolar transistor switch (ss-IGBT-s) sub-modules of the transfer branch according to the withstand voltage of the mechanical switch is introduced. To verify the validity and the feasibility of the proposed control strategy, the simulation studies in PSCAD/EMTDC and experiment validation are presented. The main contributions are as follow:

- 1) In the proposed breaking strategy, the transfer branch exits the operation step-by-step after the fast mechanical switch is opened to a safe distance. This is different from the operation of the branch in the traditional breaking strategy. The proposed breaking strategy can significantly reduce the peak value of the breaking current and shorten the fault removal time simultaneously. Accordingly, system safety and reliability can be effectively improved.
- 2) Under the breaking strategy which proposed in this paper, the energy absorbed by each arrester is reduced, and the total energy absorbed by the energy consumption branch is also significantly reduced. The life of the arresters can be extended to different degrees according to the order of operation. It can effectively protect the system to operate safely and reliably while reducing the cost.
- 3) Simulations are performed for different numbers of ss-IGBT-s submodules in the transfer branch. A comparative analysis of the results shows that when the number of sub-modules increases to five groups, the peak value of the fault current reduces significantly. When the number of sub-modules continues to increase, the peak value of the fault current will not continue to decrease accordingly, but increases the number of internal components of the circuit breaker and the complexity of the breaking control.

2. Topology and working principle of hybrid DCCB

2.1. Topology of hybrid DCCB

The basic topology of a hybrid high-voltage DCCB with forced current commutation is presented in Fig. 1 [8,16]. As shown in Fig. 1, it consists of a main current branch, a transfer branch, and an energy consumption branch, which are connected in parallel. The main current branch is composed of a fast mechanical switch and a ss-IGBT-s sub-

module. The on-state loss of the ss-IGBT-s sub-module of the main current branch is relatively small. Under normal working conditions, current flows through the main current branch. The transfer branch is composed of several ss-IGBT-s sub-modules that are connected in series. In this paper, five ss-IGBT-s sub-modules are used as an example. Compared with the main current branch, the transfer branch has a higher on-state loss. This branch is used to transfer the fault current when breaking the fault. The energy consumption branch is composed of arresters connected in series. It is used to absorb and consume energy when the DCCB breaks the fault current, so it can protect the line from an excessive voltage.

2.2. Working principle of hybrid DCCB traditional breaking

The breaking process of a hybrid high-voltage DCCB with forced current commutation is shown in Fig. 2. The l_1 in Fig. 2 denotes that when a DC line is working normally, the current flows through the main current branch. After the DC-side pole-to-pole fault occurs at t_0 , the breaking process of a DCCB includes the following steps:

- 1) At t_1 the fault current rapidly increases, reaching the preset current value. At this time, the ss-IGBT-s sub-module in the main current branch is turned off. The fault current begins to migrate to the transfer branch, as l_2 in Fig. 2 shown.
- 2) At t₂ the current flowing through the main current branch decreases to the value close to zero, and zero-current breaking of a fast mechanical switch can be realized.
- 3) At t_3 the fast mechanical switch opens to a safe distance, and the ss-IGBT-s sub-modules in the transfer branch are turned off at this time. The fault current starts to release energy from the energy consumption branch to the ground, as l_3 in Fig. 2 shown.
- 4) At t_4 the fault current flowing through the DCCB drops below the security domain value. At this time the DCCB completes the fault breaking work [8].

3. Step-by-step exit strategy of transfer branch

3.1. Calculation of breaking voltage and current in traditional control strategy

A simplified equivalent model of a DC system after a fault occurs is displayed in Fig. 3. The simplified model is used to analyze the changes in voltage and current from when a fault occurs to when the DCCB is successfully disconnected. In Fig. 3, R_C , L_C , and C_C respectively denote the equivalent resistance, inductance, and capacitance of the converter station within a short time after the fault occurs; R_{dc} and L_{dc} denote the equivalent resistance and inductance of the line, respectively; lastly, i_{fault} represents the fault current.

The first stage: When a fault occurs at t_0 , capacitor voltage U_0 and the initial current, which represents the steady-state current denoted as I_{rated} , differ from zero at the moment of the fault, and the current flows in turn through R_{dc} , L_{dc} and the main current branch of the DCCB. Let



Fig. 1. Topology of a hybrid high-voltage DCCB with forced current commutation.



Fig. 2. The breaking process of a hybrid high-voltage DCCB with forced current commutation.



Fig. 3. Simplified equivalent model of a DC system after a fault occurs.

 $R = R_{\rm C} + R_{\rm dc}$ and $L = L_{\rm C} + L_{\rm dc}$. $R \ll 2\sqrt{L/C_{\rm C}}$ in the actual system, so the system discharge process before the DCCB operation is equivalent to an oscillating discharge process with known initial circuit conditions. Then, capacitor voltage $u_{\rm C}(t)$ can be expressed as:

$$u_{\rm C}(t) = e^{-\alpha t} \left[\frac{U_0 \cdot \omega_0}{\omega} \sin(\omega t + \beta) - \frac{\mathrm{I}_{\rm rated}}{C_{\rm C} \cdot \omega} \cdot \sin(\omega t) \right]$$
(1)

where $\alpha = \frac{R}{2L}$, $\beta = \arctan \frac{\omega}{\alpha}$, $\omega = \sqrt{\omega_0^2 - \alpha^2}$, and $\omega_0 = \sqrt{1/(LC_C)}$. Under normal circumstances $(R/2L)^2 \ll 1/(LC_C)$, so we can assume that $\omega \approx \omega_0$.

The fault current i_{fault} can be expressed as:

$$i_{\text{fault}}(t) = e^{-\alpha t} \left[I_{\text{rated}} \cdot \cos(\omega t) + U_0 \sqrt{\frac{C_{\text{C}}}{L}} \cdot \sin(\omega t) \right]$$
(2)

At t_1 , when i_{fault} increases to the preset current value $I_{\text{setting}} = (1.1 \sim 1.5)I_{\text{rated}}$, the ss-IGBT-s sub-module in the main current branch receives the OFF signal, and at this moment, the fault current value is given by:

$$I_{\text{setting}} = e^{-\alpha t_1} \left[I_{\text{rated}} \cdot \cos(\omega t_1) + U_0 \sqrt{\frac{C_C}{L}} \cdot \sin(\omega t_1) \right]$$
(3)

The second stage: The traditional breaking strategy turns on the fast mechanical switch at t_2 when the main current branch current i_{main} drops to the value close to zero; $t_2 = t_1 + \Delta t_{transfer}$, where $\Delta t_{transfer}$ represents the current transfer time. At t_3 , the ss-IGBT-s sub-modules of the transfer branch are turned off to make this branch out of operation, and the fault current releases the energy through the energy consumption branch; $t_3 = t_2 + \Delta t_{switch}$, where Δt_{switch} represents the time required for the fast mechanical switch to open to a safe opening distance, and it is generally about 2 ms [8,25].

The third stage: Starting at t_3 , the arresters start to work when voltage across the arresters in the energy consumption branch denoted as $U_{\rm Ar}$ reaches the arresters' protection voltage denoted as $U_{\rm p}$. The arresters release current to the ground so that the protected line cannot generate an excessive voltage. At this stage, the energy consumption branch is equivalent to *n* reverse DC voltage sources $nU_{\rm p}$, where *n* is the number of ss-IGBT-s sub-modules and the corresponding arresters in the transfer branch.

As shown in Fig. 4, the fault current flowing through the R_{dc} , L_{dc} , and the energy consumption branch of the DCCB, and it can be expressed as:



Fig. 4. Simplified equivalent model of a fault current flowing through the energy consumption branch.

$$i_{\text{fault}}(t) = e^{-\alpha t} \left[i_j \cos(\omega t) + (U_0 - nU_p) \sqrt{\frac{C_C}{L}} \sin(\omega t) \right] + C_j (j = 1, 2, 3, ..., n)$$
(4)

where i_j is the value of the fault current before each arrester is put into operation. Due to different initial current conditions, the constant C_j is different when each arrester is put into operation. Putting each arrester into operation is equivalent to adding one reverse voltage U_p . With the gradual increase of n, " $U_0 - nU_p$ " in the equation decreases, so the rate of rise of the i_{fault} begins to decrease.

After the transfer branch is out of operation, the energy that the energy consumption branch needs to dissipate comes from two sources that are the DC power supply and the equivalent reactance of the line [26,27]. The U-I characteristic curve of the arrester is shown in Fig. 5 [28]. The II stage is regarded as a linear model, and the current flowing through the arrester can be approximately expressed as:

$$I_{\rm Ar} = 10 \frac{-m + \lg U_{\rm Ar}}{M} \tag{5}$$

where m and M are constants related to material and the geometric structure of arresters.

The arresters work in the II stage of Fig. 5, the voltage change in this stage is very small, and its error can be approximately ignored. Therefore, the total dissipated energy W_{Ar} of the energy consumption branch can be approximated by:

$$W_{\rm Ar} = \int_{t_3}^{t_4} U_{clamp} \cdot I_{\rm Ar} dt \tag{6}$$

where U_{clamp} is the clamping voltage of arresters.

The arresters discharge current during the period from t_3 to t_4 , when



Fig. 5. The U-I characteristic curve of the arrester.

the current flowing through the energy consumption branch is reduced to about zero; this period accounts for about 50% of the total DCCB breaking time.

3.2. Calculation of moment when transfer branch exits step-by-step

Fast mechanical switching is one of the important factors affecting the hybrid high-voltage DCCB. Therefore, its opening speed and withstand voltage level U_n should be improved. In order to achieve this, almost all fast mechanical switches in hybrid DCCBs use high-speed operating mechanisms. The opening speed and withstand voltage level $U_{\rm p}$ of the fast mechanical switch determine the start time of the transfer branch, which further affects the peak value of the fault current in the breaking process of a hybrid DCCB.

The movement of a fast mechanical switch represents the coupling process of the electromagnetic field and the structural field. The repulsive electromagnetic force generated in this process pushes the opening coil to accelerate. This acceleration process is the main factor determining the opening speed and the withstand voltage level $U_{\rm p}$ of the fast mechanical switch, and the actual process is very complicated. In order to facilitate the analysis and calculation, the breaking action of the fast mechanical switch is approximately regarded as a uniform acceleration process defined by a distance of d and an acceleration of a, which is expressed as:

$$d = \frac{1}{2}at^2\tag{7}$$

The breakdown voltage U_{break} of the vacuum gap of a fast mechanical switch is related to the opening distance *d*, which is given as:

$$U_{\text{break}} = \begin{cases} K_1 d, \quad d < D\\ K_1 d^{\alpha}, \quad d \ge D \end{cases}$$
(8)

where K_1 denotes the gain coefficient, which changes with the opening distance *d* and constant $\alpha = 0.4 \sim 0.8$ [29]. D is a constant depending on the type of the fast mechanical switch (0 < D < d). The U_{break} increases with the increase of the *d*, but it is not a linear relationship. The U_{break} shows saturation with the increase of the d. Their approximate relationship is shown in Fig. 6 [29,30].

The withstand voltage level U_n of the fast mechanical switch should be less than the breakdown voltage U_{break} of the vacuum gap, which is given by:

$$U_{\rm n} = U_{\rm break}/K_2 \tag{9}$$

where K_2 denotes the protection margin, which is generally between 1.1 and 1.5.

Therefore, the relationship between the withstand voltage level $U_{\rm n}$ of the fast mechanical switch and the breaking time t is expressed as:

$$U_{\rm n} = \begin{cases} Kt^2, & t < \sqrt{\frac{2\mathrm{D}}{a}} \\ Kt^{2\alpha}, & t \ge \sqrt{\frac{2\mathrm{D}}{a}} \end{cases}$$
(10)

where $K = \frac{aK_1}{2K_2}$. When the withstand voltage level U_n of the fast mechanical switch



Fig. 6. The relationship between U_{break} and d.

reaches the protection level of arresters nU_p in the energy consumption branch, the corresponding ss-IGBT-s sub-modules of the transfer branch can be turned off. Taking the time when the fast mechanical switch starts to act as the initial time, the off-time of each ss-IGBT-s submodule in the transfer branch is given by:

$$t_{j} = \begin{cases} \sqrt[2]{\frac{jU_{p}}{K}}, & t < \sqrt{\frac{2D}{a}} \\ \sqrt[2\alpha]{\frac{jU_{p}}{K}}, & t \ge \sqrt{\frac{2D}{a}} \end{cases} (j = 1, 2, 3, ..., n)$$
(11)

where i denotes the number of ss-IGBT-s sub-modules in the transfer branch, that is, the number of the corresponding arrester.

3.3. Breaking process of transfer branch exiting step-by-step

In the breaking strategy proposed in this paper, the ss-IGBT-s submodules of the transfer branch each open sequentially at times determined by the withstand voltage of mechanical switch, which depends on the position of the throw as the switch opens. The time at which each solid state switch should open is determined analytically based on constants related to the mechanical switch, arresters, and the number of IGBT switch modules. The analysis of the fault breaking process when there are five ss-IGBT-s sub-modules in the transfer branch is as follows:

- 1) Under normal operating conditions of a system, the current flows through the main current branch consisting of a fast mechanical switch and a ss-IGBT-s sub-module, as shown by path l_1 in Fig. 2.
- 2) After a DC-side pole-to-pole fault occurs at t_0 , the fault current rises rapidly. At t_1 , the fault current value increases to $I_{setting}$, and the ss-IGBT-s sub-module in the main current branch is turned off. Then, the fault current begins to flow through the transfer branch, as shown by path l_2 in Fig. 2.
- 3) At t_2 , the current flowing through the main current branch decreases to about zero. The fast mechanical switch receives the breaking signal to achieve its zero-current breaking function. To this point, the DCCB action process is the same as the traditional breaking strategy.
- 4) According to Eq. (11), the ss-IGBT-s sub-modules T₁, T₂, T₃, T₄, and T_5 in the transfer branch as shown in Fig. 7 are turned off at times t_{3-1} , t_{3-2} , t_{3-3} , t_{3-4} , and t_{3-5} , respectively; and the corresponding current flow paths are l_{3-1} , l_{3-2} , l_{3-3} , l_{3-4} , and l_{3-5} , as shown in Fig. 7.
- 5) At t'_4 , the fault current drops below the preset safety limit, and the DCCB completes the fault breaking operation.

Compared with the traditional breaking strategy, the proposed breaking strategy is based on the theoretical calculation, and the ss-IGBT-s sub-modules of the transfer branch are withdrawn at a reasonable time in advance. Therefore, this breaking strategy limits the increase of the fault current and shortens the DCCB fault breaking time.

4. Simulation analysis

In order to verify the effectiveness and superiority of the proposed step-by-step exit strategy of the transfer branch during the DCCB disconnection process, the PSCAD/EMTDC simulation software was used to build a two-terminal HVDC system simulation model, which is shown in Fig. 8. By setting a DC-side pole-to-pole fault, the step-by-step exit strategy of the transfer branch and the traditional breaking strategy of the hybrid high-voltage DCCB with forced current commutation were simulated, and the obtained results were compared. The simulation parameters of the two-terminal HVDC system and DCCB are given in Table 1.



Fig. 7. The current flow path when the transfer branch exits step-by-step.



Fig. 8. A two-terminal HVDC simulation system model.

Table 1.

Simulation pa	arameters of the	two-terminal	HVDC system	and DCCB.
---------------	------------------	--------------	-------------	-----------

Parameter Name	Value
Rated System Voltage (kV) Rated System Current (kA) Rated System Power (MW) Equivalent System Resistance (Ω) Setting Current Value (kA) IGBT On-state Resistance of the Main Current Branch (Ω) IGBT On-state Resistance of the Transfer Branch (Ω) Rated Voltage of Arrester (kV)	± 100 0.75 300 133.33 1.056 0.001 0.01 16
Protection Level of Arrester (kV)	160

4.1. Simulation of traditional breaking strategy

In a two-terminal HVDC system, a DC-side pole-to-pole fault occurred at 2 s. After the fault current flowing through the hybrid highvoltage DCCB with forced current commutation increased to I_{setting}, the traditional breaking strategy started. For the DCCB1 in Fig. 8, the fault current, voltage across the DCCB, and energy absorbed by the energy consumption branch during the breaking process using the traditional breaking strategy were as shown in Fig. 9. In Fig. 9, i_{main} is the current of the main current branch, i_{Σ} is the sum of current $i_{transfer}$ of the transfer branch and current i_{absorb} of the energy consumption branch; U_{DCCB} is the voltage of the DCCB, and *Energy* is the energy absorbed by the energy consumption branch.

As shown in Fig. 9(a), i_{main} started to increase after the DC-side poleto-pole fault occurred at $t_0 = 2$ s. At , i_{main} reached the preset current value I_{setting} = 1.056kA. At this time, the ss-IGBT-s sub-module in the main current branch received the OFF signal, and the fault current started to migrate to the transfer branch. The presented phase denoted the first commutation in the DCCB, and i_{main} started to increase, while i_{Σ} decreased. At $t_2 = 2.00016$ s, all fault currents were transferred to the transfer branch, and the fast mechanical switch in the main current branch achieved zero-current breaking. After a delay of 2 ms, at $t_3 = 2.00216$ s, the fast mechanical switch opened to a safe distance. At this time, the OFF signal was issued to the ss-IGBT-s sub-modules in the transfer branch, and U_{brk} starts to rise to about 104.4 kV (U_{brk} is the voltage across the fast mechanical switch, as shown in Fig. 10.). i_{Σ} starts to decrease from t_3 until it drops to the value close to zero at $t_4 = 2.00589$ s, and the DCCB completed the fault breaking operation.

It can be known from Fig. 9(b) that at the beginning of the fault at t_0 , U_{DCCB} is still zero until the ss-IGBT-s sub-module in the main current branch receives the OFF signal. U_{DCCB} rises to about 0.79 kV between t_1 and t_2 , and rises to about 3.28 kV at t_3 . At t_3 , due to the operation of the arresters in the energy consumption branch, U_{DCCB} quickly increased to about 156.65 kV and then gradually decreased. At t_4 , the arresters complete the energy release work, and U_{DCCB} drops and stays around 100 kV.

As shown in Fig. 9(c), during the period from t_3 to t_4 , the total energy absorbed by the arresters in the energy consumption branch of the DCCB1 was about 1200 kJ.

The voltage and absorbed energy of each arrester under the traditional breaking strategy are shown in Fig. 11. As shown in Fig. 11(a), the voltage of each arrester rises to 31.3 kV when it is put into operation at t_3 . At this time, the arresters start to absorb energy, and each arrester



Fig. 9. The simulation results of current, voltage, and energy of the traditional breaking strategy.



Fig. 10. The voltage of the mechanical switch in the traditional breaking strategy.

absorbs 240 kJ of energy until t_4 , as shown in Fig. 11(b).

Fig. 12 shows the control sequence of ss-IGBT-s sub-modules and fast mechanical switch in the traditional breaking strategy.

4.2. Simulation of step-by-step exit strategy of transfer branch

In the traditional breaking strategy, after the mechanical switch is opened to a safe distance, the OFF signal is uniformly sent to the ss-IGBT-s sub-modules in the transfer branch. The difference of the proposed strategy is that the ss-IGBT-s sub-modules T_1 , T_2 , T_3 , T_4 , and T_5 in the transmission branch are respectively given OFF signals.



Fig. 11. The voltage and absorbed energy of each arrester under the traditional breaking strategy.



As shown in the waveforms from 2 s to 2.00016 s in Figs. 9(a) and 13(a), the operation process of the main current branch is the same under this breaking strategy and the traditional breaking strategy. After the fast mechanical switch was opened under zero-current conditions, the ss-IGBT-s sub-modules T₁, T₂, T₃, T₄, and T₅ in the transfer branch were turned off at $t_{3-1}=2.000872s$, $t_{3-2}=2.001168s$, $t_{3-3}=2.001465s$, $t_{3-4}=2.001763s$, and $t_{3-5}=2.002158s$, respectively. During the period from t_{3-1} to t_{3-5} , the voltage U_{brk} rises step by step (as shown in Fig. 14), and the final voltage peak is 103.5 kV, which is almost the same as that under the traditional breaking strategy. i_{Σ} decreased to the value close to zero, and the DCCB completed the fault breaking operation at $t_4' = 2.00470s$. i_{fault} is the calculation result of Eq. (4). It can be seen that the result is close to the simulation result.

As shown in Fig. 13(b), U_{DCCB} increased gradually from t_{3-1} , and at t_{3-5} . The peak value of U_{DCCB} is about 155.86 kV. U_{DCCB} starts to decline slowly from t_{3-5} . At $t_4^{'}$, U_{DCCB} dropped to about 100 kV and remained stable.



Fig. 13. The results of current, voltage, and energy of the step-by-step exit strategy of the transfer branch.



Fig. 14. The voltage of the mechanical switch in the step-by-step exit strategy of the transfer branch.

As illustrated in Fig. 13(c), the arresters in the energy consumption branch of the DCCB1 under the step-by-step exit strategy of the transfer branch absorbed about 774 kJ of the energy during the period from t_{3-1} to t'_4 .

The voltage and absorbed energy of each arrester under the step-bystep exit strategy of the transfer branch are shown in Fig. 15. Each arrester assumes a voltage of approximately 31.2 kV when it is put into operation. This voltage is opposite to the direction of the system voltage, which is U_p . The energies E_1 , E_2 , E_3 , E_4 , and E_5 absorbed by the arresters that corresponded to the ss-IGBT-s sub-modules T_1 , T_2 , T_3 , T_4 ,



Fig. 15. The voltage and absorbed energy of each arrester under the step-bystep exit strategy of the transfer branch.

and T_5 of the transfer branch during the fault current breaking process are shown in Fig. 15(b). According to the sequence, the energy absorbed by all the arresters was decreasing gradually.

When the transfer branch exited step by step, the fault current was commutated in the ss-IGBT-s sub-modules T_1 , T_2 , T_3 , T_4 , and T_5 , and the corresponding arresters in the energy consumption branch respectively. This stage denoted the second commutation inside the DCCB. The current exchange process between the two branches is shown in Fig. 16.

By comparing the results shown in Figs. 9 and 13, it can be seen that the proposed strategy is better than the traditional breaking strategy. In order to reduce the peak value of the breaking current and shorten the fault removal time, the proposed strategy sends a turn-off signal to each ss-IGBT-s sub-module after determining that the fast mechanical switch has reached the corresponding withstand voltage level. This can make the arresters start to operate early and effectively reduce the energy they need to consume. Therefore, the peak value of the fault current is reduced to about 2.92 kA, and the breaking process of the DCCB is shortened to about 4.70 ms; the energy absorbed by the energy consumption branch dropped to about 774 kJ. Through the data comparison of the two strategies in Table 2, it can be seen that the proposed strategy has obvious optimization effects in all aspects.

Fig. 17 shows the comparison of the fault current when there are different numbers of ss-IGBT-s sub-modules in the transfer branch. As shown in Fig. 17, the peak value of the fault current decreases as the number of ss-IGBT-s sub-modules of the transmission branch increases. The early exit of the first ss-IGBT-s sub-module of the transfer branch can effectively reduce the peak value of the fault current. The greater the number of ss-IGBT-s sub-modules in the transfer branch, the smaller the protection level assumed by the arrester corresponding to each submodule. As Fig. 17 shows, when the number of ss-IGBT-s sub-modules in the transfer branch increased to five groups, the peak value of the fault current was significantly reduced. The increasing number of submodules does not continue to reduce the peak value of the fault current, but increases the number of DCCB internal components and the complexity of the disconnection control. Accordingly, it would be the most appropriate to set the number of ss-IGBT-s sub-modules in the transfer branch to five.



Fig. 16. Current exchange process between the transfer branch and energy consumption branch.

Table 2.

Performance comparison of different control strategies.

	Peak Value of Current (kA)	OFF Time (ms)	Absorbed Energy (kJ)
Traditional breaking strategy The step-by-step exit strategy of transfer branch Optimized amount	4.46 2.92 34.53%	5.89 4.70 20.20%	1200 774 35.50%



Fig. 17. Comparison of the fault current at a different number of ss-IGBT-s submodules.

5. Conclusion

This paper introduces the basic topology and traditional breaking strategy of the hybrid high-voltage DCCB with forced current commutation. The voltage and current during the breaking process and the relationship between the withstand voltage level of the fast mechanical switch and its opening time are analyzed. Therefore, a step-by-step exit strategy of the transfer branch, which is beneficial to reduce the peak value of the breaking current of a hybrid DCCB, is proposed. A twoterminal flexible unipolar DC power system model is built by the PSCAD/EMTDC simulation platform. In the built model, a DC-side poleto-pole fault on the DC side is set up to verify the effective eness of the step-by-step exit strategy of the transfer branch. The simulation is conducted for different numbers of ss-IGBT-s sub-modules in the transfer branch to determine an optimal number of sub-modules in the transfer branch. According to the sequence of the withdrawal operation, the energy absorbed by the arrester corresponding to each ss-IGBT-s sub-module in the transfer branch is gradually decreasing. The total energy absorbed by the energy consumption branch, and the peak value of the fault current are reduced in an approximate proportion. The proposed strategy provides a safe and reliable system operation while extending the arrester's life.

The analysis results prove that by setting an appropriate number of ss-IGBT-s sub-modules in the transfer branch, the transfer branch can be gradually withdrawn at the corresponding time after a DC-side pole-topole fault occurs. Compared with the traditional breaking strategy, this strategy can limit the rise rate of the fault current, so as to significantly reduce the peak value of the fault current, shorten the fault breaking time and reduce the energy consumed by the arrester.

Credit author statement

Zhenhao Wang: Supervision, Writing- Reviewing and Editing; Zhaojing Hou *: Conceptualization, Methodology, Writing - Original Draft;

Long Cheng: Writing- Reviewing and Editing; Wei Wang: Software, Data curation, Formal analysis; Guoqing Li: Project administration.

Declaration of Competing Interest

None.

Acknowledgments

This work was supported by the National Key Research and Development Program of China under grant no. 2018YFB0904600.

Appendix

Table A

Actorights and nonnenciatur.			
DC	Direct Current		
AC	Alternating Current		
DCCB	DC circuit breaker		
VSC-HVDC	Voltage Source Converter based High Voltage Direct Current Transmission		
PSCAD/EMTDC	Power Systems Computer Aided Design/Electromagnetic Transients including DC		
ss-IGBT-s	solid-state insulated-gate bipolar transistor switch		

References

 W Xinglong, X Liang, Y Jian, et al., Design method for strengthening high-proportion renewable energy regional power grid using VSC-HVDC technology, Electr. Power Syst. Res. 180 (2019) 106160.

Table A.

- [2] R Oliveira, A Yazdani, A modular multilevel converter with DC fault handling capability and enhanced efficiency for HVdc system applications, IEEE Trans. Power Electron. 32 (1) (2017) 11–22.
- [3] N Flourentzou, VG Agelidis, GD Demetriades, VSC-based HVDC power transmission systems: an overview, IEEE Trans. Power Electron. 24 (3) (2009) 592–602.
- [4] G Minyuan, X Zheng, Modeling and control of a modular multilevel converter-based HVDC system under unbalanced grid conditions, IEEE Trans Power Electron. 27 (12) (2012) 4858–4867.
- [5] D Suman, Q Jiangchao, B Behrooz, et al., Operation, control, and applications of the modular multilevel converter: a review, IEEE Trans. Power Electron. 30 (1) (2015) 37–53.
- [6] T Lanxi, D Xinzhou, S Shenxing, et al., A high-speed protection scheme for the DC transmission line of a MMC-HVDC grid, Electr. Power Syst. Res. 168 (2018) 81–91.
- [7] K Yulin, L Yong, W Weiyu, C Yijia, A virtual synchronous generator control strategy for VSC-MTDC systems, IEEE Trans. Energy Convers. 33 (2) (2018) 750–761.
- [8] L Weixing, J Dragan, N Samuel, et al., Modelling of high-power hybrid DC circuit breaker for grid-level studies, IET Power Electron. 9 (2) (2016) 237–246.
- [9] Z Shuo, Z Guibin, L Bowei, et al., Fault property identification method and application for MTDC grids with hybrid DC circuit breaker, Int. J. Electr. Power Energy Syst. 110 (2019) 136–143.
- [10] L Siyuan, P Marjan, Development of HVDC system-level mechanical circuit breaker model, Int. J. Electr. Power Energy Syst. 103 (2018) 159–167.
- [11] Q Lu, Y Zhanqing, H Yulong, et al., Research on effect of circuit parameters on breaking characteristics of mechanical DC circuit breaker, Electr. Power Syst. Res. 179 (2020) 1–8.
- [12] R Bartosz, B Gerd, H Martin, et al., Timings of high voltage circuit-breaker, Electr. Power Syst. Res. 78 (2008) 2011–2016.
- [13] X Zheng, X Huangqing, X Yuzhe, et al., Two basic ways to realise DC circuit breakers, J. Eng. 16 (2019) 3098–3105.
- [14] M Yueyang, Z Guibin, S Shenglan, et al., Novel fault current-limiting scheme for MMC-based flexible HVDC system, J. Eng. 16 (2019) 2233–2238.
- [15] Chuan D, Can W. Review of DC circuit breaker technology for HVDC application. In 2019 22nd International Conference on Electrical Machines and Systems (ICEMS), Harbin, China.
- [16] Derakhshanfar R, Jonsson TU, Steiger U, et al. Hybrid HVDC breaker a solution for

future HVDC system. In 2014 CIGRE Session 45 - 45th International Conference on Large High Voltage Electric Systems. Paris, France.

- [17] A Hassanpoor, J Häfner, B Jacobson, Technical assessment of load commutation switch in hybrid HVDC breaker, IEEE Trans Power Electron. 30 (10) (2015) 5393–5400.
- [18] J Häfner, Proactive hybrid HVDC breakers a key innovation for reliable HVDC grids, Proc CIGRE Bologna Symposium, 2011.
- [19] Häfner J, Hassanpoor A. HVDC hybrid circuit breaker with snubber circuit. WO, US8891209[P]. 2014.
- [20] L Shuai, Z Jiyuan, X Jianzhong, et al., A new topology for current limiting HVDC circuit breaker, Int. J. Electr. Power Energy Syst. 104 (2018) 933–942.
- [21] Jinkun K, Xiaoguang W, Bingjian Y, Yang G, Zhiyuan H. Control strategy of the fullbridge based hybrid DC breaker. In 2015 IEEE First International Conference on DC Microgrids (ICDCM). Atlanta, GA.
- [22] Kim BC, Chung YH, Hwang HD, et al. Development of HVDC circuit breaker with fast interruption speed. In 2015 9th International Conference on Power Electronics and ECCE Asia (ICPE 2015-ECCE Asia). Seoul, South Korea.
- [23] S Ying, S Jingfan, S Maryam, J Shengchang, et al., Reducing the fault-transient magnitudes in multiterminal HVdc Grids by sequential tripping of hybrid circuit breaker modules, IEEE Trans. Ind. Electron. 66 (9) (2019) 7290–7299.
- [24] W Xueguang, W Xiaochen, Z Yongqiang, et al., Breaking and simulation method of arrestors step-by-step operating of high voltage DC circuit breaker, High Volt. Eng. 43 (4) (2017) 1079–1085 (in Chinese).
- [25] AM Juan, M Jesper, Parametric analysis of the hybrid HVDC circuit breaker, Int. J. Electr. Power Energy Syst. 84 (2017) 284–295.
- [26] J Magnusson, R Saers, L Liljestrand, et al., Separation of the energy absorption and overvoltage protection in solid-state breakers by the use of parallel varistors, IEEE Trans. Power Electro. 29 (6) (2014) 2715–2722.
- [27] Sander R, Leibfried T. Considerations on energy absorption of HVDC circuit breakers. In: 2014 49th International Universities Power Engineering Conference (UPEC). Cluj-Napoca, Romania.
- [28] C Yancheng, W Qilin, Y Hanwu, et al., A method of creating the high-voltage circuit model of metal-oxide varistor for the simulation of square pulse forming, IEEE Trans. Circuits Syst. II-Express Briefs 67 (3) (2019) 526–530.
- [29] Paul G. Slade, The Vacuum Interrupter Theory, Design and Application, CRC Press, Taylor & Francis Group,, New York, 2008 ISBN 0-8493-9091-5.
- [30] S Giere, HC Karner, H Knobloch, Dielectric strength of double and single-break vacuum interrupters - experiments with real HV demonstration bottles, IEEE Trans. Dielectr. Electr. Insul. 8 (1) (2001) 43–47.