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TRANSPARENT OXIDE SEMICONDUCTORS GATE BASED MOSFETS FOR SENSOR APPLICATION

by

ASHWIN KUMAR SAIKUMAR
B.S. Anna University, 2012

A thesis submitted in partial fulfilment of the requirements
for the degree of Master of Science
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2014

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ABSTRACT

Starting from small scale laboratories to the highly sophisticated industrial facilities, monitoring and control forms the most integral part. In order to perform this continuous monitoring we require an interface, that would operate between the system and its processing conditions and in turn which facilitates us to act accordingly. This interface is called as a sensor. There are various types of sensors available which have wide range of functionality in various different fields.

The use of transparent conducting oxide (TCO) in the field of sensor applications has increased and has been the subject of extensive research. Good electrical properties, good optical properties, wide band gap, portability, easy processing, and low cost has led to the extensive research on TCO for sensor applications.

For this research purpose two specific types of sensor applications namely, light sensing and humidity sensing were considered. For this purpose, two sets of metal−oxide−semiconductor field-effect transistors (MOSFET) with one set having transparent aluminum doped zinc oxide and the other having indium tin oxide respectively as their gate metal was fabricated. The MOSFETs were fabricated using a four level mask and tested.

Dedicated to my parents

ACKNOWLEDGMENTS

Firstly, I would like to acknowledge and immensely thank my advisor Dr. Kalpathy B. Sundaram for all the guidance and support he provided, which was the integral factor in the completion of this work. I would like to thank Prof. Vikram Kapoor and Prof. Thomas Wu for serving on my thesis committee and for their valuable advice and comments that helped me to improve the quality of my thesis. I would also like to thank Narendra Shiradkar of Florida Solar Energy Center who had helped me sputter aluminum doped zinc oxide for my research.

My heartfelt thanks to my research group at University of Central Florida - Giji Skaria, Adithya Prakash, Ritika Oswal . Giji Skaria was instrumental in giving me the preliminary training to use the equipments inside the clean room.

Finally I would like to thank my father Mr. K.R Saikumar and mother Mrs. Bhanu Saikumar for their continuous support and constant motivation. I am highly indebted to them, without them this achievement would not have been possible.

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CHAPTER 1: INTRODUCTION

1.1 Semiconductor Sensors

In this world of ever burgeoning technologies, the need for monitoring and control of the surrounding has become indispensable. For the purpose of monitoring and controlling the factors surrounding a system there is a need for an interface called sensors. The basic requirements for a sensor are: it should be fast, highly selective, simple to fabricate, non-toxic, easy operation, durable and cheap [1]

Sensors can be classified under various different sectors, the semiconductor sensors are the ones we look into. Semiconductor sensors can be defined as materials of semiconductor origin being used for sensing operations. If a semiconductor material is not suitable for a particular sensing application then, another material that facilitates the required sensing operation can be deposited onto a semiconductor material and used.[4]

Semiconductor sensors are famous for their small size and low cost. Many processes used for semiconductor device fabrication can also be used for semiconductor sensor fabrication, thus facilitating large scale production and reduction in the cost. There are many types of semiconductor sensors, we take into consideration two important sensor types namely, humidity sensor and light sensor

1.1.1 Humidity Sensors

Humidity plays a very significant role in numerous operations, thus it has become highly necessary to detect humidity level surrounding a system. Humidity can be classified into two types namely,

relative humidity and absolute humidity. Under relative humidity the amount of moisture present in the air is compared to the maximum content of moisture, air can hold in the same temperature and pressure conditions. Absolute humidity is a more direct measure where it is the ratio of the mass of moisture in the air to total volume of the air.

Humidity sensors are majorly subdivided based on their units into ”Absolute humidity sensors” and ”Relative humidity sensors”, amongst which the relative humidity sensor is more popular. The relative humidity sensors can be further subdivided based on the sensing material and operating mechanism into organic polymer type, semiconductor type and ceramic type. These types of sensors takes into effect the changes in the electrical and physical properties that occurs when the sensor is exposed to moisture. [5]

1.1.2 Gas Sensors

The next important sensor type we look at is the gas sensor. Gas sensors are highly essential for many systems as the presence of many gases in the surrounding can hamper its working. Gas sensors can be classified into three different types namely, field effect transistor (FETs), conductometric and impedometric. In the FET gas sensors, there occurs an interaction between the gas of interest and the FET channel surface resulting in the change in gate bias. The change in gate bias in turns affects other characteristics like threshold voltage, depletion depth etc. Some FET gas sensors have the capability to detect different types of gases as they might have different metal oxide arrays on them.

The conductometric sensor does the required gas detection resulting in a change in the resistance. Based on this resistance changes in the sensor, detection of the target gas becomes possible. The conductometric sensors can be further split into two different types based on their structures namely, single nanowire structured and film type. In the single nanowire type there exists a single

nanowire connecting two metal electrode which is placed on a silicon substrate with a layer of silicon dioxide separating the metal electrode setup and the silicon substrate. The single film type on the other hand consists of a single film made by numerous nanowires being connected by a pair of electrodes placed on a silicon substrate.

The impedometric sensor is similar to the conductometric sensor but it works based on the impedance changes and works under alternating voltages when exposed to the material of interest. The impedometric sensor similar to the conductometric sensor has two structure types namely, single nanowire structured and film type. [6]

CHAPTER 2: METAL OXIDE SEMICONDUCTOR FIELD EFFECT TRANSISTOR (MOSFET)

2.1 Introduction to MOSFET

MOSFET is the abbreviation of metal-oxide-semiconductor field effect transistor. These type of transistors are majorly used for switching operations. These devices have four terminals namely, source, drain, gate, and substrate. Commonly the source terminal and the substrate terminals are internally connected, thus we mainly take three terminals (source, drain and gate) into consideration.

Previously, only metals were used as the gate material, hence its name metal-oxide-semiconductor field effect transistors. MOSFETs can also be fabricated by using polycrystalline silicon as its gate material.

Both the source region and the drain region have the same type of doping when compared to the substrate region which has a different doping type. Based on this difference in the doping types in these regions, two different MOSFET types can be made. If the source and drain regions are doped with n+ type impurities and the substrate is doped with p type impurities, then the MOSFET is called as an n-channel MOSFET or NMOS. If the source and drain regions are doped with p+ type impurities and the substrate is doped with n type impurities, then the MOSFET is called as a p-channel MOSFET or PMOS. The symbols for both the PMOS and the NMOS are shown in the figure below. The gate terminal is a conducting contact plate separated from the substrate by a dielectric oxide materials, most commonly silicon dioxide(SiO_2). The gate oxide material is used in order to avoid leakage currents.

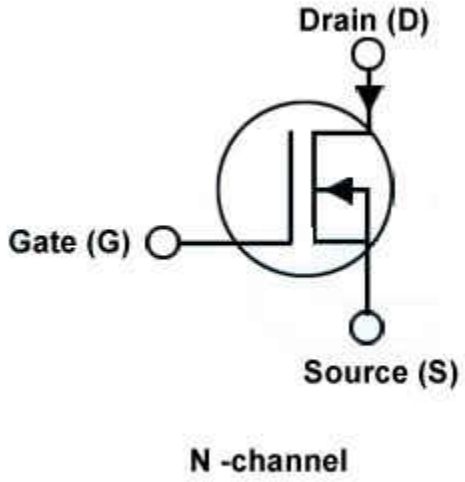

Figure 2.1: NMOS Symbol

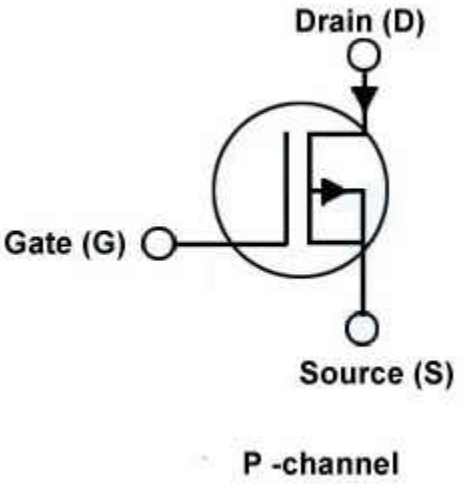

Figure 2.2: PMOS Symbol

2.2 Working Principles of MOSFET

For understanding the working principle of a MOSFET, a n-channel MOSFET is considered. As mentioned above in a n-channel MOSFET, the source and drain regions are doped with n+ type dopants and the substrate is of p type. The cross section of an NMOS is shown below where L is the channel length which is the distance between the source and the drain.

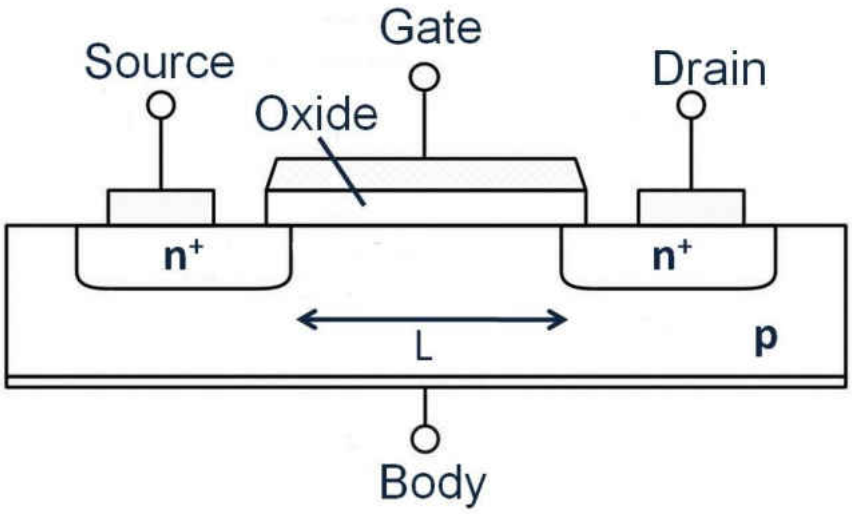

Figure 2.3: NMOS Cross Section

Under normal undisturbed conditions, the different types of dopings are confined to their own regions and there is no shift of impurities happening as shown in the cross section figure above and there is no flow of current from the source region to the drain region. This state is called as the OFF state of a MOSFET, where there is no voltage applied to the gate terminal. In the OFF state, in an NMOS the charge types near the surface of the substrate is of p type and since there is no charge flow between the source and drain there is no flow of current between them.

When positive voltage is applied to the gate terminal, the surface of the substrate gets positively

charged resulting in a repulsion of the holes and an attraction of electrons at the substrate surface. The area between the source and drain region where the repulsion of holes are taking place is called as the depletion region as there is a depletion of holes occurring there. At gate voltage below threshold voltage, there is a low amount of current flowing from the source to drain. This low current is called as leakage currents and the voltage at which they occur is called as subthreshold voltage. For an ideal MOSFET the leakage current should be very low.

If sufficient amount of positive voltage is applied across the gate, then there is an increased accumulation of electrons at the silicon surface thus making the surface n type and resulting in a channel between the source and the drain. This region where the n type accumulation occurs is called as the inversion layer. The channel between the source and the drain facilitates the current flow and this state is called as the ON state of a MOSFET. The voltage value at which there is a formation of the inversion layer is called as the threshold voltage. The current flow between the source and drain can be controlled by modulating the threshold voltage [2].

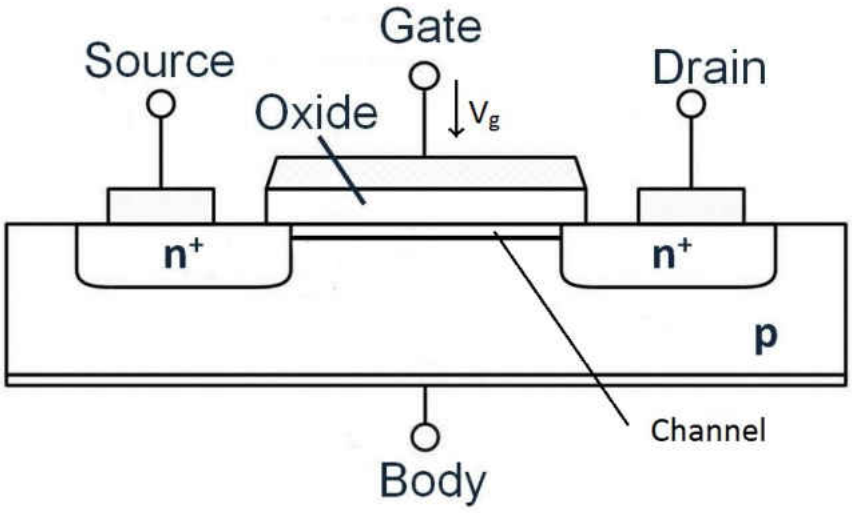

Figure 2.4: NMOS Cross Section With Channel Formation

The inversion layer and the depletion layer exists only till there is enough gate voltage application. When the gate voltage goes below the threshold voltage the channel that was formed between the source and the the drain is lost and the MOSFET returns to how it was during the OFF state, thus making the MOSFET a highly useful switch with quick switching capabilities.

2.3 I-V Characteristics and MOSFET Operating Regions

Before we look at the current vs voltage characteristics its essential to understand what transpires inside the MOSFET during its ON and OFF conditions. There are two types of electric fields acting on a MOSFET during its operation namely, transverse field and lateral field. The transverse field is downward directional and is caused by the application of the gate voltage at the gate region. The lateral field is caused due to the application of drain voltage and is one of the reasons for the flow of current.

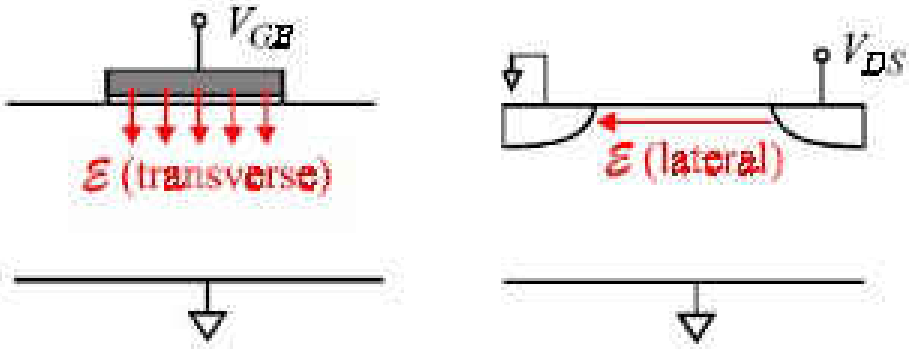

Figure 2.5: Transverse Field and Lateral Field [7]

There are three operating regions for a MOSFET, they are cutoff region, triode region and the saturation region. In the cutoff region, the gate-source voltage (V_{GS}) is less than the threshold

voltage (V_T) and the drain current (I_D) is zero. during such a condition there is only the formation of depletion region and there is no formation of inversion region. Even during the application of drain voltage (V_{DS}) there is no current flow and I_D remains zero since there is no channel formed for the flow of current.

When the value of (V_{GS}) increases more than (V_t), there is enough accumulation of electrons and the inversion region is formed. During such a condition if the (V_{DS}) is zero then due to the absence of the lateral electric field there is no current flow I_D. On application of V_{DS} there starts the flow of current through the channel. This region of operation is called as the tridoe region. With subsequent increase in the V_{DS} results with the loss of the channel density near the drain region and eventually the density becomes very small. This low density point of the channel is called as pinch-off and the V_{DS} value at which pinch-off occurs is called as the saturation voltage (V_{DSsat}).

When the V_{GS} is greater than V_t and V_{DS} is great than V_{DSsat}, the device is said to be in the saturation region. Eventhough with increase in the V_{GS} results in the increase in the channel density, further increase in V_{DS} results in pinch-off. After pinch-off the I_D vs V_{DS} becomes flat. [7][8]

The MOSFET I-V curve is shown below.

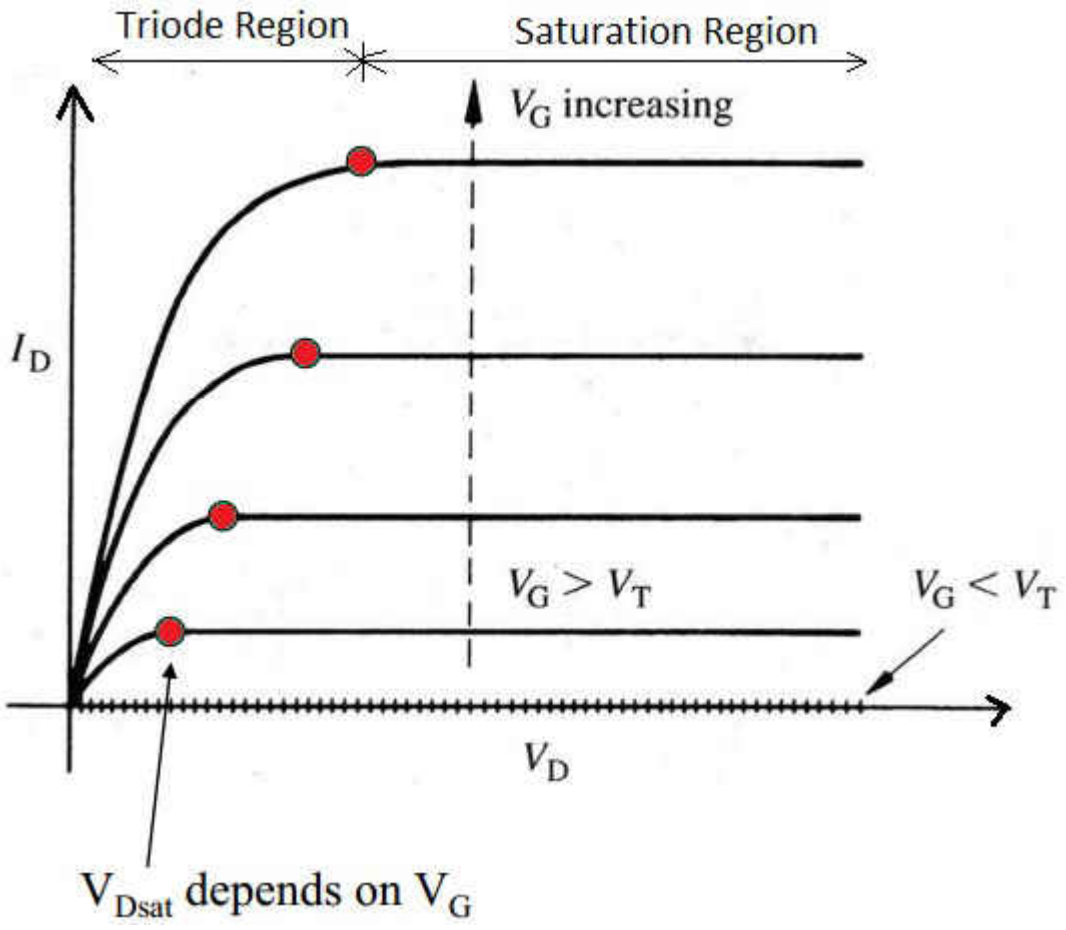

Figure 2.6: MOSFET I-V Characteristics Curve [7]

2.4 MOSFET Treshold Voltage Controlling

Threshold voltage can be defined as the minimum gate voltage required to create a inversion layer (channel) between the source and drain. The formula that is used to calculate the threshold voltage is given below.

$$V_t = -\phi_{ms} + 2\phi_f - \frac{Q_i}{C_i} + \frac{Q_d}{C_i}$$

From the equation given above we can clearly see that the threshold voltage depends on the type

of gate electrode, dielectric capacitance and varying depletion charge.

The threshold voltage can be varied by changing the gate electrode material as V_t depends on ϕ_{ms}. ϕ_{ms} can be varied by changing the gate material by in turn changing their work functions (ϕ_m) since [3],

$\phi_{ms} = \phi_m - \phi_s$

From the threshold voltage formula we can clearly see that V_t is a function of the dielectric capacitance C_i and it is commonly known that C_i is inversely proportional to oxide thickness (d). From the above relations we can say that [3],
$V_t \propto OxideThickness(d)$

The threshold voltage can be controlled by using ion implantation. Ion implantation can be used to perform highly controlled doping in the drain and source regions. By precisely controlling the doping the depletion charge (Q_d) can be controlled [3].

CHAPTER 3: LITERATURE REVIEW

This chapter provides a review of the background of TCO, specially concentrating on the two different types of TCO under consideration for this thesis namely, (Al)-Doped ZnO and ITO.

3.1 Transparent Conductive Oxide

The TCO used for sensor applications have transparency above 80%, band-gap energy of above 3eV, resistivity in the order of $10^{-4}\Omega$cm and a carrier concentration of 10^{20}cm^{-3}.

3.1.1 Aluminum Doped Zinc-Oxide

ITO is generally used for photoelectric applications, but they are expensive owing to the fact that they are not abundantly available. In order to solve this problem, inexpensive materials having nearly the same properties of ITO could become the ideal replacement for ITO. ZnO having good electrical and optical properties and also being non toxic and abundance in nature, was thought as the ideal replacement for ITO. Though sputtered ZnO films have low resistivity and good optical properties comparable to that of ITO, their resistivity tends to get unstable at high temperatures. In order to overcome this drawback, ZnO was doped with Aluminum (Al). (Al)-doped ZnO have stable resistivity at high temperatures. [9]

3.1.1.1 (Al)-Doped ZnO Deposition Technique

ZnO:Al can be deposited by various techniques. Past researches on various ZnO:Al deposition techniques are discussed in this section.

AZO films having resistivities as low as $7\times10^{-4}\Omega$cm and optical transmission in the order of 90% in the visible range were reported by G. Luka et al. The films were grown by atomic layer deposition method from diethylzinc (DEZ) and water vapor as zinc and oxygen precursors, respectively. For the Al doping purpose, trimethylaluminum (TMA) was used. [10]

Using Pulsed laser deposition (PLD) technique at low substrate temperature, Al-doped zinc oxide thin film with resistivity of $5.62\times\ 10^{-4}$ ohm cm and having a transmittance of about 90% was made by Suzuki A et al. For this process ArF laser with $\lambda = 193$ nm. [11]

Highly conducting and transparent Al-doped ZnO were deposited using RF magnetron sputter deposition by T Minami et al. A target with 1-2 wt% of Al_2O_3 and ZnO was used for the sputtering. The films made by this technique were reported to have stable resistivity at different temperatures. [9]

3.1.1.2 (Al)-Doped ZnO Properties

ZnO is a material which has a wide bandgap and a very high binding energy (around 60 meV at room temperature)[12]. Zinc oxide is not an efficient donor and in the undoped state ZnO is highly resistive. In order to get a conductive films ZnO is doped with IIIrd group elements like Ga, In, Ti, Al. Doped ZnO films have high conductivity and good transmittance. ZnO is most commonly doped with Al due to its properties like malleability, durability, ductile, light weight etc.

Al-doped ZnO films have a resistivity in the 10^{-4} range and good films have transmittance of above 85%. Anders et al [12] investigated the optical and electrical properties of Al-doped ZnO thin films and showed that the AZO film quality strongly depends on the growth temperature and marginal improvements were only noticed with post deposition anealing.

Using pulsed filtered cathodic arc technique AZO films of about 200 nm was made by Gao et al

[13] and they also showed that with increase in the anealing temperature from $500^{\bullet}$C to $650^{\bullet}$C the visible transmittance remained almost the same of about 85% but the infrared(780-2500 nm) transmittance improved from 22% to 58% at 600 C and 71% at 650 C. The crystallinity and transmittance increased with high temperature anealing.

3.1.2 Indium Tin Oxide (ITO)

Indium tin oxide is a very widely used and researched semiconductor material. ITO has been widely used in the electronic and optoelectronic industries for making solar cells, flat pannel display etc [14]. Discussions about the various techniques used to deposit ITO and also about the properties of ITO has been done in this section.

3.1.2.1 ITO Deposition Technique

Over the years many methods have been adopted for making ITO thin films. P.D. Szkutnik et al [15] reported the growth of ITO by MOCVD from different indium precursors and tin precursors. The good films produced were reported to have had resistivity of $2.5\times10^{-4}\Omega$cm and a transmittance higher than 84%.

ITO thin films deposition by activated reactive evaporation (ARE) was reported by K. Narasimha Rao et al. The ITO films were deposited by evaporating pure indium and 90% In + 10% Sn alloy using an electron gun in the presence of oxygen ions at ambient temperature. The ITO films deposited had a resistivity of about $6\times10^{-4}\Omega$cm and optical transmission of 85%. [16]

Using PLD technique ITO thin films were deposited by I. A. Petukhova et al. LC 7020 KrF excimer laser ($\lambda = 248$ nm, E = 400 mJ) was used in this process. By adopting this process thin films less than 100 nm this were able to be deposited.

Mehmet Tumerkan Kesim et al [18] reported making ITO films using the sol-gel process. For this process indium ($InCl_3$·4H2O) and tin salts ($SnCl_4$·5H2O) were used as the coating sols. The stable sols were obtained by adding oxalic acid dihydrate ($C_2H_2O_4$·$2H_2O$) to ethanol (C_2H_5OH) and acetylacetone ($C_5H_8O_2$) solvents in different amounts. ITO films with high values of transparency (93%) with a sheet resistance of 3.8 $\pm$ 0.4 kΩ/sqr have been formed by employing coating sols with optimized oxalic acid amount.

3.1.2.2 ITO Properties

ITO thin films have a low resistivity in the range of (10^{-4} - 10^{-3} Ωcm) and high transmission (85 - 90%)in the visible range. [17] Many researches have been taking place in the past to improve the transmittance and also to reduce the resistivity by altering the deposition parameters. In one such research conducted by Guisheng Zhu et al [14] on RF sputtered ITO films it was reported that the the resistivity and transmittance of the films deposited and annealed at temperatures of 500•C, 600•C, 700•C and 800•C was 3.37×10^{-4}, 2.54×10^{-4}, 2.08×10^{-4} and $5.62\times10^{-4}\Omega$cm , and 87.4, 85.3, 83.2 and 74.7 %, respectively.

ITO is a promising material for thermoelectric applications. ITO has very good thermal and chemical stability in air and has the ability to operate at temperatures upto 1400•C [19]. ITO films deposited by K. Narasimha Rao et al by activated reactive evaporation, showed lower resistivity (6×10^{-4}) , higher mobility (3×10^{20} cm^{-3}) and better free carrier concentration (35.6 cm^2/V-s) when compared to indium oxide.

CHAPTER 4: PROCESS METHODOLOGY

Chapter four, also called Methodology presents an overview of the methods used for fabricating the MOSFET devices for further researching on this subject.

4.1 ZnO Gate MOSFET Fabrication

A MOSFET having a gate contact material which is different from that of the source and drain needed to fabricated, for this purpose a four level mask was designed. The MOSFET fabrication was done using this special four level mask. The mask structure and dimensions are given in the Appendix section.

4.1.1 Silicon Type and Cleaning Procedure

A 3" p-type wafer was chosen for the fabrication of the MOSFET. The wafer was cut into 4 nearly equal pie shaped pieces. The silicon wafer data is given in the table below.

Table 4.1: Silicon Data

Type	p
Thickness	350-400 μ
Majority Carriers	Holes
Resistivity	2-7 ohm-cm
Orientation	100 ± 5

For cleaning the silicon wafer, the substrate was initially scrubbed using Alconox (Detergent) and rinsed using De-ionized (DI) water. The purpose of using Alconox is to remove the major contaminant bulk off the substrate. The wafer was then rinsed using Trichloroethylene to completely

remove the residual detergent. Acetone was then used to clean the substrate followed by methanol and DI-water.

Figure 4.1: Cross Section of the Silicon Substrate

4.1.2 Initial Field Oxide Formation

The oxide layer is mainly grown for the purpose of making a masking pattern for the source and drain impurities deposition. For the purpose of oxidation the furnace used was Thermco Mini-Brute, Model MB-71H. The wet oxidation was done at $1100^{\bullet}$C for 45 minutes. Nitrogen at a pressure of 5 Psi was passed into the oxidation furnace tube through a water bubbler. The water temperature inside the bubbler was maintained at $98^{\bullet}$C.

The wafer was loaded onto a quartz boat and fed into the mouth of the furnace tube's mouth with the help of an elephant.The quartz boat was then slowly pushed inside the furnace tube till it reached the furnace center, where the temperature was maximum. The quartz boat is always slowly pushed in before oxidizing and slowly pulled out after oxidizing, in order to prevent a thermal shock on the substrate. The push and pull times of the quartz boat were 3 minutes each.

After the oxidation was completed the color of the wafer was noted to be bluish green which pointed to a thickness of approximately 5200Å on the color chart for SiO_2.

Figure 4.2: Substrate Cross Section After Initial Oxidation

4.1.3 First Level Masking

The first level masking was done to make a well in the SiO_2 layer and reach the silicon top surface.The first level mask structure is shown in the figure below. The purpose of making these wells in the oxide layer is to confine the deposition of phosphorous (n-type dopant) only to the specific source and drain regions. The first level masking was done using NR9-1500 negative photo resist (PR). The substrate was coated with the specified negative PR on top of a spinner and was spun at a speed of 3000 rpm, for 30 seconds.

Once the negative PR was evenly coated on top of the wafer, the wafer was baked inside a oven kept at $150^{\bullet}$C for 1 minute. This process of heating for 1 minute after the application of PR is called as soft baking. Next step in the lithography procedure was ultra violet (UV) exposure, for this purpose, Karl Suss mask aligner MJB3 model was used. The mask was loaded into the mask aligner and the substrate was kept on the chuck and once a hard contact was made with the mask, UV light exposure was done for 10 seconds.

The wafer was again heated in another oven which was kept at $100^{\bullet}$C for 1 minute, this step is called as post exposure baking. The PR was now ready to be developed, thus the wafer was developed in a petridish containing RD6 negative PR developer for 30 seconds and was rinsed with DI water at the 30 second mark. This PR developing stage ensures that the PR is removed

from the areas which were unexposed to the UV light and remain only on the areas which were exposed to UV light. The final step in the first level photolithography process was called as hard baking, where the wafer had to be heated at $150^{\bullet}$C in an oven. Before hard baking the wafer was inspected under the microscope to check if the PR had been properly developed. The sample was finally hard baked at $150^{\bullet}$C for 3 minutes. After the hard baking the wafer was ready to go through etching process.

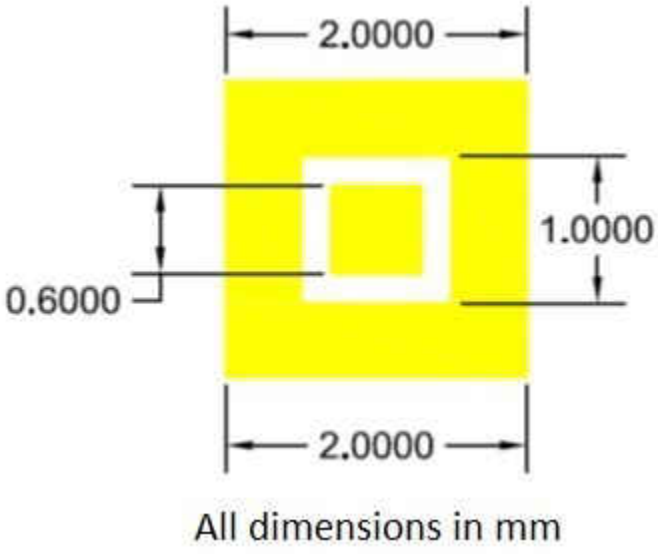

Figure 4.3: First level MOSFET mask structure

4.1.4 Drain and Source Well Oxide Etch

Once the photo resist was developed and the required pattern was attained, the next step in the fabrication process was to etch the SiO_2 to reach the silicon surface. For the purpose of etching, the acid used was, Buffer Oxide Etch (BOE) 9:1. BOE used for etching is a mixture of 40% ammonium fluoride (50 grams NH_4F crystals in 755ml H_2O) and hydrofluoric acid in the ratio of 9:1. The BOE which was used had an etching rate of 600Å. The field oxide was around 5200Å, thus it

took 9 minutes to completely etch the oxide and to reach the silicon surface. Once the etching was done the PR had to be removed. The PR was removed by rinsing with acetone.

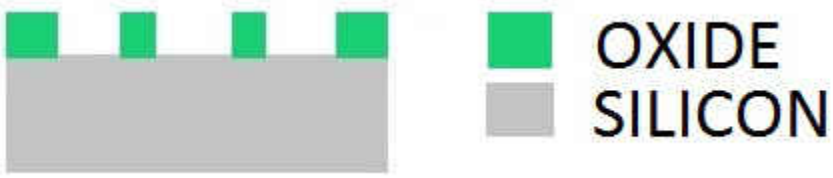

Figure 4.4: Substrate Cross Section After First level Making and Etching

4.1.5 Phosphorous Predeposition and Drive-in

After the field oxide has been patterned, the next step in the fabrication process was the phosphorous (n-type) predeposition. For the predeposition step, the wafer was kept on a quartz boat facing a phosphorous source and was fed into a furnace. The furnace was kept at a temperature of $950^{\bullet}$C and having a nitrogen pressure of 5 psi and flowrate of 4.0 on the flowmeter. The push and pull time was 1 minute each and the boat was kept inside the furnace for 15 minutes. The predeposition step ensured that the dopants were deposited, these dopants had to be driven further inside the silicon substrate.

For driving in the phosphorous dopants further inside we perform the drive-in step. The drive-in step is nothing but wet oxidation again at $1100^{\bullet}$C, nitrogen pressure of 5 psi, flowrate of 1.0 on the flowmeter and the bubbler temperature at $98^{\bullet}$C. The pull and push time for the drive-in step was 3 minute each and the oxidation inside the furnace was done for 20 minutes.

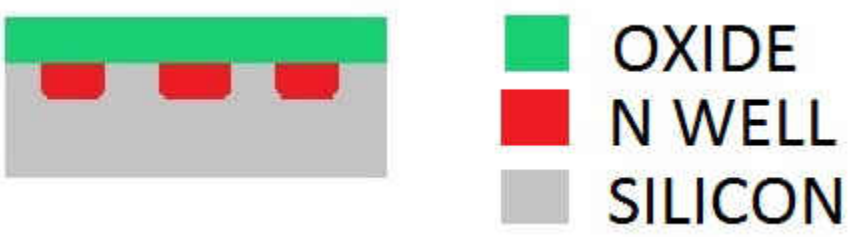

Figure 4.5: Substrate Cross Section After Phosphorous Predoposition and Drive-in

4.1.6 Second Level Masking

The next step in the procedure was to perform second level masking to create a window in the PR for via hole etching. For this second level masking negative photolithography process was again followed. The process parameters for the second level masking is the same as that used for the first level masking. The second level mask was aligned accurately with the previous level inside the Karl Suss mask aligner.

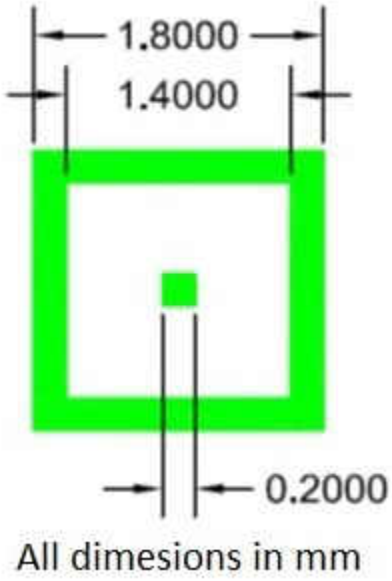

Figure 4.6: Second Level Mask Structure

4.1.7 Via Hole Oxide Etch

The via hole oxide etch step was similar to that performed for the field oxide etch step, but the etch time for this step was different. An oxide layer with thickness of approximately 3400Å was formed after the phosphorous diffusion step, in order to etch this thickness the etching time was calculated to be nearly 6 minutes. The PR was stripped with acetone once the etching was complete.

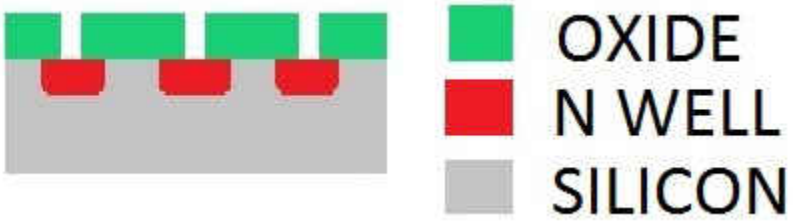

Figure 4.7: Substrate Cross Section After Second level Making and Via Hole Etching

4.1.8 Source and Drain Contact Metallization

The contacts for the source and drain had to be deposited next. For this purpose aluminum was used as the contact material and was deposited by thermal evaporation, which is a a type of physical vapor deposition techniques. An aluminum wire of about approximately 1.5 cm long was used and the evaporation was done at a pressure of about 2×10^{-5} milli-Torr.

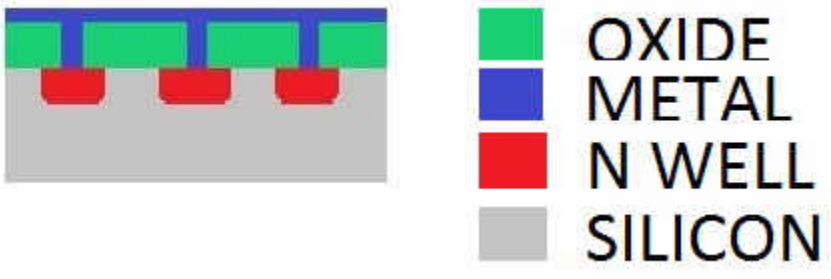

Figure 4.8: Substrate Cross Section After Source and Drain Contact Metallization

4.1.9 Third Level Masking

The aluminum metal that was deposited for making the source and drain contacts needed to be patterned, thus we use the third level masking. For the third level masking, positive photolithography technique was done. The positive PR used for this process was Shipley 1813. After the application of the PR onto the wafer substrate, the wafer was spun at a speed of 3000 rpm for 30 seconds.

The wafer was then soft baked at a temperature of about 100•C for 3 minutes. The wafer was then loaded into the Karl Suss mask aligner, where the third level mask was properly aligned with the previous level. Once the alignment was done accurately, the wafer was exposed to UV light for 10 seconds. The mask pattern on the wafer was checked under the microscope and was then hard baked in an oven at 100•C for 10 minutes. The wafer was then ready to go through the aluminum etching step to drain and source contact patterning.

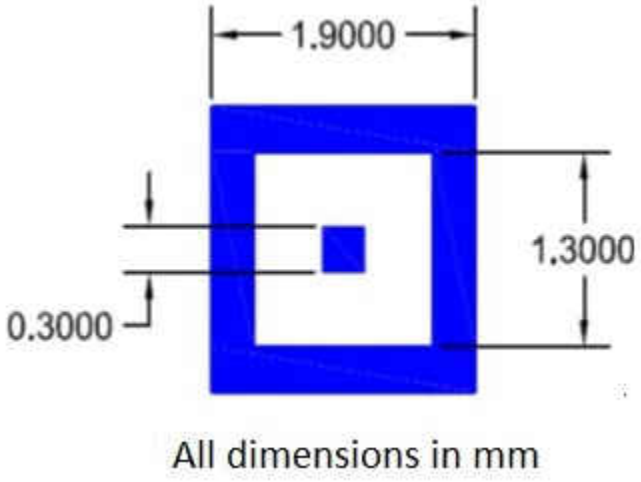

Figure 4.9: Third Level Mask Structure

4.1.10 Source and Drain Contact Patterning

Following the third level masking, the aluminum deposited onto the wafer surface had to be patterned to make the source and drain contacts. The etching of aluminum was done using aluminum etch (16 parts of phosphoric acid, 1 part of acetic acid, 1 part of nitric acid, and 20 parts of DI water) which was heated to about $50^{\bullet}$C. The etch process was stopped when the aluminum was visibly removed from the areas that were not protected by the PR. After the etching process was complete the PR was stripped using acetone.

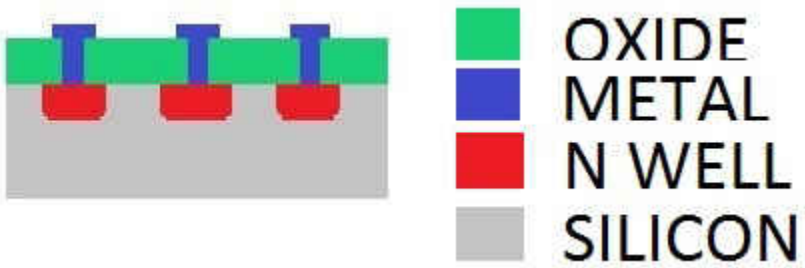

Figure 4.10: Substrate Cross Section After Source and Drain Contact Patterning

4.1.11 (Al)-Doped ZnO Sputtering

After the source and drain contacts were patterned, the gate oxide had to be deposited. In accordance with the research topic, (Al)-Doped ZnO had to be deposited. The method adopted for depositing the gate contact was Radio Frequency (RF) magnetron sputtering. The target that was used for the sputtering process had a composition of ZnO doped with 2 percent aluminum.

The sputtering was done in a sputtering chamber maintained at a pressure of 50 milli-Torr and a RF current of 100 Watts was applied. The Argon flowrate was 20 in the flowmeter. The sputtering

was done for approximately 30 minutes resulting in a (Al)-Doped ZnO thickness of about 1500Å.

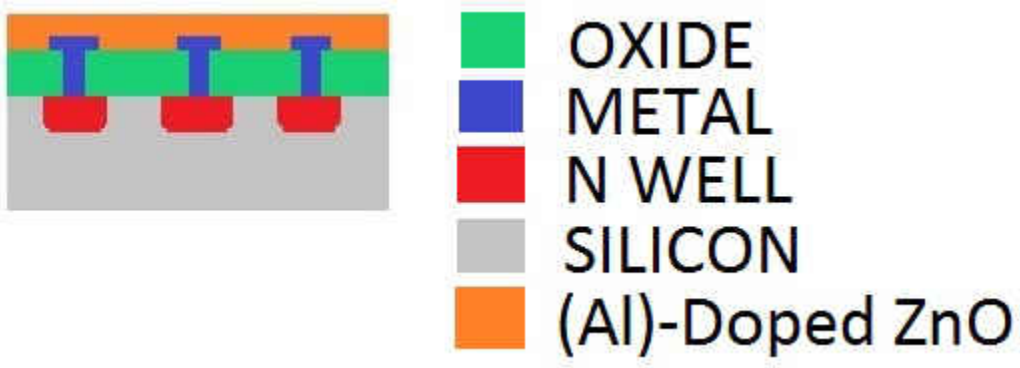

Figure 4.11: Substrate Cross Section After (Al)-Doped ZnO Deposition

4.1.12 Fourth Level Masking

(Al)-doped ZnO was deposited uniformly throughout the wafer surface. This layer of (Al)-doped ZnO needed to be patterned to only the gate contact regions, for this purpose, fourth level masking process was done. The fourth level masking process was done by positive photolithography process and had the same parameters as that followed during the third level masking.

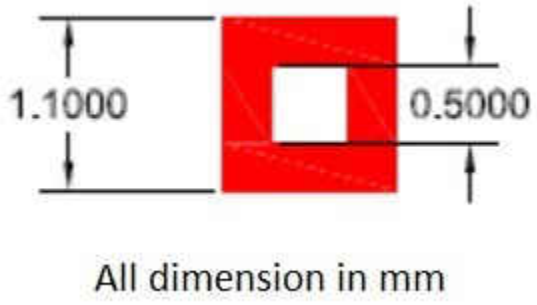

Figure 4.12: Fourth Level Mask Structure

4.1.13 (Al)-Doped ZnO Gate Patterning

Following the fourth level masking, (Al)-doped ZnO layer had to be patterned. The (Al)-doped ZnO patterning was done using (5:1) diluted hydrochloric acid (HCL) wet etchant. The etching was done till the (Al)-doped ZnO was completely removed from the areas not protected by the negative PR. Finally the PR was stripped using acetone after the etching process was completed.

This step completed the ZnO gate based MOSFET fabrication process.

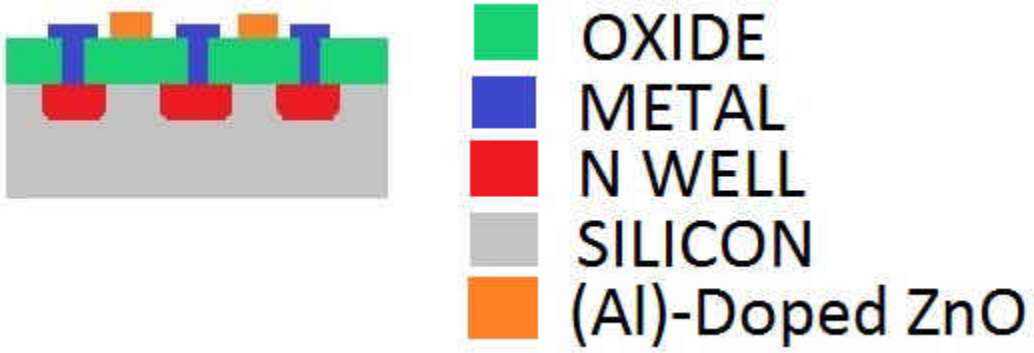

Figure 4.13: Final MOSFET Cross Section

4.1.14 MOSFET Complete Cross Section

The detailed cross section diagram of the MOSFET after every fabrication step is shown in this section.

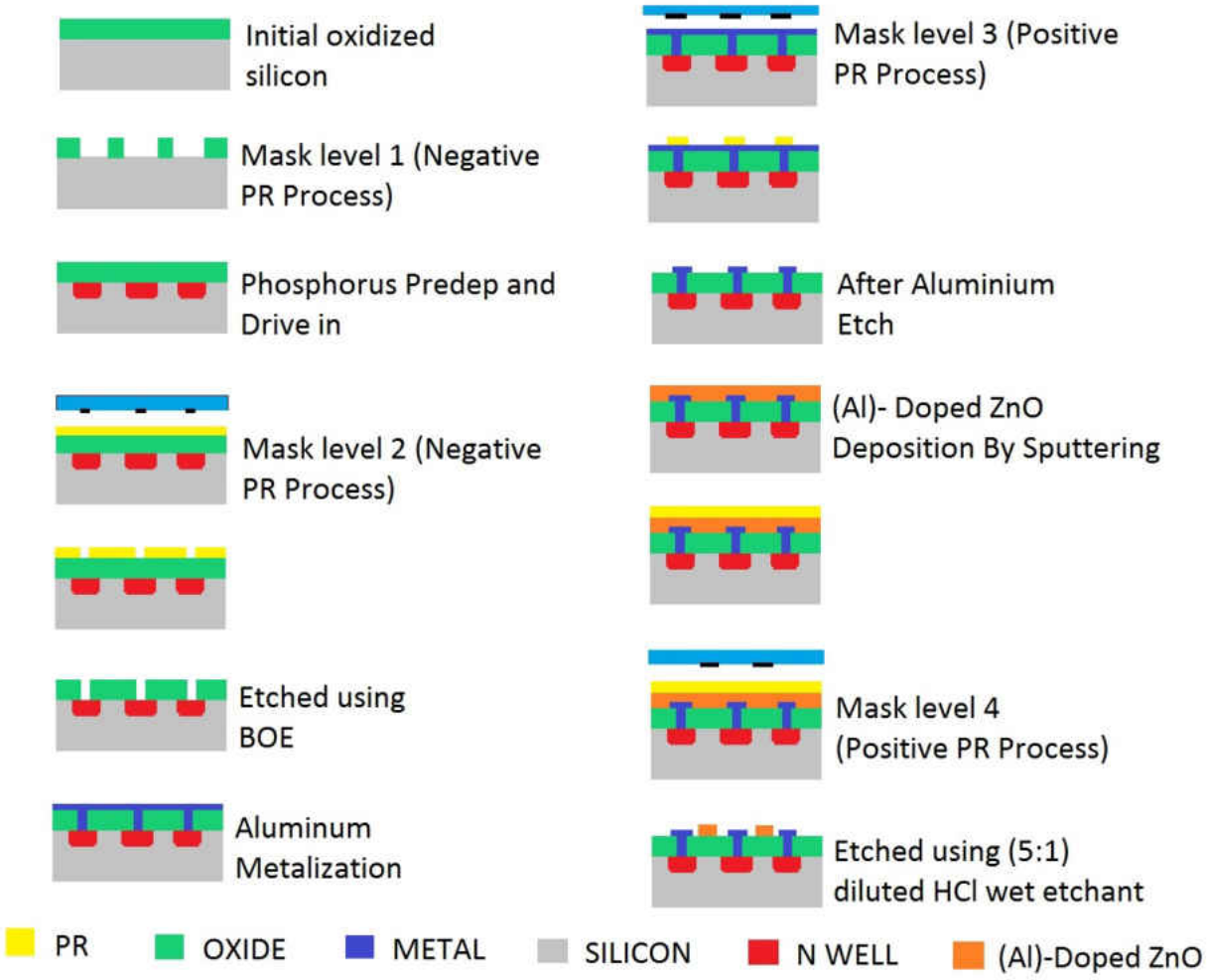

Figure 4.14: (Al)-doped ZnO Gate MOSFET Complete Cross Section

4.2 ITO Gate MOSFET Fabrication

The fabrication of the ITO gate mosfet was done following the same process steps as that followed while fabricating the (Al)-doped ZnO MOSFET till the third level masking and etching to pattern the aluminum source and drain contacts. The fab process for the ITO gate MOSFET continuation is explained further in this section. The cross section of the MOSFET post third level masking is shown in the following diagram.

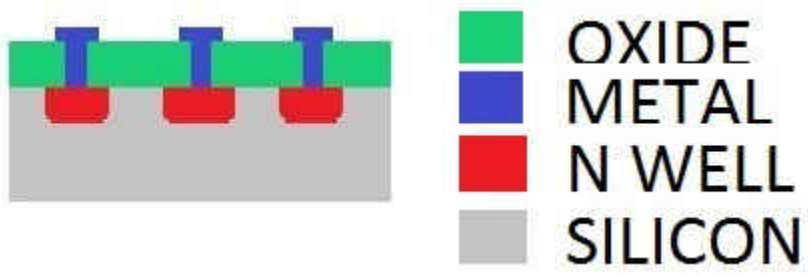

Figure 4.15: Substrate Cross Section Post Third Level Masking

4.2.1 Fourth Level Masking for Liftoff

Indium Tin Oxide (ITO) that was used for the fabrication process consists of 90% In_2O_3 and 10% SnO_2 in weight. ITO is a material that can not be etched very easily, thus liftoff process was used to pattern the gate contact. The fourth level mask structure is shown in the figure below. The fourth level masking was done following negative photolithography process and used NR9-1500 negative photo resist (PR). The substrate was coated with the specified negative PR on top of a spinner and was spun at a speed of 3000 rpm, for 30 seconds.

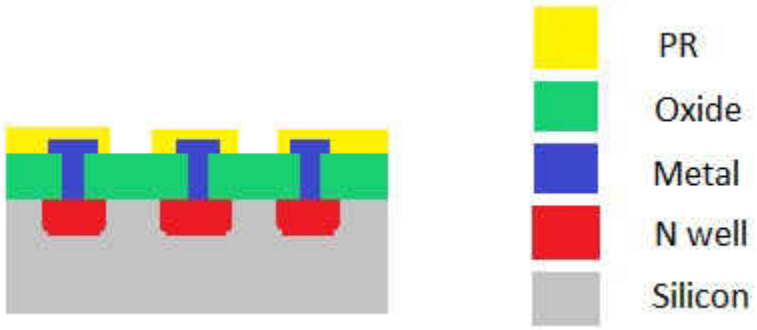

Figure 4.16: Fourth level MOSFET mask structure

Once the negative PR was evenly coated on top of the wafer, the wafer was soft baked inside a oven kept at 150•C for 1 minute. Next step in the lithography procedure was ultra violet (UV) exposure. UV light exposure was done for 10 seconds.

The wafer was post exposure baked in another oven which was kept at 100•C for 1 minute. The PR was now ready to be developed, thus the wafer was developed in a petridish containing RD6 negative PR developer for 30 seconds and was rinsed with DI water at the 30 second mark. The final step in the fourth level photolithography process was the hard baking, where the wafer was baked at 150•C in an oven. Before hard baking the wafer was inspected under the microscope to check if the PR had been properly developed. The sample was finally hard baked at 150•C for only 1 minute as the PR had to be lifted off.

4.2.2 ITO Sputtering

After the source and drain contacts were patterned, the gate oxide had to be deposited. In accordance with the research topic, ITO had to be deposited. The method adopted for depositing the gate contact was Radio Frequency (RF) magnetron sputtering. The target that was used for the

sputtering process had a composition of 90% In_2O_3 and 10% SnO_2 in weight.

The sputtering was done in a sputtering chamber maintained at a pressure of 50 milli-Torr and a RF current of 100 Watts was applied. The Argon flowrate was 20 in the flowmeter. The sputtering was done for approximately 30 minutes resulting in a ITO thickness of about 1500Å.

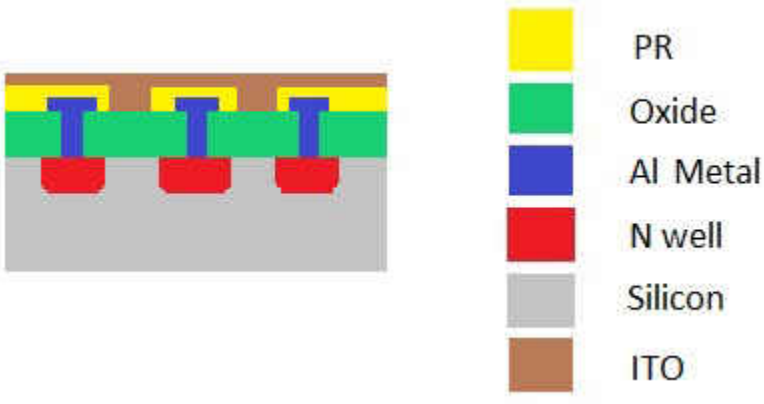

Figure 4.17: Substrate Cross Section After ITO Deposition

4.2.3 ITO Gate Patterning by Liftoff

The next step in the fabrication process was to liftoff the PR. Due to prolonged exposure of the substrate to high temperature during sputtering, over baked the PR, making it stuck to the substrate. The substrate was immersed in concentrated sulfuric acid (H_2SO_4) which completely dissolves the PR and in turn removes the ITO on top of it leaving ITO confined only to the gate area.

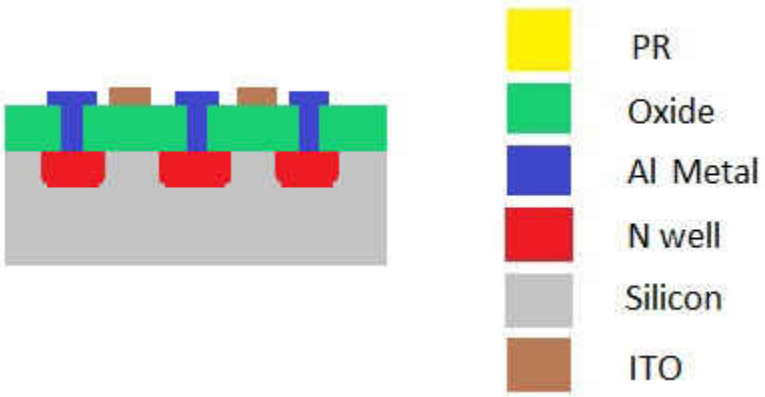

Figure 4.18: Substrate Cross Section After ITO Gate Patterning

The ITO gate MOSFET was completely fabricated. The detailed cross section diagram of the MOSFET after every fabrication step is shown in this section.

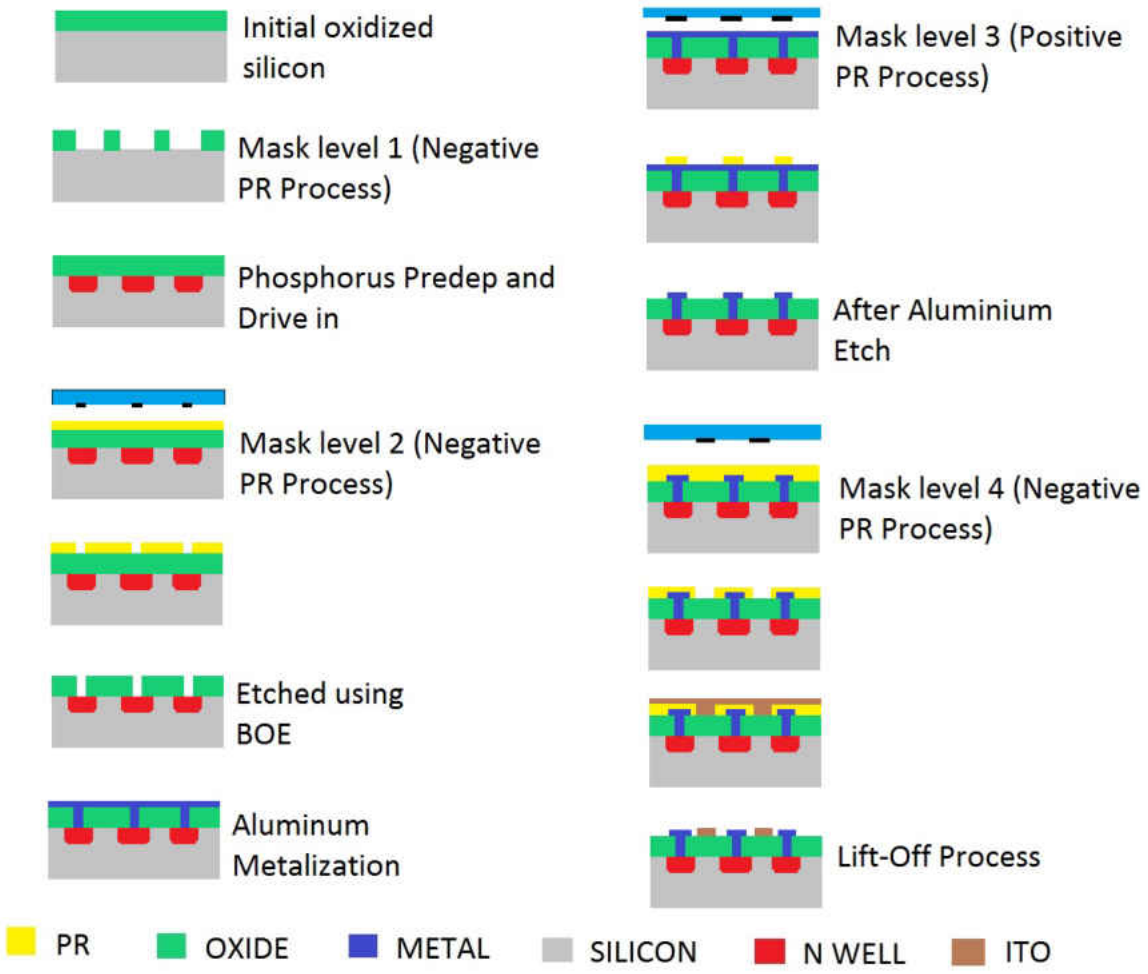

Figure 4.19: (Al)-doped ZnO Gate MOSFET Complete Cross Section

CHAPTER 5: RESULTS

This chapter provides the detailed findings of this research.

5.1 ZnO Film Transmission Curve

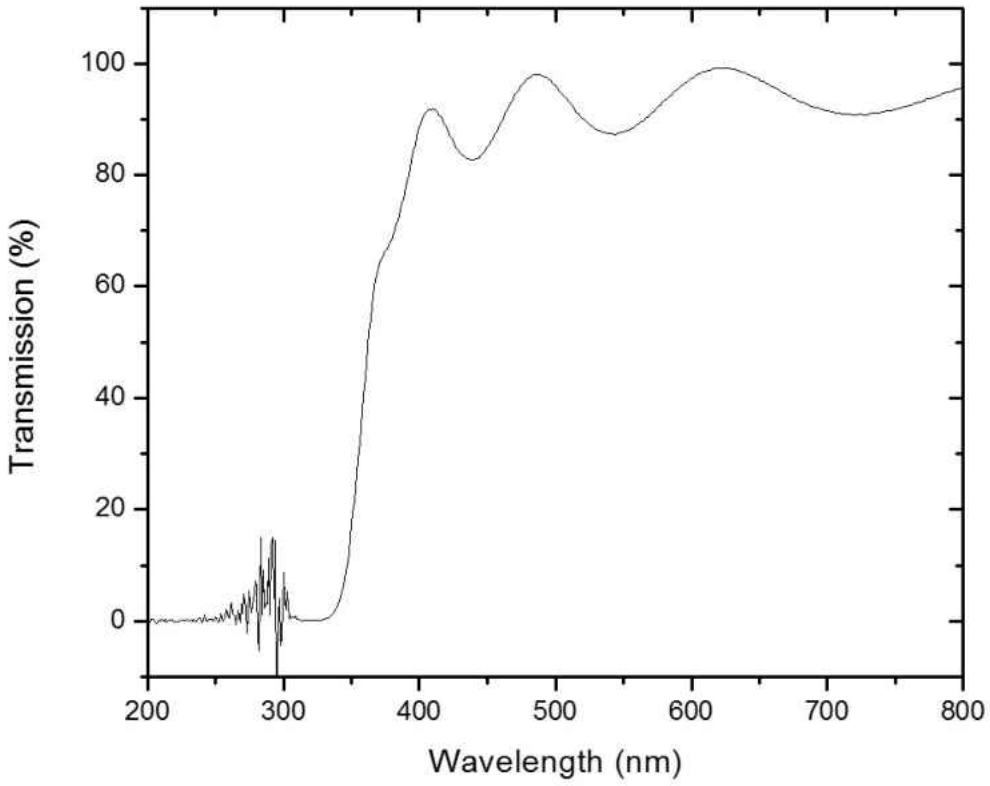

Figure 5.1: ZnO Optical Transmission

The optical transmission value of the deposited ITO thin film was found to be about 90% in the region of 400 to 800 nm using spectrophotometer

5.2 ITO Film Transmission Curve

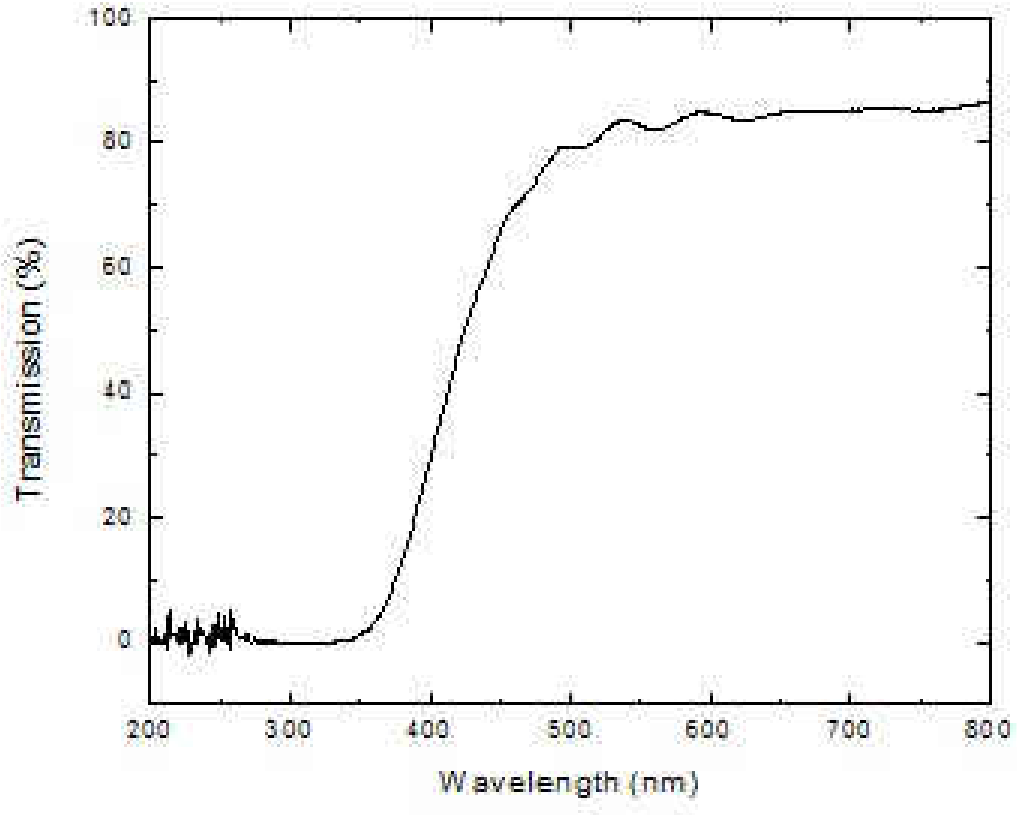

Figure 5.2: ITO Optical Transmission

The optical transmission value of the deposited ITO thin film was found to be about 85% in the region of 450 to 800 nm using spectrophotometer

5.3 ZnO Gate MOSFET Practical Vt Calculation

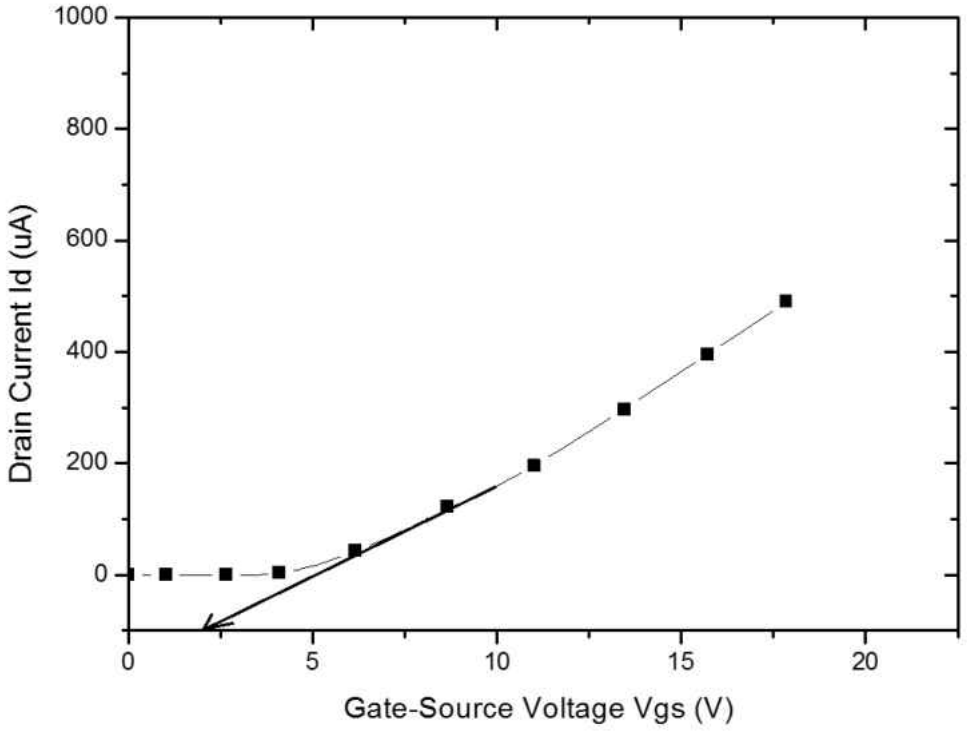

Figure 5.3: ZnO Gate MOSFET Id vs Vgs graph

From the graph shown above comparing drain current Vs gate-source voltage, we can approximately guess the MOSFET threshold voltage to be around 2.5V.

5.4 ITO Gate MOSFET Practical Vt Calculation

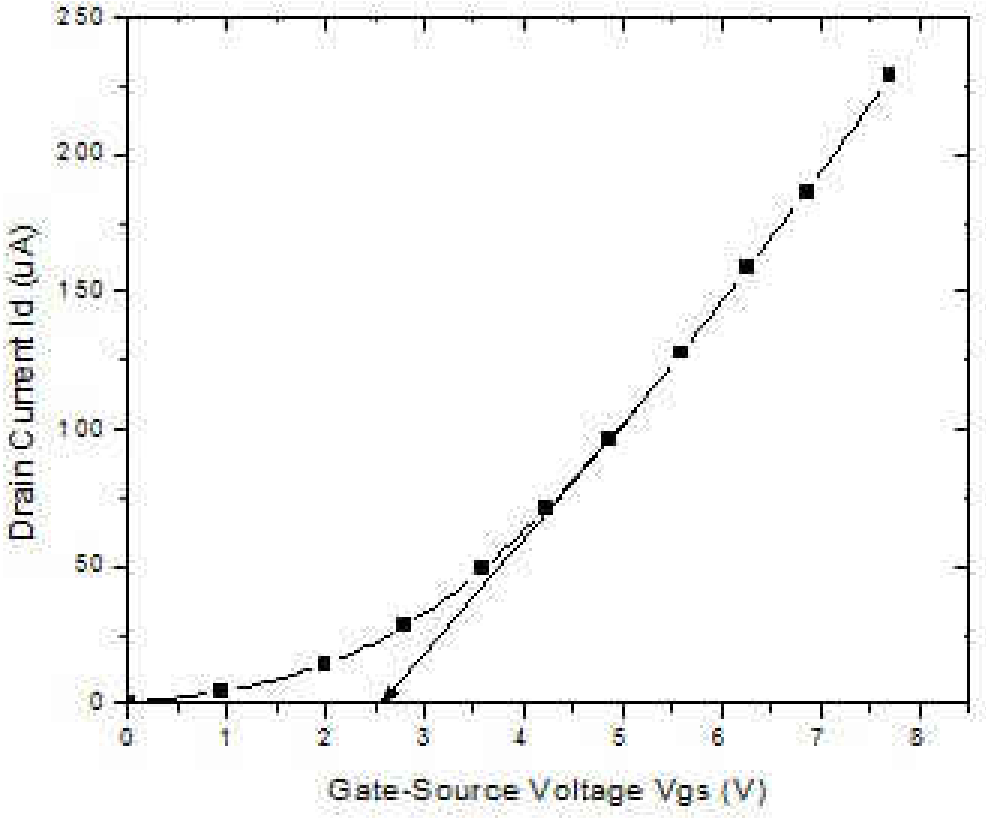

Figure 5.4: ITO Gate MOSFET Id vs Vgs graph

From the graph shown above comparing drain current Vs gate-source voltage, we can approximately guess the MOSFET threshold voltage to be close to 2.5 V.

5.5 ZnO Gate MOSFET I-V Characteristics

The I-V characteristics (Id vs Vds) of the fabricated MOSFET with Al-Doped ZnO as the gate metal is shown in this section. Comparison between the I-V curves taken during dark conditions and the I-V curves with different color light illumination on the gate of the MOSFET is also shown in this section.

All this curves were recorded using Tektronix type 576 curve tracer. A 3 watt led light bulb with different color light illumination was used. The light source had light illumination capability of 250 lumens. The I-V characteristics of the Al-Doped ZnO gate MOSFET with de-ionized water vapor on the gate region is also shown.

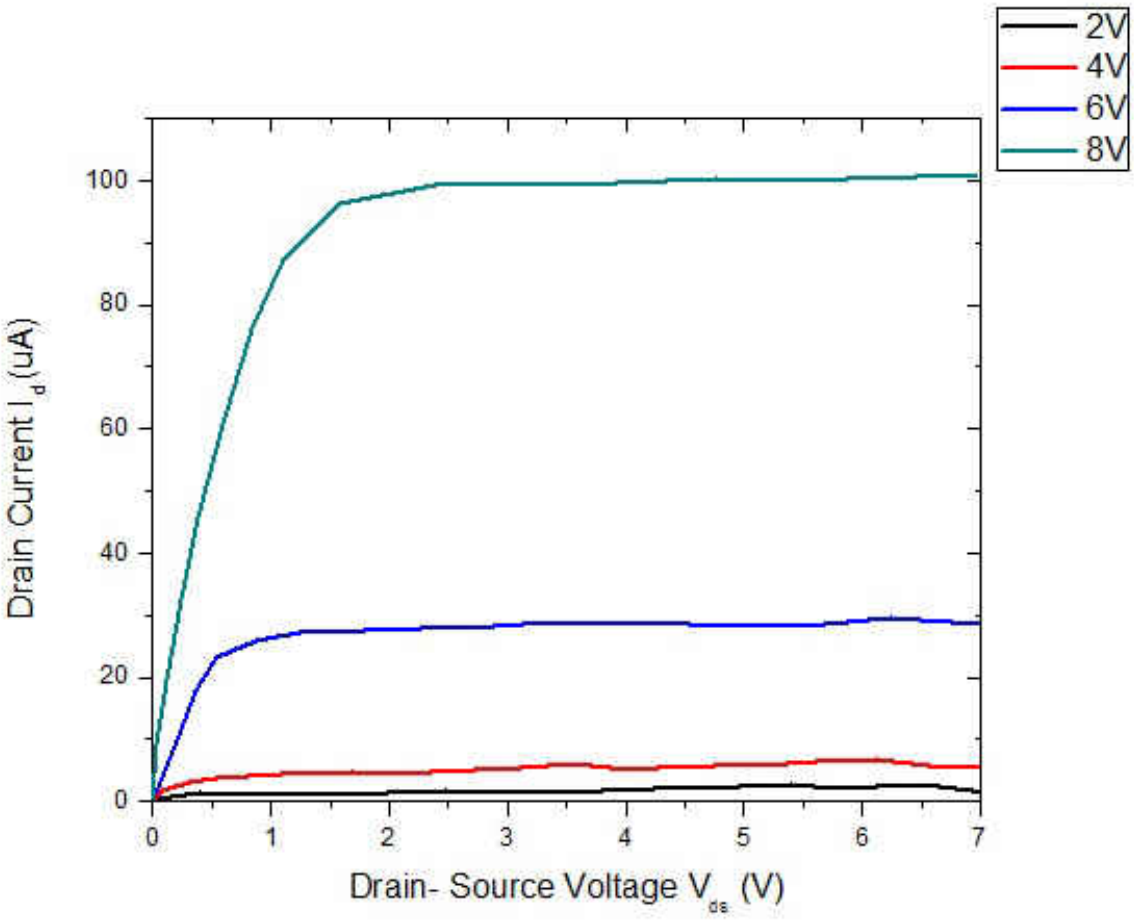

Figure 5.5: ZnO Gate MOSFET I-V Characteristics in Dark Conditions

The lowest drain current value was observed under this condition when compared to other different illuminated conditions. The drain current value observed at 8V gate voltage is clearly seen to be 100 μA.

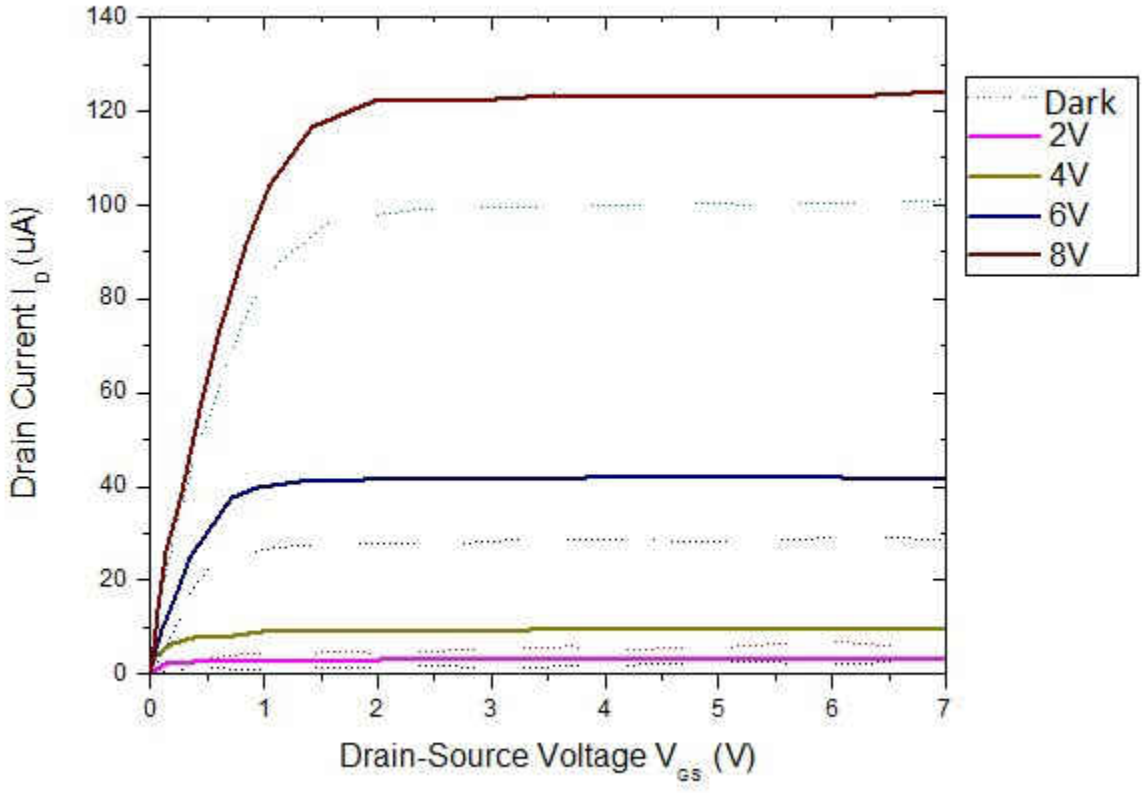

Figure 5.6: ZnO Gate MOSFET I-V Characteristics with White Light illuminations

In the plot shown above is the comparison between the MOSFET I-V characteristics taken during dark conditions and when white light is illuminated. It is noted that the I-V curve under this condition had an increased drain current value when compared to the same I-V characteristics recorded inside a dark room. The drain current was observed to be increased by 22 μA when 8V gate voltage was applied compared to the same graph recorded during the dark conditions.

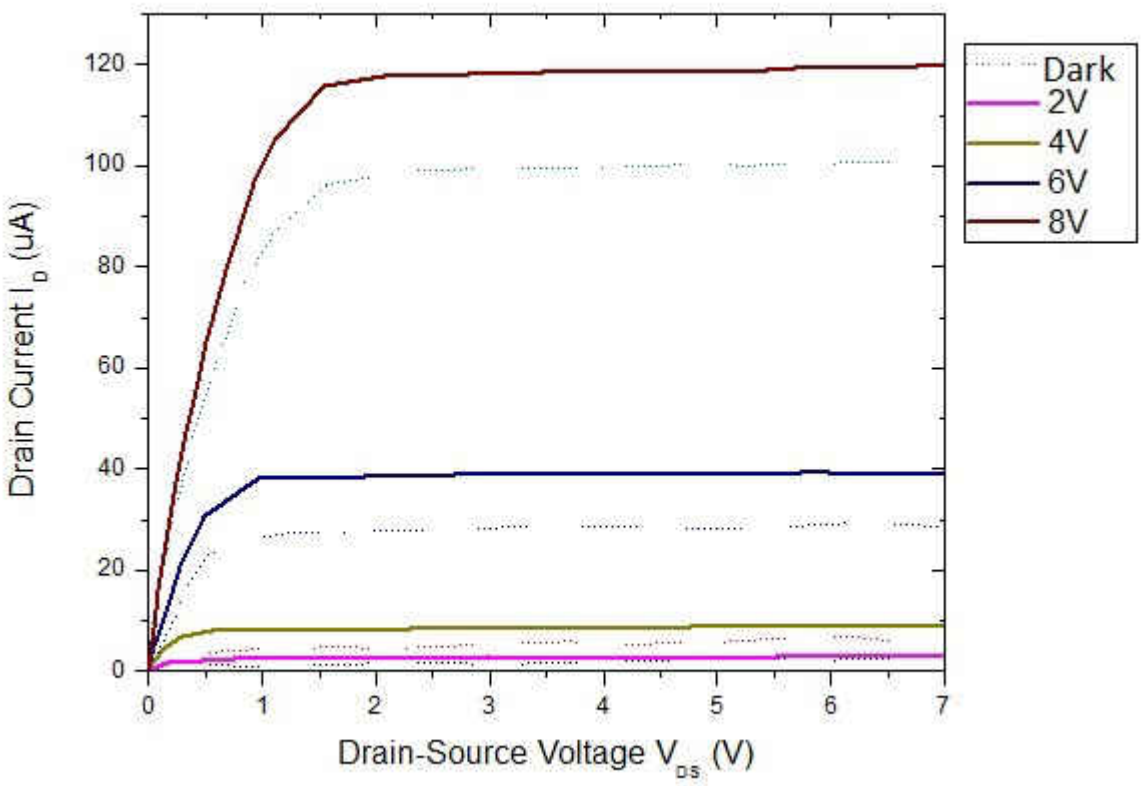

Figure 5.7: ZnO Gate MOSFET I-V Characteristics with Blue Light Illuminations

In the plot shown above is the comparison between the MOSFET I-V characteristics taken during dark conditions and when blue light is illuminated. It is noted that the I-V curve under this condition has an increased drain current value when compared to the same I-V characteristics recorded inside a dark room but is lesser when compared to the values taken during white light illumination. The drain current was observed to be increased by 18 μA when 8V gate voltage was applied compared to the same graph recorded during the dark conditions.

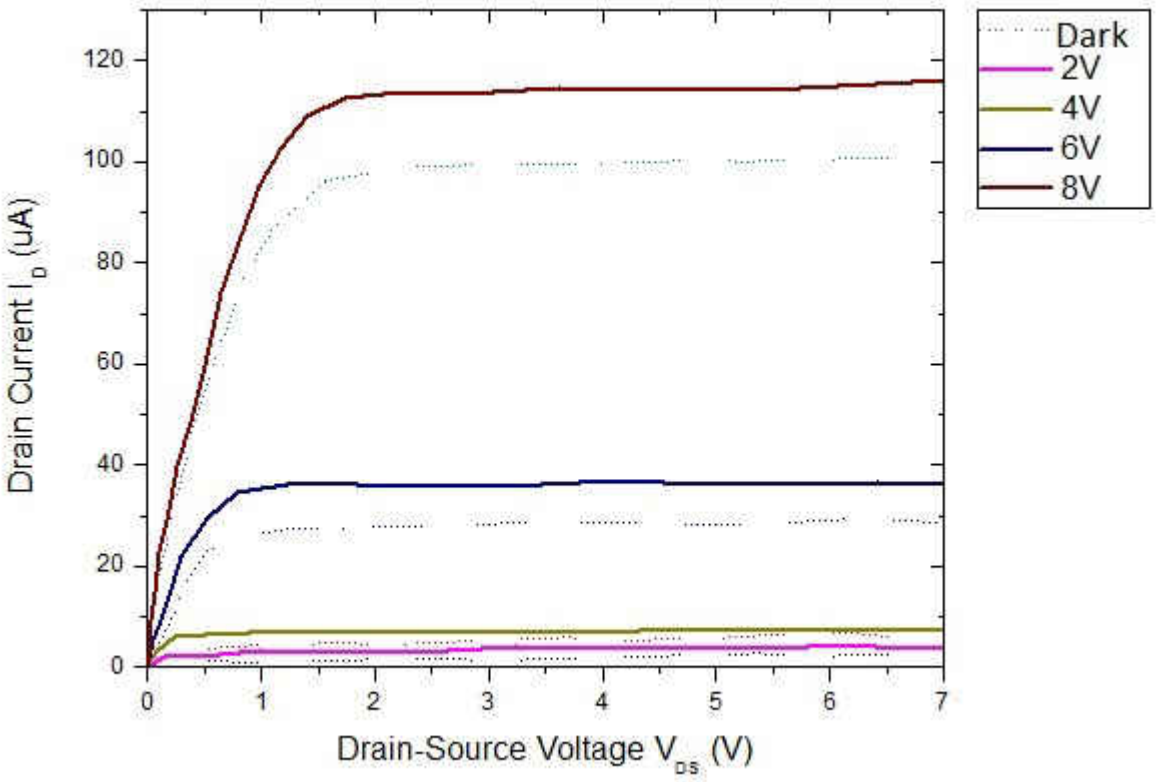

Figure 5.8: ZnO Gate MOSFET I-V Characteristics with Red Light Illuminations

In the plot shown above is the comparison between the MOSFET I-V characteristics taken during dark conditions and when red light is illuminated. It is noted that the I-V curve under this condition has an increased drain current value when compared to the same I-V characteristics recorded inside a dark room but is lesser when compared to the values taken during white light and blue light illumination. The drain current was observed to be increased by 16 μA when 8V gate voltage was applied compared to the same graph recorded during the dark conditions.

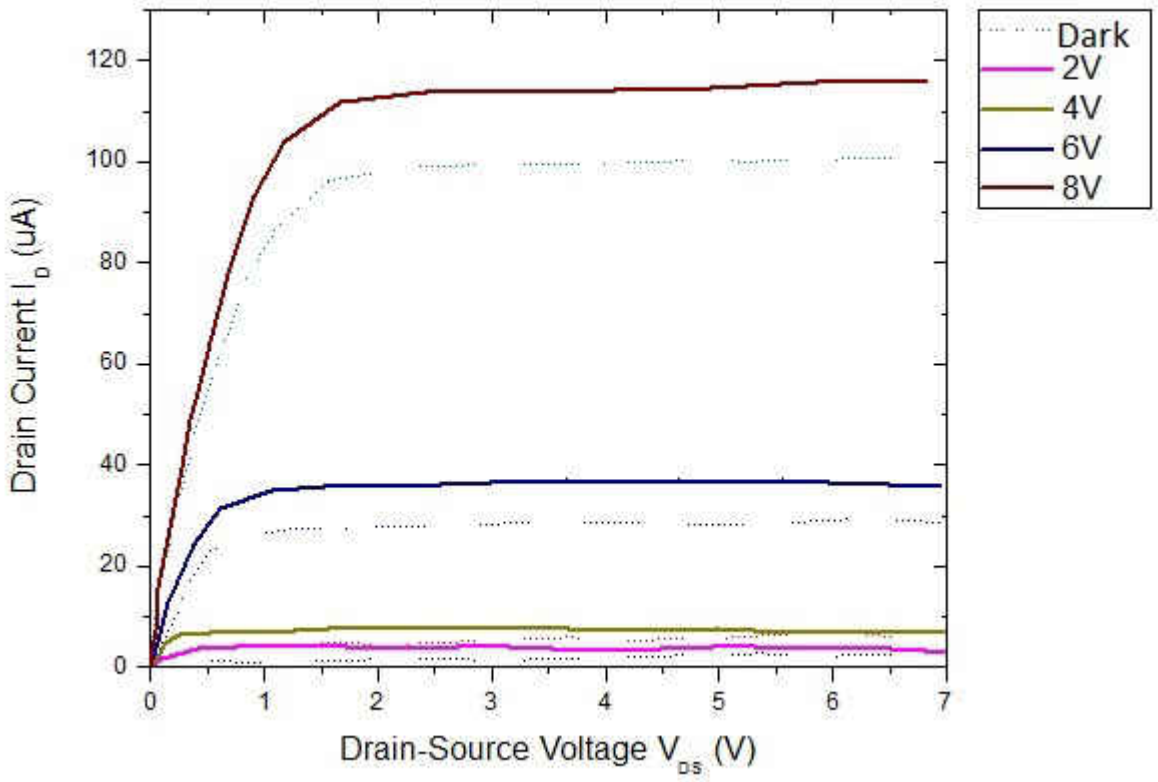

Figure 5.9: ZnO Gate MOSFET I-V Characteristics with Green Light Illuminations

In the plot shown above is the comparison between the MOSFET I-V characteristics taken during dark conditions and when green light is illuminated. It is noted that the I-V curve under this condition has an increased drain current value when compared to the same I-V characteristics recorded inside a dark room but is lesser when compared to the values taken during white light and blue light illumination. The drain current value is same when compared to the red light illuminated condition. The drain current was observed to be increased by 16 μA when 8V gate voltage was applied compared to the same graph recorded during the dark conditions.

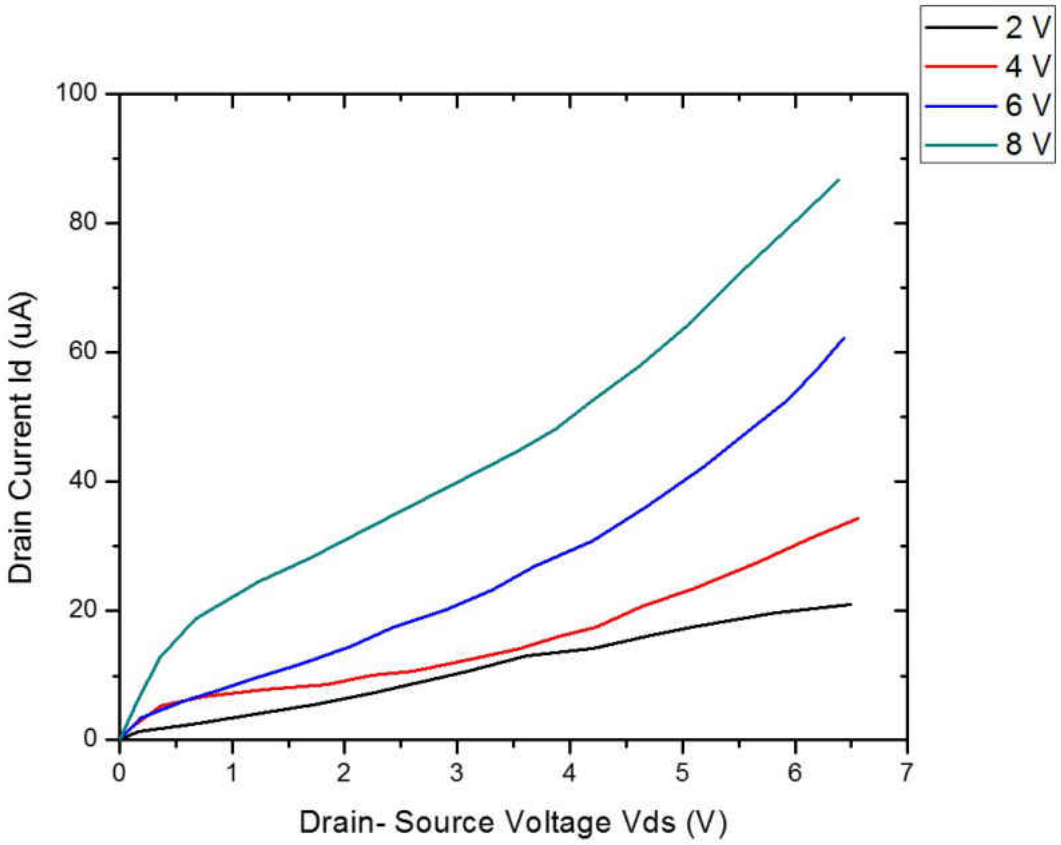

Figure 5.10: ZnO Gate MOSFET I-V Characteristics with De-ionized water vapor on the gate

For this measurement, the same MOSFET used under dark conditions was used. It can clearly be noticed that there is a complete change in the characteristics which evidently displays the humidity detection capability of the fabricated Al-Doped ZnO gate MOSFET device.

5.6 ITO Gate MOSFET I-V Characteristics

The I-V characteristics (Id vs Vds) of the fabricated MOSFET with ITO as the gate metal is shown in this section. Comparison between the I-V curves taken during dark conditions and the I-V curves with different color light illumination on the gate of the MOSFET is also shown in this section.

All these curves were recorded using Tektronix type 576 curve tracer.

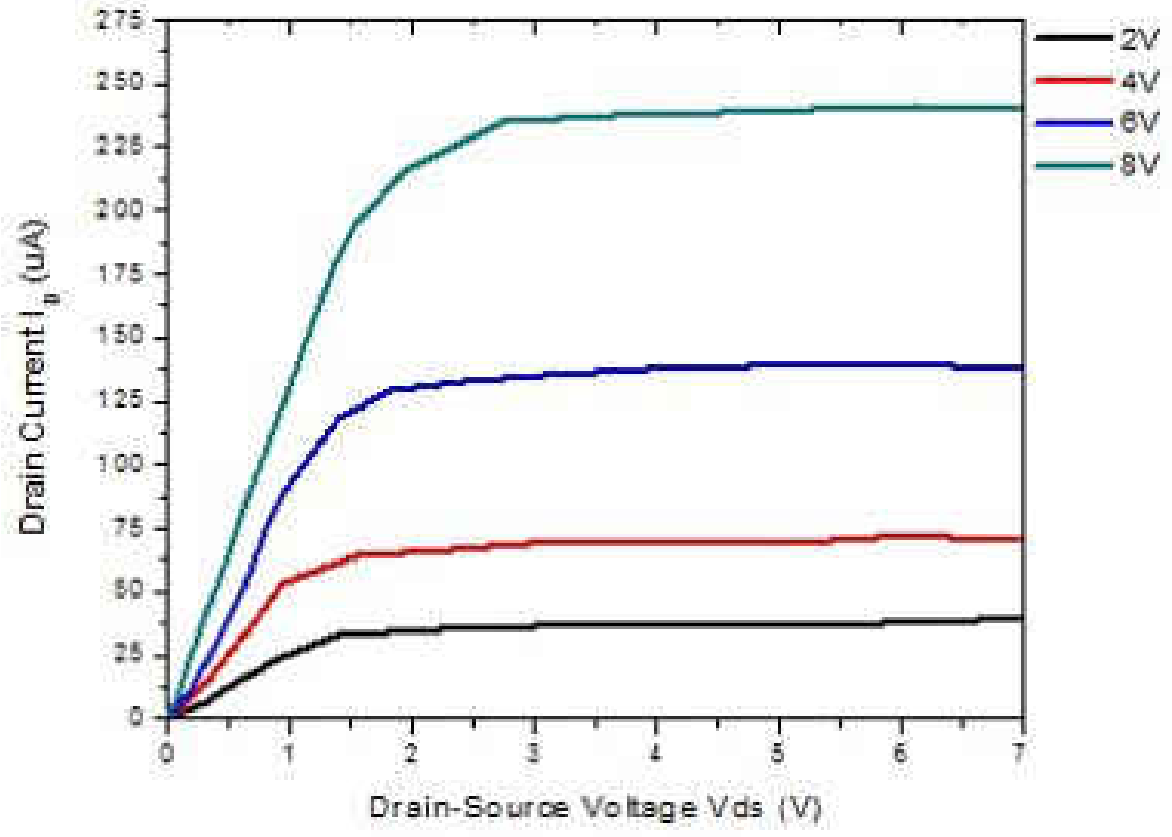

Figure 5.11: ITO Gate MOSFET I-V Characteristics in Dark Conditions

The lowest drain current value was observed under this condition when compared to other different illuminated conditions. The drain current value observed at 8V gate voltage is noted to be 240 μA.

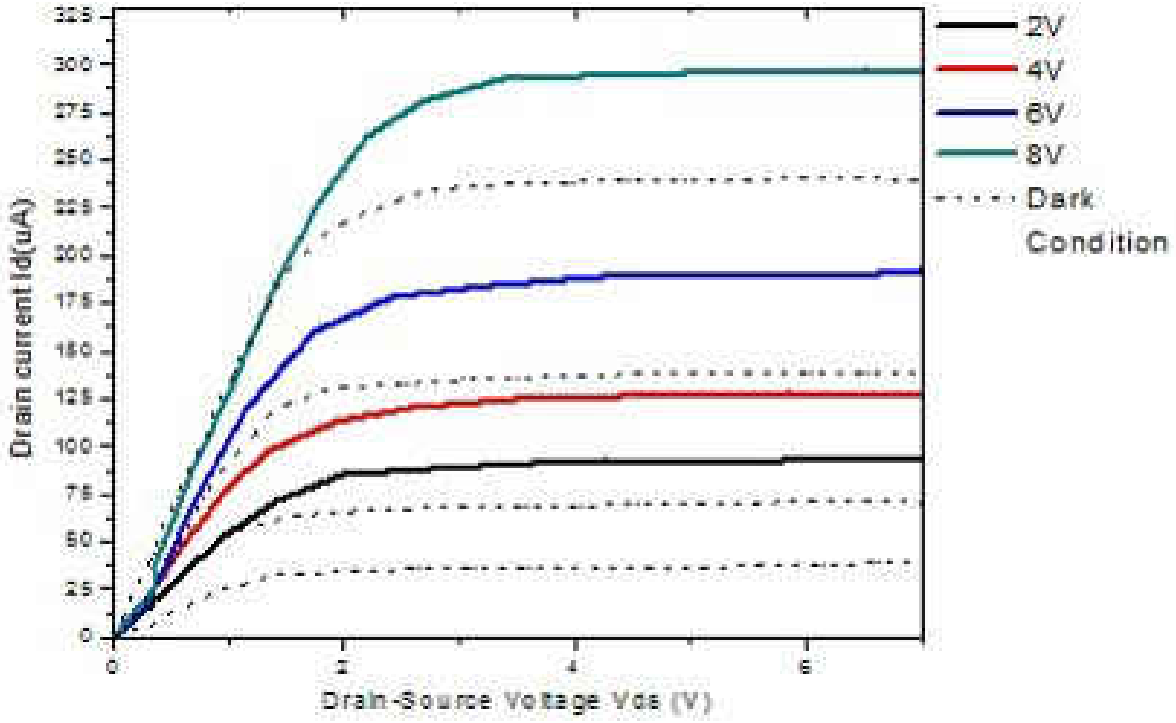

Figure 5.12: ITO Gate MOSFET I-V Characteristics with White Light illuminations

In the plot shown above is the comparison between the MOSFET I-V characteristics taken during dark conditions and when white light is illuminated. It is noted that the I-V curve under this condition had an increased drain current value when compared to the same I-V characteristics recorded inside a dark room. The drain current was observed to be increased by 60 μA when 8V gate voltage was applied compared to the same graph recorded during the dark conditions.

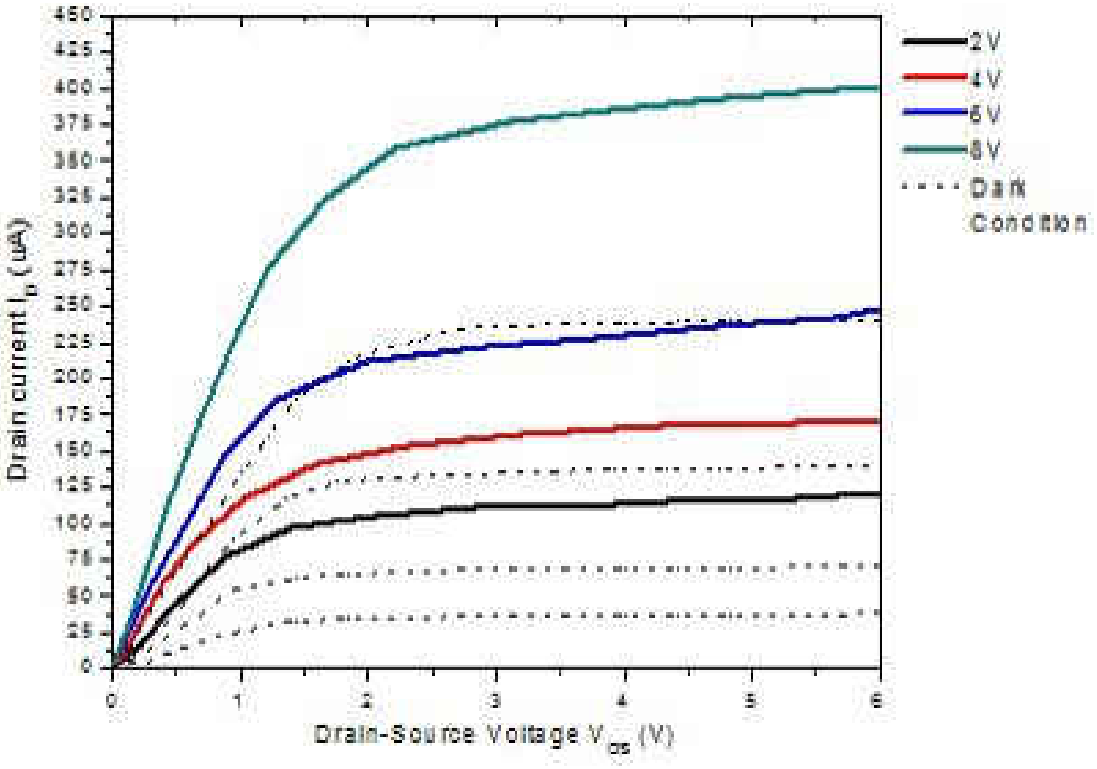

Figure 5.13: ITO Gate MOSFET I-V Characteristics with Yellow Light Illumination

In the plot shown above is the comparison between the MOSFET I-V characteristics taken during dark conditions and when yellow light is illuminated. It is noted that the I-V curve under this condition has an increased drain current value when compared to the same I-V characteristics recorded inside a dark room and when illuminated with white light. The drain current was observed to be increased by 160 μA when 8V gate voltage was applied compared to the same graph recorded during the dark conditions.

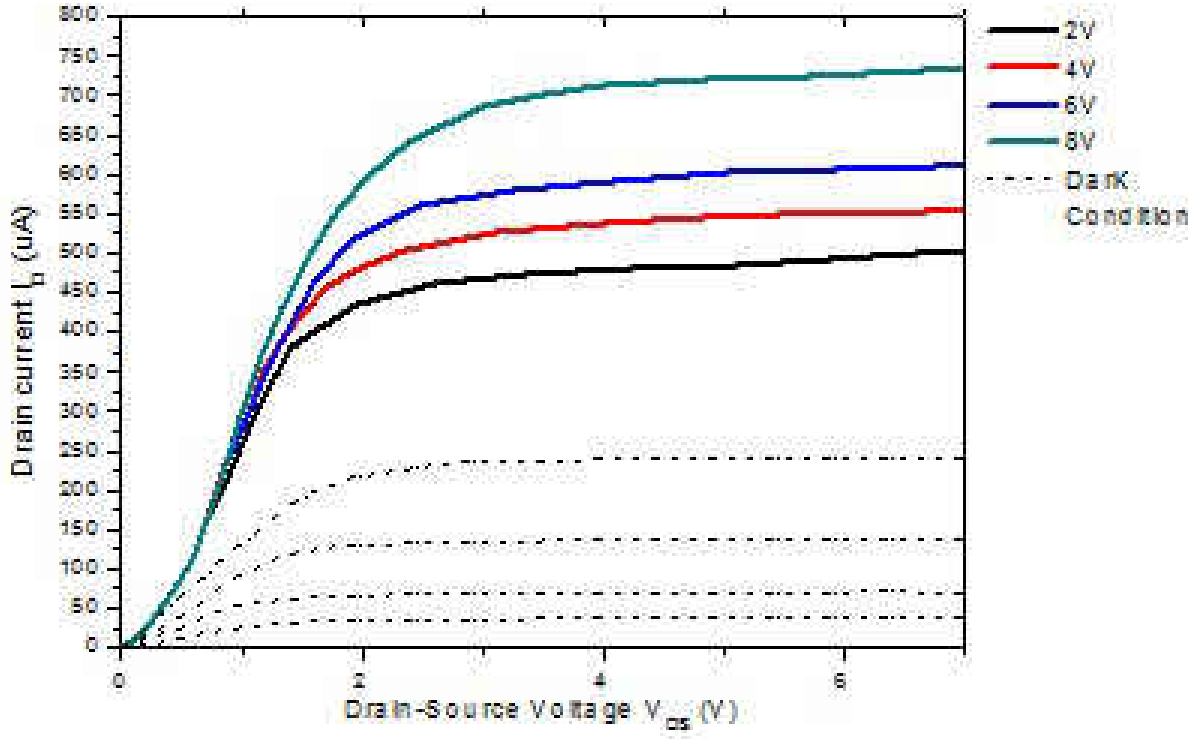

Figure 5.14: ITO Gate MOSFET I-V Characteristics with Red Laser Illuminations

In the plot shown above is the comparison between the MOSFET I-V characteristics taken during dark conditions and when red laser is illuminated. A He-Ne laser is used for the illumination. It is noted that the I-V curve under this condition had a very large increased drain current value when compared to the same I-V characteristics recorded inside a dark room and also with white light and yellow light illumination. The drain current was observed to be increased by 485 μA when 8V gate voltage was applied compared to the same graph recorded during the dark conditions.

5.7 ZnO Gate MOSFET theoretical Vt Calculation

Type of Silicon :p

Resistivity, ρ :9 Ω-cm

N_A value for 9 Ω-cm :4.5×10^{15} atoms/cm^3 [From Jaegar Book]

Work Function Difference

$$\Phi_{ms} = 0.21V$$

Built in Voltage

$$\Phi_f = \frac{kT}{q} ln \frac{N_A}{n_i}$$

$$= 0.026 ln \frac{3 \times 10^{15}}{1.5 \times 10^{10}}$$

$$= 0.324V$$

Depletion Width

$$W = 2 \times \sqrt{\frac{\varepsilon_{si}\Phi_f}{qN_A}}$$

$$W = 0.434\mu m$$

Charge in the Depletion Region

$$Q_D = -qN_AW$$

$$Q_D = -3.122 \times 10^{-8}\frac{C}{cm^2}$$

Dielectric Capacitance

$$C_i = \frac{\varepsilon_i}{d}$$

$$C_i = 6.903 \times 10^{-9}\frac{F}{cm^2}$$

ZnO Gate MOSFET Threshold Voltage

$$V_t = \Phi_{ms} + 2\Phi_f - \frac{1}{C_i}(Q_i + Q_D)$$

$$V_t = 2.644V$$

5.8 ITO Gate MOSFET theoretical Vt Calculation

Type of Silicon :p

Resistivity, ρ :7 Ω-cm

N_A value for 7 Ω-cm :6 X 10^{15} atoms/cm^3 [From Jaegar Book]

Work Function Difference

$$\Phi_{ms} = 0.29V$$

Built in Voltage

$$\Phi_f = \frac{kT}{q} ln \frac{N_A}{n_i}$$

$$= 0.026 ln \frac{2 \times 10^{15}}{1.5 \times 10^{10}}$$

$$= 0.332V$$

Depletion Width

$$W = 2 \times \sqrt{\frac{\varepsilon_{si}\Phi_f}{qN_A}}$$

$$= 2\sqrt{\frac{11.8 \times 8.85 \times 10^{-14} \times 0.303}{1.6 \times 10^{-19} \times 2 \times 10^{15}}}$$

$$W = 0.38\mu m$$

Charge in the Depletion Region

$$Q_D = -qN_A W$$

$$Q_D = -3.646 \times 10^{-8} \frac{C}{cm^2}$$

Dielectric Capacitance

$$C_i = \frac{\varepsilon_i}{d}$$

$$C_i = 7.67 \times 10^{-9} \frac{F}{cm^2}$$

ITO Gate MOSFET Threshold Voltage

$$V_t = \Phi_{ms} + 2\Phi_f - \frac{1}{C_i}(Q_i + Q_D)$$

$$V_t = 3.041V$$

CHAPTER 6: CONCLUSION

The main focus of this work was to utilize the highly useful TCOs for sensor applications. For this purpose, two different materials were chosen to be used for sensor applications namely, ITO and ZnO. In order to use these oxide semiconductors for sensor applications, MOSFETs were fabricated with these materials as gate contact.

For the fabrication of the MOSFET a four level mask was used. The first level for the initial impurity doping. The second level for making the via holes. The third level for etching the source and drain contacts. The fourth level photolithography process varied for both the oxides. For making ZnO gate MOSFET, the fourth level was used for patterning the deposited ZnO film to form the gate contact. In the ITO gate MOSFET fabrication process, the fourth level masking was done to perform lift-off of ITO to form the gate contact.

Once the fabrication process was completed, the I-V characteristics of the MOSFET was found using a curve tracer. The MOSFET was illuminated with different color lights and their I-V characteristics were noted. It was observed that there was an increase in the drain current I_D. The I-V characteristics of the ZnO gate MOSFET was noted after the application of of de-ionized water vapors on the gate area of the MOSFET. There were visible changes in the I-V curves of the MOSFET.

APPENDIX A: FABRICATION MACHINES AND INSTRUMENTS

Figure A.1: Oxidation and Diffusion Furnaces

Figure A.2: Diffusion Furnace Elephant

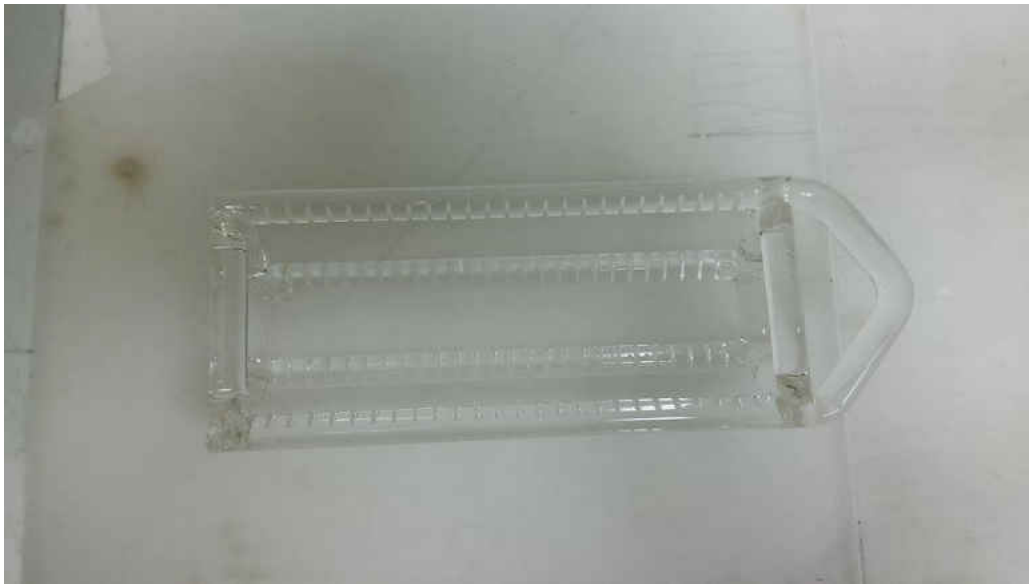

Figure A.3: Furnace Quartz Boat

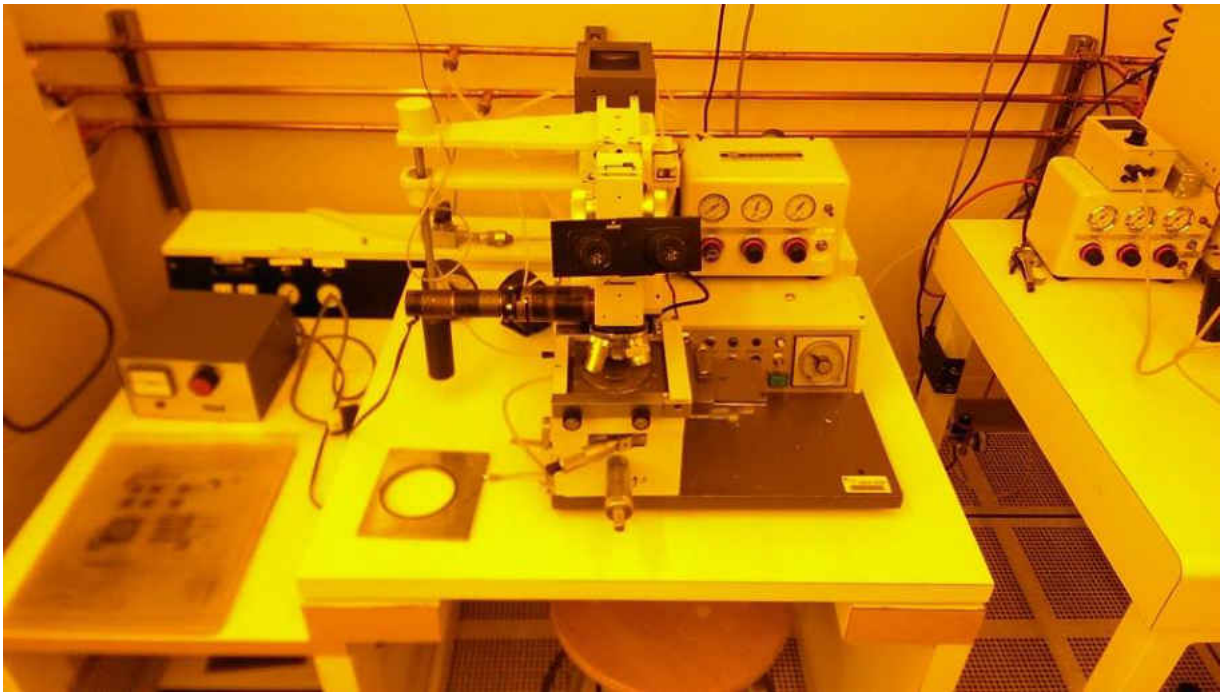

Figure A.4: Karl Suss Mask Aligner

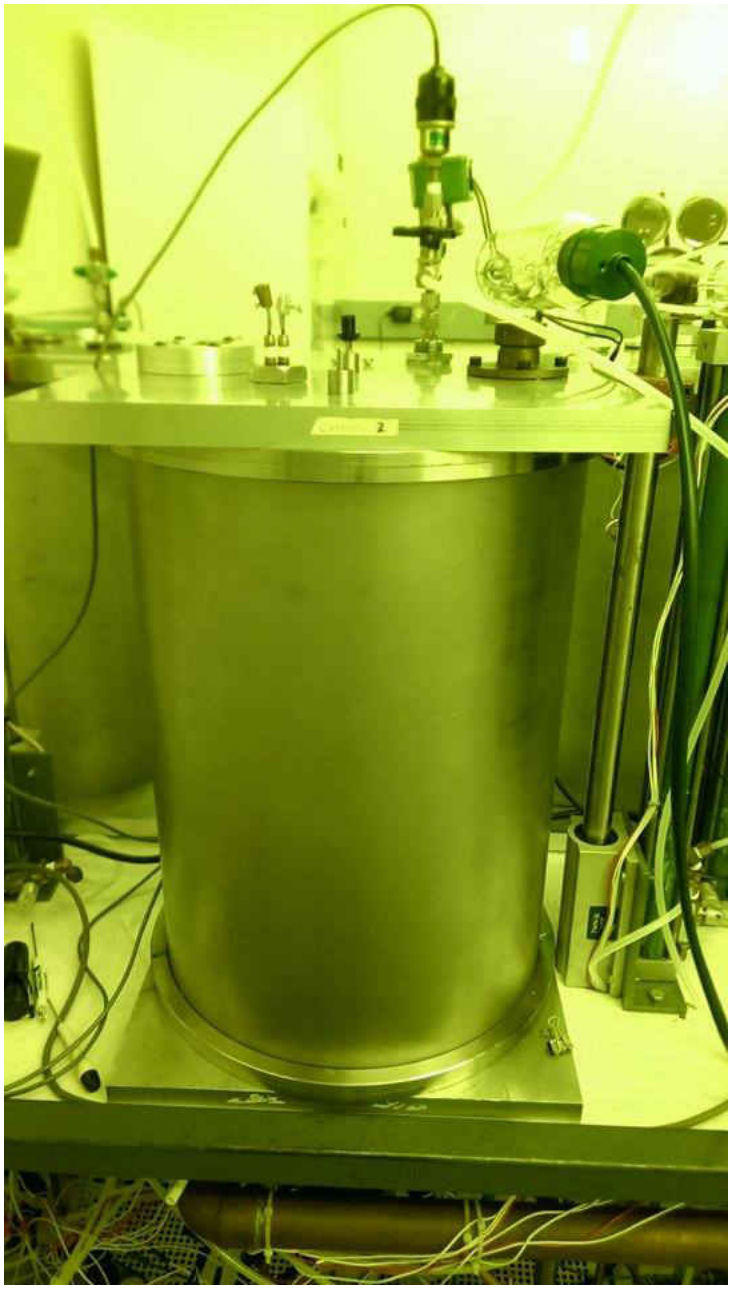

Figure A.5: RF Magnetron Sputtering Chamber

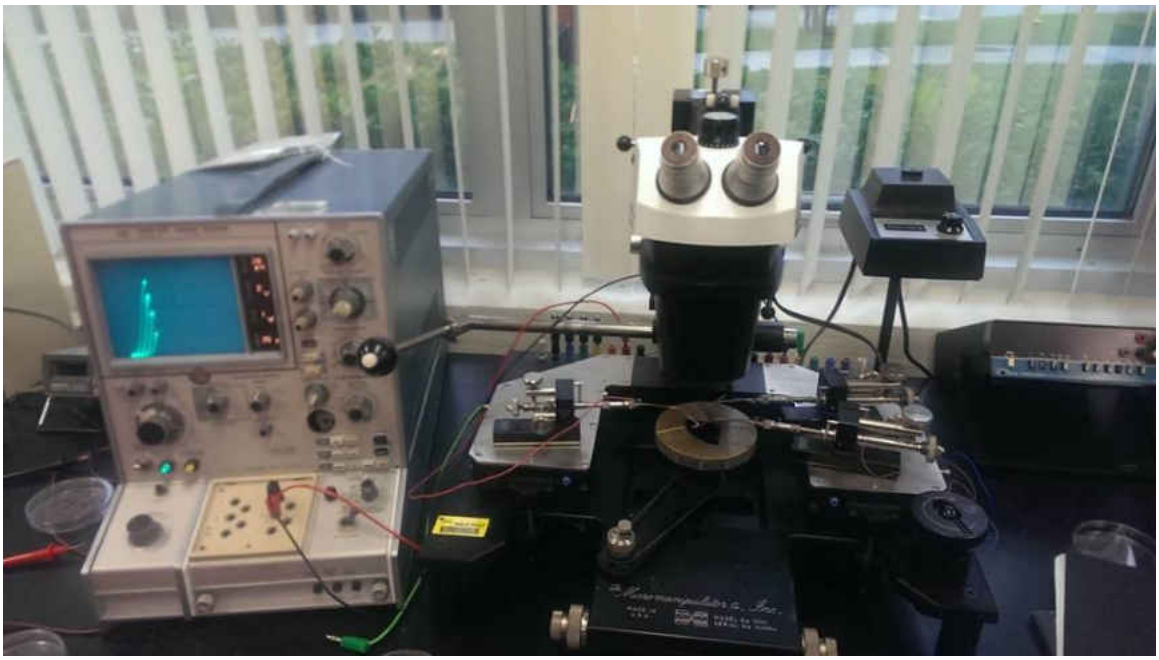

Figure A.6: Tektronix 576 Curve Tracer and Probing Station

APPENDIX B: MASK STRUCTURE

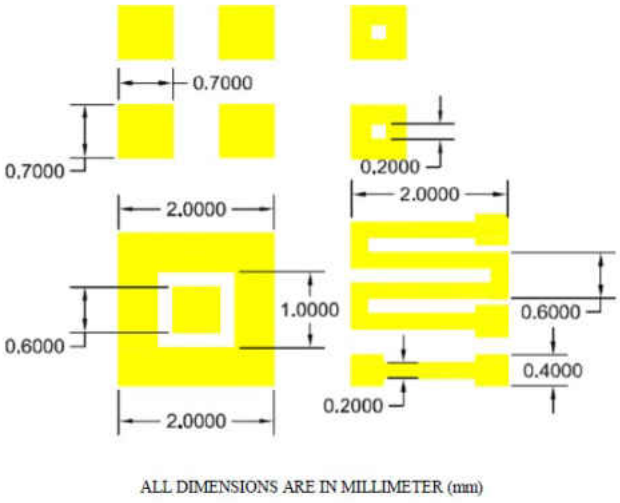

Figure B.1: Mask Level 1

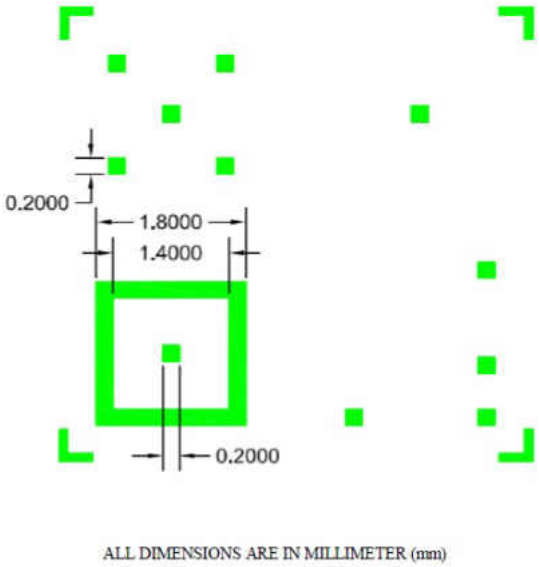

Figure B.2: Mask Level 2

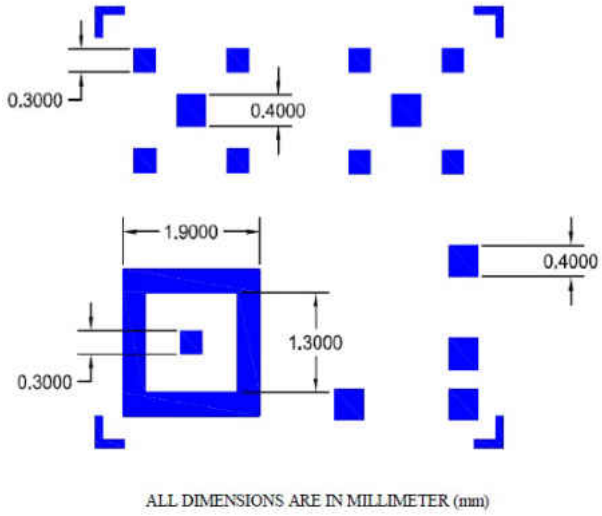

Figure B.3: Mask Level 3

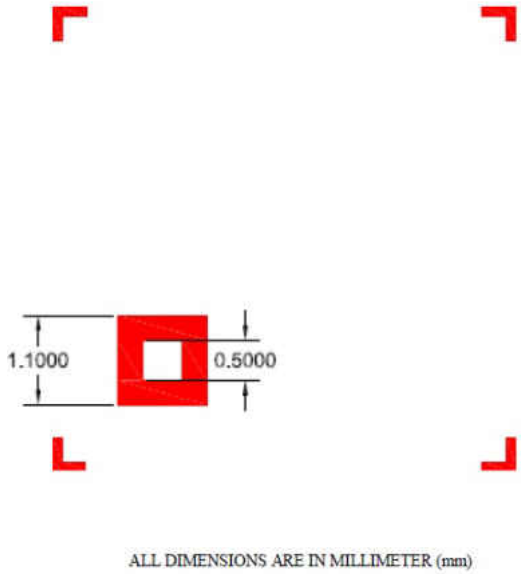

Figure B.4: Mask Level 4

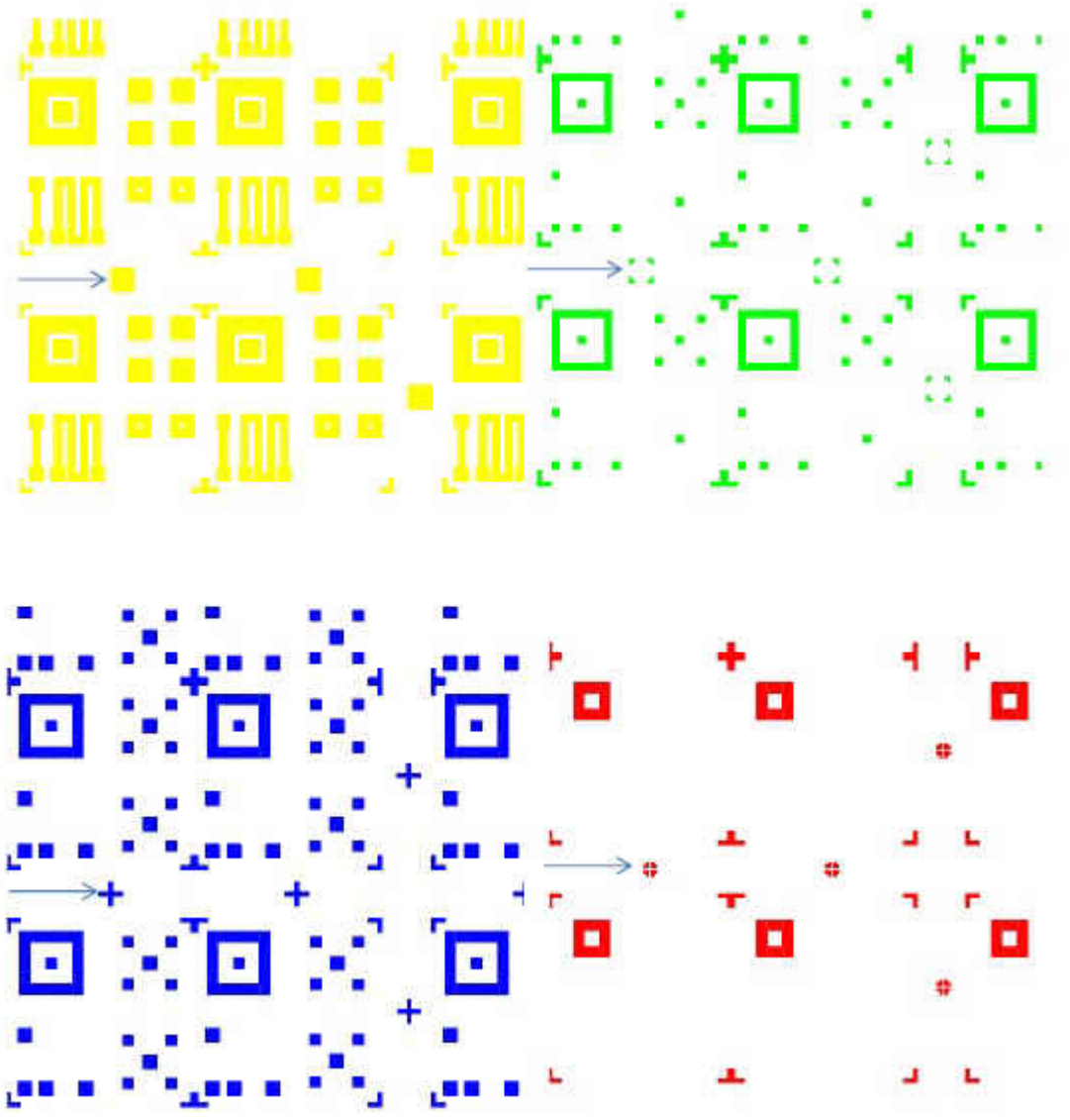

Figure B.5: Four Levels of the Mask

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