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Post Conversion Correction of Non-Linear Mismatches for Time Interleaved Analog-to-Digital Converters

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POST CONVERSION CORRECTION OF NON-LINEAR MISMATCHES FOR TIME INTERLEAVED ANALOG-TO-DIGITAL CONVERTERS

by

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ABSTRACT

Time Interleaved Analog-to-Digital Converters (TI-ADCs) utilize an architecture which enables conversion rates well beyond the capabilities of a single converter while preserving most or all of the other performance characteristics of the converters on which said architecture is based. Most of the approaches discussed here are independent of architecture; some solutions take advantage of specific architectures. Chapter 1 provides the problem formulation and reviews the errors found in ADCs as well as a brief literature review of available TI-ADC error correction solutions. Chapter 2 presents the methods and materials used in implementation as well as extend the state of the art for post conversion correction. Chapter 3 presents the simulation results of this work and Chapter 4 concludes the work. The contribution of this research is three fold: A new behavioral model was developed in Simulink™ and MATLAB™ to model and test linear and nonlinear mismatch errors emulating the performance data of actual converters. The details of this model are presented as well as the results of cumulant statistical calculations of the mismatch errors which is followed by the detailed explanation and performance evaluation of the extension developed in this research effort. Leading post conversion correction methods are presented and an extension with derivations is presented. It is shown that the data converter subsystem architecture developed is capable of realizing better performance of those currently reported in the literature while having a more efficient implementation.

This dissertation is dedicated to my friends and family, you made sure I had the moral and emotional support I needed. When I shut myself away for days at a time researching, simulating or writing you took turns pulling me back out into the world to have fun. When I let myself get caught up in doing too many things at once you nudged me back into focus. And in particular, to my brother Michael Parkey, you moved me and my stuff around Florida so many times in the last 7 years and only requested one thing, never move to the third floor again. I think I can handle that.

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To Dr. David Chester and Dr. Wasfy B Michael your encouragement, support, wisdom and expertise guiding me through this process as my Co-Advisors was invaluable. Without your help I would have several concussions from beating my head against the proverbial wall.

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LIST OF MEDIA/ABBREVIATIONS/NOMENCLATURE/ACRONYMS

Acronym	Description
ADC	Analog-to-Digital Converter
bkgd	background
BLMS	block least mean squared
BW	bandwidth
cal	calibration
CIC	cascade integrator-comb
CMOS	complementary metal-oxide-semiconductor
COTS	commercial off the shelf
DAC	Digital to Analog Converter
dB	decibels
DNL	differential non-linearity
ENOB	effective number of bits
FIR	finite impulse response
Freq	frequency
FS	full scale
Fs	sampling rate
Gsps	giga samples per second
HOCS	higher order cyclostationary statistics
HOS	higher order statistics
Hz	Hertz
I/O	Inputs/Outputs
IEEE	Institute of Electrical and Electronics Engineers
IF	intermediate frequency

INL	integral non-linearity
LMS	least mean squared
LSB	least significant bit
MHz	mega hertz
mW	milli Watt
NLMS	normalized least mean squared
NRE	non-recurring engineering
OBALMS	optimum bock adaptive least mean squared
PM	phase modulation
ps	pico second
RMS	root mean square
S/H	sample and hold
SAR	successive approximation
SFDR	spurious free dynamic range
SNDR	signal to noise and distortion ratio
sps	samples per second
SWaP	size, weight, and power
T/H	track and hold
TI-ADC	Time Interleaved Analog to Digital Converter
Typ	typical
UWB	ultra wide band
V	Volt
VDF	variable digital filter

CHAPTER 1: GENERAL INTRODUCTION

Time interleaved analog-to-digital converters (TI-ADCs) are made up of multiple ADCs, also known as sub-ADCs, which sample the input signal in a round robin fashion to increase the sample rate of the system [1]. An ideal TI-ADC increases the overall sample rate by M times while preserving the critical performance characteristics, where M is the number of converters interleaved. In practice periodic time varying mismatches are introduced through device differences that exacerbate the single device's linear, nonlinear and timing errors and distortion. In addition to the errors introduced strictly due to interleaving the sub-ADCs, the analog front end including the sample and hold(s) that may be required to support the sampling operation add additional nonlinear errors. The first step in matching the ADCs is during device selection, by picking closely matched devices from a large inventory. However since the devices cannot be fully matched to near required accuracies largely due to semiconductor process variations the use of post conversion correction is needed.

The first paper written on TI-ADCs was by Black and Hodges [1], published in 1980. Though the technology is not a new concept, the evolution of semiconductor technology to enable the concepts to be practically implemented has resulted in a recent expansion of interest in TI-ADCs that has produced over 30 US Patents awarded in the last 5 years. Current and emerging applications benefiting from TI-ADCs include instrumentation, ultra wide band (UWB) communications [2], high-bandwidth I/Os requiring sampling rates of 10 to 25GHz, 70GHz radar systems [2], etc. Direct conversion techniques for Radar and communications [3-7], measurement systems [8,9], and photonic sampling systems [10] have been addressed in the past

year with TI-ADCs using a variety of device architectures such as pipeline, Flash, successive approximation (SAR), optical and photonic ADCs.

In 2014 there were 37 of 62 articles reporting TI-ADC hardware level simulations and fabrication developments in the Institute of Electrical and Electronics Engineers (IEEE) proceedings and journals, Figure 1 shows the increasing trend of reported developments for all academic pursuits of TI-ADCs including theory, mismatch correction research, tutorials, supportive circuitry, applications, and hardware.

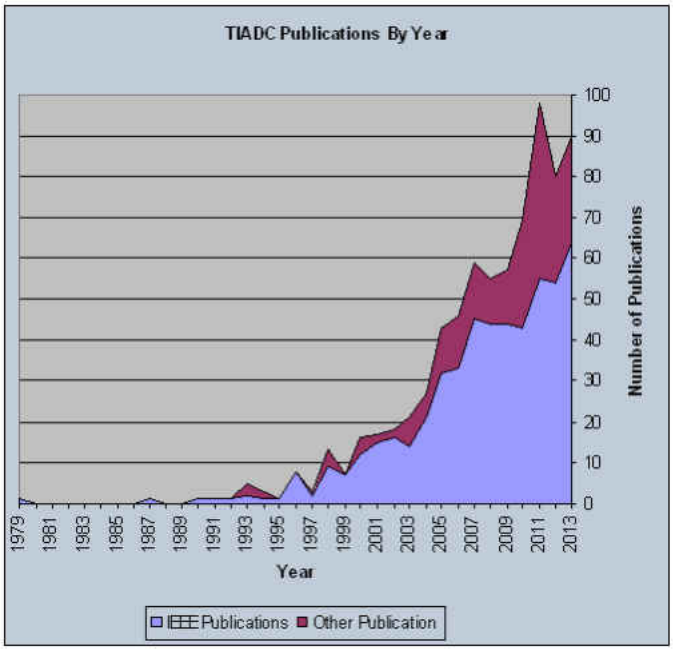

Figure 1: Academic publication trends in TI-ADCs

Taking advantage of TI-ADCs requires a basic understanding of the hardware, errors, layout, application, and correction algorithms used to maximize the performance of the system. A basic knowledge of the uniform sampling analog-to-digital conversion process is assumed; this

understanding is extended with the basic concepts of TI-ADC technology and its recent developments.

The following subsections discuss the general structure of a TI-ADC and the use cases that the application of TI-ADCs were intended to address. The errors sources present in the analog front end, individual and time interleaved converters are then discussed before introducing current mismatch correction methods.

Problem Formulation

The bottleneck in most cutting edge signal processing based technologies is the barrier between the analog and discrete time amplitude domains: the data converter and specifically the more performance limited is the ADC on the receive side. The limiting factor in most use cases is the performance characteristics as a function of either the input frequency or sampling rate. The motivation of TI-ADCs is to cost effectively increase the sample rate of a converter by *M* times while maintaining the level of performance at or near that of a single constituent. The top level architecture of an M ADC, TI-ADC is illustrated in the signal block diagram in Figure 2. In the figure, $x(t)$ is the analog input signal; the sample and hold (S/H) block may contain a single S/H [11], an individual S/H for each sub-ADC [2], or a number of S/Hs for groups of sub-ADCs [12] with an output of $x(k)$, followed by sub-ADCs for digitization. In the instantiation case where a single S/H feeds all M sub ADCs the bandwidth of the S/H must support an input bandwidth which is greater than or equal to $M * Fs/2$ where Fs is the sample rate of the sub ADCs. In the instantiation case where each of M/K S/Hs feed K sub ADCs the bandwidth of the S/Hs must support an input bandwidth which is greater than or equal to $K * Fs/2$ fed by a single S/H with

an M*Fs/2 bandwidth or each of the M/K S/Hs must have a M*Fs/2 bandwidth. Each of the sub-ADCs is clocked with an appropriately phase shifted clock divided to trigger the round robin sampling of each ADC. The samples are then multiplexed and the output $v(m)$ is the composite sampled signal at the $M * Fs$ rate affected by the cyclic mismatches and nonlinearities in the ADCs and the analog front end. The estimation and compensation blocks correct the samples $v(m)$ at the $M * Fs$ rate and will be discussed later.

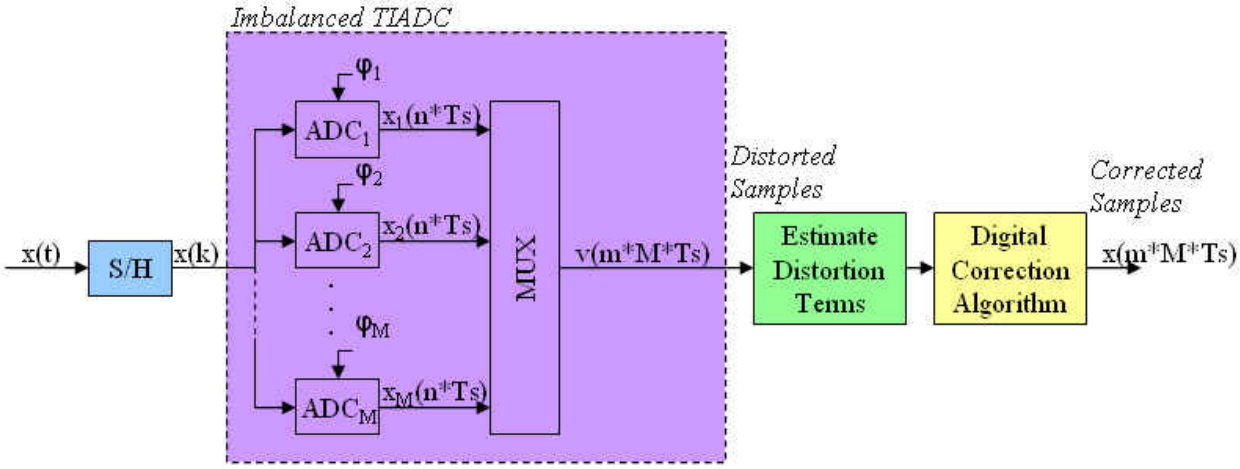

Figure 2: General TI-ADC Structure © 2013 IEEE

Power, area, performance, and cost are the variables that are balanced in any given sampling application. Computational complexity of the estimation and mismatch correction is a concern for TI-ADCs in both single device semiconductor and multiple device application specific implementations independent of the difference in non-recurring engineering (NRE) versus recurring engineering cost trade models. In the latter product space upfront matching of the converters increases the initial test time but reduces the computational power needed for correction. However even in single die instantiations of the converters the devices cannot be exactly matched and the use of analog circuitry and/or post conversion correction can only

compensate for the mismatch errors to a certain, usually inadequate, level. Additionally, analog domain calibration circuits are area consuming and digital correction algorithms are preferred in most cases for this reason and additionally for the level of compensation that they can provide. Digital correction also better lends itself to off the shelf implementations due to their adaptability and stability over time and temperature.

As previously mentioned, the differences in devices translate into what is called *M*-periodic error mismatch or simply *M*-periodic mismatches. Periodic mismatches deteriorate the performance of the composite converter structure reducing the effective performance. This problem can be addressed to some level, either online or offline in hardware or software. The purpose of this compensation is not to correct the errors of the individual ADCs, only to compensate for differences between them. Thus the ideal case is not an ideal converter but a multi-channel converter wherein all of the channels have identical transfer functions and have sample intervals which are as uniform as a single device sampling interval. In other words the goal of the compensation circuit is to make the time interleaved multiple channel data converter perform as closely to ideal sampling as illustrated in Figure 3 for a uniform staircase as one of its channels sampling at 1/M the rate and ignoring clock jitter considerations (described below).

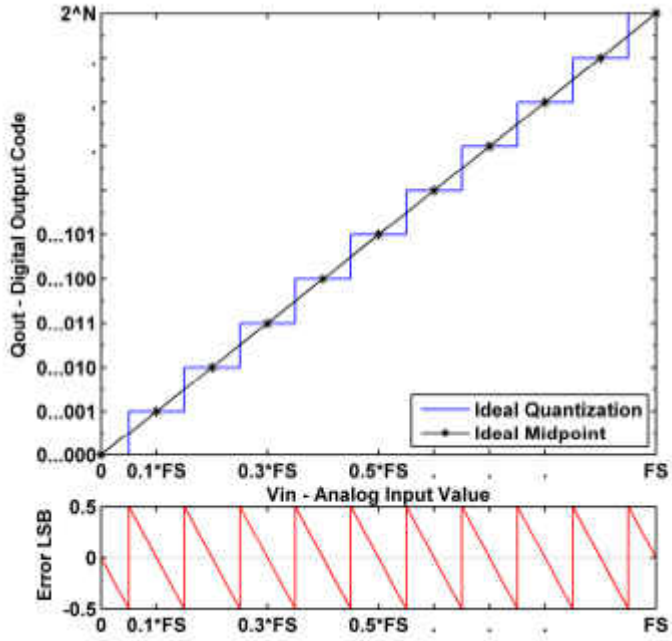

Figure 3: Ideal Uniform Quantization © 2013 IEEE

Errors

Ideally the TI-ADC system is uniformly sampled to within the required accuracy with non-periodic errors. Note two key concepts that can cause confusion: 1) quantization error is not caused by non-ideal behavior as a result of the hardware instantiation but is inherent in the quantization process, and 2) compensation in a TI-ADC is not attempting to change the transfer function of any single converter to be closer to the ideal but is meant to match the transfer functions of the multiple devices.

While non-uniform sampling is not considered in this dissertation, it is worth pointing out the generalized Nyquist sampling theory allows for non-uniform sampling and reconstruction. For a recent reference on the application of non-uniform sampling in TI-ADCs see [13]. However, non-uniform sampled signal processing is very computationally intensive. A compromise is to

generate uniform samples from the non-uniform samples. This is computationally within the realm of feasibility given *a priori* knowledge of the temporal offset of each sample. In most practical applications acquisition of said offset information is more limiting than the correction itself. In consideration of these facts the reader is once again reminded that the goal of post conversion correction algorithms is not to make the individual ADC performance better but to correct mismatches to make the TI-ADC performance approximate the single ADC performance characteristics while increasing the sample rate by correcting the periodic errors.

The following reviews the non-quantization errors of a typical ADC that is relevant to TI-ADCs and their impact on interleaved performance; the figures in each subsection visually exaggerate the magnitude of the errors so that the reader can see the impact. When realistic error levels are used they are difficult if not impossible to see in the time domain waveform with the naked eye. Actual performance is the aggregated effects of all of the errors and the aggregated effects differ device to device. By convention, first the error sources of a single ADC are described. Then how the effects are exacerbated in a 2 channel TI-ADC, Figure 4 shows the blue lines as the ideal reference ADC and the red and green lines as the two non-ideal ADCs to be interleaved. Subsequent subsections refer back to this figure in detail.

Offset

The offset error in a single converter with a bipolar input capability is the midstep value when the digital output is zero. For a TI-ADC this error is M periodic if left uncorrected as seen in Figure 4a where the sample points are the TI-ADC samples of the sinusoid. In a single converter the error affects all codes by the same amount so this is a static periodic error. In the frequency

domain, the periodic error shows up as spurs at multiples of the sub ADC sample rate *Fs*. Offset mismatch is a well understood problem with available simple solutions in the public domain, for example the use of a sinusoid to determine the value to subtract in the time domain samples of sub-ADC outputs compared to a reference channel.

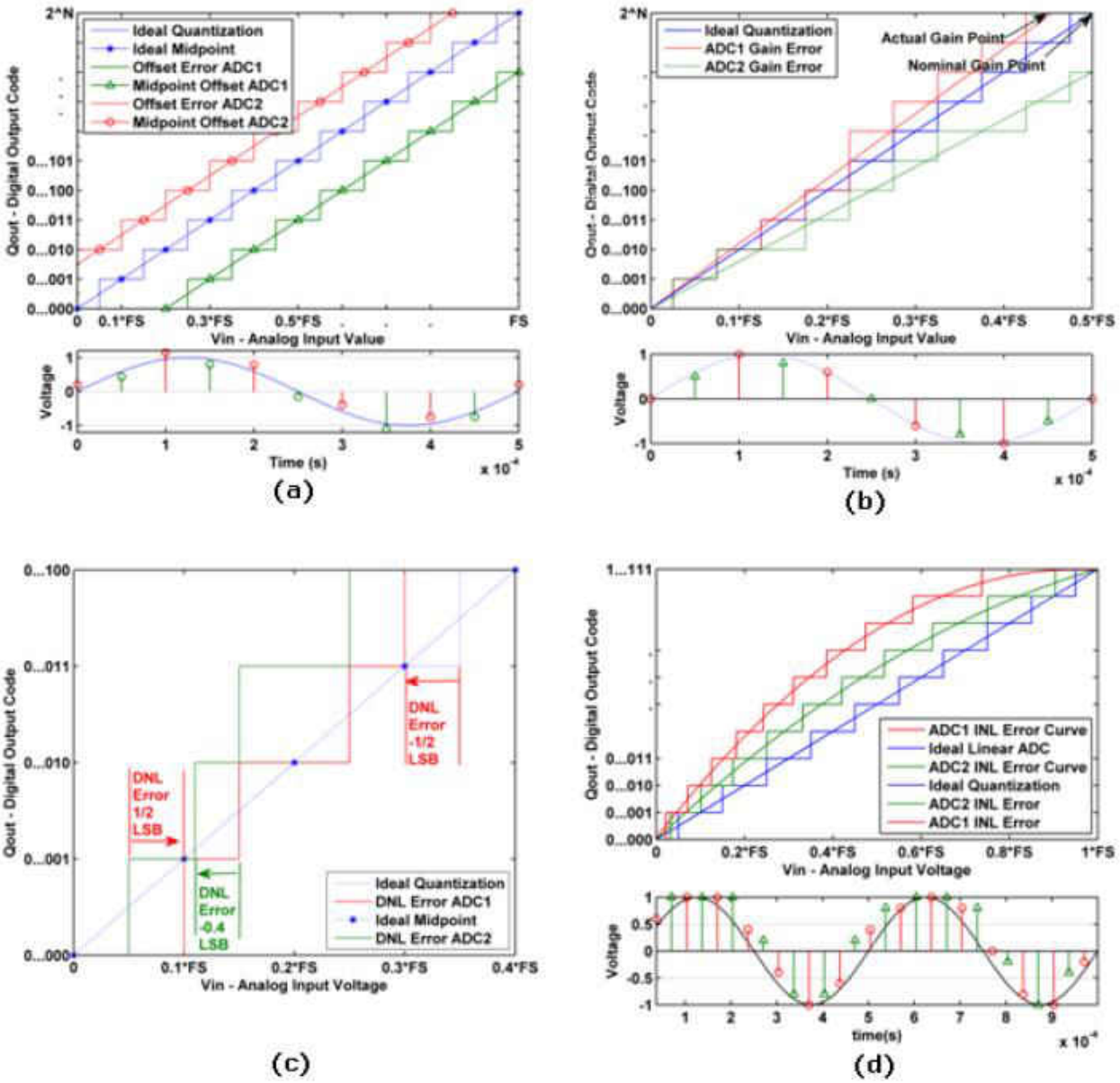

Figure 4: Stair Case Illustrations of Mismatch Errors © 2013 IEEE

Gain

Gain error for a single ADC is the difference between the nominal and actual gain points on the transfer function after the offset error has been corrected to zero. The error results in a difference in slope of the actual and ideal transfer function as seen in Figure 4b. This error, if large enough can cause missing codes as can be seen in the actual ADC staircase approximation. The mismatch effect in an interleaved system is again periodic for this static gain error, and the frequency domain spurs for a single sinusoid are located at the input frequency plus and minus multiples of the sampling rate, $\pm f_i + k * Fs$ where $k = \{0,1, \dots M-1\}$. This static mismatch is also well known and has been addressed with a single gain correction parameter multiplying the output of the non-reference channel ADCs. It is the case in implementation however that this gain error is not uniform across frequency and may not be completely matched across the entire frequency range with a single correction parameter. This nonlinear mismatch as well as the nonlinearities to be discussed later are highly dependent on manufacturing process and thus relevant information is often held as proprietary and is not well documented in the open literature. This results in its correction being a current challenge in TI-ADC research.

INL

The difference between the ideal and measured code transition levels after correcting for static offset and gain is called integral nonlinearity (INL). This is a nonlinear error that originates from various sources but typically results from semiconductor process f_T[1] limits which is also process

[1] f_T is the convention for describing the bandwidth of a semiconductor process and is formally defined as the frequency at which the maximum gain of a transistor implemented in that processes is unity.

bandwidth limitations. INL is shown graphically in Figure 4d and it has an unpredictable impact on the interleaved output. Manufacturers specify the effects of INL in a few different ways; the most descriptive plots related to INL show the spurious free dynamic range (SFDR) of the converter as a function of frequency. This particular parameterization is useful in sub sampling applications that tend to exploit the full input bandwidth of the ADCs analog front end but not its logic circuitry. Again, this periodic nonlinear mismatch is unpredictable in its combination across frequency but can be characterized via measurement.

Aperture Delay and Jitter

A limiting factor in high speed applications, especially in subsampling, is the uncertainty of the sampling aperture. Aperture jitter is the source of error in the temporal dimension of the error "fuzz ball" around each converted sample. (The other dimension being the dimension of the quantity being measured, e.g. voltage.) The aperture is the time window of deviation from the ideal sampling instant. This causes a deviation from ideal equal samples of the measurement of the input to the ADC and therefore affects the output. Any deviation from ideal uniform spacing manifests itself as a frequency dependent amplitude error. Individual ADCs have an overall aperture delay which is static and results from a fixed sampling clock propagation delay. As this is a fixed delay it is a measurable fixed delay in the output. However when interleaving this delay is no longer constant but periodic as seen in Figure 5 and is one aspect of the timing mismatch when interleaved. At any given tonal frequency it is a periodic phase modulation with phase increasing linearly with frequency. In the figure the black sample points and times indicate

the ideal sample location and the green triangles and red circles indicate the extremes of where the sample might be taken in time for each sample.

Error compensation for aperture delay mismatch has been well researched and the four methods often used to correct this Skew are interpolation, blind compensation, fractional delay filters and the perfect reconstruction method, more discussion of these methods can be found in [14] and its references. As inferred above, constant time offset looks like a phase dependent amplitude error a.k.a. a fixed phase offset.

Aperture jitter or aperture uncertainty is generally specified as the standard deviation of the sampling time, also called timing jitter and timing phase noise. This standard deviation defines a Gaussian distributed random process which defines one limitation of the maximum frequency of the input. Figure 5 illustrates both periodic delay and jitter. Though the sample times are shown in Figure 5a as periodic delays, Figure 5c shows the distribution of the sample time that could actually occur. This jitter impacts estimation and correction of the mismatch.

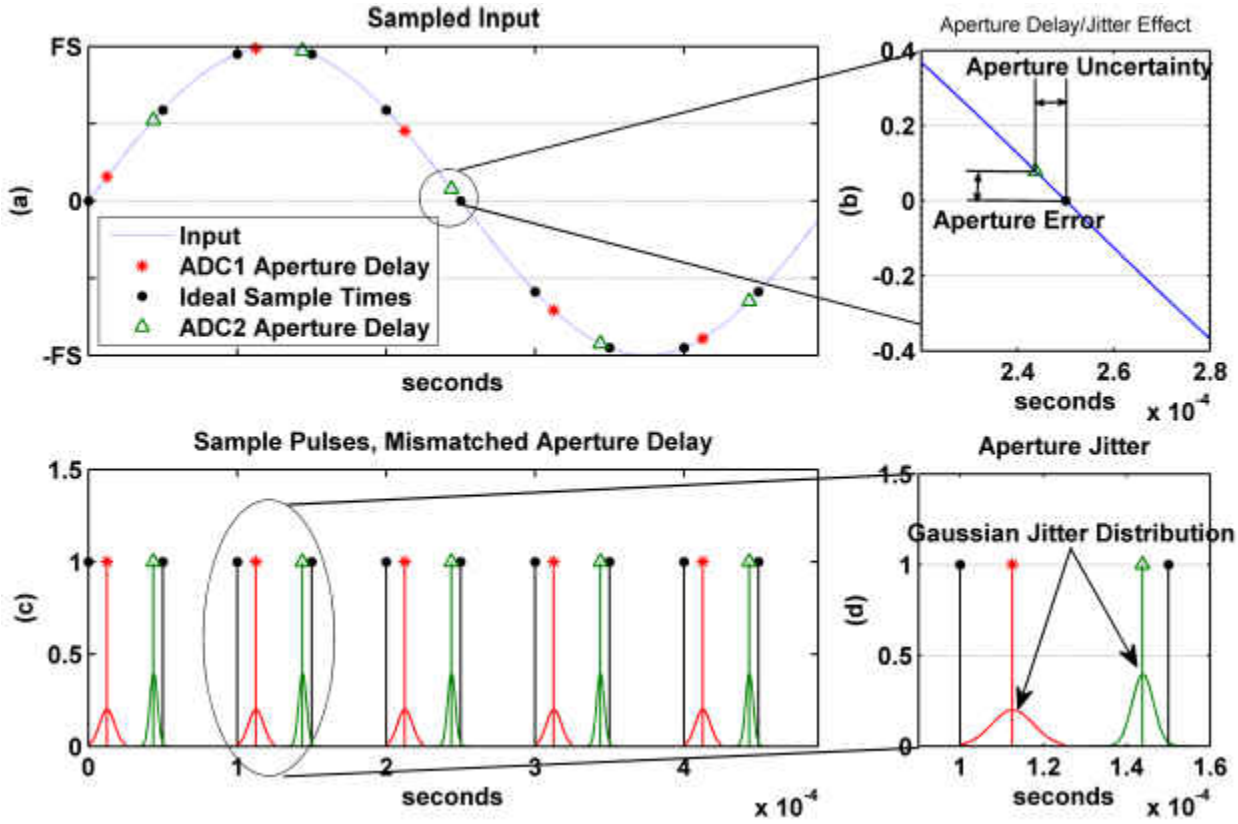

Figure 5: Aperture Delay and Jitter Mismatch © 2013 IEEE

Analog Front End and S/H errors

Some architectures require the use of a S/H for each sub-ADC which can introduce bandwidth mismatches and nonlinear mismatch errors when interleaving due to the nonlinear behavior inherent in S/H circuits. Today most S/Hs are integrated into the ADC however it is important to understand the operation of the S/H as it contributes to the dynamic performance of the ADC and the mismatch errors encountered in TI-ADCs. S/Hs may also need to be used as additional discrete components in the time interleaving circuit to allow for the desired higher BW of interleaved sampling rate.

ADCs use comparators or capacitors to convert an analog input to a discrete value, continuous variations in the input cause errors in the conversion. The S/H is used to eliminate these variations by maintaining the input to the ADC at a constant value during conversion. A simplistic S/H can be realized as a switch and a capacitor. When the switch closes current flows, charging the capacitor this is the sample stage. The charging time constant is proportional to the input impedance and the capacitance. When the switch opens the capacitor discharges over a period proportionate to the output impedance and the capacitance this is the hold stage. When the input impedance is zero and the output is infinity the S/H performs ideally with the input being sampled very quickly and held for infinity. This is impossible however, and implementation requires tradeoffs.

If the capacitor is large, switching errors are minimized with a stable hold period but the performance of the circuit is not ideal and a smaller capacitor is needed for fast sampling. This is because the capacitor charging time depends on the time constant set by the size of the capacitance and on the resistance of the switch. Any resistive load on the output will cause an error in the voltage held by discharging the capacitor when the switch is opened, when this error is greater than ½ LSB before the conversion is complete, the problem needs to be addressed. Operational amplifiers are used to mitigate this problem.

The simplest implementation structure is made up of an input buffer amplifier, the switch and capacitor and an output buffer. Others structure exist with various benefits and drawbacks, but the specifications that describe S/H operation in its four states, sample mode, sample to hold transition, hold mode and hold to sample transition are the same. During sampling the static

specifications of concern are offset, gain error and nonlinearity and the dynamic specifications are settling time, bandwidth, slew rate, distortion and noise. The transition from sample to hold specifies the pedestal, and pedestal nonlinearity static behavior and aperture delay time, aperture jitter, switching transient, and settling time dynamic behavior. During the hold period static behavior of concern includes droop, and dielectric absorption; feedthrough, distortion, and noise as the dynamic. Finally the hold to sample transition specifies the dynamic performance of acquisition time, and switching transient.

The dielectric absorption is of particular concern because of the memory effect introduced that allows the previous sample to contaminate a new one, introducing random errors. This memory effect and other nonlinear effects introduced by the S/H forces compensation in the form a Volterra series filter. The Volterra series inverts the nonlinearity with a nonlinear series with memory. Satarzadeh, Levy and Hurst show in their 2009 paper that modeling of this nonlinearity can be achieved with a Volterra series expansion and compensation can be achieved at the cost of oversampling and linear filters cascaded with digital mixers [15].

It is possible to implement a time-interleaved system with individual S/Hs per interleaved ADC; however an additional level of mismatch is introduced through the unique parameters inherent in each S/H mentioned above, particularly offset, gain, nonlinearity, bandwidth, aperture delay and jitter. While the aperture delay of a single S/H is not an error, differences in delay introduce a periodic mismatch delay. However the use of two stages of S/H where the first stage is a single S/H that sets the sampling instant and the second stage of interleaved S/Hs does not contribute to time Skew interleaving errors is possible [11].

Combined Time Interleaved Mismatches

Taking the example of four time interleaved ADCs in this subsection, the components are independent parts driven by the same clock source with their own specific internal and external characteristics such as clock delay due to layout and manufacturing variances. When individually analyzing each error and their mismatch, the frequency domain characteristics measured and the contributing mismatches can be at least partially identified. However this is more difficult in the interleaved case. The time variant spectral characteristics resulting from mismatch errors with unknown aggregation features can combine to create greater or lesser harmonics due to the relative differences between individual ADC transfer functions. Examples of the combined mismatch errors are shown in Figure 6 and Figure 7. The behavioral model that is detailed in chapter 2 was developed as a part of this research and previously published in [16, 17] was used to simulate the interleaved system with errors specified in the extreme to extreme range of a high performance ADC data sheet [18].

The linear distortions might be approached with the use of M FIR polyphase filters in each of M lower rate channels or an M periodic FIR filter at the higher interleaved rate whose filter coefficient are periodic. However these schemes do not address the nonlinear errors from the gain, DNL, INL and S/H(s) in the system. There is very little published work in this area, and the few that have addressed the topic suggest varying methods of compensation, one such method is the Volterra series based nonlinear polyphase filter [19, 20].

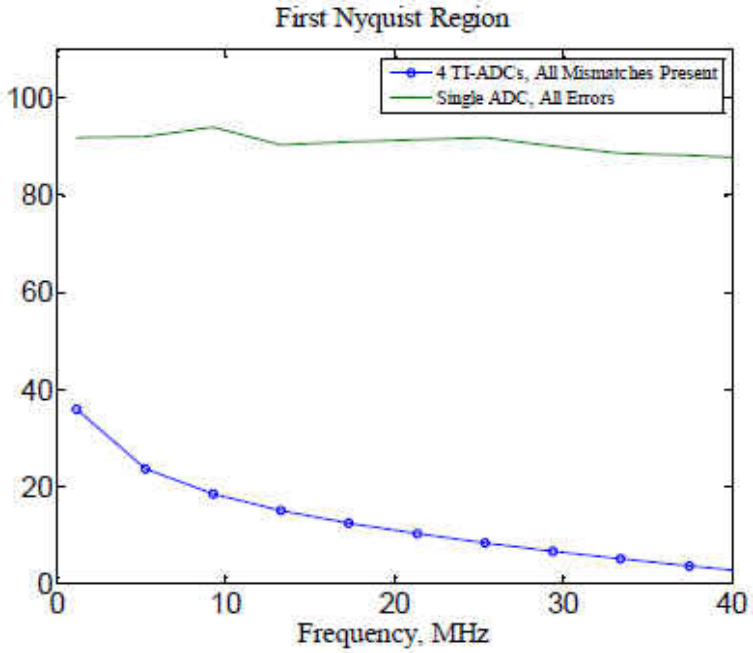

Figure 6: TI-ADC SFDR vs. Frequency © 2011 IEEE

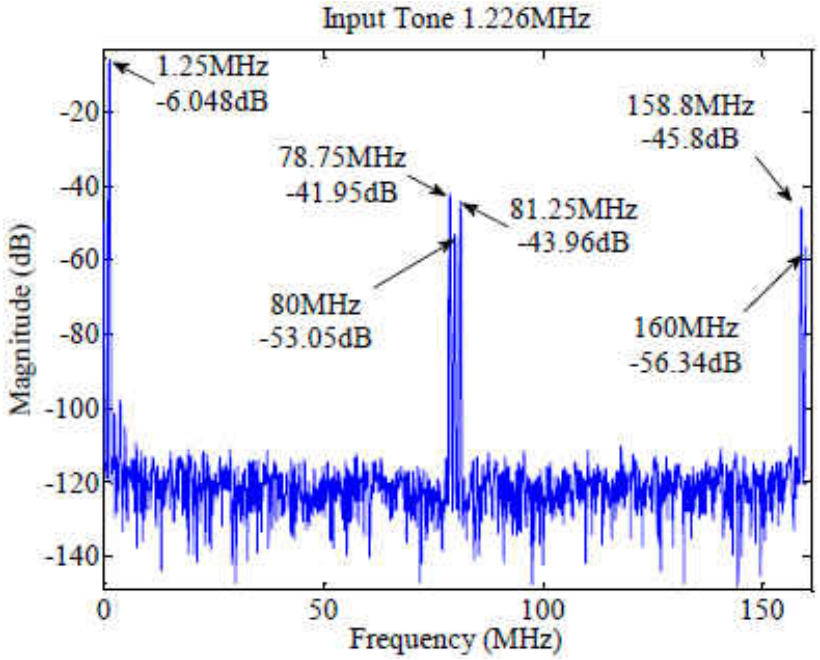

Figure 7: TI-ADC Spectrum with Mismatch Errors Identified © 2011 IEEE

Mismatch Correction

As stated above, the goal of post conversion correction algorithms is not to make the individual ADC performance better but to correct mismatches to make the TI-ADC performance approximate the single ADC performance characteristics by eliminating the periodic errors resulting from device and physical implementation mismatch. One method is to utilize one channel as a reference while all other channels are compensated to match the reference by producing the inverse of the differences of the responses. This is a realizable compromise to the theoretical ideal of taking the inverse of each channel with respect to the ideal sampling response. If the ideal of perfect compensation were physically realizably then there would be no need to interleave ADCs let alone use post conversion correction to match their performance.

There are two main categories of correction methods: online and offline, which can be done in the foreground or background, with active or passive correction. Here we use the term online to mean that the TI-ADC is in use while the correction is being made i.e. a post conversion correction in real time. Offline is either hardware based, where characterized converters are matched to each other, or static correction methods that do not take into account time-varying characteristics of the transfer function and their impact on ADC performance. Online methods allow for periodic or continuous updating of the mismatch compensation.

Foreground methods require the periodic or event triggered interruption of the normal operation of the subsystem so that a known input sequence can be applied and compared to the expected output, that is the application of a data driven adaptive correction methodology. This methodology is most viable when the host system has an *a priori* need for known sequences as is

found for example in communications systems requiring a known header, frame sync, etc. appended to an incoming message. Background techniques allow for the continued normal operation of subsystems, including a TI-ADC.

The described methodologies can be used in various combinations. For example, in either foreground or background techniques, active or passive methods may be used. Active implies the use of a known injected signal, while passive assumes the method is blind or semi blind (where nothing or very little about the incoming signal is known *a priori*) utilizing the unknown signal for correction. Background methods are limited in the measurement and correction of errors to a typically out of band frequency range that is excited by the unknown signal or by having an extremely low level in band signal. Additionally, background methods typically require fast adaptation or correlation based error detection to make them beneficial Table 1 summarizes the section by listing advantages and disadvantages to the mismatch correction methods; this table is not exhaustive but rather gives examples of each type of method discussed.

Table 1: Categories of Mismatch Correction Methods

	Online	Offline	Example	Advantages	Disadvantages
Active, Foreground	X		Providing a calibration mode that is activated through software in the field such as with instrumentation.	Could allow for more accurate correction of mismatches with the use of a clean test signal over the desired frequency range	Requires interruption of the system and does not automatically correct for long term varying errors such as temperature
Active, Background	X		Injecting a tone in a known vacant area of the spectrum.	Allows for short term and long term adaptation to errors. Can take advantage of existing architectures	Limited to correcting the errors present or measurable at the tone frequency of interest
Active, Foreground		X	In the production and or system testing phase a chirp is used to determine TI-ADC system response.	One time correction, allows for reduction in computational complexity due to relative simplicity of static correction	Requires hands on individual testing of each system. Does not adapt over time to error changes
Passive, Foreground	X		A Software Defined Radio will be receiving frame syncs in front of each message. These are used to adapt the correction.	A known signal is available, which could allow for faster or better error reduction.	Overhead to the message is required, if adaptation is not able to finish with one message performance can be temporarily reduced.
Passive, Background	X		An adaptive blind method is used to adapt a polyphase filter bank to reduce frequency response mismatch.	No additional signal required, allows for short and long term adaptation to errors.	Computational complexity may be high, an additional FPGA will be needed to perform the correction.
Passive, Foreground		X	Utilizing in house testing of the ADCs closely match the responses of the hardware.	Requires no additional computational complexity	Does not take advantage of correction structures and performance will suffer. Does not adapt to changes over time.

The performance improvement limitation of any method used to correct mismatch errors in TI-ADCs is the performance of the individual ADCs, S/H(s), the clock characteristics, and the uniformity of the layout used in the implementation of the subsystem. We seek to improve the performance of the interleaved data converter subsystem, dominated herein by its SFDR, to that

of a single constituent ADC while increasing the sample rate. Other limitations may include channel limitations due to size, weight, and power (SWaP) requirements, noise, clock stability etc. Clock stability is the ultimate limiter of sampling accuracy in any data conversion operation due to limitations imposed by aperture jitter.

To better illustrate some of the research ongoing in TI-ADCs, Table 2 details a subset of the latest publications on implemented TI-ADCs spanning 2 to 128 channels and up to 6 sub-ADC architectures. Exclusively simulation results are not included in this table.

Table 2: Select Fabricated TI-ADCs

Reference	**[38]**	**[34]**	**[33]**	**[37]**	**[39]**	**[35]**	**[36]**
Channels	2	4	8	16	24	64	128
Resolution (bits)	14	7	6	11	11	10	7/8/9
ENOB	*11.2525	6	4.9	*6.6844	8.1	*7.7641	*6.186/7.0166/ 8.0133
Sample Rate (Gsps)	0.2	2.2	16	3.6	2.8	2.6	1/0.5/0.25
Architecture	Pipeline & Flash (7 & 1 per channel)	Subranging	Flash	SAR	SAR	SAR	Channel counter ADC aka single slope converters
Compensation Method	LMS-FIR and interp filter. Corrects offset, gain, BW and sample time error.	Distributed resistor array for gain, digitally corrective current sources for offset, nested T/H for timing	Digital offset and timing skew, using an on chip cal signal	Startup and bkgd cal	Two extra SAR for calibration using LMS weight update	Startup on chip cal for offset and gain mismatches as well as DAC linearity	Cal of the devices at statup and at regular intervals using foreground cal and continuous correction
Complexity	Un-specified filter lengths	Analog Circuitry, a resistor network and additional T/H of high BW	One Random chopping latch, Two Choppers, & a zero crossing detector	2, 12b current steering startup caldacs	Extra hardware & simple LMS	Un-specified	Buffer shifting and subtraction
Power (mW)	460	40	435	795	44.6	480	26.5/26/25.3
Supply(V)	1.8	1.15	1.5	1.2/2.5	1.2	1.2/1.3/1.6	1.2
SNDR (dB)	69.5@ 15.3MHz	38@ 1080MHz	30.8@ 170MHz	42@ Nyq	48.2@ Nyq	48.5@ Nyq	39/44/50@ Nyq
Active Area (mm^2)	15.2	0.2	0.93x1.58	7.44	1.03x1.66	5.1	0.55

*calculated based on SNDR, not reported

CHAPTER 2: METHODS AND MATERIALS

A key stumbling block to cost effective research and development for improving TI-ADC performance is the availability of high fidelity, high level models for simulations incorporating realistic error performance of data converters. Without realistic high level models researchers are forced to use simplified approximations that are inadequate from the point of view of both error sources and fidelity, spice models that are too costly to develop and time consuming to run, or hardware based emulation which forces the use of expensive hardware based simulations and does not allow researchers to selectively apply error sources to facilitate effective evaluation of the correction algorithms under development. The Simulink^{TM} model presented herein simulates high performance ADCs tuned to emulate the performance of known commercial off the shelf (COTS) devices. This model can be generalized to M analog-to-digital converters and serves as a basis for the research described herein.

In this dissertation four ADCs are used in an interleaved configuration to serve as the base example. The following subsections discuss the behavioral model and presents statistical properties of the mismatch errors. In some simulations a polynomial model is used to compare performance to other methods of post conversion correction; the implementation is also described here. For completeness a survey of recent correction methods is presented and their models and methods noted at the end of this chapter and it is used for comparison in a later chapter.

Design of the Behavioral Model

As a research and development tool the goal of the behavioral model is to closely approximate the behavior of the dominate error sources in an ADC such that when combined, the overall ADC simulation represents the behavior of that ADC to a required fidelity without the use of expensive time consuming Spice models or the inflexibility of hardware in the loop. To this end each error source is modeled independently so that they can be individually enabled as desired to aid the performance evaluation process.

Table 1 shows the parameters used from the Maxim 12554 14 bit, 80Msps, 3.3V ADC to configure the model. Since the converter has a wide input bandwidth and supports subsampling, the error model must likewise support these capabilities. Figure 8 shows the top level diagram of the implementation of the behavioral model of a 4 channel TI-ADC in Simulink™. The input sine wave sampling rate is 9 times the interleaved rate of 4**Fs* where *Fs* is the sub-ADC (per channel) sampling rate. It is important to note here that the 9 times oversampling is required in the model to relax the filter requirements on the implementation of the Farrow filter structure introducing jitter as well as supporting subsampling behavior for the INL and gain errors and is not based on an actual hardware instantiation requirement. This oversampling requirement shall be discussed in the description of the aperture jitter section detailing the Farrow resampling filter below.

Table 3: MAX 12554 Datasheet Characteristics and Parameters

Parameter	Data Sheet Values	Model Values
FS Range	+/- 0.35V to +/- 1.10V	+/- 1.10V
INL	+/-2.4 Typ, +/-4.9 Max (LSB): at 3MHz	Used Plot across Freq
DNL	-1 Min, +/-0.5 Typ, +1.3 Max (LSB): at 3MHz	Used Plot across Freq
Offset Error	+/- 0.1 Typ, +/- 0.72 Max (%FS)	+/- 0.1 %FS
Gain Error	+/- 0.5 Typ, +/- 4.9 Max (%FS)	+/- 0.5 %FS
Aperture Jitter	<0.2 ps RMS	0.2 ps RMS

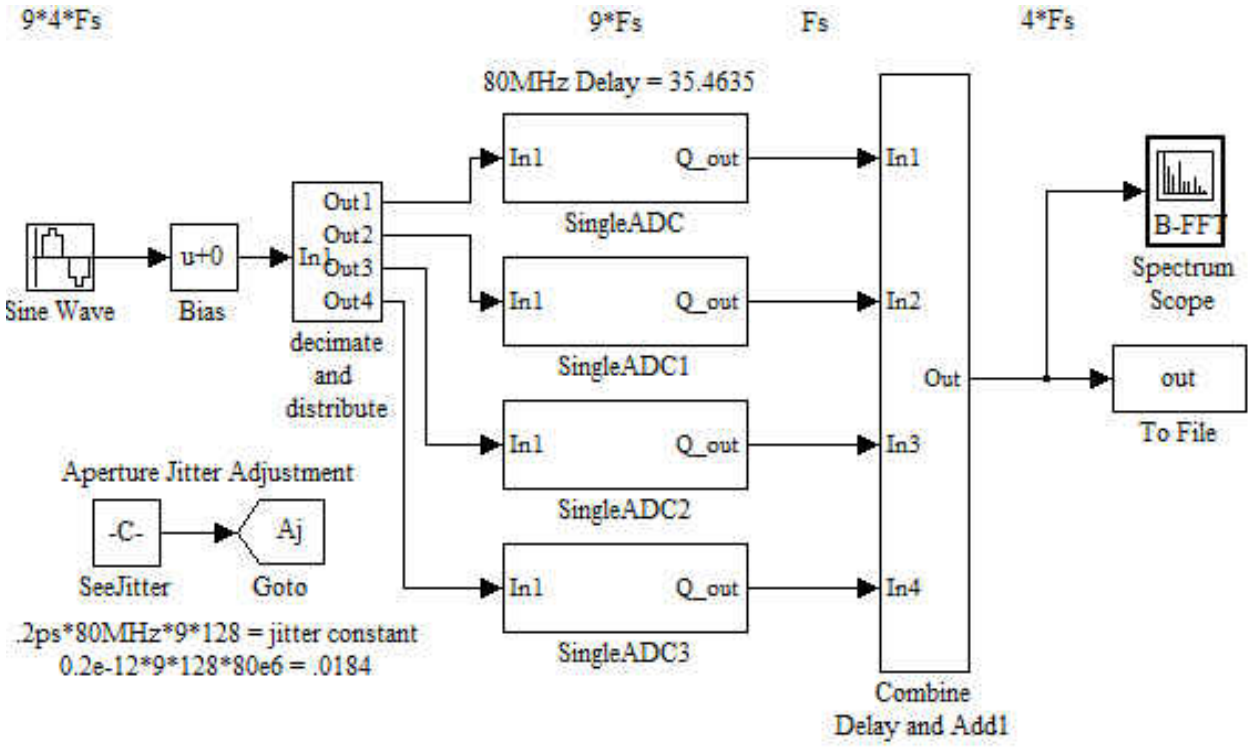

Figure 8: Top level view, 4 Channel TI-ADC Behavioral Model, Simulink™

Figure 9 shows a top level block diagram of the single ADC Simulink behavioral model and its error source control mechanism. As seen in the figure each error source has an individual control bit that is set to enable the corresponding error source model. This enables the analysis of the

effect of the correction algorithm under evaluation on the error sources individually and in all possible combinations.

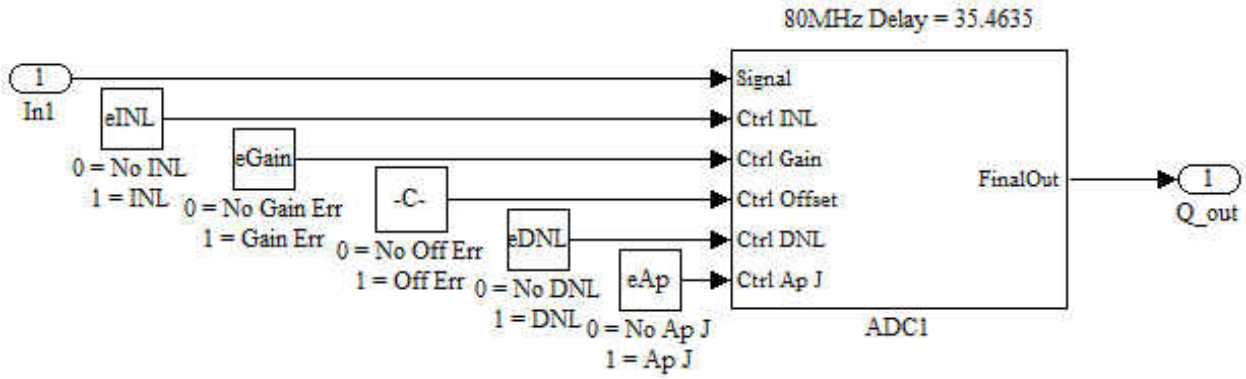

Figure 9: Single ADC block view, illustration of enabling errors, Simulink™

Error Implementations: Offset, Gain, Quantization, DNL, INL

The device targeted for description in this dissertation has a constant DC offset of 0.1% full scale (FS) [40]. This error is seen in the spectrum of the output as a non-zero value at DC. In the model, offset error is modeled by adding a constant to the signal prior to digitization as shown in Figure 10. If left uncorrected, when interleaved, the distortion due to mismatch manifests itself as harmonics of $k * Fs/M$, where Fs is the interleaved sampling rate, M is the number of converters interleaved, and k is an integer; 1,2, 3,4 . . . [41].

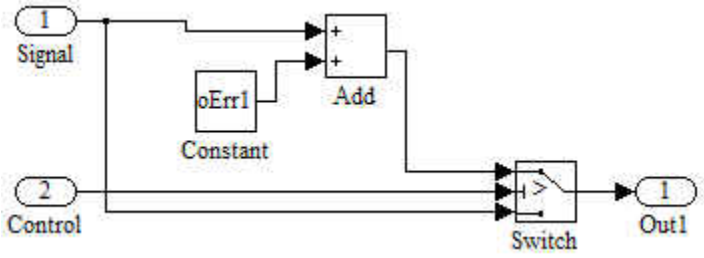

Figure 10: Offset Error Implementation, Simulink™

Gain error is modeled by an equiripple gain deviation from the ideal as shown in Figure 11. Though this is a simplistic implementation it provides a worst case scenario. The proposed correction algorithm does not take unique advantage of the equidistant peaks and these peaks allow multiple gain errors at the maximum. This is accomplished with a polynomial approximation in the passband region of interest. The ripple as a function of frequency is described in linear terms, consistent with the published data for the device being modeled, is calculated within the band of interest as $D_{pass} = FS * E_{gain}$ where FS is the full scale value and E_{gain} is the percent of full scale gain error as specified in the characterization of the device. This error manifests itself in the frequency domain as amplitude ripple. It should be noted that the gain errors can usually be trimmed by the user; however with multiple interleaved ADCs, if left uncorrected, the mismatch distortion will be present in the spectrum at $\pm f_i + k * Fs/M$ [42].

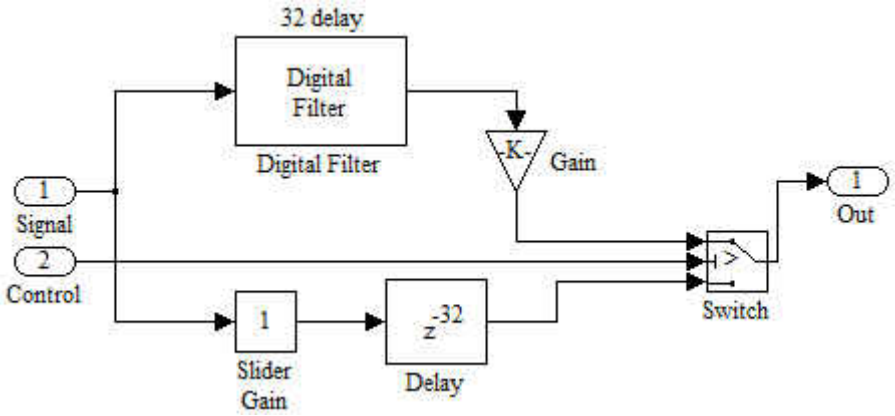

Figure 11: Nonlinear Gain Error Implementation, Simulink™

The quantizer component of an ADC converts a discrete time, continuous voltage sample into a discrete time, discrete voltage sample where the voltage is represented as a numerical value. DNL error is due exclusively to the encoding process [43] and can be combined with quantization error as non-uniform quantization levels. That is, ideally the transition voltage

between consecutive codes should be uniform and DNL characterizes the deviations from the ideal spacing.

A statistical distribution of the DNL error is used in this model. In this model it is assumed that the error mechanism is a stationary random process related to the manufacturing process, uncorrelated with the input, and a white-noise process. Ideal quantization is a uniform probability distribution over the range of quantization that is commonly described with the following statistical representation.

For small quantization levels Δ, it is assumed that the error due to quantization, $e_Q[n]$ is a uniformly distributed random variable from $-\frac{\Delta}{2}$ to $\frac{\Delta}{2}$. Assume also that successive noise samples are uncorrelated with each other. The mean value is zero and the variance is $\sigma_e^2 = \int_{-\Delta/2}^{\Delta/2} e^2 \frac{1}{\Delta} de = \frac{\Delta^2}{12}$. DNL error can be combined with the above formulation of quantization error by no longer assuming that Δ is a constant width.

Figure 12 shows the implementation of quantization and DNL in Simulink™. When modeling quantization the provided quantizer block is ideal and thus passes its input through a stair-step function so that a certain interval is mapped to one level at the output. The output is computed using the round-to-nearest method which produces an output that is symmetric about zero. The spectrum effect is that of an additive uniform noise process. The DNL plot in the characterization of the target device shows that error appears to have an approximate uniform distribution across digital output codes with a mean around -.15 LSB (least significant bit) and a range of 0.7 LSB. NOTE: the actual error mechanism is likely more precisely a truncated Gaussian process but the

uniform distribution used in the model provides the required accuracy without the added complexity of truncating a Gaussian distributed noise source. This is reproduced in Simulink™ using a uniform random number generator with a minimum set to 0 and max set to 0.7, 0.5 is subtracted from the number to adjust the mean. This number is then multiplied by the quantization interval to convert to the scale relative to the size of the LSB and added to the incoming signal to model DNL. Distortion products depend on the amplitude and positioning of the DNL along the quantizer transfer function. As can be deduce from the description of DNL, for lower level signals the harmonic content becomes dominated by the DNL and does not generally decrease proportionally with decreases in signal amplitude. INL in contrast determines the distortion of nearly full-scale signals [43].

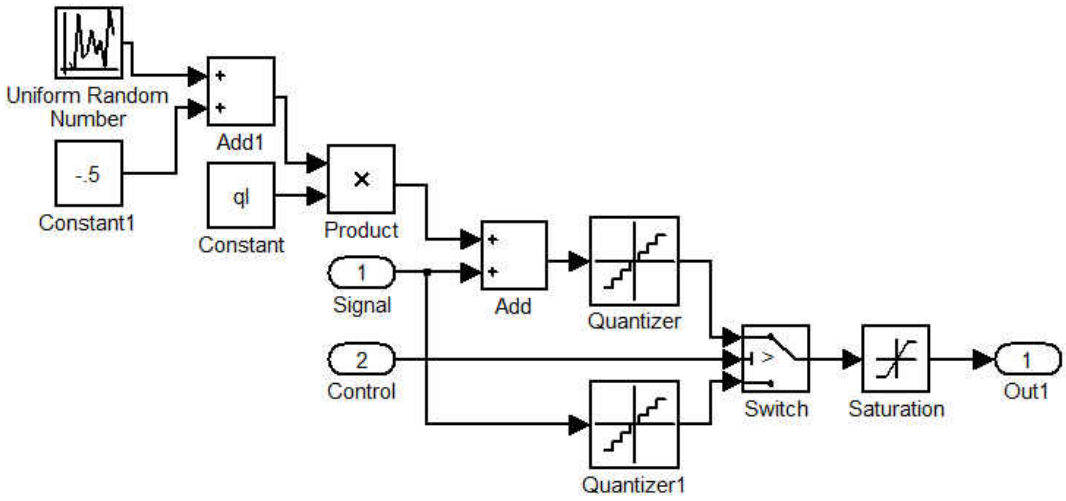

Figure 12: Quantization and DNL error implementation, Simulink™

The sample and hold component of an ADC ideally samples a continuous time signal at equally spaced time intervals and holds the sampled voltage fixed while the quantizer measures the voltage to the accuracy of its minimum quantization level. In simplistic terms, the sample and

hold is an ideal analog switch and an ideal holding amplifier. In practice these requirements present a conundrum. Capacitance is required to track and hold the input voltage. To track a signal varying with high frequency content requires a low capacitance. However, to hold the voltage constant during the quantization process requires a high capacitance. (To be completely accurate it is the resistance-capacitance (RC) products that must be low and high.) These conflicting requirements force design tradeoffs to be made and the conflicting requirements are magnified in sub-sampling application spaces of which TI-ADC are inherently members.

Conflicting requirements like those just described coupled with the bandwidth limitations of any semiconductor process introduce INL. INL is due primarily to the nonlinearities, slew rates due to device bandwidth limits, etc. in the analog front end of the ADC. This includes the sample and hold amplifier as well as to a lesser extent the overall nonlinearity of the ADC and is ultimately influenced by the process f_T, the frequency at which the transistor current gain drops to unity, an indicator of process bandwidth.

Distortions produced by INL have amplitudes that vary as a function of the input signal amplitude and frequency. The location of the spurious harmonics can be calculated based upon the input signal's span of frequency components, amplitude and on other factors affecting the specific ADC transfer function. For an interleaved configuration with INL mismatch errors, spurs from multiple ADCs can interact to create worse or lesser harmonics depending on the periodically varying combined spectrums of the ADCs.

To model this type of error practically one must use the representative measured INL characteristics of the ADC being modeled as a performance template. The SFDR plots relate the

input frequency and amplitude of the signal from which INLs can be derived. By analyzing the characteristic data for this parameter family, a sufficient approximation to the lumped nonlinearities can be produced. For the model described herein the lumped integral nonlinearities were modeled as frequency dependent amplitude nonlinearity. This can be seen in Figure 13 where the first digital filter channelizes the input into frequency dependent segments in which nonlinearities are introduced as a function of frequency and amplitude, the mu law compressors generate nonlinearities as a function of amplitude and the second digital filter recombines the frequency dependent nonlinear channels back into a single contiguous composite channel.

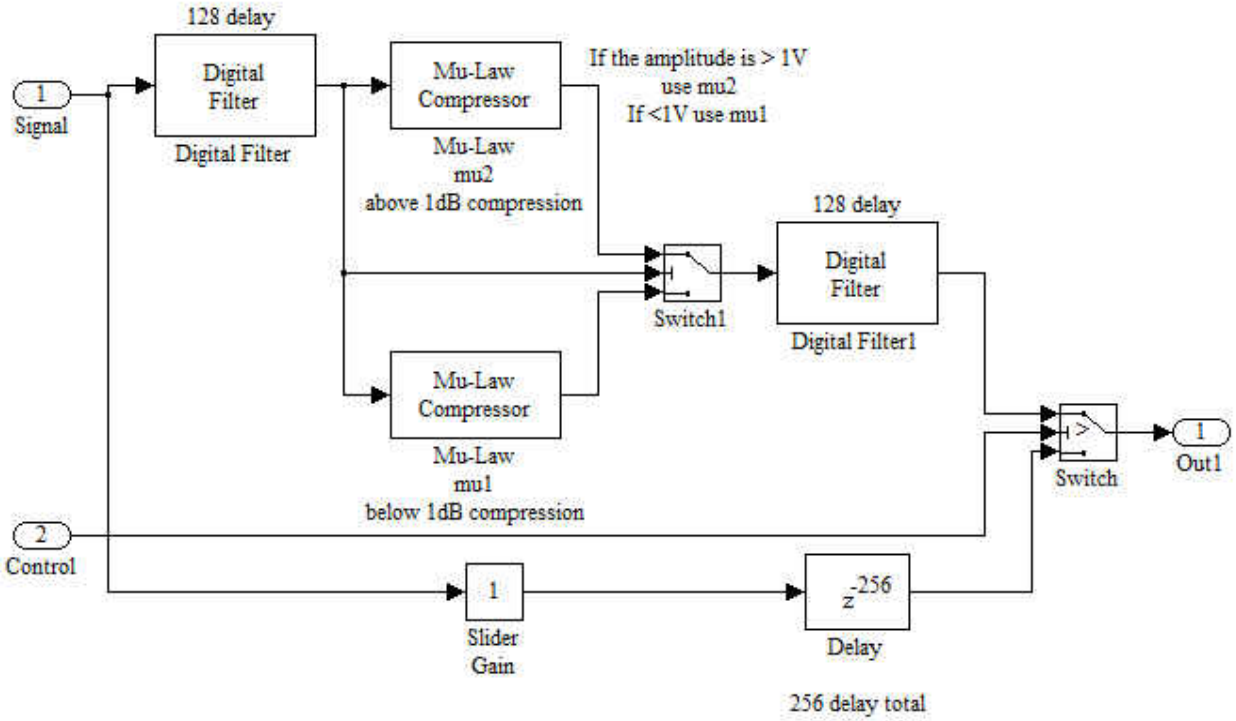

Figure 13: INL Error Modeling in Simulink™

Aperture Jitter

Quantization of an analog signal into a discrete time digital signal is a two dimensional process. To this point error sources in the amplitude dimension have been discussed. The other dimension is temporal and although non-uniform sampling is valid from a theoretical perspective, it is complex to practically implement, especially for random sample times. (In practice the two dimensional quantization error sources are vernacularly referred to as the error "fuzz ball.")

In high performance data converter implementations, especially subsampling implementations, aperture jitter is usually the dominant temporal error source and the overall performance limiter of the conversion process. Aperture jitter is driven by the highest input frequency. In real input Nyquist sampling implementations, the highest input frequency is approximately equal to the converter's Nyquist frequency. In subsampling implementations aperture jitter requirements are driven by the highest intermediate frequency (IF) signal frequency input to the subsampling ADC.

Any aperture jitter manifests itself as breaking the assumption of equally spaced samples input to any subsequent digital signal processes and can be viewed as phase modulation (PM). When using multiple sampling phase offset ADCs, a constant sampling clock offset is introduced between the ADCs creating an additional and deterministic PM. The mismatch distortion is located at intervals of $\pm f_i + k * Fs/M$ [42].

In modeling aperture jitter, a Farrow filter with the timing offset signal driven by a Gaussian random number generator is used to emulate continuously deviating sample times of the input signal in the Simulink™ model. In order to relax the interpolation filter requirements the

sampling rate of the input data is set at 9 times the required rate for the rest of the simulation and then additionally interpolated 128 times to meet the desired delay times to be introduced. This structure is shown in Figure 14. The Farrow structure is accurate for only small frequencies compared to the overall bandwidth. The data sheet of the converter which is the example for this dissertation specifies the aperture jitter typical in the ADC as <0.2ps. For the 14-bit ADC 0.2ps corresponds to 97.14MHz before the aperture jitter causes more than ½ LSB of sampling error as described by reorganizing the maximum jitter Equation in 1 to find f_{max}.

$$t_{j,max} = \frac{1}{2\pi f_{max} 2^{N-1}} \quad (1)$$

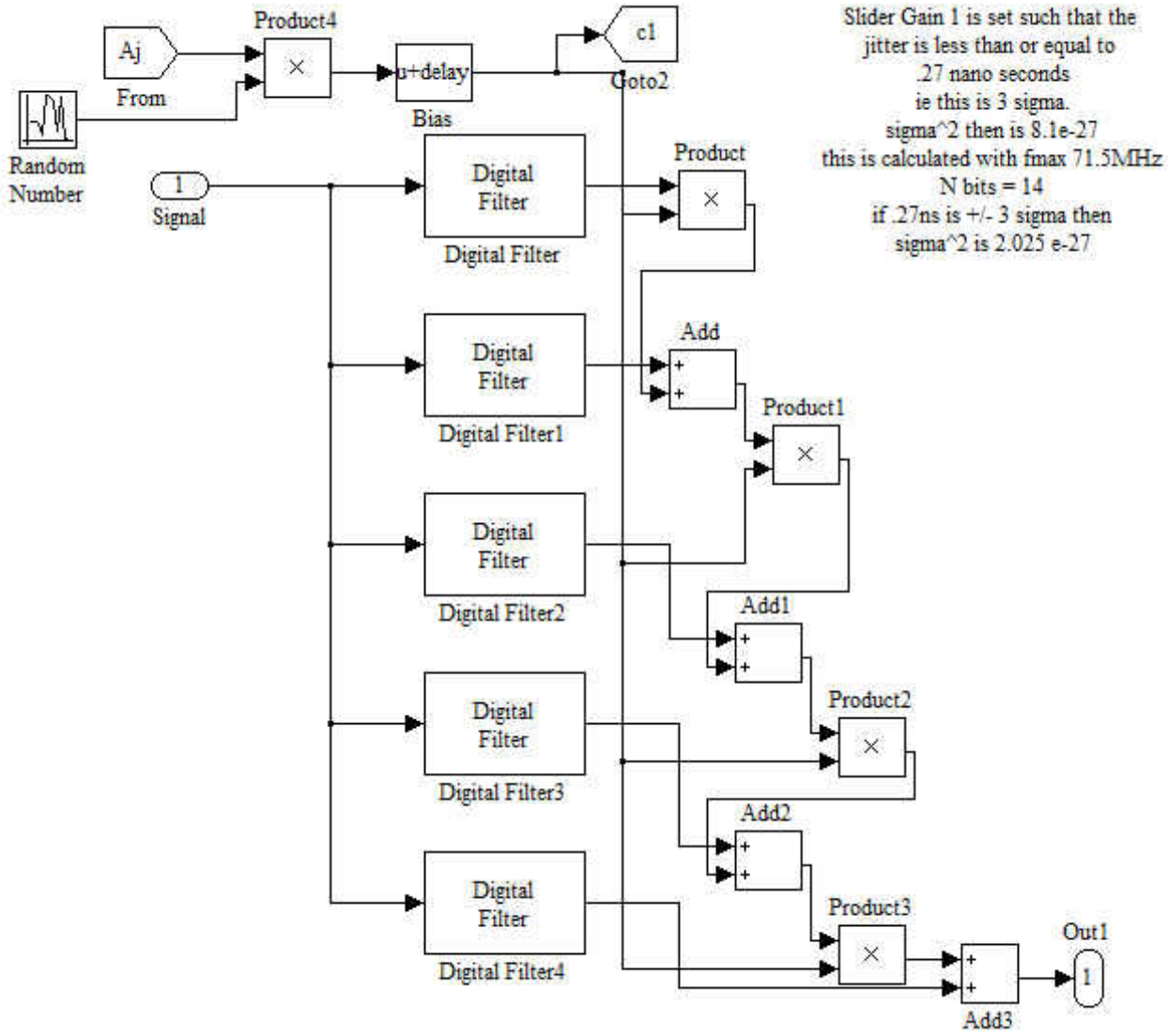

Figure 14: Aperture jitter implementation, Simulink™

Cumulant Statistics

Identifying, classifying the source, and quantifying the presence of errors in ADCs and TI-ADCs is fundamental in the pursuit of correcting these errors. This problem, characterization of error effects as a function of error source and mechanism is investigated through calculation of higher

order statistics on the error signals of each type of error source individually and combined in a single ADC and time interleaved configuration.

The concept of the calculation of high order statistics and their interpretation in the context of this dissertation is presented and applied to time varying error environments and input signals. The behavioral model allows for isolation of the errors sources in the device as well as any varying combination. Second order statistics are sufficient whenever the signals can be completely characterized by the first two moments. If the desire is to characterize Gaussian signals, this would be sufficient but the errors that are being characterized in this study benefit from higher order statistics. Cumulants of a Gaussian random process greater than the second order are zero (if excess Kurtosis is considered the fourth order statistic). All distributions except the Gaussian do not have a finite number of non-zero cumulants (statistics), shown by Marcinkiewicz [44]. Using higher order statistics, a departure from Gaussianity can be exploited, such as in nonlinear system identification.

Background on the first eight order statistics is described further in the following subsection. The method of computation and results of the higher order analysis is also presented and discussed.

Cumulant Equations

Cumulants are the coefficients in the Taylor series expansion of the cumulant generating function about the origin. The first two cumulants are equal to the first two moments, the mean and the variance. However, higher order cumulants are not the same as moments about the mean, though they can be related to the moments. There are two common important properties of cumulants mentioned in the literature: Cumulants suppress additive Gaussian noise of unknown

covariance, and the cumulant generating function of the sum of independent processes is the sum of the cumulants instead of the product. These properties and more can be found in [45] and [46].

The *kth order cumulant* in general can be calculated as described in Equation 2, the ratio of the expected value of the variable x to the *k*th power of the standard deviation for integers of $k>2$. For $k = 1$ the cumulant is simply the mean of the signal, and for $k = 2$ the cumulant is the variance.

$$kth\ order\ cumulant = \frac{\mu_{x,k}}{(\mu_{x,2})^{\frac{k}{2}}} \quad (2)$$

Where $\mu_{x,k}$ is the mean of the mean removed signal, *x*, raised to the *kth* power, for $k > 1$, and $\mu_{x,2}$ is the second order cumulant. A summary of higher order cumulant behavior of the third and fourth order cumulants of common distributions is shown in Table 4. These cumulants are termed Skewness and Kurtosis that describe the effect they are measuring.

Table 4: 3rd and 4th Cumulants of Common Distributions

Statistical Distribution	**Skewness**	**Excess Kurtosis**
Exponential	2	6
Gaussian	0	0
Laplacian	0	3
Rayleigh	$(\pi - 3)\sqrt{\frac{\pi}{2(2 - \pi/2)^3}}$	$\frac{6\pi(4-\pi) - 16}{(\pi-4)^2}$
Uniform	0	-6/5

Skewness is the measure of asymmetry of the distribution of the signal being measured. A negative value indicates negative Skewness, where the left tail of the distribution is longer than

the right. Positive Skewness is the opposite effect. If Skewness is zero, the distribution is symmetric. Figure 15a shows a comparison of these states.

Kurtosis measures how peaked the distribution is around the mean. Excess Kurtosis is the Kurtosis minus three because the Kurtosis of a normal Gaussian distribution is three. Figure 15b shows a comparison of excess Kurtosis (K) measurements, where $K < 0$ is platykurtotic, $K = 0$ is mesokurtotic, and $K > 0$ is leptokurtotic.

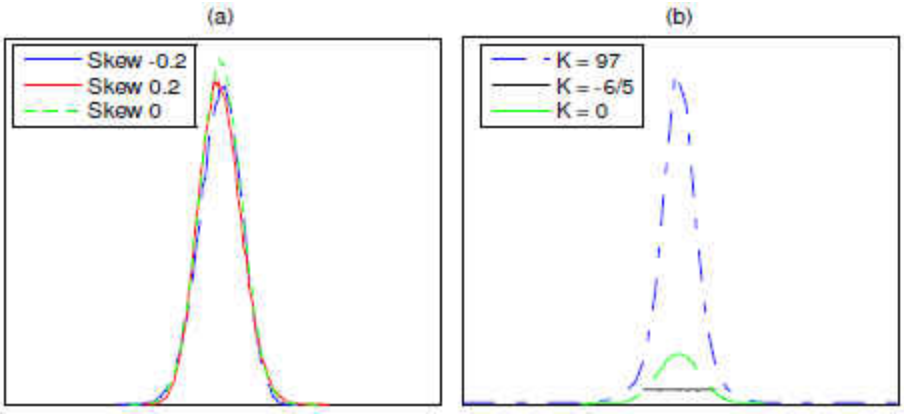

Figure 15: (a) Skewness and (b) Kurtosis Illustrations © 2012 IEEE

Higher order cumulants are simply called by their order: 5th, 6th, 7th etc. As the order of the cumulant increases it becomes more sensitive to subtle changes. This can be useful when the measureable component sought is small; however this is a detriment when there is undesirable non-additive or non-Gaussian noise. Also, the higher order cumulants are very sensitive to finite word length effects in their computation.

Cumulants of Error Sources

In many areas of signal processing, observations can be modeled as a superposition of an unknown number of signals corrupted by additive noise. This makes the use of cumulants, which

are resistant to noise, useful. An important problem in TI-ADC applications is to detect the number and type of error sources present. Here it is proposed that the errors can be classified using their statistical characteristics. This section describes these errors, and the shape of their distributions, showing the limitation of using only second order statistics.

To fully characterize the errors of single converters and TI-ADCs a combination of 128 data sets were captured and processed using Equation 2 from $k = 1$ to 8. Two input types to the system were tested: Gaussian Noise and a 75MHz sinusoid. The inputs were characterized and each of the errors tested in isolation and in every combination taken 2, 3, 4 and 5 at a time, this is 32 combinations per input, per configuration (ADC or TI-ADC).

The error cumulant calculations use the quantization only model of conversion as the reference signal to calculate the error. This allows for characterization of the error distribution without the effects of the ideal quantization component. This is not practical in an actual implementation using the cumulant calculation, but there are approaches available when interleaving to estimate the desired signal, *d(n)*, from a reference channel to calculate the error. Such as using the first channel as a reference and a resampling filter is used to generate a reference for each of the non-reference channels. The difference of the actual channel output and the calculated reference are subtracted generating an error. The design of the resampling filter limits the accuracy of the reference and thus of the amount the error can be minimized. This method is used later in Chapter 3.

Many methods currently found in the literature on post conversion correction for mismatched errors focus on minimizing one or a few errors in the absence of other errors. This approach

requires that the other error forms are already minimized. Using higher order statistics facilitates determining which errors are present and potentially their magnitude is possible. If it is known what errors are present then a hybrid approach to correction can be implemented or the statistics themselves can be used as error minimizers in an adaptive method. Chapter 3, section 2, presents simulation results using an exact error calculation.

Since the samples of the TI-ADCs are time interleaved, the error is also interleaved making the sampled signal cyclostationary because of the process cyclostationarity resulting from the periodic nature of the errors as explained in [47]. The cumulant theory of cyclostationary time series is treated in depth by Gardner in [48-50]. It is shown that higher order statistics (HOS) characterize the higher than second order probabilistic functions of stationary signals, higher order cyclostationary statistics (HOCS) characterizes the higher than second order probabilistic functions of cyclostationary signals, and that HOS is a subset of HOCS [48]. Therefore the cumulant characterization is still as valid in the TI-ADC case as it is for a single ADC.

Cumulant Adaptation

As mentioned in the previous section, the method used to characterize the error sources and gain insights into the use of these statistics for adaptation is not practically implemented. Instead, in Chapter 3, results are presented with the use of approximate cumulant statistics adapting the weights. These statistics are calculated using Boxcar FIR filter moving average approximations in place of averages over the entire dataset. A single channel is used as a reference and is interpolated to generate the reference samples for the second channel. The interpolation filter is discussed more in depth in a later subsection in this chapter. The signal error is calculated,

channel 2 minus the reference, in the cumulant block. The model is quite large so the first four cumulants can been seen in Figure 16.

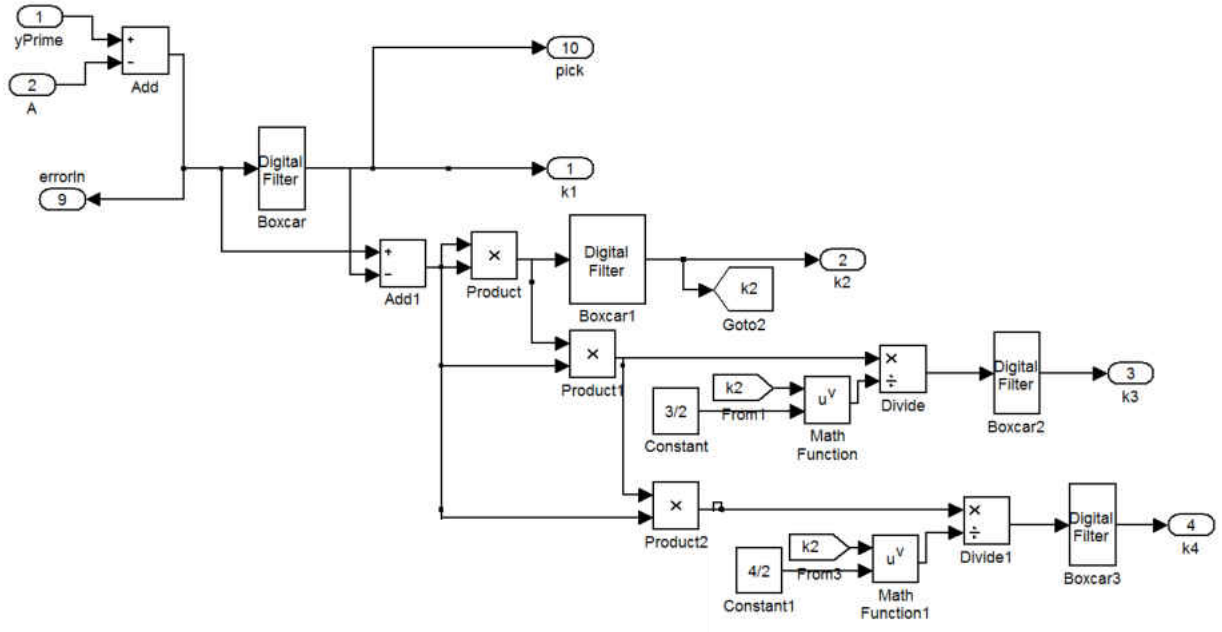

Figure 16: Boxcar cumulant approximation, Simulink™

The length of the boxcar directly relates to how accurate the cumulant calculation is, the best length can change based upon the input. Since some errors, such as gain, can dominate and bring the input into the error, a very low frequency sinusoid would need a longer filter length so as not to skew the results based on an inaccurate estimate of the mean. A very long filter increases memory requirements, though the use of a cascade integrator-comb (CIC) Boxcar FIR architecture can mitigate this tradeoff. The Boxcar filter is a moving average; the prior N samples affect the results, eliminating the ability of a dramatic change in the channel to effect the adaptation beyond the impulse response of the filter. In the results section the length of every Boxcar filter, N is set to be the same for each of the cumulants, though this is not required. It should also be noted that the goal of the LMS algorithm is to minimize the error, so if Kurtosis is

the parametric calculation whereby the desired statistic value is 3, then the input to the LMS adaptation should be the cumulant minus 3, excess Kurtosis.

Polynomial Model Implementation

A polynomial model has been used in prior works to implement a nonlinear model of the ADC channel, in particular that of [53], the paper that the contribution of this dissertation is based upon. This same model has been used in part to evaluate the effectiveness of the proposed correction structure for comparison purposes. Equation 3 represents the frequency domain polynomials implemented for the ADCs

$$Q_n(j\omega) = 1 + \sum_{p=1}^{P} \varepsilon_n^{(p)} (j\omega)^p \qquad (3)$$

Where the ε_n's are the coefficients representing mismatches, P is the order of the system and n is the channel from 0 to M-1.

Figure 17 shows the Simulink implementation of this structure, with P = 3. The digital filter blocks are first order differentiators cascaded to get second and third order differentiation terms. This model does not quantize the signal, the only limitation in the implementation is that the signal is sampled, so the sampling rate sets the Nyquist frequency and bandwidth; however the number of bits or full-scale range is not limited. The resulting implemented channels are shown in Figure 18 using a chirp to determine the response of each of the overall polynomial systems and the coefficients used are the same as the design example in [53] where $\varepsilon_{1,2,3,4}^{(1)} = 3[0.01, -0.0078,\ 0.0082, -0.002]$, $\varepsilon_{1,2,3}^{(2)} = 3[0.0075, 0.0014,\ -0.0001, -0.0075]/(\omega_0 T)$, and $\varepsilon_{1,2,3}^{(3)} = 3[0.008, -0.0045,\ 0.008, -0.015]/(\omega_0 T)^2$.

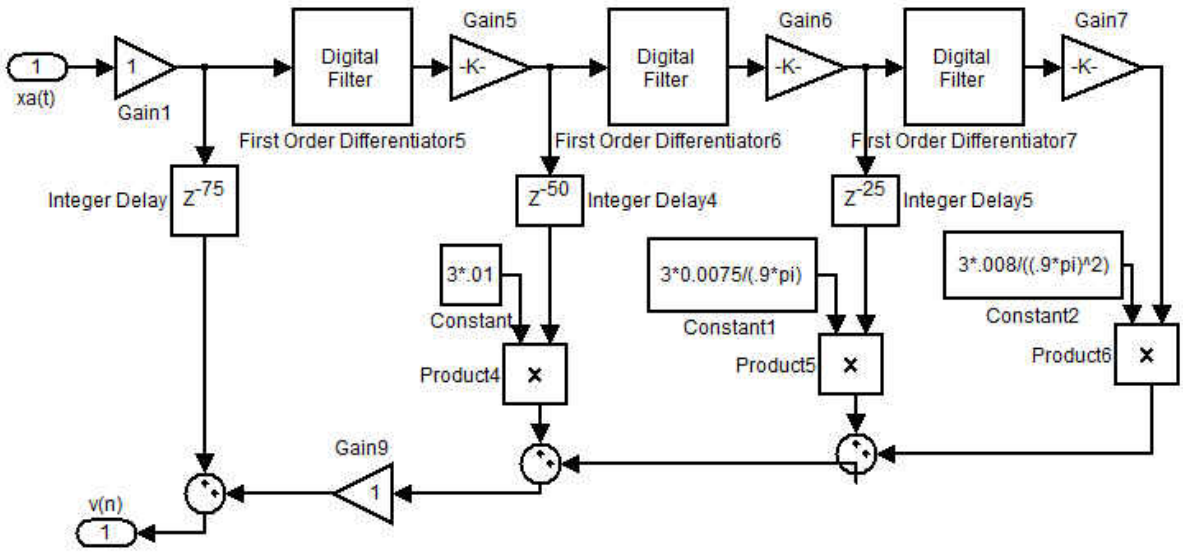

Figure 17: Polynomial model implementation, Simulink™

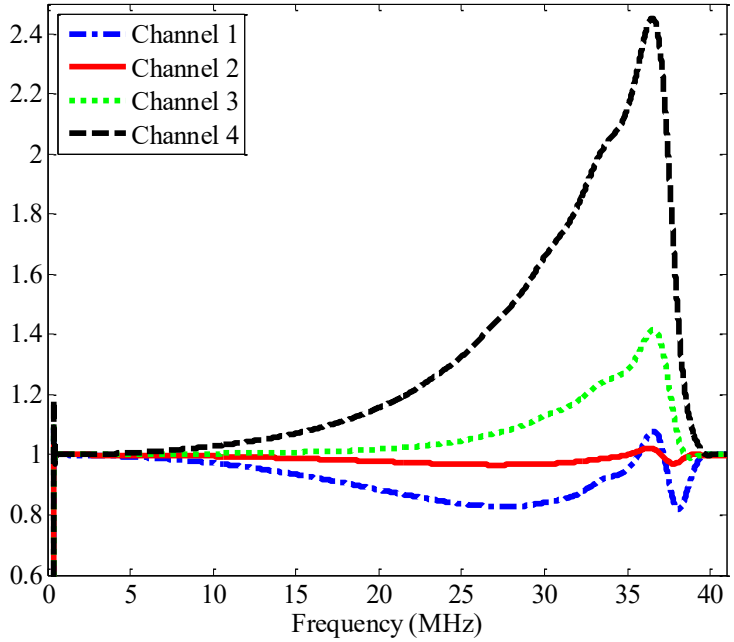

Figure 18: Polynomial Chirp Responses

Post Conversion Correction

This section discusses the related work that this dissertation is based upon, presents the original contribution and discusses the theory and implementation methods used to update the

coefficients in this work. The least mean squared (LMS) algorithm is used and considerations for the parameters that affect the level of correction achievable are discussed. They are: update rate, step size, and leakage factor. Methods for generating the error signal that is input into the LMS are also discussed. They include interpolation techniques and the use of known information about the signal

Related work

Recent work has reported on methods using an adaptive equivalent recombination structure [51] and variable digital filter (VDF) structures [52] to solve some inter-device mismatch problems. In [51] the problem of sample time skew mismatch is addressed through the use of all adjacent channels; however the method does not address nonlinear mismatches. Online compensation of offset, gain and frequency response mismatches are addressed in [52] which is also based on the work in [53]. However it requires the use of reserved sample times to correct the mismatch and Farrow filters are used in the polynomial structure instead of a nonlinear filter as is the case in this work.

The proposed method in [53] by Johansson describes a compensation structure made up of stages of derivative filters combined with coefficients that can be modified to compensate for the general channel mismatches. Each stage output feeds into the input of the next stage. This nested structure creates a non-quadratic error surface if the weights in each stage are adapted online in the background. Higher order error surfaces can have local minima, and as such the solution can depend on the starting point of the weights. The frequency domain channel transfer function of each of the mismatched ADCs is described by $Q_n(j\omega)$ in Equation 3 and was described in a prior

section. The nested compensation structure is reproduced here as Figure 19 that appears as Fig. 2 in [53].

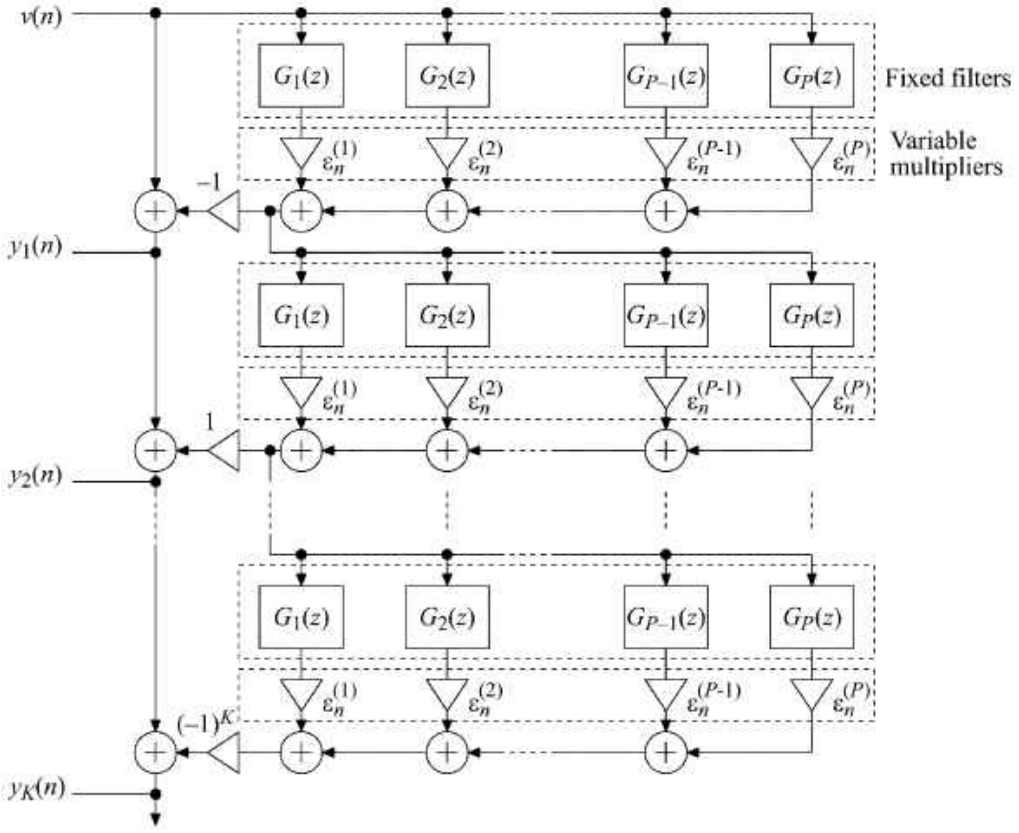

Figure 19: Nested Compensation Structure, © 2009 IEEE

The mathematical expression for the final output is nested as can be seen in Equation 4

$$y_K(n) = y_{K-1}(n) + (-1)^K \sum_{p=1}^{P} \varepsilon_n^{(p)} \sum_{i=0}^{N} g_{p,i} v_{K-1}(n-i) \qquad (4)$$

where v_{k-1} is the unlabeled input to each stage k of $G_p(z)$ from Figure 19 to simplify the expression below and $g_{p,i}$ is the coefficients of $G_p(z)$, N is the length of $G_p(z)$, K is the final stage of the correction structure and P is the number of fixed filters and coefficients in each stage.

The nested structure requires K*P fixed filters and variable multipliers for compensation, increasing the computational complexity as the desired level of correction increases. This method is extended by this dissertation in the following section. A general form has been derived for a single stage compensation equivalent to Fig. 2 in [53], based on the number of stages *K* and the order of compensation *P* shown in Figure 20. This allows adaptive updating using a quadratic error surface, guaranteeing that there is a set of coefficients that minimize the error.

Original Contribution

The general form of Equation 4 is summarized in Equations 5 – 8 and the full derivation is given later in this section, this section has been submitted to [62].

$$w_0(n) = \sum_{m=1}^{P} \varepsilon_n^m v^{(m)}(n) \quad (5)$$

$$y_1(n) = v(n) - w_0(n) \quad (6)$$

$$w_k(n) = \sum_{m=1}^{P} \varepsilon_n^m w_{k-1}^{(m)}(n) \quad (7)$$

$$y_k(n) = y_{k-1}(n) + (-1)^k w_{k-1}(n) \quad (8)$$

In Equations 5 – 8 $w_k(n)$ is an intermediate signal, the ε's are constants, $v(n)$ is the input signal, $v^{(m)}(n)$ is the mth derivative of the input, and $y_k(n)$ is the output after k stages of compensation. If the desired compensation structure for example is a *K*=4 stage with an order *P*=3 then the final structure is described when $y_4(n)$ is reached. As K or P is increased the computational load increases though the performance may also increase. If a polynomial of order P=5 will accurately correct for the channel mismatch the computation increase may not be worth

the tradeoff. Also very large K or P runs into the risk of precision error in implementation as the some of the coefficients may be very close to or equal to zero.

The computation is described algorithmically as follows.

Step 1, find $w_0(n)$ using Equation 5,

Step 2 find $y_1(n)$ using Equation 6,

Step 3 find $w_2(n)$, then $y_2(n)$, using Equations 7 and 8 repeat step 3 until $y_4(n)$ is found. The result is a 12th order structure that can be reduced to 12 adaptive coefficients and 12 fixed filters. Figure 20 shows a signal flow diagram describing the algorithmic process where $v(n)$ is the input to the compensation structure, b_m are the adaptive coefficients, G is a fixed derivative filer and $y(n)$ is the compensated output.

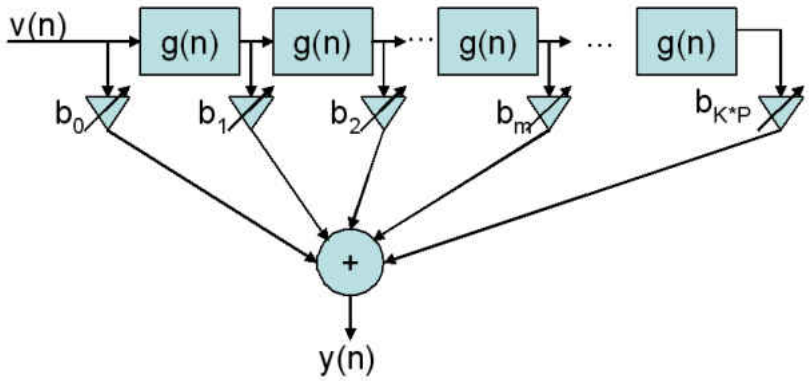

Figure 20: Adaptive compensation structure, fixed, filters, adaptive weights

To derive the general iterative form described in Equations 5 – 8 the starting point is extractable from Figure 19 by writing out explicitly what $y_1(n)$ through $y_k(n)$ is equivalent to. Equation 9 shows that $y_1(n)$ is the input $v(n)$ minus the epsilons multiplied by increasing orders of derivatives of the input, where the order of the derivative is notated using a superscript in

parenthesis. This can be written in a summation as in Equation 10. Let us call this first intermediate signal w_0 as in Equation 11. This is the signal that gets passed through the nested structure thus the further intermediate signals $w_k(n)$ are based on w_0 as seen in Equation 12. Substituting Equation 11 into 10 gives us Equation 13.

$$y_1(n) = v(n) - \left(\varepsilon_n^1 v^{(1)}(n) + \varepsilon_n^2 v^{(2)}(n) + \cdots + \varepsilon_n^P v^{(P)}(n)\right) \quad (9)$$

$$y_1(n) = v(n) - \sum_{m=1}^{P} \varepsilon_n^m v^{(m)}(n) \quad (10)$$

$$w_0(n) = \sum_{m=1}^{P} \varepsilon_n^m v^{(m)}(n) \quad (11)$$

$$w_k(n) = \sum_{m=1}^{P} \varepsilon_n^m w_{k-1}^{(m)}(n) \quad (12)$$

$$y_1(n) = v(n) - w_0(n) \quad (13)$$

Looking back at Figure 19 we see that $y_2(n)$ is based on the input and $y_1(n)$ expanded. Reorganizing we get Equation 14 which can then have Equation 11 easily substituted to get Equation 15 after simplifying into a summation. Equation 12 is then substituted to get Equation 17.

$$y_2(n) = v(n) - \left(\varepsilon_n^1 v^{(1)}(n) + \varepsilon_n^2 v^{(2)}(n) + \cdots + \varepsilon_n^P v^{(P)}(n)\right) + \varepsilon_n^1 \left(\varepsilon_n^1 v^{(2)}(n) + \varepsilon_n^2 v^{(3)}(n) + \cdots + \varepsilon_n^P v^{(P+1)}(n)\right) + \varepsilon_n^2 \left(\varepsilon_n^1 v^{(3)}(n) + \varepsilon_n^2 v^{(4)}(n) + \cdots + \varepsilon_n^P v^{(P+2)}(n)\right) + \varepsilon_n^3 \left(\varepsilon_n^1 v^{(4)}(n) + \varepsilon_n^2 v^{(5)}(n) + \cdots + \varepsilon_n^P v^{(P+3)}(n)\right) + \cdots + \varepsilon_n^{P-1} \left(\varepsilon_n^1 v^{(P)}(n) + \varepsilon_n^2 v^{(P+1)}(n) + \cdots + \varepsilon_n^P v^{(2P-1)}(n)\right) + \varepsilon_n^P \left(\varepsilon_n^1 v^{(P+1)}(n) + \varepsilon_n^2 v^{(P+2)}(n) + \cdots + \varepsilon_n^P v^{(2P)}(n)\right) \quad (14)$$

$$y_2(n) = y_1(n) + \varepsilon_n^1 w_0^{(1)}(n) + \varepsilon_n^2 w_0^{(2)}(n) + \varepsilon_n^3 w_0^{(3)}(n) + \cdots + \varepsilon_n^{P-1} w_0^{(P-1)}(n) + \varepsilon_n^P w_0^{(P)}(n) \quad (15)$$

$$y_2(n) = y_1(n) + \sum_{m=1}^{P} \varepsilon_n^m w_0^{(m)}(n) \quad (16)$$

$$y_2(n) = y_1(n) + w_1(n) \quad (17)$$

Taking a closer look at this pattern it is easy to generalize and arrive at Equation 18.

$$y_K(n) = y_{K-1}(n) + (-1)^K w_{K-1}(n) \quad (18)$$

This correction scheme is implemented as shown in Figure 21. In the figure xa(n) is the output of an single converter. The digital filters along the top of the Simulink™ model are approximate derivative filters followed by gain compensation. Each derivative output is then multiplied by an adaptive coefficient collectively shown as e1, e2 through ePK and added together to form v(n), the corrected output. The adaptation is achieved using the least mean squared (LMS) algorithm and the s1, s2 through sPK signals are fed into the adaptation block as the gradient. The figure shows broken traces with an ellipsis (…) such that it can be seen that any number of stages can be added to achieve a required order for Equation 18.

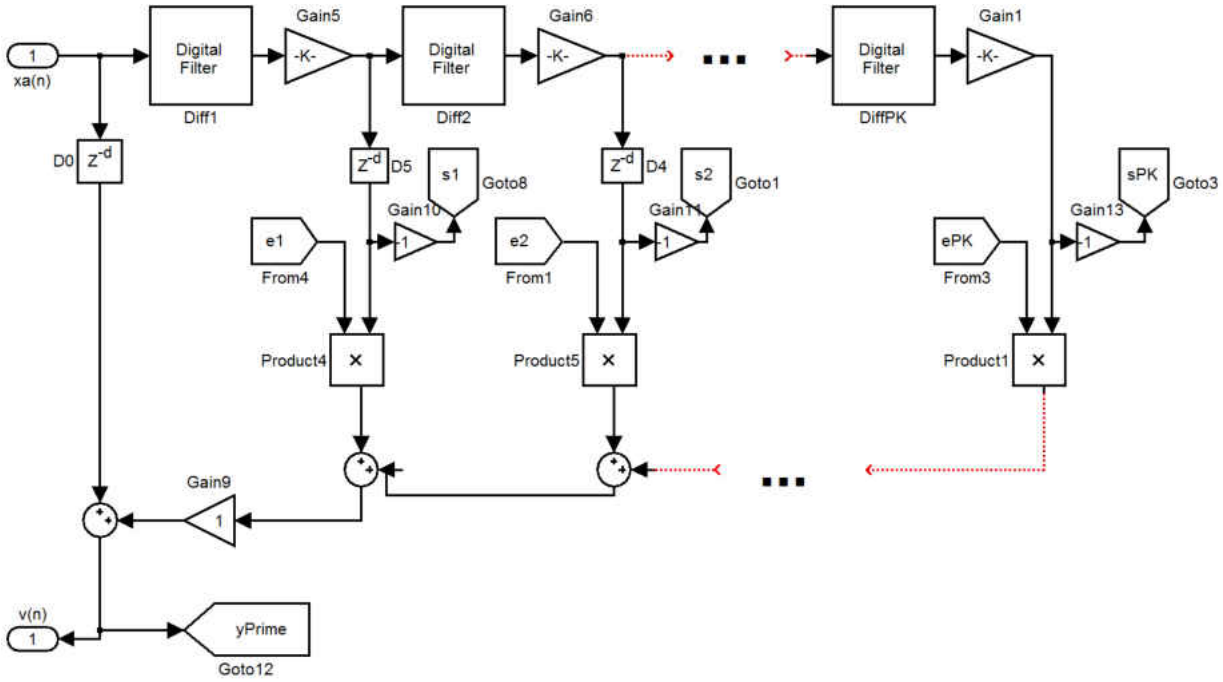

Figure 21: Compensation Implementation, Simulink™

Adaptive Theory

The LMS algorithm, invented in 1960 by Dr. Bernard Widrow, is well known and is used to update the weights of the adaptive filter structure at the current time using a stochastic gradient descent method. The algorithm estimates the coefficients, w(n) in Equation 21, needed to minimize the error, e(n) in Equation 20, between the output signal, y(n) in Equation 19, and the desired signal, d(n). The weight update function, in Equation 22, uses an adaptation step size μ multiplied by the error and the complex conjugant of the vector buffered input.

$$y(n) = \boldsymbol{w}^T(n-1)\boldsymbol{u}(n) \qquad (19)$$

$$e(n) = d(n) - y(n) \qquad (20)$$

$$w(n) = w(n-1) + f(\boldsymbol{u}(n), e(n), \mu) \quad (21)$$

$$f(\boldsymbol{u}(n), e(n), \mu) = \mu e(n) u^*(n) \quad (22)$$

The LMS algorithm allows finding the minimum of a quadratic error surface in some convergence time, the step size and the magnitude of the error determine how quickly the algorithm converges, and how closely to the minimum the algorithm can reach, as a step size that is too large may cause the weights to oscillate around the minimum and a step size that is too small will take a very long time to converge.

The LMS algorithm has since been extended to methods such as Normalized LMS (NLMS), Sign Error LMS, Sign Data LMS, Sign Sign LMS, Block LMS (BLMS), Optimum Block Adaptive LMS (OBALMS) and more. Each variant has advantages and disadvantages such as convergence rate, memory requirements, etc. See Chapter 15 in [60] for a more complete analysis of various adaptive methods, LMS is not a required method of adaptation of the weights.

Since the step size can limit the performance and affect the convergence rate of the minimization a variable step size is used based on the rate of change of the weights in the implementation to form a compromise between convergence rate, convergence minimum and complexity. When the rate of change of the weights gets below a certain level the step size is first increased until an incremental increase does not increase the rate of change over a limit or the weights begin to oscillate. If oscillation occurs the step size in decreased by an increment and the process starts over if the error increases over a threshold. Figure Figure 22 shows the difference between stopping adaptation when the weights are oscillating and decreasing the step size to allow continuing the adaptation closer to the minimum.

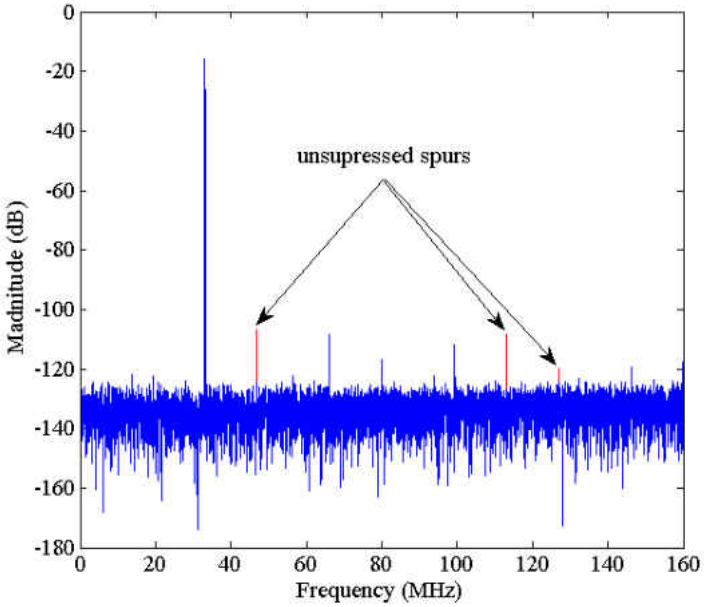

Figure 22: 4 TI-ADC Corrected Spectrum, Two Step Sizes, Indicated Spurs from Larger Step Size

Interpolation Implementation

The use of interpolation techniques allows the use of a single channel as a reference to generate an error source to feed the weight update algorithms. Subsampling of the input folds all of the energy into the first Nyquist region for each channel. When all channels are ideally matched the aliasing terms cancel when recombined because of opposing phasing information. Knowledge gained from the mismatched combined signal can inform the need for shifting and flipping the interpolated spectrum of the reference channel to the correct region for adaptation. The nonlinearities are proportional as frequency increases and therefore adjusting for the higher frequencies to remain intact in the reference for correction is ideal. See Figure 23 for an example of a 4 TI-ADC situation where the desired energy is overlapping two Nyquist regions, all energy in all bands folds back into the first Nyquist region. Though there is overlapping, shifting the

reference channel up to the third Nyquist region allows for the most correction in this example as the highest frequencies present for adaptation are located here.

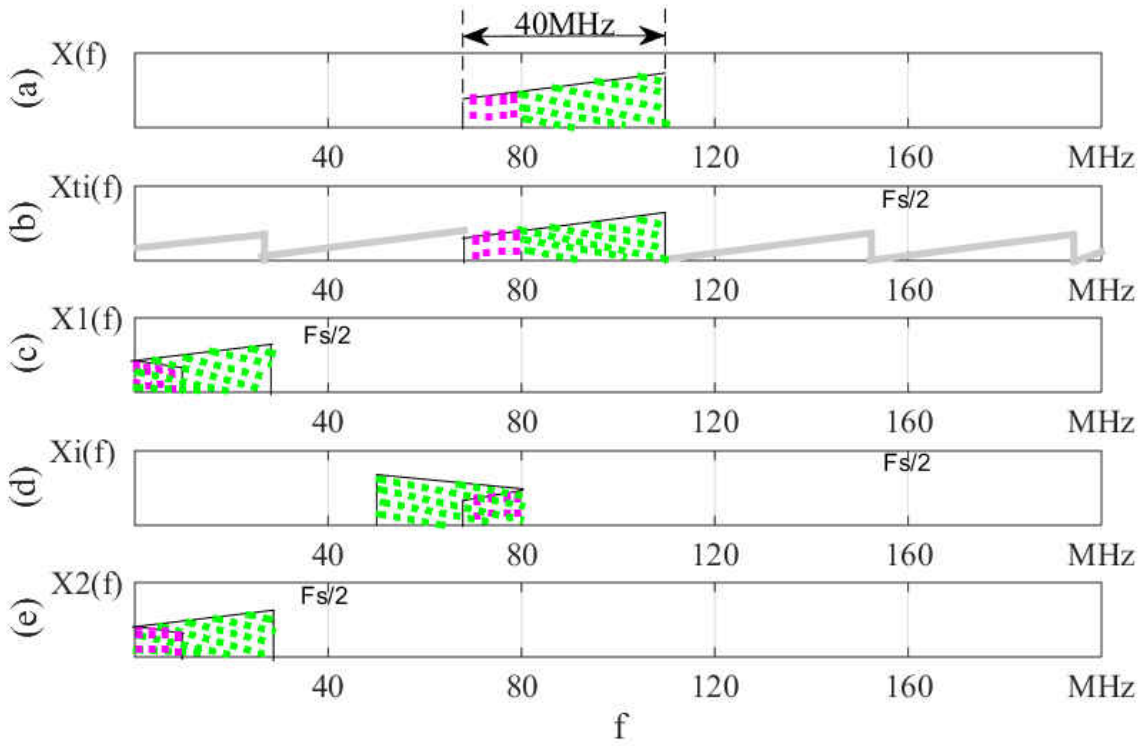

Figure 23: Subsampling and recovery, consolidation of energy into a single Nyquist Region (a) analog signal spectrum (b) mismatched 4 TI-ADC spectrum (c) channel 1 ADC spectrum (d) interpolated shifted spectrum (e) channel 2 ADC spectrum

It is also useful to use an interpolation filter in the instances where the spectrum is fully contained within a single Nyquist region, see Figure 24, bandpass sampling is a very common use of oversampling ADCs. The analog spectrum (a) is sampled with mismatched 4 TI-ADCs in (b), the energy folds to the first Nyquist for each of the channels (c) (e), but an interpolated reference (d) of channel 1 can be used to accurately generate the phase shifted reference for the other channels. An efficient and symmetrical method is a half band filter designed using the Parks-McClellan optimal FIR filter design, post design identically setting every other coefficient to zero and the center coefficient to 0.5. Define the start of the pass band roll off as α*Fs and the

stop band as (1- α)*Fs, $\alpha \in (0,0.5)$, and the length of the filter to yield an equal pass band ripple and stop band rejection. In the case of 4 times the sampling rate, two half band filters can be used, or a quarter band, or another method depending on the transition band requirements.

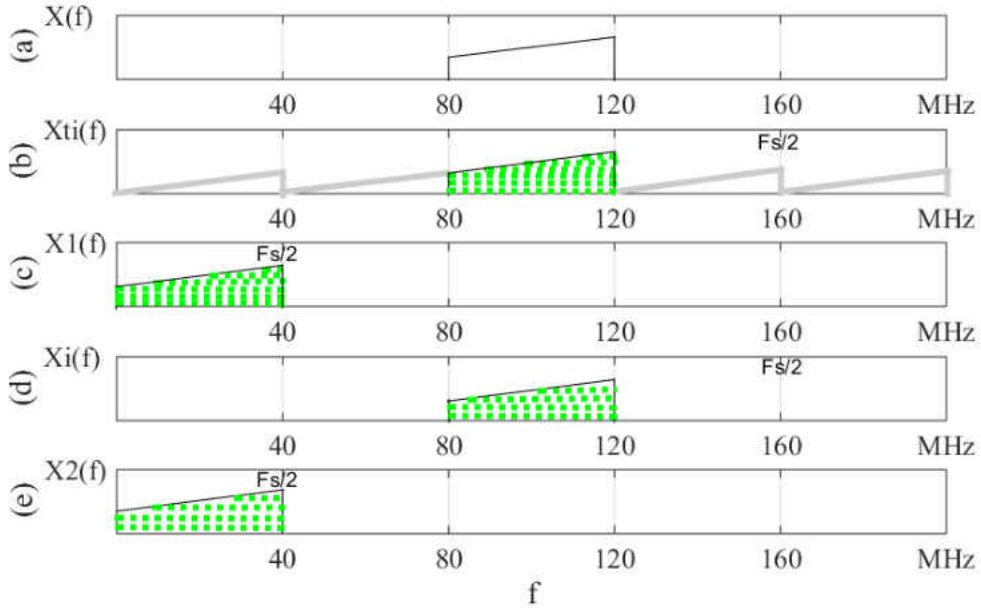

Figure 24: Subsampling and recovery (a) analog signal spectrum (b) mismatched 4 TI-ADC spectrum (c) channel 1 ADC spectrum (d) interpolated shifted spectrum (e) channel 2 ADC Spectrum

The fidelity of the filter needs to be at least equal to the desired SFDR or SNR, whichever is the limiting parameter. For lower ENOB or narrower pass band regions, the half band interpolator works well. Once a very sharp transition is needed however it can be more efficient to switch to a different architecture, one oriented on sharp transitions.

CHAPTER 3: RESULTS

This chapter first details the characteristics of the ADC behavioral model as compared to the data sheet specifications it is based upon [18]. The cumulant statistics calculated with individual and combinations of errors enabled in the behavioral model are then presented. On this basis we then move on to the results of the proposed post conversion correction first applied to the polynomial model for comparison purposes and then to the behavioral model. Each of these sections use one of three methods to update the adaptive coefficients, the ideally matched error to show that the correction structure should be able to correct the mismatches, then the interpolated reference channel and cumulant statics to show two possible implementation methods.

Behavioral Model Characteristics

The SFDR in the first Nyquist region of the behavioral model was shown in Figure 6 and is repeated here for convenience as Figure 25. Comparing the solid line of the single ADC's SFDR to the dotted line of the 4 TI-ADC system's SFDR with every error mismatched it can be seen that the range is dramatically reduced when mismatches are left uncorrected, even operating in expected ranges. The largest mismatch spur in this case is due to the offset mismatch, correcting this mismatch results in a SFDR of around 45dBc across the 4 TI-ADC Nyquist range 160MHz.

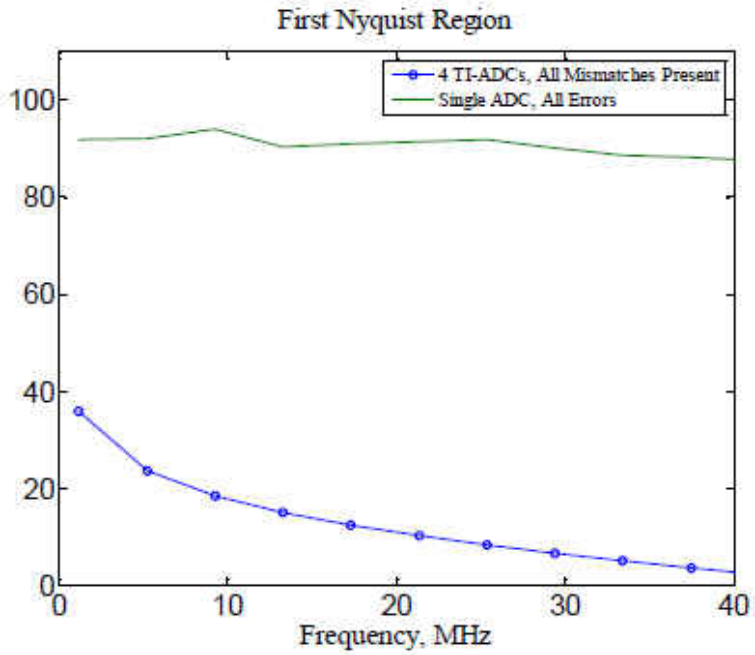

Figure 25: TI-ADC SFDR vs. Frequency © 2011 IEEE

To show the spectral content of the mismatched system in its best and worst cases in this implementation a low and high frequency example is given. The best performance is expected at a low frequency since jitter mismatch and nonlinearity effects are at a minimum. Figure 26 shows the spectrum of a low frequency tone at 1.226MHz for the single ADC, offset error is seen at DC. Compare this to Figure 27 with the same input frequency to the 4 TI-ADC system with mismatches at $\pm f_i + k * Fs/M$, $k * Fs/M$ and nonlinear distortions in the uncorrected spectrum. Even at this low frequency the SFDR was reduced to less than 40dB.

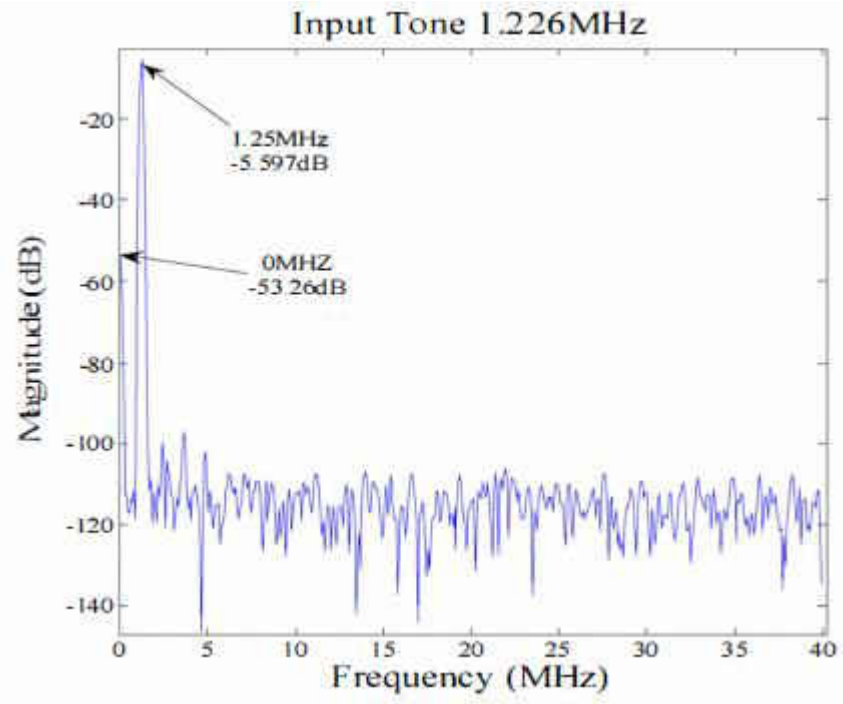

Figure 26: Single ADC with All Errors Enabled

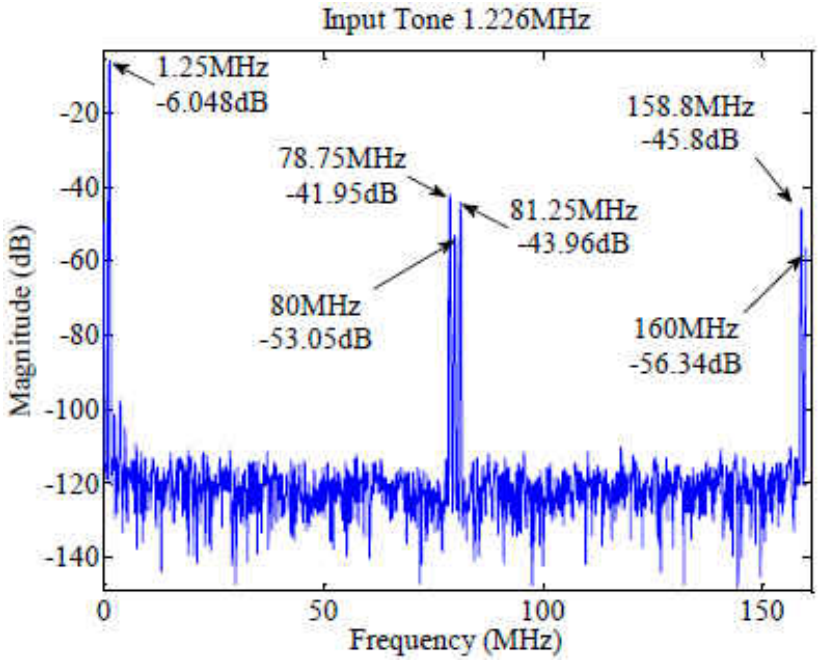

Figure 27: TI-ADC Spectrum with Mismatch Errors Identified © 2011 IEEE

Figure 28 and Figure 29 shows a high frequency example with an input tone at a frequency in the 5th Nyquist region of the single ADC and the 2nd Nyquist of the TI-ADC. In this example the SFDR is reduced to less than -12 dB. This is a situation where the system should be able to operate if the mismatches are corrected as the ADC is specified as performing well up to 400MHz with 70dB SFDR in the SFDR figure on page 8 of [18]. Since the behavioral model actually operates at a much higher sampling rate when implementing jitter (approximately 92 GHz), INL and gain errors (720 MHz) before decimating and adding the offset and DNL after the decimation it should also perform well when interleaved and mismatches are corrected up to 360MHz. This can be seen in Figure 30 where the SFDR is plotted up to 360MHz with all errors matched in a 4 TI-ADC system.

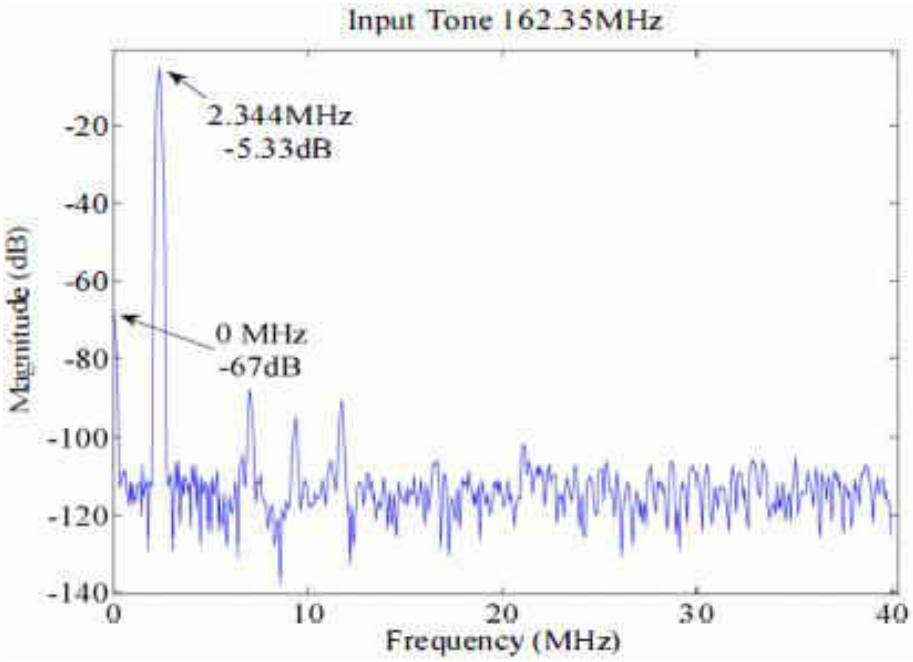

Figure 28: Single ADC, Fifth Nyquist Tone with All Errors

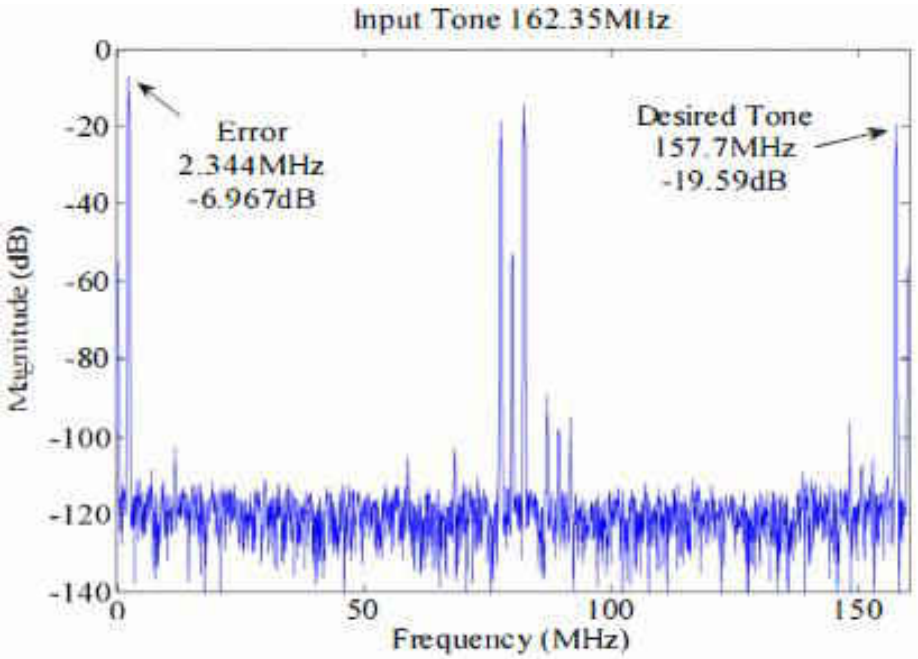

Figure 29: Second Nyquist Tone, 4 TI-ADC with Uncorrected Mismatch Errors

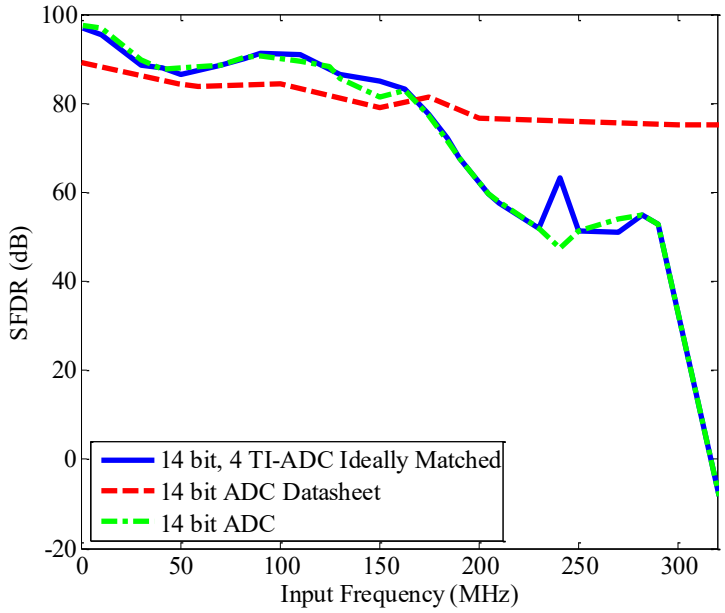

Figure 30: SFDR of ideally matched 4 TI-ADC system

A practical example is also shown in Figure 31 with a QPSK input through a 2 TI-ADC behavioral model system, with all but the offset mismatches turned on. The mismatch spectrum

(red) is overlapped with the ideally matched spectrum (blue). An image of the input can be seen approximately 63dB down. A similar example will be used later in this chapter to show the performance of the post conversion correction on a QPSK input.

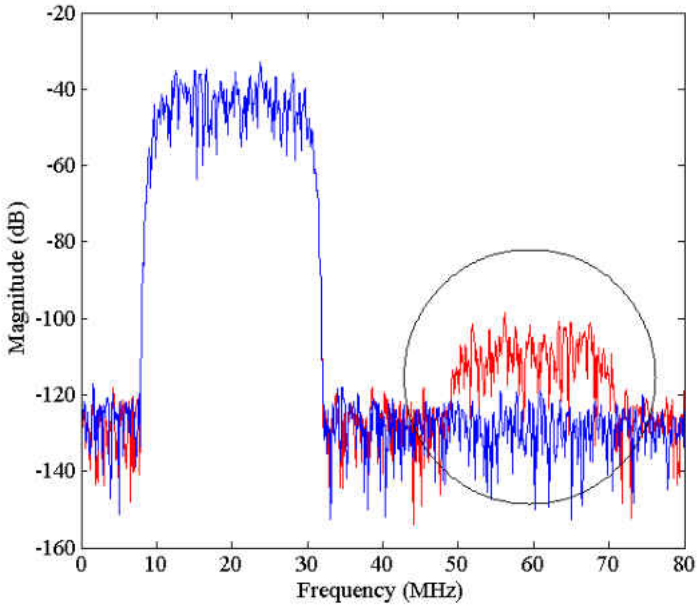

Figure 31: 2 TI-ADC Mismatched Spectrum, QPSK Input 20MHz Symbol Rate

Cumulant Statistic Simulations

The cumulants of the 14 bit ideally quantized input signals are shown in Figure 32. It can be seen that, for the sinusoidal input, only the even order statistics are present due to the symmetry of the input and the quantization error. There is some small variation in the calculation between the single ADCs as they start at slightly different sample times but this is an artifact of length of the observation window and a longer data set would thus reduce this phenomenon see Table 5 (all cumulants have a variance as a function of length.). The statistics of the Gaussian noise input

have a higher variation, however as expected from Table 4 the Skewness and Kurtosis approach 0 and 3 respectively.

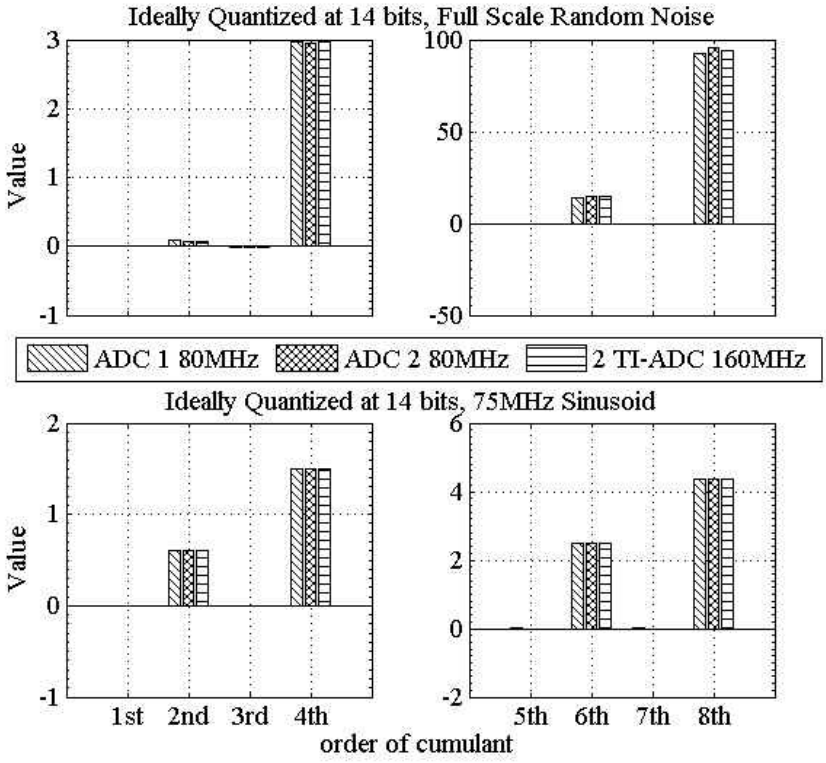

Figure 32: Input Cumulants

Table 5: Input Cumulant Estimation Lengths

Cumulant	N per ADC	14 bit 75MHz Sine			14 bit, Full Scale Noise		
		ADC 1	ADC 2	2 TI-ADC	ADC1	ADC 2	2 TI-ADC
1st	14.5e3	-1.5276e-4	1.9442e-4	0.2083e-4	0.0020	-0.0013	0.0003
	75000	-0.7373e-4	0.7517e-4	0.0072e-4	-0.0007	-0.0015	-0.0011
	75e4	0	0	0	-1e-4	4.168e-5	-2.9618e-5
2nd	14.5e3	0.6050	0.6050	0.6050	0.0630	0.0615	0.0623
	75e3	0.6050	0.6050	0.6050	0.0595	0.0594	0.0594
	75e4	0.6050	0.6050	0.6050	0.0443	0.0442	0.0443
3rd	14500	9.4469e-4	-12e-4	-1.1202e-4	-0.0048	0.0303	0.0129
	75e3	4.4070e-4	-4.5190e-4	-0.056e-4	-0.0103	0.0074	-0.0014
	75e4	0	0	0	0.0039	-0.0012	0.0014
4th	14.5e3	1.5	1.5001	1.5001	3.0719	3.0045	3.0396
	75e3	1.4999	1.5001	1.5	2.9946	2.9908	2.9927
	75e4	1.4999	1.5001	1.5	3.0064	2.9983	3.0024

The individual ADCs, in the 2 channel TI-ADC configuration are referred to as ADC1 and ADC2 in the figures, each collected 14,500 points sampled at a rate of Fs = 80MHz. The two ADCs are interleaved to yield 29000 samples at an aggregate rate of 2*Fs = 160MHz. The cumulants are then calculated over the entire record. Figure 33 through Figure 36 are based on these variables.

The cumulants of the isolated errors, using the behavioral model, for a single ADC and 2 TI-ADC system are shown in Figure 33. The input $x(t)$ is white Gaussian noise, used to excite all possible frequencies in the system. The error contribution is then worst case statistically in a long data set and would be similar to a wide band signal excitation of the TI-ADC. It can be seen from

the third order statistics that DNL and offset errors create the largest Skew. A closer look shows that the offset mismatch Skew became negative when the two ADCs were interleaved. As explained above, the sign and magnitude of the Skew will depend on the shape of the distribution of the errors introduced from each ADC and their magnitudes.

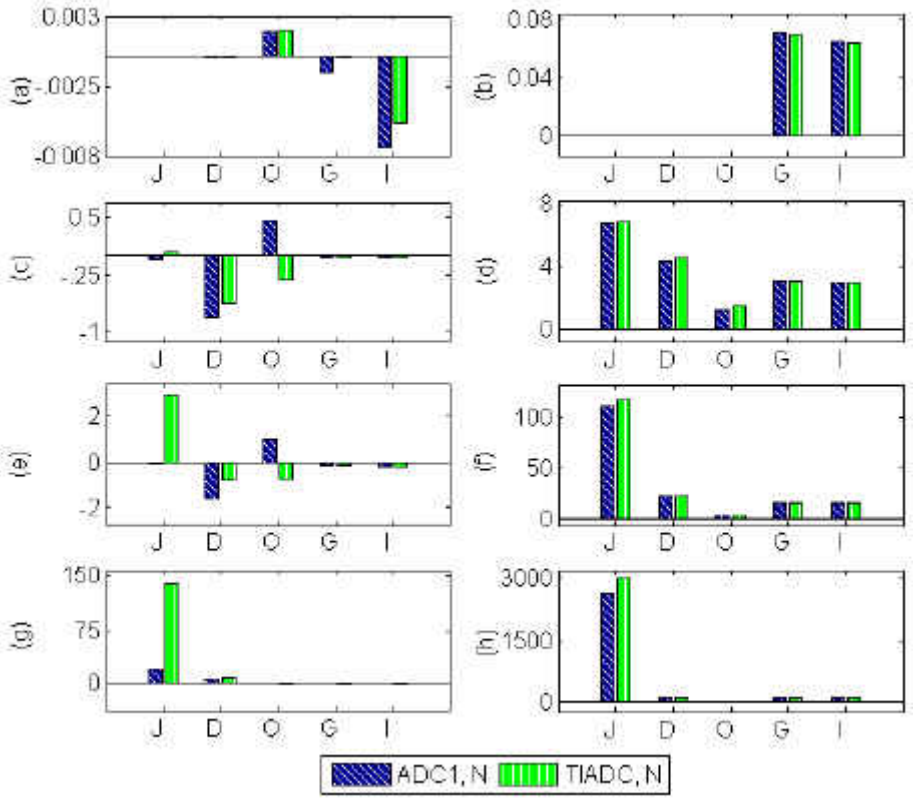

Figure 33: Single and Time Interleaved, Isolated Error Cumulants, Noise Input (N), Cumulant: (a) Mean, (b) Variance, (c) Skew, (d) Kurtosis, (e) 5th , (f) 6th , (g) 7th , (h) 8th © 2012 IEEE

In combination the errors have additive and subtractive effects as described in previous dynamic analysis of TI-ADCs [54-57]. These effects were experimentally captured via simulation in 160 different combinations of 2 types of inputs, 5 types of error, and three system configurations (two single ADCs and a 2 TI-ADC) as described in methods section of Chapter 2.

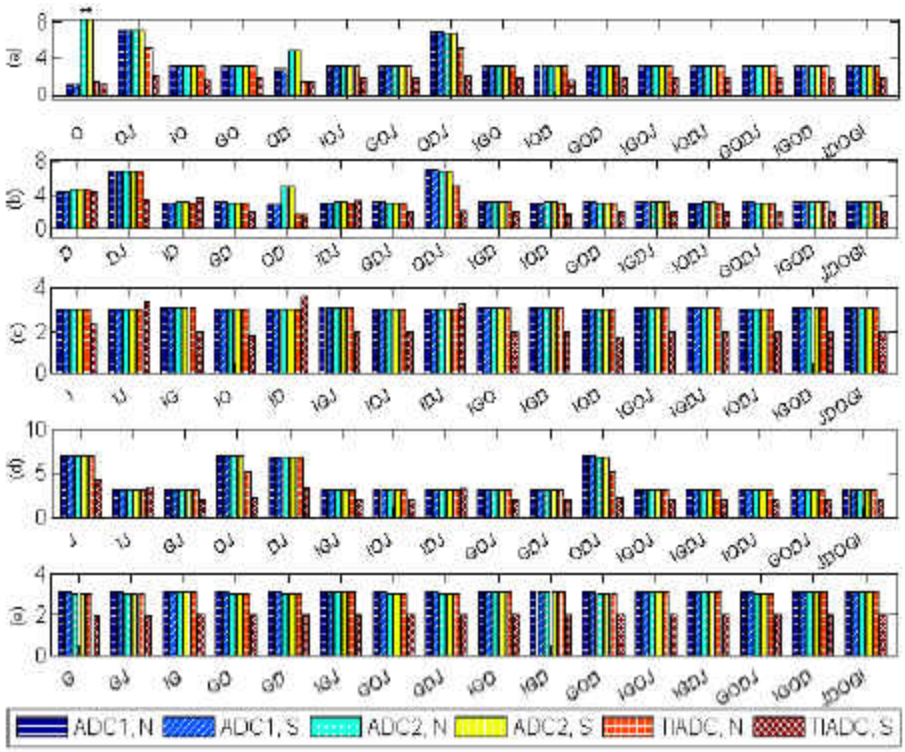

Figure 34: Fourth Order Cumulants, Error Combinations for Noise (N) and Sinusoidal (S) inputs: (a) Offset, (b) DNL, (c) INL, (d) Aperture Jitter, (e) Gain, *bar extends axis, zoomed for detail © 2012 IEEE

Figure 34 shows bar charts of different combinations of errors on each system configuration for the Kurtosis. Each sub plot shows a single error in combination with other errors indicated by the x-axis labels, for example Figure 34a on the left most side the axis label shows O, the only error and mismatch error here is offset for a noise input and a sinusoidal input into two individual ADCs and a 2 TI-ADC, the second grouping shows offset and jitter, the third INL and Offset etc, until every combination of errors with offset included is shown. The purpose of this is to analyze how the Kurtosis statistic is dominated when errors are eliminated. In this way we may be able to determine how valuable the statistic may be in the use of updating adaptive filter coefficients whose purpose it is to eliminate the mismatches.

Close observation shows that gain error in combination with any other error, Figure 34e, dominates the Kurtosis measurement. This portion of the figure has been reformatted for clarity in Figure 35. For the single ADC configuration this is true because the error is only dependent upon the input signal and when the reference is subtracted from signal the remaining error contains either a smaller amplitude sinusoid or a smaller magnitude of the noise in this example. The TI-ADC configuration will additionally have mismatches introduced and the error will be a modulated form of the input

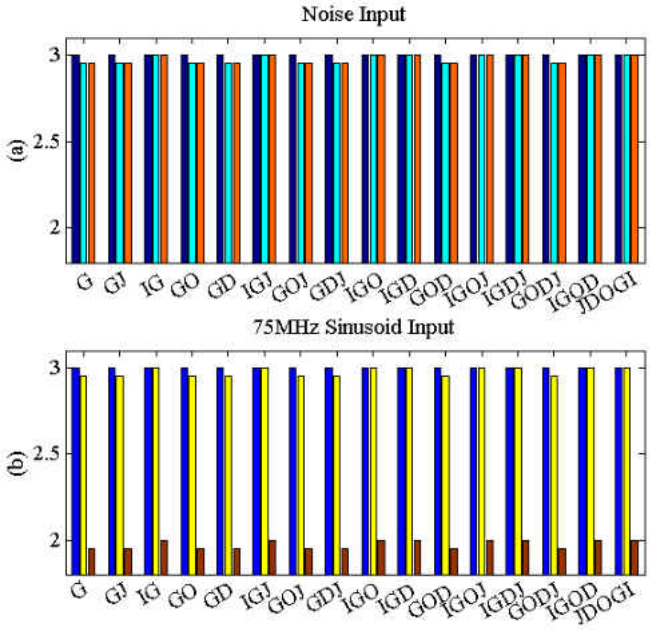

Figure 35: Kurtosis Statistic with Gain Error Combinations, a different view

It can also be seen that, in wide band input cases that the cumulant of the gain error is seemingly invariant to interleaving. As each ADC has a different response, the error is slightly different for each channel and when interleaved the resulting error is periodic. However, if the gain mismatch dominates the error, the input statistics dominates the Kurtosis statistic. When the input is Gaussian noise that spans the entire frequency range, the error signal contains mismatches across

the entire response of the ADC, and the Kurtosis cumulant shown in Figure 35(a) measures approximately 3 regardless of interleaving. In the case of the sinusoidal input, the gain error dominates in the interleaved case as a measurement of 1.5 is expected as the Kurtosis measurement of a sine.

Figure 34c, INL error combinations, indicates similar affects, partly due to the same reason. The INL is nonlinear across the frequency response of the ADCs and this in turn creates an error signal dependent upon the input though of varying magnitudes over frequency. After removing both gain and INL errors from the system it can be seen then that the Kurtosis takes on various values depending on the remaining errors present.

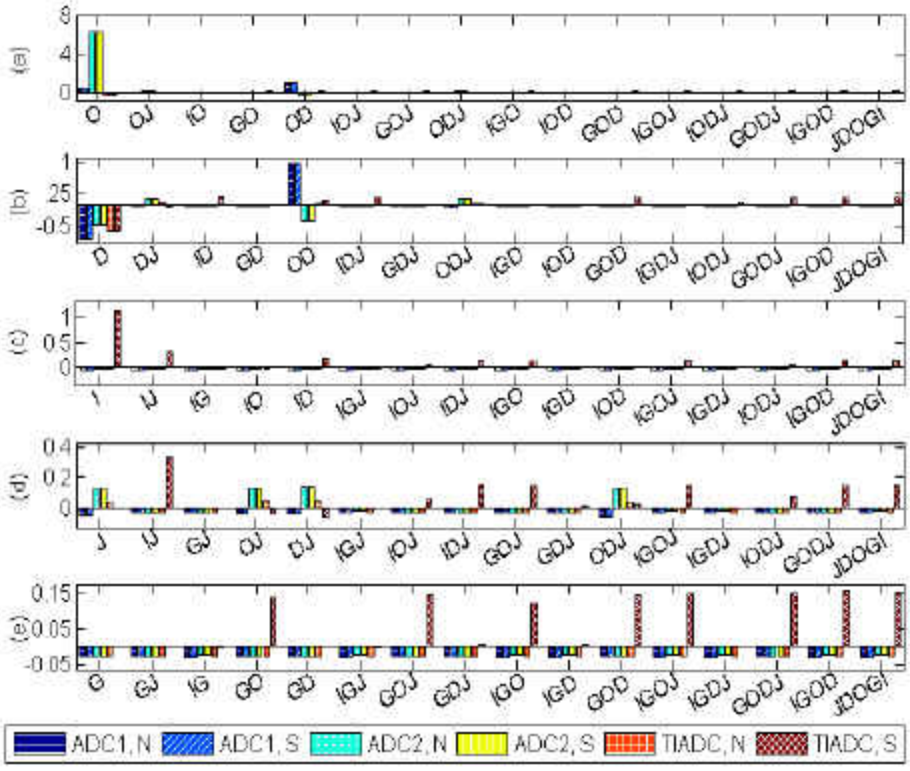

Figure 36: Third Order Cumulants, Error Combinations (a) Offset, (b) DNL, (c) INL, (d) Jitter, (e) Gain © 2012 IEEE

For Skew, or the third order cumulant is shown in Figure 36, offset dominates this statistic as seen in part (a) followed by DNL in (b). This is because the non-symmetric nature of the errors in question, any of the odd order cumulants will show a dominance of Offset and DNL but the sensitivity will increase. In implementation, the third and fifth order are less likely to introduce precision error into the calculations.

These characterizations as mentioned before are based on a data collected from the behavioral model with errors and mismatches set in the ranges of Table 3. The error signal is calculated by subtracting a reference generated by an ideal quantizer. A different method, discussed in Chapter 2 as Cumulant Adaptation is used in the post conversion correction adaptation described in the coming subsections.

Post Conversion Correction Algorithms

The level of correction achievable is limited by the error signal directing the adaptation and the order of the polynomial correction. The following subsections use a fifth order polynomial correction and either a polynomial ADC channel or a behavioral channel. The polynomial model results are used to validate the correction scheme, make a comparison to [53], and to visualize how the overall channel changes in response to narrow band correction. The behavioral model subsection presents the results with correction based on the ideally matched error, interpolated error and cumulant based correction.

Polynomial Model, Channelized Correction

The adaptive linear combination of nonlinear filters has been derived and implemented for post conversion correction of TI-ADCs using a polynomial ADC model described above. Adaptive correction is achieved through using the first of *M* channels as a reference. That is, the goal of the correction is to create a composite ADC correction algorithm transfer function that approximates the transfer function of the first (reference) ADC to a required accuracy; to match all channels to remove mismatched errors. Simulation results are presented in this section for 2 and 4 channel TI-ADCs using a frequency domain polynomial to model the channels with correction placed before interleaving.

The channelized adaptive post conversion correction is able to match the non-linear polynomial channels, on average a 40dB increase in SFDR was realized in the 2 channel case where the channels were more closely matched and a 90dB increase in SFDR was realized in the 4 channel case. The level of suppression is based upon how poorly matched the channels were in the first place; mismatch spurs can become quite large. Figure 37 shows the multi-tone spectrums before and after correction. This represents a nearly ideal suppression of the mismatch error generated spurs.

The same polynomial order that was used in [53] in Example 1 is used here giving the linearized correction structure seen in Chapter 2 Equation 18. Figure 37a shows the SFDR across the first Nyquist region of the 4 TI-ADC for four scenarios, the matched case, the ideal matched case, before correction and after correction is applied. Figure 37b shows multiple tones and their mismatch spurs before correction and Figure 37c shows the spectrum after correction in the 4 TI-

ADC channelized correction case. The frequencies of the tones were chosen such that the interleaving spurs would not overlap any of the other tones or mismatch spurs as much as possible. The overlapping of spurs at DC and multiples of the single ADC Nyquist rate is unavoidable.

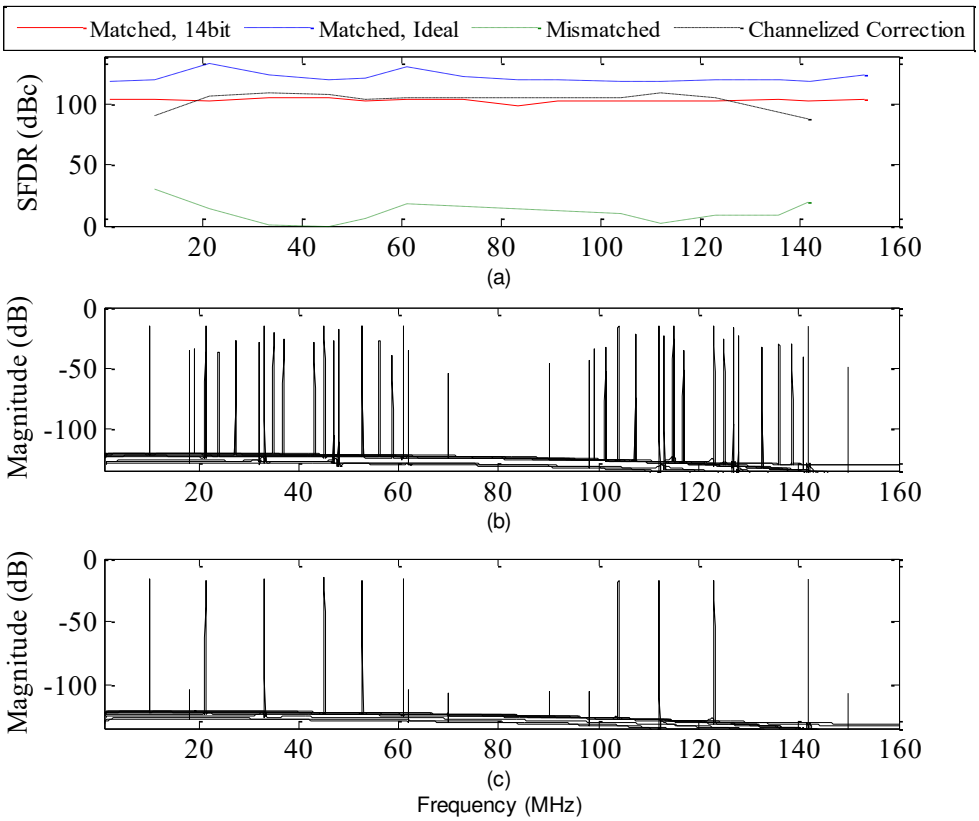

Figure 37: Polynomial Model a) SFDR for 4 TI-ADC matched, mismatched, channelized correction, and interleaved correction. b) 4 TI-ADC multitone input uncorrected c) 4 TI-ADC multitone input with channelized correction

Taking a closer look at what is happening, a single tone at 33.1 MHz is used for adaptation at a given frequency for this example. The chirp response is possible in the polynomial case, but not in the behavioral model as the rate changes do not support this type of fast overall channel characterization. So it is used here to better understand the limitations of the contribution. The first channel is used as a reference to adapt shown as the red in Figure 38, the original

mismatched channel shown in green, gets modified by the channelized correction to the new combined channel response shown in blue. The 33.1MHz point, where the red and blue lines cross, matches at that frequency and the error is seemingly minimized to the algorithm. Since the adaptation of the weights are based upon the input minus a reference, if only a single tone is used in adaptation only that frequency is being matched as the channel varies across the spectrum. The rest of the spectrum is in a don't care state, potentially making the mismatch larger in other areas to quickly adapt to the error. This indicates that an initial calibration period for adaptation across the usable frequency range would be beneficial as the error across the range would be minimized and only small corrections would be needed over time even when switching between narrow and wideband inputs.

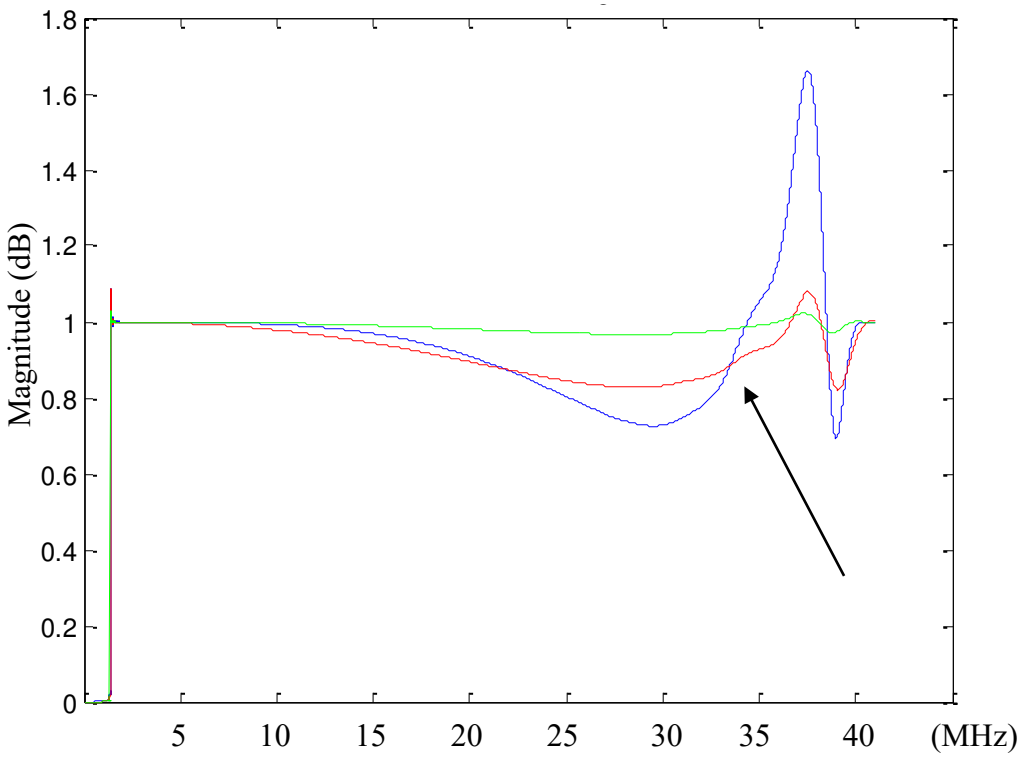

Figure 38: Chirp response 2 TI-ADC, red ADC 1, green ADC2, blue ADC1 after correction only at 33.1MHz

Behavioral Model, Channelized Correction

Some limitations for the level of correction seen here are an artifact of the error implementations of the behavioral model, seen in the ideally matched error subsection, others from the reference channel implementation, seen in both the interpolated reference error and the cumulant error subsection, and the estimate of the cumulant seen in the cumulant error subsection. These sections have been submitted for publication as [63-65]. Details on the parameters used, such as step size selection in the simulations can be found in Chapter 2. Both multi-tone and wide band QPSK inputs are used for adaptation in the behavioral model subsection.

Ideally Matched Error

Adaptive correction is achieved in a 4 TI-ADC implementation using the first of 4 channels as a reference. Figure 39 compares the SFDR of the original datasheet as the red dashed line, the reference channel ADC as the solid green line, the uncorrected 4 TI-ADC channel with gain, INL, DNL and jitter mismatches as the magenta dotted line with circles and the channelized correction as the black dot dashed line. The SFDR is improved to the reference channel performance in the first two Nyquist regions of the single ADC, averaging a 42dB improvement. The improvement tapers off in the third and fourth regions due to the roll off of the correction structure leaving a remaining spur at 80MHz though the others are reduced.

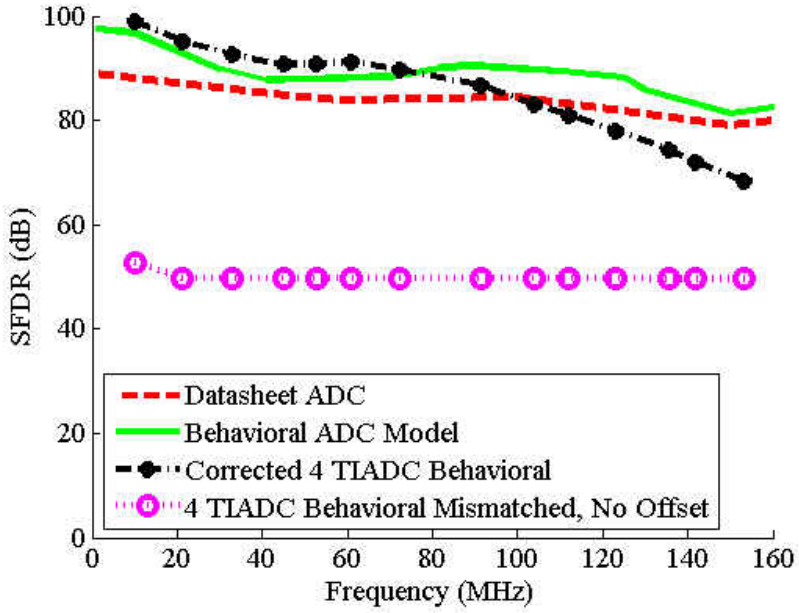

Figure 39: SFDR, Ideally Matched Error 4 TI-ADC

Figure 40b shows the multi-tone spectrum and mismatch spurs before correction and Figure 40a the spectrum after correction in the 4 TI-ADC channelized correction case. Comparing the two parts of the figure more clearly shows that there are two outstanding spurs, the first at 80MHz and the other at 6.9MHz, the mismatch spur from the 153.1MHz tone. A potential improvement would be to implement the channelized correction at a higher interpolated sampling rate to take into account the potential for subsampling applications.

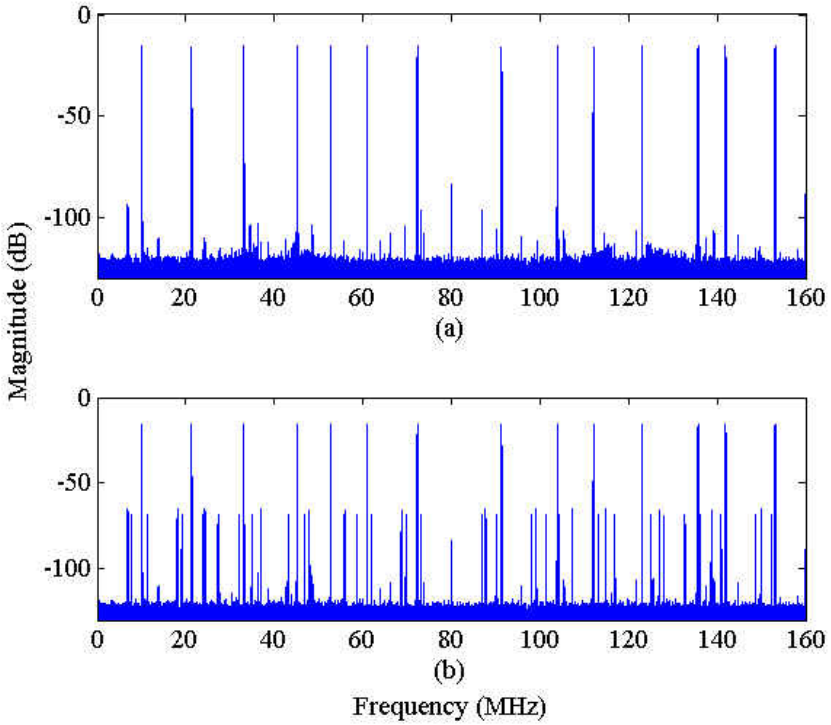

Figure 40: Behavioral Model Ideally Matched Error a) 4 TI-ADC multitone input with channelized correction b) 4 TI-ADC multitone input uncorrected

In the results shown in Figure 41, a 2 TI-ADC model is used to digitize a QPSK input with a 10MHz symbol rate centered at 20MHz. Suppression of about 16dB is achieved using the channelized correction using the ideally matched error. The uncorrected mismatched is seen as the blue line, overlapping with the corrected spectrum in red.

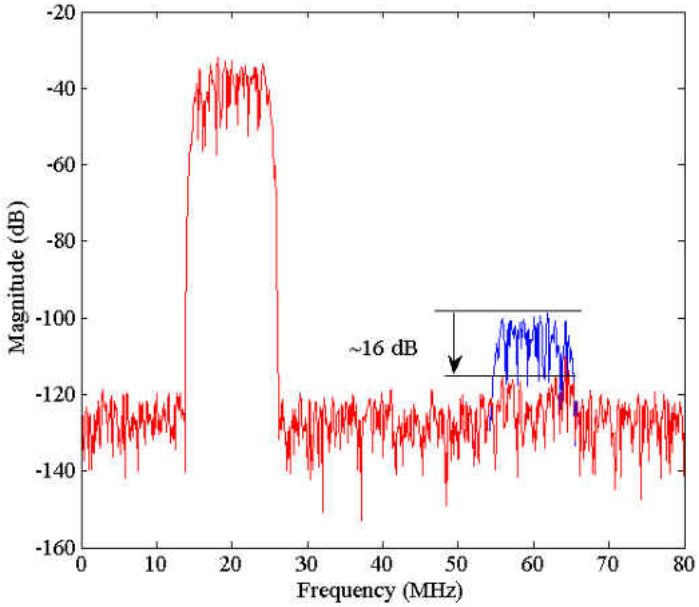

Figure 41: 2 TI-ADC Input (blue) overlapped with Corrected (red) 4 QPSK spectrum

Interpolated Reference Error

The performance in this section, the SFDR in Figure 42, is limited by the interpolation filter used to generate the reference channels. A 2 TI-ADC behavioral model is used with a half band interpolator designed using the Parks-McClellan optimal FIR filter design, post design setting every other coefficient to zero and the center coefficient to 0.5. The pass band starts rolling off at (38/80)*Fs and the rejection is -87dB at >(1-38/80)*Fs. Based upon the center frequency of the input, the interpolated reference is then shifted and flipped if necessary, which is determined based upon detection of the majority of the frequency content in the interleaved spectrum before correction or by user input, such as in a communications system or test and measurement environment. If a sharper transition is desired a different structure may be used as described in Chapter 2. The roll off can be seen in the SFDR of the corrected model with and without the

jitter mismatch in Figure 42. The purpose of this distinction was to see if the jitter mismatch would affect the correction scheme greatly due to the interpolated reference, it does not.

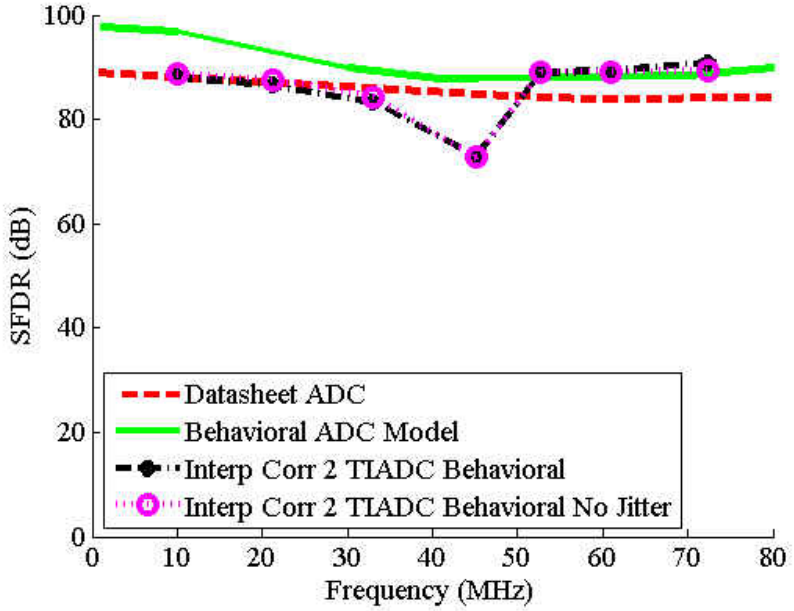

Figure 42: SFDR, Interpolated Reference 2 TI-ADC

Figure 43b shows the multi-tone spectrum and mismatch spurs before correction and Figure 43a the spectrum after correction in the 2 TI-ADC channelized correction case. Comparing the two parts of the figure more clearly shows that the largest spurs can be seen near the 40MHz region where the interpolated reference tapers off.

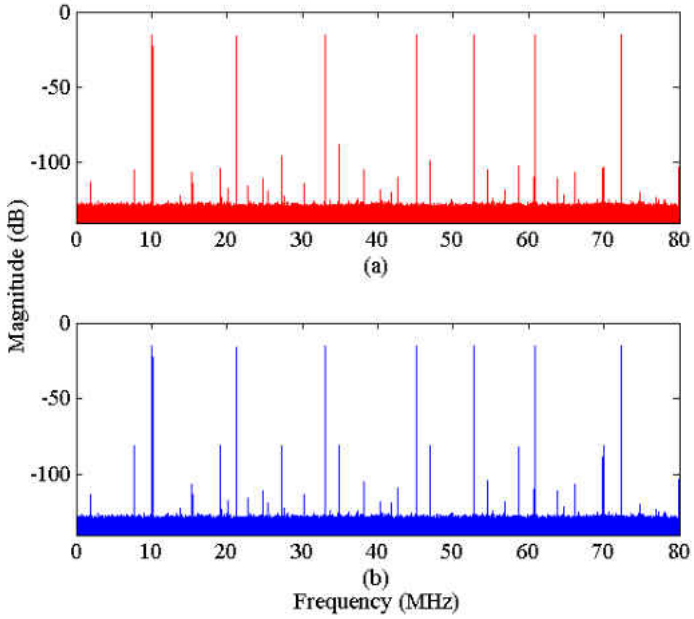

Figure 43: Behavioral Model Interpolated Error a) 2 TI-ADC multitone input with channelized correction b) 2 TI-ADC multi-tone input uncorrected

Cumulant Error

The performance in this section is limited not only by the interpolation filter used to generate the reference channel but also the approximation of the cumulants as well as the choice of which cumulant is being used to drive the adaptation. The SFDR of the corrected channel in a 2 TI-ADC system is shown as the dot dashed black line in Figure 44. The same interpolation filter as the prior section is used here. The Boxcar filter length in the cumulant approximation is 1000. The offset mismatch is turned off and assumed to be corrected before adaptation begins when using the first order cumulant for adaptation, this initial correction reduces the time to convergence. The results shown in, Figure 44, Figure 45, and Figure 46 are based on the first order cumulant. Experimentations were also done with the third and fourth order cumulants, however known information about the input is required to estimate what the Skewness or

Kurtosis of the error signal would be in order to subtract this value from the cumulant for minimization.

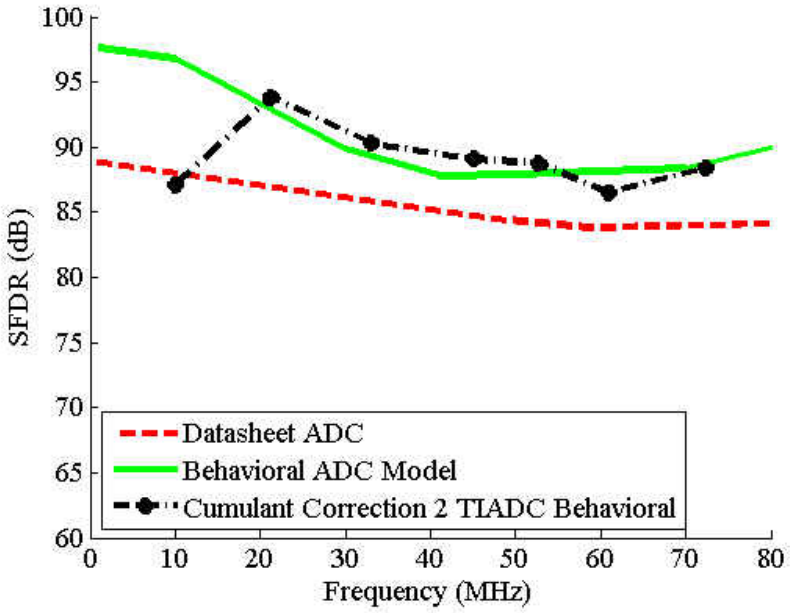

Figure 44: SFDR, Cumulant Correction 2 TI-ADC

Figure 45b shows the multi-tone spectrum and mismatch spurs before correction and Figure 45a the spectrum after correction in the 2 TI-ADC channelized correction case. Comparing the two parts of the figure shows that the remaining spurs after correction are suppressed below -100dB. This method was much more sensitive to step size, requiring a step to be at least two orders of magnitude smaller than the direct error correction. Only a partial suppression of the QPSK input was achieved based only on the first order cumulant. The overlapped corrected and mismatched spectrums are shown in Figure 46.

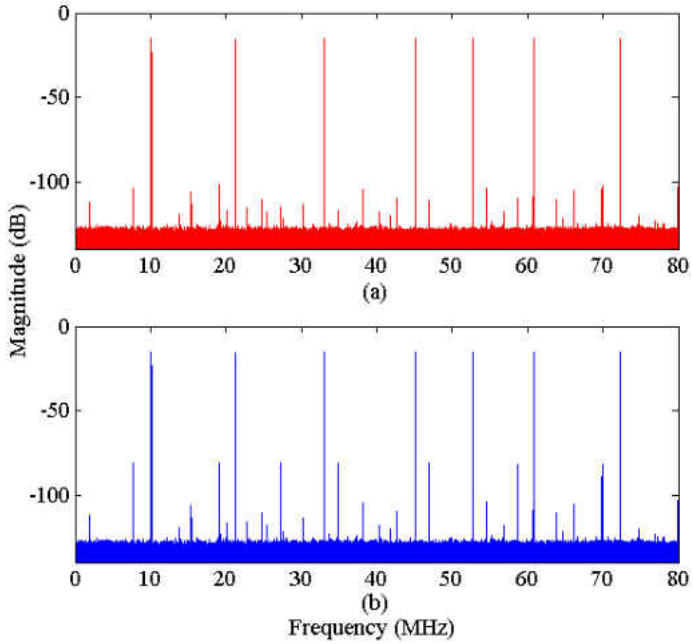

Figure 45: Behavioral Model Cumulant Based Correction 2 TI-ADC multitone input (a) with channelized correction b) uncorrected

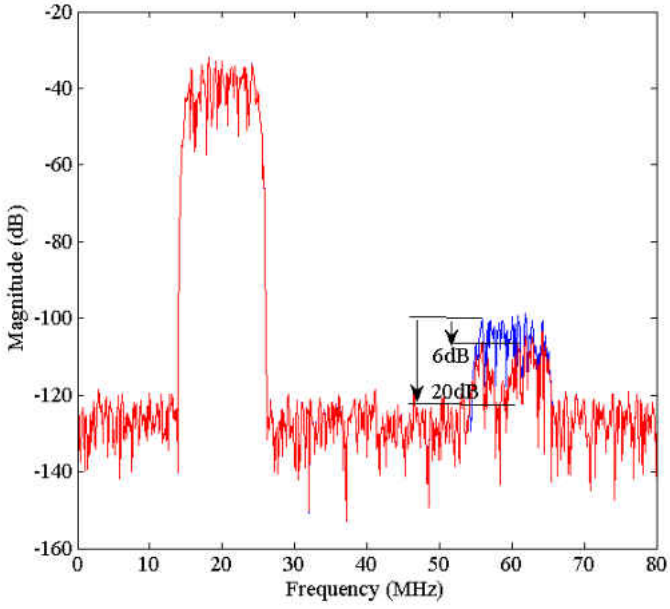

Figure 46: Partially suppressed QPSK correction based on cumulant statistics

CHAPTER 4: CONCLUSIONS

The contribution of the research presented in this dissertation is three fold. A behavioral model was developed and introduced as a research and development tool, an adaptive post conversion correction for non-linear mismatches was derived and simulated, and the use of cumulants in adaptation for this field was introduced.

The behavioral model had the goal of closely approximating the behavior of the dominate error sources in an ADC such that when combined, the overall ADC simulation represents the behavior of that ADC to a required fidelity without the use of expensive time consuming Spice models or the inflexibility of hardware in the loop. It also allows researchers to test the performance of their correction schemes with selective errors mismatched allowing the evaluation of these methods to potential sensitivities. This model, if widely used will allow researchers to compare new and existing methods on an independent model.

The correction method allows adaptive updating using a quadratic error surface, guaranteeing that there is a set of coefficients that minimize the error. The adaptive method is left up to the user but an example of the LMS algorithm was used in the results presented in Chapter 3. Ideal suppression was shown to be possible and realizable solutions were presented with good performance results.

Channelized correction, utilizing sinusoidal inputs, applied to the polynomial model, for comparison to existing methods, achieved ideal suppression utilizing an ideally matched error, up to 100dB in the 4 TI-ADC case. This outperforms that of [53] both in performance and computational complexity. The behavioral model showed suppression of an average of 42dB and

up to ideal suppression in the ideally matched 4 TI-ADC case, an average of 40dB suppression up to ideal suppression in the interpolated reference 2 TI-ADC case due to filter constraints, and an average of 35 dB up to ideal suppression in the cumulant based correction 2 TI-ADC case. Applied to a QPSK input, approximately 16dB of suppression, close to ideal, was achieved in the interpolated reference case and between 6 and 20dB of suppression in the cumulant based correction, 2 TI-ADC case. Due to the use of the behavioral model direct comparison to other methods is not possible but since ideal suppression is shown this is an improvement over the partial suppression of competitors.

Further research in the use of cumulants for adaptation of the weights could be useful as this dissertation has only scratched the surface of what is possible. Parameters that will affect the speed and efficacy of adaptation include the level of approximation of the cumulants, the sensitivity of a given cumulant to the errors present and the adaptation step size used. If a particular implementation can be characterized fully the use of these cumulants could selectively reduce certain mismatches. Further investigation of hybridizing this method with others should be completed.

APPENDIX A: IEEE COPYRIGHT PERMISSION

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APPENDIX B: MATLAB CODE

Simulink™ Models

All .mdl files seen in Figure 47 through Figure 58 may be requested via email from charna@charnaparkey.com. See below for screen shots of the various models used in this research.

Polynomial Model

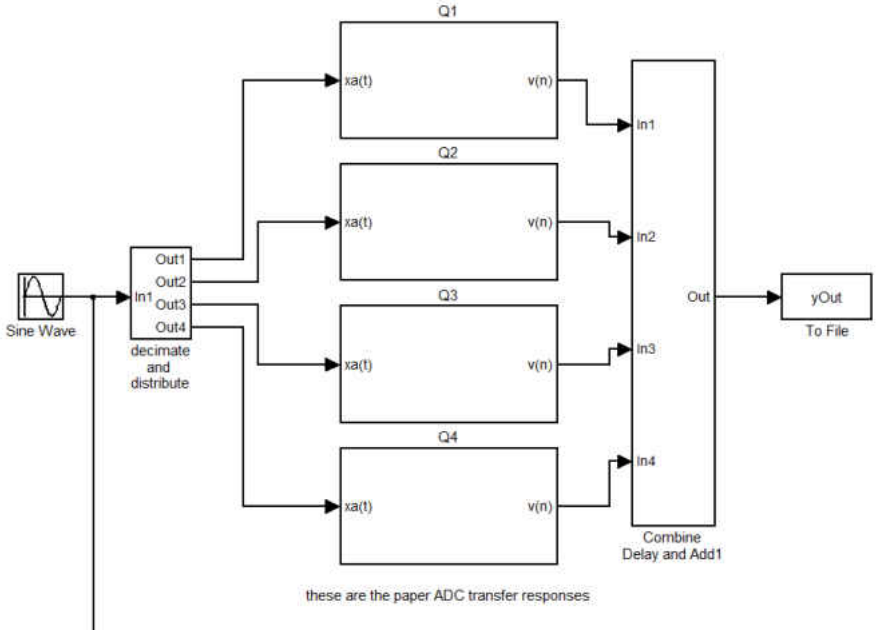

Figure 47: Polynomial 4 TI-ADC Model

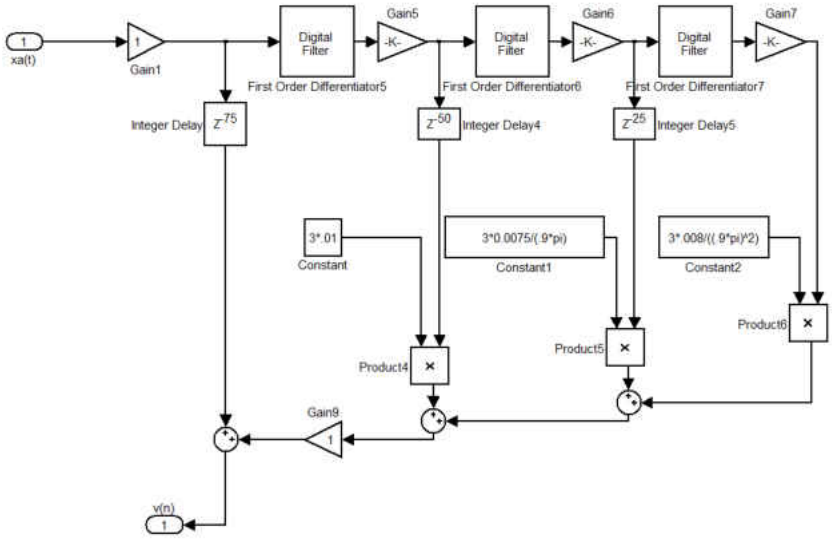

Figure 48: Individual Polynomial Channel Model

Behavioral Model single ADC

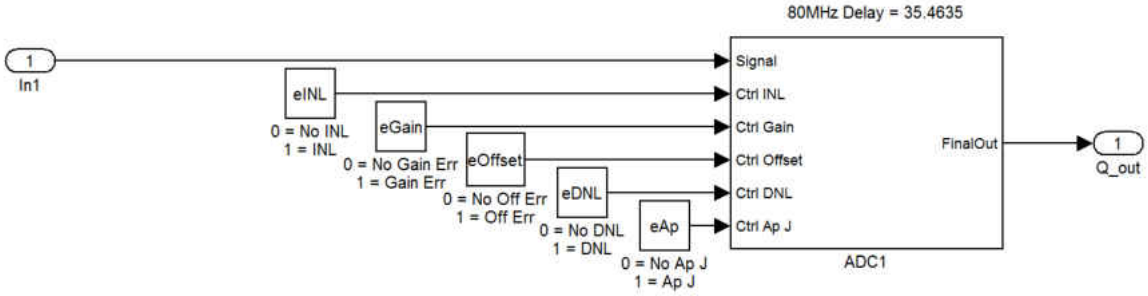

Figure 49: Single ADC Behavioral Model

2 TI-ADC Model with Correction and Test

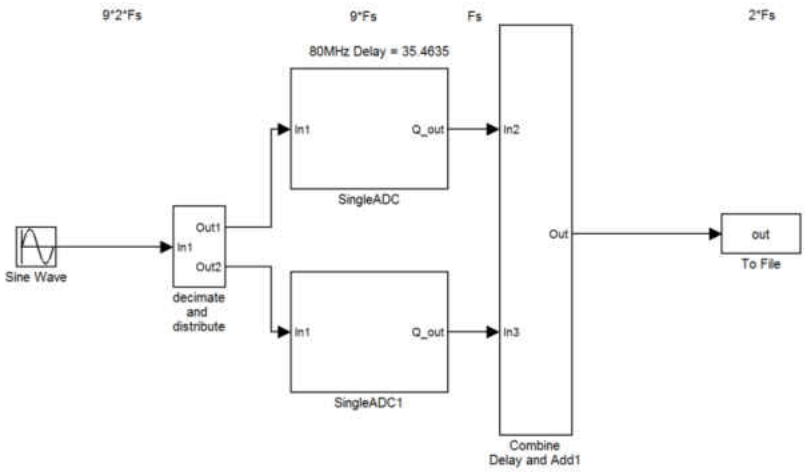

Figure 50: Behavioral 2 TI-ADC Model

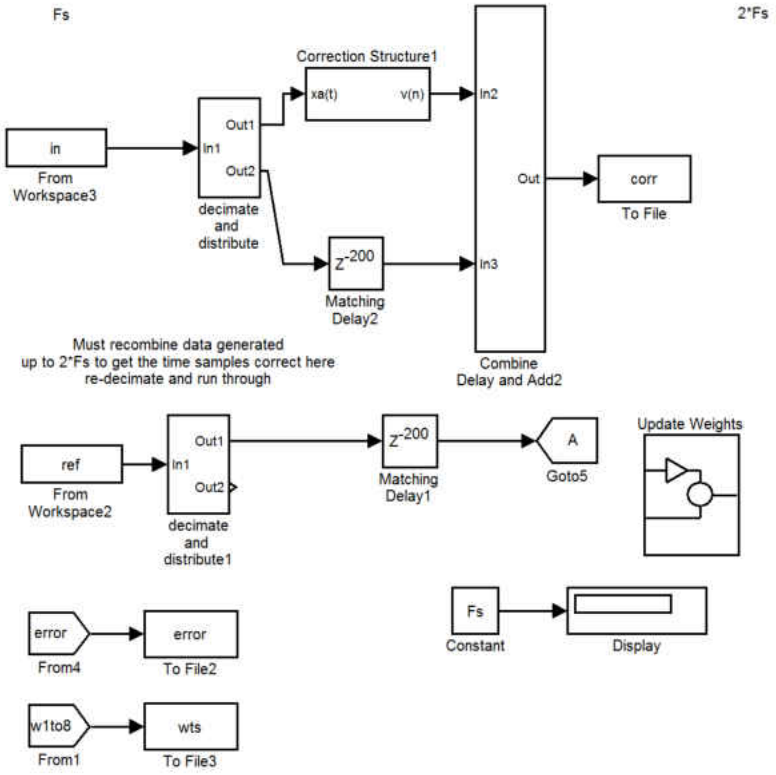

Figure 51: Behavioral 2 TI-ADC Correction Model

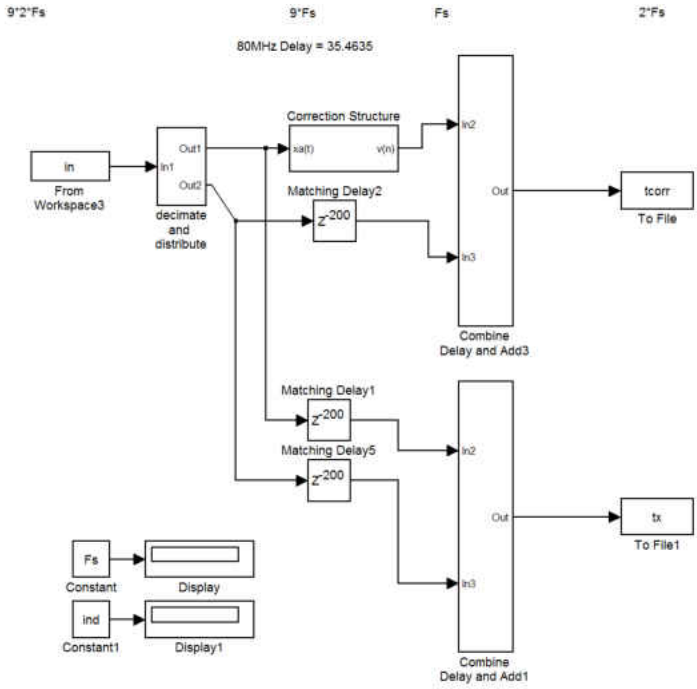

Figure 52: Behavioral 2 TI-ADC Weights Test Model

4 TI-ADC Model with Correction and Test

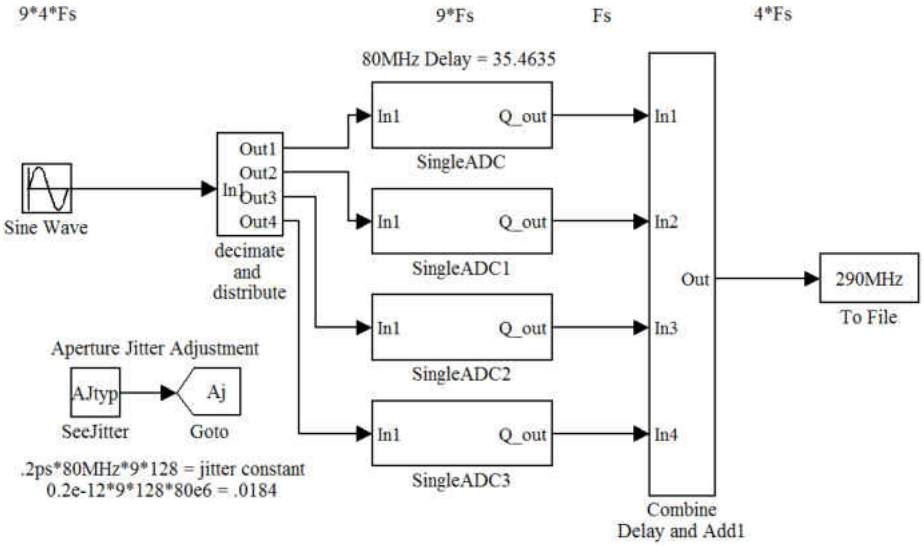

Figure 53: Behavioral 4 TI-ADC Model

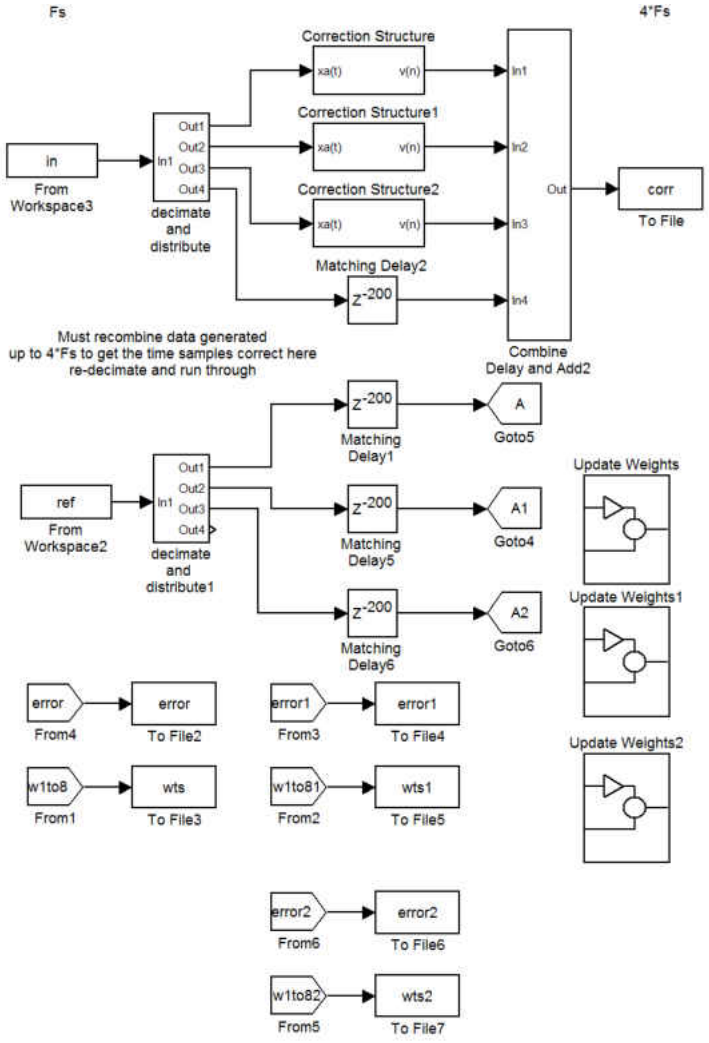

Figure 54: Behavioral 4 TI-ADC Correction Model

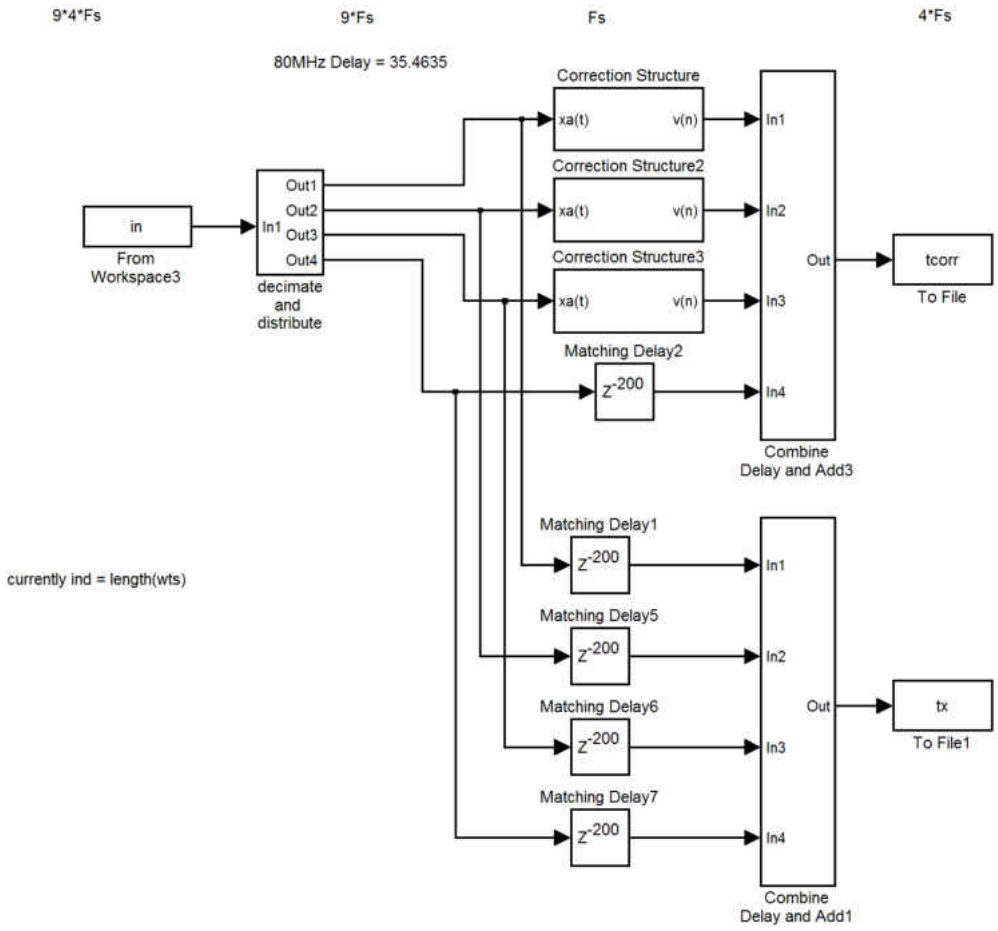

Figure 55: Behavioral 4 TI-ADC Weights Test Model

Generate QPSK Input

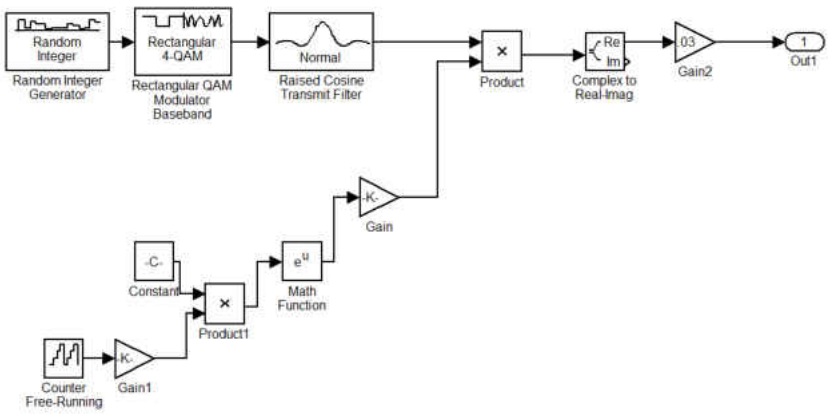

Figure 56: Wideband QPSK Passband Input Model

Cumulant Calculation

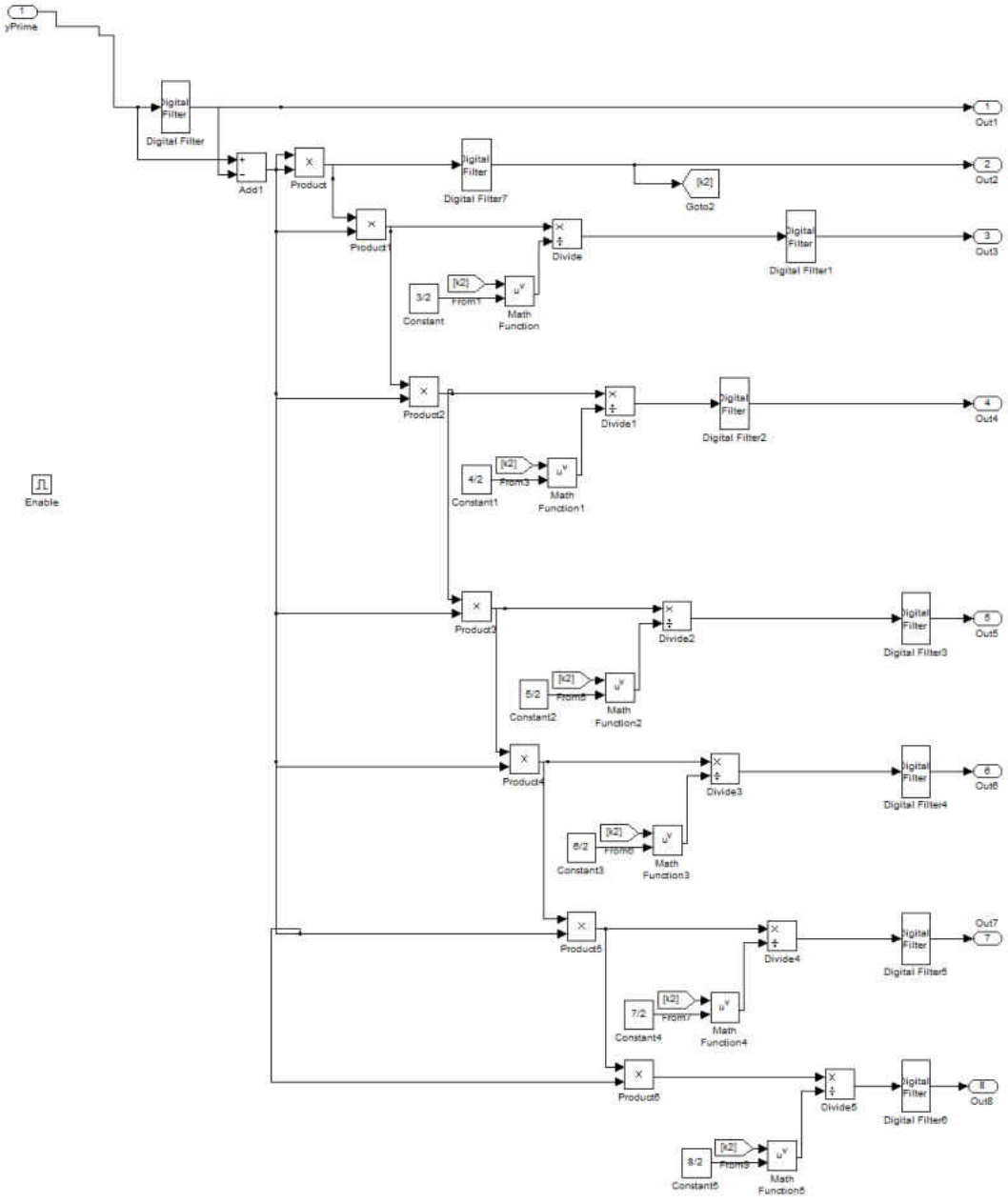

Figure 57: Cumulant Calculation Model

Chirp Response

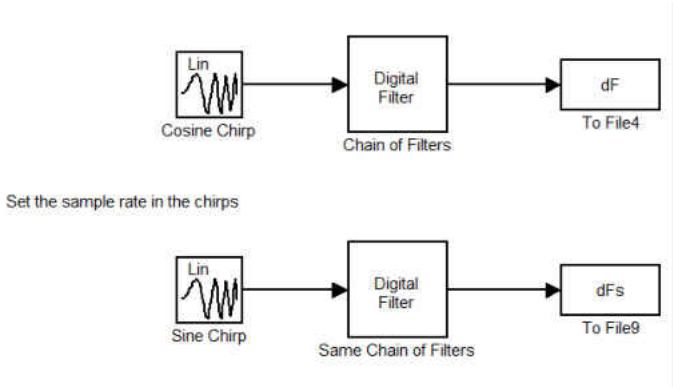

Figure 58: Generic Single Rate Chirp Response Model

Custom Functions

The following m files are also available upon request from charna@charnaparkey.com other m files not listed are supporting plot functions that are not specific contributions to this research but are available as well in order to reproduce results.

CreateINLErrorFirpm

```
function [InvINLErrCoeff, INLErrCoeff] = CreateINLErrorFirpm

clc

%close all;

%these are the samples I made from the plot in the datasheet

%they accurately represent the graph when plotted
```

```
% x = [0,49,58.75,100,150,175,200,300,325,400];

% y= [89,84.4,83.8,84.4,79,81.5,76.5,75.2,75.2,71.5];

% FsINL = 800; %MHz sampling frequency for the filter

L = 128; %number of samples to take of the curve

N = 32*8;%2^9; %order of the FIRPM output filter

% %Use a shape preserving interpolant to recreate the plot and get the L

% %values for the firpm recreation.

% pp = interp1(x,y,'pchip','pp');

% xi = 0:FsINL/((L-1)*2):FsINL/2;

% yi = ppval(pp,xi);

%These are values from the 6th order polynomial approx of above sfdr curve

%256 points 0:.8

fx=[89.8803103719853,89.6217487425421,89.3731908768659,89.1343351894494,88.90488545
64346,88.6845507663877,88.4730454712236,88.2700891372780,88.0754064965295,87.888727
3979697,87.7097867591234,87.5383245177163,87.3740855834925,87.2168197901809,87.0662
818476098,86.9222312939715,86.7844324482343,86.6526543627054,86.5266707757404,86.40
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472854,84.6484023326184,84.6091954640346,84.5711629943280,84.5341946557228,84.49818
35170509,84.4630259410783,84.4286215419808,84.3948731429684,84.3616867340584,84.328
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48163,83.4574288378483,83.4143199787961,83.3702597987681,83.3252284258765,83.279207
9574776,83.2321824225612,83.1841377442884,83.1350617026790,83.0849438974469,83.0337
757109850,82.9815502714991,82.9282624162905,82.8739086551870,82.8184871341239,82.76
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61,81.7907995073252,81.7183543598128,81.6450472263049,81.5709006170825,81.495937981
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00894,78.1782633543420,78.0972636373847,78.0168599500532,77.9370865950371,77.857977
4899894,77.7795661407857,77.7018856149321,77.6249685151216,77.5488469529398,77.4735
525227194,77.3991162755435,77.3255686933981,77.2529396634731,77.1812584526124,77.11
05536819129,77.0408533014725,76.9721845652866,76.9045740062942,76.8380474115722,76.
7726297976788,76.7083453861462,76.6452175791216,76.5832689351577,76.5225211451514,
76.4629950084320,76.4047104089983,76.3476862919038,76.2919406397920,76.23749044957
96,76.1843517092892,76.1325393750307,76.0820673481311,76.0329484524146,75.985194411
6298,75.9388158270272,75.8938221550848,75.8502216853834,75.8080215186294,75.7672275
448283,75.7278444216057,75.6898755526777,75.6533230664704,75.6181877948877,75.58446
92522290,75.5521656142547,75.5212736974011,75.4917889381444,75.4637053725134,75.437
0156157510,75.4117108421244,75.3877807648850,75.3652136163766,75.3439961282922,75.3
241135120803,75.3055494395003,75.2882860233255,75.2723037981969,75.2575817016241,7
5.2440970551362,75.2318255455815,75.2207412065754,75.2108164000981,75.202021798240
7,75.1943263651001,75.1876973388232,75.1821002137998,75.1774987230041,75.1738548204
859,75.1711286640096,75.1692785978432,75.1682611356953,75.1680309438017,75.16854082
41605,75.1697416979159,75.1715825888918,75.1740106072729,75.1769709334364,75.180406
8019308,75.1842594856052,75.1884682798863,75.1929704872051,75.1977014015721,75.2025
942933014,75.2075803938838,75.2125888810091,75.2175468637366,75.2223793678150,75.22
70093211512,75.2313575394278,75.2353427118697,75.2388813871594,75.2418879595011,75.

```
2442746548344,75.2459515171959,75.2468263952305,75.2468049288512,75.2457905360476,
75.2436843998443,75.2403854554067,75.2357903772970,75.2297935668785,75.22228713986
87,75.2131609140418,75.2023023970795,75.1895967745712;];

%convert from dB to a number

ynum=10.^(fx/10);

%normalize

ynorm=ynum/max(ynum);

xnorm1 = 0:.8/255:.8;

%xnorm1 = 0:1/127:1;

%prepare the final curve for firpm

%1 plus Inverse of the curve

y3 = 1+ynorm.^(-1);

%figure(2);

%plot(xnorm1,y3);

y2=zeros(1,length(fx));

y2(1:length(y3))=y3;

%inverse y3
```

```
y6 = y3.^(-1);

%y6 = ynorm;

%figure(1);

xnorm = [xnorm1, .95, 1];

%plot(xnorm1,y6)

y2 = [y2, 0, 0];

y6 = [y6, 0, 0];

%Create the first filter

%Method 2

INLErrCoeff = fir2(N,xnorm,y2);

%fvtool(INLErrCoeff)

%Create the inverse filter

%Method 2

InvINLErrCoeff = fir2(N,xnorm,y6);

%fvtool(InvINLErrCoeff)

%To plot the error uncomment the following two lines
```

```
%errOut=conv(INLErrCoeff,InvINLErrCoeff);

%freqz(errOut);
```

gainErr_equi_D_p011

```
function b = gainErr_equi_D_p011(Dpass)

%GAINERR_EQUI_D_P011 Returns a discrete-time filter object.

% M-File generated by MATLAB(R) 7.7 and the Signal Processing Toolbox 6.10

% Generated on: 16-Jun-2010 13:39:27

% Equiripple Lowpass filter designed using the FIRPM function.

% All frequency values are normalized to 1.

Fpass = 0.8;    % Passband Frequency

Fstop = 0.9;    % Stopband Frequency

% Dpass = 0.0011;  % Passband Ripple

Dstop = 0.001;  % Stopband Attenuation

dens  = 20;     % Density Factor

% Calculate the order from the parameters using FIRPMORD.

[N, Fo, Ao, W] = firpmord([Fpass, Fstop], [1 0], [Dpass, Dstop]);
```

```
% Calculate the coefficients using the FIRPM function.

b  = firpm(N, Fo, Ao, W, {dens});

Hd = dfilt.dffir(b);

% [EOF]
```

LoadHalfBandInterps

```
function [b1, b2, b3, b4, b5, b6, b7] = LoadHalfBandInterps()

%Design 7 integrators.

%% Stage 1

N = 42;

b1 = firpm(42,[0 32/80 1-32/80 1],[1 1 0 0]); %Why 42 taps?

b1(2:2:end) = 0;

b1(ceil(end/2)) = .5;

%% Stage 2

%Design a new filter since the spectrum is now in a smaller band.

b2 = firpm(22,[0 32/160 1-(32/160) 1],[1 1 0 0]);

b2(2:2:end) = 0;
```

```
b2(ceil(end/2)) = .5;

%% Stage 3

%Design a new filter since the spectrum is now in a smaller band.

b3 = firpm(22,[0 32/320 1-(32/320) 1],[1 1 0 0]);

b3(2:2:end) = 0;

b3(ceil(end/2)) = .5;

%% Stage 4

%Design a new filter since the spectrum is now in a smaller band.

b4 = firpm(22,[0 32/640 1-(32/640) 1],[1 1 0 0]);

b4(2:2:end) = 0;

b4(ceil(end/2)) = .5;

%% Stage 5

%Design a new filter since the spectrum is now in a smaller band.

b5 = firpm(10,[0 32/1280 1-(32/1280) 1],[1 1 0 0]);

b5(2:2:end) = 0;

b5(ceil(end/2)) = .5;
```

```
%Design a new filter since the spectrum is now in a smaller band.

b6 = firpm(10,[0 32/2560 1-(32/2560) 1],[1 1 0 0]);

b6(2:2:end) = 0;

b6(ceil(end/2)) = .5;

%% Stage 7

%Design a new filter since the spectrum is now in a smaller band.

b7 = firpm(10,[0 32/5120 1-(32/5120) 1],[1 1 0 0]);

b7(2:2:end) = 0;

b7(ceil(end/2)) = .5;
```

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