THE ELECTRONIC STRUCTURE WITHIN THE MOBILITY GAP OF TRANSPARENT AMORPHOUS OXIDE SEMICONDUCTORS

by

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Transparent amorphous oxide semiconductors are a relatively new class of materials which show significant promise for electronic device applications. The electron mobility in these materials is at least ten times greater than that of the current dominant material for thin-film transistors: amorphous silicon. The density of states within the gap of a semiconductor largely determines the characteristics of a device fabricated from it. Thus, a fundamental understanding of the electronic structure within the mobility gap of amorphous oxides is crucial to fully developing technologies based around them. Amorphous zinc tin oxide (ZTO) and indium gallium zinc oxide (IGZO) were investigated in order to determine this sub-gap structure. Junction-capacitance based methods including admittance spectroscopy and drive level capacitance profiling (DLCP) were used to find the free carrier and deep defect densities. Defects located near insulator-semiconductor interfaces were commonly observed and strongly depended on fabrication conditions. Transient photocapacitance spectroscopy (TPC) indicated broad

valence band-tails for both the ZTO and IGZO samples, characterized by Urbach energies of 110±20 meV. These large band-tail widths imply that significant structural disorder exists in the atomic lattice of these materials. While such broad band-tails generally correlate with poor electronic transport properties, the density of states near the conduction band is more important for devices such as transistors. The TPC spectra also revealed an optically active defect located at the insulator-semiconductor junction. Space-charge-limited current (SCLC) measurements were attempted in order to deduce the density of states near the conduction band. While the SCLC results were promising, their interpretation was too ambiguous to obtain a detailed picture of the electronic state distribution. Another technique, modulated photocurrent spectroscopy (MPC), was then employed for this purpose. Using this method narrow conduction band-tails were determined for the ZTO samples with Urbach energies near 10 meV. Thus, by combining the results of the DLCP, TPC and MPC measurements, a quite complete picture of the density of states within the mobility gap of these amorphous oxides has emerged. The relationship of this state distribution to transistor performance is discussed as well as to the future development of device applications of these materials.

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For Grandpa Del and Far-Far

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CHAPTER I

INTRODUCTION

1.1. Amorphous Materials

A wide variety of materials used every day including window glass, candle wax and even cotton candy have an amorphous atomic structure. The term amorphous simply means that there is short range atomic order in the lattice, however there is no long range repeatability of this order. There may be the same number of nearest neighbors to an atom which are located approximately the same distance away from said atom with roughly similar bond angles. A cartoon of a disordered lattice as opposed to a crystalline lattice is shown in Figure 1.1, illustrating the disorder present in these materials. However, if one were to look at the radial distribution function of the next nearest neighboring atoms and those further away, the function would appear smeared out, without any of the discrete features that are found in crystalline lattices. A good example of this, for amorphous germanium, can be found in Zallan.[1] Amorphous matrices are formed when materials do not have time for the constituent atoms to rearrange

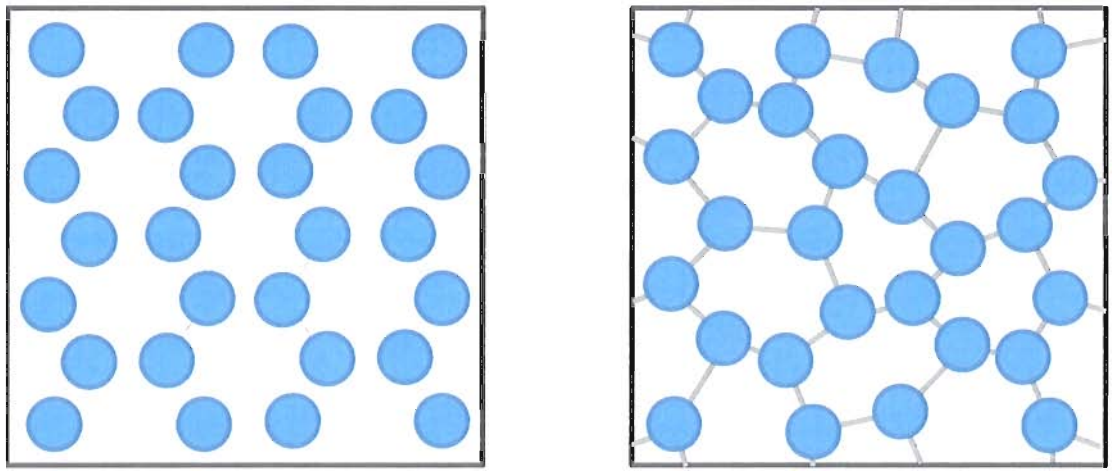

Figure 1.1: Sketch of a crystalline lattice (left) as opposed to an amorphous lattice (right). The underlying crystalline structure is evident in the amorphous network, however the bond angle disorder negates any long-range periodicity. Structural disorder such as impurities, interstitial atoms, and lattice vacancies may also be present in disordered materials.

themselves into the most thermodynamically stable state before they are cooled. Thus it is theoretically possible for most materials to be fabricated with an amorphous structure, although it may not be practically possible. For electronic device applications, amorphous materials are desirable because they can typically be fabricated in large areas at lower temperatures, opening the door to flexible substrates and lower costs of manufacturing.

The very possibility of amorphous semiconductors was debated until the 1950s, when research began on amorphous selenium. The fact that the bond lengths and angles are distorted destroys the repeatability of the unit cell, thus the materials do not contain any of the long-range periodic structure which enables mathematical descriptions of

crystalline semiconductors. In spite of this, many of the formalisms used to describe crystalline materials work well in describing amorphous semiconductors as well. Most notable, and most important in semiconductor physics, are the conduction and valence bands, and the "forbidden" energy gap between the bands. The difference in the descriptions of the crystalline and amorphous materials arises in exactly how one defines the band-gap in the amorphous state. In purely crystalline materials, there is a complete lack of states within the band gap, and the delocalized conduction and valence bands begin somewhat abruptly at the band edges. In amorphous materials there is a smooth transition between the localized states (in which carriers can become trapped) and the states which extend throughout the lattice. Thus, it is more common to speak of a "mobility gap" in amorphous materials. That is, in crystalline materials there are no states below the gap for electrons to reside, while in amorphous materials electrons below the mobility gap can become trapped in localized states. In either material, an electron with energy above the gap will be able to conduct DC current.

In addition to the band-tails extending into the band-gap, in amorphous and disordered materials it is also common to find bands of defect states within the mobility gap. These defects are the result of lattice disorder including atomic vacancies, substitutions and interstitials. In most amorphous and disordered materials being developed for semiconductor applications, these defect states typically have a density between 10^{14} cm^{-3} and 10^{17} cm^{-3}. A worthwhile goal in order to produce the full potential of a device built around an amorphous material is to completely understand and control the defect

structure within the mobility gap. Some parts of the density of states are intrinsic to a material, however others can by modified with fabrication and passivation methods.

Hydrogenated amorphous silicon (a-Si:H), probably the most prototypical disordered semiconductor, has been very extensively studied since the first report of an a-Si photovoltaic solar cell in 1976 by Carlson and Wronski.[2] The promise of cheap, renewable energy brought many investigations, both experimental and theoretical, into the fundamental nature of this disordered material. The amount of insight gained into the atomic processes that are present in a-Si certainly sets the standard high in the development of other disordered materials. While there are still many questions that remain unanswered, there is a majority consensus on the sub-band gap defect structure and the atomic origin of the defects. This is illustrated in Figure 1.2 showing exponential band tails extending into the gap plus several mid gap defects attributed to dangling Si bonds. Amorphous silicon was nearly unusable for devices because of the very large density of dangling bond defects initially. Spear and LeComber discover that the defect density could be greatly reduced through hydrogenation, and also that a-Si:H could exhibit both n-type and p-type conductivity as dopants were added.[3] Brodski later quantified the importance of hydrogen in the network in 1977.[4] Hydrogen passivates the silicon dangling bonds and can reduce the deep defect density from near 10^{19} cm^{-3} to 10^{15} cm^{-3}. As a result of these investigations, the stabilized conversion efficiency of amorphous silicon photovoltaic solar cells has increased from 2.4% to over 12%. Amorphous silicon has also become widely used in thin-film transistor devices and

maintains a dominant role in driving LCD displays. The benefits of large area and lower temperature deposition outweigh the downsides of decreased device performance when compared to crystalline silicon in certain applications such as LCD displays.

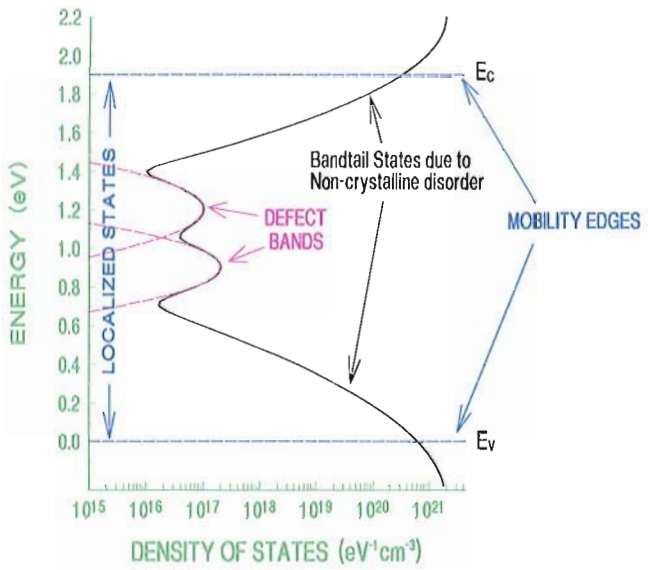

Figure 1.2: Sub band-gap density of states in amorphous silicon showing exponential band tails and discrete defect bands. The exponential band tails stem from the structural disorder in the lattice while the discrete defect bands arise from impurities such as dangling bonds.

To further complicate the sub-band gap defect structure in amorphous materials, electrically active defects can also readily appear at interfaces and junctions as well as in the bulk of the semiconductors. All of these electrically active defects can limit the performance of whatever device is being utilized, whether that refers to switching speeds in electronic circuits or conversion efficiencies in photovoltaic solar cells. Thus, in order

to achieve the full potential of devices that are manufactured from amorphous and disordered materials, a fundamental understanding of the sub-band gap defect structure is required. Only at this point can the material be fine-tuned by means of passivating detrimental defects or introducing dopants to control the carrier density.

1.2. The Urbach Edge

The states which extend from the edge of the gap into the "forbidden region" are commonly referred to as band-tails. The density of states typically decreases exponentially into the gap for at least several orders of magnitude. This phenomenon was first noticed in 1953 by Franz Urbach[5] while studying optical absorption in AgBr, and has consequently been found in a very wide range of materials. The slope of this decay is thus called the Urbach energy, and is closely related to the amount of disorder in the material. The density of states extending into the gap is typically represented as follows:

$$N \propto N_0 e^{\frac{E-E_0}{E_U}}$$

Where N_0 is the density of states either at the conduction band or valence band edge, E is the optical energy, E_0 is a fitting parameter that has to do with the band gap of the material, and E_U is the Urbach energy representing the slope of the decay. The disorder

represented by the Urbach energy can be both thermal and structural. Crystalline materials have an Urbach energy which is attributed solely to thermal fluctuations in the lattice, thus providing a direct measurement of the thermal occupation of phonon states in the crystal. In amorphous materials the Urbach energies are typically much larger, and contain contributions from the bond angle variations, interstitial atoms, and vacancies where an atom is missing from the lattice. While studying hydrogenated amorphous silicon, Cody concluded that the types of disorder are additive[6], meaning that the Urbach energy can be represented as follows:

$$E_U(T,X) = k[\langle U^2\rangle_T + \langle U^2\rangle_X]$$

Where T and X correspond to the thermal and structural contributions to the disorder.

The investigation into understanding the origins and effects of Urbach edges in amorphous materials continues to yield interesting developments. Recently Pan and Drabold used a simulated 512-atom model to investigate the atomic origins of the Urbach tails in amorphous silicon[7]. They found very interesting results including the presence of "islands and filaments" of long and short bonds which appear to be connected to the tail states in the electronic structure. While the most intuitive explanation of band tails might be the random fluctuation of the conduction and valence bands[8], this result finds more established order in the amorphous network.

1.3. Thin-Film Transistors and Mobility

Transistors in general are one of the primary building blocks in any electronics application. Since the first transistor action was demonstrated in 1947 by Bardeen and Brattain[9], transistors have become smaller and more efficient devices. Transistors act as a very low-power switch: by applying a potential to the gate, the semiconductor is converted from an insulating layer to a conducting channel between the source and the drain. The typical structure of a thin-film transistor (TFT) is shown in Figure 1.3, illustrating the co-planar source and drain contacts as well as the gate. The transistors are termed "thin-film" to refer to the channel layer thickness, which is normally less than several hundred nanometers and are at most several micrometers thick.

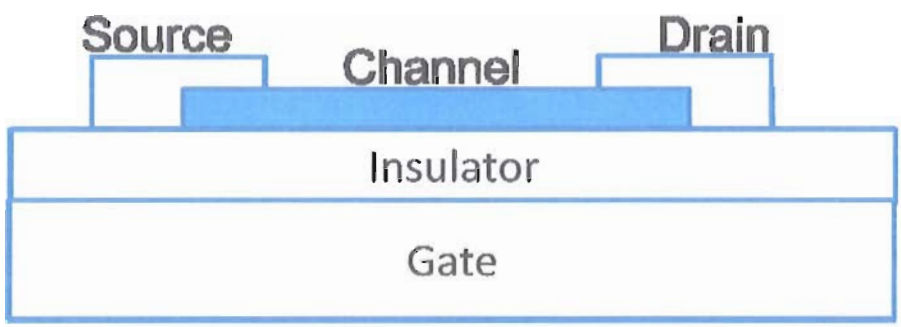

Figure 1.3: Thin film transistor (TFT) structure. When the correct bias is applied to the gate, the channel layer will switch between being conducting and insulating between the source and drain.

When a sufficient potential is applied to the gate, an excess of carriers (either electrons or holes) collects along the interface between the insulator and the semiconductor, creating the conducting layer. Depending on the materials used, transistors can be either depletion mode or enhancement mode, referring to whether or not the channel is conducting with no potential applied to the gate, respectively. These types of transistors can be thought of as normally on devices or normally off devices. This nomenclature persists whether the channel is n-type or p-type. A typical way to characterize transistor devices is shown in Figure 1.4, measuring the current between the source and the drain (at one voltage) while varying the potential on the gate.

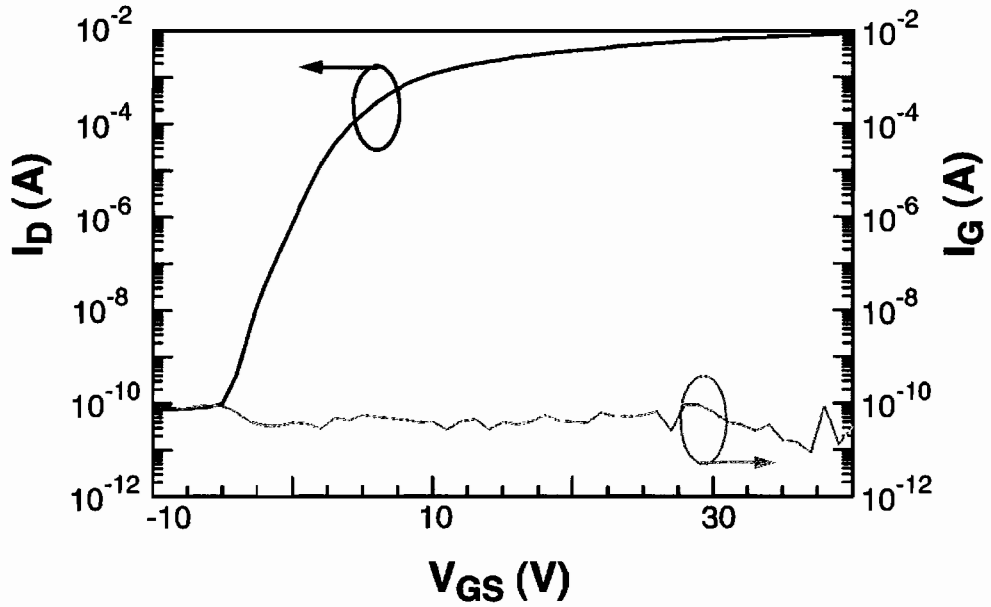

Figure 1.4: Typical characterization of thin-film transistor performance. This device shows very good performance behavior with a on/off current ratio of $>10^6$ and a turn-on voltage near $V_{GS} = 0V$.

When this device has $V_{GS} \sim -10$ V, the device is "off" and very little current flows between the source and the drain, less than 10^{-10} A. However, when $V_{GS} \sim +10$V, the current increases by more than seven orders of magnitude to better than 10^{-3} A. Note also the turn-on voltage where the current starts to increase (in this device near -5 V) and the quite shallow slope of the plot near 0 V. Both of these parameters are very important for device performance as well, and depend strongly on the characteristics of the interface between the channel layer and the insulator.

1.4. Mobility: Device and Bulk

Mobility measurements can provide a good idea of the quality of a material for electronics applications. In the most general sense, mobility measures how efficiently a carrier moves in response to an applied electric field. The mobility, μ, is then defined to be

$$v_n = -\mu_n \mathcal{E}$$

With this constant, the electron drift velocity can be written as a function of the applied electric field $\mathcal{E}$. In crystalline materials, where the mean free path is much larger than the bond length, the mobility can be related to other fundamental properties:

$$\mu = \frac{q\tau_c}{m_n}$$

where q is the fundamental charge, τ_c is the mean free time, and m_n is the effective mass of the carrier. The mean free time is determined by the probability of scattering events, both with the lattice and with impurities. The effective mass of the carrier is determined by the band structure of the material. In amorphous materials the mobility becomes much more complicated. For instance, how could one determine an effective mass for an electron without a band structure, when the band structure is calculated from the periodicity of the lattice? In most amorphous materials, an "effective mobility" is used which may be influenced by a number of factors including the disorder and fluctuations in the structure of the lattice.[1, 10]

Thorough discussions of carrier mobility in semiconductors can be found in texts such as Sze[11]. For reference, doped crystalline silicon will typically have electron mobilities near 200 $cm^2(V*s^{-1})$ while the highest mobilities measured for amorphous silicon are around 1 $cm^2(V*s^{-1})$. The mobility of a material is typically limited by disorder in the material such as impurities and grain boundaries, thus it is easy to recognize that the mobility is greatly impacted by the Urbach energy in a material. It is important, however, to distinguish between several different ways to measure the mobility. These can be divided into two sets: mobility measurements on the bulk of a semiconductor, and mobilities derived from transistor current vs. voltage characteristics.

Bulk Measurements

Hall effect and four point resistivity measurements are the most common way to determine the carrier concentration and mobility of a semiconductor. The Hall effect measures the potential generated across a sample when a magnetic field is applied in a direction perpendicular to the direction of current flow.[11] That is, the potential (and the associated electric field, $\mathcal{E}_y$) is generated in the direction orthogonal to both the direction of current flow (J_n) and the applied magnetic field (B_z). The Hall coefficient is defined as

$$R_H \equiv -\frac{\mathcal{E}_y}{J_n B_z} = -\frac{1}{qn}$$

Thus the carrier concentration can be determined from the Hall effect measurements (q is a fundamental unit of charge). Although the conductivity of a semiconducting sample technically depends on both the electrons and holes, typically the carrier concentration of the majority carrier is many orders of magnitude larger than that of the other, which is then regarded as insignificant. The conductivity for a sample with an excess of electrons (n-type) can then be written as

$$\sigma = nq\mu_n$$

Now, knowing the carrier concentration and the conductivity of a sample, the electron mobility can be determined. Both Hall Effect and four point resistivity measurements

can be performed on samples fabricated in the van der Pauw geometry, enabling accurate mobility determinations.

Another common way to measure the bulk mobility is a time-of-flight measurement, where carriers are generated at one side of a sample and allowed to drift to the other under an applied electric field. For a good descriptions of drift-mobility experiments in relation to the Urbach edges in disordered silicon materials, see the articles written by Tiedje[12] and Schiff (2004)[13]. Also, Orenstein and Kastner discuss mobilities in the amorphous chalcogenide system.[14]

Device Mobility Measurements

Transistor curves such as shown in Figure 1.4 can also provide mobility information. Mobilities derived from the transistor curves are typically referred to as device mobilities, and while they do not necessarily reflect the mobility of the bulk of the semiconducting channel, they effectively characterize the characteristics of the entire device. The average device mobility is derived as follows:

$$\mu_{avg}(V_{GS}) = \left.\frac{G_D(V_{GS})}{\frac{W}{L}C_{Ins}(V_{GS} - V_{ON})}\right|_{V_{DS}\to 0}$$

In this expression, V_{GS} is the potential between the gate and the source, W and L are the width and length of the channel, C_{Ins} is the insulator capacitance, V_{ON} is the turn-on voltage, and $G_D(V_{GS})$ is the drain conductance. The expression is evaluated at small values of V_{DS}, in the linear regime of transistor performance, so that the channel can be modeled as a resistor. The drain conductance, G_D, is found at small values of V_{DS} as well:

$$G_D(V_{GS}) = \left.\frac{I_D}{V_{DS}}\right|_{V_{DS}\to 0}$$

Incremental and saturation mobilities can also be derived from transistor current vs voltage characteristics. These mobilities contain very specialized information and will not be referenced here. For a discussion of all three types of device mobilities with respect to thin film transistors, see Hoffman[15].

1.5. Transparent Conducting Oxides

Transparent conducting oxides (TCOs) formed with post-transition metal cations such as indium tin oxide (ITO) and zinc oxide (ZnO) have been investigated for a variety of applications for over 50 years. The material properties of high conductivity combined with transparency have proven to be very useful in a wide variety of applications from

photovoltaic solar cells to defrosting car windshields to UV opto-electronics. The conductivity of most TCOs is intrinsically n-type, however typically several orders of magnitude less than that of metals, so a variety of doping schemes are used to increase the conductivity of the materials such as SnO_2:F, In_2O_3:Sn and ZnO:Al.[16] The electron mobility in these crystalline materialsis quite high: up to 100 $cm^2V^{-1}s^{-1}$.

Because of the broad applicability of these materials, a wide variety of new components have been investigated for application in TCOs with the hope of increasing the conductivity to near metallic levels while at the same time decreasing costs. Researchers at the National Renewable Energy Laboratories have developed a way to explore broad regions of compositional phase space quickly by stoichiometrically grading samples in one and even two dimensions on a single substrate.[17] Many of these materials could be good candidates for semiconducting applications as well, with slightly different processing conditions and goals.

The amount of experimental work directed towards TCOs has also attracted theoretical investigations into the fundamental processes of present in the materials. There is some consensus that the conductivity in the materials is controlled by oxygen vacancies[18-20], however recent work by Janotti[21] has challenged this idea, at least in ZnO. While initial work suggested that the oxygen vacancies were close enough to the conduction band to donate carriers, more recent work has shown that the level is actually quite deep.

Janotti suggests that all intrinsic point defects in the material are too deep to efficiently dope the material, and instead outside dopants, such as hydrogen, should be considered. Another possibility for the source of intrinsic carriers in these materials could be interstitial metal atoms, as suggested by Kilic and Zunger.[22]

Transparent conducting oxides in the amorphous, rather than the crystalline, state have been attracting attention recently as well. Amorphous TCOs have been shown to retain the high electron mobilities associated with crystalline TCOs, with the added benefit of enabling low-temperature depositions and flexible substrates.[23, 24] While many of the formalisms developed in the extensive research into electronic processes in a-Si can be readily applied to amorphous TCOs, the differences between the materials must be noted as well. In a-Si, band structure calculations have determined that the valence band maximum is composed primarily of p-states and the conduction band minimum consists of mixed s- and p-states.[25] The angular dependence of the p-states means that the band structure is very susceptible to disorder in the material, and localized states near the mobility edges are easily produced. Indeed, the Urbach energy of the valence band tail in a-Si is typically near 45-50 meV and while the Urbach energy of the conduction band tail is lower, around 25-30 meV, it is still large enough to reduce the effective electron mobility to roughly 1 $cm^2V^{-1}s^{-1}$ at room temperature. In contrast, the conduction band minimum in TCOs is composed primarily of s-states from the metal cations such as Sn, Zn or Ga. If one were to consider any interaction between the orbitals of two

neighboring atoms, the distance between the atoms (r), angle between the orbitals (θ), and the dihedral (vertical) angle (φ), or

$$V(l,m) = V(r,\theta,\varphi)$$

However, when only the s-states need to be considered, all angular dependence to the orbitals can be neglected due to the spherical symmetry of the system, leaving just variations in the next-nearest neighbor distance.[25, 26]

$$V(l,m) = V(r)$$

Thus, structural disorder in amorphous TCOs should be expected to have little effect on the electron transport mechanism. The valence band maximum, however, is composed of p-states from the oxygen anions in TCOs, so the Urbach edge of the valence band-tail could be expected to reflect the structure disorder of amorphous TCOs. The first material known to exhibit this dichotomous type of behavior was amorphous SiO_2.[27] The electron drift mobility of this disordered material was measured by Hughes to be near 20 $cm^2V^{-1}s^{-1}$.[28] This high mobility can be explained by realizing that the conduction band of SiO_2 is composed of Si and O s-states, while the valence band depends on p-states. Thus there will be very few localized states to trap electrons and limit the mean free path length.

Zinc stannate, the crystalline form of one of the semiconductors on which I will focus, was the subject of some attention for a while. Young, following the preliminary work of Wu and Mulligan[29], found that the intrinsic optical band gap of zinc stannate to be 3.35 eV, which increases with increasing carrier density up to 3.85 eV due to the Burstein-Moss shift.[30] He also found that the electron effective mass ranges from 0.16 m_e to 0.26 m_e depending on the carrier density. Young also briefly examined amorphous ZTO films to determine the local atomic environments and concluded that they were very similar to the crystalline films.[31]

Further work has been carried out by Walsh[32], Da Silva[33] and Nomura[34] investigating the nature of conduction in the amorphous TCOs with an emphasis on amorphous $InGaZnO_4$. Walsh used density functional theory (DFT) to model the amorphous system in order to analyze the distribution of electronic states near the conduction band and valence band edges. He found that the primary difference between the amorphous and crystalline phases of IGZO is a series of bands which reside near the valence band maximum. He found no additional states near the conduction band minimum, explaining the persistence of good n-type conductivity in amorphous TCOs. Nomura[34] compared x-ray absorption fine structure (XAFS) data for IGZO to calculations to investigate the short range ordering and coordination structures. He found that the short range structures in a-IGZO are almost identical to that of crystalline IGZO, and that the conduction band minimum is composed primarily of In 5s orbitals.

1.6. Amorphous Oxide Semiconductors

Prior to 1996, only one transparent conducting material was investigated in its amorphous state: a-In_2O_3.[35, 36] In 1996, Hosono et. al. proposed that many of the crystalline materials used for transparent conducting oxides would retain their high mobility even if they were fabricated in an amorphous state.[37] It is now known that a wide range of heavy metal cations, such as In, Ga, Sn, Zn, Cd, etc., retain their high electron mobilities after they have been alloyed into amorphous oxides. Additionally, by controlling the processing conditions, the carrier concentration can be varied from 10^{15} cm^{-3} to around 10^{20} cm^{-3}. This enables the use of amorphous oxides in both conductive applications and semiconducting applications. The band gaps of the amorphous oxide semiconductors (AOSs) vary significantly depending on the cations used, from around 2 eV to 3.8 eV, opening the door to high performance fully transparent electronic devices (all visible light photons have energy less than 3.1 eV). The first fully transparent TFT was fabricated around a crystalline ZnO channel layer in 2003 by Hoffman et. al.[38], however the channel mobility was barely better than that of a-Si:H: around 1 $cm^2V^{-1}s^{-1}$. Further development of the AOSs led to a completely transparent TFT built around a ZTO channel layer which yielded mobilities up to 50 $cm^2V^{-1}s^{-1}$.[39] So, while the mobility of AOS's are not as good as those of doped crystalline silicon (c-Si) (typically at least 200 $cm^2V^{-1}s^{-1}$), they are much higher than those of a-Si:H. The transparency of these materials is illustrated in Figure 1.5, adapted from Chiang et. al.[39], which is the

transmission through an entire transparent thin film transistor built around a ZTO channel layer.

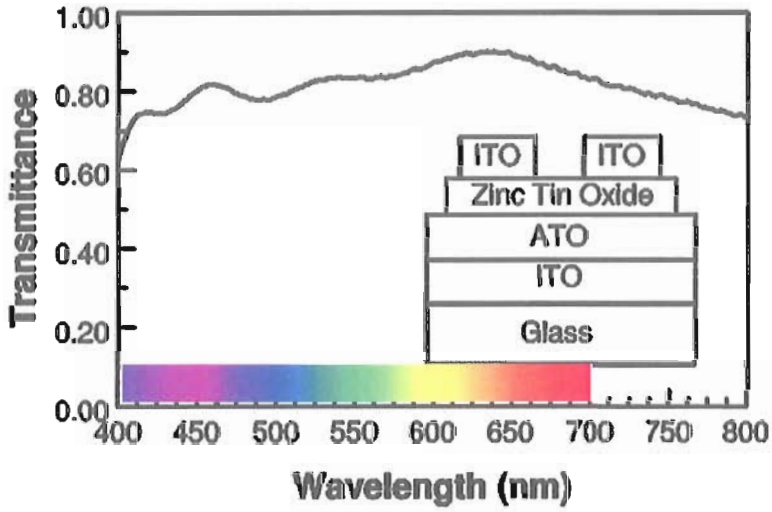

Figure 1.5: Transmittance of fully transparent thin film transistor with ZTO channel layer.

Anwar[40] has investigated the optical absorption characteristics of several amorphous oxide semiconductors in the $ZnO:SnO_2$ family. Through direct optical absorption measurements, he found very broad Urbach edges in the majority of the samples, from 170 meV to 230 meV. Substrate temperature had a large effect on the properties of the evaporated films: increased substrate temperature led to a decrease in the optical band gap, which was attributed to impurity scattering. It was also found that the optical band gap increased as the film thickness was increased up to 200 nm. Tin was identified as a source of electrons which increased the carrier density in the films.

1.7. Zinc Tin Oxide and Indium Gallium Zinc Oxide

The two AOSs on which I have focused, zinc tin oxide (ZTO) and indium gallium zinc oxide (IGZO) both have band gaps between 3.3 and 3.6 eV, and are currently being developed for transparent electronics applications. Transistors based on ZTO and IGZO show very good device characteristics, with turn-on voltages near 0 V and on to off current ratios of $> 10^6$. Displays are already being produced which are fabricated around AOS TFTs. However, the properties of these devices are very dependent on the growth and annealing conditions which means they need to be well characterized and understood at a basic level. For example, transistors with amorphous ZTO as the channel layer perform best after a 600 °C post-deposition anneal. Table 1.1, adapted from Chiang[39], illustrates the increase in device performance (high mobility and turn-on voltage near 0 V) with increasing anneal temperature up to the point where the ZTO was observed to start crystallizing, 650 °C.

Table 1.1: The transistor performance increases as the post-deposition anneal temperature increases up to the crystallization temperature of 650 °C.

T_{anneal} (°C)	100	200	400	600	800
μ ($cm^2V^{-1}s^{-1}$)	25	25	30	26	6
V_{on} (V)	-5	-5	-1.5	.1	-3

While these preliminary results (good transistor devices) are very promising, and encourage further exploration into the development of these devices, the transistor performance is currently not good enough to realize the full potential of these materials. Modeling transistor performance to learn about basic materials properties has been actively pursued and can be useful. However such device characteristics are typically embedded within three levels of integration of the fundamental material properties, so that a lot of the underlying physics can be obscured or misinterpreted.[41] As was learned from the investigations into amorphous silicon, a fundamental understanding of the density of states requires simplified device structures and specialized experiments.

At the same time, while there are many similarities between amorphous silicon and the amorphous oxide semiconductors, key differences must also be kept in mind. Indeed, there are sharp distinctions already. A notable example is the temperature dependent hall mobility in a-Si:H, which changes sign at low temperatures.[42] The temperature dependence of the hall mobility of at least several amorphous oxide semiconductors including IGZO has been investigated by Narushima,[43] and Hosono[37] with no indication of sign change. This can be understood by considering the mean free path of an electron in these materials as indicated from the mobilities. In the case of AOSs, the mean free path is much larger than the bond length, while in amorphous silicon the mean free path is at most equal to, and usually less than the bond length. This makes transport in amorphous silicon more susceptible to structural disorder and much more difficult to understand.[44]

In order to simplify the device structure and thus hopefully gain more insight into the fundamental structure of these materials we have focused our investigation primarily on metal-insulator-semiconductor (MIS) capacitors, rather than transistor (triode) structures. Such MIS capacitors allow us to investigate not only the relevant junction in the transistors, the interface between the insulator and the semiconductor, but also the bulk of the semiconductor independent of the source-drain interactions.

1.8. Summary

Amorphous oxide semiconductors are a new class of materials which are very promising for the development of new electronic devices, particularly those involving transparent electronics. The electronic properties of AOSs exceed those of hydrogenated amorphous silicon, the current material of choice for thin-film transistors. Extensive investigations into the basic structure and processes of amorphous silicon have allowed this material to become heavily used in many different applications. This dissertation will attempt to understand the fundamental structure of the density of states within the mobility gap of the AOSs zinc tin oxide (ZTO) and indium gallium zinc oxide (IGZO). While there are differences between amorphous silicon and AOSs, we can understand much more about the new disordered material by drawing upon what has been learned from amorphous silicon. An understanding of the defect structure of AOSs will allow the full potential of these materials to be reached.

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CHAPTER II

DEVICE FABRICATION AND STRUCTURE

2.1. Fabrication Methods

All samples discussed here were fabricated either at Oregon State University or at the University of Braunschweig in Braunschweig, Germany. Unless noted otherwise, samples consisted of a commercially available heavily doped Si substrate capped with a SiO_2 insulating layer on which the amorphous oxide semiconductor was deposited. The samples were then finished with either a gold or aluminum thermally evaporated top contact. This top contact was designed to be semi-transparent to enable electro-optical characterization techniques. For a good overview of thermal oxidation techniques used to grow the SiO_2 and metal evaporation techniques, consult Sze.[1] A brief discussion of the techniques used to fabricate the amorphous oxide semiconductor layers will be presented here.

Rf-Sputtering

All amorphous oxide semiconductor layers deposited at Oregon State University were fabricated in a custom system fabricated and designed by Chris Tasker and Hai Chiang. Details of the tool can be found in Chiang's thesis.[2] Sputtering in general refers to the process in which atoms are removed from a compressed target by impinging ions. The ejected atoms then travel from the target to the substrate, on which they nucleate, to form thin films. The sputtering target and the sample are kept in a controlled atmosphere which depends on the material being fabricated. In this case, the environment was mixed 90% Ar and 10% O_2.

In the case of conductive substrate, a DC bias between the substrate and target is sufficient to accelerate ions produced by the interaction of cosmic rays with the ambient gas and start the sputtering process. However, this does not work with insulating substrates (as are used here) and an additional AC voltage must be used to sustain the discharge. The most typical frequency of this AC voltage is 13.56 MHz, although other frequencies can be used.

Post-Deposition Anneal

High temperature post-deposition anneals are often used to control the structure of thin films. Anneals were carried out at Oregon State University in either an AET Thermal Processing, Inc. Rapid Thermal Processing System or a Barnstead Thermolyne box furnace. Temperatures ranged from 300 °C to 600 °C with ramp rates near 10 °C/sec. Anneals were performed in air, and typically lasted 1 hour.

Pulsed Laser Deposition (PLD)

Pulsed laser deposition (PLD) is a process in which a high power laser beam is focused onto the target which is to be evaporated.[3] The constituent atoms of the target form a plume above the target and then nucleate on the substrate. The process can either be carried out under ultra-high vacuum or in the presence of an ambient gas beneficial to the film being deposited, such as oxygen, as is the case for the materials discussed here. Further information about the specifics of the PLD system employed at the University of Braunschweig are discussed by Görrn elsewhere.[4] AOS devices deposited by PLD have very good device characteristics without needing a post-deposition anneal, pushing the overall fabrication temperature as low as 150 °C.

2.2. Scherrer Equation

The Scherrer equation is used to help determine the structure of a material from x-ray scattering experiments.[5] Crystalline materials will typically produce very sharp rings in the scattering data, and while amorphous materials will also produce rings, they will typically be very fuzzy and smeared out. The Scherrer equation adds some quantification to the "fuzziness" of the rings to estimate the largest grain size possible to produce the rings. Analysis of the ZTO thin films prepared in a manner similar to that of the devices analyzed here reveals that if there are nanocrystallites present, they are no larger than 5 nm. In contrast, ZTO films subjected to anneal temperatures above 650 °C exhibited a multiplicity of sharp peaks, indicating that the film was becoming much more crystalline.[6]

2.3. Device Structures

The devices examined using junction capacitance methods were all fabricated in metal-insulator-semiconductor (MIS) structures. These MIS structures typically consisted of a degenerately doped Si substrate, ~ 100 nm insulator (usually SiO_2), and then 1-2 μm of semiconductor. The devices were then finished with a semi-transparent Au or Al top contact. These structures are illustrated below in Figure 2.1. It is crucial that the Si substrate has a very high level of doping, around 10^{18} cm^{-3} is usually sufficient. Doping

levels closer to 10^{16} cm^{-3} can influence some of the characterization techniques discussed here, in particular the transient photocapacitance spectroscopy method.

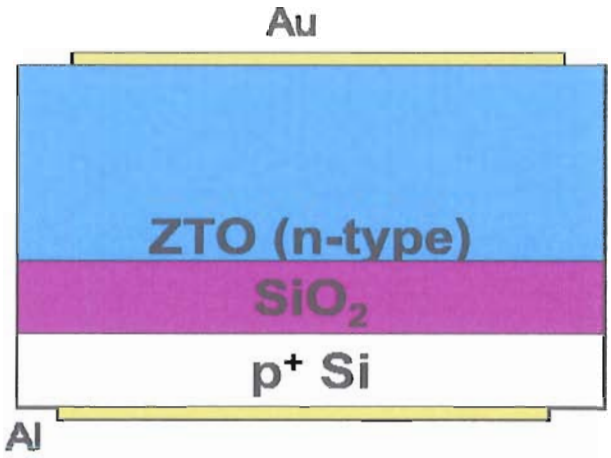

Figure 2.1: Metal-insulator-semiconductor (MIS) device structure used for junction capacitance measurements.

The capacitive characterization methods employed require a semiconductor junction in the device. While one-sided p^+-n or Schottky barriers are the most simple to investigate, there is no material available at this time which produces a robust rectifying contact with the amorphous oxide semiconductors. This is actually beneficial for investigating the issues relevant to transistor device performance with these materials though, as the MIS structure is one key part of the thin film transistor. This structure allows us to examine electronically active defect states at the insulator-semiconductor interface and in the bulk of the semiconductor which may be affecting transistor performance.

Modulated photocurrent spectroscopy measurements were carried out both on coplanar and sandwich (metal-semiconductor-metal) geometry samples. The coplanar samples all had a length/width ratio of 10:1 and semiconductor thicknesses ranging between 50 nm and 200 nm. The samples were fabricated on ESR grade quartz substrates and finished with aluminum contacts. Devices were then subjected to post-deposition thermal anneals ranging from 300 °C to 500 °C. The ESR grade quartz substrates proved necessary for these experiments as the gated Si/SiO_2 substrates influenced the MPC results dramatically. Although the coplanar geometry samples provided meaningful results about the nature of the conduction band tail, the conduction path is somewhat ambiguous. There is no way to determine whether the primary conduction path is through the bulk of the semiconductor, along the surface of the semiconductor which is exposed to air, or along the semiconductor-insulator interface. The sandwich geometry samples resolve this dilemma by forcing the conduction path to be only in the bulk of the semiconductor. These samples consisted of an indium tin oxide (ITO) back contact, a 1.2 μm ZTO layer, and then an aluminum top contact.

2.4. Notes

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CHAPTER III

MEASUREMENT TECHNIQUES

3.1. Introduction

A wide range of measurement methods exist to characterize semiconducting materials. However, measurement techniques applied to these materials must be carefully considered, not just applied blindly, in order to obtain meaningful results. For example, a resistivity measurement on a semiconductor using a two-point probe will yield wildly different (and incorrect) results, whereas the four-point resistivity measurement will generally provide a good idea of the intrinsic properties of the material. In order to determine the density of states within the mobility gap of amorphous zinc tin oxide (ZTO) and indium gallium zinc oxide (IGZO), a variety of methods were utilized. Several methods based around the junction capacitance of a device will be discussed. Junction capacitance methods account for a large portion of our map of the electronic structure within the band gap of these amorphous oxide semiconductors (AOSs) with the

remaining piece completed through the use of modulated photocurrent spectroscopy (MPC).

Junction capacitance measurements have proven extremely useful for investigating the fundamental properties of semiconducting materials and devices.[1-4] A depletion region, from which the capacitance stems, is present in nearly any sandwich geometry semiconductor device that contains a junction, for example photovoltaic solar cells or the metal-insulator-semiconductor (MIS) devices discussed here. A good overview of admittance spectroscopy, or junction capacitance as a function of frequency and temperature, was provided by Losee[5]. Cohen and Lang calculated the AC and thermal dynamic response of a Schottky barrier[6] for a semiconductor containing broad distributions of defect levels within the mobility gap, thus demonstrating the usefulness of deep level transient spectroscopy (DLTS) in characterizing amorphous semiconducting materials. A wide range of optical techniques are available for characterizing the density of states within the band-gap including direct absorption methods, photothermal deflection spectroscopy[7], and the constant photocurrent method (CPM)[8]. While these methods have strengths and weaknesses, transient photocapacitance spectroscopy (TPC) has shown superior usefulness in characterizing optically active defects in semiconductor devices with a very large dynamic range, sensitivity to carrier type, and ability to effectively probe buried junctions[9].

The aforementioned techniques are all useful in characterizing states that are usually filled with the majority carriers (electrons in n-type devices such as amorphous oxide semiconductors). However, additional measurements are required to probe states that are usually empty, or above the Fermi energy. These states typically have a very large effect on the conduction mechanism. Modulated photocurrent spectroscopy[10] and space-charge-limited current[11] were employed to gain understanding about the conduction mechanism in these materials. Combining all of these techniques can yield a thorough understanding of the structure of the density of states within the mobility gap of amorphous oxide semiconductors.

3.2. Junction Capacitance Overview

The measured capacitance of a metal-insulator-semiconductor (MIS) device can be, in the simplest manner, considered as two capacitors in series. The capacitance of the first, the insulating layer, will be largely independent of any varying measurement condition, for example temperature or applied voltage bias. In contrast, the second capacitance, due to the depletion layer in the semiconductor, will be very dependent on those same measurement conditions and thus provide a large amount of information about the material properties of the semiconductor. Understanding how the measured capacitance changes with respect to the measurement conditions is necessary in order to interpret our results.

A rudimentary energy band diagram for a MIS capacitor is shown in Figure 3.1, showing the wide gap insulating layer and the n-type semiconducting layer with a band of deep defects an energy depth E_d from the conduction band, E_C. The intrinsic depletion region is formed because of the requirement that the material is charge neutral: the Fermi energy must remain constant throughout the material thus the conduction and valence bands are bent. Charges of opposite polarity accumulate at the metal-insulator interface and at the edge of the depletion region in the semiconductor, resulting in a dipole. This creates an electric field which sweeps carriers to the edge of the depletion region, marked W. The amount that the bands are bent is called the interface potential.

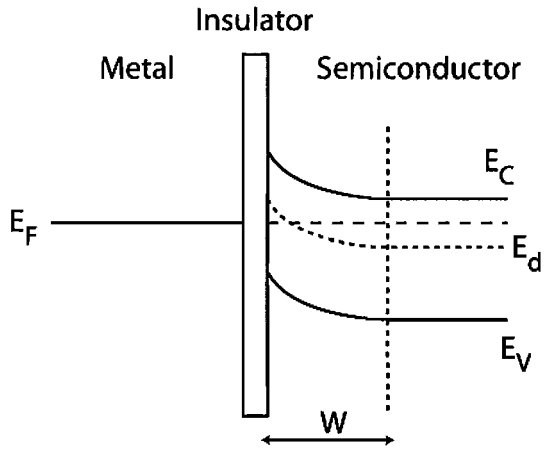

Figure 3.1: Energy band diagram of an n-type MIS capacitor including a band of defects in the upper half of the band gap.

In order to begin interpreting the information provided by junction capacitance measurements, we must first discuss differential capacitance, defined as

$$C = \frac{dQ}{dV}$$

where dQ is the change in the amount of charge responding as a result of a change in the applied potential dV. The charge response in the sample is limited by the characteristic energy of the measurement, set by the frequency and temperature, and the response time of carriers trapped in the deep defect states. The characteristic energy of the experiment, E_e, can be written as

$$E_e = k_B T ln\left(\frac{\omega}{2\pi\nu}\right)$$

In this expression, T and ω are the measurement temperature and angular frequency, respectively, and ν is the thermal emission prefactor (with units of s^{-1}) of states within the mobility gap. The value of ν can be related to materials properties through detailed balance arguments: When $E_d = E_F$, the carrier capture and escape times must be equivalent, as the probability that the state is occupied is equal to ½. In doing this, one obtains the following expressions for the emission (τ_d) and capture (τ_c) times:

$$\frac{1}{\tau_d} = \nu e^{-\frac{E_d}{kT}}$$

$$\frac{1}{\tau_C} = N_C \langle v \rangle \sigma_n e^{-\frac{E_F}{kT}}$$

Setting these two equations equal when $E_d = E_F$ then yields

$$\nu = N_C \langle v \rangle \sigma_n$$

where N_C is the effective density of states in the conduction band, $\langle v \rangle$ is the average thermal velocity, and σ_n is the electron capture cross-section.

Now the capacitance response for the deep states can be calculated for an arbitrary distribution of defects within the band-gap. We start with Poisson's equation in the direction perpendicular to the junction (we assume uniformity in the plane of the junction)

$$\frac{d^2\psi}{dx^2} = -\frac{\rho}{\varepsilon}$$

where ψ is the potential within the depletion region, ρ is the charge density, and ε is the dielectric constant of the semiconductor. Far from the junction, ψ is defined to be 0. The

additional knowledge that there will not be any band-bending far from the junction (or $d\psi/dx = 0$ as well), allows us to solve for the potential at the interface:

$$\psi(0) = -\int_0^\infty x\frac{\rho}{\epsilon}dx$$

A small, additional, voltage applied across the junction will perturb the potential at the interface and result in a small change in the charge density within the depletion region.

$$\delta V = -\int_0^\infty x\frac{\delta\rho}{\epsilon}dx$$

The total amount of charge responding to this small applied bias within the measurement area A is now

$$\delta Q = A\int_0^\infty \delta\rho(x)\,dx$$

Thus the differential capacitance for any distribution of states within the band gap responding to a small change in applied potential is just

$$C = \frac{dQ}{dV} = \frac{\epsilon A\int_0^\infty \delta\rho(x)\,dx}{\int_0^\infty x\delta\rho(x)\,dx} = \frac{\epsilon A}{\langle x\rangle}$$

Where <x> is the first moment of charge response

$$\langle x \rangle = \frac{\int_0^\infty x\delta\rho(x)\,dx}{\int_0^\infty \delta\rho(x)\,dx}$$

In the case of a material without any defects responding to the applied voltage within the depletion region, <x> will just be equal to the depletion width W and the junction capacitance reduces to C=εA/W. A material such as illustrated in Figure 3.1 will have an additional response at x_e, where E_d crosses E_F, as shown in Figure 3.2.

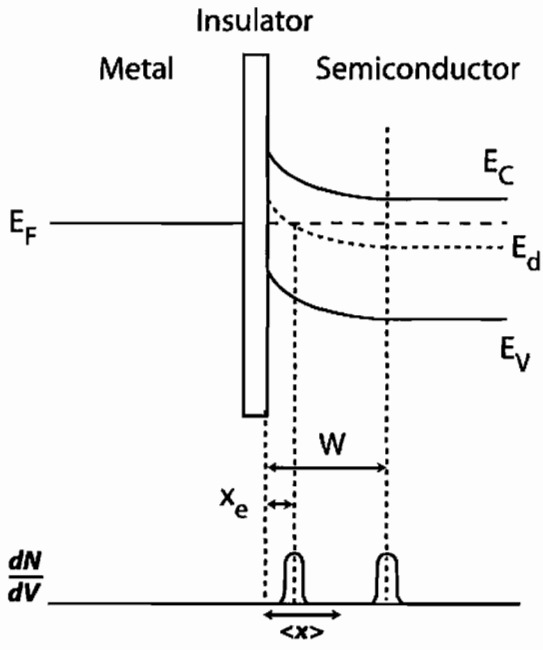

Figure 3.2: Materials with deep defects within the band gap will have an additional charge response at the point where the defect energy crosses the Fermi energy.

The first moment, $\langle x \rangle$, now becomes

$$\langle x \rangle = \frac{N_D x_e + nW}{N_D + n}$$

N_D is the density of deep defects responding and n is the free carrier density of the sample, responding at the edge of the depletion region W. The first moment, $\langle x \rangle$, is now essentially a weighted average of where the charges are responding in the sample.

3.3. Measuring Capacitance

As was previously discussed, the differential capacitance measures the change in charge response due to a change in the applied potential, dQ/dV. The change in charge response can then be detected by measuring the current response of the sample, $I = dQ/dt$. MIS devices can be modeled in the most simple way as a circuit consisting of a capacitor (C_{ox}) (the insulating layer) in series with a capacitor and a resistor in parallel (the semiconducting layer), as shown in Figure 3.3.

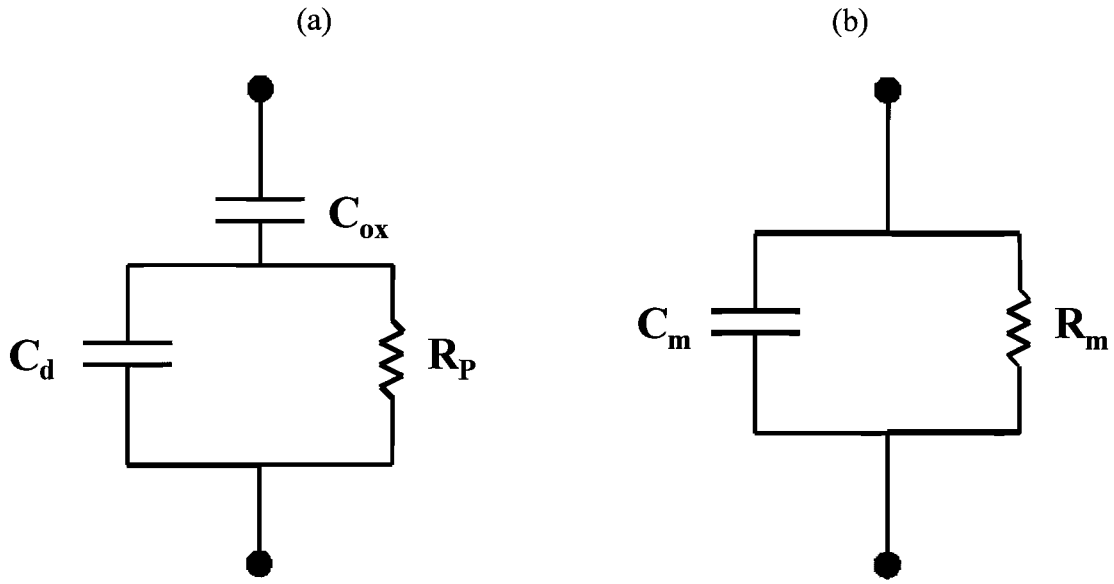

Figure 3.3: (left) Equivalent circuit model of MIS device consisting of a capacitor representing the insulating layer (C_{ox}) in series with the depletion capacitance of the semiconductor (C_d) and the resistance (R_P) which represents losses from traps. (right) Circuit measured by lock-in amplifier.

A lock-in amplifier differentiates between the in phase and out of phase responses, thus the data collected actually represents the circuit in Figure 3.3(b). In most analysis presented here, the oxide capacitance only represents an offset in the calculated effective width which can be subtracted away if necessary. Solving for the current response of this (measured) circuit to an applied oscillating voltage bias $V=V_0*\cos(\omega t)$ clearly shows the phase difference between the capacitive and conductive responses, yielding

$$I = \frac{V_0}{R_m}\cos(\omega t) - V_0 \omega C_m sin(\omega t)$$

For the junction capacitance measurements presented here, a Stanford Research Systems SR850 lock-in amplifier was used. This lock-in amplifier has an internal oscillator for providing the reference AC signal between 1 Hz and 100 kHz. The current pre-amplifier used in these experiments was a Stanford Research Systems 570. The general experimental setup is sketched in Figure 3.4. The temperature of the measurement was controlled with either a Linkam 340 cold stage or with nitrogen gas flow-through dewars. Both of these temperature control systems allow the measurement temperature to vary between 80 K and 400 K, spanning a wide range of emission energies.

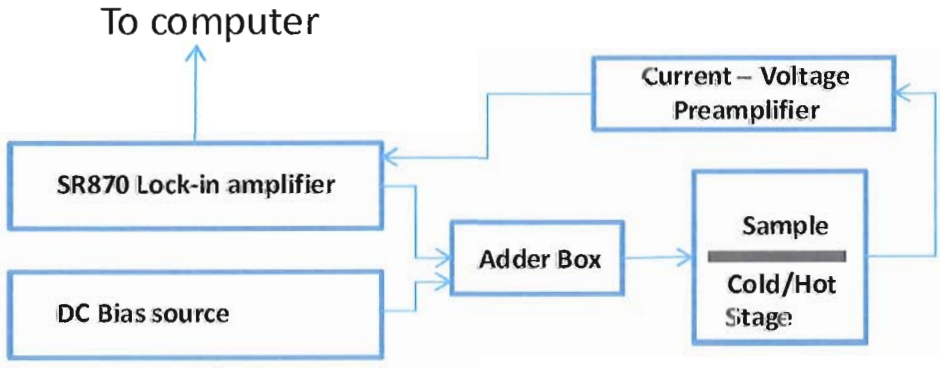

Figure 3.4: General experimental setup for measuring the capacitance and conductance as a function of frequency and temperature.

3.4. Admittance Spectroscopy

Admittance spectroscopy examines the complex response of a sample to an applied AC signal as a function of both frequency and temperature. A lock-in amplifier is used to distinguish between the in-phase and out-of-phase components of the response. The in-

phase and out-of-phase components are related by the Kramers-Kronig relation as the capacitance and the conductance (divided by the frequency, G/ω). Two terminal devices, such as the MIS capacitors, are thus the easiest to interpret, as the sample can be thought of as simply a complicated, bias-dependent capacitor.

Admittance spectroscopy provides information both about the free carriers and the deep defects in a material. By controlling the frequency and temperature of the measurement, one defines a characteristic energy of the experiment, $E_e = k_B T \ln(\nu/\omega)$, where ν is the thermal emission prefactor and ω is the frequency. When this emission energy is low, such as at either low temperatures or high frequencies or both, only the free carriers in the sample can respond. When the emission energy is high, both the free carriers and electron traps deeper in the band gap can respond. The transition between these two situations is characterized by an observed step in the capacitance response, from a low capacitance value at high frequencies/low temperatures to a high capacitance value at high temperatures/low frequencies. An example of this step is shown in Figure 3.5 below.

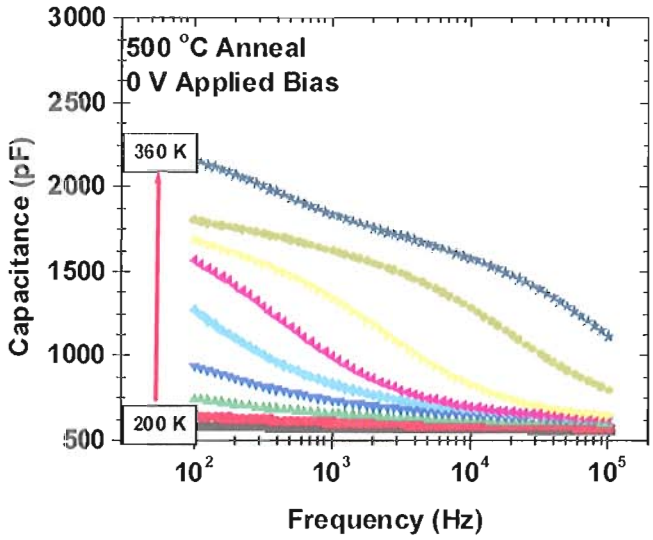

Figure 3.5: Admittance spectrum showing the step transition as a deep carrier begins to respond. At high frequencies and low temperatures, only the free carriers can respond, while at low frequencies and high temperatures all carriers can react to the AC signal.

Correspondingly, there will be peaks in the conductance spectra at the inflection point of the capacitive step. Activated processes such as this, where the system must overcome an energetic barrier, are typically regarded as below:

$$X = X_0 e^{\frac{-E_A}{k_B T}}$$

E_A is the energy barrier, X_0 is the prefactor of the process, and T is the measurement temperature. The temperature dependence of the system is utilized to find the activation energy: Either the peaks in conductance or the inflection points in capacitance can then

be plotted in an Arrhenius plot (Figure 3.6) to determine the activation energy of the deep level.

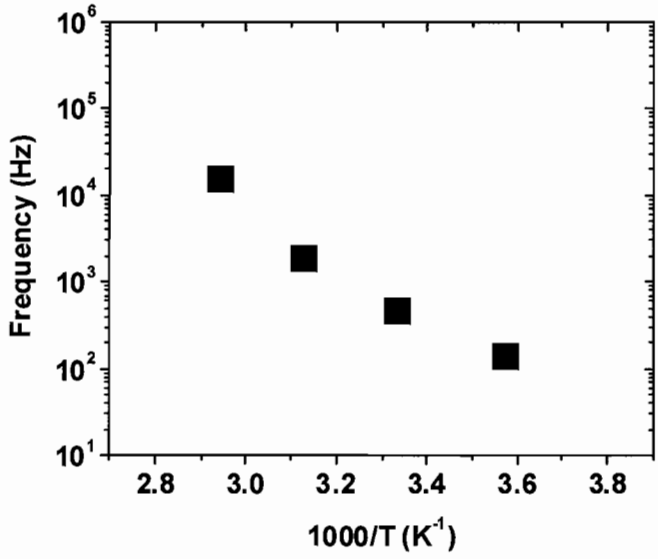

Figure 3.6: Arrhenius plot of the inflection point in a capacitance step used to determine the activation energy of the trap. Identical results could be obtained by using the peaks in the conductance vs. frequency data as well.

While admittance spectroscopy is useful in determining the activation energy of a step, it does not provide any information about the spatial location of the defect within the device. Electron traps located at the junction interface can respond in a manner almost identically to traps located in the bulk of the semiconductor. That is, as the interface defects begin to respond as the characteristic energy of the measurement increases, the effective width measured by the capacitance decreases exactly as if a bulk defect were responding. In order to differentiate between these two situations, admittance spectra must be taken under several different DC biases. If the activation energy one obtains

under different biases is the same, then the deep level is likely in the bulk of the semiconductor. If the activation energy changes with different applied DC biases, then the defect is likely situated at the junction interface and the activation energy that is being measured is the potential at the interface. Figure 3.7 is a sketch of how the measured activation energy may change if the states responding are located at the insulator-semiconductor interface.

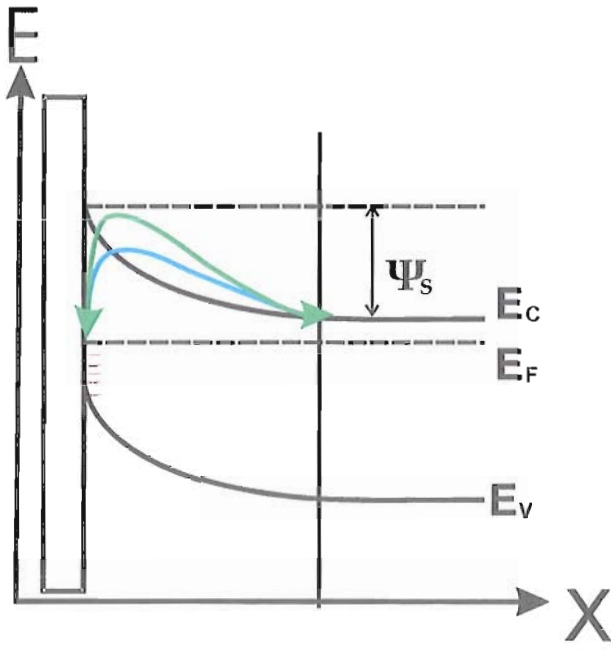

Figure 3.7: Admittance spectroscopy performed under varying DC biases can help reveal the location of the states responding in a MIS device. If the measured activation energy changes as the DC bias changes then the state is most likely located at the insulator-semiconductor junction, and the activation energy is representative of the interface potential Ψ_s.

Admittance spectroscopy was performed on a wide range of samples as a first step in the characterization procedure. In some cases, the defect level appeared to be bias-independent, suggesting that the defect level is located in the bulk of the semiconductor. In other samples, the activation energy of the defect was very bias dependent, suggesting that the defect level was located at the insulator-semiconductor interface.

If the capacitance step is determined to stem from a state at the interface, a simple model can be used to estimate the area density of the defects. The basis of the method is very similar to that of a bulk defect: at high frequencies and low temperatures we assume that the capacitance is only due to the free carriers at the edge of the depletion region, and at low frequencies and high temperatures we are seeing the response of the trapping states as well as the free carriers. A simple circuit model is shown in Figure 3.8, with the

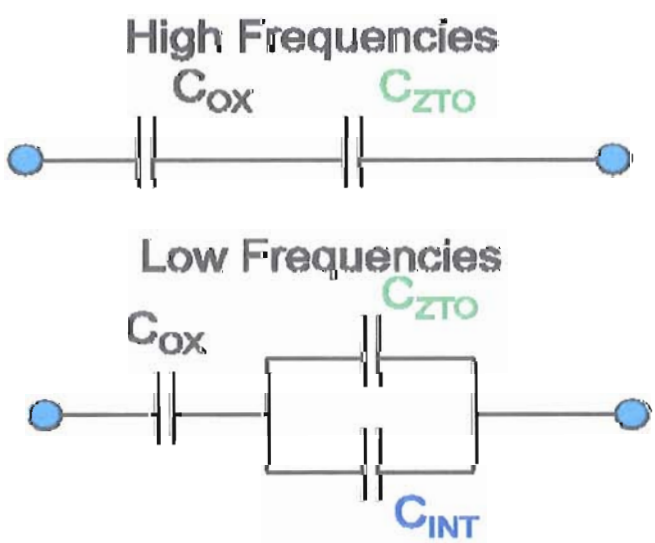

Figure 3.8: Circuit model for estimating the area density of states at the interface from the capacitance step.

interface capacitance added in parallel for low frequencies. As long as the oxide capacitance is known, the interface density of states can be isolated and the interface density of states estimated from the high frequency (C_{HF}) and low frequency (C_{LF}) capacitances.

$$qD_{it} \approx C_{int} = \left(\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_{ox}}\right)^{-1}$$

For more detail, I will outline the method as presented by E. H. Nicollian[12] below. Terms with the subscript "s" refer to the semiconductor in question, and the subscript "it" refers to the interface trap. Start with the differential capacitance at low frequencies:

$$C_{LF} = \frac{-d(Q_{it} + Q_s)}{dV_G}$$

Gauss' law sums and balances the charge present around the interface.

$$Q_G = C_{ox}(V_G - \psi_s) = -Q_{it}(\psi_s) - Q_s(\psi_s)$$

Note that if there were no charges present at the interface, any small change in the charge (bias) on the gate would be completely reflected by the charge in the semiconductor. However, with the interface charges present, a larger change in the gate bias is required

for the same change in the charge in the semiconductor. This leads to broadened transitions in the transistor IV characteristics as well.

For a slow change in the gate bias, and defining the differential interface and semiconductor capacitances as $C_{it} = -dQ_{it}/d\psi_s$ and $C_s = -dQ_s/d\psi_s$ we obtain

$$C_{ox}dV_G = [C_{ox} + C_{it}(\psi_s) + C_s(\psi_s)]d\psi_s$$

Now we obtain the expression for the low frequency capacitance, equivalent to adding the interface traps in parallel with the bulk response of the semiconductor:

$$C_{LF} = \frac{-d(Q_{it} + Q_s)}{dV_G} = \frac{-d(Q_{it} + Q_s)}{d\psi_s}\frac{d\psi_s}{dV_G} = \frac{-d(Q_{it} + Q_s)}{d\psi_s}\frac{C_{ox}}{C_{ox} + C_{it}(\psi_s) + C_s(\psi_s)}$$

$$= \frac{(C_s + C_{it})C_{ox}}{C_{ox} + C_{it} + C_s}$$

While this method will come in handy for estimating the density of states at the interface between the semiconductor and the insulator, it does not account for deep states within the bulk of the semiconductor. Thus this derivation is somewhat limited for providing actual defect densities when there may be both interface and bulk defect densities.

3.5. Spatially Sensitive Capacitance Profiling Methods

Two spatially sensitive capacitance profiling methods were used to determine the free carrier densities and deep defect densities in the amorphous oxide semiconductors. Capacitance vs. DC bias measurements, as outlined in semiconductor texts such as Sze[13], are based on the assumption that there are no deep states within the gap responding. This makes the C-V profile a sum of the free carriers, deep states, and any states responding at interfaces within the device.

An applied potential across a junction, δV, can be written as a change in the charge density within the junction as

$$\delta V = \frac{1}{\varepsilon}\int_{W_1}^{W_2} x\rho(x)dx \approx \frac{1}{\varepsilon} W\rho(W)\delta W$$

Where ε is the dielectric constant of the material. Rearranging to solve for the charge density gives:

$$\rho(W) = \frac{\varepsilon}{W}\frac{\delta V}{\delta W}$$

The capacitance of a parallel plate capacitor is:

$$C = \frac{\varepsilon A}{W}$$

Differentiating with respect to the depletion width W:

$$dC = -\frac{\varepsilon A}{W^2} dW$$

And then combining to solve for the change in capacitance with respect to a change in applied voltage:

$$\frac{dC}{dV} = -\frac{C^3}{\epsilon A^2 \rho(W)}$$

Finally yields an expression for the charge density responding to the potential:

$$\rho(W) = -\frac{C^3}{\epsilon A^2 \frac{dC}{dV}}$$

Thus the charge density that is responding to the DC bias reflects the number of carriers present at that spatial position.

Drive Level Capacitance Profiling

Another spatially sensitive profiling method is drive level capacitance profiling, DLCP. DLCP improves on the standard C-V profiling defect measurement method by adding an AC signal of varying magnitude to each of the DC biases, then examining the capacitive response of the sample to the magnitude of the AC signal at each DC bias. Thus ONLY

the carriers that can respond at the single characteristic energy of the measurement are included in the calculation. By varying the frequency and temperature of the measurement, differentiation between free carriers, deep trapping states, and states at interfaces becomes possible.

Drive Level Capacitance Derivation

Here the basis of drive level capacitance profiling will be outlined, as it is also presented by Heath et al.[2] We start with Poisson's equation for 1-D:

$$\frac{d^2\psi}{dx^2} = -\frac{\rho}{\varepsilon}$$

Where ψ is the electrostatic potential, ρ is the charge distribution, and ε is the dielectric constant in the material. By using the boundary conditions that far from the junction (x=0) ψ=0 and also $d\psi/dx=0$, the potential at the interface can be written as

$$\psi_0(0) = \int_0^\infty x\frac{\rho_0}{\varepsilon}dx = \int_0^{x_e} x\frac{\rho_0}{\varepsilon}dx + \int_{x_e}^\infty x\frac{\rho_0}{\varepsilon}dx$$

Then with the addition of a small voltage, δV, x_e is perturbed to $x_e+\delta x$, such that

$$\psi(0) = \int_0^{x_e} x\frac{\rho_0}{\varepsilon}dx + \int_{x_e}^{x_e+\delta x} x\frac{\rho_e}{\varepsilon}dx + \int_{x_e+\delta x}^\infty x\frac{\rho_0(x-dx)}{\varepsilon}dx$$

If $\rho(x)$ is spatially uniform, then $\rho(x) \approx \rho_0(x\text{-}dx)$

Continuing then

$$\psi(0) = \int_0^{x_e} x\frac{\rho_0}{\varepsilon}dx + \frac{\rho_\varepsilon}{2\varepsilon}((x_{e+} + dx)^2 - {x_e}^2) + \int_{x_e+\delta x}^{\infty} x\frac{\rho_0(x-dx)}{\varepsilon}dx$$

Investigating the last term a bit, and letting $y = x - \delta x$

$$\int_{x_e+\delta x}^{\infty} x\frac{\rho_0(x-dx)}{\varepsilon}dx = \int_{x_e}^{\infty}(y+\delta x)\frac{\rho(y)}{\varepsilon}dy$$

Now, recognizing that the first term in the equation for $\psi(0)$ can be combined with the transformed term above,

$$\psi(0) = \psi_0 + \frac{\rho_e}{2\varepsilon}((x_e + \delta x)^2 - x_e^2) + \int_{x_e}^{\infty}\delta x\frac{\rho(y)}{\varepsilon}dy$$

Then,

$$\delta V = \psi(0) - \psi_0 = \frac{\rho_e}{2\varepsilon}((x_e + \delta x)^2 - x_e^2) - \delta x F_e$$

Where F_e is the electric field at x_e. One can then solve for δx, which gives

$$\delta x = \left(\frac{\varepsilon}{\rho_e} F_e - x_e\right)\left[1 - \sqrt{1 + \frac{2\rho_e \varepsilon \delta V}{(\varepsilon F_e - \rho_e x_e)^2}}\right]$$

Expanding the term within the square root yields a quadratic expression (neglecting the insignificant higher order terms) in δV, which can be turned into the amount of charge responding at x_e.

$$dQ = Ap_e \delta x = \frac{-A\rho_e \varepsilon}{(\varepsilon F_e - \rho_e x_{e)}} \delta V + \frac{-A{\rho_e}^2 \varepsilon^2}{2(\varepsilon F_e - \rho_e x_e)^3} \delta V^2$$

Then, assigning the coefficients C_0 and C_1 to the leading factors, we obtain the expression

$$C = \frac{dQ}{dV} = C_0 + C_1 \delta V + \ ...$$

And after some re-working, the number of carriers responding to the applied δV is

$$N_{DL} = \frac{\rho_e}{q} = -\frac{C_0^3}{2q\varepsilon A^2 C_1}$$

The drive level density is equal to the amount of charge responding between the Fermi energy and the emission energy.

$$N_{DL} = n + \int_{E_C - E_e}^{E_F} g(E)dE$$

In order for the emission depth, x_e, to remain constant, the maximum (forward) applied voltage must remain constant. Thus during the measurement, the amplitude of the DC bias must be adjusted simultaneously with the AC signal. This is illustrated in Figure 3.9, showing the AC signals added to a 0.5 V DC reverse bias.

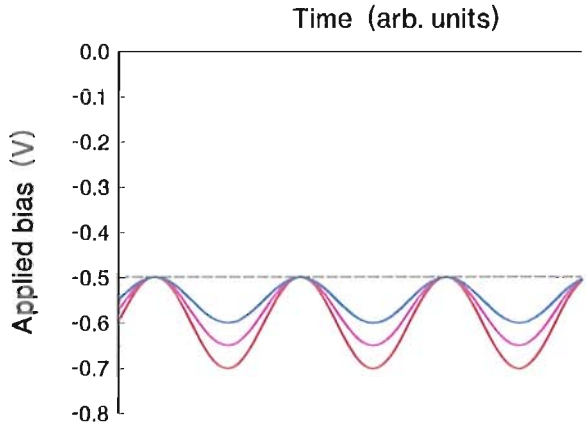

Figure 3.9: The amplitude of the DC bias must be adjusted for each value of AC signal so that the maximum forward bias is kept constant throughout the DLCP measurement. This is necessary so that the maximum emission depth is kept constant throughout the measurement.

3.6. Transient Photocapacitance Spectroscopy

Transient photocapacitance spectroscopy (TPC) is a sub-band-gap optical absorption-like technique used to obtain information about the optically active states within the mobility gap of disordered materials. By analyzing the transient capacitance response after a bias filling pulse with and without sub-band-gap monochromatic light on the sample, a signal which is proportional to an integral over the density of states within the gap is obtained. TPC can effectively probe the density of states within the mobility gap of completed devices and buried semiconductor junctions. This makes it very useful for investigating structures such as are used in photovoltaic solar cells and also MIS capacitors.

The general form for optical transitions is shown in the equation below:

$$P(E_{opt}) = \int |\langle i|ex|f\rangle|^2 g_{occ}(E) g_{unocc}(E + E_{opt}) dE$$

There are two possible transitions for an n-type material: Either from an occupied defect into the conduction band or from the valence band into an unoccupied defect. These transitions are illustrated below in Figure 3.10. Note that transitions always involve at least one delocalized state. Unless the semiconductor is degenerately doped (when the localized wavefunctions of the discrete defect states begin overlapping), transitions between two defect states are not possible.

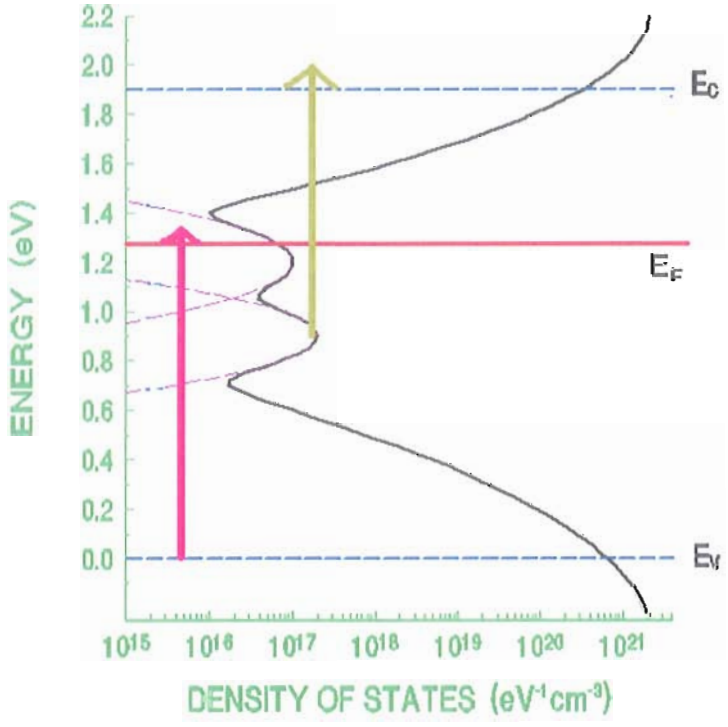

Figure 3.10: Possible optical transitions in a semiconductor. All transitions occur between an occupied state and an unoccupied state. Transitions between localized states are not possibly unless the density is degenerately high.

If we focus only upon the transition from filled localized states into the conduction band, then the general equation for an optical transition can be simplified for the n-type semiconductor into

where g(E) is the density of states within the gap and $g_c(E)$ is the density of states in the conduction band. Transitions into the conduction band can occur as long as the states are occupied after a time *t* following a voltage filling pulse, i.e. up to an energy $E_e=k_BT*ln(vt)$. To further simplify the integral we sill assume that the optical matrix element does not vary significantly over the energies probed, and we will also take the density of states within the conduction band to be a constant as well.

$$P(E_{opt}) \propto \int_{E_c-E_{opt}}^{E_c-E_e} g(E)dE$$

Under these assumptions, the optical signal will simply be proportional to an integral over the density of states within the band gap. Indeed, very good fits to TPC spectra are obtained most of the time with an integral over a Gaussian defect band (error function) plus an exponential Urbach edge.

Carrier type sensitivity

Although not utilized yet in these materials, TPC has the added capability of being sensitive to the type of carrier which is being trapped.[14] For a dominantly n-type material,

$$TPC \propto n - p$$

This can affect the spectra in several different ways. If the minority carriers (holes) are being collected efficiently above the band gap, then the TPC signal will be suppressed significantly. This is seen in some photovoltaic solar cell materials where the minority carrier mobilities are significantly higher than that in amorphous oxide semiconductors. The other way that this sensitivity can affect the spectra is in the defect signal. If there is a defect which can strongly trap an optically excited minority carrier, a sign change in the TPC spectrum will be observed. This means that the recovery of the depletion capacitance after the bias pulse will be optically suppressed. In order for this to happen there must be a higher concentration of minority carrier traps which are optically active.

An example of the transient responses is shown in Figure 3.11, showing the light difference in response when the device recovers under illumination as opposed to in the dark. It is important to keep the intensity of the incident light very low in order to obtain a linear response from the sample; that is, we work in a regime such that if the intensity of the monochromatic light is doubled, the measured signal doubles as well.

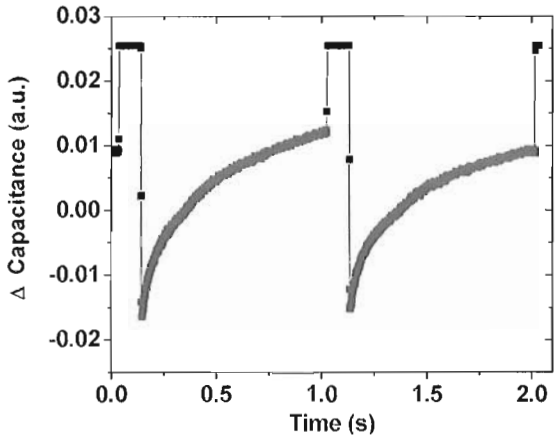

Figure 3.11: Transient capacitance response of sample with (left transient) and without (right transient) incident light.

If the incident photon flux is too high the signal will begin to saturate, which then results in a sub-linear intensity response. The timing sequence of the measurement is shown in Figure 3.12. Note that the DC bias pulse is never applied while the light is on the sample.

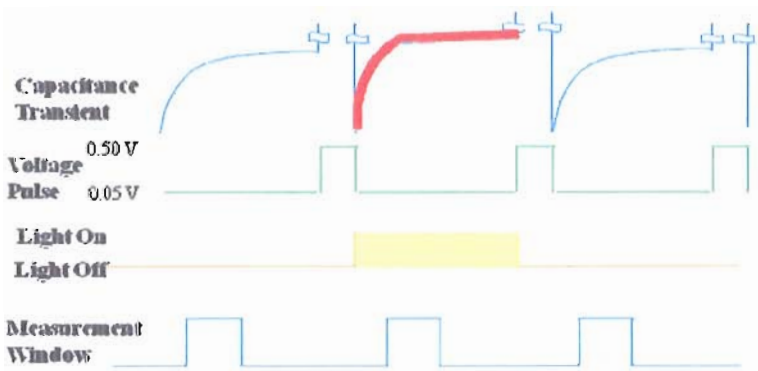

Figure 3.12: Timing sequence of TPC measurement. Note that the sample is not illuminated while the bias pulse occurs.

A wide variety of disordered semiconductors have been investigated with TPC, with band-gaps ranging from 1.0 eV ($CuInSe_2$) to 3.7 eV (ZTO). Figure 3.13 shows TPC spectra of several of these materials. All of the TPC spectra exhibit an exponential (Urbach) edge (which is ubiquitous in disordered semiconductors), and several of the spectra show mid-gap optically active defects. The fits to the spectra are integrals over the Gaussian defect band plus an exponential edge. The Urbach edges have characteristic energies which range from 11 meV for the $CuInSe_2$ to 120 meV for the ZTO.

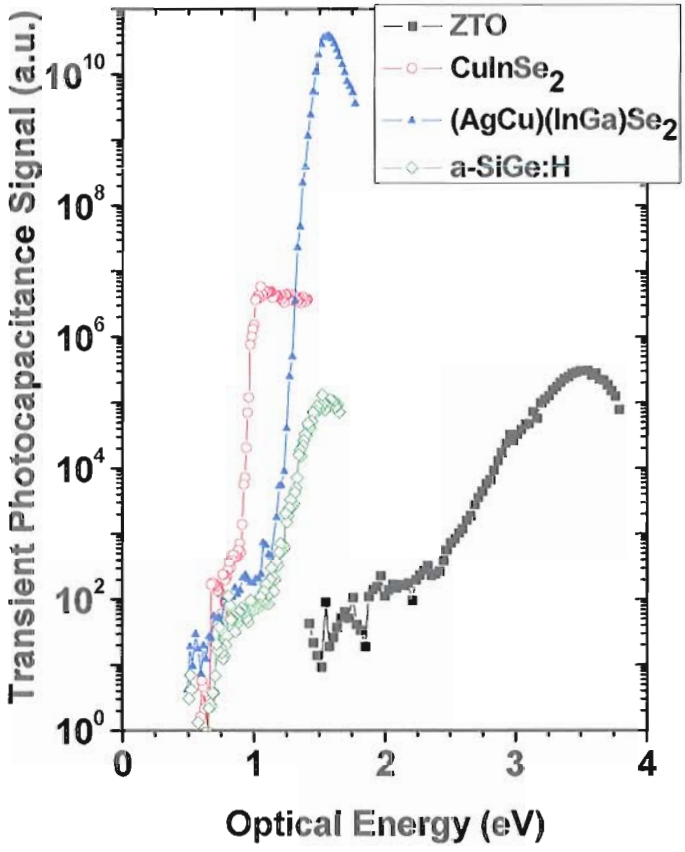

Figure 3.13: Transient photocapacitance spectra of materials with a wide range of band gaps (typically the maximum of each spectrum). The materials with band gaps between 1.0 and 1.8 eV are designed for photovoltaic solar cell applications.

The Urbach energies are a reflection of the amount of structural disorder in the material. Like any sub-band-gap optical absorption measurement, the measured Urbach energy reflects the broader of the two band-tails. Therefore, depending on the type of device, this may or may not be correlated with its performance.[15] In the case of ZTO and IGZO, the valence band tail is the broader of the two; however the transistor device properties are primarily determined by the density of states near the conduction band. Thus, while we can obtain information about the amount of structural disorder in the materials, we do not expect to establish direct correlations to transistor performance via the deduced Urbach energies.

While a one-sided junction (p^+-n in this case) would be ideal for interpreting TPC results, currently there are no materials which make a good rectifying contact with the n-type amorphous oxide semiconductors. As a result, there is some ambiguity as to the physical location of the defect band because states located at the AOS/insulator interface will have an associated dipole moment and thus also contribute a capacitive response. However, by investigating a structure which is similar to that of an AOS transistor, more direct relations to device performance can be made.

3.7. Modulated Photocurrent Spectroscopy

While the aforementioned characterization techniques are very useful in determining the sub-mobility-gap density of states, they are limited in the fact that they only probe states which are normally filled with electrons, that is, those lying below E_F. The performance of uni-polar devices based on these materials, such as transistors, depends more strongly on the density of states near the conduction band edge. The modulated photocurrent spectroscopy (MPC) method probes the density of usually empty defect states (above E_F) by examining the amplitude and phase shift of the photocurrent induced in the sample in response to a chopped light source, as illustrated in Figure 3.14.

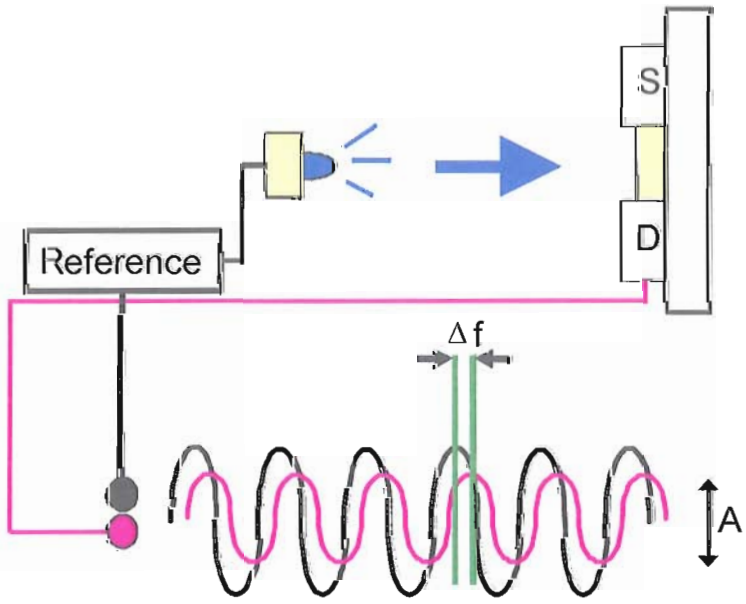

Figure 3.14: The amplitude (A) and phase shift (Δf) of a sample in response to a chopped light source is probed by the MPC measurement. This response yields information about the density of states near the majority carrier band edge, in this case the conduction band.

MPC was developed first by Oheda[10], with later contributions by Brüggeman[16] and Hattori[17]. There are several requirements for MPC to provide insight into the density of states near the conduction band (for an n-type semiconductor). The sample must be very intrinsic, or E_F must be at least several tenths of an eV from the band-edge. MPC can be performed on either co-planar or sandwich geometry samples, but in a sandwich geometry there must be a substantial portion of the film lying outside the depletion region. MPC must be performed in a regime within or near the dielectic freeze-out, so that the free charge in the sample does not have time to move and screen the photo-generated charge.

Modulated Photocurrent Theory

The photoinduced carriers are governed by rate equations which take into account the generation rates, recombination time, and the density of states. I have briefly reproduced the derivations first presented by Oheda[10] and Brüggeman[16] below. The rate equation for the free carriers is:

$$\frac{dn}{dt} = f_0 + f_1 e^{i\omega t} - \int_{E_{Fn}}^{E_c} \frac{dn_t(E)}{dt} dE - \frac{n - n_d}{\tau_R}$$

And the trapped carriers:

$$\frac{dn_t(E)}{dt} = nv\sigma[N_t(E) - n_t(E)] - N_c v\sigma n_t(E)e^{-\frac{E_c - E}{k_B T}}$$

Where f_0 and f_1 are the DC and AC generation rates, respectively, ω is the modulation frequency, v is the thermal velocity, σ is the electron capture cross section, n_d is the free carrier density in the dark and τ_R is the characteristic recombination time. These equations can be solved exactly, and solutions have the form

$$n = n_0 + n_1 e^{-i\omega t}$$

With n_1 given by

$$n_1 = \frac{f_1}{(A^2 + B^2)^{\frac{1}{2}}} e^{-i\phi}$$

A and B are the in-phase and quadrature components of the modulated photocurrent, and are given by

$$A = \frac{1}{\tau_R} + \int_{E_{Fn}}^{E_c} G_2(E) v\sigma N_t(E) dE$$

$$B = \omega + \int_{E_{Fn}}^{E_c} G_1(E) \upsilon \sigma N_t(E) dE$$

And thus the phase shift is given by

$$\phi = tan^{-1}\left(\frac{B}{A}\right)$$

$G_1(E)$ and $G_2(E)$ are weighting functions which give the relative contributions of traps to the in-phase and quadrature components of the response. $G_1(E)$ is sharply peaked at the excitation energy E_ω while $G_2(E)$ is flat below E_ω and then falls exponentially above E_ω. These weighting functions are shown in Figure 3.15 for excitation energies near 0.4 eV and 0.6 eV.

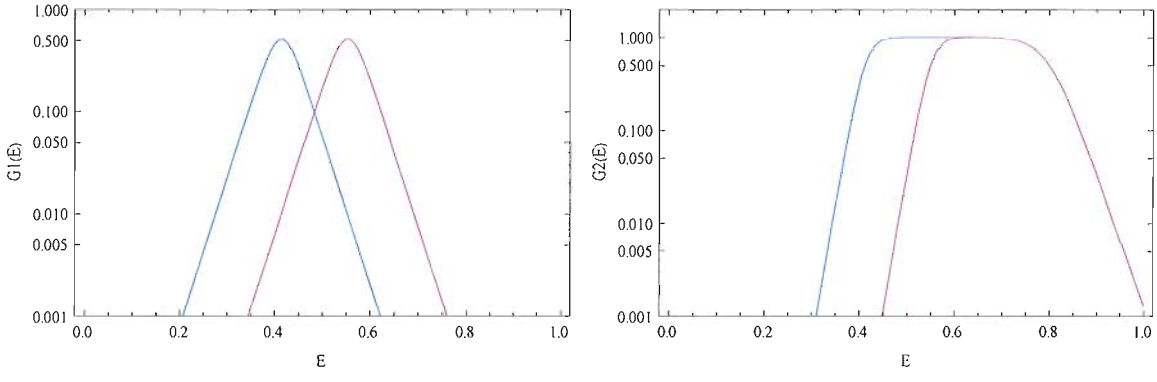

Figure 3.15: Graphic representation of weighting functions used in MPC derivation. $G_1(E)$ peaks sharply at the excitation energies E_ω near 0.4 eV (blue) and 0.6 eV (red).

By approximating $G_1(E)$ as a delta function and $G_2(E)$ as a step function, Oheda[10] was able to develop a recursive method for calculating the density of states. Additionally, this calculation required independent measurements of the thermal velocity, electron capture cross section and the effective recombination time. Brüggeman[16] improved the MPC derivation by including the amplitude of the modulated current, as the current is directly related to the number of photogenerated carriers.

$$I_{ph1} = f_1 \mu e E A |n_1|$$

Where μ is the free carrier mobility, A is the area of the device being investigated, E is the applied electric field. If we use the same approximations for G_1 and G_2 now we can directly calculate the relative density of states at energy E_ω.

$$N_t(E_\omega) = \frac{2}{\pi k T v \sigma} \left\{ \frac{f_1 e \mu E A}{I_{ph1}(\omega)} sin\, \phi - \omega \right\}$$

The frequency term in the braces is usually negligible. This equation will be referred to as the Brüggeman analysis. The Brüggeman analysis is very convenient and useful method, however suffers from a resolution limited by k_BT. That is, at room temperature (k_BT ~26 meV) it would be impossible to resolve a band-tail with a characteristic energy less than 26 meV. Cold stages capable of using liquid nitrogen as the coolant are then

necessary to resolve band tails near 10 meV, however even then ambiguity about the resolution limit vs. the band tail can occur.

Hattori[17] formulated another method for determining the density of states from the amplitude and phase shift data using a derivative method. While this method requires a much greater signal to noise ratio, the increased resolution limit of ½ k_BT is very beneficial.

In the Hattori analysis, the modulated photocurrent signal S(ω) is defined as:

$$S(\omega) = \frac{d}{dln(\omega)} \frac{cos\phi}{\Delta J}$$

Where ϕ is the phase shift and ΔJ is the amplitude of the modulated current. The increased energy resolution in this analysis is due to the derivative with respect to the measurement frequency, *d/d(ln(ω))*.

Sample Geometry Considerations

MPC may be performed on samples in either the co-planar or sandwich geometries without any change in the analysis procedure. The co-planar geometry is advantageous in some respects: it does not require a thick layer of the material under investigation, the device more closely mimics the structure of MOS transistors, and because the channel layer is typically very long any effects due to non-ohmic contacts to the semiconductor are usually negligible. However, the co-planar geometry also leaves some ambiguity about the exact conduction path. There is a very distinct possibility that the dominant conduction path is along the insulator-semiconductor interface or on the surface of the semiconductor. Indeed, samples fabricated on transistor substrates of heavily doped Si with a SiO_2 insulating layer showed a much different photocurrent response than samples fabricated on ESR grade quartz (SiO_2) substrates. While these differences could have also been caused by optical absorption in the silicon gate, in general this indicates the difficulty in trying to make precise conclusions from triode structures such as that of the transistor.

The sandwich geometry samples solve the conduction path problem by requiring that the conduction path is through the bulk of the semiconductor. Sandwich geometry samples however typically do need much thicker layers to be analyzed, on the order of 1-2 μm as opposed to ~100 nm for coplanar geometry samples. Fabricating thick devices can raise

questions as to the morphology of the sample – whether the material is still truly amorphous or whether crystallites are forming.

3.8. Space Charge Limited Current

In insulating materials, currents much larger than what would be possible with purely ohmic conduction are possible. These currents are referred to as space-charge-limited currents (SCLC). SCLC measurements were initially performed on vacuum diodes, after which the technique was then transferred to insulating materials with very low carrier densities as a direct analog. In materials with deep trapping states, the actual current will be much less than what would be theoretically expected. As such, SCLC can reveal information about the density of states within the band gap of insulating materials. Rose[11] was one of the first to actively pursue space charge limited currents as a way to characterize the energy distribution of states within the band-gap of insulators. The measurement was then applied to a-Si:H and a-SiGe:H by researchers including Solomon[18], Weisfield[19] and den Boer[20] as they attempted to understand the sub-band-gap structure of these disordered materials.

SCLC is characterized by a super-linear dependence of the current I on the applied voltage, that is:

$$I \propto V^m$$

If m = 1, then there is an ohmic response. If m > 1, then a space charge limited response may be observed. In this case, a characteristic energy can be obtained which is likely representative of the slope of the density of states near the Fermi energy. In this case

$$m = 1 + \frac{E_{char}}{k_B T}$$

where T is the measurement temperature and k_B is Boltzmann's constant. If the Fermi energy is located near the band-tail in a disordered material, then the characteristic energy may be indicative of the Urbach energy of the majority carrier band-tail.

SCLC measurements were initially attempted on ZTO MOS transistor structures. Results indicative of SCLC were obtained, however it became apparent that the gate was influencing the IV characteristics. In an attempt to resolve this issue, matched samples were fabricated, one device on a Si gated SiO_2 substrate matched to an identically finished coplanar device on an ESR grade quartz (SiO_2) substrate. The samples with the Si gate showed SCLC characteristics; however the sample on the quartz substrate did not. We believe that in the Si gated samples a narrow conducting channel is formed near the

ZTO/SiO_2 interface. When a bias is applied between the source and the drain, the majority of the current is carried by this channel. Since the charge density within the channel is very high, the current is much more likely to become space charge limited. In the quartz substrate devices, this conduction channel is not formed and the current is carried by the bulk of the ZTO. The charge density then does not become high enough to limit the current through the sample. While one cannot obtain information about the bulk of the semiconductor with this technique, it does provide insight into the conduction path in ZTO transistor devices. Results are discussed further in the Appendix.

3.9. Notes

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CHAPTER IV

EXPERIMENTAL RESULTS

4.1. Admittance spectroscopy

Admittance spectroscopy measurements were performed on a wide range of samples as a preliminary way of determining whether each sample could provide useful information from the other capacitive profiling methods. A scan of capacitance and conductance versus frequency and temperature provides information about whether or not there are sub-band-gap defect states responding in the sample, or if the sample is completely depleted. Additional information about the spatial location of defect states that are identified by the step in the capacitance spectrum is gained by performing admittance spectroscopy at different DC biases. Sandwich geometry samples with some sort of barrier junction are required for admittance spectroscopy measurements; in this study the metal-insulator-semiconductor (MIS) device structure was utilized.

Zinc Tin Oxide (ZTO)

Admittance spectroscopy was performed on a wide variety of ZTO MIS devices. Most devices exhibited evidence defect states in the bulk of the ZTO, at the ZTO/insulator interface, or both. As a result of the observation that the performance of thin-film transistors (TFT's) based around ZTO channel layers generally improved with increasing post-deposition anneal temperature up to the point where the ZTO began to crystallize, a series of MIS capacitor samples were co-deposited and then subjected to varying post-deposition anneal temperatures. Several different sets of devices were fabricated on heavily doped Si/SiO_2 substrates with ZTO layers varying from 600 nm to 1.8 μm. Capacitive steps in the spectra such as illustrated in Figure 4.1 were observed for many devices. This step is indicative of a broad band of defects responding within the mobility gap.

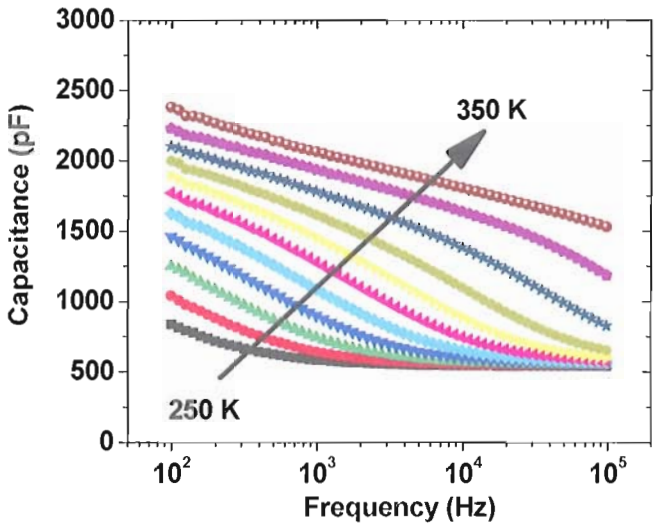


Figure 4.1: Admittance spectrum of ZTO MIS device indicating that a very broad band of defects are beginning to respond above 250 K. The activation energy for this step is near 800 meV.

Initially the results from admittance spectroscopy were unclear. Arrenhius plots to determine the energies of activation from these steps yielded anything from E_A = 1 eV to E_A = 200 meV for different samples, with no apparent underlying mechanism. However, when the DC bias dependence of these energies was examined it became clear that trap states at the ZTO-SiO_2 interface were having a large influence on the spectra. Figure 4.2 displays the capacitance and conductance of the same ZTO sample as in Figure 4.1, only with a 3 V DC bias applied in the forward direction. The activation energy is near 800 meV when the sample does not have any bias applied, and then decreases to near 380 meV with the forward bias.

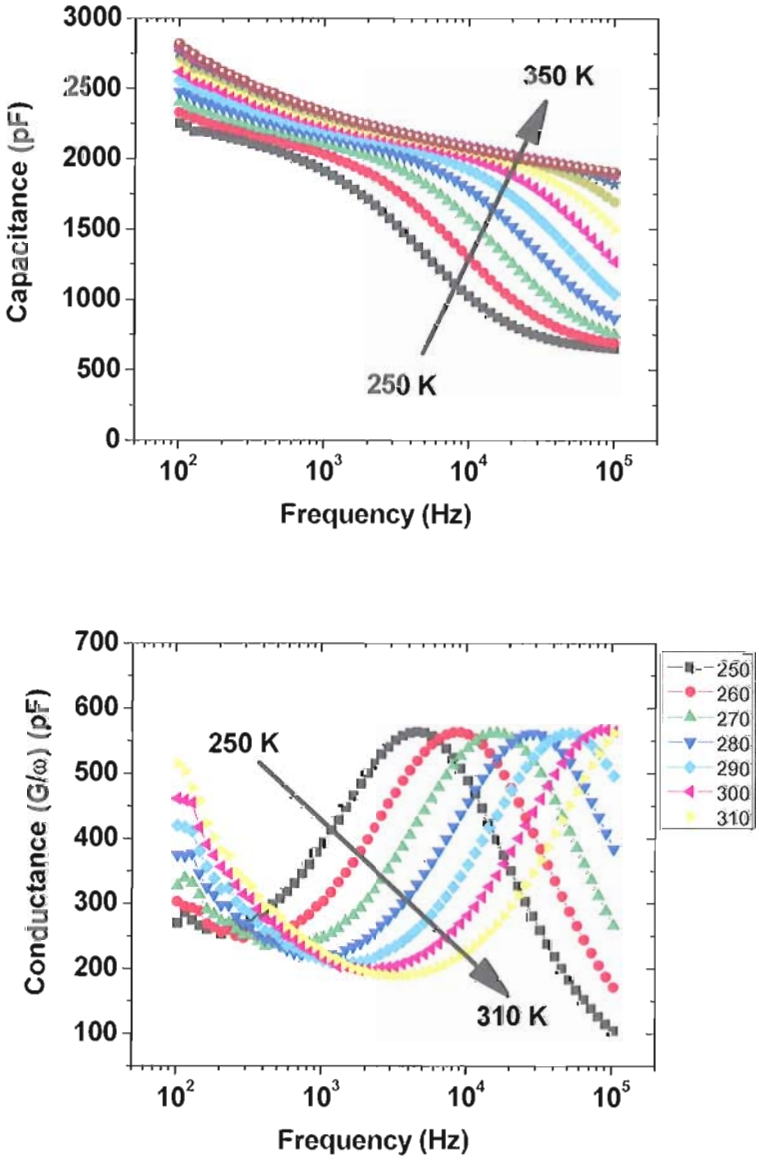
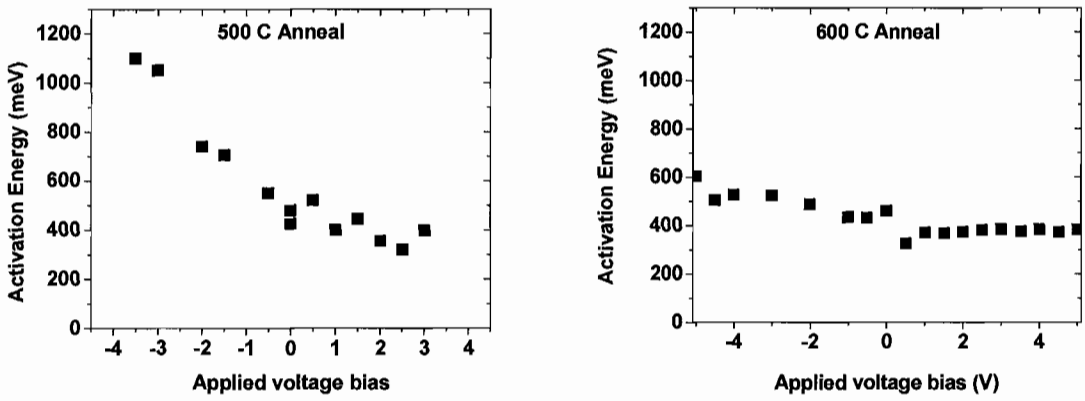


Figure 4.2: Capacitance (top) and conductance (bottom) of ZTO MIS device under 3 V forward bias. Now the activation energy is near 380 meV, down from 800 meV when admittance was performed under 0 V bias.

The dependence of the activation energy on applied DC bias for two co-deposited samples subjected to different post-deposition anneal temperatures (500 °C and 600 °C) are shown in Figure 4.3.



(a) (b)

Figure 4.3: Activation energy vs DC bias for ZTO MIS device subjected to (a) 500 °C post-deposition anneal and (b) 600 °C anneal.

Based on the large variation in the activation energy of the sample annealed at 500 °C, it is clear that we are not measuring the energetic depth of a band of defects in the bulk of the ZTO. Rather, we are likely observing the response of defects at the ZTO/SiO_2 interface and the "activation energy" is actually related to the interface potential. In the 600 °C annealed device there is a much smaller variation in the activation energy with DC bias. While the sample is in reverse bias there appears to be some contribution from states at the interface, however there is likely a band of defects in the bulk of the ZTO approximately 400 meV from the conduction band. Indeed, the activation energies of the

sample annealed at 500 °C appears to reach a limiting value near this as the DC bias is increased. Thus the post-deposition anneal increases the TFT performance by reducing the number of states at the ZTO/SiO_2 interface, also making the TFT "turn-on" voltage much closer to 0 V.

The density of interface defects can be estimated in the manner presented in the previous chapter. Figure 4.4 is the derived density from the high and low frequency capacitance values plotted as a function of the activation energy derived from the Arrhenius plots, which we take to be the interface potential.

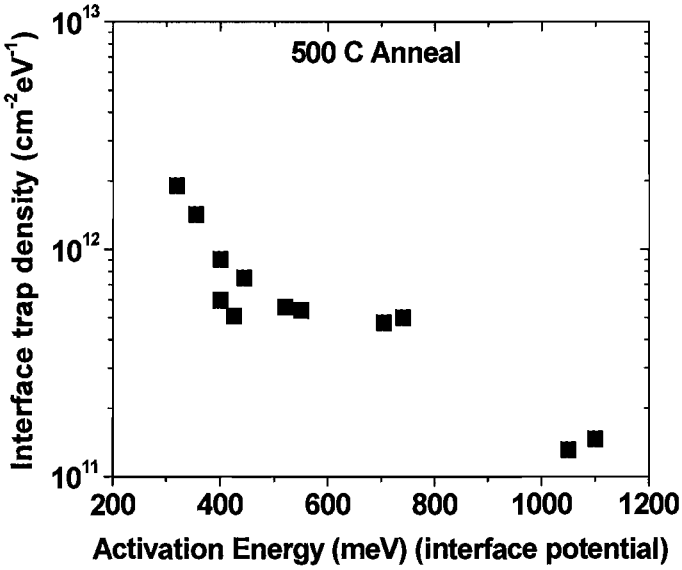


Figure 4.4: Area density of defects derived as a function of interface potential for 500 °C anneal ZTO sample. The derived density at activation energies below 400 meV are likely influenced by a bulk defect level in the ZTO as well.

Note that the values at low activation energies may include some of the response from a bulk defect, so our most accurate estimate of interface density would be near ~ $5*10^{11}$ $cm^{-2}eV^{-1}$.

Indium Gallium Zinc Oxide

The admittance spectra of IGZO MIS devices are very similar to those of the ZTO devices, suggesting commonalities within the amorphous oxide semiconductor class of materials. Some IGZO devices exhibited bias-independent deep levels, while others showed features likely located at the IGZO/insulator interface. Figure 4.5 shows the bias dependence of the activation energy for IGZO deposited on a 25 nm chemical-vapor deposited SiO_2 insulator layer. The activation energy drops dramatically, and finally appears to reach a limiting value near 170 meV, slightly closer to the conduction band than for the ZTO device discussed previously.

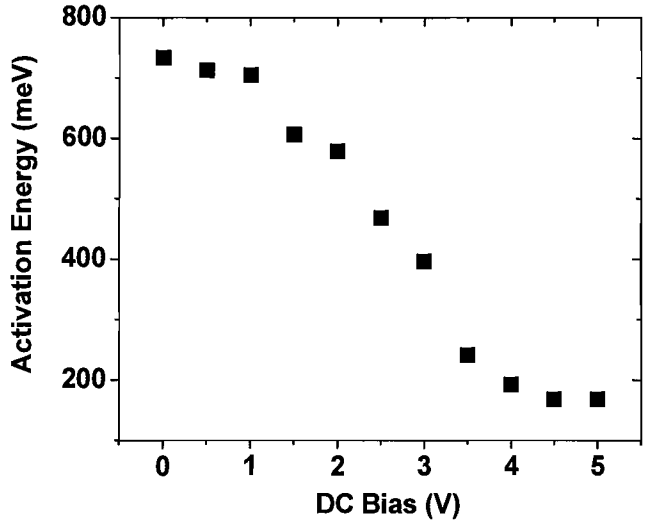


Figure 4.5: Bias dependent activation energy in an IGZO MIS device on a SiO_2 substrate.

IGZO samples on different substrates, such as the AlPO[1] insulating layers, exhibited activation energies which were much less sensitive to the applied DC bias. The very abrupt capacitive step shown in Figure 4.6, for example, did not vary at all as the admittance spectra were measured under different DC biases.

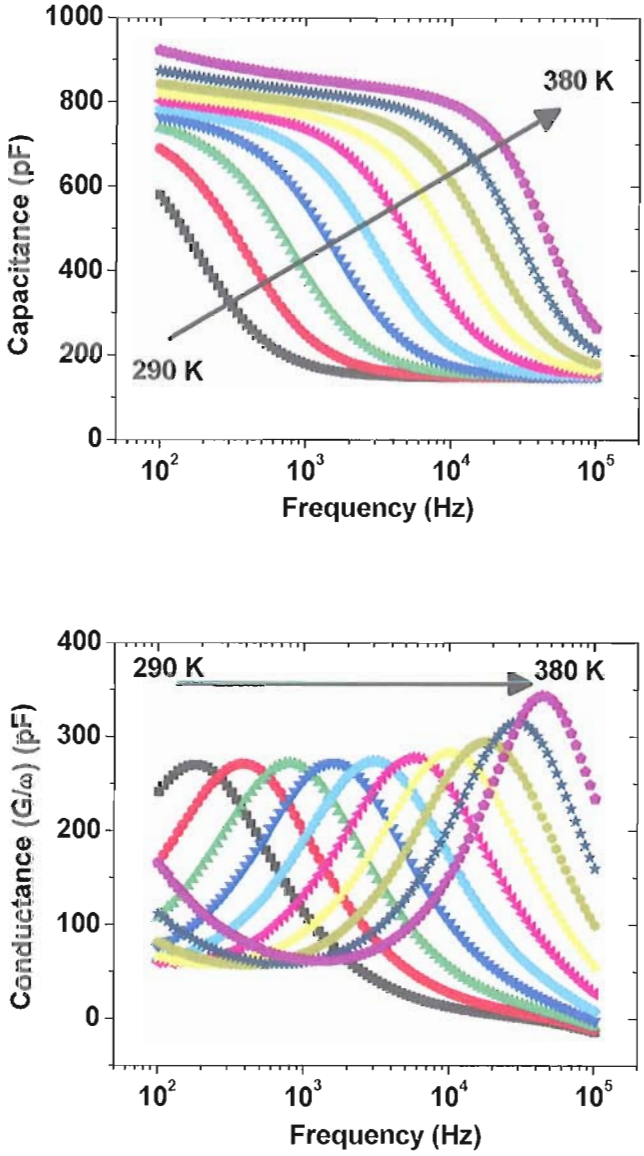


Figure 4.6: Admittance spectrum of IGZO on 50 nm AlPO insulating layer. This activated step was relatively bias-independent, with an activation energy of 600±30 meV over DC biases ranging from -2 V to 2 V.

4.2. Spatially Sensitive Capacitance Profiling

Zinc Tin Oxide

In order to further understand the changes induced in ZTO thin-film transistors inducted by the differing post-deposition anneals, several sets of co-deposited ZTO MIS capacitors were fabricated at Oregon State University.[2] The devices were annealed for one hour in air at temperatures ranging between 400 °C and 600 °C.[3] ZTO thin-film transistors processed in an identical manner as to this experiment were found to possess uniform properties across the substrate. Thus, the films being assessed in this study are believed to be quite homogeneous.

Drive-level capacitance and capacitance-voltage (C-V) profiles could only be obtained for the higher temperature anneals of 500 °C and 600 °C and these are compared in Figure 4.7. Samples annealed at lower temperatures showed evidence of a very large defect density which would not allow us to profile into the bulk of the films. The profiles indicate free carrier densities of $5x10^{14}$ cm^{-3} and $1x10^{15}$ cm^{-3} for the 600 °C and 500 °C samples, respectively. As the profiles are presented, x = 0 corresponds to the Si/SiO_2 interface so that as x increases the distance to the insulator-semiconductor interface is becoming larger.

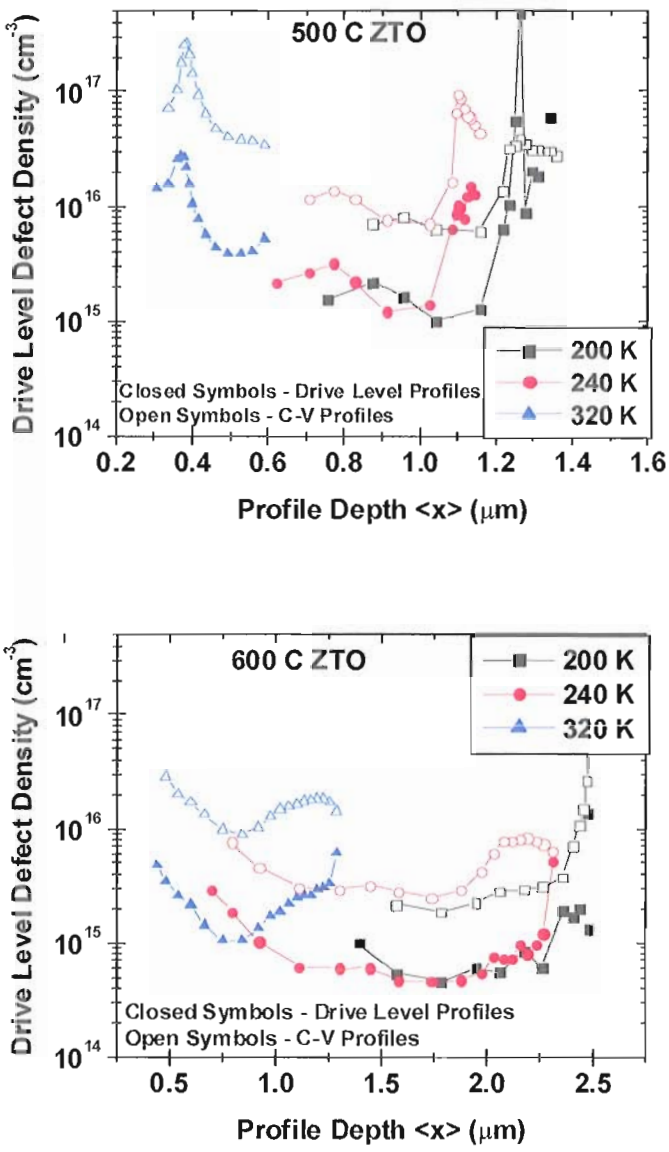


Figure 4.7: DLC and C-V profiles for 500 °C (top) and 600 °C (bottom) ZTO samples. The DLC and C-V profiles taken at lower measurement temperatures show the free carrier and deep defect densities, respectively. The higher temperature DLC profiles are likely influenced by the response of states at the ZTO/SiO_2 junction (x = 0.1 μm).

The profiles also exhibit deep defect densities of $1.5x10^{15}$ cm^{-3} and $5x10^{15}$ cm^{-3} for the respective samples. Thus, as the post-deposition anneal temperature increases, the free carrier density and deep defect density both decrease. The profiles taken at the highest measurement temperatures are most likely influenced by the response from the interface charges which are observed in admittance spectroscopy, and so cannot yield a good estimate of the bulk film free carrier density or deep defect density at that temperature. However, note that the maximum defect density in the high temperature DLC profile corresponds with the low temperature C-V density. This agrees with the interpretation of the differences between drive level and C-V profiling as discussed in the previous chapter, and so the information contained in the low temperature profiles is likely representative of the basic materials properties.

By examining the temperature dependence of one of the ZTO samples and also using the thermal prefactor obtained from admittance spectroscopy, a rough idea of the energetic width of the deep defect was obtained. Using the relation $E_e = k_B T \ ln(v/2\pi f)$ the measurement temperature can be converted to an energy scale. Figure 4.8 is the temperature dependence of the drive level carrier density of a ZTO sample annealed at 600 °C on an energy scale.

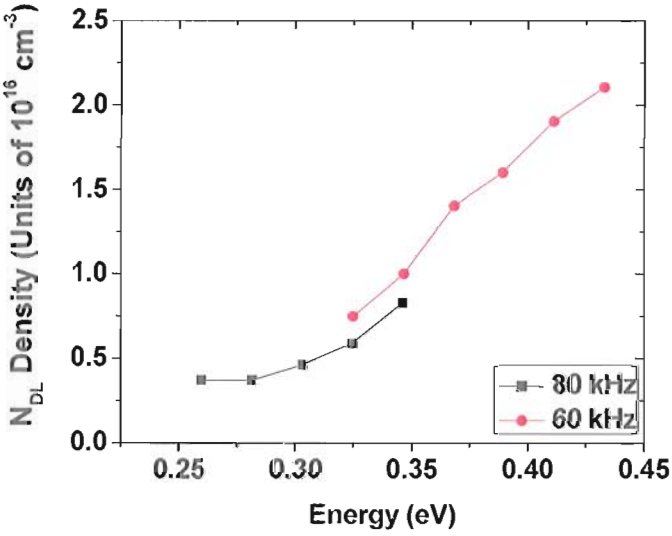


Figure 4.8: Carrier density vs emission energy for 600 °C annealed ZTO. A broad band of defects centered near 0.4 eV is the most likely explanation for this increase in carrier density as the measurement temperature increases.

In devices with the MIS structure, a large part of the applied DC potential will drop across the insulating layer. The profile depth, <x>, from the drive level profiles can be used to estimate the amount of potential difference within the semiconducting layer as the DC bias is varied. By using the following equation, it was determined that for the ZTO samples on a 100 nm SiO_2 insulating layer, for every 1 V DC bias applied across the sample, there was a 0.9 V drop over the insulating layer and a 0.1 V drop across the ZTO. This corresponds closely to the result obtained with admittance spectroscopy for the same sample, where the activation energy obtained by the Arrhenius plots varied by approximately 800 meV as the DC bias changed from -4 V to +4 V.

$$< x_2 >^2 - < x_1 >^2 = \frac{2\epsilon A^2}{qN}(V_1 - V_2)$$

Where N is the carrier density, q is a fundamental charge unit, A is the sample area, ϵ is the dielectric constant of the material, and $(V_1\text{-}V_2)$ is the change in the potential across the semiconductor.

Amorphous ZTO defect profiles commonly showed evidence of a large defect located at the ZTO/SiO_2 interface as well. The samples discussed previously exhibited a sudden, large shift in the profile depth from which we inferred a state at the interface. Another way in which interface traps are identified is by comparing the drive level profiles to the

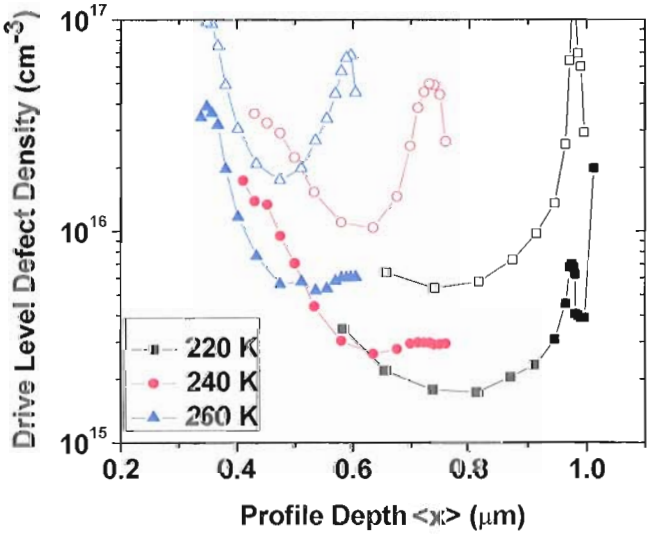


Figure 4.9: DLC (closed symbols) vs. C-V (open) profiles for the ZTO sample provides strong evidence for an interfacial defect; namely, the peak in the C-V profiles which is not present in the DLC profiles.

C-V profiles. In most situations, drive level capacitance profiles are insensitive to interface states whereas C-V profiles can be strongly influenced by the same states. Large differences between profiles produced by the two methods can then be attributed to interfacial states. In Figure 4.9 this large discrepancy between the two profiling methods is clearly evident in pulse laser deposited ZTO MIS devices. Although the peak in the C-V profiles might indicate a spatially localized state deep within in the sample, it is much more likely to be located at the ZTO/SiO_2 interface. When the sample is strongly reverse biased, the interface defect is partially filled. This allows the charges within the defects to respond dynamically to the AC bias, altering the shape of the C-V profile, and thus influencing the C-V carrier profiles. As the reverse bias is decreased, the band of defects becomes more completely filled, thus less of the charges can respond to the AC bias. This lessens the influence of the interface states on the carrier profile. When the reverse bias is decreased even more, or perhaps even when the sample is forward biased, the defect is completely occupied and then can no longer respond to the AC bias. The C-V profiles then decrease and become more similar to the DLC profiles. This series of situations is illustrated in Figure 4.10.

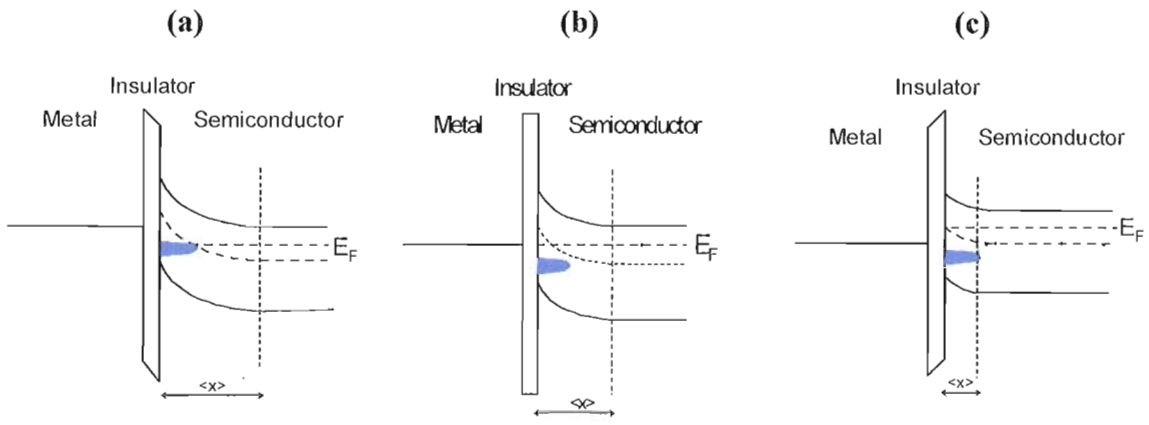


Figure 4.10: As the reverse bias is decreased from (a) to (c), the interface state initially responds to an AC perturbation, then can respond slightly less in (b), then does not respond in (c), when the state is completely occupied.

Figure 4.11 displays profiles for a ZTO MIS device co-deposited with the previously mentioned device; however, the substrate for this device is commercially available ITO/ATO. ATO refers to an Al_2O_3/TiO_2 super-lattice, which is used for the insulating layer. This device was examined to make a comparison to the Si/SiO_2 devices since the ITO/ATO substrates are more commonly used to fabricate completely transparent TFT's.

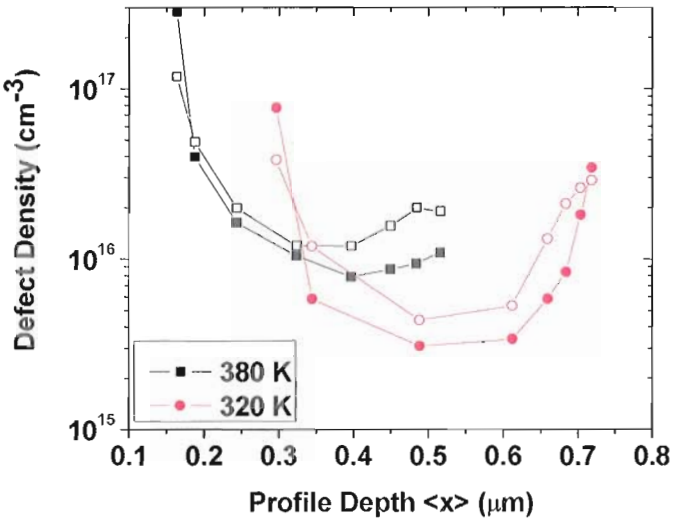


Figure 4.11: DLC (solid symbols) and C-V (open) profiles of ZTO on an ITO/ATO substrate. This sample is matched to the sample shown in Figure 4.9 but does not show signs of interface states.

Of particular interest in these profiles is the lack of the interface defect signature which was observed in the sample with the Si/SiO_2 substrate. Interfacial defects commonly occur because lattice mismatches at surfaces, so this suggests that there may be a difference between the SiO_2 and ZTO resulting in an electrically active defect which is not present between the ATO and ZTO. The defect may be either not present at all, or shifted in energy such that it is not electrically active under our measurement conditions.

Indium Gallium Zinc Oxide

IGZO shows many similarities to ZTO with respect to the spatially sensitive profiling methods. IGZO on SiO_2 MIS devices exhibited free carrier densities near $8x10^{14}$ cm^{-3} and deep defect densities near $1.5x10^{15}$ cm^{-3}, as shown in Figure 4.12. IGZO on aluminum phosphate (AlPO) insulators[1] were also investigated. While the drive-level profiles for these devices never showed a clear lower limit in their profiles to estimate the carrier density, they appeared to be approaching roughly the same free carrier density as for the IGZO on SiO_2 devices. The spatial defect profiling methods again did not show the signature of interface defects as was observed in the ZTO devices.

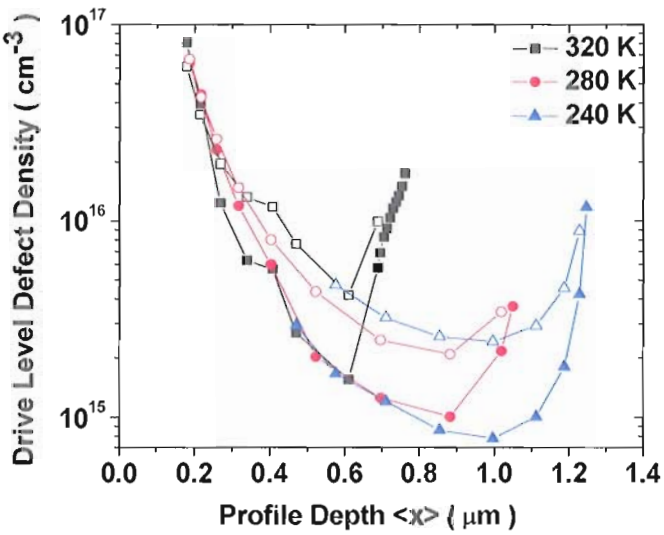


Figure 4.12: DLC (closed symbols) and C-V (open) profiles of IGZO on SiO_2 showing a free carrier density near $8x10^{14}$ cm^{-3} and deep defect density around $3x10^{15}$ cm^{-3}.

4.3. Transient Photocapacitance Spectroscopy

Zinc Tin Oxide

Transient photocapacitance spectroscopy (TPC) was used to investigate the optical transitions in ZTO MIS capacitors. TPC is useful in amorphous and disordered materials for two primary reasons: 1) The TPC spectra can determine the exponential slope of the density of states, also known as the Urbach edge, into the band gap, and 2) the spectra can provide information about optically active defects within the band gap. The set of ZTO samples which were co-deposited and then subjected to varying post-deposition anneals were all examined with TPC as well. The TPC spectra along with fitting functions are shown below in Figure 4.13.

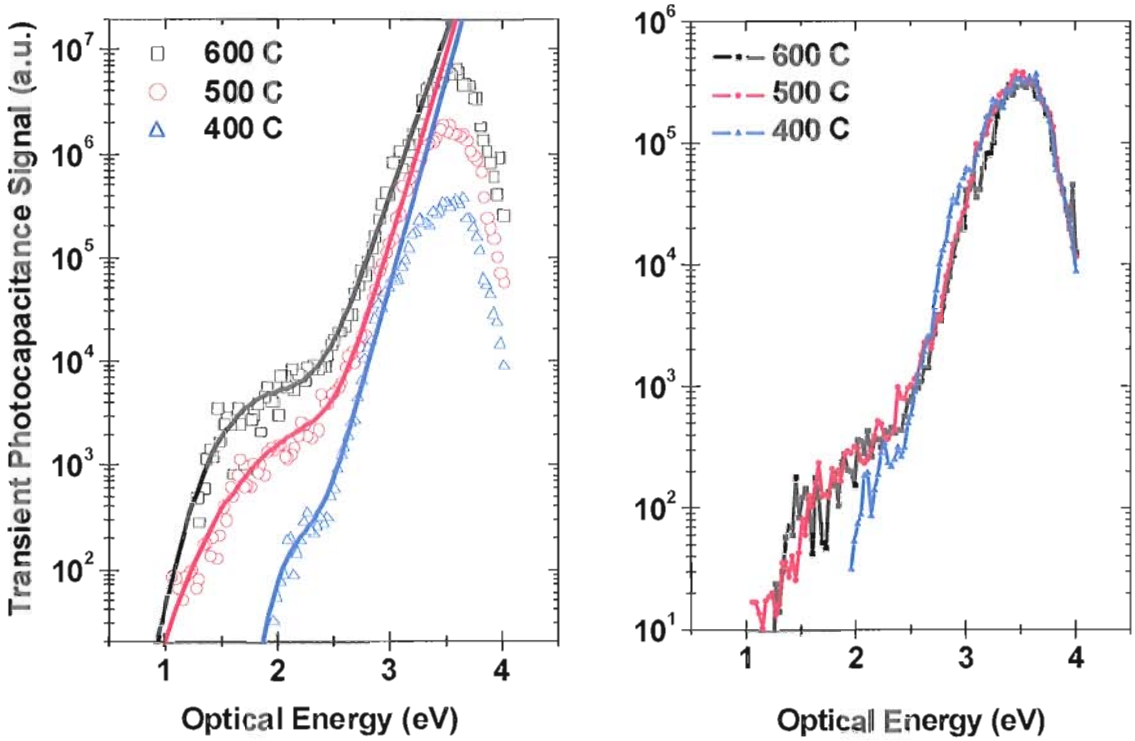


Figure 4.13: TPC spectra of amorphous co-deposited ZTO MIS capacitors annealed at varying temperatures. (left) The spectra have been offset to exhibit the different Urbach energies. (right) The same spectra aligned near 3.5 eV in order to compare the magnitude of the defect bands, which actually does not significantly change in these samples.

The spectra show that the Urbach edge actually increases with increasing post-deposition anneal temperature, as is summarized in Table 4.1. This implies that the amount of structural disorder in the sample increases up to the point where the ZTO begins to crystallize. The energetic position of the sub-band-gap optically active defect also moves further from the conduction band as the annealing temperature increases, however the magnitude of the defect band does not change significantly.

Table 4.1: Fitting parameters of TPC spectra for samples subjected to different post-deposition anneals.

Anneal temperature	400 °C	500 °C	600 °C
E_U (meV)	110	120	140
E_D (eV)	2.05	1.9	1.6

While it is somewhat counterintuitive that transistor device performance would increase as the structural disorder increases, it must be remembered that the TPC spectra only discloses information about the broader of the two band tails. In these materials this is likely the valence band tail: the conduction band is composed primarily of s-orbitals which are mostly insensitive to bond angle disorder while the valence band is composed of p-orbital hybrids which do depend on the angular disorder. Therefore the TFT device performance is likely unrelated to the Urbach energy in these samples.

The use of MIS capacitors for TPC measurements leaves the spatial location of the sub-band-gap defect ambiguous. One-sided junctions are ideal for these measurements as defects located at the junction interface do not have any effective moment and so do not generate a capacitive response. The thickness of the insulating layer in these devices means that optically active defects at the insulator-semiconductor interface will generate a capacitance response and so could potentially be observed with TPC. Several observations about the TPC spectra for ZTO have indicated that this is indeed the case,

that the sub-band-gap feature is an optically active defect located at the insulator-semiconductor junction rather than in the bulk of the ZTO.

First, the magnitude of the defect band can be estimated even though the TPC spectra are in arbitrary units. The density of states at the edge of the band gap is commonly around 10^{20} cm^{-3}.[4] The shoulder feature in the spectra in Figure 4.13 is approximately three orders of magnitude below the band-gap, which gives a density near 10^{17} cm^{-3}. This defect density approaches that of amorphous silicon, which was nearly abandoned for any kind of electronic device before it ws realized that the defects could be passivated with hydrogenation.

Additionally, the magnitude of the defect band varies drastically between depositions and samples. Figure 4.14 shows the two endpoint samples, the sample annealed at 500 °C with a very large defect band and another ZTO sample with no defect band present.

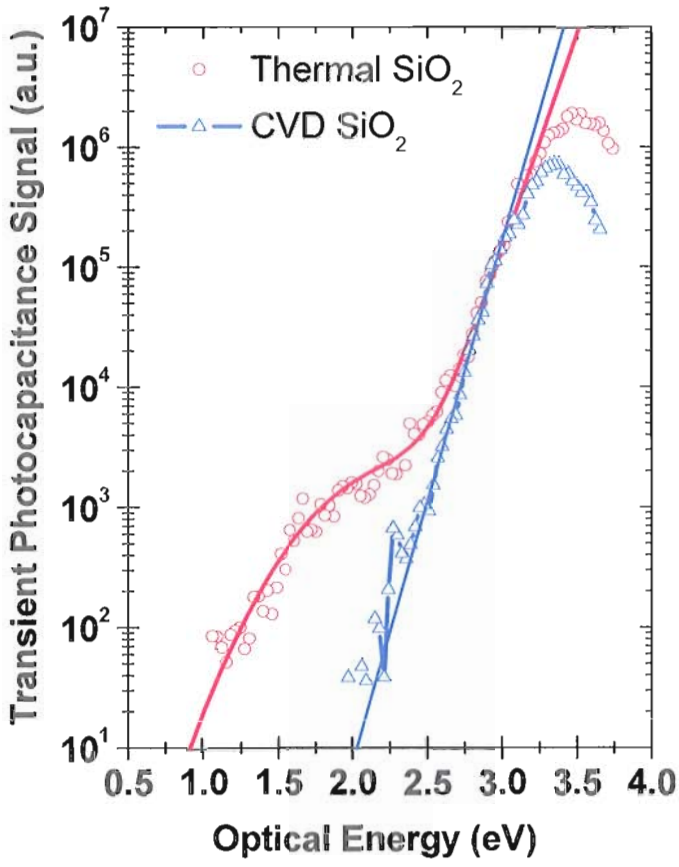


Figure 4.14: TPC spectra of ZTO on different insulator substrates, indicating the large variations in the magnitude of the sub-band gap optically active defect feature.

The final argument for locating the optically active defect at the insulator-semiconductor interface in ZTO comes from the dependence of the magnitude of the signal on the bias conditions. Figure 4.15 shows the magnitude of the signal increasing nearly two orders of magnitude as the bias conditions are adjusted. The height of the pulse is the same in all of the spectra, 1 V forward, only the steady state DC bias is adjusted. If the defect was located in the bulk of the ZTO there might be a small amount of variation in the TPC

signal due to the spatial sensitivity of the measurement. This small amount of variation does not account for the nearly 100x change however.

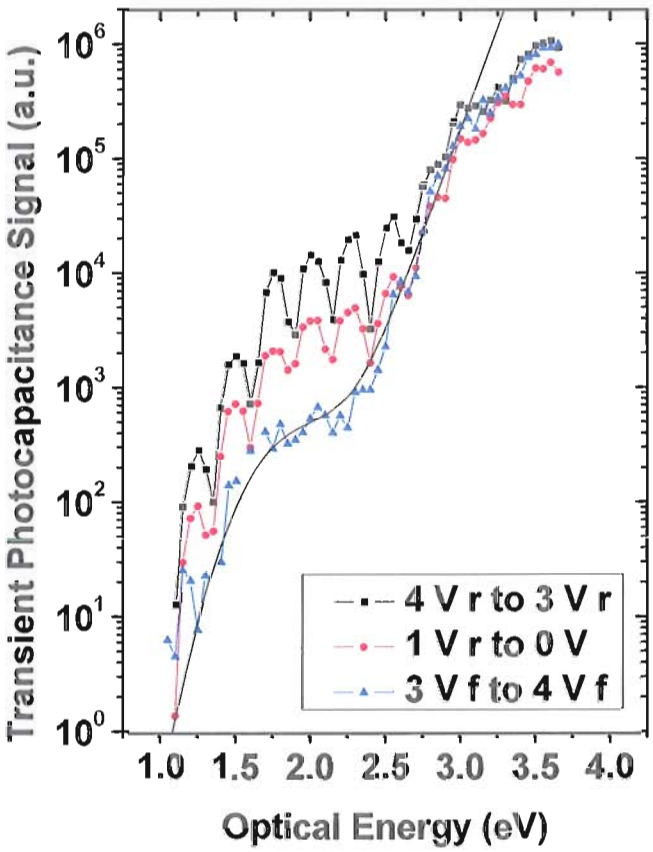


Figure 4.15: The amplitude of the defect signal depends on the bias conditions, suggesting that the defect is located at the insulator-semiconductor interface.

Indium Gallium Zinc Oxide

The similarities between the ZTO and IGZO devices suggest that there is an underlying fundamental structure to these amorphous oxide semiconductors. The Urbach energies in

IGZO MIS capacitors were all observed to be near 110 meV, much like the ZTO devices. Once again, there remained ambiguities as to the spatial location of the sub-band-gap optically active defect. In this study we were able to co-deposit 1.8 μm IGZO layers on four AlPO insulating layers with thicknesses varying between 25 nm and 200 nm. Drive level capacitance profiling confirmed that the IGZO layers had similar free carrier and deep defect densities. The TPC spectra for the IGZO devices are shown in Figure 4.16.

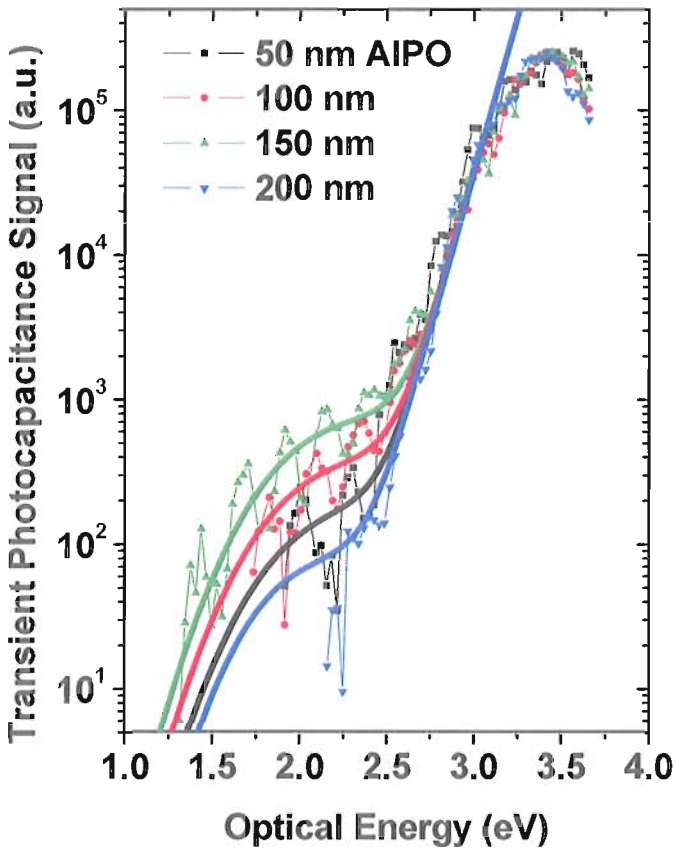


Figure 4.16: TPC spectra of IGZO on AlPO insulators of different thicknesses. The wide variation of the magnitude of the defect (shoulder) feature suggests that this state is located at the AlPO-IGZO interface.

The devices all exhibit the same exponential Urbach edge of 100 meV. The variation in the magnitude of the defect band again suggests that this optically active site is located at the AlPO/IGZO interface rather than in the bulk of the IGZO. As was seen in the ZTO samples as well, in some IGZO samples the magnitude of the defect signal also depended strongly on the biasing conditions, further suggesting that we are observing an interface state. Alternatively, some samples did not show any optically active defect feature within the sensitivity of the measurements, as shown in Figure 4.17. This particular sample was IGZO deposited on 25 nm thick SiO_2.

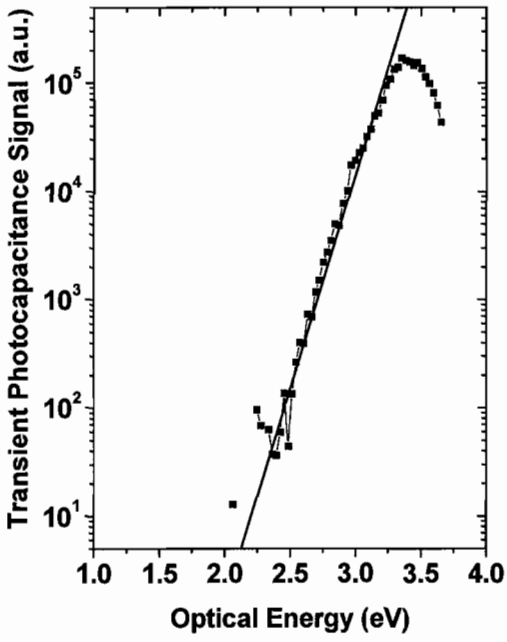


Figure 4.17: TPC spectra of IGZO on CVD SiO_2 showing no sign of an optically active defect in the middle of the optical gap within the measurements sensitivity. The Urbach energy in this sample is 110 meV.

Transient Photocapacitance Summary

The Urbach edges which were measured for both ZTO and IGZO MIS capacitors are summarized in Figure 4.18. For both of these amorphous oxide semiconductors the degree of structural disorder is characterized by the Urbach edges. For reference, a-Si:H typically has an Urbach edge of 45 meV for the best devices. Both types of transparent semiconductors show optically active states at the insulator-semiconductor interface. These states might be responsible for metastable effects observed in transparent transistors.

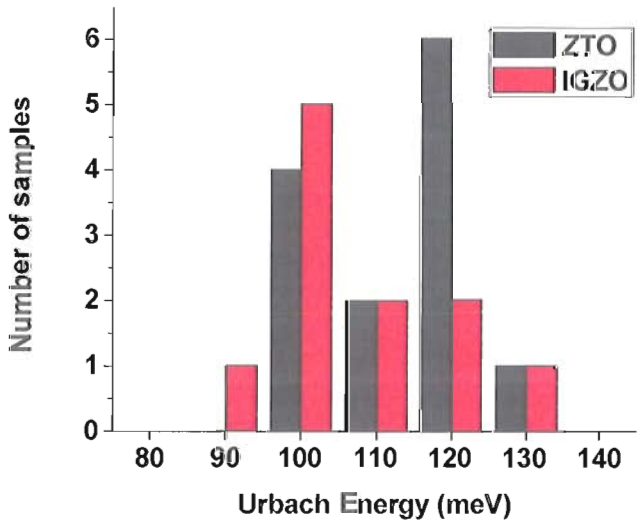


Figure 4.18: Summary of Urbach edges measured for ZTO and IGZO MIS capacitors by transient photocapacitance spectroscopy.

4.4. Modulated Photocurrent Spectroscopy

Modulated photocurrent spectroscopy (MPC) examines the amplitude and phase shift of the current generated in a device in response to a chopped light source. While the aforementioned junction capacitance based measurements only provide information about states in the gap which are usually filled with electrons, MPC probes states which are usually empty, or above the Fermi energy. The operation of uni-polar devices such as AOS transistors (which are n-type) is most affected by trapping states close to the conduction band. If the photogenerated current is limited by trapping in states within the band gap, then careful analysis of the amplitude and phase shift of the current with respect to the modulated signal can disclose the density of states near the conduction band.

In order for the MPC method to provide information that can be interpreted in this manner, the material and experimental conditions must satisfy several requirements. First, the material must be highly intrinsic, or the quiescent carrier concentration must be very low. Correspondingly, the Fermi energy must be sufficiently far away from the conduction band. Measuring the DC conductivity as a function of temperature provides a good estimate of the depth of the Fermi energy. In the most simple model, not taking into account deep states,

$$n = N_C e^{-\frac{E_C - E_F}{k_B T}}$$

And the resistivity is $\rho = (ne\mu)^{-1}$.

Therefore one can estimate the Fermi energy depth via an Arrenhius plot of the conductivity. As shown in Figure 4.19, the Fermi energy appears to be at least several tenths of an eV from the conduction band for the coplanar samples subjected to several different post-deposition anneal temperatures.

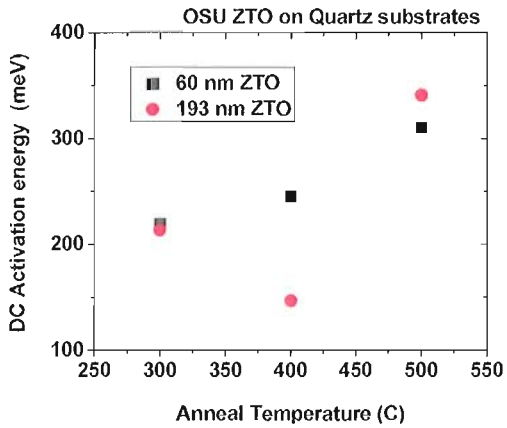


Figure 4.19: Depth of Fermi energy in band gap for coplanar ZTO samples subjected to several different post-deposition anneal temperatures.

Secondly, the experimental frequency and temperature must be chosen such that carriers cannot move to screen the light-induced charge before the charge is collected. Admittance spectroscopy measurements, such as shown in Figure 4.1, indicate that these

materials approach dielectric freeze-out conditions below approximately 220 K for frequencies commonly used for lock-in spectroscopy techniques, at or below around 40 kHz.

Initially a set of coplanar geometry samples were fabricated on ESR grade quartz substrates and subjected to varying post-deposition anneals. The amplitude and phase shift of the photogenerated current from the sample annealed at 300 °C are shown in Figure 4.20.

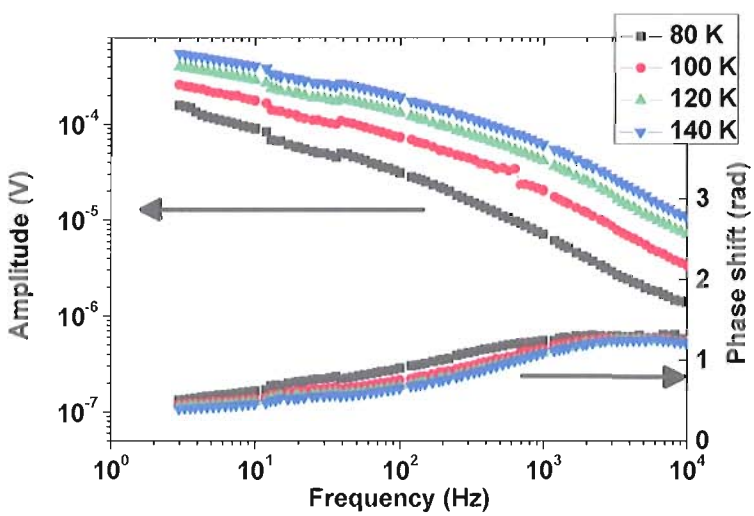


Figure 4.20: Amplitude and phase shift of photogenerated signal for coplanar ZTO sample annealed at 300 °C.

From this amplitude and phase shift information, the Brüggemann[5] and Hattori[6] analyses are applied (see section 3.7). Figure 4.21 displays the Brüggemann analysis of this data. It shows what appears to be an exponential band tail, however as the measurement temperature increases the band tail broadens significantly. Further investigation reveals that the band tail width simply reflects the temperature resolution of the analysis, as the exponential slope is just k_BT at each value of measurement temperature.

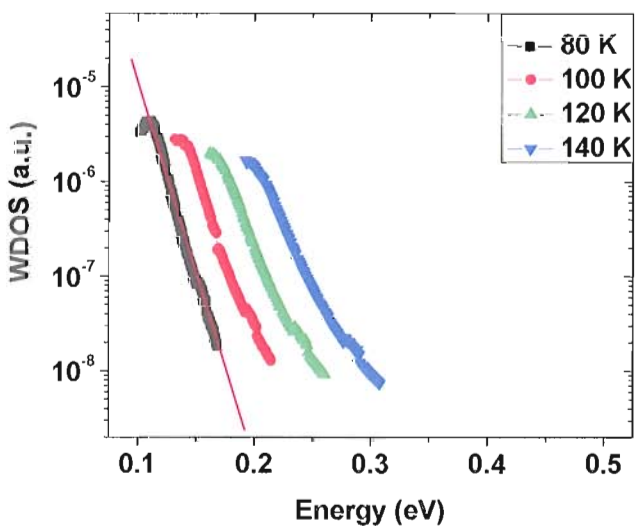


Figure 4.21: Brüggemann analysis of amplitude and phase shift of photogenerated current in coplanar ZTO sample. The fit line at the lowest temperature shows a 10 meV exponential slope.

The analysis developed by Hattori has a higher energy resolution of ½ k_BT, and since our data has sufficiently high signal to noise ratio this technique can be used effectively. Figure 4.22 now clearly shows an exponential band tail with a characteristic slope of 10 meV along with a defect band just below the band tail. The exponential part of the calculated density of states is largely temperature independent until approximately 220 K, when it starts broadening significantly. It is worth noting that the two analysis techniques agree at the lowest temperatures, where $k_BT \sim 10$ meV.

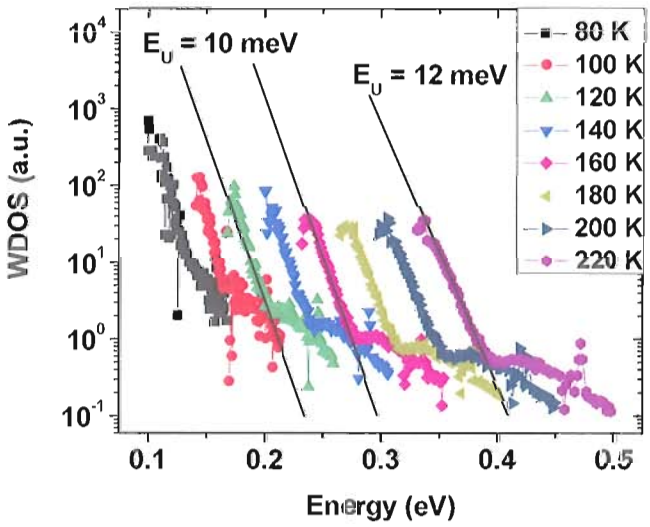


Figure 4.22: Exponential band tail and defect band as calculated from the Hattori method for the coplanar ZTO sample annealed at 300 °C.

Sandwich geometry ZTO samples were fabricated to confirm the value for the band tails found in the coplanar samples. In that case, ITO was used as the conducting back contact

and aluminum as the top contact with a 1.2 μm ZTO layer. For these samples it proved difficult to obtain data that was not too noisy. However, one clear spectrum was obtained, shown in Figure 4.23, which yielded a 12 meV Urbach edge in the Brüggemann analysis. This sample was subjected to a 300 °C post-deposition anneal. Because this spectrum was obtained at 80 K, where $k_BT = 6.8$ meV, we could be certain that the slope of the exponential edge was not being limited by the energy resolution of the analysis or the temperature of the measurement.

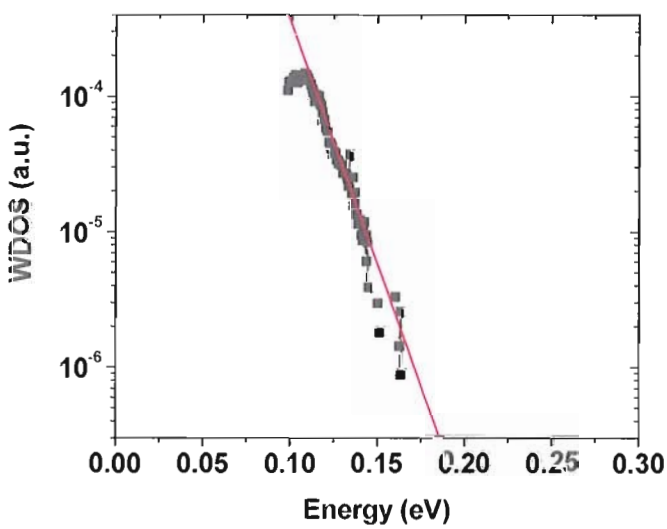


Figure 4.23: MPC results for ZTO sandwich geometry sample showing 12 meV Urbach edge from Brüggemann analysis. This spectrum was taken at 80 K, where $k_BT = 6.8$ meV, thus the analysis is not being limited by the measurement temperature.

The high mobility of ZTO can now be understood in terms of the very steep conduction band tail obtained by these MPC measurements. It is indeed very difficult to obtain the energy resolution necessary to resolve the band tail from the discrete defect band located just below the conduction band tail. We suspect that many other methods of estimating the density of states near the conduction band tail would not be able to distinguish between the two features.

4.5. Notes

[1] S. T. Meyers, J. T. Anderson, D. Hong, C. M. Hung, J. F. Wager, and D. A. Keszler, Chemistry of Materials **19,** 4023 (2007).

[2] P. T. Erslev, H. Q. Chiang, D. Hong, J. F. Wager, and J. D. Cohen, Journal of Non-Crystalline Solids **354,** 2801 (2008).

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CHAPTER V

SUMMARY AND DISCUSSION

Amorphous materials are at the same time incredibly complicated from a fundamental physics point of view and also extremely appealing as the foundation of new and improved electronic devices. Hydrogenated amorphous silicon (a-Si:H) is used in the transistors that drive most LCD displays in spite of relatively poor electron transport properties. This device development has been enabled by a fundamental understanding of the electronic structure. That comprehensive knowledge base is the result of many years of specialized experiments aimed specifically at understanding the properties and distribution of defect levels within the mobility gap. Amorphous oxide semiconductors (AOS) offer an entirely new system on which to test ideas and theories on the fundamental properties of disordered materials. While there are some similarities between a-Si:H and AOSs, there are also many distinct differences. Most notable, from a electronic transport perspective, the electron mean free path in a-Si:H is on the order of one bond length, whereas in AOS the mean free path can be more than ten times as much. Thus electronic properties such as mobility in AOSs can be considered much like those in crystalline materials, whereas a-Si:H requires the formalisms to be modified and relaxed.

A complete understanding of the density of states within the mobility gap of AOSs offers both a way to frame the electronic transport properties and also a basis for guiding the development of devices fabricated around these materials.

Admittance spectroscopy, drive level capacitance profiling (DLCP), transient photocapacitance spectroscopy (TPC), and modulated photocurrent spectroscopy (MPC)[1] were used to determine the density of states within the mobility gap of amorphous zinc tin oxide (ZTO) and indium gallium zinc oxide (IGZO). Although MPC was not able to be performed on our amorphous IGZO samples, the other measurements were sufficiently similar that it is likely that the Urbach edge of the conduction band tail is very steep as well. The device performance of transistors based on these materials can now be understood in relation to a very steep conduction band tail near 10 meV, a distribution of defects deep within the band gap, and a very broad valence band tail, as illustrated in Figure 5.1.

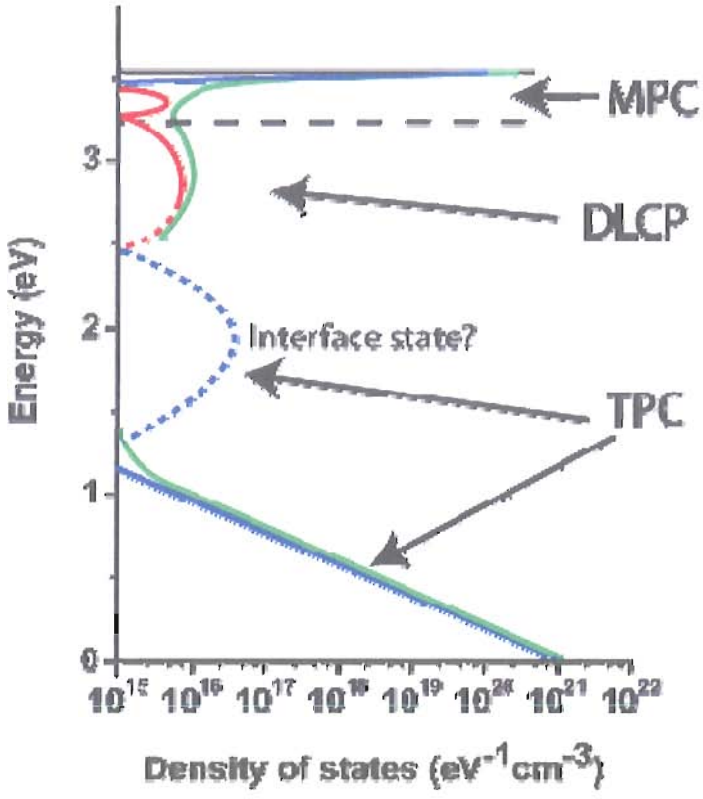

Figure 5.1: Density of states within the mobility gap of amorphous ZTO as compiled from DLCP, TPC and MPC measurements. The interface state disclosed by TPC is likely located at the insulator-AOS interface, rather than in the bulk of the semiconductor.

5.1. Density of States near the Conduction Band Edge

The density of states near the conduction band controls most of the electrical transport characteristics of an n-type semiconductor. Thus obtaining a fundamental knowledge and understanding of the electronic structure near the conduction band edge is crucial to optimizing devices based around AOS materials. It was only through the increased

energetic resolution of the Hattori[2] analysis of the MPC data that the steep conduction band tail was distinguished for amorphous ZTO. Additionally, low temperature measurements (less than 200 K) were required in order to distinguish the Urbach edge from the $k_BT/2$ energetic resolution of the measurement. Higher temperature measurements gave results which could have been incorrectly interpreted n terms of a much broader Urbach edge. While the Brüggemann[3] analysis did agree with the Hattori analysis at the lowest temperatures, there was not enough information to unambiguously identify the slope of the band tail versus the energetic resolution of the analysis technique. The Hattori analysis of the MPC data of ZTO at low temperatures also disclosed a band of defects located very near to the bottom of the Urbach tail. Again, without the low temperature measurements and enhanced resolution limit of the analysis technique, this feature would likely be smeared into the conduction band tail.

Another technique which was attempted to measure the conduction band tail in ZTO, space charge limited current (SCLC), gave hints of a very steep conduction band tail; however, again there was an ambiguity about which feature was actually being probed. These ambiguities arose from the use of the transistor triode structure: there were multiple possibilities as to the conduction path and no way to determine which path was dominating the measurement. Subsequent measurements of coplanar devices on ESR grade quartz substrates (similar to the triode structures, without the gate) did not reveal any signs of SCLC. Thus we concluded that in the transistor devices we were likely measuring a conduction path located in a narrow channel near the SiO_2/ZTO interface

rather than in the bulk of the ZTO, while in the ungated devices we were measuring the conduction primarily through the bulk of the ZTO. That is, it appears that the charge density within the conduction path of the gated devices could become high enough to show space charge limited behavior.

It is worth noting that attempts to determine the conduction band tail from the analysis of transistor device characteristics have produced results which do not agree with the results presented here. Hseih et. al.[4] derived very broad conduction band tail from IGZO transistor characteristics, ranging between 80 meV and 140 meV. This was later corrected by some of the authors as being too large and was replaced with a broad range of estimates from 20 meV to 100 meV[5]. This illustrates the difficulty in attempting to determine fundamental materials properties from transistor (or any three-terminal device) and co-planar geometry samples. The gate action of the transistor greatly influences the conduction properties of the material. Additionally, co-planar devices leave ambiguities about the conduction path between the source and drain. Thus exploring the basic properties of a material is best accomplished with two-terminal, sandwich geometry structures whenever possible.

5.2. Interface and Bulk Deep Defects

Admittance Spectroscopy

Admittance spectroscopy has revealed that processing conditions can greatly influence the density of states at the insulator-semiconductor interface. Under lower temperature post-deposition anneals, ZTO showed the very clear signature of defect trapping at this interface, a strongly bias dependent activation energy of the capacitive step. This activation energy varied from close to 1 eV to nearly 200 meV as the DC biased was increased. The density of interface defects could be estimated to be near $5*10^{11}$ $cm^{-2}eV^{-1}$. As the post-deposition annealing temperature was raised, the activation energy became much less bias-dependent, possibly indicating a band of deep defects in the bulk of the ZTO.

IGZO also exhibited characteristics of both interface and bulk defect trapping which varied as the fabrication process was varied. The sample fabricated on chemical vapor deposited SiO_2 exhibited a smooth transition of the activation energy from 800 meV to 200 meV as the DC bias was varied from 0 V to 5 V in the forward direction. Other samples processed differently did not show such strong DC bias dependence, indicating that there was likely a bulk deep defect present with an activation energy near 600 meV.

Drive Level Capacitance Profiling

Drive level capacitance profiling showed that typical free carrier densities for good ZTO and IGZO transistor devices were near $1x10^{15}$ cm^{-3}. Deep defect densities were typically several times this, in the mid-10^{15} cm^{-3} range. Both the free carrier and deep defect densities depended on the processing conditions, with higher post-deposition anneal temperatures yielding lower carrier densities. The signatures of interface defects were also noted in DLC and C-V profiling technique. In the PLD deposited ZTO, there was a clear "hump" in the C-V profiles while the DLC profiles were completely flat. This indicates a trapping state located at the interface which responds as the Fermi energy moves through the state, and then stops responding as the states become either completely filled or completely emptied. In the rf-sputtered ZTO, there was a clear shift in the DLC profiles as the measurement temperature was raised to near room temperature. This is significant because typically DLC profiles are generally insensitive to interface states.[6] Transistor devices based around ZTO channel layers could thus be strongly influenced by these interface states which respond so easily.

Transient Photocapacitance Spectroscopy

TPC has revealed a large, optically active, defect state located near the center of the mobility gap. This state is typically very broad, with a FWHM of near 0.8 eV. Because

of the MIS structure of samples which were investigated, it was not initially clear whether this state was located in the bulk of the semiconductor or at the semiconductor-insulator interface. A series of results have indicated that this feature is actually located at the interface rather than in the bulk of the material. Thus this broad band may be responsible for instabilities observed in ZTO thin-film transistors when the TFTs are subjected to light and bias stresses.[7]

When the series of rf-sputtered, co-deposited ZTO MIS devices were subjected to varying post-deposition anneal temperatures, the TPC spectra of all of the devices exhibited optically active sub-band gap features of differing magnitudes. The feature moved closer to mid-gap as the anneal temperature was increased, as was presented in the previous section.[8]

ZTO MIS devices fabricated by PLD exhibited behavior that appears to strongly indicate that the sub-gap feature is located at the insulator-semiconductor interface. The intensity of the defect changes by nearly two orders of magnitude as the biasing conditions are changed. By changing the pulsing conditions, different regions in the bulk of the sample are being probed. A small change in the magnitude of the defect feature would be expected due to the spatial sensitivity of the measurement technique. This change could not explain the observed large difference however. Thus the evidence points to the defect being located at the insulator-semiconductor interface.

A series of IGZO samples were grown on AlPO[9] insulators of varying thicknesses in order to investigate the spatial location of the sub-band gap defect feature in IGZO. As discussed in the previous chapter, the thickness of the insulator varied between 25 nm and 200 nm while the IGZO was 1.8 μm thick. The samples were found to have very similar deep defect and free carrier densities from capacitive profiling methods. The defect signal varied from nearly indistinguishable from the noise to very strong. Additionally, the magnitude of the defect feature in these samples exhibited a similar sort of bias dependence as was noted in the ZTO samples. This bias dependence, along with the large variation with different insulator thicknesses, suggests that the feature originates at the insulator-semiconductor interface. IGZO MIS devices fabricated on other substrates such as SiO_2 did not show any indication of a band of defects within the gap, again indicating the importance of the insulator-semiconductor junction.

5.3. Density of States near the Valence Band Edge

Transient photocapacitance spectroscopy has revealed that the valence band tail is very broad in the amorphous oxide semiconductors studied. The distribution of Urbach energies is actually quite narrow: all 25 ZTO and IGZO samples measured had Urbach

energies of 110 meV ± 20 meV, as was shown in figure 4.18. A series of co-deposited samples which were subjected to varying post-deposition anneal temperatures exhibited an interesting correlation: as the anneal temperature increased, the Urbach energy increased as well. This implies that the amount of structural disorder in the sample increases up to the point where the material begins to crystallize. The Urbach energies of the IGZO samples were all found to be very near those of the ZTO samples. They were all found to be much lower than the Urbach energies measured by Anwar[10] in the In_2O_3-SnO_2 materials system (between 170 meV and 230 meV).

Devices which have been fabricated out of these amorphous oxide materials thus far have been uni-polar n-type and thus unaffected by the large density of states near the valence band tail. However, further development of these materials for technology may be limited until a suitable p-type oxide semiconductor is found. One of the advantages of amorphous silicon is its ability to be doped both n-type and p-type, making p-n junctions very easy to form. The large density of states extending from the valence band edge will both limit the carrier concentration which can be achieved in a p-type AOS and also greatly limit the transport properties of holes. Thus in order to develop a p-type material based on these (Zn, Sn, Ga and In) there must be a way to neutralize the disorder. There has been progress in oxide semiconductors with different cations, such as Cd and Cu[11-13], however nothing has progressed as quickly as the semiconductors formed with heavy metal cations such as Zn, Sn, In and Ga.[14]

5.4. Notes

[1] H. Oheda, J. Appl. Phys. **52,** 6693 (1981).

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CHAPTER VI

CONCLUSIONS

The electronic states within the mobility gap of amorphous zinc tin oxide (ZTO) and indium gallium zinc oxide (IGZO) were successfully mapped using several different characterization methods. These materials belong to the larger class of transparent amorphous oxide semiconductors which are receiving a large amount of interest due to their attractive electronic transport properties; that is, the electron mobility is much greater than that of amorphous silicon in spite of their amorphous structure. In disordered and amorphous materials, the carrier transport properties are largely determined by the density of states within the mobility gap. Thus a fundamental understanding of the structure of the mid-gap density of states is crucial to the full development of technologies based on amorphous and disordered materials.

The class of materials "amorphous oxide semiconductors" as a whole only began in earnest in 1996.[1] Since then there has been significant progress towards developing them into transparent thin-film transistor (TFT) applications. Device mobilities of up to

80 $cm^2V^{-1}s^{-1}$ have been reported for IGZO and 50 $cm^2V^{-1}s^{-1}$ for ZTO in laboratory samples. However, stability and deposition issues have kept the mobility of TFTs in electronic devices to near that of a-Si:H, ~1-2 $cm^2V^{-1}s^{-1}$. An in-depth understanding of what processes are at work within the material will allow the development of more efficient and better performing devices. Transistor action has been modeled in an attempt to uncover the basic structure of the density of states within the mobility gap. However, it is very hard to derive basic materials properties from device action, and the results of these investigations have been largely unrepresentative of the true materials properties.

We have used a number of experiments on simplified device structures in order to determine the sub-gap structure in amorphous oxide semiconductors. Junction-capacitance based measurements were performed on metal-insulator-semiconductor (MIS) devices to investigate the free carrier and deep defect concentrations. The MIS structure allowed us to directly examine two critical components of a thin-film transistor: the bulk of the semiconductor and the insulator-semiconductor interface. Drive level capacitance profiling (DLCP) revealed that the free carrier density in both ZTO and IGZO is typically near $1x10^{15}$ cm^{-3} and tended to increase as the post-deposition anneal temperature was decreased. A broad band of bulk defects with density near $3x10^{15}$ cm^{-3} was also found, centered approximately 0.4 eV from the conduction band edge. Both admittance spectroscopy and DLCP indicated the presence of a significant amount of deep trapping defects at the insulator-semiconductor junction. The presence of these defects also appeared to depend on the fabrication conditions; less evidence of interface

traps appeared in devices that were subjected to higher annealing temperatures. In other sets of co-deposited MIS devices, ZTO fabricated on SiO_2 insulating layers showed the clear response of interfacial defects, whereas ZTO grown on ATO (gate dielectric composed of Al_2O_3 and TiO_2 super-lattice) did not show any evidence of interface states.

Several types of opto-electronic measurement techniques were also used to investigate the density of states within the mobility gap of these materials. Transient photocapacitance spectroscopy is a sub-gap optical absorption-like method where the capacitive response of a sample is analyzed after a voltage filling pulse with and without the presence of monochromatic light. TPC has revealed a very broad Urbach edge in the amorphous oxide semiconductors: 110±20 meV for 24 ZTO and IGZO devices. Like any sub-band gap optical absorption technique, this only shows the broader of the two band tails. In the case of AOSs, this is likely the valence band tail, as the conduction band consists mostly of s-orbitals from the metal cations, which are much more resistant to lattice disorder.[2] There were very few differences observed between the ZTO and IGZO TPC spectra, suggesting that this large Urbach edge could be present in most of the AOSs. While the performance of n-type thin film transistors will be unaffected by this large band tail, p-type oxides may be difficult to fabricate using the same heavy metal cations that are discussed here.

Finally, the density of states near the conduction band edge in ZTO was determined through modulated photocurrent spectroscopy (MPC).[3] MPC examines the amplitude and phase shift of the current generated in a sample in response to a modulated light source. A narrow conduction band tail with an Urbach energy of 10 meV was found as well as a defect feature located very close to the bottom of the Urbach tail. It was only with the enhanced energy resolution of the method developed by Hattori[4] that we were able to distinguish the band tail from that defect band.

Thus a complete picture of the density of states within the mobility gap of amorphous ZTO and IGZO has been determined. It is hoped that this fundamental understanding of the electronic structure within the gap will allow further development of technologies based around these materials by means of controlling carrier densities and deep defects located both at interfaces and in the bulk of the material.

6.1. Notes

[1] H. Hosono, M. Yasukawa, and H. Kawazoe, Journal of Non-Crystalline Solids **203,** 334 (1996).

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APPENDIX

SPACE CHARGE LIMITED CURRENT

Space-charge-limited current (SCLC) measurements were used in an attempt to examine the density of states near the conduction band edge in amorphous zinc tin oxide (ZTO). The density of states near the conduction band is the most relevant for n-type device performance. SCLC has been used to study a wide range of insulating and semiconducting materials; however results must be interpreted carefully. Thus an experiment was designed to investigate the temperature dependence of the SCLC characteristics which had been previously observed. The study was sparked by initial results examining IGZO films at Oregon State University and Samsung Electronics.[1, 2] Hong's results suggested that SCLC could indeed be used on amorphous oxide semiconductors and indicated an interesting result: that the total number of states within the conduction band tail remains the same in samples subjected to different post-deposition anneals, however the energetic distribution of the states varied. The Urbach energies in these samples were estimated to vary between 50 meV and 130 meV, becoming steeper with higher anneal temperatures.

A series of coplanar ZTO samples were fabricated on Si/SiO_2 substrates and then subjected to varying post-deposition anneal temperatures. Initial results showed behavior indicative of SCL conduction: a transition in the current vs. voltage (IV) curves from ohmic behavior at low biases ($I \propto V$) to super-linear behavior ($I \propto V^m$, $m>2$) at higher biases. Some samples even showed the transition at high biases to trap-limited currents, when m=2.[3] An example of this behavior is shown in Figure A.1, a ZTO device annealed at 600 °C.

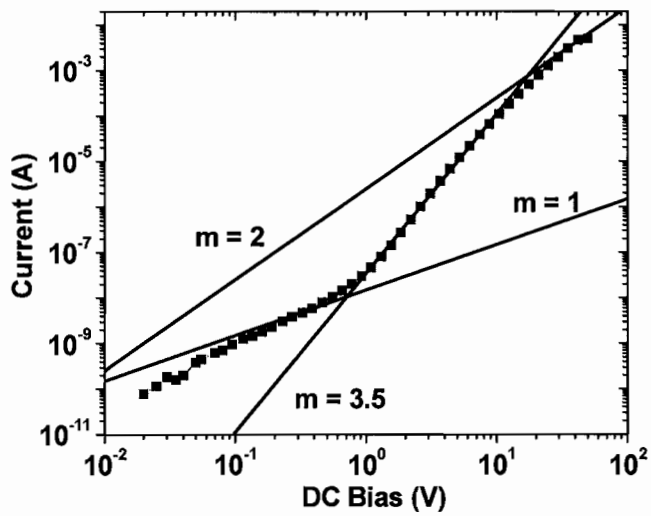


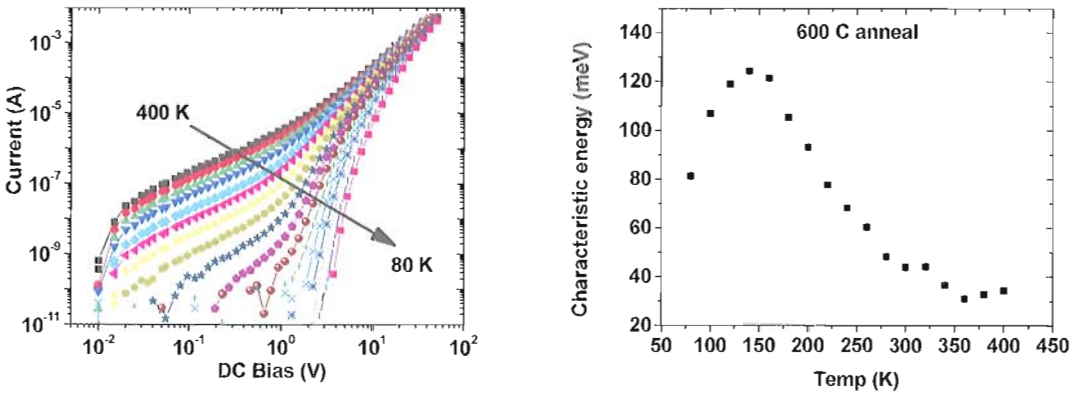
Figure A.1: Space-charge-limited current in coplanar ZTO device annealed at 600 °C.

As was discussed earlier in Chapter III, the exponent of the voltage can be converted to a characteristic energy in the following way:

$$m = 1 + \frac{E_{char}}{k_B T}$$

For the device in Figure A.1, a characteristic energy near 60 meV was found at the measurement temperature of 260 K. This characteristic energy is representative of the slope of the density of states near the Fermi energy.[4] Thus, if the characteristic energy is constant, independent of the measurement temperature, then the quantity being measured is likely related to the Urbach energy of the conduction band tail.

As such, the temperature dependent I-V measurements were undertaken over a range of temperatures from 80 K to 320 K. The results for the sample shown in Figure A.1 are shown in Figure A.2, along with the characteristic energies determined for each temperature. The characteristic energies are clearly very temperature dependent, indicating that the Fermi energy is not within a band tail, rather near some mid-gap feature.



(a) (b)

Figure A.2: (a) Temperature dependent IV characteristics of ZTO annealed at 600 °C. (b) Characteristic energies from IV curves varies greatly with measurement temperature.

Temperature dependent IV measurements were performed on a series of co-deposited samples which were then subjected to varying post-deposition anneal temperatures. All samples exhibited characteristics of SCLC. The characteristic energies derived from the IV curves are shown below in Figure A.3 for the varying anneal temperatures.

None of the samples showed the temperature-independent behavior which might indicate a band tail. This would imply that the Fermi energy is fairly deep in the band gap, rather than near the conduction band edge.

During this investigation, questions were raised about the influence of the Si gate on the

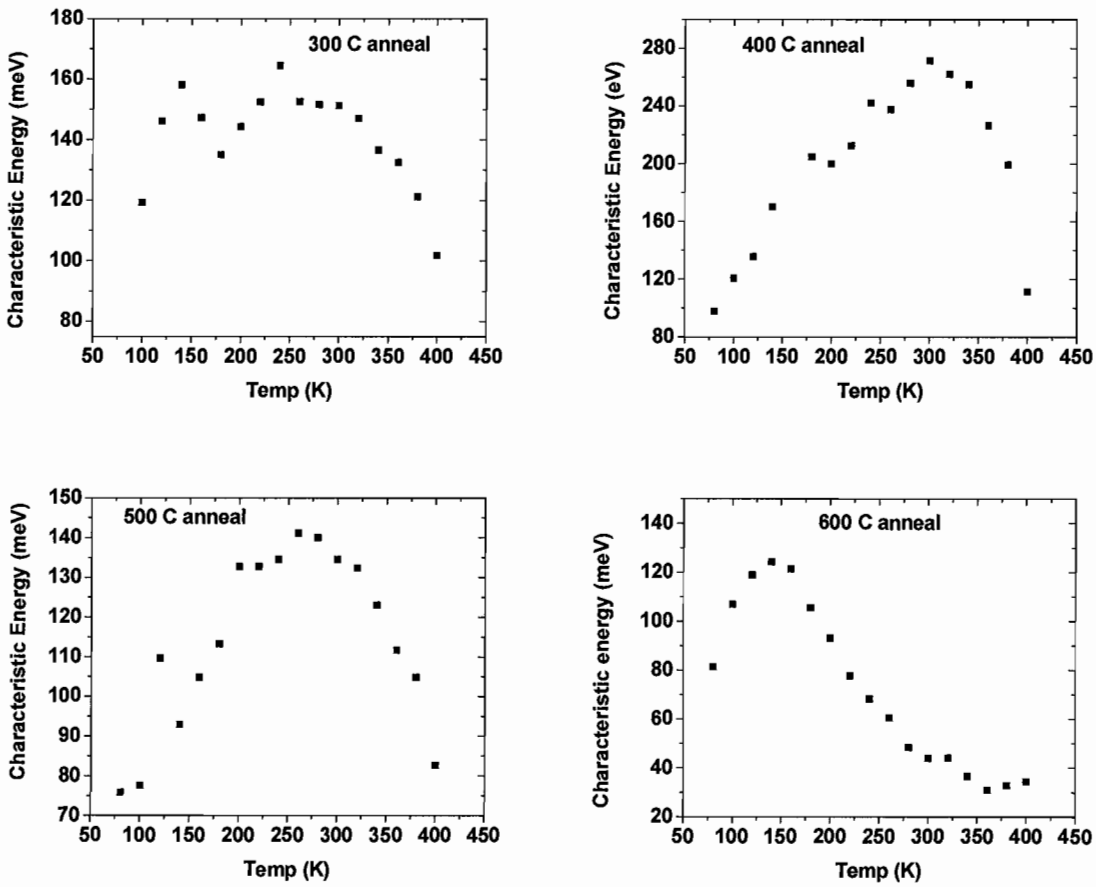


Figure A.3: Characteristic energies derived from SCLC measurements on a set of co-deposited ZTO samples subjected to varying post-deposition anneal temperatures. None of the samples show the temperature-independent behavior which would indicate a band tail.

conduction characteristics of the ZTO. Indeed, there was evidence that the conductivity of the channel was changing between measurements. This could be caused either by deep traps in the channel becoming charged, or by the gate becoming charged as well. In order to rule out the influence of the gate, a series of samples were co-deposited on ESR grade quartz (SiO_2) substrates and on the gated Si/SiO_2 substrates. Typical temperature dependent IV curves of this set of samples is shown in Figure A.4.

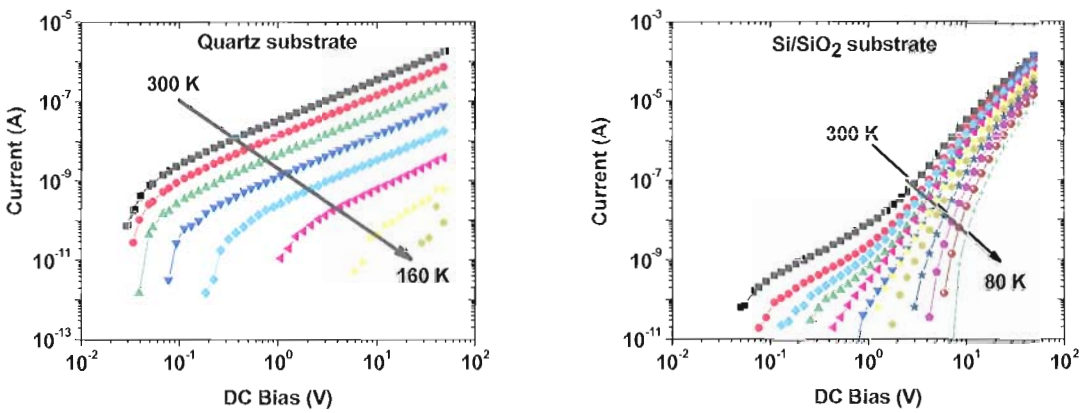


Figure A.4: Matched coplanar devices show very different IV characteristics depending on the substrate.

There is clearly no sign of space-charge-limited conduction in the sample on the quartz substrates. This suggests that the gate has a significant effect on the conduction in the first set of devices, even without any applied bias.

In order for SCLC to occur, the charge density induced in the conduction path by the applied bias must be sufficiently high. Our results suggest that perhaps a narrow conducting channel forms at the insulator-ZTO interface when the Si gate is present. When the Si gate is not present, the conduction occurs throughout the entire ZTO film. Thus for similar applied DC biases, the charge density within the narrow conduction path will be much greater than when the entire ZTO film is conducting. This is only one possible explanation for the results, however it illustrates the difficulties in understanding transport mechanisms when there may be more than one conducting path. While the SCLC measurements are likely revealing important information about the conduction mechanism in AOS TFTs, it is impossible to extract fundamental materials properties.

A.1. Notes

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