SOLUTION PROCESSING ELECTRONICS USING Si_6H_{12} INKS: POLY-SI TFTS AND CO-SI MOS CAPACITORS

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The Supervisory Committee certifies that this ***disquisition*** complies with North Dakota State University's regulations and meets the accepted standards for the degree of

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ABSTRACT

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The development of new materials and processes for electronic devices has been driven by the integrated circuit (IC) industry since the dawn of the computer era. After several decades of "Moore's Law"-type innovation, future miniaturization may be slowed down by materials and processing limitations. By way of comparison, the nascent field of flexible electronics is not driven by the smallest possible circuit dimension, but instead by cost and form-factor where features typical of 1970s CMOS (i.e., channel length ~ 10 μm) will enable flexible electronic technologies such as RFID, e-paper, photovoltaics and health monitoring devices. In this thesis, cyclohexasilane (Si_6H_{12}) is proposed and used as a key reagent in solution processing of poly-Si and Co-Si thin films with the former used as the active layer in thin film transistors (TFTs) and the latter as the gate metal in metal-oxide-semiconductor (MOS) capacitors. A work function of 4.356 eV was determined for the Co-Si thin films via capacitance-voltage (C-V) characterization which differs slightly from that extracted from ultraviolet photoemission spectroscopy (UPS) data (i.e., 4.8 eV). Simulation showed the difference between the C-V and UPS-derived data may be attributed to the existence of 8.3 x 10^{10} cm^{-2} interface charge density in the oxide-semiconductor junction. Poly-Si TFTs prepared using Si_6H_{12}-based inks maintained the following electrical attributes: field effect mobility of 0.1 $cm^2V^{-1}s^{-1}$; threshold voltage of 66 V; and, an on/off ratio of 1630. A BSIM3 version 3 NFET model was modified through global parametric extraction procedure to match the transfer characteristics of the

fabricated poly-Si TFT. It is anticipated that this model can be utilized for future design simulation for solution-processed poly-Si circuits.

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Above all, I'd like to thank family - my lovely wife, for enduring the 'grad life' with me, for always being there and my mom and dad for the unwavering affection and love.

DEDICATION

To my parents and my wife

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CHAPTER 1. INTRODUCTION

In this chapter, the trend of modern semiconductor research is reviewed with an emphasis on solution-processed electronics. The current state-of-the-art technologies in materials development derived from ink-based precursors are discussed in brief along with the organization of this thesis.

1.1. Solution-processed electronics:

For the last several decades, advancements in the field of electronics have been unprecedented and are likely to continue with special emphasis on growth areas such as the field of mobile computing consumer devices. Success in technology innovation can be attributed to the entire hierarchy of scientific know-how starting from new material utilization to efficient system level circuit design. Since the form factor and price of consumer electronics depends to a great extent on the fabrication techniques employed, it seems necessary to endeavor to introduce new material and processes so that the market may be expanded to offer cost-competitive solutions to consumer demands.

The majority of the semiconductor industry depends on single-crystal silicon for different device manufacture. Though conventional crystalline inorganic semiconductors offer higher charge carrier mobility, they are traditionally difficult to manufacture using low-cost processes since crystallization of most inorganic semiconductors requires high temperature treatments [1]. Also, traditional VLSI (very large scale integration) technology requires cleanroom processing such as chemical vapor deposition (CVD), plasma-enhanced chemical vapor deposition (PECVD) and optical lithography for the deposition

and patterning of device geometry. This technology hence encounters certain trade-offs between device performance, cost and compatibility when considering the transition to flexible substrates such as polyethylene terephthalate (PET). Research endeavors in the flexible electronics fields of radio frequency tags, sensors, photovoltaic cells and displays could be enabled if a low-cost alternative route to conventional Si processing technology was available.

In recent years, solution-processed electronics has gained much interest in comparison to conventional vacuum-based processes and vapor-phase deposition technologies given the potential to reduce production cost in a roll-to-roll manufacturing environment. Semiconductor devices produced using solution-based precursors have great potential in the field of large scale flexible displays and solar cells [2], [3]. Electronic devices derived from liquid inks has potential advantage over traditional VLSI fabrication technology given ease of fabrication, manufacture at ambient pressure, the possibility of low temperature processing and most importantly the ability to tune the mechanical and chemical properties to enhance device performance [4].

1.2. Basics of solution processing of semiconductor material:

Chemical solution deposition (CSD) has been used in the semiconductor industry for almost 20 years [5] and is considered as the focal factor in solution processing of electronics given the potential cost reductions achieved through liquid phase deposition of thin films. The process flow for CSD is shown in Figure 1-1 where independent, controllable processing variables are shown on the left, material states at different process points are illustrated within the boxes, and dependent processing behavior is shown in italic font on the right [6].

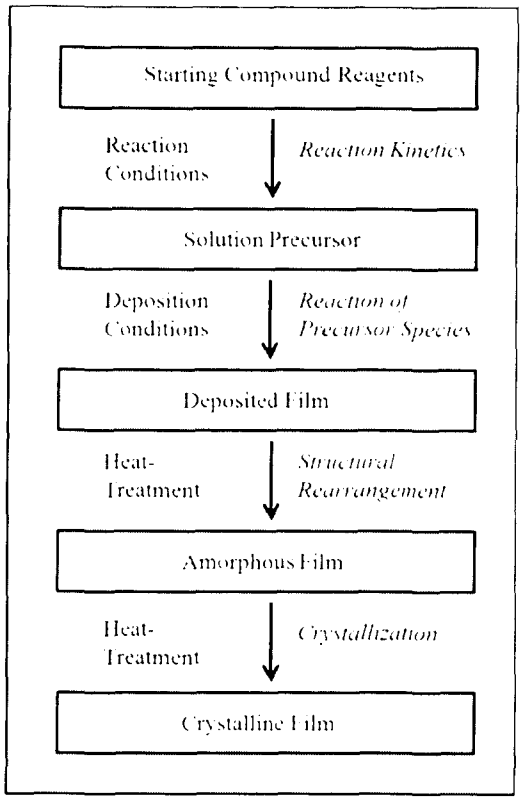

Figure 1-1: Processing stages of CSD of thin films [6].

CSD starts with selecting a chemical reagent which is added to a system in order to bring about a required reaction [7]. The chemistry of a candidate reagent compound will set the stage for what reactions will take place and what by-products will be formed. By controlling the reaction conditions (i.e., temperature, agitation, processing environment), the product of the reaction will differ.

After selection, this reagent is then mixed with other reagents and solvents to give a liquid precursor that allows the formation of the targeted material (e.g., metal, insulator or semiconductor). This solution is then deposited on a substrate (e.g., glass, Si wafer, plastic) using standard deposition techniques such as spin-coating, ink jet printing or screen

printing. Depending on the deposition conditions and ink chemistries involved, films with various attributes are formed. After the precursor film is formed, films are typically subjected to a post-deposition treatment (e.g., thermal anneal, laser anneal, UV irradiation) so that the inherent molecular structure is rearranged. At first, an amorphous state is realized where the film lacks long range order for the targeted phase or composition [8]. Further heat treatment at higher temperature allows the amorphous film to transition into the targeted crystalline phase that is applicable for semiconductor devices. In the following section, different techniques using in the semiconductor industry for solution processing are discussed.

1.3. Different techniques for depositing solution derived materials:

Solution-based processing of electronics is mainly realized in ambient temperature and pressure [9]. This attribute allows the possibility for large area film growth via continuous processing. The major techniques incorporated for solution processing are now discussed.

1.3.1. Ink-jet printing:

Ink-jet printing is based upon the ejection of precursor ink from a nozzle onto a substrate in a fashion that is similar to that used for printing on paper. Advantages of this approach include ease to incorporation into a processing scheme, non-contact and no-mask patterning, low temperature processing and low cost [10], [11]. Ink from a jet printer is usually deposited on the substrate in either continuous or drop-on-demand (DOD) method.

1.3.2. Screen printing:

In this method, an ink is poured onto a screen mesh that sits just above the substrate and the distance between the mesh and substrate is referred to as the standoff distance. The mesh contains openings that match the patterns to be printed. Printing occurs when a squeegee blade moves the ink bead across the screen mesh with downward pressure such that the ink fluid comes into contact with the substrate for a moment before snapping back into the original standoff distance. The blade pushes the ink through the mesh and correspondingly the ink is patterned with the help of a stencil to create open areas so that a certain feature could be transferred to the circuit board [12]. It is commonly used to produce not only conducting lines from inorganic materials but also create insulating and passivation layers [13].

1.3.3. Spin-coating:

In this method, the solution precursor liquid material is dispensed onto a stationary substrate in order to flood the surface. Then the substrate is spun at a very high speed which causes the liquid film to break - leaving a uniformly thin layer of precursor liquid coating the substrate. During spinning, the solvent evaporate leaving a thin precursor film in solid form. After spinning, the substrate is subjected to post-deposition thermal treatment to completely eliminate the solvent with subsequent processing leaving a uniform layer of the target material [14]. Spin coating is the most matured technology - being used for decades in photoresist deposition and patterning. With appropriate consideration of the ink formulation, spin coating is now used to deposit insulators, metals and semiconductors. Spin coating was used to deposit different materials in this work.

1.4. State-of-the-art of solution-processed materials:

At the current stage, the centerpiece of realizing printed electronics is developing new sets of materials— semiconductors, insulators, and conductors—that can be used in a solution form. In particular, there is marked interest is finding a suitable semiconductor material for the active layer of a thin film transistor (TFT) – an essential building block for printed electronics [15], [16]. In the following sections, the recent progress on the solution processed electronics materials is briefly reviewed.

1.4.1. Solution-processed metal:

TFT performance greatly depends on its electrical contacts. Traditionally a transistor is made with doped contacts that provide an ohmic electrode for the TFT in the ON state while affording a blocking contact when the TFT is turned OFF [17]. In addition, conductive tracks interconnecting different devices are also required to be made from low resistance, conducting materials. Traditionally this is done by sputtering a metal layer followed by subsequent patterning of the layer to create such electrodes and conductive paths. But sputtering gate electrode materials on active layer of TFTs sometime causes surface damage due to cracking and may result in device failure [18]. Hence, for the development of solution processed electronics, a liquid phase route to metal electrodes is necessary to ensure low temperature process for heat sensitive substrates [19]. Two major approaches have been advocated to do so. Firstly, suspensions of metal nanoparticles of diameters less than 5 nm are used such that low temperature processing results in sintering of the metals with concomitant thin film resistivity that approaches the bulk resistivity of the material [20]. Secondly, metal complex-based solutions are used whereby the

molecular nature of the compound (and the other processing components) allows conversion to the metal at low temperature [21].

There have been several reports on the research endeavors of solution processed conductive tracks and electrode materials. Ink jet printed silver lines with low curing temperature [22], transparent Ag nanowire mesh by the reduction of Ag nitrate in the presence of poly(vinyl pyrrolidone) (PVP) in ethylene glycol [23], highly conducting organic charge-transfer salt (tetrathiafulvalene) (tetracyanoquinodimethane) [(TTF)(TCNQ)] based contact material for solar cells [24], ink jet printed Cu lines from solution precursor copper hexanoate [25] as well as metal nanoclusters of palladium, platinum and gold synthesized by reducing the salt form of the required metal [26] have all been used in solution routes to conductive deposits. There have been, however, very few reports on solution-processed gate electrode material used specifically for inorganic TFTs.

Ag and Au nanoparticles inks for organic TFT electrodes have been reported [27],[28] but appear prone to large contact resistance which degrades device performance. $LaNiO_3$ (LNO) film was used as a gate electrode on which a PZT ferroelectric gate insulator was formed [29]. It is interesting that most of these reports concentrated on the formation technology and conductivity rather than characterizing the device-centric electrical characteristics such as work function or the interaction with interface state charges which can prove critical in designing high performance devices.

In modern electronics, metal silicides serve as essential role being used as interconnects and source/drain and gate contact pads in various devices such as TFTs and MOS capacitors. Silicides possess inherent properties that make them favorable candidates

for metal gate contact such as low resistivity, adhesion to Si, thermal stability, appropriate morphology for subsequent lithography or etching, oxidation resistance, good adhesion and low reaction with SiO_2, low interface stress [30]. Generally the silicides are formed as follows – a cleaned Si wafer (RCA or Ar sputter clean) is coated (sputtering or any vapor deposition technique) with a metal layer followed by a heat treatment to complete the phase transformation in the metal/Si junction to produce metal silicide.

For devices with line width of 0.18μm or smaller, $TiSi_2$, $CoSi_2$ and NiSi are being considered as possible candidate contact materials [31]. Cobalt silicide processes, specifically, were developed for 0.25/0.18μm technology nodes because the cobalt silicide process is less sensitive to the scaling of lateral feature sizes of CMOS transistors than Ti-Si processes [30]. But, during traditional silicidation, the silicon consumption increases the sheet resistivity of the underlying Si layer and decreases the effective contact area, which results in a constrained design space [30]. Nevertheless, deposition of Co metal typically requires standard clean room techniques in most cases which limits the applicability to the roll-to-roll processes. A solution route to cobalt silicide would allow consideration of this materials system for device engineers working in the continuous manufacturing environment.

1.4.2. Significance of metal work function:

Measurement of work function of a material is an essential part of the surface characterization and helps to forecast on device performance derived from such material [32]. Besides electrical resistance, the choice of gate metal electrode is determined by its work function since it is desirable that the contact presents smallest possible energy barrier

for carrier transport [33]. Also the work function value has impact on the physical fabrication process of the device and its stability too. In general, metals with high work function are not reactive and hence become difficult to pattern whereas metals with low work function are too much reactive resulting instability [34]. Using a metal with mid gap work function in bulk CMOS technology may result in undesirably high threshold voltage in TFT's. The acceptable range for work function was summarized as 4.1-4.4 eV for NMOS and 4.8-5.1eV for PMOS devices [35]. Hence, if a solution routed gate material candidate shows potential in terms of chemical stability, it is imperative that this material meets the work function requirement as discussed above.

1.4.3. Extraction of metal work function:

The work function of a material can be evaluated using different techniques like ultraviolet photoelectron spectroscopy (UPS) or capacitance-voltage (C-V) measurements. The work function of metals or metal-like thin films can be determined through a C-V measurement procedure where a metal-oxide-semiconductor (MOS) capacitor is fabricated and then subjected to a DC voltage sweep superimposed with an AC signal to extract the capacitance at different bias condition. When explored at different gate oxide thickness of the MOS capacitor, evaluation of the C-V characteristics allow determination of the work function of the metal. Not only that, C-V analyses allow a measure of the interface state condition of the dielectric-semiconductor junction. An understanding of the physics of an MOS capacitor allows an estimate for how the metal silicide material will behave in a potential active, transistor devices. In Chapter 2, the working principle of a MOS capacitor is described along with details on the parametric extraction theory used for Co-Si prepared by a solution process.

1.4.4. Solution processed active material:

Most recent attention on solution-processed semiconductors has focused on organic materials [36], [37]. Organic semiconductors can be divided into three main groups: (i) conjugated polymers; (ii) short polymer chains or oligomers; and, (iii) organic-inorganic hybrids. Organic semiconductors provide reasonable performance with mobilities as high as 0.89 $cm^2V^{-1}s^{-1}$ being achieved in p-type TFT channels comprised of solution-processed pentacene [38]. Though promising in terms of processing and cost, molecular organic semiconductor typically have a number of disadvantages including poor thermal and mechanical stability where mobility appears to be fundamentally limited by the weak van der Waals interactions between organic molecules versus stronger covalent and ionic bond for extended inorganic systems [39]. Also organic compounds are sensitive to moisture and oxygen and may result to degradation in device performance if not appropriately encapsulated [40]. On the contrary, inorganic semiconductors offer better device performance with higher mobility. Inorganic semiconductor nanowires, nanotubes, and nanorods are promising active materials for electronics [41]. Solution-processed metal oxides are also considered as potential candidates for active semiconductor layer with reports of zinc oxide ZnO [42], [43], indium zinc oxide In–Zn–O [44], [45] and indium tin oxide (In-Sn-O) [46] being used as the active channel materials.

There have been some reports where metal chalcogenide semiconductors are utilized as the active channel material for TFTs. A dispersion of cadmium selenide nanocrystals was employed to form thin CdSe films that formed an active gate alongside Cr/Au source/drain contact and n^+ Si bottom gate TFT [47]. More recently, semiconducting $SnS_{2-x}Se_x$ films derived from low temperature decomposition of highly soluble hydrazinium

precursors was reported to give TFTs with a high mobility of 10 cm^2V^{-1} s^{-1} [48]. However, the integration of metal chalcogenide materials into existing CMOS architectures is not straightforward and a solution route to Si would be a valuable addition to the scientific community.

An effort led by Shimoda resulted in a solution route to Si TFTs [49]. A solution containing cyclic silane compound (with formula Si_nX_m where n is 5 or more and m is an integer of n, 2n-2 or 2n), modified by boron or phosphorus dispersed in an organic solvent was deposited on to substrate via spin-coating. This film was then converted to silicon-based thin films with a post-deposition thermal treatment. One variant of this approach was to form poly-Si TFTs by ultraviolet (UV) light exposure of a solution containing Si_5H_{10}, cyclopentasilane (CPS) [50]. Here, the CPS solution was partially polymerized with UV irradiation to give a viscous solution that was then thermally treated to give a-Si with additional heating yielding polycrystalline Si thin films. It was suggested that such a technique can also utilize cyclohexasilane Si_6H_{12} to form the poly-Si active layer for the TFT [49]. In the present work, a TFT was fabricated using a technique similar to that described by Shimoda et al. [49], [50] but using an Si_6H_{12}- based ink.

1.5. Outline of the thesis:

The remainder of the thesis is organized as follows. In chapter 2, the MOS capacitor theory is discussed in detail along with the theoretical extraction procedure of work function and other physical parameters through C-V measurement. Chapter 3 presents the fabrication procedure of Si_6H_{12} derived Co-Si ink gated MOS capacitor with C-V measurement data extraction and work function determination of the Co-Si ink. Also, the

detailed analysis on the measured data is presented there. In chapter 4, Si_6H_{12} derived poly-Si TFT fabrication procedure and performance analysis is presented. The experimental results are matched with BSIM 3 version 3 NFET model through global parametric extraction procedure and the obtained results are presented in this chapter. Chapter 5 concludes the thesis with recommendations for future studies.

CHAPTER 2. CHARACTERIZATION OF METAL THROUGH METAL – OXIDE – SEMICONDUCTOR (MOS) CAPACITOR

In this chapter, the basic theory on the MOS capacitor is discussed. Also emphasis is given on how to extract physical and electrical characteristics of a metal through the capacitance-voltage (C-V) measurement of a MOS capacitor structure.

2.1. MOS capacitor:

The MOS heterostructure is the basis for metal-oxide semiconductor field effect transistors (MOSFET). MOS capacitors are made with a semiconductor substrate, a dielectric or insulator (example, SiO_2) and a metal or metal like gate electrode and a generic MOS capacitor structure is shown in Figure 2-1. These capacitors can be used to characterize different properties of the metal gate electrode, semiconductor-dielectric interface, dielectric quality etc. in order to define the operations of a MOSFET device.

2.2. Energy band diagram:

To understand and analyze the working principle of MOS capacitors, the energy band diagram and the C-V curves are usually considered. Hence it is necessary to have some insights on the energy band diagram of semiconductors.

Electrons in a single atom have discrete energy levels. The scenario considerably changes when two similar atoms are brought close together as the outer subshell of the atoms will start interacting with each other resulting in a split of the similar energy levels given Pauli's exclusion principle which states that each quantum state can be occupied by no more than one electron in an atom [51]. As more and more atoms are added into a larger crystal system, splitting of energy level continues and thereby results in almost continuous set of energy levels, which are referred to as an energy

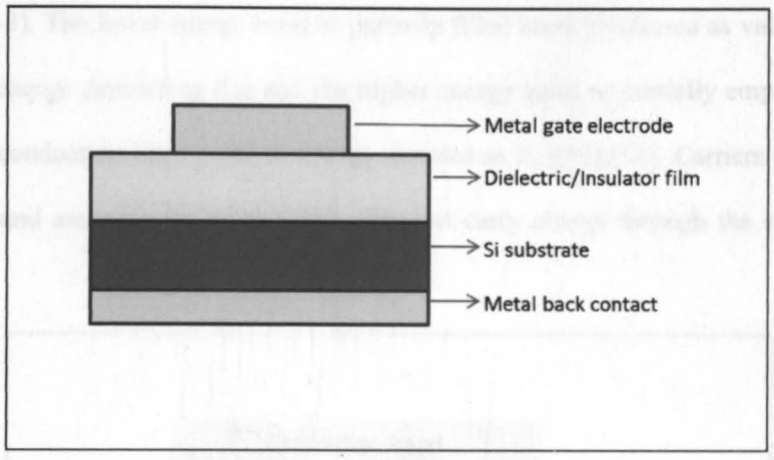

Figure 2 -1: Basic MOS capacitors structure.

band [52]. The formation of energy bands is depicted in Figure 2-2 which shows the progression of increasing number of energy states resulting in the formation of a 'many-atom' band system.

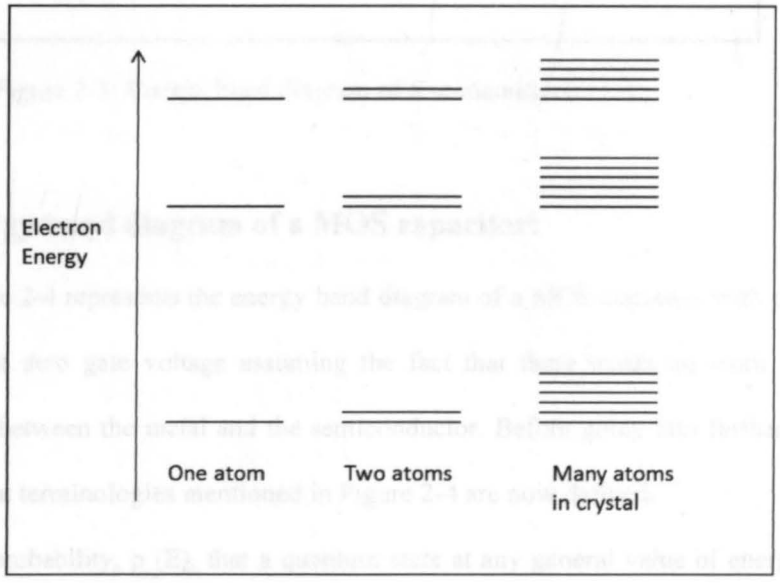

Figure 2-2: Energy levels of electrons of a system with many atoms [52].

In semiconductors, lower energy bands are usually filled first with higher energy bands remaining unoccupied. These two energy bands are separated by a gap where no energy states are available. The gap is called the band gap, E_g of the semiconductor

(Figure 2-3). The lower energy band or partially filled band is referred as valence band (with its energy denoted as E_V) and the higher energy band or partially empty band is regarded conduction band (with its energy denoted as E_C)[51],[52]. Carriers within the valence band are typically holes while electrons carry charge through the conduction band.

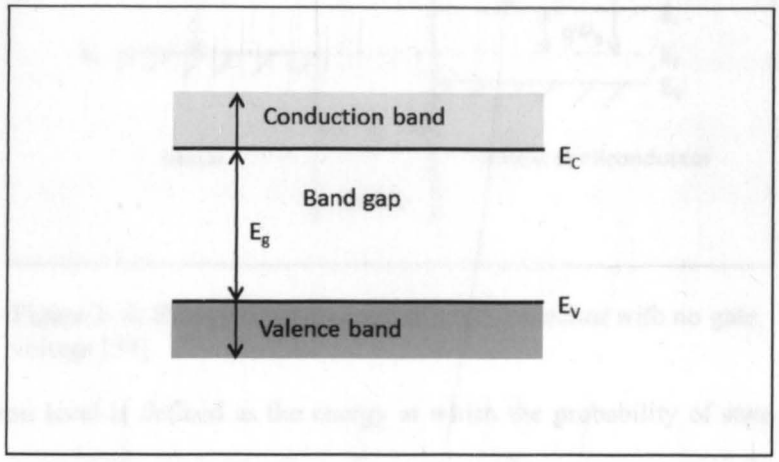

Figure 2-3: Energy band diagram of a semiconductor [1].

2.3. Energy band diagram of a MOS capacitor:

Figure 2-4 represents the energy band diagram of a MOS capacitor with p-type Si substrate at zero gate voltage assuming the fact that there exists no work function difference between the metal and the semiconductor. Before going into further details, the different terminologies mentioned in Figure 2-4 are now defined.

The probability, p (E), that a quantum state at any general value of energy, E, is occupied by an electron can be found by Fermi-Dirac distribution function [53]:

$$p(E) = \frac{1}{1+e^{\frac{E-E_f}{kT}}} \tag{2.1}$$

where E_f is the Fermi level or Fermi energy, k is the Boltzmann's constant and T is the absolute temperature in Kelvin.

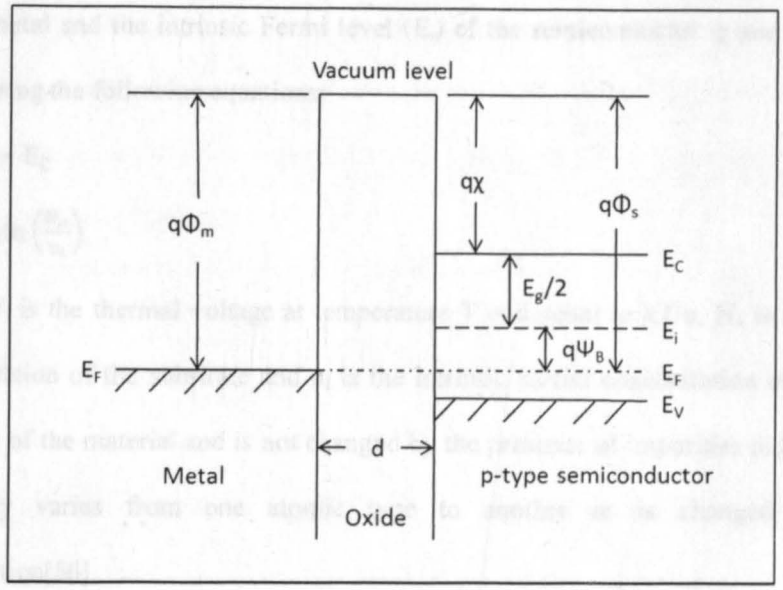

Figure 2- 4: Energy band diagram of MOS capacitor with no gate voltage [54].

Fermi level is defined as the energy at which the probability of state occupancy by an electron is exactly 50% [55] or more simply put, the Fermi level is the energy level at which the probability of finding an electron at T > 0K is 50% [56]. The Fermi level in intrinsic Si or in absence of doping is referred as intrinsic Fermi level, E_i.

From energy diagram perspective, the work function of a material is the amount of energy required to remove one electron from Fermi level to vacuum, that is, the energy difference between Fermi level and vacuum level. Mathematically, the work function (Φ) of a material is described as:

$$\Phi = E_o - E_f \quad (2.2)$$

where E_o is the vacuum energy level.

In Figure 2-4, the metal and semiconductor work functions are denoted as $q\Phi_m$ and $q\Phi_s$ respectively. The electron affinity ($q\chi$) is the energy difference between the bottom of the conduction band edge and the vacuum level in the semiconductor. Bulk potential or Fermi potential ($q\Psi_B$) is the energy difference between the Fermi level E_F

of the metal and the intrinsic Fermi level (E_i) of the semiconductor. χ and Ψ_B can be found using the following equations:

$$\chi = E_o - E_C \tag{2.3}$$

$$\Psi_B = V_t \ln\left(\frac{N_a}{n_i}\right) \tag{2.4}$$

where V_t is the thermal voltage at temperature T and equal to kT/q, N_a is the doping concentration of the substrate and n_i is the intrinsic carrier concentration of Si. χ is a property of the material and is not changed by the presence of impurities to any degree but only varies from one atomic type to another or is changed by alloy composition[56].

Figure 2-4 shows the work function of p-type Si can be easily extracted graphically as follows [56]:

$$\Phi_s = \chi_s + \frac{E_g}{2} + q\Psi_B \tag{2.5}$$

where χ_s is the electron affinity of silicon (4.05 eV) and E_g is the band gap energy of Si (1.12 eV). But when there is work function difference between the metal and the semiconductor, it causes distortion in the band shape and the energy band diagram changes from the one shown in Figure 2-4. If a metal and a semiconductor in a MOS structure are shorted together, there is charge flow between the materials until a potential is built up between the two which consequently counterbalances the difference of work function. This potential is referred as surface potential, Ψ_s, which represents the electrostatic voltage difference at the surface measured from the bulk intrinsic level E_i. Since there exists this electrostatic potential difference between the elements owing to the work function difference, band bending results in the interior of the structure and Ψ_s is a measure of the band bending. Because the metal is an equipotential region, no band bending occurs there. Therefore, the energy bands bend in the oxide and semiconductor regions exhibiting upward slope when the metal work

function is greater than the semiconductor work function (i.e., $\Phi_m > \Phi_s$) and a downward slope when $\Phi_m < \Phi_s$ [56]. For example, in the case of an Al-SiO_2-p-type Si MOS system where $\Phi_m < \Phi_s$, the bands bend downwards even under no applied gate voltage as depicted in Figure 2-5.

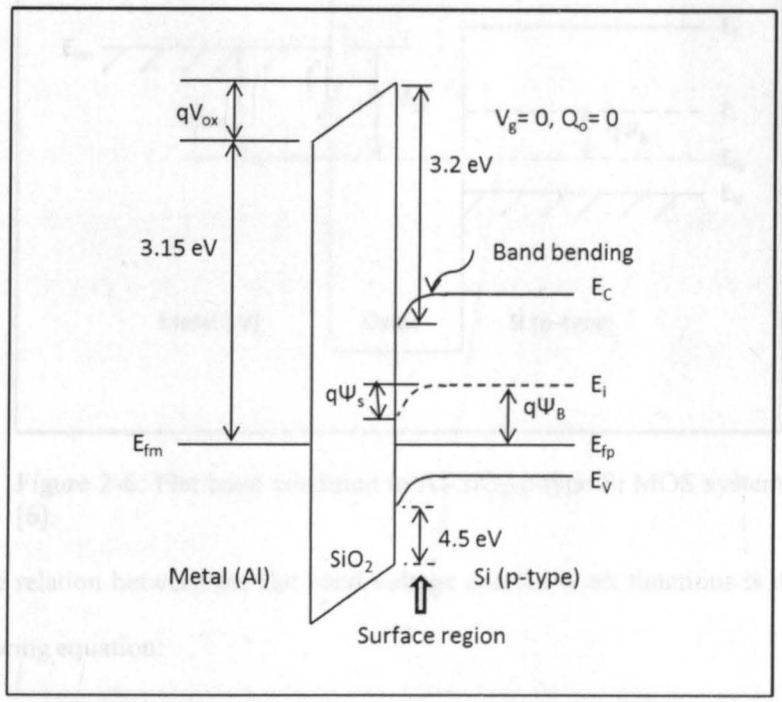

Figure 2-5: Energy band diagram of Al-SiO_2-p-type Si MOS system under zero gate bias, $V_g = 0$ and it is assumed that there exists no oxide charge, $Q_o = 0$ [56].

This band bending phenomenon also occurs due to the presence of oxide charge, Q_o. The band bending can be compensated by applying an external voltage, V_{FB}, which is simply equal to the work function difference between the metal and the semiconductor that caused the bend bending in the first place. Applying V_{FB} at the gate causes the bands to flatten over the entire MOS structure as shown in Figure 2-6. Hence flat band voltage is the amount of gate voltage that ensures zero surface potential ($\Psi_s=0$) with flat energy bands over the entire semiconductor surface [57]. Hence it is critically important to extract the amount of flat band voltage.

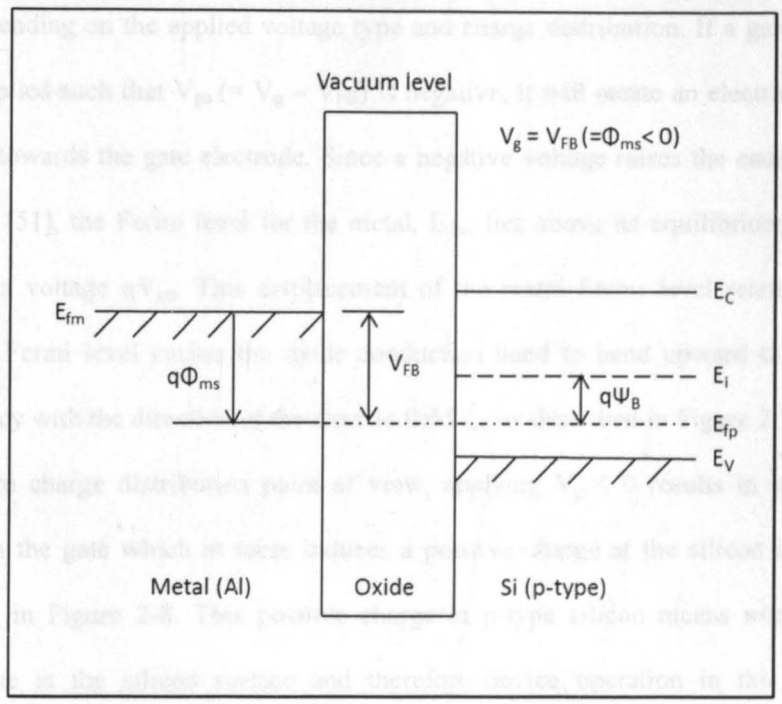

Figure 2-6: Flat band condition in Al-SiO_2-p-type Si MOS system [6].

The relation between the flat band voltage and the work functions is depicted in the following equation:

$$V_{FB} = \Phi_m - \Phi_s = \Phi_{ms} \tag{2.6}$$

Equation (2.6) considers the fact that there exists no oxide charge. If there is presence of oxide charges, equation (2.6) changes to following –

$$V_{FB} = \Phi_{ms} - \frac{Q_o}{C_{ox}} \tag{2.7}$$

where C_{ox} is the capacitance at strong accumulation. The phenomenon of accumulation will discussed in detail below. From equation (2.5) and (2.6) the relation between the metal and semiconductor work function can be deduced as follows:

$$\Phi_{ms} = \Phi_m - (\chi_s + \frac{E_g}{2} + q\Psi_B) \tag{2.8}$$

2.4. MOS capacitor at different gate bias:

When a MOS structure is biased with a non-zero voltage, three distinct states may

exist depending on the applied voltage type and charge distribution. If a gate voltage, V_g, is applied such that V_{go} (= $V_g - V_{FB}$) is negative, it will create an electric field ξ_{ox} pointing towards the gate electrode. Since a negative voltage raises the energy of the electrons [51], the Fermi level for the metal, E_{fm}, lies above its equilibrium position, E_{fmo}, by a voltage qV_{go}. This displacement of the metal Fermi level relative to the substrate Fermi level causes the oxide conduction band to bend upward to maintain consistency with the direction of the electric field ξ_{ox} as described in Figure 2-7.

From charge distribution point of view, applying $V_g < 0$ results in a negative charge on the gate which in turns induces a positive charge at the silicon surface as described in Figure 2-8. This positive charge in p-type silicon means excess holes accumulate at the silicon surface and therefore device operation in this mode is regarded as "accumulation". The hole concentration in p-type silicon, p, is governed by the following equation [56]:

$$p = n_i \exp\left(\frac{E_i - E_{fp}}{kT}\right) \tag{2.9}$$

where n_i = intrinsic carrier concentration of Si, k = Boltzmann's constant and T = temperature. As the hole concentration increases, the value ($E_i - E_{fp}$) also increases according to equation (2.9) resulting a band bending as shown in Figure 2-7.

When the applied gate voltage V_g is increased in such a way that V_{go} is positive, an electric field ξ_{ox} pointing from the gate to the substrate is created. ξ_{ox} raises the potential of the gate, lowering E_{fm} by the amount qV_{go} relative to the substrate Fermi level E_{fp}. This phenomenon causes downward bending in the oxide energy band, consistent with the direction of ξ_{ox} as depicted in Figure 2-9. From charge distribution point of view, the applied positive gate voltage repels holes from the silicon surface and in turns exposes the negatively charged acceptor ions [56],[58]. Since hole concentration decreases at the surface, from equation (2.9) it can be seen that (E_i- E_{fp})

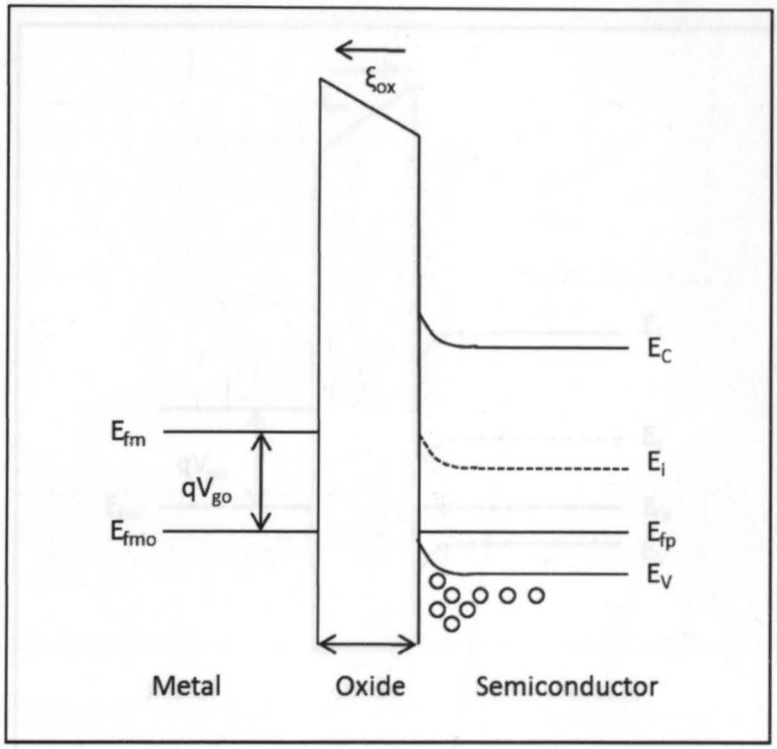

Figure 2-7: Energy band diagram of MOS capacitor in accumulation region.

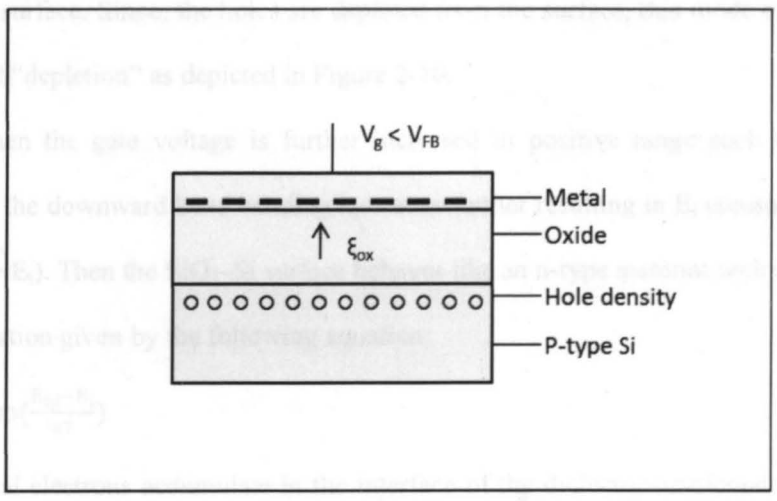

Figure 2-8: Charge distribution in MOS capacitor at accumulation region.

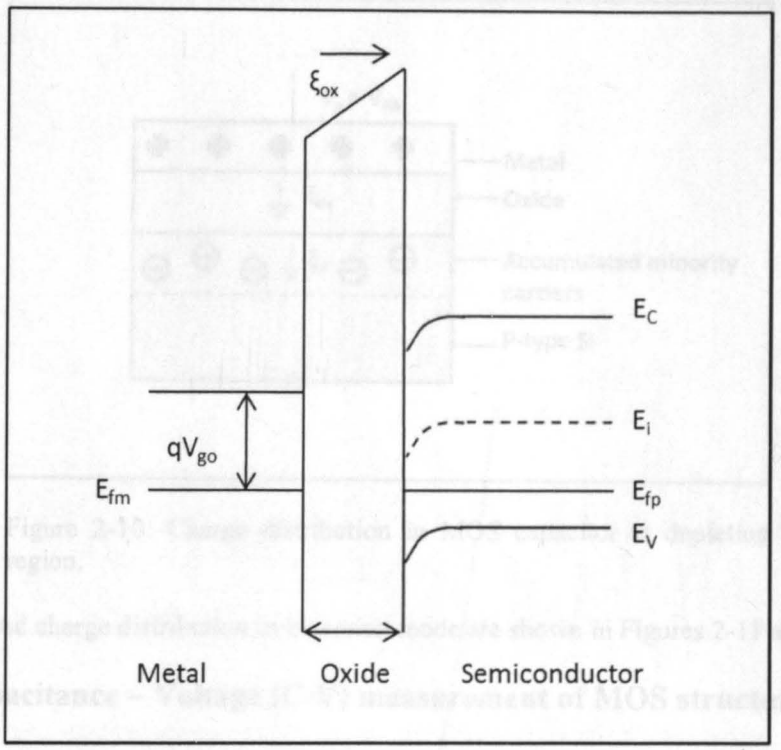

Figure 2-9: Energy band diagram of MOS capacitor in depletion region.

must decrease resulting in E_i coming closer to E_{fp} thereby bending the bands downward near the surface. Since, the holes are depleted from the surface, this mode of operation is termed "depletion" as depicted in Figure 2-10.

When the gate voltage is further increased in positive range such that V_{go} is positive, the downward band bending increases further resulting in E_i crossing over E_{fp} (i.e. $E_{fp} > E_i$). Then the SiO_2–Si surface behaves like an n-type material with an electron concentration given by the following equation:

$$n = n_i \exp\left(\frac{E_{fp} - E_i}{kT}\right) \quad (2.10)$$

Additional electrons accumulate in the interface of the dielectric-semiconductor along with minority carriers further depleting the majority holes. This n-type surface is formed not by doping but instead by inversion of the original p-type substrate due to the applied gate voltage. This mode of operation is termed inversion. The energy band

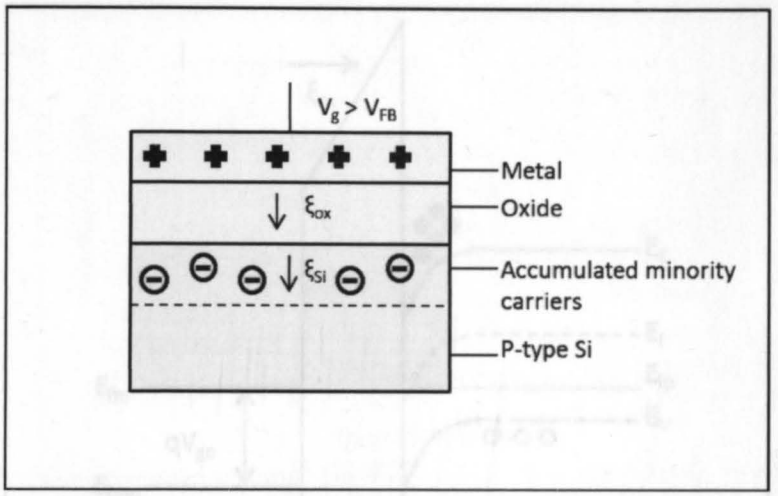

Figure 2-10: Charge distribution in MOS capacitor at depletion region.

diagram and charge distribution in inversion mode are shown in Figures 2-11 and 2-12.

2.5. Capacitance – Voltage (C-V) measurement of MOS structure:

C-V measurement is a basic technique to characterize semiconductor material extracting many electrical parameters which can be related to the physical parameters in the fabrication process, to bulk material or to the interface properties of the MOS structure [59],[60]. In this process, a MOS structure is subjected to DC voltage sweep, superimposed with an AC signal with variable frequency. The capacitance of the MOS structure is then probed for each oxide thickness giving a C-V curve for a MOS capacitor as shown generically in Figure 2-13. The three operational modes for MOS capacitors (accumulation, depletion and inversion) are labelled in Figure 2-13.

At high negative bias the MOS capacitor is under accumulation and the C-V curve approaches a constant value $C_g = C_{ox}$. This behaviour is akin to a parallel plate capacitor because of the assemblage of majority carriers at the dielectric-Si interface. The accumulation of high concentration of holes at the Si surface makes the surface metal-like and therefore acts as the second conductor electrode of the oxide capacitor opposite to the metal gate electrode [58]. C_{ox} can be determined as follows:

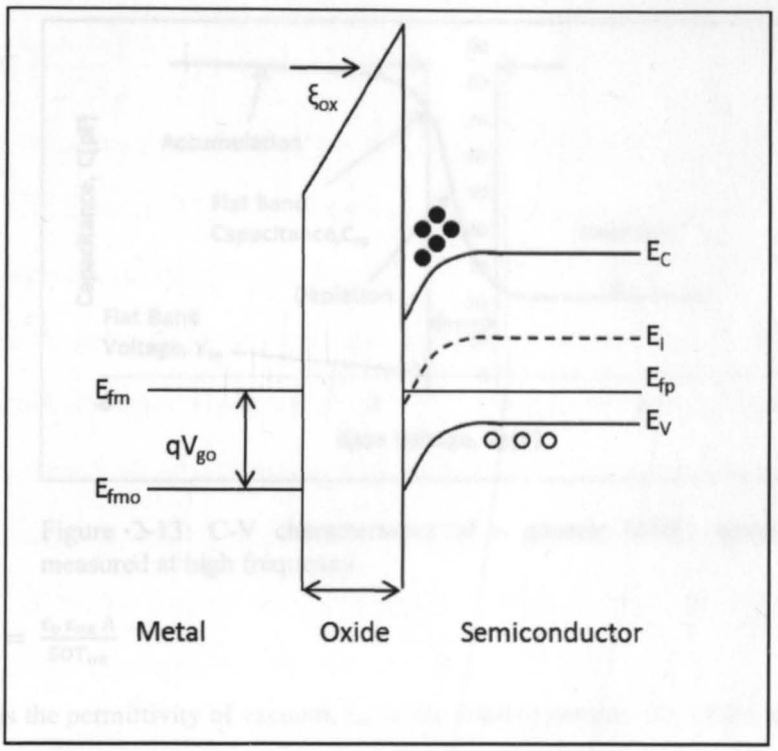

Figure 2-11: Energy band diagram of MOS capacitor in inversion region.

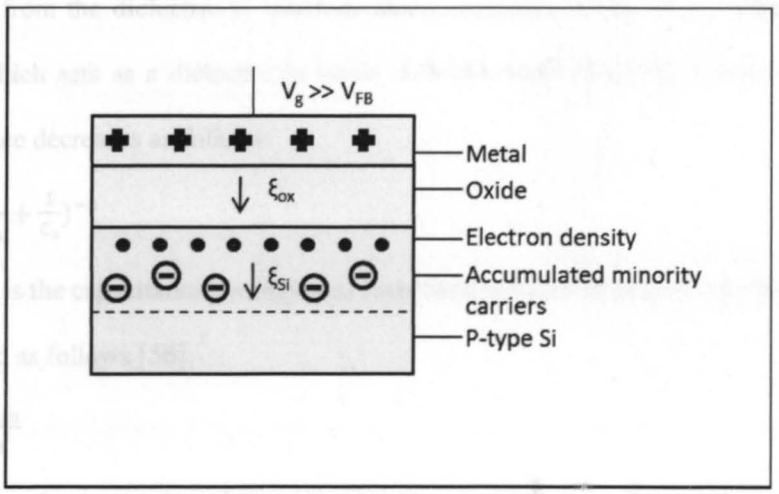

Figure 2-12: Charge distribution in MOS capacitor at inversion region.

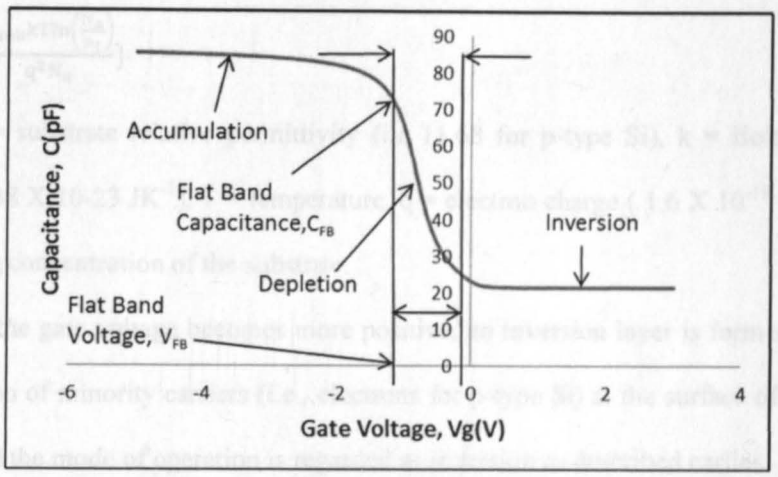

Figure 2-13: C-V characteristics of a generic MOS capacitor measured at high frequency.

$$C_g = C_{ox} = \frac{\varepsilon_o \varepsilon_{ox} A}{EOT_{ox}} \tag{2.11}$$

where ε_o is the permittivity of vacuum, ε_{ox} is the relative permittivity of the oxide layer (3.9 for SiO_2), A is the gate area of the capacitor and EOT_{ox} is the effective gate dielectric thickness.

As the voltage becomes less negative during the DC voltage sweep, holes are repulsed from the dielectric-Si interface and a depletion width, W_d, is formed in the region which acts as a dielectric in series with the oxide [54],[56]. Consequently the capacitance decreases as follows:

$$C_g = \left(\frac{1}{C_{ox}} + \frac{1}{C_s}\right)^{-1} \tag{2.12}$$

where C_s is the capacitance per unit area associated with the depletion region. C_s can be calculated as follows [56]:

$$C_s = \frac{\varepsilon_o \varepsilon_{sub}}{W_d} \tag{2.13}$$

where ε_o and ε_{sub} are the relative permittivity of vacuum and the substrate material, respectively. The maximum width of the depletion region, W_m can be obtained as follows [54]:

$$W_m = 2\sqrt{\{\frac{\varepsilon_{sub} kT \ln\left(\frac{N_a}{n_i}\right)}{q^2 N_a}\}} \quad (2.14)$$

where ε_{sub} = substrate relative permittivity (i.e 11.68 for p-type Si), k = Boltzmann constant (1.38 X 10-23 JK^{-1}), T = temperature, q = electron charge (1.6 X 10^{-19} C) and N_a = doping concentration of the substrate.

When the gate voltage becomes more positive, an inversion layer is formed from the generation of minority carriers (i.e., electrons for p-type Si) at the surface of the Si substrate and the mode of operation is regarded as inversion as described earlier.

Two cases may arise in this condition depending on the frequency of the imposed AC signal. If the DC gate voltage and AC signal are changed very slowly, the MOS capacitor always approaches equilibrium as the carriers in the inversion layer can easily follow the signals. In this instance, the capacitance values start from C_{ox} at accumulation, decrease to minimum value during depletion, and then increases back to C_{ox} as the surface becomes strongly inverted as shown in Figure 2-14.

When the imposed AC signal is high enough so that the inversion layer charge density cannot follow the variation, the charge density remains constant and the capacitance settles down to the minimum value as depicted in Figure 2-13. Figure 2-13 and Figure 2-14 represent high frequency (HF) and low frequency (LF) C-V curves, respectively.

2.6. Work function and other parameter extraction from C-V curve:

The flat-band condition can be evaluated from the depletion region C-V data through the calculation of flat-band capacitance, C_{FB}. To measure C_{FB}, it is necessary to find the extrinsic Debye length, λ, which is a measure of the distance over which a charge imbalance in a MOS capacitor is neutralized by majority carriers under steady state or equilibrium condition [61]. From the doping profile of the p-type substrate, an

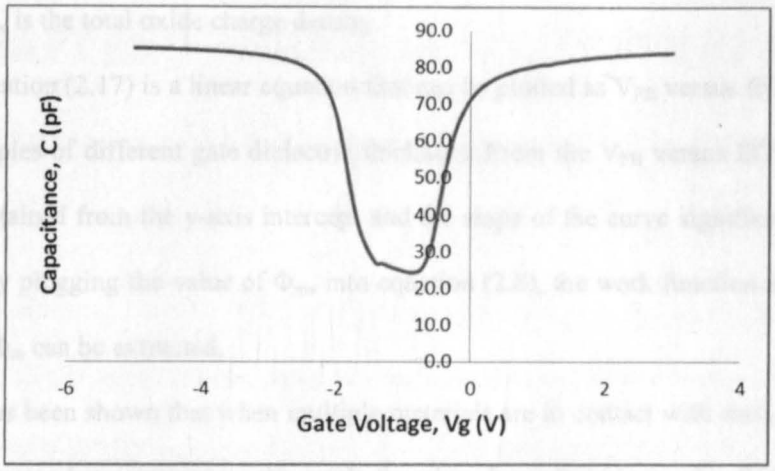

Figure 2-14: Generic C-V characteristics of a MOS capacitor measured at low frequency.

extrinsic Debye length can be calculated as follows:

$$\lambda = \sqrt{\left(\frac{\varepsilon_{sub}\varepsilon_o kT}{q^2 N_a}\right)} \tag{2.15}$$

Flat band capacitance C_{FB} is the capacitance of the MOS structure when the energy bands are flat near Si-SiO_2 interface [62] and is governed by the following equation:

$$C_{FB} = \frac{C_{ox}\left(\varepsilon_o \varepsilon_{sub} \times \frac{A}{\lambda}\right)}{C_{ox} + \left(\varepsilon_o \varepsilon_{sub} \times \frac{A}{\lambda}\right)} \tag{2.16}$$

where C_{ox} = gate oxide capacitance at strong accumulation region (F), and A = area of the capacitor gate region (m^2). Each value of C_{FB} corresponds to a specific value of V_{FB} that can be extracted from the C-V curve by drawing a tangent on the x-axis from the C_{FB} value. The x-axis intercept represents the V_{FB} value for a specific gate oxide thickness of the MOS structure. For different EOT_{ox}, corresponding V_{FB} can be extracted from C-V measurement data. The relation between metal to semiconductor work function difference, Φ_{ms} with V_{FB} and EOT_{ox} is well described in the following equation [51],[63]:

$$V_{FB} = \Phi_{ms} - \frac{Q_{ox} EOT_{ox}}{\varepsilon_{ox}} \tag{2.17}$$

where Q_{ox} is the total oxide charge density.

Equation (2.17) is a linear equation that can be plotted as V_{FB} versus EOT_{ox} curve with samples of different gate dielectric thickness. From the V_{FB} versus EOT_{ox} curve, Φ_{ms} is obtained from the y-axis intercept and the slope of the curve signifies the value of Q_{ox}. By plugging the value of Φ_{ms} into equation (2.8), the work function of the gate material Φ_m can be extracted.

It has been shown that when multiple materials are in contact with each other in a semiconductor heterostructure, the work function depends only on the first and last material of that structure [64]. Therefore in a MOS system, the metal to semiconductor work function difference depends only on the metal and semiconductor work function which can be seen from the theoretical analysis.

CHAPTER 3. FABRICATION, TESTING AND RESULT ANALYSIS OF MOS CAPACITOR

In this chapter, the fabrication and testing process for both Al gate and Co-Si gate MOS capacitor devices are discussed along with detailed characterization of the gate metals. C-V measurement data and ultraviolet photoemission spectroscopy (UPS) results are presented with an analytical discussion on the results.

3.1. Fabrication of Al gate MOS capacitor:

Al-gated MOS capacitors were fabricated to serve as a standard for the Co-Si MOS capacitor fabrication process. In this manner, the cleanroom routines needed to form MOS capacitors were developed to ensure there were no process related variants that would adversely affect measurements of new cobalt silicide materials. There have been several reports on MOS capacitor fabrication techniques to extract metal electrode work function [65-75]. The majority of these routines involve depositing an insulator layer (SiO_2 or other high k dielectric) on p-type or n-type Si wafers followed by patterned metal, alloy or nitride layer [67] as the top gate electrode. The works depicted in [73-75] specifically focus on MOS structures with Al gate electrode. Based on these studies, a generic structure for the Al gated MOS structure was devised and is shown in Figure 3-1. The process flow for Al gated MOS capacitor fabrication is depicted in Figure 3-2 and this approach was utilized in this thesis work.

3.1.1. Wafer preparation:

The fabrication started with a boron-doped p-type Si wafer (doping concentration

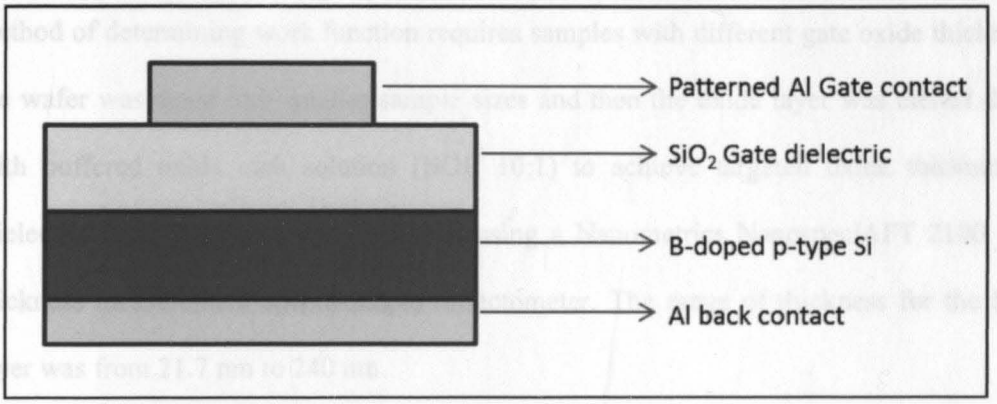

Figure 3-1: Generic MOS structure with Al gate.

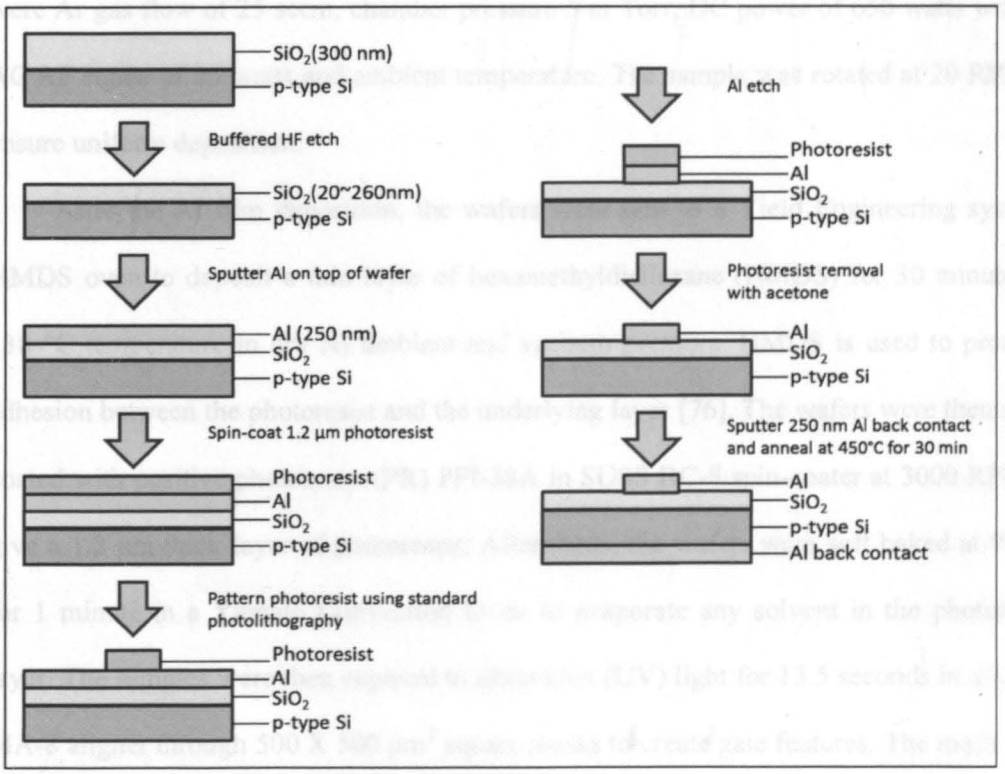

Figure 3-2: Process flow for Al gated MOS capacitor.

26 X 10^{14} cm^{-3}) with a 300 nm thick thermally evaporated SiO_2 layer on top. Since the C-V method of determining work function requires samples with different gate oxide thickness, the wafer was diced into smaller sample sizes and then the oxide layer was etched down with buffered oxide etch solution (BOE 10:1) to achieve targeted oxide thicknesses. Dielectric layer thickness was measured using a Nanometrics Nanospec/AFT 2100 film thickness measurement spectroscopic reflectometer. The range of thickness for the SiO_2 layer was from 21.7 nm to 240 nm.

3.1.2. Patterning Al gate:

The samples with variable gate oxide thicknesses were then deposited with 250 nm Al on top of the SiO_2 layer using Kurt J. Lesker CMS-18 sputterer. Process parameters were Ar gas flow of 25 sccm, chamber pressure 5 m Torr, DC power of 650 watts with an AC RF signal of 25 watts and ambient temperature. The sample was rotated at 20 RPM to ensure uniform deposition.

After the Al film deposition, the wafers were sent to a Yield Engineering systems HMDS oven to deposit a thin layer of hexamethyldisilazane (HMDS) for 30 minutes at 138 °C temperature in dry N_2 ambient and vacuum pressure. HMDS is used to promote adhesion between the photoresist and the underlying layer [76]. The wafers were then spin-coated with positive photoresist (PR) PFI-38A in SUSS RC-8 spin-coater at 3000 RPM to give a 1.2 μm thick layer of photoresist. Afterwards, the wafers were soft baked at 90 °C for 1 minute in a Yamato Convection Oven to evaporate any solvent in the photoresist layer. The samples were then exposed to ultraviolet (UV) light for 13.5 seconds in a SUSS MA-8 aligner through 500 X 500 μm^2 square masks to create gate features. The mask used for Al gate patterning is shown in Figure 3-3. All the samples went through soft bake

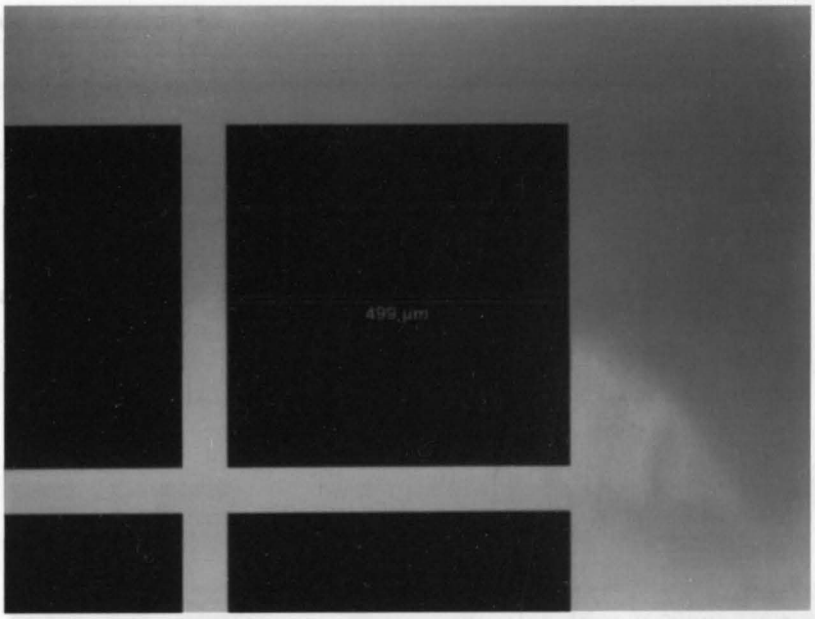

Figure 3-3: Optical microscopy photograph of the gate pattern mask for MOS capacitors.

again at 90 °C for 1 minute. The photoresist layer was developed using OPD 262 positive photoresist developer (tetramethylammonium hydroxide) for 20 seconds to remove all the exposed PR. Distilled (DI) water was used to rinse the samples followed by drying with flow N_2 gas. The samples were then subject to a hard bake at 120 ° C for 1 minute to ensure complete solvent elimination and to harden the PR. After the hard bake, all the samples were etched with Al Etch II w/SURF solution (phosphoric acid : water : acetic acid = 78: 12-16: 5-9). Thus the developed part of the Al layer was removed leaving only the Al gate patterns for the MOS capacitors. The PR was stripped from the samples by rinsing with acetone followed by isopropanol with a final drying using flowing N_2 gas.

3.1.3. Back contact deposition and heat treatment:

To ensure that the MOS capacitors have a good back contact that is necessary for electrical testing, 250 nm of Al layer was deposited using a Kurt J. Lesker CMS-18 sputterer with a deposition of 714 seconds followed by an argon (Ar) etch to remove any

residue oxide or contaminants. Then the samples were annealed at 450 °C for 30 minutes in a tube furnace to create ohmic contact. It has been reported that Al readily reacts with the native oxide on the Si surface to produce Al_2O_3 that diffuses the oxide into the bulk of the Al and allows fresh Al to diffuse into the Si interface resulting a very low resistance ohmic contact [77]. An optical microscopy photograph of Al gated MOS capacitor samples is shown in Figure 3-4.

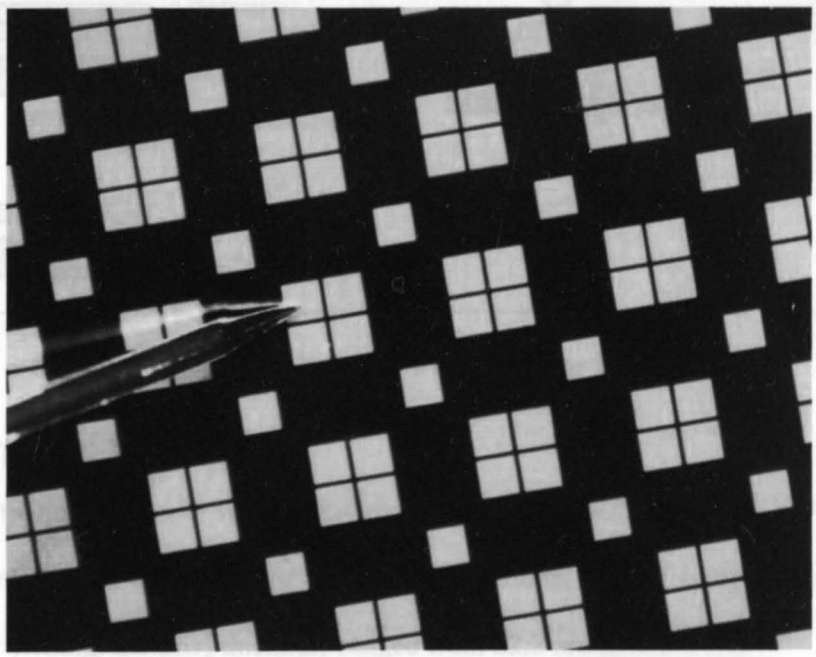

Figure 3-4: Optical microscopy photograph of Al gated MOS capacitor samples with a probe touching a gate pattern.

3.2. Co-Si gated MOS capacitor fabrication process:

The structure of Co-Si gated MOS capacitor was formulated similar to the Al gated MOS capacitor with the exception that the Al gate was replaced with a solution processed Co-Si gate. The process flow of Co-Si gated MOS fabrication process is described in Figure 3-5 which is discussed in the following sections.

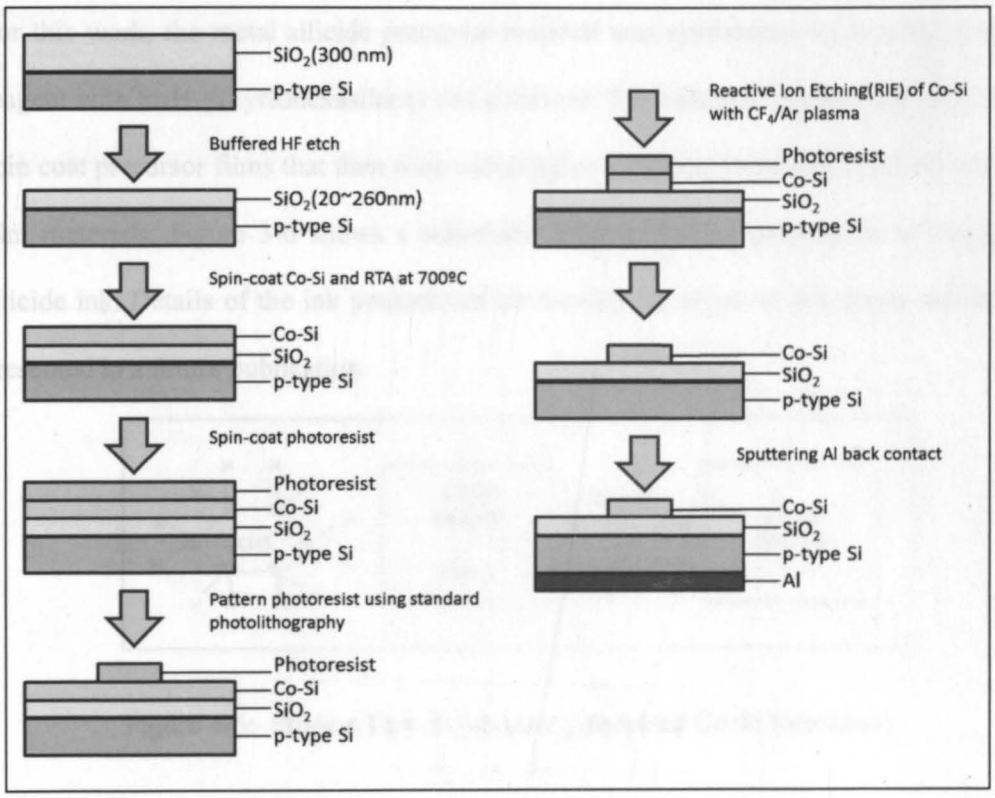

Figure 3-5: Process flow of Co-Si gated MOS capacitor fabrication.

3.2.1. Wafer preparation:

Boron-doped p-type Si wafers (doping concentration of 26 X 10^{14} cm^{-3}) with 300 nm thermally evaporated SiO_2 layer were prepared in similar manner as described in section 3.1.1. After etching, the SiO_2 thickness ranged from 22.2 nm to 236.9 nm.

3.2.2. Co-Si gate patterning:

3.2.2.1. Liquid phase cobalt silicide (Co-Si) preparation:

Solution-processing of cobalt silicide differs from traditional silicide formation technology. Currently, $CoSi_2$ thin films are produced by thermal treatment of a cobalt film on a silicon wafer with the metal deposited using molecular beam epitaxy (MBE), reactive deposition epitaxy (RDE), solid phase epitaxy (SPE), sputtering or evaporation [78-80].

For this work, the metal silicide precursor material was synthesized by reacting a cobalt reagent with Si_6H_{12} (cyclohexasilane) and a solvent. The resultant viscous ink was used to spin coat precursor films that then were subjected to a thermal treatment to give Co-Si thin film materials. Figure 3-6 shows a schematic diagram for the preparation of the cobalt silicide ink. Details of the ink preparation are beyond the scope of this thesis and will be presented in a future publication.

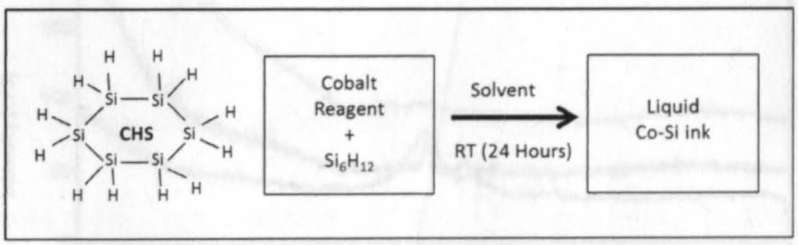

Figure 3-6: Process flow for solution processed Co-Si formation.

3.2.2.2. Co-Si deposition:

The cobalt silicide ink was spin-coated on to the SiO_2 layer of the samples at 3000 RPM for 30 seconds. The precursor film was thermally transformed into Co-Si phase via rapid thermal annealing (RTA) at 700 °C for 60 sec in a nitrogen glove box. The bulk resistance of the Co-Si film was measured as 28.255 Ω and the sheet resistance was found 128.051 Ω/square. Glancing angle x-ray diffraction (XRD) characterization of the metal-like layer showed broad peaks that correlate to a mixture of amorphous CoSi and $CoSi_2$. Figure 3-7 shows XRD data representative of the films produced in this study. The samples were then sent to the HMDS chamber for adhesion promotion followed by a spin-coat with 1.25 μm thin layer of positive PR PFI-38A at 3000 RPM. After a soft bake at 90 °C for 1 minute, the samples were exposed to UV for 13.5 seconds through 500 X 500 μm^2 masks

to create the gate features. Then the exposed PR on the samples was developed for 20 seconds with OPD 262 positive PR developer followed by a contact bake at 90 °C for 1 minute. All the wafers were rinsed with DI water and dried in liquid N_2 flow followed by a hard bake at 120°C for 1 minute to remove any solvent on the surface.

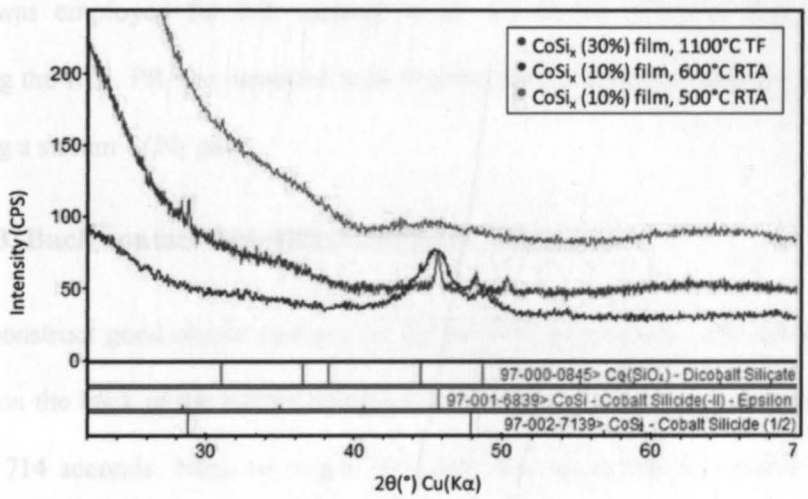

Figure 3-7: X-ray diffraction (XRD) data for thin films after RTA at 700 °C for 30 sec under N_2.

3.2.2.3. Co-Si etch:

There have been several reports of research endeavors describing the etching method for $CoSi_2$ and other cobalt silicides [81],[82],[84]. But these reports involved acid-based isotropic etching which is non-directional and can result in significant surface roughness [85]. In addition, wet etch processes are often temperature and agitation sensitive which complicated control of the lateral and vertical geometries [86]. An anisotropic (directional) reactive ion etch (RIE) method for $CoSi_2$ was reported that uses CF_4/Ar plasma and an RF power up to 90 watts [83]. Since anisotropic etching is insensitive to agitation and provides good lateral and vertical geometry control, this method was selected for the present study

of solution processed Co-Si. A test structure with spin-coated Co-Si layer on glass substrate was etched with CF_4/Ar plasma (70 sccm : 30 sccm) at 100 W RF power and 50 mbar pressure in a Trion Phantom RIE Plasma etcher. An etch rate of 11.8 nm/min was observed for Co-Si with no noticeable impact on the underlying glass substrate. This protocol was employed for RIE etching of all Co-Si thin films in this study. After completing the RIE, PR was removed with acetone and isopropanol and the samples were dried using a stream of N_2 gas.

3.2.3. Back contact deposition and heat treatment:

To construct good ohmic contacts on the back of the samples, 250 nm Al layer was sputtered on the back of the wafers using a Kurt J. Lesker CMS-8 sputterer with a sputter period of 714 seconds. Next, an argon (Ar) etch was employed to remove any residue oxide or contaminants. The ohmic contact was formed during a thermal treatment at 450 °C for 30 minutes in a N_2-purged tube furnace. Figure 3-8 shows an optical micrograph of the top of a typical Co-Si gated MOS capacitor structure.

3.3. Testing and data extraction:

3.3.1. C-V measurement:

High frequency (HF) C-V and low frequency (LF) C-V (quasi-static) measurements were carried out for both Al and Co-Si gated MOS capacitors using an Agilent B1500A semiconductor tester. A DC voltage was swept from -5 to 3 V whereas an AC signal of 50 mV amplitude and varying frequency from 1 kHz to 5 MHz was imposed to observe the various characteristics of the MOS capacitors. The system was calibrated to correct for

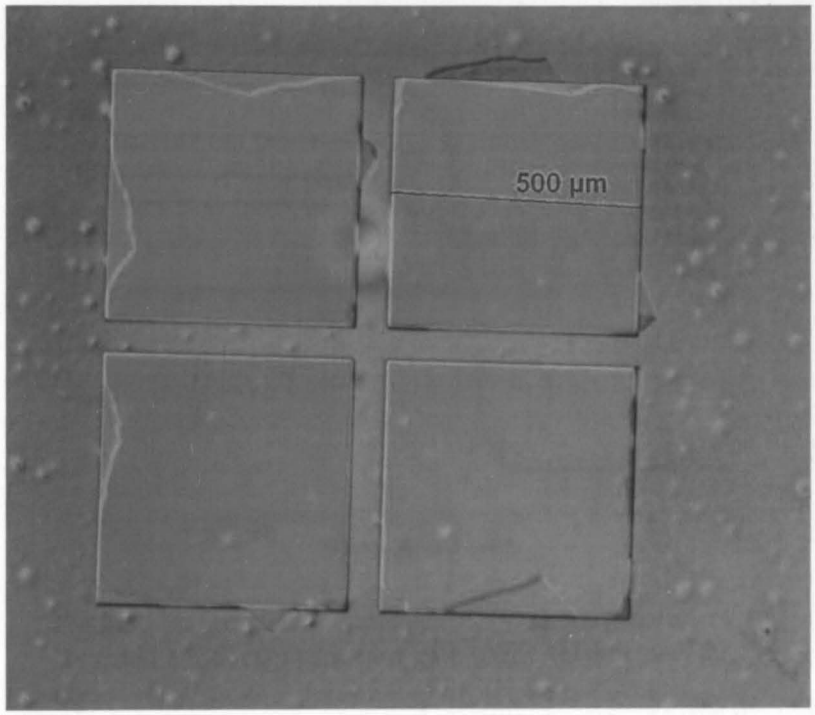

Figure 3-8: Optical microscopy photograph of the test structure for Co-Si MOS capacitor.

phase error, stray admittance and residual impedance. A total of 66 samples of Al gated MOS capacitors and 58 samples of Co-Si gated MOS capacitors with different gate oxide thickness were subjected to the C-V measurement.

In Figure 3-9, the C-V characteristics of Al gated MOS capacitor with gate oxide thickness of 23 nm is shown at different frequencies. As expected, higher frequency gave lower capacitance values whereas lower frequencies gave higher capacitance. This is consistent with the following relationship between capacitance, C and frequency, f –

$$C \propto \frac{1}{f} \tag{3.1}$$

C-V data for Al-gated MOS capacitors with variable gate oxide thickness ranging

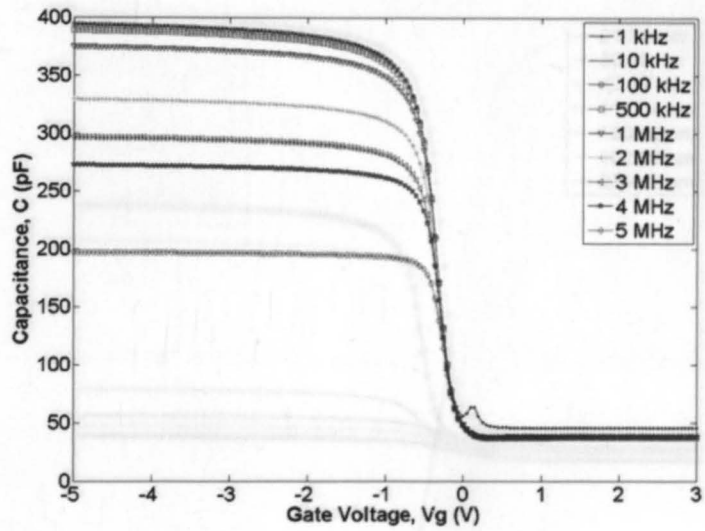

Figure 3-9: Frequency dependent C-V characteristics of Al gated MOS capacitor at a gate oxide thickness of 23 nm.

from 21.8 nm to 239.1 nm are shown in Figure 3-10. Since the capacitance is inversely proportional to gate oxide thickness according to equation (2.10), higher capacitance is observed with lower gate oxide thickness. Moreover, in Figure 3-9, a constant C_{ox} was noted from gate voltage (V_g) -5 V to -1 V indicating "accumulation" mode of operation where the majority carriers in the p-type semiconductor silicon wafer (i.e., holes) are accumulated at the Si/SiO_2 interface with the device acting as a parallel plate capacitor. A depletion of the majority carriers is noted for V_g from -1 to 0 V where the capacitance drops as the minority carriers are attracted to the interface signifying the "depletion" mode of operation. Forward bias of the gate gives an inversion in the type of surface conductivity where the minority carriers now dominate the Si/SiO_2 interface referring the onset of "inversion" mode of operation as discussed in chapter 2.

If the minority carriers are somehow rapidly supplied to the Si/SiO2 interface, a rise in the capacitance towards the value of Cox can be observed in the inversion region instead

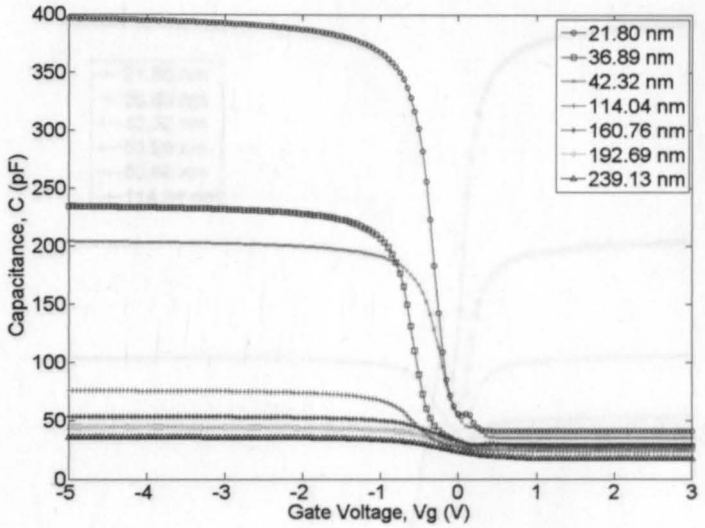

Figure 3-10: Gate oxide thickness dependent C-V characteristics of Al gated MOS capacitor at 1 KHz.

of remaining to flat capacitance value. Because of the increased density, minority carriers can follow the signal frequency. This supply can be created through optical generation or illumination which can be observed in Figure 3-11. This test was identical to that shown for Figure 3-10 but a light source was provided during the test. Because of the luminance, excess minority carriers tend to increase the capacitance to C_{ox} above 0 V. Similar C-V curves were obtained for Co-Si gated MOS capacitors as shown Figure 3-12 and Figure 3-13 where gate oxide thickness dependent C-V characteristics and frequency dependent C-V characteristics are depicted. Akin to the data for Al-gated MOS capacitors, higher capacitance was observed in lower frequency and lower gate oxide thickness delivered higher capacitance.

The conductance technique is considered to be one of the most sensitive technique in measuring interface state density and other interfacial parameters [87],[88]. In Figure 3-14

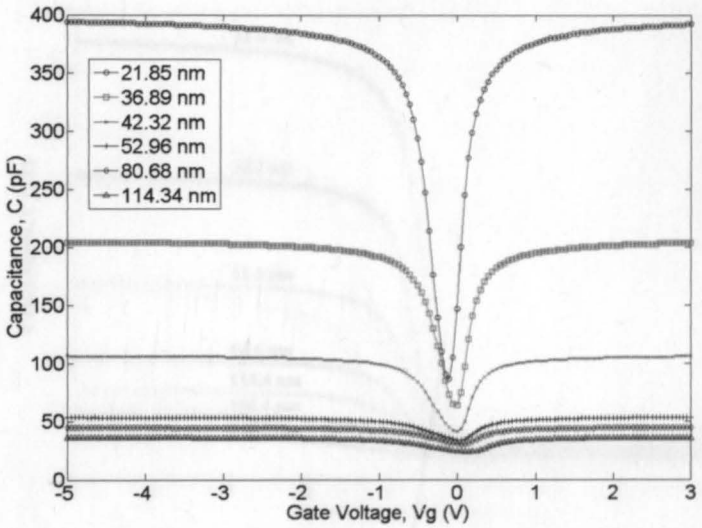

Figure 3-11: Gate oxide thickness dependent C-V characteristics of Al gated MOS capacitor at 1 KHz with room lights turned on.

and Figure 3-15, the variation of conductance in Co-Si gated MOS capacitors with changing frequency and gate oxide thickness respectively are shown. The upturn of the conductance at large negative bias may correspond to tunneling currents when metal electrode Fermi level intersects the conduction band edges [89]. It is evident from Figure 3-14 that conductance is proportional to frequency since at higher frequency, higher conductance is observed. It is interesting to note that the conductance remains constant up to almost -1 V and gradually increases to higher values as shown in Figure 3-15. However, the curve does not depict any specific regularity or trend in progression at positive gate bias.

3.3.2. Extraction of parameters from C-V measurement:

The goal of the C-V measurement is to extract physical and electrical properties of

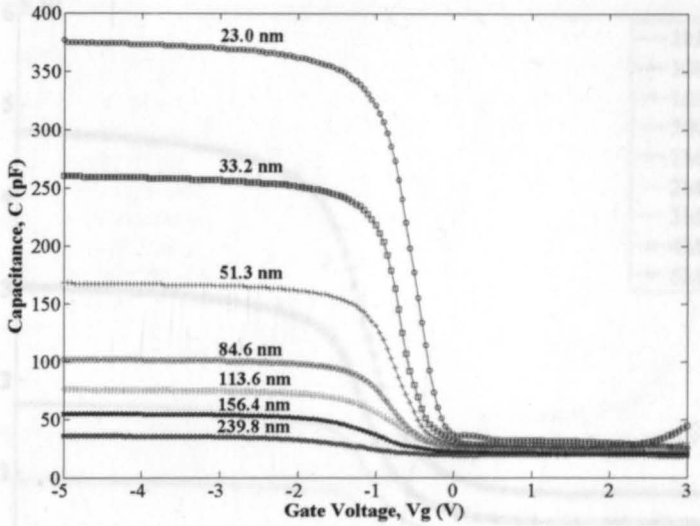

Figure 3-12: Gate oxide thickness dependent C-V characteristics of Co-Si gated MOS capacitor at 1 KHz.

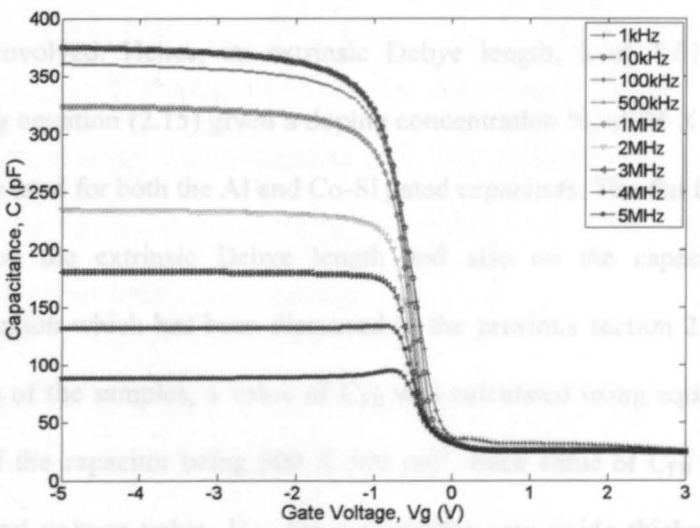

Figure 3-13: Frequency dependent C-V characteristics of Co-Si gated MOS capacitor at a gate oxide thickness of 23 nm.

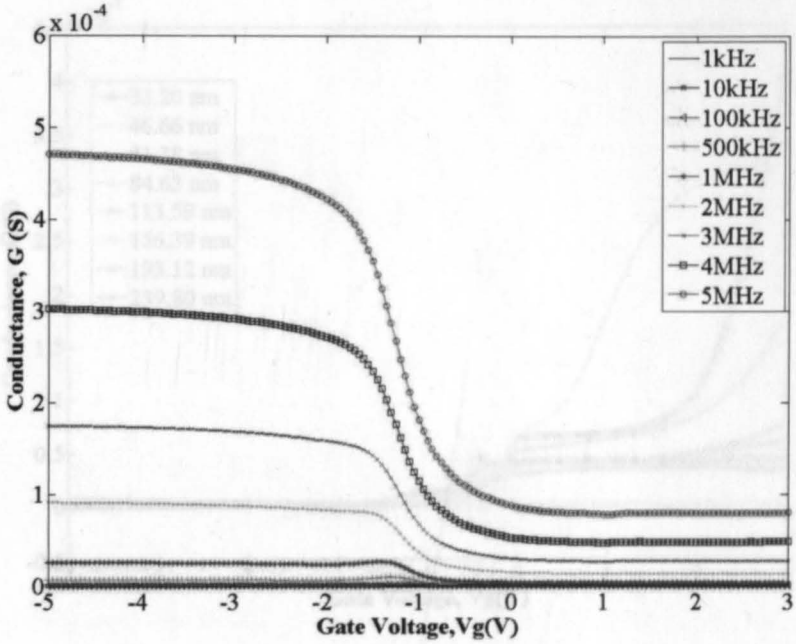

Figure 3-14: Frequency dependent G-V characteristics of Co-Si gated MOS capacitor at a gate oxide thickness of 159 nm.

the materials involved. Hence, an extrinsic Debye length, λ of 8.01 X 10^{-8} m was calculated using equation (2.15) given a doping concentration N_a of 26 X 10^{14} cm^{-3} for the p-type substrate used for both the Al and Co-Si gated capacitors. The flat band capacitance, C_{FB} depends on the extrinsic Debye length and also on the capacitance at strong accumulation region which has been discussed in the previous section 2.6. For each gate oxide thickness of the samples, a value of C_{FB} was calculated using equation (2.16) with the gate area of the capacitor being 500 X 500 μm^2. Each value of C_{FB} corresponds to a specific flat band voltage value, V_{FB} for a particular gate oxide thickness of the MOS capacitor. From the C-V curve for each specific gate oxide thickness, V_{FB} was determined using linear interpolation. From the strong accumulation region, C-V measurement of C_{ox}, effective oxide thickness EOT_{ox} was calculated using equation (2.11).In appendix section,

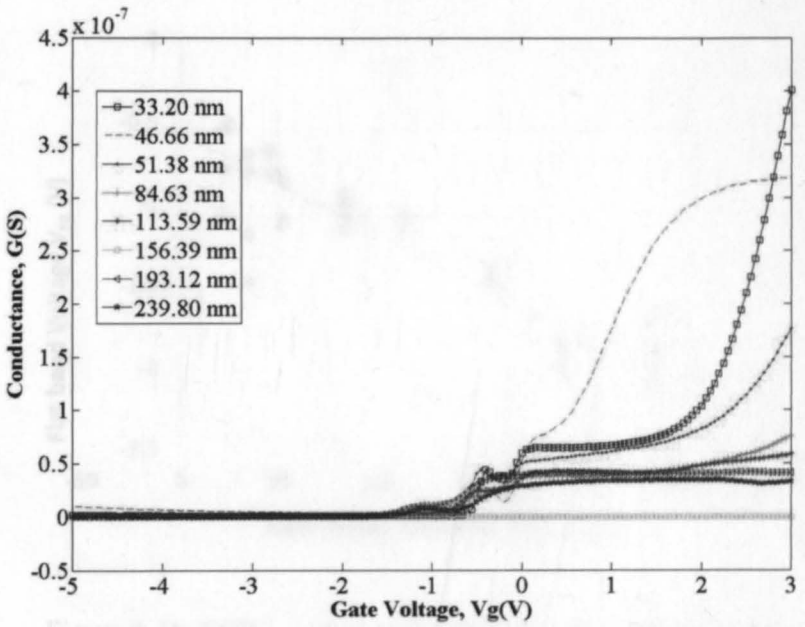

Figure 3-15: Gate oxide thickness dependent G-V characteristics of Co-Si gated MOS capacitor.

Table A1and Table A2 shows the detailed data for Co-Si and Al gated MOS capacitors. The EOT_{ox} values from C-V measurements varied only slightly (i.e., 0 to 12%) from those measured by reflectometry which suggests little inter-diffusion between Co-Si and the SiO_2 under layer which is consistent with previous data for Co films on SiO_2 where CoO decomposes to Co after 700 °C for 30 seconds [90].

The flat band voltages and their corresponding gate oxide thickness were plotted to obtain the EOT_{ox}-V_{FB} curve as shown in Figure 3-16 for Co-Si MOS capacitor and Figure 3-17 for Al MOS capacitor. The metal-to-semiconductor work function difference Φ_{ms} for Cobalt silicide was -0.575 eV as determined from the y-axis intercept of the EOT_{ox}-V_{FB} curve shown in Figure 3-16. The bulk potential Ψ_B for the Si substrate was calculated using equation (2.4) with doping concentration of the Si substrate, Na = 26 X 10^{14} cm^{-3},

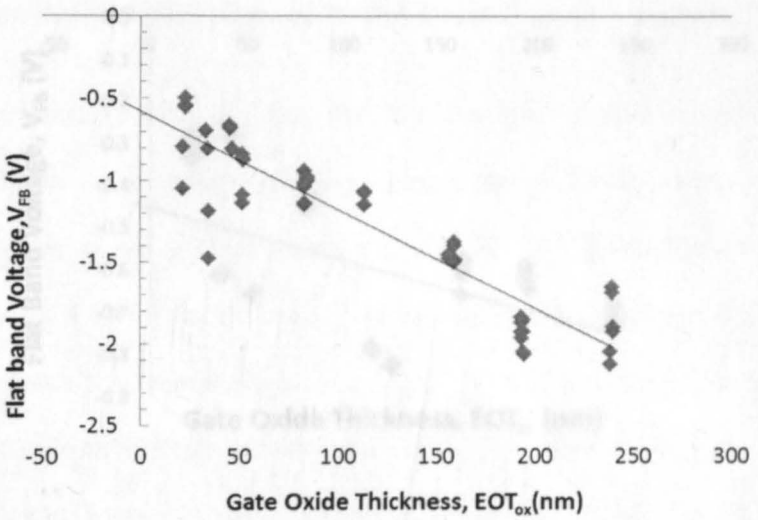

Figure 3-16: $EOT_{ox} - V_{FB}$ curve for Co-Si gated MOS capacitor with gate oxide thickness ranging from 21.58 nm to 239.80 nm.

intrinsic carrier concentration of Si, n_i = 1.02 X 10^{10} cm^{-3} and ambient temperature, T = 300 K and found to be 0.321 eV. By plugging the values of Si electron affinity χ_{Si} = 4.05 eV, Si band gap energy E_g = 1.12 eV and the metal-to-semiconductor work function difference between Co-Si and Si Φ_{ms} = -0.575 eV (as found from Figure 3-16) into equation (2.8), the work function of Co-Si was found to be 4.356 eV.

From Figure 3-17, the metal to semiconductor work function difference, Φ_{ms} between Al and Si was found to be -0.451 eV. Using the same methodology as above, the work function of Al was extracted using equation (2.8) as 4.48 eV.

3.3.3.Work function extraction of Co-Si and Al with ultraviolet photoemission spectroscopy (UPS):

Ultraviolet photoemission spectroscopy (UPS) uses photoionization phenomenon and

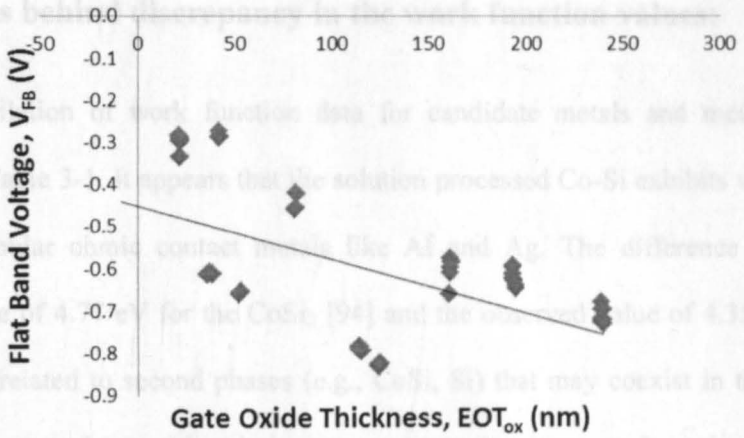

Figure 3-17: EOT_{ox} – V_{FB} curve for Al gated MOS capacitor with gate oxide thickness ranging from 21.69 nm to 239.13 nm.

analysis of the kinetic energy spectra distribution of the emitted photoelectrons by ultraviolet photons to study the composition and electronic state of the surface region of a sample [91],[92]. To verify the work function of the Co-Si ink, a sample of Co-Si film on a 1x1 cm^2 Si wafer substrate (<0.005 Ω.cm) was sent to University of Missouri – Kansas City for extracting the work function through UPS characterization along with an Al sample with similar configuration. Ultraviolet photoelectron spectroscopy (Kratos Axis HS) was used for direct work function measurements using He I (21.1eV) secondary cutoffs respect to clean gold (5.1eV) and silver (4.73eV) with a percentage error of 5%. Calculation of the work function was made at the transition of the low-energy secondary-electron edge to the sharp photoemission onset [93]. UPS analysis of a Co-Si film on a conducting Si wafer gave a Φ_m value of 4.80 eV (shown in Figure 3-18) which is close to UPS data previously reported for a $CoSi_2$ film prepared by heating a Co film on Si (i.e., Φ_m = 4.77 eV) [94]. A work function of 4.40 eV was derived for the Al film.

3.4. Reasons behind discrepancy in the work function values:

A compilation of work function data for candidate metals and metal silicide is presented in Table 3-1. It appears that the solution processed Co-Si exhibits work function similar to popular ohmic contact metals like Al and Ag. The difference between the literature value of 4.77 eV for the $CoSi_2$ [94] and the observed value of 4.356 eV for the Co-Si maybe related to second phases (e.g., CoSi, Si) that may coexist in these films as stoichiometric control over this solution process is in development. It is also possible that Li+ impurities may be present in the Co-Si layer given the method of synthesizing Si_6H_{12} (i.e., residual LiCl from the $LiAlH_4$ reduction) [98]. There also exists a slight discrepancy between the work function of Al measured in this study and literature reports [95].

It is also possible that differences in work function may be related to a parallel shift of the C-V. In such instances, a parallel shift of the C-V curve along the DC applied voltage axis from ideal theoretical curve occurs because of trapped space charges distributed in the oxide layer and this parallel shift is quantified by the following [54]-

$$V_{FB} = \Phi_{ms} - \frac{Q_f + Q_m + Q_{ot}}{C_{ox}} \qquad (3.2)$$

where Q_f is the fixed oxide charge, Q_m is the mobile ionic charge, Q_{ot} is the oxide trapped charges and C_{ox} represents the capacitance at strong accumulation (Figure 3-19).

The interface trap charges, Q_{it} are located at the SiO_2/Si interface and may be a consequence of factors such as lattice mismatch, incomplete bonding or impurity atom absorption at the interface. These charges are the most concerning since distortion of the CV curve along the voltage axis compared with ideal CV curve may occur because of the

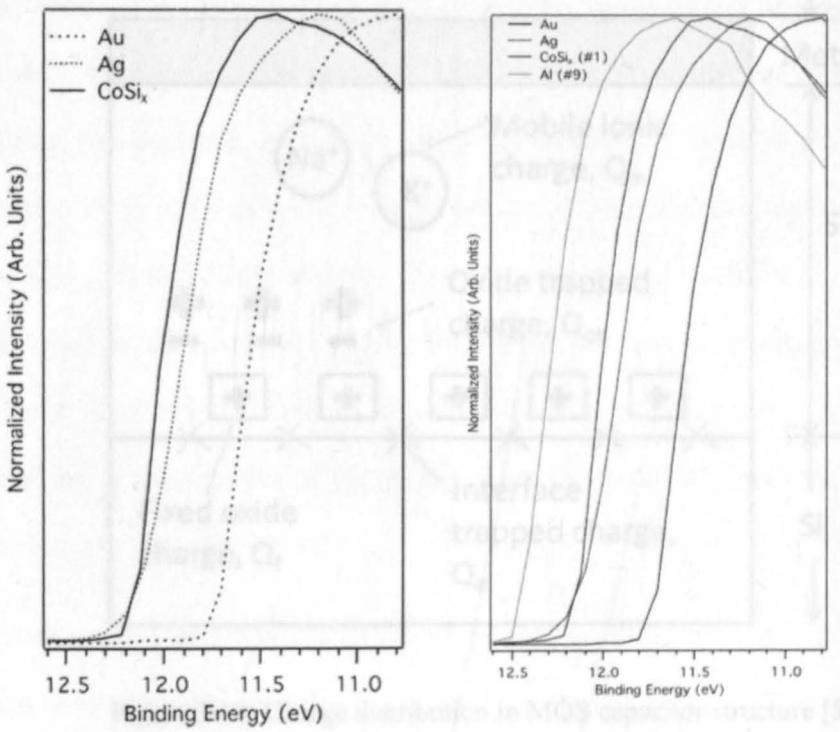

Figure 3-18: UPS data for a solution processed Co-Si film and Al film on a doped Si wafer. Calculated work function for Co-Si is 4.80 eV and for Al is 4.40 eV.

Table 3-1 Metal work function data for candidate materials

Material	Work Function (eV)	Reference
Co-Si	4.356	This Work (C-V data)
Co-Si	4.80	This Work (UPS data from UMKC)
$CoSi_2$	4.77	[30]
Al	4.48	This Work
Al	4.28	[31]

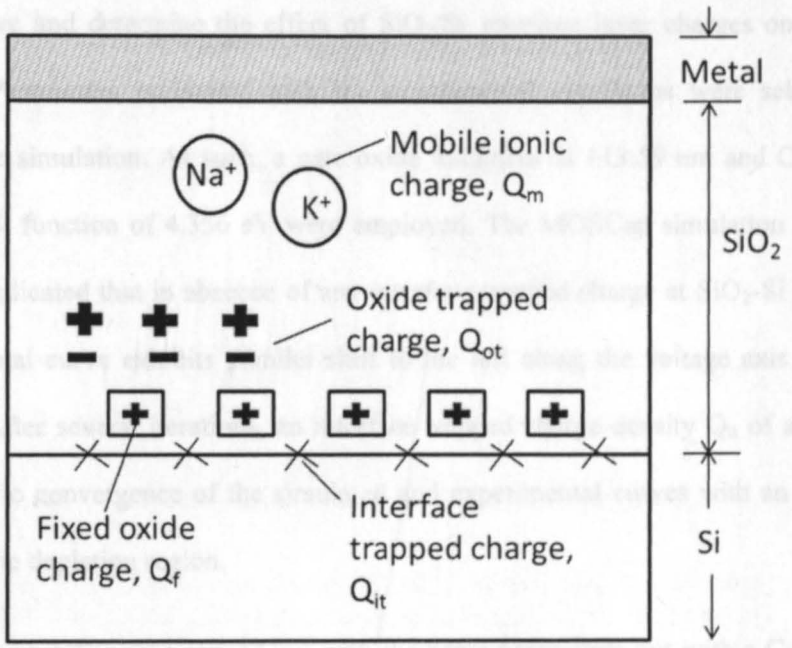

Figure 3-19: Charge distribution in MOS capacitor structure [56].

existence of interface trapped charges at the SiO_2/Si interface or in the Si surface space-charge region. The distortion is caused by the voltage dependence of the density of the trapped interface charge when applied DC voltage is varied resulting in a shift of the work function value [58].

Fixed oxide charge Q_f arise due to structural damage during oxidation or impurity atoms that are located close to the interface state. The oxide trapped charge Q_{ot} are associated with defects in the SiO_2 layer. The mobile ionic charge Q_m are due to sodium (Na^+) or other alkali ions that enter the oxide during cleaning, processing or handling of the MOS device [96]. The charges are time variant and may result electrical instability in Si MOS transistor.

A simulation of the Co-Si MOS capacitor was carried out using MOSCap software

[97] to observe and determine the effect of SiO_2/Si interface layer charges on the C-V curve shift. Parameters consistent with the experimental conditions were selected for initializing the simulation. As such, a gate oxide thickness of 113.59 nm and Co-Si gate electrode work function of 4.356 eV were employed. The MOSCap simulation shown in Figure 3-20 indicated that in absence of any interface trapped charge at SiO_2-Si interface, the experimental curve exhibits parallel shift to the left along the voltage axis from the ideal curve. After several iterations, an interface trapped charge density Q_{it} of about 4 X 10^{10} cm^{-2} led to convergence of the simulated and experimental curves with an excellent match along the depletion region.

Similar simulation was carried out with the same parameters but with a Co-Si work function of 4.8 eV as found by UPS. The simulation result along with experimental data is shown in Figure 3-21. With the higher work function, the C-V curve shifted even more to left in comparison to the curve shown in Figure 3-20. In this instance, an interface charge density Q_{it} of 8.3 X 10^{10} cm^{-2} led to convergence of the simulated with experimental data. Therefore, it is concluded that the discrepancy of work function measured through C-V measurement and UPS is a result of the presence of interface trapped charges in the SiO_2/Si interface.

3.5. Additional parameter extraction:

There have been several reports for modeling MOS capacitors using a combination of basic electrical elements like resistors and capacitors [99-103]. The two element series model is such a model where a the MOS capacitor is represented as a series combination of a capacitor C_{ox} and a resistor R_s (which simulates the impact of series resistance of the sub-

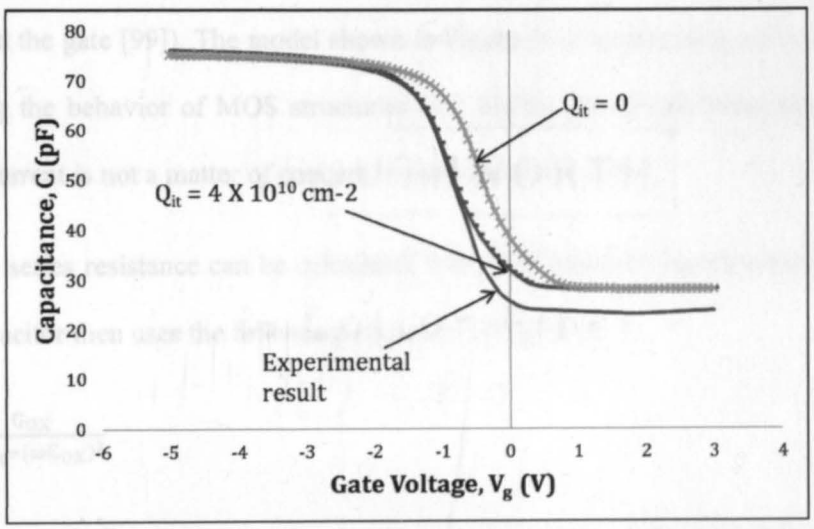

Figure 3-20: Experimental and MOSCap simulated (Q_{it} = 0 and 4 X 10^{10} cm^{-2}) C-V curves with work function of Co-Si Φ_m = 4.356 eV.

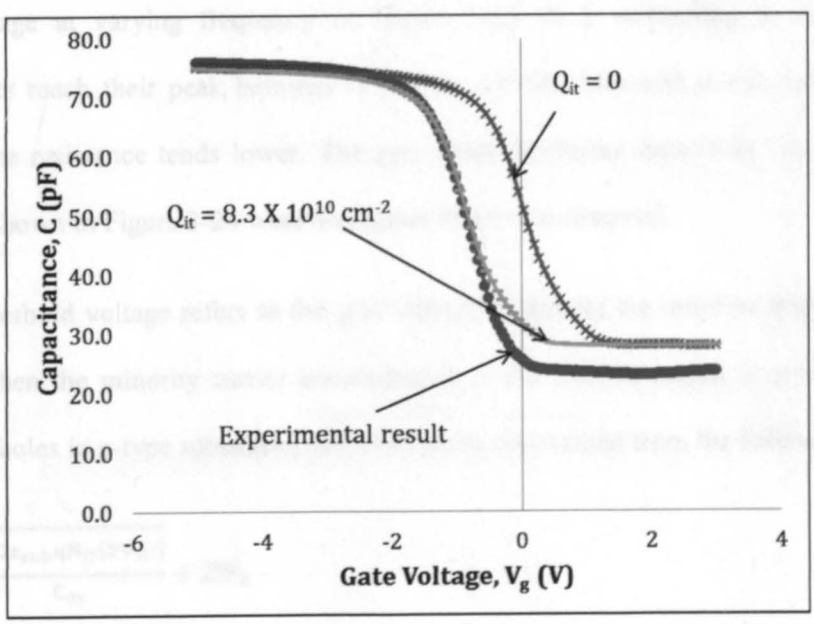

Figure 3-21: Experimental and MOSCap simulated (Q_{it} = 0 and 8.3 X 10^{10} cm^{-2}) C-V curves with work function of Co-Si Φ_m = 4.8 eV.

-strate and the gate [99]). The model shown in Figure 3-22 maintains good accuracy when describing the behavior of MOS structures with higher gate oxide thickness [100] since leakage current is not a matter of concern in such instances [101].

The series resistance can be calculated from C-V and G-V measurement data of the MOS capacitor then uses the following equation [102],[104]-

$$R_S = \frac{G_{OX}}{(G_{OX}^2+(\omega C_{OX})^2} \tag{3.3}$$

where C_{ox} and G_{ox} represent the measured capacitance and conductance in strong accumulation region.

R_s is calculated using equation (3.3) based on the C-V and G-V measurement data of Co-Si capacitors with a gate oxide thickness of 159.86 nm and plotted as a function of gate bias voltage at varying frequency in Figure 3-23. It is interesting to note that the resistances reach their peak between -1.5 V to -1V DC bias and as the frequency goes higher, the resistance tends lower. The gate oxide thickness dependent series resistance curve is shown in Figure 3-24 were no regular trend was observed.

Threshold voltage refers to the gate voltage triggering the onset of strong inversion region when the minority carrier concentration in the SiO_2/Si region is greater than the majority holes in p-type substrate [104] and can be determined from the following [54] –

$$V_{Th} = \frac{\sqrt{(2\varepsilon_{sub}qN_D(2\Psi_B))}}{C_{ox}} + 2\Psi_B \tag{4}$$

where ε_{sub} = permittivity of Si ($11.9 \times 8.854 \times 10^{-14}$ Fcm^{-1}), q = electron charge (1.602×10^{-19} C), N_D = doping concentration of the substrate (26×10^{14} cm^{-3}) and C_{ox} = gate oxide

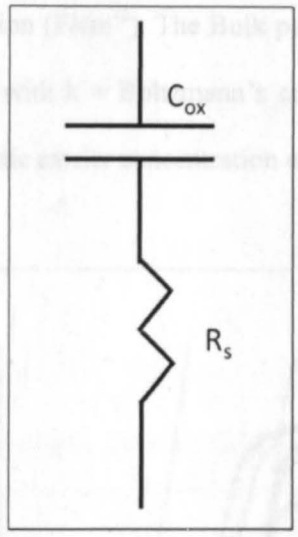

Figure 3-22: 2 element series model for MOS capacitor.

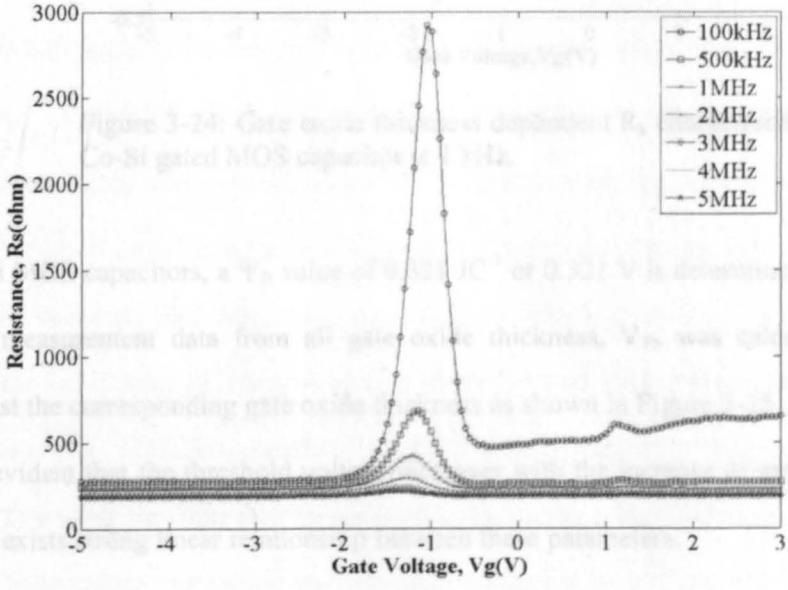

Figure 3-23: Frequency dependent R_s characteristics of Co-Si gated MOS capacitor (EOT_{ox} =159.86 nm).

capacitance at strong accumulation (F/cm^{-2}). The Bulk potential Ψ_B of a MOS structure is calculated using equation (2.4) with k = Boltzmann's constant (1.38 X 10-23 JK^{-1}), T = Temperature (300 K), n_i = intrinsic carrier concentration of Si (1.02 X 10^{10} cm^{-3}). For the

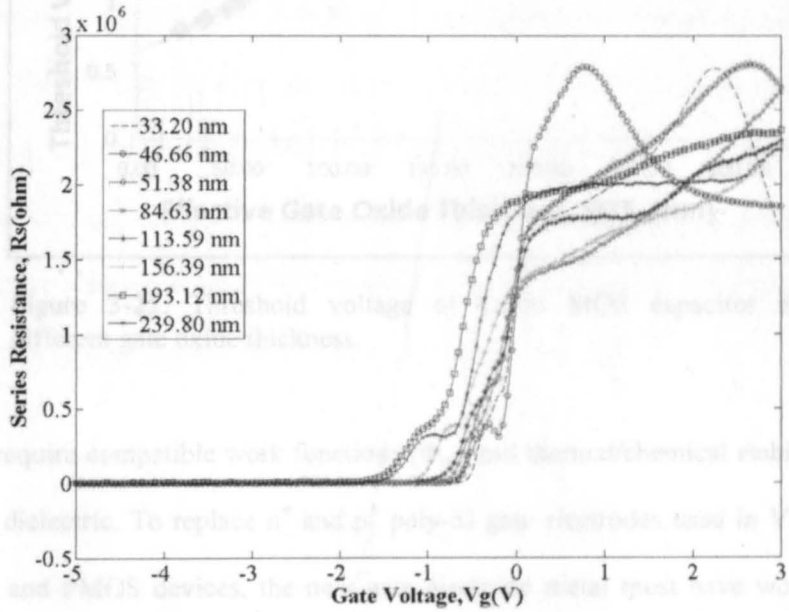

Figure 3-24: Gate oxide thickness dependent R_s characteristics of Co-Si gated MOS capacitor at 1 kHz.

Co-Si MOS capacitors, a Ψ_B value of 0.321 JC^{-1} or 0.321 V is determined. Considering the C-V measurement data from all gate oxide thickness, V_{Th} was calculated and plotted against the corresponding gate oxide thickness as shown in Figure 3-25. From Figure 3-25, it is evident that the threshold voltage increases with the increase of gate oxide thickness, there exists strong linear relationship between these parameters.

3.6. Co-Si as a gate metal candidate:

Candidate gate metals to be used as ohmic contacts in thin film transistors or MOS

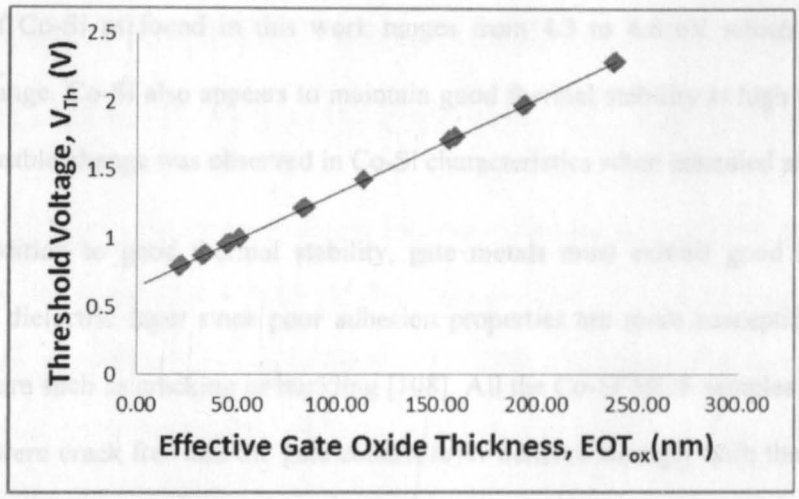

Figure 3-25: Threshold voltage of Co-Si MOS capacitor at different gate oxide thickness.

capacitors require compatible work functions (Φ_m) and thermal/chemical stability with the underlying dielectric. To replace n^+ and p^+ poly-Si gate electrodes used in VLSI systems for NMOS and PMOS devices, the new gate electrode metal must have work functions near 4.1 eV and 5.2 eV, respectively [106]. In addition to the appropriate work function requirements, several material properties such as free energy of oxide formation, oxygen solubility, diffusion barrier properties and film microstructure can be used as indicators of thermal stability [106]. Since electronegativity is generally inversely related to free energy of oxide formation and is proportional to work function, elemental metals with lower work functions (i.e., NMOS-compatible) typically exhibit stability problems. This implies that most low work function NMOS-compatible elemental metals are expected to suffer from high temperature instability and reactions resulting in a degraded interface with the underlying dielectric. For example, metals such as Ta, Ti, Al, Zr, Hf, which have work functions less than 4.3 eV and are considered inadequate for gate application under conventional process flows since they react with the underlying dielectric [107]. The work

function of Co-Si as found in this work ranges from 4.3 to 4.8 eV which is near the specified range. Co-Si also appears to maintain good thermal stability at high temperature as no noticeable change was observed in Co-Si characteristics when annealed at 700 °C.

In addition to good thermal stability, gate metals must exhibit good adhesion to underlying dielectric layer since poor adhesion properties are more susceptible to stress related failure such as cracking or buckling [108]. All the Co-Si MOS samples prepared in this study were crack free and the gate contact layer adhered strongly with the underlying layer. For these reasons, solution processed Co-Si thin films appear to be good low work function candidates for use as ohmic contacts in NMOS devices.

CHAPTER 4. SOLUTION PROCESSED THIN FILM TRANSISTORS FROM CYCLOHEXASILANE INK

In this chapter, the cyclohexasilane ink preparation method and fabrication process for solution processed polycrystalline Si thin film transistors (TFT) is discussed. A detailed performance analysis on the extracted data of the TFT is also presented. In a later section of the chapter, the experimental results are matched with BSIM3 version 3 NFET model and the parameter extraction procedure is detailed.

4.1. Basic TFT working principle:

TFTs are similar to traditional MOSFETs operating in either a linear or a saturation region. A cross-sectional view of the channel region of a poly-Si TFT is shown in Figure 4-1. With the application of drain voltage V_d, a channel region evolves in the active layer between the source and drain with charge density per unit area in the channel depending upon the amount of drain voltage applied [109]. When the applied gate voltage V_g is greater than the threshold voltage V_{Th}, the mobile charge Q_m can be calculated using the following equation [109]-

$$Q_m = C_i(V_g - V_{Th} - V) \tag{4.1}$$

where C_i is the capacitance per unit area of the insulator layer and V is the voltage between the drain and source. The current induced by the charges in the channel can be found by the following equation [110]-

$$I_d = W\mu_{FE}Q_mE_d \tag{4.2}$$

where W = width of the channel, μ_{FE} = field effect mobility and E_d = electric field along the channel.

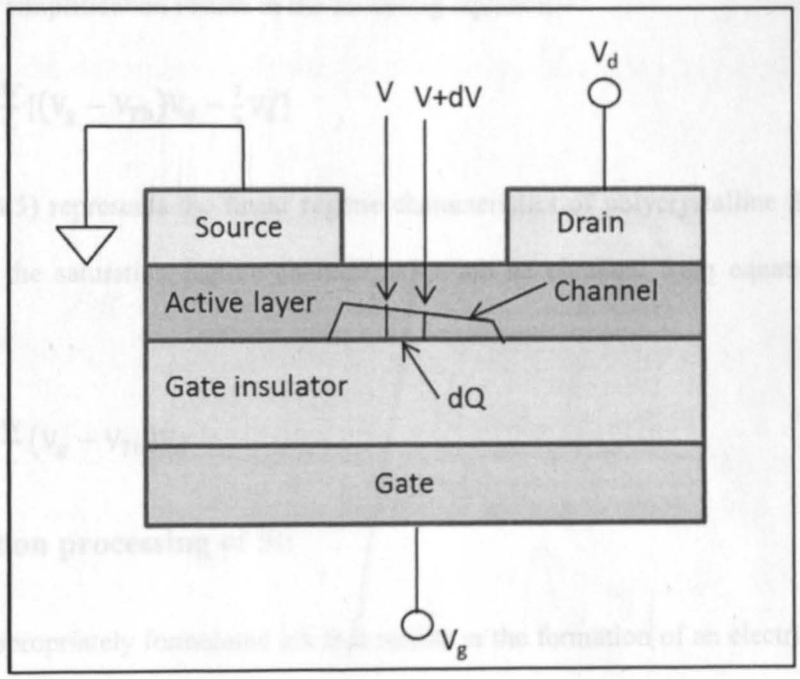

Figure 4-1: Cross-sectional view of the channel region of a TFT.

Assuming the field is uniform along the channel, it can be written as –

$$E_d = -\frac{dV}{dx} \tag{4.3}$$

Combining equation (4.1), (4.2) and (4.3), the relation reduces to –

$$I_d dx = W\mu_{FE}C_i(V_g - V_{Th} - V)dV \tag{4.4}$$

By integrating equation (4.4) with boundary conditions, x = 0 to x = channel length = L and V = 0 to V = drain voltage = V_d, the following expression can be obtained –

$$\int_0^L I_d dx = \int_0^{V_d} \{W\mu_{FE}C_i(V_g - V_{Th} - V)\}dV$$

which after simplification results in the following equation –

$$I_d = \mu_{FE}C_i\frac{W}{L}\left[(V_g - V_{Th})V_d - \frac{1}{2}V_d^2\right] \tag{4.5}$$

Equation (4.5) represents the linear regime characteristics of polycrystalline Si TFT's. If $V_d << V_g$, the saturation regime characteristics can be obtained from equation (4.5) as follows –

$$I_d = \mu_{FE}C_i\frac{W}{L}(V_g - V_{Th})V_d \tag{4.6}$$

4.2. Solution processing of Si:

An appropriately formulated ink that results in the formation of an electrically active Si film is key to solution processing of Si. Given the need for high purity in the device, obvious choices for suitable chemistries include carbon- and oxygen-free compounds. Akin to their carbon-based counterparts, hydrogenated silicon compounds exist in both straight chain (Si_nH_{2n+2}) and cyclic (Si_nH_{2n}) forms. For $n \geq 3$, these compounds are liquid at room temperature and decompose to form a-Si when heated to 300 °C or higher [39]. As the chemistry of the compounds are just Si and H and the H can be removed via thermolysis, hydrogenated silanes are potential candidates in the formation of electronic-grade silicon thin film materials.

Cyclohexasilane (Si_6H_{12}) is a liquid (melting point 18 °C) used by researchers in the formation of silicon thin film materials. Si_6H_{12} is prepared in two steps as shown in Figure 4-2. First, a solution of trichlorosilane ($HSiCl_3$) and pentaethyldiethylenetriamine

(PEDETA) in dichloromethane (CH_2Cl_2) is refluxed at 40-45 °C for 48 hours to give a novel complex $[PEDETA{\cdot}H_2SiCl^+]_2[Si_6Cl_{14}^{2-}]$ as reported in [111]. Secondly, $LiAlH_4$ is used to reduce the $[PEDETA{\cdot}H_2SiCl^+]_2[Si_6Cl_{14}^{2-}]$ salt to give Si_6H_{12}. The crude product is purified via reduced-pressure distillation to give the colorless Si_6H_{12} liquid.

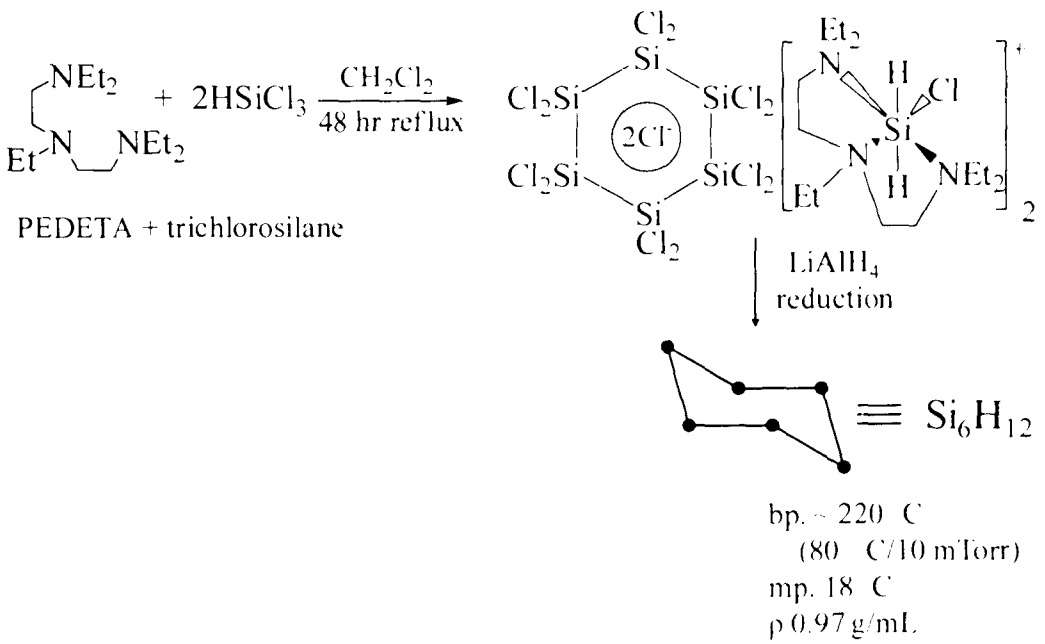

Figure 4-2: Synthetic route to Si_6H_{12}.

Liquid cyclosilanes have been considered as precursors in direct-write fabrication of printed electronics [50]. Si_6H_{12} can be transformed into solid polydihydrosilane $-(SiH_2)_n-$ by thermal treatment or light activation via radical polymerization (Figure 4-3). Additional thermal decomposition causes evolution of H_2 gas giving a-Si:H at a temperature around 350 °C and crystalline silicon at 750 °C [112]. The Si TFTs prepared in this study utilized this approach in the formation of the active semiconductor layer.

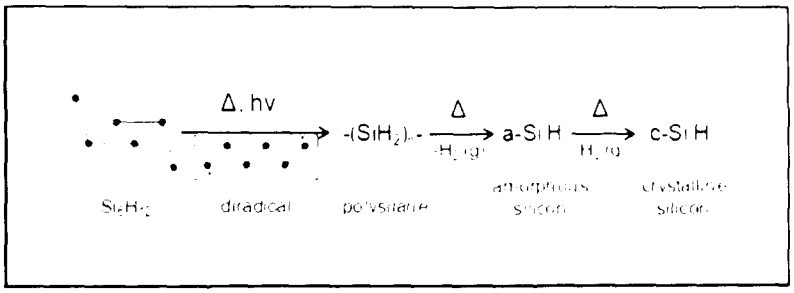

Figure 4-3: Schematic illustrating the transformation of Si_6H_{12} to Si thin film materials.

4.3. TFT structure:

TFTs are typically constructed with either staggered or coplanar orientations. A staggered TFT has the gate and source/drain electrodes on opposite sides of the semiconductor whereas a coplanar structure has the gate and the source/drain contact on the same side of the semiconductor. Staggered structures are formed in two types – normal and inverted-staggered. In the inverted-staggered structure, the gate electrode is fabricated at the bottom which makes the process convenient as subsequent pattering stage are minimized. Figure 4-4 shows both the staggered and inverted staggered TFT structures. Since the inverted-staggered TFT configuration is widely used for LCD displays [113] and is convenient to fabricate, this structure was chosen for the proposed solution processed poly-Si TFT as shown in Figure 4-5.

4.4. Fabrication of Al gated TFT:

4.4.1. Ink preparation:

$[(PEDETA)(H_2SiCl)]_2[Si_6Cl_{14}]]$ of an amount of 40.6 mmol was mixed with 200 mL

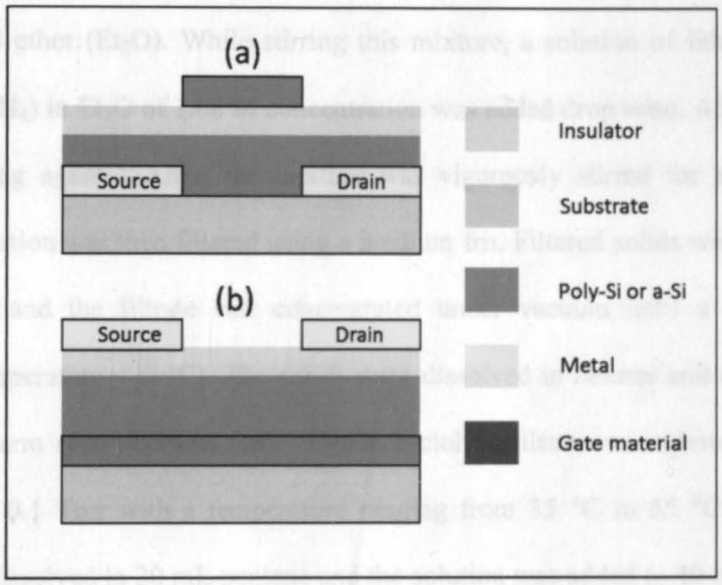

Figure 4-4: Generic TFT structures for (a) staggered and (b) inverted-staggered geometries.

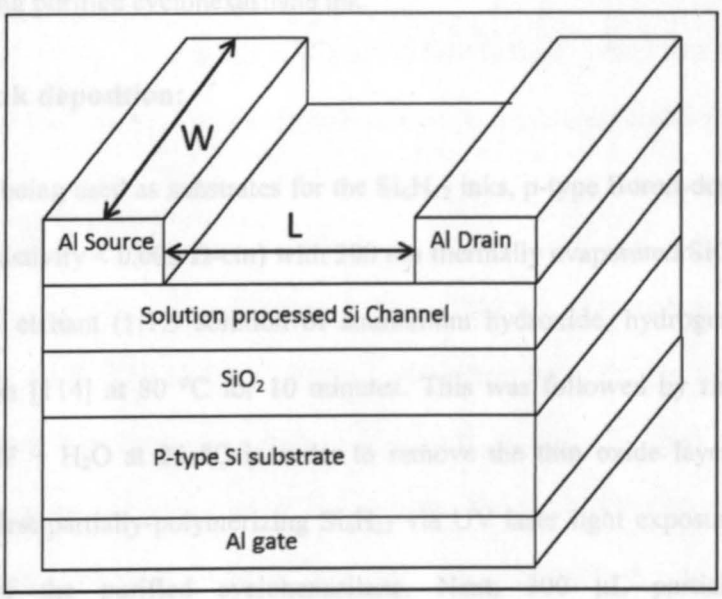

Figure 4-5: Inverted-staggered TFT structure used for solution processing of Si TFTs.

of dry diethyl ether (Et_2O). While stirring this mixture, a solution of lithium aluminum hydride ($LiAlH_4$) in Et_2O of 1.08 M concentration was added drop wise. After the addition of the reducing agent $LiAlH_4$, the mixture was vigorously stirred for an additional 3 hours.The solution was then filtered using a medium frit. Filtered solids were washed with 80 mL Et_2O and the filtrate was concentrated under vacuum until a colorless solid remained (temperature < 0 °C). The solids were dissolved in hexane and decanted into a 100 mL side arm round bottom flask. Crude cyclohexasilane was isolated after vacuum distillation at 0.1 Torr with a temperature ranging from 35 °C to 55 °C. The isolated product was dissolved in 20 mL pentane and the solution was added to 40 mL 6 M H_2SO_4. The immiscible liquids were mixed for 10 min and the organic layer was isolated. After removing volatile pentane under vacuum, the remaining liquid was distilled at 0.1 Torr at 35-45 °C giving purified cyclohexasilane ink.

4.4.2. Ink deposition:

Prior to being used as substrates for the Si_6H_{12} inks, p-type Boron-doped 4" Si wafer substrates (resistivity < 0.005 Ω-cm) with 300 nm thermally evaporated SiO_2 were cleaned with an RCA etchant (1:1:5 solution of ammonium hydroxide, hydrogen peroxide and water) solution [114] at 80 °C for 10 minutes. This was followed by rinsing in a 1:50 solution of HF + H_2O at 25 °C in order to remove the thin oxide layer. The ink was prepared by first partially-polymerizing Si_6H_{12} via UV laser light exposure (355 nm and 300 mW) of the purified cyclohexasilane. Next, 300 µL partially-polymerized cyclohexasilane was mixed with 2.7 mL of cyclooctane (C_8H_{16}) and stirred for 5 minutes. Residuum was removed by a filtration through 1 µm syringe filter to give a colorless solution that was stored in cleaned glass vials. Then the p-type substrate with SiO_2 layer

was loaded to the spin coater and a 2.5 mL of the ink was delivered on top of the wafer using a micropipette. The Si_6H_{12} in C_8H_{16} solution was left for 1 minute while the sample was exposed to UV light from a Hg (Xe) short arc lamp at 220-400 nm wavelength and 100 mW power which led to polymerization of unreacted Si_6H_{12} monomer. The sample was rotated at 1200 rpm for 60 seconds and placed on 100 °C preheated hotplate for 10 minutes. The hotplate was ramped to 400 °C in 15 minutes and held at the temperature for 1 hour and then cooled to room temperature in 10 minutes. This heat treatment to drive out some hydrogen content from the film is regarded as "dehydrogenation" [115] and is necessary to avoid rapid explosive out-diffusion of hydrogen content from the a-Si film.

4.4.3. Post deposition heat treatment:

After the film deposition, the 4" wafer sample was diced into smaller pieces and then annealed at 900 °C for 1 hour inside a N_2-purged tube furnace. This annealing process was done to convert the a-Si film to poly-crystalline form as mentioned earlier (Figure 4-3).

4.4.4. Al gate patterning:

To create source/drain contacts for the TFT, a 250 nm Al layer was deposited using Kurt J. Lesker CMS – 18 sputterer. Process parameters were Ar gas flow of 25 sccm, chamber pressure 5 m Torr, DC power of 650 watts, an AC RF signal of 25 watts RF, ambient temperature and total time of 714 seconds. The sample was rotated at 20 rpm to ensure uniform deposition. After the Al film deposition, a thin layer of hexamethyldisilazane (HMDS) was employed to promote adhesion using a Yield Engineering systems HMDS oven (30 minutes at 138 °C temperature in dry N_2 ambient). Then the wafers were spin-coated with PFI-38A photoresist (PR) using a SUSS RC-8 spin-

coater at 3000 RPM to give a 1.2 μm thick PR layer. The sample was then subjected to a soft bake at 90 °C for 1 minute followed by UV exposure for 13.5 seconds in SUSS MA-8 aligner through 2 X 2 mm^2 shadow masks. In Figure 4-6, an optical photograph of the mask used is shown where (a) depicts the pad size and (b) illustrates the channel length.

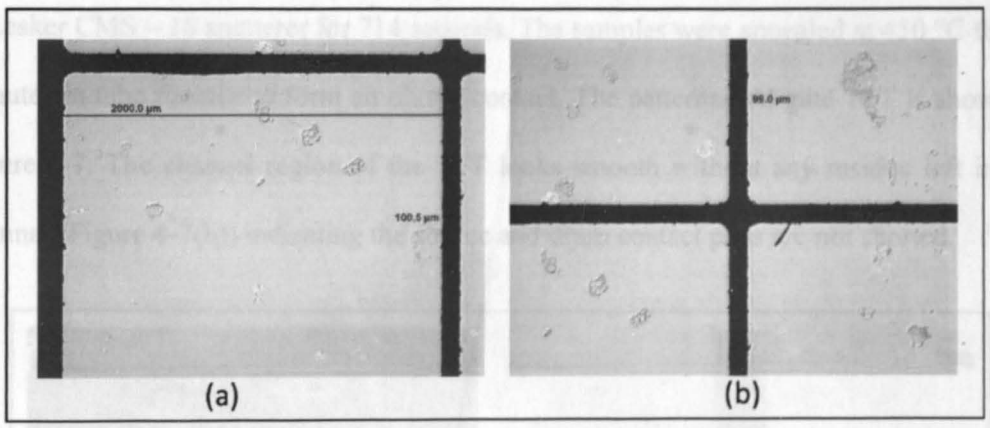

Figure 4-6: Optical microscopy picture of the mask used for TFTs (a) showing pad size and (b) showing channel length.

After another soft bake at 90°C, the photoresist layer was developed using OPD 262 positive photoresist developer (tetramethylammonium hydroxide) for 20 seconds to remove all the exposed PR. Distilled (DI) water rinse then took place followed by N_2 flow to dry the wafers. Following a hard bake at 120°C for 1 minute, the sample was etched with Al Etch II w/SURF solution (phosphoric acid:water:acetic acid = 78:12-16:5-9). Thus, the developed part of the Al layer was removed leaving only the Al gate patterns for the TFT structure. The sample was rinsed with acetone solution followed by isopropanol solution to remove the rest of the PR with a final drying under flowing N_2 gas.

4.4.5. Back contact deposition and heat treatment:

To create a good conductive bottom contact in the bottom gate TFT structure, the back side of the sample first went through an Ar etch with 25 sccm flow of Ar gas, 5-10 mTorr pressure and 100 W RF power. Then 250 nm of Al layer was deposited using Kurt J. Lesker CMS – 18 sputterer for 714 seconds. The samples were annealed at 450 °C for 30 minutes in tube furnace to form an ohmic contact. The patterned Al gate TFT is shown in Figure 4-7. The channel region of the TFT looks smooth without any residue left in the channel (Figure 4-7(b)) indicating the source and drain contact pads are not shorted.

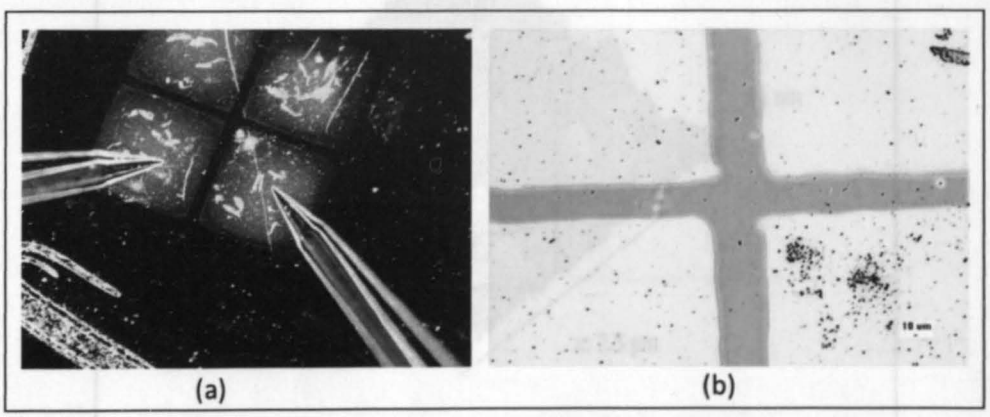

Figure 4-7: Optical microscopy photographs of an Al gated TFT with (a) two probes touching source/drain contacts and (b) the channel region magnified.

4.5. Sample surface quality and channel length measurement:

To evaluate the sample in terms of surface roughness, an atomic force microscopy (AFM) scan was collected using an Agilent Technologies 5500 AFM over different parts of the sample. Figure 4-8 shows an AFM image of the Al gate electrode where the average surface roughness was found to be around 3.52 nm indicating a smooth Al source/drain

contact. Similar AFM data were collected for the solution processed Si thin film with Figure 4-9 showing the Si_6H_{12}-derived polycrystalline Si thin film have an average roughness of 0.59 nm.

The channel length of the TFT was measured using a KLA-Tencor P-15 Longscan contact stylus profiler. The channel length, L between the Al source/drain contact was measured to be 144.8 μm as shown in Figure 4-10.

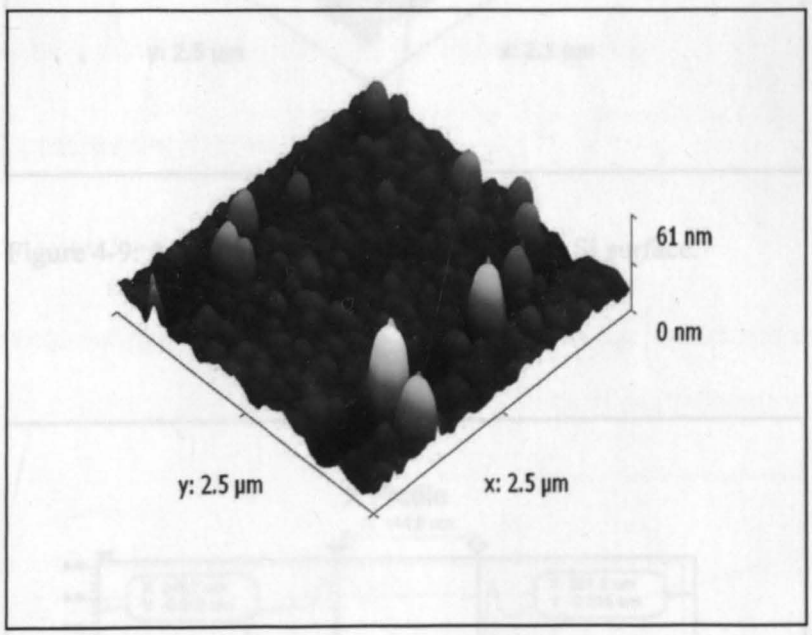

Figure 4-8: AFM profile for Al source/drain contacts.

4.6. Testing and results:

The samples were tested with an Agilent B1500 A semiconductor tester using the stored programs entitled "TFT I_d-V_g" and "TFT I_d-V_d". To obtain the output characteristics (I_d-V_d curve) of the TFT samples, a DC sweep was applied at the drain from 0 to 100 V while the gate voltage, V_g was increased from 60 to 100 V with a 20 V step and correspon-

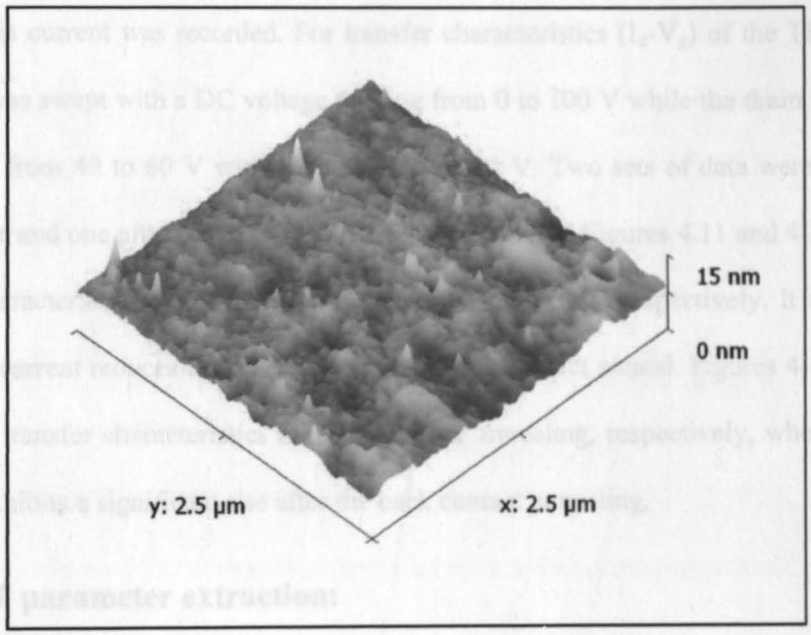

Figure 4-9: AFM profile for the polycrystalline Si surface.

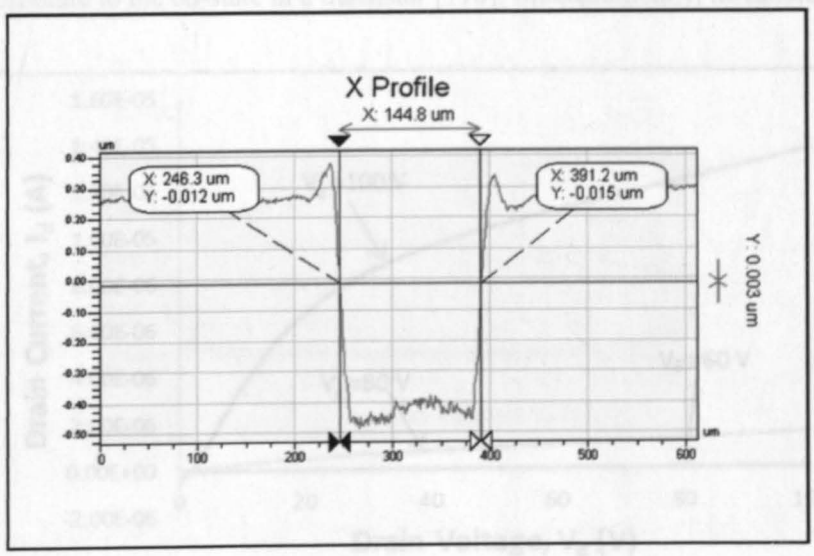

Figure 4-10: Stylus profile of the polycrystalline TFT channel.

-ding drain current was recorded. For transfer characteristics (I_d-V_g) of the TFT samples, the gate was swept with a DC voltage ranging from 0 to 100 V while the drain voltage was increased from 40 to 60 V with an increment of 20 V. Two sets of data were recorded – one before and one after the 450 °C tube furnace anneal. In Figures 4.11 and 4-12 show the output characteristics of the TFT before and after annealing, respectively. It appears that the drain current reduces threefold after the Al back contact anneal. Figures 4-13 and 4-14 show the transfer characteristics before and after annealing, respectively, where the drain current exhibits a significant rise after the back contact annealing.

4.7. TFT parameter extraction:

4.7.1. Threshold voltage extraction:

Threshold voltage V_{Th} can be defined as the gate voltage that causes the transition from the off-state to the on-state in a transistor [116]. Mathematically, threshold voltage is

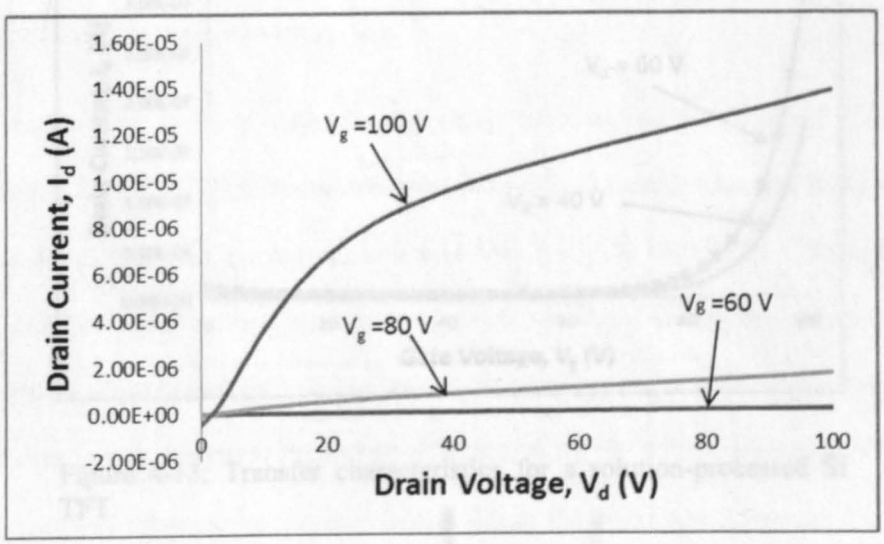

Figure 4-11: Output characteristics for a solution-processed Si TFT.

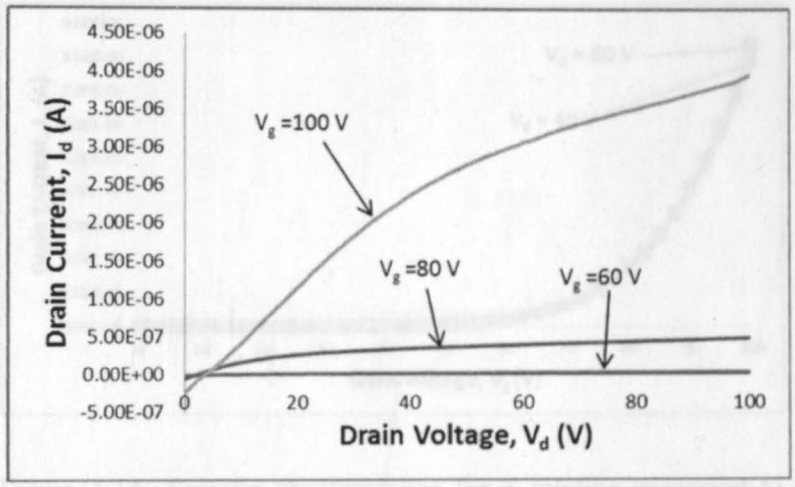

Figure 4-12: Output characteristics for a solution-processed Si TFT after treatment at 450 °C.

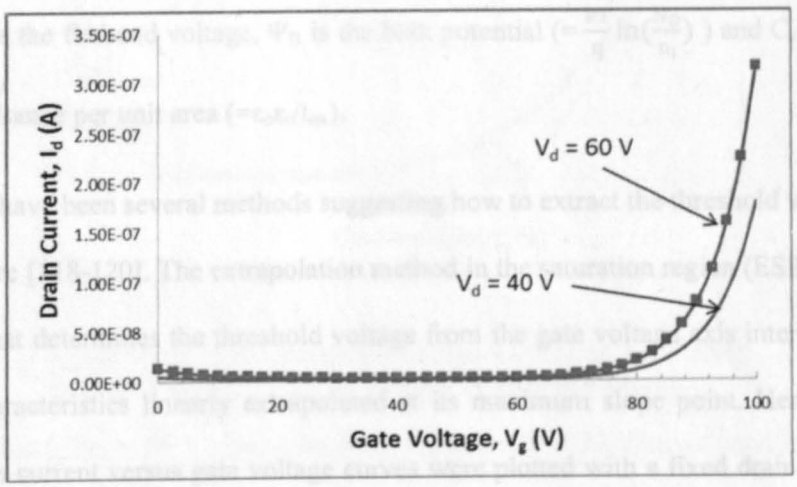

Figure 4-13: Transfer characteristics for a solution-processed Si TFT.

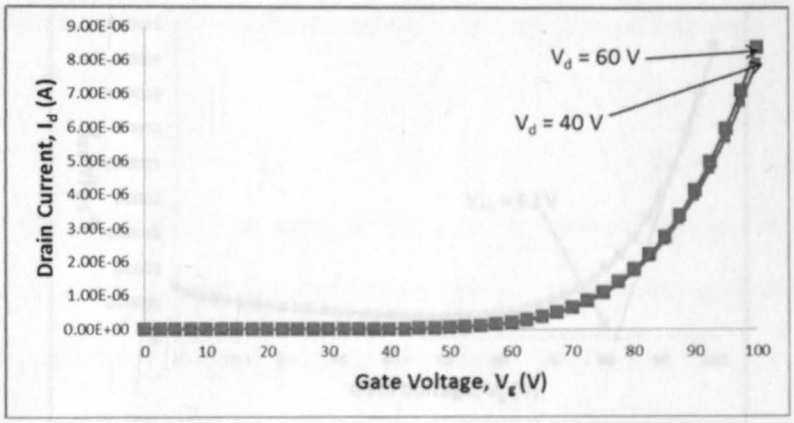

Figure 4-14: Transfer characteristics for a solution-processed Si TFT after treatment at 450 °C.

defined as [117]-

$$V_{Th} = V_{FB} + 2\Psi_B + \frac{\sqrt{(\varepsilon_{sub} q N_D \Psi_B)}}{C_i} \tag{4.7}$$

where V_{FB} is the flatband voltage, Ψ_B is the bulk potential ($=\frac{kT}{q}\ln(\frac{N_D}{n_i})$) and C_i is the gate oxide capacitance per unit area ($=\varepsilon_o\varepsilon_s/t_{ox}$).

There have been several methods suggesting how to extract the threshold voltage of a TFT structure [118-120]. The extrapolation method in the saturation region (ESR) is such a technique that determines the threshold voltage from the gate voltage axis intercept of the $I_D^{0.5}$–V_g characteristics linearly extrapolated at its maximum slope point. Hence, square root of drain current versus gate voltage curves were plotted with a fixed drain voltage of 40 V for data before (Figure 4-15) and after (Figure 4-16) the 450 °C treatment. Threshold voltage, V_{Th} was obtained by linearly extrapolating the maximum slope of the $I_d^{0.5}$–V_g curve to the voltage axis intercept which gives V_{Th} = 82 V before the 450°C Al back conta-

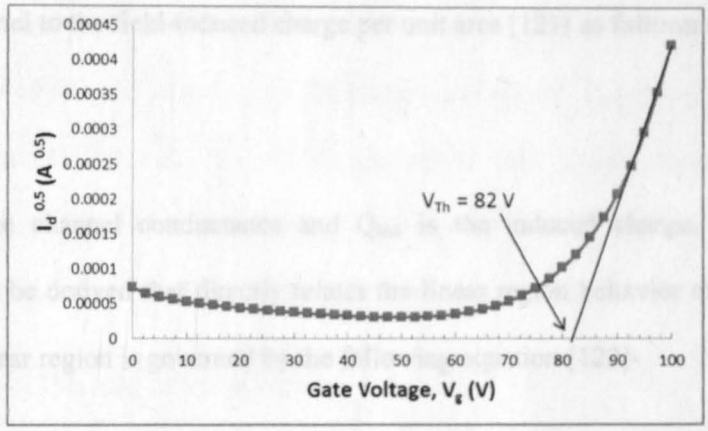

Figure 4-15: TFT threshold voltage extraction with ESR method at V_d = 40 V (before Al back contact annealing).

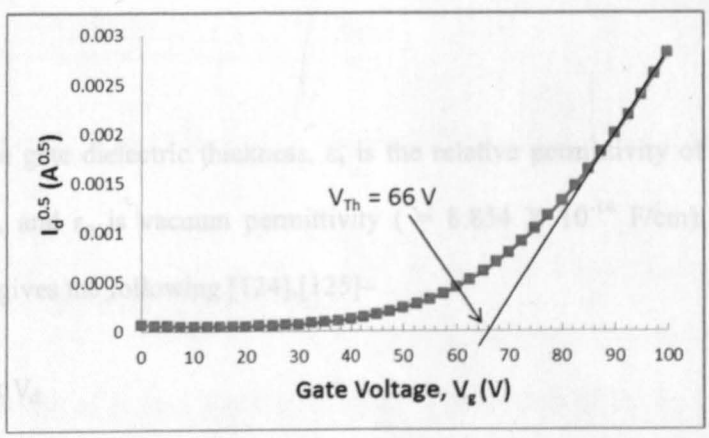

Figure 4-16: TFT threshold voltage extraction with ESR method at V_d = 40 V (after Al back contact annealing).

-ct treatment and V_{Th} = 66 V after annealing. V_{Th} drop after the thermal treatment appears related to the formation of a good ohmic contact.

4.7.2. Field effect mobility (μ_{FE}) calculation:

Field effect mobility can be defined as the term relating the thin film conductance

along the channel to the field-induced charge per unit area [121] as follows –

$$\mu_{FE} = \frac{g}{Q_{ind}} \tag{4.8}$$

where g is the channel conductance and Q_{ind} is the induced charge. An alternative expression can be derived that directly relates the linear region behavior of the TFT. TFT behavior in linear region is governed by the following equation [122]-

$$I_d = \frac{\mu_{FE} W C_i}{L}\left[(V_g - V_{Th})V_d - \frac{V_d^2}{2}\right] \tag{4.9}$$

where, I_d = drain current, W = width of the channel, C_i = capacitance per unit area and L = length of the channel. C_i can be determined using the following equation [123] -

$$C_i = \frac{\varepsilon_s \varepsilon_o}{t_{ox}} \tag{4.10}$$

where t_{ox} is the gate dielectric thickness, ε_s is the relative permittivity of dielectric layer (3.9 for SiO_2), and ε_o is vacuum permittivity (= 8.854 X 10^{-14} F/cm). Differentiating equation (4.9) gives the following [124],[125]–

$$\frac{dI_d}{dV_g} = \frac{\mu_{FE} W C_i}{L} \times V_d \tag{4.11}$$

From equation (4.11), the field effect mobility can be readily obtained as follows -

$$\mu_{FE} = \frac{\frac{dI_d}{dV_g} \times L}{W C_i \times V_d} \tag{4.12}$$

The value of C_i can be obtained using equation (4.10) with a SiO_2 thickness of 300 nm and was found to be 1.15102 X 10^{-8} F cm. $\frac{dI_d}{dV_g}$ represents the slope of the I_d-V_g curve. From Figure 4.13 and Figure 4.14, the slopes of the I_d-V_g curves were obtained as 1.3 X

10^{-8} A/V and 4.24 X 10^{-7} A/V respectively for V_d = 40 V. The TFT sample specifications gave L = 0.01448 cm and W = 0.2 cm. By plugging all these values into equation (4.12), μ_{FE} was obtained as 2.044 X 10^{-3} $cm^2/V.s$ (before Al back contact annealing) and 0.06 $cm^2/V.s$ (after Al back contact annealing). It appears the Al back contact annealing increases the field effect mobility significantly in these solution processed Si TFTs.

4.7.3. On/Off ratio calculation:

One measurement of the TFT performance is the ratio between the highest ON current measured (I_{don}) and the minimum leakage current measured when the TFT is OFF (I_{doff})[125]. Analytically,

$$\text{On/Off ratio} = \frac{\text{Maximum value of drain current, } I_{don}}{\text{Minimum value of drain current, } I_{doff}} \tag{4.13}$$

From Figure 4.13 and Figure 4.14, the On/Off ratio was found to be 23 and 1631, respectively.

4.8. Review on the extracted results:

A compilation of several reports for solution processed TFTs along with pertinent electrical characteristics are given in Table 4-1. Thing to notice is that the threshold voltage of the TFT sample is higher and the mobility and on/off ratio is lower in comparison to some of the literature reports mentioned in Table 4-1.

When considering equation (4.7), it can be said that threshold voltage depends strongly on the device geometry and physical properties like gate oxide thickness and doping concentration of the channel. By reducing the gate oxide thickness, the per unit area

Table 4-1 Electrical data for solution-processed thin film transistors

Active Semiconductor	W/L	V_{th} (V)	Mobility ($cm^2V^{-1}s^{-1}$)	On/Off ratio	Ref.
Cadmium selenide	293μm/8μm	6.7	1	$3.1X10^4$	[47]
$SnS_{2-x}Se_x$	250μm/14μm	40 - 45	0.32	$8X10^4$	[48]
$(C_6H_5C_2H_4NH_3)_2SnI_4$	1000μm/28μm	-30	0.55	$\sim 10^4$	[126]
Zinc-tin-oxide	1000μm/150μm	6.89	0.86	$\sim 10^6$	[44]
Indium-tin-oxide	60μm/5μm	2.5	0.2	10^7	[29]
Si	60μm/5μm	5	74 -108	10^7	[50]
Zinc oxide	60μm/5μm	-	0.018	1.6	[42]
Zinc oxide	60μm/5μm	18	1 - 2	$\sim 10^4$	[43]
Indium-tin-oxide	60μm/5μm	0	0.012	300	[46]
Si	2000μm/145 μm	66	0.06	1631	This work

gate oxide capacitance can be increased which in turn can reduce the threshold voltage significantly. The use of a thinner or higher dielectric constant gate insulator (relative to the 300 nm SiO_2 layer used in this work) is expected to enable significant reduction of the device operating voltage [127]. Also it has been reported that the mobilities of devices with smaller W/L ratio are considerably higher since it reduces the impact of stray current losses outside the channel [127]. Therefore, a W/L of at least 10 it is recommended to minimize the effects of such currents. The metal gate work function plays a significant role in directing the threshold voltage value [128],[129] where the desirable range of threshold voltage has been described as 4.4-5.1 eV. The thickness of the active layer of the TFT impacts the threshold voltage and mobility at the same time [130] with decreasing

thickness reducing the threshold voltage and increasing mobility. Referring to equation (4.12), it appears that the field effect mobility depends on the device geometry strongly where the channel width/length ratio plays a critical role along with gate oxide thickness toward increased mobilities. It has been reported [131] that the type of dielectric (i.e., PECVD or thermal evaporation) can also affect the field effect mobility with thermal oxide anticipated to give better performance. The larger TFT specifications in this work (i.e., gate oxide thickness of 300 nm, channel length of 144.8 μm and an Al gate with work function in the range of 4.18 eV) afford an increase in the threshold voltage level which also contributes to lower mobilities and on/off ratios. This can be easily verified in Table 4-1 where other reports utilized smaller device geometry parameters. Scaling down the device geometry of the solution processed Si TFTs (i.e., smaller W/L ratio, thinner gate oxide) is expected to improve device performance.

4.9. Curve fitting of TFT experimental result with BSIM 3 version 3:

Most circuit simulation tools maintain their own sets of models for MOSFET, BJT and other device structures. However, in most cases the models are not open-source and hence do not allow any sort of alteration except for some physical attributes (i.e., channel length and width). Additionally, each simulation technology (i.e., IBM, Intel) has some specific design rules and the graphical user interface (GUI) of the tools do not permit modification of the physical parameters beyond a defined range. The solution processed Si thin film electronics appear to have different characteristics than standard VLSI technology and there are only limited models in the public domain that mimic the experimentally observed characteristics directly [132]. There are some specialized commercial software like TFT 2D/3D and UTMOST III from SILVACO [133] as well as Virtuoso UltraSim

from Cadence [134] that are capable of extracting model parameters based on experimental results. Such tools allow the user to simulate with a modified model. One challenge of the present work was finding existing simulation platforms that could be modified within the parameters offered with an educational license. Hence, for simulation purpose, an open source model for TFT was necessary that could be tweaked to match experimental transfer characteristics of the solution processed TFT and enable circuit simulation facility to predict behavior in a combinational arrangement.

BSIM3v3 is the latest physics-based, open source, deep-submicron MOSFET model for digital and analog circuit designs from the University of California at Berkeley [135]. About 30 different fitting parameters can easily be modified with many more left untouched for fitting of data [132]. By optimizing these parameters, it is possible to attain the electrical characteristics of solution processed electronics as is described below.

There exist two main optimization strategies – a) global optimization and b) local optimization. Global optimization focuses on finding a set of model parameters which will best fit the available experimental (measured) data. This methodology gives the minimum average error between measured and simulated (calculated) data points, but also treats the parameter as a "fitting" parameter. Physical parameters extracted in such a manner might yield values that are not consistent with their physical intent [135].

For extracting parameters two major strategies are typically employed – a) the single device extraction strategy and b) group device extraction strategy.

In the single device extraction strategy, experimental data from a single device is used to extract a complete set of model parameters. This strategy fits one device very well

but may not fit similar devices with different geometries. Furthermore, single device extraction strategy cannot guarantee that the extracted parameters are physically relevant although the transfer characteristics can be identically fitted for a certain bias condition as mentioned in [135].

For convenience, global optimization of BSIM3 version 3.3 NFET model file was used with single device extraction strategy in Cadence Spectre simulation platform with an educational license. A schematic with the circuit arrangement used in the simulation is shown in Figure 4-17.

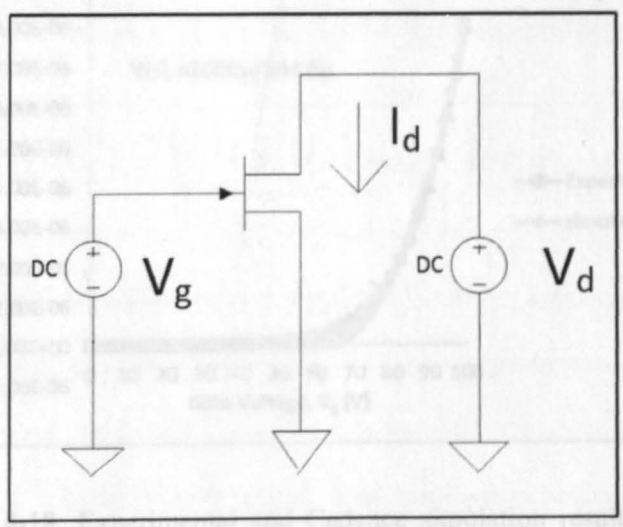

Figure 4-17: Circuit used for parameter extraction.

A constant drain voltage, V_d = 40 V was applied while the gate voltage, V_g was swept from 0 to 100 V to mimic the experimental condition described in earlier part of the chapter. In the netlist file for the simulation, the nfet model was replaced with BSIM3 version 3.3 NMOS model and simulation was run from command prompt window instead of using the GUI. The physical parameters for the model were set exactly like the

experimental configuration with W = 2000 μm, L=144.8 μm, t_{ox} = 300 nm. From several iterations of manually changing different model parameters, it followed that the "vth0" (threshold voltage @ V_{bs} = 0 for large L) parameter plays the pivotal role in fixing threshold voltage value whereas changing "wint" (width offset fitting parameter from I-V without bias) affects the shape of the drain current. Primarily set at 0, an increase in "wint" value resulted in a decrease in drain current and vice versa. Finally, with "vth0" set to 60, "lint" (length offset fitting parameter) set to 9.36 X 10^{-8} and "wint" set to 996.5 X 10^{-6}, both the experimental and simulated curves overlapped as shown in Figure 4-18.

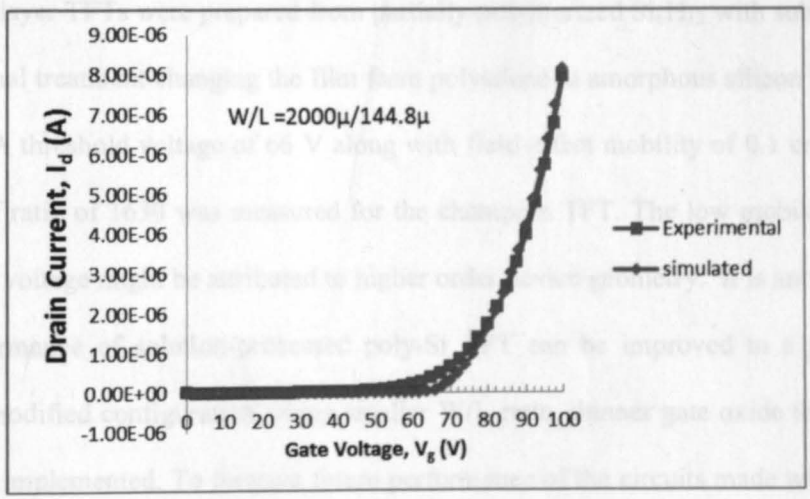

Figure 4-18: Experimental and Cadence simulation result of the transfer characteristics of the TFT.

Since the modified BSIM model is capable of replicating the electrical transfer characteristics of the TFT under a specified bias condition, it can be expected that this model may be utilized to simulate circuits made from solution processed TFT and be able to predict critical circuit performance and efficiency. The modified netlist is attached in the appendix section.

CHAPTER 5. CONCLUSION

This thesis presents a solution route to MOS capacitors and TFTs using inks that utilize Si_6H_{12} as a key reagent. Solution processed Co-Si films were characterized through C-V measurement and a work function of 4.356 eV was derived for Co-Si whereas the UPS-derived work function was found to be 4.8 eV. Since both the values fall in the range of acceptable work function requirement for gate electrode material, Co-Si can be a potential candidate as a low resistance contact material for TFTs. Solution processed poly-Si active layer TFTs were prepared from partially-polymerized Si_6H_{12} with subsequent UV and thermal treatment changing the film from polysilane to amorphous silicon followed by poly-Si. A threshold voltage of 66 V along with field effect mobility of 0.1 $cm^2V^{-1}s^{-1}$ and an off/off ratio of 1630 was measured for the champion TFT. The low mobility and high threshold voltage might be attributed to higher order device geometry. It is anticipated that the performance of solution-processed poly-Si TFT can be improved to a great extent through modified configuration where smaller W/L ratio, thinner gate oxide thickness etc. would be implemented. To forecast future performance of the circuits made with the poly-Si TFT, BSIM 3 version NFET model was matched with experimental transfer characteristics of the TFT through global parametric extraction procedure. The modified model can assist to simulate circuits designed with solution processed poly-Si TFTs with potential applications including displays, wallpaper computers, RFID, e-paper, photovoltaic and health monitoring devices.

The next logical step in the progression of this research would be the fabrication of an all solution-processed mesoscale TFT where Si_6H_{12}-based inks would be used in the

formation of Co-Si gates, sources and drains as well as the poly-Si channel material. While the present study showed that Co-Si possesses good interface stability with both SiO_2 and Si, additional processing parameters will become apparent when all of the contacts as well as the active layer are produced from solution. It has also been reported that Si_6H_{12} can be used in the growth of SiO_x dielectrics [136]. Thus, Si_6H_{12} has the potential of serving as the basis for all components of a solution processed TFT – semiconductor, metal and dielectric. Such inks could be enabling in the roll-to-roll manufacture of flexible electronics if the costs of associated with producing and processing Si_6H_{12} become favorable.

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APPENDIX

Table A1 Cobalt silicide metal-oxide-semiconductor capacitor data

Sample No	Effective gate oxide thickness, EOT_{ox} (nm)	Flat band capacitance, C_{FB} (pF)	Flat band voltage, V_{FB} (V)
1	21.6	178.6	-0.797
2	21.7	178.2	-1.054
3	22.7	174.5	-0.54
4	22.7	174.5	-0.551
5	23.1	173.3	-0.496
6	33.2	144.0	-0.697
7	33.2	144.0	-0.697
8	34.7	140.6	-1.48
9	34.0	142.1	-0.81
10	34.5	140.9	-1.19
11	45.0	120.4	-0.665
12	45.2	120.0	-0.68
13	46.7	117.6	-0.807
14	46.7	117.6	-0.807
15	45.4	119.6	-0.678
16	51.7	110.1	-1.14
17	51.7	110.1	-0.844
18	52.0	109.6	-0.875
19	51.4	110.5	-0.863

Table A1 (Continued)

Sample No	Effective gate oxide thickness, EOT_{ox} (nm)	Flat band capacitance, C_{FB} (pF)	Flat band voltage, V_{FB} (V)
20	51.4	110.5	-1.09
21	83.0	78.7	-0.946
22	83.0	78.7	-0.941
23	84.6	77.5	-1.01
24	84.6	77.5	-1
25	83.0	78.7	-1.04
26	83.0	78.7	-1.02
27	83.0	78.7	-1.15
28	83.0	78.7	-1.14
29	84.6	77.5	-0.987
30	84.6	77.5	-0.979
31	113.6	61.5	-1.07
32	113.6	61.5	-1.15
33	113.6	61.5	-1.08
34	113.7	61.5	-1.15
35	159.6	46.3	-1.5
36	159.6	46.3	-1.38
37	159.9	46.3	-1.49
38	159.9	46.3	-1.49
39	156.4	47.1	-1.48

Table A1 (Continued)

Sample No	Effective gate oxide thickness, EOT_{ox} (nm)	Flat band capacitance, C_{FB} (pF)	Flat band voltage, V_{FB} (V)
40	156.4	47.1	-1.46
41	159.6	46.3	-1.4
42	159.6	46.3	-1.5
43	193.1	39.3	-1.93
44	193.1	39.3	-1.843
45	194.0	39.1	-1.93
46	194.0	39.1	-1.86
47	194.4	39.0	-2.07
48	194.0	39.1	-2.05
49	193.1	39.3	-1.97
50	193.1	39.3	-1.93
51	193.1	39.3	-1.876
52	193.1	39.3	-1.843
53	238.5	32.5	-2.05
54	238.5	32.5	-2.13
55	239.8	32.4	-1.9
56	239.8	32.4	-1.93
57	239.1	32.5	-1.66
58	239.1	32.5	-1.69

Table A2 Aluminum metal-oxide-semiconductor capacitor data

Sample No	Effective gate oxide thickness, EOT_{ox} (nm)	Flat band capacitance, C_{FB} (pF)	Flat band voltage, V_{FB} (V)
1	21.69	178.2	-0.3
2	21.69	178.2	-0.3
3	21.8	177.8	-0.3
4	21.8	177.8	-0.3
5	22.66	174.7	-0.3
6	21.58	178.6	-0.3
7	21.85	177.6	-0.3
8	36.89	135.7	-0.613
9	38.54	132.2	-0.614
10	36.89	135.7	-0.61
11	36.89	135.7	-0.613
12	36.12	137.3	-0.614
13	42.32	125.0	-0.29
14	42.11	125.4	-0.288
15	42.11	125.4	-0.274
16	42.11	125.4	-0.288
17	52.96	108.3	-0.656
18	52	109.6	-0.663
19	52.96	108.3	-0.656
20	52.96	108.3	-0.656

Table A2 (Continued)

Sample No	Effective gate oxide thickness, EOT_{ox} (nm)	Flat band capacitance, C_{FB} (pF)	Flat band voltage, V_{FB} (V)
21	53.29	108.3	-0.655
22	113.89	61.4	-0.787
23	115.26	60.8	-0.797
24	114.34	61.2	-0.787
25	114.19	61.3	-0.794
26	81.44	79.8	-0.42
27	80.68	80.4	-0.461
28	81.44	79.8	-0.456
29	82.22	79.2	-0.424
30	81.44	79.8	-0.422
31	124.03	57.3	-0.826
32	123.68	57.4	-0.832
33	125.47	56.7	-0.825
34	124.39	57.1	-0.833
35	124.21	57.2	-0.827
36	160.76	46.0	-0.577
37	160.46	46.1	-0.662
38	161.66	45.8	-0.587
39	160.76	46.0	-0.613
40	192.69	39.3	-0.6

Table A2 (Continued)

Sample No	Effective gate oxide thickness, EOT_{ox} (nm)	Flat band capacitance, C_{FB} (pF)	Flat band voltage, V_{FB} (V)
41	194.43	39.0	-0.65
42	192.69	39.3	-0.624
43	193.56	39.2	-0.632
44	239.13	32.5	-0.683
45	239.13	32.5	-0.728
46	36.89	135.7	-0.612
47	38.54	132.2	-0.612
48	36.89	135.7	-0.609
49	36.89	135.7	-0.613
50	36.12	137.3	-0.614
51	42.32	125.0	-0.287
52	42.11	125.4	-0.287
53	113.89	61.4	-0.787
54	115.1	60.9	-0.796
55	114.34	61.2	-0.787
56	114.04	61.3	-0.793
57	160.76	46.0	-0.577
58	160.46	46.1	-0.663
59	161.36	45.9	-0.586
60	160.76	46.0	-0.6

Table A2 (Continued)

Sample No	Effective gate oxide thickness, EOT_{ox} (nm)	Flat band capacitance, C_{FB} (pF)	Flat band voltage, V_{FB} (V)
61	192.69	39.3	-0.6
62	194.43	39.0	-0.643
63	192.69	39.3	-0.614
64	193.56	39.2	-0.629
65	239.13	32.5	-0.721
66	239.13	32.5	-0.700

Cadence netlist with modified BSIM 3 version 3 NFET model:

// Generated for: spectre

// Generated on: Apr 29 12:35:50 2010

// Design library name: cris_lib_clone_backup

// Design cell name: dcmosfet

// Design view name: schematic

simulator lang=spectre

global 0 sub!

include "/cad/cds/IBM_PDK/bicmos7hp/rel/Spectre/models/design.scs"

include "/cad/cds/IBM_PDK/bicmos7hp/rel/Spectre/models/process.scs"

// Library name: cris_lib_clone_backup

// Cell name: dcmosfet

// View name: schematic

model ntft bsim3v3

+tnom=27.0

+acnqsmod=1 elm=3

+capmod=3

+nch= 2.498E+17 tox=300E-9 xj= 1.00000E-07

+lint=9.36e-8 wint=996.5e-6

+lintnoi=1e-9

+vth0=60 k1=0.5 k2= 0 k3= 80

+dvt0= 2.812 dvt1= 0.462 dvt2= -9.17e-2

+nlx= 3.52291E-08 w0= 1.163e-6

+k3b= 2.233

+vsat= 86301.58 ua= 6.47e-9 ub= 4.23e-18 uc= -4.70628IE-11

+rdsw=0 u0= 100 wr=1

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+dwg = -6.0E-09 dwb = -3.56E-09 prwb -.213

+keta=-3.605872E-02 a1= 2.778747E-02 a2 .9

+voff=-6.735529E-02 nfactor= 1.139926 cit 1.622527E-04

+cdsc=-2.147181E-05

+cdscb= 0 dvt0w = 0 dvt1w = 0 dvt2w 0

+cdscd = 0 prwg = 0

+eta0= 1.0281729E-02 etab=-5.042203E-03

+dsub= .31871233

+pclm= 1.114846 pdiblc1 2.45357E-03 pdiblc2 6.406289E-03

+drout= .31871233 pscbe1= 5000000 pscbe2 5E-09 pdiblcb -.234

+pvag= 0 delta=0.01

+ wl = 0 ww = -1.420242E-09 wwl = 0

+ wln = 0 wwn = .2613948 ll = 1.300902E-10

+ lw = 0 lwl = 0 lln = .316394

+ lwn = 0

+kt1=-.3 kt2=-.051

+at= 22400

+ute=-1.48

+ua1= 3.31E-10 ub1= 2.61E-19 uc1 -3.42e-10

+kt11=0 prt=764.3

M1 (net7 net3 0 sub!) ntft l=144.8u w 2000u

V1 (net3 0) vsource dc=3 type=dc

V0 (net7 0) vsource dc=40 type=dc

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    digits=5 cols=80 pivrel=1e-3 ckptclock=1800
    sensfile="../psf/sens.output" checklimitdest=psf
dc dc dev=V1 param=dc start=0 stop=100 write="spectre.dc" oppoint=rawfile
    maxiters=150 maxsteps=10000 annotate=status
modelParameter info what=models where=rawfile
element info what=inst where=rawfile
outputParameter info what=output where=rawfile
designParamVals info what=parameters where=rawfile
primitives info what=primitives where=rawfile
subckts info what=subckts where=rawfile
saveOptions options save=allpub pwr=all currents=all
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