HIGH POWER DENSITY GAN BASED BOOST INVERTER AND RESONANT MODULAR MULTILEVEL BOOST CONVERTER FOR AUTOMOTIVE APPLICATIONS

A Thesis
Submitted to the Graduate Faculty
of the
North Dakota State University
of Agriculture and Applied Science

By

Jalen Craig Johnson

In Partial Fulfillment of the Requirements
for the Degree of
MASTER OF SCIENCE

Major Department:
Electrical and Computer Engineering

April 2018

Fargo, North Dakota

North Dakota State University
Graduate School

Title

HIGH POWER DENSITY GAN BASED BOOST INVERTER AND RESONANT MODULAR MULTILEVEL BOOST CONVERTER FOR AUTOMOTIVE APPLICATIONS

By

Jalen Craig Johnson

The Supervisory Committee certifies that this ***disquisition*** complies with North Dakota State University's regulations and meets the accepted standards for the degree of

MASTER OF SCIENCE

SUPERVISORY COMMITTEE:

Dong Cao
Chair

Benjamin Braaten

Zhibin Lin

Approved:

04/03/2018
Date

Benjamin Braaten
Department Chair

ABSTRACT

With the rise in demand for electric vehicles increasing, the need for high efficiency electrification systems is in high demand. One challenge is keeping full output power to the electric drives as the vehicle battery drops. This thesis presents a GaN based three-phase semi-quasi-z-source boost inverter that can produce twice the output voltage of a traditional inverter without the need for a boost converter stage. This single stage approach is great when the AC output voltage is relatively low. A second approach presented in this paper is a novel GaN based composite boost converter topology which is made up of a very efficient unregulated converter topology with an integrated partial power voltage regulation stage. This approach offers the benefits of very high efficiency from the unregulated converter stage and the regulated output voltage with the voltage regulation stage. This design can offer an estimated efficiency up to 98.6%.

ACKNOWLEDGEMENTS

I would like to thank my advisor Dr. Dong Cao for his support and expertise while pursuing my degree. I would also like to thank the help and support of my fellow SPEED lab members.

Outside of school, I would like to thank my friends and family for all of your support and encouragement while I pursued my education at NDSU. John, thank you for buying beer and keeping me sane! I especially would like to thank my parents for your never-ending support over the past few years.

Finally, I would like to thank NDSU for allowing me to receive a great education throughout my undergraduate and graduate studies. Go Bison!

DEDICATION

This work is dedicated to my Mom and my sister.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

Figure Page

LIST OF ABBREVIATIONS

RMMC .....resonant modular multilevel converter.

PPVR.....partial power voltage regulation.

DCX .....direct current transformer.

GaN .....gallium nitrate.

Si .....silicon.

dv/dt .....change in voltage over change in time.

DC .....direct current.

AC .....alternating current.

V.....volts.

A.....amps.

RMS .....root mean square.

Vrms.....root mean square voltage.

Arms.....root mean square current.

Oz. .....ounce.

DSP .....digital signal processing.

PCB .....printed circuit board.

ENIG .....electroless nickel immersion gold.

Tg .....glass transition temperature.

ZCS .....zero current switching.

IC.....integrated circuit.

Rds(on).....drain-source on resistance.

LC .....inductor.

C.....capacitor.

PWM .....pulse width modulation.

SPWM.....sinusoidal pulse width modulation.

THI.....third harmonic injection.

Hz.....hertz.

kHz.....kilohertz.

kW.....kilowatt.

µF.....microfarad.

nF .....nanofarad.

µH .....microhenry.

ns.....nanosecond.

C0G.....temperature compensating capacitor material.

3D.....three-dimensional.

1. INTRODUCTION

The heart of modern electric vehicles is a voltage source in the form of a battery pack and an inverter to power the motor drives in the drivetrain. This sounds simple from an overview, however once you start peeling back the layers of the design you can see some problems with standard topologies. One main challenge is that as the vehicle is driven, the battery pack loses voltage. To maintain full power output of the inverter, a boost converter needs to be added and placed between the battery pack and the inverter so the inverter can receive rated voltage while the battery voltage drops. Standard boost converters pose many problems. These problems range from lower power density, low efficiency, and very high switching device current and voltage stress. There are two main solutions to replace the less desired traditional boost converter.

The first way is to implement a boost inverter. A boost inverter is an inverter that can generate a higher output voltage than a traditional three-phase inverter with the same input voltage. This approach can eliminate the need for a boost converter while still keeping the same output voltage level and it also reduces the number of switching devices needed in the system. The semi-quasi-z-source inverter presented in Chapter 2 is the boost inverter topology that has been developed to solve this problem. The topology also solves some other problems that are presented with the use of a traditional three-phase inverter.

One of the main problems with traditional three-phase inverters is that the output voltage is directly a PWM voltage. This large dv/dt event is very hard on the windings of an electric motor. This hard switching causes the windings to break down and motor bearing to start wearing out prematurely due to bearing currents. The traditional way to mitigate this issue is to add filtering to the output of the inverter to create a sinusoidal output voltage. This works, but the passive component size becomes very large because the switching frequency of most Si

based inverters for motor drive applications is 4-20 kHz [5], [6]. A second problem is that if the inverter source and the load cannot share the same ground, there is the problem of leakage currents in the system that needs to be handled. This adds complexity and cost to the system [7].

The proposed inverter topology that is featured in Chapter 2, the semi-quasi-z- source inverter, handles all of these problems very well. The inverter can generate sinusoidal output voltage thanks to the inherit filtering in the inverter topology. The inverter can also utilize GaN switching devices so the switching frequency can be greatly increased which greatly reduces the passive component size. As mentioned above, this topology generates a high conversion ratio so lower input voltages are required for many applications which can eliminate the need for a boost converter. Also, the load and inverter input grounds can be shared to common mode and leakage current issues are eliminated. The design of a GaN based three-phase semi-quasi-z-source inverter prototype is featured in Chapter 3.

A second way to eliminate the traditional boost converter is to develop a more efficient way to boost up the voltage from the battery pack to the DC link of the inverter. As mentioned above, the traditional boost converter suffers from low efficiency and very high switch voltage and current stresses when the converter is operating at high conversion ratios. To overcome these problems, topologies like in [9]-[13] have been developed. These new topologies offer very high efficiency system efficiencies with lower switch voltage and current stresses than the traditional boost inverter. These topologies use multiple converter topologies combined in one overall system to form a "composite" converter that utilizes a non-regulated DC Transformer stage (DCX) and a regulated stage to achieve output voltage regulation which is very important for motor drive applications when the DC-link voltage is critical motor control. The topologies mentioned above mainly consist of a full-bridge converter with a boost converter [11], [12] or a

buck converter [9], [10] in series with the output but share the same input voltage. The full-bridge converter acts as the DCX stage while the other converters offer the voltage regulation. The system efficiency is high because the DCX stage is processing most of the overall power while the less efficient buck or boost converter processes a small amount of power to keep the output voltage regulated. The proposed composite modular boost converter topology that is featured in Chapter 4 also combines a DCX stage and a regulation stage. However, the proposed topology utilizes a modular, transformer-less resonant converter topology that offers even lower switch voltage and current stress than the topologies mentioned above. The design of a GaN based 4 kW prototype is discussed in Chapter 5.

2. THREE-PHASE SEMI-QUASI-Z-SOURCE INVERTER ANALYSIS AND OPERATION

2.1. Inverter Operation

The semi-quasi-z-source inverter is derived from the z- source inverter [1],[2]. In a z-source inverter, the LC network is on the DC link input side of the inverter. However, in the semi-quasi-z-source inverter, the LC network components are on the AC output side of the inverter. Because the components are on the AC side, the component size can be reduced because the passive components can take advantage of the high switching frequencies in the switch network. The three-phase inverter topology can be seen in Figure 2.1.

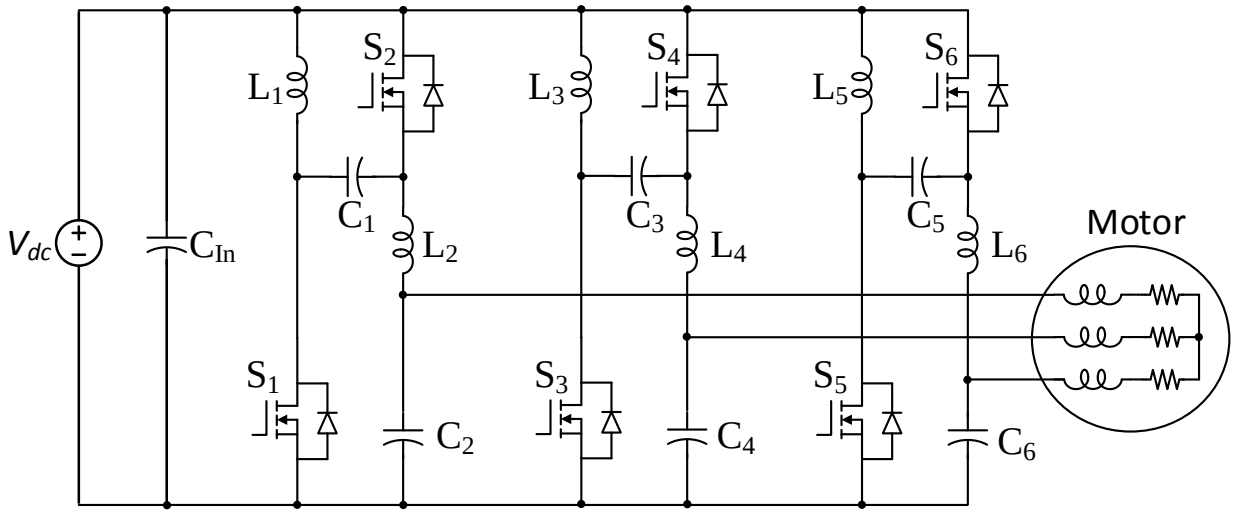

Figure 2.1. Three-Phase Semi-Quasi-Z-Source Inverter Topology

However, for operation analysis, the inverter can simply be broken down to a single-phase inverter for explanation [2],[3]. Then three single-phase inverters can be built up together to generate the three-phase inverter [8]. The single-phase inverter can be seen in Figure 2.2.

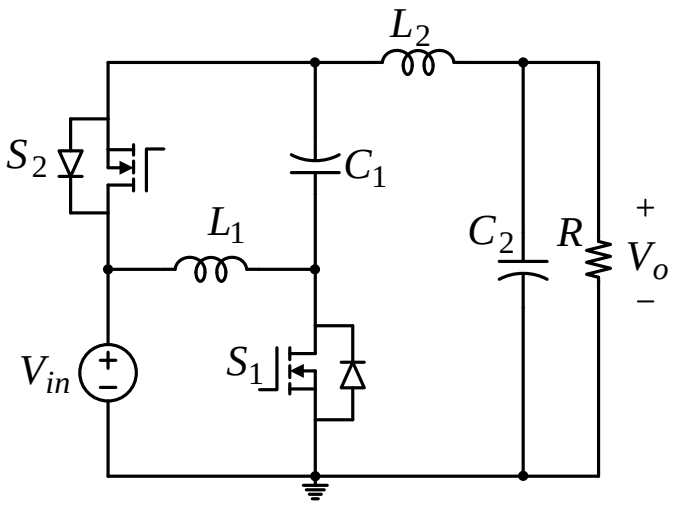

Figure 2.2. Single-Phase Semi-Quasi-Z-Source Inverter Topology

The inverter operates the two switching devices in a complementary manner, so the inverter has two switching states. The first switching state is when S_1 is on and the second switching state is when S_2 is on. The first switching state can be seen in Figure 2.3. When S_1 is on, the input voltage and capacitor C_1 charge inductors L_1 and L_2. When L_1 and L_2 are being charged the current increases and the voltage across the inductors increase.

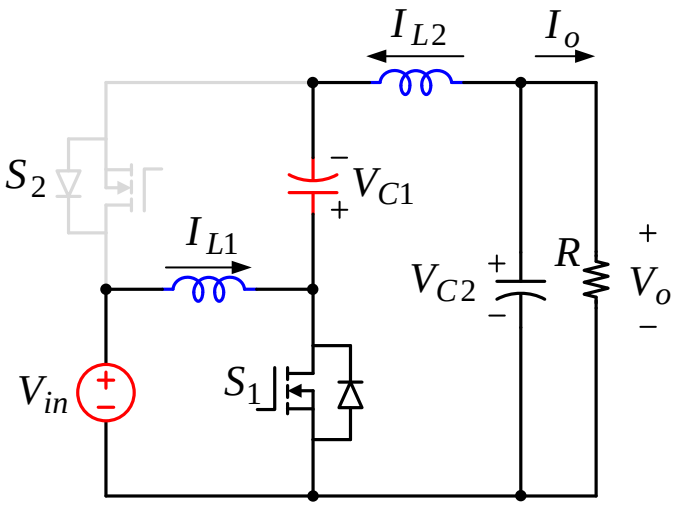

Figure 2.3. Current Loops when S_1 is On

The second switching state can be seen in Figure 2.4. When S_2 is on, the inductors become the source and their current decreases and capacitor C_1 keeps the voltage clamped while the voltage across L_1 changes during each switching cycle.

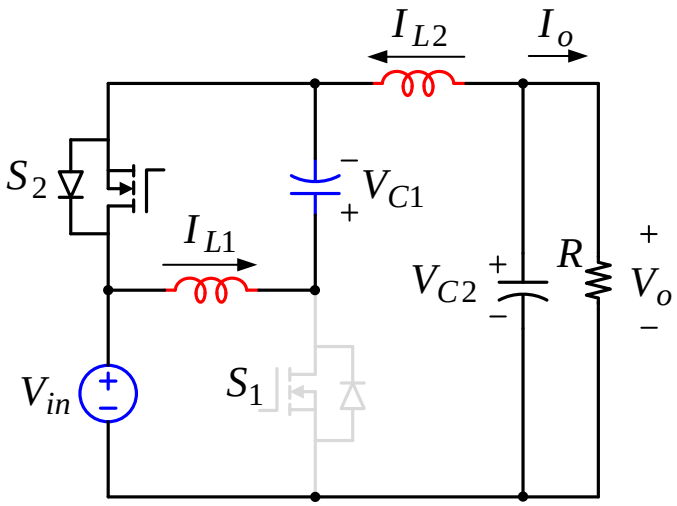

Figure 2.4. Current Loops when S_2 is On

The inverter has a sinusoidal output voltage that is shown as (Eq. 2.1). From (Eq. 2.1) it can be seen that the single-phase inverter can generate both positive and negative output voltage. This feature is what allows three single-phase semi-quasi-z-source inverters to be combined to form a three-phase inverter. The modulation index can be defined as (Eq. 2.2) and the relationship between the input and output voltage can be shown by (Eq. 2.3). By substitution of (Eq. 2.1) and (Eq. 2.2) into (Eq. 2.3) we can derive the duty cycle equation for S_1 (Eq. 2.4). The duty cycle equation for S_2 is 1–D also shown as D' or (Eq. 2.5). The equations for the voltage on C_1 and C_2 are shown in (Eq. 2.6) and (Eq. 2.7), respectively. The equations for the current through L_1 and L_2 can be defined by (Eq. 2.8) and (Eq. 2.9), respectively.

$$V_0 = V\sin(\omega t) \qquad \text{(Eq. 2.1)}$$

$$M = \frac{V}{V_{In}} \qquad \text{(Eq. 2.2)}$$

$$\frac{V_O}{V_{In}} = \frac{1\text{-}2D}{1\text{-}D} \quad \text{(Eq. 2.3)}$$

$$D = \frac{1\text{-}M\sin(\omega t)}{2\text{-}M\sin(\omega t)} \quad \text{(Eq. 2.4)}$$

$$D' = \frac{1}{2\text{-}M\sin(\omega t)} \quad \text{(Eq. 2.5)}$$

$$V_{C1} = \frac{DV_{In}}{1\text{-}D} \quad \text{(Eq. 2.6)}$$

$$V_{C2} = V_O \quad \text{(Eq. 2.7)}$$

$$I_{L1} = \frac{DI_O}{1\text{-}D} \quad \text{(Eq. 2.8)}$$

$$I_{L2} = -I_O \quad \text{(Eq. 2.9)}$$

The modulation scheme for the single-phase and three-phase semi-quasi-z-source inverters will be presented in the next section.

2.2. Inverter Modulation

2.2.1. Modified Single-Phase SPWM

The modulation strategy of the semi-quasi-z-source inverter is similar to the standard SPWM modulation schemes that are used for traditional inverter topologies. However, the reference signal has been modified as shown in (Eq. 2.4) and (Eq. 2.5). While standard modulation schemes are based on the modulation function for D. In this case, the modulation reference signal will be the function for D'. This allows for less processing power to be used to generate the gate signals. The modified modulation scheme for the single-phase semi-quasi-z-source inverter is shown in Figure 2.5. The modulation index of the reference signal is 1. The duty cycle of the complementary, D, switch function shown in (Eq. 2.4) is shown in Figure 2.6.

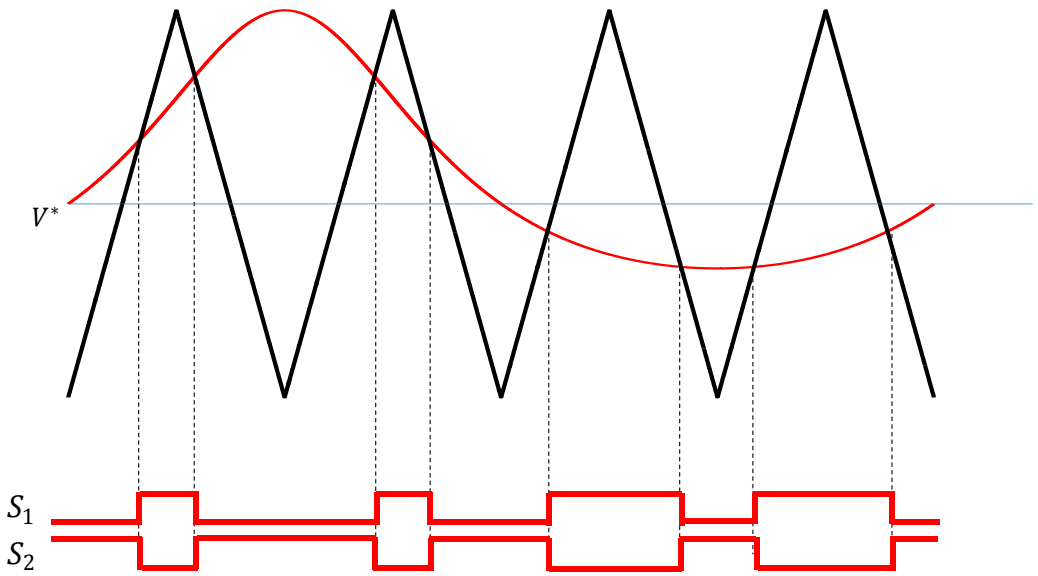

Figure 2.5. Modified SPWM Modulation for Single-Phase Semi-Quasi-Z-Source Inverter

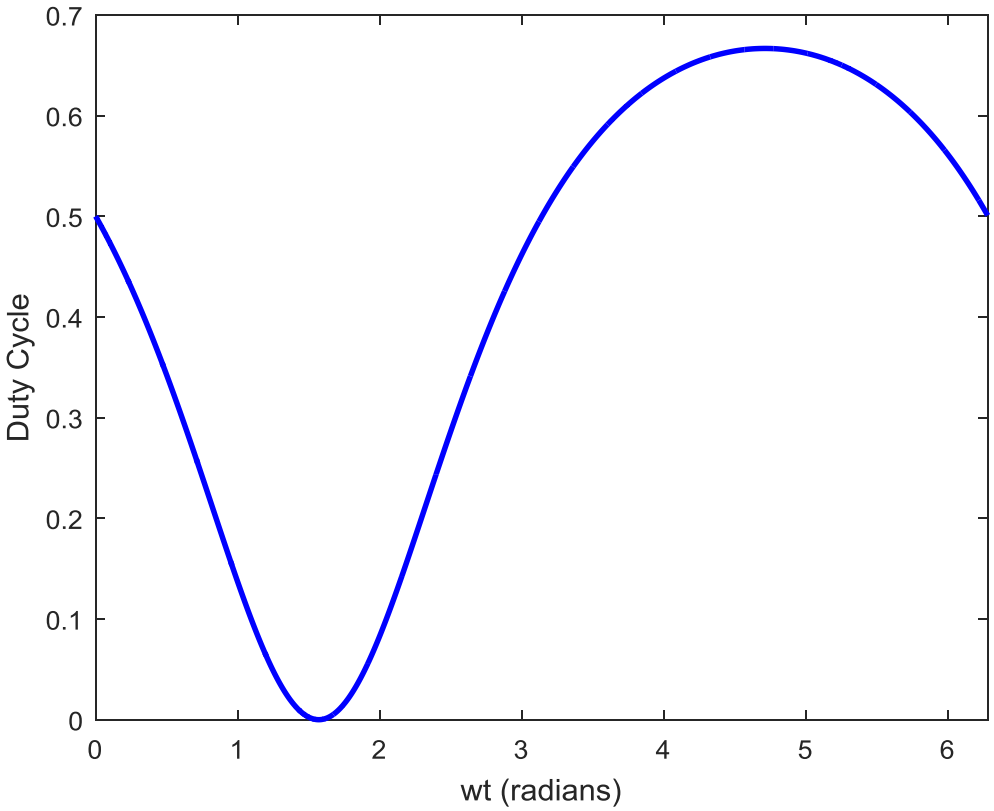

Figure 2.6. Duty Cycle of S_1 (Eq. 2.4) Over One Fundamental Period

2.2.2. Modified Three-Phase SPWM

As mentioned above, a three-phase inverter can be made by using three single-phase semi-quasi-z-source inverters. This is because each single-phase inverter can generate both positive and negative voltages. This is shown by the output voltage of a single-phase inverter in (Eq. 2.1). When a three-phase inverter is formed, the line-to-line output voltage is shown in (Eq. 2.10). The line-to-neutral voltage still follows (Eq. 2.1)

$$V_0=\sqrt{3}V\sin(\omega t) \qquad \text{(Eq. 2.10)}$$

Generating the PWM signals is very simple. The same reference signal function as shown in (Eq. 2.5) is used, however two more signals are added and shifted so the three signals are 120 degrees apart. This modulation scheme is very similar to SPWM for traditional three-phase inverters. We are just modifying the reference sinusoidal signal to the modified signal required for the inverter. The three-phase SPWM modulation is shown in Figure 2.7.

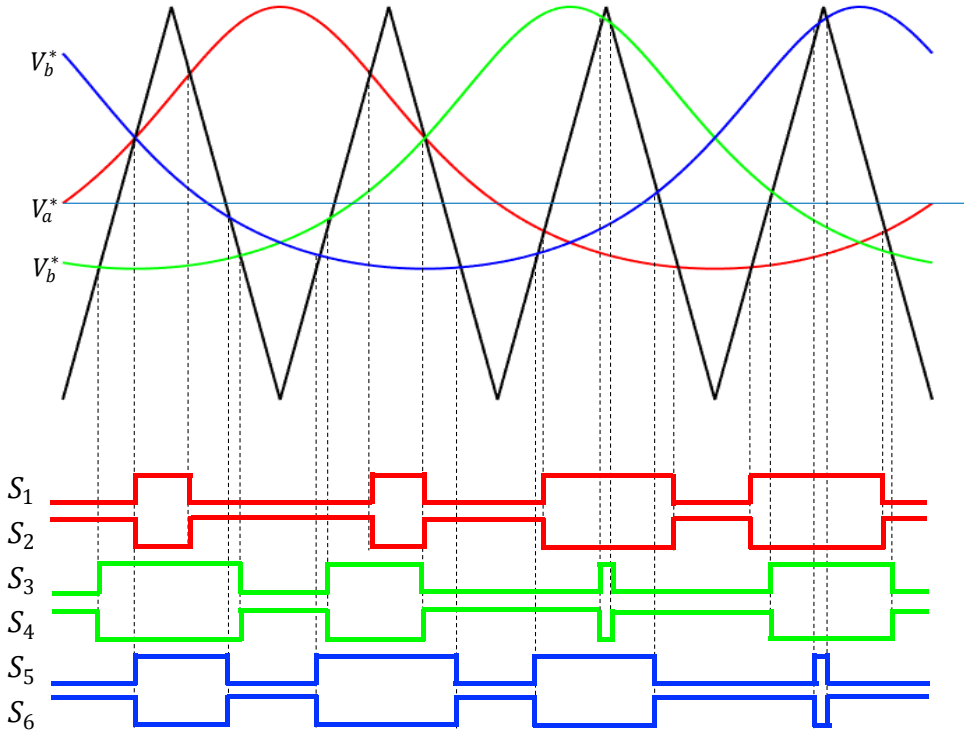

Figure 2.7. Three-Phase Modified SPWM Modulation

2.2.3. Modified Three-Phase SPWM with THI

Because this inverter is being used for a motor drive application, third harmonic injection can be used to generate a higher output voltage while keeping the input voltage unchanged. Because third order sinusoidal harmonics are common in all three reference signals, they can add to the reference signal to allow the modulation index to be increased from 1 to 1.1547. This increases the output voltage of the inverter. Now, harmonics are generally not a desired thing to be added to the output voltage of an inverter. However, since the inverter is driving an electric motor, the third harmonics are common in all three phases which are feeding the stator windings of the motor. The third order harmonics that are injected is a common mode signal within the motor windings. Because it is common with each phase voltage the motor windings don't even see it as it is canceled out between the phases. So the motor only sees the pure sinusoidal fundamental signal that can be extracted using Fourier expansion. The sinusoidal third harmonic signal that is added to the sinusoidal reference signal is shown in (Eq. 2.11). It is also shown in Figure 2.8. The resultant reference modulation signal, excluding the phase angle of the signal is shown in (Eq. 2.12). The SPWM modulation strategy with THI based from (Eq. 2.12) is shown in Figure 2.9.

$$\text{Third\_Harmonic} = \frac{1}{6}\sin(3\omega t) \qquad \text{(Eq. 2.11)}$$

$$D_{\text{With\_Third\_Harmonic}} = \frac{1}{2\text{-}M\left(\sin(\omega t) + \frac{1}{6}\sin(3\omega t)\right)} \qquad \text{(Eq. 2.12)}$$

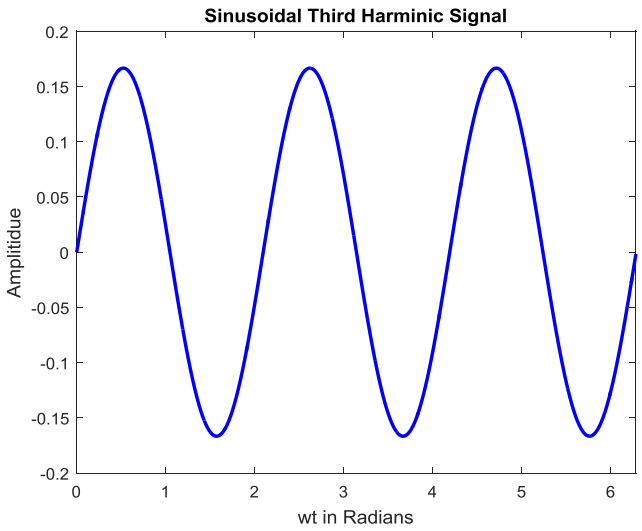

Figure 2.8. Sinusoidal Third Harmonic Signal

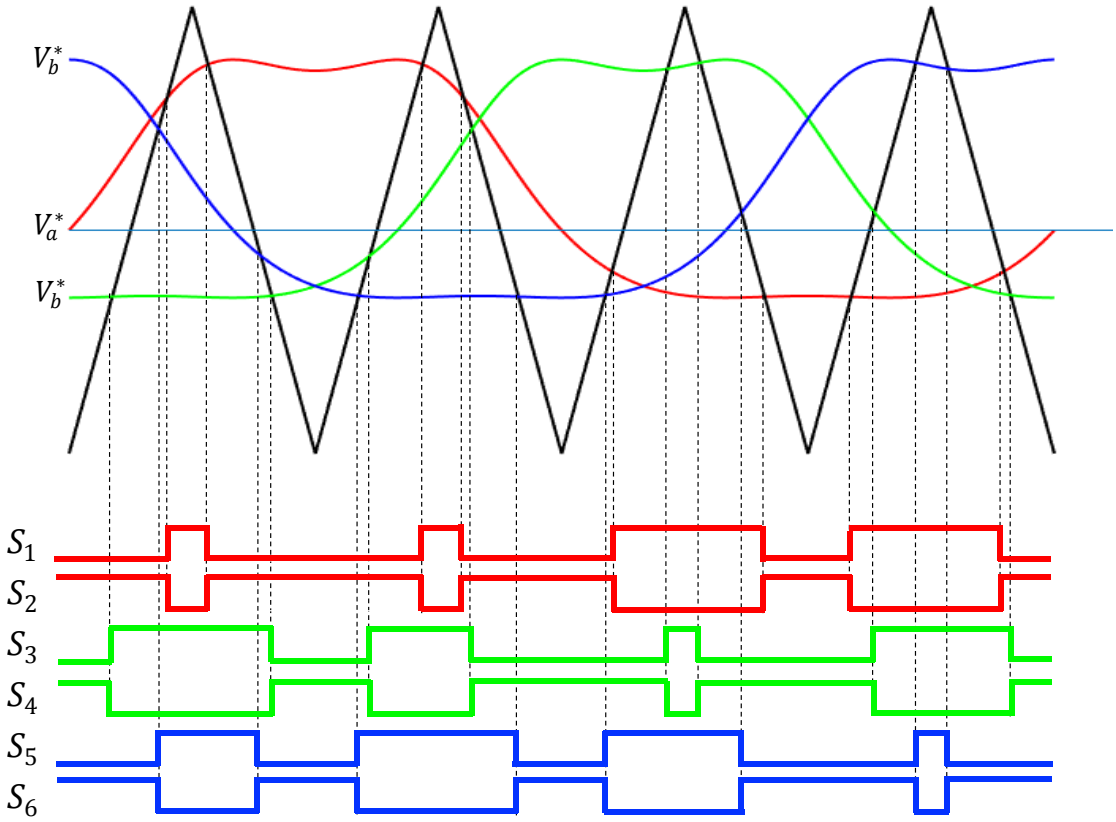

Figure 2.9. Three-Phase Modified SPWM Modulation with THI

To build off of the sinusoidal third harmonic injection mentioned above. This idea can be extended to inject all odd triplen order harmonics. This is achieved by using a triangular signal rather than the third harmonic sinusoidal signal used above. The triangular signal contains all odd triplen order harmonics. It is implemented the same way as the third harmonic injection, but the third harmonic signal in (Eq. 2.12) is replaced with the triangle signal shown in Figure 2.10. The triangle signal has an amplitude of 0.25 and a frequency three times higher than the fundamental frequency. The SPWM modulation strategy with all triplen injection is shown in Figure 2.11.

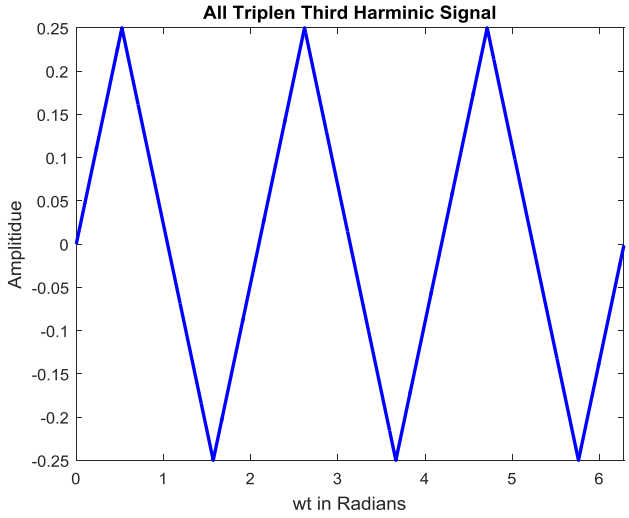

Figure 2.10. Triangular Third Harmonic Injection Signal

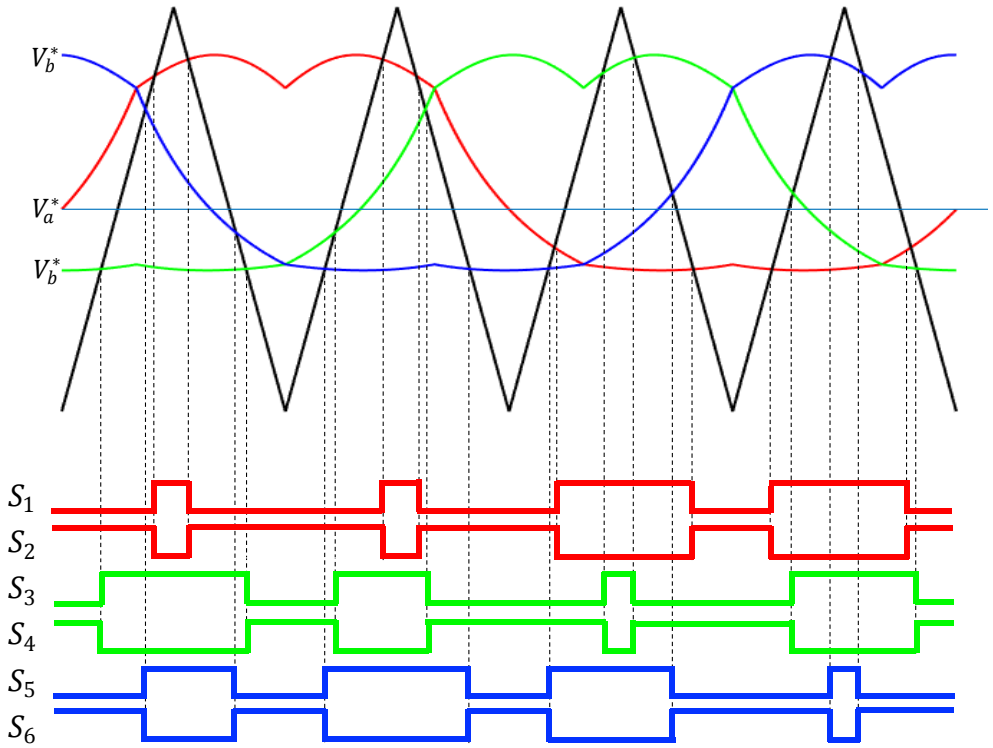

Figure 2.11. Three-Phase Modified SPWM Modulation with All Triplen Injection

Both the third harmonic injection and the all triplen injection offer the same output voltage of the inverter as the modulation index range of each can both increased to 1.1547.

2.3. Conversion Ratio Comparison

As mentioned earlier in the chapter, the semi-quasi-z-source inverter has a high conversion ratio which is two times higher than a traditional three-phase inverter. This allows the inverter to produce the same output voltage with half of the input voltage. The voltage conversion ratio comparisons between these inverters can be seen in Table 2.1. Figure 2.12 features a graph that shows input voltage versus output voltage of the semi-quasi-z-source inverter and a traditional inverter with SPWM and SPWM with THI modulation schemes.

Table 2.1. Conversion Ratio Comparison

Inverter Topology	Modulation Scheme	Conversion Ratio
Semi-Quasi-Z-Source	Modified SPWM	1.225
Semi-Quasi-Z-Source	Modified SPWM w/THI	1.414
Traditional	SPWM	0.612
Traditional	SPWM w/THI	0.707

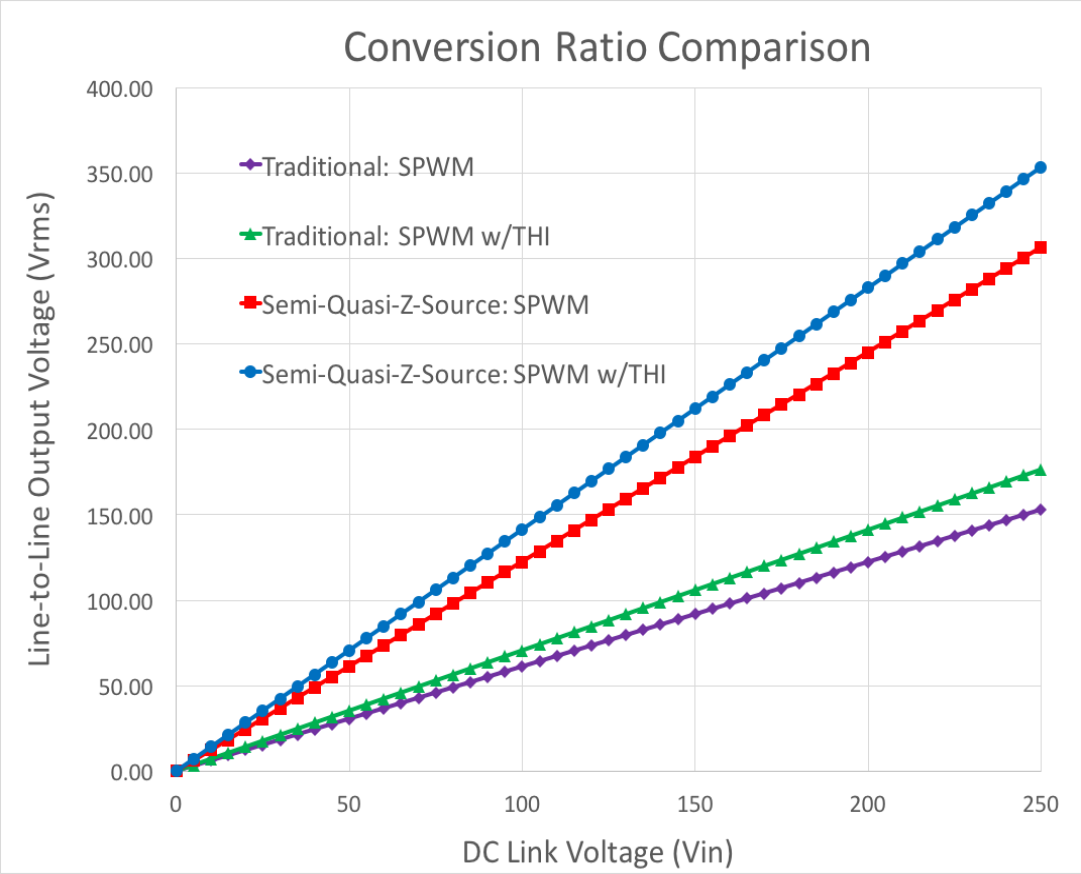

Figure 2.12. Inverter Input Voltage vs. Line-to-Line RMS Output Voltage

As shown above, the semi-quasi-z-source topology has a higher conversion ratio than the traditional inverter topology. In order for the traditional inverter to produce the same output

voltage as the semi-quasi-z-source inverter, a boost converter needs to be added to the input of the traditional inverter to increase the DC link voltage. The boost converter would need to double the DC link voltage of the traditional inverter. Based on the duty cycle equation of a boost converter (Eq. 2.13) the duty cycle of the boost converter needs to be 0.5 in order to allow the traditional inverter to match the output of the three-phase semi-quasi-z-source inverter. Device stress analysis and comparison between the three-phase semi-quasi-z-source inverter and the traditional three-phase inverter with a boost converter input is discussed in the next section. The topology of a traditional three-phase inverter with a boost converter is shown below in Figure 2.13.

$$\frac{V_0}{V_{In}} = \frac{1}{1\text{-}D} \qquad \text{(Eq. 2.13)}$$

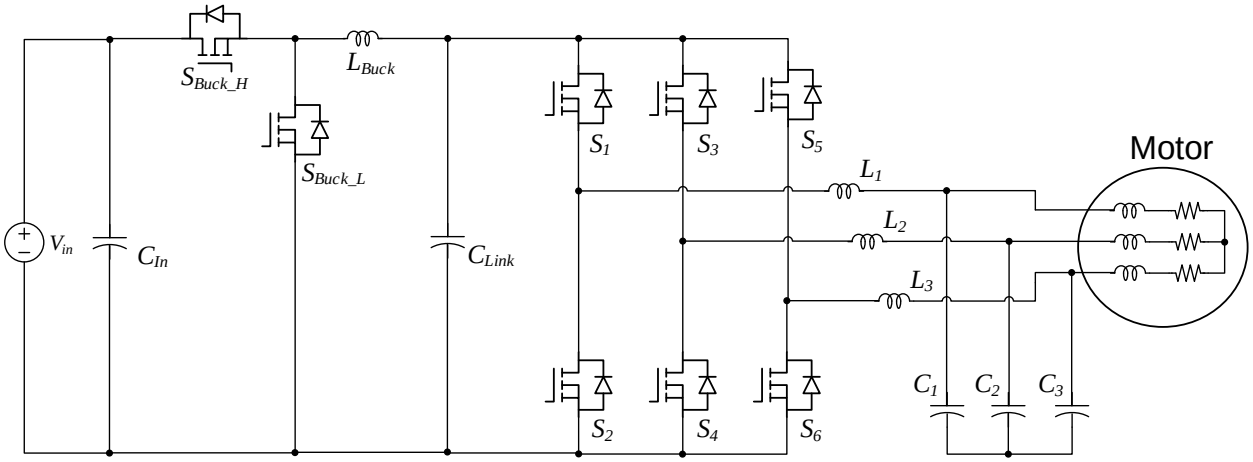

Figure 2.13. Traditional Three-Phase Inverter with Boost Converter

2.4. Device Stress Analysis and Comparison

2.4.1. Three-Phase Semi-Quasi-Z-Source Inverter Device Stress Analysis

The switch voltage stress for the semi-quasi-z-source inverter can be shown by (Eq. 2.14). The switch current stress can be depicted by (Eq. 2.15). Unlike [4], this paper isn't too concerned with the peak current stress. The RMS current stress was derived for the switches for

the semi-quasi-z-source topology. The RMS current is the focus, because peak currents for a very brief amount of time won't cause damage to the switch if properly designed. The RMS current stress is what will determine the current rating of the switching device. Proper PCB design and cooling will handle the current peak current and maintain proper operating temperature of the switching device. The peak voltage is important because an overvoltage can damage the switching device. The derived RMS current stress equation for S_1 and S_2 is detailed by (Eq. 2.16) and (Eq. 2.17), respectively. These derived functions can be used to calculate the switch current stress without the need for complex simulation software. The function shown in (Eq. 2.18) calculates the absolute value of the current for (Eq. 2.16) and (Eq. 2.17). The duty cycle equations for the RMS current stress functions for S_1 and S_2 are detailed by (Eq. 2.19) and (Eq. 2.20), respectively. A Boolean function (Eq. 2.21) is multiplied with (Eq. 2.18) when (Eq. 2.19) and (Eq. 2.20) are greater than zero. This is to scale the current function pulse width according to the value of the duty cycle during that switching event. The number of switching periods per fundamental period is calculated by (Eq. 2.22). The capacitor ripple voltage on C_1 and the inductor ripple current in L_1 are shown in (Eq. 2.23) and (Eq. 2.24), respectively.

$$V_S = \frac{MV_{In}}{1\text{-}D} \quad \text{(Eq. 2.14)}$$

$$I_S = \left(-2\sin(\omega t) + M\left(\sin(\omega t)\right)^2\right) I \quad \text{(Eq. 2.15)}$$

$$I_{S1\_RMS} = \sum_{n=1}^{N} u[D_{S1}(n)]\, K \quad \text{(Eq. 2.16)}$$

$$I_{S2\_RMS} = \sum_{n=1}^{N} u[D_{S2}(n)]\, K \quad \text{(Eq. 2.17)}$$

$$K = \sqrt{\left(\left(-2\sin(\omega t) + M\left(\sin(\omega t)\right)^2\right) I\right)^2} \quad \text{(Eq. 2.18)}$$

$$D_{S1}(n) = \frac{1\text{-}M\sin\left(\frac{2\pi n}{N}\right)}{2\text{-}M\sin\left(\frac{2\pi n}{N}\right)};\ n = 1 \ldots N \quad \text{(Eq. 2.19)}$$

$$D_{S2}(n)=\frac{1}{2\text{-}M\sin\left(\frac{2\pi n}{N}\right)};\ n=1\ldots N \quad \text{(Eq. 2.20)}$$

$$u[D_{S\#}(n)]=\begin{cases}1, & T_S(n)\leq T_S D_{S\#}(n)\\ 0, & \text{Otherwise}\end{cases} \quad \text{(Eq. 2.21)}$$

$$N=\frac{f_{switching}}{f_{fundamental}} \quad \text{(Eq. 2.22)}$$

$$\Delta V_{C1}=\frac{I_S}{f_{switching}(2\text{-}M\sin(\omega t))C_1} \quad \text{(Eq. 2.23)}$$

$$\Delta I_{L1}=\frac{V_{In}(1\text{-}M\sin(\omega t))}{f_{switching}(2\text{-}M\sin(\omega t))L_1} \quad \text{(Eq. 2.24)}$$

The RMS switch current stress was calculated using MATLAB by using the derived equations above. The calculation was based on a 10 kW inverter with a 200 V input voltage and a power factor of 1, and modulation index of 1. The resultant plots of the switch current stress of switch S_1 and switch S_2 are shown in Figure 2.14 and Figure 2.15, respectively.

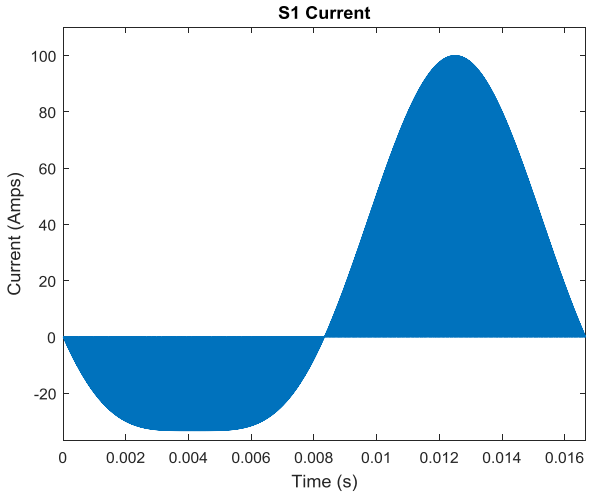

Figure 2.14. Three-Phase Semi-Quasi-Z-Source Inverter S_1 Current Stress using MATLAB

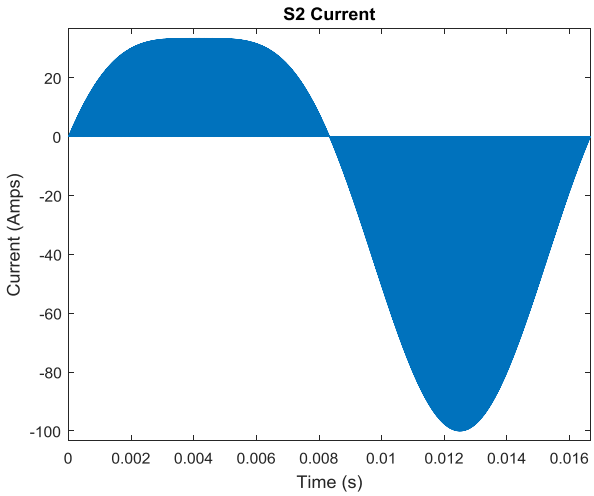

Figure 2.15. Three-Phase Semi-Quasi-Z-Source Inverter S_2 Current Stress using MATLAB

2.4.2. Traditional Three-Phase Inverter with Boost Converter Device Stress Analysis

The switch voltage stress for a traditional inverter with a boost converter can be shown by (Eq. 2.25). The switch current stress for the inverter switches and the boost converter switches are shown by (Eq. 2.26) and (Eq. 2.27), respectively. Like the analysis in the previous section, the RMS current stress of the switching devices are what are important for the inverter design. The RMS current stress on the inverter switches is found with (Eq. 2.28) and the RMS current stress on the boost converter switch is (Eq. 2.29). The function shown in (Eq. 2.30) calculates the absolute value of the current for (Eq. 2.28) and (Eq. 2.29). The duty cycle equations for the RMS current stress functions for the inverter switches and the boost converter switches are (Eq. 2.31) and (Eq. 2.32), respectively. The function (Eq. 2.21) is also used in (Eq. 2.28) and (Eq. 2.29) to form the switching pulse widths.

$$V_{Traditional\_Inverter\_S} = V_{Boost\_Out} \quad \text{(Eq. 2.25)}$$

$$I_{Traditional\_Inverter\_S} = \sin(wt) I_{Traditional\_Inverter\_O} \quad \text{(Eq. 2.26)}$$

$$I_{Boost\_S} = \frac{P_{In}}{V_{In}} \quad \text{(Eq. 2.27)}$$

$$I_{S\_Trad\_RMS} = \sum_{n=1}^{N} u[D_{S\_Trad}(n)]\, K_{Trad} \quad \text{(Eq. 2.28)}$$

$$I_{S1\_Boost\_RMS} = \sum_{n=1}^{N} u[D_{S1\_Boost}(n)] \sqrt{I_{Boost\_S}{}^2} \quad \text{(Eq. 2.29)}$$

$$K_{Trad} = \sqrt{(M\sin(wt) I_{Traditional\_Inverter\_O})^2} \quad \text{(Eq. 2.30)}$$

$$D_{S\_Trad}(n) = M\sin\left(\frac{2\pi n}{N}\right); n = 1 \ldots N \quad \text{(Eq. 2.31)}$$

$$D_{S1\_Trad}(n) = M\sin\left(\frac{2\pi n}{N}\right); n = 1 \ldots N \quad \text{(Eq. 2.32)}$$

The RMS switch current stress was calculated using MATLAB by using the derived equations above. The calculation was based on a 10 kW inverter with a 200 V input voltage and a power factor of 1, modulation index of 1, and boost converter duty cycle of 0.5. The resultant plots of the switch current stress of the inverter switches and boost converter switches are shown in Figure 2.16 and Figure 2.17, respectively.

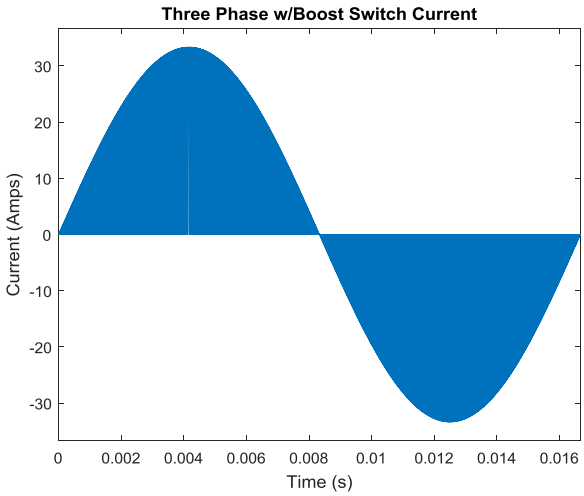

Figure 2.16. Traditional Three-Phase Inverter Switch Current Stress using MATLAB

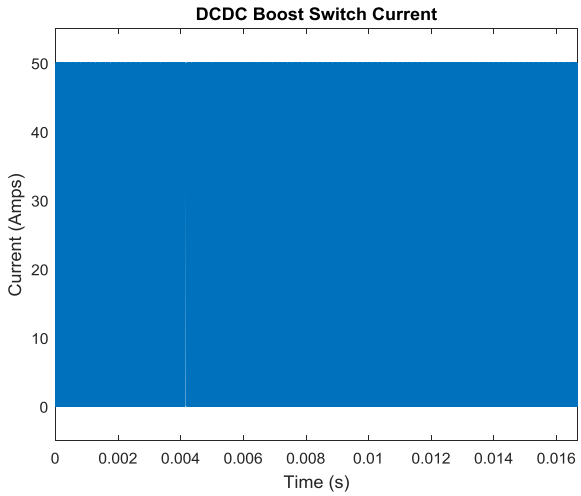

Figure 2.17. Boost Converter Switch Current Stress using MATLAB

2.4.3. Device Stress Comparison

Voltage and current stress comparisons between the semi-quasi-z-source and the traditional inverter with a boost converter input will be analyzed in this section. A 10 kW inverter example will be compared in Table 2.2 and Table 2.3. These values were selected so each inverter has the same input and output voltage. The switch voltage stress results are shown in Table 2. The voltage stress is higher on the semi-quasi-z-source and the RMS current stress is higher than the traditional inverter with a boost converter. The RMS current stress results are shown in Table 3. The semi-quasi-z-source topology has a higher current stress than the traditional inverter switches, but the current stress on the boost converter switch lies between the two values of the semi-quasi-z-source inverter. Although the semi-quasi-z-source topology has a higher switch voltage and current stress, it has less switching devices. The boost converter adds switching devices to the system. There are at least two more switches required, but in reality it is more than two because switches will need to be put in parallel to handle the current in the boost converter. Also, the semi-quasi-z-source converter doesn't need the very large boost converter inductor. The magnetic components of the semi-quasi-z-source are shifted to the higher voltage output side so the current rating and inductance of the devices is lower than that of the boost

converter input. Getting a large enough inductor to handle the current stress and current ripple requirements will put a damper on the system in regards to cost and power density. The semi-quasi-z-source takes advantage of high switching frequencies to reduce passive component size and there is a minimized number of switching devices. A GaN device is a great option for this topology because of the switching frequency capability and the low number of switching devices needed. This results in a cheaper and more power dense system than that of a traditional inverter with a boost converter input.

Table 2.2. Voltage Stress Comparison

Inverter Parameters	Inverter Topology	Input Voltage Stress Ratio (V_S/V_{in})	Switch Voltage Stress	Output Voltage Stress Ratio (V_S/V_o)
V_{in}= 200 V V_o= 245 V_{ll} M=1	Semi-Quasi-Z-Source	3	600 V	2.45
V_{in}= 200 V V_o= 245 V_{ll} M=1, D=0.5	Traditional with Boost Converter	2	400 V	1.63

Table 2.3. Current Stress Comparison

Inverter Parameters	Inverter Topology and Switching Component	RMS Current Stress Ratio ($I_{S\#\_RMS}/I_{O\_RMS}$)	RMS Switch Current Stress
Io_rms= 23.56 A	Semi-Quasi-Z-Source S_1	1.6586	39.09 A
	Semi-Quasi-Z-Source S_2	1.4145	33.33 A
	Traditional Inverter S_1	0.7072	16.66 A
	Boost Converter S_1	1.5002	35.35 A

2.5. Simulation Results

The simulation results are for a 10 kW system with an input voltage of 200 V. The modulation index was set to 1. The capacitor voltage ripple calculations were based on 5% voltage ripple and the inductor current ripple calculation were based on a 30% current ripple. From (Eq. 2.23), the capacitor values used in the simulation are 11.1 µF and from (Eq. 2.24) the inductor values used are 66.7 µH. A resistive load of 6 Ohms is used to showcase the sinusoidal output voltage of the semi-quasi-z-source inverter topology. The simulation used the topology featured in Figure 2.1 and used the modified SPWM modulation method showcased in the previous section. Figure 2.18 is the line-to-line output voltage and Figure. 2.19 is the phase current. Figure 2.20 and Figure 2.21 show the switch voltage and current stress for S_1. Figure 2.22 and Figure 2.23 show the switch voltage and current stress for S_1. Figure 2.24 shows the voltage stress on C_1 and Figure 2.25 the current stress on L_1. By comparing the simulation results with the calculated switch current using MATLAB, it is shown that the results are the same.

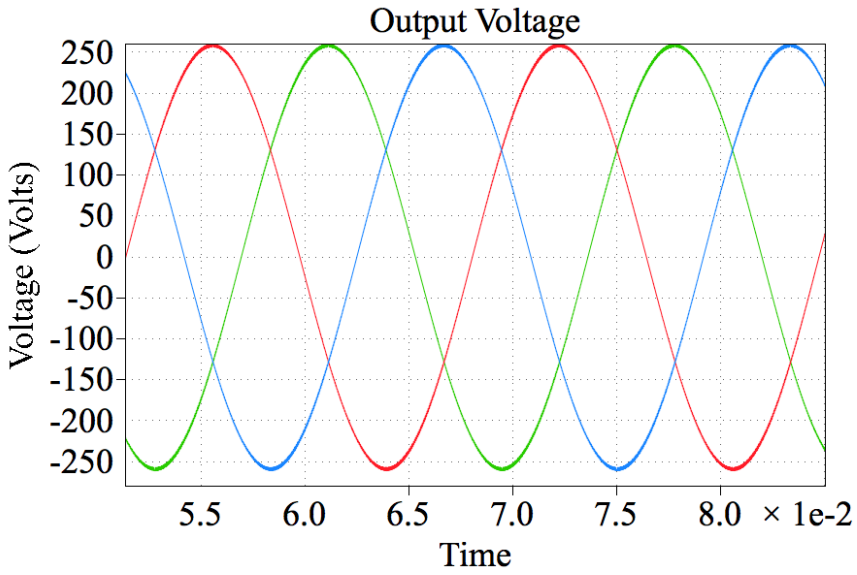

Figure 2.18. Three-Phase Semi-Quasi-Z-Source Line-to-Line Output Voltage

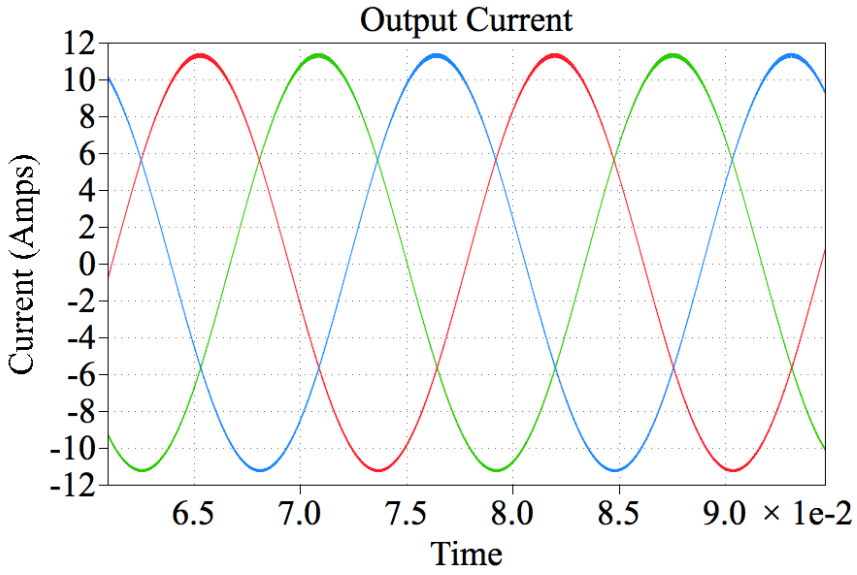

Figure 2.19. Three-Phase Semi-Quasi-Z-Source Line-to-Line Output Current

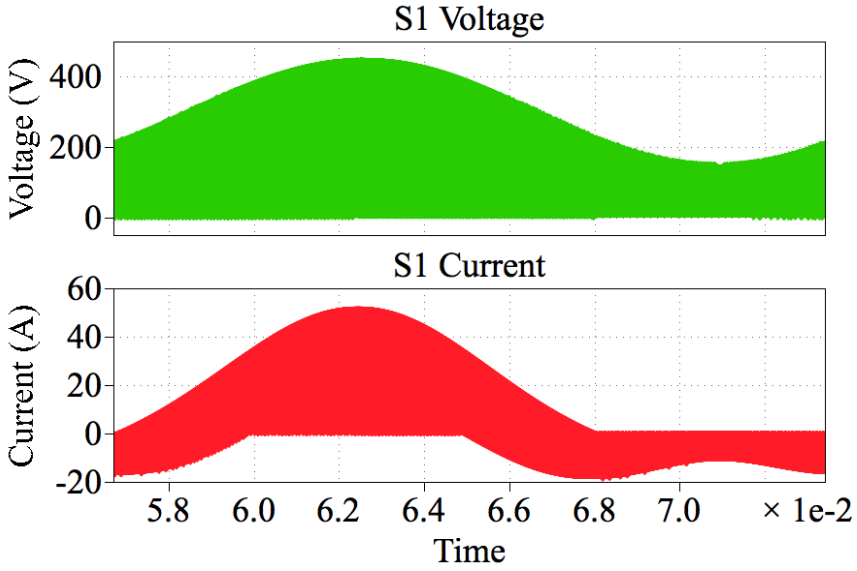

Figure 2.20. Three-Phase Semi-Quasi-Z-Source S_1 Voltage and Current: One Fundamental Cycle

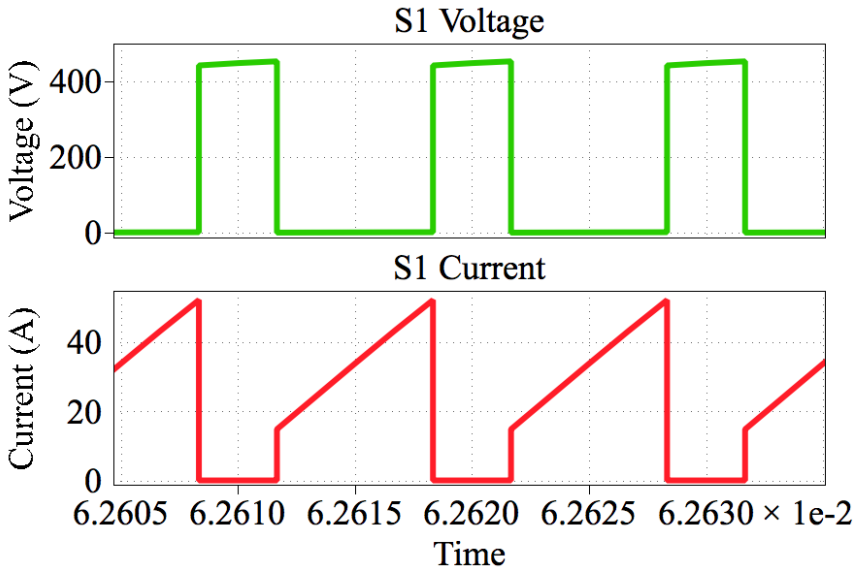

Figure 2.21. Three-Phase Semi-Quasi-Z-Source S_1 Voltage and Current: Three Switching Cycles

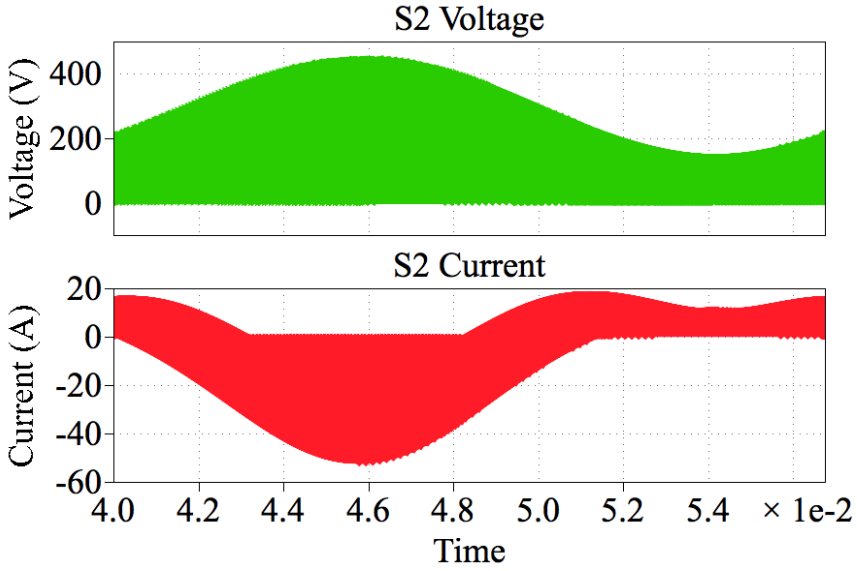

Figure 2.22. Three-Phase Semi-Quasi-Z-Source S_2 Voltage and Current: One Fundamental Cycle

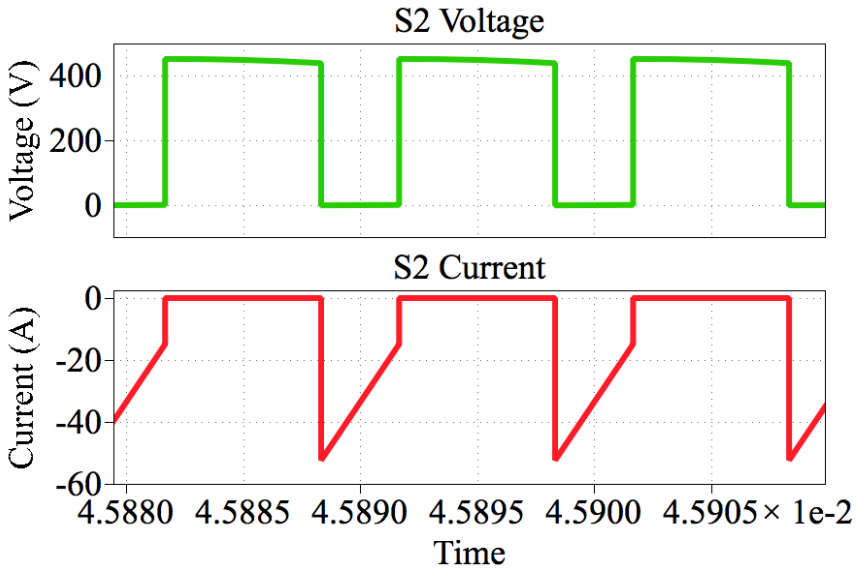

Figure 2.23. Three-Phase Semi-Quasi-Z-Source S_2 Voltage and Current: Three Switching Cycles

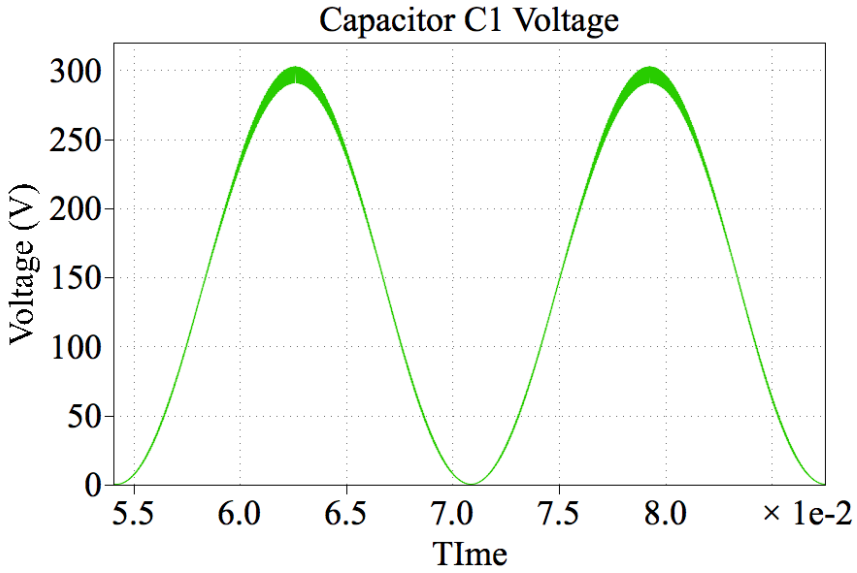

Figure 2.24. C_1 Voltage: Two Fundamental Cycles

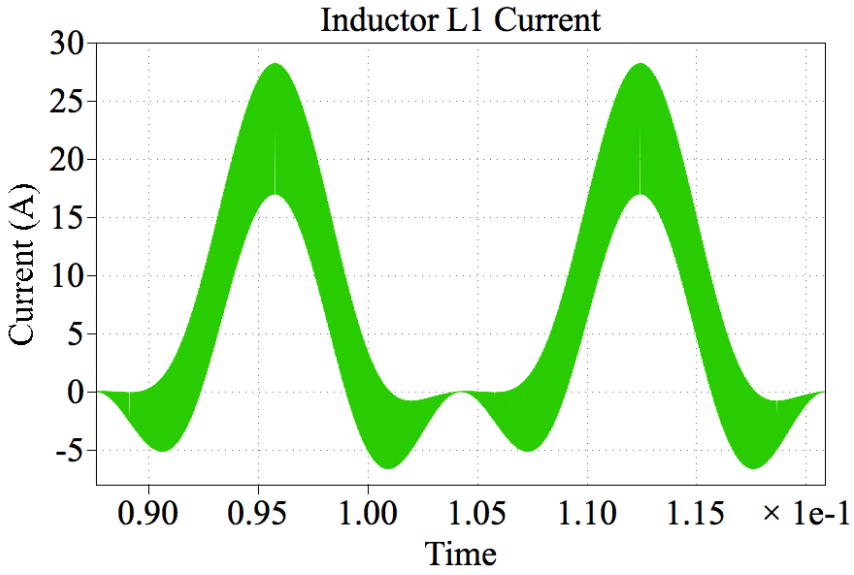

Figure 2.25. L_1 Current: Two Fundamental Cycles

3. THREE-PHASE SEMI-QUASI-Z-SOURCE INVERTER PROTOTYPE DESIGN

3.1. 2.5 kW Three-Phase Semi-Quasi-Z-Source Prototype Design

A 2.5 kW prototype was developed following the topology that is featured in Figure 2.1. The design was based around a 130 V input utilizing third harmonic injection. The expected output voltage is 183 Vrms so the prototype has an output current of 8 Arms. With this input voltage using THI, the voltage stress on each switch is 450 V, so 650 V is required to handle the voltage. Based on the current stress analysis shown above, the current stress of S_1, S_3, and S_5 is 20 Arms. Based on this, a minimum of a 60 A device is required. The GaN Systems device that was selected was the GS66516T. Because a GaN device was selected, the switching frequency is 100 kHz. The clamping capacitors C_1, C_3, and C_5 were calculated based on a 10% voltage ripple, so 2.469 µF is needed. The inductors L_1, L_3, and L_5 were calculated based on 200% current ripple, so the inductor value is 19.5 µH. Capacitors C_2, C_4, and C_6 were set to 4.64 µF and inductors L_2, L_4 and L_6 were set to 24 µH. This gives an output LC filter value of approximately 15 kHz. The inverter PWM signals are controlled by a Simulink program and a dSPACE DSP card with a dSPACE DS1104 breakout box to interface with the prototype board. This will be discussed more in the following sections.

3.2. Switch Isolation and Gate Drive Schematic

Each switching device has its own isolation stage and gate driver circuit. The isolation stage provides isolation between the low voltage PWM signals from the dSPACE breakout box and the high voltage output of the inverter. This isolation is for safety and it also adds noise immunity thanks to the optocoupler of the digital isolator. The isolation stage consists of a digital isolator and an isolated power supply. The digital isolator provides an isolated PWM signal for the gate driver. The isolated power supply provides isolated power so the high voltage side of the

inverter. This power supply powers the isolated side of the digital isolator and the gate driver and the 6 V gate drive linear regulator. The isolation stage and power supply schematic for one switch is shown in Figure 3.1. The gate drive circuit and GaN Systems switch is shown in Figure 3.2.

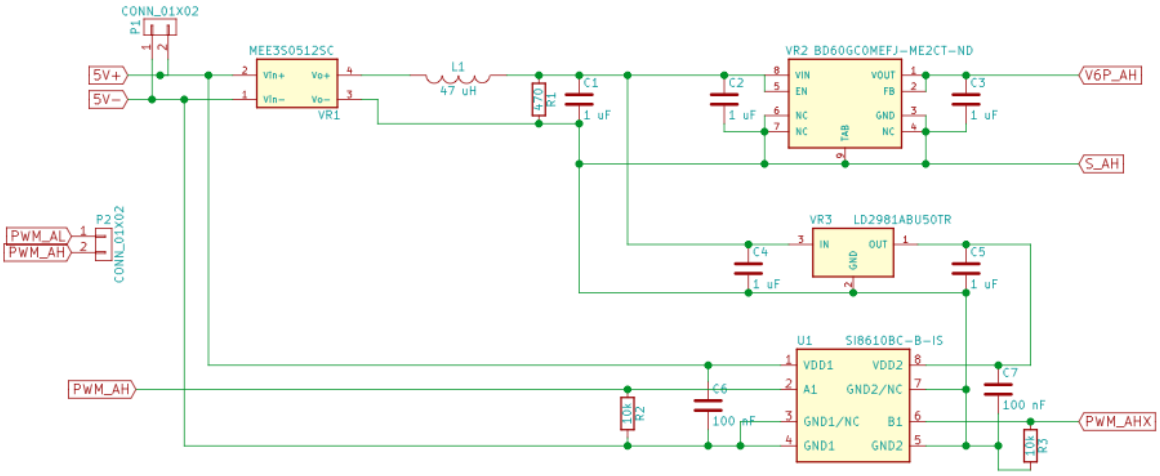

Figure 3.1. Isolation Stage and Power Supplies for One GaN Switch

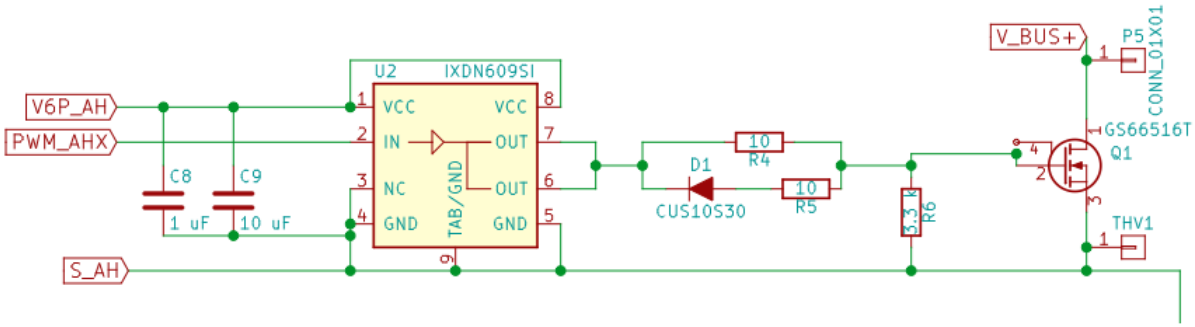

Figure 3.2. Gate Driver Cirtuit for one GaN Switch

3.3. PCB Design

The PCB design is based around a 4-layer stack-up with 2 oz. copper on each layer. The board material selected was standard FR-4. The board layout was optimized so the gate signal stray inductance loop for each switch was minimized. The main power loops were optimized to maximize the available space on the board so the highest power density could be achieved.

Figure 3.3 shows the PCB design with all 4 layers turned on. The bare PCB top side and bottom side is featured in Figure 3.4 and Figure 3.5, respectively.

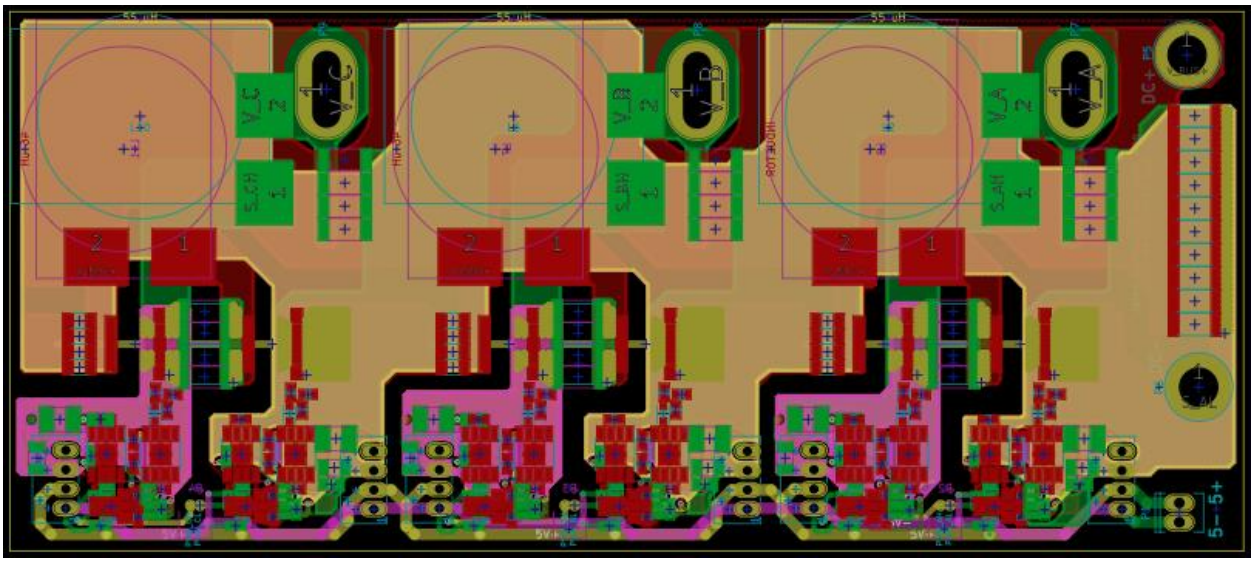

Figure 3.3. Inverter PCB Layout with All Layers Turned On

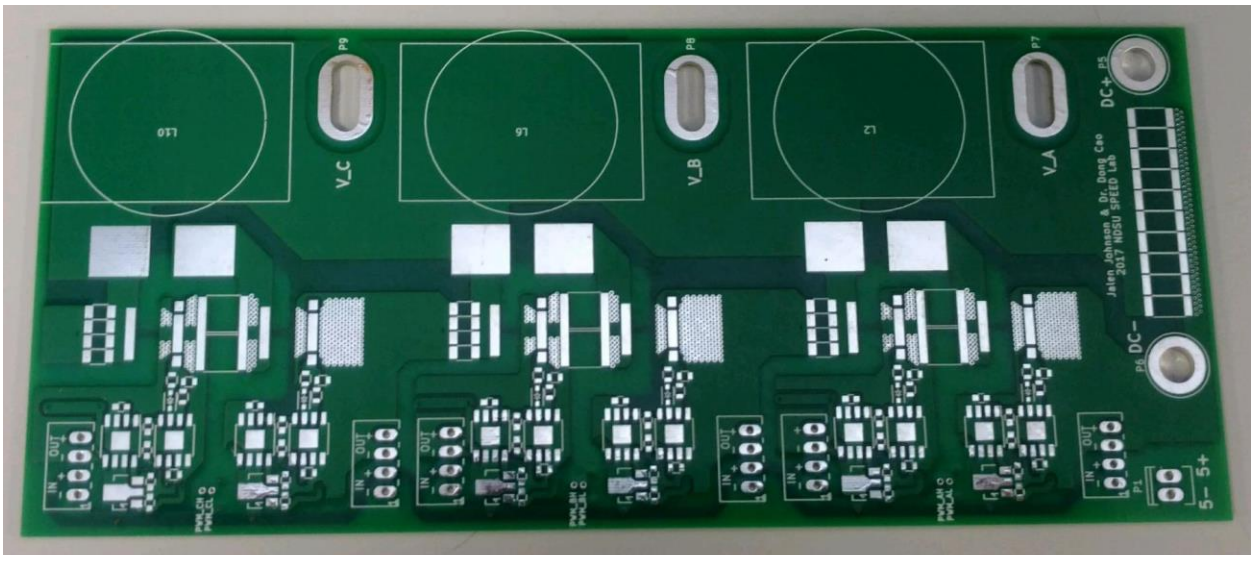

Figure 3.4. Bare PCB Top Side

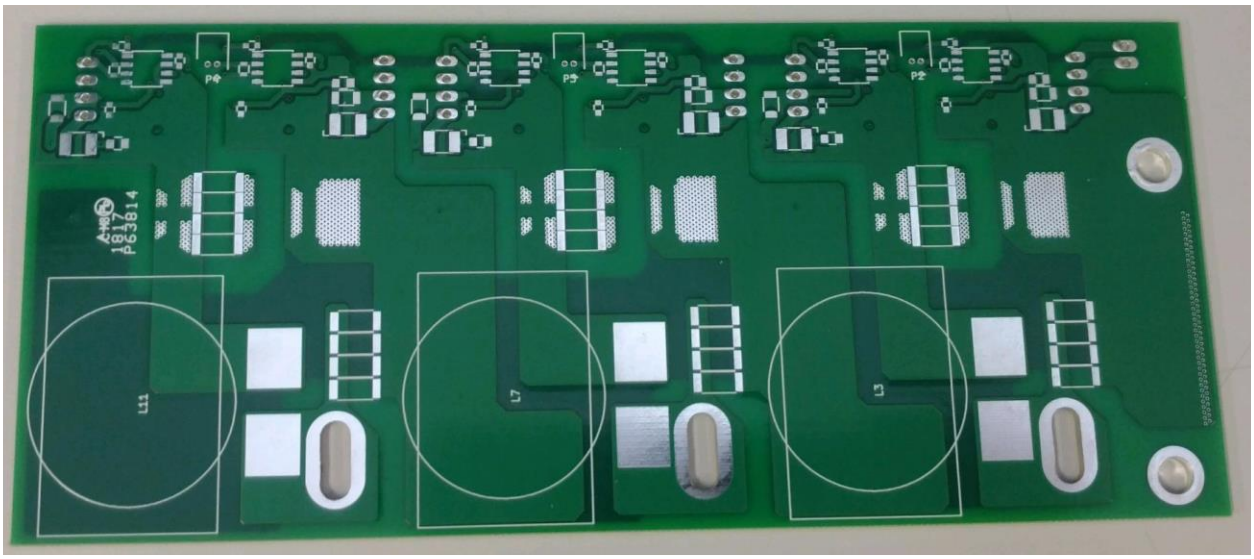

Figure 3.5. Bare PCB Bottom Side

The board was assembled by hand and verified along the way to ensure the design was working and no components were damaged or misplaced during assembly. The fully assembled board is shown in Figure 3.6.

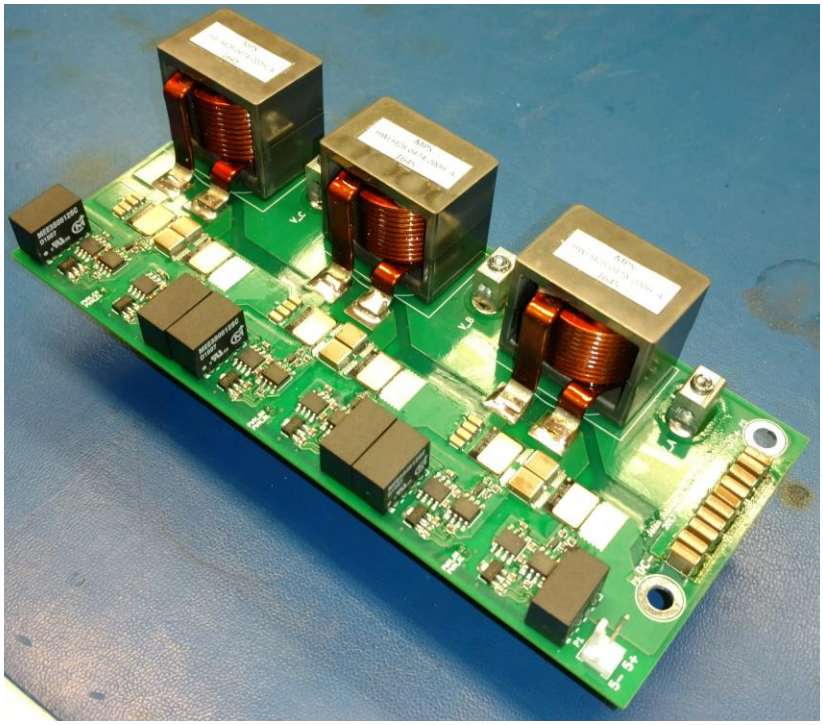

Figure 3.6. Fully Assembled Prototype

3.4. Control Setup

As mentioned above, a dSPACE DSP card and a Simulink model are the heart of the control for the three-phase semi-quasi-z-source inverter. Simulink allows for the creation of a model very quickly and is graphical so algorithms are easier to follow during development than standard text based coding. The control model for the inverter is shown in Figure 3.7.

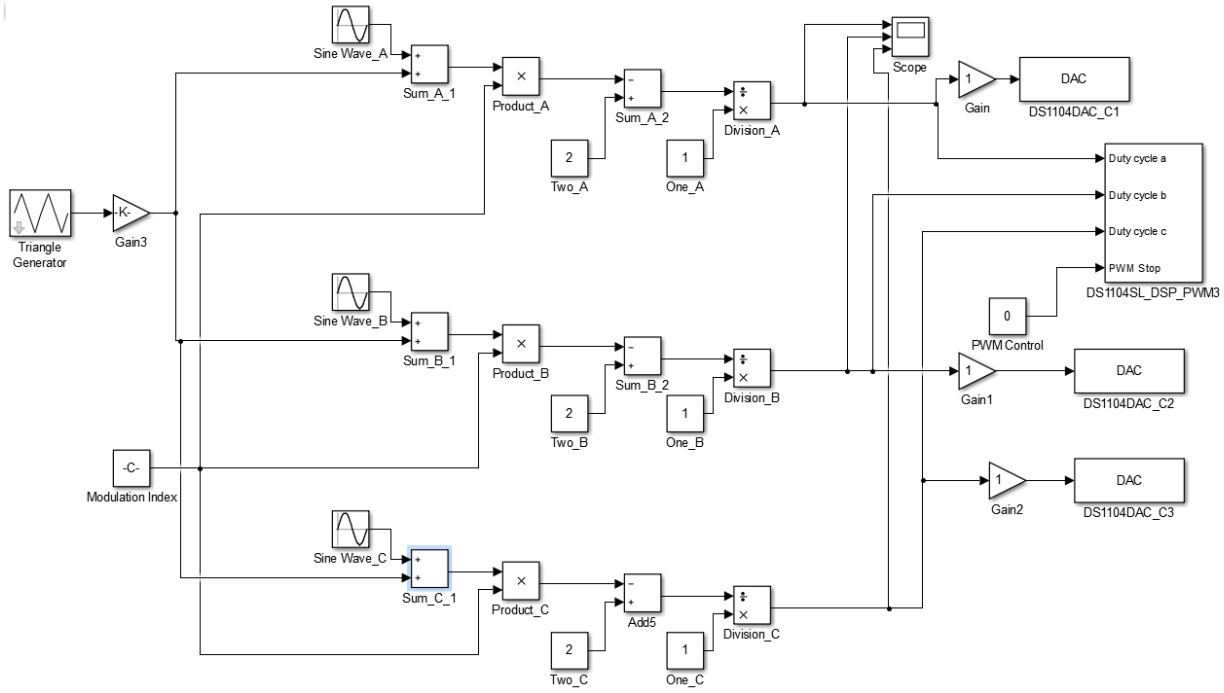

Figure 3.7. Simulink Control Model

The switching frequency was set to 100 kHz with a 60 Hz fundamental frequency output. The deadtime for the complementary switches is set to 200 ns. The nice thing about working with a Simulink model is all of the control parameters can be changed on the fly in real time so the control can be fine-tuned very quickly which aides in testing the prototype. The signals from the dSPACE DSP card are sent to a dSPACE DS1104 breakout box where a connector is attached to the breakout box and 6 shielded cables containing the 6 PWM gate signals for each switch are sent to the prototype board. The DS1104 breakout box and signal cables to the prototype is shown in Figure 3.8.

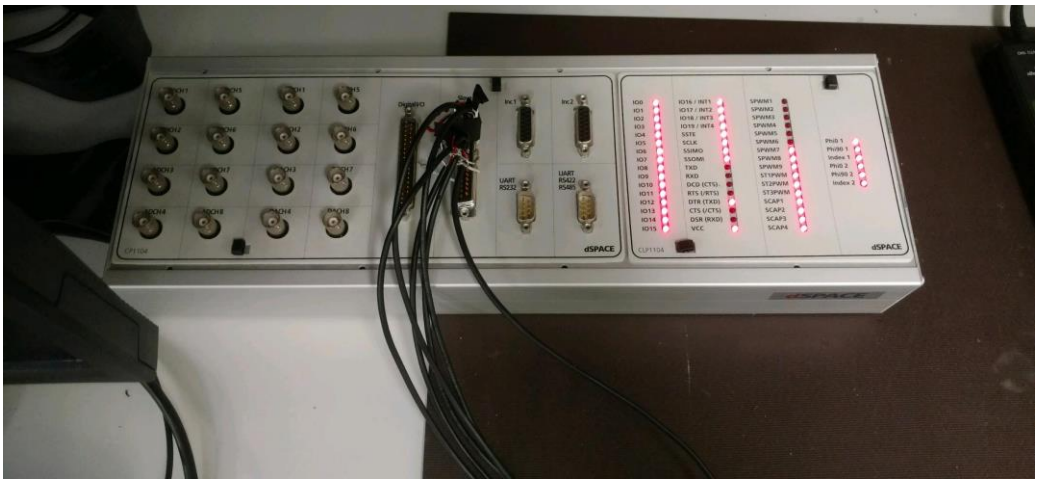

Figure 3.8. dSPACE PWM Breakout and Connections

3.5. Experimental Results

The inverter was first tested with a very light load with 70 ohms of resistance across each phase leg to verify the functionality before the power is increased. The input voltage was increased slowly from 0 V to gain confidence in the prototype before the full 130 V of rated input voltage was applied. The input voltage was increased up to around 40 V when a lot of noise was detected on the gates of the switches. This noise was causing erratic signals and shoot through which was pulling the input voltage down as the shoot through events would occur. Due

to the large amounts of shielding and careful design to condition the PWM signals getting to the board, it was determined that the signals being sent to the board were not the source of the gate signal corruption. The gate turn-on and turn-off resistances were originally 10 ohms and 1 ohm respectively. Both resistors were increased to a value of 49.9 ohms to try and mitigate the erratic noise signal that was being induced on each switch. Once this modification was performed, the erratic noise issue was mitigated with the input voltage being increased to 50 V and the signals showing no sign of corruption. Figure 3.9 shows the preliminary results of the inverter with a 50 V input and a 70 ohm load on each phase. Figure 3.10 features the output voltage of the inverter with a 86 V input and 70 ohm load on each phase. During preliminary testing, the voltage was increased to 91 V successfully, however half of the oscilloscope capture image got corrupted while the flash drive was ejected from the oscilloscope. Due to this, the measurement numbers were cut off from the bottom of the image, but the waveform was still saved. The output voltage with a 91 V input is shown in Figure 3.11

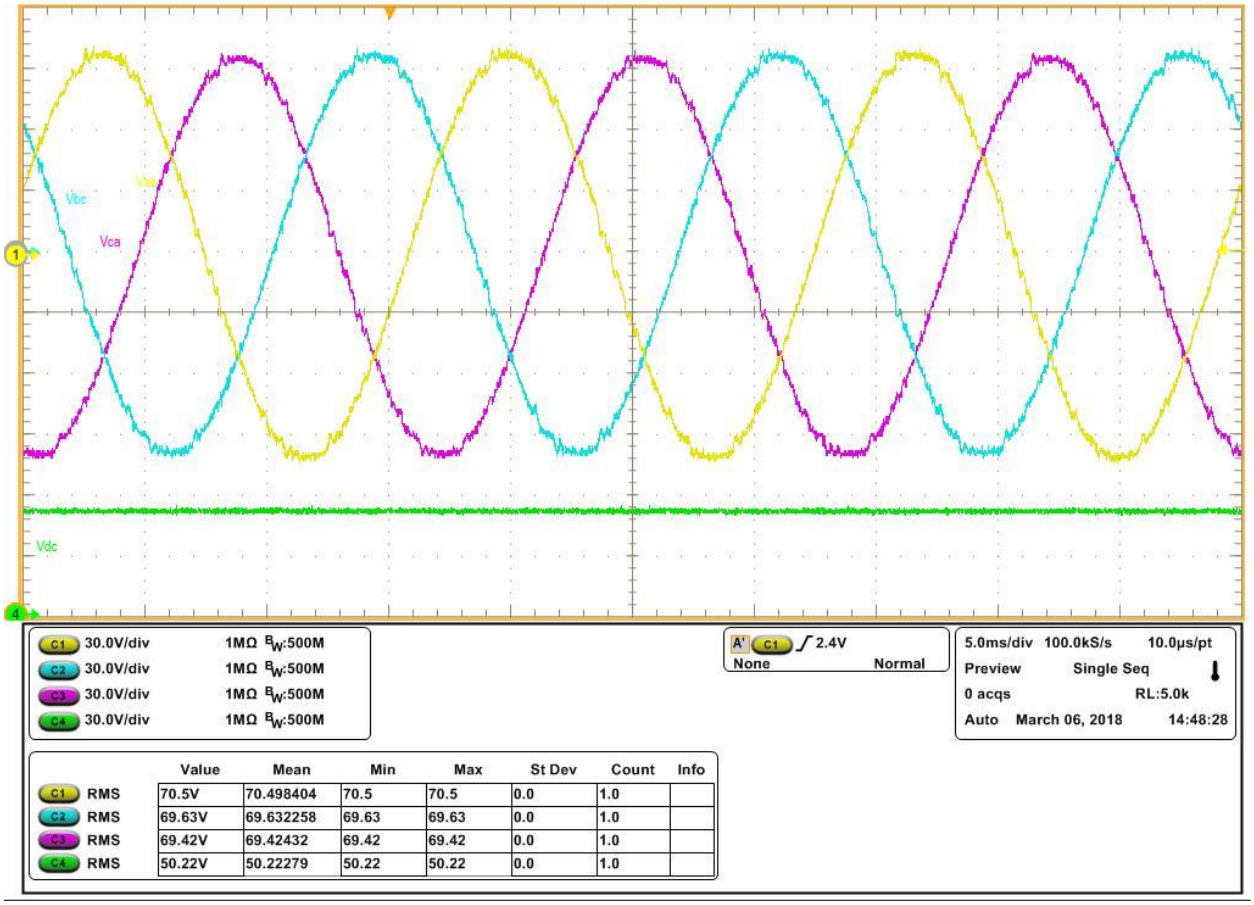

Figure 3.9. Three-Phase Semi-Quasi-Z-Source Output Voltage with 50 V Input

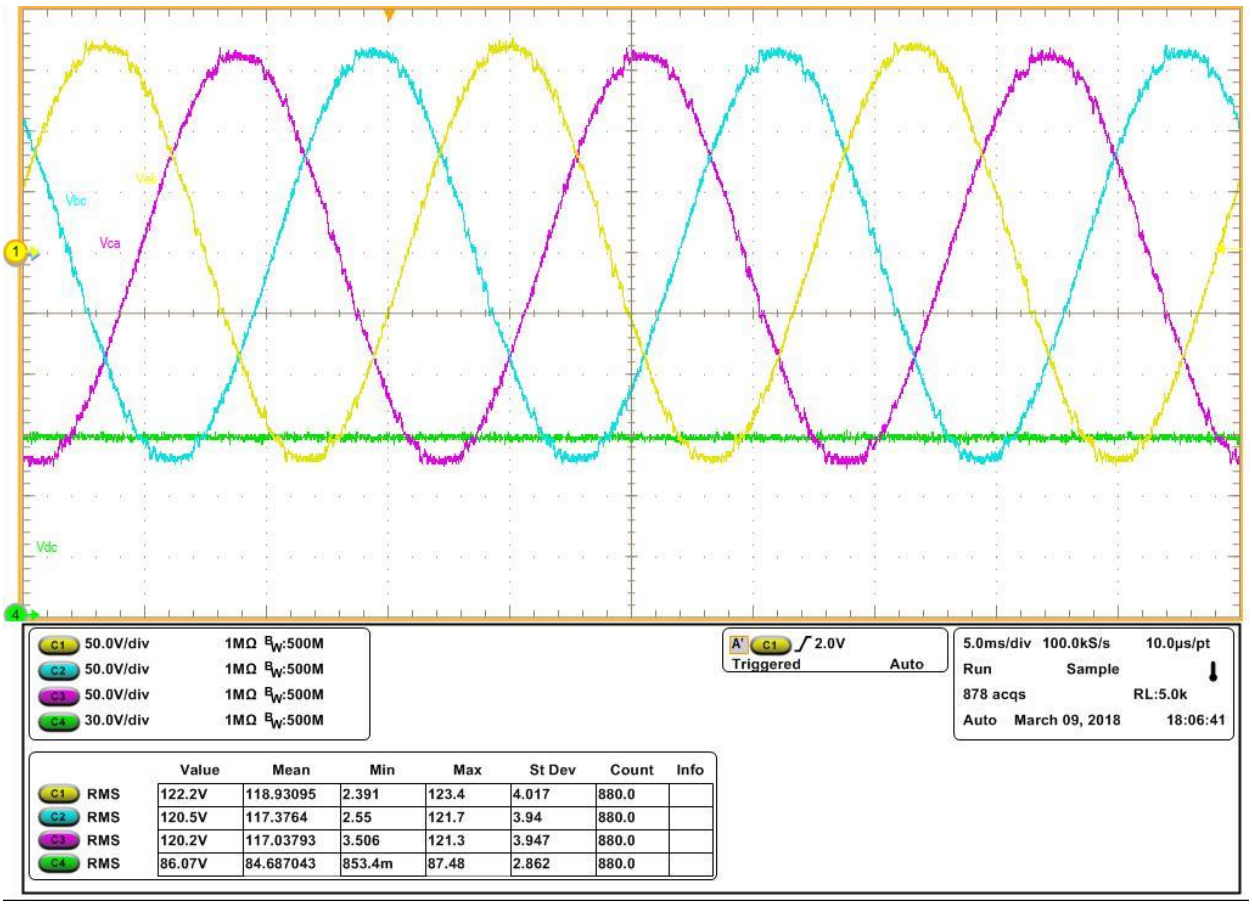

Figure 3.10. Three-Phase Semi-Quasi-Z-Source Output Voltage with 86 V Input

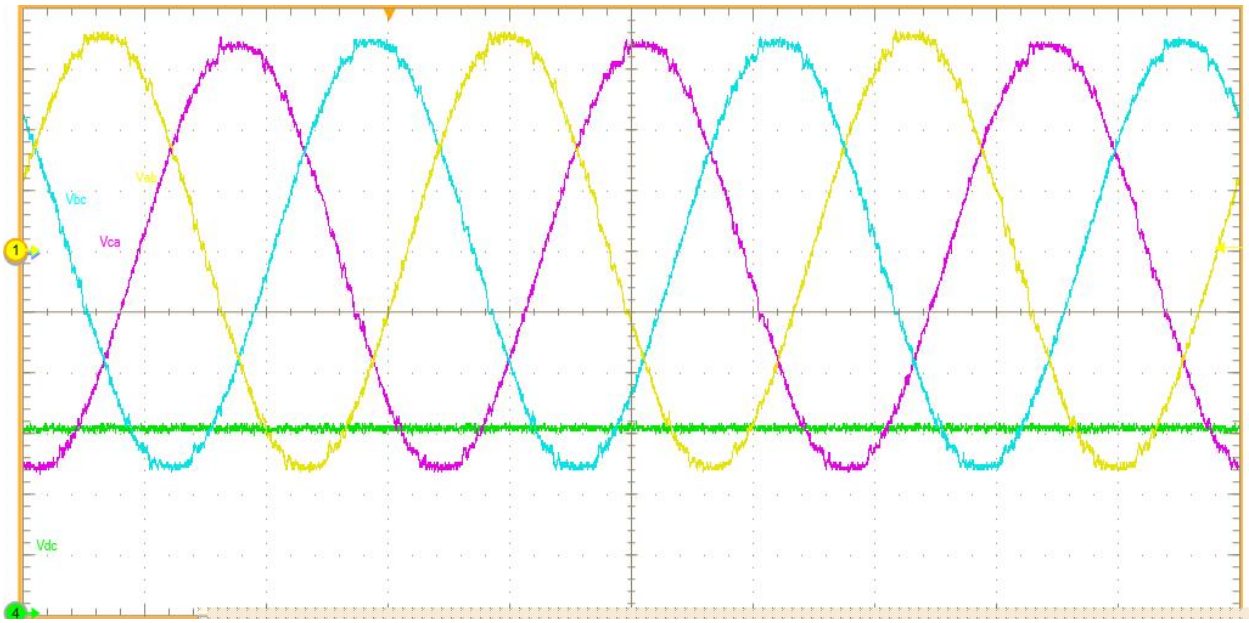

Figure 3.11. Three-Phase Semi-Quasi-Z-Source Output Voltage with 91 V Input

Due to the tight constraints of the PCB layout, custom heatsinks were created for each pair of switches to sink heat from the top side cooling pad of each switch. The one of the custom heatsinks is shown in Figure 3.12.

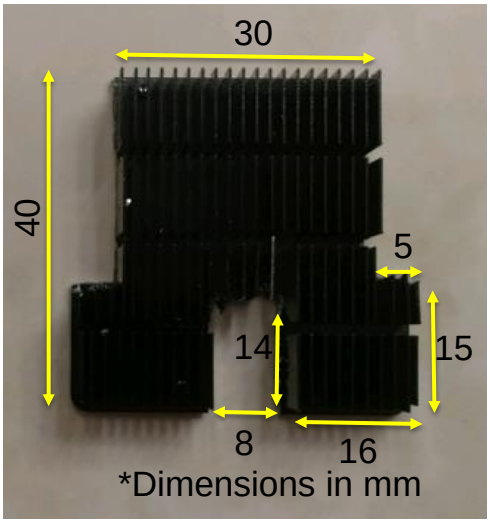

Figure 3.12. Heatsink Design

The thermal analysis of the heatsink design was calculated based on the original gate resistor values. Because the gate resistor values were increased to eliminate the erratic gate signal oscillations, the switching losses of each switch were increased. Due to the increased losses, the designed output power will need to be derated based on the junction temperature of the switching devices. Further thermal analysis and heatsink design will need to be investigated to dissipate the additional losses of each switch at full rated power.

4. RMMC WITH PPVR ANALYSIS AND OPERATION

4.1. RMMC with PPVR

As mentioned in Chapter 1, an unregulated resonant converter is a very efficient way to transfer power. Many unregulated regulated converter topologies have been developed that have very high efficiencies and high conversion ratios. These highly efficient, unregulated topologies are also known as DC transformers or DCX as mentioned in Chapter 1. The downfall of these converters is that they are unregulated. This means that the output voltage is directly proportional to the input voltage so as the input voltage drifts up and down, the output drifts as well. The solution is to use a regulated converter, however many of the standard regulated converter topologies are less efficient than the unregulated topologies and they offer very high device stresses. The solution to this problem is to use the idea of partial power voltage regulation (PPVR). The main idea of PPVR is to use a highly efficient and low device stress unregulated topology to convert a bulk of the power in a system and then a lower efficiency and higher device stress regulated topology is used to provide the voltage regulation but only process a small amount of power. This split in power offers the benefits of voltage regulation with the benefit of very high system efficiency thanks to the unregulated converter doing a bulk of the work. The PPVR power breakdown idea is shown in Figure 4.1. This figure shows that using a regulated converter to process just a small amount of the system power still results in a very high system efficiency but with the added benefit of voltage regulation.

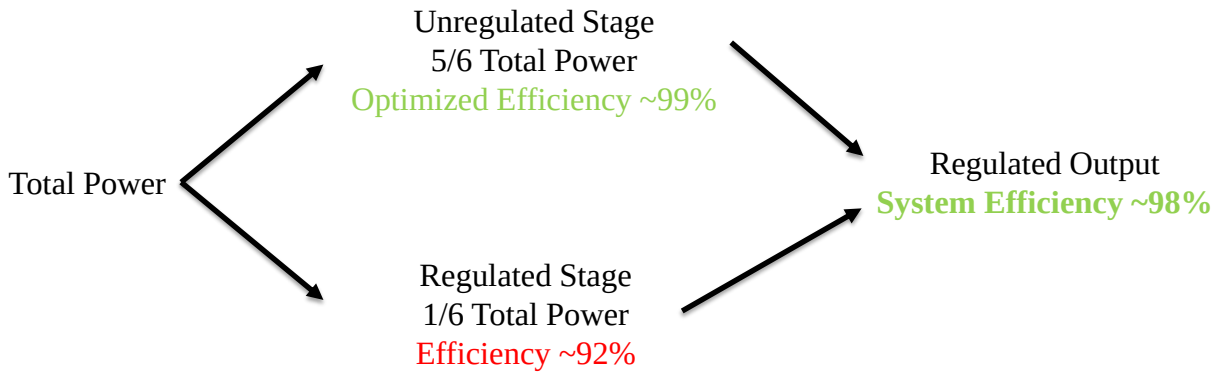

Figure 4.1. PPVR Power Breakdown

This voltage regulation is key for an automotive application where the input battery voltage fluctuates greatly as the battery is discharged. With the voltage regulation, the output voltage of the converter is always stable and at the desired value so the inverter can run at peak efficiency and the electric vehicle can deliver maximum power to the road when it is desired. If just an unregulated topology was used, the inverter input voltage would be constantly fluctuating and the vehicle power could be derated as the battery voltage drops due to current limitations of the system.

4.2. Operation of RMMC Topology

A very efficient resonant modular converter was selected for the unregulated portion of the system. The topology is based off of the work presented in [19],[20]. The converter features a very modular topology so scaling for various conversion rations is very easy. Due to the resonant operation, the converter also offers ZCS which reduces the switching losses to almost zero with aides in device stress and overall efficiency. The converter topology has two switching states. Each pair of switches operates at a fixed 50% duty cycle, so the pairs of switches are switched in a complementary fashion and all evenly share the voltage and current stress because each switch operates for half of the switching period. The topology for the selected RMMC topology is

shown in Figure 2.1. This figure features a topology with a conversion ratio of 2 for ease of analysis. However, this topology can be scaled for N-times conversion ratio.

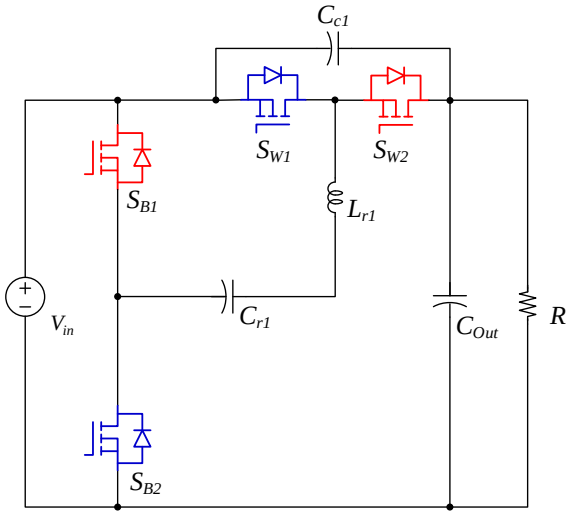

Figure 4.2. 2X RMMC Topology

The first switching state for this topology is shown in Figure 4.3. In this state switches S_{B2} and S_{W1} are conducting. In this state C_{r1} charges through L_{r1} and charges up to V_{in}.

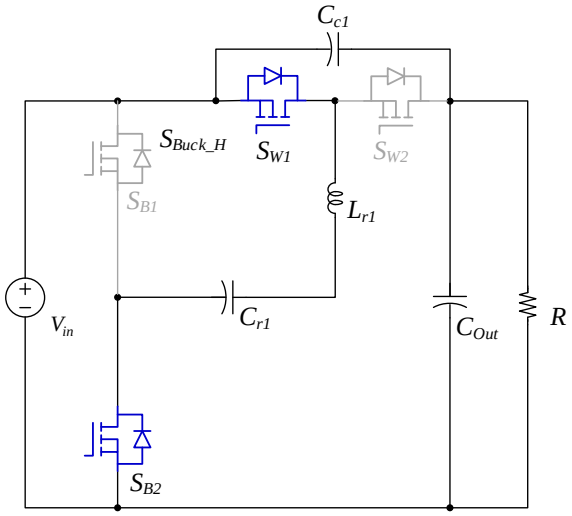

Figure 4.3. RMMC Switching State I

The second switching state is shown in Figure 4.4. In this state switches S_{B1} and S_{W2} are conducting. During this state C_{r1} charges C_{c1} up to V_{in} because C_{r1} is charged up to V_{in}. C_{out} is charged up to the potential of C_{r1} plus V_{in}. Since C_{r1} is charged to V_{in}, then C_{out} is charged to 2 times V_{in}.

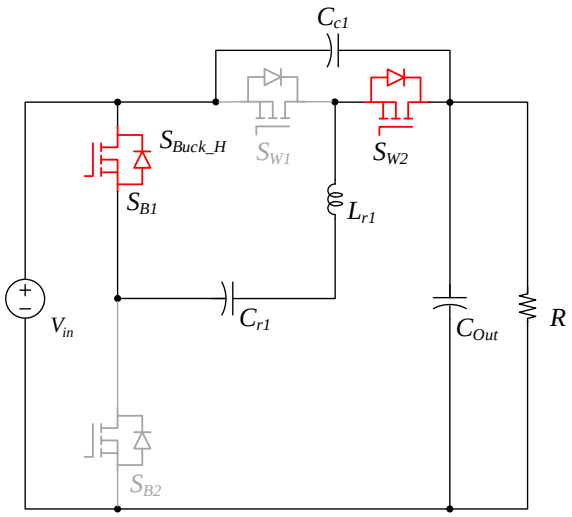

Figure 4.4. RMMC Switching State II

During both switching states C_{c1} clamps the voltage across S_{W1} and S_{W2} so there is negligible voltage spike when the switches turn off. The addition of the inductor gives a sinusoidal current in the series L_{r1} and C_{r1} path. The resonant frequency of this LC chain is shown in Eq. 4.1. If the switching frequency of the switching devices is set to this resonant frequency, then when the current in the LC branch crosses zero, ZCS can be achieved.

$$f_r = \frac{1}{2\pi\sqrt{LC}} \qquad \text{(Eq. 4.1)}$$

As more modules are added on, the conversion ratio goes up by the number of modules added. This shows how the topology is highly modular. Figure 4.5 shows a 6X conversion ratio topology that will be used for analysis in the following sections. Even though the topology is for a conversion ratio of 6, the conversion ratio can be lowered by putting modules in a pass-through state. In this state the $S_{w\#}$ switches will be turned on all the time and the $S_{B\#}$ switches will be turned off all the time so the module is active.

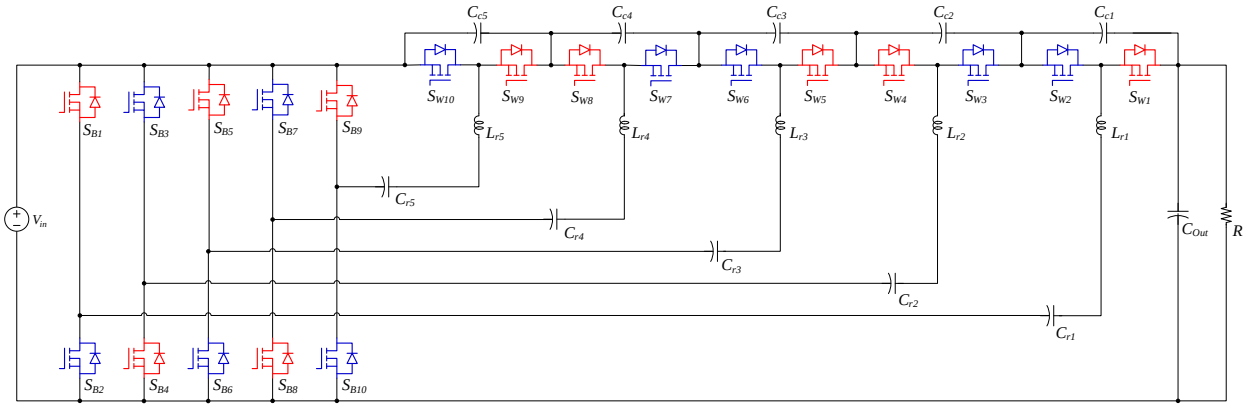

Figure 4.5. 6X RMMC Topology

4.3. Operation of RMMC with PPVR

The topology mentioned in the previous section is a great choice for a modular RMMC topology and since this topology is unregulated, it is a great choice to apply PPVR. This is achieved by inserting a regulated converter topology within the existing topology. As mentioned in the previous section, the voltage across each module is equal to the input voltage of the converter. By controlling the number of resonant full-bridge modules are active in the RMMC, the DCX stage can achieve the discrete conversion ratios of 4, 5, and 6. The inactive modules are put into a bypass mode where the wing side switches are in a fully on state and the input side switches are in a fully off state.

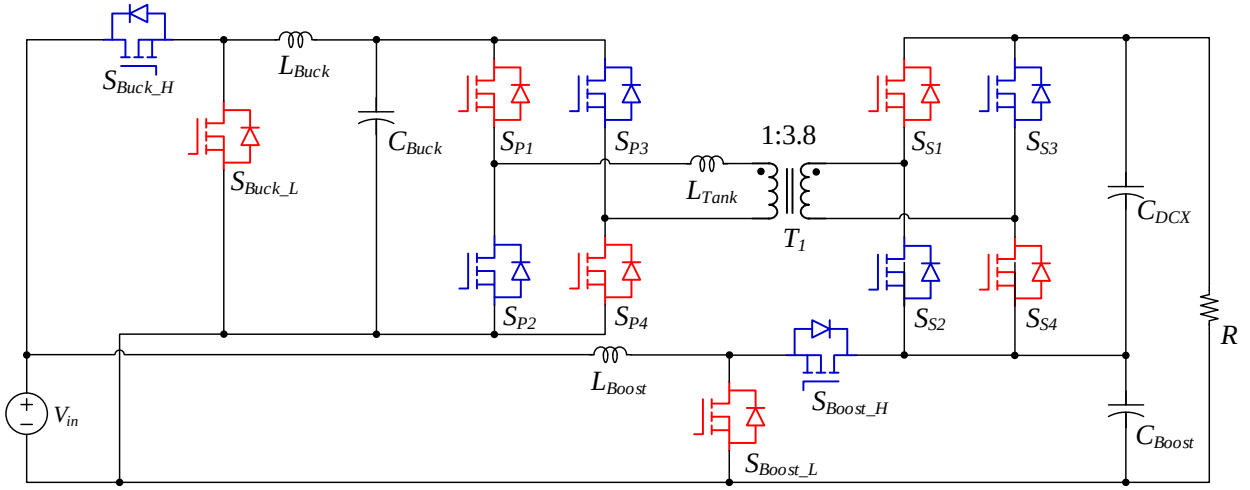

Figure 4.6. Composite Converter Topology

With the addition of the regulation stage, the converter can operate at any conversion ratio between 4 and 6. As mentioned in the introduction, the proposed topology is transformer-less, so the system is fully modular and is more flexible for different battery voltage ranges and output voltage requirements. Whereas the topologies in [9]-[11] rely on a fixed transformer turns ratio, which limits the applications of the converter without having to redesign the transformer and the switch selection. The composite converter topology featured in [11], [12] is shown in Figure 4.6. The voltage regulation can be achieved by changing the voltage on the node where the bottom side switches and the wing side switches meet. The output voltage then becomes the number of modules minus one times the input voltage plus the voltage at the regulation node. This is shown in equation 4.2. The location of where the PPVR circuit is added is shown in Figure 4.7.

$$V_{Out}=(\#\ \text{of Modules-1})V_{In}+V_{Regulation} \qquad \text{(Eq. 4.2)}$$

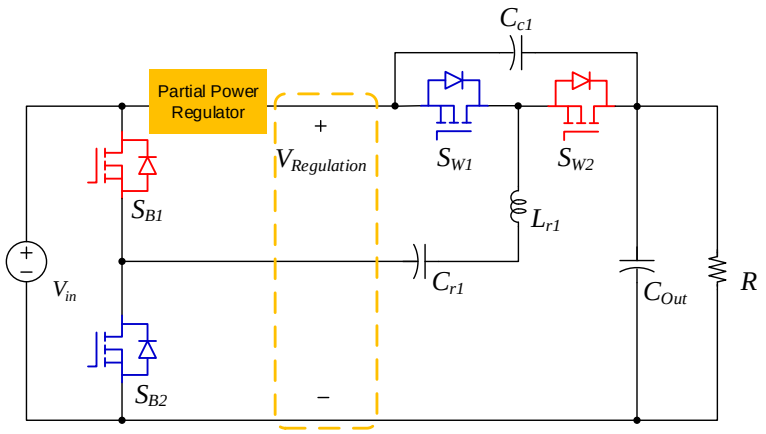

Figure 4.7. PPVR Location

The optimized regulated topology is up for debate depending on the application of the overall converter and the conversion ratio range required. The buck converter topology for the PPVR circuit will be analyzed further in the following sections. A 6X RMMC converter with a buck converter PPVR stage is shown in Figure 4.8. However, many topologies can be used. For example, a non-inverting buck-boost PPVR converter is shown with a 6X RMMC topology in Figure 4.9. This topology may be useful if the conversion ratio range is very small but can drift slightly above or below what the unregulated converter can deliver. The non-inverting buck-boost regulation stage can mitigate duty cycle limitations of the buck converter regulation stage when duty cycle is nearing 0% or 100% [14].

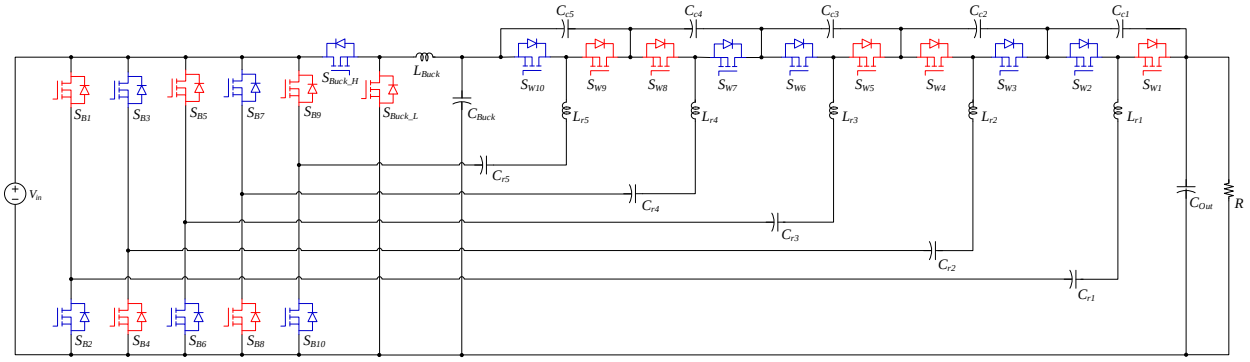

Figure 4.8. 6X RMMC with Buck Converter PPVR

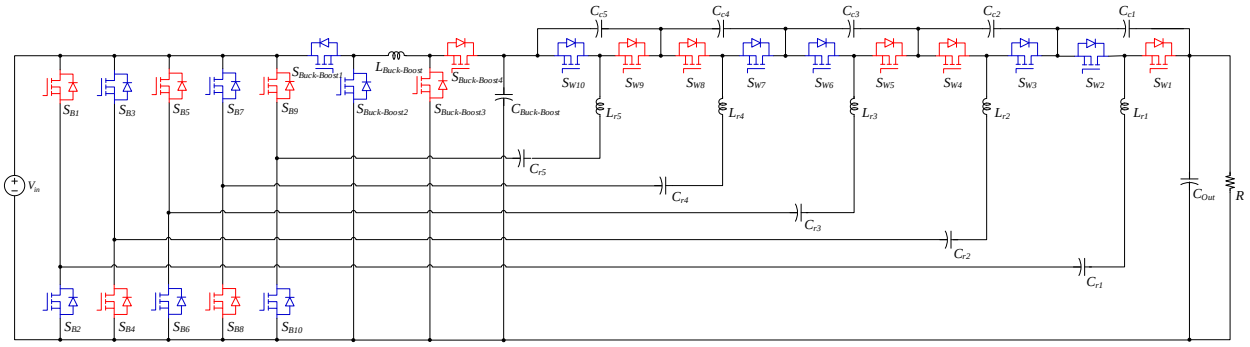

Figure 4.9. 6X RMMC with Non-Inverting Buck-Boost Converter PPVR

4.4. RMMC with PPVR Device Stress Analysis

With the demand for more efficient converter topologies, switching device selection has also been a driver to topology efficiency and a driving factor for topology selection. This analysis will focus on using a GaN based switching device for comparison between the traditional boost converter, the composite converter architecture in [11], [12] and the proposed converter topology. For an equal comparison, the $R_{ds(on)}$ for an ideal GaN device will be used. The device resistance is based on the blocking voltage of the device. By interpolating the data in [15]-[18] a curve and a function have been derived for an ideal GaN device. The ideal $R_{ds(on)}$ curve can be seen in Figure 4.10 and it is mathematically shown in (Eq. 4.3). Three device voltage ratings and the corresponding $R_{ds(on)}$ is shown in Table 4.1. The $R_{ds(on)}$ has been nominalized with the die area which accounts for the current ratings for the switching devices.

Many comparisons were made between the three different topologies. The conduction power stress and the voltage and current stress ratios were all analyzed among the three different converters. All comparisons were made using the nominal 250 V input voltage, 1200 V output, and a 4 kW load. To make a fair comparison, it was assumed that the transformer turns ratio for the composite converter in [11], [12] could be changed from 1:1.9 to 1:3.8 to achieve the 1200 V output voltage requirement. The conduction power stress can be found using (Eq. 4.4) and (Eq. 4.5) and the comparison table is shown in Table 4.2. The device stress ratio can be found using (Eq. 4.4), (Eq. 4.6), and (Eq. 4.7) and the comparison table is shown in Table 4.3.

$$R_{DS(on)} = 0.0000003(BV_{DS}{}^{1.99}) \quad \text{(Eq. 4.3)}$$

$$\text{Switch Current Stress} = I_{RMS} \quad \text{(Eq. 4.4)}$$

$$\text{Conduction Power Stress} = \sum \left(\frac{I_{RMS}}{I_{Out}}\right)^2 R_{DS(On)} \quad \text{(Eq. 4.5)}$$

$$\text{Switch Voltage Stress} = V_S \quad \text{(Eq. 4.6)}$$

$$\text{Device Stress Ratio} = \sum \left(\frac{I_{RMS}}{I_{Out}}\right)\left(\frac{V_S}{V_{Out}}\right) \quad \text{(Eq. 4.7)}$$

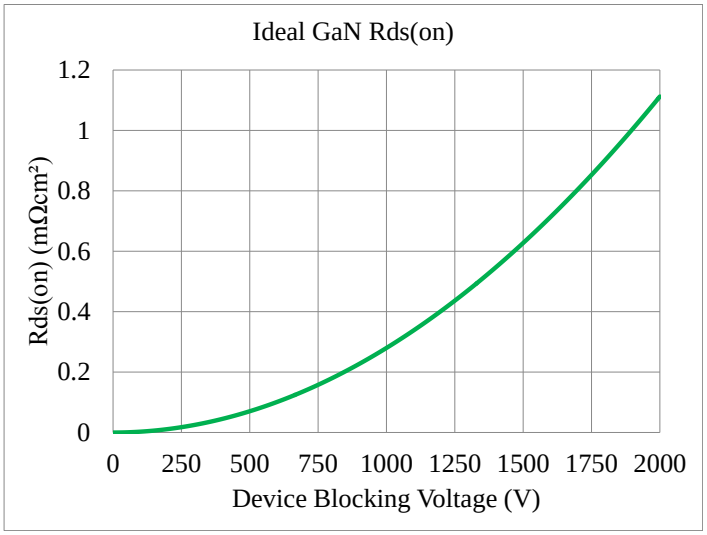

Figure 4.10. Ideal GaN $R_{ds(on)}$ versus Device Blocking Voltage Curve

Table 4.1. $R_{ds(on)}$ for Device Voltage Ratings

Device Blocking Voltage (V)	$R_{ds(on)}$ (Ωcm²)
650	0.12
1200	0.40
1700	0.80

Table 4.2. Converter Conduction Power Stress Comparison

Converter Conduction Power Stress Comparison: 250 V Input, 1200 V Output, 4 kW								
Converter Parameters	Converter Switch	Switch RMS Current (Arms)	Switch Voltage Rating (V)	Switch Rdson ($m\Omega cm^2$)	Number of Switches	Conduction Power Stress	Total Switch Conduction Power Stress	Total Partial Power Processing Conduction Stress
Boost D=0.792	Conventional Boost High	7.31	1700	0.80	1	3.85	18.43	N/A
	Conventional Boost Low	14.23	1700	0.80	1	14.58		
Buck D=0.844 Boost D=0.375 Turns Ratio=1:3.8	Composite Buck High	11.61	650	0.12	1	1.46	10.57	2.03
	Composite Buck Low	5.00	650	0.12	1	0.27		
	Composite Boost High	4.22	650	0.12	1	0.19		
	Compositie Boost Low	3.27	650	0.12	1	0.12		
	Composite DCX Primary	12.67	650	0.12	4	6.93		
	Composite DCX Secondary	3.33	1200	0.40	4	1.60		
Buck D=0.8	Proposed DCX (Active)	5.24	650	0.12	16	4.74	5.10	0.12
	Proposed DCX (Bypass: On)	3.33	650	0.12	2	0.24		
	Proposed DCX (Bypass: Off)	0.00	650	0.12	2	0.00		
	Proposed Buck High	2.98	650	0.12	1	0.10		
	Proposed Buck Low	1.49	650	0.12	1	0.02		

Table 4.3. Device Stress Ratio Comparison

Device Stress Ratio Comparison: 250 V Input, 1200 V Output, 4 kW									
Converter Parameters	Converter Switch	Switch RMS Current (Arms)	Switch Voltage Stress (V)	Current Stress Ratio (Irms/Iout)	Voltage Stress Ratio (Vs/Vout)	Number of Switches	Device Stress Ratio	Total Device Stress Ratio	Total Partial Power Processing Stress Ratio
Boost D=0.792	Conventional Boost High	7.31	1200	2.19	1.00	1	2.19	6.46	N/A
	Conventional Boost Low	14.23	1200	4.27	1.00	1	4.27		
Buck D=0.844 Boost D=0.375 Turns Ratio=1:3.8	Composite Buck High	11.61	250	3.48	0.21	1	0.73	7.12	1.79
	Composite Buck Low	5.00	250	1.50	0.21	1	0.31		
	Composite Boost High	4.22	400	1.27	0.33	1	0.42		
	Compositie Boost Low	3.27	400	0.98	0.33	1	0.33		
	Composite DCX Primary	12.67	211	3.80	0.18	4	2.67		
	Composite DCX Secondary	3.33	800	1.00	0.67	4	2.66		
Buck D=0.8	Proposed DCX (Active)	5.24	250	1.57	0.21	16	5.24	5.52	0.28
	Proposed DCX (Bypass: On)	3.33	0	1.00	0.00	2	0.00		
	Proposed DCX (Bypass: Off)	0.00	250	0.00	0.21	2	0.00		
	Proposed Buck High	2.98	250	0.89	0.21	1	0.19		
	Proposed Buck Low	1.49	250	0.45	0.21	1	0.09		

The total conduction power stress and device stress are calculated using all of the switching devices in each topology. Also, the partial power processing stress is calculated using just the switches used for voltage regulation. It can be seen that the proposed converter topology has a much lower conduction power stress than the traditional boost converter and half the conduction power stress than the composite converter architecture. The total device stress ratio is also much lower on the proposed topology than the other two topologies. The partial power processed by the proposed converter is also much less than the composite converter architecture. The conduction power stress of the proposed partial power circuit is almost 17 times lower than the composite converter partial power processing devices. The disadvantage that the composite converter architecture has in the device stress ratio is that it requires the use of a 1200 V device on the secondary side of the DCX stage, whereas the proposed topology can utilize 650 V devices for all switches.

4.5. RMMC with PPVR Simulation Results

A simulation was performed for a 4 kW converter with an output voltage of 1200 V. The input voltage was set to a nominal 250 V battery voltage to stay consistent with the analysis performed in the above sections. The resonant inductor and capacitor values are 1.5 µH and 132 nF, respectively. From (Eq.4.1) the switching frequency of the RMMC switches was set to 357.674 kHz. A buck converter was selected as the PPVR circuit for the simulations. The buck inductor was set to 38 µH and the buck output capacitor was set to 4 µF. The switching frequency of the buck converter was set to the same frequency as the resonant frequency and had a duty cycle of 0.8. The output capacitor for the converter was set to 2 µF. The clamping capacitors for the wing side resonant switches were 3 µF each. The output voltage of the converter is shown in Figure 4.11. The RMMC DCX switch current is shown in Figure 4.12. The

DCX resonant LC current is shown in Figure 4.13. The converter input voltage and the output of the PPVR buck converter is shown in Figure 4.14. Finally, the PPVR buck converter switch current is featured in Figure 4.15.

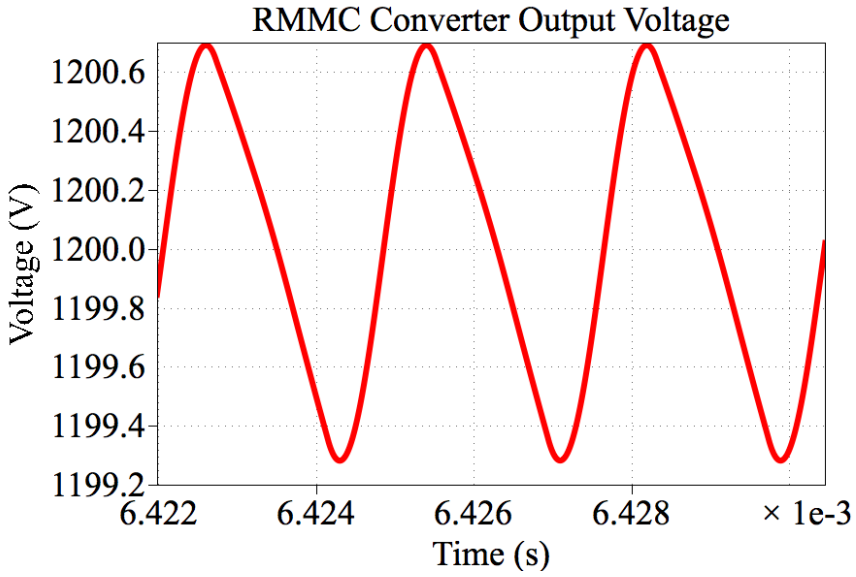

Figure 4.11. Converter Output Voltage

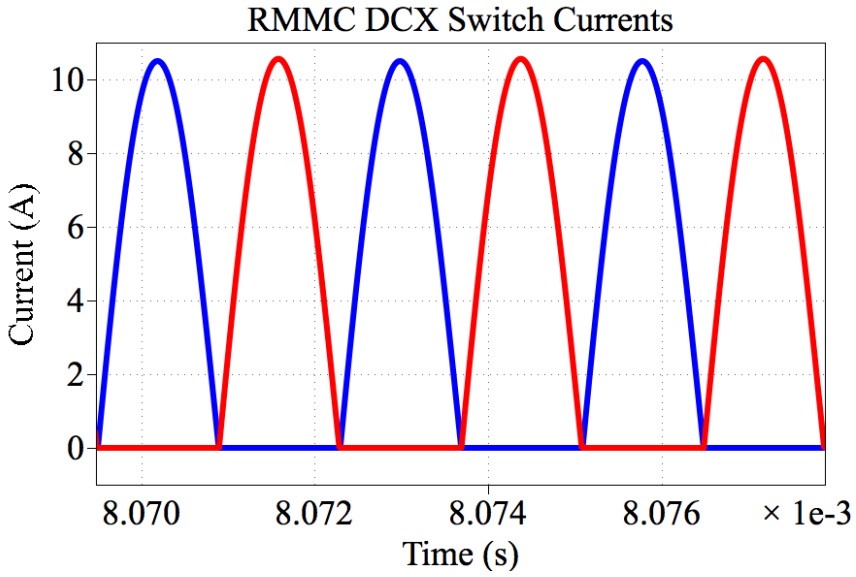

Figure 4.12. Converter DCX Switch Current

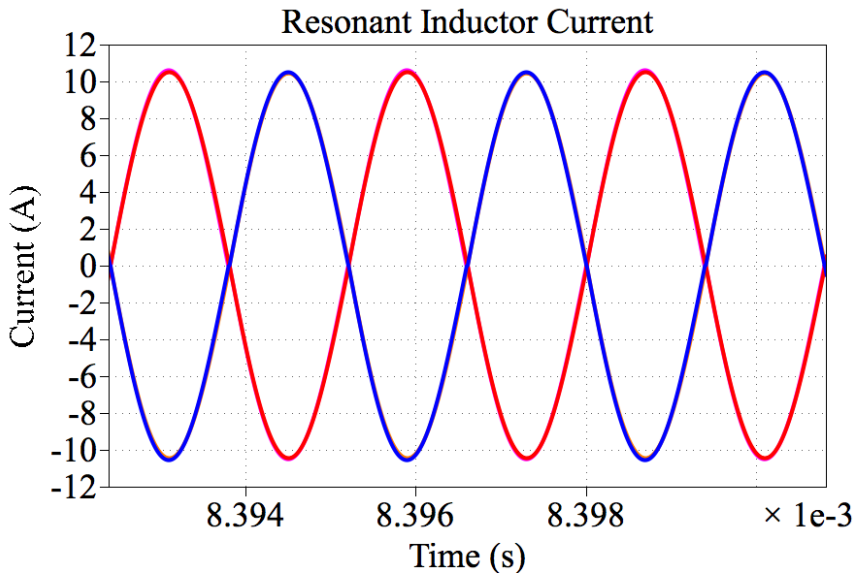

Figure 4.13. Converter Resonant LC Current

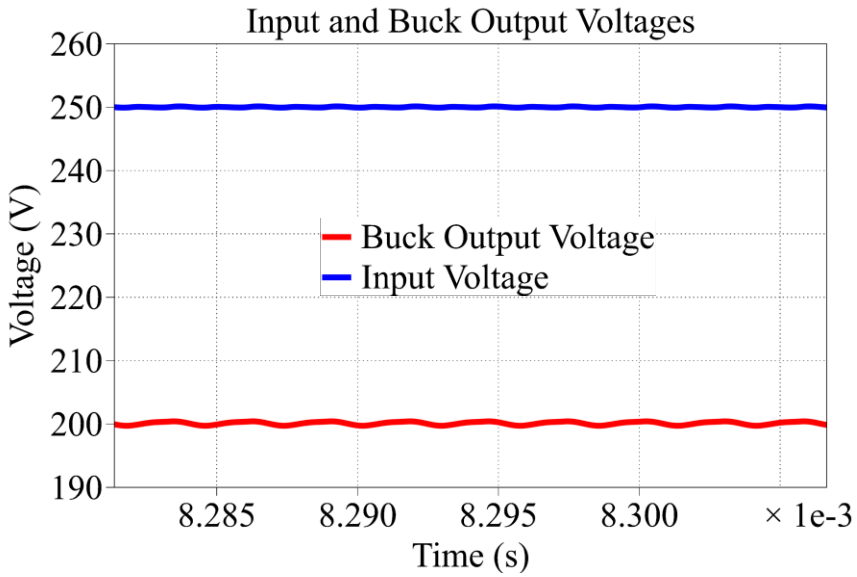

Figure 4.14. Input and PPVR Buck Output Voltage

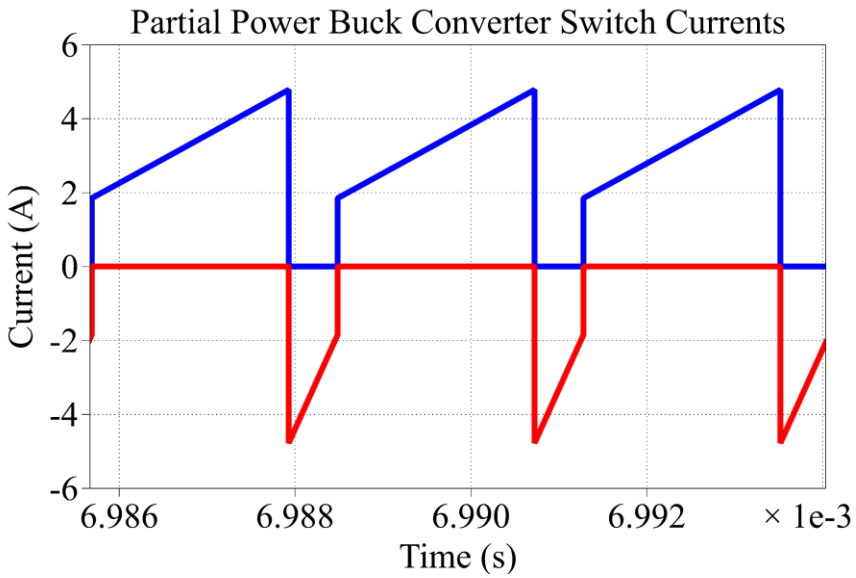

Figure 4.15. PPVR Buck Switch Current

5. RMMC WITH PPVR PROTOTYPE DESIGN

5.1. 4kW RMMC with PPVR Buck Converter Design

A 4 kW prototype was developed based on the topology featured on Figure 4.7. A 6 times conversion ratio RMMC converter with a buck converter PPVR circuit interleaved. The output voltage of the converter is rated at 1200 V. The input voltage was designed to range from 200 V to 300 V with a nominal battery voltage of 250 V. The RMMC converter and the PPVR buck converter were designed as two separate boards to different PPRV circuits can be interleaved and tested with the resonant converter in future testing. The GaN Systems GS66508B device was selected for the switching device for all resonant switches and the buck converter switches. The resonant inductor value was set to 1.5 µH so the Coilcraft XAL1060-152MEB inductor was selected. The resonant capacitor value was set to 132 nF. To get an equivalent 132 nF, four TDK CGA9Q1C0G3A333J280KC parts were selected and assembled in parallel to obtain the desired capacitance value. These capacitors are a C0G material, so there no chance in capacitance with voltage bias. This feature is critical for the resonant capacitor, so the LC string doesn't change resonant frequency with voltage. The resonant clamping capacitance value was set to 3.84 µF. The TDK C5750X6S2W225K250KA was selected and six parts are placed in parallel to obtain the desired capacitance value at nominal input voltage. The output capacitor for the buck converter was set to 4 µF. Six TDK C5750X6S2W225K250KA parts were placed in parallel to obtain the desired capacitance at the nominal input voltage case. The buck converter inductor was set to 38 µH. Two Coilcraft XAL6060-223MEB parts are connected in series to obtain the desired inductance. The output capacitor value is set to 2 µF so thirty-eight TDK B58031U9254M062 Ceralink capacitors were placed in parallel to achieve the desired capacitance at full 1200 V output voltage.

5.2. RMMC and Gate Drive Schematic

Similarly to the semi-quasi-z-source inverter gate drive circuity, each switching device for the resonant converter circuit has its own isolation stage and gate driver circuit. An isolated gate drive IC was selected to eliminate the need for a digital isolator and a gate driver IC. This reduces the number of parts needed and simplifies the circuit. The Silicon Labs SI8271GB-IS isolated gate driver IC was selected for the design. The 9 V isolated power supply voltage was biased using a 6.2 V Zener diode. This gives a positive 6.2 V and negative 2.8 V gate signal. Having a negative bias gate voltage when the switch is off makes for a more robust driver circuit and helps mitigate any noise turning the device on when it is not signaled to be on. Figure 5.1 shows the gate drive circuitry for one GS66508B device. Figure 5.2 shows the schematic for one of the five resonant modules on the board. The same topology was duplicated to build up to a 6 times conversion ratio resonant DCX converter.

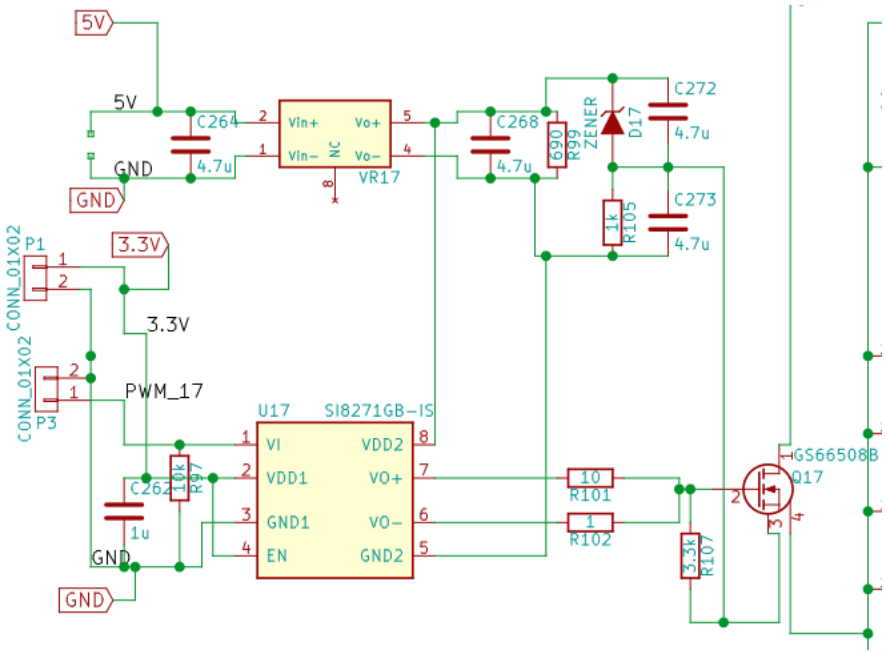

Figure 5.1. RMMC Gate Drive Circuit Schematic

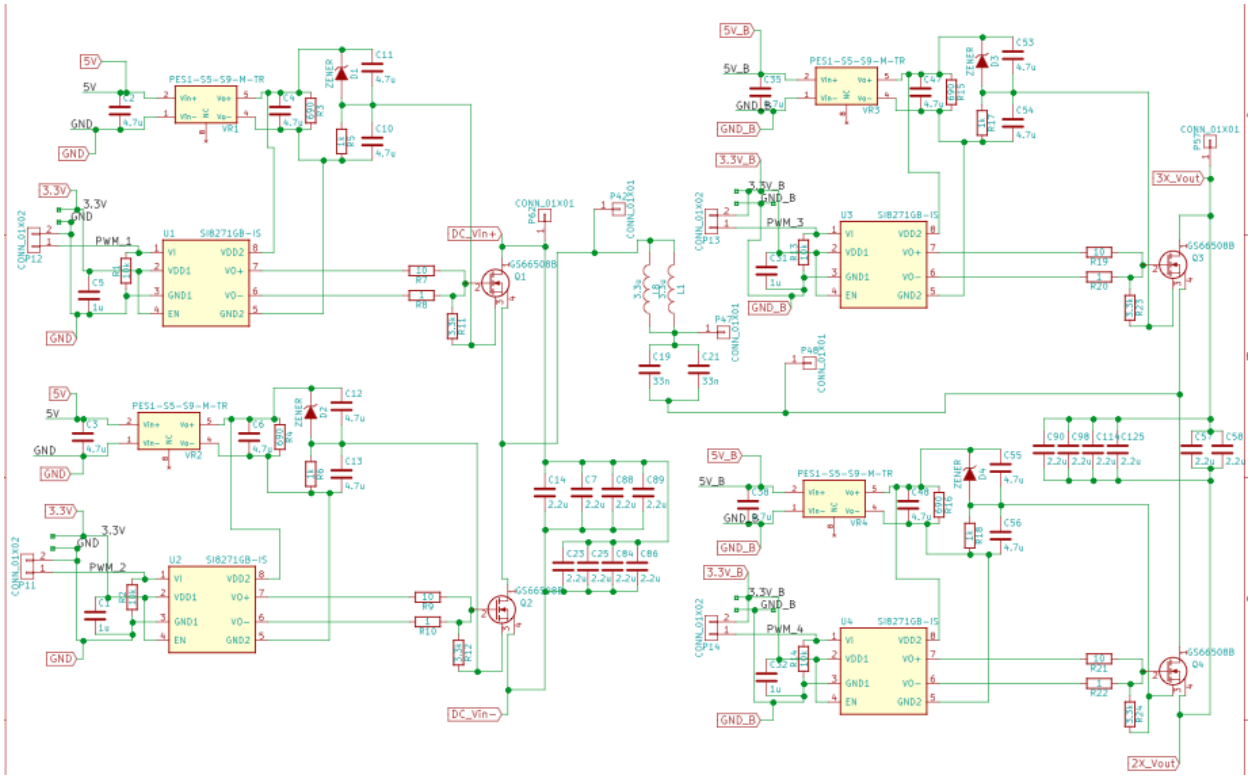

Figure 5.2. One RMMC Module Schematic

5.3. RMMC PCB Design

The PCB is a 6-layer design with 2 oz. copper on each layer. The board material that was selected was IT-180A to provide a higher dielectric strength than standard FR-4 and IT-180A can handle higher temperatures than standard FR-4. The PCB stack-up for the board is shown in Figure 5.3. An ENIG finish was selected for the board design.

	6L build up	
L1		finished copper 2.0oz
	0.19mm (prepreg 2116 + 1080)	
L2 L3	0.26mm core(excluding copper)	2.0 oz 2.0 oz
	0.23mm (prepreg 2116*2)	
L4 L5	0.26mm core(excluding copper)	2.0 oz 2.0 oz
	0.19mm (prepreg 2116 + 1080)	
L6		finished copper 2.0oz
	final board thickness: 62mil +/- 10%	

Figure 5.3. Custom PCB Stack-Up

The board was designed to minimize the high frequency current loops to minimize losses and to optimize the design so provide the clearance and creepage requirements for a high voltage board design but still provide the maximum power density. Both sides of the board were fully utilized to allow for design changes in the future. The resonant LC design allows for multiple resonant inductor and resonant capacitor placements to change the values so the resonant frequency can be changed and the capacitor voltage ripple can be changed based on the capacitance value. The design also allows for some of the modules to be bypassed when they are not in use so the board allows for higher flexibility when it is used for testing. The PCB layout with all 6 copper layers shown is featured in Figure 5.4. The bare PCB top and bottom sides are featured in Figure 5.5 and Figure 5.6, respectively.

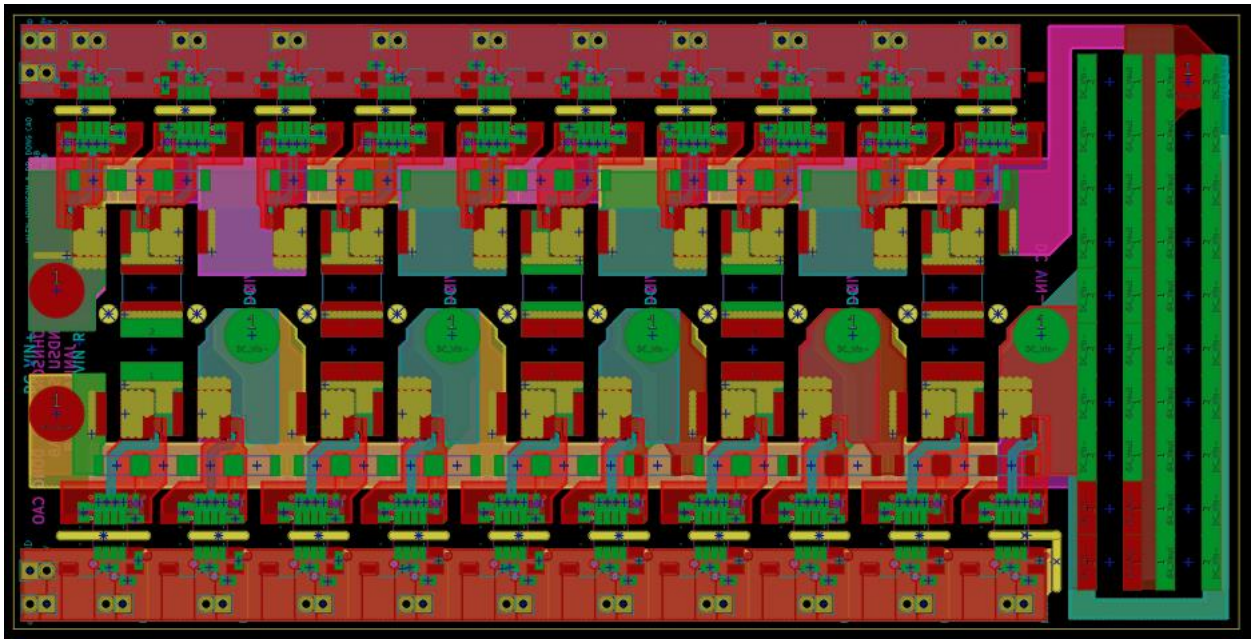

Figure 5.4. RMMC PCB Layout with 6 Copper Layers Shown

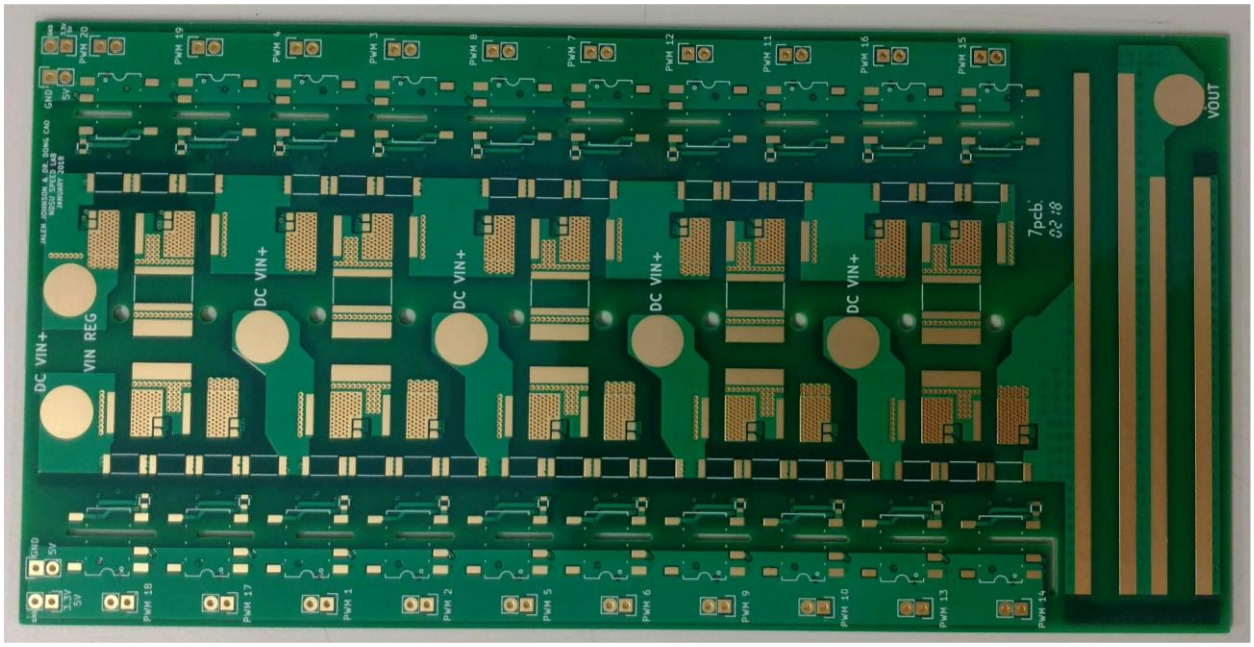

Figure 5.5. RMMC DCX PCB Top Side Bare Board

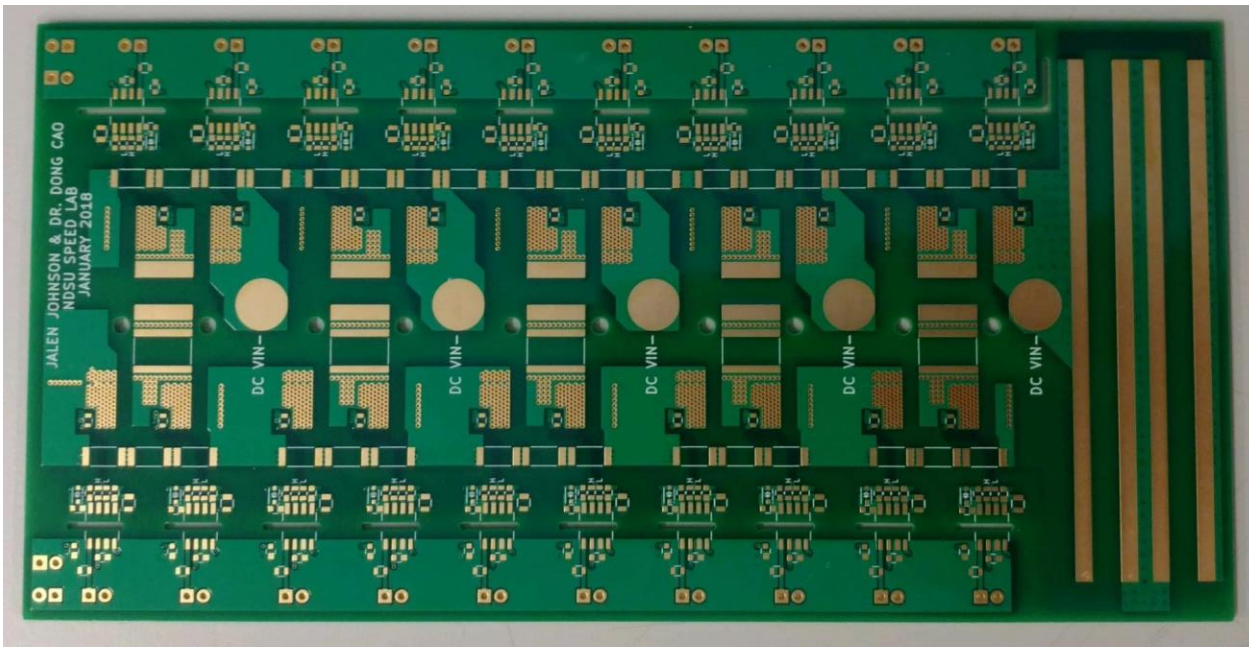

Figure 5.6. RMMC DCX PCB Bottom Side Bare Board

The board was assembled by hand and one circuit was assembled and verified before the whole board was assembled. The top side assembly is shown in Figure 5.7. The bottom side assembly is shown in Figure 5.8. The side profile of the fully assembled prototype is shown in Figure 5.9. The connection to add the PPVR converter is featured on the two connectors on the left side on the top of the RMMC board. These two terminals are shorted together when a PPVR circuit is not utilized.

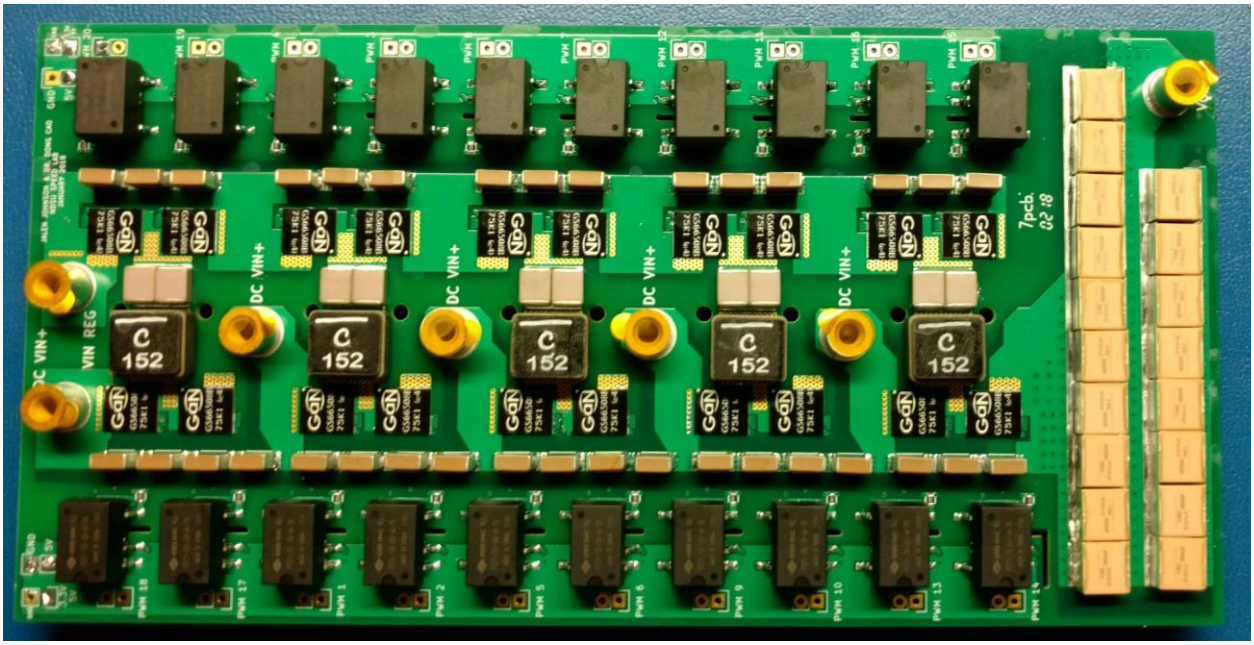

Figure 5.7. RMMC DCX Assembled Top Side

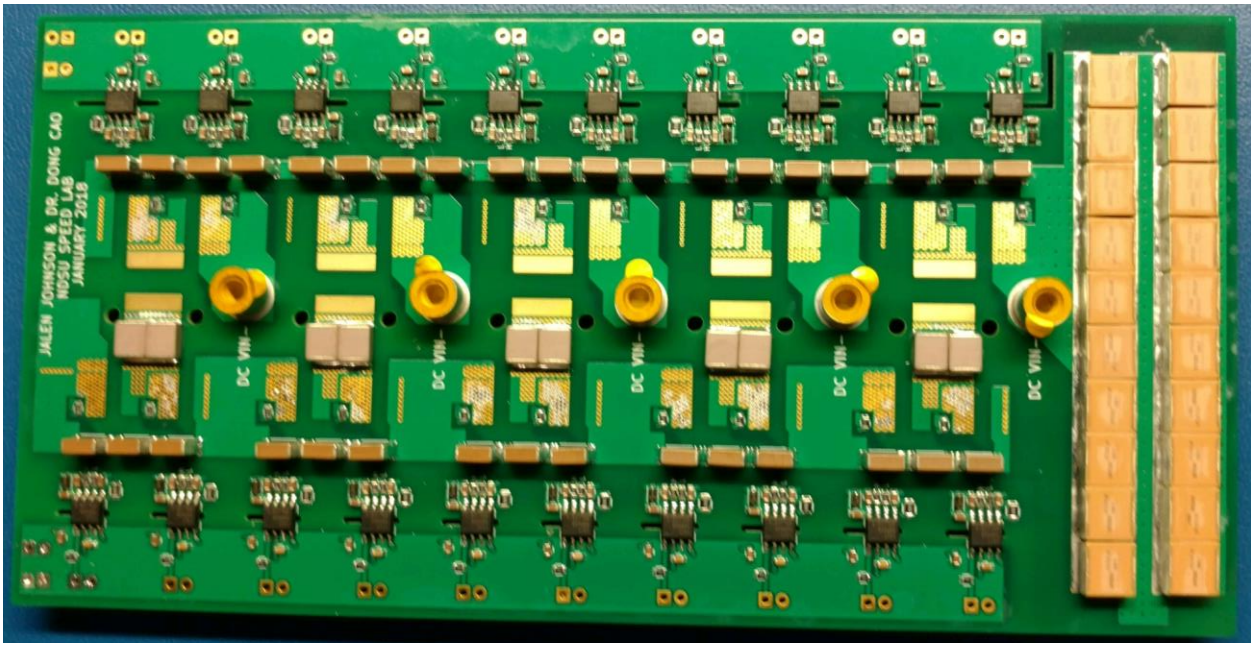

Figure 5.8. RMMC DCX Assembled Bottom Side

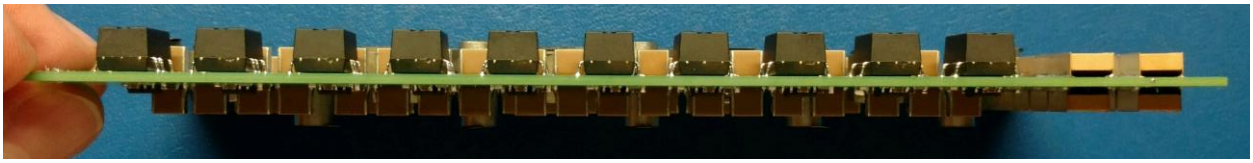
Figure 5.9. RMMC DCX Assembled Side View

5.4. PPVR Buck Converter Schematic

The buck converter PPVR board was based off of the gate drive design of the RMMC board featured in the previous sections. The schematic for the buck converter is shown in Figure 5.10.

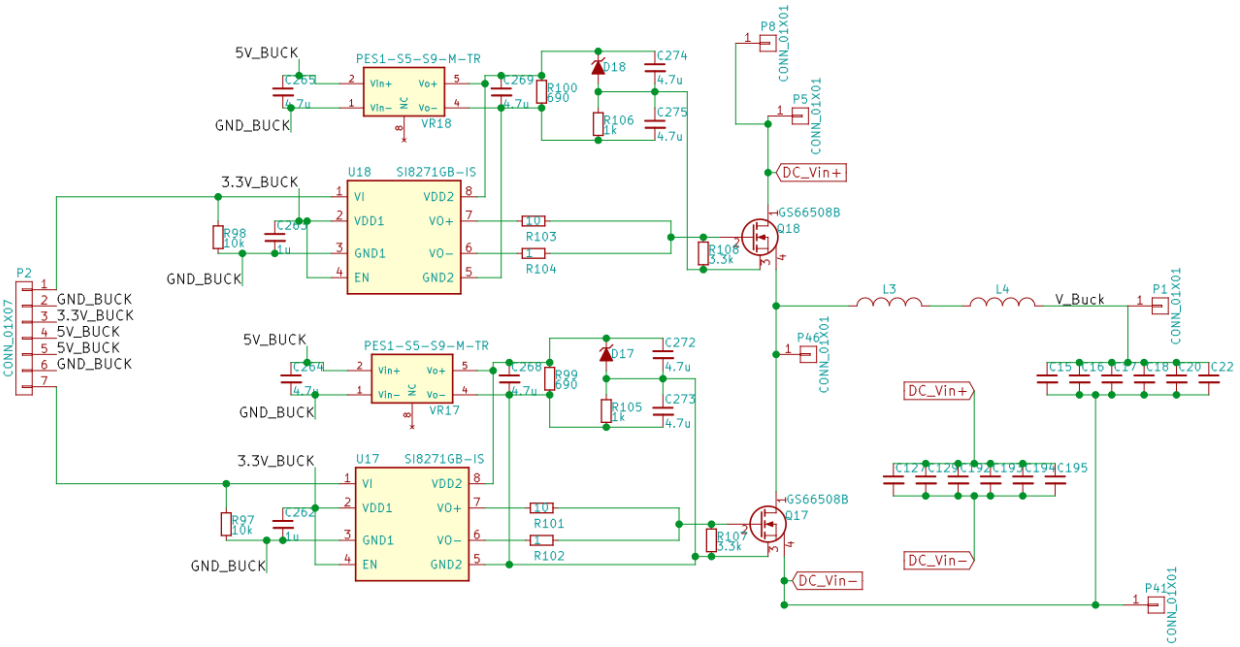

Figure 5.10. PPVR Buck Converter Schematic

5.5. PPVR Buck Converter PCB Design

The buck converter board is a 1 kW design that is a 6 layer board with 2 oz. copper on each layer. The board stack-up follows the same as the RMMC design shown in Figure 5.1. The buck converter used a high temperature 170 Tg FR-4 material instead of IT-180A based off of the materials that the PCB manufacturer had available. The PCB layout with all 6 layers shown is in Figure 5.11. The top and bottom sides of the buck converter prototype are featured in Figure 5.12 and Figure 5.12, respectively.

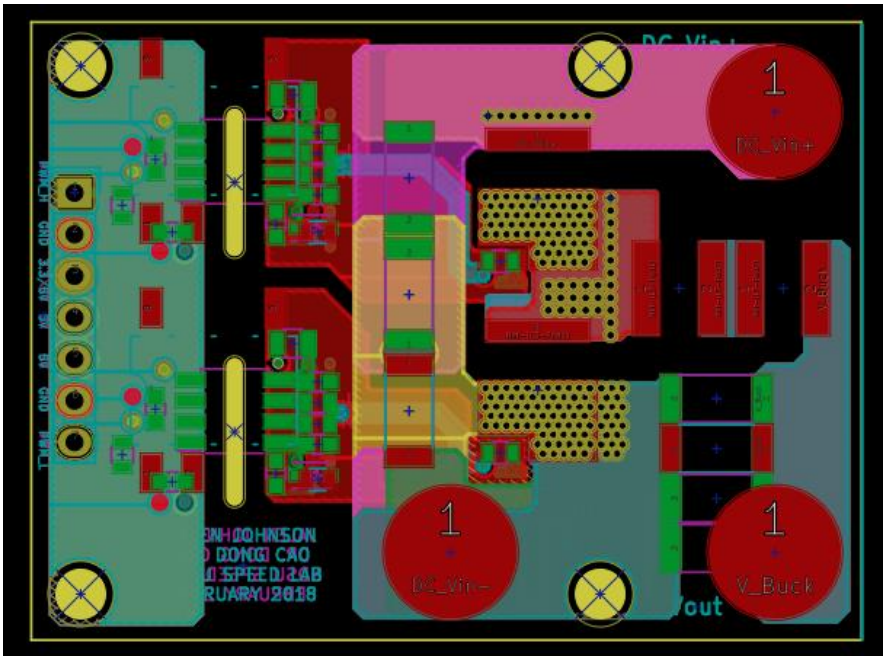

Figure 5.11. Buck Converter PCB Layout with 6 Copper Layers Shown

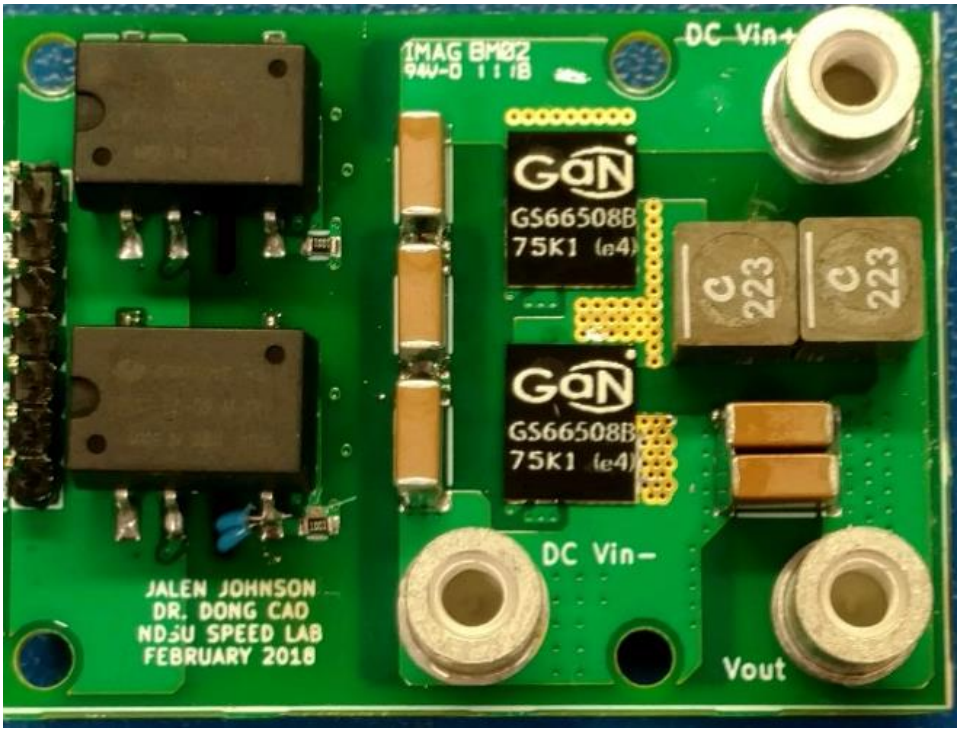

Figure 5.12. Buck Converter Top Side

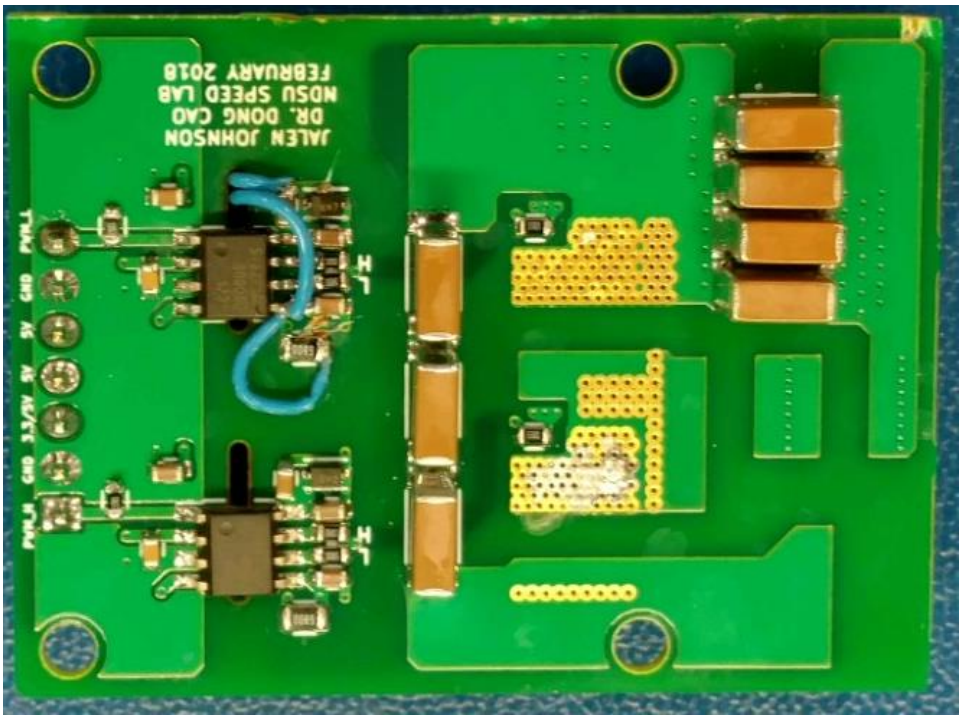

Figure 5.13. Buck Converter Bottom Side

5.6. Converter Efficiency Estimations

Efficiency estimation calculations were performed to develop an idea of the efficiency of the converter prototype. The calculations are based on the nominal 250 V battery input with a resistive load. The efficiency is calculated based on the MOSFET output capacitance loss, gate driver loss, inductor loss, capacitor ESR loss, and the MOSFET conduction loss. The output capacitance loss, Coss loss, calculation is shown in (Eq. 5.1). The gate driver loss calculation is shown in (Eq. 5.2). The inductor loss is the inductor copper loss and the core loss which were obtained from Coilcraft's online calculator. The capacitor ESR loss is shown in (Eq. 5.3) and the MOSFET conduction loss is shown in (Eq. 5.4).

$$C_{oss}\ \text{Loss} = \frac{C_{oss} {V_{DS}}^2 f_s}{2} \qquad \text{(Eq. 5.1)}$$

$$\text{Gate Driver Loss} = \left(\frac{V_G Q_G f_s}{2}\right)\left(\frac{R_{GH}}{R_{GH}+R_I+R_{ON}} + \frac{R_{GL}}{R_{GL}+R_I+R_{OFF}}\right) \quad \text{(Eq. 5.2)}$$

$$\text{Capacitor ESR Loss} = I^2 R_{ESR} \quad \text{(Eq. 5.3)}$$

$$\text{MOSFET Conduction Loss} = I^2 R_{DS(on)} \quad \text{(Eq. 5.4)}$$

The estimated efficiency of the converter is shown in Figure 5.14. The power loss breakdown of the system is shown in Figure 5.15. Figure 5.16 shows the breakdown in power loss between the DCX converter and the PPVR buck converter.

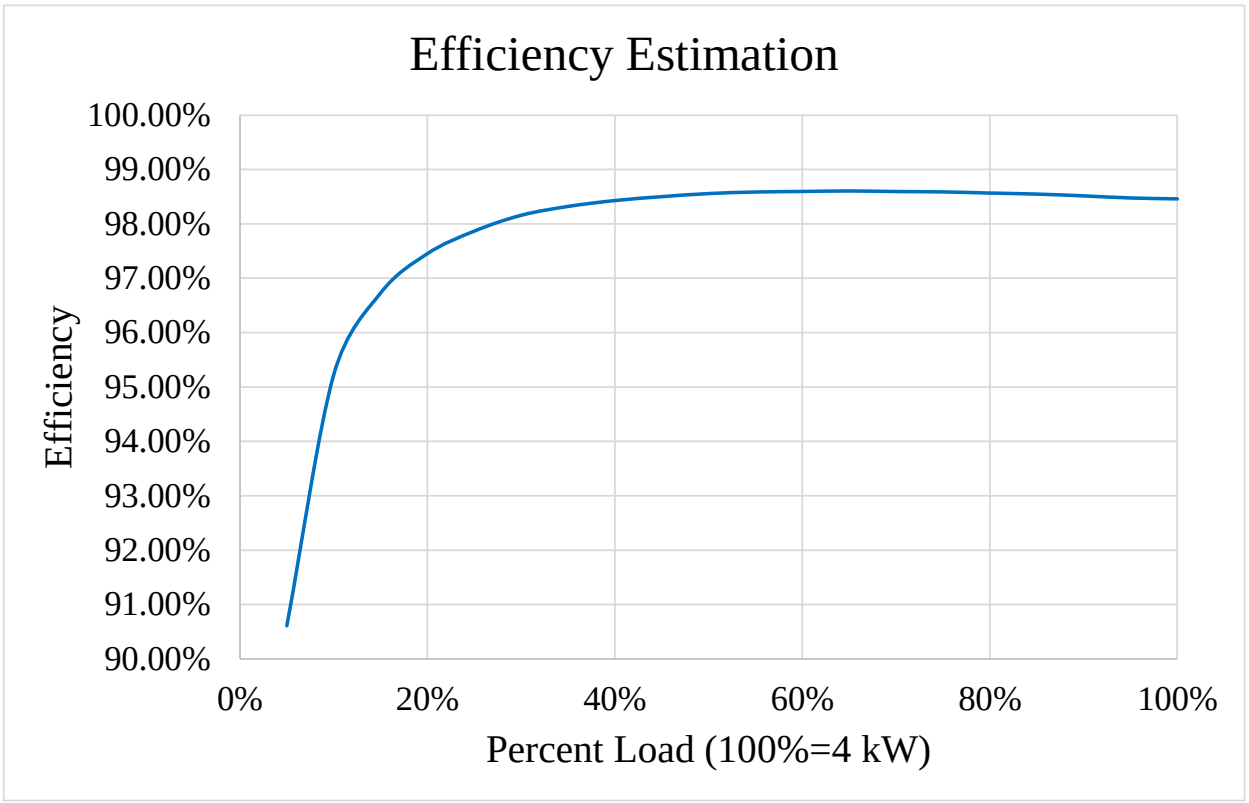

Figure 5.14. Estimated Converter Efficiency

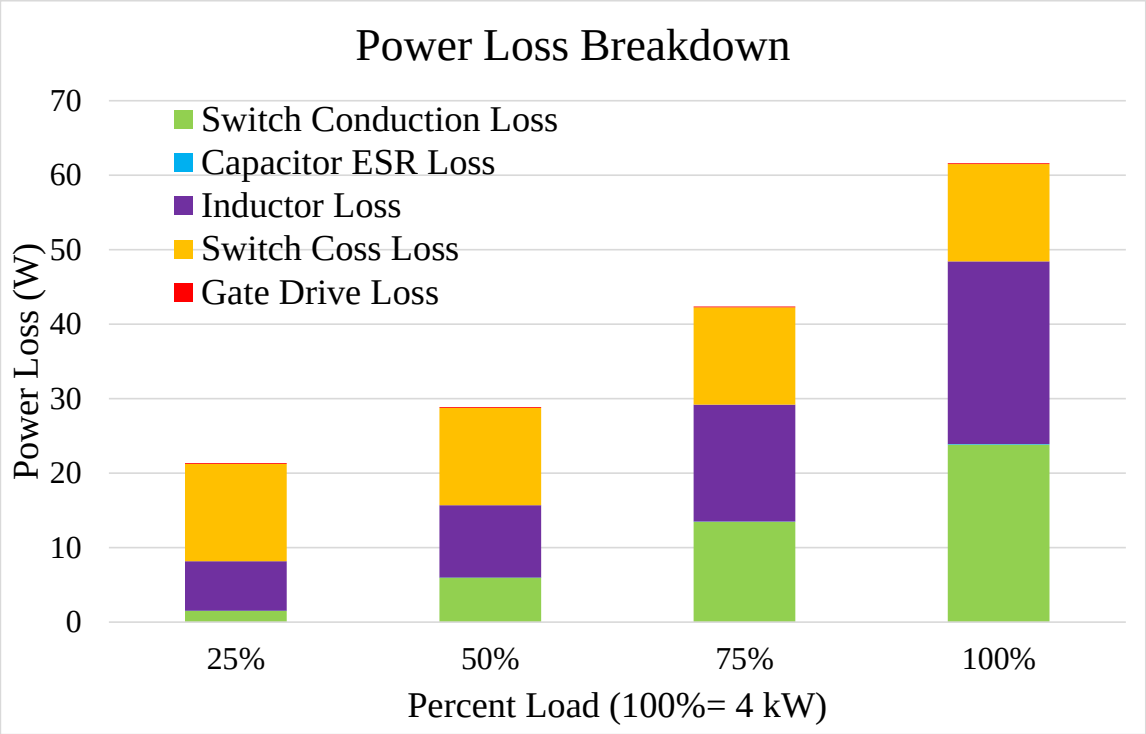

Figure 5.15. Power Loss Breakdown of System

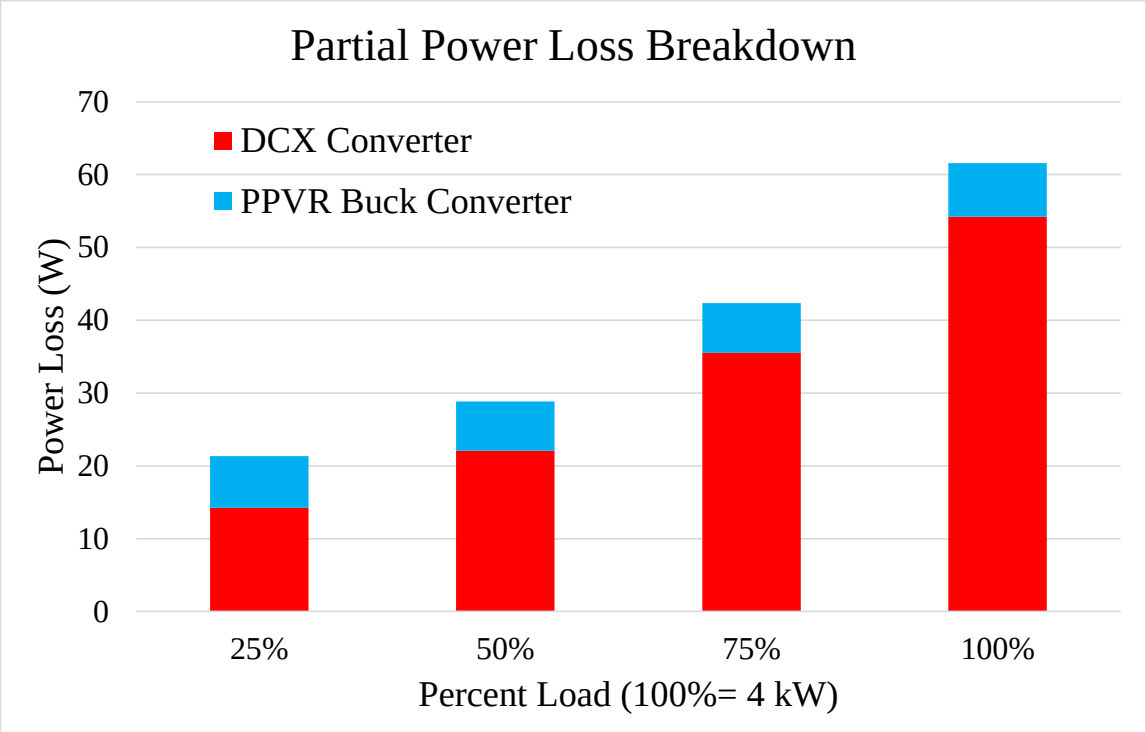

Figure 5.16. Power Loss Breakdown between DCX and PPVR

As shown in Figure 5.14, it is estimated that the converter reaches a peak efficiency of 98.6% at around 60% of the rated load. The main loss mechanisms of the converter are the MOSFET output capacitance loss, the inductor losses and the switch conduction losses. It is also shown that the PPVR circuit does not dominate the system losses which shows the advantage of using a partial power circuit.

5.7. Preliminary Results

Some preliminary results of the RMMC DCX prototype were obtained. To start, only two of the modules were activated with the other three being put into a pass through mode. This makes an unregulated conversion ratio of 3. A 40 V input was applied with a 150 ohm load. The output power was 100 watts. Figure 5.17 shows the input voltage, output voltage and the two inductor resonant current waveforms. Figure 5.18 shows the bridge side switch voltages for S_{B1} and S_{B2}. Figure 5.19 shows the bridge side switch voltages for S_{W1} and S_{W2}. From the switch voltage results, it is shown that the switch voltage stress is equal to the input voltage. Based on the results, the converter is working properly and testing will be continued for more power and higher conversion ratios in the future. Once confidence of the DCX converter is obtained, the PPVR buck converter prototype will be added to the system to obtain a regulated output voltage. The fully assembled RMMC prototype with the PPVR buck converter is featured in Figure 5.20.

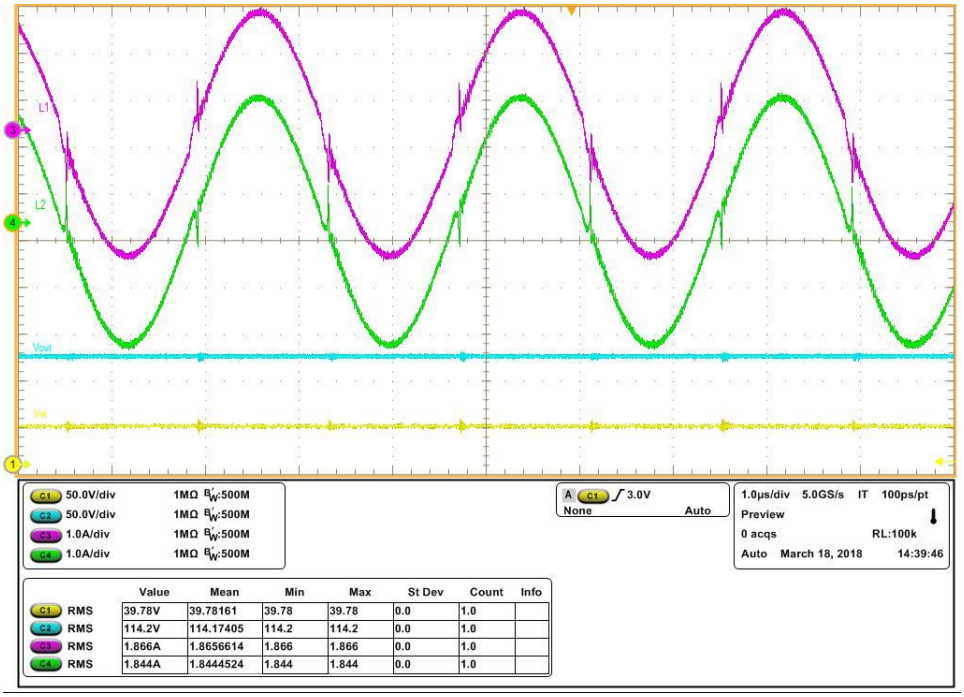

Figure 5.17. 3X DCX Converter Preliminary Output Results: V_{in}= 40 V, P= 100 W

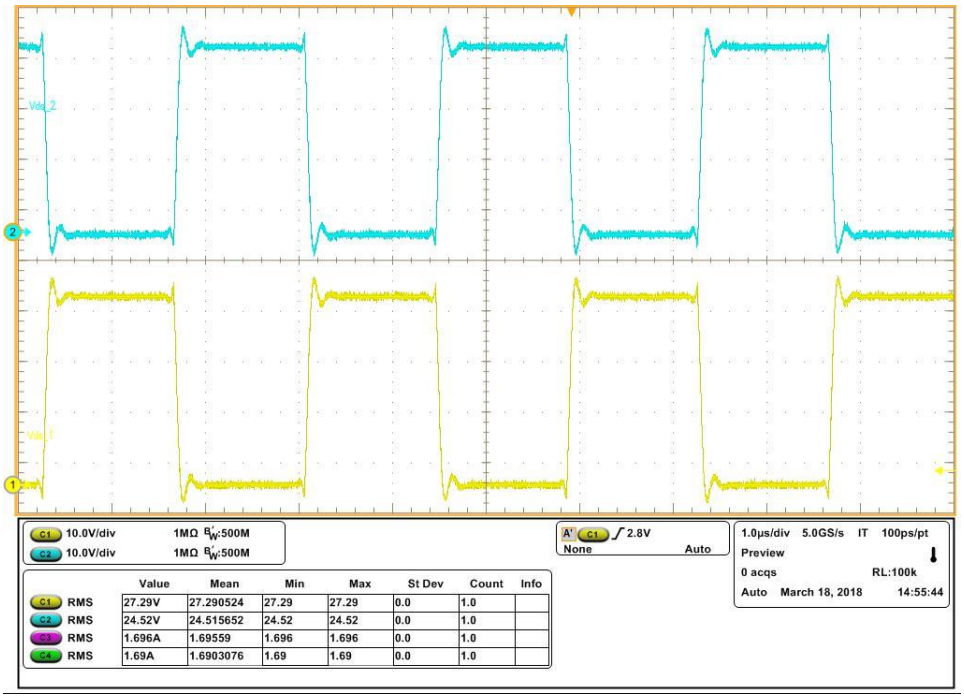

Figure 5.18. 3X DCX Converter Bridge Side Switch Voltages: V_{in}= 40 V, P= 100 W

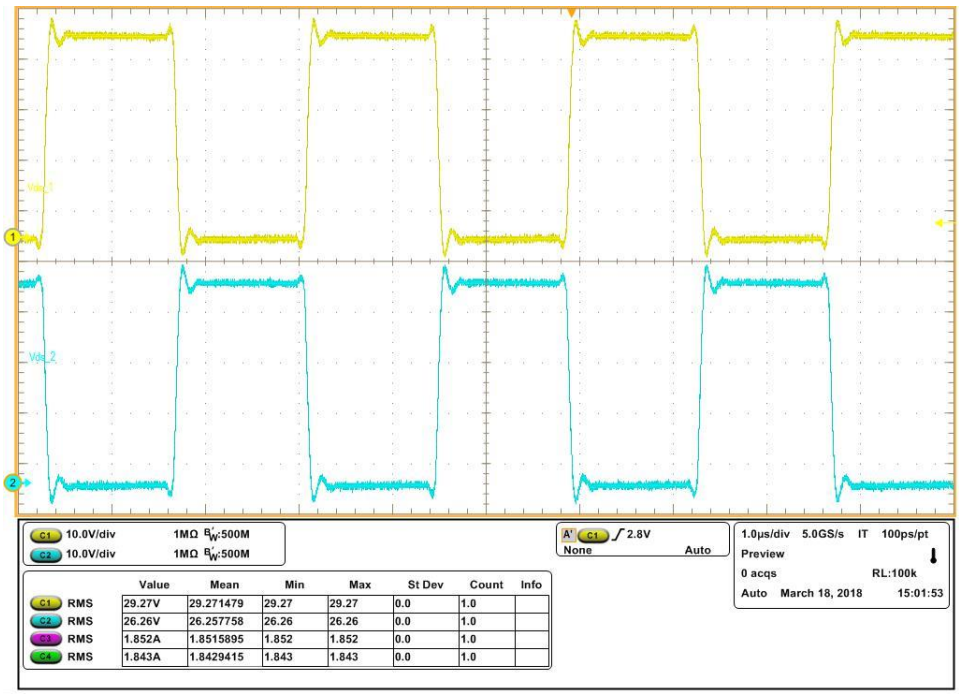

Figure 5.19. 3X DCX Converter Wing Side Switch Voltages: V_{in}= 40 V, P= 100 W

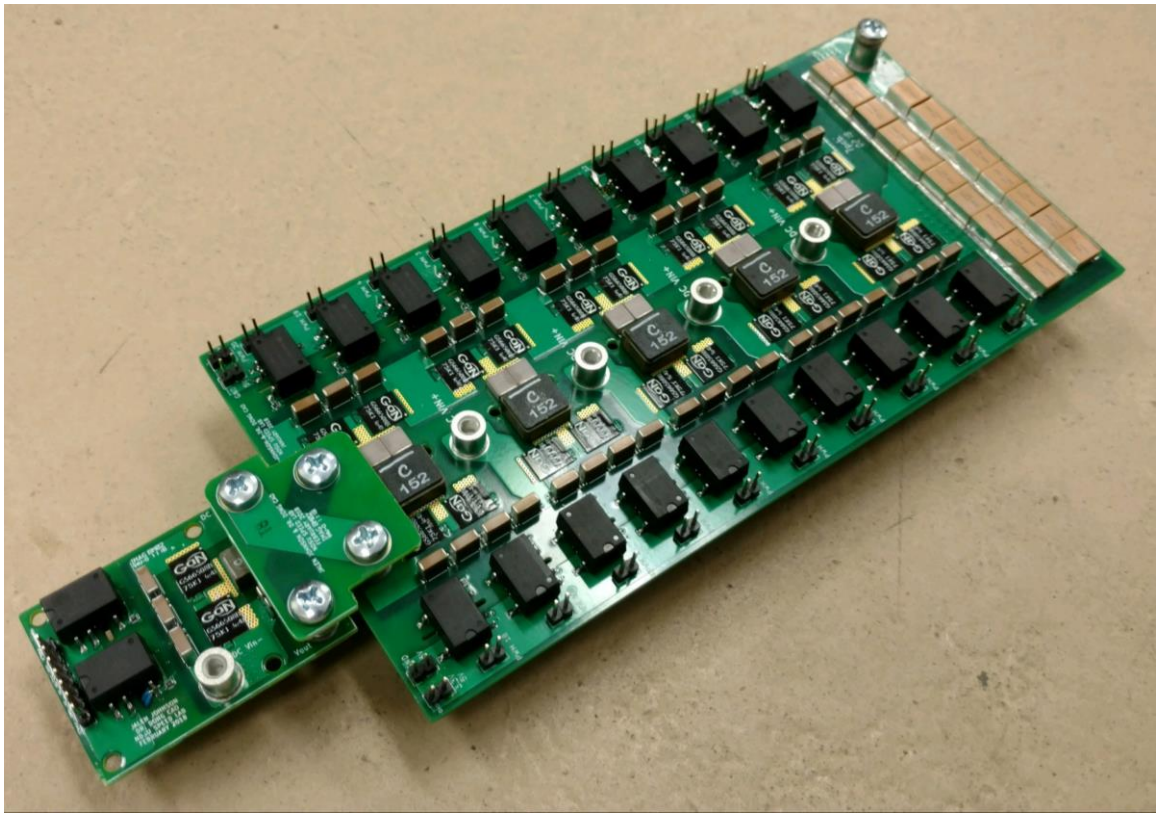

Figure 5.20. Fully Assembled 4 kW RMMC with Buck PPVR

6. CONCLUSION

This thesis presented two different approaches to boost the voltage for electrified vehicle applications. One approach was to boost the AC voltage in one stage rather than having a two stage approach where a boost converter increased the DC link voltage of the inverter. The other approach was to develop a very efficient boost converter topology that can replace the traditional boost converter topology and offer a very high overall efficiency.

The first approach featured a three-phase semi-quasi-z-source inverter topology that offered twice the output voltage of traditional inverter topologies and offered a sinusoidal output voltage due to the internal LC filter in the inverter topology. This system not only allows for a higher power density and less complex system because it eliminates the need for a boost converter, but the life of the electric motor is also extended due to the sinusoidal voltage. The downfall of this topology is that the voltage and current stresses are higher than a traditional inverter switching. As a result, the switches in this new topology will need higher voltage and current rating.

The second approach was to develop a much more efficient boost converter. This approach makes the system more complicated, but the increase in efficiency can outweigh the additional complexity. The converter design discussed in this thesis consists of a DCX converter stage and a partial power voltage regulation stage. This approach allows for a very efficient unregulated converter topology to become regulated with very few additional losses with the incorporation of the PPVR stage. The topology that was presented has an estimated efficiency of up to 98.6% with switching device stresses that are much lower than other leading composite converter designs that were discussed. This allows for smaller and cheaper switches to be used which increased converter power density and makes the converters cheaper.

REFERENCES

[1] Fang Zheng Peng, "Z-source inverter," in *IEEE Transactions on Industry Applications*, vol. 39, no. 2, pp. 504-510, Mar/Apr 2003.

[2] D. Cao, S. Jiang, X. Yu and F. Z. Peng, "Low-Cost Semi-Z-source Inverter for Single-Phase Photovoltaic Systems," in *IEEE Transactions on Power Electronics*, vol. 26, no. 12, pp. 3514-3523, Dec. 2011.

[3] D. Cao and F. Z. Peng, "A Family of Z-source and Quasi-Z-source DC-DC Converters," *2009 Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, Washington, DC, 2009, pp. 1097-1101.

[4] M. Shen, A. Joseph, J. Wang, F. Z. Peng and D. J. Adams, "Comparison of Traditional Inverters and Z -Source Inverter for Fuel Cell Vehicles," in *IEEE Transactions on Power Electronics*, vol. 22, no. 4, pp. 1453-1463, July 2007.

[5] "Bearing Currents in Modern AC Drive Systems." ABB Technical Guide No.5, http://https://library.e.abb.com/public/8c253c2417ed0238c125788f003c ca8e/ABB_Technical_guide_No5_RevC.pdf.

[6] "Motor Bearing Current Phenomenon." Yaskawa Application Note AN.AFD.17, https://www.yaskawa.com/pycprd/lookup/getfile/workspace&SpacesSto re&2eab05d0-6571-4fce-9295-7d886052459f&AN.AFD.17.pdf

[7] T. Zhao, V. Bhavaraju, P. Nirantare and J. Xu, "Evaluation of commercial scale transformerless solar inverter technology," *2015 IEEE Energy Conversion Congress and Exposition (ECCE)*, Montreal, QC, 2015, pp. 5342-5348.

[8] J. Johnson, D. Cao, X. Lyu and Z. Ni, "GaN based inverter with high conversion ratio and sinusoidal output for motor drive applications stress analysis," *2017 IEEE 5th*

Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Albuquerque, NM, 2017, pp. 195-200.

[9] M. Ahmed, C. Fei, F. C. Lee and Q. Li, "High-efficiency high-power-density 48/1V sigma converter voltage regulator module," *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Tampa, FL, 2017, pp. 2207-2212.

[10] Ming Xu, Ya Liu, Julu Sun and F. C. Lee, "Σ/sigma DC/DC conversion for computing and telecom applications," *2008 IEEE Power Electronics Specialists Conference*, Rhodes, 2008, pp. 1190-1195.

[11] H. Chen, K. Sabi, H. Kim, T. Harada, R. Erickson and D. Maksimovic, "A 98.7% Efficient Composite Converter Architecture With Application-Tailored Efficiency Characteristic," in *IEEE Transactions on Power Electronics*, vol. 31, no. 1, pp. 101-110, Jan. 2016.

[12] H. Chen, H. Kim, R. Erickson and D. Maksimović, "Electrified Automotive Powertrain Architecture Using Composite DC–DC Converters," in *IEEE Transactions on Power Electronics*, vol. 32, no. 1, pp. 98-116, Jan. 2017.

[13] Julu Sun, Ming Xu, D. Reusch and F. C. Lee, "High efficiency quasi-parallel Voltage Regulators," *2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition*, Austin, TX, 2008, pp. 811-817.

[14] N. Zhang, S. Batternally, K. C. Lim, K. W. See and F. Han, "Analysis of the non-inverting buck-boost converter with four-mode control method," *IECON 2017 - 43rd Annual Conference of the IEEE Industrial Electronics Society*, Beijing, 2017, pp. 876-881.

[15] A. Lidow and J. Strydom, “Gallium Nitride (GaN) Technology Overview,” Efficient Power Conversion Corporation, El Segundo, CA, USA, 2012.

[16] S. Colino and R. Beach, “Fundamentals of Gallium Nitride Power Transistors,” Efficient Power Conversion Corporation, El Segundo, CA, USA, 2011.

[17] N. Kaminski, "State of the art and the future of wide band-gap devices," *2009 13th European Conference on Power Electronics and Applications*, Barcelona, 2009, pp. 1-9.

[18] B. J. Baliga, "Power semiconductor device figure of merit for high-frequency applications," in *IEEE Electron Device Letters*, vol. 10, no. 10, pp. 455-457, Oct. 1989.

[19] Y. Li, X. Lyu, D. Cao, S. Jiang and C. Nan, "A high efficiency resonant switched-capacitor converter for data center," *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Cincinnati, OH, 2017, pp. 4460-4466.

[20] Dong Cao and Fang Zheng Peng, "Zero-current-switching multilevel modular switched-capacitor dc-dc converter," *2009 IEEE Energy Conversion Congress and Exposition*, San Jose, CA, 2009, pp. 3516-3522.

APPENDIX. MATLAB CODE FOR SEMI-QUASI-Z-SOURCE INVERTER SWITCH CURRENT CALCULATIONS

```
clear all;
close all;
tic
fs=100020;%switching frequency 100 kHz
fo=60;%fundemental frequency
res=60000; %number of steps per fs cycle
step=1/(fs*res); %step size
cycle=1; %number of periods
w=2*pi*fo;%angular frequency
Ts=1/fs;%switching period
Vin=200; %Vin
R=6; %Load Resistance
io_peak=Vin/R; %peak output current
N=fs/fo;%N points during one fundamental period
N_Cyc=N*cycle;
t=0:step:cycle/fo;
D=zeros(1,N*cycle);
Dz=zeros(1,N*cycle);
Dz_2=zeros(1,N*cycle);
Dboost=zeros(1,N*cycle);
T=zeros(1,N*cycle);
Tz=zeros(1,N*cycle);
Tz_2=zeros(1,N*cycle);
Tboost=zeros(1,N*cycle);
Ti=zeros(1,N*cycle);
Ti_z=zeros(1,N*cycle);
Ti_z_2=zeros(1,N*cycle);
Ti_boost=zeros(1,N*cycle);
i=zeros(1,length(t));
iz=zeros(1,length(t));
iz_2=zeros(1,length(t));
iboost=zeros(1,length(t));
DCDC_Duty=0.5;
Voll_z=Vin*sqrt(3)/sqrt(2);
Voll_boost=Vin/DCDC_Duty*sqrt(3)/2/sqrt(2);
Pout_Z=Voll_z*io_peak/sqrt(2)*sqrt(3);
Pout_boost=Voll_boost*io_peak/sqrt(2)*sqrt(3);
I_DCDC=Pout_boost/Vin;

for n=1:N*cycle
 Dz(n)=Ts*((1-sin(2*pi*n/N))./(2-sin(2*pi*n/N)));
 %Dz(n)=Ts*((1)./(2-sin(2*pi*n/N)));
 %D(n)=abs(Ts*(sin(2*pi*n/N)));
 Tz(n)=Ts*n;
 if(n==1)
     Ti_z(n)=Dz(n);
 end
 if(n>1)

   Ti_z(n)=Tz(n-1)+Dz(n);
 end
```

```
end
irms_z=0;
n=1;

for k=1:length(t)
   if(mod(k,res)==0 && n<N_Cyc)
       n=n+1;
   end


        if(t(k)<=Ti_z(n))
            %i(k)=io_peak.*sin(w.*t(k));
           iz(k)=((io_peak.*-(2.*sin(w.*t(k))-sin(w.*t(k)).*...
               sin(w.*t(k)))));

        end
        if(t(k)>Ti_z(n))
            iz(k)=0;
        end

  irms_z=irms_z+((iz(k).*iz(k)));
end
Z_Irms=sqrt(irms_z*(1/length(t)))

figure
%subplot(411)
plot(t,iz)
title('S1 Current')
ylim([-io_peak*1.1 3*io_peak*1.1])
xlim([0 (1/fo)*cycle])
ylabel('Current (Amps)')
xlabel('Time (s)')


%
%%%
%%%%%
%%%%%%%
%%%%%%%%%
%%%%%%%%%%%
%%%%%%%%%
%%%%%%%
%%%%%
%%%
%

for n=1:N*cycle
 Dz_2(n)=Ts*((1)./(2-sin(2*pi*n/N)));
 %Dz(n)=Ts*((1)./(2-sin(2*pi*n/N)));
 %D(n)=abs(Ts*(sin(2*pi*n/N)));
 Tz_2(n)=Ts*n;
 if(n==1)
     Ti_z_2(n)=Dz_2(n);
 end
 if(n>1)
```

```
   Ti_z_2(n)=Tz_2(n-1)+Dz_2(n);
 end
end
irms_z_2=0;
n=1;

for k=1:length(t)
   if(mod(k,res)==0 && n<N_Cyc)
       n=n+1;
   end


        if(t(k)<=Ti_z_2(n))
            %i(k)=io_peak.*sin(w.*t(k));
           iz_2(k)=-((io_peak.*-(2.*sin(w.*t(k))-sin(w.*t(k)).*...
               sin(w.*t(k)))));

        end
        if(t(k)>Ti_z_2(n))
            iz_2(k)=0;
        end

  irms_z_2=irms_z_2+((iz_2(k).*iz_2(k)));
end
Z_Irms_2=sqrt(irms_z_2*(1/length(t)))

figure
%subplot(412)
plot(t,iz_2)
title('S2 Current')
ylim([-io_peak*3.1 io_peak*1.1])
xlim([0 (1/fo)*cycle])
ylabel('Current (Amps)')
xlabel('Time (s)')


%
%%%
%%%%%
%%%%%%%
%%%%%%%%%
%%%%%%%%%%
%%%%%%%%%
%%%%%%%
%%%%%
%%%
%
for n=1:N*cycle
 %Dz(n)=Ts*((1-sin(2*pi*n/N))./(2-sin(2*pi*n/N)));
 %D(n)=abs(Ts*(sin(2*pi*n/N)));
 D(n)=(Ts*(0.5+(0.5.*sin(2*pi*n/N))));
 %D(n)=Ts*0.5;
 T(n)=Ts*n;
 if(n==1)
```

```
     Ti(n)=D(n);
 end
 if(n>1)

  Ti(n)=T(n-1)+D(n);
 end
end
irms_boost=0;
n=1;
for k=1:length(t)
   if(mod(k,res)==0 && n<N_Cyc)
       n=n+1;
   end


        if(t(k)<=Ti(n))
            i(k)=io_peak.*sin(w.*t(k));
           %(k)=((io_peak.*-(2.*sin(w.*t(k))-sin(w.*t(k)).*sin(w.*t(k)))));

        end
        if(t(k)>Ti(n))
            i(k)=0;
        end

  irms_boost=irms_boost+((i(k).*i(k)));
end
Boost_Irms=sqrt(irms_boost*(1/length(t)))

figure
%subplot(413)
plot(t,i)
title('Three Phase w/Boost Switch Current')
ylim([-1.1*io_peak 1.1*io_peak])
xlim([0 (1/fo)*cycle])
ylabel('Current (Amps)')
xlabel('Time (s)')



%
%%%
%%%%%
%%%%%%%
%%%%%%%%%
%%%%%%%%%%%
%%%%%%%%%
%%%%%%%
%%%%%
%%%
%


for n=1:N*cycle
 %Dz(n)=Ts*((1-sin(2*pi*n/N))./(2-sin(2*pi*n/N)));
 %D(n)=abs(Ts*(sin(2*pi*n/N)));
```

```
 %D(n)=(Ts*(0.5+(0.5.*sin(2*pi*n/N))));
 Dboost(n)=Ts*DCDC_Duty;
 Tboost(n)=Ts*n;
 if(n==1)
     Ti_boost(n)=D(n);
 end
 if(n>1)

  Ti_boost(n)=Tboost(n-1)+D(n);
 end
end
irms_dcdc_boost=0;
n=1;
for k=1:length(t)
   if(mod(k,res)==0 && n<N_Cyc)
       n=n+1;
   end


        if(t(k)<=Ti_boost(n))
            iboost(k)=I_DCDC;
           %(k)=((io_peak.*-(2.*sin(w.*t(k))-sin(w.*t(k)).*sin(w.*t(k)))));

        end
        if(t(k)>Ti_boost(n))
            iboost(k)=0;
        end

  irms_dcdc_boost=irms_dcdc_boost+((iboost(k).*iboost(k)));
end
Boost_DCDC_Irms=sqrt(irms_dcdc_boost*(1/length(t)))

figure
%subplot(414)
plot(t,iboost)
title('DCDC Boost Switch Current')
ylim([(0-0.1*I_DCDC) 1.1*I_DCDC])
xlim([0 (1/fo)*cycle])
ylabel('Current (Amps)')
xlabel('Time (s)')

Semi_Z_Current_Stress_Ratio= (3.*(Z_Irms.*Z_Irms)+3.*(Z_Irms_2.*...
    Z_Irms_2))./((io_peak./sqrt(2)).*(io_peak./sqrt(2)))
Three_Phase_Boost_Current_Stress_Ratio= (6.*(Boost_Irms.*Boost_Irms)...
    +2.*(Boost_DCDC_Irms.*Boost_DCDC_Irms))./((io_peak./sqrt(2)).*...
    (io_peak./sqrt(2)))
Ratio_Semi_Z_to_Three_Phase_Boost=Semi_Z_Current_Stress_Ratio./...
    Three_Phase_Boost_Current_Stress_Ratio
toc
```