POWER EFFICIENT EMBEDDED MEMORY DESIGN FOR MOBILE VIDEO APPLICATIONS

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The Supervisory Committee certifies that this ***disquisition*** complies with North Dakota State University's regulations and meets the accepted standards for the degree of

MASTER OF SCIENCE

SUPERVISORY COMMITTEE:

Na Gong
Chair

Rajesh Kavasseri

Jacob Glower

Canan Bilen-Green

Approved:

04/07/2015
Date

Scott C. Smith
Department Chair

ABSTRACT

This thesis mainly addresses the issue of low-power technology for streaming media applications. In order to ensure high output video quality under low-voltage supply, the proposed 8-bit pixel memory is sized by different bit positions. A novel MSE_{pixel} estimation method is then developed according to bit failure rates to directly evaluate the video quality for every 8-bit sizing combination. Based on this estimation, one area-priory and one quality-priority mobile video applications are proposed by SPIDER algorithms.

The results show that both luma and chroma data should be considered. More than 70% power is saved in memory units by using sizing-priority SPIDER algorithms. And the proposed SPIDER design methodology for low-voltage application is a feasible and efficient trade-off between the memory reliability and area overhead. Besides, a sample SRAM chip is designed for tape-out for further verification of the proposed SPIDER methodology.

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DEDICATION

I dedicate this thesis work to my beloved family for their unconditional love and support, especially my deceased grandparents who gave their amazing love to me without expecting anything in return.

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CHAPTER 1. INTRODUCTION

1.1. Background

Since Dawon Kahng and Martin Atalla invented the Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) at Bell Labs in 1960, MOSFET has become the predominant basic element in silicon integrated circuits (IC). Complementary Metal Oxide Semiconductor (CMOS), combined by a p-type and an n-type MOSFETs, is now widely used to implement various logic gates in digital integrated circuits found in mobile devices, computers, etc. This essentially benefits from the geometric downsizing from semiconductor manufacturing processes.

Over the past decade, typical transistors have been geometrically scaled down in size from several micrometers to only dozens of nanometers. With the size scaled down, transistors have lower gate capacitance and lower on-state resistance. Besides, scaled transistors also mean smaller silicon area, and lower cost per chip.

On the other hand, technology scaling brings subsequent challenges mainly from process control and circuit and physical design, such as design complexity, costs, random process variation, reliability, and power issues. Among all these challenges, power dissipation is the most critical one, which may limit further development of digital integrated circuits. Based on published results in ISSCC [1], the power dissipations of chips were increasing very fast (4 times every 3 years) before 1990 as shown in Figure 1. Since then, designers began to restrict overall power consumption increasing at a slower rate (1.4 times every 3 years).

Obviously, power consumption problem becomes a more and more critical issue in IC design, especially in Very-Large-Scale Integration (VLSI) technology, though reducing transistors in size means the switching capacitance also decreases, power consumption becomes higher due to the following reasons.

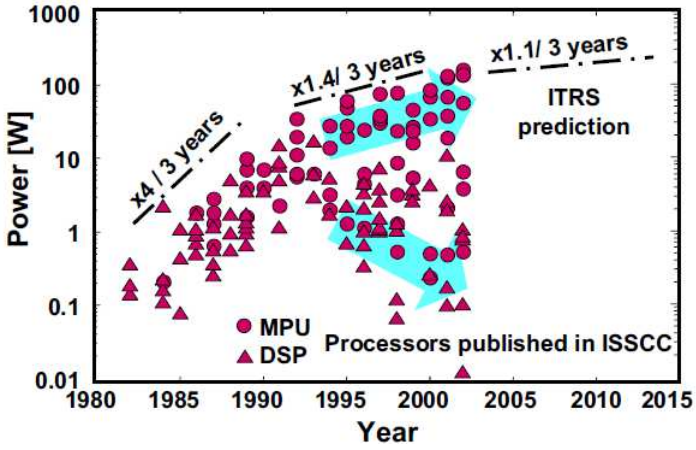


Figure 1. Increasing VLSI power [1]

One of the reasons of power consumption increase in an IC design is that transistor speed/density is becoming higher and higher so that the power dissipation per unit area increases as technology evolves. Another reason is that, in order to offset the downgrade problem of switching speed increase, new techniques are employed in the device, which cause higher power densities and power leaky, especially for mobile applications. The third reason comes from the System-on-Chip (SoC) and System-in-Package (SiP) technology, which combine many different function blocks into one IC, and result in chip power dissipation and heat disposal problems.

In general, with the transistor scaled down in size, the power dissipation, on the contrary, keeps increasing. This particularly becomes a critical problem in battery-based device such as mobile phone application. A successful design has to address the issue of power dissipation via design and technology innovations.

1.2. Motivation

Recently, mobile devices such as smart-phones and tablets have become the most important medium. And mobile embedded memory incurs large power consumption owing to the high frequent access and extensive computation. On the other hand, According to research from Cisco

in Feb. 2013, two-thirds of global mobile data traffic will be driven by video by 2017 [2]. Figure 2 shows an example of a video streaming system. The original video is compressed to reduced number of data bits and then transmitted to mobile devices over a communication channel based on a specific protocol, such as Apple's HTTP Live Streaming (HLS). And video decoding has become the most important energy-intensive application used in mobile devices [3]. In particular, the major signal processing units in video decoders, such as motion estimation, require a significant number of calculations and need frequent embedded memory accesses. Embedded SRAM occupies over 65% of the core area of a video decoder chip [4] and contributes to over 30% of the system power consumption of a mobile device [5,6,7,8].

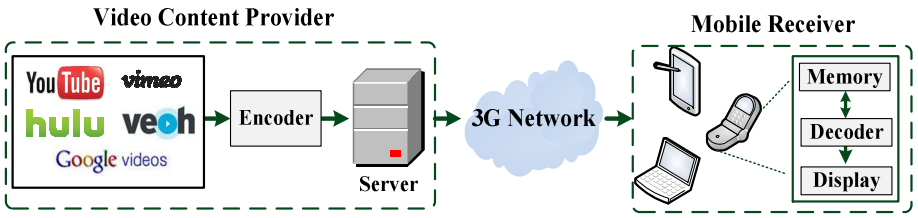


Figure 2. Mobile video streaming

Supply voltage scaling is one of the most effective techniques to reduce power consumption of memory [2,3,9,10,11,12,13]. However, there are three main considerations for low-voltage memory designers: (1) the noise margin of conventional SRAM deteriorates significantly due to process variation at low voltage; (2) reducing the area overhead of low power embedded SRAM is another major design concern; and (3) various mobile video applications have different requirements, from area-priority applications such as healthcare video streaming to quality-priority applications such as HD video and 3D gaming.

1.3. Contributions

In this thesis, a Sizing-PrIority based application-Driven mEmoRy (SPIDER) design methodology is developed for power efficient mobile video applications. The contributions are listed as follows:

(1) With the failure characteristics analysis, a novel priority-based SRAM sizing methodology is represented to enhance SRAM faulty tolerance ability. For every 6T SRAM bit-cell, the proposed sizing technique only increases the sizes of two access NMOS transistors, the most sensitive transistors to failure, thereby reducing the area overhead rate in an acceptable limit. It is proved that this sizing method is an optimal trade-off between bit-cell reliability and size overhead.

(2) A novel MSE_{pixel} estimation method is developed to directly evaluate the video quality for every 8-bit sizing combination. This estimation builds a calculable relation between memory bit failure rate decided by the memory sizing and output video quality PSNR. And compared with conventional estimation method, it considers not only luma effects but also chroma effects to video quality, thus avoids over-optimization.

(3) Based on this MSE_{pixel} estimation, SPIDER algorithms are designed for area-priority and quality-priority applications, maximizing the power efficiency.

(4) A hardware-based evaluation flow is designed, in which bit-cell failure is precisely injected into the proposed memory based on a Verilog-based H. 264 decoder. In order to achieve an automatic evaluation process, a Python-assisted controlling scheme is programmed for a HSPICE and Matlab based failure analysis process.

(5) NCSU 45nm technology is utilized in the proposed SRAM model. Based on this model, area-priority and quality-priority SPIDER simulations are performed, and related results are

concluded. It is proved that the proposed SPIDER design methodology for low-voltage application is a feasible and efficient trade-off between the memory reliability and area overhead.

(6) Four different sizing combinations and related peripheral circuits are designed as a sample SRAM chip for future power consumption tests by Cadence software. This chip has been sent to MOSIS Integrated Circuit Fabrication Service for tape-out. It will be very helpful for further verification of the proposed SPIDER methodology.

1.4. Organization

Chapter 2 introduces H.264 video decoding processes, and indicates the application of proposed low-power embedded SRAM. PSNR-based objective quality measurement is introduced for video quality evaluation algorithm. Chapter 3 points out that low-voltage method is adopted for proposed SPIDER design, and also shows that varying only two access NMOS transistors in standard 6T SRAM is an optimal compromise method. Chapter 4 proposes a novel MSE_{pixel} estimation method which can be directly used to evaluate the video quality for different sizing combinations. Based on this estimation, one area-priory and one quality-priority mobile video applications are then developed by SPIDER algorithm. Chapter 5 presents the output video quality (PSNRs) in both area-priority and quality-priority applications, and the chip tape-out design. Some results are listed to support those conclusions. Chapter 6 concludes this research. Chapter 7 presents other contributions on wind energy conversion system of wind turbine in author's Master program. A maximum power point tracking scheme for a PMSG-based variable-speed wind energy conversion system is proposed. Its mathematical model of the wind power system is built and simulated by MATLAB/SIMULINK software. And the related results are concluded.

CHAPTER 2. VIDEO CODEC OVERVIEW

Video codec is an essential technology for applications such as videoconferencing and streaming media. Standardizing video compression makes it possible for storage or transmission of digital video content (a data file or bitstream). The proposed SPIDER is discussed in H.264 format which is one of the most popular video codec standards in mobile multimedia communications. Based on the concepts of earlier standards, it offers the potential for better compression efficiency, such as better-quality compressed video, and greater flexibility in compressing, transmitting and storing video [14].

H.264 is also a set of tools for video compression and digital video communication. In a typical application of H.264, video from a camera is converted into a compressed format using H.264 to produce a related bitstream. Then the bitstream is sent to a decoder across a network, in which it is decompressed to a version of the source video.

2.1. Brief of Decoder Processes

For a mobile device, only decoding process is considered. A typical H.264 decoder extracts the information from each of the syntax elements, such as quantized transform coefficients, prediction information, etc. And the information can then be used to recreate a sequence of video frames.

Figure 3 shows the general block diagram of the H.264 decoder. In this process, the decoded video frames can be reconstructed by adding the prediction to the decoded residual. And the prediction is created by the inter prediction from previously-decoded frames and intra prediction from previously-decoded samples in the current frame. For all coded data, some parameter sets and slices, such as those used for reference frames, are considered as high priority, since their loss could make it difficult to decode subsequent coded slices. Therefore, these

reference slices should be stored much more reliably. Any fault happened in this kind of memory will nonlinearly affect the output video quality seriously.

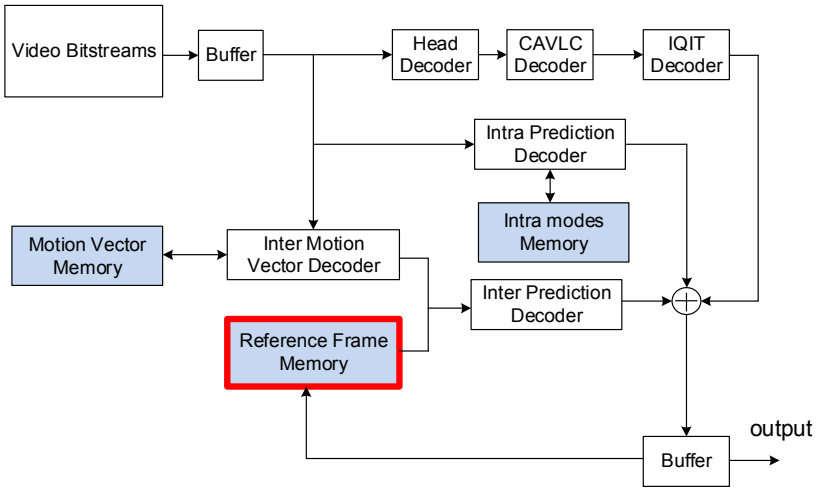


Figure 3. Block diagram of H.264 decoding processes

On the other hand, embedded SRAM consumes large power due to the frequent accesses, which is the dominant contributor to the entire H.264 decoder power [10]. Scaling supply power is one of the effective solutions for the power consumption problem, which will be discussed in chapter 3. Therefore higher reliable low-voltage embedded SRAM design is extremely essential for power efficient mobile video applications. In this thesis, this kind of SRAM is designed for reference frame buffer SRAM, shown as highlight block in Figure 3, which is considered as high priority.

2.2. Video Data Characteristics

A color image require at least three numbers per pixel position to accurately represent color [14]. Since the human visual system (HVS) is more sensitive to luminance (brightness) than to color, YCrCb color space is a more efficient way to compress a color image than RGB color space.

And it is becoming more popular in image compression technology, especially in mobile device application.

In YCrCb color space, Y represents the luminance component; Cr means red chrominance component; Cb stands for blue chrominance component. As mentioned before, Cr and Cb components (chroma) is represented with a lower resolution than Y component (luma) based on HVS. Hence, the amount of chroma data is required to be reduced in image compression. And to a casual observer, there is no obvious difference between an RGB image and a YCrCb image with reduced chroma resolution [14].

In various YCrCb sampling formats, 4:2:0 sampling format is widely used for video conferencing, digital television and video streaming system for mobile devices. For every Y/Cr/Cb, 8 bits data are used to represent the brightness/color information as shown in Figure 4. Previous research only considers luma factor in memory design [9,10]. However, ignoring the memory failure impact on chroma may induce over-optimization and lose power saving opportunities. In the proposed SPIDER, the contribution of both luma and chroma factors is considered to the output quality while optimizing the application-driven memory.

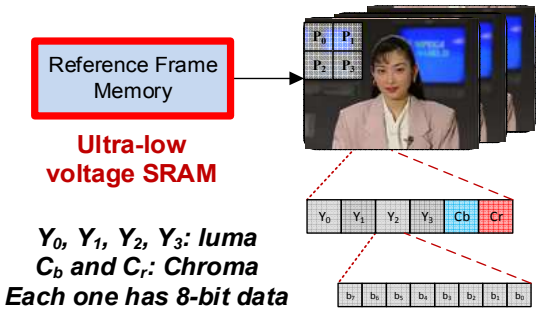


Figure 4. Video data storage in proposed SRAM

2.3. Video Quality Evaluation

The perception of a visual scene is formed by a complex interaction of HVS. Visual quality measurement therefore is influenced by many factors, such as viewing environment, visual attention, etc. And it is very difficult to be accurately and quantitatively measured.

Objective quality measurement is much more attractive to the developers of video codec processing systems than subjective quality measurement, because it is able to measure quality automatically using an algorithm. The most widely used objective quality measurement is Peak Signal to Noise Ratio (PSNR), though it has many limitations compared with the real response from human observers.

PSNR depends on the mean squared error (MSE) between an original and an impaired video frame. PSNR is defined as [13]

$$PSNR = 20\ log_{10}\left(\frac{255}{\sqrt{MSE}}\right) \tag{2.1}$$

And MSE is expressed in equation (2.2), where Y_{Org} is the data from original video, and Y_{Deg} is the degraded video data.

$$MSE = \frac{1}{mn}\sum_{i=0}^{m-1}\sum_{j=0}^{n-1}\left[Y_{Org}(i,j) - Y_{Deg}(i,j)\right]^2 \tag{2.2}$$

If both luma and chroma data are considered in video frames, the overall PSNR can be calculated as

$$PSNR = \frac{1}{8}(6PSNR_Y + PSNR_{Cr} + PSNR_{Cb}) \tag{2.3}$$

2.4. Overview

In order to increase the reliability of the video output in a mobile device, the proposed low-power embedded SRAM is designed for reference-frame storage of video decoding processes. H.264 based video decoder is currently popular for its better compression efficiency. However,

due to the inter and intra prediction processes, it is difficult to build a fixed relation between the memory bit-failure and video output/quality. Thus, a relatively precise PSNR-based estimate algorithm is extremely essential for a sizing-priority SRAM design.

CHAPTER 3. LOW-POWER SRAM MODEL

3.1. Power Consumption Sources

There are four sources of power dissipation in conventional digital CMOS circuits. As equation (3.1) shows below, the total power consumption P_t is composed of switching power consumption P_{sw}, short-circuit power consumption P_{sc}, leakage power consumption P_{lk}, and static power consumption P_{st}.

$$P_t = P_{sw} + P_{sc} + P_{lk} + P_{st} \tag{3.1}$$

(1) Switching Power Consumption

Currently, switching consumption is the most significant component of the total power dissipation in ICs. It comes from the load capacitance charging from 0 to power supply. Equation (3.2) shows the mathematically determination.

$$P_{sw} = C_L {V_{dd}}^2 f \tag{3.2}$$

where C_L is the load capacitance; f is the switching activities. From this equation, it is obvious that V_{dd} is the most influential term.

(2) Short-circuit Power Consumption

Due to the finite rise/fall time for both transistors in CMOS, both NMOS and PMOS will be partially conductive synchronously for a short period of time during switching, which causes a direct current to flow from V_{dd} to ground. This short-circuit power dissipation is significant when the rise/fall time at the input of gate is much longer than the output rise/fall time. On the other hand, when the output rise/fall time is too long, the circuit will be slowed down, and it may cause short-circuit current in the fanout gates. Hence, a sequential of gates each with nearly equal input and output edge times is required to minimize the total average short-circuit current in a cell chain.

(3) Leakage Power Consumption

Leakage power is primarily considered in products which spend most of operating time in standby mode. Reverse-bias diode leakage at transistor drains and sub-threshold leakage through the channel of an "off" device are the two main types of leakage currents. From Figure 5, it is predicted that leakage power dissipation will exceed dynamic power dissipation for many chips/devices in the near future [1].

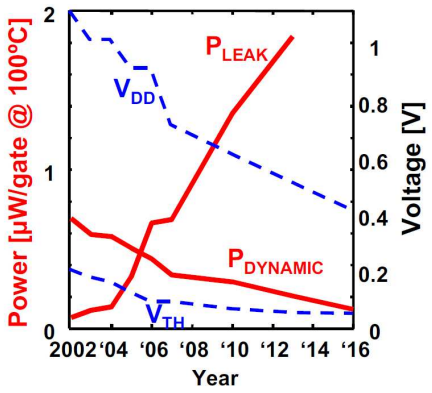


Figure 5. Estimated voltage and power trend [1]

Equation (3.3) describes the leakage power P_{lk}.

$$P_{lk} = e^{-qV_{th}/KT} \tag{3.3}$$

where V_{th} is the transistors threshold; T is the temperature. Leakage power consumption has an exponential dependence on temperature which is directly affected by V_{dd}. That means that lowering the supply voltage reduces the amount of heat, and then the leakage power consumption.

(4) Static Power Consumption

In order to prevent an abnormal short circuit, CMOS, conventionally, does not produce static power. However, there are some special circuits, such as reduced voltage level feeding into

complementary static gates and pseudo NMOS/PMOS circuit styles, in which circuits dissipate power in steady state operation.

In summary, both switching power and short-circuit power are called dynamic power, because they are dissipated only during switching events. Leakage power and static power are called static power. They are consumed during holding or maintaining periods.

Amount these four type of power consumption sources, switching power is currently the most important part of the total power. However, leakage power is estimated to be a new top power dissipation part in the near future. And both of them are seriously influenced by supply voltage. Therefore, scaling down V_{dd} is one of common methods for power dissipation decrease.

3.2. Related Work

Significant amount of research on low-power mobile video techniques has been reported in the literature. Low-power memory can be broadly classified into two different categries.

3.2.1. General-Purpose Memory Used For Mobile Video Applications

Many solutions are developed to lower the power consumption of memory utilizing assist schemes such as adjustment of cell voltage [15], boosted wordline voltage [16,17], dual-rail supply schemes [18], negative bitline schemes [19,20], and read-modify-write or write-back schemes [21,22]. The improvements in power efficiency are often achieved with significant design complexity and power penalty for voltage regulations or boosting circuits.

Most existing solutions adopt more than 6T to achieve low power operation, such as asymmetric 7T cell [23], single-ended read-decoupled 8T cells [24,25], Zigzag 8T cells [26], read-disturb-free 9T [27] and 10T SRAM cells [28], and bit-interleaving 12T cells [29]. However, the developed memory cells still suffer the write half-select disturb problem, limiting the power efficiency that can be achieved. Most importantly, all of these general-purpose memory designs

fail to consider the context of the target video applications, thereby losing potential power saving opportunities.

3.2.2. Mobile Video Specific Memory

Several recent efforts have explored mobile video memory design with attempts to consider simple application-specific properties, such as data patterns [3] and contributions of different data bits [10,11,21]. Many mobile video SRAM designs have been presented for low power consumption. In [9] and [13], hybrid 6T+8T and 8T+10T SRAM structures were presented to achieve quality-area optimization. However, such hybrid structures increase the implementation complexity of peripheral circuitries such as memory decoders. In [10], a heterogeneous sizing scheme was presented to reduce the failure probability of conventional 6T bit-cells, but it suffers from large area overhead and can only achieve 0.9 V operation supply, limiting the power efficiency. In [11], ECC approach is proposed to reduce the area overhead of 8T bit-cells, but it suffers from a performance penalty for data encoding/decoding and area overhead for both ECC circuitry and redundancy data. Also, all of those techniques ignore Chroma data and they may lose optimization opportunities.

The common feature of the above exisiting techniques is that the power savings comes at a cost of large area overhead. In contrast, SPIDER realizes significant power savings with reduced area overhead and considers both luma and chroma in area-priority and quality-priority mobile video applications simultaneously.

3.3. Proposed SRAM Model and Reliability Analysis

Figure 6 shows the schematic of 6T SRAM bit-cell. In low-voltage operation with process variation, the worst process corners for 6T SRAM are “Fast-NMOS and Slow-PMOS” (FS) at reading operation and “Slow-NMOS and Fast-PMOS” (SF) at writing operation [9,10,13]. Since

the read failure rate at FS corner ($P_{RF}(FS)$) is much larger than the write failure rate at SF corner ($P_{WF}(SF)$), the overall 6T SRAM cell failure rate (P_F) can be estimated as the read failure rate in the FS process corner as equation (3.4) expressed:

$$P_F = P_{RF}(FS) + P_{WF}(SF) \cong P_{RF}(FS) \tag{3.4}$$

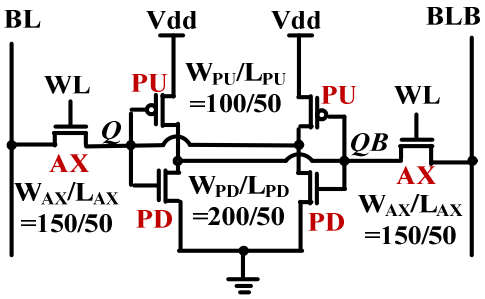


Figure 6. Standard 6T SRAM (WPU:WPD:WAX=1:2:1.5)

Researchers have shown that the failure rate of SRAM bit-cells decrease with larger transistor size and they increase all 6T transistors to reduce the failure rate [10]. In order to ensure the size of the memory is increased efficiently, failure characteristics in memory are discussed based on extensive SPICE Monte Carlo simulations. During the case discussion, it is assumed that the width and length of each transistor are varied simultaneously so that the sizing ratio of each device is kept the same. The following is the four considered sizing cases:

CASE I: to increase sizes of all 6 transistors simultaneously;

CASE II: to increase sizes of two pull-down NMOS transistors (PD);

CASE III: to increase sizes of two access NMOS transistors (AX);

CASE IV: to increase sizes of two pull-up PMOS transistors (PU).

The results are shown in Table 1, in which x% means both width and length of devices are increased by x% at the same time. As observed, if only two PMOS transistors (PUs) are increased

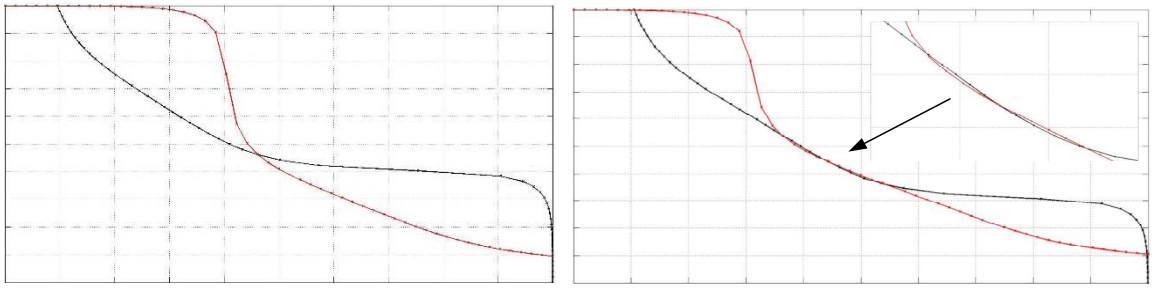
in size, the failure rate is growing. This is because, larger pull-up transistors make the reading process even more difficult. It should be noted from Table 1 that, increasing all 6T transistors in prior work cannot optimize the failure rate but induces large area overhead. However, the failure rate is minimized by increasing two pull-down NMOS access transistors (AXs). As the size of access transistors are increased by 50%, the failure rate is sharply reduced from 1335/10,000 to 3/10,000. Therefore, case III will be utilized in proposed SRAM model, and all the following analysis and discussion will depend on it.

Table 1. Sizing dependent SRAM failure characteristics

	Failure Rate (/10, 000), V_{dd} = 0.5 V					
CASE	basic	10%	20%	30%	40%	50%
I: All-6T [9]	1335	718	463	336	259	211
II: Only-PD	1335	970	870	477	457	403
III: Only-AX	**1335**	**216**	**57**	**39**	**4**	**3**
IV: Only-PU	1335	3326	4891	6018	6817	7386

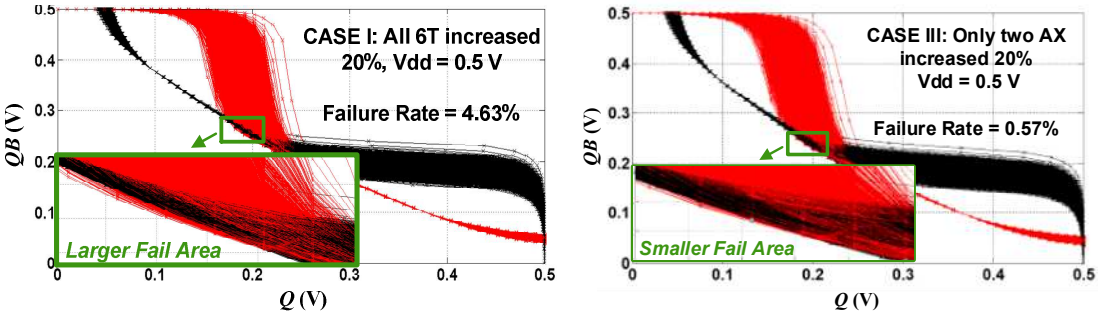
Static Noise Margin (SNM) in an SRAM cell is the minimum dc disturbance voltage present in logic gates at which the status of the memory flips [30]. Worst-case SNM can be geometrically defined by butterfly curve as the maximum square between the normal and mirrored transfer characteristic. The length of the square edge represents the reliability of an SRAM cell, the longer square edge is the more reliable the SRAM cell is. Furthermore, SRAM cell is disturbed by static noisy more easily in reading mode than in writing mode. Thus, the maximum square between the normal and mirrored transfer characteristic in reading mode usually indicates the SNM of an SRAM cell.

Figure 7(a) shows normal butterfly curves while reading successfully, in which there are three intersection points. When the SRAM cell reads failed, the intersection points will be less or more than three, shown in Figure 7(b). Case I and case III are simulated by Monte Carlo method in reading mode. And the results are presented in Figure 8(a) and (b). As shown, the abnormal curves in case I is more than those in case III. That means the failure rate in case III is smaller. Accordingly, in SPIDER design, case III sizing methodology is adopted to reduce memory failure with reduced area overhead or better video quality, which will be discussed in chapter 4.



(a) Butterfly curves in correct condition (b) Butterfly curves in failed condition

Figure 7. Butterfly curves in correct and failed conditions



(a) Failure rate in case I (b) Failure rate in case III

Figure 8. Comparison of failure rates in case I and case III

3.4. Overview

Low-power technology is becoming a critical challenge for battery-based streaming media application. Due to the power consumption analysis in conventional digital CMOS circuits, low-voltage method is adopted for proposed SPIDER design. In this SRAM model, “fast-NMOS and slow-PMOS” is taken as the worst process corner. Based on standard 6T SRAM, only two access NMOS transistors will be resized in the following analysis and algorithms discussion for its optimal tradeoff between bit-cell reliability and size overhead. And with SNM-based butterfly curves analysis, it is proved that this method is feasible for sizing-priority SRAM design.

CHAPTER 4. SPIDER ALGORITHM

In order to ensure the high quality of video output under low-voltage operation, SPIDER algorithm optimizes the sizes of an 8-bit SRAM by scaling from more significant bits to less significant bits. Since the bit-cell size at a specific position is selected depending on its failure rate, the video quality (PSNR calculated by equation (2.3)) is required to be estimated by the failure rates of all 8 bits, which makes it possible to evaluate the video quality of different 8-bit combination design. Based on this relation, one area-priory and one quality-priority mobile video applications are then developed by SPIDER algorithm. In the following part, an 8-bit luma/chroma SRAM (byte unit) is considered as a case study.

4.1. Video Quality Evaluation

The increase of SRAM failure rate leads to the degradation of video quality. In a video quality evaluation process, PSNR is a direct function of MSE as equation (2.1) shown. It means that MSE can be utilized to decide the optimal cell sizing since smaller MSE guarantees better video quality (larger PSNR). In decoding processes, MSE of an 8-bit pixel data is the mean square error between the original data and the impaired video data, which is described in equation (4.1).

$$MSE_{pixel} = \left(Y_{Org} - Y_{Deg}\right)^2 \tag{4.1}$$

Y_{Org} is an original 8-bit data. Y_{Deg} is the corresponding degraded 8-bit data. Suppose the most significant bit is bit 7. MSE_{pixel} can be represented by separate bit as

$$MSE_{pixel} = [\sum_{k=0}^{7}(2^k|Y_k|)]^2 \tag{4.2}$$

where Y_k is the difference between the original bit k and the degraded bit k. That means

$$Y_k = \begin{cases} 1 & bit\ k\ flips \\ 0 & bit\ k\ does\ not\ flip \end{cases} \tag{4.3}$$

However, in a sizing priority design algorithm, Y_{Deg}s cannot be obtained due to the complex calculation and the statistic characteristics of bit-cell failures. Therefore, it is extremely necessary to build an estimation of the MSE_{pixel} by separate 8 bit. Assume memory failure coefficient Y_{FR} is a value between 0 and 1, and introduce Y_{FR} into equation (4.2). Then the equation is revised as

$$MSE'_{pixel} \cong [\sum_{k=0}^{7}(2^k Y_{FR})]^2 \tag{4.4}$$

If Y_{FR}s are pre-calculated for different sizing/failure rate conditions, MSE'_{pixel} can be estimated by equation (4.4).

For a specific size of SRAM bit-cell in which the failure rate is f, suppose all 8 bits are with the same size/failure rate. Then, by equation (4.4) MSE'_{pixel} becomes

$$MSE'_{pixel,f} \cong \left[\sum_{k=0}^{7}\left(2^k Y_f\right)\right]^2 = (\sum_{k=0}^{7} 2^k)^2 \cdot {Y_f}^2 = 255^2 \cdot {Y_f}^2 \tag{4.5}$$

where $MSE'_{pixel,f}$ can be achieved by H.264 video decoding simulation. In this decoder, faults are injected in reference frame memory as chapter 2 mentioned. Therefore, for a specific failure rate f, Y_f can be expressed as

$$Y_f = \frac{\sqrt{MSE'_{pixel,f}}}{255} \tag{4.6}$$

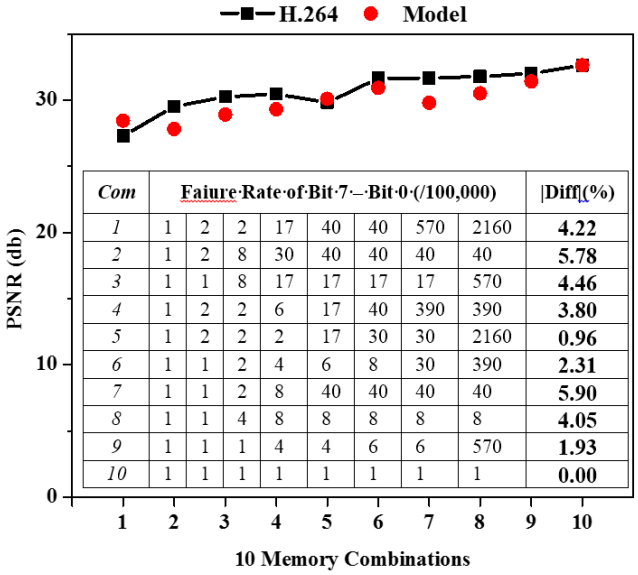
Accordingly, coefficients Y_{FR}s based on different bit-cell sizes can be pre-calculated by equation (4.6) for MSE'_{pixel} and also for PSNR estimation.

For the proposed model in this thesis, memory failure coefficients are simulated and calculated by equation (4.6), and are listed in Table 2.

Based on the Y_{FR}s shown in Table 2, video quality of any 8-bit sizing combination can then be evaluated by equations (4.4) and (2.1). Ten different combinations are randomly selected. Figure 9 compares their calculated PSNRs with their H.264 video simulated PSNRs. As shown, the error rate is less than 6%, demonstrating acceptable accuracy of the developed model.

Table 2. Memory failure coefficients of SPIDER model

L_{AX} (nm)	165	160	150	110	90	80	75	70	65	60	55
W_{AX} (nm)	495	480	450	330	270	240	225	210	195	180	165
Failure Rate %	0.001	0.002	0.004	0.006	0.008	0.017	0.030	0.040	0.390	0.570	2.160
Y_Y	0.0238	0.0298	0.0417	0.0511	0.0591	0.0831	0.1073	0.1260	0.3114	0.3286	0.3548
Y_{Cb}	0.0224	0.0329	0.0461	0.0576	0.0616	0.0923	0.1255	0.1386	0.2746	0.2867	0.3053
Y_{Cr}	0.0219	0.0261	0.0354	0.0477	0.0492	0.0730	0.0982	0.1109	0.2370	0.2491	0.2727



Com	Faiure·Rate·of·Bit·7·–·Bit·0·(/100,000)								|Diff|(%)
1	1	2	2	17	40	40	570	2160	**4.22**
2	1	2	8	30	40	40	40	40	**5.78**
3	1	1	8	17	17	17	17	570	**4.46**
4	1	2	2	6	17	40	390	390	**3.80**
5	1	2	2	2	17	30	30	2160	**0.96**
6	1	1	2	4	6	8	30	390	**2.31**
7	1	1	2	8	40	40	40	40	**5.90**
8	1	1	4	8	8	8	8	8	**4.05**
9	1	1	1	4	4	6	6	570	**1.93**
10	1	1	1	1	1	1	1	1	**0.00**

Figure 9. Comparison of calculated and simulated PSNRs for 10 random combinations

4.2. SPIDER Algorithm

Based on the developed model, SPIDER algorithms are designed and utilized to balance the required overhead size of the proposed SRAM and the output video quality in area-priority and quality-priority applications. The SPIDER sizing optimization problem can be formulated as

follows: Given an application constraint and target supply voltage, determine the size of every memory bit-cell so that the target performance parameter is optimized.

For mobile video embedded memory storing an 8-bit luma/chroma data, the bit-cell size set can be represented as $D_{SPIDER} = <d_7, d_6, d_5, \ldots d_0>$. In the proposed experiment at 500 mV target voltage, the minimum AX of a bit-cell (see Figure 6) is L_{min}/W_{min} = 55 nm/165 nm, and the maximum AX is L_{max}/W_{max} = 165 nm/495 nm. The lenth increases by step of 5 nm which is the minimum permissible grid size for 45-nm technology. To implement SPIDER, a similar look-up table is used based on the approach in [10], which provides the failure rate and silicon area for a specified SRAM bit-cell.

(1) Area-Priority SPIDER Algorithm

The SRAM bit-cell size problem can be considered as a problem of finding a sizing combination ($D_k = <d_7, d_6, d_5, \ldots, d_0>$), which gives rise to the minimum area overhead under a specific PSNR constraint. The procedure for area-priority SPIDER sizing is described in Table 3.

(2) Quality-Priority SPIDER Algorithm

The SRAM bit-cell size problem can be considered as a problem of finding a sizing combination ($D_k = <d_7, d_6, d_5, \ldots, d_0>$), which gives rise to the best output quality under a specific area constraint. Table 4 shows the algorithm pseudo code.

Depending on algorithm 1 and 2, the optimal sizing of the SRAM can be selected for a specific requirement. Compared with reference [10], the proposed algorithms are more precise since they consider the cross terms in equation (4.4). However, what needs to be mentioned is that it is impossible to have an accurate expression for the output PSNR, because the failure bit-flip can induce other bits flip by inter prediction as mentioned in chapter 2.

4.3. Overview

In this chapter, a novel MSE_{pixel} estimation method is proposed. It can be directly used to evaluate the video quality for different sizing combinations. This estimation algorithm is more precise than that in reference [10], which is proved by comparing both calculated and simulated PSNRs from 10 random-selected sizing combinations. Based on this estimation, one area-priory and one quality-priority mobile video applications are then developed by SPIDER algorithm. The experimental results will be given in next chapter.

Table 3. Area-priority SPIDER algorithm

INPUT: Target Output ($PSNR_{target}$), Voltage (V)
Initial: $A = \infty$ //*initial area to cover all possibilities*
for all D_k **do**

$$MSE_{luma} \cong \left[\sum_{i=0}^{7}\left(2^i \cdot Y_{luma,FR_i}\right)\right]^2 \qquad PSNR_{luma} = 20 \cdot \log_{10}\left(\frac{255}{\sqrt{MSE_{luma}}}\right)$$

$$MSE_{Cr} \cong \left[\sum_{i=0}^{7}\left(2^i \cdot Y_{Cr,FR_i}\right)\right]^2 \qquad PSNR_{Cr} = 20 \cdot \log_{10}\left(\frac{255}{\sqrt{MSE_{Cr}}}\right)$$

$$MSE_{Cb} \cong \left[\sum_{i=0}^{7}\left(2^i \cdot Y_{Cb,FR_i}\right)\right]^2 \qquad PSNR_{Cb} = 20 \cdot \log_{10}\left(\frac{255}{\sqrt{MSE_{Cb}}}\right)$$

$PSNR_k = (6PSNR_{luma} + PSNR_{Cr} + PSNR_{Cb})/8$
if $PSNR_k >= PSNR_{target}$ **then**
  if $A > \sum a_i$ **then**
    $A = \sum a_i$
    $D_{opt} = D_k$
OUTPUT: Optimal SRAM cell sizing D_{opt}

Table 4. Quality-priority SPIDER algorithm

INPUT: Target Area (A_{target}), Voltage (V)

Initial: $PSNR = 0$ // *initial output quality to cover all possibilities*

$A_k = \sum a_i$

if $A_k <= A_{target}$ **then**

for all D_k **do**

$$MSE_{luma} \cong \left[\sum_{i=0}^{7} \left(2^i \cdot Y_{luma,FR_i} \right) \right]^2 \qquad PSNR_{luma} = 20 \cdot \log_{10} \left(\frac{255}{\sqrt{MSE_{luma}}} \right)$$

$$MSE_{Cr} \cong \left[\sum_{i=0}^{7} \left(2^i \cdot Y_{Cr,FR_i} \right) \right]^2 \qquad PSNR_{Cr} = 20 \cdot \log_{10} \left(\frac{255}{\sqrt{MSE_{Cr}}} \right)$$

$$MSE_{Cb} \cong \left[\sum_{i=0}^{7} \left(2^i \cdot Y_{Cb,FR_i} \right) \right]^2 \qquad PSNR_{Cb} = 20 \cdot \log_{10} \left(\frac{255}{\sqrt{MSE_{Cb}}} \right)$$

$PSNR_k = (6PSNR_{luma} + PSNR_{Cr} + PSNR_{Cb})/8$

if $PSNR_k > PSNR$, **then**

$PSNR = PSNR_k$,

OUTPUT: Optimal SRAM cell sizing D_{opt}

CHAPTER 5. EXPERIMENTAL RESULTS

5.1. Experimental Methodology

300-frame Akifo colorful CIF video sequence is used to verify the output quality based on the proposed SRAM scheme. The frame size in the simulation is 176×144 pixels. In order to inject memory failure into decoding process, a hardware-based SPIDER simulator is implemented shown in Figure 10. Campared to software-based video coding simulator, such as JM simulation [31], the SPIDER simulator can specifically identify the memory modules and directly inject memory faults, achiving higher precision.

As shown in Figure 10, the SPIDER consists of three components: (1) Python-based controller; (2) HSPICE/Matlab based memory failure analyzer; and (3) Verilog-based H. 264 decoder. The proposed SRAM model is based on NCSU 45nm technology. The working process is detailed as following. In order to distinguish the video quality degradations during the low-voltage operations, 100,000 HSPICE Monte Carlo simulation is firstly performed to obtain the failure probabilities for different SRAM bit-cell sizes with local V_{th} variation in the worst global process corner. For speeding up this large-amount-computation process, Python program is introduced to run HSPICE and MATLAB and change parameters automatically as shown in Figure 10. Then, a H.264 decoder based on Verilog language is implemented, and it randomly injects the memory faults across the reference frame buffer based on the cauculated failure probabilities. Finally, the video frames are captured on the H.264 decoder side.

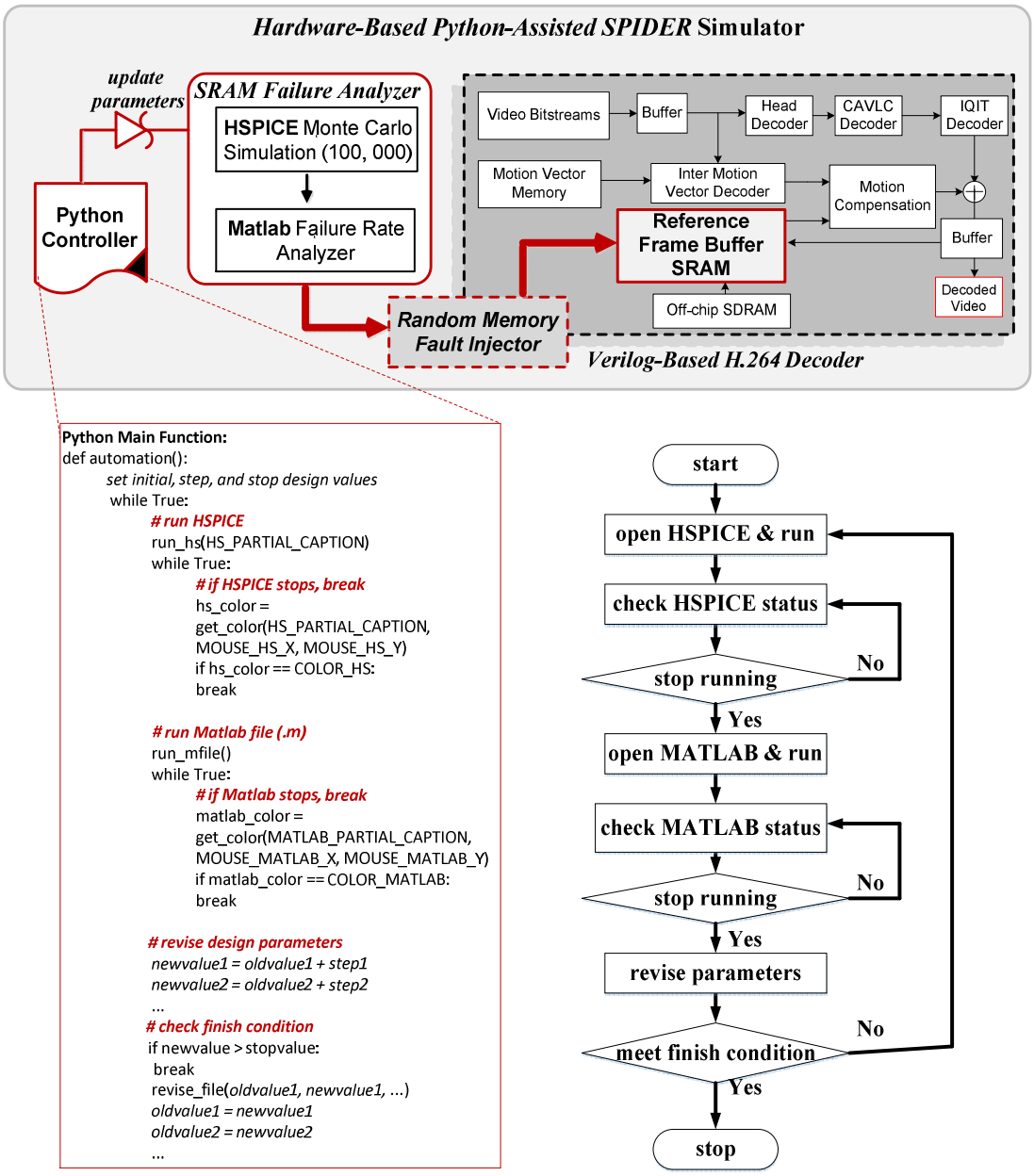


Figure 10. Block diagram of SPIDER simulator and flowchart of Python controller

5.2. Power Consumption Model

Considering both switching and leakage power, the power dissipation of video memory is modeled as:

$$P = P_w + P_r \tag{5.1}$$

where P_w, P_r are the power consumption on write and read operation, respectively. For 8-bit pixel data, the power consumption can be expressed as

$$P_w = \sum_{k=0}^{7} \sum_{\substack{i=0,1 \\ j=0,1}} [F_k(i,j) \cdot P_{wk}(i,j)] \quad (5.2)$$

$$P_r = \sum_{k=0}^{7} \sum_{i=0,1} [F_k(i) \cdot P_{rk}(i)] \quad (5.3)$$

where k is the bit number; i and j are old and new values stored in an SRAM. $F(i,j)$ indicates the bit change (switching) probability from i to j, which is extracted from the video frame in the decoding process.

5.3. Area Priority Application SPIDER

In the implementation, the target PSNR is set as 30.5 dB. Table 5 presents the optimal SRAM bit-cell sizing and failure rate based on only-luma-based optimization and luma-and-chroma-based optimization. In Figure 11, upper one is the memory considering both luma and chroma; bottom one is the memory only considering the luma. It shows that only considering luma during optimization process will induce more area.

Table 5. Optimal SRAM bit-cell sizes and corresponding failure probabilities

	Parameters	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Luma & Chroma	Bit-cell size (W nm /L nm)	495/165	495/165	480/160	270/90	270/90	**240/80**	210/70	210/70
	Area (μm^2)	1.175	1.175	1.147	0.935	0.935	**0.906**	0.874	0.874
	Failure Rate (%)	**0.001**	**0.001**	**0.002**	**0.008**	**0.008**	**0.017**	**0.040**	**0.040**
Only Luma	Bit-cell size (W nm /L nm)	495/165	495/165	480/160	270/90	270/90	**270/90**	210/70	210/70
	Area (μm^2)	1.175	1.175	1.147	0.935	0.935	**0.935**	0.874	0.874
	Failure Rate (%)	**0.001**	**0.001**	**0.002**	**0.008**	**0.008**	**0.008**	**0.040**	**0.040**

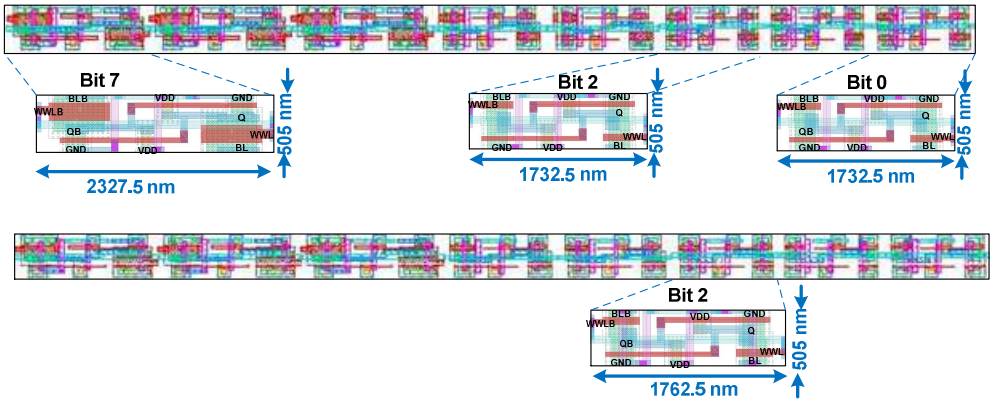


Figure 11. Layout of application-driven memory for 8-bit pixel

Figure 12 shows the comparison of power savings between the proposed memory and conventral memory. Conventional memory worked at 1V V_{dd}; SPIDER algorithms ran on the proposed memory at 0.5V V_{dd}. Area-priority SPIDER was set with $PSNR_{Target}$=30.5 db; quality-priority (50% Area) SPIDER with area constraint as 50% overhead; quality-priority (70% Area) SPIDER with area constraint as 70% overhead. The result shows that 8-bit memory array achieves over 70% power savings with the proposed SPIDER algorithm.

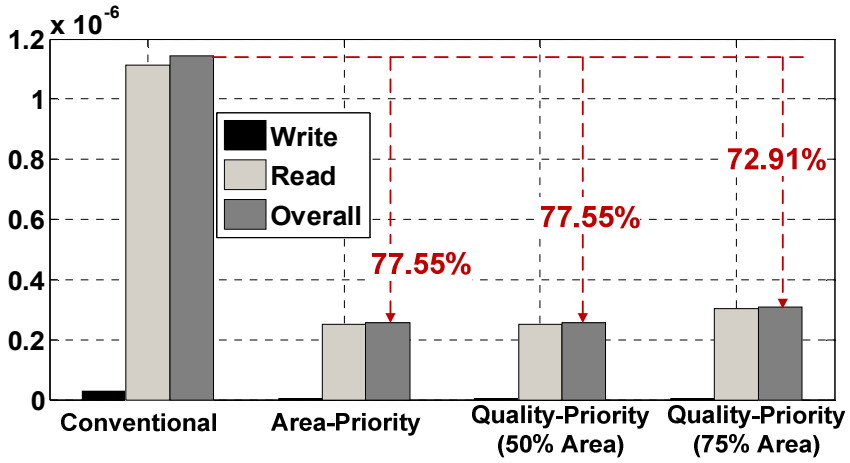


Figure 12. Power savings with SPIDER algorithms

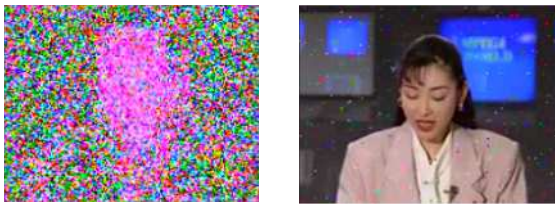
The further performance of SPIDER memory shows that although SPIDER brings performance penalty, the delay time is smaller than 1.271 ns, which is fast enough to support various mobile videos, including high quality videos.

Finally, the video output quality is evaluated base on SPIDER. Figure 13 shows the results of the *Akiyo* clip based on different memory designs. The conventional 6T SRAM results in serious degradation of frame quality worked at 0.5 V V_{dd}, whose *PSNR* is only 9.166. Alternatively, the proposed SPIDER scheme can deliver output quality with less degradation. And the video output is much better while considering both luma and chroma effects.

Figure 13. Output quality for area-priority applications

5.4. Quality Priority Application SPIDER

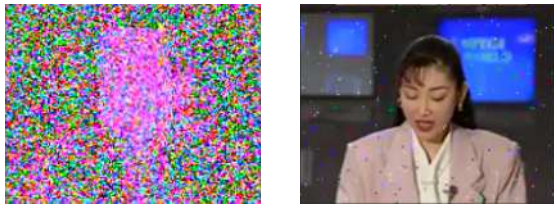
Based on the SPIDER algorithm, mobile video memory is also implemented for quality-priority applications. Figure 14 compares the video output with 50% area constraint based on All-6T sizing methodology [10] shown in Figure 14 (a) and SPIDER methodology shown in Figure 14 (b). With the same area constraint, the proposed SPIDER methodology critically improves the video output quality. As compared to all-6T sizing approach in [10], the *PSNR* is increased from 9.372 to 32.203.



(a) PSNR=9.372 (b) PSNR=32.203

Figure 14. Output quality for quality-priority applications with 50% area constraint

Figure 15 shows the video outputs with 75% area constraint. In this case, the *PSNR* based on developed SPIDER methodology is improved by 1.067. Alternately, the *PSNR* based on All-6T methodology [10] does not show obvious improvement. Accordingly, SPIDER achieves larger quality improvement as the area constraint increases.



(a) PSNR=9.603 (b) PSNR=33.270

Figure 15. Output quality for quality-priority applications with 75% area constraint

5.5. Tape-out Circuit Design

In order to test the proposed low-voltage embedded SRAM, a memory chip is designed for tape-out. Whole chip layout is shown in Figure 16, in which logic circuit is shown in Figure 17.

This memory array is shown in Figure 18. It consists of 64 bytes, including 16 bytes of area-priority sizing combination (FR: 1 1 1 8 8 40 40 40), 16 bytes of quality-priority sizing combination with 50% area overhead (FR: 1 1 1 8 17 30 40 40), 16 bytes of quality-priority sizing combination with 75% area overhead (FR: 1 1 1 1 1 1 1 2), and 16 bytes of original-size combination (L_{AX}=50nm, W_{AX}=150nm). The first three combinations share low-voltage supply;

and the last one uses normal V_{dd}. An example of one bit-cell layout is designed as shown in Figure 19. And an example of one byte SRAM layout is shown in Figure 20. Access transistor sizes of different bits in a byte may differ depending on the expected failure rates.

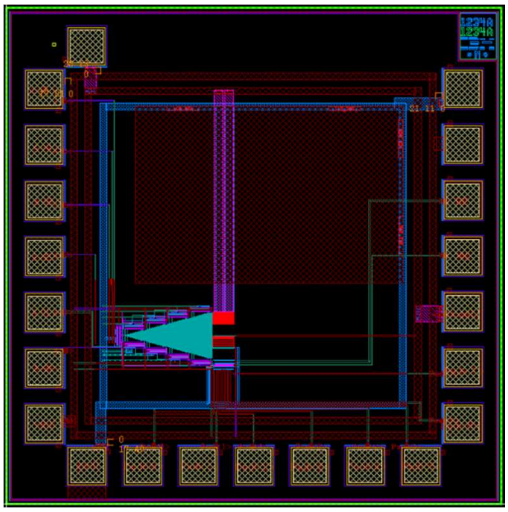


Figure 16. Whole chip layout

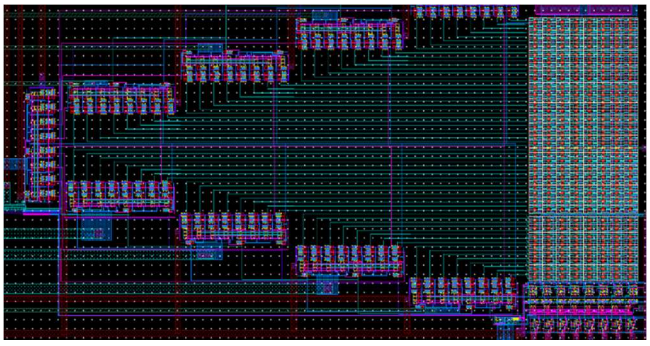


Figure 17. Logic circuit layout

By testing this chip, the power consumption of each sizing combination could be calculated in practical application, which will be a powerful verification for the proposed SPIDER methodology.

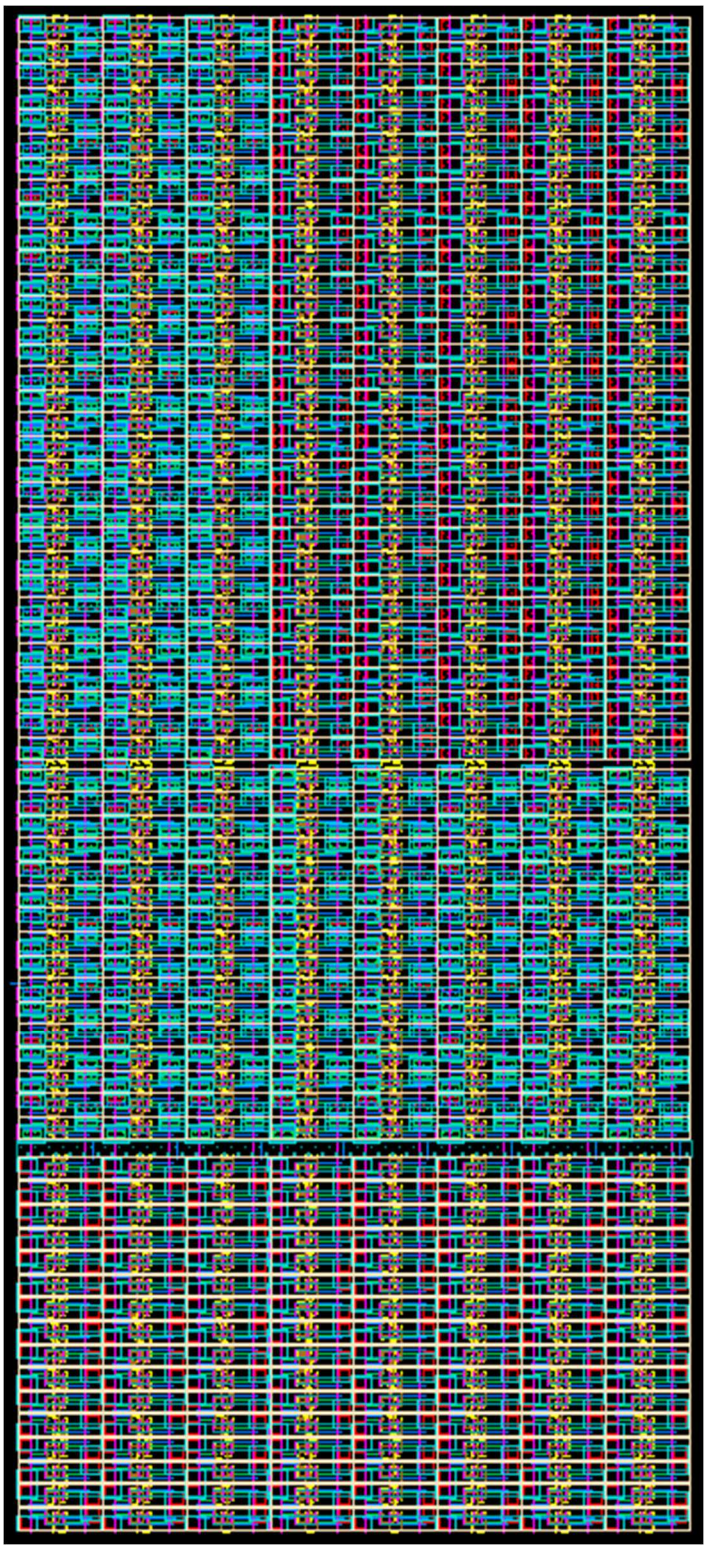


Figure 18. SRAM component layout

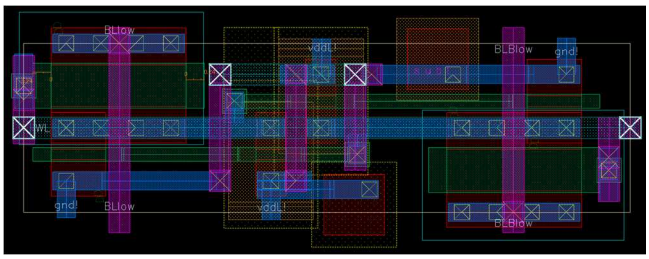


Figure 19. Bit-cell layout

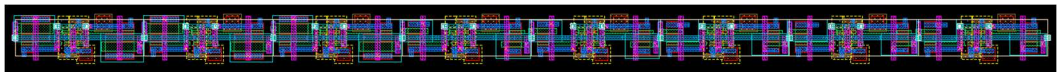


Figure 20. 8-bit SRAM layout

5.6. Overview

Akifo colorful CIF video sequence with 300 frames is used to verify the output quality of the proposed SRAM scheme. In area priority application, the sizing comparison of only-luma-based optimization and luma-and-chroma-based optimization points that only considering luma will induce more area overhead. From the power savings analysis, it outstandingly shows that over 70% power is saved with the proposed SPIDER. And then the output video quality (PSNRs) in both area-priority and quality-priority applications are represented compared with conventional video quality. It is proved that the proposed SPIDER design methodology for low-voltage application is a feasible and efficient compromise between the memory reliability and area overhead.

The chip tape-out design is also presented. Four different sizing combinations are built for power consumption tests. This chip will be very helpful for further verification of the proposed SPIDER methodology.

CHAPTER 6. CONCLUSION

6.1. Conclusion

In order to solve the power dissipation problem in battery-based streaming media applications, this thesis presents an embedded application-driven SRAM used as reference frame memory in a H.264 decoder. To mitigate memory failure at low-voltage supply, this SRAM design adopts a sizing-priority technique, in which only two access NMOS transistors in every 6T SRAM bit-cell are resized, because this is an optimal trade-off between bit-cell reliability and size overhead. Since bit failure rate which is decided by the memory sizing cannot be used to precisely calculate the video quality PSNR, a novel MSE_{pixel} estimation method is developed to directly evaluate the video quality for every 8-bit sizing combination. Based on this low-error-rate estimation, one area-priory and one quality-priority mobile video applications are then proposed by SPIDER algorithms.

Based on Akifo colorful CIF video sequence with 300 frames, simulation results demonstrate that both luma and chroma data should be considered in sizing optimization algorithms. And based on both area-priority and quality-priority SPIDER algorithms, more than 70% power is saved in memory units. And the output videoes have quite higher quality than those in conventional memory. It is proved that the proposed SPIDER design methodology for low-voltage application is a feasible and efficient trade-off between the memory reliability and area overhead.

Besides, a sample SRAM chip with four different sizing combinations and related peripheral circuits is designed for future power consumption hardware tests. This chip has been sent to MOSIS Integrated Circuit Fabrication Service for tape-out. It will be very helpful for further verification of the proposed SPIDER methodology.

6.2. Future Work

Although the proposed SPIDER methodology is verified by simulation and achieve expected results, there are several issues that need to be improved in future work.

- The area-priority and quality-priority SPRIDER algorithms are all performed by brute-force search algorithm. It requires a huge computation overhead since it needs to compute all of the optimal sizing combinations. A more efficient algorithm, such as dynamic programming approach, should be developed to guarantee the SRAM sizing process has a reasonable time complexity.
- Hardware experiment tests are also essential for practical applications. Thus, hardware tests should be implemented based on designed memory chip, whose results will be more powerful for the SPIDER design methodology verification.

CHEPTER 7. OTHER CONTRIBUTIONS: WECS DESIGN FOR WIND TURBINE

7.1. Introduction

Variable-speed wind generation systems make it possible to extract the maximum energy from wind with widely varying speeds. The permanent magnet synchronous generators (PMSGs) are suitable for small variable-speed wind turbine generator systems. The wind generation system with a PMSG represents one important trend of wind power applications with numerous advantages, such as higher efficiency due to the absence of field copper loss, lower operating speed due to higher number of poles with smaller pole pitch, and the elimination of gearbox [32,33]. Smaller wind turbines use fixed pitch angle without the need for additional pitch control. The power from the wind energy conversion system (WECS) is normally fed to an AC grid.

Like other variable-speed wind power system, it is desirable to extract the maximum available power at a given wind speed. There are different methods used to extract the maximum power from the wind. Different control concepts for maximum power point tracking (MPPT) in WECS with PMSG are described and the performance for each is compared in [34]. The MPPT methods can be broadly classified as those which use sensors and those which do not use sensors. They are also classified based on the type of control, such as fuzzy logic based control [35] and sliding mode control [36].

To convert the variable-frequency output voltage from the PMSG into an AC voltage of the grid frequency (60Hz), two typical power converter topologies for small wind turbine systems with PMSG are presented and explained in [37]. The first configuration uses a diode-bridge rectifier, a boost converter and an inverter; and the second configuration uses a back-to-back

converter system. The MPPT is implemented on the DC-DC converter in the former system and on the PWM inverter in the latter one. In the DC-DC converter, the duty cycle is controlled, and in the PWM inverter the modulation index is controlled for MPPT. An input-output feedback linearization (IOL) technique is applied to design the high-performance nonlinear current controller on the PWM rectifier in [38]. A sensorless MPPT control strategy on the PWM inverter is implemented in [39], which is achieved without a wind speed sensor and mechanical sensors such as rotor speed sensor and position sensor. A new variable-speed WECS with a PMSG and Z-source inverter is proposed in [40]. Compared to the conventional WECS with boost converter, the number of semiconductor switches used in [40] is reduced by one and the system reliability is improved. Another nonlinear approach for MPPT is also presented in [41]. It uses a matrix converter, and the controller is based on the nonlinear adaptive backstepping method which is able to effectively accommodate the effects of system uncertainties.

This section proposes an MPPT scheme for a WECS with a PMSG. The major advantage of using a PMSG is its ability to handle a wide range of rotor speeds which correspond to a large range of wind speeds. In a PMSG, the frequency and amplitude of the output voltage change with wind speed varying. In order to maintain a narrow range of DC link voltage, the proposed wind generation system uses a DC-DC converter with buck-boost feature which can step up or step down the rectified voltage by controlling its duty cycle. Also, in the PWM inverter, another closed-loop is designed to accurately track the maximum power point by shifting the phase angle of the output voltage with respect to that of the grid voltage.

7.2. Description of the WECS Set Up

The functional block diagram of the proposed wind energy MPPT system is shown in Figure 21. The wind speed measured using an anemometer is utilized to compute the maximum

power P_{max}* which is used as the reference for the outer power control loop. While extracting maximum power, the wind turbine runs the PMSG at the optimum speed ω_m. The three-phase variable frequency output voltage from the PMSG is rectified using a three-phase diode rectifier and fed as the input to the buck-boost DC to DC converter. At any wind speed, the output voltage of the buck-boost converter V_{dc} can be regulated at a constant level by controlling the duty cycle of the active switch through a PI controller as shown in Figure 21. The reference voltage V_{dcref} is chosen to match the output of the PWM inverter which will be the grid voltage. The use of a buck-boost converter allows the WECS to operate over a wide range of wind speeds (very low to very high) but within permissible limits.

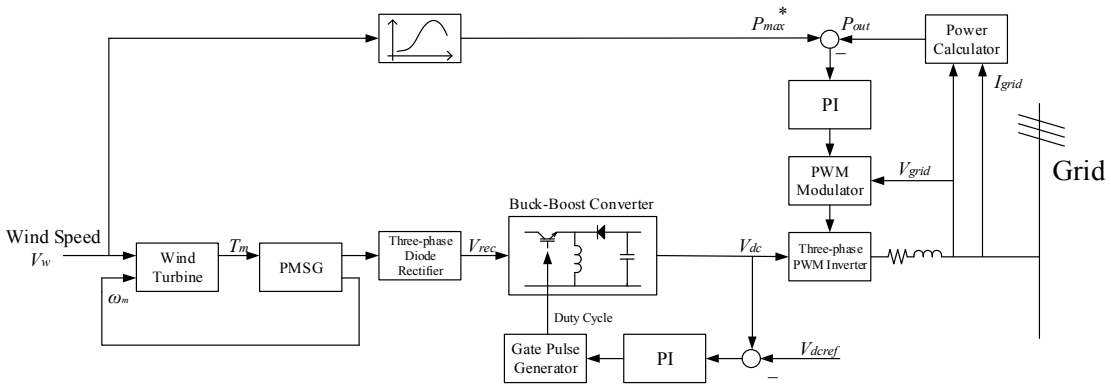


Figure 21. Block diagram of proposed MPPT system

The output of the buck-boost converter is fed to the PWM inverter whose reference sine input is taken from the grid. Keeping the modulation index constant, the phase of the inverter output voltage can be shifted using a feedback loop. This is done by comparing the reference power P_{max}* and the real power that is fed to the grid. A second PI controller modifies the angle between the grid voltage and corresponding current in the same phase. By varying the phase angle, the proposed system can extract maximum power from the wind turbine and supply the grid.

7.3. Mathematical Model

7.3.1. Wind Turbine

The mechanical power output from the wind turbine is given by [32]

$$P_m = \frac{1}{2}\rho A C_p {V_w}^3 \tag{7.1}$$

where ρ is the air density, A is the sweep area of the turbine blades, V_w is wind speed, C_p is the aerodynamic power coefficient which is a function of the pitch angle β and the tip speed ratio λ. Since ρ and A are constant parameters, the wind turbine can produce maximum power under a certain wind speed only when the turbine operates at the maximum C_p. One generic equation is used to express C_p. This equation, based on the turbine characteristics of [42], is given by

$$C_p(\lambda, \beta) = C_1 \left(\frac{C_2}{\lambda_i} - C_3\beta - C_4\right) e^{\frac{-C_5}{\lambda_i}} + C_6\lambda \tag{7.2}$$

with

$$\frac{1}{\lambda_i} = \frac{1}{\lambda + 0.08\beta} - \frac{0.035}{\beta^3 + 1} \tag{7.3}$$

where β is blade pitch angle, and λ is defined by

$$\lambda = \frac{\omega_m R}{V_w} \tag{7.4}$$

In equation (7.4), ω_m is the turbine angular velocity and R is the turbine radius. In small wind turbine generation systems, β is rarely changed.

Figure 22 shows the C_p-λ curve described by equation (7.2) for the proposed wind turbine. From Figure 22 and the definition of λ, at a specific wind speed, there is a unique wind turbine shaft speed to achieve the maximum power coefficient C_{pmax}. When C_p is controlled to be at its maximum value, the maximum mechanical power is extracted from the wind energy at any wind speed.

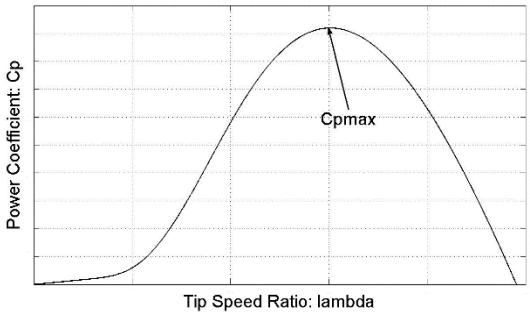


Figure 22. *Cp*-λ curve of the wind turbine

7.3.2. PMSG

The steady-state-induced voltage and torque equations of a PMSG are given by

$$T_e = K_t I \tag{7.5}$$

$$E = K_e \omega_m \tag{7.6}$$

The mechanical characteristics of the PMSG can be described by

$$\frac{d}{dt}\omega_m = \frac{1}{J}(T_m - T_e - F\omega_m) \tag{7.7}$$

where J is combined inertia of the rotor and load, T_m is the mechanical torque input from the wind turbine, T_e is electromagnetic torque, and F is the combined viscous friction of the rotor and load.

In the simulation, an alternate model for the PMSG is used. For this, the output voltage of the PMSG at any given speed and output current is obtained from the experimental characteristics. Figure 23 shows the illustrative characteristics of the phase voltage as a function of load current at different speeds. The drop in the speed with load current represents the internal drop of the PMSG which is partly due to the winding impedance. The per-phase output voltage is given by

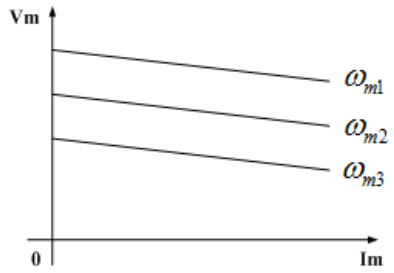


Figure 23. Illustrative characteristics of phase voltage and load current at different speeds

$$V_m = K_1\omega_r - K_2 I_m \tag{7.8}$$

where K_1 is a constant for the PMSG calculated from the experimental characteristics, K_2 is the equivalent impedance constant, and I_m is the amplitude of the sinusoidal current drawn from the PMSG. The *rms* value of the line-line voltage from the PMSG is given by

$$V_{llrms} = \frac{\sqrt{3}}{\sqrt{2}} V_m \tag{7.9}$$

7.3.3. Diode rectifier

The output from the PMSG is rectified using a three-phase rectifier whose output voltage V_{rec} is given by [43].

$$V_{rec} = \frac{3\sqrt{2}}{\pi} V_{llrms} \tag{7.10}$$

If the losses of diodes are ignored, diode rectifier does not change the power. It is only used to convert AC to DC.

7.3.4. Buck-boost Converter

The rectified voltage V_{rec} is stepped up/down by the buck-boost converter (shown in Figure 24), whose output voltage V_{dc} and output current I_{dc} are given respectively by

$$V_{dc} = -\frac{D}{1-D} V_{rec} \tag{7.11}$$

$$I_{dc} = \frac{1-D}{D} I_{rec} \tag{7.12}$$

where *D* is the duty cycle. The inductor is designed to have continuous current. From the above expression, it can be seen that the polarity of the output voltage is always negative as the duty cycle goes from 0 to 1. Apart from the polarity, this converter is capable of operating at either step-up mode (as a boost converter) or step-down mode (as a buck converter). In order to obtain a constant DC output voltage, the difference between the desired output voltage and the actual output voltage is used to adjust the duty cycle of the buck-boost converter under different wind speeds. It is worth noting that buck-boost converter maintains a constant power like other DC to DC converter, when the losses are neglected.

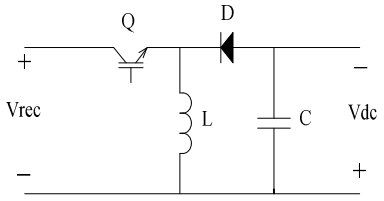


Figure 24. Power circuit of buck-boost converter

7.3.5. PWM Phase shift Control

The buck-boost converter with the voltage control loop supplies a constant DC voltage to the three-phase PWM inverter as shown in Figure 25.

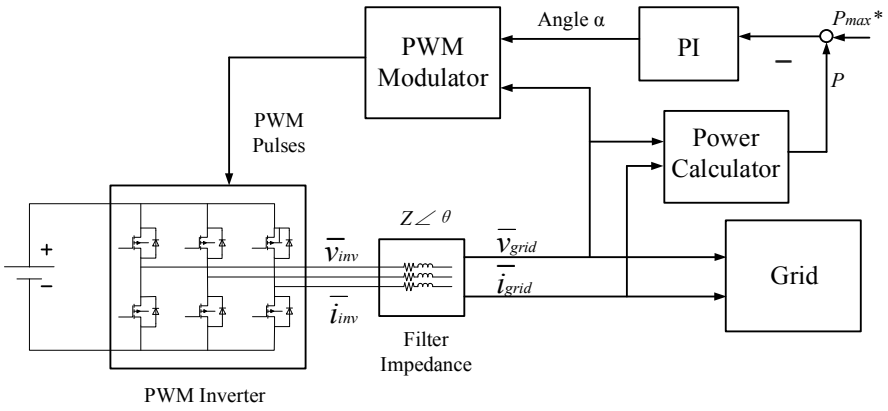


Figure 25. Block diagram of PWM phase-shift controller

The PWM inverter converts a DC voltage into a three-phase AC voltage which is applied to the grid through smoothing inductors including their parasitic resistors. The currents flowing into the grid along with the inverter output voltages are measured for actual power calculation. In order to have a phase-shift angle with respect to the grid voltage, another PI controller is utilized. The PWM circuit compares the phase-shifted reference sinusoidal wave (obtained from both the grid and the PI controller) and a high-frequency triangular wave with a large frequency modulation index $m_f = f_t/f$ and a nominal amplitude modulation index $m_a = V_{gird}/V_t$ where f_t and V_t are the frequency and amplitude of the triangular wave respectively, and f (60Hz) and V_{grid} are the frequency and amplitude of the phase-shifted reference sine wave from the grid. The PWM inverter provides a three-phase output with voltage $\overline{v}_{inv}$ and current $\overline{i}_{inv}$. The relation between v_{inv} and v_{dc} is given by [43]

$$V_{invllrms} = 0.612 m_a V_{dc} \tag{7.13}$$

where $V_{invllrms}$ is the *rms* value of the line-to-line voltage.

If both the three-phase PMSG and three-phase grid operate under balanced steady-state conditions, and the instantaneous grid terminal voltage in phase A is $\overline{v}_{gridan} = V\angle\delta$ (line-to-neutral

voltage), the equation for $\bar{v}_{invan}$ will be

$$\bar{v}_{invan} = V'\angle(\delta + \alpha) \tag{7.14}$$

where V' is the amplitude of inverter output voltage and α is the phase shift angle provided by the PI controller. According to equation (7.9), if m_a is fixed and V_{dc} is maintained constant, V' will also be constant. If the per-phase impedance of the line filter is $Z\angle\theta$, the current fed to the grid by phase A can be expressed as

$$\bar{\imath}_{grida} = \frac{\bar{v}_{invan} - \bar{v}_{gridan}}{Z\angle\theta} = \frac{V'\angle(\delta+\alpha) - V\angle\delta}{Z\angle\theta} = I\angle\beta \tag{7.15}$$

Under balanced operating conditions, the total power to the grid $P_{3\phi}$ is given by [44]

$$P_{3\phi} = p_{3\phi}(t) = \bar{v}_{gridan}\bar{\imath}_{grida} + \bar{v}_{gridbn}\bar{\imath}_{gridb} + \bar{v}_{gridcn}\bar{\imath}_{gridc} = 3VI\cos(\delta - \beta) \tag{7.16}$$

where $p_{3\phi}(t)$ is the instantaneous power delivered by all three phases.

Equation (7.16) shows that the average power is equal to the total instantaneous power delivered to the grid which can be easily calculated using measured three-phase currents and voltages. In addition, equation (7.16) shows that the actual power is not a function of time, but depends on vectors $\bar{v}_{gridln}$ and $\bar{i}_{grid}$. The phase-shift control strategy varies the phase angle of the inverter output voltage while keeping its amplitude constant at V' (the amplitude of grid voltage). The line impedance in each phase is a constant as well. Besides, δ is the phase angle of grid which cannot be varied. From equations (7.14), (7.15), and (7.16), it is seen that $P_{3\phi}$ can be varied by adjusting the phase-shift angle α.

7.4. MPPT Principle

Optimal operation of the PMSG-based WECS is to extract the maximum power from wind. According to equation (7.1), the maximum power at a given wind speed can be extracted when C_p, which is a function of the pitch angle β and the tip speed ratio λ, is maximum. Since β is fixed, λ

has to be at its optimal value. From equation (7.4), it is seen that λ can be regulated by changing the turbine angular velocity ω_m. Thus, the optimal control of the WECS means that the system has to operate at the optimal value of the rotating speed of the PMSG at different wind speeds.

Figure 26 represents the relation between generator speed and output power for different wind speeds. It is seen that the maximum power output occurs at different rotating speeds for different wind speeds. The role of the MPPT control strategy is to track the maximum power curve shown in Figure 26.

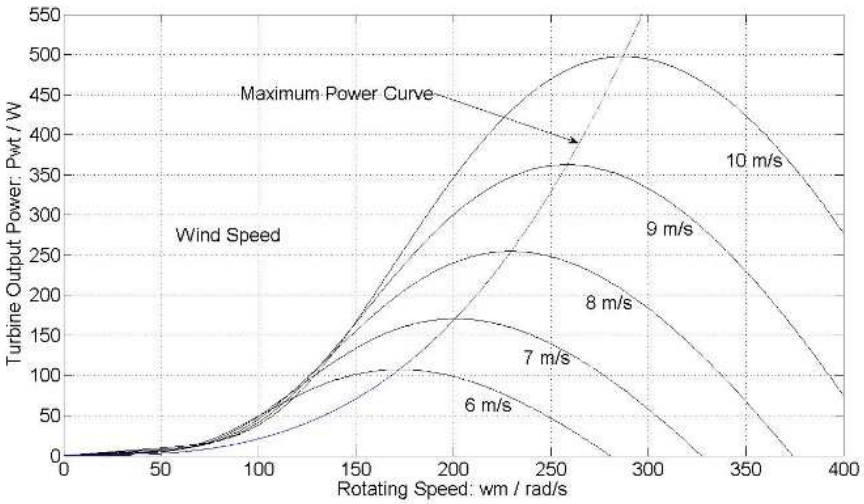


Figure 26. Mechanical power versus rotating speed for different wind speeds

The vector representation of equation (7.15) is shown in Figure 27. Figure 27(a) shows the case without phase-shift control while Figure 27(b) shows the case with phase-shift control. It is obvious that the value of *V-V'* in Figure 27(a) is smaller than that in Figure 27(b). Since *Z* is a constant parameter of the circuit, the output current in the system without phase-shift control is smaller than that of a system with phase-shift control. Initially, if the system operates at a higher

value of ω_m, then P_m* will be higher than the actual power which increases the phase shift. As a result, the output current will increase. And then, the input current of the inverter will also increase because of conservation of energy (neglecting the losses in the inverter). From equation (7.12), the output current of the diode rectifier also increases, which leads to an increase in the PMSG current. Since the PMSG current is proportional to electromagnetic torque T_e, T_e is raised as well. Then the value of $\frac{d\omega_m}{dt}$ decreases as in equation (7.7), which means the PMSG decelerates and settles down at the optimum ω_m which is lower than the initial speed.

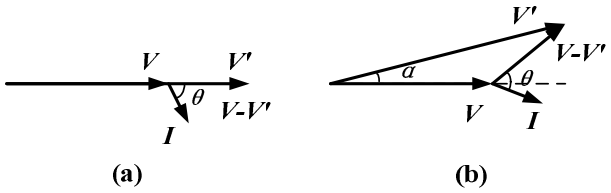


Figure 27. Vector representations of inverter output without and with phase-shift control

7.5. Simulation Results

The model of the PMSG-based variable-speed wind turbine system in Figure 21 is built mainly using Matlab/Simulink dynamic system simulation software, shown in Figure 28, for simulating the behavior of the entire system subjected to wind speed variations. The simulation model is developed for a 500W industrial permanent magnet synchronous alternator. The parameters of the turbine and the PMSG used are given in Table 6. The power converters and both the duty cycle and phase-shift control algorithms are also implemented in the model. The sampling time used for the simulation is 10μs. The wind speed waveform is simulated by TurbSim software based on the data for the state of North Dakota in US published by the Department of Energy's Wind Program and the National Renewable Energy Laboratory (NREL) [45].

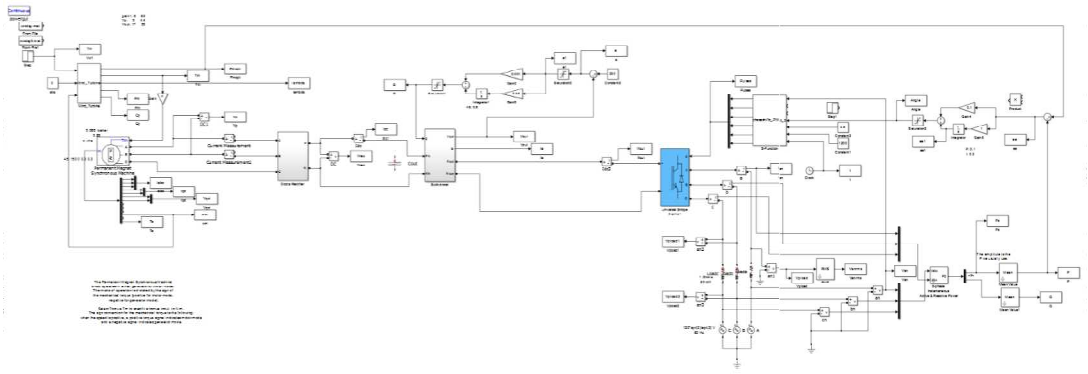


Figure 28. Diagram of wind turbine control system

Table 6. Parameter of the turbine-generator system

WIND TURBINE		
Air Density (ρ)	1.25	kg/m^3
Radius of the Turbine Blades (r)	0.525	m
PMSG		
Rated Voltage, phase	115	V
Rated Output	500	VA
Rated Speed	3428	rpm
Rated Frequency	400	Hz
Stator Phase Resistance (R_s)	1.57	Ω
Inductances ($L_d = L_q$)	3.51	mH
Inertia (J)	0.0008	kg.m^2
Friction Factor (F)	0.00005	N.m.s
Pole Pairs	7	
K_1	0.0353	V/(rad/s)
K_2	1.939	Ω
BUCK-BOOST CONVERTER		
L	5	mH
C	220	μF
PWM MODULATOR		
Amplitude Modulation Index	0.8	
Frequency of Triangular Wave	1200	Hz

The operation of the MPPT scheme for a wind speed profile with step changes is shown in Figure 29 where the wind speed and output power are plotted. Figure 30 shows the variation of rotating speed and the phase-shift angle which is controlled as expected. The sight overshoot in the response of the PMSG's rotating speed ω_m shows that the controller parameters are set properly. From both these responses, it is seen that the phase-shift control system can extract the maximum power from wind even when the wind speed changes sharply.

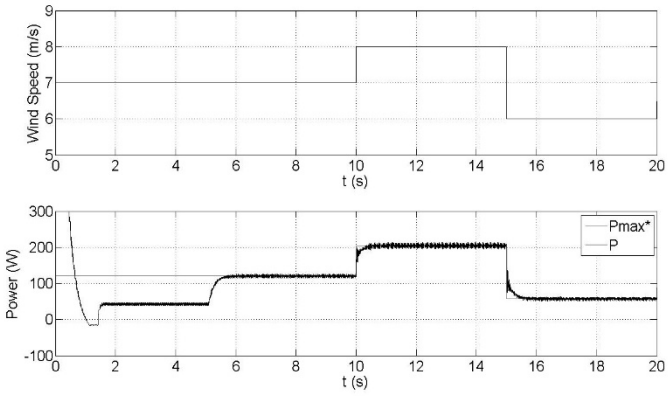


Figure 29. Plot of stepped wind speed profile, maximum power P_{max}* and output power P

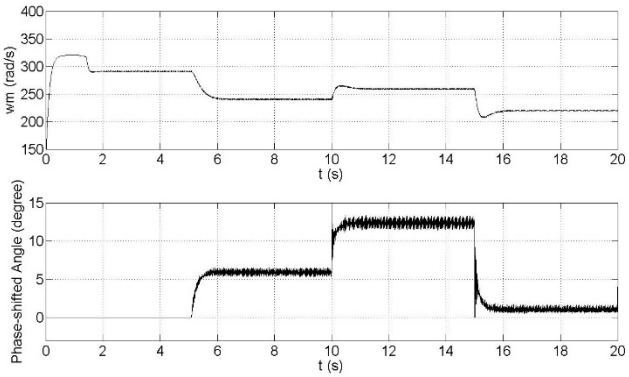


Figure 30. Waveforms of rotating speed of PMSG and phase shift angle

Instead of a stepped wind speed, a variable wind speed is given as a practical one. In order to ensure supplying a constant input voltage (higher than grid voltage) to the phase-shift closed-loop, duty cycle is regulated in buck-boost converter.

Instead of the stepped wind-speed profile, the system is tested with a practical profile. Figure 31 shows the plot of the wind speed profile which is simulated by TurbSim software for the wind speed levels in North Dakota state, the corresponding maximum power P_{max}* calculated from the wind speed, and the actual power P fed to the grid. It is seen that the actual power tracks the maximum power very well in the higher wind speed range. However, some sharp variations are not tracked quite well. That is because of the delay in the phase-shift controller which is found to be somewhat higher when achieving robustness. The whole system could be unstable when there are sharp transitions in the wind speed.

The balancing of the rotating speed and the torque in the PMSG is the key point in MPPT. The torque is varied following the changes in the wind speed. The phase-shift control strategy implements the regulation of the rotating speed ω_m in PMSG by shifting the phase angle which is shown in Figure 32.

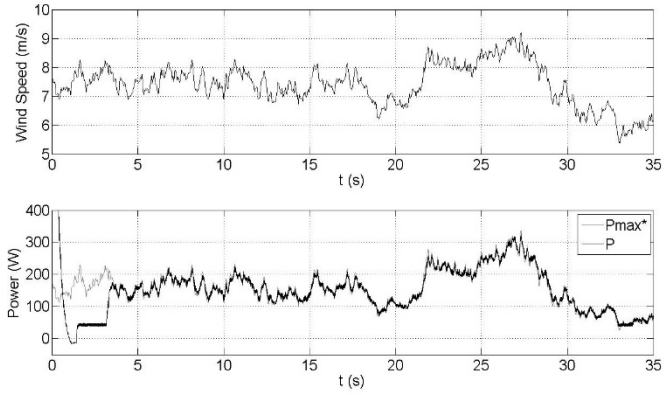


Figure 31. Plot of wind speed profile, maximum power P_{max}* and output power P

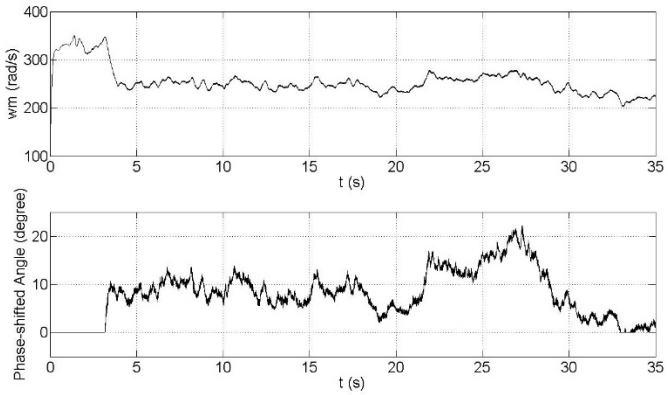


Figure 32. Waveforms of rotating speed of PMSG and phase shift angle

The duty cycle of the buck-boost converter is controlled to give a constant dc link voltage to the grid. In Figure 33, the variation of duty cycle for the wind speed profile of Figure 31 is shown and it stays around 0.57. As a result, the output voltage is kept constant at 250V as shown in Figure 33.

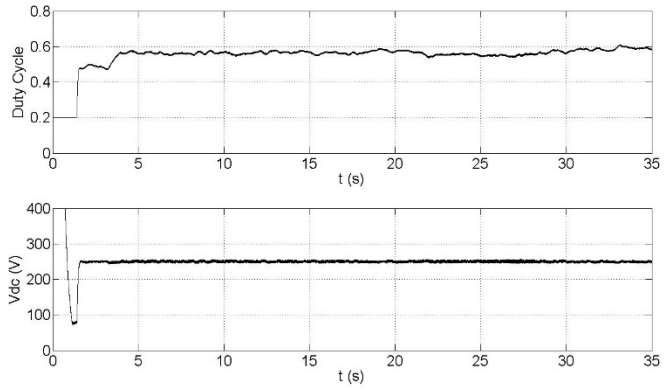


Figure 33. Waveforms of duty cycle and output voltage of buck-boost converter

Figure 34 shows the sinusoidal waveform of output current i_{grid}. Since the grid voltage is supposed to be independent of PMSG output, changing the output current means that the output

power is varied under different wind speeds to match the maximum power. The oscillations in current waveform are the high frequency ripple at triangle wave frequency (1200 Hz). This effect can be further reduced using a low-pass filter.

Figure 35 shows the inverter line-line voltage and the corresponding grid voltage. The inverter output voltage contains discrete pulses caused by the inverter switches and it is clearly seen that there is a phase shift between the two.

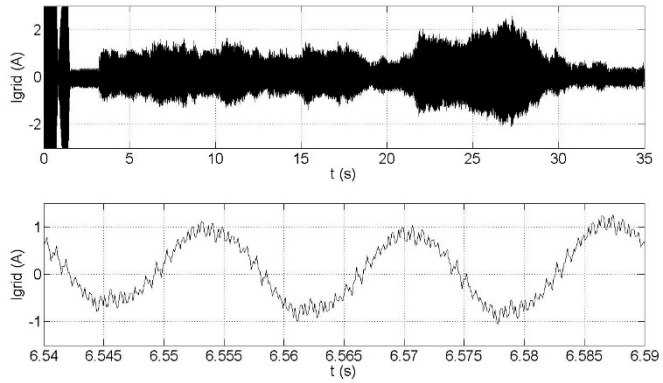


Figure 34. Waveforms of output current (i_{grid}) and the zoom-in plot

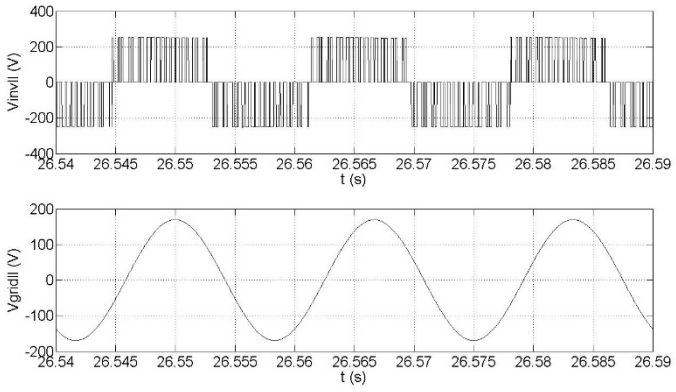


Figure 35. Waveforms of inverter line-line output voltage and grid voltage

7.6. Conclusions

This paper proposes and demonstrates an MPPT strategy for a PMSG-based variable-speed wind turbine generator system. In this strategy, the dc voltage is controlled at a constant value and applied as the input voltage to the inverter by a buck-boost converter under variable wind speeds. Then the phase angle of the ac output voltage is shifted by PWM inverter in order to extract the maximum power from the wind for a wide range wind speeds.

The PMSG is simulated using an approximate model derived from the experimental load characteristics. The feedback control scheme uses a power control loop and feeds power to the grid. The simulation results show that the output power follows the reference wind speed and the computed maximum power. The output current has an acceptable sinusoidal waveform.

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