FINE LINE METALLIZATION

OF SILICON HETEROJUNCTION SOLAR CELLS

VIA COLLIMATED AEROSOL BEAM DIRECT WRITE

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Title

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The Supervisory Committee certifies that this ***disquisition*** complies with North Dakota State University's regulations and meets the accepted standards for the degree of

MASTER OF SCIENCE

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ABSTRACT

Solar energy has come to the forefront as a scalable and largely underutilized renewable energy resource. The current cost of solar electricity, namely from photovoltaics, along with other logistics factors, has prevented the widespread adaptation of the technology. A key determinant of efficiency and cost for a solar cell is the current collector grid. This work presents the Collimated Aerosol Beam Direct Write (CAB-DW) system as a non-contact printing method that can achieve current collector grid finger widths of less than 10 μm which are amenable to decreasing both resistive and optical losses. The ability to produce high aspect ratio grid fingers, and deposit optimized grid structures on high efficiency SHJ solar cells using silver nanoparticle inks is also demonstrated. A decrease in shadowing and via profile modification of the grid fingers is presented, along with a study of aging and degradation of electrical properties within silver nanoparticle inks.

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$\frac{\partial u}{\partial y}$ ..... Gradient of the x component of velocity in the y direction

$\Delta P_{F,\ total}$ ..... Fractional power loss due to the grid finger

A ..... Height dimension of the solar cell

a ..... Unit cell dimension corresponding to finger spacing

A_C ..... Area coverage

a_c ..... Cross-sectional area of the bulk resistivity sample

B ..... Half width of the solar cell

b ..... Unit cell dimension corresponding to finger length

C_S ..... Shadowing coefficient

d ..... Variable pad spacing in TLM structure

FF ..... Fill factor

F_{Sa} ..... Saffman Force

G_t, G_B, G_C ..... Modifying factors for the total series resistance of a unit cell

h_b ..... Average height of the bus bar

h_F ..... Average height of the grid finger

I ..... Current

I_L ..... Light induced current

I_{mf} ..... Maximum current in grid finger of the solar cell

I_{mpp} ..... Maximum power point current

I_{mt} ..... Maximum current in top layer of the solar cell

I_o ..... Reverse saturation current

I_{sc} ..... Short circuit current

J_L ..... Light induced current density

J_{mpp} .....Maximum power point current density

J_{mpps} .....Maximum power point current density as determined by the Suns-V_{oc} system

J_o.....Reverse saturation current density

J_{sc}.....Short circuit current density

k.....Boltzmann's constant

l .....Length of the bulk resistivity sample

L .....Pad width in TLM structure

L_T .....Transfer length

n_{air}.....The index of refraction of air

n_{glass} ..... The index of refraction of glass

P_b ..... Ohmic losses in the bus bar

P_{bS} .....Shadowing losses due to the bus bar

P_C.....Power loss due to contact resistance in the unit cell

P_E.....Power lost in the top layer of a solar cell due to sheet resistance in the unit cell

P_F.....Ohmic power losses in grid finger

P_{FS} ..... Shadowing losses due to the grid finger

$P_{max\ theor.}$ ..... The maximum theoretical power of a solar cell, the product of I_{sc} and V_{oc}

P_{max}.....Power at the maximum power point

$P_{total,\ cell}$ .....Total power generated by the cell without losses

$P_{total,\ unit\text{-}cell}$ .....Total power generated by the unit-cell without losses

q.....The charge of an electron

R.....Measured resistance of the bulk resistivity sample

R_b ..... Resistance of the bus bar

R_C ..... Contact resistance

R_E ..... Resistance of the top layer of the solar cell

R_{ES} ..... Reflectance of the encapsulated substrate

R_F ..... Resistance of the grid finger

R_N ..... Normalized sample reflectance

R_{NE} ..... Normalized sample reflectance after encapsulation

R_s ..... Series resistance in the solar cell

R_{sh} ..... Parasitic shunt resistance

R_{SH} ..... Sheet resistance of the semiconductor layer in the TLM test structure

R_{Sub} ..... Reflectance of the substrate

R_{SW} ..... Reflectance from the swatch sample

R_{SWE} ..... Reflectance of the swatch sample after encapsulation

R_t ..... The total series resistance of a unit cell

R_T ..... Total measured resistance between two pads in the TLM structure

S ..... Spacing between grid fingers

T ..... Absolute temperature

t ..... Thickness of the top cell layer

u ..... Instantaneous gas velocity

u_p ..... Instantaneous particle velocity

V ..... Voltage

V_{mpp} ..... Maximum power point voltage

V_{mpps} ..... Maximum power point voltage as determined by the Suns-V_{oc} system

V_{oc} ..... Open circuit voltage

W ..... Conductive width in the TLM structure

W_b ..... Width of the bus bar

W_b^* ..... Optical busbar width

W_F ..... Width of the grid finger

W_F^* ..... Optical finger width

W_G ..... Geometric line width

W_R ..... Reflective line width

W_O ..... Optical line width

Z ..... Pad height in the TLM structure

α ..... The critical angle of incidence above which total internal reflection occurs

β ..... The critical slope angle required to facilitate total internal reflection

ΔP_b ..... Fractional power loss due to ohmic losses in the bus bar

$\Delta P_{b,\ total}$ ..... Fractional power loss due to the bus bar

ΔP_{bS} ..... Fractional power loss due to shadowing by the bus bar

ΔP_C ..... Fractional power loss due to contact resistance

ΔP_E ..... Fractional power loss due to sheet resistance

ΔP_F ..... Fractional power loss due to ohmic losses in the grid finger

ΔP_{FS} ..... Fractional power loss due to shadowing caused by the grid finger

$\Delta P_{measured}$ ..... Fractional power loss of the solar cell determined experimentally

$\Delta P_{predicted}$ ..... Theoretically predicted fractional power loss

P ..... Bulk resistivity of the top conductive layer of a unit cell

ρ_C ..... Specific contact resistivity

ρ_E ..... Sheet resistivity of top layer of the solar cell

ρm ..... Bulk resistivity of deposited metal

x_c ..... Position at which the critical slope, β is first achieved

1. INTRODUCTION

1.1. Photovoltaic Electricity as a Renewable Energy Source

A growing concern for the effects of human progress on the environment from pollution and green-house gases along with the world-population reaching a landmark 7 billion in October 2011 has greatly increased the pressure for reliable renewable energy sources [1]. Studies put forth by the United States Department of Energy estimate the world power consumption at 13 terra Watts (TW) with an expected increase to 30 TW by 2050 [2]. As such, there are few options that are both carbon neutral and can meet the enormous scale required to tackle this increase in power consumption. Continued fossil fuel use combined with carbon sequestration has been explored, but logistics and cost problems remain a serious road block [3]. Nuclear energy is a promising candidate that could be scaled to meet the increased demand, but the required expansion would create such a strain on the global uranium sources that it would necessitate refining uranium isotopes from sea water [2]. Fortunately, the chief source of energy for the Earth, the Sun, remains a largely underutilized resource for power generation. Furthermore, the sunlight incident on the Earth's surface provides a radiant flux equivalent to 120,000 TW, much greater than the human population of Earth could ever utilize [2].

With all of these considerations, it is not surprising that the photovoltaic market has maintained an annual growth rate of 30% over the last decade [4]. As a direct result of growing mass production, installed cost of photovoltaic power has dropped significantly to around \$7/Watt at peak power output (W_p) on average in the US, with economies of scale further reducing the cost to around \$2.9/W_p for utility scale projects [5, 6]. Unfortunately, this is still 10

to 20 times the estimated cost that needs to be reached to meet grid parity, \$0.05-0.06/kWh (~\$0.33/W_p) [7]. Therefore the increased expense compared to grid power, combined with other logistics factors (energy storage, intermittency, required infrastructure, etc.) are hindering the widespread adaptation of this technology.

There are many areas for improvement that can be exploited to decrease the cost of solar power. Great strides have been taken in increasing efficiency over the past decades (see Figure 1), but increased efficiency alone cannot solve the problem.

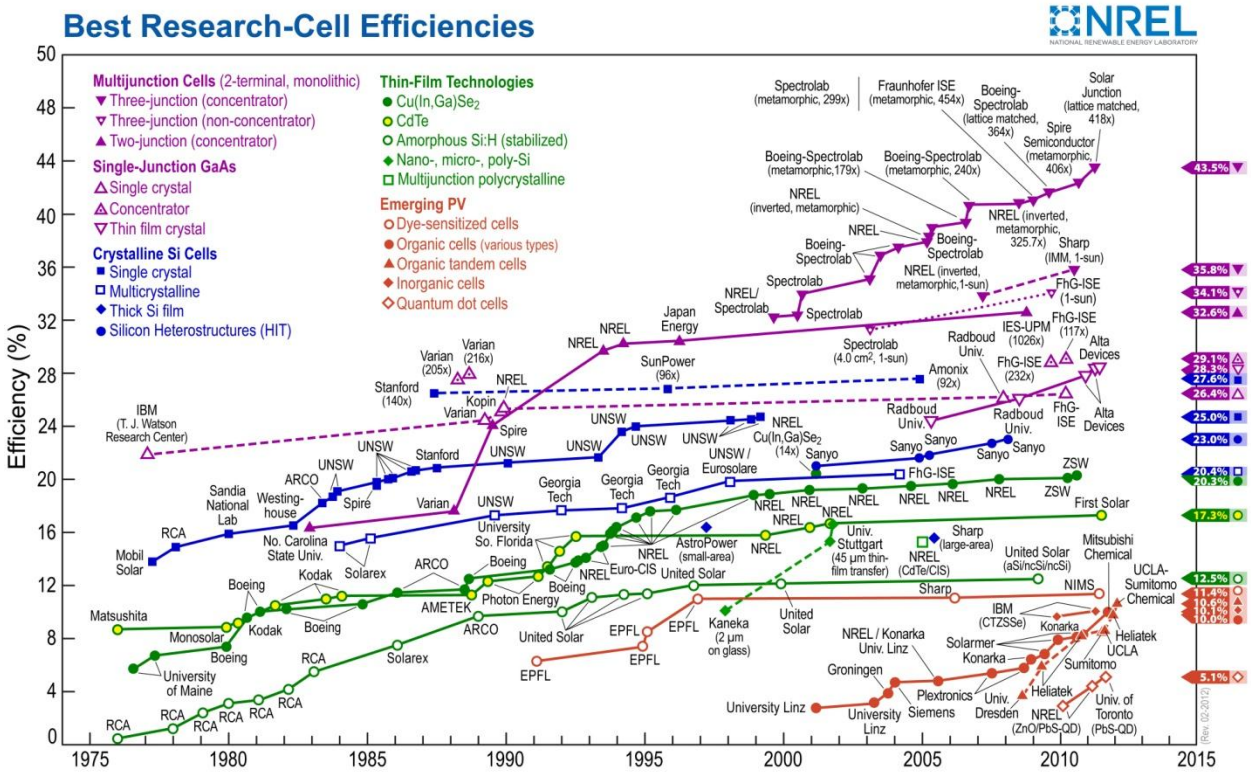


Figure 1. World record efficiencies for various photovoltaic technologies over the past four decades. Adopted from [8].

Attention must be given to the cost of materials and manufacturing processes that are required to make highly efficient cells when evaluating their ability to provide inexpensive electricity. Thus, for any technology to truly be an "advance" it must provide a decrease in the cost per W_p,

through either an efficiency increase, or material cost savings, or both. Consideration must also be given to the practical matter that for current manufacturers of photovoltaic devices to adopt a new technology, it must be modular in design so that it can be placed in the already existing production lines with little or no modification. As a practical example, the current collector grids of most crystalline-silicon solar cells are currently deposited via screen printing. Screen printing has dominated the photovoltaic industry because of its relative simplicity and scalability. However, it is a well-known fact that screen printed collector grids can be a major source of losses in the finished cell due to low conductivity and shadowing of the active cell area. Furthermore, because screen printing is a contact printing process, an increased occurrence of wafer breakage is expected as solar cells become thinner for better material utilization, increasing overall production costs [9]. Despite its noted short comings, any technology that seeks to supplant screen printing within the manufacturing of solar cells must be similarly scalable and modular in design.

1.2. Thesis Outline

With the previous considerations noted, this study presents an alternative non-contact, direct-write method of depositing the current collector grid. Collimated Aerosol Beam Direct Write (CAB-DW) is a technology that was developed at NDSU and has the ability to deposit gridlines much narrower than possible with screen printing, which may translate into decreased shadowing and resistive losses within the solar cell. A survey of competing collector grid deposition methods including screen printing, ink jet, Aerosol-Jet, and nScrypt is presented with the best grid finger dimensions achieved to date on test cells. The respective geometries are then compared using an analytical model obtained from the literature. By combining device characteristic data with measured material properties, a clear advantage of CAB-DW in cell

performance is demonstrated by the model with an optimal grid finger width of around 20 μm. A study of the electrical properties of two types of silver nanoparticle inks, namely bulk resistivity and specific contact resistivity, is demonstrated through extensive experimental results. Experimental cell performance data for optimized and non-optimized grid structures deposited via CAB-DW is also presented within this work. By combining the experimental and modeled results it is then possible to conclude that grid fingers deposited with the CAB-DW system allow for increased cell efficiency.

2. LITERATURE REVIEW

2.1. A Brief History of Photovoltaics

The photovoltaic effect was first observed by Edmond Becquerel in 1839 when he noticed a voltage was produced when light shone on an electrode in an electrolyte [10, 11]. Further progress was made in 1876 when Adams and Day discovered the same phenomenon occurred in selenium [10]. However, by 1914 selenium solar cells had only reached ~1% efficiency, limiting their usefulness mainly to photographic light meters [10]. It wasn't until 1954 that researchers at Bell Laboratories created the first practical crystalline silicon (C-Si) solar cell having an efficiency of 6% [10]. Finally, a useful amount of electricity could be produced using a solid-state device. Although this achievement ushered in the promise of virtually unlimited energy from the sun, the electricity was still much more expensive than that produced by traditional fossil fuel sources.

The launch of the first manmade satellite, Sputnik I, on October 4th, 1957 opened a new era of exploration, as well as immense military and civilian opportunities [12]. However, the remoteness of space required a stand-alone power source which could provide energy for the duration of the space-craft's lifetime, which may be years or even decades. Although Sputnik I relied on zinc-silver batteries as its power source, the practicality of using photovoltaics as a power source was realized first on the U.S. Vanguard I satellite thanks to a visionary named Hans Ziegler [12,13,14]. The batteries powering one half of the satellite's radio system lasted only 20 days, while the solar array kept the satellite active for ~7 years [13]. This technological success created a strong demand for photovoltaics in the space industry, and would drive their further development. Unfortunately, the expense of the systems still prohibited widespread adaptation of the technology on earth beyond specialty applications, such as powering navigation

buoys, lighthouses, and navigation lights on offshore oil rigs in which photovoltaic electricity have proven more cost effective than other alternatives [14]. However, with recent gains in production capacity and cell efficiency, the cost per W_p has been steadily declining.

2.2. Basic Solar Cell Physics

One of the most unique and appealing characteristics of solar cells is that they can directly convert sunlight into electricity, with no moving parts to wear out. The device is able to do this by capturing free electrons created by the photo-electric effect. For the sake of clarity the basic operation will be explained using standard mono-crystalline silicon solar cells, however these concepts can be applied to other device types as well.

Although silicon is a semi-conductor, in its intrinsic crystalline form it is actually an insulator. Silicon is a group 4 element, meaning that each silicon atom has four unpaired valence electrons. When silicon crystallizes it forms what is known as a diamond lattice, with each silicon atom forming a valence bond with the four closest silicon atoms in the lattice [15]. As such, for crystalline intrinsic silicon the outer valence shell of each atom is filled. At this time it is proper to recall from quantum theory that an electron in free space is able to attain energy levels that are essentially a continuum [16]. For an electron associated with a single atom, this changes to the electron being confined to well defined energy levels [16]. However, when several atoms are grouped in an ordered fashion, such as in a crystal lattice, the discreet energy levels which the electron was previously confined to smear together yielding bands of energy which are attainable by the electron separated by forbidden bands [16]. Thus, intrinsic silicon will act as an insulator, unless sufficient amounts of energy are supplied to push the valence electrons up into the conducting band. Through the introduction of impurities, by a process called doping; it is possible to alter the electron structure of the crystal lattice.

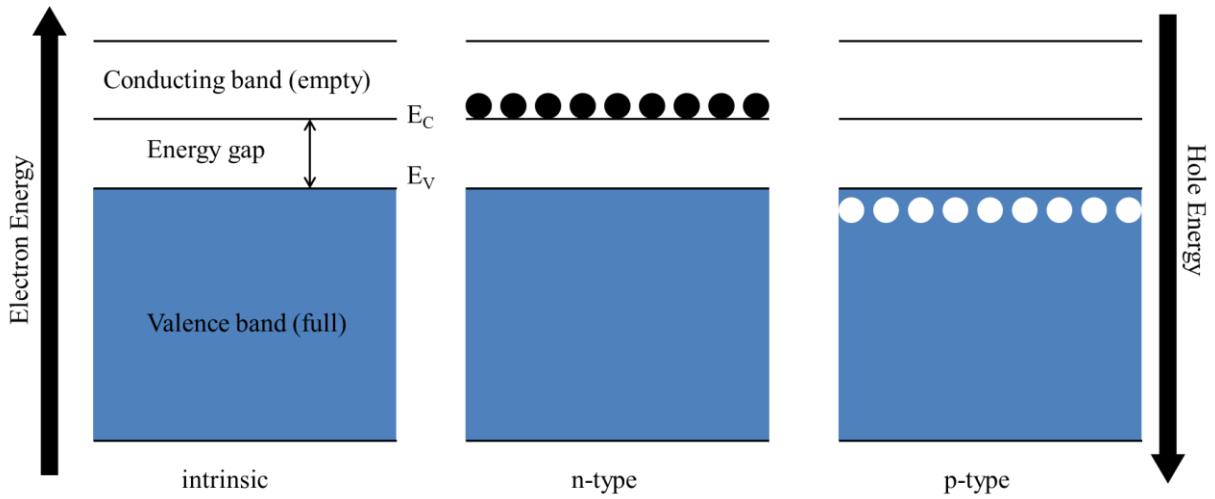


Figure 2. Band diagram of valence electron structure, band gap energy, and the effects of n-type and p-type doping. Adapted from [15].

Adding a group-5 element such as phosphorous will yield n-type silicon, while introducing a group-3 element such as boron will yield p-type silicon [17]. In the first case, phosphorous atoms are substituted into the lattice structure, but unlike the silicon atoms which they replace, phosphorous has five valence electrons. Because the valence band of the crystal structure is filled by only four of the five electrons associated with the dopant atom, the extra electron associated can easily dissociate from the dopant atom and move into the conducting band of the crystal structure [15]. A schematic representation of this can be seen above in Figure 2 where the free electrons are represented by black circles. A similar process takes place when making p-type silicon. When boron, a group-3 element, is substituted into a crystal of silicon, it only has three valence electrons to donate to the lattice, leaving an empty position or hole [15]. The hole remains neutral until it captures a neighboring electron, at which point it essentially begins to move freely as a charge carrier within the crystal lattice. Whereas in n-type silicon the charge carriers are considered negative (electrons), in p-type silicon the charge carriers are considered positive (holes). In short, n-type silicon contains free electrons which can act as

negatively charged current carriers, and p-type silicon contains holes which act as positively charged current carriers. A useful analogy proposed by Green can be seen below in Figure 3 [16].

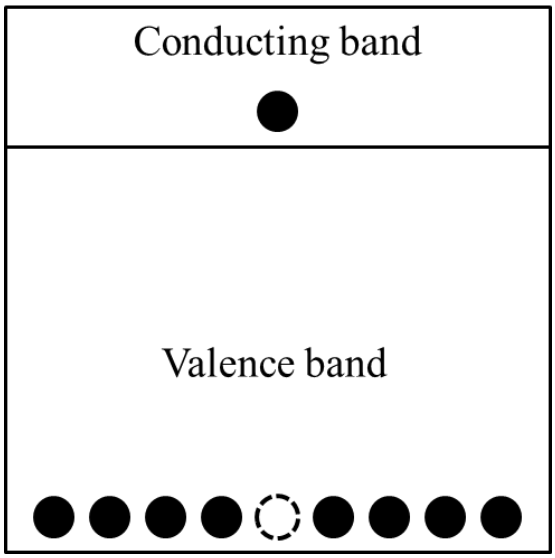


Figure 3. Diagram illustrating how electrons and holes both act as charge carriers. Adapted from [16].

As shown in Figure 3 for intrinsic silicon, if an electron is moved from the valence band to the conducting band, it is then free to carry current. However, the hole that it leaves behind in the valence band allows an electron to shift in the valence band to fill the hole. This in turn creates another hole in the previous location of the electron; or from a different perspective, the hole moves from its initial position to another adjacent position. It is by this mechanism that a hole can be thought of as a positive charge carrier.

An interesting phenomenon occurs when a junction is formed with p-type and n-type silicon. Although the process for forming such junctions is more involved, let us assume that it is as simple as taking the respective materials and joining them. The excess electrons in the n-type material will diffuse into the p-type material, and the excess of holes in the p-type material will

diffuse into the n-type material. However, as the majority carriers (electrons in n-type material and holes in p-type material) diffuse, an electric field is created by the ions they have left behind in the crystal lattice. This electric field then acts as a barrier limiting additional diffusion of majority carriers [17]. This barrier, in the form of an electric field, is one of the key components that make a solar cell functional.

Drawing from quantum physics, it is known that when a photon with energy greater than or equal to the band gap energy is incident on a given material it can be absorbed resulting in the excitation of an electron into the conduction band from the valence band, a process known as fundamental absorption [16]. However, the laws of physics demand that both energy and momentum be conserved during this process. That is the energy and momentum of the absorbed photon must be equal to the energy and momentum of the resultant excited electron [16]. In an indirect band gap material such as silicon, the difference in the momentum of an electron in the valence conducting bands is much larger than the momentum provided by a photon whose energy is greater than or equal to the band gap of silicon [15]. As such, a third particle known as a phonon, or lattice vibration, must make up for the momentum discrepancy [15, 16]. The requirement of three particles interacting simultaneously greatly reduces the likelihood of fundamental absorption occurring, which effectively decreases the absorption by silicon. On the other hand, materials such as gallium-arsenide (GaAs), are direct band gap materials and do not require a three particle interaction and are therefore much better absorbers [15, 16, 17].

Assuming that the newly created free electron-hole pair is sufficiently close to the p-n junction, the electric field of the junction will keep the majority carrier in its respective material, and accelerate the minority carrier across the junction [17]. Thus an accumulation of free majority carriers is produced in each material, and if the n and p sides of the junction are

connected through a load, a current is produced (See Figure 4 below). In a concurrent process electron hole pairs can recombine and release a phonon (heat), further increasing cell inefficiencies. Proper care must be taken when designing solar cells to maximum the utilization of the electron-hole pairs.

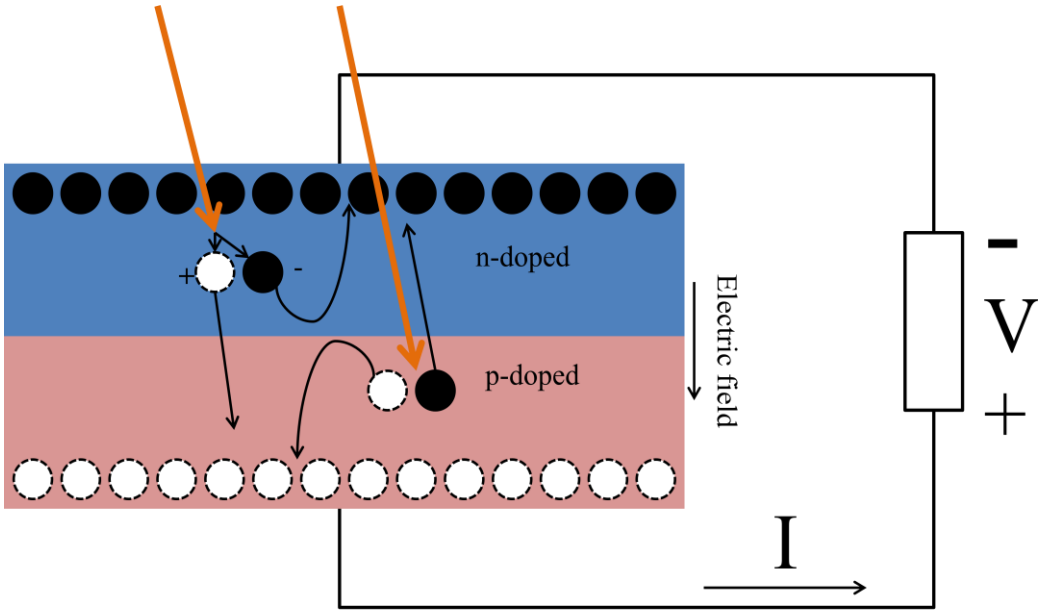


Figure 4. Diagram of the formation and separation of free charge carriers within the depletion region of the p-n junction within a solar cell. Adapted from [17].

There is a further consideration that must be made with regard to the band gap energy of semiconductor materials. The air mass 1.5 global (AM 1.5 G) solar spectrum, shown below in Figure 5, is used as a reference with regard to the intensity and wavelength of incident radiation on the earth's surface assuming a standard set of conditions [15]. The overall solar spectrum is similar to a black-body radiation source but with bands of energy reduced due to absorption by compounds in the atmosphere such as water vapor. The AM 1.5 G solar spectrum is a model of the actual solar spectrum after passing through a model atmosphere 1.5 times the thickness of Earth's atmosphere. The additional thickness is due to the increased path length through the atmosphere experienced by sunlight at latitudes further from the equator. Notice that the majority

of the incident radiation is in the visible spectrum (380-740 nm). This corresponds to photon energies between ~ 2 and 3 electron volts (eV), which are larger than the band gap energy of c-Si (~ 1.12 eV) [15]. Therefore, an absorbed photon has energy in excess of the band gap of the absorbing material, and the excess energy will be wasted as heat generation which corresponds to inefficiency within the solar cell [15].

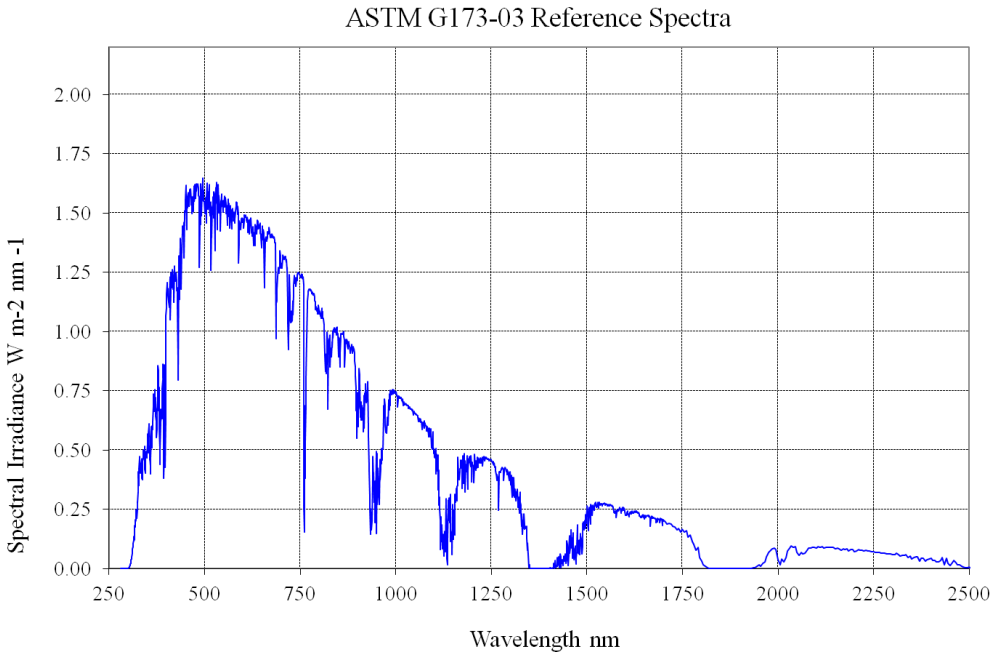


Figure 5.AM 1.5 G reference solar spectrum. Adapted from [18].

The efficiency of a device operating under AM 1.5 G solar conditions is then directly related to the band gap energy of the semiconductor material it is made from. As such, it is possible to calculate theoretical efficiencies based on the band gap of the material in question. A plot of the theoretical efficiencies of various solar cell types can be seen below in Figure 6. From this it can be seen that the maximum efficiency expected from silicon is around 27%, whereas efficiencies of ~ 30% are projected from GaAs and cadmium telluride (CdTe) cells [19].

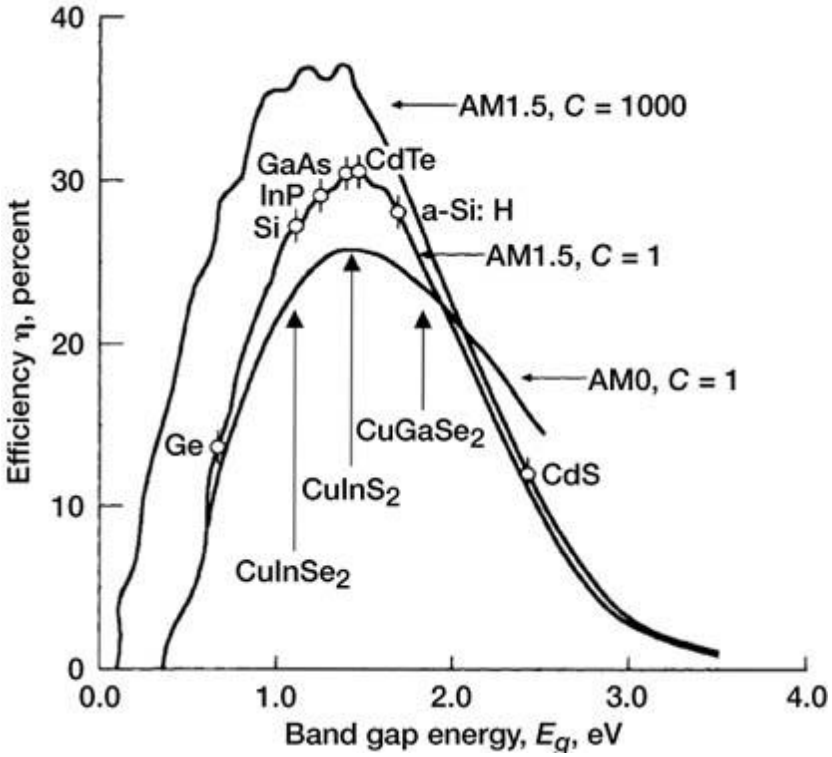


Figure 6. Theoretical efficiency versus band gap energy for standard solar spectra. Adopted from [19] with permission.

2.3. Mono and Multi-Crystalline Silicon Solar Cells

Although crystalline-silicon (c-Si) solar cells have dominated solar power generation since the 1950's, changes in technology utilizing different materials and processes have been developed along the way. The key driver for all such research has ultimately been cost reduction, either through decreased material cost, increased efficiency or both. Starting from its humble roots of lab scale production, an industrial process for producing affordable and reliable solar cells using both multi and mono-crystalline silicon has been developed over the past decades. For mono-crystalline silicon cells the process begins with production of the substrate material, which is commonly p-type silicon. Previously, wafers from the very large scale integration (VLSI) electronics industry, along with polysilicon that did not meet VLSI specifications were used as a supply stock for the solar cell industry [10].

Mono-crystalline silicon is produced using either the well-known Czochralski (CZ), or float zone (FZ) processes, both of which are expensive resulting in increased material costs. According to del Canizo et al [9] ingot growth and conversion of the ingot into wafers makes up 19% of the cost of producing a solar cell. Furthermore, the wafering process, which breaks the ingot down into individual wafers, can be extremely wasteful, with up to ~50% of the original ingot being destroyed because of the 200 µm wide kerf needed to cut a 200 µm wide wafer [9].

Once the wafers have been produced they are usually processed with an alkaline etch to remove damage done by the sawing process and texture the surface of the wafer to reduce reflective losses, enhancing cell performance [10, 20]. The wafers are then cleaned in preparation for the doping process. Alternative processing methods have been explored that attempt to skip the waste and added cost associated with using the CZ process. Although each method is unique in its own right, they all share the common goal of producing continuous silicon ribbons, which can simply be scribed and used as a direct wafer feed stock [10, 16, 17, 20].

Doping is usually accomplished by introducing a phosphorous containing liquid, such as $POCl_3$, into the atmosphere of a furnace via a bubbler and carrier gas while the wafers are heated to high temperatures (850 °C – 900 °C) [10, 21, 22]. Other methods of applying the dopants directly on the cell surface, as either a sprayed on liquid or a paste have also been explored [21]. After the formation of the p-n junction, the wafers must be chemically processed to remove a layer of phosphorous-silicate glass, which forms as a byproduct of the $POCl_3$ doping proces [22]. A chemical process is then used to remove the parasitic p-n junction that has formed on the edges of the wafer [10]. A surface passivation layer, usually consisting of a thermally grown oxide layer [22] is then deposited to decrease the effects of surface recombination. Anti-reflection coatings (ARC) are then applied usually in the form of TiO_2, or SiN_x [10, 22]. Finally,

front and back metallization layers are deposited via screen printing methods, allowed to dry and then fired to both sinter the metallic particles, increasing bulk conductivity and allow the front contacts to burn through the ARC and make electrical contact with the solar cell [10, 22]. The finished cell structure can be seen in Figure 7.

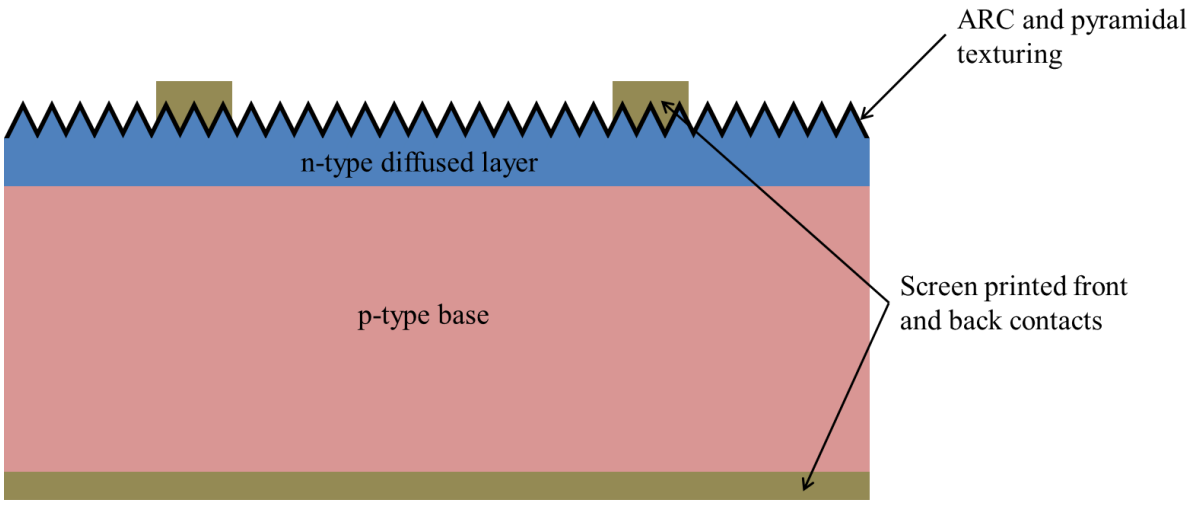


Figure 7. Schematic of standard cell structure for mono-crystalline silicon solar cells.

Multi-crystalline silicon solar cells are generally processed in a similar fashion except that standard texturing techniques cannot be used due to the different orientations of each crystal. Methods such as casting and ribbon processes [16, 17, 20] have also been developed specifically for making solar grade multi-crystalline silicon. In addition, specialized processes incorporating hydrogen have been developed to limit the effects of the grain boundaries acting as recombination sites [10]. Using these and other proprietary processes, current mass produced mono and multi-crystalline silicon solar cells have reached efficiencies of 19% and 17%, respectively [23]. Record cells of both types have reached efficiencies of 25% and 20.4% respectively [8].

2.4. Thin Film Solar Cells

Thin film solar cells hold an advantage over c-Si cells in that they do not require the expensive crystal growth and wafering processes associated with crystalline silicon solar cells. Instead, thin layers of semi-conductor materials such as $CuInSe_2$ (CIS), CdTe, CdS, amorphous silicon (a-Si), and $Cu(InGa)Se_2$ (CIGS) are deposited either on a substrate or a superstrate usually consisting of glass or other inexpensive materials such as metal foils [23, 24, 25].

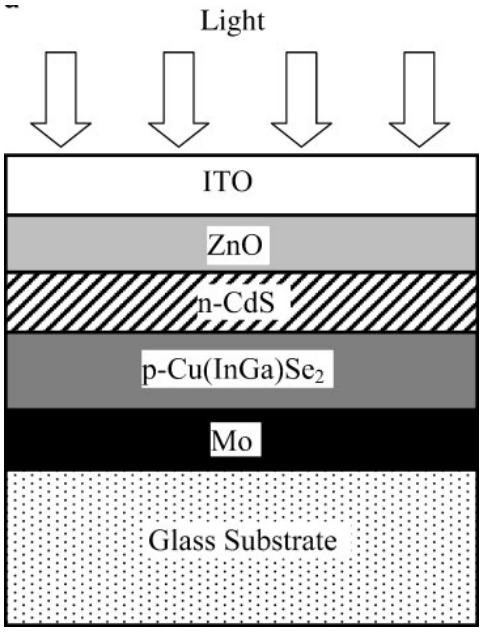


Figure 8. Example structure of $Cu(InGa)Se_2$ (CIGS) thin film solar cell. Adopted from [24].

The ability to utilize thin films removes the geometric constraints associated with c-Si solar cell technology. Instead of being restricted to the largest production wafer size , currently at 156 mm × 156 mm for c-Si technology [26], the possibility of solar cell dimensions in the meter range are feasible [25].

Perhaps the most promising thin film devices are those using $Cu(InGa)Se_2$ (CIGS). A diagram of the typical architecture of a CIGS thin film solar cell can be seen in Figure 8. The world record for a CIGS thin film solar cell is currently held by ZSW (Center for Solar Energy and Hydrogen Research, Germany) at 20.1%, supplanting the NREL which produced the highest efficiency CIGS cells for 16 years [27]. However, production scale CIGS thin film solar cells range in rated efficiency from 11%-14% efficiency [28, 29].

Different deposition methods are used to produce thin film devices depending on structure type, but generally they include chemical vapor deposition (CVD), plasma enhanced chemical vapor deposition (PECVD), sputtering processes, screen printing, and electrolytic baths [10, 23]. However, there has been a recent push toward roll-to-roll processing, including inkjet and other printing methods to mass produce thin film solar cells, therefore avoiding the batch processing associated with vacuum based processes [25, 30, 31]. Although the resulting solar cells are not as efficient as the champion cells produced in the laboratory, the cost savings through efficient mass production greatly outweigh the loss in efficiency.

Amorphous silicon (a-Si), deposited using the previously mentioned processes, has also been used as a feedstock for thin film solar cells. Unfortunately, upon exposure to the sun the performance of a-Si solar cells decreases substantially, resulting in stabilized efficiencies of only ~ 8% due to the Staebler-Wronski effect [32]. However, a-Si technology has been successfully combined with c-Si technology to produce a highly efficient hybrid solar cell.

2.5. Hybrid Solar Cells

Thin film and c-Si technologies have been combined into hybrid structure known as a silicon heterojunction (SHJ) or heterojunction with intrinsic thin layer (HIT™). HIT™ cells were

first developed by Sanyo Electric Company, and entered mass production in 1997 [33]. Record efficiencies of 23% have been demonstrated with devices built at Sanyo Electric Company, with current mass produced cells reaching efficiencies of 20.2% [33, 34]. The cell structures consist of a doped c-Si wafer that is cleaned and then coated with a very thin layer (~ 10 nm) of amorphous silicon (a-Si) to passivate the c-Si surface and form the p-n junction [33]. Unfortunately, due to the proprietary nature of their process, no other additional information could be found on the HIT™ solar cells produced by Sanyo Electric Company [35]. There has been a strong push in the scientific community to better understand the construction and refinement of SHJ devices due to the lack of transparency on the part of Sanyo Electric Company

A group at the National Renewable Energy Laboratory (NREL) has also been conducting research in the area of SHJ devices, and it is their devices that are studied in the present work. A typical cell structure produced at NREL can be seen in Figure 9. The SHJ structure consists of a c-Si wafer that is either polished, or textured for anti-reflection purposes [36] with an extremely thin (< 10 nm) a-Si layer deposited onto the c-Si wafer. It is very important that the c-Si be cleaned well using established chemical cleaning processes prior to any film depositions [36]. Intrinsic and doped a-Si layers are then deposited using hot wire chemical vapor deposition (HWCVD) [36]. HWCVD, like other CVD processes, is a vacuum based process in which a precursor gas or gasses are broken down by imparting thermal energy to the gas. The products then deposit on all exposed surfaces within the chamber.

The added benefit of HWCVD over PECVD is that faster growth rates are achieved and the damaging ion bombardment of the c-Si by the plasma greatly reduced [35, 37]. In this case, silane (SiH_4) gas is used to grow the intrinsic layer, and a combination of silane, hydrogen (H_2),

and either phosphine (PH_3), or diborane (B_2H_6), are used to deposit the emitter and back contact layers [36]. Process temperatures range from 100 °C to 250°C [36].

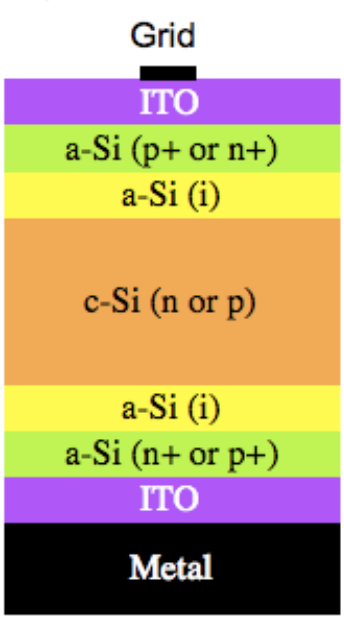


Figure 9. A typical SHJ structure produced at NREL. Adapted from [36].

A layer of indium tin oxide (ITO), is then deposited on the front and backside of the cell, serving as an anti-reflection coating and transparent conducting layer [36, 38]. Finally, metal contacts in the form of a Ti/Pd/Ag/Pd stack are applied to the front and back of the device via electron-beam evaporation [39]. The Ti layer is used to promote adhesion to the device and the Pd is used as a capping layer to the Ti to prevent an undesirable reaction between the Ag and Ti. Efficiencies as high as 18.8%-19.0% have been realized with NREL produced SHJ devices using p-type CZ and FZ c-Si as the base [40].

2.6. Efficiency Considerations

2.6.1. I-V characteristics and effect on cell efficiency

It has been demonstrated that the inherent efficiency of a solar cell is largely dependent upon the internal quality and workings of the p-n junction and surrounding semi-conductor materials. However, a more detailed analysis of the complete solar cell device is needed to understand the other factors which can affect a cell's efficiency. Various models have been developed over the past decades to approximate the solar cell and expected efficiency with a common example shown in Figure 10.

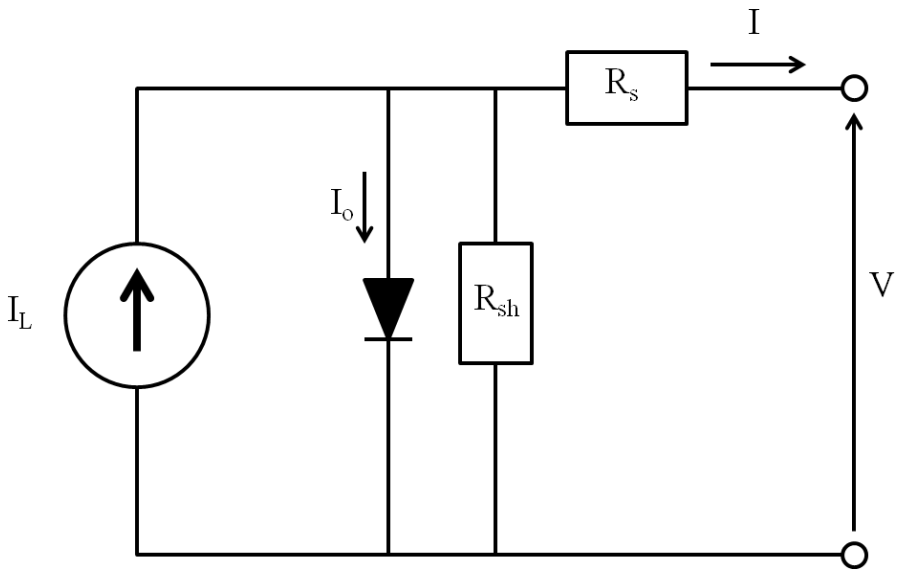


Figure 10. Equivalent circuit model of a solar cell including light generated current source (I_L) parasitic shunt resistance (R_{sh}), and parasitic series resistance (R_s). Adapted from [41].

By analyzing the equivalent circuit in Figure 10, and including the Shockley diode equation, it is then possible to derive an equation that includes the effects of resistive losses within the solar along with the diode behavior of the device. The result, Eq. (1) can be seen below [41, 42].

$$I = I_L - I_0\left(e^{\frac{q(V+IR_s)}{kT}} - 1\right) - \frac{V + IR_s}{R_{sh}} \quad (1)$$

Where I_L is the light induced current, I_o is the reverse saturation current, I is the current drawn from the cell, V is the voltage across the cell, q/kT is the thermal voltage, R_s is the series resistance, and R_{sh} is the shunt resistance. It should be noted that for most production solar cells $I_L \cong I_{sc}$. The above expression can be plotted parametrically for R_s and R_{sh} respectively as shown in Figure 11.

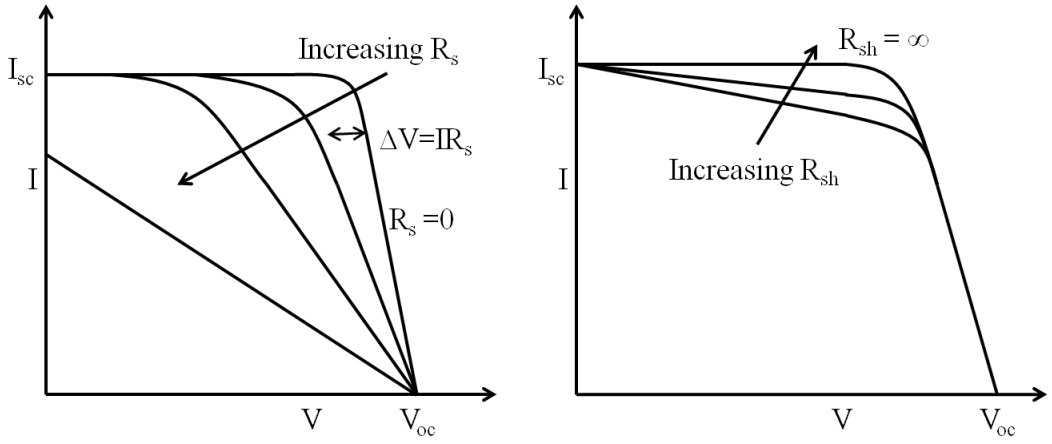


Figure 11. Schematic illustrating the effects of changes in R_s and R_{sh} respectively. Adapted from [41].

Figure 11 demonstrates how changes in the values of R_s and R_{sh} affect the I-V characteristics of the cells. From the I-V curve in the left of Figure 11, it is clear that the current, I, remains relatively constant with voltage until a certain threshold voltage is reached, where even a small increase in voltage results in a steep decrease in I. As R_s increases, this threshold voltage decreases, and if R_s is large enough, the short circuit current can actually be reduced. For high efficiency solar cells R_s should be minimized, R_{sh} should be maximized. R_{sh} is a measure of the quality of the p-n junction in that the higher the value of R_{sh} the less current flows backward across the p-n junction which would result in power loss. In order to better understand the

relationship between R_s, R_{sh} and efficiency it is helpful to introduce a measure known as the fill factor (FF). For any solar cell, the power output at each point on its I-V curve can be calculated as a product of I and V. A plot of this can be seen in Figure 12. At some point along the I-V curve the product of I and V will be maximized. This point is termed the maximum power point (mpp) and is characterized by the current (I_{mpp}) and voltage (V_{mpp}) at that point.

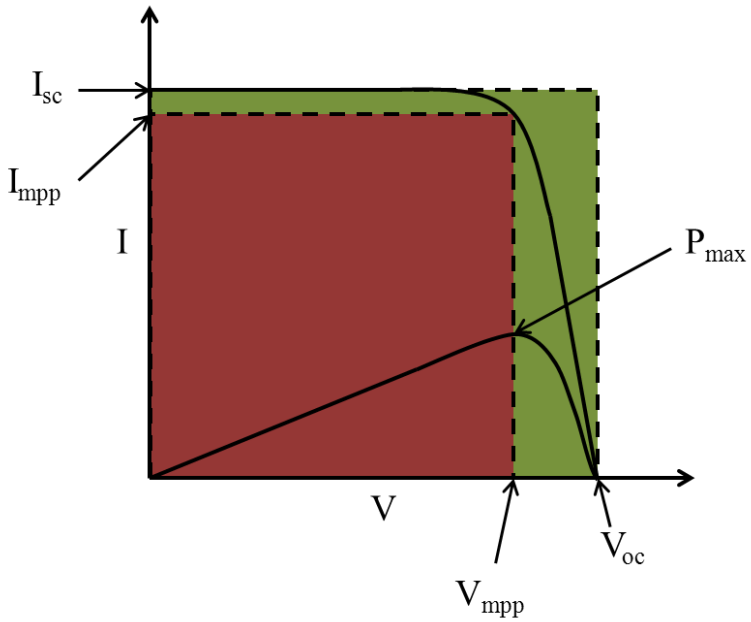


Figure 12. Illustration of fill factor (FF) and power output of a typical solar cell.

The maximum theoretical power output of the solar cell is defined as the product of the short circuit current (I_{sc}) and the open circuit voltage (V_{oc}). The fill factor can be defined as the ratio of the actual maximum power to the maximum theoretical power output of the solar cell (see Eq. (2) below).

$$FF = \frac{P_{max}}{P_{max\ theor.}} = \frac{I_{mpp}V_{mpp}}{I_{sc}V_{oc}} \tag{2}$$

It should be emphasized that due to the imperfect diode behavior of a solar cell, a fill factor of 100% is impossible, even if R_s is infinitely small and R_{sh} is infinitely large. As such,

typical fill factors for industrial solar cells are in the 75-80% range [10]. In order to achieve such high fill factors it is necessary to decrease R_s to as small as practically possible. It is for this reason that both an ITO layer and a top metallization layer are applied to the SHJ devices. Recently there has also been research directed toward developing more robust transparent conductors using metallic nanowires and fibers [43, 44, 45]. Care must be taken in the addition of a metallic collector grid, as the grid also shadows the active area of the cell, directly affecting I_{sc}. As such, a balance between the shadowing or optical losses of the cell and the electrical losses of the cell must be struck.

2.6.2. Optical losses and light trapping

Although achieving a high fill factor through minimizing resistive losses within a solar cell is necessary to yield high efficiency, a very important aspect of the cell's efficiency is its ability to absorb incident light.

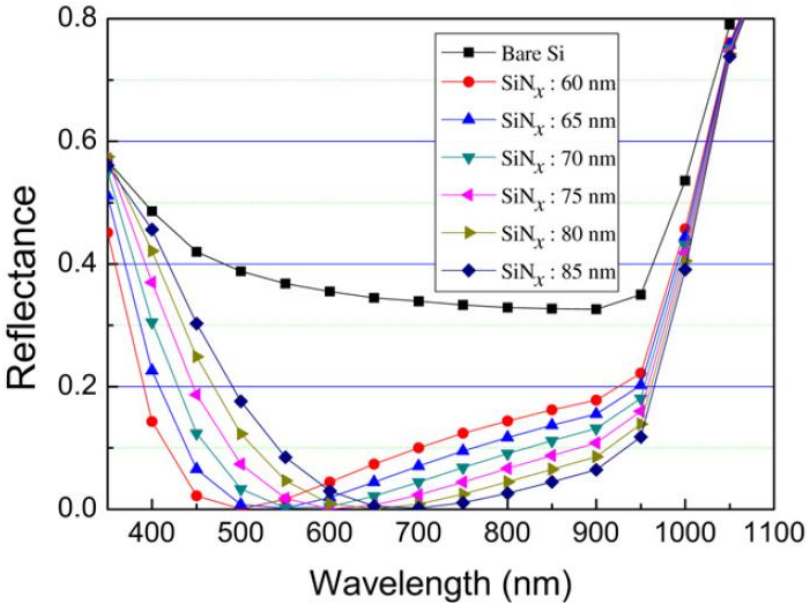


Figure 13. Numerical simulation of the reduction in reflection with ARC of varying thickness. Adopted from [47].

In fact, the short circuit current, I_{sc} is directly related to the solar cell's ability to absorb incident light. To maximize I_{sc} reflective losses need to be minimized. Reflection of incident light can occur when light encounters the current collector grid, the front surface of the cell, as well as the back contact of the cell [42].

ARC layers and cell texturing are employed in order to maximize the probability of absorption of incident photons. ARC's usually consist of single or multiple thin layers of materials such as TiO_2 and SiN_x, $SiO_x(C)$, SiN_x:H due to their desirable index of refraction which makes them amenable to forming a ¼ wavelength ARC [15, 17, 42, 46, 47, 48]. These materials are widely used because their index of refraction is near the geometric mean of Si (n = 3.7 - 3.8) and glass (n = 1.5) which is usually used as a capping layer in the final cell assembly [15, 42]. Once the material or materials for the ARC have been chosen it is necessary to determine the optimum thickness for the ARC layers which directly affects which wavelengths of light will be best absorbed as is clearly demonstrated in Figure 13.

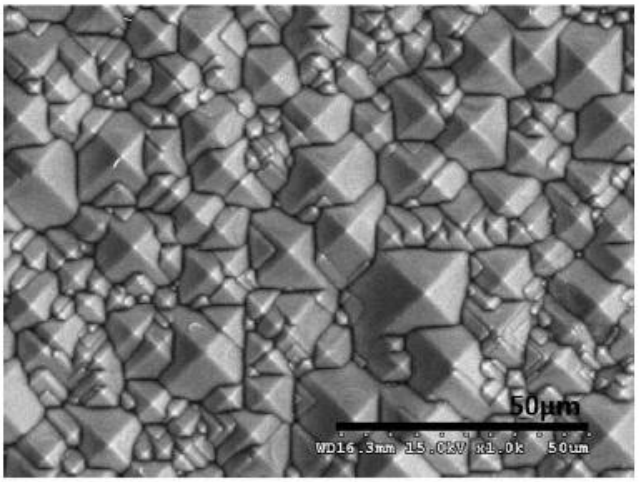


Figure 14. SEM image of textured c-Si wafer surface. Adapted from [49].

Besides substantially reducing the reflectance from the front solar cell surface the ARC can also act as a surface passivation layer, reducing the carrier recombination velocity at the

front surface of the cell [46, 47]. PECVD is used for depositing most SiN_x and SiN_x:H ARC's [15, 46] however some ARC's such as SiO_x(C) are deposited via spray coating and subsequent baking [48].

Surface texturing, normally carried out with an alkaline etching process, is another method used to reduce reflection from solar cells. For c-Si (100), anisotropic etching preferential along the (111) crystal plane results in the formation of pyramidal structures as shown in Figure 14 [49].The added optical benefit of a textured surface is that light which does reflect from the cell's surface is more likely to be reflected back onto an adjacent portion of the cell before being reflected out of the cell module (see Figure 15). As a direct result, the probability that the light is absorbed increases substantially.

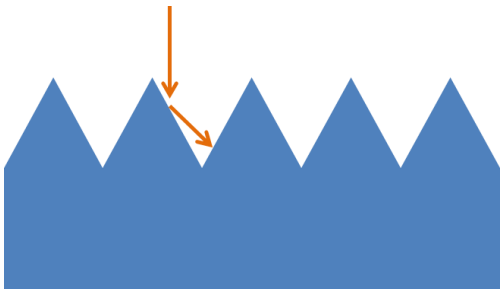


Figure 15. Schematic of the multiple reflections necessary for light to be reflected from a textured solar cell.

For example, if the reflectance of the non-textured silicon is assumed to be around 20%, the probability that incident light will reflect off of the surface twice drops to 4% (0.2×0.2) [17]. It should be noted that both front and back solar cell surfaces can be textured to reduce reflective losses. When an ARC and texturing are combined the reflective losses can be decreased to values below 5% for much of the visible spectrum as shown in Figure 16.

The final source of optical loss is the shadowing brought about by the current collector grid, or top metallization layer. Careful grid design is extremely important as a balance must be struck which minimizes both resistive losses and shadowing losses simultaneously.

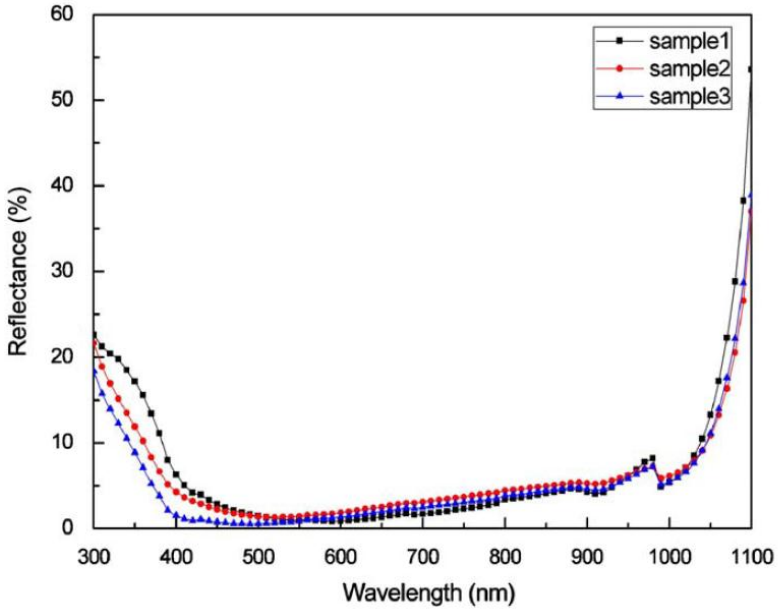


Figure 16. Reflectance from 3 solar cells having both textured surfaces and SiN_x ARC. Adopted from [49].

Although in most cases shadowing losses are equivalent to the area coverage of the cell with metal, Blakers demonstrated that for an encapsulated collector line with semi-circular cross section, the optical line width could be as little as 35% of the geometric line width [50, 51]. Similarly, Woehl, Horteis and Glunz, demonstrated optical widths of 36% and 42% of the geometrical width of Aerosol Jet printed and plated grid fingers, and standard screen printed grid fingers respectively [52].

It should be noted that as a standard practice, it is necessary to encapsulate solar cell arrays in glass assemblies to protect them from their operating environment. In standard industry practice, ethylene vinyl acetate (EVA) is used as a transparent binding layer between the glass

and the solar cells. In this case it is assumed that the EVA layer has the same index of refraction as the encapsulant glass.

In order to better understand how a reduced optical grid finger width occurs it is helpful to consider the case of a semicircular cross section grid finger as shown in Figure 17.

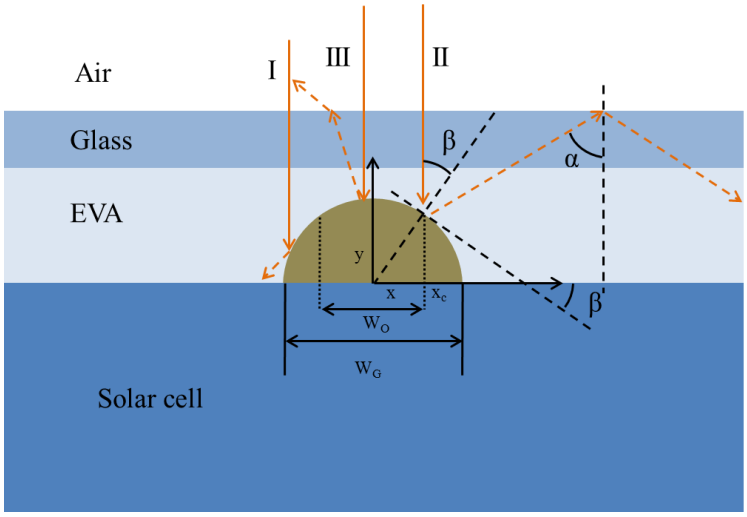


Figure 17. Diagram illustrating the types of reflection that can occur from a semicircle cross-section collector gridline. Adapted from [52].

It is assumed that the incident light is normal to the solar cell surface, that the absorption of the silver is negligible, and that the reflectance from the silver contact is specular in nature. With these assumptions, light encountering the silver contact will be reflected in one of three fashions. In case I, the incident light will be reflected directly from the contact onto the active region of the solar cell. In case II, the incident light will be reflected from the contact back toward the glass-air interface at the front of the module, but the angle at which it is reflected will be greater than or equal to the critical angle needed to facilitate total internal reflection, in this case α. Case III is simply a direct reflection of the incident light out of the module. A tangent with an angle of inclination of β can be drawn with respect to the semi-circular cross section of the collector line.

It is easily seen that β can be defined as α/2. α can be derived from the optical properties of the encapsulant as shown in Eq. (3).

$$\alpha = \sin^{-1}\left(\frac{n_{air}}{n_{glass}}\right) \approx 40.8\,° \tag{3}$$

where n_{air} is the index of refraction for air, which is assumed to be 1.0 and n_{glass} is the index of refraction for glass, in this case assumed to be 1.47. Using basic geometry, it is then possible to relate the slope of the semicircle at the critical point to the critical tangent angle β. Assuming a unit semicircle with the origin defined at its center as in Figure 17.

$$\frac{dy}{dx} = \left(\frac{-x}{\sqrt{1-x^2}}\right) = \tan\beta = -0.37 \tag{4}$$

The expression in Eq. (4) can then be solved for the critical x location, x_c, at which the critical slope occurs. At values greater than x_c any normally incident light will be reflected back to the solar cell either by internal reflection at the glass-air interface or by direct reflection as in case I. This results in an effective optical width (W_O) that can be as little as 35% of the geometric width (W_G) [51]. The decrease in W_O results in a decrease in the shadowing losses within the solar cell due to the grid fingers.

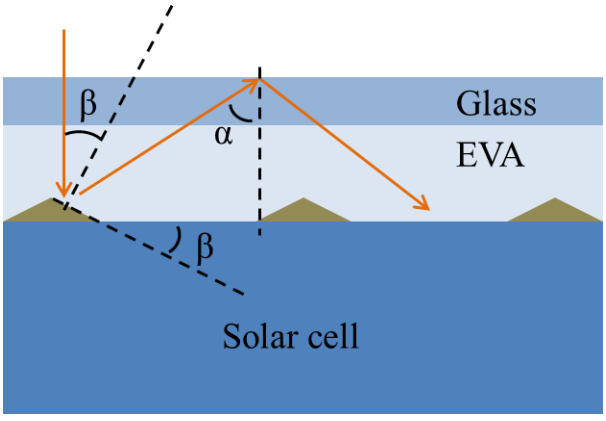


Figure 18. Diagram illustrating optically ideal triangular cross section collector lines.

Under the same assumptions, it is readily apparent that the optically ideal electrical contact would be triangular in cross-section having a slope, β, greater than or at the very least equal to α/2 (see Figure 18). With such a structure, and assuming perfect reflectance from the grid fingers, W_O would theoretically be 0%.

2.6.3. Background of cell modeling and optimization

There are several factors that need to be considered when attempting to optimize the performance of solar cells by minimizing series resistance. The sources of ohmic losses due to series resistance within a solar cell include: (1) The resistance of the bulk material of the cell. (2) The resistance within the top layer of the solar cell through which current flows toward its final collection site. (3) The contact resistance between the metal collector grid and the top layer of the cell. (4) The resistance of the metal making up the collector grid and the resistance of the back contact material. (5) The contact resistance between the back contact and the bulk of the device. A further loss of efficiency is brought about by the shadowing of active cell area by the metal collector grid. The optimization procedure must be able to minimize the power loss due to ohmic losses, while also minimizing the power loss due to shadowing of the active material.

Power loss due to series resistance depends not only on the current flowing from the cell, but the series resistance also affects the magnitude of the current flow from the cell. This can be seen by careful analysis of Eq. (1). Notice that this equation is non-linear, in that I, is dependent upon itself. As such, a closed form solution for I is impossible without making approximations or handling the problem numerically. Early attempts at modeling did consider the diode equation in efforts to maximize the power available from a solar cell. The basic scheme being to first determine an expression for R_s in terms of cell dimensions, collector grid dimensions and

material properties, and then maximize the resulting power expression written using the diode equation [53, 54].

Implicit in the previously mentioned approach is the ability to calculate an R_s value for the entire cell. In his paper, Handy models the total series resistance of a cell by means of an equivalent array of resistors, each representing one source of ohmic loss within the cell [55]. The values for the resistors making up the array are then rigorously derived analytically [55]. This same method, with some corrections and dispute over the accuracy of Handy's results was also employed by Sahai and Milnes [56].

Additional work was carried out by Wyeth [57] whose efforts were focused on a more accurate calculation of the sheet component of the series resistance brought about by the thin conducting layer in solar cells and its interaction with the current collector grid. In his paper, Wyeth showed analytically that reports by Wolf [54] and Handy [55] overestimated the series resistance component due to the top layer of the cell [57]. The following expression (Eq. (5)) for total resistance of a unit cell due to current flow, parallel to a, in the top conducting layer of the cell is given by Wyeth as follows [57]:

$$R_t = \frac{1}{12}(a/b)(\rho/t)G_t \tag{5}$$

where R_t is the total series resistance for a single unit cell, a and b are unit cell dimensions, ρ is the bulk resistivity of the top layer of the cell, t is the thickness of the top layer, and G_t is a modifying factor which depends on the unit cell dimension.

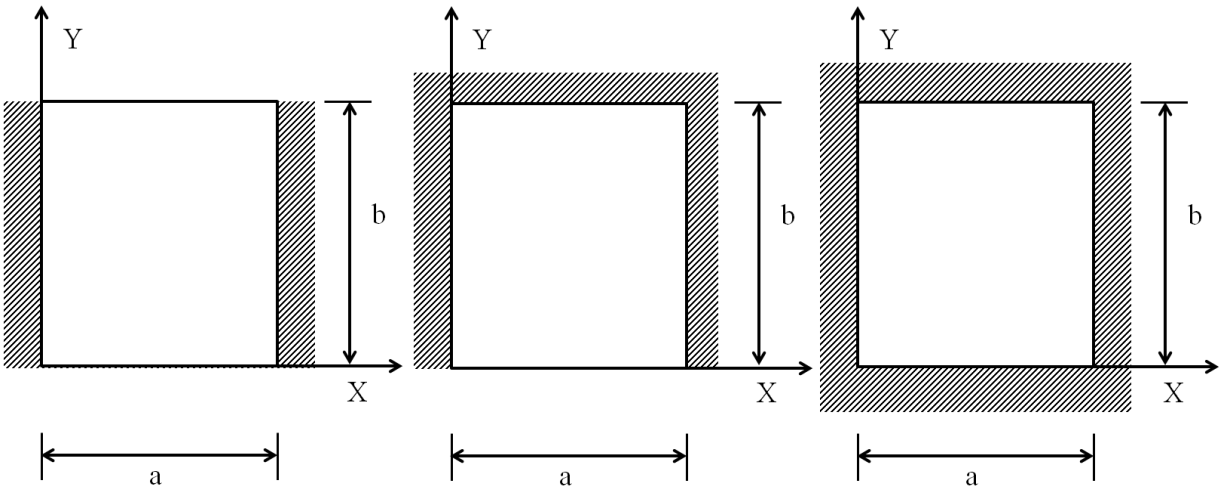


Figure 19. Diagram of grid structures considered in [57]. From left to right: parallel gridlines, gridlines connected by a bus-bar, mesh type grid.

The factor is equal to unity for the case in which the parallel collector lines tending a given unit cell are not connected by a bus bar (see Figure 19, left). For cases in which the collector line joins to a larger bus bar (see Figure 19, center), or in the case of a mesh type grid (see Figure 19, right) the modifying factors are given in Table 1.

Table 1. Modification factors for calculating series resistance in the top layer of a unit cell using Eq. (6). Adapted from [57].

a/b	**G_B** ***(Parallel Gridlines and Bus-bar)***	**G_C** ***(Mesh Grid)***
1.0	0.6860	0.4217
0.5	0.8424	0.6860
0.2	0.9370	0.8740
0.1	0.9685	0.9370
0.05	0.9842	0.9685
0.02	0.9937	0.9874
0.01	0.9968	0.9937

From Table 1 it is plain to see that when the grid fingers are much longer than the spacing between them (a << b) the modification factor G_t approaches unity.

An alternative method of optimizing the collector grid structure of a solar cell was proposed by Serreze in 1978 [58]. This method considers both a single unit cell of the larger collector grid structure, and the larger grid structure layout and design [58]. The method assumes that the solar cell operating point, that is the values of J_{mpp} and V_{mpp}, is already known [58]. Using these cell characteristics, the ohmic power losses (I^2R) due to the sheet resistance of the solar cell , and the collector grid can then be calculated as a function of the geometric and material parameters of the grid; namely finger width, finger spacing, bus-bar width, number of bus-bars, metal sheet resistivity, and solar cell sheet resistivity. Furthermore, the power losses due to shadowing of active area by the collector grid can also be considered in the optimization process. Serreze also considered the effects that the larger grid structure layout has on power losses due to such parameters as the number and location of bus bars [58]. A similar study of the multi-level architectural considerations of optimal collector grid design was also carried out by Flat and Milnes [59], and by Basore [60].

A more detailed explanation and expansion of the above method introduced by Serreze can be found in [59] and in work conducted by Gessert and Coutts [61]. It is on these works that the model employed in this effort is based.

2.6.4. Derivation of grid optimization model

The method of modeling presented here relies on minimizing the power lost due to ohmic and shadowing losses in a unit cell of the collector grid structure. As can be seen in Figure 20, the collector grid being considered can be broken down into a single unit cell. Each of the unit

cells in turn collects the current from a small portion of the solar cell and delivers that current to the bus bar.

In this model, it is assumed that 1-dimensional current flow occurs in the conductive top layer of the solar cell (blue) in the direction of y toward the grid finger of width W_F. Through 2-D numerical simulation , it has been shown that this assumption is not entirely correct, but the error introduced is reasonably small for solar cells operating at 1-sun illumination [62]. It is also assumed that no current flows directly to the bus-bar from the active area of the unit cell. This was previously shown to be a reasonable assumption as evidenced by the correction factors found in Table 1 [57].

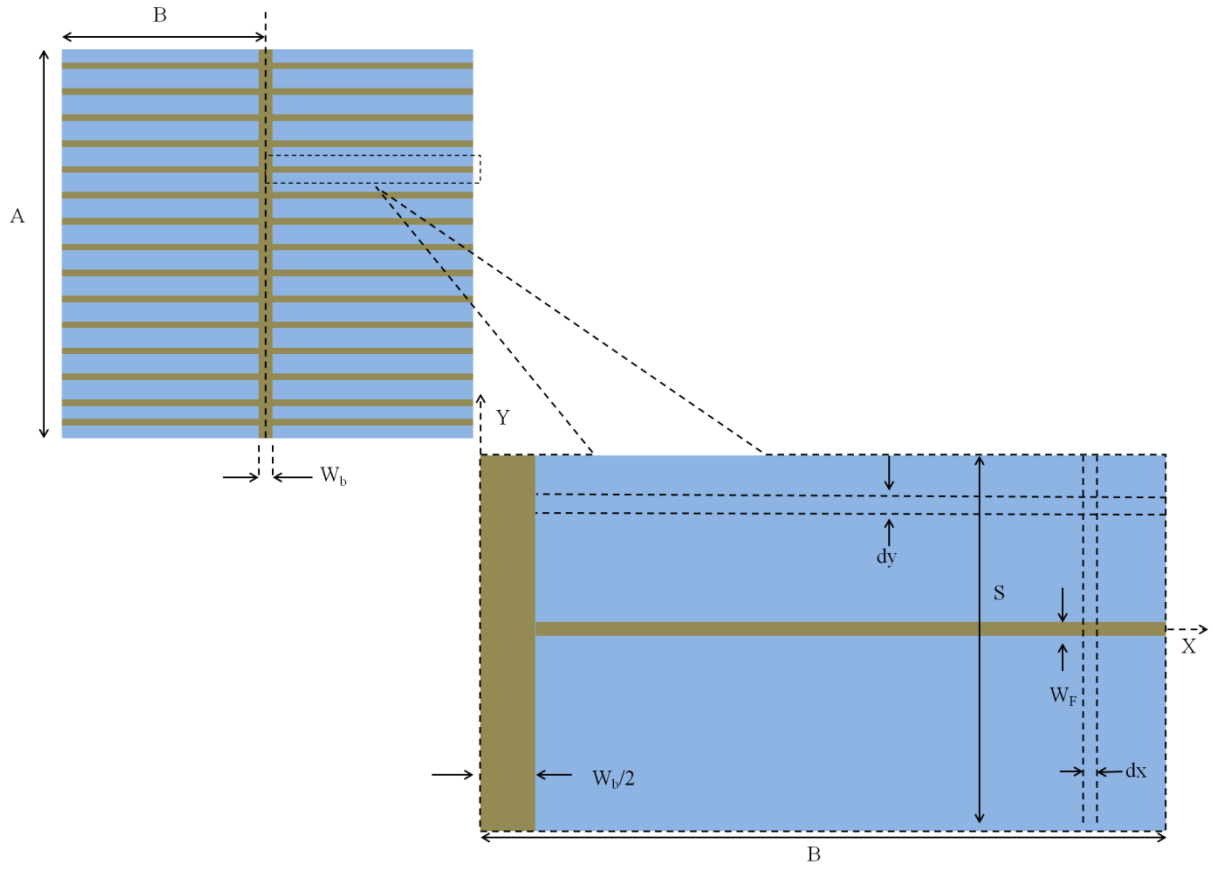


Figure 20. Left: A diagram defining the cell and collector grid dimensions. Right: Close up of a unit cell of the collector grid, containing one grid finger and the surrounding area from which it collects current.

Finally, the operating point, J_{mpp} and V_{mpp} of the cell is assumed to be a known value. J_{mpp} and V_{mpp} are considered to be constant throughout the active area of the cell. With this in mind, it becomes clear that the current flowing within the top layer of the solar cell is exactly zero at a distance of S/2 from the centerline of the grid finger. The current density within the top layer then increases linearly, due to the constant current density generated by the cell, to a maximum value of I_{mt} as illustrated below in Figure 21.

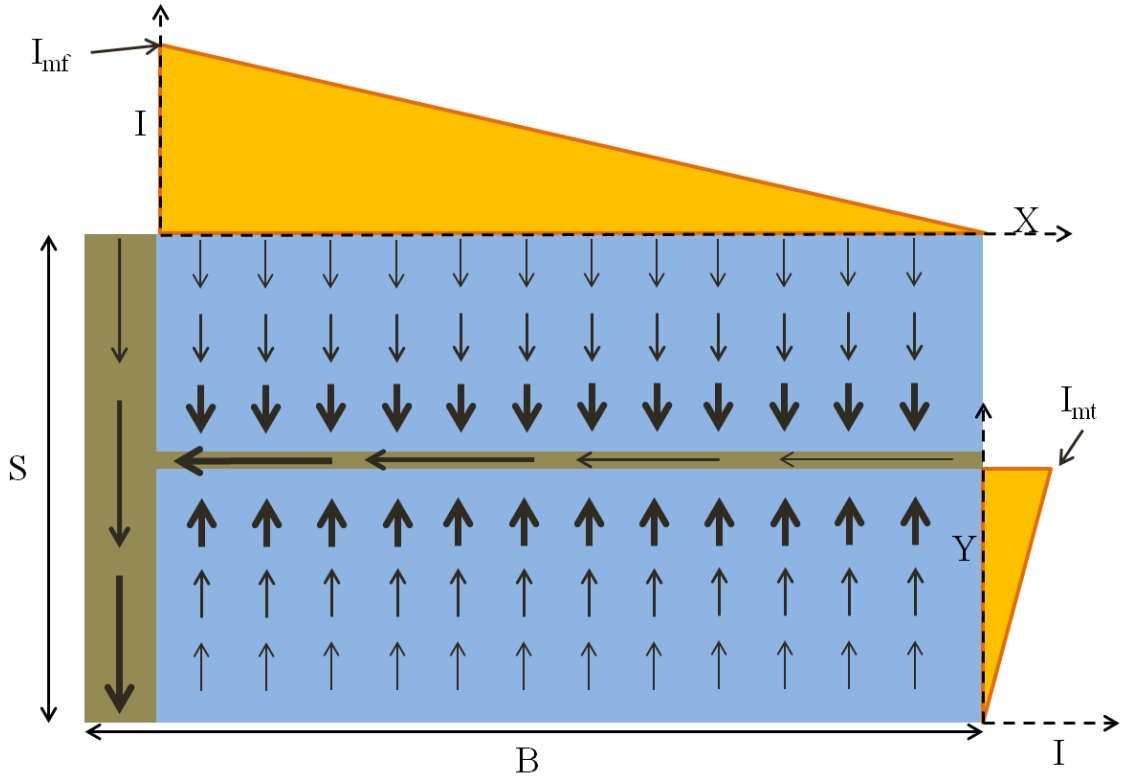


Figure 21. Diagram demonstrating the linear increase in current density both in top conducting layer of the solar cell and along a collector finger.

The value of I_{mt} is calculated in Eq. (6):

$$I_{mt} = J_{mpp}\left(B - \frac{W_b}{2}\right)\frac{(S - W_F)}{2} \tag{6}$$

A similar trend is observed in the current flow within the collector finger which has zero current at the very tip and increases linearly to a maximum value shown in Figure 21. A similar expression for the I_{mf} is given in Eq. (7):

$$I_{mf} = J_{mpp}\left(B - \frac{W_b}{2}\right)(S - W_F) \tag{7}$$

Using variations of Eq. (6) and Eq. (7) along with basic integration, it is possible to derive power loss terms for the unit cell based on its dimensions, material properties, and the assumed current density and operating voltage.

2.6.4.1. Power Loss in the Top Layer of the Solar Cell

As was seen previously, the current flowing in the top layer of the cell depends on y. As such, an expression for the current can be written as follows:

$$P_E = I^2 R_E = \int_{W_F/2}^{S/2} I^2(y)\, dR_E(y) \tag{8}$$

From Eq. (8) we can see that both current and resistance a function of the y-coordinate, and can be written as:

$$I(y) = J_{mpp}\left(B - \frac{W_b}{2}\right)\left(\frac{S}{2} - y\right) \tag{9}$$

$$dR_E(y) = \rho_E \frac{dy}{\left(B - \frac{W_b}{2}\right)} \tag{10}$$

where ρ_E is the sheet resistivity (Ω/□) of the top layer of the cell. Eq. (9) and Eq. (10) can then be placed into the integral of Eq. (10) and evaluated resulting in Eq. (11):

$$P_E = \rho_E J_{mpp}^2 \left(B - \frac{W_b}{2}\right)\left(\frac{S^3}{12} - \frac{S^2 W_F}{4} + \frac{S W_F^2}{4} - \frac{W_F^3}{12}\right) \tag{11}$$

It should be noted that this expression was multiplied by two to account for the power loss from both halves of the unit cell.

2.6.4.2. Power Loss Due to Contact Resistance between the Collector Grid and the Top Cell Layer

The power loss due to the finite contact resistance between the grid finger and the top layer of the cell can be calculated assuming the current is constant, and the contact resistance is a function of only the line width and transfer length:

$$P_C = 2 * I^2 R_C \tag{12}$$

$$I = J_{mpp}\left(B - \frac{W_b}{2}\right)\frac{(S - W_F)}{2} \tag{13}$$

$$R_C = \frac{\sqrt{\rho_C \rho_E}}{\left(B - \frac{W_b}{2}\right)} \coth\left(\frac{W_F}{L_T}\right) \tag{14}$$

where ρ_C is the specific contact resistivity (Ω-cm^2) between the metal and the top layer of the cell, and L_T is the transfer length as obtained from TLM measurements. By substituting Eq. (13), and Eq. (14) into Eq. (12) the total power loss due to contact resistance can be calculated for the unit cell shown below in Eq. (15):

$$P_C = 2 * J_{mpp}^2\left(B - \frac{W_b}{2}\right)\left(\frac{(S - W_F)}{2}\right)^2 (\rho_C \rho_E)^{\frac{1}{2}} \coth\left(\frac{W_F}{L_T}\right) \tag{15}$$

2.6.4.3. Power Loss Due to Ohmic Losses in Grid Finger

The power losses due to the finite resistance of the collector fingers can be calculated in a similar fashion to the losses associated with the top layer of the cell. However, this time the current density and resistance are both a function of the x- coordinate, along the length of the finger:

$$P_F = I^2(x)R_F(x) = \int_{\frac{W_b}{2}}^{B} I^2(x)dR_F(x) \tag{16}$$

$$I(x) = J_{mpp}(S - W_F)(B - x) \tag{17}$$

$$dR_F(x) = \frac{\rho_m dx}{W_F h_F} \tag{18}$$

where ρ_m is the bulk resistivity (Ω-cm) of the metal grid, and h_F is the average height of the grid finger. By substituting Eq. (17), and Eq. (18) into Eq. (16) the total power loss due to finger resistance can be found for a unit cell yielding Eq. (19).

$$P_F = \frac{\rho_m J_{mpp}^2 (S - W_F)^2}{W_F h_F}\left(\frac{B^3}{3} - \frac{B^2 W_b}{2} - \frac{B W_b^2}{4} + \frac{W_b^3}{24}\right) \tag{19}$$

2.6.4.4. Power Loss Due to Resistance of the Bus Bar

The power loss due to the finite resistance of the bus bar can be calculated in a similar fashion to the power losses in the grid finger. The expression for the power loss in a bus bar can be seen below in Eq. (20).

$$P_b = I^2(y)R_b(y) = \int_0^A I^2(y)dR_b(y) \tag{20}$$

$$I(y) = J_{mpp}(2B - W_b)(A - y) \tag{21}$$

$$dR_b(x) = \frac{\rho_m dy}{W_b h_b} \tag{22}$$

where h_b is the height of the bus bar. Equation (21) and Eq. (22) can then be substituted into equation (20), and the power loss in the bus bar can be found yielding Eq. (23).

$$P_b = \frac{\rho_m J_{mpp}^2 (2B - W_b)^2 A^3}{3 W_b h_b} \tag{23}$$

2.6.4.5. Power Loss Due to Shadowing

The power loss due to shadowing is calculated using J_{mpp} and V_{mpp}. An expression for the power loss in a unit cell due to shadowing caused by the grid finger can be seen below in Eq. (24).

$$P_{FS} = J_{mpp}V_{mpp}\left(B - \frac{W_b}{2}\right)(W_F^*) \tag{24}$$

where W_F^* is the optical width of the finger. A similar expression can be written for the busbar of the cell yielding Eq. (25).

$$P_{bS} = J_{mpp}V_{mpp}(A)(W_b^*) \tag{25}$$

where W_b^* is the optical width of the busbar, which is usually considered to be equal to the geometric width of the busbar, W_b.

2.6.4.6. Normalization of the Power Loss Terms

All of the power loss terms, Equations (11), (15), (19), (23), (24), (25) can be normalized to determine the fractional power loss of each loss component. The total power that could be generated by the entire solar cell is expressed in Eq. (26):

$$P_{total,cell} = 2 * J_{mpp}V_{mpp}AB \tag{26}$$

The power loss due to the bus bar can be normalized to Eq. (26) resulting in a fractional power loss due to the bus bar. The sum of Eq. (23) and Eq. (25) will be divided by Eq. (26) yielding Eq. (27):

$$\begin{aligned}\Delta P_{b,total} &= \frac{P_{bS}}{P_{total,cell}} + \frac{P_b}{P_{total,cell}} = \Delta P_{bS} + \Delta P_b \\ &= \frac{W_b}{2B} + \frac{\rho_m J_{mpp}(2B - W_b)^2 A^2}{6W_b h_B V_{mpp} B}\end{aligned} \tag{27}$$

$\Delta P_{b,total}$ is the fractional power loss due to the busbar, ΔP_{bS} is the fractional power loss due to shading by the bus bar, and ΔP_b is the fractional power loss due to ohmic losses in the bus bar. The roots of Eq. (27) can then be found to minimize the power loss due to the bus bar, taking into account both the shadowing losses and the ohmic losses. Once this process has been carried out, the same can be done to minimize the power losses associated with the unit cell.

$$P_{total,\ unit-cell} = J_{mpp} V_{mpp} S \left(B - \frac{W_b}{2}\right) \tag{28}$$

The sum of Equations (11), (15), (19), (24) can then be normalized by Eq. (28) yielding Eq. (29 a,b):

$$\Delta P_{F,total} = \frac{P_E + P_C + P_F + P_{FS}}{P_{total,\ unit-cell}} = \Delta P_E + \Delta P_C + \Delta P_F + \Delta P_{FS} \tag{29 a}$$

$$= \frac{\rho_E J_{mpp}}{12 V_{mpp} S}(S^3 - 3S^2 W_F + 3S W_F^2 - W_F^3)$$

$$+ \frac{2 J_{mpp}(s - W_F)^2}{V_{mpp} S}(\rho_C \rho_E)^{\frac{1}{2}} \coth\left(\frac{W_F}{L_T}\right)$$

$$+ \frac{\rho_m J_{mpp}(S - W_F)^2}{24 W_F h_F V_{mpp} S \left(B - \frac{W_b}{2}\right)}(8B^3 - 12B^2 W_b - 6B W_b^2 + W_b^3)$$

$$+ \frac{W_F^*}{S} \tag{29 b}$$

where $\Delta P_{F,\ total}$ is the total fractional power loss due to the grid finger, ΔP_E is the fractional power loss due to the sheet resistance of the unit cell, ΔP_C is the fractional power loss due to the contact resistance in the unit cell, ΔP_F is the fractional power loss due to the ohmic losses of the grid finger, and ΔP_{FS} is the fractional power loss due to shadowing caused by the grid finger. The roots of the expression in Eq. (29 b) can then be found with respect to S, which will in turn minimize the power loss function. From this model it is then possible to examine the

effects of the specified material and cell properties and cell dimensions on the power loss experienced by the cell. The end result then will be an optimized grid structure that minimizes the power loss for a given set of parameters.

2.7. Grid Deposition Methods

2.7.1. Screen printing technology

As was previously indicated, one of the critical parts of efficient cell operation is the current collector grid. It was the introduction of the collector grid in the 1950's that helped to break the 6% efficiency mark. However, the difficulty of making adequate electrical contact to a silicon solar cell poses many challenges. The current widely utilized high throughput industrial method for depositing collector grids as well as the back contact of solar cells is screen printing. The basic process starts with the creation of a mask which is bonded to a metal screen. The resulting stencil is placed in close contact with the solar cell, and a squeegee pushes metallic paste through the stencil depositing it onto the solar cell in the prescribed pattern (Figure 22). Using this basic method, collector fingers of around 90-150 µm wide and an average height of ~12 µm can be produced from a mask having a stencil opening of 100-120 µm wide [63].

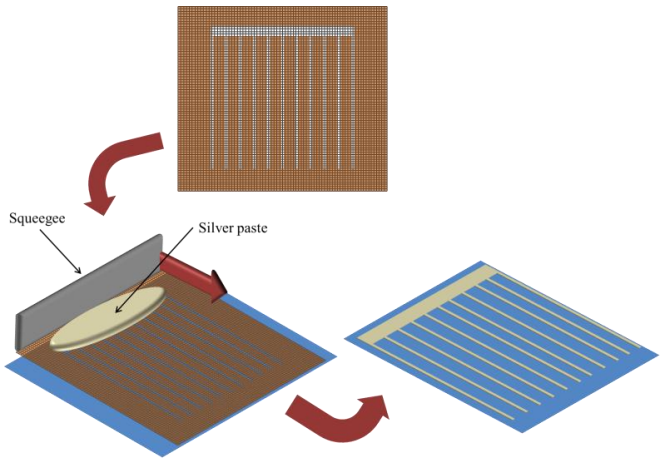


Figure 22. Schematic of the screen printing process.

There has been a strong push toward producing narrower collector fingers using specialized versions of this process to decrease resistive and shadowing losses within the finished solar cell. As a result of these efforts, the average line width used in production solar cells is dropping to 80-100 μm wide [64, 65]. One of the main limiting factors of this process is the minimum wire diameter that can be used to create the mesh. This limits the smallest mesh opening and thus minimum resolution. Current meshes utilize wires in the 20-25 μm diameter range but this is expected to drop to around 18 μm and maybe as low as 10 μm with the introduction of new stronger metal alloys [64]. Although reducing the line width allows closer spacing of the collector lines without increased shadowing, it is still necessary to minimize the resistance of each line by keeping its cross-sectional area as high as possible. The aspect ratio, defined as the ratio of the average height of the line to the width of the line (h/w), should then be as high as possible. Several techniques for increasing the aspect ratio of collector lines have been developed including heated printing, double printing (DP), and Light Induced Plating (LIP) processes [63, 64, 65, 66].

2.7.1.1. Heated Printing

The most basic of the improved screen printing methods involves simply carrying out the screen printing process on a preheated solar cell [63]. This reduces the post deposition spreading of the metal paste, maintaining a high aspect ratio. In their paper, Erath et al. were able to demonstrate line widths as narrow as 52 μm having aspect ratios of 0.15 [63]. Another method, developed at Ferro Inc. involves using metal paste inks containing binders with melting points from 50-80°C along with specialized heated screen printing equipment [66]. With this process grid finger widths as narrow as 60 μm have been achieved with aspect ratios ranging from 0.2 to a maximum of 0.26 [67].

2.7.1.2. Double Printing

Another method for printing high aspect ratio collector lines is by using the double print (DP) method [65, 68]. In its simplest form, this method consists of printing one layer directly on top of a base layer [65, 68]. Another method utilizes two different pastes, one specially formulated for making strong electrical contact to the solar cell, and another formulated for high conductivity is more promising [65, 68]. Aspect ratios of up to 0.36 have been reported utilizing this form of the DP method [65]. Images comparing standard single print to double print lines can be seen in Figure 23.

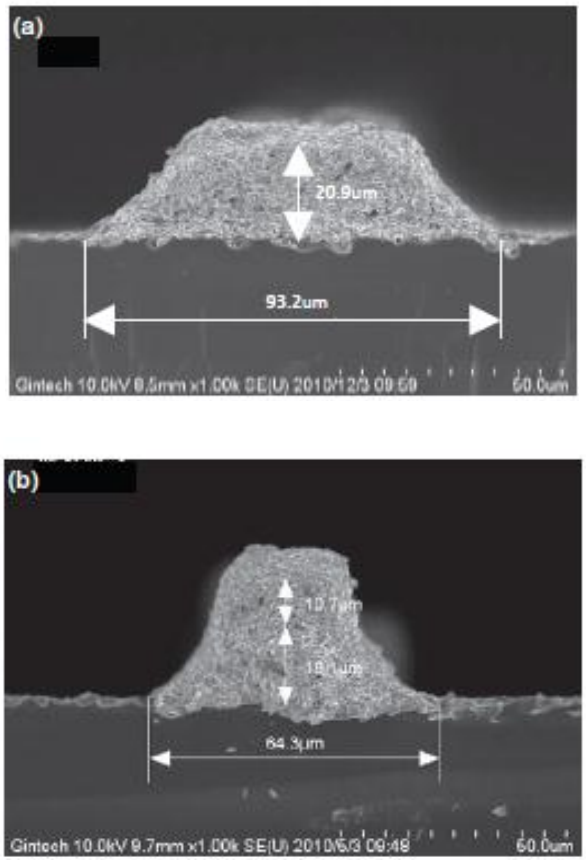


Figure 23. Comparison of line cross section for single print screen printed contact (a) and double print screen printed contact (b). Adapted from [68].

2.7.1.3. Light Induced Plating (LIP)

The very nature of a solar cell makes it especially amenable to an electroplating process designed to bolster the conductivity of the current collector grid. In the most basic form of the LIP process the solar cell is placed in an electrolytic bath with a silver anode [69, 70]. The back contact of the cell is protected by applying a voltage relative to the silver anode [69, 70]. A light is then shown on the cell and the front collector grid develops a negative voltage, thus causing the positive silver ions to deposit on the grid [69, 70]. A "seed layer" of conductor, in this case silver, must first be applied to the cell using a method such as screen printing [68, 69].

Substantial increases in electrical properties and cell performance have been reported in [69] and [70] including a 3.2% absolute efficiency increase for one test cell. This is mainly due to the drastic increase in collector line cross-sectional area that occurs as a result of the LIP process as shown below in Figure 24.

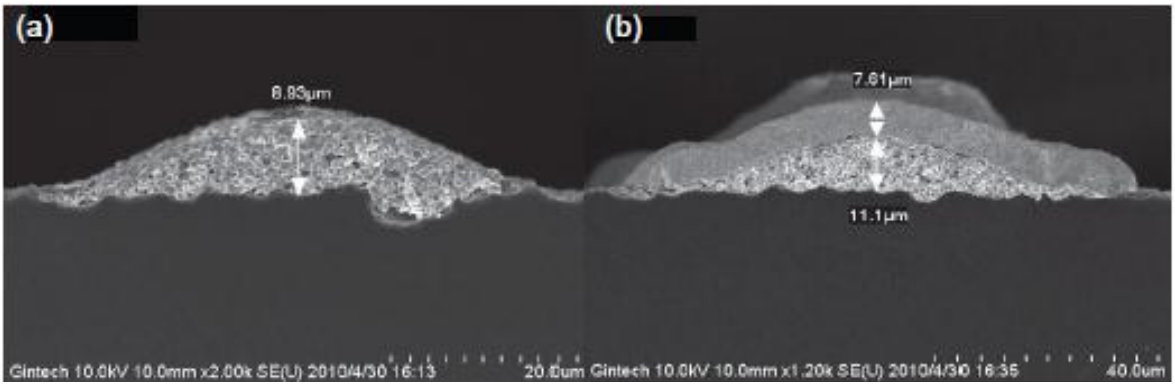


Figure 24. SEM image of (a) screen printed seed layer, (b) plated seed layer. Adapted from [68].

One drawback of this technology, as can been seen above in (b) of Figure 24, is that the conductor growth is nearly isotropic, and thus an increase in line width occurs along with an increase in line height. It can also be seen from the above images that the electroplated silver is much denser than the screen printed silver, resulting in a bulk resistivity decrease of the

conductor lines from 4.3 μΩ-cm down to 2.56 μΩ-cm [68]. The combined effect of the increased cross-sectional area, and decreased bulk resistivity leads to an increased cell fill factor and overall higher cell efficiency.

2.7.2. Ink jet printing

Ink jet direct write technology, initially patented in the 1950's is perhaps most familiar from its use in home desktop printers [71]. However, this tool has proven extremely versatile as a direct write system, and has found many uses in the manufacture of electronics [72]. There are two basic types of inkjet, continuous ink jet (CIJ) and drop on demand inkjet (DOD) [72]. In CIJ, the print head produces a constant stream of droplets, each of which is either deflected onto the substrate usually via electrostatic force (as shown below in Figure 25), or deflected into a catch basin and re-circulated into the ink supply [71, 72].

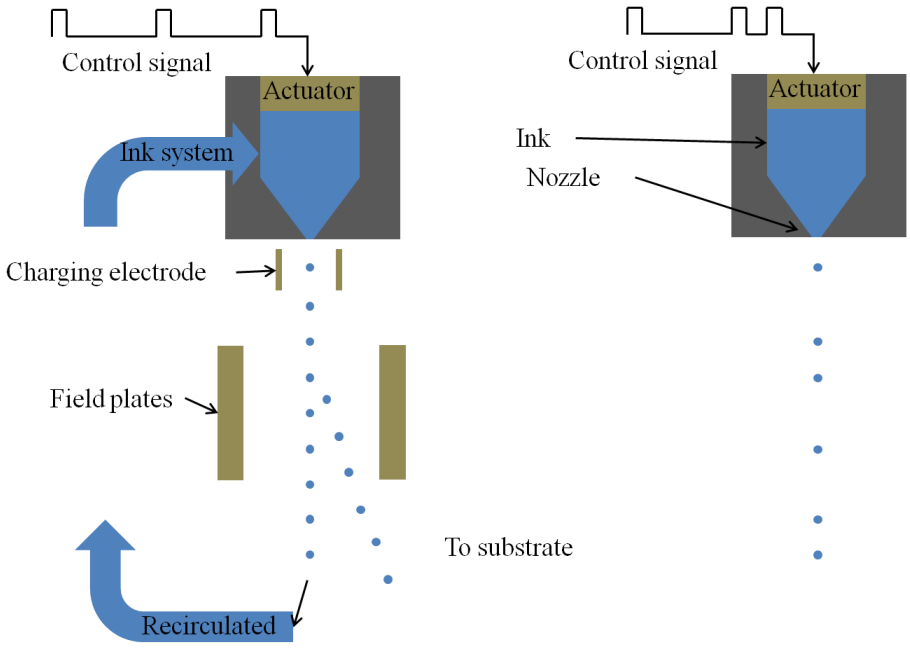


Figure 25. Schematic of Continuous Ink Jet (CIJ) (Left) and Drop On Demand (DOD) ink jet printing (Right). Adapted from [73].

By comparison, DOD printing only produces a droplet when needed [71, 72]. An in-depth discussion of the physics of inkjet printing and details of their operation can be found elsewhere [72], but it is important to note that the general ink jet printing process is limited with regard to the inks that can be printed. Not only must the ink have the proper physical properties necessary to deposit using ink jet, mainly viscosity, but it also must have the desirable electrical and mechanical properties necessary for the intended application [74]. Thus it is necessary to balance the desired electrical and geometric properties with properties that directly affect printability.

To meet these material needs, efforts for metallizing solar cells via ink jet have made use of both metalorganic (MO) and nanoparticle inks as their material feedstock [74, 75, 76, 77, 78, 79, 80]. However, a general trend of wide and low aspect ratio depositions has been seen in all efforts (see Table 2). It should be noted that all efforts toward metallizing solar cells utilized DOD ink jet to the exclusion of continuous ink jet.

Table 2. Typical geometric characteristics of collector grid lines deposited on solar cells via ink jet.

	Line Width (μm)	**Line Height (μm)**	**Aspect Ratio (H/W)**
NREL [79]	80-120	0.4-4.5 (with multiple passes)	0.005-0.0375
Fraunhofer ISE [80]	38	5	0.13
IMPIKA [74]	80	~1	0.0125

Researchers at Fraunhofer ISE are currently working on increasing the aspect ratio of their inkjet depositions by the addition of a light induced plating step [80] in the same fashion as mentioned previously. The aspect ratio can also be increased by depositing onto pre-heated

substrates, which speeds the drying of the metal inks reducing the amount of ink spreading. Typical deposition temperatures in such cases range from 90°C to 200°C [74, 80]. Depositing on a heated substrate can further be combined with printing in multiple layers to achieve high aspect ratio depositions [76, 80]. This process is particularly suited to DOD inkjet in that most DOD print heads consist of arrays of nozzles of similar diameters and known spacing. Thus it is possible to make multiple deposits in a single pass [80]. The parallel nature of ink jet also increases its throughput to industrial rates despite relatively low print speeds of ~28 mm/s [76] (see Figure 26).

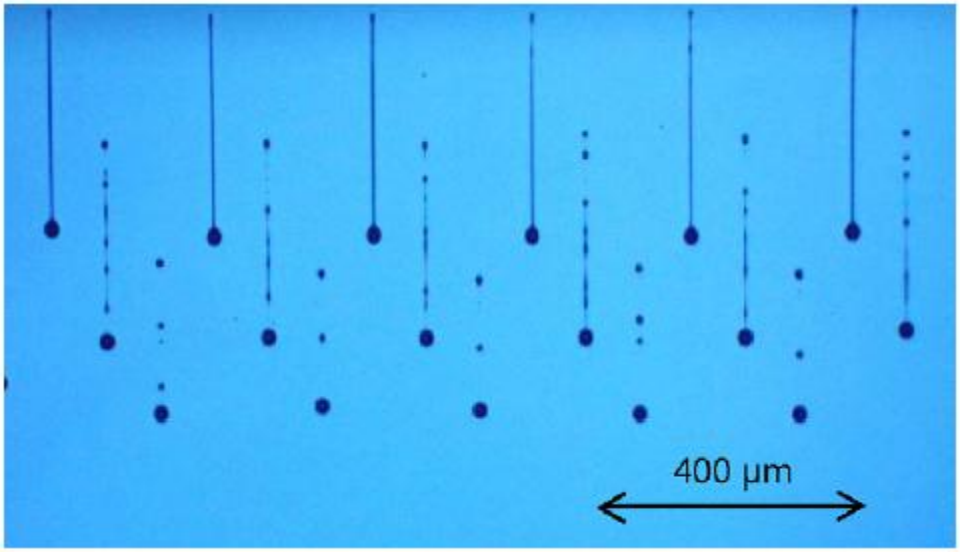


Figure 26. High speed image of three groups of droplets jetted from an array of DOD ink jet nozzles. Adopted from [73].

2.7.3. Aerosol Jet printing

Aerosol Jet (formerly M^3D) printing was developed by Optomec (Albequerque, NM) for the Defense Advanced Research Projects Agency-Mesoscale Integrated Conformal Electronics (DARPA-MICE) program [81]. The technology is unique from ink jet in that it relies on the aerodynamic focusing of an aerosol consisting of ink droplets entrained in a carrier gas to form

depositions [81]. The system works by first creating a suspension of ink droplets in the 1-5 µm range either by ultrasonic or pneumatic atomization depending on ink viscosity [73, 81]. The aerosol is then fed into a deposition head where a sheath gas is merged around the periphery, forming an annular flow with aerosol rich gas flow in the center of the beam and protective sheath gas on the outside of the beam [73, 81, 82].

The sheath gas serves a dual purpose in focusing the aerosol beam down to a minimum width of ~10 µm [81] and preventing the impact of aerosol droplets on the inner surfaces of the deposition head which would lead to clogging [81]. The aerosol flow then passes through a final converging nozzle before it is deposited onto the substrate [82] (see Figure 27). Features are then produced by translating the substrate via motion controlled stages, with a shutter system used to interrupt the aerosol outflow from the nozzle when deposition is not desired. The maximum print speed is advertised at 200 mm/s [73].

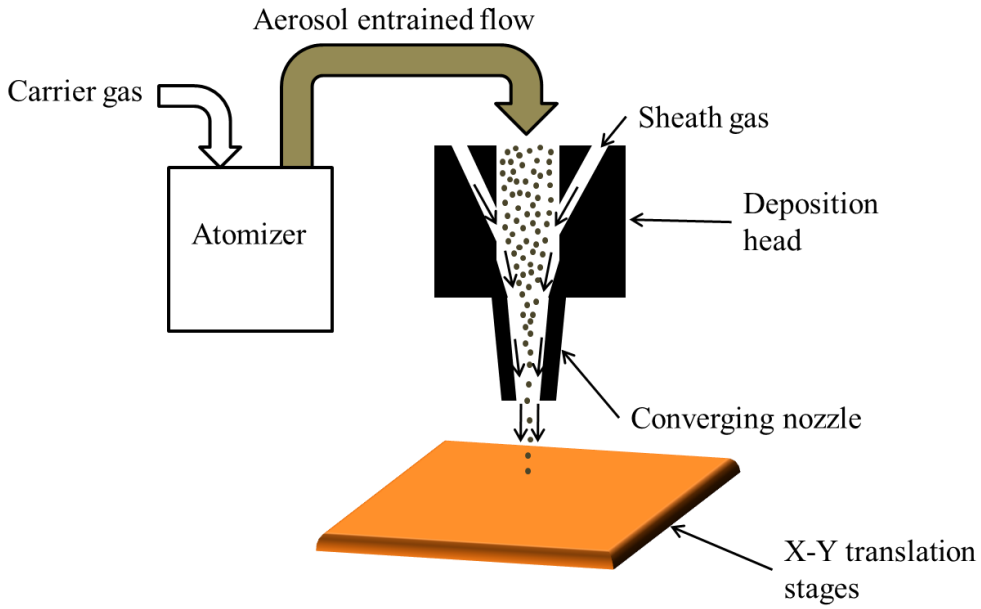


Figure 27. Schematic of the Aerosol Jet deposition system.

One of the added benefits of the Aerosol Jet direct write system, as with most direct write systems, is that it is able to print features that conform to the substrate without making contact. This is especially desirable in the photovoltaics industry where there is a strong push for ever thinner more delicate silicon wafers for decreased materials cost. The direct write advantage has also made the system useful in repairing open circuits in the display industry, as well as printing 3-D interconnects [83, 84]. Furthermore, a wide variety of inks can be deposited using the Aerosol Jet system, with the only limitation stemming from an ability to create a liquid aerosol out of the material feedstock [81].

Using the Aerosol Jet system, a research team working at Fraunhofer ISE was able to deposit what they termed a "seed-layer" of silver ink roughly 30 µm to 40 µm wide and from 1 µm to 5 µm in height [80, 82] (see Figure 28) .

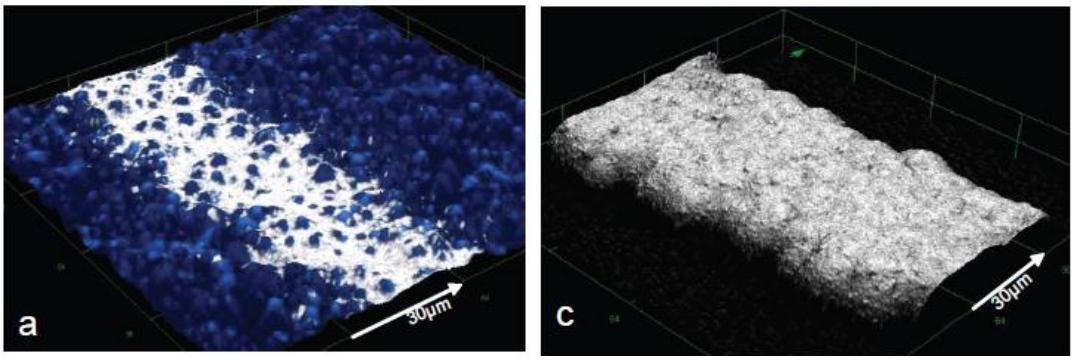


Figure 28. a.)3-D image of seed-layer of silver deposited onto textured crystalline silicon solar cell. c.) 3-D image of same seed-layer after LIP process. Adapted from [80].

The deposited seed-layer was then fired to between 790 °C and 840 °C to allow the silver ink to burn through the ARC layer, making electrical contact to the solar cell [80, 82]. The cells were then subjected to the LIP process to build up a more substantial layer of silver, resulting in finished line widths from ~ 66 µm to ~ 74 µm wide and 12 µm to 22 µm tall depending on process parameters [80, 82]. Due to the isotropic nature of the LIP process, increase in line width

and height occur simultaneously, making narrower seed layers desirable to increase the finished line aspect ratio. In order to make the Aerosol Jet printing process more industrially viable Optomec has developed a 40 nozzle print head that can deposit the seed layer on a 156 mm × 156 mm solar cell in 2.5-3 seconds [73, 85].

2.7.4. Collimated Aerosol Beam Direct Write (CAB-DW)

The Collimated Aerosol Beam Direct Write process (CAB-DW) is a direct write process which was developed at NDSU based on research conducted by Hoey, Akhatov, Schulz and Swenson [86, 87]. The system is based on Optomec's Aerosol Jet system (previously M^3D) , with the addition of a three part nozzle in place of the single converging nozzle usually employed [86, 87]. The CAB-DW nozzle consists of a two converging sections and a diverging section joined as shown in Figure 29.

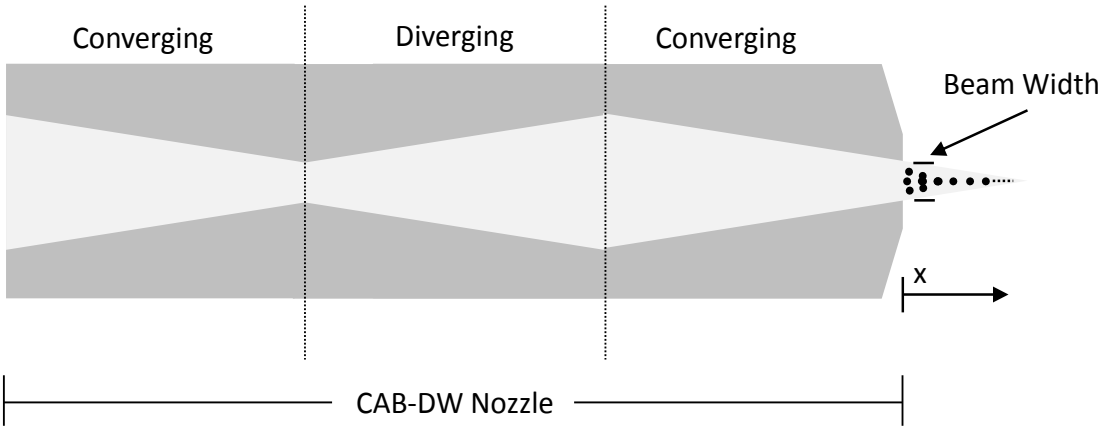


Figure 29. Schematic of CAB-DW nozzle assembly with converging, diverging, and final converging sections. Adopted from [88].

This configuration exploits the aerosol focusing brought about by the Saffman force, which results from a difference between the aerosol particle velocity and the carrier gas velocity [86, 87, 88]. The resulting force depends on the product $(u - u_p)(\partial u/\partial y)$ where u and u_p are the carrier gas velocity and particle velocity in the x direction respectively. For a flow in which

the gas velocity is larger than the particle velocity $(u - u_p > 0)$ the force experienced by the particle is in the direction of increasing velocity (See Figure 30). However, if the particle is traveling faster than the surrounding gas flow $(u - u_p < 0)$ the force will be in the direction of decreasing velocity.

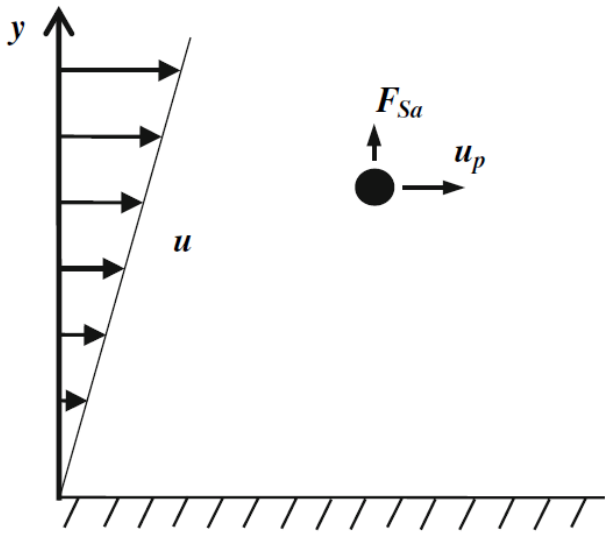


Figure 30. A diagram illustrating the effect of Saffman force on a particle traveling slower than the surrounding gas flow. Adopted from [86].

When the aerosol flow is passed through the converging section of the nozzle, the carrier gas is accelerated causing a velocity difference between the carrier gas and aerosol particles $(u - u_p > 0)$. The resulting Saffman force (F_{Sa}) along with Stokes force will cause the particles to migrate towards the centerline of the nozzle. However, as in a standard nozzle, the aerosol particles will build up momentum and diverge after passing through a focal point as shown in Figure 31(b). By incorporating a diverging section following the converging section, the tendency of the aerosol droplets to diverge after passing through the focal point is damped by a development of an opposing Saffman force $(u - u_p < 0)$. The flow is then passed through a

final converging section (see Figure 31 a) to further accelerate the flow to make a more robust aerosol beam for deposition [86].

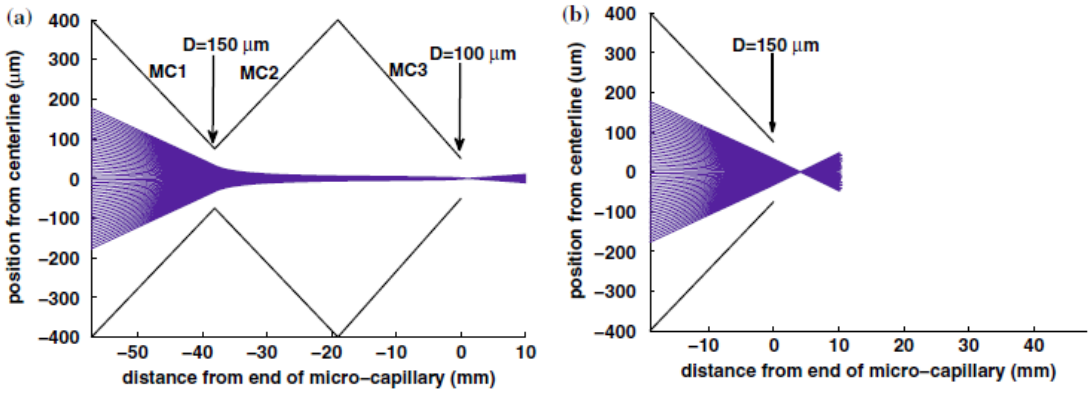


Figure 31. Schematic illustrating aerosol droplet collimation in the CAB-DW nozzle (a), and aerosol focusing in a single linear converging nozzle (b). Adopted from [86].

The end result of employing the CAB-DW is an ability to deposit narrower lines with less overspray. A comparison between a single linear converging nozzle and the CAB-DW nozzle both operating with the same process parameters can be seen in Figure 32.

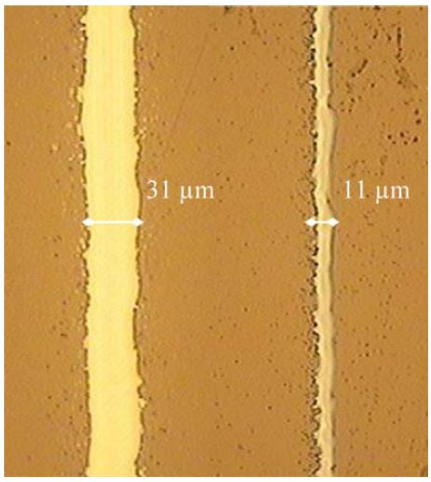


Figure 32. Comparison of silver line deposited with a single converging nozzle (left) and the CAB-DW nozzle (right). Adopted from [86].

As is clear from Figure 32, the CAB-DW system provides the ability to deposit very narrow, continuous lines of metallic inks, making ultra-fine metallization solar cells possible without the use of expensive photolithography and vacuum based processes. In fact, line widths of < 5μm have been realized under certain operating conditions which greatly increase the potential efficiency gains through grid optimization. The scalability and print speed of the CAB-DW system is equivalent to that of the Aerosol Jet system, although it should be noted that the print speed is heavily dependent upon the mass flow rate of the atomization process with typical values in the range of 10 mm/s.

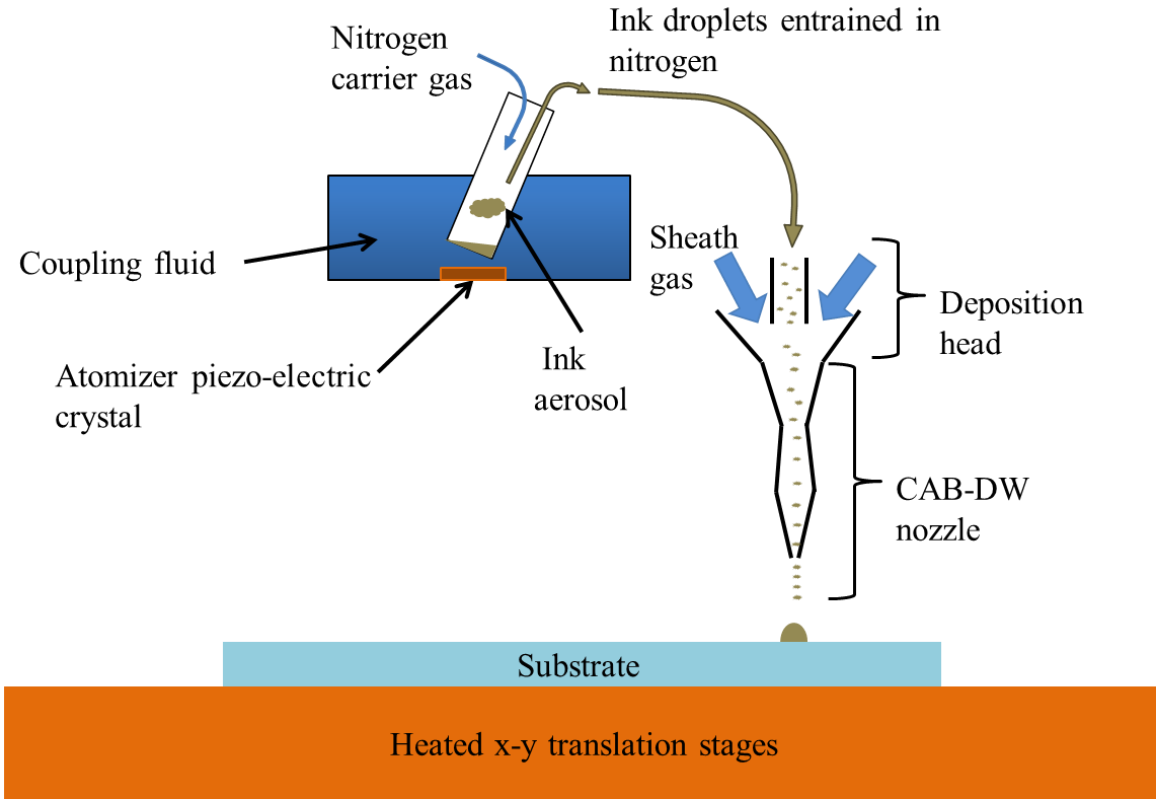


Figure 33. Schematic of the CAB-DW deposition system used at NDSU.

A schematic of the deposition system used for the current research at NDSU can be seen in Figure 33. The system consists of an ultrasonic atomizer which is used to create an aerosol of silver nanoparticle ink in a vial. Dry nitrogen is then fed into the vial, exiting as an entrained

aerosol carrier gas flow. This flow is then fed into the deposition head where it is merged with a sheath gas flow. Both gas flows are controlled with mass flow controllers (mks, model number M100B01312CP1BV). The translation stages are nanometer resolution (Aerotech, model number ALS130) and include a heated platen with a heating range from room temperature to 350 °C.

2.7.5. Dispensing based direct write technology

In addition to the previously mentioned aerosol and droplet based direct write technologies, another promising system for depositing current collector grid fingers is the nScrypt dispensing system. This system was also a product of the DARPA-MICE program [73]. The key innovation of the system is a high precision micro-dispensing pump that can make controlled depositions down to 20 picoliters [73].

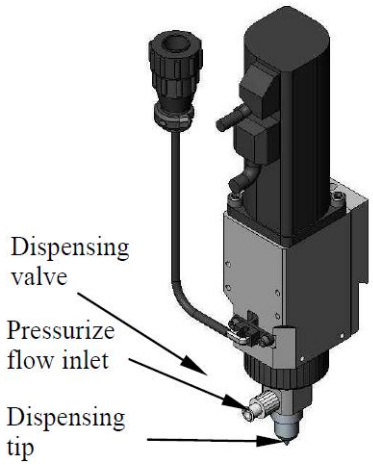


Figure 34. 3-dimensional model of the nScrypt dispensing device. Adapted from [89].

The system is able to make linear high aspect ratio depositions down to 50 µm wide and can deposit at write speeds of up to 300 mm/s [73, 89]. However, the flow rate and resulting line width are extremely dependent upon stand-off distance from the substrate, and therefore

precision z-axis control maintained with the help of a laser ranging system is required [73, 89]. The SEM images in Figure 35 demonstrate the high aspect ratio narrow grid fingers that can be deposited using this technology.

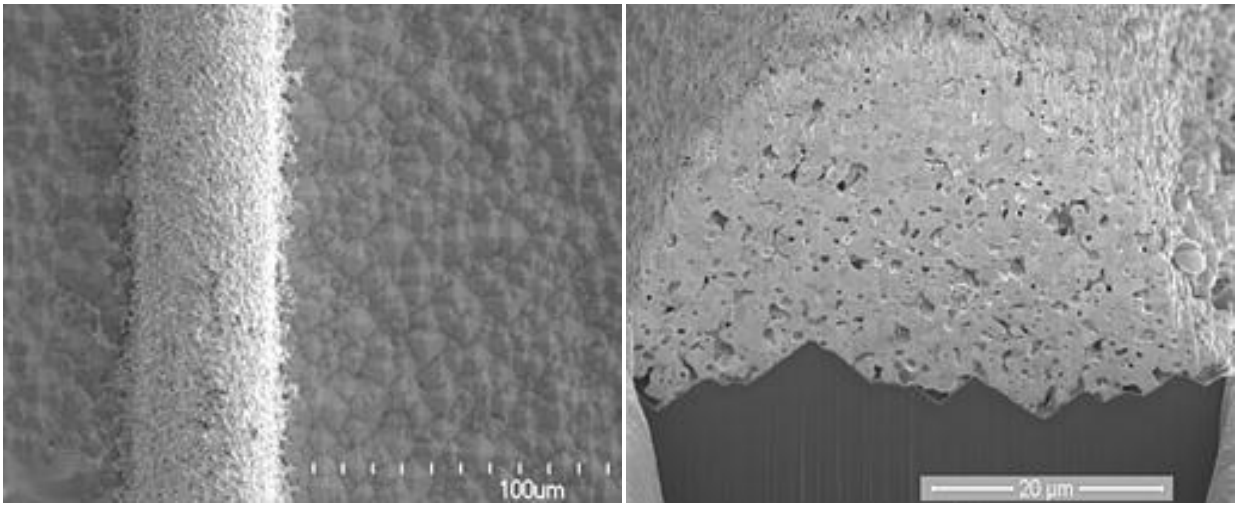


Figure 35. SEM images of nScrypt deposited grid fingers on a solar cell. Adapted from [90].

2.7.6. Cima NanoTech Self Aligning Nanoparticles for Transparent Electrode (SANTE) Coatings

Each of the methods discussed to this point have been centered on deposition methods that produce user-defined grid structures. Self-assembling nano-materials have also found a niche within the solar cell market in the form of SANTE coatings developed and introduced by Cima NanoTech (St. Paul, Minnesota) [91]. The process involves coating the desired substrate with a proprietary emulsion of water, oil, and silver nanoparticles and then allowing the deposition to dry [92]. During the drying process the silver nanoparticles self-assemble into networks of conductive silver as shown in Figure 36. Notice that the resulting grid structure is random in nature. Sheet resistance values of 3.5 Ω/□ have been realized in as-deposited structures, with lower values of 0.01 Ω/□ being demonstrated with plated structures [92].

Shadowing of the substrate can be significant with transmission levels measured to be around 88% for wavelengths between 400 and 700 nm [92]. The chief advantage of this process is found in the ease of material application using conventional processes, making it amenable for roll to roll manufacturing.

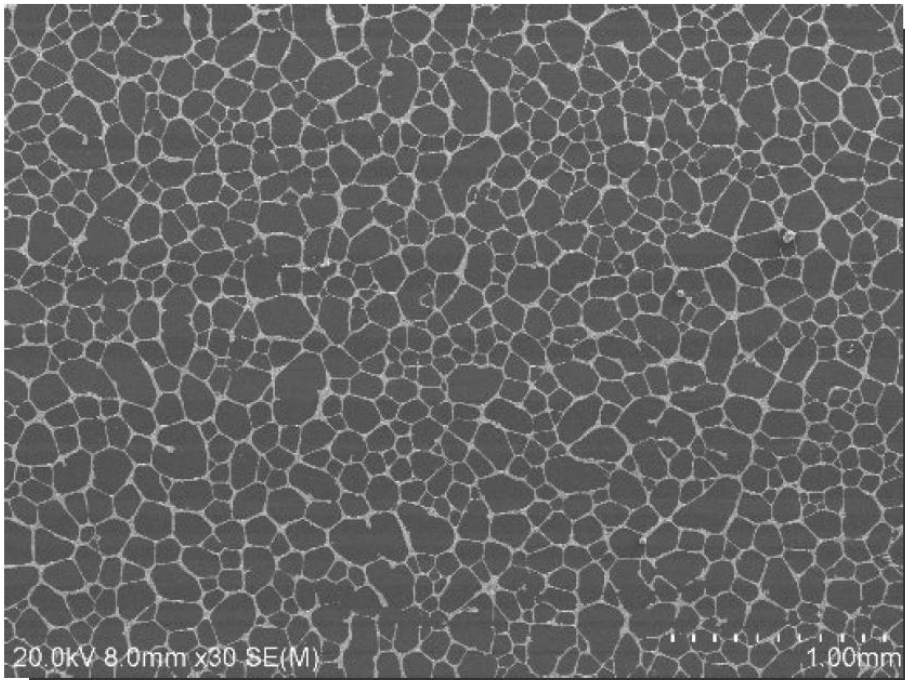


Figure 36. SEM image of conductive silver network produced through the SANTE coating process. Adapted from [92].

2.7.7. Comparison of grid deposition methods using optimized-grid model

In order to better understand the effect of grid finger width and aspect ratio on the efficiency of a solar cell it is helpful to employ the model presented in section 2.6.4. To apply this model, it is necessary to assume material properties such as bulk resistivity (ρ_m) of the deposited grid material, contact resistivity (ρ_C) and transfer length (L_T) between the material and the solar cell, and the sheet resistivity (ρ_E) of the top layer of the solar cell. Furthermore, expected maximum power point values for the current density (J_{mpp}) and voltage (V_{mpp}) must also be specified. The values used in this study can be seen in Table 3.

Table 3. Material and solar cell operating properties used in the geometric analysis of grid deposition methods.

ρ_C	L_T	ρ_m	ρ_E	J_{mpp}	V_{mpp}
0.02 mΩ-cm^2	4 µm	6×10^{-8} Ω-m	60 Ω/□	34 mA/cm^2	0.500 V

The above values were incorporated into the previously derived model along with an aspect ratio of 0.1.

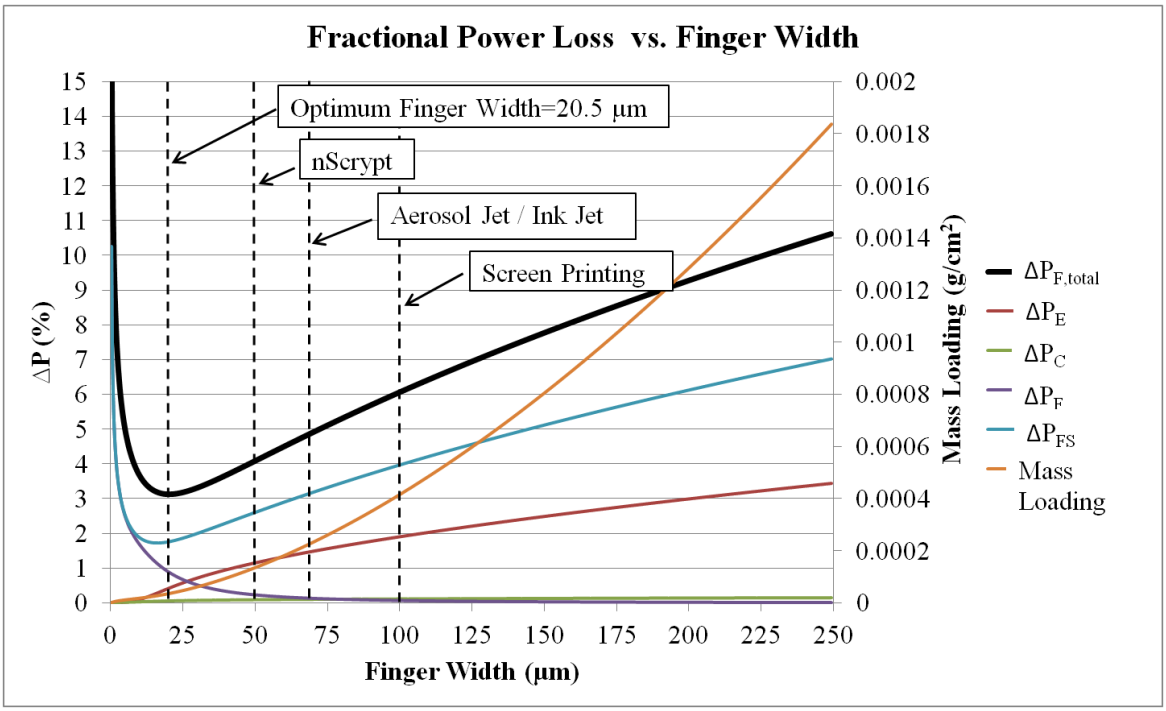


Figure 37. Plot of fractional power loss components and normalized conductor mass calculated for an aspect ratio of 0.1.

The plot above (Figure 37) demonstrates the relationship of each fractional loss parameter in the unit cell of the collector grid. Notice that there is a well-defined minimum fractional power loss which occurs at finger width of ~ 20.5 µm. This clearly demonstrates that for the given cell conditions, which are typical of the NREL SHJ cells being studied, the CAB-DW system holds the advantage of being able to deposit grid fingers < 50 µm in width as long as an aspect ratio of 0.1 can be achieved. The mass loading of conductive material (g/cm^2) also decreases substantially with decreasing finger width, which would result in substantial material

and cost savings. It is also useful to consider the effects of the aspect ratio of the finger on the fractional power loss curve.

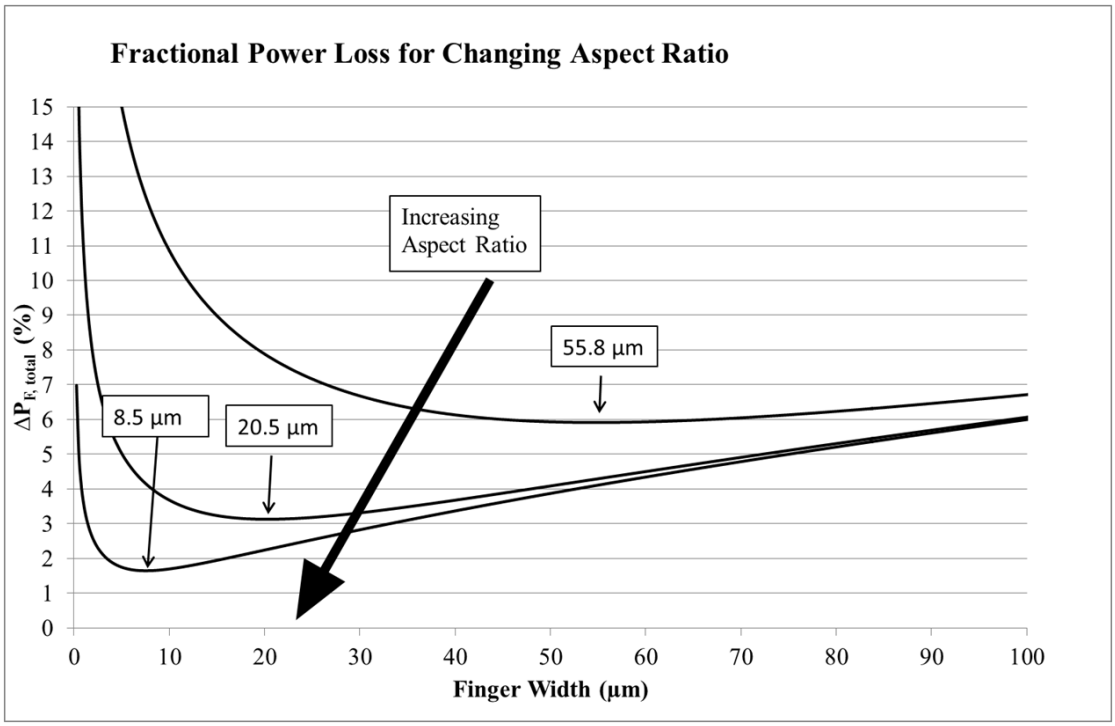


Figure 38. Demonstration of the effect aspect ratio has on the fractional power loss.

The plot above (Figure 38) gives a clear demonstration of the role that finger aspect ratio plays in the fractional power loss of a solar cell. In this plot aspect ratios of 0.01, 0.1 and 1.0 were used along with the previously defined material and electrical properties to calculate the fractional power loss versus finger width. It is clear from Figure 38 that increased aspect ratio significantly decreases the minimum fractional power loss. Increased aspect ratio also decreases the finger width at which the minimum fractional power loss occurs. For an aspect ratio of 0.01, the optimum finger width is around 55.8 µm whereas for an aspect ratio of 1.0 the optimum finger width is less than 8.5 µm.

Finally it is important to demonstrate the effect sheet resistivity has on optimum finger width. The plot below (Figure 39) is the fractional power loss for ρ_E values of 1 Ω/□, 10 Ω/□,

and 100 Ω/□. All other model parameters were as initially assumed, with the aspect ratio defined to be 0.1.

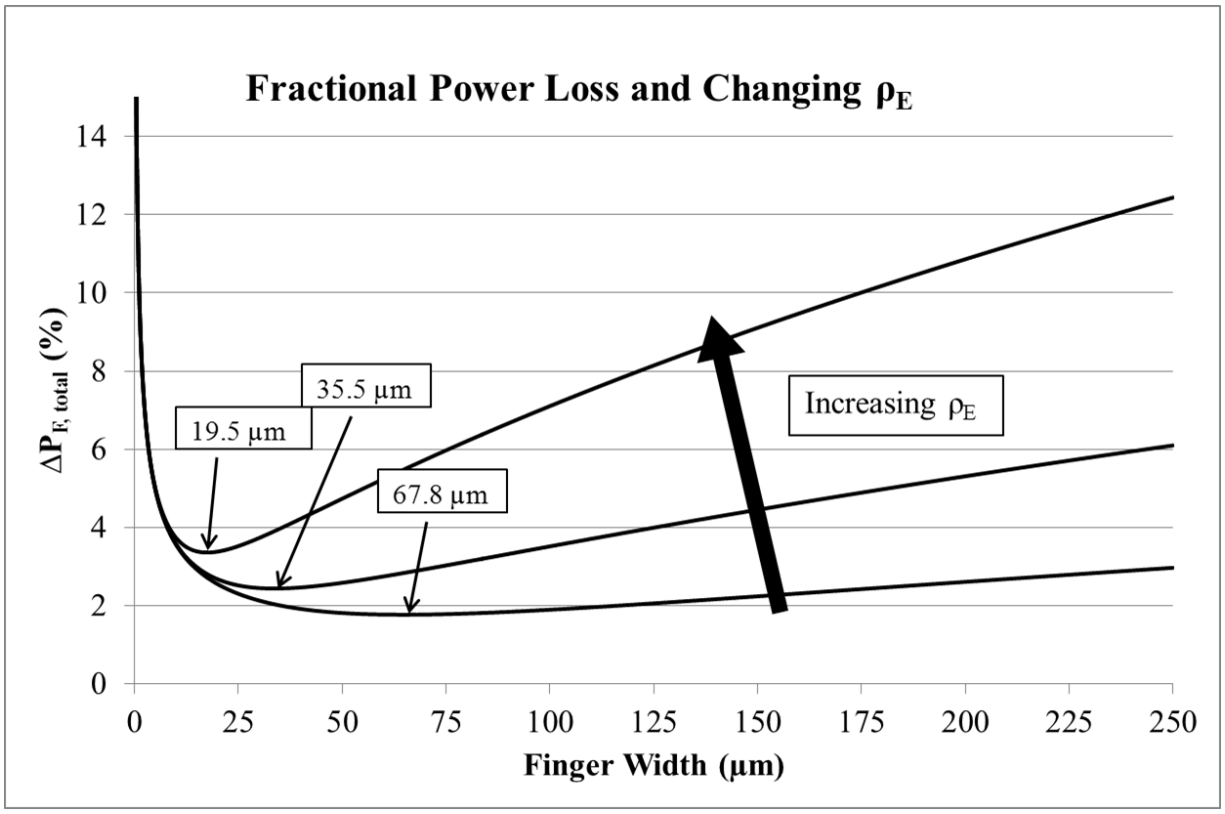


Figure 39. Demonstration of the relation between optimum finger width and ρ_E.

As ρ_E increases, the optimum finger width shifts from around 67.8 µm to only 19.5 µm with a corresponding increase in the fractional power loss of roughly 1.75%. The knowledge gained through this modeling effort serves as a much needed tool to analyze the complex task of designing an optimum grid structure. Although many in literature assume that a narrower grid finger is always an advantage, it is clear from the above results that a careful investigation of all material, electrical and geometric properties must be conducted to arrive at an optimal grid design.

3. DEMONSTRATION OF COLLECTOR GRIDS PRINTED WITH PV-NANOCELL INK

3.1. Optimization of Collector Line geometry

As was discussed previously the shadowing of an encapsulated solar cell can be less than the expected shadowing due to light trapping via internal reflection [50, 51, 52]. By inspection it is logically determined that a triangular cross section collector line is ideal optically to facilitate such light trapping. An investigation was undertaken to determine whether the CAB-DW system could produce near triangular depositions by printing multi-pass patterns. Initially, three different contouring methods were tried in which each of three patterns was printed in differing number and order on top of each other (Figure 40).

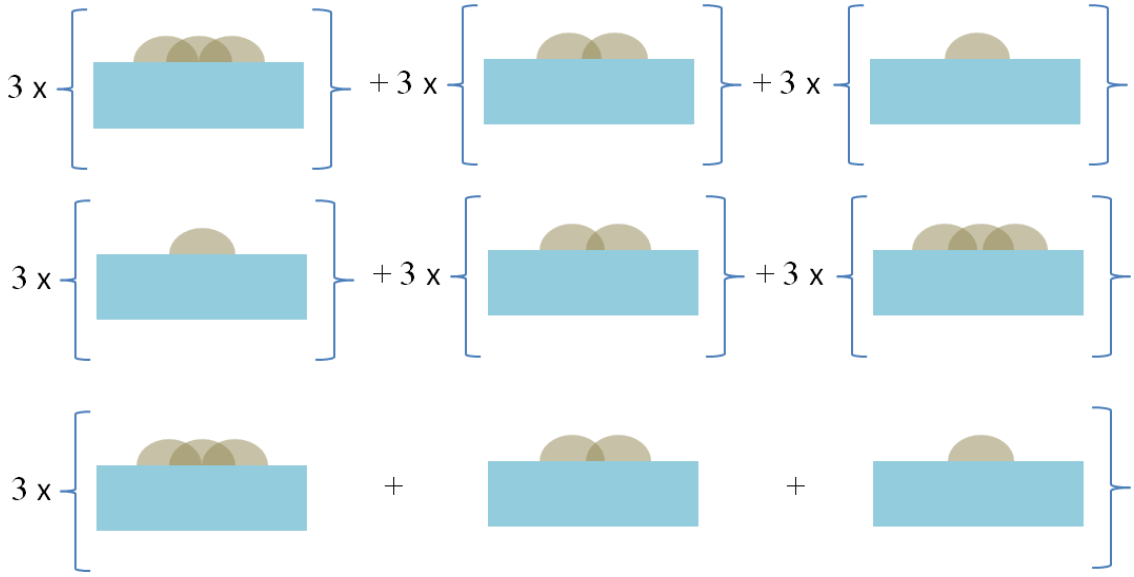


Figure 40. From top to bottom, the deposition schemes of contours 1, 2, and 3.

Each of the above patterns was deposited with PV-Nanocell silver nanoparticle ink (Migdal Ha'Emek, Israel) onto a glass microscope slide substrate heated to 100 °C. In general the ink was mixed in a 1:2 ratio of ink to deionized water in order to achieve atomization. It is

important to state here that the carrier gas flow rate was used to regulate the quality and quantity of the depositions. The flow rates used varied from as little as 10 standard cubic centimeters per minute (sccm) to as high as 25 sccm, depending upon the quality of the atomization process. A sheath gas flow rate of 30 sccm was used almost invariably throughout all of the deposition efforts. It was found that the depositions were generally of the best quality when a carrier gas flow rate of 15 sccm was used, atomization permitting, with very few instances of the system clogging. As a final note, for all of the depositions a print speed of 10 mm/s was used unless otherwise noted.

After depositing each of the above contours the samples were sintered at 250 °C for 1 hour in a N_2 atmosphere. The samples were then measured to obtain their profile (P-15 Longscan Contact Stylus Profiler, KLA-Tencor). Unfortunately, it was determined that the contacts were very wide, at around 50 to 60 µm, and lacked the height to produce sides with the desired critical slope which is clearly shown in Figure 41.

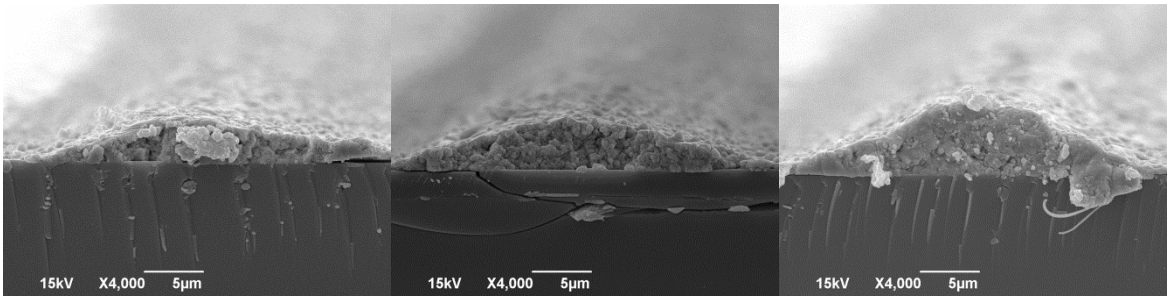


Figure 41. SEM images of contours 1 (left), 2 (center) and 3 (right).

Several new profiling patterns were then made and tested with the intent of increasing the aspect ratio of the resulting depositions (see Figure 42). After printing samples of all three contours shown in Figure 42 the sample were then characterized using the contact profiler. The same printing parameters were used as previously mentioned. Several scans were taken across

each sample and the resulting data was processed using a custom computer code to estimate the optical width of the depositions as well as their cross-sectional area.

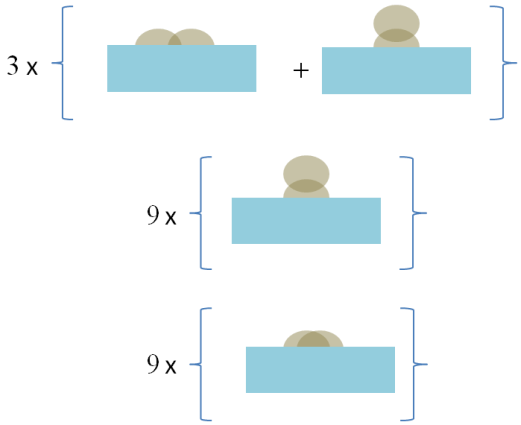


Figure 42. From the top, printing schemes of contours 4, 5, and 6.

The custom program calculates the slope between each profile data point and compares the slope to the critical slope. If the calculated slope is larger than the critical slope (type II), that small section of the line is counted as contributing to internal reflection light trapping. Furthermore, if the slope is large enough to promote direct reflection to the substrate (type I) it is also counted. The length of all such segments is then summed and subtracted from the total line width. The resulting quantity is then divided by the geometric line width, resulting in an effective shadowing coefficient (see Eq. (30)).

$$\frac{W_G - W_R}{W_G} = \frac{W_O}{W_G} = C_S \tag{30}$$

where W_R is the reflective line width, and C_S is the resulting shadowing coefficient. As mentioned previously, the critical angle is a function of the optical properties of the encapsulant materials, in this case glass and ethylene vinyl acetate (EVA). The model used to determine C_S assumes that all reflections are specular, that the EVA encapsulant and glass cover have the same index of refraction of 1.47, the absorption of light is negligibly small, and also ignores the

possibility of multiple reflections. From the data collected using the contact profiler it was decided that contours 5 and 6 created were the best candidates for creating samples which could be characterized via SEM (see Figure 43). Note that all samples in Figure 43 exhibit exceptional aspect ratios.

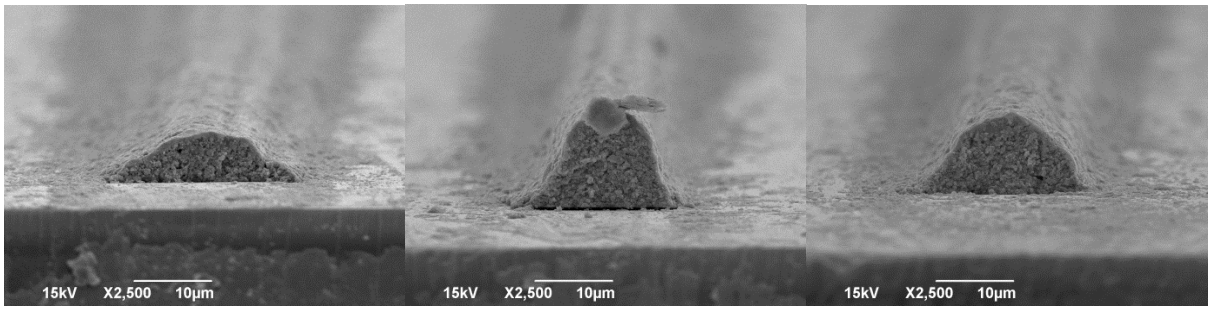


Figure 43. SEM images of contour 4 (left), contour 5 (center), and contour 6 (right).

Although high aspect ratio lines can exhibit a reduced shadowing, the advantageous electrical properties of the increased cross-sectional area corresponding to a high aspect ratio grid finger are very important. As such, an effort was made to deposit high aspect ratio grid fingers in a single printing pass. In order to accomplish this, the substrate was heated to around 150 °C and the print speed was decreased to 1 mm/s.

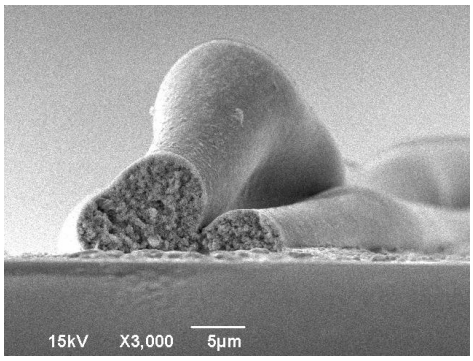


Figure 44. SEM image of a collector line
deposited on a heated substrate in a single pass.

One of the resulting depositions can be seen in Figure 44. Surprisingly complex three dimensional structures were noticed in the finished depositions as is clear from the above image.

This is likely a result of the rapid drying of the deposited aerosol droplets as they impinged on the heated substrate.

3.2. Demonstration of Grid Induced Light Trapping

With this in mind, two samples having roughly 10% area coverage of grid fingers with contour 5 and 6 were printed onto a heated (100 °C - 150 °C) glass microscope slide using PV-Nanocell silver nanoparticle ink. The pattern consisted of a 20 cm × 20 cm swatch, with each line spaced 300 μm from the previous line, resulting in a 42 minute print time per sample. Once these samples were deposited, they were examined using an optical microscope to determine if the proper height and width requirements had been met. They were then sintered at 250 °C for one hour in a N_2 atmosphere. Next, the samples were characterized using the contact profiler and custom program discussed previously. The results for contours 5 and 6 as deposited on their respective samples can be found below in Table 4. From the values of C_S in Table 4 it can be seen that the effective shadowing was predicted to be only about 46% and 52% of the geometric shadowing for contours 5 and 6 respectively following encapsulation.

Table 4. Average properties of printed contacts gathered via contact profilometry.

	Area (μm^2)	**Width (μm)**	**C_S**
Contour 5	199	26.2	0.464
Contour 6	108	27.6	0.529

The samples were then characterized optically to determine reflectance using an integrating sphere (QEX7 Solar Cell Spectral Response/ QE/IPCE, PV Measurements, Boulder CO). Sweeps from 400 nm to 1100 nm were made in step sizes of 10 nm. After the initial characterization, the samples were encapsulated with EVA encapsulant (STR Solar 15295P/UF) and an additional layer of microscope glass. The reflectance characterization was repeated on the

encapsulated samples, and baseline readings were taken of the two types of sample substrates, a blank glass slide and a sandwich of glass and EVA encapsulant (STR Solar 15295P/UF) between two glass microscope slides. This data was then used to normalize the previous tests by removing the reflectance components due to the substrates, leaving only the reflectance due to the deposited lines. The method of normalizing the data can be seen below in Eq. (31) and Eq. (32).

$$R_N = R_{SW} - R_{Sub}(1 - A_C) \tag{31}$$

where R_N is the normalized reflectance before encapsulating the samples, R_{SW} is the reflectance of the swatch sample, R_{Sub} is the reflectance of the substrate, and A_C is the area coverage of the silver lines on the substrate. A_C was determined taking several measurements of line width throughout the finished swatch pattern and determining an average line width. This average line width was then divided by the spacing between each line, in this case 300 μm, resulting in an A_C value of 8.7% and 9.2% for contours 5 and 6 respectively. A similar method was used to normalize the reflectance measurements for the encapsulated samples.

$$R_{NE} = R_{SWE} - R_{ES}(1 - A_C) \tag{32}$$

where R_{NE} is the normalized reflectance of the encapsulated sample, R_{SWE} is the measured reflectance from the encapsulated swatch, R_{ES} is the measured reflectance of encapsulant sandwich substrate, and A_C remains as defined before. The normalized data for both samples before and after encapsulation can be seen below in Figure 45.

It is immediately apparent that a large decrease in reflectance was realized by the encapsulation of contour 5. In fact an average decrease in reflectance of 49% relative from 400 nm to 1100 nm was realized, which corresponds to a C_S of 0.51 after encapsulation. This is in close agreement with the modeled estimate of $C_S \cong 0.464$. However, a similar correlation is not

noticed for contour 6. It is likely that flow or shifting of the EVA occurred during the encapsulation process disrupting the profiles of the lines and thus their optical properties.

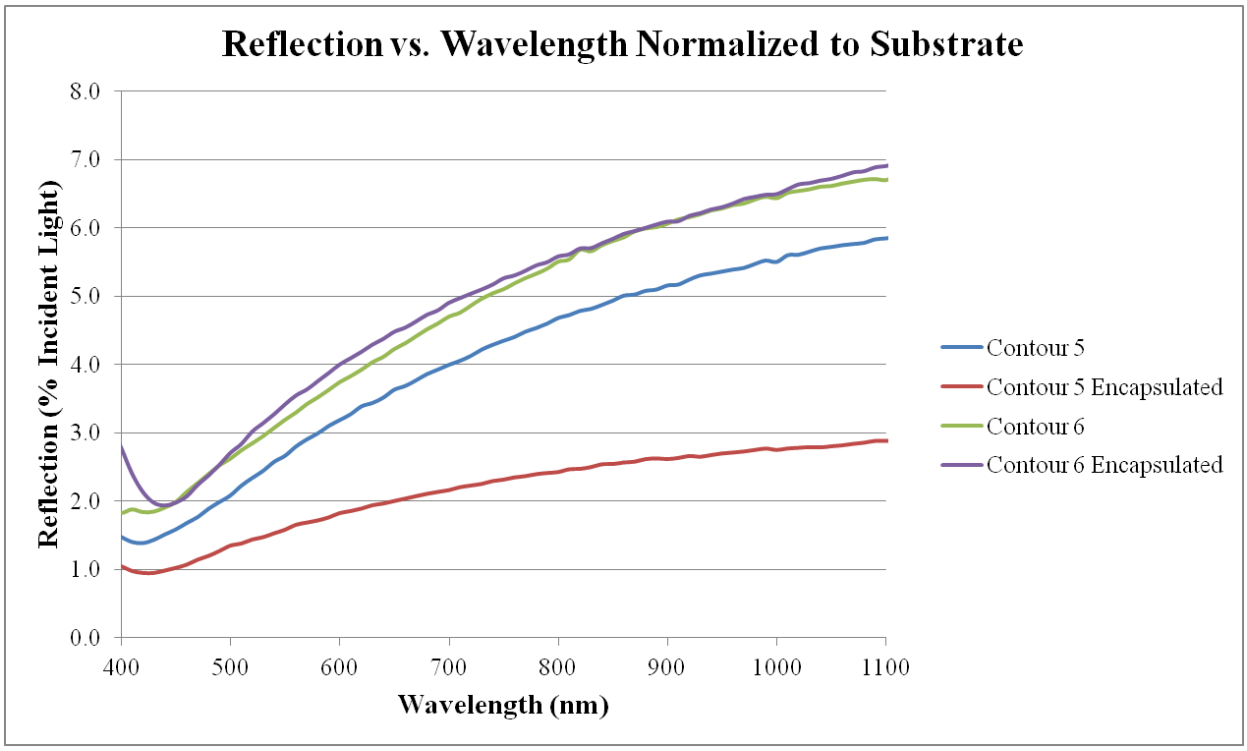


Figure 45. Reflectance versus wavelength of contours 5 and 6.

Initially it was thought that the decrease in reflectance from the sample would be realized by an increase in transmission of light through the sample. However, transmission measurements were made and an increase in transmission corresponding to the decreased reflectance was not realized.

Although this seems troubling on the surface an explanation can be found in the sample architecture. As shown below in Figure 46, once a light ray incident to a silver line is reflected at the critical angle β, internal reflection at the front glass-air interface occurs, and will also occur at the back glass-air interface. The light then becomes truly trapped in the sample module, resulting in an increased absorption rather than transmission.

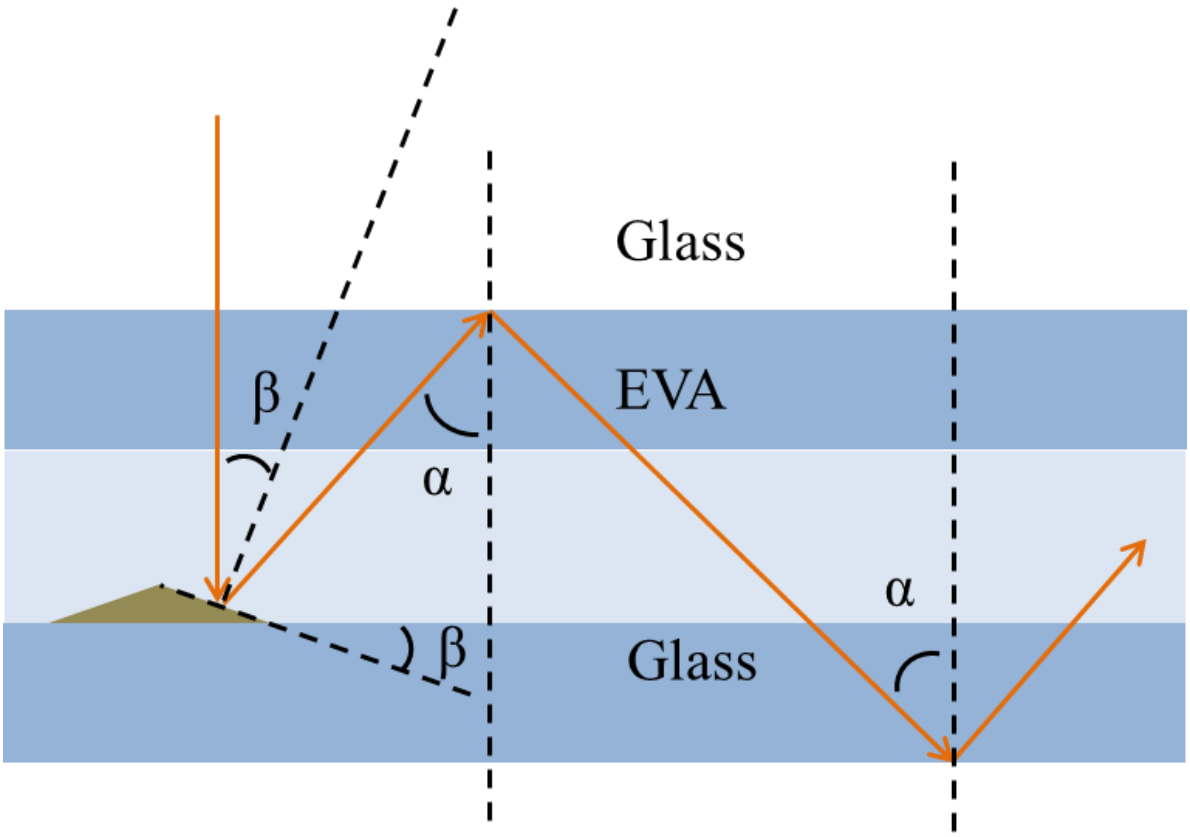


Figure 46. Diagram illustrating the possibility of multiple internal reflections.

3.3. Deposition and Performance of Collector Grids with Shadowing Equal to the Reference NREL Pattern

The goal of this research has been to investigate whether an increase in experimental SHJ solar cell performance can be realized by introducing a current collector grid consisting of ultra-fine conductive silver lines deposited via CAB-DW. As such, the first generation of solar cells was designed to highlight the increase in efficiency possible by maintaining the same geometric shadowing as a reference metallization pattern provided by NREL. This pattern consists of eight evenly spaced (1.25 mm) collector fingers each 25 µm wide and all connected to a 200 µm wide central busbar, resulting in 2% shadowing due to the collector fingers, and ~4% shadowing including the busbar. The same type of pattern was used for depositing collector grids via CAB-

DW except that to maintain the same amount of shadowing more collector lines, narrower in width and spacing were deposited.

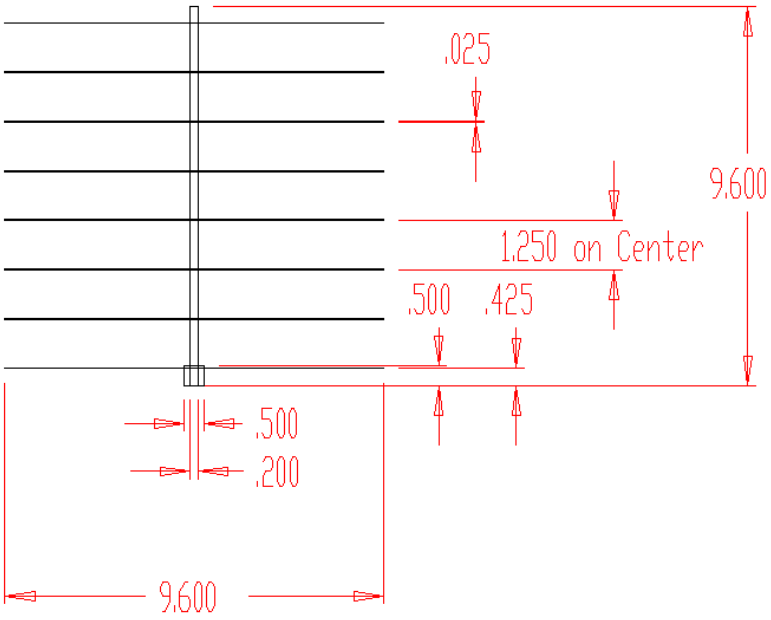


Figure 47. Auto-CAD drawing of NREL reference collector grid.

Four Silicon Heterojunction (SHJ) devices along with one diffused junction device were provided by a team of researchers at the National Renewable Energy Laboratory (NREL) in Golden, CO. Each device was created using n-type or p-type FZ or CZ (100) c-Si wafers 2.5 cm × 4.5 cm, 220 - 300µm and having a base resistivity of 1-4 Ω-cm. The a-Si intrinsic and doped layers were deposited using tungsten and tantalum HWCVD. Specifically, the HWCVD conditions for depositing the a-Si layer were a 20 standard cubic centimeter per minute (sccm) flow rate of SiH_4 at a chamber pressure and substrate temperature of 10 mTorr and 100 °C respectively. The n-doped a-Si layers were deposited using 2.5 sccm of SiH_4, 3 sccm of 5% PH_3 in H_2, and 50 sccm of H_2 at 60 mTorr and a substrate temperature of 200 °C. Similarly, the p-type a-Si was deposited using the same flow rates for SiH_4 and H_2, with the PH_3 being replaced by 10 sccm 3% B_2H_6 in H_2. To deposit the p-type a-Si the substrate was heated to 250 °C. The

resulting intrinsic, p and n layers were around 4 and 6 nm respectively, with their thicknesses confirmed via tunneling electron microscopy measurements. An ITO layer, approximately 760 nm thick, was also used as an anti-reflection coating/electrode on both the front and the back of each device

For this set of experiments the quality of the devices was not critical. Therefore the devices provided by NREL were not peak performers but rather non-optimized samples. The first step in processing the devices was to etch the top ITO layer into 1 cm × 1 cm individual cell regions spaced 1 mm apart. The segregation of individual test cell areas was necessary to decrease the effects of the adjacent materials on the individual test devices. If electrical contact is maintained between two adjacent solar cells, with one being illuminated, and the other being shadowed, the illuminated cell's performance will be degraded by the adjacent shadowed cell. Thus, the ITO layer is etched to decrease this effect.

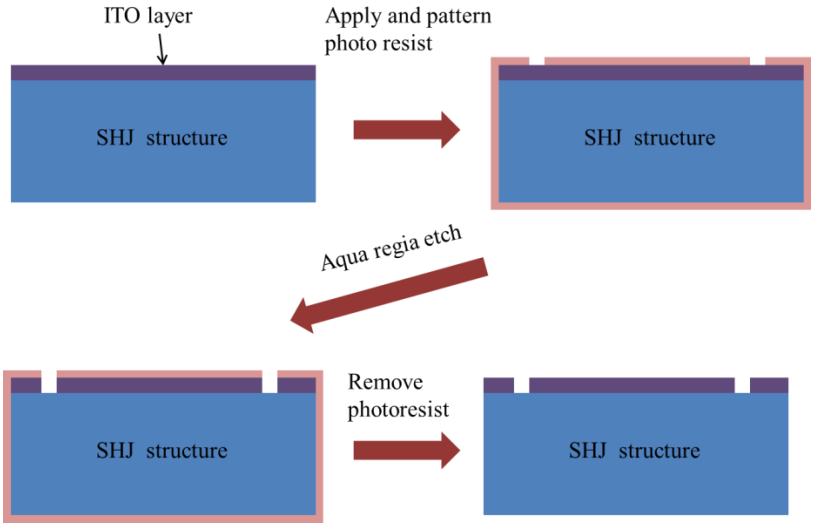


Figure 48. Diagram of the process used to etch the top ITO layer of each substrate.

The etching process (Figure 48) was carried out using standard cleanroom photolithography, in which a 1 µm layer of positive photoresist was applied to the front cell

surface via spincoating. The layer was then soft baked in a convection oven for 30 minutes at 95 °C. An additional layer of photoresist was applied to the backside of each sample to protect the back metal contact. After an additional soft bake, the front side was aligned with a shadow mask to maximize the number of individual cells per substrate. Following the exposure, the photoresist was treated with developer as per the manufacturer's guidelines. The samples were then subjected to an additional hard bake at 120 °C for 30 minutes. The samples were then etched in an aqua regia solution consisting of a 9:1 mixture of HCL to concentrated $HN0_3$ for one minute or until all traces of the ITO layer had been removed. After rinsing with deionized water, the samples were then ready for application of the current collector grid via CAB-DW.

The first substrate processed was T3690. A preliminary check found that the silver ink to be used for printing the collector grids had a bulk resistivity after post-processing of ~23 × bulk silver. A bus bar was printed in a single layer on each of the three cells of the sample. Collector lines around 9 µm wide were deposited with a spacing of 450 µm to achieve the desired 2% area coverage, matching the NREL reference grid. During the deposition process the substrate was heated to 100 °C to produce narrow lines with relatively high aspect ratios. In addition, each collector line was printed over four times to further increase their aspect ratio. The cells were then post-processed by sintering at 200 °C for one hour in air.

Following the sintering process, the finished cells were tested on the solar simulator test station (Photon Emission Technologies, Solar Simulator Model # SS50AAA) with a standard AM 1.5 G 1 sun illumination, and a 0-1V sweep while measuring the current through the cell. Initial results showed relatively poor performance, and it was suspected that the relatively thin bus bar was causing excessive resistive losses. To counter this, an additional three layers were deposited on each of the solar cells' bus bars to build up more conductive material. The cells

were heated to 100 °C while making the depositions, and then sintered at 200 °C for one hour in air. This increased the solar cells performance as can be seen below in Table 5. As such, four additional passes were deposited on each cell's bus bar using the same parameters and sintering processes mentioned previously.

It is also important to mention the necessity of shadowing the area surrounding the solar cell to be tested. If the adjacent cells and surrounding area are not shadowed, they can still contribute to the individual cell's J_{sc} despite the ITO layer having been etched. The strength of this effect can be seen when comparing the masked and unmasked measurement samples for T3690-5 (Table 5) with 8 bus bar layers deposited. Masking the surrounding area resulted in a 3.3 mA/cm^2 decrease in the J_{sc} value. To maintain consistency and accuracy, a testing protocol was developed which included the use of a mask to ensure that only the device being tested would be illuminated. Finally it must be noted that the stress induced by depositing 8 layers of silver ink on the bus bars of the samples of substrate T3690 caused them to peel off of the solar cells, destroying the collector grids. This effect was a direct result the ink being deposited on a heated substrate. Each layer of deposited ink was dry before the deposition of the next layer.

Table 5. Data from T3690-5 illustrating the effects of increased bus bar thickness and masking on cell performance.

	1 pass bus bar, no mask	**4 pass bus bar, no mask**	**8 pass bus bar, masked**	**8 pass bus bar, no mask**
V_{oc} (V)	0.570	0.576	0.567	0.570
J_{sc} (mA/cm^2)	30.8	31.3	28.1	31.4
FF	0.557	0.578	0.581	0.567
V_{mpp} (V)	0.384	0.424	0.384	0.384
I_{mpp} (mA)	25.5	24.5	24.1	26.4
V_{oc} slope (Ω)	4.47	4.43	4.60	4.44
Efficiency (%)	9.79	10.4	9.26	10.1

The resulting shrinkage of each deposition layer and its adhesion to the layer below resulted in a large stress gradient within the deposition, causing the bus bars to peel from the substrate.

After developing a general deposition and testing process collector grids were deposited on a new substrate, T3704. Both the bus bar and collector lines of each grid were deposited in 4 layers on a substrate heated to 100 °C. The collector lines were ~8 µm wide and spaced 400 µm apart to match the desired 2% area coverage. The bus bars throughout the initial PV-Nanocell study maintained the same dimensions shown in Figure 47. The samples were sintered at 200 °C for one hour in nitrogen. The same testing methods using the solar simulator test station were used to characterize the cells' performance and determine their efficiency.

Table 6. Data from tests of T3704-1 demonstrating the effects of overspray removal.

	Not Cleaned	**Cleaned**
V_{oc} (V)	0.607	0.606
J_{sc} (mA/cm^2)	27.4	28.1
FF	0.693	0.688
V_{mpp} (V)	0.455	0.460
I_{mpp} (mA)	25.3	25.5
V_{oc} slope (Ω)	3.56	3.54
Efficiency (%)	11.5	11.7

Table 6 demonstrates the effects that overspray could have on cell efficiency. Excess overspray, in the form of micrometer scale silver agglomerates, was removed mechanically with a cotton swab and isopropanol. The effect of removing the overspray can be seen in a 0.7 mA/cm^2 increase in the J_{sc}, which lead to 0.2% increase in cell efficiency. This cell was also the first to achieve an efficiency of over 11% utilizing a collector grid deposited solely via CAB-DW.

After demonstrating the ability to attain reasonable fill factors of around 69 % (Table 6), the intention was to deposit high-aspect ratio optically ideal collector lines, demonstrating an

increase in cell performance via total internal reflection induced light trapping. Several additional sample substrates (T3874, T3826, T3889) were prepared via an ITO etch as previously mentioned. Bus bars were then deposited in five layers on each of the samples which were heated to 150 °C. The resulting bus bars were at least 10 μm thick as estimated via optical microscopy.

The collector gridlines were then deposited using the same heated substrate. Several of the grids were deposited in a single low speed (1 mm/s) while the rest were deposited in 10 layers at the standard translation speed of 10 mm/s. The resulting grid geometries can be seen below in Table 5. It should be noted that due to the instability of the atomization process used when printing the contacts, some deposited line widths were significantly different than the designed widths.

Table 7. Comparison of designed and as deposited grid geometries. *Denotes additional deposition width, and resulting spacing and shadowing.

	T3874			**T3889**		**T3826**	
	1	**2**	**3**	**1**	**2**	**1**	**2**
Device type	p-type diffused junction			n-type SHJ		p-type SHJ	
Design line width (μm)	15	12	15	10	16	10	12
Spacing (μm)	750, 375*	600	750, 375*	500	800	500	600
Actual line width (μm)	14.7, 12.2*	24.9	14.3, 11.3*	15.5	11.3	9.6	10.6
Area Coverage (%)	1.95, 2.58*	4.15	1.90, 2.41*	3.1	1.42	1.92	1.76

Following deposition, the samples were sintered in nitrogen at 200 °C for one hour. They were then characterized using the testing system mentioned previously. Initial results were quite promising, and so the samples were left in open air overnight. The samples were then washed using methanol and a cotton swab. The samples were then tested, and a large decrease in cell performance was seen. The change was determined to be due to a rapid decrease in fill factor, which was indicative of a rapidly increasing series resistance (R_s) within the cell collector grid.

As an additional indicator, the slope of the I-V curve at the V_{oc} can serve as an estimate of the value of R_s of the cell, in this case the slope nearly tripled after staying in air overnight and being washed with methanol (Table 8).

Table 8. Data collected from T3874-2 illustrating how each of the cell's key parameters was affected by the rapid decrease in cell performance.

	Day 1	**Day 2**
V_{oc} (V)	0.673	0.675
J_{sc} (mA/cm^2)	34.9	33.1
FF	0.600	0.379
V_{mpp} (V)	0.455	0.333
J_{mpp} (mA)	30.9	25.4
V_{oc} slope (Ω)	5.37	15.0
Efficiency (%)	14.1	8.47

After realizing that such degradation was taking place, the samples deposited on substrate T3874 were re-sintered at 200 °C for one hour in nitrogen. This temporarily brought back some of the lost performance of the cells. In fact, T3874-2 saw an initial increase to 15.4% efficiency following the re-sintering, but this dropped to only 11.3% in less than an hour of being exposed to air. It was suspected that either oxidation of the collector grid or some unknown effect of the methanol was the cause of the decreased cell performance. In particular, the interface between the ITO layer on the top surface of the solar cell and the silver contact was of concern as such rapid decrease in the bulk resistivity of other silver depositions had never been observed. As an initial test of the oxidation hypothesis the samples on substrate T3874 were again heated to 200 °C for one hour, but this time in air. An increase in performance for T3824-2 from 8.5% to 11.8% was again realized, but degradation quickly followed.

In order to further test the ITO/silver interface oxidation hypothesis, additional collector lines were deposited on samples T3874-1 and T3874-3. This doubled the area coverage of the

collector grid, and thus doubled the area of contact between the ITO layer and the metallization grid. Substrate T3874 was sintered again at 200 °C in nitrogen for 1 hour. A substantial increase in performance was noted in samples T3874-1 and 3, with T3874-2 showing a slight decrease from the previous iteration of sintering (Table 9). This result was taken to be a clear indication that the culprit was indeed oxidation of the contact between the ITO layer and the silver collector grid.

Table 9. Cell performance results after doubling the area coverage of T3874-1 and T3874-3.

	T3874		
	1	**2**	**3**
V_{oc} (V)	0.651	0.662	0.661
J_{sc} (mA/cm^2)	33.7	33.5	34.3
FF	0.642	0.611	0.699
V_{mpp} (V)	0.475	0.455	0.505
J_{mpp} (mA)	29.7	29.9	31.3
V_{oc} slope (Ω)	3.95	5.31	3.46
Efficiency (%)	14.1	13.6	15.8

To further investigate this suspicion, high-resolution SEM images were taken of a collector line deposited on ITO coated glass using the same printing parameters and the same ink as was used to deposit the collector grids on sample T3874. A porous interface between the ITO coated glass and silver deposition can be seen in Figure 49. With such a structure in place it was not hard to imagine the rapid formation of native oxide and subsequent degradation in cell performance. A more in depth discussion of variation in ink and deposition electrical properties will be presented in Chapter 4.

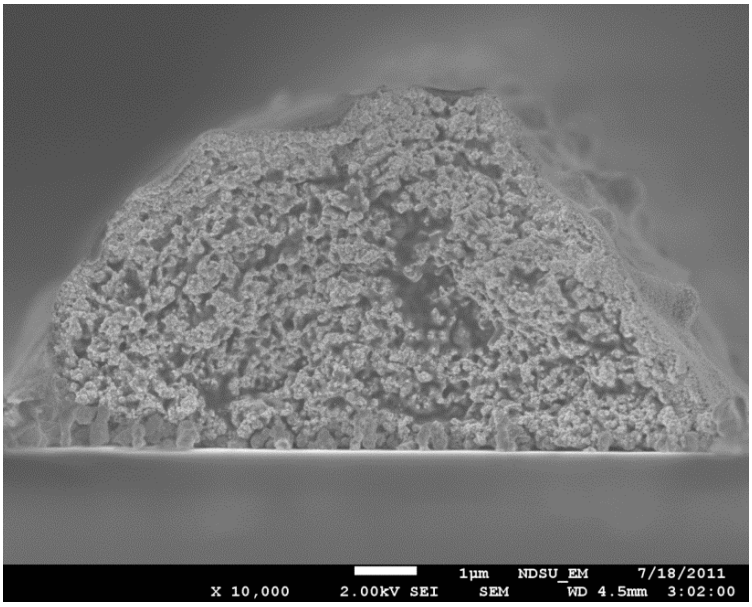


Figure 49. High resolution SEM image of a collector grid contact deposited on ITO coated glass.

Despite the complicating factors of the performance degradation due to apparent oxidation of the collector grid, many of the cells did perform quite well. A summary of the best performance data for each of the cells printed using PV-Nanocell silver nanoparticle ink and the CAB-DW system can be seen below in Table 10.

Table 10. Best results from solar cells with collector grids deposited using CAB-DW system and PV-Nanocell Silver nanoparticle ink.

	T3874			**T3889**		**T3826**		**T3704**	
	1	**2**	**3**	**1**	**2**	**1**	**2**	**1**	**2**
V_{oc} (V)	0.652	0.671	0.661	0.676	0.633	0.630	0.629	0.607	0.570
J_{sc} (mA/cm^2)	33.7	33.6	34.3	31.5	31.9	23.1	30.7	27.4	26.2
FF	0.642	0.682	0.699	0.625	0.510	0.302	0.289	0.693	0.629
V_{mpp} (V)	0.475	0.505	0.505	0.485	0.434	0.283	0.283	0.455	0.424
J_{mpp} (mA)	29.7	30.5	31.3	27.4	23.7	15.5	19.7	25.3	22.2
V_{oc} slope (Ω)	3.95	3.73	3.46	4.40	5.18	29.0	27.3	3.56	4.55
Efficiency (%)	14.1	15.4	15.8	13.3	10.3	4.40	5.58	11.5	9.40

Suns-V_{oc} measurements were also conducted on each of the test samples. The convenience of the Suns-V_{oc} measurement is that it is based on how the V_{oc} changes with varying light intensity. This data is then used, along with a supplied J_{sc} to calculate a device I-V

curve that is unaffected by the series resistance within the cell. As such, the results can be viewed as the cell performance that could be achieved if no R_s were present in the device.

Table 11. Suns-V_{oc} data for substrates T3874, T3889 and T3826.

	T3874			**T3889**		**T3826**	
	1	**2**	**3**	**1**	**2**	**1**	**2**
J_{sc} (mA/cm^2)	33.7	33.6	34.3	31.5	31.9	23.1	30.7
V_{oc} (V)	0.682	0.691	0.687	0.693	0.651	0.639	0.638
FF	0.785	0.808	0.807	0.825	0.706	0.786	0.790
V_{mpp} (V)	0.578	0.595	0.586	0.601	0.548	0.546	0.539
J_{mpp} (mA)	31.0	32.0	32.0	30.0	27.0	21.0	29.0
Efficiency (%)	18.0	18.8	19.0	18.0	14.6	11.6	15.5

When the experimentally obtained results in Table 10 are compared to the Suns-V_{oc} results found in Table 11, it is clear that there is ample room for improving the efficiency of each solar cell by the addition of better collector grid structures. This information, along with the difficulties experienced with the electrical properties of the current collector grid changing when exposed to air have emphasized the importance of the electrical properties of the silver depositions. Therefore, it became obvious that a thorough investigation of the electrical properties of structures deposited via CAB-DW needed to be conducted.

4. STUDY OF INK ELECTRICAL PROPERTIES

4.1. Bulk Resistance measurements for PV-Nanocell and Novacentrix inks

4.1.1. Bulk resistivity measurements

The electrical properties of deposited silver nanoparticle ink are very important when optimizing the collector grid structure. It has been previously demonstrated that an increase in contact resistance can be extremely detrimental to solar cell performance. In order to design an optimum collector grid, it is then necessary to quantify the bulk resistivity of the deposited metal ink, as well as the contact resistivity between the ink and its substrate.

In order to determine the bulk resistivity of the deposited metal structures, a test structure was designed consisting of two 0.5 mm X 0.5 mm pads connected by a 1 cm line (see Figure 50).

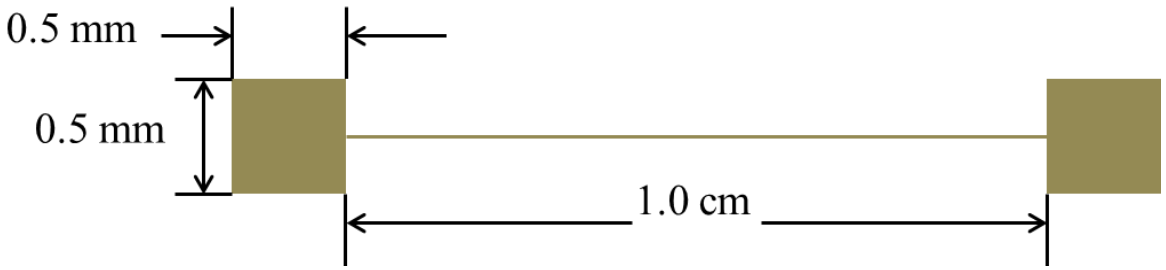


Figure 50. Diagram of bulk resistivity test structure.

After depositing the test structure onto an insulating substrate, usually a glass slide, the samples are then processed using the desired sintering schedule. The resistance of the structure is then measured using an R-V Kelvin measurement on the Agilent B1500A Semi-conductor Device Analyzer (Agilent Technologies). In this method, a voltage is applied between probes 1 and 2, causing a current to flow. Probes 3 and 4 are then used to measure ΔV between the pads. This voltage, and the current measured with probes 1 and 2 are then used to calculate the

resistance of the structure. By using this method, the contact resistance between the probes and the test structure is removed. This results in an accurate measurement of the resistance of the test structure. In this measurement scheme, the measured resistance is a sum of a portion of the resistance of the pads on each end and the resistance of the single line connecting the pads. However, it is assumed that the resistance due to the connecting line is much larger than that of each end pad. As an approximation then, the measured resistance is assumed to be only a measure of the resistance of the connecting line.

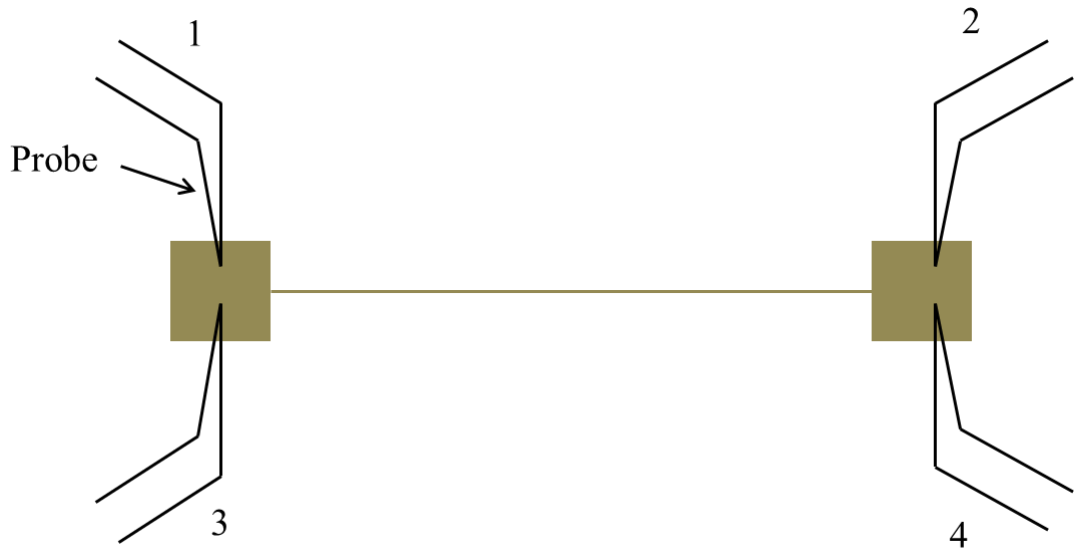


Figure 51. Diagram of the R-V Kelvin measurement scheme.

Once the resistance data has been gathered, it is necessary to obtain an estimate of the volume of the connecting line. Two methods have been used to accomplish this task. In the first method, profile data from the connecting line is obtained using a Contact Profiler instrument (P-15 Longscan Contact Stylus Profiler, KLA-Tencor). However, as noted previously, this method is precise, but not very accurate, resulting in profiles that are skewed to one side and overestimate the width of the deposited lines. The advantage of this method is that multiple measurements can be obtained for a single line, giving a better idea of the mean cross-sectional

area of the deposited line. After the profile data is obtained it is integrated numerically, using the trapezoid rule.

The other method used to obtain the cross-sectional area of the connecting line in the bulk resistivity structure was by fracturing the sample and then taking SEM images of the fractured line. The cross-sectional area of the contact can then be extracted from the SEM image manually using the trapezoid rule. The disadvantage to this approach is that only one profile can be extracted from each line, and samples do not always fracture as desired. In either case the end result is an estimation of the cross-sectional area of the connecting line, which along with the resistance value, and the length of the line, can be used to calculate the bulk resistivity of the material (see Eq. (33)).

$$\rho_m = R\frac{a_c}{l} \tag{33}$$

where ρ_m is the bulk resistivity of the metal deposition, R is the measured resistance of the test structure, a_c is the cross-sectional area of the test structure's connecting line, and l is the length of that same line. After obtaining a measured bulk resistivity value, it was then normalized by dividing by the bulk resistivity value for silver, 1.59×10^{-8} Ω-m.

4.1.2. Results for PV-Nanocell silver nanoparticle ink

Although the above method can be used to determine bulk resistivity, an initial study was conducted in which a set of resistance structures was deposited onto a substrate heated to 100 °C and sintered are various temperatures in air for one hour.

The samples were then tested using the Agilent test station. The results of this preliminary study can be seen in Figure 52. It should be emphasized that the cross-sectional area

of this sample set was not measured, and so the data reported assumes similar cross-sectional area for each sample set.

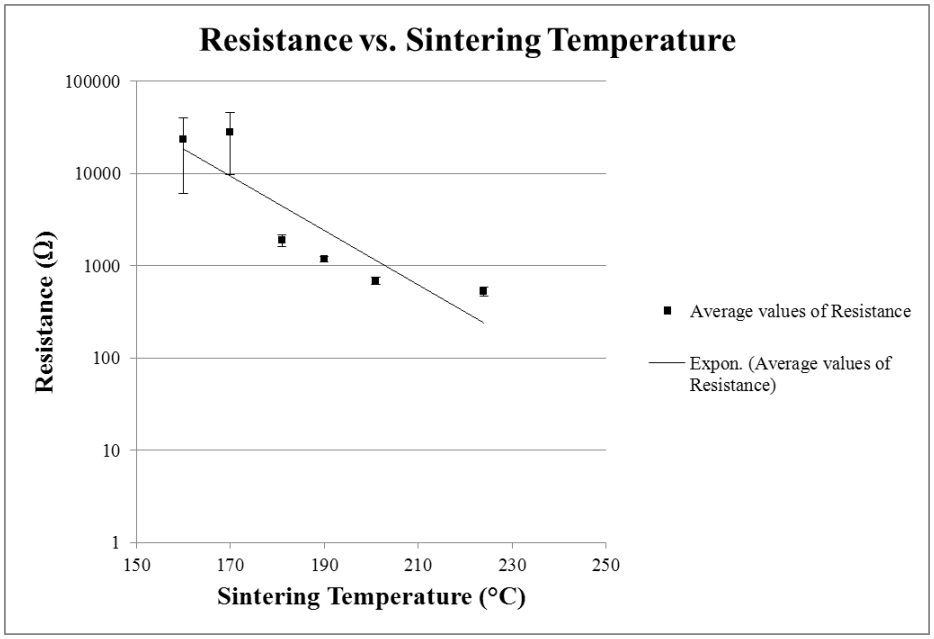


Figure 52. Plot illustrating the trend in decreasing resistance with increasing sintering temperature.

The results can be treated as relative values, and in doing so it is clear that increased sintering temperature decreases resistivity significantly. From this information it was concluded that a sintering temperature of 200 °C in air for one hour was sufficient to minimize the resistivity of the ink.

In order to get a better idea of what the actual bulk resistivity of the ink was before printing on the actual samples, a complete bulk resistivity study was carried out. Five conductivity samples were printed using PV-Nanocell silver nanoparticle ink, on a glass substrate heated to 100 °C. These samples were then sintered at 250 °C for one hour in air. Resistance and profile measurements were conducted as previously discussed, and the average bulk resistivity of the depositions was found to be ~ 23 × bulk silver, a value that at the time was deemed reasonable. This ink was then used in depositing the collector grid structures on

substrates T3690 and T3704. The relatively high bulk resistivity value of this ink was likely a result of its age, having been used for depositions for several months.

At the time it was not known that the electrical properties of the nanoparticle inks could change dramatically and so ink age was not viewed as a concern. A subsequent test of the bulk resistivity of a newly mixed ink was found to have a bulk resistivity of only ~3.8× bulk silver after being sintered at 200 °C for one hour in nitrogen. This experiment also investigated the bulk resistivity that could be achieved by sintering at 250 °C for one hour in nitrogen, and using a Rapid Thermal Anneal (RTA) process for one minute. The RTA apparatus consists of a 600 W Twin Tube Short Wave Emitter (Heraeus, model # 09751713) and reflector (Heraeus, model #KR85). The output of the apparatus is controlled by a variac (Staco Energy Products, model # 3PN1010B) with an output range of 0-140 V. The standoff distance between RTA emitter and the samples was approximately 5 cm. The results of the experiment can be seen below in Table 12.

Table 12. Data obtained from bulk resistivity study for various sintering methods and temperatures.

	Bulk Resistivity
400 °C RTA	6.4 × bulk silver
250 °C	3.3 × bulk silver
200 °C	3.8 × bulk silver

Bulk resistivity tests measured a batch of ink freshly mixed from the same ink supply used to deposit the current collector grids on substrates T3874, T3889, and T3826. It was found that the baseline resistivity had risen to ~15.6 × bulk silver. Being that the ink used in this test

was newly mixed, it was decided that the bulk ink from which all other inks were being mixed for printing had itself gone bad due to age.

4.1.3. Results for Novacentrix silver nanoparticle ink

A new ink, JSB-25HV (Novacentrix, Austin Texas) was then purchased as a replacement. In order to achieve atomization of this ink it was also necessary to mix it in a 1:1 ratio of ink to deionized water. The first task undertaken with the new ink was to determine the electrical properties that could be achieved under various sintering conditions. Although the PV-Nanocell ink could be sintered in either air or nitrogen, the Novacentrix ink was found to only sinter in air.

An initial experiment consisted of sintering several bulk resistance samples printed with 1, 5 and 10 passes over their connecting line at 250 °C for one hour in air. After testing the resistance of the samples, they were again sintered at 250 °C for an additional two hours. The resistance measurements were repeated, and contact profiles were taken to determine the bulk resistance of the material. The results, shown below in Table 13 demonstrate that a one hour sintering time was sufficient to obtain the best bulk resistivity possible at a sintering temperature of 250 °C.

Table 13. Initial sintering tests for Novacentrix silver nanoparticle ink.

250 °C Sinter	**10 passes**	**5 passes**	**1 pass**
1 hour	29 × bulk silver	10 × bulk silver	15 × bulk silver
+ 2 hours	28 × bulk silver	9.5 × bulk silver	16 × bulk silver

The next experiment was conducted to determine the lowest possible bulk resistivity that could be achieved by reasonable sintering temperatures, and through the use of RTA. Samples were deposited onto a 200 °C substrate. Individual sample sets were then sintered at 250 °C and 300 °C in air for one hour. An additional set of samples were processed using a one minute 300

°C RTA, and 400 °C RTA. The samples were then measured using the R-V Kelvin method described previously, with the results being displayed below in Table 14. Notice, that the lowest bulk resistivity was achieved after sintering at 300 °C for one hour in nitrogen. However, reasonable bulk resistivities were also achieved with the other methods as well.

Table 14. Bulk resistivities achieved via several different sintering methods and temperatures.

250 °C in air	300 °C in air	300 °C RTA	400 °C RTA
8.8 × bulk silver	5.0 × bulk silver	11 × bulk silver	11 × bulk silver

In order to fully optimize the electrical properties of the Novacentrix ink, the effect of substrate temperature on bulk resistivity was also measured. Bulk resistivity samples were deposited onto glass substrates heated to 75 °C, 100 °C, 150 °C, and 200 °C. The samples were then sintered using a one minute RTA treatment at a reference temperature of 300 °C.

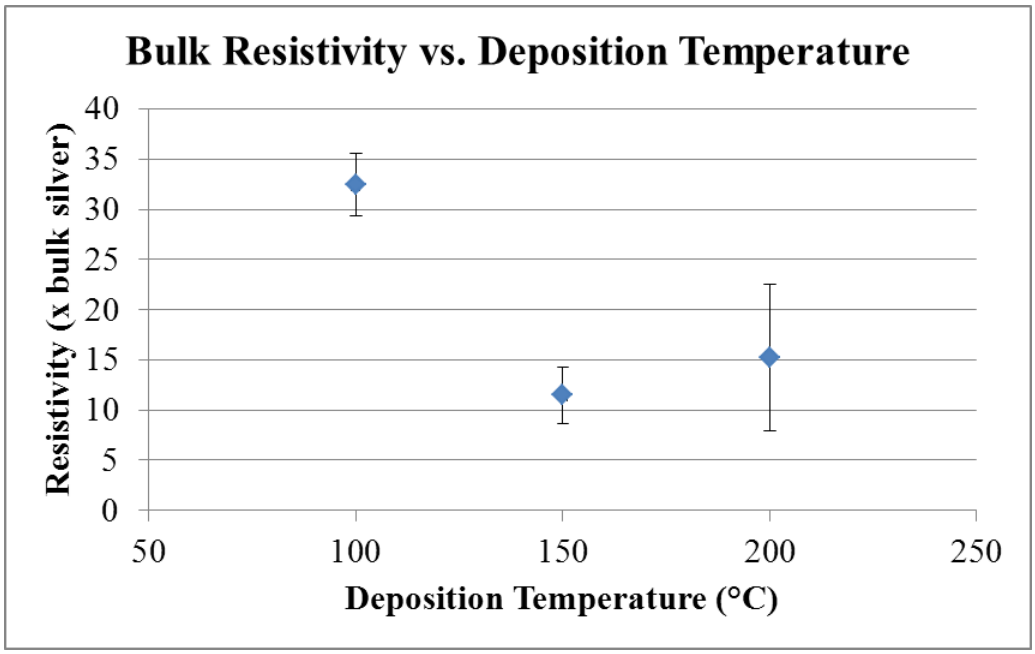


Figure 53. Plot of bulk resistivity with deposition temperature.

Unfortunately, the samples deposited at 75 °C were not conductive even after RTA processing and so they were not included in Figure 53. It should be noted, that although there seems to be a general downward trend in bulk resistivity with increasing deposition temperature, the actual values found in this study were somewhat higher than expected. Furthermore, the samples deposited onto the 200 °C substrate showed pretty significant scatter, which could be a result of the combined error of using the contact profiler to measure the profiles of very thin depositions.

An experiment was also conducted to find the relationship between sintering time and bulk resistivity. Five sets of bulk resistivity samples were deposited onto glass slides. They were then sintered at 300 °C for 5, 15, 30, 45 and 60 minutes.

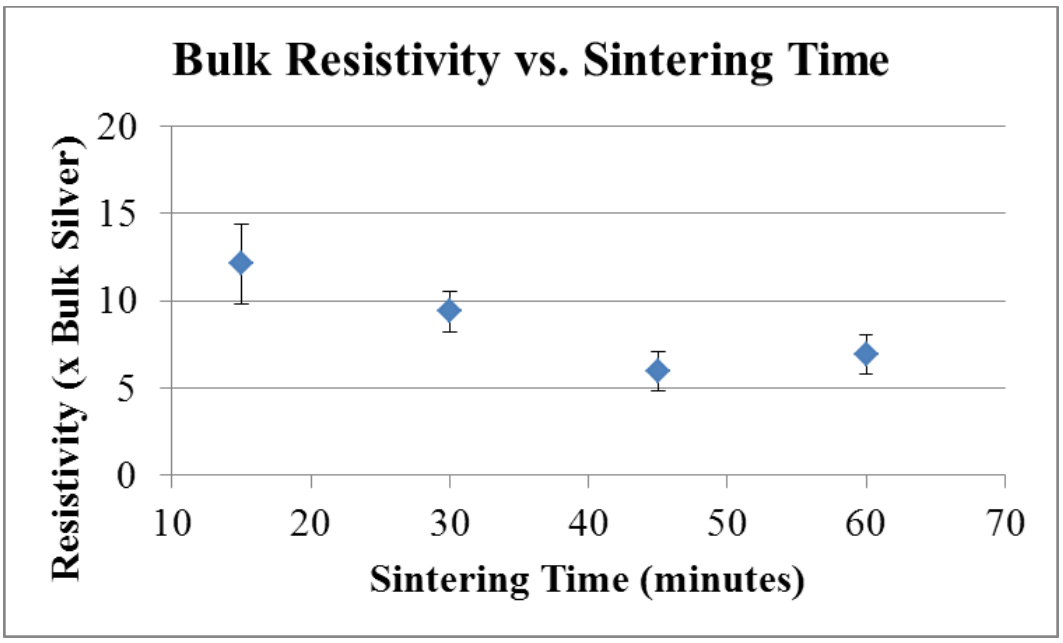


Figure 54. Plot of decrease in resistivity with increased sintering time.

The samples were then measured using the R-V Kelvin method. Due to the large variation in the samples sintered for 5 minutes, their data was not included in the above data. It is clear from the data presented in Figure 54 that a significant reduction in bulk resistivity is seen

with increased sintering time up to about the 45 minute mark. The data for 45 and 60 minutes overlaps and so no real distinction can be made between them.

In addition to thermal methods of curing the deposited silver nanoparticle ink structures, a non-thermal laser sintering method was also investigated. Unfortunately, despite much effort measureable conductivity was never achieved via the laser sintering process. It was found that instead of sintering the ink silver nanoparticles, the high-energy short-duration laser pulses simply ablated the depositions. An example of this can be seen in Figure 55 which shows a Novacentrix silver line before and after processing with the High Intensity Peak Power Oscillator (HIPPO) laser (Newport, Franklin, Massachusetts). The 355 nm wavelength harmonic was used, and passed through a hurrySCAN 10 laser scan head (SCANLAB, Munich, Germany) with a flat top beam profile. A scan rate of 250 mm/s, and a repetition rate of 50 kHz with a power output of 50 mW was used in to process the sample in Figure 55.

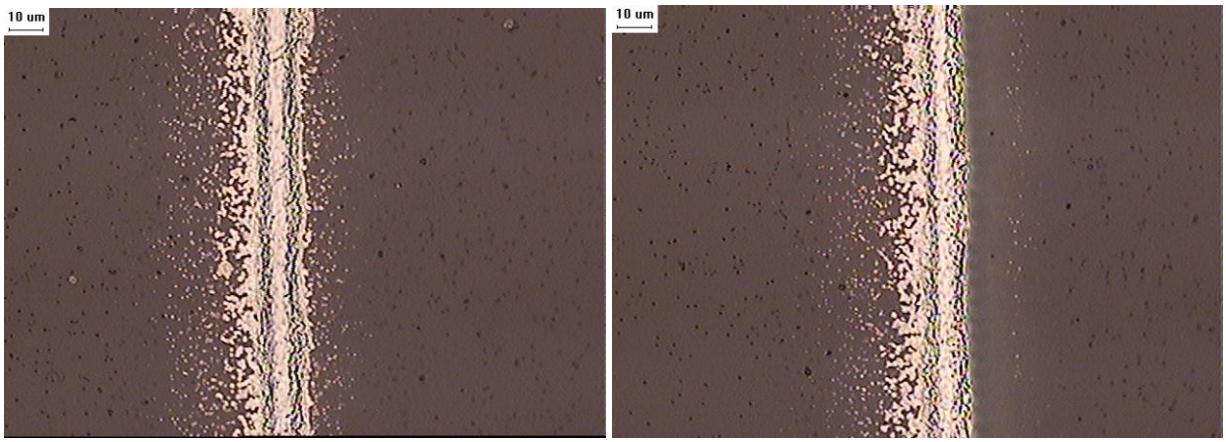


Figure 55. Images of a line deposited in 5 layers using Novacentrix silver nanoparticle ink. Left: the line before laser treatment, Right: the same line after laser treatment.

Notice, in the right image of Figure 55, that a portion of the line has been removed, along with the surrounding overspray. The ablation rather than sintering of the silver nanoparticles was typical. High resolution SEM images were also taken to compare a thermally sintered silver line to a laser treated line.

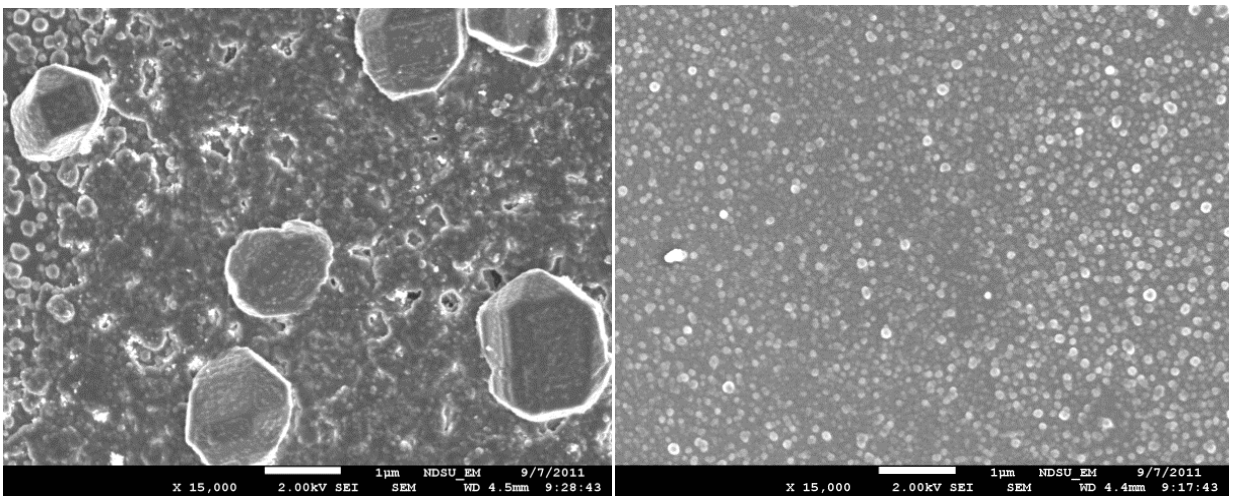


Figure 56. High resolution SEM images comparing silver sintered at 300 °C for one hour in air (left), and silver treated with the HIPPO laser (right).

Figure 56 demonstrates the vast difference in the nanostructure of Novacentrix ink that has been thermally treated, and ink that has been laser treated. Notice that in the laser treated ink, individual nanoparticles are still visible, whereas for the thermally treated depositions all such nanoparticles have fused with neighboring particles. Furthermore, the formation of silver crystals can be seen in the thermally treated silver. Electron Discharge Spectroscopy (EDS) was used to confirm the composition of the crystals that can clearly be seen in the left image of Figure 56. Due to a complete lack of results, laser processing of the silver depositions was abandoned.

4.2. TLM Measurement and Determination of Specific Contact Resistivity

4.2.1. The TLM test structure

Specific contact resistivity is another critical property that must be considered in the design of the current collector grid for solar cells. Unlike bulk resistivity, the determination of specific contact resistivity is somewhat more difficult. Different methods and test structures can be used to determine specific contact resistivity, but the most common method is the Transfer Length Method (TLM). A diagram of the TLM test structure can be seen in Figure 57. The test

pattern consists of metallic pads of the same size spaced by a distance d from each other. The distance d increases linearly between each pad. In the particular test structures used in this study, the minimum pad separation distance was 0.1 mm and was increased by 0.1 mm for each successive pad.

The substrate used in the TLM measurements must also be electrically conductive, as such ITO coated glass with a sheet resistance of 70-100 Ω/□ was used (Sigma-Aldrich, part #576352). After the test structures are prepared, RV-Kelvin measurements are conducted between neighboring pads, measuring the total resistance between them. The total resistance is a sum of the resistance of the metal pads, the contact resistance between the pads and the substrate, and the sheet resistance of the substrate itself.

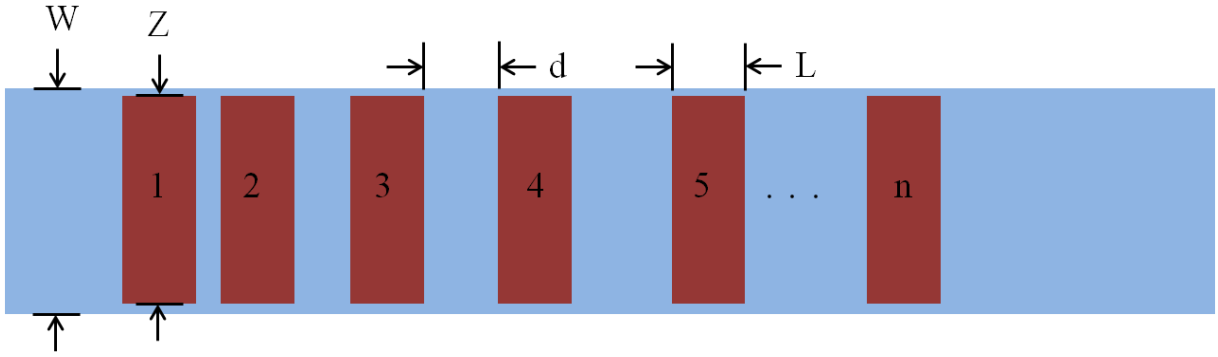


Figure 57. Diagram illustrating the test structure used for determining the specific contact resistivity using the transfer length method.

The measured total resistance is then plotted versus d, and a linear fit is performed on the data. An example of this plot can be seen in Figure 58. From analysis of the current flow through the test structure it can be shown that the total resistance, R_T is a function of the contact resistance of the metal pads to the substrate, as well as the pad spacing, d.

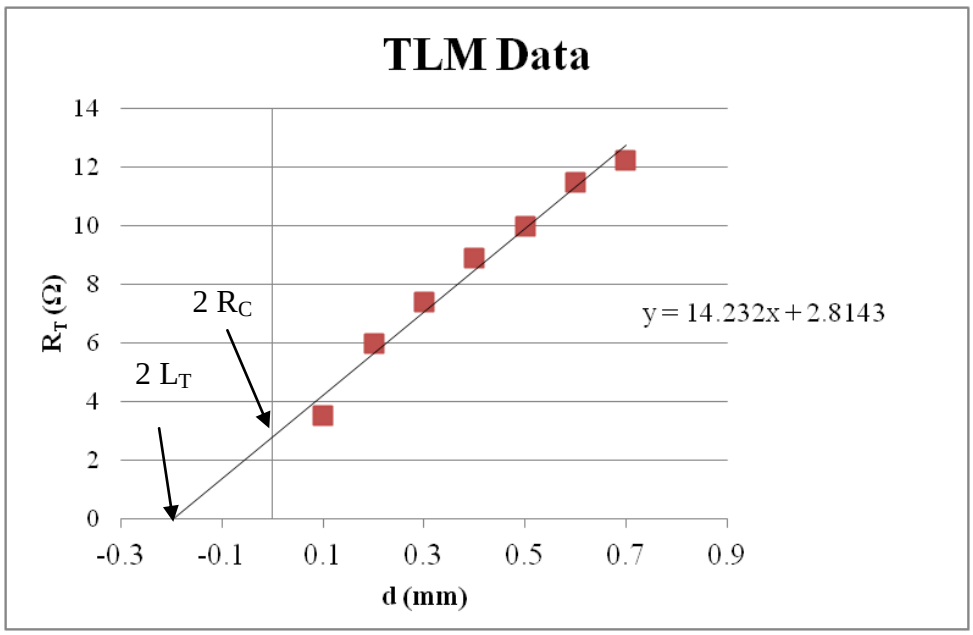


Figure 58. An example of TLM data with R_T plotted versus d.

The linear fit to the data can then be used to extract the desired parameters as shown below in Eq. (34).

$$R_T = 2R_C + \frac{R_{SH}d}{Z} \tag{34}$$

Where R_C is the contact resistance of each pad, R_{SH} is the sheet resistance of the film or semiconductor onto which the contact pads are deposited, W is the width of the pad, and d is the distance between the adjacent pads. $2R_C$ can be found from Eq.(34) at the limit where d=0; this point is extrapolated from the linear fit to the data as shown above in Figure 58.

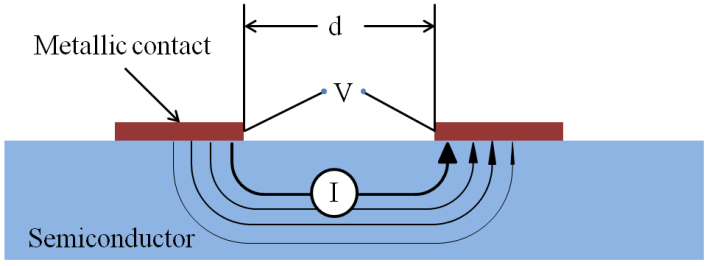


Figure 59. Diagram of the effects of current crowding.

Due to the nature of the TLM test structure, a phenomenon known as current crowding must also be considered. Current crowding is a direct result of the geometry of the TLM test structure, and has a larger effect when very low contact resistivity between the contact and the substrate is present. When a voltage is applied between two adjacent pads, a current begins to flow. However, because the substrate usually is much more resistive than the metal contacts, the current follows the path of least resistance, remaining in the metal contact as long as possible. The resulting current in the semiconductor reaches a maximum at the edge of the metal contact as shown in Figure 59. Schroder [93] presents a highly detailed theory based derivation of the expressions used to deal with the current crowding effect, which are crucial in conducting accurate TLM measurements.

The transfer length then is essentially defined as the length it takes for the majority of the current to transfer between the semiconductor layer into the metal contact. A further relation given by Schroder [93] is found in Eq.(35):

$$R_C = \frac{\rho_C}{L_T Z}\coth\left(\frac{L}{L_T}\right); where\ L_T = \sqrt{\frac{\rho_C}{R_{SH}}} \tag{35}$$

Where, ρ_c is the specific contact resistivity of the metal-semiconductor interface. L_T can be found by studying the limit where $R_T = 0$ of the line fitted to the data. L_T is equal to one half of this value which can be extracted from the plotted and fitted data. Therefore, by extracting both R_C and L_T from the plotted data it is possible to calculate a value for the specific contact resistivity, ρ_c, using Eq. (35). A further approximation can be made by examining the limits of the expression in Eq. (35). The resulting expressions, Eq. (35 a) and Eq.(35 b) can then be used to calculate a value for ρ_C.

$$If\ L \geq 1.5L_T;\ \coth\left(\frac{L}{L_T}\right) \approx 1\ ;\ R_c = \frac{\rho_C}{L_T Z} \quad (35\ a)$$

$$If\ L \leq 0.5L_T;\ \coth\left(\frac{L}{L_T}\right) \approx \frac{L_T}{L};\ R_c = \frac{\rho_C}{LZ} \quad (35\ b)$$

It should be noted that several assumptions are made with regards to the derivations of the previous relations used to determine ρ_C. The major assumption is that one-dimensional current flow is taking place. This is a safe assumption as long as the test structure is prepared appropriately, with (W-Z) << Z. This dimension is critical to minimize the amount of current that is able to flow around the contact violating the assumption of one-dimensional current flow. In addition the constraint of Z >> L and should also be met to ensure one dimensional current flow. Furthermore, it is best to design the test structure such that $L \leq L_T$. This ensures that all of the area of each pad is completely utilized in transferring the current between the metallization layer and the semiconductor layer.

4.2.2. TLM measurements of PV-Nanocell silver nanoparticle ink on ITO coated glass

Unfortunately, the understanding of this method was not known in such detail when the first TLM structures were created to determine the ρ_C value for the PV-Nanocell. As such, the test structures for measuring this inks performance consisted of 0.5 mm × 0.5 mm pads, spaced starting from 0.1 mm, with the spacing increasing by 0.1 mm for each successive pad. No attempt was made to accommodate the assumption that (W-Z) << Z, as the TLM patterns were deposited on to glass slides completely coated with an ITO layer. The results from these test structures then can be seen as precise, but not necessarily accurate.

Two experiments, conducted two months apart, were used to determine the specific contact resistivity of PV-Nanocell silver ink deposited and subjected to various conditions. In the first experiment, three test structures were produced by making depositions on ITO coated glass

heated to 100 °C, 150 °C, and 200 °C. Following deposition, the samples were sintered at 250 °C for one hour in a nitrogen atmosphere. They were then characterized as described above, with the results being displayed below in Table 15.

Table 15. Effects of substrate deposition temperature on change of ρ_C over time.

Deposition temperature	**100 °C**	**150 °C**	**200 °C**
Baseline ρ_C (mΩ-cm^2)	11.0	10.2	13.4
After 2 months in air ρ_c (mΩ-cm^2)	27.0	39.0	71.0
Post 200 °C anneal ρ_c (mΩ-cm^2)	23.0	30.0	41.0

Also included in this table, are the ρ_c values measured for the same samples after allowing them to sit in open air for 2 months. Notice that the samples deposited at higher substrate temperatures seem to have experienced a higher level of degradation over the same time period. This is likely a result of the increased porosity caused by depositing on heated substrates. Finally, the samples were also subjected to an additional anneal at 200 °C for one hour in nitrogen. Each sample showed a slight decrease in ρ_C, with the decrease being largest for the sample printed on a 200 °C substrate. This experiment clearly offers more evidence that oxidation at the ITO/silver interface was the cause of the degradation in performance of the solar cells.

A further experiment was conducted to investigate the effects a solvent wash consisting of methanol, would have on the specific contact resistivity of the test structure. As such, a baseline measurement was taken of the samples mentioned above. The samples were then soaked in methanol, and dried with purified nitrogen for 30 seconds. An additional measure of the specific contact resistivity proved impossible following the solvent wash, as the resistance measurements were extremely unstable. The samples were then annealed at 250 °C, 300 °C, and 350 °C for one hour each time in nitrogen. The samples were also retested after each anneal. The results of the study can be seen below in

Table 16. A study of the effects of a methanol wash on ρ_c.

Deposition Temperature	**100 °C**	**150 °C**	**200 °C**
Baseline ρ_C (mΩ-cm^2)	25.0	30.0	70.0
Post methanol wash ρ_C (mΩ-cm^2)	N/A	N/A	N/A
Post 250 °C anneal ρ_C (mΩ-cm^2)	57.0	35.0	Sample destroyed
Post 300 °C anneal ρ_C (mΩ-cm^2)	27.0	Sample destroyed	Sample destroyed
Post 350 °C anneal ρ_C (mΩ-cm^2)	15.0	Sample destroyed	Sample destroyed

A substantial increase in ρ_C was noted for the TLM structures even after the annealing at 250 °C. Unfortunately, only the sample deposited at 100 °C survived through the final annealing processes. However, the ρ_C of this sample did decrease down to its original value following the 300 °C anneal.

Following the completion of the above experiment, a final set of two TLM structures were printed using a newly mixed ink, onto ITO coated glass substrates heated to 150 °C. The samples were then sintered at 250 °C, and ρ_C values of 42 mΩ-cm^2 and 53 mΩ-cm^2 were measured from the structures. This result presented a further indication that the electrical properties of the ink, both bulk resistivity and specific contact resistivity, had increased substantially due to ink aging. Therefore, the ink was declared expired, and was no longer used in experiments.

4.2.3. Characterization of Novacentrix silver nanoparticle ink

Initially, TLM structures identical to those used to characterize the PV-Nanocell depositions were also used to characterize the Novacentrix depositions. The first experiment conducted was to investigate the ρ_C value that could be achieved on ITO coated glass by sintering at 250 °C and 300 °C for one hour in air, as well as by processing samples using a one minute RTA treatment at 300 °C and 400 °C respectively. Although the ρ_C values produced by the standard sintering processes at 250 °C and 300 °C (Table 17) were in the same range as

measured with the PV-Nanocell ink, a substantial decrease was noticed for the sample processed with the 300 °C RTA treatment (Table 17). This result was quite promising, as it was hypothesized that the major cause of the solar cell performance degradation was due to high contact resistance of the grid to the top ITO layer.

Table 17. Specific contact resistance of JS-B25HV silver ink.

	250 °C	**300 °C**	**300 °C RTA**	**400 °C RTA**
ρ_C (mΩ-cm^2)	24.3	26.5	6.8	29.3

After conducting this initial test, a new TLM pattern was designed to better meet the assumptions made previously. The major changes included narrowing the L dimension of the pads to 0.2 mm, extending the Z dimension to 2 mm, and using the HIPPO laser to isolate the TLM test structure from the surrounding ITO layer by ablating the ITO layer directly surrounding TLM pattern (Figure 60). The last adjustment essentially reduced the W dimension of the structure from a value much larger than Z (W>>Z) to a value approximately equal to Z (W≅Z). This satisfies the assumption that the current flow in the TLM structure is one-dimensional.

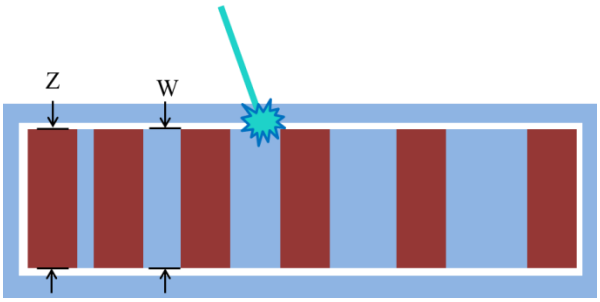


Figure 60. Schematic of the HIPPO laser isolation process.

An experiment was conducted to investigate the differences brought about by the changed TLM test structure, as well as the effects of isolating the TLM test structure from the

surrounding ITO layer. Samples 1 and 2 consisted of TLM structures with pads having dimensions of Z=L=0.5 mm (500 µm), and samples 3 and 4 consisted of TLM structures with pads having dimensions of Z=2 mm (2000 µm) and L= 0.2 mm (200 µm).

Table 18. Key parameters measured from four different TLM test structures.

	1	**2**	**3**	**4**
R_C (Ω)	19.9	8.3	5.5	6.4
Slope	188	42	40	26.9
L_T (µm)	212	393	273	472
L (µm)	518	518	216	224
Z (µm)	460	543	1993	2050
ρ_C (mΩ-cm^2)	19.4	17.6	23.5	29.2

The TLM structures for each sample were deposited onto ITO coated glass at a substrate temperature of 150 °C. The samples were then sintered via a 300 °C RTA treatment for one minute. Samples 1 and 3 were then isolated from the surrounding ITO layer using the HIPPO laser. Finally, each of the samples was tested using the R-V Kelvin test scheme previously described. The resultant resistance data were processed, along with microscope measurements of the as deposited TLM test structures to obtain the results found in Table 18. It should be noted as well that the isolation via laser ablation worked very well, resulting in a resistance value across the barrier in the MΩ to GΩ range.

One of the key things to notice from this data is that the slope of the fit line for the data from sample 1 is significantly larger than the other samples. This stands out because the slope of the fitted data should depend only on the sheet resistivity of the substrate onto which the TLM structures were deposited. Thus, such a high slope value indicates a strong deviation in the sheet resistivity of the ITO layer in sample 1. This could either be a result of the isolation process, or simply non-uniformity in the ITO coating of the glass slide. The transfer length (L_T) is also

another important quantity that is different for each of the samples. In particular, a L_T value is noticed for the isolated samples compared to the non-isolated samples. This is likely a manifestation of restricting the current flow to one-dimension and no longer allowing the current to be transferred into the pads along the sides as well as at the front.

Although this data makes it clear that the refined TLM structure behaves differently from the initial pattern used, it is not clear what the end result is on the measured ρ_C value. To illustrate this, consider the values of ρ_C for samples 1 and 2. The ρ_C of sample 1 is measured to be larger than that of sample 2, which has not been isolated. However, if the same comparison is made between samples 3 and 4, the opposite is noticed: the isolated sample has a lower ρ_C.

The revised TLM test structure presented above is very useful for determining a value for ρ_C, but one of the chief concerns regarding the effectiveness of the current collector grid was of course the contact resistance between a single current collector line, and the ITO layer. Particular regard has been paid to the effects of oxidation on the TLM structures produced using the PV-Nanocell silver nanoparticle ink, however, the change in ρ_C for those samples increased over a period of around two months. The degradation in performance noticed in the solar cells was occurring on a much shorter time-scale, on the order of minutes to hours. It was hypothesized that the decreased dimensions of the current collector gridlines, namely their higher surface area to volume ratio, could bring about a rapid increase in the rate at which the ρ_C of the samples was affected by the oxidation process. To further investigate this, a pseudo-TLM structure with measurements consisting of single silver lines.

To produce the structure, two pads measuring 0.5 mm × 7 mm and spaced 0.5 mm apart were deposited with the CAB-DW system using five layers of Novacentrix silver nanoparticle ink. The pads were then sintered using a one minute 300 °C RTA treatment. After sintering the

two large pads, they were then isolated and diced into 14 pads roughly 0.5 mm × 0.5 mm. Single lines were then printed in five layers, connecting pads from the adjacent bars and spaced from each other starting from 0.1 mm and increasing by 0.1 mm for each successive pair of pads (see Figure 61). The finished structure was then processed again with a one minute 300 °C RTA.

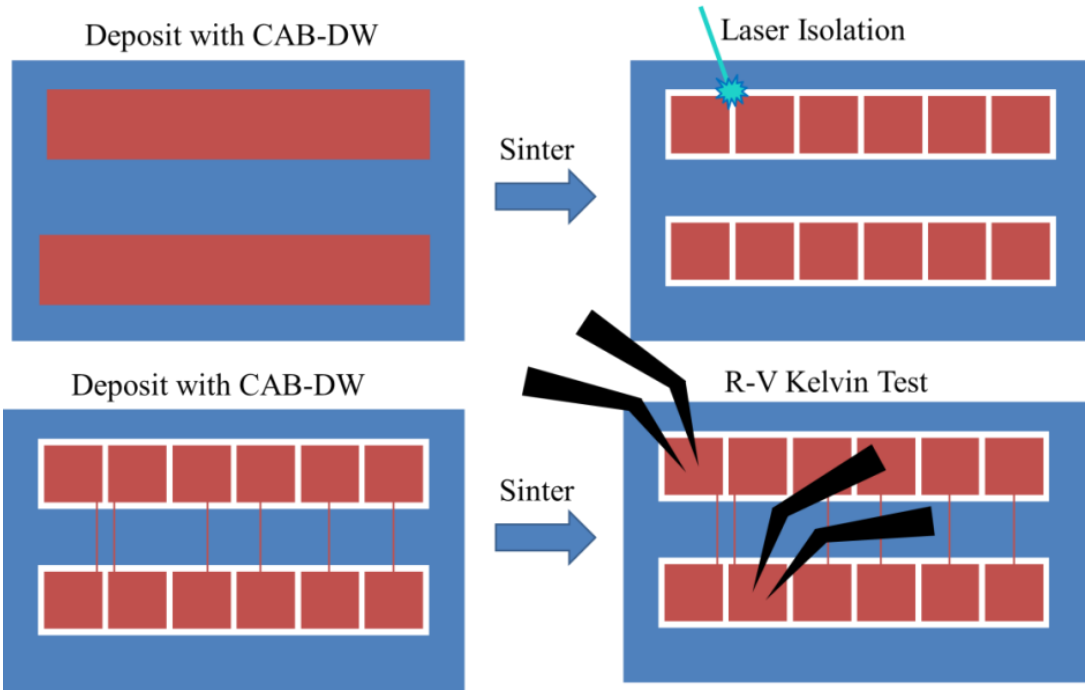


Figure 61. Diagram of the construction of a pseudo-TLM structure for measuring ρ_C for a single line.

Following this final processing step, the resistance was measured between adjacent lines using an RV-Kelvin measurement on the Agilent test station. The electrical measurements were repeated multiple times while the test structure was allowed to oxidize and age in a normal atmosphere. The measured resistance data was then used to calculate a ρ_C value. It should be emphasized that although the measurement structure was very precise, the measured ρ_C values are likely not accurate. This is because in a standard TLM measurement the pads are considered to be equipotential structures, an assumption that does not hold with single lines due to their large length to width ratio. After calculating the values for ρ_C at each of the measurement times,

the values were normalized by dividing by the initial value of ρ_C. The resulting increase in contact resistance can be seen in Figure 62.

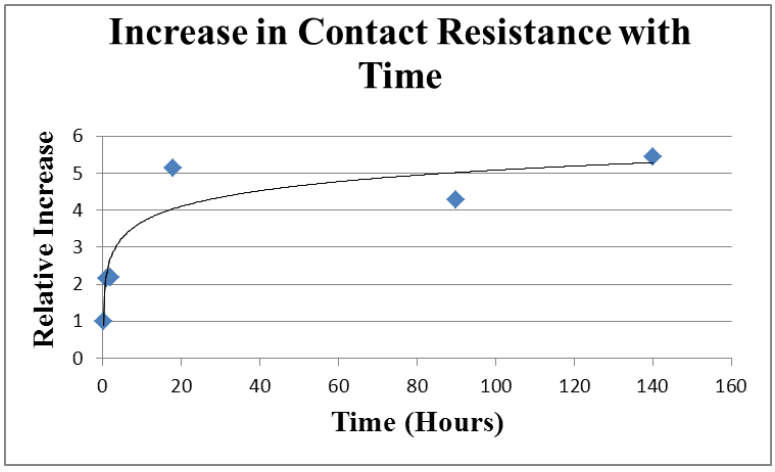


Figure 62. Relative increase in contact resistance for a single line over time.

The contact resistivity increases by a factor of five in the first 20 hours in air, but it appears that the process plateaus at that point, with no significant change after the initial increase.

4.3. Ink Aging Study and Discussion

In order to avoid the complications of using an expired ink, the electrical properties of a batch of Novacentrix silver nanoparticle ink were monitored over a period of approximately four months. According to the manufacturer, the useful life of the ink was estimated to be more than six months at room temperature [94]. To monitor the health of the ink a standard ink sample was produced. As can be seen from Figure 63, the sample consists of lines printed in 1, 5, 10, 20, and 40 passes all deposited at an elevated substrate temperature of 150 °C. The substrates used for the samples were pieces of ITO coated p-type silicon wafer. This substrate was chosen to act as a close approximation to an actual solar cell with regard to thermal and surface characteristics. Additionally, a droplet of ink is applied at room temperature using a pipette. The samples were then sintered at 300 °C in air for one hour. The samples were then sectioned to expose the cross-

section of each of the lines and the droplet. High resolution SEM images were then taken of the samples to study both the line profiles and look for any changes in the nanoparticle sintering characteristics.

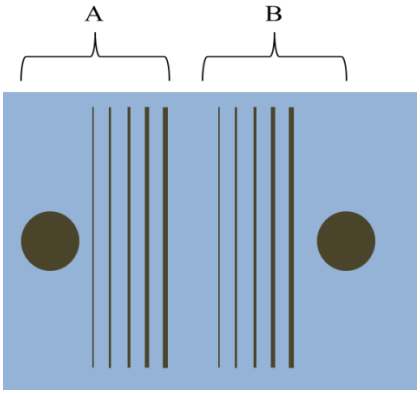


Figure 63. Schematic of a standard SEM ink aging study sample.

While conducting the investigation, two methods of ink storage were also studied, both inks were stored in a nitrogen atmosphere, with one being stored at ~0 °C and the other being stored at room temperature ~22-25 °C. Bulk and specific contact resistivity samples were also deposited using each of the inks and processed in the same manner as the previously mentioned SEM samples.

Table 19. Measured specific contact resistivity from the study of ink aging.

	~ 25 °C		**~ 0 °C**	
	ρ_C (mΩ-cm^2)	**L_T (µm)**	**ρ_C (mΩ-cm^2)**	**L_T (µm)**
Week 3	3.8	40	5.5	50
Week 4	0.53	17	2.3	34
Week 8	0.0025	1.5	0.069	7.6
Week 16	0.015	3.4	NA	NA

One of the things immediately noticed from the ink aging study was a general decrease in specific contact resistivity, ρ_C, with time. Specifically, the measured transfer length, L_T decreased substantially over the period of several months. Although the chief cause of this is unknown, it is hypothesized that it may be due to a degradation of the dispersants used to create nanoparticle inks. The dispersants normally act as a protective shell around the silver nanoparticles, preventing agglomeration. However, it is also the dispersant that must be destroyed during the sintering process to bring about useful electrical properties.

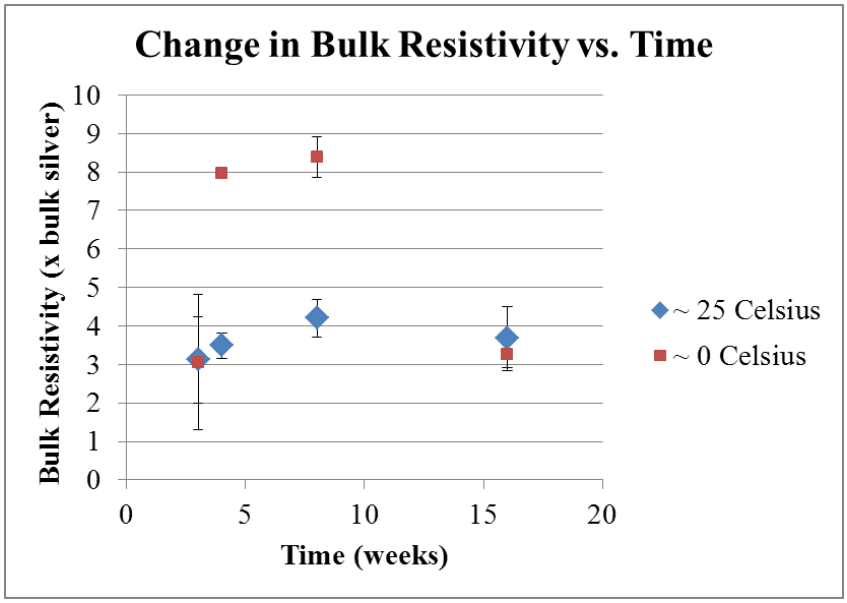


Figure 64. Plot of measured bulk resistivity data for inks stored at different temperatures.

Bulk resistivity data was also collected during the same study. SEM images of the bulk resistivity sample profiles were measured manually to determine the cross-sectional area, and a bulk resistivity value was calculated based on this information. The plotted data can be found above in Figure 64. The standard deviation of each measured value is included in the plot in the form of error bars, but unfortunately only one sample survived for the week 4 data of the ink stored at ~ 0 °C and thus no error bar was included. Although their seems to be some fluctuation

for the ~ 25 °C ink sample the bulk resistivity remained between 3 and 5 times the bulk resistivity of silver. A significant increase in the week 4 and week 8 values for the ~ 0 °C ink were noted.

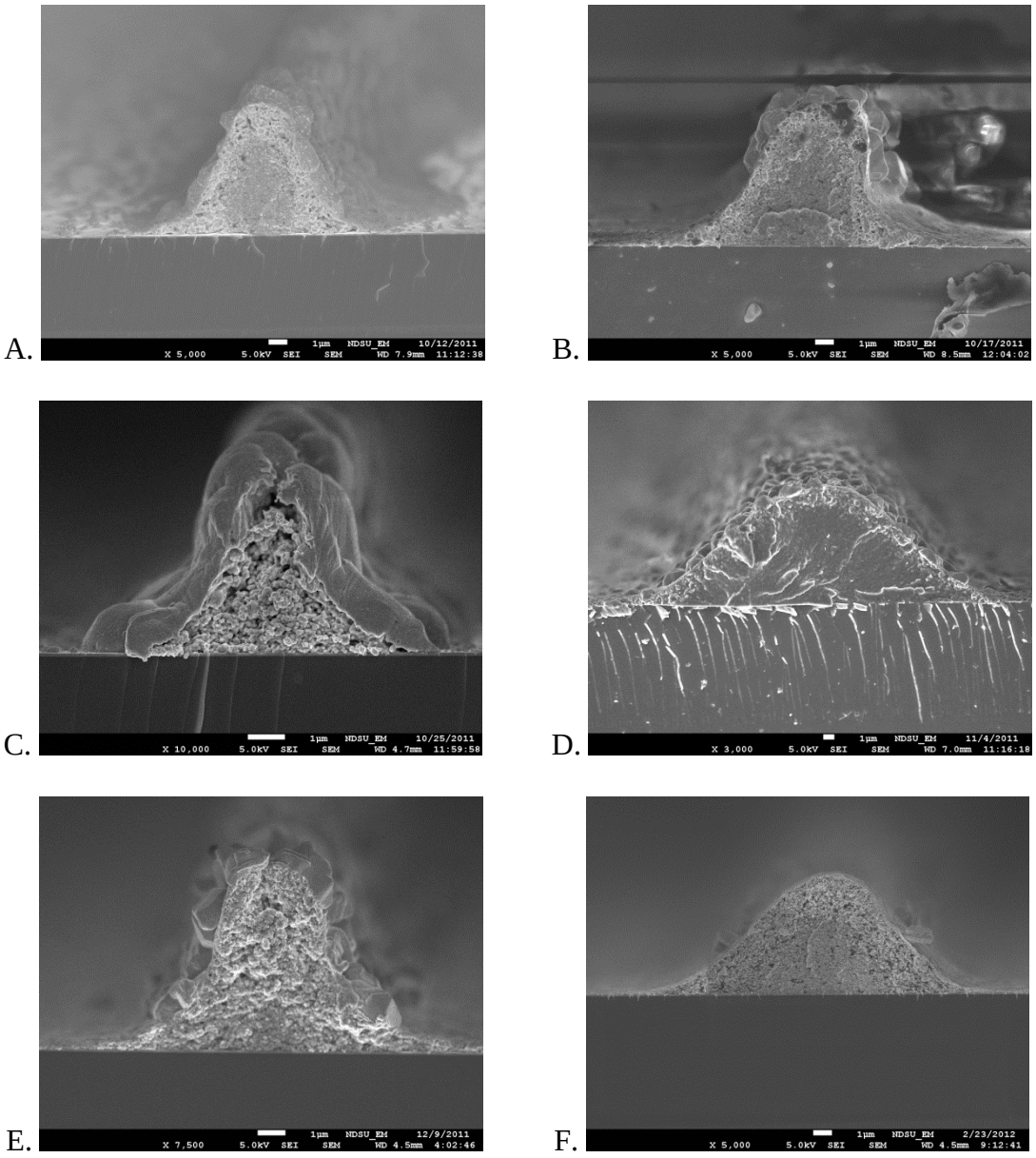


Figure 65. High resolution SEM images of Novacentrix ink stored at ~ 25 °C and printed in 40 layers during A.)Week 1, B.) Week 2 , C.) Week 3, D.) Week 4, E.)Week 8, F.) Week 16.

This is likely a result of the ink changing over time, as the same trend is noticed in the ~ 25 °C sample, only in a less pronounced manner. Based on the results of this and the previous TLM data, it was decided that the final set of current collector grids would be deposited using ink that had been stored in ambient conditions.

Examination of the high resolution SEM images did provide some interesting pictures, however there did not seem to be a clear correlation between the appearance of the sintered ink and the corresponding electrical properties. The SEM images above (Figure 65) were taken of lines printed in 40 layers onto ITO coated p-type silicon heated to 150 °C using samples of ink which had been stored at ~ 25 °C. The above images illustrate the effects that changes in atomization can have on the resulting profile. The mass flow rate of silver nanoparticle ink is directly related to the carrier gas flow rate, as well as the amount of atomization occurring in the ultrasonic atomizer. For example, if a large amount of atomization is occurring, only a low carrier gas flow rate of around 10-15 sccm (standard cubic centimeters per minute) needs to be used. However, if a low amount of atomization is occurring, the carrier gas flow rate can be increased to increase the mass flow of ink through the deposition head. Unfortunately, it has been the authors experience that the amount of atomization occurring can be very unstable, causing insufficient mass flow of ink droplets through the deposition head.

For the images of Figure 65, a standard carrier gas flow rate of 15 sccm was used in all of the depositions. The result then was depositions of varying cross-sectional area. Another interesting phenomenon to point out is the formation of silver crystals on the depositions during the sintering process. Crystal formation is present in all of the samples, but seems to be particularly extreme in the sample found in image C of Figure 65. It appears that the silver material migrated to the outside surface of the silver deposition, contributing to the formation of

silver crystals there. The migration of silver to the outside of the deposition clearly leaves behind voids in the central portions of the depositions.

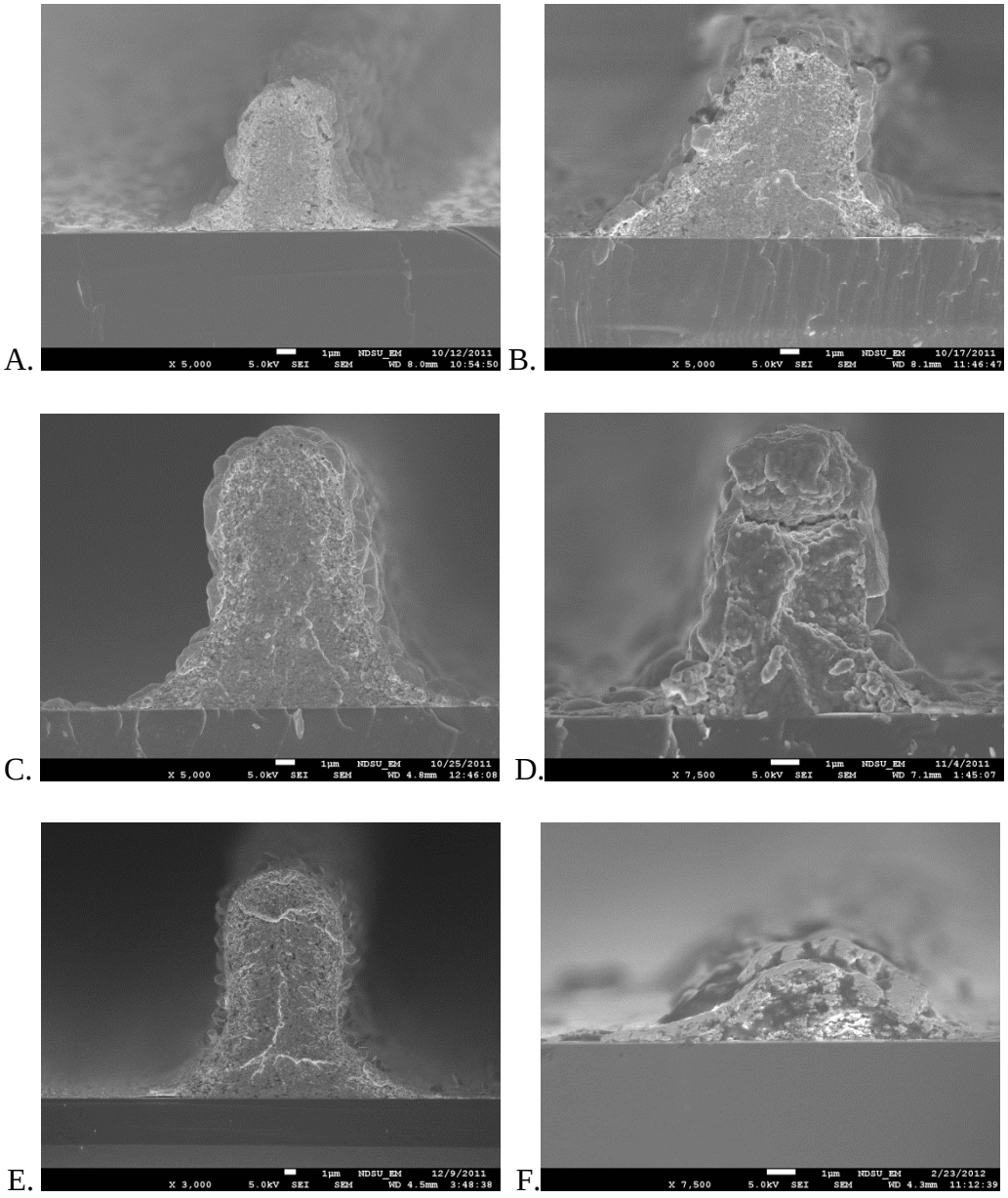


Figure 66. High resolution SEM images of Novacentrix ink stored at ~ 0 °C and printed in 40 layers during A.)Week 1, B.) Week 2, C.) Week 3, D.) Week 4, E.)Week 8, F.) Week 16.

This phenomenon was not noticed in the lines deposited in 40 passes using the ink stored at ~ 0 °C which can be seen in Figure 66. However, it does not appear to be unique to the ink storage method either, as it was seen in depositions from both ink sources.

Very large aspect ratios are also seen in Figure 66. The depositions in Figure 66 were also made with a carrier gas flow rate of 15 sccm, and onto an ITO coated p-type silicon substrate heated to 150 °C. The high aspect ratios are a direct result of the ink atomizing very well, producing an adequate mass flow of ink to the deposition head. Attention should be drawn to the large amount of overspray, corresponding to such high aspect ratio depositions. The presence of overspray in effect decreases the aspect ratio of the line due to the increased shadowing.It appears that the amount of overspray present in a deposition is a direct result of the quality of the atomization process. Further study into devising a better atomization process could greatly improve the overall quality of depositions made with the CAB-DW system.

5. DEPOSITION OF COLLECTOR GRIDS WITH NOVACENTRIX INK

5.1. Device Characteristics and Optimal Grid Design

Once it was determined that the electrical properties of the Novacentrix silver ink were stable, and within a reasonable range, optimal collector grid design for the ink was undertaken. Unlike the previous study using PV-Nanocell ink, the new set of current collector grids would be optimized using the previously reviewed model developed from literature. In order to design the optimal grid structure, an estimate of the maximum power point current density and voltage, J_{mpp} and V_{mpp}, was needed. In order to obtain this data Suns-V_{oc} measurements were conducted (Sinton Instruments, Boulder CO). The Suns-V_{oc} system works by measuring the open circuit voltage of the solar cell as it is subjected to varying amounts of illumination. This information, combined with several user inputs such as J_{sc}, base resistivity of the cell, and cell thickness, are then used to calculate a pseudo- IV curve, along with a pseudo-fill factor, and pseudo-efficiency. Because these values are calculated from measured V_{oc} characteristics, there are no series resistance losses in the measured data. Thus, the resulting data represents the maximum performance that could be achieved by the measured cell. A detailed explanation of the theory and development of the Suns-V_{oc} measurement system can be found in [95, 96, 97].

As previously mentioned, it is necessary to provide the J_{sc}, cell thickness, and base resistivity of the solar cell being measured using the Suns-V_{oc} system. Of the required inputs, the J_{sc} proved the most difficult to obtain. Due to the poor performance of PV-Nanocell current collector grids a comparison had to be made between the cell performance with and without the current collector grids applied. The PV-Nanocell collector grids were removed with an etching

process (Transene, Silver Etchant TFS). The I-V characteristics were then measured using the solar cell test station. The highest J_{sc} value from the two measurements was then used as the input into the Suns-V_{oc} instrument. An exact value for the base resistivity of the samples was not known, and so an estimated value of 3 Ω was used. It should be noted that other values were input into the fitting software of the measured data and the important output values were not very sensitive even to large changes in the base resistivity value. The cell thickness was simply measuring with a caliper and found to be 250 μm. With this data it was then possible to obtain the required J_{mpp} and V_{mpp} values. The measured values can be found in Table 20.

Table 20. Suns-V_{oc} data for each of the solar test cells.

	T3874			**T3826**		**T3889**	**T3704**	
	1	**2**	**3**	**1**	**2**	**1**	**1**	**2**
J_{sc} (mA/cm^2)	35.3	35.5	35.6	28.4	27.6	31.6	28.1	27.7
V_{oc} (V)	0.644	0.641	0.640	0.593	0.585	0.663	0.568	0.568
V_{mpp} (V)	0.543	0.554	0.550	0.509	0.505	0.576	0.491	0.488
J_{mpp} (mA/cm^2)	32	33	33	26	26	29	27	26
FF	0.758	0.815	0.809	0.797	0.814	0.807	0.816	0.812
Efficiency (%)	17.2	18.5	18.4	13.4	13.2	16.9	13	12.8

After obtaining values for J_{mpp} and V_{mpp} it was also necessary to obtain a sheet resistivity (R_{sh}) value for the ITO layer of each of the cells. This was measured using a standard 4-point probe station (Cascade Microtech) and sourcemeter (Keithley). Due to the small area being measured, it was only possible to conduct one accurate measurement on each of the solar cells. The measured data can be seen in Table 21.

Table 21. Measured R_{sh} values for each of the test cells.

	T3874			**T3826**		**T3889**	**T3704**	
	1	**2**	**3**	**1**	**2**	**1**	**1**	**2**
R_{sh} (Ω/□)	46.2	44.4	43.7	60.3	62.4	204	379	110

In addition to the above input parameters, it was also necessary to include values for bulk and contact resistivity. These values were taken to be a bulk resistivity (ρ_m) of 5.84×10^{-8} Ω-m, and a specific contact resistivity (ρ_C) of 0.0152 m Ω-cm^2. Both values were taken from the final results of the ink aging study performed on the Novacentrix ink stored at room temperature (see chapter 4). The final input information needed for determining the optimal grid structure for each solar cell was the expected geometry of the current collector grid lines and busbar.

As was demonstrated previously, the aspect ratio of the depositions along with the deposited line width are the key determining factors in the optimized grid design. Unfortunately, due to unstable atomization, it was not possible to deposit current collector lines of a known aspect ratio and width. To approximate the possible aspect ratios, a study of the aspect ratios of depositions made during the ink aging study was undertaken. In particular, the 20 pass lines deposited for SEM study were examined, and an average aspect ratio of ~0.2 was determined to be a reasonable value. This value was attained by manual application of the trapezoid rule to determine cross-sectional area of the depositions. The cross-sectional area was then divided by the square of the line width, resulting in the above aspect ratio. It should be noted, however, that this data was based solely on SEM images, which often failed to capture the extent of the overspray extending on either side of the deposition. As such a more conservative estimate of an aspect ratio of 0.1 was used to determine the optimal grid structure. A summary of the material and geometric properties used in the model can be seen below in Table 22.

Table 22. Material and geometric properties used in modeling.

ρ_m (Ω-m)	ρ_C (mΩ-cm^2)	Aspect Ratio (h_F/W_F)	Line Width (μm)
5.84×10^{-8}	1.52×10^{-2}	0.1	10-25

It should also be noticed that the optimal grid structures were calculated for a range of line widths. This approach was used to account for the possibility of line width variation during

the printing process due to unstable atomization. The final assumptions needed were the expected geometric values of the bus bar.

Table 23. Map of number of contacts to apply to each cell for a given line width to achieve an optimal grid structure assuming an aspect ratio of 0.1.

	T3874			T3826		T3889	T3704	
Line width (μm)	**1**	**2**	**3**	**1**	**2**	**1**	**1**	**2**
25	7	7	7	7	7	9	11	8
24	7	7	7	7	7	9	12	8
23	7	7	7	7	7	10	12	8
22	7	7	7	7	7	10	12	9
21	8	8	8	8	8	10	12	9
20	8	8	8	8	8	10	13	9
19	8	8	8	8	8	11	13	9
18	9	9	9	9	9	11	13	10
17	9	9	9	9	9	12	14	10
16	10	10	10	10	10	12	14	11
15	10	10	10	10	10	13	15	11
14	11	11	11	11	11	13	16	12
13	12	12	12	12	12	14	16	13
12	14	14	14	13	13	15	17	14
11	15	15	15	14	15	16	19	16
10	17	17	17	16	16	18	20	17

A decision was made to deposit the bus bar in 10 layers, which was estimated to result in an average height of 5 μm. This information, along with the above material properties and an average set of solar cell properties were input into the model resulting in a calculated optimal busbar width of 140 μm. This bus bar width was assumed in the determination of the optimal grid structure for each of solar cells. The result of all modeling efforts can be seen in Table 23.

The data in Table 23 was used by estimating the line width that will be deposited on each particular sample. Due to the difficulty in controlling the atomization process, it was assumed that the most likely line width would be 20 μm. As can be seen by the highlighted row, the number of collector lines to include in the current collector grid for each sample is given. By

comparing the data in Table 21 with the data in Table 23 a clear relationship between optimal number of collector lines and R_{sh} can be seen, with higher R_{sh} necessitating more collector lines for optimum performance.

5.2. Deposition and Characterization of Solar Cell Grids

After determining the optimal grid structure for each of the solar cells, preparations were made for depositing the collector grids. A new ink consisting of 0.5 mL of the ink stored at room temperature in the ink aging study and 0.5 mL of deionized water was mixed in a standard ink atomization vial (VWR, catalogue # 23050-026). A carrier flow rate of 15 sccm and a sheath gas flow rate of 30 sccm were used in the printing of all samples. The deposition velocity was set to a standard value of 10 mm/s. The substrate was heated to 150 °C and the deposition of each of the collector grids was and busbars was performed. Each set of collector grid lines was deposited in 20 passes, while only 10 passes were used on each of the bus bars. The samples were then sintered at 300 °C for one hour in the tube furnace (SPX Thermal Product Solutions, model number STF55346C-1) with an air flow rate of 5 standard cubic feet per hour (scfh).

Table 24. I-V data from solar cells having current collector grids of Novacentrix ink.

	T3874			**T3889**	**T3826**		**T3704**	
	1	**2**	**3**	**1**	**1**	**2**	**1**	**2**
V_{oc} (V)	0.613	0.636	0.633	0.636	0.633	0.637	0.571	0.572
J_{sc} (mA/cm^2)	34.4	34.6	35.5	30.7	34.2	34.5	27.8	29.2
FF	0.631	0.746	0.615	0.658	0.590	0.617	0.367	0.430
V_{mpp} (V)	0.455	0.505	0.455	0.455	0.444	0.444	0.283	0.333
J_{mpp} (mA)	29.2	32.5	30.4	28.2	28.8	30.5	20.6	21.6
V_{oc} slope (Ω)	3.03	2.27	3.58	4.44	5.19	5.02	18.4	11.5
Efficiency (%)	13.3	16.4	13.8	12.8	12.8	13.6	5.82	7.18

After sintering the samples were characterized using the solar cell test station to establish a performance baseline. The baseline results for each of the samples can be seen in Table 24.

The samples deposited on substrate T3874 were then left in air for 66 hours to see whether cell performance would degrade over that time period. For samples T3874-1 and 3 there were only very small changes. However samples T3874-2 saw an increase in cell efficiency of 0.8%. This was likely due to a mask misalignment in the baseline measurements, as indicated by the increase in J_{sc} seen in the data of Table 25.

Table 25. I-V data for samples on substrate T3874 after 66 hours in air.

	T3874		
	1	**2**	**3**
V_{oc} (V)	0.615	0.639	0.634
J_{sc} (mA/cm^2)	34.2	36.2	34.5
FF	0.623	0.743	0.631
V_{mpp} (V)	0.455	0.515	0.465
J_{mpp} (mA)	28.8	33.4	29.7
V_{oc} slope (Ω)	3.11	2.26	3.55
Efficiency (%)	13.1	17.2	13.8

The atomization system performed very erratically during the deposition of the samples, resulting in non- optimum grid structures on the majority of the samples. In anticipation of this, a representative collector line was deposited on an ITO coated piece of p-type silicon immediately after the deposition of each collector grid structure. These samples were then sectioned and high-resolution SEM images were taken of the cross sections to estimate the actual line width and aspect ratio achieved for each collector grid. This data was then used to compare the cell performance losses to those predicted by the model.

5.3. Comparison to Modeled Results

In order to compare the actual results to those input in the model another set of Suns-V_{oc} measurements were conducted on all of the samples to determine the maximum efficiency and operating characteristics that could be expected from each of the solar cells. As a reminder, the model works by predicting the percentage of power loss while the cell is operating at its maximum power point. Therefore, by inputting the deposited current collector grid dimensions and material properties into the model, along with the Suns-V_{oc} measured J_{mpp} and V_{mpp}, a predicted fractional power loss value can be calculated. However, it needs to be emphasized that this process is heavily dependent upon the accuracy of the model input parameters.

The representative grid finger samples were processed in exactly the same manner as the solar cells themselves. Following the sintering process, the representative grid fingers sectioned and imaged using SEM. These images were used to estimate the aspect ratio of the actual grid fingers deposited onto the solar cells. Once this data was obtained, it was then possible to predict the fractional power loss each cell would exhibit as a result of the current collector grid. The predicted fractional power loss for each solar cell can be calculated as follows:

$$\Delta P_{predicted} = \Delta P_E + \Delta P_C + \Delta P_F + \Delta P_{FS} + \Delta P_b + \Delta P_{bS} \tag{36}$$

$\Delta P_{predicted}$ is the predicted total fractional power loss. The other terms in Eq. (36) are as previously defined. The calculated value for the predicted fractional power loss can then be compared directly with the measured fractional power loss value as calculated below in Eq. (37).

$$\Delta P_{measured} = \left(1 - \frac{J_{mpp}V_{mpp}}{J_{mpps}V_{mpps}}\right) \tag{37}$$

$\Delta P_{measured}$ is the measured fractional power loss computed from the measured maximum power point current density and voltage values, J_{mpp} and V_{mpp}, and the corresponding Suns-V_{oc}

maximum power point values, J_{mpps} and V_{mpps}. A direct comparison of these values can then be made by plotting $\Delta P_{measured}$ versus $\Delta P_{predicted}$. Ideally, the resultant plot would be a straight line, however, as is clear from the plotted data in Figure 67 there is substantial deviation from the expected straight line for some of the data points.

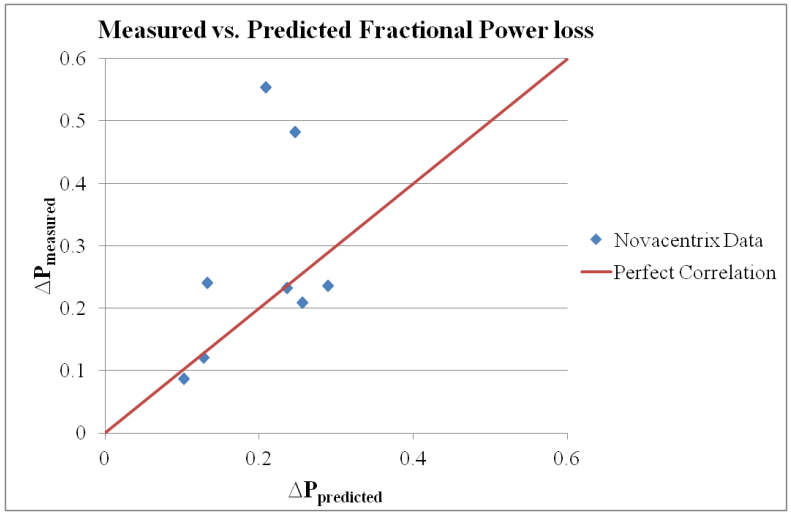
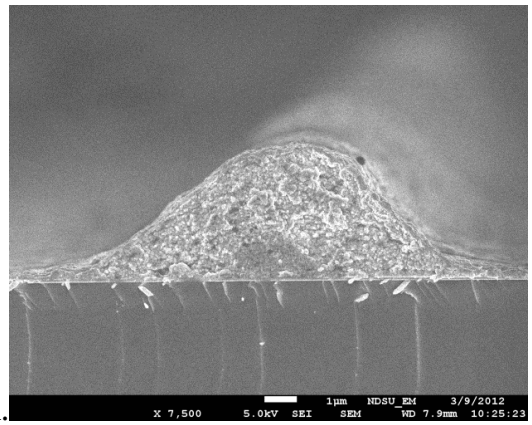


Figure 67. A plot of the measured fractional power ($\Delta P_{measured}$) loss against the predicted fractional power loss ($\Delta P_{predicted}$).

Upon further investigation, it was generally found that the errant data points were from samples in which the current collector lines were of very poor quality, much narrower and thinner than expected.

A. 

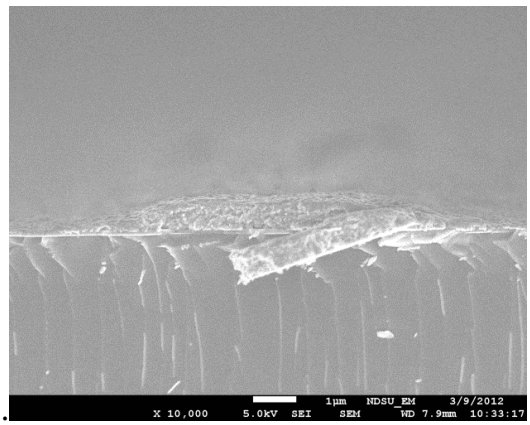
B. 

Figure 68. High resolution SEM images of representative grid finger cross-sections from A.) sample T3874-1, and B.) T3704-1.

As a result of this it is much more likely that the estimated geometric properties of the grid structures, which are critical to the modeling effort, are not truly representative of the entire structure. To give light to this point a comparison between representative grid fingers from samples T3874-1 and T3704-1 is made in Figure 68.

It must be emphasized that despite the apparent differences in the above images, the estimated aspect ratio for samples T3874-2 and T3704-1 are surprisingly similar at 0.068 and 0.062 respectively. This is due to the rather large amount of overspray associated with otherwise high aspect ratio depositions.

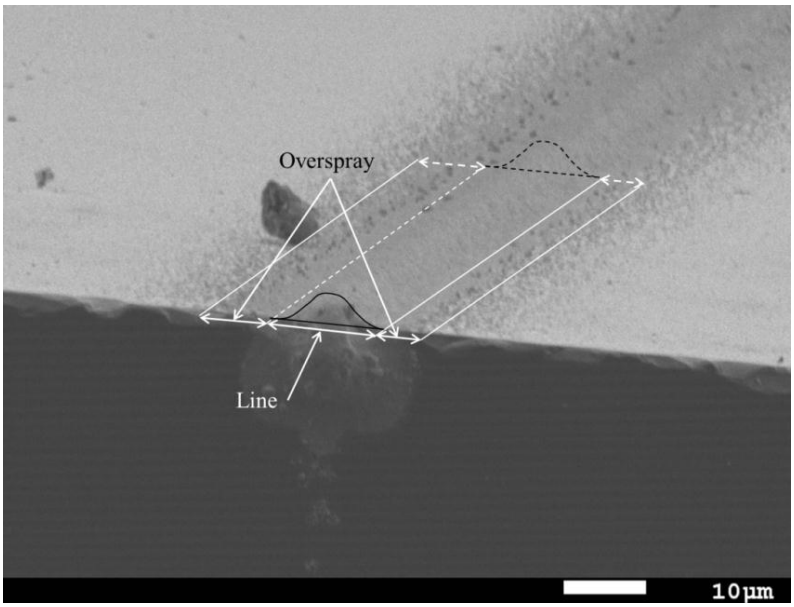


Figure 69. High resolution SEM image demonstrating large amount of overspray associated with high-aspect ratio lines (sample T3874-1).

A clear demonstration of the amount of overspray that can build up after printing multiple passes can be seen in Figure 69. Note that the overspray is almost as wide as the line itself. The excessive overspray effectively decreases the aspect ratio of the line significantly, as a larger active area of the solar cell is shaded.

Furthermore, each of collector grid fingers in this study was deposited using 20 passes. As such, the resulting low aspect ratio lines which occurred in some of the samples are indicative of very poor atomization of the silver ink. Such poor atomization can be very irregular, resulting in large variations in grid finger cross-sectional area and continuity, both of which directly affect the performance of the resulting collector grid. A clear example of this can be seen below in Table 26.

Table 26. Comparison of predicted and actual power loss, and resulting efficiency

	T3874			**T3826**		**T3889**	**T3704**	
	1	**2**	**3**	**1**	**2**	**1**	**1**	**2**
$\Delta P_{predicted}$	0.128	0.102	0.133	0.236	0.289	0.255	0.208	0.247
$\Delta P_{measured}$	0.121	0.086	0.241	0.233	0.236	0.208	0.554	0.482
Error (%)	5.30	18.4	44.8	1.56	22.7	22.6	62.4	48.9
Aspect ratio	0.063	0.068	0.041	0.020	0.019	0.018	0.061	0.062
Design line width (μm)	20.0	20.0	20.0	20.0	20.0	20.0	20.0	20.0
Deposited line width (μm)	22.2	22.7	23.7	19.3	14.5	13.0	10.1	8.60

The largest deviation from the designed grid structure can be found in sample T3704, which is also the poorest performer out of all prepared samples. In this sample the deposited grid fingers were much smaller than intended in the design. Furthermore, the ITO layer on both solar cells of the sample had a very large sheet resistivity of 380 Ω/□ for T3704-1 and 110 Ω/□ for T3704-2. Therefore, any decrease in the current collector grid function has a much larger effect on the fractional power loss.

With all of these contributing factors in mind, it is no surprise that such a large disagreement between the modeled fractional power loss and the measured fractional power loss could be seen for some of the samples. It must be reemphasized that the purpose of this study has been to demonstrate high-efficiency solar cells with current collector grids deposited completely by CAB-DW. As such, the model seems to have served its purpose as a design tool quite well.

As a final remark, an attempt to compare the results obtained from the same solar cells with current collector grids deposited using PV-Nanocell silver ink proved unsuccessful due to a lack of the key information required for the simulation. As such, no theoretical results are presented regarding the samples prepared using PV-Nanocell ink.

6. SUMMARY AND RECOMMENDATIONS

The recent drive toward highly efficient low cost renewable energy has sparked huge growth in the photovoltaics industry. The appeal of a nearly endless supply of carbon free energy has been met with the reality of increased energy cost however. In order to decrease manufacturing and material costs while increasing efficiency, novel manufacturing processes and materials are needed that push the limit of what is currently possible. Non-contact direct write processes such as Aerosol Jet, ink jet, nScrypt, and CAB-DW all strive to become viable current collector grid deposition processes that can produce grid fingers <100 µm in width.

Using an established modeling method taken from literature, it has been demonstrated that the CAB-DW system has a clear advantage over the competition with regard to its ability to deposit optimal grid finger widths. This was then demonstrated by depositing high aspect ratio grid fingers onto SHJ and diffused junction solar cells provided by NREL. Reasonable efficiencies of 15.8% and 17.2% were demonstrated using two different nanoparticle inks. It was also demonstrate both theoretically and experimentally that the fractional power loss could be reduced to only 8% relative of the maximum theoretical power output as measured using the Suns-V_{oc} method. The importance of ink aging when using nanoparticle based inks was also studied in this work. It is highly important that the electrical properties of the material used to create the current collector grid are known and accurately tracked over time. Failure to do so can result in increased electrical performance and substantial losses in cell efficiency.

Although the study has demonstrated that highly efficient current collector grids can be deposited using the CAB-DW system, more work with regard to increasing the efficiency of the deposition process must be conducted. The limiting factor in the laboratory trials was in all cases

the ability to produce stable and repeatable depositions especially when depositing grid fingers in the ~ 10 μm range. The root cause of this was an inability to produce a stable aerosol source using ultrasonic atomization. A stable source would be needed in order to realize a full scale industrial process centered on the CAB-DW system. The industrial feasibility of the Aerosol Jet deposition system, along with ink jet as a method to deposit a seed layer of silver for the LIP process has already been demonstrated, and could easily be adapted for the CAB-DW system. Future work should be centered on stabilizing and optimizing the atomization process to provide a better feedstock with which to make high aspect ratio depositions.

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