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An RF CMOS Implementation of an Adaptive Filter for Narrow-Band Interferer Suppression in UWB Systems

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AN RF CMOS IMPLEMENTATION OF AN ADAPTIVE FILTER FOR NARROW-BAND INTERFERER SUPPRESSION IN UWB SYSTEMS

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AN RF CMOS IMPLEMENTATION OF AN ADAPTIVE FILTER FOR NARROW-BAND INTERFERER SUPPRESSION IN UWB SYSTEMS

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Ultra-wideband (UWB) technology is a new type of technology for wireless communication that is based on the transmission of low power sub-nanosecond pulses. UWB communication utilizes a large bandwidth that overlaps and is coexistent with other wireless communication standards that can be also considered as narrow-band interferers. Because UWB systems are highly susceptible to narrow-band interferers, there is a demand for interferer suppression. An adaptive filter consisting of a two-element diversity receiver that performs minimum mean square error combining (MMSE) by the LMS algorithm is proposed. Thereby the elements of the LMS algorithm as well as the receiver LNA were implemented in an analog RF integrated circuit using 0.13μm CMOS technology. A former research project in 0.25μm CMOS proved operation of the algorithm and attained 14.5dB interferer suppression for the bandwidth from 800MHz to 970MHz.

In this research project, SpectreRF simulations of the implemented design show an interferer suppression of more than 30 dB for interferer levels of up to -10dBm at an operating frequency range of 1GHz to 3GHz. The total average noise figure, in case of no present interferer becomes 6.2dB.

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Chapter 1

Introduction

Ultra wideband (UWB), which sounds like a rather general term, is however, a new specific type of technology for wireless communication systems. Whereas sinusoidal carrier modulation techniques are currently the conventional methods for wireless communications, UWB is based on the modulation of sub-nanosecond pulses.

The origins of pulse transmission go back to two of the pioneers of wireless communications, Heinrich Hertz and Guglielmo Marconi, who used electric sparks to induce radiated electromagnetic waves. Later, the invention of vacuum tubes and first transistors lead to the rise of sinusoidal modulation technologies, which displaced pulse transmission methods. The major reasons why pulse transmission had not further been established was because of technical difficulties generating short pulses, the limited attainability of bandwidth of the RF components and a later on, the limited availability of non-interfering bandwidth, with other communication standards.

Driven by the significantly increasing demand for high data rates in consumer wireless applications, research and development has started to put a greater focus on pulse transmission again. According to Shannon [26], the channel capacity, which is a theoretical upper bound for the maximum net data rate that can be attained for given bandwidth B

and signal to noise ratio (SNR), is described by 1.1.

$$C = B \log (1 + \frac{S}{N}) \tag{1.1}$$

It can be seen that high capacity can be attained with high bandwidth, whereby increasing the transmitted signal power S would only logarithmically increase the capacity. Inversely, for a linearly extended bandwidth the transmitted power can be decreased exponentially and maintain the same capacity.

UWB technology uses short pulses in time domain that exploit a wide bandwidth, with low spectral power density. Thereby the bandwidth, may intersect with other utilized frequency bands, and the absolute value of the transmitted power spectral density has to be low enough, so that other wireless communication standards will not get distorted, and are not able to distinguish between UWB signal and noise. The problem is the definition of this power threshold, which started a large controversy in recent years, due to concerns of current wireless service providers.

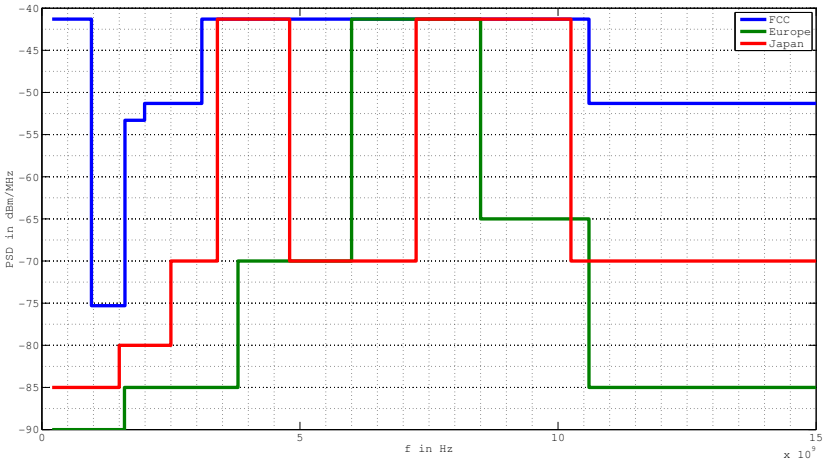


Figure 1.1: UWB spectral masks from different countries

The Federal Communication Committee (FCC), which is the frequency regulation

authority in the USA, were the first entity that allowed the unlicensed use of UWB and specified an allowable spectral mask (Fig. 1.1) in their Part 15 regulations. Other countries followed with different spectral masks, however the US is seen as a UWB-friendly area. In the US, the power limit of the maximum emitted power is located at the frequency range of 3.1 to 10.6 GHz, which made this range a major focus for research and development for UWB technology. The maximum equivalent isotropically radiated power (EIRP) by a UWB sender is -41.3dBm/MHz. In comparison, thermal noise of 1 MHz Bandwidth has the power of -114dBm, which gives UWB a theoretical available signal-to-noise ratio of about 73dB.

Furthermore, the FCC defined that a UWB signal can be any wide-band signal that occupies a larger -10dB bandwidth than 500MHz or a fractional bandwidth of 20% from its center frequency. It is not specified that a UWB signal shall be generated by pulses. Two major technologies for UWB communication have since emerged; they are called *Impulse Radio UWB* and *Multi band UWB*.

1.1 UWB Technologies

1.1.1 Impulse Radio UWB

In impulse radio UWB technology, a high bandwidth signal is generated by specific sub-nanosecond pulses, which are DC-free and utilize the targeted bandwidth. Many of theses pulses together build a pulse train, which can represent a data stream, if a certain type of modulation is applied on the pulses. Equivalent pulse modulation methods to conventional digital sinusoidal modulation techniques like OOK, ASK and BPSK, are possible pulse modulation techniques. In addition, pulse position modulation (PPM), an orthogonal modulation method has been high popular. PPM will be discussed in more

detail in the next chapter. The pulse repetition time determines the maximum achievable data rate and each pulse of the data stream covers the entire spectral bandwidth, but the pulse repetition time is by some factors lower than the utilized bandwidth. This shows that IR-UWB introduces a system gain, that allows for a decrease the transmitted power. IR-UWB enables the generation of a UWB signal without the use of a carrier frequency signal. RF hardware such as frequency conversion mixers, local oscillators, and PLLs are not necessary for that type of technology, because the generated baseband signal is directly transmitted and received without any frequency conversion.

1.1.2 Multiband UWB

The general idea behind multi-band UWB is to attain a wide-band signal by multiple signals of smaller bandwidth that are non-overlapping in frequency domain. In contrast to MB-UWB, the previously described IR-UWB, can be seen as single- band UWB. In some literature it also called pulsed multiband. Pulsed multiband can be seen as a extension of IR UWB, and is still a pulse band method. A further more conventional UWB technology is called multi band OFDM. The WiMedia Alliance [1] a non-profit open industry association has specified a communication system with UWB orthogonal frequency division multiplexing (OFDM). Some literature also calls this type of technology time-frequency interleaved OFDM (TFI-OFDM). UWB OFDM utilizes a large bandwidth of non-overlapping frequency channels that are OFDM modulated. Each OFDM channel consists of many orthogonal subcarriers and each subcarrier is modulated by standard digital modulation (e.g. QPSK). Many subcarriers together represents am ODFM symbol that has a bandwidth of greater than 500MHz. These OFDM symbols are transmitted according to a time-frequency code.

In general, there is no advantage in the signal-to-noise ratio, if only one signal with

a 7.5 GHz bandwidth or 15 signals with 500MHz bandwidth are transmitted. However, multi-band UWB has more flexibility than single-band UWB. So the transmission can always be adjusted to a specific spectral mask. And in case of a distortion narrow band interferer, one channel can be turned entirely off, which results in a lower data rate, while the signal transmission is not interrupted. Nevertheless, multi-band UWB increases the complexity of transmitter and receiver.

1.2 Characteristics of UWB Communication

According to [11] and [12] and major characteristics of UWB Communication are summarized:

- High data rate:

  The most important advantage of UWB is its capability to reach a high data rate without occupying additional frequency bands. Since the available frequency spectrum itself can be seen as natural resource, UWB utilizes the channel capacity not used by narrow-band sinusoidal communication systems. The coexistence of UWB and other communication standards, can therefore be seen as a more effective bandwidth utilization. In the technical proposal IEEE 802.15.4 [2] a data rate of up to 100MBit/s for 10m distance and up to 480MBit/s for 4 m distance is specified.

- Multi-path fading immunity:

  An optimal Rake-type receiver can diminish the effects of multi-path fading on the UWB signal. This property makes the technology attractive for indoor communication.

- Ranging and communication:

  The high bandwidth allows a very accurate resolution for ranging applications.

Furthermore, UWB is capable of simultaneously performing communication and ranging, which means the transmitted radar pulses can also contain information. This can lead to new types of applications, e.g. an automotive collision avoidance radar.

- Communication distance:

  The low transmitted power has the effect of limiting the maximum range of a UWB communication to a few meters. However, possible interferences with other communication standards are less likely because the UWB signal is kept locally.

- Budget:

  UWB transceivers can be integrated as a system-on-chip (SoC). Especially silicon CMOS will ultimately lead to lower power consumption and lower costs.

- Applications:

  A possible consumer application of UWB technology is wireless personal area networks (WPAN) that allow communication of personal devices (e.g. computers, TV screens, etc.) at home. Further applications are: Automotive systems could use UWB as a collision avoidance radar with very high accuracy. Wireless ad hoc networking, wireless sensor networks, RFID, consumer electronics, asset location, medical applications. [12]

- Interference:

  UWB is highly susceptible to narrow band interferers. This is primarily, due to the low transmit power of the useful signal in comparison to possible interferer levels. Furthermore, due to the high occupied bandwidth and the overlapping with other communication services there is a high likelihood that interferers are within the receiver bandwidth. IEEE 802.11a WLAN is especially considered an issue because

it has an operating frequency of 5.5 GHz, which is located at about the center of the FCC mask. This leads to the motivation of the thesis.

1.3 Thesis Motivation

As previously described, UWB signaling has capabilities to become a state-of-the-art communication technology for a large number of different applications. Narrow-band interferers, however, may lead to communication loss of IR-UWB signals and to data rate reduction in MB-UWB. This performance degradation of a UWB communication system creates the need of interference mitigation. Since the signal is spread over a large bandwidth narrowband filtering can suppress the interferer with only little effect on the useful signal. Even if the filter has its center frequency within the useful signal range, the useful signal can still be fully recovered at the receiver. However, in order to do any kind of mitigation, interferer parameters have to be known by the receiver. Adaptive filters automatically adjust their filter coefficients dependent on the interferer characteristics. A former research project [18] proved the feasibility of interferer suppression by an adaptive LMS filter. Thereby, an integrated circuit design using 0.25μm CMOS RF technology by TSMC was designed, manufactured, and tested. The research showed that within the frequency range of 800 MHz - 970 MHz a interferer suppression of 14.5 dB was possible. The availability of IBM 0.13μm technology through MOSIS [17] lead to the motivation for this further research project with a further implementation of the adaptive filter for UWB interference cancellation. Through the higher attainable technological upper corner frequency, the motivation in this project is to prove that the algorithm will also operate properly within a frequency band from 1GHz to 3GHz and shows a higher interferer suppression than 20dB.

Chapter 2

Effects of Interference on UWB

2.1 UWB Signaling

There are many UWB technologies that can be analyzed for the effects of narrow-band interferences. However, in this project, the analysis will be limited to impulse radio UWB.

Short time pulses that are transmitted carrier-less on the channel need to be easily generated, should have simple scaleable spectral characteristics, and should be DC free, because no DC can be transmitted wirelessly. Derivates of Gaussian pulses have been emerged as the most suitable for these requirements. By increasing the number of derivations the DC content can be reduced and the frequency content is shifted towards higher frequencies.

The function of the gauss pulse is described by (2.1). Its first derivative is called the gaussian monocycle pulse (2.2), and its second derivative gaussian doublet (2.3). [11] The only parameter that describes the gaussian function is the pulse duration time τ.

$$g(t) = K\, e^{-\left(\frac{t}{\tau}\right)^2} \tag{2.1}$$

$$g'(t) = g_1(t) = K_1 \frac{-2t}{\tau^2} \, e^{-\left(\frac{t}{\tau}\right)^2} \tag{2.2}$$

$$g''(t) = g_2(t) = K_2 \frac{-2t}{\tau^2} \left(1 - 2\frac{2t^2}{\tau^2}\right) \, e^{-\left(\frac{t}{\tau}\right)^2} \tag{2.3}$$

Whereby, K, K_1 and K_2 are normalizations factors to maintain the same signal energy for each deviation:

$$\int_{-\infty}^{\infty} g_n^2(t) \, \mathrm{d}t = E_S \tag{2.4}$$

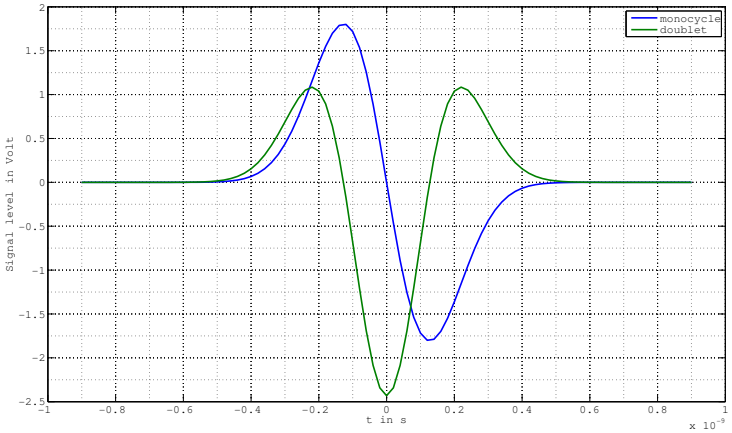


Figure 2.1: Gaussian Pulses

A sequence of these modulated gauss pulses generate the pulse train. Binary Antipodal Modulation (BAP) is described by (2.5) and Pulse Position Modulation (PPM) by (2.6).

$$w_{BAP}(t) = \sum_{n=-\infty}^{\infty} (1 - 2D) \, g_1(t - nT_f - T_c) \tag{2.5}$$

$$w_{PPM}(t) = \sum_{n=-\infty}^{\infty} g_1(t - nT_f - T_c - D\,\delta) \tag{2.6}$$

Whereby T_f represents the pulse repetition time, which equals to the symbol rate and also the bit rate, for the case that every bit is coded by one symbol. The spectrum of the UWB signal, will be the spectrum of gaussian pulse with the property that is it will have zeros at integer multiples of the symbol rate. These spectral zeros are undesired and depend on the transmitted bit pattern. Therefore a further modulation by a pseudo-random binary sequence (PRBS) is applied on the gauss pulses, which results in a noise-like spectrum. Depending on how the PRBS sequence modulation is performed this method is either called time-hopping UWB (TH-UWB) or direct-sequence UWB (DS-UWB). These two types can be seen as an analogy to spread spectrum modulation (THSS, DSSS).

Similarly, different PRBS codes can be used to facilitate multiple access in UWB communication. Equations (2.5) and (2.6) describe TH-UWB, whereby T_c represents a pseudo-random bit-shift derived from a pseudo-random code. The binary data is represented by $D = [0, 1]$. In PPM modulation the additional parameter δ, represents the modulation parameter, which determines the time shift distance.

The generated signal pulse train is now transmitted over the channel to the intended receiver. The receiver performs correlation and integration with a modified version of the original pulse, which is also called template. The reason for templates is that the channel characteristic will modify the original pulse shape. Template and received pulse need to be matched to achieve a matched filter receiver. If g(t) is normalized to have the signal energy Es, at a matched filter receiver Es will be extracted, if attenuation is neglected.

The ratio of the overall occupied bandwidth and the data bandwidth results in a *processing gain*, also called *duty cycle gain*. For example, in a UWB communication scenario where the gauss pulse duration equals 500ps, and the UWB signal is generated by a pulse repetition time of 10ns which equals the symbol rate of 100 MSymbols/s, the system gain is 13dB. The reason for this gain comes from the idea that noise bandwidth, before the

matched filter is larger than the noise bandwidth after filtering. The processing gain does not mean that the signal along the communication channel is amplified. It is rather a value on how much less energy a UWB sender can transmit the signal in order to still maintain the same bit error rate (BER) performance as for a communication through sinusoidal carrier modulation.

2.2 Interferer Signal

A narrow-band interferer can be simplified to a single sinusoidal tone with amplitude A_{int} and frequency f_{int}.

$$i(t) = A_{int}\, cos(2\pi f_{int} t + \phi) \tag{2.7}$$

The matched filter will also perform correlation on the interferer signal, which leads to the following equation.

$$\int_{-\infty}^{\infty} i(t)g(t)\,\mathrm{dt} = \int_{-\infty}^{\infty} A_{int}\,\Re\big(e^{i(\omega_{int}t+\phi)}\big)g(t)\,\mathrm{dt} \tag{2.8}$$

$$= \Re\bigg(\int_{-\infty}^{\infty} A_{int}\,\big(e^{i(\omega_{int}t+\phi)}\big)g(t)\,\mathrm{dt}\bigg) \tag{2.9}$$

$$= \Re\bigg(A_{int}\,e^{i\phi}\int_{-\infty}^{\infty} e^{i\omega_{int}t}g(t)\,\mathrm{dt}\bigg) \tag{2.10}$$

$$= A_{int}\,cos(\phi)G(\omega_{int}) = I(\phi,\omega_{int}) \tag{2.11}$$

Because receiver and interferer are non-coherent, the receiver will sample the interferer at different phases. This effect is expressed by the cosine term of 2.11. $G(\omega_{int})$ is the fourier transform of the gaussian pulse evaluated at the interferer frequency f_{int}. It becomes maximum if the interferer frequency is located at the center frequency of the UWB signal. In case the interferer is out-of-band, $G(\omega_{int})$ will be zero. The effect of the

interferer in signal space on binary antipodal is graphically described in Fig. 2.2.

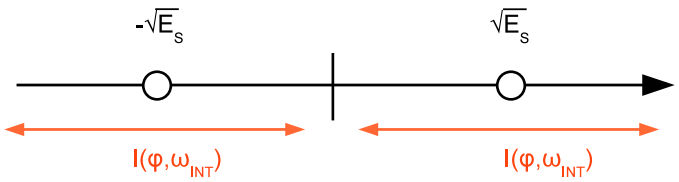


Figure 2.2: Interferer Distortion in Signal Space

While the useful signal will experience the processing gain, the narrow-band interferer however will remain constant.

2.3 BER Simulation

With the knowledge of the two previous sections, a bit error rate (BER) simulation with binary antipodal modulation of UWB pulses can be performed. Thereby, the complete simulation can be performed in signal space. The useful signal is simply described by the samples +/- $\sqrt{E_S}$. The interferer is described as samples of a cosine signal, with an energy of $A_{INT}^2/2$. The interferer power at the receiver is reduced by the processing gain. In this simulation the worst case scenario is considered, where the interferer frequency is located at the UWB center frequency. Additive white gaussian noise (AWGN) and hard decision maximum likelihood detection is modeled. The result of the BER simulation for a UWB signal with 1GHz bandwidth and a pulse repetition time of 200MHz can be seen in Fig. 2.3, whereby the parameter represents the interference to signal ratio ($\frac{I}{S}$).

It can be seen that the BER performance will considerably degrade for present interferers. Therefore, any kind of interferer suppression on UWB system has become a

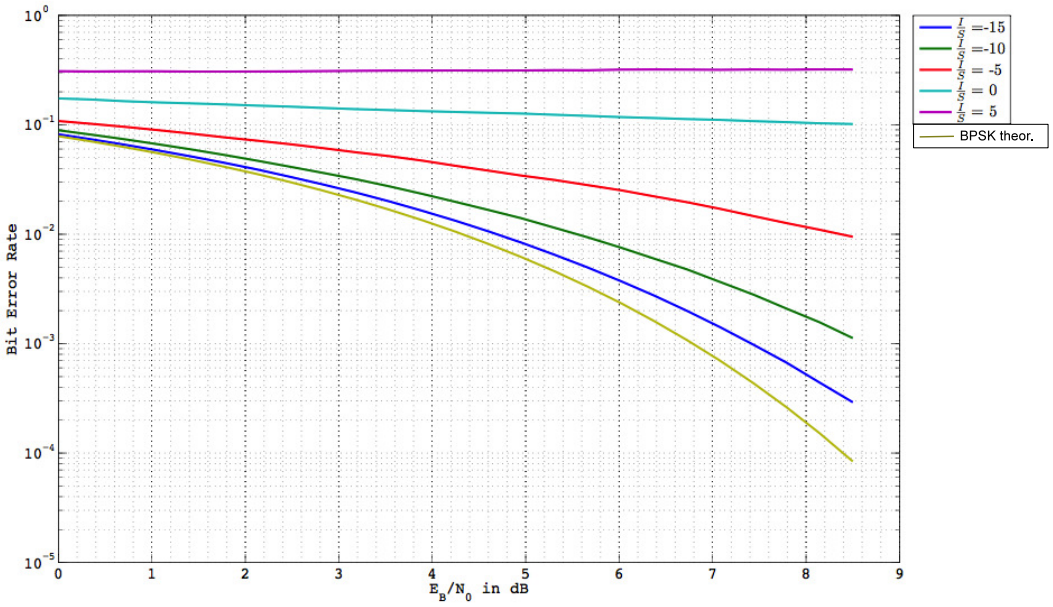


Figure 2.3: BER for an interferer at $\omega_i = \omega_s$

major focus on current research. The proposed adaptive filter will decrease the interferer amplitude, but also increase the noise power. An adaptive filter will lead to an overall performance improvement, if its introduced noise figure will introduce less BER degradation than the interferer. However, adaptive filtering will always be useful, if the interferer is so strong that the LNA stage will operate in compression and the signal link will be completely lost. The MatLAB code for the simulation can be seen in Appendix C.

The influence of narrow-band interferers on UWB M-array PPM is further discussed in [29].

Chapter 3

Interference Mitigation Methods

3.1 Signal Diversity Principle (Proposed)

In distorted communication channels induced by multi-path fading or narrow-band interferers, channel diversity can be a method to ensure stable communication. The idea behind signal diversity is to generate multiple copies of the original signal with the intention that in distorted channel the receiver can extract the signal information out of more available signals. This method will increase the signal communication reliability. The signal diversity can be generated at the transmitter and/or the receiver.

One way signal diversity can be attained is by utilizing more frequency bands that carry the same signal information. This is called *frequency diversity* and is usually generated at the transmitter. Multi-band UWB technology can also be seen as a frequency diversity if there are redundant frequency bands, or if only non-distorted frequency bands are utilized.

Time diversity, implies that the same signal is transmitted or generated more often in time. In UWB technology, Rake receivers generate time shift multiples at the receiver. At the transmitter, time diversity can be done by the T-R technique, where every UWB pulse

is sent multiple times and the delay times of those pulses are known at the receiver and are used for the correlation [9].

With *Spatial diversity* time shifted replicas are achieved by antenna arrays or independent antenna. Systems, where transmitter and receiver use multiple antenna are called *multiple input, multiple output* (MIMO), and belong to the space-time coding theory [27], that has become established high popularity in communication engineering research and development.

In this research project, a spatial diversity receiver with two antenna was implemented, which was able to cancel one single narrow-band interferer. In an antenna array, elements are close to each other (e.g. $\frac{1}{4}\lambda$ or $\frac{1}{2}\lambda$), which results in an overall antenna beam in a certain direction. Through beamforming, the direction of the major lobe can be directed towards the angle of arrival of the useful signal, so the interferer will not distort the communication link. This method can also be called *angle-of-arrival diversity*. A different method of making use of spatial diversity is to have independent antenna by setting the elements apart from each other to many λ. The hardware implementation of this research project can make use of both methods. Advantages and disadvantages of a short or long element distance will be discussed in detail in Chapter 4.

3.1.1 Spatial Diversity Receiver

In a spatial diversity receiver for IR-UWB, delayed copies of the signal are received. The time delay between the signal copies is a function of the spatial antenna separation and the angle of arrival. In Fig. 3.1 a example for an two element antenna array can be seen. The relation of the delay is described by (3.1), whereby c_0 is the velocity of light. Thus, if the angle of interferer and the angle of useful signal are different, the time delay between the elements will be also different.

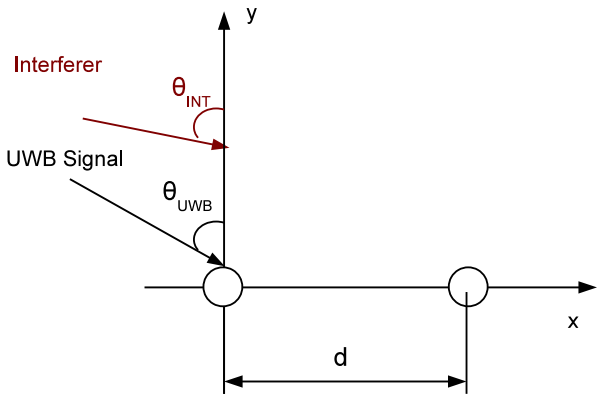


Figure 3.1: Two element Spatial Diversity

$$\tau = \frac{d}{c_0} \, cos(\theta) \tag{3.1}$$

Depending on what type of distortion on the channel is present, an optimum combining method of the diversity paths can be performed. There are several methods for combining the signal parts. Fig. 3.2 shows a general block diagram of a diversity receiver with two elements. It can be seen that each signal path is multiplied by gain $a_{1,2}$ and phase shifted by $\phi_{1,2}$ before both signal parts are combined together, whereby different methods on the selection of $a_{1,2}$ and $\phi_{1,2}$ has been established. [23].

In *selective combining* only one signal branch is selected that has the best communication conditions. In this case, the gain of all branches is set to zero, with the exemption of one selected branch. In [5] a method of interferer suppression by the method of selective combination with the use of signal diversity is shown. This demonstrates how described that the interferer in UWB no-line-of-sight communication channel suffers under Rayleigh

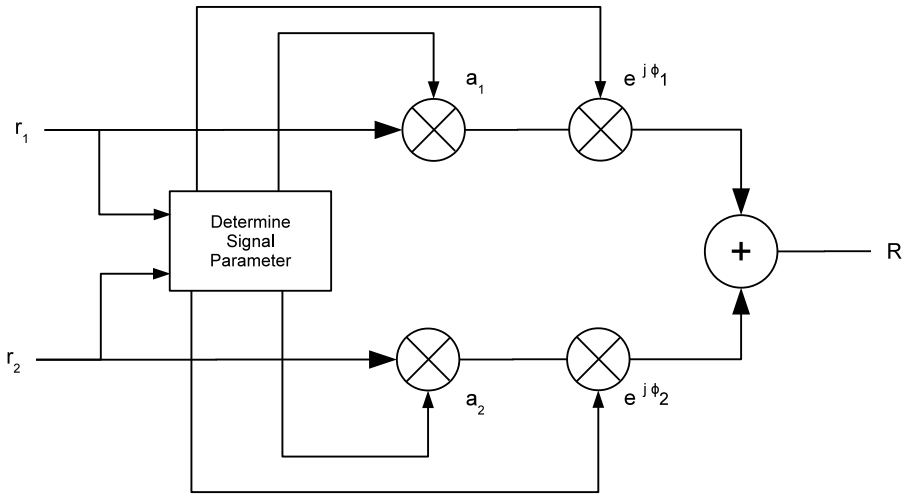


Figure 3.2: Spatial diversity receiver

fading by a much larger amount than the useful signal. By selecting the right signal branch, the interferer will be present at the receiver with a reduced power level.

With *Equal gain combining* all signal paths are shifted so that they are in aligned phase, and each signal branch is weighted equally. A more popular combining method is *maximum ratio combining* (MRC), where, in addition to the phase coherence, every signal path is weighted by its signal strength. Both methods are used in multi-path fading distorted channels, but are not useful for interference cancellation.

An effective method for interference cancellation is *minimum mean square error* (MMSE) combining. Thereby the weights and the phase of each signal path are selected in order to minimize the mean square error. The error $e(mT) = e_m$ is defined as the difference of sampled transmitted symbol $a_m = a(mT)$ and sampled received symbol $z_m = z(mT)$.

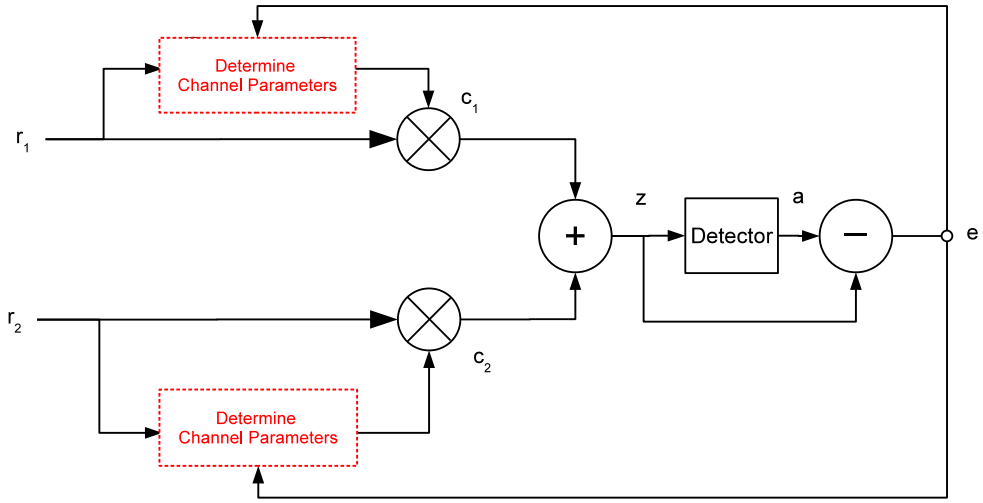


Figure 3.3: Spatial diversity receiver with MMSE combining

$$e_m = z_m - a_m \tag{3.2}$$

$$z(t) = c_1\, r_1(t) + c_2\, r_2(t) \tag{3.3}$$

$c_1 = a_1\, e^{j\phi_1}$ and $c_2 = a_2\, e^{j\phi_2}$ are the complex valued channel coefficients (Fig. 3.2). z(t) sampled at $t = mT$ leads to

$$z(mT) = c_1\, r_1(mT) + c_2\, r_2(mT) \tag{3.4}$$

Due to spatial element separation, it is assumed that $r_2(mT) = r_1(mT - \tau)$. For simplicity $r_1(mT) = r(mT)$. This will define the mean squared error (MSE) as:

$$J = E\Big\{ \left[(c_1\, r(mT) + c_2\, r(mT-\tau)) - a_m\right]^2 \Big\} \tag{3.5}$$

In order to find the minimum mean squared error, the gradient of zero has to be found. In the case of a two element array, this leads to two conditions.

$$I \quad \frac{\partial J}{\partial c_1} = 0 \tag{3.6}$$

$$II \quad \frac{\partial J}{\partial c_2} = 0 \tag{3.7}$$

With some calculation the equation array leads to: [22], [28]

$$I \quad c_1 R_r(0) + c_2 R_r(\tau) = R_{ar}(0) \tag{3.8}$$

$$II \quad c_2 R_r(\tau) + c_1 R_r(0) = R_{ar}(\tau) \tag{3.9}$$

$R_r(\tau) = E\{(r(mT)\; r^*(mT-\tau))\}$ represents the autocorrelation function and $R_{ar}(\tau) = E\{(a(mT)\; r^*(mT-\tau))\}$ the cross correlation function at time shift τ. Both equations have to be fulfilled at the same time to ensure that the minimum mean square error is achieved. The equation array can be also written in matrix form:

$$\begin{pmatrix} R_r(0) & R_r(\tau) \\ R_r(\tau) & R_r(0) \end{pmatrix} \begin{pmatrix} c_1 \\ c_2 \end{pmatrix} = \begin{pmatrix} R_{ar}(0) \\ R_{ar}(\tau) \end{pmatrix} \tag{3.10}$$

$$\boldsymbol{Z}\, \boldsymbol{c} = \boldsymbol{E} \tag{3.11}$$

Z represents the channel matrix and E the input vector. Now the value of c that will lead

to the MMSE of the spatial diversity receiver can be expressed by:

$$\boldsymbol{c_{opt}} = \boldsymbol{Z^{-1}}\, \boldsymbol{E} \tag{3.12}$$

The solution of MMSE combining for N antenna elements is determined in [23] and [22].

In case all channel parameters are always known to the receiver, both channel coefficients can be determined at once and applied to the receiver. However, in practical implementations the correlation functions are unknown and can only be estimated.

A more practical way to determine c_{opt} is to approach it iteratively by the LMS algorithm.

3.1.2 LMS Algorithm

The LMS algorithm (Widrow and Hoff) is a state-of-the-art algorithm for adaptive filters. It is an iterative algorithm, which means that the filter coefficients c_1 and c_2 from (3.4) are updated with every received symbol. Every filter coefficient will be updated independently by the same algorithm. Therefore, for simplicity the coefficients will be only described as c, which becomes c_k for the value of c at the k-th iteration. The filter coefficients are updated by a correction term g_k, which will be subsequently determined. The general algorithm can be formulated as:

$$c_{k+1} = c_k - \mu\, g_k \tag{3.13}$$

The value of μ represents a constant gain and determines the step size of the algorithm. The idea behind the LMS algorithm is that g_k is determined by the gradient of the error function with the steepest descent with respect to the channel coefficients. The steepest

descent is determined by the first derivation [22].

$$g_k = \frac{\partial J_k}{\partial c_k} \tag{3.14}$$

The algorithm adjusts iteratively and the values of c_k and g_k are approaching the optimum, however these values are estimated of the optimum value:

$$\hat{c}_{k+1} = \hat{c}_k - \mu \, \hat{g}_k \tag{3.15}$$

Now equation (3.5) is set into (3.14). According to [22] this will lead to:

$$g_k = -E(e_k \, r_k^*) \tag{3.16}$$

The signal e is the error described according to (3.2). $r(k)$ describes the k-th sample of r which equals the m-th sample $r(mT)$. Since the expected value of an estimate becomes the argument of the expected value, estimate $\hat{g}_k$ becomes

$$\hat{g}_k = -e_k \, r_k^* \tag{3.17}$$

Setting (3.17) in (3.15) leads to

$$\hat{c}_{k+1} = \hat{c}_k + \mu \, r_k^* \, e_k \tag{3.18}$$

If both filter coefficients c_1 and c_2 are updated according to LMS algorithm from (3.18) the block diagram of Fig.3.3 changes to the block diagram shown in Fig.3.4.

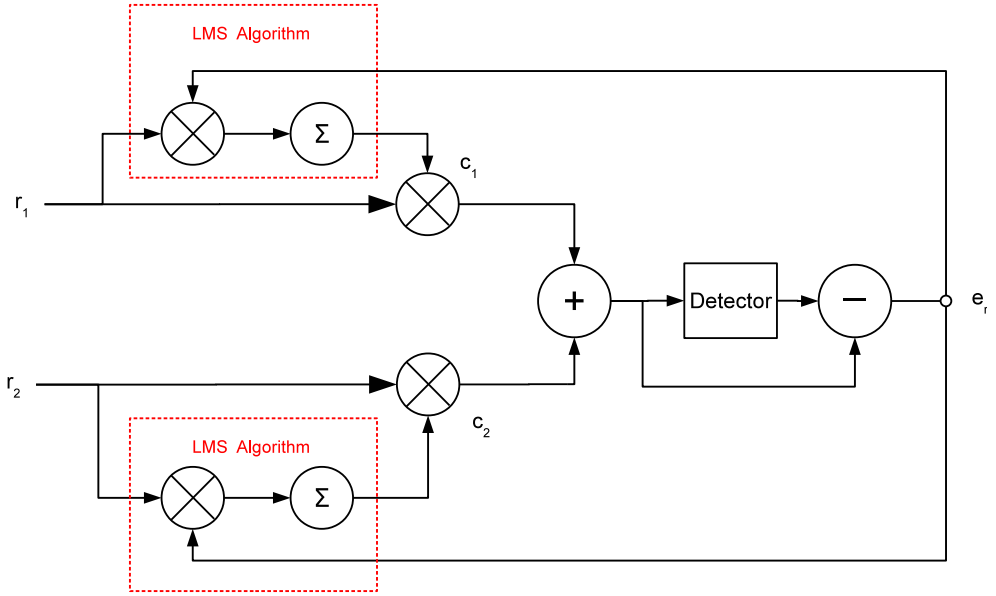


Figure 3.4: Spatial diversity receiver with LMS algorithm

3.1.3 Simplification for Hardware Implementation

The block Fig. 3.4 need to be simplified, so that the hardware implementation becomes less complex and more feasible. Since there are only two paths, it is not necessary that both paths are weighted by the filter coefficients. It is sufficient if one path stays constant and the other path is modified by the filter coefficient. The filter coefficient is then a constant, whereby only c_2 is iteratively updated according to the LMS algorithm.

$$z_m = kr_1 + c_2 r_2 \tag{3.19}$$

The error is previously defined as the difference between the received symbol z_m and the decided symbol a_m after the detector. It will be shown that, in the case for UWB interferer cancellation a detector is not necessary. Without the detector the error can be

simplified to (3.19).

$$e_m = z_m \tag{3.20}$$

Both simplifications lead to the simplified MMSE criterion and simplifies equation (3.10) to:

$$k\, R_r(\tau) + c_2\, R_r(0) \;=\; 0 \tag{3.21}$$

Equation (3.21) shows that without the detector every signal that goes through the filter is seen by the algorithm as an error. This raises the question of whether the useful signal will be suppressed as well. The reason for this comes from the specific interferer scenario on UWB signaling. There are three conditions necessary, which will later be proven by simulation.

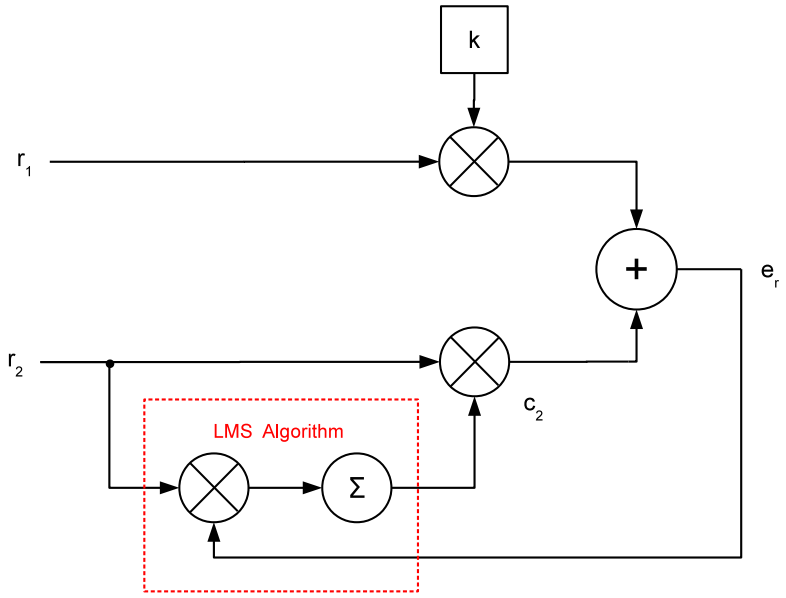


Figure 3.5: Block diagram of spatial diversity receiver with LMS algorithm

First, through signal diversity, it is given that under the right conditions, useful signal and interferer signal have different time delays $\tau_{UWB} \neq \tau_{INT}$. Second, it is also assumed that the power spectral density of the interferer is larger than the one of the useful signal. Last, it is assumed that the useful signal consists of short pulses in time. If all three conditions are fulfilled, the algorithm will try to suppress interferers and preserves the UWB power at the output. If the interferer power is many times larger that the UWB signal, $R_r(\tau)$ will become $R_r(\tau_{INT})$:

$$k\ R_r(\tau_{INT}) + c_2\ R_r(0)\ =\ 0 \tag{3.22}$$

The introduced error by the useful signal will be seen by the LMS algorithm as negligible and the algorithm will try to approach (3.22).

If the signal paths would be weighted by both filter coefficients c_1 and c_2, the LMS algorithm will be overdetermined, and with present noise the algorithm will find the trivial solution of $c_1 = 0$ and $c_2 = 0$. So the first simplification (3.19) is a required condition to be able to set the error $e_m = z_m$.

For the sake of convenience throughout the rest of this thesis, both branches according to Fig. 3.5 will be named as *path* r_1 and *path* r_2. Whereby path r_1 represents the major signal path and path r_2 the feedback path.

3.2 Further Methods

3.2.1 Rake-Reciever

In general Rake-Receivers are the extension of a matched filter-type receiver for multi-path fading distorted channels. A block diagram can be seen in Fig. 3.6. The implicit realized time diversity of Rake-Receiver can be also used for MMSE combining. Many

different articles refer to a MMSE Rake-Receiver for narrow-band interference cancellation [6],[3],[8],[4],[16]. However, they do not describe or show hardware realizations of Rake-Receiver for UWB.

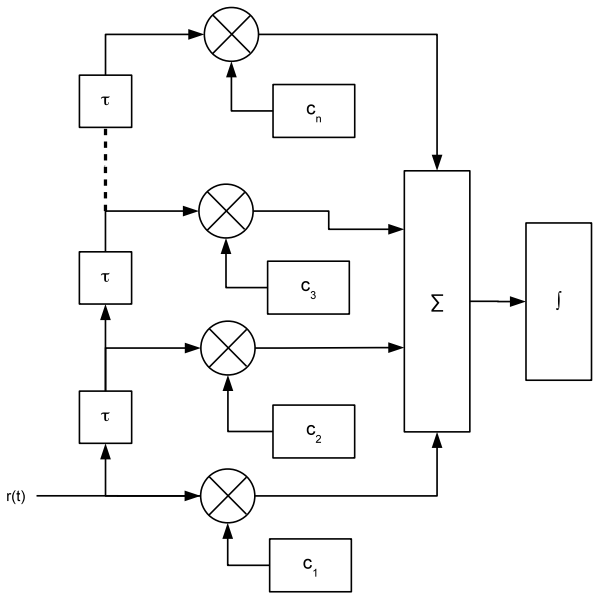


Figure 3.6: Rake-Receiver

A simplification to a two element MMSE Rake-Receiver, will lead to a very similar solution as the proposed solution, as can be seen in Fig. 3.7.

3.2.2 Notch Filter

A notch filter (band stop filter) with the center frequency of the interferer frequency would be able to suppress the interferer. The challenge of the using a notch filter is that its passband has to be flat over the entire pass band, which can be difficult for a bandwidth over several GHz. If the interferer frequency is unknown the notch filter needs to be adaptive to ensure reliable interferer cancellation.

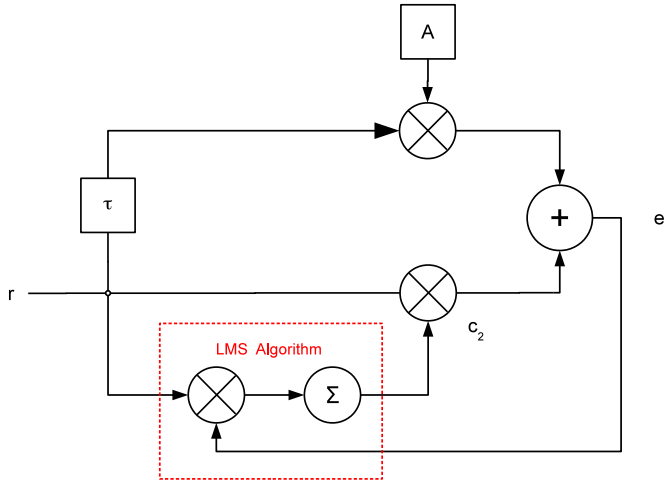


Figure 3.7: Two element MMSE Rake receiver

3.2.3 Delta-Method

In [8] the cross correlation of interferer and UWB template for Pulse Position Modulation can be expressed by:

$$R_i[k,l] = 4\ N_S\ P\ |W_r(f_I)|^2\ [sin(\pi f_i \delta)]^2 cos(2\pi f_i(\tau_k - \tau_l)) \tag{3.23}$$

Whereby, N_A is the number of pulses per symbol, P the interferer power and $W(f)$ the fourier transform of the useful signal evaluated at the interferer frequency f_I. In the special case of PPM modulation, the modulation parameter δ can be chosen to be $\frac{1}{f_i}$. This will bring the sine term of (3.23) to zero. If the interferer is narrow-band, with a certain bandwidth greater than zero, the value of δ needs to be chosen between the minimum and maximum frequency of the interferer.

3.2.4 Multicarrier Templates

[19] and [12] describe a receiver that correlates the received signal with special multi-carrier templates instead of using one single template that would correspond to the transmitted waveform. By the selection of the right modified multi-carrier template, interferer cancellation can be achieved, however the bit error rate in a non-interference scenario will increase.

Chapter 4

System Simulation in MatLAB

In the proposed design in Chapter 3, three conditions were assumed, to simplify the circuit:

1. $\tau_{UWB} \neq \tau_{INT}$
2. The interferer has a higher power spectral density
3. The useful signals are short pulses in time

The third condition will always be assumed, since this research project focuses only on interference mitigation in impulse radio UWB signals. It is not known how the proposed filter will behave if the other two requirements are not or only partially fulfilled. Furthermore it is uncertain how the distance between the antenna elements has to be chosen, to ensure the optimum performance, and what drawbacks may result from those. Last, the stability of the control loop has to be taken under consideration.

A system model in MatLAB was implemented according to Fig. 3.5 to give answers to these questions.

The useful signal consists of gaussian doublet pulses (See Fig. 2.1), which are modulated by pulse position modulation (PPM) and time hopping (TH) with a PRBS length

of 1023. There was no noise and no multi-path fading modeled in order to see the LMS performance on its own. The receiver was modeled according to Fig. 3.5.

The interferer is modeled as a single tone sinusoidal function.

4.1 Performance vs. Interferer Power

In order to get a relation of UWB signal energy and interferer energy, it is important to compare them within the same bandwidth. This can be achieved if the energy is calculated by integration over the same time window for both interferer and UWB signal.

The energy of the gaussian doublet is normalized by the the value of K_2. (2.3).

$$K_2 = \sqrt{\frac{\tau E_2}{\sqrt{\frac{\pi}{2}}}} \tag{4.1}$$

So that:

$$\int_{-T_f/2}^{T_f/2} g_2^2(t)\,\mathrm{d}t = E_S \tag{4.2}$$

$$\int_{-T_f/2}^{T_f/2} i(t)\,\mathrm{d}t = \frac{A^2}{2} T_f \tag{4.3}$$

With (4.3) the interferer energy is determined as the energy within one pulse repetition T_f. This energy can be compared to the energy of one single UWB pulse. This determines the interference-to-signal ratio l (ISR) per pulse. A time domain simulation with parameters shown in Tab. 4.1 was performed. The sampling rate was set to 40GHz.

ISR per Pulse	E_S	τ	T_f	θ_{UWB}	f_{INT}	θ_{INT}	μ	$d_{ELEMENT}$
40 dB	10^{-9}	$150ps$	50ns	270	2 GHz	90	$5 \cdot 10^{-7}$	0.25λ
10 dB	10^{-9}	$150ps$	50ns	270	2 GHz	90	$2 \cdot 10^{-3}$	0.25λ

Table 4.1: Simulation Parameters

Note: The calculated *ISR per pulse* in this Chapter is not equal to the *ISR* value used in the BER simulation of Chapter 2.

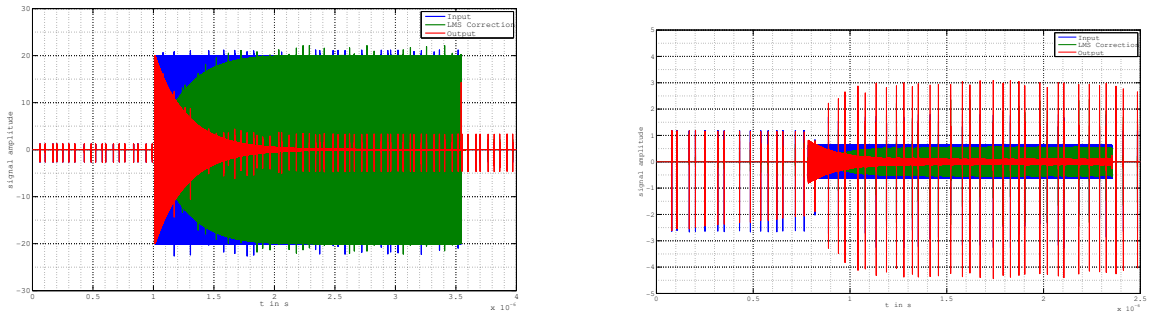
The effect of the element displacement will be discussed in the next chapter. The simulation result in time domain can be seen in Fig. 4.1. At $t = 0$ only the UWB signal is present. The interferer is then manually applied on the useful signal at $t = 1\mu s$ and turned off at $t = 3.6\mu s$. The interferer amplitude on the output of the filter decays and the algorithm finally converges after $t = 1.5\mu s$. When calculating an FFT out of the converged time domain signal, the frequency spectrum can be determined. (Fig. 4.2). The imaginary and real part of the filter coefficient c_2 of (3.22) can be seen in Fig. 4.6. Because the input amplitudes of both input paths are set the same, the absolute value of the filter coefficient has to converge to 1. It can be seen that the coefficient converges to the vale $0 - 1\,j$. This represents a negative 90° phase shift and correspons to the applied positive 90° phase shift θ_{INT} of the interferer signal between both input paths.

From the simulation results it can be concluded that the convergence time and the suppression ratio is increasing for lower interferer levels. The step size parameter can be set very large, to compensate for these effects, however as a result, ringing is a negative side effect of this method (See 4.4) and if goes beyond a certain threshold the algorithm becomes unstable.

4.2 Performance vs. Element displacement

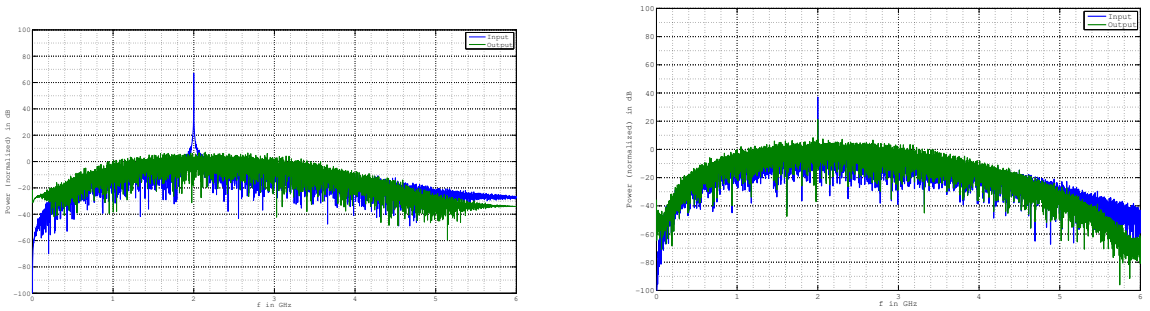
The element displacement, which is the distance between both antennas, is a key parameter of diversity receiver, because it determines the introduced time shift between both signal paths. Both UWB signal and interferer signal experience a time delay that is a function of the element displacement and their angle of arrival. (See Fig. 3.1)

First, it is considered that no interferer is present and only the useful UWB signal is



(a) (b)

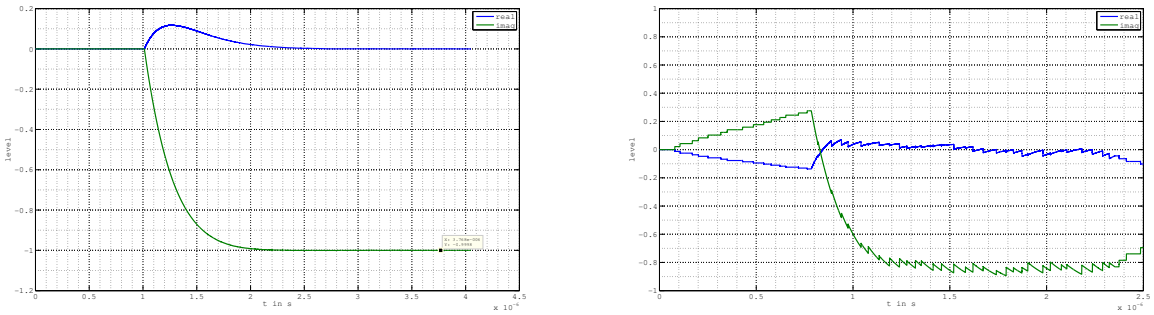
Figure 4.1: Time domain simulation a) ISR = 40dB b) ISR = 10dB



(a) (b)

Figure 4.2: Frequency domain simulation a) ISR = 40dB b) ISR = 10dB

received. For the case $\theta = 0°$ and $\theta = 180°$ the time delays of both signal paths are equal. This is the worst case scenario, since the UWB signal will be suppressed, because the LMS filter will adjust its coefficient to $+1 + 0j$ respective $-1 + 0j$ which always leads to destructive coherent combination. Correspondingly, for angles of arrival that are close to 180°, the output signal amplitude will be reduced.A simulation of the LMS filter output of this scenario was performed to get a better picture of this issue. The time domain characteristic of the pulse is seen in Fig. 4.5. It can be seen that due to the overlap of both pulses, the original pulse form gets reshaped and, depending on the angle of arrival, the



(a) (b)

Figure 4.3: Filter Coefficient a) ISR = 40dB b) ISR = 10dB

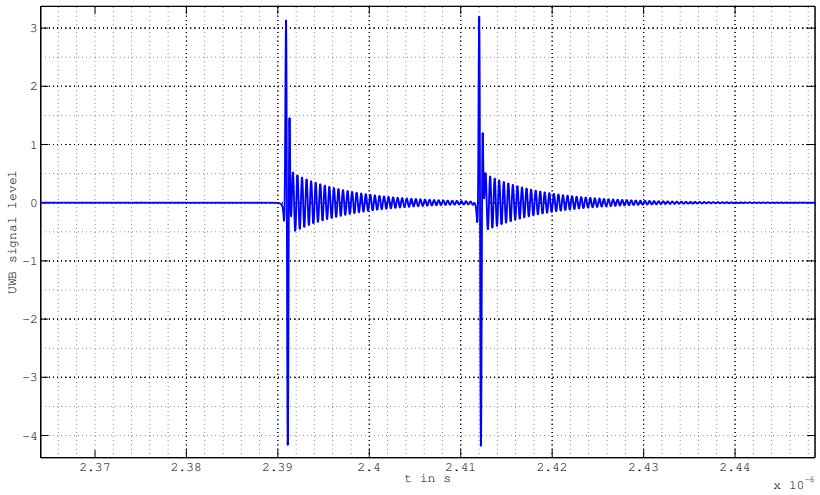


Figure 4.4: Step-size Parameter set very high results in ringing

output amplitude will be different, whereby the maximum output amplitude is attained at $\theta = 90°$. The angle of arrival dependency of the output amplitude is further illustrated by an angle diagram which is shown in Fig. 4.6. The diagram is normalized to the maximum amplitude.

Depending on the UWB demodulator the reshaped pulse must be taken into consideration for demodulation. The angle of arrival influence on the output amplitude

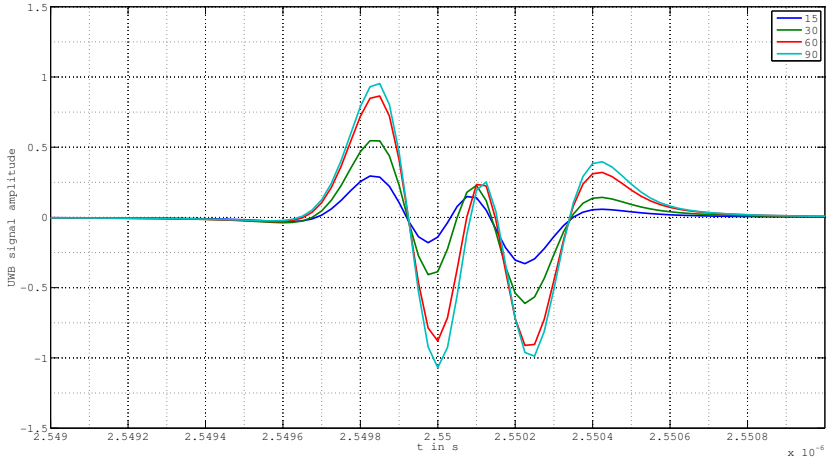
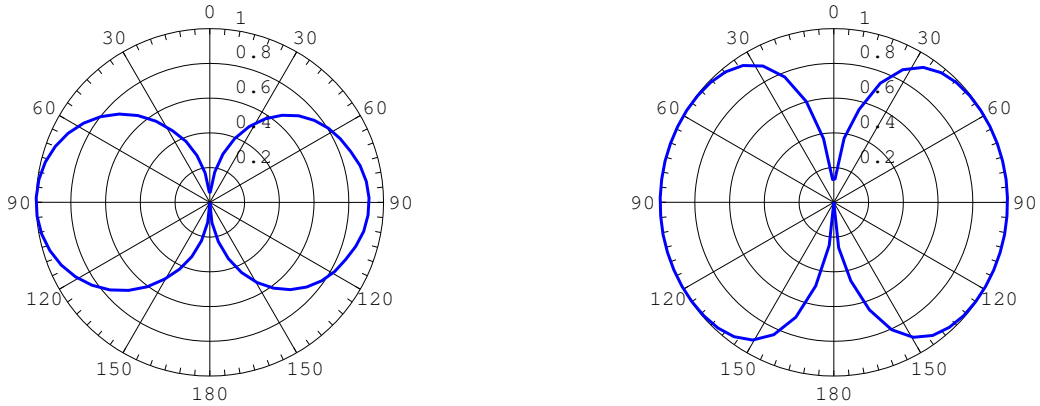


Figure 4.5: Time domain vs θ_{UWB}



(a) o .25 λ element displacement

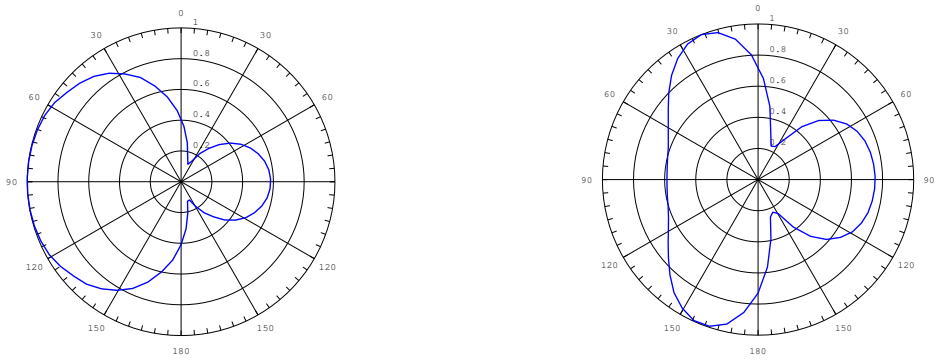
(b) λ element displacement

Figure 4.6: Antenna Factor with no interferer present

makes the communication unreliable or impractical for some applications, because the antenna need to be directed in the direction of the incoming useful signal wave. Some literature suggests that a diversity receiver should have an element displacement of many λ. [23]. If the element displacement becomes larger, the angle of arrival to amplitude dependency will be minimized, because a small deviation of the angle of arrival from

$\theta = 0°$ or $\theta = 180°$ for large element displacements will introduce such a large time shift, so that both signal path do not coherently combine anymore. In other words, the range of the angle of arrival that will lead to the signal cancellation becomes smaller. However for large element displacements both antenna will start to operate independently and there will be no further useful antenna array gain.

Now, the simulation was repeated, with the presence of an interferer to see how the LMS algorithm will change the antenna beam of the array for the case of small values of λ. This effect can be seen in Fig. 4.7, which shows that, if the interferer and useful signal have the same angle of arrival, both interferer signal and useful signal will vanish at the output of the filter. For interferers with certain angle of arrival, a broadside reception of the useful signal can become possible, which is never the case if there is no interferer present.



(a) 0.25 λ element displacement (b) 0.5 λ element displacement

Figure 4.7: Antenna Factor with present interferer from 30° angle

If the element displacement becomes larger, the effect on the antenna beam due to the interferer will vanish. The output pulse of the filter with respect to the element displacement λ is illustrated in Fig. 4.8 . It can be seen that a large value of λ will lead to the reception of two pulses. The algorithm will try to cancel the interferer by shifting the

received signal (UWB signal plus interferer) by +/- 180°. However, a +/- 180° phase shift of an interferer at, for example 2 GHz, equals to a time shift of the signal of +/- 250ps. In Fig. 4.8, it can be seen that the maximum introduced time shift becomes smaller than the element displacement induced time shift for larger element displacements ($> \lambda$).

Although a large displacement will not lead to a useful signal cancelation for interferers that arrive from the same angle, the reception of a double pulse need to be taken into consideration by the receiver, which introduces additional complexity. Furthermore, the minimum pulse repetition time and thus the data rate is limited by the duration of the double pulse. Depending on the system requirements and the amount of complexity, the right element displacement needs to be chosen. The proposed LMS filter according to Fig. 3.5 will operate in both cases.

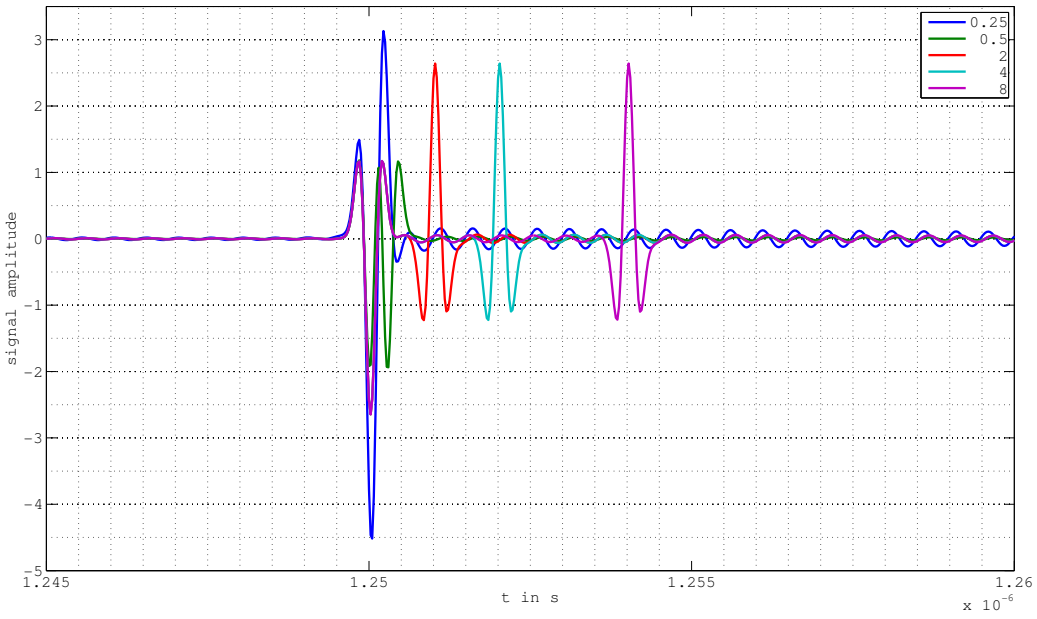


Figure 4.8: Amplitude vs θ_{UWB}

4.3 Stability

The LMS filter can be seen as a control loop with a certain gain and phase margin. It is important to consider the stability parameters especially for the hardware implementation. The details on the hardware implementation will be discussed in the next chapter. Each block used in the control loop will add some frequency dependent phase shift. This was done to determine, how this additional phase affect the filter performance, and what criteria are required so that the system can be considered as stable. In a simulation the feedback signal of the control loop, which is the error signal (See Fig. 3.5), was delayed by different phase shifts. The outcome of the filter performance with respect to the introduced signal phase delay is shown in Fig. 4.9 and Fig. 4.10.

The simulation shows that stable operation can be accomplished if the introduced phase delay is between -90° to +90°. An exact +/- 90° phase shift leads to an oscillation. A phase shift greater than 90° or smaller than -90° will lead to an inverse control loop that will lead to an behavior that will try to maximize the interferer amplitude. If in this case, the loop direction is inverted, e.g. by introducing an inverter in the control loop, a proper operation of interferer cancellation can be reestablished again.

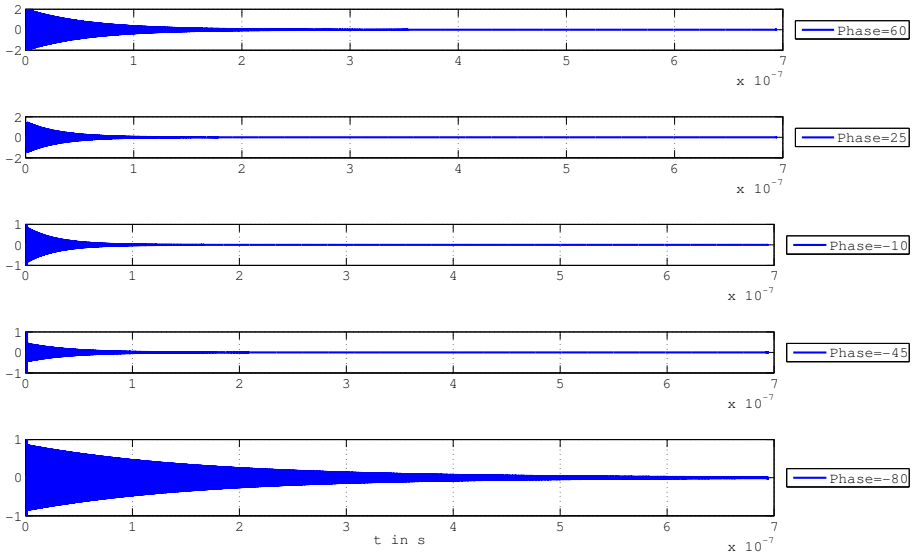


Figure 4.9: Filter Time Domain Output - Convergence vs. phase shift

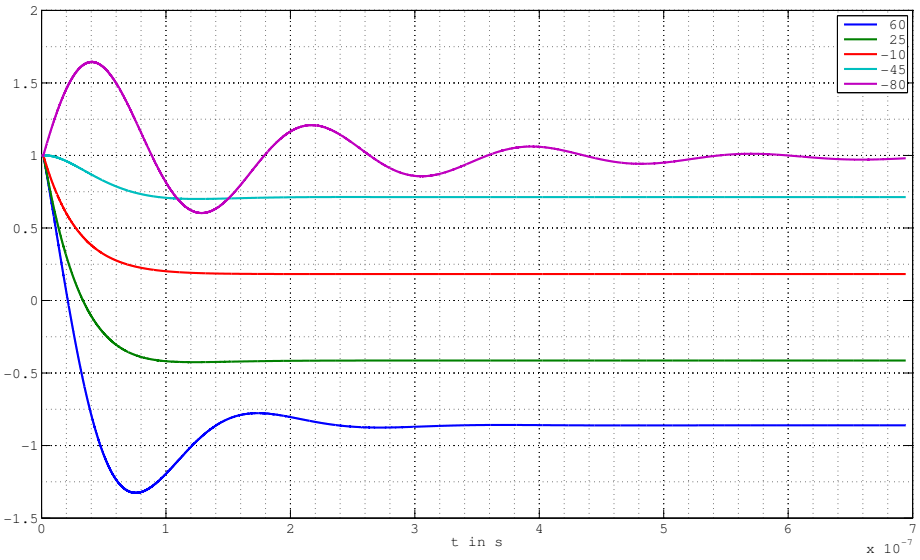


Figure 4.10: Filter Coefficient - Convergence vs. phase shift

Chapter 5

Hardware Implementation

5.1 Technology

One of the requirements and challenges of this research project was that the implementation of the proposed adaptive filter (Fig. 3.5) needed to show full functionality of interferer cancellation and UWB signal reception, within a range of 1 GHz to 3 GHz. This means that the implemented RF front-end need to be designed to comply to this frequency range. The hardware design is implemented in 0.13 μm IBM 8RF CMOS technology, which is accessible through MOSIS [17].

IBM 0.13 μm CMOS technology is offering following key features:

- 1.2 V core voltage
- RF transistor models
- Low voltage transistors with a 300mV threshold voltage
- Poly-silicon resistors
- Single and Dual MIM Capacitors

- Series and Parallel inductor models that uses 2 layers
- 8 layers of Metal: 3 thin, 2 thick and 3 top level metals

5.2 Theory to Hardware

The LMS filter according to Fig. 3.5 needs to be translated in parts that are feasible to realize in CMOS RF. A simplification can be seen in Fig. 5.1, whereby the entire circuit is analog and continuous time. Received signal r_2 and error e are multiplied and then integrated, whereas the result, filter coefficient c, will control the gain and phase of the path of r_2.

The value of c is a complex valued number and the variable gain amplifier (VGA) is a complex amplifier. In order to implement a complex multiplier, the multiplier inputs must be split into two components: The in-phase components r_{2I} and c_I and quadrature-phase components r_{2Q} and c_Q, which are 0° and 90° shifts of the original signal. In-phase and quadrature-phase component can then be seen as real and imaginary parts of c. A complex multiplier can now be implemented according to equation (5.1).

$$c\, r_2 = r_{2I}\, c_I + j\, r_{2Q}\, c_Q \tag{5.1}$$

From (5.1) it can be seen that two multipliers, one summation circuit, and a 0° and 90° input signal representation are necessary to implement a complex multiplier.

Usually multipliers are implemented by gilbert cells that require differential signaling, which means that input signals of each real multiplier must be present in a 0° and 180° representation. Furthermore, differential signals have some major performance advantages versus single-ended signaling, which are summarized in the following aspects:

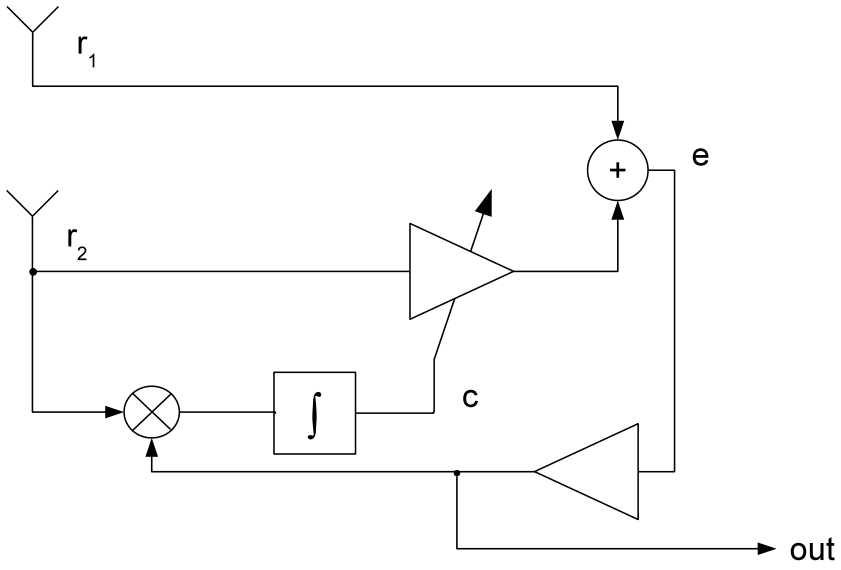


Figure 5.1: Abstract model of proposed block diagram

- In multipliers all second order intermodulation products will not affect the differential signal.
- Common mode noise immunity: Due to the low core voltage the signals are more vulnerable to additive noise which will not affect the signal if the same noise value is present on both signal parts.
- Voltage offsets will be cancelled

In order to generate a differential signal a balun-unbalanced circuit *balun* is necessary.

Additional simulations have shown that the filter performance can be improved, if the signal error is amplified, because it more highly penalize the error introduced by the interferer signal, while at the same time amplifying the filter output signal. This leads to a better interferer rejection, even with smaller ISR values. The preferred and optimal amplifier of the signal is a low noise amplifier (LNA) so that the useful signal will be

amplified, whereby the noise amplification is kept low. The LNA represents the first stage of the whole receiver circuit, while all other blocks belong to the adaptive filter and are not part of the major signal path.

Last, as seen in the stability simulation from chapter 4.3, the maximum phase shift of the error signal need to be within a +/- 90° angle over the whole frequency band of 1GHz to 3GHz. Since 0.13 μm CMOS technology does not have a transit frequency of several GHz, every circuit block will introduce a considerable phase shift. In comparison, the phase shift introduced by an arbitrary circuit at the 3dB corner frequency is already 45°. That means about every block in the circuit will contribute to the overall phase shift, whereby the +/- 90° requirement is limited to the feedback path. The elements in the feedback path are combiner, LNA, correlation multiplier, complex multiplier, and buffer amplifier. The hardware designs of these elements are optimized to contribute as little phase shift as possible, however first simulations have shown that the phase shift within the feedback path in the desired operating frequency band is more than 180°. In order to ensure proper operation, a phase equalizer circuit is required, which compensates for the phase response of all elements in order to comply to the phase shift requirement.

All these described modifications are applied on the block diagram shown in Fig. 5.1, which leads to the proposed block diagram shown in Fig. 5.2.

5.3 Description of Implemented Circuit Blocks

5.3.1 Combiner

The combiner is an integral part of the LMS algorithm and is the first block of the signal path of the useful signal. (Fig. 5.2). Because the combiner is in front of the LNA, it will add an insertion loss on the signal path, which will increase the noise figure by the

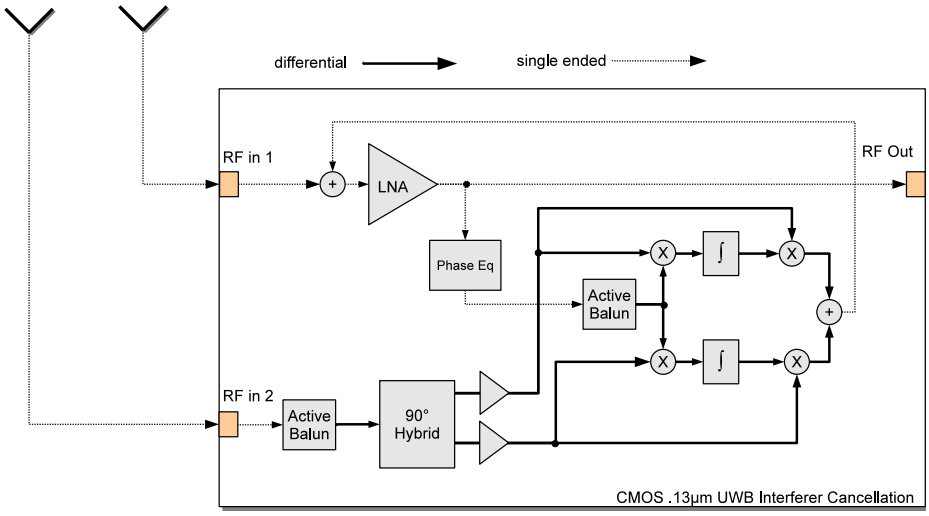


Figure 5.2: Proposed block diagram

same amount. However, the position of the combiner in the circuit, also determines at what point the interferer gets cancelled, which is implemented in the circuit before the first active stage. Otherwise, a strong interferer will drive the LNA into compression so that a useful signal can not be extracted anymore, even with any other type of interferer removal.

The combiner was realized with a resistive combiner circuit, because resistors provide a load for the interferer power with a high dynamic range. On the contrary, a conventional resistive combiner adds up to 6dB insertion loss and is the worst noise figure contribution that can be selected. However, the noise contribution of the resistive combiner can be optimized with an unequal resistive combiner as seen in Fig. 5.3.

As the term "unequal" implies, both input ports are not combined with the same factor. Hence, only a portion of the signal power of the port In_2 will be added to the input

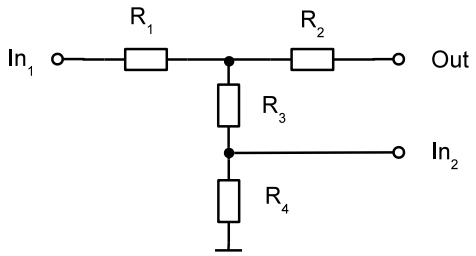


Figure 5.3: Resistive combiner

In_1, which represents the major signal path (r_1 of Fig. 3.5). This will lead to small values R_1 and R_2, which will lead to a low insertion loss and hence a good noise figure. The ratio of R_3 and R_4 determine the transfer characteristic of the second input In_2 to the output. A small added signal portion from In_2 also leads the lower total noise figure, which will be further discussed in Chapter 6.3. However, the absolute maximum interferer level that can be suppressed by the filter is also limited by the amount of attenuation of In_2.

This circuit shall have equivalent 50 Ω impedances on all three ports. If one value is changed, all other values need to adjust to stay within the 50Ω system. The values were chosen to be $R_1 = 15\Omega$, $R_2 = 15\Omega$, $R_3 = 37.5\Omega$ and $R_4 = 250\Omega$. The S-Parameter simulation result of the combiner can be seen in Fig. A.1. In exchange of lower input matching, the noise figure was further reduced by excluding the series resistors R_1 and R_2. As a result the insertion loss becomes about 3dB (See Fig. A.2).

A different topology of the signal combiner can be a wilkinson combiner, that has about 3dB insertion loss and a equal combination. With a wide-band wilkinson power splitter the range from 1GHz to 3 GHz can be attained, however its phase response will be about more than 180°, which makes this topology impractical.

Another method for signal combination is when LNA and combiner are merged together to a *Combiner LNA* [18]. In a Combiner LNA drain current summation is realized by a common load resistor of two different amplifiers. Nevertheless, simulations have shown that LNA performance requirements are difficult to accomplish with that topology, due to the larger bandwidth requirements. Furthermore, one drawback of this design is the fact that, after the adaptive filter has been converged, the dynamic range of the LNA is reduced by the power of the interferer level.

5.3.2 LNA

The LNA is the first active stage for the incoming signal wave. It is important that the signal will have a 50 Ω input resistance, which matches to the signal combiner from Chapter 5.3.1 and the antenna. The output stage of the LNA as well as all other stages of the entire integrated circuit can be high impedance. The distances among the blocks within the integrated circuit in relation to the wavelength are so small that wave propagation effects are negligible.

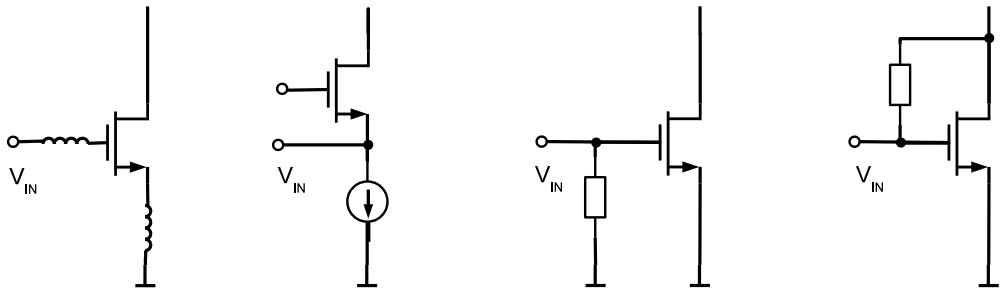


Figure 5.4: Common CMOS LNA Topologies [25]

A CMOS transistor does not necessarily have a 50 Ω input impedance without additional circuitry. Different LNA topologies have emerged for CMOS RF circuits which

attain the 50 Ω impedance by different methods. [25] provides an overview of CMOS LNA topologies, which can be seen in Fig. 5.5.

- The *Common Source LNA* uses an input matching network as well as a source inductor to achieve the low input impedance. It is also called source degenerative LNA. The number of coils needed for that topology are at least two.

- The *Common Gate LNA* uses the low impedance of the transistors source. It is also called $\frac{1}{g_m}$ LNA, because the low input impedance is achieved by the transconductance. From all topologies it has the lowest gain.

- The *Resistive Termination LNA* is a commons source amplifier with a parallel resistor connected to ground, which leads to the worst noise performance.

- The *Resistive Feedback LNA* is a common source amplifier with feedback resistor from output back to the gate. This circuit was implemented because it has a low number of coils, it has a high gain and a low noise figure. Most importantly, it has a flat gain and phase response which is required for the whole circuitry blocks that are part of the feedback path.

The resistive feedback LNA was designed according to [20] with the addition of a cascode stage and a *shunt-peaking* load. A simplified circuit can be seen in Fig. 5.5.

Shunt-peaking is a common method to increase the bandwidth of an active stage. A shunt-peaking loads usually consist of an inductor L_{SHUNT} with a series resistor R_{SHUNT}. A higher resistor value increases the gain, however it also decreases the bandwidth and it shifts the bias output level. The inductor L_{SHUNT} compensates the capacitive load of the amplifier, which leads to higher gain.

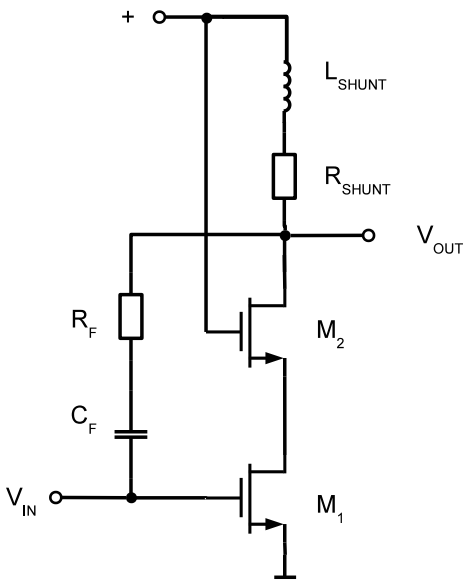


Figure 5.5: Feedback LNA schematic

A design formula for the input impedance is provided in [30]:

$$Z_{in} \cong \frac{R_F}{1 + A_V} \cong \frac{R_F}{A_V} \tag{5.2}$$

From [20] voltage gain A_V is calculated by equation (5.3)

$$A_V \cong -g_m(R_L \parallel R_F) \tag{5.3}$$

R_F represents the feedback resistor and R_L the amplifier's load impedance. Furthermore it is shown in [20] and [30] that a low noise figure can be achieved by a high feedback resistance R_F and high transconductance g_m.

The chosen feedback resistor R_F is 500 Ω, which results in an input impedance of 50 Ω if the voltage gain is 10dB. (5.2). S-Parameter Simulation results can be seen in Fig. A.3. The gain S_{21} lies between 8.6dB and 11.4 dB within the specified bandwidth (1GHz -

3GHz). The reflection coefficient (S_{11}) is lower than -10dB. A minimum noise figure (NF) of 2.7dB at 1GHz and 3.3dB at 3GHz was achieved.

A further simulation of the LNA in combination with the combiner from Chapter 5.3.1 is shown in Fig. A.4. It can be seen that the total noise figure increases with the amount of the combiner loss. The curve S_{32} represents the transfer function of the second combiner output to the output of the LNA, which is about 6dB less than the major signal path.

The circuit draws a current of 5.5 mA at a supply voltage of 1.2 V, which results in a power dissipation of 6.6mW.

5.3.3 Active Balun

As mentioned in Chapter 5.2, differential signaling has some major advantages. To generate a differential signal, an active balun was implemented. The requirements of the balun are good 180° phase accuracy over the operating bandwidth, low insertion loss and the same DC level output and gain on both paths.

In general, a differential signal can be simply generated by a conventional differential amplifier. Thereby, one input of the amplifier represents the single ended input, and the other input need to be connected to the mid-level DC voltage. Nevertheless, due to parasitic capacitances, a simple differential amplifier will not have a good performance at high frequencies anymore. For wide-band applications, a circuit proposed by [15], which is shown in Fig. 5.6 was implemented.

The capacitance C_F couples an additional part of the input power to transistor M_2 to compensate the lower gain of the second stage. The cross-coupling of the cascode stage M_3, M_4 ensures an equal gate-source voltage on both stages. Shunt-peaking coils as well as the current source for the two lower transistors as proposed in [15], were not necessary

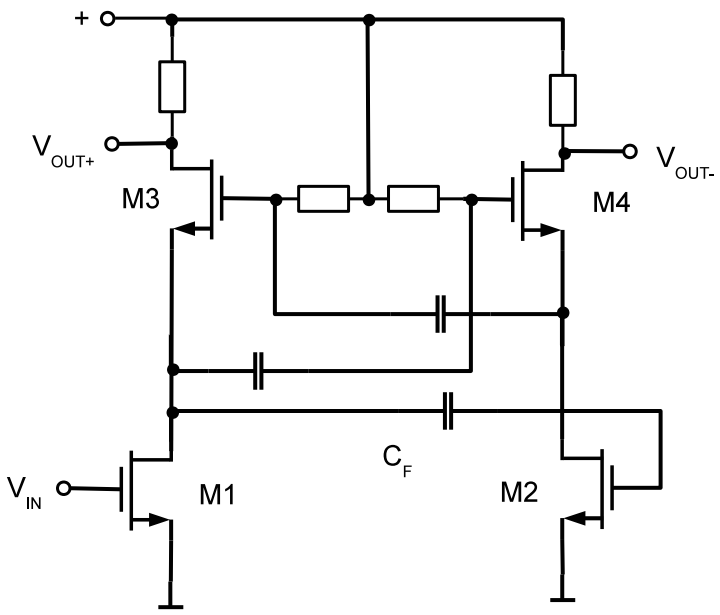


Figure 5.6: Balun with differential amplifier - simplified schematic

to comply to the requirements. The transfer function is illustrated in Fig. A.5 and its gain and phase accuracy in Fig. A.6 respective Fig. A.7. It can be seen that over the targeted bandwidth (1-3 GHz) the gain error is within 0.77dB and the phase error about 2.3°.

The circuit described by Fig. 5.6 is implemented twice. One implementation is used to generate a differential signal after the LNA. A further implementation is needed for the first active stage of the input path r_2. The second input path also needed low noise amplification and input matching, therefore the proposed balun, was adapted to become a balun LNA. Since the feedback input r_2 will contribute less to the overall noise figure, a simple resistive termination was implemented. Moreover, it is important that the feedback path has a larger signal dynamic range than the major signal path, because any compression within the feedback path would reduce the filter performance.

S-Parameter simulation results are shown in Fig. A.8. The active balun LNA has about 10dB gain, 10dB noise figure, and a wide band input match of about 12dB. Each circuit draws 11mA at a supply voltage of 1.2V, which results in a power dissipation of 14mW.

The RF input of the second path is AC coupled by a 1pF capacitor. Simulations of the circuit performance of this specific circuit, were performed with a capacitor from the analog library, instead of the IBM design library. Further simulations have shown that the capacitor model from the IBM design library shows considerably higher equivalent series resistor (ESR) value, which degrades the input matching of the feedback path. This degradation can be compensated for by an external matching circuit, with the disadvantage that the noise figure will rise. The matching circuit is presented in the test circuit chapter. The S-Parameter simulation of the balun LNA with additional external matching circuit can be seen in Fig. A.9.

5.3.4 90° Hybrid

The 90° hybrid was implemented by a lumped element passive circuit, also described as a polyphase filter. The implemented circuit is presented in, [10] and [13]. Both papers propose a schematic diagram as shown in Fig. 5.7. The proposed circuit requires a differential input signal to generate both 0° and 90° differential output signals. In order to achieve an operating bandwidth of 1GHz to 3GHz, three cascaded stages with individual RC time constant were required. The simulation results are shown in Fig. A.10. It can be seen that the phase error is lower than 2°, however the insertion loss is about 8dB. It is important that the path r_2 has a positive gain ($>$ 0dB), so that there is enough signal amplitude available to cancel the interferer completely.

Due to the high insertion loss, differential amplifiers for each path are connected directly after the filter. The schematic diagram is shown in Fig. E.7. The amplifiers are

fully differential at the input and output and use shunt-peaking by a resistor of 80 Ohm and an inductor of 11nH in both paths in order to achieve enough gain. Instead of two single coils, it would be possible to use one single differential coil; however differential coils have a lower Q-value which will lower the maximum attainable gain. The transfer function of the differential amplifier can be seen in Fig. A.11.

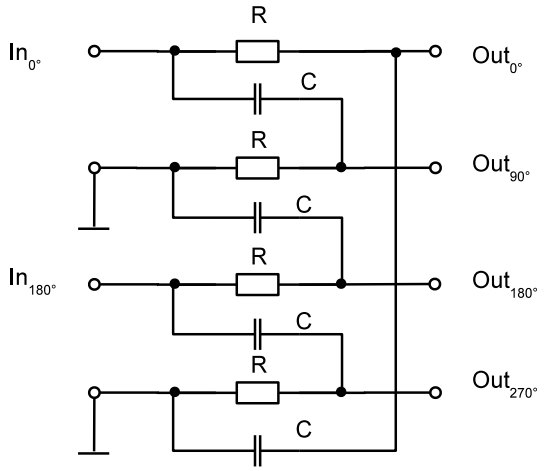


Figure 5.7: A 90° hybrid [10]

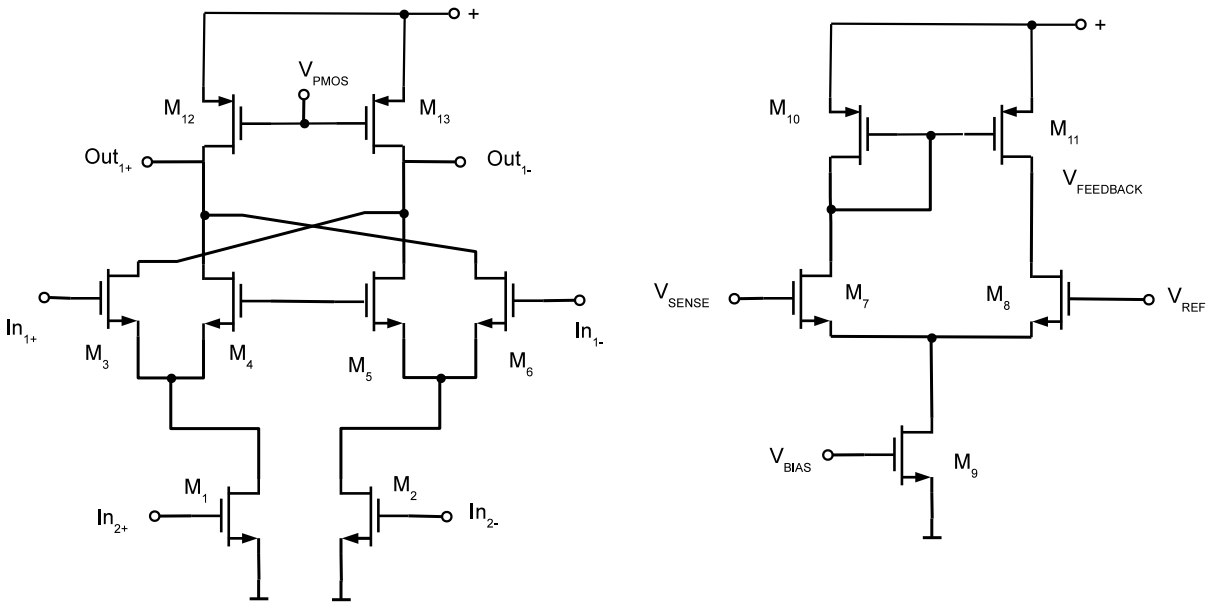
5.3.5 Correlation Multiplier

The two correlation multipliers perform $r_{2I} \cdot e + r_{2Q} \cdot e$. Both inputs of the multiplier are bandpass signals and have the same frequency, but a different phase delay. The multiplication of two signals with the same center frequency, will result in a baseband signal with a phase depended term. Any narrowband interferer will be downconverted to about zero IF.

The requirements of the correlation multiplier are first, that a high frequency wide-band input range is utilized on both signal inputs. Second, signal variations on both

signal paths need to contribute equally to the output signal. This is the major difference between a multiplier and a mixer. Whereas a shall maintains the output power regardless of its LO input power, the multiplier passes any signal level change on both inputs to the output. Third, the output bandwidth needs to be kept as low as possible, so that frequency intermodulation products and out-of-band products do not distort the outcome of the filter coefficient. Finally, because the multiplier is within the feedback path, its insertion loss needs to be low, while and gain and phase response shall be flat.

The correlation multiplier was designed from a gilbert cell with differential output. The corresponding schematic can be seen in Fig. 5.8.



(a) (b)

Figure 5.8: a) Fully diff. gilbert multiplier and b) CMFB circuit

The bias voltage V_{PMOS} of the active PMOS load must be within a very small range to maintain mid-level output. This effect comes from the mismatch of λ_p and λ_n of PMOS and NMOS devices. Therefore, a common mode feedback (CMFB) circuit was needed that automatically adjust the voltage V_{PMOS} [24]. In [21] a gilbert multiplier with CMFB and offset cancellation network is presented. The CMFB circuit is shown at the right side in Fig. 5.8. The circuit is a one-stage differential amplifier. The gate voltage of M7 represents the sense input voltage. The voltage V_{Sense} is determined by a center tapped high ohmic resistive load on each side of the differential pair of the mixer circuit. The feedback signal $V_{feedback}$ represents the bias of the active load.

The active load has 90μm width and minimum length. Additionally, all transistors of the CMFB circuit are designed with 90μm in width and minimum length. The performance is characterized by periodic-steady state simulations [7]. The output level is further described as IF, the upper input as RF,2 and the lower input as RF1. Every simulation is performed for each input, whereby the other input is kept at a constant power level of -15dBm.

The compression point and third order intercept point simulation result for input RF1 and input RF2 can be seen in Fig. A.12 and Fig. A.13. The RF bandwidth of both inputs is seen in Fig. A.14.

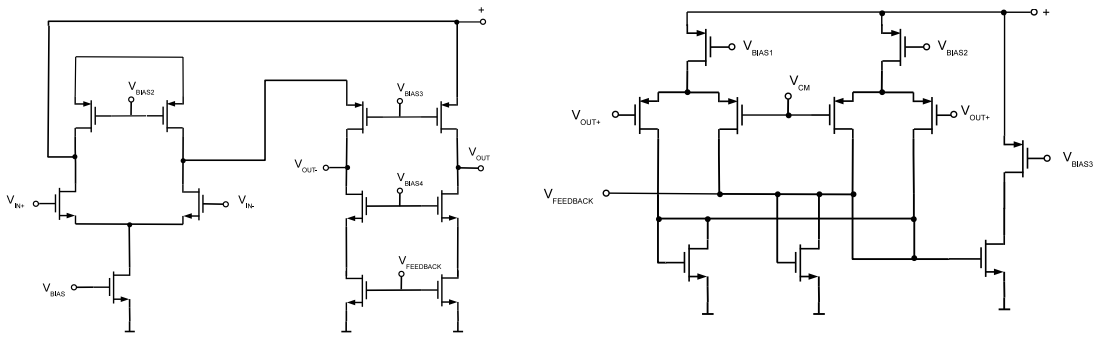
The final simulation of the IF bandwidth is presented in Fig. A.15

5.3.6 Integrator

Each output of both correlation multipliers is directly applied to the inputs of the integrator. The integrator time constant is a continuous time representation of the step size parameter μ from equation (3.18). A CMOS integrator can be designed with a transconductance amplifier. Transconductance amplifiers are basically voltage input -

current output amplifiers that can be realized by a high gain amplifier with the addition of a high output impedance circuit. The current output of the amplifier is then fed to a integrator capacitor. The integrator time constant is determined by $\tau_{Integrator} = \frac{C}{g_m}$.

The major requirement of this block is to attain as much gain as possible, so the required capacitance value is minimized. A small capacitance value allows the hardware integration of the capacitor on chip. A fully differential amplifier with folded cascode was designed according to [14]. A simplified schematic diagram of the circuit can be seen in Fig. 5.9.



(a) (b)

Figure 5.9: a) Integrator and b) CMFB circuit

This circuit is also fully differential and therefore requires a CMFB circuit. However, in order to reach a high gain, the CMFB circuit that is used in the circuit of the correlation multiplier is not suitable. A different CMFB circuit described by [14] shows good simulation results.

There are two options to connect the integrator capacitors. Either one single capacitor is connected between both differential outputs, or two capacitors are connected to each path of the differential signal output. Simulations have shown that the CMFB becomes unstable, if the capacitance is connected between both paths. Therefore four individual

dual MIM capacitors were integrated in the design. The MIM capacitor value was chosen to be 20pF.

All integrator output circuit nodes are connected to the external pins, so it is possible to externally connect additional capacitors and increase the overall capacitance value. Furthermore, those output pins are also used for testing. Real and imaginary parts of the filter coefficient can be monitored. A digital switch is able to turn the entire integrator stage from active to high impedance. This allows for external configuration of those coefficient voltages to an arbitrarily value.

The simulated transfer function of the integrator can be seen in Fig. A.16. A gain of 54dB was achieved. In this simulation the integrated circuit without additional capacitance is shown. The integrator is operating properly within the range of about 2MHz to 200MHz. The lower frequency corner is determined by the integrator capacitor value. For example with a total 400pF capacitance, the integrator range can be extended resulting in a span of 5kHz to 200MHz. (Fig. A.17)

5.3.7 Complex Multiplier

The complex multiplier performs $r_2\ c$, whereby the filter coefficient c is a slowly varying signal and r_2 is a high frequency bandpass pass signal, as well as the output signal. Thus, the complex multiplier can also be considered a variable gain-phase amplifier (VGA) as drawn in Fig. 5.1.

The complex multiplier is also part of the feedback loop, which requires a positive ($>$ 0dB) and flat gain and a flat phase response. The multiplier is implemented by two correlation multipliers from Chapter 5.3.5 with the same CMFB circuit as in Chapter 5.3.5. A simplified schematic is shown in Fig. 5.10. Shunt-peaking was not necessary to achieve good performance.

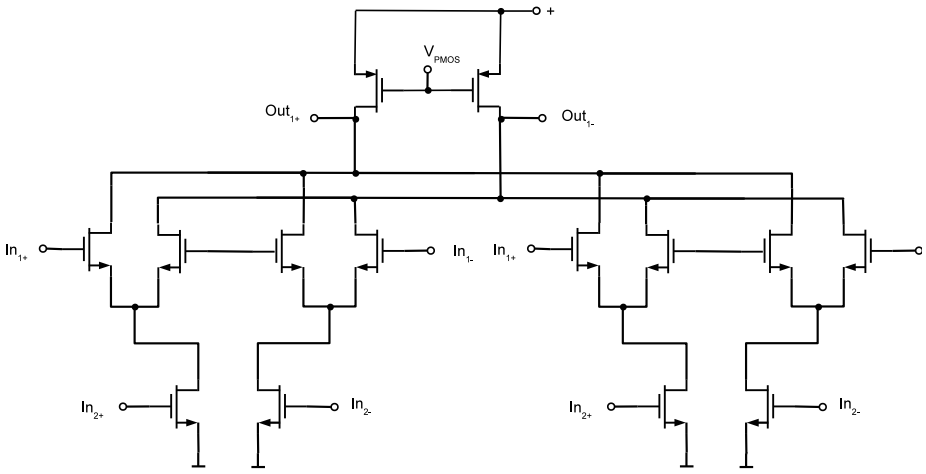


Figure 5.10: Complex Multiplier - simplified circuit

The major difference to the circuit illustrated in Fig. 5.3.5 is that AC coupling can be used only for high frequency multiplier inputs. The lower transistor differential input is DC coupled, which means that the input signal also carries the bias voltage. The bias voltage is determined through previous stage, which is the integrator, whereby its CMFB circuit gives the degree of freedom to choose the output level.

In a simulation the transfer function is determined with respect to the low frequency input signal that is represented by different DC values. The simulation result can be seen in Fig. A.18. The output of the complex multiplier is still a differential signal, whereby a single-ended signal for the signal combiner (5.3.1) is required. Therefore, a high frequency differential to single-ended conversion circuit is necessary. This circuit is implemented by a differential amplifier with a cascode stage and a PMOS current mirror to combine both signal paths. In order to avoid additional phase shifts, DC input coupling is used as well. The transfer function of the differential to single ended amplifier can be seen in Fig. A.19.

5.3.8 Phase Equalizer

The phase equalizer needs to compensate for frequency dependent phase shift in the feedback path. System simulations made apparent the need for a phase equalizer circuit to ensure proper operation within the entire bandwidth from 1 to 3 GHz. The reason for that circuit comes from the fact that analog control loops in a frequency range from 1 to 3 GHz in 0.13 μm CMOS approaches its performance boundaries.

The phase equalizer needs to have a phase response that introduces less phase shift for higher frequencies.

A special characteristic of this kind that, was realized by a circuit shown in Fig. 5.11.

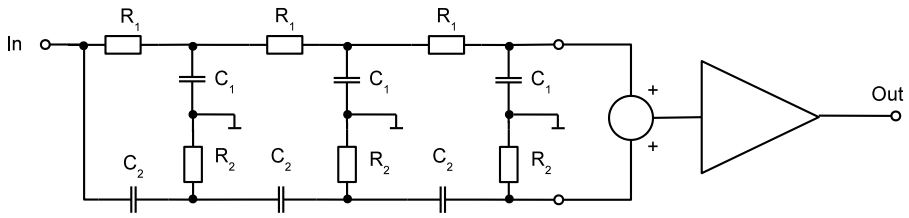
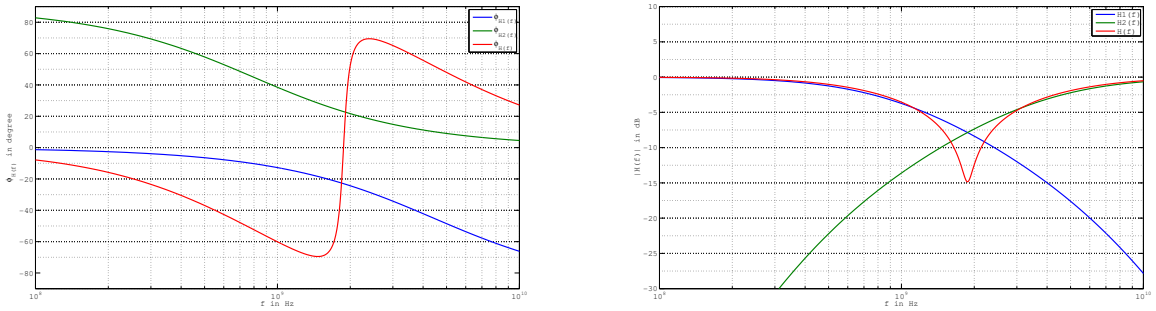


Figure 5.11: Phase Equalizer - simplified schematic

The circuit consists of a RC low-pass and a high-pass filter with transfer functions $H_1(f)$ and $H_2(f)$. The corner frequencies of each filter are close to each other, but different. By adding both signal paths together, the resulting transfer function can be calculated by $H_(f) = H_1(f) + H_2(f)$. With an appropriate selection of both corner frequencies the desired characteristic phase response can be achieved. For the selection of both corner frequencies, a model in MatLAB was implemented and the output transfer function was numerically determined. A MatLAB simulation result with the parameters $R_1 = 180\Omega$, $C_1 = 200fF$, $R_2 = 1k\Omega$ and $C_2 = C_1$ can be seen in Fig. 5.12.



(a) (b)

Figure 5.12: a) Phase Response b) Magnitude Response

It can be seen that for the chosen corner frequencies and a three stage R-C filter, the phase response at 1GHz is about -60° and at 3 GHz + 65°, which add up to a total phase shift within the operating frequency band of 125°. The disadvantage of this circuit can be seen in the magnitude response shown in Fig. 5.12. The circuit introduces a 15dB attenuation at the center frequency of the operating frequency band. This is where the transfer characteristics of low-pass and high-pass filter intersect and form a notch filter. It is possible to reduce the notch filter effect by an additional amplifier or by setting the high-pass corner frequency lower and the low pass corner frequency higher; however in both cases this will reduce the established min-max phase shift.

In order to add both paths together a combiner amplifier is needed. It is implemented by two common source stages with cascode stage and a common drain shunt-peaking circuit to add both paths. The value of the coil was chosen to get the maximum gain at the frequency of the unwanted notch from the equalizer. The combiner amplifier itself will introduce another transfer function with a non-flat phase response. This need to be taken into consideration when selecting the corner frequencies of the phase equalizer. The simulation of the implemented hardware can be seen in Fig. A.20.

5.3.9 Bias Circuitry

All circuits were designed to operate with the voltages 400mV, 600mV and 800mV. A wide-swing constant transconductance bias circuit according to [14] with resistive external bias adjustment was implemented to deliver these voltages. A simplified circuit is shown in Fig. 5.13. It consists of one NMOS and one PMOS wide swing current source with the addition of an NMOS and PMOS cascode bias voltage generation. This circuit is used twice in the design. One circuit was implemented for the generation of an resistor adjustable 600mV bias voltage and the second circuit generates a resistor adjustable 400mV and 800mV supply voltage. All voltages were connected to external pins. If no resistor is connected to ground, the bias circuit is turned off and all voltages can be supplied externally.

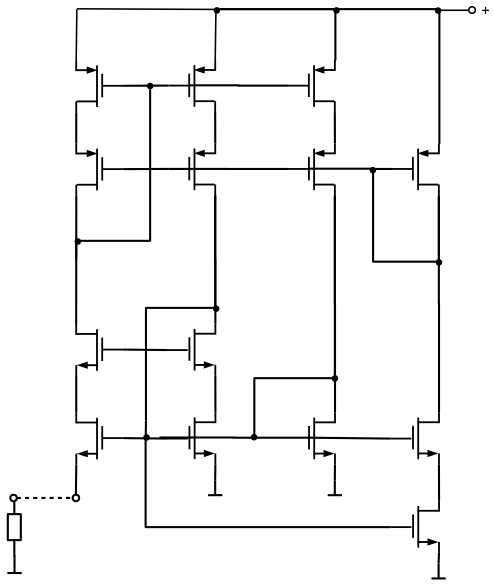


Figure 5.13: Bias Circuit according to [14]

According to the simulation, the proposed external resistor value is 750 Ω for both bias circuits. The dependency on the external resistor can be seen in Fig. A.22.

In order to avoid feedback paths through the voltage distribution network, many of the left open spaces in the circuit layout were filled with voltage-blocking capacitors.

5.3.10 Output stage

The output stage converts the signal from the high impedance system within the entire circuit back to the 50 Ω impedance system. This is realized by a source follower circuit, so that its combination of source resistance and $\frac{1}{g_m}$ equals 50Ω. This circuit is used three times within the entire integrated circuit (IC).

The signal combiner that determines the error of the LMS algorithm from Chapter 5.3.1 needs 50 Ω inputs and outputs. That requires a 50Ω output impedance of the complex multiplier, which is realized by the proposed buffer amplifier. The two other output stages are for the package pin RF output and wafer prober RF test output.

Those output stages do not contain a source resistor or an DC output coupling. By externally connecting a resistor to DC at one of both RF outputs, the corresponding output stage will be enabled. This allows for choosing between both output stages without the need for both stages to be powered on. Simulations on AC and DC coupled configurations can be seen in Fig. A.21.

5.3.11 Digital Circuits

For testing purposes it is useful to be able to turn complete circuit blocks on and off and is able to tune some circuit parts. A digital shift register was implemented, because CMOS technology is state-of-the-art technology for digital circuits. The advantage of an N-bit shift register is that the number of implemented states in the circuit is determined

by 2^N, and not limited by the number of external pins because a shift register can be loaded by a particular bit pattern from a serial interface. In this design, an 8-bit shift register was implemented by an external SPI interface. A simplified block diagram is shown in Fig. 5.14.

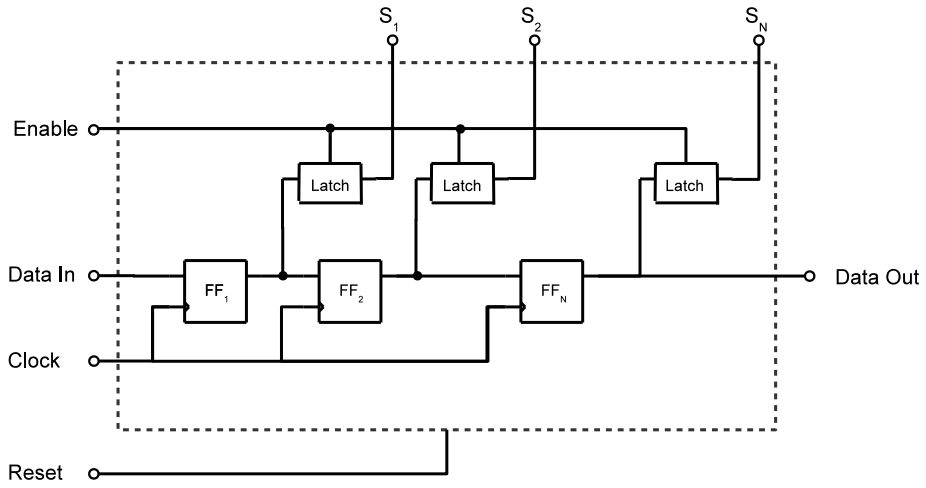


Figure 5.14: Shift register - simplified block diagram

The binary value of each *D-Flip-Flops* will be updated every rising clock edge. The output of the D-Flip-flops are connected to latches which become transparent only after an *Enable* signal. The output of the latch will drive the switching transistors within the circuit. This method ensures that no switch will toggle, during the loading of the data.

In some cases, especially, if a complete block is turned off, two transistor stages need to switch consecutively. This is realized by a digital delay circuit that is also used for the generation of non-overlapping clocks. The circuit diagram is shown in Fig. E.25. The time switching delay is determined by the capacitance value of the load capacitors.

The time domain simulation of the shift register can be seen in Fig. E.20. The input

data was chosen to be a triangle shaped signal, which is testing the behavior of the digital circuit on slow input signal slopes. Underneath the data, the clock and the reset is shown. Reset is active till t=900ns. The data outputs of flip-flops 1 to 3 are shown in this simulation. It can be seen that the bit will pass through the shift register which proves its proper operation.

Chapter 6

Hardware System Simulation

The complete block diagram is shown in appendix E.1 and the corresponding layout can be seen in F.1. Time and frequency domain as well as noise analysis were performed to convert system requirements to circuit block requirements and to verify the system performance on the hardware level.

6.1 Frequency Domain

As known from the MatLAB simulation, phase shifts in the feedback path of the filter need to be within +/- 90 ° to ensure proper operation. Therefore, the open loop transfer function of the entire circuit with all sub-circuits, was determined. Thus, the feedback path of the adaptive filter loop was opened as seen in Fig. 6.1. The DC voltages set the filter coefficient to a fixed value. In general this value can be chosen to a arbitrary value different from zero. The goal of the simulation is to determine the frequency dependent phase shift of the realized circuit. The value of the coefficient will introduce an offset in the phase transfer characteristic.

An AC simulation was performed that will determine the transfer characteristic of the

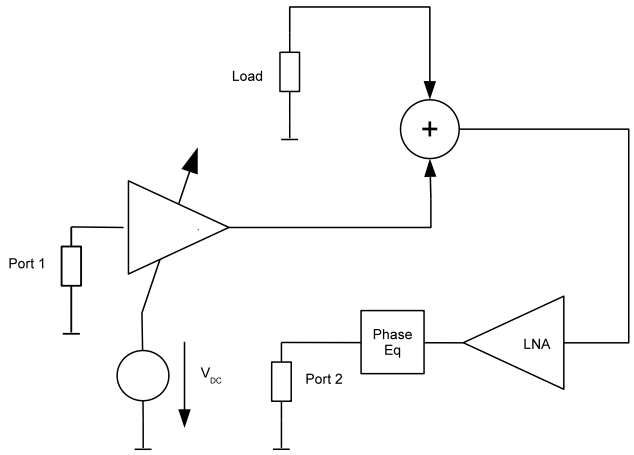


Figure 6.1: Frequency Domain Simulation - Block Diagram

filter from *Port 1* to *Port 2*. The DC voltages were set to the characteristic values after the filter has converged for a 2 GHz interferer.

The simulation result can be seen in Fig. 6.2. The gain at 1 GHz and 3 GHz is about 10dB, while the gain at 2GHz is about zero. In the phase response the effect of the phase equalizer can be seen. Between 1GHz and 3GHz the phase shift is between 300° and 380°.

As mentioned in the MatLAB simulation, at a phase shift of exact +/- 90 °, the feedback loop will start to oscillate. As seen in the simulation, the circuit shows a positive gain at 850MHz, where the phase shift is equal to -270°. This is a major difference to the conventional method of determining the stability of a circuit by phase and gain margin in LTI systems because it does not mean that the circuit itself is unstable and will oscillate at 850 MHz. It rather means that present interferers at 850 MHz, can induce a oscillation of the feedback loop, and the interferer can not get cancelled anymore; however the frequency 850MHz is outside of the operating frequency range.

Furthermore at interferer frequencies between 400 MHz and 850MHz, the positive

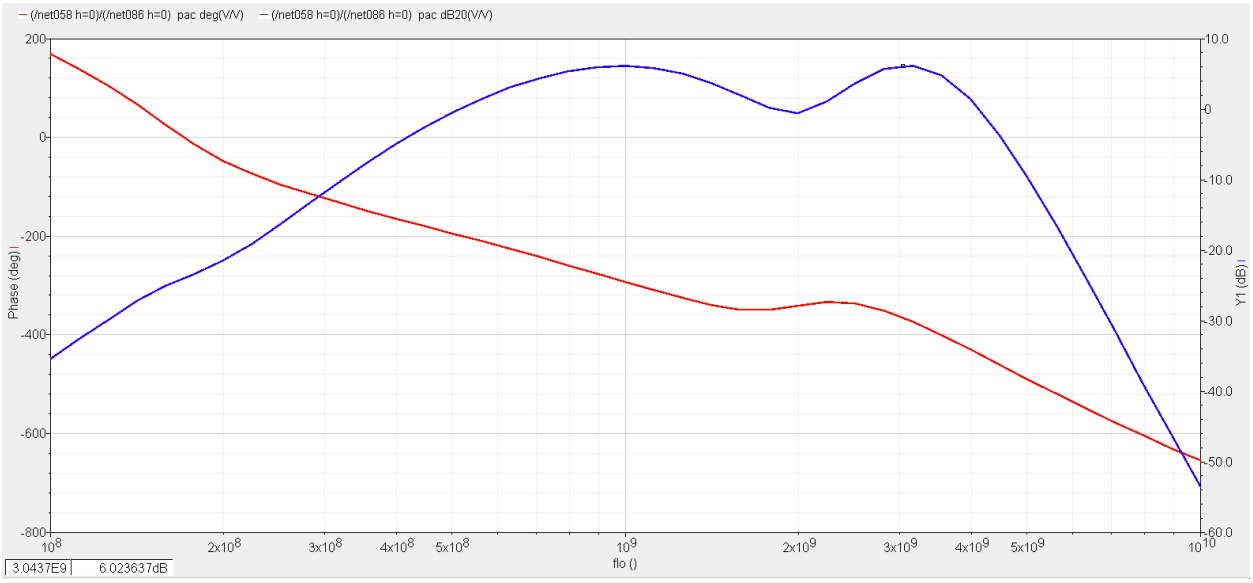


Figure 6.2: System Transfer Function

gain (> 0) of the circuit will lead to an increase of the interferer amplitude. If in this case the control loop direction would be inverted, e. g. by simply exchanging positive and negative connections of a differential path, the interferer amplitude will be suppressed, and the operating frequency range can be extended.

Because 400MHz to 850MHz is outside the specified useful signal bandwidth, additional conventional filtering can separate those interferers from the useful signal. For example, additional LNAs which are connected directly after the antenna can diminish this effect, if their transfer characteristic will not pass signals in this frequency range. However, additional filtering within the control loop is not recommended, since those blocks will introduce additional phase shifts which will result in improper operation. The stability of the system is further proven by time domain simulations.

6.2 Time Domain

A time domain simulation was performed with a 2 GHz interferer at a power level of -20dBm. The UWB pulse amplitude was set to 120mV, with a 800ns pulse width of and a pulse repetition time of 12ns. With the digital circuit an impulse was sent to turn the algorithm on and off, to see how the filter will respond. The result of the conventional time domain simulation can be seen in Fig. 6.3. The filter algorthim was turned off at 80ns and turned back on again at 500ns. The convergence time was in this case about 100ns. The signal C1, C2 illustrate the differential signal pair of the real part and C3, C4 illustrates the differential signal pair of the imaginary part of the filter coefficient. This simulation was performed with QRC extracted parasitic capacitances of the final layout.

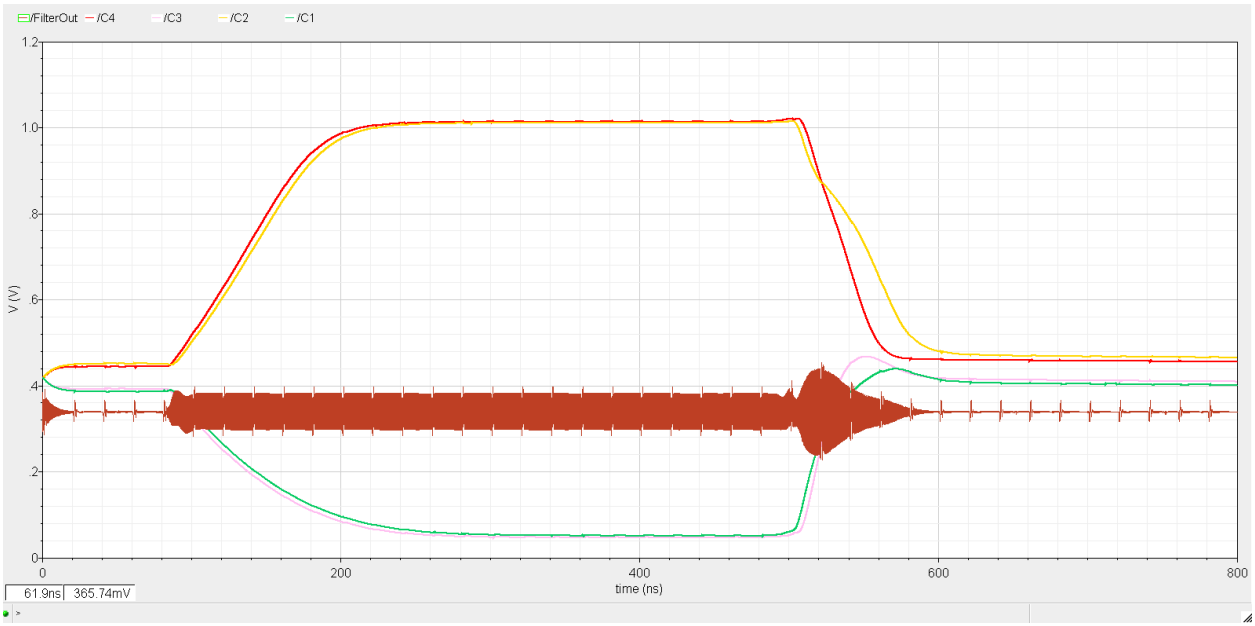


Figure 6.3: System Time Domain Simulation

In a further simulation the interferer suppression level was determined. This simulation result is illustrated in Fig. 6.4, which shows that the interferer amplitude was reduced from 220 mV to 7 mV. This is equal to an interferer suppression of about 30dB.

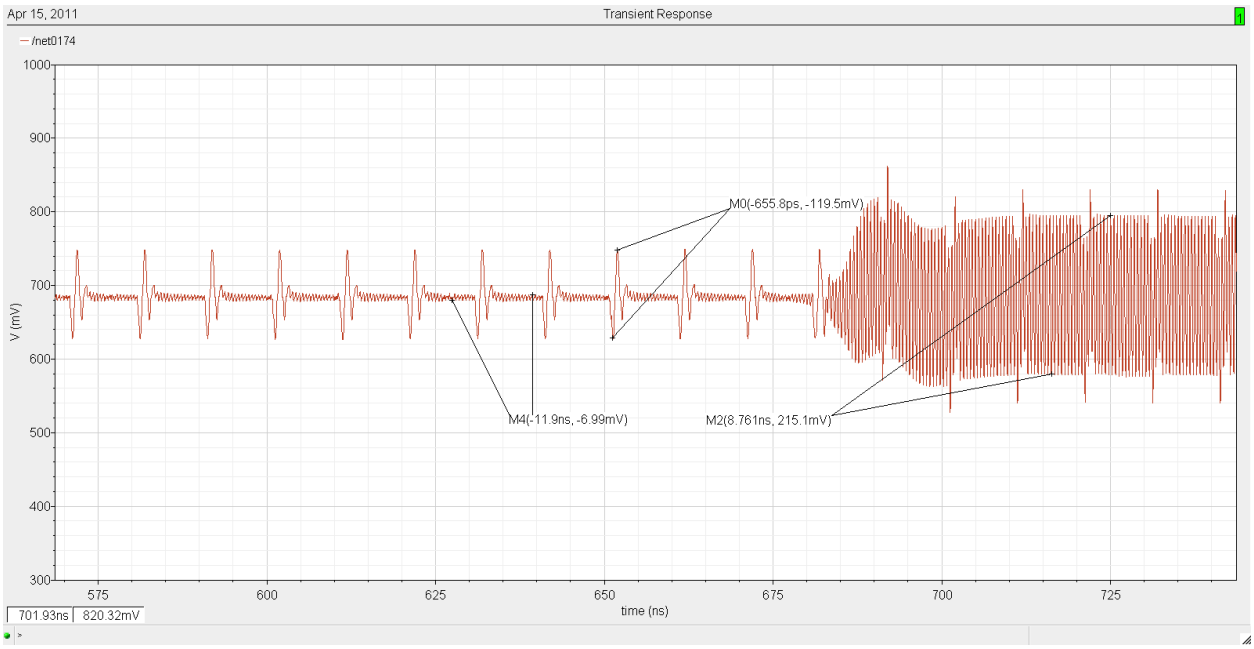


Figure 6.4: System Time Domain Simulation - Suppression Level

For further analysis, this time domain simulation was performed versus its interferer level power and interferer frequency. As simulated in MatLAB, the convergence time depends on the deviation of the system phase shift from 180° and if the phase shift approaches 90° an oscillation will occur. All time domain simulations were performed in the frequency range of 1GHz to 3GHz in Fig. B.1 - Fig. B.6.

A major difference between MatLAB simulation and SpectreRF system simulation could be observed. The signal combiner is AC coupled, and the capacitances are not large enough so that the sub-nanosecond UWB pulse from the path r_2 will pass. That means that with this implementation the useful signal can theoretically arrive from any arbitrary angle without any signal cancellation because the signal combiner will not let the UWB signal pass for constructive and destructive combining.

6.3 Noise Figure

As discussed, in the description of the combiner, the purpose of setting the signal combiner before the LNA is to avoid the strong interferers that will lead to LNA compression and a loss of the useful signal. However, the disadvantage of this method is the higher system noise. The total noise figure will be determined sequentially.

If there is no present interferer, the filter algorithm can be turned off completely, so the feedback path will not contribute to the total noise figure. Hence, the noise is determined only by the signal path r_1, which results in a noise figure as simulated in the LNA with combiner simulation. The noise figure when no interferer is present becomes 5.5dB at 1GHz to 6.9dB at 3GHz, which results in 6.2dB average noise figure.

In order to determine the total noise for present interferers a theoretical consideration on total noise figure has to be done first. The situation of the noise addition is shown in Fig. 6.5.

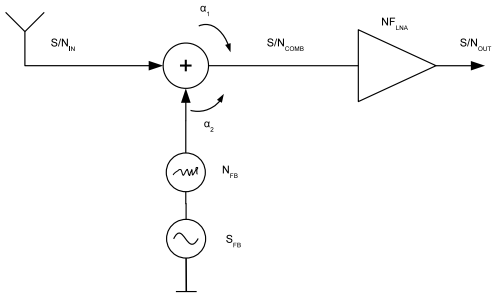


Figure 6.5: Noise Contribution of the feedback input

$$NF_{TOTAL} = \frac{(S/N)_{IN}}{(S/N)_{OUT}} \tag{6.1}$$

$$NF_{LNA} = \frac{(S/N)_{COMB}}{(S/N)_{OUT}} \tag{6.2}$$

Combining and leads to:

$$NF_{TOTAL} = \frac{(S/N)_{IN}}{(S/N)_{COMB}} \, NF_{LNA} \tag{6.3}$$

The Signal and Noise Power of the output of the combiner are

$$S_{COMB} = S_{IN} \, \alpha_1 + S_{FB} \, \alpha_2 \qquad N_{COMB} = N_{IN} + N_{FB} \, \alpha_2 \tag{6.4}$$

Whereby $\alpha_1 = [0...1]$ and $\alpha_2 = [0...1]$ represents the gain of each path at the signal combiner. The signal power of the feedback signal S_{FB} after convergence is dependent on the relation of the phases of interferer to useful signal. Equal power input on both antenna is assumed. The best case condition for the total noise figure is when both signals combine equally and the feedback signal has a signal power of the input signal multiplied by the attenuator values. The angle dependency will be further expressed by $\beta = [0...1]$. It can be expressed as:

$$S_{FB} = \frac{S_{IN}}{\alpha_2} \, \alpha_1 \, \beta \tag{6.5}$$

$$(S/N)_{COMB} = \frac{S_{IN} \, \alpha_1 \, (1 + \beta)}{N_{IN} + N_{FB} \, \alpha_2} \tag{6.6}$$

Setting (6.6) in (6.3) with simple calculus leads to a total noise figure of:

$$NF_{TOTAL} = NF_{LNA} \, \frac{N_{FB} \, \alpha_2 + N_{IN}}{\alpha_1 N_{IN} \, (1 + \beta)} \approx \frac{NF_{LNA} \, N_{FB} \, \alpha_2}{\alpha_1 N_{IN} \, (1 + \beta)} \tag{6.7}$$

For $\beta = 1$:

$$[NF_{TOTAL}]_{dB} = [NF_{LNA}]_{dB} + [N_{FB} - N_{IN}]_{dB} + [\alpha_2 - \alpha_1]_{dB} - \ 3dB \tag{6.8}$$

The absolute noise value N_FB present at the signal combiner from path r_2 is determined in a noise simulation. The simulation result can be seen in 6.6.

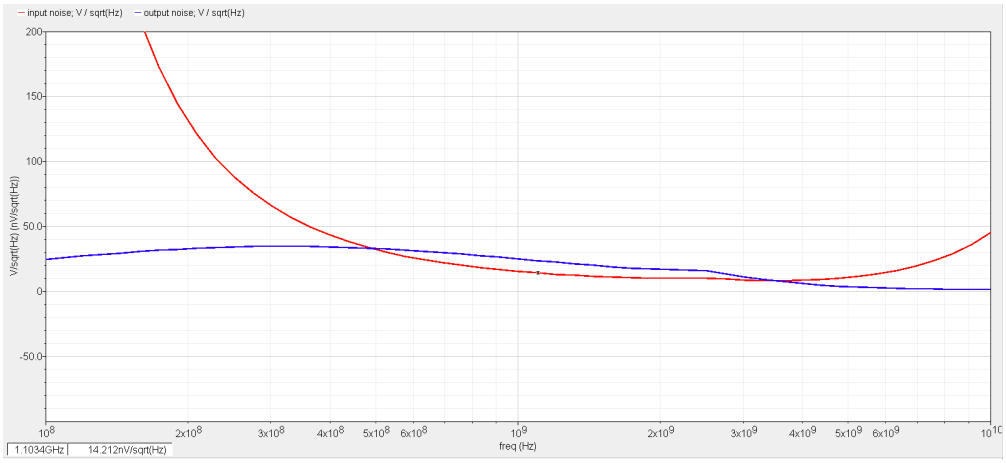


Figure 6.6: Absolute noise value at the combiner input of path r_2

It can be seen that the noise N_{FB} equals to about $\frac{25nV}{\sqrt{Hz}}$ to $\frac{12nV}{\sqrt{Hz}}$, which can also be expressed as $\frac{-145dBm}{Hz}$ to $\frac{-151dBm}{Hz}$. The noise of the N_{IN} is considered to be the thermal noise floor at room temperature that equals to $\frac{-174dBm}{Hz}$.

Using equation (6.8) the total noise figure can now be calculated by using the following values: $[\alpha_2]_{dB} = -8dB$, $[\alpha_1]_{dB} = -3dB$, $[NF_{LNA}]_{dB} = 3.0dB$. This leads to a total noise figure of $NF_{TOTAL} = 23.9dB$ at 3GHz and $NF_{TOTAL} = 17.6dB$ at 1GHz with an average of 21dB. This is the best case for coherent useful signal combining.

The overall noise figure is considerably higher than a usual noise figure optimized receiver. Furthermore, an even higher noise figure needs to be expected when signal demodulation is performed. One way to dramatically improve the noise figure is the use

of LNAs in both paths directly after the antenna. Those LNAs would need to have large dynamic range, so that interferer does not drive the LNA into saturation. Therefore these LNAs might not necessarily be implemented in CMOS RF technology. The implemented LMS adaptive filter is optimized, so that it will operate properly if the input signal power in both paths is about the same. This allows for adding amplifiers in front of both RF inputs with about same gain. A different gain between the feedback path and the major path can result in an improper operation.

Chapter 7

Circuit Test Description

Due to long delivery times of MOSIS and the requirement to merge two different designs on one single chip, this research project does not include the test of the fabricated design. A proposed test description however is provided. There are two methods to test the circuit. The packaged chip can be tested on a test printed circuit board or the unpackaged chip itself is tested on wafer by a wafer prober. It is recommended to perform the circuit functional and performance test on the test board.

A drawing of the implemented die, can be seen in Fig. 7.1. The overall die size is 4x4 mm^2, whereby the implemented LMS algorithm utilizes a size of 1.3 x 0.8 mm^2. The correspondence of the I/O Pads with their functionality is listed in Tab. 7.2. With the exception of Pads 33, 34 and 35, all pads are necessary for a bond connection to the chip package. Pad 33 - 35 are for optional use for wafer prober testing.

7.1 Bondpad Connections

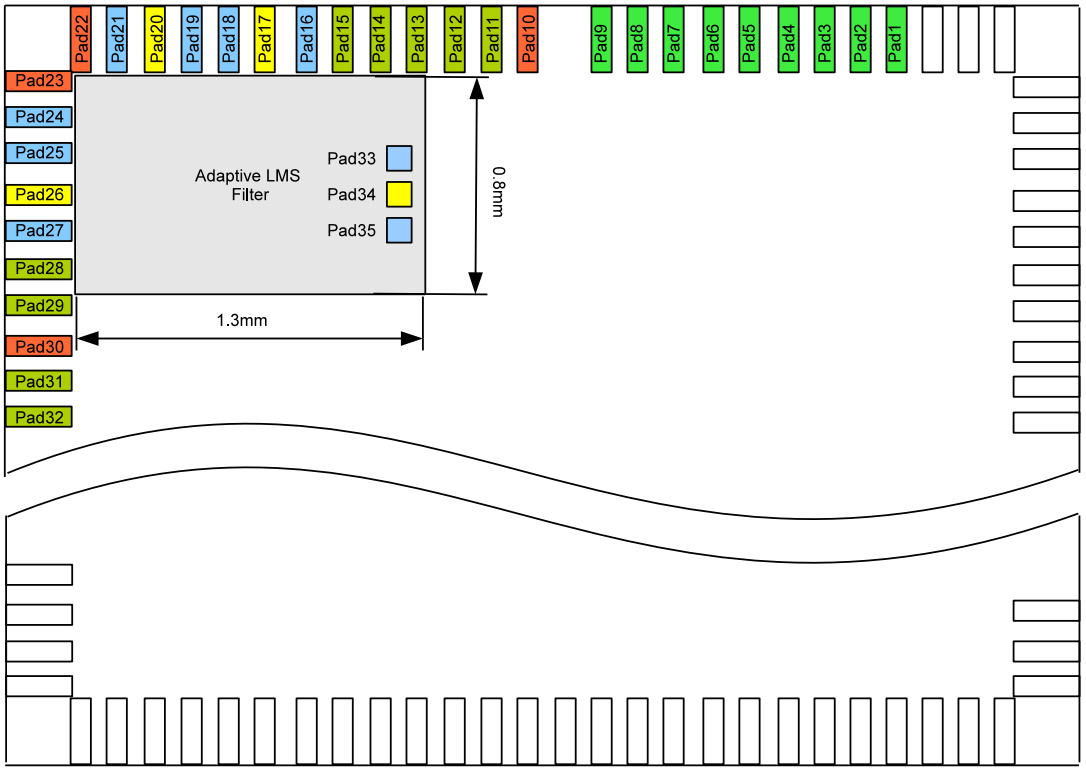


Figure 7.1: Pad Connections - Layout

Pad 1	Digital GND	Pad 10	Analog VDD	Pad 19	GND	Pad 28	C1/ WI_p
Pad 2	Digital VDD	Pad 11	Res4-8	Pad 20	RF IN 1	Pad 29	C2 / WI_n
Pad 3	Digital GND	Pad 12	V800	Pad 21	GND	Pad 30	Analog VDD
Pad 4	Digital VDD	Pad 13	V600	Pad 22	Analog VDD	Pad 31	C3/ WQ_p
Pad 5	DataOut	Pad 14	V400	Pad 23	Analog VDD	Pad 32	C4/ WQ_n
Pad 6	Enable	Pad 15	Res6	Pad 24	GND	Pad 33	GND
Pad 7	DataIN	Pad 16	GND	Pad 25	GND	Pad 34	RF OUT
Pad 8	Clk	Pad 17	RF OUT	Pad26	RF IN 2	Pad 35	GND
Pad 9	Reset	Pad 18	GND	Pad 27	GND		

Table 7.1: Pad Connections

7.2 Test Board

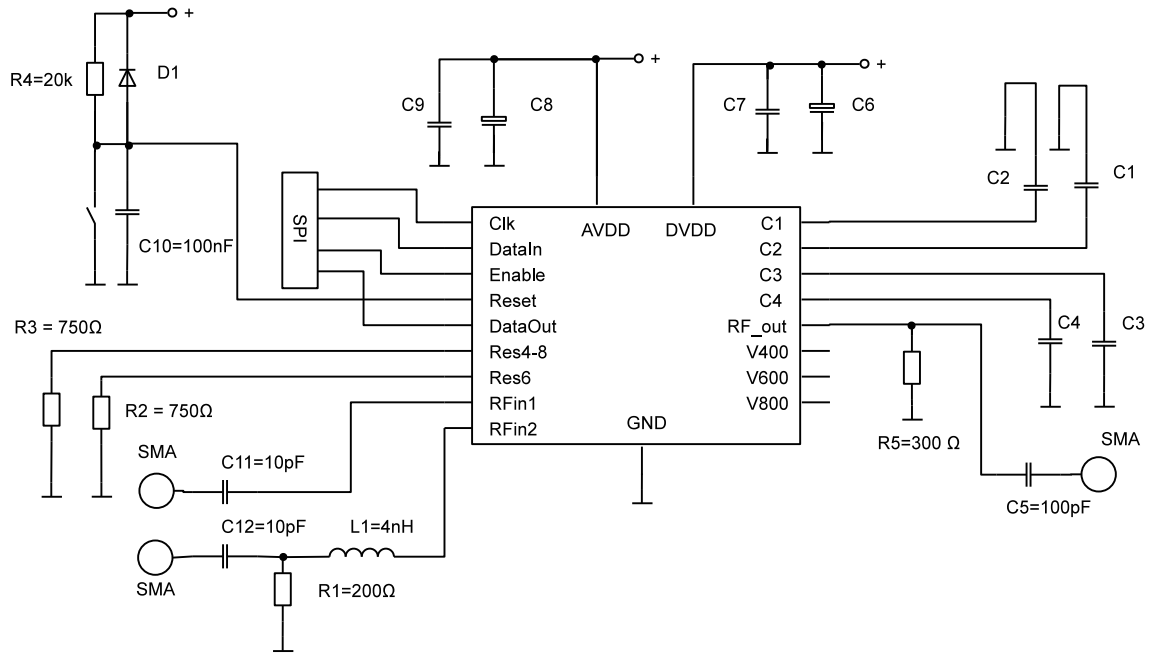


Figure 7.2: Proposed Test Board Schematic

Bit	Initial State	Function	Remark
0	1	Feedback Path On/OFF	Complex multiplier is active with 1 and passive with 0
1	1	Weights On/OFF	Integrator is active with 1 and passive with 0
2	0	–	unused
3	0	$C1_{on}$	Phase Equalizer transfer function tuning
4	0	$C2_{on}$	Phase Equalizer transfer function tuning
5	1	$C3_{on}$	Phase Equalizer transfer function tuning
6	0	$R1_{on}$	Phase Equalizer transfer function tuning
7	0	$R2_{on}$	Phase Equalizer transfer function tuning

Table 7.2: Functional Modes

The circuit is powered with 1.2 V. All power connections shall have at least one block capacitor to ground, which are connected as close as possible to the circuit package.

The circuit can also be seen in Fig. 7.2. As mentioned earlier, the design is able to switch its internal states by changing the pattern of the 8 Bit shift register. The register can be serially loaded by the SPI interface. The functionality of the shift register is shown in Tab. 7.2. Bit 0 stand for the LSB and 7 for the MSB, whereby the register is loaded with MSB first. The reset circuit will introduce a power on reset. The switch allows for the performance of additional resets after powering on. If the reset is active, all digital circuit I/Os will also be turned off completely.

The two RF inputs and the RF output are connected to the test board through SMA connectors. As mentioned in Chapter 5.3.3, the second input needs an additional matching network for good input matching. The corresponding circuit for the input RF2 consists of R1, L1 and C12 according to Fig. 7.2.

The output RF port requires the an resistor (R5) to ground to enable the output stage.

The bias voltages can be adjusted with the resistors R2 and R3. The resulting internal voltage can be tested at the connections V400, V600 and V800 which stands for 400mV, 600mV and 800mV. If the voltages cannot be adjusted to the appropriate values, R2 and R3 can be left open, and the appropriate voltage can be externally applied directly on V400, V600 and V800.

At the connection of C1 to C4 the filter coefficients can be measured. With the capacitances C1 to C4 the integrator bandwidth can be extended. Through the SPI interface the integrator can be turned off, and the filter coefficient voltages can be applied from externally as well.

7.3 Wafer Prober Test

For a wafer prober test, three GSG probes with 150μm are required. All RF Ports are placed so that there is only one probe at one side of the circuit. The digital circuit can be turned off completely by connecting the reset pin to ground, which will deactivate all digital I/Os. One issue with this test is that the RF-output Pad33 - Pad35 will only become active if there is a DC-connection to ground. Usually spectrum analyzers are AC coupled at the input. An RC element as used in test board (Fig. 7.2) will solve this issue. The wafer prober test method gives less testing functionality, however for debugging purpuses this testing method can become helpful.

Chapter 8

Conclusion

A UWB receiver that adaptively cancels single narrow-band interferers is proposed. The adaptive filter is based on a diversity receiver with minimum mean square error (MMSE) combining, whereby MMSE is approached by the LMS algorithm. An analog continuous time filter circuit is implemented in 0.13m CMOS RF and will be fabricated by IBM. SpectreRF simulation results show an interferer suppression of more than 30 dB, within the frequency range of 1GHz to 3GHz and interferer power levels of up to -10dBm. The minimum convergence time of the algorithm for a 2GHz interferer with -10dBm is about 25ns. The total average noise figure, in case of no present interferer becomes 6.2dB. For present interferer the noise figure rises up to 21dB. . The manufactured design need to be validated and compared with its simulation results of the validation, according to the given test plan.

Approaching the large operating bandwidth has shown some difficulties due to the accumulating phase shifts of major circuit blocks that can invert the direction of control loop if they are greater than +/- 90°. For future work on the topic of adaptive narrow-band interferer cancellation, the filter topology needs to be optimized so that a larger bandwidth can be attained. An example of a bandwidth extension is shown in Fig. 8.1.

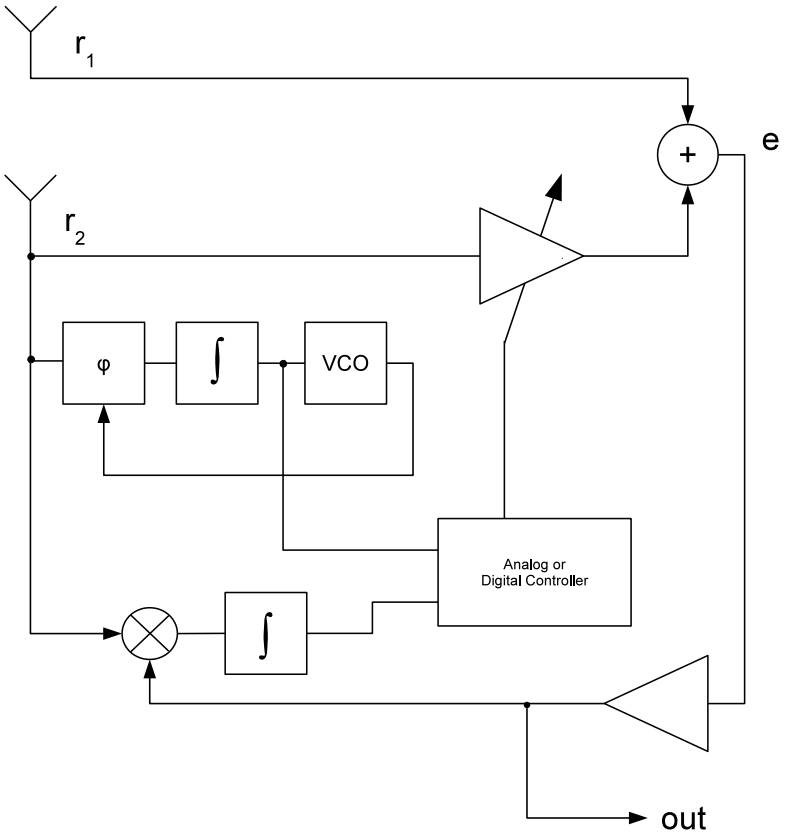


Figure 8.1: Bandwidth Extension

To be able to extend the operational bandwidth a frequency information of the interferer is necessary, which can be, for example, extracted out of a PLL. The frequency information can then be used to set the loop in that direction, so that the algorithm will always try to minimize interferers. This can be done with a digital or an analog control circuit, that sets the loop direction fora certain frequency band in the direction for interferer cancellation. With this additional circuitry and a smaller RF- CMOS technology a reasonable bandwidth extension can be expected.

Appendix A

Circuit Simulations

A.1 Combiner

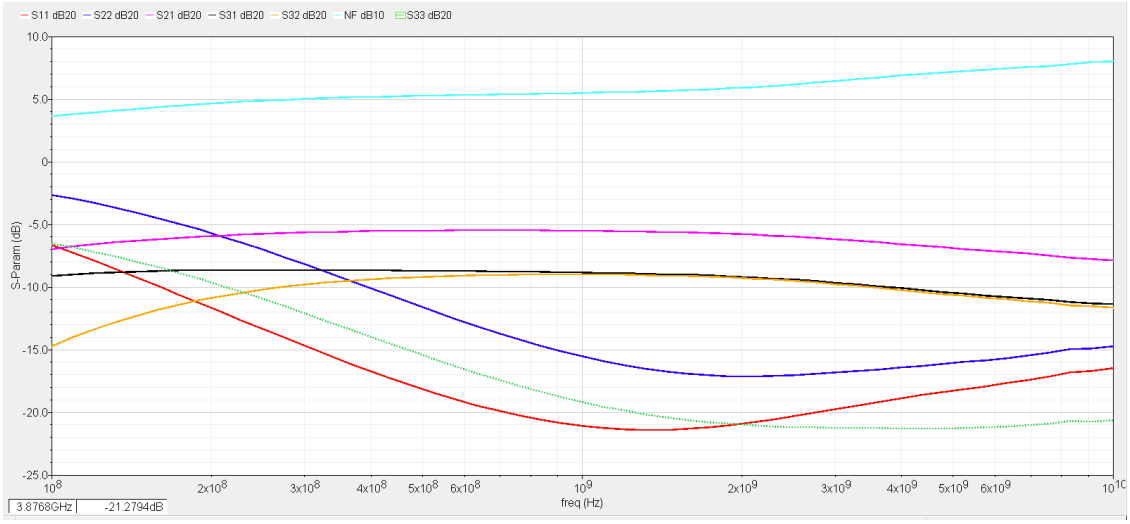


Figure A.1: Combiner - S-Parameter Simulation

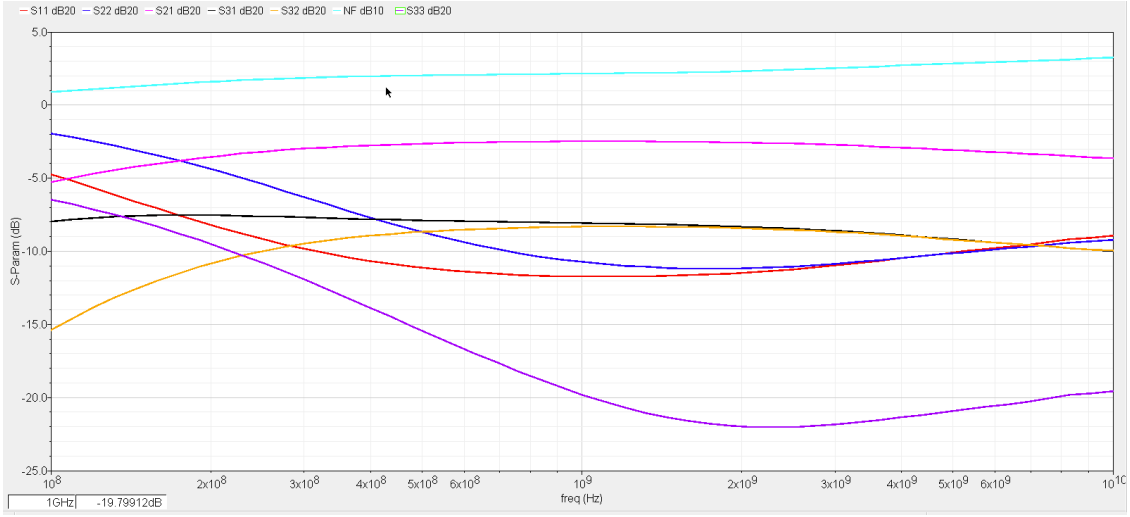


Figure A.2: Combiner without series resistors R_1 and R_2- S-Parameter Simulation

A.2 LNA

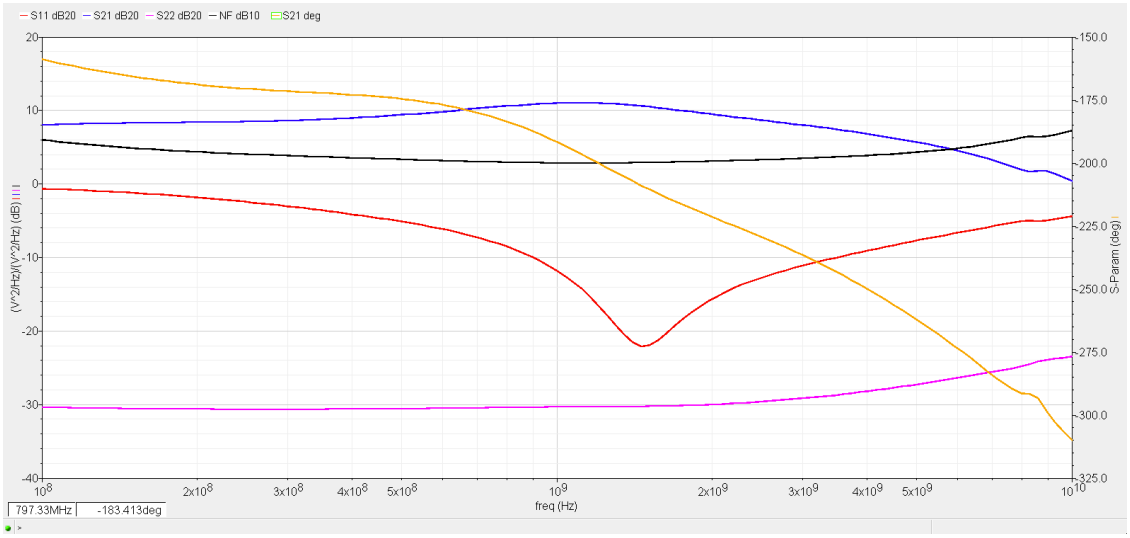


Figure A.3: LNA - S-Parameter Simulation

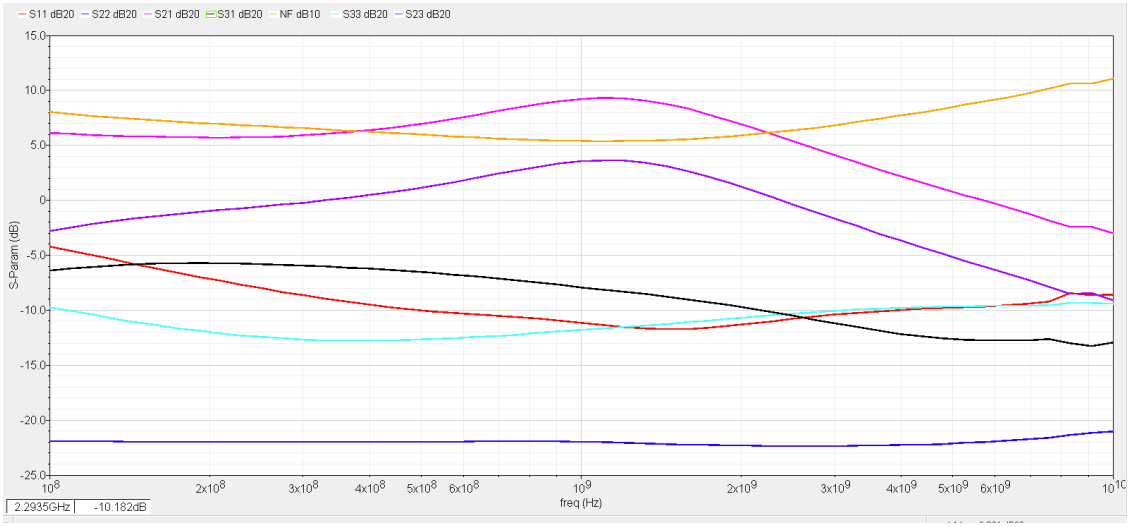


Figure A.4: LNA with Combiner - S-Parameter Simulation

A.3 Active Balun

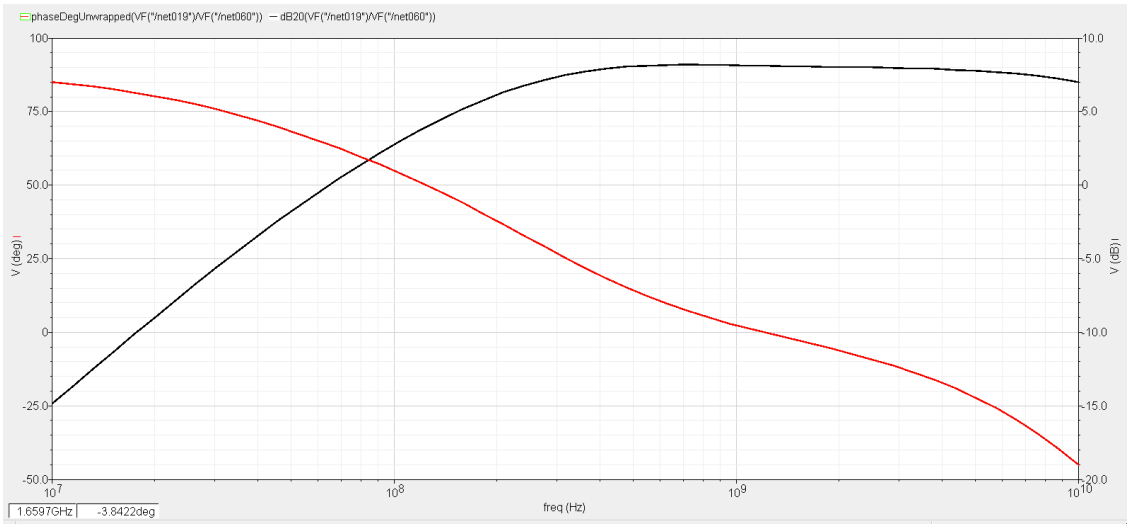


Figure A.5: Active Balun - Transfer Funtion

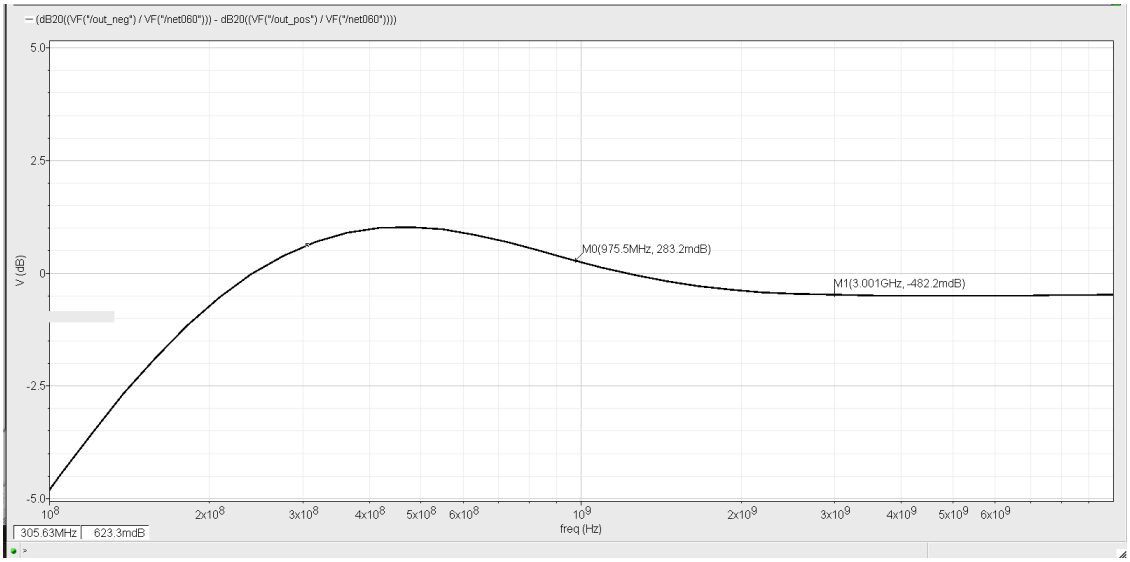


Figure A.6: Active Balun - Gain Error

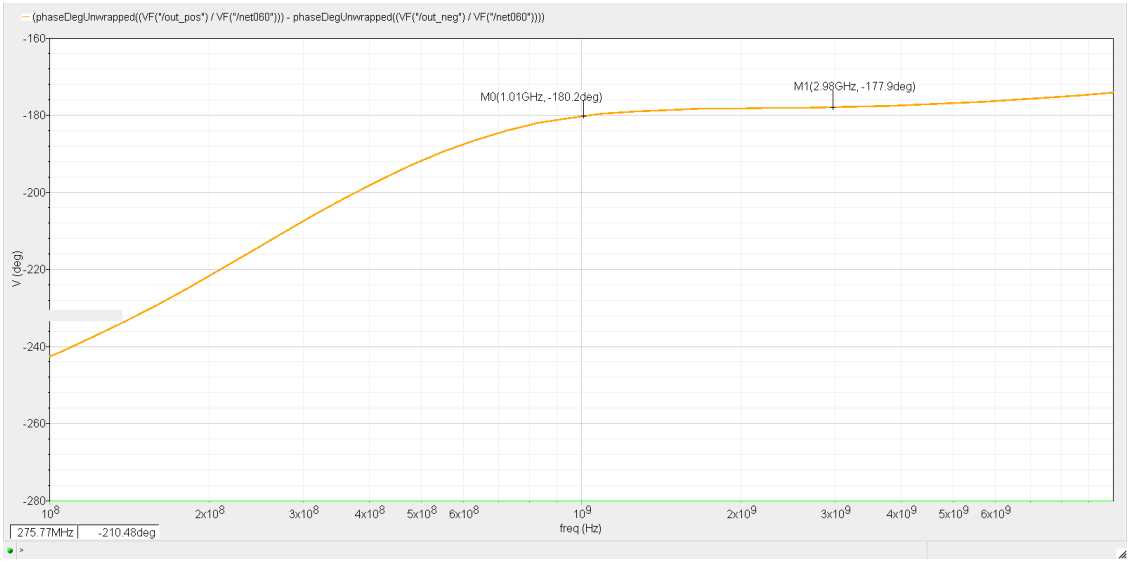


Figure A.7: Active Balun - Phase Difference

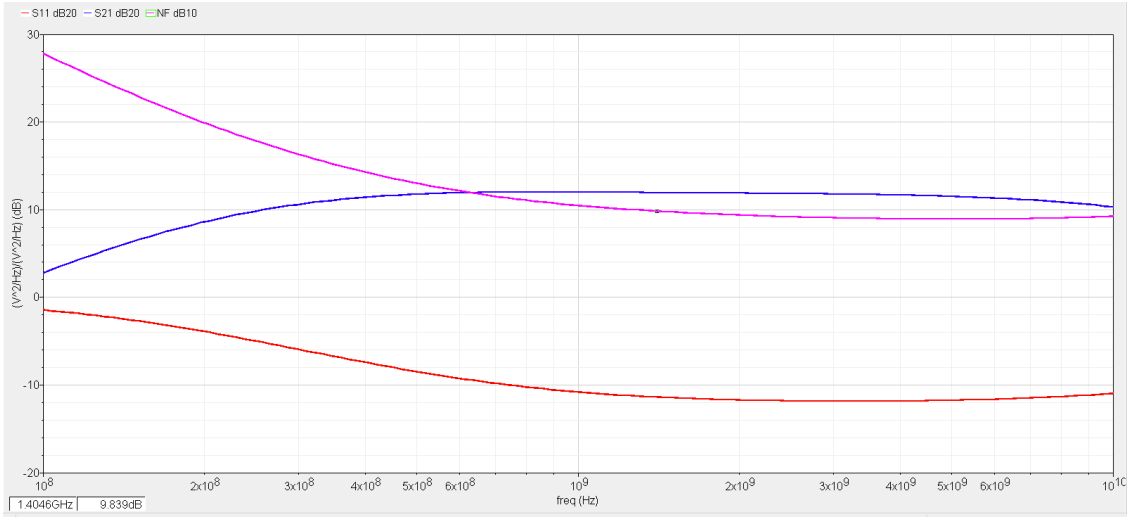


Figure A.8: S-Parameter Simulation - Active Balun LNA

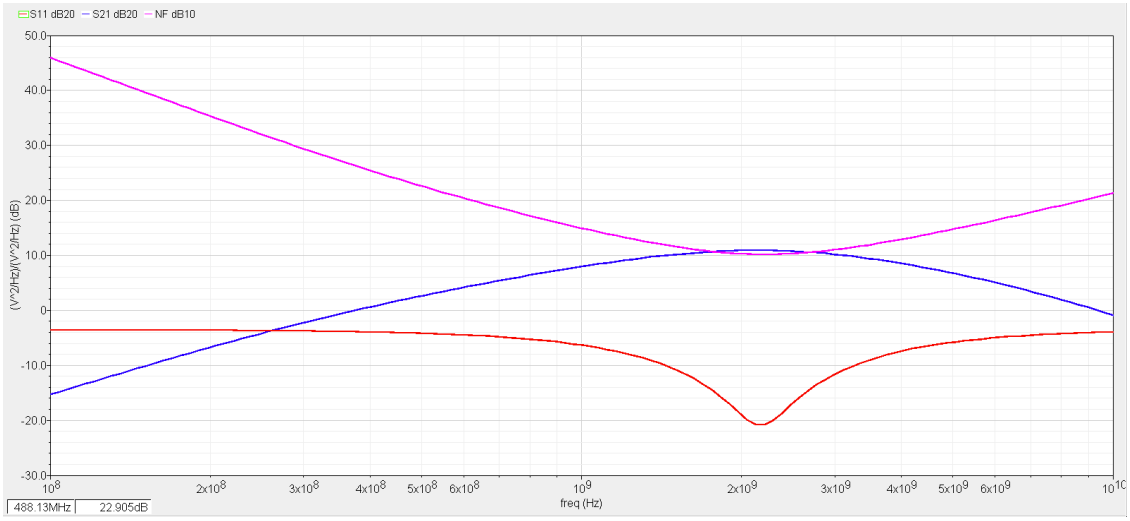


Figure A.9: S-Parameter Simulation - Active Balun LNA with ext. matching

A.4 90° Hybrid

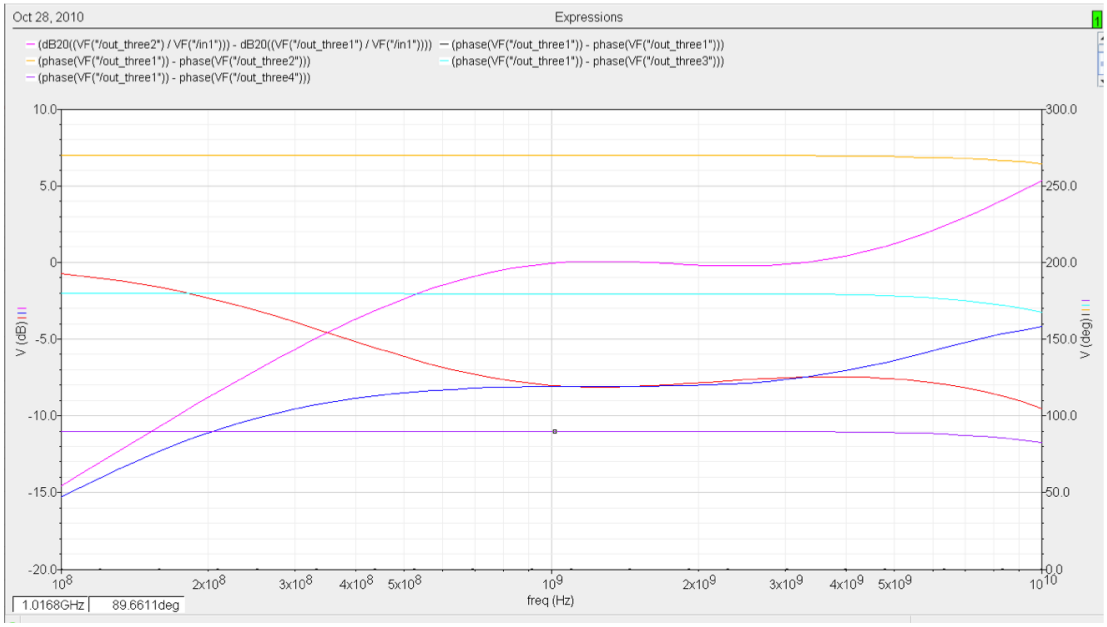


Figure A.10: 90° Hybrid - transfer function and gain and phase accuracy

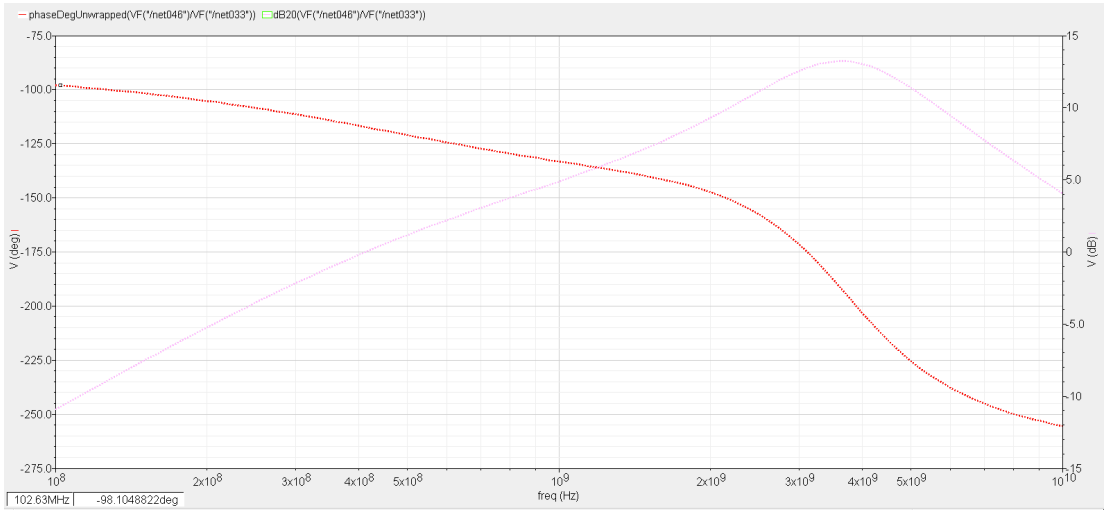


Figure A.11: After 90° Hybrid following differential amplifier transfer function

A.5 Correlation Multiplier

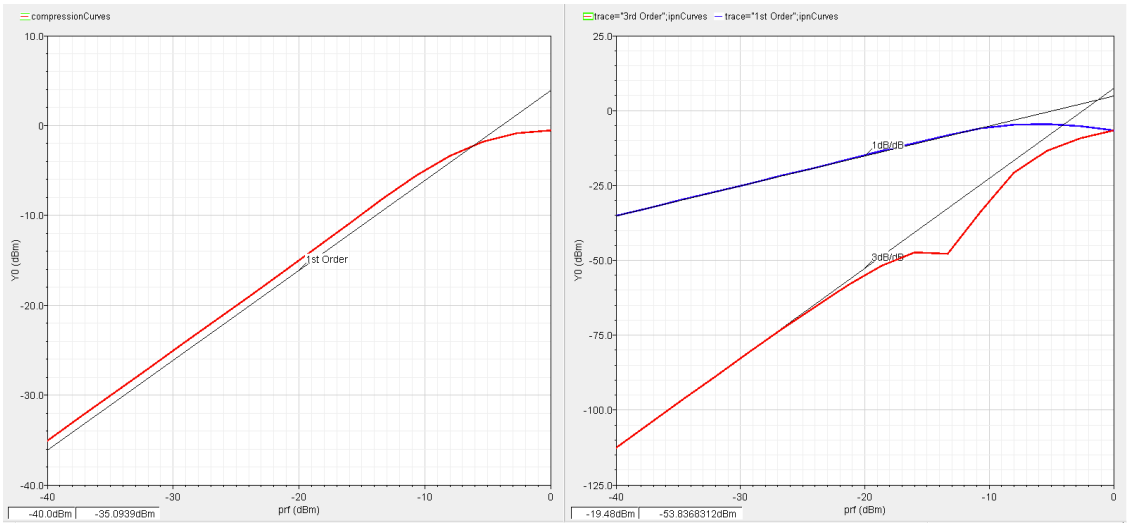


Figure A.12: RF1 - 1dB compression and IP3 - QPAC Simulation

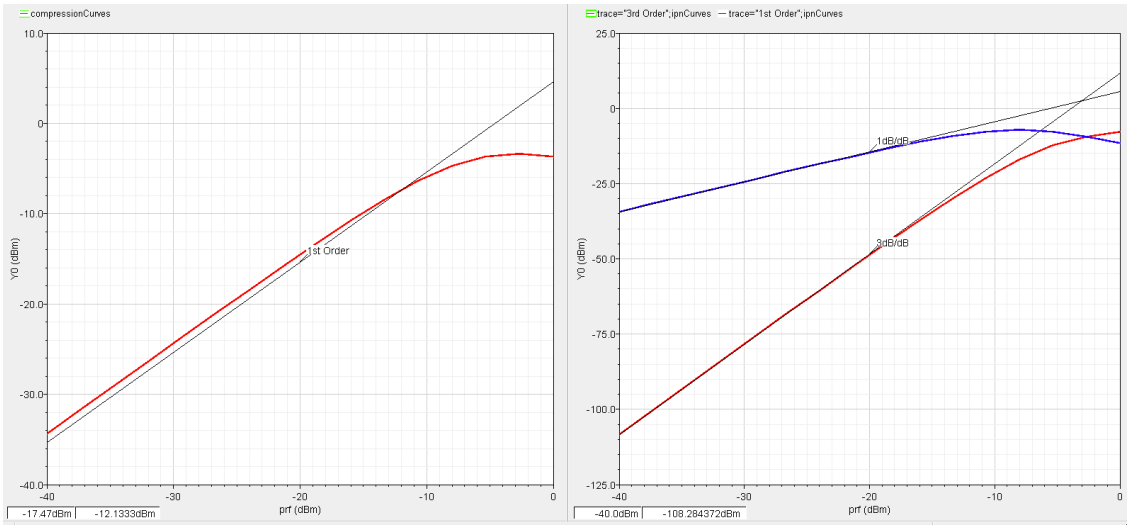


Figure A.13: RF2 - 1dB compression and IP3 - QPAC Simulation

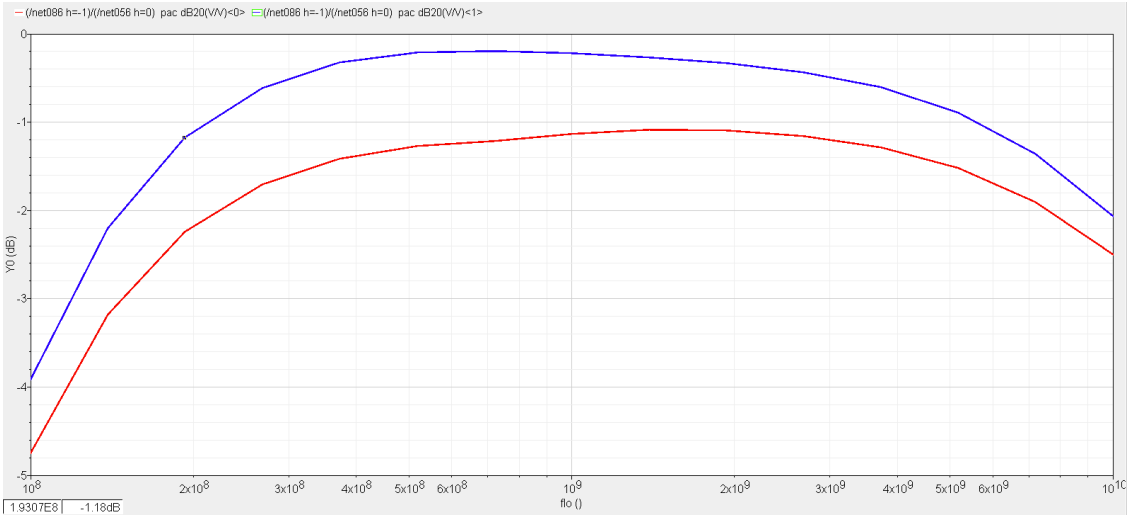


Figure A.14: RF1 input bandwidth (red) and RF2 input bandwidth (blue) - PAC Simulation

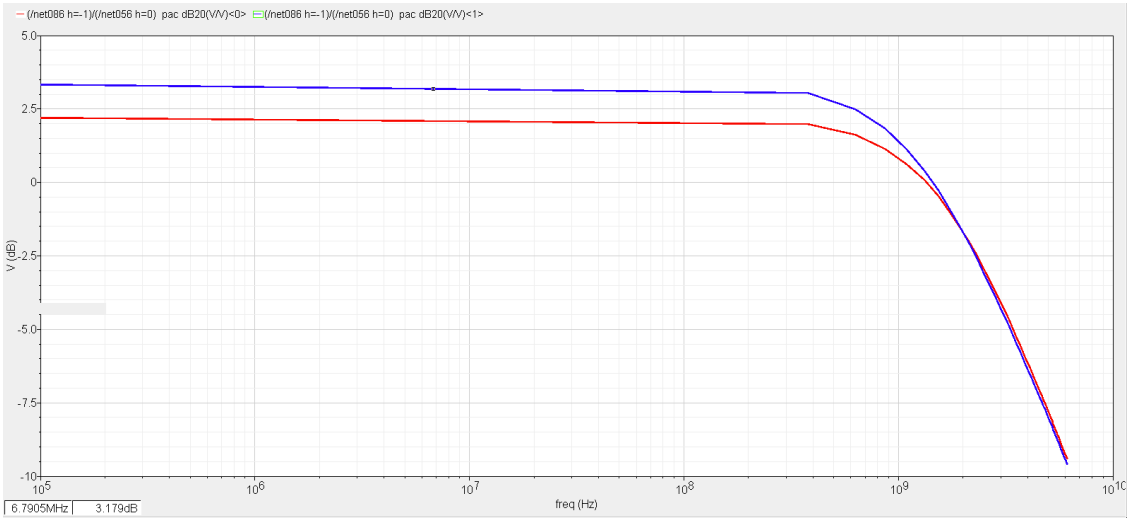


Figure A.15: IF output bandwidth for RF1 (red) and RF2 (blue) - PAC Simulation

A.6 Integrator

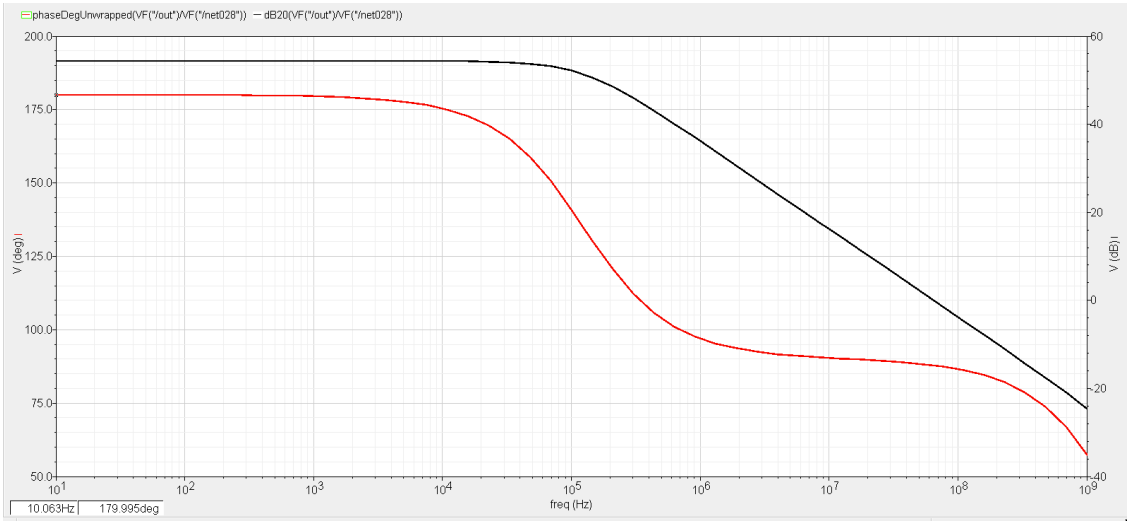


Figure A.16: Integrator with implemented 20pF MIM capacitor

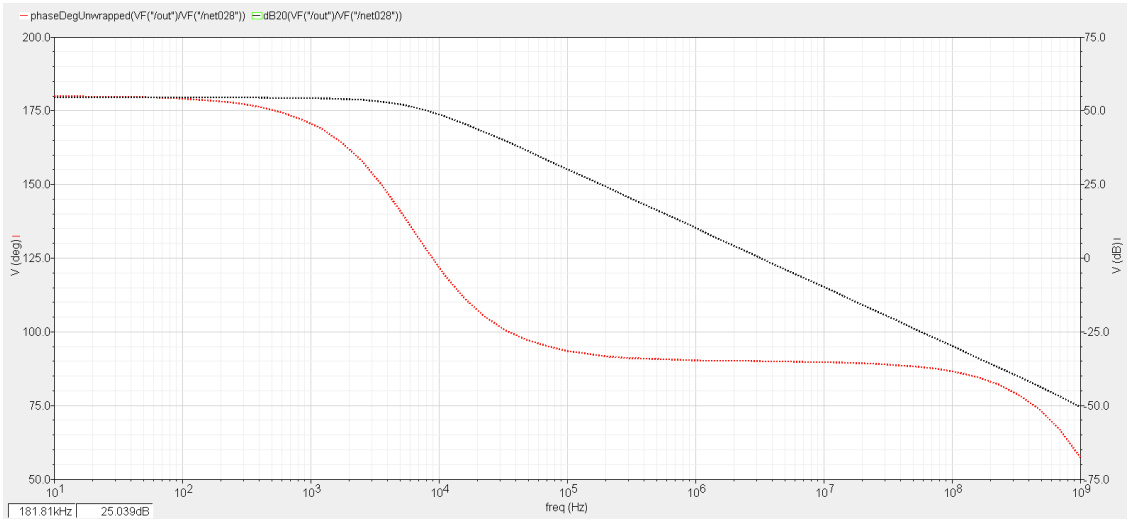


Figure A.17: Integrator with additional 380pF external capacitance

A.7 Complex Multiplier

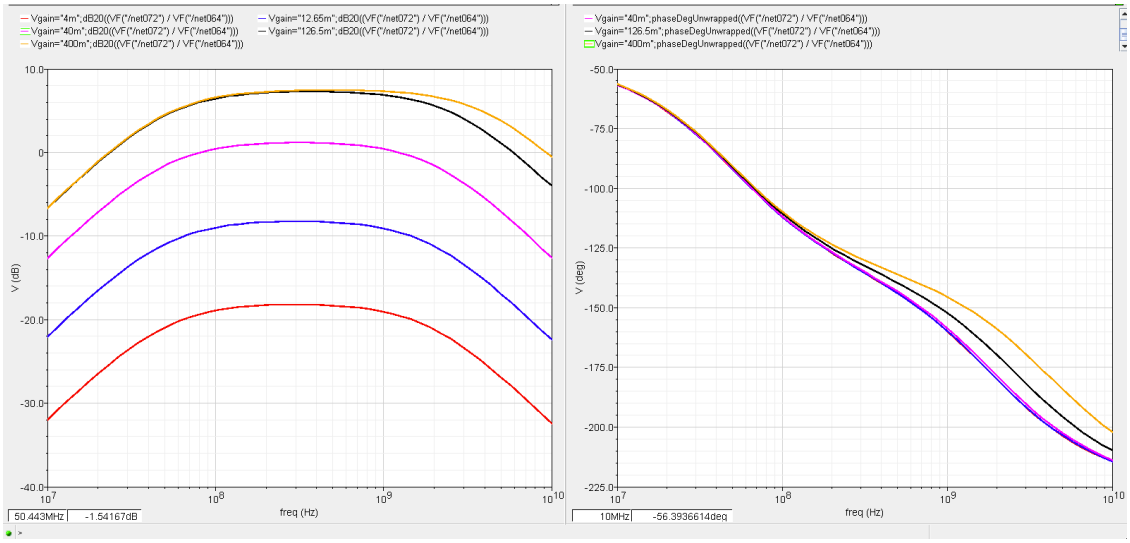


Figure A.18: Complex Multiplier Transfer function

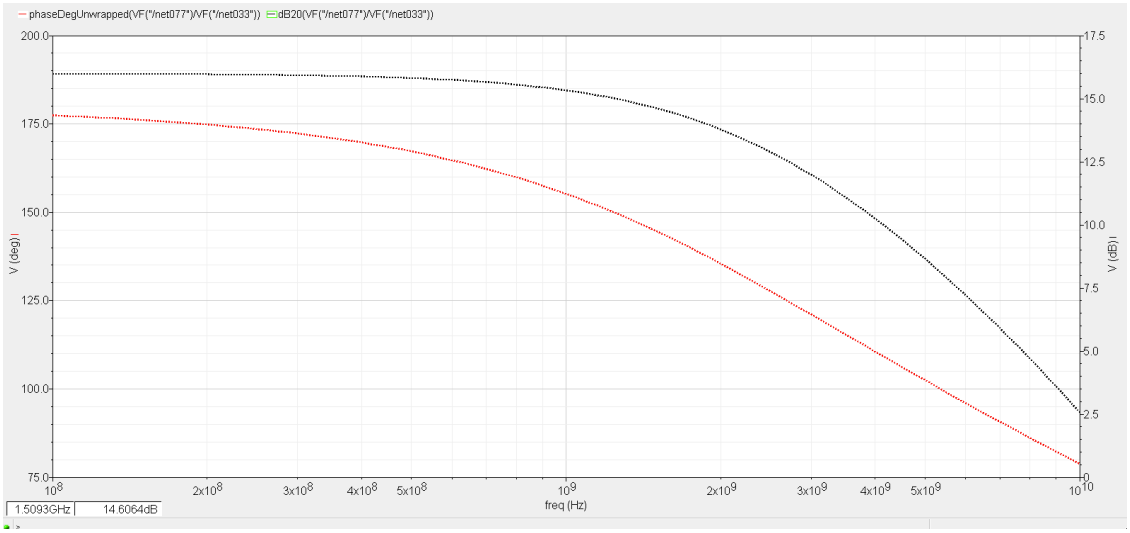


Figure A.19: Differential to single-ended stage transfer function

A.8 Phase Equalizer

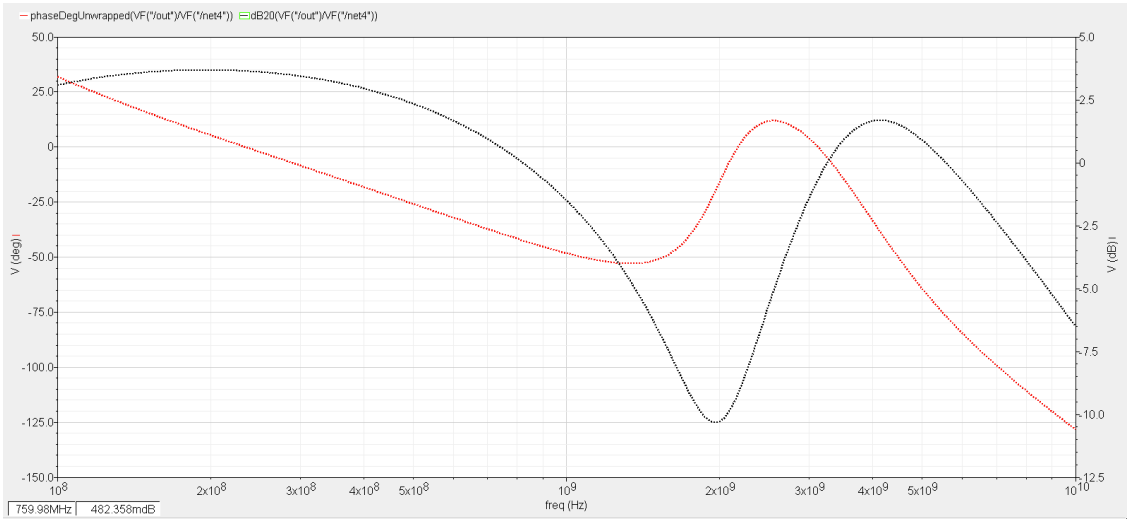


Figure A.20: Phase Equalizer transfer function

A.9 Buffer

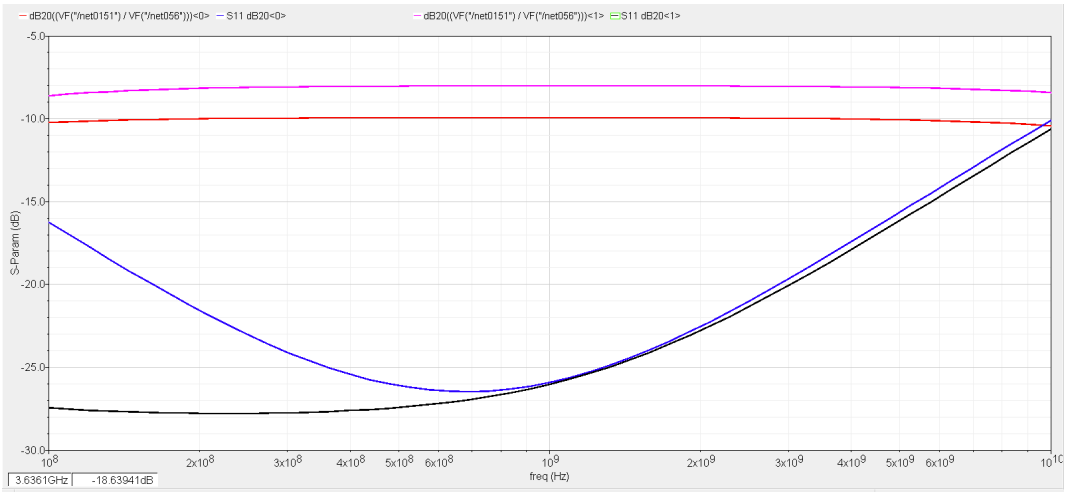


Figure A.21: Buffer transfer function

A.10 Biasing

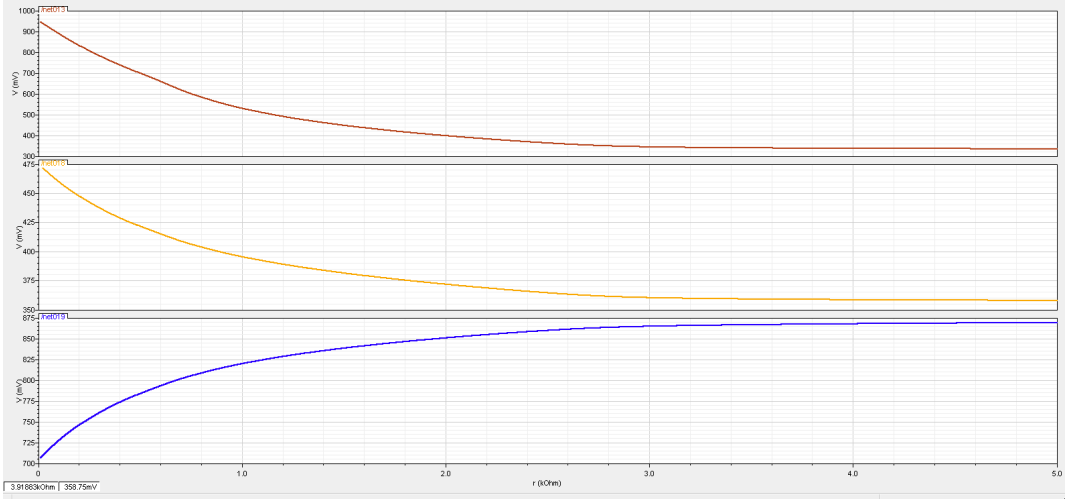


Figure A.22: Bias Circuit Vs R_{EXT}- From up to down: 600mV, 400mV, 800mV

A.11 Digital Circuit

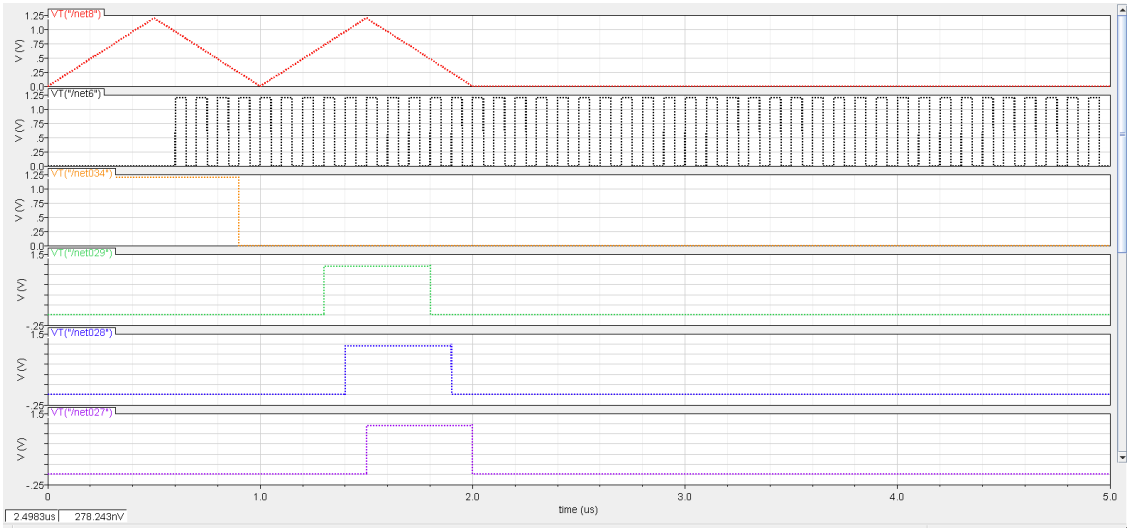


Figure A.23: Shift Register - Time Domain Simulation

Appendix B

Time Domain System Simulations

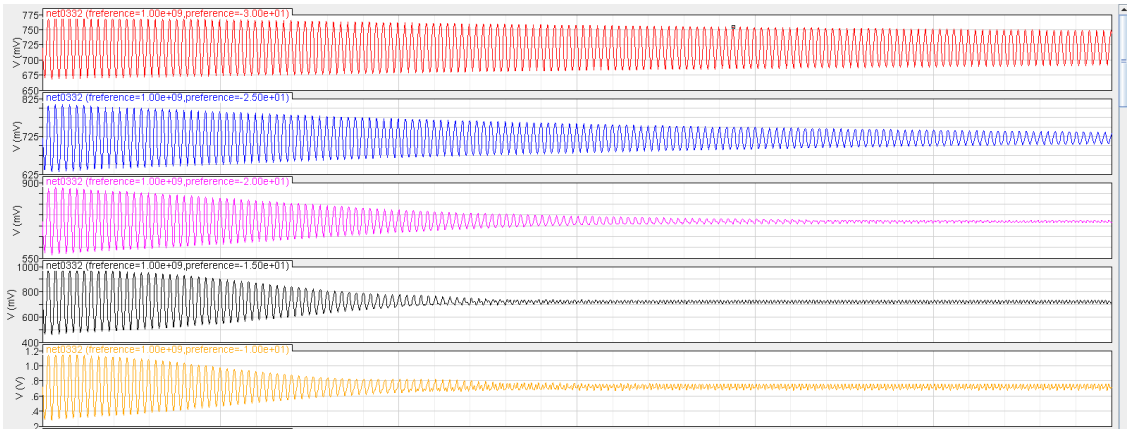


Figure B.1: Interferer at 1.0 GHz, input power -30dBm -to -10dBm

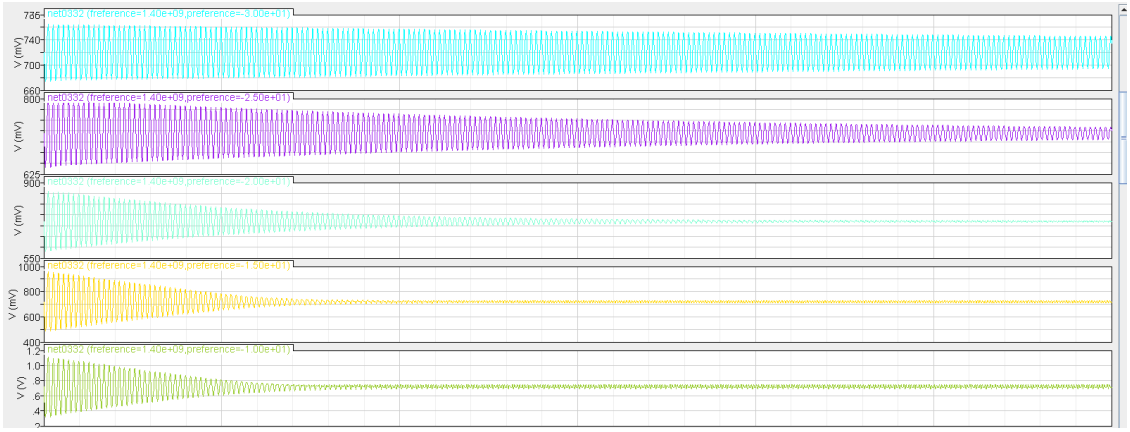


Figure B.2: Interferer at 1.4 GHz, input power -30dBm -to -10dBm

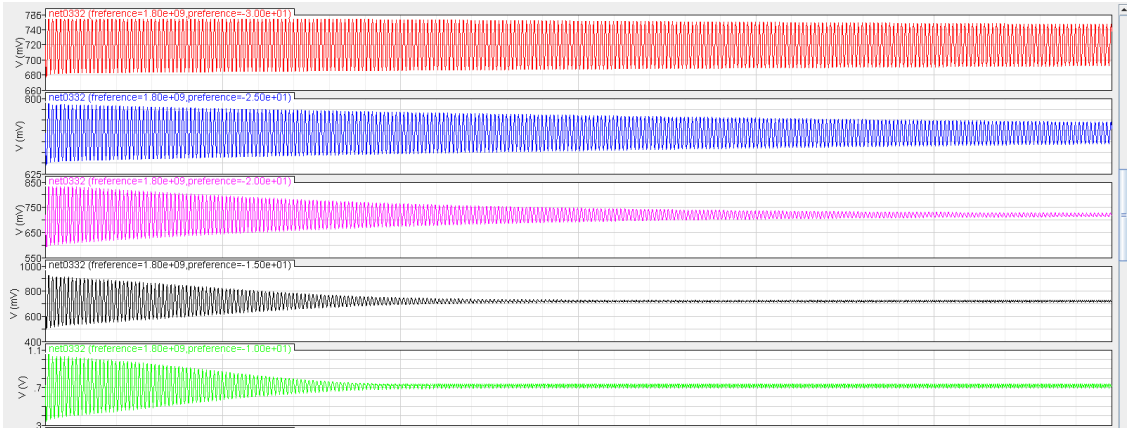


Figure B.3: Interferer at 1.8 GHz, input power -30dBm -to -10dBm

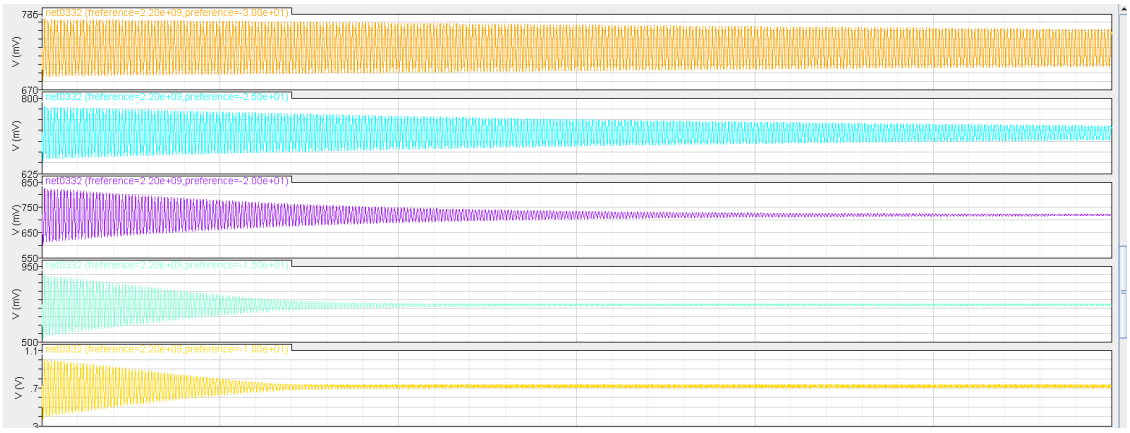


Figure B.4: Interferer at 2.2 GHz, input power -30dBm -to -10dBm

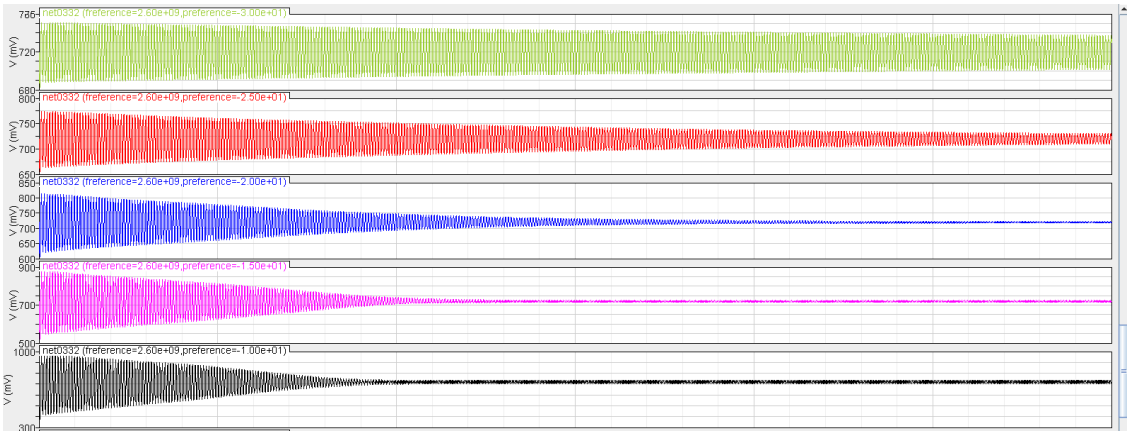


Figure B.5: Interferer at 2.6 GHz, input power -30dBm -to -10dBm

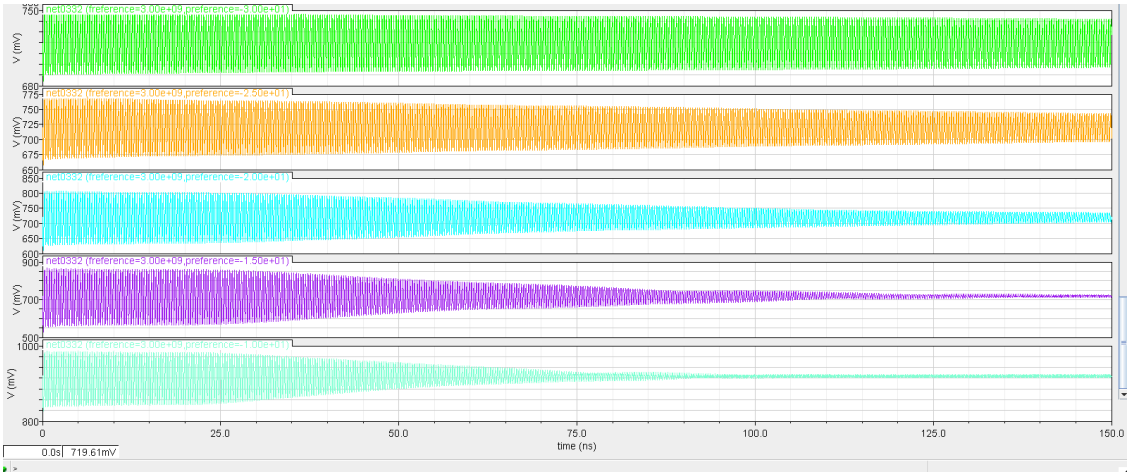


Figure B.6: Interferer at 3.0 GHz, input power -30dBm -to -10dBm

Appendix C

MatLAB BER Simulation Model

```
%%%-----------Settings Matlab
    ------------------%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%
clc;
clear all;
close all;
set(0,'DefaultLineLineWidth',2);
set(0,'DefaultAxesFontSize',14);
set(0,'DefaultTextFontSize',14);
set(0,'DefaultTextFontName','Tahoma');
set(0,'DefaultAxesFontName','Tahoma');
% %%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%%

%Definitions
BW_UWB=1e9
BW_Bit=200e6
BW_ratio=10*log10(BW_UWB/BW_Bit)
%BW_ratio=0
M=25;   %Number of different signal levels
```

```
Mi=5;   %Number of interferer interferer levels

Es_dB=15   % Setting Es in dB
EstoNo_dB=linspace(0,8.5,M); %Es to No ratio
A=sqrt(10.^(Es_dB./10));                %useful signal amplitude

Pi_dB=linspace(0,15,Mi);
Ei_dB=Pi_dB-BW_ratio;
Ei=(10.^(Pi_corr_dB./10))

%Ei_dB=linspace(0,15,Mi); %interferer energy
%Ei=(10.^(Ei_dB./10)); %interferer amplitude
Ai=sqrt(2.*Ei)

No_dB=-EstoNo_dB+Es_dB;

%No_dB=linspace(6,17,M);
%No_dB=11
No=10.^(No_dB./10);

MinErrCount=600; %loop will stop after min MinErrCount is achieved

fi=1e9;
nmax=100;
ni=1:1:nmax;
fn=nmax*fi;
Tn=1/fn;
omega=2*pi*fi;
int=Ai'*sin(omega.*ni.*Tn); %ni-times sampled sine wave
length(A);
errorcount=zeros(Mi,M);
```

```
errcount_old=0;
trials=zeros(Mi,1);
i=0;
BER=ones(Mi,M);
IN=zeros(Mi,M)
for k=1:Mi
   while errorcount(k,M) < MinErrCount

        trials(k)=trials(k)+1;
        sign=ceil(2*rand(1)); %BPSK Modulator
        if sign==1
            s=A;
        else
            s=-A;
        end

        n=randn(1)*sqrt(No./2); %Noise Generator
        int(mod(i,length(int))+1);
        r=s+n+int(k,mod(i,nmax)+1);% AWGN Channel plus Narrowband Interferer

        %M Parallel BER Testing
        err1= r > 0 & sign==2;
        err2= r < 0 & sign==1;

        errcount_old=errorcount(k,M); %
        errorcount(k,:)=err1+err2+errorcount(k,:) ;

        if errorcount(k,M) == errcount_old
        else
           errorcount(k,M) %status display
        end
```

```
    end
    BER(k,:)=errorcount(k,:)./trials(k);
end

%No= No/2



Es=A.^2;
SINR=10.*log10(Es./IN)
alpha=sqrt(2*Es./No);



%%%%%%%%          Output  %%%%%%%%%%%%%%%%%%%%%%%%%%
figure
h2=semilogy(10.*log10(Es./(No)),BER,10.*log10(Es./No),.5-.5.*erf(alpha./sqrt
    (2)));
grid minor
l=legend(strcat('$\frac{I}{S}=$',int2str((-Es_dB+Ei_dB+BW_ratio)')))
set(l,'Interpreter','latex','Location','NorthEastOutside');
xlabel('E_B/N_o_in_dB')
ylabel('Bit_Error_Rate')
```

Appendix D

Matlab Model Time Domain Simulation

```
%%%----------Settings Matlab----------
clc;
clear all;
close all;
set(0,'DefaultLineLineWidth',2);
set(0,'DefaultAxesFontSize',14);
set(0,'DefaultTextFontSize',14);
set(0,'DefaultTextFontName','Tahoma');
set(0,'DefaultAxesFontName','Tahoma');
% %%%%%%%%%%%%%%%%%%%%%%%%%%
%
%
loops=1

phi_In=[15 30 60 90]
phi_In=-90 %RF Input Phase
fc=2e9
fs=40e9     %sampling rate
```

```
tau=150e-12  %length of single pulse
Es=1e-9      %energy of one single pulse
Tf=50e-9 %pulse repetition time

Pseudo=PRNGen %% Pseudo Random Code loading

%Gaussian Doublet
K_g=tau*sqrt(tau*Es/3/sqrt(pi/2))
t   = -max/fs/2: 1/fs : (max)/fs/2;            % Gaussian Doublet signal time
y=-K_g*2/(tau^2)*(1-2.*(t).^2./tau^2).*exp(-((t)./tau).^2);

%Interferer Parameter:
ISR=10
Ei=10^(ISR/10)*Es
Bandwidth=100e3
omega_int=2*pi*fc;
Ai=sqrt(Ei/Tf*2)
gain=2e-2/Ai % Step size Parameter
phi_Int=90 % Interferer Phase


Nt=50 %number of pulses in pulse train = pulse train length
t_end=Tf*(Nt+1);
t1   = 0 : 1/fs : t_end;   % signal evaluation time
N=length(t1)-1
trans_end=round(length(t1).*3./4);
Ns=length(t1)


co=299.792e6 %Speed of Light
```

```
f=2*1e9
lambda=co/f
d=lambda*[.25 .5 2 4 8]
d=lambda*.25 %Element Displacement
loops=1

filteroutput=zeros(loops,N);
err=zeros(loops,N);
WI=zeros(loops,N);
WQ=zeros(loops,N);

for(k=1:loops) % Loops for Monte Carlo Analysis



%lambda=co/f
%d=lambda*32/4 %element displacement

t_element=d./co *sin(deg2rad(phi_In(k))) %signal time shift due to element
    delay
t_delay=0*1e-9 %fixed delay in circuit

t_element_i=d./co *sin(deg2rad(phi_Int)) %Time shift of interferer
phi_i=360*f*t_element_i(1) %Phase shift of interferer




for (ii=1:Nt) %Until the end of the pulse train

%%%%%%%%%%%%%%
```

```
%Input Signal
%%%%%%%%%%%%%%

    T1=ii*Tf;
    bit=ceil(2*rand(1)); % BPSK Modulator
    if bit==1
        T2=0;
    else
        T2=Tf/3; %PPM
    end
    T3(ii)=Pseudo(mod(ii,1022)+1)*Tf/length(Pseudo)/2; % Time Hopping
    %T3(ii)=Pseudo(mod(ii,1022)+1)*Tf/15;
    tn(ii)=T1+T2+T3(ii); % Time delay Input 1
    tn2(ii)=T1+T2+T3(ii)+t_element(1)+t_delay; % Time delay Input 2

end

yp = pulstran(t1,tn,@doublet,tau,Es); % Generates Pulsetrain for RF input 1
yp2 = pulstran(t1,tn2,@doublet_phase,tau,Es,phi); % Generates Pulsetrain for
    RF input 2


%%%%%%%%%%%%%%
%Interferer
%%%%%%%%%%%%%%

OnOff=zeros(1,Ns);
OnOff(round(Ns*4/16):round(Ns*14/16))=1 ; %Interferer on off
OnOff(round(1e-7*fs):round(Ns*(7/8)))=1; %Interferer on off

interferer=Ai(1).*sin(omega_int.*t1).*OnOff;
```

```
interferer2= Ai(1).*sin(omega_int.*t1-deg2rad(phi_i(1))).*OnOff; %Different
    angle of arrival!!!
%interferer2=real(Ai(k)./2*sinc(Bandwidth*(t1-4e-6)).*exp(i.*((t1-4e-6).*omega
    +deg2rad(phi_i)))/sqrt(2*pi));

SLevel(k)=abs(min(yp))+abs(min(yp))
ILevel(k)=abs(min(interferer))+abs(min(-interferer))

x=zeros(loops:N)
X=zeros(loops:N)

N=length(t1)-1 %feedback

In=interferer+yp; % RF In 1

x=yp2+interferer2; %RF In 2
X=imag(hilbert(x));

LNAgain=1;
att=1
ii=1

%%%%%%%%%%%%
%LMS Algorithm Begin
%%%%%%%%%%%%

    for(ii=1:N)
        WI(k,ii+1)=WI(k,ii)+gain.*(err(k,ii)).*(x(ii));
        WQ(k,ii+1)=WQ(k,ii)+gain.*(err(k,ii)).*(X(ii));
        filteroutput(k,ii)=WI(k,ii).*x(ii)+WQ(k,ii).*X(ii);
        %WI_old(ii)=WI(ii);
```

```
        %WQ_old(ii)=WQ(ii)
        err(k,ii+1)=LNAgain.*(In(ii)-att*filteroutput(k,ii));
    end

%%%%%%%%%%%%
%LMS Algorithm End
%%%%%%%%%%%%


level(k,:)=min(abs(err(k,trans_end:N))+abs(min(-err(k,trans_end:N))));

PlotErr=0;
PlotIn=0;
end

%%%%%%%%%%%%
%Plotting
%%%%%%%%%%%%

%plot(t1(1:N),filteroutput(1:N));
figure;
plot(t1,(err));
%legend(num2str((180-phi_In)'))
axis([1.245e-6 1.26e-6 -5 3.5]);
grid minor
xlabel('t in s')
ylabel('signal amplitude')


figure
elevation(phi_In'./180.*pi,abs(level/min(level)),0,1,10)
```

```
level(k,:)=min(err(k,trans_end:N)+min(-err(k,trans_end:N)))

trans_end=round(length(t1).*3./4);

freq=linspace(0,fs,N-trans_end+2);
PlotErr=err(trans_end:length(err));
PlotIn=In(trans_end:length(In));



figure
plot(freq/1e9,20*log10(abs(fft(PlotIn))),freq/1e9,20*log10(abs(fft(PlotErr))))
    ;
axis([0 10 -100 50]);
xlabel('f in GHz')
ylabel('Power (normalized) in dB')
grid minor;

figure
plot(freq/1e9,20*log10(abs(fft(PlotIn))));
axis([0 10 -100 50]);
xlabel('f in GHz')
ylabel('Power (normalized) in dB')
grid minor;

figure
freq=linspace(0,fs,N-trans_end+2);
plot(freq/1e9,20*log10(abs(fft(PlotErr))));
axis([0 10 -100 50]);
xlabel('f in GHz')
ylabel('Power (normalized) in dB')
grid minor;
```

```
figure
plot(t1(1:N),LNAgain*In(1:N),t1(1:N),err(1:N));
axis([0 4e-6 -4 4]);
grid minor
xlabel('t in s')
ylabel('signal amplitude')
legend('Input','LMS Correction','Output')
```

Appendix E

Circuit Schematics

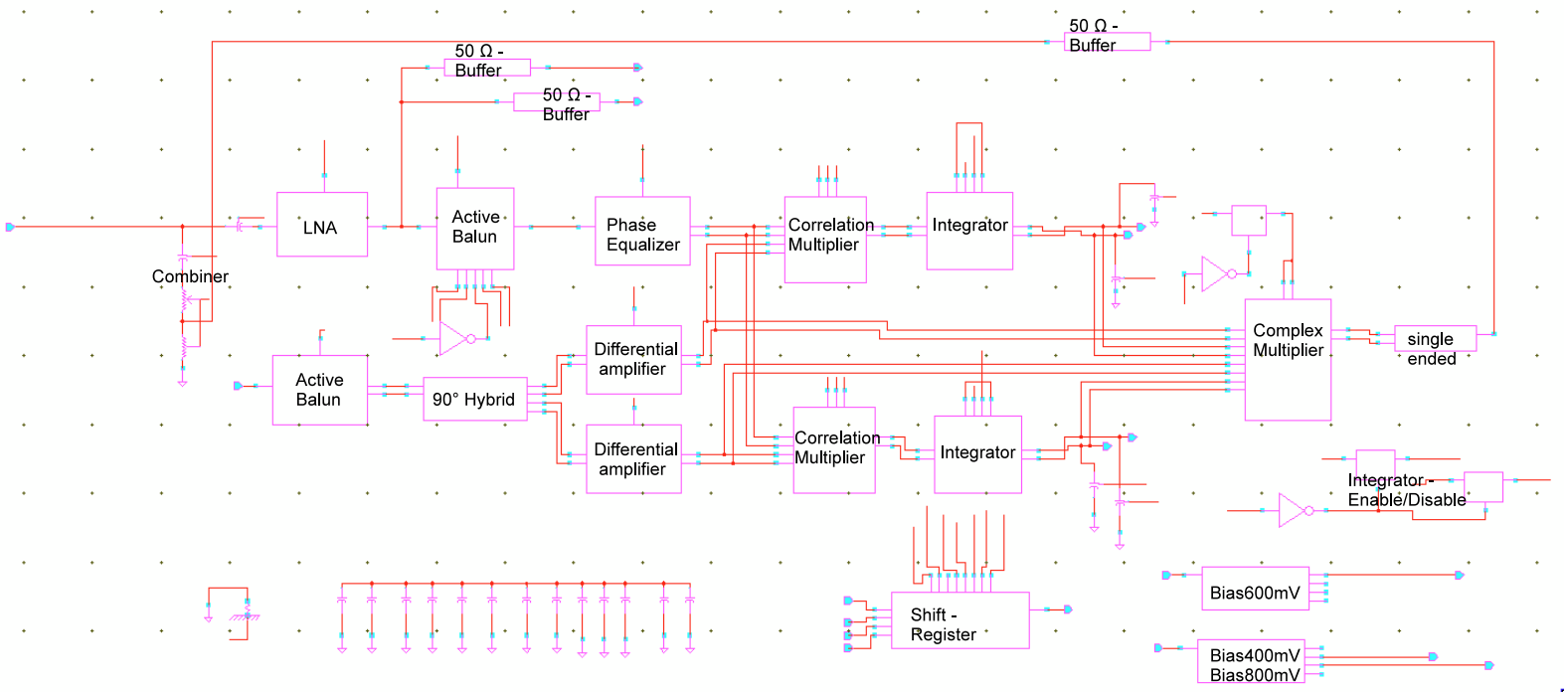


Figure E.1: TOP Level Schematic

E.1 Combiner

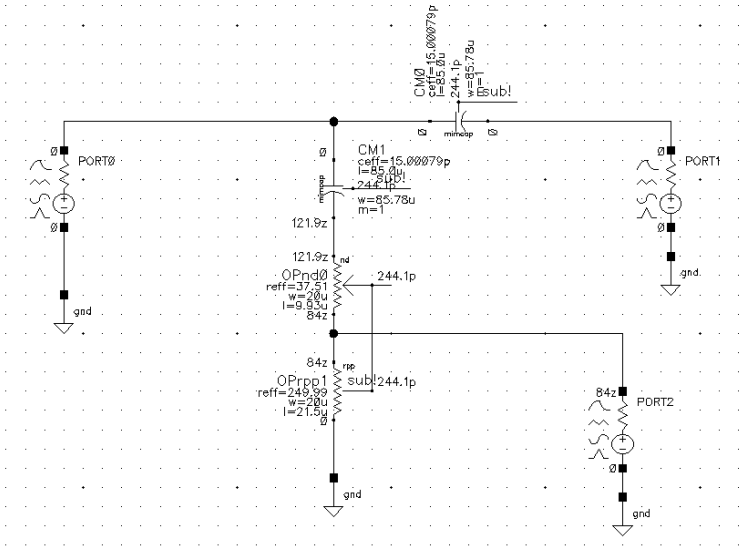


Figure E.2: Combiner Schematic

E.2 LNA

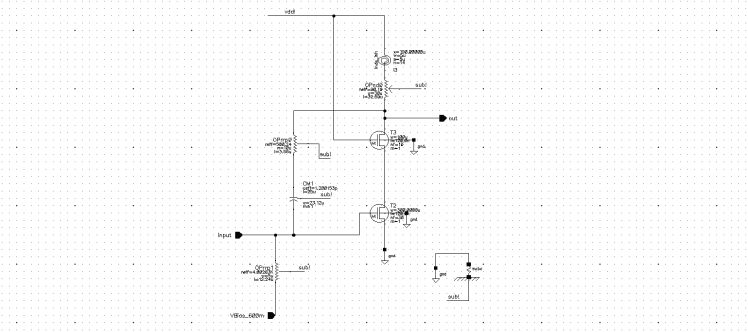


Figure E.3: LNA - Schematic

E.3 Active Balun

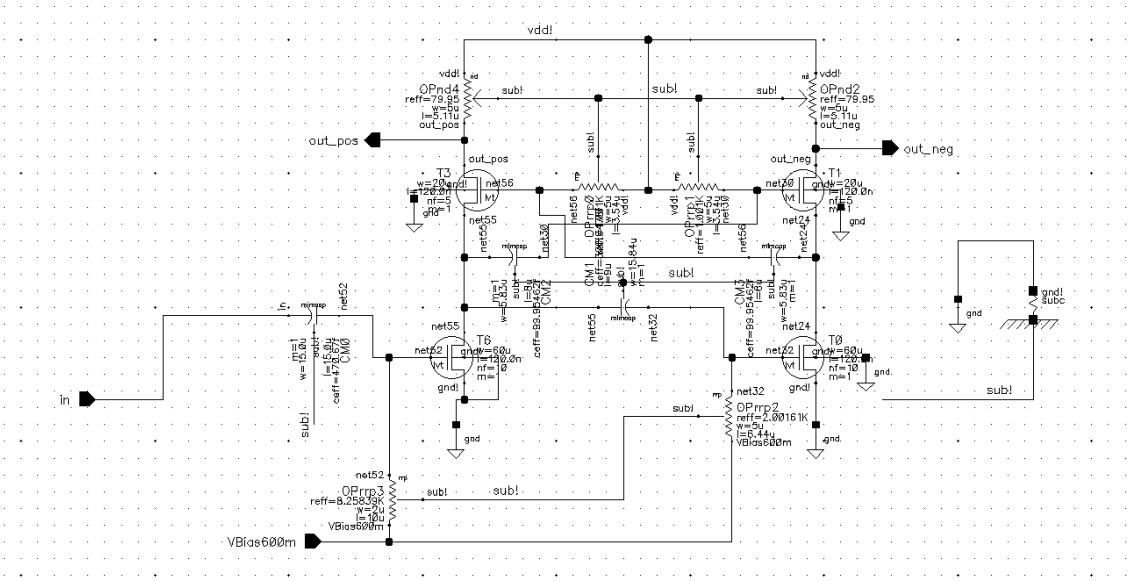


Figure E.4: Active Balun - Schematic

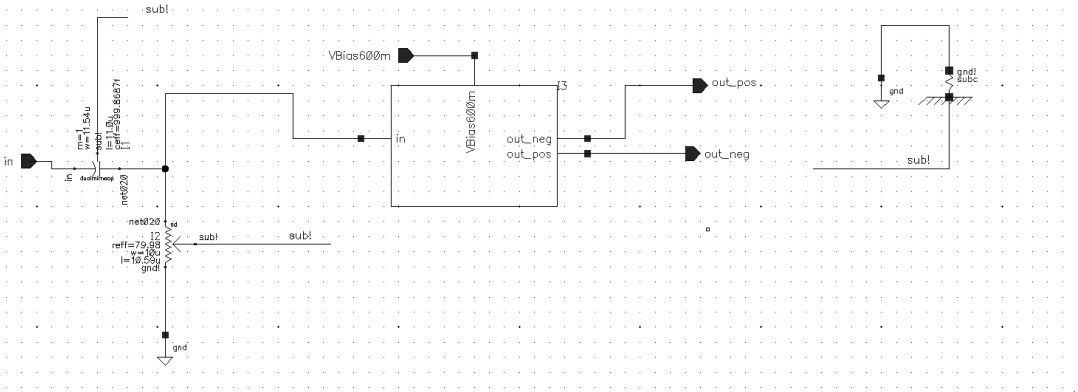


Figure E.5: Active Balun LNA - Schematic

E.4 90° Hybrid

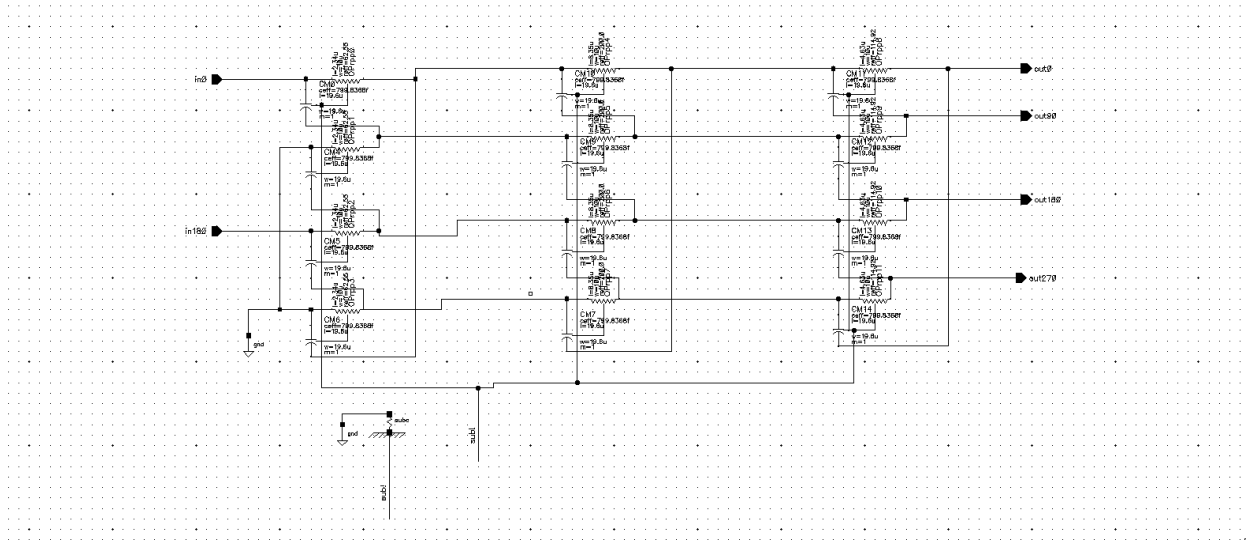


Figure E.6: 90° Hybrid - schematic

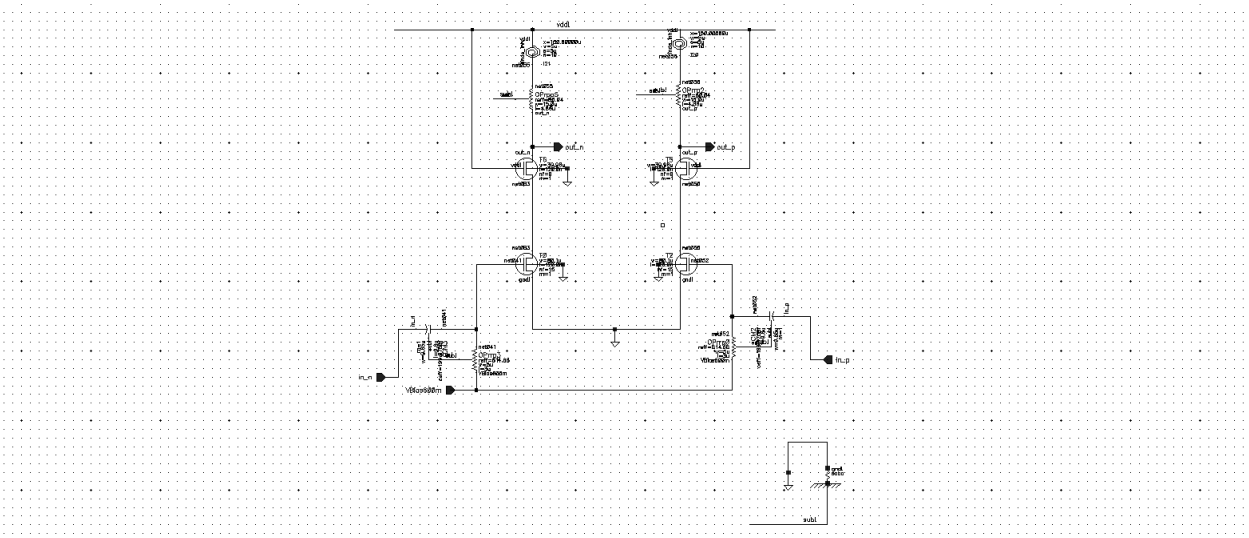


Figure E.7: Differential Amplifier Schematic - Follows Hybrid

E.5 Correlation Multiplier

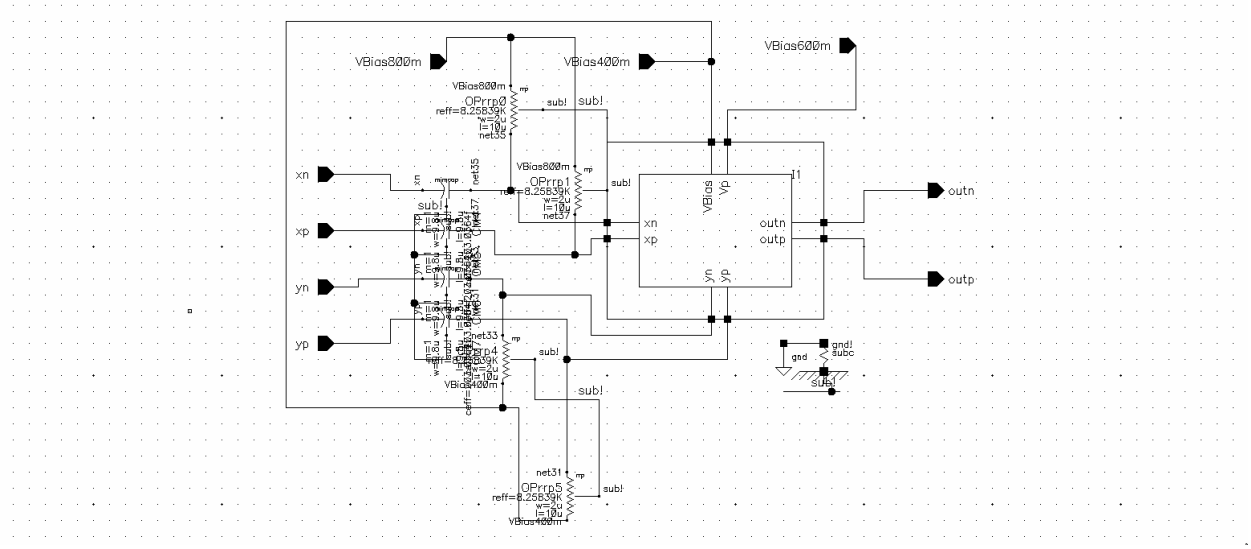


Figure E.8: Correlation Multiplier - TOP Level

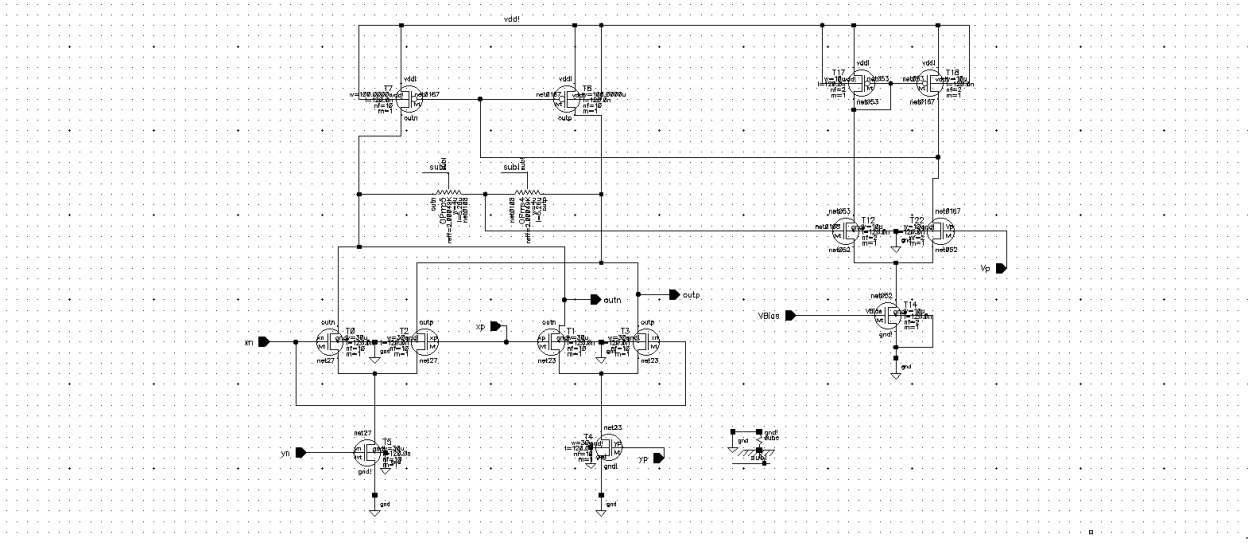


Figure E.9: Correlation Multiplier - Transistor Level with CMFB

E.6 Integrator

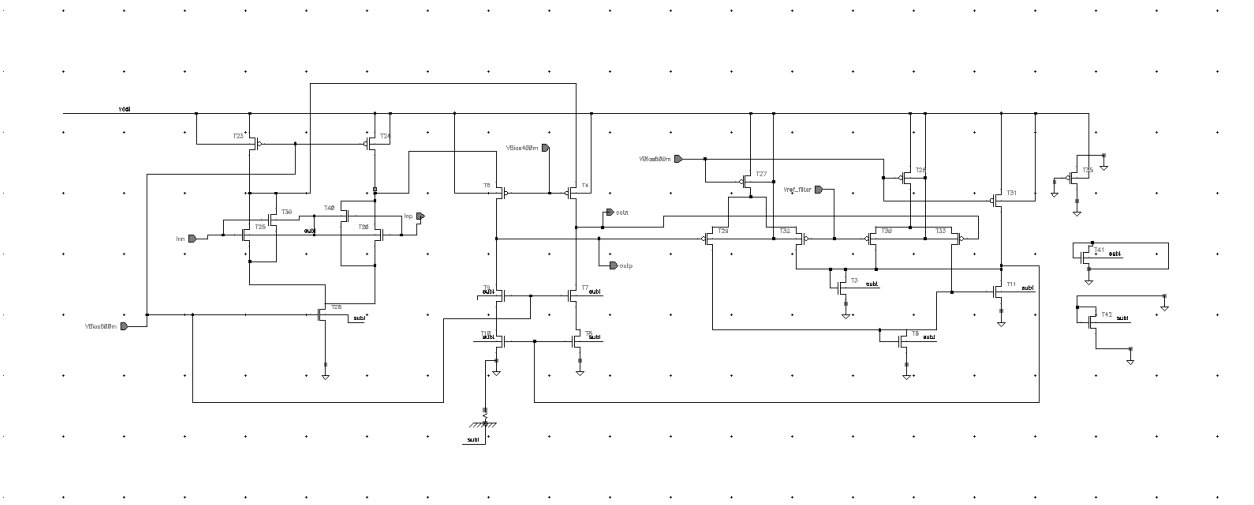


Figure E.10: Integrator with CMFB circuit

E.7 Complex Multiplier

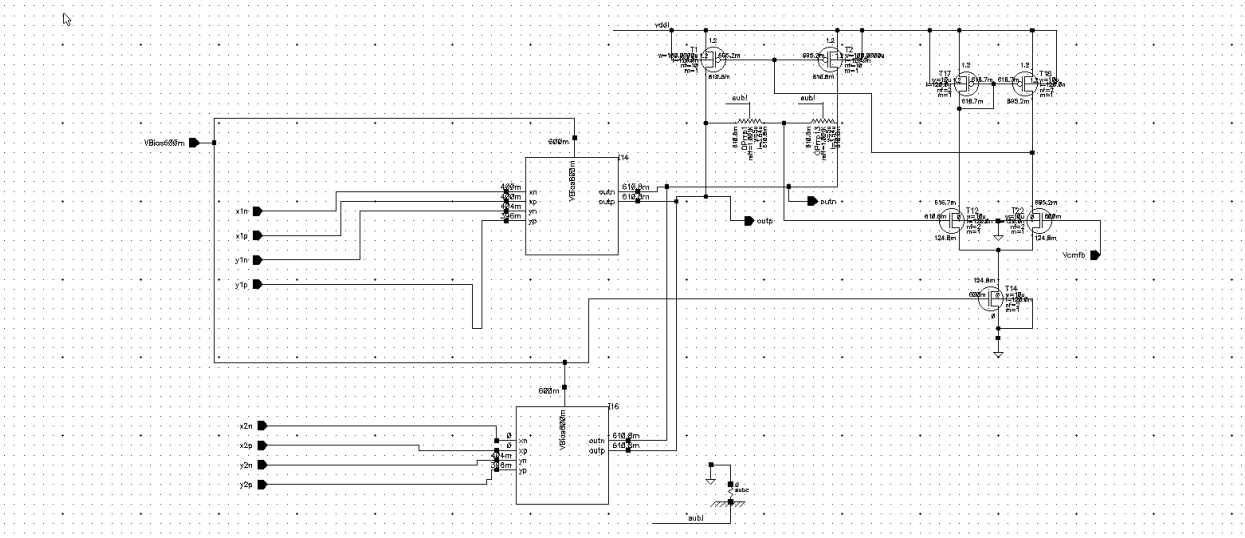


Figure E.11: Complex Multiplier - Top Level

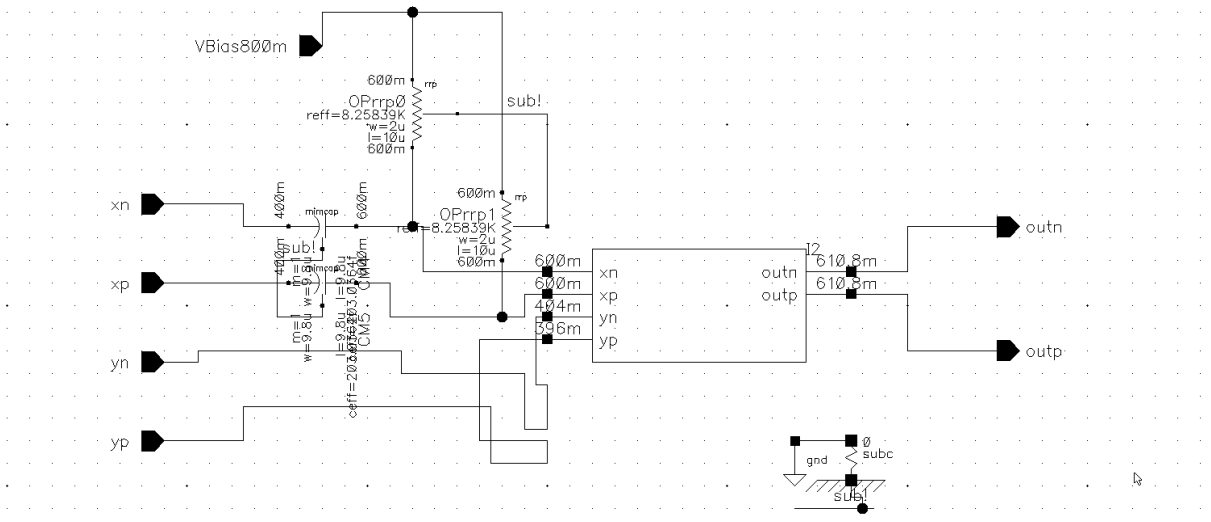


Figure E.12: Complex Multiplier - first level - AC Coupling

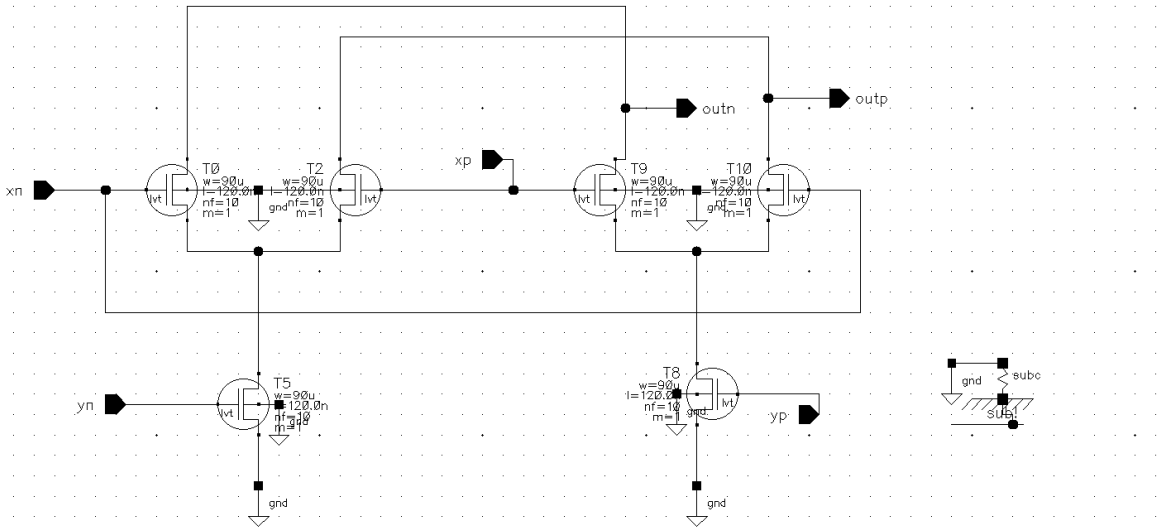


Figure E.13: Complex Multiplier - Transistor Level

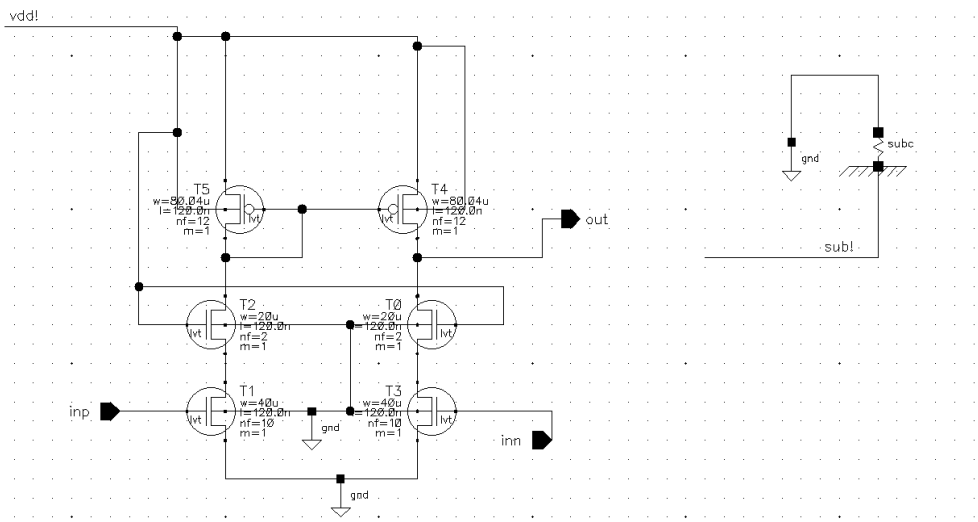


Figure E.14: Differential to Single-Ended Amplifier

E.8 Phase Equalizer

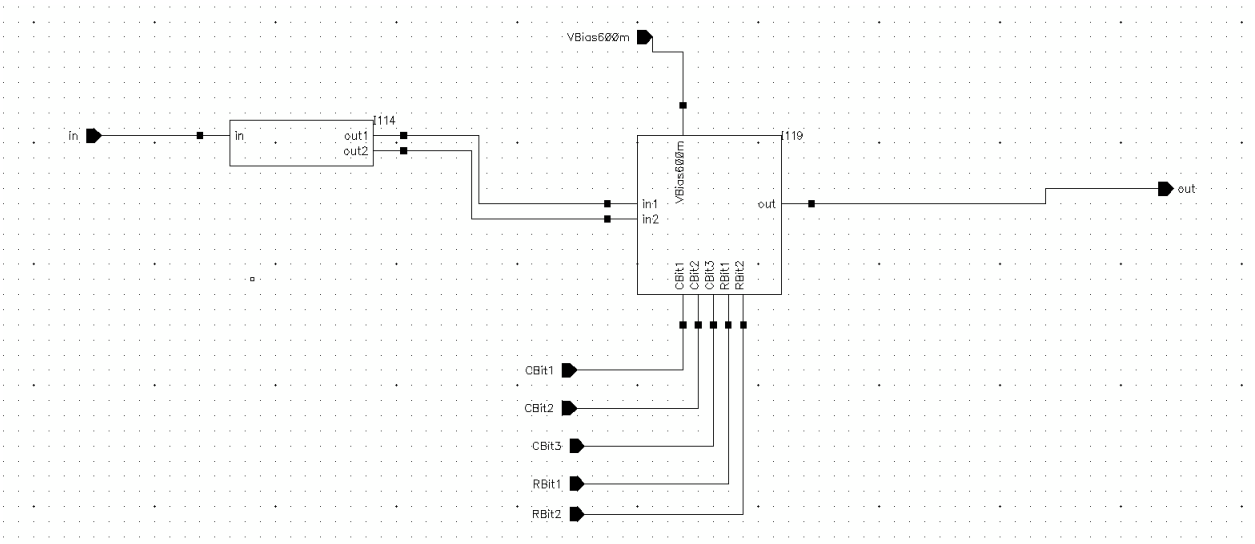


Figure E.15: Phase Equalizer - TOP Level

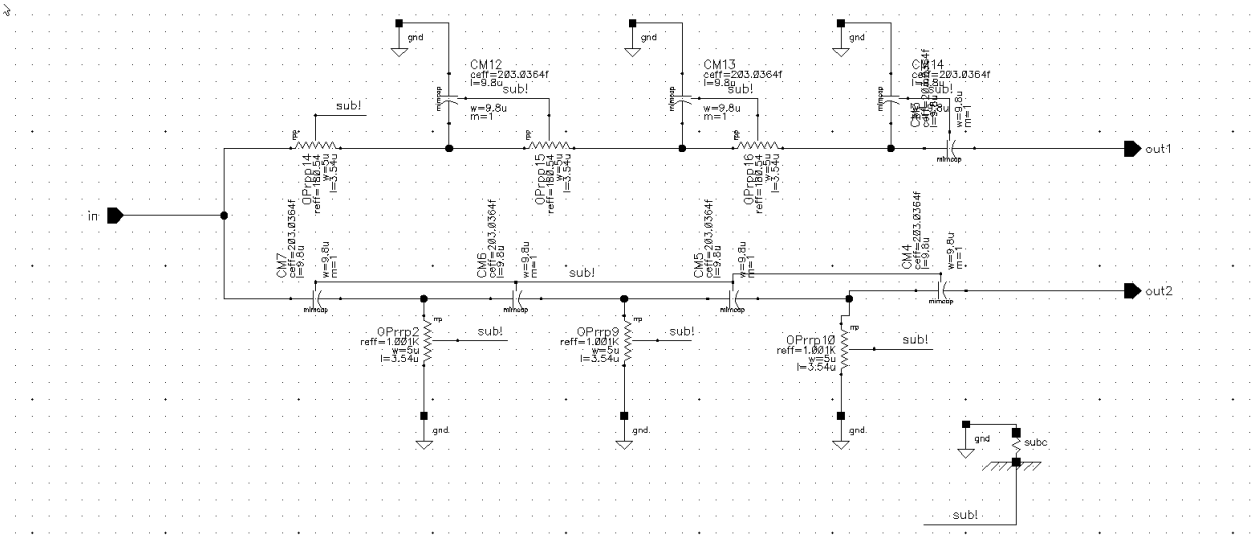


Figure E.16: Phase Equalizer - First Level - Passive Filter

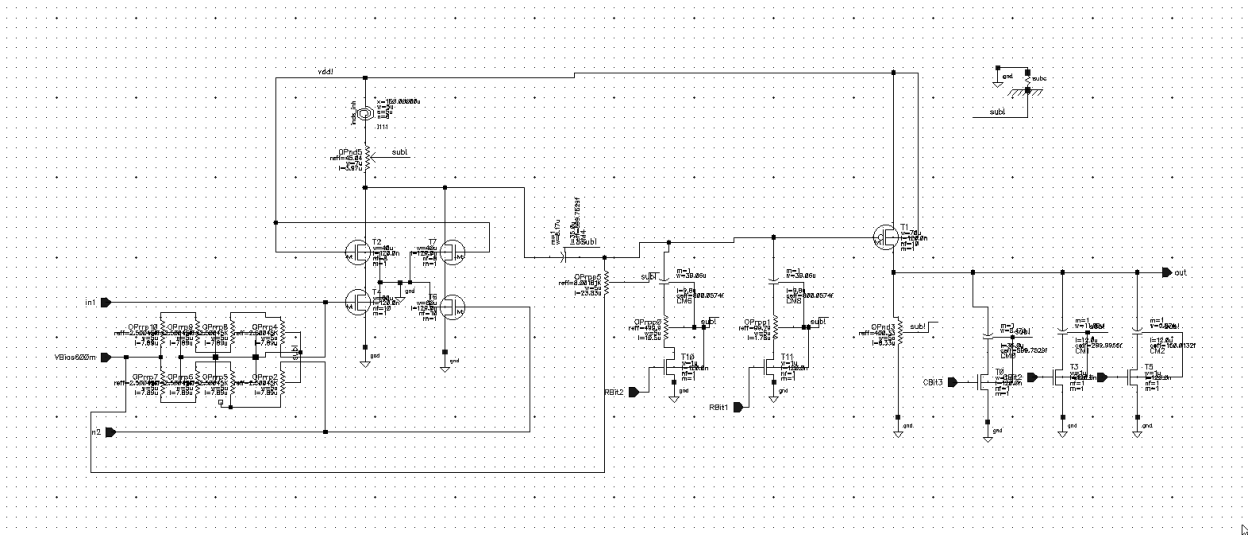


Figure E.17: Phase Equalizer - First Level - Differential Amplifier with Common Collector Stage

E.9 Buffer

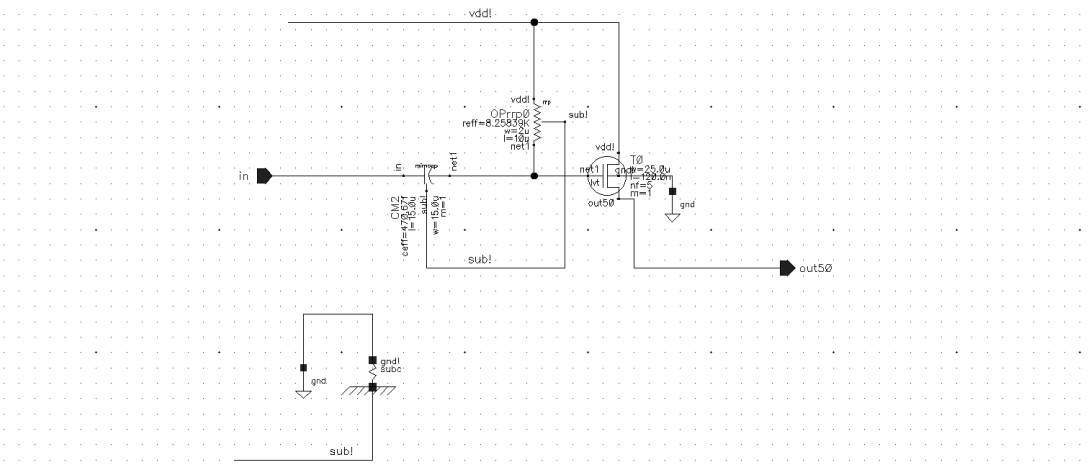


Figure E.18: Output Buffer Schematic

E.10 Biasing

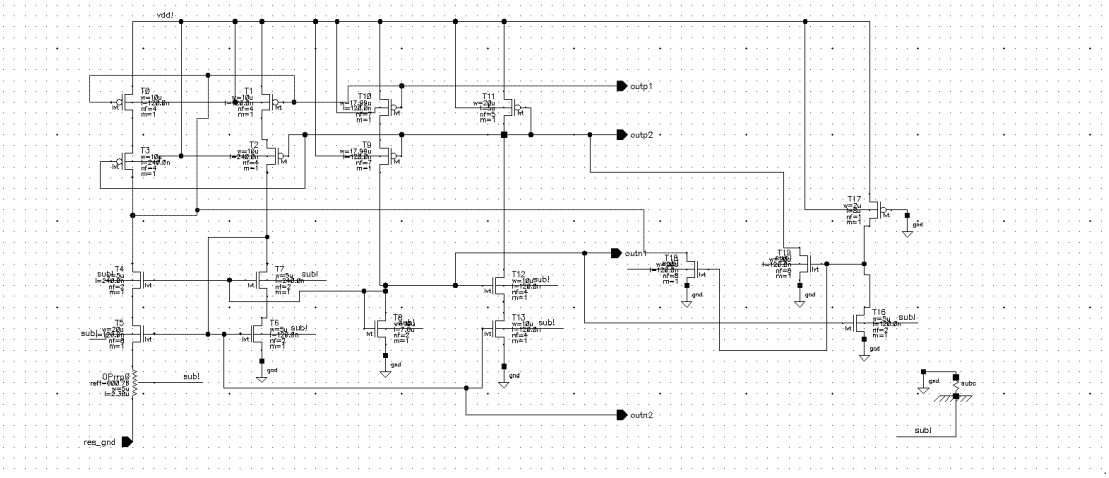


Figure E.19: Bias Circuit Schematic

E.11 Digital Circuits

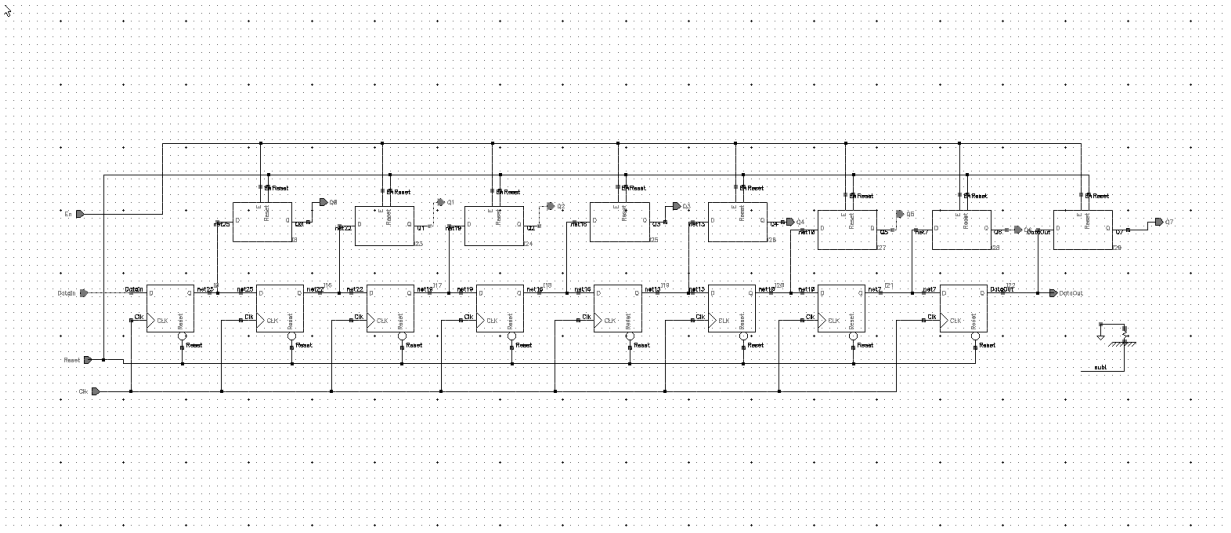


Figure E.20: Shift Register - TOP Level Schematic

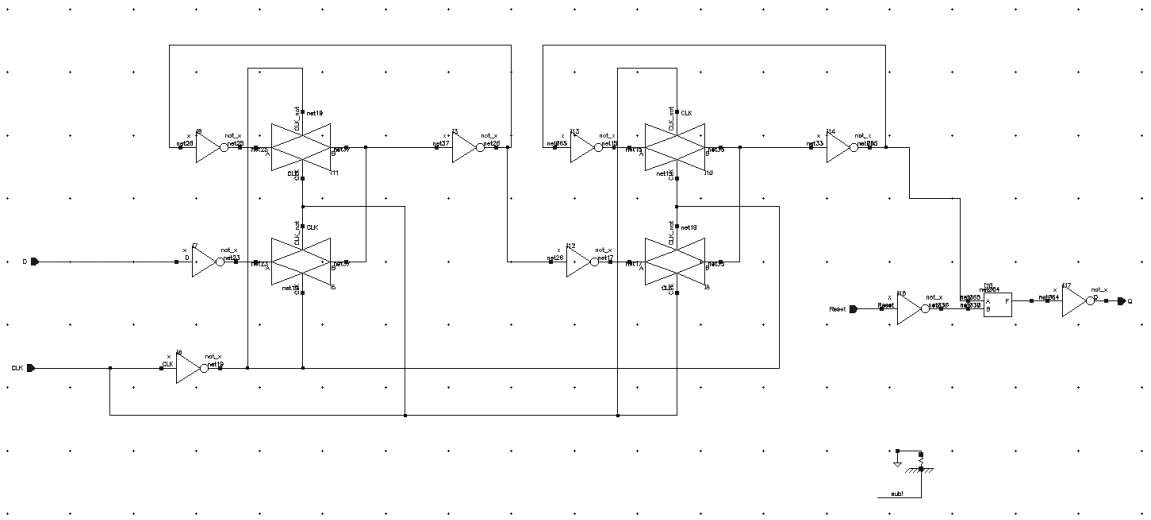


Figure E.21: D-Flip Flop Schematic

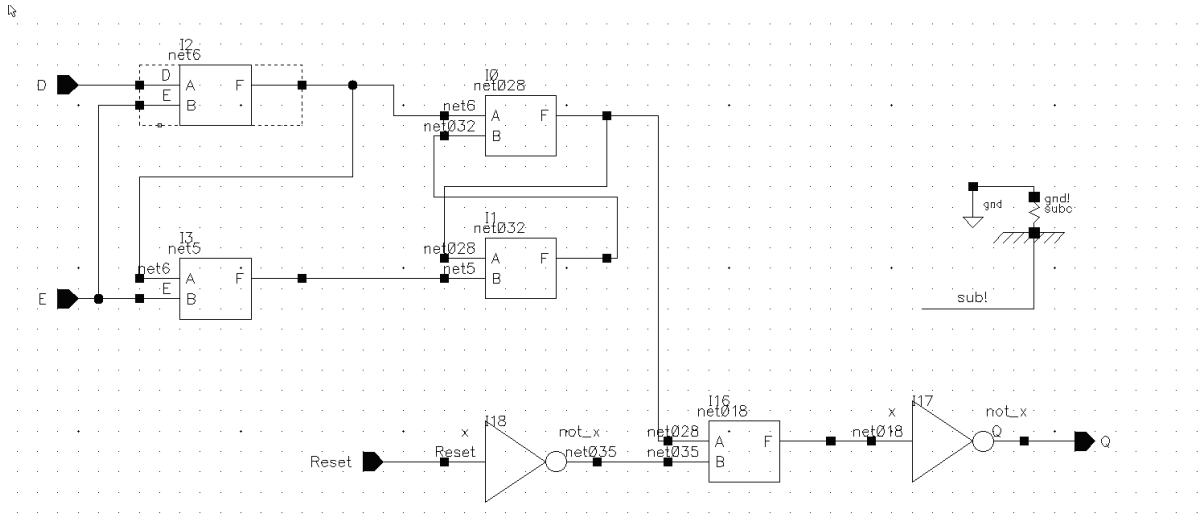


Figure E.22: D-Latch Schematic

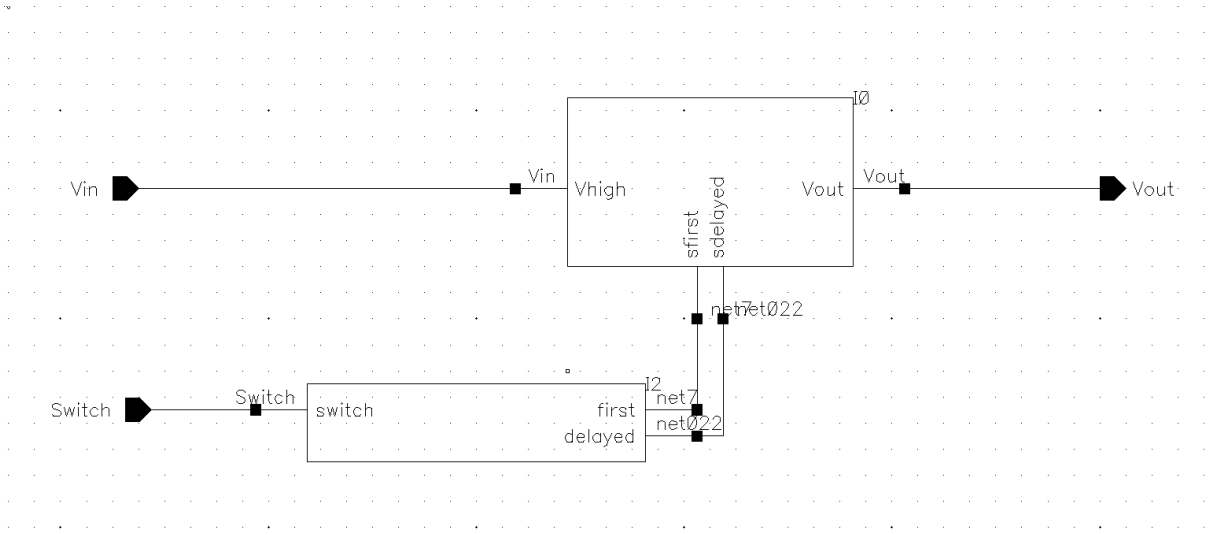


Figure E.23: Double Switch - TOP Level

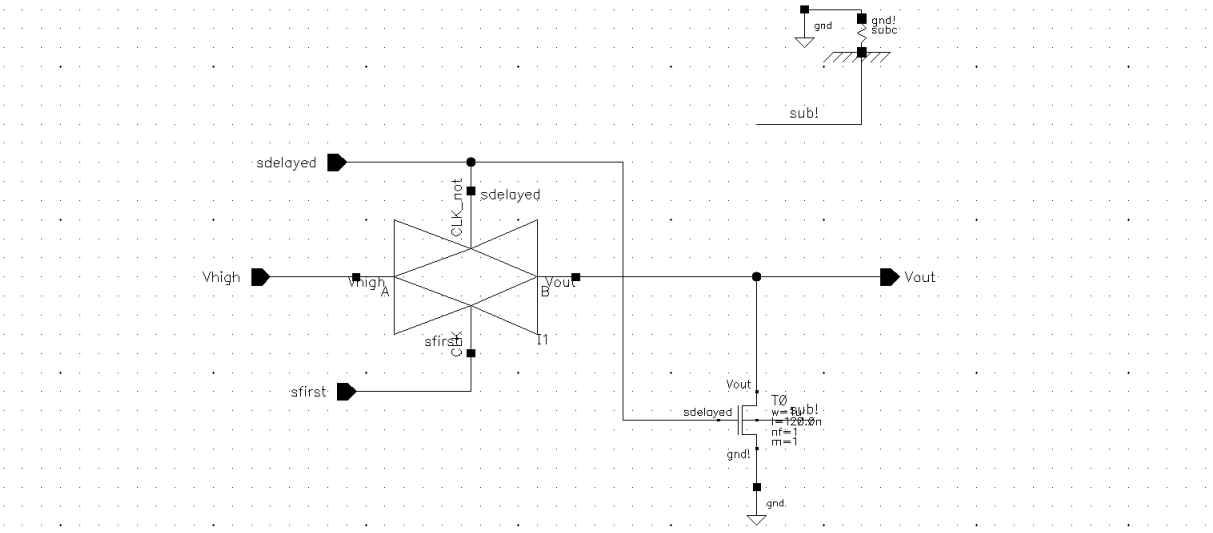


Figure E.24: Double Switch - Transistor Level

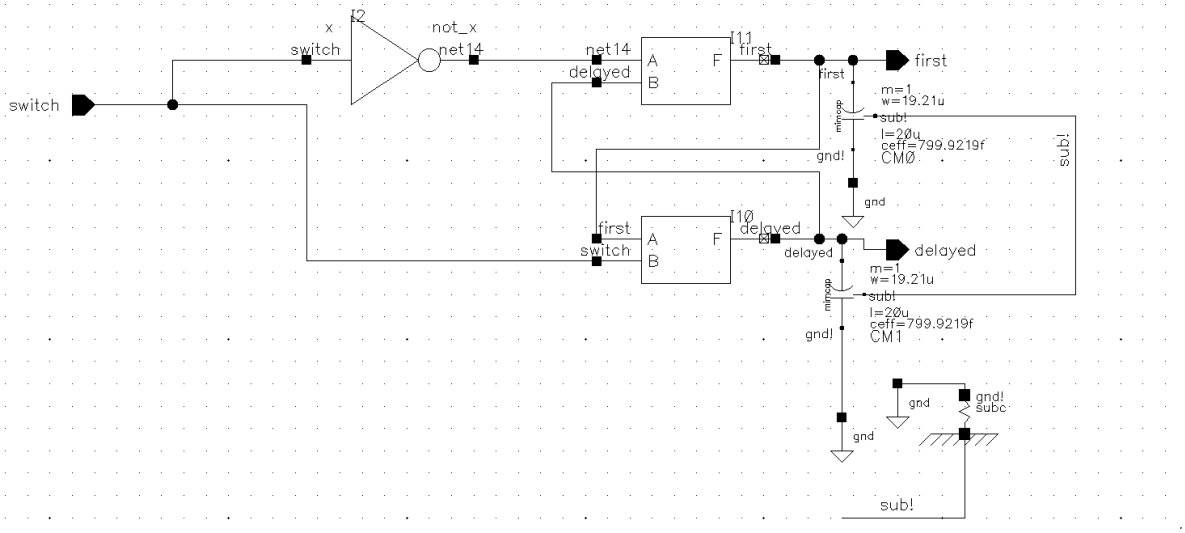


Figure E.25: Generating Non-Overlapping Clocks Circuit

Appendix F

Circuit Layout

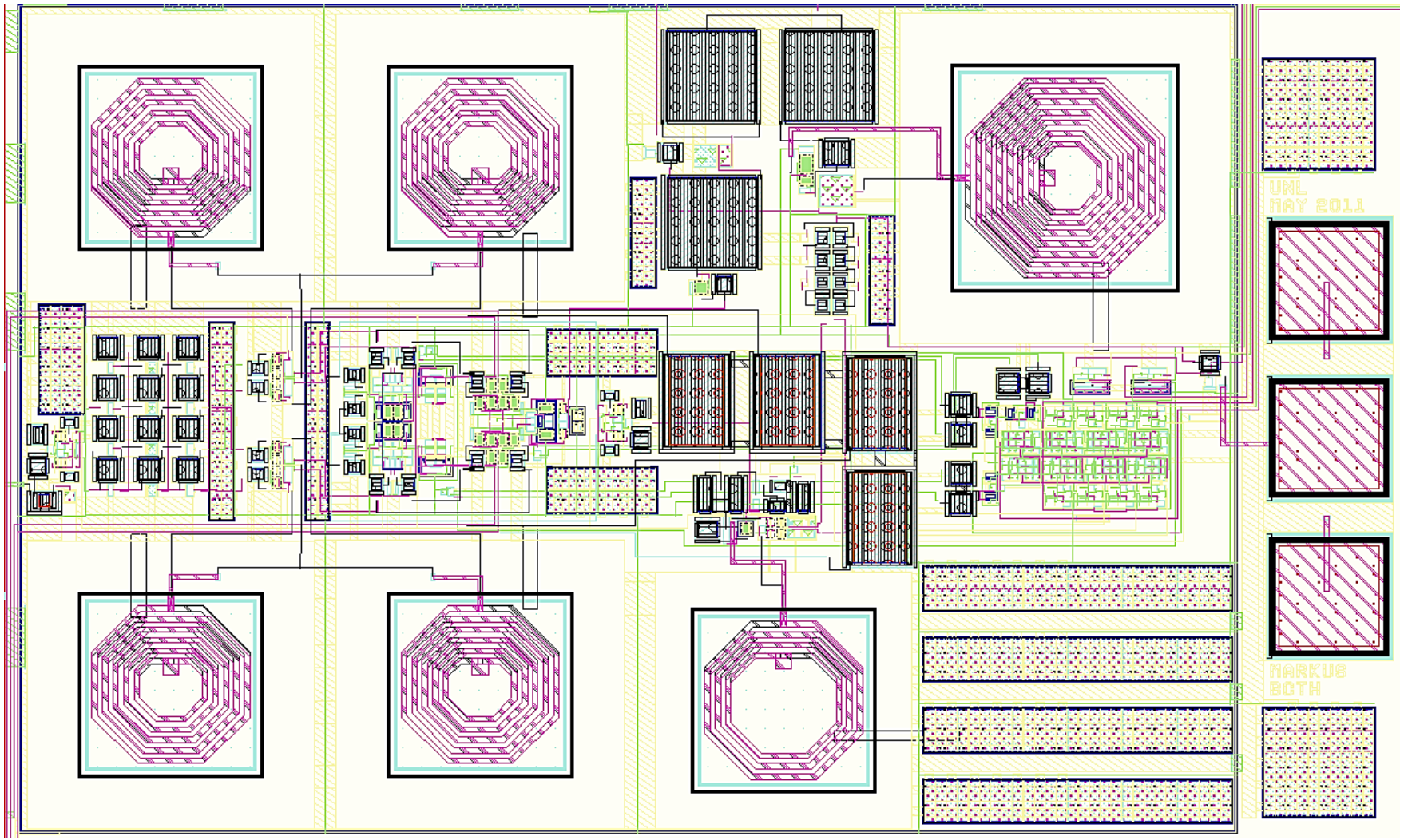


Figure F.1: Chip Layout - No Bondpads

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