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ENERGY STORAGE AND MANAGEMENT FOR A SMALL SERIES PLUG-IN HYBRID ELECTRIC VEHICLE

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By

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ENERGY STORAGE AND MANAGEMENT FOR A SMALL SERIES PLUG-IN HYBRID ELECTRIC VEHICLE

Liqin Ni, Ph.D.

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Advisors: Dean J. Patterson and Jerry L. Hudgins

Plug-in hybrid electric vehicles (PHEVs) are gaining increasing interest for both residential and commercial transportation applications. In PHEV design, energy storage system (EES) is a critical component which will impact the overall design efficiency, performance, cost and etc. This dissertation aims to design an advanced energy storage system for a small plug-in hybrid electric vehicle, whose performance will approach very closely to the optimal possible, in terms of energy efficiency and acceleration, for passenger road vehicles application. Moreover, practical automotive requirements are considered during ESS design, such as cost, life time, safety and volume.

This dissertation utilizes ultracapacitors in conjunction with Lithium-ion batteries to combine the power performance ability of the former with the greater energy storage capability of the latter. This combination can improve vehicle performance, battery life time and safety issue with appropriate design. This dissertation describes the entire ESS design, from energy storage size optimization (determination of power and capacity), multi-source control strategy, to associated power electronics design and testing.

An economical 16-phase interleaved bidirectional DC/DC converter connected between ultracapacitors and batteries, is presented featuring smaller input/output filters,

faster dynamic response and lower device stress advantages, which are highly preferable in high power applications. Discontinuous conduction mode (DCM) methodology is applied in the proposed converter to reduce imbalance current between phases so that the current control loop in each phase can be removed. The high current ripples associated with DCM operation are then alleviated by interleaving. The design, construction and testing of hardware prototype are presented with experimental results. Moreover, a novel ZVS/ZCS soft switch is proposed for the DC/DC converter based on DCM operation to improve efficiency, reduce spike voltage between MOSFET, and reduce Electromagnetic Interference (EMI). Both simulation model and experiment circuit have been built for one stage DC/DC converter to verify the proposed method.

In addition, a battery charger for residential application with power factor correction (PFC) capability is designed. A single stage of boost converter is proposed to achieve both PFC and battery charging control simultaneously. A modified charger system is proposed by utilizing ultracapacitor combined with bidirectional DC/DC converter, to remove large filtering capacitor requirement in traditional charger system, due to the fact that the power absorbed from the single phase AC supply has a large 120 Hz component.

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INTRODUCTION

1.1 Background

The automotive industry has prompted the progress of the world's economy and brought the convenience of human life. Every year, tens of millions of vehicles are sold all around the world. However, most of automobiles using internal combustion engine (ICE) have caused and continuously cause serious problems, such as air pollution, global warming, and the rapid depletion of the Earth's petroleum resources. According to [1] , transportation emissions is the second largest source of greenhouse gas emissions in U.S. and global temperature has increased on average 0.6 degree C in last 50 years [2]. The rate of oil discovery has been falling since 1981 that will lead to falling in production and increasing in oil price [3]. The recent crude oil price fall is merely the impacting of economic crisis, but eventually will continue to growth. Therefore, people began to reduce dependence on oil and emphasize on the development of higher efficiency and cleaner transportation vehicles. Electric vehicles (EV), hybrid electric vehicles (HEV), and fuel cell vehicles are the three typical vehicles that are proposed to replace conventional vehicles with ICE in the near future [4] [5].

It is believed that the electric vehicles will eventually replace the conventional vehicles [6]. However, currently, the performance is far behind the requirement because of poor energy storage capability of batteries [7]. Thus, in recent years, advanced vehicle technology research has been turned to focus on HEV or plug-in HEV (PHEV) [8][9]. In

last decade, HEV has been commercialized, such as Toyota Prius, Honda Insight and Civic Hybrid. In order to further reduce vehicles' dependence on oil and provide lower-emission or zero-emission, plug-in HEV has been widely studied.

This project covered in this dissertation is proposed to develop a small series plug-in HEV for city driving with 20 miles range on electric power alone. Since the typical daily driving distance is between 10-30 miles [10], a 20 miles range plug-in HEV would allow most people consume no gasoline while use the vehicle for urban driving. Recharging would be accomplished by plugging their car batteries into an electric outlet at night. This practice would not only reduce consumers' dependency and cost on oil, but also significantly reduce the vehicle emissions. The original vehicle emission from oil is transferred to the electric power plants which typically have higher efficiency, or even eliminated if renewable energy resources. For those whose daily driving distance are farther than 20 miles and have to use additional gasoline in their cars, the technology of PHEV will also have less fuel cost.

1.2 HEV Classifications by Drive train Architectures

One of the most common ways to classify HEV is based on configuration of vehicle drive train. There are mainly three architectures used in current hybrid vehicle market: series, parallel and series-parallel [11][12].

1.2.1 Series Hybrid System

One of the basic types of HEV is series hybrid. In this configuration, as shown in Figure 1.1, the vehicle is driven by electric motor, which is powered by energy storage system (ESS) or generator or both of them. A small internal combustion engine is turned

on intermittently to generate electric power. During braking regeneration, the electric motor operates as generator to absorb braking power and recharge energy storage system. For plug-in HEV, the energy storage system can be recharged not only from the generator but also from the electric utility grid.

One advantage of series hybrid architecture is that the control system is relatively simple due to the lack of a mechanical link between the combustion engine and the wheels. The combustion engine runs at a constant speed and torque at its peak efficiency point, even when the speed of car changes. During the stop-and-go type city driving, series hybrids are relatively the most efficient. Another advantage is that series hybrid operation is very similar with electric vehicle.

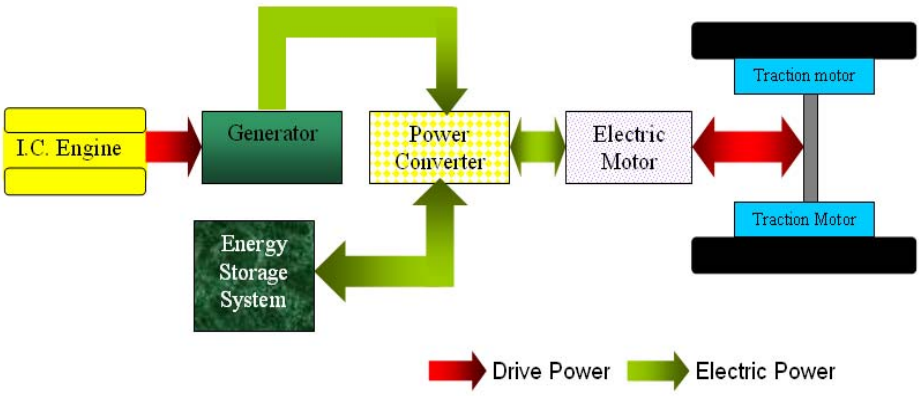


Figure 1.1 Series hybrid system configuration

1.2.2 Parallel Hybrid System

In parallel configurations, shown in Figure 1.2, both the engine and the motor provide traction power to the wheels, which means that the hybrid power is summed at a mechanical node to power the vehicle. In this system, the motor is powered by the battery to drive the wheels, and is also used as a generator to recharge the battery. Consequently, the motor cannot be used to generate electricity while the car is running. The parallel

hybrid vehicles usually use the same gearboxes of the counterpart conventional vehicles, either in automatic or manual transmissions. The control of parallel hybrid system is more complex than that of a series hybrid system, due to the mechanical coupling between the engine and the driven wheels.

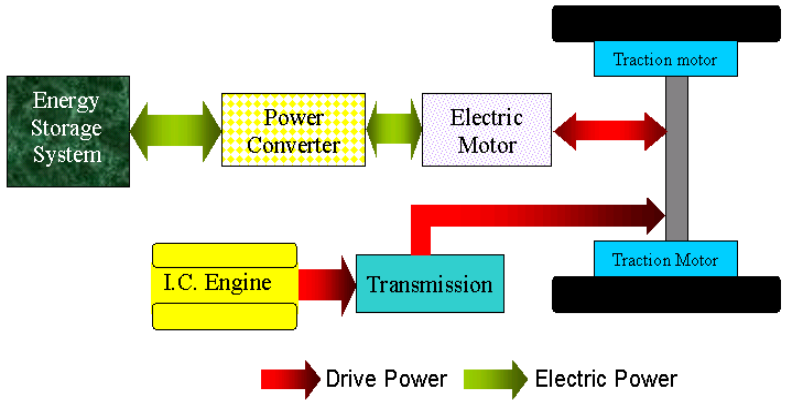


Figure 1.2 Parallel hybrid system configuration

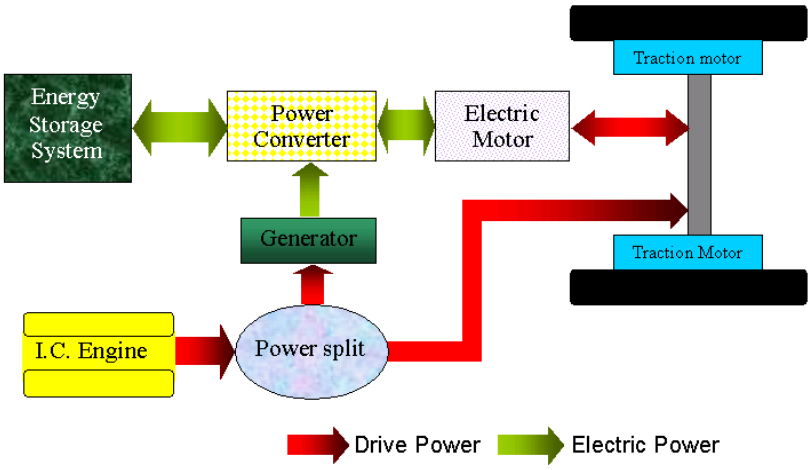


Figure 1.3 Series-parallel hybrid system configuration

1.2.3 Series-Parallel Hybrid System

In the series-parallel configurations, shown in Figure 1.3, the vehicles have features of both series and parallel hybrids. This design depends on the presence of two motors/generators and the connections between them, which can be both electrical and mechanical. The connections between the engine and electric machines are usually accomplished by planetary gears known as power-splitting devices. The main principle behind this system is the decoupling of the power supplied by the gas/petrol engine from the power demanded by the driver. The battery is charged by regenerative braking or with surplus power generated by gas/petrol engine. It takes advantage of the energy-efficient electric motors when the car runs in the low speed range, and calls on the gas/petrol engine when the car runs in the higher speed range. Toyota Prius is using this type configuration.

1.3 Energy Storage System and Power Electronics Requirements

Energy storage technologies, especially batteries, are critical enabling technologies for the development of hybrid vehicles or pure electric vehicles. Recently, the batteries widely used for vehicle mainly include three types: Lead Acid, Nickel-Metal Hydride and Lithium-ion. In fact, most of hybrid vehicles in the market currently use Nickel-Metal-Hydride due to high voltage requirement in its battery system. Lithium-ion batteries are expected to be the battery chemistry of choice for hybrid vehicle or even electric vehicles because they have relatively lighter weight and higher energy density. However, there are still many technical barriers which have to be overcome before the batteries are widely used. These barriers include cost, performance, life, and durability [13][14][26].

Ultracapacitors, like batteries, are energy storage devices and store charges electrostatically. Ultracapacitor can provide a very high power, rapidly charged and discharge, long life time and maintenance free [15][16]. Ultracapacitors can be the primary energy source during acceleration and hill climbing, as well as regenerating braking energy. Using of ultracapacitor in conjunction with a battery combines the power performance of the former with the greater energy storage capability of the latter. This combination can extend the life of the battery, reduce the size of battery, and improve the performance of vehicle since ultracapacitor can provide high peak power whenever necessary [18]. The ultracapacitor can capture and store large amounts of electrical energy during braking in short time and release it fast during the next acceleration. Thus, the ultracapacitor can greatly improve fuel efficiency under stop-and-go urban driving conditions. However, the combination of ultracapacitors and batteries requires additional power electronics, such as a bidirectional DC/DC converter [18][19][20]. The additional cost and weight of ultracapacitor and power electronics may be justified by the downsized battery and the IC engine, and improved the battery life time. Meanwhile, the cost of ultracapacitors has been decreasing markedly over the last few years [21][22]. In addition, not only hybrid vehicle, many other applications can benefit from ultracapacitors [23][24][25].

The power electronics and electric drive system are the technology foundation for hybrid electric vehicles and electric vehicles. It is necessary to develop the power electronics research to support and promote the design, development, and demonstration of power electronic components and systems that will overcome major technical barriers to the commercialization of hybrid electric vehicle technologies [26]. The main

components of power electronics in hybrid vehicles include DC/DC converters, AC/DC rectifier, the motor controller and inverters that condition the electrical signal between the power generation unit (ultracapacitor or battery) and the electric motor to provide power to various components.

The power electronics requirements for energy storage system include: 1). Bidirectional DC/DC converters to boost battery pack voltage to high voltage bus or boost/buck between different energy storage devices (such as between ultracapacitor and battery); 2) the battery charger with special charging strategy and power factor correction (PFC) capability, in order to recharge the battery from power grid; 3) battery management system for battery pack; 4) circuit protection.

The selection of power semiconductor devices, control and switching strategies, the packaging of the individual units, and the system integration are also very crucial to the development of efficient and high performance energy storage system. The Electromagnetic Interference (EMI) filters needs to be considered due to the switching of the devices. Soft switch techniques could be applied if necessary to lower switching losses and lower EMI [27].

1.4 Project Overview

This dissertation aims to design an advanced energy storage system for a small plug-in hybrid electric vehicle whose performance will approach very closely to the optimal possible, in terms of energy efficiency, for passenger road vehicles. The efficiency will be higher that of currently commercially available hybrid vehicles, whose structure has been customized to be accepted in the larger market place. This dissertation will adopt

the series hybrid system due to its simple control system and high efficiency in the urban drive condition.

Following is the outline of this dissertation:

Chapter 2 describes different types of energy storage device and selection of two types energy storage device (dual-source energy storage system) for this dissertation. A simulation model is built to determine the size of energy storage including the capacity (kWh) for a 20 miles range on PHEV and the peak power during urban driving.

Chapter 3 describes the power train among different energy sources for the series plug-in HEV, especially the power flow control strategy between the battery and the ultracapacitor in energy storage system. A simulation based on MATLAB Simulink is built to validate the power train control strategy.

Chapter 4 describes a 45 kW power rating bidirectional DC/DC converter between the battery pack and the ultracapacitor pack. The interleaving technique is adopted for this converter to reduce the input/output current ripple and decrease device stress. A 16-phase interleaved bidirectional DC/DC converter based on discontinuous conduction mode (DCM) is proposed. The design, construction and testing of the hardware prototype are presented, and the experimental results are included.

Chapter 5 proposes a novel ZVS/ZCS soft switch for DC/DC converter based on DCM operation to improve efficiency and decrease EMI.

Chapter 6 describes the charger design for battery pack from power grid. Two types of charger design are proposed and simulated. One uses a large output capacitor and the other utilizes ultracapacitor and the dc/dc converter described at Chapter 4 as capacitance filter which removes the requirement of large output capacitors.

Chapter 7 concludes the dissertation and provides a discussion of future work.

Chapter 2.

ENERGY STORAGE SYSTEM FOR HEV

2.1 Introduction

The focus of HEV design is mostly on energy storage system (ESS) which is closely related with their performance, fuel economy, cost, safety, weight and volume. There are different energy storage devices available for HEV in current market, such as Nickel Metal Hydride (NiMH) batteries, Lithium-ion batteries and ultracapacitors. The size of the ESS is determined to provide sufficient energy storage capacity (kWh) and adequate peak power (kW) ability. Too large capacity and high peak power will increase the cost, volume and complexity of the control system, while too small capacity and low peak power will decrease the performance of the vehicle and the operating range on electrical power alone in plug-in HEV. This requirement can be obtained once the vehicle is specified and the performance target is established. However, it is a challenging to find an optimal ESS design that would satisfy the special characteristics. In addition, the life cycle and hardware cost have to be appropriately considered.

2.2 Energy Storages Technologies

Currently, energy storage devices mainly include chemical batteries, flywheels, ultracapacitors and fuel cells. Figure 2.1 shows the energy density and power density of most widely used energy storage devices [28]. ESS can use one or more types of energy storage devices. Most hybrid vehicles choose battery as energy storage system, some of

them choose a combination of battery with ultracapacitor since battery has high energy density and ultracapacitor has high power density characteristics. At present, there are three types of batteries that are widely used: lead acid (L-A), Ni-MH, and Lithium-ion (Li-ion). With the differences of battery chemistry, there are tradeoffs between energy density and power density. Different types of energy storage device have different advantages and disadvantages.

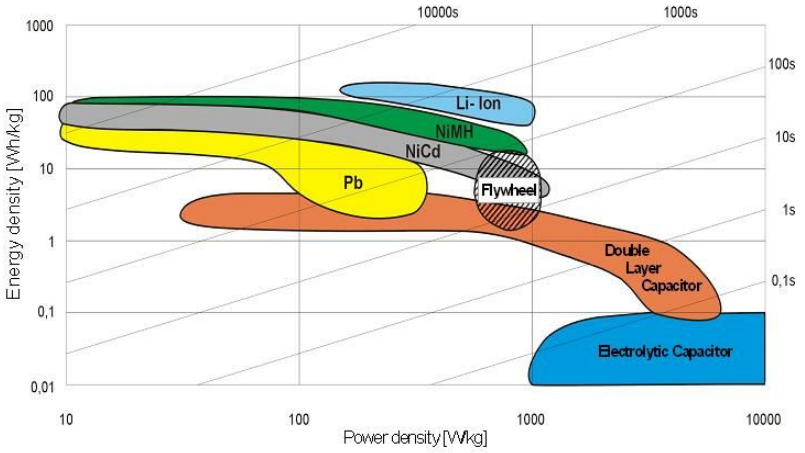


Figure 2.1 Energy density vs power density of different energy-storage devices

2.2.1 Lead Acid

Lead acid batteries are the most prevalent batteries used for vehicle starting and other ancillary power functions. They have advantages of low cost per watt-hour, robust, durable, low self-discharge rate, and no memory effect characteristics. The drawbacks of the lead acid battery include low power and energy densities, and potential environmental impact, where the lead electrodes and electrolyte can cause environmental harm if not disposed properly at a recycling facility [30].

2.2.2 Nickel Metal Hydride Battery (Ni-MH)

The Ni-MH has been on the market since 1992. Its characteristics are similar to those of the nickel/cadmium battery. The Ni-MH battery is the most widely used battery in commercial hybrid vehicle. The Ni-MH battery has a higher energy density than a Lead acid battery. It is also relatively environmentally friendly, has good endurance against misuse, and more maturity technology than Li-Ion. The disadvantages of Ni-MH include high self-discharge, memory effect and low recharging energy efficiency. Ni-MH battery pack has higher cost than a lead acid battery pack and lower power and energy density than lithium-ion battery pack.

2.2.3 Lithium Ion Battery

Lithium ion is the most potential battery type used as energy storage in hybrid vehicle due to high power and energy density. It also has advantages of no memory effect, low self-discharge and high recharging energy efficiency. Lithium-ion batteries can be formed into a wide variety of shapes and sizes, thus, they can efficiently fill the limited space of the devices that they power for. The major concerns of using Li-ion battery on a hybrid vehicle are the over-heating problem during recharging, safety and high cost.

2.2.4 Ultracapacitor

Ultracapacitors are electrochemical capacitors that have an extremely high energy density compared to common capacitors. Energy is storied in the double layer formed at a solid/electrolyte interface [29]. Advances in new materials and new ultracapacitor designs have considerably improved the energy storage capability and cost of this emerging electrical energy storage device. The advantages of ultracapacitor include long

life, high output power, reliable and very high rates of charge and discharge. The disadvantage is high cost. The ultracapacitor generally used in combination with the battery as energy storage in HEV. The ultracapacitor devices are commercially available from several companies, including Maxwell, Ness, and EPCOS. The capacitance of their products, range from 1000-5000 F.

2.3 Size and Types of Energy Storage Devices

The size of the ESS is determined to provide sufficient energy storage capacity (kWh) and adequate peak power (kW) ability, which is related with vehicle performance and cost. The cost of energy storage system is still very high; therefore it is a major obstacle for plug-in HEV to be viable. Thus, it is vital important to estimate energy storage size to make reasonable choice for energy storage devices. Generally, the estimation can be obtained once the vehicle is specified and the performance target is established.

In order to determine the size of energy storage system, a simulation model is built to simulate the battery state of charge (SOC) and the battery output power during the pure electric power drive with a given driving condition. This model will consider rolling resistance, aerodynamic drag, grading resistance (or potential energy charge with altitude), regeneration braking, system energy loss, and the battery efficiency.

This simulation is based on practical urban driving test around Lincoln city, Nebraska. The total distance of the test route is 18.2 miles, and total time is 2980 s. From the driving test, the vehicle speed data and roads longitude and latitude data are obtained. These data are measured by a Global Position System device (Delorme Tripmate GPS

Navigation). This simulation model also considers the potential energy changes with altitude. The altitude data is acquired by checking topographic map according to measured longitude and latitude. Current hybrid vehicles, in the urban driving condition, do not have adequate storage for the often much larger potential energy changes with altitude, which are quite noticeable even in cities such as Lincoln, significant in hilly cities such as San Francisco, and dominate in mountainous areas.

2.3.1 Simulation Model

Most roads have a non-zero gradient. While the vehicle is moving, there is resistance that tries to block its movement. The resistance usually includes tire rolling resistance F_{roll}, aerodynamic drag F_{aero}, and uphill resistance F_g (which becomes an impetus during downhill), as shown in Figure 2.2. The tractive effort, F_{tot}, is produced by the battery energy and is transferred through the transmission and final drive to the wheels. The tractive effort is required to overcome the resistance effort and to accelerate the vehicle. In the longitudinal direction, the dynamic equation of vehicle motion can be described by the following relation:

$$F_{tot} = F_{roll} + F_{aero} + F_g + F_{acc} \tag{2-1}$$

According to [30], equation (2-1) can be expressed as:

$$F_{tot} = Pf_r \cos a + \frac{1}{2}\rho A_f C_D (V + V_w)^2 + m_v g \sin a + m_v \frac{dV}{dt} \tag{2-2}$$

P is the normal load, acting on the center of the rolling wheel. In here, $P = m_v$g.

f_r is the rolling resistance coefficient.

α is the road angle (refer to Figure 2.2).

ρ is air density, 1.202 kg/m^3.

A_f is vehicle frontal area.

C_D is the aerodynamic drag coefficient.

V is the vehicle speed.

V_w is the wind speed in the vehicle's moving direction.

m_v is the mass of vehicle.

g is acceleration of gravity.

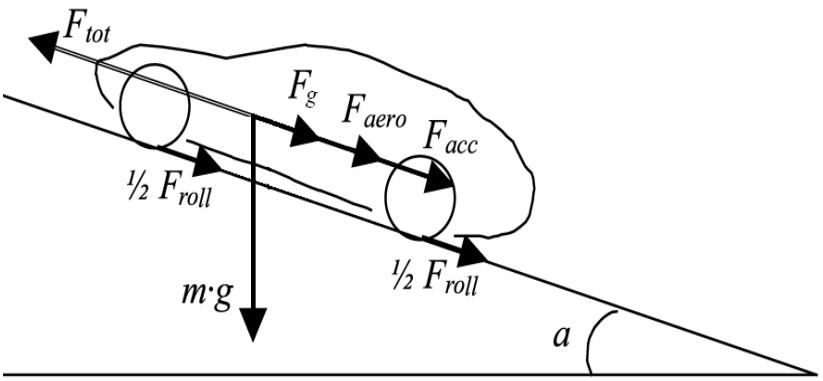


Figure 2.2 Forces acting on the vehicle

$\frac{dV}{dt}$ is the acceleration of the vehicle.

According to Mechanical power definition and equation (2-2), the total tractive energy J_{tot} and demand power P_{demand} can be expressed as:

$$J_{tot} = F_{tot}s = (Pf_r \cos a + \frac{1}{2}\rho A_f C_D (V + V_w)^2 + m_v g \sin a + m_v \frac{dV}{dt})s \quad (2\text{-}3)$$

$$P_{demand} = F_{tot}V = (Pf_r \cos a + \frac{1}{2}\rho A_f C_D (V + V_w)^2 + m_v g \sin a + m_v \frac{dV}{dt})V \quad (2\text{-}4)$$

where s is the driving distance of the vehicle and V is the vehicle speed.

It is assumed that the energy loss from the battery due to vehicular energy management is J_{loss} and the battery discharge/charge efficiency is η_d/η_c. The battery energy $J_{battery}$ during discharge and charge can be expressed, respectively, as:

$$J_{battery} = (J_{tot} + J_{loss}) / \eta_d \tag{2-5}$$

$$J_{battery} = (J_{tot} + J_{loss})\eta_g \eta_c \tag{2-6}$$

And the battery output power $P_{battery}$ can be expressed as:

$$P_{battery} = \frac{dJ_{battery}}{dt} = \frac{\Delta J_{battery}}{\Delta t} \tag{2-7}$$

Where η_g is the regeneration efficiency and t is the vehicle drive time.

2.3.2 Initialization of Simulation

According to the simulation model, the vehicle parameters need to be initialized, such as C_D, m_v and A_f, energy losses, vehicle speed and the road gradients. Relevant vehicle technical parameters for this simulation are listed in Table 2-1 [31][32], which is taken from the specifications for the 2004 Toyota Prius. However, the energy storage parameters are different with the Toyota Prius, as shown in Table 2-2. There are two simulations, one is based on Lithium ion batteries, and another is based on NiMH. The simulation results are then compared.

Table 2-1 Toyota 2004 Prius specifications

Mass m_v (lb)	Wheel dia. (inch)	f_r	C_D	A_f (m^2)
2890	15	0.008	0.26	2.16

Table 2-2 Energy storage specifications for the simulation

Battery	Wh/kg	Useable SOC	η_d	η_c
Lithium Ion	143	~70%	0.95	0.95
NiMH	46	~40%	0.84	0.84

Energy loss J_{loss} includes electric circuit losses and hybrid drive system losses. The electric circuit losses are assumed to be 5%. The hybrid drive system losses include gear losses, motor-rotor losses, and other gear losses. According to [33], the hybrid drive system losses in 2004 Toyota Prius vehicle are related to the motor shaft speed, as shown in Figure 2.3.

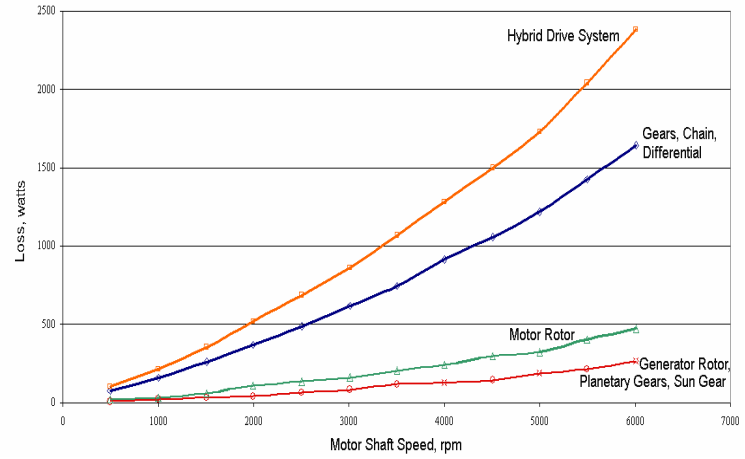


Figure 2.3 Hybrid electric drive system losses at different motor shaft speeds

During simulation, road features and vehicle speeds are the two main dominating factors. *Road features* are the geographic properties of the road, such as up-hill grades and down-hill grades. *Vehicle speeds* contains stops (velocity of zero), acceleration, constant speed, and braking or deceleration. Both road features and vehicle speeds were

initially treated as random variables, but are determined by the regions where the vehicles are running, and traffic situations.

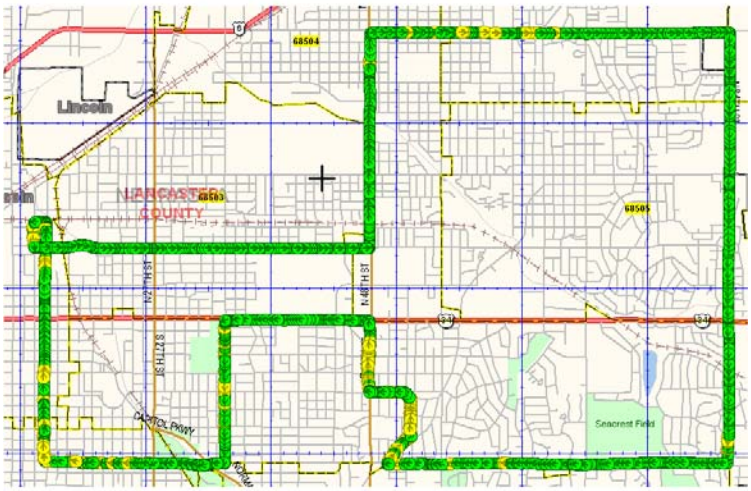


Figure 2.4 The driving test route around Lincoln urban

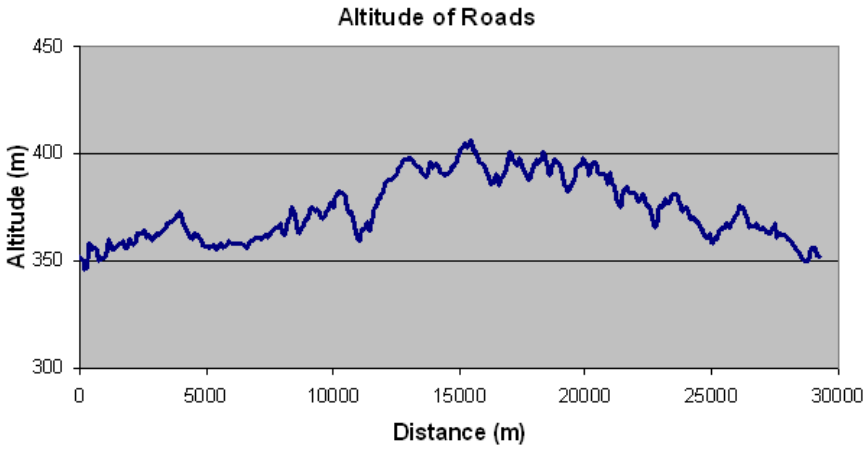


Figure 2.5 Altitude variation of road

Therefore, in order to achieve a more realistic result in the simulation, these entire road features and vehicles speeds need to be considered during the calculations. This research involved logging a driving test on a specific route around the city of Lincoln, Nebraska. The route is shown in Figure 2.4. The total distance of the test route is 18.2

miles, and total time is 2980 s. The altitude of roads is measured by topographic map according to its longitude and latitude, and the results are shown in Figure 2.5. The vehicle speed is measured by a Global Position System device, (Delorme Tripmate GPS Navigation), and results are shown in Figure 2.6. The maximum speed of vehicle is 44.2 mph (miles per hour) and average speed is 22.0 mph.

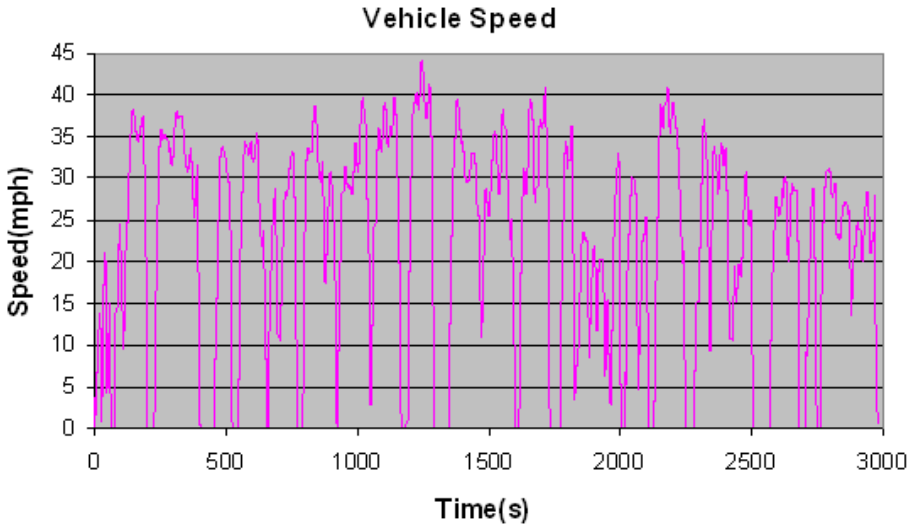


Figure 2.6 Driving speed schedule of vehicle

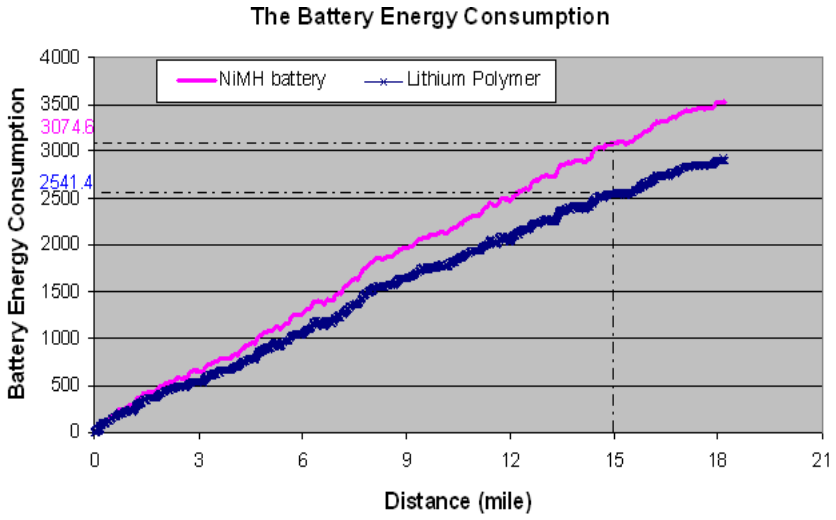


Figure 2.7 Battery energy consumption during driving

2.3.3 Result of Simulation

According to equations (2-3), (2-5), (2-6) and the test data shown in section 2.3.2, the demands on battery energy at different distances and times can be calculated, and the results are shown in Figure 2.7. The simulation results show how much battery energy is consumed at different driving distances. For example, designing an energy system with a 15 miles range on battery power alone, it needs 2.54 kWh usable energy using Lithium ion batteries, while it needs 3.07 kWh usable energy using NiMH batteries. The difference of requirement for these two type batteries is caused by different charge/discharge efficiency, shown in Table 2-2. From the simulation results, the battery transfer energy has almost linear relationship with the driving distances. For a 15 miles range on all electrical power, the useable energy and capacity requirements are shown in Table 2-3.

Table 2-3 Battery requirement for a 15 miles range

Battery Type	Useable energy (kWh)	Capacity (kWh)	Weight (kg)
NiMH	3.07	7.68	167
Li-Ion	2.54	3.63	26

Figure 2.8 is the state of charge of Lithium ion battery between 20%-90%, and NiMH battery between 40%-80%. The results show that expanding the usable SOC window drastically reduces the total battery capacity requirement, which can substantially reduce the energy storage system cost and volume. Hence, the selection of battery and battery parameters, especially the usable SOC window, are crucial and dramatically affect the ranges operating on battery power alone.

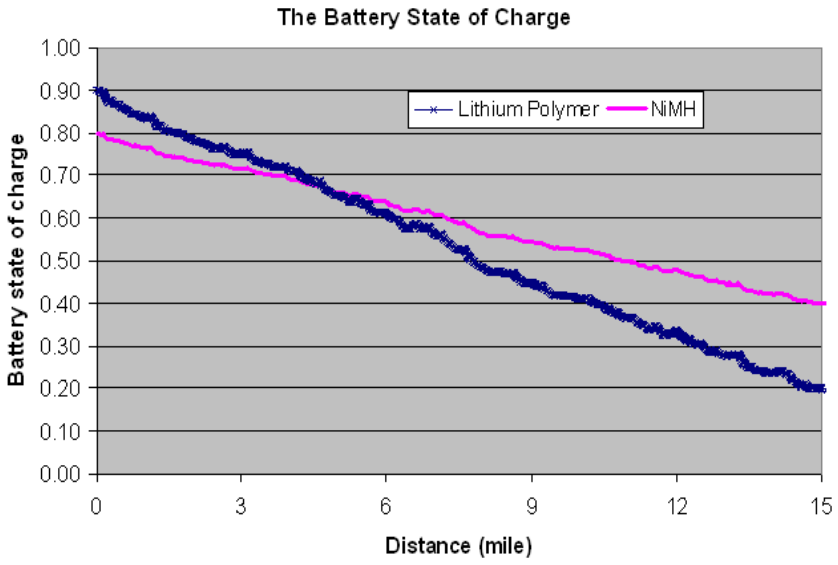


Figure 2.8 Battery SOC during drive cycle

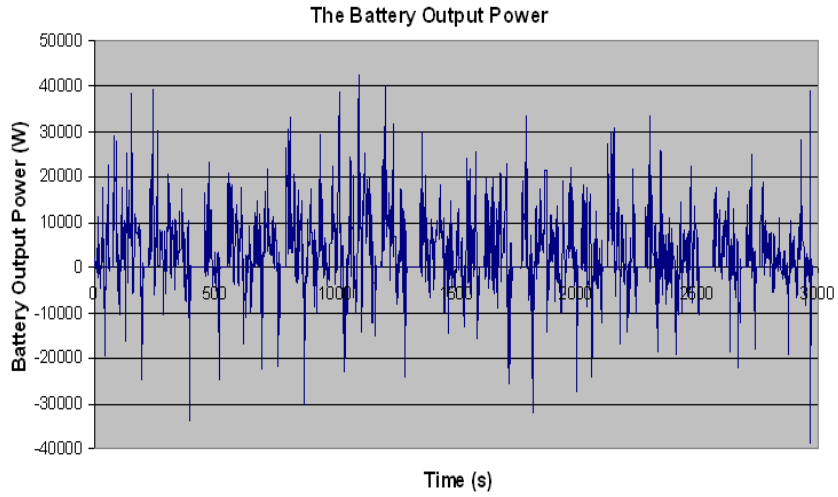


Figure 2.9 Output power of the battery along a graded road

According to equation (2-7), the battery output power can be simulated, shown in Figure 2.9. The energy storage system is chosen as a Lithium ion battery, and the road altitude profile is shown in Figure 2.5. The result shows that the peak output power is nearly 41kW. The battery power works in a broad region and change very quickly and frequently. In order to decrease the battery peak power, improve battery cycle lifetime

and reduce system cost, the ultracapacitors are applied to combine with chemical batteries in energy storage system [34][35]. The ultracapacitors are designed to provide peak power to meet high power requirement during vehicle acceleration, or absorb the peak charging power during regenerative braking.

2.4 Conclusion

According to simulation, the energy storage capacity is almost linear with driving distance. Thus, for 20 miles range plug-in HEV with Lithium ion battery pack, the energy storage capacity is 4.84 kWh. For a 1.2 factor of safety, the battery pack capacity should be around 5.8 kWh.

This project is based on modifying Toyota Prius vehicle, so the battery system should be compatible with Prius vehicle. The Prius NiMH pack nominal voltage is 201.6V, ranging from 180V to 270V during use. Therefore, this project uses 64 cells of 3.7V 25Ah of Lithium ion battery with 5.9 kWh capacity. The battery pack nominal voltage is 236.8 V and working range is from 180V to 268V.

The peak output power is more than 40 kW and the power of the electric motor in Prius vehicle is 50 kW. The battery can only provide 5.9 kWh, so the extra power will be provide by ultracapacitor.

Chapter 3.

CONTROL STRATEGY FOR DUAL-SOURCE ENERGY STORAGE SYSTEM

3.1 Introduction

Due to the existence of multiple energy sources, power train control strategy needed be developed. There are many different control strategies used for HEV in order to achieve the best performance and the highest efficiency during driving [17][18][36][37]. Reference [18] proposes a control strategy to determine both the ultracapacitor current and battery current based on load current frequency. According to [18], battery provides current with low frequency component and ultracapacitor provides extra current with high frequency component. This control strategy does not consider particular condition such as ultracapacitor energy is low and needs recharging from battery. In another strategy presented by [36], the battery is designed to provide a minimum power for a request power and any remaining required power is supplied by ultracapacitor. If the full power cannot be supplied by the ultracapacitor then the remaining is supplied by the batteries. In [37] the different control strategies are summarized and compared for ultracapacitor and battery combination storage system.

In the proposed series plug-in HEV system design in this dissertation, there are three types of energy sources: battery, ultracapacitor and a small internal combustion (IC) engine. Two main operation modes are studied in this system. One is pure electrical operation mode, while IC engine is turned off; another is hybrid operation mode, while

IC engine is turned on and combined with ultracapacitor and battery to provide power. Figure 3.1 is the architecture of power train control system. This chapter mainly focuses on pure electrical operation mode. The ultracapacitor current is determined by the load demand, vehicle speed, ultracapacitor SOC and battery SOC.

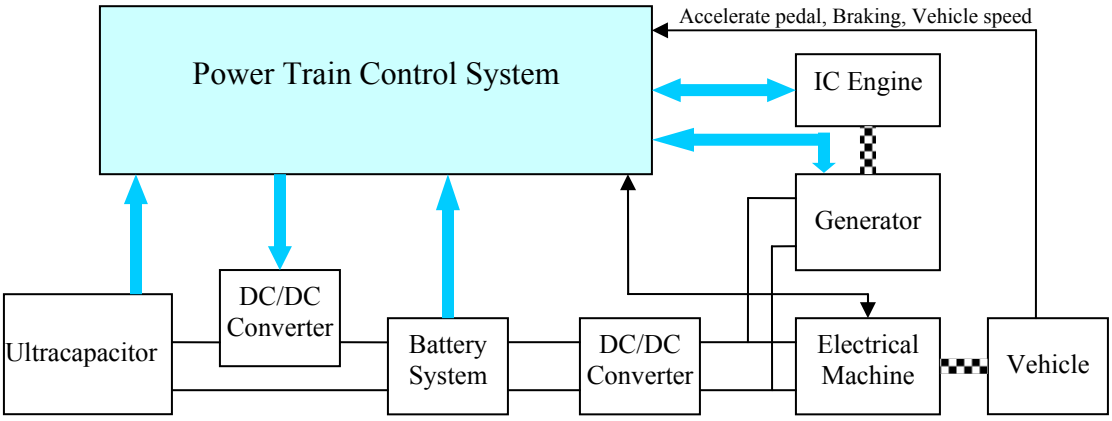


Figure 3.1 Power train control system architecture

3.2 Electrical Operation Mode

When the dual-source (ultracapacitor and battery) energy storage system can provide enough power and energy during driving, the vehicle will work on pure electrical mode and IC engine is kept off. Since the battery power is low in this system, the ultracapacitor should not only provide enough power for acceleration but also absorb enough power during regenerative braking. Therefore, the ultracapacitor SOC should be maintained in a range which can obtain both acceleration and braking performance.

The energy of ultracapacitor will be kept between E_a and E_d according to vehicle speed. E_a is the energy of UC to guarantee the vehicle acceleration from current speed to a demand speed in a short time, and it is a function of vehicle speed. The maximum demand speed at different current vehicle speed is shown in Table.3.1. E_d is designed to

ensure the ultracapacitor has enough room to absorb regeneration energy when vehicle speed is decelerated from current speed to zero in a short time. The maximum energy of ultracapacitor E_{max} minus E_d is the room for regeneration energy. E_a and E_d can be calculated at different vehicle speed based on simulation in chapter 2. The calculation results are shown in Table 3-1, in which the battery discharge/charge during acceleration/deceleration is already considered.

Table 3-1 Acceleration energy and regeneration energy according to vehicle speed

Vehicle Speed (m/s)	Maximum Demand Speed (m/s)	E_a (J)	E_{max} - E_d (J)
0	24	377313	0
4	24	373606	2569
8	24	349896	23746
12	24	303158	62749
15	24	250637	103051
18	25	222088	150612
21	26	173977	208244
24	27	117257	285148
28	29	40710	399303
30	31	14634	460677

Since the energy of ultracapacitor is a function of voltage, ultracapacitor energy E_{uc}, E_a and E_d can be calculated by following equations:

$$E_{uc} = \frac{1}{2} C V^2 \tag{3-1}$$

$$E_a = \frac{1}{2} C (V_a^2 - V_{\min}^2) \tag{3-2}$$

$$E_{\max} - E_d = \frac{1}{2} C (V_{\max}^2 - V_d^2) \tag{3-3}$$

C: capacitance of ultracapacitor, 46.875 F in this system.

V: ultracapacitor voltage.

V_a: ultracapacitor voltage to guarantee sufficient energy for acceleration from current speed to the maximum demand speed.

V_d: ultracapacitor voltage to guarantee sufficient room to absorb regeneration energy when vehicle speed is decelerated from current speed to zero.

V_{min}: minimum ultracapacitor voltage, 86.4 V in this system.

V_{max}: maximum ultracapacitor voltage, 172.8 V in this system.

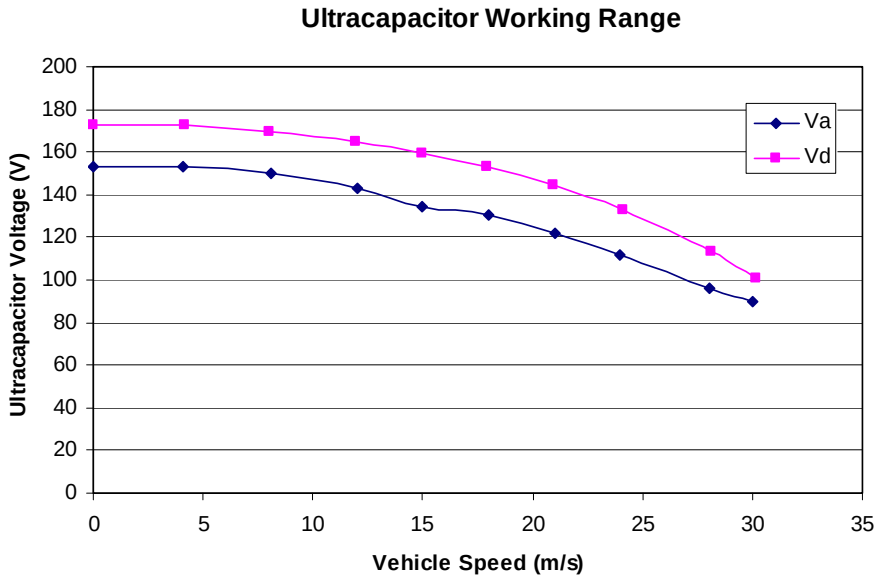


Figure 3.2 Ultracapacitor voltage working range

According to equations (3-2) and (3-3), the control system can keep ultracapacitor voltage between V_a and V_d so that the ultracapacitor energy can be maintained between E_a

and E_d. According to the data in Table 3-1, V_a and V_d can be calculated and the results are shown in Figure 3.2. The ultracapacitor can provide sufficient energy for acceleration and enough room for regeneration as long as the ultracapacitor voltage is kept between V_a and V_d.

The rule for power flow among ultracapacitor P_{uc}, battery P_{batt} and load P_{demand} are shown in as follow:

a). If $|P_{demand}| <= |P_{batt\_max}|$, P_{uc} is zero and P_{batt} is equal to P_{demand}.

b). If $|P_{demand}| > |P_{batt\_max}|$, P_{demand} is equal to the sum of P_{uc} and P_{batt}.

c). If $V_{uc} > V_d$, P_{batt} will be decreased but not smaller than - P_{batt_max}.

d). If $V_{uc} < V_a$, P_{batt} will be increased but not more than P_{batt_max}.

3.3 Hybrid Operation Mode

When the SOC of battery is low, the IC engine will be turn on. The IC engine will be operated under the highest efficiency condition. The electricity generated by IC engine will charge the energy storage system till the battery SOC reaches at high level. Figure 3.3 is the battery SOC at different operation mode. The first operation mode, electrical operation mode, is discussed in last section. The third operation mode is that the battery is charged by plugging into power grid when the vehicle is already stopped. This section will focus on the second operation mode: hybrid operation mode.

Following are the rules for hybrid operation mode:

a) If $P_{demand} <= P_{engine}$, the load demand power is supplied by IC engine and the energy storage system will be charged in this condition.

b) If $P_{demand} > P_{engine}$, the load demand power is supplied by both IC engine and ultracapacitor.

c) During hybrid operation mode, the ultracapacitor power control is the same with electrical operation mode. The ultracapacitor voltage will be kept between V_a and V_d.

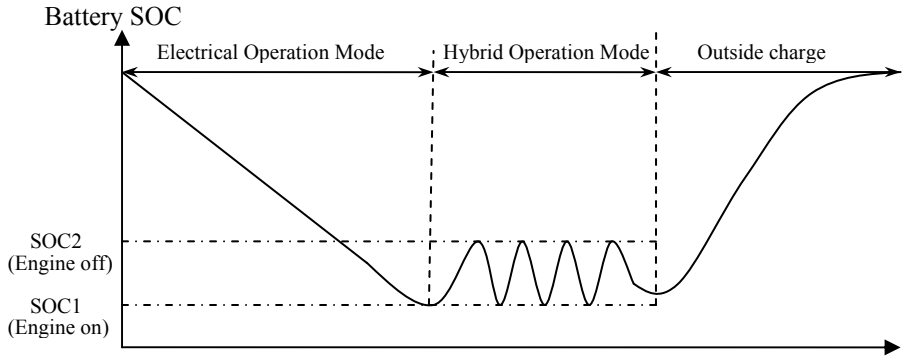


Figure 3.3 The battery SOC at different operation mode

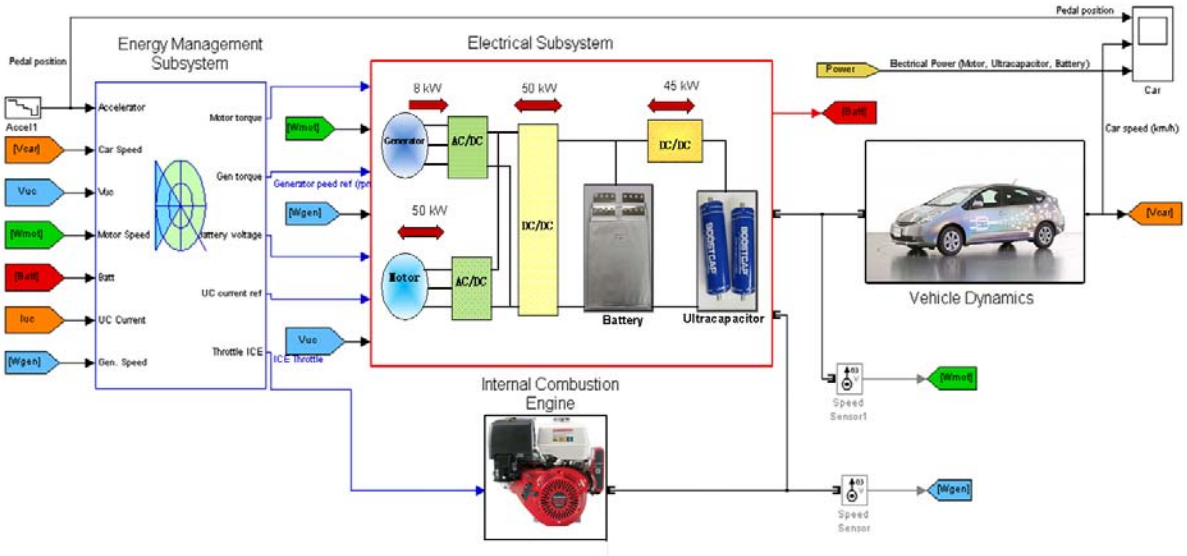


Figure 3.4 HEV power train system model based on MATLAB Simulink

3.4 Simulation Model for HEV Power Train System

To demonstrate the performance of vehicle based on the rule discussed in section 3.2, a simulation model is built based on MATLAB Simulink, shown in Figure 3.4.

The Energy Management Subsystem is the power train control system, which determines the reference signals for ultracapacitor, the electric motor drive, the electric generator drive and the IC engine in order to accurately distribute the power from different sources. These signals are calculated according to pedal position, vehicle speed, battery SOC and ultracapacitor SOC.

The Electrical Subsystem is composed by six parts: the ultracapacitor, the battery, the generator, the electrical motor, and two bidirectional DC/DC converters.

a) The battery is a 25 Ah, 236.8 V, 6 kW Lithium ion battery.

b) The ultracapacitor is a 46.88 F, 172.8 V ultracapacitor.

c) The electrical motor is a 500 Vdc, 50 kW interior permanent magnet synchronous machine (PMSM) with associated drive.

d) The generator is a 500 Vdc, 10 kW PMAM with the associated drive.

e) The first DC/DC converter between the battery and the motor/generator is voltage-regulated. The converter adapts the low voltage of the battery to the high voltage DC bus which feeds the AC motor at a voltage of 500V.

f) The second DC/DC converter between the battery and ultracapacitor is to control the power flow from the ultracapacitor. This DC/DC converter is a bidirectional 16-phase interleaved converter based on DCM operation, and the detail discussion is shown in chapter 4.

The Vehicle Dynamics Subsystem models the mechanical parts of the vehicle. The IC engine is based on the model of Honda GX390 engine.

3.5 Simulation Results

The demonstration simulates the power flow between battery and ultracapacitor during different operation modes: accelerating and regenerative braking. The results are shown in Figure 3.4.

a) 0 ~ 0.7 s, the vehicle speed starts from 0 km/h and the driver pushes the accelerator pedal to 70%. The electrical motor power is only fed by the battery as long as the power is lower than 6 kW.

b) 0.7 ~ 10 s, the required power is greater than 6 kW. The electrical motor power comes from both battery and ultracapacitor. The battery power is kept constant and the ultracapacitor power varies with load power.

c) 10 ~ 12 s, the required power is smaller than 6 kW at high speed. The ultracapacitor power falls to zero, and the electrical motor power is only fed by the battery.

d) 12 ~ 15 s, the accelerator pedal is set to -50% and vehicle is operated under regenerative braking condition. The battery is kept recharging at aconstant power and other extra regenerative braking power is absorbed by ultracapacitor.

Figure 3.5 shows the ultracapacitor voltage and working range V_a and V_d. The ultracapacitor voltage is kept between V_a and V_d during driving. Figure 3.6 shows the battery SOC, the voltages (DC bus, battery and ultracapacitor) and the currents (motor, battery and ultracapacitor).

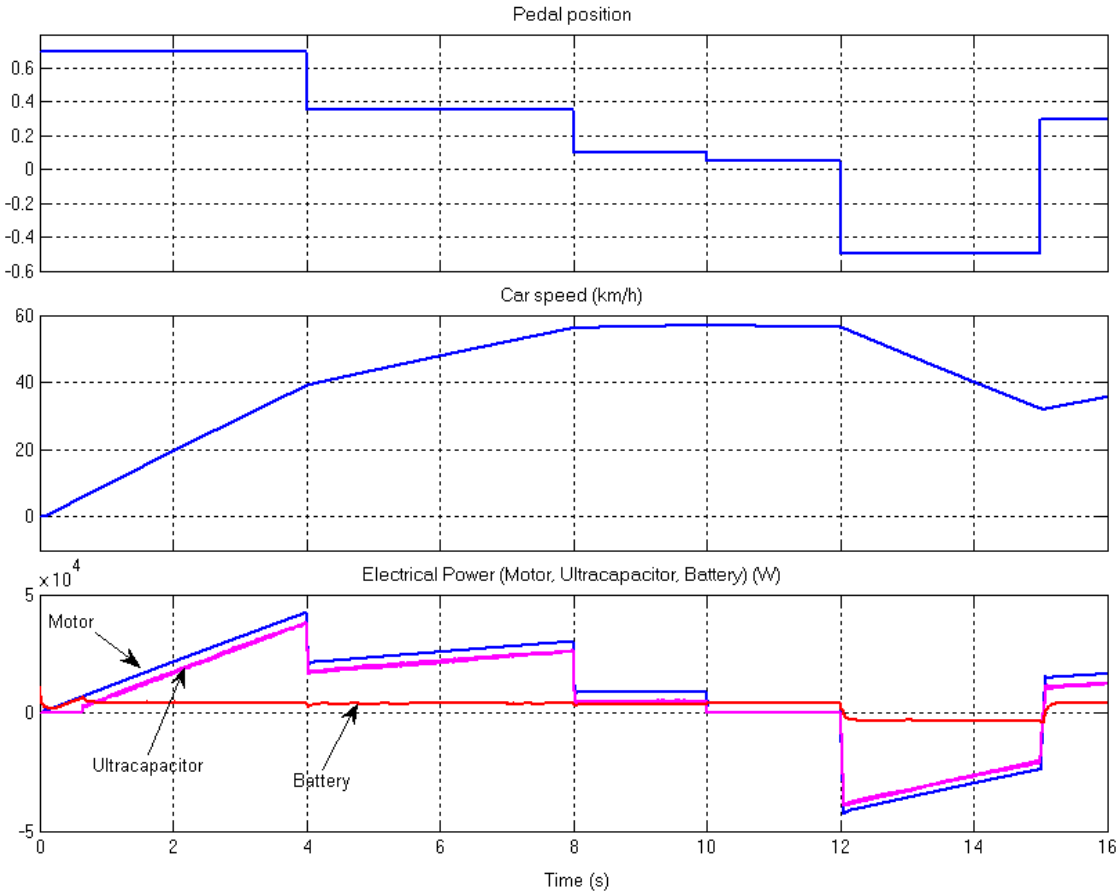


Figure 3.5 Vehicle pedal position, car speed and electrical power distribution

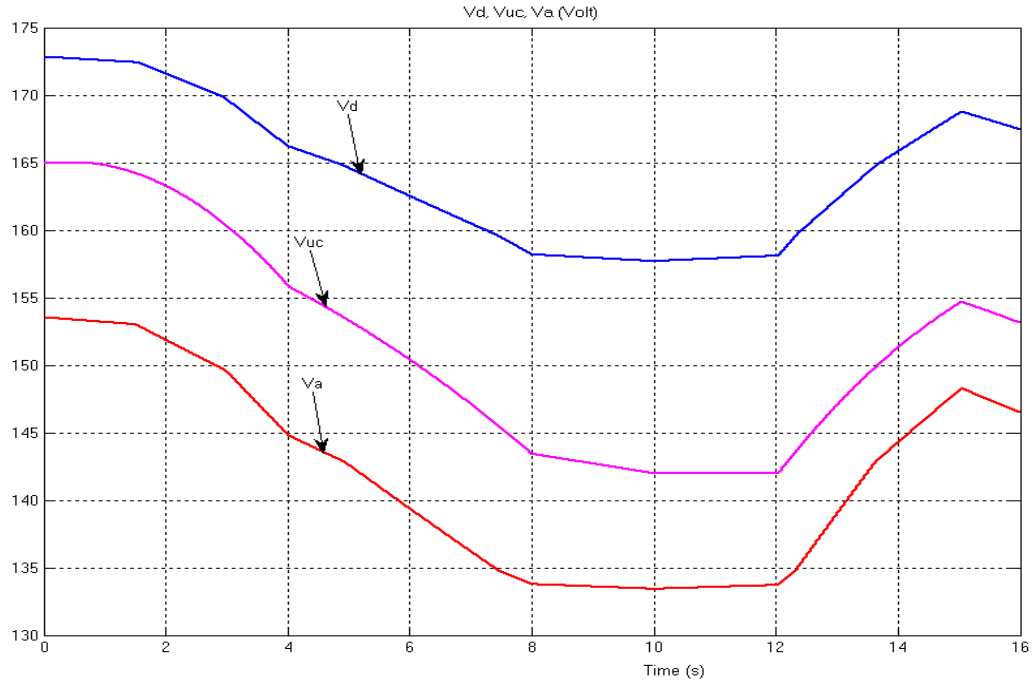


Figure 3.6 Ultracapacitor voltage and its work voltage range

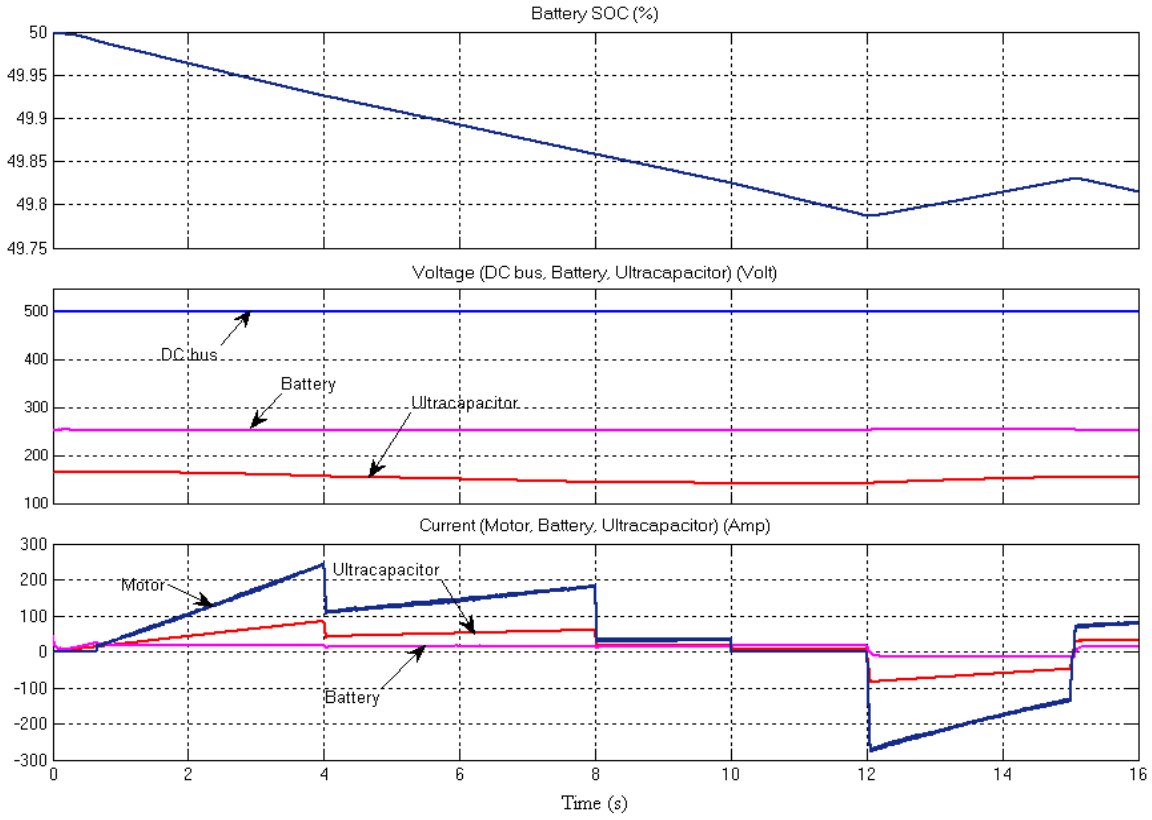


Figure 3.7 Electrical measurements

3.6 Conclusion

For the application of broad range (from average to high peak) of power demand such as HEV, the dual-source energy storage system, battery plus ultracapacitor, can bring significant benefits, due to complementary characteristics of batteries and ultracapacitors. The proposed control strategy can keep the battery working at low peak power and low current ripple conditions, which will improve battery life and ensure battery working under safety range. Meanwhile, the control strategy also maintains the ultracapacitor SOC in a range depending on vehicle speed, which will improve the vehicle's ability to meet power demands and the overall vehicle efficiency.

Chapter 4.

16-PHASE BIDIRECTIONAL INTERLEAVED DC/DC CONVERTER BETWEEN ULTRACAPACITORS AND BATTERIES

In this chapter, a 16-phase interleaved bidirectional DC/DC converter is presented featuring smaller input/output filters, faster dynamic response and lower device stress for hybrid vehicle applications. This converter is connected between the ultracapacitor (UC) pack and the battery pack in energy storage system of hybrid vehicle. Typically, multi-phase interleaved converters require a current control loop in each phase to avoid current imbalance between phases. This increases system cost and control complexity. In order to minimize imbalance currents and remove the current control loop in each phase, the converter is designed to operate in the discontinuous conduction mode (DCM). The high current ripple associated with DCM operation is then alleviated by interleaving. The design, construction and testing of experimental hardware prototype are presented with the testing results are included in this chapter.

4.1 Motivation and Background

The transition from internal combustion engine (ICE) vehicles to pure electric vehicles (EVs), or hybrid electric vehicles (HEV) is very attractive and desirable, but there are still some serious issues in energy storage technology. The combination of batteries and ultracapacitors as an energy storage unit is considered as a potential solution

to improve vehicle performance, and battery lifetime and safety [37] [38]. This combination allows an excellent performance in both high acceleration and regenerative braking power. The typical topology of a battery and ultracapacitor energy storage system is shown in Figure 4.1. The battery pack is parallel connected with the ultracapacitor pack through a bi-directional DC/DC converter [39][40]. One objective of the design is that the converter has to achieve high power density with low current/voltage ripple, particularly on the battery side. Moreover, the converter also has to meet prevalent automotive requirements, such as high efficiency, low cost, low EMI, and compacted component size. Several different circuit topologies for high power applications have been published in [41][42][43][44][45]. A multi-phase interleaved DC/DC converter is adopted as a good solution for the application with high power and high current.

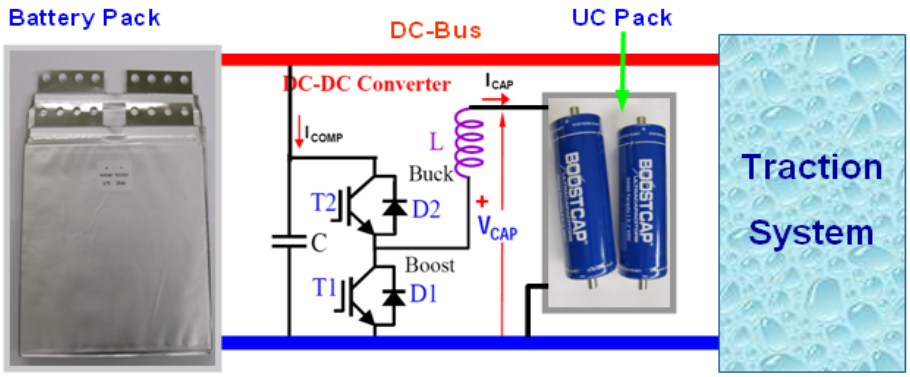


Figure 4.1 Typical topology for battery and ultra-capacitor energy storage system

Interleaving techniques have been used widely in power converters in recent years [45][46][48][49][50][51]. Typical benefits of interleaving techniques includes: reducing device stress by separating power into each separate phase, reducing filter size by increasing effective frequency, and cancellation of the current ripple effect. The interleaving techniques also enables some other beneficial technology changes, such as

from aluminum electrolytic or polymer organic capacitors to film, or even ceramic capacitors that would improve the equivalent series resistance, power density, and reliability in a rugged thermal environment.

However, most of the published papers require a current control loop in each phase to achieve balanced phase currents and improve dynamic response [48][51][52][53]. The cost, weight, and control complexity grows when the number of phases increases, which limits the total number of phases to be considered. The optimum number of phases will be another issue that has to be considered [46][54][55]. Because imbalance current depends mainly on duty cycle differences, inductance value differences, and parasitic resistance differences among different phases, all of which integrate over time in a continuous conduction mode converter. In order to minimize imbalance currents and eliminate the current control loops, some authors designed a synchronous converter working in continuous conduction mode (CCM). However, the inductor current falls to a negative value during every switching cycle [49][50], which would lead to a higher current ripple per phase and lower efficiency, especially for light load condition.

This chapter proposed a design of a 16-phase interleaved power converter operating in discontinuous conduction mode (DCM) that improves the current balance without using current control loops. The design also has a fast dynamic response since the phase current is reset to zero at every switching cycle. To verify the proposed approach, a 45-kW hardware prototype has been constructed and tested with experimental results presented.

4.2 Multi-phase Interleaved DC/DC Converter on DCM

4.2.1 Interleaved Converter Topology and Operation

The multiphase interleaved DC/DC converter is a circuit topology where the basic converter circuits are placed in parallel between the input and output. The schematic diagram of the 16-phase interleaved DC/DC converter is shown in Figure 4.2. An ultracapacitor pack is placed on the low-voltage side and a battery pack is placed on the high-voltage side. The high-voltage side is also connected with the traction system or load. When the demand power is larger than battery pack rating power, the ultracapacitor supplements power for acceleration and the converter works in boost mode. When the energy stored in ultracapacitor is not full and regenerative braking power is larger than the battery's maximum charging power, the ultracapacitor absorbs power from regenerative braking and the converter is operated in buck mode.

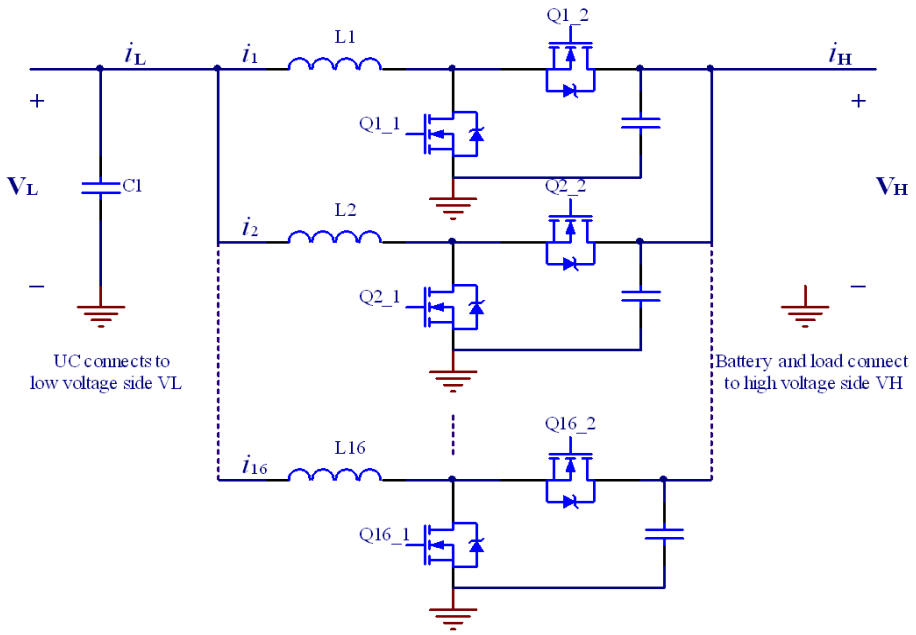


Figure 4.2 Power stage of a 16-phase bidirectional DC/DC converter

The switch gate signals and inductor currents are shown in Figure 4.3. The gate signals for the phases are exactly shifted by $360^0/N$ (N is the number of phases, here N = 16). All the phase currents have the same waveform, and are also shifted 360^0/N. The ripple in the low voltage side current i_L, which is the sum of all low side phase-currents, is significantly reduced due to harmonic cancellation. Furthermore, the frequency of the ripple in i_L is increased to $N*f_s$ (f_s is switching frequency).

Because of lower current ripple and less harmonic, the requirement of filter capacitance on the low voltage side can be greatly reduced or even be removed. The filter capacitance on the high side is composed of N capacitors, each one being placed physically close to its phase, in order to reduce the parasitic inductance between the switch and the capacitor. Each phase processes only $1/N$ of the total power, which greatly reduces the stresses on switch devices.

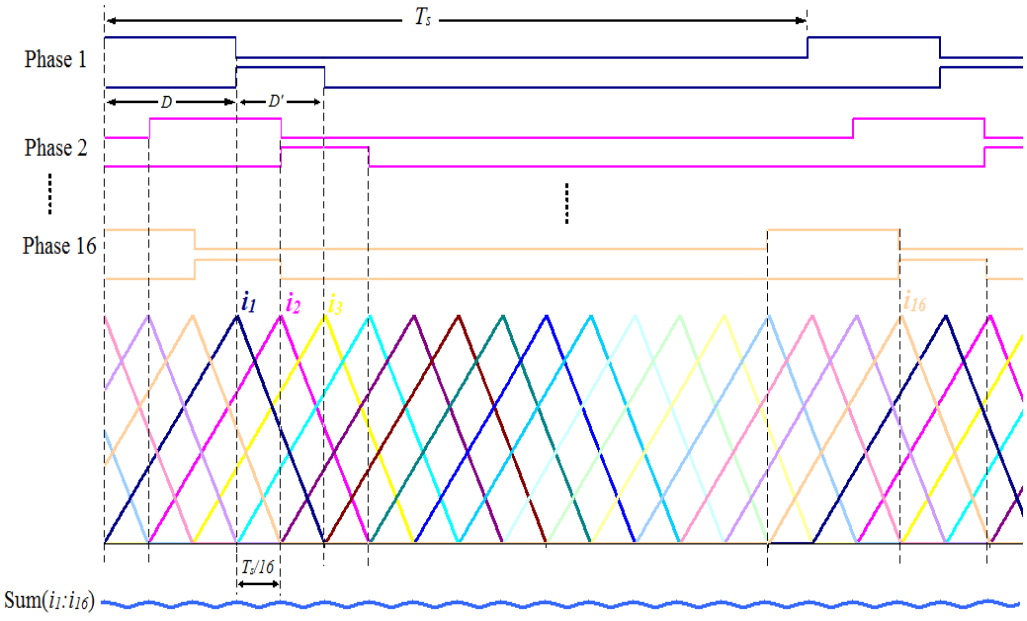


Figure 4.3 The gate signal and inductor currents waveforms

4.2.2 DCM in Synchronous DC/DC converter

In DCM operation, the main switch duty ratio is demanded by the output current. This allows the control system to respond very rapidly to the changes in the demanded load current. Figure 4.4 shows circuit diagram of single phase and Figure 4.5 shows the gate control signal and inductor current of the single phase in boost mode.

In boost mode operation, the duty ratio of the main switch (low side switch Q1) is a function of output current, and can be calculated by following equation:

$$D_{boost} = \sqrt{\frac{2Lf_s I_2 (V_H - V_L)}{V_L^2}} \tag{4-1}$$

Where, L is the inductance in each phase; f_s is the switch frequency; I_2 is the average current on the low voltage side; I_H is the average current on the high voltage side; V_H is the voltage on the high voltage side; V_L is the voltage on the low voltage side.

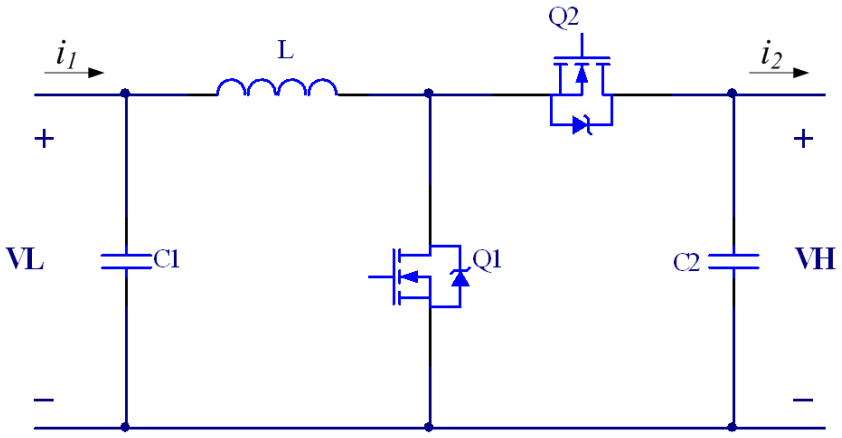


Figure 4.4 Circuit diagram of single phase

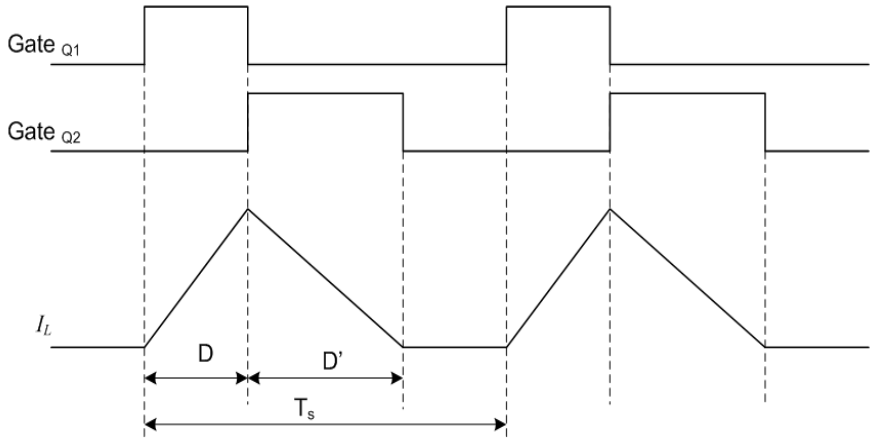


Figure 4.5 Gate signal and inductor current waveform of boost mode

In CCM condition of synchronous converter, the duty ratio D' of the freewheeling MOSFET equals to $\overline{D}$ with necessary dead time. While in DCM condition, the freewheeling MOSFET has to be turned off by zero current detection in inductor current, or the on-time is estimated by the control stage. In this converter, the on-time of freewheeling MOSFET is estimated by the following equation in boost mode:

$$D'_{boost} = \frac{D_{boost} \cdot V_L}{V_H - V_L} \tag{4-2}$$

Figure 4.6 shows the tested waveforms of following four signals: the low side switch gate voltage v_{gs1}, the high side switch gate voltage v_{g2} with ground as reference, the low side switch voltage v_{ds1}, and the inductor current i_L in boost converter mode. The figure shows that the high side switch turns off close to where the inductor current reaches zero and thus that the D' estimation equation works well in the real system.

Equations (4-3) and (4-4) are the duty ratio functions for main switch and freewheeling MOSFET in buck mode.

$$D_{buck} = \sqrt{\frac{2Lf_s I_1 V_L}{V_H (V_H - V_L)}} \tag{4-3}$$

$$D'_{buck} = \frac{D_{buck} \cdot (V_H - V_L)}{V_L} \tag{4-4}$$

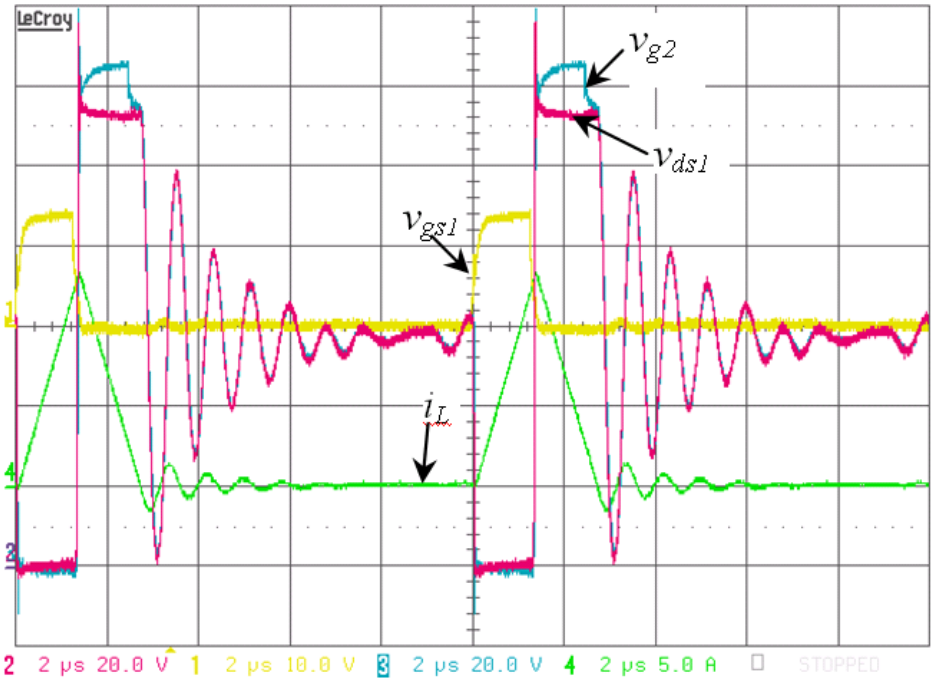


Figure 4.6 Measure waveforms for one phase

From above equations, the imbalance current depends primarily on duty ratio differences and inductance differences. However, in DCM mode, the imbalance current is very small since each phase current starts from zero at every switching cycle. A 1% difference in duty cycle will causes a 2% current imbalance. In CCM mode, however, a 1% difference in duty cycle can cause an unacceptable current imbalance (for example, 84% imbalance current [46]) over time. In order to minimize the difference in each duty cycle, digital controllers, such as field-programmable gate arrays (FPGA), can generate

many signals simultaneously with high accuracy [47]. The phase shift techniques are also implemented in the digital controller.

4.2.3 Control Stage Design

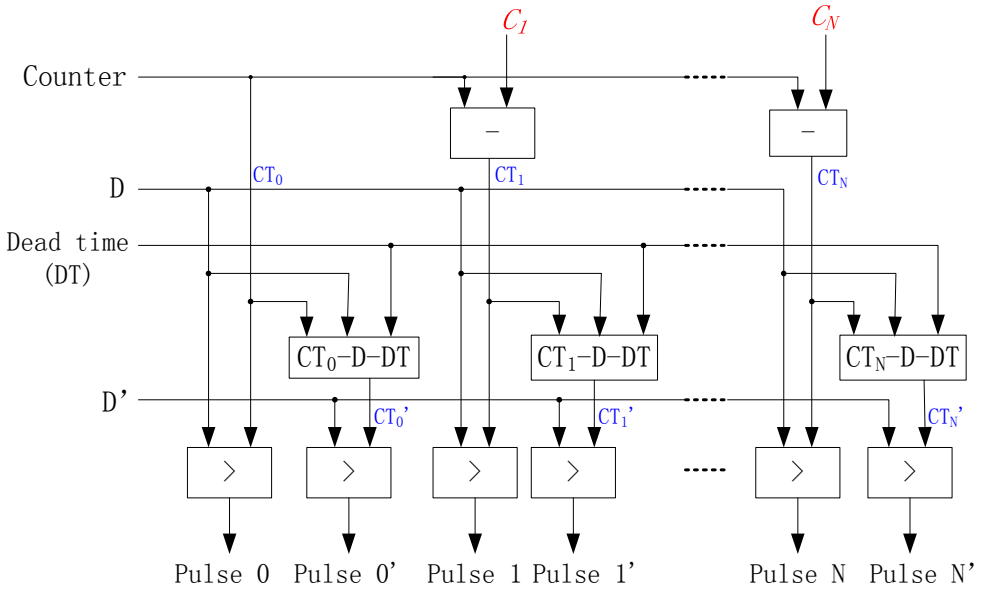


Figure 4.7 Phase-shifter structure implemented in a FPGA

The control circuit will generate the driving signals for the 16 phases, that is, totally 32 gate signals need to be generated. Input voltage, output voltage and high-voltage side current should be measured to generate pulses. Using digital control, these pulses can be kept to a high accuracy level therefore the imbalance current is very small. Thus, current control loop in each phase can be removed and the complexity of control circuit can be reduced. The main switch duty ratio can be calculated by equation (4-1) in boost mode and equation (4-3) in buck mode in the open-loop control system. Also, it can be achieved by a simple proportional-integral controller (PI) in the closed-loop control

system. The duty ratio of freewheeling transistor is calculated by equation (4-2) or equation (4-4). Each driving signal is shifted from the previous one.

The gate signals are generated by making a comparison between duty cycle and counter. Each phase has its own counter. The phase shift is achieved by controlling the value of the counter. The phase-shifter structure is shown in Figure 4.7. There is a main counter, and the calculation of other counters is based on it (CT_0 in Figure 4.7). For the main switch of each phase, these counters are the main counter minus some constants to get new counters, and then compare to the duty cycle. The main switch counter CT_i and constants C_i to be added are:

$$CT_i = CT_0 - C_i \tag{4-5}$$

$$C_i = \frac{i \cdot C_p}{N+1} \tag{4-6}$$

For the slave switch of each phase, the counter can be calculated:

$$CT_i^{'} = CT_i - D - DT \tag{4-7}$$

Where, i is the phase number; N+1 is the number of phase; C_p is the resolution of period which is equal to the range of the counter; DT is the dead time.

The FPGA NI 7831R has 40 MHz on board frequency generator with a high duty cycle resolution (400 different duty cycles for 100 kHz switch frequency). Figure 4.8 shows part of the phase-shifter program for the 16-phase interleaving based on NI LabVIEW environment.

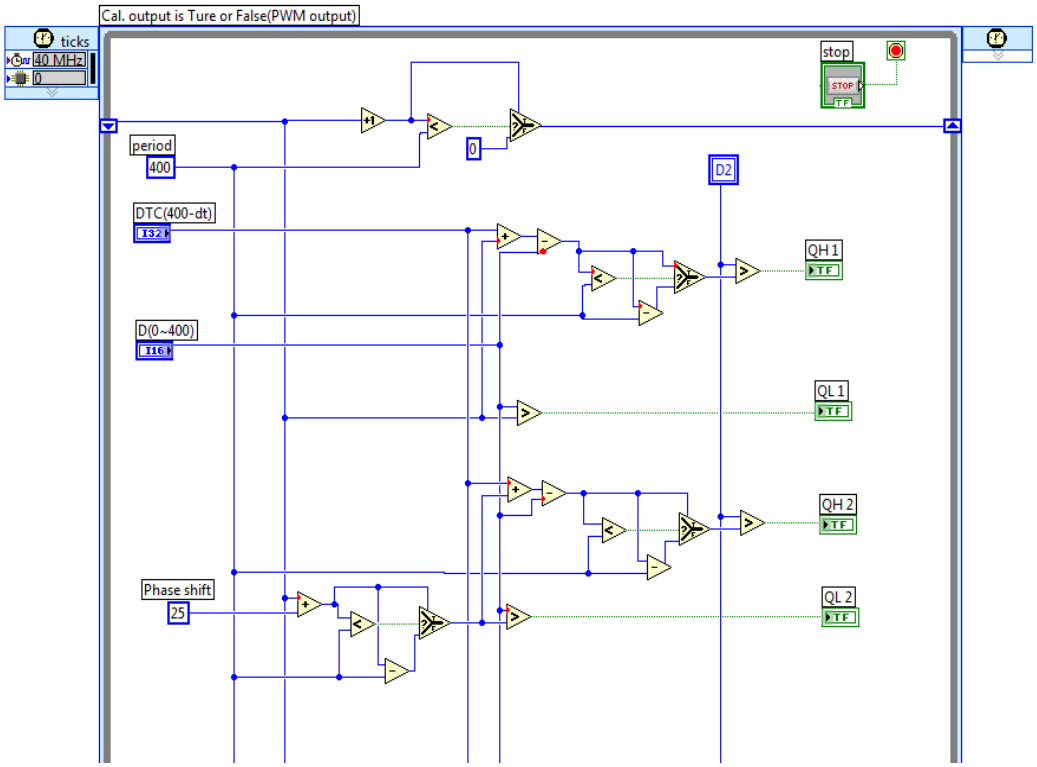


Figure 4.8 Phase-shifter program based on NI LabVIEW

4.3 Circuit Parameter Optimization

4.3.1 Inductor Design

Generally, inductors are the largest, most expensive and inefficient items in a power system. A reasonable design in inductor can have a significant impact on the rest of the power electronics design. The inductors applied on this interleaved DC/DC converter are low value but will work under high frequency with high current ripple. Therefore, the inductor losses become a main issue during design.

The inductor losses mainly include core loss and winding loss. Core loss, for a given frequency, is material dependent. The common core materials for inductor at 100 kHz frequency are ferrite cores and powdered metal cores. The ferrite cores are the most

popular core materials for inductor and fly back transform due to lower cost and lower loss than powdered metal core. Usually, an air gap is added in series with the core to provide the required energy storage capability, lower effective permeability and thus lower the operating flux density. The problem for this type of inductors is the gap-loss. Any winding turns positioned closed to the gap will most likely exist within the high flux density of the fringing field and huge eddy current losses can occur in those few turns close to the gap, which can cause severe localized heating problems, even leading to the failure of the inductor. To solve this problem of gap-loss, one way is to keep the windings to a single layer substantially mitigating copper losses; another way is to use a powdered metal core. Powdered core helps keep the operating flux density low without creating localized gap-loss problems. However, powdered cores typically have significantly higher core losses than ferrite cores, especially with relatively high ripple current at very high frequency.

Core losses are a result of variable magnetic field in the core material. For a given material, the core loss curve can be found in its datasheet which is a function of operating frequency and flux swing. The core losses are due to hysteresis, eddy current and residual losses in the core material.

For a typical square wave voltage across an inductor in a switching power supply on CCM shown in Figure 4.9, the biasing magnetic material with DC current will shift the minor alternating BH loop, shown in Figure 4.10. It is only the alternating flux density (ΔB) that generates core loss. The value of peak AC flux density used with the core loss curve in datasheet can be calculated:

$$B_{pk} = \frac{5 \cdot E_{pk} \cdot t}{A \cdot N} \tag{4-5}$$

Where, B_{pk} is the peak AC flux density (ΔB/2) (unit: mT); E_{pk} is the peak voltage across coil during "t" (unit: volt); t is the time of applied voltage (us); A is the cross-sectional area (cm^2); N is the number of turns.

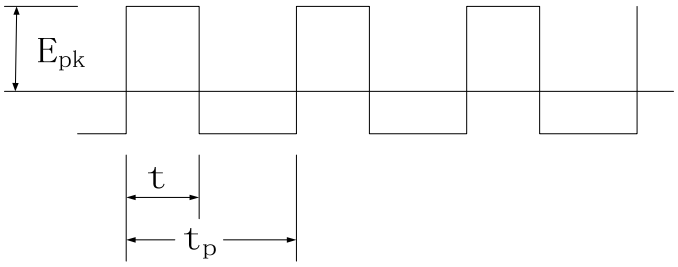


Figure 4.9 The Square wave voltage across an inductor on the CCM.

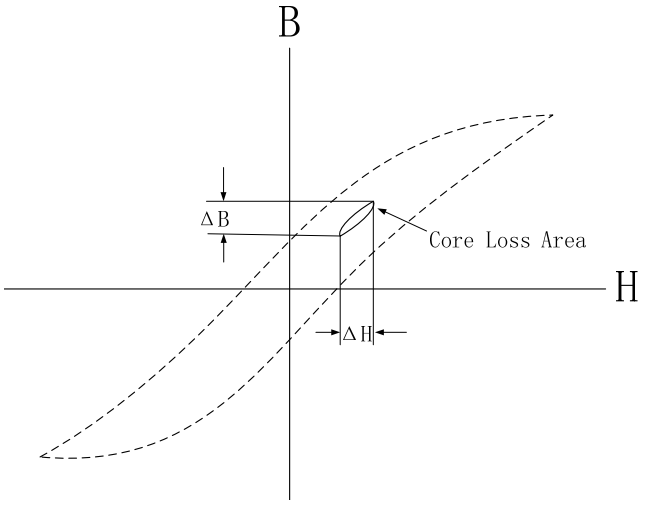


Figure 4.10 BH loop with DC current on CCM

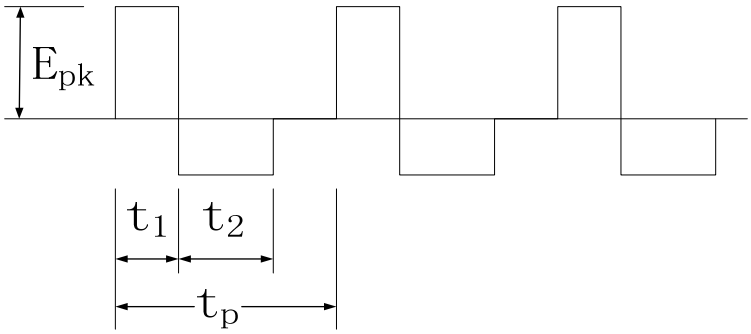


Figure 4.11 The voltage across an inductor on DCM

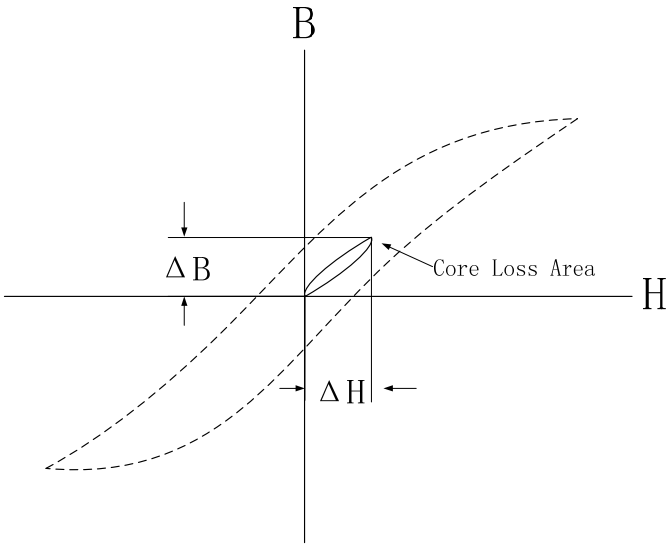


Figure 4.12 BH loop with DC current on DCM

On the DCM operation, the current falls to zero and is kept at zero until next cycle. The core loss is very small and can be ignored after the current falls to zero on each cycle. The voltage across an inductor and the BH loop during DCM operation are shown in Figure 4.11 and Figure 4.12. The peak AC flux density can be calculated by:

$$B_{pk} = \frac{5 \cdot E_{pk} \cdot t_1 \cdot (t_1 + t_2)}{A \cdot N \cdot t_p} \tag{4-6}$$

Since the current ripple on DCM operation is more than twice of average current value, the core loss in an inductor might become a noticeable effect on the whole circuit efficiency. The core loss is calculated for different core material and different core size at a specific condition. Assuming the 16-phase interleaved dc converter working at power rating with boost converter, so each phase is working at 2.8 kW. The low side voltage is 87 V and the high side voltage is 268V. Other specific work conditions for an inductor are listed in Table 4-1.

Table 4-1 Specifications for the inductor

L (μH)	E_{pk} (V)	t_1 (μs)	t_2 (μs)	f (kHz)
5	87	5	2.4	100

Table 4-2 is the powdered core properties and core loss calculation results. Table 4-3 is the ferrite core properties and core loss calculation results. Comparing with these two tables, the core loss of powdered core materials is much greater than the core loss of ferrite core materials. Therefore, the ferrite core 3C94 has been chosen for the inductor in DC/DC converter.

The gap-loss has to be considered, especially for high-current, high-ripple inductors with air gap. To reduce the gap-loss and avoid the winding being melted, following action were taken during experiment hardware design: 1) Using Litz wire winding to reduce ac winding loss; 2) Keeping the windings positioned close to the air gap to a single layer; 3) Keeping other windings a little distance from air gap. Figure 4.13 is a photo of a hardwired inductor in the DC/DC converter circuit. The bobbin has been eliminated to save the space in the board.

Table 4-2 Powdered core properties and calculation results

Core Material	A_L (nH/N^2)	*le* (cm)	A_e (cm^2)	V_e (cm^3)	*Turns N*	B_{pk} (mT)	Core Loss (W)
XFlux	135	10.74	1.99	21.3	6	132.9	63.9
Cx60	85.32	19.612	2.2192	43.523	7.6	94.8	27.4
-M125	628	6.496.49	2.636	17.12	2.8	216.4.	66.8
-66	130	33.1	5.24	173	6.2	49.6	88.2

Table 4-3 Ferrite core properties and calculation results

Core material	μ	*le* (cm)	A_e (cm^2)	V_e (cm^3)	*Turns N*	B_{pk} (mT)	Core Loss (W)
3F3	1660	12.7	2.80	35.5	6.6113	86.95	2.0
3C90	1770	12.7	2.80	35.5	6.54301	87.85	2.0
3C94	1770	12.7	2.80	35.5	6.54301	87.85	1.6
3C96	1660	12.7	2.80	35.5	6.6113	86.95	1.1

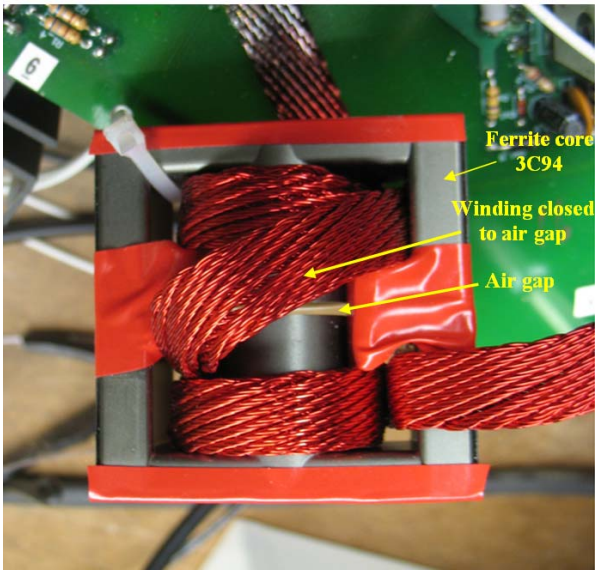
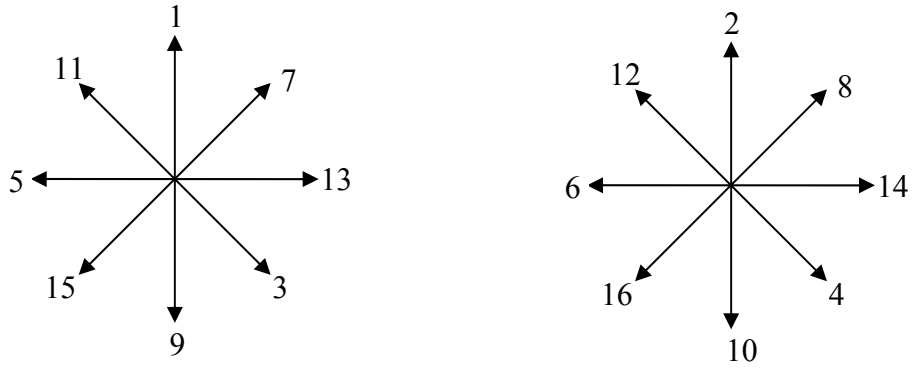


Figure 4.13 Photo of a hardwired inductor

4.3.2 PCB Board Topology

In order to minimize imbalance current between phases, the structure differences between phases should be minimized. The heat sink and inductor occupy a large volume in each phase therefore it would be congested if all 16 phases been put on a single circuit board. Therefore, the 16 phases are separated into two boards and each board has 8 phases, distributed as a star-shaped with optimized phase order. Figure 4.14 shows the physical phase positions of two boards with phase number labeled. One board hosts the odd phases and is ordered with optimized parasitics. Another board hosts the even phase and is also ordered with optimized parasitics. The capacitors in high voltage side are composed of 16 film capacitors, and each one is placed closed to its phase, to reduce harmonics in the circuit. The star-shaped distribution is to maintain the same physical position of each phase. The optimized phase orders not only keeps each phase under the same operation condition but also allows precise harmonic cancellation and current ripple reduction in the high side capacitor.



a) Physical positions of the odd phases b) physical positions of the even phases

Figure 4.14 Optimized order for two boards

Based on above design methodology, a 16-phase bidirectional DC/DC converter without current control loops has been built and tested. A photo of the 16-phase prototype is shown in Figure 4.15, which is composed two circuit board with each one hosts 8-phase converter. Figure 4.16 shows a view of one of the two circuit boards.

Figure 4.15 Prototype of 16-phase interleaved DC/DC converter

Figure 4.16 Prototype of 8-phase on one board

4.3.3 Circuit Protection

For the purpose to prevent over-current or short circuit conditions of the experimental circuit board during testing, a circuit protection module was developed. Though existing devices, such as a circuit breaker or a fuse, are capable to perform the same functions, the speed of fuse or circuit breaker is not fast enough to clear the fault current, such as within several seconds for 200% of rating current. The red dotted line in Figure 17 is the schematic diagram of the circuit protection for over current protection between ultracapacitor and DC/DC converter, which can be opened in μs during over current condition. The diode D1 in the circuit is to keep the voltage positive in the diode and avoid the over voltage of MOSFET when over current happened.

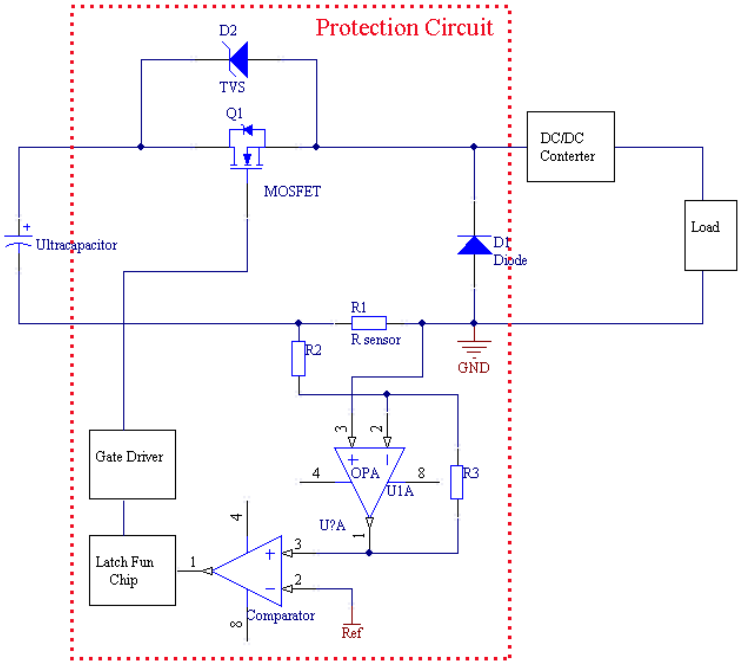


Figure 4.17 Over current protection circuit

4.4 Experiment and Results

In the experimental hardware design, following components has been used: Power MOSFET IRFP4242; Gate driver FAN7390; Inductor 5 μH, ETD54 core and 3C94 material with Litz wire winding; Low side capacitor 30 μF ; High side capacitor 240 μF which is composed of 16 film capacitors of 15 μF each (one capacitor close to one phase). The gate control signal has been implemented by applying an FPGA board (National Instrument NI-7831R FPGA, 40 MHz) programmed by PC. The complete converter power rating is 45 kW, and the switching frequency is 100 kHz.

The imbalance currents are mainly caused by the differences in inductance and duty ratio between each phase. Figure 4.18 shows the inductor current of each phase and the total current before/after capacitor filter. The differences of each phase current are primarily caused by the inductance differences since those inductors are made by hand and the unequal inductance values are inevitable. The differences on the duty ratio between each phase are very small because of high accuracy driving signals generated by FPGA. The values of inductance and current on each phase are shown in Table 4-4. The results show that based on the proposed design discussed above, the imbalance current between these phases is very small. In theory, 1% difference in inductance would case 1% of current imbalance. It is concluded from testing that generally a 5% difference in inductance causes just a 10% or less current imbalance. The ripple of total current from 16 phases before capacitor is much smaller than that of individual phase current. Therefore, it is possible to get a lower ripple current in the low side of converter by using a small capacitor filter.

Table 4-4 Inductance and current in each phase

Phase number	Phase1	Phase2	Phase3	Phase4	Phase5	Phase6	Phase7	Phase8
Inductance (uH)	4.86	5.28	4.99	5.29	4.92	4.95	5.25	5.14
Inductance deviation (%)	5.1%	-3.0%	2.7%	-3.3%	4.1%	3.4%	-2.5%	-0.2%
Phase current (A)	1.43	1.21	1.39	1.25	1.34	1.32	1.32	1.30
Current deviation	-10.1%	6.0%	-6.0%	3.6%	-3.5%	-1.6%	-1.8%	-0.6%
Phase number	Phase9	Phase10	Phase11	Phase12	Phase13	Phase14	Phase15	Phase16
Inductance (uH)	4.91	5.09	5.06	5.18	5.23	5.29	5.29	5.28
Inductance deviation	4.3%	0.8%	1.3%	-1.1%	-2.0%	-3.3%	-3.3%	-3.0%
Phase current (A)	1.31	1.29	1.27	1.27	1.29	1.23	1.24	1.25
Current deviation	-1.2%	0.2%	1.9%	1.9%	0.3%	4.7%	4.1%	3.2%

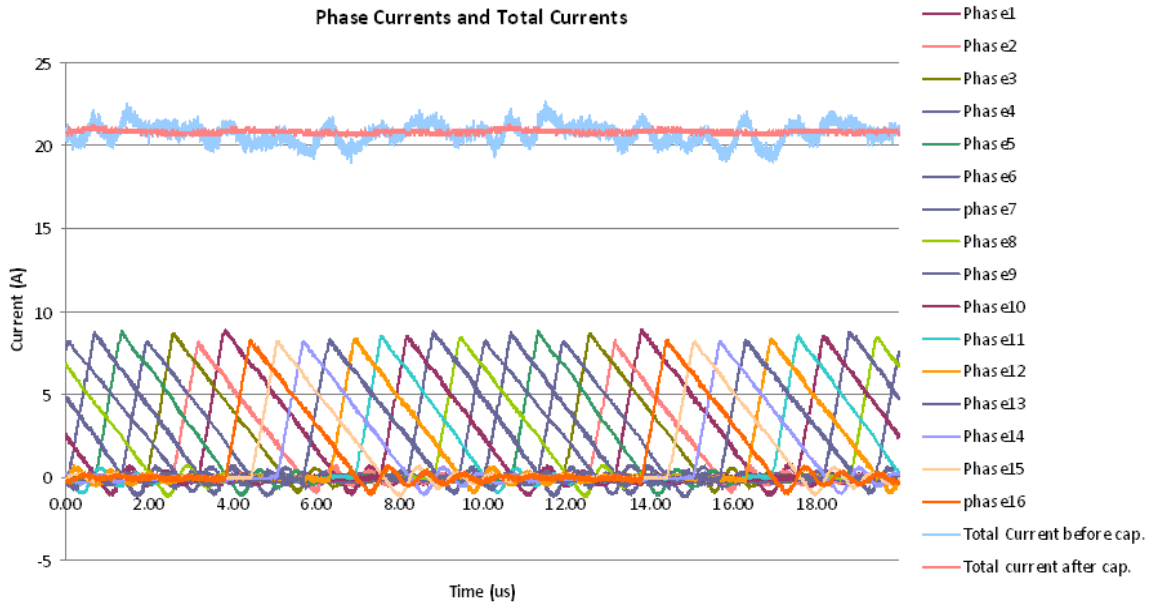


Figure 4.18 Phase currents and their total currents

Table 4-5 Imbalance current induced by differential duty ratio

	Average current in Phase14 (A)	Average current in Phase15 (A)	$1-I_{\_14}/I_{\_15}$
Without extra duty ratio	1.32	1.31	0.8%
Extra 0.5% duty ratio in phase 14	1.38	1.32	4.5%
Extra 1% duty ratio in phase 14	1.48	1.33	11%

To validate the effectiveness of this approach, an external 0.5% and 1% extra duty cycle has been applied to Phase 14 to compare the inductor current with and without extra duty cycle condition. Figure 4.19 – Figure 4.21 and Table 4-5 show the results of this experiment. Phase 15 is chosen to compare with Phase 14 in Table 4-5 since the inductance in these two phases are very close. The results are shown that the current imbalance is still acceptable or the performance is very good even with extra 1% duty cycle. Normally, the differences on the duty ratio in an FPGA are very small, which is less than 0.25% in this application.

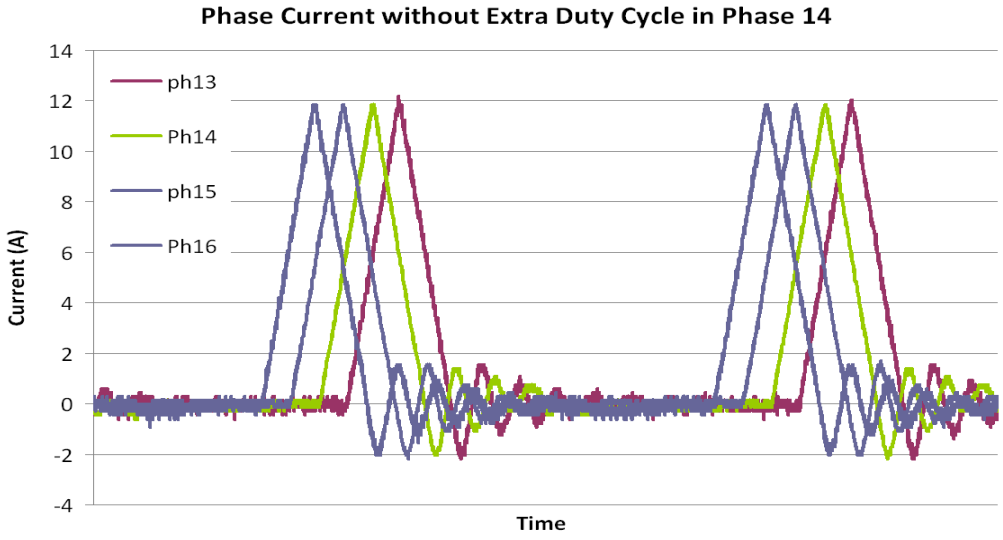


Figure 4.19 Phase currents without extra duty cycle

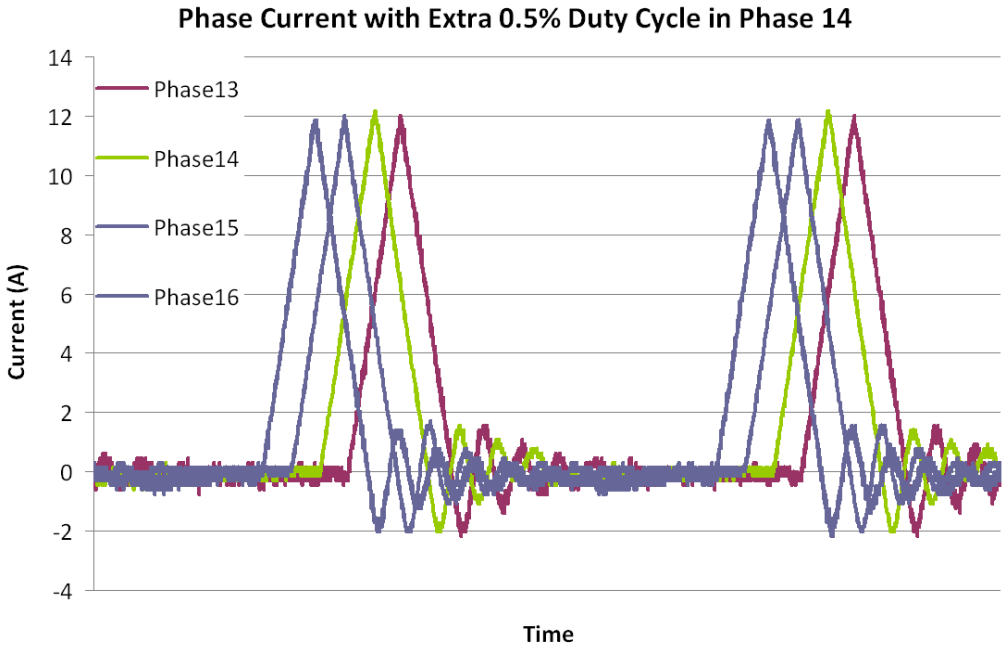


Figure 4.20 Phase current with extra 0.5% duty cycle in phase 14

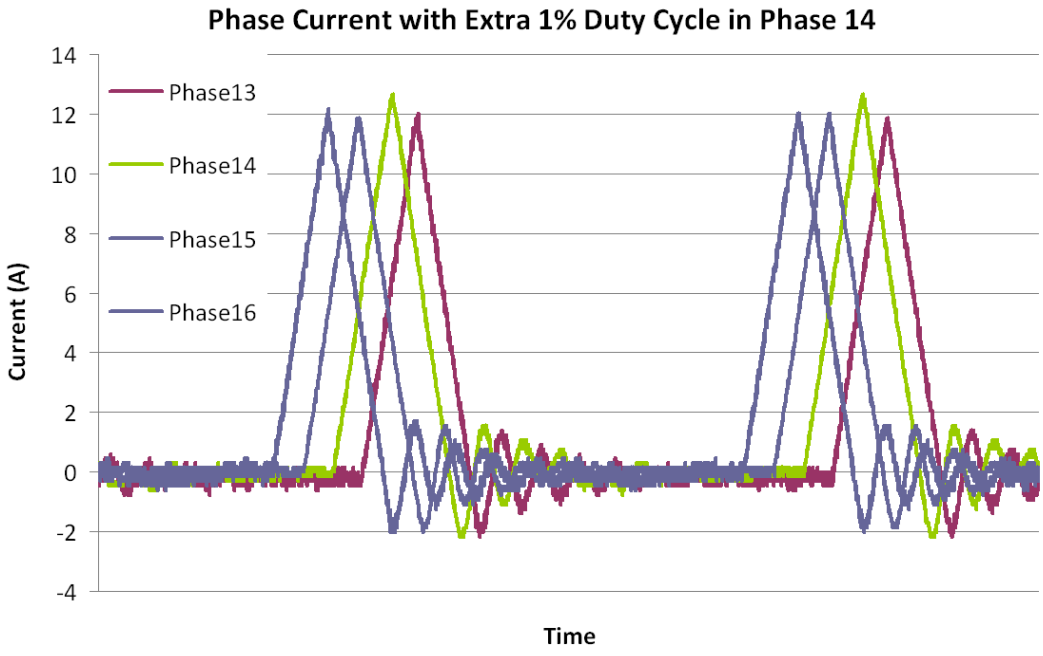


Figure 4.21 Phase current with extra 1% duty cycle in phase 14

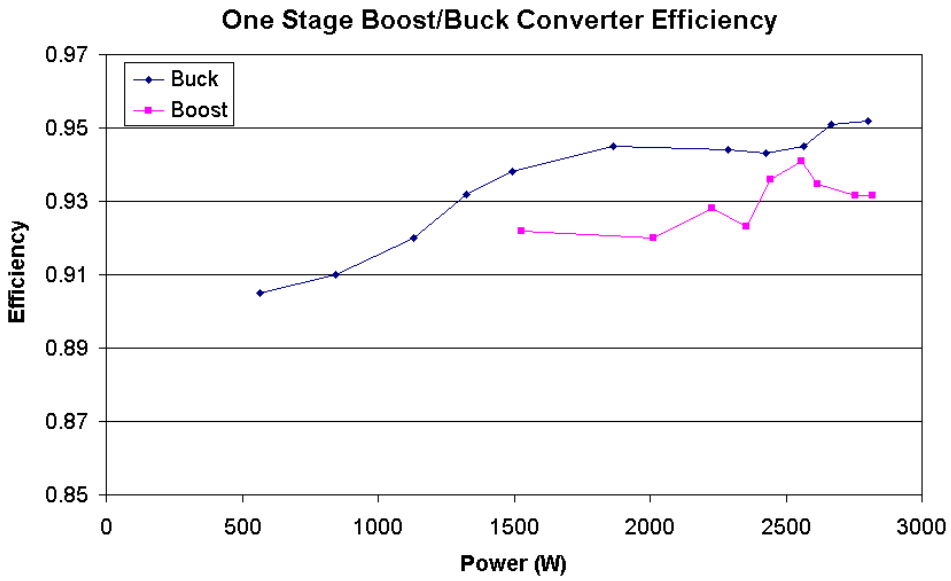


Figure 4.22 One stage boost/buck converter efficiency against input power

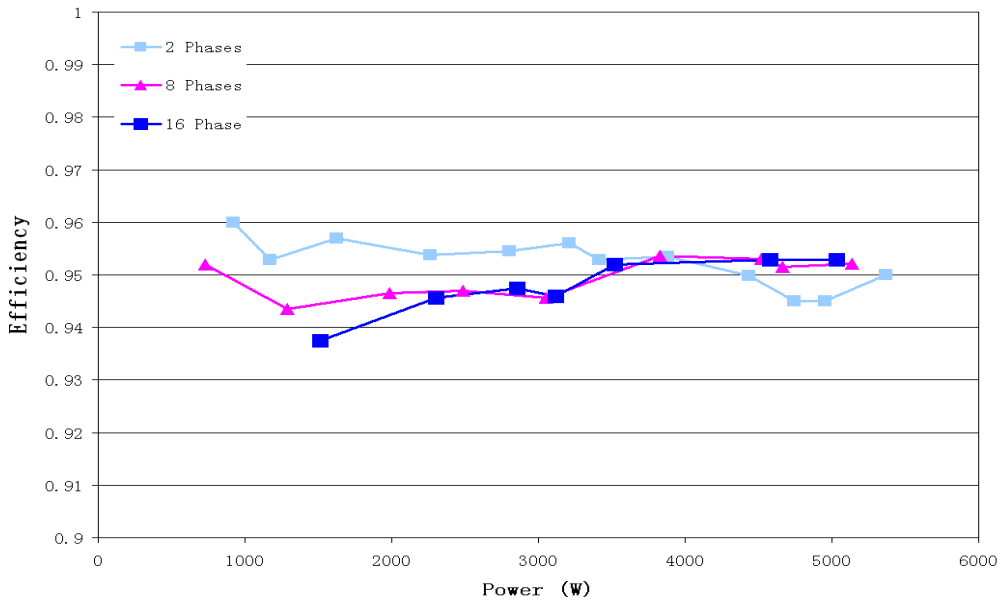


Figure 4.23 Efficiency of boost converter with 2, 8 and 16 phases against input power

The power rating for this DC/DC converter is 45 kW, so the power rating separated in each phase is 2.82 kW. Due to equipment limits, only 5.5 kW power experiment can be

carried out in the lab. The efficiency as a function of input power for one stage boost/buck converter is shown in Figure 4.22. The efficiency of buck converter is a little higher than that of boost converter. And the efficiency values for 2 phases, 8 phases and 16 phases of boost converter is shown in Figure 4.23. The efficiency for 16 phases is very high and there is a trend that the efficiency will be higher if more power were taken from it. The switch loss in this type converter is one of the major loss due to large peak current on the inductor and the high switching frequency.

One stage of boost converter with power rating has been tested and the results are shown in Figure 4.24. The low side voltage is 172 V and the high side voltage is 220 V. The peak inductor current I_L is 48.1 A. V_{ds1} is the voltage between drain and source in the low side of MOSFET. There is high voltage spike in voltage V_{ds2} due to high *di/dt* value. The efficiency for one stage boost converter is 93.2% at 2.82 kW.

The test results from one stage of buck converter with 2.8 kW power are shown in Figure 4.25. The low side voltage is 170 V and the high side voltage is 200 V. The peak of inductor current I_L is 35.9 A. V_{gs1} is the voltage between gate and source of low side MOSFET, which is estimated by Equation (4-4). V_{g2} is the gate voltage of the high side MOSFET to the ground. V_{d2} is the drain voltage of the high side MOSFET to the ground. The efficiency of one stage buck converter is 95.2% at 2.8 kW power.

Two phases of boost converter with 5.4 kW power has been test and the results are shown in Figure 4.26. The low side voltage is 172.8 V and the high side voltage is 236 V. The peak of inductor current I_L is 50.3 A. The efficiency for two-phase boost converter is 94.9%.

Eight phases of boost converter with 5.1 kW power has been test and the results are shown in Figure 4.27. The low side voltage is 172.4 V and the high side voltage is 200V. The peak of inductor current I_L is 18 A. The efficiency is 95.2%.

Sixteen phases of boost converter with 5.1 kW power has been test and the results are shown in Figure 4.28. The low side voltage is 163 V and the high side voltage is 195V. The peak of inductor current I_L is 14.22 A. The efficiency is 95.3%.

The ultracapacitors have been connected to the low voltage side of 16-phase DC/DC converter. The test result is shown in Figure 4.29. The input/output voltage and current data is collected by NI DAQ.

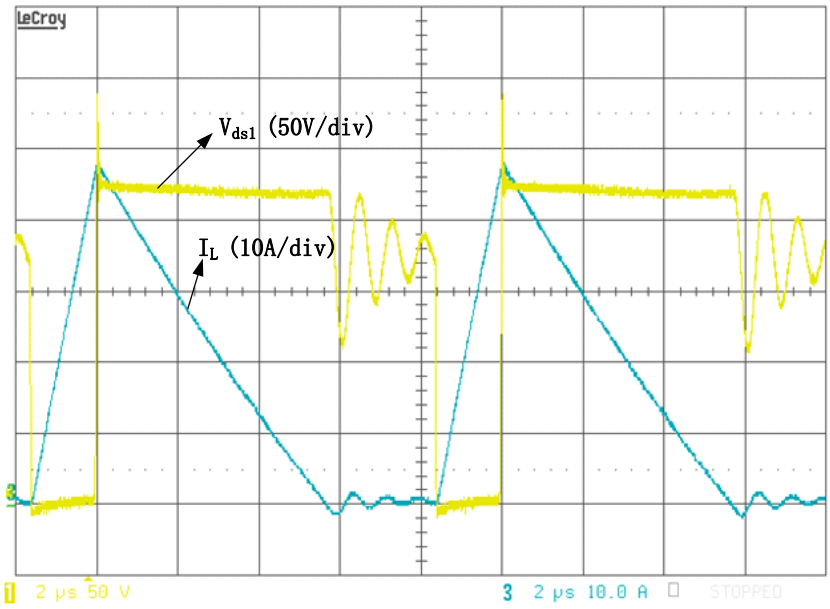


Figure 4.24 Inductor current and MOSFET voltage V_{ds1} of one phase

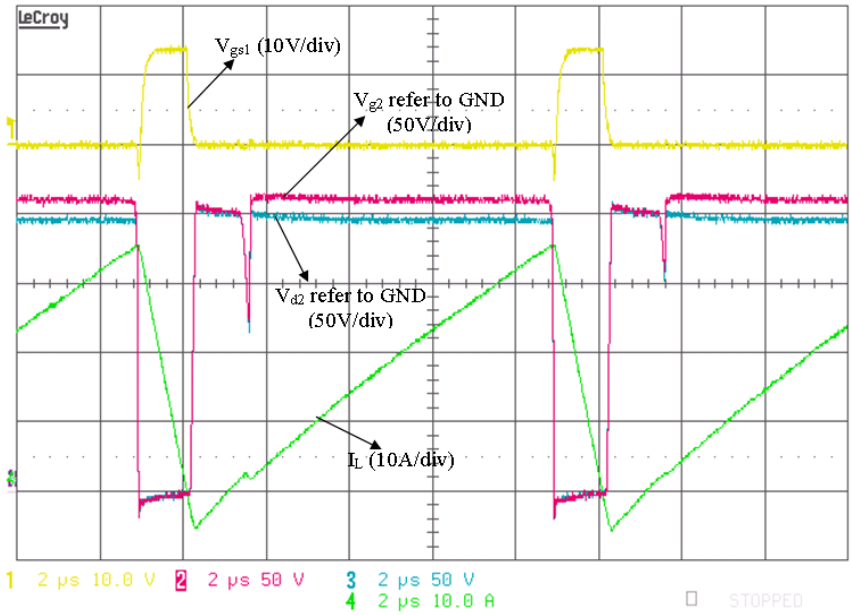


Figure 4.25 Waveforms of buck converter at rating power

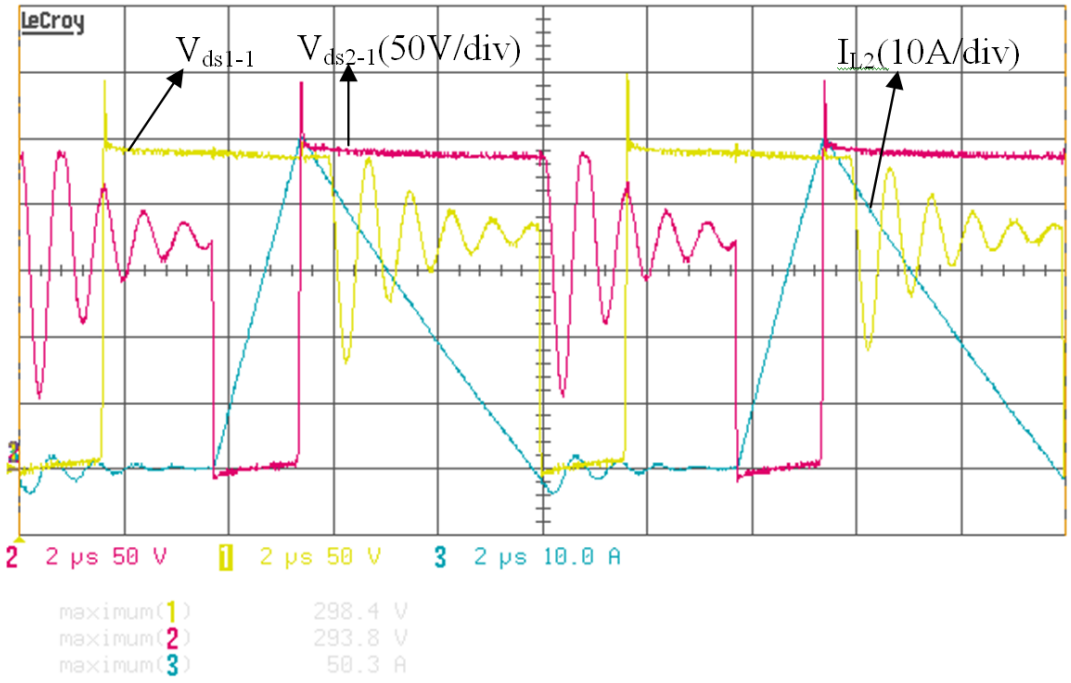


Figure 4.26 Inductor current and MOSFET voltage V_{ds1} of two-phase boost converter

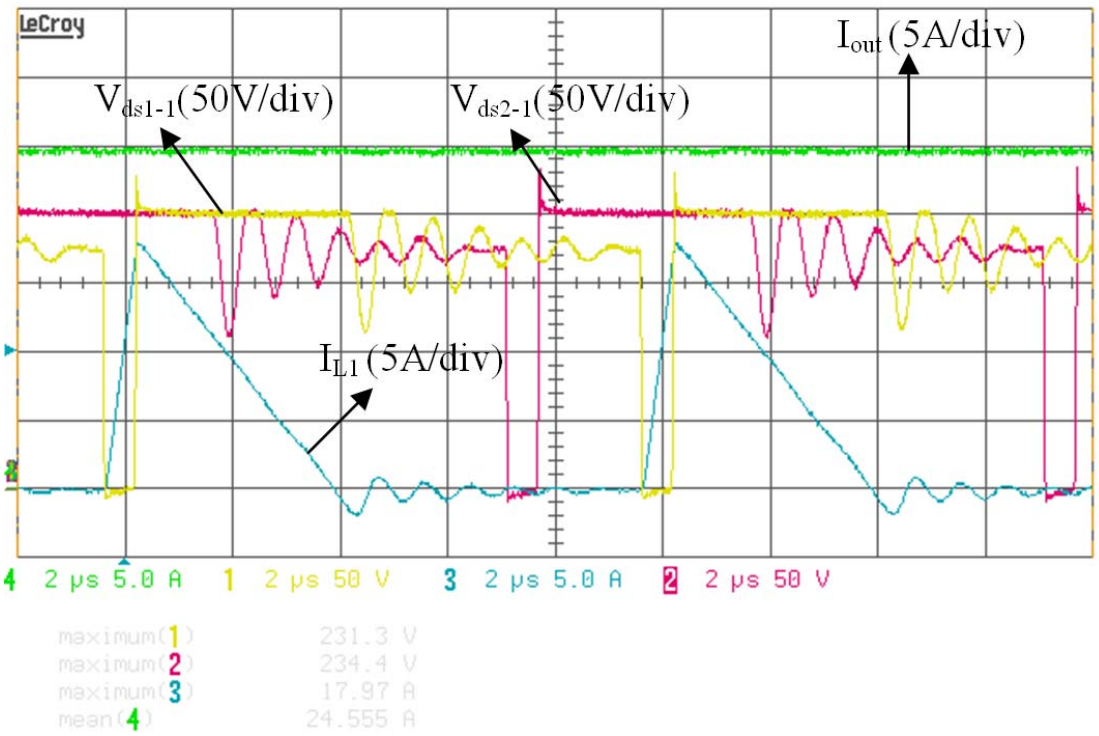


Figure 4.27 Inductor current and MOSFET voltage V_{ds1} of 8-phase boost converter

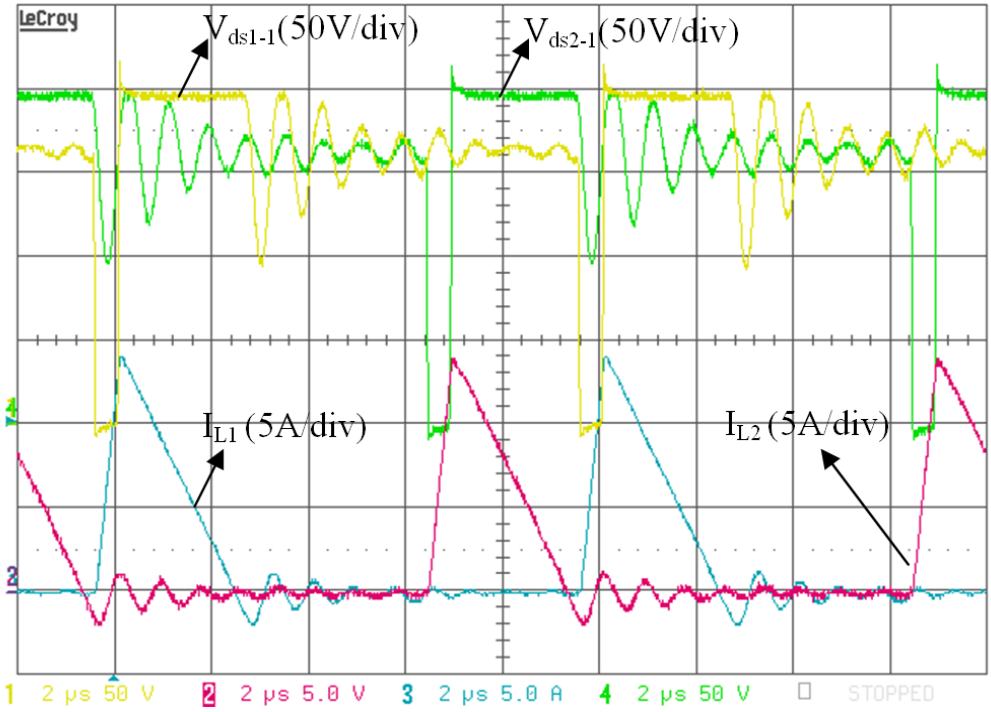


Figure 4.28 Inductor current and MOSFET voltage V_{ds1} of 16-phase boost converter

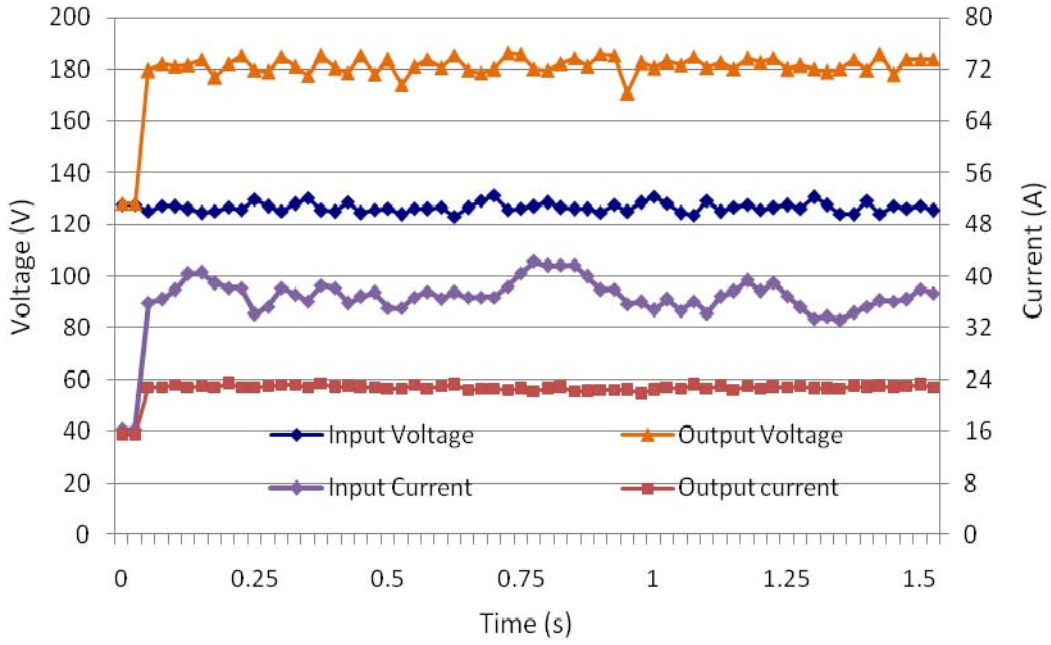


Figure 4.29 Experiment results for 16-phase boost converter connected with ultracapacitor

4.5 Conclusion

The imbalance current between phases in the proposed design based on DCM operation is small and acceptable, thus the current control loop in each phase can be removed allowing cost-effective converters with a high number of phases. Another advantage of DCM operation is that it can reduce inductance in each phase. The high current ripple in each phase associated with DCM operation can be alleviated by interleaving. By interleaving techniques, the power and current can be separated in each phase, and the device stress can be reduced. The current ripple is also reduced, particularly on the battery side which might improve the battery life time. The proposed method makes it possible to increase switch frequency and reduce filter size requirements that can benefit the smaller volume, lower cost, and higher safety. Moreover, high

efficiency can be achieved with proper design. The proposed design is generic and is also applicable for other applications.

Chapter 5.

ZVS/ZCS SOFT SWITCH FOR DC/DC CONVERTER BASED ON DCM

5.1 Introduction

DCM operation has the advantage of zero current turn-on. However, this operation significantly increases turnoff loss because the main switch is turned off at more than twice of the inductor average current. This drawback not only increases power losses but also induces current/voltage parasitic ringing. Soft switching techniques provide a solution for this problem.

DC/DC converter with soft switching techniques can achieve both benefit of switch transition control and switching loss reduction. This gives the potential to increase switch frequency and decrease filter size. The soft switching techniques have evolved from series and parallel resonant techniques (RC), quasi-resonant converters (QRC), multi-resonant converters (MRC) to soft switching PWM converters. In all the resonant converters, the output power is depended on the changing of switching frequency which makes difficult to optimally design the resonant converter elements [58][59]. Another disadvantage is that the switch current rating and/or voltage rating required is significantly increased compared with hard switch. To overcome this problem, ZVS with clamped voltage topologies was proposed in [58][60]. The disadvantage of these converters is that inductor current must be operated in CCM, which would not be a good choice for the multi-phase interleaving converter on DCM operation.

Another commonly solution is soft switch with half bridge (HB) or full bridge (FB) DC converter which have become an important research topic during recent years. A bi-directional FB DC converter uses phase shifted PWM control and adds auxiliary active clamping circuits to achieve zero-voltage and zero-current switching [61][62]. The bi-directional FB DC converter has higher cost than other topologies. It is too expensive and complex to utilize in multi-phase interleaving DC converter.

To reduce switch losses, a novel zero voltage zero current switch (ZVZCS) for bidirectional DC/DC converter based on DCM operation is proposed. An auxiliary circuit is added in each phase of the converter to achieve ZVS/ZCS PWM converter and improve efficiency. The proposed converter can operate at fixed frequency and has a very similar control system with hard switching converter. And it does not increase current rating or voltage rating on switch device. Furthermore, the Radio Frequency Interference (RFI) and Electromagnetic Interference (EMI) can be decreased by increasing switch rise and fall times (lower dv/dt and di/dt) [63][64][65].

5.2 Proposed ZVS/ZCS Topology for DCM Operation

A novel topology is proposed to achieve ZVS/ZCS for the DC/DC converter on the DCM operation, shown in Fig5.1.

A). Boost converter operation

In the boost mode, Q1 turns on under ZCS and turns off under ZVS, Q2 turns on and off under ZVS. The auxiliary switch Q3 turns on under ZCS and turns off under ZVZCS. The waveforms of boost operation are shown in Figure 5.2.

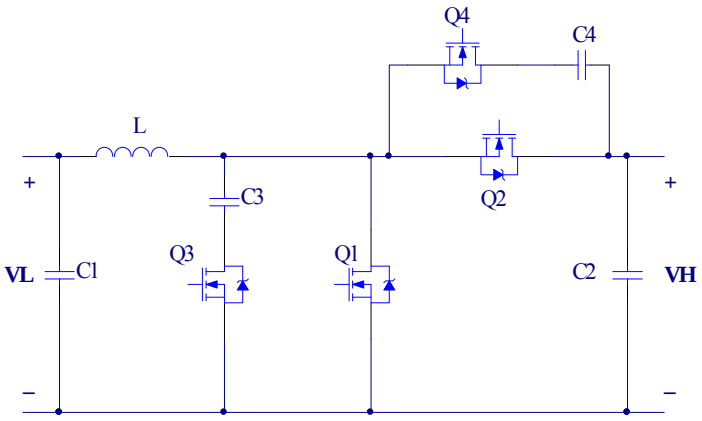


Figure 5.1 Proposed soft switch topology.

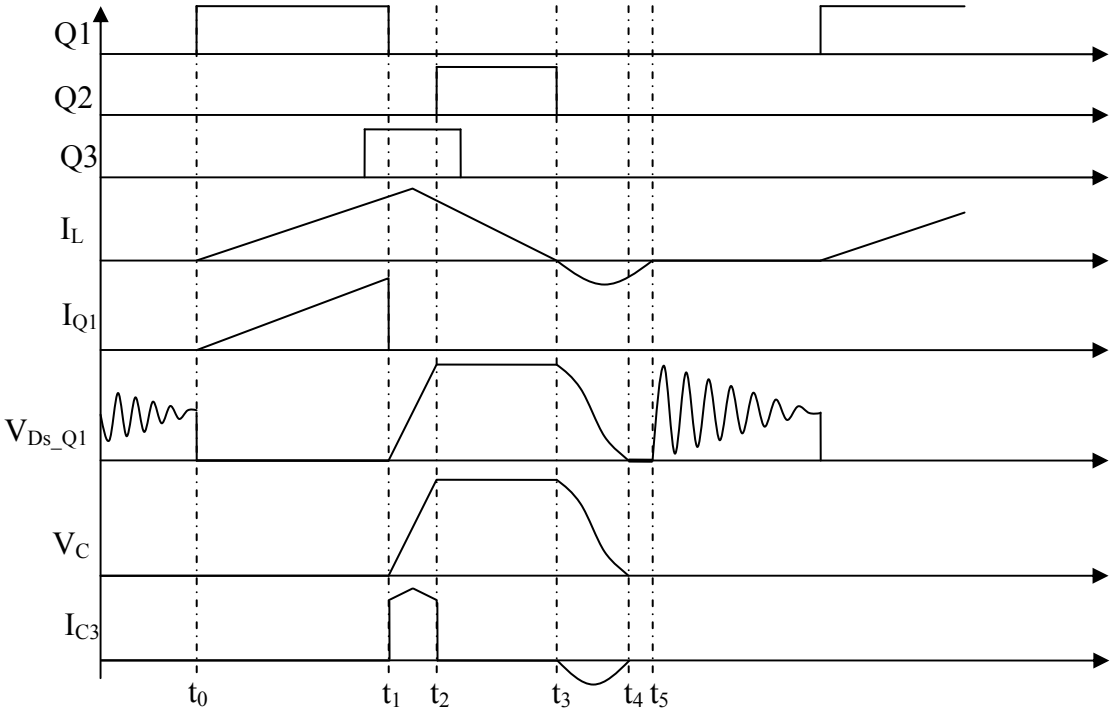


Figure 5.2 The operation waveform on the boost mode.

Mode 1 [t_0<t<t_1]: At t_0, Q1 turns on at zero current since the inductor current I_L already fall to zero before t_0. Then inductor current I_L will be increased till t_1. During this mode, the auxiliary switch Q3 turns on under ZCS. This is because no current flow auxiliary circuit since both V_{C3} and V_{DS_Q1} are kept at zero.

Mode 2 [$t_1<t<t_2$]: At t_1, Q1 turns off under ZVS and I_L charge C3 till V_{C3} reach to high side voltage VH.

Mode 3 [$t_2<t<t_3$]: After V_{C3} reach to VH, Q2 turns on under ZVS when the anti-parallel body diode is conducting. Q2 would be turned off before inductor current I_L falls to zero so that Q2 turns off under ZVS. The auxiliary switch Q3 turns off after Q2 turns on and before Q2 turns off, so Q3 turns off under ZVZCS.

Mode 4 [$t_3<t<t_4$]: Inductor current I_L falls to zero and both Q1 and Q2 keep off after t_3. The inductor L and capacitor C3 compose a series LC resonant circuit, and Q3 anti-body diode is conducting. The voltage V_{C3} is fall to zero at t_4.

Mode 5 [$t_4<t<t_5$]: V_{C3} is camped at zero, so inductor current I_L has to flow anti-parallel body diode of Q1 till I_L decrease to zero.

Mode 6 [$t>t_6$]: During this mode, inductor L and parasitical capacitor/inductor produce oscillation circuit till V_{DS_Q1} stabled at V_L or till next cycle.

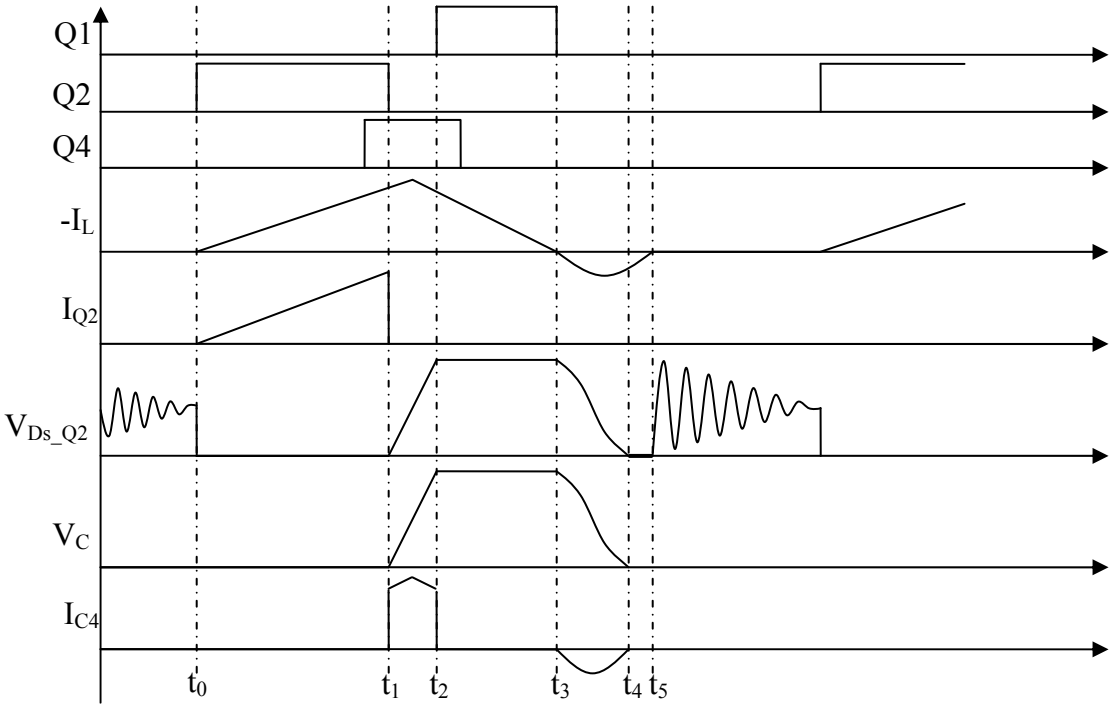


Figure 5.3 The operation waveforms on the buck mode.

B). Buck converter operation.

The operation of buck converter is very similar with boost converter. The auxiliary switch Q3 turns off all the time. And switch Q4 turns on before Q2 turns off and turns off after Q1 turns on. The circuit waveforms of buck converter are shown in Figure 5.3.

5.3 Simulation and Results

To verify the theoretical analysis of proposed topology, simulation model is built in PSpice for one stage converter using the following design specification: L = 5 μH, C3 = C4 = 47 nF and switching frequency f_s = 100kHz; VL = 90 V with R_load = 51 ohm connected to VH for boost mode operation. And VH =220 V with R_load = 11ohm connected to VL for buck mode operation. The switches used in this simulation are the model of MOSFET IRFP4242 which is built by International Rectifier Inc.

The simulation results of boost mode are shown in Figure 5.4, and the results of buck mode are shown in Figure 5.5. The inductor current I_L, main switch Q1 voltage V_{DS_Q1} and current I_{D_Q1}, auxiliary switch Q3 voltage V_{DS_Q3} and current I_{D_Q3}, and capacitor C3 voltage V_{C3} are displayed in the boost mode. The inductor current I_L, main switch Q2 voltage V_{DS_Q2} and current I_{D_Q2}, auxiliary switch Q4 voltage V_{DS_Q4} and current I_{D_Q4}, and capacitor C4 voltage V_{C4} are displayed in the buck mode.

In the boost mode, there are two different operations compared with the hard switched topology. One is the period of transition from Q1 turn-off to Q2 turn-on; and another is the period of series LC resonance (inductor L and capacitor C3) after the inductor current has reached zero. The auxiliary switch Q3 turns on before the main switch turns off, so that Q1 turns off at zero voltage due to the capacitor C3. Q3 turns off

before the high side switch Q2 turns off. After the inductor current I_L falls to zero, the inductor L and capacitor C3 compose a series LC resonant circuit, until C3 voltage V_{C3} falls to zero, and then V_{C3} will be clamped at zero. All switches in this circuit is turn on/off at zero voltage, or zero current, or both. The circuit has a similar operation in the buck converter mode.

The proposed method can improve efficiency, reduce the heat sink size for the main switch and allow reduction of both *di/dt* and *dv/dt* by increasing the gate drive resistor. Since the losses in auxiliary switches are very small, it's not necessary to use a heat sink for the auxiliary switches. This proposed method can be used for future research.

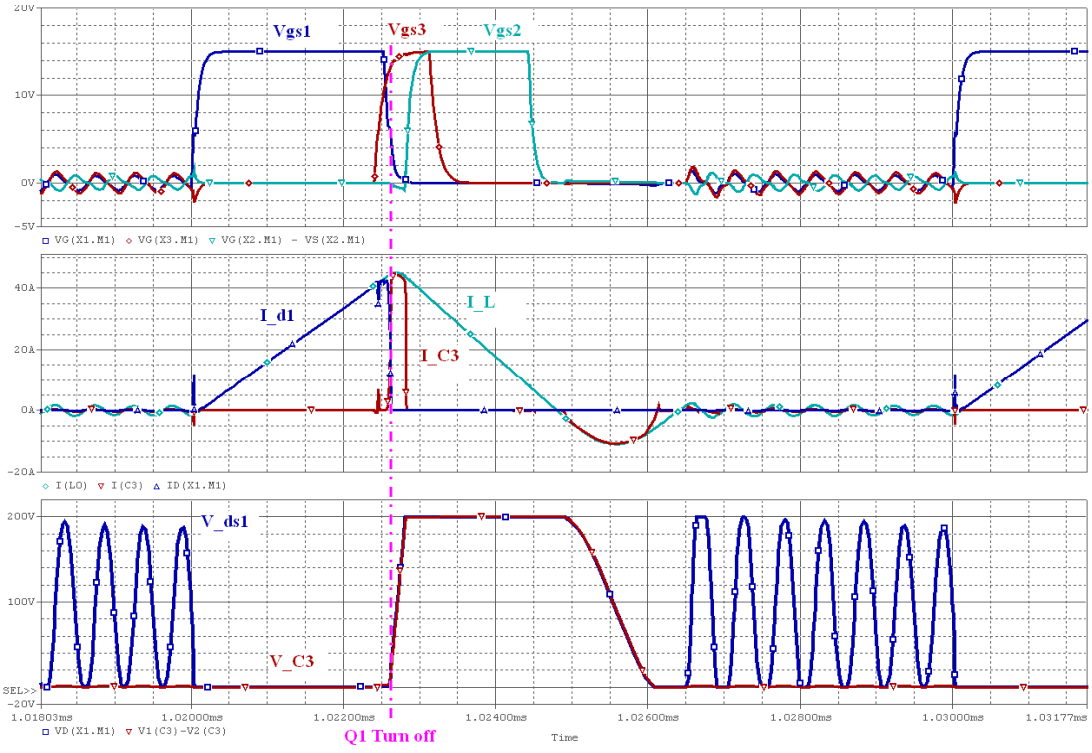


Figure 5.4 Simulation results of the boost mode

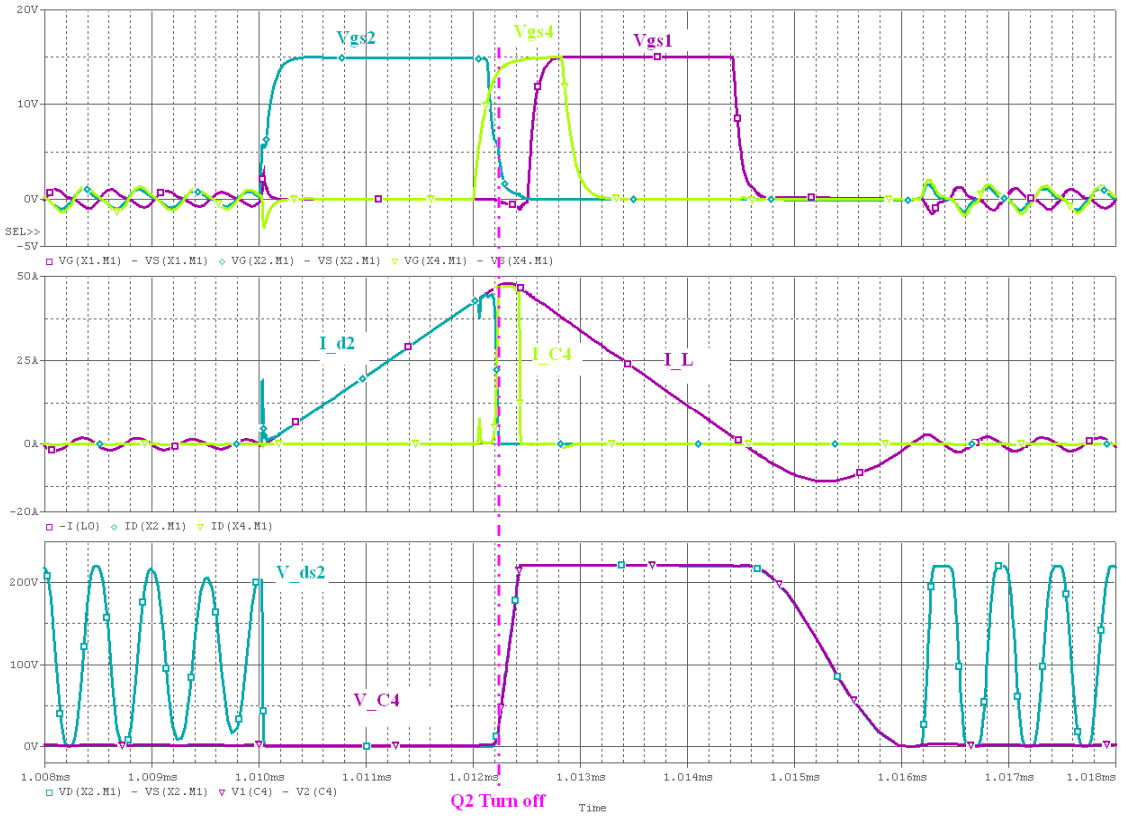


Figure 5.5 Simulation results of the buck mode

5.4 Experiment and Results

A 400 W hardware prototype is designed, built and tested to verify the proposed soft switch and evaluate its performance. A 16.8 nF capacitor and IRFP4242 MOSFET are used in the circuit. The frequency for main switch is 100 kHz. The control signal is generated by FPGA.

The result is shown in Figure 5.6 on the boost mode without any snubber and external gate resistor. Figure 5.7 is zooming in of Figure 5.6 when the main switch Q1 turns off. The input voltage is 50 V and output voltage is 120V. The efficiency is 92%. Similar operation for hard switch is also tested and compared with soft switch. Figure 5.8 and Figure 5.9 are the experiment results for hard switch topology with gate resistor 2.7

ohm. The efficiency is 91.5% for hard switch. Comparing soft switch with hard switch, the efficiency does not improve significantly. However, the spike voltage and the voltage ringing of soft switch are reduced even without external gate resistor. The noise of soft switch gate signal is also smaller than that of hard switch.

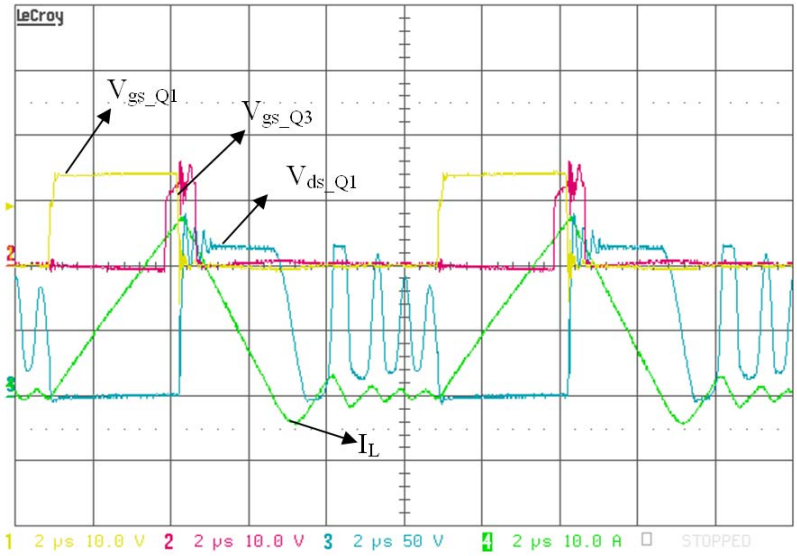


Figure 5.6 Experiment result for proposed soft switch with Rg = 0 ohm

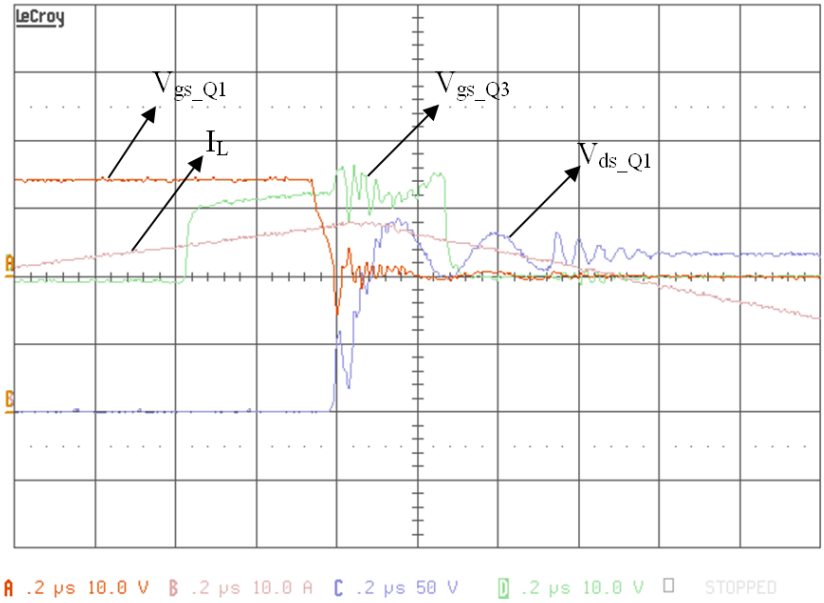


Figure 5.7 Zoom in of Figure 5.6 when Q1 turns off

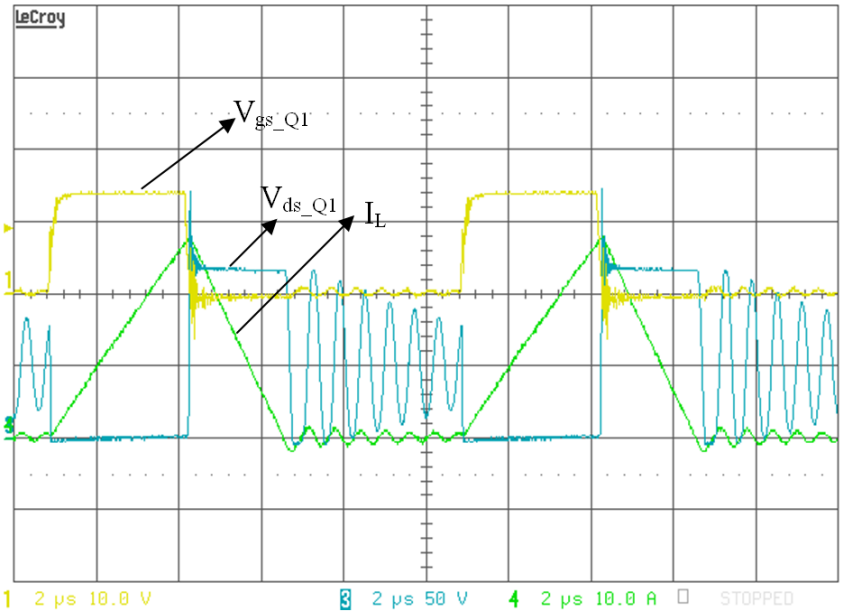


Figure 5.8 Experiment result for hard switch with Rg = 2.7 ohm

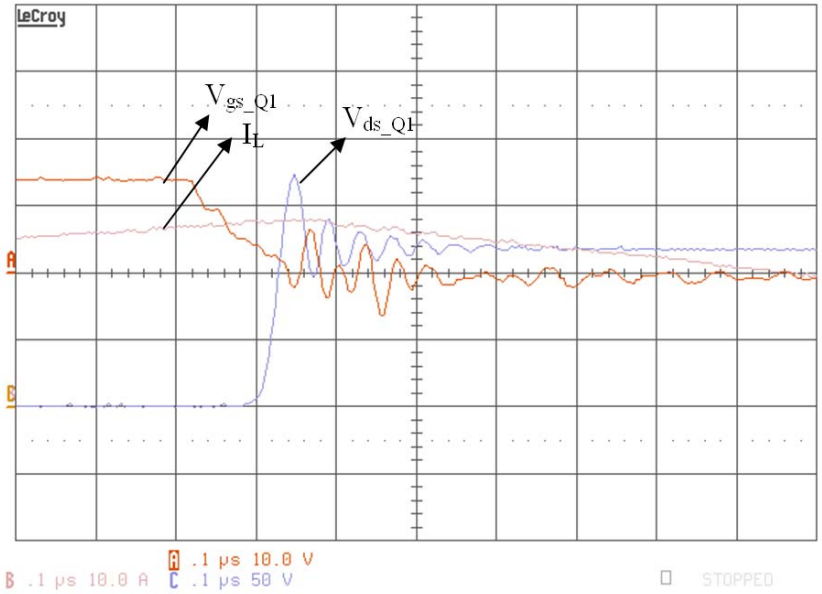


Figure 5.9 Zoom in of Figure 5.8 when Q1 turns off

5.5 Conclusion

The simulation results and experiment results of proposed soft switch topology match well with the theory analysis. The control system is simple and similar with hard switch. The proposed method can reduce switch loss and improve efficiency which

makes it possible to increase frequency and reduce heat sink for the main switch. It's not necessary to use a heat sink for auxiliary switch since the losses in it are small enough. The EMI is also reduced since the spike voltage and ringing voltage are reduced. The limitations of proposed method are that it only works for DCM operation and the ratio of high side voltage and low side voltage should be larger than 2. However it is still worth to apply proposed soft switch in multi-phase interleaved converter for some special applications, such as 14-V/42-V power converter in automobiles.

Chapter 6.

A NOVEL BATTERY CHARGER DESIGN

6.1 Introduction

Compared with traditional HEV technology, one of the most promising features of plug-in HEV is that PHEVs have a high capacity battery pack which can be recharged from power grid. The full exploitation of the battery capacity and the respect of the nominal lifetime are strongly influenced by the characteristics of the battery charger. Thus the smart charger for PHEVs becomes a valuable topic.

The prime requirement for the battery system is that provides a rapid and efficient charge without damage to the battery. The common charging strategy is constant-current/constant-voltage (CC-CV) [66][67]. The first charging phase is at constant current and with the battery voltage progressively rising. As soon as the battery voltage reaches the trickle level, the constant-voltage charging method should be applied, with the charging current progressively falling down to cut-off current [68]. Since the power of the battery charger for EV or PHEV is mostly larger than 1 kW, the AC current supplied by the distribution system must respect the international standards of high power factor and low harmonics distortion [69]. The power factor correction (PFC) has to be considered in the charger system to decrease the impact to power grid. Different battery charger circuits with PFC have been published [68][70][71][72]. In generally, the battery charger includes two stages: one stage is a boost converter to achieve PFC function; another stage is a dc/dc converter to achieve CC-CV charging control.

This chapter is proposing a boost converter to achieve both PFC and battery charging control simultaneously. Single stage charger is reducing the switch devices and simplifying the control system that would also decrease the cost and minimize the size of charger. Figure 6.1 shows the schematic diagram design for the battery charger. The control system includes voltage controller, outside current controller and inside current controller. These controllers determine a gate signal for MOSFET switch finally according to the rectified voltage from power grid and the inductor current.

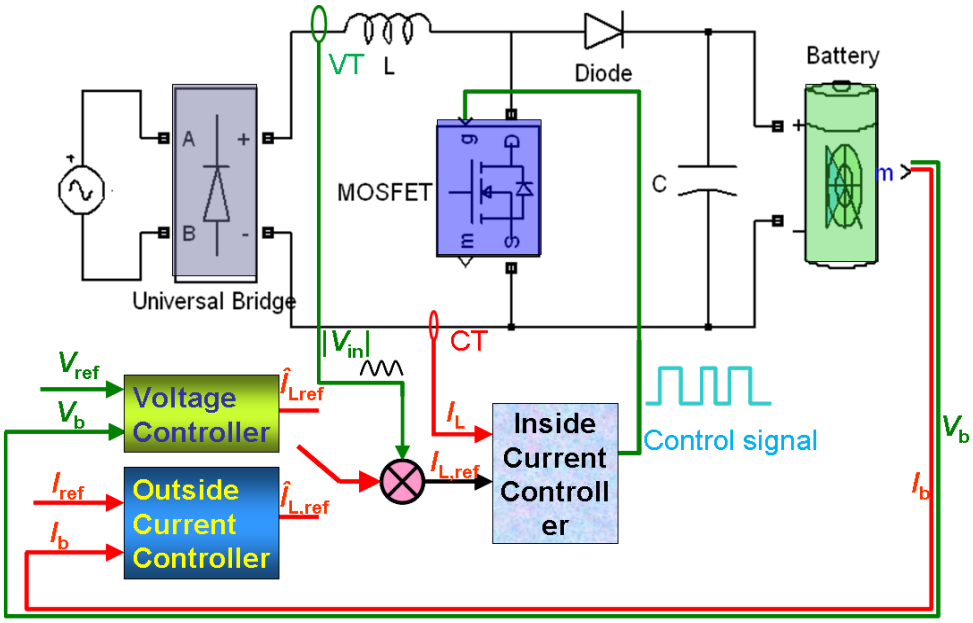


Figure 6.1 Schematic diagram of battery charger circuit

6.2 Three Control Loops Design

The operating principle of a commonly used single-phase PFC is shown in Figure 6.2, where, between the utility supply and the battery bus, a boost DC/DC converter is introduced. This boost converter consists of a MOSFET, a diode, and a small inductor L.

Using the average model of the boost converter as shown in Figure 6.3 and neglecting a small voltage drop across the inductor [73],

$$\frac{V_d}{|v_s|} = \frac{1}{1-d(t)} \tag{6-1}$$

Thus,

$$d(t) = 1 - \frac{\hat{V}_s |\sin(\omega t)|}{V_d} \tag{6-2}$$

The switch duty ratio is plotted in Figure 6.4. The output current can be calculated from ideal transformer:

$$\bar{i}_d(t) = (1-d)\bar{i}_L(t) = \frac{\hat{V}_s}{V_d}\hat{I}_L |\sin(\omega t)|^2 \tag{6-3}$$

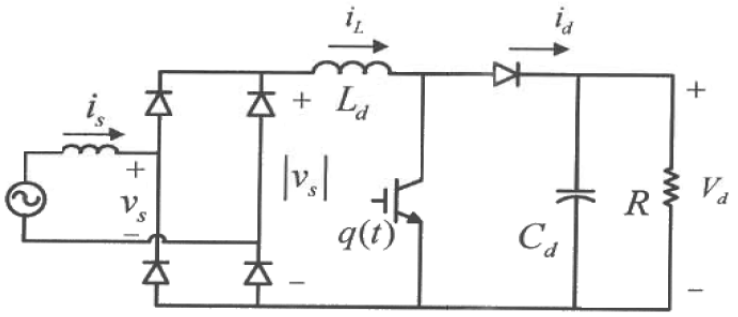


Figure 6.2 Single-phase PFC circuit

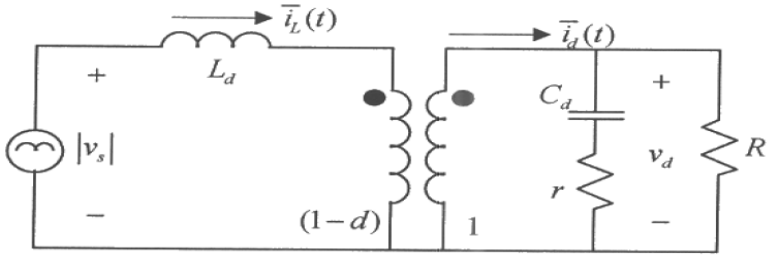


Figure 6.3 Average model of PFC circuit

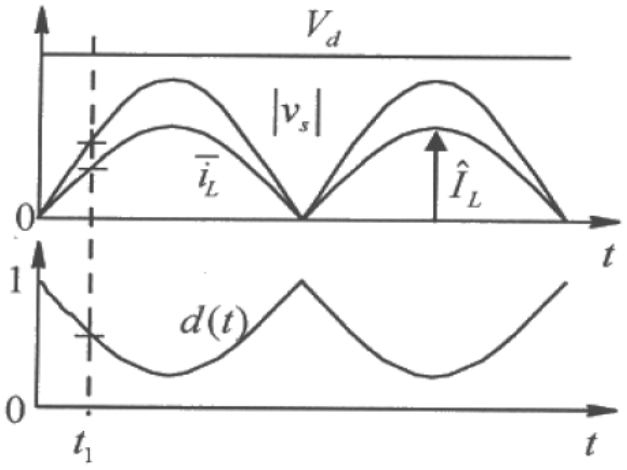


Figure 6.4 PFC circuit waveforms

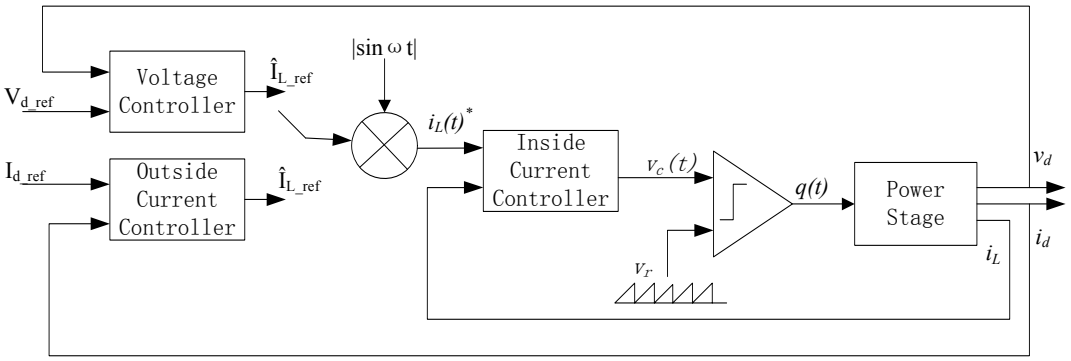


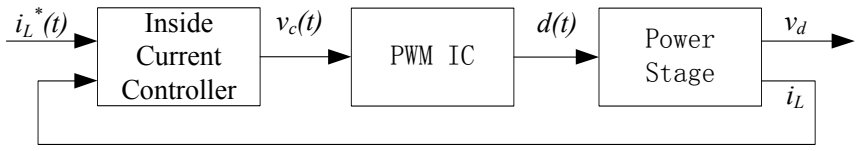
Figure 6.5 Battery charger control loops with PFC

In controlling a PFC, the main objective is to draw a sinusoidal input current, in-phase with the utility voltage. In the charging control, the main objective is to draw a constant output current during CC charging, or to regulate a constant output voltage during CV charging. These objectives lead to three control loops, as shown in Figure 6.5, to pulse-width modulate the switch of the boost converter: the inside current control loop, outside current control loop and voltage control loop.

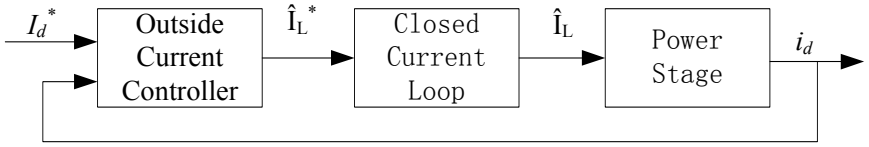
The inside current control loop ensures the form of $i_L^*(t)$ and is shown in Figure 6.6 (a). An average current mode control is used with a high bandwidth, where the error between the reference and the measured inductor current $i_L(t)$ is amplified by current controller $G_i(s)$ to produce the control voltage $v_c(t)$. A PID controller is adopted for $G_i(s)$ according to the transfer functions of power stage and PWM IC. The control voltage $v_c(t)$ is compared with a ramp signal with a peak of V_{r_pk} at PWM IC. The PWM IC and power stage transfer functions are:

$$\frac{\tilde{d}(s)}{\tilde{v}_c(s)} = \frac{1}{V_{r\_pk}} \tag{6-4}$$

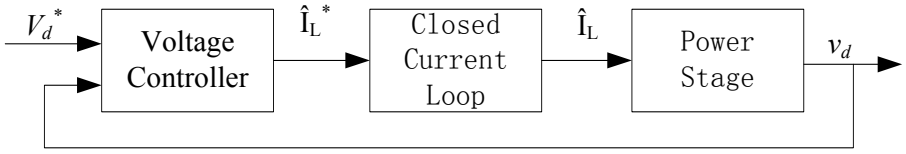
$$\frac{\tilde{i}_L(s)}{\tilde{d}(s)} = \frac{V_d}{sL} \tag{6-5}$$



(a) Inside current control loop



(b) Outside current control loop



(c) Voltage control loop

Figure 6.6 Three control loops

The outside current control loop determines the amplitude $\hat{I}_L$ of $i_L^*(t)$ based on the output current (battery charging current) feedback. By comparing the output current with reference current, the current control loop adjusts the inductor current amplitude to bring the output current to its reference value. The closed current loop transfer function is equal to 1. The power stage transfer function is:

$$\frac{\tilde{i}_d(s)}{\tilde{\hat{I}}_L(s)} = \frac{\hat{V}_s}{2V_d} \tag{6-6}$$

The operation of voltage control loop is similar with outside current control loop, shown in Figure 6.6 (c). The power stage transfer function is:

$$\frac{\tilde{v}_d(s)}{\tilde{\hat{I}}_L(s)} = \frac{\hat{V}_s}{2V_d}\frac{R}{1+sRC} \tag{6-7}$$

A simply PI controller can be adopted for both outside current controller and voltage controller in the charging system.

6.3 Charger Simulation Model and Results

The battery pack used in this project is composed by 64 Li-ion cells connected in series. The individual capacity of each cell is 25 Ah and the nominal voltage is 3.7 V. The total energy is 5.92 kWh for the whole battery pack. The standard charging current for this battery pack is 0.2 C (5 A), and the quick charging current is 0.5 C (12.5 A). The charger utilizes a common charging strategy: constant-current/constant-voltage (CC-CV). At beginning of charging, the charger works on the constant current charging operation until the battery pack voltage rise to 268 V (64*4.2), then the charger transit to the

constant voltage charging operation until the charging current falls to lower than the cut-off current (0.05C).

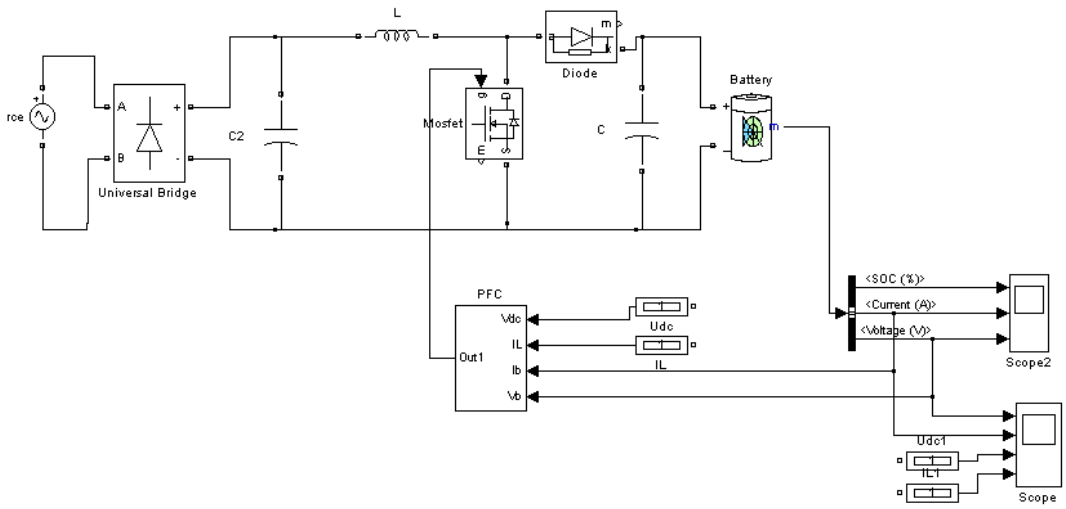


Figure 6.7 Battery charger simulation circuit based on MATLAB Simulink

The charger simulation model is built based on the MATLAB Simulink, shown in Figure 6.7. The PFC subsystem includes these three control loops mentioned above. The reference of constant charging current is set to 5 A and constant charging voltage is set 268 V. The power absorbed from the single phase AC supply has a large 120 Hz component that cannot be accumulated by a small output capacitor. Thus, a large output capacitor 20 mF is applied in this simulation model. The output capacitor rating is influenced by the systems hold up requirements and the maximum RMS current rating. The hold-up time should be the time of half cycle at least. In generally, the capacitance value is greater than the minimize size and should provide a holdup time of one full cycle [56]. In this simulation, in order to reduce 120 Hz component in the charging voltage/current, the output capacitor is much greater than the minimize size.

The capacitance required for a given hold-up time is given by [57]:

$$C_{out} = \frac{2 \cdot P_{out} \cdot t_{hold-up}}{V_{out}^2 - V_{out\_\min}^2} \tag{6-8}$$

The simulation results for the constant charging current operation are shown in Figure 6.8. The battery voltage is 252.2 ± 0.32V; battery charging current is 5 ± 0.5 A, and power factor (P.F.) is as high as 0.99. The results for the constant charging voltage operation are shown in Figure 6.9. The battery voltage is reach to 268V, the charging current is 3.6 ± 0.37 A, and P.F. is ~ 0.99. Figure 6.10 is the battery charging transit state from CC charging to CV charging.

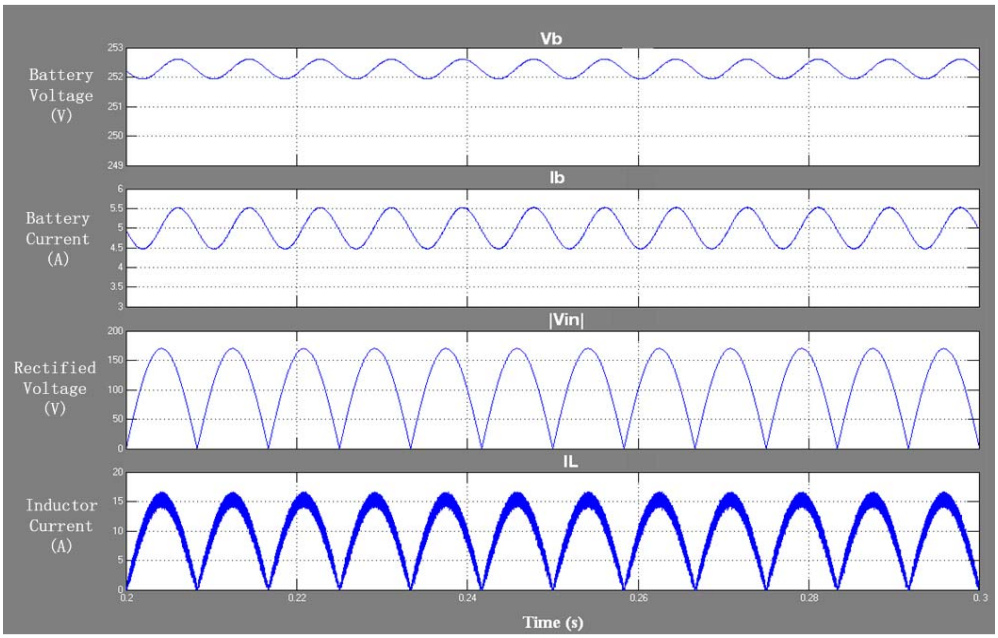


Figure 6.8 Simulation results of battery charger during CC charging

From the simulation results, the power factors are close to 1 on both CC charging and CV charging. The charging current/voltage is matching well with the reference current/voltage. The simulation results validate the feasibility of the proposal charger system. The drawback is this charger need a large filter capacitor connected to battery pack so that the battery can be charged with low current ripple. The 120 Hz current ripple

is still remarkable even using a large capacitor. The output capacitor makes up a significant portion of cost and volume in the charger system.

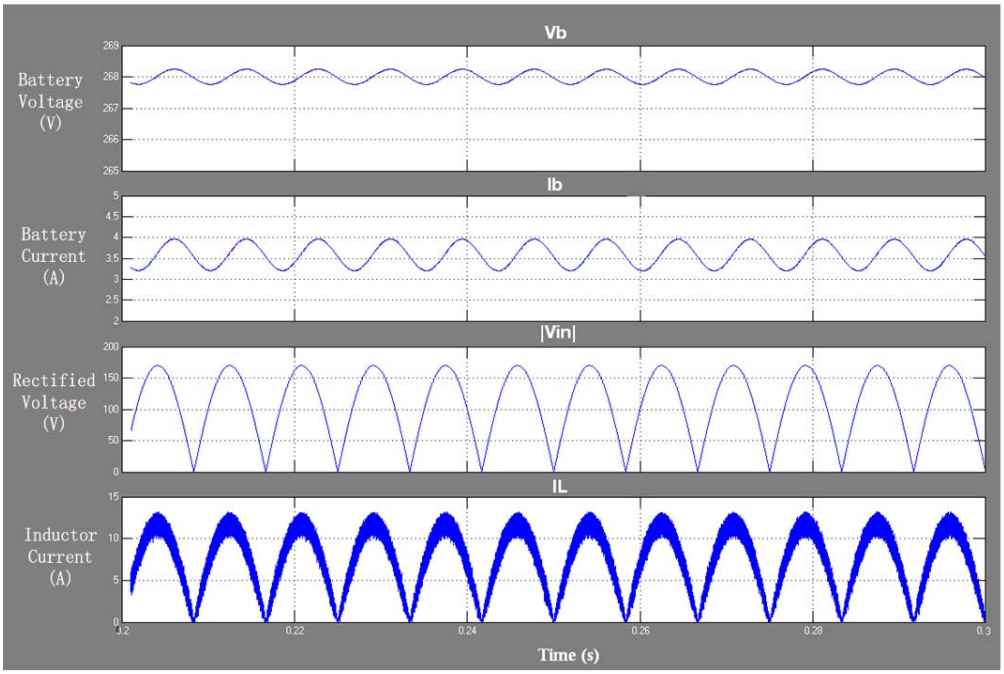


Figure 6.9 Simulation results of battery charger during CV charging

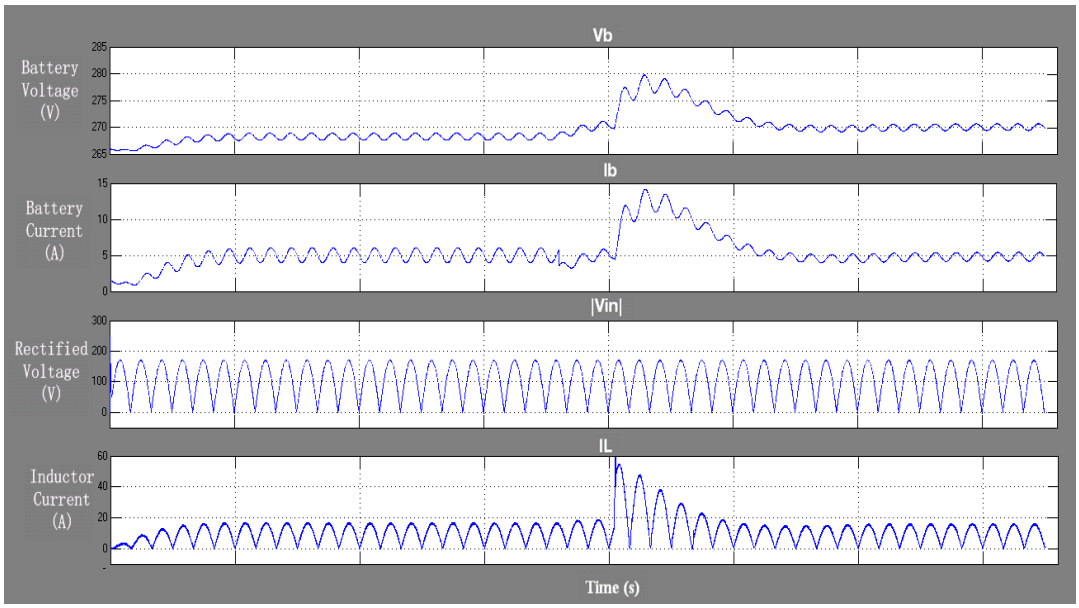


Figure 6.10 Transit from CC charging state to CV charging state

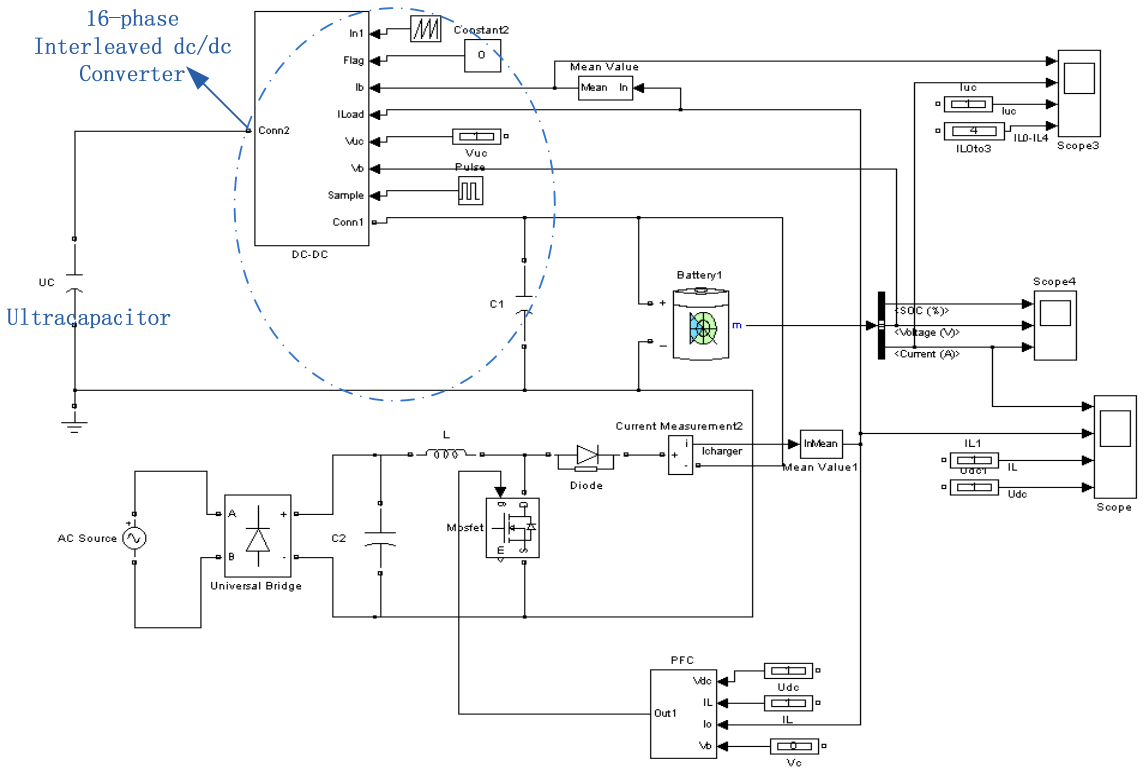


Figure 6.11 Modified charger circuit utilizing ultracapacitor as filter capacitor

6.4 Modified Charger by Utilizing Ultracapacitor

As stated in last section, the charger needs a large filter capacitor to reduce 120 Hz component, which would increase the cost and the volume significantly. A modified charger system is proposed in this section by utilizing the ultracapacitors and the 16-phase interleaved dc/dc converter which is connected between ultracapacitor pack and battery pack, so that the current ripple can be filtered by ultracapacitors and the capacitor size can be reduced significantly or removed. The modified charger circuit is shown in Figure 6.11. The output capacitor in the charger system is removed (a small capacitor already exists in the 16-phase DC/DC converter system), and the battery pack is connected with ultracapacitors through a 16-phase interleaved dc/dc convert. The 16-

phase interleaved dc/dc converter has been described detail in Chapter 4. When the battery charging current/voltage is larger than the reference signals, the DC/DC converter works on the buck mode and the ultracapacitors absorb extra charging power. When the battery charging current/voltage is smaller than the reference signals, the DC/DC converter works on the boost mode and the ultracapacitors supply extra power to charge the battery.

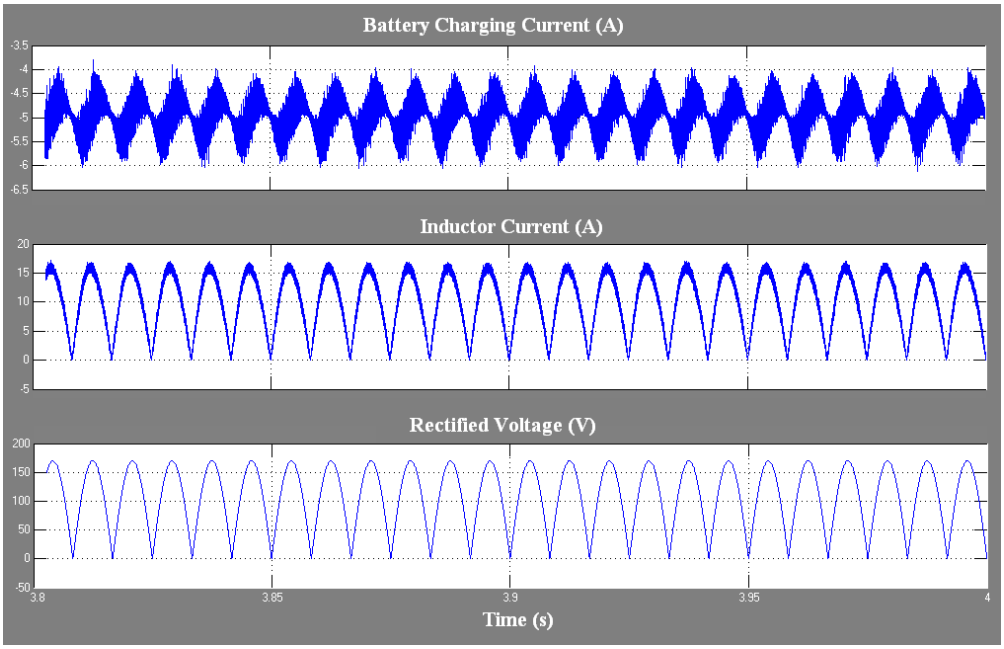


Figure 6.12 Simulation results for modified charger circuit

Figure 6.12 shows the simulation results for the modified charger circuit. The battery charging current is 5 ± 1 A. The current ripple is acceptable when the large output capacitor is removed. There is some high frequency harmonics in the current which is induced by the high frequency DC/DC converter connected between ultracapacitors and batteries. Power factor is still around 0.99. Figure 6.13 shows the currents in the battery, ultracapacitor and the phase currents in DC/DC converter. When the battery charging

current is larger than 5A, the ultracapacitors will be recharged; when the battery charging current is smaller than 5A, the ultracapacitors will be discharged.

As shown in simulation results, the ultracapacitors through a DC/DC converter can replace a large output capacitor to achieve the filter function that would reduce the cost and the volume significantly in the whole system since both ultracapacitors and DC/DC converter are already existed.

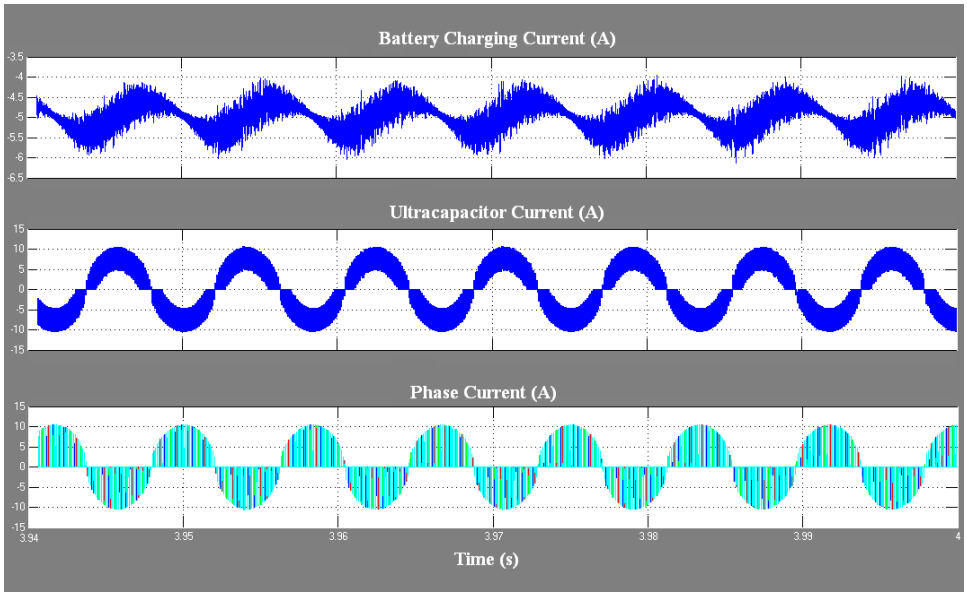


Figure 6.13 The results of battery current, ultracapacitor current and phase current in dc/dc converter

6.5 Conclusion

An economical single stage AC/DC topology with power factor correction is proposed for battery charger system. Operation, features and practical values of the proposed approach are illustrated and verified by the simulation model. However, the battery current has a significant 120 Hz component which requires a large capacitor to

filter. Therefore, a novel modified battery charger is proposed to reduce capacitor significantly by utilizing ultracapacitor and DC/DC converter as filter function since they are already existed in the system and won't increase any additional cost but reduce the whole system volume. A simulation based on MATLAB Simulink has been built to verify the proposed method. It is worth to build hardware prototype for the future research.

Chapter 7. SUMMARY

An energy storage system design has been discussed in detail, from the selection of energy devices, evaluation of energy storage size, determining power flow control among different energy sources, to the design of associated power electronics. The aim of this dissertation is to develop an advanced energy storage system for a small plug-in HEV whose performance can approach very closely to the optimal possible, in terms of energy efficiency, peak power, cost and volume.

The size of energy storage would impact hybrid vehicle performance directly. To get more realistic results, a model for evaluating the energy size is studied based on a real driving test around Lincoln city which included the entire road feature and vehicle speed. A dual-source (battery and ultracapacitor) energy storage system is chosen to improve battery life cycle, reduce the cost and size, while getting high power rating. The dual-source energy storage system combines higher power performance of the ultracapacitor with greater energy storage capability of the battery. The power flow control strategy among different sources is studied to achieve the best performance. A simulation model is built to validate the control strategy.

The power electronics design including battery charger, power converter between ultracapacitors and batteries, and circuit protection has been presented. A 16-phase interleaved bidirectional DC/DC converter is proposed to connect between battery pack and ultracapacitor pack. The proposed DC/DC converter has the feature of smaller input/output filters, faster dynamic response and lower device stress. This converter works on DCM in order to minimize the imbalance current and remove the current

control loop in each phase which can simplify the control system and reduce the converter cost. The high current ripple associated with DCM operation is alleviated by 16-phase interleaving. The design, construction and testing of hardware prototype with 45 kW power rating is presented. The experimental results show that this converter has high efficiency and low imbalance current. The current ripples at both low side and high side of the converters are small, even with the using of small capacitors only. Also, a ZVS/ZCS soft switching topology is proposed for the 16-phase DC/DC converter to reduce the switching losses and improve efficiency.

A single stage charger without large output capacitor is proposed, which utilizes the existing ultracapacitor through this DC/DC converter as filter capacitor instead of a large output capacitor. The cost and volume are decreased significantly by removing the large capacitor. The simulation model is built to verify the proposed method.

In the future research, the number of phases in the multi-phase DC/DC converter should be optimized according to energy efficiency, cost and size. The EMI and noise in the circuit should be analyzed in order to reduce the effect between phases and improve circuit reliability. The proposed multi-phase DC/DC converter can also be applied in other application, especially for high current applications. Dual-source energy storage system with a DC/DC converter can not only be used in hybrid vehicles, but also applied in other applications. Following are brief examples of potential application of the dual-source energy storage system with a DC/DC converter:

1. Interface of renewable energy system and grid system

Because of the intermittent characters of some renewable energy system, such as Wind and Photovoltaic, energy storage system is necessary to be applied. The

developed dual-source energy storage system with a DC/DC converter can be applied in the interface of the energy storage system and grid system, to absorb/release high power while decreasing the magnitude of spike voltage and currents.

2. Power quality improvement

The developed system can also be applied in power supply system, such as Uninterrupted Power Supply (UPS), for battery management. With UC used, the system can improve the capacity of the power that can be delivered or absorbed, compared with traditional UPS system

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