Fall 12-6-2013

Physical Design of a Smart Camera with Integrated Digital Pixel Sensors Using a 0.13μm 8-Layer Metal CMOS Process

Mahir K. Gharzai
University of Nebraska-Lincoln, mkgharzai@gmail.com

PHYSICAL DESIGN OF A SMART CAMERA WITH INTEGRATED DIGITAL PIXEL SENSORS USING A 0.13 µm 8-LAYER METAL CMOS PROCESS

by

Mahir Kabeer Gharzai

A THESIS

Presented to the Faculty of

The Graduate College at the University of Nebraska

In Partial Fulfilment of Requirements

For the Degree of Master of Science

Major: Electrical Engineering

Under the Supervision of Professor Sina Balkir

Lincoln, Nebraska

December, 2013

PHYSICAL DESIGN OF A SMART CAMERA WITH INTEGRATED DIGITAL PIXEL SENSORS USING A 0.13 µm 8-LAYER METAL CMOS PROCESS

Mahir Kabeer Gharzai, M.S.

University of Nebraska, 2013

Adviser: Sina Balkir

The design of cameras has historically kept imagery and computational circuitry isolated in an attempt to maximize image quality by improving pixel pitch and routing density. Although this technique has worked in creating high density arrays of pixels for large resolution imagers, it has never been able to achieve high framerate computational operations.

A radical approach is introduced to solve this dilemma by creating compact, low-power pixel elements with built-in analog-to-digital converters that directly interface with digital logic. These pixels are capable of integrating alongside logic cells and to create an array of pixels inside the processor that can capture a scene and perform operations across the entire image in parallel. Minimization of electronic circuitry is explored to design exotic miniature logic cells to further compact the design and optimize imaging quality.

Contents

List of Figures

Chapter 1

Smart Camera History

1.1 What is a Smart Camera

CMOS imaging arrays are silicon circuits that utilize structures on the substrate to convert photons to electric current. These structures contain readout circuitry to be able to interface with other portion of the chip, sometimes including converters or buffers. The combination of these is known as a pixel. CMOS technology has allowed other circuit elements to be placed alongside an array of pixels to perform a variety of operations such as compression, dynamic range adjustment, and object recognition. When such electronics are integrated directly onto silicon to perform processing operations in-chip, the camera is considered a Smart Camera.

1.2 Chip-Level Imagers

The original technique for adding processing power to an imager array was to integrate processing circuitry separate, but nearby an imaging array. The processing circuitry was able to process data across the entire array of pixels but had to read

each value sequentially, slowing down operation. The flexibility of being able to program the processor to do a variety of operations was its primary appeal, even if high framerate operations were not possible. In addition to speed constraints, the chip-level processing paradigm suffered from scalability issues. As imager sizes increased, processing speeds began to suffer due to the single processor having to manipulate data for an increasing amount of pixels. Framerates for simple operations remained limited to hundreds of frames per second. Computationally expensive operations, such as compression, were limited to tens of frames per second.

1.3 Column-Level Imagers

As technlogies started to get more compact, around 0.25 µm and 0.18 µm, smaller feature sizes allowed simple circuitry to become embedded nearby pixels in the array. Simple computational operations requiring few transistors for functionality could be integrated at the row or column level of the imaging array to provide fast computation during readout [8]. Processing flexibility was lost due to having these operations hardcoded into the circuit, but processing speeds began to see an improvement. It was now possible to process data in the thousands of frames per second [2].

1.4 Pixel-Level Imagers

The final architecture explored in imaging arrays used in specialized applications embedded processing directly into pixels themselves. Technologies using feature sizes of 0.13 µm and below were finally able to include circuitry compact enough to fit in the array without increasing pixel pitch enough to destroy imaging quality. Pixel-level imagers sacrificed imaging quality for the pursuit of ultimate processing speed. Simple

operations achieved framerates in the tens of thousands of frames per second. Like the column-level processing architecture, pixel-level processing was also inflexible. Instructions had to be hardcoded and resulted in imagers that could only do a handful of tasks at incredible speeds [10].

Chapter 2

A Massively Parallel Smart Camera

2.1 The Neighborhood Processor

In the work of a previous graduate student, Anantha Nelliparthi, a processor architecture was designed which could perform parallel operations and communicate with other processors in a neighborhood array [3]. The advantages from the chip, column, and pixel-level processing architectures were combined to create a flexible, high framerate imager with acceptable image quality. Each neighborhood processor (NP) contained 64 pixels and could perform a variety of operations in parallel across this small array. An array of NP's could be created of any size without sacrificing speed, due to the parallelism of the design.

The design was verified on an FPGA platform demonstrating several imaging operations across the pixel array that showed promise of the NP's potential. In this work, the NP design is fully implemented in a 0.13 µm silicon technology to create a novel Smart Camera.

2.2 Migrating to Silicon

2.2.1 Pixel Sensors

The most fundamental step in pixel design involves the method of sensing photons at the silicon level. An established technique for this conversion is to charge a capacitance to a reset voltage and allow it to decay. The natural loss of the voltage across the capacitance from tunneling effects is modeled as a current, known as dark current. When photons collide with one of the surfaces of the capacitor they will cause more loss of the voltage across the capacitance due to recombination effects. This drop in voltage is modeled as a current as well, known as photocurrent. By monitoring the photocurrent across the capacitors of the pixel array, we can obtain an image and deduce brightness levels for each pixel.

The two techniques used in detecting this photocurrent involve different methods of creating the capacitance. The first technique is known as photogate and uses the gate of a transistor as a capacitance, shown in Figure 2.1. A transmit transistor is created adjacent to the photogate to read out the value of the voltage across the capacitance. The gate material is made of polysilicon and is insulated from the substrate with a thin gate oxide. In technologies prior to 0.18 µm, the gate oxide was thick enough to not suffer significantly from tunneling effects which resulted in relatively small dark currents. As technologies began to shrink, photogate began to show poor imaging quality due to an increase in dark current caused by smaller gate oxide thicknesses. When gate area was increased to improve imaging quality and increase the amount of photons absorbed by the polysilicon, quantum efficiency and signal-to-noise ratio did not increase linearly [7]. This led to a movement away from photogate technology and the development of a new pixel design for modern technologies.

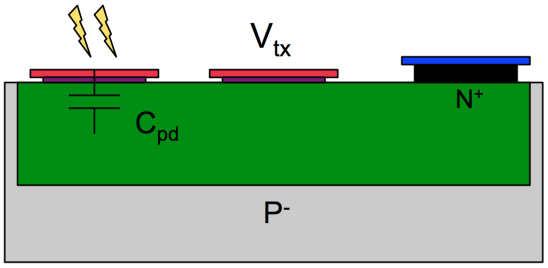

Figure 2.1: Photogate Pixel

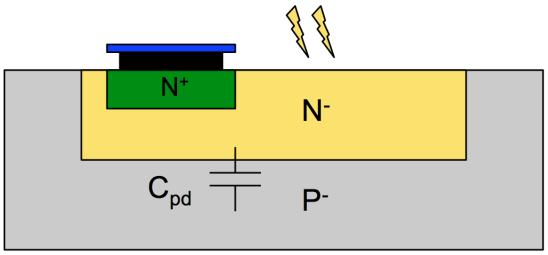

Figure 2.2: Photodiode Pixel

The second technique for photon absorption, known as a photodiode, utilizes the capacitance of the reverse biased diode created by P and N junctions, shown in Figure 2.2. An N-well is charged to a reset voltage and its capacitance across the substrate due to bulk and sidewall terms is allowed to leak. Due to the N-well's increased perimeter and area than the photogate, it has an improvement in quantum efficiency and signal-to-noise ratio that make it appealing for small feature sized technologies that need high quality imaging. Additionally, the photodiode scales very well with N-well size, allowing larger pixel fill to capture significantly more photons primarily due to an increase in perimeter area for larger N-wells.

The advantages of the photodiode and its imaging performance in the 0.13 µm technology make it the superior technique for use in the neighborhood processor.

2.2.2 Readout Schemes

A secondary aspect to pixel design is in reading out the value of the voltage across the capacitance. If the voltage is buffered and processed directly by analog circuitry, the pixel element is known as an analog pixel sensor (APS). The entire readout operations maintains the voltage in the analog domain, which reduces the need for conversion circuitry, but poses a problem for transmitting the value to other portions of the chip. When transmitting the pixel's voltage, large nets that span the image array to nearby processing elements may cause capacitance loading and introduce losses along the way. Additionally, if the processing operation is not immediately performed the pixel will continue to leak after the image capture, having inconsistencies across the pixel array [6].

An alternate method which alleviates many of these problems is to introduce analog-to-digital conversion circuitry for each pixel, creating a digital pixel sensor (DPS). At the cost of increased area requirements, the digital conversion eliminates the need to immediately process the pixel data and allows the digital value to be transferred across large nets. Another advantage introduced in converting the signal to a digital value is allowing immediate interface with digital electronics. The digital value of the pixel brightness can be directly processed by the processor once leaving the pixel [1, 9]. The drawback of using a digital pixel sensor is the need for a global ramp and counter to provide a reference for the analog-to-digital converter in each pixel. The ramp must be consistent across the image array with minimal slew, which then triggers the processor to save the counter's value for the pixel brightness equivalent.

For allowing direct integration and compatibility with the neighborhood processor, a digital pixel sensor design was chosen.

Chapter 3

Schematic Design

3.1 Design Considerations

The fundamental operation of the photodiode circuitry is shown in Figure 3.1. The photodiode is charged to a reset voltage then released, allowed to integrate over a period of time. Once this time has elapsed, the ramp is globally sent to every pixel and the comparator triggers a compare line high when the ramp exceeds the photodiode voltage.

The ramp and reset voltages were chosen to use the analog supply (2.5V), for maximum dynamic range and resolution, and the output compare to use the digital supply (1.2V) for direct integration to the processor. Additionally, all analog transistors were chosen to be thick-oxide transistors which are less prone to leakage and provide better imaging characteristics at the cost of less compact design rules.

The design began with a subthreshold comparator, shown in Figure 3.2. The bias voltage was tweaked until the maximum gain for the common-source amplifier was found that could provide reasonably fast slew-rate. The slew-rate of the comparator translated into a lag in conversion response time when the ramp exceeded the pho-

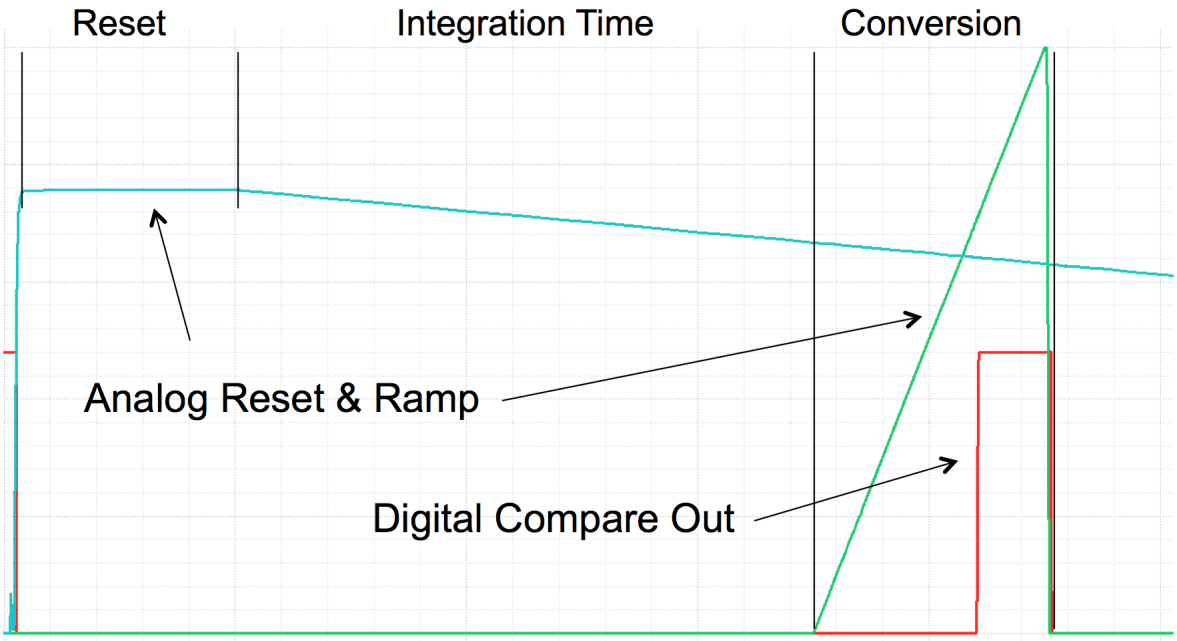

Figure 3.1: Photodiode Acquisition

todiode voltage that had to be minimized for an accurate conversion. For routing simplification, the two bias voltages for the differential pair and the common-source amplifier were chosen to use the same value..

The next portion added to the comparator was the reset circuitry to charge the photodiode. A P-type transistor is utilized to pull the photodiode all the way to $Vreset$ during the reset phase. Because of the behavior of the *reset* line functioning as only high or low, it was treated as a digital signal in Encounter and routed as one. When it reached the photodiode circuitry, however, it needed to be converted to analog supply levels before it could be used to drive the thick-oxide reset transistor. A level shifter was added to the circuit to convert the reset signal from the digital supply (1.2V) to analog supply (2.5V) [4].

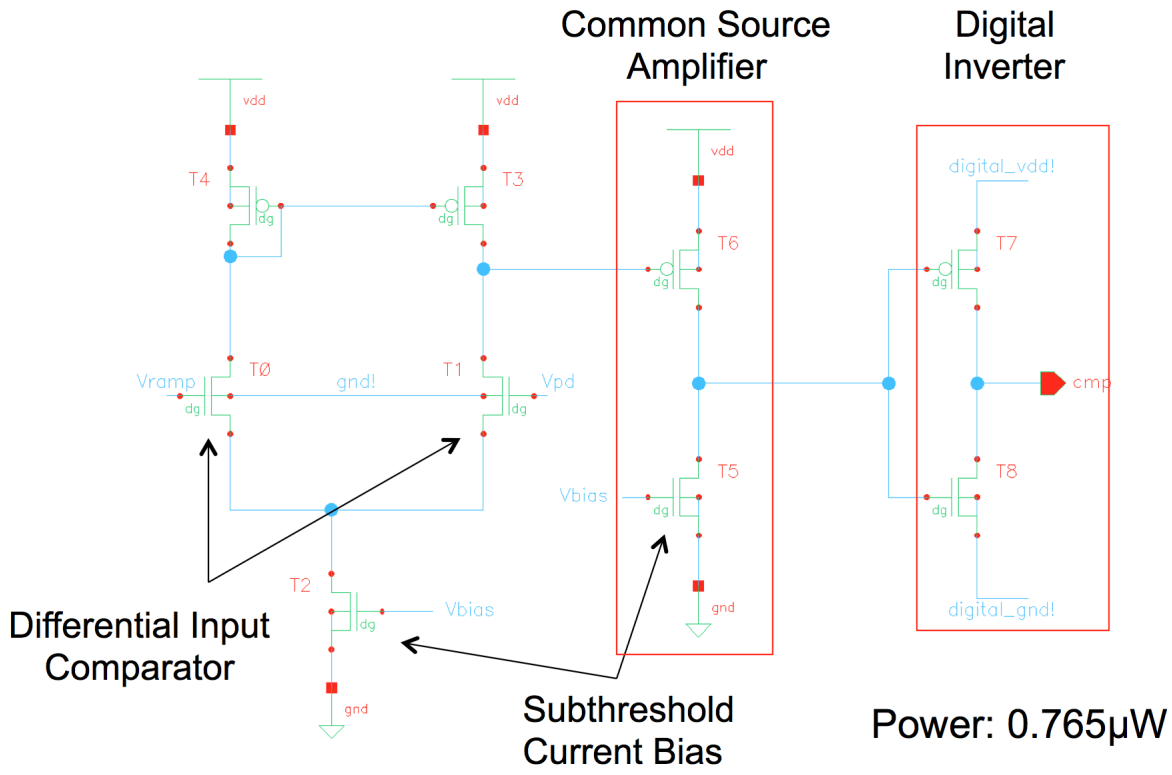

Figure 3.2: Subthreshold Comparator

3.2 Schematic Drawing

The complete schematic for the photodiode circuitry is shown in Figure 3.3 with an ideal photodiode capacitance modeling dark current and photocurrent.

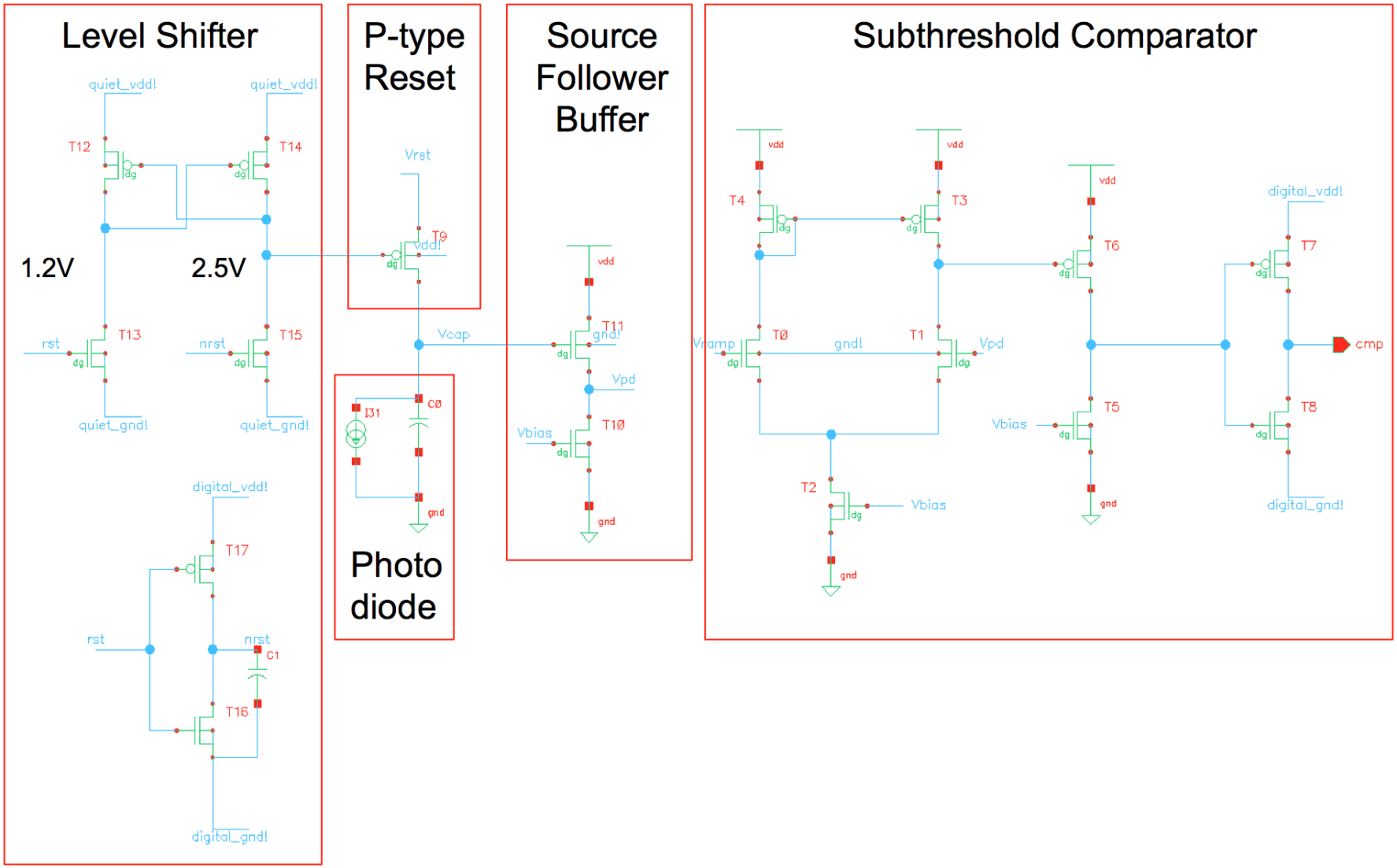

Figure 3.3: Photodiode Schematic

Chapter 4

Layout Design

4.1 Photodiode Design Considerations

The design considerations for the photodiode's silicon footprint are:

- Integration into standard cell rows
- Pin locations
- Shielding from substrate and digital signals
- Pixel fill factor
- Antenna rules
- Exclude fill layers

The digital place and route system places the digital cells in a fixed height row of cells, known as a standard cell row. The proprietary library of digital cells contain layouts with a fixed height that share N-wells and power rails with adjacent cells, forming a continuous strip of N-well and metal for Vdd and Gnd.

The photodiode and comparator must fit alongside these standard cells so that when it is placed by the place and route system it does not collide with or obstruct the N-wells and supply rails. For this reason, the analog layout must fit within an integer multiple of the standard cell height and constrain itself form the perimeter to not interfere with the overhanging layers. the standard cell height.

The place and route tool will also try to run routes over the comparator. The high density routing necessary to realize the NP on the silicon limited area requires these routes to be clear for these nets. This forces the entire layout to be done on as few metal layers as possible, leaving only the first metal layer and below to work with for routing the comparator. Additionally, the pins that will be brought to various metal layers for connectivity must be cleverly placed to only take up a single routing channel, or about 0.6 µm at the third layer of metal.

To protect the comparator from the noise and coupling of these digital signals that will be routed on top, shielding must be introduced immediately above the comparator. The place and route tool will route digital signals on the third layer of metal and analog signals on the upper 3 layers of metal in the 8-layer metal technology. This requires a shield on the second layer of metal to protect the analog transistors from the digital routes. Another shield is also required on the fourth layer of metal to protect the analog routes from the digital routes. To reduce coupling effects of these shields, they will be tied to different potentials. Both of these shields must have as much shielding as possible while still allowing pins through from the first through fifth layer of metal. Lastly, the shields will be routed together by the place and route software to create a globally connected shield that is tied down external of the chip.

The last form of shielding included is to protect the comparator and photodiode from nearby substrate noise from the adjacent standard cells. This is done in the form of a guard ring that encloses both the photodiode and analog circuitry. The

guard ring is tied to the same shield that is used for the second layer metal shield.

Lastly, the pixel fill factor is maximized once all of the other design requirements are met. For the final design of the photodiode, an 11% fill factor was achieved.

4.2 Antenna Rules

During the design process, checks for design rules are made to ensure minimum and maximum geometries, proximity rules, and fabrication rules are met.

A type of fabrication rule that is strictly enforced by the foundry relates to the creation of metal during the wafer run. As metal layers are created by photolithography, ions are absorbed by metals that create static charge. The buildup of this charge can destroy structures on the wafer if they are not provided a method of dissipation. In particular, upper layer metals most at risk due to being larger and must be tied down to the substrate in some manner. For this reason, the comparator will have to have diodes to tie down the nets that use these layers, which are the analog $Vramp$ and $Vbias$ signals. Another antenna rule that is enforced is related to the metal to N-well ratio. There exists a minimum ratio that is necessary for each metal connected to an N-well that is enforced. This issue arised after the chip was submitted to fab, but the problem was alleviated by introducing a structure at the layout level. The standard cell rows between photodiodes were unusually short due to the blockages introduced by the photodiode N-well, and violated this ratio requirement. The solution to this problem was to introduce a stripe of metal 1 on the left hand side of the cell to staple Vdd rails together that had these issues.

4.3 Fill Rules

Another check that is done at the foundry level is to ensure metal utilization on areas is within specification. Since an 8-layer metal wafer in created in stages, each metal layer must be structurally sound before the next layer of metal can be applied. For this reason, there exist minimum and maximum percentages of utilization set by the foundry.

In the design of the comparator, and in particular the shielding, it was important to not exceed any of these fill factors. The foundry allows the designer to insert their own fill to meet requirements for the upper layers of metal, but introduces their own fill for the lower layers of metal. This was problematic due to the fill being placed over the photodiode would block incoming light for each pixel. With foundry approval, special drawing layers were used to exclude fill from being placed over the photodiodes.

4.4 Photodiode Layout

The completed photodiode drawing is shown in Figure 4.1. Dozens of design iterations took place to be able to fit the entire pixel circuitry in its final compact form factor, $28\,\mu m \times 14\,\mu m$. The pin locations were arranged to obstruct only one routing channel on the horizontal metal 3 row, as shown in Figure 4.3. Analog pins continued up the via stack to metal 5 where they were manually connected to global nets, shown in Figure 4.4.

The shields on metal 2 and metal 4 are visible, along with the metal 1 staple on the left-hand side to connect standard cell rows together. A custom place and route boundary, shown in cyan, was created to let standard cell rows be abutted as close

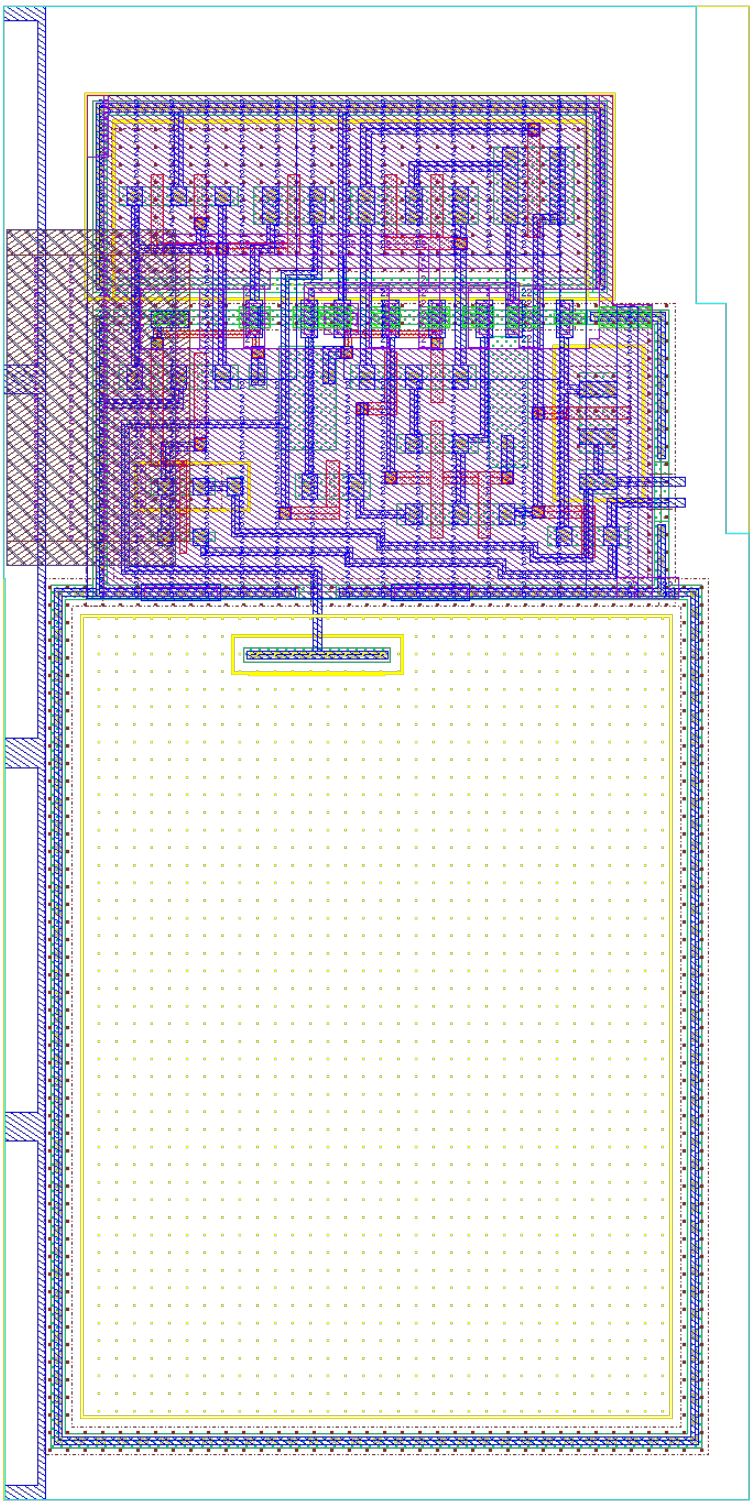

Figure 4.1: Photodiode Layout

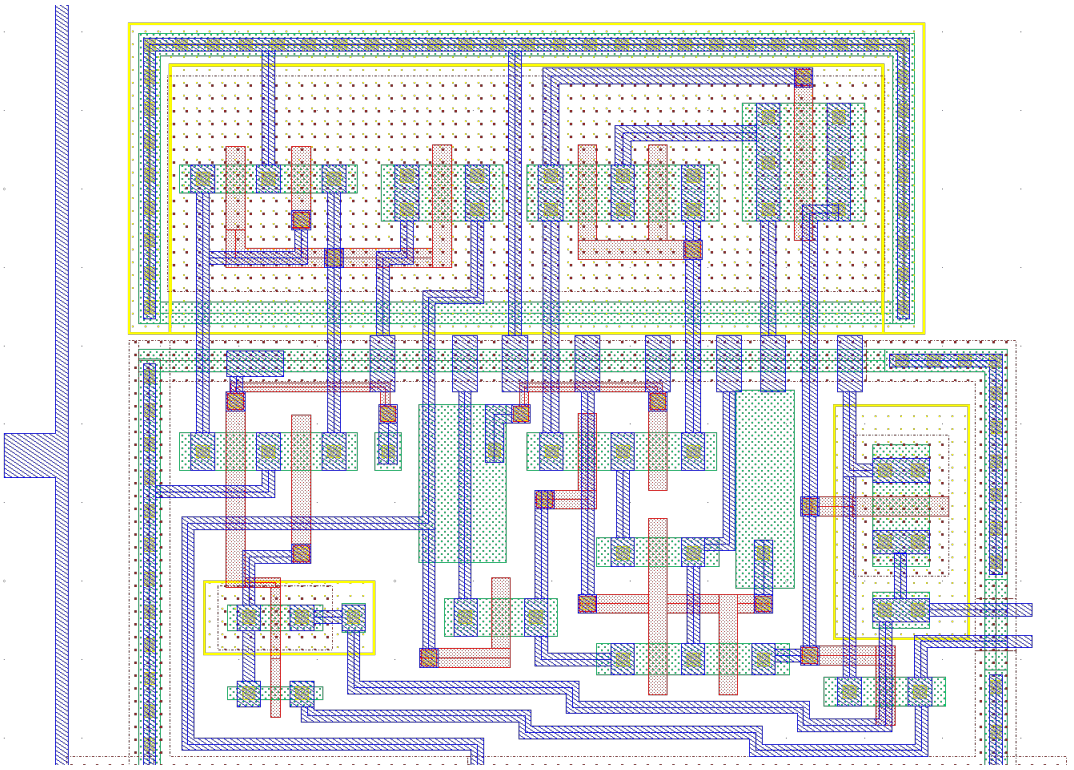

Figure 4.2: Analog Section Layout (Metal 1 and below)

as possible without violating design rules.

The analog portion is shown in Figure 4.2 with upper layer metals removed. The level shifter N-wells are visible in the N-type section, spaced far away from the P-type section. The diodes required for Vbias and Vramp are visible here as well.

4.5 NP Layout

The photodiode is next exported into the place and route system where it can be placed as a standard cell.

The completed layout is shown in Figure 4.5, where a 8×8 array of photodiodes can be seen. A close-up of a pixel with its surrounding pixels is shown in Figure 4.6.

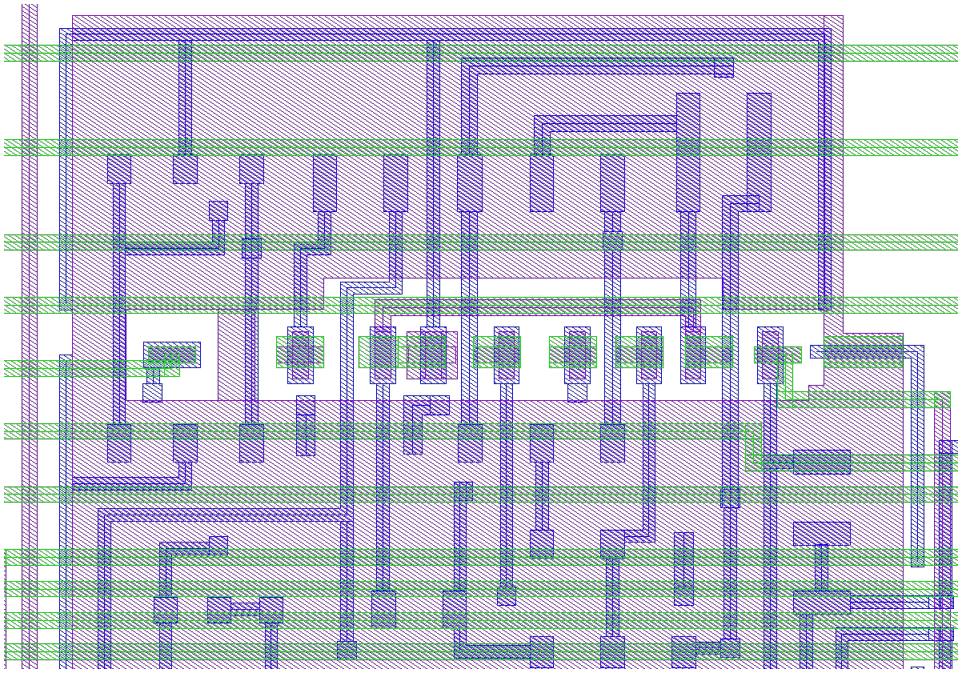

Figure 4.3: Pins Along Metal 3 Routing Channel

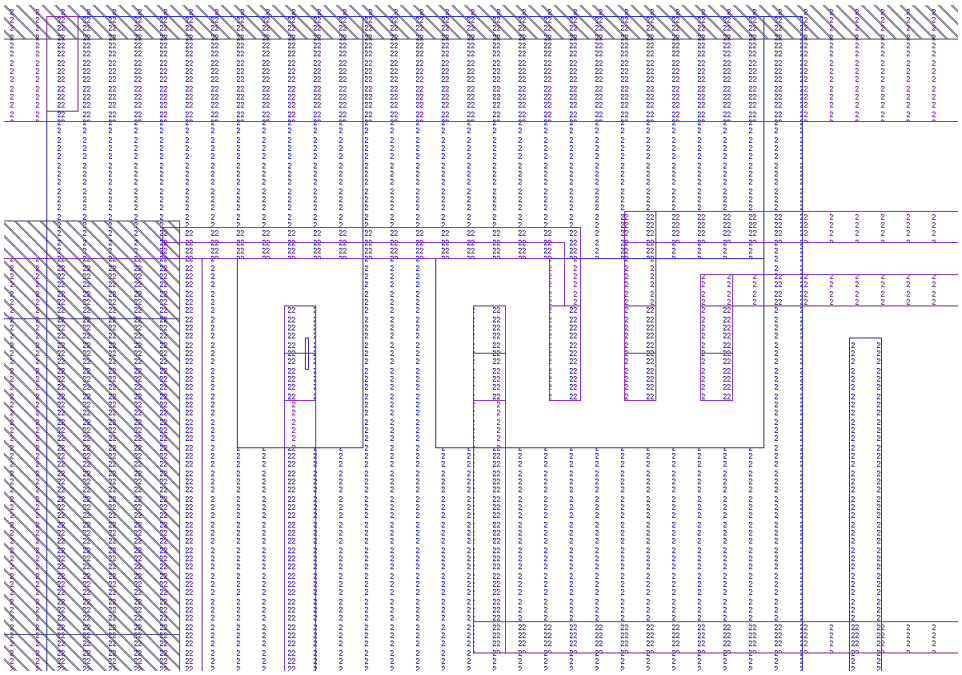

Figure 4.4: Analog Routes

The photodiode exclude layers' effects are shown, with no routing or fill being placed on them.

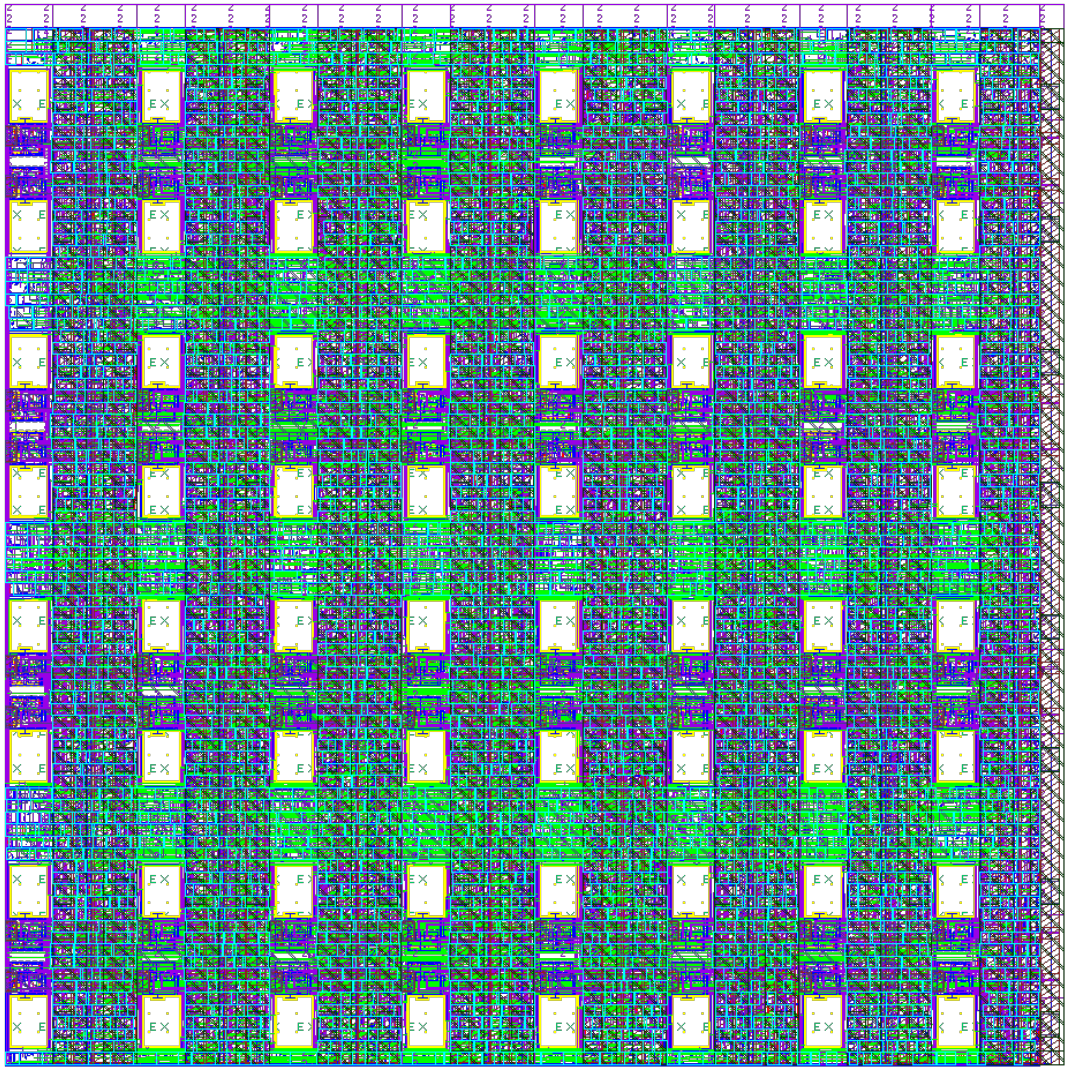

Figure 4.5: NP Layout

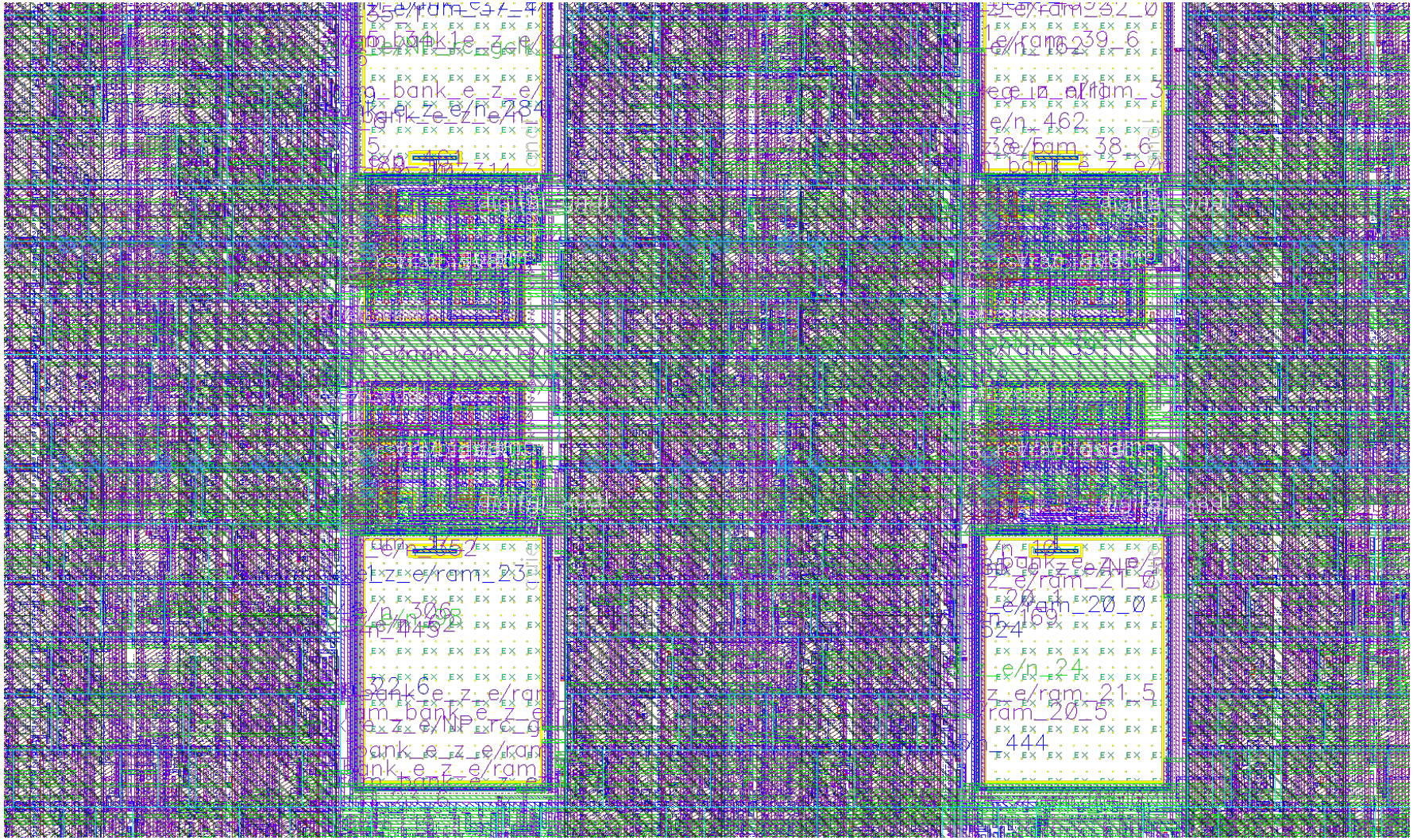

Figure 4.6: NP Layout Detail

4.6 Top Layout

The NP layout is hierarchically used in a top level design to create an array of processors. Alongside the processor array is a microcontroller to provide control and communication with the array. The final layout is shown in Figure 4.7. A hierarchical view is shown in Figure 4.8.

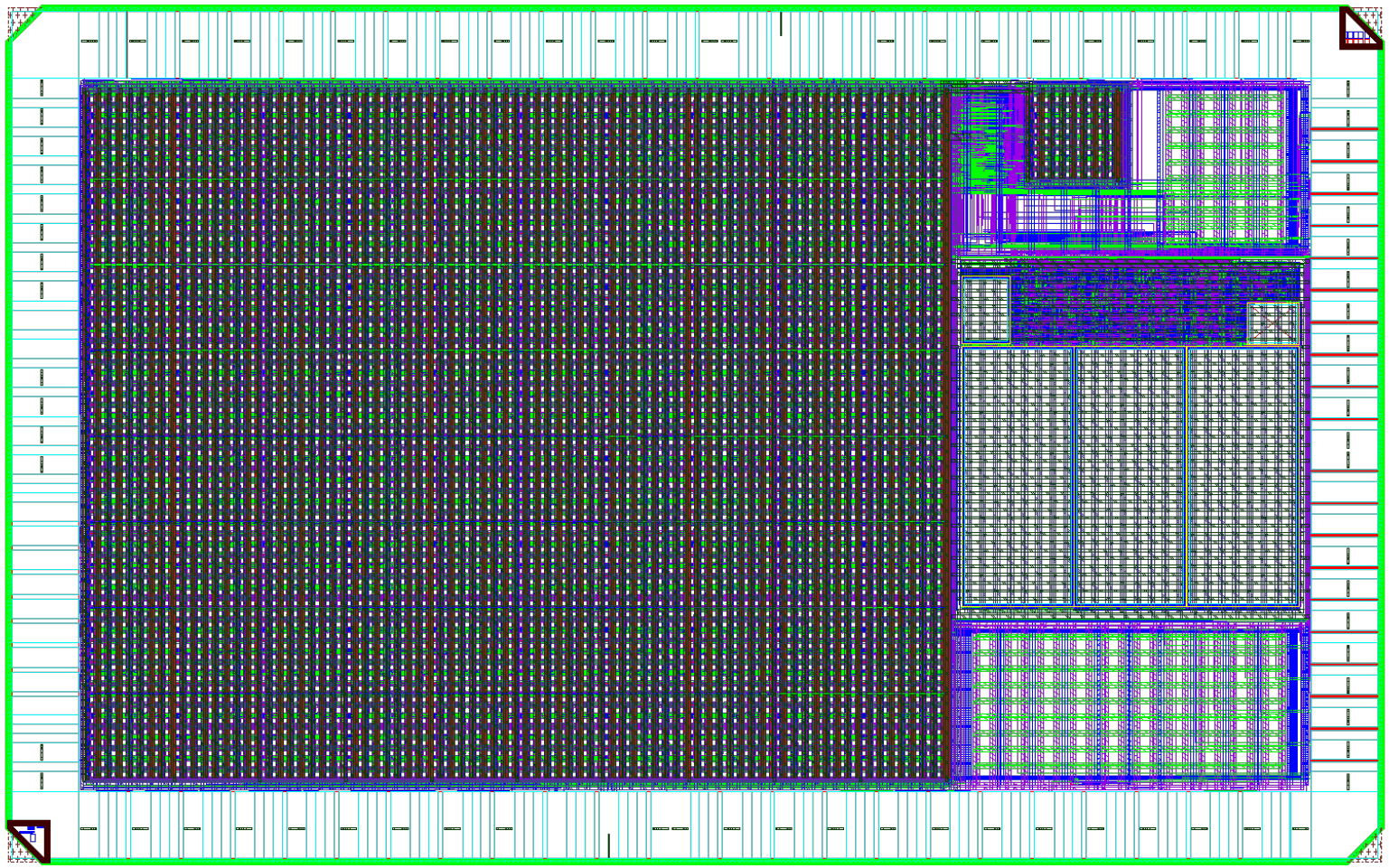

Figure 4.7: Top Layout

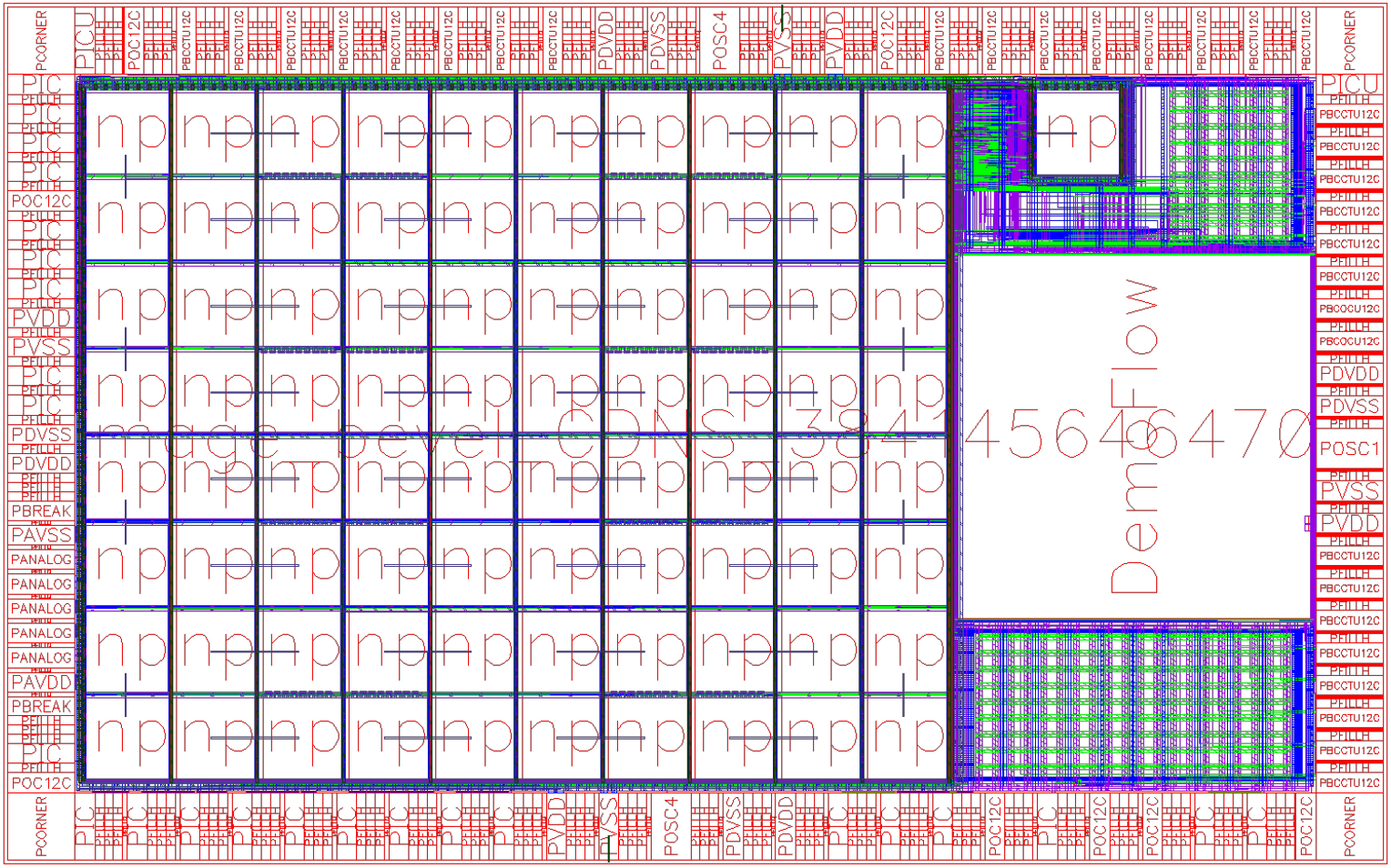

Figure 4.8: Hierarchical Top Layout

Chapter 5

Verification

5.1 DRC

ASSURA was used to ensure the design met the technology design rules. Particular attention was placed on the thick-oxide transistors used in the analog portion due to increased spacing requirements for these N-wells and active regions. Large spaces had to be left on the top and sides of the photodiode to ensure that approaching N-wells from standard cells after IP insertion did not violate thick-oxide transistor spacing rules. Recommended rules for high yield were ignored in order to minimize area and create a layout as compact as possible. At the top level a global DRC check was run which consisted of design rule, antenna, and fill checks. Fill was properly handled by Encounter and did not require any intervention. However, multiple design iterations were done to eliminate all the antenna issues. Some of these were visible early in the design flow, such as the need for tie down diodes on the photodiode. Others were discovered after going to fab, where IP insertion created more problems, such as the standard cell stapling done on metal 1.

5.2 LVS

The photodiode, NP, and top level layout designs were compared to their schematic counterparts in Open Access and Verilog. The photodiode's N-well could not be compared to an ideal capacitor, because the extraction utility, ASSURA QRC, did not recognize the N-well to substrate junction as a capacitance. Thus, a modified schematic without photodiode capacitance was used for LVS. The NP and top level layouts were compared against Verilog utilizing blackboxing techniques on standard cells and pads. The layouts for these are proprietary, so they could not be analyzed during LVS. Blackboxing stops LVS from descending into a cell, instead it simply verifies extracted pin connectivity, making sure it is properly connected. This was particularly important for the photodiode, since no Verilog equivalent was created for the comparator and reset circuitry. At the top level, LVS was able to hierarchically analyze the top level Verilog which made reference to the NP Verilog.

Chapter 6

Area Minimization Techniques

6.1 Custom Logic Cells

A majority of chip area is utilized by sequential logic cells in the construction of memory elements and registers throughout the digital design. To help reduce area utilization and provide more area for routing channels and pixel elements, the most heavily utilized cell was redesigned. A report of area utilization is shown in Table 6.1.

If we create our own sequential logic cell, we can improve area utilization by providing a less robust, but much smaller digital flip-flop (DFF). The design that

Table 6.1: Area Utilization

Type	Area (µm^2 μm^2)	Area %
timing	3,774,714.750	42.6
sequential	3,261,820.320	36.8
inverter	24,276.960	0.3
buffer	43,649.280	0.5
clock_gating	481,096.800	5.4
logic	1,275,981.120	14.4
total	8,861,539.230	100.0

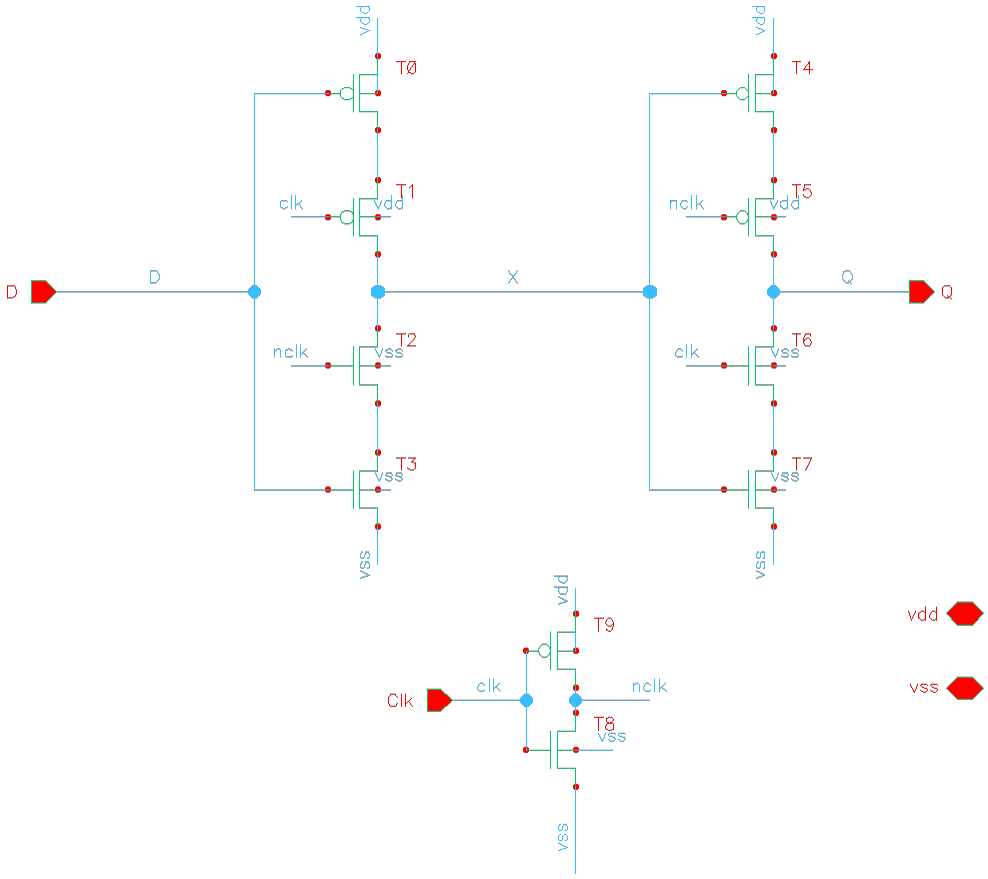

Figure 6.1: C^{2}MOS DFF Design

was chosen used a clocked gate composed of two tristate buffers in series that could hold a logic state between them using an internal capacitance across net X, shown in Figure 6.1 [5]. This design uses eight fewer transistors than a standard transmission gate design, shown in Figure 6.2.

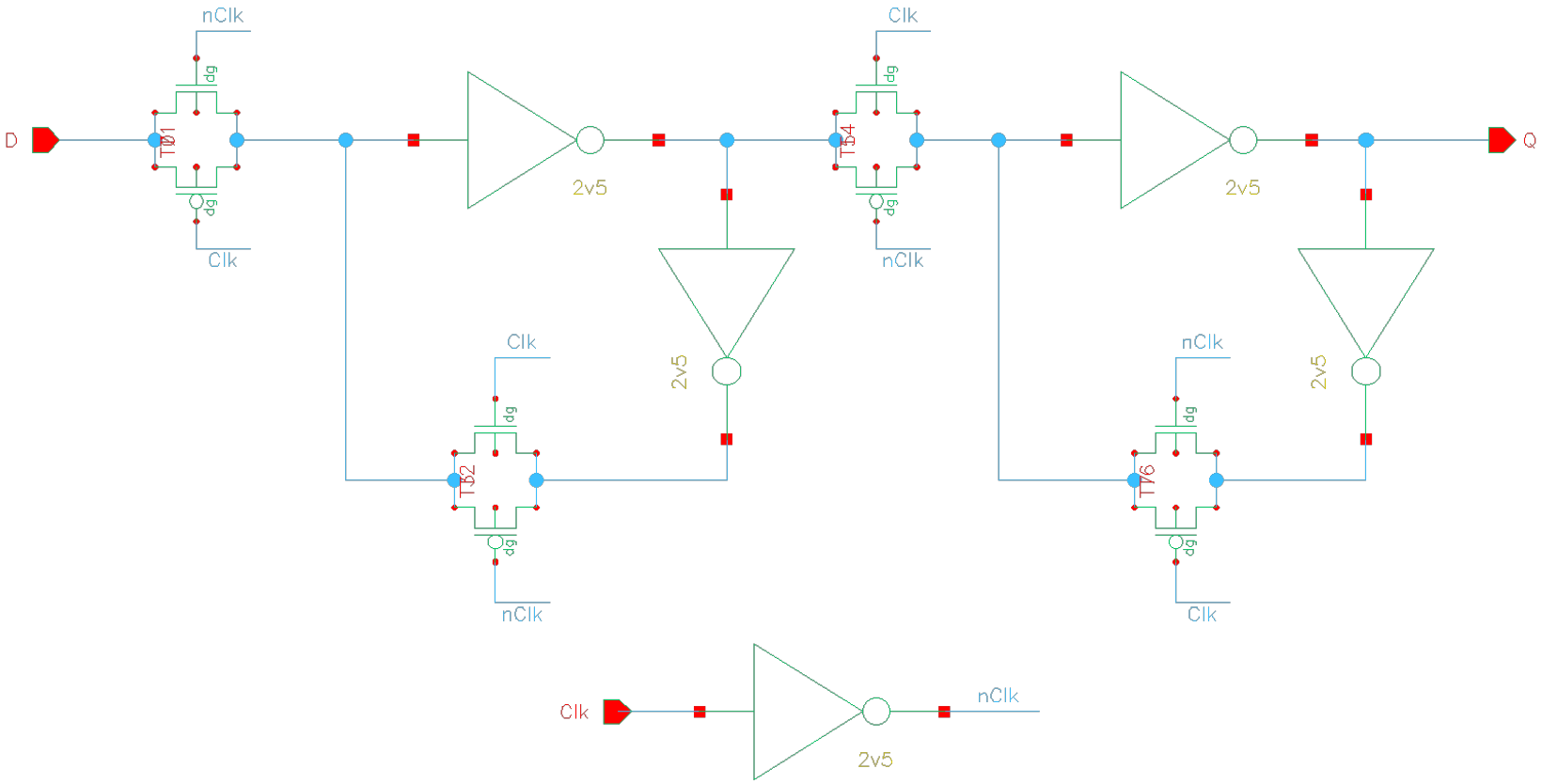

Figure 6.2: Transmission Gate DFF Design

6.2 DFF Layout

The final layout of the DFF is shown in Figure 6.3. To maximize routing ability and minimize the number of layers used, active and poly were used as routing layers. The design rules were pushed to the limits and recommended rules were ignored to ensure minimum area utilization. Special logic-only rules were applied to the design to further allow area minimization and allow the smallest possible DFF design. The height is matched to the standard cell library's. In 0.13μm it is not possible to make the design any smaller width-wise.

6.3 Encounter Library Characterizer

After a layout and abstract were created for the new DFF, Encounter needed timing and characterization data to be able to recognize its functionality, place it as a standard cell, and ensure timing was met. The Encounter utility used for this was Encounter Library Characterizer (ELC). ELC received a schematic netlist of the design to be modeled along with a handful of initial conditions and operating ranges for the technology and generated a truth table of conditions to attempt to model based on the pins seen. Next, ELC would run a SPECTRE simulation on the design and feed it various inputs to determine its functionality. The output of this is shown below in ELC's function format and Verilog:

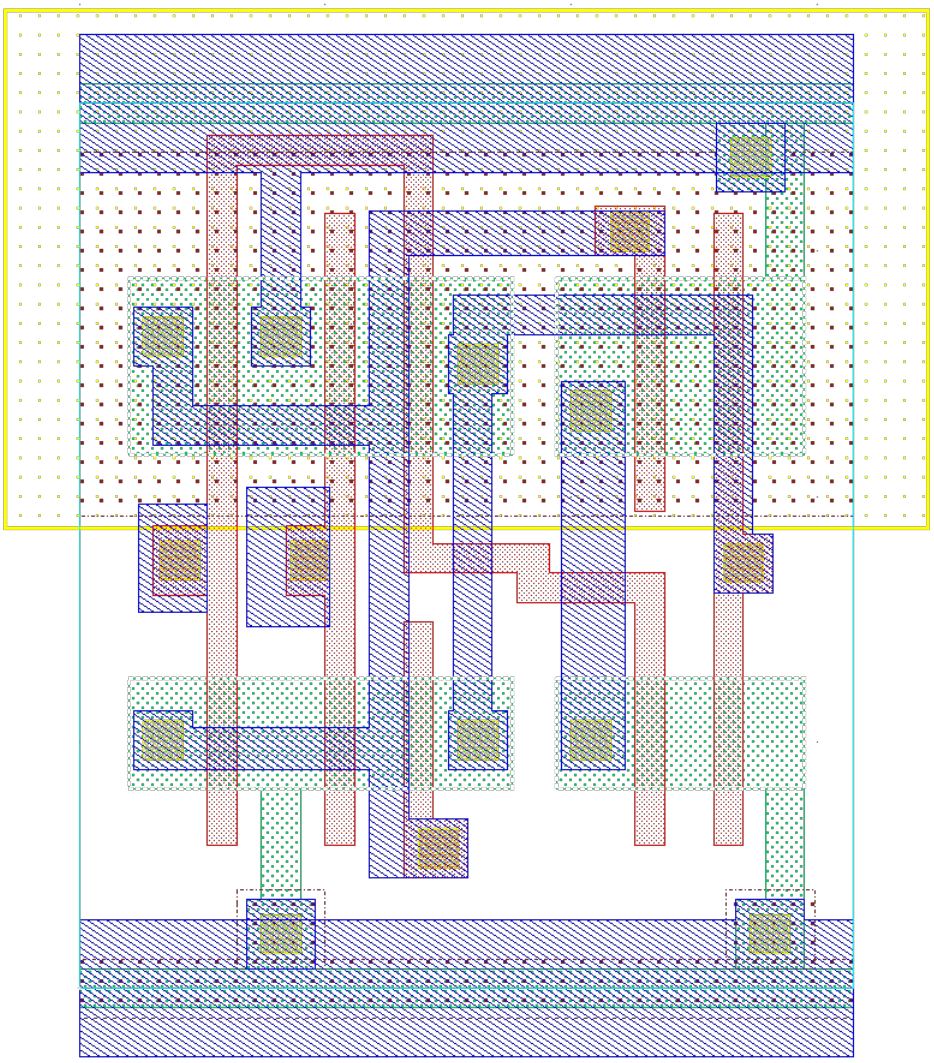

Figure 6.3: DFF Layout

```
DFF
,       REGISTER([X])::=(~D@~CK)
,       Q::=(~[X]@CK)
;
```

```
module DFF(CK,D,Q);
        input  CK,D;
        output Q;
        trireg _n1;
        notif1(Q,_n1,CK);
        notif0(_n1,D,CK);
endmodule
```

ELC properly recognized the flip-flop as a register and identified its internals as two inverters with an internal tristate buffer. The timing library created by ELC was fed into Encounter where it was selected during synthesis for placement. When Encounter sees this register as meeting timing requirements while having less required area than the digital library's flip-flop cell, it is selected for placement and its layout is inserted into the floorplan.

6.4 A Gated Clock

After the design of the DFF, analog simulations were run to ensure that the state could be preserved in the case of the clock being turned off to the logic cells due to clock gating. In the case of transmission gate DFF design, a feedback loop ensures the state is not lost, even if clock stops. However, the C^2MOS design solely relied on an internal capacitance held by two transistors' gates, which would leak over time. It was determined that the integrity of the DFF's output could not be guaranteed, so

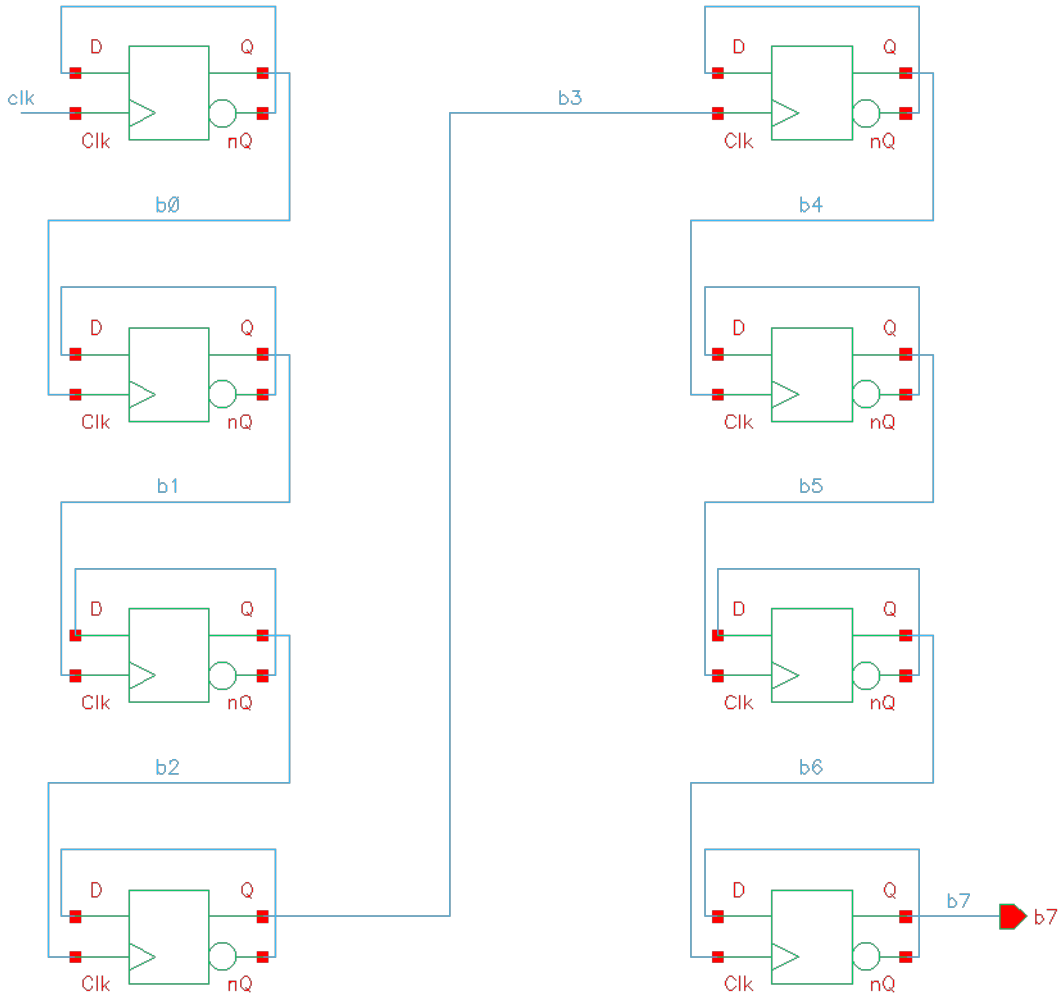

Figure 6.4: Ripple Counter

it would not be used in the final design.

To monitor its abilities in integrating with other standard cells, a test structure was built and included in the top level design. In the test structure were two tests: to interface the DFF with inverters to create a ripple counter, and to feed into a NAND gate from the standard cell library. The schematic for the ripple counter is shown in Figure 6.4. The schematic for the NAND test is shown in Figure 6.5. The combined layout is shown in Figure 6.6.

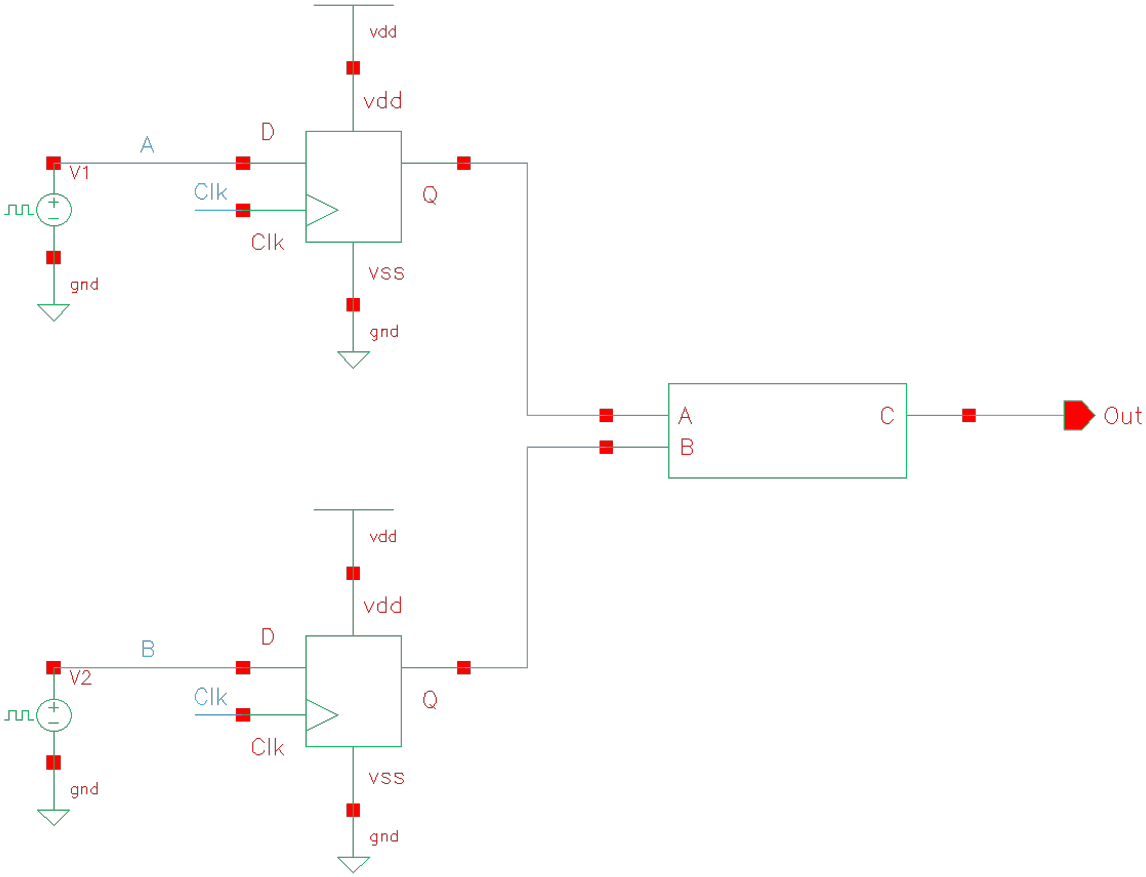

Figure 6.5: NAND Test Structure

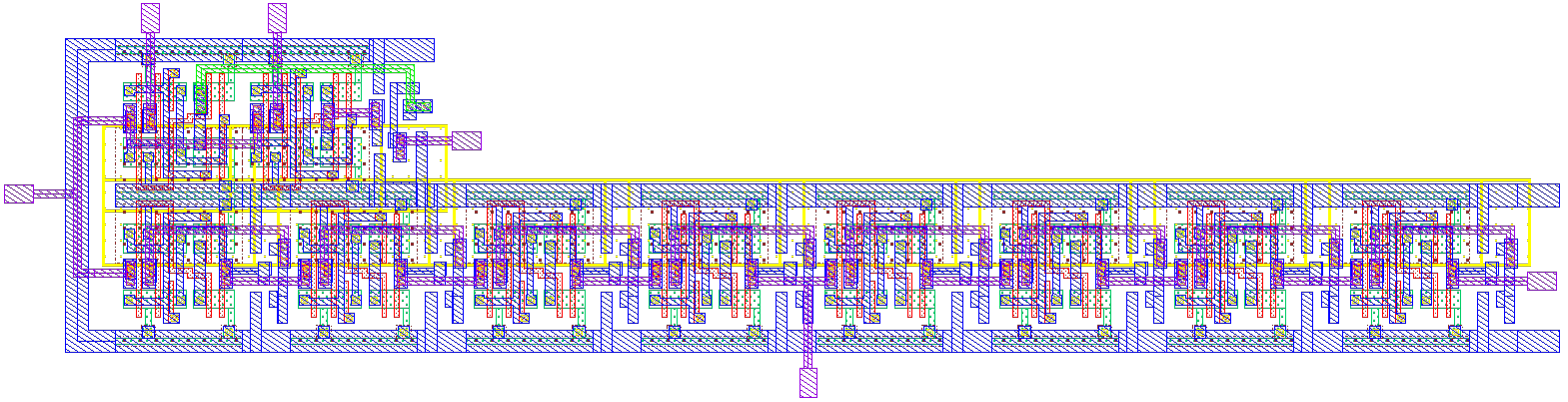

Figure 6.6: DFF Test Structure

Chapter 7

Future Work

After the chip is returned from fab, it will be tested and insight on optimizing the design will be incorporated in the next revision. This section highlights the forseeable advances for the chip in various aspects from the hardware level.

7.1 Testbed

A test PCB will be made to mount and interface the chip with an external lens and FPGA to task image operations and collect readout data. The results of this board will allow us to determine what kind of manipulations can be done from an external level to optimize imaging capabilities. Some expected examples include the adjustment of the ramp signal's starting and ending voltages to integrate pixels for various lighting conditions, controlling dynamic range. Another tweak that could be made is to slow down the clock during capture, to allow the integration time to be lengthened for very dark scenes or if photodiode capacitance is not as small as we had imagined. The imaging quality seen from this board will also give us insight into how to redesign the photodiodes, if pixel pitch needs to be changed or fill increased.

Lighting anomalies are not expected but may be seen, such as upper layer metal blocking light capture at oblique angles.

7.2 DFF Test Structures

The data collected from the test structures of the custom DFF can have drastic impacts on the area utilization of this chip. If no problems are detected for slow clocks, the DFF could become the new candidiate for low drive strength flip-flops in the entire design, replacing the standard cell ones which take up over a third of the area. If the slow clock is problematic, but the DFF interfaces nicely with the standard cells, then clock gating could be removed from the Encounter flow to create a higher power, but high density imager. Lastly, the ultimate goal would be to create an entire area-conscious standard cell library of our own that targets the most common cells in the design which are currently taking up too much space. The test structure's results are vital in determining the value of pursuing a task of this order of magnitude.

7.3 Process Scaling

If the design were to be respun under a new technology, digital placement and routing would become significantly easier. A newer technology would not only mean smaller area utilization for standard cells and circuitry, but more layers of metal. Currently, in 0.13μm, we have 8 layers of metal, two of which are being reserved for shielding and one which is used by the standard cell library. This left only three layers for analog routing and two layers for digital routing. Even one more layer would allow us to incorporate an entire plane of routing channels in the design, further compacting and optimizing the layout.

On the other hand, a smaller technology also means analog circuitry will have to be scaled down. Although the photodiode design would also shrink in size, it would also be at the mercy of small channel length effects and leakage currents. Smaller gate oxide thicknesses would inherently mean more tunneling effects and leakage for the comparator and photodiode. The subthreshold bias transistors may also prove to be problematic if voltages cannot be maintained to draw enough current in the comparator to have acceptable slew-rate.

7.4 Parallel Imagers

The ultimate goal of this project is to further expand the parallel nature of the architecture to exploit its capabilities. By arranging multiple cameras together, a multi-chip camera could be produced to do distributed camera operations such as tracking or object recognition. The macro-scale could also introduce capabilities such as wireless communication or sensor networks. The parallel nature of these technologies would heavily utilize the abilities of the parallel architecture.

Bibliography

[1] M. Gottardi and W. Yang. A ccd/cmos image sensor array with integrated a/d conversion. In *Circuits and Systems, 1997. ISCAS '97., Proceedings of 1997 IEEE International Symposium on*, volume 3, pages 1908–1911 vol.3, 1997.

[2] S. Kleinfelder, SukHwan Lim, Xinqiao Liu, and A. El Gamal. A 10000 frames/s cmos digital pixel sensor. *Solid-State Circuits, IEEE Journal of*, 36(12):2049–2059, 2001.

[3] Anantha Krishna Nelliparthi. A 2-d processor array for massively parallel image processing, 2011.

[4] P.O. Pouliquen. A ratioless and biasless static cmos level shifter. In *Circuits and Systems (ISCAS), Proceedings of 2010 IEEE International Symposium on*, pages 4097–4100, 2010.

[5] Rabaey, Chandraskan, and Nikolic. *Digital Integrated Circuits*. Prentice Hall, 2nd edition, 2003.

[6] F. Serra-Graells, J.M. Margarit, and L. Teres. A self-biased and fpn-compensated digital aps for hybrid cmos imagers. In *Circuits and Systems, 2007. ISCAS 2007. IEEE International Symposium on*, pages 2850–2853, 2007.

[7] Hui Tian, Xinqiao Liu, SukHwan Lim, Stuart Kleinfelder, and Abbas El Gamal. Active pixel sensors fabricated in a standard 0.18-μm cmos technology. In *Photonics West 2001-Electronic Imaging*, pages 441–449. International Society for Optics and Photonics, 2001.

[8] D.X.D. Yang, Boyd Fowler, and A. El Gamal. A 128 times;128 pixel cmos area image sensor with multiplexed pixel level a/d conversion. In *Custom Integrated Circuits Conference, 1996., Proceedings of the IEEE 1996*, pages 303–306, 1996.

[9] D.X.D. Yang, Boyd Fowler, and A.E. Gamal. A nyquist rate pixel level adc for cmos image sensors. In *Custom Integrated Circuits Conference, 1998. Proceedings of the IEEE 1998*, pages 237–240, 1998.

[10] Hongbo Zhu and T. Shibata. A real-time motion-feature-extraction image processor employing digital-pixel-sensor-based parallel architecture. In *Circuits and Systems (ISCAS), 2012 IEEE International Symposium on*, pages 1612–1615, 2012.