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MODELING OF POWER SEMICONDUCTOR DEVICES

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One of the requirements for choosing a proper power electronic device for a converter is that it must possess a low specific on-resistance. The specific on-resistance of a bipolar device is related to the base width and doping concentration of the lightly doped drift region. This means that the doping concentration and the width of the low-doped base region in a bipolar device must be carefully considered to achieve a desired avalanche breakdown voltage and on-resistance. In order to determine the technological parameters of a semiconductor device, a one dimensional analysis is used to calculate the minimum depletion layer width, W_{min}, for a given breakdown voltage, V_{BD}, in Si, SiC and GaN $p^+n^-n^+$ structures. Further investigation is done to determine the optimum width of associated depletion layers for different blocking voltages to achieve a minimal forward conduction voltage drop.

The complete one-dimensional model for calculation of the minimum depletion layer width, W_{min}, for a given breakdown voltage, V_{BD}, of a $p^+n^-n^+$ structure is developed and used to calculate the optimum width of the depletion layer for different blocking voltages to achieve a minimal forward drop. The results show that the calculations of the lightly doped drift region thicknesses, and associated breakdown voltages and forward

voltage drops, lead to incorrect solutions when applied to high voltage $p^+n^-n^+$ structures using the simplified model equations for a p^+n structure. These results also indicate a minimal impurity doping concentration for $p^+n^-n^+$ structures, below which little improvement in breakdown capability can be had. The analysis shows for example that optimization of the doping concentration to minimize V_F in a 5 kV Si diode could result in more than a 12% decrease in the forward drop, while for SiC and GaN this decrease is insignificant; typically less than 1%. Therefore, an optimization of the forward voltage drop by using the optimal doping concentration for corresponding breakdown voltages is necessary for proper design of a Si diode, while for wide band gap material devices this optimization is not necessary.

The second part of the dissertation presents a physics-based model of a SiC BJT and verification of its validity through experimental testing. The Fourier series solution is used to solve the ambipolar diffusion equation (ADE) in the transistor collector region. The model is realized using MATLAB® and Simulink®. The experimental results of static operation and also the simulated and experimental results of switching waveforms are given.

From the experimental and simulated results it is concluded that the model represents the static and switching characteristics of the SiC BJT quite well. From the experimental measurement results are calculated the switching losses of the BJT. The differences between simulated and measured switching losses during the turn-on and turn-off are 6.28% and 3.52%, respectively.

To my mother, Tsvetanka Dyulgerova (Цветанка Дюлгерова), she never missed to call and encourage me.

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NOMENCLATURE

A	Active device area, cm^2
A_i, b_i, and m_i	Amplitude parameter (cm^{-1}), ionization energy parameter (V/cm), and fit parameter
BV	Breakdown voltage, kV
BV_{CEO}	Maximum open base breakdown voltage of BJT, kV
C, C_n, and C_p	Auger coefficients, cm^6/s
d	Length from junction to case, cm
d_1, W, and d_2	Depletion region thicknesses of each section of $N^+N^-P^+$ regions, respectively, cm
D	Ambipolar diffusivity, cm^2s^{-1}
D_n and D_p	Electron and hole diffusivities, cm^2s^{-1}
D_{N^-}	Electron diffusivity in N^- region, cm^2s^{-1}
E_G	Band gap energy, eV
h_n and h_p	Recombination parameters, $cm^{-4}s^{-1}$
I_n and I_p	Electron and hole currents, A
I_{n0}, I_{n1}, and I_{n2}	Electron current at junctions J_0, J_1, and J_2, A
I_{p0}, I_{p1}, and I_{p2}	Electron current at junctions J_0, J_1, and J_2, A
I_{disp1} and I_{disp2}	Displacement currents, A
$J_{n(N^+N^-)}$, $J_{n(PN^-)}$	Electron carrier densities at the N^+N^- and PN^- junctions, Acm^{-2}
k and n	Harmonic indexes for CSR carrier density of Fourier series representation

k	Boltzmann's constant (1.381×10^{-23} J/K)
K	Coefficient
K_{FV}	Feedback constant
M	Number of the terms of the Fourier series
N_{D1}	Doping concentration in the lightly-doped n-base, cm^{-3}
N_{D2}, N_{D1}, N_A	Doping concentration in the $N^+ N^- P^+$ regions, respectively, cm^{-3}
N_{N^-}	Doping concentration in the N^- region, cm^{-3}
N_S	Number of effectively available states per unit volume
n	Electron carrier concentration, cm^{-3}
n_i -	Intrinsic carrier concentration, cm^{-3}
$n_0 \ldots n_7$	Nodes in lumped-charge model
N_A	Acceptor doping concentration, cm^{-3}
N_D	Donor doping concentration, cm^{-3}
p	Hole carrier concentration, cm^{-3}
$p(x)$	Ambipolar carrier density as a function of position, cm^{-3}
$p(x; t)$	Ambipolar carrier density as a function of position and time, cm^{-3}
$p_0(t)$	DC Fourier series component of the carrier storage region (CSR) carrier density profile, cm^{-3}
$p_k(t), p_n(t)$ - k- or n^{-th}	Fourier series component of CSR carrier density profile, cm^{-3}
p_{x1} and p_{x2}	Excess carrier concentrations at the two boundaries of the drift region, cm^{-3}

p_{T1}, p_{T2}, and p_{T1}	Carrier densities of the two points of a segment and the carrier density of the segment, cm^{-1}
q	Unit electrical charge ($\cong 1.6 \times 10^{-19}$)
R_{SRH}	Shotkley-Read-Hall carrier recombination rate, cm^{-3}s^{-1}
R_{AUG}	Auger recombination rate, cm^{-3}s^{-1}
R_{SP_ON}	Specific on-resistance, mΩ.cm^2
R_{th-jc}	Junction-to-case thermal resistance, Ω
T	Absolute temperature, K
V_{br}	Breakdown voltage, V
V_{d1} and V_{d2}	Depletion layer voltages, V
$V_{N^- \text{-} N}$	Drift region voltage drop, V
V_{j0}, V_{j1}, and V_{j2}	Voltage drop at junctions J_0, J_1 and J_2, V
v_{sat}	Saturation velocity, cm s^{-1}
V_{seg}	Voltage drop of a segment, V
V_T	Thermal voltage, V
W_1; W_2; W	Widths of the depletion region on the N^- and P sides of the junction and total depletion layer, cm
W_{d1} and W_{d2}	Depletion widths, cm
W_I	Intrinsic layer width, cm
W_{min}	Minimum width of the depletion layer of N-base, cm
x_1 and x_2	Boundary positions of the carrier storage region, cm

α_i, and α_{eff}	General ionization coefficient, effective ionization coefficient, cm^{-1}
β	Common-emitter gain
$\mathcal{E}$	Electric field strength, V/cm
$\mathcal{E}_C$	Critical electric field strength, V/cm
ε	Material permittivity, Fcm^{-1}
λ	Thermal conductivity, W/cm.K
μ_n, and μ_p	Electron and hole mobilities, $(cm^2V^{-1}s^{-1})$
τ_n, τ_p, and τ_{HL}	Electron, hole and high-level injection lifetimes, s
τ_{N^-}	Electron lifetime in N^- region, cm^2s^{-1}
ψ	Potential, V
AC	Alternating current
ADE	Ambipolar diffusion equation
BJT	Bipolar junction transistor
C	Carbon
CS	Carrier storage
CSR	Carrier storage region
CTE	Coefficient of thermal expansion
DC	Direct current
GaN	Gallium nitride
Ge	Germanium
GTO	Gate turn-off thyristor

ICM	Integral charge control model
IGBT	Insulated gate bipolar transistor
IGCT	Integrated gate-commutated thyristor
JFET	Junction field-effect transistors
MCT	MOS-controlled thyristors
MOS	Metal-oxide-semiconductor
MOSFET	Metal-oxide-semiconductor field-effect transistor
MTO	MOS turn-off thyristor
NO	Nitric oxide
NPT	Non-punch-through
PT	Punch-through
RC	Resistor-capacitor
SCR	Silicon controlled rectifier
Si	Silicon
SiC	Silicon carbide
SiO_2	Silicon dioxide
SRH	Shockley-Read-Hall
VJFET	Vertical junction gate field-effect transistors

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In Chapter 5, calculations are presented for the minimum width of a lightly doped drift region (W_{min}) and breaking voltage (V_{BD}) for $P^+N^-N^+$ and P^+N high voltage diodes as a function of doping concentration of a lightly doped drift region (N_{D1}). Also, the power diode model in Simulink; simulation results for Si, SiC, and CaN high-power diodes; and a comparison of the results are given. Next, a power SiC BJT model in Simulink and simulation results of the switching losses of a SiC BJT are presented. Measurement and simulation results of a SiC BJT are compared, and the power BJT model is validated.

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Chapter 1 − Background

1.1 Background of Power Semiconductor Devices

Power semiconductor devices are key components of power electronics technology, used primarily as switches or rectifiers in circuits and systems. Currently, more than 70% of all electrical energy consumed is processed by power electronics. The main function of power electronics is to control and transfer the flow of electrical energy from one form to another and in a form that is suitable to the user. Semiconductor devices are widespread and can be found in almost every electrical and electronic device. Their power range depends on the application and can be from milliwatts to megawatts. Power devices have a significant impact on the economy as they determine system cost and efficiency.

The invention of the bipolar junction transistor in 1947 by Shockley, Bardeen, and Brattain (1), (2) was the beginning of semiconductor electronics and allowed direct solid-state control of electricity for the first time. However, the application of transistors for controlling electrical power was limited until the invention of the thyristor in 1957 (3). Although the thyristor has limited switching capability, it cannot be turned off by external control. Thyristors have been used for the design of different applications, such as control of DC motors. The first power bipolar junction transistor (BJT) with substantial power handling capabilities was introduced in the 1960s. The device overcame some of the limitations of the thyristor, because it can be switched on or off by applying an external signal.

Further developments of the thyristor led to the realization of a fully controllable switching device, a thyristor that can be turned off using a gate (GTO) (4). This enables the GTO to be used in more complex power conversion technology capable of controlling power more directly and efficiently. This significant development greatly enhanced power electronics technology.

The metal-oxide-silicon field-effect transistor (MOSFET) was the next major device introduced in the 1970s (5). It has minimal drive requirements due to its insulated gate. Also, the MOSFET is a voltage-controllable device having high input impedance and fast switching response. MOSFETs are unipolar majority carrier devices which gives them a faster switching speed than the BJT or thyristor. On the other hand, the power handling capabilities of the MOSFET are lower compared to the thyristor because of high on-state resistance associated with high blocking voltage.

In the early 1980s, a new process technology was developed allowing MOSFET and BJT technology to be integrated on the same chip (6), (7). A new device, the insulated gate bipolar transistor (IGBT), was introduced. IGBTs possess the advantages of both devices: faster switching (inherited from MOSFET) and lower specific on-state resistance (from the *PNP* BJT). Improvements in design and technology have made IGBTs popular replacements for BJTs and low to medium power thyristor technology. The IGBT is presently the dominating semiconductor device for most medium power applications.

Figure 1.1 summarizes the most important power semiconductor devices on the market (8) along with silicon carbide (SiC) power devices that have been developed and studied in recent years in various semiconductor laboratories. Due to poorly established technology for production of large area wafers without defects for SiC, silicon (Si) is still the most used element for production of power semiconductor devices.
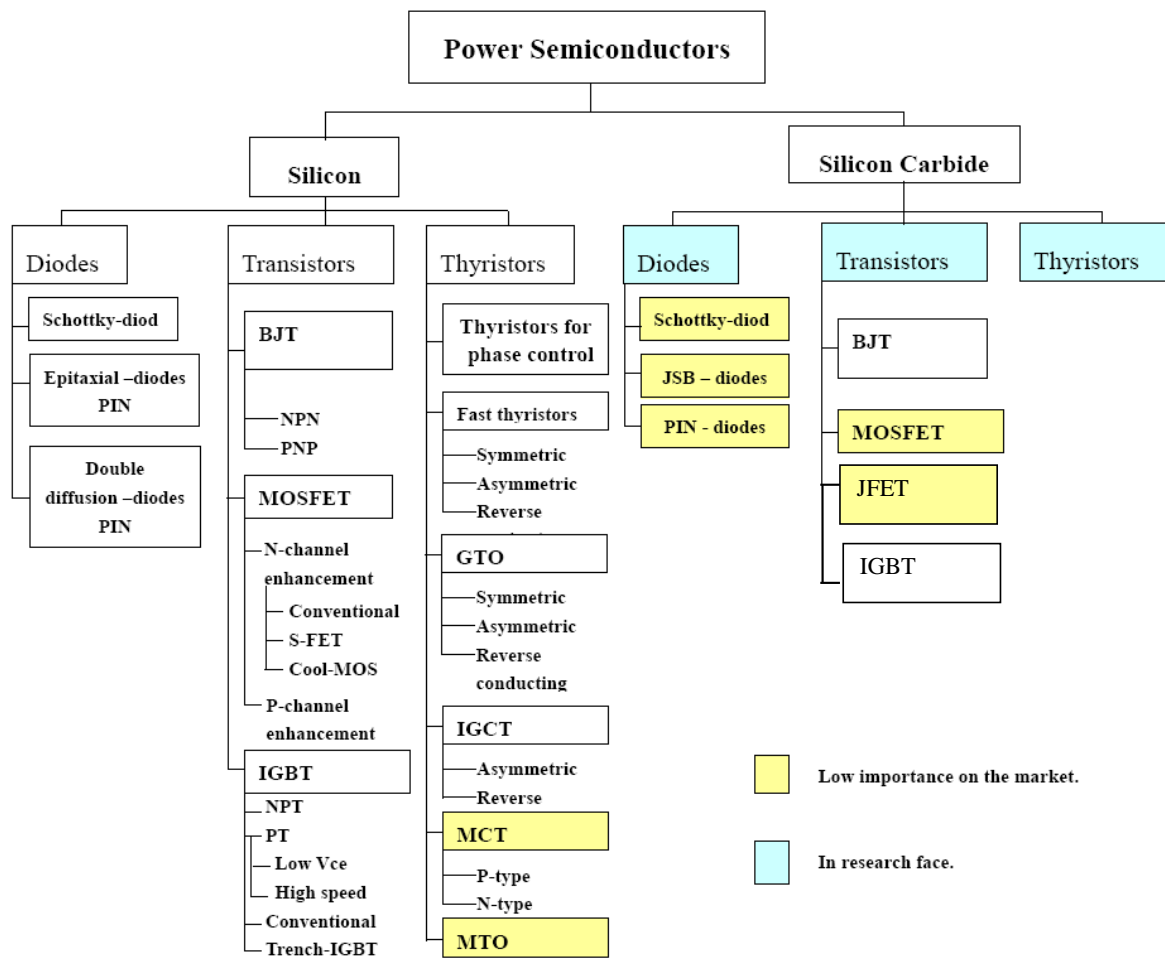
Figure 1.1. Most of the important power semiconductor devices on the market (8) (along with SiC power devices) have been developed and studied in various semiconductor laboratories in recent years.

The devices can be classified as diodes, transistors, and thyristors based on their structure. Schottky diodes are typically used for high switching frequencies at low voltage, $BV \leq 100$ V, the fast switching epitaxial PIN diodes are used for $BV \leq 600 - 1200$ V, and double diffused PIN diodes are applied at higher voltages $BV \geq 1000$ V.

BJTs have been completely replaced by MOSFETs and IGBTs. By introducing an extra P doping region in the MOSFET drift region, a high breakdown voltage can be achieved with much higher drift doping, which results in a drastic reduction (5-10 times) in specific on-resistance for the same chip area in a voltage range of $BV = 600-1000$ V.

Large-area Si devices capable of handling thousands of amperes and kilovolts are now available on the market. MOS gate devices, such as IGBTs, are designed using two different structures: punch-through (PT) and non-punch-through (NPT). Both types of IGBTs can handle voltage up to 3.3 kV and current up to 1.2 kA (9). IGBT modules for 6.5 kV and 0.6 kA are also available.

Si GTOs and thyristors are still widely used for very high power applications. FMCC Group is currently selling asymmetric GTO thyristors for 4.5 kV and 26 kA (10). The devices are optimized for low conduction losses, and the switching frequency is in the range of 200-500 Hz for most applications. All GTOs require the use of snubbers for protection during turn-on and turn-off switching. Significant improvement to the GTO structure, including a gate driver, an integrated inverse diode, and better packaging, resulted in a new semiconductor device, the integrated gate-commutated thyristor

(IGCT). The IGCTs have much faster turn-off times compared to GTOs. This allows them to operate at higher frequencies - up to several kHz - for very short periods of time. However, the typical IGCT operating frequency is up to 500 Hz because of high switching losses at higher frequencies. Asymmetric IGCTs, optimized for snubberless turn-off, can operate at 6.5 kV and 4.2 kA. MOS-controlled thyristors (MCTs) and MOS turn-off thyristors (MTOs) have been proposed, but the market demand for these devices is very low at this time (8).

The need for high-voltage, high power density devices operating at high frequencies and junction temperatures higher than 150 ^{o}C is growing, especially for advanced power electronics. Silicon-based devices are not able to meet these requirements without connecting, in series and in parallel, to a large number of devices using costly active or passive snubbers and expensive cooling systems (11). For this reason, the limitations of Si material properties for power devices are currently being debated; and wide band gap semiconductors, such as SiC and gallium nitride (GaN), have attracted considerable attention.

Significant research into SiC as a material for semiconductor devices has been carried out during the last 20 years. The wide and indirect band gap enables the devices to operate at elevated temperatures (600 ^{o}C), and they still have low leakage current. The higher breakdown strength for a given blocking voltage of SiC results in ten times smaller drift layers as compared to Si. This reduces the storage of the minority carriers and the associated switching losses at a given switching frequency. Also, the switching frequency can be increased to 50-100 kHz with acceptable switching losses, which will significantly reduce the size of the magnetic components in power electronic systems.

Regardless of the advantages that SiC possesses, it has not been adopted for manufacturing of the entire range high-power devices. Difficulty with SiC crystal growth, the presence of crystal defects, such as micropipes and dislocations, and absence of abundant wafer suppliers have all contributed to a lack of progress in the fabrication of SiC power devices by the commercial sector (12). Several industrial research groups and universities have been working on the development of SiC power devices and on improving the material properties. In September 2001, two companies advertised the commercial availability of SiC Schottky diodes: Infineon (600 V up to 6 A or 300 V up to 10 A) and Microsemi (100-200-480 V, 1A) (13).

In 2001, a high-voltage PIN diode in SiC capable of blocking over 19 kV was reported (14). The diode has a forward voltage drop of 6.5 V at 100 A/cm^2. Also in 2002, the design, fabrication, and high temperature characteristics of 4H-SiC PIN rectifiers with 5, 6, and 10 kV blocking voltage were reported (15). For the 10 kV rectifier, a forward voltage drop of less than 4.8 V was observed at 100 A/cm^2 in the entire 25 to 200 ^{o}C temperature range. It has also been reported in the literature that Schottky and PIN SiC diodes have significantly less reverse current compared to the conventional fast or ultrafast Si diode (16). Now, Cree Inc. is announcing the world's first commercially available 1700 V and 10 A and 25 A silicon carbide Schottky diodes (17).

Power BJTs in SiC are very attractive for power switching applications due to their very low specific on-resistance and high-temperature operation with high power densities (18). The common emitter gain, β, the specific on-resistance, R_{SP_ON}, and the open-base breakdown voltage, BV_{CEO}, are important parameters that should be accounted for in the optimization of SiC BJTs (19). Different SiC BJTs developed in the last several years are

listed in Table 1.1. Considerable work has been done to improve device performance. One of the main challenges is to increase the low current gain, because BJTs are driven by base currents (20). The current gain of 4H-SiC BJTs is limited by the surface recombination (21). Reducing the surface recombination current by optimizing the surface passivation improves the current gain (22). Also, the common emitter current gain can be improved by increasing the minority carrier lifetime in the base and emitter regions (23). The maximum current gain for high-voltage SiC BJTs that has been reported in the literature is 110 (24).

Table 1.1. Parameters of SiC BJTs developed in the past few years.

β	R_{SP_ON}, $m\Omega.cm^2$	BV_{CEO},kV	Reference
3	28.3	6	(25)
18.8	2.9	0.757	(26)
20	10.8	1.8	(27)
20	28	>3.2	(28)
24.8	8.4	1.75	(29)
31	11.2	1.3	(30)
32	17	>1	(19)
38	14	0.48	(31)
42	9	1.75	(32)
44	8.1	3.2	(33)
44.3	8.7	5.5	(34)
60	5.2	1.2	(20)
110	3.7	0.27	(24)

To increase the blocking voltage, the growth of high-purity SiC homoepitaxial thin films on SiC single crystal wafers is required to form NN^+ wafer structures (35). The maximum open base breakdown voltage, BV_{CEO}, for SiC BJT was reported to be 6 kV (25). From the data presented in Table 1.1, it can be seen that the BJT having the highest current gain has the smallest open breakdown voltage and vice versa. Further work is

necessary to improve the design and to develop a new processing technology so that an increase in BV_{CEO} can be achieved without sacrificing the current gain of the transistor.

For Si power MOSFETs (breakdown voltage higher than 200 V), the on-resistance becomes dominated by the drift region resistance leading to an increase in the on-state voltage drop and conducting losses. Novel Si structures have allowed the breakdown voltage to extend to 600 V, but the specific on-resistance is still reasonably large which limits high frequency operation. Theoretically, the much lower drift region resistance in SiC would allow development of power MOSFETs with high breakdown voltages and smaller switching and conducting losses.

Since the introduction of the first SiC power double MOSFET (DMOSFET) in 1996 (36), different devices have been designed, characterized, and studied to improve their performances. In **Error! Reference source not found.** are presented some SiC MOSFETs developed since then. Over this period, blocking voltages have increased from 0.76 to 14 kV. For a long period of time, the power MOSFET structures developed in Si could not be directly employed for SiC devices due to the following reasons.

The first reason is that in low voltage devices, the on-resistance is caused by the low mobility of inversion electrons at the SiO_2/4H-SiC interface. Electrical quality of the interface can be improved dramatically by post-oxidation annealing in nitric oxide (NO) which leads to an increase in inversion layer electron mobility and a corresponding reduction in channel resistivity (37). Also, the introduction of a self-aligned process reduces the channel resistance; and therefore, the specific on-resistance of a well-fabricated power device is no longer limited by the channel resistance (38).

The second reason is that a high electric field occurring in the isolator (silicon dioxide (SiO_2) of a silicon carbide MOSFET can cause the device to fail during the blocking mode. The problem is aggravated at the trench corners leading to rupture of the gate oxide at higher drain voltages (39), thus restricting the maximum operating voltage. It can be solved by using a buried P^+ layer to shield the channel region (40). As a result, the electrical field in the gate oxide will reduce, increasing the reliability of the SiC MOSFETs.

Table 1.2. Parameters of SiC MOSFETSs developed in the past few years.

BV, kV	R_{SP_ON}, $m\Omega.cm^2$	Reference
0.76	66	(36)
0.95	220	(41)
0.95	8.7	(42)
1	6.95	(43)
1.1	74@100 °C	(44)
1.3	7	(45)
1.4	313	(46)
1.6	27	(47)
1.8	8	(48)
2	10.3	(49)
2.6	200	(50)
3.06	121	(51)
3.36	199	(51)
10	236	(52)
10	133	(53)
10	123	(54)
10	111	(55)
14	228	(56)

The third reason is that the injection of electrons into the oxide can take place when the electrons in the semiconductor gain sufficient energy to surmount the potential barrier

between the SiC and SiO$_2$. This can cause shifting of the threshold voltage of the MOSFET leading to reliability problems.

To make further progress in the design of MOSFETs, all limiting factors should be addressed simultaneously, especially the quality of the oxide-semiconductor interface which must be improved to allow good control over the channel mobility and threshold voltage. Despite the problems mention above, a new12 kV SiC MOSFET was ready for production and presented by Cree Inc. at the ECCE 2011 Phoenix conference.

Other unipolar power switching devices, junction gate field-effect transistors (JFETs), have also been intensively investigated. They are free of gate oxide reliability issues and are the most promising candidates for high-temperature operation since only pn-junctions are involved in the active device structure. The SiC power JFETs are still the most mature SiC devices that are close to commercialization and available as restricted samples (57). In October 2009, SemiSouth Laboratories in Starkville, MS, USA, which designs and manufactures SiC-based discrete electronic power devices, claimed the first SiC JFET (normally-off, 1.2 kV, 100 m-Ohm) used in the audio amplifier market for a new audiophile-quality power amplifier (58).

Some JFETs with high blocking voltage and low specific on-resistance reported by different research groups in the last few years are: a vertical JFET (VJFET) with a blocking voltage of 3.5 kV and less than 30 mΩ-cm^2 on-resistance (59); a VJFET with a blocking voltage of 4 kV and 45 mΩ-cm^2 on-resistance (60); a static expansion channel JFET, a normally off type with 5.3 kV blocking voltage and 69 mΩ-cm^2 specific on-

resistance (61); and a normally off 11.1 kV TI-VJFET (trenched-and-implanted vertical JFET) with 124 mΩ-cm^2 specific on-resistance (62).

One disadvantage of JFETs is that they are normally-on devices which require a negative gate voltage to be turned off. Using a cascode device comprised of a SiC JFET and a series-connected, low-voltage Si MOSFET will result in a normally-off device having a behavior very similar to a conventional MOSFET (63). The first cascode based on a SiC VJFET was reported with a blocking voltage of 4.5 kV and an on-resistance of 1.2 Ω (64). Although using a cascode makes a JFET operate as a normally-off device, there are several limitations. The maximum operating temperature of the cascode is limited by the Si MOSFET. The conduction losses increase, because the two devices are connected in series, which should be taken into consideration during the design of a power application.

As was mentioned, the rapid improvement in 4H- SiC material quality and maturing of SiC device processing have enabled the development of high-voltage SiC power devices (MOSFETs and JFETs) in recent years. However, the on-resistance of SiC MOSFETs and JFETs rapidly increases as the blocking voltage and operating junction temperature increase. This makes the conduction loss of the unipolar devices unacceptable for applications with a blocking voltage higher than 10 kV. For these applications, bipolar devices are preferred, because they have shown a small voltage drop at elevated temperatures due to strong conductivity modulation in their drift region (65).

Simple gate drive interfaces make 4H-SiC IGBTs attractive devices. Both *N*- and *P*-channel SiC IGBTs have been demonstrated with higher than 10 kV blocking voltage.

The first 10-kV *P*-IGBT on SiC was reported in 2005 (66). Since then, 12-kV *P*- channel IGBTs with 14 mΩ.cm^2 on-resistance (67), 13 kV *N*- channel IGBTs with 22 mΩ.cm^2 on-resistance (68), and 20 kV self-aligned *P*-channel DMOS-IGBTs have been reported (69). The 20 kV *P*- channel IGBT has a less than 15 times smaller voltage drop at 31 A/cm^2 current density compared to a theoretical MOSFET with the same blocking voltage (69).

A 4H-SiC thyristor is capable of higher current densities than an IGBT, because the physical mechanism for conductivity modulation is more effective in the thyristor compared to the IGBT. However, the thyristor requires more complex external circuitry as it is a current-controlled device. The first SiC symmetrical thyristors (700 V with a rated current of 6 A and a forward drop of 3.9 V) were demonstrated by Cree, Inc. (70). Since then, scientists from Cree have designed and fabricated different asymmetrical *NPNP* devices. The thyristors are made on N^+ 4H-SiC substrates, because P^+ substrates have higher resistance compared to the N^+. The limitations of the epilayer thickness and device footprint have been the main obstacles to increasing the blocking voltage and the current passing through the devices.

Different scientific groups have worked on the design, fabrication, and characterization of SiC thyristors. Some of the parameters of thyristors reported in the last few years are: 1.77 kV blocking voltage with 4 V voltage drop at 100 A and 200 $^{\circ}$C (71); 2.6 and 3.1 kV blocking voltage and 6.5 V voltage drop at 12 A (72); 7 kV blocking voltage with a voltage drop of 3.66 V at a current density of 300 A/cm^2 at room temperature and a forward voltage drop of 3.1 V at 300 A/cm^2 at 224 $^{\circ}$C (73); 4.5-kV SiC *P*-type GTO prototype with forward voltage drop of 4.6 V at a current density of 25

A/cm^2 and a turn-off energy loss of 9.88 mJ (74); 4H-SiC 7.8 kV thyristors with a graded, etched junction termination extension with forward voltage drop of 3.9 V at a current density of 100 A/cm^2 and specific on-state resistance of 5.3 mΩ-cm^2 (75); and a 12.7 kV SiC commutated GTO with leakage current less than 1 x 10^{-3}A/cm^2 at 9 kV and 250°C and onstate voltage drop at 100 A/cm^2 is 6.6 V (76).

From the literature review, it can be concluded that rapid progress (blocking voltage increasing, on-state voltage dropping, and leakage current decreasing) in the design, fabrication, and characterization of SiC power-switching devices has been made. Several SiC devices have demonstrated better performance compared to the existing comparable Si devices. SiC technology has not matured yet and has some limitations. The same limitations existed for Si when it was thought that it could replace germanium (Ge); and today, few remember the initial processing problems of Si. The SiC advantages lead many scientists to continue work on improving the quality of the material and device design. Power electronics based on SiC devices will bring a renaissance in power electronics in the future, particularly in the high power area.

1.2 Lightly Doped Drift Region Thickness

One of the requirements for choosing a proper power electronic device for a converter is that it must possess a low specific on-resistance. The specific on-resistance of a bipolar device is related to the width and doping concentration of the lightly doped drift region (N^--base). This means that the doping concentration and the width of the low-doped base region in a bipolar device must be carefully considered to achieve a desired avalanche breakdown voltage and on-resistance (conduction characteristics).

The avalanche breakdown voltage, V_{BD}, for an abrupt parallel plate junction is a function of the background doping and the semiconductor properties, such as dielectric constant, energy band gap, and impact ionization coefficient. Breakdown occurs when the carrier multiplication becomes greater than unity. Impact ionization coefficients empirically describe the exponential relationship of the applied electric field and associated charge carrier creation. The impact ionization coefficients for electrons and holes have different values, and values for semiconductor materials of interest are obtained empirically. The general ionization coefficient has been determined to have a theoretical form that is exponential and represented by (77):

$$\alpha_i = A_i e^{-\left(\frac{b_i}{\mathscr{E}}\right)^{m_i}} \tag{1.1}$$

where $\mathscr{E}$ is the electrical field (V/cm), A_i is the amplitude parameter (cm^{-1}), b_i is the ionization energy parameter related to the mean free path between collisions (V/cm), and m_i is an additional fit parameter for use with a multitude of semiconductor materials (77) (78). These parameter values depend on the semiconductor material, and they are different for electrons or holes. For Si, 6H-SiC, and GaN, m_i has been determined to be 1 for both electrons and holes (77), (78).

Near the breakdown condition, a small error is introduced by equating the impact ionization coefficients of electrons and holes to an effective ionization coefficient, α_{eff}. In this case, the breakdown voltage is defined as the applied voltage at which the summed effects described by the ionization coefficient acting over the depletion width, W, create more free charge carriers. The boundary at breakdown is when the integral (1.2) achieves

15

a value of unity (79). The associated breakdown condition in terms of the effective

ionization coefficient is:

$$\int_0^W \alpha_{eff}\, dx = 1 \tag{1.2}$$

Evaluation of this integral using Equation (1.1) is very difficult; and no analytical

expressions result, thus limiting its usefulness for device design. However, a simplified

(and purely empirical) polynomial expression for the ionization coefficient in terms of the

electric field is widely used (79):

$$\alpha_{eff} = K\mathcal{E}^7 \tag{1.3}$$

The two previous fit parameters, A_i and b_i, are absorbed into the prefactor, K. The

coefficient, K, is expressed in terms of new parameters, A, b, and m, that are averages of

the previous A_i, b_i, and m_i values, expressed in Equation (1.1) for holes and electrons

(78):

$$K = 9 \times 10^{-38} \frac{A216^m}{b^{0.85} E_G^{15}} \tag{1.4}$$

where E_G is the band gap energy (eV) for the semiconductor material of interest.

For a one-sided abrupt P^+-N junction, the electrical field and the voltage across the

lightly doped region are functions of the depletion distance and depend on the impurity

doping concentration, N_{D1}, in the lightly doped N-base and the depleted N-base width, W.

The electric field and voltage relations are presented in Equations (1.5) and (1.6), respectively.

$$\mathscr{E}(x) = \frac{q}{\varepsilon} N_{D1}(W - x) \qquad (1.5)$$

$$V(x) = \frac{q}{2\varepsilon} N_{D1}(W - x)^2 \qquad (1.6)$$

The maximum electrical field is observed at junction ($x = 0$). Using this and substituting Equation (1.5) in Equation (1.3) and then substituting into the integral (1.2), one can obtain the minimum width of the depletion layer, W_{min}, at breakdown (78).

$$W_{min} = \left(\frac{K}{8} \frac{q^7}{\varepsilon^7} N_{D1}^7 \right)^{-\frac{1}{8}} \qquad (1.7)$$

The corresponding breakdown voltage can then be determined from Equation (1.6) as:

$$V_{BD} = \left(2K \frac{q^3}{\varepsilon^3} N_{D1}^3 \right)^{-1/4} \qquad (1.8)$$

It should be noted that the permittivity is correctly placed in the denominator in Equation (1.8), not in the numerator as was presented in the expressions from (78).

To reduce the lightly doped region width and maintain the same breakdown voltage requires the addition of a highly-doped N^+ buffer layer at the end of the drift (N-base) region to create a $P^+N^-N^+$ structure. This will modify the expressions for the minimum width of the depletion layer, W_{min}, and the corresponding breakdown voltage, V_{BD}.

Reducing the width of the base region will decrease the effective on-resistance during conduction and reduce the volume of stored charge, thus decreasing the turn-off (and turn-on) time.

Anantharam and Bhat, 1980, calculated the breakdown voltage as a function of the thickness of the intrinsic layer, W_I, by solving the ionization integral. It was assumed that the PT voltage of the purely intrinsic region was equal to zero, and the breakdown voltage was given by (80):

$$BV = \frac{W_I^6}{A}.$$ (1.9)

The first objective of this dissertation is to extend the concepts for the breakdown voltage of the PT diodes with abrupt junctions using the theory of the average ionization coefficient and investigate the modifications due to the PT structure.

1.3 Overview of Models

The rapid developments in semiconductor technology over the past few years have led to a remarkable increase in interest in device modeling. It is necessary to understand the detailed operation of the devices and to optimize their design. This implies that device modeling now plays an essential role in modern technology. As the scale of the semiconductor devices decreases and the complexity of the physical structure increases, the modeling concepts become more complicated. Also, the difficulty connected with measuring some of the semiconductor device's parameters means that the results obtained from the theoretical characteristics must be highlighted. Modeling also allows new device structures to be accurately investigated prior to fabrication.

In (81) there are six proposed model levels that can be adapted for categorization of the device models in any circuit simulator or finite element (or finite difference) simulator. The categorization of the levels begins with simple behavioral models and then moves to more complex physics-based models. Different model levels have been developed using different programing languages. A brief review of these six model levels is presented below.

1.3.1 Level 0 Model

The Level 0 model is a behavioral model that does not have a real physical representation. In other words, this model can be considered as an ideal electrical switch with two stages: no current flow, when the device is in blocking condition, and no forward voltage drop, when it is in conducting condition. In order to assist numerical convergence during the simulation, the commutation time may either be zero (instantaneous) or finite. Thermal or power loss data cannot be obtained with this model. For the model to work, some parameters, such as maximum forward or reverse blocking voltages and maximum forward current, and the current and voltage directions should be specified. The model allows fast, rough simulation and can be used in the early stages of the design process. One of the applications of the Level 0 model is for simulation of many switching cycles.

1.3.2 Level 1 Model

A Level 1 model is a behavioral model, suitable for basic system-level modeling where the circuit methodologies are tested, validated, and compared. It models only the

basic properties of the devices: forward voltage drop as a function of forward current and temperature, and turn-on and turn-off switching losses as a function of current and voltage. This model does not calculate triggering losses. Breakdown voltage limits, maximum forward conduction-current limits, and maximum junction-temperature limits are imposed. The junction temperature of the device is estimated by the simple multisection resistor-capacitor (RC) equivalent network.

1.3.3 Level 2 Model

Level 2 models predict the same basic physical properties and behavior as the switching characteristics of semiconductor devices. They are one dimensional and are a simplified physical-properties-based system. These models include all of the features of the Level 1 model, but they are not behavioral models. They accurately describe the dynamic characteristic within the device except the operating area. An example of a Level 2 model is a lumped-charge model.

The lumped-charge modeling technique was first introduced by P.O. Lauritzen and C.L. Ma in 1991 (82). The technique is based on Linvill's lumped-parameter approach and the standard charge control method. It has been successfully used to create diode (82), BJT (83), Si controlled rectifier (SCR) (84), GTO (85), MCT (86), and MOSFET (87) models. The basic idea is to divide the device into several critical regions; each of these regions contains one charged storage node and up to two connection nodes. The electron and hole values of the charge at each node are equal to the product of the region volume and carrier concentration at each node. Then, the charge nodes are linked using a set of equations related by semiconductor physics and circuit theory.

Based on the physical equations, the injected carrier distribution inside the device is determined with a given external circuit condition. The voltage drops across each segment are calculated based on the carrier distribution at different nodes. The lumped-charge model captures some of the physical behavior of the device, but it does not provide adequate detail for the carrier distribution profile in the base and low-doped drift regions. The models are not easy to adapt to incorporate all thermal dependencies and implementation for use in circuit simulators.

1.3.4 Level 3 Model

Level 3 models are typically full physics-based models. Beside the external electrical characteristics, internal physical and electrical information, such as the junction temperature and carrier distribution in different regions of the device, can be obtained. This requires solving the Ambipolar Diffusion Equation (ADE) by using some of the numerical algorithms: Fourier series, Laplace transformation, internal approximation, or difference methods. In most cases, due to high level injection, the ADE is assumed to be one dimensional, which is valid for the power semiconductor devices.

The Level 3 models using Fourier series solutions for solving the ADE in the lightly doped drift region have been developed for Si diodes, IGBTs (88), (89), and IGCTs (90).

1.3.5 Level 4 Model

This is a complete, complex physical-properties-based model that captures all of the relevant physical parameters of the device, such as the motion of charge carriers and the

associated electrical fields. The models are process based and should be able to have full two- or three-dimensional representation of the device design. They can also give information about the failure behavior of the device during operation outside of the safe operation area. The models could be implemented by using finite-element techniques; but due to their complexity, no analytical models exist.

1.3.6 Level 5 Model

These models have the ability to precisely simulate degradation effects that occur in the device during long periods of operation. The models take long-term radiation and degradation into account as well as any effects due to power or thermal cycling. Such models can be used to predict a failure of the device due to degradation. Because of their complexity, very few Level 5 models for power semiconductor devices exist (81).

1.4 Power BJT Models

Since the invention of BJT in 1947, scientists have attempted to describe the behavior of the BJT by using different models. The coupled diode model, developed by Ebers and Moll in 1954 (91), is one of the first BJT models and is widely used in simulating the static behavior of bipolar transistor circuits. A main advantage of the model is its mathematical simplicity; but the disadvantages are that the model neglects various phenomena that can occur in transistors, such as high injection in the base, emitter crowding, breakdown, space-charge-limited flow in the collector, appreciable net recombination in junction transition regions, etc. In 1970, a compact bipolar transistor model (integral charge control model (ICM)) was developed by Gummel and Poon (92). It basically includes many high-level effects, such as conductivity modulation, base push-

out effect, Early effect, and impact ionization. Most SPICE simulators use the Gummel-Poon model for modeling of signal BJTs, but it is inaccurate for modeling of power BJTs (93).

The power BJT models published to 1992 describe the static characteristics, for instance, the quasi-saturation effect, without considering the recombination (94) (95) or giving some dynamic characteristics; but they only take into account the quasi-static behavior of the charge in the collector layer (96), (97). These models do not include the charge in the lightly doped collector which is substantial for determining the dynamic behaviors of a power BJT. A power BJT model, including the charge in the lightly doped collector layer, was proposed by Xu and Schröder in 1992 (98). The model uses an empirical solution to the diffusion equation and sometimes has convergence problems during the transistor switching. Goebel et al., 1993 (99), presented a unified method for modeling power devices based on a hybrid algorithm that solves the equations describing the semiconductor part numerically and part analytically. The method is more exact but requires higher computation time.

Bayer et al., 1994, presented a circuit model of a BJT based on the calculation of the charge carrier distribution in the base and the lightly doped collector region by approximation of the time derivatives (100). Two years later, Talwalkar et al., 1996, proposed a lumped-charge method for modeling a BJT using simplified forms of Poisson's equation, the continuity equation, and the Boltzmann relation (83). It is a Level 2 model that includes all physical effects, such as base widening, recombination in the base, emitter, and collector and base conductivity modulation.

It was mentioned in Section 1.1 that power BJTs have been completely replaced by MOSFETs and IGBTs. This can also be seen on the modeling side. No more models have been proposed for power Si BJTs since then. Now, the new technology, using SiC for the power BJT, requires the development of more precise power BJT physics-based models. The models should provide all of the external electrical characteristics and internal physical and electrical information for the BJT.

Most of the research groups have used some old, already-developed models for Si power BJTs and have only changed the properties of Si to SiC. An example worth mentioning is the modeling of dc gain performance of 4H-SiC BJTs by using a 2D device simulator, PISCES-IIB (101).

The second objective of this work is to develop a new physics-based Level 3 model to model the transient processes in 4H-SiC BJT using the Fourier series for solving the ADE in the lightly doped collector region. The model should be realized using Matlab and Simulink.

Chapter 2 – Silicon Carbide Material

2.1 Introduction

This chapter includes an introduction to SiC as a material for power electronic devices. The chapter starts with a brief history of the material, including the very first reported discovery of SiC, right up to the latest existing semiconductor technology. Then, it is followed by details of the physical characteristics of SiC, in parallel with highlights on the advantageous properties from electrical and thermal perspectives.

2.2 History of Silicon Carbide

Silicon carbide is one of the oldest compounds in the universe. It is older than our solar system, and it has been floating around the Milky Way for billions of years as stardust that was generated in the atmospheres of carbon-rich red giant stars (102). In 1924, a Swedish chemist, Jöns Jacob Berzelius, discovered SiC while trying to make a diamond. The material was first used as an alternative to diamond for cutting and polishing. Sixty-seven years after Berzelius' discovery, Eugene G. Acheson of Monongahela, Pennsylvania, melted coke and silica in a furnace and found a crystalline product characterized by great hardness. The mineral produced could substitute for diamond as an abrasive and cutting material. It was called "carborundum" from Al_2O_3, which is called "corundum." Later, it was found that the new compound was made up of silicon and carbon; however, SiC is still known as "carborundum." The first commercial process to synthesize SiC in the form of a polycrystalline powder was the Acheson process developed and patented in 1893.

In 1905, Moissan found the first natural SiC crystal in a meteorite. Because of this discovery, mineralogists refer to natural SiC as "moissanite" (103). Two years later, a British experimenter, H.J. Round of Marconi Labs, discovered electroluminescence by using a crystal of SiC and a cat's-whisker detector (104). In 1913, Baumhauer used the word "polytype" to describe the ability of SiC to crystallize into different forms varying only in their stacking mode (105). Since then, the research in SiC did not progress far until J.A. Lely at Philips Research Labs in Einhoven (1955) developed a small-scale sublimation technique for growing high purity, good crystallinity SiC crystals for semiconductor purposes (106). This significantly increased the interest in SiC as a semiconductor material, with it becoming even more popular than Si and Ge. The first SiC conference was held in Boston in 1958. However, the initial interest was diverted from SiC to Si because of the advances in silicon processing technology. During the silicon era, there was still some SiC research going on, especially in the former Soviet Union.

In 1978, Tairov and Tsvetkov developed the seeded sublimation process (107) which marked the start of the second stage in the SiC evolution as semiconductor material (102). The first commercial move into SiC growth for semiconductor devices was evident after heteroepitaxial growth of cubic silicon carbide on foreign substrates was introduced in 1981 (108). The interest in SiC technology started again when researchers realized that Si technology had peaked and new semiconductor materials were required with capabilities beyond that of Si.

In 1987, Cree Research was founded. The introduction of 25 mm single crystal wafers of 6H-SiC by Cree in 1990 activated and initiated SiC research and gave new life

to the use of SiC in device development. At present, 35 mm diameter wafers of both 4H

and 6H SiC are commercially available from Cree Research (Durham, NC, USA) and

Advanced Technology Materials, Inc. (Danbury, CT, USA). Wafers 75 mm in diameter

have been prototyped by both Cree and Westinghouse (now Northrup Grumman). Cree

was the first to sell devices and quality SiC substrates, and they continue to research ways

to surmount the limitations connected with SiC technology. In August 2011, Bridgestone

reported that the company had developed a 5-inch SiC wafer. The company is currently

working on the development of 6-inch SiC wafers and is planning to bring them to

market during the latter half of 2012 (109).

2.3 Silicon Carbide Polytypes

SiC is known as a classical polytypic substance existing in more than 250

polytypes; and the common polytypes are 6H, 15R, 4H, and 3C (110). All polytypes

have a hexagonal frame with a carbon atom positioned at the center of the mass of the

tetragonal structure outlined by the four neighboring Si atoms, and the distance between a

carbon (C) atom to each of the Si atoms is the same (111). Figure 2.1 shows a tetragonal
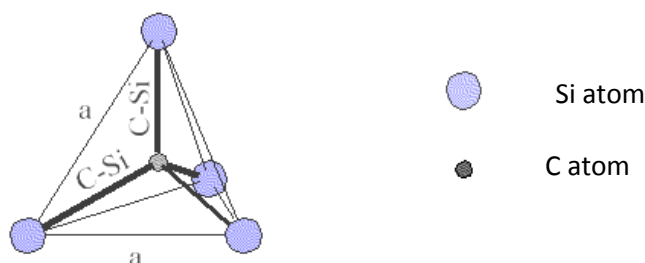
Figure 2.1. The tetragonal bonding of a carbon atom with the four nearest silicon neighbors (111).

shape formed by four silicon atoms bonded to the carbon atom.

Polytypes are formed by stacking SiC molecules on top of each other in a certain order. The stacking order between succeeding double layers of carbon and silicon atoms determine the difference between different polytypes. The stacking sequence for the three most common polytypes, 3C, 4H, and 6H, is shown in (112). If the first double layer has an A position, the next layer that can be placed, according to a closed packed structure, will be placed on the B position or the C position. The different polytypes are created by permutations of these three positions. For instance, a stacking sequence, ABCABC … or ACBACB…, represents a 3C-SiC polytype. The number in the formula of a polytype denotes the periodicity. The letter H, C, or R denotes the overall lattice type as being hexagonal, cubic, or rhombohedral, respectively.

During substrate manufacturing for semiconductor devices, it is important that the entire wafer is a single polytype. Growth conditions during substrate production should be stable, because any instability in the growing process will lead to spontaneous switching from one polytype to another. This will alter the electrical properties of the
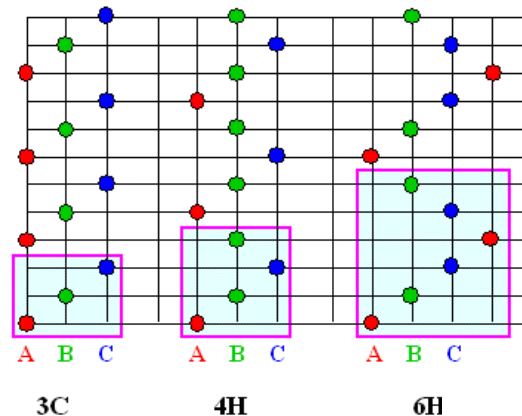
Figure 2.2. Illustration of common SiC polytypes 3C, 4H, and 6H (112).

material and act as a nucleation site for micropipes (113).

Currently, two SiC polytypes are accepted in SiC research: 6H-SiC and 4H-SiC. Before the introduction of 4H-SiC wafers in 1994, 6H-SiC was the dominant polytype. Since then, both polytypes have been used in research; but recently, 4H-SiC has become the more dominant polytype. This is because the mobilities in 4H-SiC are identical along the two planes of the semiconductor, whereas the 6H-SiC polytype exhibits anisotropy, which means that the mobilities of the material in the two planes are not the same.

2.3.1 Silicon Carbide Physical Properties

Silicon carbide displays a wide range of properties, such as high breakdown electric field strength, high thermal conductivity, high saturated drift velocity, and high thermal stability, which make it attractive for use as a material for semiconductor devices. Table 2.1 summarizes some of the physical properties for the most popular wide band gap semiconductors and Si. The most important properties that benefit 4H-SiC devices are explained in the following sections.

Table 2.1. Physical properties for various semiconductors.

Material	E_G, eV	$\mathscr{E}_C$, MV/cm	n_i, cm^{-3}	μ_r, cm^2/Vs	v_{SAT}, 10^7 cm/s	σ_T, W/m.K	CTE, ppm/K
Si	1.1 [114]	0.3 [114]	10^{10} [114]	1400 [114]	1.02 [114] [114]	130 [114]	2.6 [114]
GaAs	1.424 [114]	0.4 [114]	2.1×10^6	8500 [114]	2.0 [115]	55 [114]	5.73 [114]
3C-SiC	2.36 [116] [115]	1 [116]	10 [118]	≤ 800 [116]	2.0	360 [116]	3.8 [116]
4H-SiC	3.23 [116]	3-5 [116]	8.2×10^{-9}	≤ 900 [116]	2.0	370 [116]	5.12 [116]
6H-SiC	3.0 [116]	3-5	2.3×10^{-6}	≤ 400 [116]	2.0	490 (116)	4.3-4.7 [116]
GaN	3.39 [116])	3-5 [116]	1.9×10^{-10}	≤ 1000 [116]	2.2	130 [116]	3.2-5.6 [116]
Diamond	5.45 [117]	5.6 [117]	1.6×10^{-27} [117]	1900 [117]	2.7 [117]	600-2,000 [117]	0.8 [117]

2.3.2 Wide Band Gap

To understand the basic fundamental transport properties in a material, knowledge about electron band structure near the fundamental band gap is essential. In solid state physics, a band gap is an energy range where no electron states exist. It refers to the energy difference (in electron volts) between the top of the valence band and the bottom of the conduction band, which is found in insulators and semiconductors. Band gap is the amount of energy required to free a valence electron from its orbit around the nucleus so that it becomes a mobile charge carrier, capable of free movement in the solid.

SiC is from the IV-IV group semiconductor family and has an indirect band gap. Every polytype has a different band gap. See the schematic energy band structures of 4H-SiC in Figure 2.3 (116), (120). The doping levels and the optically excited photocarriers are slightly low in the system. Therefore, the band edge transition, where the parabolic bands can be approximated, as characterized by carrier effective masses, should be considered (120).

The highest occupied state of the valence band is at the Γ-point, as the energy separation between Γ_{15v}-valley and Γ_{1c}-valley is $E_\Gamma = $ 5-6 eV. The conduction band
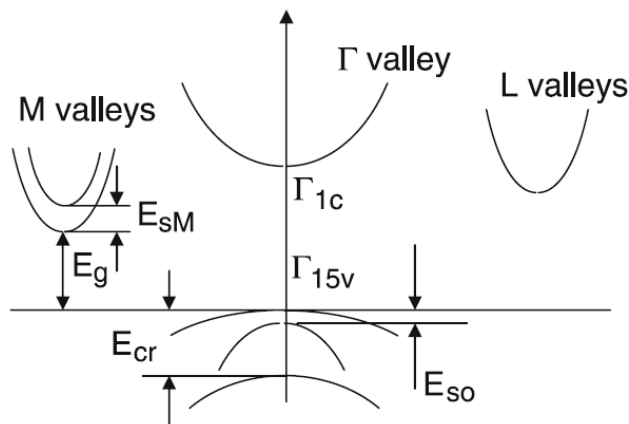
Figure 2.3. Band structure of 4H-SiC (120)

minimum is at the *M*-point, and it determines the band gap of 4H-SiC $E_g = 3.26$. There is

a second minimum of the conduction band at the *M*-point, which is approximately 0.1 eV

above the lowest unoccupied state. The energy separation between Γ_{15v}-valley and *L*

valley is approximately 4 eV. Other relevant physical parameters of the energy band

structures are: energy of spin-orbital splitting E_{so} = 0.007 eV and energy of critical-field

splitting E_{cr} = 0.08 eV.

Some of the electrical properties of the semiconductor materials, such as critical

electrical field, intrinsic carrier concentration, mobility, and conductivity, are strongly

dependent on the band gap. These dependencies of 4H-SiC will be discussed next.

2.3.3 High Critical Electric Field

An expression for the critical electrical field in the band gap energy for the indirect

band gap materials is (121):

$$\mathcal{E}_c = 2.38 \times 10^5 E_G^2 \tag{2.1}$$

There is no dependence on the background doping included in this expression,

because the voltage blocking capability, during the off-state of power electronic devices,

depends on the property of the lightly doped drift region.

The critical electric field of SiC is higher as compared to Si, because it has a wider

band gap. A wider band gap of SiC indicates that energy required to break a bond is

significantly higher compared to the energy required for Si. This allows a larger electrical

field to be applied before the avalanche of a multitude of ionized carriers occurs in the

semiconductor. The more than ten times higher critical electric field of SiC compared to

Si allows power devices to be designed with thinner, more highly doped drift regions for

the same blocking voltage.

Figure 2.4 presents a theoretical, specific on-state resistance of blocking regions

designed for certain breakdown voltages in Si and 4H-SiC, under optimum punch-

through conditions (122). Also, the specific on-resistance can be related to the

breakdown voltage, BV, electron mobility, μ_n, dielectric constant, ε, and critical electric

field strength, $\mathcal{E}_C$, by the following equation:

$$R_{SP-ON} = \frac{4BV^2}{\varepsilon \mu_n \mathcal{E}_C^3} \qquad (2.2)$$
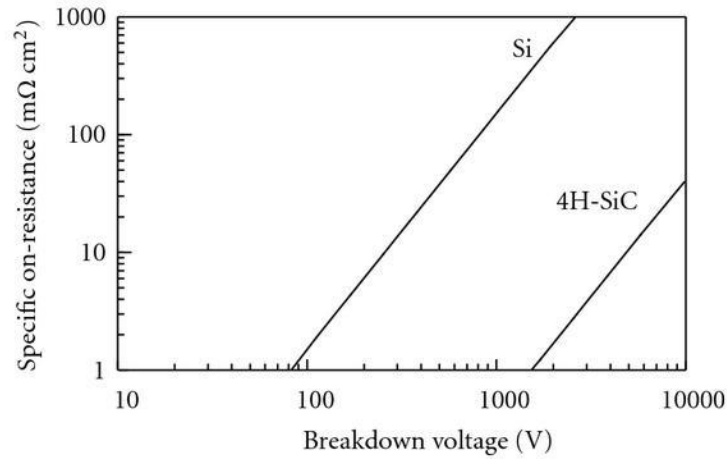
Figure 2.4. Theoretical, specific on-state resistance of the blocking regions in function of the breakdown voltages for Si and 4H-SiC (122).

From Figure 2.4 and Equation (2.2), it can be deduced that, for the same blocking

voltage, SiC devices offer specific on-resistance that is around 350 times lower than their

Si counterparts. The doping concentration also affects the blocking voltage. For the

same blocking voltage, the background doping in a SiC device is 10 to 100 times higher

than that of a Si device. An increase in doping concentration will also lead to a decrease in specific on-resistance. This is one of the most important advantages of high-voltage SiC; because for the same blocking voltage, the on-resistance is much lower. The fact that the devices can be made thinner and more highly doped means that SiC devices have the capability of operating at a higher frequency. Thinner devices are faster, because the carriers do not have to travel as far through the device.

2.3.4 Low Intrinsic Carrier Concentration

The intrinsic carrier concentration of a semiconductor completely free of impurities and defects is the number of excited electrons from the valence band to the conduction band (and also the number of excited holes in the valence band) per unit volume. It is given by the equation:

$$n_i = N_S e^{-\frac{E_G}{2kT}} \tag{2.3}$$

where N_S is the number of effectively available states per unit volume; E_G is the energy band gap; k is Boltzmann's constant (1.381×10^{-23} J/K); T is the absolute temperature in Kelvin, and it is assumed that $kT \leq E_G/5$.

Due to the wide band gap of SiC, its intrinsic carrier concentration is approximately 8.2×10^{-9} cm^{-3}, while the intrinsic carrier concentration of Si is 10^{10} cm^{-3}. Wide band gap semiconductors have the advantage of operating at high temperature and radiation. As the temperature increases, the electron's thermal energy in the valence band increases leading to an uncontrolled condition that should be avoided. The temperature at which this condition occurs for Si is about 150 ^{o}C, while SiC has a wide bandgap; and the

valence electrons require more thermal energy to move from valence to the conducting band. This intrinsic temperature for SiC is approximately 900 $^{\circ}$C.

Radiation energy can also excite an electron and make it move to the conducting band. Similar to temperature, a wide band gap material will require more radiation energy to free an electron from the conducting band.

As a result of a wide band gap, devices built with SiC can endure more heat and radiation without losing their electrical properties. These devices can operate in extreme conditions where Si-based devices cannot operate.

2.3.5 High Saturated Drift Velocity

The saturated drift velocity is also one of the most important device-related characteristics of a semiconductor, because it determines the frequency limits of the devices and, consequently, the range of their most efficient use. The high frequency capability of a semiconductor material is directly proportional to the material drift velocity. The drift velocity of 4H-SiC ($2x10^7$ cm/s) is twice as large as the drift velocity of Si (10^7 cm/s); hence, it is expected that 4H-SiC-based power devices could be switched at higher frequencies compare to their Si counterparts. In addition, higher drift velocity allows charge in the depletion region to be removed faster; therefore, the reverse recovery current is smaller, and the reverse recovery time is shorter.

2.3.6 High Thermal Stability

As was mentioned previously, one of the advantages of 4H-SiC-based semiconductor devices is that they can operate at high temperatures due to the wide band

gap in 4H-SiC material. Besides this, 4H-SiC has another thermal advantage - high thermal conductivity. This means that SiC devices can operate at higher power densities.

The junction-to-case thermal resistance (R_{th-jc}) of a device can be calculated by:

$$R_{th-jc} = \frac{d}{\lambda A}$$
(2.4)

where λ is the thermal conductivity (W.cm^{-1}.K^{-1}); d is the length (cm); A is the cross-section area (cm^2).

With more than three times higher thermal conductivity (4.9 W.cm^{-1}.K^{-1}) compared to Si (1.5 W.cm^{-1}.K^{-1}), the junction-to-case thermal resistances of 4H-SiC devices are three times lower than their Si counterparts, taking into account Equation (2.4). Lower R_{th-jc} indicates that the heat generated in 4H-SiC devices during the operation could easily be spread to the case, heat sink, and then to the environment. An advantage of 4H-SiC devices is faster heat dissipation, reducing the requirement for a heavy heat sink and complex thermal packaging. There is also a real benefit in terms of long-term reliability, as this allows the device to maintain a maximum output power.

2.3.7 High Coefficient of Thermal Expansion

All materials change their size when subjected to a temperature change as long as the pressure is held constant. The coefficient of thermal expansion (CTE) describes a change in the size of an object with a change in the temperature. It is the fractional change in the volume of the object per degree change in temperature at a constant pressure. During the design of high-voltage semiconductor devices, it is necessary for the semiconductor CTE to closely match the package substrate CTE.

The CTE of 4H-SiC (5.2 ppm/K) is two times bigger compared to the CTE of Si (2.6 ppm/K). The CTE of package materials is higher than 4.5. The best matches of the package materials and 4H-SiC are: AlN substrate (4.5 ppm/K), Beryllia (BeO) substrate (6.1 ppm/K), and Al_2O_3 (Alumina) substrate (6.5 ppm/K).

Chapter 3 – Physics of Power Semiconductor Devices

3.1 Introduction

Power semiconductor devices are generally used as switches in power electronic circuits. An ideal power semiconductor switch should be able to carry any amount of current with zero on-state voltage drop when it is in the forward conduction mode, and it should be able to hold off any value of voltage with zero leakage current when it is in the reverse blocking mode. In addition, the time for switching from one mode to another should be zero. Unfortunately, real semiconductor switches have a finite voltage drop during the on-state leading to conduction power losses; and they also have leakage current during the off-state leading to power loss. Their switching time is not zero. The power dissipation in power devices increases with increases in the voltage rating, because the on-state voltage drop also increases. For that reason, the doping concentration and the thickness of the drift region of a power semiconductor device must be optimized so the device can hold a maximum blocking voltage and the conduction losses are minimized.

The operation of semiconductor devices can be analyzed using six basic equations governing the behavior of semiconductor devices: Poisson's equation, Maxwell's equation, two carrier continuity equations, and two current transport equations. The

behavior of the semiconductor devices depends on the mode of operation. Some characteristics of the two modes, on-state or conductive mode and off-state or reverse mode, will be introduced in detail in this chapter.

3.1.1 On-State

Power semiconductor bipolar devices, such as diodes, BJTs, thyristors, and IGBTs, operate under steady-state conditions at current densities on the order of several hundred amperes per centimeter squared. At these high current densities, large carrier injection levels exist; and, therefore, some of the crystal properties are significantly modified compared to the properties at low injection levels. As a result, the semiconductor device properties are also changed; and their behavior during the high injection level cannot be described using small-signal theory.

A high injection level is defined as the level at which the injected minority carrier density exceeds the majority carrier concentration during the equilibrium. Therefore, during the high-level injection, the injected carrier densities are greater than the doping densities in all device regions with the exception of the highly doped N^+ and P^+ layers. The lightly doped regions are most affected by the high-level injection.

A lightly doped drift region in a power semiconductor device has low conductivity during the low injection level. The absence of a depletion region and stored charge are the main reasons for this. In order to increase conductivity, carriers must be injected into the lightly doped drift region. This is known as conductivity modulation, and it is a typical feature of all bipolar power devices.

During the high injection level, the injection of the carriers into the lightly doped drift region is caused by the current flowing across a large difference in doping levels. In order to preserve the charge neutrality, the concentration of electrons and holes in the drift region should be equal. This is known as quasi-neutrality $(p \approx n)$. Carrier distribution in a lightly doped drift region during a high injection level is depicted in Figure 3.1. Electrons are injected from the N^+ emitter to the lightly doped N^- drift region, and holes are injected from the P emitter to the drift region, too. The drift region doping level, N_B, is negligible compared to the excess carrier density in the drift region during the high-level injection.
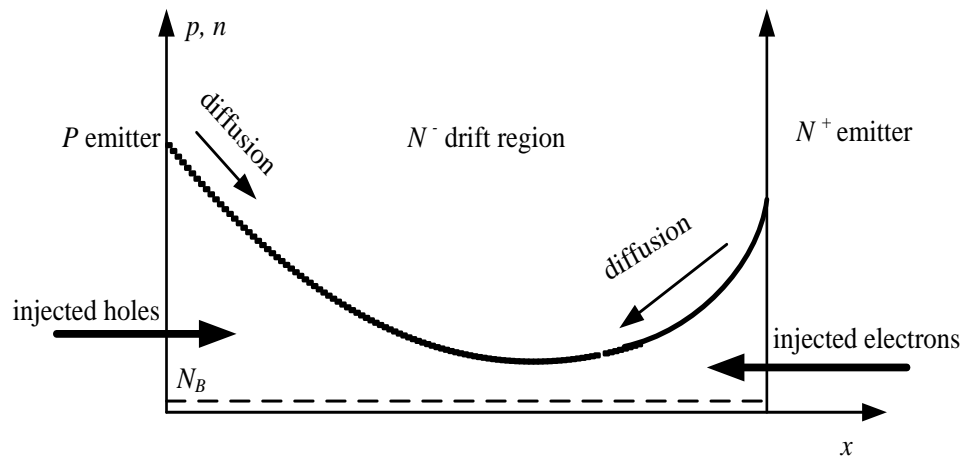
Figure 3.1. Typical carrier distribution in the N^-- drift region during high level injection.

Due to the carrier scattering mechanism at high injection levels, the hole and electron mobilities become much smaller compared to their mobility at low concentration. They become equal to each other $(\mu_n = \mu_p = \mu)$. The electron and hole

diffusion constants also decrease due to the scattering mechanism, and their values became equal to each other and almost equal to the ambipolar diffusion constant $(D_n = D_p = D)$.

The carrier lifetime is defined as the average time taken for an excess minority carrier to recombine. Three recombination mechanisms, band-to-band, trap-assisted (or Shockley-Read-Hall (SRH)), and Auger recombinations, determine the carrier lifetime. At low and moderately high injection levels, the recombination of carriers is adequately described by SRH theory, as the recombination is determined by the amount of impurities and defects in the material. In the region where $n \approx p \approx 10^{15} - 10^{17}$, the SRH carrier recombination rate is given:

$$R_{SRH} = \frac{p}{\tau_n + \tau_p} = \frac{p}{\tau_{HL}}$$
(3.1)

where τ_n, τ_p, and τ_{HL} are electron, hole, and high-level injection lifetimes.

At very high injection levels, due to the high minority and majority carrier concentrations, the other two recombination processes, band-to-band and Auger, may also become important. The direct radiative, band-to-band recombination involves two carriers (a hole and an electron) without an intermediary trap. In this case, both carrier types should be available in the recombination process. Therefore, the rate is expected to be proportional to the product of n and p. Auger recombination involves three particles, an electron and a hole recombination in a band-to-band transition as the released energy is passed on to another electron or hole. The expression for the net recombination rate includes the density of the electrons or holes which receive the released energy from the

electron-hole annihilation. Auger recombination is significant only for very high injected

carrier densities ($\geq 10^{17}$). In this case, the recombination rate is calculated by:

$$R_{AUG} = (C_n + C_p)n^3 \tag{3.2}$$

where the Auger coefficient for SiC at 300 K is $C = C_n + C_p \approx 7 \times 10^{-31}\,\text{cm}^6/\text{s}$ (117).

Emitter recombination in the heavy doped emitter regions is also observed at high-

level injection. For a high-voltage diode, there is a hole concentration at the N^+N^-

junction and also a high electron concentration at the PN^- junction due to the equal

concentrations of holes and electrons (Figure 3.1). As a result of these high

concentrations, the minority carriers flow into the heavily doped N^+ and P region and

recombine with electrons and holes, respectively. This phenomenon is known as emitter

recombination. The minority current densities for the two emitters are calculated by:

$$J_{n(N^+N^-)} = qh_n p^2_{(N^+N^-)} \tag{3.3}$$

$$J_{n(PN^-)} = qh_p p^2_{(PN^-)} \tag{3.4}$$

The carrier densities are expressed in p; because at the N^+N^- and PN^- junctions,

$p \approx n$ due to the high-level injection. The recombination parameters, h_n and h_p, are

functions of the emitter doping levels (N_{N^+}, N_P), the minority carrier diffusivities

($D_{nP}, D_{P_{N^+}}$), and lifetimes ($\tau_{nP}, \tau_{P_{N^+}}$) (123) are calculated by:

$$h_n = \frac{1}{N_{N^+}} \sqrt{\frac{D_{P_{N^+}}}{\tau_{P_{N^+}}}} \qquad (3.5)$$

$$h_P = \frac{1}{N_P} \sqrt{\frac{D_{n_P}}{\tau_{n_P}}} \qquad (3.6)$$

3.2.2 Off-State

During the off-state of power devices, the voltage is supported across a depletion layer formed across either a *PN* junction, a metal semiconductor interface (Schottky barrier), or a metal-oxide-semiconductor interface (MOS). The electrical field existing across the depletion layer is responsible for sweeping out the minority carriers randomly entering the layer. The sweeping is due to space charge generation or diffusion from the neighboring quasi-neutral regions. Increasing the reverse bias voltage, the electrical field in the depletion layer increases and accelerates the mobile carriers to high velocity. At a high electric field, the mobile carriers have sufficient kinetic energy that the collision can free a valence electron from the atom or cause an electron from the valence band to jump into the conduction band, thus creating an electron-hole pair. This phenomenon is known as impact ionization.
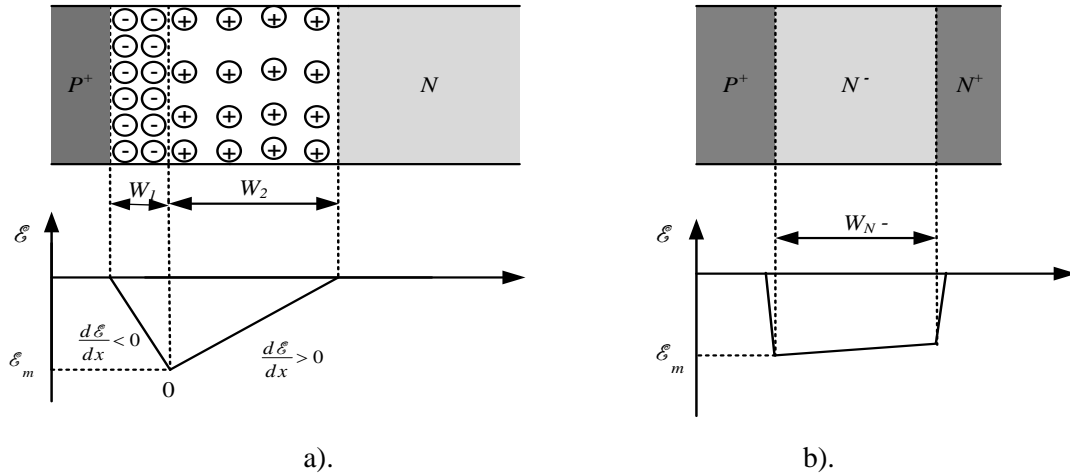
Figure 3.2. The electrical field within: a) P^+N structure; b) $P^+N^-N^+$ structure.

To achieve a high blocking voltage, a power semiconductor device has a lightly doped drift region.   Since the forward voltage drop during the on-state is mainly determined by the thickness of the drift region, it is important to obtain a breakdown voltage as close as possible to the intrinsic capability of the material to optimize device performance (124).

The shape of the electric field within the depletion layer for an abrupt P^+N junction is shown in Figure 3.2a). With the following approximations, the carrier concentrations are assumed to be negligible compared to the doping concentration in the depletion layer; and the charge density out of the depletion layer is assumed to be equal to zero.

In the case shown in Figure 3.2a), where the N- type material on the right side is lightly doped and N_D is low, the electrical field has a shallow positive slope. While the P-type material on the left side is heavily doped, the value of N_A is higher; and the electric field has a steep negative slope. Since the doping level, N_A, in P-type material is

much greater than the doping level, N_D, in the N-type material, a large negative gradient of the electric field exists in the P region with a very small depletion width, W_2.

To reduce the thickness of the drift region for the same blocking voltage, a heavily doped N^+- type buffer layer should be added to the end of the drift region to create a $P^+ N^- N^+$ structure (Figure 3.2b)). Due to the high doping level in the buffer layer, the gradient of the electrical field will be steep and positive, in the same way as in the P-type region. The electrical field has maximum value at the $P^+ N^-$ junction. The electrical field in the drift region will decrease gradually with no requirement for an excessive depletion layer width. The phenomenon that occurs when the depletion layer extends across the entire drift region is known as punch-through.

Consider a two-dimensional $P^+ N^- N^+$ structure under equilibrium conditions with the doping profile sketched in Figure 3.3. The electric field in the different regions can be obtained by substituting the charge densities into Poisson's equations and then integrating:

$$\mathcal{E} = \begin{cases} (q/\varepsilon)N_{D2}x & 0 \leq x \leq d_1 \\ (q/\varepsilon)\left(N_{D1}x + d_1\left(N_{D2} - N_{D1}\right)\right) & d_1 \leq x \leq d_1 + W \\ (q/\varepsilon)N_A(d_1 + W + d_2 - x) & d_1 + W \leq x \leq d_1 + W + d_2 \\ 0 & x \leq 0 \ \text{ and } d_1 + W + d_2 \leq x \end{cases}$$

(3.7)

where the respective impurity doping concentrations for the $N^+ N^- P^+$ regions are N_{D2}, N_{D1}, and N_A. The corresponding depletion region thicknesses of each section are d_1, W, and d_2.

The maximum electric field of the $P^+N^-N^+$ structure will be at the N^-P^+ junction ($x = d_1 + W$). Charge neutrality from Equation (3.7) gives the depletion thickness, d_2, of the P^+ region as:

$$d_2 = (N_{D1}W + N_{D2}d_1)/N_A \qquad (3.8)$$
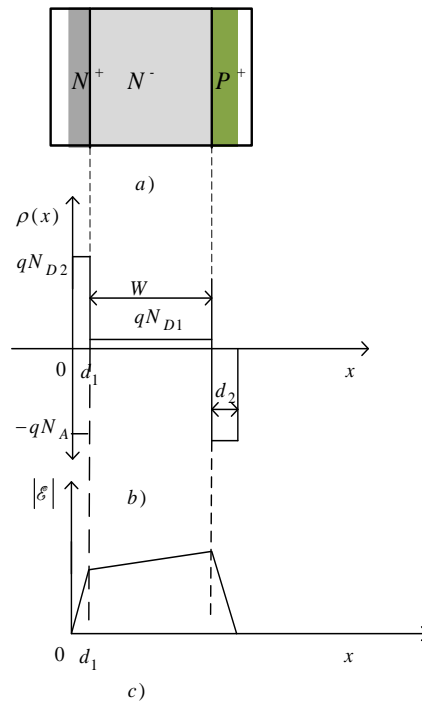
Figure 3.3.   a) A $P^+N^-N^+$ structure highlighting the depleting region under a large reverse applied voltage; b) doping profile of the $P^+N^-N^+$ structure with charge density as a function of position; c) electrical field as a function of position.

Since $\mathscr{E} = -dV/dx$, the electrical potential applied to the structure is obtained by integrating the electrical field from 0 to $d_1 + W + d_2$ resulting in:

$$V_{appl} = \frac{q}{\varepsilon}\left[\frac{N_{D2}^2 + N_{D2}N_A}{2N_A}d_1^2 + \left(\frac{N_{D1}N_{D2}}{N_A} + N_{D2}\right)d_1W + \left(\frac{N_{D1}^2 + N_A N_{D1}}{2N_A}\right)W^2\right] \qquad (3.9)$$

Substituting Equations (3.8) into (3.7) and using the result to calculate the ionization coefficient (1.3), we can reevaluate the ionization integral (1.2) as:

$$N_{D2}^7 d_1^8 + \frac{N_{D2}^8 d_1^8}{N_A} + (\frac{N_{D1}}{N_A} + 1)(8N_{D2}^7 d_1^7 W + 28N_{D1}N_{D2}^6 d_1^6 W^2 + 56N_{D1}^2 N_{D2}^5 d_1^5 W^3 +$$

$$+70N_{D1}^3 N_{D2}^4 d_1^4 W^4 + 56N_{D1}^4 N_{D2}^3 d_1^3 W^5 + 28N_{D1}^5 N_{D2}^2 d_1^2 W^6 + 8N_{D1}^6 N_{D2}d_1 W^7 + N_{D1}^7 W^8) = \frac{8\varepsilon^7}{Kq^7} \qquad (3.10)$$

For a given breakdown voltage, *BV*, the thicknesses of the drift region, *W*, can be calculated numerically using Equations (3.9) and (3.10).

Chapter 4 – Modeling of Power SiC Diodes and Bipolar Junction Transistors

4.1 Introduction

Chapter 4 presents Level 3 physics-based models of SiC diodes and BJTs. The devices are divided into three and four regions, respectively; and the basic equations governing the behavior of the semiconductor devices, such as Poisson's equation, Maxwell's equation, carrier continuity equations, and current transport equations, are used to analyze their operation. The ambipolar diffusion equation (ADE) of a lightly doped drift region is solved using the Fourier series.

4.2 Modeling of the Lightly Doped Drift Region of a Bipolar Power Device

Since SiC diode and BJT models are developed by employing a Fourier-based solution for the ADE of the N^- drift region, the Fourier-series-based modeling approach is presented. The solutions to the carrier densities at the drift region boundary are used to determine the depletion region voltage drops, junction voltages, and the voltage drop in the lightly doped drift region.

4.2.1 Solution of the Ambipolar Diffusion Equation

Figure 4.1 shows the arrangement of the carrier distribution in the carrier storage region (CSR) of bipolar power semiconductor devices. The CSR is sandwiched between two depletion layers. During the on-state, the depletion layers effectively vanish, allowing the CSR to occupy the whole width of the drift region. During the turn-off, the two depletion layers expand from the ends of the drift region as the excess carriers are removed from the CSR. This allows the device to support the applied voltage in the off-state. Depending on the applied voltage, the boundaries of the CSR, x_1 and x_2, have different positions.
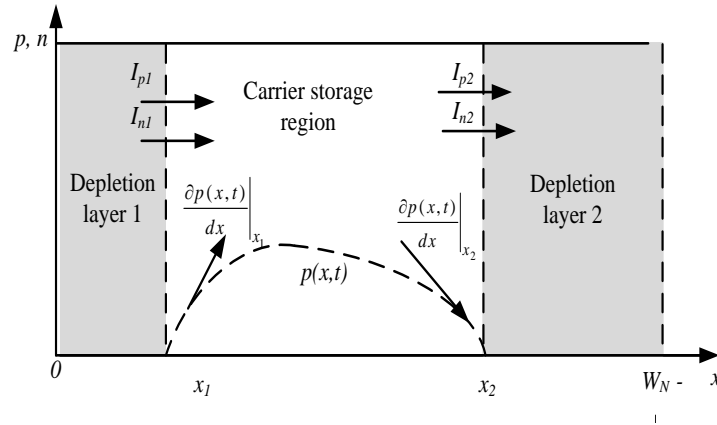
Figure 4.1. The general arrangement of the carrier storage region and depletion layers in the lightly doped N^- - drift region.

Under high-level injection, the density concentrations of holes and electrons in the CSR are equal $(p = n)$; and the charge dynamic in it can be described by the well-known ADE:

$$D\nabla^2 p = \frac{p}{\tau_{HL}} + \frac{\partial p}{\partial t} \tag{4.1}$$

where D is ambipolar diffusivity and τ is high level carrier lifetime.

In the one-dimensional carrier dynamic, this equation can be given as:

$$D\frac{\partial^2 p(x,t)}{\partial x^2} = \frac{p(x,t)}{\tau_{HL}} + \frac{\partial p(x,t)}{\partial t} \tag{4.2}$$

The solution of the ADE, obtained by using appropriate boundary conditions, allows determination of general device behavior. The basic idea of the Fourier-based solution is to separate $p(x,t)$ into its space and time functions. According to Leturcq (125), the excess carrier concentration, $p(x,t)$, can be represented as a discrete cosine Fourier series:

$$p(x,t) = p_0(t) + \sum_{k=1}^{\infty} p_k(t)\cos\left[\frac{k\pi(x-x_1)}{x_2-x_1}\right] \tag{4.3}$$

where the Fourier series coefficients $p_k(t)$ are:

$$p_0(t) = \frac{1}{x_2-x_1}\int_{x_1}^{x_2} p(x,t)dx$$

$$p_k(t) = \frac{2}{x_2-x_1}\int_{x_1}^{x_2} p(x,t)\cos\left(\frac{k\pi(x-x_1)}{x_2-x_1}\right)dx \tag{4.4}$$

By substituting the carrier concentration in Fourier-series form (4.4) into the ADE (4.2), the amplitude of the Fourier-series $p_k(t)$ can be determined in a group of first order differential equations. This requires employing the boundary conditions at the edges of the drift region. The required boundary conditions are the boundaries of the regions (x_1

and x_2), their differentials (dx_1/dt and dx_2/dt), and the carrier density gradients at x_1 and x_2 given by the equations:

$$\left.\frac{\partial p}{\partial x}\right|_{x_1} = \frac{1}{2qA}\left(\frac{I_n}{D_n} - \frac{I_p}{D_p}\right)\Bigg|_{x_1} \qquad \left.\frac{\partial p}{\partial x}\right|_{x_2} = \frac{1}{2Aq}\left(\frac{I_n}{D_n} - \frac{I_p}{D_p}\right)\Bigg|_{x_2}$$

and , (4.5)

where D_n and D_p are electron and hole diffusivities, I_n and I_p are electron and hole currents, and A is the active device area.

The solution to the ADE is given by the following differential equations as each of them refers to a harmonic, p_k, of the carrier charge density, $p(x)$:

for $k > 0$

$$\frac{2D}{x_2 - x_1}\left[\left.\frac{\partial p(x,t)}{\partial x}\right|_{x_2}(-1)^k - \left.\frac{\partial p(x,t)}{\partial x}\right|_{x_1}\right] = \frac{dp_k(t)}{dt} + \left[\frac{1}{\tau} + \frac{Dk^2\pi^2}{(x_2 - x_1)^2}\right]p_k(t)$$

$$+ \frac{2}{x_2 - x_1}\left(\sum_{\substack{n=1 \\ n \neq k}}^{\infty} \frac{n^2}{n^2 - k^2}\left[\frac{dx_1}{dt} - (-1)^{n+k}\frac{dx_2}{dt}\right]p_n(t) + \frac{p_k}{4}\left(\frac{dx_1}{dt} - \frac{dx_2}{dt}\right)\right)$$

for $k = 0$

$$\frac{D}{x_2 - x_1}\left[\left.\frac{\partial p(x,t)}{\partial x}\right|_{x_2} - \left.\frac{\partial p(x,t)}{\partial x}\right|_{x_1}\right] = \frac{dp_0(t)}{dt} + \frac{p_0(t)}{\tau}$$

$$+ \frac{1}{x_2 - x_1}\sum_{n=1}^{\infty}\left[\frac{dx_1}{dt} - (-1)^n\frac{dx_2}{dt}\right]p_n(t)$$

(4.6)

At the boundary, x_1 and x_2, the carrier densities, p_{x1} and p_{x2}, are calculated using Equation (4.7), respectively:

$$p_{x1} = \sum_{k=1}^{n} (-1)^k p_k$$

$$p_{x2} = \sum_{k=1}^{n} p_k$$

(4.7)

4.2.2 Depletion Layer Parameters

The depletion layer voltages, V_{d1} and V_{d2}, across the N^-P and N^-N^+ depletion layers, respectively, are derived using feedback from the boundary carrier densities, p_{x1} and p_{x2}:

$$V_{d1} = \begin{cases} 0 & \text{if } p_{x1} > 0, \\ -K_{FV}\, p_{x1} & \text{otherwise.} \end{cases}$$

$$V_{d2} = \begin{cases} 0 & \text{if } p_{x2} > 0, \\ -K_{FV}\, p_{x2} & \text{otherwise.} \end{cases}$$

(4.8)

where K_{FV} is a feedback constant (126).

The associated depletion widths, W_{d1} and W_{d2}, are calculated using a step doping concentration change on each side of the junction.

$$W_{d1} = \sqrt{\frac{2\varepsilon V_{d1}}{qN_{N^-} + \dfrac{|I_{p1}|}{A v_{sat}}}}$$

$$W_{d2} = \sqrt{\frac{2\varepsilon V_{d2}}{qN_{N^-} + \dfrac{|I_{n2}|}{A v_{sat}}}}$$

(4.9)

where N_{N^-} is the doping concentration in the N^- region, v_{sat} is the saturation velocity, and I_{p1} and I_{n2} are the hole and electron currents at the respective boundaries, x_1 and x_2.

The boundary positions x_1 and x_2 are calculated by:

$$x_1 = W_{d1}$$
$$x_2 = W_{N^-} - W_{d2}$$

(4.10)

The displacement currents, I_{disp1} and I_{disp2}, are due to the change in the depletion widths at junctions J_1 and J_2 and are calculated by:

$$I_{disp1} = C_{J1} \frac{dV_{d1}}{dt} = \varepsilon A \frac{1}{W_{d1}} \frac{dV_{d1}}{dt}$$
$$I_{disp2} = C_{J2} \frac{dV_{d2}}{dt} = \varepsilon A \frac{1}{W_{d2}} \frac{dV_{d2}}{dt}$$

(4.11)

It can be noted that when the depletion layer exists, there is no recombination current; and the displacement current is negligible. Therefore, the collector current, I_C, of a BJT can be used instead of the hole and electron currents, I_{p1} and I_{n2}, for the calculation of the depletion widths, W_{d1} and W_{d2}, in Equation (4.9).

4.2.3 Voltage Drop in Lightly Doped Drift Region

The voltage drop in the lightly doped drift region, V_{N^-}, can be calculated based on electron and hole currents passing through the drift region. The current transport equations are:

$$J_n = q\mu_n n\mathscr{E} + q\mu_n \nabla n$$

(4.12)

$$J_p = q\mu_p n\mathscr{E} - q\mu_p \nabla p$$

(4.13)

Due to conductivity modulation, it can be assumed that:

$$n = p + N_{N^-}$$

(4.14)

Including the doping concentration, N_{N^-} is necessary, especially during the switching when the drift region has low conductivity due to the low-level injection.

Summing the current transport equations and including the Einstein relation $(D_p/\mu_p = kT/q)$ and Equation (4.14), the total current density is:

$$J = qE(p(\mu_n + \mu_p) + \mu_n N_{N^-}) + qV_T(\mu_n - \mu_p)\frac{\partial p}{\partial x} \tag{4.15}$$

The electrical field, $\mathcal{E}$, is:

$$\mathcal{E} = \frac{J}{q(p(\mu_n + \mu_p) + \mu_n N_{N^-})} - \frac{V_T(\mu_n - \mu_p)}{p(\mu_n + \mu_p) + \mu_n N_{N^-}}\frac{\partial p}{\partial x} \tag{4.16}$$

The drift region voltage drop is calculating by integrating the electrical field between the two boundaries, x_1 and x_2.

$$V_{N^-} = \frac{J}{q}\int_{x_1}^{x_2}\frac{dx}{p(\mu_n + \mu_p) + \mu_n N_{N^-}} - \int_{p_{x1}}^{p_{x2}}\frac{V_T(\mu_n - \mu_p)}{p(\mu_n + \mu_p) + \mu_n N_{N^-}}\partial p \tag{4.17}$$

The voltage drop in lightly doped drift region, V_{N^-}, is comprised of two components, a resistive voltage drop due to the resistivity of the lightly doped drift region and voltage due to the diffusion across the drift region. The first integral of the Equation (4.17) cannot be solved analytically from the Fourier series relation, because the carrier densities must be calculated for each point along the CSR and then substituted in (4.17). Instead, the CSR is divided into segments of equal width. It is desirable that the number of segments, M, be equal to the number of the terms in the Fourier series used to calculate the carrier densities. The width of a segment is calculated by the equation:

$$\Delta x = \frac{x_2 - x_1}{M - 1} \tag{4.18}$$

The carrier distribution in every point is calculated by the inverse Fourier transformation. The carrier distribution between two points is assumed to be a linear approximation (Figure 4.2):

$$p_T = p_{T1} + (p_{T2} - p_{T1})\frac{x}{\Delta x} \tag{4.19}$$
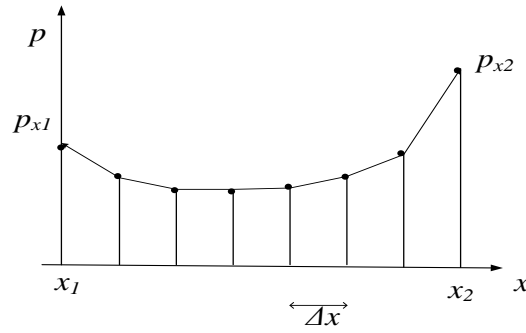
Figure 4.2. The carrier distribution in CSR during the on-state.

The resistive voltage drop for every segment, V_{seg}, is calculated by:

$$V_{seg} = \frac{J}{q(\mu_n + \mu_p)}\int_0^{\Delta x}\frac{dx}{p_T} = \frac{J}{q(\mu_n + \mu_p)}\frac{\Delta x}{p_{T2} - p_{T1}}\ln\left(\frac{p_{T2}}{p_{T1}}\right) \tag{4.20}$$

For $p_{T1} = p_{T2} = p_T$, the Equation (4.20) is not defined. Using l'Hôpital's rule for this case, the voltage drop of the segment is:

$$V_{seg} = \frac{J}{q(\mu_n + \mu_p)}\frac{\Delta x}{p_T} \tag{4.21}$$

These two cases for calculating V_{seg} are generalized in (126) as follows:

$$V_{seg} = \begin{cases} \dfrac{J}{q(\mu_n + \mu_p)} \dfrac{\Delta x}{p_{T2} - p_{T1}} \ln\left(\dfrac{p_{T2}}{p_{T1}}\right) & \text{if } \ |p_{T2} - p_{T1}| \geq 0.00005(p_{T2} - p_{T1}), \\ \dfrac{J}{q(\mu_n + \mu_p)} \dfrac{\Delta x}{p_T} & \text{otherwise.} \end{cases} \tag{4.22}$$

and the voltage drop, V_{N^-}, of the SCR is:

$$V_{N^-} \approx \frac{I}{qA(\mu_n + \mu_p)} \frac{x_2 - x_1}{M - 1} \sum_{\kappa=0}^{M-1} \left[\frac{1}{p_{T(k)} - p_{T(k-1)}} \ln\left(\frac{p_{T(k)}}{p_{T(k-1)}}\right) \right] - V_T \left(\frac{\mu_n - \mu_p}{\mu_n + \mu_p}\right) \ln\left(\frac{p_{x2}}{p_{x1}}\right) \tag{4.23}$$

where I is the current passing through the drift region, A is its cross-section area, M is the number of terms of the Fourier series, and the carrier distribution, $p_{T(k)}$, is calculated by:

$$p_{T(k)} = p\left(x_1 + \frac{k(x_{2\_} x_1)}{M - 1}\right) + \frac{\mu_n N_B}{\mu_n + \mu_p}. \tag{4.24}$$

4.3 Modeling a Power Diode

A Level 3 Model for modeling a power diode using a Fourier-based solution for the ADE of the lightly doped N^- drift region is developed. The $P^+N^-N^+$ diode is divided into three regions, and the basic equations governing the behavior of semiconductor
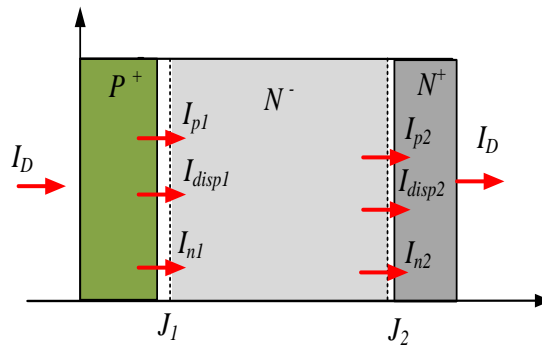
Figure 4.3. Schematic structure of a $P^+N^-N^+$ power diode.

devices are used to analyze the operation of the diode. The diode current, I_D, and the electron, hole, and displacement currents at junctions J_1 and J_2 (I_{n1}, I_{p1}, I_{disp1} and I_{n2}, I_{p2}, I_{disp2}) and their direction are shown in Figure 4.3. The P^+ and N^+ emitters are assumed to be minority sinks.

4.3.1. P^+ Emitter Region

Figure 4.4 shows the P^+ emitter region of a power diode with currents entering and leaving the region and the minority carrier concentration profile. The P^+ emitter region is highly doped; and, therefore, there is a significant electron concentration adjacent to the P^+N^- junction due to the high-level injection during the on-state. As a result of this high concentration, minority carriers flow into the highly doped P^+ emitter region recombining with the holes. The resulting electron current due to the emitter recombination is:

$$I_{n1} = qAh_p p_{x1}^2 \tag{4.26}$$

where, p_{x1} is the hole concentration at the junction, J_1. The recombination parameter, h_p, is calculated using Equation (3.6).

The current continuity at junction J_1 (Figure 4.4) requires that:

$$I_D = I_{n1} + I_{p1} + I_{dis1} \tag{4.27}$$
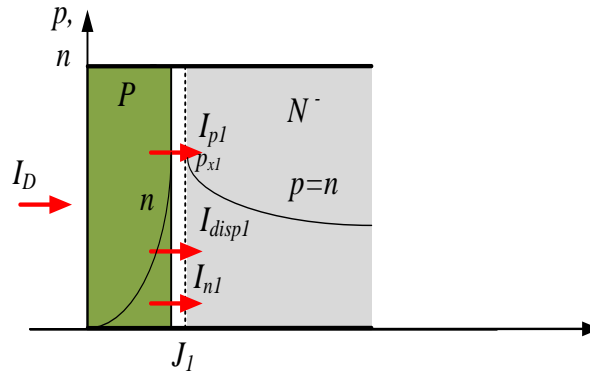
Figure 4.4. Schematic structure of the P^+ emitter region of a power diode during the on-state.

The junction voltage of junction J_1 is (124):

$$V_{j1} = V_T \ln\left(\frac{p_{x1} N_{N^-}}{n_i^2} \right),$$

(4.28)

where V_T is thermal voltage (kT/q).

4.3.2. N^- Drift Region

A high power diode has a thick drift region required to support high blocking voltage.

The simple charge control modeling approach cannot be applied for the drift region, because the transient duration is comparable to or shorter than the transient time of the
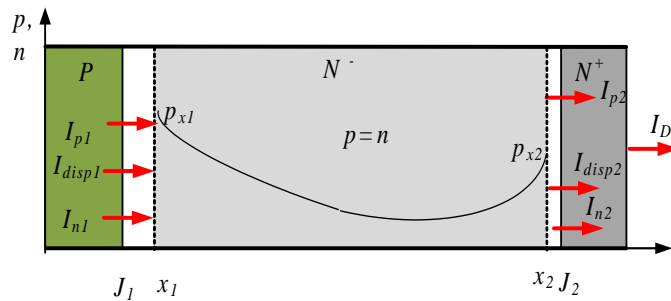
Figure 4.5. Schematic structure and carrier concentrations of lightly doped drift region of a power diode during the on state.

charge carriers. In this case, the charge dynamics in the drift region can be described by the continuity and the transport equations. The charge profile in the thick drift region can be assumed to be one dimensional for more than 90% of its volume, which simplifies the analysis. The minority carrier concentration profile and the currents entering and leaving the N^- drift region of a power diode are shown in Figure 4.5.

High-level injection in a lightly doped drift region during most of the time of the transient and on-static-state can be assumed. Under this assumption and quasi-neutrality, the one-dimensional ADE describing the carrier dynamics in the majority of this region is given by the equation:

$$D_{N^-} \frac{\partial^2 p(x,t)}{\partial x^2} = \frac{p(x,t)}{\tau_{N^-}} + \frac{\partial p(x,t)}{\partial t} \tag{4.29}$$

where D_{N^-} is the ambipolar diffusion coefficient, τ_{N^-} is the high-level carrier lifetime within the drift region, and $p(x,t)$ is the excess carrier concentration.

Using Fourier analysis, described in Section 4.2.1, the solution to the ADE is given by the following differential equations as each of them refers to the harmonic p_k of the carrier charge density, $p(x)$:

for $k > 0$

$$D_{N^-}\left[\frac{\partial p(x,t)}{\partial x}\bigg|_{x2} (-1)^k - \frac{\partial p(x,t)}{\partial x}\bigg|_{x1} \right] = \frac{x_2 - x_1}{2}\left(\frac{dp_k(t)}{dt} + \left[\frac{1}{\tau} + \frac{D_{N^-}k^2\pi^2}{(x_2-x_1)^2} \right] p_k(t) \right) +$$

$$+ \left(\sum_{\substack{n=1 \\ n \neq k}}^{\infty} \frac{n^2}{n^2 - k^2}\left[\frac{dx_1}{dt} - (-1)^{n+k}\frac{dx_2}{dt} \right] p_n(t) + \frac{p_k}{4}\left(\frac{dx_1}{dt} - \frac{dx_2}{dt} \right) \right)$$

for $k = 0$

$$D_{N^-} \left[\frac{\partial p(x,t)}{\partial x} \bigg|_{x_2} - \frac{\partial p(x,t)}{\partial x} \bigg|_{x_1} \right] = (x_2 - x_1) \left(\frac{dp_0(t)}{dt} + \frac{p_0(t)}{\tau} \right) +$$

$$+ \sum_{n=1}^{\infty} \left[\frac{dx_1}{dt} - (-1)^n \frac{dx_2}{dt} \right] p_n(t) \qquad (4.30)$$

The required boundary conditions for solving carrier densities, p_{x1} and p_{x2}, are the boundaries of the region (x_1 and x_2), their differentials (dx_1/dt and dx_2/dt), and also the carrier density gradients at x_1 and x_2 given by the equations:

$$\frac{\partial p}{\partial x} \bigg|_{x_1} = \frac{1}{2q} \left(\frac{J_n}{D_n} - \frac{J_p}{D_p} \right) \bigg|_{x_1} \quad \text{and} \quad \frac{\partial p}{\partial x} \bigg|_{x_2} = \frac{1}{2q} \left(\frac{J_n}{D_n} - \frac{J_p}{D_p} \right) \bigg|_{x_2} \qquad (4.31)$$

where D_n and D_p are electron and hole diffusivities in the lightly doped drift region.

The current continuity equation at junction J_2 is:

$$I_{n2} = I_D - I_{p2} - I_{disp2} \qquad (4.32)$$

Assuming that:

$$\frac{1}{D_n} + \frac{1}{D_p} = \frac{D_n + D_p}{D_n D_p} = \frac{2}{D_{N^-}} \quad \text{and} \quad D \left(\frac{1}{D_n} - \frac{1}{D_p} \right) = \frac{D_n - D_p}{D_n + D_p} = D_{diff} , \qquad (4.33)$$

and using the current continuity equations at junctions J_1, Equation (4.27), and J_2, Equation (4.32), and the left side of Equation (4.30), for even and odd numbers of k can be calculated by the following equations:

$$I_{even} = D \left(\frac{\partial p}{\partial x} \bigg|_{x_2} - \frac{\partial p}{\partial x} \bigg|_{x_1} \right) = \frac{1}{2qA} \begin{vmatrix} I_D \\ I_{p2} \\ I_{n1} \\ I_{disp1} \\ I_{disp2} \end{vmatrix} \begin{vmatrix} 2 & -2 & -2 & -\dfrac{D}{D_p} & -\dfrac{D}{D_n} \end{vmatrix}$$

$$I_{odd} = D\left(\frac{\partial p}{\partial x}\bigg|_{x_2} - \frac{\partial p}{\partial x}\bigg|_{x_1}\right) = \frac{1}{2qA}\begin{vmatrix}I_D\\I_{p2}\\I_{n1}\\I_{disp1}\\I_{disp2}\end{vmatrix}\begin{vmatrix}-2D_{diff} & 2 & 2 & -\dfrac{D}{D_p} & \dfrac{D}{D_n}\end{vmatrix} \qquad (4.34)$$

The boundary carrier densities, p_{x1} and p_{x2}, at the boundaries, x_1 and x_2, are calculated using equations:

$$p_{x_1} = \sum_{k=1}^{n} p_k$$

$$p_{x_2} = \sum_{k=1}^{n} (-1)^k p_k \qquad (4.35)$$

The depletion layer voltages, V_{d1} and V_{d2}, across the P^+N^- and N^-N depletion layers are derived using a feedback from the boundary carrier densities, p_{x1} and p_{x2}:

$$V_{d1} = \begin{cases} 0 & \text{if } p_{x1} > 0, \\ -K_{FV}\,p_{x1} & \text{otherwise.} \end{cases}$$

$$V_{d2} = \begin{cases} 0 & \text{if } p_{x2} > 0, \\ -K_{FV}\,p_{x2} & \text{otherwise.} \end{cases} \qquad (4.36)$$

The feedback constant, K_{FV}, is set to 10^{-12}, which gives good convergence and minimal error. The same value of K_{FV} is used to calculate the depletion layer voltages of a diode and an IGBT in (126).

The depletion widths, W_{d1} and W_{d2}, are:

$$W_{d1} = \sqrt{\dfrac{2\varepsilon V_{d1}}{qN_{N^-} + \dfrac{|I_{p1}|}{Av_{sat}}}}$$

$$W_{d2} = \sqrt{\dfrac{2\varepsilon V_{d2}}{qN_{N^-} + \dfrac{|I_{n2}|}{Av_{sat}}}}$$

(4.37)

The boundary positions, x_1 and x_2, are:

$$x_1 = W_{d1}$$
$$x_2 = W_{N^-} - W_{d2}$$

(4.38)

The displacement currents, I_{disp1} and I_{disp2}, at junctions J_1 and J_2 are:

$$I_{disp1} = C_{J1}\dfrac{dV_{d1}}{dt} = \varepsilon A\dfrac{1}{W_{d1}}\dfrac{dV_{d1}}{dt}$$

$$I_{disp2} = C_{J2}\dfrac{dV_{d2}}{dt} = \varepsilon A\dfrac{1}{W_{d2}}\dfrac{dV_{d2}}{dt}$$

(4.39)

During the on-state, the drift region of a power diode has significantly higher voltage drop compared to the other regions as it has the lowest doping and the longest length. The voltage drop in the N^- drift region, V_{N^-}, is calculated based on the carrier concentration in this region.

$$V_{N^-} \approx \dfrac{I_D}{qA(\mu_n + \mu_p)}\dfrac{x_2 - x_1}{M-1}\sum_{\kappa=0}^{M-1}\left[\dfrac{1}{p_{T(k)} - p_{T(k-1)}}\ln\left(\dfrac{p_{T(k)}}{p_{T(k-1)}}\right)\right] - V_T\left(\dfrac{\mu_n - \mu_p}{\mu_n + \mu_p}\right)\ln\left(\dfrac{p_{x2}}{p_{x1}}\right)$$

(4.40)

where:

$$p_{T(k)} = p\left(x_1 + \dfrac{k(x_{2\_}x_1)}{M-1}\right) + \dfrac{\mu_n N_{N^-}}{\mu_n + \mu_p}.$$

(4.41)

4.3.3. N^+ Emitter Region

The N^+ emitter region, shown in Figure 4.6, has a high doping concentration; and, therefore, there is a significant hole concentration adjacent to the $N^- N^+$ junction. Due to the high-level injection during the on state, electrons from the N^+ region are injected into the lightly doped drift region; and high concentration holes flow into the highly doped N^+ emitter region. The holes recombine with the electrons, and the resulting hole current due to the emitter recombination is:

$$I_{p2} = qAh_n p_{x2}^2 \tag{4.42}$$

The recombination parameter, h_n, calculated by (3.5), depends on emitter properties such as doping level, electron diffusivity, and electron lifetime.

The junction voltage, V_{J2}, is calculated by (124):

$$V_{j2} = V_T \ln\left(\frac{p_{x2}}{N_{N^-}}\right) \tag{4.43}$$
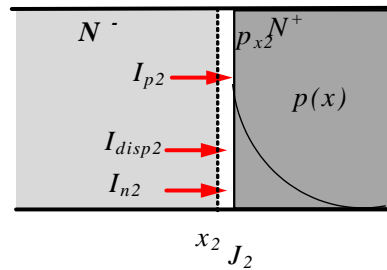
Figure 4.6. Schematic structure of the N^+ emitter region of a power diode during the on state.

4.3.4. Voltage Drop

The voltage drop, V_{AK}, across the power diode is comprised of five components including the voltages across the junctions, J_1 and J_2, the voltage across the two depletion regions, V_{d1} and V_{d2}, and the voltage across the drift region, V_{N^-}.

$$V_{AK} = V_{j1} + V_{j2} - V_{d1} - V_{d2} + V_{N^-} \tag{4.44}$$

4.4 Modeling a Power BJT

The basic one-dimensional structure of a power BJT is illustrated in Figure 4.7. The BJT is divided into four regions: N^+ emitter, P-base, N^- drift, and N^+ collector. The external (emitter base and collector currents, I_E, I_B, and I_C) and internal electron and hole and displacement currents (at junctions J_0: I_{n0}, I_{p0}; J_1: I_{n1}, I_p, and I_{disp1}; and J_2: I_{n2},
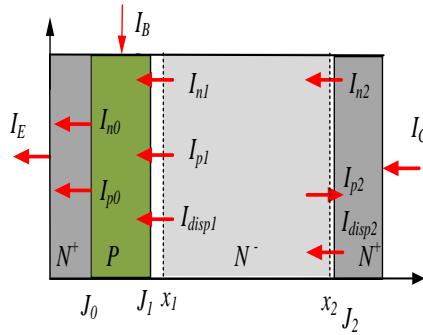
Figure 4.7. One-dimensional cross-section used for modeling the power BJT showing the hole and electron currents in each region.

I_{p2}, and I_{disp2}) are indicated for each region.

4.4.1. N^+ Emitter Region

The N^+ emitter layer of a power BJT can be simply characterized as a hole sink. The hole current at the junction, J_0, is obtained by the equation:

$$I_{p0} = qAh_n n_{B0} P_B \tag{4.45}$$

where n_{B0} is the electron concentration at junction J_0, and P_B is the base doping concentration. The N^+ emitter recombination parameter, h_n, depends on emitter properties, such as doping level (N_E), hole diffusivity (D_p), and hole minority lifetime (τ_p) and can be calculated by Equation (3.5).

The electron current component at junction J_0 is determined by:

$$I_{n0} = I_C - I_{p0} \tag{4.46}$$

The voltage drop across junction J_0 is:

$$V_{j0} = V_T \ln\left(\frac{n_{B0}(n_{B0} + P_B)}{n_i^2} \right) \tag{4.47}$$

4.4.2. *P* - Base Region

The *P*- base region is used to find the boundary current at junction J_1. The lumped charge method is used to model the charge behavior in the base region due to its moderate doping level and comparatively narrow base width. The injected carrier distribution in the base region during conduction is shown in Figure 4.8.
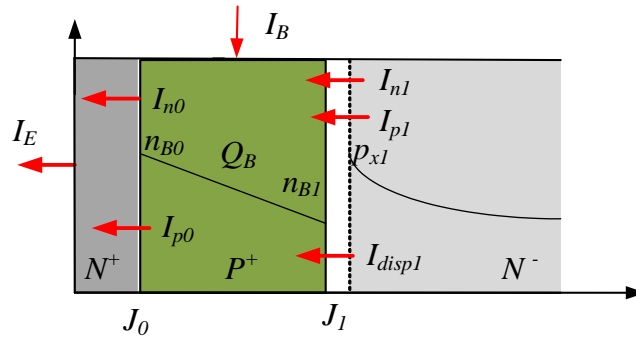
Figure 4.8. Charge distribution and boundary current components in *P* base.

Using the continuity equation for the base region, the injected minority carrier charge is described by the relation:

$$\frac{dQ_B}{dt} + \frac{Q_B}{\tau_{BHL}} = I_{n0} - I_{n1} = I_B + I_{p1} + I_{disp1} - I_{p0}, \tag{4.48}$$

where, τ_{BHL} is the high-level lifetime in the *P*- base region.

The total electron charge in the base is expressed as:

$$Q_B = \frac{n_{B0} + n_{B1}}{2} qAW_B \tag{4.49}$$

where W_B is the base width. The electron concentration at the base region boundary on the collector side, n_{B1}, is related to the excess carrier concentration, p_{x1}, by the doping concentration of the base, P_B, by the equation:

$$n_{B1} = \frac{p_{x1}^2}{P_B} \tag{4.50}$$

Since the diffusion length in the base region is much greater than the base width, the gradient of the electron concentration is approximately linear, giving the electron current at the base-collector junction, J_1, as:

$$I_{n1} = qD_n A \frac{n_{B0} - n_{B1}}{W_B} \tag{4.51}$$

The base-emitter voltage V_{BE} is calculated by the equation:

$$V_{BE} = V_T \ln\left(\frac{n_{B0} P_B}{n_i^2} + 1 \right) \tag{4.52}$$

4.4.3. N^- Drift (Collector) Region

The voltage drop in this region is calculated during the on state. The injected excess carrier concentration is determined by the ADE. As for all power switches, high-level injection and quasi-neutral conditions exist. Under high-level injection conditions, the ADE for the lightly doped drift describes the carrier dynamics of the majority carriers:

$$D\frac{\partial^2 p(x,t)}{\partial x^2} = \frac{p(x,t)}{\tau} + \frac{\partial p(x,t)}{\partial t} \tag{4.53}$$

where D is the ambipolar diffusion coefficient, τ is the high-level carrier lifetime within the drift region, and $p(x, t)$ is the excess carrier concentration.

The Fourier series solution for the ADE is given by the following first order differential equations as each of them refers to a harmonic, $p_k(t)$, of the total minority carrier density, $p(x,t)$:

for $k > 0$

$$D\left[\frac{\partial p(x,t)}{\partial x}\bigg|_{x_2} (-1)^k - \frac{\partial p(x,t)}{\partial x}\bigg|_{x_1} \right] = \frac{x_2 - x_1}{2}\left(\frac{dp_k(t)}{dt} + \left[\frac{1}{\tau} + \frac{Dk^2\pi^2}{(x_2 - x_1)^2} \right] p_k(t) \right)$$

$$+ \left(\sum_{\substack{n=1 \\ n \neq k}}^{\infty} \frac{n^2}{n^2 - k^2}\left[\frac{dx_1}{dt} - (-1)^{n+k} \frac{dx_2}{dt} \right] p_n(t) + \frac{p_k}{4}\left(\frac{dx_1}{dt} - \frac{dx_2}{dt} \right) \right)$$

for $k = 0$ $\qquad\qquad$ (4.54)

$$D\left[\left.\frac{\partial p(x,t)}{\partial x}\right|_{x_2} - \left.\frac{\partial p(x,t)}{\partial x}\right|_{x_1}\right] = (x_2 - x_1)\frac{dp_0(t)}{dt} + \frac{p_0(t)}{\tau} + \sum_{n=1}^{\infty}\left[\frac{dx_1}{dt} - (-1)^n\frac{dx_2}{dt}\right]p_n(t)$$

The solution to the ADE is determined by using the boundary conditions at the edges of the charge storage region. The representation requires the width of the undepleted region and the hole and electron currents at the boundaries of the drift region, which give the gradients of the carrier concentrations at x_1 and x_2, respectively. For the given direction of the currents (Figure 4.9), the required boundary conditions are given by the equations :

$$\left.\frac{\partial p}{\partial x}\right|_{x_1} = \frac{1}{2q}\left(\frac{J_n}{D_n} + \frac{J_p}{D_p}\right)\Bigg|_{x_1} \quad \text{and} \quad \left.\frac{\partial p}{\partial x}\right|_{x_2} = \frac{1}{2q}\left(\frac{J_n}{D_n} + \frac{J_p}{D_p}\right)\Bigg|_{x_2} \qquad (4.55)$$
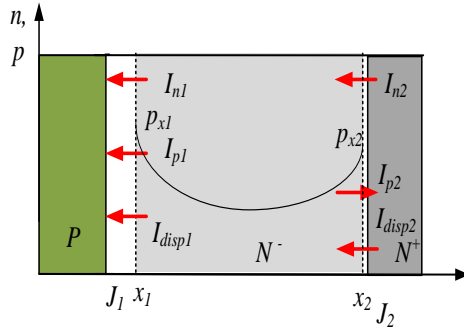

Figure 4.9. Charge distribution and boundary current components in N^-- collector.

Using Equations (4.55), the left side of Equations (4.54), for even and odd numbers of k, can be calculated by the following equations:

$$I_{even} = D\left(\left.\frac{\partial p}{\partial x}\right|_{x_2} - \left.\frac{\partial p}{\partial x}\right|_{x_1}\right) = \frac{1}{2qA}\begin{vmatrix} I_{n1} \\ I_{p1} \\ I_{n2} \\ I_{p2} \end{vmatrix}\begin{vmatrix} -\dfrac{D}{D_n} & -\dfrac{D}{D_p} & +\dfrac{D}{D_n} & +\dfrac{D}{D_p} \end{vmatrix}$$

$$I_{odd} = D\left(\left.\frac{\partial p}{\partial x}\right|_{x_2} - \left.\frac{\partial p}{\partial x}\right|_{x_1}\right) = -\frac{1}{2qA}\begin{vmatrix} I_{n1} \\ I_{p1} \\ I_{n2} \\ I_{p2} \end{vmatrix}\begin{vmatrix} \dfrac{D}{D_n} & \dfrac{D}{D_p} & \dfrac{D}{D_n} & \dfrac{D}{D_p} \end{vmatrix} \qquad (4.56)$$

The boundary carrier densities, p_{x1} and p_{x2}, at the boundaries, x_1 and x_2, are calculated using the equations:

$$p_{x_1} = \sum_{k=1}^{n} p_k \ \text{ and } \ p_{x_2} = \sum_{k=1}^{n}(-1)^k p_k \qquad (4.57)$$

The voltages across the N^-N^+ and N^-P^+ depletion layers, V_{d1} and V_{d2}, are calculated by the following equations:

$$V_{d1} = \begin{cases} 0 & \text{if } p_{x1} > 0, \\ -K_{FV}\,p_{x1} & \text{otherwise.} \end{cases}$$

$$V_{d2} = \begin{cases} 0 & \text{if } p_{x1} > 0, \\ -K_{FV}\,p_{x2} & \text{otherwise.} \end{cases} \qquad (4.58)$$

The feedback constant, K_{FV}, is set to 10^{-12}, which gives good convergence and minimal error (126). The associated depletion widths, W_{d1} and W_{d2}, are calculated using a step doping concentration change on each side of the junction:

$$W_{d1} = \sqrt{\frac{2\varepsilon V_{d1}}{qN_{N^-} + \frac{|I_c|}{Av_{sat}}}}$$

$$W_{d2} = \sqrt{\frac{2\varepsilon V_{d2}}{qN_{N^-} + \frac{|I_c|}{Av_{sat}}}}$$

(4.59)

The boundary positions, x_1 and x_2, are calculated by:

$$x_1 = W_{d1}$$
$$x_2 = W_{N^-} - W_{d2}$$

(4.60)

The displacement currents, I_{disp1} and I_{disp2}, are due to the changing depletion widths at junctions J_1 and J_2,

$$I_{disp1} = C_{J1}\frac{dV_{d1}}{dt} = \varepsilon A \frac{1}{W_{d1}}\frac{dV_{d1}}{dt}$$

$$I_{disp2} = C_{J2}\frac{dV_{d2}}{dt} = \varepsilon A \frac{1}{W_{d2}}\frac{dV_{d2}}{dt}$$

(4.61)

The voltages at junctions J_1 and J_2 are:

$$V_{j1} = 2V_T \ln\left(\frac{p_1}{n_i}\right)$$

$$V_{j2} = V_T \ln\left(\frac{p_{x2}}{N_C}\right)$$

(4.62)

The voltage drop in the carrier storage region, V_{N^-}, is calculated based on the injected carrier concentration discussed in Section 4.2.3.

$$V_{N^-} \approx \frac{I_C}{qA(\mu_n + \mu_p)}\frac{x_2 - x_1}{M-1}\sum_{\kappa=0}^{M-1}\left[\frac{1}{p_{T(k)} - p_{T(k-1)}}\ln\left(\frac{p_{T(k)}}{p_{T(k-1)}}\right)\right] + V_T\left(\frac{\mu_n - \mu_p}{\mu_n + \mu_p}\right)\ln\left(\frac{p_{x2}}{p_{x1}}\right)$$ (4.63)

where the carrier distribution, $p_{T(k)}$, is calculated as:

$$p_{T(k)} = p\left(x_1 + \frac{k(x_2 - x_1)}{M - 1}\right) + \frac{\mu_n N_{N^-}}{\mu_n + \mu_p} \qquad (4.64)$$

4.4.4. N^+ Collector Region

The N^+ collector region has similar properties to the N^+ emitter region as it also can be presented as a hole sink. The hole current at junction J_2 is obtained by the equation:

$$I_{p2} = qA h_n p_{x2}^2 \qquad (4.65)$$

The electron current at the junction, J_2, is:

$$I_{n2} = I_c + I_{p2} - I_{disp2} \qquad (4.66)$$

4.4.5. Voltage Drop

The voltage drop, $V_{CE,}$ across the high power SiC BJT is comprised of six components, including voltages across the junctions, J_0, J_1, and pseudo-junction, J_2, the voltage across the two depletion regions, V_{d1} and V_{d2}, and the voltage across the carrier storage region, V_{N^-}.

$$V_{CE} = V_{j0} + V_{j1} + V_{J2} - V_{d1} - V_{d2} + V_{N^-} \qquad (4.67)$$

Chapter 5 – Simulation Results for the Power

SiC Diode and Bipolar Junction

Transistor

5.1 Introduction

In Chapter 5, calculations are presented for the minimum width of a lightly doped drift region (W_{min}) and breaking voltage (V_{BD}) for $P^+N^-N^+$ and P^+N high voltage diodes as a function of doping concentration of a lightly doped drift region (N_{D1}). Also, the power diode model in Simulink; simulation results for Si, SiC, and CaN high-power diodes; and a comparison of the results are given. Next, a power SiC BJT model in Simulink and simulation results of the switching losses of a SiC BJT are presented. Measurement and simulation results of a SiC BJT are compared, and the power BJT model is validated.

5.2 Calculation of W_{min} and V_{BD} for $P^+N^-N^+$ and P^+N

Structures

The average ionization parameters (A, b, and m) and the constant K for Si and GaN, as given in (78) are presented in Table 5.1 Average ionization coefficients. For 4H-SiC, the data for the electron and hole ionization parameters are taken from (127), averaged

together, and included in the table. The coefficient K is calculated using Equation (1.4). It can be noted that the calculated value of K for 4H-SiC (4.58E-42) is similar to the value given in (63) as 3.9E-42.

Table 5.1 Average ionization coefficients.

Materials	A (cm^{-1})	b (V/cm)	m	K (cm^6/V^7)
Si	1.07E+06 [78]	1.65E+06 [78]	1 [78]	1.9E-35 [78]
4H-SiC	3.15E+06 [125]	1.04E+07 [125]	1.23 [125]	3.9E-42 [63]
GaN	8.85E+06 [78]	2.60E+07 [78]	1 [78]	9.1E-43 [78]

Figure 5.1 presents the results calculated for the required minimum width of the lightly doped drift region (W_{min}) as a function of base doping concentration (N_{D1}) for a $P^+N^-N^+$ structure, for various designed breakdown voltages applied to the device and different semiconductor materials (Si, 4H-SiC and GaN). This design requires the depletion region to punch-through to the N^+ region, otherwise the device acts like a P^+N^- diode.

Equation (1.7), associated with a planar P^+N junction is also plotted in Figure 5.1 for comparison. It can be concluded from the simulation results that there are significant differences in the calculated values of the base width for the two structures (P^+N or $P^+N^-N^+$) for the same doping concentration, and for a given designed breakdown (blocking) voltage for all three semiconductor materials. Note that for theoretical base doping values below 3×10^{13} cm^{-3} for Si, 2.5×10^{15} cm^{-3} for 4H-SiC, and 5×10^{15} cm^{-3} for

GaN, there is little effect on the required minimum base width for a given breakdown voltage.
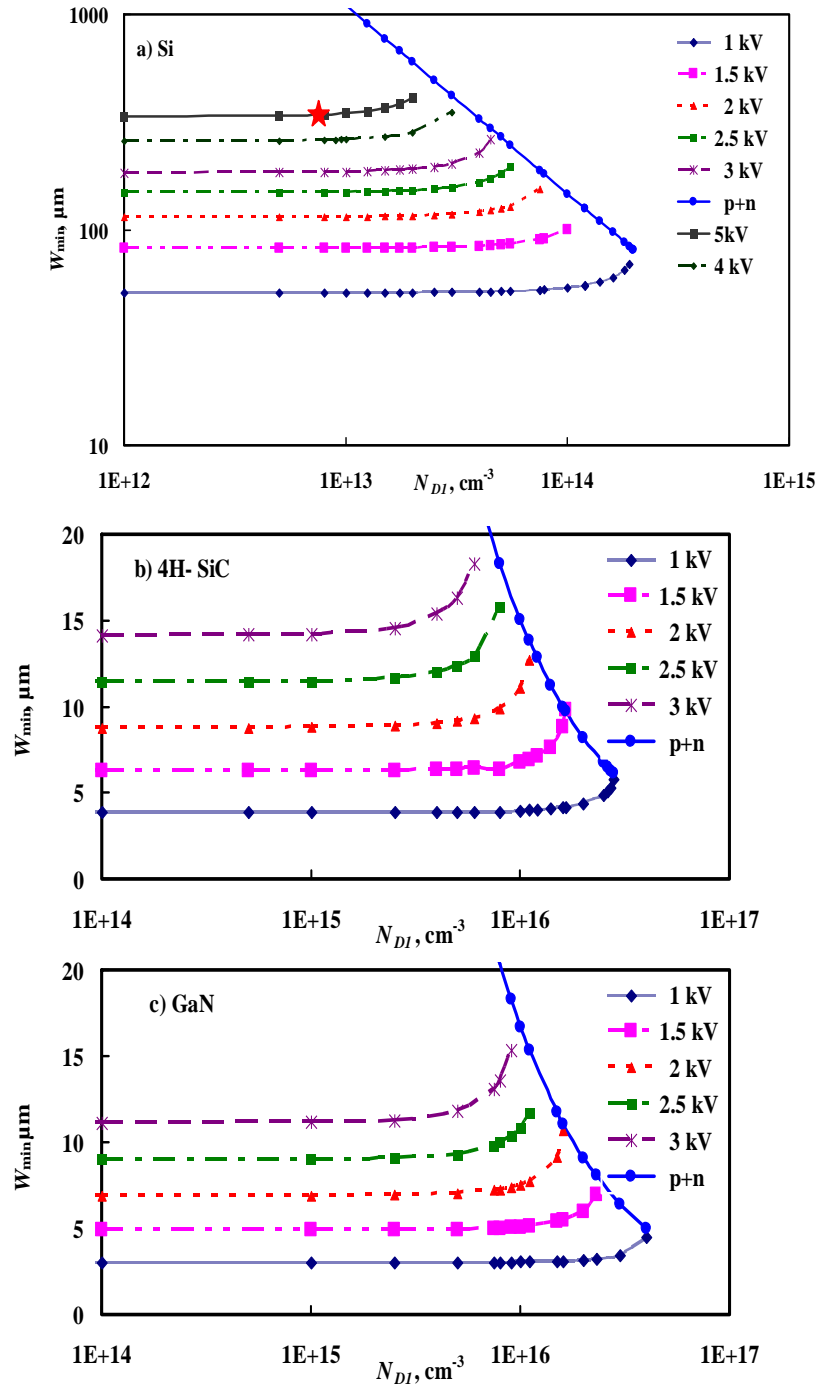
Figure 5.1 The minimum width of the lightly doped drift region (W_{min}) as a function of doping concentration (N_{D1}) for a P^+N diode and a $P^+N^-N^+$ structure for different applied voltages and different semiconductor materials a) Si, b) 4H-SiC and c) GaN.

Increasing the base doping concentration in each of the three semiconductor materials above these values significantly increases the required base width for a given designed breakdown and results in a decreasing value of d_1 (depletion width in the N^+ region) to the point that it disappears, where the structure reverts to the standard P^+N device. This phenomenon for a 3 kV designed breakdown is observed for Si at a doping concentration of approximately 4.5×10^{13} cm^{-3}, for 4H-SiC at approximately 6×10^{15} cm^{-3}, and for GaN at approximately 9×10^{15} cm^{-3}.

Lower breakdown voltage values allow for an increased doping concentration before the limiting effect is obtained. For the same blocking voltage, the highest doping concentration allowed in the drift region is for a GaN $P^+N^-N^+$ structure. This is expected since GaN has the largest bandgap energy of the three semiconductors. A 4H-SiC device has slightly a lower doping concentration than GaN, while a Si device has a significantly lower doping concentration requirement, approximately 100 times smaller compared to GaN and 4H-SiC $P^+N^-N^+$ devices at a given breakdown voltage.

Figure 5.2 presents the results calculated (family of curves using different N^- base widths at breakdown) for the breakdown voltage as a function of doping concentration (N_{D1}) for a $P^+N^-N^+$ structure, again using Equations (3.9) and (3.10), and the P^+N structure using Equation (1.8) for Si, 4H-SiC, and GaN semiconductors. It can be seen from Figure 5.2 that as technology improves to allow for lower base doping values, the estimation of a breakdown voltage rating from the analysis of the P^+N structure is inadequate. As shown, doping concentrations less than 5×10^{13} for Si, 2×10^{15} for 4H-SiC, and 5×10^{15} for GaN for the same drift region width do not significantly affect the breakdown voltage.

Loh et al. (127) have calculated the breakdown voltage for an ideal $P^+N^-N^+$ 4H-SiC diode for different thicknesses of the lightly doped drift region as a function of its doping concentration. They have used their local model, including impact ionization parameters. Their results show a trend similar to our analysis wherein the breakdown voltage is relatively independent of N_{DI} values for ultra-low doping concentrations in the base region. This indicates an independent validation of our approach. However, our work is expanded to include the behavior and optimization for GaN and extends the level of detail and correctness for Si beyond what has been previously reported. From Loh et al. (127) and our results, for a 4H-SiC device with a 10 μm N-base region width, the doping concentration that separates the region of "constant" breakdown voltage from the region where the concentration strongly affects the breakdown voltage is approximately 10^{16} cm^{-3}.
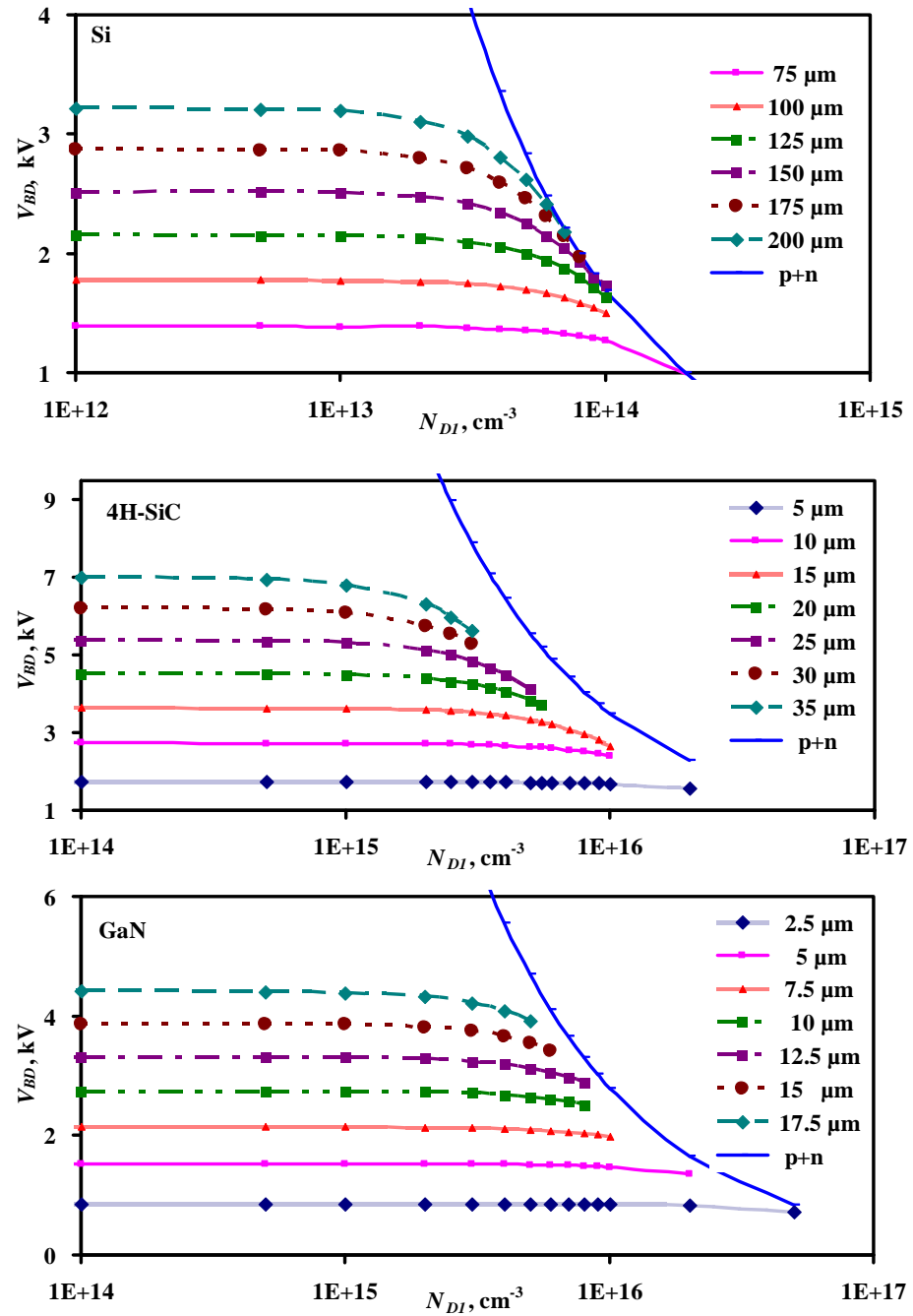
Figure 5.2. The breakdown voltage as a function of doping concentration (N_{DI}) for a P^+N diode and a $P^+N^-N^+$ structure for different N^- base widths and different semiconductor materials: a)Si, b)4H-SiC and c)GaN.

From the results calculated and presented in Figure 5.1 and Figure 5.2, it can be concluded that the estimation of the minimum lightly doped drift region thicknesses required in a $P^+N^-N^+$ structure using Equation (1.7) is not suitable. For example, if a 2 kV Si device is designed with a drift region doping concentration of 4.5×10^{13} cm^{-3}, using the P^+N structure Equation (1.7), the thickness is 296 µm, while the base thickness is only 123 µm when using the $P^+N^-N^+$ structure. For a 2 kV 4H-SiC device with a drift region doping concentration of 6×10^{15} cm^{-3}, the base thickness is 23.6 µm when using Equation (1.7) and only 9.4 µm when using the $P^+N^-N^+$ structure analysis. Similarly, for a 2 kV GaN device with a drift region doping concentration of 9×10^{15} cm^{-3}, the thickness is 18.33 µm when using Equation (1.7) and only 7.4 µm when using the $P^+N^-N^+$ structure.

5.3 Realization of Power Diode Model in Simulink®

An IGBT under an inductive load switching condition is simulated in Matlab® and Simulink®. The circuit schematic is shown in Figure 5.3. A freewheeling $P^+N^-N^+$ diode is employed in the simulation. The $P^+N^-N^+$ diode model described in Section (4.3) is used for the simulation of Si, SiC, and GaN diodes for different design voltages. The Matlab program is used to input the basic parameters used by the Simulink program. The Simulink model input parameters are: the device geometry parameters; the doping concentrations in each region (assumed to be uniform), charge carrier diffusion coefficients, and minority carrier lifetimes of the different regions. Material parameters of Si, SiC, and GaN, such as hole and electron mobilities, dielectric permittivity, carrier saturation velocity, the intrinsic carrier concentration (at 300 K), and the average ionization coefficients are also needed. The simulation parameters are presented in Table

5.3. The thickness of the lightly doped drift region is calculated using Equations (3.9) and (3.10).
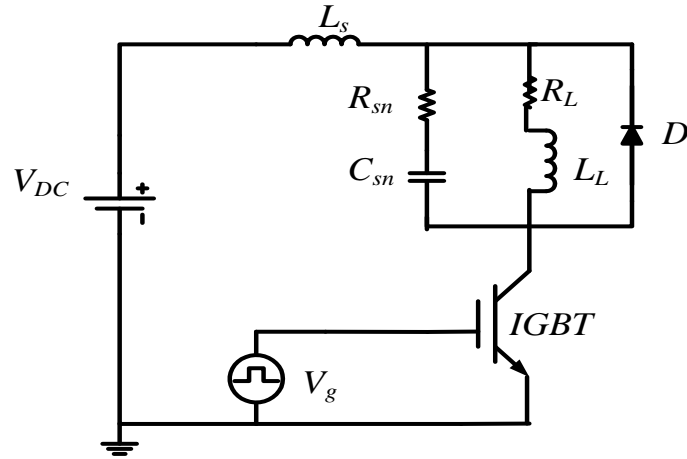
Figure 5.3. IGBT under an inductive load switching with free-wheeling diode, *D*.

Table 5.2 Simulation parameters.

Parameters	Si	SiC	GaN
N_{D2} and N_A, (cm^{-3})	10^{19} and 10^{18}	10^{19} and 10^{18}	10^{19} and 10^{18}
n_i, (cm^{-3})	1.48×10^{10}	6.84×10^{-11}	1.82×10^{-11}
τ, (µs)	0.44	0.15	0.15
h_p and h_n, (cm^{4}s^{-1})	10^{-14} and 10^{-14}	10^{-14} and 1.3×10^{-14}	10^{-14} and 1.3×10^{-14}
μ_n and μ_p, (cm^{2}V^{-1}s^{-1})	1400, 450	900, 100	1000, 200
ε, (F cm^{-1})	11.8	10	8.9
v_{sat}, (cm/s)	10^7	2.7×10^7	2.2×10^7

Table 5.3 Circuit parameters for simulations

Parameters	Units	Value
V_{dc}	V	450
L_S	nH	330
R_L/L_L	Ω/mH	0.6/22
R_{sn}/C_{sn}	Ω/nF	3.4/9.7

The implementation of the behaviour of the IGBT with a free freewheeling diode in Simulink requires use of a stiff solver due to the widely different time constants present in the model. Suitable solvers for simulation of power semiconductor devices are ode15s and ode23tb (128). The configuration parameters chosen for simulation of the model are: solver ode 15s (stiff/NDF); the maximum and minimum step sizes are, respectively, 10^{-5} and 10^{-27} s. The initial step size is set to "auto" and solver reset method to "fast." The relative and absolute tolerances are set to be 10^{-2} and 10^{-5}, respectively, step preservation is set to "use local settings," maximum order is set to 2, and the number of consecutive minimum steps is 1. Zero crossing options are: zero-crossing control is set to "Disable all," time tolerance is $10\times128\times$eps, where eps $= 2^{\wedge}$(E-52). Algorithm is set to "Nonadaptive," and the number of consecutive zero crossings is set at 1000.

The diagram presented in Figure 5.4 is the electrical circuit (Figure 5.3. IGBT under an inductive load switching with free-wheeling diode, D.) of the IGBT under clamped inductive switching realized in the Matlab/Simulink environment. The IGBT
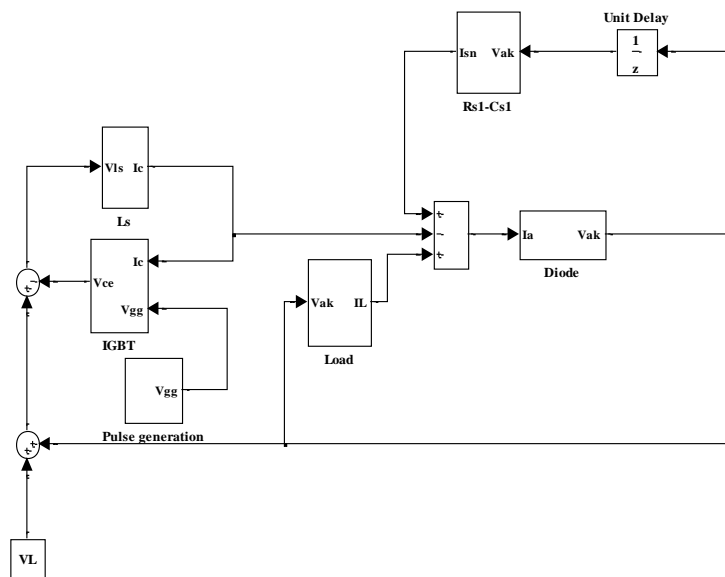

Figure 5.4. **The electrical circuit (Figure 5.3) of the IGBT under clamped inductive switching realized in the Matlab/Simulink environment.**

model described in (129) is used for the simulation.

The high power diode Simulink subsystem is presented in Figure 5.5. It has one input, tdiode current (Id), and one output, the anode-cathode voltage (Vak). The subsystem further contains embedded subsystems: P^+ emitter, N^- drift region, N^+ emitter, and a Sum block, performing addition or subtraction on its inputs, for the total voltage drop.
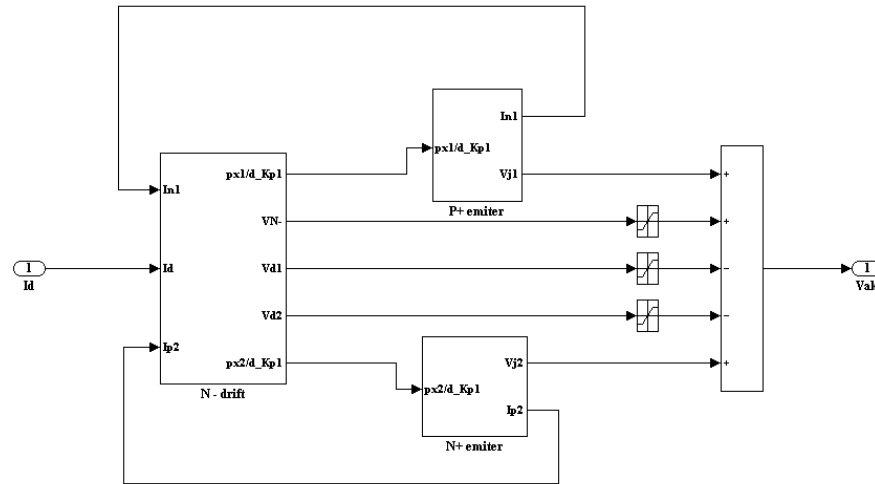
Figure 5.5. Diode subsystem implemented on Simulink.

The P^+ **emitter subsystem** is used to calculate the voltage drop at junction J_1 using Equation (4.28) and the electron current, I_{n1}, using Equation (4.26).

The N^- **drift region subsystem** presented in Figure 5.6 is the most important and complicated subsystem in the power diode model. It consists of four subsystems: carrier storage region (CSR), feedback, drift region voltage drop, and displacement current.
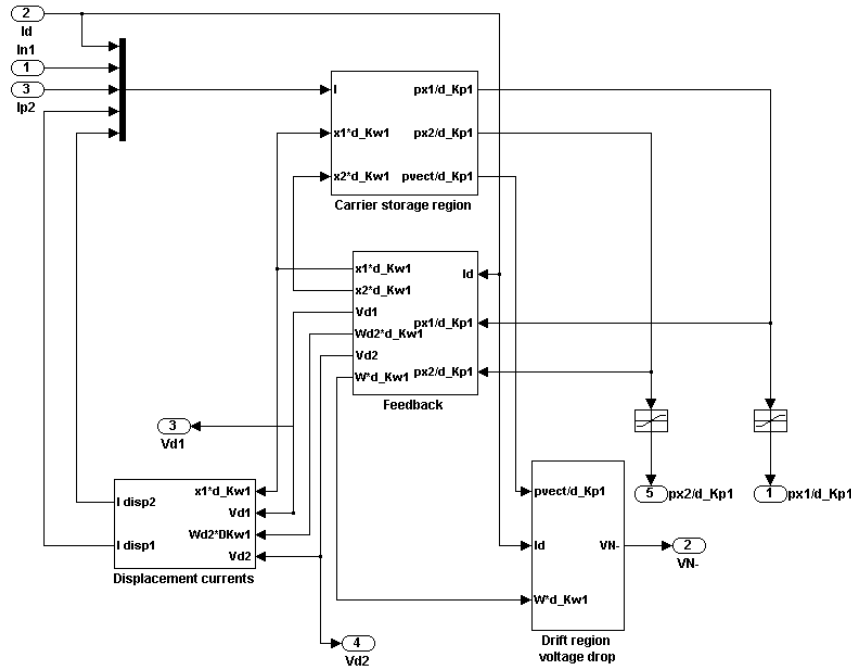
Figure 5.6. Diode subsystem implemented on Simulink.

The CSR subsystem is shown in Figure 5.7. It provides the solution to the ADE, Eq. (4.29), by using the Fourier solution, Eq. (4.30), and the boundary conditions of Eq. (4.31). Eq. (4.34) is used for the left side of the solution of the ADE, Eq. (4.30). To implement Eq. (4.30) in Simulink, differentiator blocks should be used. However, the differentiator blocks are not desirable for use in Simulink; because they contain direct feed-through as their gain increases with decreasing time steps, and this leads to poor numerical convergence (124). To avoid the convergence problem, a transfer function Eq. (5.12) with very small time constant τ_{lim}, typically 0.1-10 ns, is used. For the diode implementation, $\tau_{lim} = 0.1$ ns is chosen.
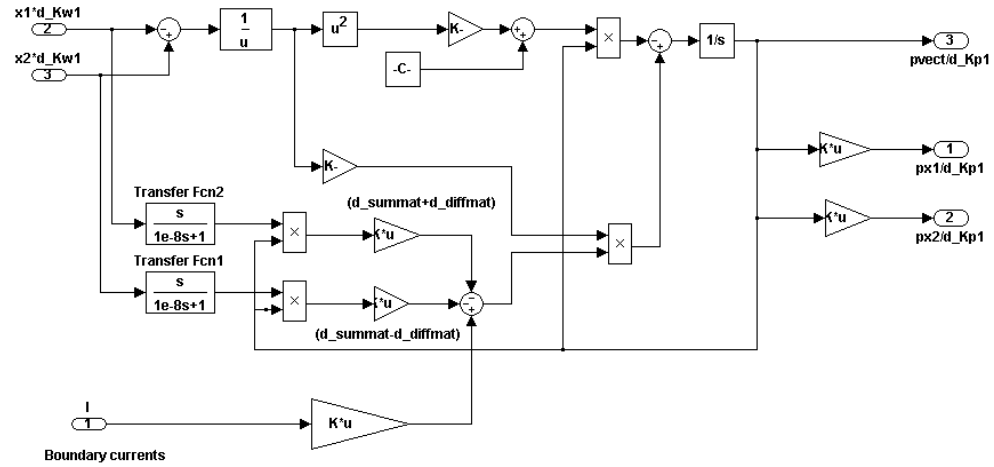
Figure 5.7. Carrier storage subsystem.

$$G(s) = \frac{1}{1 + s\tau_{lim}} \tag{5.1}$$

During the transient, the calculated boundary carrier densities, p_{x1} and p_{x2}, at the boundaries, x_1 and x_2, are in the order of 10^{15} and higher, while some of the currents also increase rapidly; and the Simulink program cannot converge. To improve the converging, a scaling factor, d_Kp1=10^{15}, is used to divide the left side (the currents) of the solution of the ADE (Equation (4.34)). Then, the calculated boundary carrier densities at boundaries x_1 and x_2 will be d_Kp1 times smaller. Therefore, before calculating the parameters (voltages and currents) that are dependent on the carrier densities, p_{x1} and p_{x2}, the carrier densities should be multiplied by the scaling factor d_Kp1.

The feedback subsystem uses the output data from the CSR subsystem, the charge carrier densities p_{x1} and p_{x2}, as inputs. These carrier densities are used to determine V_{d1} and V_{d2} by using Equation (4.36). The boundary positions, x_1 and x_2, are calculated using Equations (4.37) and (4.38). They are input signals to the CSR subsystem and also to the displacement current subsystem.

The value for the carrier densities, p_{x1} and p_{x2}, are limited to a minimum of $n_i/$ d_Kp1 and used to calculate the junction voltage, V_{J1} and V_{j2}, using Equations (4.28) and (4.43). To improve the convergence of the program, the depletion widths, W_{d1} and W_{d2}, calculated using Equation (4.37); and two scaling factors are introduced: d_Kw $=10$ is used to multiply the numerator of Equation (4.37), $2\varepsilon V_{d1}$, and d_Kw2$=10^5$ is used to multiply every member of the denominator of Equation (4.37). As a result, the scaling factor for the widths, W_{d1} and W_{d2}, is d_Kw1$=$(d_Kw/d_Kw2)$^{0.5}$. The scaling factor d_Kw1 should be considered for calculating the boundary positions, x_1 and x_2, using Equation (4.38) and for the other parameters of the program that include them.

The displacement current subsystem calculates the displacement currents at junctions J_1 and J_2 implemented by Equation (4.39).

The drift region voltage drop subsystem shown in Figure 5.8 is used to calculate the
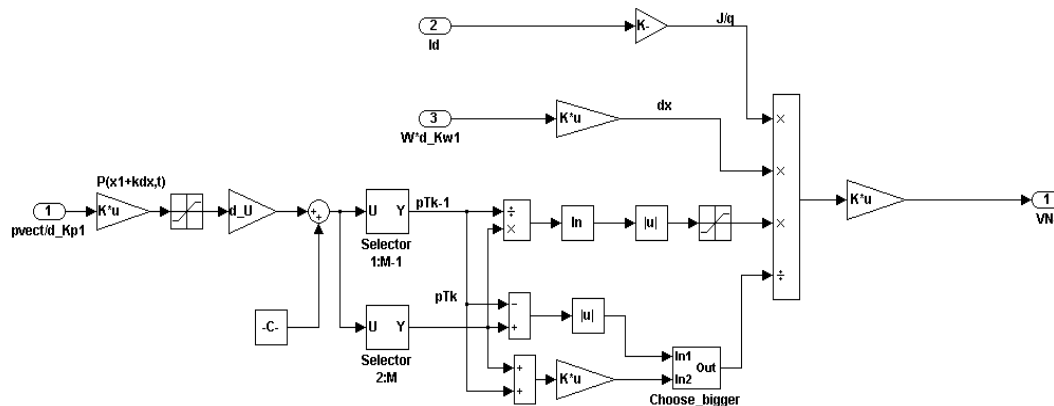

Figure 5.8. Drift region voltage drop subsystem.

voltage drop in the lightly doped drift region V_{N^-}. The subsystem uses the parameters calculated by the other subsystems and calculates the voltage drop in the storage region using Equations (4.40) and (4.41).

The N^+ **emitter subsystem** calculates the hole current, I_{p2}, and the junction voltage, V_{J2}, using Equations (4.42) and (4.43).

The total voltage of the diode, V_{AK}, is calculated by Equation (4.44).

5.4 Simulation Results for Si, SiC, and GaN High Power Diodes

As described in Section 5.2, there is little change to the minimum base width required for a given breakdown voltage (Figure 5.1) for donor impurity doping concentrations at or below 3×10^{13} cm^{-3} for Si, 2.5×10^{15} cm^{-3} for 4H-SiC, and 5×10^{15} cm^{-3} for GaN. Also, if the junction voltages, V_{j1} and V_{j2}, as calculated using Equations (4.28) and (4.43), are summed, the total junction voltage becomes:

$$V_{j12} = V_T \ln\left(\frac{p_{x1}p_{x2}}{n_i^2} \right) \tag{5.2}$$

The total junction voltage, V_{j12}, does not directly depend on the doping concentration of the lightly doped drift region, N_{D1}. However, there is a dependency between the boundary values of the excess charge concentrations, p_{x1} and p_{x2}, and the impurity doping level that then determines junction voltage values. The excess carrier concentrations, p_{x1} and p_{x2}, depend also on the emitter recombination parameters. The analysis is focused on the influence of the doping concentration of the lightly doped drift region, N_{D1}, on the forward voltage drop and the doping concentrations of the other two regions are assumed as constants, the emitter recombination parameters are taken as

constants. They are included in the model for calculation of the total forward voltage drop.

To obtain the minimum forward voltage drop during conduction, V_F, the minimum width of the drift region should be used corresponding to the minimum doping concentration. However, the results from the simulation do not agree with this simple assertion from Equation (5.2). Increasing the doping concentration, N_{D1}, for the same breakdown voltage leads to a decrease of V_F to a minimum value, after which further increases in the doping concentration cause an increase in the forward voltage drop. A higher doping concentration, N_{D1}, lead to reduced injection efficiencies of the higher doped P^+ and N^+ emitters into the drift region, and, therefore, decreases the values of the carrier densities p_{x1} and p_{x2} at the region boundaries.

From Equation (5.2) it can be seen that as the boundary charge concentrations are reduced, the contribution of the junction voltages to the total forward drop tends to cause a reduction in V_F. Simulation results for the boundary carrier densities, p_{x1} and p_{x2}, of a
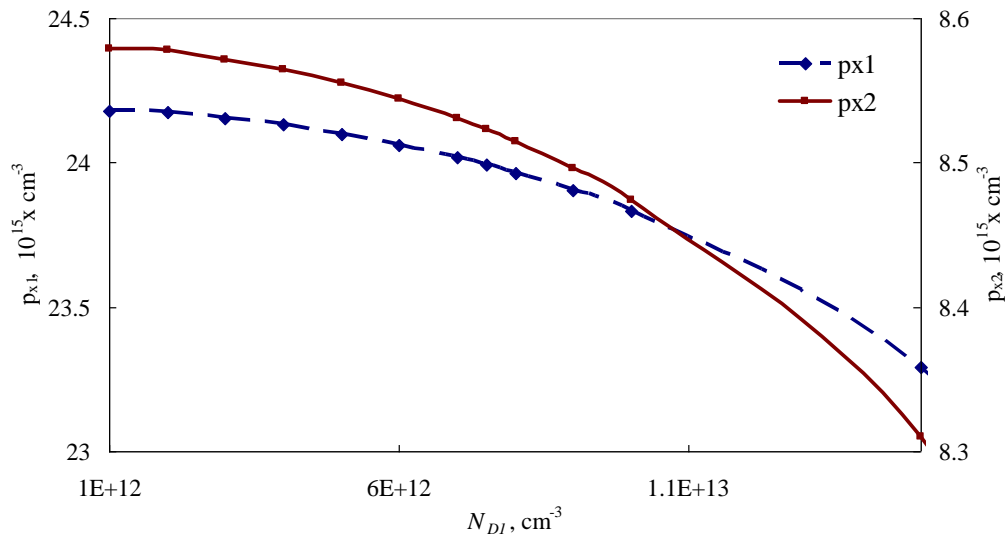

Figure 5.9. The boundary carrier densities, p_{x1} and p_{x2}, of the lightly doped drift region as a function of the doping concentration, N_{D1}, for a 5 kV $P^+N^-N^+$ structure during the on-state.

diode designed to break down at 5 kV are shown in Figure 5.9 and confirm the relationships. The boundary carrier density, p_{x1}, decreases by 3.7% as the doping concentration, N_{D1}, increases from 10^{12} to 1.5×10^{13} cm^{-3}, while correspondingly, p_{x2} decreases by 3.1 %. This explains the difference in the rate of change of the junction voltage, V_{j1}, when compared to V_{j2}, both as a function of base impurity doping.

The voltage drop across the N^- drift region, V_{N^-}, depends on the boundary carrier densities, p_{x1} and p_{x2}, and the doping concentration, N_{D1}, of the lightly doped drift region as shown in Equations (4.40) and (4.41). The simulation results for the voltage, V_{N^-}, are plotted in Figure 5.10a) along with the total junction voltage for comparison. The magnitude of change due to the contribution of the drift region voltage is much greater than the contribution from the junction voltage drops. Thus, the net effect on the total forward voltage drop, V_F (sum of junction and drift region drops), tends to follow that of V_{N^-} and is illustrated in Figure 5.10b).

Thus, an analytical optimization is possible by determining the best doping concentration and base width that simultaneously provide the appropriate voltage breakdown value and the minimal associated forward voltage drop during conduction. From the results shown in Figure 5.10b), the minimum forward voltage for this diode design is at a doping concentration of $N_{D1} = 8 \times 10^{12}$ cm^{-3} (with $V_F = 1.615$ V).

This point is also shown as a star in Figure 5.1a) and Figure 5.13a). Note that typical impurity doping concentrations for high-voltage Si devices correspond to the right-most part of the graph in Figure 5.10b). The analysis shows that optimization of the doping concentration to minimize V_F would mean a reduction of 0.23 V or more, a reduction of more than 12% in the forward drop.
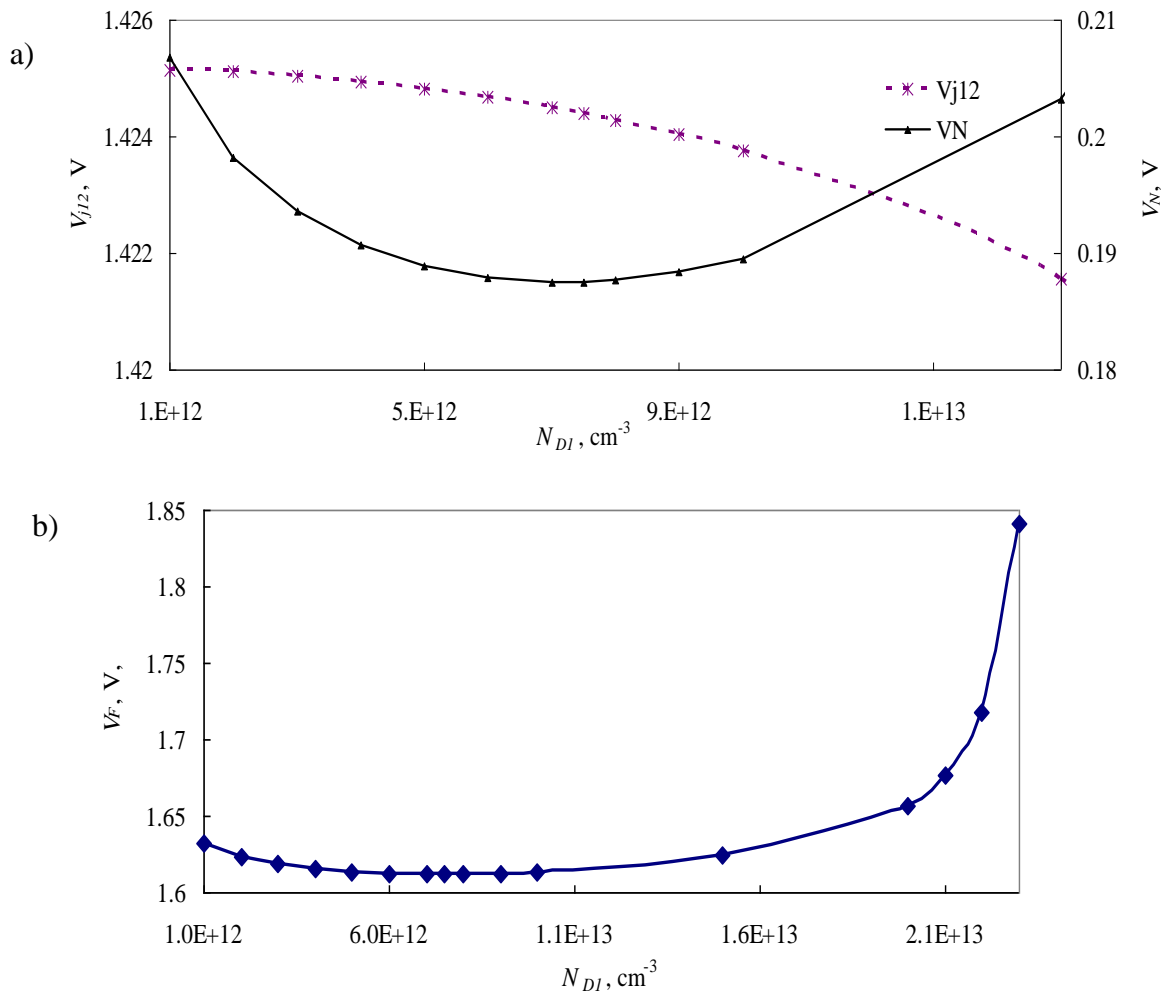

Figure 5.10. The simulation results of a Si $P^+N^-N^+$ structure for a designed breakdown voltage of 5 kV: a) the total junction voltage and the voltage drop across the N^- drift region as a function of the doping concentration of the lightly doped drift region; b) the total forward voltage drop as a function of the doping concentration.

A similar result for the wide band gap device (designed in GaN) is not present as it was for Si. Figure 5.11 indicates that reducing the base doping concentration below 10^{15} cm^{-3} reduces the forward voltage drop by less than 1%. Hence, it is clear that enforcing this optimization scheme for SiC and GaN to tie the n-base doping to the breakdown voltage and the associated forward voltage drop is not necessary. This allows a device designer additional freedom when optimizing for particular performance criteria using wide bandgap materials.
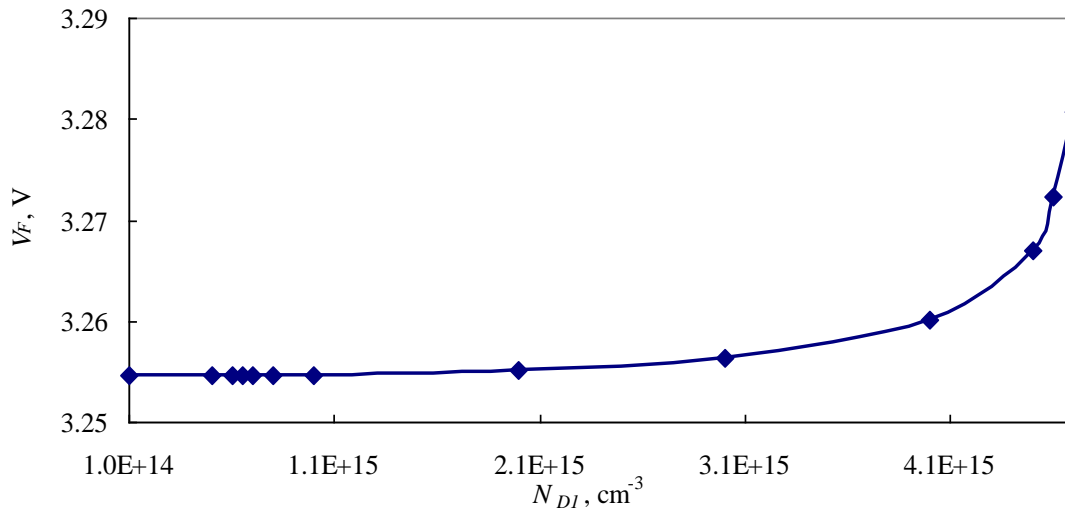
Figure 5.11. The simulation results for the total forward voltage drop as a function of the doping concentration of a GaN $P^+N^-N^+$ structure for a designed breakdown voltage of 5 kV.

The results of the (optimum required) doping concentration of the lightly doped drift region, N_{D1}, as a function of the designed breakdown voltage, V_{BD}, to achieve the minimum forward voltage drop possible are plotted in Figure 5.12. It can be seen from the simulation results that as the desired breakdown voltage increases from 1 to 10 kV,

the optimum concentration, N_{D1}, decreases for the Si diode from 1.98×10^{14} to 3.35×10^{12} cm^{-3}, for the SiC diode from 2×10^{16} to 3×10^{13} cm^{-3}, and for the GaN diode from 4×10^{16} to 7×10^{13} cm^{-3}.
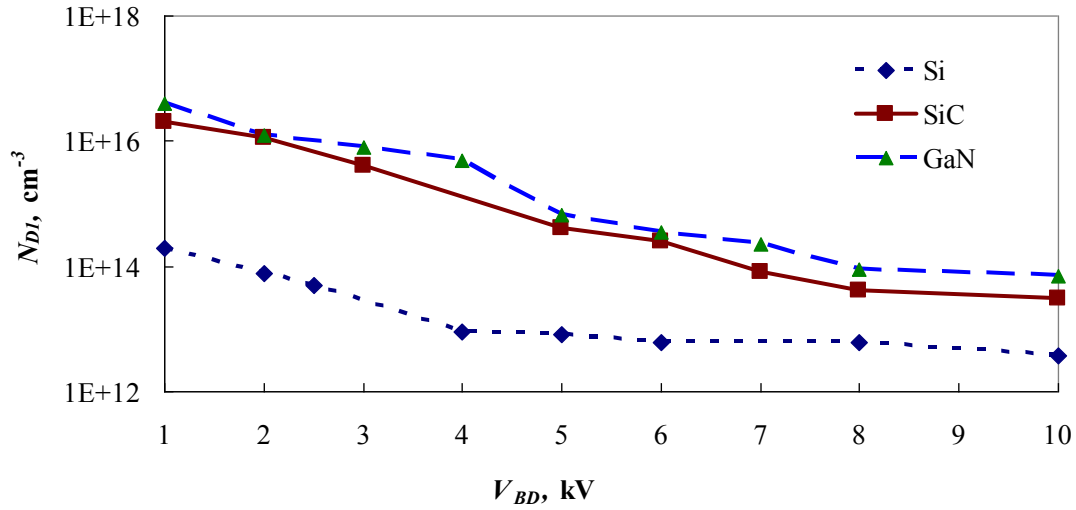
Figure 5.12. **The optimized doping concentration of the lightly doped drift region as a function of the designed breakdown voltage that results in a minimum forward voltage drop.**
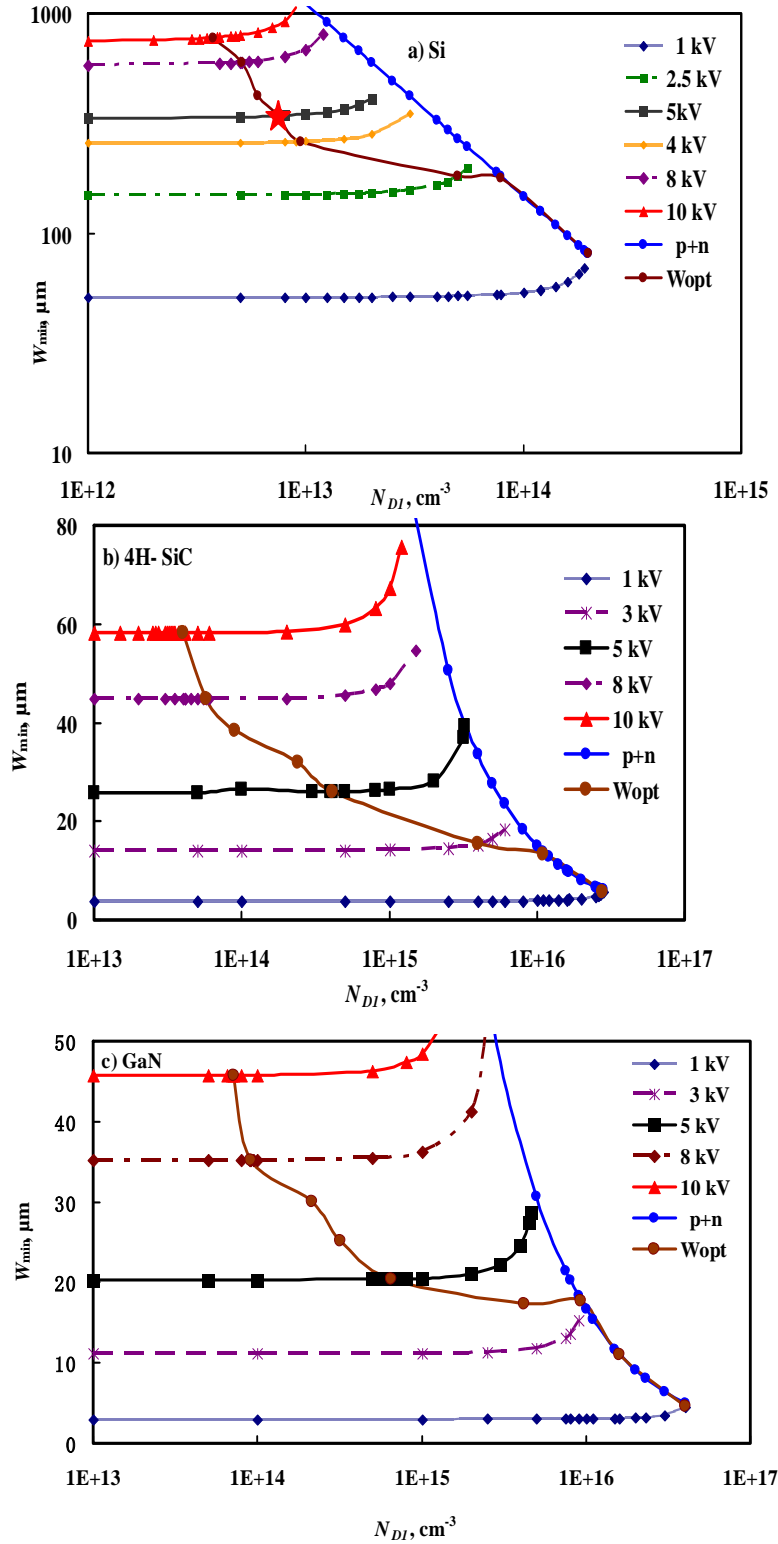
Figure 5.13. Simulated results of the minimum base width of the lightly doped drift region (W_{min}) as a function of doping concentration (N_{DI}) for a P^+N diode and a $P^+N^-N^+$ structure and the optimum width (W_{opt}) of a $P^+N^-N^+$ structure for different designed breakdown voltages that minimize the forward voltage drop in different semiconductor materials: a) Si, b) 4H-SiC, and c) GaN.

The simulation results of the minimum N^--base width (W_{min}) as a function of doping concentration (N_{D1}) for a P^+N diode and a $P^+N^-N^+$ structure for different breakdown voltage designs in Si, SiC, and GaN are presented in Figure 5.13. For breakdown voltages below a certain threshold (material dependent), the P^+N structure is preferred to achieve a minimal forward voltage drop. This threshold is 2 kV in Si, 2.5 kV in SiC, and 3 kV in GaN. Above these threshold values for breakdown voltage, a $P^+N^-N^+$ structure is preferable to achieve a minimal forward voltage drop. These optimal base widths are denoted as W_{opt} in the figure at the associated impurity doping concentration for a given designed breakdown voltage rating.

Minimizing the drift region width strictly based on a voltage breakdown capability requirement from design equations derived using a P^+N structure erroneously gives an increase in forward voltage drop over the optimized width obtained by the process described above for the $P^+N^-N^+$ device. These results collectively provide a device designer with the correct and best first-order values for base region width and associated impurity doping concentration to give the desired breakdown voltage at minimum forward voltage drop in Si, SiC, and GaN.

5.5 Realization of a Power SiC BJT Model in Simulink

The power SiC BJT is simulated under inductive load switching. The circuit schematic is shown in Figure 5.14. A freewheeling high voltage SiC diode, realized in Section (5.3), is employed in the simulation. In Table 5.4 are the BJT parameters provided by the manufacturer and used for the simulation. The carrier lifetimes were

estimated based on experimental switching waveforms. The circuit parameters listed in

Table 5.5 are used for simulation of the SiC BJT under clamped inductive switching load.
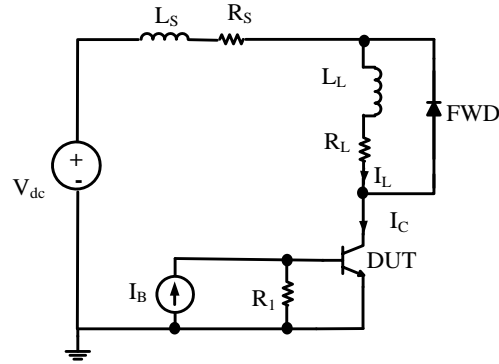
Figure 5.14. Schematic of switching test circuit used for experiments and simulation.

Table 5.4. BJT parameters.

Parameters	Units	Definition	Value
A	cm^2	Active area of the device	0.01
W_{N^-}, W_B	μm	Thickness of N^- and P^+	40, 0.9
N_{N^-}, P_B, N_C	cm^{-3}	Doping of N^-, P^+, and N^+	1.1x10^{15}, 2x10^{17}, 1.2x10^{19}
τ_p, τ_n	μs	Minority lifetime in N^- and P^+	0.02, 0.155
μ$_n$, μ$_p$	cm^{2}V^{-1}s^{-1}	Electrons and hole mobility	900, 90

Table 5.5. Circuit parameters for experiments and simulation.

Parameters	Units	Value
V_{dc}	V	450
R_I	Ω	10^9
R_S/L_S	Ω/nH	1/330
R_L/L_L	Ω/mH	16/23

The model of the high power SiC BJT is implemented using Matlab incorporated

with Simulink. The Matlab program is used to input the basic parameters used by the

Simulink program. The input parameters for the Simulink model are: the device geometry parameters, the doping concentrations in each region (assumed to be uniform), charge carrier diffusion coefficients, and minority carrier lifetimes in the different regions. SiC material parameters, such as hole and electron mobilities, dielectric permittivity, carrier saturation velocity, and the intrinsic carrier concentration (at 300 K) are also necessary for simulation.

The implementation of the behaviour of the BJT in Simulink requires use of a stiff solver due to the widely different time constants present in the model. Suitable solvers for simulation of power semiconductor devices are ode15s and ode23tb (128). The configuration parameters chosen for the SiC BJT model are: solver 23s (stiff/Mod. Rosenbrock); the maximum and minimum step sizes are, respectively, 10^{-6} and 10^{-120} s. The initial step size is set to "auto." The relative and absolute tolerances are set to be 10^{-3} and 10^{-5}, respectively. The simulation advanced options are set to use inline parameters, which means that the parameters are fixed during a simulation run. The zero crossing control is set to be "Disable all."

The electrical test circuit (Figure 5.14) of the SiC BJT under clamped inductive switching is realized in the Matlab/Simulink environment. The diagram is presented in Figure 5.15.
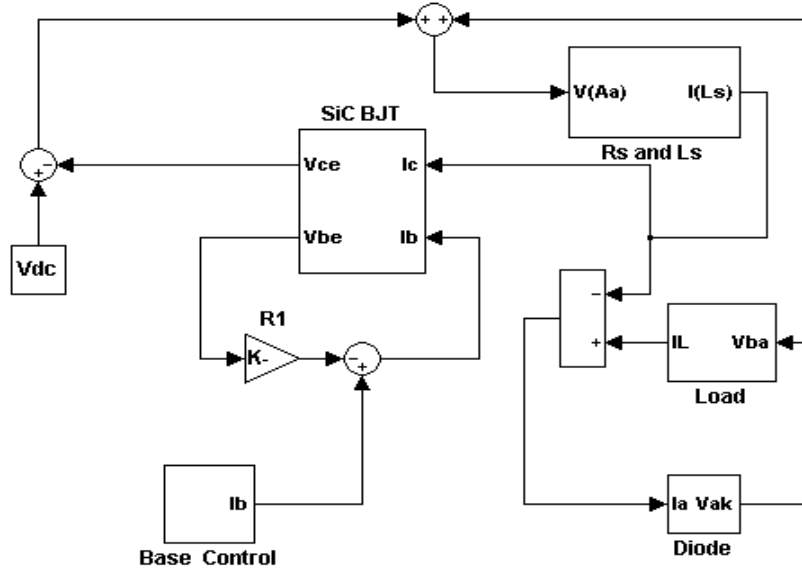
Figure 5.15. **The switching test circuit used for experiments of a SiC BJT (Figure 5.14) implemented on Simulink.**

The high-power SiC BJT Simulink model is presented in Figure 5.16. It has two inputs, collector and base currents, and two outputs, base-emitter and collector-emitter voltages. The BJT subsystem further contains embedded subsystems of the N^- drift region, the P - base, the N^+N^- pseudo-junction, N^+ emitter, and a sum for the total voltage drop.

The N^+ emitter subsystem is used to calculate the voltage drop at the junction J_0 using Equation (4.47).

Figure 5.16. SiC BJT subsystem implemented on Simulink.

Figure 5.17. *P* - base subsystem implemented on Simulink.

The **P - base subsystem** shown in Figure 5.17 is used to calculate the current, I_{n1}, voltage, V_{BE}, and the minority carrier concentration, n_{B0}, at the junction, J_0, by using Equations (4.48)-(4.52).

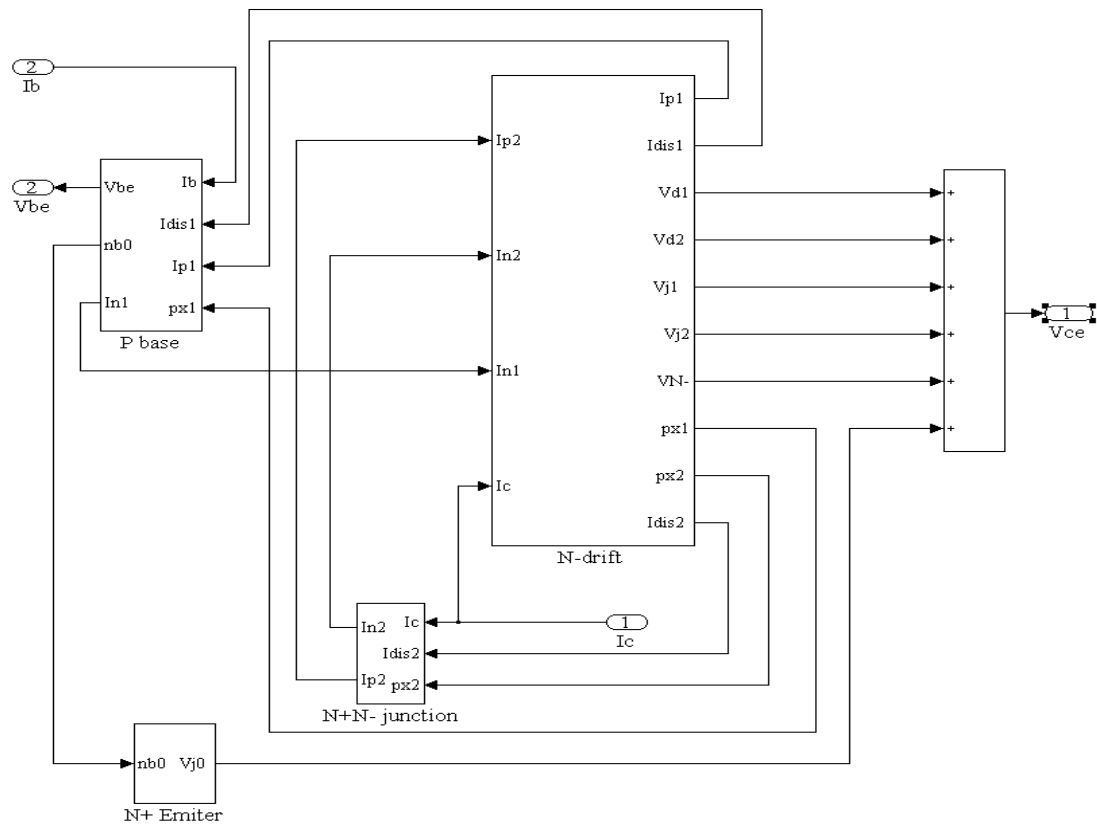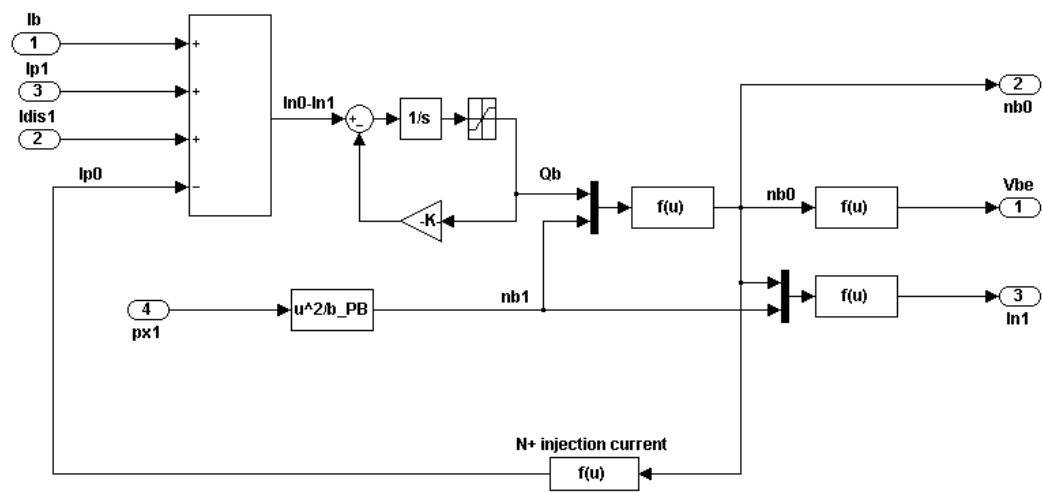The **N⁻ drift region subsystem** presented in Figure 5.18 is the most important and complicated subsystem in the power BJT model. It consists of four sub-subsystems: carrier storage (CS), feedback, drift region voltage drop, and displacement current.

The CS subsystem provides the solution to the ADE, Eq. (4.53), by using the Fourier solution given by Eq. (4.56), derived by Eq. (4.54), and the boundary conditions Eq. (4.55). The CS subsystem of a power BJT is similar to the carrier storage subsystem of the power diode given in Figure 5.7, only no scaling factors are used for the SiC BJT model. The feedback subsystem uses the output data from the CS subsystem and the charge carrier densities, p_{x1} and p_{x2}, as its inputs. These carrier densities are used to determine V_{d1} and V_{d2} using Eq. (4.58). The boundary positions, x_1 and x_2, are calculated using Equations (4.59) and (4.60). They are input signals to the CS subsystem and also to the displacement current subsystem.

The values for the carrier densities, p_{x1} and p_{x2}, are limited to a minimum of n_i and used to calculate the junction voltage, V_{J1} and V_{j2}, by Eq. (4.62).

The displacement current subsystem calculates the displacement currents at the junctions, J_1 and J_2, implementing Eq. (4.61). The drift region voltage drop subsystem uses the parameters of the other subsystems and calculates the voltage drop in the storage region using Eq. (4.63) and (4.64). The drift region voltage drop subsystem for a power BJT is similar to the drift region voltage drop subsystem for the power diode shown in

Figure 5.8, just the diode current (I_d) used to calculate the diode drift region voltage drop is substitute with the collector current (I_C).
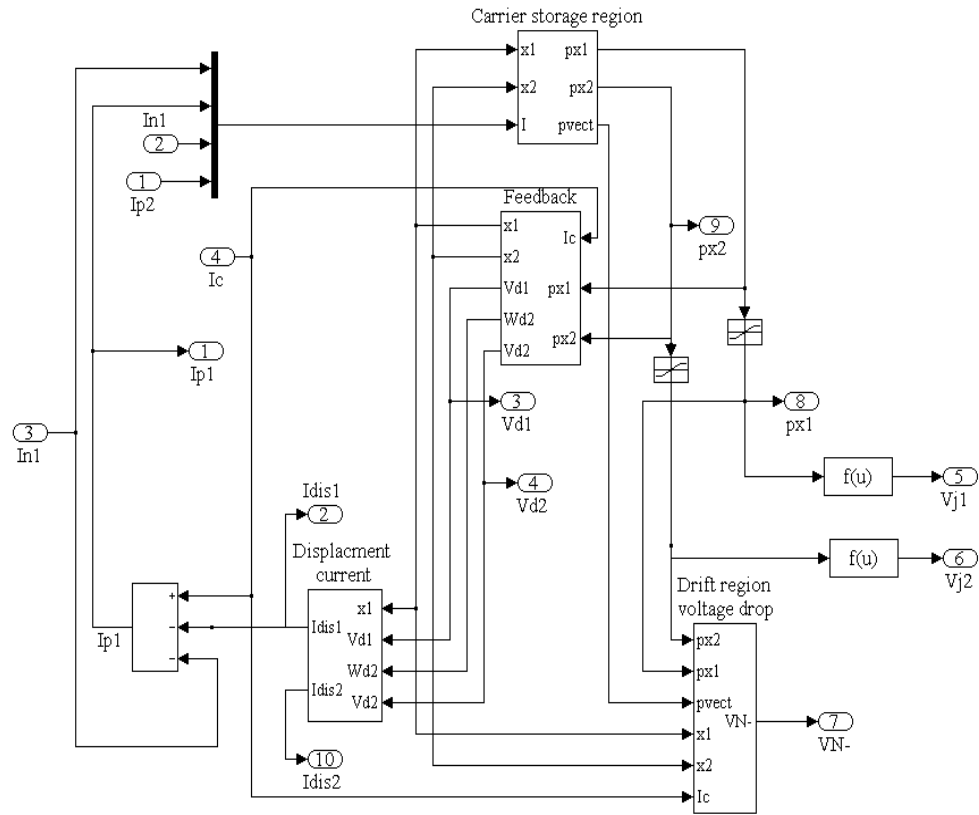

Figure 5.18. N^- **drift region subsystem of the SiC BJT model.**

The N^+N^- **junction subsystem** calculates I_{n2}, I_{p2} using Equations (4.65) and (4.66).

The total voltage, V_{CE}, is given as a sum the junction, the drift region, and the depletion layer voltages from Equation (4.47).

5.6   Simulation   Results   of   the   Switching   Losses   of

a SiC BJT

The switching losses of a power device depend on the application circuit. In general, the total switching energy losses of a power BJT during inductive load switching can be presented as a sum of four components: 1) energy loss induced in the device by the reverse recovery behavior of the freewheeling diode, 2) energy loss induced in the device during turn-on transient - due to the slowly rising collector current, 3) energy loss during turn-off - due to current tailing, and 4) energy loss in the device due to the parasitic inductances and capacitances. The average switching power losses can be obtained by multiplying the total energy losses by the switching frequency. Therefore, at high switching frequencies, the switching losses of a BJT represent a significant portion of its power dissipation; and accurate calculation of the switching losses is an important step in the thermal management system design.

The switching losses of a BJT can be calculated by using current and voltage waveforms.

$$W = \int_0^t i_C(t) v_{CE}(t) dt \tag{5.3}$$

Also, the current and voltage waveforms can be derived for various intervals; and the energy losses are then calculated by a sum of the energy losses of all the intervals:

$$W = \sum_{i=1}^{n} I_{C_i} V_{CE_i} \Delta t_i \tag{5.4}$$

where I_{C_i} and V_{CE_i} are the average collector current and collector emitter voltage for the ith interval, and Δt_i is the interval time. For every interval, I_{C_i} and V_{CE_i} are calculated as the average values of the two end intervals.

In general, the simulation of power devices is done by using variable steps; therefore, Equation (5.4) can be used to calculate the power losses during switching.

Figure 5.19 Figure 5.19a) is applied to the BJT base. The simulation results of the collector current, I_C, and the collector emitter voltage, V_{CE}, are also presented in the Figure 5.19. It can be noticed that the simulated results of the collector current during switching are as expected. The collector current increases to the value of the load current as the base current is applied to the base and then slightly increases until the moment the base current is applied to the transistor. Removing the base current, the collector current starts to decrease, and the transistor is turned off. The overshoot in the collector current, I_C, during the turn-on transient is due to the reverse recovery current of the freewheeling diode, dependent on the diode parameters and especially the minority carrier lifetime. The current overshoot increases as the lifetime increases. The results are shown in Figure 5.20.
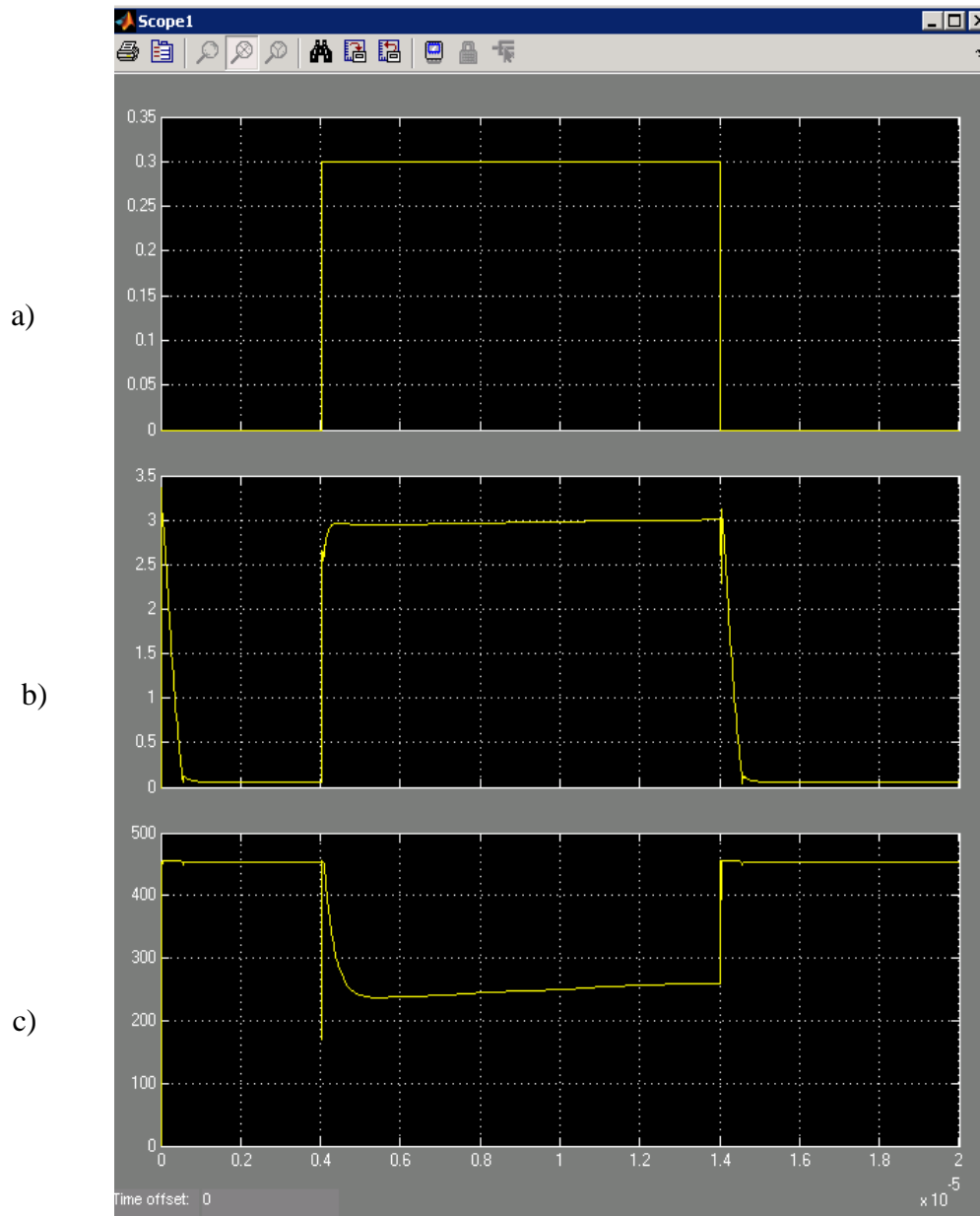
Figure 5.19. **Simulation results of a SiC BJT: a) base current, I_B; b) collector current, I_C; c) collector emitter voltage, V_{CE}.**

The simulation results of the collector-emitter voltage during switching are significantly different compared to the expected switching results for a BJT. From the results presented in Figure 5.19, it can be observed that when the base current is applied to the BJT base, the collector-emitter voltage starts to decrease. The collector-emitter voltage does not decrease to an expected value of approximately 6 V for a SiC BJT

during on-state; but the voltage decreases to approximately 120 V, and after that, it starts to increase to the moment the base current is removed. After removing the base current, the collector-emitter voltage increases to the source voltage; and the transistor is turned off. During turn-on, the collector-emitter voltage experiences a drop, primarily due to parasitic inductance. From the simulation results, it can be seen that the collector-emitter voltage begins to fall when the collector current reaches its peak value.
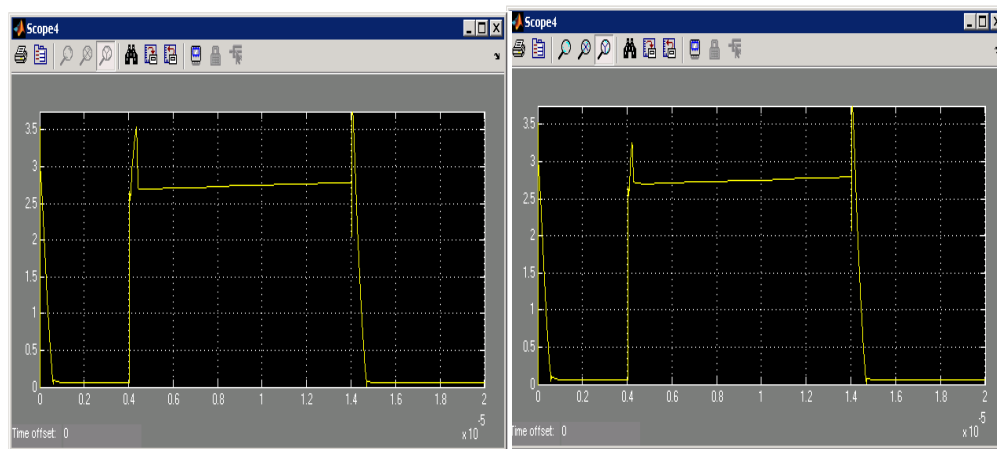
Figure 5.20. Simulation results of the collector current of a BJT for different minority carrier lifetimes: a) 0.2 μs; b) 0.1 μs.

During the on-state, the collector emitter voltage of a BJT is a sum only of the junction voltages and the voltage drop of the lightly doped drift region, because the voltages across the two depletion regions, V_{d1} and V_{d2}, equal zero. The simulation results shown in Figure 5.21**Error! Reference source not found.**, however, show that the voltage across the first depletion region, V_{d1}, is not equal to zero when the transistor is in the on-state.
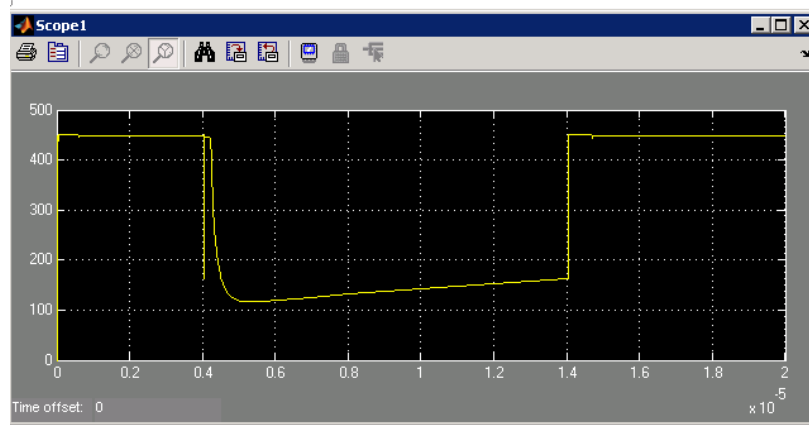
Figure 5.21. Simulation results of the depletion regions voltage V_{d1}.

If the depletion region voltage, V_{d1}, is set to zero, when it becomes smaller than 200 V, the collector emitter voltage will be equal only to the sum of the junction voltages. The collector emitter voltage can be used to calculate the switching losses of the BJT. The simulation results of the collector-emitter voltage in this case are shown in Figure 5.22.
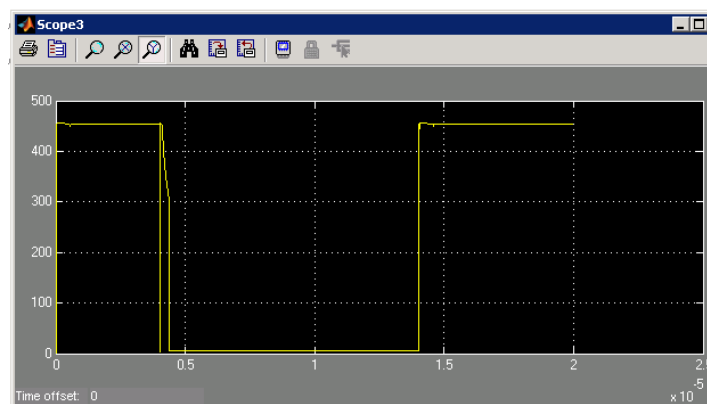
Figure 5.22. Simulation results of the collector emitter voltage, V_{CE}.

From the simulation results, the switching energy losses calculated using Equation (5.4) during turn-on and turn-off are 0.366 and 0.34 mJ, respectively.

5.7 Measurement and Simulation Results of SiC BJT

To evaluate the behavior of the power semiconductor switches, two basic tests are usually employed: a static test and a dynamic test (130). Generally, the static measurement is to validate dc current and voltage characteristics, while the dynamic test is for measuring transient switching behavior.

The static measurement includes the I-V and C-V characteristics of semiconductor devices under dc conditions, the breakdown voltage, and on-state voltage drop. SiC BJT dies used for the measurements are rated at 1200 V and 5A. The I-V curves are measured with a curve tracer, Tektronix TEK 371A.

Figure 5.23. Common emitter I-V curve of SiC BJT at room temperature: a) V_{CE} = 0-2 V; b) V_{CE} = 0-10V.

The measured common emitter I-V curves at room temperature for two different ranges of collector emitter voltage, V_{CE} 0 - 2 V and 0 - 10 V, are plotted in Figure 5.23.

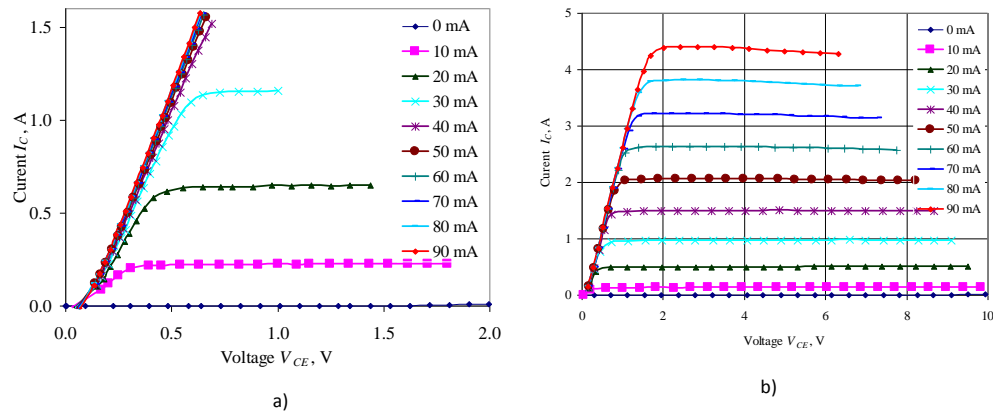The base current is increased from 0 to 90 mA in steps of 10 mA. Typically, increasing the collector-emitter voltage when the transistors are operating in the active region results in a slight positive slope due to the Early effect. Instead, for the high power SiC BJTs, it was observed that the collector current remained constant for low base current values (I_B < 50 mA). For base currents higher than 50 mA, an increasing V_{CE} leads to a decrease in collector current. This is thought to be due to self-heating, which reduces the carrier mobility, and from increased effects due to surface states in these small area devices (128).

The inductive switching test of the SiC BJT is performed using the circuit shown in Figure 5.14. To ensure a ripple-free dc voltage, a bank of five 100 μF capacitors (Model 310DM 410, General Atomic System, San Diego, CA) was connected in parallel with the voltage source. An inductor having 23 mH inductance was used in the circuit to ensure negligible current ripple during switching. A high voltage Schottky diode C3D20060 was used for the freewheeling diode. The experimental results of the SiC BJT collector current, I_C, and collector emitter voltage, V_{CE}, during the inductive switching tests are presented in Figure 5.24.

From the test results, the turn-on and turn-off switching losses calculated using Equation (5.4) are 0.343 and 0.328 mJ, respectively. The differences between simulation and measurement results for the turn-on and turn-off switching losses are 6.28% and 3.52%, re4spectively.
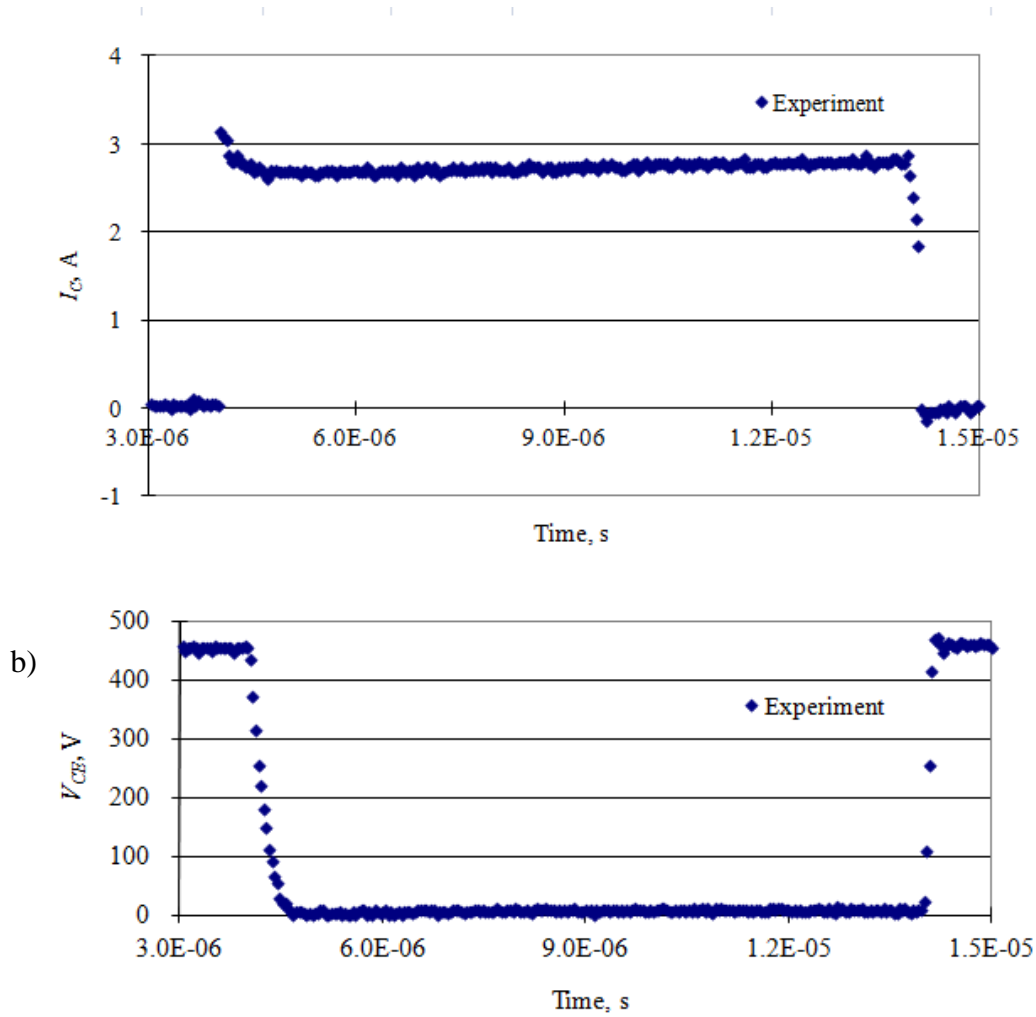
Figure 5.24. Measurement results of a SiC BJT: a) collector current I_C; b) collector emitter voltage V_{CE}.

5.8 Validation of the SiC BJT Model

The SiC BJT model is validated by comparing the simulation with the test results. The test and simulation results of the collector current, I_C, during the inductive switching tests are presented in Figure 5.25. From the results, it can be noted that during turn-off, the simulation results have some disturbance; and the current decreases and increases rapidly without physical explanation. This disturbance may be due to some simulation

problems connected with solving the amplitudes of the Fourier-series $p_k(t)$ that are

determined by using a group of first order differential equations.
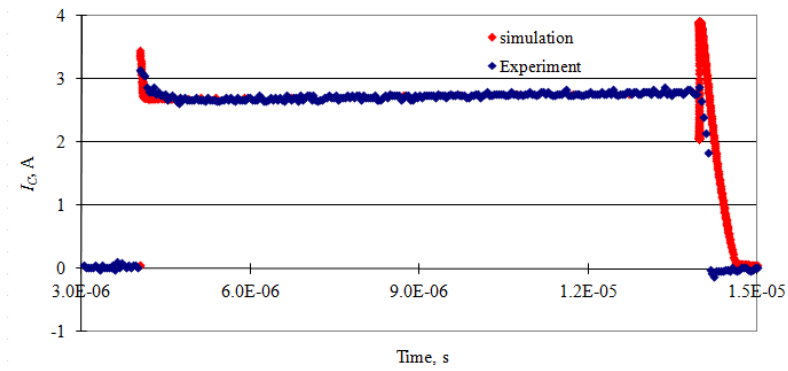
Figure 5.25. Experimental and simulation results of collector current I_C of SiC BJT during the inductive switching tests.

If this part of the simulation results is removed and the collector current is shifted,

the difference between the simulation and test results is insignificant, which can be seen

in Figure 5.26.

The test and simulation results of the collector emitter voltage, V_{CE}, during the
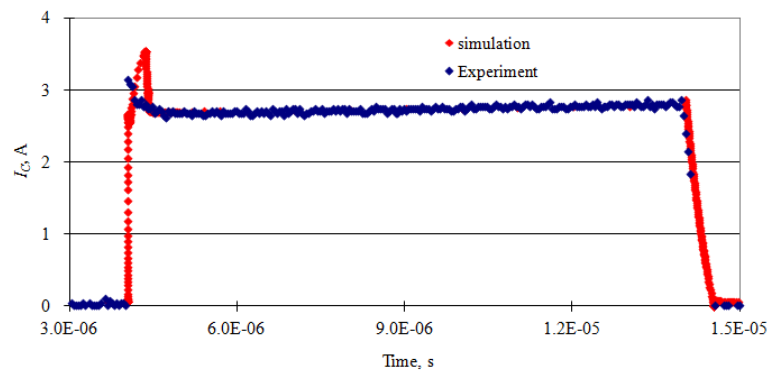
Figure 5.26. Experimental and simulation results of collector current, I_C, of SiC BJT during the inductive switching tests after removing the disturbance during turn-off.

inductive switching tests are shown in Figure 5.27. From the results, it can be noted that during the turn-on, the simulation results had some disturbance and the voltage decreased and increased rapidly and then continued to hold its maximum value without physical explanation. This disturbance maybe also be due to some simulation problems connected with solving the amplitude of the Fourier-series, $p_k(t)$.

Figure 5.27. **Experimental and simulation results of collector emitter voltage, V_{CE}, of SiC BJT during the inductive switching tests.**

If the part of the simulation results where the disturbance appears is removed and the collector emitter voltage is shifted, the difference between the simulation and test results will be insignificant, which can be seen in Figure .
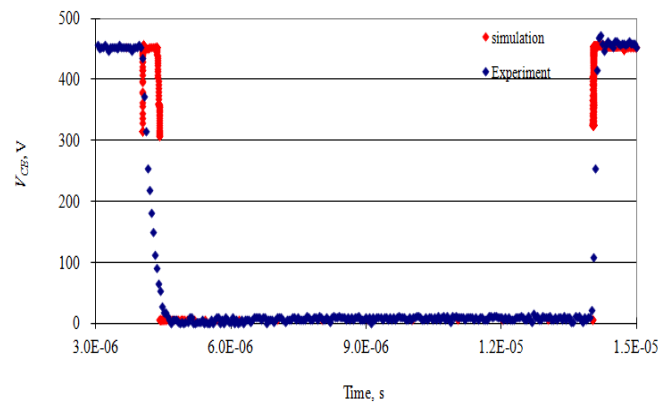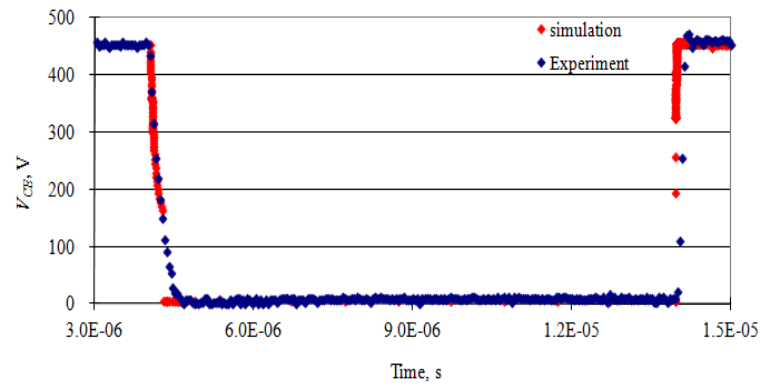
Figure 5.28. Experimental and simulation results of the collector emitter voltage, V_{CE}, of SiC BJT during the inductive switching tests removing the disturbance during turn-off.

Conclusions

The complete one-dimensional model for calculation of the minimum depletion layer width, W_{min}, for a given breakdown voltage, V_{BD}, of a $p^+n^-n^+$ structure is developed and used to calculate the optimum width of the depletion layer for different blocking voltages to achieve a minimal forward drop.

The simulation results show that the calculations of the lightly doped drift region thicknesses and associated breakdown voltages and forward voltage drops lead to incorrect solutions when applied to high voltage $p^+n^-n^+$ structures using the simplified model equations. These simplified expressions were derived strictly for a p^+n structure and have historically been presented in most publications on the subject of power devices and avalanche breakdown. The results also indicate a minimal impurity doping concentration for $p^+n^-n^+$ structures, below which little improvement in breakdown capability can be attained. This is to be expected as the impurity concentration becomes so small that the material can barely be distinguished from intrinsic one. Further, it has been shown that this optimization is appropriate for wide band gap semiconducting materials such as SiC and GaN.

The analysis shows for example that optimization of the doping concentration to minimize V_F in a 5 kV Si diode could result in more than a 12% decrease in the forward drop, while for SiC and GaN this decrease is insignificant, typically less than 1%. Therefore, an optimization of the forward voltage drop by using the optimal doping concentration for corresponding breakdown voltages is necessary for proper design of a Si diode, while for wide band gap material devices this optimization is not necessary.

A SiC power BJT physics-based model is given. The model presents the switching characteristics of the device significantly well. From the test and measurement results are calculated the switching losses of the BJT. The differences between simulation and measurement switching losses during the turn-on and turn-off are 6.28% and 3.52%.

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Appendix

1. Modeling of a power SiC GTO

The device is divided into five regions (Figure A-1), and the basic equations governing the behavior of semiconductor devices are used to analyze the operation of the SiC GTO.
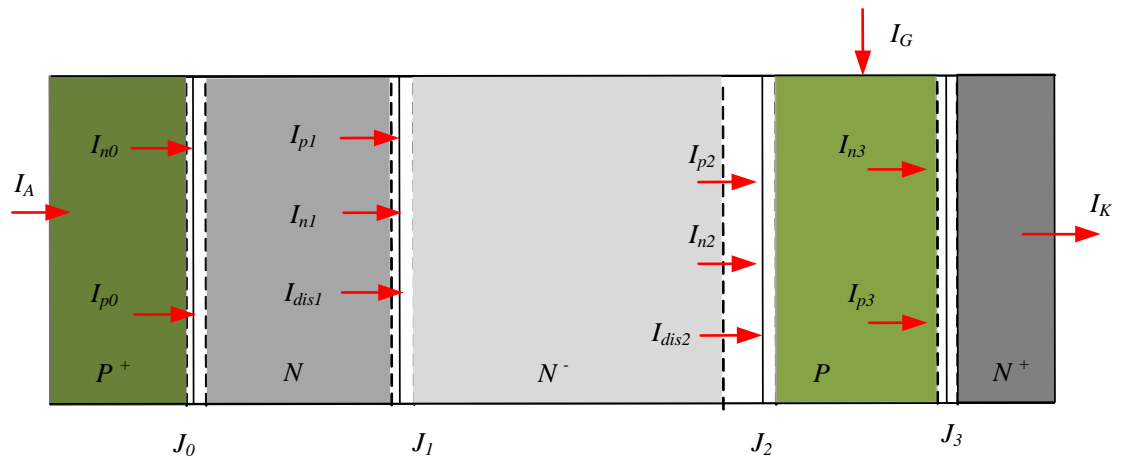

Figure A-1. Schematic structure of a power SiC GTO.

P^+ emitter region

The P^+ emitter region is highly doped; and, therefore, the minority electron current is due to the emitter recombination:

$$I_{n0} = qAh_p N_b p_{b1} \tag{A.1}$$

where, p_{b1} is the hole concentrations at the junction J_0 and h_n is the recombination parameter, depending on the emitter properties, such as doping level, hole diffusivity, and electron lifetime.

The current continuity at the boundaries at the junction J_0 requires that:

$$I_A = I_{n0} + I_{p0} \tag{A.2}$$

N Buffer Layer

Adding a buffer layer in a GTO allows a reduction of the drift region thickness for the same blocking voltage, as the electrical field has a trapezoidal form. The structure allows a rated blocking voltage to be achieved with a narrower N^- drift region compared to the GTO without a buffer layer. This leads to lower on-state voltage and lower switching losses. The buffer layer also causes reduction in the injection efficiency of holes in the N^- drift region, which will speed up the turn-off process of the thyristor.

The lumped charge method can be used to model the charge behaviour in the buffer layer of a SiC GTO, because it has a significantly narrow width and high doping concentration. A schematic structure of the P^+ emitter region and buffer layer of a power SiC GTO is shown in Figure A-2.
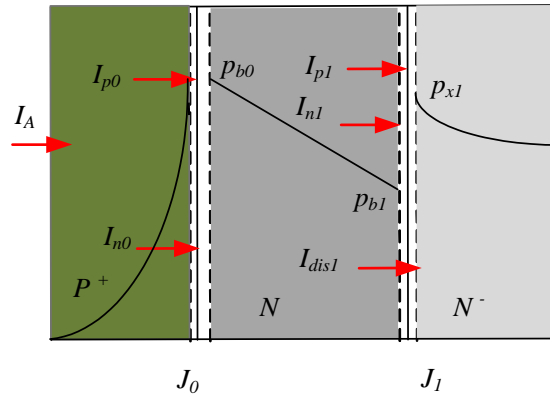

Figure A-2. Schematic structure of the P^+ emitter region and buffer layer of a power SiC GTO.

Using the continuity equation for the buffer region, the injected minority carrier charge can be described by the relation below:

$$\frac{dQ_b}{dt} + \frac{Q_b}{\tau_{pb}} = I_{p0} - I_{p1},$$ (A.3)

where, τ_{pb} is the hole lifetime in the buffer layer, I_{p0} is the hole current at the P emitter and N buffer junction, I_{p1} is the hole current at the buffer/drift region junction, and Q_b is the total hole charge.

The total hole charge in the buffer layer can be expressed as:

$$Q_b = \frac{p_{b0} + p_{b1}}{2} qAW_b$$ (A. 4)

where, p_{b0} and p_{b1} are the hole concentrations adjacent to the junctions with the emitter and drift region, respectively, and W_b is the buffer layer width.

Since the thickness of the buffer layer is much smaller than the diffusion length, the hole concentration gradient may be linearly approximate; and the hole current at the drift region junction is:

$$I_{p1} = qD_{pb}A\frac{p_{b0} - p_{b1}}{W_b}$$ (A.5)

Equation (A.5) can be rewritten as:

$$p_{b0} = I_{p1}\frac{W_b}{qD_{pb}A} + p_{b1} = K_{b1}I_{p1} + p_{b1}$$ (A.6)

The hole concentrations adjacent to the drift region junction p_{b1} is calculated by the equation:

$$p_{b1} = \frac{p_{x1}^2}{N_b}$$ (A.7)

where: N_b is the doping concentration of the buffer layer and p_{x1} is the carrier density at position x_1.

In the on-state, the rate of the change is equal to zero.

$$\frac{dQ_b}{dt} = 0 \tag{A.8}$$

Then Equation (A.3) can be written as:

$$\frac{Q_b}{\tau_{pb}} = I_{p0} - I_{p1} \tag{A.9}$$

Equation (A.4) can be rewrite as:

$$\frac{2Q_b}{qAW_b} - p_{b1} = p_{b0} \tag{A.10}$$

Substituting Equation (A.7) in (A.10) to obtain (A.11):

$$\frac{2Q_b}{qAW_b} - \frac{p_{x1}^2}{N_b} = p_{b0} \tag{A.11}$$

Substituting (A.4) and (A.7) in (A.5) and simplify to obtain the following equation:

$$I_{p1} = \frac{2qD_{pb}A}{W_b} \left(\frac{Q_b}{qAW_b} - \frac{p_{x1}^2}{N_b} \right) \tag{A.12}$$

The hole current at the junction J_0 is:

$$I_{p0} = I_A - I_{n0} \tag{A.13}$$

Substituting Equation (A.11) in (A.1) and then in (A.13) the hole current is:

$$I_{p0} = I_A - qAh_p N_b \left(\frac{2Q_b}{qAW_b} - \frac{p_{x1}^2}{N_b} \right) \tag{A.14}$$

Substitute Equations (A.14) and (A.12) in (A.9) and simplify to obtain the charge in the buffer region as:

$$Q_b = \frac{I_A + qA\left(h_p + \frac{2D_{pb}}{N_b W_b}\right)p_{x1}^2}{\frac{1}{\tau_{pb}} + \frac{2h_p N_b}{W_b} + \frac{2D_{pb}}{W_b^2}}$$

(A.15)

Then charge obtained by Equation (A.15) substituted in Equation (A.14) for the hole current at the junction J_1 and the expression is simplified to:

$$I_{p1} = \frac{I_A - qA\left(h_p - \frac{W_b}{N_b \tau_{pb}}\right)p_{x1}^2}{\frac{W_b^2}{2D_{pb}\tau_{pb}} + \frac{h_p N_b W_b}{D_{pb}} + 1} = \frac{I_A - K_{b2}p_{x1}^2}{K_{b3}}$$

(A.16)

The current continuity at the boundaries at the junction J_1 requires that:

$$I_A = I_{n1} + I_{p1} + I_{disp1}$$

(A.17)

N^- Drift Region

High-level injection conditions can be assumed during most of the time in the transient and on-static state. Under this assumption and quasi-neutrality, the one-dimensional ambipolar diffusion equation that describes the carrier dynamics in the majority of this region is given by the equation:

$$D_{P^-}\frac{\partial^2 p(x,t)}{\partial x^2} = \frac{p(x,t)}{\tau_{P^-}} + \frac{\partial p(x,t)}{\partial t}$$

(A.18)

where D_{P^-} is the ambipolar diffusion coefficient, τ_{P^-} is the high-level carrier lifetime within the drift region, and $p(x,t)$ is the excess carrier concentration.

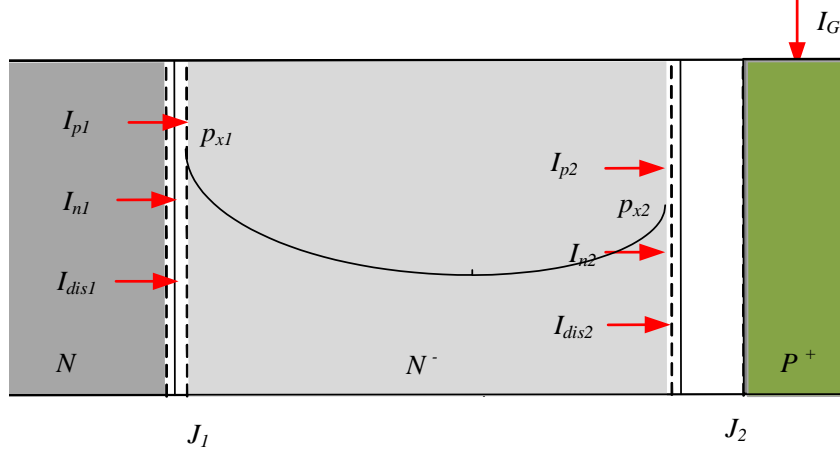A schematic structure of the N^- drift region of a power SiC GTO is shown in Figure A-3.

Figure A-3. Schematic structure of the N^- drift region of a power SiC GTO.

The solution to the ADE is given by the following differential equations as each of them refers to the harmonic p_k of the carrier charge density $p(x)$:

for $k > 0$

$$D\left[\left.\frac{\partial p(x,t)}{\partial x}\right|_{x_2}(-1)^k - \left.\frac{\partial p(x,t)}{\partial x}\right|_{x_1}\right] = \frac{x_2 - x_1}{2}\left(\frac{dp_k(t)}{dt} + \left[\frac{1}{\tau} + \frac{Dk^2\pi^2}{(x_2 - x_1)^2}\right]p_k(t)\right)$$

$$+\left(\sum_{\substack{n=1\\n\neq k}}^{\infty}\frac{n^2}{n^2 - k^2}\left[\frac{dx_1}{dt} - (-1)^{n+k}\frac{dx_2}{dt}\right]p_n(t) + p_n(t)\left(\frac{dx_1}{dt} - \frac{dx_2}{dt}\right)\right)$$

for $k = 0$ (A.19)

$$D\left[\left.\frac{\partial p(x,t)}{\partial x}\right|_{x_2} - \left.\frac{\partial p(x,t)}{\partial x}\right|_{x_1}\right] = (x_2 - x_1)\left(\frac{dp_0(t)}{dt} + \frac{p_0(t)}{\tau}\right) +$$

$$+\sum_{n=1}^{\infty}\left[\frac{dx_1}{dt} - (-1)^n\frac{dx_2}{dt}\right]p_n(t)$$

Using the boundary conditions:

$$\left.\frac{\partial p}{\partial x}\right|_{x_1} = \frac{1}{2q}\left(\frac{J_n}{D_n} - \frac{J_p}{D_p}\right)\Bigg|_{x1} \text{ and } \left.\frac{\partial p}{\partial x}\right|_{x_1} = \frac{1}{2q}\left(\frac{J_n}{D_n} - \frac{J_p}{D_p}\right)\Bigg|_{x1}$$ (A.20)

The left side of Equation (A.19) is:

$$I_{even} = D\left(\frac{\partial p}{\partial x}\bigg|_{x2} - \frac{\partial p}{\partial x}\bigg|_{x_1}\right) = \frac{1}{2qA}\begin{vmatrix} I_{n1} \\ I_{p1} \\ I_{n2} \\ I_{p2} \end{vmatrix}\begin{vmatrix} -\frac{D}{D_n} + \frac{D}{D_p} + \frac{D}{D_n} - \frac{D}{D_p} \end{vmatrix}$$

(A.21)

$$I_{odd} = -D\left(\frac{\partial p}{\partial x}\bigg|_{x2} + \frac{\partial p}{\partial x}\bigg|_{x_1}\right) = \frac{1}{2qA}\begin{vmatrix} I_{n1} \\ I_{p1} \\ I_{n2} \\ I_{p} \end{vmatrix}\begin{vmatrix} -\frac{D}{D_n} + \frac{D}{D_p} - \frac{D}{D_n} + \frac{D}{D_p} \end{vmatrix}$$

The boundary carrier densities, p_{x1} and p_{x2}, at the boundary positions, x_1 and x_2, respectively, are calculated using Equation (A.22):

$$p_{x_1} = \sum_{k=1}^{n} p_k$$

$$p_{x_2} = \sum_{k=1}^{n} (-1)^k p_k$$

(A.22)

The depletion layer voltages, V_{d1} and V_{d2}, across the N^+N^- and N^-P depletion layers, respectively, and are derived using a feedback from the boundary carrier densities, p_{x1}, and p_{x2}:

$$V_{d1} = \begin{cases} 0 & \text{if } p_{x1} > 0, \\ -K_{FV}\, p_{x1} & \text{otherwise.} \end{cases}$$

$$V_{d2} = \begin{cases} 0 & \text{if } p_{x2} > 0, \\ -K_{FV}\, p_{x2} & \text{otherwise.} \end{cases}$$

(A.23)

The associated depletion widths, W_{d1} and W_{d2}, are calculated using a step doping concentration change on each side the junction.

$$W_{d1} = \sqrt{\frac{2\varepsilon V_{d1}}{qN_{N^-} + \dfrac{|I_A|}{Av_{sat}}}}$$

$$W_{d2} = \sqrt{\frac{2\varepsilon V_{d2}}{qN_{N^-} + \dfrac{|I_A|}{Av_{sat}}}}$$

(A.24)

where, N_{N^-} is the doping concentration in the N^- region, v_{sat} is the saturation velocity, and I_A is the anode current.

The boundary positions, x_1 and x_2, are then calculated by:

$$x_1 = W_{d1}$$
$$x_2 = W_{N^-} - W_{d2}$$

(A.25)

W_{N^-} is the width of the N^- region.

The displacement currents, I_{disp1} and I_{disp2}, are due to the changing depletion widths at the junctions J_1 and J_2,

$$I_{disp1} = C_{J1}\frac{dV_{d1}}{dt} = \varepsilon A\frac{1}{W_{d1}}\frac{dV_{d1}}{dt}$$

$$I_{disp2} = C_{J2}\frac{dV_{d2}}{dt} = \varepsilon A\frac{1}{W_{d2}}\frac{dV_{d2}}{dt}$$

(A.26)

The voltage drop in the N^- drift region, V_{N^-}, is calculated based on the carrier concentration in this region:

$$V_{N^-} \approx \frac{I_A}{qA(\mu_n + \mu_p)}\frac{x_3 - x_2}{M-1}\sum_{\kappa=0}^{M-1}\left[\frac{1}{p_{T(k)} - p_{T(k-1)}}\ln\left(\frac{p_{T(k)}}{p_{T(k-1)}}\right)\right] + V_T\left(\frac{\mu_n - \mu_p}{\mu_n + \mu_p}\right)\ln\left(\frac{p_{x2}}{p_{x1}}\right)$$

(A.27)

where μ_n and μ_p are electron and hole mobilities, V_T is the thermal voltage (kT/q), and $p_{T(k)}$ is the carrier distribution calculated by the equation:

$$p_{T(k)} = p\left(x_1 + \frac{k(x_1 - x_2)}{M-1}\right) + \frac{\mu_n N_N}{\mu_n + \mu_p}$$

(A.28)

The current continuity at the boundaries of the drift layer requires that:

$$I_A = I_{n1} + I_{p1} + I_{dis1} = I_{n2} + I_{p2} + I_{dis2} \tag{A.29}$$

P Base Region

The lumped charge method can be used to model the charge behaviour in the base region due to the high doping level and comparatively narrow base width. A schematic structure of the *P* base region of a power SiC GTO is shown in Figure A-4 .
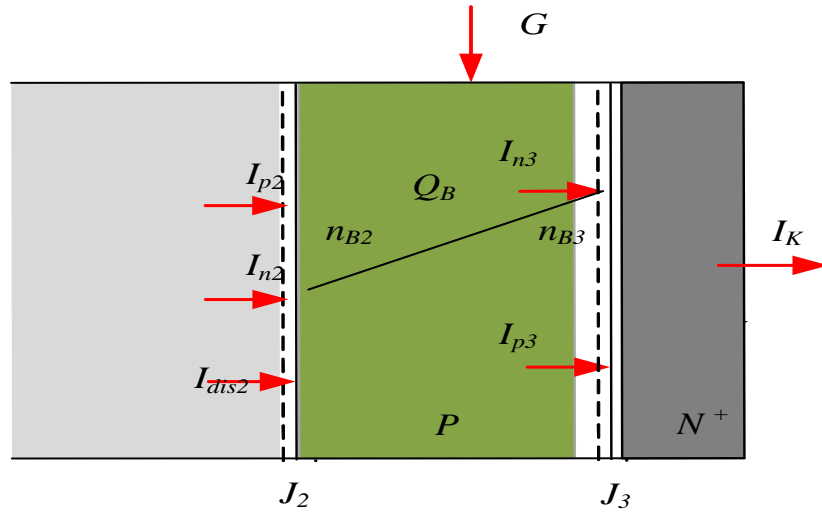

Figure A-4. Schematic structure of the *P* base region of a power SiC GTO .

Using the continuity equation for the base region, the injected minority carrier charge can be described by the relation below:

$$\frac{dQ_G}{dt} + \frac{Q_G}{\tau_{NHL}} = I_{n3} - I_{n2} = I_{p2} + I_G + I_{disp2} - I_{p3} \tag{A.30}$$

where, τ_{NHL} is the high-level lifetime in the *P* base region.

The electron concentration at the *P* - base region boundary, n_{B2} , is related to p_{x2} by the doping concentration of the base N_P by the equation:

$$n_{B2} = \frac{p_{x2}^2}{N_P} \tag{A.31}$$

The base of the GTO is significantly small, and the minority carrier distribution during on-state can be assumed as a line. The total charge in the base can be expressed by the electron concentrations of the two ends of the base, n_{B2} and n_{B3}, as:

$$Q_B = \frac{n_{B2} + n_{B3}}{2} qAW_P \qquad (A.32)$$

Then, the electron concentration at the P-base region boundary, n_{B3}, is:

$$n_{B3} = \frac{2Q_G}{qAW_P} - n_{B2} \qquad (A.33)$$

The electron current at the junction J_3 is:

$$I_{n3} = qD_p A \frac{n_{B3} - n_{B2}}{W_P} \qquad (A.34)$$

N^+ Emitter Region

The N^+ emitter region, shown in Figure A-5, has high doping concentration; and, therefore, it can be assumed as a sign for the minority carrier concentration. The resulting hole current due to the emitter recombination is:

$$I_{p3} = qAh_n n_{B3}^2 \qquad (A.35)$$

where, h_p is recombination parameter depending on the emitter properties such as doping level, electron diffusivity, and electron lifetime.
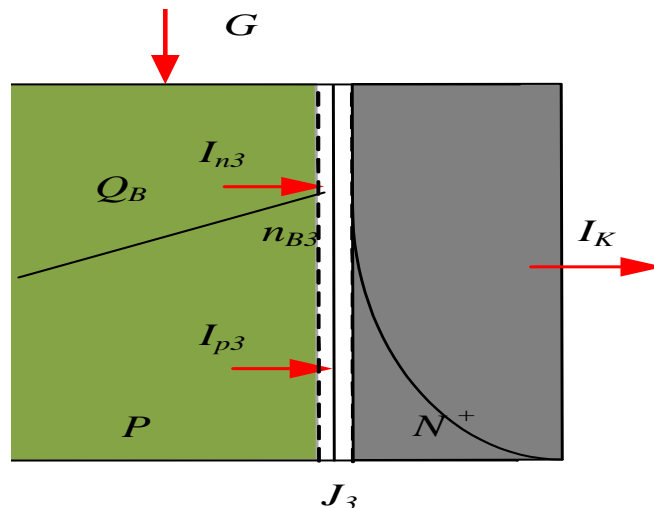

Figure A-5. Schematic structure of the P base region and N^+ emitter of a power SiC GTO.

The voltage drop, V_{AK} , across the GTO is comprised of seven components including the voltages across the junctions, J_1, J_2, J_3, and J_4, the voltage across the two depletion regions, V_{d1} and V_{d2}, and the voltage across the drift region, V_{N^-}.

$$V_{AK} = V_{J0} + V_{j1} - V_{j2} + V_{J3} + V_{d1} + V_{d2} + V_{N^-} \qquad \text{(A.36)}$$

where, the four junction voltages can be calculated by the following equations:

$$V_{j0} = V_T \ln\left(\frac{p_{b0} N_b}{n_i} \right) \qquad \text{(A.37)}$$

$$V_{j1} = V_T \ln\left(\frac{N_{N^-}}{p_{x1}} \right) \qquad \text{(A.38)}$$

$$V_{j2} = 2V_T \ln\left(\frac{p_{x2}}{n_i} \right) \qquad \text{(A.39)}$$

$$V_{J3} = V_T \ln\left(\frac{n_{B2}(n_{B2} + N_P)}{n_i^2} \right) \qquad \text{(A.40)}$$

Realization of Power GTO Model in Simulink

A GTO under an inductive load switching condition is simulated in Matlab® and Simulink®. The circuit schematic is plotted in Figure A-6. A freewheeling Si P^+NN^+ diode, described in Section 4.3, is employed in the simulation. The Matlab program is used to input the basic parameters used by the Simulink program.
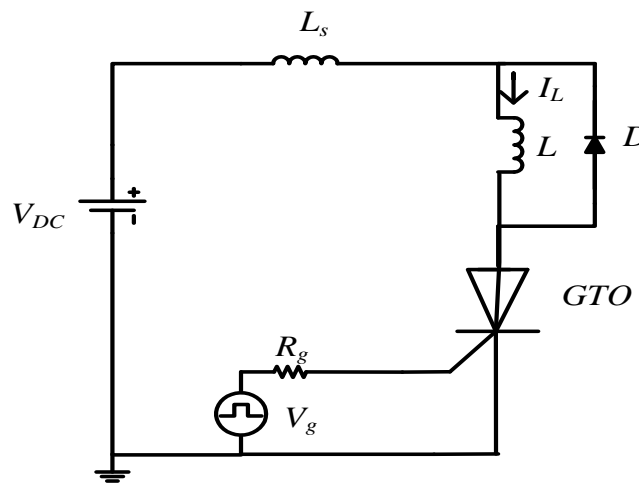

Figure A-6. Schematic of switching test circuit used for experiments and simulation.

The Simulink model input parameters are the device geometry parameters, the doping concentrations in each region (assumed to be uniform), charge carrier diffusion coefficients, and minority carrier lifetimes of the different regions. Material parameters of Si, used for the diode, and SiC, for the GTO, such as hole and electron mobilities, dielectric permittivity, carrier saturation velocity, the intrinsic carrier concentration (at

300 K), and the average ionization coefficients are also needed. The simulation

parameters and circuit parameters are presented in Table A.1 and

Table A.2.

Table A.1. Simulation parameters.

Parameter	Definition	Value
A , (cm^2)	Active area of the device	1 cm^2
W_N, W_{N^-}, W_P, (μm)	Thickness of P, P^- and N	4, 90, and 2.5
W_{P^+}, W_{N^+}, (μm)	Thickness of N^+ and P^+	1, and 2
N_N, N_{N^-}, N_P, (cm^{-3})	Doping of N, N^- and P	5x10^{16}, 2x10^{14} and 10^{17}
N_{N^+}, N_{P^+}, (cm^{-3})	Doping of N^+ and P^+	5x10^{18} and 10^{19}
τ_p, τ_n, μs	Minority lifetime in N^- and P^+	3.5, 0.5 @300K
μ_n, μ_p, (cm^2/(Vs))	Electrons and hole mobility	900, 100

Table A.2. Circuit parameters for simulations.

Parameters	Units	Value
V_{dc}	V	450
R_1	Ω	10^9
R_S/L_S	Ω/nH	1/330
R_L/L_L	Ω/mH	16/33

Due to the widely different time constants present in the model, the implementation

of the behaviour of GTO with a freewheeling diode in Simulink requires a stiff solver.

The configuration parameters chosen for simulation of the model are solver ode 23s

(stiff/Mod. Rosen)); the maximum and minimum step sizes are, respectively, 10^{-6} and

10^{-120} s. The initial step size is set to "auto" and the solver reset method to "fast." The

relative and absolute tolerances are set to be 10^{-3} and 10^{-5}, respectively, step preservation

to "Disable all;" maximum order to 2, and number of consecutive minimum steps is 1.

Zero crossing options are: zero-crossing control is set to "Disable all."

The diagram presented in Figure A-7 is the electrical circuit (Figure A-6) of the

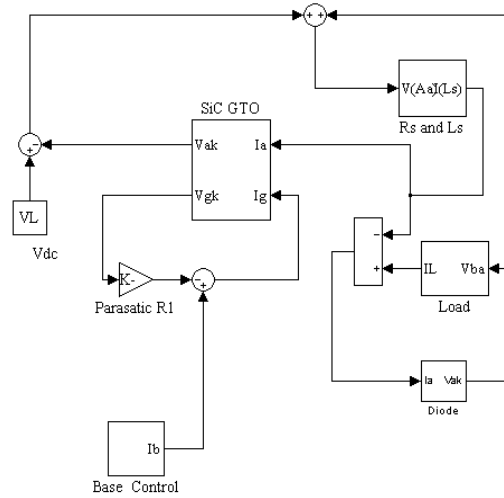GTO under clamped inductive switching realized in the Matlab/Simulink environment

Figure A-7. **The electrical circuit (Figure A-6) of the IGBT under clamped inductive switching is realized in the Matlab/Simulink environment.**

The high power GTO Simulink subsystem is presented in Figure A-8. It has two inputs, gate and anode currents (Ig and Ia), and two outputs, anode-cathode voltage and gate cathode voltage (Vak and Vgk). The subsystem further contains embedded subsystems: P^+ emitter, N buffer, N^- drift region, P base, N^+ emitter, and a sum for the total voltage drop.
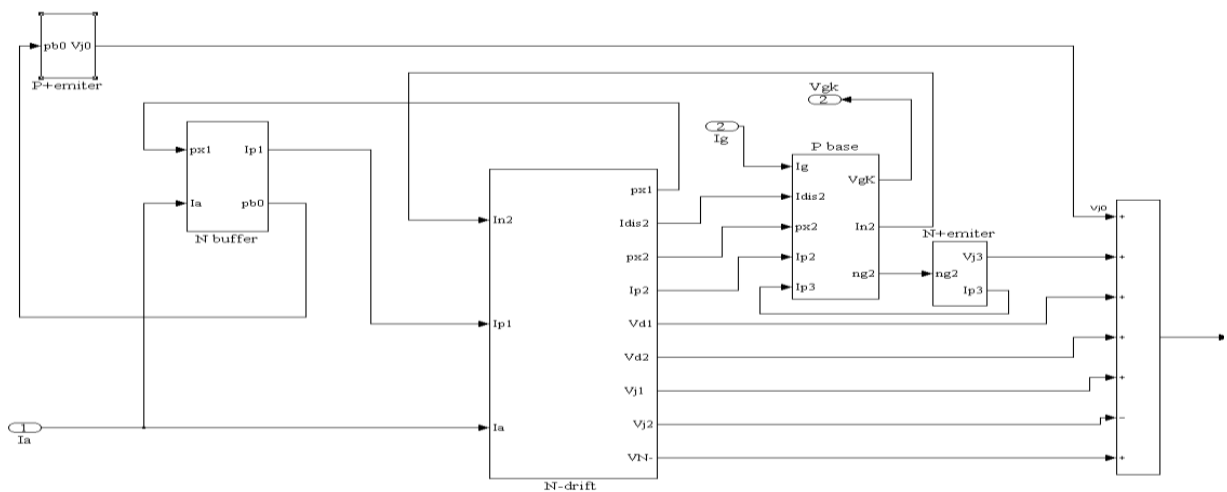

Figure A-8. GTO subsystem implemented on Simulink.

The P^+ emitter subsystem is used to calculate the voltage drop at the junction, J_0, using Equation (A.37). The input parameter for the subsystem is the hole concentration adjacent to N^+ emitter p_{b0}.

The N buffer subsystem is used to calculate the hole current, I_{p1}, at junction J_1 using Equation (A.16) and the hole concentration adjacent to N^- drift region p_{b1} by using first Equation (A.7) and then Equation (A.6). The N buffer subsystem is shown in Figure A-9. It has two inputs: anode current, Ia, and the hole concentrations, pb0.
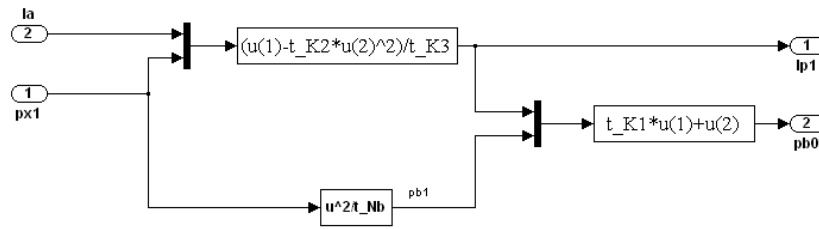

Figure A-9. N buffer subsystem implemented on Simulink.

The N^- drift region subsystem presented in Figure A-10 is the most important and complicated subsystem in the power GTO model. It consists of four subsystems: carrier storage region (CSR), feedback, drift region voltage drop, and displacement current. It is modeled in the same way as for the power diode and BJT by using Equations (A.19) to (A.29). The inputs of the subsystem are anode current, Ia, and hole current at junction J1 and electron current at junction J2. The outputs of the subsystem are: carrier concentrations, px1 and px2 at x1 and x2, displacement and hole currents at junction J2,

depletion voltage, Vd1 and Vd2, junction voltage, Vj1 and Vj2, and drift region voltage

drop VN-.

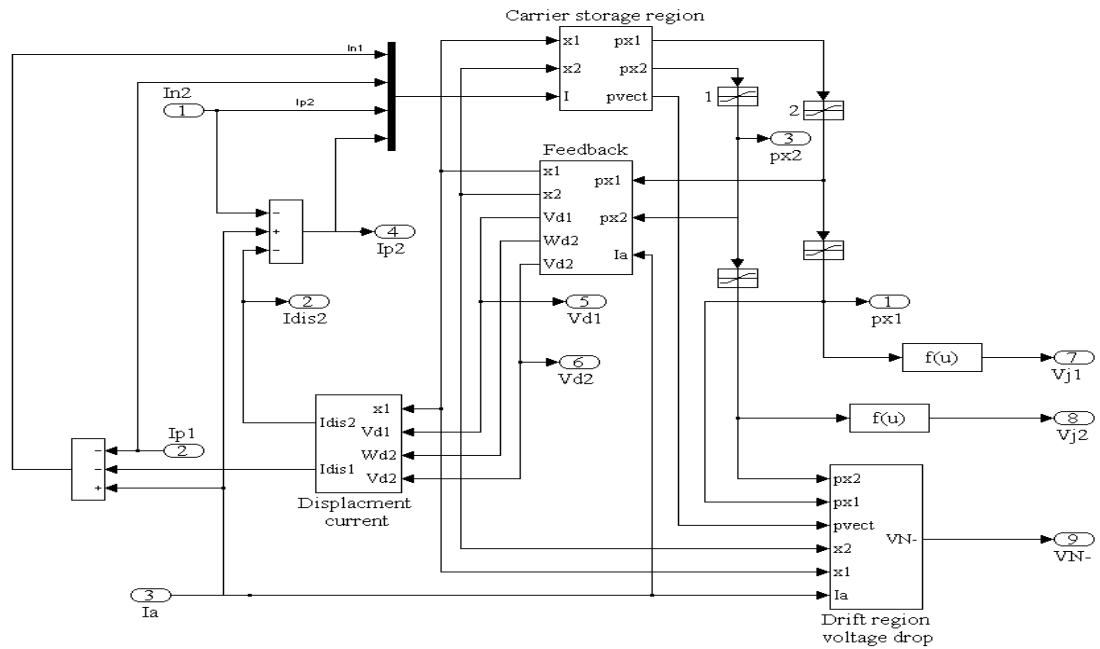**Figure A-10.** *N* **⁻ drift region of power GTO**

The *P* **base subsystem** is used to calculate gate-cathode voltage, VgK, electron

current, and minority carrier at junction J_2. It is modeled in the same way as for the

power BJT. The input parameters are gate current, Ig, displacement and electron currents

at junction J_2, doping concentration, px2 at x2, and hole current at junction J_3.

The *N*⁺ **emitter subsystem** calculates the hole current, I_{p3}, and the junction voltage,

Vj3, using Equations (A.35) and (A.40).

The total voltage of the diode, V_{AK}, is calculated by Equation (A.36).