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# AN INVESTIGATION INTO QUASI-TUNABLE RF PASSIVE CIRCUIT DESIGN

Terry L. Moss

*University of South Carolina - Columbia*

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# An Investigation Into Quasi-Tunable RF Passive Circuit Design Using MEMS Technology and High Inductors

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AN INVESTIGATION INTO QUASI-TUNABLE RF PASSIVE CIRCUIT DESIGN  
USING MEMS SWITCHING TECHNOLOGY AND HIGH Q INDUCTORS

by

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Bachelor of Science  
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---

Submitted in Partial Fulfillment of the Requirements

For the Degree of Doctor of Philosophy in

Electrical Engineering

College of Engineering and Computing

University of South Carolina

2015

Accepted by:

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## **Dedication**

To my darling wife Charlotte Moss, my father Arlon R. Moss, and Harold Askins Jr.

## **Acknowledgements**

The author would like to express his deep gratitude for Dr. Yinchao Chen's support, guidance, and patience over the last 7 and half years as his advisor. Dr. Chen's knowledge in the design of RF passive circuits, guidance in technical writing has been indispensable in creating this dissertation as a quality product.

The author would also like to acknowledge Dr. Mohammad Ali, Norwin Chamok, and Yujia Peng's support in providing measurements for this research, as well as assistance, and guidance from Wensong Wang in understanding PCB fabrication, and Hoa Li's support in identifying a low cost PCB supplier.

The author would like to express his thanks to all of the support staff who have been helpful along the way David London for technical assistance regarding Agilent ADS, Alicia Stolls, Lauren Ridings, Nat Peterson, and Ashely Burt for their assistance in coordination with the Graduate School, and help with registration.

Finally, the author would like to recognize the support from my wife, children, and management from Robert Bosch, without whose support I would not have been able to finish this work.

## **Abstract**

Modern wireless electronic circuit design is continually challenged by the needs to reduce circuit size, and to also function reliably with lower power levels. To that end, two aspects of RFIC circuit design and technology have gained great interest, i.e. RF MEMS switching technology, and RF MEMS passive component development. MEMS (Micro-Electromechanical Systems) technology, originally developed for the defense industry, has been in development since the 1970s, and today enjoys wide range of utilization, from the defense industry to the automotive industry.

Spiral inductors used in RFIC circuits, e.g. silicon technology, are ubiquitous in wireless RFIC applications. The tradeoff with low cost fabrication processes are inductors with very low quality factors which greatly affect the losses in RF passive circuits, and hence their performance. Research in the area of RF MEMS inductors has shown promise for components with significantly higher  $Q$ , and hence has the potential for wide range of benefits in both tunable and non-tunable applications.

Electronic design environments such as Agilent ADS provide automated tools for generating passive circuits, e.g. band-pass filters, based on a specified desired frequency response and circuit topology. However, they typically do not incorporate component  $Q$ , which can greatly affect the actual circuit's performance, into the results of their suggested designs. With this in mind, the development of a systematic approach to predict the relationship between passive circuit component's  $Q$  and its S-parameters can

be of great benefit to the RF electronic circuit designer, especially in the area of wireless passive circuits.

The first of part of this work develops an analytical approach, using mesh-current analysis to derive the relationship between inductor Q, and the S-parameters of a generalized passive RF circuit. For the analysis, the S-parameters of a 90° Lumped Element Hybrid coupler are derived in terms of even mode and odd mode coupler responses using mathematical functions that relate the S-parameters of each circuit to their associated even mode Q, and odd mode Q factors. The results of this research demonstrate that work can still be done in the area of circuit analysis to extend the capability of common passive circuit design tools to include the effects of component Q on the design results, e.g. filter design tools which commonly utilize simple LC circuits as building blocks for more complicated filters.

The second part of this work investigates the performance of different RF switching technologies, i.e. MEMS Switching vs. RF PIN Diode, to a 2-3 GHz quasi-tunable RFIC 90° Lumped Element Hybrid Coupler design utilizing high Q three-dimensional air-core solenoidal MEMS inductors, and IPD Capacitors.

The results of this investigation demonstrated the following:

- The concept of a tunable RFIC Lumped Element Hybrid coupler in the 2-3 GHz range is feasible, and if implement with high Q inductors, comparable to that of off-the-shelf 90° Hybrid Couplers in terms of return loss and isolation performance, but in a much small area, ~ one fiftieth of the surface area at 2 GHz.



- RF PIN Diodes at low current levels can be sufficient when only the phase imbalance of the coupler is critical. If either magnitude loss or magnitude balance is critical, then RF MEMS switching may provide a better alternative.
- RF PIN Diode forward bias resistance approaches that of DC contact switch resistance at higher current levels, e.g. 60 mA, and hence their power consumption becomes the main issue in determining the technology best suited for this application.
- The concept of a ground switched tapped capacitor bank was developed to maximize the switched capacitor Q. This approach optimized the coupler performance compared to a signal switched design.

In the third part of this work, a selectable dual-band 630 MHz and 900 MHz PCB lumped element hybrid coupler is designed, fabricated, and measured. The inductors and capacitors are fabricated with only printed conductors and metal patches respectively on a four-layer PCB. The S-parameters of the measured results and simulations correlated extremely well after adjustment of the substrate dielectric thicknesses used for the simulation of the capacitors. This work demonstrates that lumped element passive components can be cheaply fabricated in PCB technology that are useful in the frequency range of 600 MHz to 1300 MHz, partially covering the GSM and LTE bands, that can be used in quasi-tunable wireless PCB applications, e.g. base stations, while also reducing circuit size in place of commonly found in microstrip distributed circuits.

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# CHAPTER 1 INTRODUCTION

## 1.0 Introduction

Today's use of wireless applications has many different technologies competing in the same frequency range. For example; WLAN applications such as IEEE 802.11 [1.1], low speed communication protocols such as ZIGBEE [1.2], which is gaining application in wireless sensor networks, and Bluetooth all compete in the Industrial, Scientific, and Medical band (ISM) band, are expanding rapidly in many commercial applications. Traditional home wireless handsets operate a 900 MHz, 2.4 GHz, and 5 GHz, while modern cellular phone technology, e.g. 4G LTE has frequency ranges from 1.6 GHz to 2.7 GHz [1.3]. This competing use of many different technologies for communication bandwidth is pushing the limits of traditional circuit design techniques. Furthermore; the decreasing size of smartphones accompanied by touch screen technologies, has reduced the voice quality of cellular phone communications, primarily due to reduced antennae size, thus creating the need for more versatile and efficient RF front ends in the device's transceiver circuitry [1.4]. At the same time, RF MEMS switching technologies research has been ongoing to replace semi-conductor switches e.g. RF PIN diodes, to meet the demands of ever changing technology and expanding commercial applications [1.5]

Re-configurable and tunable RF Circuits have uses in both military and commercial applications. Many of the requirements arrive from the inability to establish global standards for communication technology resulting in the necessity to have wireless

transceivers capable of operating at different frequencies based on the location of their use [1.1], while others come from power optimization of battery powered wireless sensor networks, by means of optimized filter orders, operating in industrial environments which have time dependent dynamic SNR and data rate needs. [1.2].

Various performance aspects of wireless transceiver components are heavily dependent on inductor Q. For example, the phase noise of a LC oscillator used in a VCO, or that of Low Noise Amplifiers (LNA), is heavily reliant on the Q factors of the inductors in the given design, furthermore the high Q components available today are not realizable in low cost CMOS technologies, and are therefore typically implemented in off-chip designs resulting in the overall increase of the circuit's footprint. RF MEMS have the potential to improve all of these technologies, by use of high Q varactors, and inductors as, as well as the utilization of high Q mechanical resonators [1.6-1.8]. The vast majority of re-configurable or tunable RF circuits function on switching discrete capacitors in a given circuit design, while tunable inductors have for the most part not enjoyed similar success.

## **1.1 Objective of the Research**

The main objective of this research is to further RF passive circuit analysis and design approaches in three areas:

- The development of a Q-based design approach based on the theoretical analysis of passive lumped element circuits relating their Q factors and their S-parameters through the application of the mesh current methodology.
- The investigation of potential benefits of MEMS vs. solid state switching through the application of high Q MEMS solenoidal inductors and IPD capacitor

technologies to a PI-transformed  $90^\circ$  lumped element quasi-tunable hybrid coupler design.

- The design, fabrication and measurement of a re-configurable  $90^\circ$  lumped element quasi-tunable hybrid coupler in printed circuit board technology using IPD components.

In recent years, three-dimensional solenoidal inductors, which have significantly increased quality factors over traditional planar inductors, have been developed using MEMS fabrication technology. Compared with conventional two-dimensional printed spiral inductors, these three-dimensional solenoidal inductors also have a physical structure that more naturally lend them to discreet variability via a “tapped inductor” design. These tapped inductors could potentially be utilized with MEMS, or solid-state, switching topologies to select the value of the inductance for a given circuit configuration. In the design of a tunable passive circuit, it’s understood that the switching technology chosen will have an effect on the performance, but the technology needed can be application dependent, depending on the critical performance requirements stated for the design. Furthermore, an underlying issue in any RF passive circuit design, while often unanswered from a theoretical aspect beforehand, is what minimum quality factors for the inductive and capacitive components are needed to meet the performance requirements for the design, this is especially important in the area of RF passive component design where low Q inductors are utilized due to cost, but have a negative impact on circuit performance.



## 1.2 Major Contributions of the Dissertation

The research into the application of MEMS technology in the context of a quasi-tunable lumped element hybrid coupler led to a number of interesting results, of which major contributions are summarized as follows:

- The development of the PI-transformed Lumped Element  $90^\circ$  Hybrid Coupler's S-parameters using mesh current analysis, demonstrating from an educational point of view that basic circuit analysis techniques can be used to express the S-parameters of advanced lumped element four-port circuits.
- The development of mesh current analysis as a systematic approach to derive the mathematical relationship between the S-parameters of a passive circuit and its component's quality factors, while also introducing the concept of even mode Q, and odd mode Q.
- Quantification of the effects of inductor Q on the S-parameters of a PI-transformed lumped element hybrid coupler.
- Design and simulation of a 2-3 GHz Quasi-Tunable  $90^\circ$  Lumped Element Hybrid Coupler using MEMS solenoidal inductors with a layout based on a published MEMS DC-Contact switch.
- Documentation and understanding of the performance tradeoffs between MEMS switches and RF PIN diodes for a re-configurable lumped element hybrid coupler for wireless communication applications.
- Design of 2.65-3.66 pF quasi-tunable capacitor banks using switched signal and switched ground designs.

- Design, simulation, fabrication, and measurement of a 630 MHz and 900 MHz Dual Band re-configurable PCB Hybrid Coupler demonstrating the concept of a tapped inductor-capacitor  $90^\circ$  lumped element hybrid coupler in PCB technology.

### **1.3 Outline of the Dissertation**

Chapter 1 has given an introduction to the research, the background of why RF MEMS switching and passive component technologies can be beneficial in further developing wireless technology, as well as the objectives and results of this dissertation.

Chapter 2 of the proposal is a short review of RM MEMS switching fundamentals, including the advantages and disadvantages of the different type of MEMS switches, i.e. capacitive and DC-contact. The basic principles of RF switching will additionally be discussed, followed by a discussion of the application of RM MEMS to re-configurable circuits, and the state-of-the-art with respect to tunable hybrid couplers in the literature.

Chapter 3 will discuss various aspects of RFIC spiral inductor designs and the influence of design parameters on inductor Q. For the purpose of later work in this paper, the measured results of a published 3-D high Q solenoidal air-core inductor are verified with ADS simulations of a structure approximated by the author. A proposal for a signal-switched tapped capacitor bank is also presented and discussed for use in later coupler design and simulation.

Chapter 4 develops the scattering parameters of the  $90^\circ$  PI-transformed hybrid coupler via mesh current analysis, by introducing the concept of even and odd mode inductor quality factors. The relationship between the scattering parameters as a function of inductor quality factor and vice versa are developed and verified via simulation. With

these equations, the wireless RF circuit designer can estimate the  $Q$  needed to meet the specified coupler response from which they were derived.

Chapter 5 presents the design of an ideal quasi-tunable  $90^\circ$  lumped-element hybrid coupler using three-dimensional solenoidal MEMS inductor technology, and an IPD based switchable capacitor bank. To gain an understanding of the effects of RF PIN Diode switching compared to MEMS DC contact switching, the performance parameters of the coupler, i.e. magnitude and phase imbalance are compared via simulations of each switching technique. As an example of a practical design utilizing a modern MEMS DC contact switch, the ideal design is further implemented in a fully integrated circuit design layout using a MEMS DC contact switch found in the literature to demonstrate the practical effects of cross talk, and design considerations on a realizable integrated circuit layout.

In Chapter 6, the design, fabrication and measurement of a selectable Dual-Band 630 MHz and 900 MHz  $90^\circ$  Hybrid Coupler is presented as a concept demonstration of a re-configurable hybrid coupler using tapped inductor-capacitor banks. The entire coupler is fabricated on a four-layer printed circuit board by a low cost PCB supplier with both the capacitors and inductors fabricated by etching of the PCB metal layers. The layout is based on the contact pattern of an off the shelf RF relay, but for the purpose of simplification, the circuit is duplicated for each frequency by printed relay contacts in lieu of actual switching relays.

In Chapter 7, the research results and conclusions from this dissertation are summarized. The future development and application of  $Q$ -based design for S-

parameters, as well as the further investigation in the design of re-configurable hybrid couplers is also discussed.

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# **CHAPTER 2 RF MEMS, Tunable Lumped Elements, and Tunable 90° Hybrid Couplers**

## **2.0 Introduction**

MEMS stand for Micro-Electromechanical Systems; RF MEMS is the application of MEMS in RF or Microwave Communication electronic circuits. Components that have seen large areas of research and commercial implementation are solid state switches, varactors/capacitors, and inductors. Many advances have been made in the area of solid-state switching devices, e.g. numerous RF PIN diodes are commercially available for the ISM band up to 3GHz [2.1-2.3], and at least up to 18 GHz [2.4]. Nevertheless, improved switching technology is needed to extend the application of re-configurable RF circuits; MEMS switches are being developed to meet that need. Today, MEMS switches, varactors, and inductors have been created that are useful from DC-120GHz [2.5-2.8]. Much work has been done in the area of tunable reactive components, i.e. inductors and capacitors, with most of the research being in the area of tunable capacitors. Some of this work has also been implemented in the area of quasi-tunable 90° hybrid couplers, especially where tunable capacitors can be utilized.

In this chapter the concept of re-configurable circuits will be discussed from an RF transceiver point of view, as well as the basic concept of RF switching. A brief

literature review of tunable passive components with a review of published tunable lumped element hybrid couplers is also given.

## 2.1 Re-Configurable Circuits

As previously stated, wireless electronic devices are ubiquitous in modern technology, ranging in use from personal electronic devices such as the personal computer and Bluetooth headphones, to low speed industrial protocols e.g. ZigBee. This naturally leads to competing interests of different devices for communication channels, and the need for multiband tunable communication devices

There are currently five main methods of implementing tunable circuits, mechanical tuning, ferrite materials, semiconductor varactor, ferroelectric technology, and MEMS [2.9]. As can be seen in Table 2.1 many modern communications devices operate with selectable frequency bands, e.g. 900 MHz and 1800 MHz GSM bands, which are prevalent over most of the world. [2.10]. The appeal of re-configurable circuits is that they can reduce the size the integrated circuit area required to adapt to the different uplink and downlink frequencies of each band in the same hardware.

Table 2.1 Worldwide GSM Frequency Bands

Band	Uplink (MHz)	Downlink (MHz)	Duplex Spacing (MHz)
GSM 900	890-915	935-960	45
GSM1800	1710-1785	1805-1880	95
GSM 900 Extended	876-915	921-960	45
PCS 1900	1850-1910	1930-1990	80
GSM 850 (Americas)	824-849	869-894	45
GSM 450	450.4-475.6	460.4-467.6	10
GMS 480 (Nordic, Eastern Europe, Russia)	478.8-486	488.8-496	10



As a more detailed example, consider the block diagram of the multi-band Low Noise Amplifier (LNA) of an RF receiver shown in Figure 2.1[2.2]. To maximize the SNR of each of channel's LNA, each associated band pass filter must be designed to match the circuit impedance at their inputs, as well be optimally tuned for the desired frequency band of operation, while also requiring switching circuitry for each channel.

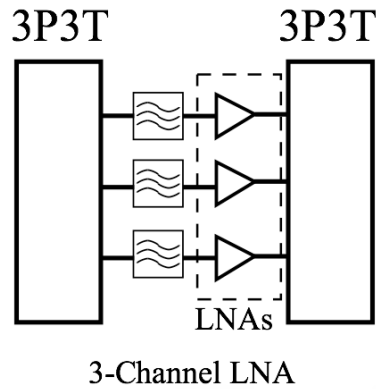


Figure 2.1 Conventional three channel LNA.

Now consider the MEMS based re-configurable LNA shown in Figure 2.2, where the complex switching network with frequency dependent bandpass filters and LNAs, are now replaced with a single tunable band pass filter, and a single LNA. This would potentially have a significant impact on the size and power efficiency of the overall circuitry.

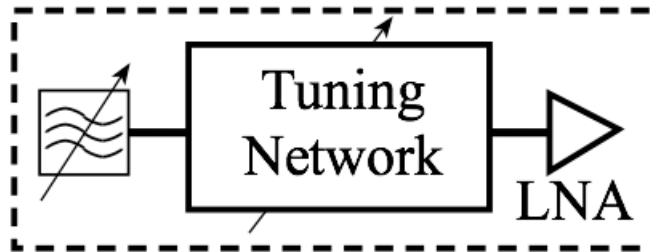


Figure 2.2 MEMS three channel LNA.

Consequently, the potential benefit for MEMS switching in re-configurable applications is obvious, and will now be discussed further in more detail.

## 2.2 RF Switching and MEMS Switches

As previously mentioned, the need for switching in modern RF communication applications arise from numerous applications, e.g. a GSM transceiver does not receive and transmit at the same time, therefore a switching circuit is required for connecting the antenna to the transmitter and receiver as appropriate during operation [2.10]. RF switches are typically utilized in one of two configurations, series or shunt, as respectively shown in Figure 2.3 and Figure 2.4 [2.10]. In the series configuration, the switch provides isolation between the input, which is typically a transmission line with characteristic impedance  $Z_0$ , and a load which is normally matched to the transmission line impedance to minimize reflections and optimize power delivery to the load.

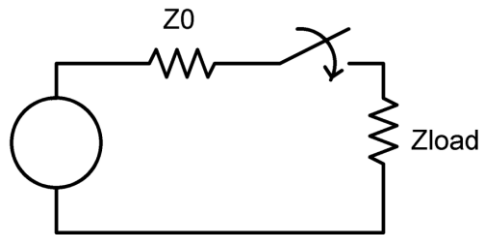


Figure 2.3 RF series switch configuration

The shunt configuration is designed such that the input signal is returned to ground instead of delivered to the load when closed, with isolation between the switch input and ground when open.

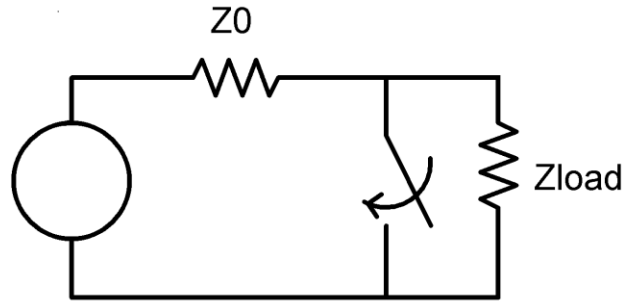


Figure 2.4 RF shunt switching configuration.

In integrated circuit or printed circuit board implementations, RF switches historically work using PIN diodes, or FET switches. Typical series and shunt switching circuits utilizing RF PIN diodes are shown in Figure 2.5 and Figure 2.6 respectively [2.10].

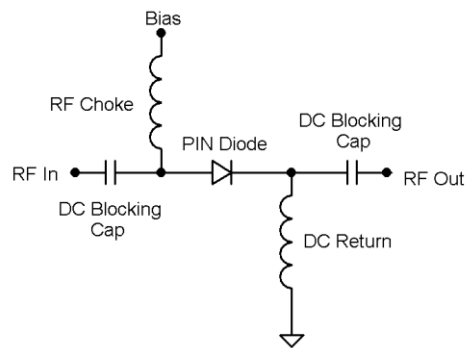


Figure 2.5 RF PIN diode series switch implementation

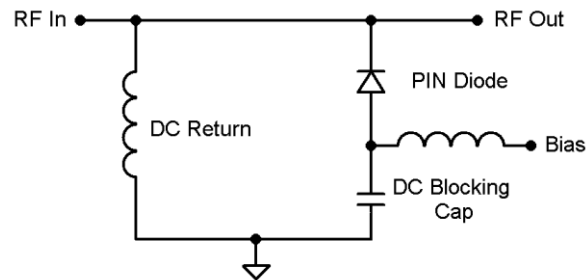


Figure 2.6 RF PIN diode shunt switch implementation.

In each case, a DC voltage is required to forward bias the switching diode to provide a low impedance path in the given design, i.e. between the input and output of the series switch, or a low impedance path to ground in the shunt switch. DC blocking capacitors, and RF chokes are required to allow biasing, but also provide high impedances to prevent unintended signal loss through the circuit.

RF MEMS Switching consist of two basic types, capacitive and DC-contact, both of which can be utilized in two different configurations, shunt and series, with each configuration having its advantages and disadvantages, two examples with their associated electrical models are now shown and discussed. As the first example, consider Figure 2.7 where a diagram of an inline DC-contact switch is shown [2.5]. As can be seen, the pull down electrode is beneath a cantilever, which when actuated with sufficient voltage, pulls down the contact at the end of the cantilever to complete the switch path.

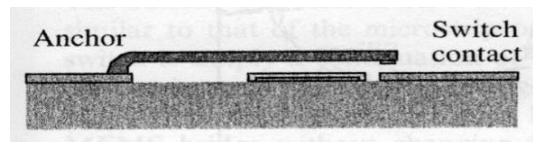


Figure 2.7 MEMs inline DC-contact switch.

The advantage of this type of switch is that the down state switch condition has a very low capacitance  $C_s$ , a series resistance  $R_s$ , typically in the range of  $0.5-2 \Omega$  for most designs, depending on the design and quality of the contact, and with no significant series inductance [2.5].

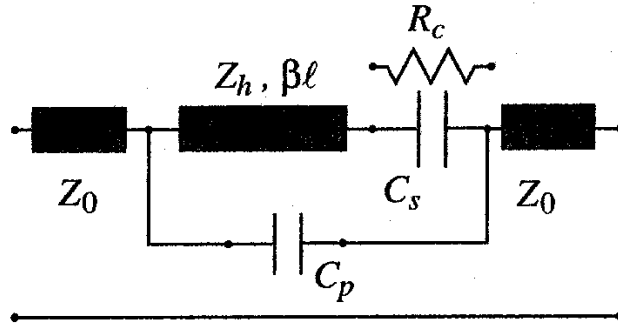


Figure 2.8 MEMs DC-contact switch electrical model.

Next consider Figure 2.9 where a diagram of an inline capacitive shunt switch is shown [2.5]. As can be seen, both contact terminals of the switch are bridged by a metal membrane with a pull down electrode beneath it. The pull down electrode in this case is covered with a dielectric layer such that when the membrane is pulled down, a capacitor is formed with the membrane and the circuits return path, shunting the signal to ground as desired.

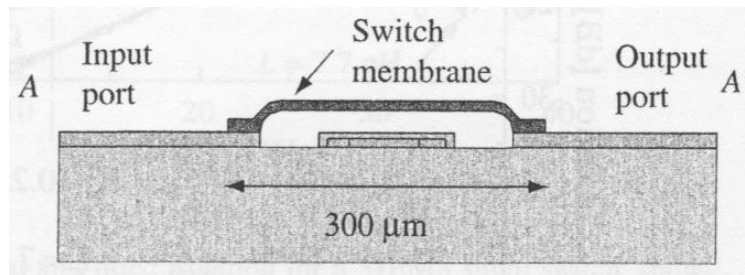


Figure 2.9 MEMs inline capacitive shunt switch.

Finally, consider the capacitive shunt switch electrical model shown in Figure 2.10. The electrical advantage of this type of switch is that the down state switch condition has a low series contact resistance  $R_s$ , depending on the frequency of utilization usually in the range of  $0.1-0.3 \Omega$ , and as in the case of the DC-contact switch a small negligible shunt inductance  $L$  [2.5].

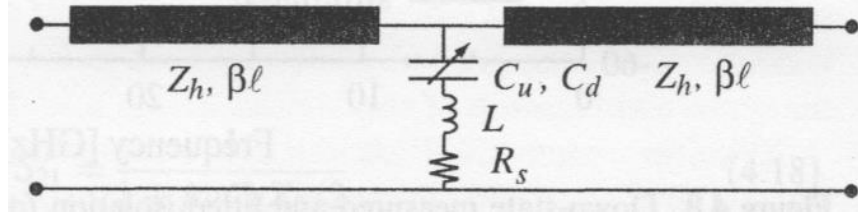


Figure 2.10 MEMS capacitive shunt switch electrical model.

PIN-Diodes and FET switches have p-n junctions that have non-linear i-v relationships. The result of this non-linearity is the production of intermodulation distortion products that degrade circuit performance. One benefit of both switching types, i.e. DC-contact or capacitive, is their linearity and low intermodulation distortion products. RF MEMS switches have been documented with +66dBm to +80dBm Third Order Intercept points (TOI), which are 25-35 dB higher than PIN diodes, and FET switches. Table 2.2 is a summary of the performance comparison between solid-state RF switching devices, and RF MEMS switches [2.11].

Table 2.2 Comparison of MEMS and Semi-Conductor Switches

<i>Switch Technology</i>	<i>Insertion Loss dB</i>	<i>Isolation dB</i>	<i>Switching Power</i>	<i>DC Voltage</i>	<i>Switching Speed</i>
PIN Diode	0.1-0.8	25-45	1-5mW	1-10V	1-5nS
FET	0.5-1.0	20-50	1-5mW	1-10V	2-10nS
MEMS	0.1-1.0	25-60	1 $\mu$ W	10-20V	>30 $\mu$ S

As can be seen, the performance characteristics of RF MEMS are usually as good as FET or PIN diode switching devices. The primary advantage MEMS switch technology is seen in the significant reduction of power consumption which is very important for handheld communication devices. To the contrary, in applications where switching speed is important, e.g. medical imaging applications [2.12], solid state devices are preferable.

In review, the primary performance advantages of RF MEMS can be summarized as improved insertion loss, isolation, power consumption, and linearity, while the primary disadvantages can be summarized as increased switching times, on the order of ~500 times, and increased switching voltages, on the order of 2 to 10 times that of solid state devices [2.5]. Compared to RF PIN Diodes from an implementation perspective, RF MEMS switches are simpler to implement due to the lack of biasing and DC blocking capacitors needed in comparable RF PIN Diode switch circuits.

### **2.3 Literature Review of Variable Reactive Components**

Over the course of many decades, much work has been done in the advancement of tunable reactive components for the advancement of high frequency switching circuits. Varactor diodes are a staple of multi-frequency electronics and are well known to the industry. While variable capacitances are commonly utilized, variable inductances are less common if not non-existent. The following examples are a brief overview of published work from other authors concerning less commonly discussed variable reactive components or designs.

#### **2.3.1 Parallel Plate BST Varactor**

Barium strontium-titanate (BST) is a ferroelectric material, suitable for use as a capacitor dielectric that changes relative permittivity with an applied DC voltage. Tombak, Maria, et al reported on tunable, thin film capacitor for RF and Microwave applications, the physical representation being show in Figure 2-11 [2.13].

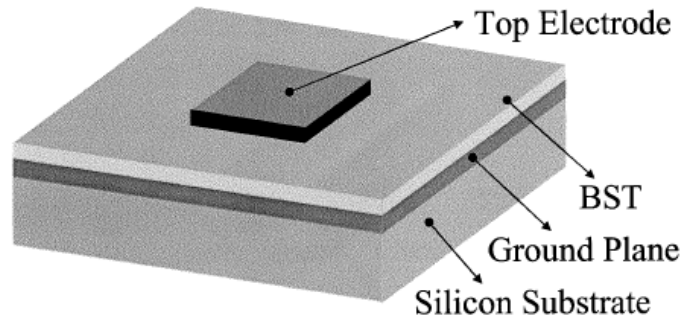


Figure 2.11 Physical representation of a BST varactor.

For this design, the capacitors were fabricated on a silicon substrate with a thickness of 500  $\mu\text{m}$ , using a 1000 Angstrom thick Pt top electrode and BST dielectrics with thickness ranging between .05  $\mu\text{m}$  to 0.5  $\mu\text{m}$ , the relative permittivity variation for a .07  $\mu\text{m}$  thick dielectric film is shown in Figure 2.12.

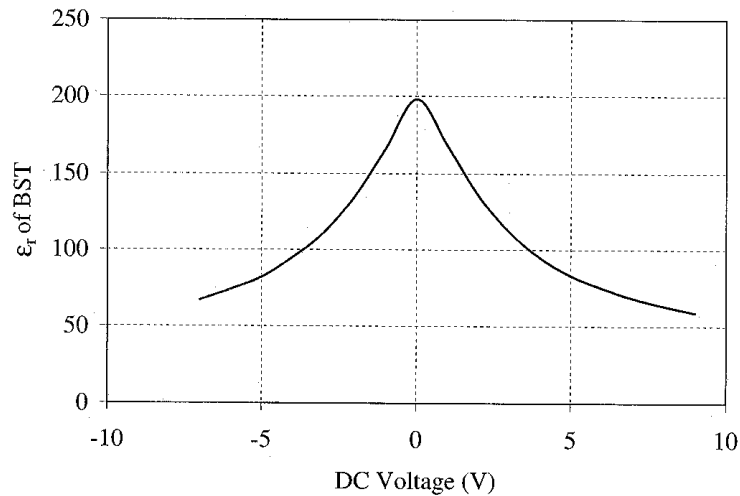


Figure 2.12 Relative permittivity of BST varactor vs. applied voltage.

The relative dielectric constant was measured over a frequency range of 45 MHz to 450 MHz with a tunability of approximately 71% with a maximum applied DC voltage of 9V. A critical parameter for any reactive component it's quality factor. As can be seen in Figure 2.13, this BST capacitor design has a Q below 50 MHz that is comparable with



typical commercial varactor diodes, but exhibit poor performance above 100 MHz, approaching a value of 10 at 450 MHz [2.6].

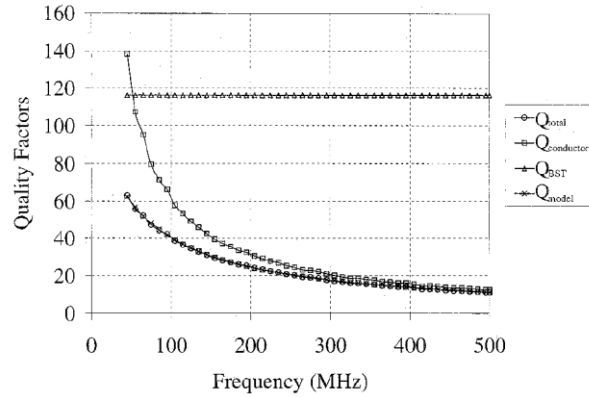


Figure 2.13 BST varactor quality factor vs. frequency.

### 2.3.2 Quasi-Tunable Variable Inductance

While variable capacitors in the RF and Microwave frequency range have for many years seen a great deal of commercial and military application, the development of variable inductors has not progressed. One instance of a quasi-variable inductor, switched by RF MEMS or MOSFET switches, based on a spiral RF inductor design, is show in Figure 2.14. [2.14].

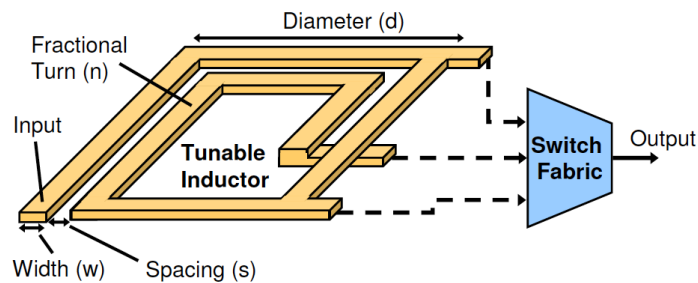


Figure 2.14 Switchable planar spiral inductor.

As shown, three inductances are selectable at the three output ports tapped by the “switch fabric”. This design was numerically optimized using the inductor’s geometric dimensions to maximize the inductor’s quality factor at each value of interest for each port. As can be seen in Figure 2.15, the quality factors have peak values in the 11-13 range, which are reported as being increased over the non-optimized design.

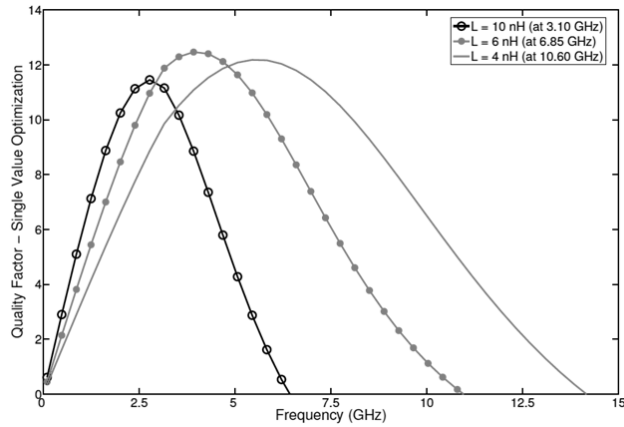


Figure 2.15 Switchable spiral inductor quality factor vs. frequency.

### 2.3.3 Multi-Layer Quasi-Tunable Spiral Inductor

Park, et al, published the results for a MOSFET switchable multilayer spiral inductor, the layout for which is shown in Figure 2.16 [2.15].

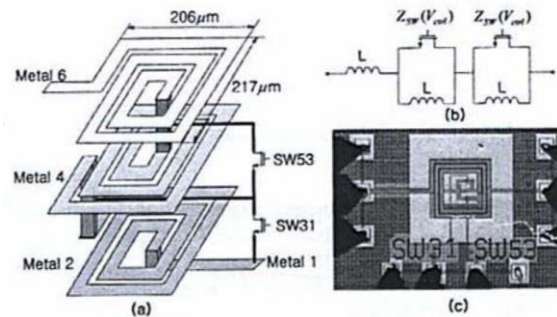


Figure 2.16 Multi-layer quasi-tunable spiral inductor.

This inductor is continuously variable from 2 to 23 nH at 2 GHz, and takes less than 50% of on chip surface when compared to standard single layer inductors. While the circuit exhibits an excellent range of tunability, the losses of its MOSFET switches result in an overall reduction of inductor Q with a maximum of 5 at 1.5 GHz as shown in Figure 2.17.

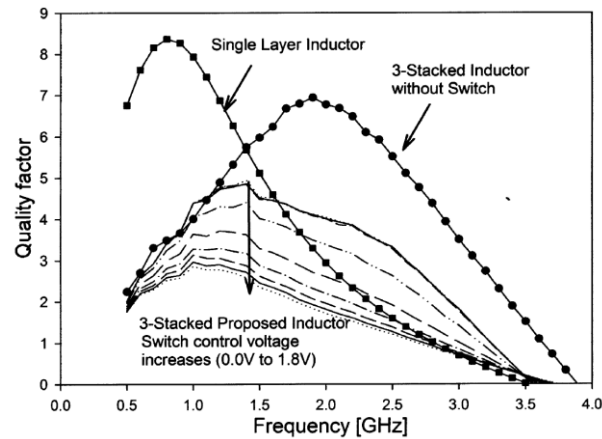


Figure 2.17 Multi-layer tunable spiral inductor quality factor vs. frequency.

### 2.3.4 Piezoelectric Actuated Tunable Inductor

It is well known from basic physics that a primary parameter in the inductance of any wire wound solenoidal inductor is the permeability of the inductor's core. Casha, Grech, et al. reported on a novel tunable inductor design that utilizes a variable permeability magneto-elastic core material show in Figure 2.18 [2.16].

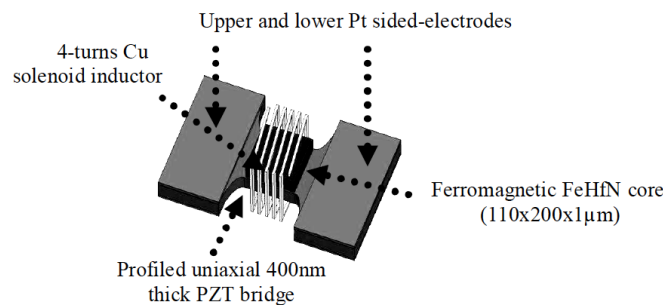


Figure 2.18 Piezoelectric tunable inductor structure.

A variable inductance is achieved by adjusting the DC voltage across the electrodes, which in turn stretches or compresses the ferromagnetic core. Figure 2.19 shows the inductance vs. a normalized inductance-series resistance ratio  $L/R_L$  for a given inductor design. The design shows good tunability from 3 nH to ~ 6 nH, and a near constant  $L/R_L$  ratio. While no quality factors were reported, taking the  $L/R_L$  ratio in the range of 1 and assuming frequency of 2.5 GHz, then the quality factors in the range of 7 to 14 should be expected with the 3 nH to 6 nH inductor design.

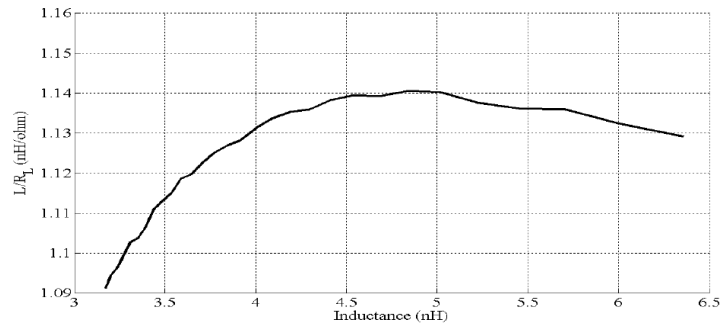


Figure 2.19  $L/R_L$  vs tunable inductance

### 2.3.5 Fixed Inductor with parallel variable capacitance

Nesimoglu, Aydm, et al, reported on a tunable inductor circuit by means of implementing a varactor diode in parallel with a fixed inductance in a VLSI layout as shown in Figure 2.20 [2.17-2.18].

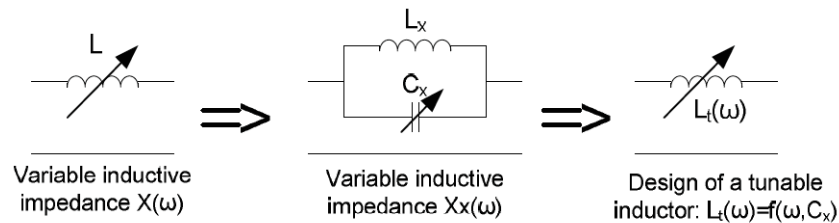


Figure 2.20 Tunable inductor-capacitance structure.

In this arrangement, the overall admittance is the result of the parallel capacitance and inductance as given by (2-1), which is the equation for a resonant parallel tank circuit.

$$Y_x = jB_x = j \left[ \frac{\omega^2 L_x - 1}{\omega^2 L_x} \right] \quad (2-1)$$

For proper operation, the desired frequency range should be well away from  $\omega_r$ . This concept was utilized in the design, simulation, and fabrication for optimization of matching networks for tunable amplifiers in the 850-7500 MHz range. While the optimized gain results for the amplifier were reported, the effective quality factors for the tuning components were not.

## **2.4 Literature Review of Re-Configurable Hybrid Couplers**

Having covered the state of the art of tunable reactive components, the state of the art of re-configurable 90° branch-line hybrid couplers will now be reviewed. Frequency agile or tunable circuits are ubiquitous in the field of microwave communications. While many types of RF and Microwave electronic circuits, e.g. band-pass filters, matching-networks, and resonators, are common in tunable microwave circuits [2.5], the quadrature 90° hybrid coupler has not found much application. The following examples are a summary of two basic design concepts, those using a quasi-lumped element design, where tunable capacitors are utilized with micro-strip transmission lines to achieve quadrature coupling, and total lumped element designs that use varactors in combination with lumped element inductors.

### 2.4.1 Quasi-Lumped Element Couplers

Nishino, Kitsukawa, et al, reported on a tunable hybrid coupler with switchable center frequencies of 1.2 GHz and 2.0 GHz in combination with tunable Band Pass Filters selectable in the range of 800 MHz to 2.4 GHz in 7 channels [2.19]. The coupler shown in Figure 2.21 is implemented in a capacitor enhanced micro-strip form, as initially reported in [2.20].

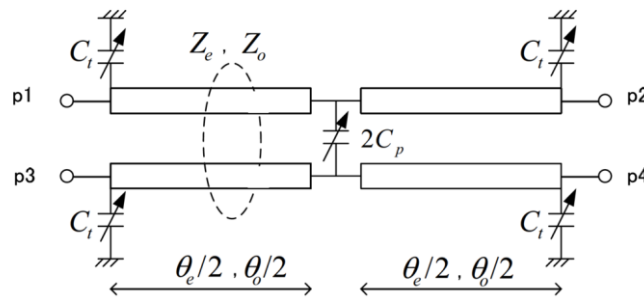


Figure 2.21 Capacitor enhanced tunable hybrid coupler schematic.

The capacitor  $C_p$  is used to strengthen the coupling to the coupled port, i.e. port 4, while the capacitors  $C_i$  are used to tune the coupler for the desired  $90^\circ$  phase shift at the selected frequency. Figure 2.22 shows the physical layout of the Hybrid Coupler accompanied with the Band Rejection Filter Section.

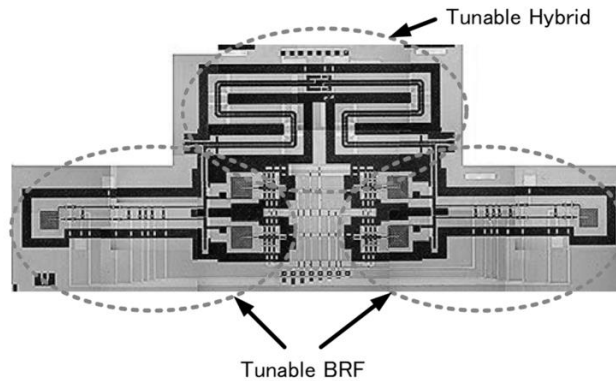


Figure 2.22 Capacitor enhanced tunable hybrid coupler layout.

The through port, i.e.  $S_{21}$ , magnitude performance of the tunable coupler is shown in Figure 2.23. As can be seen, the losses range from -6.38 dB to -5.06 dB, with an average frequency offset from the design center frequencies of approximately 80 MHz. It should also be noted that the phase imbalance and amplitude imbalance as well as the phase offset were not reported.

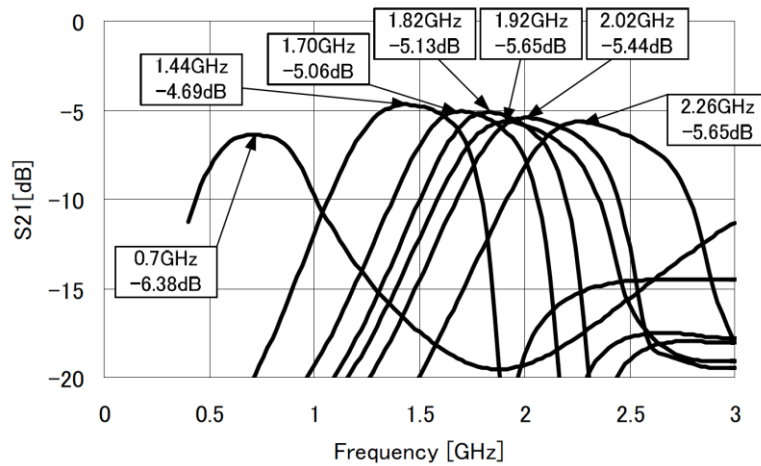


Figure 2.23 Capacitor enhanced tunable hybrid coupler S-parameters.

## 2.4.2 Varactor Tunable Lumped Element Hybrid Couplers

Fardin, Holland, and Ghorbani reported on a  $90^\circ$  tunable lumped element coupler using varactor diodes in place of the fixed capacitances theoretically found in the traditional PI-transformed lumped element hybrid couplers [2.21]. The electrical diagram of the PI-transformed coupler as shown in Figure 2.24 is tunable in the range of 1.71 GHz to 2.17GHz.

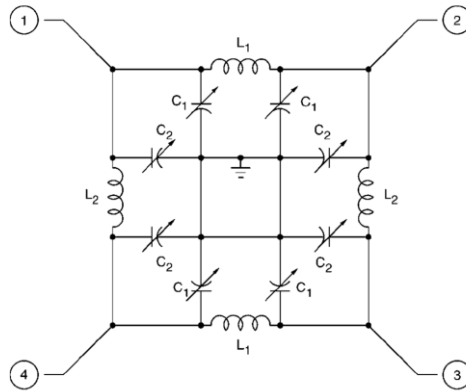


Figure 2.24 Varactor controlled hybrid coupler schematic.

Figure 2.25, the coupler shows reasonable performance between the two frequencies presented, with the best overall performance at 1.7 GHz and decreased performance at 2.17 GHz. The decreased performance in return loss and isolation are to be expected when fixed inductances are used with variable capacitances, since the impedance of inductances of the transformed PI sections no longer match that of the desired frequency.

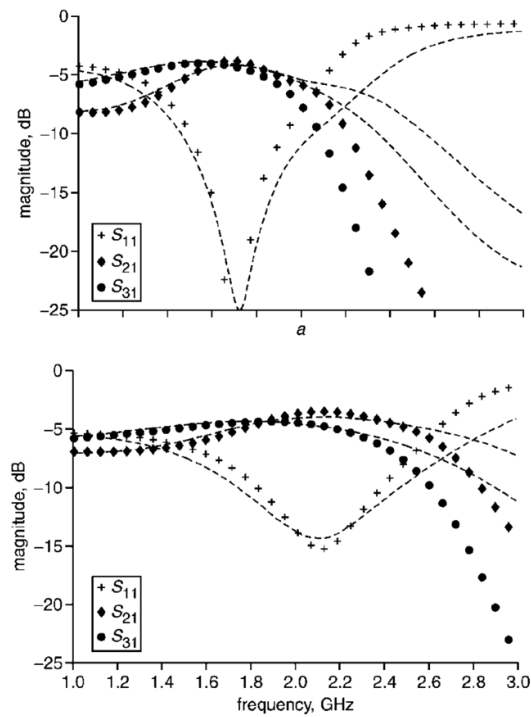


Figure 2.25 S-parameters of the varactor controlled hybrid coupler.



The phase shift response was reported to be in the range of  $92^\circ \pm 3^\circ$  for the uplink Frequency, and  $90^\circ \pm 2^\circ$  for the downlink frequency, and is show in Figure 2.26.

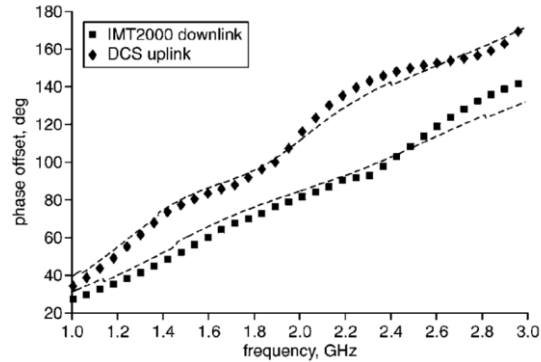


Figure 2.26 Varactor controlled hybrid coupler phase response.

As a further illustration of the varactor controlled tunable coupler, Ernst, Holland, and Ghorbani additionally reported an extended development of tunable lumped hybrid coupler in MMIC form using Barium Strontium Titanate (BST) varactors in place of the original diode varactors [2.22]. As can be seen in Figure 2.27 compared to Figure 2.24, the variable capacitors have been replaced with BST Varactors, which change capacitance by variation of the effective dielectric constant of the substrate as a function of applied voltage across the substrate, but the topology is otherwise unchanged.

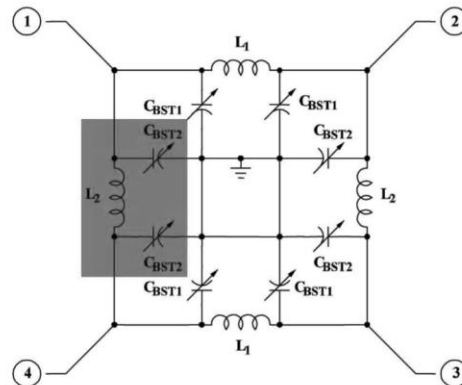


Figure 2.27 Tunable BST varactor hybrid coupler electrical schematic.

The inductance values are fixed with L1 and L2 were 2.9 and 4.15 nH respectively, with adjustable values of 2.1-2.6 pF for C1, and 1.5-5.8 pF for C2. One branch of the MMIC design is shown in Figure 2.28.

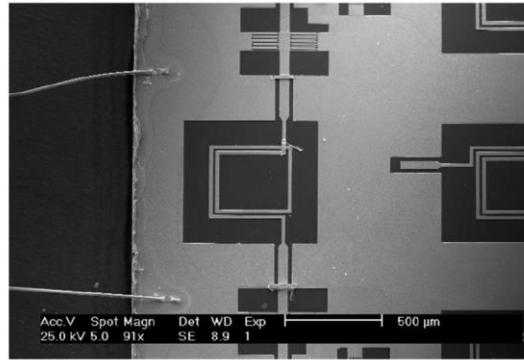


Figure 2.28 Tunable BST varactor tunable hybrid coupler layout.

In the same fashion as the printed circuit board case, the measured results of the BST coupler had a tunable range of 1710 MHz to 2170 MHz and are shown in Figure 2.29, Figure 2.30, and Figure 2.31. Compared with the PCB diode-varactor design, the MMIC BST design exhibited degraded performance in the through port, i.e.  $S_{21}$  of approximately -2.5 dB, with the quadrature phase performance of  $90^\circ \pm 5^\circ$ , which was comparable with the printed circuit board design.

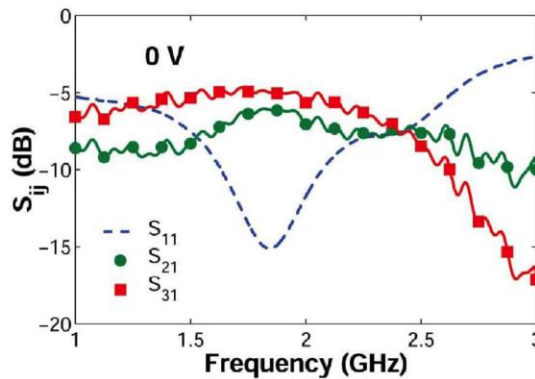


Figure 2.29 1.71 GHz BST varactor tunable hybrid coupler S-parameters.

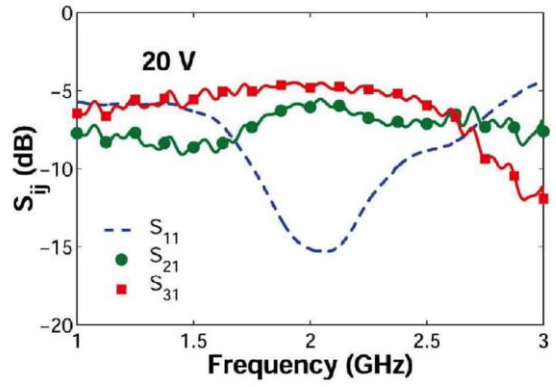


Figure 2.30 2.71 GHz BST tunable hybrid coupler S-parameters.

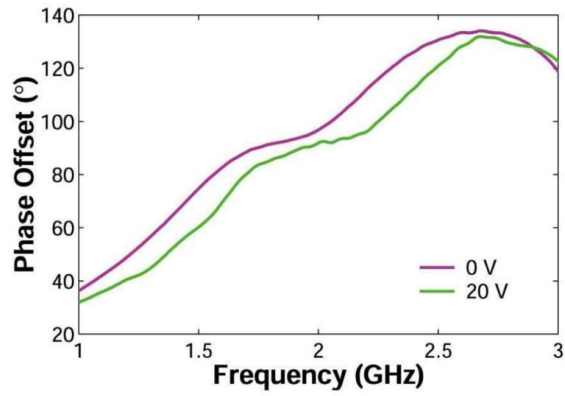


Figure 2.31 BST varactor tunable hybrid coupler phase response.

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## **CHAPTER 3 MMIC Lumped Elements**

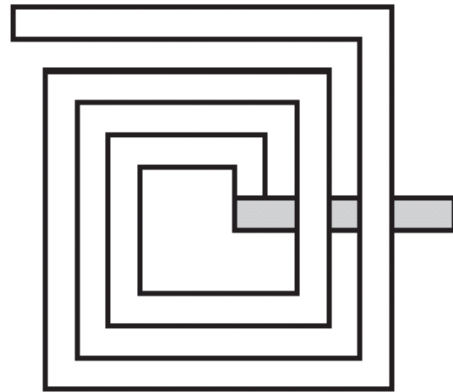
### **3.0 Introduction**

Lumped elements were initially developed for circuit component miniaturization used in RF electronics in the L and S frequency bands in the 1960s [3.1]. Passive integrated components primarily consist of printed planar inductors, and printed capacitors, both types of components can be successfully implemented in a distributed or lumped element form. Distributed components are generally based on quarter wavelength, or near quarter wavelength designs, and consequently occupy a great deal of surface area on an integrated circuit, especially at lower RF frequencies. Lumped element components, on the other hand whose electrical characteristics are not dependent on wavelength, can be used where surface area of the physical layout is a concern for the application. Planar spiral inductors typically suffer from low Q values due to substrate conductivity parasitics, but they are still often attractive based on their smaller size, lower cost and wider bandwidth [3.1], additionally inductors and capacitors for the purpose of microwave electronic circuits can be implemented via active components such as CMOS Transistors [3.2-3.3].

### **3.1 Lumped Element Inductors for RF and MMIC Circuits**

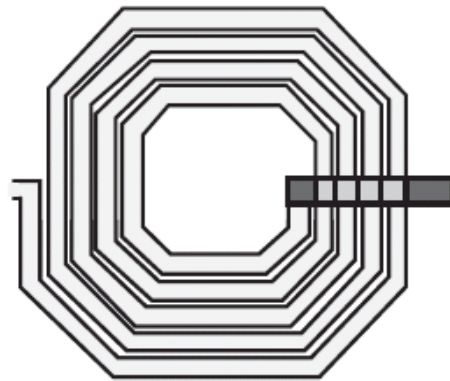
Due to their ease of fabrication, useful range up to 10 nH, and compact size [3.4], printed planar spiral inductors are commonly utilized in RF and Microwave circuits.

Many types of planar spiral inductor implementations are very common, two types of which, rectangular, and octagonal are shown in Figure 3.1 and Figure 3.2 respectively [3.1].



**Rectangular**

Figure 3.1 Rectangular printed inductor.



**Octagonal**

Figure 3.2 Octagonal printed inductor.

From the perspective of Series Resonant Frequency (SRF), ease of layout, and eddy current resistance, each inductor's geometry has its advantages and disadvantages, which are listed in Figure 3.3 [3.1].



Configuration	Advantage	Disadvantage
Meander line	Lower eddy current resistance	Lowest inductance and SRF
Rectangular	Easy layout	Lower SRF
Octagonal	Higher SRF	Difficult layout
Circular	Highest SRF	Difficult layout

Figure 3.3 Inductor geometry advantages/disadvantages.

One critical performance aspect where planar inductors typically suffer is in their Q values. A common and ubiquitous definition found in the literature for evaluating inductor Q from a two-port circuit perspective is (3-1) where  $y_{11}$  is one of four y-parameters of a two-port linear network [3.5].

$$Q = \frac{\text{Imag}\left(\frac{1}{y_{11}}\right)}{\text{Real}\left(\frac{1}{y_{11}}\right)} \quad (3-1)$$

Burghartz and Rejaei reported on the thorough analysis of the effects on inductor Q from different silicon IC spiral inductors design parameters, e.g. substrate doping, number of spiral turns, and conductor geometry [3.6]. The simulation and measurement results from one trial involved 57 inductors with inductance values of 2 nH, 5nH, and 10 nH are shown in Figure 3.4 and Figure 3.5.

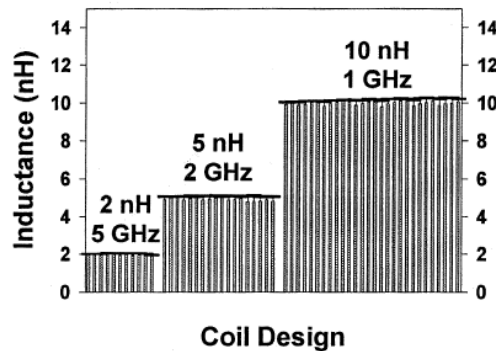


Figure 3.4 Simulated vs. measured inductor values.

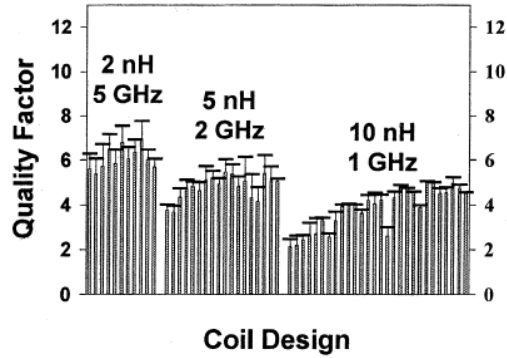


Figure 3.5 Simulated vs. measured inductor quality factors.

In this trial, the number of spirals, the spiral radii, and conductor geometries were varied to validate one of the co-author's models for predicting inductor Q. As can be easily observed, while the inductance values themselves were fairly constant, independent of the design parameters, the Q values ranged from approximately 6-8 for the 2 nH designs, 4-6 for the 5 nH designs, and 2.5 to 5 for the 10 nH designs, demonstrating the significance of properly choosing layout parameters when implementing spiral inductors in a silicon based circuit design.

### 3.1.1 Differential Spiral Inductors

As previously mentioned, planar spiral inductors, while an improvement over distributed element inductors in terms of size, they can still occupy a conservable amount of real estate on an RF integrated circuit. Furthermore; due to the typically low resistivity of Si and GaAs substrates, they still suffer from low quality factors [3.1]. Dinesh and Long reported on a more recent effort to address even further reduce the size of and improve the quality factor of spiral inductors is the development of the "differential spiral inductor" [3.7-3.8], in which a 50% increase in quality factor, with an accompanying 35% reduction in footprint size on a silicon integrated circuit.

Differential circuit designs are well known for the improved performance and common mode rejection ratio, which can be critical in receivers, etc... [3.4]. To the contrary, one disadvantage is the negative impact of the number of increased components from essentially doubling the components in each leg. Furthermore, as seen in Figure 3.6, spiral inductors that are spaced too close together suffer from the negative effects of opposing magnetic fields due the currents traveling in the opposite direction of nearby conductor paths, reducing the overall inductance, and effective quality factors when implemented.

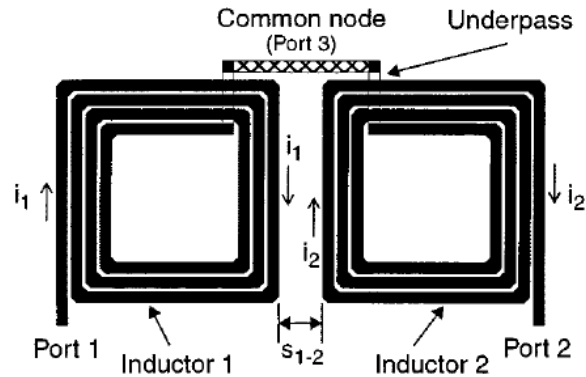


Figure 3.6 Side-by-side spiral inductors.

The proposed solution to this approach is to intertwine the two inductances as shown in Figure 3.7, the inductors are interleaved with underpasses utilizing vias, and then tied together at a central common node, which can be switch to the desired reference, i.e. circuit ground or the voltage supply. The differential inductor is then driven them with differential signals, i.e. signals that are  $180^\circ$  out of phase with each other. In that case, while the voltages are out of phase, the currents of adjacent conductors are in phase, which enhance each other instead of canceling each other, resulting in an increased Q, in a smaller surface area than in the single ended case [3.7].

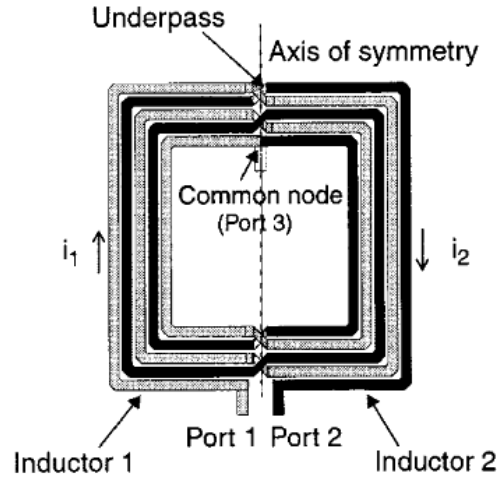


Figure 3.7 Differential spiral inductor.

An interesting note is that the evaluation of differential spiral inductors sometimes utilizes both the standard formula for extracting inductance from Y-parameters as stated in (3-2), and a less common estimation for a second inductance value which is expressed as in (3-3).

$$L_{21} = \frac{\text{imag}\left(\frac{-1}{Y_{21}}\right)}{\omega} \quad (3-2)$$

$$L_{11} = \frac{\text{imag}\left(\frac{1}{Y_{11}}\right)}{\omega} \quad (3-3).$$

These two calculations result in significantly different inductance values, but are nevertheless useful in evaluating the performance of differential inductance models [3.8].

### 3.1.2 Simulation of Three-Dimensional Solenoid Inductors

This research, based on the published results of a micro-machined three-dimensional air core inductor, is carried out primarily on the integrated circuit level via momentum simulation in Agilent ADS, without any integrated circuit prototype capability. Consequently, momentum simulations were 1st carried out to verify the results found in

the literature, and to establish a basis for further circuit design and simulation based on three-dimensional solenoid inductors. Lu, Pillans, Lee & Lee, reported on the fabrication and measurement of High Aspect ratio air core solenoid inductors using micro machine UV-LIGA technology [3.9]. The HFSS representations used in their simulations are shown in Figure 3.8 and Figure 3.9, which are 200  $\mu\text{m}$  tall by 200  $\mu\text{m}$  wide and 100  $\mu\text{m}$  tall by 100  $\mu\text{m}$  wide respectively.

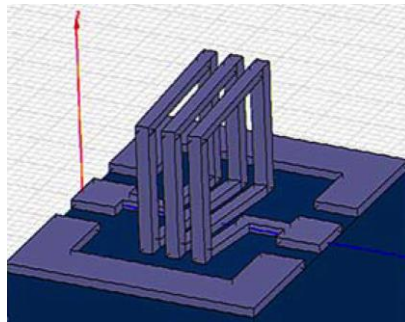


Figure 3.8 200  $\mu\text{m}$  x 100  $\mu\text{m}$  solenoidal inductor.

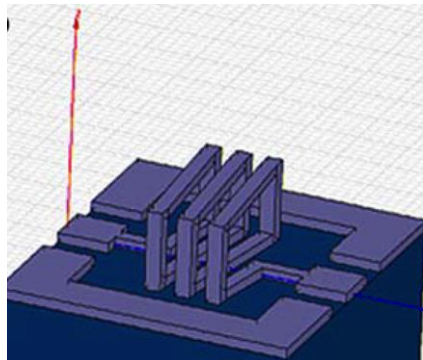


Figure 3.9 100  $\mu\text{m}$  by 100  $\mu\text{m}$  solenoidal inductor.

The published inductances and quality factors for the simulation of these structures are shown in Figure 3.10.

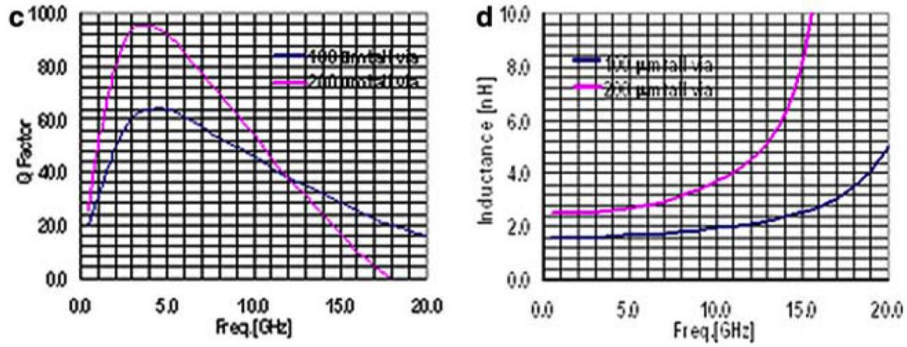


Figure 3.10 Published inductance and quality factors for 3D MEMS inductors.

As compared to the two-dimensional printed inductors described in Figure 3.1 and Figure 3.2, this three dimensional inductor topology lends itself more appropriately to “tapping” the inductor structure at different legs to form a quasi-tunable inductor. Based on the reported construction of these inductors, with an estimated  $20\ \mu\text{m} \times 20\ \mu\text{m}$  conductor size, similar inductors were simulated in Agilent ADS and are shown in Figure 3.11 and Figure 3.12.

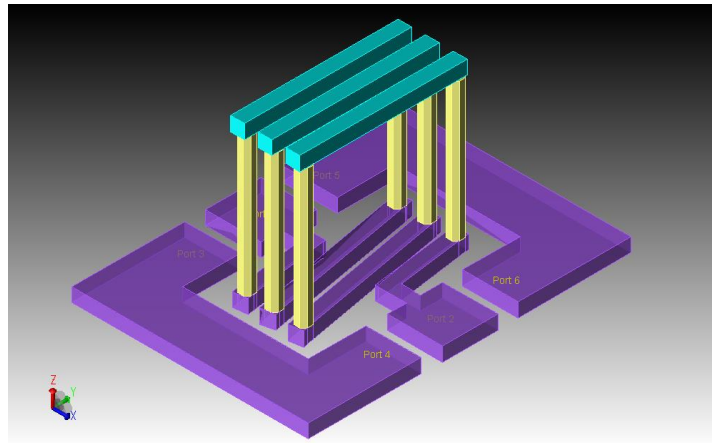


Figure 3.11 ADS simulation of  $200\ \mu\text{m} \times 200\ \mu\text{m}$  three-dimensional inductor.

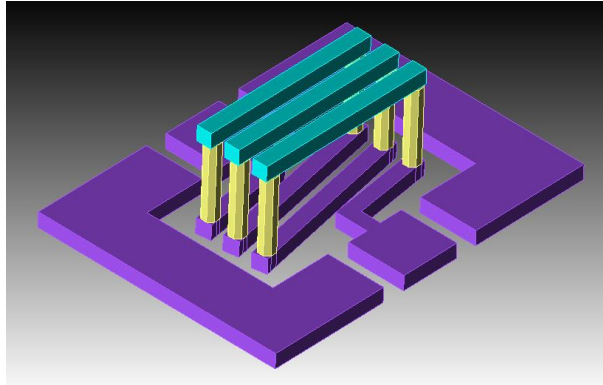


Figure 3.12 ADS simulation of 200  $\mu\text{m}$  x 100  $\mu\text{m}$  three-dimensional inductor.

To ensure the best simulation results possible for the research, both inductor simulations carried out in ADS were based on the same co-planar waveguide structures using GSG (ground-signal-ground) input-output ports. The inductance and quality factor values results for both the 200  $\mu\text{m}$  by 200  $\mu\text{m}$  and 100  $\mu\text{m}$  by 200  $\mu\text{m}$  inductors are shown in Figure 3.13.

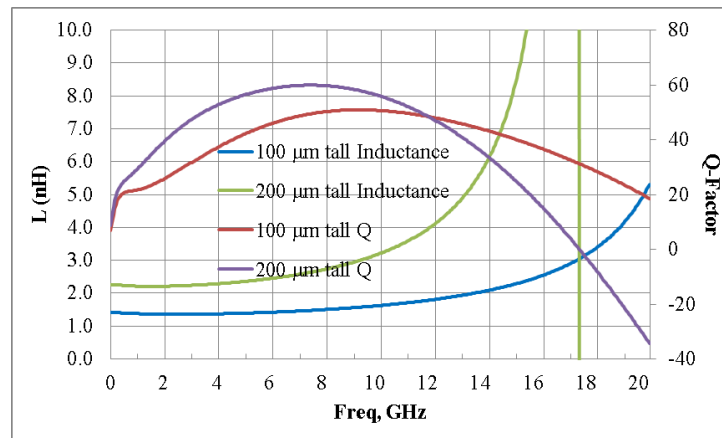


Figure 3.13 3 ADS simulated turn inductor inductance and Q vs. frequency.

As can be seen by comparing each of the 200  $\mu\text{m}$  and 100  $\mu\text{m}$  tall inductor simulations with the published measured data in Figure 3.14, the inductance and Q factors of both simulations are in good agreement.

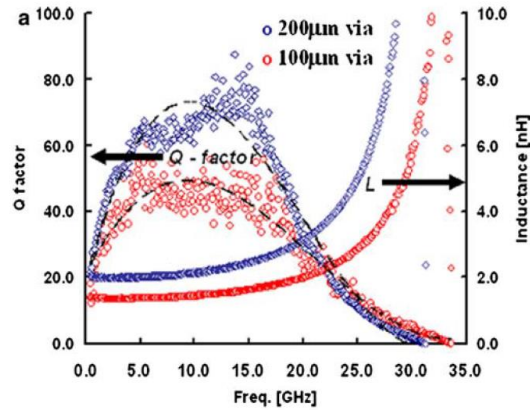


Figure 3.14 Published measured three-turn inductor data.

### 3.2 Lumped Element Capacitors

Capacitors have a wide range of use in RF and MMIC applications, ranging from use in band pass filters, to VCOs, phase shifters, etc..., they are typically characterized by relatively high Quality Factors. Numerous methods of constructing capacitors are available depending on the technology being used, e.g. VLSI CMOS, Silicon, GaAs, etc..., but are essentially classified as into three families, microstrip, interdigital, and metal-insulator-metal also known as MIM [3.1].

Capacitance from a lumped element point of view is generally based on the concept of the strength of an electric field between two conductive plates with area  $A$ , and separated by a dielectric as shown in Figure 3.15.

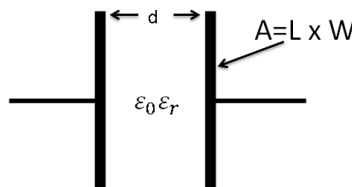


Figure 3.15 Ideal parallel plate capacitor.



The capacitance is typically states by the equation of (3-4) where  $\epsilon_0$  is the permativity of free space,  $\epsilon_r$  is the relative permativity of the dielectricic each with units of Farads per meter,  $A$  is the area of the plates that overlap each other, and  $d$  is the distance between the plates, each with units of meters.

$$C = \epsilon_0 \epsilon_r \frac{A}{d} \quad (3-4)$$

This capacitance is ideal in that it does not take into account the parasitic series inductance that is normally present at RF frequencies. For RF circuits an effective capacitance impedance for chip capacitors, which neglects the ESR is given by (3-5).

$$Z_C = -\frac{j}{\omega C} [1 - \omega^2 L_s C] \quad (3-5)$$

Alternatively, chip capacitor effective impedance can be expressed in terms of (3-6), (3-7), and (3-8).

$$Z_C = -\frac{j}{\omega C_e} \quad (3-6)$$

$$C_e = C [1 - \omega^2 L_s C]^{-1} = C \left[ 1 - \left( \frac{\omega}{\omega_s} \right)^2 \right]^{-1} \quad (3-7)$$

$$\omega_s = \frac{1}{\sqrt{L_s C}} \quad (3-8)$$

In these expressions,  $\omega_s$  is the series resonant frequency, and  $C_e$  is the effective capacitance, which for circuit design purposes, is usually higher than the nominal capacitance specified for the component [3.1].

### 3.2.1 A Proposal for a Tapped Series Parallel Plate Capacitor

MIM capacitors are typically used in in RF and Microwave circuits by forming two metal layers, and using some insulator material, e.g. silicon dioxide as the dielectric layer. The capacitance is then determined by adjusting the area of the plates and the dielectric layer

thickness if possible. It should be then possible to create quasi-tunable capacitors by tapping the capacitor layers in a successive fashion to create a series of capacitors based of three or more parallel plate structures utilizing vias to bring the metallization layer from each plate from to the top layer of the structure where some type of switching circuitry can be connected. A thorough search of the literature did not result in any proposals for a layout of this type of quasi-tunable capacitor, hence a unique proposal for such a structure is shown in Figure 3.16, and Figure 3.17.

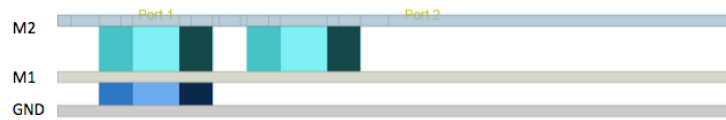


Figure 3.16 Side view of tapped series capacitor structure.

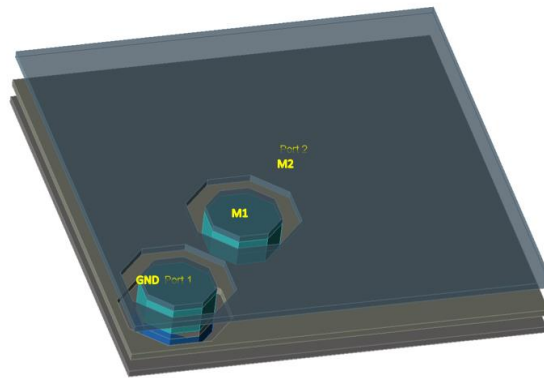


Figure 3.17 Angled three-dimensional view of tapped capacitor structure.

In this design, potentially three capacitors exist in this structure. These capacitors can be selected by using the GND to M1 plates, the GND to M2 plates, or the M1 to M2 plates. In this configuration, which utilizes hexagonal via holes with side lengths of  $T_1$ , and with area  $A_{VH}$  given by (3-9), and a generalized encompassing area  $A_G$  of width  $W$   $\mu\text{m}$  x length  $L$   $\mu\text{m}$  as stated in (3-10).

$$A_{VH} = \frac{3\sqrt{3}T_1^2}{2} \quad (3-9)$$

$$A_G = (W \times L) \quad (3-10)$$

The effective area of each capacitor metallization layer N, which is N layers away from the ground plane GND, is calculated by subtracting the relevant via hole areas from the generalized overall area  $M_{NA}$  of each layer as given by (3-11).

$$M_{NA} = A_G - A_{VH} = (W \times L) - N \frac{3\sqrt{3}T_1^2}{2} \quad (3-11)$$

Verification of this formula is shown in Figure 3.19, where the layout of Figure 3.17 was simulated based on the substrate stack up shown in Figure 3.18.

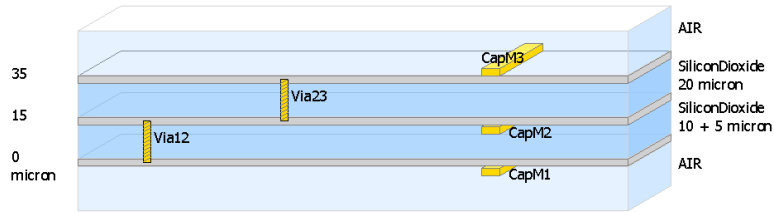


Figure 3.18 Tapped series capacitor stack up.

As can be seen in Figure 3.19, the values generated by the ADS momentum simulations are slightly higher, approximately 7%~12% than the theoretical values, but are in very good agreement, with relatively constant value across the frequency range of 0.5-5 GHz.

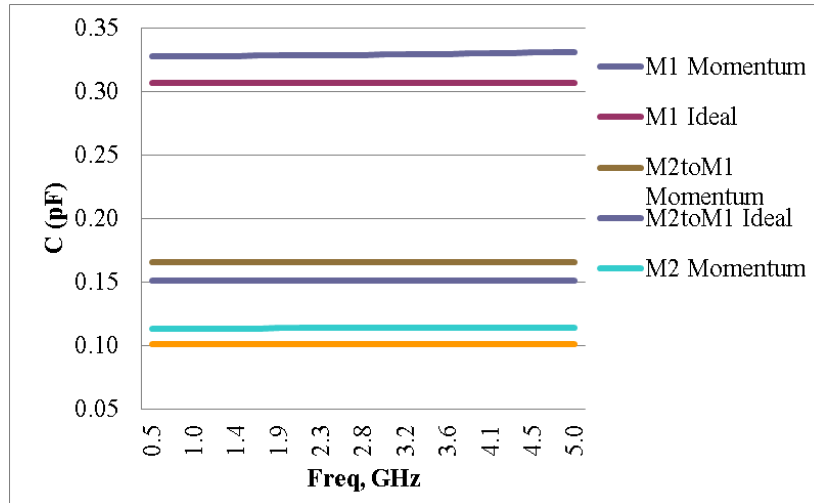


Figure 3.19 Tapped series capacitor calculation vs. momentum simulation.

### 3.3 Conclusion

A case study revealing the variation in spiral inductor Q fabricated in silicon integrated circuit technology demonstrates that inductor Q is heavily dependent on the component's design parameters, even while the target inductance is achieved.

The published measured results of a two three dimensional high aspect ratio solenoidal inductors have been verified through Agilent ADS Momentum simulations. The simulations agree well both in inductance and average Q measurements, demonstrating the simulation concept for future use in the concept study of this dissertation.

A proposal for a tapped series capacitor in the range of 0.1pF to 0.4 pF, based on IPD technology, has been simulated and described mathematically for potential use in the design of a tunable RF circuits. The simulation results match very well with the expected results based on standard capacitance equations for parallel plate series capacitors up to 5GHz.

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## Chapter 4 90° Hybrid Coupler Circuit Analysis

### 4.0 Introduction

As previously discussed, the 90° Hybrid Coupler is commonly found in the application of many RF and Microwave circuits and systems. While this is the case, the S-parameters of the hybrid coupler are usually derived based on the classic micro-strip circuit design, and not the lumped element circuit design. The microstrip coupler can be easily converted to lumped element form by transformation of each microstrip segment to equivalent PI-circuits by use of ABCD parameters [4.1]. Once converted from microstrip form into lumped element form, the mesh current methodology can be used to derive the ideal response of the hybrid coupler [4.2]. Furthermore; these derivations are typically ideal and do not take into account losses found in practical wireless communication applications, which in the lumped element equivalent coupler transformations are exacerbated by the low quality factors of the components. As is the case with any RF lumped element circuit design, e.g. a low pass filter, or band pass filter, the issue then becomes how to determine what inductor Q, or in some cases capacitor Q, is sufficient to meet the specified design criteria.

In this chapter, the performance analysis of the 90° Lumped Element Hybrid Coupler is extended beyond what's found in the literature, by the application of the mesh current methodology to develop an analytical approach to derive the S-parameters of the

hybrid coupler in terms of the coupler's inductor quality factors. With this approach the design engineer can reasonably predict the required inductor  $Q$  needed to meet a give hybrid coupler performance specification, assuming the  $S$ -parameters are known beforehand. This approach to lumped element circuit analysis, while developed for the even mode and odd mode circuits of the lumped element coupler are equally applicable to that of a generalized passive lumped element RF circuit.

#### 4.1 General Purpose Performance Analysis

The basic functionality of a directional coupler or power divider is to route or combine the power flow in an RF communications system [4.3-4.4], modern communications has led to the advent of frequency agile, or tunable couplers to meet the technological demands [4.5]. Consider Figure 4.1, the generalized block diagram of four port coupler, where the power flow from the input, port 1, is delivered to the through and coupled ports, ports 3 and 4 respectively, with an isolated port, port 2 that absorbs no power in an ideal circuit.

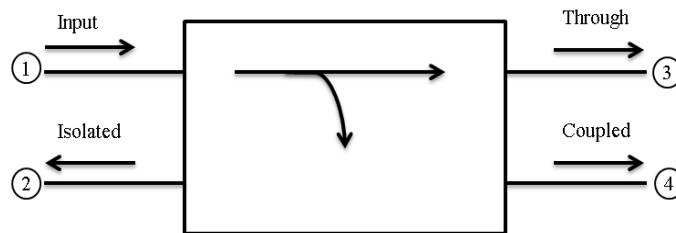


Figure 4.1 Directional coupler block diagram.

To describe the power flow in a directional coupler using  $S$ -parameters, the power delivered to the coupled port is described by the coupling factors  $\alpha$  and  $\beta$  between port 1, and 3, and between port 1 and port 4 respectively as shown in Figure 4.1, and are defined as given in (4-1) and (4-2) [4.1].



$$\alpha^2 = 1 - \beta^2 = |S_{13}|^2 \quad (4-1)$$

$$\beta^2 = |S_{14}|^2 \quad (4-2)$$

With these parameters in mind, the traditional single ended performance parameters of a directional coupler from a theoretical point of view are Coupling, Directivity, and Isolation, are given in equations (4-3) through (4-5) respectively [4.1] .

$$\text{Coupling} = C = 10 \log \frac{P_1}{P_4} = -20 \log \beta \text{ dB} \quad (4-3)$$

$$\text{Directivity} = D = 10 \log \frac{P_4}{P_2} = -20 \log \frac{\beta}{|S_{12}|} \text{ dB} \quad (4-4)$$

$$\text{Isolation} = I = 10 \log \frac{P_1}{P_2} = -20 \log(|S_{12}|) \text{ dB} \quad (4-5)$$

As previously stated, in an ideal coupler no power is delivered to the isolated port from the input port, i.e.  $S_{12}$  would be zero, meaning that the Directivity and Isolation would be infinite, and that the coupling factors  $\alpha$  and  $\beta$  would contain all of the input power [4.1].

RF power splitter and combiners typically have a number of other parameters that are used to describe their performance [4.3-4.7], some of which are commonly found in commercial data sheets. Consider the power transfer diagram of Figure 4.2, where the input power wave  $a_1$  is split into output power waves  $b_1$  and  $b_2$ . The balance loss  $\alpha$  describes the desired loss attributed to both channels equally, the balanced phase shift  $\varphi$  describes the desired forward phase shift between the input port and output ports, the amplitude imbalance  $\Delta$  describes the undesired imbalance between the magnitude of the two output waves, the phase imbalance  $\theta$  describes the undesired phase imbalance between the output power waves, and the desired phase offset  $\Phi$  describes the desired phase difference between the two output power waves [4.3].

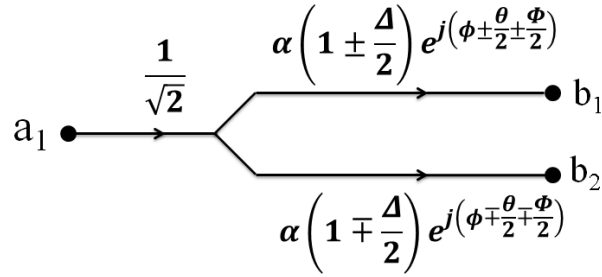


Figure 4.2 Splitter-combiner power flow block diagram.

## 4.2 Even and Odd Mode S-parameters as a Function of Inductor Q

The analytic relationship between inductor Q and the response of the 90° Lumped Element Hybrid coupler has not been found in the literature, and while modern electronic development environments provide relatively simple methods for simulating complicated circuits, they can be prohibitively expensive, and require training beyond that of the typical engineering curriculum. Therefore; it is both beneficial and desirable to develop this theory for both practical and theoretical use.

This section provides a short description of the theoretical relationships between inductor quality-factor, or inductor “Q” and the corresponding frequency response of the 90° Lumped Element Hybrid Coupler, see Appendix B for a detailed analysis. Analytic equations, and their associated inverse functions, that directly relate a hybrid coupler’s output to a given inductor Q-factor are presented. These equations are based on the concept of even mode and odd mode inductor Q which are used to describe the hybrid coupler’s corresponding even mode and odd mode output S-parameters.

The theoretical equations are then used in estimating the Common-Mode-Rejection-Ratio (CMMR) and Differential-Mode-Rejection-Ratio (DMRR) of the 90° Lumped Element Hybrid Coupler and compared to Momentum results from an ADS

simulation using more practical RFIC inductors as a function of their Q-factors to show the value of using the developed design equations from a practical point of view.

Consider the lumped element implementation of the  $90^\circ$  branch line coupler in Figure 4.3 with voltages V1 through V4.

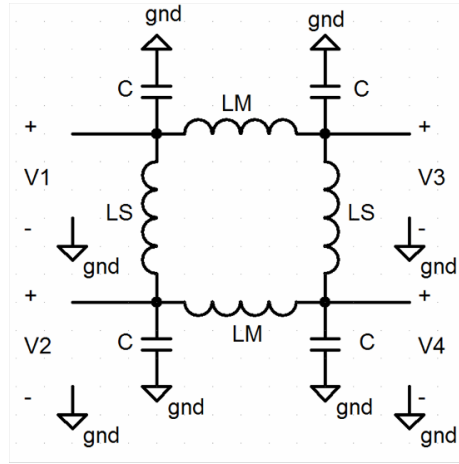


Figure 4.3 Lumped element  $90^\circ$  coupler.

In this analysis, Port 1 is the driven port, Port 2 is the isolated port with no output in an ideal circuit, Port 3 is the through port, and Port 4 is the coupled port with a  $90^\circ$  phase shift between ports 3 and 4. Mesh current analysis of the coupler in its standard form is very complicated, hence to simplify the analysis, the coupler is broken into even and odd mode circuits where the coupler outputs can be represented as in (4-6) and (4-7) [4.3].

$$S_{31} = \frac{1}{2}(S_{21e} + S_{21o}) \quad (4-6)$$

$$S_{41} = \frac{1}{2}(S_{21e} - S_{21o}) \quad (4-7)$$

To obtain the even and odd mode circuits, the normalized input at  $V_1$  of 1V is split into common mode voltages of  $V_1 = V_2 = 1/2$ . The same voltage applied to ports 1 and 2 means there is no current flow across the input side branch inductor  $L_S$ . The circuit also being symmetrical, and with a reciprocal response with ports 3 and 4 as the driven ports means that the output side branch inductor also experiences no current flow. Consequently both side branch inductors can be removed from the circuit since there is no current flow through them. This results in the simplified even mode circuit of Figure 4.4.

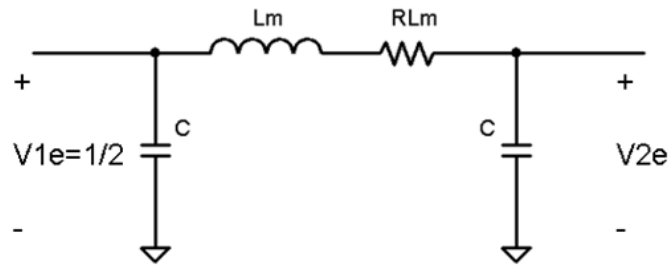


Figure 4.4 Simplified even mode lumped element  $90^\circ$  coupler.

It is important to notice that the parasitic series resistance of the main branch inductors  $R_{LM}$  has been included for completeness, and use in further analysis. Now consider the terminated even mode circuit of Figure 4.5, with mesh currents  $I_1 \sim I_3$  defined.

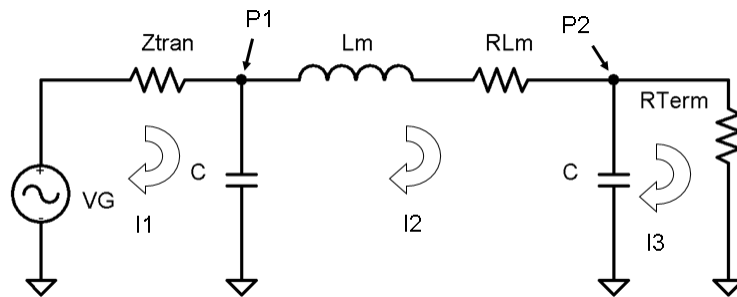


Figure 4.5 Even mode circuit mesh analysis.

Solving for the mesh currents results in the load current  $I_3$  (4-8).

$$I_3 = \frac{Z_C^2}{(1 + Z_C)(2Z_C + Z_L Z_C + Z_L)} \quad (4-8)$$

Assuming then that the even mode circuit is normalized, i.e.  $R_{\text{term}}=1$ , and  $Z_{\text{tran}}=1$ ,  $S_{21e}$  is simply  $I_3$  divided by one half the magnitude of the voltage source  $V_G$ , which means  $S_{21e}$  can be stated as in (4-9).

$$S_{21e} = \frac{2Z_C^2}{(1 + Z_C)(2Z_C + Z_L Z_C + Z_L)} \quad (4-9)$$

It can be shown that through the expression of (4-10) in terms of (4-11), that  $S_{21e}$  as a function of  $Q_e$  is given by (4-12), with the inverse function stated in (4-13).

$$Z_L = j\omega L_M + R_{LM} \quad (4-10)$$

$$Q \equiv \frac{\omega L}{R} \quad (4-11)$$

$$S_{21e} = \frac{2Z_C^2}{(1 + Z_C) \left( 2Z_C + \frac{1}{\sqrt{2}Q_e} + j \frac{1}{\sqrt{2}} (Z_C + 1) \right)} \quad (4-12)$$

$$Q_e = \frac{1}{\frac{2\sqrt{2}}{S_{21e}A} Z_C^2 - \frac{\sqrt{2}B}{A} - j} \quad (4-13)$$

For the odd mode configuration, voltage waves of opposite polarity and half the original magnitude create virtual grounds at the center points of the side branch inductors  $LS$ , which can be represented by two separate decoupled identical circuits as seen in Figure 4.6.

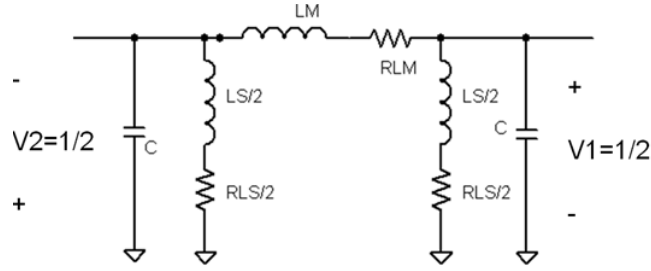


Figure 4.6 Simplified odd mode lumped element.

Consider the terminated odd mode mesh analysis circuit as shown in Figure 4.7 with a source generator of  $V_G=1V$ , an input transmission line impedance of  $Z_{tran}$ , and a load termination  $R_{term}$ .

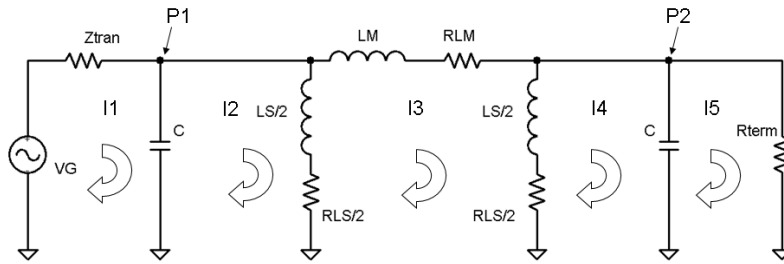


Figure 4.7 Odd mode mesh current analysis circuit.

Solving for the mesh currents results in the the load current  $I_5$  (4-14).

$$I_5 = \frac{Z_C^2 Z_{LS}^2}{(Z_C + Z_C Z_{LS} + Z_{LS})(Z_C Z_{LS} Z_{LM} + 2Z_C Z_{LS} + Z_C Z_{LM} + Z_{LS} Z_{LM})} \quad (4-14)$$

Expressing the odd mode circuit inductive impedances  $Z_{LS}$  and  $Z_{LM}$  in terms of  $Q_o$  as in (4-15) and (4-16) respectively and solving for  $S_{21o}$  in terms of results in (4-17).

$$Z_{LS} = \frac{j + Q_o^{-1}}{2} \quad (4-15)$$

$$Z_{LM} = \sqrt{2}Z_{LS} = \frac{\sqrt{2}(j + Q_o^{-1})}{2} = \frac{(j + Q_o^{-1})}{\sqrt{2}} \quad (4-16)$$

$$S_{21o}(Q_o) = \frac{Z_c^2}{\left(Z_c + \frac{j + Q_o^{-1}}{2}(Z_c + 1)\right) \left(Z_c \frac{1}{\sqrt{2}} + \frac{Z_c}{j + Q_o^{-1}}(2 + \sqrt{2}) + \frac{1}{\sqrt{2}}\right)} \quad (4-17)$$

Solving for  $Q_o$  results in a quadratic equation as expressed in (4-18) with the coefficients A, B, and C as stated in (4-19), (4-20), and (4-21) respectively.

$$S_{21o}(Q_o) = \text{Realroot}(AQ_o^2 + BQ_o + C) \quad (4-18)$$

$$A = S_{21o} \left( \left( \frac{-\sqrt{2}(a+1)^2}{4} \right) + (2 + \sqrt{2})a^2 + j \left( (1 + \sqrt{2})(a^2 + a) - \frac{a^2}{S_{21o}} \right) \right) \quad (4-19)$$

$$B = S_{21o} \left( (1 + \sqrt{2})(a^2 + a) - \frac{a^2}{S_{21o}} + \left( \frac{j2\sqrt{2}(a+1)^2}{4} \right) \right) \quad (4-20)$$

$$C = S_{21o} \left( \frac{-\sqrt{2}(a+1)^2}{4} \right) \quad (4-21)$$

$$a = Z_c = \frac{1}{j(1 + \sqrt{2})} \quad (4-22)$$

As with the even mode circuit, the assumption that the input impedance to the odd mode circuit matched the source transmission line impedance to simplify the evaluation of the  $S_{21o}$  S-parameters from the current vector produced by the mesh current analysis.

#### 4.2.1.1 Verification of $S_{21e}(Q_e)$ and $S_{21o}(Q_o)$

The design equations of (4-12) and (4-17) were derived assuming an ideal inductor  $Q_e$  and  $Q_o$ . the validity of (4-12) and (4-17) for all non-ideal Qs will now be demonstrated by the comparison of an ADS circuit simulations using the circuit of Figure 4.8 and (4-9) are

compared with the numerical calculations through MATLAB with Q values ranging from 1 to 32.

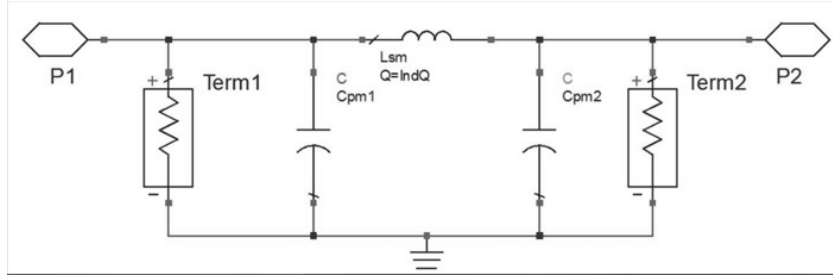


Figure 4.8 ADS equivalent even mode circuit.

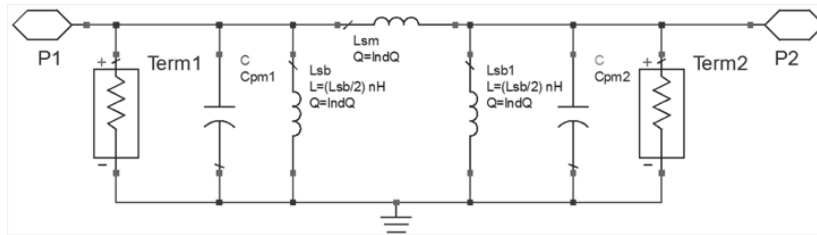


Figure 4.9 ADS Equivalent odd mode circuit.

The results, which agree very well at all Q values, for both the MATLAB analysis and the ADS simulation are shown in Table 4.1.

Table 4.1 Comparison of  $S_{210}(Q_0)$  ADS and Matlab Simulations

Q Odd	ADS Real	ADS Imag	Mat Real	Mat Imag		Q Even	ADS Real	ADS Imag	Mat Real	Mat Imag
1	0.04	-0.24	0.04	-0.24		1	-0.21	-0.21	-0.21	-0.21
2	0.19	-0.34	0.19	-0.34		2	-0.32	-0.32	-0.32	-0.32
4	0.37	-0.45	0.37	-0.45		4	-0.44	-0.44	-0.44	-0.44
8	0.51	-0.55	0.51	-0.55		8	-0.54	-0.54	-0.54	-0.54
16	0.61	-0.62	0.60	-0.62		16	-0.61	-0.61	-0.61	-0.61
32	0.66	-0.66	0.66	-0.66		32	-0.66	-0.66	-0.66	-0.66

### 4.3 Q to CMMR and DMRR Methodology for Design Goals

RF and Microwave engineers normally utilize standard magnitude imbalance, loss, and phase error specifications for evaluating a coupler's applicability to a circuit design. As



an alternative to the industry standard parameters, it is also possible to use mixed-mode S-parameters, i.e. Common-Mode Rejection Ratio (CMMR), and Differential Mode Rejection Ratio (DMRR) which express the performance of a differential circuit in terms of its ability to reject electrical noise found in RF integrated circuit applications [4.7]. The work in this chapter has established the analytical relationship between inductor Q and the S-parameters of the PI transformed 90° lumped element hybrid coupler, a natural extension of this concept is to investigate their application to the design of lumped element hybrid coupler. For that purpose, the design parameters for the PI transformed 90° lumped element hybrid coupler will be expanded based on even and odd mode S-parameters.

In the case of the 90° hybrid coupler, the CMRR is defined as the ratio of the difference between the output waves from ports 3 and 4, to the sum of the same output waves as stated in (4-23), with the DMRR being defined as the inverse of the CMRR as defined in (4-24) [4.8].

$$CMRR = \left| \frac{S_d}{S_c} \right| = \left| \frac{S_{31} - S_{41}}{S_{31} + S_{41}} \right| \quad (4-23)$$

$$DMRR = \frac{1}{CMRR} \quad (4-24)$$

Now recall that  $S_{31}$  and  $S_{41}$  can be represented as sums of even mode and odd mode coupler responses as restated in (4-25) and (4-26) [4.1].

$$S_{31} = \frac{1}{2}(S_{21e} + S_{21o}) \quad (4-25)$$

$$S_{41} = \frac{1}{2}(S_{21e} - S_{21o}) \quad (4-26)$$

Therefore; the numerator of (4-23) can be evaluated as in (4-27) with the result given in (4-28).

$$S_{31} - S_{41} = \frac{1}{2}(S_{21e} + S_{21o}) - \frac{1}{2}(S_{21e} - S_{21o}) \quad (4-27)$$

$$S_{21o} = S_{31} - S_{41} \quad (4-28)$$

Likewise, the denominator of (4-23) can be evaluated as in (4-29) with the result given in (4-30).

$$S_{31} + S_{41} = \frac{1}{2}(S_{21e} + S_{21o}) + \frac{1}{2}(S_{21e} - S_{21o}) \quad (4-29)$$

$$S_{21e} = S_{31} + S_{41} \quad (4-30)$$

With the results the CMRR and DMRR for the 90° hybrid coupler can be stated as in (4-31) and (4-32).

$$CMRR = \left| \frac{S_d}{S_c} \right| = \left| \frac{S_{21o}}{S_{21e}} \right| \quad (4-31)$$

$$DMRR = \left| \frac{S_c}{S_d} \right| = \left| \frac{S_{21e}}{S_{21o}} \right| \quad (4-32)$$

It is then seen, that either of the mixed-mode parameters can be directly expressed in terms of even mode and odd mode S-parameters.

With the ability to calculate the effects of inductor Q on  $S_{21e}$  and  $S_{21o}$  of the PI-transformed the 90° lumped element hybrid coupler, the ability to calculate the mixed-mode responses CMRR and DMRR, as well as the traditional S-parameter performance factors, e.g. magnitude imbalance and phase imbalance, from a given inductor Q-factor is straightforward. With an assumed circuit capacitance Q-factors of 300, Table 4.2

summarizes the resulting relationship between Inductor Q and the 90 Degree Lumped Element CMRR's , DMRR's, Magnitude Imbalance as the difference in magnitude of  $S_{31}$  and  $S_{41}$  with  $S_{31}$  as the reference, with Phase Imbalance as the phase difference from the nominal design phase difference of  $90^\circ$ .

Table 4.2 Mixed Mode Hybrid Coupler Performance vs. Inductor Q

Q	CMRR	DMRR	Mag Imb (dB)	Phase Imb (Deg)
4	0.932	1.072	0.898	-5.5
8	0.975	1.025	0.272	-1.75
16	0.992	1.008	0.075	-0.489
32	0.998	1.002	0.020	-0.129
64	0.999	1.000	0.005	-0.033

As further verification of the validity of this approach, a  $90^\circ$  lumped element hybrid coupler with a design frequency of 2.45 GHz was designed and simulated in Agilent ADS. Figure 4.10 is the schematic simulation circuit which utilizes momentum simulated spiral inductors with Q-factors of  $\sim 16$ , but with the capacitors implemented as more ideal schematic components with Q-factors of 300.

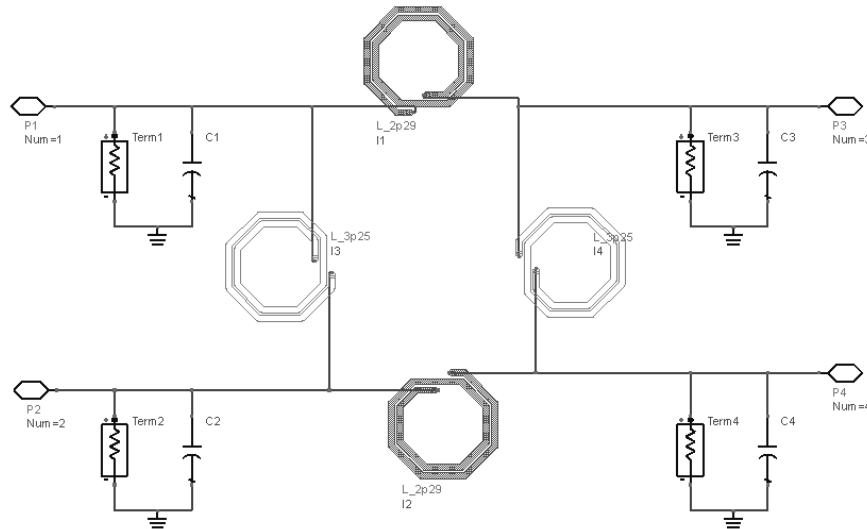


Figure 4.10 ADS simulation of  $90^\circ$  hybrid coupler with momentum simulated inductors.

As can be seen in Figure 4.11, Figure 4.12, and Figure 4.13, the mixed-mode comparisons, as well as the magnitude and phase imbalances comparisons, all agree very well with each other.

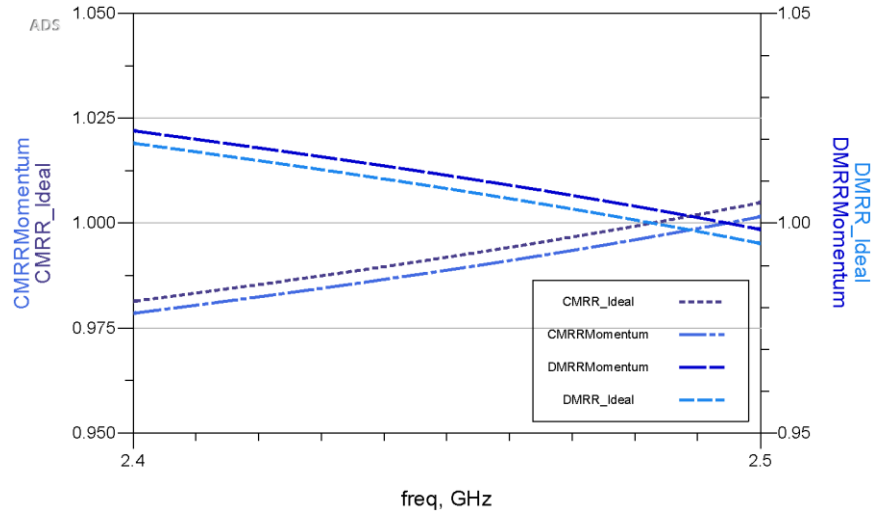


Figure 4.11 Mixed-Mode Comparison of ideal and momentum simulations.

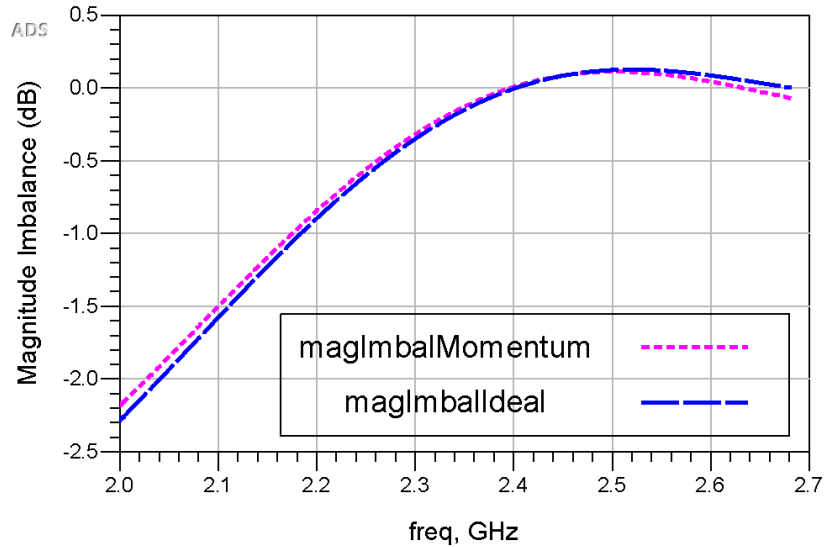


Figure 4.12 Magnitude imbalance comparison of numerical and momentum simulations.

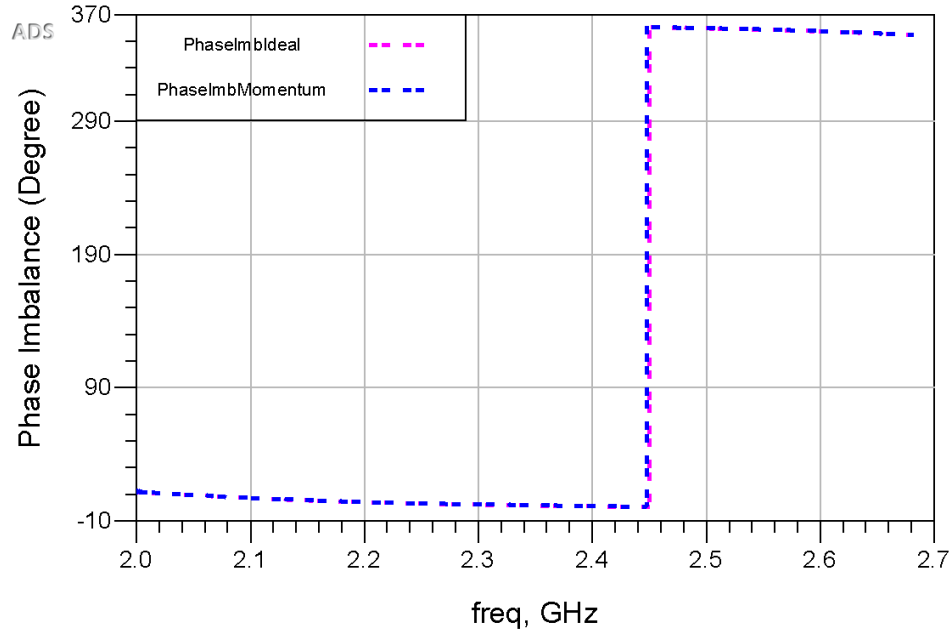


Figure 4.13 Phase imbalance comparison of numerical and momentum simulations.

#### 4.4 Conclusion

Equations expressing the even and odd mode coupler circuits Q values as functions of the desired even and odd mode coupler responses,  $Q_e(S_{21e})$  and  $Q_o(S_{21o})$  with ideal circuit capacitances were derived, along with inverse functions  $S_{21e}(Q_e)$  and  $S_{21e}(Q_e)$ . With these equations, the circuit designer has analytic equations to estimate the inductor component characteristics required to meet the specified design criteria of the coupler.

It has been shown that the mixed mode performance characteristics of the PI-transformed  $90^\circ$  lumped element hybrid coupler, i.e. common-mode rejection ratio and differential mode rejection ratio, can be directly expressed in terms of the coupler's even and odd mode inductor quality factors.

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# **CHAPTER 5 Design of a 2.0~3.0 GHz Lumped Element Quasi-Tunable Hybrid Coupler**

## **5.0 Introduction**

Integrated circuits for modern wireless communication devices are now available for use across a very wide frequency range. For example, the Skyworks 73102 Direct Quadrature Demodulator is designed for applications canvassing a frequency range of 400 MHz to 3900 MHz, [5.1]. A tunable quadrature hybrid coupler in the range of 1.6 to 2.3 GHz which utilized MEMS switched capacitor devices was recently published for use in Micro and Pico base-station phase-shifters [5.2]. Due to the effect of phase and amplitude imbalance resulting in leakage of undesired signals into the desired frequency channel, causing a degradation of SNR [5.3], the performance of modulation techniques such as Orthogonal Frequency Division Multiplexing (OFDM) are sensitive to I/Q signal imbalances [5.4]. Work has been done to compensate for the imbalance by means of Digital Signal Processing [5.5], but this requires active circuitry or extra DSP capability in the front-end receiver, leading to the possibility that minimizing quadrature coupler phase and imbalance distortion lessens the burden on error compensation schemes, with an optimized improvement in SNR. Another interesting aspect of quadrature coupler design is what level of magnitude and phase imbalance are acceptable and still provide sufficient SNR for a given desired data rate in an OFDM system. Li, and Chuang

provided a detailed theoretical analysis of the effects of I/Q signal distortion on the SNR degradation for Direct Conversion Receivers, estimating that  $5^\circ$  of phase imbalance, and 0.5 dB of magnitude imbalance are limits when a 54-Mbps data rate is desired [5.6]. This broad range of available frequencies in modern wireless communication transceivers along with their heavy dependence on accurate I/Q signals for reliable communication make the investigation of the benefits of MEMS technology, both switching and passive component fabrication, worth investigating from a performance point of view.

The main motivation of this research was to investigate the performance benefits of implementing a quasi-tunable lumped element hybrid coupler in the range of 2.0 ~ 3.0 GHz using standard IPD technology combined with three-dimensional solenoidal inductors [5.7], and to compare it with the same design using the S-parameters of an off-the-shelf PIN diode switched coupler. Furthermore; to broaden the evaluation of the research, an additional, but not necessary, goal of the design is to achieve better performance than an off-the-shelf hybrid coupler using an integrated circuit design across the frequency range of the coupler.

As previously discussed in Chapter 2, there have been numerous variations of quasi-tunable hybrid couplers, most of which are based on variable capacitances utilizing fixed inductances, or transmission lines. The approach of this research is novel in that it is based on a tapped MEMS three-dimensional inductor structures for the main branch and side branch inductances, and additionally utilizing two unique tapped capacitor designs, one utilizing a switched signal tapped capacitor, and one utilizing a switched ground tapped capacitor. The central concept of this design approach to a quasi-tunable coupler is based on the PI-transformed version of the lumped element hybrid coupler



presented and discussed in Chapter 4, and shown again in Figure 5.1, where each transmission line of the standard branch line coupler is replaced with lumped element PI circuits, for simplicity, the resulting parallel capacitances are shown as a single capacitance.

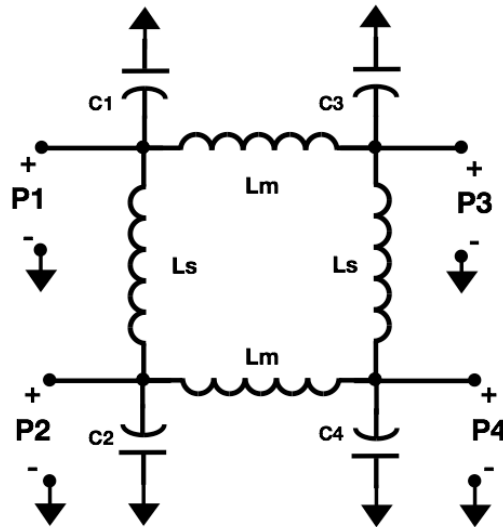


Figure 5.1 Lumped element hybrid coupler.

In this design, inductors  $L_m$  are the “main-branch” inductors, while inductors  $L_s$  are the “side-branch” inductors, and capacitors  $C_1$ ~ $C_4$  are the total corner capacitances  $C_i$ . In this form, the coupler has a center frequency based on the fixed inductor capacitor values used by the designer. To extend the circuit and make it tunable, each inductor is matched with the corner capacitor at its output to form an “inductor-capacitor” bank as shown in Figure 5.2. The electronic circuit design used in this instance is based on the tapped-capacitor presented in Chapter 3, but additionally paired with a quasi-tunable inductor to form a switchable inductor-capacitor bank. In general, the number of inductor-capacitor taps depends on the number of channels required to canvas the specified frequency range and still meet the design specifications, e.g. isolation, return

Loss, phase balance, etc.... As an example, consider the tapped inductor-capacitor bank shown in Figure 5.2, using five capacitance values and five inductance values. The input is at  $V_{in}$ , the output taken at  $V_{out}$ , with a common signal bus connected between switches Sw1 through Sw5 for the desired inductance, and Sw6 through Sw10 for the desired capacitance.

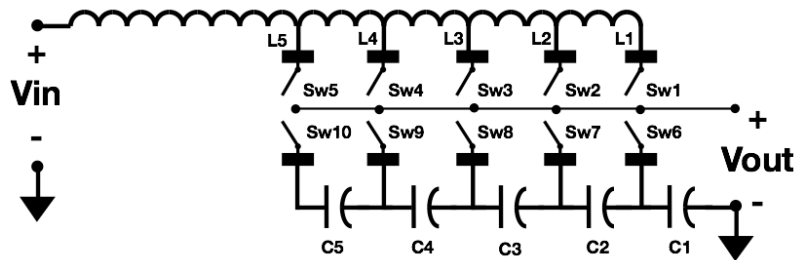


Figure 5.2 Signal switched hybrid coupler tunable L/C bank circuit.

One of the more difficult challenges was to create switchable inductances and switchable capacitances using minimal MEMS switch topology. The proposed design was reached through an iterative process where each lump element inductor was designed in a stand-alone ideal configuration. After the initial design was reached, these “prototype” inductors were combined into a Ground-Signal-Ground (GSG) input/output configuration for the purpose of including the cross-talk effects of a combined layout that results when all components are electrically connected together in the close proximity of an integrated circuit design.

A PI-transformed  $90^\circ$  lumped element hybrid coupler that operates from 2-3 GHz requires capacitances values in the 2.6 pF to 3.6 pF range for optimized performance with regards to all parameters, i.e. phase-imbalance, magnitude-imbalance, magnitude-loss, etc... . As discussed in Chapter 3, variable capacitances can be produced in a number of

ways, e.g. Varactor Diodes, BST Tunable Interdigital Capacitors, and MEMS switched capacitor banks, but for this research a novel tapped capacitor structure based on the concept shown in Figure 3.17 is utilized.

For the initial design, a prototype-tapped capacitor was developed using a common ground at the bottom of the substrate with the signal taps connected to the required metal layers in the structure by means of vias. As discussed in Chapter 3, each adjacent pair of inner metal layers of the substrate forms a metal-insulator-metal capacitor (MIM). When viewed from top to bottom it's easy to understand that a layout stack-up with  $N$  plates has at minimum an  $N-1$  set of series capacitors. The resulting series capacitance structure can then be tapped by bringing each layer to the top layer of the integrated circuit layout to the desired connection points. After including all of the components into a single design, the capacitances were re-tuned for optimal coupler performance at the desired selected frequency to compensate for distortion due to cross coupling between components.

The performance of the initial layout compared above 2.5 GHz to the ideal circuit simulation was not as expected. Analysis of the layout led to two more designs, one with a layout where the target capacitances were tuned to the output ports of the coupler, and one with the capacitor taps switched from the signal side to the ground side of the series capacitor structure with a single signal output connected at the output port of each branch. The ground switched tapped capacitor design provided the best overall performance, both in amplitude loss, amplitude imbalance, and phase distortion.

As a performance baseline for the coupler design, the Anaren's Ultra Low Profile 0805 3-dB, 90° Hybrid Coupler, part number C2327J500A00, an off the shelf coupler surface mount product in the ISM band was chosen.

Table 5.1 Anaren C2327J500A00 Electrical Specification

Parameter	Min	Typ	Max	Unit
Frequency	2300		2700	MHz
Port Impedance		50		$\Omega$
Return Loss	15	18		dB
Isolation	18	22		dB
Amplitude Balance		.1	.9	dB
Phase Balance Relative to 90 deg		4	8	Degrees

## 5.1 Influence of Inductor Q-Factors on Channel Selection

With the target design goals in mind, there are several questions that must be answered at the outset of the design process:

- What is the range of inductances required for the desired frequency range?
- What is the range of capacitances required for the desired frequency range?
- What are the effects of inductor quality factors on circuit performance?
- What are the effects of capacitor quality factors on circuit performance?

To determine what value of inductor Q, neglecting all other losses, would be sufficient to approximate the Anaren Coupler's  $S_{11}$  and  $S_{21}$ , consider the parameters shown in Table 5.1, then based on the values of the Anaren Coupler in Table 5.1, a minimum inductor Q of 15 should be sufficient.

Table 5.2 Coupler Response as a function of Inductor Q

Inductor Q	5	10	15	20	25	30	60	150
S <sub>11</sub> (dB)	-13.6	-18.7	-22.9	-24.2	-26	-27.5	-33.4	-41.3
S <sub>21</sub> (dB)	-17.2	-20.6	-23.2	-25.2	-26.8	-28.2	-33.6	-41.4
S <sub>31</sub> (dB)	-6.4	-4.9	-4.3	-4.0	-3.8	-3.7	-3.5	-3.15
S <sub>41</sub> (dB)	-7.0	-5.1	-4.4	-4.0	-3.8	-3.7	-3.6	-3.15
Phase Error (Degree)	-3.0	-1.0	0.5	0.3	0.19	0.13	0.03	0.0

Note that dB is calculated as given in (5-1).

$$dB = 20\text{Log}_{10}(x) \tag{5-1}$$

Assume  $Z_0 = 50 \Omega$ , then the main branch inductance  $L_M$  ranges from 2.814 nH to 1.876 nH, and the side branch inductance  $L_S$  ranges from 3.979 nH to 2.563 nH, and  $C_T$ , the total inductance seen at each coupler port, ranges from 2.56 pF to 3.843 pF, where  $C_T = C_S + C_M$ , the results being summarized in Table 5.3.

Table 5.3 Lumped Element Hybrid Coupler Component Ranges

Component\Frequency	2GHz	3GHz
LM (nH)	2.814	1.876
LS (nH)	3.979	2.653
CS (pF)	2.251	1.50
CM (pF)	1.592	1.06
CT (pF)	3.843	2.56

## 5.2 Tapped Inductor Initial Design

Based on the inductor values and associated quality factors needed to meet the design criteria, Agilent ADS was used to design and verify the initial layout of the three-dimensional solenoidal inductors. The basic inductor layout was designed with a 47 micron thickness between the upper and lower traces of the inductor with an air core and a glass substrate. To be comparable to the layout to that of the design in Figure 3.9, the top and bottom conductors were designed with 20 micron thickness copper metallization and a conductivity of  $\sigma = 5.8 \times 10^7 \text{ S/m}$  as shown in Figure 5.3.

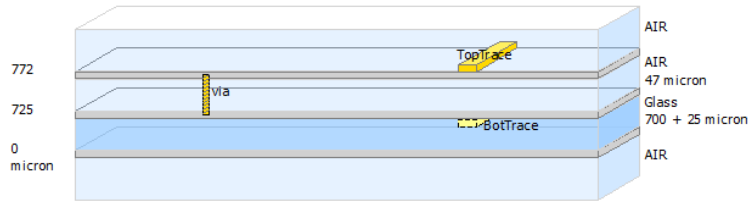


Figure 5.3 Three-dimensional solenoidal inductor layer stack up.

The inductor physical parameters were based on 20 micron trace width and spacing with associated hexagonal vias and are shown in Figure 5.4.

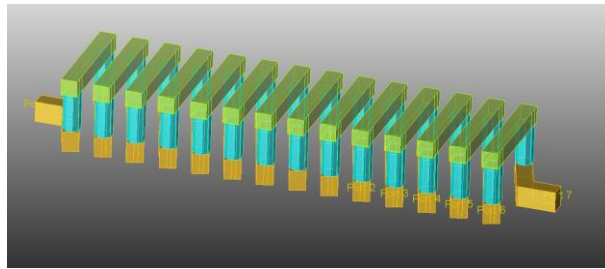


Figure 5.4 3D view of main branch solenoidal inductor.

To determine what level of inductance was available per branch leg with the given dimensions, ADS momentum simulations were carried out to model the S-parameters for the structure's input and output ports at each end, as well as at five successive taps. The S-parameter results from the momentum simulations are then converted to Y-Parameters with the corresponding inductances and quality factors calculated as in (5-2) and (5-3), the results are shown in Figure 5.5.

$$L = \frac{1}{2\pi f * \text{Imag} \left( \frac{-1}{y_{11}} \right)} \quad (5-2)$$

$$Q = \frac{\text{Imag} \left( \frac{1}{y_{11}} \right)}{\text{Real} \left( \frac{1}{y_{11}} \right)} \quad (5-3)$$

As can be seen in the inductance values change approximately 0.2 nH per branch leg, with decreasing inductance over the simulated frequency range of 2.0 GHz to 3.0 GHz. Furthermore; the quality factors which were approximately the same at each tap, vary significantly over the desired frequency range from approximately 23 at 2.0 GHz to 27 at 3.0 GHz.

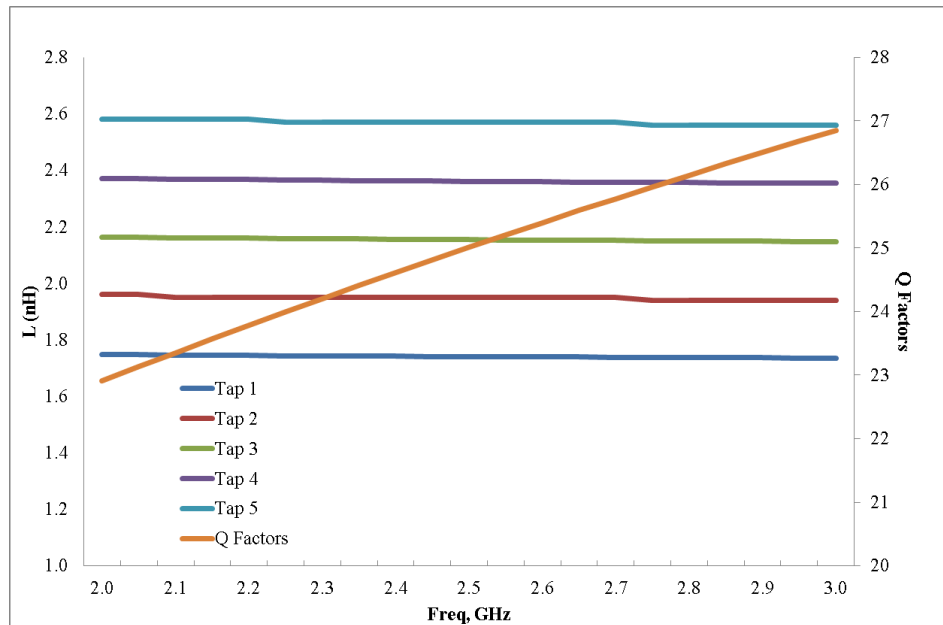


Figure 5.5 3D main branch inductor value vs. branch leg.

Next, the side branch inductor layout was created in a similar fashion to the main branch inductor, and once again momentum simulations were carried out to estimate the S-parameters for the structure for ports at each end of the structure as well as five successive taps, ports two through six as shown in Figure 5.6.

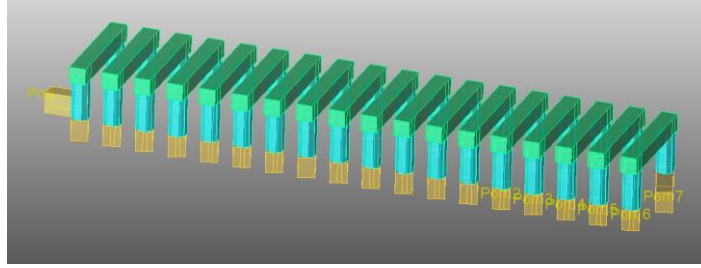


Figure 5.6 3D view of side branch solenoidal inductor.

As with the main branch inductance, the resulting momentum simulation was used in an ADS schematic for estimating the inductance and quality factors of each tap, and are shown in Figure 5.7. As can be seen the taps at about 0.2 nH per tap, with Q values that again increase as a function of frequency in the range of 23 to 27.

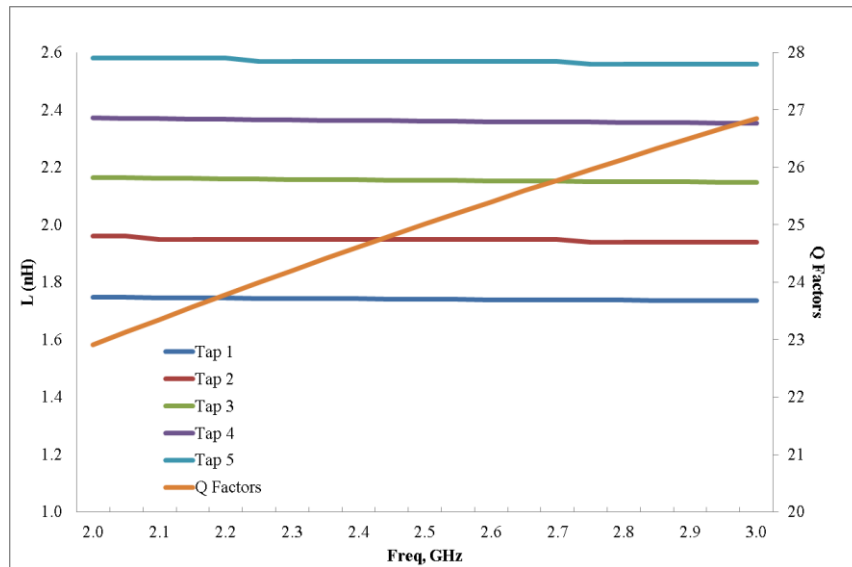


Figure 5.7 3D side branch inductor value vs. branch leg.

### 5.2.1 Determination of Coupler Channel Center Frequencies

The objective of the design is to approximate the Anaren Coupler's Isolation and Return Loss across the frequency band of 2.0 GHz to 3.0 GHz. Understanding that the inductor quality factors are not constant across the frequency range, and that the effects of



switching from a low distortion, i.e. low contact resistance MEMS switch will also alter the frequency response, simulations with non-ideal inductor Q-factors as well as an off the shelf diode's S-parameters were carried out to account for further frequency response distortion as a function of center frequencies. With the realizable tap-to-tap inductance deltas of approximately 0.2 nH, it is natural then to assume center frequencies of 2.1, 2.3, 2.5, 2.7, and 2.9 GHz. The resulting inductances and capacitances for these channel center frequencies are given in Table 5.4.

Table 5.4 Initial Coupler Center Frequencies and Component Values

Freq, GHz	2.1	2.3	2.5	2.7	2.9
L <sub>sM</sub> (nH)	2.67	2.45	2.25	2.08	1.94
L <sub>sB</sub> (nH)	3.79	3.46	3.18	2.94	2.74
C <sub>T</sub> (pF)	3.66	3.34	3.07	2.85	2.65

It is understood that forward-biased switched frequency response of PIN diodes will introduce some losses, and non-linear frequency distortion. As a worst case condition, the effects of a diode switch were also included in a final simulation to optimize the center frequencies while taking into account any frequency response distortion based on momentum simulated inductors with capacitor Qs of 300 as shown in Figure 5.8.

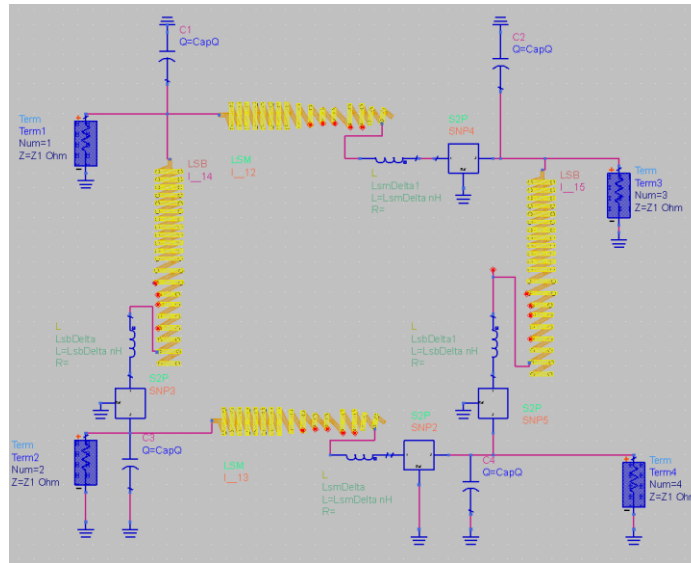


Figure 5.8 Momentum coupler design schematic with non-ideal component Q.

Due to the frequency distortion, primarily at the 2.0 to 2.4 GHz range, of the worst case forward bias current of 8mA, the center frequencies of the first two channels had to be slightly adjusted to meet the insertion and return loss goals across the entire design frequency range. The optimized frequencies as well as the new component values are given in Table 5.5.

Table 5.5 Optimized Coupler Center Frequencies and Component Values

Freq (GHz)	2.123	2.227	2.5	2.7	2.9
LsM (nH)	2.3	2.42	2.25	2.08	1.94
LsB (nH)	3.82	3.47	3.18	2.94	2.74
CT (pF)	3.69	3.35	3.07	2.85	2.65

As can be seen in Figure 5.9, the optimized design maintains an insertion loss below -15 dB worst case, as well as keeping the isolation below -18dB across the specified frequency range.

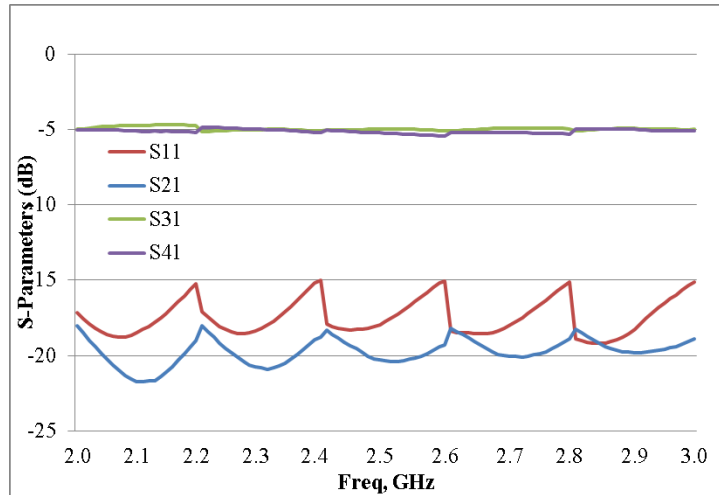


Figure 5.9 2-3 GHz diode switched coupler response with momentum simulated inductors.

Compared with the Anaren coupler, the maximum magnitude imbalance of 0.4 dB and phase imbalance of  $4.7^\circ$ , or  $\pm 2.35^\circ$ , are an improvement over the 0.8 dB magnitude imbalance and  $9^\circ$  phase imbalance reported for the off the shelf design.

### 5.3 Tapped Capacitor Initial Design

As shown in Table 5.3, the range of capacitance needed for a 2.0 GHz to 3.0 GHz coupler is from 2.56 pF to 3.84 pF. Recalling that adding plates in series causes each successive capacitance to decrease according to the well-known series capacitance equation, then a tapped capacitor can be created by extending vias from each metallization layer to a switching topology that places successive metal/dielectric layers in series with each other.

As verification of the concept's feasibility, a tapped capacitor was designed with overall surface dimensions of 625  $\mu\text{m}$  by 625  $\mu\text{m}$  as shown in Figure 5.10. This area was selected to allow for 50  $\mu\text{m}$  wide hexagonal via pads, with 75  $\mu\text{m}$  wide via holes to accommodate an undetermined switching topology. In this design, metallization layer M1 is connected to Port1, layer M2 to Port2, layer M3 to Port3, and layer M4 to Port4.

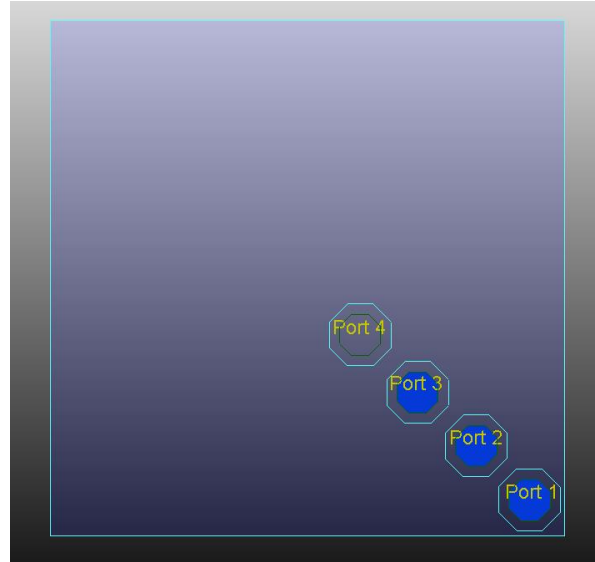


Figure 5.10 Tapped capacitor layout top view.

As mentioned in Chapter 3, the surface area of each layer is dependent on the required number of via holes necessary to bring the layer beneath it to the top layer, that is Layer M1 has no via holes, layer M2 has 1 Via hole, layer M3 has 2, so each layer MX has X-1 via holes and hence a reduced surface area available for a given series capacitance. For an initial evaluation of the coupler performance based on this structure design, the capacitances required for 2.13, 2.23, and 2.5 GHz were evaluated via Y-parameters as shown in Figure 5.11, and created by adjusting the dielectric thickness between the Layers, M1 through M4 as shown in Figure 5.12

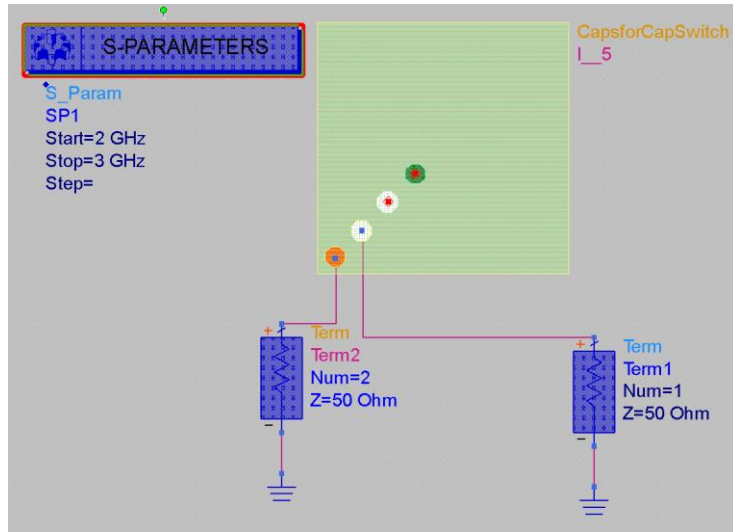


Figure 5.11 Evaluation schematic for layers M1 to M2.

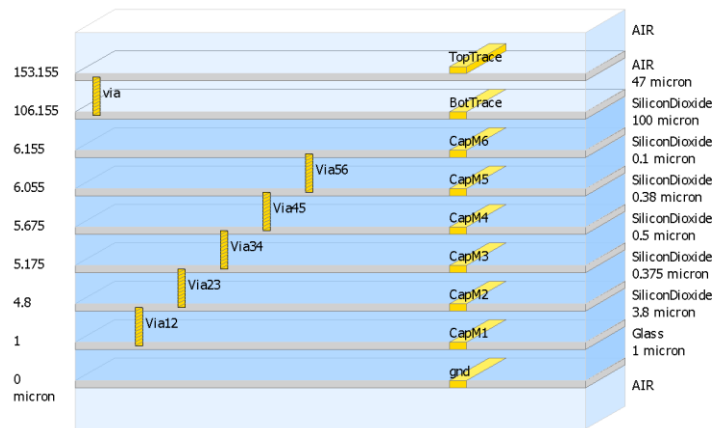


Figure 5.12 Base capacitor substrate stack up.

The corresponding capacitance value and the associated Q factors for the 2.13 GHz design are shown in Figure 5.13, each capacitor value and associated Q for all 5 channels are given in Table 5.6. Each capacitor had approximately 0.15 pF variation across the frequency range of interest, with quality factors ranging from 556 to 744, thus demonstrating their suitability for this application.

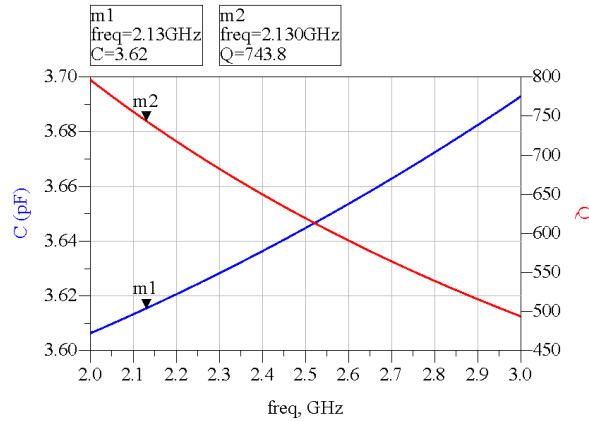


Figure 5.13 Capacitance and Q values for layers M1 to M2.

Table 5.6 Initial Tapped Capacitances vs. Q

Center Frequency	C (pF)	Q
2.13	3.62	744
2.23	3.34	722
2.5	3.05	568

## 5.4 Effects of Switching Technology

The goal of this section is to evaluate the performance of switching topology on the proposed lumped element hybrid coupler utilizing DC-contact MEMS switches compared to that of RF PIN diodes. For this purpose, an off the shelf diode, and a theoretical MEMS switch modeled as DC-contact switch will be used for performance analysis via simulation of each component type, with a final comparison of the results of each switching topology.

### 5.4.1 Mems Switching Network

MEMS switching involves two basic type of switches, the DC-Contact switch, or a capacitive coupled switch. Inserting a series capacitance in line with the selected inductor taps would alter the behavior, so the DC contact MEMS switch was chosen for evaluation purposes of this research. For the series DC-Contact MEMS switch there are

three principle parasitic effects, series contact resistance, series inductance, and parasitic capacitance to ground. Recognizing that the series inductance and parallel capacitance can be absorbed into each of the tapped inductor capacitors design respectively, then their effects needs not be accounted for, leaving only the series resistance as the key characteristic that impacts the performance of the coupler.

Typical off the shelf MEMS switches have DC-contact resistances in the range of  $0.5\sim 2\ \Omega$  [5.8] with as low as  $275\ \text{m}\Omega$  reported [5.9]. The question then for the design of a quasi-tunable lumped element hybrid coupler is what level of contact resistance has significant effect on coupler performance. For the purpose of evaluating the MEMS contact switch consider the inductor-capacitor bank of Figure 5.14. As before, the inductor-capacitor bank is configured for a center frequency of 2.5 GHz, but with the additional variable resistances R5 and R6 included to simulate the series resistance of a MEMS DC-contact switch.

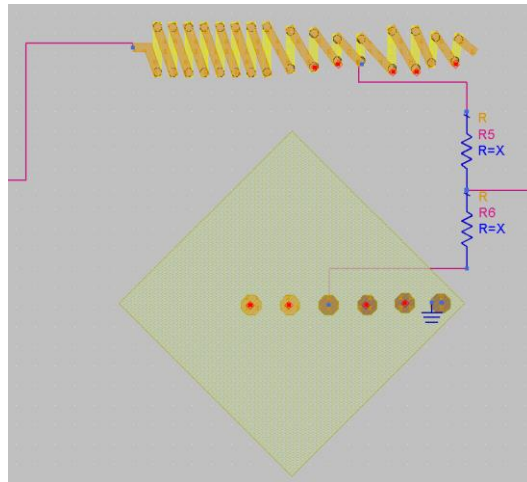


Figure 5.14 Main inductor-capacitor bank 2.5 GHz.

The total 2.5 GHz MEMS Switched Hybrid Coupler ADS schematic evaluation circuit is shown in Figure 5.15 where all of the parasitic resistances R1~R8 are shown.

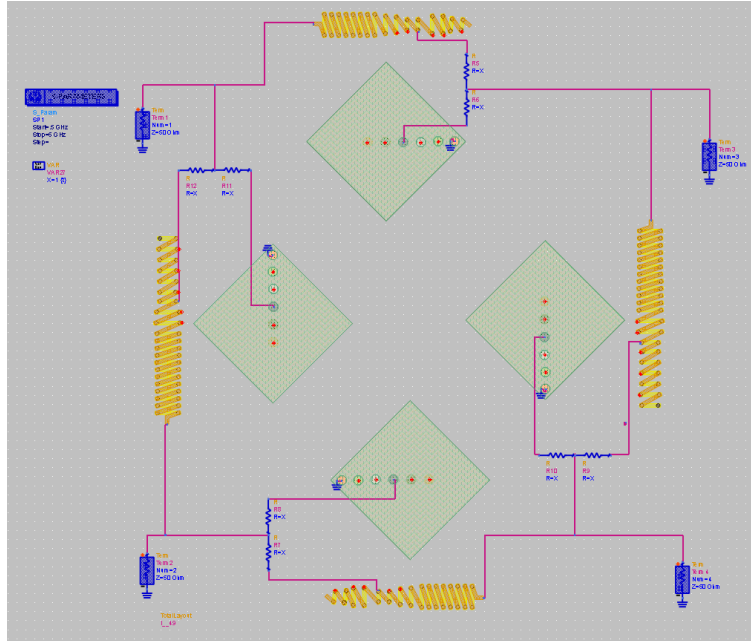


Figure 5.15 Total MEMS switched 2.5 GHz hybrid coupler.

For the purpose of evaluating the effects of contact resistance on coupler performance, simulations with parasitic contact resistances of 0  $\Omega$ , 0.25  $\Omega$ , and 1.0  $\Omega$  were performed. The ideal case of 0  $\Omega$  was to establish a baseline performance for the overall coupler, while 0.25  $\Omega$  being the state of the art, and 1.0  $\Omega$  representing the lower resistance of most published switches. The magnitude and phase response of the S-parameters for the ideal switched coupler are shown in Figure 5.16. The insertion loss is  $\sim$  -21.6 dB, the isolation is  $\sim$  -29.3 dB, with a through and coupled port magnitude losses of  $\sim$  0.6 dB per channel, a magnitude imbalance of 0.13 dB, and a phase imbalance of  $\sim$  0.2 degrees.



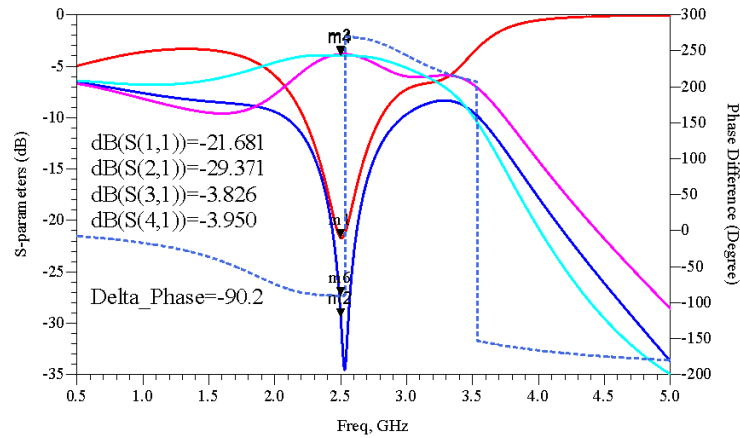


Figure 5.16 MEMS 0  $\Omega$  2.5 GHz amplitude response.

Subsequent simulations of the hybrid coupler with switch contact resistances of 0.25  $\Omega$  and 1.0  $\Omega$ . The added resistance of 0.25  $\Omega$  increased the insertion loss from  $\sim -21.6$  dB to  $\sim -19.8$  dB, the isolation is  $\sim -29.3$  dB to  $\sim -26.9$  dB, with a magnitude loss of  $\sim 1.2$  dB per channel, a magnitude imbalance of  $\sim 0.17$  dB, and a phase imbalance of  $\sim 0.3$  degrees. The contact resistance of 1.0  $\Omega$  increased the insertion loss from  $\sim -18.4$  dB to  $\sim -16.3$  dB, the isolation is  $\sim -24.7$  dB to  $\sim -21.8$  dB, with a magnitude loss of  $\sim 2.2$  dB per channel, a magnitude imbalance of 0.3 dB, and a phase imbalance of  $\sim 0.3$  degrees.

## 5.4.2 RF PIN Diode Switching Network

RF PIN Diodes are an established industry standard RF design component in switching applications. PIN Diodes differ from the traditional PN junction diode in that an “Intrinsic semiconductor” material is sandwiched between the N and P doped regions. The current-voltage characteristic of the PIN diode is comparable to that of the PN junction diode at low frequencies, but exhibits the characteristics of a linear resistance at RF frequencies [5.10].

For the purpose of this research the SKYWORKS SMP1345 Pin Diode was selected for comparison of the MEMS switched coupler. The SMP1345 has a very low forward bias capacitance of 0.15 pF and low resistance of 1.5  $\Omega$  at a forward-bias current of 10 mA [5.11]. Only the S-parameters of the given forward biased diode were used. As in the case of the MEMS coupler, the PIN diodes are inserted at the necessary switch points for a given inductor-capacitor bank, as shown in Figure 5.17 with the entire coupler schematic shown in Figure 5.18.

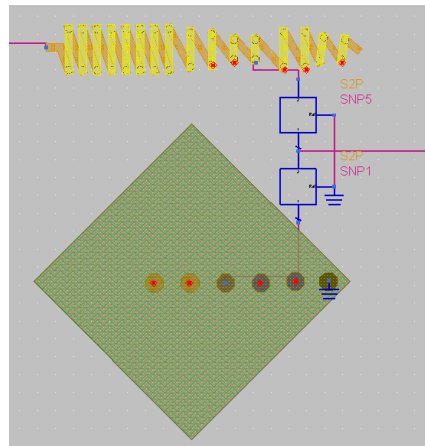


Figure 5.17 SMD 1345 2.5 GHz diode switched inductor/capacitor Bank.

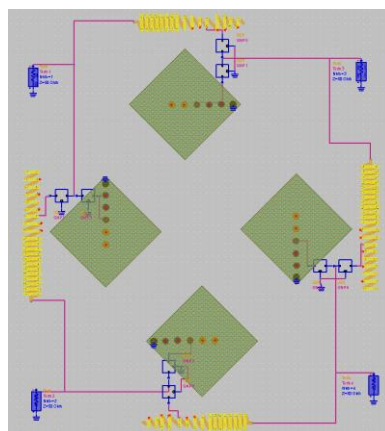


Figure 5.18 SMD 1345 2.5 GHz diode switched coupler evaluation schematic

In a similar fashion to the MEMS switched simulations, the PIN Diode switched coupler is now evaluated as function of forward bias diode current.

### 5.4.2.1 Effects of Diode Forward Bias Current

As can be seen in Figure 5.19, the insertion loss of the forward biased PIN diode is heavily dependent on the forward bias current  $I_f$ , with a forward bias current of 100 mA resulting with little to no loss at approximately 1.7 GHz, where as a forward bias current of 10 mA results in approximately -0.05 dB of loss. It's also worth noting that the overall loss vs. frequency characteristic is independent of forward bias current, only shifted in magnitude as a function of  $I_f$ .

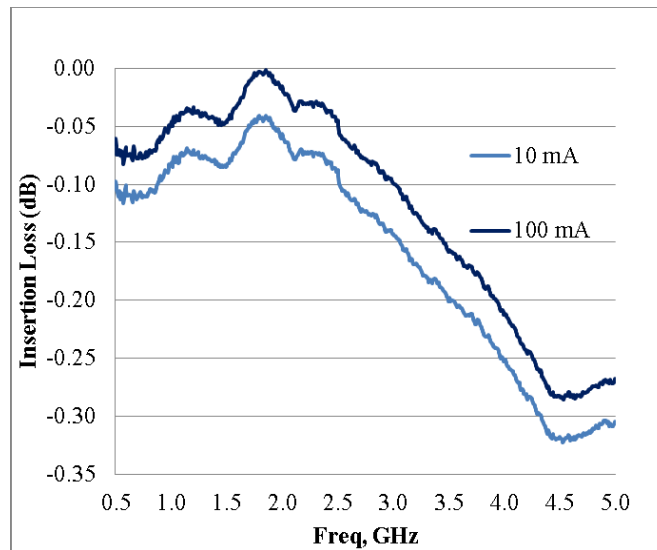


Figure 5.19 SMD 1345 forward bias insertion loss.

To further illustrate the effects of forward bias current on coupler performance, the circuit of Figure 5.18 was evaluated with forward bias currents of 10 mA, 20 mA, 50 mA, and 100 mA at 2.5 GHz, the 10 mA response is shown in Figure 5.20.

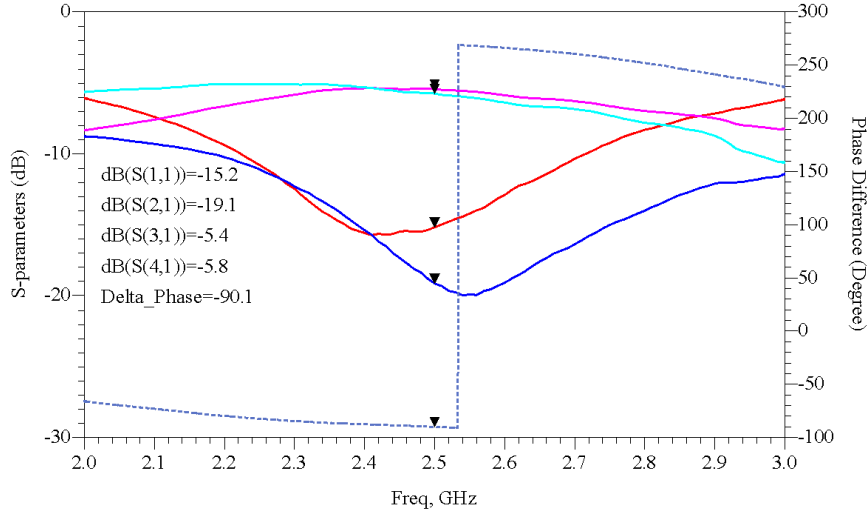


Figure 5.20 Diode switched s-parameters  $I_f=10\text{mA}$ .

The results of the simulations at various forward bias currents is as follows: the isolation loss and insertion loss are the most effected parameters between  $I_f < 20\text{mA}$ , but for  $I_f > 20\text{mA}$ , the coupler performance is mostly unchanged. Furthermore; the negligible effect on the phase difference between the coupled and through ports, i.e. between Port 3 and Port 4 demonstrate that the forward bias current has little effect on the phase performance of the coupler

To complete the MEMS switched vs. PIN diode switched hybrid coupler analysis, each of the coupler performance parameters will be analyzed and compared with the zero loss or ideal switched coupler. The return loss and isolation are presented in Figure 5.21 as S11 and S21 respectively. The 0.25 Ohm switched coupler approaches the ideal switched coupler for the S11 parameter. For a practical switching circuit, at least 50 mA of forward-bias current is required to match the performance of the 1 Ohm switched coupler. In a similar fashion, the isolation of the 0.25 Ohm coupler is the most ideal, while the performance of the PIN diode switched coupler reaches a limit around 50 mA with no improvement with higher forward-bias current.

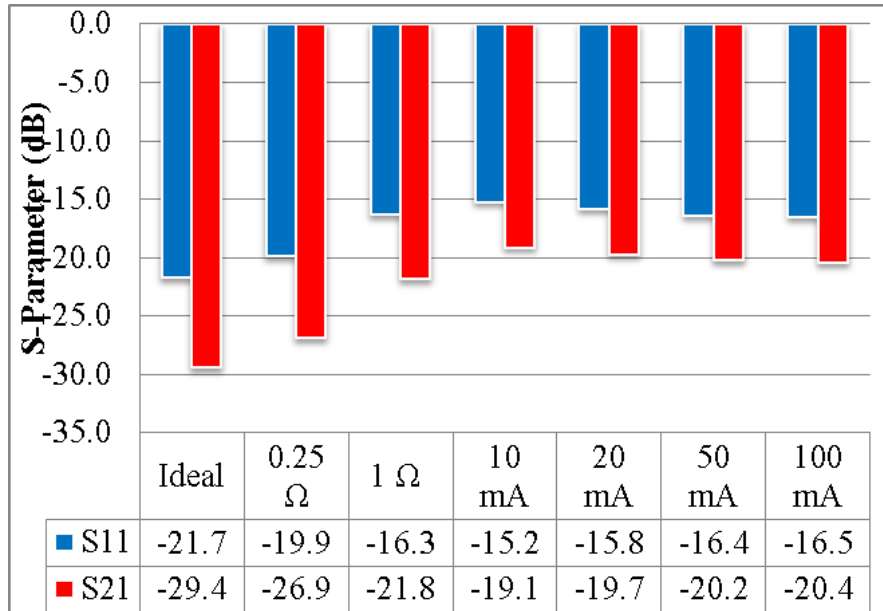


Figure 5.21 MEMS vs. PIN diode switching  $S_{11}$  and  $S_{21}$

The performance of the through port  $S_{31}$  and coupled port  $S_{41}$  are presented in Figure 5.22. Each of the momentum simulated  $S_{31}$  and  $S_{41}$  losses of the ideal switched coupler are already around -0.8 dB from the ideal theoretical coupler with no component losses, i.e. -3.8 dB vs. -3dB. The 0.25 Ohm switched coupler approaches the ideal switching with an additional 0.7 dB of loss, and the 1 Ohm additionally adds 0.6 Ohm loss for a decrease of 1.3 dB performance from the ideal MEMS switch switching case. For these parameters, only 20 mA of forward-bias current is required to match the performance of the 1 Ohm switched coupler with little to no performance improvement at higher forward bias current levels.

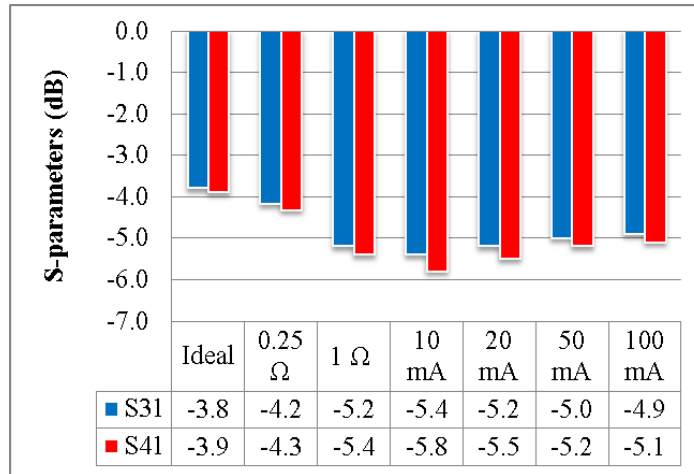


Figure 5.22 MEMS vs. diode switching  $S_{31}$  and  $S_{41}$  comparison.

A comparison of the amplitude imbalance as a function of MEMS vs. PIN Diode switching is shown in Figure 5.23. As can be easily observed, when compared with each other, the differences in each case is minimal, with even 10 mA providing a maximum of 0.4 dB, and 50 mA again approximating the 1 Ohm MEMS switched coupler. However, considering the theoretical 0.5 dB magnitude imbalance limit when a 54-Mbps data rate is desired used in an OFDM demodulator, each difference of 0.1 dB could be considered significant in when the system design is considered.

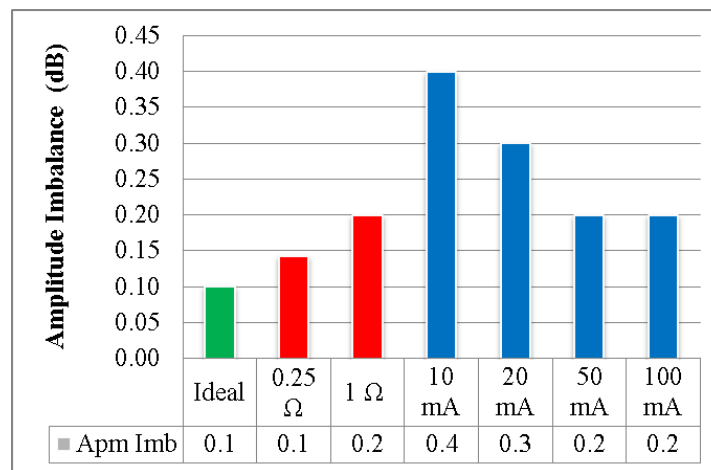


Figure 5.23 MEMS vs. diode switching amplitude imbalance comparison.

Lastly, comparison of the phase imbalance as a function of MEMS vs. PIN Diode switching is shown in Figure 5.24. The ideal switched coupler has a phase-imbalance of ~0.2 degrees, with the lowest phase imbalance being seen with the lowest diode-switched current simulated. In this case, the PIN Diode switched coupler meets, or exceeds the performance of the MEMS switched coupler in all simulated forward-bias currents.

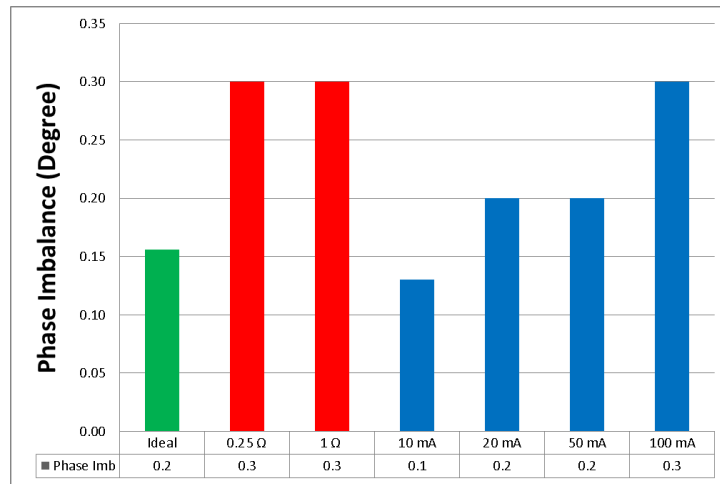


Figure 5.24 MEMS vs. diode switching phase imbalance.

The conclusion of the simulation results is that the forward bias current needed depends on the parameter that is most critical to the application. If only the phase distortion is the critical parameter for the overall circuit application, then a PIN Diode switched coupler with low forward-bias currents can be used. If any of the remaining performance parameters, i.e. isolation, return loss, amplitude loss or amplitude imbalance are critical, then the forward-bias current must be evaluated on a case-by-case basis, or the selection of a MEMS switched coupler may be optimal to minimize power consumption, or amplitude imbalance when used in I/Q transceivers .

## 5.5 Multichannel 2.0 to 3.0 GHz Coupler Design

Thus far, numerous aspects of the design of an ISM Band PI-transformed  $90^\circ$  lumped element tunable hybrid coupler have been discussed, i.e. the effects of inductor Q, as well as the effects of MEMS switching vs. Diode Switching. For completion, a full integrated circuit layout topology utilizing a practical MEMS switch found in the literature was created for the demonstration of the remaining issues involved with a practical implementation of such a concept, i.e. the effects of cross-talk between components, and the effect of component interconnections. For this purpose, the basic dimensions of the compact RF MEMS DC contact switch published by Patel and Rebiez was used as a basis for design a layout that could work on such a switch topology, a sp6T version is shown in Figure 5.25 [5.12].

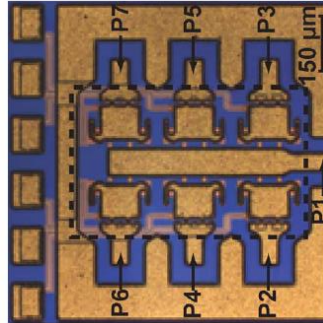


Figure 5.25 Patel and Rebeiz SP6T compact rf dc mems switch.

The 1<sup>st</sup> step taken to utilize the chosen switch was to create a GSG input-output structure, as can be seen in Figure 5.26. Points A/B/C on the left represent the input to the switched inductor-capacitor bank, while points D/E/F represent the output port. Points G through K represent in input to the inductor MEMS selection switches, while points L through P represent the input to the capacitor MEMS selection switches.



Finally, the transmission line TL is the common bus between all switches that connects the switch outputs to the output of the inductor capacitor bank.

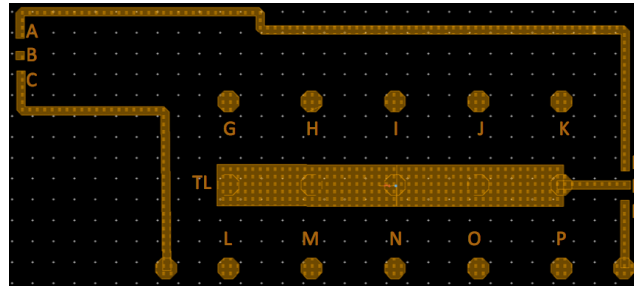


Figure 5.26 MEMS switch based ground-signal-ground I/O layout.

With this structure in mind, both of the main-branch and side-branch inductor/capacitor banks are now be discussed.

### 5.5.1 Signal Tapped Inductor-Capacitor Design

Based on this switching topology, a signal switched tapped capacitor bank layout was designed to fit the theoretical switch contact points and is shown in Figure 5.27.

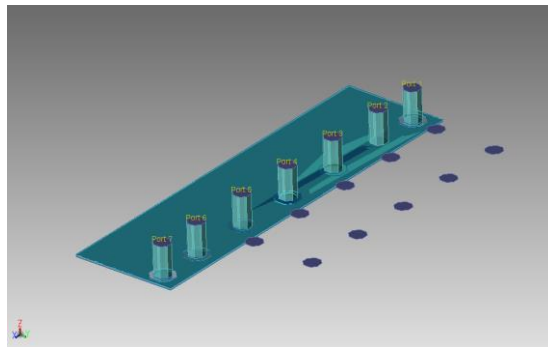


Figure 5.27 Three-dimensional view of signal switched tapped capacitor bank.

In this configuration, Ports 2 through 6 are the signal taps from the tapped series-capacitor bank, while ports 1 and 7 are used to ground each end of the ground plane from the top level ground traces. As can be seen in Figure 5.28, the simulated capacitance at

each tap is frequency dependent with approximately a 10% increase in capacitance across the frequency range of 2.0 GHz to 3.0 GHz.



Figure 5.28 Signal switched tapped capacitance vs. frequency.

As has been previously discussed, the tapped capacitor quality factors, which are shown in Figure 5.29, can be an important design parameter for the overall coupler performance. Since capacitor quality factors above 300 have negligible impact on coupler performance, the momentum simulated tapped capacitor quality factors, which range from ~375 to ~800, will have negligible effect on the coupler's performance.

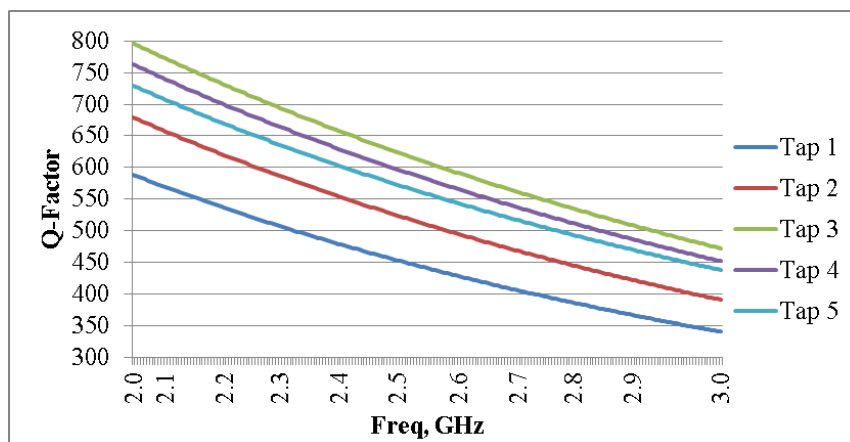


Figure 5.29 Signal switched tapped capacitor quality factor vs. frequency.

Recalling the signal switched tunable L/C bank schematically shown in Figure 5.2, then with the tapped inductor and tapped capacitor designs principally complete, they are now combined into a layout that functions as the main-branch and side-branch tapped inductor-capacitor banks, and shown in Figure 5.30 and Figure 5.31 respectively. In each case, L1/C1 through L5/C5 represents frequency 1 through frequency 5.

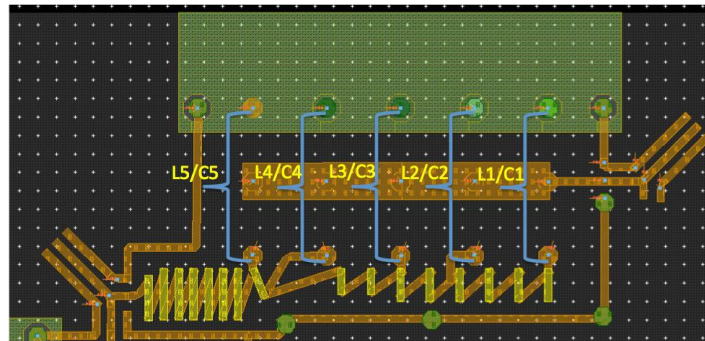


Figure 5.30 Main branch tapped inductor/capacitor bank.

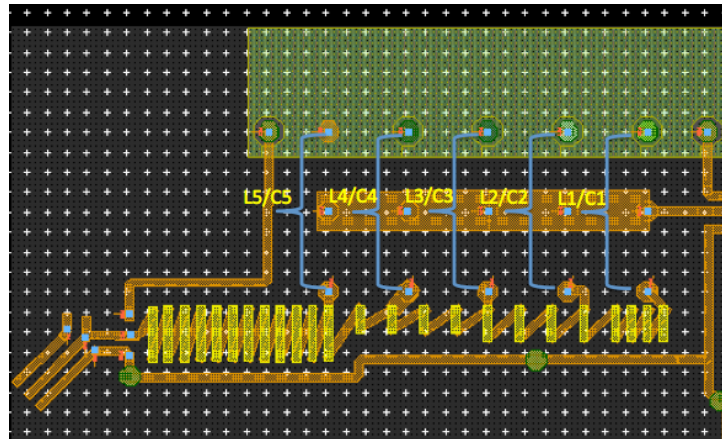


Figure 5.31 Side branch tapped inductor/capacitor bank.

The inductor Q-factor characteristic for the combined layout was essentially same as that of the standalone simulations, and is shown in Figure 5.32 for the 2.13 GHz configuration. As before, the Q-factor generally increases with frequency. Therefore; a Q at the lowest frequency implies the higher taps should still have sufficient Q.

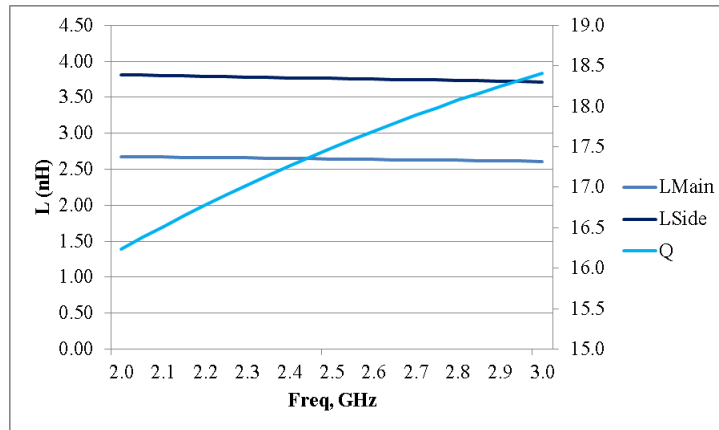


Figure 5.32 Tapped inductances and Q factors at 2.13 GHz.

The symmetry of the  $90^\circ$  PI-transformed lumped element hybrid coupler has the characteristic that the coupler can be easily reduced to a half-coupler, reducing the simulation speed for design and simulation purposes, a 3D display of the half-coupler is shown in Figure 5-60.

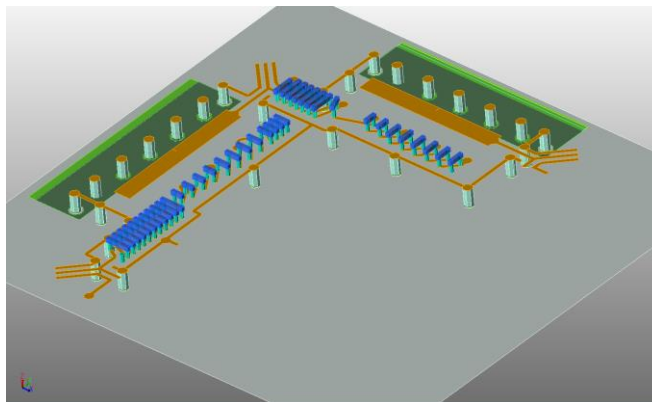


Figure 5.33 3D view main and side branches with tapped inductor/capacitor banks.

Furthermore; the half-coupler design concept has the additional benefit of eliminating duplication of design changes for the opposite coupler branch leg which

could lead to design errors. Once this iterative optimization procedure was complete, a single layout created is created by combining the two sections as needed.

### 5.5.2 Initial Design Results

To finalize the results of the initial signal switched hybrid coupler design, the circuit of Figure 5-61, shown in the 2.123 GHz configuration, was used to generate the S-parameters for each of the five center frequencies.

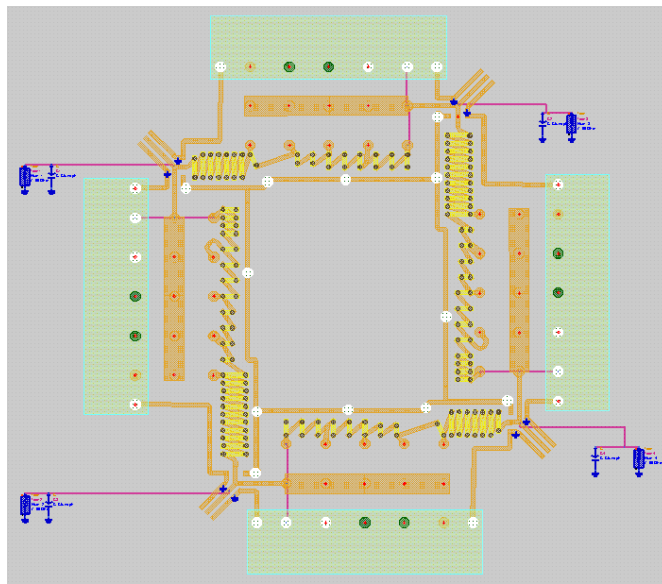


Figure 5.34 Total coupler 2.123 GHz tap momentum simulation.

To simulate the remaining center-frequency configurations, the port connections were made for each center frequency as described in Figure 5.30 and Figure 5.31 with the 0.5 GHz to 5.0 GHz magnitude responses and phase response for the 2.9 GHz configuration shown in Figure 5.35.

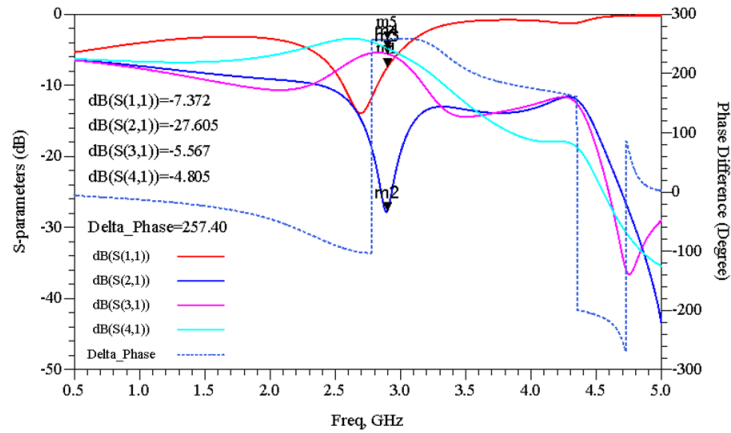


Figure 5.35 Total coupler 2.9 GHz tap s-parameters and phase response.

At 2.9 GHz, it is easily observed that the magnitude responses and phase response of the coupler differs significantly from the original design goals, and what was demonstrated as theoretically possible with no layout interaction. To determine the issues with this design, the 2.9 GHz configuration was simulated with an ideal capacitor instead of the tapped capacitor, as shown in Figure 5.36.

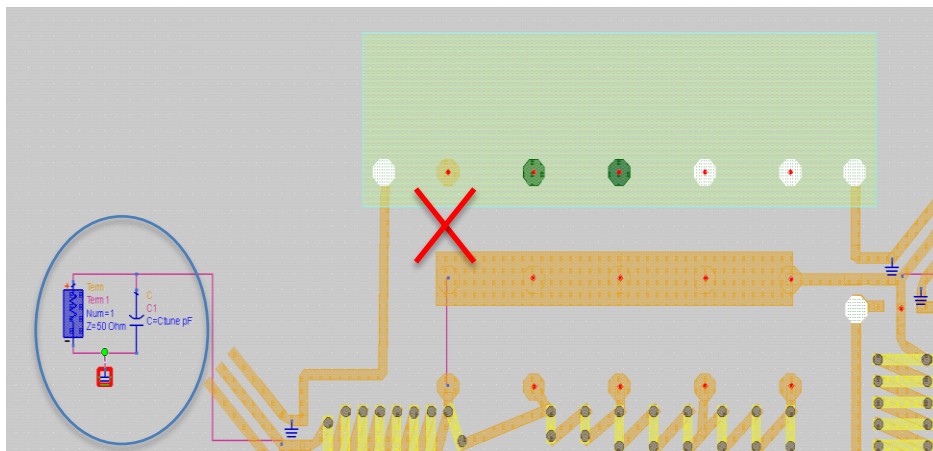


Figure 5.36 Schematic diagram of 2.9 GHz coupler with ideal capacitor.

As can be observed in Figure 5.37, the phase response is nearly ideal, with all of the S-parameters dramatically improved.

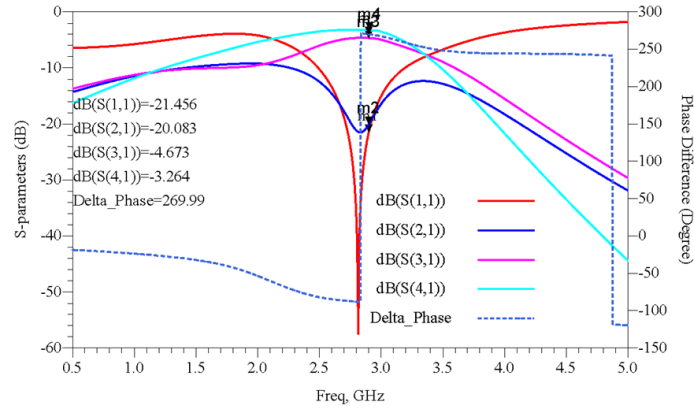


Figure 5.37 2.9 GHz amplitude and phase responses with ideal capacitors.

Hence, it is reasonable to conclude that improving the magnitude and phase responses of the coupler is dependent on understanding the influence of the layout on the signal switched capacitor banks.

### 5.5.3 Tapped Ground Switched Capacitor Design

As a consequence of the negative effects of the signal switched tapped capacitor design were understood, the question came as how to arrive at a solution. To improve the performance, the tunable capacitance has to be available at a single point of the structure’s layout, while still being quasi-tunable. Having a single signal output port variable capacitance with the switch layout chosen for this design necessitates that the grounds are switched to select the dielectric layers instead of the signal output, consequently resulting in a “Ground Switched Tapped Quasi-Tunable Capacitor”.

The concept of the ground switched tunable capacitor is essentially the reverse of the signal switched tunable capacitor. The arbitrary signal-switched tunable capacitor has a common ground port for the series capacitor structure, N-signal output ports with a given switch tapping the appropriate signal side capacitor plate through vias. To the

contrary, the arbitrary ground switched tunable capacitor has the output taken at a single port with the ground switched at the appropriate ground side plate in the series capacitance structure, with each ports along the top of the layout, as opposed to the signals outputs, connected by means of vias along the layout. To further illustrate the concept, consider the schematic shown in Figure 5.38, which represents a generalized inductor-capacitor bank of either the main or side branches. It is similar to the switch signal switched circuit with respect to the tapped inductor, but the tapped capacitor now has a single output with the ground ports switched along the series capacitor structure instead of the signal ports.

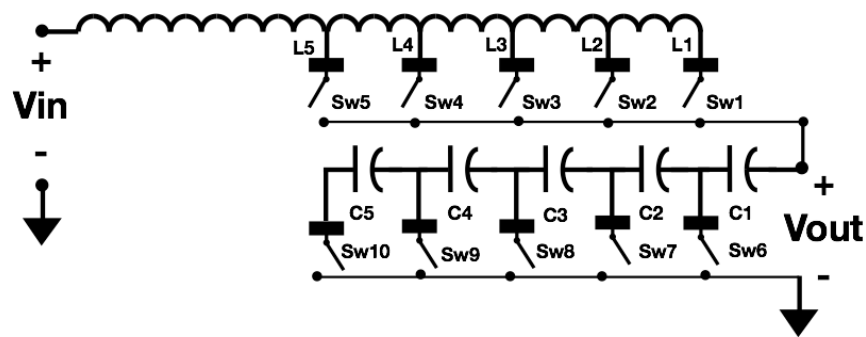


Figure 5.38 Ground switched hybrid coupler tunable L/C circuit.

The three-dimensional layout of the ground-switched capacitor bank is shown in Figure 5.39, where the ground contacts for capacitors C1 through C5 are shown, as well as the output, each contact being brought to the surface of the substrate with vias.



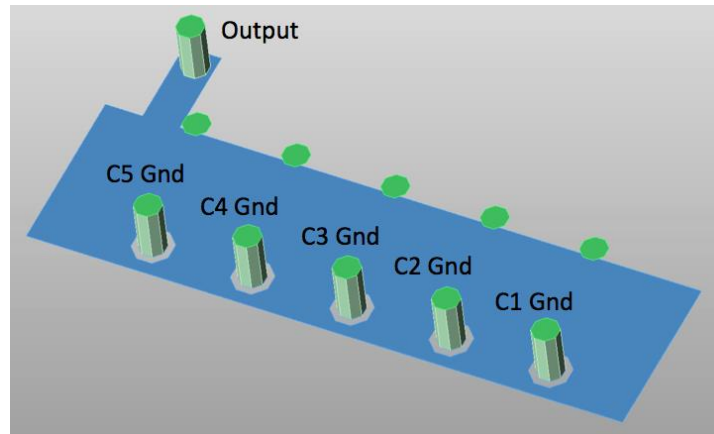


Figure 5.39 Ground switched tunable capacitor bank three-dimensional view.

For further clarification, the switching concept of the layout is shown in Figure 5.40, where the MEMS relay contacts will be attached to a common ground bus for switching, and with the output shown at the left side of the diagram.

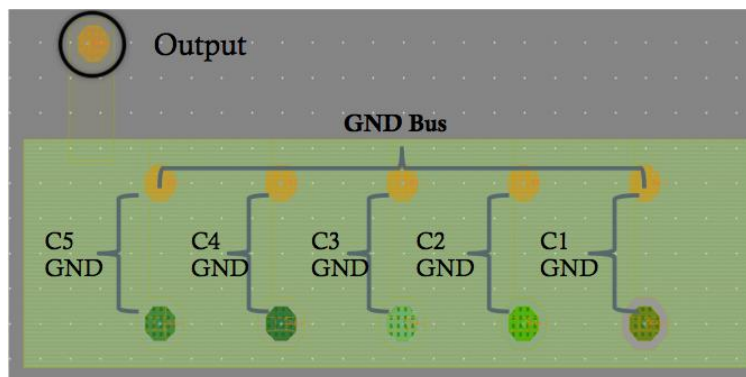


Figure 5.40 Ground switched tunable capacitor bank schematic view.

Naturally, the capacitor's substrate dielectric layers are necessarily readjusted to accommodate the specified capacitance at the coupler center frequencies of interest. The dielectric layer thicknesses are similar to the signal-switched tapped capacitor, but with the order of the layers reversed as shown in Figure 5.41.

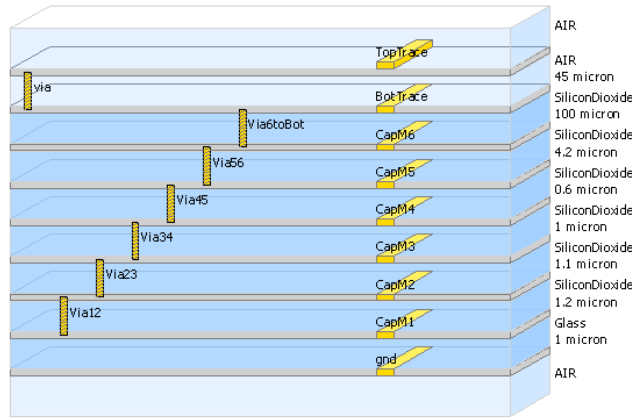


Figure 5.41 Ground switched tunable capacitor bank initial substrate.

Evaluation of the ground-switched tapped capacitor bank a 2.9 GHz is shown in Figure 5.42. As can be seen, the capacitor Q of 243 should be sufficient to improve the coupler performance, compared to the original 2.9 GHz capacitor Q of 109.

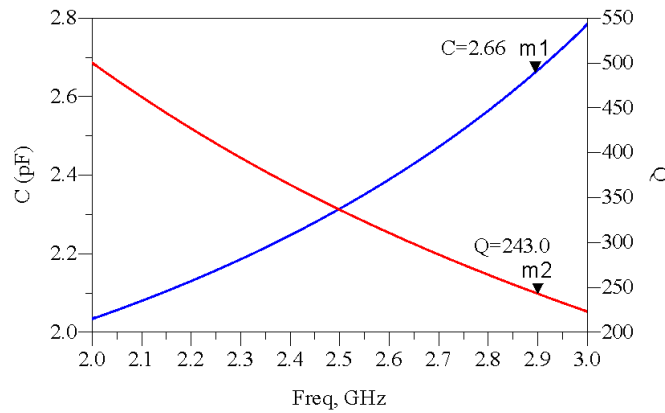


Figure 5.42 2.9 GHz ground switched capacitance and Q.

### 5.5.4 Redesign with Ground Switched Capacitor

With the new ground-switched tapped capacitor design concept validated, the updated main branch and side branch inductor-capacitor banks are shown in Figure 5.43 and Figure 5.44.

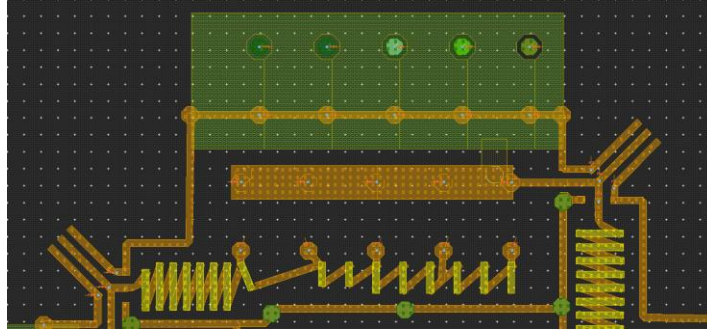


Figure 5.43 Switched ground main-branch inductor-capacitor bank.

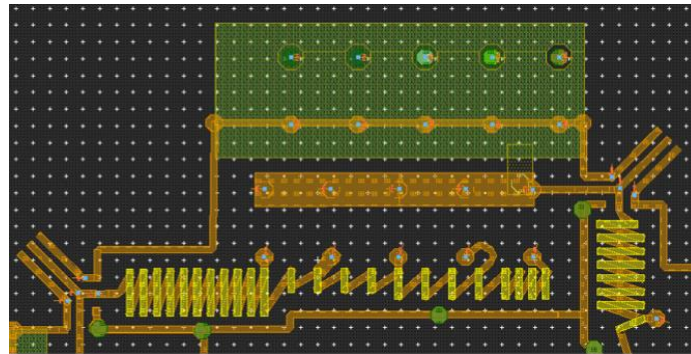


Figure 5.44 Switched ground side-branch inductor-capacitor bank.

The simulation results of the new design concept at 2.9 GHz are shown in Figure 5.45.

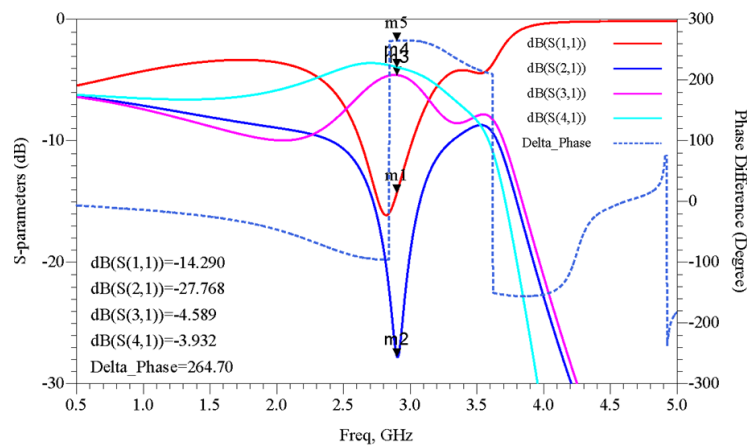


Figure 5.45 2.9 GHz amplitude and phase response switched ground capacitor bank.

As can be seen, the S-parameters of the new design at 2.9 GHz are much improved over the signal switched capacitor design. A comparison of the improvements

are shown in Figure 5.46 through Figure 5.49, where “design 1” is the initial signal switched tapped capacitor design, and “design 2” is the ground switched tapped capacitor design.

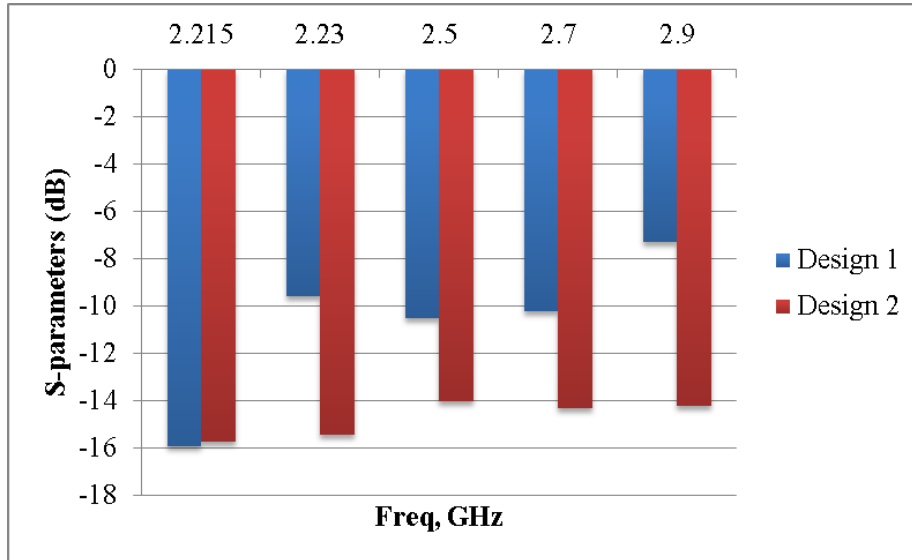


Figure 5.46 Return loss comparison of initial and final coupler designs.

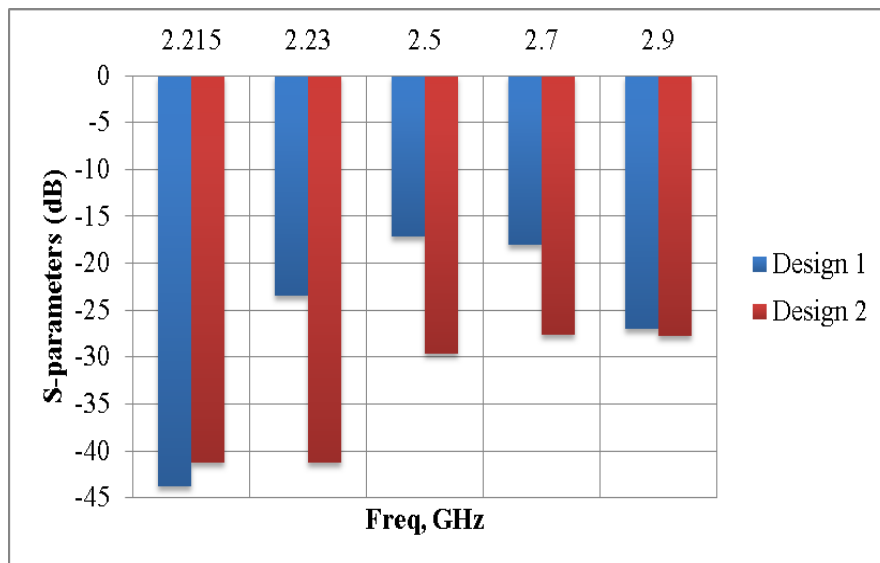


Figure 5.47 Isolation comparison of initial and final coupler designs.

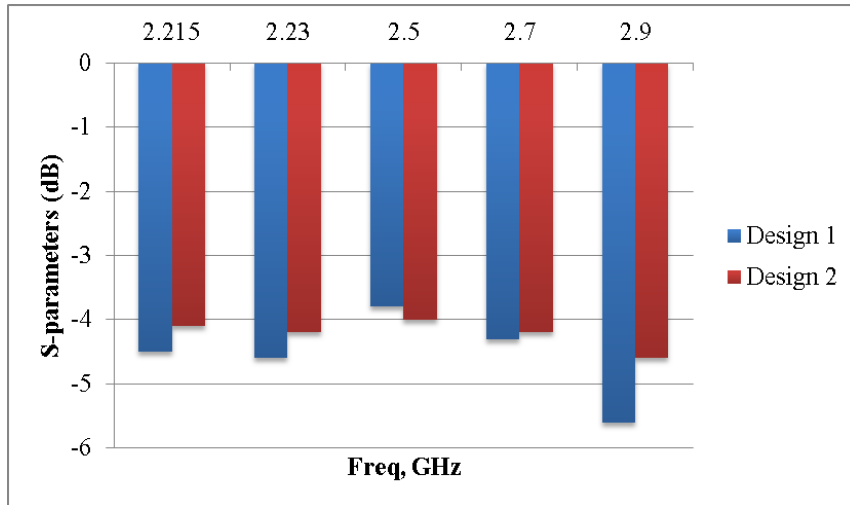


Figure 5.48 Through port coupling comparison of initial and final coupler designs.

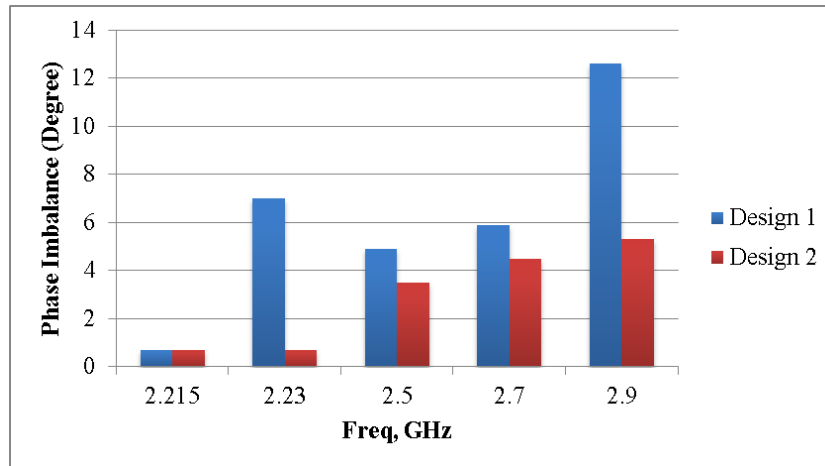


Figure 5.49 Phase imbalance comparison of initial and final coupler designs.

As is easily seen, while the coupling and isolation are improved, the phase imbalance, and return loss are the most improved performance parameters.

## 5.6 Conclusion

It has been shown, theoretically, and via ADS momentum simulation, that the performance of a tunable PI-transformed  $90^\circ$  lumped element hybrid coupler can closely

approximate that of an off the shelf industrial coupler in the 2.0 GHz to 3.0 GHz frequency range with an inductor quality factor of at least 15.

Using 3D solenoidal inductors, and the S-parameters of an off the shelf RF PIN diode as the basis for evaluation, the performance of a theoretical DC contact MEMS switched hybrid coupler, at various DC contact resistances, was compared to that of a RF PIN diode switched coupler. If only the phase performance of the coupler is critical for a given application, then a PIN diode with low forward-bias current can be used in the design with no impact on performance. If amplitude loss, insertion loss, or isolation are critical, then a DC-contact MEMS switch might be a preferable choice in technology.

A quasi-tunable lumped element hybrid coupler design based on an IPD technology tapped capacitor bank, tapped 3D air core solenoidal inductors, and the dimensions of a practical MEMS switch structure found in the literature was presented. Two coupler designs were demonstrated, one based on a signal switched tapped series capacitance, and one derived from a ground switched tapped capacitance, the latter being superior in performance, and closely approximating the off the shelf Anaren coupler in return loss and isolation performance.

The obvious practical issue involved in implementing the proposed design is how to assemble the switches and passive components together. Several methods have been proposed on how to integrated MEMS on a targeted substrate, embed the MEMS switches into the substrate, or integrate the passive components on the backside of a MEMS switch substrate prior to being packaged [5.13-5.15], any of which could potentially be suitable for this design concept.

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# **CHAPTER 6 Design of a Dual Band Lumped Element Switchable Hybrid Coupler**

## **6.0 Introduction**

The printed circuit board has for many decades been the backbone of the consumer and military electronic industries. Cutting edge personal computing technology, e.g. smart phones, laptop and desktop computers, as well as the advancement of automotive safety and comfort features have all led to the advancement of Printed Circuit Board Technology. As previously mentioned, Gurbuz, and Rebiez published the results of a tunable quadrature coupler for use in the 1.6-2.3 GHz frequency range, demonstrating the need and application of re-configurable quadrature couplers on PCB technology [6.1]. Numerous other examples exist in the literature where varactors are used with fixed branch impedances to change the center frequency of operation. These types of design invariably lead to decreased performance at the frequency/s of operation where the branch impedances deviate from the desired values. Consider Figure 6.1, where the insertion loss of a varactor tuned PCB hybrid coupler designed to operate at the GSM bands of 900 MHz and 1800 MHz are shown [6.2]. The insertion loss at 1800 MHz is approximately -40 dB, and approximately -23 dB at 900 MHz, demonstrating the unmatched coupler input impedance at different frequencies of operation.

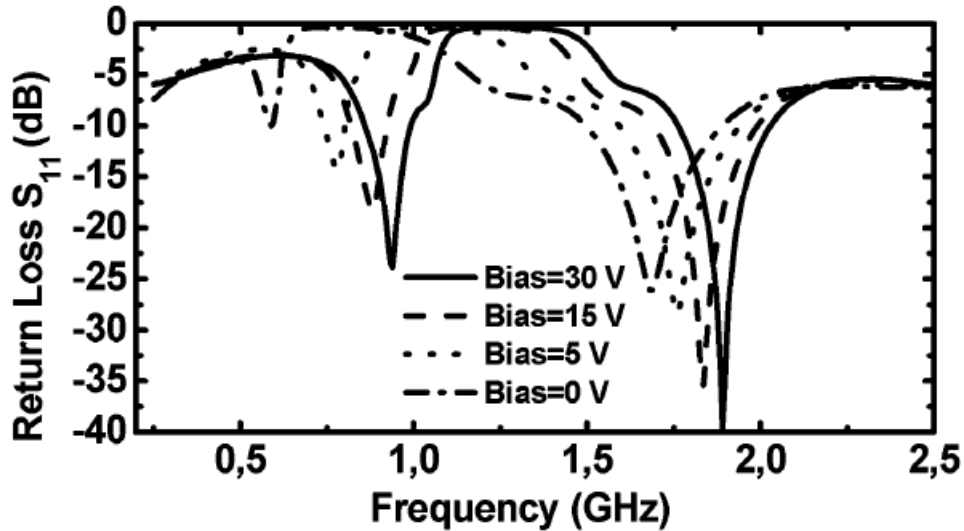


Figure 6.1 PCB Varactor tuned dual band pcb hybrid coupler.

Naturally, degradation in return loss and isolation generally leads to degradation in amplitude and phase balance, which leads to decreased performance when used as a phase shifter for an I/Q modulator/demodulator. With this in mind, a fully tunable printed circuit board RF hybrid coupler, i.e. where all branch impedances are matched at all frequencies of operation, that maximizes the coupled signal strengths, and minimizes return loss in applications that are sensitive to amplitude loss and imbalance is worthy of investigation.

To demonstrate the principle of a quasi-tunable lumped element hybrid coupler, a selectable two-channel design based on the layout and footprint of an industry standard RF relay was implemented on a printed circuit board. The physical limitations and performance of RF circuits using PCB are numerous. For example, minimum trace width and spacing, minimum via size, via ring diameters, and minimum board layer thicknesses all impact and limit the possibilities of designing and fabricating such a coupler on an industry standard printed circuit board.

## 6.1 Coupler Design Concept

The initial design goal was to have two channel center frequencies at 500 MHz, and 1 GHz. Various momentum simulations using a 10 mil thickness for the PCB and 20 mil traces widths led to the understanding that true solenoidal inductors are not achievable on a PCB, even when designed with a solenoidal structure. This is primarily assumed to be caused by the poor flux linkage between the conductor loops, which is resulted from the necessary conductor trace spacing from minimum via ring separation. That being said, it was demonstrated that self-inductance of printed conductors could be used as inductors in the range of 5 to 20 nH for use in frequency range up to 1 GHz. Furthermore; with associated quality factors of approximately 60 to 120, they are also be well suited for use in constructing a lumped element hybrid coupler.

Since the lengths of the printed conductor traces are the means for constructing the main and side branch inductors, it's obvious that the maximum frequency achievable is inversely proportional to the spacing of the switching relays. With these considerations in mind, the smallest relay possible was needed to achieve frequencies approaching the 1 GHz range. A research of off the shelf RF relays led to the selection of the Omron G6K High Frequency Relay, whose terminal arrangement is shown in Figure 6.2 [6.3]

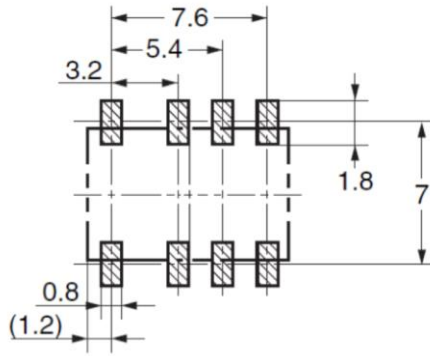


Figure 6.2 Omron GY6 terminal layout.

A detailed explanation of the re-configurable circuits will now be given. Each branch of the hybrid coupler has essentially 4 switching backs, two for the main-branch inductances, and two for the side-branch inductances, each of which have a capacitance to ground. The high frequency configuration with the switching relay in the de-energized state is shown in Figure 6.3.

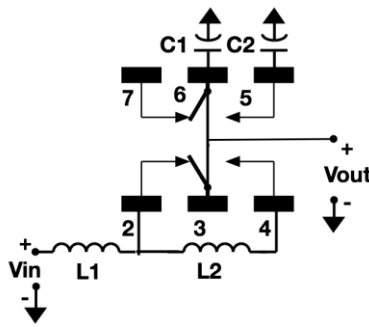


Figure 6.3 High frequency inductor/capacitor switching bank.

For the purpose of this design, pin 3 of each relay is connected to an associated input/output port of the four-port coupler circuit. To achieve two operating frequencies, the high frequency inductance  $L1$ , which will be shown to be the lower inductance value, for any given branch is connected to the normally closed contact pin 2, while the

additional inductance for the lower frequency L2 is added and connected to pin 4. In a similar fashion, the high frequency capacitance is connected to the remaining center pin, i.e. pin 6, which is also shorted to pin 3, which completes the circuit for the de-energized state of the switching relays.

For the low frequency circuit configuration, consider the schematic of Figure 6.4 , which now shows the relay switch contacts in the energized state. The resulting inductance seen at the output port is now  $L1+L2$ , and the total capacitance  $C_t$  is now  $C1 + C2$ , which is the desired inductance/capacitance configuration for the lower second operating frequency.

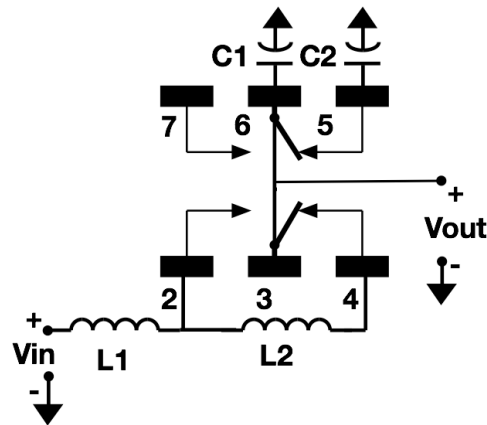


Figure 6.4 Low Frequency inductor/capacitor switching bank

With this switching topology then, a dual band lumped element hybrid coupler is feasible. Additionally important to the design is the selected printed circuit board material chosen for the application. The majority of printed circuit boards readily available for quick turnaround are based on FR-4 type materials, utilizing copper thicknesses in the range of 0.5 Oz to 2 Oz as shown in **Error! Reference source not found.**

Table 6.1 PCB Copper Weight vs. Thickness

Weight	Thickness (mils)	Thickness (um)
0.5 Oz.	0.7	~17.5
1 Oz.	1.4	~35
2 Oz.	2.8	~70

At first glance it would appear that a two-layer printed circuit board would be sufficient for the switchable coupler design. As discussed in Chapter 3, two layers are all that are required to form a MIM capacitor for use as the corner capacitance  $C_t$ , and furthermore each inductor requires only a ground and a signal trace, or combination of traces. As will be shown, to not cross the ground conductor traces, of which symmetry are important for coupler performance, another layer is required to provide a path for the additional inductance that is switched in circuit for the lower operating frequency. While a three-layer core would be sufficient, a four-layer core allows the capacitors to be placed on the opposite side of the board layout. This has the benefit of reducing cross talk between the capacitors and inductors, as well as preventing interference with the layout of the inductors and SMA connects on the opposite side of the printed circuit board.

To keep costs low, a search was performed to find a low cost PCB fabricator, which resulted in selection of Advanced Circuits Corporation as the supplier. Consultation with Advanced Circuits' Engineering department led to the selection of a four-layer core manufactured by Polar Corporation, of which the material description as well as pre and post processing layer stack-up data are shown in Figure 6-5 and Figure 6.6 respectively [6.4].

Layer	Stack up	Type	Description
1		soldermask	PSR-4000BN (semi gloss)
		foil	1/2 oz copper foil
2		pre-preg	FR406 2116 pre-preg
		core	FR406 .014 1/1 core
		pre-preg	FR406 2116 pre-preg
		pre-preg	FR406 2116 pre-preg
		pre-preg	FR406 2116 pre-preg
		pre-preg	FR406 2116 pre-preg
		core	FR406 .014 1/1 core
		pre-preg	FR406 2116 pre-preg
3		foil	1/2 oz copper foil
		soldermask	PSR-4000BN (semi gloss)

Figure 6.5 Polar PCB material vs. layer description.

Base Thickness	Processed Thickness	Resin Content	Impedance ID	$\epsilon_r$
				4.500
0.600	1.600		1	
4.830	4.253	56.000		3.790
1.200	1.200			
14.000	14.000	41.000		4.140
4.830	4.830	56.000		3.790
4.830	4.830	56.000		3.790
4.830	4.830	56.000		3.790
4.830	4.830	56.000		3.790
14.000	14.000	41.000		4.140
1.200	1.200			
4.830	4.253	56.000		3.790
0.600	1.600			
				4.500

Figure 6.6 Polar PCB pre/post processed stack up data.

Of particular interest is the post processing dielectric payer thicknesses, and the relative dielectric constants of the recommended laminated board. In general discussions, PCB layer thicknesses and dielectric constants are discussed in terms of rounded numbers, e.g. 5 mil dielectric layer thickness, and relative dielectric constants of “4”. As can be seen, not only do the actual core thicknesses and material constants differ from commonly used industry standard terminology, e.g. this PCB laminate has a base thickness of 4.83 mils between the outer and inner layers instead of 5 mils, and a dielectric constant of 3.97 instead of 4.0 as suggested by FR4, the post-processed

thickness changes significantly to 4.253 mils. While the post-processed thicknesses have negligible impact on the inductor design, they are critically important to the construction of the MIM capacitors which both depend on the distance between the capacitor plates and the dielectric constant between them. Consequently, the inductor and capacitor designs carried out by means of Agilent ADS momentum simulations were performed with the stack up definition shown in Figure 6.7.

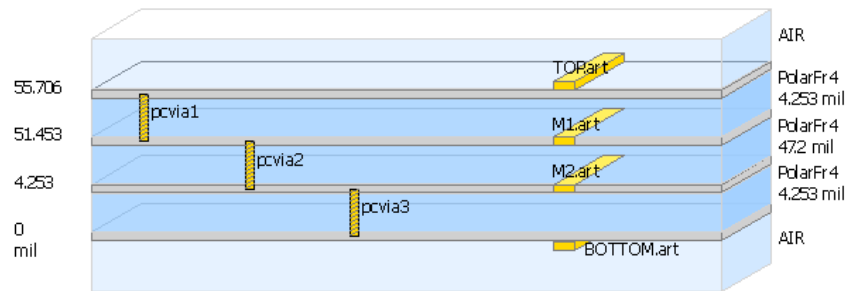


Figure 6.7 ADS momentum PCB substrate stack up.

## 6.2 Design of Switched Inductors

The series inductance of a straight wire conductor can be estimated by (6-1) [6.5], where  $l$  is the length of the conductor, and  $p$  is the conductor's outer perimeter.

$$L = \frac{\mu_0 l}{2\pi} \left[ \ln \left( \frac{4l}{p} \right) + \frac{1}{2} \right] nH \quad (6-1)$$

For this design, the required inductances are created using the series self-inductance of the printed circuit board traces. With that in mind, the first constraint to be established is the distance from the center conductor of any given relay, i.e. pin 3 to the normally closed contact of the relay to which the output series inductance is connected, or in this case pin 2. Consequently, the base layout was created using the CAD drawings of the Omron G6Y relay, and is shown in Figure 6.8.



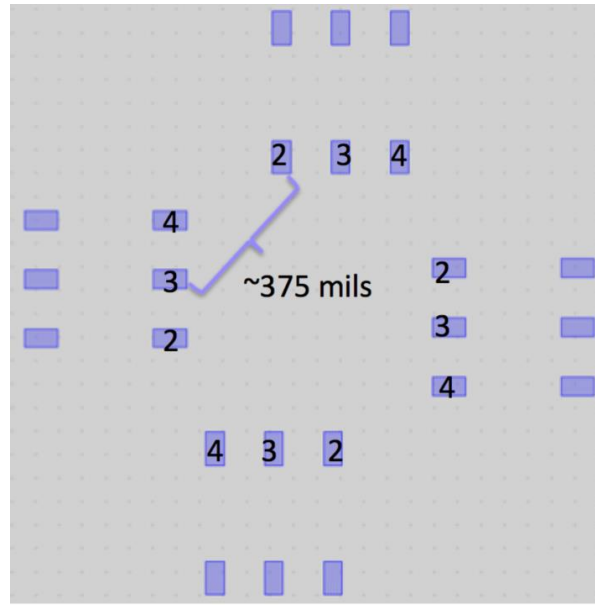


Figure 6.8 Omron relay PCB layout.

Due to a distance of approximately 375 mils between the relay center contacts, i.e. pin 3 and the adjacent normally closed contact, i.e. pin 2, and an assumed minimum conductor width of 10 mils, a minimum inductance in the range of approximately 6 nH is to be expected. The lowest inductance value in a PI-transformed  $90^\circ$  lumped element branch line hybrid coupler is associated with the main branch impedances. Hence, the first inductance that needs to be determined by the layout constraints is the main branch inductance. In this instance an inductance of 6.2 nH was achieved by a single trace connecting the center contact, i.e. pin 3 of the relay on the left, to the left pin of the relay on the right side, i.e. pin 2 through a pad that simulates the relay contacts to the right center pin as seen in Figure 6.8.

Explanation of the design will begin with a 3-D top view of the final overall 900 MHz layout as shown in Figure 6.9. The required capacitance metal layers C1, C2 and the “Capacitor Ground” layer are used to form the capacitances  $C_i$  at each coupler output. The main branch inductances  $L_{\text{main}}$  are seen as the horizontal trances, the side branch

inductances  $L_{\text{side}}$  are shown as the vertical traces. The RF switching relays are shown in the non-switched condition with the contacts simulates as short circuits between the contact pads as R1 through R4. Finally J1 through J4 represent the SMA connectors used for measuring the performance of the coupler with a Network Analyzer.

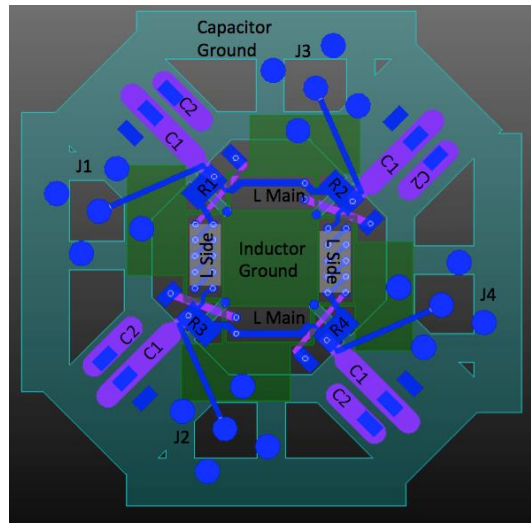


Figure 6.9 900 MHz coupler 3D top view.

The upper frequency of 900 MHz was determined by creating an inductor with more or less a straight path, and narrow conductor width of 20 mils between pins 2 and 3 of adjacent relays as shown in Figure 6.10. Assuming a  $Z_0$  of  $50 \Omega$ , the inductance of  $\sim 6.2$  nH is appropriate for a 900 MHz main branch inductor as given by (6-2).

$$L_M = \frac{Z_0}{2\pi f} \quad (6-2)$$

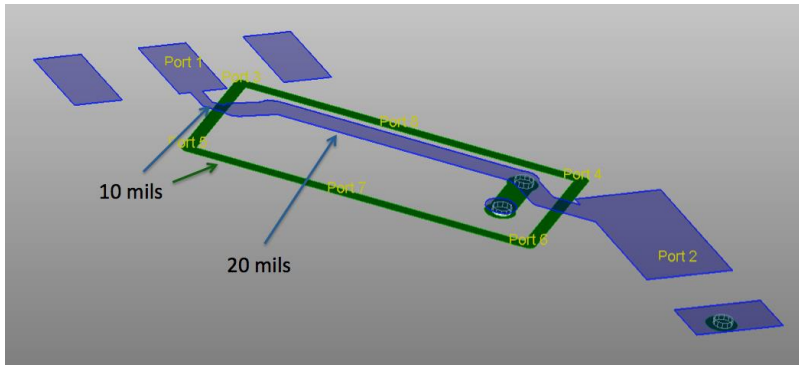


Figure 6.10 3D view of main branch inductance-900 MHz configuration.

The momentum simulation results shown in Figure 6.11 demonstrate that the inductance value is fairly consistent from 100 MHz to 1.5 GHz, with a good quality factor of approximately 137.

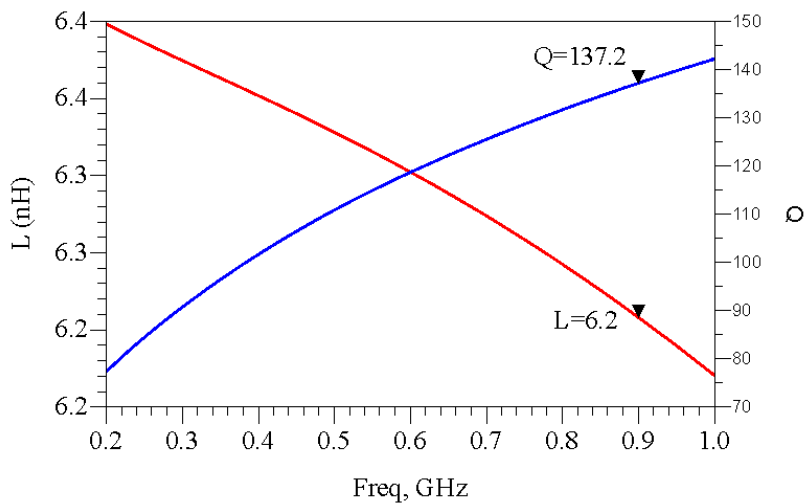


Figure 6.11 Simulated 6.2 nH main branch inductance.

The overall lower frequency main branch inductance is shown in Figure 6.12, with the additional series inductance of approximately 2.7 nH, for a combined inductance of 8.9 nH is shown in Figure 6.13.

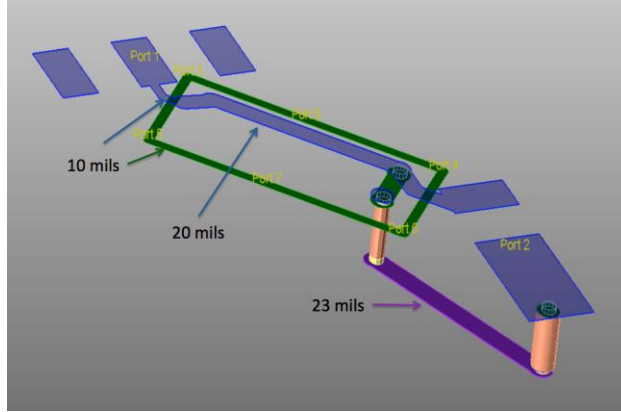


Figure 6.12 3D view of main branch inductance-630 MHz configuration.

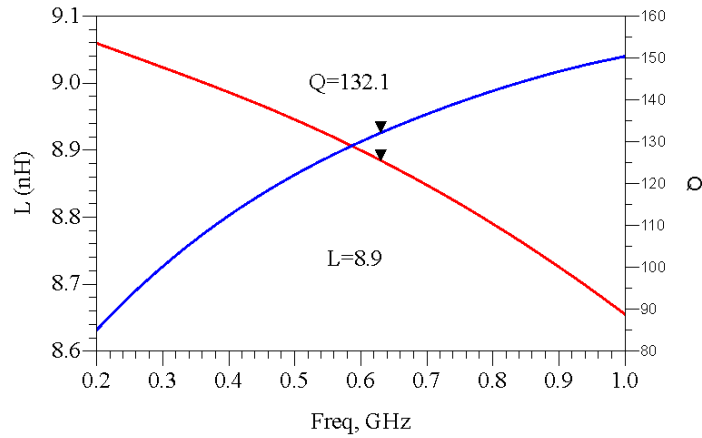


Figure 6.13 Simulated 8.9 nH main branch inductance.

For simplicity of design purposes, the parallel capacitances  $C_S$  and  $C_M$  are combined into a single capacitance  $C_T = C_S + C_m$ , the required values are shown in Table 6.2.

Table 6.2 Dual Band Switched Coupler Component Values

Frequency	630 MHz	900 MHz
$L_m$ nH	8.93	6.22
$L_s$ nH	12.63	8.84
$C_T$ pF	12.2	8.54

The next step is to create the side branch inductances of 8.6 nH and 12.6 nH. The 900 MHz side-branch 8.6 nH inductance is shown in the layout of Figure 6.14. This

inductor consists of a number of stitched series inductors across the TOP layer and the inner M1 layer by means of vias to achieve the desired value with the total inductance shown in Figure 6.15.

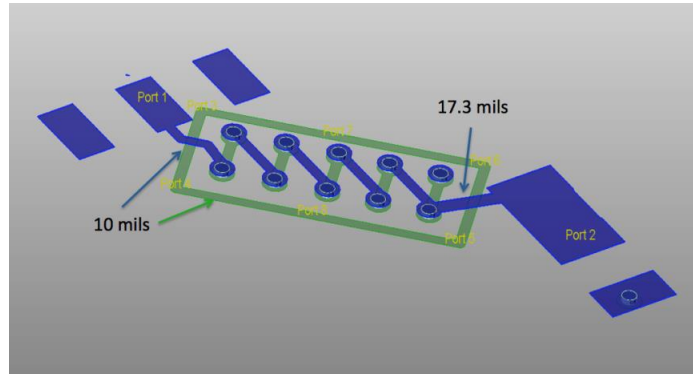


Figure 6.14 3D view of side branch inductance-900 MHz configuration,

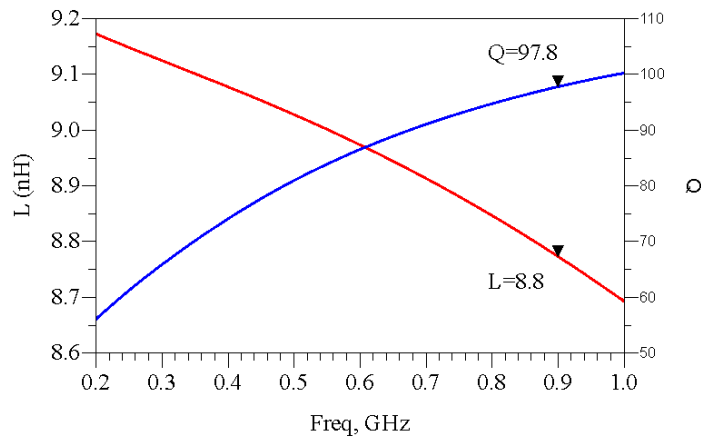


Figure 6.15 Simulated 8.9 nH side branch inductance.

To create the additional inductance approximately 4.5 nH needed from the location the main inductor structure was tapped for the 630 MHz configuration, the 15 mil Bottom layer conductor show in was used to rout the signal to the normal open relay contacts. Based on (6-1), a 15 mil wide trace with a length of ~250 mils has ~ 4.3 nH. A complete 3D view of the 630 MHz configuration side branch inductance structure is show in Figure 6.16 with the momentum simulation results shown in Figure 6.17.

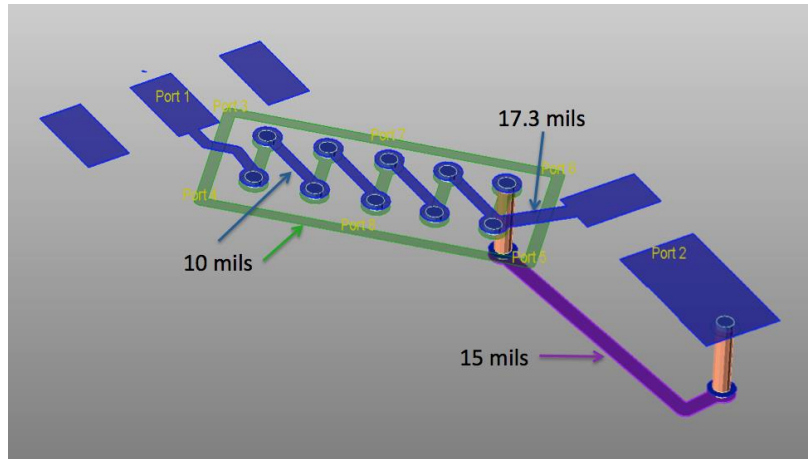


Figure 6.16 3D view of side branch inductance-630 MHz configuration.

This overall inductance ranges from 10.2 to 13 nH across the simulated frequency range with a good quality factor of approximately 97 at 630 MHz.

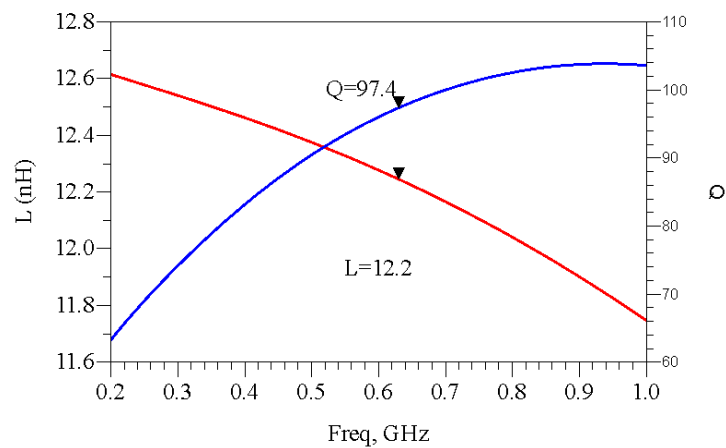


Figure 6.17 Simulated 12.4 nH side branch inductance.

### 6.2.1 Fabrication Feasibility Study

As a demonstration and evaluation of the process capability of Advanced Circuits PCB Fab, and the concept of inductors fabricated from PCB conductor traces, a layout was made for a 8.8 nH inductor as shown in Figure 6.18 using OrCAD.

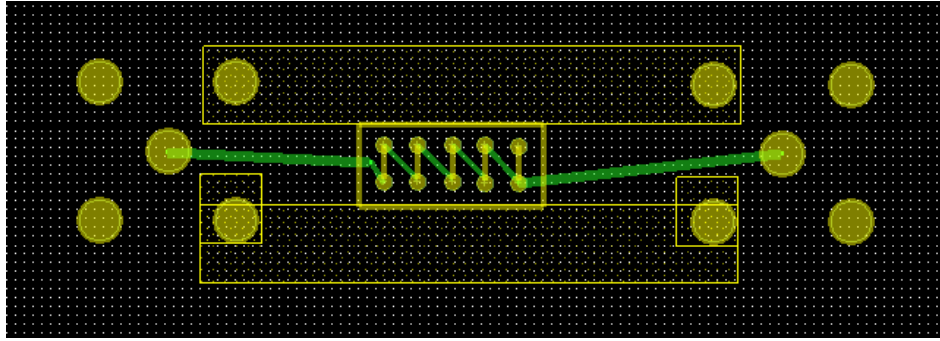


Figure 6.18 Orcad demo PCB inductor.

This inductor layout was extended to incorporate Lighthouse Technologies LTI-SASF54GT SMA connectors to provide ports for S-parameter measurements [6.6]. The top and bottom sides of the finished PCB are respectively shown in Figure 6.19 and Figure 6.20. It's worth noting that the conductor trace widths, which are important to the overall inductance, are fairly consistent, and that the via spacing is also excellent.

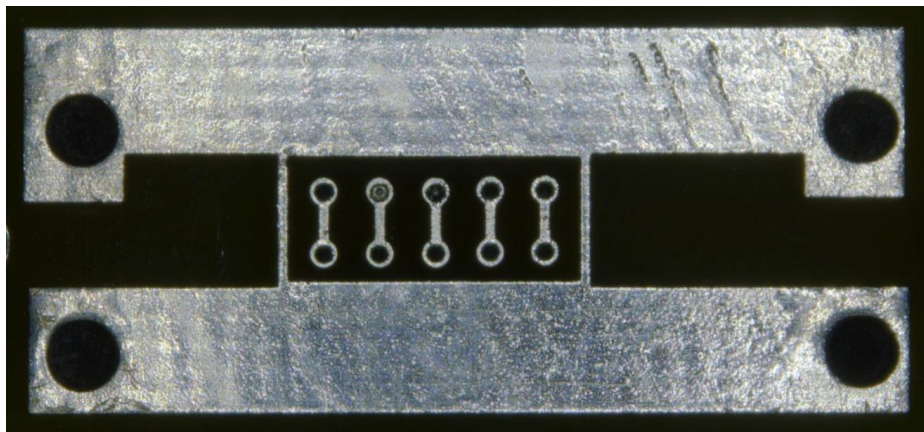


Figure 6.19 Top side view of demo PCB inductor.

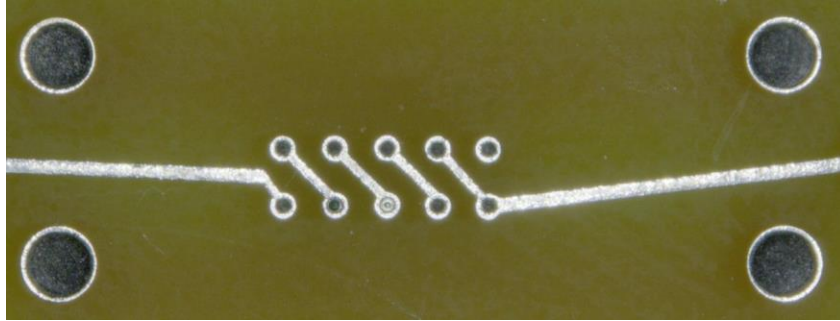


Figure 6.20 Bottom view of demo PCB inductor.

The measured and simulated inductance results are shown in Figure 6.21. The SMA connectors are not included in the simulation, nor de-embedded from the measurement data, with that in consideration, the results compare very well.

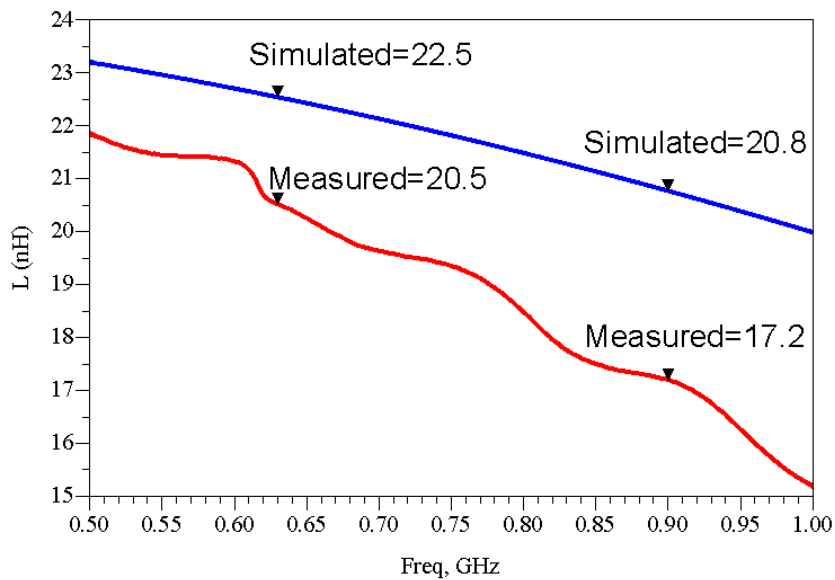


Figure 6.21 Measured and simulated demo pcb 8.8 nH inductance.

The measured Q values for the 8.8 nH inductor are shown in Figure 6.22, which don't directly match the simulated data. This is can be attributed to the fact that the measured data does not have the SMA connectors de-embed from the measurement. The SMA connectors on the input and output of the test board have very low Q, which when



combined with the high Q of the inductor, lower the overall Q. A confirmation of this theory can be seen in in Figure 6.23, which is a simulation with short coax sections to simulate the SMA connectors added to the input and output of the test inductor simulation. While the overall Q values do not agree perfectly, the effect of the SMA connectors is easily observed. With the good overall agreement of the simulated demo inductor, fabrication of the entire coupler was warranted.

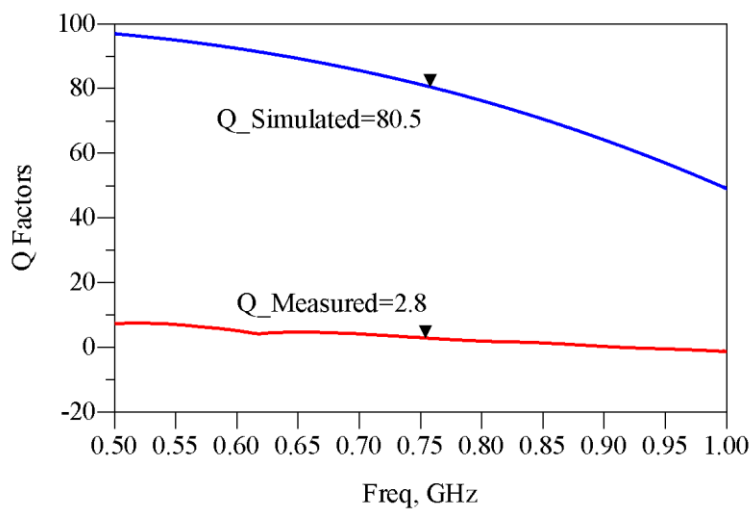


Figure 6.22 Measured and simulated demo pcb 8.8 nH Q.

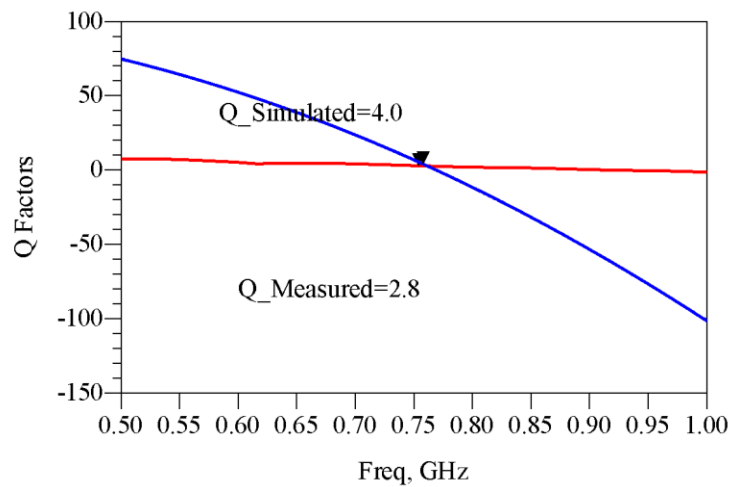


Figure 6.23 Measured and simulated inductor data including sma connector simulation.

### 6.3 Design of Switchable Capacitors

As previously stated, the design of the coupler requires 8.54 pF for the 630 MHz center frequency of operation and 12.2 pF for the 900 MHz frequency of operation. The capacitor layout was constructed such that the capacitance of the 900 MHz coupler, that is C1, was in the un-switched normally open state, which is approximately 6.2 pF at pin 5 of the Omron GY6 Relay, with the 8.93 pF capacitance obtained by switching in the additional capacitance needed by closing the contacts between pins 5 and 6, the 3D view of which is shown in Figure 6.24.

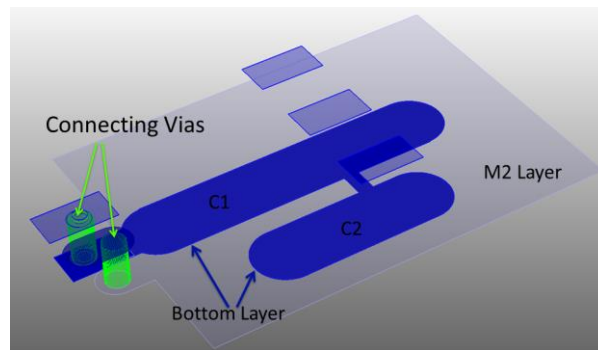


Figure 6.24 Switched capacitor layout 3D view.

The initial simulation results for C1 and C2 are shown in Figure 6.25 and Figure 6.26 respectively, it is worth noting that the Q values are approximately 94 for the 630 MHz capacitance, and approximately 109 for the 900 MHz capacitance. Furthermore; unlike the inductors, the capacitor values have are ill behaved and change significantly in value throughout of the frequency range of interest. Capacitor C1 ranges from 5.6 pF to 10.0 pF and capacitor C2 ranges from 8.3 pF to 25 pF.

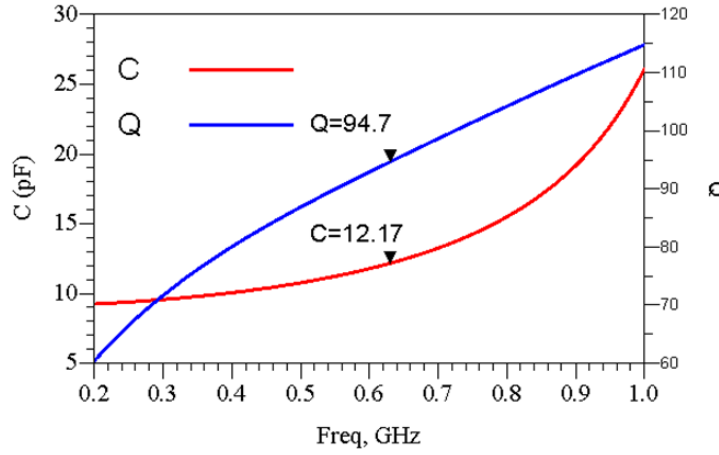


Figure 6.25 630 MHz capacitance vs. frequency.

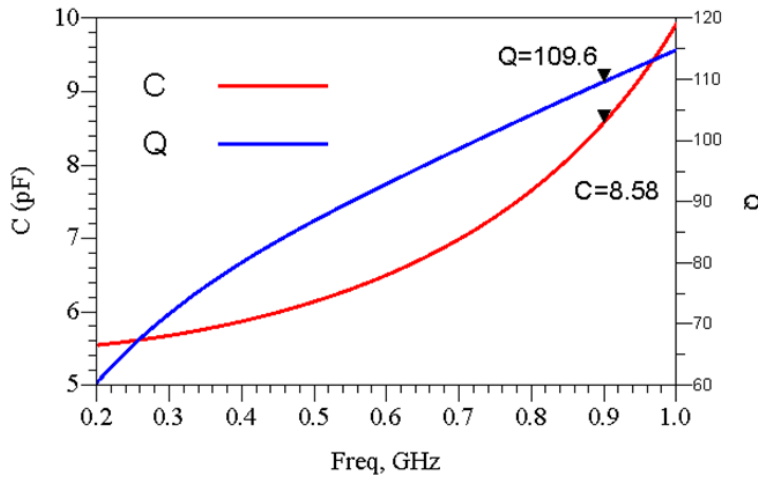


Figure 6.26 900 MHz capacitance vs. frequency.

### 6.4 Coupler Layout and Simulation

The final printed circuited board layout which shows both of the simulated couplers in Figure 6.27. For the purpose of this research, instead of using relays to select the desired frequency, the layout was duplicated with the appropriate relay pads shorted to represent the energized state, i.e. the 630 MHz circuit shown on the right, and the de-energized state, i.e. the 900 MHz circuit which is shown on the left.

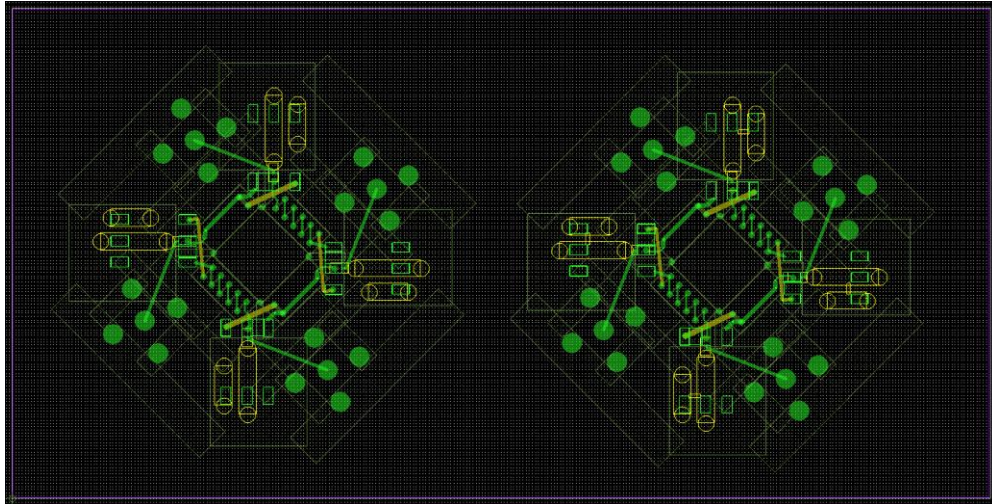


Figure 6.27 OrCAD drawing of dual channel hybrid coupler.

The final simulation of the 630 MHz configuration was carried out via the ADS with the coupler's S-parameter magnitude and phase response shown in Figure 6.28. As can be observed, the simulation produced a slight frequency error of 6 MHz, i.e. the center frequency was 624 MHz instead of the desired 630 MHz, but the overall performance is very good with near ideal performance.

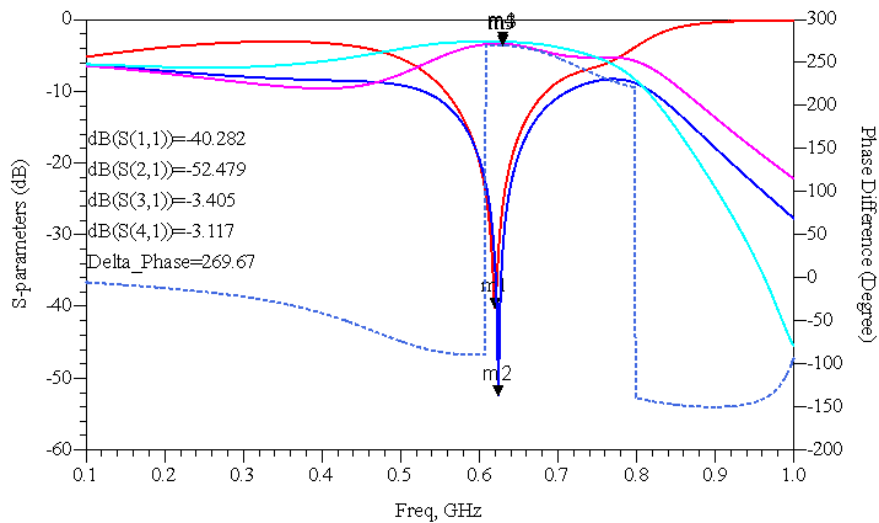


Figure 6.28 630 MHz coupler s-parameter magnitude response.

The 900 MHz configuration coupler's S-parameter magnitude and phase response shown in Figure 6.29. As can be observed, the simulation again produced a slight frequency error of 3 MHz, i.e. the center frequency was 887 MHz, instead of the desired 900 MHz, but the overall performance is very good with near ideal performance.

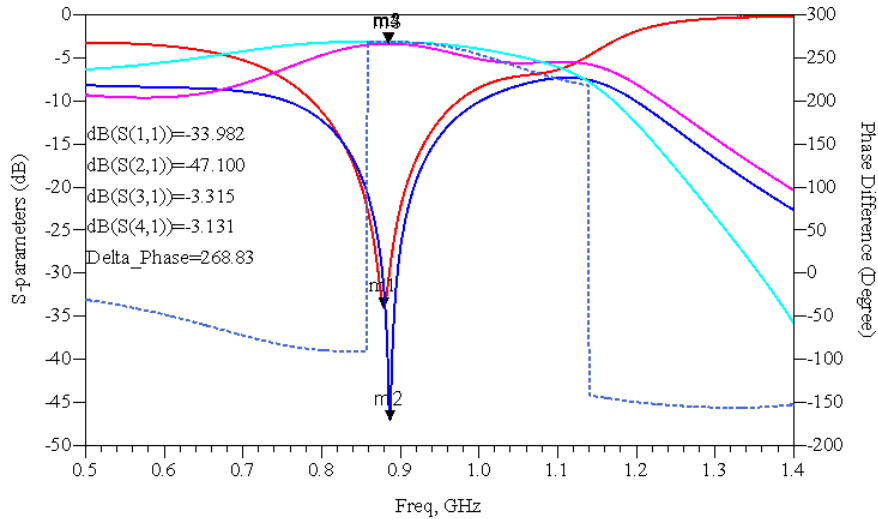


Figure 6.29 900 MHz coupler s-parameters magnitude and phase response.

## 6.5 Coupler Fabrication and Measurement

With satisfactory simulations, the Gerber Artwork files, and drill files were sent to Advanced Circuits Inc. for fabrication. The fabricated circuit board was mounted with the same SMA connectors used for the inductor feasibility test. Individual pictures of the 630 MHz 90° hybrid coupler and the 900 MHz 90° hybrid coupler, and are shown in Figure 6.30 and Figure 6.31. The only visible difference from these views being the short between the capacitor plates on the 630 MHz design compared with the open between the capacitor plates on the 900 MHz design.

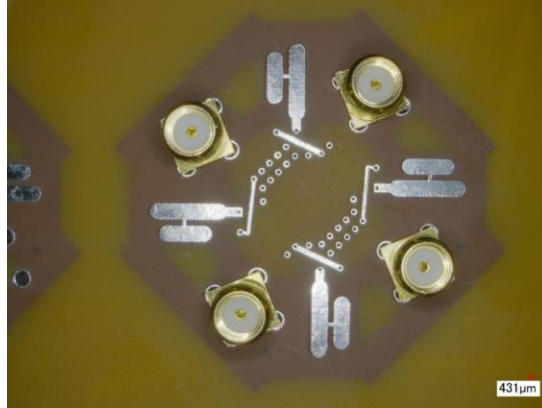


Figure 6.30 630 MHz coupler with SMA connectors.

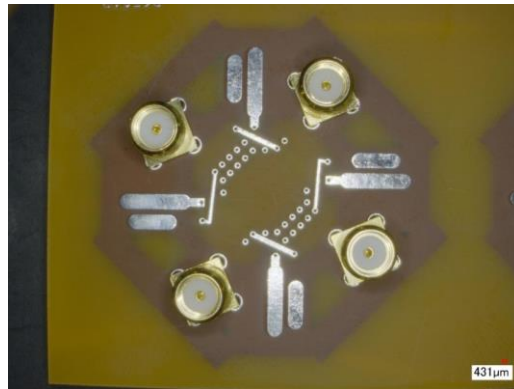


Figure 6.31 900 MHz coupler with SMA connectors.

S-parameter measurements of the 630 MHz and 900 MHz couplers were carried out using the Agilent Technologies E5071C Network Analyzer shown in Figure 6.32.



Figure 6.32 Agilent technologies E5071C network analyzer.

This particular analyzer has only a two-port measurement capability, the coupler being a four-port device required two channels to be terminated with  $50\ \Omega$  at the non-measured ports as can be observed in Figure 6.33.



Figure 6.33 Hybrid coupler measurement termination and connection.

The resulting S-parameter measurements for the 630 MHz and 900 MHz couplers are shown in Figure 6.34 and Figure 6.35 respectively. While the performance of both couplers in a qualitative sense are generally correct, that is to say the Isolation, Return Loss, and Coupling (approximately -4.0 dB at 870 MHz 1250 MHz each), are very good, the center frequencies of the couplers are up shifted  $\sim 240$  MHz for the 630 MHz coupler, and  $\sim 350$  MHz for the 900 MHz Coupler.

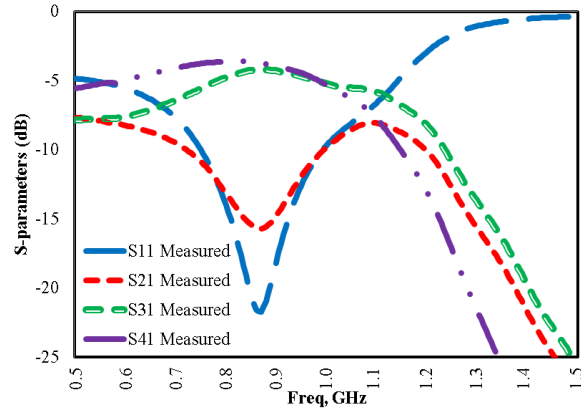


Figure 6.34 630 MHz coupler measured s-parameters.

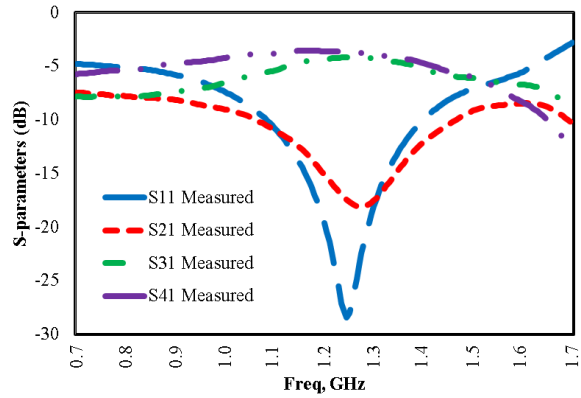


Figure 6.35 900 MHz coupler measured s-parameters.

As previously mentioned, the simulation and correlation of the inductances were verified with the small Demo-board discussed in 6.2.1 “Fabrication Feasibility Study”. With that in mind, the capacitance values are the most likely cause for investigation regarding correlation of the measured and simulated results. As has been repeatedly shown, the higher the design frequency of a hybrid coupler, the smaller capacitance values required. Hence, it is logical to assume that the resulting capacitors of the fabricated couplers are lower than what was simulated. The substrate thickness used for the capacitor design was 4.253 mils, as shown in Figure 6.7. Understanding that both couplers shifted, and the shift was somewhat proportional to the design frequency, new



simulations were carried out on the entire coupler design, but with the substrate thickness increased until a good correlation was reached for the original 630 MHz layout but with the design frequency now assumed to be 870 MHz. The final substrate thickness needed to adjust the center frequency to ~870 MHz was 10.25 mils as shown in Figure 6.36.

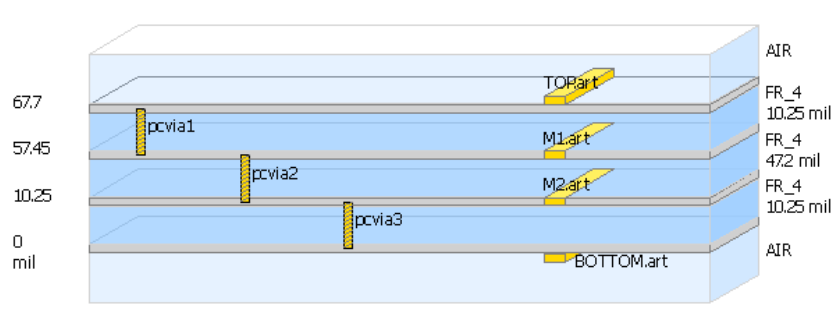


Figure 6.36 Updated PCB substrate for measurement correlation.

The updated 870 MHz layout simulation results are compared with the measured data in Figure 6.37 and Figure 6.38.

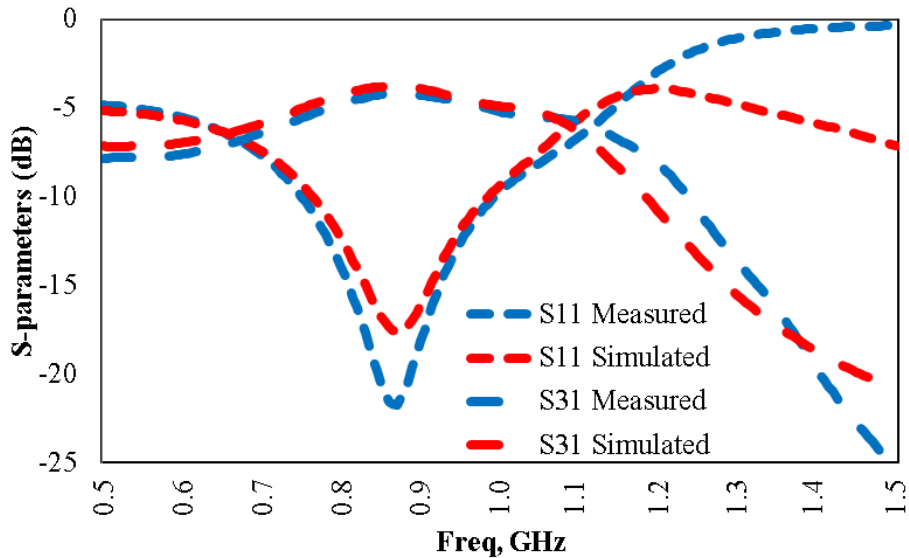


Figure 6.37 Correlated 870 MHz S11 and S31 data.

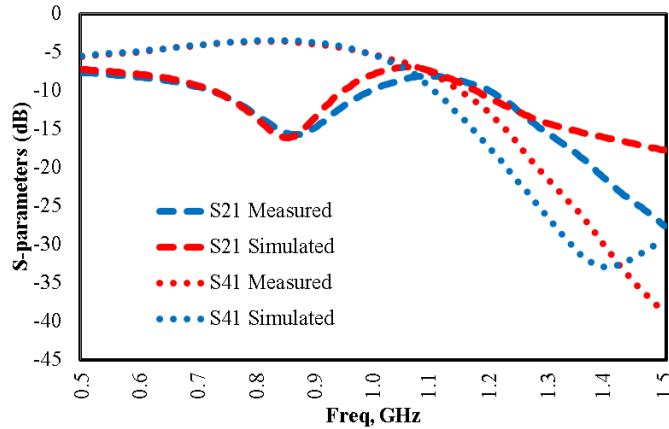


Figure 6.38 Correlated 870 MHz S21 and S41 data.

It's easily observed in the  $S_{11}$  and  $S_{21}$  data that the center frequencies are near identical, and agree very well with each other. Furthermore; the  $S_{31}$  and  $S_{41}$  data for the through and coupled ports also agree very well with each at the center frequency of operation and in general very good across the simulated and measured frequency range.

A key indicator of coupler performance is the desired phase shift between the coupled and through ports, in the case of the hybrid coupler is 90 or -270 degrees. The correlated phase difference, between the simulated and measured data is shown in Figure 6.39. As can be seen, at the center frequency of 870 MHz, the coupler has a phase shift of -270 degrees, and are near identical thus establishing the correlation of the new substrate for the 870 MHz layout.

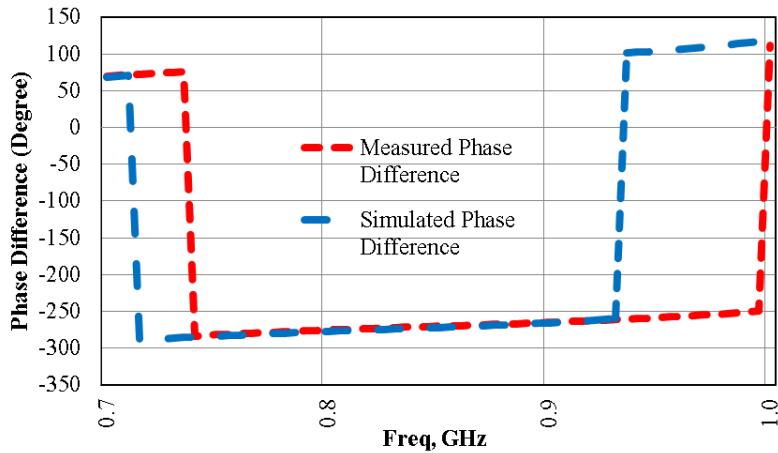


Figure 6.39 Correlated 870 MHz phase comparison.

The next issue to address is how well does the updated substrate correlated for the 900 MHz layout change to a 1250 MHz design. With that in mind, a momentum simulation was carried out with the updated substrate thickness, but with no other modifications to the original layout. The correlated results of the S-parameter magnitude data and Phase Difference are shown in Figure 6.40, Figure 6.41, and Figure 6.42 respectively.

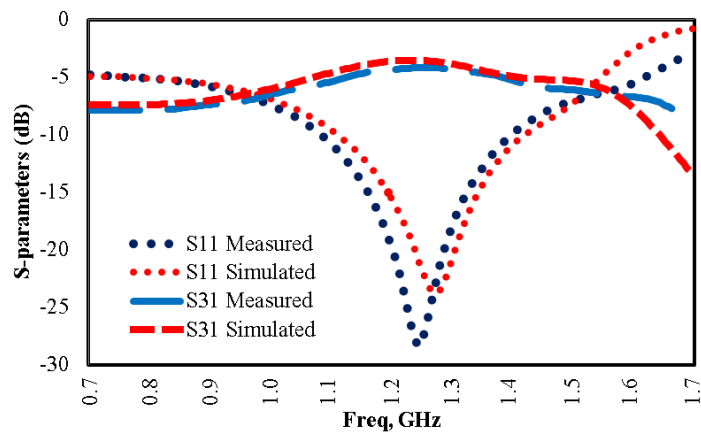


Figure 6.40 Correlated 1250 MHz S11 and S31 data.

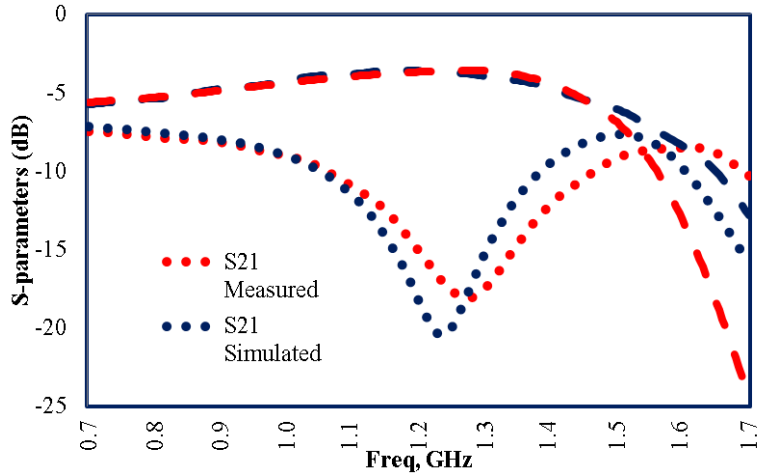


Figure 6.41 Correlated 1250 MHz S21 and S41 data.

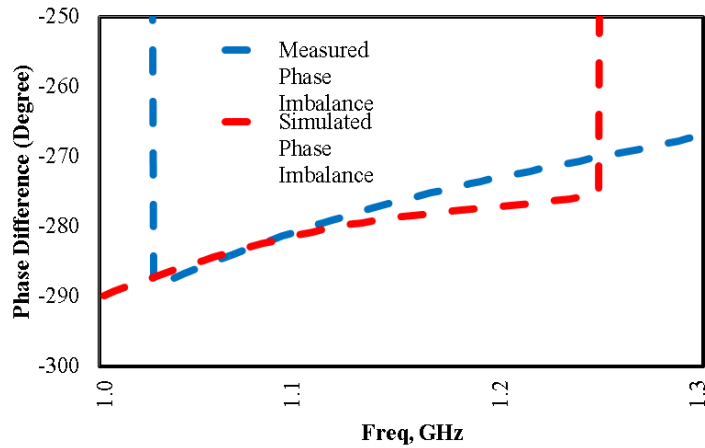


Figure 6.42 Correlated 1250 MHz phase comparison.

As in the case of the 870 MHz layout, the center frequency of the 1250 MHz layout correlates very well with the magnitude of the measured data. However, as can be seen at approximately 1250 MHz the measured data has an ideal phase difference of -270 degrees while the simulated data has a phase shift of approximately -270 degrees with a phase distortion of approximately 6 degrees.

It is interesting to note that, as in the numerous cited examples with fixed branch impedances, the hybrid coupler center frequency is adjustable by varying the total capacitance  $C_t$  while keeping the inductor values constant.

## **6.6 Conclusion**

The design, fabrication, and measurement of a dual-band lumped element hybrid coupler have been documented. It has been demonstrated that using low cost multilayer PCB fabrication technology to create printed capacitors and inductors, along with the utilization of standard off the shelf RF relays, it's possible to construct a switchable  $90^\circ$  lumped element branch-line hybrid coupler that functions well in the range of 500 MHz to 1.5 GHz with excellent phase performance and good magnitude balance [6.7].

## References

- [6.1] O. Gurbuz, G. Rebeiz, “A 1.6-2.3 GHz RF MEMS Re-configurable Quadrature Coupler and Its Application to a 360° Reflective-Type Phase Shifter”, *IEEE Transactions On Microwave Theory and Techniques*, vol. 63, no. 2, pp. 414-421, February 2014.
- [6.2] E. Djoumessi, E. Marsan, C. Caloz, M. Chaker, and K.E. Wu, “Varactor-Tuned Dual-Band Quadrature Hybrid Coupler”, *IEEE Microwave and Wireless Components and Letters*, vol. 16, no. 11, November 2006
- [6.3] OMRON G6K Data Sheet, “*Surface Mounting Relay with the World’s Smallest Mounting Area and Height of Only 5.2 mm*”.
- [6.4] Advanced Circuits Data Sheet, “*Polar Instruments Four-layer printed circuit board data sheet*”.
- [6.5] S. Hall, G. Hall, J. McCall, *High-Speed Digital System Design, A Handbook of Interconnect Theory and Design Practices*, John Wiley & Sons, 2000.
- [6.6] Lighthouse Technologies Incorporated LTI-SAS54GT Data Sheet.
- [6.7] T. Moss, Y. Chen, “A Compact Dual-Band Lumped Element 90° Hybrid Coupler on a 4-Layer PCB with Integrated Passive Components”, to be submitted to *IEEE Transactions on Microwave Theory and Techniques*. April 2015.

# **CHAPTER 7 CONCLUSIONS AND FUTURE WORK**

## **7.0 Introduction**

The research presented in this dissertation will be summarized, and discussed in this chapter with a view to future work than can be done with respect to the application of MEMS technology to tunable passive RF circuits, and passive circuit analysis and design techniques from both an education and practical design aspects.

## **7.1 Conclusions**

The main objective of this research was to further RF passive circuit design techniques through the study and application of MEMS switching and passive component technology by investigating potential benefits of MEMS switching vs. solid state switching in a  $90^\circ$  lumped element quasi-tunable hybrid coupler design based high Q solenoidal MEMS inductors, as well as develop passive circuit analysis techniques that predict the required Q to meet the specified S-parameters from a design perspective. To that end, the following tasks were accomplished.

1. A systematic approach has been developed and presented for deriving the S-parameters of any generalized lumped element circuit in terms of inductor Q, as well as the inverse functions on a restricted domain. This was accomplished through a novel application of the mesh current methodology to a four-port

- passive circuit in combination with even and odd mode circuit analysis techniques.
2. The application of MEMS switching and passive component technology was investigated through the design of two, 2.0 to 3.0 GHz  $90^\circ$  lumped element quasi-tunable hybrid coupler designs utilizing tapped solenoidal air-core inductors and tapped IPD capacitors. The two designs differed in the tapped capacitors being signal switched vs. ground switched, the latter of which was developed to maximize the capacitor Q in the circuit design, and optimize the performance of the circuit with a complete layout.
  3. A performance comparison was made between MEMS switched hybrid coupler and a RF PIN Diode to determine from an engineering point of view which technology is most effective in the application of a quadrature coupler design. It was determined that from a phase balance perspective, RF PIN Diodes can perform equally as well as MEMS switching even with low forward-bias current levels. On the other hand, applications that are sensitive to amplitude imbalance, e.g. OFDM I/Q demodulators, MEMS switching can provide 0.2~0.3 dB improvement in the signal distortion chain.
  4. A printed circuit board dual-band  $90^\circ$  lumped element quasi-tunable hybrid coupler using integrated passive components was designed, fabricated, and measured. Simulation and correlation with the measured results show that compact low cost re-configurable hybrid couplers can be fabricated on PCB technology using printed traces as inductors and capacitors.



## 7.2 Future Work

The concept of developing S-parameters as a function of component Q can be extended in the fields of electrical engineering education and RF circuit design. For example, it lends itself naturally to mesh current analysis of two-port filter designs, and aids in the understanding of why a circuit does not meet its design criteria. Furthermore; since the equations can be implemented in any simple math environment, e.g. MATLAB, students are generally familiar with what is needed to accomplish the task.

From a more advanced engineering design aspect, sophisticated tools that provide filter design aides, e.g. “Agilent ADS Filter Design Guide”, typically do not incorporate non-ideal component Q into their simulations and performance predictions. Filter design topologies, e.g. traditional “Ladder Synthesis” that are used to build filter designer tools could be updated to include Q factors for more realistic predictions.

To date, most of the research in tunable  $90^\circ$  lumped element hybrid coupler designs are geared toward circuits that have fixed inductances. This leads to decreased performance at frequencies other than that of the inductors design frequency. Research in the application of quasi-tunable spiral inductors, which can cover the 400 MHz to 3700 MHz range at the industry standard operation frequencies, in combination with MEMS switching could be valuable in the wireless communication industry.

As mentioned in Chapter 5, practical assembly aspects of this concept study were not taken into account. Neither were the activation aspects of switching the tunable inductor/capacitor banks. Research into packaging IPD capacitors and spiral inductors with MEMS switches would be a logical step to investigating practical implementations of this design concept. From a simulation point of view, addition of switching

conductors could be accomplished in Agilent ADS to further account for layout considerations. As an example layout concept, consider Figure 7.1 where the control signals for each coupler channel are shown, as well as the connections to the pull down electrodes required for each inductor/capacitor switch pair.

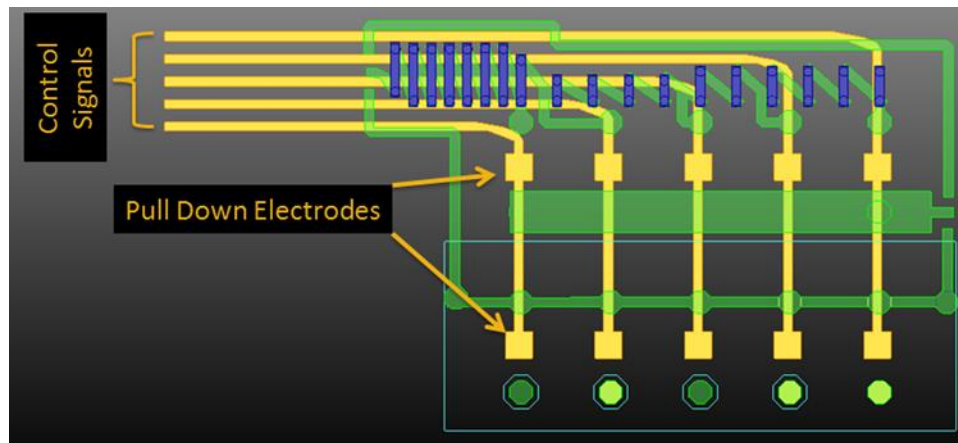


Figure 7.1 Tunable inductor/capacitor bank with control signal interconnects.

More accurate simulations to fully take into account cross-talk with physical switch designs, switching conductors, in a layout that incorporates the IPD capacitor, and three-dimensional air-core inductor designs would be better suited for 2.5D simulators, e.g. Ansoft HFSS.

The proposed design in this dissertation was not optimized from a switch count point of view. Investigation into switch topologies, e.g. a variation on a series-capacitive shunt switch might be a solution to eliminate the MIM capacitor, as well as the number of switches.

Recent research and publication in the area of re-configurable quadrature couplers on PCB technology demonstrates there are still areas open for further investigation. Advanced modern PCB fabrication has trace with capabilities down to at least 1.25 mils.

This research implies that higher frequency coupler designs are possible when combined with smaller surface mount MEMS RF switching relays, e.g. Radant MEMS.

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# Appendix A: Derivation of 90° Lumped Element Hybrid Coupler S-Parameters via Mesh Analysis

This section develops the theoretical relationships between inductor quality-factor, or inductor “Q” and the corresponding frequency response of the 90° Lumped Element Hybrid Coupler. Analytic equations, and their associated inverse functions, that directly relate a hybrid coupler’s output to a given inductor Q-factor are derived. These equations are derived based on the concept of even mode and odd mode inductor Q which are used to describe the hybrid coupler’s corresponding even mode and odd mode output S-parameters.

The first set of equations to be derived are the even mode S-parameters  $S_{21e}$  as a function of even mode inductor quality factor  $Q_e(S_{21e})$ , and its inverse function  $S_{21e}(Q_e)$ . Consider the lumped element implementation of the 90° branch line coupler in Figure A-1 with voltages V1 through V4.

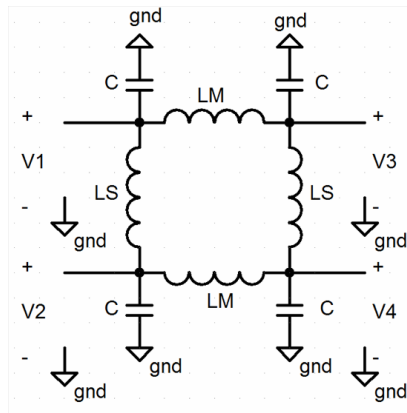


Figure A.1 Lumped element 90° coupler.

In this analysis, Port 1 is the driven port, Port 2 is the isolated port with no output in an ideal circuit, Port 3 is the through port, and Port 4 is the coupled port with a  $90^\circ$  phase shift between ports 3 and 4. Mesh current analysis of the coupler in its standard form is very complicated, hence to simplify the analysis, the coupler is broken into even and odd mode circuits where the coupler outputs can be represented as in (A-1) and (A-2) [19].

$$S_{31} = \frac{1}{2}(S_{21e} + S_{21o}) \quad (\text{A-1})$$

$$S_{41} = \frac{1}{2}(S_{21e} - S_{21o}) \quad (\text{A-2})$$

To obtain the even and odd mode circuits, the normalized input at V1 of 1V is split into common mode voltages of  $V1 = V2 = 1/2$ . The same voltage applied to ports 1 and 2 means there is no current flow across the input side branch inductor LS. The circuit also being symmetrical, and with a reciprocal response with ports 3 and 4 as the driven ports means that the output side branch inductor also experiences no current flow. Consequently both side branch inductors can be removed from the circuit since there is no current flow through them. This results in the simplified even mode circuit of Figure A-2.

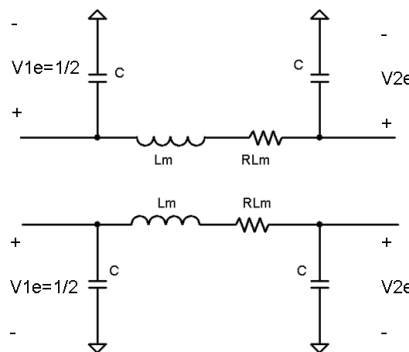


Figure A.2 Simplified even mode lumped element  $90^\circ$  coupler.

It is important to notice that the parasitic series resistance of the main branch inductors  $R_{LM}$  has been included for completeness, and use in further analysis.

To facilitate the mesh current analysis of the even mode coupler circuit, one half of the even mode circuit of Figure A-2 has been expanded in Figure A-3 to include the load termination resistance  $R_{Term}$  and a source  $V_G = 1V$ .

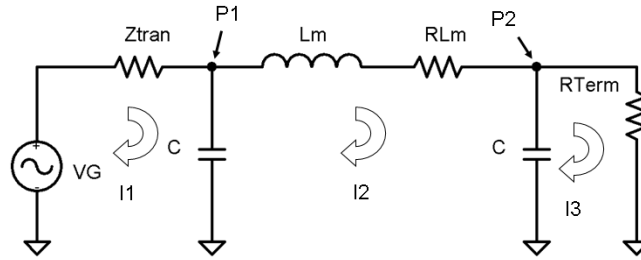


Figure A.3 Even mode circuit mesh analysis.

Writing the mesh currents using Kirchhoff's Voltage Law results in the system of equations stated in (A-3) through (A-5).

$$I_1 Z_{tran} + (I_1 - I_2) Z_C = 1V \quad (A-3)$$

$$(I_2 - I_1) Z_C + I_2 Z_{LM} + (I_2 - I_3) Z_C = 0 \quad (A-4)$$

$$(I_3 - I_2) Z_C + I_3 Z_{term} = 0 \quad (A-5)$$

This system of equations is of the form  $I||=|Z|^{-1}|V|$ , hence transforming the mesh equations results into matrix/vector form results in the matrix equation of (A-6).

$$\begin{vmatrix} I_1 \\ I_2 \\ I_3 \end{vmatrix} \begin{vmatrix} Z_{tran} + Z_C & -Z_C & 0 \\ -Z_C & 2Z_C + Z_{LM} & -Z_C \\ 0 & -Z_C & Z_C + R_{term} \end{vmatrix} = \begin{vmatrix} VG \\ 0 \\ 0 \end{vmatrix} \quad (A-6)$$

Assuming  $V_G=1V$ , and then solving for the mesh currents  $I_1 \sim I_3$  results in the current vector of (A-7).

$$\begin{matrix} |I_1| \\ |I_2| \\ |I_3| \end{matrix} = \begin{matrix} \frac{(2Z_C + Z_C^2 + Z_L + Z_L Z_C)}{(1 + Z_C)(2Z_C + Z_L Z_C + Z_L)} \\ \frac{Z_C}{2Z_C + Z_L Z_C + Z_L} \\ \frac{Z_C^2}{(1 + Z_C)(2Z_C + Z_L Z_C + Z_L)} \end{matrix} \quad (\text{A-7})$$

Recall that in the case of the full coupler analysis with ideal inductor Q, i.e.  $R_{LM} = 0$ , the input impedance to the coupler must match that of the input transmission line for  $S_{11}$  to be zero in magnitude. With that being the case, the same is assumed to be true for the even mode circuit with ideal Q. Assuming then that the even mode circuit is normalized, i.e.  $R_{term} = 1$ , and  $Z_{tran} = 1$ ,  $S_{21e}$  is simply  $I_3$  divided by one half the magnitude of the voltage source VG, which means  $S_{21e}$  can be stated as in (A-8).

$$S_{21e} = \frac{2Z_C^2}{(1 + Z_C)(2Z_C + Z_L Z_C + Z_L)} \quad (\text{A-8})$$

As can be observed, only the inductive impedances  $Z_L$  and capacitive impedance  $Z_C$  are contained in (A-8). Therefore, to express  $S_{21e}$  in terms of  $Q_e$ ,  $Z_L$  must be expressed in terms of  $Q_e$ . To accomplish this recall that the series impedance for the even mode circuit inductor is given by (A-9).

$$Z_L = j\omega L_M + R_{LM} \quad (\text{A-9})$$

Next recall that the definition of inductor Q is defined as in (A-10), which can be restated as in (A-11).

$$Q \equiv \frac{\omega L}{R} \quad (\text{A-10})$$

$$R \equiv \frac{\omega L}{Q} \quad (\text{A-11})$$

Furthermore; in the case of the  $90^\circ$  lumped element hybrid coupler, the normalized main branch impedance is defined as in (A-12).

$$j\omega L_M = \frac{j}{\sqrt{2}} \quad (\text{A-12})$$

Then expressing the even mode inductive impedance  $Z_L$  in terms of  $Q_e$  is resolved by substituting (A-11) and (A-12) into (A-9) and is given by (A-13).

$$Z_L = \frac{1}{\sqrt{2}Q_e} + j\frac{1}{\sqrt{2}} \quad (\text{A-13})$$

Substituting (A-13) into (A-8), and solving for  $S_{21e}$  as a function of  $Q_e$  leads to (A-14), which is the desired relationship for the even mode S-parameters in terms of the even mode  $Q$ .

$$S_{21e} = \frac{2Z_C^2}{(1 + Z_C) \left( 2Z_C + \frac{1}{\sqrt{2}Q_e} + j\frac{1}{\sqrt{2}}(Z_C + 1) \right)} \quad (\text{A-14})$$

To derive the even mode  $Q_e$  that is necessary for a specified even mode S-parameter  $S_{21e}$ , and eliminate the denominator to rearrange (A-14) to obtain (A-15).

$$\frac{S_{21e}}{2} \left( \left( \frac{1}{\sqrt{2}Q_e} + j\frac{1}{\sqrt{2}} \right) (Z_C^2 + 2Z_C + 1) \right) + \frac{S_{21e}}{2} (2Z_C^2 + 2Z_C) = Z_C^2 \quad (\text{A-15})$$

To solve for  $Q_e$  in terms of  $S_{21e}$ , substitute (A-16) and (A-17) into (A-15) which results in (A-18).



$$A = Z_C^2 + 2Z_C + 1 \quad (\text{A-16})$$

$$B = (2Z_C^2 + 2Z_C) \quad (\text{A-17})$$

$$\frac{S_{21e}}{2} \left( \frac{1}{\sqrt{2}Q_e} + j \frac{1}{\sqrt{2}} \right) A + \frac{S_{21e}}{2} B = Z_C^2 \quad (\text{A-18})$$

For further simplification consider the algebraic manipulations of (A-19) and (A-20) which lead to (A-21).

$$\frac{S_{21e}A}{2} \frac{1}{\sqrt{2}Q_e} + j \frac{S_{21e}A}{2} \frac{1}{\sqrt{2}} = Z_C^2 - \frac{S_{21e}}{2} B \quad (\text{A-19})$$

$$j \frac{Q_e S_{21e}A}{\sqrt{2}} + \frac{S_{21e}A}{2\sqrt{2}} = Q_e \left( Z_C^2 - \frac{S_{21e}}{2} B \right) \quad (\text{A-20})$$

$$j \frac{Q_e S_{21e}A}{\sqrt{2}} + Q_e \left( \frac{S_{21e}}{2} B - Z_C^2 \right) = -\frac{S_{21e}A}{2\sqrt{2}} \quad (\text{A-21})$$

Solving (A-21) for  $Q_e$  in terms of  $S_{21e}$  results in (A-22), which is the desired relationship.

$$Q_e = \frac{1}{\frac{2\sqrt{2}}{S_{21e}A} Z_C^2 - \frac{\sqrt{2}B}{A} - j} \quad (\text{A-22})$$

As in the case of the even mode derivations, mesh current analysis will be used to determine the frequency response of the odd mode circuit. Consider the expanded odd mode mesh analysis circuit as shown in Figure A-4 with a source generator of  $V_G=1V$ , an input transmission line impedance of  $Z_{\text{tran}}$ , and a load termination  $R_{\text{term}}$ .

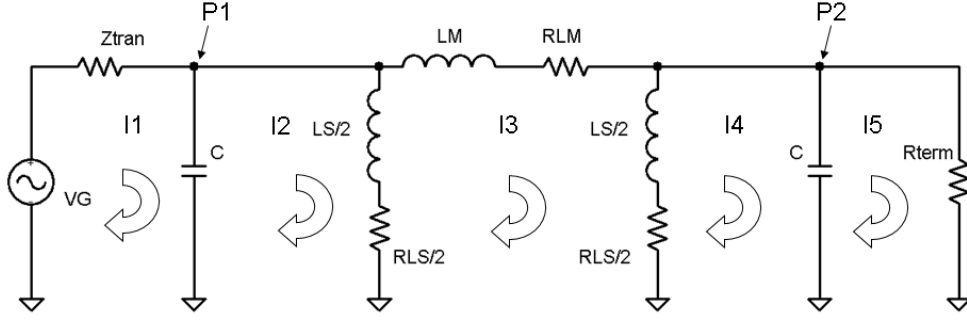


Figure A.4 Odd mode mesh current analysis circuit.

Writing the mesh current equations for  $I_1$  through  $I_5$  of Figure A-4 using Kirchoff's voltage law result in the system of equations of (A-23) through (A-27), which are expressed in matrix/vector form in (A-28).

$$I_1 Z_{tran} + (I_1 - I_2) Z_C = IV \quad (A-23)$$

$$(I_2 - I_1) Z_C + (I_2 - I_3) Z_{LS} = 0 \quad (A-24)$$

$$(I_3 - I_2) Z_{LS} + I_3 Z_{LM} + (I_3 - I_4) Z_{LS} = 0 \quad (A-25)$$

$$(I_4 - I_3) Z_{LS} + (I_4 - I_5) Z_C = 0 \quad (A-26)$$

$$(I_5 - I_4) Z_C + I_5 Z_{term} = 0 \quad (A-27)$$

$$\begin{pmatrix} (Z_{tran} + Z_C) & -Z_C & 0 & 0 & 0 \\ -Z_C & (Z_C + Z_{LS}) & -Z_{LS} & 0 & 0 \\ 0 & -Z_{LS} & (2Z_{LS} + Z_{LM}) & -Z_{LS} & 0 \\ 0 & 0 & -Z_{LS} & (Z_{LS} + Z_C) & -Z_C \\ 0 & 0 & 0 & -Z_C & (Z_C + Z_{term}) \end{pmatrix} = \begin{pmatrix} IV \\ 0 \\ 0 \\ 0 \\ 0 \end{pmatrix} \quad (A-28)$$

To solve for the mesh currents  $I_1$  through  $I_5$ , take  $|I| = Z^{-1}V$ , which when solved results in the current vector of (A-29).

$$\bar{I} = \left| \begin{array}{l} \frac{(Z_C^2(Z_{LS}^2 + 2Z_{LS} + Z_{LM} + Z_{LS}Z_{LM}) + Z_C(Z_{LS}^2Z_{LM} + 2Z_{LS}^2 + 2Z_{LS}Z_{LM}) + Z_{LM}Z_{LS}^2)}{(Z_C + Z_CZ_{LS} + Z_{LS})(Z_CZ_{LS}Z_{LM} + 2Z_CZ_{LS} + Z_CZ_{LM} + Z_{LS}Z_{LM})} \\ \frac{Z_C^2(Z_{LS}^2 + 2Z_{LS} + Z_{LM} + Z_{LS}Z_{LM}) + Z_C(Z_{LS}^2 + Z_{LS}Z_{LM})}{(Z_C + Z_CZ_{LS} + Z_{LS})(Z_CZ_{LS}Z_{LM} + 2Z_CZ_{LS} + Z_CZ_{LM} + Z_{LS}Z_{LM})} \\ \frac{Z_CZ_{LS}}{(Z_CZ_{LS}Z_{LM} + 2Z_CZ_{LS} + Z_CZ_{LM} + Z_{LS}Z_{LM})} \\ \frac{Z_C^2Z_{LS}^2(1 + Z_C)}{(Z_C + Z_CZ_{LS} + Z_{LS})(Z_CZ_{LS}Z_{LM} + 2Z_CZ_{LS} + Z_CZ_{LM} + Z_{LS}Z_{LM})} \\ \frac{Z_C^2Z_{LS}^2}{(Z_C + Z_CZ_{LS} + Z_{LS})(Z_CZ_{LS}Z_{LM} + 2Z_CZ_{LS} + Z_CZ_{LM} + Z_{LS}Z_{LM})} \end{array} \right| \quad (\text{A-29})$$

Once again, in the same manner as the even mode circuit evaluation, if we assume that the odd mode circuit is normalized, i.e.  $Z_{tran} = 1$ , and  $Z_{term} = 1$ , then as with the even mode circuit,  $Z_{in}$  looking into P1 is the same as  $Z_{tran}$ , therefore  $S_{21o}$  can be interpreted directly from the current  $I_5$  as (A-29) divided by one half of the source VG's magnitude, i.e.  $1V/2$  which given by (A-30).

$$S_{21o} = \frac{2Z_C^2Z_{LS}^2}{(Z_C + Z_CZ_{LS} + Z_{LS})(Z_CZ_{LS}Z_{LM} + 2Z_CZ_{LS} + Z_CZ_{LM} + Z_{LS}Z_{LM})} \quad (\text{A-30})$$

In a similar technique as was utilized with the even mode circuit, expressing the odd mode circuit inductive impedances  $Z_{LS}$  and  $Z_{LM}$  in terms of  $Q_o$  results in (A-31) and (A-32) respectively.

$$Z_{LS} = \frac{j + Q_o^{-1}}{2} \quad (\text{A-31})$$

$$Z_{LM} = \sqrt{2}Z_{LS} = \frac{\sqrt{2}(j + Q_o^{-1})}{2} = \frac{(j + Q_o^{-1})}{\sqrt{2}} \quad (\text{A-32})$$

An initial expression of  $S_{21o}$  in terms of  $Q_o$  is obtained by substituting equations (A-31) and (A-32) into (A-30) which result in (A-33).

$$S_{21o} = \frac{2Z_C^2 \left( \frac{j+Q_o^{-1}}{2} \right)^2}{\left( Z_C + \frac{j+Q_o^{-1}}{2} (Z_C+1) \right) \left( Z_C \frac{(j+Q_o^{-1})^2}{2\sqrt{2}} + 2Z_C \frac{j+Q_o^{-1}}{2} + Z_C \frac{j+Q_o^{-1}}{\sqrt{2}} + \frac{(j+Q_o^{-1})^2}{2\sqrt{2}} \right)} \quad (\text{A-33})$$

Further algebraic manipulation and simplification results in (A-34) which is the expression of  $S_{21o}$  in terms of  $Q_o$ .

$$S_{21o}(Q_o) = \frac{Z_C^2}{\left( Z_C + \frac{j+Q_o^{-1}}{2} (Z_C+1) \right) \left( Z_C \frac{1}{\sqrt{2}} + \frac{Z_C}{j+Q_o^{-1}} (2+\sqrt{2}) + \frac{1}{\sqrt{2}} \right)} \quad (\text{A-34})$$

To express the odd mode quality factor  $Q_o$  as an expression of the odd mode S-parameters  $S_{21o}$ , expand the denominator of (A-34) as stated in (A-35).

$$S_{21o} = 2Z_C^2 Z_{LS}^2 / Z_C^2 Z_{LS} Z_{LM} + 2Z_C^2 Z_{LS} + Z_C^2 Z_{LM} + 2Z_C Z_{LS} Z_{LM} + Z_C^2 Z_{LS}^2 Z_{LM} + 2Z_C^2 Z_{LS}^2 + 2Z_C Z_{LS}^2 Z_{LM} + 2Z_C Z_{LS} \quad (\text{A-35})$$

Recall that  $Z_{LM} = \sqrt{2}Z_{LS}$ , then the elimination of  $Z_{LM}$  in (A-35) results in (A-36).

$$S_{21o} = 2Z_C^2 Z_{LS}^2 / \sqrt{2}Z_C^2 Z_{LS}^2 + 2Z_C^2 Z_{LS} + \sqrt{2}Z_C^2 Z_{LS} + 2\sqrt{2}Z_C Z_{LS}^2 + \sqrt{2}Z_C^2 Z_{LS}^3 + 2\sqrt{2}Z_C^2 Z_{LS}^3 + 2\sqrt{2}Z_C Z_{LS}^3 + 2Z_C Z_{LS} \quad (\text{A-36})$$

Let  $a = Z_C$ , and  $b = Z_{LS}$ , then (A-36) can be restated as in (A-37)

$$S_{21o} = I_5 = 2a^2b/\sqrt{2}a^2b + 2a^2 + \sqrt{2}a^2 + 2\sqrt{2}ab + \sqrt{2}a^2b^2 + 2\sqrt{2}a^2b^2 + 2\sqrt{2}ab^2 + 2a \quad (\text{A-37})$$

To eliminate  $b$  from (A-37), express  $b$  and  $b^2$  in terms of  $Q_o$  as stated in (A-38) and (A-39).

$$b = \frac{j+Q_o^{-1}}{2} \quad (\text{A-38})$$

$$b^2 = \frac{-1 + 2jQ_o^{-1} + Q_o^{-2}}{4} \quad (\text{A-39})$$

Substituting and in (A-38) and (A-39) into (A-37), and setting the polynomial equal to zero creates a quadratic equation in terms of  $Q_o$  as in (A-40) with the coefficients A,B, and C as stated in (A-42), (A-43), (A-44) and (A-44) respectively.

$$S_{21o}(Q_o) = \text{Realroot}(AQ_o^2 + BQ_o + C) \quad (\text{A-40})$$

$$A = S_{21o} \left( \left( \frac{-\sqrt{2}(a+1)^2}{4} \right) + (2 + \sqrt{2})a^2 + j \left( (1 + \sqrt{2})(a^2 + a) - \frac{a^2}{S_{21o}} \right) \right) \quad (\text{A-41})$$

$$B = S_{21o} \left( (1 + \sqrt{2})(a^2 + a) - \frac{a^2}{S_{21o}} + \left( \frac{j2\sqrt{2}(a+1)^2}{4} \right) \right) \quad (\text{A-42})$$

$$C = S_{21o} \left( \frac{-\sqrt{2}(a+1)^2}{4} \right) \quad (\text{A-43})$$

$$a = Z_C = \frac{1}{j(1 + \sqrt{2})} \quad (\text{A-44})$$