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ENGINEERING MODEL OF III-NITRIDE POWER HETEROSTRUCTURE FIELD EFFECT TRANSISTOR ON SILICON SUBSTRATE

by

Mohammad Mirwazul Islam

Bachelor of Science
University of Dhaka, 2009

Master of Science
University of Dhaka, 2010

Submitted in Partial Fulfillment of the Requirements

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College of Engineering and Computing

University of South Carolina

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Accepted by:

Grigory Simin, Major Professor

Guoan Wang, Committee Member

MVS Chandrashekhar, Committee Member

Jamil A. Khan, Committee Member

Cheryl L. Addy, Vice Provost and Dean of the Graduate School

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DEDICATION

This dissertation is dedicated to the three most important women in my life; my late mother, sister and my wife. Without my mother's blessings and sister's sacrifices, I would never be able to come this far. Finally, without the support, encouragement and patience of my wife in the last 4 years, this work would not be possible.

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ABSTRACT

In modern society, the demand for power consumption is increasing rapidly and the need of energy savings is now an issue of global importance. Highly efficient power converters and power conditioning systems operating with wide range of traditional as well as novel renewable and clean energy sources, are playing crucial role in energy saving. Si converters have already reached their limitation in terms of switching frequency and breakdown voltage/on-resistance ratio. Research is going on all around the world and it is now well accepted that significant improvement in power conversion efficiency and speed can only be achieved using beyond Si devices, such as SiC and GaN based. GaN based converters have shown great promises for higher conversion efficiency and switching speed. It is now crucial to develop accurate models that can assist in design and fabrication of GaN based power electronics.

There are models for GaN HFETs. But these models are mainly focused on GaN HFET applications in RF power amplifiers. Although certain device characteristics (e.g. 2DEG density, power gain, cut-off frequencies etc.) are accurately estimated by existing models, currently there is no complete model usable in power electronics circuit/system simulators. In this work, we have developed a hybrid physics based/empirical compact model that describes the behavior of GaN HFETs in power switching high current, high voltage circuits. The complete model includes different modules from existing models that are suitable for GaN HEMTs for power switching applications and incorporate

models that are non-existent but crucially important for power switching applications such as current collapse and bulk current.

The Charge-Control-model can reproduce both above-threshold and subthreshold current-voltage and transient characteristics of GaN based power HFET's over a wide temperature range. The current–voltage (I-V) characteristics are described by a single, continuous, analytical expression for all regimes of operation, thereby improving convergence. The semi-empirical model includes effects such as velocity saturation in the channel, saturation of sheet carrier density, drain-induced barrier lowering (DIBL), self-heating, field plate effects, current collapse, substrate current and temperature dependence. Extensive TCAD simulations have been performed using a novel approach to investigate the mechanisms of bulk current and based on the results, a simple but accurate compact model for bulk current has been developed. The model is implemented using Verilog-AMS Hardware Description Language and extensively verified against a variety of experimental data for various HFET devices. This model does not require detail layer by layer device structure or technology because it uses directly measurable parameters.

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CHAPTER 1

INTRODUCTION TO MODELING III-NITRIDE HFETS

1.1 Background

In modern society, the demand for power consumption is increasing rapidly and the need of energy savings is now an issue of global importance. Highly efficient power converters and power conditioning systems operating with wide range of traditional as well as novel renewable and clean energy sources, are playing crucial role in energy saving. If power converter efficiency could be increased just by 5%, it would result an energy savings of 178 billion kilowatt-hours of electrical energy annually [1]. The equivalent dollar value of this savings is around $18 Billion a year assuming average electricity cost of $0.1/kWhr.

However, efficiency improvement can hardly be achieved by Si converters because of the limitations in breakdown voltage/on-resistance ratio and switching frequency imposed by material properties. It is now widely accepted that power converter efficiency and speed can only be improved using devices based on other materials than Si, such as SiC- and GaN. Research is going all around the world and GaN based converters with efficiency as high as 95% at 1 MHz clock frequency has been demonstrated by a number of research groups (see, e.g. [2]). GaN technology is attracting more and more attention day by day and the development of accurate models that can assist in design and fabrication of GaN based power electronics is becoming very urgent.

Existing MOSFET models for Si may appear to be accurate enough to describe the behavior of GaN heterostructure field effect transistors (HFETs) but these models cannot be used for simulating power GaN HFETs due to following reasons:

a) The channel properties of GaN HFETs are significantly different because of strain and related piezo- and inverse piezo-effects.

b) At high current density level, carrier scattering in HFET leads to electron real-space transfer.

c) The maximum electric field, current density and operating voltage is much higher for GaN HFETs compared to Si MOSFETs. These makes the transport properties of GaN HFET significantly different than that of Si MOSFETs.

d) GaN in general is a very defective material, due to the presence of large number of defects and charge trapping centers, current collapse is a serious concern in GaN HEMTs which negatively affects device pulse response.

On the contrary, available HFET models are mainly aimed to describe the behavior of HFETs in radio frequency applications. The models either do not include the necessary components or lacks in features crucially important for high voltage, high power applications. To demonstrate the important differences between these two model types, we can look at the following examples

1. For power switching applications, the regions below knee voltage is the most important whereas GaN RF models focusing on power amplifiers mostly targets the I-V characteristics in the saturation region.
2. Off state power loss is one of the most important factor in power switching applications, so GaN HFET models focusing on switching applications must

consider the current in the off state, whereas for RF power amplifier models, current in the sub-threshold region is not that important and usually not taken into consideration.

3. For power switches, all the traps with characteristic times ranging from microseconds to seconds are equally important; for RF power amplifiers, only traps that effects the DC and microwave properties needs to be accounted for.

Currently there is no power GaN HFET model in existence which meets the above criteria. So, there is a strong demand for the development of a novel modeling/simulation technique which can adequately describes the behavior of GaN HFET in power switching high-current, high-voltage circuits.

1.2 Development of Heterostructure

The heart of high electron mobility transistor is the two dimensional electron gas (2-DEG), revealed in the Bell Laboratory in late 1970's in undoped Gallium Arsenide (GaAs) and n-doped Aluminium Gallium Arsenide (AlGaAs) heterostructure. The measured electron mobility in the 2-DEG was much higher than that in bulk GaAs [3]. The principle behind this is shown in Fig. 1.1. Bandgap of AlGaAs is higher than that of GaAs. When these two materials are brought together, electron transfers from higher energy conduction band of AlGaAs to lower energy conduction band of GaAs. Due to this electron transfer, an electric field is created which causes band bending at AlGaAs/GaAs heterointerface. The transferred electrons are confined in a narrow quantum well on the low bandgap GaAs side which forms the 2-DEG (Fig. 1.1(b)). These electrons are spatially separated from the donor ions, so there is less ionized impurity

scattering resulting higher electron mobility in the 2-DEG channel [4]. The high electron mobility transistor (HEMT) was realized by connecting the 2-DEG channel to the source and drain and modulating the channel with the gate. It is also known as modulation doped field effect transistor (MODFET), selectively doped heterostructure transistor (SDHT), two dimensional electron gas field effect transistor (TEGFET) or heterostructure field effect transistor (HFET).

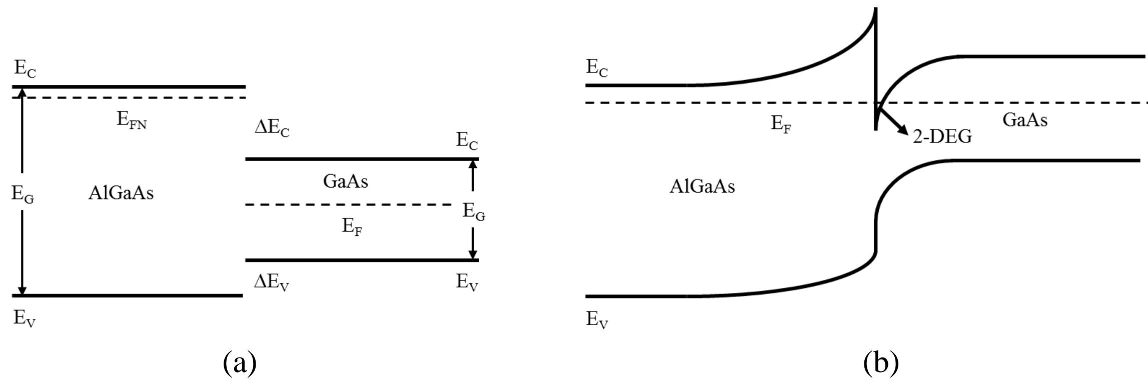

Figure 1.1 Band diagram of (a) n-type wide bandgap (AlGaAs) and narrow bandgap (GaAs) semiconductor (b) Band discontinuities and band bending at equilibrium for an ideal heterostructure

High Electron Mobility Transistor was first reported by Takashi Mimura in 1979 [5]. Initially, AlGaAs/GaAs material system was the main choice for HFET's as they showed better RF performance in terms of minimum noise figure and higher output power compared to GaAs MESFETs. But the performance improvement of AlGaAs/GaAs system was not as expected.

1.3 Drawbacks of Conventional Materials

- Si LDMOS has shown promises in the past in power amplifier segment due to excellent cost/performance ratio. But this trend was not continued because Si has

already reached performance limit due to material limitation imposed on operating frequency, breakdown voltage and power density [6].

- Silicon Germanium (SiGe) heterojunction bipolar transistors (HBTs) are used in many microwave and mixed signal products. But their application is limited to low power configuration. To make SiGe HBT's suitable power high voltage applications, the collector region of the transistor would have to be much wider. In that case, the base transit time would be lower but gains achieved due to this would be wasted because of the large collector delay. Due to this reason, SiGe HBTs are not a suitable candidate for high power applications [7].
- Gallium Arsenide (GaAs) substrates cost higher than Si substrates and difficult to handle. The heat dissipation in high power applications is not very efficient due to lower thermal conductivity. GaAs also suffers from low critical electric field [8].
- Silicon Carbide (SiC) has the advantage of higher thermal conductivity but the substrates are very expensive. The electron mobility is significantly lower than that of GaN. They are also limited in size and has a lot of defects [9].

1.4 Wide Bandgap Semiconductors

In recent years, wide bandgap materials have attracted much attention for high frequency, high temperature and high power applications. The most common wide bandgap materials include the group III-Nitrides Indium Nitride (InN), Gallium Nirtide (GaN) and Aluminium Nitride (AlN), and their alloys Aluminium Gallium Nitride (AlGaN), Indium Gallium Nitride (InGaN), Indium Aluminium Nitride (InAlN), SiC and Diamond.

The wide bandgap III-Nitride materials are very promising for high power applications due to high breakdown field [10] and high operating temperature [11]. With the development in wireless communications, the need for high-power, high-efficiency, linear, low-cost, monolithic solid-state amplifiers have increased drastically. Conventional semiconductors like Si, Ge, GaAs and SiC fails to simultaneously satisfy many of these requirements. Recently, newer materials like GaN has attracted much attention in the area of high temperature, high power applications. Researchers have reported AlGaN/GaN HEMTs with very high power densities and cutoff frequency and maximum frequency of oscillation more than 100GHz [12, 13].

Table 1.1 Material properties of GaN compared to other semiconductors

Characteristics	**Si**	**GaAs**	**β-SiC**	**4H-SiC**	**AlN**	**GaN**
Bandgap (eV)	1.1	1.43	2.2	3.26	6.2	3.45
Thermal conductivity ($Wcm^{-1}K^{-1}$)	1.5	0.46	4.9	4.9	3.0	1.3
Saturation electron velocity ($\times 10^7$ cm/s)	1.0	1.0	2.2	2.0	-	2.2
Electron mobility (cm^2/V-s)	1500	8500	1000	1140	-	1250
Breakdown field ($\times 10^5$ V/cm)	3.0	6.0	20	30	-	>10

Due to higher bandgap, high electron mobility and higher breakdown field, GaN is a preferred material among the III-Nitrides. GaN based HEMT has already shown great promises for power switching applications. That’s why, our model is focused on AlGaN/GaN HEMT but which proper choice of input parameters, our model can be used for any other III-Nitride materials.

CHAPTER 2

ALGAN/GAN HEMT OPERATING PRINCIPLE

2.1 Device Structure

The basic structure of AlGaN/GaN HEMT is shown in Fig. 2.1. The heart of high electron mobility transistor is the two dimensional electron gas (2-DEG) formed at the heterojunction formed by a wide bandgap undoped/n-doped AlGaN layer on top of an unintentionally doped narrow bandgap GaN layer. The gate is usually made of metal or poly-silicon which forms a Schottky barrier with the underlying AlGaN layer. The source and drain are low resistance ohmic contacts. Novel combinations are used in various HFET devices but the basic layers are as follows:

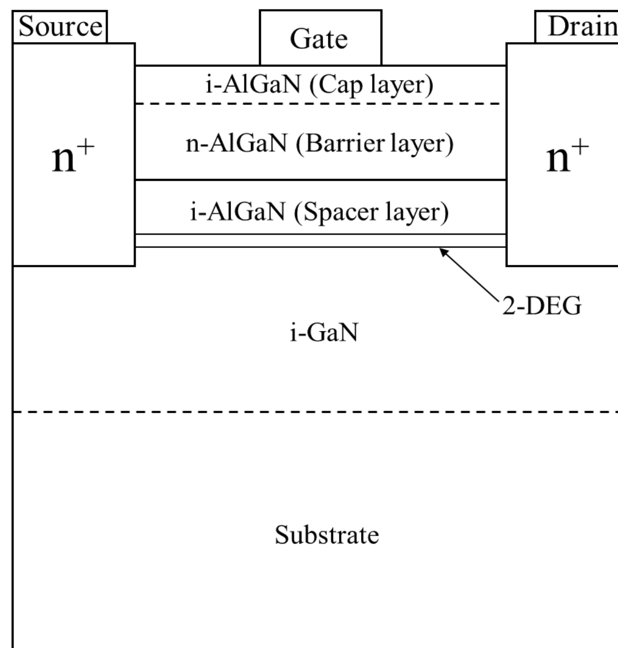

Figure 2.1 The schematic diagram of basic HFET structure

Substrate: HFET structure is grown on a semi-insulating substrate. Most commonly used substrates are Si, Sapphire, SiC and GaN. Si substrates are inexpensive, available in large sizes but there is a large lattice mismatch between GaN and Si. Sapphire has the advantage of low cost and availability in large sizes but it has poor thermal conductivity and high lattice mismatch with GaN. SiC has good lattice match and very good thermal conductivity but SiC substrates are very expensive. GaN substrate has good lattice matching with the buffer layer but they are very expensive and it's very hard to make GaN crystals in large sizes.

Buffer layer: Buffer layer is grown on the substrate and acts as the active layer for 2-DEG. The buffer layer is usually 1-5μm thick and either undoped or unintentionally doped. The material quality of the buffer layer should be high meaning there shouldn't be many traps and defects.

Spacer layer: A thin (20-50Å) undoped AlGaN layer called the spacer layer is grown on top of the GaN buffer layer. This purpose of this layer is to reduce ionized impurity scattering thereby increasing mobility. Spacer layer separates the ionized donors from the channel carriers, higher the thickness, smaller the impurity scattering. However, the transfer of electrons from the donor layer to the channel decreases with increasing spacer layer thickness leading to reduced mobility. Therefore, to achieve the optimal mobility of 2-DEG, the spacer layer should be very thin.

Barrier layer: The next layer grown on top of the spacer layer is the barrier layer. The barrier layer is highly doped and serves as the reservoir of electrons for the channel. This layer forms a Schottky barrier with the gate. Electrons in the barrier layer moves freely through the crystal and finally falls into the low energy quantum well formed at the

heterointerface of the barrier and buffer layer. These electrons form the two dimensional electron gas (2-DEG). The usual thickness of barrier layer is 150-300Å.

Cap layer: Cap layer is an optional undoped AlGaN layer which can be added on top of the barrier layer. The purpose of using this layer is to reduce gate leakage current by enhancing the Schottky barrier between the gate and barrier layer.

In GaN HEMTs, the source of 2-DEG is different than HEMT devices on other materials. Electrons in the 2-DEG of AlGaN/GaN HEMT is not supplied by the highly doped barrier layer, rather comes from the donor-like surface states in the AlGaN layer. The donor-like surface states in GaN HEMTs are facilitated by spontaneous and piezoelectric polarization. Spontaneous polarization is due to the polar nature of the AlGaN/GaN system and piezoelectric polarization arises from difference in lattice constant between GaN and AlGaN. This is the reason why the 2-DEG density in AlGaN/GaN HEMT is a strong function of the thickness of the AlGaN barrier layer.

2.2 Device Operation

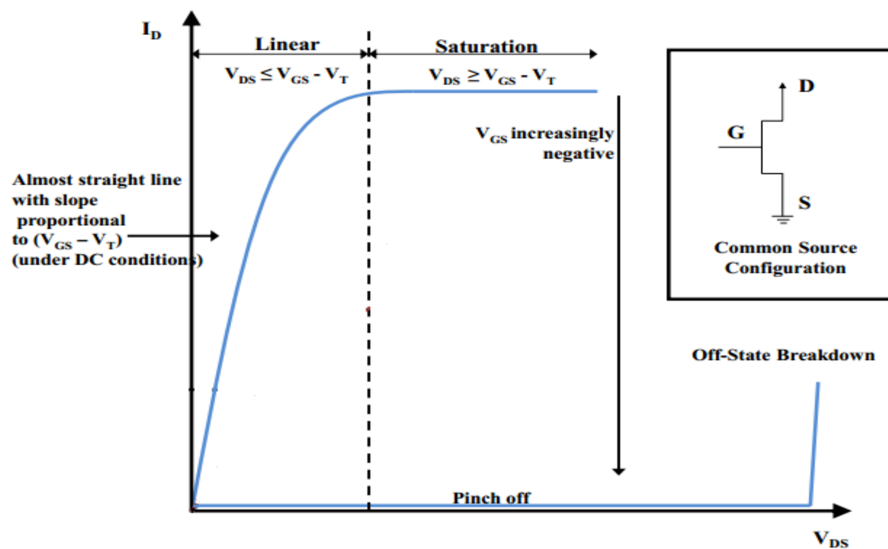

Figure 2.2 Description of I-V characteristics of HEMT

HEMT is primarily used to switch electronic signals or to amplify them. Fig. 2.2 shows the output current vs drain voltage characteristics of a depletion mode HFET. The most common way to bias a HEMT is the common source configuration as shown in the inset of Fig. 3. Source electrode is the common terminal; gate and drain electrode are the input and the output respectively. Gate acts as the control electrode of the device and has the ability to switch the device on and off. In a depletion mode device, the device can be switched off by applying a negative voltage to deplete the channel of electrons, the negative voltage at the gate results in a highly resistive channel and there is no current flow, this condition is known as 'cut-off'. V_{GS} is the gate bias voltage and V_T is some negative gate voltage at which the device begins to conduct current, known as the threshold voltage.

When $V_{GS} \leq V_T$, the channel is closed, i.e. completely depleted of electrons and drain current drops to zero. At $V_{GS} = 0V$ the channel is densely populated with electrons and the application of a drain voltage induces current flow between the source and drain. For low drain voltages ($V_{DS} < V_{GS} - V_T$), the electron velocity in the channel is proportional to the applied electric field, so current increases with this field and the device is said to be operating in the linear regime. For high drain bias ($V_{DS} > V_{GS} - V_T$), the lateral bias under the gate begins to pinch the channel off at the drain end of the gate. This continues until a point where the flow of electrons in the channel is constricted and the maximum amount of electrons that can flow to the drain contact is reached. At this point, the device operates in the saturation regime and any further increase in the drain bias does not result in an increase of current.

CHAPTER 3

OVERVIEW OF THE DEVELOPED COMPACT MODEL

3.1 Model Overview

Our model can reproduce both above-threshold and subthreshold characteristics of both n and p-channel deep submicron HFET's over a wide temperature range. The current–voltage (I-V) characteristics are described by a single, continuous, analytical expression for all regimes of operation, thereby improving convergence. The semi-empirical model includes effects such as velocity saturation in the channel, saturation of sheet carrier density, drain-induced barrier lowering (DIBL), stationary and non-stationary self-heating, transient and stationary current collapse, field plate effects and temperature dependence. The model also includes compact model for bulk current which is crucially important for power switching applications based on the results of extensive TCAD simulation study using Synopsys Sentaurus. The model is implemented using Verilog-AMS Hardware Description Language and Synopsys HSPICE and is suitable for simulation of mixed mode (digital/analog) circuits. The model has been verified against experimental data for various HFET devices.

3.2 Hardware Description Languages

The model is written using Verilog-AMS Hardware description language (HDLs). Traditional programming languages such as C/C++, Java generally describe algorithms

whereas HDLs describe hardware's. When describing a hardware, it is necessary to describe both the behavior of the individual components as well as how they are connected to each other.

There are two primary application of hardware description languages, one is simulation and the other one is synthesis [14]. With simulation, various stimuli are applied to an executable model which is described using the HDL in order to predict the behavior of the hardware. Simulation helps to understand the behavior of a complex system without actually investing time and money to implement it. On the other hand, the actual process of implementing the hardware is called Synthesis. A hardware that is not yet physically implemented, can be described at an abstract level using HDL. In contrast, synthesis is the act by which a new refined description of a hardware that has a physical implementation can be created using equivalent behavior at the inputs and outputs of the hardware. HDL should be expressive, the basis of using HDL in simulation is its ability to describe variety of behaviors easily.

3.3 Why Verilog?

Verilog-AMS language has a wide range of capabilities. It can be used to model mixed-signal systems. By using Verilog-AMS, both analog and digital systems can be described to the simulator simultaneously. Verilog-AMS can support a wide variety of situations represented by mixed-signal systems. Standard circuit simulators like SPICE only provides a few built-in models. These models are needed to model the behavior of commonly used components in integrated circuits. The ability to add new models is also limited. The execution time is longer and only components that can be described by a

small number of simple formulas can be added to these models. For complicated model development, this way of adding models is not very convenient. Verilog-AMS can efficiently describe a broad range of models, has a wide variety of features and therefore suitable for heavily used, complicated models.

Compact model is the model of semiconductor component commonly incorporated into SPICE. Models written in Verilog are portable, users can correct any flaws or modify any module or add modules to enhance the model if the model is available in source form. Verilog models are also much shorter than models written in C, usually model that serves the same purpose is 10 times longer in C than that in Verilog. Because of smaller size, Verilog models can be maintained easily.

3.4 Verilog-A in HSPICE Simulator

Synopsys HSPICE is an optimizing analog circuit simulator. It can simulate electrical circuits in steady-state, transient, and frequency domains. HSPICE is known for fast, accurate circuit and behavioral simulation compared to other circuit simulators. It uses Monte Carlo, worst-case, parametric sweep and data-table sweep for assessing circuit level performance and yield. HSPICE has the most reliable automatic convergence capability. HSPICE is the industry's "gold standard" for accurate circuit simulation and offers MOS device models certified by foundries. It incorporates state-of-the-art simulation and analysis algorithms. HSPICE is industries most trusted and comprehensive circuit simulator for the last 25 years.

CHAPTER 4

MODEL FORMULATION

4.1 Drain Current Model

When gate to source voltage is not too large, the MOSFET expressions for channel sheet carrier density n_s, linear channel conductance g_{chi}, saturation current I_{sat} and gate channel capacitance C_{ch} can also be used for HFETs [15]. For large gate bias, the transfer of electron from channel to the barrier layer must have to be considered. This spillover effect has been reported in QW FET and buried channel MOSFET structures.

The sheet carrier density in the 2-DEG cannot go beyond a maximum value. The limitation is imposed by the energy band discontinuities at the heterointerface and has a strong effect on the characteristics of HFET [15]. This can be clearly understood by looking into the energy band diagram of HFET structure shown in Fig. 4.1 (a).

As V_{GS} increases, the electron quasi-fermi level E_{Fn} in the larger bandgap AlGaN moves to the bottom of the conduction band and significant number of electrons transfer into the AlGaN layer. The transconductance of the device reduces due to this [16]. Normally, the device current doesn't depend much on the wide bandgap material because of the presence of lots of defects and traps. Fig. 4.1 (b) shows the density of sheet carriers in the channel n_s and in the AlGaN layer n_t at different gate bias. These results are based on a self-consistent solution of Poisson's and Schrodinger's equation [17]. As seen

beyond a certain gate voltage, the electron density in the AlGaN layer increase rapidly. The sheet carrier density saturates at higher gate bias.

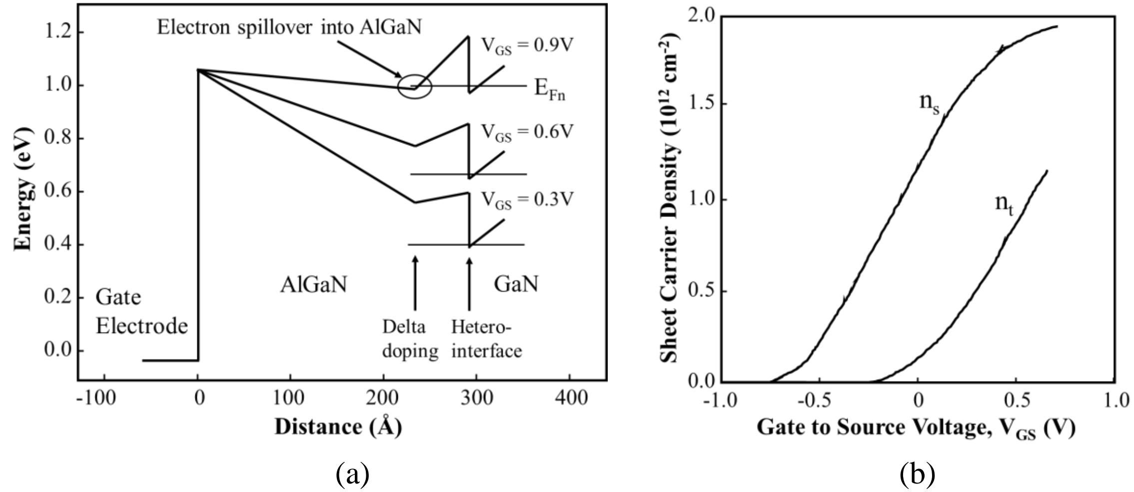

Figure 4.1 (a) Illustration of electron transfer at the heterointerface in a delta doped HFET at high V_{GS} (b) Electron sheet carrier densities in the conducting channel at different V_{GS}, indicating the electron spillover into the high band gap layer above a certain gate bias

To establish a single continuous expression for the I-V characteristics which is valid in all regions, first the drain current in each region is expressed and then a smoothing function is used to make transitions between them. In the linear region or below saturation, the drain current is proportional to drain to source voltage and can be written as

$$I_{ds} = g_{chi} V_{ds} \dots \dots \dots \dots \dots \dots (1)$$

where g_{chi} is the intrinsic channel conductance and V_{ds} is the drain to source voltage. The linear intrinsic channel conductance is given by

$$g_{chi} = \frac{q n_s W \mu_n}{L} \dots \dots \dots \dots \dots \dots (2)$$

where n_s is the sheet carrier density, μ_n is the low field mobility, W is the total device width and L is the gate length.

Intrinsic channel conductance g_{chi} is directly proportional to the sheet carrier density and is given by universal charge control model (UCCM) [18]. But, it's not possible to solve UCCM analytically w.r.t n_s. However, assuming the forward voltage is zero, we can use the generalized version of the approximate analytical solution of UCCM for the MIS capacitor

$$n_s = 2n_0 \ln\left[1 + \frac{1}{2} exp\left(\frac{V_{gt}}{\eta V_{th}}\right)\right] \dots\dots\dots\dots\dots\dots (3)$$

where V_{gt} is gate voltage overdrive and V_{th} is the thermal voltage. At threshold, the sheet carrier density is given by

$$n_0 = \frac{\eta V_{th} c_i}{2q} \dots\dots\dots\dots\dots\dots (4)$$

The two-piece velocity saturation model provides the MOSFET drain saturation current for above threshold region by substituting V_{gt} by effective gate voltage overdrive V_{gte}. Below threshold, V_{gte} is equal to $2V_{th}$ and well above threshold, it coincides with V_{gt}. If drain, source parasitic resistances are ignored, the drain saturation current can be written as

$$I_{dsat} = \frac{g_{chi} V_{gte}}{1 + \sqrt{1 + \left(\frac{V_{gte}}{V_L}\right)^2}} \dots\dots\dots\dots\dots\dots (5)$$

where $V_L = F_s L = \frac{vs}{mu} \times L$. F_s is the saturation field and vs is the saturation velocity. The effective gate voltage overdrive suitable for MOSFET can be expressed as [15],

$$V_{gte} = V_{th}\left[1 + \frac{V_{gt}}{2V_{th}} + \sqrt{\delta^2 + \left(\frac{V_{gt}}{2V_{th}} - 1\right)^2}\right] \dots\dots\dots\dots\dots\dots (6)$$

where δ is the width of the transition from linear to saturation region.

4.1.1 Smoothing Function

A model that contains two distinct equations for two different operating regions, can cause kinks and discontinuities in the device characteristics. This leads to numerical difficulty during a circuit simulation. A fundamental problem that severely affect such model is that, although both I_d and dI_d/dV_{ds} are continuous at V_{dsat}, d^2I_d/d^2V_{ds} is not. In order to ensure the numerical robustness, the derivatives of arbitrary order must be continuous at all voltage values of interest. This property is known as ∞-differentiability. One solution to guarantee ∞ differentiability is to use a single equation to describe the drain current, rather than with two separate equations. The universal smoothing function that is commonly used to make the transition from linear to saturation regimes is [15],

$$I_d = \frac{g_{ch}V_{ds}(1+\lambda V_{ds})}{\left[1+\left(\frac{g_{ch}V_{ds}}{I_{sat}}\right)^m\right]^{1/m}} \ldots\ldots\ldots\ldots\ldots\ldots (7)$$

Here, the parameter m determines the shape of the characteristics in the knee region. λ is an empirical constant which accounts for the finite output conductance in saturation.

Another special mathematical smoothing function that was introduced in the third generation BSIM model to ensure smooth and continuous transition between the linear and saturation region is [19],

$$V_{dsx} = V_{dsat} - 0.5 \times \left[V_{dsat} - V_{ds} - \Delta + \sqrt{(V_{dsat} - V_{ds} - \Delta)^2 + 4\Delta V_{dsat}}\right] \ldots\ldots\ldots\ldots\ldots (8)$$

where V_{dsx} is an auxiliary drain bias, Δ is an empirical smoothing parameter and V_{dsat} is the saturation drain voltage.

4.1.2 New Smoothing Formula

Based on equation (8), we have developed a new smoothing function which is simpler and provides continuous higher order derivatives

$$y = y_{sat} - 0.5 \times \left[dy + \sqrt{dy^2 + 4\Delta y_{sat}^2} \right] \ldots\ldots\ldots\ldots\ldots\ldots (9)$$

where $dy = y_{sat}(1 - \Delta) - y_{in}$ when $y_{in} = y_{sat}, y \approx y_{sat}(1 - \sqrt{\Delta})$

By changing the fitting parameter Δ, we can easily control the shape of transition from linear to saturation region. Use of this new smoothing function increases simulation speed significantly which is highly desirable for faster operation.

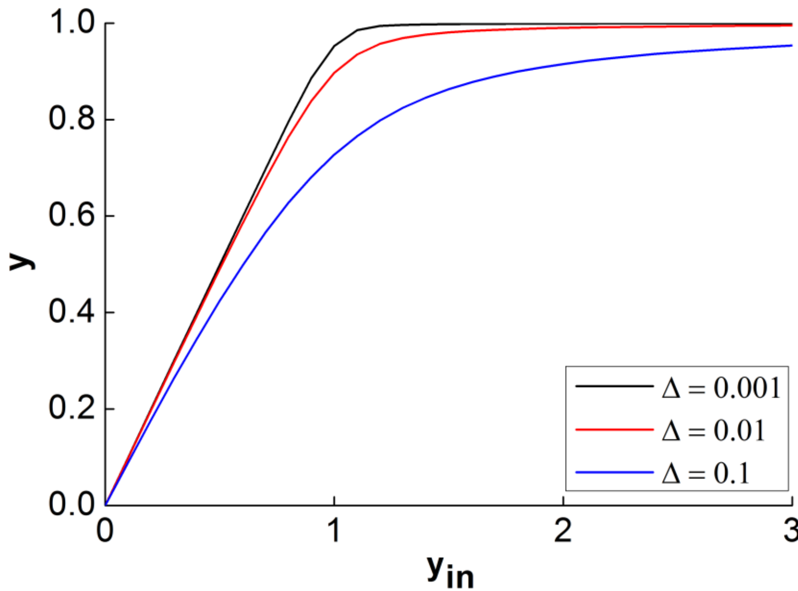

Figure 4.2 Demonstration of our new smoothing function for different values of Δ

The drain current equation used in our model using the new smoothing formula is below

$$I_{ds} = I_{dsat} - 0.5 \times \left(dI_{ds} + \sqrt{dI_{ds} \cdot dI_{ds} + 4\Delta I_{ds} \cdot I_{dsat} \cdot I_{dsat}} \right) \ldots\ldots\ldots\ldots\ldots\ldots (10)$$

$$where\ dI_{ds} = I_{dsat} \times (1 - \Delta I_{ds}) - I_{dlin}$$

$$and\ I_{dlin} = g_{chi} \times V_{ds}$$

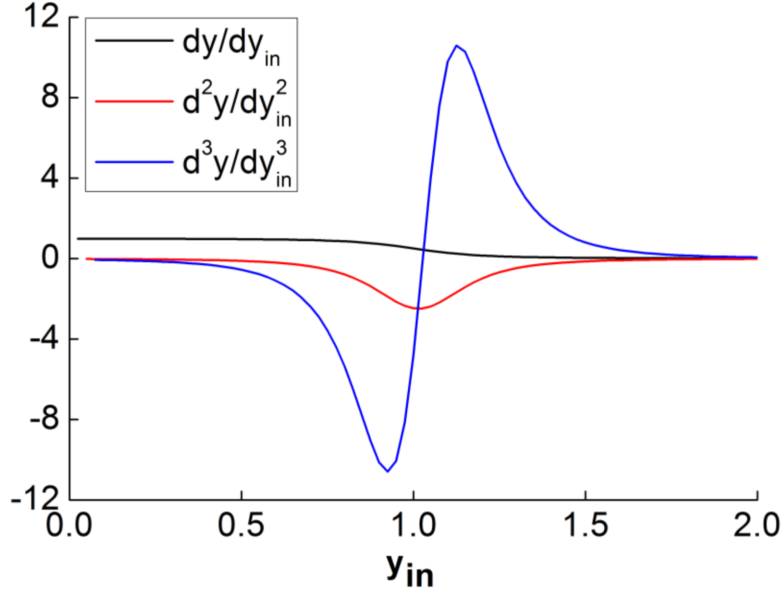

Figure 4.3 Differentiability of the new smoothing function

4.1.3 Saturation of Sheet Carrier Density

As discussed earlier, for HFETs, we have to consider electron spillover at large gate bias. Typically, it is done by assigning a maximum value n_{smax} for channel concentration and assuming that channel concentration cannot exceed this maximum value. In our model, the maximum sheet carrier density is included as a tunable input parameter which depends on the material system and doping profile of the wide bandgap semiconductor. An expression that provides reasonable description of the saturation of n_s at high gate bias based on the modeling approach in [20, 21] is,

$$n_s = \frac{n_s'}{\left[1 + \left(\frac{n_s'}{n_{smax}}\right)\right]^{1/\gamma}} \dots\dots\dots\dots\dots\dots (11)$$

Here n_s' is the sheet carrier density from the universal MOSFET model [15] and γ is a characteristic parameter for the transition from linear to saturation region.

In our model, we have incorporated the saturation of carrier density using our newly developed smoothing function. The transition at higher gate bias shows both the saturation effect and slight decrease of channel carrier density due to spillover effect.

$$n_s = n_{smax} - 0.5 \times \left(dn_{smax} + \sqrt{dn_{smax} \cdot dn_{smax} + 4\Delta n_s \cdot dn_{smax} \cdot dn_{smax}}\right) \ldots\ldots\ldots (12)$$

$$where\ dn_{smax} = n_{smax} \times (1 - \Delta n_s) - n_{stot}$$

and n_{stot} is the same as n_s in equation (3) and n_{smax} is the maximum sheet carrier density or value of n_s at saturation. Fig. 4.4 shows the transition of n_s from linear to saturation region.

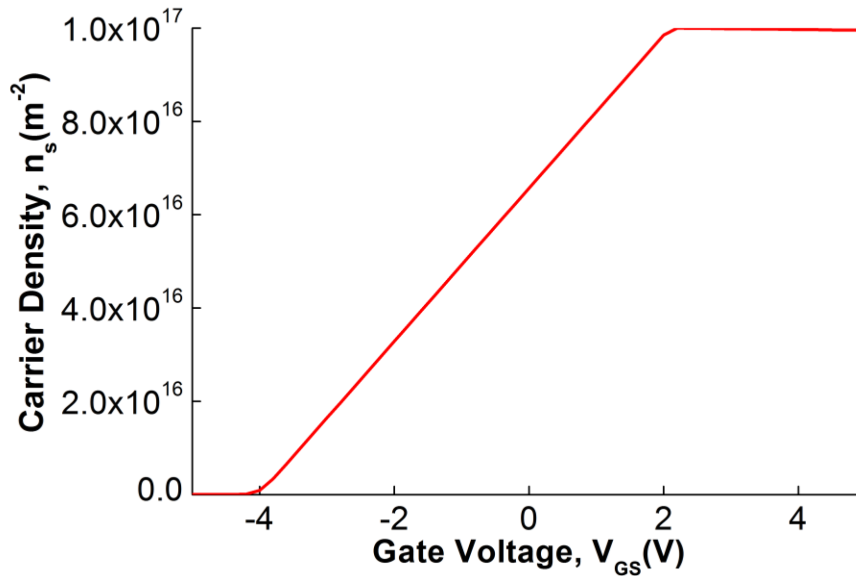

Figure 4.4 Transition of sheet carrier density from linear to saturation region at high gate bias

4.2 Non Linear Effects

4.2.1 Drain Induced Barrier Lowering (DIBL)

For a small channel length device, drain induced barrier lowering is a very common short channel effect that must have to considered. Short-channel effects start to occur if the

source and drain depletion region becomes a significant portion of the channel length. The effect can be more serious in extreme cases when the sum of these depletion widths approaches the channel length. At this condition, commonly known as punch-through, the gate completely loses control over the channel and a large leakage current flows between the source and drain. This leakage current is a strong function of the drain bias [22].

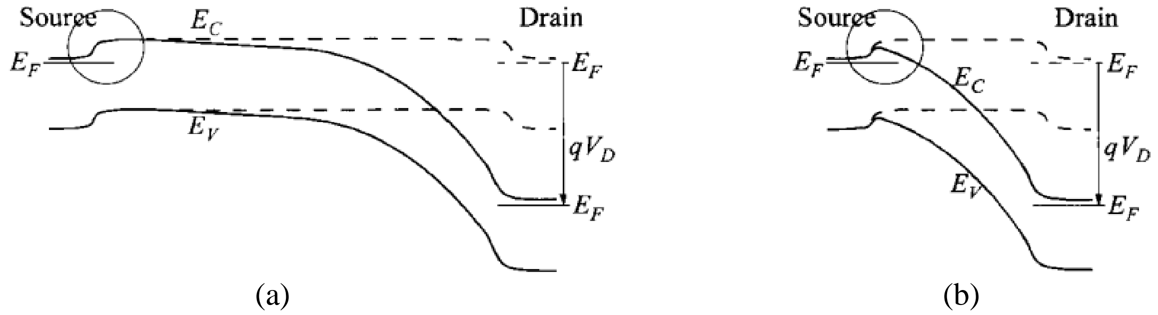

Figure 4.5 Energy-band diagram for (a) long-channel and (b) short-channel HFETs at the semiconductor surface showing the DIBL effect in the short-channel device. Dashed lines $V_{DS} = 0$, solid lines $V_{DS} > 0$

When high drain voltage is applied to a short-channel device, the barrier for electrons at the source side decreases which results in a decrease of the threshold voltage. This effect this is known as DIBL. Due to barrier lowering, the channel carrier concentration at the source side changes with applied bias. This effect is incorporated in the model by introducing σ which is the channel-length dependent DIBL parameter.

$$\sigma = \frac{\sigma_0}{1 + \exp\left[\frac{V_{gt0} - V_{\sigma t}}{V_\sigma}\right]} \dots\dots\dots\dots\dots\dots (13)$$

where V_{gt0} is the voltage overdrive at zero drain-source bias, the width of DIBL is determined by and $V_{\sigma t}$, V_σ respectively. $\sigma \to \sigma_0$ for $V_{gt0} < V_{\sigma t}$ and $\sigma \to 0$ for $V_{gt0} > V_{\sigma t}$.

$$V_{gt} = V_{gt0} + \sigma V_{ds} \qquad\qquad V_{gt0} = V_{gs} - V_T$$

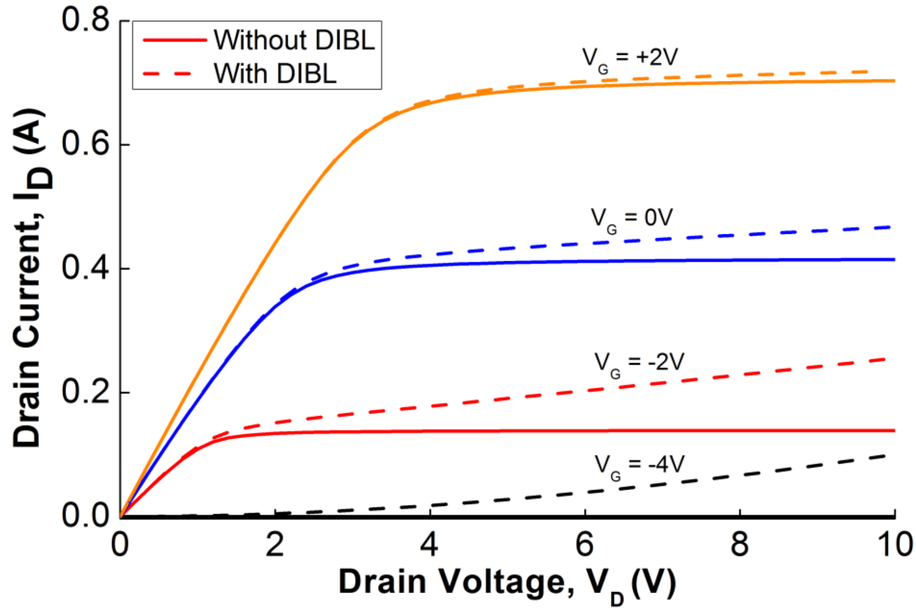

Figure 4.6 Simulated I-V curve showing drain current with and without DIBL effect

4.2.2 Temperature Dependence

Electronic devices and circuits are needed to operate in different environments, including a wide range of temperatures. Heat generation from power dissipation in an integrated circuit can be considerable and associated temperature rise must be accounted for in both device and circuit design. Devices fabricated on Si substrate has higher thermal conductivity and a well-designed chip placed on a good heat sink can achieve a relatively uniform and tolerable operating temperature. However, for devices with dimensions in the sub-micrometer range, such design becomes very difficult.

Mobility

In the presence of scattering, the average velocity of the carriers in a semiconductor is proportional to the electric field. The electron transport due to an applied electric field E, known as drift velocity is given by

$$v = \mu \times E \dots\dots\dots\dots\dots\dots (14)$$

where v is the electron drift velocity and μ is the electron mobility. The mobility is determined by a variety of scattering mechanisms. These mechanisms include lattice vibrations, ionized impurity atoms, other carriers, surfaces and other material imperfections. All these effects are functions of the local electric field, doping concentration, lattice temperature and so on. When electric field is low, carriers are almost in equilibrium with the lattice and mobility has a characteristic low-field value. The low-field mobility is dependent on phonon (lattice temperature) and impurity scattering (impurity concentration). Low-field mobility decreases as lattice temperature and impurity scattering increases.

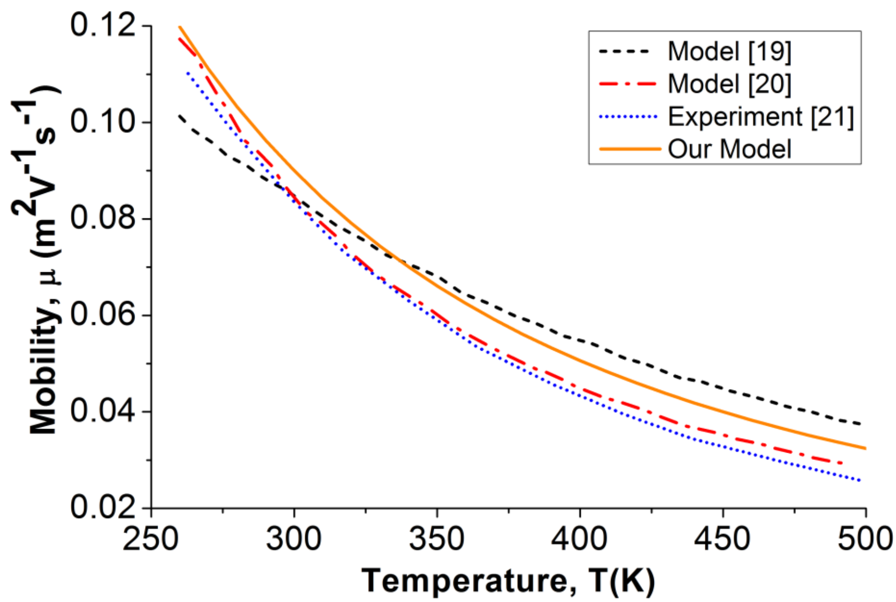

Figure 4.7 Temperature dependent mobility in our model compared to other model [23, 24] and experiment data [25]

Various mobility models have been developed to predict the behavior of low field mobility with temperature. In our model, the 2-DEG mobility at different temperatures

have been calculated using Eq. (15) which was developed based on the empirical model presented in [26].

$$\mu_T = \mu_{300K}\left(\frac{T}{300}\right)^{-\beta} \dots\dots\dots\dots\dots\dots (15)$$

where β varies between 1.5 and 2.0 for temperatures ranging from 200K to 500 K.

At high electric field, carrier mobility decreases with electric field because the carriers that gain energy takes part in various scattering processes. The mean drift velocity does not increase linearly with electric field but rises more slowly. At some point, velocity stops increasing with electric field but drops and finally saturates at a constant velocity.

Threshold Voltage

Threshold voltage is one of the key parameters that controls the switching behavior of any semiconductor device. HEMT I-V characteristics are proportional to the square of the difference of gate voltage and threshold voltage. Thus, a small change in threshold voltage causes a large change in the output current. Therefore, it is very important to calculate the threshold voltage accurately with temperature changes. There are many material parameters that are related to the calculation of threshold voltage, and a number of empirical relationships have been obtained from experimental data [27]. In our model, threshold voltage variation with temperature has been accounted by using below formula.

$$V_T = V_{T0} + K_T \times (T - 300) \dots\dots\dots\dots\dots\dots (16)$$

where K_T is the temperature coefficient of threshold voltage. Fig. 4.8 shows the variation of threshold voltage with respect to temperature, as seen our model can closely predict the change in threshold voltage with temperature.

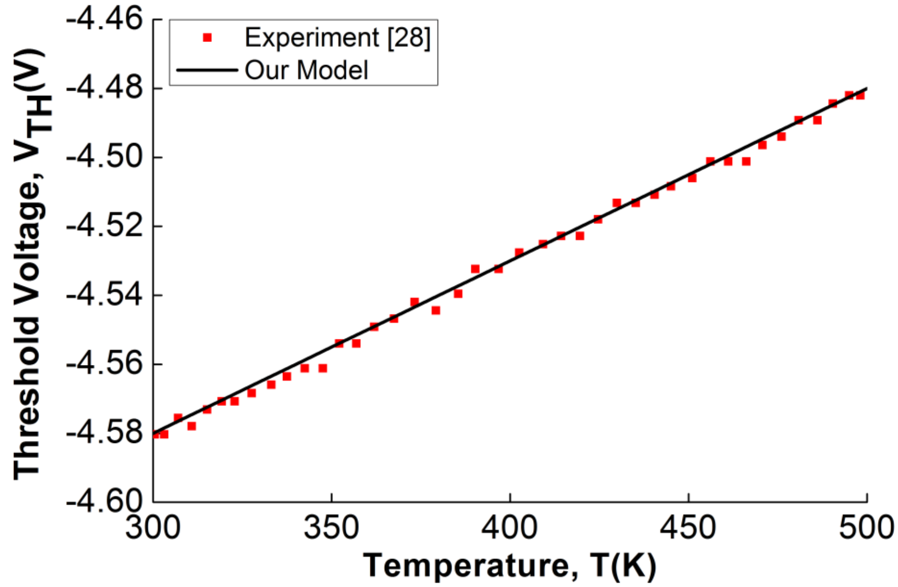

Figure 4.8 Variation of threshold voltage versus temperature, our model compared to experimental data [28]

Saturation Velocity

Precise modeling of the saturation velocity is a key element for device simulation, especially for High Electron Mobility Transistors (HEMTs) where the saturation velocity is directly related to the available gain of the device. Various models have been suggested for modeling the temperature dependence of the saturation velocity, see e.g. Mohammad [29], Allam and Pribetich [30]. Most of them seem to be unnecessarily complex in their mathematical form, or are not physically sound. In our model, we have included temperature dependence of saturation velocity using below simple formula

$$v_{sat}(T) = v_{sat}(300K) - K_{vs} \times (T - 300) \ldots \ldots \ldots \ldots \ldots (17)$$

Fig. 4.9 shows variation of saturation velocity with temperature which is in good agreement with the reference curve obtained from Monte Carlo simulation using Genetic Algorithm [31].

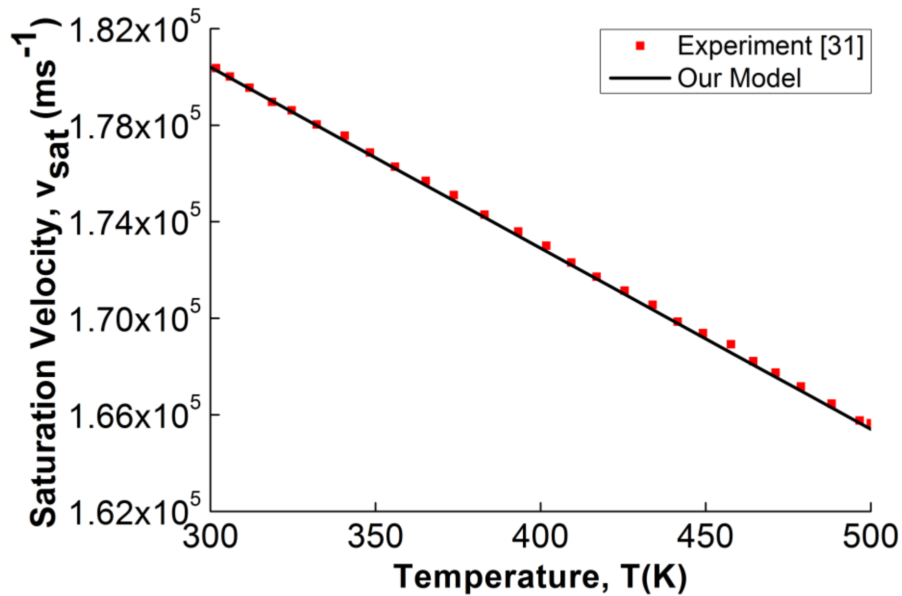

Figure 4.9 Variation of saturation velocity with temperature which is in good agreement with the reference data obtained from Monte Carlo simulation using Genetic Algorithm [31]

4.2.3 Self-Heating

GaN based HEMT has become a promising candidate for high frequency, high power applications because of high breakdown field in the wide band-gap semiconductor. However, the high power dissipation of GaN HEMTs operating at large biases may result in high junction temperature and enhance the phonon scattering causing a drop of carrier mobility. This effect has been reported to be of great influence on the static current characteristics, and is commonly referred to as “Self-Heating”. The evidence of such an effect is a negative slope of drain current I_{ds} versus drain voltage V_{ds}. The self-heating effect may degrade the gate electrode due to the accelerated electro migration and can easily burn metal wires connecting the chip to the package, thus causing device failures and reliability problems. Severe self-heating may even damage the device itself.

Stationary Self-Heating

Self-heating effects are a serious concern in GaN HEMTs because of their large power densities and hence, accurate modeling and simulation of these thermal effects is crucial to the understanding of the operation of these devices. The power densities in GaN HEMTs can be 10 times higher than those that can be obtained in silicon and GaAs devices. The temperature increase induced by self-Heating effect in the transistor can be described by the following expression [32],

$$T = T_a + R_{th} I_d V_{ds} \dots\dots\dots\dots\dots\dots (18)$$

where T is the new operating temperature, T_a is the ambient (room) temperature, I_d is the drain current, V_{ds} is the drain-source voltage, and R_{th} is the thermal resistance.

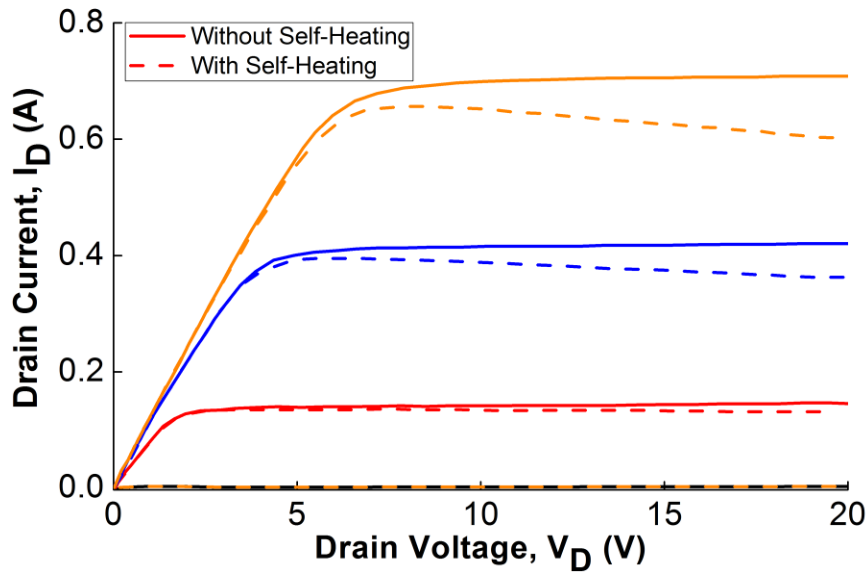

Figure 4.10 Simulated drain current with and without self-heating effect

Non-stationary Self-Heating

Thermal resistance measures how efficiently power can be dissipated from a device. It can be used to determine the junction temperature if the power dissipation is constant.

Usually, the average junction temperature is obtained by multiplying a constant with the average power dissipation. Every device has a maximum operating temperature above which the device cannot operate properly. However, using only thermal resistance, it's not possible to identify how long a large power pulse can be applied to a device before it reaches the maximum operating temperature [33]. Clearly, thermal resistance of a device is not sufficient enough to indicate the temperature variation of transistor due to changes in applied power with time.

To address this problem, Strickland [33] proposed a thermal equivalent circuit for the transistor. The approach is an extension of the thermal resistance concept and also consistent with boundary value problem. This is accomplished by drawing an analogy between certain electrical and thermal quantities. Table 4.1 shows the analogous quantities.

Table 4.1 List of analogous quantities between thermal and electrical systems

Electrical	**Thermal**
V voltage (Volts)	T temperature (^{0}C)
I current (Amps)	P power dissipation (W)
R electrical resistance (Ohms)	R_{TH} thermal resistance (^{0}C/W)
C electrical capacitance (Farads)	C_{TH} thermal capacitance (W-s/^{0}C)

Fig. 4.11 shows the thermal equivalent circuit of a transistor where the current source represents the power dissipation from the device and R_{TH} and C_{TH} are the thermal resistance and thermal capacitances respectively. dT represents the increase in local temperature due to change in input power.

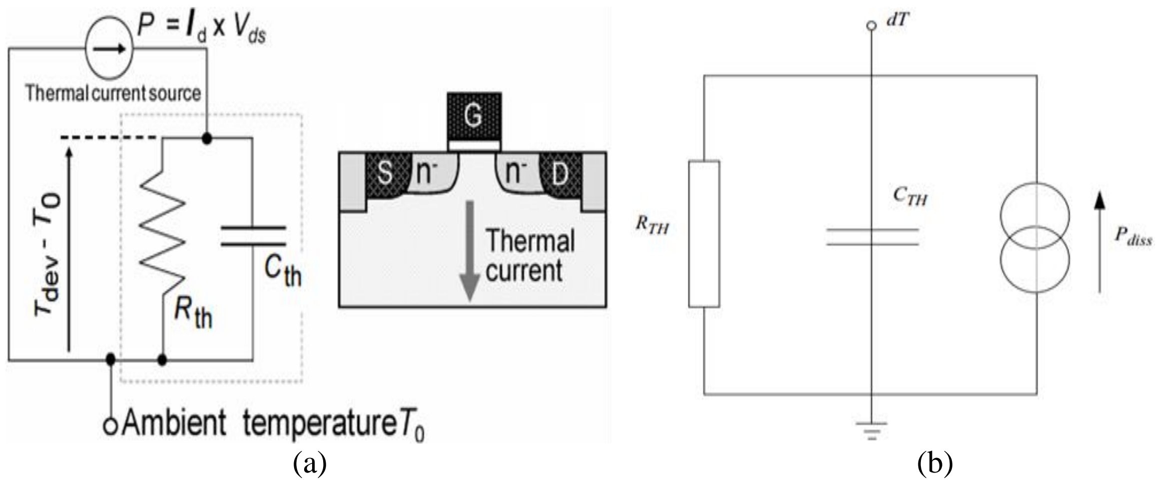

Figure 4.11 (a) One-cell thermal circuit consists of one R_{TH} and one C_{TH} (b) The self-heating network, the voltage V_{dT} at the temperature node gives the increase in local temperature

Non-stationary self-heating is modeled using this concept in MOS 11 model [34]. In our HFET model, we have also applied the same approach to simulate non-stationary or transient self-heating.

For self-heating simulation, an input parameter named sh is incorporated in the model. The mode of self-heating depends on the value of this parameter. If sh = -1, the model is simulated without self-heating effect. If sh value is 0, instantaneous self-heating is activated and the temperature at which the model is simulated is calculated by the formula given in Eq. (18). If sh = 1, the change in temperature is calculated from the one-cell thermal circuit. The I-V curves are simulated at a temperature obtained from the equation below

$$T = T_a + \Delta T_1 \dots\dots\dots\dots\dots\dots (19)$$

where ΔT_1 is the same as dT shown in the one-cell thermal circuit of Fig 4.11 (b).

The model also includes two-cell thermal equivalent circuit which can be activated by selecting sh = 2.

4.3 Gate Current Model

Gate leakage is of great concern in HFET devices because it degrades the I-V characteristics and the transconductance. The problem may be severe in enhancement-mode HFET's because here the intrinsic channel current can be effected by gate current [35].

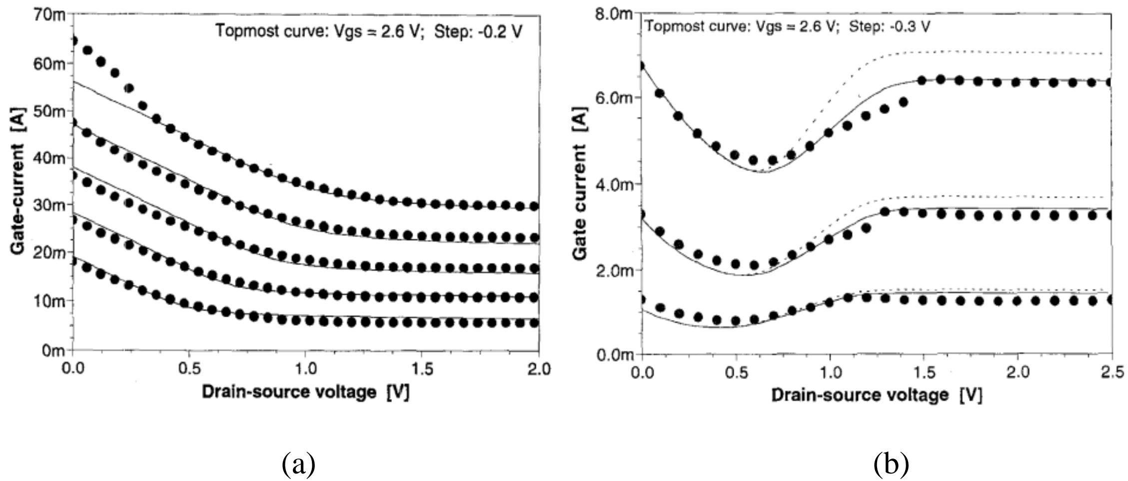

Figure 4.12 (a) Gate current versus drain-source voltage for an HFET device with gate length of 1.2-µm and gate width of 200-µm, (b) Gate current versus drain-source voltage for an 0.8-µm long and 10-µm wide HFET device

The gate current behavior or pattern varies widely among different HFET devices. In some devices, gate current decreases with increasing drain to source voltage as shown in Fig. 4.12(a), whereas in other devices gate current can decrease initially to a minimum value at low drain-source bias, then increases and finally saturates at higher drain-source bias (Fig. 4.12 (b)).

The total gate current I_g consists of two current components, gate to source current I_{gs} and gate to drain current I_{gd},

$$I_g = I_{gs} + I_{gd} \dots\dots\dots\dots\dots\dots (20)$$

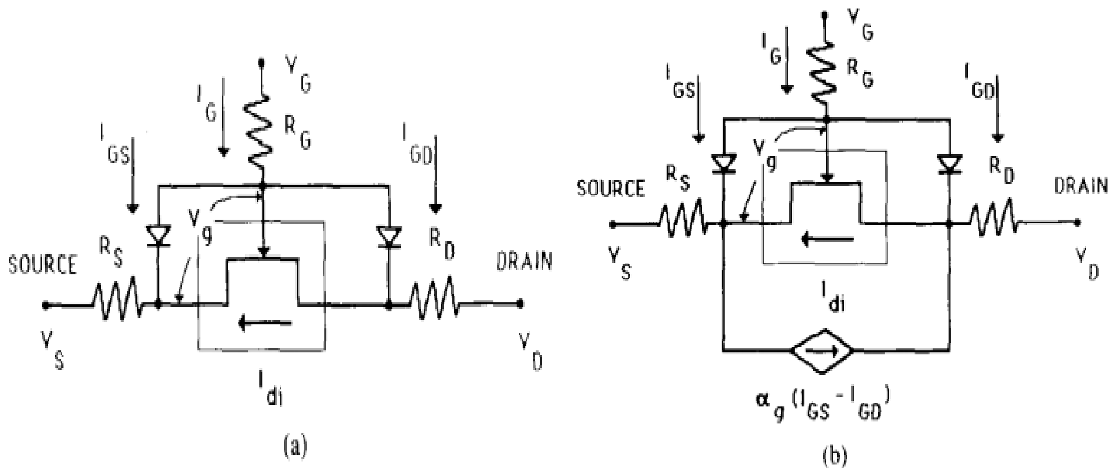

Figure 4.13 (a) Standard equivalent circuit model of Schottky gate FET using drain to gate and source to gate diodes. (b) New equivalent circuit model considering the distribution of gate current along the channel of Schottky gate FET

Typically, the circuit of field-effect transistor with Schottky gates are modelled by considering two diodes, one between the drain and the gate and the other between the source and the gate as shown is Fig. 4.13 (a). But experimental data indicates that the simple equivalent circuit model shown in Fig. 4.13 (a) cannot adequately describe the dependence of gate current on the gate and drain voltages [36, 37]. This is because the gate current is basically distributive in nature meaning it flows along the entire channel instead of just at the source and drain ends of the channel. The relationship between gate and drain current cannot be described by the gate to source diode in Fig. 4.13 (a) because the diode current is completely separated from the intrinsic drain current of the FET.

Under normal operating condition, a positive voltage is applied to the drain which makes the gate to drain diode less forward biased compared to the gate to source diode. As a result, an increase in the gate current causes almost an equal increase in the source current which means the channel current is completely unaffected by the gate current. However, in real HFET, the gate current is increased partially due to the redistribution of

potential and electron along the channel. This causes a reduction in the intrinsic channel current. This correlation between the gate and drain current is completely ignored by the circuit model shown in Fig. 4.13(a). Ruden, et al. [38], [39] proposed a modified model to account for this effect shown in Fig. 4.13(b). In this model, the charge-control model is used to calculate the intrinsic channel current of the FET.

Chen et al. [40] proposed another model which is consists of two Schottky diodes in series. One of the diode is between the metal and AlGaAs, another one is an equivalent Schottky diode at heterojunction between the higher bandgap AlGaAs barrier layer and lower bandgap GaAs buffer layer. The diodes along with the energy band diagram are shown in Fig. 4.14. Φ_1 and Φ_2 are represents the barrier height between the metal-AlGaAs and AlGaAs-GaAs interfaces, respectively. The main current transport mechanism through the GaAs Schottky barrier is thermionic emission of majority carriers over the barrier.

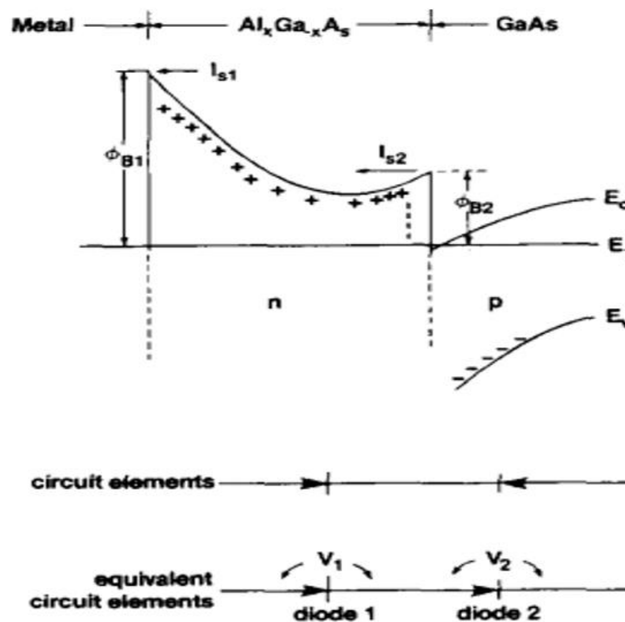

Figure 4.14 Schematical energy band diagram for AIGaAs/GaAs MODFET

A positive bias to the gate with respect to the 2-DEG makes diode 1 at metal-AlGaAs interface forward biased and diode 2 at AlGaAs-GaAs interface reverse biased. Then all the applied voltage will drop across diode 2 but since the barrier height of diode 2 is much lower than that of diode 1, the diode saturation current I_{s2} is several orders of magnitude higher than I_{s1} (Fig. 4.14). At low voltages, diode 1 is forward biased and most of the applied voltage will drop across diode 1. At larger gate bias, diode 2 will dominate. In power switching applications, most of the devices are depletion type, so Vg is small and we can ignore the second diode.

The parameter α in Fig 4.13 (b) is a temperature dependent parameter which describes the diversion of electrons from the channel into the gate. At higher drain bias, the effect is higher on the drain side, so I_{gd} is higher than I_{gs}. Lee et al. [35] modified the current source shown in Fig. 4.13 (b) from $\alpha(I_{gs} - I_{gd})$ to $\alpha_1 I_{gs} - \alpha_2 I_{gd}$ to account for the effect on I_{gd} by making α_2 bias dependent. By this modification, the model covers all observed cases.

At low gate bias, the gate-source and gate-drain current can be approximated by the well-known diode equations [21], [40]:

$$I_{gs} = A_s A^* T_s^2 \exp\left(-\frac{\Phi_B}{k_B T_s}\right)\left[\exp\left(\frac{qV_{GS}}{m_2 k_B T_s}\right) - 1\right] \ldots\ldots\ldots\ldots (21)$$

$$I_{gd} = A_d A^* \left[T_d^2 \exp\left(-\frac{\Phi_B}{k_B T_d}\right)\exp\left(\frac{qV_{GD}}{m_2 k_B T_d}\right) - T_s^2 \exp\left(-\frac{\Phi_B}{k_B T_s}\right)\right] \ldots\ldots\ldots (22)$$

where A* is the effective Richardson constant, Φ_B is the effective potential barrier for channel electrons at the heterojunction in equilibrium, q is the electronic charge, k_B is the Boltzmann constant, m_2 is the ideality factor of the heterojunction diode, A_s and A_d are effective gate areas for gate-source and gate-drain current path, V_{GS} and V_{GD} are potential

differences between the gate and the source; and the gate and the drain, respectively. T_s and T_d are the equivalent electron temperatures at the source and drain side of the channel, respectively. The second term in the parentheses of Eq. (22) represents the reverse saturation current which is due to the flow of cool electrons of the gate metal from the gate to the channel.

The reverse diode conductance g_{gr} is a temperature dependent parameter which is related to the temperature dependence of the Schottky barrier height and the generation/recombination current. Usually, these effects are modeled using activation energy. However, by considering the distribution of activation energies in the bandgap due to the DX centers, Ytterdal et al. [41] added the following equation that describes the temperature dependence very well over a wide range of temperature

$$g_{gr} = g_{gr0} \exp\big(\xi(T - T_0)\big) \ldots\ldots\ldots\ldots\ldots\ldots (23)$$

where ξ is a parameter that determines the sensitivity of the reverse diode conductance to the temperature, T_0 is the ambient temperature and g_{gr0} is the value of g_{gr} at T_0. After adding the reverse diode conductance term, we get the following form of the complete gate-source and gate-drain current,

$$I_{gs} = \frac{LW}{2}\left\{A^* T_s^2 \exp\left(-\frac{q\Phi_B}{k_B T_s}\right)\left[\exp\left(\frac{qV_{GS}}{nk_B T_s}\right) - 1\right] + g_{gr} V_{GS} \exp\left(-\frac{qV_{GS}\delta_g}{k_B T_s}\right)\right\} \ldots\ldots (24)$$

$$I_{gd} = \frac{LW}{2}\left\{A^*\left[T_d^2 \exp\left(-\frac{q\Phi_B}{k_B T_d}\right)\exp\left(\frac{q(V_{GS} - V_{DSE})}{nk_B T_d}\right) - T_s^2 \exp\left(-\frac{q\Phi_B}{k_B T_s}\right)\right]\right.$$
$$\left. + g_{gr} V_{GD} \exp\left(-\frac{qV_{GD}\delta_g}{k_B T_d}\right)\right\} \ldots\ldots\ldots\ldots\ldots\ldots (25)$$

In our model, we have ignored the difference between effective electron temperature at the drain and source side. Assuming, $T_d = T_s = T$ and making $\frac{k_B T}{q} = V_{kT}$, our simplified gate current equations are

$$I_{gs} = \frac{LW}{2}\left\{A^* T^2\left(-\frac{\Phi_B}{V_{kT}}\right)\left[\exp\left(\frac{V_{GS}}{nV_{kT}}\right)-1\right]+g_{gr}V_{GS}\left(-\frac{V_{GS}\delta_g}{V_{kT}}\right)\right\} \dots\dots\dots (26)$$

$$I_{gd} = \frac{LW}{2}\left\{A^* T^2\left(-\frac{\Phi_B}{V_{kT}}\right)\left[\exp\left(\frac{V_{GS}-V_{DSE}}{nV_{kT}}\right)-1\right]+g_{gr}V_{GD}\left(-\frac{V_{GD}\delta_g}{V_{kT}}\right)\right\} \dots\dots\dots (27)$$

4.4 C-V Model

Like all other electrical circuits, transistors have internal capacitance, which can cause their behavior to depart from that of 'ideal' circuit elements. Aside from dc characteristics, capacitance modeling in AlGaN/GaN MODFETs is extremely important in order to accurately and reliably simulate high-speed digital and analog circuits in microwave and millimeter wave regime. In case of power switching application, capacitances are of great concern since the switching frequency is directly related to the capacitances.

The same C-V model for MOSFET can be applied to HFET by only modifying the expression for the gate-channel capacitance C_{ch} to account for the saturation in the channel electron sheet carrier density n_s. Following Eq. (11), the unified HFET gate channel capacitance at zero drain-source voltage can be written as

$$C_{ch} = WLq\frac{dn_s}{dV_{GS}} \approx \frac{C'_{ch}}{\left[1+\left(\frac{n'_s}{n_{smax}}\right)^{\gamma}\right]^{1+1/\gamma}} \dots\dots\dots\dots\dots\dots (28)$$

where and L and W are the gate length and width, respectively, q is the unit charge, and V_{GS} is the intrinsic gate to source bias. C'_{ch} is the unified gate channel capacitance for a potential well with infinite depth.

MOSFET **HFET**

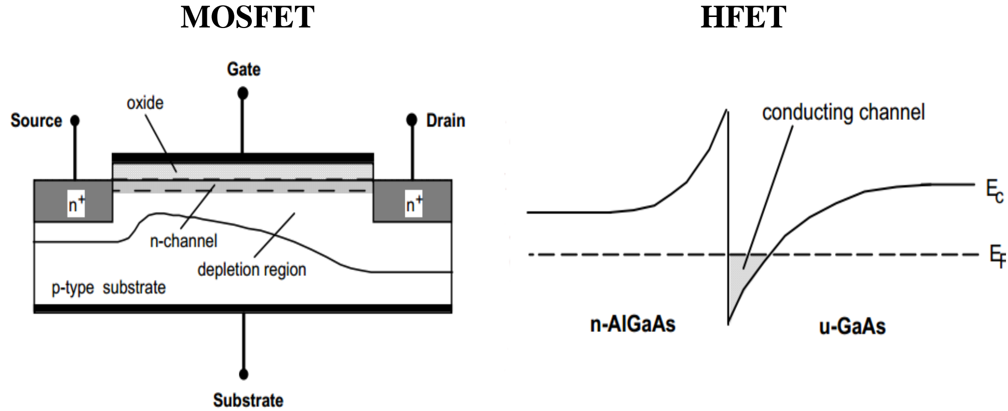

Figure 4.15 Gate channel capacitance in MOSFET and HFET

$$qn_s = C_i' V_{GT} \qquad\qquad qn_s = C_i' V_{GT}$$

$$C_i' = \frac{\varepsilon_i \varepsilon_0}{d} \qquad\qquad C_i' = \frac{\varepsilon_i \varepsilon_0}{d + \Delta d}$$

The difference in the expression of gate channel capacitance between MOSFET and HFET is that, in case of HFET, we have to consider an additional thickness which is the effective thickness of the 2-DEG layer. Above threshold, C_{ch} increases rapidly and reaches its maximum value $C_i = LWC_i'$. However, C_{ch} will decrease when n_s' is comparable to or larger than n_{smax}.

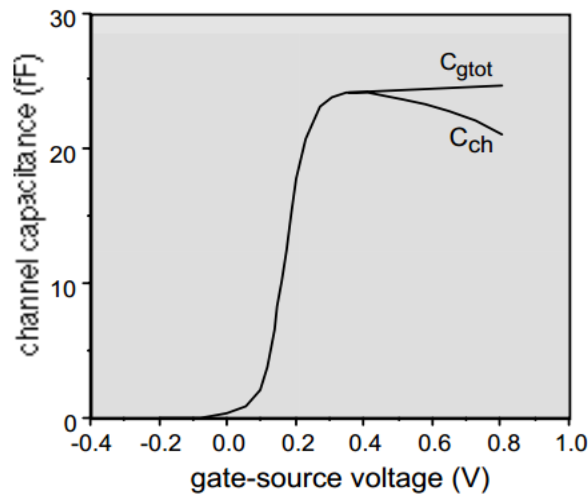

Figure 4.16 Calculated gate channel capacitance C_{ch} and total capacitance C_{gtot} for an HFET with gate length 1μm and gate width 20μm

According to Byun et al. [18], the saturation in n_s is aided by an increase in the electron sheet density n_t in the barrier layer. The additional charge gives rise to another capacitance C_{g1}. The total differential gate capacitance C_{gtot} can then be represented as a parallel combination of the channel capacitance C_{ch} and C_{g1}. This added charge contributes to the total differential gate capacitance C_{gtot}, which can be represented as a parallel coupling of C_{ch} and the capacitance C_{g1} associated with this added charge. In case of an HFET with delta-doped wide bandgap barrier layer, we may assume that the electrons in the barrier layer are at a fixed distance from the gate and independent of the gate bias. Then, this charge can be treated as the channel charge. If the onset of strong inversion in the wide bandgap layer is characterized by a threshold voltage, the capacitance can be expressed as

$$C_{g1} = \frac{C_i}{1 + 2\exp\left(-\frac{V_{GS} - V_{T1}}{\eta_1 V_{th}}\right)} \ldots\ldots\ldots\ldots\ldots\ldots (29)$$

Here V_{th} is the thermal voltage, V_{GS} is the intrinsic gate source voltage, V_{T1} is the threshold voltage characterizing the onset of significant charge transfer from the channel to the barrier layer and η_1 is a suitable ideality factor. Fig. 4.16 shows values of C_{ch} calculated from equation (28), and the total gate capacitance for a typical HFET with nominal gate length $L = 1\mu m$ and gate width $W = 20\mu m$. The drop in C_{ch} at large gate bias is related to the saturation of the channel charge density; on the other hand, the slight increase in C_{gtot} is due to the increase of carrier density in the parallel channel in the wide bandgap layer.

Using unified gate-channel capacitance along with Meyer's capacitance model [42], we can obtain continuous expressions for the intrinsic gate-source and the gate-

drain capacitances, valid for all regions of operation [15]. However, Meyer model can only provide the dominant, intrinsic FET capacitances.

$$Q_G = \frac{2}{3} C_i \frac{(V_{GS} - V_T)^3 - (V_{GD} - V_T)^3}{(V_{GS} - V_T)^2 - (V_{GD} - V_T)^2} \ldots \ldots \ldots \ldots \ldots (30)$$

$$C_{GS} = \frac{\partial Q_G}{\partial V_{GS}} \Big|_{V_{GD}, V_{GB}} \qquad C_{GD} = \frac{\partial Q_G}{\partial V_{GD}} \Big|_{V_{GS}, V_{GB}}$$

$$C_{gs} = \frac{2}{3} C_i \left[1 - \left(\frac{V_{GT} - V_{DS}}{2V_{GT} - V_{DS}}\right)^2\right] \ldots \ldots (31) \qquad C_{gd} = \frac{2}{3} C_i \left[1 - \left(\frac{V_{GT}}{2V_{GT} - V_{DS}}\right)^2\right] \ldots \ldots (32)$$

But using Meyer's capacitance formulas, we never achieved stable transient response. In most cases, we haven't observed any capacitive effect.

A capacitor is a component whose charge is a function of voltage. Its capacitance is defined as the derivative of charge with respect to voltage,

$$C(v) = \frac{dq(v)}{dv} \ldots \ldots \ldots \ldots \ldots \ldots (33)$$

The current through a capacitor is simply the time-derivative of the charge,

$$i(t) = \frac{dq(v(t))}{dt} \ldots \ldots \ldots \ldots \ldots \ldots (34)$$

This can be expanded to

$$i(t) = \frac{dq(v(t))}{dv(t)} \frac{dv(t)}{dt} = C\big(v(t)\big) \frac{dv(t)}{dt} \ldots \ldots \ldots \ldots \ldots (35)$$

Though Eq. (34) and Eq. (35) are equivalent, it is problematic for the simulator if we use Eq. (35) to build models. Simulator solve the circuit equations at different points by breaking time into discrete steps. The same C(v) is used across each step, which results in small errors on every step. This leads a problem of charge not being conserved if the capacitor is nonlinear. At every step of the simulation, a small amount of charge is either

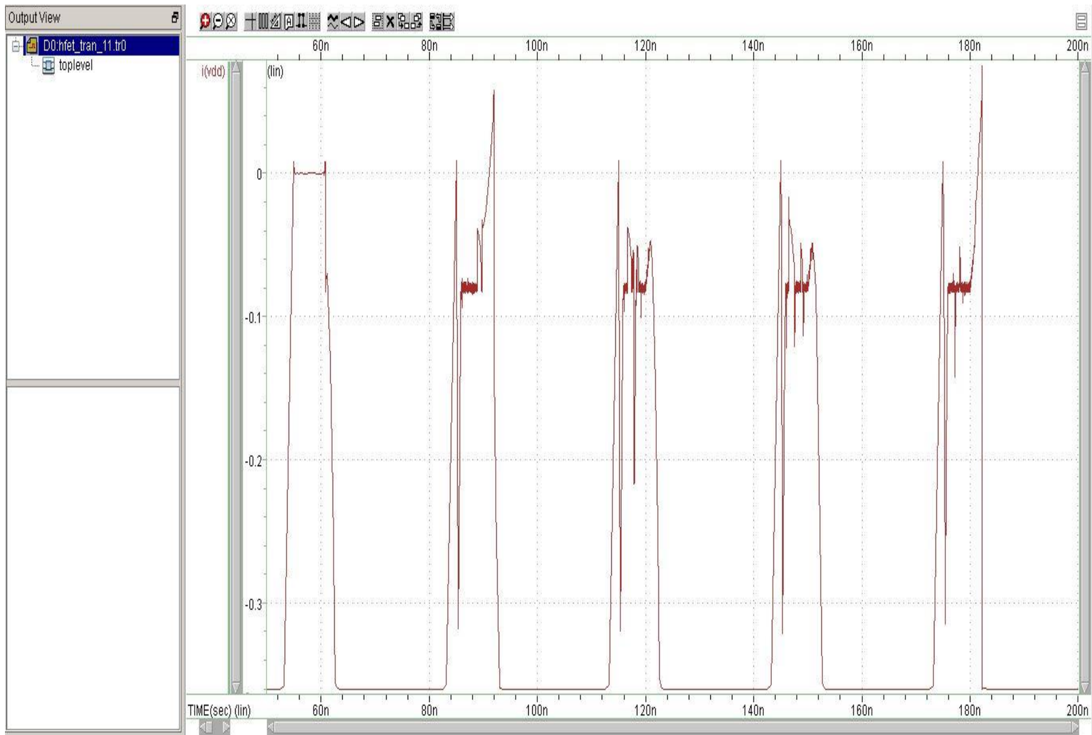

Figure 4.17 Highly unstable transient response using Meyer’s capacitance model

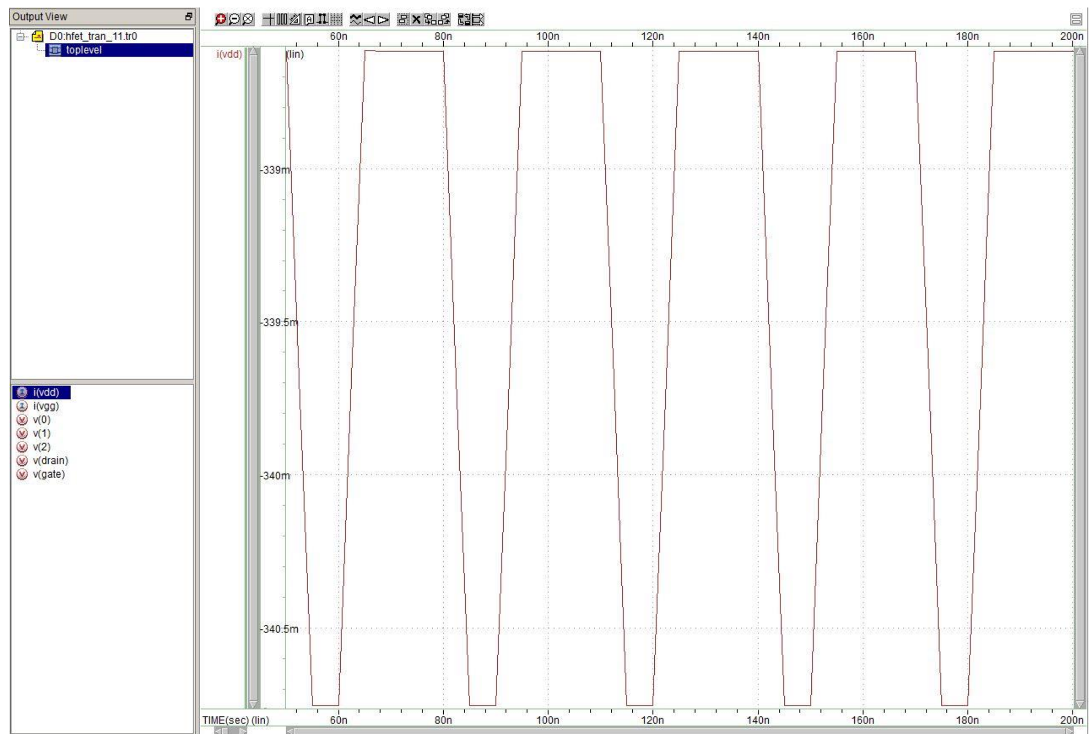

Figure 4.18 Voltage amplitude showing switching but no capacitive effect

created or destroyed. If there is not much tolerance, the amount of charge that is not conserved is small. However, the problem can be severe in many typical cases. One of the manifestation of this problem is that an unknown DC current flows through the device [43]. This problem does not occur if (34) is used.

If a capacitor is linear, its charge is $q = Cv$ and current

$$i(t) = \frac{d\big(Cv(t)\big)}{dt} \dots\dots\dots\dots\dots\dots (36)$$

$$i(t) = C\frac{dv(t)}{dt} \dots\dots\dots\dots\dots\dots (37)$$

Modeling a nonlinear capacitor by replacing C with $C(v)$ in (37) is identical to using (35) and does not conserve charge. However, the problem becomes significant if C is replaced with $C(v)$ in (36).

$$\frac{d\Big(C\big(v(t)\big)v(t)\Big)}{d(t)} \neq C\big(v(t)\big)\frac{dv(t)}{dt} \dots\dots\dots\dots\dots (38)$$

Because $C\big(v(t)\big)$ itself varies with time. Thus using

$$\frac{d\Big(C\big(v(t)\big)v(t)\Big)}{d(t)} = C\big(v(t)\big)\frac{dv(t)}{dt} \dots\dots\dots\dots\dots (39)$$

Produces large errors if C is a strong function of v and v varies significantly with t.

Solution

Charge based model formulation is required. We tried several gate charge models and obtained best result using Agilent EEHEMT1 Gate charge model in terms of transient response.

Agilent EEHEMT1 Gate Charge Model

The Agilent EEHEMT1 gate charge model was developed through careful examination of extracted device capacitances over bias [44]. The model consists of simple closed form charge expressions whose derivatives fit observed bias dependencies in capacitance data. This capacitance data can be obtained directly from measured Y-parameter data.

$$Q_G(V_J, V_O) = \left[\frac{C_{11O} - C_{11TH}}{2} \cdot \left\{V_J - V_{INFL} + \frac{DELTGS}{3}\ln\left(\cosh\left(\frac{3}{DELTGS}\cdot\left(V_J - V_{INFL}\right)\right)\right)\right\} + C_{11TH} \cdot \left(V_J - V_{INFL}\right)\right] \cdot \left(1 + LAMBDA \cdot (V_O - V_{DSO})\right) - C_{12SAT} \cdot V_O \ldots\ldots\ldots (40)$$

$$with\ V_J(V_{GS'}, V_{DS}) = 0.5 \cdot \left(2V_{GS'} - V_{DS} + \sqrt{V_{DS}^2 + DELTDS^2}\right)$$

$$V_O(V_{DS}) = \sqrt{V_{DS}^2 + DELTDS^2}$$

The gate charge is partitioned into two charge sources Q_{GS} and Q_{GD}. The equations for these charge sources are

$$Q_{GS}(V_{GS'}, V_{GD'}) = \left[Q_G\left(V_J(V_{GS'}, V_{GS'} - V_{GD'}), V_O(V_{GS'} - V_{GD'})\right) - C_{GDSAT} \cdot V_{GD'}\right] \cdot f_1 + C_{GDSAT} \cdot V_{GS'} \cdot f_2 \ldots\ldots\ldots\ldots\ldots\ldots (41)$$

$$Q_{GD}(V_{GS'}, V_{GD'}) = \left[Q_G\left(V_J(V_{GS'}, V_{GS'} - V_{GD'}), V_O(V_{GS'} - V_{GD'})\right) - C_{GDSAT} \cdot V_{GS'}\right] \cdot f_2 + C_{GDSAT} \cdot V_{GD'} \cdot f_1 \ldots\ldots\ldots\ldots\ldots\ldots (42)$$

with the smoothing factor f_1 and f_2 defined as

$$f_1 = 0.5 \cdot \left(1 + \tanh\left(\frac{3}{DELTDS} \cdot (V_{GS'} - V_{GD'})\right)\right)$$

$$f_2 = 0.5 \cdot \left(1 - \tanh\left(\frac{3}{DELTDS} \cdot (V_{GS'} - V_{GD'})\right)\right)$$

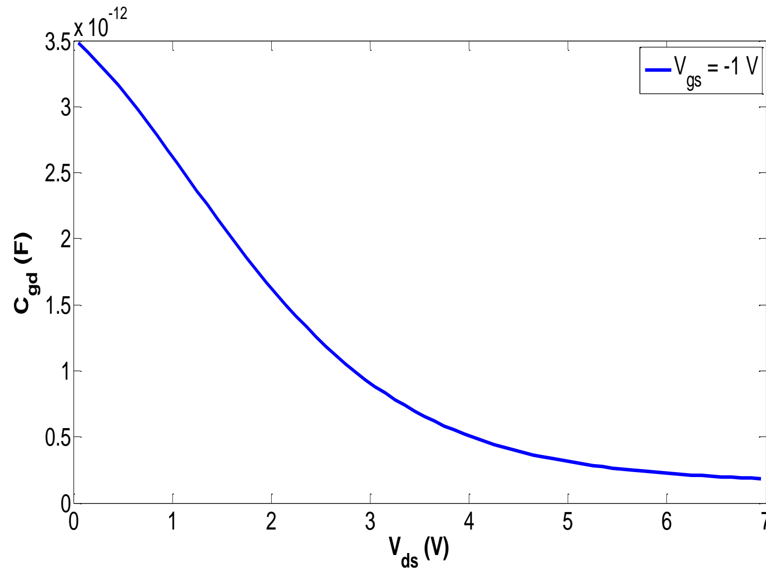

Figure 4.19 Gate to drain capacitance using Agilent EEHEMT1 gate charge model

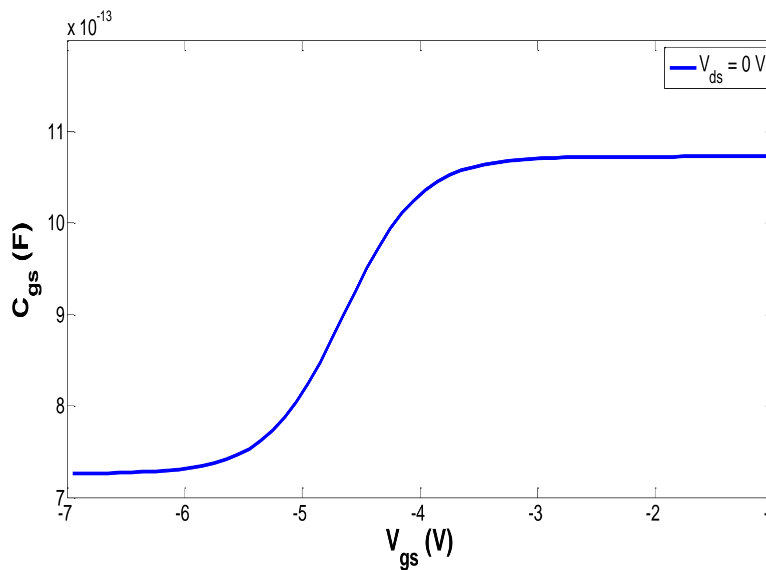

Figure 4.20 Gate to source capacitance using Agilent EEHEMT1 gate charge model

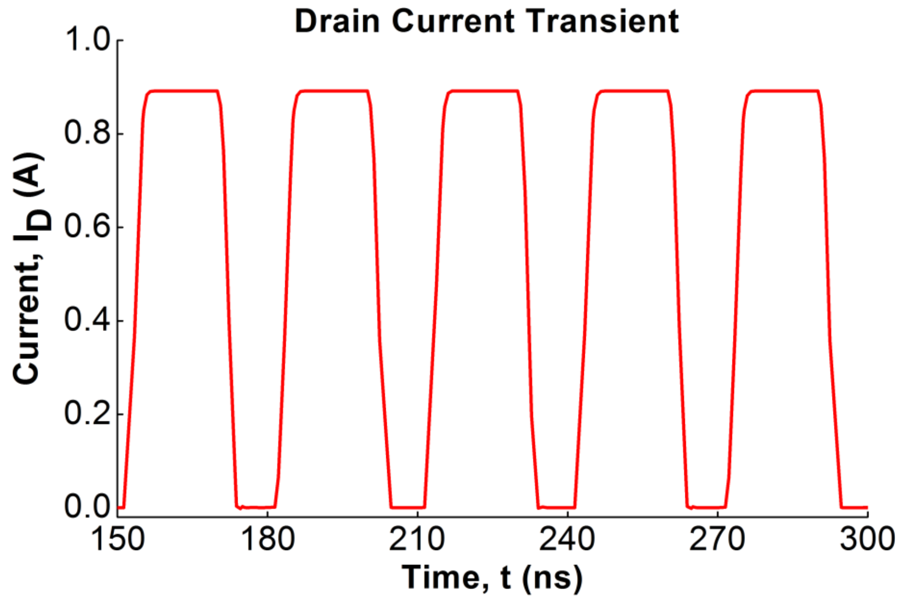

Figure 4.21 Very stable drain current transient using Agilent EEHEMT1 gate charge model

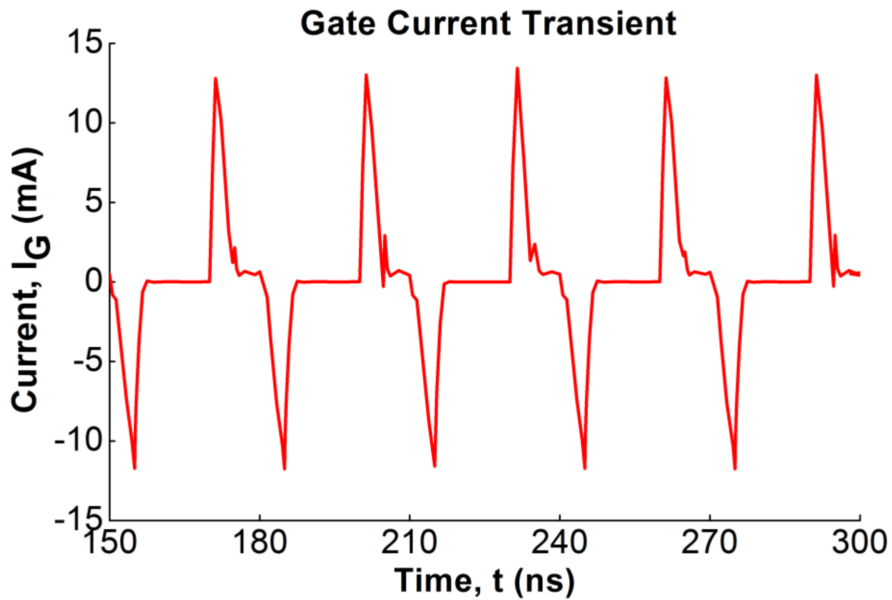

Figure 4.22 Very stable gate current transient using Agilent EEHEMT1 gate charge model

As evident from Fig 4.21 and Fig. 4.22, Agilent EEHEMT1 gate charge model very stable drain and gate transient response.

4.5 Field Pates

The electric field in the HFET channel peaks at the drain-edge of the gate, which significantly reduces device breakdown voltage. A field plate can reduce the electric field at the gate edge by providing an additional edge for the electric field lines to terminate. The field plate is a metal electrode located over the gate and extending into the region between gate and drain. This leads to a new electric field peak at the edge of the field plate which reduces the original peak electric field at the gate edge and the extending of the depletion region beneath the gate. It helps to spread the electric field between gate and drain more uniformly. Field plate also improves device linearity, stability, efficiency and reliability by suppressing current collapse, gate leakage and surface trapping effects. Many groups have reported the use of field plates and it's long been recognized as an effective method to increase device breakdown voltage and decrease leakage current. The technique has been applied to AlGaN/GaN HEMTs with great success.

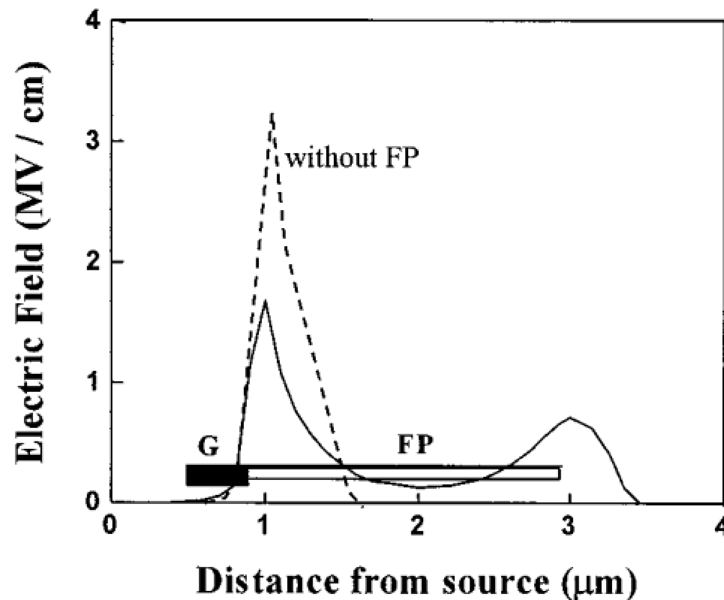

Figure 4.23 Comparison of longitudinal electric field profiles at the channel side of heterojunction in AlGaN/GaN HEMTs with and without a field plate

For power-switching applications, normally off operation is needed for safety consideration. Low gate leakage current is needed for achieving high breakdown voltage. It also reduces power consumption and enable easy gate drive design. During high voltage operation, GaN HEFTs show a reduction of dynamic Ron when the device is switched from OFF-state to ON-state. The dynamic Ron degradation significantly affects the power switching efficiency of GaN FETs and is attributed to electron trapping in the region between the gate and the drain. Use of field plates can mitigate the reduction of dynamic Ron hence increases efficiency and switching speed.

The function of filed plates is to reduce peak electric field by modifying electric field distribution, hence reducing trapping effect and increasing breakdown voltage. Generally, two different types of field plates are deployed, namely Source-connected Field Plate and Gate-connected Field Plate. Source-connected field plate is mainly used to minimize the drawback of gate to drain feedback capacitance introduced by Gate-connected field plate which significantly reduces device gain.

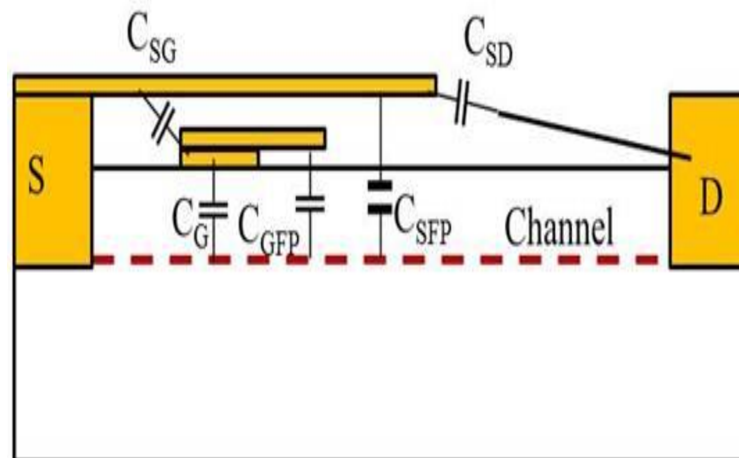

Figure 4.24 Additional capacitances introduced by Source and Gate-connected field plates

However, field plates introduce additional capacitances and reduce device transconductances. To accurately simulate device characteristics, the capacitances introduced by the field plates must be incorporated in the model. Figure 4.24 shows various capacitances associated with the source and gate-connected field plates.

In our model, we have applied the same approach to incorporate field-plate capacitances as we did for gate capacitances. Modified Agilent EEMEMT1 model equations are used to calculate FP charges

$$Q_{GGFP}\left(V_{JGFP}, V_{OGFP}\right)$$

$$= \left[\frac{C_{11OGFP} - C_{11THGFP}}{2}\right.$$

$$\cdot \left\{V_{JGFP} - V_{INFL} + \frac{DELTGS}{3}\ln\left(\cosh\left(\frac{3}{DELTGS}\cdot\left(V_{JGFP} - V_{INFL}\right)\right)\right)\right\}$$

$$\left. + C_{11THGFP}\cdot\left(V_{JGFP} - V_{INFL}\right)\right]\cdot\left(1 + LAMBDA\cdot(V_{OGFP} - V_{DSO})\right)$$

$$- C_{12SATGFP}\cdot V_{OGFP} \dots\dots\dots (43)$$

$$with\ V_{JGFP}(V_{GS'}, V_{DS}) = 0.5\cdot\left(2V_{GS'} - V_{DS} + \sqrt{V_{DS}^2 + DELTDSGFP^2}\right)$$

$$V_{OGFP}(V_{DS}) = \sqrt{V_{DS}^2 + DELTDSGFP^2}$$

The FP charge is partitioned into two charge sources Q_{GS} and Q_{GD}. The equations for these charge sources are

$$Q_{GSGFP}(V_{GS'}, V_{GD'})$$

$$= \left[Q_{GGFP}\left(V_{JGFP}(V_{GS'}, V_{GS'} - V_{GD'}), V_{OGFP}(V_{GS'} - V_{GD'})\right) - C_{GDSATGFP}\right.$$

$$\left.\cdot V_{GD'}\right]\cdot f_{GFP1} + C_{GDSATGFP}\cdot V_{GS'}\cdot f_{GFP2} \dots\dots\dots\dots\dots\dots (44)$$

$$Q_{GDGFP}(V_{GS'},V_{GD'})$$
$$= \left[Q_{GGFP}\left(V_{JGFP}(V_{GS'},V_{GS'}-V_{GD'}),V_{OGFP}(V_{GS'}-V_{GD'})\right) - C_{GDSATGFP} \cdot V_{GS'}\right] \cdot f_{GFP2} + C_{GDSATGFP} \cdot V_{GD'} \cdot f_{GFP1} \dots\dots\dots\dots\dots\dots (45)$$

with the smoothing factor f_{GFP1} and f_{GFP2} defined as

$$f_{GFP1} = 0.5 \cdot \left(1 + \tanh\left(\frac{3}{DELTDSGFP} \cdot (V_{GS'} - V_{GD'})\right)\right)$$

$$f_{GFP2} = 0.5 \cdot \left(1 - \tanh\left(\frac{3}{DELTDSGFP} \cdot (V_{GS'} - V_{GD'})\right)\right)$$

The gate-drain, gate-source and output capacitances in the presence of field plates are shown in Fig. 4.25, 4.26 and 4.27 respectively.

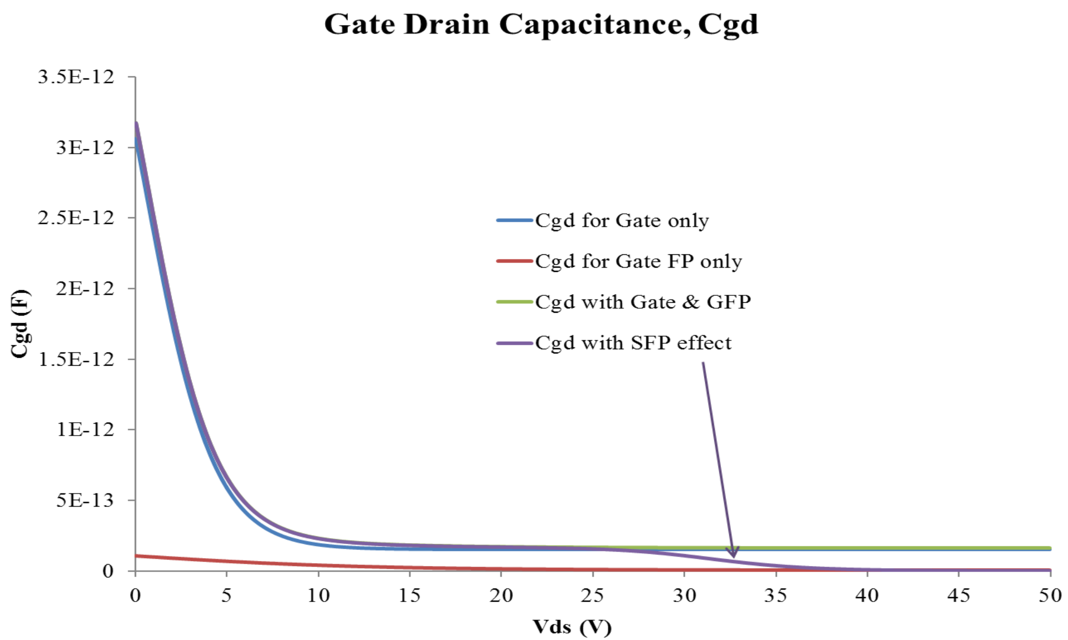

Figure 4.25 Gate to Drain capacitance with field plates using modified Agilent EEMEMT1 gate charge model

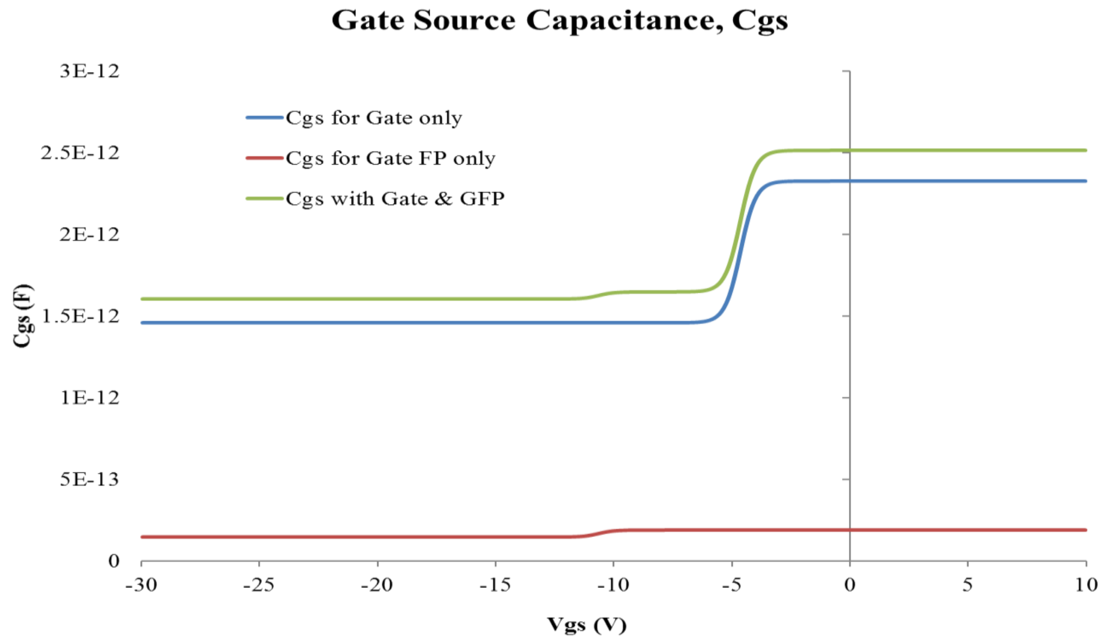

Figure 4.26 Gate to Source capacitance with field plates using modified Agilent EEMEMT1 gate charge model

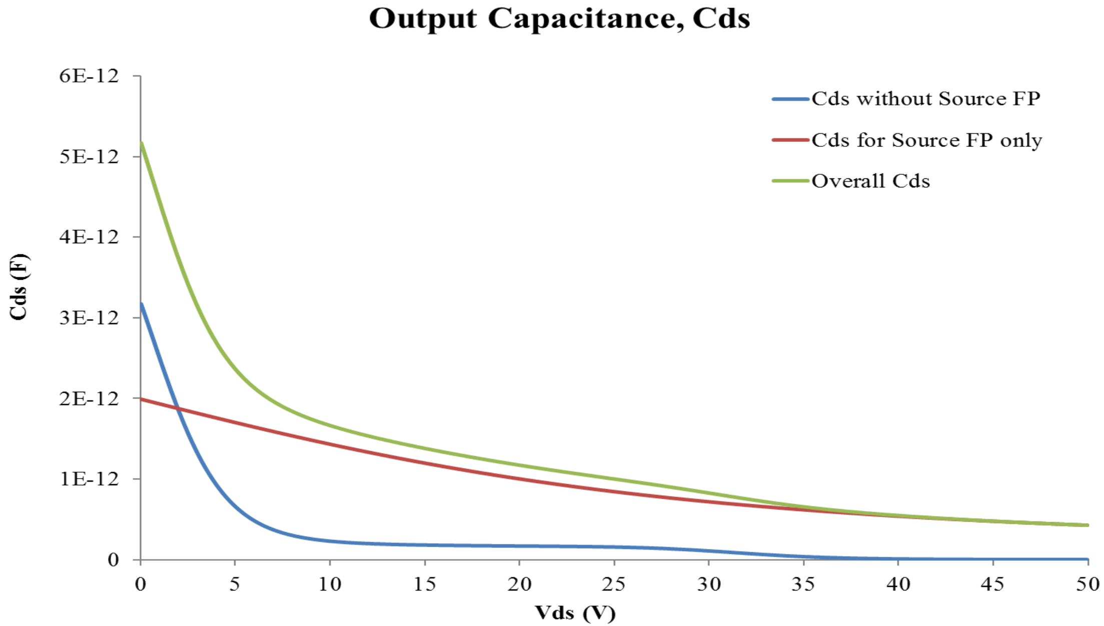

Figure 4.27 Output capacitance with field plates using modified Agilent EEMEMT1 gate charge model

The transient responses with field plates are shown in Fig. 4.28 and Fig. 4.29.

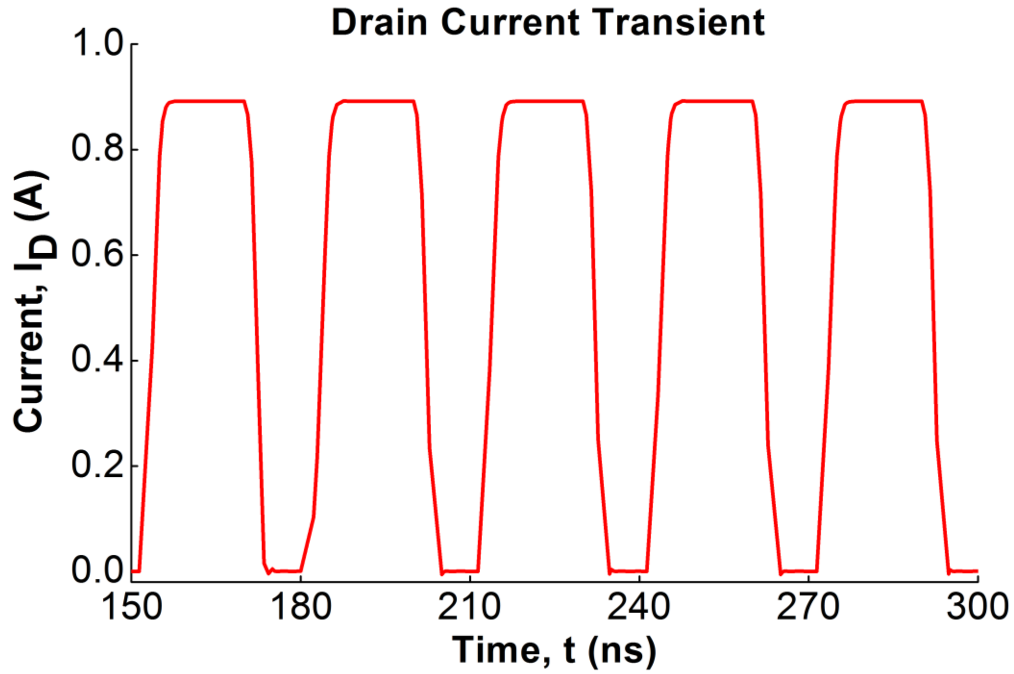

Figure 4.28 Drain current transient with field plate capacitances

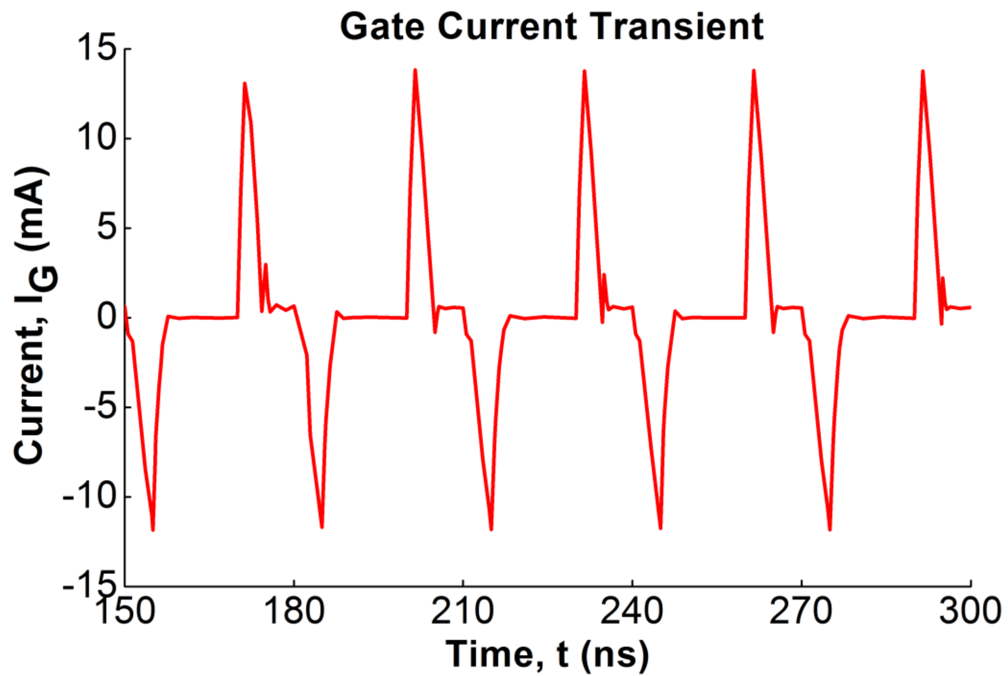

Figure 4.29 Gate current transient with field plate capacitances

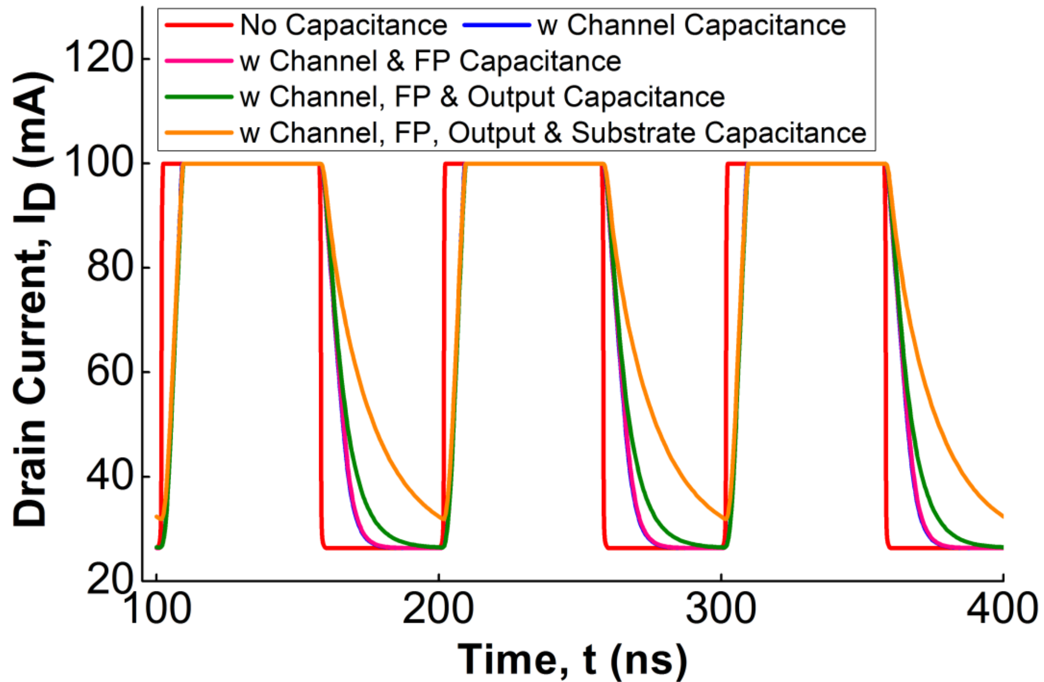

Figure 4.30 Drain current transient response after adding different capacitances compared to the transient response without any capacitance

As evident from Fig. 4.30, the transient responses are very stable with all the associated capacitances which is highly desirable for power switching applications.

4.6 Current Collapse

Current collapse (also known as gate and drain lags) is mainly referred to as the temporary reduction of drain to source current immediately after the application of high voltage. When there is large lattice mismatch such as that between GaN and silicon, the active region in the device will have a relatively higher concentration of dislocations and other defects. These defects in the HEMT channel trap a significant number of electrons at high voltages. This leads to the dynamic current-voltage (I-V) characteristics of power HEMTs which differ from the static ones during fast switching.

In 1994, Khan et al. first observed current collapse in GaN based HEMTs [45]. The effect has been studied thoroughly in the last two decades. The most important manifestation of current collapse is the temporary increase of channel resistance in the source to gate and gate to drain regions [46] as suggested by many studies [47, 48]. Conduction loss is one of the most important component during the switching of GaN HEMT from the off-state (gate voltage below threshold and high drain voltage) into the on-state (gate voltage above threshold, low drain voltage). The loss is given by

$$P_{CL} \approx V_{ON} \times I_{ON} = I_{ON}^2 \times R_{ON};$$

where V_{ON} and I_{ON} are the on-state voltage across and current through the device, R_{ON} is the on-state resistance of HEMT. In case of current collapse, the on-resistance of HEMT can be significantly higher than the static resistance which leads to excessive conduction loss. Numerous analytical and TCAD models [49, 50] has been used to study current collapse in GaN HEMTs, yet there is no simple, fast and accurate compact current collapse model for GaN HEMT switches. We have developed a compact model for current collapse which is especially suitable for SPICE type circuit simulators [51].

4.6.1 Transient Current Collapse Model

The HEMT regions mostly affected by carrier trapping are the source to gate and gate to drain regions as suggested by numerous studies (see, e.g. [46, 49]), represented correspondingly by R_S and R_D access resistances. These access resistances increase in the presence of current collapse. The additional resistances are related to the carrier trapping in the source to gate and gate to drain regions. The access resistances in the presence of current collapse can be written as

$$R_D = R_{D0} + R_{DCC} \text{ and } R_S = R_{S0} + R_{SCC}.$$

where R_{D0} and R_{S0} are the access resistances in the absence of current collapse and R_{DCC} & R_{SCC} are the access resistances due to current collapse.

In power switching applications, HEMT is turned on from the off state by increasing the gate voltage from below threshold to above threshold and decreasing the drain voltage below the knee voltage. Typically, the gate pulse rise and fall times are much faster than the time required for the trapped charges to change state. This causes lagging of the source and drain access resistances. As a result, there is a delay for the on-state current to reach the steady-state value corresponding to its DC I-V. When the switch goes from on to off-state, the drain voltage increases and trapped charges get released. During this transition, the HEMT channel under the gate quickly shuts off and there is no current flow, that's why the dynamic increase of R_S and R_D in this case is not as important as it is in the case of off-to-on transition. The characteristic de-trapping time or the current collapse recovery time in GaN HEMTs varies from microseconds to hours depending on the material quality, device layout, surface passivation and processing technology [50, 52].

The transient behavior of the additional source and drain access resistances can be described by introducing the effective gate to source and gate to drain lagging voltages V_{GLAG} and V_{DLAG} [51]. We have modelled the lagging using an auxiliary RC circuit, the same approach we used to simulate self-heating. The RC equivalent circuit for simulating V_{DLAG} is shown in Fig. 4.31. The characteristic current collapse time is given by the input parameter $\tau_{CC} = R_{CC}C_{CC}$. Fig. 4.31 (a) shows one cell equivalent circuit. The value of the equivalent capacitance C_{CC} is chosen arbitrarily for a particular τ_{CC}. The equivalent

current source I_{CC} is calculated from the instant drain-source voltage V_{DS}, $I_{CC} = V_{DS}/R_{CC}$. Similar equivalent circuit is used to simulated V_{GLAG}. Usually, current collapse related transients have more than one characteristic time. Using this approach, we can use two or more RC equivalent circuits to simulate current collapse related transients. We have used the one cell model for simulating current collapse so far but our model also incorporates the two cell model shown in Fig. 4.31 (b).

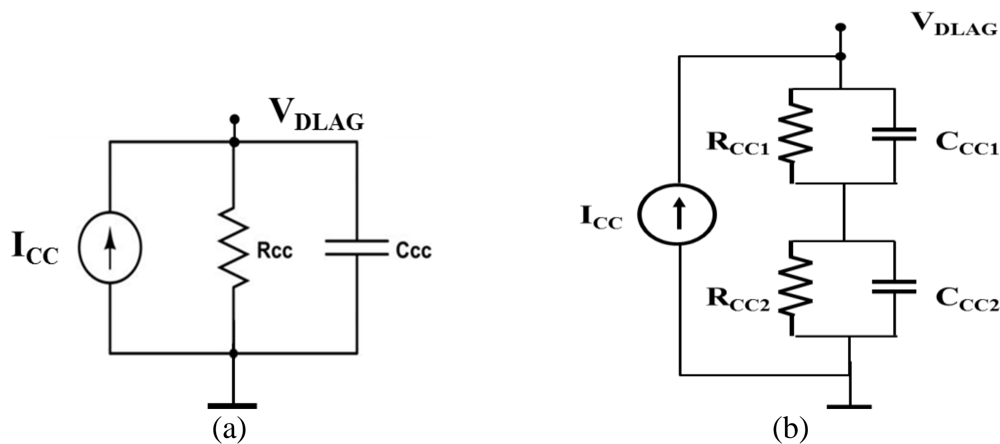

Figure 4.31 One-cell (a) and two-cell (b) equivalent circuits for transient lagging drain voltage V_{DLAG} simulations. Similar equivalent circuits are used to simulate gate lagging voltage V_{GLAG}

The V_{DS} value not affected by current collapse or the time dependent value of V_{DS} can be obtained from any available HEMT compact models (see, e.g. [49]). The drain and source access resistance R_{DCC} and R_{SCC} due to current collapse are then calculated from the generated lagging drain and source voltages V_{DLAG} and V_{SLAG} obtained from the RC circuits. R_{DCC} and R_{SCC} has complex dependency on the instant gate to source and drain to source voltages. Koudymov et al. [49] derived an analytical expression to find the time-dependent values of these additional drain and source access resistances. The formulas have the advantage of having a closed form. However, it is often hard to obtain

the device and material parameters such as effective channel thickness, equilibrium carrier densities, trap concentrations and generation/capture rates, surface potential etc. On top of these parameters, the authors [49] have used some additional fitting parameters. In this work, we have developed a model with a much simpler approximation [51] which is based on the same basic physical model as in [49]:

$$R_{DCC}(t) = R_{D0} \times b_D * \left(\frac{V_{DLAG}}{|V_{TH}|}\right)^{m_D} \ldots\ldots\ldots\ldots\ldots (41)$$

$$R_{SCC}(t) = R_{S0} \times b_S * \left(\frac{V_{GLAG}}{|V_{TH}|}\right)^{m_S} \ldots\ldots\ldots\ldots\ldots (42)$$

for the drain and source access resistances correspondingly.

Excellent fitting of the experimentally observed current-collapse related access resistances has been obtained using Eq. 41 and 42. R_{D0} and R_{S0} are the drain and source access resistances in the absence of current collapse, V_{TH} is the absolute value of the threshold voltage, b_D and m_D and b_S and m_S are the fitting parameters for the drain and source access resistances correspondingly.

4.6.2 Fast I-V Model in Presence of Current Collapse

When the duration of the switching pulse is much faster than the recovery time of current collapse, the values of the additional access resistances R_{DCC} and R_{SCC} due to current collapse remain nearly the same after the switch goes on from the off-state. The measured I-V characteristics, in these cases are often referred to as “fast” or “dynamic” I-Vs. Consequently, R_{DCC} and R_{SCC} gets affected only by the highest drain and gate voltages applied immediately before the measurement of the I-V characteristics [51].

In our model, we have introduced three different modes to activate or deactivate current collapse. When, cc = 0, current collapse is deactivated; cc = 1 activates the fast or stationary current collapse mode. In this case, $V_{DLAG} = V_{DMAX}$ and $V_{SLAG} = |V_{GMIN}|$. V_{DMAX} and V_{GMIN} are the drain and gate voltages applied to the device immediately before measuring the fast I-Vs. To activate transient current collapse mode, cc = 2 value is selected and R_{DCC} and R_{SCC} are calculated using equation 1 and 2 from the generated V_{DLAG} and V_{SLAG} values from the RC circuits.

4.7 Bulk Current

GaN on Silicon HEMT is very suitable for commercialization for its low cost and scalability to large size. However, due to the conducting nature of Silicon, the drain to substrate current is significantly higher. Drain to substrate current or bulk current is a very important for power switching applications specially in the off-state of the device when high drain bias is applied. Bulk current can significantly increase loss, cause premature breakdown and negatively affects reliability of power GaN HEMTs on Si substrates. Although different research groups have reported significant drain to bulk currents in GaN on Silicon HEMTs [53-56]; currently there is no physical model that can describe the bulk current properly.

4.7.1 Equivalent Barrier Model

In real GaN HEMTs, there are multiple strain relief layers on top of the nucleation layer between GaN and Si substrate because of the large lattice mismatch between GaN and Silicon. The transition layers are designed to ensure that the structure is crack free and

there is no unintentional parasitic channel formation. The transport mechanism in these highly defective layers are complex or hard to describe using conventional carrier transport equations. To describe the bulk current, we have introduced a simple, efficient and effective approach based on the idea that, there is an equivalent Schottky barrier at the GaN/Si interface [57].

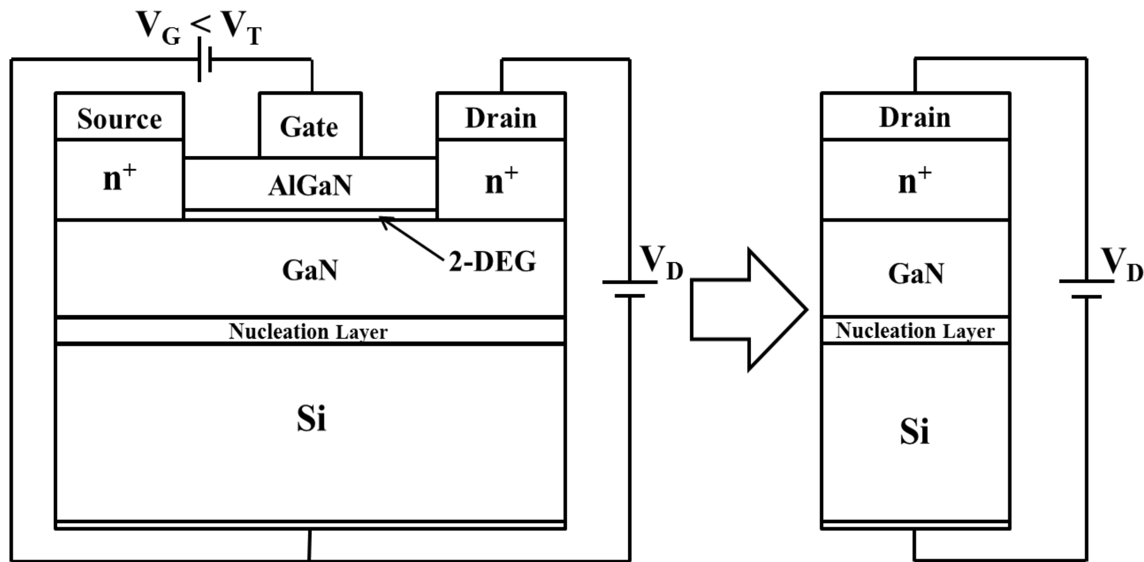

Figure 4.32 (a) Typical AlGaN/GaN HEMT device layout and setup for bulk current measurement in GaN on Si power HEMTs, (b) Equivalent two terminal structure to measure bulk current in the off-state

Fig. 4.32(a) shows the typical experimental setup for bulk current measurement in GaN on Si HEMTs. Fig. 4.32(b) illustrates our approach. Under normal operating conditions, the source and substrate is grounded, gate voltage is lower than the threshold voltage and a high drain bias, typically above 100V to 1kV or higher is applied at the drain electrode [58, 59]. In this setup condition, the channel under the gate is off and most of the bulk current flows between the drain and substrate electrodes. As there is no current flow from the drain to the source, the three terminal structure shown in Fig. 4.32(a) can be

simplified to the two terminal structure shown in Fig. 4.32(b) for bulk current measurement.

GaN bandgap is much larger than that of Si, which makes the heterointerface between GaN and Si behave like a quazi-metal-semiconductor junction as illustrated in [60]. Fig. 4.33 compares the low voltage region of the experimental bulk current I-V [61]

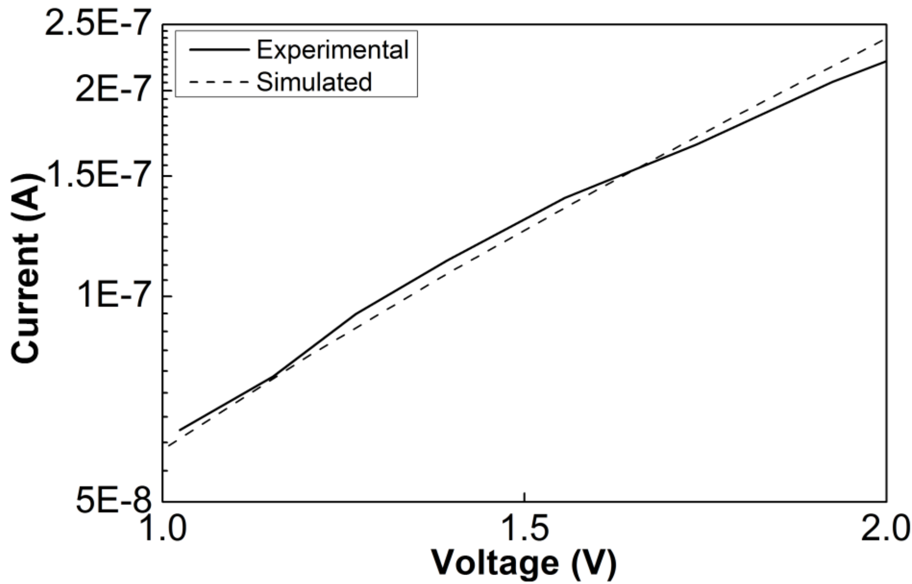

Figure 4.33 Experimental [61] low voltage bulk current I-V compared to Schottky diode equation

with simulated non-ideal Schottky diode I-V. As seen, a close fitting has been obtained which further validates that the interface acts like a rectifying junction. The ideality factor is found to be n ≈ 35 which is much higher than the value normally observed in a regular p-n or metal-semiconductor junction. These unusually high ideality factors are fairly common in III-Nitrides [62-64] due to the presence of high concentration of defects in the micro or nano-interfaces. In [64], an ideality factor of 50 has been reported. Under normal operating conditions, the drain is at a higher potential than the substrate, corresponding to a reverse-biased bottom equivalent Schottky barrier. When drain bias is

low, the Schottky barrier offers a very high resistance and current flow between the drain and the substrate is not much affected by bulk material properties.

In our proposed model [57], Si side acts as the metal of the equivalent Schottky barrier junction, an approach that has been successfully applied previously [40] to explain gate currents in HFETs. It is to be noted that the properties of silicon do not have significant effect on the bulk current, the substrate simply acts as a series resistance with the Schottky barrier. The voltage drop across this resistance can be ignored because the bulk current in GaN on Si HEMTs is typically very small.

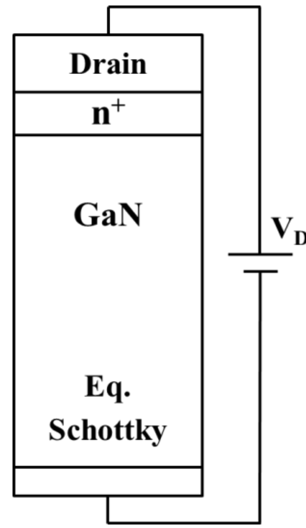

Figure 4.34 Equivalent barrier height approach for simulating current through GaN/Si interface

Bulk current in GaN HEMTs is affected by various material related parameters such as doping, trap concentration, trap type, buffer quality and the properties of GaN/Si interface. It also depends on the nucleation layer material and properties. We have introduced a novel approach to simulate the bulk current in GaN on Si HEMTs based on the fitting in Fig. 4.33. In Fig. 4.34, the Si/GaN interface is replaced by an equivalent Schottky barrier height to characterize the carrier transport through Si/GaN interface.

TCAD simulations have been performed using Synopsys Sentaurus device simulator which is widely used industry level simulator for a long time. During simulations, physical mechanisms such as polarization, thermionic emission for both electrons and holes, Shockley–Read–Hall recombination for trap-assisted tunneling, direct band-to-band tunneling, trap capture – escape processes for donor and acceptor trap types with various energy position and cross-section and Poole-Frenkel effect were incorporated. The model outcomes were validated for the critical task processes using simple test structures before actual bulk current simulations.

The simulated structure in this work consists of 5µm thick GaN layer, followed by a ohmic contact at the top, representing the drain contact and a Schottky contact at the bottom, reproducing the Si/GaN interface. Length of the sample was 10µm and width was set to 1mm. A shallow donor concentration of 10^{14} cm^{-3} was added to the GaN buffer and properties of deep donors and acceptors were chosen according to published results [65-67]. The details are given in the description of the simulation setups.

4.7.2 Bulk Current Modeling in GaN-on-Si HEMTs

The drain to substrate current is simulated for different Schottky barrier height, shown in Fig. 4.35. At high barrier height, current is lower due to higher potential seen by the electrons. When barrier height is lower, electrons move easily into GaN and current is increased. At low voltages, $V_{DB} < 5V$, a lot of electrons are trapped near the interface resulting significant space charge near the equivalent Schottky barrier. These space charges reduce the effective barrier height. Higher the applied bias, higher the space charge, greater the barrier lowering.

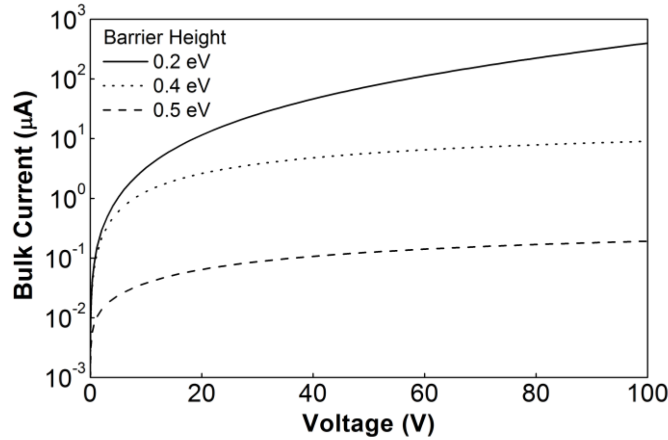

Figure 4.35 Schottky - bulk current at different equivalent barrier heights in the presence of deep traps. The GaN buffer thickness is 5 μm; buffer doping $N_D = 10^{14}$ cm^{-3}

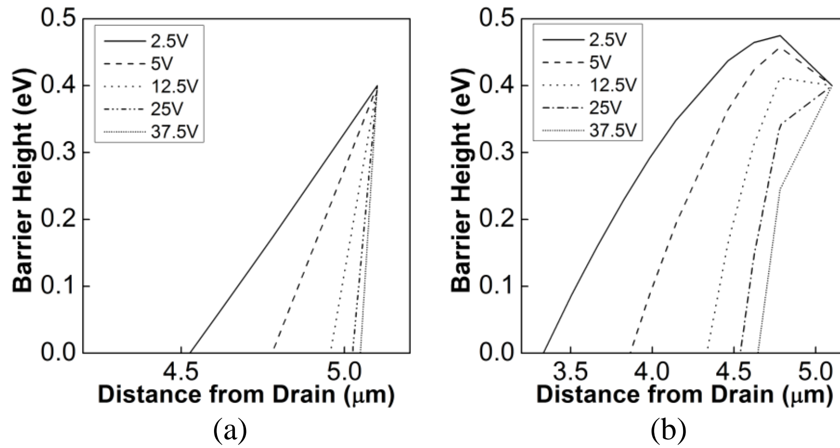

Figure 4.36 Barrier profiles in the presence of traps at different applied bias; (a) lower acceptor trap concentration, $N_T = 10^{14}$ cm^{-3}, (b) higher acceptor trap concentration $N_T = 10^{16}$ cm^{-3}

In Fig. 4.36, barrier height modulation due to space charge is shown for different applied biases. When trap concentration is low, space charge concentration at the interface is lower, so we don't see any barrier height modulation for low trap condition as shown in Fi. 4.36 (a). As trap concentration is increased which causes more electron trapping near the equivalent Schottky barrier, the fermi level is pulled down to the trap level. As a result, overall barrier height increases and current decreases. As we increase reverse bias

voltage, the field associated with the space charges is compensated by the external electric field. Due to this, the effective barrier height decreases as we increase reverse bias. This is shown in Fig 4.36 (b).

At low voltages, the slope of the bulk current I-V is relatively sharp because of the barrier lowering. When V_{DB} is higher, typically above 5V, the external field is significantly higher than the field associated with the space charge near the interface. Consequently, the barrier height is almost constant for higher voltages. The space charge due to electron trapping in the bulk GaN mostly controls the electric field and bulk current.

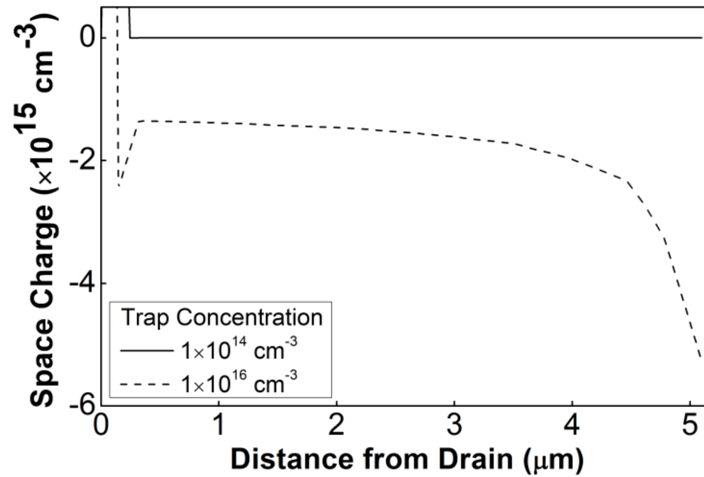

Figure 4.37 Space charge profile at 600V for acceptor concentration $N_T = 10^{14}$ cm^{-3} and 10^{16} cm^{-3}, barrier height is 0.4eV and bulk doping $N_D = 10^{14}$ cm^{-3}

The space charge concentration for two different trap concentration at 600V is shown in Fig. 4.37. As seen, significant space charge exists in the bulk when trap concentration is 10^{16} cm^{-3}. Clearly, the source of this space charge is the electrons captured by the traps. The space charge concentration varies between 1×10^{15} cm^{-3} and 5×10^{15} cm^{-3}, which is considerably higher than equilibrium carrier concentration. In real epitaxial GaN, trap

concentration is much higher than the shallow donor concentration of 10^{14} cm^{-3} used in this study. When trap concentration is low, space charge concentration is also low even at very high bias due to less number of electron trapping. The slope of the bulk I-V depends on the amount of space charge and electric field non-uniformity associated by the space charge. For low trap concentration (10^{14} cm^{-3}), the bulk current shows quazi-ohmic behavior because in this case, the electric field and mobile carrier density throughout the bulk is nearly uniform.

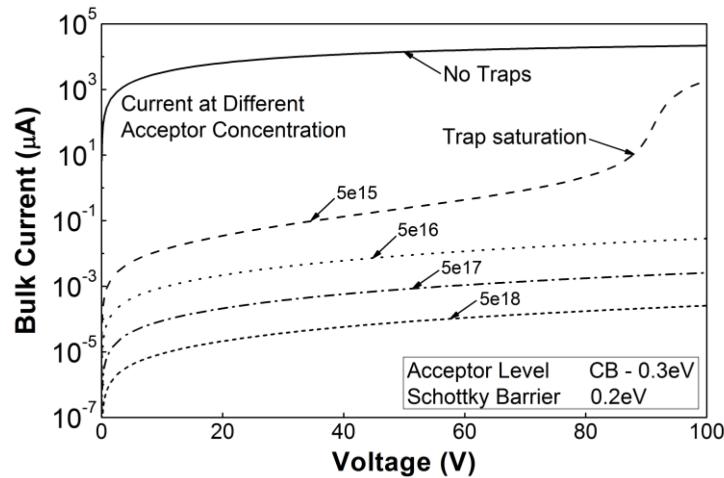

Figure 4.38 Simulated bulk currents at different acceptor trap concentrations. Schottky barrier height is 0.2eV, acceptor and donor concentrations are 3.5×10^{16} cm^{-3} and 5×10^{17} cm^{-3} respectively

In Fig. 4.38, we compare bulk current with different acceptor concentrations with bulk current in the absence of traps. As expected, when there are no traps in the bulk, current is very high. As we add acceptor traps in the bulk, current decreases with increasing trap concentration. At relatively lower acceptor concentration, there may be a condition where all the traps are occupied at some bias. When this happens, current increases rapidly as in the case of acceptor concentration of 5×10^{15} cm^{-3} shown in the Fig. 4.38.

4.7.3 Compact Model for Bulk Current

We have developed a simple but accurate compact model for GaN HEMTs on Si substrates using parameters that can be extracted directly from the experimentally observed bulk current I-Vs [57]. The assumption was made on the fact that many material parameters are either unknown or very difficult to obtain such as those related to the trap characteristics.

$$\mathrm{I_{db}} = \mathrm{I_s} * \left[1 - \exp\left(-\frac{\mathrm{V_{db}}}{\mathrm{nblk} * \frac{\mathrm{kT}}{\mathrm{q}}}\right)\right] * \exp(2.3 * \mathrm{y})\,;$$

$$\text{where } y = \frac{y1}{\left[1+\left(\frac{y1}{y2}\right)^{m}\right]^{\frac{1}{m}}};\quad y1 = s1 * \mathrm{V_{db}};\quad y2 = ykn + s2 * \mathrm{V_{db}}\,;$$

Table 4.2 Bulk current compact model parameters and fitting values

Parameters		Fig. 5.17	Fig. 5.18
I_s	Saturation current parameter of the equivalent Si/GaN barrier	1e-7	1e-7
nblk	Ideality factor of the equivalent Si/GaN barrier	30	30
s1	Low-voltage slope of the semilog I-V ($\log_{10}$(A)/V)	1.1	0.05
s2	High-voltage slope of the semilog I-V ($\log_{10}$(A)/V)	0.011	0.001
y	Low to high voltage region smoothing function		
ykn	Knee current corresponding to the low-to-high voltage region transition	2	1.25
m	Smoothing parameter	1.25	1.25

Compared to a previous compact model developed by Pérez-Tomás, et al. [58], our model is advantageous in that there is more flexibility in fitting the experimental I-Vs and the parameters can be directly extracted from semi-logarithmic I-V characteristics.

CHAPTER 5

MODEL VALIDATION

5.1 Introduction

Model validation is an integral part of any model development. Without proper validation, a model has no significance to the modeling engineers and designers. In this chapter, model validation has been done by comparing the simulated data with various experimental data obtained from published research papers as well as devices provided by our industrial partners. We have shown model validation against a variety of experimental data with different characteristics. In most cases, simulated data showed very good agreement with the experimental data indicating the model is fairly accurate.

5.2 Experimental I-V Fitting at Room Temperature

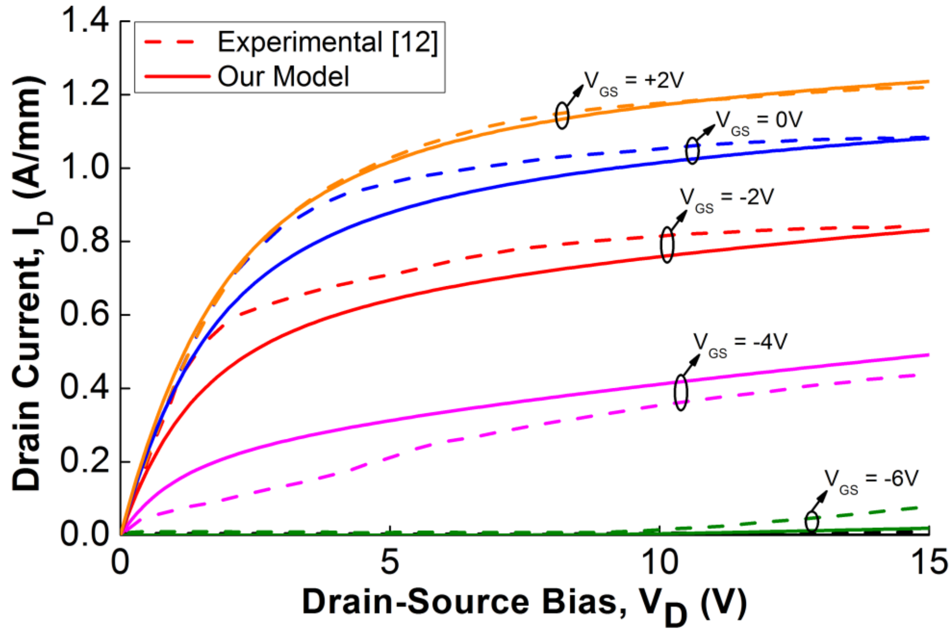

Figure 5.1 Fitting of an experimenal I_D-V_D characteristics of an AlGaN/GaN HEMT with gate length 0.12µm and gate width 100µm [12]

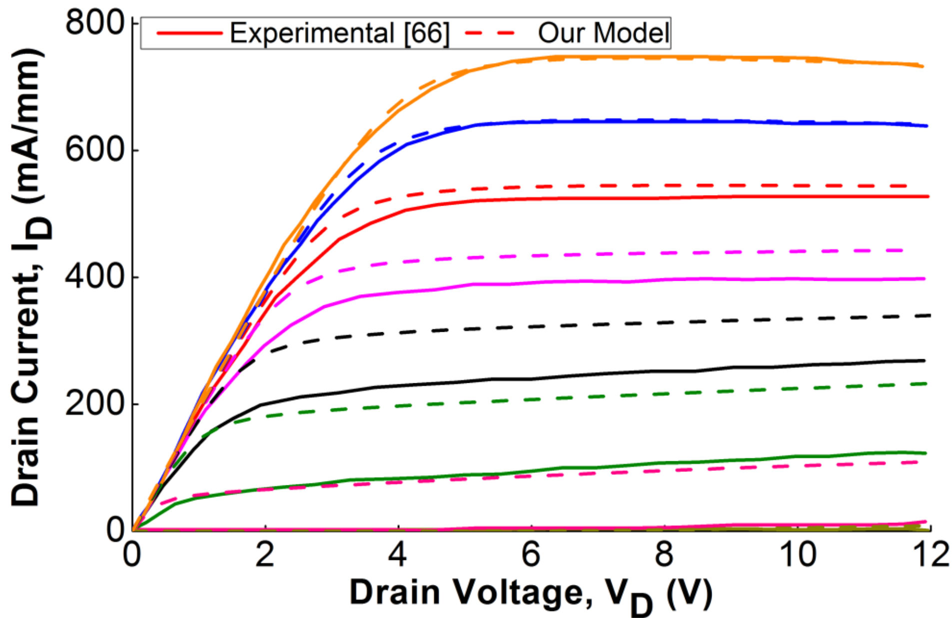

Figure 5.2 Experimenal drain current I-V fitting of an AlGaN/GaN HEMT with gate length 120nm and gate width 50µm at 25ºC. Gate bias was varied from +1V to -6V with a decrement of 1V [68]

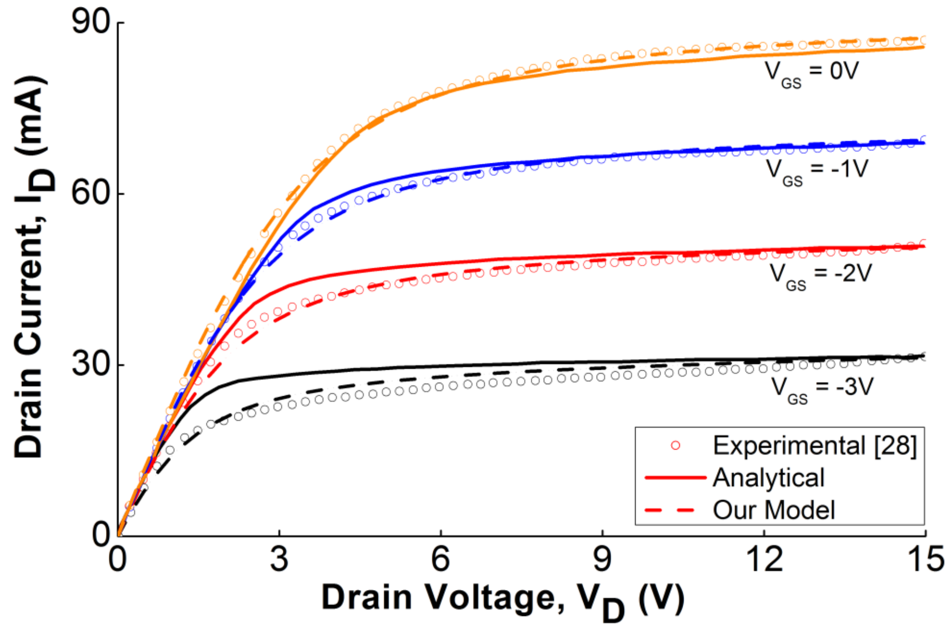

Figure 5.3 Experimenal I-V fitting of an AlGaN/GaN HEMT with gate length 0.2µm and gate width 100µm at 300K [28]

5.3 High Temperature I-V Fitting

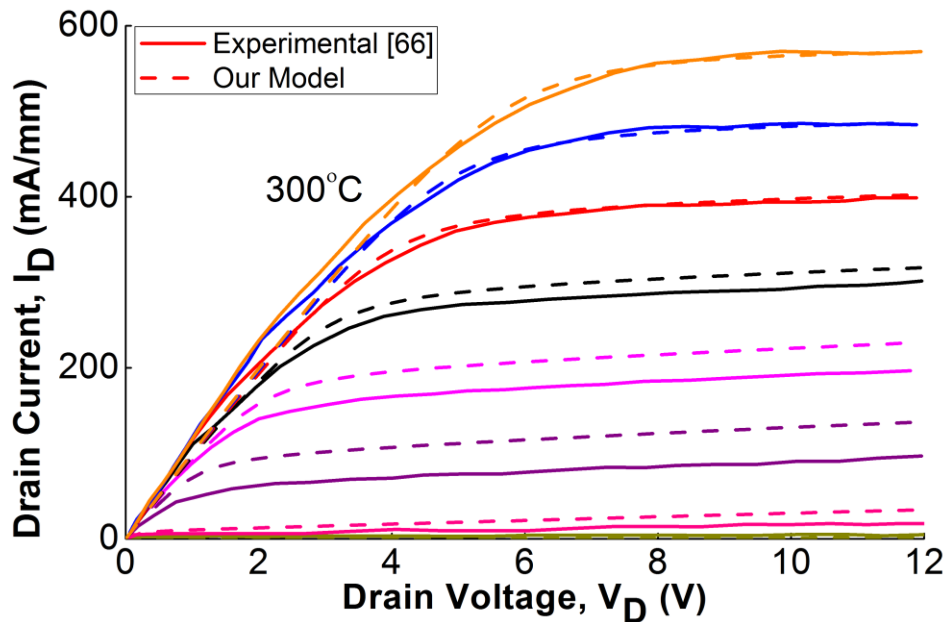

Figure 5.4 Experimenal drain current I-V fitting of an AlGaN/GaN HEMT with gate length 120nm and gate width 50µm at 300ºC. Gate bias was varied from +1V to -6V with a decrement of 1V [68]

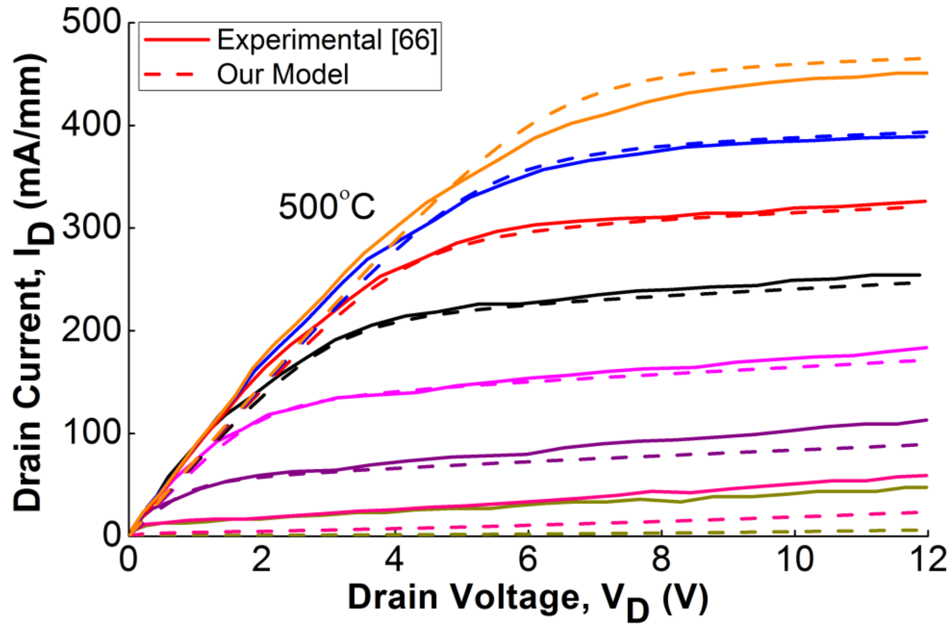

Figure 5.5 Experimenal drain current I-V fitting of an AlGaN/GaN HEMT with gate length 120nm and gate width 50µm at 500ºC. Gate bias was varied from +1V to -6V with a decrement of 1V [68]

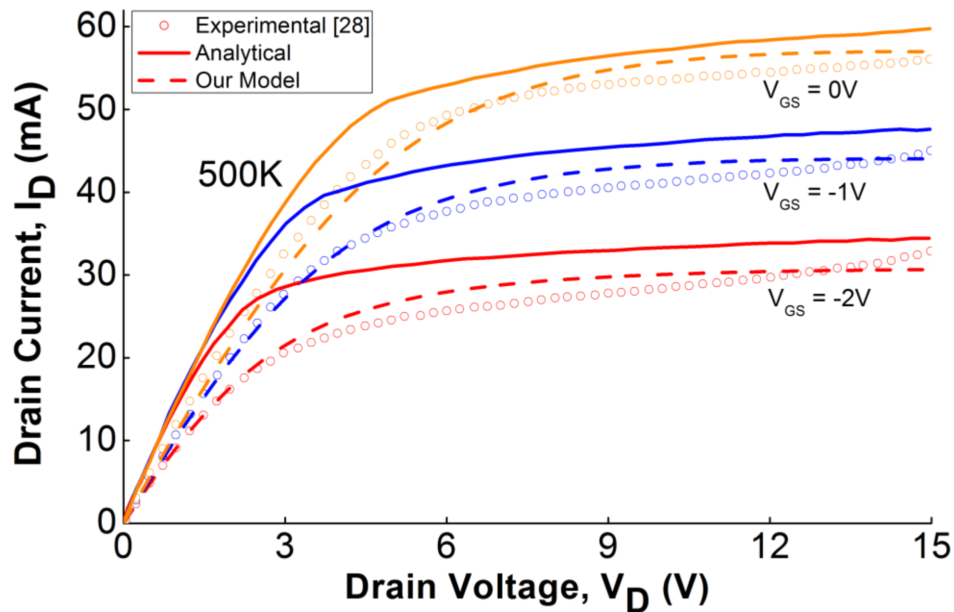

Figure 5.6 Experimenal I-V fitting of an AlGaN/GaN HEMT with gate length 0.2µm and gate width 100µm at 500K [28]

5.4 Fitting of I-V with Self-Heating Effect

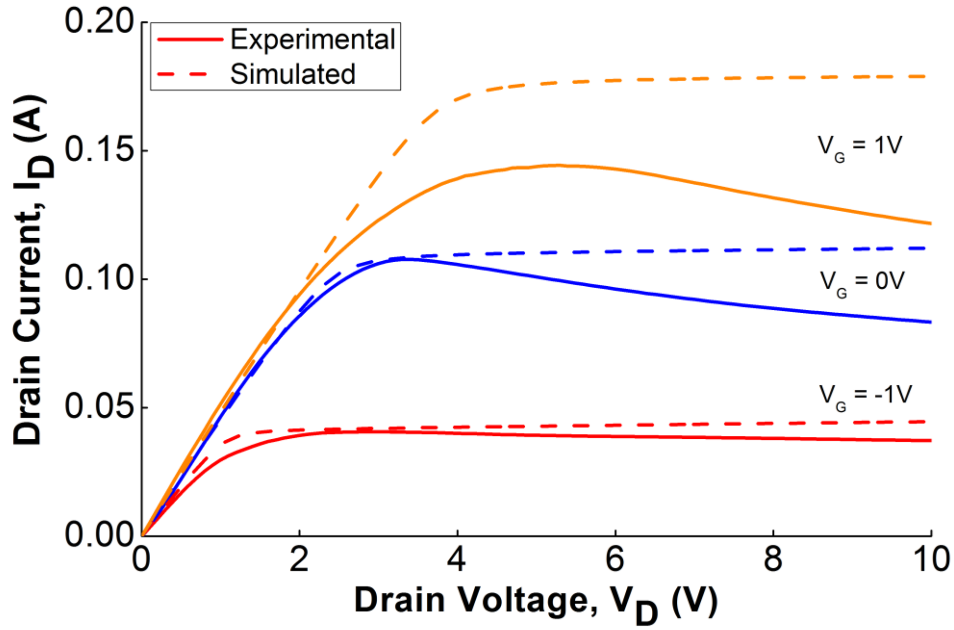

Figure 5.7 Simulated drain current I-V without self-heating effect for an AlGaN/GaN HFET with gate length, L_G = 1µm; source to drain spacing, $L_{SD} \approx$ 10µm and gate width, W = 200µm obtained from our industrial partners

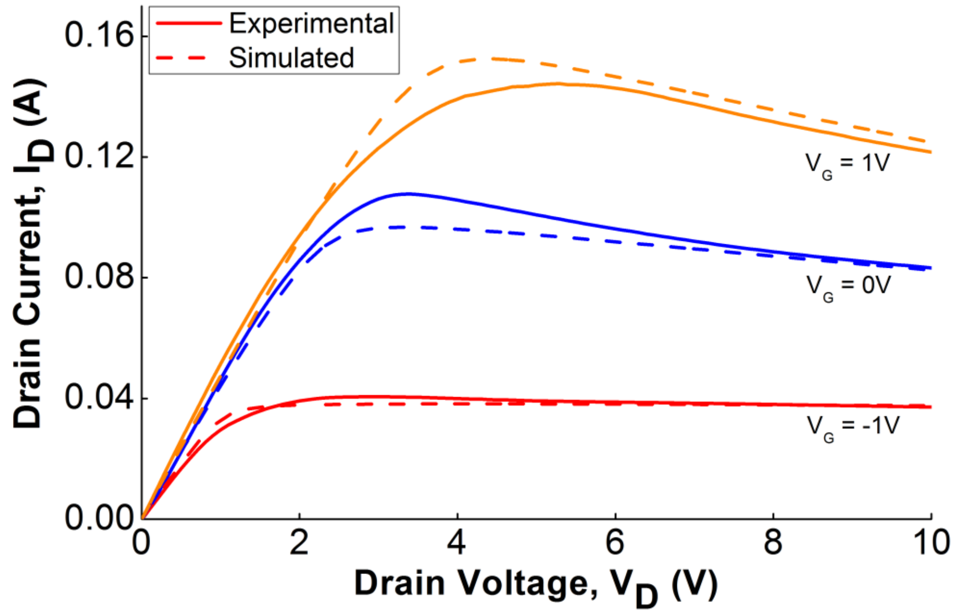

Figure 5.8 Same experimental I-V fitting shown in Fig. 5.7 after adding self-heating effect

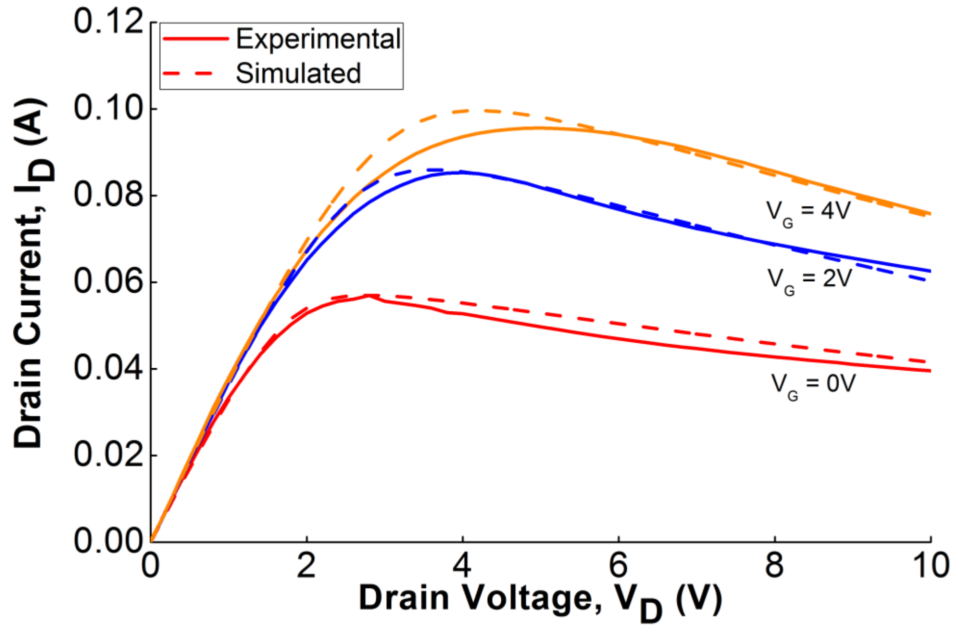

Figure 5.9 Simulated drain current I-V with self-heating effect for an AlGaN/GaN HFET with gate length, L_G = 1µm; source to drain spacing, L_{SD} ≈ 5µm and gate width, W = 100µm obtained from our industrial partners

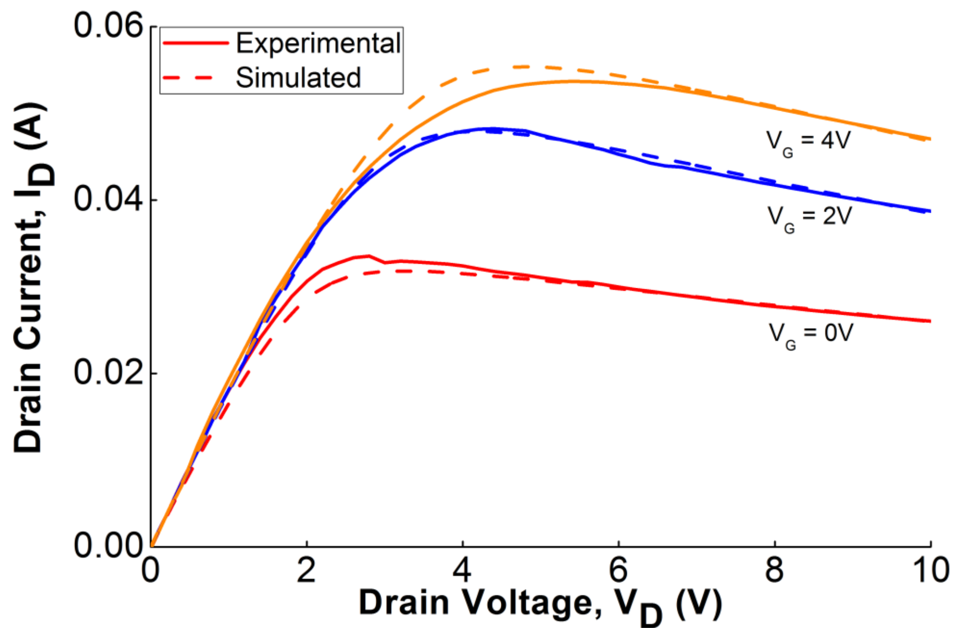

Figure 5.10 Simulated drain current versus experimental drain current for an AlGaN/GaN HFET with gate length, L_G = 1µm; source to drain spacing, L_{SD} ≈ 5µm and gate width, W = 50µm obtained from our industrial partners

5.5 Subthreshold Current Fitting

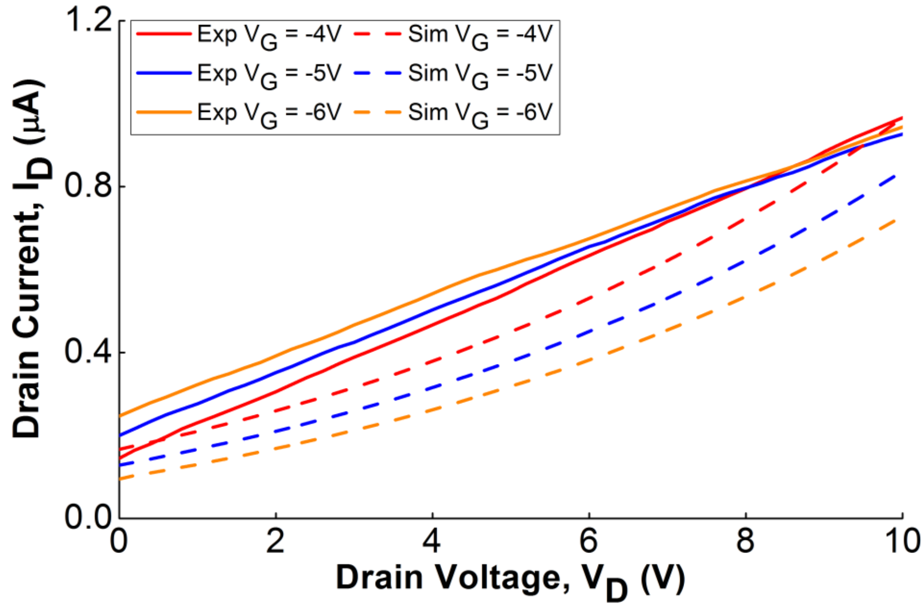

Figure 5.11 Simulated subthreshold current versus experimental subthreshold current for an AlGaN/GaN HFET with gate length, L_G = 1μm; source to drain spacing, L_{SD} ≈ 5μm and gate width, W = 100μm obtained from our industrial partners

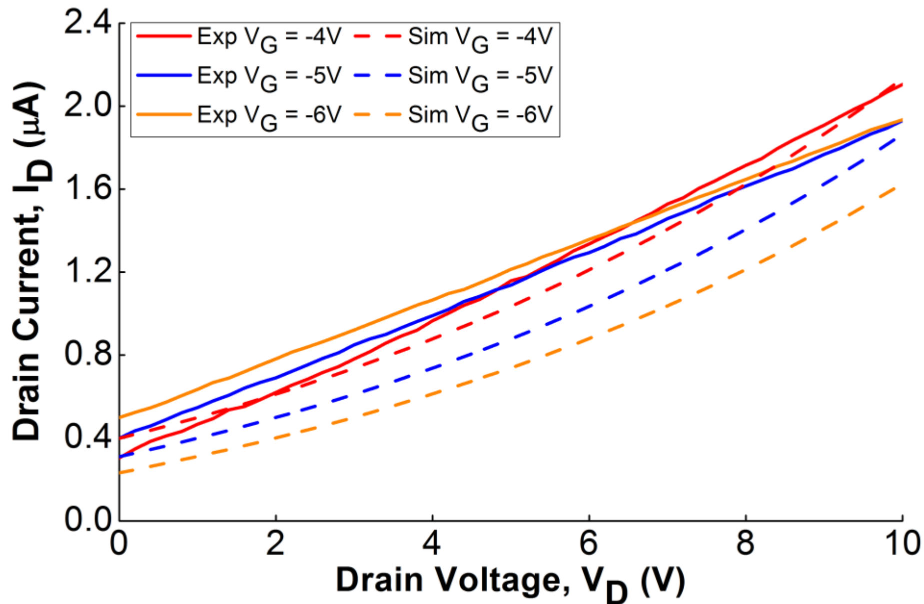

Figure 5.12 Simulated subthreshold current versus experimental subthreshold current for an AlGaN/GaN HFET on sapphire substrate with gate length, L_G = 1μm; source to drain spacing, L_{SD} ≈ 5μm and gate width, W = 50μm obtained from our industrial partners

5.6 Current Collapse Fitting

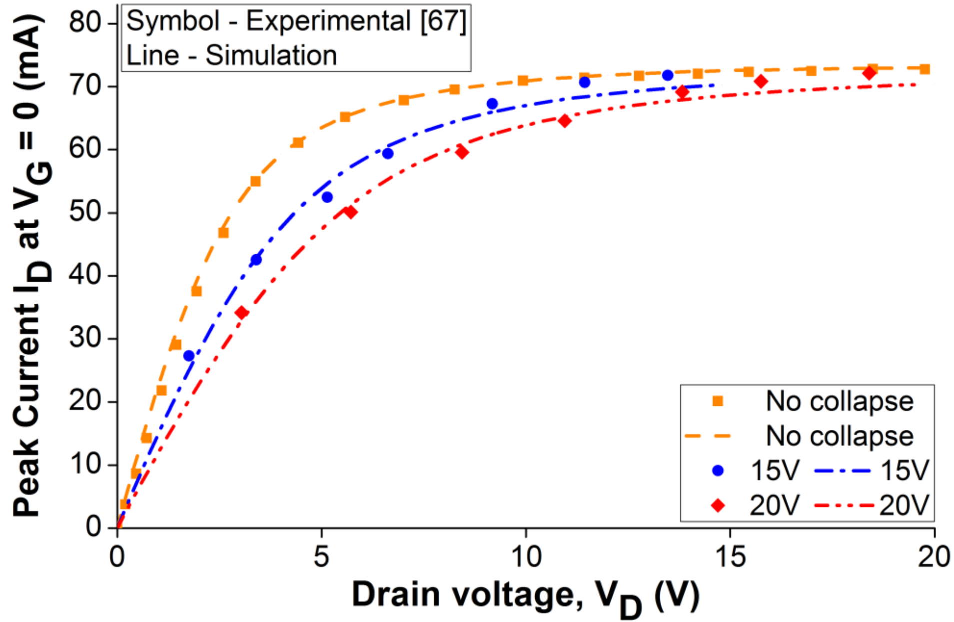

Figure 5.13 Experimental dynamic I-V fitting with current collapse of an HFET device with a gate length of 1.3µm and gate width of 100µm [69]

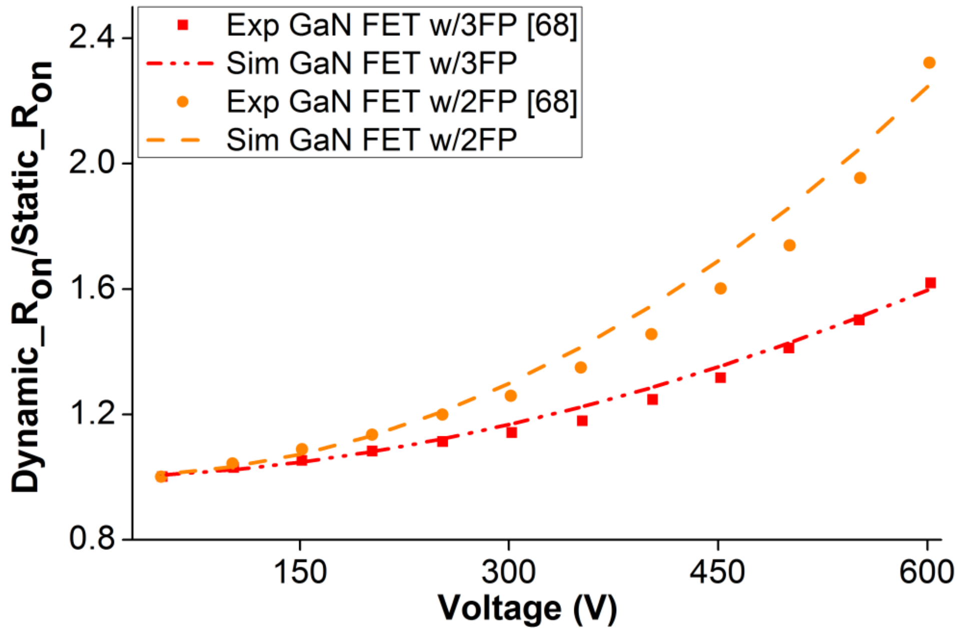

Figure 5.14 Fitting of the ratio between dynamic on-resistance and static on-resistance of different HFET devices [70]

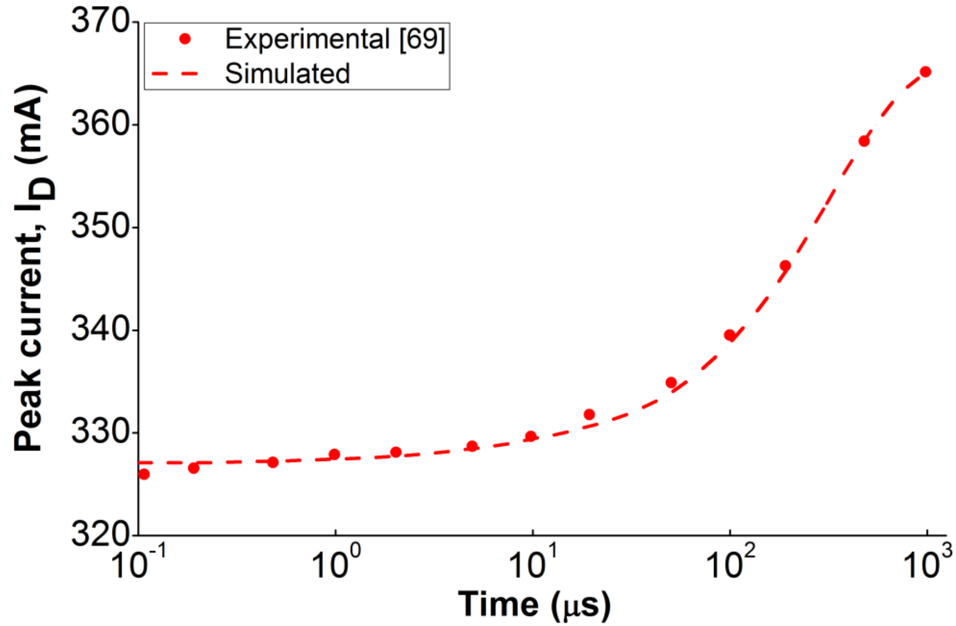

Figure 5.15 Current recovery after removing the applied drain and gate bias of 35V and -5V respectively, from 1μs to 1ms for an HFET device with gate length L_G = 0.25μm [71]

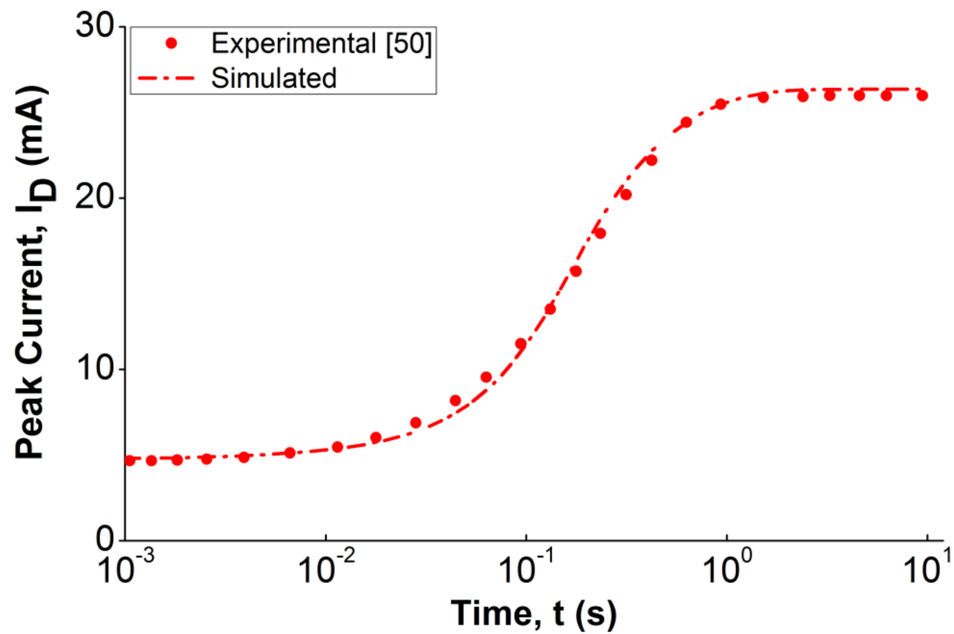

Figure 5.16 Current recovery after removing the stressed condition, drain bias of 25V and gate bias of -12V, from 1ms to 10s for an HFET device [50]

5.7 Bulk Current I-V Fitting

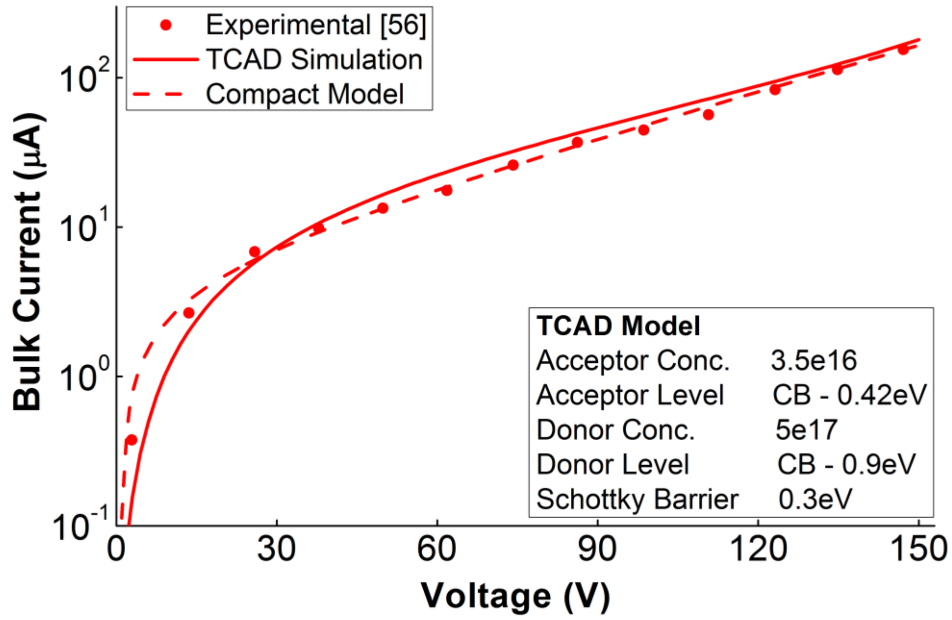

Figure 5.17 Experimental bulk current I-V fitting of an AlGaN/GaN HEMT on Si [58]

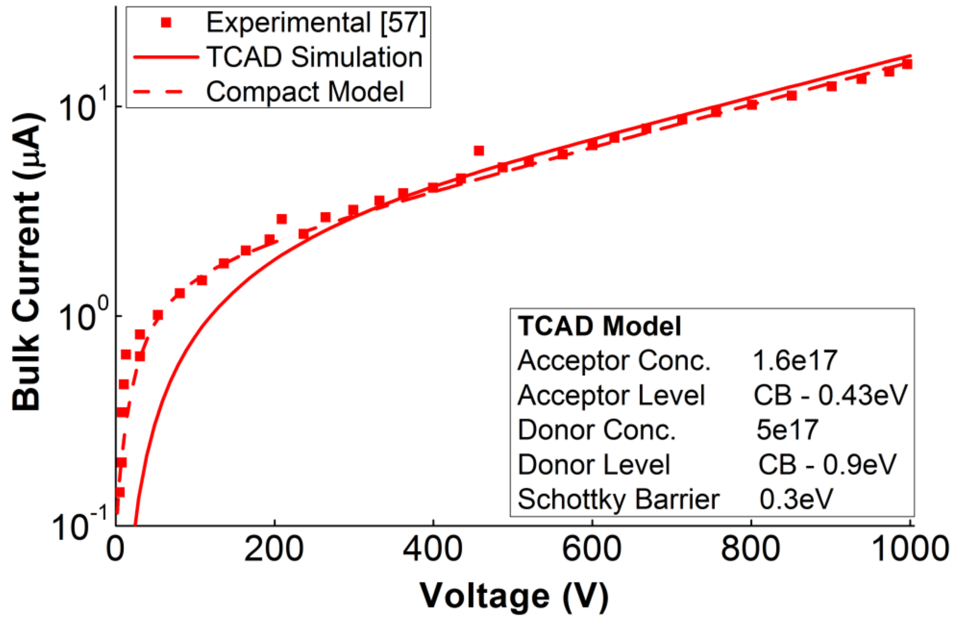

Figure 5.18 Fitting of the experimental bulk current I-V [59] using the developed TCAD and compact model

CHAPTER 6

SUMMARY AND FUTURE WORK

6.1 Summary

In this work, a novel GaN HFET compact model for power switching applications suitable for device/circuit simulators has been developed. The model accounts for all the key characteristics of GaN HFET in power switching mode: the drain current, gate current, non-linear capacitances, current collapse, temperature dependencies as well as steady-state and non-stationary self-heating effects. We have introduced a new continuous smoothing function for the drain current and other device characteristics, which enables fast and consistently converging circuit simulations. The key innovations implemented in the developed model are as follows.

1. For the first time, we have developed a compact model that describes all the characteristics of power HEMT switches
2. Field plate effects have been added based on the voltage dependent charge model.
3. Compact model for current collapse, one of the important aspect of power switching and non-existent in available GaN HFET models has been developed.
4. Bulk current which is crucially important for power switching applications has been investigated using TCAD simulation and based on the results of a novel simulation approach, a compact model has been devised.

The simulated data has been compared against various experimental data obtained from published journals and different vendors. The experimental curve fitting proves the validity of our model for a wide range of device parameters. Simulated pulse responses validate the applicability of the model in power switching applications.

6.2 Future Work

The model includes many important aspects of power switching application but there are many areas where the model can be improved. Currently, neither the current collapse nor the bulk current models have temperature dependency incorporated. Previous experimental studies showed that current collapse is temperature dependent [72]. It is very important to model the temperature dependent behavior of current collapse as it severely affects the transient behavior of HFET devices. Bulk current also has strong temperature dependency [58], at elevated temperature the current can be very high leading to substantial power loss in the off state and premature breakdown. Therefore, adding temperature dependency of current collapse and bulk current would be an important future work for this model.

The model has fairly large number of parameters. Decreasing the fitting parameters by developing simple but accurate relations can increase the convergence which will make the model faster and easier to implement. The semi-empirical model has some modules that are not physics-based. Developing physics based model will provide better understanding and more accurate results.

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APPENDIX A

MODEL PARAMETERS

Data Type	Parameter	Description	Default Value
real	Vth0	Threshold voltage [V]	-4
real	rd	Drain resistance [Ohm]	5
real	rs	Source resistance [Ohm]	1
real	Rb0	Butter resistance [Ohm]	1e6
real	LG	Gate length [µm]	1
real	Wtot	Total device width [µm]	1000
real	Vkt0	Thermal voltage [V]	26e-3
real	mu0	Low field mobility of channel electrons [m^2/Vs]	0.12
real	vs0	Saturation velocity [m/s]	2e5
real	mu2	Low-field mobility of 2nd channel electrons [m^2/Vs]	0.002
real	delta_ids	Drain current saturation smoothing parameter	0.2
real	d_vgt	Vgt to Vkt transition coefficient	3
real	ns_max	Maximum sheet carrier concentration [m^{-2}]	1e17
real	delta_ns	ns-ns_max transition smoothing parameter	0.03
real	eta	Subthreshold ideality factor	2
real	alp	Buffer resistance ideality factor	1
real	zeta	Temperature sensitivity of reverse diode conductance	0.002
real	Kmu	Temperature coefficient of mobility	5e-4
real	Kvt	Temperature coefficient of threshold voltage	1e-3
real	Kvs	Temperature coefficient of saturation velocity	90
real	m1	Ideality factor for mobility	1.5
real	Rth	Thermal resistance [Ohm]	5
real	Cth	Thermal capacitance [F]	2e-7
integer	sh	Self-heating mode selector	-1
real	sigma0	DIBL parameter	0.05
real	Vsigma	DIBL Vgt offset	1
real	dVSigma	Width of DIBL transition	1
real	Rcc1	RC circuit resistance for calculating Rdt [Ohm]	150
real	tau	Time constant of the RC circuit for calculating Rdt and Rst [s]	0.01
real	Rcc2	RC circuit resistance for calculating Rst [Ohm]	100
real	b_D	Fitting coefficient for calculating R_{DCC}	5

real	b_S	Fitting coefficient for calculating R_{SCC}	1
real	m_D	Fitting parameter for calculating R_{DCC}	1
real	m_S	Fitting parameter for calculating R_{DCC}	1
real	Vdsmax	Maximum Vds for instantaneous current collapse [V]	50
real	Vgsmax	Maximum Vgs for instantaneous current collapse [V]	-6
integer	cc	Parameter for selecting current collapse modes	0
real	C_bar1	Maximum gate to channel capacitance [F/m^2]	5e-3
real	C_bar2	Minimum gate to channel capacitance [F/m2]	1e-3
real	C_GFP1	Maximum gate FP to channel capacitance [F/m^2]	5e-4
real	C_GFP2	Minimum gate FP to channel capacitance [F/m^2]	1e-4
real	C_SFP1	Maximum source FP to channel capacitance [F/m^2]	9e-4
real	C_SFP2	Minimum source FP to channel capacitance [F/m^2]	5e-4
real	CSGFP	Capacitance between source & gate FP [F/m^2]	1.3e-4
real	CSGMP	Capacitance between source FP& gate metal [F/m^2]	1.2e4
real	C_RES1	Gate residual capacitance without SFP & GFP effect [F/m^2]	1.5e-4
real	C_RES2	Gate residual capacitance with GFP effect [F/m^2]	5e-6
real	C_RES3	Gate residual capacitance with GFP & SFP effect [F/m^2]	1e-6
real	CGFP_RES1	Gate FP residual capacitance without SFP & GFP effect [F/m^2]	1.5e-5
real	CGFP_RES2	Gate FP residual capacitance with GFP effect [F/m^2]	5e-6
real	CGFP_RES3	Gate FP residual capacitance with GFP & SFP effect [F/m^2]	1e-6
real	VINFL	Inflection point w.r.t Vgs in input capacitance	-2.65
real	DELTGS	Parameter characterizing the shape of the input capacitance	1.95
real	LABMDA	Parameter that adds Vds dependence of the input capacitance	5.7e-4
real	VDSO	Drain voltage where Vds dependency disappears from equations	5
real	C12SAT	Gate-channel saturation input transcapacitance [F/m^2]	2.9e-4
real	C12SATGFP	Gate FP-channel saturation input transcapacitance [F/m^2]	2.9e-5
real	C12SATSFP	Source FP-channel saturation input transcapacitance [F/m^2]	2.9e-6
real	m2	Ideality factor for gate to gate FP capacitance transition	20
real	m3	Ideality factor for gate FP to source FP capacitance transition	15
real	Ar	Effective Richardson’s constant [A/m^2/K^2]	0.0012

real	Phi	Effective heterojunction barrier height [eV]	0.3
real	n	Gate current ideality factor	10
real	delta_g	Reverse junction conductance inverse ideality factor	1e-4
real	g_gr0	Reverse diode conductance	10
real	LGFP	Length of gate FP [µm]	0.5
real	LSFP	Length of source FP [µm]	5
real	dbuf	Thickness of buffer layer [µm]	5
real	Ld	Length of drain electrode [µm]	10
real	s1	Low-voltage slope of the semilog bulk current I-V	0.1
real	s2	High-voltage slope of the semilog bulk current I-V	0.008
real	ks1	Temperature coefficient of s1	8e-4
real	ks2	Temperature coefficient of s2	1.5e-5
real	m4	Ideality factor for low to high voltage region smoothing function	3
real	Ikn	Knee current for bulk current model [A/mm]	7e-11
real	Is0	Reverse current of the bulk Schottky contact [A/mm]	1e-12
real	kIn	Temperature coefficient of Ikn	0.05
real	kIs	Temperature coefficient of Is0	0.05
real	nblk	Effective barrier ideality factor	30