6-30-2016

Finite Control Set Model Predictive Control Of Direct Matrix Converter And Dual-Output Power Converters

Ozan Gulbudak
University of South Carolina

FINITE CONTROL SET MODEL PREDICTIVE CONTROL OF DIRECT MATRIX CONVERTER AND DUAL-OUTPUT POWER CONVERTERS

By

Ozan Gulbudak

Bachelor of Science
Mersin University, 2008

Master of Science
Mersin University, 2010

Submitted in Partial Fulfillment of the Requirements

For the Degree of Doctor of Philosophy in

Electrical Engineering

College of Engineering and Computing

University of South Carolina

2016

Accepted by:

Enrico Santi, Major Professor

Herbert Ginn, Committee Member

Bin Zhang, Committee Member

Joshua Tarbutton, Committee Member

Lacy Ford, Senior Vice Provost and Dean of Graduate Studies

ACKNOWLEDGEMENTS

The first person that I show my gratitude is Dr. Enrico Santi for his extensive support, guidance throughout my doctoral study here in USC. He has taught me much about research in power electronics and offered me such exciting research topic. It was priceless opportunity to work with Dr. Santi and in one of the most leading research group.

I would also like to express my gratitude to my committee members, Dr. Ginn, Dr. Zhang and Dr. Tarbutton for their feedback and helping me to improve my dissertation.

I am particularly indebted to Janosch Marquart from University of Applied Science NTB, Switzerland for helping to build several hardware platforms and it was great chance to work with him. I would also like to thank my colleagues, past and present, in Power Energy Group: Dr. Isaac Nam, Dr. Kang Peng, Dr. Hossein A. Mohammadpour, Dr. Alexander Grekov, Jonathan Siegers, Silvia Arrua, Soheila Eskandari, Vinya Sri Penchala, Hessamaldin Abdollahi, Hossein Baninajar.

ABSTRACT

Model Predictive Control (MPC) with a finite control set has been successfully applied to several power converter topologies as reported in the scientific literature and research activity on predictive control techniques has increased over the last few years. MPC uses a discrete-time model of the system to predict future values of control variables for all possible control actions and computes a cost function related to control objectives to find the optimal control action. The control action which minimizes the cost function is selected and applied to the system for the next time interval. Different control objectives can be introduced in the user-defined cost function and controlled simultaneously by solving the multi-objective optimization problem. This approach is particularly advantageous for certain power converter topologies, such as Direct Matrix Converter (DMC) and dual-output power converters, for which conventional control techniques require complicated Pulse Width Modulation (PWM) schemes and multi-loop control, incurring high computational burden and complexity. Conversely, since MPC does not need a modulator to generate switching signals, implementation of the MPC technique is simple and intuitive. However, the MPC method also has several drawbacks:

1. Real-time implementation of MPC incurs high computational burden
2. There is no analytical procedure to adjust the weighting factors for multi-objective optimization problem

3. A complete system model must be derived since MPC method uses this model to predict control variables
4. MPC implementation is not straightforward for several power converter topologies, such as dual-output power converters.

In this dissertation four specific contributions are reported that address these drawbacks.

First, a fully FPGA-based real-time implementation of model predictive controller is proposed for direct matrix converter. In conventional real-time implementation of model predictive control method, Digital Signal Processors (DSPs) and Field-Programmable Gate Arrays (FPGA) are both used to ensure fast processing operation and preserve performance of the predictive controller. For the proposed, real-time implementation method, all control calculations and the safe commutation scheme for DMC are fully implemented in the FPGA and the need for a DSP is eliminated. Advantages of the proposed approach are simplicity and the ability to exploit the parallel computation capability of the FPGA to calculate in parallel the predictive state for all switch combination. This translates in a significant reduction of required computation time and potentially in reduced control hardware cost.

Second, a novel model predictive control scheme for the three-phase direct matrix converter based on switching state elimination is proposed. The conventional MPC solves a multi-objective optimization problem by minimizing a multi-objective cost function over a one-step horizon. The control performance is strongly affected by the weighting factors used in the cost function and this is problematic. The proposed method solves this difficulty by eliminating the weighting factors and using a state elimination method based on error constraints that have a clear physical interpretation.

Third, the model predictive control scheme is proposed for Nine-Switch Inverter (NSI) under an unknown load condition. Nine-switch inverter is a dual-output inverter and the proposed method can control two three-phase load simultaneously by solving single optimization problem. In power electronics applications, control of the power converter must work well under all load conditions and the control method should provide clean power no matter what the load is. In this work, two ac load currents are estimated using full-order observers and converter is controlled by using model predictive control method.

Fourth, the model predictive control scheme is proposed for dual-output Indirect Matrix Converter (IMC). Modulation method for this topology is complicated and conventional linear control techniques require tuning of the controller parameters. In conventional control technique, multi-loop control is required to independently adjust the two ac outputs. The usage of multi-loop control techniques increases the complexity of implementation of the controller. On the other hand, proposed method can achieve several control goals by using single control loop and provide good system performance.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS....iii

ABSTRACT.... iv

LIST OF TABLES ix

LIST OF FIGURES.... x

LIST OF SYMBOLS....xvi

CHAPTER 1 INTRODUCTION 1
1.1 FINITE CONTROL SET MODEL PREDICTIVE CONTROL....1
1.2 DIRECT MATRIX CONVERTER 4
1.3 DUAL OUTPUT NINE-SWITCH INVERTER....6
1.4 DUAL-OUTPUT INDIRECT MATRIX CONVERTER 8
1.5 RESEARCH OBJECTIVES 9
CHAPTER 2 FPGA-BASED MODEL PREDICTIVE CONTROLLER FOR DIRECT MATRIX CONVERTER....12
2.1 DIRECT MATRIX CONVERTER MODEL 12
2.2 MODEL PREDICTIVE CONTROL FOR DIRECT MATRIX CONVERTER 14
2.3 ISSUES WITH CONVENTIONAL REAL-TIME IMPLEMENTATION 20
2.4 PROPOSED REAL-TIME IMPLEMENTATION METHOD 21
2.5 HARDWARE PLATFORMS AND EXPERIMENTAL RESULTS 25
2.6 DISCUSSION AND CONCLUSION....37
CHAPTER 3 MODEL PREDICTIVE CONTROL BASED ON SWITCHING STATE ELIMINATION....41
3.1 CONVENTIONAL MODEL PREDICTIVE CONTROL 42
3.2 SWITCHING STATE ELIMINATION TECHNIQUE 44
3.3 SIMULATION RESULTS 51
3.4 EXPERIMENTAL RESULTS....56
3.5 CONCLUSION....62

CHAPTER 4 MODEL PREDICTIVE CONTROL FOR NINE-SWITCH INVERTER..64
4.1 CONVENTIONAL CONTROL TECHNIQUE FOR NINE-SWITCH INVERTER.....65
4.2 SYSTEM MODEL.....66
4.3 MODEL PREDICTIVE CONTROL SCHEME.....74
4.4 SIMULATION RESULTS.....78
4.5 SUMMARY.....90
CHAPTER 5 MODEL PREDICTIVE CONTROL FOR DUAL-OUTPUT INDIRECT MATRIX CONVERTER.....92
5.1 INTRODUCTION.....92
5.2 SYSTEM MODEL.....93
5.3 MODEL PREDICTIVE CONTROL SCHEME.....95
5.4 SIMULATION RESULTS.....97
5.5 SUMMARY.....105
CHAPTER 6 CONCLUSIONS AND FUTURE WORK.....106
6.1 CONCLUSIONS.....106
6.2 FUTURE WORK.....108
REFERENCES.....109

LIST OF TABLES

Table 1.1 Switches positions of Legs 8

Table 2.1 Switches positions of Legs 36

Table 2.2 FPGA resources and execution time vs number of control objectives 37

Table 2.3 Digital control platforms comparison 39

Table 2.4 Execution time for calculation tasks 40

Table 3.1 Sub-finite solution set selection 47

Table 3.2 Simulation parameters for first case 51

Table 4.1 Simulation Parameters 78

Table 5.1 Simulation Parameters 98

LIST OF FIGURES

Figure 1.1 Working principle of model predictive control. 3

Figure 1.2 General predictive control scheme for power converters. 4

Figure 1.3 Direct matrix converter topology 5

Figure 1.4 Switching combinations for direct matrix converter 6

Figure 1.5 Nine-switch inverter topology 7

Figure 1.6 Dual-Output Indirect Matrix Converter Topology 9

Figure 2.1 Model predictive control scheme for direct matrix converter 19

Figure 2.2 Conventional real-time implementation for direct matrix converter 21

Figure 2.3 Comparison between conventional method and proposed method 22

Figure 2.4 Parallel implementation of model predictive control. 23

Figure 2.5 Finite state machine for current cost calculation. 23

Figure 2.6 FPGA architecture for predictive controller. 24

Figure 2.7 Time-Area optimization. 25

Figure 2.8 Two-phase input single-phase output topology. 26

Figure 2.9 Two-phase input single-phase output prototype. 27

Figure 2.10 Output load current measurement circuit 28

Figure 2.11 Load current direction sensing wavefom a)Load current direction detection b) Rising edge c) Falling edge. 29

Figure 2.12 Four-step commutation a) Positive load current b) Negative load current. 30

Figure 2.13 RTL for reference generation. 31

Figure 2.14 Reference generation using ROM block. 31

Figure 2.15 Direct matrix converter prototype. 32

Figure 2.16 Experimental results in case of 60 Hz reference a) Experimental waveforms without reactive power control b) Experimental waveforms with reactive power control. 33

Figure 2.17 Experimental results in case of 30 Hz reference a)Experimental waveforms b) Load current frequency spectrum c) Source current frequency spectrum. 34

Figure 2.18 Experimental results in case of 120 Hz reference a) Experimental waveforms b) Load current frequency spectrum c) Source current frequency spectrum. 35

Figure 2.19 Dynamic response of FPGA-based model predictive controller. 36

Figure 2.20 Calculation loop comparison a) MPC implementation by using serial-computing device b) MPC implementation by fully paralleing technique. 38

Figure 3.1 Conventional model predictive control scheme for first case. 43

Figure 3.2 Conventional model predictive control scheme for second case. 44

Figure 3.3 Switching state elimination process. 46

Figure 3.4 Elimination process for load current control. 47

Figure 3.5 Vector representation of current error term. 49

Figure 3.6 Algorithm flow chart for proposed method for second case. 50

Figure 3.7 Simulation results for CASE 1 (45 Hz load current reference) a) Supply voltage b) Load current c) Supply current d) Output load voltage. 51

Figure 3.8 Frequency spectrum of load current (Case 1 and 45 Hz load current reference). 52

Figure 3.9 Frequency spectrum of source current (Case 1 and 45 Hz load current reference). 52

Figure 3.10 Simulation reults for CASE 1 (90 Hz load current reference) a) Supply voltage b) Load current c) Supply currentd) Output load voltage. 53

Figure 3.11 Frequency spectrum of load current (Case 1 and 90 Hz load current reference) 53

Figure 3.12 Frequency spectrum of load current (Case 1 and 90 Hz load current reference).....54
Figure 3.13 Dynamic response of MPC based on switching state elimination 54

Figure 3.14 Phase plane plot of load current 55

Figure 3.15 Simulation results for Case 2 (50 Hz load current) a) Supply voltage b) Load current c) Supply current d) Output load voltage 55

Figure 3.16 Frequency spectrum of load current (Case 2 and 50 Hz load current reference) 56

Figure 3.17 Frequency spectrum of source current (case 2 and 50Hz load current reference) 56

Figure 3.18 Experiemental results in case of 45 Hz load current frequency 57

Figure 3.19 FFT analysis of load current (45 Hz load current reference) a) Load current measurement b) Frequency spectrum of load current 58

Figure 3.20 FFT analysis of source current (45 Hz load current reference) a) Source current measurement b) Frequency spectrum of source current 58

Figure 3.21 Experimental result in case of 60 Hz load current frequency 59

Figure 3.22 FFT analysis of load current (60 Hz load current reference) a) Load current measurement b) Frequency spectrum of source current 59

Figure 3.23 FFT analysis of source current (60 Hz load current reference) a) Source current measurement b) Frequency spectrum of source current 60

Figure 3.24 Experimental result in case of 90 Hz load current frequency 60

Figure 3.25 FFT analysis of load current (90 Hz load current reference) a) Load current measurement b) Frequency spectrum of source current 61

Figure 3.26 FFT analysis of source current (90 Hz load current reference) a) Source current measurement b) Frequency spectrum of source current 61

Figure 4.1 Conventional control method for nine-switch inverter 65

Figure 4.2 Nine-switch inverter with output filter 67

Figure 4.3 Output filter model. 68

Figure 4.4 Output LC filter model 68

Figure 4.5 Block diagram of the system and observer. 72

Figure 4.6 Poles of the system and observers 73

Figure 4.7 Selection of observer poles 74

Figure 4.8 Model predictive control scheme for nine-switch inverter 75

Figure 4.9 Nine-switch inverter under unknown load conditions 76

Figure 4.10 Algorithm flow chart for predictive controller 77

Figure 4.11 Poles location of observer and LC filter for simulation 79

Figure 4.12 Simulation results a) Output upper capacitor voltage b) Output lower capacitor voltage c) Upper load current d) Lower load current 80

Figure 4.13 Output upper capacitor voltage frequency spectrum under linear load condition 80

Figure 4.14 Output lower capacitor voltage frequency spectrum under linear load condition 81

Figure 4.15 Upper load current frequency spectrum under linear load condition 81

Figure 4.16 Lower load current frequency spectrum under linear load condition 82

Figure 4.17 Output filter inductro current under linear load condition a) Upper inductor current waveform b) Lower inductor current waveform 82

Figure 4.18 Load current estimation under linear load condition a) Upper load current estimation b) Lower load current estimation 83

Figure 4.19 Dynamic response of predictive controller under linear load condition a) Upper output capacitor voltage b) Loweroutput capacitor voltage 83

Figure 4.20 Phase plane plot for capacitor voltage a) Upper output capacitor voltage plot b) Lower output capacitor voltage plot 84

Figure 4.21 Dynamic behavior of upper observer and controller under linear load conditions a) Upper output capacitor voltage b) Upper loadcurrent estimation . . 84

Figure 4.22 Dynamic behavior of lower observer and controller under linear load conditions a) Lower output capacitor voltage b) Lower load current estimation . 85

Figure 4.23 Diode-bridge rectifier 85

Figure 4.24 Output filter capacitor voltage under unbalanced load condition a) Upper capacitor voltage b) Lower capacitor voltage 86

Figure 4.25 Output load current under unbalanced load condition a) Upper load current b) Lower load current 86
Figure 4.26 Frequency spectrum of output voltage under nonlienar load condition a) Upper output voltage frequency spectrum b) Lower output voltage frequency spectrum. 87

Figure 4.27 Filter inductor current under unbalanced load condition a) Upper filter current b) Lower filter current 88

Figure 4.28 Dynamic response of predictive controller under unbalanced load condition a) Upper capacitor voltage b) Lower capacitor voltage 88

Figure 4.29 Dynamic reponse of observer under unbalanced load condition a) Upper load current estimation b) Lower load current estimation 89

Figure 4.30 Step response ofthe system a) Upper capacitor voltage b) Upper load current estimation 89

Figure 4.31 Step response of the system a) Lower capacitor voltage b) Lower load current estimation 90

Figure 5.1 Predictive control scheme for dual-output indirect matrix converter 96

Figure 5.2 Switching state elimination process 97

Figure 5.3 Simulation results for dual-output indirect matrix converter a) Supply voltage b) Upper load current c) Lower load current d) Source current 99

Figure 5.4 Frequency spectrum of upper load current. 99

Figure 5.5 Frequency spectrum of lower load current 100

Figure 5.6 Frequency spectrum of source current 100

Figure 5.7 Dynamic response of proposed control scheme a) Upper load current b) Lower load current 101

Figure 5.8 Phase planeplot of output load current a) Upper load current b) Lower load current 101

Figure 5.9 DC-link voltage 102

Figure 5.10 DC-link current 102

Figure 5.11 Instantanesous reactive power 103

Figure 5.12 Supply current 104

Figure 5.13 Frequency spectrum of input current a) Spectral contents with reactive power b) Spectral content without reactive power control 105

LIST OF SYMBOLS

α	Coefficient of characteristic equation
θ	Angle of the vector (radian)
ξ	Damping ratio
σ	Normalized current error
A	Weighting factor
B	Weighting factor
C	Weighting factor
C_f	Input filter capacitance
C_1	Control constraint for load current control problem
C_2	Control constraint for reactive power control problem
D	Weighting factor
f_1	Sub-optimization problem (Load current control)
f_2	Sub-optimization problem (Reactive power control)
f_3	Sub-optimization problem (Switching frequency control)
g	Cost function
I	Identity matrix
i_{DC}	DC-link current (A)

i_f	Output filter current (A)
i_o^e	Load current error (A)
$i_o(k)$	Load current value at instant k (A)
$i_o(k+1)$	Load current value at instant k+1 (A)
i_{o_low}	Lower load current (A)
i_{o_up}	Upper load current (A)
$i_{o\_low}^*$	Upper load current reference (A)
$i_{o\_up}^*$	Lower load current reference (A)
K	Observer gain
L	Load inductance (H)
L_f	Input filter inductance (H)
m	Size of the solution set for reactive power control
n	Size of the solution set for switching frequency control
P	Active power (W)
p	Pole of the system
Q	Reactive power (VAR)
Q^*	Reactive power reference (VAR)
R	Load resistance (Ω)
R_f	Input filter resistance (Ω)
S	Switch position
S(k+1)	Future switching combination
S_{LC}	LC filter pole

$S_{observer}$	Observer pole
S_{sys}	Pole of the system
T	Instantaneous transfer matrix
T_1	Sub-finite solution set (Load current control)
T_2	Sub-finite solution set (Reactive power control)
T_3	Sub-finite solution set (Switching frequency control)
T_{CSR}	Interconnection of rectifier stage
T_L	Interconnection matrix of lower load
Ts	Sampling period
T_U	Interconnection matrix of upper load
$u(k)$	Control input
v_c	Output filter capacitor voltage (V)
v_{DC}	DC-link voltage (V)
v_i	Input voltage (V)
v_{i_low}	Lower load voltage (V)
v_{i_up}	Upper load voltage (V)
v_o	Output voltage (V)
v_s	Supply voltage (V)
x	State vector
$\hat{x}$	Estimated state
$x(k)$	State variable
$x(k+1)$	Future value of state variable

$x^{*}(k+1)$	Future reference of state variable

CHAPTER 1

INTRODUCTION

1.1 FINITE CONTROL SET MODEL PREDICTIVE CONTROL

Finite Control Set Model Predictive Control (FCS-MPC) is an optimization-based control approach that minimizes a cost function to optimize system behavior. MPC offers many advantages: in particular it makes it easy to handle multiple control objectives, which can be represented by a multi-term cost function. The inclusion of nonlinearities and constraints in the control law is straightforward. The MPC techniques applied to power converters have been classified into two main categories [1]-[3]: Continuous Control Set MPC and Finite Control Set MPC. In the first category, a modulator is used to generate gate signals and the control signal is continuous [4]-[7]. In the second category, FCS-MPC solves a multi-objective optimization problem by making an exhaustive search over a finite control set and determining the optimal control action. The main advantage of FCS-MPC lies in the direct application of the control action to the converter without requiring a modulation stage.

A power converter can be modeled as a discrete system with a finite number of possible states and MPC uses this discrete model of the system to predict the future evolution of the controller variables [8]-[13]. Future values of control variables are calculated by using prediction equations for each possible switching state and these predictions are used to calculate the errors with respect to the reference values. The user-

defined cost function, which is a function of these errors, is calculated for all possible switching states to determine the optimal switching combination. This optimal switching combination, which represents the optimal control action, is applied to the converter for the next time interval [14]-[18]. The user-defined cost function is usually a multi-objective cost function, so that more than one control objectives can be achieved simultaneously. Note that, in order to implement a multi-objective controller using conventional linear control technique, a multi-loop controller is typically required with all the associated complications. In MPC, different control objectives can be controlled simultaneously using a single control loop. Since MPC does not use a modulator and a change of switching state does not occur at every sampling time, the system has a variable switching frequency. Different control objectives can be introduced in the cost function, such as output load current control, reduction of the switching frequency and minimization of instantaneous reactive power [19]-[23]. The future values of the state of the system are predicted for a single predefined horizon. The working principle of MPC is shown in Figure 1.1 for the case of a single control objective and a one-time-step horizon. A variable x is required to follow a reference x*. A time t_k all possible future states are calculated by applying to the system model for all possible control variables. The control action that provides the minimum error is selected for the t_k-t_{k+1} time interval.

The optimal action is determined by minimizing the cost function and the whole process is repeated again for each sampling instant considering the new measured data. All possible switching states are evaluated to determine the best-suited switching combination and the so-determined optimal switching state is selected for the next time

interval. The number of calculations required is directly related to the number of possible switching states. In case of three-phase voltage source inverter, there are eight possible switching states and calculating predictions for the eight possible switching states is a manageable task. But in case of DMC or multi-level converter, real-time implementation of the MPC algorithm may be problematic given the large number of possible switching states and consequently the large amount of calculations required.

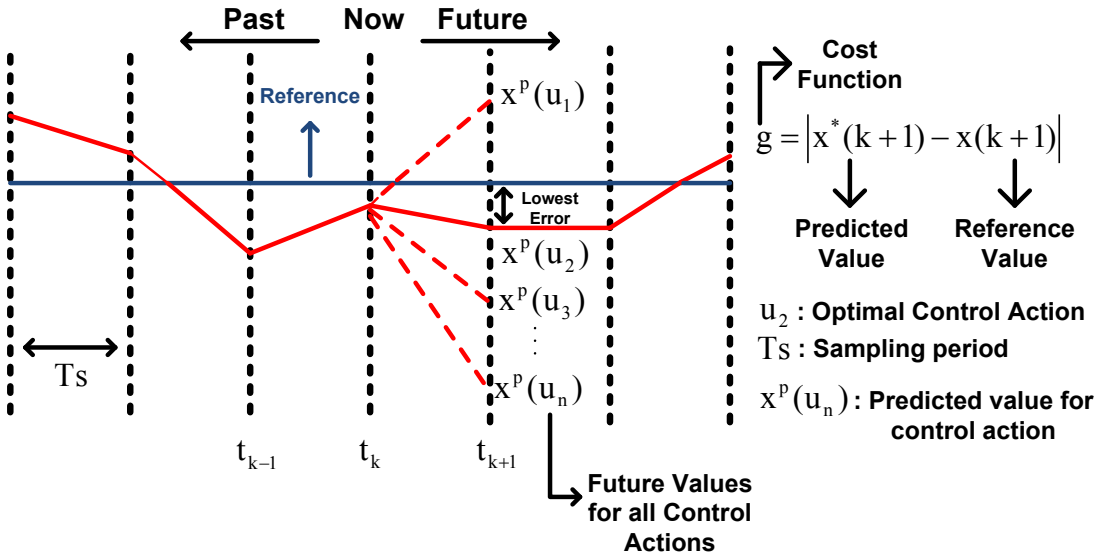


Figure 1.1: Working principle of model predictive control

Although the theory of MPC was developed in the 1970s, its application in power electronics and drives is more recent due to the high computation burden. The fast microcontrollers available in the last decade have triggered research in new control schemes for power converter systems, such as MPC. For this application, the optimization problem is made easier by the discrete nature of power converters. Fast digital control platforms make online optimization process possible and solving online optimization problem by using the finite number of switching states is a real possibility. The design of finite control set model predictive control consists of the following steps:

1) Modeling of power converter with finite states

2) Derivation of the relationship between switching states and control variables

3) Design of cost function that represents the desired system behavior

4) Development of an algorithm that finds the switching state that minimizes the cost function

In general, these four steps can be used to design a model predictive controller. The general model predictive control scheme for power converter systems is shown in Figure 1.2.

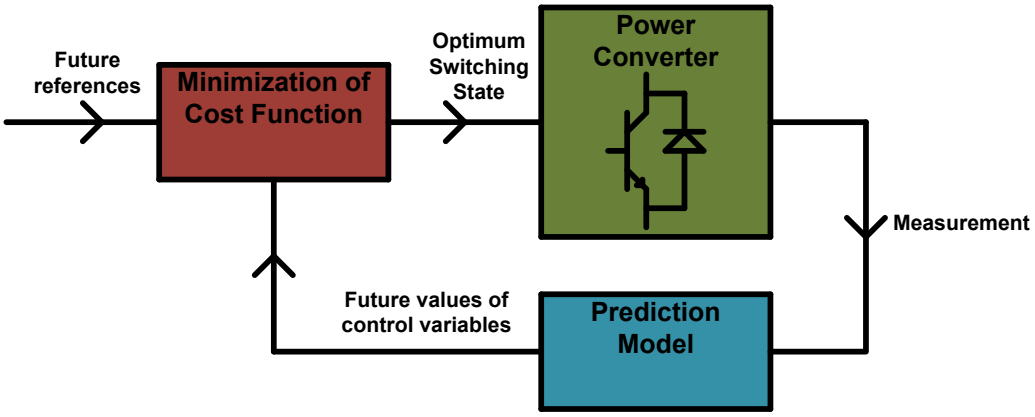


Figure 1.2: General predictive control scheme for power converters

1.2 Direct Matrix Converter

The Direct Matrix Converter (DMC) was introduced by Venturini and Alesina [24]. The Direct Matrix Converter is a good alternative to the traditional two stage ac-dc-ac topology, because it can convert an ac source to an ac load without a dc-link and without large energy storage components. This significantly improves overall system reliability by eliminating failure-prone dc-link electrolytic capacitors and may improve efficiency, given the single power conversion stage. The DMC, shown in Figure. 1.3, has

nine bi-directional switches, which directly connect the three-phase power supply to the three-phase ac load. An L-C filter is used at its input to improve the quality of the input current. At the output, it delivers voltages and currents to the load with high quality and without restrictions on frequency, which can be different from the source frequency. Moreover, the DMC is power bidirectional, i.e., it allows power to flow from source to the load and in the opposite direction, which means that it is suitable for regenerative load applications. Two switching restrictions must be considered for proper operation. Firstly, since the DMC is fed by a voltage source, any switching state that shorts two input lines is not allowed. Secondly, since the converter output is inductive, an interruption of the output current is not allowed, because it would lead to large voltage spikes. Considering these two switching restrictions, 27 possible switching combinations are allowed for proper operation.

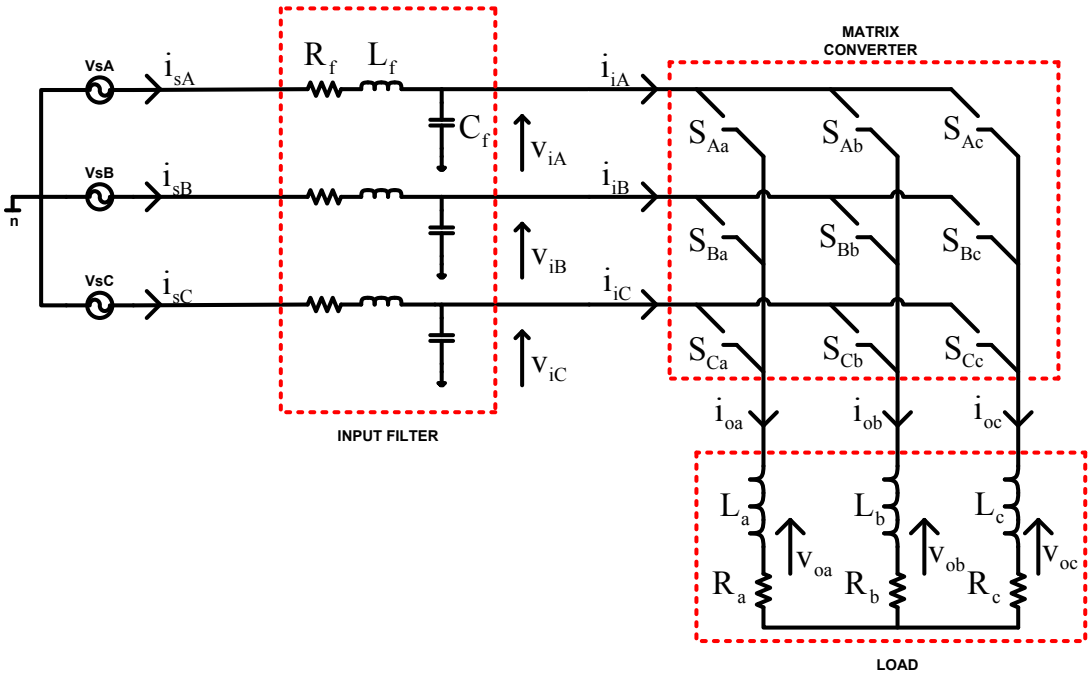


Figure 1.3: Direct matrix converter topology

These 27 switching combinations can be considered as possible control actions for DMC. With reference to Figure 1.3, the switching function of a bi-directional switch of DMC is defined as,

$$S_{ij} = \begin{Bmatrix} 1, & \text{switch} & \text{on} \\ 0, & \text{switch} & \text{off} \end{Bmatrix} \tag{1.1}$$

The two switching restrictions described above can be represented by the conditions

$$S_{Aj} + S_{Bj} + S_{Cj} = 1 \quad \forall \quad j \in \{a, b, c\}$$

which require that each output be connected to one and only one input. Several switching combinations for DMC are shown in Figure 1.4. The first two switching combinations are allowed for proper operation, whereas the remaining two are not. In case of the third switching combination, two input lines are shorted. For the fourth combination, the output load current is interrupted.

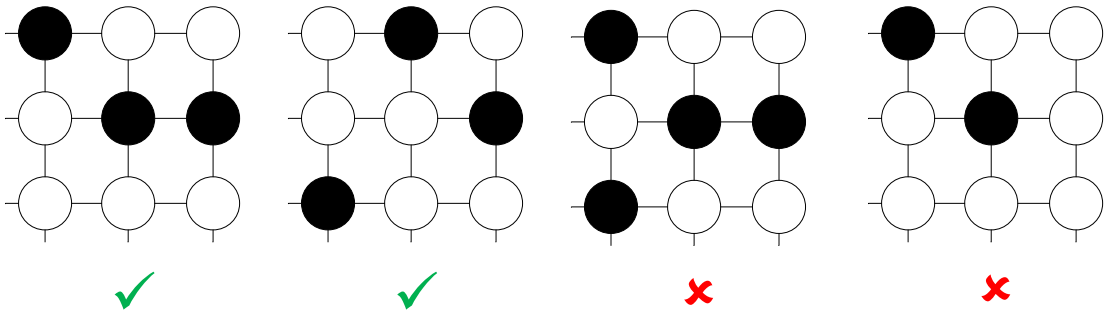


Figure 1.4: Switching combinations for direct matrix converter

1.3 Dual Output Nine-Switch Inverter

Conventional three-phase inverters have a single three-phase ac output and six switches. The Nine-Switch Inverter (NSI) is a dual-output inverter (see Figure 1.5), recently introduced [25], having only nine switches. Note that two separate inverters would require a total of 12 switches. The NSI is based on the conventional voltage-source

inverter with three series switches and it has been used for various applications such as industrial motor control and electrical vehicle motor drives [26]. For the NSI topology, each leg has three switches and there are eight different ON-OFF positions. All switches on the same leg cannot be turned on at the same time to avoid DC bus short circuit. Another switching restriction is that at least two switches on the same leg should be on, so that floating of the connected load is avoided.

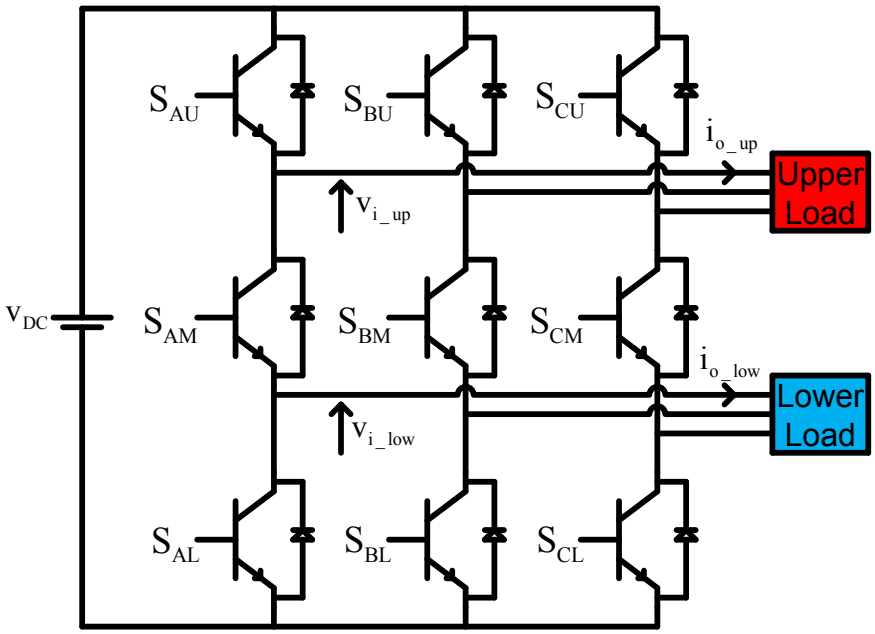


Figure 1.5: Nine-switch inverter topology

Considering these switching restrictions, each leg can be in three different switch combinations which are called {1, 0, -1} [30]. Possible switch positions are illustrated in Table I with I=A, B, C identifying the inverter legs. The NSI has 27 possible switching states, but, since some of them redundant, only 15 of these switching states are sufficient to control the two ac loads. Frequencies and amplitudes of the two ac loads can be different and the two loads can be controlled independently. Benefit of using only 15

switching states instead of all 27 allowable switching states is that computational burden is decreased.

Table 1-1 Switches positions of Legs

	$S_i = 1$	$S_i = 0$	$S_i = -1$
S_{iU}	ON	OFF	ON
S_{iM}	OFF	ON	ON
S_{iL}	ON	ON	OFF

1.4 DUAL-OUTPUT INDIRECT MATRIX CONVERTER

The Indirect Matrix Converter (IMC) is a two-stage ac-ac power converter that can convert ac source to ac load without a dc-link capacitor or other storage components. Dual-output indirect matrix converter is based on the traditional IMC topology but the conventional six-switch inverter is replaced by a nine-switch inverter. Many matrix converter topologies have been proposed, mostly of the single-output type [22],[28]. The dual-output IMC, shown in Figure 1.6, uses four-quadrant switches in the bidirectional Current Source Rectifier (CSR) stage and no dc-link capacitor is required. The rectifier stage is connected to the Nine-Switch Inverter stage [27].

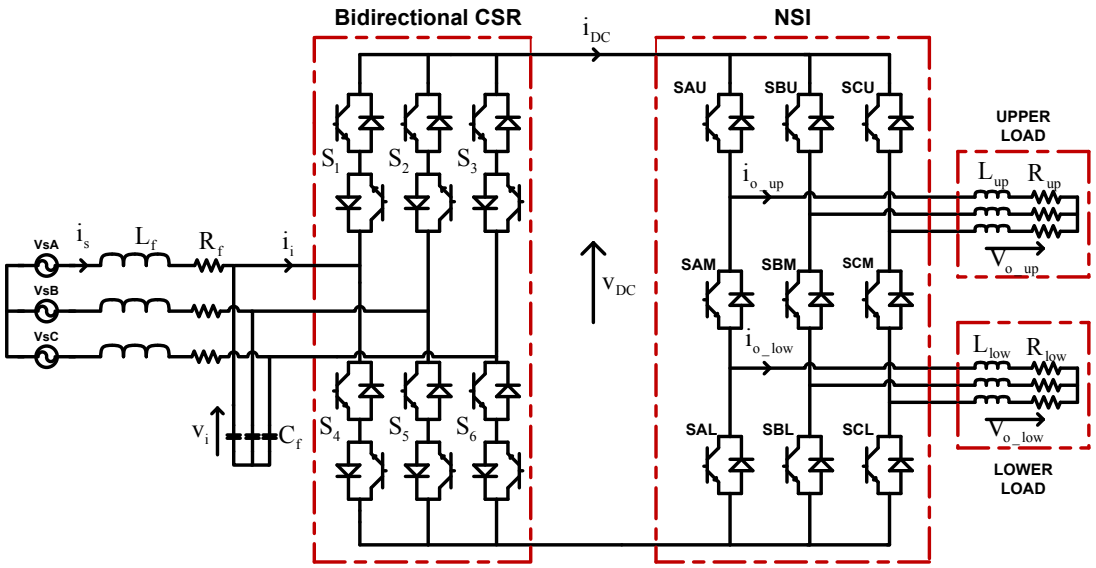


Figure 1.6: Dual-Output Indirect Matrix Converter Topology

1.5 RESEARCH OBJECTIVES

On the one hand, model predictive control method has several advantages, such as allowing easy inclusion of nonlinearities and providing fast dynamic response. On the other hand, the MPC method has several drawbacks:

1. Real-time implementation of MPC incurs high computational burden
2. There is no analytical procedure to adjust the weighting factors for multi-objective optimization problem
3. A complete system model must be derived since MPC method uses this model to predict control variables
4. MPC implementation is not straightforward for several power converter topologies, such as dual-output power converters.

In this dissertation, these four disadvantages are considered and methods are proposed to overcome them. In general, the proposed research can be divided into four parts that will be described in later chapters.

Chapter 2 presents efficient real-time implementation of MPC for direct matrix converter. Finite Control Set MPC (FCS-MPC) imposes a very high computational burden that causes significant hardware requirements and suitable technology should be used to implement this control algorithm due to its complex computational scheme. The objective is to reduce execution time of MPC algorithm by taking advantage of the fact that MPC control is very parallelizable. A solution exploiting the parallel processing capability of FPGAs is proposed.

Chapter 3 presents novel model predictive control method based switching state elimination. In a multi-optimization problem, adjusting weighting factors is problematic since there is no specific procedure to pick weighting factors. Switching state elimination technique is proposed to control several control objectives without weighting factors.

Chapter 4 investigates model predictive control performance under unknown load condition. The proposed method can control a nine-switch inverter and two ac loads are controlled simultaneously. Full-order observers are used to estimate load currents and the proposed method is tested under linear and nonlinear load conditions. This chapter presents the observer design procedure and predictive controller design for a nine-switch inverter.

Chapter 5 presents the model predictive control scheme for a dual-output indirect matrix converter. This chapter includes modeling of dual-output IMC and the design steps for predictive control scheme. Predictive controller design procedure covers

derivation of system model and future expression of control variables, cost function design and selecting weighting factors. The proposed method controls two ac loads and instantaneous reactive power simultaneously.

Chapter 6 gives a summary of the contributions and proposes some future work.

CHAPTER 2

FPGA-BASED MODEL PREDICTIVE CONTROLLER FOR DIRECT MATRIX CONVERTER

The model predictive control method implementation imposes a very high computational burden and causes significant hardware requirements for real-time implementation. Suitable technology should be used to implement this control algorithm due to its computationally intensive computation scheme. In conventional real-time implementation of model predictive control for direct matrix converter, DSP and FPGA are both used to ensure fast processing operation and preserve performance of the predictive controller [41]-[43]. In this work, a fully FPGA-based real-time implementation of model predictive control is proposed for DMC, eliminating the need for a DSP. This simplifies system implementation. A 1.6 kW DMC prototype was built to validate the proposed method. An Altera-DEO nano FPGA evaluation board is used to implement the control algorithm.

2.1 DIRECT MATRIX CONVERTER MODEL

The MPC uses the discrete-time model of the system for predicting the future behavior of the controlled variables and calculates a cost function related to multiple control objectives to find its minimum. For this reason, derivation of the system model is

critical in the model predictive control approach. With reference to Figure 1.3, the instantaneous transfer matrix T is defined as

$$\mathbf{T} = \begin{bmatrix} S_{Aa} & S_{Ab} & S_{Ac} \\ S_{Ba} & S_{Bb} & S_{Bc} \\ S_{Ca} & S_{Cb} & S_{Cc} \end{bmatrix} \tag{2.1}$$

The elements of matrix **T** are 1 when the corresponding switch is closed and zero when it is open. The load and input voltages can be expressed as vectors. The output load voltage is defined as

$$\mathbf{v_o} = \begin{bmatrix} v_{oa} & v_{ob} & v_{oc} \end{bmatrix}^T \tag{2.2}$$

and the input voltage vector is defined as

$$\mathbf{v_i} = \begin{bmatrix} v_{iA} & v_{iB} & v_{iC} \end{bmatrix}^T \tag{2.3}$$

Thus the relationship between input and output voltages is given by

$$\mathbf{v_o} = \mathbf{T}^T \mathbf{v_i} \tag{2.4}$$

The input and output load current vectors are defined as

$$\mathbf{i_i} = \begin{bmatrix} i_{iA} & i_{iB} & i_{iC} \end{bmatrix}^T \tag{2.5}$$

$$\mathbf{i_o} = \begin{bmatrix} i_{oa} & i_{ob} & i_{oc} \end{bmatrix}^T \tag{2.6}$$

The relationship between input and output load current is given by

$$\mathbf{i_i} = \mathbf{T}\mathbf{i_o} \tag{2.7}$$

In this work, an RL circuit is used as the load model and therefore the continuous model of RL load is

$$\mathbf{v_o} = R\mathbf{i_o} + L\frac{d\mathbf{i_o}}{dt} \tag{2.8}$$

where R is the load resistance and L is the load inductance. The dynamic model of the second order input filter can be expressed as

$$\mathbf{v_s} = L_f \frac{d\mathbf{i_s}}{dt} + R_f \mathbf{i_s} + \mathbf{v_i} \tag{2.9}$$

$$\mathbf{i_s} = \mathbf{i_i} + C_f \frac{d\mathbf{v_i}}{dt} \tag{2.10}$$

2.2 Model Predictive Control for Direct Matrix Converter

The predictive control strategy is based on the idea that only a finite number of possible switching states can be generated by power converters. For the selection of the appropriate switching state to be applied, a proper cost function needs to be defined and this cost function will be evaluated for each possible switching state. Prediction of the future values of control variables is used to calculate the cost function and the switching state that minimizes the cost function is selected. There are three steps to design the predictive controller:

1) Building the prediction model of the system

2) Defining control objectives

3) Designing cost function

A discrete-time model is used to predict future value of the control variables and the cost function defines the desired system behavior.

2.2.1 Prediction Model

In order to obtain the discrete-time model, the forward Euler approximation is used

$$\frac{di_o}{dt} \approx \frac{i_o(k+1) - i_o(k)}{Ts} \tag{2.11}$$

The load current prediction equation can be obtained using (2.8) and (2.11). The future load current is given in (2.12). In (2.12), $v_o(k)$ is the candidate voltage vector and $i_o(k)$ is the load current measurement.

$$i_o(k+1) = \frac{Ts}{L} v_o(k) + i_o(k)(1 - \frac{RTs}{L}) \tag{2.12}$$

The second order input filter can be represented by a state-space model.

$$\begin{bmatrix} \dot{v}_i \\ \dot{i}_s \end{bmatrix} = A_c \begin{bmatrix} v_i \\ i_s \end{bmatrix} + B_c \begin{bmatrix} v_s \\ i_i \end{bmatrix} \tag{2.13}$$

where

$$A_c = \begin{bmatrix} 0 & \frac{1}{C_f} \\ \frac{-1}{L_f} & \frac{-R_f}{L_f} \end{bmatrix} \quad \text{and} \quad B_c = \begin{bmatrix} 0 & \frac{-1}{C_f} \\ \frac{1}{L_f} & 0 \end{bmatrix} \tag{2.14}$$

The discrete time state-space model of the input filter can be expressed as follows

$$\begin{bmatrix} v_i(k+1) \\ i_s(k+1) \end{bmatrix} = \Phi \begin{bmatrix} v_i(k) \\ i_s(k) \end{bmatrix} + \Gamma \begin{bmatrix} v_s(k) \\ i_i(k) \end{bmatrix} \tag{2.15}$$

where

$$\Phi = e^{A_c Ts} \quad \text{and} \quad \Gamma = \int_0^{Ts} e^{Ac(Ts-\tau)} B_c \, d\tau \tag{2.16}$$

The future source current can be determined by using a discrete-time model of the input filter. Source current prediction is defined as

$$i_s(k+1) = \Phi(2,2) i_s(k) + \Phi(2,1) v_i(k) + \Gamma(2,1) v_s(k) + \Gamma(2,2) i_i(k) \tag{2.17}$$

Instantaneous input active and reactive power can be predicted using source current prediction and source voltage measurement. Input active and reactive power are expressed in α-β frame and the Park transformation is used to calculate real and imaginary components of associated vectors. Subscript α and β represent real and imaginary components of source current and source voltage. Reactive power is calculated as the imaginary part of the product of the source voltage multiplied by the complex conjugate of the source current.

$$Q(k+1) = \mathrm{Im}\left\{ \mathbf{v_s}(k+1)\,\overline{\mathbf{i_s}(k+1)} \right\} = v_{s\beta}(k+1) i_{s\alpha}(k+1) - v_{s\alpha}(k+1) i_{s\beta}(k+1) \tag{2.18}$$

Instantaneous input active power is defined as

$$P(k+1) = \mathrm{Re}\left\{ \mathbf{v_s}(k+1)\,\overline{\mathbf{i_s}(k+1)} \right\} = v_{s\alpha}(k+1) i_{s\alpha}(k+1) + v_{s\beta}(k+1) i_{s\beta}(k+1) \tag{2.19}$$

2.2.2 COST FUNCTION DESIGN

Cost function design is critical in model predictive control approach because it defines switching state selection criteria. The most commonly used terms in a cost function are the ones that represent a variable following a reference. These terms can be expressed as an error between future value of the control variable and its reference:

$$g = \left| x^*(k+1) - x(k+1) \right| \tag{2.20}$$

where $x^*(k+1)$ is the reference value and $x(k+1)$ is the predicted value. The cost function term g is the absolute value of the error between predicted value and its reference. In this work, there are three control objectives: output load current control, minimization of instantaneous reactive power and reduction of switching frequency (to

reduce switching losses and improve efficiency). The output load current control can be achieved by minimizing the absolute error between future load current and future load current reference. The load current control term can be expressed in orthogonal coordinates

$$g_1 = \left|i_{o\alpha}{}^*(k+1) - i_{o\alpha}(k+1)\right| + \left|i_{o\beta}{}^*(k+1) - i_{o\beta}(k+1)\right| \tag{2.21}$$

where $i_{o\alpha}(k+1)$ and $i_{o\beta}(k+1)$ are the real and imaginary parts of the predicted load current. This prediction is obtained using the load model, which is defined in (2.12). $i_{o\alpha}{}^*(k+1)$ and $i_{o\beta}{}^*(k+1)$ are the real and imaginary part of the future load current reference. For simplicity, it can be assumed that the reference load current does not change significantly in one sampling period in case of short sampling period. In this case, the $i_o^*(k+1) \approx i_o^*(k)$ approximation can be used to predict the future load current. On the other hand, extrapolation methods can be used to predict sinusoidal reference in case of a large sampling period. Lagrange extrapolation method can be used to predict the load current reference [58]. Lagrange extrapolation technique is given in (2.22).

$$i_o^*(k+1) = \sum_{h=0}^{n} (-1)^{n-1} \begin{bmatrix} n+1 \\ h \end{bmatrix} i_o^*(k+h-n) \tag{2.22}$$

Sinusoidal load current reference can be predicted in case of n=2.

$$i_o^*(k+1) = 3i_o^*(k) - 3i_o^*(k-1) + i_o^*(k-2) \tag{2.23}$$

The objective of controlling instantaneous reactive power can be easily achieved by introducing term g2, which penalizes the absolute error of reactive power.

$$g_2 = \left|Q^*(k+1) - Q(k+1)\right| \tag{2.24}$$

The reactive power is predicted using the input filter model and the reference value for reactive power control, $Q^*(k+1)$, can be chosen as zero. In power electronics applications, obtaining unity input power factor is really important to improve power quality. Classical modulation methods to obtain unity input power factor are complicated, whereas the predictive control approach is very simple. Power factor can be improved significantly by introducing reactive power minimization term in the cost function.

Another important control objective is to reduce the average switching frequency of the system. For power converter systems, switching losses are typically proportional to the switching frequency, so reducing the switching frequency of the system is highly desirable to reduce losses and improve efficiency. Since FCS-MPC does not use modulator and a change of switching state does not necessarily occur at every sampling time, the system has a variable switching frequency. To assign a cost to the average switching frequency, one can count the number of switches that commutate when a new switching state is applied to the system. The cost for controlling switching frequency is defined as

$$g_3 = \left|S(k+1) - S(k)\right| \tag{2.25}$$

where $S(k)$ is current switching combination and $S(k+1)$ is future switching state. The difference between future and current switching states is penalized to reduce switching frequency. The total cost function of the system, including terms (2.21), (2.24) and (2.25), is expressed in (2.26).

$$g = Ag_1 + Bg_2 + Cg_3 \tag{2.26}$$

A, B and C are the weighting factors. Typically they are adjusted empirically. These weighting factors need to be properly tuned to obtain desired system performance.

Otherwise, the controller performance is affected significantly. In this work, the weighting factor for output load current control term A, is chosen as 1 and an offline-tuning technique is used to adjust weighting factor B and C.

2.2.3 MODEL PREDICTIVE CONTROL SCHEME

The predictive control scheme for the direct matrix converter is represented in Figure 2.1. The MPC selects the switching state of the converter that minimizes the cost function, defined in (2.26). The load model is used to predict the future load current and the input filter model is used to predicted instantaneous reactive power. Consequently, the valid switching state that produces the lowest value of the cost function is selected for the next sampling period.

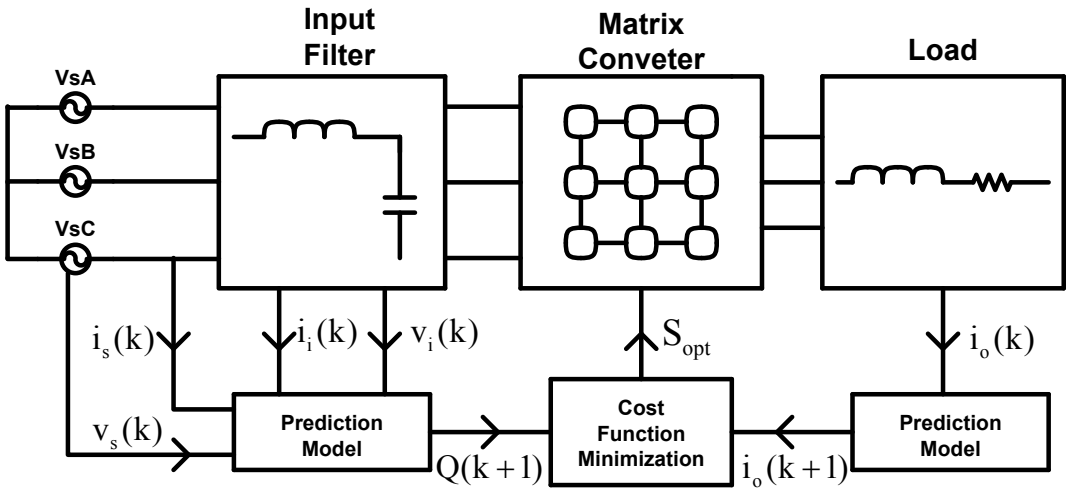


Figure 2.1: Model predictive control scheme for direct matrix converter

Predictive control approach can effectively control the output current and instantaneous reactive power. The strategy presented allows the input power factor to be regulated by simple and straightforward means. This method can be easily implemented by taking advantage of the present technologies, which will be explained in a later chapter, and

implementation of MPC algorithm is much simpler compared to conventional control technique.

2.3 ISSUES WITH CONVENTIONAL REAL-TIME IMPLEMENTATION

In conventional real-time implementation of model predictive control for matrix converter, Digital Signal Processors (DSPs) and Field-Programmable Gate Arrays (FPGAs) are both used to complete all control calculations and several other tasks, such as commutation and protection. In the literature, using both DSP and FPGA is the preferred technology for implementing the MPC algorithm for matrix converter but it requires two separate digital control platforms for proper operation [48]-[50]. The main issue with the conventional real-time implementation approach is that DSP devices can do only serial computing and they are not fast enough to complete all required tasks in case of a short sampling period. For this reason, a separate digital control platform, such as FPGA, is used to complete other tasks such as safe commutation scheme and protection, and DSP is only responsible for performing control calculations. When control schemes based on model predictive control method are implemented experimentally, a large number of calculations are required. For the power converters, if DSP is used for performing model predictive control calculations, there will be a delay in control actuation [51]. In order to overcome this problem, several delay compensation methods have been reported [55],[56]. The main drawback of the delay compensation technique is that an accurate system model is required. Otherwise delay compensation techniques do not work well. For all these reasons, decreasing the time required for control calculations is highly desirable. The conventional real-time implementation is shown in Figure 2.2.

Conventional real-time implementation is complicated because interfacing between two digital control platform is not straightforward in terms of software architecture. The interface between FPGA and DSP also contributes a delay because a finite time is required to transfer the data from DSP to FPGA for generating the appropriate gate signals. As a result, the interfacing between to digital control platform and the delay in applying new control actions is problematic in conventional method.

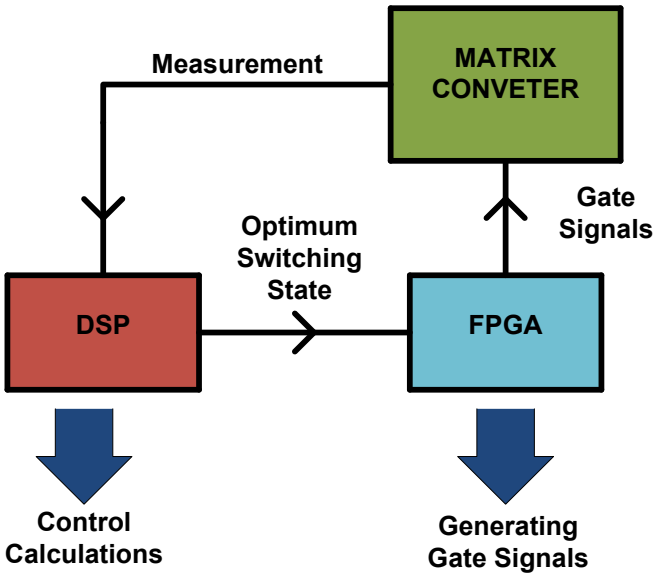


Figure 2.2: Conventional real-time implementation for direct matrix converter

2.4 Proposed Real-Time Implementation Method

Field Programmable Gate Arrays (FPGAs) are a better solution for the real-time implementation of FCS-MPC method over traditional microcontrollers and DSPs, since the discrete nature of predictive controller fits well with the features of FPGA devices, such as parallel processing capability and pipelining. Parallel computational capability of FPGA devices can be used to perform independent control calculations during the same clock cycle, so that the time required for MPC implementation can be significantly

reduced [59]. This overcomes the control delay issue and provides better performance under transient conditions, especially in the presence of in accuracies in the prediction model.

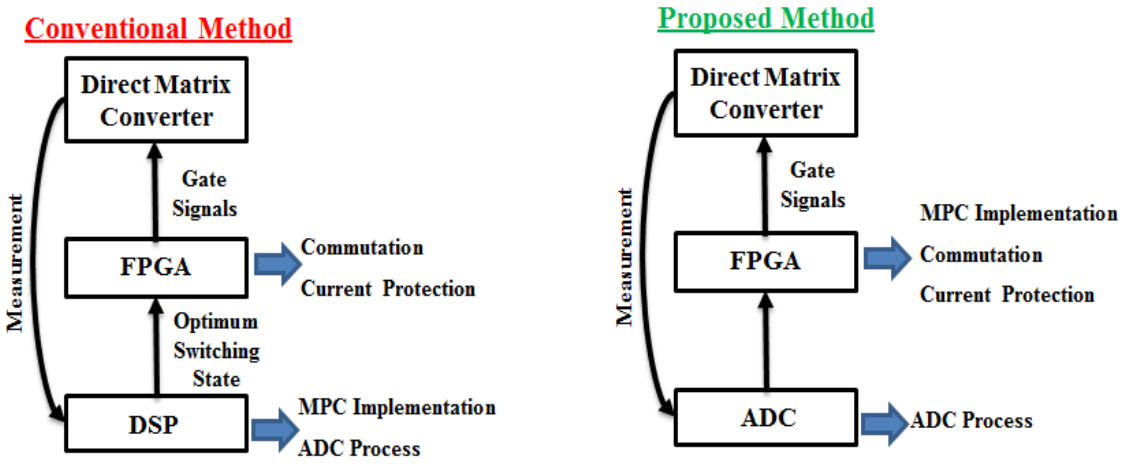


Figure 2.3: Comparison between conventional method and proposed method

FCS-MPC is a strategy to control selected state variables by performing a real-time optimization. At the beginning of the current time intervals, measurements of the current values of the state variables are performed. The trajectories of the state variables in the following time interval are calculated for all possible states using the system model and the optimal switching state is selected by evaluating the possible values of a cost function. The state resulting in the minimal cost is selected. The so-determined optimal switching state is applied at the beginning of the following time interval. The one-step-ahead prediction for control goals must be completed within the current time interval. The computational time can be dramatically reduced by parallel computing implementation of the FCS-MPC, as shown in Figure 2.4. Since future control variables values for different switching states are independent, these calculations can be

parallelized. Notice, however, that some blocks depend on the output of other blocks, and therefore proper order of execution is essential. For example, current cost calculations require the predicted current results. The order of execution is controlled by a synchronizer block which is based on Finite State Machine (FSM).

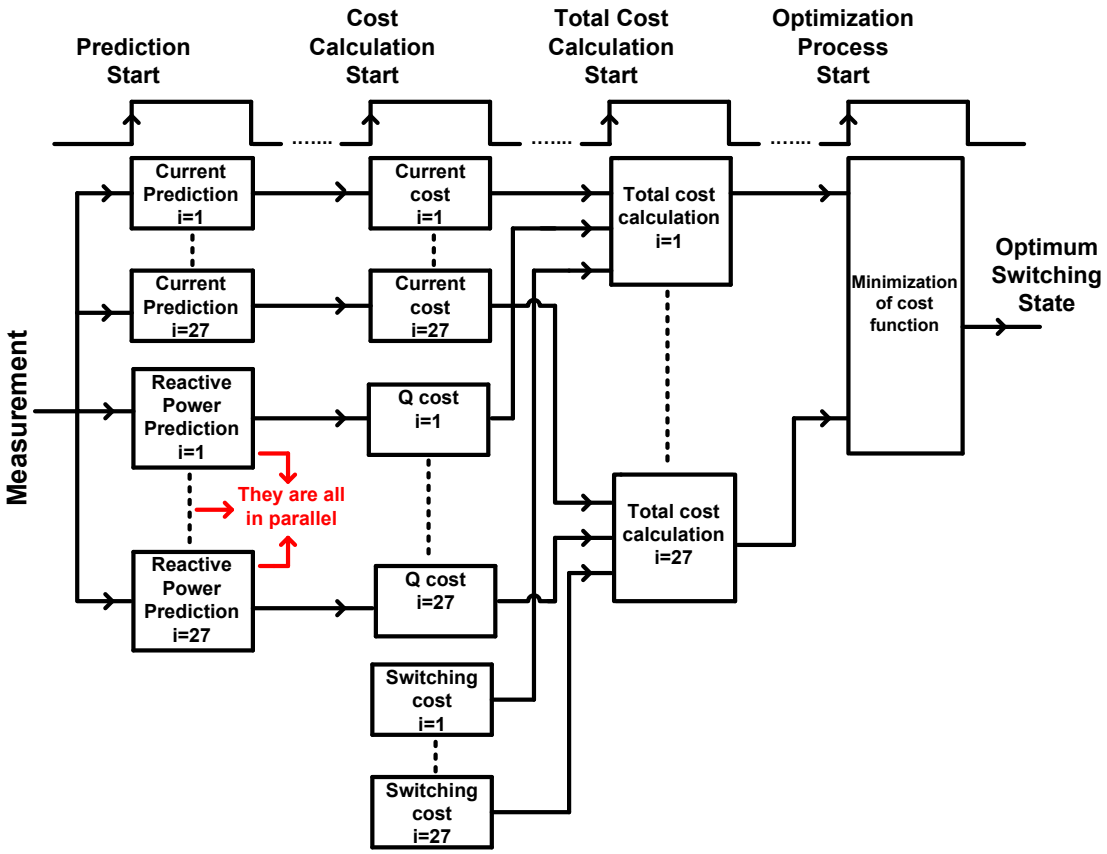


Figure 2.4: Parallel implementation of model predictive control

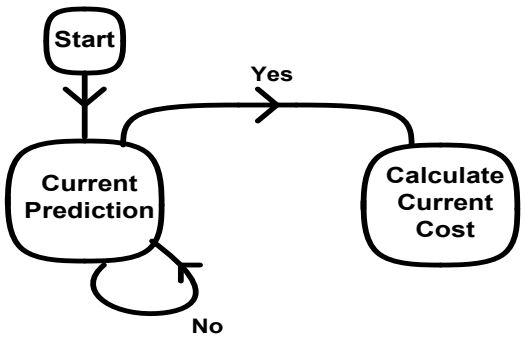


Figure 2.5: Finite state machine for current cost calculation

The current prediction is enabled when the measurements for the current step are available at the inputs. When each block finishes its task, a done signal is generated and sent to the control block. After completion of the current prediction calculations, the cost calculation blocks are enabled. When these complete, the total cost calculation starts and when this is completed the optimization process starts. Figure 2.6 shows the FPGA architecture for the predictive controller. Notice how the synchronizer block sends enable and done signals to each block to ensure proper order of execution.

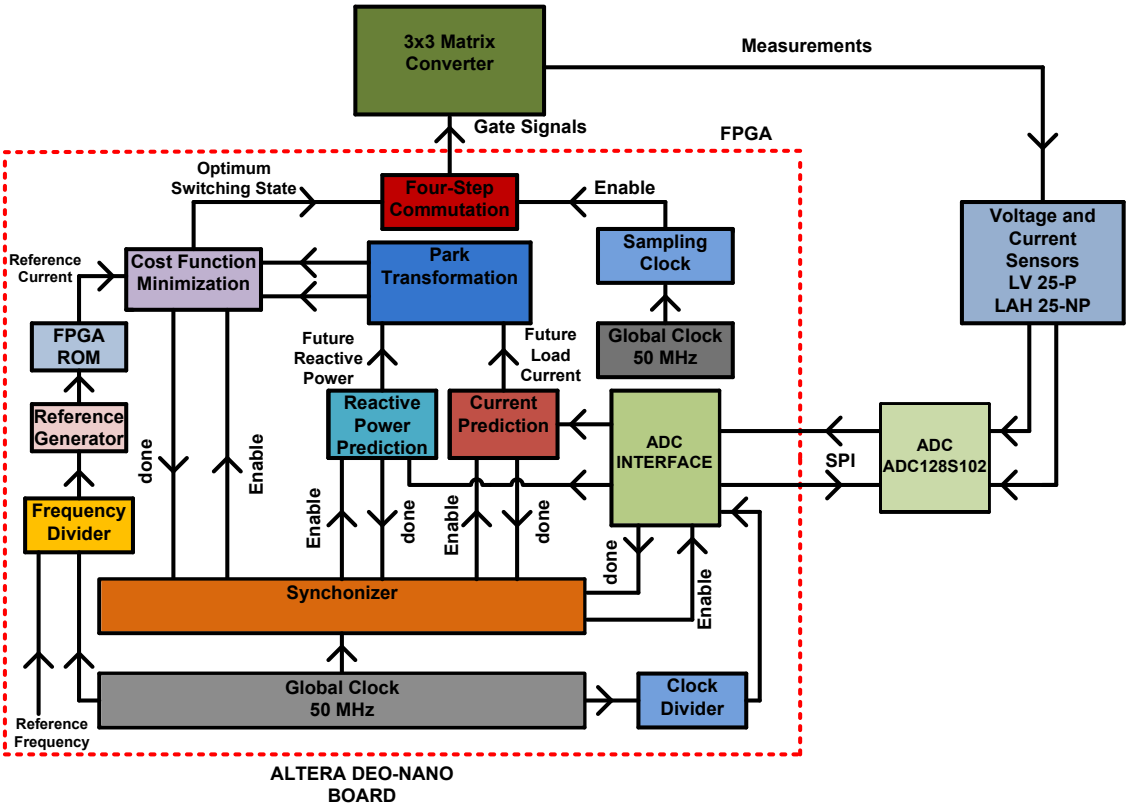


Figure 2.6: FPGA architecture for predictive controller

The model predictive controller is implemented using an Altera DEO-Nano board. The prediction and optimization steps present the largest computational burden and there is a tradeoff between calculation time and required FPGA resources, such as memory bits and logic elements. The number of memory bits and logic elements required

is directly related to the number of parallel computation blocks. To improve execution speed, the calculations are performed in parallel, but this increases demand for resources. When the sampling period is greater than the time required for control calculations, the FPGA resources can be shared between functional blocks in order to minimize the area used to implement the model predictive control method. In Figure 2.4, each current prediction sub-block calculates the future value of the output load current based on the same measurement data for different switching combination. In this way, the computation delay is decreased considerably, but larger area of the FPGA is used. For this reason, the area-time optimization needs to be considered in the controller design. In Figure 2.7, different computation architectures are shown and highest speed can be achieved when the control calculations are fully paralleled.

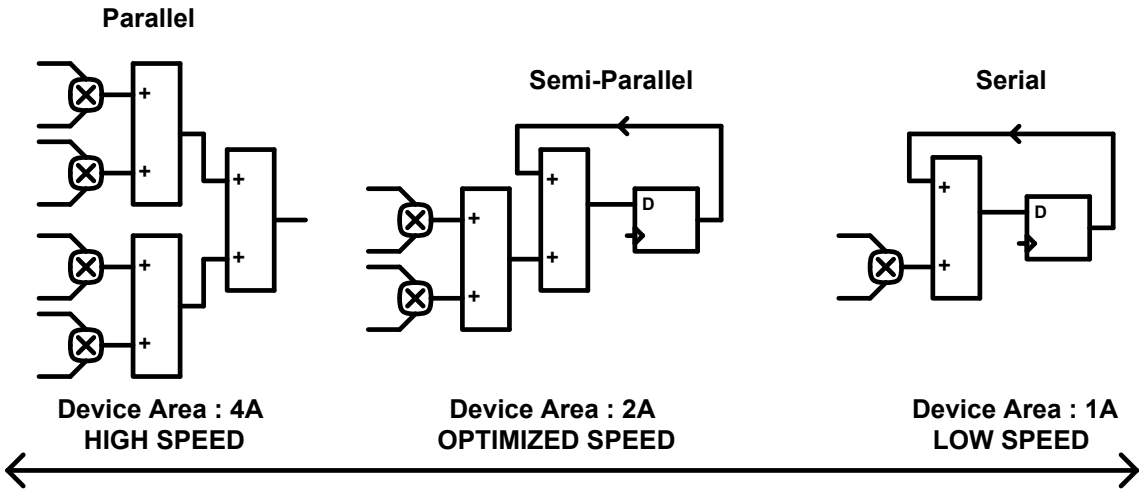


Figure 2.7: Time-Area optimization

2.5 HARDWARE PLATFORMS AND EXPERIMENTAL RESULTS

Many different subsystems have to be built and interconnected to realize a matrix converter evaluation board. The two-phase input single-phase output prototype is used to test all sub-circuits and software. Direct matrix converter topology has a complicated

commutation scheme, four-step commutation technique, and output load current direction needs to be sensed to implement the four step commutation method. Over current and voltage protections are tested using this prototype and VHDL code for interfacing between analog-to-digital (ADC) chip and FPGA board was developed. Basic schematics for the two-phase input single-phase output prototype is shown in Figure 2.8 and the hardware prototype is shown in Figure 2.9.

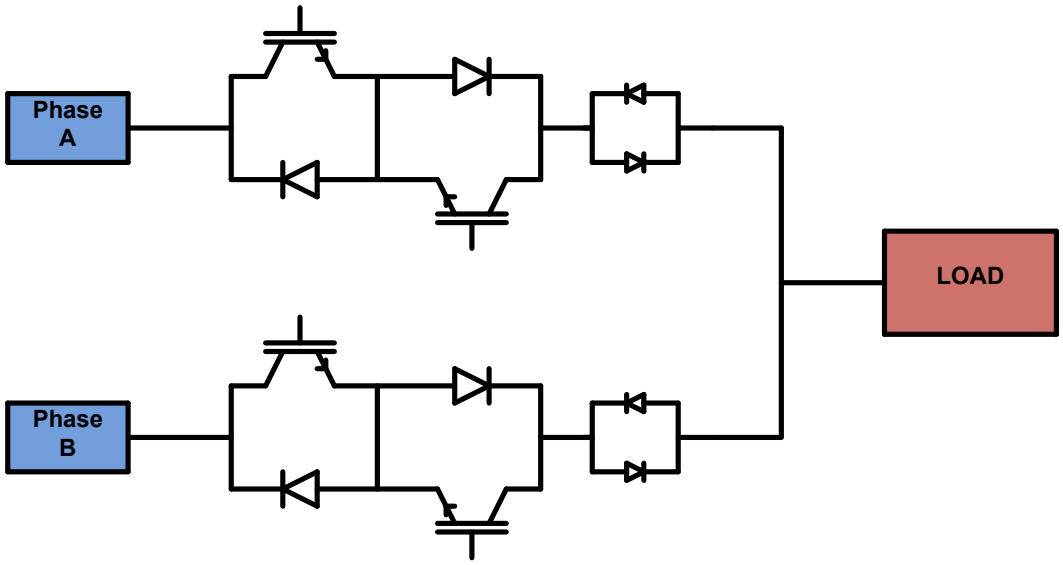


Figure 2.8: Two-phase input single-phase output topology

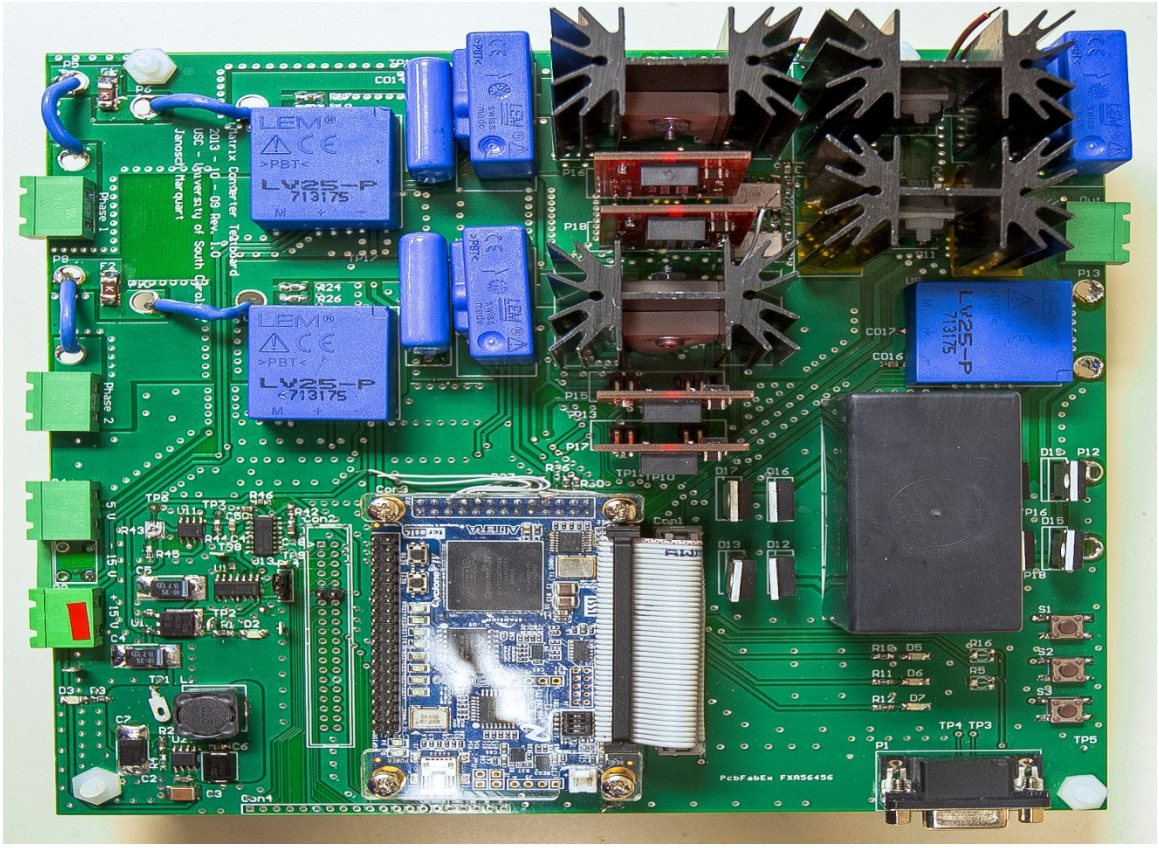


Figure 2.9: Two-phase input single-phase output topology

The matrix converter topology requires four-quadrant switches, which do not have free-wheeling diodes. For this reason, a proper commutation scheme must be implemented to prevent short circuits between input phases and interruption of the inductive load current [46], [54]. The current flowing through the switches must be actively controlled and several commutation methods for proper commutation have been reported [45]. The most common technique for commutation is the four-step commutation technique, typically implemented in FPGA using a finite state machine. It is important to accurately measure the current direction to implement the four-step commutation technique. Different ways to detect the current direction are possible for proper DMC operation [47]. For detection of output load current direction, two Schottky diodes are connected in anti-parallel in

each output phase. The voltage-drop (maximum 380 mV in amplitude) on top of the output voltage is sensed using an instrumentation amplifier, given the large DC offset. The output signal coming from the instrumentation amplifier is galvanically isolated using a high-speed gate-logic optocoupler. This signal can be directly read by the FPGA. Figure 2.10 shows the circuit used for load current sign detection using the instrumentation amplifier. Figure 2.11 shows that current direction measurement and zero crossing of the output load current is precisely detected.

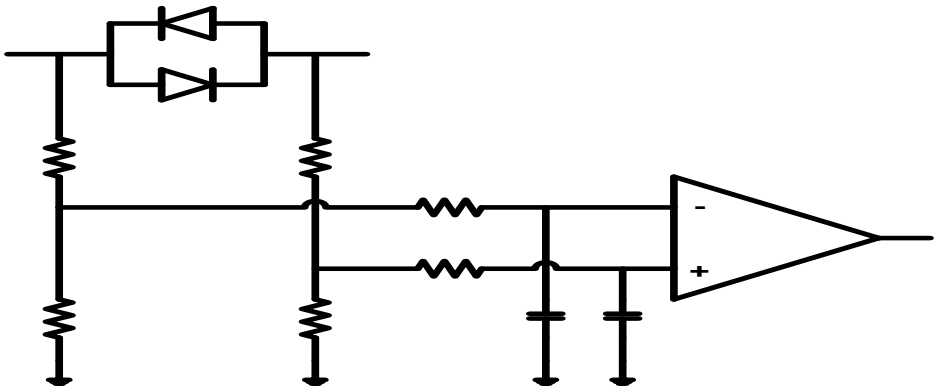
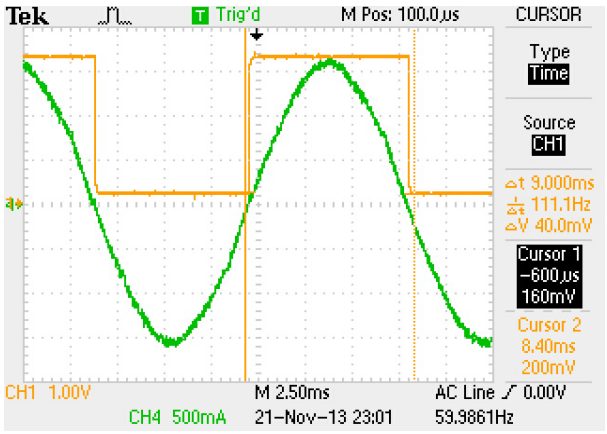
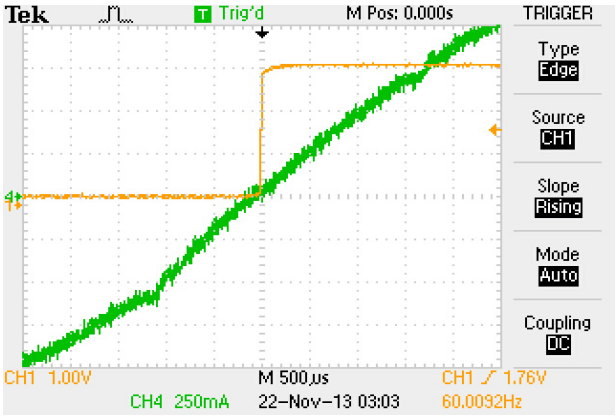


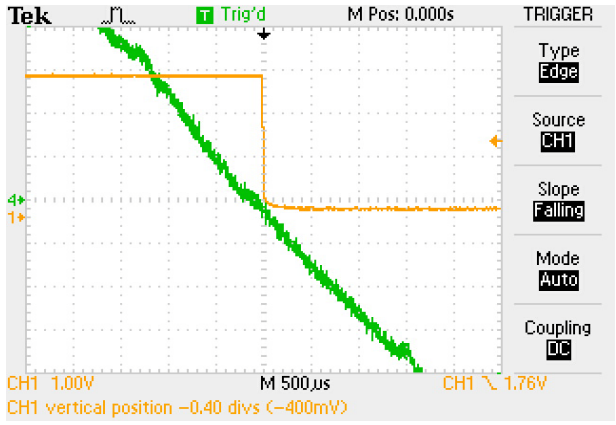
Figure 2.10: Output load current measurement circuit



a)



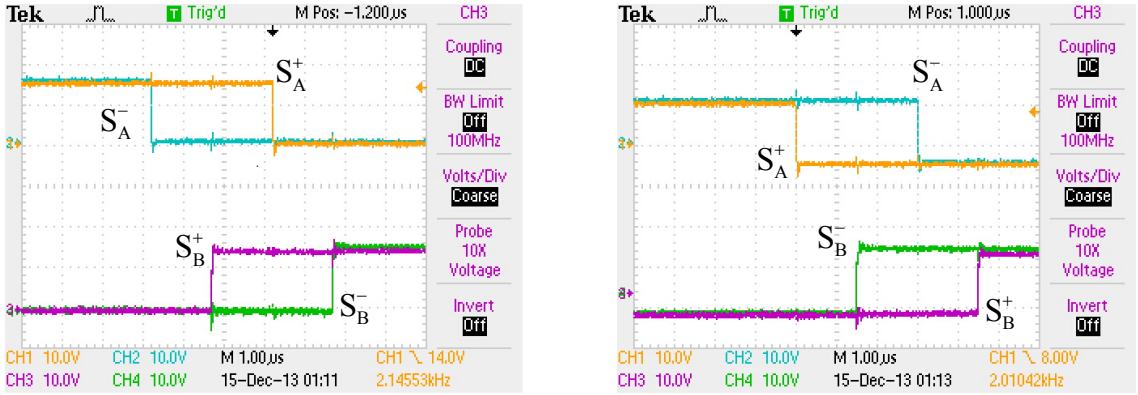
b)



c)

Figure 2.11: a) Load current direction detection b) Rising edge c) Falling edge

The delay between each subsequent step is set at TD=1.5 µs. This value is chosen based on turn-on/off characteristic of the power semiconductor devices. Gate waveforms generated from FPGA-based implementation are shown in Figure 2.12 in case of positive load current and in Figure 2.12b in case of negative load current.



a) b)

Figure 2.12: Four-step commutation a) Positive load current b) Negative load current

The source current and output load current are sensed using the LAH 25-NP current sensor from LEM. The source voltage, input filter capacitor voltage and output load voltage are sensed using LV 25-P from LEM. Since the FPGA board, Altera DEO-Nano, used to implement the control algorithm, does not have Analog-to-Digital Converter (ADC), an external ADC circuit, ADC128S102 from Texas Instruments, is used for the analog-to-digital conversion process. The external ADC chip has 8 channels and 12 bit resolution. Communication between FPGA and the external ADC chip is implemented over SPI protocol. For sinusoidal reference, the use of extrapolation methods for the reference can compensate the delay in the reference tracking. In this work, a ROM block from Altera FPGA is used to generate a look-up-table with necessary values for the sine wave. The future value of the reference current can be directly read from look-up-table. RTL for reference generation is shown in Figure 2.13 and simulation results for reference generation block is presented in Figure 2.14. ModelSim Altera is used to simulate the testbench code.

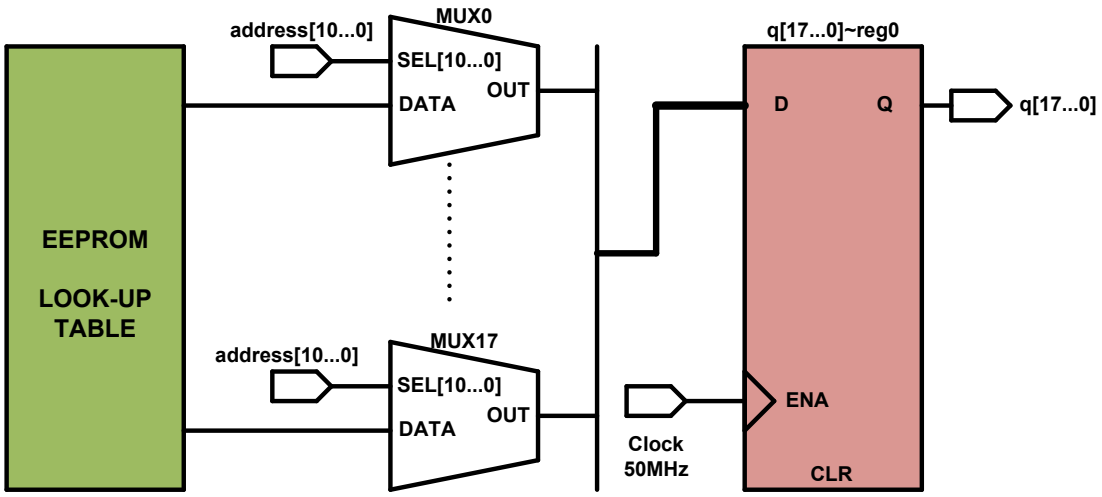


Figure 2.13: Register Transfer Level (RTL) for reference generation

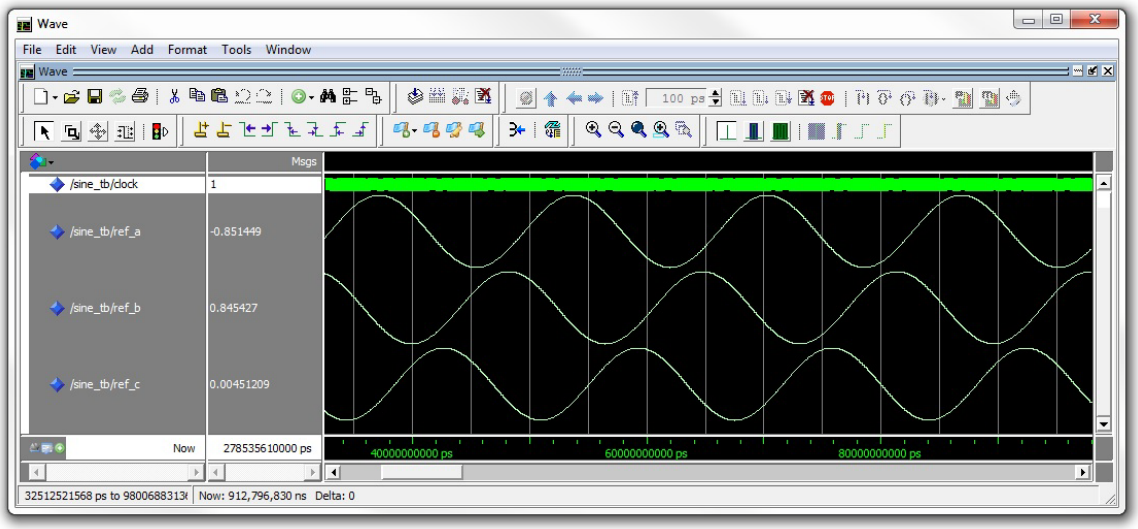


Figure 2.14: Reference generation using ROM block

To verify the performance of the parallel implementation method, a 1.6 kW direct matrix converter prototype was built. The IGBTs used are IKW40N120T2 from Infineon Technologies. A serial UART connection is added to the prototype to communicate with a host PC and a clamp circuit is used for protection. The experimental setup is shown in Figure 2.15. Currents and voltages are measured using Tektronix TDS 2014B

oscilloscope and LeCroy DA1855A differential amplifier is used to measure output load voltage. The three-phase input voltage is at 60 Hz.

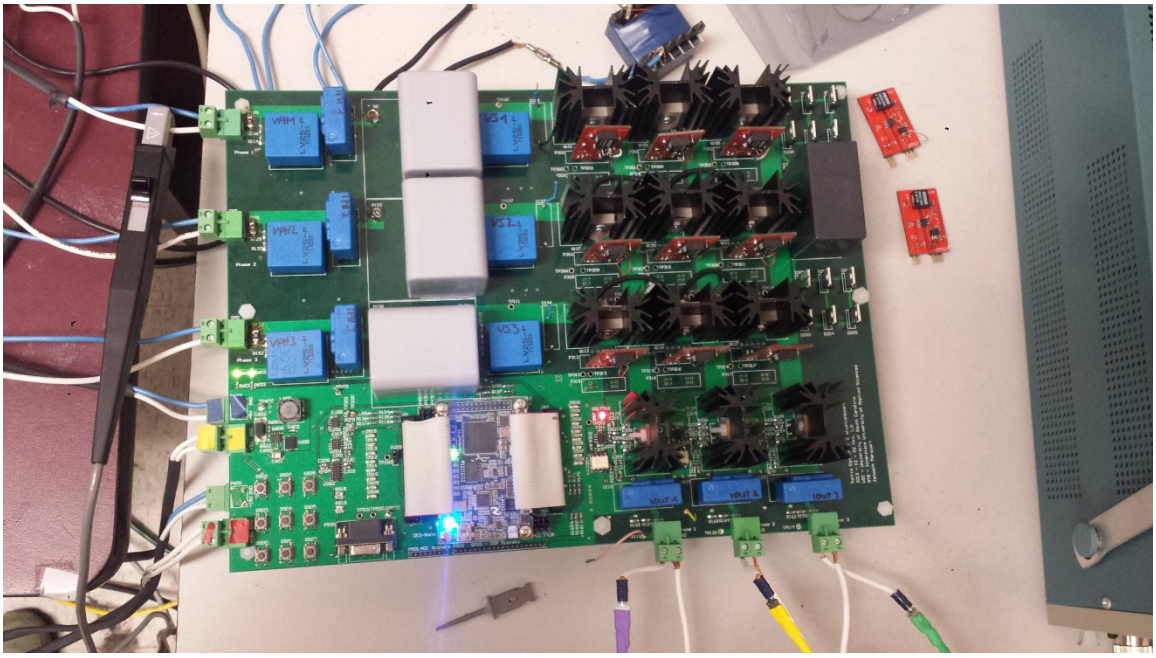
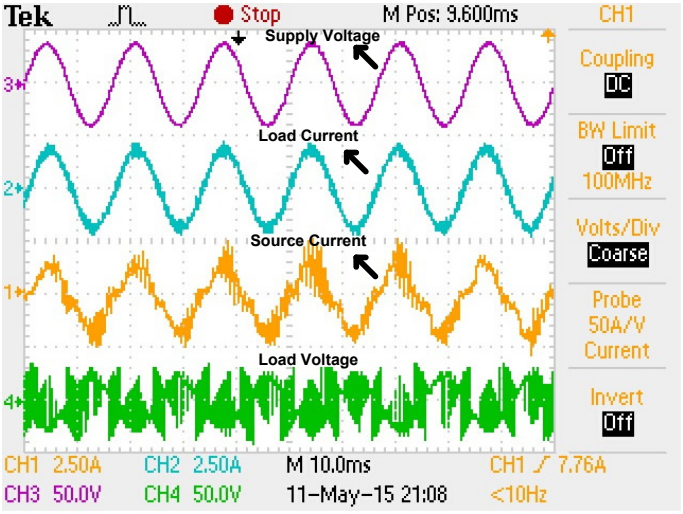
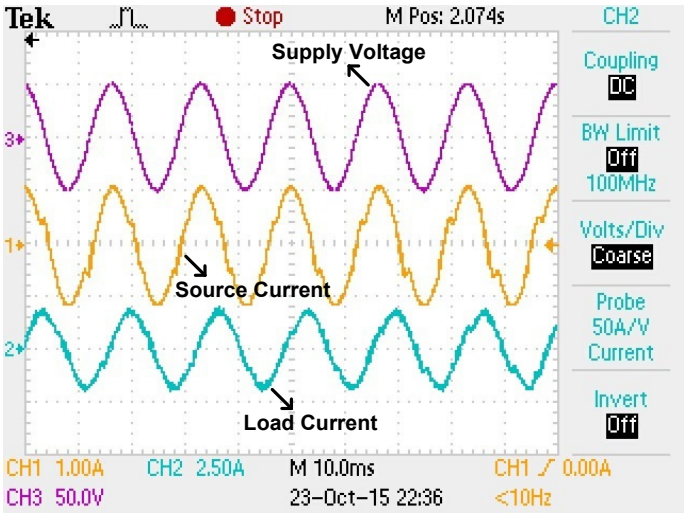


Figure 2.15: Direct matrix converter prototype

Figure 2.16 shows experimental results without reactive power control, B=0, AND with reactive power control, B=0.042. Load voltage waveform is the voltage across both the load resistor and load inductor and consequently it is a chopped waveform at the switching frequency. Figure 2.16 shows that source current is less distorted for the case of non-zero B. The sampling time is 16 µs. Output load current THD is 8.67% and source current THD is 12.43% in case of 30 Hz load current reference, see Figure 2.17.b and c. Figure 2.18 shows that load current THD is 15.14% and source current THD 18.33% in case of 120 Hz load current frequency. The effect of weighting factors is important in model predictive control method. Load current THD, source current THD and average switching frequency are tabulated in Table 2.1. Effects of the weighting factors are investigated for the case of load current frequency equal to 30 Hz.



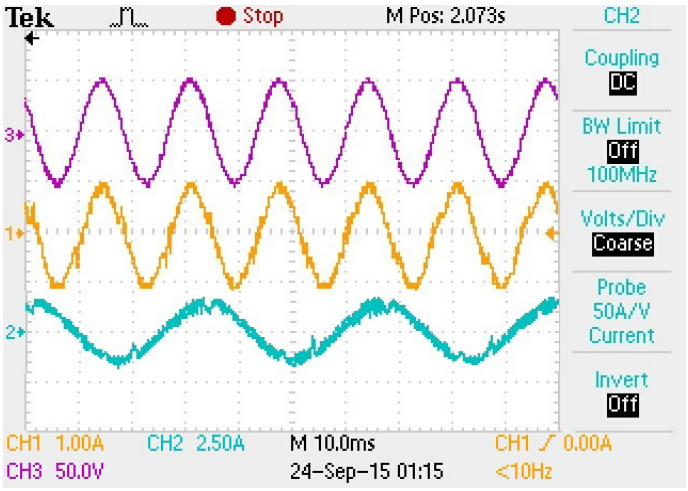
a)



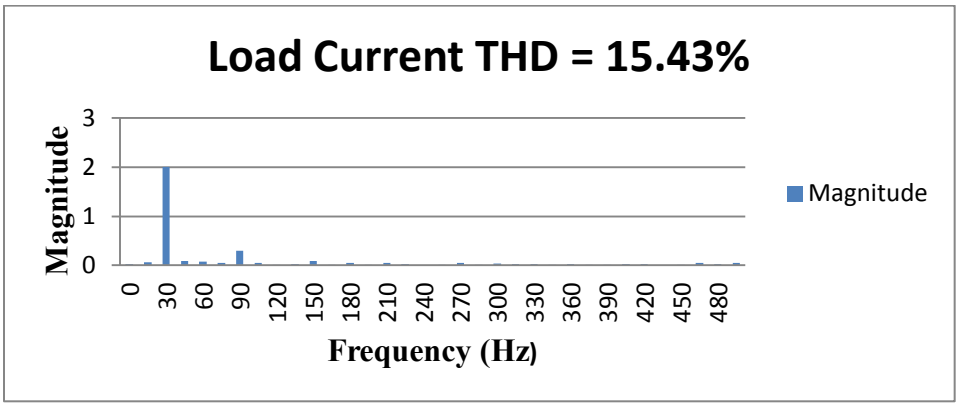
b)

Figure 2.16: Experimental results in case of 60 Hz reference a) Experimental waveforms without reactive power control b) Experimental waveforms with reactive power control

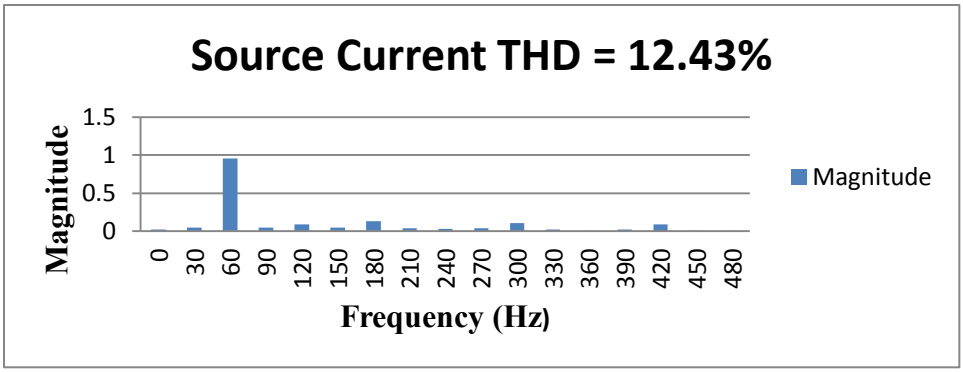
The results show that increasing values of B and C improve the corresponding control objectives at the cost of increased load current THD. However, good compromise values can be found, as shown by the experimental results.



a)

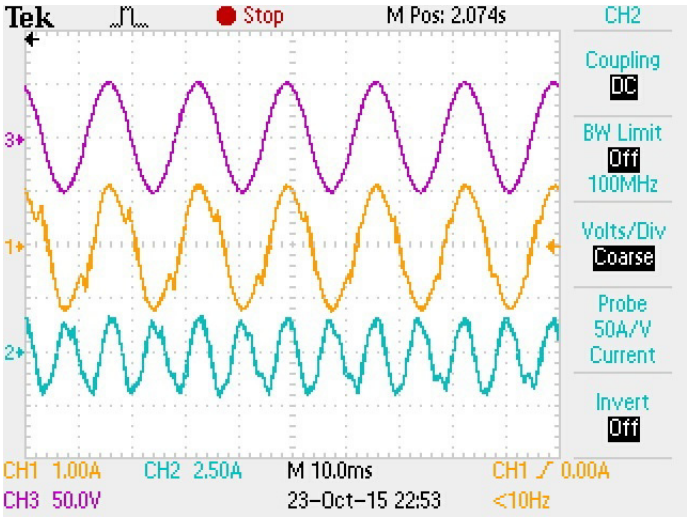


b)

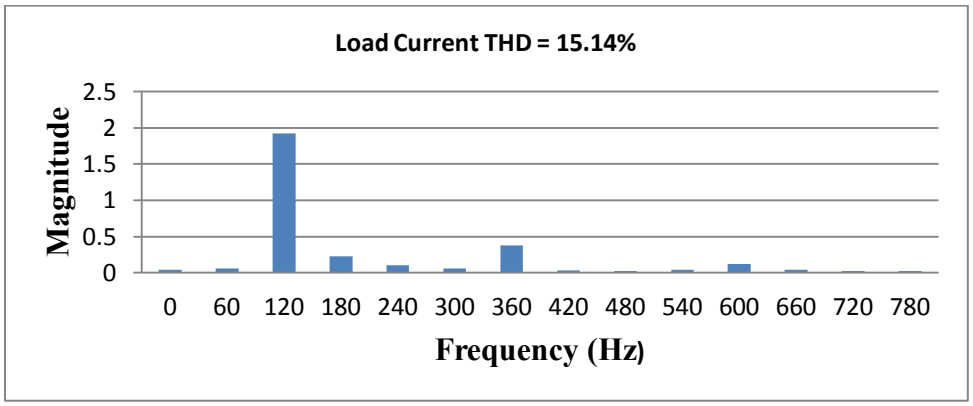


c)

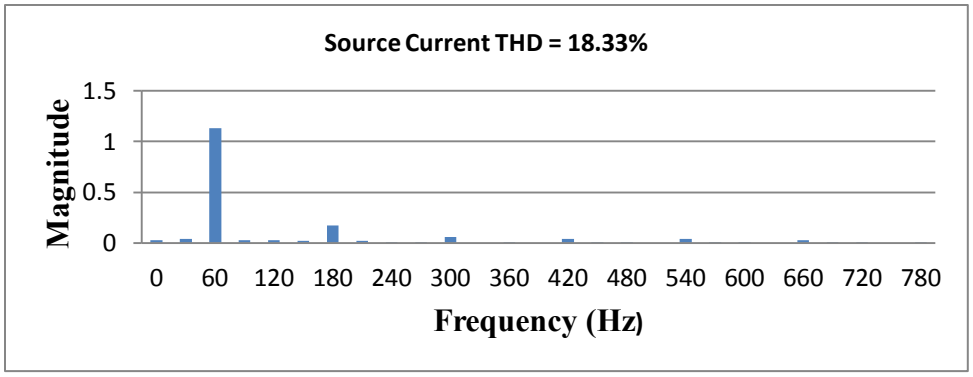
Figure 2.17: Experimental results in case of 30 Hz reference a) Experimental waveforms b) Load current frequency spectrum c) Source current frequency spectrum



a)



b)



c)

Figure 2.18: Experimental results in case of 120 Hz reference a) Experimental waveforms b) Load current frequency spectrum c) Source current frequency spectrum

In the cost function equation (2.26), weighting factor A is 1. THD values and average switching frequency are listed for different values for B and C.

Table 2.1: Effect of weighting factors

A	B	C	Load Current THD	Source Current THD	Average Frequency
1	0	0	6.32%	48.12%	13.12 kHz
1	0.0012	0.002	8.13%	21.57%	11.23 kHz
1	0.0068	0.002	8.50%	11.93%	12.79 kHz
1	0.0068	0.047	8.67%	12.43%	10.48 kHz
1	0.015	0.047	10.16%	12.68%	11.12 kHz
1	0.030	0.06	12.77%	12.65%	9.2 kHz
1	0.12	0.06	19.14%	28.78%	9.65 kHz

In order to evaluate the dynamic performance of the predictive control method, the frequency of the load current is changed in a step-wise fashion from 60 Hz to 30 Hz and the resulting step response is shown in Figure 2.19. According to experimental results, predictive control technique works well under both steady-state and transient conditions. Reference tracking is quite good and FPGA-based implementation provide good dynamic response.

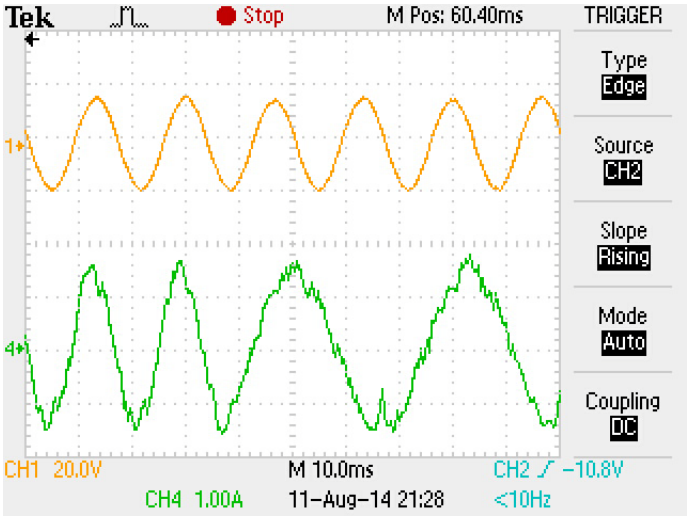


Figure 2.19: Dynamic response of FPGA-based model predictive controller

2.6 DISCUSSION AND CONCLUSION

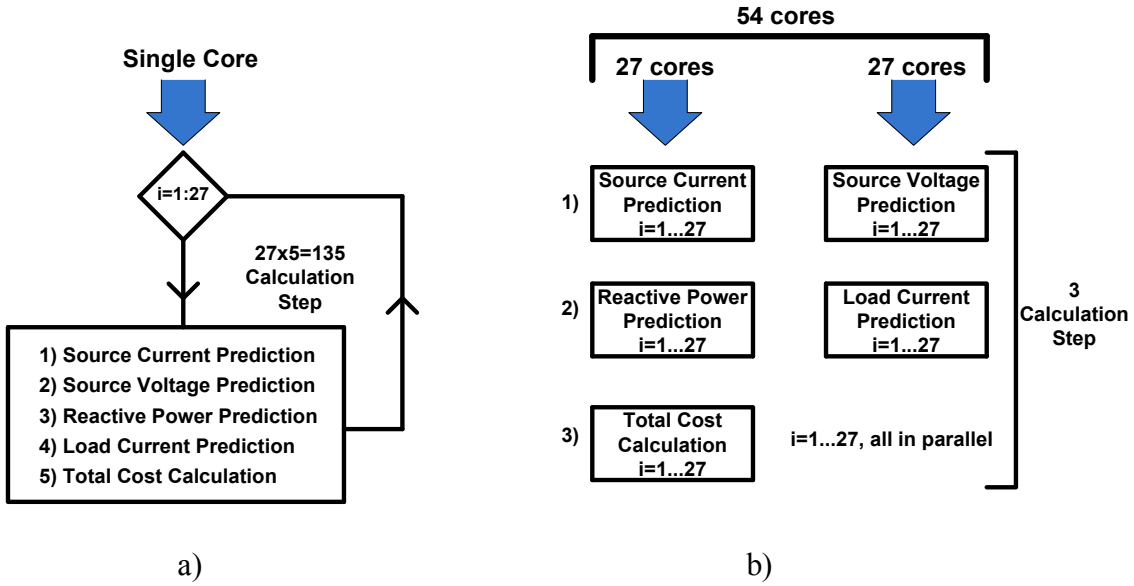
This chapter presented FPGA-based model predictive control method for direct matrix converter. The proposed real-time implementation technique eliminates the need for DSP, reduces complexity of hardware implementation and shortens computation time by exploiting parallelization in the FPGA. Control algorithm and tasks are performed in the FPGA and the advantages of implementing digital controllers using FPGA are demonstrated. In the predictive control method, increasing the number of control objectives increases the computation burden significantly. In FPGA-based implementation, execution time can be kept almost the same even if more control objectives need to be controlled. FPGA resources and execution time are tabulated in Table 2.2 in case of different numbers of control objectives.

Table 2.2: FPGA resources and execution time vs number of control objectives

	Combinational Functions	**Dedicated Logic Register**	**Memory Bits**	**Execution Time**
One Objective - Load current	3875/22320 (17 %)	1617/22320 (7 %)	110592/608256 (18%)	1.72 µs
Two Objective - Load current - Switching Frequency	4390/22320 (20 %)	1691/22320 (8 %)	110592/608256 (18%)	1.89 µs
Two Objective - Load current - Switching Frequency - Reactive Power	21787/22320 (98 %)	5500/22320 (25 %)	120317/608256 (19%)	2.12 µs

It can be concluded that, if control calculations are fully paralleled using an FPGA, significant extra execution time is not required in the case of multiple objectives, but only a small amount of extra time is required since source current and source voltage need to be calculated for future reactive power calculation. As shown in Table 2.2, execution time does not change significantly as long as FPGA resources are used to parallelize calculations. To better understand the benefit of using FPGA devices, comparison between different digital control platforms is shown in Table 2.3.

If a serial-computing device is used for MPC implementation, 135 calculation steps are required, but, on the other hand, only 3 calculation steps are required for FPGA implementation in case of fully paralleling, see Figure 2.20. In order to achieve the same execution speed with a serial-computing device, at least 45 times higher clock speed is required compared to the clock speed of FPGA used in this work (50 MHz), which corresponds to 2250 MHz. Digital control platforms having this capability are more expensive compared to a 50 MHz FPGA device. For this reason, using FPGA is the lowest-cost solution to reduce the execution time.



a) b)

Figure 2.20: Calculation loop comparison a) MPC implementation by using serial-computing device b)MPC implementation by fully paralleling technique

According to Table 2.3, using multi-core DPSs with high clock speed can be a solution to reduce execution time but it is not cost effective. The other important aspect is that fixed-point devices, such as FPGAs, work faster than floating-point devices, such as DSPs, because of flexibility in the number of bits used for representing the numbers in calculations. Working with fixed-point numbers in FPGAs is not straightforward

compared to floating-point numbers. On the other hand, fixed-point implementation of algorithms yields considerable improvement in computation time at the cost of reduced accuracy of the variables and increased programming effort. The development of fixed-point software requires proper scaling of variables to prevent overflows while maintaining the accuracy. Fewer bits can be used to represent numbers in calculations resulting in high execution speed. This also leads to a reduction in accuracy and resolution. However, model predictive control approach has a discrete solution set, which means that the control signal is not continuous, so accuracy is less critical.

Table 2.3: Digital control platforms comparison

Digital Controller	**Controller Type**	**Arithmetic**	**Clock Speed**	**Calculation Step**	**Performance (Clock Speed*Core)/ 1 clock cycle**
TMS320F2812	DSP-Single Core	Fixed-Point	150 MHz	135	150 MMACS
TMS320F2837	MCU-Dual Core	Floating-Point	200 MHz	68	400 MMACS
TMS320C6678	DSP- 8 Core	Fixed-Point	1 GHz	17	8192 MMACS
dSPACE	R&D Controller	Floating-Point	230 MHz	135	230 MMACS
Altera Cyclone IV	FPGA	Fixed-Point	50 MHz	3	2700 MMACS
Xilinx Spartan	FPGA	Fixed-Point	200 MHz	3	10800 MMACS

Table 2.4 shows execution times for important calculation steps in the MPC implementation. According to results, the optimization and decision making task takes longer time compared to other calculation tasks. The implementation starts with format conversion of ADC values. The ADC values need to be converted to signed format since ADC values from ADC chip are 12 bits unsigned format. Resolution adjustment is done during the control calculations and total execution time for this implementation is 2.12 μs, which is quite small amount of time for MPC implementation.

Table 2.4: Execution time for calculation tasks

Calculation Tasks	Clock Cycle	Execution Time
Wait for Start	1 Cycle	0.02 µs
Format conversion of ADC values	4 Cycles	0.08 µs
- Source current prediction - Source voltage prediction	11 Cycles	0.22 µs
- Load current prediction - Reactive power prediction	15 Cycles	0.30 µs
Resolution adjustment	3 Cycles	0.06 µs
Park transformation	7 Cycles	0.14 µs
- Current cost calculation - Reactive power cost calculation - Switching cost calculation	9 Cycles	0.18 µs
Total cost calculation	19 Cycles	0.38 µs
Optimization and decision making	37 Cycles	0.74 µs
TOTAL	106 Cycles	2.12 µs

CHAPTER 3

MODEL PREDICTIVE CONTROL BASED ON SWITCHING STATE ELIMINATION

Model Predictive Control (MPC) is an optimal control approach that uses the system model to predict future behavior of the control objectives and evaluate the cost function to determine the optimum control action. The control action which minimizes the user-defined cost function is selected and applied to the converter for the next time interval [39]. Different control objectives, such as output load current control, minimization of instantaneous reactive power and reduction of switching frequency, can be introduced in the cost function and controlled simultaneously by solving a multi-objective optimization problem. FCS-MPC is a good strategy for controlling power converters, but adjusting the weights used in the multi-objective cost function is problematic since there is no formal procedure to select them in order to obtain good control performance. In the conventional approach, the controller calculates the predicted cost function value for the next control interval for each possible switching state and the optimum switching state is the one that minimizes the cost function. When the cost function has more than one control objectives, offline tuning is necessary to adjust control goal weightings. As the tuning of weightings is cumbersome, avoiding this nontrivial process is an interesting option. In this work, model predictive control based on

switching state elimination is proposed that does not require weighting factors. The direct matrix converter is used as a case study to assess the feasibility of the proposed control scheme.

3.1 CONVENTIONAL MODEL PREDICTIVE CONTROL

In this chapter, to illustrate how conventional model predictive control works, two different cases with different control objectives and cost functions will be considered. In the first case, the conventional model predictive control has three objectives: to output load current, to minimize instantaneous input reactive power and to reduce average switching frequency [41]. The cost function is defined as

$$g = \left(\left|i^{*}_{o\alpha} - i_{o\alpha}\right| + \left|i^{*}_{o\beta} - i_{o\beta}\right|\right) + A\left|Q\right| + B\left|S(k+1) - S(k)\right| \tag{3.1}$$

Q is reactive power and superscript "*" indicates reference value. Constants A and B are the weighting factors that need to be adjusted empirically [40], [52]. These weighting factors affect system performance significantly and depend on system model and power level. The $\left|S(k+1) - S(k)\right|$ term is responsible for reducing switching frequency. The conventional model predictive control scheme for first case is shown in Figure. 3.1. According to the conventional approach, the cost function defined in (3.1) is calculated for each of the 27 switching states and the one which provides the minimum cost is selected and applied to the matrix converter. The process to derive prediction equations for load current, source current and reactive power has been explained in the previous chapter.

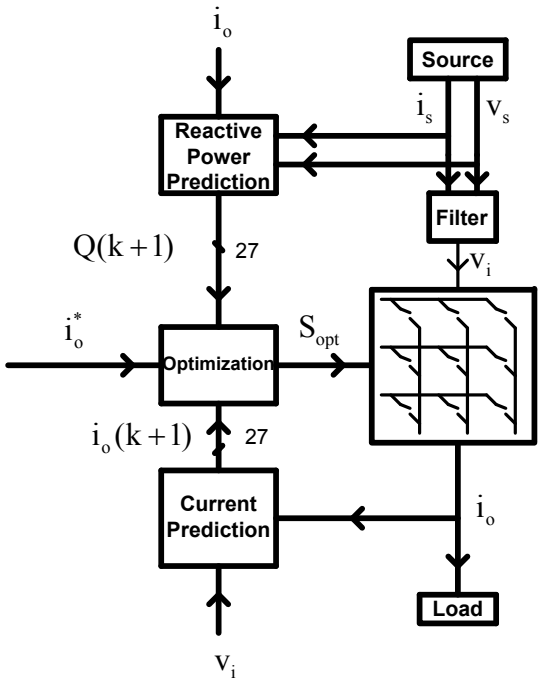


Figure 3.1: Conventional model predictive control scheme for first case

In the second case, the MPC control objectives are load current and source current control. Therefore, current error terms for both of them are introduced in the cost function [42]-[44]. The cost function is defined as

$$g = \left(\left|i_{o\alpha}^* - i_{o\alpha}\right| + \left|i_{o\beta}^* - i_{o\beta}\right|\right) + D\left(\left|i_{s\alpha}^* - i_{s\alpha}\right| + \left|i_{s\beta}^* - i_{s\beta}\right|\right) \tag{3.2}$$

$i_{s\alpha}$ and $i_{s\beta}$ are the real and imaginary component of the three-phase source current. A method for the determination of source current reference is reported in [43]. The constant D is the weighting factor. The conventional control scheme for the second case is shown in Figure 3.3. The source current is predicted using input filter model and output current is predicted using load model. The cost function, defined in (3.2), is evaluated for each of the 27 switching state and the best switching combination is determined.

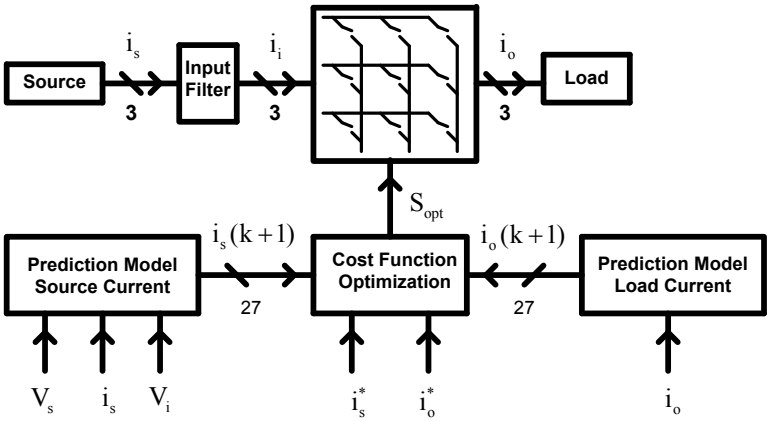


Figure 3.2: Conventional model predictive control scheme for second case

3.2 SWITCHING STATE ELIMINATION TECHNIQUE

Different control objectives can be controlled simultaneously by introducing specific dynamic and static constraints for each goal instead of solving a single multi-objective optimization problem [58]. The main idea of the proposed algorithm is that a control sub-optimization problem can be defined depending on control constraints and elimination conditions. This approach defines a rank order of importance for control objectives.

In the first case, three control goals are considered: load current control, minimization of instantaneous reactive power and reduction of switching frequency. The three sub-optimization problems are defined as

$$f_1 = \sqrt{\left|i^*_{o\alpha}(k+1) - i_{o\alpha}(k+1)\right|^2 + \left|i^*_{o\beta}(k+1) - i_{o\beta}(k+1)\right|^2} \tag{3.3}$$

$$f_2 = \left|\frac{Q(k+1)}{\sqrt{P(k+1)^2 + Q(k+1)^2}}\right| \tag{3.4}$$

$$f_3 = \left|S(k+1) - S(k)\right| \tag{3.5}$$

Figure 3.3 shows a flowchart of the switching state elimination algorithm. T_1, T_2 and T_3 are sub-finite solution sets for load current, reactive power and reduction of switching frequency, respectively. T_1 contains all possible switching states and it is defined as

$$T_1 = \left(S_1, S_2, S_3, \ldots, S_{27}\right) \tag{3.6}$$

Sub-finite sets T_2 and T_3 are not fixed since they are the result of the switching state elimination process. For example, Figure 3.4 shows how to calculate T_2.

As mentioned above, a rank order of importance is defined by the proposed method. For the first case, load current has the highest importance and reduction of switching frequency has the least importance. Algorithm flow chart is shown in Figure 3.3 and control constraints, C_1 and C_2, are used for the elimination process. Since load current is the most important objective, the finite solution set T_1 is reduced to set T_2 by imposing the constraint $f_1 \le C_1$. Only the m switching states in T_2 will be candidate solutions for the reactive power control problem. The same elimination procedure is applied to the reactive power control problem and permissible-solution set is further reduced to set T_3, consisting of n states($n \le m$) that also meet the condition $f_2 \le C_2$.

The last step of this algorithm is performing an exhaustive search for switching frequency reduction cost function using the n-state sub-finite set to determine the optimum switching state to be applied to the converter. Basically, finite solution set can be reduced step-by-step using the specific criteria to eliminate switching states that violate a certain conditions.

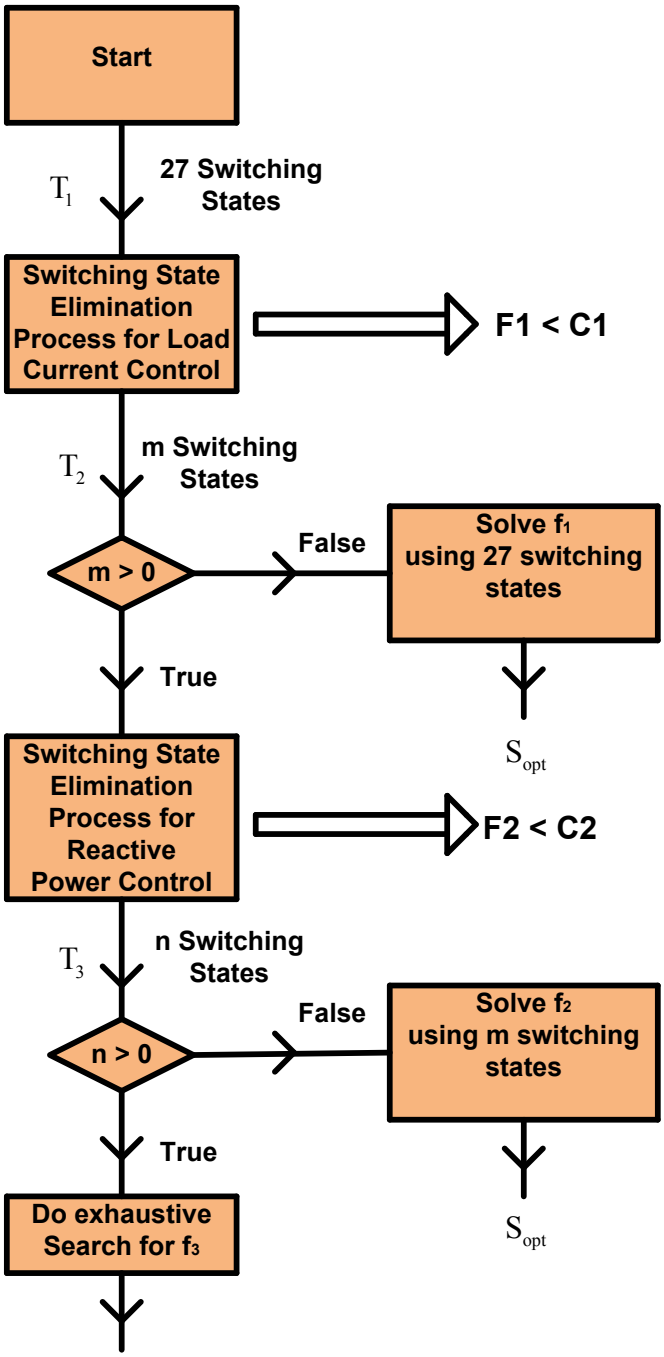


Figure 3.3: Switching state elimination process

Table 3.1: Sub-finite solution set selection

T_2	T_3	
$\neq 0$	$\neq 0$	Satisfy first two constraints and select the best state for the reduction of the switching frequency problem.
$\neq 0$	$= 0$	Satisfy first constraint and select the best state for the reactive power minimization problem. Sacrifice the reduction of switching frequency.
$= 0$	$= 0$	Do not meet the first constraint. Select the best state for the load current control problem. Sacrifice the reactive power minimization and the reduction of the switching frequency.

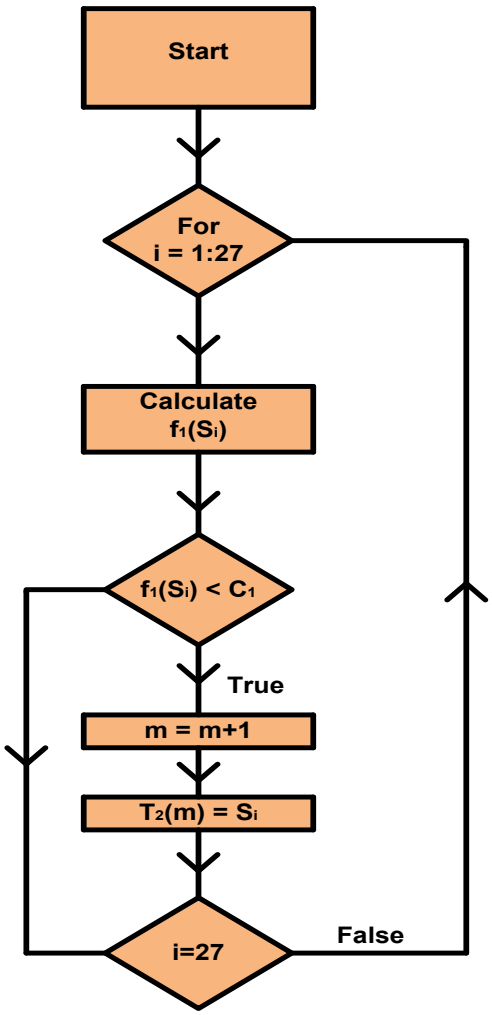


Figure 3.4: Elimination process for load current control

It may happen that no switching state satisfies one of the constraint conditions. For example, load current error is very large during a large signal transition, so that none the possible 27 switching states meets condition $f_1 < C_1$ and m=0. In this case, sub-optimization problem f_1, which is a single-optimization-problem, is solved in order to determine the optimum control action. This is the adaptive part of the proposed algorithm which allows control of the load current in a worst-case situation. The rationale is that, reactive power control and reduction of switching frequency can be sacrificed to obtain good load current tracking. It may also happen that, during the state elimination for reactive power, no switching state meets condition $f_2 < C_2$. The result is that reduction of switching frequency is sacrificed to decrease the instantaneous reactive power. Load current and reference current are defined in the α-β frame as

$$i_o = i_{o\alpha} + j i_{o\beta} \tag{3.7}$$

$$i_o^* = i_{o\alpha}^* + j i_{o\beta}^* \tag{3.8}$$

The current error term which is the error between measurement and reference is given (3.9).

$$i_o^e = \left(i_{o\alpha}^* - i_{o\alpha}\right) + j\left(i_{o\beta}^* - i_{o\beta}\right) = i_{o\alpha}^e + j i_{o\beta}^e \tag{3.9}$$

The vector representation of current errors is shown in Figure 3.5. In order to obtain good load current tracking, current error term must be kept small. Control constraint for load current is given in (3.10).

$$C_1 = \sqrt{(\sigma i_o^*)} \tag{3.10}$$

In order to determine C_1, a range of values for load current relative error is chosen. The minimum error tolerance is 1.5% and maximum error tolerance is 4.5%, so that normalized error can be chosen in the range

$$0.015 \le \sigma \le 0.045 \tag{3.11}$$

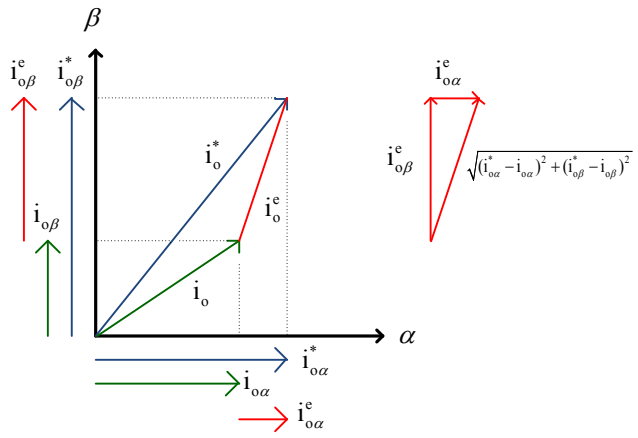


Figure 3.5: Vector representation of current error term

When normalized current error is chosen in this range, good load current tracking is guaranteed, since error between reference and measurement is kept low. Note that the parameter σ has a clear physical interpretation in terms of relative current error, whereas the weightings constants A and B used in the conventional FCS-MPC do not. Elimination condition for load current control can be defined as

$$\sqrt{\left|i^*_{o\alpha}(k+1)-i_{o\alpha}(k+1)\right|^2+\left|i^*_{o\beta}(k+1)-i_{o\beta}(k+1)\right|^2} < \sqrt{(\sigma i^*_{o\alpha})^2+(\sigma i^*_{o\beta})} \tag{3.12}$$

Reactive power control is important for improving power quality of power converter system. In order to reduce the reactive power of DMC, control constraint can be introduced. C_2 is defined as the upper bound on the ratio between reactive power and apparent power. Control constraint C_2 can be chosen in the range,

$$0.05 \le C_2 \le 0.09 \tag{3.13}$$

When C_2 is chosen within this range, a good power factor is obtained and power quality is improved significantly. The elimination condition for reactive power control is defined as (3.14).

$$\left| \frac{Q(k+1)}{\sqrt{Q(k+1)^2 + P(k+1)^2}} \right| < C_2 \tag{3.14}$$

For the second case, output load current and source current are the control objectives of the switching state elimination and load current control has the highest priority. Switching sate elimination strategy for this case is shown in Figure 3.6. Since there are only two control objectives, after sub-finite solution set is reduced for load current, an exhaustive search is done for source current control problem. Sub-optimization problem for source current control is defined as (3.15).

$$f_4 = \left| i^*_{s\alpha}(k+1) - i_{s\alpha}(k+1) \right| + \left| i^*_{s\beta}(k+1) - i_{s\beta}(k+1) \right| \tag{3.15}$$

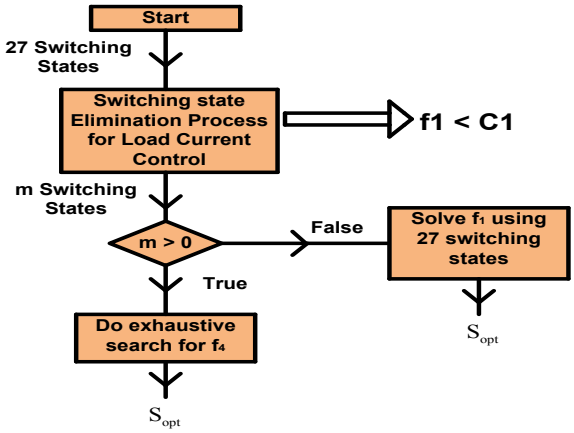


Figure 3.6: Algorithm flow chart for proposed method for second case

3.3 SIMULATION RESULTS

The proposed method was simulated for the two cases. Simulations were carried out using MATLAB/Simulink. The simulation parameters for the first case are tabulated in Table 3.2.

Table 3.2: Simulation parameters for first case

Simulation Parameters	**Values**
Supply Voltage	110 V rms/60 Hz
RL Load	10 Ω/20 mH
σ	0.015
C_2	0.05
Filter resistor	0.5 Ω
Filter inductor	420 µH
Filter Capacitor	33 µF
Sampling Period	10 µs

For the first case, output load current, source current and output load voltage waveforms are shown in Figure 3.7 in case of load current reference at 45 Hz. Figure 3.7 shows that switching state elimination technique provides good reference tracking and good power quality.

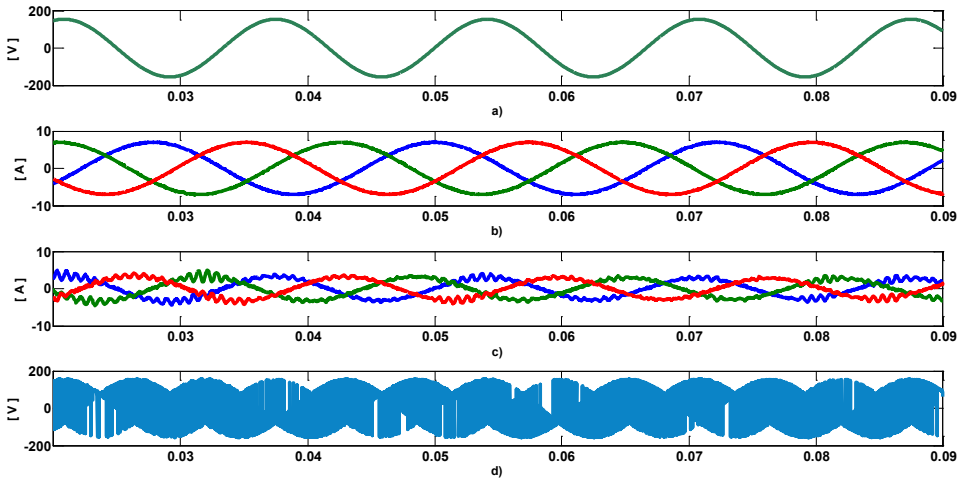


Figure 3.7: Simulation results for Case 1 (45 Hz load current reference) a) Supply voltage b) Load current c) Supply current d) Output load voltage

The spectral content of load current and source current is shown in Figure 3.8 and Figure 3.9, respectively. According to FFT results, load current THD is 0.98% and source current THD is 14.22%. These values of THD are quite good for power conversion systems. Figure 3.10 shows simulation results for the case of 90 Hz load current reference. Figures 3.11 and 3.12 show the spectral content of the load and source currents, which are very similar to the 45Hz case of Figures 3.8 and 3.9.

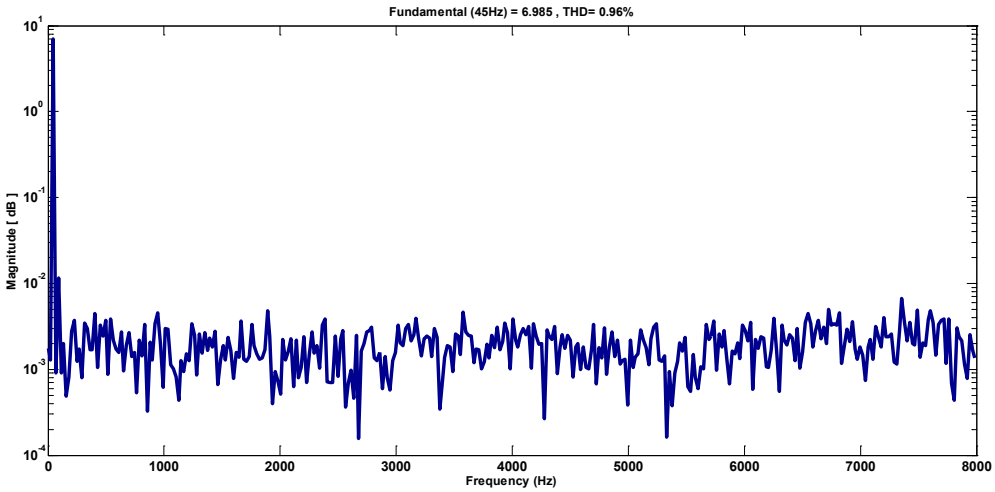


Figure 3.8: Frequency spectrum of load current (Case 1 and 45 Hz load current reference)

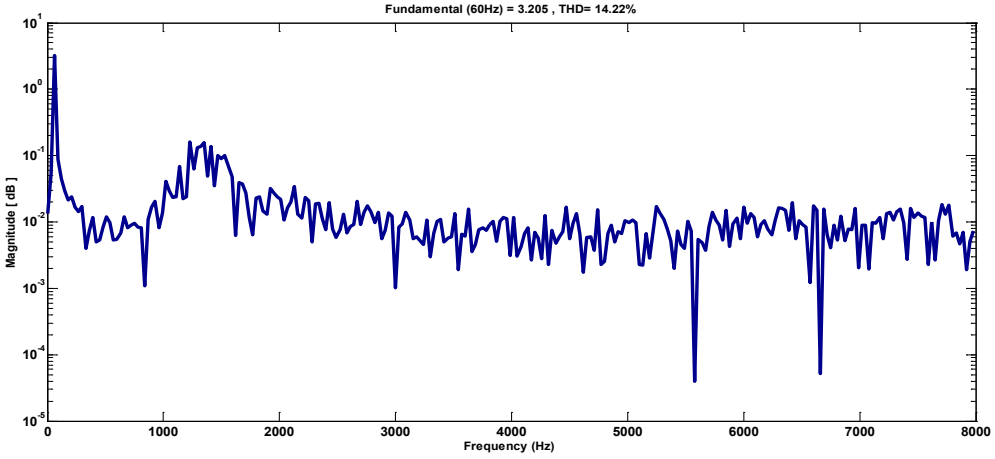


Figure 3.9: Frequency spectrum of source current (Case 1 and 45 Hz load current reference)

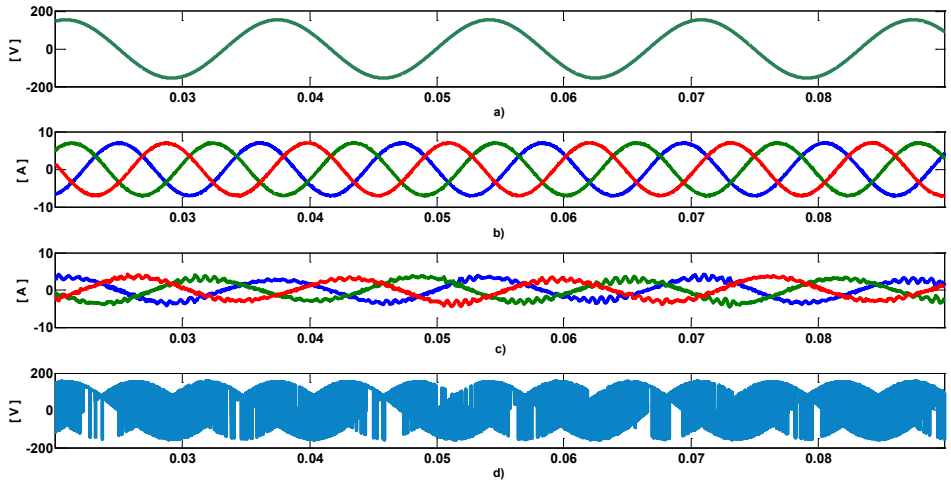


Figure 3.10: Simulation results for Case 1 (90 Hz load current reference) a) Supply voltage b) Load current c) Supply current d) Output load voltage

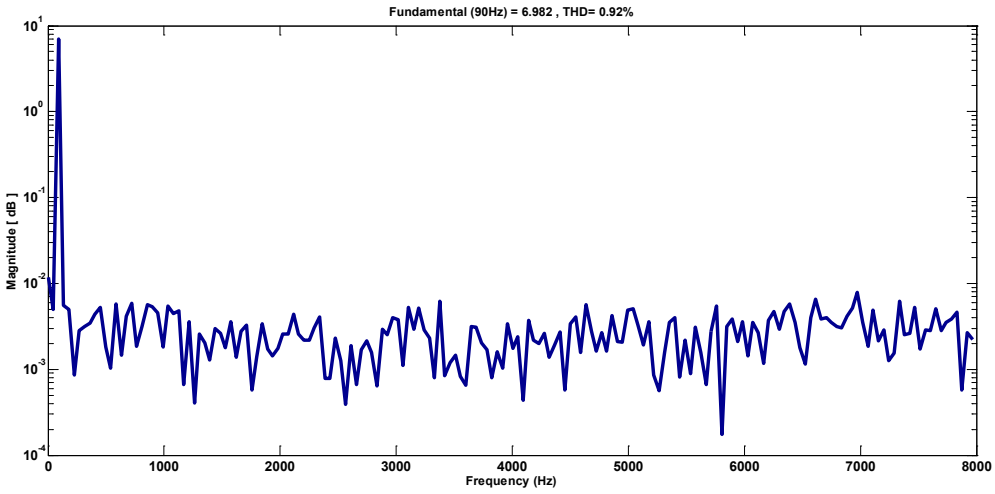


Figure 3.11: Frequency spectrum of load current (Case 1 and 90 Hz load current reference)

Step response of the model predictive control based on switching state elimination is shown in Figure 3.13 and phase plane plot for load current is shown in Figure 3.14. In Figure 3.13, the load current reference step is applied from 7A/45 Hz to 5A/90 Hz. No

effort is made to match the sine wave phase at the step instant, so that a more severe transient is obtained. The system response is fast and clean and shows no oscillation.

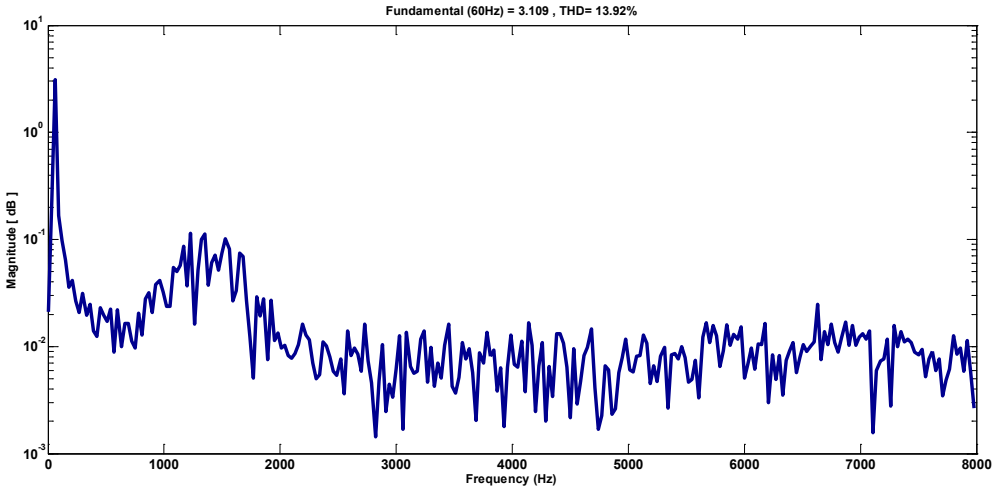


Figure 3.12: Frequency spectrum of source current (Case 1 and 90 Hz load current reference)

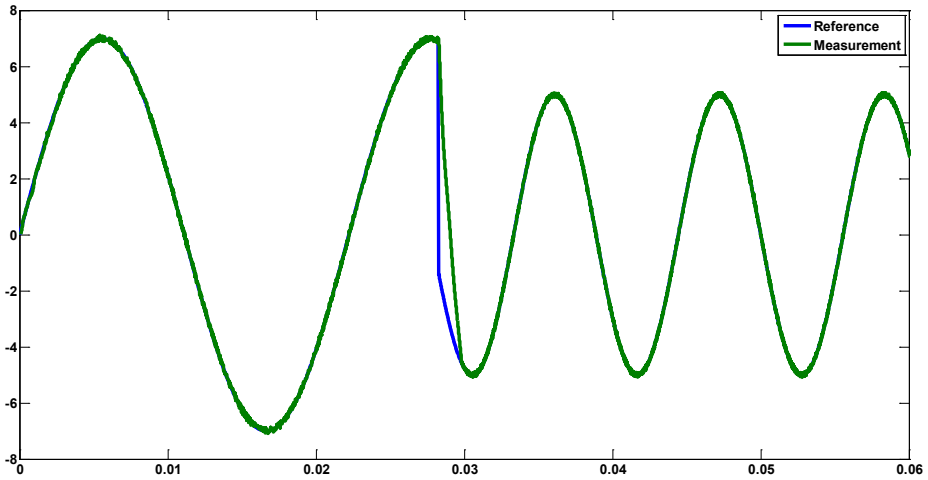


Figure 3.13: Dynamic response of MPC based on switching state elimination

Simulation parameters for the second case are the same as for the first case, see Table 3.2. Reference source current peak value is 3.3 A. Normalized current error term is exactly the same as for CASE 1, σ=0.015, and it allows us to obtain good power quality

and load current tracking. The simulation results for second case are shown in Figure 3.15. Figure 3.16 and 3.17 show the spectral content of the load and source current. The source current THD is significantly better than in CASE 1 (0.25% versus 13-14% for CASE 1).

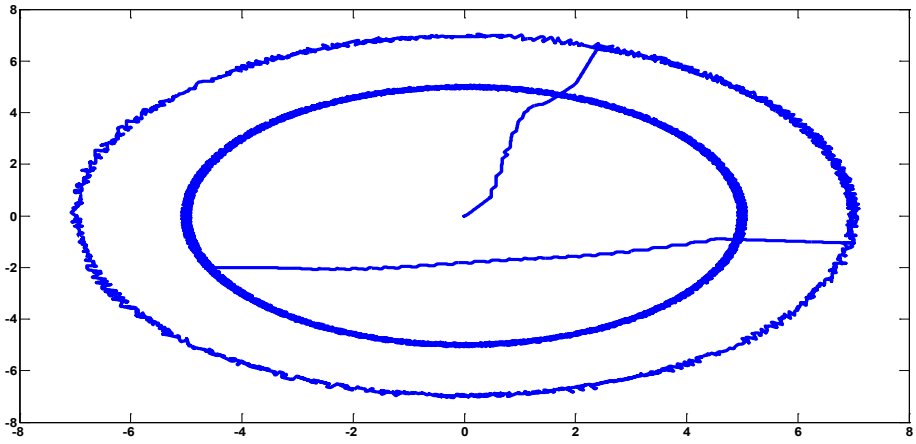


Figure 3.14: Phase plane plot of load current

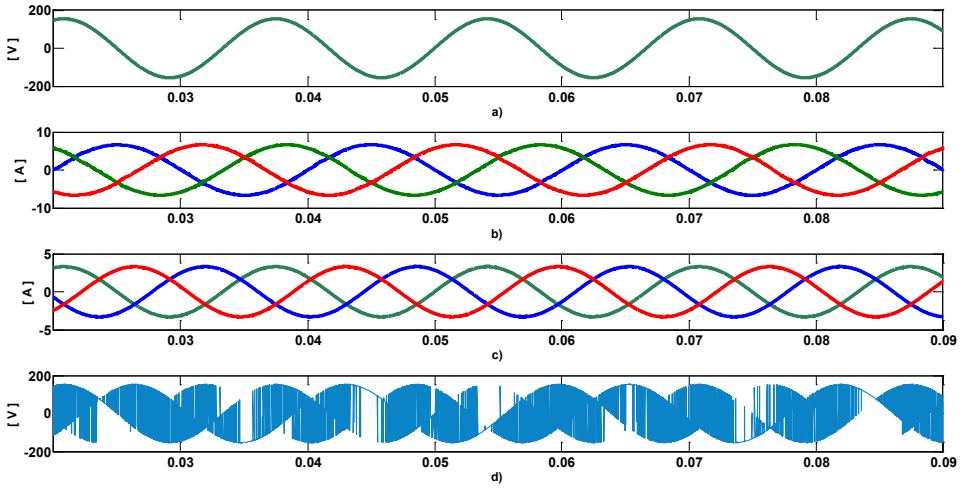


Figure 3.15: Simulation results for Case 2 (50 Hz load current reference) a) Supply voltage b) Load current c) Supply current d) Output load voltage

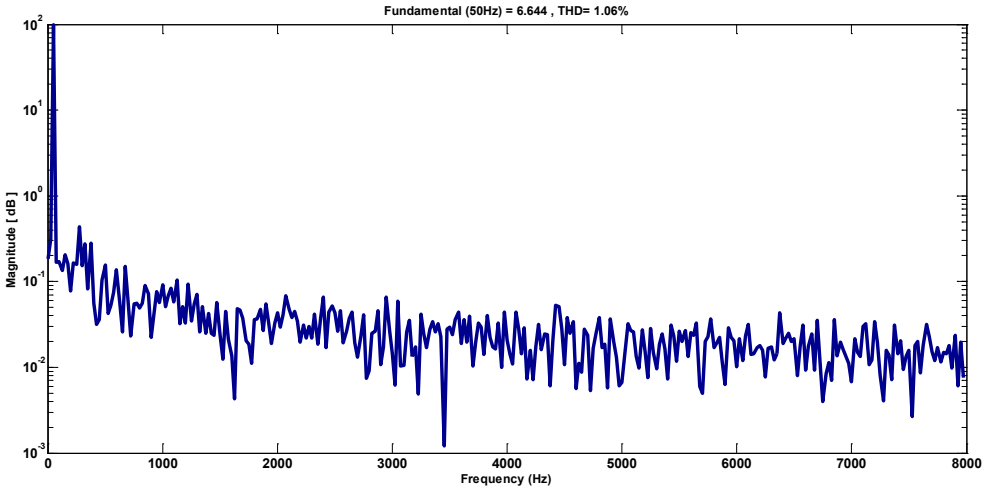


Figure 3.16: Frequency spectrum of load current (Case 2 and 50 Hz load current reference)

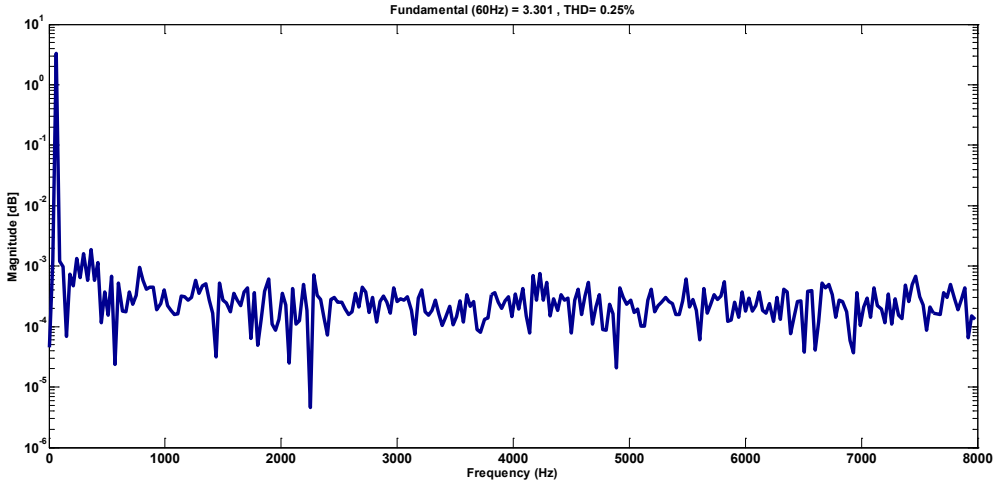


Figure 3.17: Frequency spectrum of source current (Case 2 and 50 Hz load current reference)

3.4 EXPERIMENTAL RESULTS

The matrix converter prototype, see Figure 2.15, is used to validate switching state elimination technique. The proposed method is implemented in DEO-nano FPGA board and tested for different load current reference. The experimental result is shown

Figure 3.18 in case of 45 Hz load current frequency. In all experimental results, channel 1 is source current measurement. channel 2 is load current measurement and channel 3 is supply voltage. In order to analyze the load current quality and source current quality, FFT analysis is carried out using MATLAB. The sampled data from scope, Tektronix TDS2014B, is extracted and analyzed using MATLAB toolbox. Since MATLAB has powerful math toolboxes, Total Harmonic Distortion is calculated using MATLAB. Load current frequency spectrum and source current frequency spectrum are shown in Figure 3.19 and Figure 3.20, respectively.

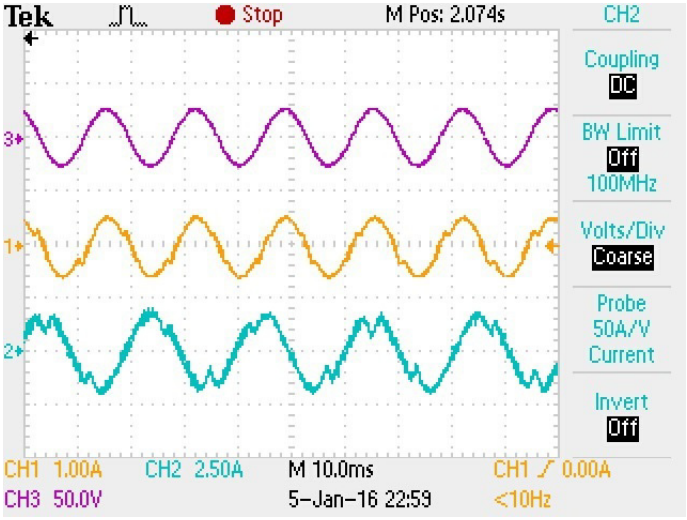


Figure 3.18: Experimental result in case of 45 Hz load current frequency

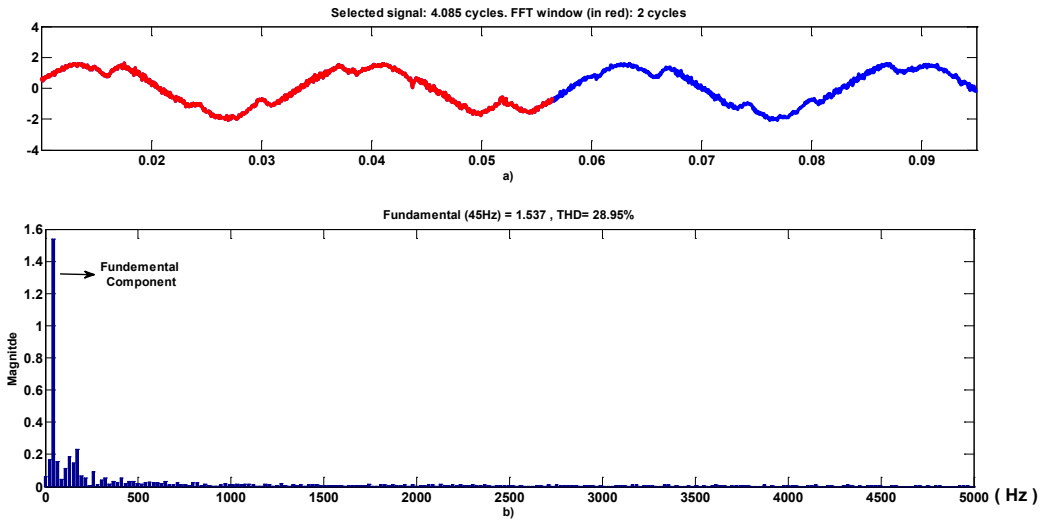


Figure 3.19: FFT analysis of load current (45 Hz load current reference) a) Load current measurement b) Frequency spectrum of load current

In Figure 3.19, FFT window is shown in red and FFT is carried out up to 5 kHz. In Figure 3.19b, the magnitude of spectral contents are displayed relative to base value, which is 1.0, and total harmonic distortion of load current is 28.95%. For FFT analysis, hanning window is used and maximum frequency for THD computation is Nyquist frequency.

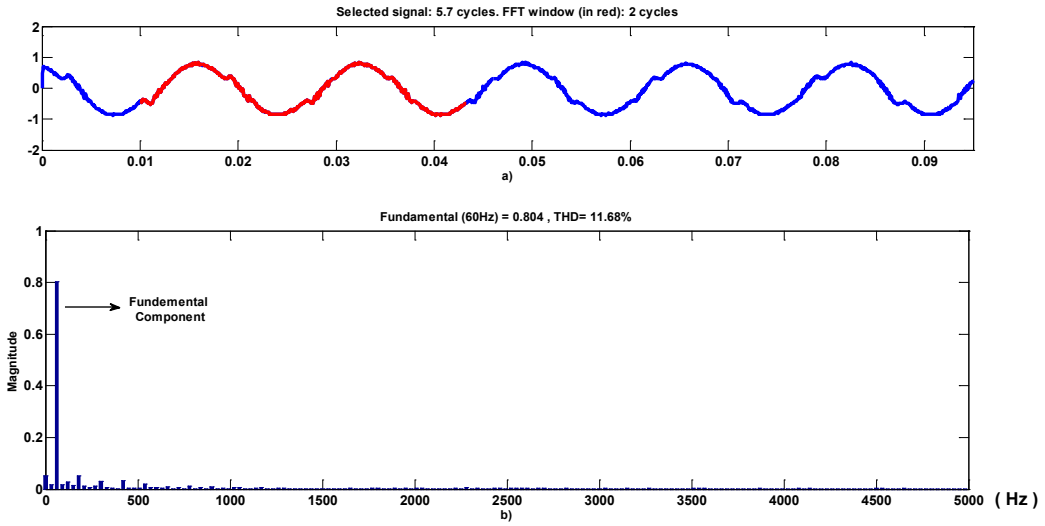


Figure 3.20: FFT analysis of source current (45 Hz load current reference) a) Source current measurement b) Frequency spectrum of source current

Figure 3.21 shows experimental results in case of 60 Hz load current reference. The experimental results are better compared to the ones in case of 45 Hz load current frequency. Load current quality is better and the proposed method provides good load current tracking.

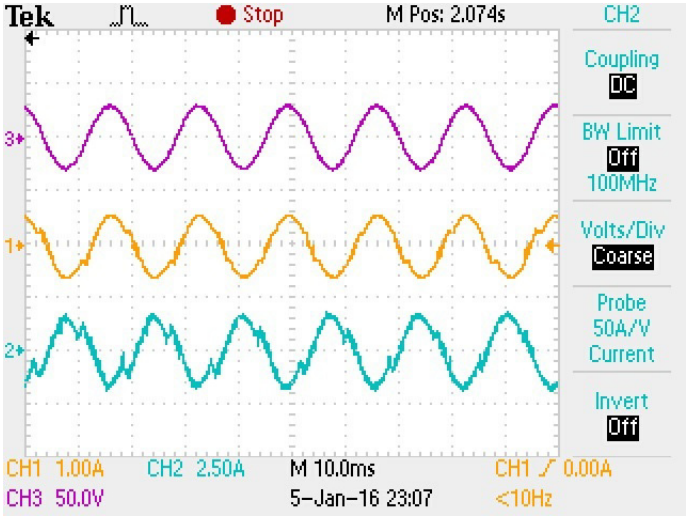


Figure 3.21: Experimental result in case of 60 Hz load current frequency

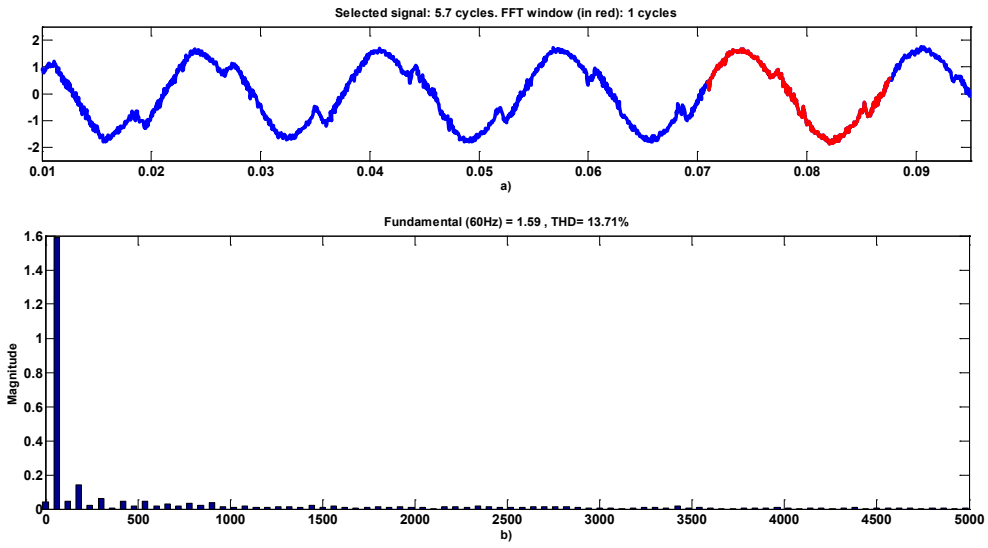


Figure 3.22: FFT analysis of load current (60 Hz load current reference) a) Load current measurement b) Frequency spectrum of load current

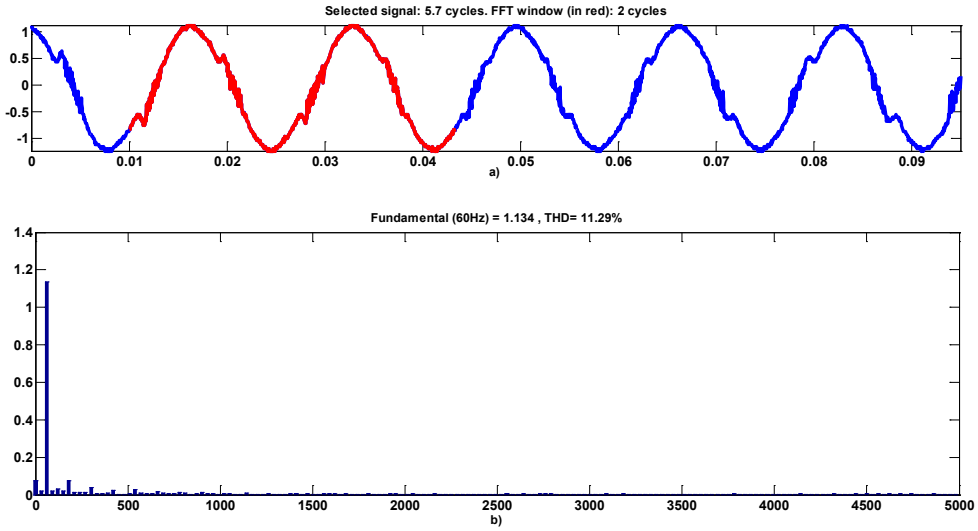


Figure 3.23: FFT analysis of source current (60 Hz load current reference) a) Source current measurement b) Frequency spectrum of source current

According to Figure 3.22 and Figure 3.23, load current THD is 13.71% and source current THD is 11.29%. The proposed method is tested when load current frequency is higher than the supply frequency. Figure 3.24 shows experimental results in case of 90 Hz load current reference.

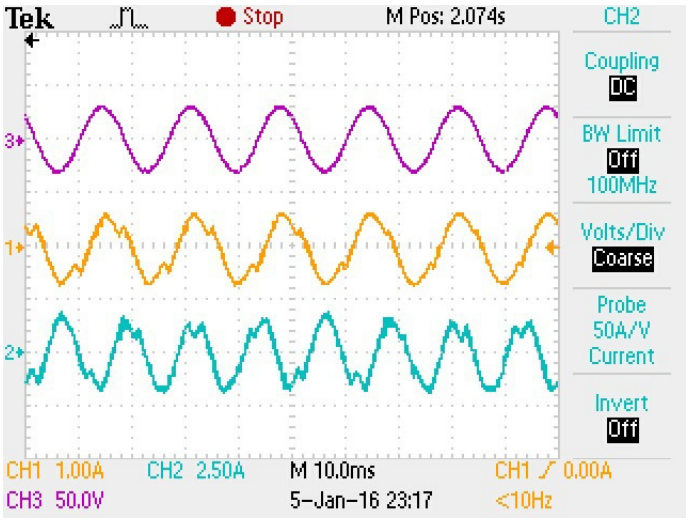


Figure 3.24: Experimental result in case of 90 Hz load current frequency

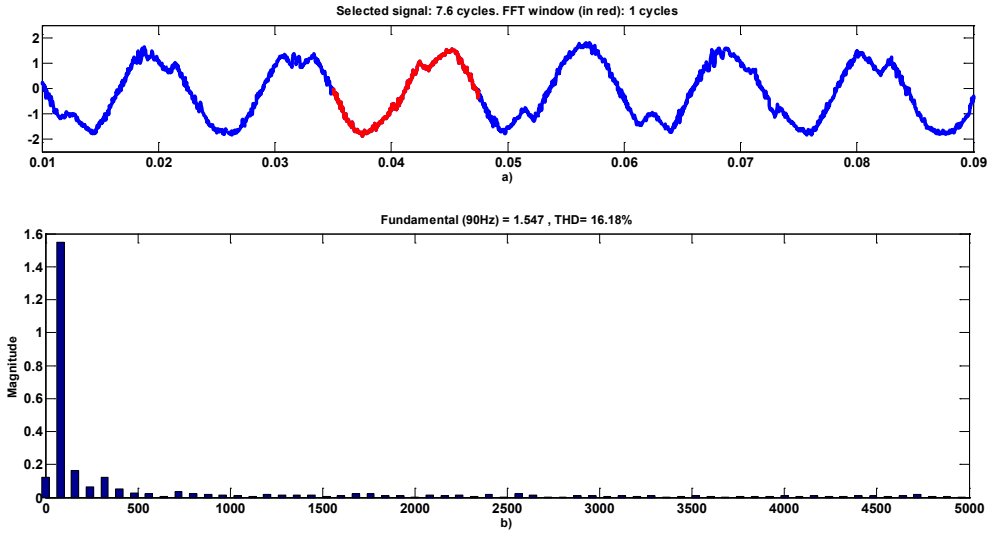


Figure 3.25: FFT analysis of load current (90 Hz load current reference) a) Load current measurement b) Frequency spectrum of load current

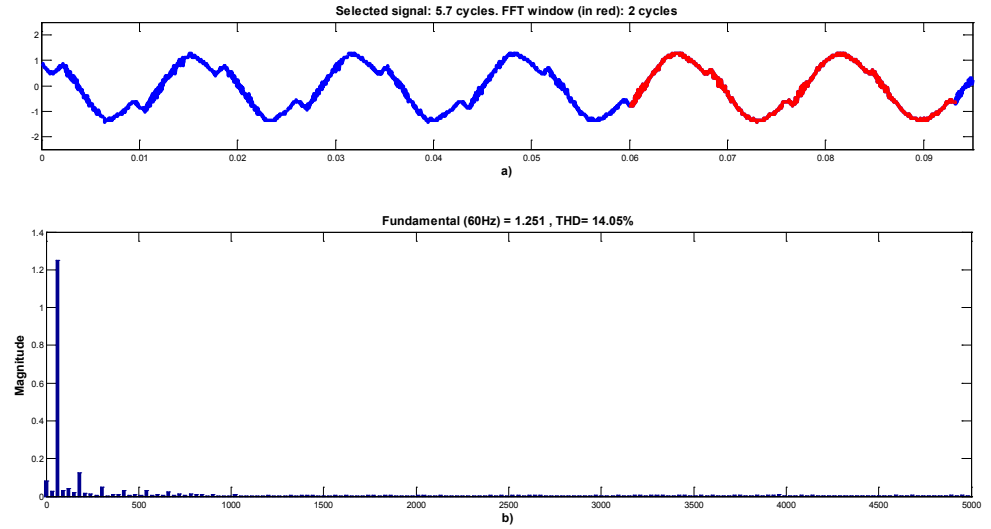


Figure 3.26: FFT analysis of source current (90 Hz load current reference) a) Source current measurement b) Frequency spectrum of source current

3.5 CONCLUSION

This chapter presents a model predictive control algorithm based on switching state elimination technique. The proposed method uses simple control constraints and elimination condition with a clear physical interpretation to determine the optimum switching combination. The main advantage of the proposed algorithm is easy tuning process since the range of control constraints is independent from system parameter and power level.

CASE 1 is considered to make a comparison between the proposed method and conventional FCS-MPC. The proposed algorithm has a higher computational burden than the FCS-MPC. The FCS-MPC approach solves just one multi-objective problem and required calculation time is smaller than the time needed for the switching state elimination technique. Prediction horizon and size of the finite sets increase time needed for calculating the optimum switching combination. Number of switching states, prediction horizon and control objectives can be used to make a comparison between conventional MPC and new algorithms in terms of computational cost [50]. The comparison results in terms of computational burden are shown in Table 3.3.

Table 3.3: Comparison results in terms of computational burden

Task	**Conventional MPC**	**Switching State Elimination**
Optimization	a^h	0
Model	a^h	a^h
Elimination	0	$(a+m)^h$
Exhaustive Search	0	n^h
TOTAL	54	75.63

In Table 3.3, m and n are the average size of the sub-finite solution sets, T_2 and T_3, and they are calculated for one period. the average size of T_2 is 13.13 and the

average size of T_3 is 8.5. a refers to size of T_1 and it is 27. The prediction horizon h is 1. Calculation time for the proposed method is not constant and depends on how many acceptable switching states are obtained for the sub-optimization problem.

It is shown that good performance was obtained with switching state elimination technique in steady state and transient. The proposed method was tested for different control objectives and simulation results show that proposed method works well under different conditions. The proposed method was also tested experimentally for CASE 1 (three control objectives) and experimental results show that switching state elimination technique works well for direct matrix converter.

CHAPTER 4

MODEL PREDICTIVE CONTROL FOR NINE-SWITCH INVERTER

In power electronics applications, it is very important to control the power converters under unknown load conditions. Power electronics converters play an important role in providing clean power to loads in stand-alone systems. The loads can be single-phase, balanced or unbalanced, linear or nonlinear. Control of the power converter must work well under all load conditions and the control method should provide clean power no matter what the load is. Since model predictive control uses the system model for prediction process, investigation of predictive controller performance under unknown load condition is interesting an topic. The method will be studied for a dual-output nine switch inverter. Another important aspect is that conventional control technique for nine-switch inverter is complicated and this converter topology requires complicated modulation scheme with conventional control approaches.

In this chapter MPC is applied to the control of the dual-output nine-switch inverter and with unknown loads. The use of an inverter with an output filter allows the generation of output sinusoidal voltages with low harmonic distortion, suitable for UPS applications. Load current estimation is performed using an observer and performance of the predictive control technique is investigated under linear and nonlinear load conditions.

4.1 CONVENTIONAL CONTROL TECHNIQUE FOR NINE-SWITCH INVERTER

In the literature, different pulse width modulation (PWM) and linear control methods have been reported for the control of the nine-switch inverter. Different modulation schemes, such as carried-based modulation and space vector modulation (SVM), can be used to control dual-output power converters [29]. The main drawback with these linear controllers is that multi-loop control is required to independently adjust the two ac outputs [31],[60]. The usage of multi-loop techniques increases the complexity of implementation of the controller [32]. Figure 4.1 shows the conventional linear control technique for nine-switch inverter. According to Figure 4.1, two separate PI controller calculate the reference voltage and space vector modulator generates the gate signals.

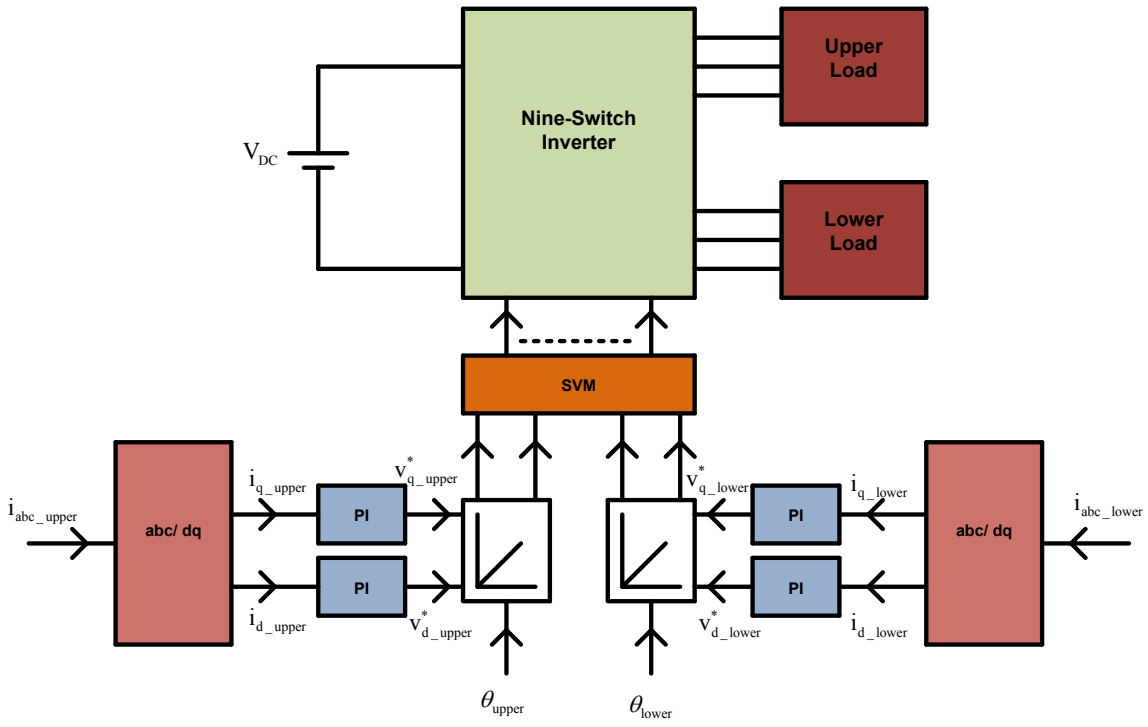


Figure 4.1: Conventional control method for nine-switch inverter

There are four linear control loops for two-ac loads and output load currents are controlled in the d-q reference frame using PI controllers. There is a modulation stage in control scheme and implementation of space vector modulation for nine-switch inverter is more complicated compared to implementation of SVM for conventional two-level three-leg Voltage Source Inverter (VSI). Output load currents are controlled in d-q frame and phase information must be extracted using PLL technique. In general, the four control loops need to be separately tuned and the output of the PI controllers provide reference voltages to the modulator.

4.2 SYSTEM MODEL

Derivation of system model is critical in model predictive control approach. In this work, nine-switch inverter with output filter is chosen as a case study to explain how proposed method works. System model includes nine-switch inverter model, output filter model and load current observer model. The proposed predictive controller uses these models to predict future values of the control variables for different switch combination. The load current observer estimates the current value of load currents, so that they do not need to be measured.

4.2.1 NINE-SWITCH INVERTER MODEL

The nine-switch inverter model with output with filter is shown Figure 4.2. There are two interconnection matrices, one is for lower load and other is for upper load [61]. The interconnection matrix of upper load T_U and interconnection matrix of lower load T_L are given in (4.1) and (4.2).

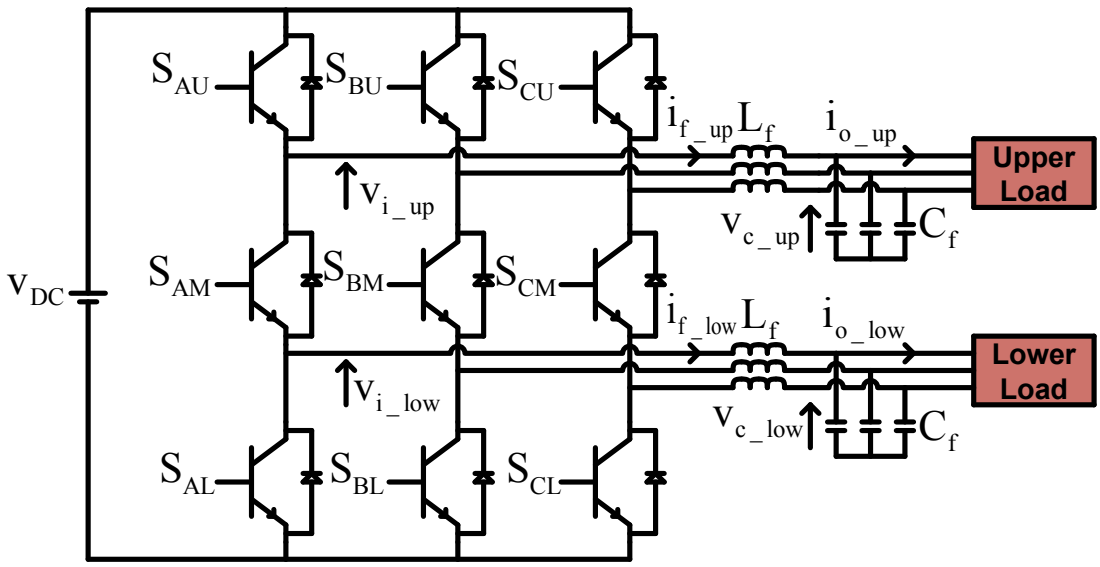


Figure 4.2: Nine-switch inverter with output filter

$$\mathbf{T_U} = \begin{bmatrix} S_{AU} & S_{BU} & S_{CU} \end{bmatrix} \tag{4.1}$$

$$\mathbf{T_L} = \begin{bmatrix} 1-S_{AL} & 1-S_{BL} & 1-S_{CL} \end{bmatrix} \tag{4.2}$$

The inverter leg voltages of upper and lower loads can be calculated using interconnection matrix and dc-link voltage. The relationship between inverter leg voltages and dc-link voltage for upper load side are expressed in (4.3) and (4.4).

$$\mathbf{v_{i\_up}} = v_{DC}\mathbf{T_U^T} \tag{4.3}$$

$$\mathbf{v_{i\_low}} = v_{DC}\mathbf{T_L^T} \tag{4.4}$$

4.2.2 Output Filter Model

The LC output filter, shown in Figure 4.3, is used to eliminate harmonics of the output load current. Filter parameters can be chosen depending on load current specifications.

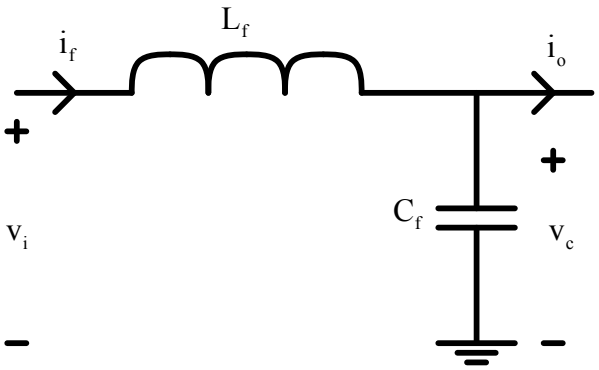


Figure 4.3: Output filter model

The dynamic model of the output filter can be expressed as

$$L_f \frac{di_f}{dt} = v_i - v_c \tag{4.5}$$

$$C_f \frac{dv_c}{dt} = i_f - i_o \tag{4.6}$$

L_f and C_f are the inductance and capacitance of the output filter, respectively. Voltage v_i is the input voltage of the output filter, voltage v_c is the capacitor voltage, current i_f is the inductor current and i_o is the output current. The dynamic model expressed in (4.5) and (4.6) can be used for upper load side and lower load side. The block diagram of LC filter model is shown in Figure 4.4.

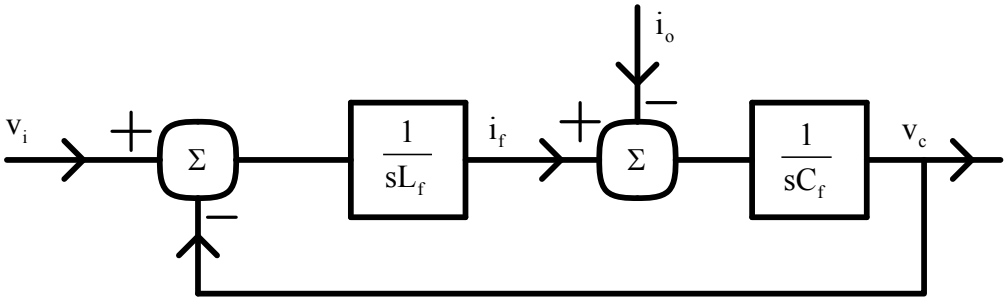


Figure 4.4: Output LC filter model

The dynamic model of the filter can be represented by state-space approach. The state-space model of the output LC filter is expressed in (4.7) and (4.8) using (4.5) and (4.6).

$$\frac{d}{dt}\begin{bmatrix} i_f \\ v_c \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L_f} \\ \frac{1}{C_f} & 0 \end{bmatrix}\begin{bmatrix} i_f \\ v_c \end{bmatrix} + \begin{bmatrix} \frac{1}{L_f} & 0 \\ 0 & -\frac{1}{C_f} \end{bmatrix}\begin{bmatrix} v_i \\ i_o \end{bmatrix} \tag{4.7}$$

$$y = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}\begin{bmatrix} i_f \\ v_c \end{bmatrix} \tag{4.8}$$

4.2.3 OBSERVER MODEL

For most control systems, the measurement of the full state vector is sometimes impractical. In order to implement a control system based on full state feedback, state variables need to be estimated based on measurements that are practical. The first step is to decide which state variables to measure and which ones to estimate. Then an observer can be designed for state estimation. Since output current is needed in the output filter model of (4.7) and (4.8), this current can be either measured or estimated using an observer. For current and voltage measurement, several sensing methods can be used but these techniques usually cost extra money. In this work, to reduce the number of sensors required, two separate observers are used to estimate the two three-phase output load currents. Since the dynamics of the load currents are unknown, the dynamic model of the output load current can be approximated as a constant.

$$\frac{di_o}{dt} \approx 0 \tag{4.9}$$

The approximation expressed in (4.9) can be used for upper load and lower load current. The system model augmented to include this load model is given in (4.10) and (4.11).

$$\frac{d}{dt}\begin{bmatrix} i_f \\ v_c \\ i_o \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{C_f} & 0 \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f} \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_f \\ v_c \\ i_o \end{bmatrix} + \begin{bmatrix} \frac{1}{L_f} \\ 0 \\ 0 \end{bmatrix} v_i \tag{4.10}$$

$$y = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} i_f \\ v_c \\ i_o \end{bmatrix} \tag{4.11}$$

Observer can estimate the system state variables from available measurements. In the dynamic model presented in (4.10) and (4.11), filter capacitor voltage v_c and filter inductor current i_f are available measurements. In order to define the observer model, we can choose the control input $u(k)$ by the relationship

$$u(k) = -\mathbf{K}\mathbf{x}(\mathbf{k}) \tag{4.12}$$

where,

$\mathbf{K} = \begin{bmatrix} K_1 & K_2 & K_3 \end{bmatrix}$ and $\mathbf{x} = \begin{bmatrix} i_f & v_c & i_o \end{bmatrix}^T$

The observer model for estimating the load current is defined as

$$\frac{d\hat{\mathbf{x}}}{dt} = A\hat{\mathbf{x}} + Bv_i + K(y - \hat{y}) \tag{4.13}$$

$$\hat{y} = C\hat{\mathbf{x}} \tag{4.14}$$

where,

$$A = \begin{bmatrix} 0 & -\frac{1}{C_f} & 0 \\ \frac{1}{C_f} & 0 & -\frac{1}{C_f} \\ 0 & 0 & 0 \end{bmatrix}, \quad B = \begin{bmatrix} \frac{1}{L_f} \\ 0 \\ 0 \end{bmatrix} \text{ and } C = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

K is the state gain matrix, which can be determined by either the pole-placement method or the quadratic optimal control method. If the system considered is completely state controllable, then poles of the closed loop system can be placed at any desired locations by using an appropriate state feedback gain matrix. Design method begins with a determination of the desired close-loop poles based on frequency response requirements, such as bandwidth, noise-cancellation or damping ratio. For proper operation, **K** is chosen to make the matrix **A-CK** stable. The regulators poles, which are the eigenvalues of the matrix **A-CK**, must be placed in the left half s-plane. If we assume that desired close-loop poles are p_1, p_2 and p_3, the desired characteristic equation is defined as

$$(s - p_1)(s - p_2)(s - p_3) = s^3 + \alpha_1 s^2 + \alpha_2 s + \alpha_3 \tag{4.15}$$

Ackermann's formula can be used to determine the state gain matrix. The system considered in this work is a third order system and the Ackermann formula for third order system is defined as in (4.16).

$$\mathbf{K} = \begin{bmatrix} 0 & 0 & 1 \end{bmatrix} \left| \mathbf{A} \vdots \mathbf{AB} \vdots \mathbf{A^2 B} \right|^{-1} \Phi(\mathbf{A}) \tag{4.16}$$

where

$$\Phi(\mathbf{A}) = \mathbf{A^3} + \alpha_1 \mathbf{A^2} + \alpha_2 \mathbf{A} + \alpha_3 \mathbf{I} \tag{4.17}$$

The selection of the desired poles is a compromise between speed of convergence of the observer and measurement noise. If dominant poles are located far from the origin, system response becomes fast. The block diagram of the system and the observer is shown in Figure 4.5.

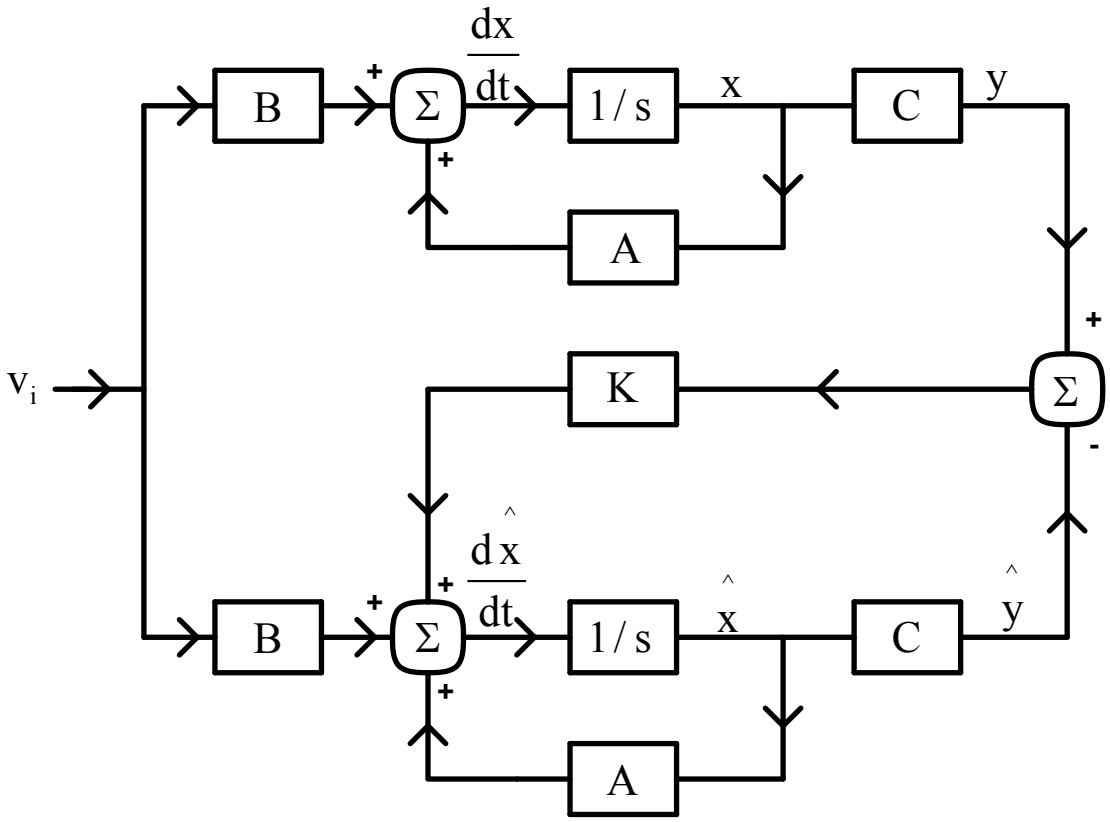


Figure 4.5: Block diagram of the system and observer

Figure 4.6 shows the poles of the system presented in (4.10) and (4.11) and the poles of the slow observer and fast observer. If poles are chosen far from the origin, dynamic response of the observer will be faster, which is the characteristic of fast observers. However, if observer poles are chosen closer to the LC filter poles, observer will be better for noise rejection.

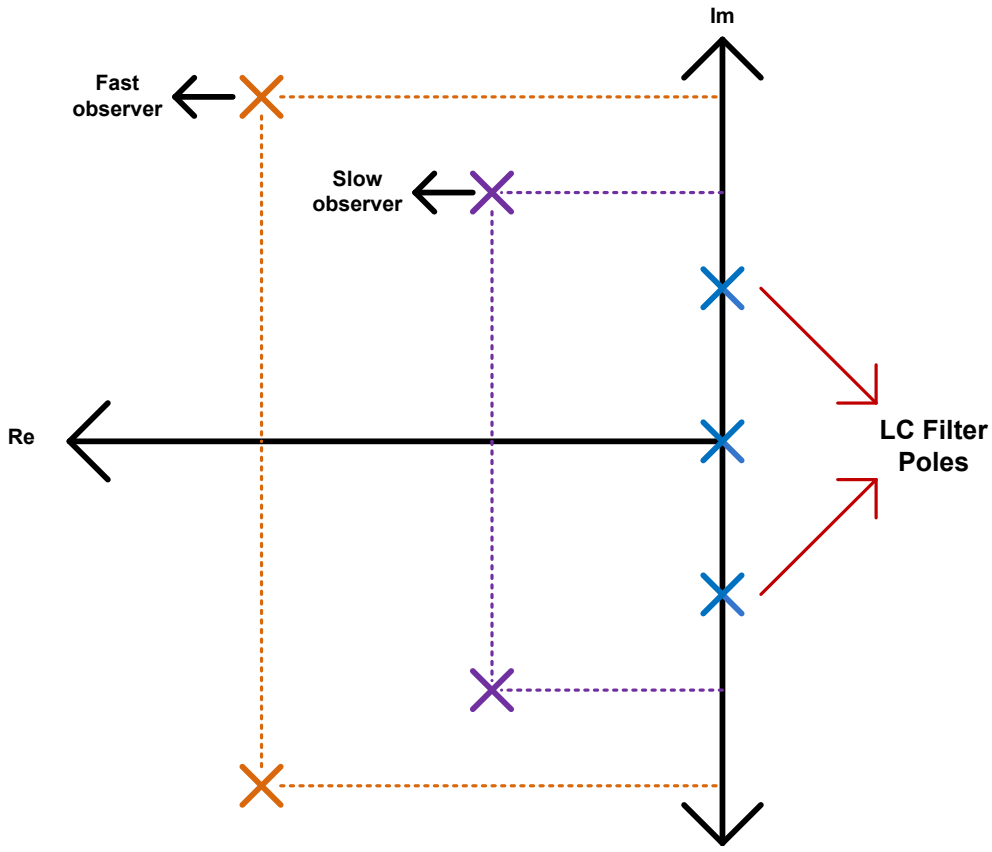


Figure 4.6: Poles of the system and observers

For a good observer design, observer poles can be chosen as several times faster than original systems. The simple approach is to choose the ratio of magnitude of the observer pole to magnitude of LC filter poles in the range,

$$8 \le \frac{|S_{observer}|}{|S_{LC}|} \le 12 \tag{4.18}$$

$|S_{observer}|$ is magnitude of the observer and $|S_{LC}|$ is magnitude of LC filter pole. The another important aspect is that damping ratio should be chosen properly to obtain enough damping. Figure 4.7 presents the damping ratio and magnitude of the observer pole.

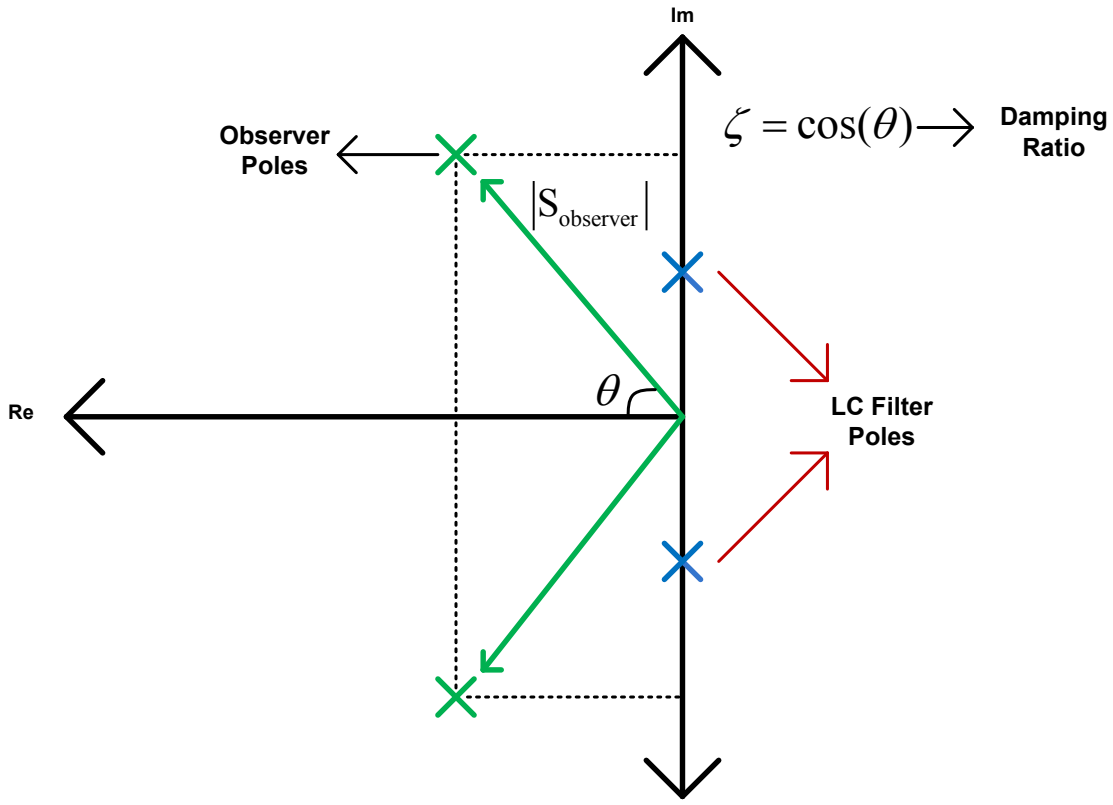


Figure 4.7: Selection of observer poles

4.3 Model Predictive Control Scheme

The model predictive control strategy is based on the idea that upper load and lower load voltages are predicted for each possible switching combination and an appropriate switching state that provides good voltage tracking is selected and applied to the converters. The predictive control scheme for nine-switch inverter with output filter is shown in Figure 4.8. Two output voltages are controlled using a single control loop and the control scheme is not dependent on load parameters, since the load current is provided by the observer.

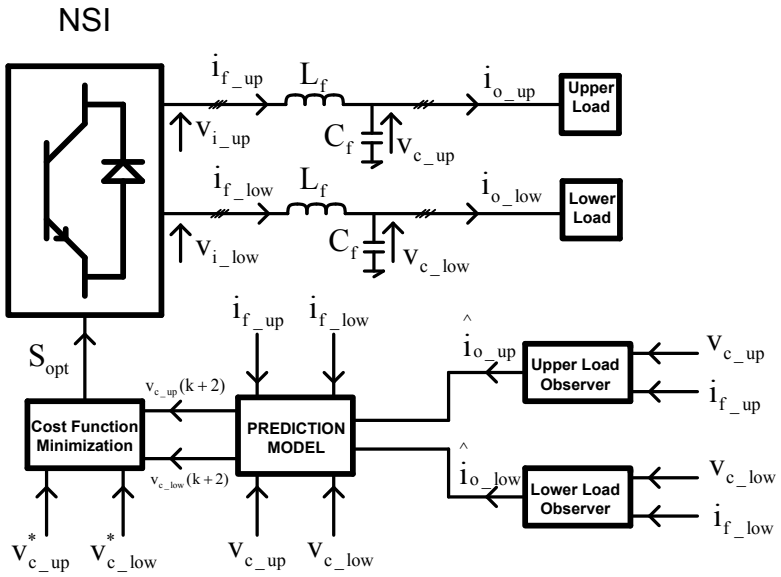


Figure 4.8: Model predictive control scheme for nine-switch inverter

In order to obtain future output voltage expression for upper load and lower load, the load model is discretized using the classical Euler method.

$$\frac{dx}{dt} \approx \frac{x(k+1)-x(k)}{Ts} \tag{4.19}$$

The future values of the filter inductor currents for upper load and lower load side can be obtained using (4.5) and (4.19).

$$i_{f\_up}(k+1) = i_{f\_up}(k) + \frac{Ts}{L_f}(v_{i\_up}(k) - v_{c\_up}(k)) \tag{4.20}$$

$$i_{f\_low}(k+1) = i_{f\_low}(k) + \frac{Ts}{L_f}(v_{i\_low}(k) - v_{c\_low}(k)) \tag{4.21}$$

The future values of the capacitor voltages for upper load and lower load side are given in (4.22) and (4.23).

$$v_{c\_up}(k+1) = v_{c\_up}(k) + \frac{Ts}{C_f}(i_{f\_up}(k) - i_{o\_up}(k)) \tag{4.22}$$

$$v_{c\_low}(k+1) = v_{c\_low}(k) + \frac{Ts}{C_f}(i_{f\_low}(k) - i_{o\_low}(k)) \tag{4.23}$$

The proposed predictive control method aims to control the two three-phase output voltages by solving a single multi-objective cost function. Figure 4.9 shows nine-switch inverter topology under unknown load condition. Present-time load current values are required to predict the future output voltages according to (4.22) and (4.23). Since load parameters and dynamic model of the load are unknown, load current must be either measured or an observer can be used. In this control implementation, an observer is used.

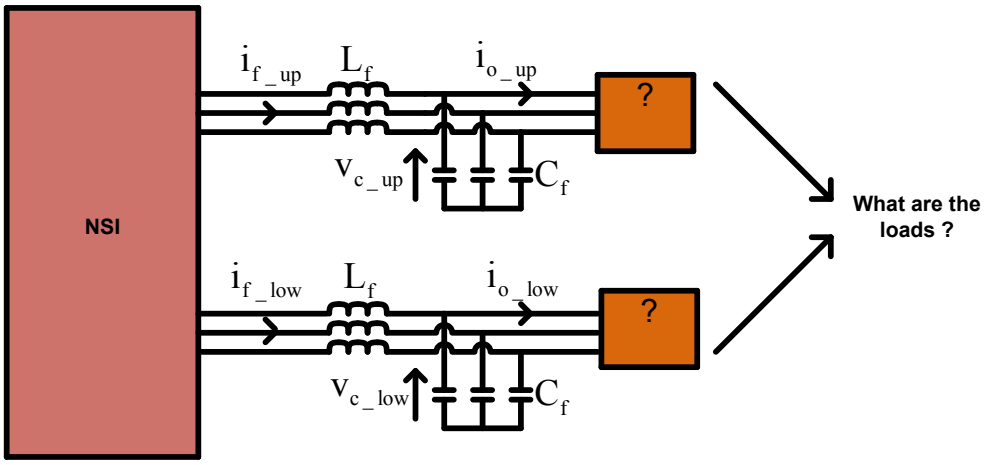


Figure 4.9: Nine-switch inverter under unknown load conditions

Since predictive controller aims to minimize the error between predicted output filter capacitor voltage and its reference, the cost function is chosen as in (4.26).

$$g_1 = \sqrt{\left|v^*_{c\alpha\_up}(k+1) - v_{c\alpha\_up}(k+1)\right|^2 + \left|v^*_{c\beta\_up}(k+1) - v_{c\beta\_up}(k+1)\right|^2} \tag{4.24}$$

$$g_2 = \sqrt{\left|v^*_{c\alpha\_low}(k+1) - v_{c\alpha\_low}(k+1)\right|^2 + \left|v^*_{c\beta\_low}(k+1) - v_{c\beta\_low}(k+1)\right|^2} \tag{4.25}$$

$$g = Ag_1 + Bg_2 \tag{4.26}$$

Three-phase output capacitor voltages for upper load and lower load side are transformed to the α-β reference frame and costs for the two capacitor voltage errors are evaluated in this frame.

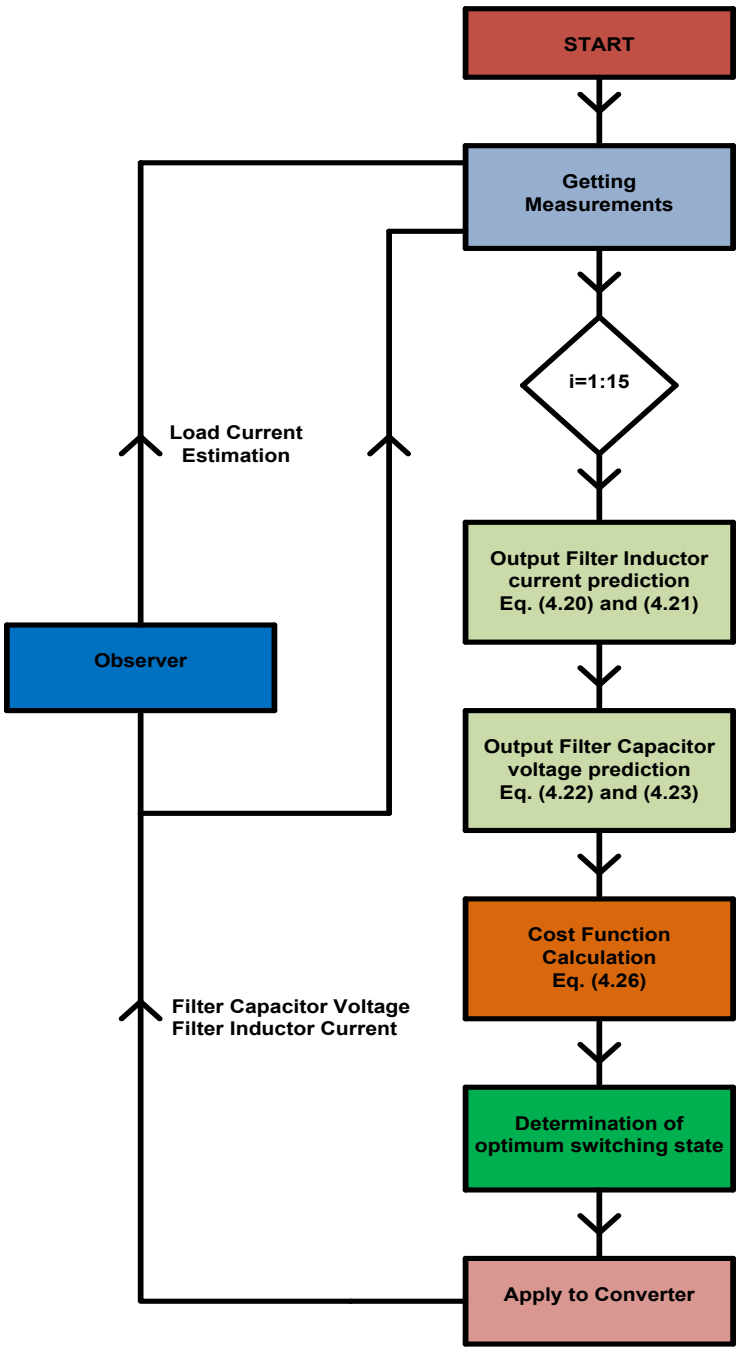


Figure 4.10: Algorithm flow chart for predictive controller

A and B are the weighting factors and reference values are denoted by superscript "*". The cost function, (4.26) is calculated for all 15 different switching states and the switching combination that minimizes this cost function is selected as the optimal action for the next time interval. The algorithm flow chart for proposed predictive control scheme is shown in Figure 4.10. Note the observer used for load current estimation. The terms in the cost function are homogeneous in nature, in the sense that g_1 and g_2 are both voltage errors. Therefore, the weighting factors for each term can be selected to be equal (A=B=1) so that upper output voltage control and lower output voltage control have the same importance. If tighter control of one of the control output voltages in desired, the corresponding weighting factor can be increased. Some empirical adjustment of weighting factors would be required.

4.4 SIMULATION RESULTS

The Nine-switch inverter shown in Figure (4.2) is simulated using MATLAB Simulink. The proposed control scheme is tested in case of both linear load condition and nonlinear load condition. The observer performance is tested under the steady-state and transient condition. Simulation parameters are listed in Table 4.1.

Table 4.1: Simulation Parameters

Parameter	**Value**
Filter inductor	1.85 mH
Filter capacitor	33 μF
DC-link voltage	220 V
Sampling period	40 μs
Upper load resistor	10 Ω
Upper load inductor	20 mH
Lower load resistor	10 Ω
Lower load inductor	20 mH

The observer poles are located approximately 10 times faster than poles of the actual system. Figure 4.11 shows poles location of observer and LC filter.

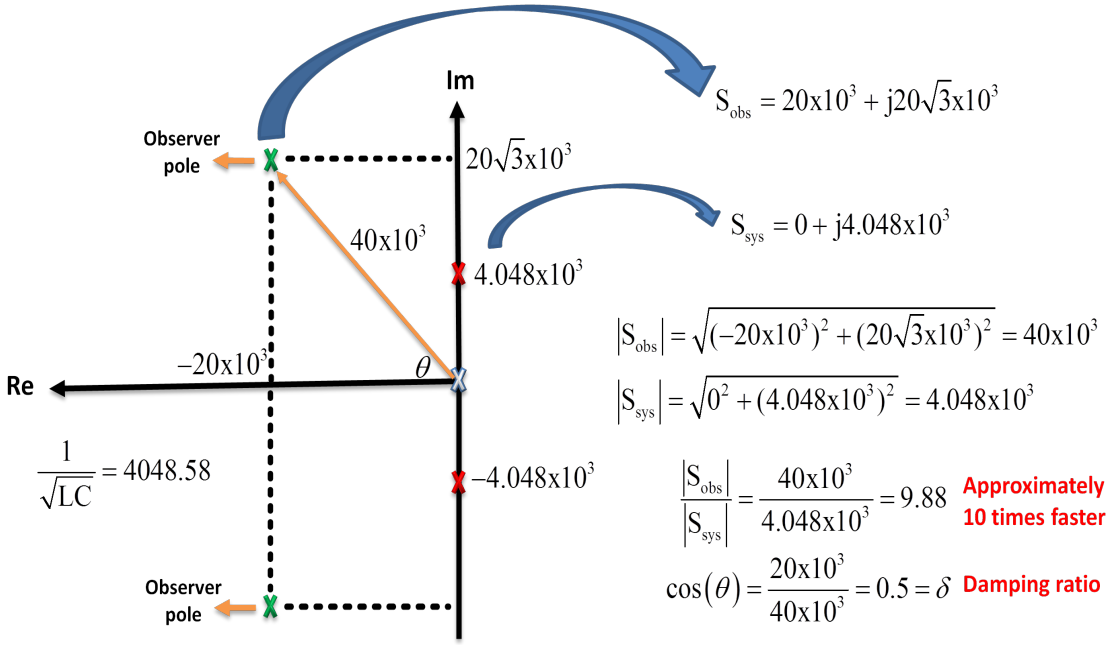


Figure 4.11: Poles location of observer and LC filter for simulation

4.4.1 Linear Load Condition

An R-L circuit is chosen as a load for testing controller performance under linear load condition. Figure 4.12 shows output load voltage and load current waveforms under linear load condition. According to results, predictive control technique provides good sinusoidal output voltage and load current. Reference frequencies and peak values for upper output voltage and lower output voltage are different and these two output voltages are controlled independently. Upper capacitor voltage reference is 40 V/120Hz and lower capacitor voltage reference is 50 V/80 Hz. Figure 4.13 and Figure 4.14 show the frequency spectrums of the output capacitor voltages obtained with predictive control up

to 5kHz. According to Figure 4.13, the upper capacitor Total Harmonic Distortion (THD) is 1.12%.

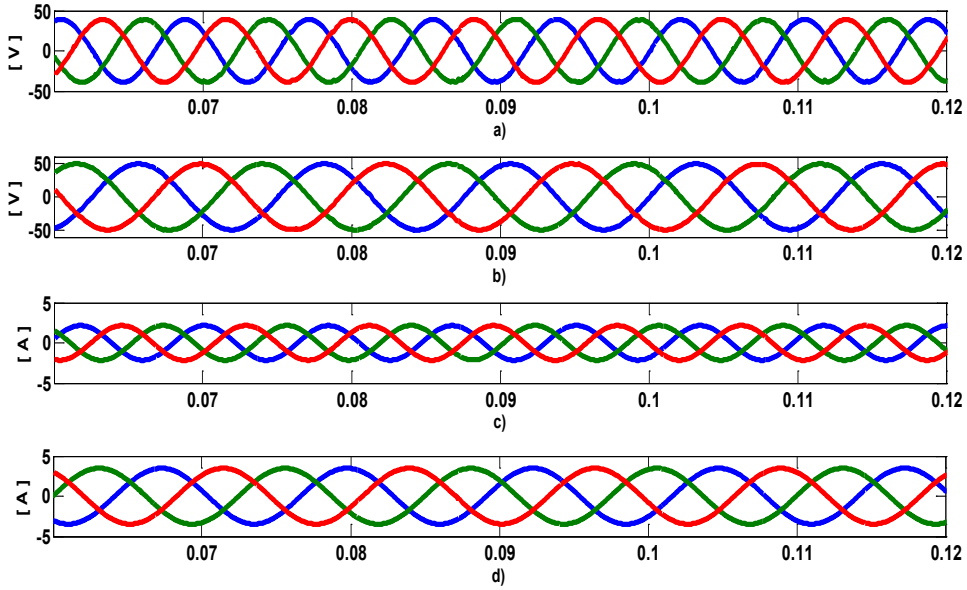


Figure 4.12: Simulation results a) Output upper capacitor voltage b) Output lower capacitor voltage c) Upper load current d) Lower load current

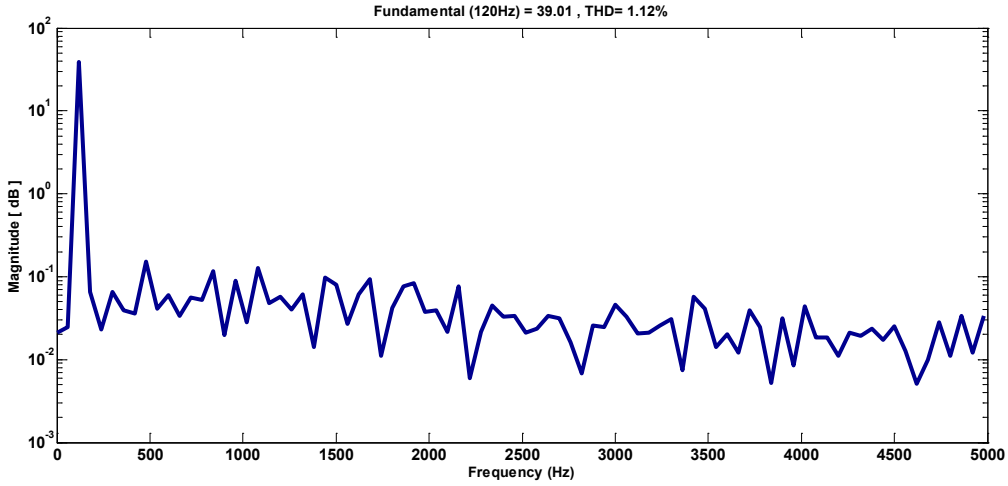


Figure 4.13: Output upper capacitor voltage frequency spectrum under linear load condition

Figure 4.14 shows that lower capacitor voltage quality is slightly better, with total harmonic distortion of 0.74%, These values of THD are quite good.

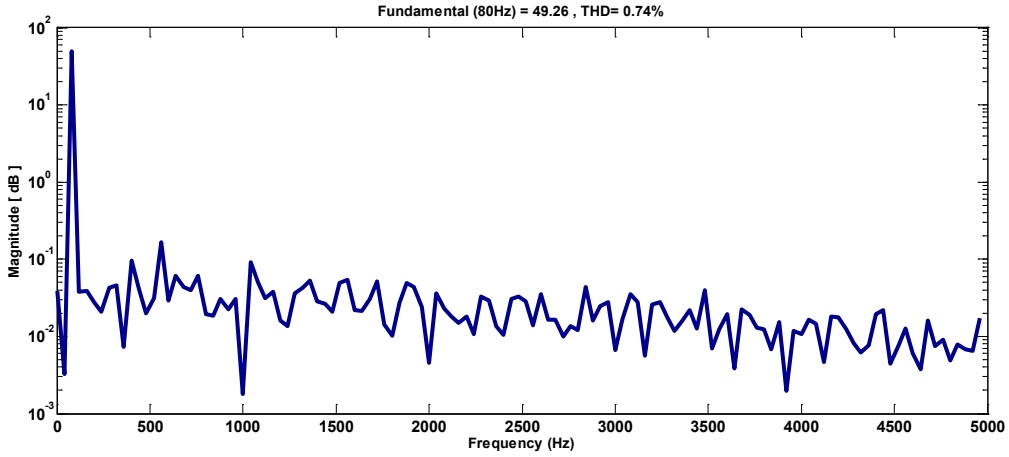


Figure 4.14: Output lower capacitor voltage frequency spectrum under linear load condition

Figure 4.15 and Figure 4.16 the frequency spectra for upper load current and lower load current. The frequency spectrum is presented up to 5kHz and according to Figure 4.15, value of THD is for upper load current is 0.24%, which is quite good. THD value for lower load current is 0.20% and simulation results show that predictive controller provides good power quality.

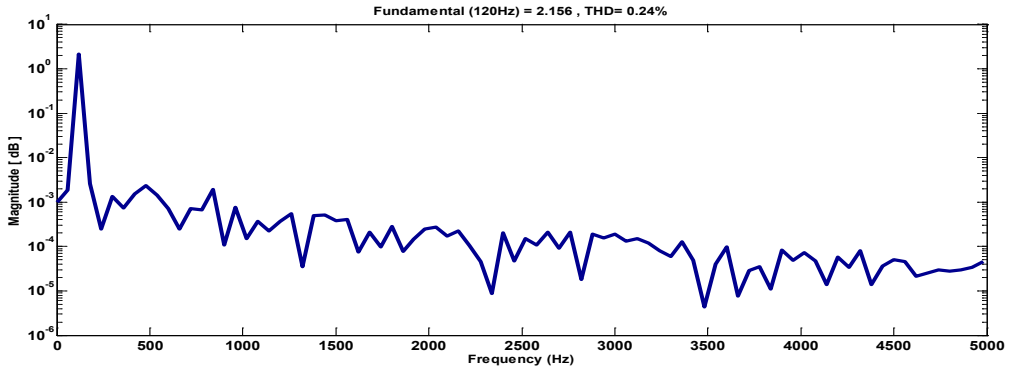


Figure 4.15: Upper load current frequency spectrum under linear load condition

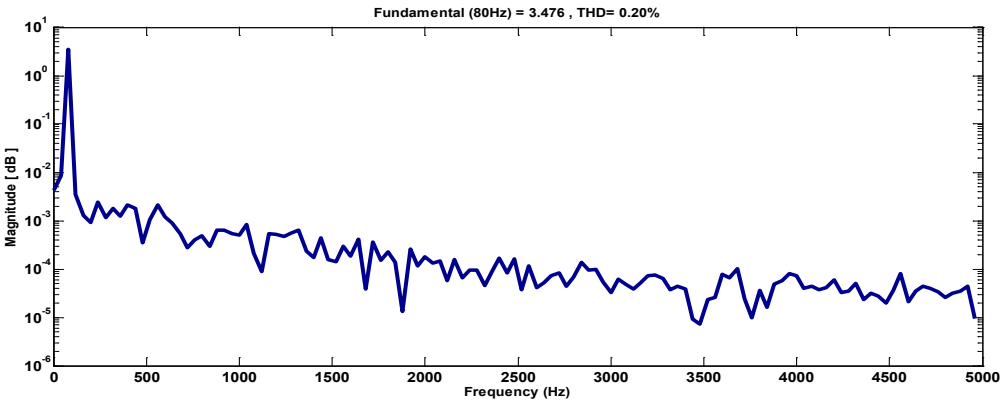


Figure 4.16: Lower load current frequency spectrum under linear load condition

Output filter inductor current for upper load side and lower load side is presented in Figure 4.17. Currents presented in Figure 4.17 are measured before filtering so it quite normal that these two currents contain high frequency components. Another important aspect is observer performance in predicting load current under linear load condition, which is shown in Figure 4.18. According to results, the estimated current accurately tracks the actual current with a small time delay.

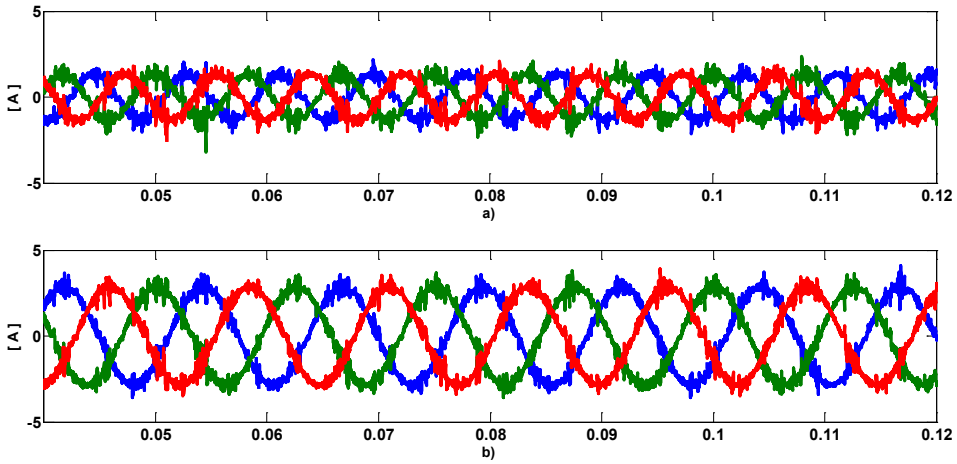


Figure 4.17: Output filter inductor current under linear load condition a) Upper inductor current waveform b) Lower inductor current waveform

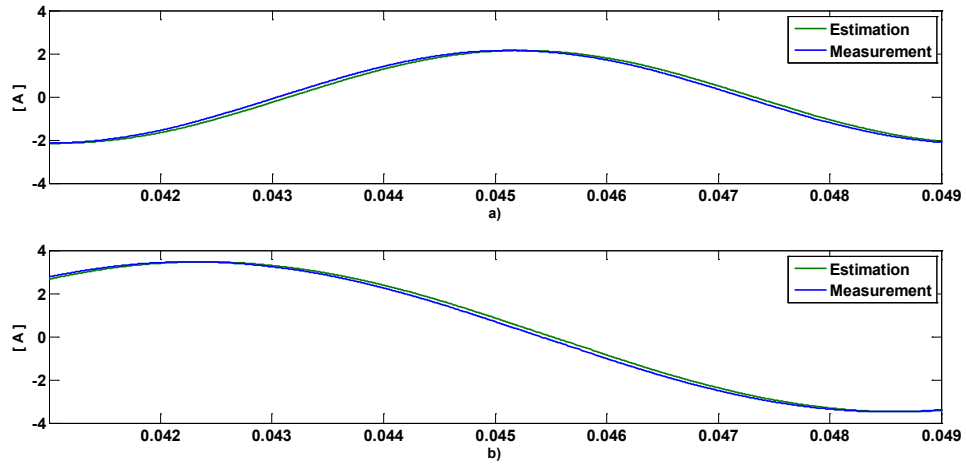


Figure 4.18: Load current estimation under linear load condition a) Upper load current estimation b) Lower load current estimation

In order to evaluate the controller and observer performance, two different load steps are applied. Figure 4.19 shows the dynamic behavior of the predictive controller and Figure 4.20 shows the phase plane plots during signal transition. Good reference tracking is observed.

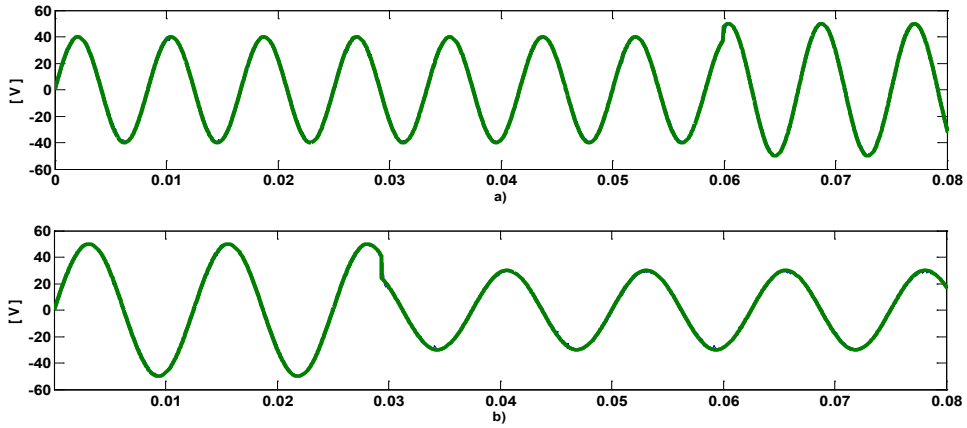


Figure 4.19: Dynamic response of predictive controller under linear load condition a) Upper output capacitor voltage b) Lower output capacitor voltage

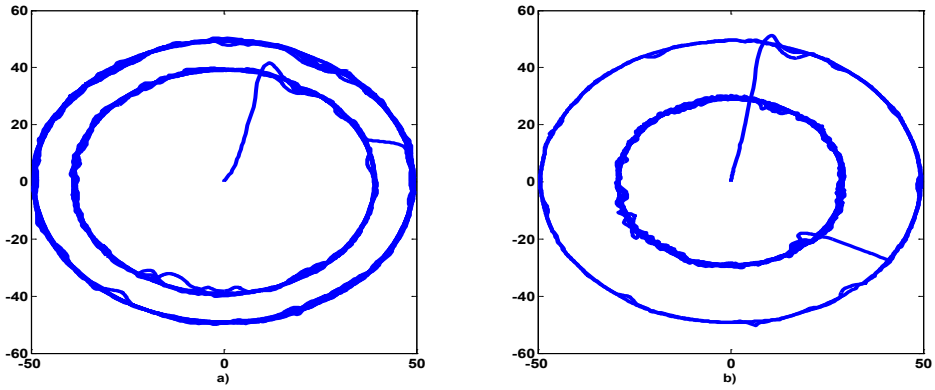


Figure 4.20: Phase plane plot for capacitor voltage a) Upper output capacitor voltage plot b) Lower output capacitor voltage plot

The first reference step is applied to lower load at time 0.03s and the second reference step is applied to the upper load at time 0.06s. According to Figure 4.21 and Figure 4.22, fast dynamic response is obtained and the controller maintains control each output capacitor voltage independently.

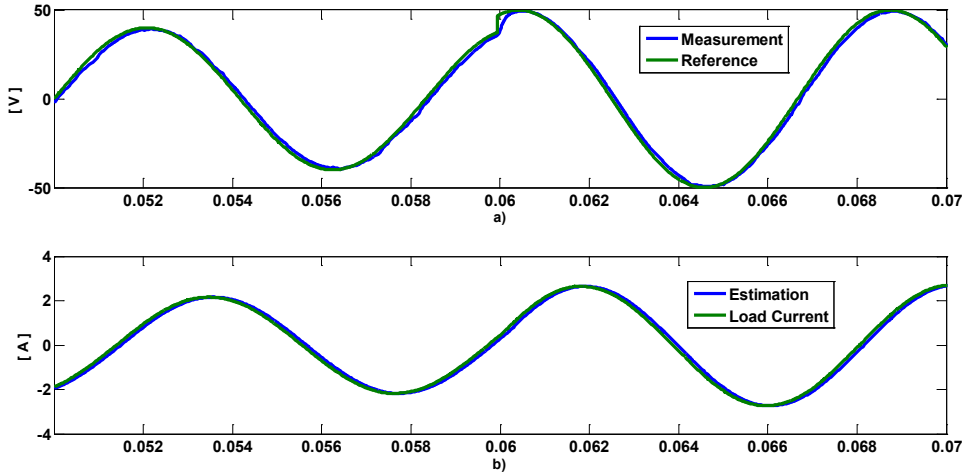


Figure 4.21: Dynamic behavior of upper observer and controller under linear load conditions a) Upper output capacitor voltage b) Upper load current estimation

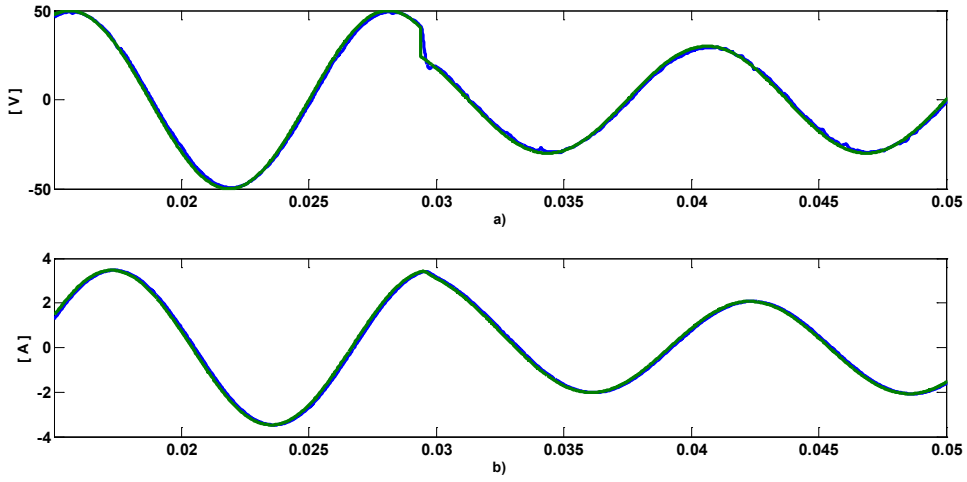


Figure 4.22: Dynamic behavior of lower observer and controller under linear load conditions a) Lower output capacitor voltage b) Lower load current estimation

4.4.2 NONLINEAR LOAD CONDITION

In power electronics applications, load may be nonlinear and controller must provide good voltage regulation for this case as well. In this work, a diode-bridge rectifier, shown in Figure 4.23, is used as a nonlinear load for upper load and lower load. Capacitor value and resistor values for diode-bridge rectifier are 2.8 mF and 54Ω.

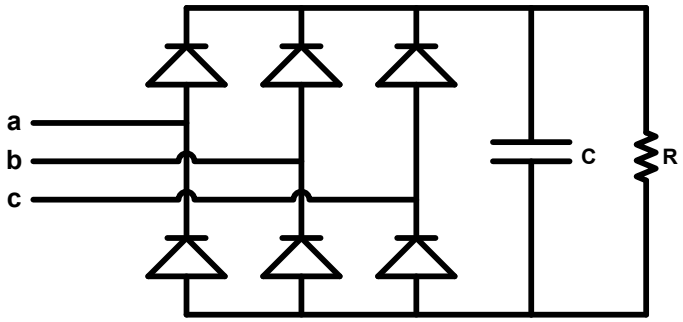


Figure 4.23: Diode-bridge rectifier

The measured output capacitor voltage and output current for upper load side and lower load side are shown in Figure 4.24 and Figure 4.25. The upper capacitor voltage reference is 50 V/120 Hz and the lower capacitor voltage reference is 40 V/60 Hz. In steady state, predictive controller can handle the two nonlinear loads and provide sinusoidal voltage to the load side.

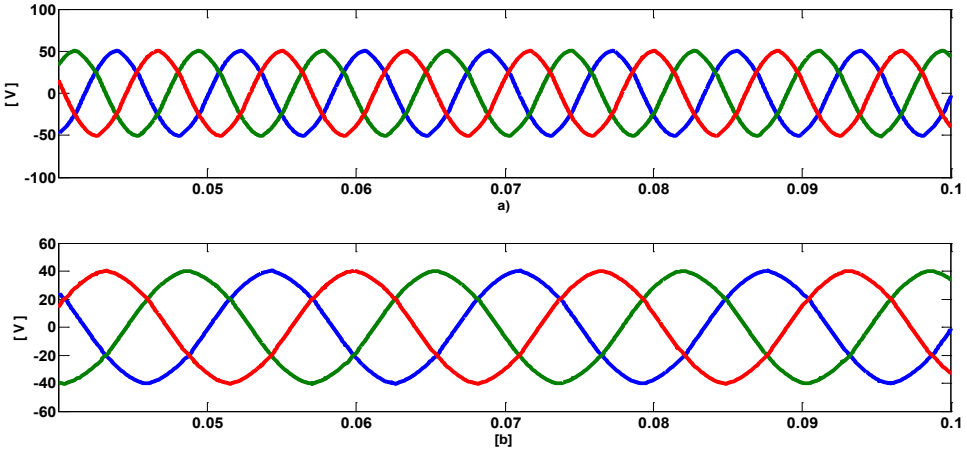


Figure 4.24: Output filter capacitor voltage under unbalanced load condition a) Upper capacitor voltage b) Lower capacitor voltage

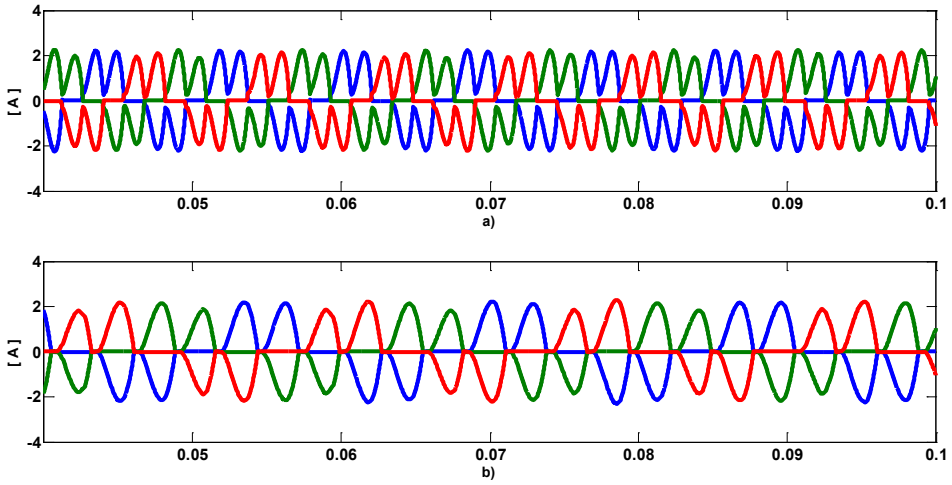
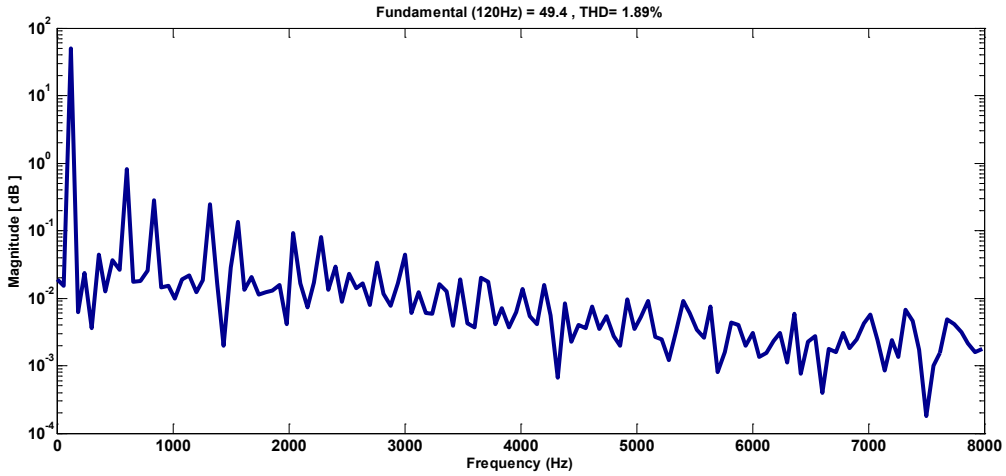
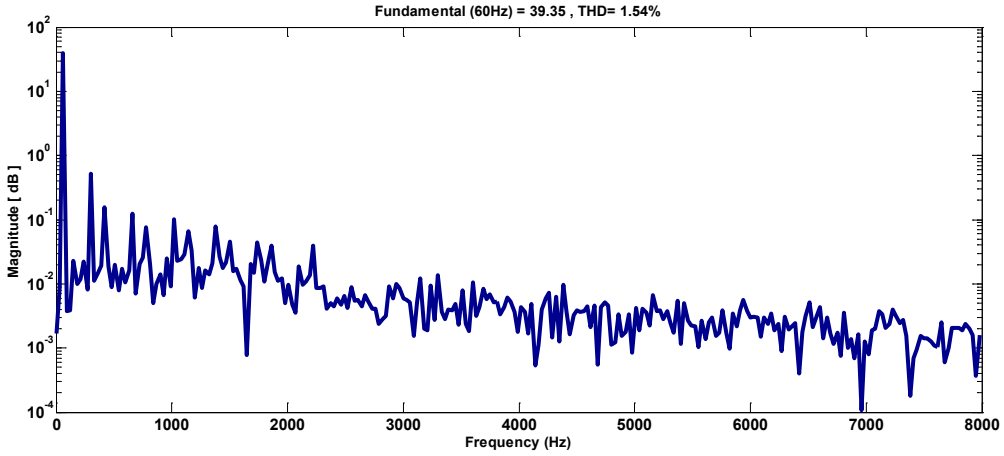


Figure 4.25: Output load current under unbalanced load condition a) Upper load current b) Lower load current

In order to evaluate the quality of output voltage, FFT was carried out up to 8 kHz to calculate the spectral content and frequency spectrum of capacitor voltage is presented in Figure 4.26. Magnitudes of frequency contents are presented in log scale. According to FFT results, upper output voltage THD is 1.89% and lower output voltage is 1.54%. The THD is mostly caused by the first few harmonics, even if high frequency do not drop off as fast as in the linear load case of Figure 4.13 and Figure 4.14.



a)



b)

Figure 4.26: Frequency spectrum of output voltage under nonlinear load condition a) Upper output voltage frequency spectrum b) Lower output voltage frequency spectrum

In conclusion, model predictive control strategy provides good output voltage for both upper and lower load. Output filter inductor current is shown in Figure 4.27. In order to evaluate the controller and observers performance, output capacitor voltage shown in Figure 4.28 and observer dynamic response shown in Figure 4.29.

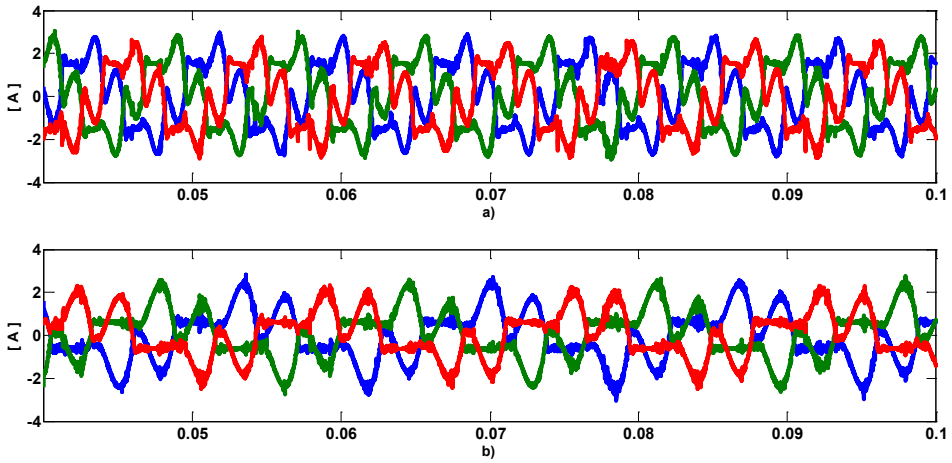


Figure 4.27: Filter inductor current under unbalanced load condition a) Upper filter current b)Lower filter current

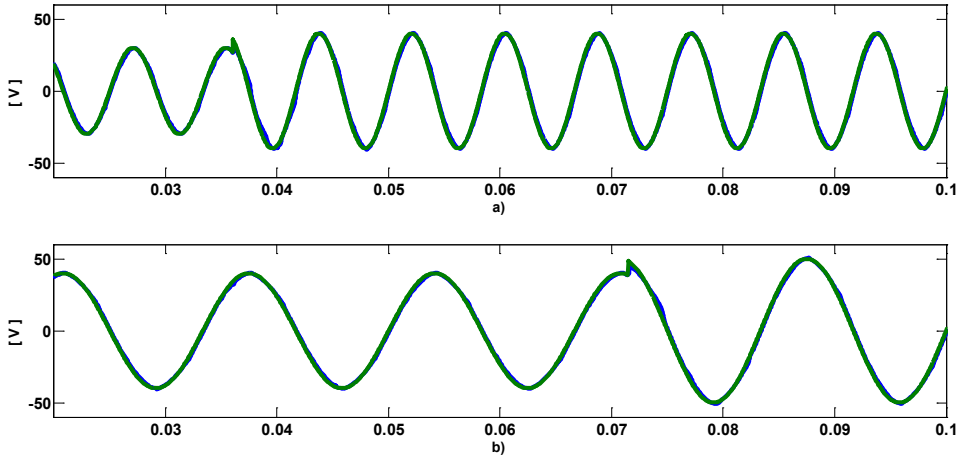


Figure 4.28: Dynamic response of predictive controller under unbalanced load condition a) Upper capacitor voltage b) Lower capacitor voltage

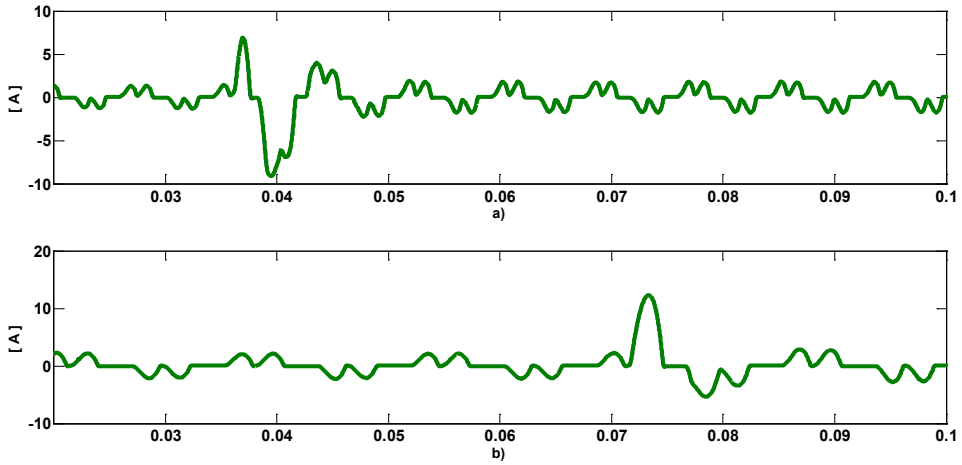


Figure 4.29: Dynamic response of observer under unbalanced load condition a) Upper load current estimation b) Lower load current estimation

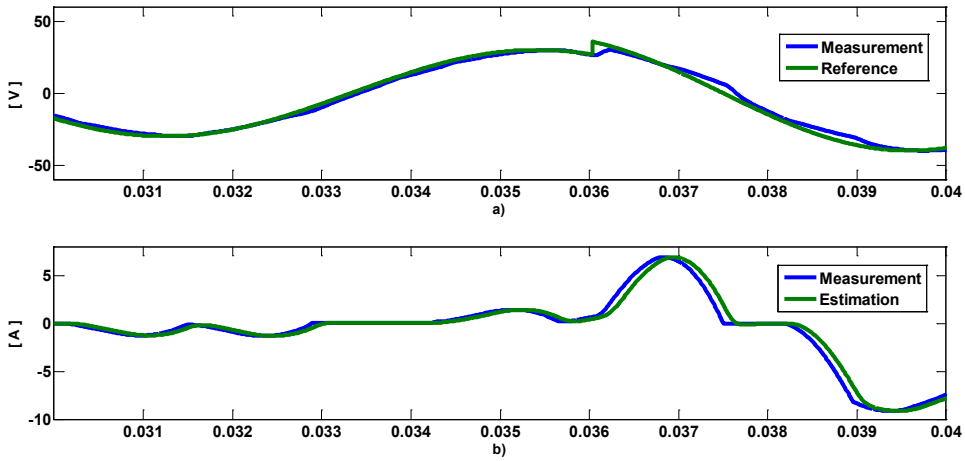


Figure 4.30: Step response of the system a) Upper capacitor voltage b) Upper load current estimation

Figure 4.30 and Figure 4.31 show the dynamic behavior of the predictive controller and observer response during large signal transitions. Step response waveforms show that step response time for upper load (system step at t=0.036) is 480 µs which corresponds to 12 sampling intervals and step response time for the lower load (system step at t=0.0715) is 200 µs which corresponds to 5 sampling intervals.

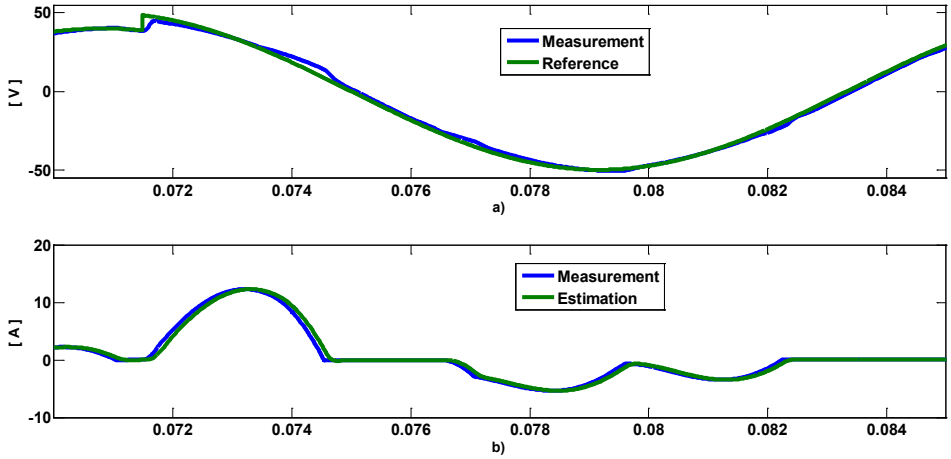


Figure 4.31: Step response of the system a) Lower capacitor voltage b) Lower load current estimation

4.5 SUMMARY

In this work, model predictive control of nine-switch inverter with output filter is presented. This control scheme uses the discrete-time model of the NSI and the output filter to determine the best suited switch by solving a multi-objective optimization problem. The proposed control scheme can control the two three-phase output voltages simultaneously and provides clean sinusoidal output voltages to the upper load and lower load. Two observers are used to estimate the two output load currents, eliminating the need for sensors for load current measurements.

The model predictive control technique is tested under both linear and nonlinear load conditions. Simulation results show that predictive control scheme performs well under different conditions. It provides fast dynamic response and good steady-state behavior. The main advantage of the predictive control lies in the ease of implementation

and flexibility. Different control objectives can easily be added to the cost function and controlled simultaneously.

In future work, control interaction between upper load and lower load under dynamic conditions will be investigated. Since the NSI has three common switches per leg, the upper load side and lower load side may interact.

CHAPTER 5

MODEL PREDICTIVE CONTROL FOR DUAL-OUTPUT INDIRECT MATRIX CONVERTER

5.1 INTRODUCTION

Dual-output indirect matrix converter is based on the traditional indirect matrix converter topology but the conventional six-switch inverter is replaced by a nine-switch inverter. This topology produces two-sets of three-phase ac loads since the nine switch inverter is a dual output inverter. Several modulation and control strategies have been proposed for this topology but these conventional modulation and control techniques are very complicated [27],[33]. In this work, a model predictive control scheme is proposed for dual-output indirect matrix converter. Different control objectives, like output load current and minimization of the instantaneous input reactive power, are considered and performance of the MPC technique is investigated. Model predictive control method is an interesting approach for this topology since three objectives need to be considered.

AC-AC power conversion systems have been widely used in industry [35]-[36]. In conventional conversion systems, i.e., ac-dc-ac systems, a dc-link energy storage element, such as an electrolytic capacitor, is required for balancing the instantaneous difference between input source power and output load power [54]. However, these energy storage elements are usually large in size and liable to cause reliability issues, thus

reducing power converter expected lifetime. Moreover, passive components may have a significant impact on the overall converter losses. For these reasons. eliminating the dc-link storage elements is desirable to improve reliability and efficiency.

The dual-output indirect matrix converter, see Figure 1.6, consists of two stages: the rectifier stage and the dual-output inverter stage. Since the rectifier stage is connected to the inverter stage without any energy storage element, fictitious dc-link voltage exist in between inverter stage and rectifier stage [53]. The important aspect is that the rectifier stage must provide positive voltage to the inverter stage and this constraint must be considered in the controller design. Otherwise input side of the inverter is shorted by the free-wheeling diodes of the inverter stage and the converter cannot work properly.

5.2 SYSTEM MODEL

With reference to Figure 1.6, the rectifier stage includes input filter to eliminate the high frequency component of the input currents and prevent over voltages. For the rectifier stage, producing positive dc-link voltage is critical for the proper operation of the inverter stage that it supplies. The interconnection matrix $\mathbf{T_{CSR}}$ is given by (5.1).

$$\mathbf{T_{CSR}} = [S_1 - S_4 \quad S_2 - S_5 \quad S_3 - S_6] \tag{5.1}$$

The input voltage $\mathbf{v_i}$ and the input current vector $\mathbf{i_i}$ are defined as (5.2) and (5.3), respectively.

$$\mathbf{v_i} = \begin{bmatrix} v_{iA} & v_{iB} & v_{iC} \end{bmatrix}^T \tag{5.2}$$

$$\mathbf{i_i} = \begin{bmatrix} i_{iA} & i_{iB} & i_{iC} \end{bmatrix}^T \tag{5.3}$$

The rectifier model is used to predict dc-link voltage v_{DC}. The dc-link voltage is given by (5.4).

$$v_{DC} = \mathbf{T}_{\mathbf{CSR}}^{\mathbf{T}} \mathbf{v}_{\mathbf{i}} \tag{5.4}$$

The relationship between the input and dc-link current is given by (5.5).

$$\mathbf{i}_{i} = \mathbf{T}_{\mathbf{CSR}} i_{DC} \tag{5.5}$$

For proper rectifier operation, the input phases of the rectifier cannot be short circuited. Thus, only nine switching combinations are valid for the rectifier stage. For the inverter stage, all switches on the same leg cannot be turned on at the same time to avoid dc bus short circuit. Another switching restriction is that at least two switches on the same leg must be on, so that floating of connected load is avoided. Considering these two switching restrictions, the inverter stage has 81 possible switching combinations, but since some of them are redundant, only 45 of these switching states are sufficient to control the two ac loads independently. To describe the inverter model, two interconnection matrices are defined as (5.6) and (5.7).

$$\mathbf{T}_{\mathbf{U}} = \begin{bmatrix} S_{AU} & S_{BU} & S_{CU} \end{bmatrix} \tag{5.6}$$

$$\mathbf{T}_{\mathbf{L}} = \begin{bmatrix} (1-S_{AL}) & (1-S_{BL}) & (1-S_{CL}) \end{bmatrix} \tag{5.7}$$

The relationship between output upper load voltage and dc-link voltage is defined as in (5.8) and the relationship between output lower load voltage and dc-link voltage is defined as in (5.9).

$$\mathbf{v}_{\mathbf{o\_up}} = \frac{V_{DC}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \mathbf{T}_{\mathbf{U}}^{\mathbf{T}} \tag{5.8}$$

$$\mathbf{v}_{\mathbf{o\_low}} = \frac{V_{DC}}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix} \mathbf{T}_{\mathbf{L}}^{\mathbf{T}} \tag{5.9}$$

The dc-link current is defined as

$$i_{DC} = \mathbf{T_U}\begin{bmatrix} i_{oa\_up} \\ i_{ob\_up} \\ i_{oc\_up} \end{bmatrix} + \mathbf{T_L}\begin{bmatrix} i_{oa\_low} \\ i_{ob\_low} \\ i_{oc\_low} \end{bmatrix} \tag{5.10}$$

The future values of upper load current and lower load current are given by

$$i_{o\_up}(k+1) = \frac{Ts}{L_{up}} v_{o\_up}(k) + (1 - \frac{R_{up} Ts}{L_{up}}) \tag{5.11}$$

$$i_{o\_low}(k+1) = \frac{Ts}{L_{low}} v_{o\_low}(k) + (1 - \frac{R_{low} Ts}{L_{low}}) \tag{5.12}$$

The derivation process of the prediction equation of the instantaneous reactive power of dual-output indirect matrix converter is exactly the same as for the direct matrix converter.

5.3 Model Predictive Control Scheme

Model predictive control solves a cost function related multiple control goals by making an exhaustive search over the finite control set and determining the optimal control action. The choice of the objective function is critical since it determines the desired system behavior. In this work, the controller aims to minimize the load current errors of two ac loads and input instantaneous reactive power. Upper load and lower load current tracking terms are defined as in (5.13) and (5.14).

$$g_1 = \sqrt{\left|i^*_{o\alpha\_up}(k+1) - i_{o\alpha\_up}(k+1)\right|^2 + \left|i^*_{o\beta\_up}(k+1) - i_{o\beta\_up}(k+1)\right|^2} \tag{5.13}$$

$$g_2 = \sqrt{\left|i^*_{o\alpha\_low}(k+1) - i_{o\alpha\_low}(k+1)\right|^2 + \left|i^*_{o\beta\_low}(k+1) - i_{o\beta\_low}(k+1)\right|^2} \tag{5.14}$$

The reactive power term is expressed as

$$g_3 = \left| Q^*(k+1) - Q(k+1) \right| \tag{5.15}$$

For reactive power minimization, future reference reactive power $Q^*(k+1)$ is set to zero. The cost function for this system contains these three error terms and it is defined as

$$g = Ag_1 + Bg_2 + Cg_3 \tag{5.16}$$

Predictive control scheme is shown in Figure 5.1 and reference values for load currents and reactive power are denoted by "*". Constants A, B and C are the weighting factors. Three phase load currents are calculated in α-β frame and costs for the two ac load currents are evaluated in this frame. Producing a positive dc-link voltage is necessary for the operation of the NSI stage.

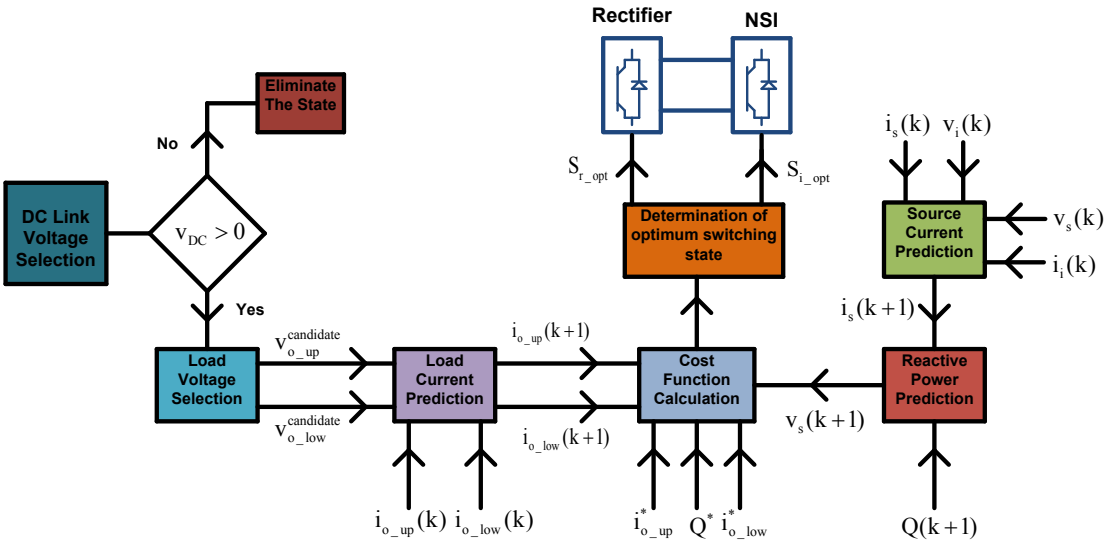


Figure 5.1: Predictive control scheme for dual-output indirect matrix converter

The switching state elimination process is responsible for selecting rectifier switching states that provide positive dc-link voltage. Figure 5.2 shows the flow diagram of the switching state elimination process that provides the positive voltage then used for calculating the future load current. At instant k the input voltage vector and the output

current vector are measured. The switching state elimination process identifies valid rectifier switch combinations and the corresponding value of the DC link voltage is sent to Load Current Prediction block that calculates future output current values. The determination of optimum switching state block selects the best switch combination. The process is repeated for all possible switch combinations and the optimal switch combination is found and applied to the converter.

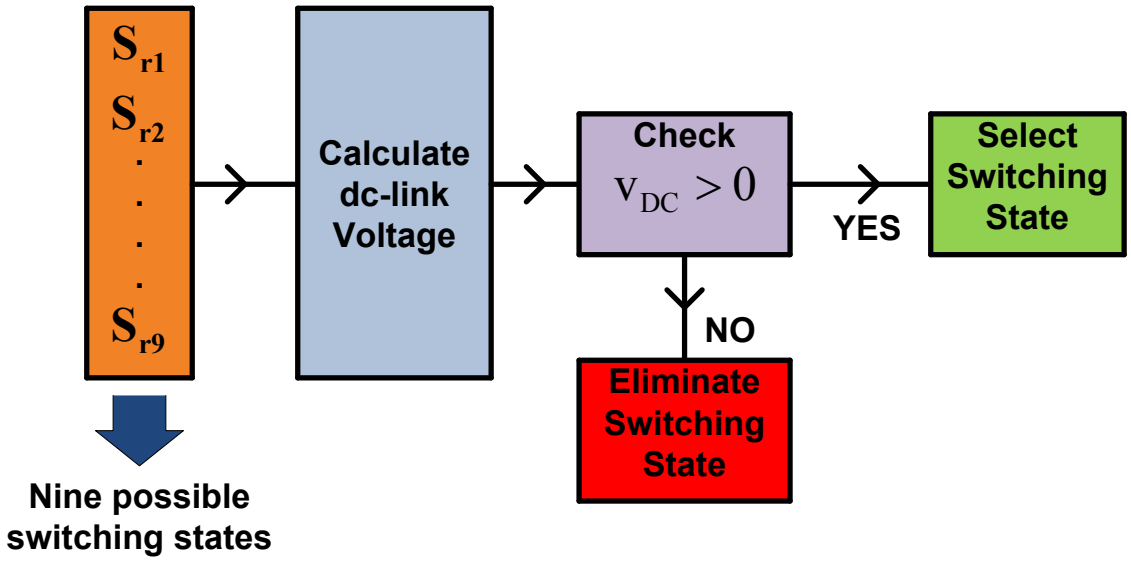


Figure 5.2: Switching state elimination process

5.4 Simulation Results

A simulation study was performed to validate the proposed method. Simulations are carried out using MATLAB/Simulink to validate the proposed method. Simulation parameters are listed in Table 5.1. Upper load current, lower load current and source current are shown in Figure 5.3. In Figure 5.3, supply voltage for only one phase is shown. FFT analysis is carried out to analyze the quality of the load current and source

current. According to simulation results, good output load current tracking is obtained. Upper load current THD is 2.37%, which is shown in Figure 5.4, and lower load current THD is 2.33%, see Figure 5.5. Minimization of the instantaneous reactive power is achieved and source current THD is 26.59%, which is shown in Figure 5.6. In order to evaluate dynamic behavior of the predictive control technique. the system step response is shown in Figure 5.7. Step response waveform shows that step response time for upper load (system step at t= 0.027) is 500 µs which corresponds to 25 sampling steps and step response time for the lower load(system step at t=0.054) is 800 µs which corresponds to 40 system steps. Figure 5.7 shows that predictive controller can provide both excellent dynamic and steady-state performance.

Table 5.1: Simulation Parameters

Parameters	**Values**
Supply Voltage	220V/60Hz
Sampling Time	20 µs
Upper Load Current Reference	4A/120Hz
Lower Load Current Reference	7A/30Hz
Filter resistor	0.5 Ω
Filter inductor	145 µH
Filter capacitor	32 µF
Load resistor	10 Ω
Load inductor	30 mH
A	1
B	1
C	0.015

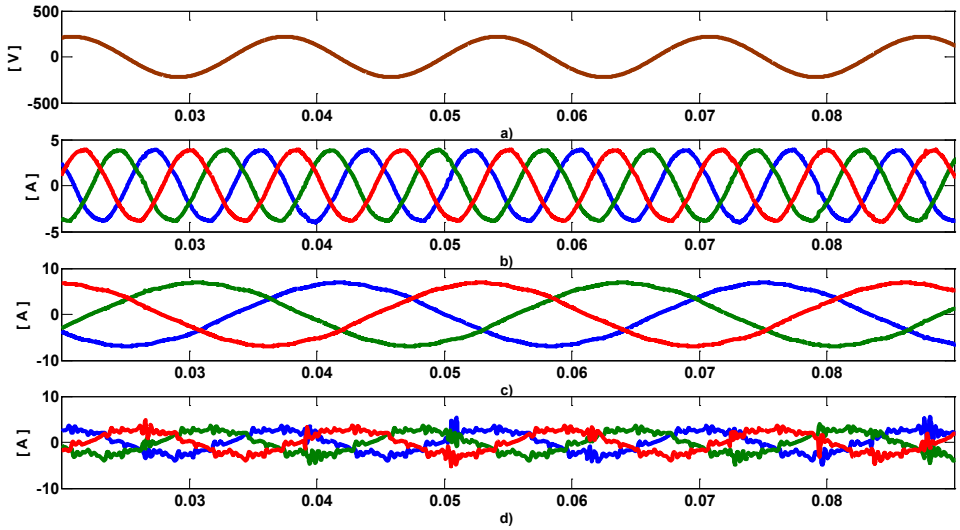


Figure 5.3: Simulation results for dual-output indirect matrix converter a) Supply voltage b) Upper load current c) Lower load current d) Source current

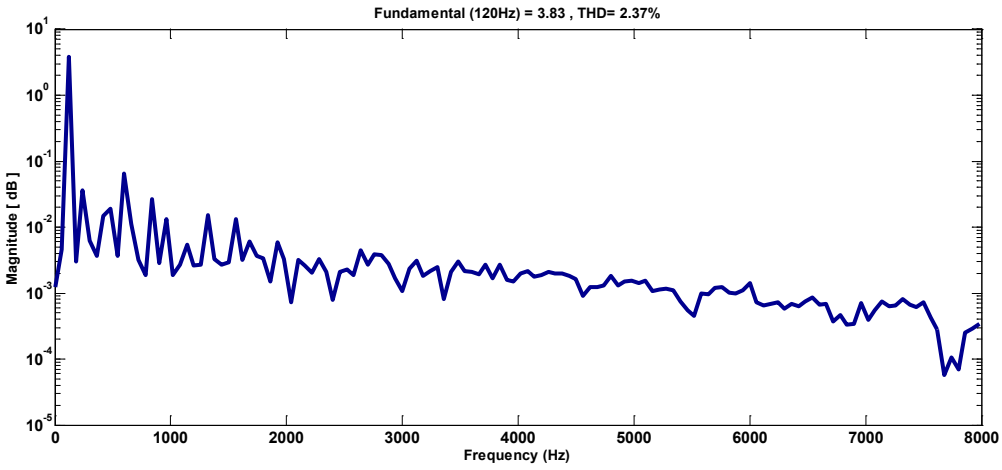


Figure 5.4: Frequency spectrum of upper load current

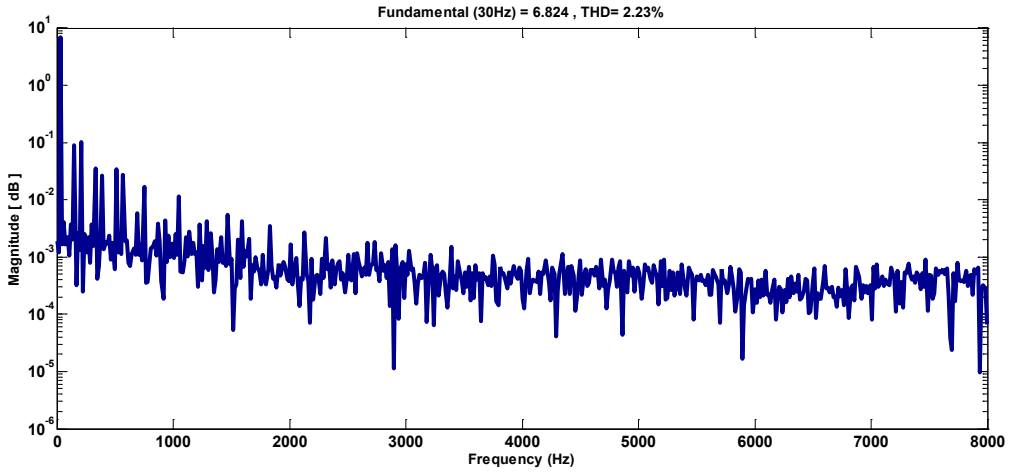


Figure 5.5: Frequency spectrum of lower load current

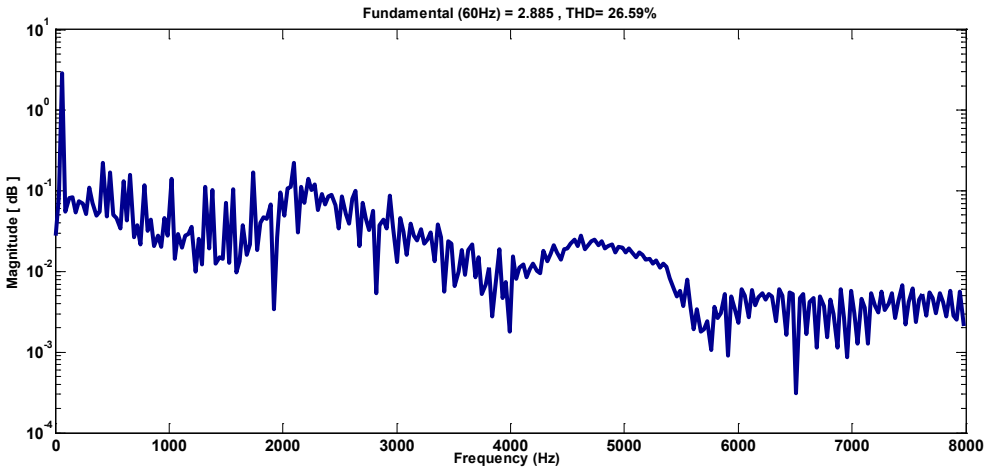


Figure 5.6: Frequency spectrum of source current

Phase plane plot for upper load current and lower load current are shown in Figure 5.8 where horizontal axis is the real component of the associated vector and vertical axis is imaginary component of the associated vector.

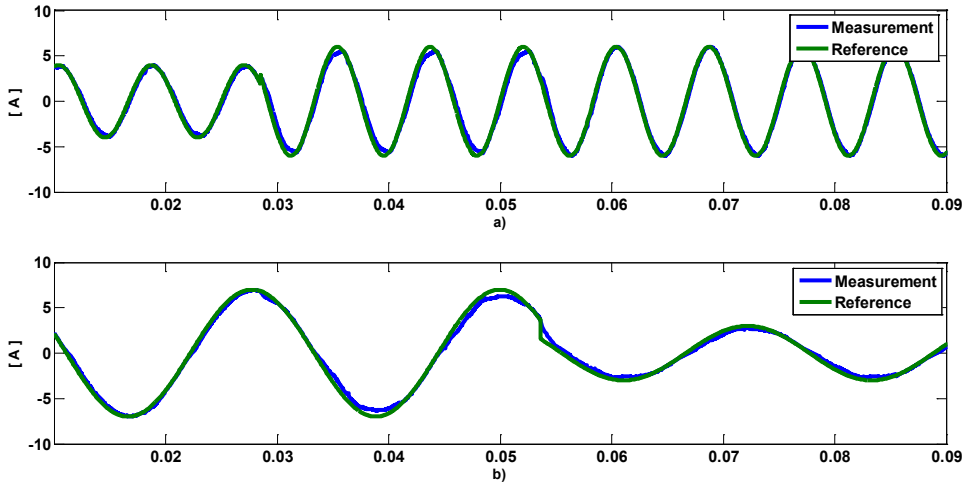


Figure 5.7: Dynamic response of proposed control scheme a) Upper load current b) Lower load current

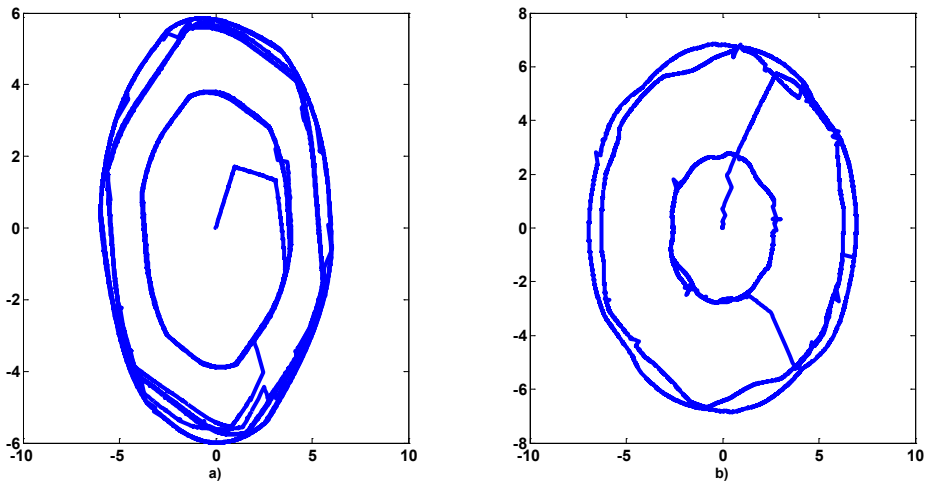


Figure 5.8: Phase plane plot of output load current a) Upper load current b) Lower load current

Model predictive control technique is able to control two ac loads even when their frequencies and magnitudes are different. Two ac loads are controlled independently by solving single multi-objective cost function. The proposed method always provides positive dc-link voltage. Figure 5.9 shows that dc-link voltage is always positive. The state elimination process in the control scheme always provides positive dc-link voltage,

which is important for proper operation. The main idea of the state elimination process is that switching combinations of rectifier stage that generate a negative dc-link voltage are eliminated and future load current for upper load and lower load are calculated using only proper switching combinations of the rectifier stage.

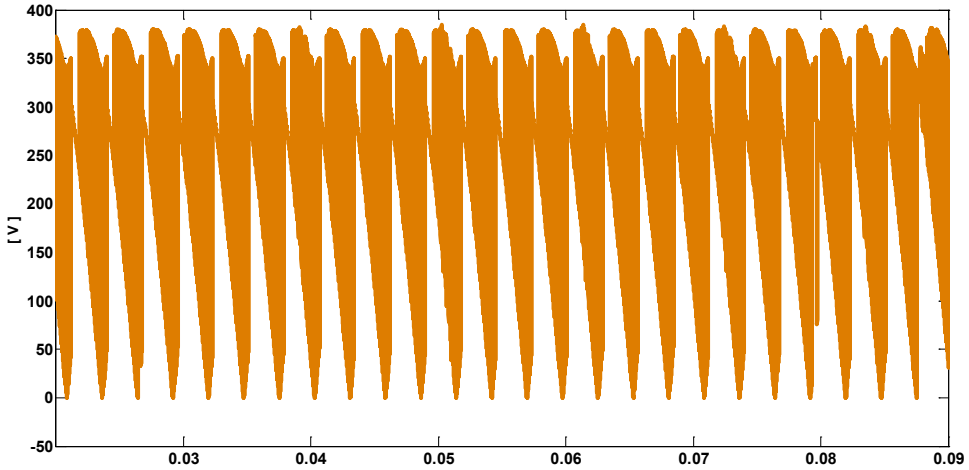


Figure 5.9: DC-link voltage

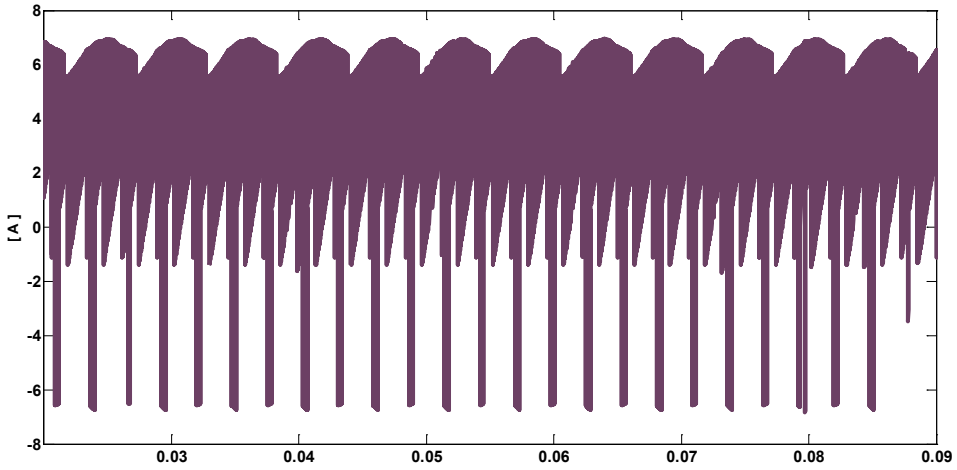


Figure 5.10: DC-link current

Whereas the DC-link voltage has to be positive, the DC-link current can be positive or negative, which is shown in Figure 5.10. Figure 5.11 and Figure 5.12 show the change in reactive power and supply current due to reactive power control. Weighting factor C is initially set at zero so that reactive power is not controlled. Under this condition input current is significantly distorted, see Figure 5.12, and reactive power is larger, see Figure 5.11. When reactive power control is introduced at time t=0.045s by setting C=0.015, reactive power decreases significantly and supply current waveform quality improves.

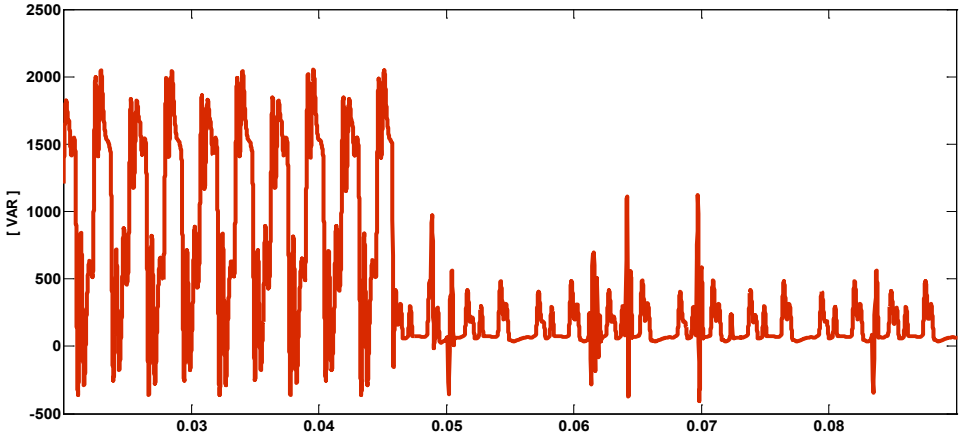


Figure 5.11: Instantaneous reactive power

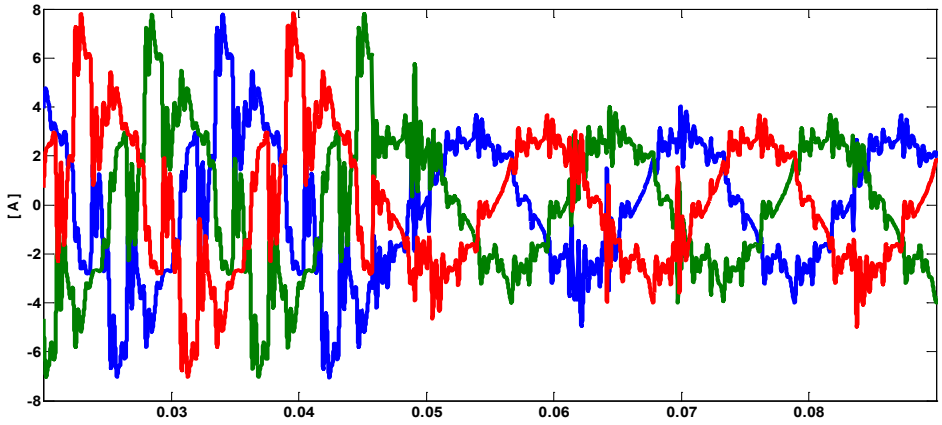
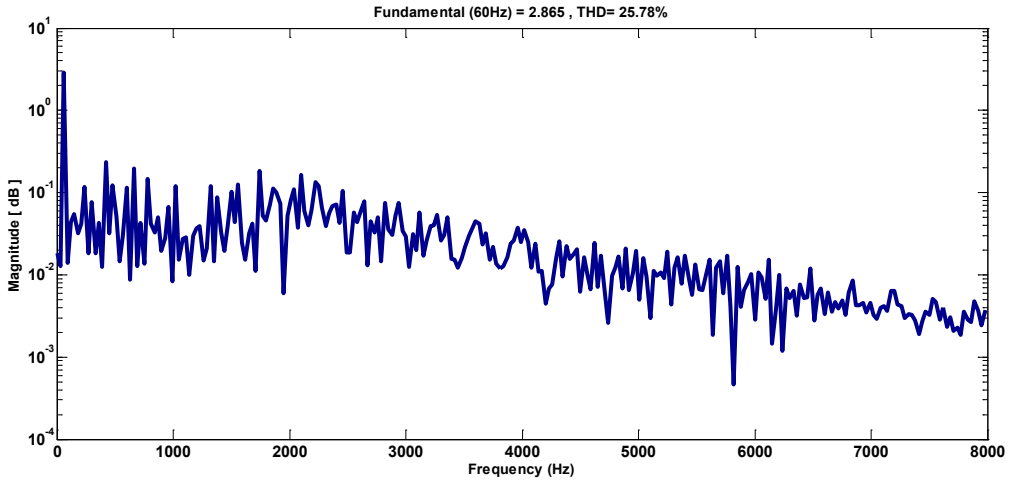
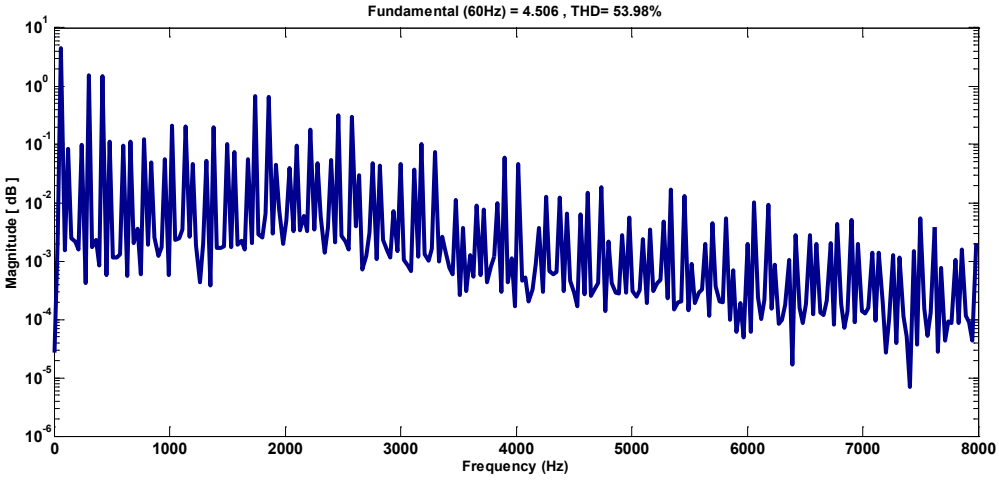


Figure 5.12: Supply current

Frequency spectrum of input current with reactive power control and without reactive power control is shown in Figure 5.13a-b. According to FFT results, input current THD is 25.78% with reactive power control and THD is 53.98% without reactive power control.



a)



b)

Figure 5.13: Frequency spectrum of input current a) Spectral contents with reactive power control b) Spectral content without reactive power control

5.5 SUMMARY

In this work, model predictive control of dual output indirect matrix converter is presented. This control scheme uses a discrete-time model of the converter and predicts load current and reactive power to determine the best suited switching combination by solving a multi-objective optimization problem. Model predictive control technique provides fast dynamic response and good steady-state behavior.

Model predictive control technique is tested for different control objectives and it performs well under different conditions. Simulation results show that good system performance was obtained with predictive control scheme in steady state and under transient conditions. The main advantage of the predictive control approach is easy implementation and flexibility. New control objectives can be added in the cost function and controlled simultaneously.

CHAPTER 6

CONCLUSIONS AND FUTURE WORK

6.1 CONCLUSIONS

This dissertation presents finite control set model predictive method for power converters. The model predictive control theory is being used in many fields of science and it has received attention from power electronics society last several decades. The predictive control approach could be competitive with well-known control techniques, such as linear control, deadbeat control or sliding mode control. This work considers real-time implementation issues and provides solutions to several disadvantages of model predictive control technique.

In Chapter 2, new real-time implementation of model predictive control method for direct matrix converter is presented. The proposed method reduces the execution time significantly and improves controller performance. FPGA-based implementation eliminates the need for two separate digital control platforms and improves reliability. Parallel computation capability of FPGA device is exploited and all required control calculations and the implementation of the safe commutating scheme and protections are all performed in the FPGA.

In Chapter 3, novel model predictive control technique based on switching state elimination is presented. The proposed method uses control constraints and eliminations

conditions instead of using weighting factors to control several control objectives simultaneously. Adjusting weighting factor process for multi-objective optimization problem is eliminated and novel easy tuning procedure for selecting control constraints is proposed. In proposed method, control constraints and elimination conditions have a clear physical interpretation and they are independent from power level.

In Chapter 4, model predictive control for nine-switch inverter is presented. The dual output nine-switch inverter control typically uses complicated modulation scheme and multi-loop control approach. The main advantage of the proposed method is that it requires a single control loop to control two ac loads and provides faster dynamic response compared to the conventional multi-loop control method using PI controllers. Observer estimates load currents and the need for load model information or load current measurement is eliminated. The proposed method is independent from the load and provides clean waveforms for both linear and nonlinear unknown loads.

In Chapter 5, model predictive control scheme for dual output indirect matrix converter is presented. The conventional control scheme has two separate controllers, one for rectifier stage and one for inverter stage. Conversely, the proposed method controls the whole system using a single loop and it requires only a single controller. It is less complicated compared to conventional control technique and easy to implement. Two load currents and reactive power are controlled by solving a single optimization problem and gate signals are directly generated by the predictive controller. The proposed method does not use a modulator, so complicated modulation scheme is eliminated for dual output indirect matrix converter topology.

6.2 FUTURE WORK

The results of this thesis have the potential to be extended in several directions:

1) It is important to compare the proposed real-time implementation for direct matrix converter to conventional real-time implementation technique in terms of several performance criteria, such as load current THD, source current THD and dynamic response. It would be useful to show benefits of FPGA-based predictive control implementation by showing experimental comparison results between conventional real-time implementation method and the proposed method.

2) The proposed model predictive control schemes of nine switch inverter and dual output indirect matrix converter, presented in Chapter 4 and Chapter 5, can be validated experimentally. This experimental validation is critically important to show advantages of these model predictive control schemes and some implementation issues can be considered. An FPGA implementation would be of particular interest.

REFERENCES

[1] Cortes P., Kazmierkowski M., Kennel R., Quevedo D., Rodriguez J., "Predictive Control in Power Electronics and Drives", *IEEE Transaction on Industrial Electronics,* Vol.55, No.12, pp. 4312-4324, December 2008

[2] Rodriquez J., Kazmierkowski M., Espinoza J., Zanchetta P., Abu-Rub H., Young H., Rojas C., "State of the Art of Finite Control Set Model Predictive Control in Power Electronics", *IEEE Transaction on Industrial Informatics,* Vol. 9, No.2, pp. 1003-1016, May 2013

[3] Kouro S., Cortes P., Vargas R., Ammann U., Rodriquez J., "Model Predictive Control - A Simple and Powerful Method to Control Power Converters", *IEEE Transaction on Industrial Electronics,* Vol. 56, No.6, pp. 1826-1838, June 2009

[4] Mariethoz S., Morari M., "Explicit Model-Predictive Control of a PWM Inverter With an LCL Filter", *IEEE Transactions on Industrial Electronics,* Vol. 56, No. 2, pp. 389-399, February 2009

[5] Barros D., Silva F., Jesus E., "Fast-Predictive Optimal Control of NPC Multilevel Converters", *IEEE Transactions on Industrial Electronics,* Vol. 60, No. 2, pp. 619-627, February 2013

[6] Beccuti A., Kvasnica M., Papafotiou G., Morari M., "A Decentralized Explicit Predictive Control Paradigm for Parallelized DC-DC Circuits", *IEEE Transactions on Control Systems Technology,* Vol. 21, No. 1, pp. 136-148, January 2013

[7] Karamanakos P., Geyer T., Manias S., "Direct Model Predictive Current Control Strategy of DC-DC Boost Converters", *IEEE Journal of Emerging and Selected Topics in Power Electronics",* Vol. 1, No. 4, pp. 337-346, December 2013

[8] Mo W., Loh P.C., Blaabjerg F., "Model predictive control for Z-source power converter", 2011 IEEE 8th International Conference on Power Electronics - ECCE Asia, Korea,

[9] Davari A., Khaburi, Kennel R., "Using a Weighting Factor Table for FCS-MPC of Induction Motors with Extended Prediction Horizon", IEEE Industrial Electronics, IECON 2006

[10] Cortes P., Wilson A., Kouro S., Rodriquez J., Abu-Rub H., "Model Predictive Control of Multilevel Cascaded H-Bridge Inverters", *IEEE Transactions on Industrial Electronics,* Vol. 57, No. 8, pp. 2691-2699, August 2010

[11] Perez M., Cortes P., Rodriquez J., "Predictive Control Algorithm Technique for Multilevel Asymmetric Cascaded H-Bridge Inverters", *IEEE Transactions on Industrial Electronics,* Vol. 55, No. 12, December 2008

[12] Quevedo D., Aguilera R., Perez M., Cortes P., Lizana R., "Model Predictive Control of an AFE Rectifier with Dynamic References", *IEEE Transactions on Power Electronics,* Vol. 27, No. 7, pp. 3128-3136, July 2012

[13] Cortes P., Vattuone L., Rodriquez J., Duran M., " A Method of Predictive Current Control with Reduced Number of Calculations for Five-Phase Voltage Source Inverters", IEEE Industrial Electronics, IECON 2006

[14] Rodriquez J., Pontt J., Correa P., Lezana P., Cortes P., "Predictive Power Control of an AC/DC/AC Converter", IEEE Industry Applications Society Annual Meeting 2005

[15] Perez M., Rodriquez J., Fuentes E., Kammerer F., "Predictive Control of AC-AC Modular Multilevel Converters", *IEEE Transactions on Industrial Electronics,* Vol. 59, No. 7, pp. 2832-2839, July 2012

[16] Acuna P.,Moran L., Rivera M., Dixon J., Rodriquez J., "Improved Active Power Filter Performance for Renewable Power Generation Systems", *IEEE Transactions on Power Electronics,* Vol.29, No. 2, pp. 687-694, February 2014

[17] Prieto J., Riveros J., Bogado B., Barrero F., Toral S., Cortes P., "Electric propulsion Technology based in Predictive Direct Torque Control and Asymmetrical Dual Three-Phase Drives", 2010 13th IEEE Annual Conference on Intelligent Transportation Systems, Madeira, Portugal

[18] Vazguez S., Leon J., Franquelo L., Carrasco J., Dominguez E., Cortes P., Rodriquez J., "Comparison Between FS-MPC Control Strategy for an UPS inverter application in α-β and abc frames", 2010 IEEE International Symposium on Industrial Electronics

[19] Cortes P., Rodriquez J., Vargas R., Ammann U., "Cost Function-Based Predictive Control for Power Converters", 2006 32nd Annual Conference on IEEE Industrial Electronics

[20] Rodriquez J., Kennel R., Espinoza J., Trincado M., Silva C., Rojas C., " High-Performance Control Strategies for Electrical Drives: An Experimental Assessment", *IEEE Transactions on Industrial Electronics,* Vol. 59, No. 2, pp. 812-820, February 2012

[21] Rodriquez J., Pontt J., Silva C., Correa P., Lezana P., Cortes P., Ammann U., "Predictive Current Control of a Voltage Source Inverter", *IEEE Transactions on Industrial Electronics,* Vol. 54, No. 1, pp. 495-503, February 2007

[22] Rivera M., Rodriquez J., Wu B., Espinoza J., Rojas C., "Current Control for an Indirect Matrix Converter with Filter Resonance Mitigation", *IEEE Transactions on Industrial Electronics,* Vol. 59, No. 1, pp. 71-79, January 2012

[23] Cortes P., Vattuone L., Rodriquez J., "Predictive Current Control with Reduction of Switching Frequency for Three Phase Voltage Source Inverters", 2011 IEEE International Symposium on Industrial Electronics, pp. 1817-1822

[24] Alesina A., Venturini, "Analysis and design of optimum nine-switch direct AC AC conversion", *IEEE Transactions on Power Electronics,* Jan 1989

[25] Kominami T., Fujimoto Y., " A novel nine-switch inverter for independent control of two three-phase loads", IEEE Industry Applications Society Annual Conference (IAS), 2007, pp. 2346-2350

[26] Dehghan M., Mohamadian M., Rajaei A., Yazdian A., "Full Modeling a Series HEV Based on BZS-NSI", 2011 2nd Power Electronics, Drive Systems and Technologies Conference

[27] Liu X., Wang P., Loh P., Blaabjerg F., "A Compact Three-Phase Single-Input/Dual-Output Matrix Converter", *IEEE Transactions on Industrial Electronics,* Vol. 59, No. 1, pp. 6-16, January 2012

[28] Nguyen T., Lee H., "Dual Three-Phase Indirect Matrix Converter With Carrier-Based PWM Method", *IEEE Transactions on Power Electronics,* Vol. 29, No. 2, pp. 569-581, February 2014

[29] Dehghan M., Mohamadian M., Yazdian A., Ashrafzadeh F., "A Dual-Input-Dual-Output Z Source Inverter", *IEEE Transactions on Power Electronics,* Vol. 25, No. 2, pp. 360-368, February 2010

[30] Dehghan M., Amiri A., Mohamadian M., Andersen M., "Modular space-vector pulse-width modulation for nine-switch converters", IET Power Electronics

[31] Dehghan M., Mohamadian M., Yazdian A., "Hybrid Electric Vehicle Based on Bidirectional Z-Source Nine-Switch Inverter", *IEEE Transactions on Vehicular Technology,* Vol. 59, No.6, pp. 2641-2653, July 2010

[32] Dehghan M., Mohamadian M., Yazdian A., Ashrafzadeh F., "Space Vector Modulation for Nine-Switch Converters", *IEEE Transactions on Power Electronics,* Vol. 25, No. 6, pp. 1488-1496, June 2010

[33] Nguyen T., Lee H., "A New SVM Method for an Indirect Matrix Converter With Common-Mode Voltage Reduction", *IEEE Transactions on Industrial Informatics,* Vol. 10, No. 1, pp. 61-72, February 2014

[34] Pena R., Cardenas R., Reyes E., Clare J., Wheeler P., "A Topology for Multiple Generation System With Doubly Fed Induction Machines and Indirect Matrix Converter", *IEEE Transactions on Industrial Electronics,* Vol. 56, No. 10, pp. 4181-4193, October 209

[35] Kolar J., Friedli T., Rodriquez J., Wheeler P., "Review of Three-Phase PWM AC-AC Converter Topologies", *IEEE Transactions on Industrial Electronics,* Vol. 58, No. 11, pp. 4988-5008, November 2011

[36] Loh P., Blaabjerg F., Gao F., Baby A., Tan D., " Pulsewidth Modulation of Neutral-Point-Clamped Indirect Matrix Converter", *IEEE Transactions on Industry Applications,* Vol. 44, No. 6, pp. 1805-1814, November 2008

[37] Liu X., Loh P., Wang P., Blaabjerg F., Tang Y., Al-Ammar A., "Distributed Generation Using Indirect Matrix Converter in Reserve Power Mode", *IEEE Transactions on Power Electronics,* Vol. 28, No. 3, pp. 1072-1082, March 2013

[38] Karaman E., Farasat M., Trzynadlowski A., "A Comparative Study of Series Cascaded Z-Source Matrix Converters", *IEEE Transactions on Industrial Electronics,* Vol. 61, No. 10, pp. 5164-5173, October 2014

[39] Miranda H., Cortes P., Yuz J., Rodriquez J., "Predictive Torque Control of Induction Machines Based on State-Space Models", *IEEE Transactions on Industrial Electronics,* Vol. 56, No.6, pp. 1916-1924, June 2009

[40] Cortes P., Kouro S., La Rocca B., Vargas R., Rodriquez J., Leon J., Vazquez S., Franquelo L., "Guidelines for weighting factors design in Model Predictive Control of power converters and drives", IEEE International Conference on Industrial Technology, 2009

[41] Vargas R., Ammann U., Rodriguez J., "Predictive Approach to Increase Efficiency and Reduce Switching Losses on Matrix Converters", *IEEE Transactions on Power Electronics,* Vol. 24, No. 4, pp. 894-902, April 2009

[42] Rivera M., Rodriquez J., Wheeler P., Rojas C., Wilson A., Espinoza J., "Control of a Matrix Converter With Imposed Sinusoidal Source Currents", *IEEE Transactions on Industrial Electronics,* Vol. 59, No. 4, pp. 1939-1949, April 2012

[43] Rodriquez J., Espinoza J., Rivera M., Villarroel F., Rojas C., "Predictive Control of Source and Load Currents in a Direct Matrix Converter", IEEE International Conference on Industrial Technology, 2010

[44] Rivera M., Rodriquez J., Espinoza J., Friedli T., Kolar J., Wilson A., Rojas C., "Imposed Sinusoidal Source and Load Currents for an indirect Matrix Converter", *IEEE Transactions on Industrial Electronics,* Vol. 59, No. 9, pp. 3427-3435, September 2012

[45] Wheeler P., Clare J., Empringham L., Bland M., Apap M., "Gate Drive Level Intelligence and Current Sensing for Matrix Converter Current Commutation", *IEEE Transactions on Industrial Electronics,* Vol. 49, No. 2, pp. 382-389, April 2002

[46] Wheeler P., Rodriquez J., Clare J., Empringham L., Weinstein A., " Matrix Converters: A Technology Review", *IEEE Transactions on Industrial Electronics,* Vol. 49, No. 2, pp. 276-288, April 2002

[47] Empringham L., Kolar J., Rodriguez J., Wheeler P., Clare C., "Technological Issues and Industrial Application of Matrix Converters: A Review", *IEEE Transactions on Industrial Electronics,* Vol. 60, No. 10, pp. 4260-4271, October 2013

[48] Vargas R., Ammann U., Rodriguez J., Pontt J., "Predictive Strategy to Control Common-Mode Voltage in Loads Fed by Matrix Converters", *IEEE Transactions on Industrial Electronics,* Vol. 55, No. 12, pp. 4372-4380, December 2008

[49] Rivera M., Wilson A., Rojas C., Rodriguez J., Espinoza J., Wheeler P., Empringham L., "A Comparative Assessment of Model Predictive Current Control and Space Vector Modulation in a Direct Matrix Converter", *IEEE Transactions on Industrial Electronics,* Vol. 60, No. 2, pp. 578-588, February 2013

[50] Villarroel F., Espinoza J., Rojas C., Rodriguez J., Rivera M., Sbarbaro D., "Multiobjective Switching State Selector for Finite-States Model Predictive Control

Based on Fuzzy Decision Making in a Matrix Converter", *IEEE Transactions on Industrial Electronics,* Vol. 60, No. 2, pp.589-599, February 2013

[51] Rivera M., Rojas C., Rodriguez J., Wheeler P., Wu B., Espinoza J., " Predictive Current Control With Input Filter Resonance Mitigation for a Direct Matrix Converter", *IEEE Transactions on Power Electronics,* Vol. 26, No. 10, pp. 2794-2803, October 2011

[52] Rojas C., Rodriguez J., Villarroel F., Espinoza J., Silva C., Trincado M., "Predictive Torque and Flux Control Without Weighting Factors", *IEEE Transactions on Industrial Electronics,* Vol. 60, No. 2, pp. 681-690, February 2013

[53] Nguyen T., Lee H., "Space Vector Modulation for Single-input dual-output indirect matrix converter", 38th Annual Conference on IEEE Industrial Electronic Society, 2012

[54] Friedli T., Comparative Evaluation of Three-Phase Si and SiC AC-AC Converter Systems, Ph.D. Dissertation, ETH Zurich, Switzerland, 2010

[55] Cortes P., Rodriguez J., Silva C., Flores A., "Delay Compensation in Model Predictive Control of a Three-Phase Inverter", *IEEE Transactions on Industrial Electronics,* Vol. 59, No. 2, pp. 1323-1325, February 2012

[56] Uddin M., Mekhilef S., Nakaoka M., Rivera M., "Model Predictive Control of Induction Motor with Delay Time Compensation: An Experimental Assessment", IEEE Applied Power Electronics Conference (APEC) 2015, Charlotte, NC

[57] Rodriguez J., Cortes P., Predictive control of Power Converters and Electrical Drives, John Wiley & Sons, 2012

[58] Gulbudak O., Santi E., Marquart J., "Finite State Model Predictive Control for 3x3 Matrix Converter based on Switching State Elimination", IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburg, USA, 2014, pp. 5805-5812

[59] Gulbudak O., Marquart J., Santi E., "FPGA-based Model Predictive Current Controller", IEEE Energy Conversion Congress and Exposition (ECCE), Montreal, Canada, 2015, pp. 4307-43144

[60] Dehghan M., Mohamadian M., Yazdian A., "Hybrid Electric Vehicle Based on Bidirectional Z-Source Nine-Switch Inverter", *IEEE Transactions on Vehicular Technology,* Vol. 59, No. 6, pp. 2641-2653, July 2010

[61] Gulbudak O., Santi E., "Model Predictive Control of Dual-Output Nine-Switch Inverter with Output Filter", IEEE Energy Conversion and Exposition (ECCE), Montreal, Canada, 2015, pp. 1582-1589