Development, Optimization, and Integration of Inline Phase-Change Switches for Reconfigurable RF Systems

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Why not you?

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Abstract

The goal of any switch is to enable reconfiguration, flexibility, or adaptability for the network in which it is being implemented. Electrical switches that operate at radio frequencies (RF) are designed to increase system functionality and flexibility, such as routing signals to different locations or changing the frequency response of a circuit. Unfortunately, current state-of-the-art (SOA) RF switches do not have the performance, size, or cost in order to enable the large scale flexibility seen in modern digital system-on-chips (SoCs) and FPGAs. Non-volatile chalcogenides present a unique opportunity to create analog SoCs, as low loss, low power consumption, small size, and low cost integration are all simultaneously achievable in this material system.

This thesis details the first demonstration, performance, and integration of 4-terminal, indirectly heated phase-change switches for reconfigurable RF systems. The first demonstration of device functionality outperformed SOA FET-based RF switches in terms of frequency performance (1.1 THz F_{co}, or 145 fs R_{on}*C_{off}), and was improved by over an order of magnitude over the course of this research (12.5 THz F_{co}, or 12.7 fs R_{on}*C_{off}). The investigations into power handling have resulted in an extracted threshold field of 12.6 V/µm in 50:50 GeTe, an improvement in OFF-state power handling from 18 dBm to 29 dBm, and a switch with a simultaneous R_{on}, C_{off}, F_{co}, V_{th}, $P_{RFmax,off}$, and reliability of 1.2 Ω, 12.3 fF, 10.6 THz, 6 V, 28 dBm, and >500,000 cycles, respectively. A correlation between the DC V_{th} and the RF power handling was demonstrated, identifying the fundamental mechanism for power handling limitations.

Three different reconfigurable RF system prototypes were fabricated using heterogeneous integration of these phase-change switches with a multifunction SiGe BiCMOS MMIC.

Problems with the RF performance of the system highlighted the need for an improved integration of these phase-change switches. A back-end-of-line (BEOL), CMOS-compatible monolithic integration process was then experimentally demonstrated for the first time, detailing the benefits of future monolithically integrated phase-change switches on a variety of semiconductor technologies.

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1 Introduction

1.1 Motivations

The goal of any switch is to enable reconfiguration, flexibility, or adaptability for the network in which it is being implemented. Simple examples include such common things as light switches and stoplights, where the flow of electricity (or traffic) on a particular wire (or road) is governed by the state of the switch module. The switches allow the network to have access to different states, such as the lights being on or off or cars going in a different direction, which would not be available on a direct, uninterrupted connection. Perhaps the most ubiquitous switch on the planet is the complementary metal-oxide-semiconductor (CMOS) field-effect transistor (FET), which is the basis of all modern digital electronics. Here, the FET acts as a switch and reconfigures the output of a circuit based on the inputs to the switch module (Boolean logic gate in this case). The performance of the CMOS transistor has driven the digital revolution, with better and smaller switches delivering more flexibility and functionality to the overall system, allowing digital system-on-chips (SoCs) to be implemented in almost all modern electronics used today.

The fundamentals of this digital SoC development can also be applied to analog electronics, which are the basis of wireless communication and interfaces to the real world. The switches that operate at these radio frequencies (RF) provide the same benefits as their digital counterparts, namely to increase functionality and flexibility of the overall system. While the ultimate performance of both a digital and analog system is governed by the RC delays of the switch, digital switches have an advantage in the "gain" provided by the next stage in the logic gate. Because the output of a single stage is fed into the input of the next stage in a digital circuit, signal losses associated with the actual switch are reset at the next stage. Therefore, the

main requirements for the digital switch are suitable OFF/ON ratios, drive currents (speed), and leakage currents (power consumption).

In analog and RF systems, switches also contribute parasitic signal losses, and there can be many circuit stages before the signal can be amplified back again to optimal levels (where the number of stages also increases with the number of switches used). There are also many disadvantages to adding amplifier stages to compensate for switching losses, such as increased circuit area (cost), increased power consumption, and decreased linearity. Therefore, the parasitic losses associated with a signal passing through a switch (insertion loss for the ON-state and isolation for the OFF-state) are the main requirements that govern the performance of the switching network and govern the amount of the switches that can be implemented at a given frequency and loss budget. In order to increase the functionality and flexibility of RF systems similar to digital SoC development through Moore's law, RF switches need to have progressively lower loss to allow larger system flexibility in a smaller area. This would allow reconfiguration by switching in different components to change the frequency response of the system (like in a tunable filter), or to route signals to different components for further processing (larger multi-throw switch circuits), or through a variety of other methods (redundancy, component swapping, etc.). The lower the loss of the switch, the more flexibility a designer can add to the system for the same loss penalty, or alternatively reduce the loss of the system for the same level of flexibility. The increased overall system efficiency could even allow certain components to be removed from the system, lowering power consumption and system cost.

In order to increase RF system functionality and flexibility, better and smaller RF switches need to be integrated into the system. While this primarily translates into an RF switch that has very low transmission losses (as mentioned previously), other specifications also

determine its usefulness. Size, power consumption, power handling (breakdown limitations), switching speed, and linearity are other specifications that also significantly determine the application space of an RF switch. Finally, the switch also needs to be easily integrated and actuated with the other RF components in the system, in order to maximize the overall RF system functionality.

1.2 Analog/RF Switch Background

1.2.1 Frequency Performance of RF Switches

The primary characteristic of any RF switch is the frequency dependent transmission loss associated with each state. Assuming an ideal resistor in the ON-state and an ideal capacitor in the OFF-state, the insertion loss (ON-state transmission loss) and isolation (OFF-state transmission loss) of a series switch in a 2-port network can be shown to have the following dependencies on the ON-resistance (R_{on}) and the OFF-capacitance (C_{off}) [1]:

$$\text{insertion loss} = 20 \cdot \log_{10}\left(1 + \frac{R_{on}}{2 \cdot Z_o}\right) \tag{1.1}$$

$$\text{isolation} = 10 \cdot \log_{10}\left(1 + \frac{1}{(2 \cdot \omega \cdot C_{off} \cdot Z_o)^2}\right) \tag{1.2}$$

The typical figure of merit (FoM) used for RF switches is the cut-off frequency (F_{co}) [2], which is defined as the frequency at which the OFF-impedance equals the ON-impedance, assuming the switch is an ideal series resistor in the ON-state, and an ideal capacitor in the OFF-state (discussed more in 2.4.2.3):

$$F_{co} = \frac{1}{2 \cdot \pi \cdot R_{on} \cdot C_{off}} \tag{1.3}$$

Comparable to the FoM for transistors in amplifiers (F_t), the F_{co} is used as a guide to evaluate the value of one RF switch versus another. The two main components, R_{on} and C_{off}, vary for different technologies, and a table of the F_{co} of state-of-the-art (SoA) switches is given in Figure 1.1.

Technology	F_{co} (THz)	Ref.
45nm CMOS	0.53	[3]
130nm SOI CMOS	1.5	[4]
GaAs pHEMT	1.1	[5]
GaN HEMT	2.1	[2]
AlGaAs Diode	2	[6]
RF MEMS	3.8	[7]
VO_2	40	[8]

Figure 1.1 Table showing the different F_{co} values for different RF switch technologies

Typically, the R_{on} is dominated by the semiconductor physics which govern the underlying material's electronic structure, whereas the C_{off} is typically dominated by the architecture and layout of the device, and how it is able to address parasitic capacitances [2].

To date, there is not an RF (>1 GHz) switch which exists in current manufactured technology that has low enough loss to enable the analog system flexibility typically seen in digital systems. The CMOS FET (45nm node) has significant advantages in terms of integration and manufacturing capability, but the R_{on} is typically high due to the limitations of the Si material resistivity, and the C_{off} is also high due to the non RF-optimized overlapping gate structure that it is forced to use due to being an inversion-based FET fabricated in dedicated digital Si processes [3]. Improvements to the RF performance in CMOS have been demonstrated with processes more optimized for RF performance, such as the 180nm SOI process [9], [10]. In this process, the normally low resistivity substrate is exchanged for a high resistivity substrate with a buried oxide layer, which significantly improves the isolation and insertion loss of the switch. The SOI process also shows promise to improve the F_{co} as they are scaled to more advanced manufacturing nodes [4]. While this makes the SOI CMOS the RF switch technology of choice for most wireless and handset products, the still-inadequate insertion loss and isolation limit the number of switches that can be placed in a system. Moreover these switches show little

promise to be able to provide adequate performance at the frequencies that will be used in future 5G communication systems.

Fundamental improvements to RF switches are possible by using materials with lower channel electrical resistivities (ρ), such as GaAs or GaN switches, which can have an F_{co} as high as 2.1 THz [2], [5]. These pseudomorphic high electron mobility transistors (pHEMTs) use heterostructures to decrease the $R_{on,}$ and high resistivity substrates with optimized gate configurations to decrease the C_{off}. GaAs and GaN switches also have faster switching speeds and higher breakdown voltages when compared to CMOS and SOI CMOS due to the heterostructures and higher semiconductor bandgap. The major drawback comes from the fact that they are manufactured in their own dedicated process, which requires heterogeneous integration with CMOS in order to complete the RF system (discussed more in Section 1.2.3). This integration is expensive and lossy, and negates the benefit from using the lower loss switches.

AlGaAs diodes [6], RF MEMS [7] and VO_2 switches [11] offer an improved FoM , but have less desirable secondary qualities (poor integration, high rail voltage, poor reliability, large size, poor hot switching, poor power handling) that make them unsuitable for massive system reconfiguration (discussed more in section 1.2.2). Figure 1.2 shows the ON-state transmission and OFF-state transmission of different switch technologies in a single-pole, double-throw

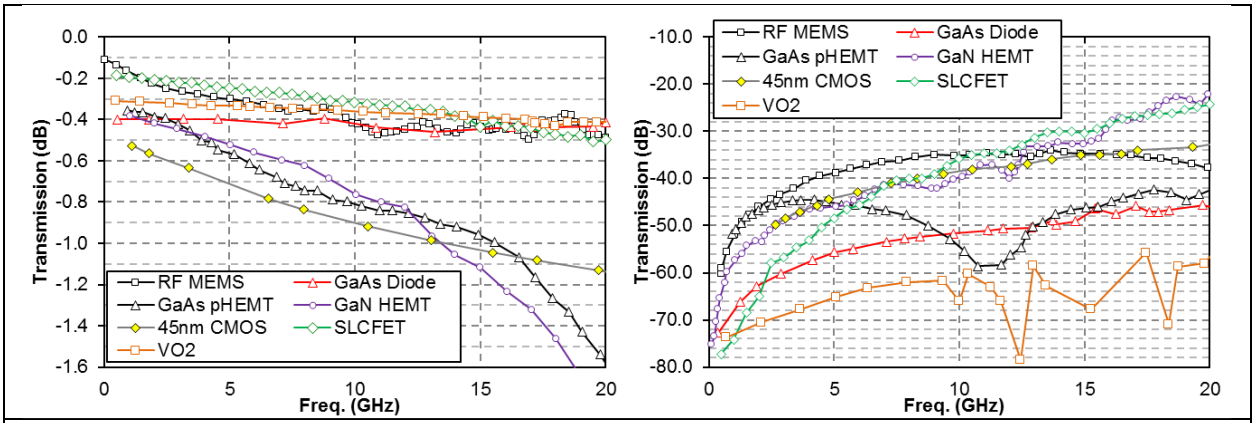


Figure 1.2 ON-state transmission (left) and OFF-state transmission (right) vs. frequency of different RF switch technologies in series-shunt, single-pole, double throw configuration

circuit with a series-shunt configuration [12], [13]. The insertion loss and isolation tracks well with the F_{co}, with the highest F_{co} switch technologies having the lowest insertion loss and best isolation as a function of frequency. Further analysis on the different SPDTs is given in Section 3.4.

1.2.2 Power Handling and Other Specifications of RF Switches

In addition to the frequency performance of the switch, there are secondary switch properties that important in determining the usefulness of an RF switch [14], [15]. These secondary switch properties, such as power handling, switching speed, power consumption, linearity, actuation voltage, size, and reliability often dictate the technology choice for certain topologies and applications. For example, military systems such as radar and electronic warfare systems typically need RF switches that can withstand very high power levels, which leads to a greater number of GaAs and GaN switches being used in those systems when compared to lower power analog systems such as cell phones. One of the most important secondary properties in this category is power handling, followed closely by switching speed, power consumption, actuation voltage, and linearity.

For any switch, the power handling must be evaluated independently for both states, as the failure mechanism can be quite different depending on the technology and the state of the

switch. In FET technologies, the ON-state power handling ($P_{RF,max,ON}$) is determined by the current carrying capacity of the semiconductor channel material, whereas OFF-state power handling ($P_{RF,max,OFF}$) is determined by the electric-field induced voltage breakdown of the device [14], [16]. This can lead to different circuit implementations in order to meet the required system breakdown requirements. For example, systems that implement a FET technology with a lower OFF-state breakdown than the system specifications, system performance is achieved by "stacking" the FETs in series (adding multiple FETs in series to increase the OFF-state breakdown across the sum) [15]. This comes at the expense of the ON-resistance (and insertion loss) as there is now more resistance in the signal path. If a designer decided to make each FET wider in order to lower the resistance of each FET, it would correspondingly increase the OFF-capacitance associated with each FET. The same scenario for the ON-state results in a similar conclusion, where the use of a wider FET in order to decrease the current density will increase the OFF-capacitance. This exposes a fundamental trade-off between power handling and F_{co}, which is a common trade-off for RF switches.

Figure 1.3 shows a comparison of different RF switch technologies power handling capabilities for a given size of switch. For FET technologies, the breakdown voltage is a function of the device layout and the semiconductor breakdown field, which is a function of the band gap [17]. A larger electric field is needed to create carriers from impact ionization in semiconductors with a large band gap, which is why GaN FETs have a larger breakdown voltage than GaAs FETs, and GaAs FETs have a larger breakdown than CMOS FETs (for the same device layout). Looking strictly within CMOS FETs, the power handling (and breakdown voltage) typically decreases with the node, as the source and drain connections are now closer

together, requiring smaller voltages to reach the same critical breakdown field [15]. Increasing source/drain spacing results in an increased ON-resistance, which why the Baliga FOM (which uses the ON-state conductivity and electric breakdown field product) is commonly used to evaluate semiconductors for RF applications [17].

Technology	Single Finger/Device FET V_{br}	Reference
45nm CMOS	1.15 V	[18]
130nm SOI CMOS	4.7 V	[4]
GaAs pHEMT	12 V	[5]
GaN SLCFET	40 V	[19]
AlGaAs Diode	25 V	[20]
RF MEMS	1-30 V	[21]
VO_2	< 2 V	[11]

Figure 1.3 Table showing the different power handling capabilities for different RF switch technologies

The non-FET based RF switches (diodes, RF MEMS, VO_2) also have voltage and power handling requirements with different trade-offs. For example, the stand-off voltage/power handling in RF MEMS is a trade-off with the actuation voltage [21]. Larger power handling capabilities require larger pull-down voltages, which are less desirable to produce and handle in the circuit. VO_2 based switches have similar breakdown mechanisms to a FET, where a large enough voltage will cause the channel to become conductive. The mechanism for this is quite different from FETs though, where the large voltage causes a leakage current which produces the heat required for phase transformation [22].

In order to have a high-performance RF switch, a low ON-state resistivity is needed for both low insertion loss and high ON-state power handling (lower current density), with a simultaneous high breakdown field for the OFF-state power handling, regardless of the switch technology used. Other device performance characteristics such as linearity and switching speed (not discussed in this thesis) can play a role in determining the usefulness of a new switch technology. But system-level characteristics such as integration, actuation, and packaging are

often the deciding factor when determining the usefulness and application space of a new switch technology and are discussed in the next section.

1.2.3 Integration, Actuation, and Packaging

Based on Figure 1.1 and Figure 1.3, GaN HEMTs look quite superior to all other FET technologies for RF switches in terms of their F_{co} vs. $P_{RF,max}$ trade-off. But SOI CMOS FETs are by far the most common type of RF switch in RF systems. The discrepancy between ultimate performance and use can be explained by the integration and packaging of the different RF switch technologies. GaN HEMT switches must be fabricated in their own dedicated process, which then requires heterogeneous integration through either wire-bonding, flip chipping, or micro-bumping in order to be integrated into the RF system [23]. All 3 methods come at cost of performance and increased cost, due to the labor and additional processing required.

In addition, GaN HEMTs require larger, non-standard actuation voltages and are expensive to fabricate [2], [24], meaning the cost per switch and cost for integration is significantly higher than CMOS technologies. SOI CMOS switches, on the other hand, are fabricated using cheaper/fabrication-friendly materials, higher metallization complexity, and digital control logic which greatly reduces the cost per switch and integration [9]. While no standard or published FOM exists for evaluating the F_{co} per unit cost of fabrication and integration, an easily understood guideline is that RF switches utilizing a CMOS-like process and integration are cheaper than RF switches that must be fabricated in their own dedicated processes and heterogeneously integrated into an RF system.

A final and often overlooked consideration of RF switches is the method of actuation. One of the main advantages of FET-based RF switches is that they are voltage-controlled, meaning only a change in gate voltage is required to change the state of the switch. This is

advantageous when compared to PIN diodes, which require significant current during operation and are viewed as a current-controlled device. The current-actuation requires special control circuitry and results in significant power consumption per switch, limiting the total number of switches that could be used for a given power budget. In addition, because the diode is a two-terminal device, the current used to control the diode must travel on the same path as the RF signal. This further complicates implementation when compared to a FET, where the gate is located on a separate terminal and significantly reduces the implementation complexity from a design standpoint.

FETs also have an advantage over MEMS devices, which are also voltage-controlled switches, due to the significantly lower actuation voltage. Depletion-mode GaAs pHEMTs and GaN HFETs typically have pinch off voltages between -0.5 V and -2.5 V [5], enhancement-mode CMOS SOI switches are typically gate biased between 2-3 V to turn on [9], but MEMS devices require large rail voltages (between 35 V [25] and 60 V [7] for high-performance devices) in order to switch or hold the state of the switch. These large voltages are difficult to supply for certain systems that are highly digital or power constrained (such as cell phones), and increase power and design overhead by requiring charge pumps to create the voltages from 1.8 or 3.3 V rails [25]. These type of voltage supply constraints are also disadvantageous to certain FETs such as GaN SLCFETs (which require a larger negative voltage to turn off, typically between -8 V to -14 V [2]) because they require special (meaning non-CMOS) supply voltages that increase the complexity of system integration.

In order to be viewed as a viable RF switch technology when compared to these incumbent technologies, there are 3 requirements that need to be satisfied: (1) the frequency performance, (2) the secondary device characteristics such as power handling, power

consumption, and linearity, and (3) integration, actuation, and packaging considerations. The ability of a new switch technology to succeed in these three areas will determine how large of an impact it can have for new RF systems with demanding requirements on flexibility and tunability. In this context, an ideal RF switch has the following properties: zero R_{on}, zero C_{off}, infinite current and voltage handling capabilities, zero power consumption in any state or to switch states, instantaneous switching speed, easily integrated with any technology, and actuated using standard protocols. This framework is useful in discussing new switch technologies and how they relate back to the goals of the system.

1.3 Chalcogenide Devices

1.3.1 Chalcogenide Basics

Chalcogenide phase-change materials (PCMs) have been researched for use as novel switches since their discovery in the 1960's [26]. Chalcogenides have drastically different optical and electrical properties depending on the state of the crystalline phase, which allows them to be used as both an optical and electrical switch [27]. The amorphous state behaves very similar to a semiconductor or dielectric, with a very low optical reflectivity and a very high electrical resistivity. Amorphous GeTe in particular is a *p*-type semiconductor, with a band gap (E_g) of 0.8 eV [28]. The crystalline state, on the other hand, is a degenerate p-type semiconductor, behaving very similar to a metal with high optical reflectivity and low electrical resistivity [27], [29]. The low electrical resistivity of crystalline GeTe is due to the narrow band gap (~0.1–0.2 eV) with Fermi level ~0.3–0.5 eV inside the valence band [28]. One of the most important chalcogenides properties is the inherent non-volatility of the material, meaning chalcogenides retain their crystalline state until perturbed by an external energy source. This

means that unlike a semiconductor switch, no power is consumed to hold the chalcogenide switch in a certain state. Energy is only required to switch between states.

When starting in the crystalline or ON-state, thermal energy is required in order to heat the material past its melting point, which then needs to be dissipated rapidly (going from ~700°C to ~150°C in less than 1 µs [30]) in order to quench the material in the highly resistive amorphous state (OFF-state) [31]. In order to return to the low resistivity ON-state, another (lower energy) thermal energy pulse is required to give the atoms enough energy to realign into the crystalline state [31]. Transitioning between the two states is then accomplished by applying the correct pulse, either the crystallizing (or SET) pulse to turn the device ON, or the amorphizing (or RESET) pulse to turn the device OFF, as depicted in Figure 1.4 .

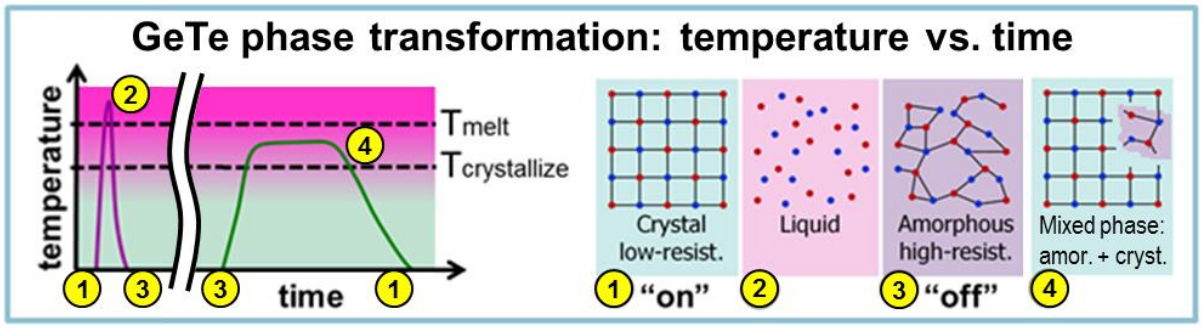


Figure 1.4 Diagram showing temperature profiles of thermal pulses used to transition between phases in chalcogenides.

1.3.2 Chalcogenide Devices

There are several types of devices that exploit the phase-dependent properties of chalcogenides, and can be grouped into two categories: volatile and non-volatile. An example of a volatile chalcogenide device is their application as a memory selector for cross-point memory architectures [32]. In these ovonic threshold switches (OTS), the chalcogenide remains in the high-resistivity state until a large enough voltage is applied, exceeding the threshold voltage of the material, at which point the chalcogenide converts to the low-resistivity state. It will remain

in the low-resistivity state as long as minimum holding voltage (or current) is present, below which the material will return to the high-resistivity state. The required minimum holding voltage makes this device volatile, acting similar to a diode. While not particularly useful as an RF switch, this type of device is *critical* to advanced memory architectures for future digital systems.

Historically, the non-volatile devices have dominated chalcogenide uses and applications. The first widespread use was in optical memory systems, where chalcogenides were used as the material on CD-RWs and DVD-RWs. Here, laser pulses were used to provide the thermal energy for melt/quenching and recrystallization, and the reflectivity difference between the amorphous and crystalline states was used to store bits of data as 1's or 0's. Newer digital memory applications also use chalcogenides as non-volatile memory, but use the phase-dependent electrical resistivity to store data bits [31]. In these applications, electrical contacts are formed on each side of the chalcogenide material, and an electrical current pulse is sent through the device to provide the heat necessary to switch between states. While similar to optical memory and basic chalcogenide phase transformations, there is a subtle (but important) distinction in their operation. In order to amorphize the material and obtain the OFF-state (RESET), enough heat needs to be created from the electrical current to melt the material and dissipated quickly enough to quench in the amorphous state, as in regular chalcogenide physics. But the process of recrystallizing the material into the ON-state (SET) is two-step process that is different from the optical memory operation. An appropriately large voltage pulse is applied across the device, and when the threshold voltage of the device is exceeded, the chalcogenide quickly reorients into the low-resistivity state. This low-resistivity state is not permanent, and the threshold voltage is determined by the compositionally-dependent threshold field and

fabricated thickness of chalcogenide, similar to the conduction and operation of OTS devices. If the voltage remains applied across the device once the chalcogenide is in the low-resistivity state, a significant increase in current flows through the device due to the lower material resistivity. The heat generated from this current raises the temperature of the material above the recrystallization temperature, which (unlike OTS devices) then thermally recrystallizes the material and locks in the ON-state. At the conclusion/termination of the pulse, the material remains in the low-resistivity crystalline state, without additional energy being applied.

The underlying physics of conduction between the two different low-resistivity states has been the focus of intense research due to their interest for digital memory applications. The classic non-volatile crystalline conduction is the most understood, and is attributed to the electronic band structure giving rise to high concentration of p-type carriers. The threshold-field induced volatile conduction is less understood, with two main theories currently being researched as the fundamental mechanism. The first is a theory proposed by D. Ielmini, which accounts for the threshold switching as thermally-assisted tunneling phenomena between localized states in the amorphous material [33], [34]. The threshold switching is explained as a "field-induced energy increase in electrons in their hopping transport, moderated by the energy relaxation due to phonon-electron interaction. The energy increase leads to an enhancement of conductivity and a collapse of the electric field within the amorphous chalcogenide layer, accounting for the observed negative differential resistance at switching [34]." The second theory is proposed by V.G. Karpov *et al.*, where the threshold switching is based on a field-induced crystal nucleation model [35]. The threshold switching is explained by "the nucleation of a needle-shaped crystal embryo. Similar to a lightning rod, it concentrates the electric field, which facilitates nucleation of additional particles at its end, etc. This instability leads to a low-

resistive crystalline filament across the structure [35]." While it is not clear which theory is correct, and both theories have strong experimental data to support their claims, understanding the underlying physics of this soft electronic breakdown are critically important to understanding and engineering the OFF-state breakdown in RF chalcogenide devices, discussed more in the next section and in Chapter 4.

1.3.3 Chalcogenide Devices in RF Implementations

There are three main implementations of chalcogenide switches used in RF applications. The first is a via-style phase-change RF switch (2T-DH in Figure 1.5), which has an identical device design to the digital memory phase-change switch [36]. In this design, the chalcogenide is sandwiched between two electrodes in a CMOS-like process, and is actuated by joule heating from current flowing directly through the chalcogenide [37]. These types of switches have been used to create on-chip reconfigurable inductors [37], and reconfigurable voltage-controlled oscillators (VCO) [38], where the chalcogenide switch is used to connect different capacitors and inductors in a circuit. The advantages of this design are the low voltage actuation (~5V [36]) and CMOS-integration simplicity. The major disadvantages are the limited RF performance due to incomplete recrystallization resulting in higher ON-resistances [36], the inability to parallelize switches to lower the resistance [39],[40], and the co-location of the actuation control signal and the RF signal (similar to the disadvantage of the diodes in RF switch implementations).

The second type of chalcogenide switch is a 4-terminal, directly-heated phase-change switch (4T-DH in Figure 1.5). This design is similar to a via-style phase-change switch in that a piece of chalcogenide material is sandwiched between two electrodes and joule heating with current flowing directly through the PCM is used to initiate the phase transformations, but additional electrical contacts are now placed on the side of the PCM. These additional contacts

are used as the RF signal contacts [41]. The advantages of this design over the via-style phase-change switch are the segregation of actuation and RF signal paths, and the simplicity of creating lower ON-resistance (i.e. insertion loss) devices through simple layout modifications (device width increase). The disadvantages of this design are the increase in switching power (due to more material being melt/quenched), increased fabrication complexity compared to via-style PCM switches, and significant parasitic RF signal losses due to the directly connected actuation terminals between the RF electrodes. The design fixes implemented to limit these losses (higher resistance microheaters and RF chokes at the microheater terminals) significantly increase the actuation voltage and design complexity. This device design has been used to create RF switches and tunable filters [42].

The third type of device is a 4-terminal, indirectly heated phase-change switch, also called an inline phase-change switch (IPCS) (4T-IH in Figure 1.5). This design is very similar to a bottom-gated FET, where ohmic contacts are made to a channel material (the PCM), with a dielectrically-isolated but thermally-coupled microheater sitting below the chalcogenide channel (Figure 1.6). In this design, the PCM material is heated indirectly, meaning no electrical current flows through the PCM in order to change the material phase. Rather, electrical current flows through the proximal microheater, and the heat from the microheater is thermally conducted up to the PCM and used for the amorphization and recrystallization process. The advantages of this design are the decoupled actuation and RF signal paths, the simplicity of creating low R_{on} devices, and the significantly reduced C_{off} due to the dielectrically-isolated microheater. The disadvantages of this design are the restrictions placed on the materials and thicknesses to ensure proper quenching/actuation, the increased energy required to melt the PCM, and the increased stress (both thermal and electrical) placed on the microheater. While being the most difficult to

design, fabricate, and operate correctly due to the thermal quench requirements and demand placed on the microheater, this design offers the largest advantage in terms of RF performance and integration (Figure 1.5). This device design has been used to create multiple types of circuits (SPDT [13], SP4T, SP8T [43], tunable filters, phase shifters, millikelvin temperature circuits, reconfigurable low-noise amplifiers (LNAs) [44], [45]) and reconfigurable transceivers [43].

Device Type	R_{on} Scaling	RF performance	Actuation	Power to Actuate	Fab Complexity	BE Integration
2T, DH	Difficult	Poor	Difficult	Low	Simple	Simple
4T, DH	Simple	Medium	Simple	Medium	Medium	Medium
4T, IH	Simple	Good	Simple	High	Medium	Medium

Figure 1.5 Table comparing the different properties of the three different RF implementations of phase-change switches

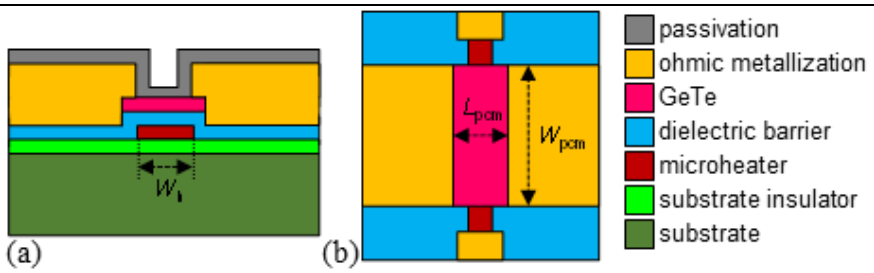


Figure 1.6 Schematic (a) cross section and (b) plan-view cartoon of the 4-terminal, indirectly heated, phase-change switch (or inline phase-change switch)

1.3.4 Thesis Outline

This thesis is focused on the development, improvement, and optimization of 4-terminal, indirectly heated phase-change switches towards becoming a viable switch technology (compared to all types of RF switches) for analog SoC and reconfigurable RF applications. Chapter 2 gives an overview of the fabrication process flow for the devices reported on in this thesis, as well as a summary of the DC and RF tests and how they are performed. Chapter 3

discusses the development, demonstration, and optimization of IPCS devices for improved frequency performance (R_{on}, C_{off}, F_{co}). It will focus on the fabrication and initial demonstration of the first-generation devices, as well as the performance optimizations and improvements, and concluding with RF SPDT circuit demonstrations. Chapter 4 discusses the power handing limitations of the first generation process, detail significant improvements made in the second and third-generation processes, and correlate these improvements to improved power handling capabilities. It will focus on the fundamental mechanisms that determine device V_{th}, extraction of threshold field for 50:50 GeTe along with direct observation of the amorphous region in devices, device improvements in the second and third-generation processes, and a correlation between OFF-state power handling and threshold voltage for all 3 process generations. Chapter 5 discusses the heterogeneous integration required to create reconfigurable systems, and the benefits of using a monolithic integration scheme for IPCS devices. It will focus on the limitations of heterogeneous integration, and the demonstration of functional IPCS devices using a CMOS compatible monolithic integration fabrication process. Chapter 6 will summarize the work of this thesis and describe future directions of development and research in order to create unique and reconfigurable RF systems.

2 Methods of Fabrication and Testing

2.1 Abstract

In this chapter, the methods of fabrication and testing are discussed to provide context for the results in Chapters 3-5. First, the fabrication of the three different process generations is discussed, with specific detail given to the different microheater formations. Next, the DC testing is reviewed, with circuit diagrams to provide an understanding of the placement of the device under test (DUT) where appropriate. The importance of each test is discussed and example data taken from real devices is given. Finally, the RF test is reviewed with test schematics, circuit diagrams, and small signal models to provide to details on the RF extraction of device parameters and the methods for evaluating RF performance. The test equipment used and calibration is listed for the tests as well.

2.2 Introduction

The most important aspect in developing any new technology is building a device that can be measured. Proper design, fabrication, and testing of process control monitors is needed in order to ensure that each layer or level in the device is being accurately fabricated according to the integration design. Different process flows (or integrations) can have distinctly different performance advantages and disadvantages, and need to be evaluated electrically. The fabrication section of this chapter will discuss the fabrication process flow, with details on the individual layers and how they were formed for each unique process flow. The advantages and disadvantages of each process are discussed more thoroughly in Chapters 3 and 4.

Having clearly defined DC and RF metrics are then essential to evaluating the different integrations and device performance. Ultimately, the performance needs to be measured and demonstrated at RF frequencies (as this is the application of this type of switch), and so the RF

metrics used are much more standard among different switch technologies. But the measured DC results can give insights into the RF performance as well as the secondary qualities discussed in Section 1.2.2 and 1.2.3, and are often quite different and specific to the technology being used. The DC test section of this chapter will discuss the different unique tests used to characterize the phase-change switches reported in this thesis, as well as how they can be related to RF metrics. The RF test section of this chapter will discuss the small signal and power handling tests, how they are performed, and the unique aspects of testing and extracting data of the phase-change switches at RF frequencies.

2.3 Fabrication

Three different process generations are reported on in this thesis. The characteristics and results of each process generation are discussed in Chapters 3 and 4, as well as the motivations for developing each process generation.

2.3.1 First-Generation Process (Gen1)

A schematic cross-section of the Gen1 fabrication process flow is depicted in Figure 2.1. Fabrication begins with a dielectric material (substrate insulator) being CVD or thermally grown on the surface of the substrate. Both Si and SiC substrates are used, with 30-nm SiO_2 as the substrate insulator. Next, a 120 nm NiCrSi thin-film resistor (TFR) is patterned through lift-off techniques. A 30-60 nm plasma-enhanced CVD (PECVD) Si_3N_4 dielectric barrier material is then deposited, depending on the integration specification. Contact openings in the dielectric barrier are then dry etched in a CHF_3/O_2 plasma RIE, followed by a liftoff of a sputtered amorphous GeTe (75-120 nm in thickness, again depending on the integration specification), which was then crystallized. The GeTe deposition was optimized using the process detailed in [46] in a Kurt J. Lesker sputter deposition system. 1 µm Ti/Au contact and interconnect

metallization is then patterned via liftoff, followed by an additional 160 nm PECVD Si_3N_4 dielectric passivation with dry etched openings for electrical probing of the device.

An extension of the Gen1 process is the addition of a 2nd interconnect metal, thru-substrate vias (TSVs), and backside metallization, depicted in Figure 2.2 (e-Gen1). The 4 µm thick 2nd interconnect metallization is formed with plated Au to decrease line resistance and allow the formation of air bridges. The wafer is then thinned to 100 µm, and TSVs are dry-etched using an SF_6 inductively-coupled plasma process, before a 3 µm backside ground plane is Au-plated, establishing ground vias to the front side of the wafer. The plated interconnect metallization and backside processing represent a traditional III-V process flow, and demonstrate the ability of the IPCS devices to be integrated with either a CMOS or III-V process flow. The benefits of using the extended Gen1 process are detailed in Section 3.3.3. The RF performance of both processes are given in Sections 3.2.3, 3.3.2 and 3.3.3.

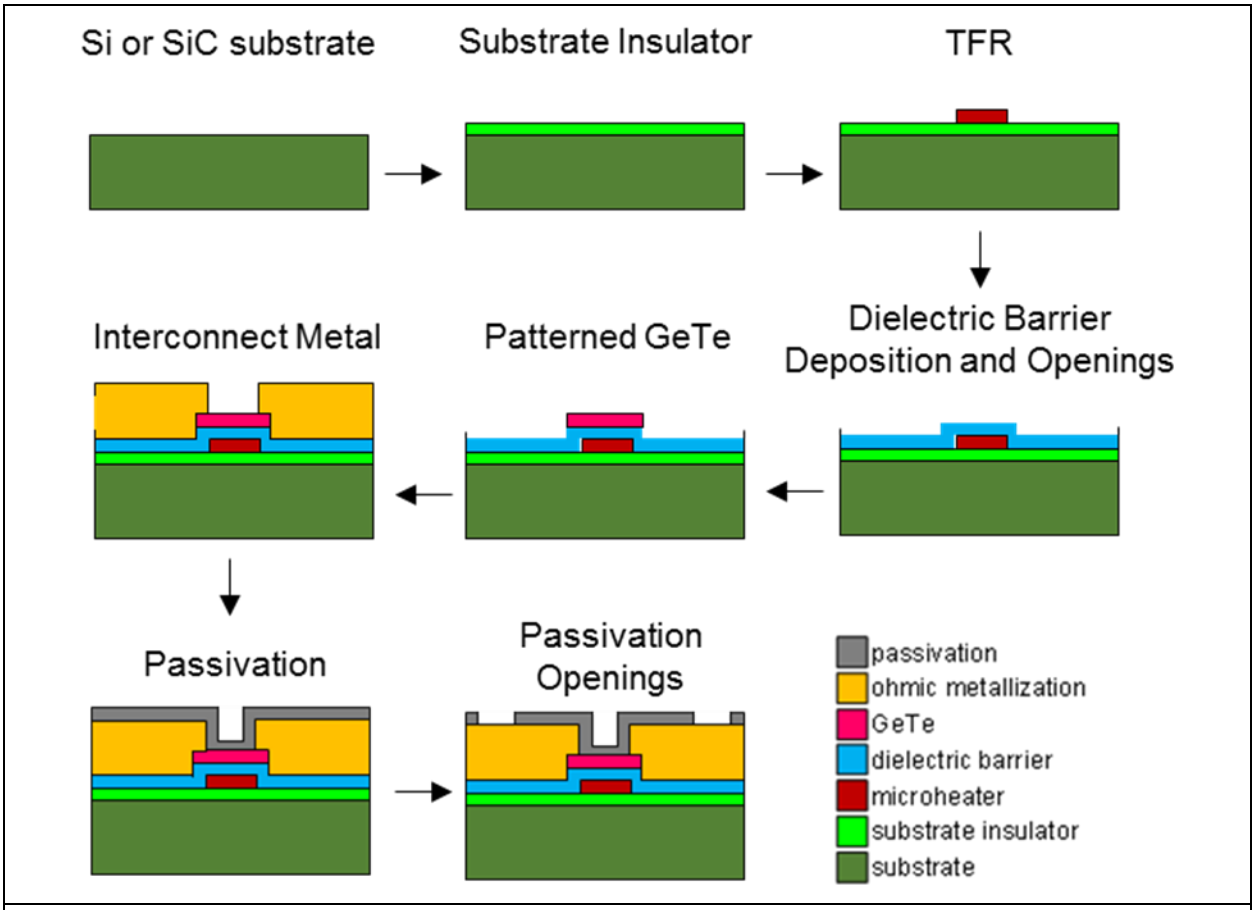


Figure 2.1 Schematic cross section of the Gen1 fabrication process flow for the 4-terminal, indirectly heated, phase-change switch (or inline phase-change switch)

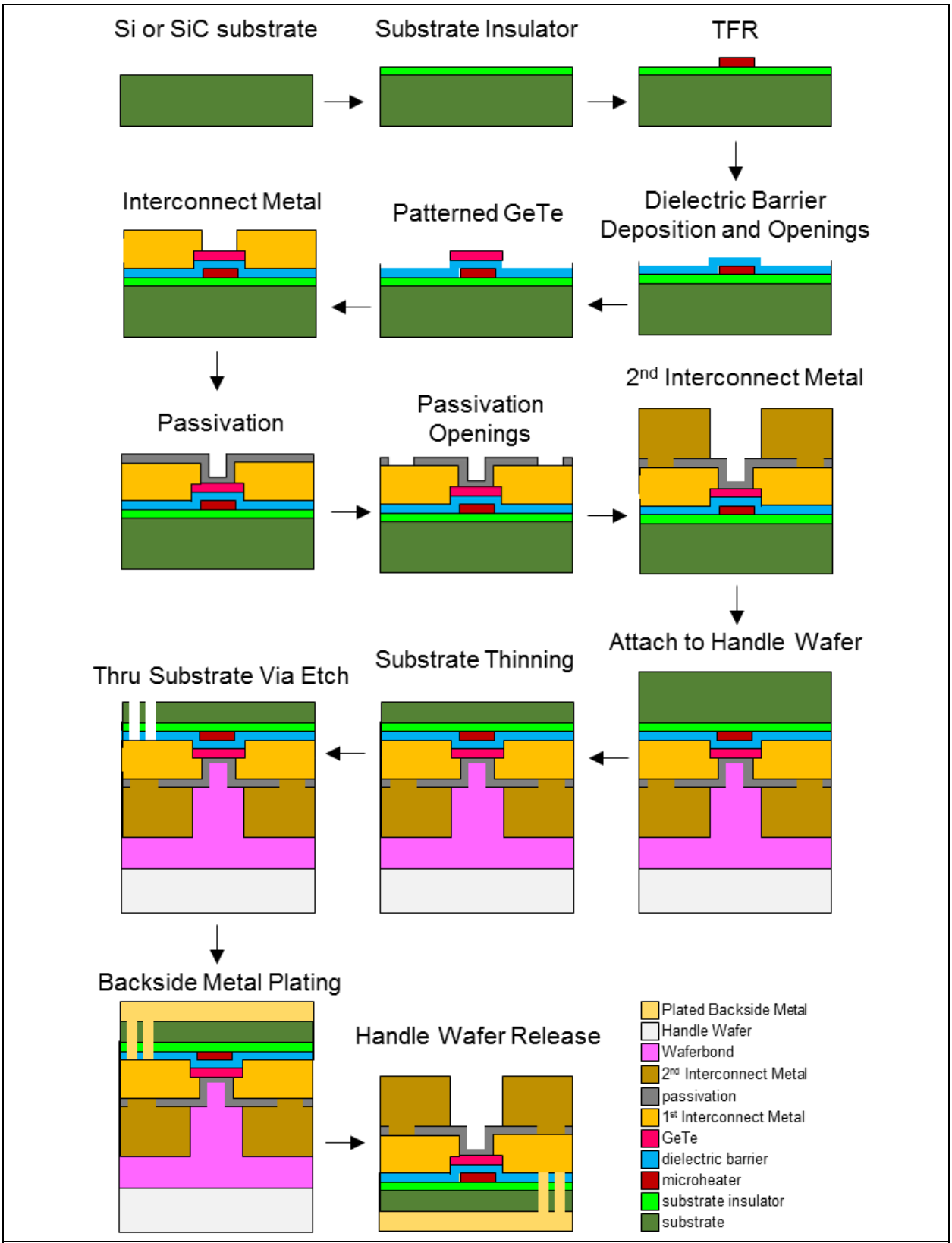


Figure 2.2 Schematic cross section of the extended Gen1 (e-Gen1) fabrication process flow for the 4-terminal, indirectly heated, phase-change switch

2.3.2 Second-Generation Devices (Gen2)

A schematic cross-section of the Gen2 fabrication process flow is depicted in Figure 2.3. Fabrication begins with a substrate insulator being CVD or thermally grown on the surface of the substrate. Both Si and SiC substrates are used, with a 60 nm SiO_2 as the substrate insulator. Next, a 50 nm W thin-film microheater is patterned through a blanket deposition followed by a CHF_3/O_2 RIE plasma etch. A 60 nm PECVD Si_3N_4 (or SiN) dielectric barrier material is then deposited. Contact openings in the dielectric barrier are then dry etched in a CHF_3/O_2 plasma RIE, followed by a liftoff of a 110 nm sputtered amorphous GeTe, which was then crystallized. The GeTe deposition was done in a Perkin-Elmer sputter deposition system and optimized using the process detailed in [46]. 0.25 µm Ti/Au contact and interconnect metallization is then patterned via liftoff, followed by an additional 160 nm PECVD SiN dielectric passivation with dry-etched openings. A 2 µm thick evaporated Ti/Au 2nd interconnect metallization is then patterned via liftoff before a 4 µm thick 3rd interconnect metallization is formed with plated Au to decrease line resistance and allow the formation of air bridges.

The process is similar to the Gen1 process with the exception of a W microheater, and the addition of the 2nd metal interconnect without any backside thinning or processing. A comparison table between all process generations is given at the end of Section 2.3.3. The reasoning behind developing the Gen2 process as well as the RF performance of the process is given in Sections 4.5 and 4.6.

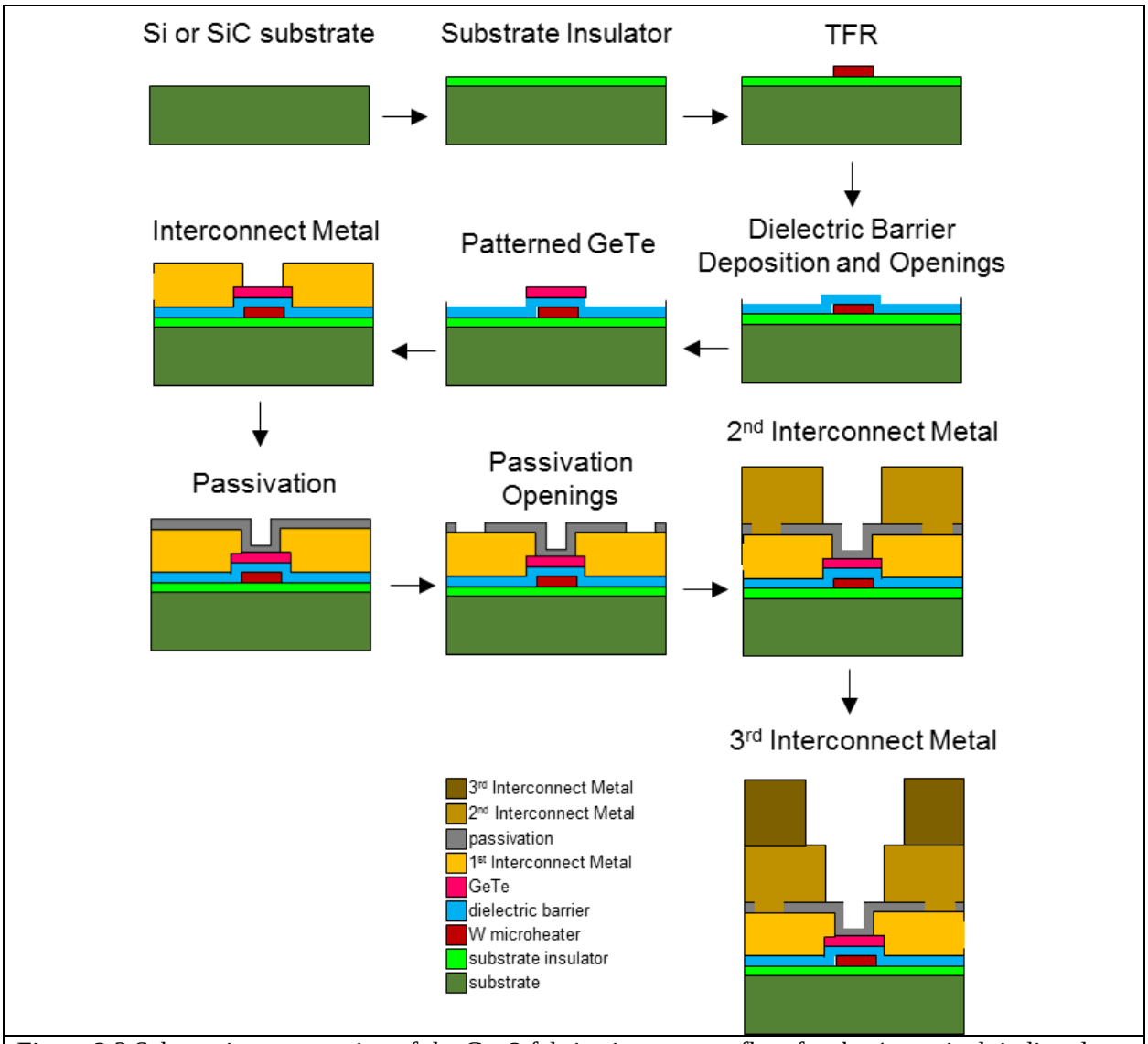


Figure 2.3 Schematic cross section of the Gen2 fabrication process flow for the 4-terminal, indirectly heated, phase-change switch, which uses etched-W microheaters and a 2nd level metal interconnect

2.3.3 Third-Generation Devices (Gen3)

A schematic cross-section of the Gen3 fabrication process flow is depicted in Figure 2.4. Fabrication begins by thermally oxidizing a 6" high-resistivity Si wafer (>10 kΩ·cm) with 250 nm of SiO_2. An opening is then RIE-etched in the SiO_2 which lands on the Si substrate. A 30 nm SiO_2 layer is then thermally grown again, which serves as the substrate insulator. A Ti/TiN/W metal layer is then deposited using sputter deposition for the Ti/TiN layer and CVD for the W

layer. The metal layer is then polished down to the underlying oxide layer using an Applied Materials Mirra CMP system, resulting in a planar surface with a patterned Ti/TiN/W microheater. The rest of the process is then identical to the Gen2 process, starting with the dielectric SiN deposition and ending with the 2nd interconnect metal formation.

The Gen3 process is a modification of the Gen2 process where the non-planar, etched-W microheater formation of the Gen2 process is replaced with a planar W-microheater formed using standard CMOS fabrication techniques. The reasoning behind developing the Gen2 process as well as the RF performance of the process is given in Sections 4.5, 4.6, and 4.7. A summary table of all process generations is given in Figure 2.5.

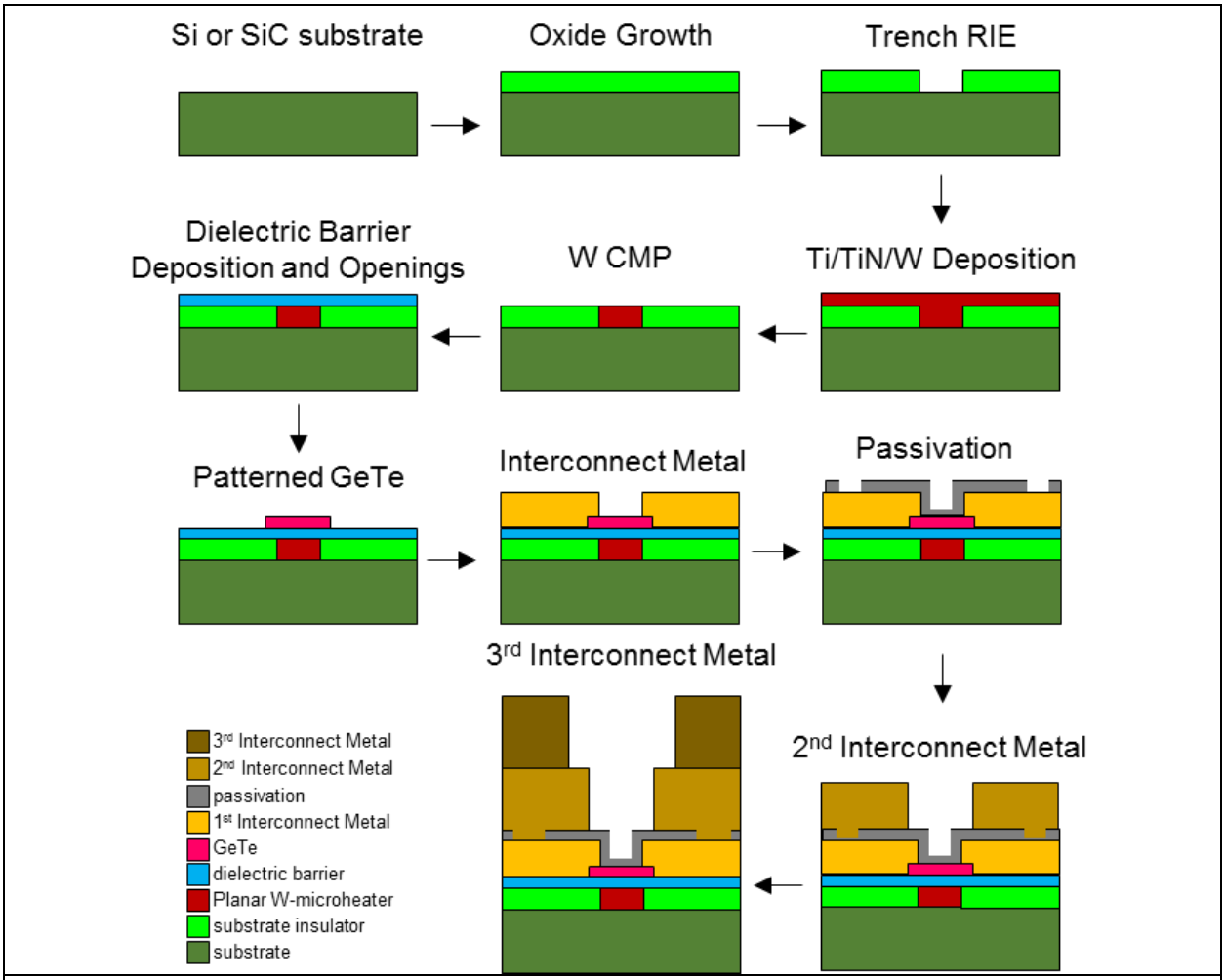


Figure 2.4 Schematic cross section of the Gen3 fabrication process flow for the 4-terminal, indirectly heated, phase-change switch, which uses planar CMP W-microheaters

Process	Substrate	Microheater	Dielectric Barrier	GeTe	1st IC metal	2nd IC metal	TSVs & Backside metal
Gen1	4" SiC or Si	Lift-Off NiCrSi	30-60 nm	75-120 nm	1.0 µm Ti/Au	N/A	N/A
e-Gen1	4" SiC or Si	Lift-Off NiCrSi	60 nm	75-120 nm	1.0 µm Ti/Au	4 µm Au	3 µm Au
Gen2	4" SiC or Si	etched-W	60 nm	110 nm	0.25 µm Ti/Au	4 µm Au	N/A
Gen3	6" Si	CMP W	60 nm	110 nm	0.25 µm Ti/Au	4 µm Au	N/A

Figure 2.5 Table comparing all process generations

2.4 Test

A variety of DC and RF tests are used to characterize the fabricated device and process flow. A description of each test, how they are performed, and what they are used for is included in each section.

2.4.1 DC Tests

2.4.1.1 Equipment

- Electroglas EG2001 Wafer Prober
- (2) Cascade ACP40 125 or 150GS probes
- (2) Keithley 237 Source Measurement Units (SMUs)
- Teledyne CCR-33S30 SPDT
- HP 8114A Pulse Generator (PG)
- HP DC power supply

2.4.1.2 Calibration

In addition to the equipment being calibrated and maintained by the test and calibration group at Northrop Grumman Mission Systems, on wafer calibration is done for 2-point measurements by landing the probes on a thru structure on wafer. This thru structure is simply a

single, continuous piece of metal in the either the 1st or 2nd interconnect metal. This measured resistance is then subtracted from all DC measurements using that probe during that test period.

2.4.1.3 Measuring Device Resistances and Pulsing of the Microheater

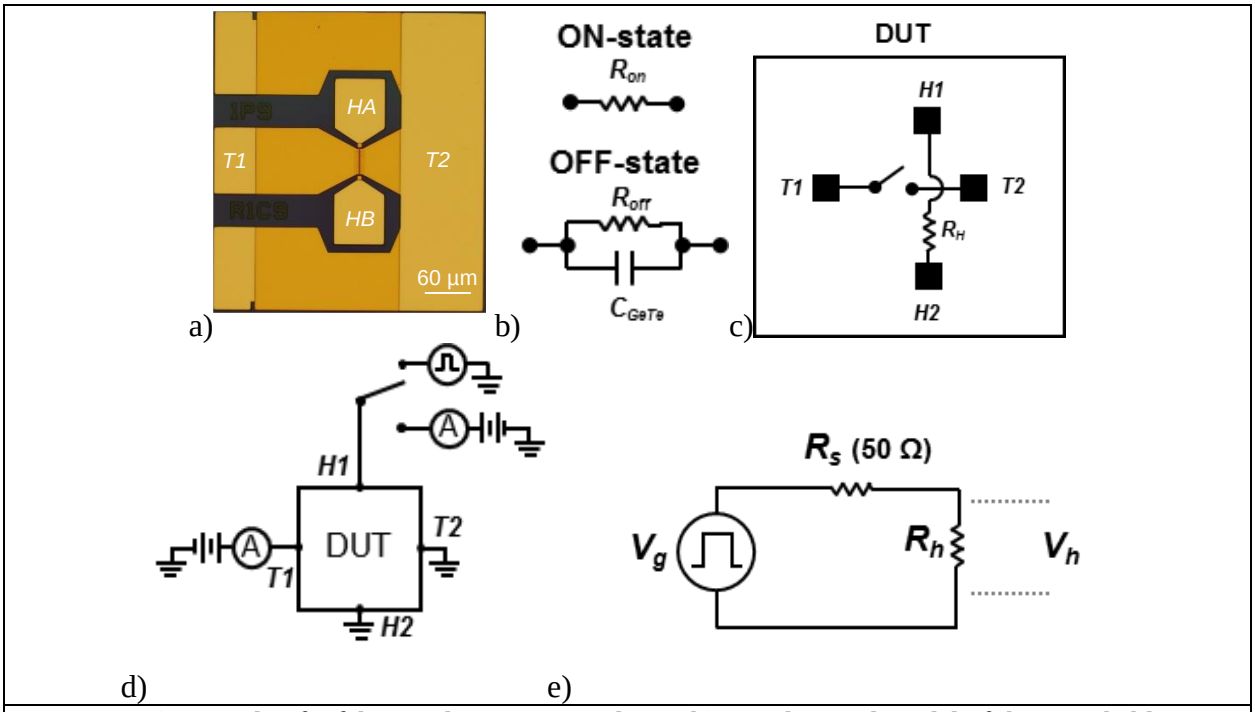


Figure 2.6 a) example of a fabricated 1-port IPCS device b) DC electrical model of the switchable GeTe channel c) model of the 1P device that includes the heater d) diagram of the test set up used to pulse and measure the device e) circuit diagram of the heater pulsing circuit

An example of a fabricated 1-port (1P) IPCS device is shown in Figure 2.6(a). The GeTe in the device (i.e. the switchable "channel") is modeled as a low-value resistor in the ON-state, and a high-value resistor in parallel with an ideal capacitor in the OFF-state, as depicted in Figure 2.6(b). The 4-terminal device is depicted in Figure 2.6(c), where microheater resides between terminals *H1* and *H2*, and the GeTe is represented as the switch between terminals *T1* and *T2*. A diagram of the test set-up for both of the above-mentioned studies is given in Figure 2.6(d). The resistance of the switch (R_{on} or R_{off}) and the heater (R_h) are measured by applying 0.05 V across the GeTe terminals (*T1* and *T2*), and 0.1 V across the microheater terminals (*H1*

and *H2*), and then measuring the current using a source measurement unit (Keithley 237). The measured DC R_{on} is an example of a DC measurement that can be translated to give insight into an RF metric (insertion loss in this case). The DC measurement excludes the effect of shunt capacitances, but can give a preview or estimation of the RF insertion loss in a quicker, less complicated measurement than a full RF test. It is helpful as a screen to know which devices to focus on for the RF test in order to save time.

Once the state of the device is known, the microheater is connected to an HP 8114A pulse generator, and the R_h is communicated to the pulse generator, as in Figure 2.6(e). The HP 8114A will then adjust its source voltage in order to accurately deliver the requested voltage pulse from the 50 Ω source impedance to the nominally unmatched (non-50 Ω) microheater. After the pulse is sent, the microheater is reconnected to the SMU and the resistance of the switch and microheater are re-measured. The applied pulse power (P_{app}) is defined as the calculated power based off the initial R_h and initial voltage of the pulse applied across the microheater (V_h): $P_{app} = V_h^2/R_h$. Of course, the actual applied voltage, microheater resistance, and instantaneous microheater power will all vary during the pulse depending on the temperature coefficient of resistance (TCR) of the microheater material used [47]. The R_{off} is measured 1 s after a desired OFF-pulse is sent. This is important as the OFF-state resistance drifts, as observed and analyzed in [48], [49].

The pulsing could easily be achieved with a pulse generator that does not account for the heater resistance. For example, if the heater resistance was not communicated to the pulse generator, and the pulse generator was set to assume a 50 Ω load impedance, the delivered voltage to the heater would need to be calculated:

$$V_h = \frac{R_h}{R_h+50} \cdot 2 \cdot V_{generator} \qquad (2.1)$$

where $V_{generator}$ is the voltage reported by the pulse generator.

2.4.1.4 Minimum Power to Amorphize (MPA)

The minimum power to amorphize (MPA) is defined as the minimum pulse power required to induce an increase in the switch resistance by a factor 10^4 when compared to the initial ON-state. This is a critical parameter to the device, as it determines the minimum pulse amplitude required to turn the switch OFF at a given pulse width. To determine the MPA at a given pulse width, pulses are applied with increasing pulse power until the 10^4 criteria is met, as shown in Figure 2.7(a). By determining the MPA at various pulse widths, amorphization curves can be created as shown in Figure 2.7(c), which show the minimum pulse power and pulse width combinations that can be used to turn off the device. Insight into the device and process can be gained by viewing the MPA data in a power-time effect plot, as done in [50] (all thermal simulations performed by Rob Young). Changes to the fabricated thicknesses of layers can significantly change the MPA, and is discussed further in Section 5.5.1.

2.4.1.5 Minimum Power to Crystallize (MPC)

The minimum power to crystallize (MPC) is defined as the minimum pulse power required to induce the switch resistance to decrease below 100 Ω. This is another important parameter to the device, as it determines the minimum pulse amplitude required to turn the switch ON at a given pulse width. To determine the MPC at a given pulse width, pulses are applied with increasing pulse power until the 100 Ω criteria is met, as shown in Figure 2.7(b). While the MPC is the power that determines what pulse can induce the crystalline phase in the device, it is not the optimal power used to obtain the lowest R_{on} in the device. In order to determine the optimal ON-pulse, the MPC test is continued until the resistance begins to rise again. The pulse power at which the R_{on} was the lowest is considered the optimal pulse to

crystallize (OPC). In the example MPC curve given in Figure 2.7(b), the MPC is the first point below 100 Ω (which occurs at 1.3 W), and the OPC occurs at 1.7 W.

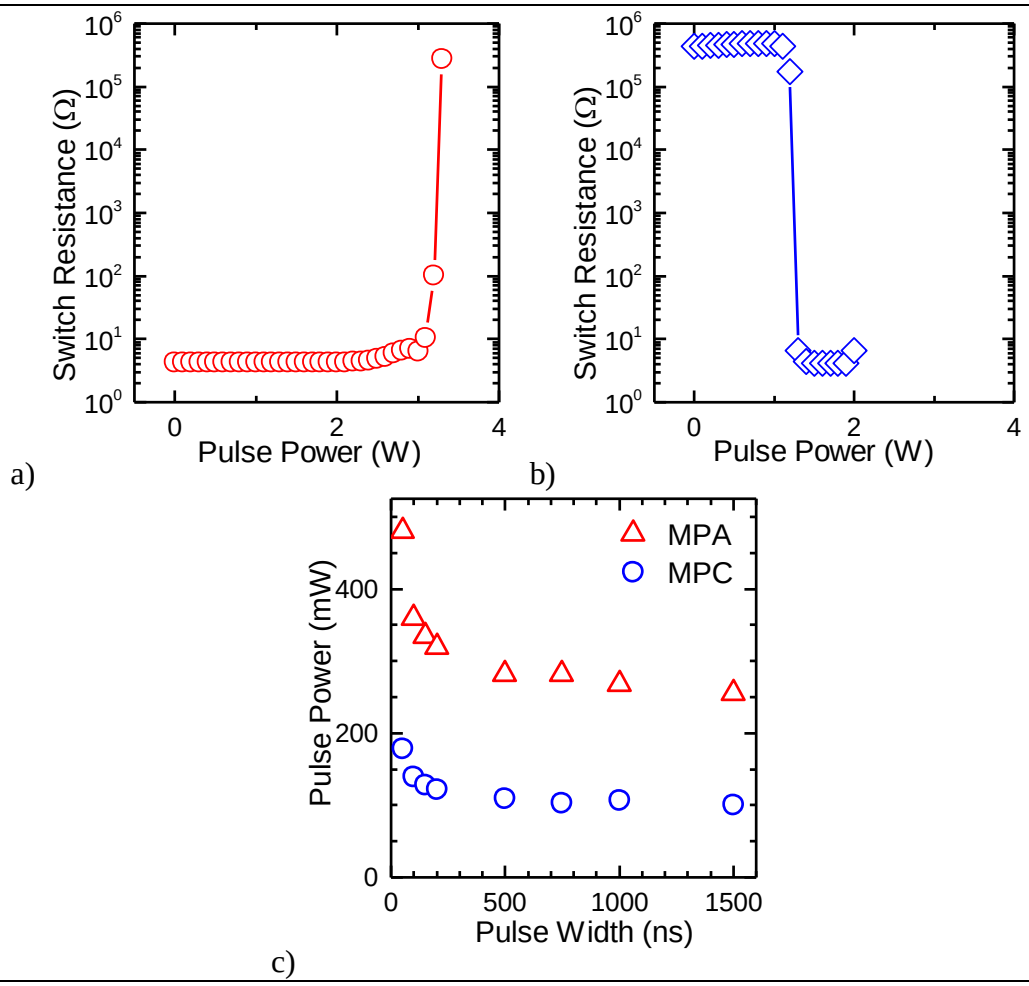


Figure 2.7 example a) MPA plot b) MPC plot c) amorphization and crystallization curves

2.4.1.6 Device Cycling

Device cycling is done with alternating OFF (amorphization) and ON (crystallization) pulses. Typically the OPC at a specific pulse width is used for the ON-pulse, once it is determined for a specific device on a specific wafer. In this thesis, 1500 ns pulse width is used almost exclusively for the ON-pulse, as it produces the lowest R_{on} more easily than smaller pulse widths. The OFF-pulse is then specified with a percentage above the MPA (e.g. 3.5% above MPA, 3.5% > MPA, or MPA +3.5%). To cycle the device, the pulses are then sent in alternating

fashion to turn the device ON and OFF, as seen in the example plot in Figure 2.8. There are variations on the cycling test where the switch and the heater resistances are not measured after every pulse, but rather after every 10, 100, 1000, or 10000 pulses in order to decrease the amount of time the cycling test takes. It is common that even after large quantities of pulses are sent (500,000+) the device is still working and functional, but the test is terminated due to test stand availability.

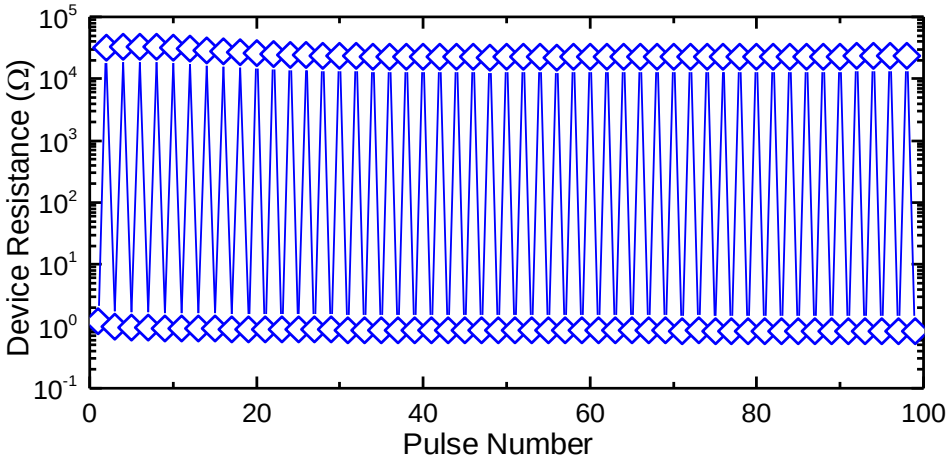


Figure 2.8 example plot of cycling data up to 100 pulses

2.4.1.7 Threshold Voltage Test (V_{th})

Once set in the desired OFF-state, the V_{th} test is performed by ramping the voltage on the SMU connected to *T1* and *T2* (in Figure 2.6) in 0.25 V increments (at an average ramp rate of 0.5 V/s), while monitoring the current. The compliance current is set to 1 mA and the voltage ramp was limited to 8 V, to avoid damaging a device and allow repeated measurements on the same device. The V_{th} is defined as after the inflection point of the OFF-state voltage sweep, which is the voltage at which the current reaches compliance. An example plot of V_{th} test on 6 different device layouts is given in Figure 2.9. The V_{th} is another parameter that can be mapped to RF performance, namely the OFF-state power handling ($P_{RF,max,OFF}$) which is covered in detail in

Chapter 4. Changes to the fabricated thicknesses of layers can significantly change the V_{th} of the device, and is covered in Section 5.5.1.

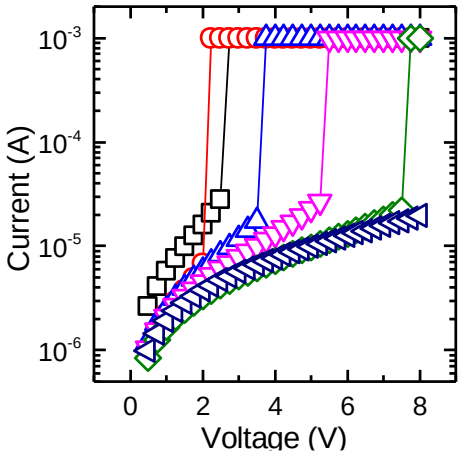


Figure 2.9 example plot of a V_{th} test, where the voltage is swept across the switch set in the OFF-state

2.4.2 RF Tests

2.4.2.1 Equipment

- Electroglas EG2001 Wafer Prober
- (2) Cascade ACP40 125 GSG probes
- (2) Cascade ACP40 S-only probe
- (2) Keithley 237 Source Measurement Units (SMUs)
- Teledyne CCR-33S30 SPDT
- HP 8114A Pulse Generator (PG)
- HP DC power supply
- Agilent PNA-X Network Analyzer
- Cascade Microtech 101-190 Cal Substrate

2.4.2.2 Calibration

In addition to the equipment being calibrated and maintained by the test and calibration group at Northrop Grumman Mission Systems, the RF test is calibrated using SOLT method with the two GSG ACP40 probes and the Cascade cal substrate. Once the SOLT cal is complete, it is verified by landing one probe at a time on the long open stub on the cal substrate, and verifying the smooth, inward spiral of the S11 or S22 on the smith chart with frequency. The DC resistance is calibrated similarly as before, by landing the probes on a thru structure on wafer. This thru structure is a single, continuous piece of metal in the either the 1st or 2nd interconnect metal. This measured resistance is then subtracted from all DC measurements using these probes during a single test period.

2.4.2.3 Small Signal RF Test

The goal of the small-signal RF test is to obtain the insertion loss and isolation of the DUT as a function of frequency. From insertion loss and isolation, the R_{on} and C_{off} can be extracted from equations 1.1 and 1.2 using the simplified F_{co} or $R_{on}*C_{off}$ model shown in Figure 2.10(a). The insertion loss and isolation are measured after calibrating the RF test (i.e. probes, cables, network analyzer on a cal substrate) and landing the probes on a 2-port (2P) series single-pole, single-throw (SPST) switch (pictured in Figure 2.10(b)) programmed in either the ON or the OFF-state. In all cases, the C_{off} is extracted from the isolation with no de-embedding done after calibration. In some cases, the R_{on} is extracted from the insertion loss after subtracting an on-wafer thru-line from the raw data. It is stated in this thesis when and where this is done. The programming pulse is sent to the heater in the exact same fashion as in Section 2.4.1.3, with the exception that two signal-only ACP40 probes are used instead of a single GS probe, in order for all the probes to be landed (if desired) at the same time. The 2P model for the series SPST is

shown in Figure 2.10(c) (with the corresponding shunt-SPST model), and the test circuit diagram (for S21) is shown in Figure 2.10(d) where the dotted lines represent the reference plane of the probes. The resulting S-parameters that are recorded are used to extract the insertion loss (IL) and isolation (ISO):

$$IL = -S_{21,reported,ON-state} \qquad (2.2)$$

$$ISO = -S_{21,reported,OFF-state} \qquad (2.3)$$

Where $S_{21,reported}$ is the reported magnitude of S21 in dB by the network analyzer.

The inherent problem with the F_{co} or $R_{on}*C_{off}$ model for any RF switching technology is that it forces a simplification of a complex device down into only a single resistor and capacitor. As seen in Figure 2.10(e) and Figure 2.10(f), the ON- and OFF-state model for the IPCS device is much more complicated than just a single resistor and capacitor. Further complicating the simplification (aside from the additional components) is the two additional heater terminals (*H1* and *H2*) that are intrinsically part of the device. Much like a CMOS MOSFET (which is also a 4-terminal device), how these terminals are terminated can greatly affect the insertion loss and isolation, as well as the reported F_{co} or $R_{on}*C_{off}$ numbers [45]. In order to be consistent with literature and the F_{co} or $R_{on}*C_{off}$ model, the RF extracted F_{co}, R_{on}, and C_{off} numbers that are reported in this thesis are extracted with the heater terminals left floating (see Figure 2.11). It should be noted that this is done in order to be ethical and consistent about the reported numbers, as it actually results in less attractive F_{co} and C_{off} results [12] and is discussed further in Section 3.3.3. It should also be strongly noted that while this is done to be ethical and consistent, it does not represent how a switch would actually be implemented in an RF system. The most common implementation would be to have the one heater terminal DC grounded and the opposite heater terminal RF grounded. The effects of the "grounded vs. floating" insertion loss and isolation are

discussed in detail in Section 3.3.3, with comments about how to limit these effects from a fabrication and integration point of view. In all reported insertion loss and isolation numbers in this thesis it is stated whether the measurements are taken with the heater terminals grounded or floating, and where possible both measurements are shown.

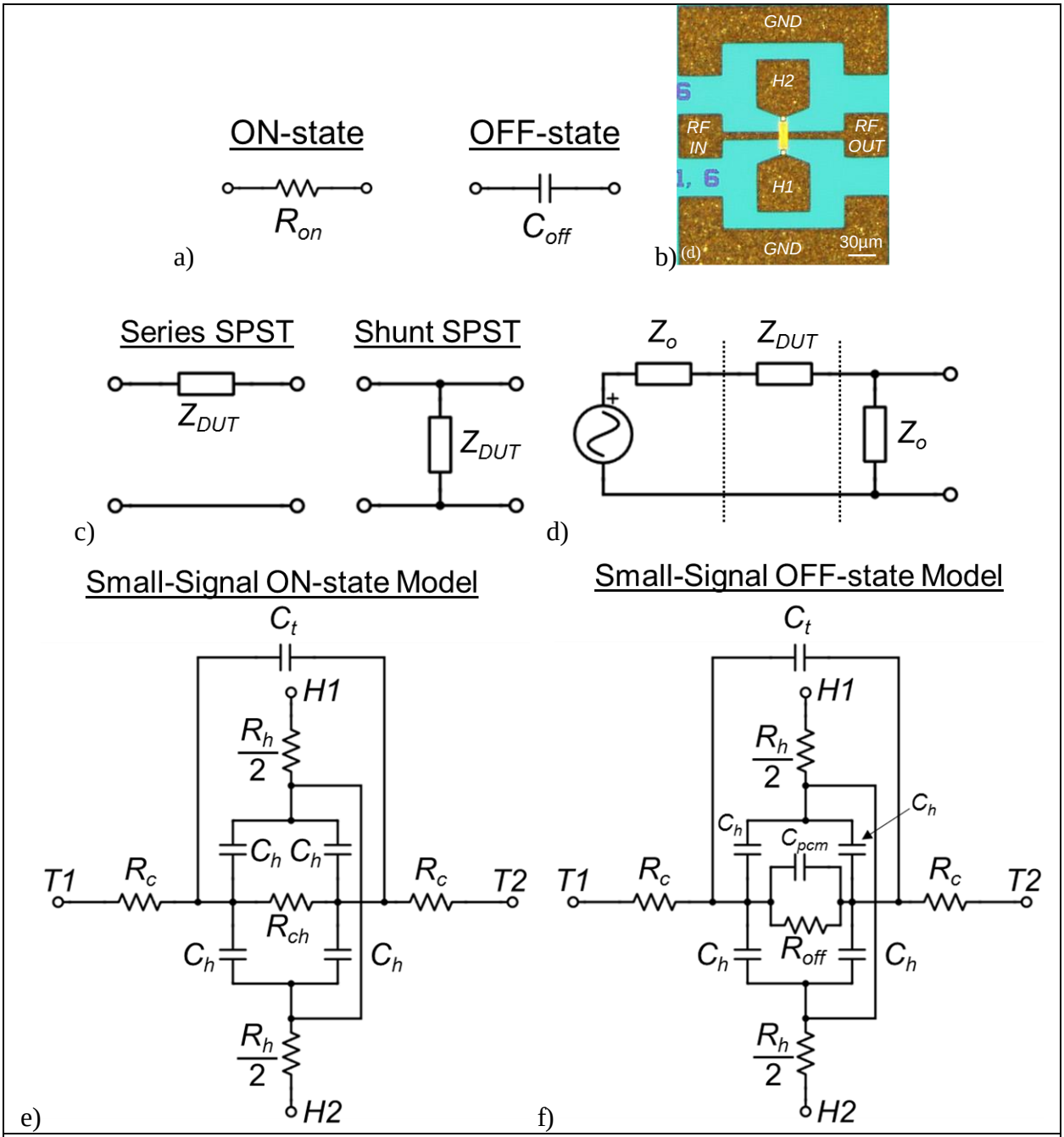


Figure 2.10 a) 2-terminal circuit model used for F_{co} and R_{on}*C_{off} extractions b) optical microscope picture of a 2-port SPST fabricated in the Gen3 process c) 2-port model of a series and shunt SPST d)

2-port circuit diagram of an S21 measurement of a series SPST, where the dotted lines represent the reference plane of the probes e) realistic small-signal circuit model for the IPCS device in the ON-state and f) realistic small-signal model for the IPCS device in the OFF-state

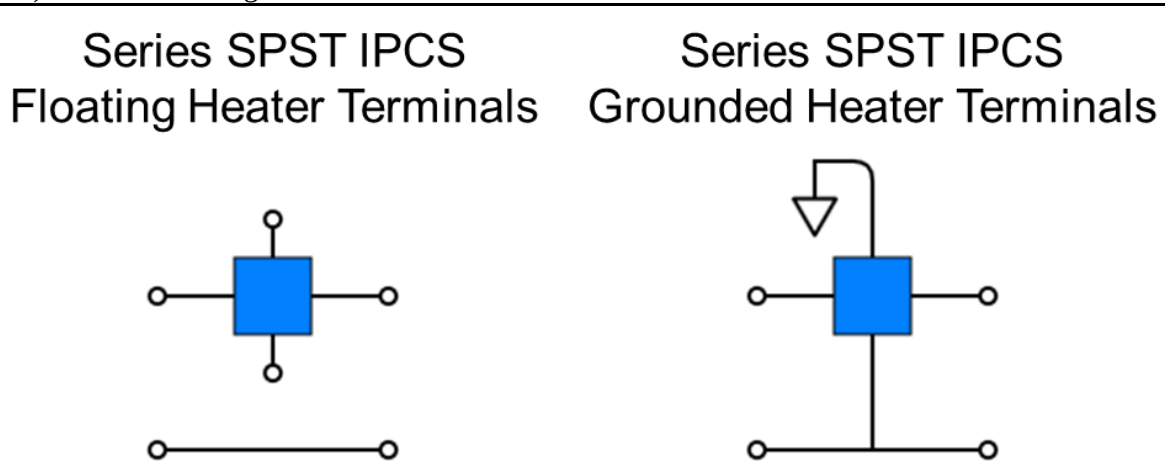
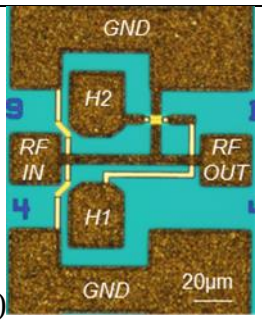


Figure 2.11 2P schematic showing the floating heater terminations (left) and grounded heater terminations (right) of the a series SPST implementation of an IPCS device

2.4.2.4 Power Handling Test

Power handling tests are performed on 2P shunt SPST devices, as pictured in Figure 2.10(c) and Figure 2.12(a) and Figure 2.12(b). A 10-GHz continuous-wave RF signal was applied to the input port, where the time-averaged signal power was discretely ramped from 0 dBm to 30 dBm in steps of 0.5 dBm, holding for 1 s at each power level. Between power steps, a DC resistance measurement was made on the shunt switch to determine if it was still in the OFF-state (finite resistance) or if it had been catastrophically destroyed (open circuit). The power level at which the switch resistance changed to an open circuit was recorded as the $P_{RF,max,OFF}$ of the switch. The results of this test are discussed in Section 4.7.

a) 

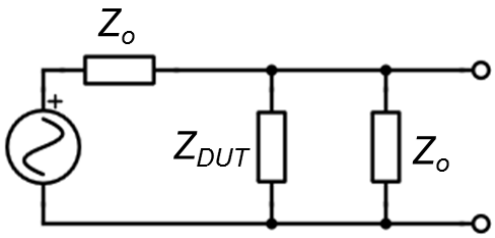
b) 

Figure 2.12 example plot of a V_{th} test, where the voltage is swept across the switch set in the OFF-state

2.5 Conclusion

In this chapter the methods of fabrication, process flows, DC and RF tests have been described. Diagrams of the process flows along with specifications of the fabrication details have been given for 3 different process generations discussed in this thesis. The equipment, calibration, and execution of the different DC tests has also been discussed. The importance of each test, along with example data has been given to help the reader understand more deeply the reported numbers in the subsequent chapters. Finally, the RF tests have been detailed, with explanations for the different extractions of the RF parameters. Care has been given to explaining the differences and consequences of different microheater terminations.

3 Demonstration and Performance of 4-Terminal, Indirectly Heated Phase-Change Switch (Inline Phase-Change Switch)

3.1 Abstract

An inline chalcogenide phase-change radio-frequency (RF) switch using germanium telluride and driven by an integrated, electrically isolated thin-film heater for thermal actuation has been fabricated. A voltage pulse applied to the heater terminals was used to transition the phase-change material between the crystalline and amorphous states. An ON-state resistance of 4.5 Ω (0.08 Ω-mm) with an OFF-state capacitance and resistance of 35 fF and 0.5 MΩ respectively, were measured resulting in an RF switch cutoff frequency (F_{co})of 1.0 THz and an OFF/ON resistance ratio of 10^5. The output third-order intercept point measured >55 dBm, with zero power consumption during steady-state operation, making it a nonvolatile RF switch. This is the first reported implementation of an RF phase change switch in a four-terminal, inline configuration. Improvements to the GeTe inline phase-change switch have resulted in an ON-state resistance of 0.9 Ω (0.027 Ω·mm) with an OFF-state capacitance and resistance of 14.1 fF and 30 kΩ, respectively, resulting in a calculated F_{co} of 12.5 THz. This represents the highest reported Fco achieved with chalcogenide switches to date. The threshold voltage (V_{th}) for these devices was measured at 3V and the extracted ON-state third-order intercept point (TOI) was 72 dBm. Single-pole, single-throw (SPST) switches were fabricated, with a measured insertion loss less than 0.15 dB in the ON-state, and 15dB isolation in the OFF-state at 18 GHz. Single-pole, double-throw (SPDT) switches were fabricated using a complete backside process with through-substrate vias, with a measured insertion loss 0.25 dB, and 35dB isolation.

3.2 Initial Demonstration of 4-terminal, indirectly heated, phase-change switch

3.2.1 Introduction

Chalcogenide phase-change materials (PCMs) have been exploited for their unique optical characteristics since their discovery in the late 1960s [26]. Recently, the digital memory industry also began exploiting PCMs for their distinct phase-dependent electrical properties [27], [31]. PCM devices are based on a vertical architecture, which offers increased memory density and improved switching speed over flash memory.

Unlike digital applications where the dominant requirement is a large dc OFF/ON ratio, radio-frequency (RF) applications require switches with a low ON-resistance and OFF-capacitance. In solid-state switching devices, OFF-state capacitance can be improved by changing the device geometry, but only at the expense of degraded ON-state resistance, and vice

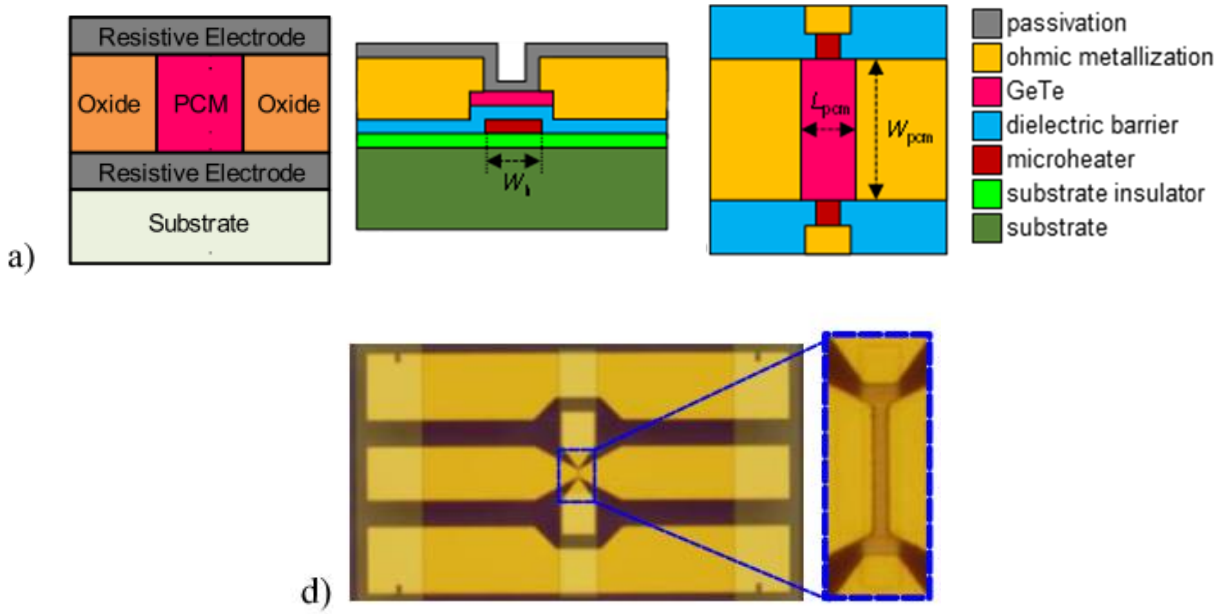


Figure 3.1 (a) Cross section of the conventional vertical PCS architecture where the control current flows directly through the PCM producing one of the two heating profiles shown in Figure 1.4 , resulting in phase transformation. (b) Cross-sectional schematic diagram of the IPCS and its constituent layers. (c) Top-side view of the switch showing the control signal path and the RF signal trace, not showing the passivation. (d) Fabricated 1.0-THz single-pole, single-throw CPW IPCS switch before measurement, with a zoomed-in-view on the IPCS region.

versa. The ultimate performance is limited by the sheet resistance of the switchable channel. The sheet resistance of switchable PCM films, such as germanium telluride (GeTe), can be more than an order of magnitude lower than that of state-of-the-art FETs, allowing for a lower switch ON-resistance for the same or similar device geometry. In addition to improved performance, PCM switches also possess the unique characteristic of zero prime power consumption during steady-state operation, making them nonvolatile switches.

3.2.2 Device Structure, Fabrication, and Operation

A cross-sectional schematic of the Gen1 fabricated device (described in 2.3.1) is shown in Figure 3.1. To convert the PCM to the amorphous state, a short voltage pulse was applied across the TFR terminals, causing an increase in the TFR temperature due to joule heating. The heat from this pulse conducts from the TFR through the dielectric barrier to the proximal PCM above it, raising the temperature of the PCM above its melting point of 725 °C [51] by the end of the pulse. The natural cooling that takes place at the end of the pulse (with heat being conducted into the underlying substrate and surrounding contact metallization) is rapid enough to freeze the atoms of the PCM in the amorphous state. The length of the cooling cycle is a function of the material configuration around the PCM and TFR and was optimized before device fabrication using finite element thermal modeling software. To convert the amorphous PCM back to the crystalline state, a lower intensity pulse was applied across the heater, causing the temperature of the PCM to rise above the recrystallization temperature (~190 °C) but remain below the melting temperature through the duration of the pulse.

3.2.3 Results

GeTe was used as the PCM for this device as it demonstrates the lowest resistivity in the crystalline state relative to other chalcogenides typically used as PCMs [29]. Deposition was

done in a Kurt J. Lesker sputter deposition tool. A power-pressure matrix was used for resistivity optimization. Recrystallization temperatures varied from 186 °C to 190 °C depending on the deposition parameters. It was also confirmed through four-point probe and Hall measurements that the crystalline GeTe exhibits p-type conductivity behavior.

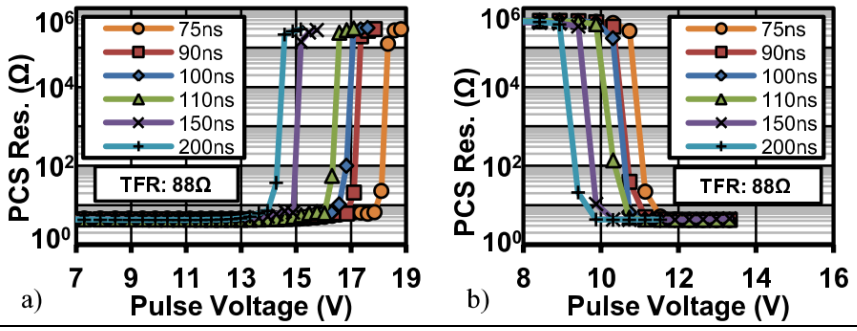
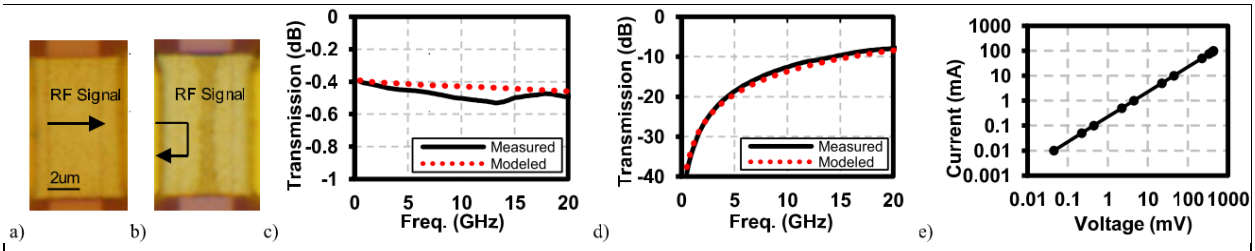


Figure 3.2 Measured (a) pulse voltage to amorphize and (b) pulse voltage to recrystallize for different pulsewidths on the 1.0-THz switch. The x-axis shows the voltage of the pulse through the 88 Ω TFR, and y-axis shows the resulting PCS (GeTe) line resistance.

Using the fabrication process described, different layouts of the IPCS were fabricated with L_{pcm} ranging from 1 to 7 µm and W_{pcm} ranging from 6 to 50 µm [Figure 3.1]. Figure 3.1(d) shows the fabricated single-pole, single-throw switch with a magnified view of the IPCS area. Figure 3.2 shows the GeTe line resistance as a function of TFR pulse voltage and pulse width. Once set in the amorphous (OFF) or crystalline (ON) state, the switch consumed no power, making it a nonvolatile switch. The switches were successfully cycled 1500 times between the ON and OFF states before the test was terminated due to time constraints. Figure 3.3(a) and (b) shows magnified views of a different fabricated IPCS in the ON and OFF states to demonstrate the optical difference between the crystalline and amorphous states of GeTe film. Figure 3.3(b) shows the IPCS in the OFF-state with a clearly defined darkened stripe down the center of the GeTe, which is orthogonal to the RF signal trace. This darkened stripe is the amorphous GeTe that prevents horizontal current flow. Figure 3.3(c) and (d) shows the measured and modeled

insertion losses and isolation for the fabricated two-port coplanar waveguide (CPW) single-pole, single-throw IPCS of Figure 3.1(d) (simulations of the model performed by Pavel Borodulin). For a switch with PCS width of 18 µm, insertion loss measured <0.5 dB up to 18 GHz. The measured isolation of 9 dB at 18 GHz is attributed to the coupling of the RF signal through the heater and coupling through the CPW gap capacitance. The figure of merit commonly used for RF switches is the ratio of OFF-impedance to ON-impedance, referred to as cutoff frequency (F_{co}):$1/(2\pi \cdot R_{on} \cdot C_{off})$. The GeTe IPCS measured in Figure 3.3 had an F_{co} of 1.0 THz, limited by the large width of the heater and large PCS length. Figure 3.4 shows power handling data and measured output third-order intercept (OTOI) for the measured IPCS (measurements performed and values calculated by Pavel Borodulin). The ON-state power handling capability of the switches was measured at 33.4 W/mm of device width (W_{pcm}) with the switch of Figure 3.4(a) capable of handling over 0.6 W (27.8 dBm) continuous wave input RF power at 3 GHz. OFF-state breakdown voltage or threshold switching voltage of these devices has not yet been measured. Figure 3.4(b) shows measured third-order intercept data of >55 dBm and potentially better, as all three measurements were limited by the test set noise floor. The same switch could handle >100 mA of DC current without failure, as shown in Figure 3.3(e). Figure 3.3(f) lists measured data on four different IPCS layouts.



PCS Length	PCS Width	TFR Width	R_{on} (Ω)	R_{off} (MΩ)	Off/On	C_{off} (fF)	F_{co} (THz)
2µm	10µm	3.5µm	8.35	2.15	$2.6x10^5$	17.96	1.1
3µm	10µm	3.5µm	13.56	1.91	$1.4x10^5$	16.28	0.7
2µm	18µm	4.8µm	4.48	0.52	$1.2x10^5$	35.14	1.0
3µm	18µm	4.8µm	6.83	0.47	$6.9x10^4$	30.72	0.8

f)

Figure 3.3 (a) and (b) IPCS switch in the crystalline and amorphous states. It is worth noting that only a limited area in the center of the IPCS was amorphized. (c) and (d) Measured and modeled insertion loss (ON-state transmission) and isolation (OFF-state transmission) are shown for the 1.0-THz single-pole, single- throw IPCS switch with 2-µm PCS length and 18-µm PCS width. Red dashed line shows the modeled data, whereas the black solid line shows the measured data. (e) DC I–V measurements from 0.01to 100 mA of the same 1.0-THz IPCS switch (f) Table showing RF results for devices described in Section 3.2.3

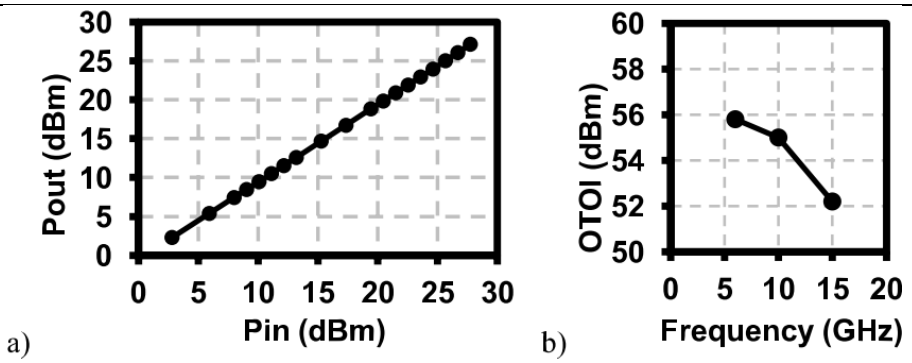


Figure 3.4 (a) Measured Pout versus Pin for the 1.0-THz Fco switch at 3 GHz, showing 33.4 W/mm of CW power handling. (b) Measured OTOI showing >52 dBm across three frequencies, limited by the test set

3.3 Performance Optimization and Circuit Demonstrations

3.3.1 Introduction

The first demonstration of a functional chalcogenide RF inline phase-change switch (IPCS) was discussed in detail in section 3.2. This device employed an initial design intended to

demonstrate the ability to quench chalcogenide PCM in the amorphous state utilizing an integrated, electrically isolated thin-film heater in a horizontal configuration. While only intended to demonstrate the concept for functionality, this design nonetheless achieved an F_{co} of 1.0 THz, which outperforms traditional FETs in frequency performance [14]. By altering device geometry to optimize the complex electro-thermal actuation mechanism, significant performance improvements have since been realized and fabricated into state-of-the art RF circuits.

3.3.2 Coplanar Waveguide SPST Optimizations

Using the fabrication process described Section 3.2.2, different layouts of the IPCS switch were fabricated in order to decrease R_{on}, C_{off}, and hence improve the insertion loss, isolation, and F_{co}. Referring to circuit model in Figure 2.10(f), in order to decrease the C_{off} of the device, C_t, C_{pcm}, and C_h need to be minimized. Of these three capacitances, C_h is the largest contributor (as determined by simulations done by Pavel Borodulin), as it affects both the C_{off}, isolation, and insertion loss. In order to reduce C_h, smaller linewidth microheaters (W_h in Figure 3.1) between 0.5 µm and 2.5 µm are used (compared to the devices reported in Section 3.2.3), and a thicker SiN dielectric barrier (60 nm) is used between the GeTe and the microheater.

Referring to Figure 2.10(e), in order reduce the R_{on} of the device, R_c and R_{ch} need to be minimized. By optimizing the sputter deposition and crystallization processes, contact resistances to the GeTe of 0.001 Ω·mm were measured by standard 100 µm wide TLM (transmission line model) structures. This results in R_{ch} being the dominant resistance between the two. In order to reduce R_{ch}, traditional 3-dimensional layout and processing thicknesses were modified. Compared to the devices reported in Section 3.2.3, smaller device lengths (L_{pcm} in Figure 3.1) between 0.9 µm to 2.5 µm, larger device widths (W_{pcm} in Figure 3.1) between 10 µm and 30 µm, and a thicker GeTe material (120 nm) were used.

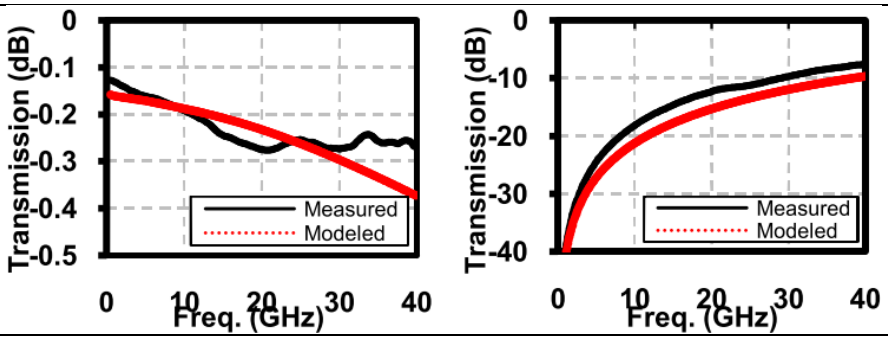
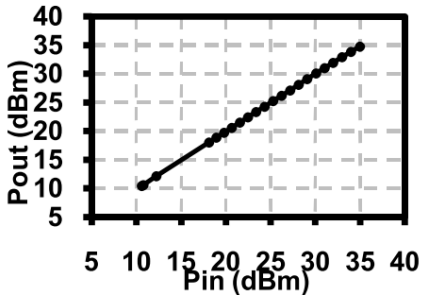


Figure 3.5 Measured and modeled (a) insertion loss (ON-state transmission) and (b) isolation (OFF-state transmission) for a single pole, single throw switch with 0.9um PCS length and 30um PCS width. The red dashed line shows the modeled data, while the black solid line shows the measured data.

Switching between the two states was achieved with electrical pulse powers ranging from 0.5 W to 4 W (depending on the pulse width), and pulse widths ranging from 30 ns to 1.5 µs. The GeTe IPCS switches were successfully cycled 10,000 times between the ON- and OFF-states before the test was terminated due to time constraints. Figure 3.5 shows the measured and modeled insertion loss and isolation for the fabricated 2-port coplanar waveguide (CPW) single-pole, single-throw switch with dimensions listed in Figure 3.6 (simulations of the model performed by Pavel Borodulin). For a switch with PCS width of 30 µm, insertion loss measured better than 0.3 dB up to 40 GHz. The measured isolation of 13 dB at 18 GHz is attributed to the coupling of the RF signal through the heater and to the coupling through the CPW gap capacitance. The featured GeTe IPCS device had an F_{co} of 7.3 THz, limited by the width of the heater and dielectric barrier thickness between the GeTe and heater. Figure 3.6(a) shows power handling data for the GeTe IPCS switches. The power handling capability of the 7.3 THz switch was measured at 3.1 W continuous wave RF power at 10 GHz (measured by Pavel Borodulin), or 104.7 W/mm when normalized for periphery. OFF-state breakdown voltage or threshold switching voltage of these devices was not measured. Similar to the previous devices fabricated in Section 3.2.3, these IPCS devices had measured third-order intercept data of greater than 55

dBm and potentially better, as all measurements were limited by the test set dynamic range. Figure 3.6(b) shows measured data on 3 different switch layouts. The increase in performance over the devices listed in Section 3.2.3 is attributed to the increased GeTe thickness (120 nm vs. 75 nm), increased SiN barrier thickness (60 nm vs. 30 nm), smaller RF contact spacing (0.9 µm vs. 2.0 µm), smaller TFR width (1.7 µm vs. 4.8 µm), and a larger device width (30 µm vs. 18 µm), which all serve to decrease the R_{on} from 4.48 Ω to 1.2 Ω and the C_{off} from 35 fF to 18 fF.



a)

PCS Length	PCS Width	TFR Width	R_{on} (Ω)	R_{off} (MΩ)	Off/On	C_{off} (fF)	F_{co} (THz)
0.9µm	10µm	1.7µm	3.7	1.47	$4.0x10^5$	7.7	5.7
0.9µm	20µm	1.7µm	1.8	0.17	$9.7x10^4$	13	6.8
0.9µm	30µm	1.7µm	1.2	0.11	$9.2x10^4$	18.1	7.3

b)

Figure 3.6 a) Measured Pin vs. Pout for the 7.3 THz Fco switch at 10 GHz, showing 104.7 W/mm of CW power handling b) summary of results

3.3.3 Microstrip Designs Optimizations and Notes on RF Measurements

In order to improve the SPST RF performance and show improved aspects of integration, microstrip designs were fabricated to show better insertion loss and isolation from the entire SPST structure. Using the e-Gen1 fabrication process described in 2.3.1, IPCS were fabricated with the improved layout dimensions and layer thicknesses described in the previous section with the new microstrip designs (RF device layout design and simulations performed by Pavel Borodulin). Figure 3.7(a) shows a fabricated SPST switch utilizing a microstrip design, with a magnified view of the IPCS area. All devices are pulsed with an HP8114A pulse generator, utilizing a 10 ns rise and fall time. Figure 3.7(b) shows an IPCS device cycled for 100 pulses, using alternating ON and OFF pulses. A 100 ns voltage pulse was used to set the device

in the OFF-state, and a 1500 ns voltage pulse was used to set the switch in the ON-state. The switch had an initial R_{on} of 1.2 Ω, but stabilized to 0.9 Ω after 5 cycles.

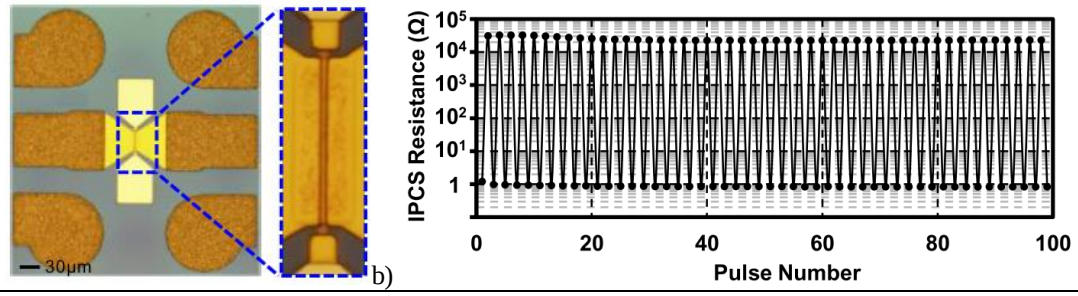


Figure 3.7 a) optical view of fabricated IPCS SPST using a microstrip design, with a close-up of the IPCS switch area b) measured resistance of the 12.5 THz IPCS device as a function of pulse number, using alternating ON and OFF pulses for 100 pulses. A 100-ns pulse was used to set the device in the OFF-state, and a 1500-ns pulse was used to set the switch in the ON-state

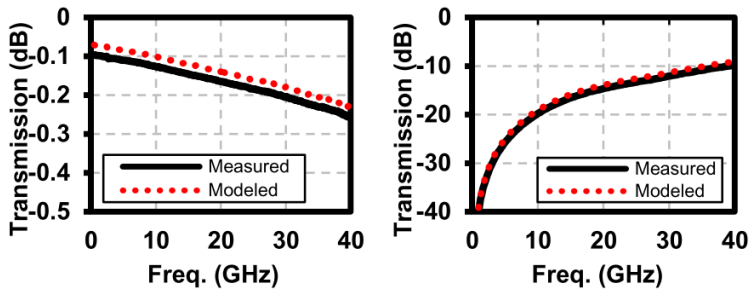
Figure 3.8 lists the device dimensions, measured R_{on}, R_{off}, V_{th}, C_{off}, and calculated F_{co} for 3 different IPCS configurations. It is observed that the C_{off} increases with increasing TFR width, which is consistent with RF simulations. By optimizing device geometry and pulse parameters to minimize R_{on} and C_{off}, an F_{co} of 12.5 THz was achieved. This represents the highest reported value for chalcogenide switches to date. Figure 3.8 (a) shows the measured and modeled insertion loss and isolation for the 12.5 THz switch. The insertion loss measured less than 0.25dB from 0-40 GHz, and measured 0.15dB at 18 GHz. The third-order intercept (IP3) for all 3 devices measured 72 dBm in the ON-state. The measured isolation was 15 dB at 18 GHz, primarily attributed to the parasitic capacitance through the TFR. All RF measurements are taken without de-embedding the CPW or microstrip pads, with the reference plane being the RF probe tips. The C_{off} for these devices was extracted from the measured isolation with the TFR contact pads floating (disconnected from the pulse generator). This is done intentionally, as the connection of the TFR pads to an unknown load can lead to inconsistent and incorrect extractions of the C_{off} on 2-port structures, as mentioned in Section 2.4.2.3. Figure 3.9(a) shows

the switch response when the TFR pads are terminated to ground. The isolation of the 2-port IPCS SPST with a grounded TFR is significantly higher, due to reduced capacitive coupling through the TFR. The energy that normally couples from port 1 to port 2 through the TFR is partially reflected and partially dissipated in the TFR, increasing the overall isolation at the expense of some increased insertion loss. This could potentially lead to a false assumption in the cutoff frequency and improper evaluations of the switch, as the lower isolation at port-2 (due to the shunt element) decreases the perceived extracted C_{off} by more than 110%, as seen in Figure 3.9(b).

In order to limit this effect and align the grounded vs. floating insertion loss and isolation, the shunt microheater capacitance (C_h) needs to be minimized. This can be done by reducing the microheater width (W_h), increasing the dielectric barrier thickness, or by using dielectric materials with a lower dielectric constant. When the heater is completely decoupled, the grounded data will resemble the floating data, meaning less frequency dependence of the insertion loss.

A further complicating issue is the capacitance added by the heater actuation pads (large metal pads where the probes make contact to H1 and H2). While not part of the intrinsic device, these pads are quite large (on the order of 50 µm to 100 µm), and add a significant capacitance in parallel to the C_h that cannot be eliminated by dielectric thickness changes (discussed in detail in [52]). Integration changes are required to eliminate or reduce this capacitance, and are discussed more in Section 5.4.

a)



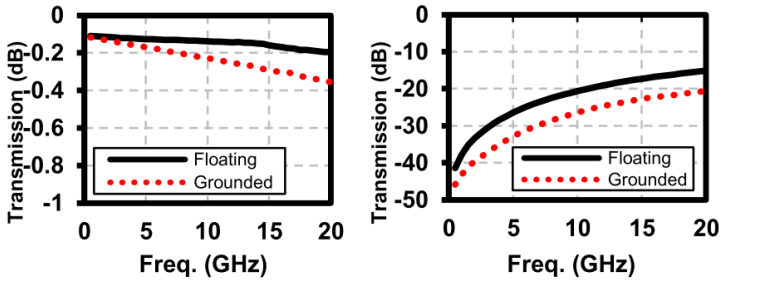
b)

GeTe IPCS Measured Results

IPCS Length	TFR Width	IPCS Width	R_{ON} (Ω)	R_{OFF} (kΩ)	V_{TH} (V)	C_{OFF} (fF)	F_{CO} (THz)
0.9um	0.9um	30um	0.90	26.9	2.09	14.1	12.5
0.9um	1.3um	30um	0.92	31.5	2.72	16.5	10.5
0.9um	1.7um	30um	0.91	35.3	3.31	18.2	9.6

Figure 3.8 a) Measured and modeled (left) insertion loss (ON-state transmission) and (right) isolation (OFF-state transmission) for a 12.5 THz SPST IPCS with 0.9um PCS length and 30um PCS width. b) table of measured results for microstrip devices

a)



b)

Measured IPCS Devices With Floating & Grounded TFR Contacts

TFR Contacts	IPCS Length	TFR Width	IPCS Width	R_{ON} (Ω)	C_{OFF} (fF)	F_{CO} (THz)
Floating	0.9um	0.9um	20um	1.41	15.2	7.5
Grounded	0.9um	0.9um	20um	1.40	7.2	15.8

Figure 3.9 a) Measured a) insertion loss (ON-state transmission) and b) isolation (OFF-state transmission) for the two different heater configurations. It is worth noting the two measured switches were 20um in IPCS width, as opposed to the switches in Figure 3.8 that were 30um wide b) table of measured results

3.3.4 Gen1 Device Performance Summary and Optimization Path

A summary of the devices reported on for the two different Gen1 process variants is summarized in Figure 3.10. In general, a clear improvement in RF performance is seen with increasing layer thicknesses, and decreasing layout dimensions. The 3 main drawbacks of increasing the layer thicknesses (preventing their indefinite increase) to increase RF performance

are the increased MPA, the decreased V_{th} (discussed in 4), and the decreased quench or ability to amorphize (discussed in Chapter 5).

In order to improve RF performance while maintaining reasonable processing thickness and secondary switch qualities, higher performance materials and integrations need to be incorporated into the device. Higher thermal conductivity dielectric materials such as AlN [53] can significantly improve the RF, MPA, V_{th}, and reliability by decreasing the thermal resistance between the microheater and GeTe. This would allow the thickness to be increased to the point where the heater is completely decoupled from the RF signal path, as demonstrated in [54]. Improving the material resistivity of the chalcogenide is another material change will significantly improve the overall device performance. Lower resistivity chalcogenides (as demonstrated in [52]) instantly improve device, as a thinner material is now needed for the same R_{on} (resulting in a lower MPA and larger V_{th}), or a lower R_{on} is achieved for the same thickness.

While improving the device with material changes is essential for future RF performance gains, understanding the trade-offs and relationships between all the device parameters (not just R_{on} and C_{off}) and device fabrication is critically important in developing the device into a viable switch technology. These trade-offs and relationships are discussed in the first half of Chapters 4 and 5. Once these relationships are understood, creating an integration to maximize all of the desired aspects of a switch is of utmost importance. These integrations are the focus of the second half of Chapters 4 and 5. Before they are discussed, the circuit performance of an SPDT built in the e-Gen1 process is discussed and compared to SPDTs created in other switch technologies.

Process	Sub.	(μm) L_{pcm}	(μm) W_{pcm}	(μm) W_h	(nm) SiN t	(nm) GeTe t	(Ω) R_{on}	(fF) C_{off}	(THz) F_{co}
Gen1	SiC	2.0	10.0	3.5	30	75	8.35	17.96	1.1
Gen1	SiC	3.0	10.0	3.5	30	75	13.56	16.28	0.7
Gen1	SiC	2.0	18.0	4.8	30	75	4.48	35.14	1.0
Gen1	SiC	3.0	18.0	4.8	30	75	6.83	30.72	0.8
Gen1	SiC	0.9	10.0	1.7	60	120	3.7	7.7	5.6
Gen1	SiC	0.9	20.0	1.7	60	120	1.8	13	6.8
Gen1	SiC	0.9	30.0	1.7	60	120	1.2	18.1	7.3
e-Gen1	SiC	0.9	30.0	0.9	60	120	0.9	14.1	12.5
e-Gen1	SiC	0.9	30.0	1.3	60	120	0.92	16.5	10.5
e-Gen1	SiC	0.9	30.0	1.7	60	120	0.91	18.2	9.6

Figure 3.10 summary of the reported devices for the two different Gen1 process variants

3.4 Single-Pole, Double-Throw (SPDT) Switch Circuit Performance

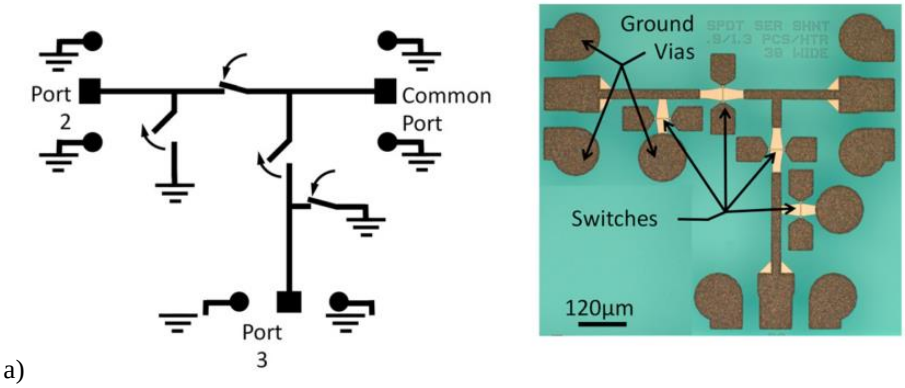
Using the switch in Figure 3.7(a), a series-shunt single-pole double-throw (SPDT) switch was fabricated, a widely used configuration found throughout the RF industry and a common means for comparing switch to switch performance [13]. The schematic in the upper left of Figure 3.11(a) shows that this is constructed from four individual switches, where sending the RF signal to Port 2 is accomplished by setting its series switch to the ON-state and the shunt to ground switch to the OFF-state, while Port 3's switches are toggled to the opposite states to set Port 3 into isolation. RF testing and calibration was similar to that of the CPW SPST switch, using a DC probe to pre-configure the four switches of the SPDT leaving the heaters floating. No on-wafer through was subtracted, and the RF test results after off-wafer calibration are reported here with the RF launches included with no de-embedding. Two RF ground-signal-ground probes were used between the common and port-2. Port-3 was 50 Ω terminated on-wafer (not visible in the photograph) with thin film NiCrSi resistors. Figure 3.11(a) shows the insertion loss

and Figure 3.11(b) shows the isolation for the phase-change SPDT switch in comparison to other RF switch technologies. All of the solid-state technologies and the phase-change switch use a SPDT series-shunt configuration, while the MEMS and VO_2 SPDTs uses only two series switches to achieve its SPDT with no shunts to ground. The data from the alternate switch technologies in Figure 3.11 is reproduced from published data, referenced below.

The GaN HEMT [55], GaAs pHEMT [13], and Si CMOS [3] SPDT devices are observed to have increasingly poor insertion loss at higher frequencies. The GaN SLCFET [2] also exhibits degraded insertion loss with frequency, but to a much smaller extent than the GaN HEMT due to the increased channel conductivity. The AlGaAs diode [6] and VO_2 [22] SPDT exhibit good insertion loss and isolation, with the VO_2 switch showing the best isolation. As mentioned in Section 1, the AlGaAs diode and VO_2 device consume prime power during operation, with the diode consuming 40 mW per switch [6] and the VO_2 device consuming 100 mw per switch [22]. The relatively poor MEMS [12] isolation could be improved by adding shunt switches to its series circuit topology, at the expense of more chip area. The CMOS device is fabricated on a relatively low-resistivity substrate, impairing the insertion loss and increasing the importance of its size optimization. A buried oxide was used to enhance RF isolation, which could be further improved by changing to a high-resistivity substrate or by increasing the buried oxide thickness [9].

The phase-change switch SPDT exhibits the lowest insertion loss of all technologies, due to the order of magnitude improvement in channel resistivity. The insertion loss is limited by the effective device width, channel resistivity, and parasitic coupling to the heater and heater contact pads (which can be leakage paths in a grounded configuration). The isolation is limited by the parasitic capacitances to the pads and the heater, where the parasitic coupling to the heater

contact pads (not the heater itself) is the main contributor to the C_{off} and isolation limitation [52], [54]. The integration of phase-change switches into a legitimate RF circuit conclusively demonstrates the extracted DC device parameters translate into significant RF performance gains.



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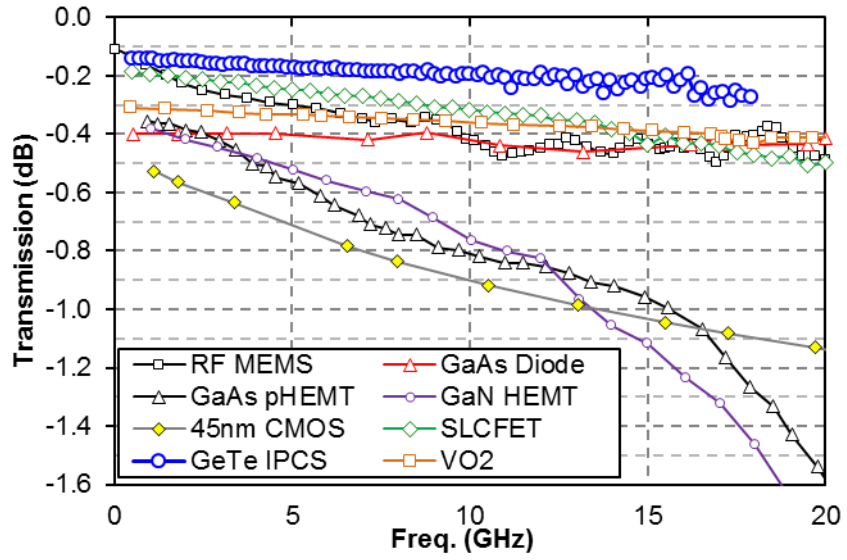

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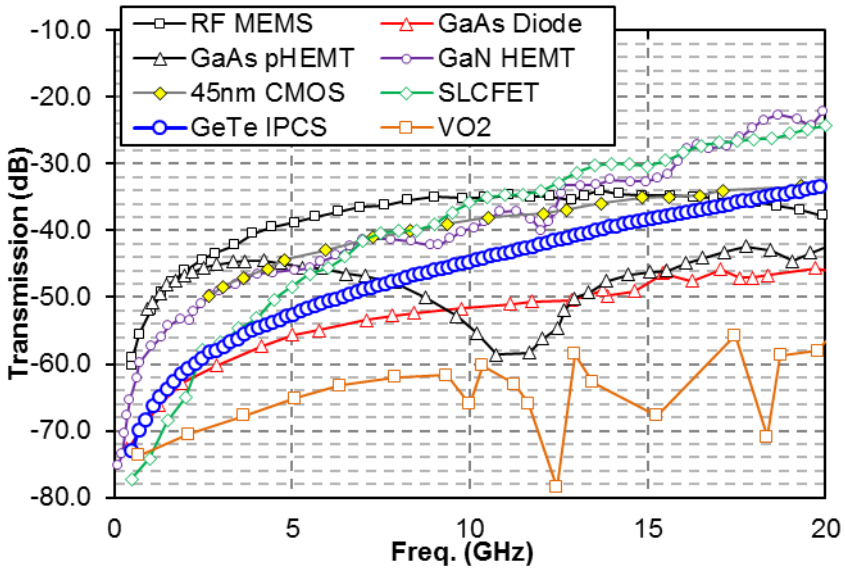


c)

Figure 3.11 a) schematic circuit dia- gram of the SPDT RF switch and an optical photograph of the SPDT realized in micro-strip b) measured insertion loss (ON-state transmission) and c) isolation (OFF-state transmission) for the fabricated SPDT switch, with comparisons to other technologies [12], [13]

3.5 Conclusion

A four-terminal inline GeTe RF switch has been fabricated with an integrated, independent resistive heater. The switch demonstrated a 0.08 Ω·mm R_{on} with an F_{co} of 1.0 THz and with zero prime power consumption during steady-state operation. To the best of our knowledge, this is the first time an electrically isolated heater has been used to successfully actuate both states of an inline, phase-change switch. Improvements to the CPW design resulted in a switch with a 0.036 Ω·mm R_{on} with an F_{co} of 7.3 THz. Utilization of traditional III-V MMIC process to incorporate microstrip designs decreased the R_{on} and C_{off} to 0.9 Ω (0.027 Ω·mm) and 14.1 fF, respectively. This results in an F_{co} of 12.5 THz for an SPST switch, which represents a 10x improvement over first generation IPCS devices. These devices have been integrated into an SPDT RF switch that measures less than 0.25dB insertion loss from 0-18GHz, and greater than 35dB of isolation across the same band, demonstrating the ability to fabricate non-volatile IPCS MMICs such as SPDTs, tunable filters, phase shifters, time delay units, and multi-port switch matrices.

4 Origin and Optimization of RF Power Handling Limitations in Inline Phase-Change Switches

4.1 Abstract

The power handling capabilities of inline phase-change switches (IPCS's) at radio frequencies (RF) has been correlated to the DC threshold voltage (V_{th}) of the devices. The dependence of V_{th} on microheater pulsing parameters and device layout has been characterized, accompanied by observation of the size of the amorphous chalcogenide region through scanning transmission electron microscopy (STEM). All observations are consistent with threshold field (F_{th}) of nominally 50:50 GeTe of 12.6 V/μm. Use of W-based microheaters in the IPCS processes has improved device performance and reliability, with increases in the product of cutoff-frequency (F_{co}) and V_{th} over previous IPCS devices using NiCrSi microheaters. The improved devices demonstrated power handling capabilities up to 29 dBm in a 50 Ω system for a switch with submicron dimensions, where the improvement is attributed to the larger amorphous zone created at the minimum power to amorphize. These improved devices demonstrate the feasibility of these switches in both transmit and receive wireless applications. A correlation between the peak allowed RF voltage across the OFF-state switch and the DC V_{th} of the OFF device was observed, indicating the DC V_{th} is an accurate predictor of RF power handling.

4.2 Introduction

Chalcogenide materials have been researched since the 1960's [26], due to the significant difference in optical and electrical properties of the material when in the amorphous or crystalline states. Optical memory systems exploit the state-dependent reflectivity to store data bits, whereas more recent phase-change storage class memories utilize the state-dependent

electrical resistivity [27], [31], [56]. Recently, chalcogenide materials have also been implemented in high-performance radio-frequency (RF) switches [40], [51], [54], [57], [58]. These inline phase-change switches (IPCS) have demonstrated a 10x improvement in the cut-off frequency (F_{co}=1/[2π·R_{on}·C_{off}]) when compared to conventional field-effect transistors (FETs) [2], [12], a 3x improvement when compared to MEMS switches [7], [12], and show promise for 5G and high frequency applications [37], [38], [44], [47]. They have also been heterogeneously integrated with commercial SiGe BiCMOS ICs to create reconfigurable front end modules up to 18 GHz, and show potential to be monolithically integrated in a variety of semiconductor processes [43]. IPCS devices are even viable for cryogenic applications (measured to 10K) [59].

Standard evaluation of any RF switch technology focuses on the frequency dependent transmission of an RF signal when the switch is in the ON- or OFF-state, and uses the F_{co} as the figure-of-merit (FOM) [2]. However, RF systems like cell phones, radar, and communication links typically have other important specifications for RF switches that are not addressed by the F_{co} as the sole FOM. Other properties such as (i) the maximum RF power handling ($P_{\mathrm{RF,max}}$, defined as the maximum continuous-wave RF power level which either inadvertently changes the switch state or catastrophically destroys the switch) (ii) the linearity of the switch as extracted by the output third-order intercept (OTOI), and (iii) switching speed directly affect the application space of any RF switch technology. Extremely high ON-state $P_{\mathrm{RF,max}}$ ($P_{\mathrm{RF,max,ON}}$) and OTOI (35 dBm [51] and 72 dBm [12], respectively) have been analyzed in [60]. The switching speed has also been characterized in [47], demonstrating 10-90% switching/settling times of 2 µs.

For the IPCS devices reported in [12] and [13], the $P_{\mathrm{RF,max,ON}}$ as limited by the current-carrying capacity of the switch in the ON-state was usually larger than the OFF-state $P_{\mathrm{RF,max}}$ ($P_{\mathrm{RF,max,OFF}}$), the power level as limited by the voltage that the switch could be exposed to in the

OFF-state. This ratio can be as much as 17 dB in some cases, with $P_{RF,max,OFF}$ as low as 18 dBm. This presents a problem in multi-port or multi-throw switching circuits that require both the ON- and OFF-state switches, as the OFF-state switches become the limiting factor for the $P_{RF,max}$ of the circuit. While a series and parallel matrix combination multiple switches is a design option to increase $P_{RF,max}$ without degrading the RF performance, this solution requires an increase in actuation power, as multiple switches are now needed for the same arm of the circuit. Consequently, it is important to understand and ultimately increase the $P_{RF,max,OFF}$ capabilities of a single switch in order to simplify designs, reduce switch power consumption, and widen the application space of the technology.

Threshold switching in amorphous chalcogenides (specifically $Ge_2Sb_2Te_5$) has been examined in vertical, via-style architectures for DC digital memory applications [27], [31], [33], [34], [56], [61], [62]. Based on this work, we hypothesize the $P_{RF,max,OFF}$ limitation of IPCS devices lies in the electric field-induced threshold switching caused by the transient voltage that appears across the switch on the transmission line. However, the threshold field (F_{th}) and threshold voltage (V_{th}) of nominally 50:50 GeTe that has been indirectly amorphized with an integrated microheater has not been well-characterized. It is also not clear exactly how the DC V_{th} relates to $P_{RF,max,OFF}$ due to the crystallization speeds and inherent time varying fields at GHz frequencies. Furthermore, the relationship between V_{th}, $P_{RF,max,OFF}$, and RF performance (F_{co}), and what design trade-offs may exist among these three parameters, requires elucidation. This work identifies the connection between GeTe structural characteristics, device pulsing conditions, V_{th}, achievable $P_{RF,max,OFF}$, and RF performance, thereby establishing the ability to reason about key tradeoffs in the IPCS technology.

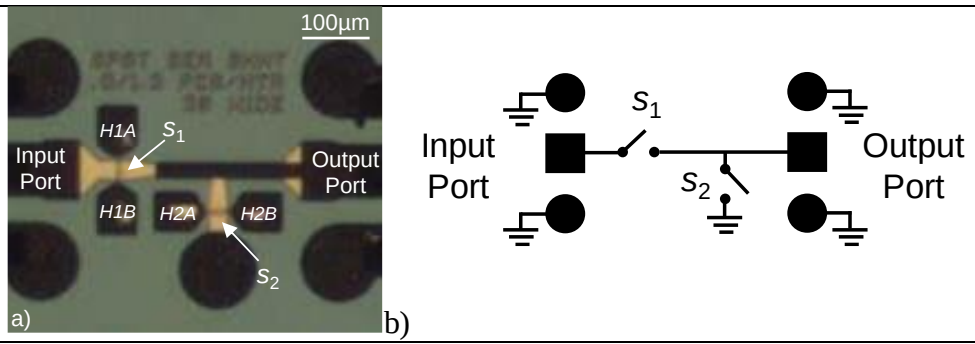
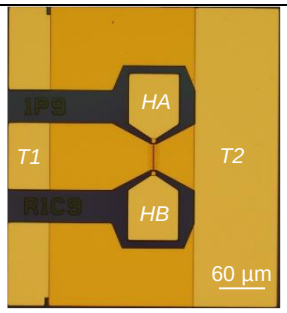


Figure 4.1 (a) Optical photo of the microstrip SPST tested (b) circuit schematic of SPST in (a)

4.3 Initial Observation of Power Handling Limitations

Using the fabrication process described in [13] (referred to as the Gen1 process), multiple types of circuits were fabricated, including the single-pole double throw (SPDT) switch reported in [13]. While attempting to characterize the linearity of the series-shunt, single-pole single throw (SPST) switch circuit in Figure 4.1(a) using the extracted TOI method described in [63], the shunt-to-ground switch (labeled s_2 on Figure 4.1(a) and Figure 4.1(b)) was observed to inadvertently convert from the OFF-state to the ON-state when a large enough power amplitude (18 dBm) was applied to the input port, resulting in a sudden decrease in output power. The switching of s_2 was not catastrophic, and the device could be switched back OFF for additional/repeated measurements using the microheater terminals (*H2A* and *H2B* in Figure 4.1(a)). To characterize this behavior more fully, DC I-V measurements across the GeTe terminals for 1-port SPST switches with layout dimensions identical to s_2 (Figure 4.2(a)) were done for switches in the OFF-state. Figure 4.2(b) shows the results of five repeated OFF-state I-V measurements on the same switch, performed at room temperature. The DC voltage was ramped across the GeTe terminals (*T1* and *T2* in Figure 4.2(a)) while monitoring the current in a test described fully in section IIIA. The DC breakdown event (reversible) observed between 1.75 V and 2.5 V was attributed to the V_{th} of the chalcogenide, extensively studied and reported on for



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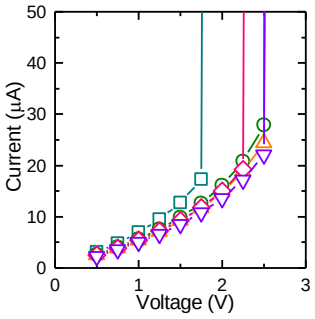

b)

Figure 4.2 a) Optical photo showing the 1-port IPCS breakout SPST and (b) repeated V_{th} measurements on the breakout SPST pictured in (a)

storage class memories [61], [64]–[66]. While not depicted in Figure 4.2(b), reversing the terminals for the voltage sweep (or ramping a negative voltage) results in a similar (with opposite polarity) distribution of the V_{th}.

It was hypothesized that larger V_{th} in a single device should result in larger $P_{RF,max,OFF}$ for the overall circuit, but it was not clear what controlled the value of V_{th}. Thus, V_{th} was characterized as a function of pulse parameters and device layout (discussed next in Sec III). This permitted an assessment of interactions and the development of understanding of the tradeoff between F_{co} and V_{th} in these devices.

4.4 Threshold Voltage Characterization

To simplify the measurements and increase the ability to do repeated measurements on single devices, devices were fabricated using the same process as [13] with two changes to layer thicknesses: the α-Si_xN_y (hereafter "SiN") barrier dielectric was reduced from 60 nm to 30 nm, and the GeTe was reduced from 135 nm to 75 nm. We will refer to these devices as Gen 1A, since they represent a small change to the structure of the Gen1 devices. Two studies were done on these Gen1A devices, each discussed in a separate section below. The first study focused on analyzing the V_{th} and OFF-resistance (R_{off}) of a single device (no variation in device dimensions) while varying the pulse power and pulse width, while the second study focused on analyzing V_{th} as a function of layout geometries, i.e. critical switch dimensions. First, some details are provided about the experimental method.

4.4.1 Pulsing and V_{th} Test Set-Up

A cross-section and plan-view schematic is provided for reference in Figure 4.3(a) and Figure 4.3(b). The device (referred to as device 1A) has a 1.3 µm switch length (L_{pcm}), 0.9 µm microheater width (W_h), and 10 µm switch width (W_{pcm}), where "length" is defined as being parallel to current flow and "width" as being perpedicular to current flow [40].

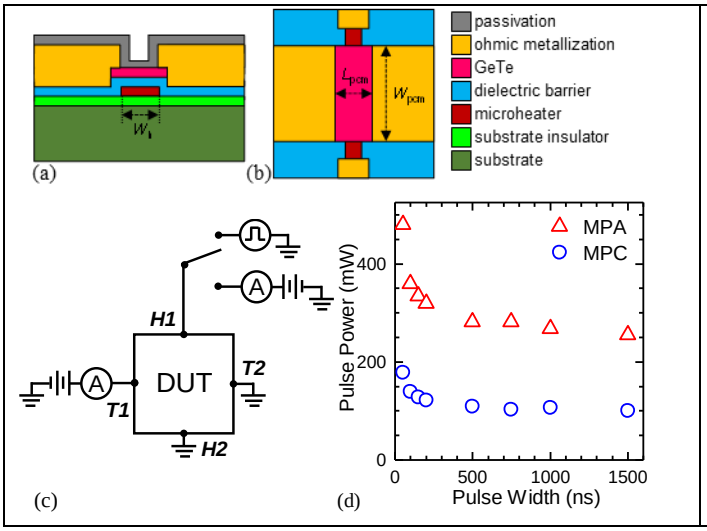

Figure 4.3 (a) Schematic cross-section of Gen1 IPCS process (b) plan-view schematic of Gen1 IPCS process (c) schematic of the V_{th} test setup (d) amorphization and crystallization curves for device 1A

A complete thermal analysis of the Gen1 process (including thermal models and simulations) is given in [29].

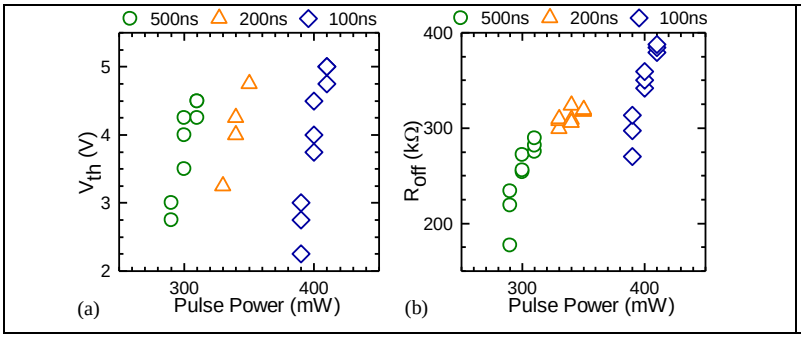

Figure 4.4 (a) V_{th} and (b) R_{off} measurements on device 1A as a function of pulse power, grouped by pulse width

4.4.2 Pulse Power and Pulse Width Analysis

Using the test setup described above, repeated V_{th} and R_{off} measurements were made on device 1A, which had an R_{on} of 5.5 Ω (2.8 THz F_{co}) and a microheater resistance of 487 Ω. Nine different types of pulses were used, chosen from a matrix of three different pulse powers (PP) and three different pulse widths (PW). The three different PPs were MPA, MPA+3.5%, and

MPA+7%, while the three different PWs were 500ns, 200ns, and 100ns. For each PP/PW combination, V_{th} and R_{off} were measured three times, and after each measurement the device was both cycled twice and then reset to the OFF-state for the next measurement using the specific PP/PW combination being evaluated.

Figure 4.4(a) and Figure 4.4(b) show the results of the V_{th} and R_{off} for each pulsing combination. It is observed that both the V_{th} and R_{off} increase with increasing pulse power for each pulse width, although similar V_{th} can be achieved for vastly different R_{off} using different pulsing combinations. Previous analysis on threshold switching for directly heated memory switches (primarily using $Ge_2Sb_2Te_5$), concluded the bulk, field-driven threshold switching was linearly dependent on the size of the amorphous region [33], [34], [56], [67]. Combined with previous reports of threshold switching in GeTe [36], [68], this suggests the V_{th} in IPCS devices is determined by the F_{th} of amorphous $Ge_{50}Te_{50}$ and length of amorphous region (L_α) that is created in the device channel, according to $V_{th} = F_{th} \cdot L_\alpha$. The linear relationship between V_{th} and pulse power (at a constant pulse width) then suggests the increase in V_{th} with pulse power results

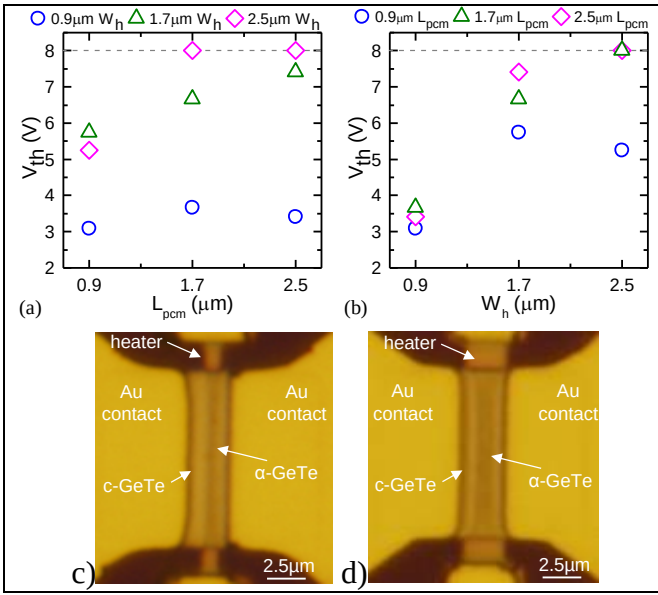

Figure 4.5 (a) Plot of V_{th} vs. L_{pcm} grouped by W_h (b) plot of V_{th} vs. W_h grouped by L_{pcm} (c) optical photo of a device with a 0.9µm microheater (d) optical photo of a device with a 2.5µm microheater. The dark stripe in the center of each device is the amorphous region created by pulsing the microheater

from melt/quenching a wider amorphous region in the channel. If this were the case, the wider amorphous region (and larger V_{th}) could be observed by testing devices with wider microheaters (i.e. larger W_h), under the assumption that wider heater produce wider amorphous regions [50]. One caveat in this strategy that the ohmic contacts to the GeTe acting as a thermal ground/heat sink. Thus, the GeTe directly underneath and slightly inside the ohmic contacts can never reach melting temperature [50]. Therefore layouts with both larger L_{pcm} and W_h were analyzed in order to further elucidate the connection between V_{th} and device design.

4.4.3 Layout Analysis

In order to further characterize the amorphous fraction of the OFF-state and V_{th}, and also determine the F_{th} of the GeTe, different layout geometries were analyzed. A matrix of nine devices was tested, having L_{pcm} and W_h values of 0.9 µm, 1.7µm, and 2.5 µm, all with a W_{pcm} of 10 µm. All dimensions were verified on wafer. The MPA for each device was experimentally determined, then pulsed OFF using the MPA+ 3.5% pulse power and 100 ns pulse width, then tested for V_{th}. Three repeated measurements were made on each device, similar to the methodology used in section IIIB. Figure 4.5(a) and Figure 4.5(b) show the average results of the repeated V_{th} measurements for the 9 different device layouts. Figure 4.5(a) shows the V_{th} vs. L_{pcm}, grouped by W_h, while Figure 4.5(b) reconfigures the data to plot V_{th} vs. W_h, grouped by L_{pcm}. It is observed that V_{th} generally increases with both the L_{pcm} and W_h, further suggesting that V_{th} is dominated by the amount of amorphous material created between the two ohmic contacts. Unfortunately, increased V_{th} with L_{pcm} and W_h comes at cost of RF performance due to the increase in R_{on} with L_{pcm} and an increase in C_{off} with W_h [12], exposing a fundamental trade-off between F_{co} and V_{th}.

Optical pictures of two different devices pulsed OFF with an L_{pcm} of 2.5 µm are shown in

Figure 4.5(c) and (d), differing only in the size of the microheater. The device in Figure 4.5(c) has a W_h of 0.9 µm, while the device in Figure 4.5(d) has a W_h of 2.5 µm. The dark stripe in the center of each device is the amorphous GeTe created through pulsing the microheater. It is observed that the length of the amorphous region (L_α) is larger for the 2.5 µm-microheater device when compared to the 0.9 µm-microheater device. While interesting to note, measurements of the L_α from the optical pictures can't provide insight into the F_{th} of the GeTe due to the 8 V limit placed on the V_{th} measurement. Hence, the dependence of L_α on pulse power, which will ultimately be used to determine the F_{th}, was investigated through cross-sectional STEM analysis.

4.5 STEM Analysis of Amorphous Region

Experimental details on the device samples, pulsing history, preparation and STEM equipment can be seen in [69], where devices with identical L_{pcm} and W_h to device 1A from the same wafer were pulsed with two different powers and analyzed in a STEM. Figure 4.6(a) shows a dark-field STEM cross-section of a virgin/untested device. Figure 4.6(b) shows a bright-field STEM image of a device pulsed OFF at MPA, specifically focused on the channel region. The red dashed lines indicate the border between the polycrystalline (ON) regions and amorphous (OFF) regions, as verified through nanobeam diffraction analysis. Significant structural changes (recrystallization, strain) are induced in the microheater (due to the temperature and current density) as evidenced by the striking contrast in the NiCrSi layer. Figure 4.6(c) shows a higher

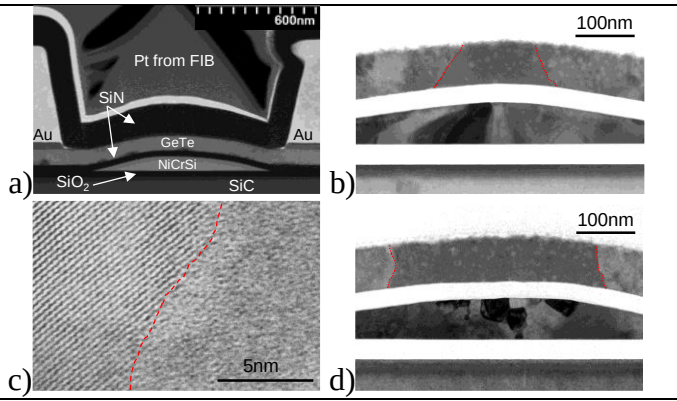

Figure 4.6 (a) Dark field STEM image of a virgin device (b) high-magnification bright field STEM image of the amorphous region for the device pulsed OFF at MPA (c) higher magnification bright field STEM image of the polycrystalline/amorphous boundary (d) high-magnification bright field STEM image of the amorphous region for the device pulsed at 15% > MPA

magnification image of the crystalline/amorphous boundary, where the lattice fringes on the left side of the image are indicative of crystalline GeTe, while the lack of lattice fringes on the right indicates significant disorder associated with amorphous GeTe. Figure 4.6(d) shows an image at the same magnification as Figure 4.6(b), for a device where the OFF pulse power was MPA+15%. The red dashed lines again indicate the border between the polycrystalline and amorphous regions. Large crystal grains are observed in the NiCrSi microheater, and based on nanobeam diffraction this crystalline NiCrSi does not extend outside the central region of the microheater. This can be explained by the measured negative TCR of the $Ni_{47.5}Cr_{47.5}Si_5$ thin film used in the microheater (measured on wafer to be -31 ppm/°C between 20-520 °C and -98 ppm/°C between 520-996 °C, and previously characterized in [70]), where hot spots in the heater reduce the local resistance, thereby drawing more current and driving further heating. This is also consistent with top center of the microheater being the hottest point in the system during the pulse [50]. It is clear from comparing Figure 4.6(b) and (d) that the higher pulse power has created a larger amorphous region in the center of the device. Measurements of the top and bottom of the amorphous region ($L_{\alpha\text{-TOP}}$ and $L_{\alpha\text{-BOT}}$, respectively) in Figure 4.6(b) and (d) are listed in Figure 4.7.

SUMMARY OF ELECTRICAL AND STEM MEASUREMENTS

(W) PP	(ns) PW	(V) V_{th}	(nm) $L_{\alpha\text{-TOP}}$	(nm) $L_{\alpha\text{-BOT}}$	(V/μm) $F_{th\text{-MIN}}$	(V/μm) $F_{th\text{-MAX}}$
0.91	100	2.42	148	210	11.52	16.35
1.05	100	5.15	354	375	13.73	14.55

Figure 4.7 Summary of electrical and STEM measurements

In order to extract the F_{th} of amorphized GeTe by correlating the STEM-measured L_{α} to the V_{th} (and preserve the devices for STEM imaging), V_{th} measurements were not done on STEM-analyzed devices, but instead on devices from the same wafer, one reticle away. Device parameters such as R_{on}, R_{off}, C_{off}, V_{th}, etc. typically vary <5% from device to device with a given process, layout, wafer, and pulse history. On devices having a layout identical to those analyzed

with STEM, repeated V_{th} measurements were made on two different devices (one pulsed at MPA, one pulsed at MPA+15%, identical to the methodology in [69]). The results are shown in Figure 4.7, where minimum and maximum critical threshold fields ($F_{th\text{-}MIN}$ and $F_{th\text{-}MAX}$) are calculated by dividing the average V_{th} by the $L_{\alpha\text{-}TOP}$ and $L_{\alpha\text{-}BOT}$, respectively. Averaging the $F_{th\text{-}MIN}$ values results in an F_{th} of 12.6 V/µm. This compares well to previous reports of as-deposited amorphous GeTe (23 V/µm [30], also nominally 50:50), and is of the same order as other chalcogenides such as $Ge_{15}Sb_{85}$ (9 V/µm [71]), $Ge_2Sb_2Te_5$ (56 V/µm [71]), and $Ag_7In_{11}Sb_{48}Te_{34}$ (19 V/µm [71]).

Combining the results from this section and section 4.4, it is clear that in order to increase V_{th} in IPCS devices using GeTe (and potentially increase $P_{RF,max,OFF}$), a larger amorphous region needs to be created in the device channel. For devices made in the Gen1 process, this can be done by increasing the microheater width at the expense of RF performance, or by increasing the pulse power, as seen in Figure 4.5 and Figure 4.7. Unfortunately, the NiCrSi microheaters have two significant drawbacks: (1) the negative TCR decreases the effective thermal width of the microheater, resulting in a smaller melt region for the same electrical width, and (2) increasing the pulse power significantly reduces the lifetime of the NiCrSi heaters to an unacceptable level. This necessitates building IPCS devices with a more robust microheater material in order to improve both reliability and V_{th}.

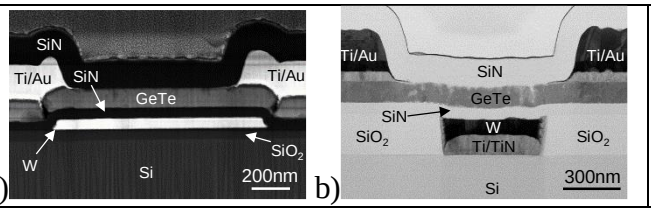

Figure 4.8 (a) Dark-field STEM image of a Gen2 device with an etched W microheater (b) Bright-field STEM image of a Gen3 device with a CMP-patterned Ti/TiN/W microheater

4.6 Material and Device Changes to Improve V_{th}

In order to fundamentally improve the V_{th} and reliability of IPCS devices without degrading the RF performance, tungsten (W) was introduced as a new material for the

microheater due to its high melting temperature and positive, linear TCR with temperature [72]. For the second-generation process (Gen2), a 50 nm thick W film was dry-etched to form the microheater, with a 60 nm SiN dielectric barrier and 110 nm GeTe layer (pictured in Figure 4.8(a) and described in Section 2.3.2). RF performance and switching speed characteristics have been reported in [47]. As can be seen from Figure 4.8(a), the GeTe layer forms cracks at the edge of the W microheater. These were found to be stress cracks formed over the step height of the microheater, due to the non-heated GeTe sputter deposition and subsequent ex-situ post-deposition crystallization anneal (conversion from α-GeTe to c-GeTe). While both the reliability and V_{th} of the Gen2 devices was significantly improved compared to Gen1 devices [60], the cracking of the GeTe necessitated a W_h larger than the L_{pcm} in order to have continuous GeTe between the ohmic contacts. This inherently increased the C_{off} of the devices, and limited the highest performing devices to only 6 THz [47] .

In order to improve the RF performance while maintaining the improved reliability V_{th}, a third-generation process was developed (Gen3) with a planar microheater architecture (described in Section 2.3.3). Figure 4.8(b) shows the baseline Gen3 device, where a Ti/TiN/W microheater is now formed in an oxide trench using a damascene process. The W_h can now be reduced to 0.5 µm, the lithographic limit of the stepper used in this work, while maintaining the same L_{pcm}. The ON- and OFF-state transmission of this device implemented in a series coplanar waveguide (CPW) SPST circuit is shown in Figure 4.9(a), measured from 0-65 GHz (thru-line subtracted for insertion loss data). The insertion loss measured less than 0.13 dB across the entire band. The extracted parameters of the SPST are shown in Figure 4.9(b) (limited to 20 GHz), resulting in a nominal R_{on}, C_{off}, and F_{co} of 1.22 Ω, 12.31 fF, and 10.6 THz, respectively. The reliability and RF performance of an SPDT up to 30,000 cycles is shown in [47]. The reliability of a single switch

in this process up to 100,000 cycles (200,000 pulses) is pictured in Figure 4.10. The device was still fully functional at the end of the test, which was terminated due to test stand availability. As with the other measurements reported for IPCS devices, the pads are *not* de-embedded for this measurement, and the data represents the IPCS device with the entire CPW structure.

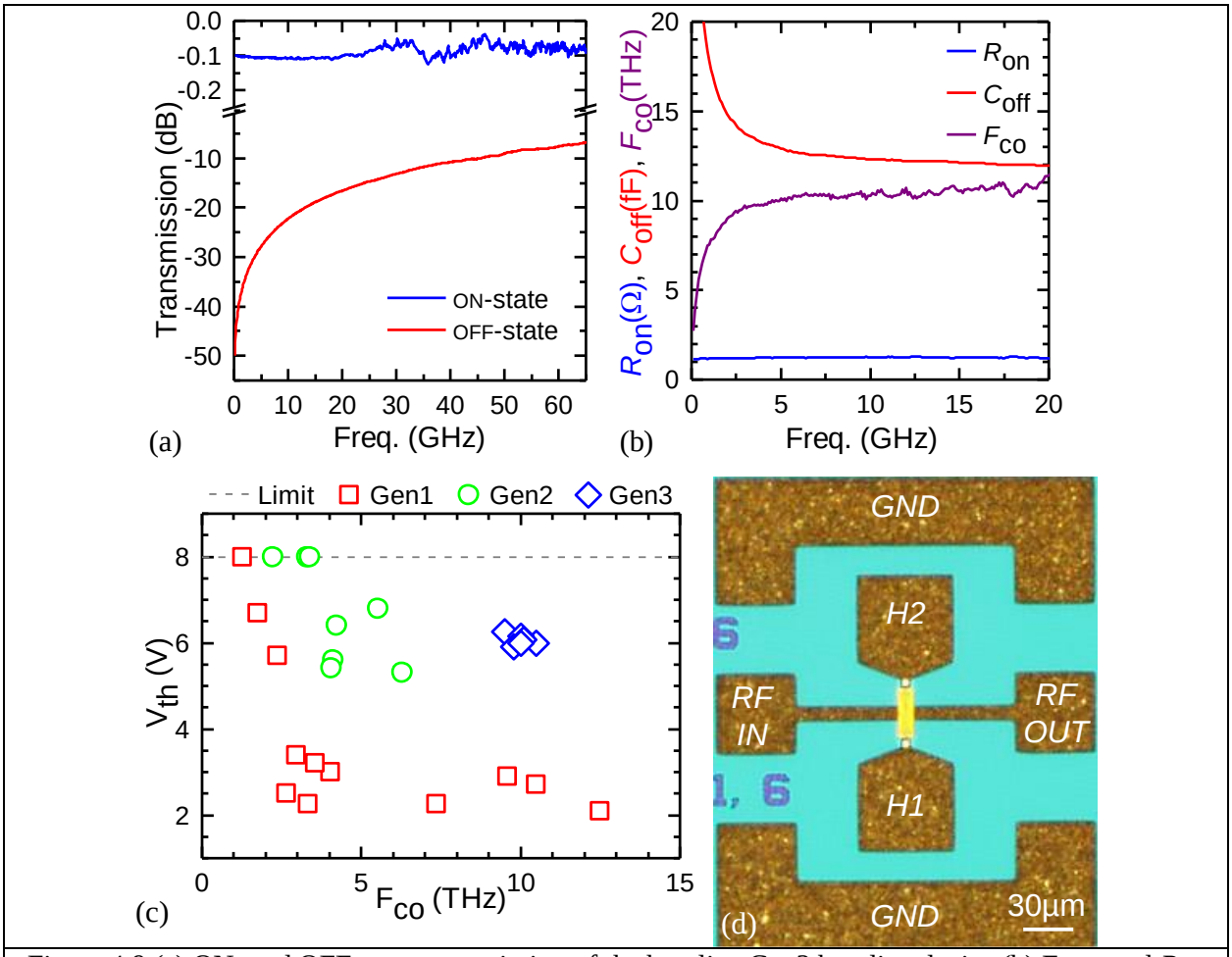

Figure 4.9 (a) ON- and OFF-state transmission of the baseline Gen3 baseline device (b) Extracted R_{on}, C_{off}, and F_{co} of the baseline Gen3 baseline device (c) plot comparing the V_{th} vs. the F_{co} for all three process generations (d) optical photo of the series SPST used for the RF data shown in (a)-(c)

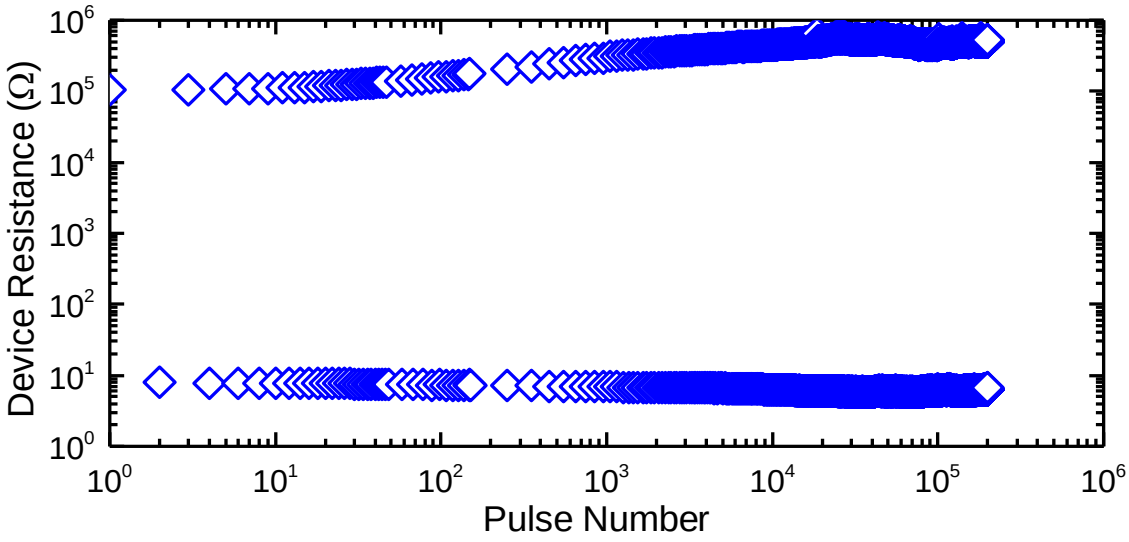

Figure 4.10 Device resistance vs. pulse number for a 10 µm wide switch made in the Gen3 process up to 200,000 pulses. The device was fully functional at the conclusion of the cycling test, highlighting the need for more advanced testing procedures to decrease the test time to observe device failure

The SPST is measured with the heater actuation probes physically disconnected from the pulse generator in order to obtain accurate measurements of the R_{on} and C_{off} [12], [47]. Figure 4.9(c) shows a plot of the V_{th} vs. F_{co} for all three process generations of IPCS devices. A clear trade-off between F_{co} and V_{th} is observed, and a clear improvement in V_{th} is seen in all devices using a tungsten microheater. The fabricated series-SPST measured in Figure 4.9(a)-(c) is pictured in Figure 4.9(d), and a summary of the different process generations is given in Figure 4.11.

SUMMARY OF IPCS PROCESS GENERATIONS

PROCESS	HEATER MATERIAL	HEATER FORMATION	SIN BARRIER	GETE
Gen1	NiCrSi	Lift-Off	60 nm	135 nm
Gen1A	NiCrSi	Lift-Off	30 nm	75 nm
Gen2	W	Etch	60 nm	110 nm
Gen3	Ti/TiN/W	CMP	60 nm	110 nm

Figure 4.11 summary of IPCS process generations

4.7 Correlating RF Power Handling to V_{th}

Having characterized the V_{th} of IPCS devices and incorporated W microheaters in a reproducible and reliable process, it is now possible to examine the relationship between V_{th} and

$P_{RF,max,OFF}$. Switches fabricated using the Gen3 process were fabricated on 6", >10 kΩ-cm Si wafers with a nominal L_{pcm} of 0.9 µm, W_{pcm} of 10 µm, and W_h of either 0.5 µm or 0.7 µm. Nine 2-port shunt SPST switches (inset of Figure 4.12(a)) were set to the OFF-state with varied V_{th} between 1-7.25 V. A power handling test was then performed as described in Section 2.4.2.4. The measured $P_{RF,max,OFF}$ for each switch is plotted against the corresponding measured V_{th} in Figure 4.12(a). There is a good correlation between the measured V_{th} and the measured $P_{RF,max,OFF}$, indicating at these RF frequencies that V_{th} is a good predictor of $P_{RF,max,OFF}$ for IPCS devices.

To understand this correlation more deeply, we express this maximum RF power, $P_{RF,max,OFF}$, as a breakdown voltage, $V_{br,RF}$. This is meaningful because the switch does not carry $P_{RF,max,OFF}$, through it in the OFF-state shunt configuration. Rather, the switch is exposed to the

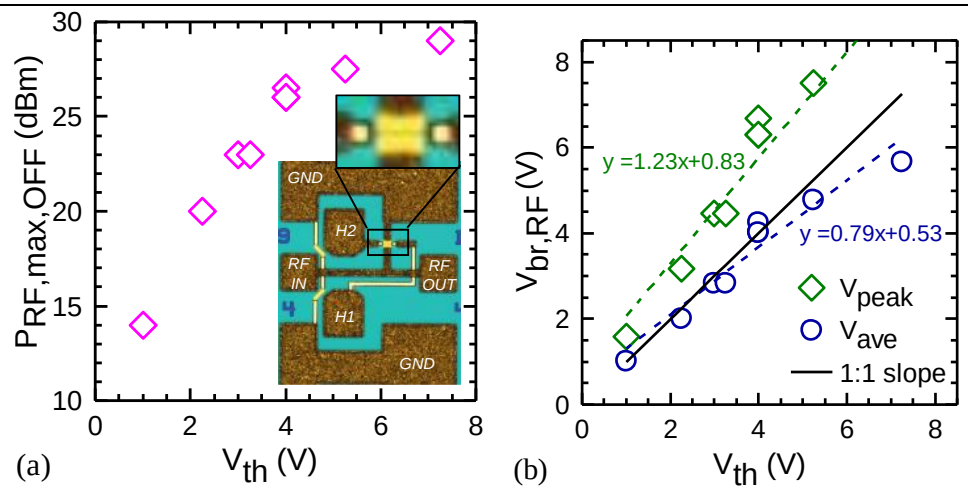

Figure 4.12 (a) plot of measured $P_{RF,max,OFF}$ vs. measured V_{th} for the same device. The inset shows the shunt switch used for the measurements. (b) plot showing the correlation between $V_{br,RF}$ and V_{th}, where peak and averaged values of $V_{br,RF}$ are used to gain insight into the physical mechanism of threshold switching

same voltage as a 50 Ω load absorbing a time averaged power level of $P_{RF,max,OFF}$. Since the instantaneous voltage is time varying we examine the peak RF voltage ($V_{peak} = (1/2) \cdot \sqrt{8R_o P_{RF,max,OFF}}$) and the average RF voltage ($V_{ave} = (1/\pi) \cdot \sqrt{8R_o P_{RF,max,OFF}}$) of

the time varying RF waveform. Both are plotted versus the V_{th} in Figure 4.12(b).

Insight can be gained by examining the slope of these curves and comparing to a slope of unity (also shown in the figure). While the correlation is good (as expected form the power), neither of the slopes in unity, and this reveals aspects of the breakdown mechanism. The peak RF voltage is larger than the corresponding DC value of V_{th} (slope greater than unity). This is consistent with previous observations of time-dependence in the threshold event [30], [73], where V_{th} is dependent on the duration of the applied field. V_{ave}, on the other hand, is relevant if the breakdown event could accumulate over multiple RF cycles and could accumulate even as the voltage is switching sign. This might be appropriate in the case for breakdown events that are initiated by carrier accumulation effect, which has been suggested as a source of threshold switching in chalcogenides [74]. The extracted V_{ave} slope of 0.8 suggests a modest non-linearity where higher voltages count for more than lower ones in the averaging of the threshold event.

Ultimately, it remains an open question whether the breakdown occurs in a single RF cycle or as an average of multiple cycles. Unfortunately, due to the test setup and long duration (1 s) of each application of RF signal in this work, it is difficult to determine (i) when the threshold event occurred during the application of the RF signal (ii) if the threshold event occurs rapidly during a single RF signal half-cycle, or if it is dependent on the cumulative exposure to the electric field over many cycles of the RF signal, and (iii) how the threshold event depends on the RF signal frequency. While the IPCS device and OFF-state RF power handling tests may provide a new avenue for researching the temporal evolution of threshold switching in amorphous chalcogenides with rapidly changing fields, the limitations in the test setup prevent any conclusions on threshold switching mechanism based on this work.

The newly established $P_{RF,max,OFF}$-V_{th} relationship does provide valuable insight into the

design trade-space for IPCS devices. For example, a target $P_{RF,max,OFF}$ of 30 dBm (1 W) for a single device would dictate a V_{th} between 7-8 V. Using the extracted F_{th} of 12.6 V/µm, this would imply a minimum L_{α} between 540 nm and 615 nm. This number provides the primary constraint to balance L_{pcm} W_{pcm}, W_h, and material thicknesses for maximum RF performance at a given $P_{RF,max,OFF}$ requirement. It also allows further trades to be made in improving the RF performance for applications that don't have high voltage or power handling requirements. A second noteworthy result is the high $P_{RF,max,OFF}$ observed (29 dBm) in the test for devices using both an L_{pcm} and W_h less than 1 µm. This result represents a significant achievement in widening the application space of this technology, as now both receive and transmit applications can be considered with this high F_{co} and power handling capabilities.

4.8 Conclusion

V_{th} dependence on pulsing parameters and layout has been characterized, with the F_{th} of GeTe (12.6 V/µm) being extracted from direct STEM observation of the amorphous region. V_{th} and F_{co} improvements have been demonstrated by incorporating W microheaters. A fundamental trade-off between V_{th} and F_{co} has been observed in all 3 process generations. Devices built in the 3rd generation process show an R_{on}, C_{off}, and F_{co} of 1.22 Ω, 12.31 fF, and 10.6 THz, respectively. A series CPW SPST switch was built using these devices, and measured less than 0.13 dB insertion loss from 0-65 GHz. These switches show an average V_{th} of 6 V, which translates to a $P_{RF,max,OFF}$ of 28.5 dBm. Finally, a direct correlation between the maximum RF power handling capabilities and the DC V_{th} of IPCS devices has been established, with a maximum measured $P_{RF,max,OFF}$ of 29 dBm for devices with submicron layout dimensions.

5 Heterogeneous and Monolithic Integration of Inline Phase-Change Switches for Reconfigurable RF Systems

5.1 Abstract

Passive RF circuits have been built with inline phase-change switches to compare their frequency performance to state-of-the-art technologies, as well as to demonstrate fine-grain reconfigurability in RF circuits. Simulations of 8-port omni-directional IPCS switches used in a reconfigurable transceiver demonstrates less than 2dB degradation in gain and 1dB in noise figure when reconfiguring a single chip for 4 different receiver chain frequencies (S-band, X-band, Iridium, and CDL-Ku), demonstrating the feasibility of IPCS devices for low-power, broadband reconfigurable RF systems. Omni-directional GeTe inline phase-change switches were then fabricated and heterogeneously integrated with commercial SiGe BiCMOS technology to create a reconfigurable receiver. The reconfigurable receiver required integrating thirteen (13) 8-port and two (2) 4-port omni-directional switch circuits with a commercial SiGe IC, requiring very stable and repeatable performance from the 112 integrated GeTe IPCS devices. Insertion loss, isolation, and cycling data will be presented, as well as performance issues encountered during the heterogeneous integration process. A new monolithic integration scheme is then discussed that is independent of the substrate and semiconductor technology used. In order to experimentally demonstrate this concept, IPCS devices were fabricated on top of an AlN heat spreading layer deposited on a thick SiO_2 layer. The thick SiO_2 emulates the inter-layer dielectric (ILD) thermal properties that prevent direct integration of IPCS devices at the end of a back-end-of-line (BEOL) CMOS process. The AlN acts as a heat spreading layer, enabling the proper thermal quench rate despite the low thermal conductivity of the oxide underneath. Multiple AlN thicknesses were examined and shown to properly quench the device. Use of this heat spreading

layer experimentally demonstrates a substrate agnostic monolithic integration (SAMI) scheme, where IPCS devices can be integrated at the end of any microfabrication process—regardless of the substrate or materials underneath. This is attractive for many CMOS applications where wafer real estate is expensive, or in III-V applications where the wafer thermal properties are poor and vary among different technologies. This integration enables the monolithic fabrication of GeTe IPCS devices on any semiconductor technology, allowing low-loss, low-power, broadband reconfigurable RF systems and SoCs to be realized in any semiconductor or RF technology.

5.2 Introduction

Implementing any reconfigurable analog SoC requires a fabric of interconnect metallization layers and low-loss switches to fully take advantage of the reconfiguration, regardless of the technology in which it is implemented. With the IPCS device performance exceeding 12 THz and possessing potential for significant future performance gains, significant interest in their implementation for reconfigurable RF systems has developed [12], [43]–[45], [75]. Simulations of reconfigurable, passive RF circuits based on IPCS devices demonstrate significant system benefits when implemented in a frequency agile reconfigurable transceiver, opening the possibility for unique, low power, flexible RF systems based on this switch.

Complicating the issue for GeTe IPCS devices is that they are currently fabricated on separate chips that require micro-bumping (μ-bumping) to an active semiconductor chip that contains the active RF elements. Despite the impressive RF performance, the heterogeneous integration adds interconnect routing on both the base CMOS/SiGe/base chip and the IPCS chip which increases the overall loss of the system. The heterogeneous integration also adds considerable manufacturing complexity, as multiple IPCS chips need to be bonded to a single

base chip, which can significantly increase cost and cycle time, as opposed to a monolithic or wafer-level solution. Due to the low-cost nature and high compatibility of the IPCS process with standard CMOS/SiGe processes, a back-end-of-line (BEOL), substrate agnostic monolithic integration (SAMI) solution has been developed that allows the addition of IPCS devices to be implemented on the back-end of any semiconductor technology.

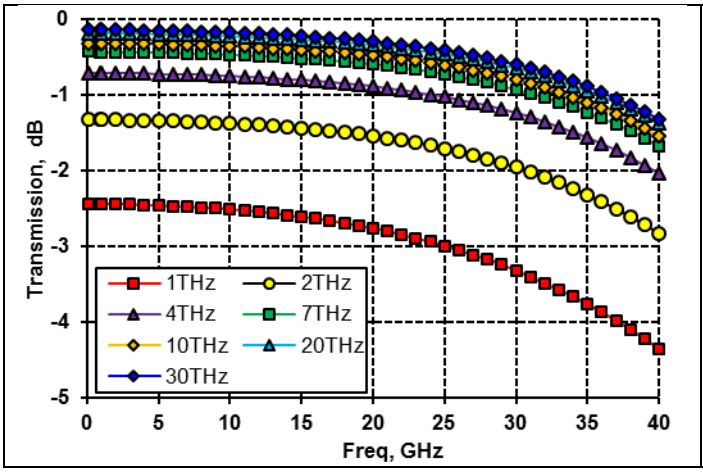

Figure 5.1 simulated transmission of an 8-port omnidirectional switch vs. frequency, for 7 different cutoff frequency switches. Constant OFF-capacitance was assumed for each cutoff frequency.

5.3 Simulations of IPCS-based Reconfigurable Systems

Using omni-directional switches provides the greatest flexibility for interconnecting components in a reconfigurable system [63]. However, building systems with omni-directional switches has not been practical because of the high losses associated with conventional solid-state switch technologies. These technologies are limited to switch cutoff frequencies of below 2 THz, which would result in a minimum loss of 1.5-2 dB for a single 8-port omnidirectional switch up to 20 GHz (Figure 5.1). Figure 5.1 shows the simulated insertion loss of an 8-port omnidirectional switch with a range of cutoff frequencies (all simulations done by Pavel Borodulin). The circuit model from Figure 2.10 is implanted in each of the 8 switches depicted in Figure 5.1. A constant capacitance of 10 fF is used for each F_{co} in the simulation, where the R_{ch} is adjusted to simulate the correct F_{co} to show the effect of the decreased F_{co} on the insertion loss. While coarse and not perfectly accurate to transfer to other switching technologies (due to

the intricacies of the circuit model for different switch technologies and the simplification of the F_{co} model), this simulation is useful in demonstrating the effect lower F_{co} switches have on higher throw count switching circuits. Reconfigurable system architectures utilizing 1-2 THz switches (as is currently SoA) are forced to use system-level reconfigurability in order to limit the system degradation due to switching losses. This system-level reconfigurability is shown in Figure 5.2(a), where four example systems are built as standalone entities and single-pole multi-throw switches are added to toggle between the different systems. This solution does not allow for the ability to share common components or to swap out a single failed component without having to swap out an entire system.

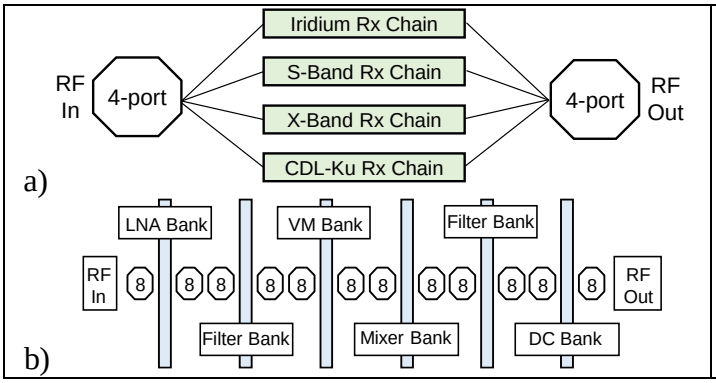

Figure 5.2 a) block diagram of a system-level reconfigurable architecture b) block diagram of a component-level reconfigurable receiver architecture. 8-port omnidirectional switches are inserted before and after each bank of components to allow for course-grain switching

A much greater degree of flexibility is afforded by the architecture shown in Figure 5.2(b). Here, omni-directional 8-port switches are inserted between sets of components that fall into a common category (i.e. LNAs, mixers, filters, etc.). Component banks can be created consisting of components that are different in terms of the operating frequency band, gain, power output, efficiency or TOI and chained together to dynamically restructure the system to some optimum for the particular situation or system need. The component banks can also contain duplicates to allow the system to heal itself in the event that a component breaks. For this type of component-level reconfigurability to be attainable, where 10-15 8-ports (and hence 100+ individual switches) would be needed in a single receive or transmit chain, high F_{co} switches

with zero or limited prime power consumption are required. Using the IPCS devices in an 8-port omnidirectional switch could reduce the loss by up to 2.4 dB per 8-port (Figure 5.1).

To demonstrate the ability to do component-level reconfiguration with a high performance switch, a reconfigurable transceiver was built utilizing inline phase-change switches. The transceiver architecture was designed by Pavel Borodulin, and the RF circuitry was designed by Ryan Walsh. The transceiver supports at least the four systems shown in Figure 5.2, namely an S-band radar (5 GHz), an Iridium uplink/downlink (1.6 GHz), an X-band radar (10 GHz) and a Ku-band common data link (CDL) (18 GHz). Figure 5.3 shows the performance analysis (gain, OTOI, and noise figure) of the reconfigurable transceiver as a function of generic switch performance for 4 different frequency bands and functions (analysis performed by Fred Kuss and Pavel Borodulin). Each system utilizes the component-level reconfiguration architecture shown in Figure 5.2(b), where twelve (12) 8-port switches are inserted in the chain to allow for component-level reconfiguration on a single board. This totals 24 ON-state and 72 OFF-state switches in a single chain (96 total individual switches). For the four particular systems shown in Figure 5.2, most of the system performance is recovered when using switches having cutoff frequencies of 30 THz or above (Figure 5.3). All four systems of interest degrade by less than 2 dB in gain and less than 1 dB in noise figure and OTOI when compared to a system using ideal lossless switches.

These system level simulations show that reconfigurable RF systems are possible with an RF switch that has high enough F_{co}. Inline phase-change switches certainly can meet this requirement, and have enough performance in their current state to create very unique and adaptable RF systems. In order to demonstrate a prototype reconfigurable RF system, 4 and 8

port omni-directional switch circuits were fabricated and heterogeneously integrated with a commercial SiGe BiCMOS chip (with the active RF circuitry).

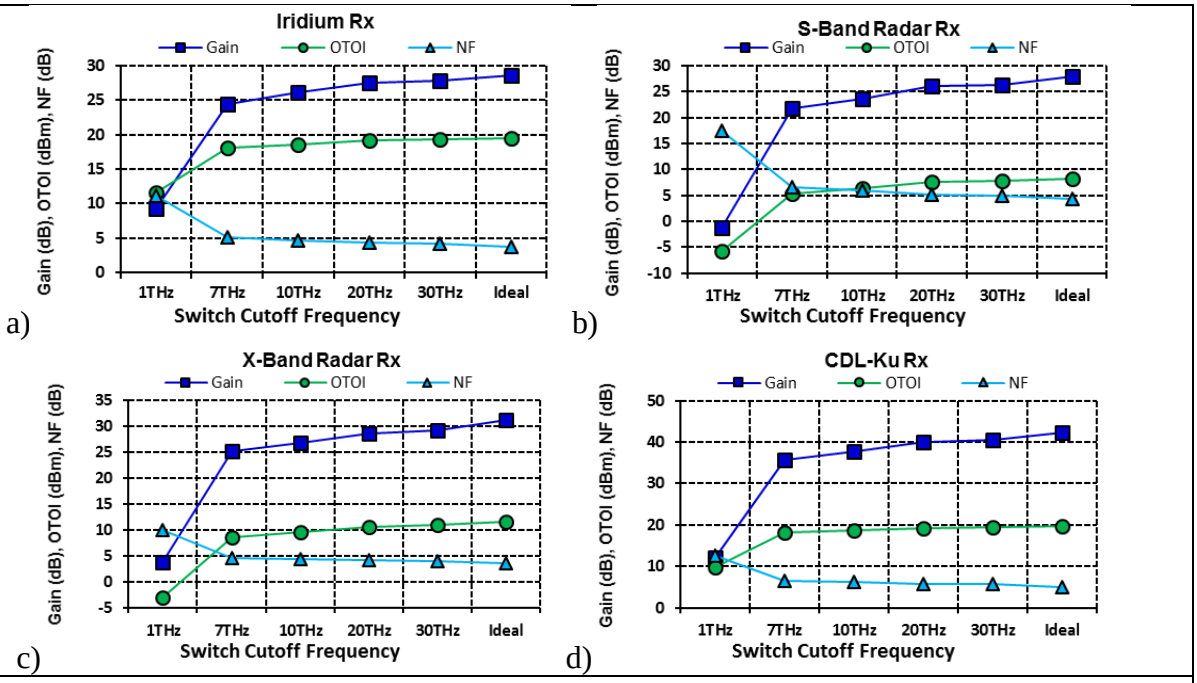

Figure 5.3 simulated receiver performance for a) Iridium receive chain b) S-band receive chain c) X-band receive chain d) CDL-Ku receive chain as a function of generic switch cutoff frequency

5.4 IPCS-Based Reconfigurable Transceiver

5.4.1 Fabrication and Heterogeneous Integration

Figure 5.4(a) shows a schematic cross-section cartoon of the integrated IPCS devices on the SiGe BiCMOS chip. A modified Gen2 process is used for these prototypes, where 50µm tall µ-bumps are plated at the end of the Gen2 process to allow for dense flip chip interconnections with the SiGe BiCMOS chip. Significant effort was taken to fabricate the µ-bumps uniformly, as there are 96 µ-bumps per 8-port omnidirectional switch and a single missing bond due to a non-uniform µ-bump could result in the entire system failing (and only a manual optical inspection can screen out questionable parts prior to bonding). The IPCS chip is then flipped and bonded to

the BiCMOS chip that has all the active circuitry (amplifiers, mixers, vector modulators, filters, etc.). The SiGe BiCMOS integrated circuit was fabricated in TowerJazz's SBC18H3 process to provide the high levels of circuit density and integration needed for the RF circuitry [76]. The FETs from the SiGe BiCMOS process are also used for the pulser circuitry required to individually actuate the IPCS devices, which took less than 7 V to be actuated once integrated. Figure 5.4(b)-(d) shows a SEM image of an 8-port omni-directional IPCS switch circuit. Figure 5.5 shows the port-to-port resistance of an 8-port circuit as the input switch is being toggled, up to 1,000 pulses (500 cycles).

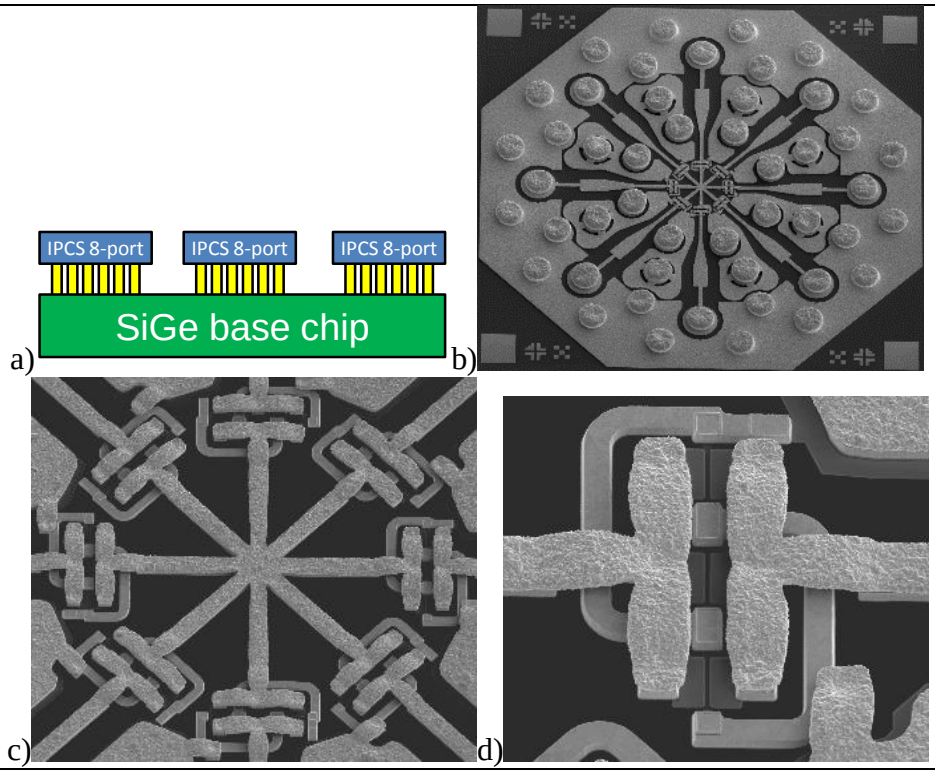

Figure 5.4 a) Schematic cross section of the IPCS chiplets bump-bonded to the base SiGe BiCMOS chip b) SEM image of the 8-port omni-directional IPCS circuit c) zoom in of the center region, showing the 8 IPCS devices d) zoom in of a single 3-finger IPCS device wired in parallel

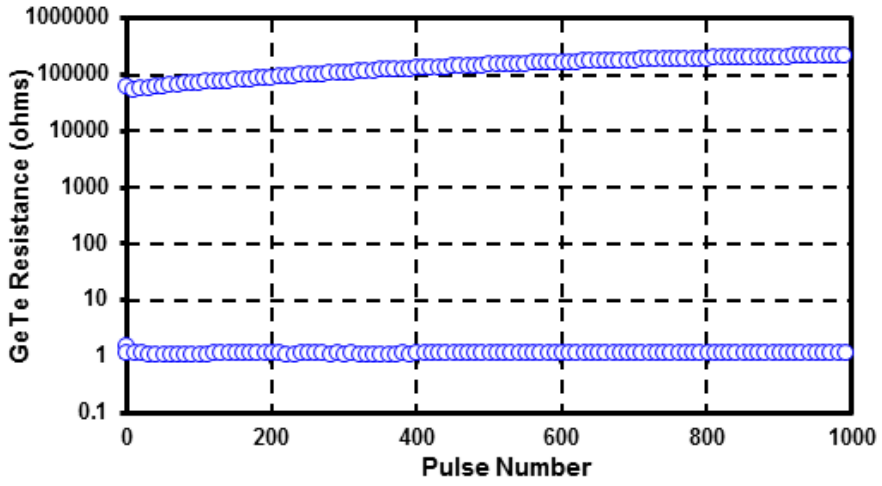

Figure 5.5 Cycling data of a single switch in the 8-port circuit. DC ON-resistance stabilized near 1.1 Ω after 4-5 cycles, which was maintained through the course of the cycling test. The test was terminated after 1000 pulses due to time constraints

5.4.2 Limitations of the Packaged Reconfigurable Transceiver

Three different IPCS-based reconfigurable receivers were fabricated through the 3D integration of SiGe BiCMOS chips with multiple IPCS chiplets. Figure 5.6(a) shows the SiGe BiCMOS chip mounted and wirebonded in a commercial QFN (quad flat no leads) package, with no IPCS 8-ports bonded to it, as a test vehicle. The first prototype used IPCS devices manufactured on low-resistivity Si and bonded to the base chip without being thinned, pictured in Figure 5.6(b) (in a QFN package with wirebonds). The IPCS chiplets are passive multi-port (4- or 8-way) omnidirectional RF switches. The particular prototype shown in Figure 5.6(b)-(d) is a reconfigurable receiver, containing 5 amplifiers, 2 IF down converters, 1 baseband down converter, 2 vector modulators and 7 band-pass filters with frequency coverage from 0.1 to 18GHz. The SiGe BiCMOS chip is 9 mm on a side, while the 4- and 8-port switch chiplets are 1.3 and 1.7mm, respectively. The second prototype used IPCS devices manufactured on high-resistivity Si and bonded to the base chip after being thinned (Figure 5.6(c)). The third prototype used IPCS devices manufactured on semi-insulating SiC and bonded to the base chip after being thinned (Figure 5.6(d)). The different prototypes had better performance with better RF quality

substrates, due to the number of switches and length of routing on each switch chiplet. Thirteen (13) 8- port and two (2) 4-port IPCS chiplets allow for a large number of arbitrary ways to configure the electrical paths between components in response to digital commands. Not including any active RF components, there are greater than 800 possible unique paths to connect the RF input to the RF output, while passing through a minimum of 4 switch chiplets or a maximum of 12. Two possible configurations that would result in a full receiver system (RF-to-baseband) are shown in Figure 5.7 (a) and (b) (figure and system schematic created and provided by Pavel Borodulin).

Basic functionality of the RF-FPGA chip pictured in Figure 5.6 has been demonstrated, such as the ability to toggle individual switches ON and OFF using commands supplied via the SiGe BiCMOS chip's digital logic circuits, and the successful configuration of different receiver systems (in the frequency domain) resulting in different gains. Unfortunately, there was too much loss associated with the receiver to produce gain out of the X and Ku band systems. The loss was found to be a combination of transmission line losses from the routing on the BiCMOS chip, very long transmission line paths due to non-optimal component placement (up to 61mm of transmission line runs in some cases), return/mismatch losses from the IPCS chiplets due to the large number of OFF-ports on each circuit, and transmission line losses on the IPCS circuits themselves due to substrate losses and ohmic losses of the μ-bumps.

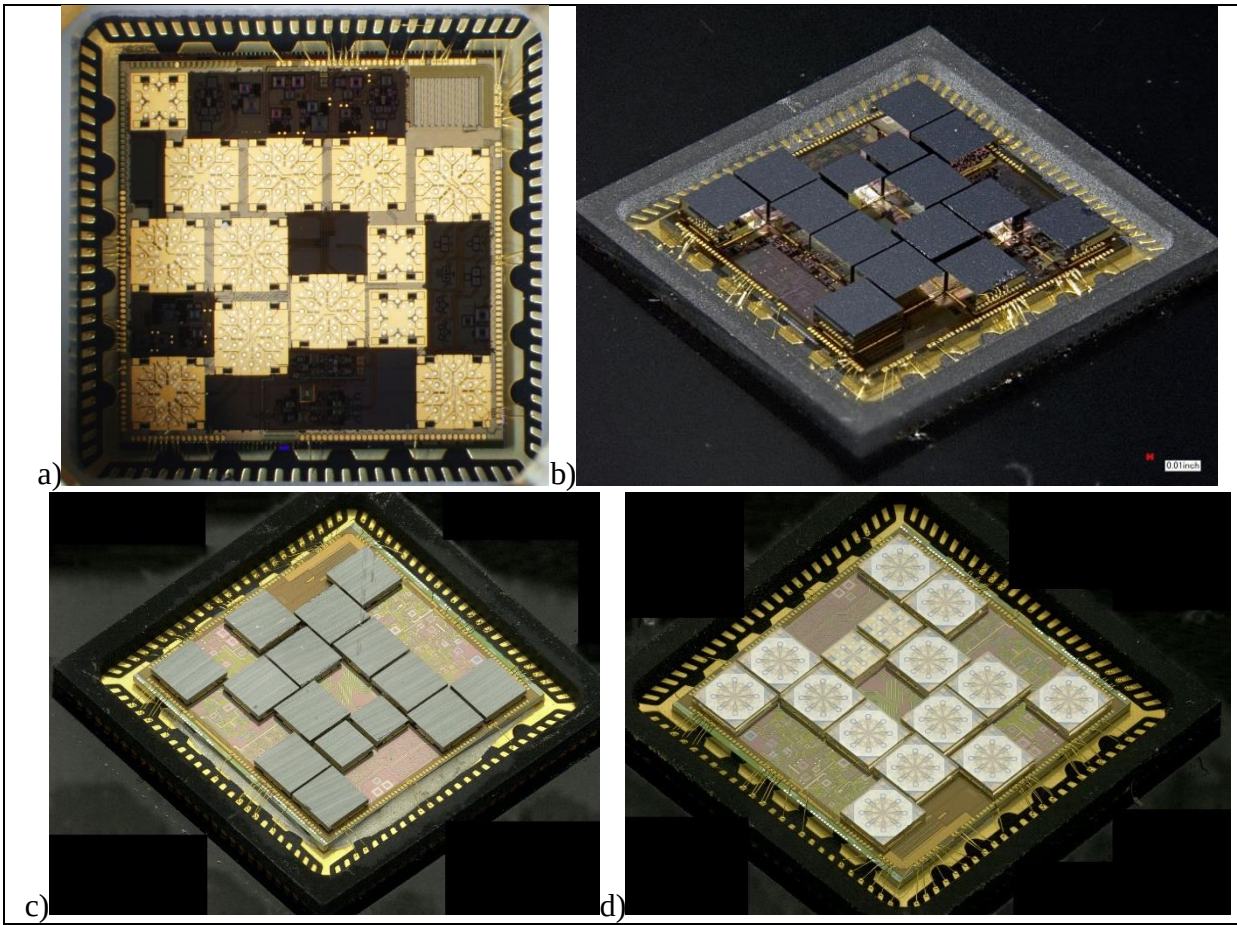

Figure 5.6 a) Stitched optical microscope image of the SiGe base chip mounted and wirebonded in a QFN with no IPCS chiplets (b) optical image of the first (unthinned lossy Si substrate) (c) the second (thinned higher-res Si substrate) and (d) the third (semi-insulating SiC substrates) fully reconfigurable receiver prototype, with the IPCS chiplets bonded to the SiGe BiCMOS chip, mounted and wirebonded in a QFN. The frontside circuits in (d) are optically visible through the backside due to the transparent nature of the semi-insulating SiC substrate

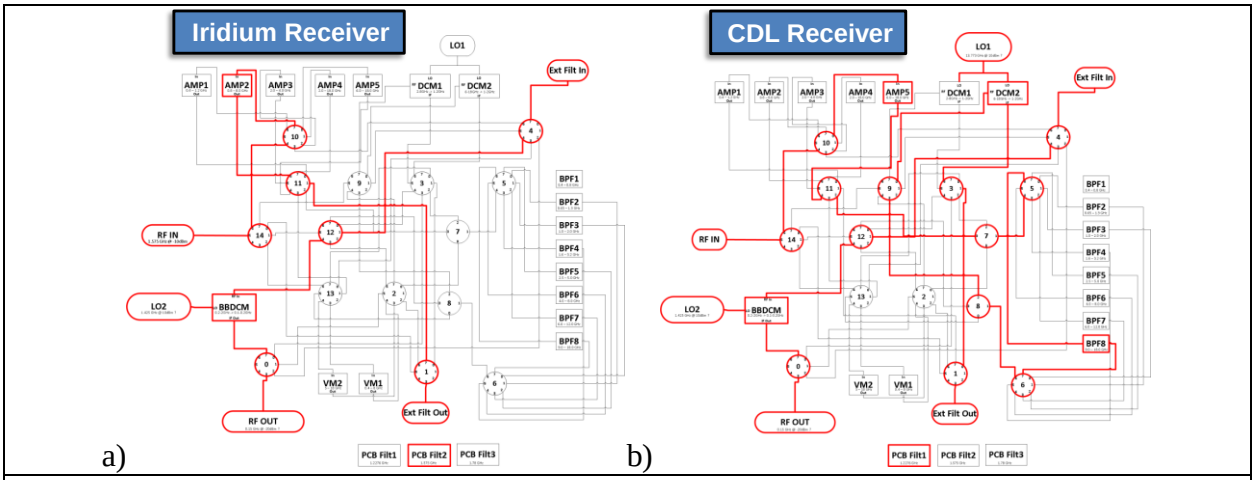

Figure 5.7 A schematic showing the paths of two possible ways the receiver can be reconfigured. a) is for an Iridium system, while b) is for a CDL receiver

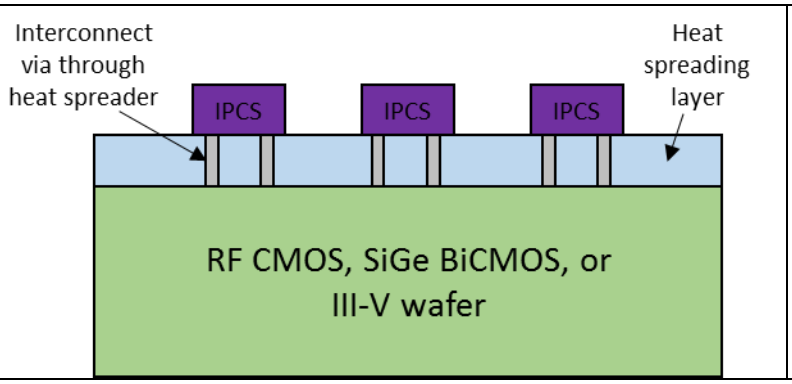

Figure 5.8 schematic cross-section cartoon of phase-change switch devices monolithically integrated with active RF components in their native process

While the current demonstration suffices for proof of concept, it also comes with undesirable limitations that can easily be overcome with the size and performance advantages offered by a fully monolithic integration. In the current approach, flip-chip integration imposes minimum size constraints on the switch chiplet due to mechanical constraints (handling and structural integrity) and due to a relatively large electrical interconnect section (per switch) that is required to achieve good electrical match and isolation within the integrated SiGe BiCMOS/PCS assembly. When compared to a monolithic approach (pictured in Figure 5.8) that would create phase-change switch devices monolithically in the BiCMOS process, fewer high

throw-count switches would need to be used due to the availability of any switch in any area. Monolithic integration would also negate the need for a larger switch chip area, resulting in dramatically less transmission line losses associated with simply wiring up the phase-change switches, and give the designer more flexibility on component placement and negate the need for long, cross-chip lossy transmission lines in order to piece together complementary components. Finally (and perhaps most importantly), monolithic integration would allow for the heaters to be contacted from below (i.e. a different height-plane than the transmission line) and eliminate the parasitic capacitance to the heater contact pads, which is a significant capacitance contribution limiting the performance of the phase-change switch in either grounded or floating configurations [52].

5.5 Substrate Agnostic Monolithic Integration of Inline Phase-Change Switches

While IPCS devices can be heterogeneously integrated with active RF circuitry (in either CMOS or SiGe BiCMOS process) to create reconfigurable circuits and systems [43]–[45], [52], the routing losses associated with the heterogeneous integration can negate much of the benefit in using the low-loss IPCS devices [43], as described in the previous section. In principle, monolithic integration can solve this problem by significantly reducing parasitic losses of the switching network [43]. The low deposition temperature (~250°C [54]) and high tolerance to crystalline defects allows PCMs to be fabricated in any traditional semiconductor process, compatible with the 400°C limit of Cu-BEOL CMOS fabrication processes [32]. Digital memory architectures using PCMs take advantage of this quality by integrating PCMs at the end of a BEOL process to avoid consuming expensive/desirable silicon wafer real-estate and metallization levels [32].

The special monolithic integration challenge for IPCS devices relative to their digital

memory PCM counterparts is dissipating the significant increase in thermal energy required to melt and quench the device into the OFF-state. In order to quench any chalcogenide in the amorphous state, the heat required to melt the PCM needs to be dissipated quickly enough to avoid recrystallization during cooling [31], [77]. Modern dash-confined PCM cells only melt and quench a volume less than 20 nm on each side (7.5 nm x 17 nm x 17 nm, or $2x10^{-6}$ μm^3) [78], [79]. In contrast, 1-2 Ω ON-resistance IPCS devices must melt and quench a volume that is 300nm in length, 110nm thick, and 30µm wide (0.99 μm^3) [69]. This ~10^6 increase in

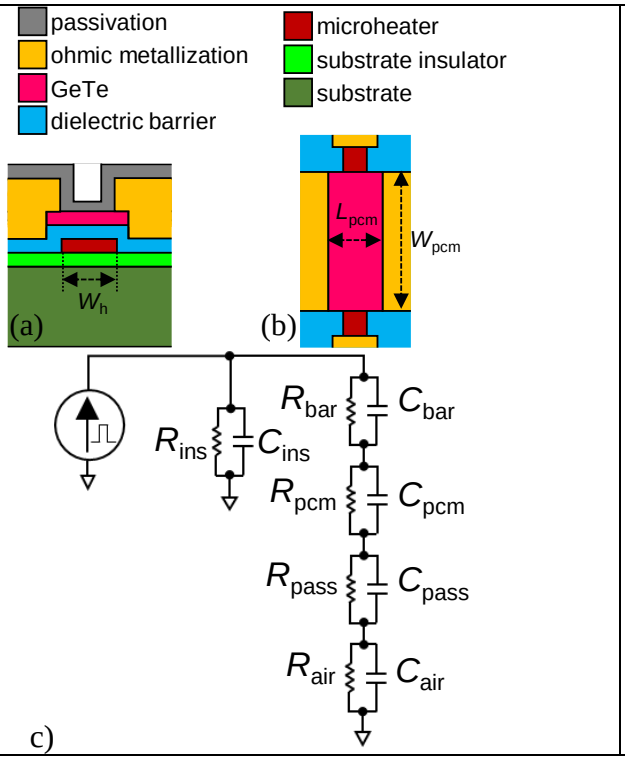

Figure 5.9 (a) schematic cross-section and (b) top-down schematic of the IPCS device (c) thermal circuit schematic of the IPCS device center pictured in (a). Resistances and capacitances are defined in the text.

melt/quench volume (and hence heat) in IPCS devices places severe restrictions on the thermal design in order to successfully quench the device into the OFF-state. In dedicated IPCS fabrication processes, this is done by balancing the materials and thicknesses (thermal resistances and capacitances) in relation to a large thermal ground—the substrate [40], [54]. However, monolithically integrating IPCS devices at the end of a BEOL CMOS process poses a unique problem. Typical interlayer dielectrics (ILD) are on the order of microns in thickness [32], and

the thermal conductivity (κ_{th}) of these films is typically low (0.5-1 W/m·K [80]). Thus the thermal resistance to ground (and associated thermal time constant, τ_{th}) will be large and render the switch inoperable.

In this section, the experimental demonstration of a CMOS-compatible substrate-agnostic monolithic integration process for IPCS devices is presented, as first described in [43]. This is accomplished by introducing a BEOL-compatible heat spreading dielectric layer (AlN) on top of the thick oxide, which acts as a heat sink to successfully quench IPCS devices in the OFF-state. This heat spreading layer enables their monolithic integration on any substrate, regardless of materials used.

5.5.1 Thermal Design

The IPCS device cross-section and plan-view is depicted in Figure 5.9(a) and (b), and the corresponding thermal circuit schematic is shown in Figure 5.9(c). The amorphization process can be understood as having two primary components: (1) the melting of the PCM (GeTe) as the charging of thermal capacitor C_{pcm} and (2) the quenching of the PCM as the discharging of C_{pcm}.

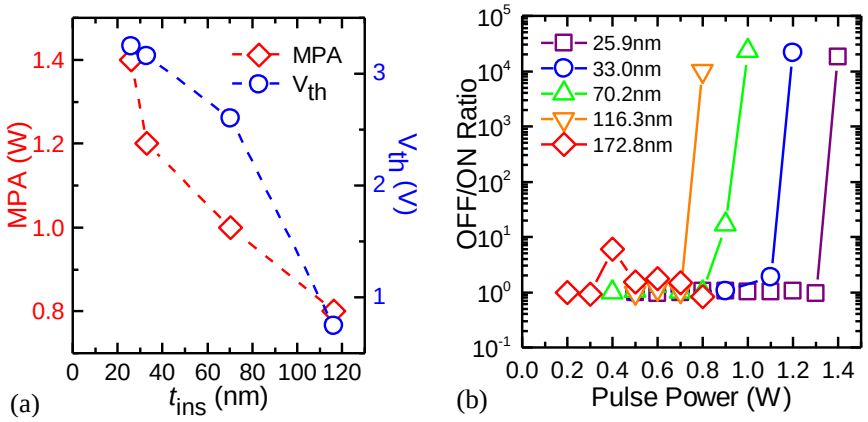

Figure 5.10 (a) MPA and V_{th} as a function of t_{ins}. Larger t_{ins} results in an increased thermal efficiency (reduced MPA) but also a larger τ_{th} (reduced V_{th}) (b) Pulse power vs. OFF/ON ratio (MPA test) grouped by t_{ins}. For t_{ins} larger than ~120nm, the OFF-state could not be realized.

In order to successfully quench the device in the OFF-state, the charged C_{pcm} (molten GeTe) needs to be discharged (cooled) fast enough to prevent the two crystal growth fronts originating

from the crystalline/supercooled-liquid interface from meeting in the center of the device [69], [81].

By increasing τ_{th} with thicker or less thermally conductive layers, it is possible to prevent the IPCS device from turning OFF (amorphizing) entirely. Due to the low thermal conductivity of the passivation (R_{pass}) and the air above (R_{air}), the dielectric between the heater and the substrate (SiO_2 substrate insulator in Figure 5.9(a)) becomes the critical parameter in balancing the thermal efficiency of the pulse versus the quench speed of the device. This effect is shown in Figure 5.10(a), where the measured minimum power to amorphize (MPA) (defined and explained in detail in [82]) and threshold voltage (V_{th}) of identical layout devices decrease as a function of substrate insulator thickness (t_{ins}). Wafers were fabricated with the Gen1 process, described in detail in [40] and [13], with t_{ins} varying between 20-180 nm. No other layer thicknesses were modified. The fabricated dimensions and ON-resistance for devices in Figure 5.10 were 0.9 µm L_{pcm}, 1.3 µm W_h, 10 µm W_{pcm}, and 5-6 Ω, respectively. The MPA decreases with increasing t_{ins}, as more of the pulse power is delivered to C_{pcm} instead of being shunted to the substrate. The V_{th} decreases with t_{ins} as the larger τ_{th} allows the crystal growth fronts to propagate further, decreasing the length of the amorphous region [82]. Figure 5.10(b) shows the MPA test for the devices shown in Figure 5.10(a), where the pulse power is increased until a 10^4 change is seen in

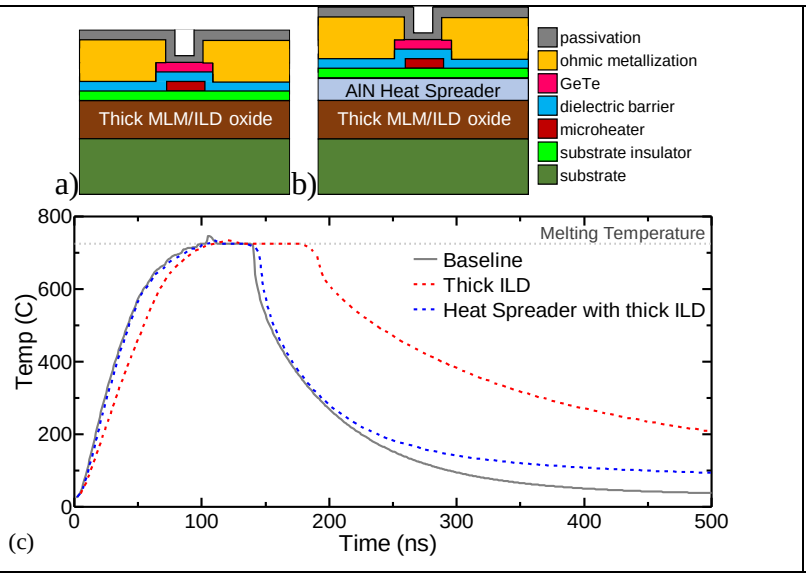

Figure 5.11 schematic cross-section of monolithic BEOL IPCS integration with (a) no heat spreader and (b) with an AlN heat spreader. (c) Thermal simulations of the devices pictured in Fig. 1(a) (solid gray), Fig. 3(b) (dashed red), and Fig. 3(b) (dashed blue) showing the quench on the AlN heat spreader is possible

device resistance [50]. For t_{ins} larger than 120nm, the τ_{th} is large enough that the OFF-state cannot be achieved.

In order to quench the device in the OFF-state for t_{ins} larger than 120 nm (as would be the case in a BEOL integration), a heat spreading layer is introduced above the oxide (Figure 5.11). The goal of the heat spreading layer is to act as a pseudo thermal ground, meaning it will absorb the heat from the molten GeTe in a manner sufficient to quench the GeTe in the OFF-state, without the heat actually dissipating into the substrate. For the heat spreader to work correctly, the new thermal time constant to discharge C_{pcm} must be as close to the baseline process as possible. This requirement most directly translates to a high thermal conductivity for the heat spreading layer, with a thickness (thermal capacitance) large enough to temporarily store all the energy from the melt. In addition, the deposition of the heat spreading layer must be compatible with the 400°C temperature limit of BEOL CMOS processes [32]. Sputtered aluminum nitride (AlN) can meet these requirements, as it can be deposited below 400°C with thermal conductivities between 10-50 W/m·K depending on the thickness [53]. 2-D thermal simulations of the integrations depicted in Figure 5.9(a) (baseline), Figure 5.11(a) (BEOL thick ILD with no heat spreader), and Figure 5.11(b) (BEOL thick ILD with heat spreader) are shown in Figure

5.11(c). Details on the simulation methodology can be found in [50]. For these simulations, an ILD thermal conductivity of 1.1 W/m·K was used at a thickness of 1 µm, and an AlN conductivity of 50 W/m·K was used at a thickness of 2 µm, with a 60nm SiO_2 capping layer. The pulse width is kept constant for each simulation (100 ns), but the pulse power in the heater is adjusted to raise the GeTe to the same temperature in each integration in order to evaluate the quench speed from a common temperature (0.48 W/µm^3 for baseline, 0.28 W/µm^3 for thick ILD, and 0.285 W/µm^3 for heat spreader with thick ILD). The thermal simulations in Figure 5.11(c) show it is possible to sufficiently match the baseline quench rate using an AlN heat spreader.

5.5.2 Device Fabrication and Results

To experimentally demonstrate the modeled results, high-resistivity Si wafers were thermally oxidized with a 250 nm thick SiO_2 layer—thick enough that IPCS devices cannot be quenched to the OFF-state. AlN was then sputtered deposited as described in [53], with thickness ranging from 0.5 µm to 4 µm. For each AlN thickness, additional wafers with a 30 nm PECVD SiO_2 capping layer following AlN deposition were included in the experiments. The fabrication then followed a modified Gen 2 process [82]. Briefly, a 50 nm thick etched-W microheater was patterned, followed by deposition of a 60 nm PECVD SiN barrier and dry-etched heater contact vias. Instead of a room-temperature sputter lift-off GeTe pattern process, a heated sputter deposition of 110 nm GeTe was patterned with an RIE using CHF_3 and O_2. A 0.25 µm thick evaporated Ti/Au ohmic contact was then patterned with lift-off, finishing with a 160 nm PECVD SiN passivation layer with dry-etched contact vias.

Figure 5.12(a) shows an MPA test undertaken for identical layout devices with no heat spreader, 3 µm AlN, and 4 µm AlN variants, compared to the baseline process. The measured devices had dimensions of 2.5 µm L_{pcm}, 1.3 µm W_h, and 10 µm W_{pcm}, pictured in the inset of

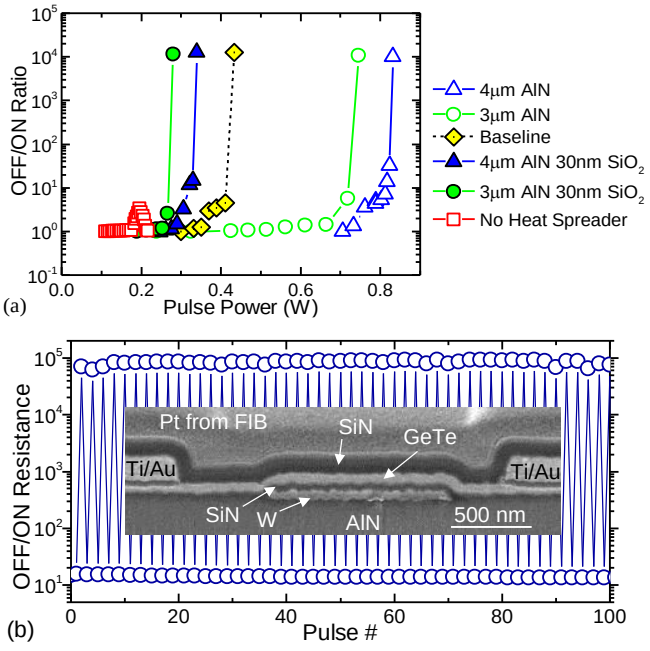

Figure 5.12 (a) MPA test of different AlN heat spreader thicknesses and capping layers compared to baseline. (b) 100 pulse cycling of a device on 3 um of AlN. The inset shows a SEM picture of the device after cycling.

Figure 5.12. The devices had a resistance of 15-16 Ω due to the larger L_{pcm} (3x) compared to the devices in Figure 5.10, which was done to remove or limit any quenching effect of the ohmic metal [50]. Without the heat spreader, a minor resistance change can be achieved, but not the full 10^4 resistance ratio transition to the OFF-state. Both the 3 µm and 4 µm AlN thicknesses (no SiO_2 cap) could successfully achieve the OFF-state, with a larger MPA than the baseline process. This is indicative of the lower τ_{th}, due to the high κ_{th} of the AlN. The larger MPA for 4 µm compared to the 3 µm film is indicative of the increased AlN thermal conductivity as a function of thickness [53]. Figure 5.12(a) also shows the successful amorphization of the 3 and 4 µm AlN heat spreader devices with 30 nm SiO_2 cap. The MPA in this case was lower than baseline devices, demonstrating that the thermal resistance can be tuned using the AlN heat spreader to match the baseline MPA. AlN heat spreader thicknesses below 3 µm could not be successfully switched OFF, but it is unclear whether this a thermal limitation or due to the W microheater delaminating from the AlN surface. More work is needed to optimize the fabrication process and determine the optimal AlN thickness to match the baseline process reliability and performance

levels.

Figure 5.12(b) shows cycling data up to 100 pulses for a device on 3 µm AlN. The devices typically did not have the reliability of the Gen2 process (< 500 pulses before failure), but it is unclear whether this is a thermal limitation, or a processing limitation due to the AlN-W adhesion or the roughness of the AlN. The inset of Figure 5.12(b) shows a SEM of the device cycled 100 times, where the roughness in the AlN is translated directly to the heater and overlying materials.

5.6 Conclusion

The low-loss and non-volatile nature of the IPCS technology enables highly reconfigurable, broad band, and high frequency RF systems. Three different prototypes were created using the heterogeneous integration of IPCS devices and commercial SiGe BiCMOS circuitry. While the prototypes demonstrated the usefulness and advantages of IPCS devices used as a low-loss switching network, the losses contributed by the heterogeneous integration negate a large portion of the benefit in these systems. The substrate agnostic monolithic integration of phase-change switches allows for the highly reconfigurable architecture to be deployed in any semiconductor technology. IPCS devices were fabricated on 3 and 4 µm AlN heat spreading layers to demonstrate this integration, and could be successfully quenched despite having a thick SiO_2 layer between the device and the substrate. The successful operation of IPCS devices integrated with thick oxide and heat spreader experimentally demonstrate a CMOS-compatible monolithic integration process, which can be applied to any substrate or underlying material.

6 Conclusions and Outlook

6.1 Conclusions

This thesis detailed the demonstration, performance, and integration of 4-terminal, indirectly heated phase-change switches for reconfigurable RF systems. The first demonstration of device functionality outperformed SOA FET-based RF switches in terms of frequency performance (1.1 THz F_{co}), and was improved by over an order of magnitude over the course of this research (12.5 THz F_{co}). The improvements were made by improving the fabrication in order to accommodate thicker materials while still being able to quench the device into the OFF-state, and by scaling the dimensions for lower resistances and capacitances. Using a standard III-V MMIC process flow, multiple circuits were fabricated including an SPDT that showed the lowest insertion loss among competing solid-state or MEMS technologies.

The investigations into power handling resulted in an extracted threshold field of 12.6 V/μm in 50:50 GeTe, an improvement in OFF-state power handling from 18 dBm to 29 dBm, and a switch with a simultaneous R_{on}, C_{off}, F_{co}, V_{th}, $P_{RFmax,off}$, and reliability of 1.2 Ω, 12.3 fF, 10.6 THz, 6 V, 28 dBm, and >500,000 cycles, respectively. The dependence of V_{th} on pulsing parameters and layout was investigated, with a fundamental trade-off between F_{co} and V_{th} being identified. A change from NiCrSi to W was made for the Gen2 and Gen3 devices, which drastically increased the reliability, V_{th}, and power handling of the switches. A correlation between the DC V_{th} and the RF power handling was demonstrated, identifying the fundamental mechanism for power handling limitations.

Three different reconfigurable RF system prototypes were created and demonstrated using heterogeneous integration of these phase-change switches. The heterogeneous integration combined the high performance phase-change switches with a commercial SiGe BiCMOS

MMIC to create a reconfigurable RF system. Problems with the RF performance of the system highlighted a critical area of improvement for the integration of phase-change switches, and a monolithic integration approach was developed as a result. A BEOL, CMOS-compatible monolithic integration scheme was demonstrated for the first time, detailing the benefits of future monolithically integrated phase-change switches on a variety of semiconductor technologies.

6.2 Future Research Directions

Through the research that has been presented in this thesis, there are certain research directions that have either a clear need to be addressed before this technology can become mainstream, or present very unique device and material property investigations.

6.2.1 Reliability

The final major hurdle for any semiconductor technology to become mainstream is to address endurance and reliability requirements. In addition to providing critical insights on device physics during the melt, quench, and recrystallization processes, King et al. [83],[69] identifies the major failure mode mechanism in IPCS devices as being void conglomeration in the center of the device. Improvements to both the material deposition and device integration have created devices in the Gen2 and Gen3 process that have been cycled greater than 1 million cycles, but limitations in test stand time and test protocol have prevented obtaining larger set of statistics in this area. Further research, fabrication volume, and frankly test stand time is needed in this area in order to demonstrate how different material deposition parameters or fabrication techniques can improve the reliability to desired standards. In addition, the concept of "reliability" will need to be refined in a much more thorough manner by device manufacturers and circuit designers, as no JEDEC standards exist for such a new technology.

6.2.2 Superconducting Phase-Change Switches

GeTe has previously demonstrated superconductivity, and has been incorporated into cryogenic circuits and measured and cycled at cryogenic/mK temperatures using this inline phase-change switch process [84]. The superconducting channel opens the possibility of creating an almost ideal switch (zero R_{on} at DC) with contacts spaced extremely far apart to reduce C_{off} even further. This type of switch has many important and critical cryogenic applications, in addition to creating a near lossless RF switch.

6.2.3 Pulsed V_{th} experiments and Power Handling vs. Frequency

Section 4.7 correlated the $P_{RFmax,off}$ to the V_{th} of the device, and attempted to use this data to gain insights into the fundamental nature of threshold switching. Unfortunately this was limited by the ability of the test stand to measure when the devices threshold switched into a quasi ON-state. By pulsing individual OFF-devices and monitoring the voltage drop across them during the pulse, it would be possible to determine how much time at specific field strengths is necessary to initiate threshold switching. From this, a model could be built to predict what the $P_{RFmax,off}$ vs. frequency would look like, and actual measurements of the $P_{RFmax,off}$ vs. frequency could then verify whether breakdown at RF frequencies is accomplished in a single RF half-cycle, or whether it needs to accumulate over many cycles.

6.2.4 Linearity (IP_3) vs. Threshold Voltage (V_{th})

Initial data certainly suggests that the linearity (IP_3) of the OFF-state is correlated to the V_{th} of the device, but a formal derivation from the ON and OFF-state I-V curves is necessary in order to develop a complete understanding of the linearity dependence in phase-change switches.

6.2.5 Empirical FoM and $W_{h,min}$ derivations

Section 4.6 plotted and discussed the inherent trade-off between Fco and Vth. By adding the energy to amorphize into the trade-space, a more useful FoM can be created that combines all the trades a designer could make in sizing and operating the device. More importantly, it is possible to empirically define the FoM only as a function of fabrication thicknesses and material properties, and create a theoretical framework that can maximize the FoM for different integrations and materials.

7 Thesis Contributions

7.1 A Four-Terminal, Inline, Chalcogenide Phase-Change RF Switch Using an Independent Resistive Heater for Thermal Actuation

- Published in IEEE Electron Device Letters [40]
- First demonstration of a 4-terminal indirectly heated phase-change RF switch
- Outperformed SoA FETs with initial, un-optimized process (1.1 F_{co})

7.2 A 7.3 THz, Inline, Chalcogenide Phase-Change RF Switch Using an Independent Resistive Heater for Thermal Actuation

- Published in 2013 IEEE Compound Semiconductor Integrated Circuit Symposium [51]
- Demonstrated significantly improved RF performance through layout and process scaling
- Outperformed all SoA technologies with 7.3 THz F_{co}

7.3 12.5 THz Fco GeTe Inline Phase-Change Switch Technology for Reconfigurable RF and Switching Applications

- Published in 2014 IEEE Compound Semiconductor Integrated Circuit Symposium [12]
- Demonstrated further improved RF performance with additional fabrication scaling and a more complex integration
- Demonstrated ability of switch to be used in a legitimate MMIC process with the inclusion of microstrip designs and TSVs
- Reported on the consequences of measuring/extracting insertion loss, isolation, and F_{co} with different heater terminal configurations

7.4 Low-loss latching microwave switch using thermally pulsed non-volatile chalcogenide phase change materials

- Published in Applied Physics Letters [13]
- First demonstration of an SPDT using indirectly heated phase-change switches
- Lowest demonstrated insertion loss of published RF switch technologies

7.5 Thermal Analysis of a Heat Pulsed Non-Volatile Phase Change Material Microwave Switch

- Published in Journal of Applied Physics [50]
- Correlated measured MPA and MPC values to simulated values based on thermal simulations (thermal simulations performed by Rob Young)
- Developed framework for valid device pulsing parameters as a function of pulse width (PTE analysis performed by Rob Young)

7.6 Morphological analysis of GeTe in inline phase change switches

- Published in Journal of Applied Physics [69]
- First STEM observation of amorphous GeTe created in indirectly heated phase-change switches
- Correlation between larger pulse powers and larger amorphous regions
- Observations of crystalline changes in GeTe and microheater with different pulse conditions

7.7 Examination of the Temperature Dependent Electronic Behavior of GeTe for Switching Applications

- Published in Journal of Applied Physics [59]

- Reported on the electrical behavior of amorphous GeTe down to 10°K
- Reported the successful switching of indirectly heated phase-change switches down to 10°K
- Fit a space-charge limited conduction model to amorphous GeTe at different temperature regimes
- Demonstrated the lack of OFF-resistance dependence on C_{off} by measuring isolation as a function of temperature

7.8 Substrate Agnostic Monolithic Integration of the Inline Phase-Change Switch Technology

- Published in 2016 IEEE International Microwave Symposium [43]
- Reported the problems with heterogeneous integration of the reconfigurable transceiver
- Reported the first monolithic integration concept of indirectly heated phase-change RF switches

7.9 Origin and Optimization of RF Power Handling Limitations in Inline Phase-Change Switches

- Published in IEEE Transactions on Electron Devices [82]
- Reported the power handling limitations of the different processing generations
- Reported the V_{th} dependence on pulse power, pulse width, and layout dimensions in the Gen1 process
- Demonstrated the V_{th} vs. F_{co} trade-off exists for indirectly heated phase-change RF switches

- Extracted the critical threshold field for 50:50 GeTe through STEM observation of amorphous length
- Developed second-generation process with W-microheaters in order to improve reliability, $V_{th,}$ and RF power handling
- Developed third-generation process with CMOS like formation of W-microheaters to improve F_{co}, reliability, $V_{th,}$ and RF power handling
- Demonstrated SPST with less than 0.13 dB insertion loss from 0-65 GHz
- Demonstrated a switch with simultaneous R_{on}, C_{off}, F_{co}, V_{th}, $P_{RFmax,off}$, and reliability of 1.2 Ω, 12.3 fF, 10.6 THz, 6 V, 28 dBm, and >500,000 cycles, respectively
- Correlated the V_{th} to the OFF-state power handling capability of the devices

7.10 Experimental Demonstration of AlN Heat Spreaders for the Monolithic Integration of Inline Phase-Change Switches

- Published in IEEE Electron Device Letters [85]
- Reported on the trade-off between MPA and V_{th} as a function of insulator thickness
- Reported on the quenching limits of the device as a function of insulator thickness
- Demonstrated the first successful switching of indirectly heated phase-change switches on AlN using a monolithic integration concept

7.11 Recent Advances in Fabrication and Characterization of GeTe-based Phase-change RF Switches and MMICs

- Published in 2017 IEEE International Microwave Symposium [47]
- Reported on an SPDT with less than 1 dB of insertion loss and 40 dB of isolation from 0-65 GHz using the Gen3 process

7.12 Connecting Post-Pulsing Electrical and Morphological Features in GeTe-based Inline Phase Change Switches

- In publication review at Journal of Applied Physics
- Demonstrated void content in GeTe films as the limiting factor in device reliability
- Developed framework for correlating R_{on} and R_{off} with void content
- Demonstrated reduced void content using heated deposition methods

7.13 Operation of a Latching, Low-Loss, Wideband Microwave Phase-Change Switch Below 1 K

- In publication review at Journal of Applied Physics
- First demonstration of indirectly heated phase-change switch operation down to 40°mK

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