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System Level Analysis And Design For Wireless Inter-Chip Interconnection Communication Systems By Applying Advanced Wireless Communication Technologies

Xin Zheng
University of South Carolina

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by

Xin Zheng

Bachelor of Science
University of Electronic Science and Technology of China, 2007

Bachelor of Business Administration
University of Electronic Science and Technology of China, 2007

Master of Science
University of Electronic Science and Technology of China, 2010

Master of Science
University of Electronic Science and Technology of China, 2012

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Accepted by:

Yinchao Chen, Major Professor

Paul Huray, Committee Member

Krishna Mandal, Committee Member

Xiaofeng Wang, Committee Member

John Rose, Committee Member

Cheryl L. Addy, Vice Provost and Dean of the Graduate School

DEDICATION

To my dear wife, Yi Chen, my parents Hui Zheng, and Ju Wu, and my children Tiancheng and Khaleesi Zheng.

To Dr. Yinchao Chen.

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ABSTRACT

As the dramatic development of high speed integrated circuits has progressed, the 60 GHz silicon technology has been introduced to enable much faster computer systems and their corresponding applications. However, when signals are propagating at 60 GHz or higher frequencies on a PCB (Printed Circuit Board), the crosstalk among signal buses and devices, trace losses, and introduced parasitic capacitance and inductance between high density traces, become significant and may be severe enough such that the inter-chip communications will not be able to meet computer system signal specifications. High speed circuit signal integrity researchers in both electronic industries and academia have explored various methodologies to resolve these high frequency issues. Moreover, Intel is introducing Ultra Path Interconnect (UPI) for multi-core server systems, which demands more than 2.44 Tbps data rate between two CPUs, and 1.5 Tbps data rate for PCIe channel operation.

Recently, the concept of the wireless inter/intra-chip interconnection (WIIC) technology was introduced [19, 23] for solving high frequency signal integrity issues. Here this dissertation mainly focuses on the inter-chip case while still using the WIIC designation for generality. Various WIIC technologies have been presented in the literature, which have focused on the investigations on Ultra Wide-Band (UWB), propagation channels, modulations, antennas, and power controls and interference.

However, not much research has focused on a system level design, which includes the lowest two layers of the communication protocol in a WIIC system, namely, the physical, and data link layers. Also, the previously published literature has rarely reached the data rate at 100 Gbps or higher, and none of the prior research has obtained a spectrum utilization ratio of 4 bit/Hz or greater. In addition, currently existing research has not fully taken advantage of advanced and matured wireless communication technologies such as Orthogonal Frequency Division Multiplexing (OFDM), high order modulation, and Multiple-Input/Multiple-Output (MIMO) systems for increasing data rates and improving reliability, although the use of UWB [29], conventional FDMA or TDMA [39], and binary modulations including Binary Phase Shift Keying (BPSK) [22], On-Off Keying (OOK) [31], and Amplitude Shift Keying (ASK) [35] have been studied in previous research.

In this dissertation, a complete WIIC system and a representative WIIC channel model have been developed by taking full advantages of advanced wireless communication techniques. First, this research has analyzed the potential of higher-order modulation, error correction, OFDM, and channel coding to the WIIC setting. Although MIMO, interleaving and scrambling are also analyzed but not included in the current version of the proposed WIIC system, they could be featured in hypothetically ideal future research to determine their potential benefits. Second, the performance of a proposed WIIC system has been analyzed in order to reach 100 Gbps data rate. Third, a 60 GHz WIIC channel based on metamaterial Electronic Band Gap (EBG) absorbers has been designed and analyzed using the numerical electromagnetics solver HFSS® and this EBG is integrated into the representative WIIC channel. Moreover, the impulse response

of the WIIC channel is numerically extracted and is used for the system validation and testing. Furthermore, the system has been simulated with the WIIC channel and the wired PCB channel. It has been found that, the Bit Error Rate (BER) performance of the proposed WIIC channel is close to that of an AWGN channel with FEC, and much better than the AWGN channel without FEC, which means that the designed WIIC system and channel work properly within the frequency band centered at 60 GHz, while the wired PCB channel is almost cut off at 15 GHz or higher for the cases investigated. With only five or six layers on a PCB board, the WIIC system is able to provide 384 Gbps data rate theoretically with 12 GHz bandwidth, while the wired PCB counterpart needs more than 20 layers in order to avoid severe SI problems and to properly layout the Tbps channels. The current version of the WIIC system is able to provide 24 Gbps data rate with the bandwidth of 12 GHz using OFDM and QPSK.

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$a_{k^{(-)}}^{(p)}$	kth modulated OFDM symbol at antenna port p
T_s	Time slot
$N_{CP,l}$	Length of Cyclic Prefix
N	Total number of subcarriers
l	OFDM symbol index number
N_{FFT}	Points of FFT
Δf	Subcarrier bandwidth
β	Power control ratio
φ	Offset in the frequency domain location of the subcarrier within the PRBs
K	Difference in subcarrier spacing between DFT-S-OFDM and normal OFDM
Δf_D	Subcarrier bandwidth of DFT-S-OFDM
n_{PRB}^{signal}	First PRB number occupied by the signal
N_{sc}^{RB}	The number of subcarriers of a PRB
N_{RB}^{D}	The number of RBs of a channel of a DFT-S-OFDM system
W_N	Rotation factor
E_b	Bit energy of a BPSK signal

T_b Time duration of a bit in BPSK modulation

f_c Carrier frequency in modulation

E_S Symbol energy of a QPSK signal

T_S Time duration of a symbol in QPSK modulation

LIST OF ABBREVIATIONS

ADS ..... Advanced Design System

AMC ..... Artificial Magnetic Conductor

ARQ ..... Automatic Repeat reQuest

ASK ..... Amplitude-Shift Keying

AWGN ..... Additive White Gaussian Noise

BER ..... Bit Error Rate

BIOS ..... Basic Input/Output System

BLER ..... BLock Error Rate

BPF ..... Band-pass Filter

BPSK ..... Binary Phase-Shift Keying

CAZAC ..... Constant Amplitude Zero Auto-Correlation

CDMA ..... Code-Division Multiple Access

CP ..... Cyclic Prefix

CQI ..... Channel Quality Indicator

CRC ..... Cyclic Redundancy Check

CSI ..... Channel State Information

CTF ..... Channel Transfer Function

DFT ..... Discrete Fourier Transform

DFT-S-OFDM ..... Discrete Fourier Transform Spreaded OFDM

DPSK ..... Differential Phase-Shift Keying

DS ..... Delay Spread

DSP ..... Digital Signal Processor

DS-BPSK ..... Direct Sequence Binary Phase-Shift Keying

DS-CDMA ..... Direct Sequence Code Division Multiple Access

DUT ..... Device Under Test

EBG ..... Electromagnetic Band Gap

EIRP ..... Equivalent Isotropically Radiated Power

FDD ..... Frequency-Division Duplexing

FDMA ..... Frequency-Division Multiple Access

FDTD ..... Finite-Difference Time-Domain

FEC ..... Forward Error Correction

FFT ..... Fast Fourier Transform

FMRI ..... Functional Magnetic Resonance Imaging

FPGA ..... Field-Programmable Gate Array

FT ..... Fourier Transform

HFSS ..... High Frequency Structural Simulator

IDFT ..... Inverse Discrete Fourier Transform

IFDMA ..... Interleaved Frequency-Division Multiple Access

IFFT ..... Inverse Fast Fourier Transform

IR-UWB ..... Impulse-Radio based Ultra-WideBand

ISI ..... Inter-Symbol Interference

ITU-R ..... Telecommunication Union Radio

iWISE ..... inter-router Wireless Scalable Express Channel

LI ..... Linear Interpolation

LS ..... Least Square

LNA ..... Low-Noise Amplifier

LTCC ..... Low-Temperature Co-fired Ceramic

LTE .....Long Term Evolution

LTE-A ..... Long Term Evolution-Advanced

MATLAB.....Matrix Laboratory

MIMO ..... Multiple Input Multiple Output

MLS ..... Maximum Length Sequence

MMSE.....Minimum Mean Squared Error

MMW..... millimeter wave

OFDM .....Orthogonal Frequency Division Multiplexing

OFDMA .....Orthogonal Frequency Division Multiple Access

OOK.....On-Off Keying

OQPSK ..... Offset Quadrature Phase-Shift Keying

PA .....Power Amplifier

PAPR ..... Peak to Average Power Ratio

PCB..... Printed Circuit Board

PDF ..... Probability Density Function

PEC ..... Perfect Electrical Conductor

PMC ..... Perfect Magnetic Conductor

PRB.....Physical Resource Block

PCIe.....Peripheral Component Interconnect Express

QAM .....Quadrature Amplitude Modulation

QPP .....Quadratic Permutation Polynomial

QPSK ..... Quadrature Phase-Shift Keying

RB ..... Resource Block

RTD .....round trip delay

SC-FDMA ..... Single Carrier-Frequency Division Multiple Access

SDM ..... Space Division Multiplexing

SDMA ..... Spatial Division Multiple Access

SINR ..... Signal to Interference and Noise Ratio

SiP ..... System in a Package

SNR ..... Signal-to-Noise Ratio

TDMA ..... Time-Division Multiple Access

TDP ..... Thermal Design Power

TDR ..... Time Domain Reflectometry

TDT ..... Time Domain Transmission

TEM ..... Transverse-Electric-Magnetic

TNMSE ..... Truncated Normalized Mean Square Error

WAVA ..... Wrap-Around Viterbi Algorithm

WIIC ..... Wireless Inter/Intra-Chip Interconnection

WiMAX ..... Worldwide Interoperability for Microwave Access

WLAN ..... Wireless Local Area Network

WPAN ..... Wireless Personal Network

WSS ..... Wide Sense Stationary

VNA ..... Vector Network Analyzer

UMB ..... Ultra Mobile Broadband

UPI ..... Universal Path Interconnect

UWB ..... Ultra Wide-Band

ZC ..... Zadoff-Chu

1/3 TBCC ..... 1/3 Code Rate Tail-Biting Convolutional Coding

8PSK ..... 8 Phase-Shift Keying

CHAPTER 1

INTRODUCTION

1.1 Wired Interconnect Issues

As the dramatic evolution of high speed, high density integrated circuits has occurred for the rapid development of computer science and microelectronic industries, the use of silicon technology at 60 GHz has been explored for much faster, more reliable, and more compact computer systems [1-4]. However, when signals are propagating at 60 GHz or higher frequencies along a traditional integrated printed circuit board (PCB) transmission lines, the crosstalk, transmission loss, parasitic capacitance and inductance are significant and may be severe enough such that it will be very hard for digital communications on PCB boards to meet the designed signal specifications. Also, as a result of complex PCB circuits, the design cycle of planar circuits has been greatly elongated, and the testing and verification process have become more and more complicated. These signal integrity problems have been increasingly prominent, and the hardware and overhead costs have been substantially high. Meanwhile, with increasing clock frequencies and the number of the signal pins on integrated circuits and chips, the challenge of maintaining highly reliable interconnection communications between chips has become an issue of great importance. The problems of reflection at the interconnection of pins, the parasitic and mutual inductance and capacitance, and other signal integrity problems have been restricting the performance, clock frequency, and data rate of wired PCBs [5, 6].

Clearly, the high data rate in today's computer systems is very demanding. For example, in the current Intel multi-core wired PCB systems, Ultra Path Interconnect (UPI), which transmits high-speed data among CPUs, operates at more than 2.44 Tbps data rate for two CPUs, 68.78 Tbps for 8 CPUs; Peripheral Component Interconnect Express (PCIe), which carries signals between CPU and the peripheral components, transfers at the data rate about 1.5 Tbps for 2 CPUs, and 42 Tbps for 8 CPUs. Table 1.1 summarizes details of the data rates for these two high-speed data links.

Table 1.1 Data rates for UPI and PCIe links in multi-CPU systems

No. of CPUs	**UPI Data Rate**	**PCIe Data Rate**	**Total Data Rate for UPI and PCIe Channels**
2	2.44 Tbps	1.5 Tbps	3.94 Tbps
4	14.64 Tbps	9 Tbps	23.64 Tbps
8	68.78 Tbps	42 Tbps	110.78 Tbps

However, in order to support the high speed requirements listed in Table 1.1, the high-speed channels operating at 9.6 GHz frequency requires thousands of channels at the data rate of 5.12 Gbps for each channel, and thousands of traces in a number of PCB boards should be designed meet the SI requirements and specification. The essential drawbacks for the wired PCBs are briefly summarized as follows.

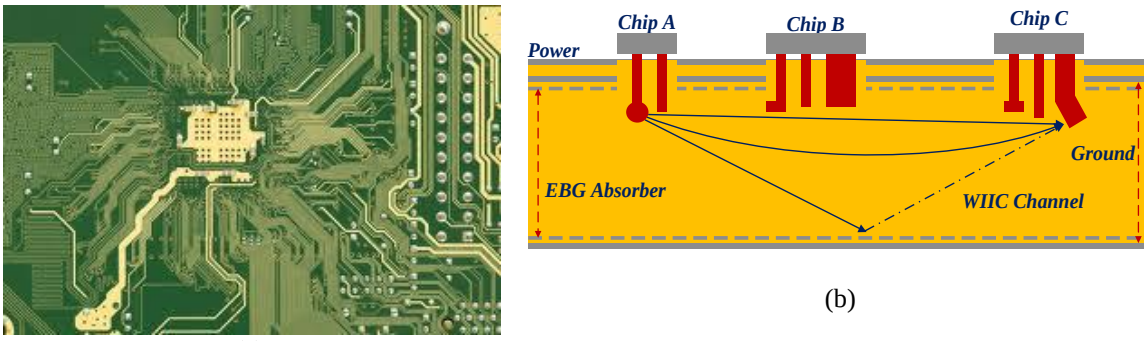
- **SI problems for high speed wired channels.** At Tbps data rates, SI problems, including crosstalk, transmission loss, parasitic capacitance and inductance, signal dispersion and distortion have become more and more severe.
- **Extremely high demand of next generation of high-speed channels on PCB board.** The next generation of the proposed high-speed channels, which operate at 60 GHz or above, will bring more and more significant SI issues. According to

the measurement in this dissertation, one of the most innovative PCBs is not able to provide reliable communications at such a speed. As a result, not only SI engineers are highly demanded to support the new version of the high-speed signaling, but also the material engineers should provide new formulas to improve communication environments in PCBs.

- **Increment of PCB cost.** In order to support the high speed channels in the wired PCB, the numbers of the traces for interconnect channels have been increased dramatically. Meanwhile, the layers of the wired PCB have to be augmented, which will directly add the cost for the wired PCBs.
- **Elongated design cycle.** The design cycle of the wired PCB channels has been significantly elongated, as SI engineering takes longer and longer time to perform simulations before actual board design. During the design process of a PCB board, electric engineers make tremendous efforts to design the wired channels, to perform accurate simulations, to correlate the simulations and measurements, and to verify the PCB design.
- **Testing and verification issues.** The process of testing and verification has become more and more complicated, expensive, and time consuming.

1.2 Wireless Inter-chip Interconnection

Recently, Wireless Inter-Chip Interconnection (WIIC) technology has been introduced into industry and academia for exploring novel solutions to the problems of wired inter-chip communication systems. The major concept of the WIIC communication is to provide a supplement to the existing high density trace communication by using wireless communication technology, as shown in Figure 1.1.



(a) (b)

Figure 1.1 The concept of WIIC communication developed in this research. (a) Traditional high-density, trace-based interconnect PCB, and (b) the concept of the proposed WIIC communication system with an EBG absorber.

At very high frequencies, a WIIC system can present various advantages over the traditional trace-based interconnection systems. First, the wireless interconnect channel will have more freedom than its correspondingly wired counterparts, in terms of the placement of the broadband transceivers printed into communication chips. Second, the WIIC system can reduce the cost of PCBs, as the number of PCB layers is reduced from more than ten layers to no more than five. Third, when traces are removed from the systems, crosstalk, time delay, distortion and dispersion will be greatly reduced or completely eliminated with proper wireless configuration and design, although interferences from the existing wired transmissions and WIIC channels are unavoidable. Fourth, the long cycles in designing PCB trace wiring and routing will be alleviated. Furthermore, another advantage brought by wireless is that it can easily and efficiently do broadcast (or multicast) transmission. Also, because the proposed PCBs are parallel metal layers, electromagnetic waves can be made to propagate broadband signals at a high speed with low time latency. Finally, the newly designed WIIC communication system can take advantages of the techniques developed for advanced, mature macro wireless and mobile communication systems. In addition, it has to be pointed out that electromagnetic interference generated by the wireless communication can be greatly

reduced by using the parallel ground planes and the metamaterial Electromagnetic Band-Gap (EBG) absorber layers.

1.3 Previous WIIC Research

Both industry and academia have done research on the WIIC to solve the signal integrity problems brought by the use of higher frequency and high density PCBs. The dominant previous research of the WIIC mainly focused in the following areas:

- **Micro-Antenna Design.** Many early works focused on micro-antenna analysis. Traditional chip pins were extended and converted to micro-antennas to achieve the wireless interconnection between chips for the purpose of solving the interconnection and signal integrity issues [7-19]. For instance, in these works, on-chip diode [9], Low-Temperature Co-fired Ceramic (LTCC) antennas [10], leaky wave antennas [11], nano-antennas and integrated antennas [12, 17], directional antennas [13], miniaturized antennas [15], ladder reflector antennas [16], and tapered slot antennas [19], were designed and analyzed. Other closely related research focused on the packaging wireless transceivers [7], transmission gain of an antenna [12], clock delivery in the WIIC communication systems [14], and the feasibility of using antennas [18]. These literatures' analysis, comparison, and design for different types of antennas have helped the RF system design used in the WIIC system. In the current version of the WIIC system presented in this dissertation, the type of the antenna has been chosen as on-chip dipole. In future the directional antennas will be used to provide spatial diversity.

- **Propagation Channel Analysis.** It was reported that researchers developed and analyzed a number of wireless signal propagation channel models [20-26]. Some

of these references focused on the resulting BER induced by the propagation channels [22, 24], while the other channel analyses employed the overly simplified Friis transmission formula [23], Cagniard-DeHoop model [25], multi-band network-on-chip [20], and the Finite-difference time-domain (FDTD) analysis [25] techniques. Three groups of researchers used a full wave analysis of WIIC systems by extracting the scattering parameters for a simplified wireless system from the point of view of RF and microwave network analysis [26-28]. According to these analyses, the WIIC channels are almost linear and time-invariant with path loss, distortion and dispersion.

- **UWB Technology and Power Analysis.** UWB technology was investigated to make the WIIC systems low-power, wide-band, and low BER [22, 29, 30]. Based on the UWB technology development, several researchers focused on minimizing power consumption of the systems [31-40]. As the UWB is a power efficient technology, most of this research improved power efficiencies [105-108].
- **Interference Mitigation or SINR Improvement.** The interference problems between WIIC antennas were analyzed recently by a number of researchers [22 24]. As a result, a number of technologies were put forward attempting to mitigate the interference, including using DS-CDMA (Direct Sequence Code Division Multiple Access) [41], spatial diversity [43], dynamic power control methods [31], and using different MA approaches, namely, TDMA and FDMA. Some progresses were made in attempting to solve the interferences and noise problems by using some schemes such as interference avoidance and dynamic power control [22, 31, 40, 43, 45].

- **Clock and Timing Issue Analysis.** A few researchers analyzed the clock and timing issues that can possibly appear in a WIIC system. One work analyzed the clock delivery in a WIIC system [14], and another paper was interested in the issues of wireless transmission of a clock signal of the system in a package (SiP) [41].
- **Wireless Optical Communication Applications in the WIIC Systems.** Researchers have also analyzed the opportunity of implementing the wireless optical communication technology in the WIIC systems [73, 86-89], i.e., the Optical-Wireless Network-on-Chip (OWN). The optical wireless communication systems are usually low-latency and scalable, but they suffer from issues such as high component cost and complex device-to-device variations [113]. In addition they often have large power consumption requirements, especially for off-chip layers. One of the references focused on a high-frequency broadcast "OWN" system using the frequency band from 172 THz to 222 THz [88], and analyzed the transmission loss of the system, while other papers analyzed MIMO [86], and one-hop photonic interconnect with Time Division Multiplexing (TDM) [89] applications in OWN communications.

1.4 Limitation of Previous WIIC Research

Most of the previous WIIC technologies have encountered a number of limitations, most of which fail to provide a system level overview, to greatly show the advantages of WIIC systems over the traditional trace based (wired) PCB communication channels, and to effectively illustrate its feasibility in practice. The drawbacks and limitations for previous research are summarized as follows:

- **Lack of System Level Analysis and Design of WIIC Technologies.** Firstly, a system level design in PCB signal transmission is missing in most of the published research. In this dissertation, the system level design is defined as the design of functional block diagrams for the lowest two layers of the communication protocol in a WIIC system, namely, the physical and data-link layers. The major effort of system level design will focus on the design for signal processing to obtain higher signal processing speed, which certainly indicates high power consumption [49]. The system level design also includes the analyses of data rate, reliability (BER), latency, estimations for energy and chip area consumption, and manufacturability.
- **Interference Issues Resulted from Multiple Access Methods.** Secondly, the existing research mostly employed the conventional multiple access methods, such as Frequency-Division Multiple Access (FDMA), Time-Division Multiple Access (TDMA) [39], Code-Division Multiple Access (CDMA) [41, 42] or the newly developed multiple access method, namely, inter-router Wireless Scalable Express Channel (iWISE) [45], which is a hybrid of TDMA and FDMA as the channel access methods in transmitting the wireless signals. Even though there is low crosstalk among signals, the interference resulted from the multiple access method still remain in these WIIC systems. Usually, the interferences brought by the traditional multiple access methods are not BER performance limiting but lowering the interference is still high demanding in WIIC systems. Hence, it would be preferred to employ Orthogonal Frequency Division Multiple Access

(OFDMA) in order to minimize interference and to increase the data rate in comparison to the conventional FDMA.

- **Without Taking Great Advantages from Advanced Wireless Communication Technologies.** Previous research did not take full advantage of advanced and matured wireless communication technologies. For example, these researchers mainly used Binary Phase-Shift Keying (BPSK) [22, 27], binary Differential Phase-Shift Keying (DPSK) [41], On-Off Keying (OOK) [31], or binary Amplitude-Shift Keying (ASK) [35] as the modulation methods. Obviously, more bandwidth efficient modulation methods, such as Quadrature Phase-Shift Keying (QPSK) and Quadrature Amplitude Modulation (QAM), are highly desirable for increasing data rate dramatically. This may be due to the fact that these simple modulation methods are low-cost, simple to implement, and energy-efficient with a low peak-to-average power ratio (PAPR). Meanwhile, widely used in macro wireless and mobile communication systems, like the Orthogonal Frequency Division Multiplexing (OFDM) are not found to be employed in any of these WIIC systems. This may be resulted from that OFDM is not as power efficient as those technologies, such as Ultra Wide-Band (UWB) or IR-UWB (Impulse-Radio based Ultra Wide-Band) based WIIC systems. As a result, the published research paid a lot more attention to the channels and the power control [28, 39, 34-40], while not mainly focusing on one of the most important issue in the previous WIIC systems, that is, achieving high data rate and improving spectral efficiency [24, 37, 38, 43]. However, if the WIIC system cannot reach similar data rate as the wired counterpart, the wired communication issue would still significant on the

PCBs. Table 1.2 shows a comparison of the bandwidths, data rates, and spectrum utilizations of the previous WIIC systems and the wireless technologies that can be potentially used in a WIIC system and applied in this dissertation, including OFDM, QPSK, and QAM.

Table 1.2 Spectrum utilization comparisons

Year and System	**Technology Used**	**Bandwidth**	**Data Rate**	**Spectrum Utilization**
2014 (WIIC) [33]	3-D IC	28.3 GHz	10 Gbps	0.35 bit/Hz
2012 (WIIC) [39]	IR-UWB BPSK	5 GHz	5 Gbps	1 bit/Hz
2010 (WIIC) [38]	IR-UWB	N/A	200 Mbps	N/A
2006 (WIIC) [24]	UWB	7.5 GHz	200 Mbps	0.027 bit/Hz
2015 (Optical WIIC) [73]	Optical WIIC	20 GHz	25 Gbps	1.25 bit/Hz
2009 (LTE) [46]	OFDM QPSK	20MHz	33.6 Mbps	1.68 bit/Hz
This Design	FDMA QPSK SISO	12 GHz	24 Gbps	2 bit/Hz
	OFDM QPSK SISO	12 GHz	24 Gbps	2 bit/Hz
Theoretically Upper Bound of the System	OFDM 256QAM 4×4 ideal MIMO antennas	12 GHz	384 Gbps	32 bit/Hz

- **Rarely Seeing the Application of Metamaterials in the Previous WIIC Systems.** Finally, in the previous research, it has not been found that metamaterial applications were commonly used in the wireless channel construction, including the Artificial Impedance Surface (AIS) and Electromagnetic Band Gap (EBG). It is found that the metamaterials can be used to build up a high frequency and broadband channel for the WIIC systems and are capable to prevent electromagnetic wave leakage.

1.5 Objectives of the Dissertation

The project goal is to develop a WIIC system, which includes a transmitter, a propagation channel, and a receiver. A channel bounded with metamaterial-based absorbing layers to create a novel PCB propagation channel was designed and analyzed. The designed WIIC channel will be inserted into the developed WIIC system as a functional box for assessment. Precisely, the proposed research concentrates on the following objectives:

- **System Level Analysis and Design of the WIIC System.** The first objective is to develop a system level analysis and design methodology which includes the physical, and data-link layers of the WIIC protocol, in order to reach a higher data rate. Although the final goal for the proposed WIIC system is 3.94 Tbps, more realistically, the starting point in this dissertation is to attempt to reach 100 Gbps. Channel coding, estimation and equalization will be implemented in the WIIC system after determining the channel characteristics, in order to decrease BER by correcting errors caused by the channel. Channel equalization modifies the channel impulse response or transfer function to make it closer to a desired form. Furthermore, the high order modulation method and OFDM technologies will be analyzed for their capability to be integrated into the WIIC system to increase the data rate and spectrum utilization. Moreover, a Cyclic Prefix (CP) will be employed to deal with signal round trip timing delay between chips and multipath delay spread.
- **Construction and Characteristic Determination of WIIC Propagation Channel Models.** Second, one of the most important objectives is to develop a practical WIIC propagation channel model by using HFSS. An innovative PCB structure with the

metamaterial EBG wave absorber layers was designed, and the equivalent circuit of the absorber unit was developed. Using the simulated results, various channel models will be constructed with consideration of attenuation, dispersion, time delay and delay spread. The S-Parameters of the designed WIIC channel are generated in HFSS for further analysis including impulse response and transfer function extraction, and link budget analysis.

- **Measurement of Wired PCB Channels.** Third, a PCB channel with the current transmission line technology was analyzed and measured. Time Domain Reflectometry (TDR) and Time Domain Transmission (TDT) of the PCB channel was measured and simulated, in order to extract the impulse response of the channel.
- **Impulse Response and Transfer Function Extraction.** Furthermore, the S-Parameters of the WIIC, and the simulated wired PCB channel, along with the measured TDR/TDT of the wired PCB channel, will be used to extract the impulse response by injecting a non-perfect unit impulse into the channel's input ports. The channel transfer functions of the systems will be then extracted by performing a Fourier Transform (FT) to the extracted impulse responses. Employing this method is to guarantee the consistency of the results extracted from the simulated S-Parameters and the TDR/TDT measurements. The transfer functions of the simulated/measured wired PCB, and simulated WIIC channels are compared accordingly.
- **Validation and Virtual Implementation of the WIIC System.** Finally, the designed WIIC system with all the developed technologies listed above will be validated theoretically and implemented in simulation using MATLAB to obtain the

BER performance for the cases of the Additive White Gaussian Noise (AWGN), the wired PCB and the designed WIIC channels. In the validation, perfect Digital Down Convertor (DDC) and Low-Pass Filter (LPF) are assumed in the WIIC systems, and the gains for Power Amplifier (PA) and Low-Noise Amplifier (LNA) are counted in link budget and are combined with other gains in SNR and BER analysis. For the issues of power and chip area consumption, especially for the QAM, FFT, and MIMO are analyzed and estimated in the dissertation, but the actual implementation issues of these technologies will be handled via future technology advances.

1.6 Content of the Dissertation

The second chapter of this dissertation mainly introduces the method of the Orthogonal Frequency Division Modulation (OFDM) applied in the WIIC system, from the points of views of both concept and implementation perspectives. Chapters 3 and 4 are, respectively, to present a system level WIIC communication system analysis and design, including the detailed transmitter, and receiver. The system will include error detecting and correcting, interference control methods, modulation, and multiple access method. Chapter 5 discusses the design, measurement, and parameters extraction of channel models. Three types of channel models are investigated, including the AWGN, wired PCB and WIIC channel models. The WIIC channel model is constructed by implementation of two metamaterial EBG absorber layers. The absorber unit design and equivalent circuit development are also included in this chapter. Chapter 6 describes the virtual WIIC system in MATLAB, and compares the BER performance of the designed WIIC channel with AWGN and the wired PCB channels. Chapter 7 is the conclusion of the dissertation, and the summary of the future the WIIC research.

CHAPTER 2

ORTHOGONAL FREQUENCY DIVISION MODULATION USED IN WIIC TRANSCEIVERS

This chapter is a brief introduction to the Orthogonal Frequency Division Multiplexing (OFDM) technology proposed for future use in the WIIC transceivers. It also covers the advantages, disadvantages, types, and block diagrams of the OFDM.

2.1 The OFDM Concept

The OFDM is frequently used in wireless communication for splitting a frequency band into a number of sub-bands or subcarriers for the purpose of eliminating complex equalizers that is required in single carrier systems. OFDM is also able to improve reliability by taking advantage of efficient FFT circuitry that allows elimination of complex and relatively power-inefficient equalizers required for comparable single-carrier systems. OFDM divides the time-frequency resource plane into slots as Resource Elements (REs), which can be easily allocated to different users. With the OFDM employed in a communication system, the multiple access method Orthogonal Frequency Division Multiplexing – Frequency Division Multiple Access (OFDM-FDMA), or Orthogonal Frequency Division Multiple Access (OFDMA) can be employed. The OFDM and OFDMA are widely applied in the fourth generation of mobile communication protocols such as Long Term Evolution (LTE), Ultra Mobile Broadband (UMB), and Worldwide Interoperability for Microwave Access (WiMAX). However, it

has not been reported that they are used in any Wireless Inter- and Intra-chip Interconnection systems, which may be due to the fact that they are not as power efficient as UWB, although UWB is currently limited in applications mainly for effective designs of millimeter wave (MMW) and RF components.

In a conventional multi-carrier system such as the Frequency Division Multiple Access (FDMA), there is often a band gap between two subcarriers to diminish inter-carrier interference as shown in Figure 2.1. The reason for this is that the imperfect band-pass filters (BPF) at the receiver cannot separate the signals on different carriers if they are too close to each other. Nowadays, the guard band is relatively smaller than it used to be, but it is still a significant problem to be improved for spectrum utilization.

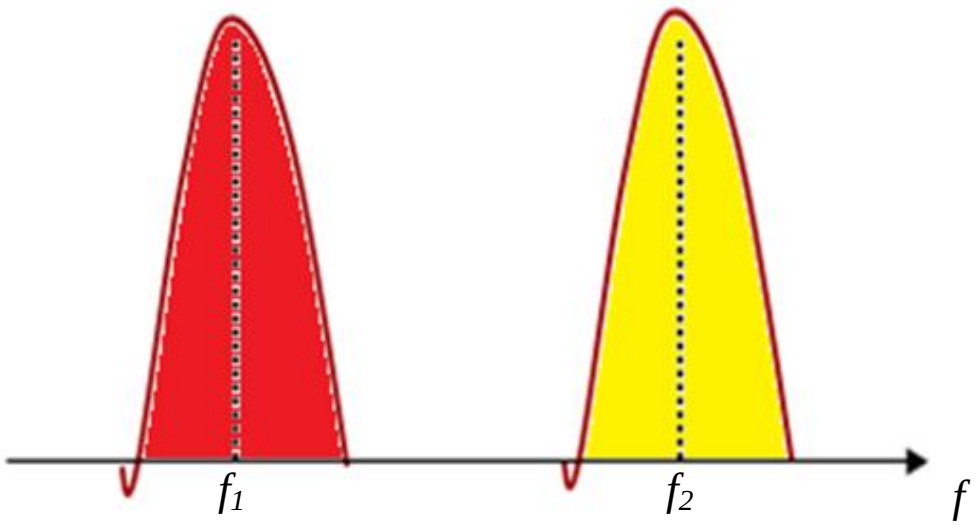


Figure 2.1 Subcarriers in conventional multi-carrier systems.

The OFDM, however, is a technology that divides the whole channel bandwidth into a number of subcarriers, where each subcarrier is orthogonal to one other with minimal frequency separation. It means that theoretically the amplitudes of a signal's Fourier transform at all the central frequencies of other subcarriers are zero in magnitude. The subcarriers in an OFDM communication system are shown in Figure 2.2.

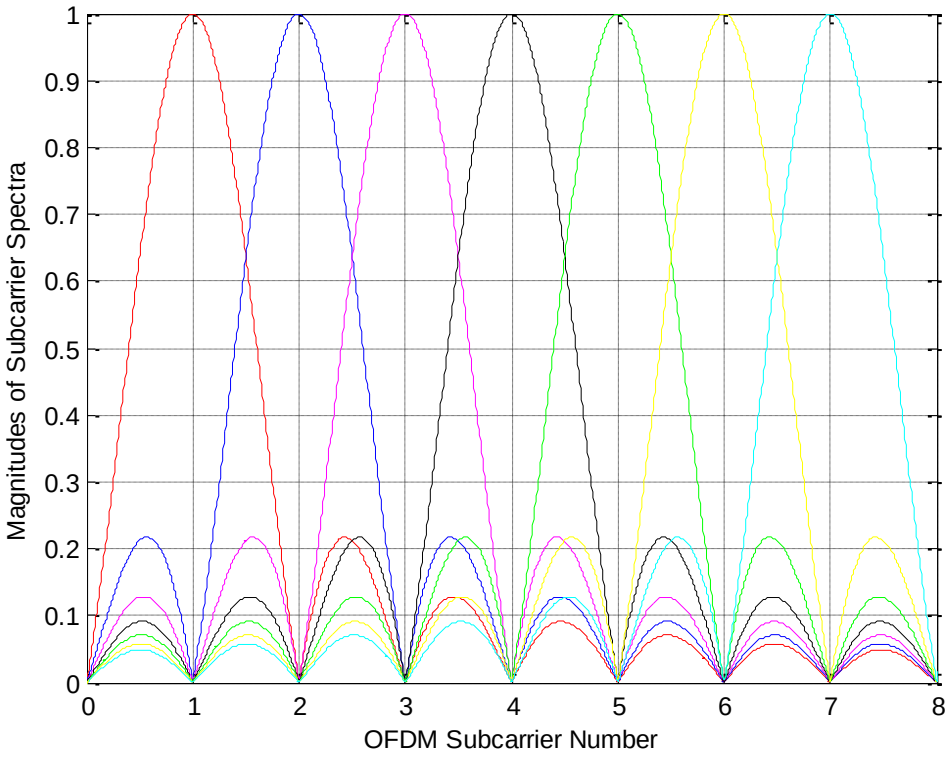


Figure 2.2 Subcarriers in an OFDM system.

In this case, no matter how the channels (or subcarriers) are distributed to the chips, in the WIIC systems, channels used by one chip should have little interference to one another. Consequently, the main concept of the OFDM is to convert a broadband signal into some number of multi-carrier narrow-band signals to deal with the poor channel circumstance, namely, allocating sub-carriers to the subscribers with smaller attenuation, and minimize the dispersion across any single subcarrier.

The OFDM technique has been shown to have various unique advantages over the conventional multi-carrier FDMA systems. The primary advantage of the OFDM over the conventional multi-carrier schemes is its ability to cope with a number of different small time-frequency slots other than dealing with wideband signals. Second, using OFDM means the requirement for design of band pass filters can be much relaxed. Third, as long

as the signal bandwidths are small enough, the channel equalization is much simplified in comparison to equivalent-bandwidth single-carrier schemes because OFDM signals can be viewed as a set of narrowband, slowly modulated signals rather than wideband, rapidly modulated ones. Furthermore, because OFDM can increase the spectral efficiency, the data rate is also increased for the same bandwidth. For example, with only 20 MHz total bandwidth, with single subcarrier bandwidth to be 15 kHz:

- In the LTE standard, the OFDM technology can provide over 200 Mbps data rate with 64QAM [46].
- In the LTE-Advanced standard, the data rate even exceeds 3 Gbps [46].
- The conventional FDM can only reach $20\ MHz \times \log_2 64\,\text{bit} = 120\ \text{Mbps}$ with the same bandwidth, 64QAM and with perfect band-pass filters (which is not realistic) [51].

Moreover, since the high data rate signals are modulated to the OFDM symbols with much lower symbol rates, which make use of a guard interval between symbols affordable, this makes it possible to circumvent Inter-Symbol Interference (ISI). Also, OFDM can include channel equalization and subcarrier allocation schemes to improve the Signal to Noise and Interference Ratio (SINR) by allocating time-frequency slots with smaller noise, attenuation and fading to the subscriber [76-79]. Finally, unlike conventional frequency division multiplexing (FDM) systems, the OFDM receivers do not require high-performance BPFs to obtain all signals on different sub-carriers, which will reduce hardware development cost.

2.2 OFDM Technologies

There are a number of types of OFDM such as the conventional OFDM, Digital Fourier Transform Spread OFDM (DFT-Spread-OFDM, or DFT-S-OFDM), Generalized OFDM (G-OFDM), Filtered-OFDM (F-OFDM), OFDM/O-QAM (OFDM/offset QAM), etc. The conventional OFDM is often associated with its multiple access method OFDMA, and the DFT-S-OFDM is usually implemented in conjunction with the multiple access technology named Single Carrier-Frequency Division Multiple Access (SC-FDMA). Both the conventional OFDM and the DFT-S-OFDM will be discussed in the following sections.

2.2.1 The Conventional OFDM

A typical block diagram of an OFDM transmitter can be described as shown in Figure 2.3.

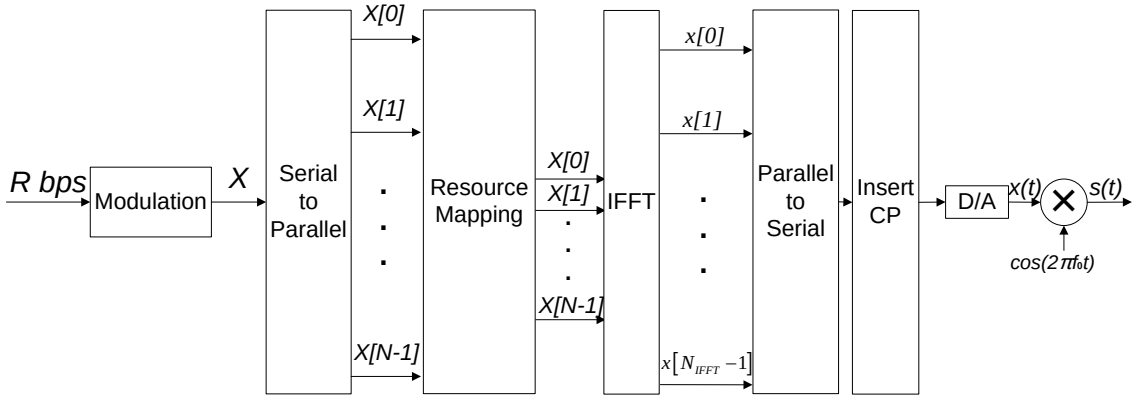


Figure 2.3 Block diagram of an OFDM transmitter.

Herein the modulation scheme can be chosen from a variety of methods and the serial-to-parallel operation converts a high bit rate stream to low symbol rate OFDM symbols. The serial-to-parallel block is used to collect a series of symbols that will be mapped onto a set of subscribers during the same time slot. The resource mapping block allocates the

symbols in one time slot to their frequency positions, *i.e.*, the subcarriers in the frequency domain, before the processing of IFFT. The IFFT block performs a function to convert a signal from the frequency domain to the time domain. The block of Parallel to Serial and Insert CP provides an output time domain signal and enable handling of the timing and ISI issues in the channel.

The time domain expression of an OFDM signal is given as follows [46]:

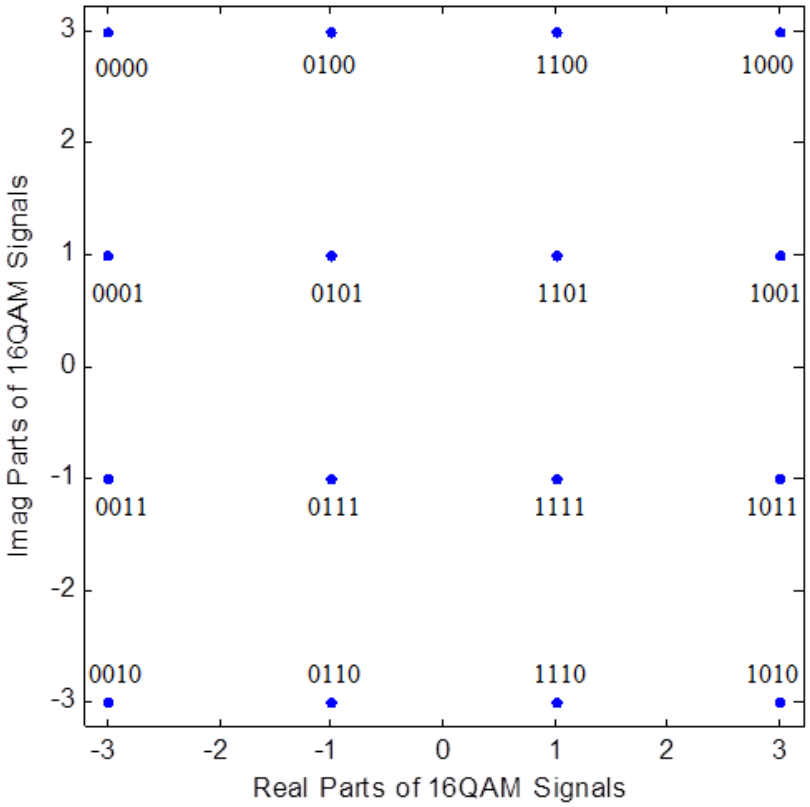
$$s(t) = \sum_{k=-\lfloor N/2 \rfloor}^{-1} a_{k^{(-)},l} \cdot e^{j2\pi k\Delta f(t-N_{CP,l}T_s)} + \sum_{k=1}^{\lfloor N/2 \rfloor} a_{k^{(+)},l} \cdot e^{j2\pi k\Delta f(t-N_{CP,l}T_s)} \quad (2.1)$$

where time duration t satisfies $0 \le t \le (N_{CP,l} + N_{FFT})T_s$, $a_{k,l}$ is the $(k,\ l)th$ OFDM symbol, $l = 1, 2, 3, ...,k = -\lfloor N/2 \rfloor, -\lfloor N/2 \rfloor + 1, \dots, \lfloor N/2 \rfloor - 2\ \lfloor N/2 \rfloor - 1$, N is the total number of subcarriers, and Δf is the bandwidth of one subcarrier. The OFDM symbols in a time slot shall be transmitted in an increasing order of l, which is the time domain OFDM symbol index number, starting from 0 and ending at $\sum_{l'=0}^{l-1}(N_{CP,l} + N_{FFT})T_s$ within a time slot when $l = 1, 2, 3, ...$The OFDM symbols will be modulated in the frequency domain and indexed by subcarrier number k. In the equation above, N_{FFT} and $N_{CP,l}$ are the total number of points, respectively, for Inverse Fast Fourier Transform, and the Cyclic Prefix (CP). Also, $k^{(-)}$ and $k^{(+)}$ are the frequency domain subcarrier numbers and defined as:

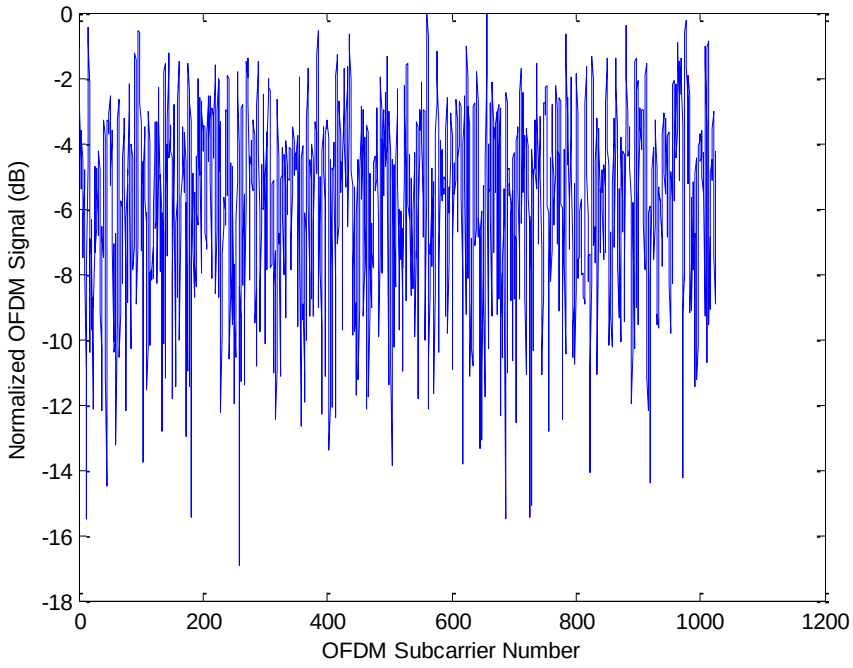
$$k^{(-)} = k + \lfloor N/2 \rfloor \quad (2.2)$$

$$k^{(+)} = k + \lfloor N/2 \rfloor - 1 \quad (2.3)$$

The 16-QAM modulated constellation, which is the input signal of an OFDM functional block, and the OFDM processed signal are shown in Figure 2.4 for N_{FFT}=1024.



(a)



(b)

Figure 2.4 Input and output of the OFDM functional block. (a) The input 16QAM constellation to the OFDM functional block, and (b) the average output of the OFDM baseband processing of 500 realizations.

2.2.2 The DFT-S-OFDM

The conventional OFDM has an issue of high Peak to Average Power Ratio (PAPR), which can potentially lead to power consuming problems. In contrast, in the DFT-S-OFDM processing, the Serial to Parallel (S/P) block in the conventional OFDM is replaced by a Digital Fourier Transform (DFT) block in the DFT-S-OFDM to convert a multi-carrier signal into a single carrier signal, in order to reduce PAPR. Other parts of the DFT-S-OFDM are the same as those in the conventional OFDM. The multiple access method of DFT-S-OFDM is called Single Carrier Frequency Division Multiple Access (SC-FDMA). The DFT-S-OFDM can be mathematically represented as [46]:

$$s(t) = \beta \sum_{k=0}^{N-1} \sum_{n=0}^{N-1} x(n) e^{-j\frac{2\pi nk}{N}} e^{-j2\pi(k+\varphi+K(k_0+1/2)\Delta f_D(t-t_{CP}))}, 0 \le t \le T_{SEQ} + T_{CP} \quad (2.4)$$

where T_{SEQ} is the length of the transmitted signal, factor β is the power control ratio, and φ is an offset variable for determining the frequency domain location of the subcarrier used in the DFT-S-OFDM within the Physical Resource Blocks (PRBs). The channel resources in OFDM systems are partitioned in the time-frequency plane, *i.e.*, groups of subcarriers for a specific time duration. Such time-frequency blocks are known as Resource Blocks (RBs). RBs usually include Physical Resource Block (PRB) and Virtual Resource Block (VRB). The PRBs can be allocated to the sub-channels. For example, a PRB in LTE communication systems typically includes seven contiguous OFDM symbols in the time domain, and twelve contiguous subcarriers in the frequency domain. The factor $K = \Delta f / \Delta f_D$ describes the difference in subcarrier spacing between the DFT-S-OFDM and conventional OFDM, where Δf is the subcarrier bandwidth of the conventional OFDM, which is the same in Equation (2.4). Δf_D is the subcarrier bandwidth of the DFT-S-OFDM, The symbol k_0 is given as follows:

$$k_0 = n_{PRB}^{signal} N_{sc}^{RB} - N_{RB}^{D} N_{sc}^{RB}/2 \tag{2.5}$$

where n_{PRB}^{signal} is the first Physical Resource Block (PRB) number occupied by the signal, N_{sc}^{RB} accounts for the number of subcarriers of one single PRB, and N_{sc}^{RB} represents the number of RBs of a channel of a DFT-S-OFDM system.

The DFT-S-OFDM procedures can be described in the block diagram as shown in Figure 2.5.

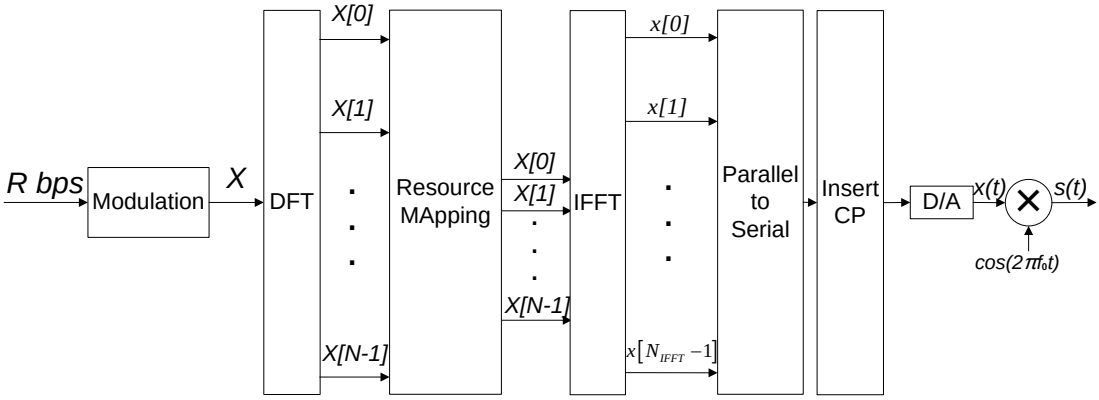


Figure 2.5 Block diagram of a DFT-S-OFDM transmitter.

The differences between the conventional OFDM (OFDMA system) and the DFT-S-OFDM (SC-FDMA system) can be graphically described in Figure 2.6 [47].

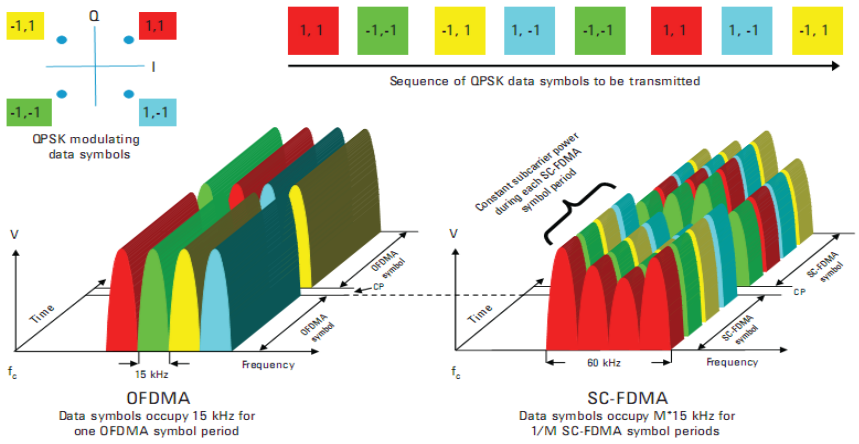


Figure 2.6 Graphical representation of differences between the OFDMA and SC-FDMA [110].

In the example above, a series of eight modulated QPSK symbols is mapped by both the procedures of the conventional OFDM and the DFT-S-OFDM to the time and frequency resources. For conventional OFDM, assuming that the subcarrier bandwidth is 15 kHz and there are four subcarriers per time slot, the total bandwidth of the conventional OFDM signal is 60 kHz. In contrast, for the DFT-S-OFDM, the same bandwidth of 60 kHz is used, which is also the total bandwidth for the subcarrier of DFT-S-OFDM. As a result, the conventional OFDM system consumes two time slots to transmit a total of eight QPSK symbols, while the DFT-S-OFDM employs eight time slots to transmit all the symbols. In other words, the spectrum utilization of the DFT-S-OFDM system is not as high as the conventional OFDM. However, single carrier transmission from DFT-S-OFDM will provide lower PAPR, flexible transmission bandwidth, but the scheduling in the frequency domain is channel dependent.

There are two different ways to distribute the total bandwidth of DFT-S-OFDM, namely, the localized FDMA and distributed FDMA (also called Interleaved FDMA, IFDMA). Their differences are shown in Figure 2.7.

For the Localized FDMA, each transmitter uses localized spectrum in the frequency domain, *i.e.*, consecutive blocks spectrum within the whole frequency band. In contrast, the distributed FDMA distributes signals from all users equally in the frequency domain. Distributed FDMA provides frequency diversity and flexibility of sub-carriers allocations.

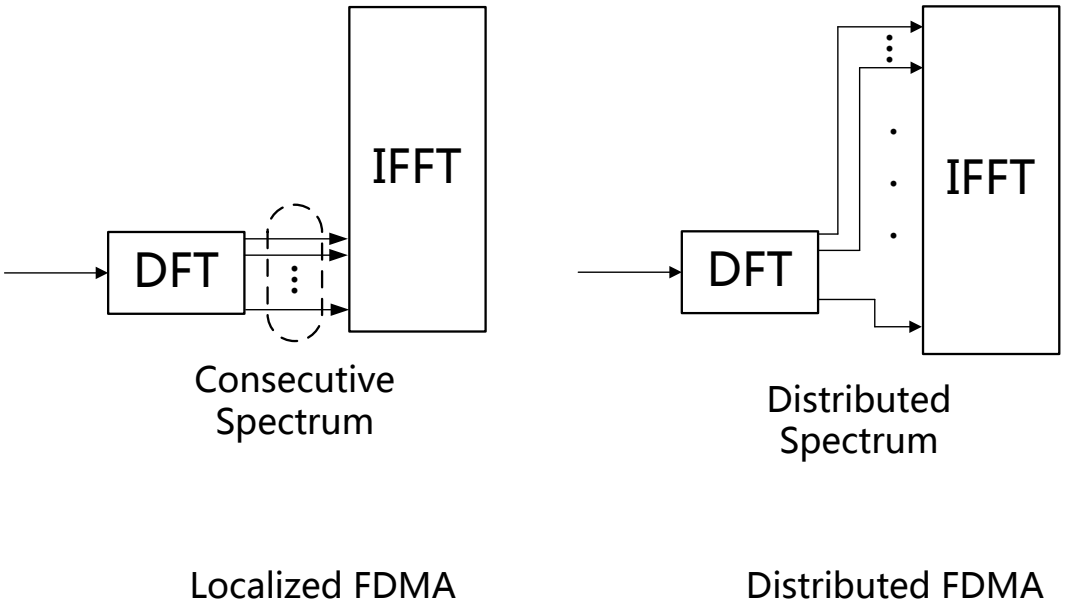


Figure 2.7 Localized FDMA vs. distributed FDMA.

2.3 OFDM Implementation and Multiple Access Method in the WIIC System

2.3.1 OFDM Implementation in the WIIC System

Unlike the DFT-S-OFDM, in most of the cases, signal transmission will be in a form of chip to chip, rather than the scenario of multiple chips transmitting signals to one "central" chip. Therefore, in the proposed WIIC system, the conventional OFDM is employed. In practical analysis, if a system has high PAPR, the WIIC system will switch to the SC-FDMA mode. In this mode, the Localized FDMA will be employed to reduce complexity of the system since it uses the consecutive spectrum for each sub-channel, and the IFFT size will be set to be smaller than that used in the Distributed FDMA.

2.3.2 Multiple Access Method Used in the WIIC System

In the dissertation, single carrier FDMA is first chosen as the multiple access method, and Time Division Duplex (TDD) is used to distinguish between transmitting and receiving for link budget and data rate calculations. Afterwards, OFDMA will be

applied as the primary multiple access method since it can provide better reliability and higher data rate for the same channel condition and frequency band without design of complicated equalizers. In order to minimize the PAPR problem brought by OFDM, the QPSK has been chosen as the modulation method in the dissertation, to attain a reasonable data rate and with a nearly-constant envelope.

CHAPTER 3

WIIC SYSTEM TRANSMITTER DESIGN

This chapter will primarily focus on the system level design and development of the WIIC transmitter. In the WIIC system, when a transmitter initiates a signal, all other existing chips including the receiver will receive it simultaneously. A process for a prescribed WIIC receiver to receive this signal only and for the other receivers to reject the signal will be described.

In practice, there are two ways to construct the wireless inter-connect transceiver system. One is just adding a modulation block to modulate the traditional baseband signal used on wired links to the required carrier frequency, and then transmit it with an antenna at the modulated frequencies, which is commonly used in the previous WIIC system and channel research. The other way is to employ higher order modulation and multiple carriers, as per the focus on the design of functional block diagrams of the system. The design also includes the analyses of data rate, reliability (BER), latency, estimations for energy and chip area consumption, and manufacturability. In this research, the latter approach is going to be used by applying the advanced wireless communication technologies such as OFDM, Forward Error Correction (FEC), interference control schemes, high order modulation, Cyclic Redundancy Check (CRC), and Cyclic Prefix (CP) for building up a virtual WIIC system.

3.1 Transmitter System Block Diagram

By using OFDM, adopting from an LTE system, a system block diagram for the WIIC transmitter is developed as shown in Figure 3.1:

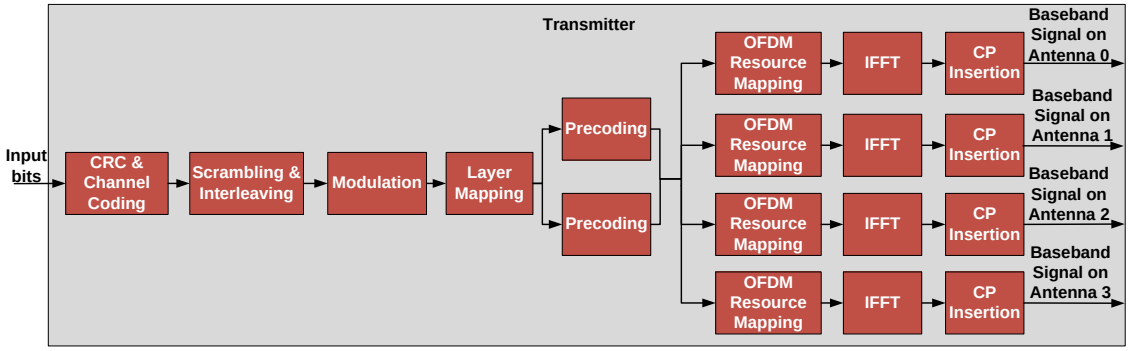


Figure 3.1 Block diagram of the WIIC transmitter with four diversity antennas.

The transmitter of the WIIC system includes error control schemes including FEC, and Cyclic Redundancy Check (CRC) [46]. In the modulation block, QPSK or QAM will be used to modulate bit streams to low symbol rate complex symbols [46]. The OFDM includes OFDM resource mapping and IFFT to allocate the QPSK or QAM symbols to PRBs. Besides, MIMO blocks consisting of layer mapping and precoding are also limitedly included, and these could be analyzed in future work if it can be demonstrated that these techniques can provide additional gains for a final version of the proposed WIIC system.

The remaining sections of this chapter will briefly summarize the design and analysis of each functional block listed in the WIIC transmitter, in total seven parts, i.e., Forward Error Control (FEC) schemes, interference control, modulation, reference signal generation, Cyclic Prefix, and the OFDM-UWB implementation. These parts mainly concentrate on the principles, procedures, and outputs for the subsystems. In each part,

there will be a decision to determine whether the block should be kept, replaced, or removed, and at the end of this chapter, a revised block diagram will be presented.

3.2 Error Control Schemes [46]

Cyclic Redundancy Checking (CRC), automatic repeat request (ARQ) and channel coding are normally employed for error checking and correction in wireless communication systems. Channel coding can correct errors due to a channel's unfavorable conditions in the process of decoding in the receiver side, while CRC is used for error checking after the channel decoding scheme, and the ARQ scheme is to send a request to the transmitter for requesting it to re-transmit the errored bits. In this proposed WIIC system, CRC and convolutional channel coding are included.

3.2.1 CRC [46]

An 8-bit CRC error checking technique is applied in the current implemented transmitter system, which can detect with high probability whether the decoded bits contain errors or not.

CRC error checking schemes can detect whether the decoded bit sequence contains errors or not, but it is not able to correct the errors. The CRC error checking result can be employed to calculate BLock Error Rate (BLER). The CRC error checking result can also be used to estimate the BER by dividing BLER by the number of bits in a transmission block.

3.2.2 Channel Coding [46]

The basic concept of channel coding is that, in a digital communication system, the transmitter employs a scheme that encodes an *n*-bit sequence into an *m*-bit signal,

where $m>n$. Therefore, the receiver can attempt to discover the transmission errors and try to correct some of them by decoding the received signal.

Many OFDM systems and other communication systems often employ convolutional coding as the encoding procedure. The convolutional coding can enhance the system performance when it uses a maximum likelihood decoding algorithm, which can correct some random bit errors from the channel. The system block diagram of a 1/3 Code Rate Tail-Biting Convolutional Encoder (1/3 TBCC) is shown in Figure 3.2.

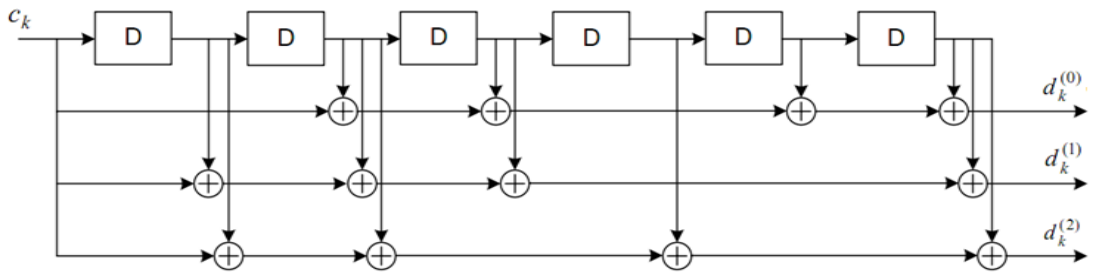


Figure 3.2 Block diagram of the 1/3 Tail-Biting convolutional encoder.

The 1/3 TBCC includes a 6-bit coding register, with the initial value to be the last six digits of the input signal. As a result of the processing, the end value of the register will be exactly the same as the initial value, which explains why this is called Tail-Biting Convolutional Coding. Because normal convolutional coding employs a method to make the end value of the registers to be the same as the initial values, another advantage of the 1/3 TBCC is that there will not be any extra redundant bits after the coding compared to the conventional convolutional coding algorithm. Since the data block size is equal to 1024 or 2048 bits in the WIIC system, these redundant bits are negligible here. The procedure to make the end values of the registers equal the initial values will generate redundant bits with the same length as the number of coding registers multiplied by the number of the output bit streams. Because of the uniqueness of this encoding algorithm,

the receiver can estimate the most likely transmitted sequence by computing the correlation metric between the received data and the possible codeword. The receiver typically employs a decoding method based on the Viterbi algorithm, which can correct errors.

In the initial implementation, channel coding, sounding, estimation and equalization are not included for a preliminary validation of the WIIC system. These features as well as the designed WIIC channels are subsequently added into the full system analysis for the validation and BER performance simulation.

3.3 Interference Control Methods [46, 76-80]

3.3.1 Scrambling [46]

The basic concept of scrambling is that, each chip uses a distinct scrambling mask to that is Exclusive OR-ed (XOR) with the signals. Adopting from the LTE system, the technique of scrambling in the proposed WIIC system is shown as follows:

$$b_k = \begin{cases} a_k \, , for \; k = 0, 1, 2, \dots, A-1 \\ (a_k + x_{k-A}) \bmod 2, for \; k = A, A+1, A+2, \dots, A+15 \end{cases} \qquad (3.1)$$

where b_k represents the scrambled sequence with receiver scrambling mask, a_k represent the bits before scrambling, and $x_n, n = 0, 2, 3, \dots, 15$ is the receiver scrambling mask used in the procedure for the receiver chip, which is designed to be the binary antenna number in the proposed WIIC system. Although CRC is mainly applied for error checking, each receiver will be able to determine whether the received signal is sent to itself or other chips using CRC checking and descrambling. When channel coding and channel equalization correctly decode all the OFDM symbols, the procedure of receiver identification is processed as follows. If the CRC checking result is correct, the decoding chip will recognize itself as the correct receiver of the decoded bit stream; otherwise the

bit stream will be discarded by the receiving chip since it is transmitted to another chip with a different scrambling mask. However, this requires the channel decoding to correct all the errors caused by the WIIC channels, which may not always occur.

Thus, a packet header is much simpler, and will be used to perform the same technique described above. As a result, in the final version of the proposed WIIC system in the dissertation, scrambling has been removed from the transmitter block diagram while the packet header is included. Packet header will be discussed in Section 3.8.

3.3.2 Interleaving [46]

In the proposed WIIC system, as there will be more than two transceivers, the same bandwidth will be allocated to different sub-channels between chips, for spectrum reuse purposes. For example, as shown in Figure 3.3, in a four-chip WIIC system, the same frequency band (f_1) will be allocated to both Channels 12 and 34, which indicate the communications between Chips 1 and 2, and the transmissions from Chips 3 and 4, and so on. This approach will increase the spectrum utilization, and it will cause interference as well.

Interleaving technology is usually employed to deal with the burst interference from the channels. Interleaving can improve the performance of FEC by providing frequency diversity, in other words, interleaving the same data across separated subcarriers in OFDM, to mitigate frequency-selective fading or narrowband interference. Interleaving is the procedure to scatter the positions of data and redundant bits so that the burst errors from the channels will be less possible to influence an entire group of data bits and redundant bits.

The interleaving procedure is described as follows. For a block interleaver, the coded data bits are written by rows into a matrix with a fixed number of columns, optionally exchanging some columns with others, and read out by columns. If the last row of the interleaving matrix cannot be filled out with the coded data bits, the remaining positions will be filled by zeros.

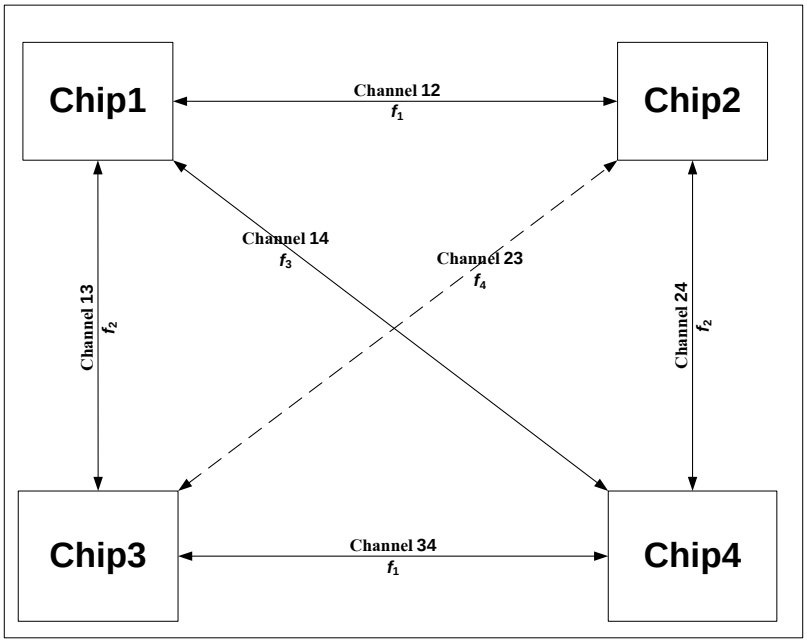


Figure 3.3 Four-chip WIIC system example.

The formats of interleavers include rectangular interleavers, convolutional interleavers, random interleavers, pseudo-random interleavers, and contention-free quadratic permutation polynomial (QPP) interleavers.

The QPP is frequently used in mobile communications. For the systems using convolutional coding, the output coded data is usually in several bit streams. With 1/3 TBCC, the input of the QPP is given by three serial bit streams, and the block diagram of QPP is shown in Figure 3.4.

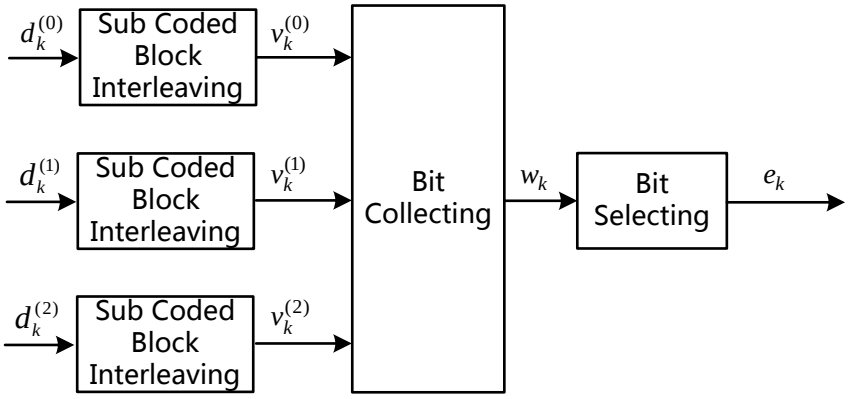


Figure 3.4 Block diagram of QPP interleaving.

In Figure 3.4, $d_k^{(i)}, (i = 0,1,2)$ is the *kth* output bit from the *ith* channel coding output bit stream. Each bit stream, called a sub coded block, will be interleaved separately, and the interleaved bits will be collected together. The blocks of bit collecting and selecting are collectively termed rate matching. These procedures can add zero bits so as to match the desired FFT/IFFT points.

In the proposed WIIC system, the interference channels are transmitting high speed signals, which are almost continuous. However, as interleaving primarily deals with burst interference, in other words discontinuous interference, it cannot highly eliminate continuous interference. Since interleaving cannot contribute much performance improvement for the system, interleaving has been removed in the process.

3.4 Modulation [22, 46]

Modulation of a communication system can increase the data rate in a given bandwidth when using high order modulation methods such as the Quadrature Phase-Shift Keying (QPSK), 8 Phase-Shift Keying (8PSK), and Quadrature Amplitude Modulation (QAM). QPSK and QAM are widely used in modern wireless and mobile communication systems. Although OFDM itself is a modulation method, BPSK, QPSK,

QAM and other modulation methods can still be implemented in the system modulation block for each subcarrier. In severe channel conditions, the OFDM modulation type is often BPSK as this modulation method achieves better Bit Error Rate (BER) performance than higher order techniques for a given SNR, otherwise, OFDM tends to employ higher order modulation methods to enable higher data rate and better spectrum utilization.

3.4.1 BPSK [22, 46]

The BPSK signal is represented by:

$$s_k(t) = \sqrt{\frac{2E_b}{T_b}} h_t(t - nT_s)\cos\left(2\pi f_c t + \pi(1-n)\right), n = 0, 1,\ kT_b < t < (k+1)T_b \quad (3.2)$$

where $s_k(t)$ is the *kth* bit of the BPSK signal, E_b is the energy of one bit where one BPSK symbol represents one bit, T_b is the time duration of a BPSK symbol, f_c represents the carrier frequency, and *n* is the data bit from the output of the functional blocks scrambling and interleaving. When the communication connections between the receiver and transmitter have not been set up, BPSK is usually a good choice as a default modulation method for broadcasting and random access.

3.4.2 QPSK [46]

The general form of QPSK signal is given as follows

$$s_k(t) = \sqrt{\frac{2E_S}{T_S}} h_t(t - nT_s)\cos\left(2\pi f_c t + (2n-1)\frac{\pi}{4}\right), n = 0, 1, 2, 3, kT_b < t < (k+1)T_b \quad (3.3)$$

where E_S is the energy of one QPSK symbol where one QPSK symbol contains two data bits, T_S is the time duration of one QPSK symbol, which equals twice the bit duration, f_c represents the carrier frequency, and *n* represents one of four symbols, each of which is composed of two consequent bits that are the output of the scrambling and interleaving

functional block. These symbols are represented by decimal numbers- 0 for 00, 1 for 01, 2 for 10, and 3 for 11. The block diagram of QPSK modulation is shown in Figures 3.5.

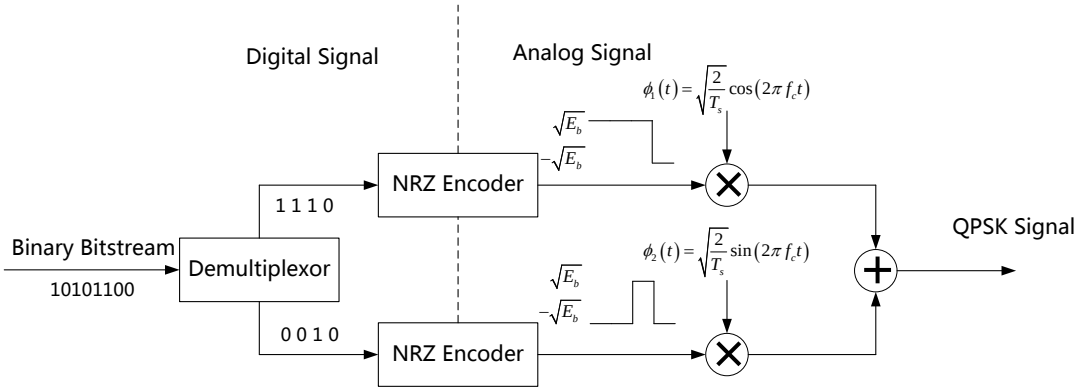


Figure 3.5 Block diagram of QPSK modulation [117].

3.4.3 QAM [46]

The QAM signal is represented, respectively, in the time domain and frequency domain as follows:

$$\begin{aligned} s(t) &= \sum_{n=-\infty}^{\infty}[v_c(n)h_t(t-nT_s)\cos(2\pi f_0 t) - v_s(n)h_t(t-nT_s)\sin(2\pi f_0 t)] \\ &= I(t)\cos(2\pi f_0 t) + Q(t)\sin(2\pi f_0 t) \end{aligned} \quad (3.4)$$

$$S(f) = \frac{1}{2}[M_I(f-f_0) + M_I(f+f_0)] + \frac{j}{2}\left[M_Q(f-f_0) + M_Q(f+f_0)\right] \quad (3.5)$$

where $v_c(n)$ and $v_s(n)$ are real and imaginary parts of a complex number that represent consecutive $\sqrt{X}$ input bits in XQAM. Take 16QAM as an example, '0000', '0001', '0010', '0011', and '0100' will be modulated to $v_c(n) + jv_s(n)$ as $-3+3i$, $-3+i$, $-3-3i$, $-3-i$, and $-1+3i$, respectively, where $j=\sqrt{-1}$. $h_t(t)$ is the impulse response of the modulation filter, $I(t)$ and $Q(t)$ are the time domain signals of the real and imaginary parts passed through the modulation filter, and $S(f)$, $M_I(f)$, and $M_Q(f)$ are the Fourier Transforms of $s(t)$, $I(t)$, $Q(t)$ respectively.

The modulation block diagram of QAM is shown in Figure 3.6.

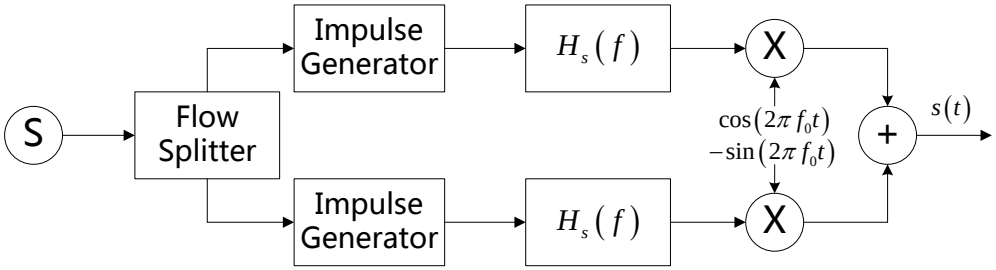


Figure 3.6 Block diagram of QAM modulation [117].

In order to minimize the bit error rate, on the constellation of 16QAM modulation, each constellation point will be only one-bit different to other constellation points next to it, i.e., the Gray Code is used. As a result, the error will be limited to one bit if the received QAM symbol at the receiver is estimated as another constellation point next to the constellation point on the transmitter.

In the WIIC research in this dissertation, the modulation method is initially chosen to be QPSK to validate the designed system and channels, and in the full system and channel investigation, both QPSK and 16QAM are available in MATLAB implementation.

3.5 Reference Signal Generation [76-80]

Channel sounding with reference signal (RS), channel estimation and channel equalization can improve the performance of the system greatly. RSs are sent from the transmitter and the receiver can employ channel estimation to extract an approximation of the frequency response by comparing the received RS and local generated RS. Channel equalization can compensate for errors caused by the channels by using the channel estimation results.

A receiver compares the received RS and those RS generated locally to obtain the Channel State Information (CSI) and Channel Quality Indicator (CQI), which can be

further used for channel equalization to improve the performance of the system. In wireless communications, the CSI refers to the properties of a communication channel, typically the channel gain. The CQI is a relative indicator, which carries information on how good the communication channel quality is. The CQI and CSI information describes in a gross manner the combined effect of, for example, scattering, fading, and power decay with distance.

In the WIIC system, Zadoff-Chu (ZC) sequences [56-58] are employed as the base sequence of RS. ZC sequences are constant amplitude zero autocorrelation (CAZAC) sequences.

- **ZC Sequences.** The waveforms for ZC sequences are as given as follows:

$$x_u(n) = e^{-j\frac{\pi un(n+1+2q)}{N_{ZC}}} \tag{3.6}$$

where $0 \leq n \leq N_{ZC}$, $0 \leq u \leq N_{ZC}$, $gcd(N_{ZC}, u) = 1$, $q \in Z$, and N_{ZC} is the length of the ZC sequence. ZC sequences are characterized with the following properties:

(A) ZC sequences are periodic, with the period to be N_{ZC}, when N_{ZC} is an odd number.

$$x_u(n + N_{ZC}) = x_u(n) \tag{3.7}$$

(B) If N_{ZC} is a prime number, the Discrete Fourier Transform (DFT) $X_u[k]$ of one ZC sequence is another ZC sequence represented by [76-80]:

$$X_u[k] = x_u^*(\tilde{k})X_u[0] \tag{3.8}$$

where $x_u^*(\tilde{k}) = e^{-j\frac{\pi u(\tilde{k}+1+2q)}{N_{ZC}}}$.

(C) The autocorrelation of a ZC sequence with a cyclically shifted version of itself is an impulse of weight N_{ZC} at the instant which corresponds with the cyclic shift.

$$R_x(n) = \sum_{k=0}^{N_{ZC}} x_u(k)x_u'(n+k) = \begin{cases} N_{ZC}, & n = l \\ 0, & else\ where \end{cases} \tag{3.9}$$

where $x'_u(n) = x_u(n+l)$, and $R_x(n)$ is the autocorrelation function of $x_u(n)$.

(D) The cross-correlation between two ZC sequences with the same prime length N_{ZC}, *i.e.*, with different u_1 and u_2, is a constant $\sqrt{N_{ZC}}$, which is relatively prime to $u_1 - u_2$.

$$R_{12}(n) = \sum_{k=0}^{N_{ZC}} x_{u_1}(k) x'_{u_2}(n+k) = \sqrt{N_{ZC}} \ for\ all\ n \qquad (3.10)$$

where $x_{u_1}(n) = e^{-j\frac{\pi u_1 n(n+1+2q)}{N_{ZC}}}$, and $x_{u_2}(n) = e^{-j\frac{\pi u_2 n(n+1+2q)}{N_{ZC}}}$ are two ZC sequences with the same length, $R_{12}(n)$ is the cross-relation function of $x_{u_1}(n)$ and $x_{u_2}(n)$.

As a comparison, other base sequence candidates for RS include the conventional Pseudo-Noise (PN) sequence, conventional CAZAC sequence, and M-sequence.

- **PN sequences.** One common PN sequence is defined as follows:

$$p(n) = e^{j\frac{\pi}{4}\varphi(n)} \qquad (3.11)$$

where the sequence $\varphi(n)$ is a complex random sequence defined as:

$$\varphi(n) = r_2(n) + jr_2(n) \qquad (3.12)$$

where $r_1(n)$ and $r_2(n)$ are the normally distributed pseudorandom numbers and $r_1(n), r_2(n) \sim N(0,1)$. In practice, $r_1(n)$ and $r_2(n)$ will be carefully quantized, the configuration of which will affect performance. In the comparison of Figures 3.9 and 3.10, the PN sequence is demonstrated in MATLAB with random sequences to see the correlation performance of a normal PN sequence.

- **Conventional CAZAC sequences.** The conventional CAZAC sequence is given by:

$$c(n) = e^{\frac{j2\pi k(n+n^2/2)}{N}} \qquad (3.13)$$

where *k* is an integer that is prime to the length of CAZAC sequence *N*.

- **M-Sequences.** A maximal length sequence (MLS) or M-Sequence is a type of pseudorandom binary sequence. An M-Sequence is generated by using a maximal-length linear feedback shift register. It is so called because the M-sequence is periodic has the longest period possible for a given shift register length. Practical applications for M-Sequence include channel estimation and generation of pseudo-random sequences, instead of purely random ones, in digital communication systems. M-Sequences are widely used in communication systems that employ direct-sequence spread spectrum and frequency-hopping spread spectrum transmission systems. In the efficient design of some Functional Magnetic Resonance Imaging (FMRI) experiments, M-Sequences have also been employed for better performance [115]. The block diagram for M-Sequence generation for a length-15 sequence is shown in Figure 3.7, where the adder in the figure represents a modulo-2 addition. The registers can be initialized to any states with the exception of the all-zero vector.

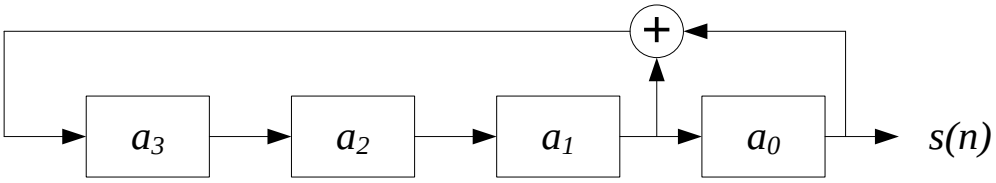


Figure 3.7 Block diagram for M-Sequence generation.

The comparison of the autocorrelation functions of 97 bits of PN, conventional CAZAC and ZC sequences is illustrated in Figure 3.8.

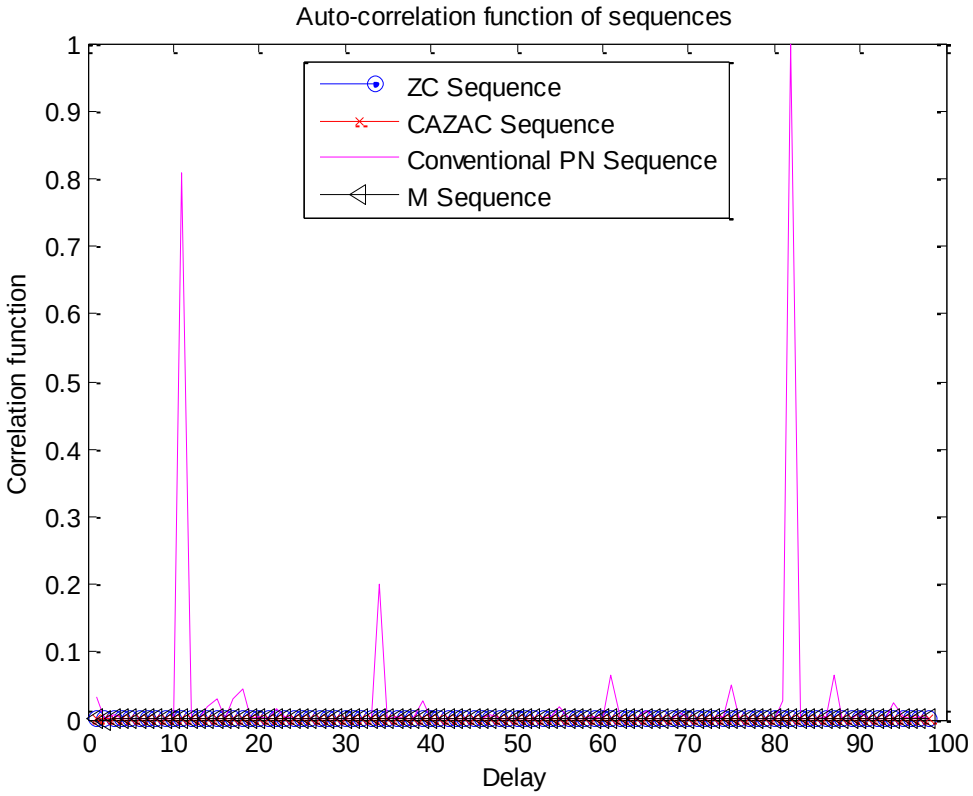


Figure 3.8 Auto-correlation functions of RS base-sequence candidates.

The pseudorandom numbers of PN sequence are generated by MATLAB. The comparison of the cross-correlation functions of PN, conventional CAZAC and ZC sequences is demonstrated in Figure 3.9. To have a better comparison to the auto-correlation function, the cross-correlation function has been defined with the same length as the autocorrelation function [85]:

$$R(n) = \frac{1}{N}\sum_m x(m)y(m+N) \qquad (3.14)$$

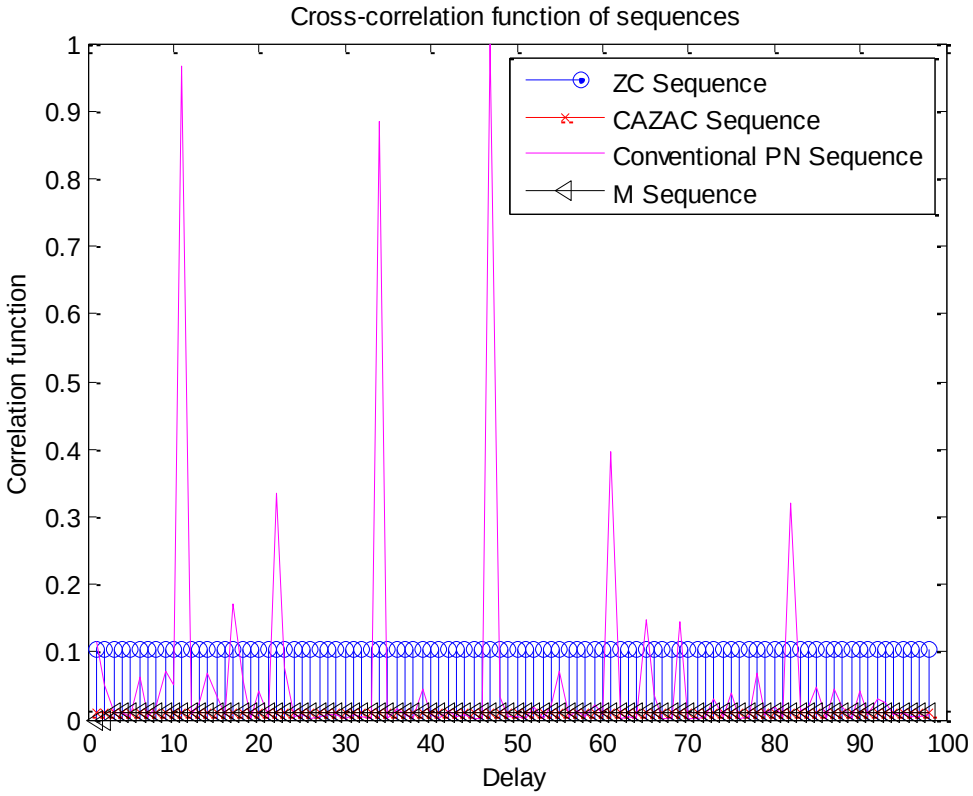


Figure 3.9 Cross-correlation functions of RS base-sequence candidates.

The correlation function simulation results for these sequences show that the ZC sequence has the best performance for both auto and cross-correlation properties among the RS base-sequence candidates. M-sequences and conventional CAZAC sequences have good autocorrelations, but cross-correlation is not as good as the ZC sequence. Therefore, in the proposed WIIC system, a 17-bit ZC sequence is employed as the RS base.

In order to simplify the receiving procedure of the proposed WIIC system, as the WIIC channel can be considered to be time-invariant (TI), the RS will be transmitted when the system powers on, and the channel estimation will be performed when the RS signal is received. The same channel estimation result will be used in the channel equalization process.

3.6 Multiple Input Multiple Output [46]

A system that employs MIMO technology can upgrade the reliability, which means that a lower BER can be obtained for the system under the same SNR. MIMO is able to increase the data rate by splitting one data stream into a number of layers and using precoding to separate the data stream layers to different antennas [59]. Also, MIMO systems separate interferers in space, and achieve a better Signal to Interference and Noise Ratio (SINR) by increasing the receiving power using beamforming. Except for beamforming, all MIMO techniques require inter-antenna-pair channels to be uncorrelated. In conventional macro-scale links, this is typically attained in non-line-of-sight (NLOS) channels via rich scattering over both the temporal and spatial angular domains. In LOS channels, MIMO gains can also be attained via careful design of the arrays as a function of link distance, array element separation, and spatial orientation [114].

MIMO works before the OFDM baseband signal processing schemes and splits data streams on to each layer and antenna. The block diagram of MIMO is shown in Figure 3.10. This is also adopted from the LTE communication system.

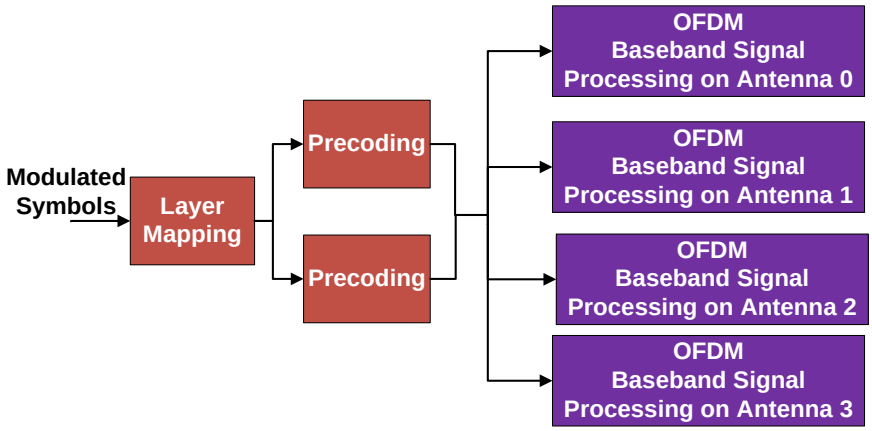


Figure 3.10 Block diagram of MIMO systems.

3.6.1 Layer Mapping [46, 66]

Layer Mapping basically splits one OFDM symbol stream into several OFDM symbol streams. Each split data stream is called a layer. The number of layers should be no greater than the number of antennas. For real-time processing, layer mapping can be expressed as:

$$s^i(n) = s(M(n-1)+i) \tag{3.15}$$

where $s(k)$ is the OFDM baseband signal processing output, $s^i(n)$ is the signal on *ith* layer, *n* is the index of the OFDM symbol in the time domain, $0 < n \leq M$, and *M* is the total number of bits on one layer.

3.6.2 Precoding [46, 81]

Precoding distributes the MIMO symbols by mapping them on all layers onto each antenna. All multi-antenna systems need precoding so as to support multi-layer transmission via a multi-antenna wireless system. The most significant advantage of precoding is that the receiver will be able to maximize the throughput with multiple receiving antennas for multi-layer signals. Precoding converts *M* layers of OFDM symbol streams to *N* streams, where *N* is equal to the number of antennas.

If a Digital Signal Processer (DSP) is included in a WIIC system, the main procedure of precoding is to multiply the *M* layer stream with the designed complex precoding matrix. The precoding matrices should be orthogonal matrices so that it would be simple enough to find their inverse matrices for the receiver to retrieve information from each receiving antenna.

3.6.3 Potential MIMO Applications in the Proposed WIIC System

MIMO can bring data rate increase and/or diversity for WIIC systems. However, in this dissertation, the simulation of the channel uses only one monopole antenna per transmitter. Therefore, in the channel analysis in this dissertation, SISO, rather than MIMO is selected. Only MIMO's spatial multiplexing is used for the calculation of the theoretical upper bound of the data rate used in the proposed future WIIC system, where the channels are simplified to be ideal, statistically identical, and uncorrelated. In the future work for WIIC, realistic MIMO model may be employed if it can bring spatial multiplexing gain or beamforming, without adding unacceptable burden on power, antenna array, PCB area, and other costs.

3.7 Cyclic Prefix [46]

Cyclic Prefix (CP) is often used in OFDM systems to deal with channel dispersion. Considering wireless signals may be reflected, diffracted and scattered in the PCB area, the timing issues would include the one-way time delay (One-Way TD) as a result of the distance between chips, delay spread (DS) due to multi-path effect, and the clock timing problems. How CP in OFDM systems solve the former two issues are shown in Figure 3.11.

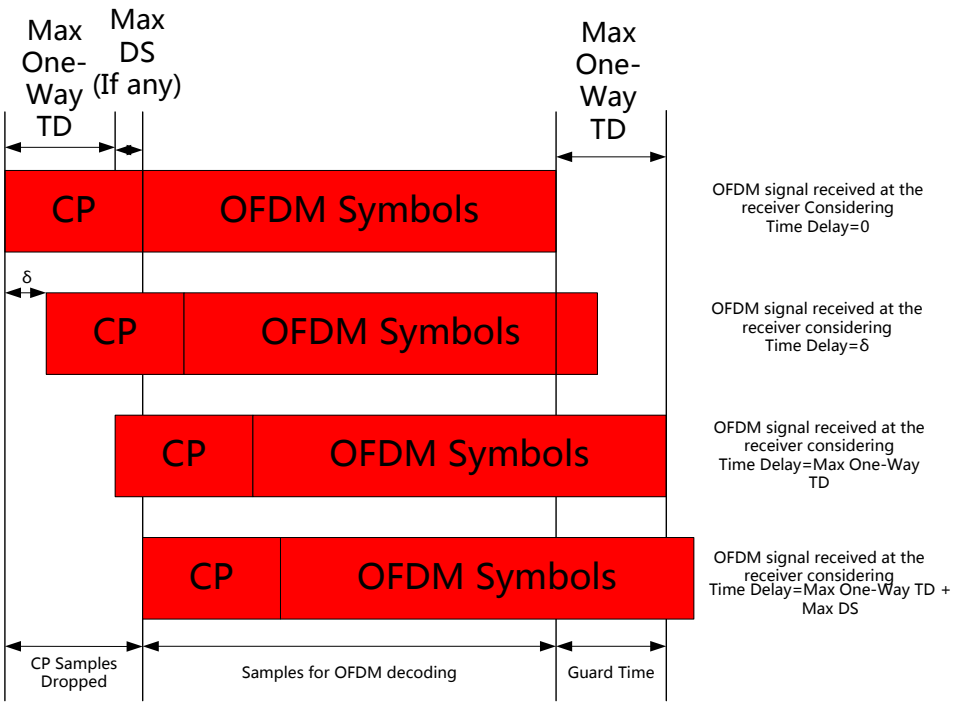


Figure 3.11 Cyclic Prefix and timing issues in the WIIC system [116].

In the designed WIIC system, the one way time delay is approximately 102.67 ps, while the symbol duration is about 34.14 μs, which are further analyzed in detail in Section 5.7.1 **B)** and **D)**. As the time delay between chips is relatively small compared to the transmission block duration, in the WIIC situation, the CP implementation includes a small length of CP block (20 CP points vs. 1024 OFDM blocks) to minimize the added processing delay brought by CP insertion.

3.8 Packet Header Insertion

For the purpose of chip identification, a packet header has been included in the system. As a server system usually has no more than 10 CPUs, seven bits of packet header for both transmitter and receiver identifications have been reserved for future use. Packet header is inserted as the first seven bits in the front of the input data, and the data

stream with the packet header will be processed with CRC, channel coding, symbol mapping, OFDM, and CP insertion signaling.

3.9 Modified Block Diagram for the Transmitter

With consideration of implementation cost and complexity of design, the WIIC transmitter block diagram has been modified as displayed in Figure 3.12.

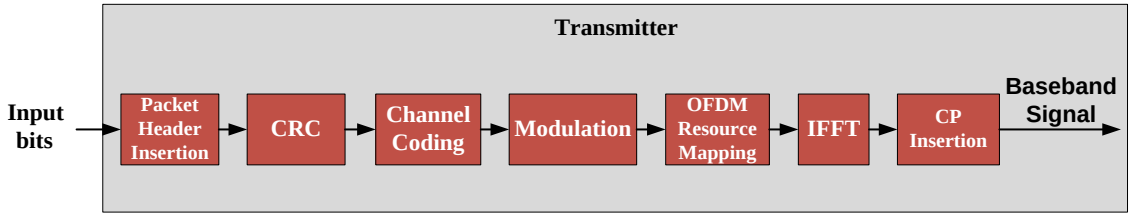


Figure 3.12 Revised block diagram for the transmitter.

In the revised block diagram of the proposed WIIC transmitter, the following changes have been made in comparison to the one shown in Figure 3.1:

- The block of interleaving has been removed as it is not necessary for the WIIC channels.
- Scrambling has been also removed and will be replaced by an optional packet header before CRC redundant bits generation. The transmitter and receiver chip ID (or IDs for multi-cast/broadcast) are included in the packet header if there are more than two CPUs in the WIIC system.
- MIMO blocks, including layer mapping and precoding, have been removed due to their high power consumption, and the lack of substantial benefit in the WIIC channels. In future work, a careful multi-antenna array design could show worthwhile MIMO benefits.
- RS generation, channel sounding, and channel estimation will be performed at the moment when the system is powered on.

CHAPTER 4

WIIC SYSTEM RECEIVER DESIGN

The receiver of the WIIC system consists of the functional blocks of CP removal, OFDM symbol demapping, channel estimation & equalization, demodulation, channel decoding, and CRC checking. This chapter is primarily going to focus on design of the WIIC system receiver.

4.1 Receiver System Block Diagram [66]

The receiver block diagram is shown in Figure 4.1. The features of all the functional blocks are analyzed and designed in this chapter. The preliminary implementation of the WIIC system in an AWGN channel does not include the blocks of channel decoding, estimation and equalization. Afterwards, these three blocks are then added and integrated into a full WIIC system and channel analysis with all three different channels, including AWGN, the wired PCB, and the designed WIIC channels. After CRC checking, the bit error rate (BER) versus signal-noise ratio (SNR) is obtained by comparing the decoded bits with the delayed original data.

When the system is first initialized, a RS sent by the WIIC transmitter will be compared to the local RS signal to estimate the channel transfer function. The extracted WIIC channel transfer function will be used to equalize the received signals.

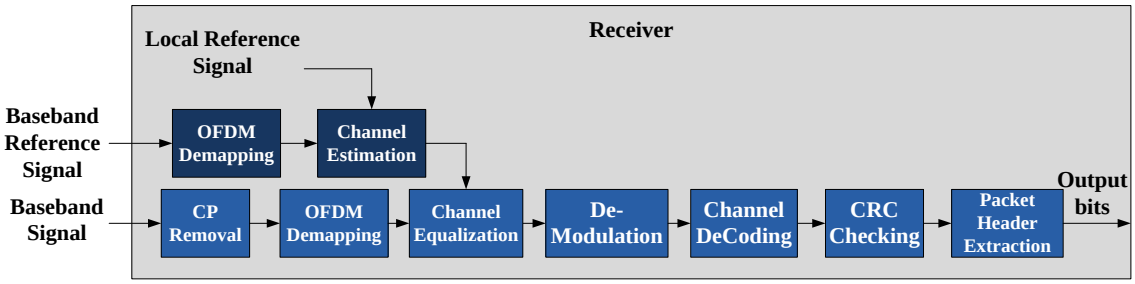


Figure 4.1 Block diagram of the WIIC receiver.

4.2 OFDM Baseband Signal Processing [22, 29, 46, 66]

In reality, received OFDM signals will first go through an antenna, a Low-Noise Amplifier (LNA), a down converter and a Low-Pass Filter (LPF) to become baseband signals. The antenna model is integrated in the channel model. Besides, a perfect LPF and a mathematical Digital Down Converter (DDC) at the transmitter are used in the system validation; the gains of LNA at the receiver and Power Amplifier (PA) at the transmitter are counted in the link budget and are combined with other gains in SNR and BER analysis.

The OFDM baseband signal processing procedure includes OFDM signal demodulation, CP removal, FFT, and OFDM symbol demapping. After the baseband signal processing, the receiver of the WIIC system will recover the original OFDM symbols in sequence.

4.3 Channel Estimation and Channel Equalization [46, 76-80]

Various communication systems always make efforts to sound and estimate the transmission channels using different channel estimation methods. With the channel estimation results a receiver system is able to equalize the channel response, and via the MA scheme it could utilize channels by avoiding portions of the frequency band with higher loss or fading [62]. Channel estimation could also include SNR estimation, and it

can enable selection of proper modulation method to balance data rate and BER performance. In this dissertation, the channel equalization is used to compensate each OFDM subcarrier by a single complex multiplication of the reciprocal estimated channel transfer function.

4.3.1 Channel Estimation [46, 76-80]

Channel estimation methods usually include Linear Interpolation (LI) Estimation, IFFT Estimation, Least Square (LS) Estimation, Minimum Mean Squared Error (MMSE) Estimation, etc. An analysis of these techniques is to use the Truncated Normalized Mean Square Error (*TNMSE*) to evaluate these Channel Estimation methods [50]. *TNMSE* is defined as follows:

$$TNMSE_{\widehat{H}} = \frac{Ttr\{C_{\widehat{H}}\}}{Ttr\{F_L C_h F_L^H\}} \tag{4.1}$$

where

- Normalized Mean Square Error (NMSE) is the normalized average of the square of the error of each channel estimation method compared to the actual value of channel state, *i.e.*, the impact of the mistake of one channel estimation method compared to the whole Channel Transfer Function (CTF);
- Ttr{·} is the truncated trace operation, where the truncation is such that only the used subcarriers are included [50];
- $C_{\widehat{H}}$ is the error covariance matrix for the estimated CTF, $\widehat{H} = H + \widetilde{H}$;
- $\widetilde{H}$ is the error of the estimation related to the real transfer function;
- F_L is the matrix obtained by taking the DFT of the true CTF $H = F_L h$;
- h is the impulse response of the channel;

- $C_h = E\{hh^H\}$ is the channel covariance matrix, and $\{\cdot\}^H$ is the Hermitian operation; and finally
- $E\{\cdot\}$ is the mathematical expectation operator.

Thus, $F_L C_h F_L^H$ is the covariance matrix of the true CTF. The better the channel estimation, the smaller *TNMSE* will be.

In order to analyze the performance for the estimation methods, these channel estimation approaches are assessed for the transfer function of the designed WIIC channel with the absorber layers, which is further discussed in Chapter 5. The corresponding *TNMSE* result for the comparison is displayed in Figure 4.2.

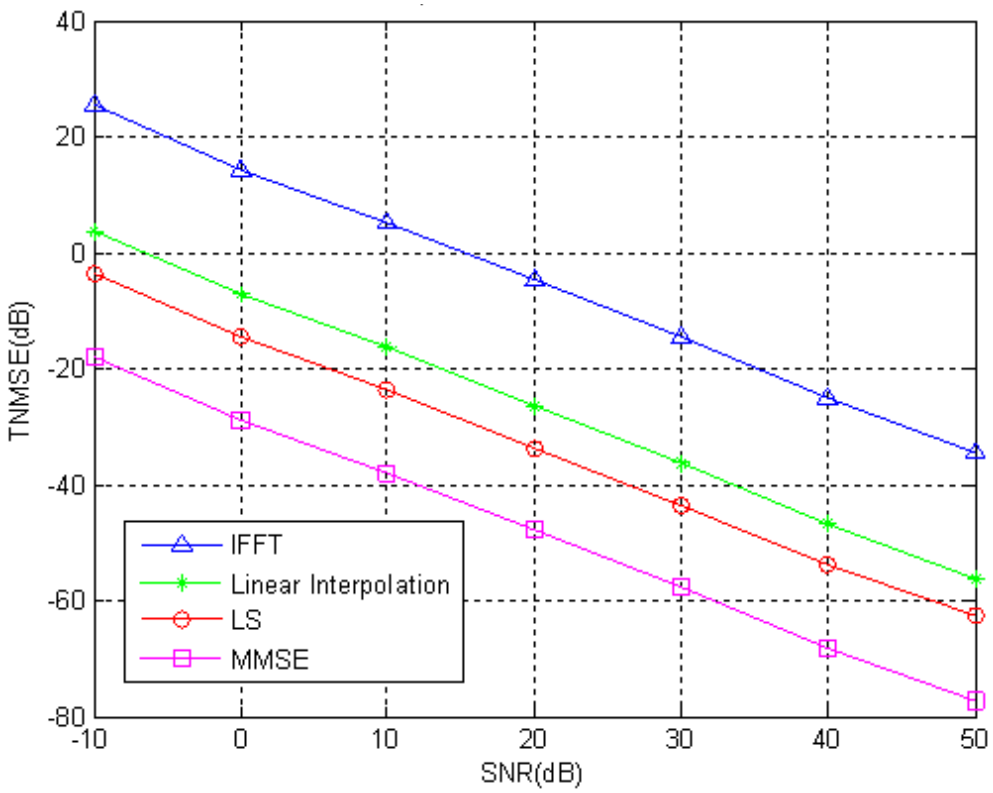


Figure 4.2 Comparison of channel estimation methods in the designed WIIC channel.

The simulation result shows that MMSE is the best channel estimation scheme among the four approaches for the designed WIIC channel. As channel estimation will

only be performed once in the proposed WIIC system when the system powers up, MMSE is chosen to be the channel estimation method as it should have the best performance.

4.3.2 Channel Equalization [76-80]

Channel equalization is a procedure in the receiver of a communication system. In the OFDM systems used to un-do the distorting effects of the channel. In OFDM systems, it employs the estimated channel transfer function obtained from the channel estimation. It equalizes every subcarrier by multiplying the signals obtained from the output of the OFDM symbol demapping block with the reciprocal of the estimated complex transfer function. This is known as zero-forcing equalization. The OFDM symbol demapping is abbreviated as deOFDM block in the rest of the dissertation.

4.4 OFDM Symbol Decoding [46, 76-80]

Demodulation produces estimated transmitted symbols from the input RF waveform, and channel decoding can correct some errors in the received signals.

4.4.1 Demodulation and Constellation [46, 76-80]

At the transmitter, the constellation for modulated signals is perfectly shaped to the designed constellation points of BPSK, QPSK, Offset Quadrature Phase-Shift Keying (OQPSK), and QAM, and so forth. However, at the receiver, affected by the channel, noise, and possibly interference the constellation becomes irregular. The channel behavior can be qualitatively judged by observing the constellation at the receiver.

4.4.2 Decoding [46, 62, 82]

As the encoding method employs convolutional coding, accordingly, Viterbi decoding technique is a usual choice for the decoder. For the 1/3 code rate TBCC, although the receiver does not have the preset values of the encoding registers, the

convolutional decoder can use tail-biting property to determine starting/ending stages. As a result, the Wrap-Around Viterbi Algorithm (WAVA) is suitable for the WIIC receiver system. The Flow Chart of WAVA is shown in Figure 4.3.

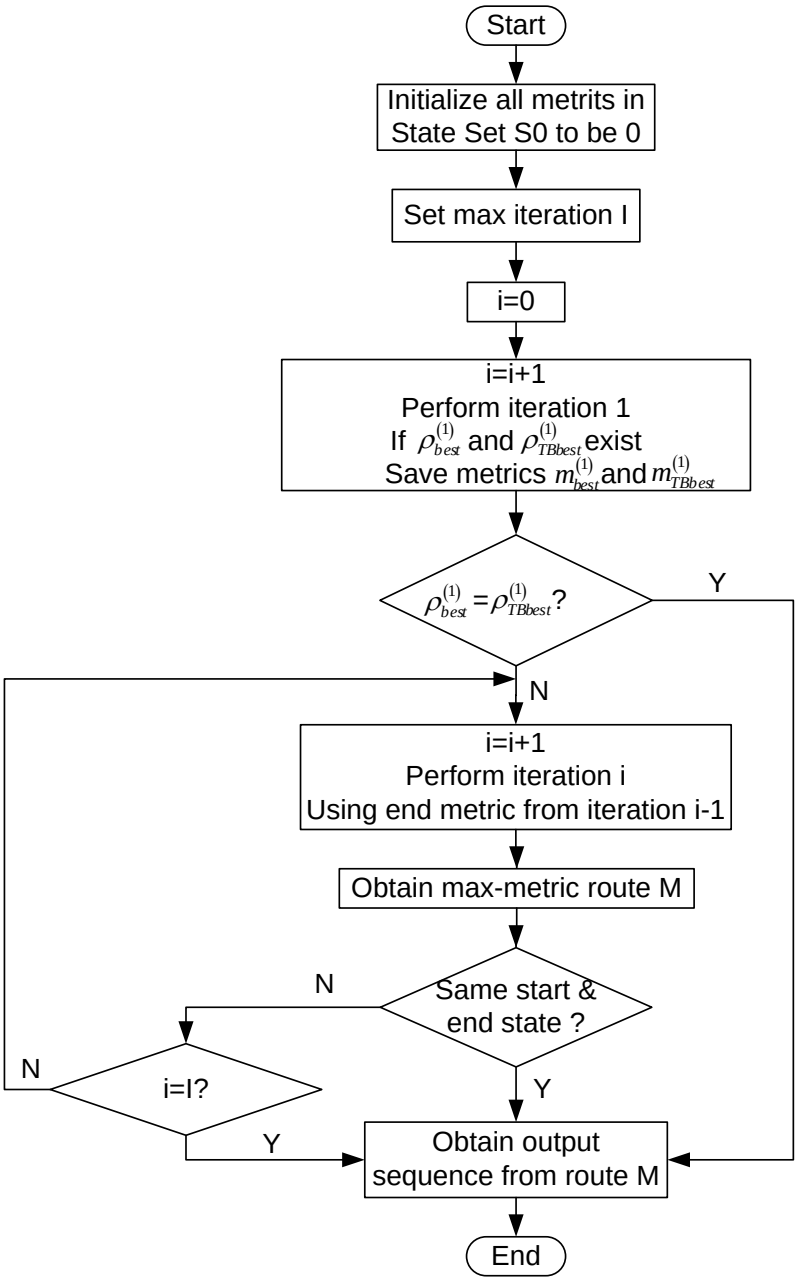


Figure 4.3 Flow chart of WAVA decoding, where the metric indicates the likelihood metric for a decoding route.

In the flow chart, the “metric” is defined as the likelihood metric for a decoding route, which is commonly used in Viterbi algorithms. When the maximum number of iterations (I) increases, the performance of WAVA improves, at the expense of a larger decoding delay and energy consumption. A comparison of the BER performance as a function of the maximum number of iterations for the AWGN channel with QPSK modulation is given in Figure 4.4 [62].

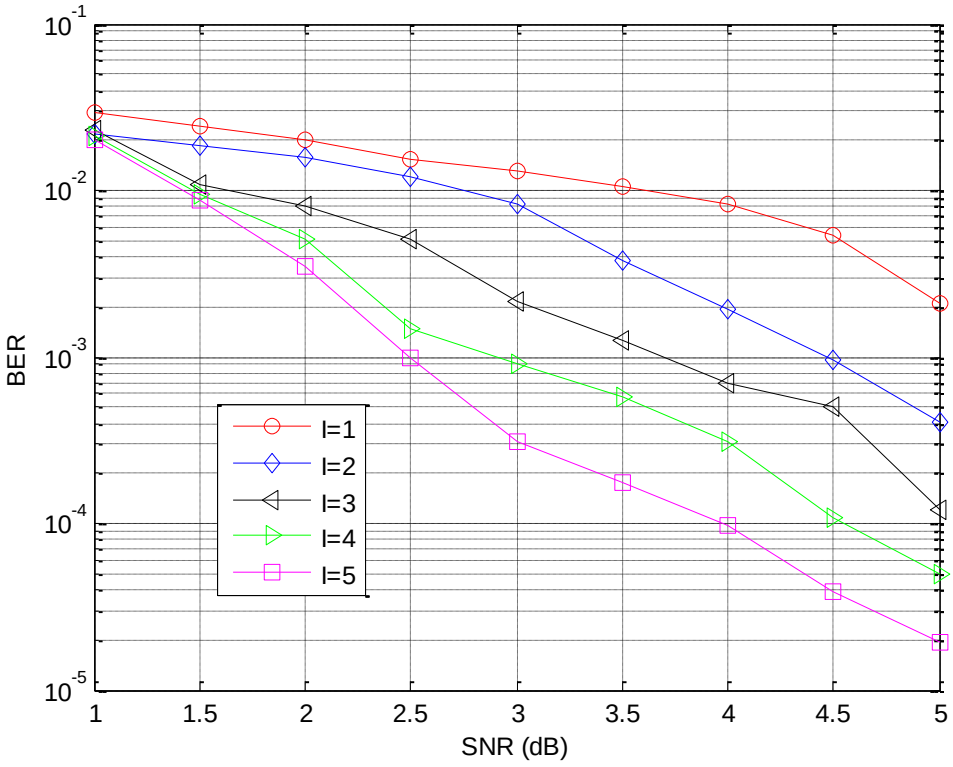


Figure 4.4 Comparison of different maximum iterations in WAVA decoding.

As seen in Figure 4.4, when SNR or maximum iteration increases, better BER performance is achieved, but the complexity, decoding delay and energy consumption also increase accordingly. The simulation result for WAVA decoding only analyzes the iterations with acceptable decoding delay. In the proposed WIIC system design, in order

to balance the performance and the decoding delay, the maximum number of iterations is chosen as $I = 5$.

CHAPTER 5

WIIC SYSTEM CHANNEL MODELING AND DESIGN

There are a variety of channel models to be chosen for validation of the proposed WIIC system. The Additive White Gaussian Noise (AWGN) channel is a simple idealized channel model without attenuation and fading, and it includes only additive noise in the channel. To further consider multipath effect in a WIIC system, a more realistic and hence complicated channel model needs to be analyzed and simulated.

5.1 WIIC Channel Models [52, 63-65]

In the research, the AWGN channel is first built in to an initially developed WIIC simulation to establish proper operation of all the functional blocks of the WIIC transceivers, by obtaining Bit Error Ratio (BER) versus Signal to Noise Ratio (SNR) results that can be compared with known theoretical results. The noise in the AWGN channel satisfies a normal (or Gaussian) distribution, which is independent of the signal, with expected value 0 and variance N_0. The double sided power spectral density (PSD) of the AWGN channel is equal to $N_0/2$. The noise power equals $P_N = N_0 \cdot B$, where B is the RX bandwidth in *Hz*. The noise power spectral density N_0 is usually normalized to 1. The transmitted bit energy is given as $E_b = N_0 \cdot \gamma_b = \gamma_b$,where γ_b is the linear form of the bit energy to noise density ratio.

Second, a WIIC channel with two monopoles and a parallel metal plate waveguide is designed, which not only serves as the ground planes but also reduces millimeter wave leakage to other wireless (or wired) channels outside the WIIC system.

Furthermore, a metamaterial EBG absorber unit operating in 60 GHz band is designed to absorb electromagnetic waves for minimizing the multipath effect and further reducing signal leakage. The WIIC transceivers are placed on the top layer of the WIIC PCB, and the antennas are constructed as vias through the ground plane, with the EBG absorbing walls on the borders on the top and bottom layers of the channel. The S-Parameters, impulse response and transfer function of the WIIC system for these physical models are then extracted.

Other than using the existing theoretical channel models in the simulation, a physical WIIC channel is established and simulated in HFSS and MATLAB to access the system performance. Herein the WIIC channel of 20 GHz bandwidth centered at 60 GHz is designed and analyzed.

A simplified WIIC channel model is first designed with two parallel plates as the ground planes in High Frequency Structural Simulator ® (HFSS). After that, a metamaterial based Electromagnetic Band Gap (EBG) absorber unit is designed and added to the WIIC channel to build up the top and bottom layers of the PCB board. The diagram of the WIIC channel structure is shown in Figure 5.1.

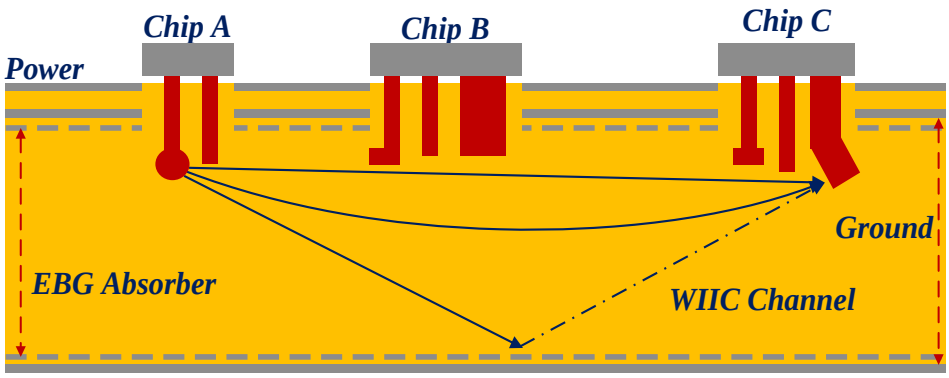


Figure 5.1 WIIC channel concept with EBG absorbers.

With this physical structure, the impulse responses and transfer functions for the WIIC channel, as well as those for the simulated and measured wired PCB channels are extracted from the corresponding S-Parameters.

In order to compare the WIIC system to conventional approaches, a wired PCB channel consisting of microstrip and strip lines, vias, through hole pins, and connectors, is analyzed, and the Time Domain Reflectometry (TDR) and Time Domain Transmission (TDT) of the wired PCB channel are measured. Also, the microstrips, strip lines, and the via and the through hole pins are simulated in HFSS to extract S-Parameters. Those components with the connector's S-Parameters provided by its vendor, are connected in series in Advanced Design System® (ADS) and then used to obtain the total channel S-Parameters, and TDR/TDT signals of the wired PCB channel. The measured TDT and TDR responses are also converted to S-Parameters in order to perform a comparison to the designed WIIC channel.

5.2 WIIC Channel Model Design with a Parallel Plate Waveguide

A very first version of the WIIC channel model with a parallel plate waveguide is designed in HFSS. Then, an improved version with two monopole micro-antennas and a propagation channel bounded by a pair of the metamaterial absorber layers has been

developed and studied in HFSS [52]. The parallel plate waveguide model is filled with the dielectric substrate of FR4, which is imbedded between the parallel metal plates. The metal plates form the ground planes and microwave shields. Two micro-antennas represent the antennas for the transceiver chips of the proposed WIIC system. The dimension of the WIIC channel is 80×60×3.072 *mm*, and the dielectric substrate material is FR4 with the dielectric constant of $\varepsilon_r = 4.4$ and loss tangent of $\tan\delta = 0.02$,. The thickness of the parallel copper plate is 0.018 *mm*, and the thickness of the dielectric substrate is 3.036 *mm*. The distance between two chip pin antennas is 35.8 *mm*. The pin antennas are embedded in the dielectric, which are directly connected to the chip pins and pass through the ground plane of top PCB layer as seen from Figure 5.1. In the HFSS simulation, a coper pin prober protruding through the top layer is set to be the coaxial cables served as the wave port of the design. The designed WIIC channel is shown in Figure 5.2.

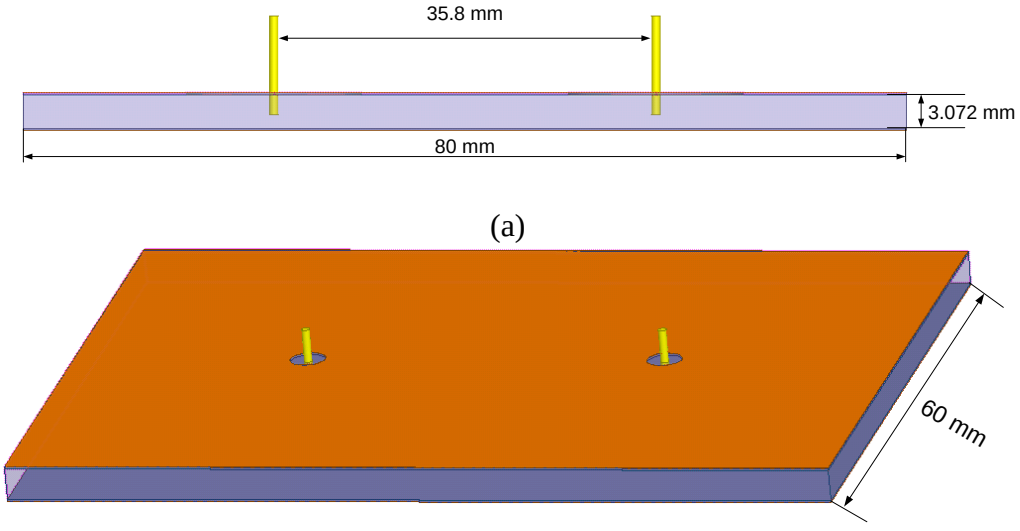


Figure 5.2 Monopole antennas and propagation channel model bounded by a pair of parallel plates. (a) Side view and (b) the geometry of the WIIC channel.

The derived S-Parameters between a pair of chip ports are displayed in Figure 5.3.

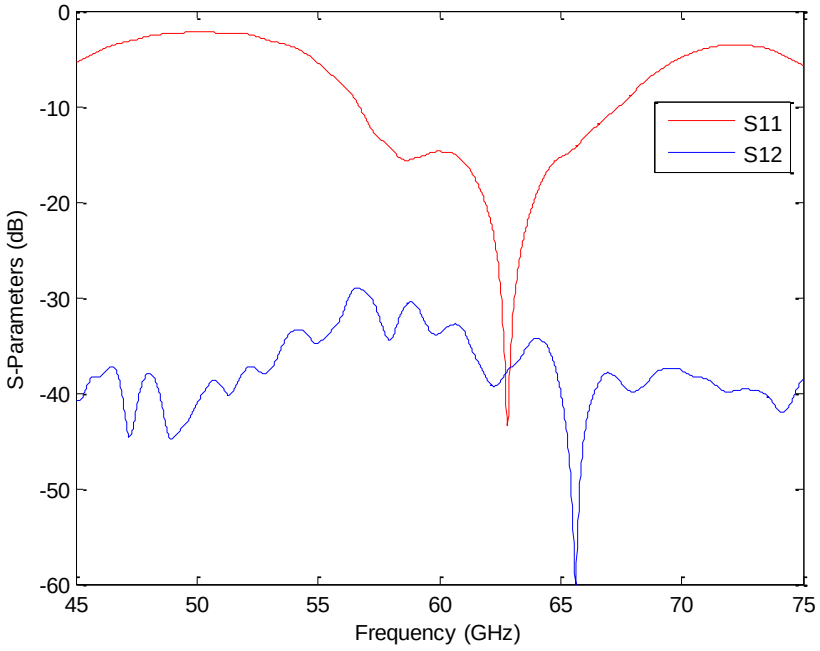


Figure 5.3 Extracted S-Parameters for the parallel plate WIIC channel model.

In this initial WIIC channel design, the return loss (S_{11}) significantly drops at the frequency of 62.8 GHz, and the insertion loss (S_{21}) essentially exhibits a null at the neighborhood around 66 GHz, which is a clear limitation of the channel. The *10-dB* bandwidth of S_{11} for the channel is 56.7-67.4 GHz. This channel is not preferable because of the electromagnetic wave resonance in the vertical direction due to the hard truncation of the metal walls. A potential problem is that the signal resonances can directly lead to heat generation, which is certainly an unwanted consequence. As a result, a much better idea is to design a pair of EBG absorber layers to replace the ground planes to absorb electromagnetic energy and to eliminate the potential heating problem. Another disadvantage is that within the bandwidth, S_{21} varies significantly from approximately -60 to -30 dB. Even though the effective bandwidth is limited to 57-65 GHz, to avoid the null of S_{21} at about 66 GHz, the insertion loss for the designed channel ranges from 29 dB to -

40 dB, which is a great amplitude variation. Therefore, equalization should be mandatorily applied in the corresponding WIIC system to reach proper BER performance.

5.3 Metamaterial Based Absorber Design and Equivalent Circuit Extraction [63-65]

5.3.1 Metamaterial Based Absorber Design

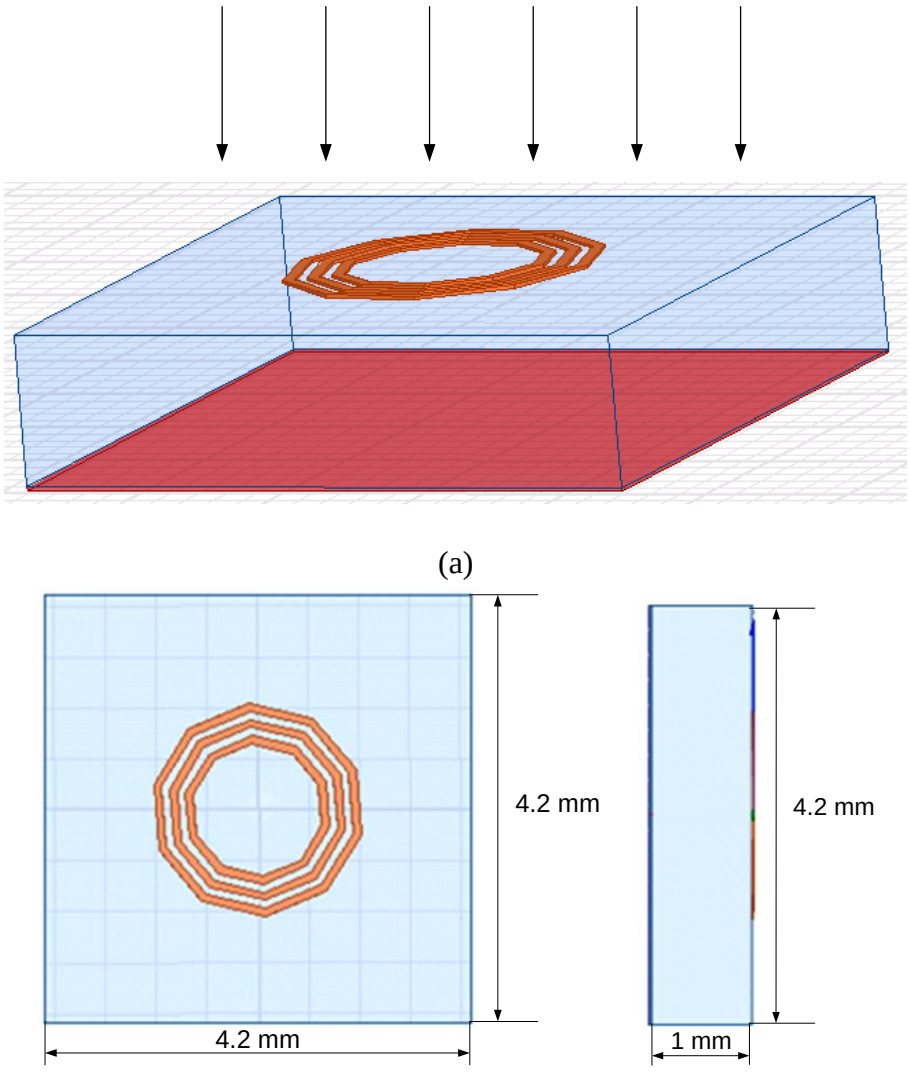
In order to prevent EM wave leakage, a metamaterial-based EBG absorber unit that operates at the center frequency of 60 GHz is designed and then applied on the top and bottom layers of the WIIC channels. The absorber will be shown to be one of the most essential components of the designed WIIC channel model [63-65]. The absorber will invariably deform the antenna patterns, when the absorber is embedded into the channel environment. The simulated S-Parameters model will automatically account for the impact from the absorber, propagation channel, and the original antenna radiation patterns.

In order to describe the performance of the proposed microwave absorber, the concept of absorbtance is introduced [63]. Absorbtance is a measurement of the effectiveness of the electromagnetic wave absorbing ability, and is defined as:

$$A(f) = 1 - |S_{11}|^2 - |S_{21}|^2 \tag{5.1}$$

, where S_{11} and S_{21} are the return and insertion losses of the S-Parameters for the absorber, which are extracted from a normal electromagnetic wave incidence onto the absorber unit.

The bandwidth of the absorbers is calculated as the frequency band with the absorbtance being greater than 90%. In order to make the frequency band centered at 60 GHz, the absorber unit cell has been tuned, and the designed absorber unit is shown in Figure 5.4.



(a)

(b) (c)

Figure 5.4 Absorber unit cell. (a) Overview, (b) top view, and (c) side view.

The proposed WIIC channel is built within a PCB board with the dielectric substrate made by Foam. The substrate is characterized by the dielectric constant of $\varepsilon_r = 1.0$. The dimensions of the designed absorber unit are 4.2×4.2×1 mm. The absorber unit consists of three decagon resistive loops, substrate, and a reference plane so as to achieve a broadband frequency responses centered at 60 GHz. As the absorbtance is determined by the dimensions, and the dimensions has been tuned to a boarder frequency band centered at 60 GHz as follows. The thickness of the metal is 0.02 *mm*, the width of

the loop traces is 0.08 *mm*, the edge-to-edge spacing among loops is 0.08 *mm*, and the side lengths of three loops are 0.3245, 0.2503, and 0.2256 *mm*.

The absorbtance of the designed three-layer decagon absorber unit is displayed in Figure 5.5. Table 5.1 summarizes a comparison between the proposed EBG absorber unit and prior designs of electromagnetic absorbers from the literature.

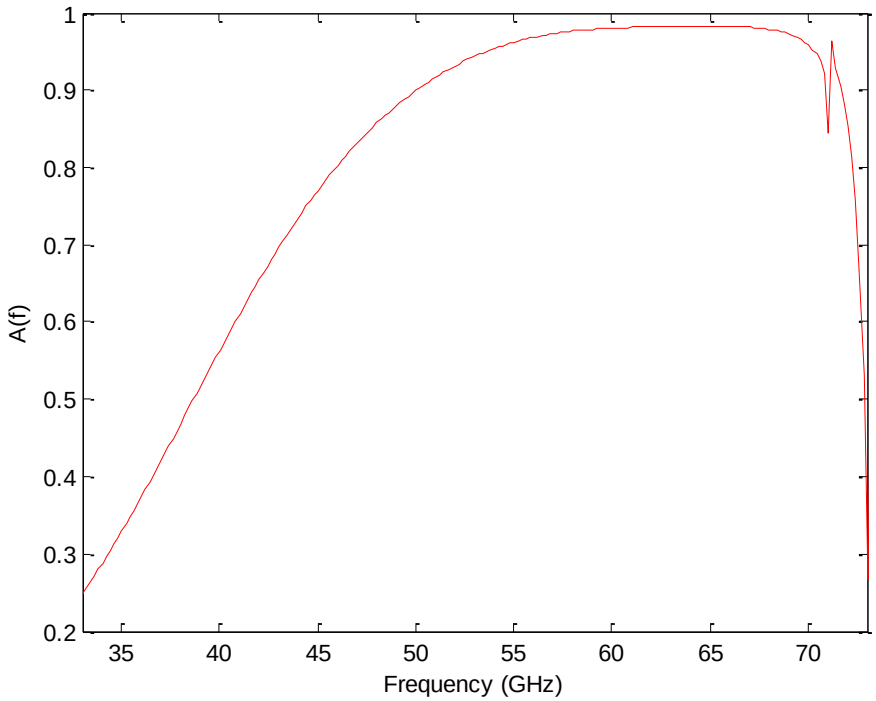


Figure 5.5 Absorbtance of the designed metamaterial absorber vs. frequency.

As demonstrated in Figure 5.5 and Table 5.1, in this design, both the central frequency (60 GHz) and the absolute bandwidth (50.02~70.22 GHz) are the highest among all the recent EM wave absorbers. The EBG metamaterial absorber is mainly designed to absorb the normal components of electromagnetic waves.

Table 5.1 Parameters of EBG absorber designs

Central Frequency (GHz)	Bandwidth (GHz)	No. of Dielectric Layers	Dielectric	Unit Dimension (mm)	Paper
4.91	4.79-5.04	7	FR-4	10.2×10.2×0.9	[67]
14.68	8.37-21	8	Teflon, RogersTMM4	6.4×6.4×3.65	[68]
17.33	12.38-22.28	3	FR-4	29.6×29.6×1.6	[70]
22	4-40	4	CIFs, epoxy resin	20×20×3.7	[71]
10.87	6.79-14.96	5	FR-4, air	11.1×10×0.4	[72]
60.52	**50.02-70.82**	**3**	**Foam**	**4.2×4.2×1**	**This Design**

5.3.2 Equivalent Circuits of the Absorber Unit

To better understand the absorption mechanism for the EBG absorber and to obtain a fast simulation model of the absorber, its equivalent circuit has been developed in this section, by using the transmission line models [5, 6] as given in Figure 5.6. Although the EBG absorber has been designed and simulated in the full-wave Maxwell solver HFSS, the equivalent circuit has been developed in ADS for better understanding of the concept of the absorber and fast evaluation and design of the physical structure for different absorber applications.

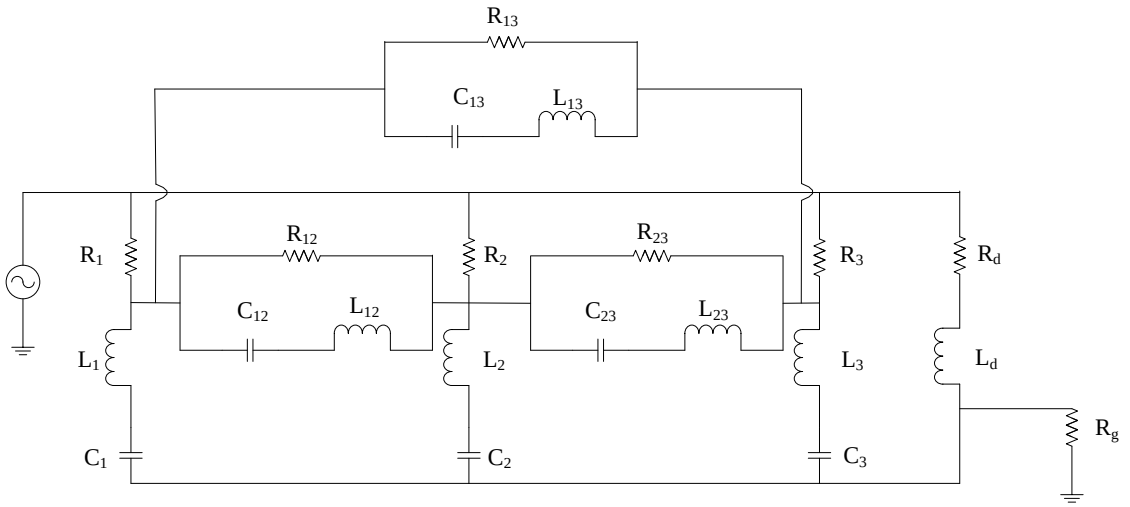


Figure 5.6 Equivalent circuit of the metamaterial absorber [5, 6].

Herein, L_i $(i = 1,2,3)$, C_i $(i = 1,2,3)$, and R_i $(i = 1,2,3)$ are the self-inductance, self-capacitance, and resistance for the three decagon loops. Also, inductors, capacitors, and resistors L_{ij}, C_{ij}, and R_{ij} $(i, j = 1,2,3, i \neq j)$ are the mutual inductance, mutual capacitance, and resistance resulting from the crosstalk between pairs of the three loops, which derived from the crosstalk model of transmission lines.

The initial self-capacitances, self-inductances and resistances of the three loops are extracted from the microstrip line model as follows:

$$C_i = \frac{\varepsilon_0 \varepsilon_r w l(i)}{h} \ (i = 1,2,3) \tag{5.2}$$

$$L_i = 2 \times 10^{-13} l(i)\left(ln\left(\frac{2l(i)}{w+h}\right) + 0.5 + \frac{0.2235(w+h)}{l(i)}\right. \ (i = 1,2,3) \tag{5.3}$$

$$R_i = \begin{cases} \frac{1}{\sigma w t}, \delta \geq t \\ \frac{l(i)}{w}\sqrt{\frac{\pi \mu_0 \mu_r f}{\sigma}}, \delta < t \end{cases} \ (i = 1,2,3) \tag{5.4}$$

where w is the width of each loop, $l(i)$ is the perimeter of the ith loop, h h is the height of the substrate, ε_0 is the permittivity of free space, and ε_r is the relative permittivity of the substrate; σ and t are the conductivity and thickness of the loops, respectively, μ_0 and μ_{r}

are the permeability of the free space, and the relative permeability of the substrate, respectively. The variable δ is the skin depth on the loops, and is used to quantify the skin effect, which is defined as the penetration depth at a given frequency where the amplitude is attenuated to 63% (e^{-1}) of the initial value at the surface of the conductor. Skin depth is given as:

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} = \sqrt{\frac{\rho}{\pi f \mu_0 \mu_r}} \tag{5.5}$$

where ρ is the resistivity of the conductor. As the skin depth δ of the loops within the operation band of the absorber is larger than the conductor thickness t, the resistance will be evaluated with the first equation.

R_g is the ground resistance is defined as the resistance between the traces and the ground plane, which is mainly contributed from the substrate. It can be derived from the same resistance equation as R_i where $l(i)$ and w values need to be changed to the length and width of the ground plane shown in Figure 5.4.

The mutual inductances and mutual capacitances are evaluated from the crosstalk theory as follows.

$$C_m = \frac{\pi \varepsilon_0 \varepsilon_r l(i)}{ln\,(4(w+g)w)}\ (i,j = 1,2,3, i \neq j) \tag{5.6}$$

$$L_m = \frac{\mu_0 \mu_r w l(i)}{\pi(w+g)}\ (i,j = 1,2,3, i \neq j) \tag{5.7}$$

where g is the gap between the loops.

For the resistance between Loop 1 and Loop 2, and that between Loop 2 and Loop 3, these resistance values can be approximately equal to the characteristic impedance of free space:

$$R_{12} = R_{23} = \frac{1}{\varepsilon_0 c} \tag{5.8}$$

where c is the speed of light. And because Loop 1 and Loop 3 are separated by Loop 2, R_{13} is relatively small compared to R_{12} and R_{23}. So that R_{13} is set to zero in this case:

$$R_{13} = 0 \tag{5.9}$$

Variables R_d and L_d are the real and imaginary parts of the characteristic impedance for the dielectric substrate η_d, which is defined as:

$$\eta_d = \frac{j\omega\mu_d}{\gamma} = \frac{1}{\sqrt{\varepsilon_0 \cdot \varepsilon_r - 2j\pi f(\varepsilon_d' tan\delta' - \varepsilon_d^{"})}} = R_d + jL_d \tag{5.10}$$

where $\varepsilon_d = \varepsilon_d' - j\varepsilon_d^{"}$ is the complex permittivity, μ_d is the permeability, γ is the propagation constant, and $tan\delta' = \frac{2\pi f \varepsilon_d^{"} + \sigma_d}{2\pi f \varepsilon_d'}$ is the loss tangent of the dielectric substrate.

The calculated values of the components in the equivalent circuit are used in ADS and tuned in order to have the absorbtance agree to that of the designed absorber unit. The values of the components after tuning are illustrated in Table 5.2. A comparison of the absorbtance values derived from the designed decagon absorber unit simulated in HFSS and from the equivalent circuit evaluated in ADS are displayed in Figure 5.7.

Table 5.2 Equivalent circuit values for the EBG absorber unit

R_1 (Ω)	C_1 (pF)	L_1 (nH)	R_2 (Ω)	C_2 (pF)	L_2 (nH)
55.97	0.0046	0.36	1183.45	0.081	0.061
R_3 (Ω)	C_3 (pF)	L_3 (nH)	R_{12} (Ω)	C_{12} (pF)	L_{12} (nH)
997.31	0.67	0.04	278.80	0.040	
R_{23} (Ω)	C_{23} (pF)	L_{23} (nH)	R_{13} (Ω)	C_{13} (pF)	L_{13} (nH)
0	0.14	0.65	278.80	0.081	0.20
R_d (Ω)	L_d (nH)	R_g (Ω)			
0.0045	0.32	0.72			

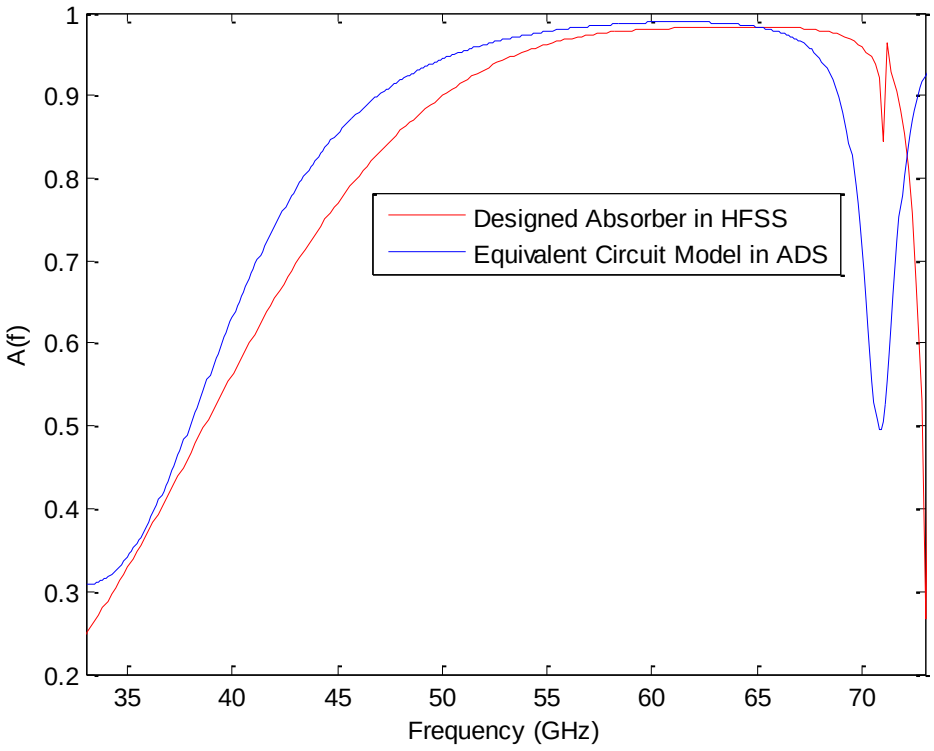


Figure 5.7 Absorbtance for the equivalent circuit and the designed absorber.

As can be seen in Figure 5.7, the absorbtance bandwidths for both cases are approximately 20 GHz, which are fairly consistent although they have shifted at the front at the back edges of the band by a few GHz. If the desired frequency band changes, it would be very convenient to set up a design in the ADS circuit model by modifying the dimensions and the air gap of the three loops, because the circuit simulation runs much faster than that of the full wave field modeling in HFSS. The developed circuit model will be very helpful for accurately and quickly establishing the physical absorber model.

5. 4 WIIC Channel Model Design with Absorber Layers

Based on the design of the metamaterial absorber, an entire WIIC channel is modeled, as shown in Figure 5.8.

In the channel design, two layers of the metamaterial EBG absorber units are placed at the top and bottom layers of the PCB board. Also, in order to analyze the S-Parameters of the system, three antennas are placed on the top layer to perform as the transceivers of the chips in the WIIC system. The transceivers are used to transmit and receive signals operating at 60 GHz frequency band.

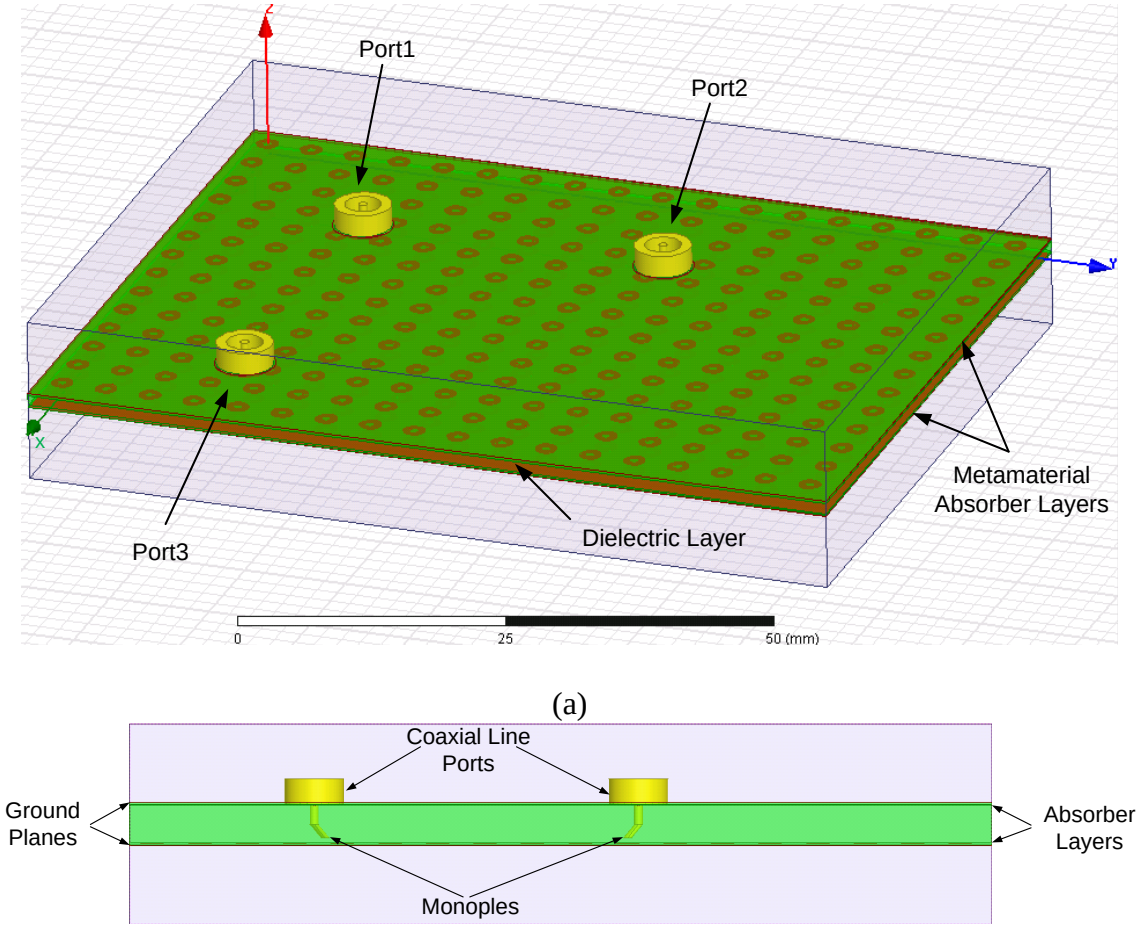


Figure 5.8 WIIC channel built with the metamaterial EGB absorber layers. (a) The geometry of the WIIC channel, and (b) its side view.

The WIIC channel is designed with the dimensions of 60×80×5 mm, and equipped with 249 and 252 (14×18) absorber units on top and bottom layer, respectively. The substrate dielectric material is Foam in the designed WIIC channel. Three micro-

antennas are placed on the top layer, which are fed with the coaxial lines. The micro-antennas are about 30 mm apart from each other.

The HFSS-simulated S-Parameters result for representative WIIC channels with ground planes and absorbers is given in Figure 5.9.

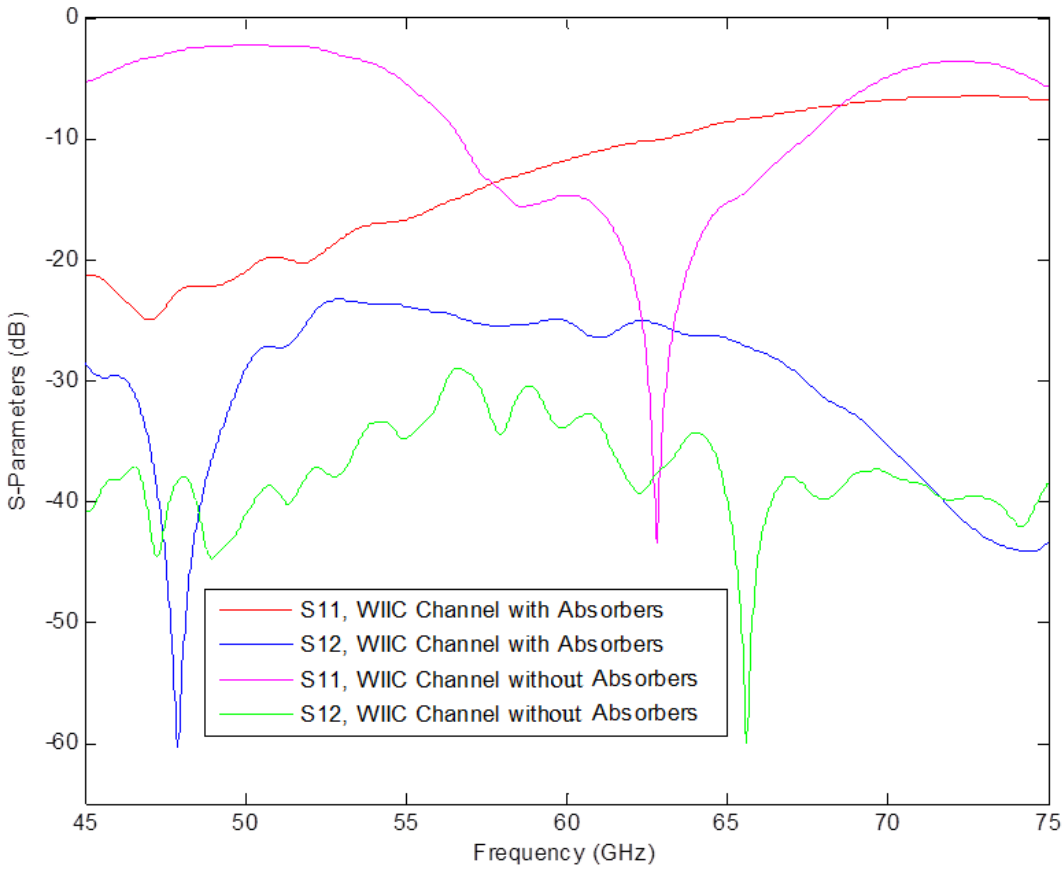


Figure 5.9 Comparison of S-Parameters for the designed WIIC channels with the metamaterial EBG absorber layers and ground plates.

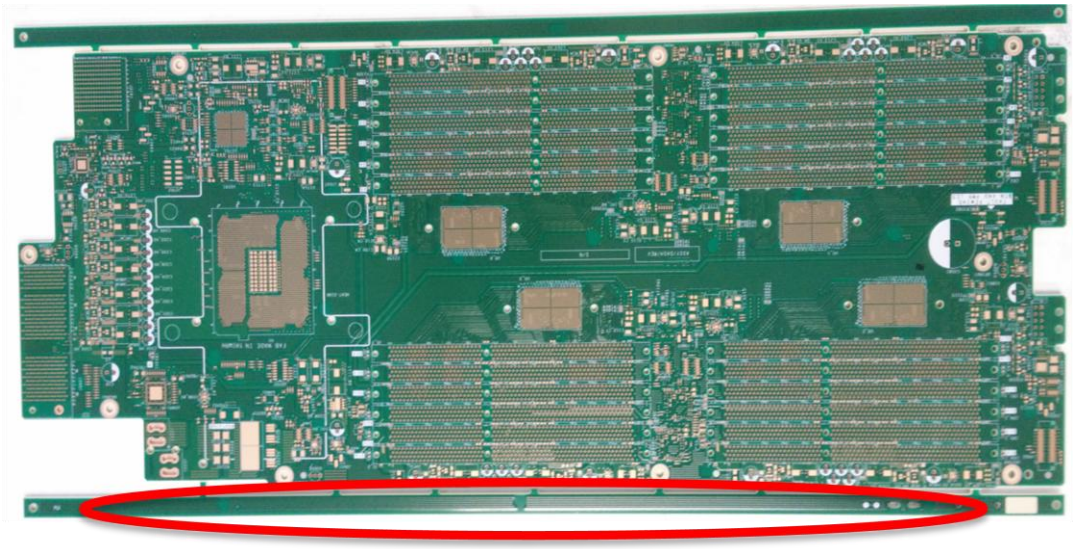
The 10 dB bandwidth with acceptable insertion loss approximately ranges from 50 to 70 GHz. As seen from the figure, the insertion loss between the transceivers ranges approximately from 22 to 35 dB, in the frequency band from 50 to 70 GHz. Thus, an equalizer at the receiver is also required. The return loss is about -13 dB at the central frequency, with a minimum of -32.06 dB at 49.62 GHz. The simulated S-Parameters of the designed WIIC channel with absorber layers will be utilized for impulse response and

transfer function extraction, which are further used in channel analysis and system. In this design the radiation from the pin monopole antennas will impinge upon the absorber layers over a range of incident angles. The majority of the normal electromagnetic waves will be significantly absorbed, and the tangential components parallel to the planes will remain in the system. It would be very nice to add absorber walls on all the sides of the WIIC channel. However, it would significantly add to simulation complexity, running time, and computer memory consumption. This will be studied in future research.

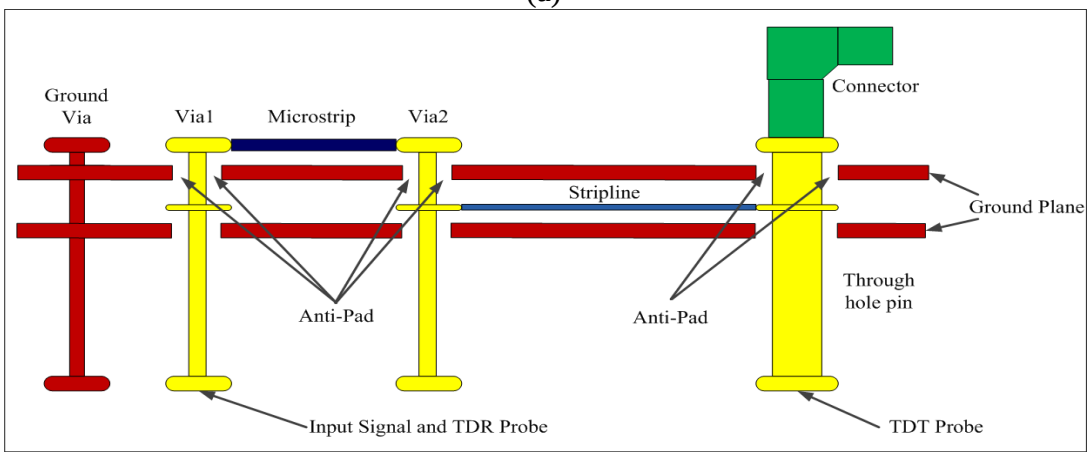
5.5 Wired PCB Channel Measurement and S-Parameter Generation

In order to compare the WIIC channel analysis to existing wired approaches, a wired PCB channel with a number of vias, striplines, microstrip lines, through hole pins, and connectors, has been analyzed and measured. The motherboard, which includes a CPU on the top layer, is shown in Figure 5.10 (a). The dimensions of the motherboard are 508×218×2.54 mm. In practice, there will be a backplane, which is even slightly larger than the motherboard. Sometimes there will be another board equipped for Field-Programmable Gate Arrays (FPGAs) and Basic Input/Output System (BIOS). There are usually a total of twenty-two layers on these PCB boards, including eight stripline layers, two microstrip line layers, ten ground planes, and two power planes. The size of the boards is much larger than the simulated WIIC PCB, because the wired PCB channels consist of hundreds of traces at different layers in order to reduce the crosstalk among these traces. Usually, PCB designers would have each motherboard with only one or two CPUs, such that they can focus on the design of the backplanes when the number of CPUs varies for different customers.

The analysis of the wired channel is to provide a reference structure by using the current technology implemented in PCBs, to validate the methodology developed for the wireless channel analysis in the frequency band of 60 GHz, and to find and understand the characteristics and limitation of the wired channel.



(a)



(b)

Figure 5.10 Wired PCB channel for TDR and TDT measurement. (a) The PCB board and (b) the designed wired PCB channel demo.

The channel consists of a 300-mil microstrip, two vias, a 5.3-inch stripline, a through hole pin, and a connector. The wired PCB channel is measured using both TDR and TDT signals. The S_{11} and S_{12} can be approximately generated from TDR and TDT, respectively. The reason for why not directly measuring the S-Parameters form a Vector

Network Analyzer (VNA) to extract the S-Parameters is primarily due to that the cost of the VNA capable for the desired high frequency band of 50-70 GHz is too expensive. It was unavailable when doing the measurement for the wired PCB channel. The TDT signals will be used for extraction of the impulse response and transfer function of the channel. The wired PCB channel is displayed in Figure 5.10, and represented in ADS in Figure 5.11. The S-Parameter models of via, through hole pin, microstrip and stripline simulated in HFSS, and the connector S-Parameters model provided by the vendor are cascaded in ADS to generate the combined S-Parameters and to obtain the simulated TDT/TDR for the wired PCB channel.

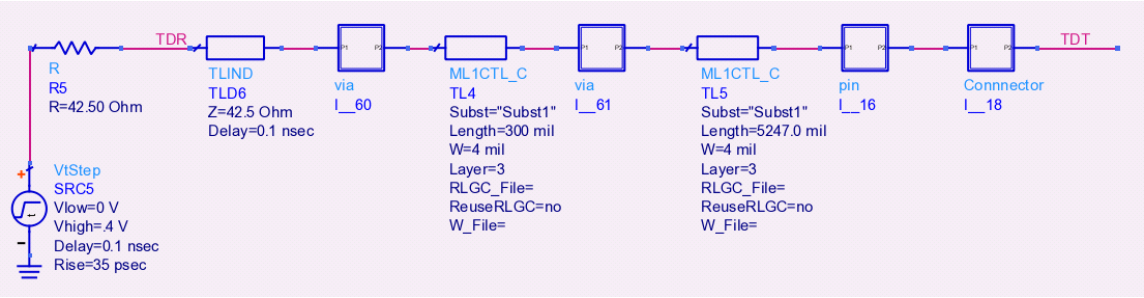


Figure 5.11 Schematic for wired PCB channel TDR and TDT simulation in ADS.

The measured and simulated TDR and TDT signals are represented in Figures 5.12 and 5.13, respectively.

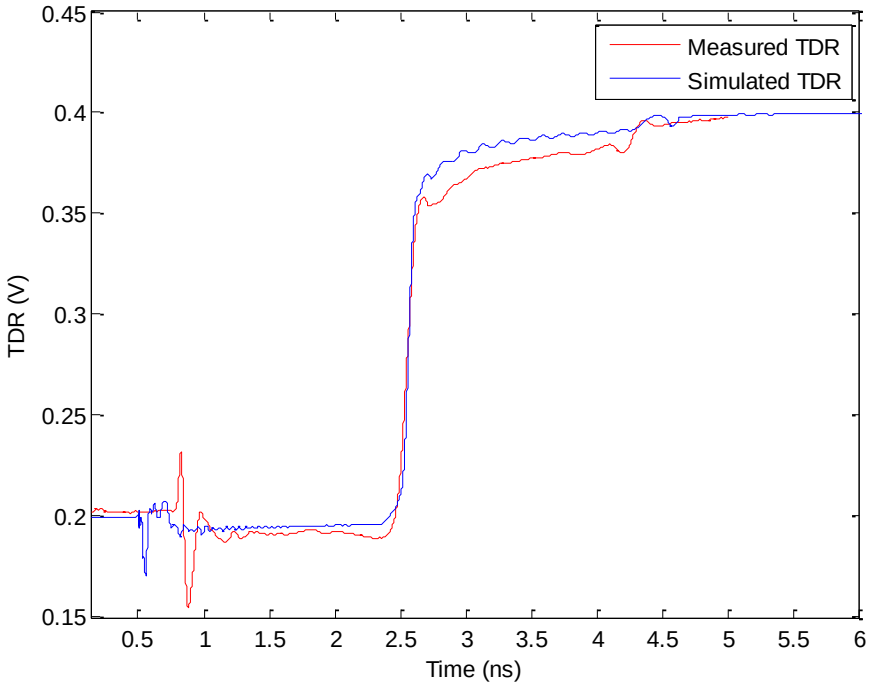


Figure 5.12 Measured and simulated TDR for the wired PCB channel.

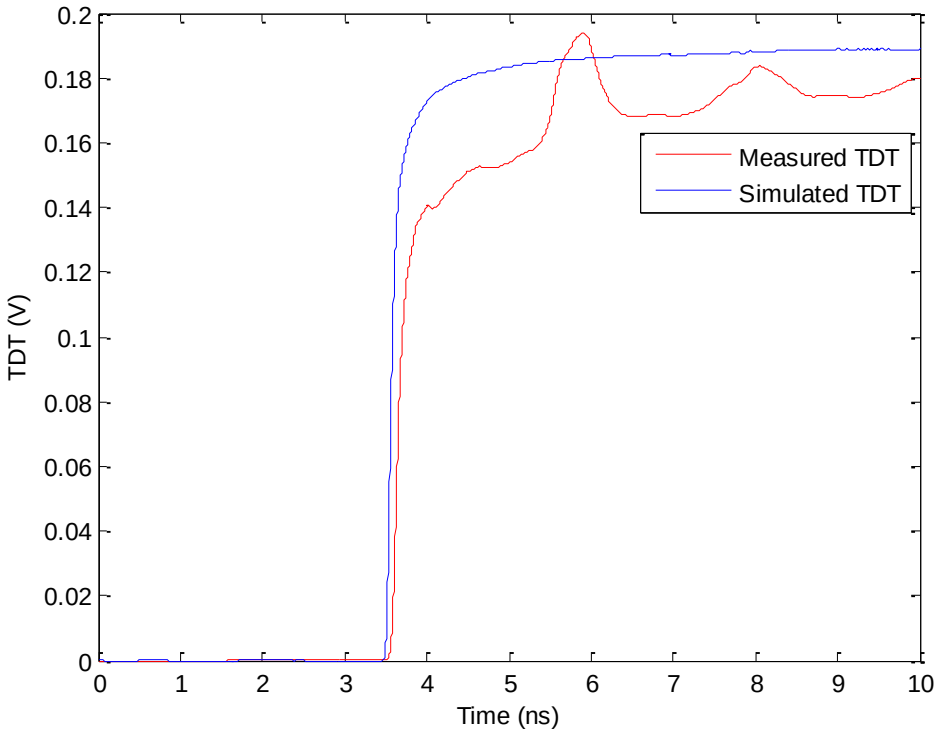


Figure 5.13 Measured and simulated TDT for the wired PCB channel.

TDR measures the impedance of each segment in a transmission line system, while TDT shows the transmission delay and the termination of the system. Details for TDT and TDR are specifically described in Appendix A.

As seen in Figure 5.12, the measured and simulated TDR signals are quite similar, except a peak at 0.8 ns in measured result, which indicates a high impedance resulting from the imperfect contact between the probe and the via pad on the bottom layer of the PCB board.

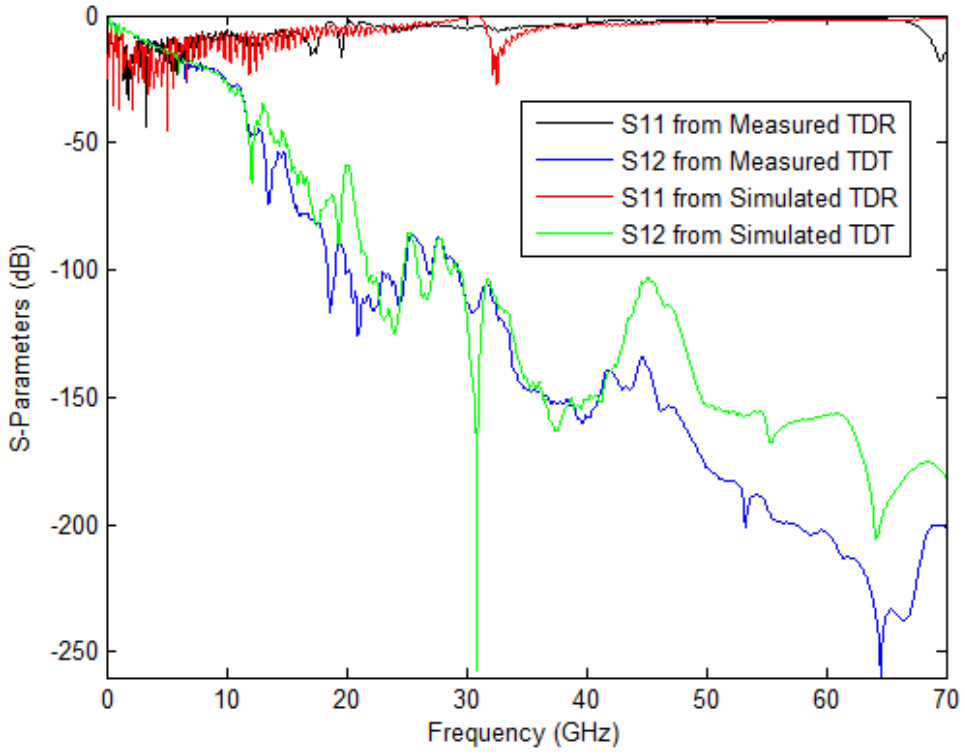
The measured and simulated TDT results are also very close with a little difference on their amplitudes. The simulated TDT final value is slightly higher than that derived from the measurement. This may be a result of the circuit mismatch or fabrication or measurement errors.

With the measured and simulated TDR and TDT signals, the S-Parameters of the PCB channel can be extracted in the frequency domain [74, 75]. The S-Parameters can be extracted in the following manner:

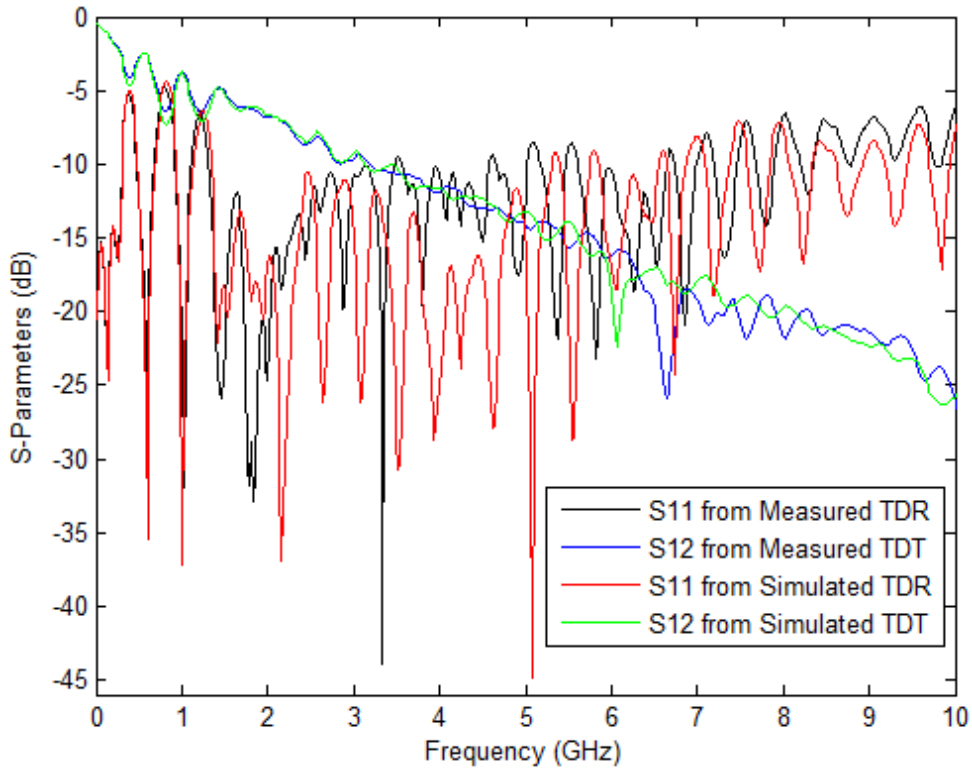
$$S_{11} = \frac{V_1^-}{V_1^+}\Big|_{V_2^+=0} = \frac{V_r(f)}{V_i(f)} = \frac{FFT(TDR)-FFT(V_i)}{FFT(V_i)} \tag{5.11}$$

$$S_{21} = \frac{V_2^-}{V_1^+}\Big|_{V_2^+=0} = \frac{V_t(f)}{V_i(f)} = \frac{FFT(TDT)}{FFT(V_i)} \tag{5.12}$$

The extracted S-Parameters are shown in Figure 5.14.



(a)



(b)

Figure 5.14 Extracted and simulated S-Parameters for the wired PCB channel. (a) 0-70 GHz frequency band, and (b) 0-10 GHz frequency band.

The measured and simulated S-Parameters extracted from the wired PCB channel agree fairly well at low frequencies. At the frequency of 60 GHz, the insertion losses are approximately -160 dB and -200 dB for the simulation and measurement of the wired PCB channel, while the return losses at the same frequency band are about 0 dB.

The results show that it is almost impossible for signals to propagate at the frequency band centered at 60 GHz, but this is not the most relevant observation. The most important observation regarding the wired PCB channel is its available bandwidth. The 10-dB bandwidth for the wired PCB channel is approximately 0-7 GHz. Within the bandwidth, the insertion loss varies from approximately 0-18 dB.

5.6 Generation of Impulse Response and System Transfer Function

5.6.1 Impulse Response Generation

To better describe the channel and to enable channel performance analysis, with the obtained S-Parameters of the wired PCB and the WIIC channels, the impulse responses are extracted. Although a proper IFFT of the insertion loss (S_{21}) can directly generate the impulse response, the IFFT of the TDT is not the exact impulse response by its definition. As seen from Figure 5.14, the converted S-Parameters from the TDR/TDT results via MATLAB and from the circuit simulation via ADS of the wired channel are not very consistent. To have a fair comparison among those channels and to avoid additional simulation errors introduced by conversions of signals in the frequency and time domains, the impulse responses are all generated via ADS with the same unit impulse input. The schematic for impulse response extraction is shown in Figure 5.15. The block in the middle represents either the S-Parameters of the WIIC or the wired PCB channel.

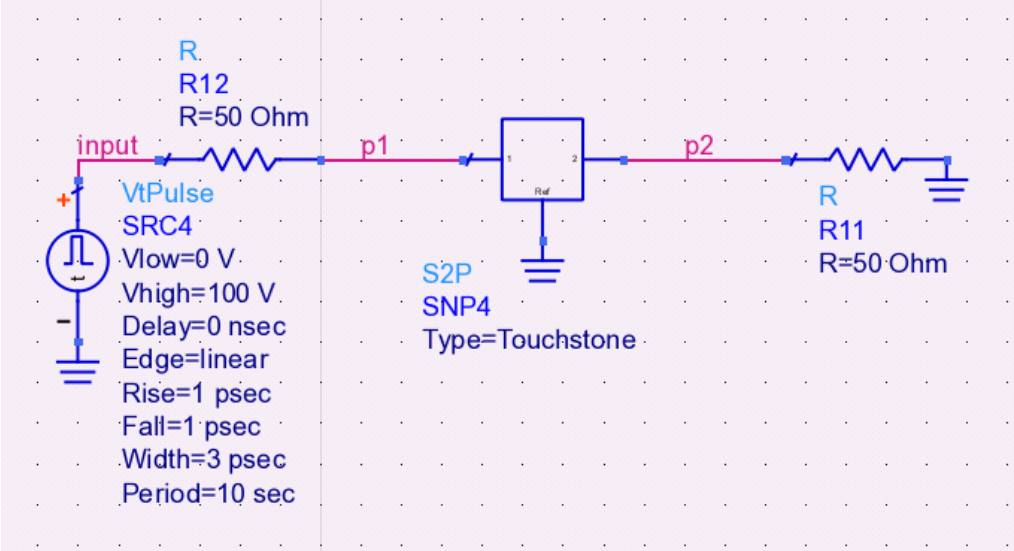


Figure 5.15 Schematic for impulse response extraction.

In ADS, a numeric, non-perfect unit impulse is injected into the channels. The generated unit impulse is determined to satisfy the following equation:

$$\int_{-\infty}^{\infty} \delta_W(t)dt = \frac{1}{2}(\Delta t_1 + \Delta t_2)V_H = 1\ (V \cdot s) \qquad (5.13)$$

where V_H is the magnitude of the impulse, Δt_1 and Δt_2 are the impulse widths at its bottom and top positions.

The injected impulse is chosen with $V_H = 250$ GV in magnitude, 3 *ps* width, 1 *ps* rising and falling edges, in order to satisfy the definition of impulse response as given in Equation (5.13) and is shown in Figures 5.16.

The extracted impulse responses of the designed WIIC channel and the wired PCB channels are displayed in Figure 5.17. The WIIC channel are the designs that equipped with a pair of parallel plates, and two layers of metamaterial EBG absorbing units, while the impulse responses for wired PCB channel are extracted from both the measured and simulated results.

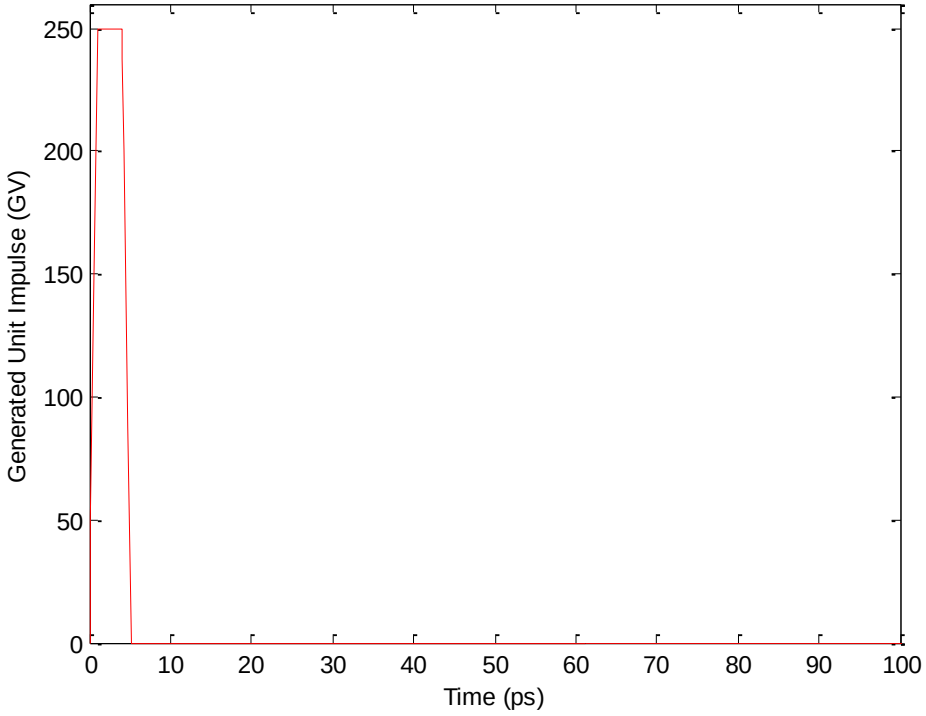


Figure 5.16 The injected unit impulse in the time domain.

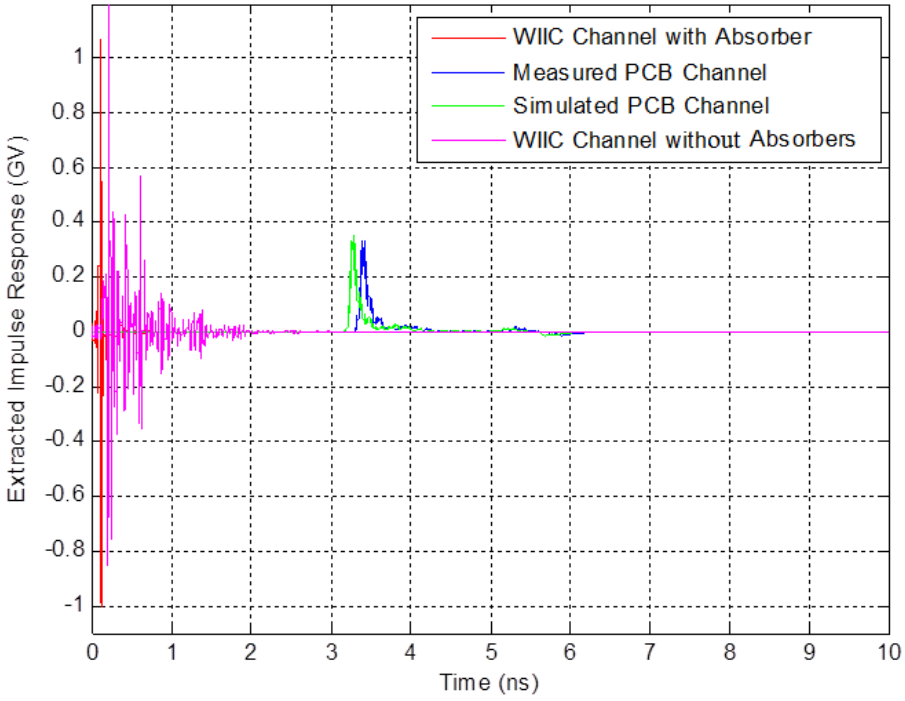


Figure 5.17 Impulse responses for the designed WIIC and PCB channels.

As can been seen from the figure, the simulated and measured impulse responses for the wired PCB channel are similar, with a little time delay difference. The time delay may be resulted from by parasitic mutual capacitance and inductance of the PCB circuit components, or from the imperfect contact between the probe and the via pad on the bottom layer during the measurement. It is noticed that, the time domain amplitude of the impulse response for the wireless WIIC channel's is about three times of that of the wired PCB channel. In other words, with a same input to the channels, the response magnitudes of the WIIC channels will be much larger than that of the wired PCB channel, which can also be deduced from the insertion loss as seen in Figures 5.9 and 5.14.

5.6.2 System Transfer Functions Generating

The frequency response of a system can be easily generated in MATLAB (Matrix Laboratory) by performing an FFT of its corresponding impulse response. The relation between the discrete frequencies of the FFT signal and the sampled time domain points have to satisfy the following relations [74]:

$$\Delta f = \frac{1}{\Delta t N} \tag{5.14}$$

where Δf is the frequency interval of frequency response, the Δt is the sampling time interval of the impulse response, and N is the total samples of the impulse response in the time domain.

With the above equation, the FFT transformed versions of the impulse responses are simply as the frequency transfer functions of the measured and simulated wired PCB, and designed WIIC channels. The extracted system normalized transfer functions, $|H_w(f)|$ for the WIIC system equipped with two layers of metamaterial EBG absorber

units, $|H_{wp}(f)|$ for the WIIC system with two parallel plates, $|H_p(f)|$ for the measured PCB channel and $|H_s(f)|$ for the simulated PCB channel are shown in Figure 5.18.

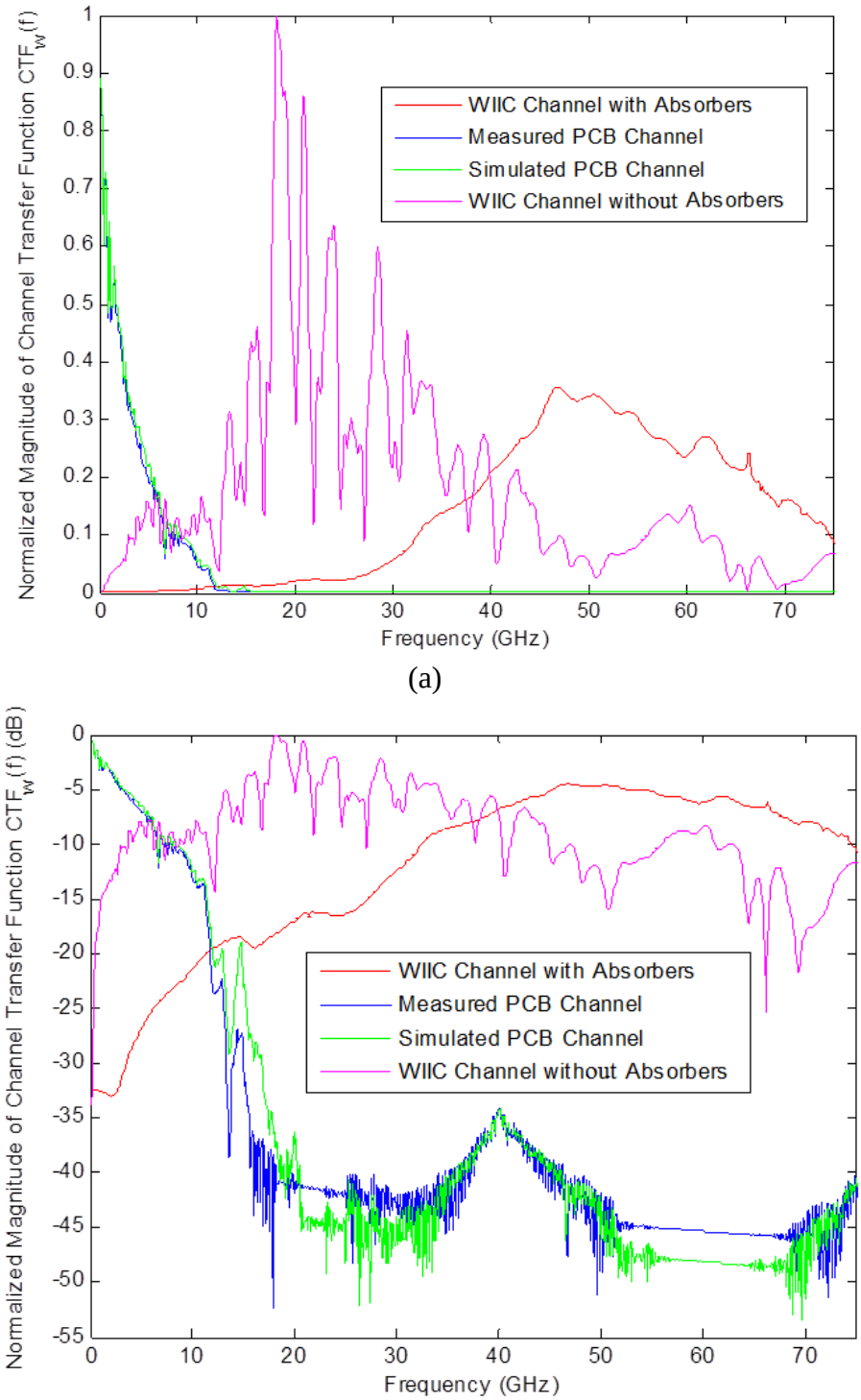


Figure 5.18 Normalized transfer functions for the designed WIIC and wired PCB channels. (a) Linear scale, and (b) dB scale.

It is clearly seen that the normalized transfer functions of the simulated and measured PCB channels are very consistent, and they are almost cutoff from 15 GHz. However, the proposed WIIC channel performs very well for the desired frequency band around the neighborhood of 60 GHz. In other words, with an identical input to the channels, the bandwidth of the WIIC channels will be larger than that of the wired PCB channel. The transfer function for the WIIC channel with absorbers is flat within 3 dB of variation in the frequency range of 45-65 GHz. It is noticed that this bandwidth is not completely consistent with that of the Insertion Loss simulation resulted from HFSS. The reasons can be summarized as follows:

- **The definitions between Insertion Loss and Transfer Function are slightly different.** The Insertion Loss is derived from the division of the scattering coefficient, which is defined as the ratio of the square root of the transmitted and injected powers. When measuring the insertion loss, all ports must be matched. On the contrary, the transfer function is defined as the Fourier Transform of the impulse response of a system, while the impulse response is derived by the division of the input and output signals, which can be voltage-voltage, current-current or voltage-current, etc. The impulse response is measured when any of the ports to be open, matched or mismatched. In this dissertation, as can be seen in Figure 5.15, the unit impulse is injected into the S-Parameters circuit block, with both the source and load impedances to be 50 Ohms, which cannot guarantee a matched port in this situation.
- **The approximation of the impulse response and Transfer Function.** In this dissertation, the injected impulse is quasi-unitary. Thus, the generated impulse

response is an approximation of the actual impulse response. Consequently, the transfer functions are also an approximation to the actual transfer function.

5.7 Characteristics for the WIIC Channels

In order to better characterize the designed WIIC channels, the extracted S-Parameters and impulse response are used for the calculation of the link budget, round trip delay and delay spread analysis. In the link budget analysis, conventional FDM QPSK modulation and SISO are employed.

5.7.1 Characterized Parameters for the WIIC Channel

A) Path Loss

If all I/O ports are well matched, the attenuation (path loss) and the insertion loss (S_{21}) in dB are given as follows [5-6]:

$$PL = \frac{P_t}{P_r}$$
$$PL(dB) = 10log\frac{P_r}{P_t}(dB) \tag{5.15}$$

$$S_{21} = \frac{b_2}{a_1} = \frac{V_2^-}{V_1^+} = \sqrt{\frac{P_r}{P_t}}$$
$$S_{21}(dB) = 20log|S_{21}| = 20log\left|\sqrt{\frac{P_r}{P_t}}\right| = 10log\frac{P_r}{P_t} = PL(dB) \tag{5.16}$$

where PL is the path loss, P_t and P_r are the transmitted and received power.

Therefore, if all I/O ports are well matched, the path loss will be approximately equal to the insertion loss [109], while the simulation in HFSS included an inherent antenna gains or possibly losses. As seen in Figure 5.8 where all I/O ports are well matched in HFSS simulation, the path loss of the designed WIIC channel at 60 GHz is approximately 22 dB and varies from 22 to 35 dB within the total bandwidth of the channel of 50-70 GHz.

B) One-way Time Delay

The one-way time delay in the WIIC channel is evaluated as

$$t_D = \frac{d}{v_c} = 102.67\ ps \tag{5.17}$$

where t_D is the one-way time delay that is the time of a signal to transmit from the transmitter to the receiver, d is the distance between the transceivers, and v_c is the speed of light in the dielectric substrate.

C) Root-Mean-Square Delay Spread

The root-mean-square (RMS) delay spread is given as the second central moment of the power delay profile [51]:

$$S_\tau = \sqrt{\frac{\int_{-\infty}^{\infty} P_h(\tau)\tau^2 d\tau}{\int_{-\infty}^{\infty} P_h(\tau) d\tau} - T_m^2} \tag{5.18}$$

where S_τ is the RMS delay spread and T_m is the mean delay, which is defined as the first-order moment of the power delay profile [51]:

$$T_m = \frac{\int_{-\infty}^{\infty} P_h(\tau)\tau d\tau}{\int_{-\infty}^{\infty} P_h(\tau) d\tau} \tag{5.19}$$

where $P_h(\tau)$ is the power delay profile (PDP) as a function of delay τ, which is the measured power of the impulse response of the designed WIIC channel, defined as follows:

$$P_h(t) = |\mathrm{h(t)}|^2 \tag{5.20}$$

where $h(\tau)$ is the complex baseband impulse response. The PDPs of the WIIC channel with absorber, WIIC channel with parallel ground plane, and the wired PCB channel are displayed in Figure 5.19.

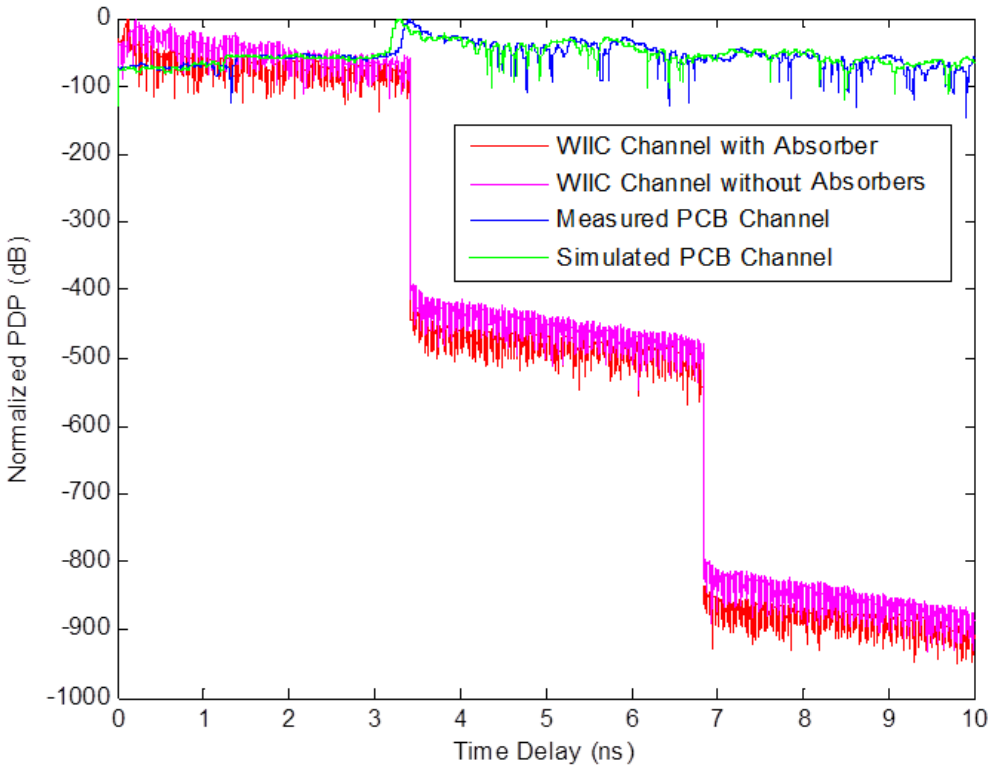


Figure 5.19 Power delay profiles for WIIC and wired PCB channels.

The RMS delay spreads are calculated in MATLAB® to be:

$$S_\tau = \begin{cases} 24.14\ ps,\ WIIC\ Channel\ with\ Absorbers \\ 214.18\ ps,\ WIIC\ Channel\ with\ Parallel\ Plates \\ 245.46\ ps,\ Wired\ PCB\ Channel \end{cases} \quad (5.21)$$

The coherence bandwidths, which are the approximate bandwidths over which the channel yields little distortion, are

$$B_c = \frac{1}{5S_\tau} = \begin{cases} 8.29\ GHz,\ WIIC\ Channel\ with\ Absorbers \\ 933.79\ MHz,\ WIIC\ Channel\ with\ Parallel\ Plate \\ 814.80\ MHz,\ Wired\ PCB\ Channel \end{cases} \quad (5.22)$$

As a result, the approximately zero distortion bandwidth is about 8.29 GHz for the WIIC channel with the absorbers. With the OFDM employed in the system, a wideband signal is separated to several narrow band signals, each of which can be equalized via the zero forcing complex multiplication.

D) Estimated Data Rate for QPSK Modulation

The corresponding achieved peak data rates for the following cases: *(i)* QPSK, single carrier and SISO; *(ii)* QPSK, SISO and conventional FDM; *(iii)* QPSK, OFDM and SISO; *(iv)* 256 QAM, OFDM and with identical and ideal 4×4 MIMO (theoretically upper bound) are given as follows:

Table 5.3 Achievable peak data rate

Parameters	**Peak Data Rate**
QPSK, conventional FDMA and SISO	$R_{b\_FDMA\_ideal} = R_{b\_sc} \cdot \frac{BW}{BW_{sc}} = 40\ Gbps$ (with Ideally perfect BPFs and no bandgap between symbols) $R_{b\_FDMA} = 16\ Gbps$ (To allow for filter guard bands)
QPSK, OFDM and SISO	$R_{b\_OFDM\_ideal} = 2R_{b\_FDMA\_ideal} = 80\ Gbps$ $R_{b\_OFDM} = 4Bc = 33.2\ Gbps$
Theoretically upper bound - 256 QAM, OFDM and with identical and ideal 4×4 MIMO antenna arrays	$R_{b\_OFDM\_256QAM\_4MIMO} = R_{b\_OFDM} \cdot \frac{\log_2 256}{2} \cdot 4$ $= 531.2\ Gbps$

In the dissertation, as MIMO and QAM are not included in the final version of the proposed WIIC system, the last row of Table 5.3 only gives the theoretical upper bound of the peak data rate for the WIIC system with 256 QAM, OFDM, identical and ideal 4×4 MIMO antenna arrays. The feasibilities of MIMO and QAM in the WIIC system are not analyzed in the dissertation, and the design and analysis of MIMO and QAM are suggested as future research in Chapter 7.

E) Estimated Required SNR for QPSK Modulation

As the target BER is set to be 10^{-12}, for QPSK modulation, the theoretical BER-SNR relationship is:

$$BER(QPSK) = Q\left(\sqrt{2\gamma_B}\right) \tag{5.25}$$

where γ_B is the SNR in linear units:

$$\gamma_B = \frac{E_B}{N_0} \tag{5.26}$$

The Q-function is the tail probability of the standard normal distribution. In other words, $Q(x)$ is the probability that a normal (Gaussian) random variable will obtain a value larger than *x*, i.e.:

$$Q(x) = P(X \geq x) = \frac{1}{2} erfc\left(\frac{x}{\sqrt{2}}\right), X \sim N(0,1) \tag{5.27}$$

$$erfc(x) = 1 - erf(x) = 1 - \frac{2}{\sqrt{\pi}} \int_0^x e^{-t^2} dt = \frac{2}{\sqrt{\pi}} \int_x^\infty e^{-t^2} dt \tag{5.28}$$

Using the embedded inverse complementary error function $erfc^{-1}(*)$ function in MATLAB®, the required SNR for the target BER is calculated to be:

$$\gamma_B \geq 24.72, or\ SNR \geq 13.93\ dB \tag{5.29}$$

5.7.2 Link Budget

A link budget is required to compute the required TX power. It tabulates all parameters that connect the TX power to the received SNR. As most factors influencing the SNR enter in a multiplicative way, it is convenient to write all the equations in a logarithmic form – specifically, in dB. The link budget for two transceivers in the WIIC channel is provided in Table 5.4.

The minimum required RX power P_{min}, required Transmission power (P_t), minimum TX power P_{TX} and required energy E_b per bit are derived as follows:

$$P_{r\_min}(dB) \geq P_n(dB) + SNR(dB) \tag{5.30}$$

$$P_n(dB) = 10\log(k_B T_e) + NF + 10\log(B) \tag{5.31}$$

$$P_r(dB) = P_t(dB) + G_t(dB) + G_r(dB) - PL \tag{5.32}$$

$$E_b = P_{TX}/BW \tag{5.33}$$

Table 5.4 Link budget of the WIIC channel

Item	Symbol	Value
Noise		
Noise Figure	NF	10 dB
Bandwidth	B	20 GHz
Power Noise at Rx	P_n	-60.81 *dBm*
RX side:		
Target BER		10^{-12}
Required SNR	SNR	13.93 *dB*
RX Antenna Gain	G_{RX}	1.5 *dB*
Minimum RX Power	P_r	-46.89 *dBm*
Path Loss	PL	-25 *dB*
TX side:		
TX Antenna Gain	G_{TX}	1.5 *dB*
Required Transmitter Power	P_t	-28.17 *dBm*
Minimum bit energy	E_b	1.22 *pJ/bit*

5.8 Proposed Layout Plan and Silicon Area Estimation

5.8.1 Comparison of DSP and ASIC Solutions of the Proposed WIIC System

Independent from CPUs, an integrated WIIC DSP system will be included to perform the process of CRC, packet header insertion, channel coding/decoding, modulation and OFDM.

DSP technology rather than ASIC for the WIIC system is preferable in the dissertation based on the following consideration:

- ASIC technology [93-104] is also capable for signal processing with better performance in terms of board area and power consumption, while it usually needs a longer cycle for complex circuit design. Also, ASIC circuits are especially complicated for OFDM, FFT/IFFT, higher order modulation, and potentially MIMO for WIIC systems. In this dissertation, the estimation for board area consumption will

be based on the implementation of low-power consuming DSPs. The analysis of WIIC ASICs will be the one of the primary future research topics.

- It is known that the low power consuming DSP chip (such as ARM) requires much less power than that of an Intel conventional CPU [91] [92]. Also, the area of this DSP has been estimated to be much smaller in comparison to the Intel conventional CPU. This low power-consuming DSP technology will be potentially used in the WIIC system. The power consumption, processing speed, board area consumption and maximum FFT points for current CPUs, DSPs and ASICs are shown in Table 5.5, which indicates that the DSPs are power efficient, require a smaller board area, and are with acceptable clock rate and FFT points.

Table 5.5 Comparison of conventional Intel CPU, DSP and FFT ASIC

	Intel ® Skylake ® CPUs [90]	**NXP® DSPs** [91]	**FFT ASICs** [100]
Thermal Design Power (TDP)	15-91 W	0.15 mW/MHz	2.9 mW
Clock rate	4.2 GHz	1.2 GHz (8 Cores)	Up to 2 GHz
Board area consumption	37.5 × 37.5 mm	3.5 × 3.5 mm	81.6 mm^2
Maximum FFT Points	Not specially designed for FFT, but up to 768K	Typical 2048 (up to 8192)	Up to 1024
High order modulation	Yes	Included	Need extra design
Channel Coding/Decoding	Yes	Included	Need extra design

- Furthermore, the cost of the DSPs is expected to be much less expensive than the cost of the conventional CPU, and the design of the connection from the antenna array to the DSP pins is simple and compact.

5.8.2 Proposed Layout Plan

The initial proposed WIIC system operations will be processed in a DSP, including the high-speed process of higher order modulation, convolutional coding, Viterbi decoding and FFT/IFFT. For power efficient purpose, the ARM ® DSPs will be preferred, while the Intel WiMAX DSPs are also options that they may be more compactable with Intel's CPUs. The proposed layout plan is shown in Figure 5.20. The discussion with the industry comes to a suggestion of the antennas to be layout as vias. The DSP pins, CPU socket pins and antennas can be connected by through hole vias and microstrips.

The area of an Intel CPU is about 37.5 *mm* × 37.5 *mm*, while the DSP is approximately 6.4 *mm* × 9.7 *mm*. There will be some microstrip lines from the input DSP pins to the through hole vias, as the DSP pins are not always aligned with the CPU pins. Also, microstrip lines exist between DSP output pins and the antenna vias, in order to perform phase matching. For instance, as shown in Figure 5.20 (b), in the 4-Socket multi-CPU system, there are three antennas for each CPU to transmit WIIC signals to others. Therefore, the total Silicon Area of the WIIC system should not exceed the Silicon Area of the CPU, 37.5 *mm* × 37.5 *mm*. In other words, the Silicon Area for the proposed WIIC system is much less than the wired counterpart, which takes at least four layers of three boards of 40 *cm* × 70 *cm*.

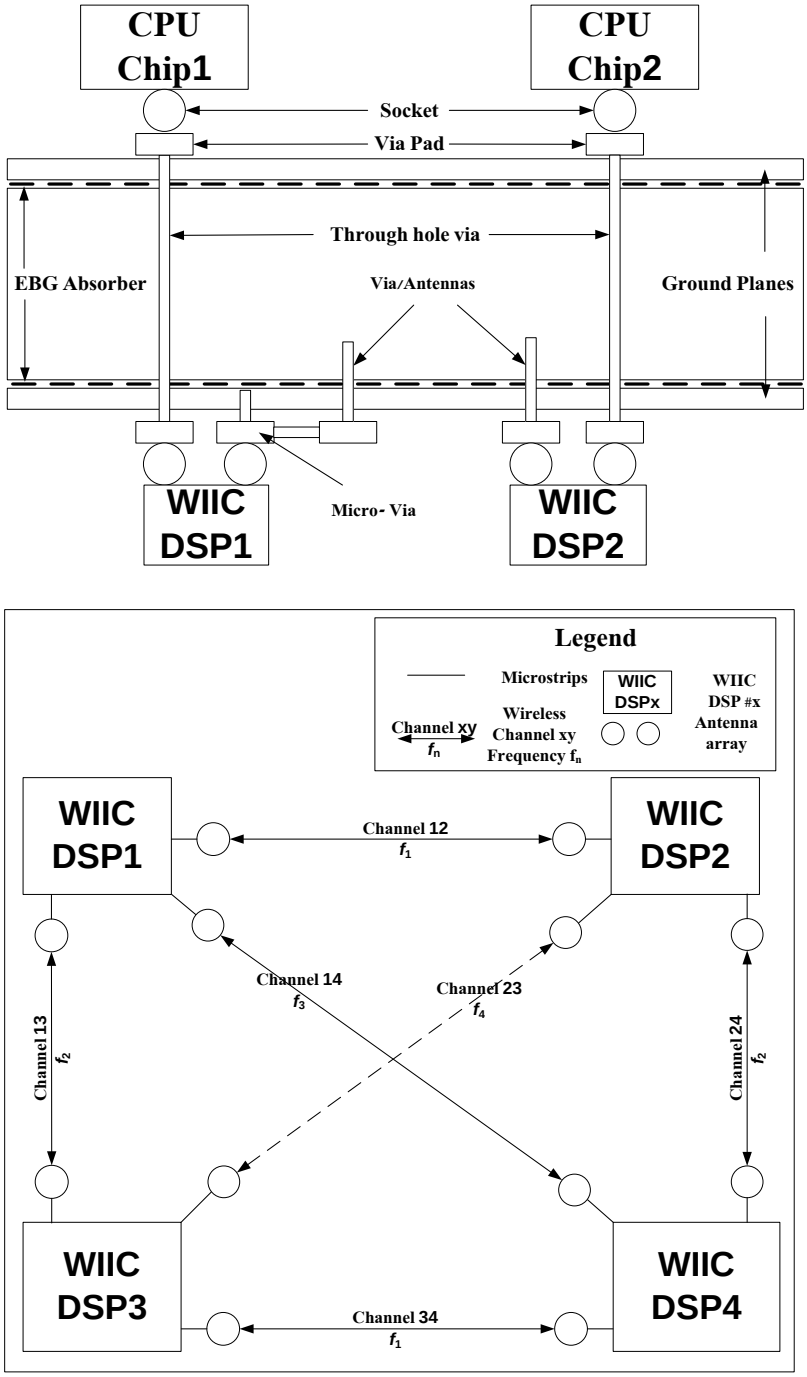


Figure 5.20 Proposed layout view of the WIIC system. (a) Side view, and (b) Top view.

CHAPTER 6

SIMULATION OF THE WIIC SYSTEM

The proposed WIIC system developed in the previous chapters has been simulated in MATLAB. The preliminary WIIC system includes the functional blocks of Cyclic Redundancy Check, QPSK modulation, SISO, the OFDM and CP insertion. In this chapter, a preliminary WIIC system is first validated by using an AWGN channel in MATLAB. Then, OFDM, RS channel sounding, channel coding, channel estimation and channel equalization are further investigated in the full-system BER analysis with all four channels including AWGN, wired PCB and the WIIC channels. In the preliminary system validation, a series of 480,000,000 bits are randomly input into the designed WIIC system for obtaining the bit error rate (BER) for each signal to noise ratio (SNR). In addition, the total number of random input bits at one single SNR point in the full system and channel analysis is 441,600,000.

6.1 Preliminary System Implementation with an AWGN Channel

In this section, the designed WIIC system described in Chapters 3 and 4 are simulated in an AWGN channel, with the analysis including OFDM signal generation, constellation collection at the receiver, and BER vs. SNR.

6.1.1 OFDM Signal Generation

When the random binary symbols are input to the transmitter of the OFDM system, the baseband signals are processed by the proposed transmitter signal processing

system. When the SNR at the receiver are of 10dB, 20dB and 30dB SNR, the processed signal at the transmitter are shown in Figures 6.1, 6.2, and 6.3 respectively.

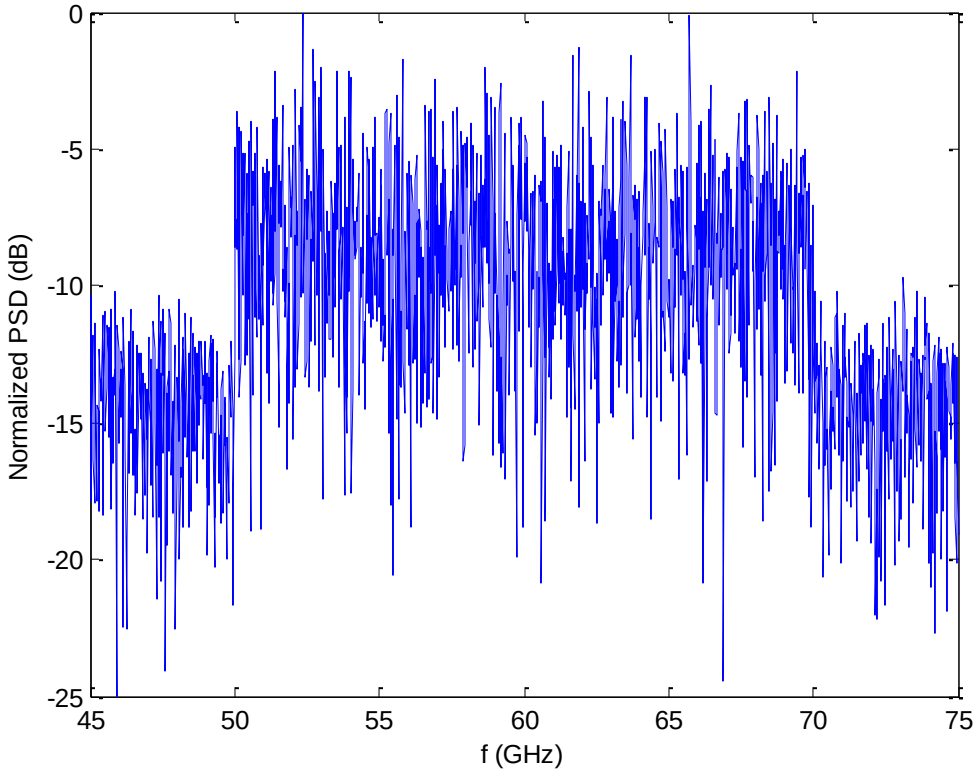


Figure 6.1 Normalized Power Spectral Density of the transmitted signals for an average for 10000 realizations.

6.1.2 Constellations Generated at the Receiver

After the transmitted signals pass the AWGN channel model, the receiver collects the signals and noise from its antennas, correctly removes the Cyclic Prefix, obtains the data samples, and processes these samples in the OFDM demapping subsystem, which is abbreviated as deOFDM in Figure 6.2, and Figures 6.4-6.9. After completing all these procedures, the receiver gets a series of QPSK complex symbols. When plotting all these symbols in a Cartesian coordinate system, a constellation diagram of the received signals

is obtained. The constellation of the received signals before QPSK demodulation at 20 dB SNR is shown in Figures 6.2.

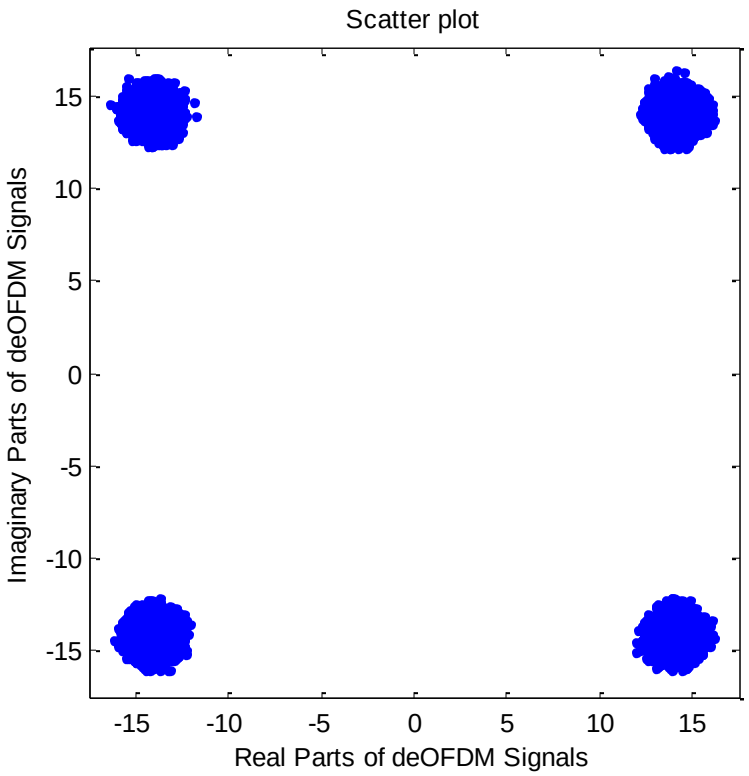


Figure 6.2 Constellation of the received signals at 20dB SNR for the AWGN channel.

6.1.2 BER Analysis

An initial simulation result for the AWGN channel is shown in Figure 6.3. In these results, the system does not include channel coding/decoding, RS signals, and channel equalization. As predicted in the previous analysis, the BER is less than 10^{-5} at 6.5 dB SNR, and BER at 5 dB SNR is about 9.4×10^{-5}. Furthermore, in the case investigated, no error bits occur out of ~400 million bits sent, if SNR is greater than 9 dB, which is an acceptable SNR level in the proposed channel model.

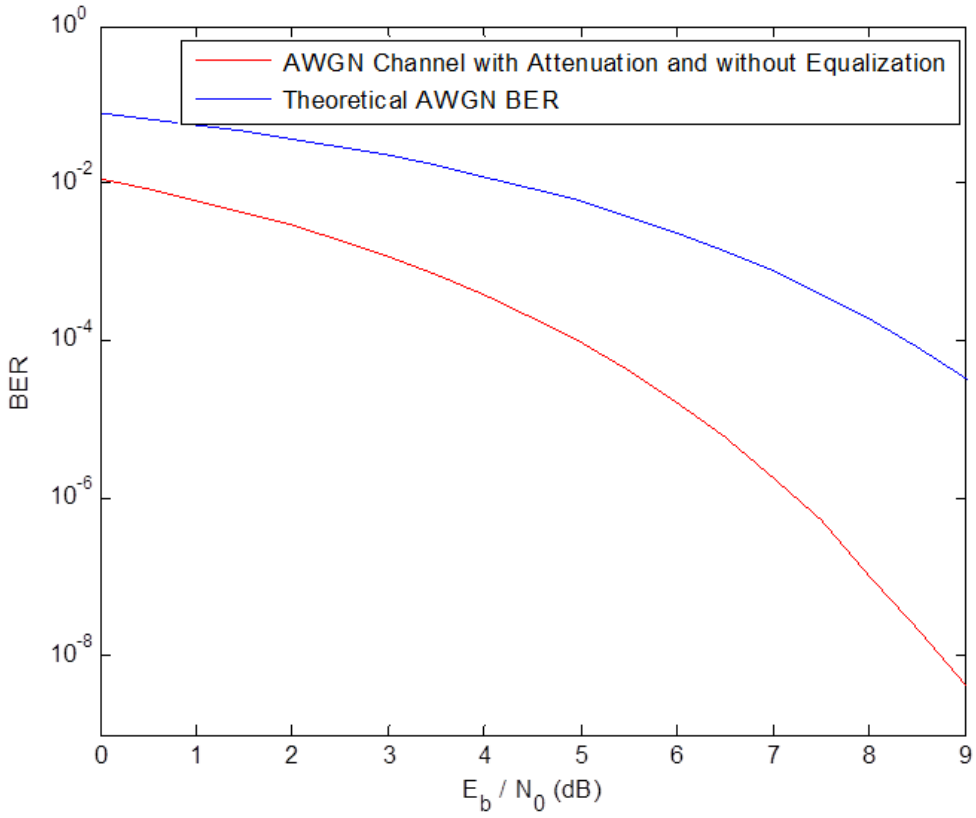


Figure 6.3 BER vs. SNR without channel coding and equalization.

Herein, BERs are extracted by directly comparing the input and output, so that the results are more reliable than obtaining the BER result by calculating using CRC checking results.

6.2 Full System Analysis for AWGN, WIIC and PCB Channels

In this section, the functional blocks of RS channel sounding, channel coding, channel estimation and channel equalization schemes are added to the simulation of the WIIC system. The simulation employs all three channels including AWGN with FEC, the designed WIIC, and the wired PCB channels. In this section, the constellation plots for the three channels are firstly represented, and then the BER vs. SNR results are displayed.

The wired PCB channel analyzed in the dissertation was designed and fabricated for digital communications at about 10 GHz between CPUs used in Oracle X5-4 servers. The channel was selected for measurement and simulation due to that it is the highest frequency band in comparison to other available wired channels.

Rather than a comparison between the wired and wireless communication systems in the 60GHz frequency band, the wired channel mainly serves as a reference structure to provide a validation for the methodology developed for measurement and simulation. The validation between the measurement and simulation includes HFSS simulation, TDR/TDT measurement and simulation, S-parameter calculation, impulse response and transfer function extraction, and WIIC system simulation.

6.2.1 Constellations Generated at Receiver

Constellation graphics are capable to illustrate the characteristics of the channels. The constellations for the equalized AWGN, and WIIC with absorbers and wired PCB channels, are shown in Figures 6.4 through 6.9. Each channel yields constellations for the cases of 3, 5, and 10 dB SNR.

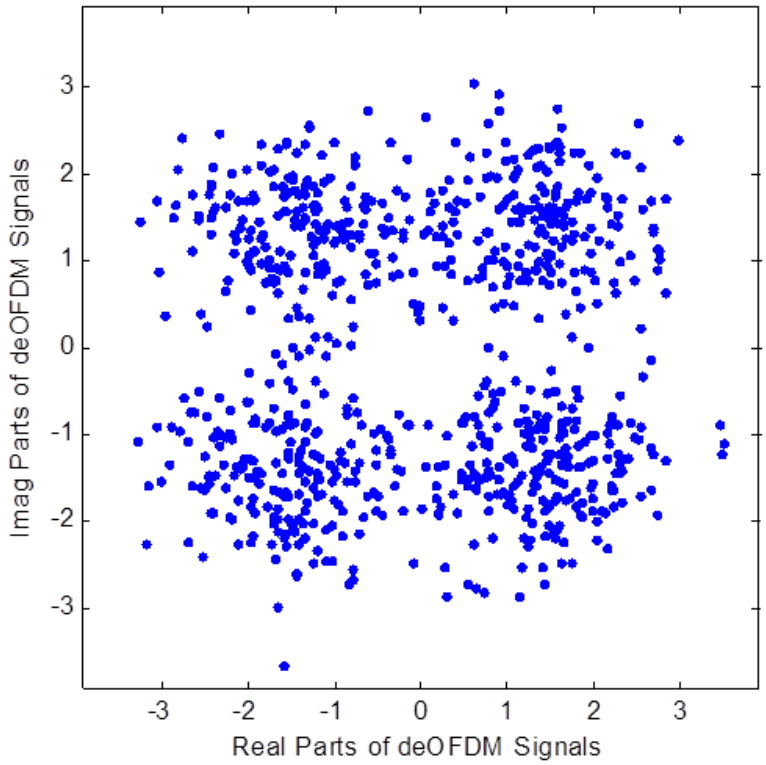


Figure 6.4 Constellation of the received signals for AWGN Channel at 3 dB SNR.

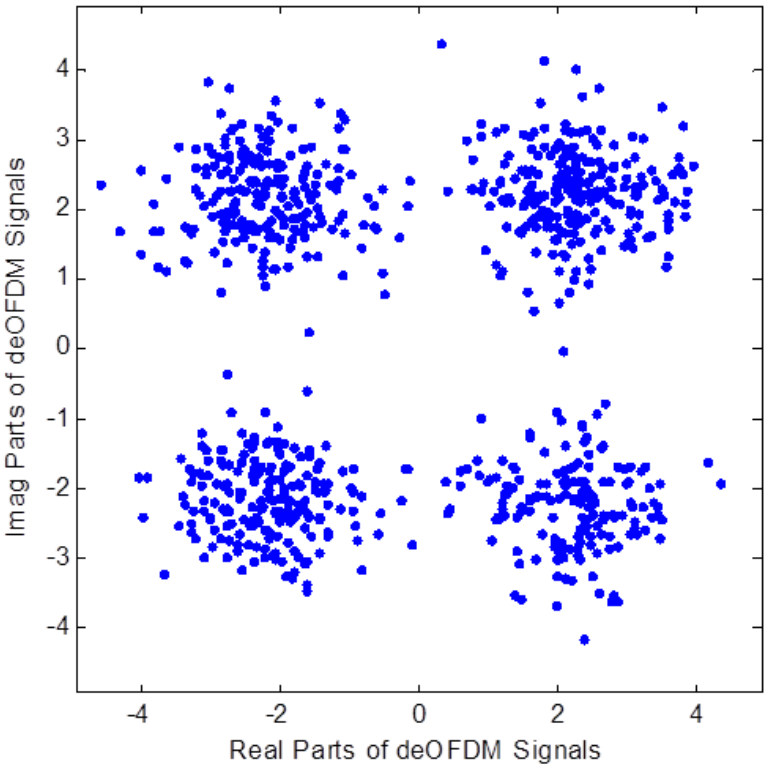


Figure 6.5 Constellation of the received signals for AWGN Channel at 5 dB SNR.

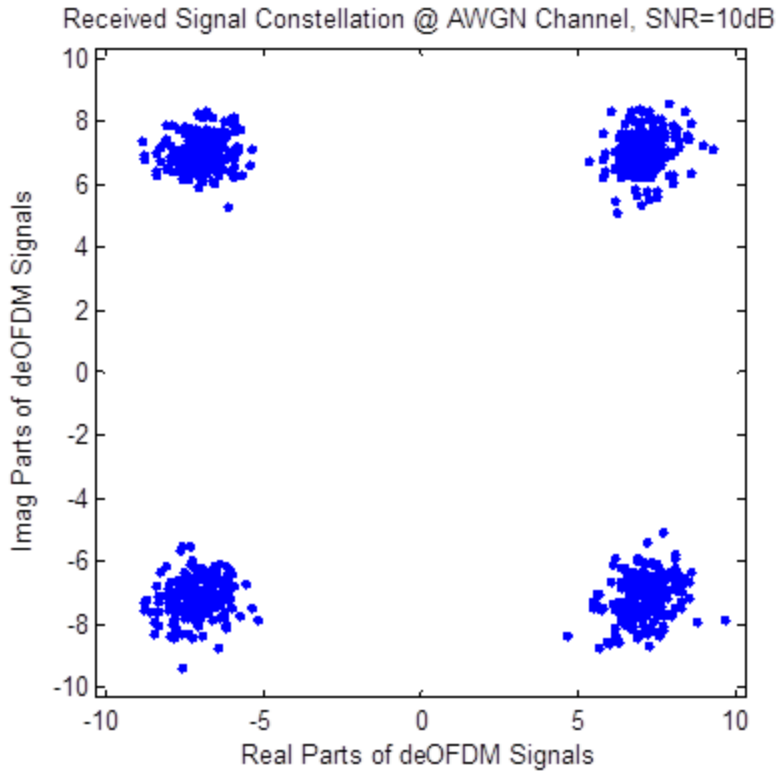


Figure 6.6 Constellation of the received signals for AWGN Channel at 10 dB SNR.

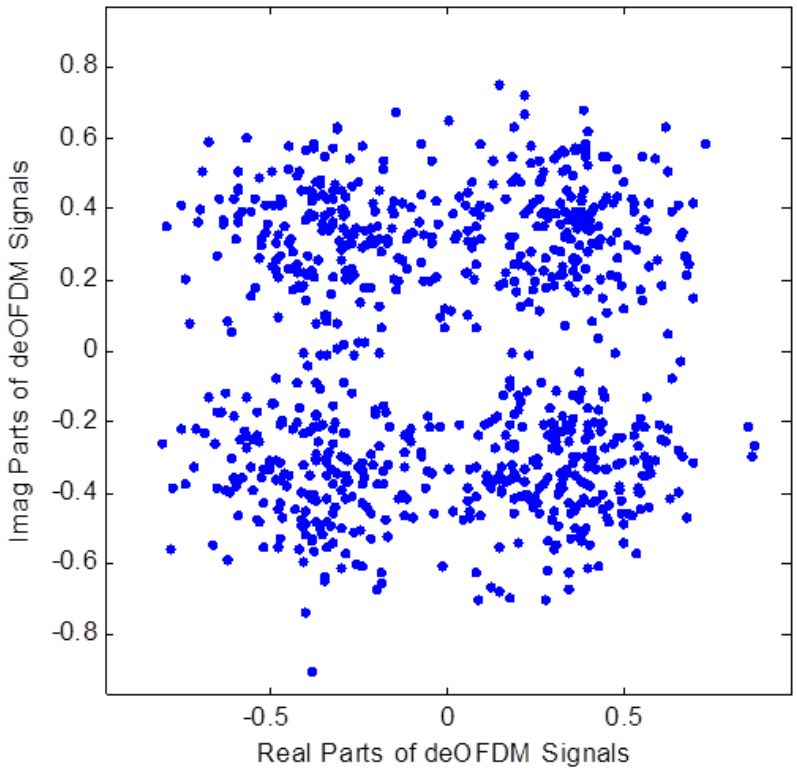


Figure 6.7 Constellation of the received signals for WIIC Channel at 3 dB SNR.

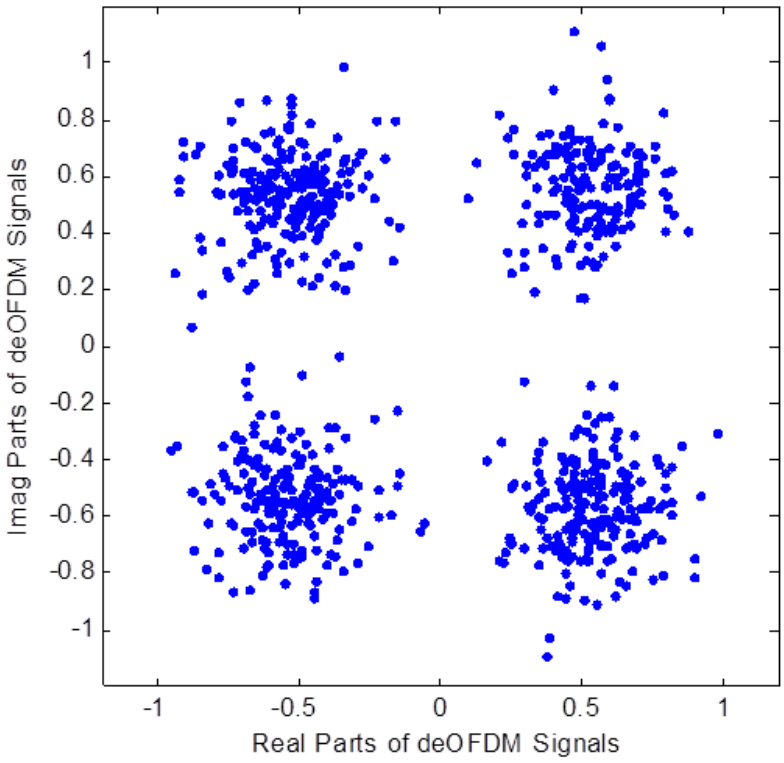


Figure 6.8 Constellation of the received signals for WIIC Channel at 5 dB SNR.

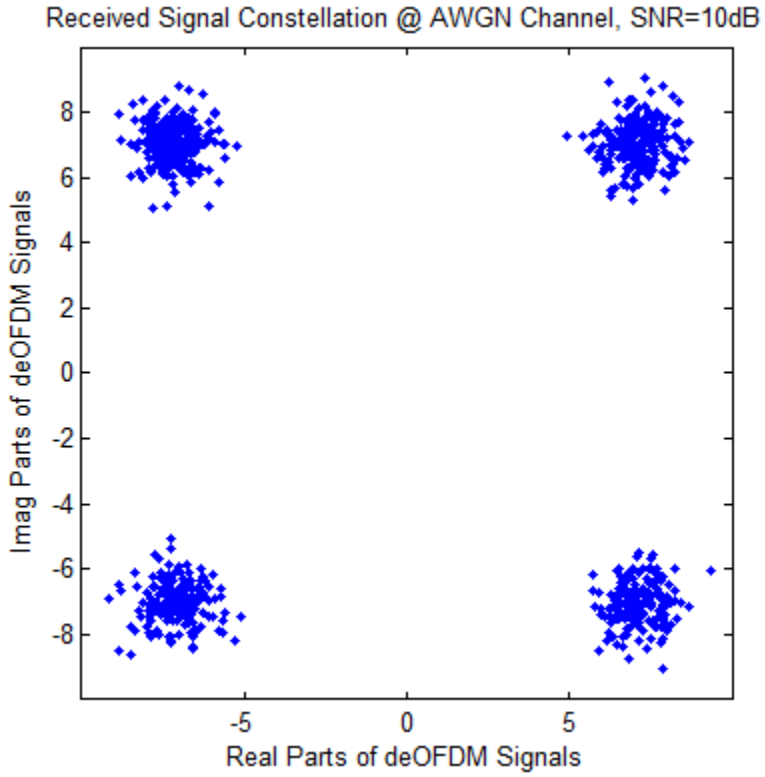


Figure 6.9 Constellation of the received signals for WIIC Channel at 10 dB SNR.

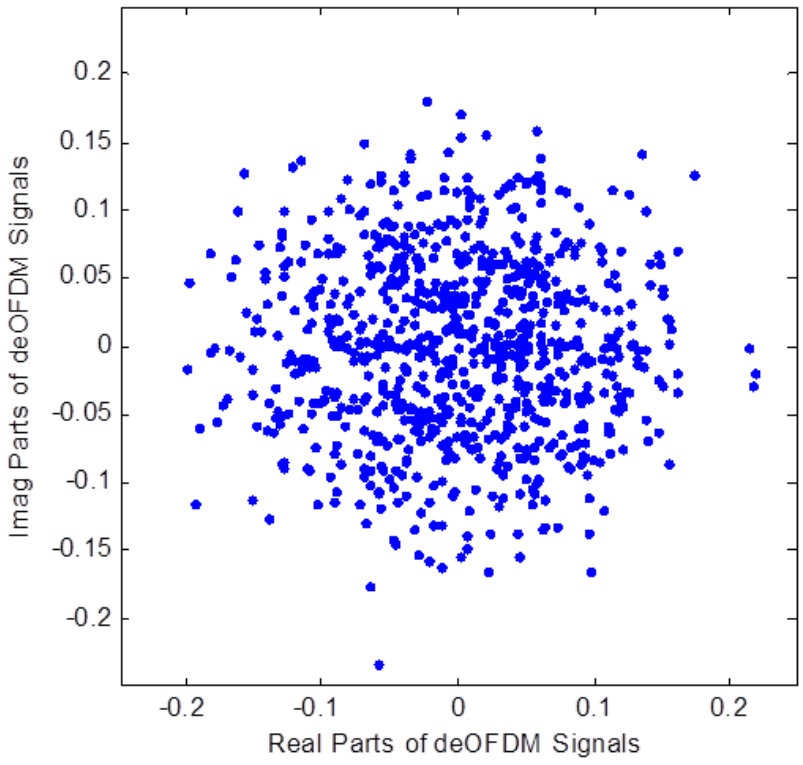


Figure 6.10 Constellation of the received signals for the wired PCB Channel at 3 dB SNR.

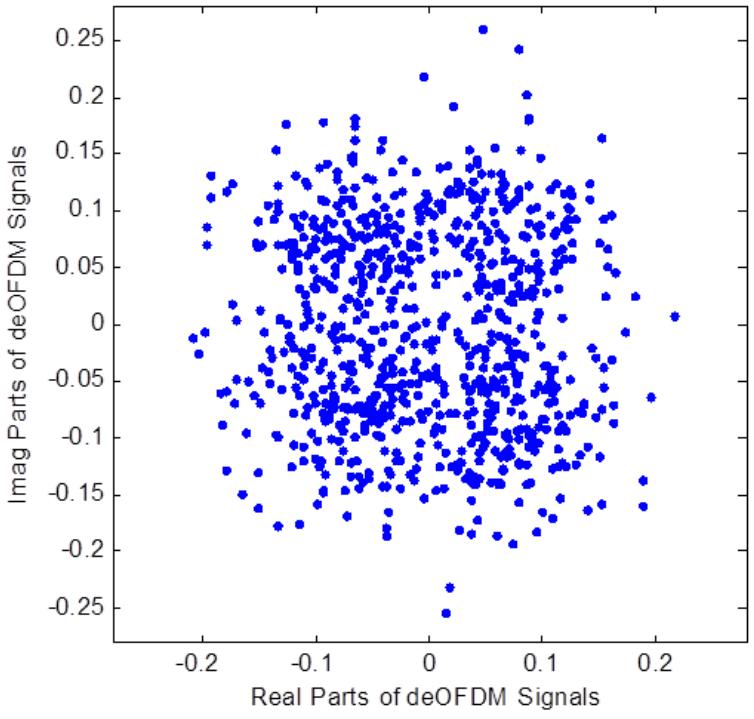


Figure 6.11 Constellation of the received signals for the wired PCB Channel at 5 dB SNR.

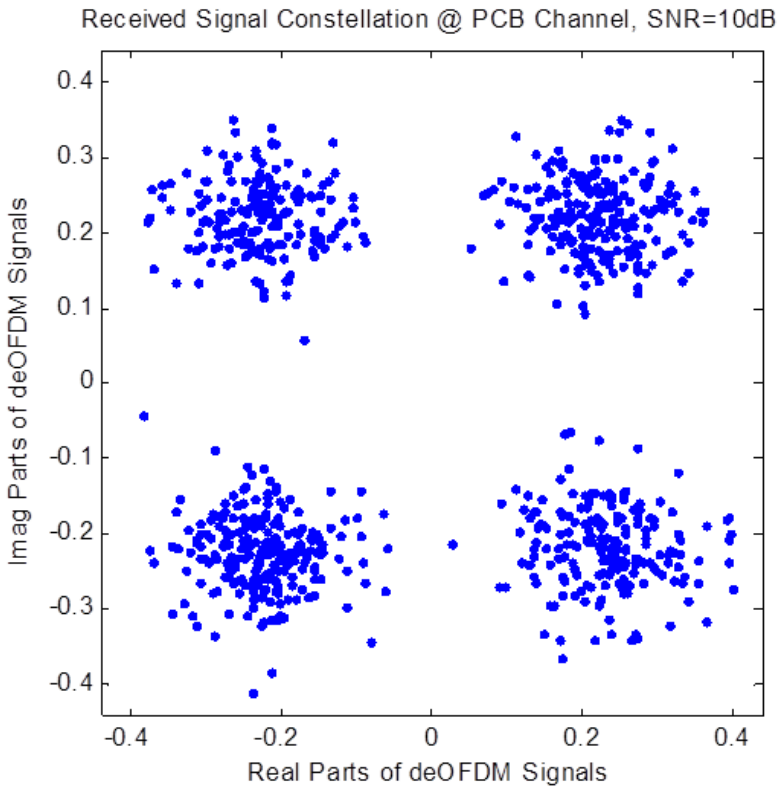


Figure 6.12 Constellation of the received signals for the wired PCB Channel at 10 dB SNR.

6.2.2 BER Simulation

With the full modules of the designed WIIC system, a BER simulation has been performed. The simulated BER vs. SNR for the AWGN with FEC, WIIC and the PCB channels are shown in Figure 6.13.

The AWGN channel with FEC refers the WIIC system with FEC included in an AWGN channel, and the WIIC Channel-Absorber is the WIIC system with equalization simulated with the WIIC channel bounded by the absorber layers. In the simulation, equalized AWGN channels provide the best case for wireless channels, which can not only validate the designed system, but also can be compared to the WIIC channel and wired PCB channels.

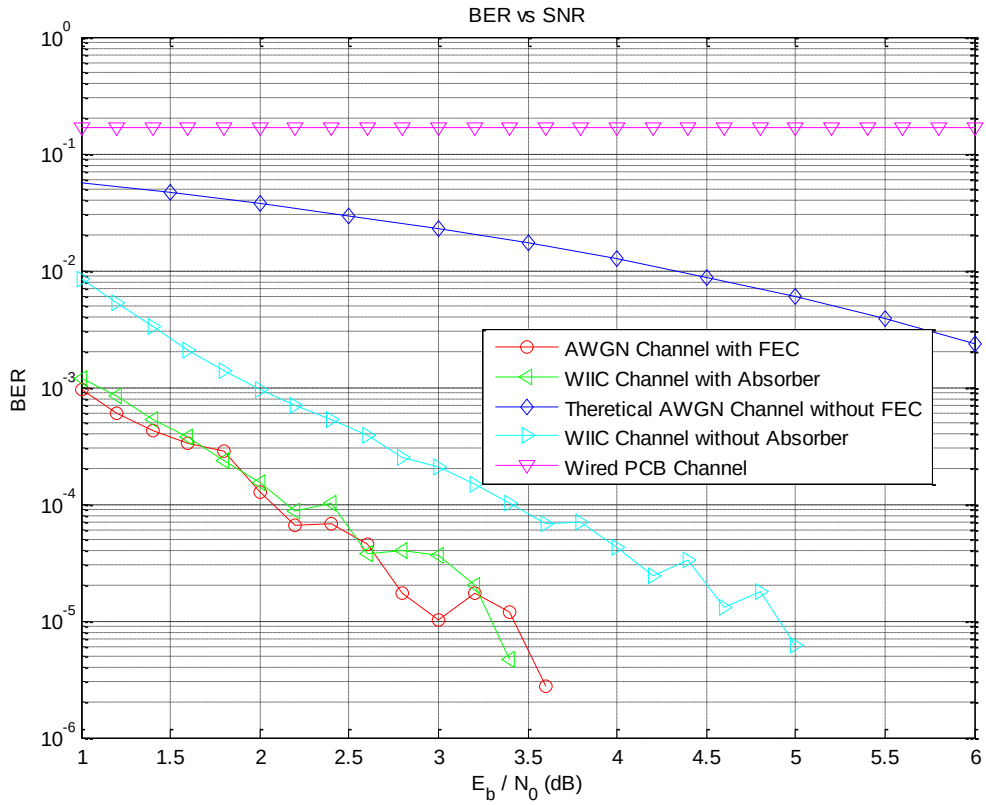


Figure 6.13 BER vs. SNR when using channel coding, estimation and equalization.

As seen from figure 6.13, the BER reaches a value less than 10^{-5} at SNR of 3.4 dB for both AWGN with FEC and WIIC channels, respectively. In contrast, it is not surprising that the BER for the wired PCB channel is much higher than the other channels due to its cutoff characteristics in the frequency band of interest.

By a comparison to Figures 6.3 and 6.13, it is obvious that the designed system with FEC, RS channel sounding, channel estimation and channel equalization can obtain much lower BER than the preliminary system without these features.

In the proposed WIIC system, it is possible to achieve a much higher SNR at 20 or 30 dB with higher-gain LNAs. In this case, higher-order modulation methods,

including 64QAM, 128 QAM or even higher could be employed in the proposed WIIC system, without increasing the BER, at the expense of larger power dissipation.

It is observed that the current wired PCB channel is not suitable for the transmission of digital signals at the frequency of 15 GHz or higher due to signal integrity issues, such as crosstalk, parasitic inductance and capacitance, power loss, and distortion. It is expected that the SI issues will become much severe in the 60 GHz band. It is found that the designed wireless channel could be potentially a solution to such SI problems.

CHAPTER 7

CONCLUSION AND FUTURE WORK

7.1 Summary of the Research

A complete WIIC system and channel have been simulated in MATLAB in conjunction with ADS and HFSS. The proposed WIIC system includes FEC, QPSK/QAM modulation, packet header, RS channel sounding, channel estimation, channel equalization, and OFDM with CP. The WIIC channel contains two layers of the designed EBG absorbing units operating at the frequency band centered at 60 GHz. In particular, the research of this dissertation is summarized by the following points:

- **Comparison of the WIIC Technologies.** First, currently wired PCB systems, previous WIIC systems, and wireless optical communication on-chip were discussed for comparison to the proposed WIIC communication system. Obviously, the current wired PCB systems are not able to transmit signals operating at the center frequency of 60 GHz for the case investigated.
- **WIIC System Analysis and Design.** Second, the WIIC system has been shown by simulations to enable wireless communication at the center frequency of 60 GHz. In order to enhance the reliability and the BER performance for the proposed WIIC system, CRC checking, channel coding, channel estimation, and channel equalization are included in the system. In the simulation results, it was shown that RS channel sounding, channel coding, channel estimation and channel

equalization can significantly improve performance as measured by BER. So as to increase the data rate and spectrum utilization for the proposed WIIC system, the QPSK modulation method, and OFDM technologies are employed in the proposed system. In comparison to the previous WIIC systems, the proposed WIIC channel in this dissertation is able to provide much higher spectrum utilization.

- **Design of WIIC Propagation Channel Models.** Third, a practical WIIC channel has been designed and a model for the channel developed by using HFSS. One WIIC channel is simply designed by using a parallel metal plate waveguide which performs as both the ground planes and the microwave leakage preventer. Another innovative WIIC channel structure is designed with two metamaterial EBG microwave absorber layers implemented at the top and bottom positions of the PCB board. The simulated results show that, the WIIC channel with the absorbing layers can provide less than 10 dB return loss and relatively flat insertion loss within the designed frequency band in the range of 50 through 70 GHz.
- **Measurement of a Wired Channel on PCB Boards.** Furthermore, the TDR and TDT signals of a representative wired PCB channel have been measured. S-Parameters were derived from the TDR/TDT results using the FFT. With the structure of the wired PCB channel, the vias and through hole pins were designed and simulated in HFSS with the obtained S-Parameters. The microstrip lines and striplines were designed in ADS. Along with the simulated S-Parameter models as sub-circuits as well as the S-Parameters of the connectors provided by the connector vendor, the system TDT, TDR, and S-Parameters were simulated in

ADS. The measured and simulated results of TDR, TDT and S-Parameters were shown to be consistent. As seen from the S-Parameters of the wired PCB channel, it was concluded that the current transmission-line technology on PCB boards for the case investigated herein is not able to transmit high frequency signals at 60 GHz.

- **Simulation of the WIIC System.** Finally, the designed WIIC communication system with all the processing listed above was simulated in MATLAB. The BER performance in different channel models was obtained. The AWGN channel provided validation for the system design. It was shown that the WIIC channel system is able to properly decode the received bit stream, with a BER less than 10^{-5} at 3.4 dB SNR, in the frequency band centered at 60 GHz. The BER result is similar to the AWGN channel with FEC, which means the designed system achieved almost perfect equalization in the WIIC channel.

The BER analysis shows that the performance of the designed WIIC channel with the EBG absorbing layers is close to that of the AWGN channel with FEC, when channel coding, channel estimation and equalization are employed.

7.2 Future outlook of the Research

It is likely that the WIIC systems will have a very promising future within the next decade. In principle, it should be straightforward to place the WIIC DSPs on PCB boards. The WIIC DSPs require a smaller amount of power and board area consumption, and have a lot design freedom in comparison to the conventional Intel CPUs. The systems and channels are able to provide high-speed and high data rate transmission at high frequency bands.

In the foreseen future, it is believed that the WIIC systems will be gradually taking the place of some parts of the wired PCB boards because of its great features in terms of reliability, simplicity in design and implementation, higher data rate, and better spectrum utilization.

7.3 Future work of the Research

The potential future research is considered to be extended to the following five areas:

- **Antenna Array and Further WIIC Channel Design with Metamaterial Absorbers.** First of all, the proposed WIIC channel integrated with antenna array system will be optimized in order to achieve an optimum antenna array configuration for obtaining a higher array gain, enabling spatial interference suppression. In the process of design, the analysis of RF system should account for mutual coupling between the antenna elements in the array, and RF characteristics of all coupled wired or wireless WIIC sub-channels. Another new design for the WIIC channel is to add the absorber layers to the entire four side walls if the cost is allowable, while keeping the absorbing ground planes at the top and bottom layers.
- **ASIC Design and Analysis for OFDM and High Order Modulation.** Second, design of ASICs will be further studied for the applications of OFDM, high order modulation, channel sounding, estimation and equalization. The power consumption, the required SNR, the link budget, and the complexity of the system brought by QAM and OFDM would need to be analyzed. The transmitter power amplifier must be carefully designed, and the advantages of QAM and OFDM,

including the data rate and performance increment, will be balanced by the power and chip area consumption. If the cost is acceptable, the ASIC circuits for WIIC system could be designed and improved so as to outperform the DSPs in terms of BER performance, total power as well as board area consumption.

- **Fabrication and Measurement of the Designed WIIC Channel with Metamaterial EBG Absorber Layers.** Third, the proposed WIIC channel with the metamaterial EBG absorber layers should be fabricated and measured, with all the parameters and the dimensions of the absorber units, the dielectric substrate, and the micro-antennas with LNAs optimized. The fabricated channel should also be measured to obtain its S-Parameters. The impulse response and transfer function can be extracted, which will be compared with the simulation results from this dissertation.
- **Implementation of the Designed WIIC System with all Functional Blocks.** Fourth, the designed WIIC system could be implemented on the same PCB board of the manufactured WIIC channel. The system would be manufactured with either DSPs or the designed ASIC circuits, whichever is found to be better in performance, power and board area consumption.
- **System Validation and Functional Test and Optimization.** Furthermore, the manufactured WIIC system on the PCB board should then be tested. If warranted, the automatic repeat request (ARQ) technique could also be employed to improve BER performance after the physical layer performance is characterized.
- **Industrial Standard of the WIIC Channel and System.** Finally, when the proposed WIIC system and channel with metamaterial EBG absorber layers are

fabricated, measured and ready to be applied to the PCB boards, the simulation and measurement results could be provided to relevant industries and communities for standard or specification development.

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APPENDIX A – TIME DOMAIN REFLECTOMETRY AND TIME DOMAIN TRANSMISSION

Time domain Reflectometry (TDR) and time domain transmission (TDT) can be measured by injecting a step signal into port 1 for a device under test (DUT), and the transmitted signal at port 2 is defined as TDT, whereas the measured signal at port 1, which is the total wave including the reflected and incident waves, is called TDR. The principle of TDR and TDT measurements and the time domain reflectometer are demonstrated in Figures A.1 and A.2, respectively.

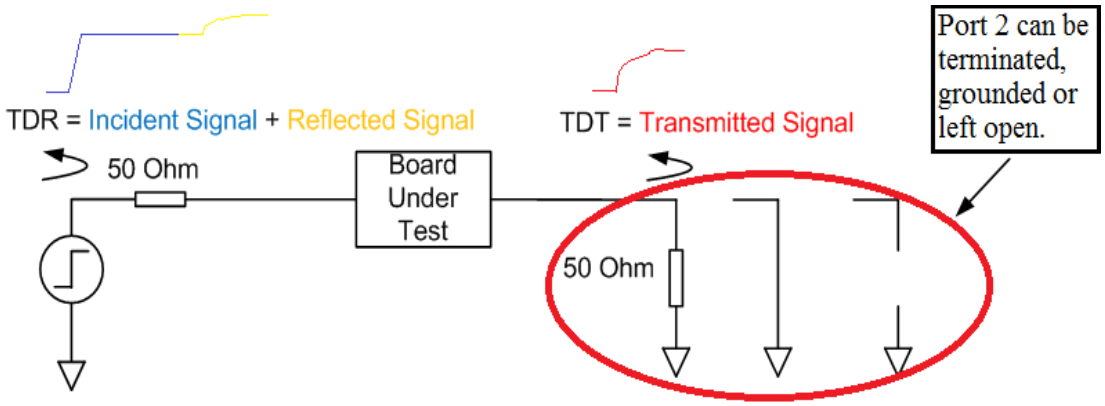

Figure A.1 The principle of TDR and TDT measurement.

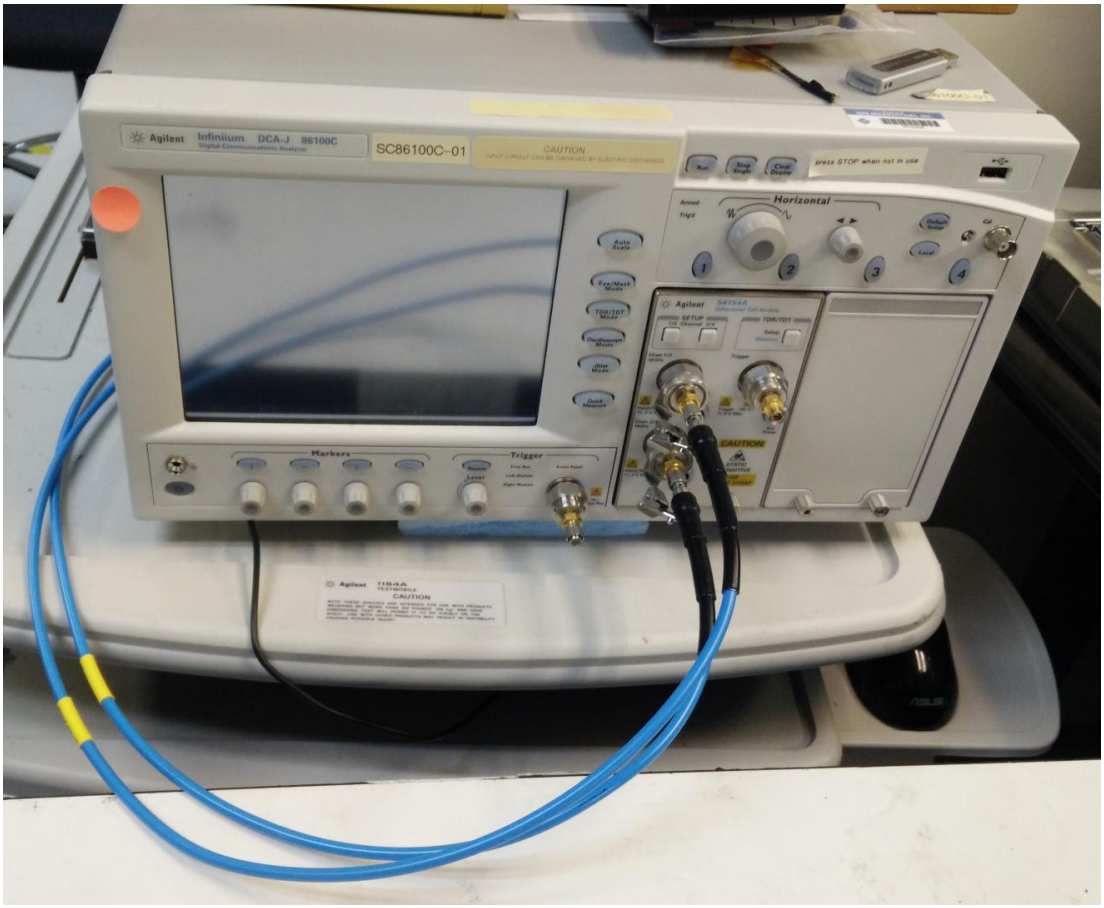

Figure A.2 Time domain reflectometer.

In TDR/TDT measurement, port 2 can be terminated, grounded or left open, which will influence the final values of the TDR/TDT results. The terminated cases include matched termination, and mismatched termination. The different TDR results among these four terminations are shown in Figure A.3.

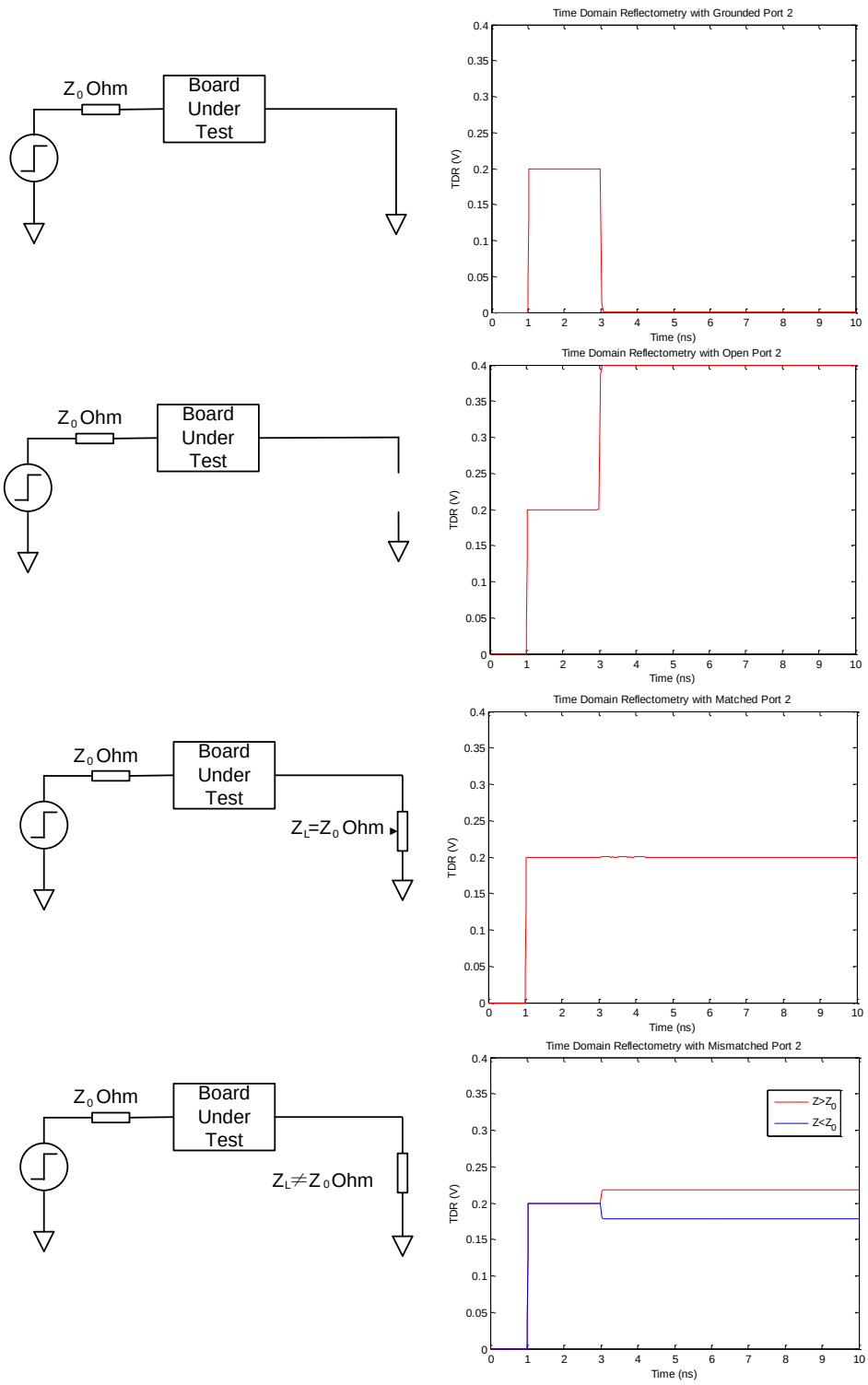

Figure A.3 Different TDT results for different terminations.

TDR is usually used for examining the characteristic impedance of the DUT, which is calculated from the measurement for the sum of the injected and reflected signals, and TDT is actually the step response that can express the characteristics of the channel. They are given as follows:

$$TDR = V_r + V_i \tag{A.1}$$

$$TDT = V_t \tag{A.2}$$

where V_i, V_r, and V_t are the incident, the reflected, and the transmitted signals.

If the characteristic impedance of a transmission line is unknown, it can be measured by connecting it to another transmission line with the given characteristic impedance Z_{ref} . Because the reflection co-efficient between two mismatched transmission lines is defined as [6]:

$$\rho = \frac{V_r}{V_i} = \frac{Z - Z_{ref}}{Z + Z_{ref}} \tag{A.3}$$

where Z is the characteristic impedance of the unknown transmission line, and Z_{ref} is the characteristic impedance of a transmission line. As a result, the measured characteristic impedance can be derived as:

$$Z = Z_{ref} \frac{1+\rho}{1-\rho} \tag{A.4}$$

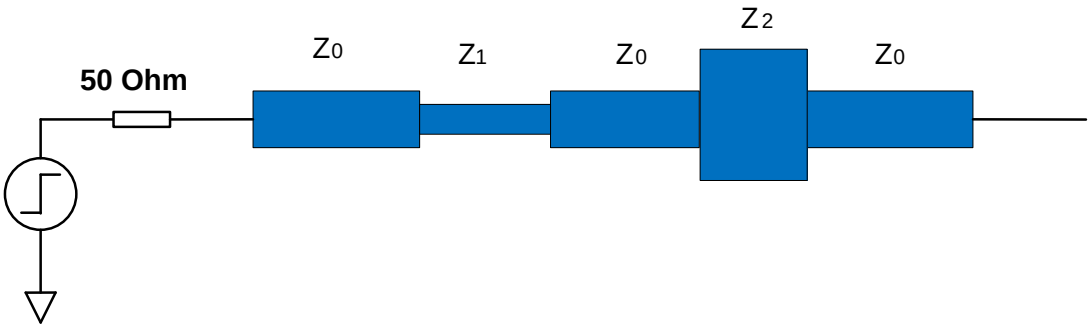

Figure A.4 TDR measurement example.

In Figure A.4, the characteristic impedance of Z_0 is known, and the characteristic impedances of Z_1 and Z_2 remain unknown. The relationship between the measured TDR signals and the characteristic impedances of the five segments of transmission lines is displayed in Figure A.5. From Figure A.5, the characteristic impedances of Z_1 and Z_2 can be calculated and displayed.

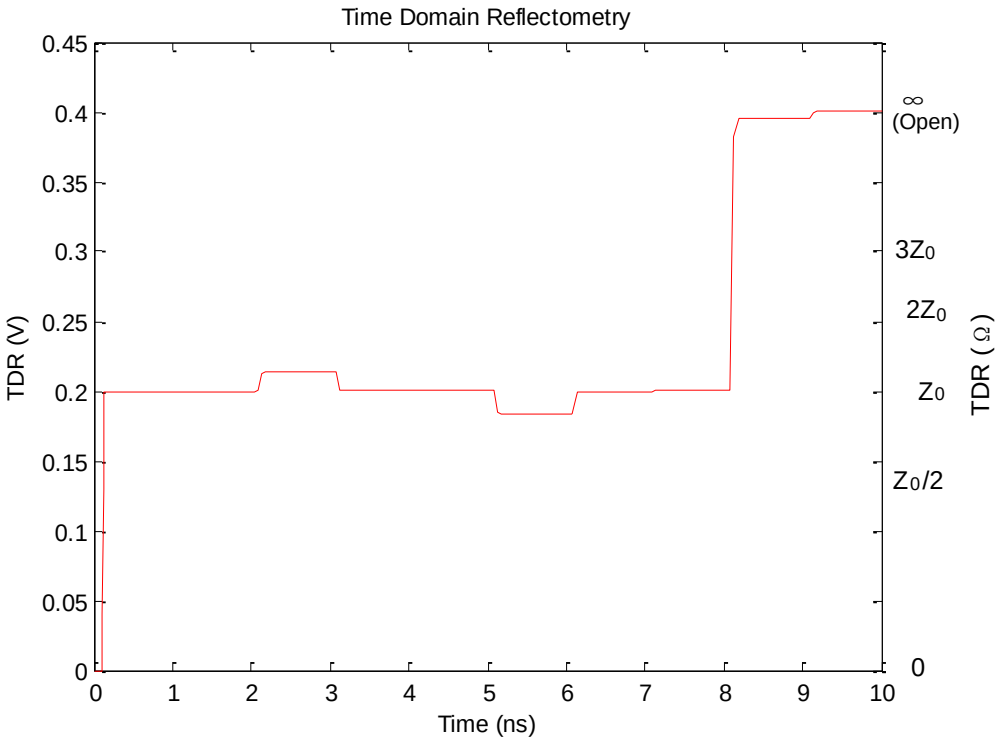

Figure A.5 Relationship between TDR measurement result and calculated characteristic impedance.

Besides the examination of the variation of characteristic impedance along the transmission line, TDR is also able to determine that the round-trip delay of each segment. The delay on the TDR measurement is the round-trip delay of each partial transmission line. With the unit delay of each portion of the trace, it is simple enough to find the length of the corresponding segment. For instance, when a fixed telephone line is down, the telecommunication operators will use TDR to compute the distance between the broken point and the TDR device, and then the potentially broken places of the long-term

transmission line will be determined, which can save the engineers weeks before they finally find out the actual places of the broken down electronic equipment or transmission line.