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THE ROLE OF INTERFACE EFFECTS AND MINORITY CARRIERS IN THE METAL-SEMICONDUCTOR SCHOTTKY JUNCTION

by

Sabih Uddin Omar

Bachelor of Science
Bangladesh University of Engineering and Technology, 2009

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Accepted by:

MVS Chandrashekhar, Major Professor

Tangali S. Sudarshan, Committee Member

Grigory Simin, Committee Member

Andrew B. Greytak, Committee Member

Lacy Ford, Vice Provost and Dean of Graduate Studies

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DEDICATION

To my parents, my wife, my sister and brother-in-law and my lovely nieces.

I found y'all in the vastness of the universe and the immensity of time,

and that is wonderful!

ACKNOWLEDGEMENTS

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Last, but not the least, I am truly grateful to my wife, Aniqua, for having patience with me, and keeping up with my offbeat work hours and deadline-frenzy. I hope I will make up for all these sometime in future.

ABSTRACT

The metal-semiconductor (MS) Schottky barrier junction, formed by putting a metal in contact with a semiconductor crystal, is the simplest form of electronic rectifier. Despite the simple structure, the MS junction shows a variety of anomalous electrical characteristics. The non-ideality is generally described as a linear bias-dependence of the energy barrier height at the MS junction, quantified by an ideality factor. As the physical origin of this bias-dependent barrier height, the presence of various interface effects, such as the Schottky barrier inhomogeneity, interface trap states and morphological defects, have been proposed. However, there is no consensus among the researchers about the extent to which each of these interface anomalies effect the ideality of the junction.

Another intriguing aspect of the Schottky junction is its ability to inject minority carriers under certain conditions, as was demonstrated by the early works in the 1940s (e.g., the point contact transistor). However, the lack of physical understanding of this phenomenon, combined with poor reproducibility and the development of the p-n junction, inhibited technological progress of Schottky bipolar emitters. In recent years, the development of new material technologies, such as epitaxial graphene, has opened up possibilities for novel bipolar mode Schottky devices, reviving the interest in the theory of minority carrier injection in Schottky junctions.

In this study, the role of non-ideal interface effects and minority carrier injection on the transport properties of the Schottky junction interface are explored in relation to experimental observations made in silicon carbide Schottky interfaces. Silicon carbide (SiC) is an indirect wide band gap material with electronic and thermal properties suitable for high power, high temperature and high frequency electronic applications. The electronic applications of SiC electronics include high power systems such a hybrid/electric vehicle and smart grid systems as well as high sensitivity sensors, such as nuclear radiation detectors. Many of these applications require large barrier Schottky junctions, which are obtained by using large work function metals, such as nickel (Ni) and platinum (Pt).

As the Schottky junctions are formed on the surface of the semiconductor crystal, the crystal quality, and especially the surface characteristics are important regulators of the Schottky device performance. In this work, the epitaxial growth of 4H-SiC by CVD was optimized using dichlorosilane, a halogenated reactant gas as the silicon precursor. Large barrier (> 1.6 eV) Ni/4H-SiC Schottky contacts were fabricated on lightly doped n-type SiC epitaxial layers. The as-deposited diodes showed non-ideal characteristics, Rapid thermal annealing of the contacts at > 650^{o}C improved the diode ideality.

In this dissertation, the Schottky barrier inhomogeneity in the as-deposited diodes is studied using Tung's inter-acting barrier model. It is shown that the Tung model was not applicable for the highly non-ideal (n > 1.2) Schottky junctions. Rather, it is argued that interface trap states are responsible for the high level of non-ideality based on the observation of hysteresis patterns in the I-V and C-V characteristics. The trap density is estimated at 10^{8}~10^{10} cm^{-2} from the hysteresis results.

In a parallel effort, the very large barrier (Φp ~2.6 eV) Schottky heterojunction between epitaxial graphene (EG) and p-doped SiC was studied in this work for its potential in sensing applications. Surprisingly, the junction showed the capability of high efficiency (> 99%) minority carrier injection. The theories of minority carrier injection in MS junctions are re-visited in this dissertation for explaining this result. It is shown analytically that highly efficient minority carrier injection is possible in large barrier Schottky junctions under a high injection level. An EG/p-SiC/n-SiC photo-transistor structure was developed that showed a bipolar gain in the order of 10^2 and a responsivity of 10^1~10^2 A/W under UV illumination. The bipolar EG/SiC Schottky junction, therefore, opens up unique possibilities in radiation detection and power switching applications.

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LIST OF ABBREVIATIONS

DAP ..... Donor-acceptor pair

DCS ..... Dichlorosilane (SiH_2Cl_2)

EBIC ..... Electron beam induced current

EG ..... Epitaxial graphene

MS ..... Metal-semiconductor

PL ..... Photoluminescence

QNR ..... Quasi-neutral region

SCR ..... Space charge region

TFS ..... Tetrafluorosilane (SiF_4)

CHAPTER 1

INTRODUCTION

The metal-semiconductor Schottky junction is a solid-state rectifier of electric signal, i.e., it allows electric current to flow in one direction and blocks in the other. The rectification property of such junctions was discovered as early as the late eighteenth century. These early Schottky junctions were formed by putting metal whiskers or point contacts on the semiconductor surface. The point contact junction found widespread use in crystal radio receivers, and later led to the invention of the point contact transistor in the 1940s. However, the lack of controllability and reproducibility of the point contact junction prompted the development of semiconductor p-n junctions around the same time. Despite a rapid improvement in metal deposition techniques and realization of large area contacts, the reproducibility of the Schottky behavior remained an issue. As a consequence, with the advent of p-n junctions, the application space of Schottky devices shrunk by a considerable degree. Nevertheless, Schottky devices found application in electronic systems requiring high speed of operation and low power loss, such as power switching, radio frequency (RF) electronics, non-volatile memory and sensor devices.

The conduction mechanism in the Schottky junction has intrigued the researchers for over a century, and some aspects of it, remains unresolved till this day. The electrical conduction properties in a Schottky junction are generally described by the field-enhanced thermionic emission of carriers from the semiconductor material, commonly

known as the Schottky effect. However, the electrical characteristics of Schottky devices often deviate from the ideal thermionic emission behavior. Various non- ideal effects with varying degrees of impact on device characteristics have been identified in different metal-semiconductor junction systems. These effects range from physical interfacial anomaly such as charge capture centers and Schottky barrier inhomogeneity at the metal-semiconductor junction to drastically different current transport mechanisms owing to the barrier characteristics, such as quantum-mechanical tunneling of carriers through the barrier or minority carrier injection effects.

While the modeling of tunneling or minority carrier transport needs unique formulations, the interface anomaly effects, such as interface traps and inhomogeneity can be explained by extending the basic thermionic emission model to incorporate the non-ideality. A number of such theories (or extensions to the basic theory) exist, as will be discussed in detail in Chapter 2. These theories range from empirical to strictly theoretical, and not every one of them provides a sound qualitative understanding. Above all, the conditions for the applicability of each theory are not well understood.

In this dissertation, the non-ideal effects in silicon carbide Schottky junctions are studied and the roles of the anomalous interface effects as well as minority carrier injection are explored analytically and experimentally. For the experimental study, large barrier Schottky junctions to silicon carbide, a wide bandgap material, were used.

1.1 MOTIVATION OF THE CURRENT STUDY

The last couple of decades saw a rapid development of wide bandgap compound semiconductors such as SiC and GaN as viable materials for high power and high speed electronics. These novel material platforms open up possibilities for novel Schottky

device applications such as power Schottky or junction barrier diodes, as well as MESFETs and HEMTs, that employ the MS junction as the gate. As each material system has its unique characteristics, and poses unique challenges to any device implementation, each new material system brings about an opportunity to re-visit the unresolved aspects of the Schottky conduction theories, as well as the non-ideal effects observed in their electrical characteristics.

In this work, we focus on the transport characteristics in high barrier silicon carbide (SiC) Schottky junction diodes. SiC is a wide band gap semiconductor that shows promise as a post-silicon material technology for high power, high temperature, and harsh environment electronic applications. All these capabilities come from the excellent material properties of SiC (Appendix-A). As shown in Fig-1, 4H-SiC shows a 3x band gap, a 10x break down electric field, a 3x thermal conductivity, and a 2x saturation velocity as compared to silicon. In power devices, these values translate into higher breakdown voltage, lower loss, higher speed and higher temperature operation.

The high barrier SiC schottky diodes are technologically important, as these devices show better or comparable performance as Si p-i-n junction diodes in the > 1 kV application space. The large barrier height allows SiC Schottky to operate in the application range of Si p-i-n diodes. The low reverse recovery time and the low forward voltage drop inherent in the Schottky design is expected to provide lower power loss, lower current transient and faster switching for SiC Schottky diodes, and system level

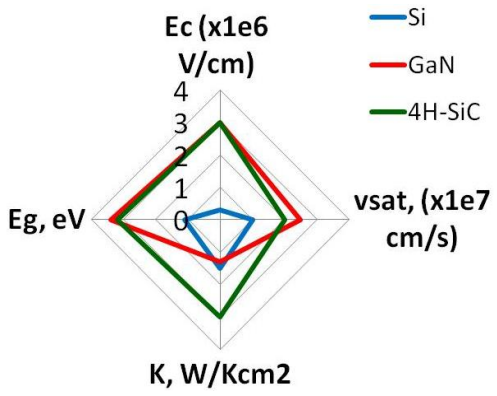

Figure 1.1 Power semiconductor properties. A comparison of important material properties of the three contending power electronic materials— Si, 4H-SiC and GaN. The parameters shown are band gap (E_g), electric field (E_c), electron saturation velocity (v_{sat}) and thermal conductivity (K).

experimental results corroborate this theoretical prediction [1][2][3]. Moreover, the positive temperature coefficient of resistivity in SiC epitaxial layers enables parallel operation of SiC diodes, which is not available in Si power devices.

Power electronic applications, however, put a stringent requirement on the reliability and reproducibility of the devices. The major reliability issue in SiC power devices is the edge breakdown, which can be mitigated by an optimized edge termination design. On the other hand, the reproducibility issue arises primarily from the non-uniform distribution of morphological defects across the wafer as well as the spatial inhomogeneity of the junction barrier height. To avoid these problems, typically a merged pin-Schottky design is employed, in which the high power blocking is performed by the lateral pinch-off of the p-n junction surrounding the Schottky active area. However, this leads to new reliability issues, such as defect induced forward voltage drift caused by bipolar injection[4] and electro-migration of aluminum contact on the p-region during high voltage switching [5]. A reproducible Schottky contact fabrication process

can, therefore, have a significant impact on the adoption of SiC devices at the system-level.

Apart from power electronic applications, SiC is an ideal semiconductor for fabricating high sensitivity detectors, owing to its low intrinsic carrier concentration and the capability to withstand harsh environment like high temperature and high dose of radiation. SiC Schottky junctions have been employed in gas sensing and radiation detection applications, and showed high responsivity values[6][7][8][9].

An added advantage for SiC is that by the thermal decomposition of its crystal surface, a few-to-monolayer epitaxial graphene film can be grown, which forms a Schottky heterojunction with the underlying SiC. Graphene is a two-dimensional allotrope of carbon with unique physical properties that make it an attractive candidate for the future nano-scale electronics. Graphene is attractive for sensing applications too, as the low dimensionality of graphene renders it highly sensitive to external stimulation, while its universal transparency makes it an ideal radiation window. The Schottky junction between graphene and SiC, therefore, renders a unique opportunity of fabricating SiC-based sensors and detectors with unprecedented responsivity.

As can be inferred from the discussion above, the common requirement for both power and sensor applications is a reproducible and reliable Schottky junction. It is, therefore, important to understand the non-ideal effects in the current transport characteristics in these junctions, as these need to be eliminated or controlled for reliable device performance. The engineering goal of this study is to identify the sources of the non-ideality in the electrical performance of the Schottky junction, while finding means to capitalize on the non-ideal effects. However, the nature of the study (and the generous

indulgence of the PI) allows the author to explore the non-ideal behavior from a broader perspective, and draw conclusions that are applicable across material platforms.

1.2 OUTLINE OF THE DISSERTATION

The current study spans the entire fabrication process of the Schottky diodes, starting from the epitaxial growth of SiC crystals to the Schottky contact formation and characterization. The presentation of the results follows the order of the process. However, each chapter is independent from the rest, and can be read out of order. The organization of the dissertation is as follows—

Chapter 2 provides a brief overview of the historical development of the theory and experimental practices in metal-semiconductor Schottky diodes, and identifies the open questions in the field.

Chapter 3 describes the epitaxial growth process of device-grade silicon carbide (SiC) crystal for Schottky junction formation. The step-flow growth mechanism using a chlorinated silicon precursor is discussed in some detail. Also, a novel non-destructive technique of defect characterization is introduced.

Chapter 4 provides a discussion on the fabrication of nickel-SiC Schottky diodes with near-ideal, reproducible characteristics. The non-ideality of the as-deposited are studied in detail and the modern theories of non-ideality are re-examined for their applicability range.

Chapter 5 re-visits the theories of minority carrier injection in large barrier Schottky diodes, and attempts at a generalized formulation of the various concepts related to the phenomenon. Efficient minority carrier injection is demonstrated in the epitaxial

graphene/SiC Schottky heterojunction. The fabrication and characterization of a graphene/SiC heterojunction bipolar phototransistor (HBPT) is also discussed in this chapter.

Chapter 6 summarizes the (humble) contributions of this work in understanding the non-ideal behaviors in Schottky junctions, and proposes future directions of investigation.

CHAPTER 2
FUNDAMENTALS OF METAL-SEMICONDUCTOR SCHOTTKY BARRIER JUNCTIONS

2.1 A BRIEF HISTORY OF SCHOTTKY BARRIER JUNCTIONS

Metal-semiconductor Schottky junction devices have been around for over a century. The first observation of the rectification property of metal semiconductor junctions dates back to 1874. F. Braun, a German physicist, showed that the sulfides of various metals showed uni-directional flow of current when contacted with fine metal whiskers[10], known as the cat's whisker or the point contact. About two decades later, J. C. Bose reported the capability of the detector to pick up millimeter waves [11], followed by a US patent by G. W. Pickard on a radio receiver based on the point contact [12]. The cat's whisker detector made its way into radio transmission and reception systems as a replacement of the even more unreliable and power-hungry vacuum tubes. However, the unreliable nature of the contact made the arrangement really difficult to work with. Nevertheless, Braun received the Nobel Prize in Physics in 1909 along with G. Marconi.

The demand for high frequency communication during the World War II prompted a flurry of semiconductor research in the USA. High purity silicon and germanium crystals were prepared, and doping techniques were explored. Soon the unreliable point contact rectifiers were replaced by the fixed contact germanium diodes

[13]. In 1947, the quest for a field-effect transistor led the Bell Labs scientists J. Bardeen and W. Brattain to the fortuitous invention of the point contact transistor. Puzzlingly, the transistor action showed significant minority carrier injection through a metal-semiconductor point contact junction, which was generally considered a majority carrier device. Bardeen attempted to explain the result by assuming the formation of an inversion layer at the metal-semiconductor junction [14]. However, Shockley et al. and Shive argued that the minority carrier penetrates the bulk of the crystal, and demonstrated transistor action with contacts put on opposing sides of the crystal [15][16]. The concept was expanded to large area contacts and Schottky junction transistors were demonstrated by several researchers [17][18][19]. However, the development of more robust and controllable p/n junction transistors rendered the metal-semiconductor point contact transistor obsolete within a decade. The point contact rectifiers, on the other hand, gave way to large area Schottky contacts deposited by painting, electroplating or thermal evaporation.

In the next section, a brief overview of the Schottky junction theories is provided. The theories encompass Schottky barrier characteristics, current transport mechanism, interface effects and Schottky barrier inhomogeneity.

2.2 THE SCHOTTKY JUNCTION THEORY

2.2.1 The barrier formation: the Schottky-Mott limit

Although the rectification property of Schottky junctions was discovered in 1874, the theory took a considerable time to take shape. The advance in quantum mechanics in the 1920s helped the scientists to have a realistic picture of the atom and the electrons in

it. It was obvious that the conduction across the Schottky interface occurred through electrons overcoming the surface energy barrier, quantified by the work function. The works of Schottky, Mott, Bethe and Davydov[20][21][22] showed that the current in a Schottky junction followed a field enhanced thermionic emission mechanism, described as—

$$J = A^{*}T^{2}\exp\left(\frac{-q\varphi_{bn}}{kT}\right)\left\{\exp\left(\frac{qV}{kT}\right)-1\right\} \tag{2.1}$$

Here, φ_{bn} is the barrier height, T is the temperature and V is the junction voltage. A* is the Richardson constant, a parameter intrinsic to the interface, and defined as $4\pi q m_n^{*} k^2 / h^3$, where m_n* is the effective mass of electrons in the semiconductor, k is the Boltzman's constant and h is the Planck's constant.

The energy band diagram of the system is shown in Fig-2.1. As the metal comes in contact with the semiconductor, the Fermi level (average energy of electrons) in the two metals tend to align. The band alignment requires a reduction in the electron density from the semiconductor surface, which forms a space charge region (SCR) of width W at the semiconductor surface. This causes an upward band bending on the semiconductor side, creating a potential barrier at the interface. As can be seen from Fig-2.1, in n-type semiconductor the barrier formation at the interface requires a metal workfunction (Φ_m) greater than the electron affinity (χ) of the semiconductor. The barrier height is defined by the difference of the two parameters—

$$\varphi_{bn} = \phi_m - \chi_s \tag{2.2}$$

The barrier height defined by equation (2.2) is called the Schottky-Mott limit.

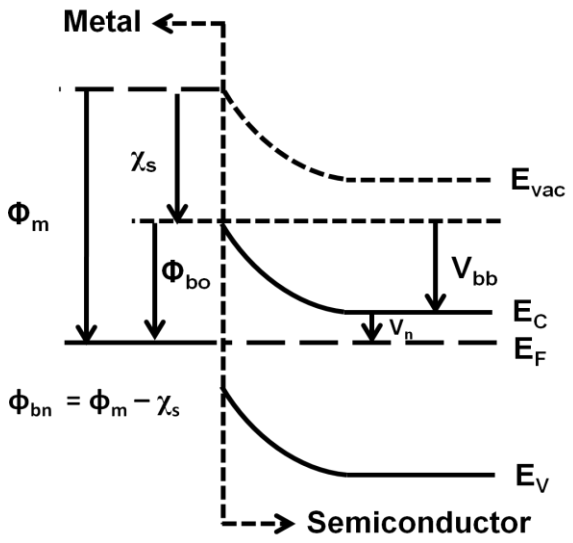

Figure 2.1 The interface band diagram of a metal/n-doped semiconductor Schottky junction in the Schottky-Mott limit.

It can be noticed from Fig-2.1 that the barrier height φ_{bn} is related to the band bending (V_{bi}) by—

$$\varphi_{bn} = V_{bi} + V_n \tag{2.3}$$

V_n is the conduction band position with respect to the Fermi level, which can be obtained by—

$$V_n = E_c - E_F = \frac{kT}{q}\ln(\frac{N_c}{N_D}) \tag{2.4}$$

The charge neutrality at the interface requires a sheet charge on the metal side of the interface, which is of the same magnitude of the space charge extended over the SCR on the semiconductor side. The charge balance can be written as—

$$-\sigma_m = \sigma_{SC} = qN_D W \tag{2.5}$$

Here, A is the area of the junction and N_D is the doping of the semiconductor crystal.

2.2.2 Effect of interface states: The Bardeen limit

In practical semiconductor Schottky junctions, the barrier height values do not always match up to the Schottky-Mott limit, and often show barrier heights independent to the metal work function. The Schottky barrier height is often determined by a Fermi level pinning close to the middle of the semiconductor bandgap. Bardeen argued that the deviation can be attributed to the presence of localized interface states at the Schottky interface [14]. It was argued that the interface states were associated with dangling bonds at the metal-semiconductor interface. In highly reactive semiconductor surfaces, the interface states may arise from the presence of a thin layer of oxide or adsorbed complexes, such as the hydroxyl group at the Schottky interface. Another potential source of interface states is ionic contamination of the surface during the surface treatment prior to metal deposition. In the later years, more sophisticated theories were developed for a quantum mechanical description of the interface states based on the works of V. Heine [23]. These theories include the interaction of the electron wavefunctions in the metal and the semiconductor, which can be modeled as metal-induced gap states (MIGS). On the other hand, using the modern tools of molecular physics, Tung showed that the interface energy states are a consequence of electric dipole formation at a molecular level at the metal-semiconductor interface [24][25]. The major difference between the classical theory (Bardeen) and the modern theories is that in classical theory, the interface states are assumed to be a property of the semiconductor surface alone, whereas the modern theories define an interface specific region (ISR), the charge transfer in which is affected by both the metal and the semiconductor.

Irrespective of the origin, the surface states typically have a flat energy distribution, and are characterized by a charge neutrality level (CNL), Φ_o. The CNL is defined as the energy level, up to which the states must be occupied by electrons for achieving charge neutrality at the interface. In the presence of interface states, this CNL determines the amount of band bending on the semiconductor side, rendering an effective surface barrier height insensitive to the metal work function, as shown in Fig-2.2.

As pointed out by Bardeen, in the case of a high density of interface states, instead of equation (2.2), the barrier height is given by—

$$\varphi_{bn} = E_g - \phi_o \tag{2.6}$$

,where E_g is the band gap of the semiconductor.

The charge distribution at the interface also changes in the presence of interface trap states. In this case, a sheet charge of corresponding to the surface states appears at

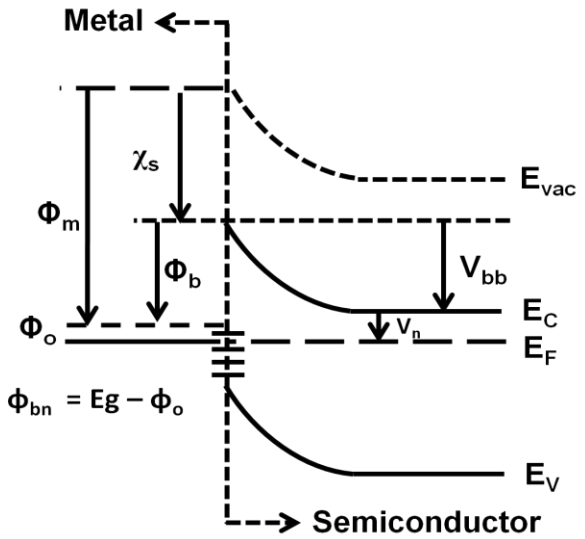

Figure 2.2 The interface band diagram of a metal/n-doped semiconductor Schottky junction in the Bardeen limit.

the interface, causing the semiconductor space-charge to reduce. The interface charge balance in this case is given by—

$$-\sigma_m = \sigma_i + \sigma_{SC} \tag{2.7}$$

This reduces the SCR width, as well as the built-in potential V_{bi}, so equation (2.3) still remains valid where φ_{bn} is determined by equation (2.6).

Equation (2.6) is an extreme case, in which the barrier height is determined solely by the interface state charge neutrality level. Real Schottky diodes, however, show a weak sensitivity on the metal work function. Sze and Cowley [26] argued that in real diodes, both metal work function and interface states influence the barrier height. Using the analytical expression for the charge densities in equation (2.7), they derived the effective barrier height as—

$$\varphi_{bn} = \gamma(\phi_m - \chi) + (1-\gamma)(E_g - \phi_o) \tag{2.8}$$

$$\text{,where } \gamma = \frac{\varepsilon_i}{\varepsilon_i + q\delta D_{it}} \tag{2.9}$$

Here, ε_i is the dielectric permittivity of that layer. D_{it} is the δ is the width of a hypothetical interface layer that separates the sheet charges σ_m and σ_i. In the quantum mechanical theories, this interface layer is referred to as the interface specific region (ISR), where the electron wavefunctions in the metal and the semiconductor collide.

As can be seen from equation (2.8) and (2.9), in the absence of interface states, D_{it} = 0, and the expression becomes the same as the Schottky-Mott limit defined in equation (2.2). On the other hand, for very high density of surface states, D_{it} is very high, and equation (2.8) reduces to equation (2.6), generally called the Bardeen limit of Schottky barrier height.

For estimating the dependence of experimentally determined barrier heights formed with metals with different work function values, an interface index (S) is defined as $\delta\phi_m / \delta\varphi_{bn}$. In the Schottky limit S = 1, while in the Bardeen limit, S = 0. In real semiconduction junctions, S resides between 0 and 1.

2.3 NON-IDEAL EFFECTS

The current-voltage characteristics in Schottky junctions is defined by equation (2.1), which accounts for thermionic emission of electrons over a Schottky barrier, φ_{bn}. The conduction mechanism may vary depending on the nature of the junction; tunneling transport and field emission are also observed. These effects arise in special cases, and are not observed in regular Schottky junctions. The regular Schottky junctions, however, show thermionic emission behavior with a current characteristic that deviates from the expression given in (2.1). A common form of non-ideality is a barrier height that is dependent on the applied bias. Assuming the dependence to be linear, this bias dependence can be encapsulated into a single parameter called the ideality factor (n). If the zero bias barrier height is denoted by φ_{bo}, the linear dependence can be written as [27]—

$$\varphi_{bn}(V) = \varphi_{bo} + \beta V \tag{2.10}$$

Replacing this value of φ_{bn} in equation (2.1) yields—

$$\begin{aligned} J &= A^{*}T^{2}\exp\left(\frac{-q(\varphi_{bo}+\beta V)}{kT}\right)\exp\left(\frac{qV}{kT}-1\right) \\ &= A^{*}T^{2}\exp\left(\frac{-q\varphi_{bo}}{kT}\right)\left\{\exp\left(\frac{qV(1-\beta)}{kT}\right)-\exp\left(\frac{-q\beta V)}{kT}\right)\right\} \end{aligned} \tag{2.11}$$

Replacing (1-β) with 1/n in equation (2.11) yields—

$$J = A^{*}T^{2}\exp(\frac{-q\varphi_{bo}}{kT})\left\{\exp(\frac{qV}{nkT}) - \exp(\frac{1-n}{n})(\frac{qV}{kT})\right\} \qquad (2.12)$$

For V >> kT/q, this equation reduces to—

$$J = A^{*}T^{2}\exp(\frac{-q\varphi_{bo}}{kT})\exp(\frac{qV}{nkT}) \qquad (2.13)$$

Equation (2.13) is generally used for modeling experimental I-V characteristics. The ideality factor (n) is obtained from the slope of the linear region of the experimental ln(I) vs V characteristics. The value of n is unity in ideal diodes, and is greater than unity in non-ideal diodes.

The ideality factor, n, although mathematically convenient, does not provide any physical description of the non-ideal behavior. The factor is based solely on the assumption that the variation in the barrier height with voltage is linear. In highly non-ideal diode characteristics, the linear region in the ln(I) vs V characteristics is often obscured by series resistance, double barriers (or humps), and/or bias-dependent slopes, which sometimes makes it difficult to extract a single value for n, independent of the bias voltage. This kind of anomalous, bias dependent barrier height is commonly attributed to nanoscopic Schottky barrier inhomogeneity at the interface.

2.3.1 Image force lowering

The image force lowering of the Schottky barrier height arises from the image force experienced by an electron in the space-charge region. When an electron is generated in the space-charge region or simply reaches there, it electrostatically interacts with the Schottky barrier. The interaction can be modeled as an induced mirror charge of same magnitude and opposite polarity on the metal side of the interface. The resulting

potential opposes the potential caused by the SCR electric field, which reduces the Schottky barrier height by—

$$\Delta\varphi_{if} = \frac{1}{4}\left\{\frac{2q^3 N_D}{\pi^2 \varepsilon^3}(V_{bi} - V - \frac{kT}{q})\right\} \tag{2.14}$$

The effective barrier height (φ_{eff}) is obtained by subtracting the image force 'correction'($\Delta\varphi_{if}$) from the original barrier height (φ_{bn}) The effect of the reduction is shown in the band diagram in Fig-2.3(a). Fig-2.3(b) plots φ_{eff} vs junction bias (V) for a SiC Schottky diode with a barrier height of 1.6 eV and a doping concentration of 10^{15} cm^{-3}. As shown in the figure, the image force lowering is significant in reverse bias although it saturates at some point as the reverse bias is increased. On th other hand, in the forward bias regime, the barrier height increases sharply with the applied bias and approaches the ideal value at the flat band voltage ($V = V_{bi}$).

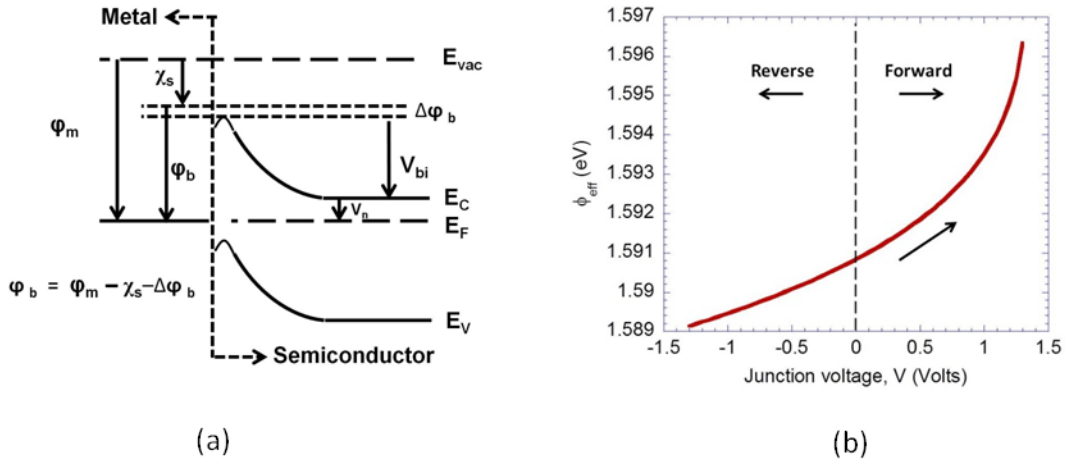

Figure 2.3 Image force lowering in Schottky junction. (a) interface band bending. (b) A plot of effective barrier height vs applied bias for a SiC Schottky junction.

As argued by Rhoderick et al. [27], in the absence of interface states, the non-ideality can arise only from the image force lowering. Although the image force lowering does in no way accounts for a linear variation of the barrier height (Fig-2.3b), an approximate, voltage dependent ideality factor (n) in that case is derived as—

$$\begin{aligned}\frac{1}{n} &= 1-\beta = 1-\frac{\delta\varphi_{eff}}{\delta V} \\ &= 1-\frac{1}{4}\left(\frac{q^3 N_D}{8\pi^2\varepsilon^3}\right)^{1/4}\left(V_{bi}-V-\frac{kT}{q}\right)^{3/4}\end{aligned} \tag{2.15}$$

In a moderately doped forward biased SiC Schottky junction, n_{if} assumes near unity values, in which case the image force effect in the forward I-V characteristics can be ignored altogether.

2.3.2 Schottky barrier inhomogeneity

The spatial variation in the Schottky barrier height across the contact area is studied as a major non-ideal effect. Barrier inhomogeneity models have been successful in describing highly non-ideal characteristics such as the double barrier characteristics.

The most primitive model for describing the double barrier characteristics is the parallel conduction model that assumes distinct regions of high and low Schottky barriers in the contact area [25][28]. The total diode current is considered an aggregate of the current flowing through the different regions in the interface with different barrier heights. The non-ideality in the diode characteristics arises from the low barrier regions turning on at a lower bias than the high barrier region.

A major weakness of this model is that it is dependent on the ideality factor, the physical implication of which is not apparent. The barrier heights extracted from this

model are also theoretical estimates that cannot be attributed to any physical interface parameter. Moreover, real metal-semiconductor interfaces are expected to consist of a distribution of Schottky barrier heights rather than large patches of two different barrier heights. Werner et al. argued that the small barrier regions can be in the form of microscopic patches with a Gaussian distribution of barrier heights [28]. However, this model comes with the intrinsic assumption of an ideality factor, and does not provide a physical understanding of the non-ideal behavior. It is interesting to note that a similar model was proposed for point contacts, in which, in spite of the low dimension of point contacts, the total junction current was assumed to be an aggregate of the current from multiple contact points [29]. This 'multi-contact' theory assumed an exponential distribution of surface potential across the device active area, which fit the non-ideal point contact characteristics.

Tung et al.[24][25] considered a similar distribution of Schottky barrier height across the contact interface. In this model, the Schottky interface is described as a uniform 'high barrier' region with patches of lower barrier height embedded in it. Tung pointed out that the length-scale associated with barrier inhomogeneity can be comparable to the Schottky depletion width. In that case, low barrier regions surrounded by higher barrier regions can undergo current pinch-off at low bias voltages (Fig. 2.4). The effective barrier height of these pinched-off view of the interface showing the depletion regions corresponding to the low and high barrier regions. (c) At low bias, the LSBH patch starts conducting, while the bulk of the interface remains depleted. As the depletion width is comparable to the patch dimension, 'patch' (LSBH) surrounded by the high barrier bulk of the interface. (b) A cross sectional the field under the HSBH bulk

laterally pinches off (PO) the current through the LSBH patch, the amount of pinch-off being a patches becomes a function of the applied voltage, which leads to a high ideality factor. In the current study, the Tung model is applied to the experimental data obtained from non-ideal SiC schottky diodes, which renders further insight into the model parameters, as will be discussed in Chapter 4.

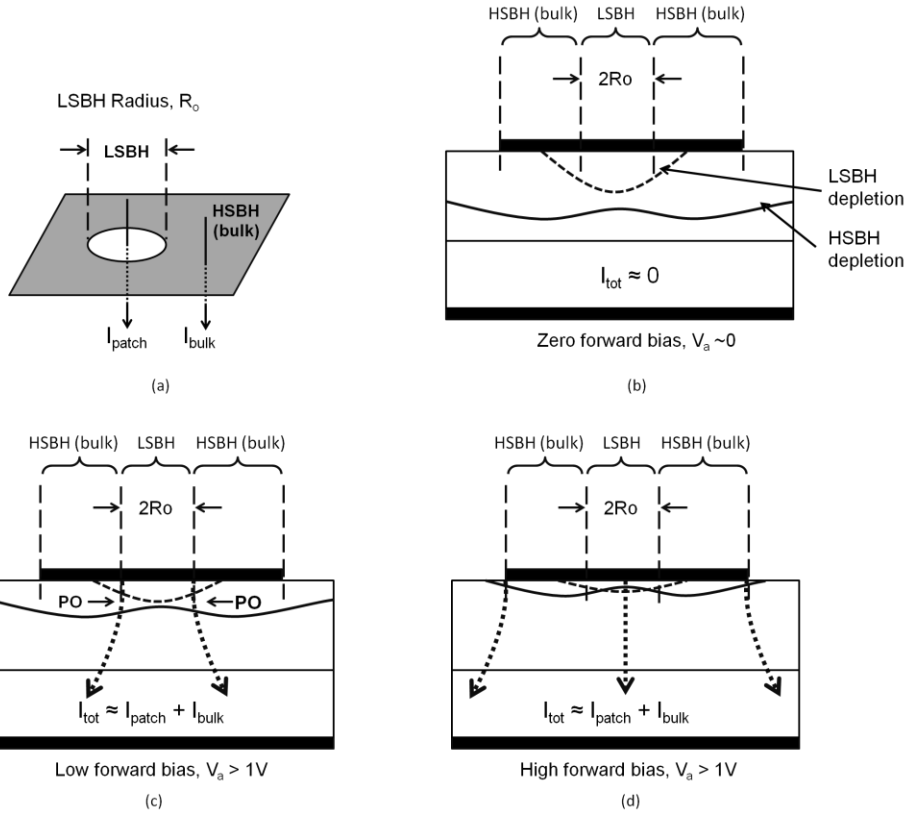

Figure 2.4 A qualitative illustration of Tung's model: non-ideal diode behavior caused by the Schottky barrier inhomogeneity. (a) The inhomogeneity is perceived as a low barrier function of applied voltage. (d) At sufficiently high bias, the bulk turns on and both the LSBH and HSBH regions start conducting, and the pinch-off effect disappears.

2.3.3 Minority carrier injection

Schottky junction devices are generally considered majority current devices. The minority carrier current is often negligible, and the omission of the minority injection

effect from the theoretical models is acceptable in most modern Schottky junction diodes. However, in the early days of solid-state physics, significant minority carrier injection was routinely observed from metal point contacts into the semiconductor [14][15][16][17][18][19]. Bardeen et al. showed that the minority carrier injection is the major conduction mechanism in a point contact to germanium, and demonstrated the first transistor using this phenomenon . However, the conduction mechanism across the interface was never Bradley et al. demonstrated the same effect in a wide area Schottky contact to Ge, and fabricated a surface barrier phototransistor.

The interest in the minority carrier injection properties of metal contacts waned with the advent of 'buried' semiconductor p-n junctions, as these junctions rendered a higher level of control over the minority carrier injection and ease of fabrication. The effect re-appeared again in diamond point contact transistors, in which case, the surface inversion characteristics of diamond was found instrumental behind the minority injection [30]. Unlike the point contacts and earlier surface barrier devices, the large area MS Schottky barrier diodes showed negligible minority carrier injection. The injection properties were nevertheless studied, especially with a view to explaining the non-ideal effects in Schottky diodes. However, the minority carrier current was observed to constitute no more than 10% of the total current [31]. In the later years, the observation of considerable minority carrier injection became rarer, which is attributed to the practice of fabricating diodes on epitaxial layers grown on highly doped substrate, instead of bulk semiconductor materials. In these devices, the epi-substrate back junction acts like a reflecting barrier for minority carriers, inhibiting further injection from the Schottky contact [32].

The injection of minority carriers across an MS interface is quantified by the injection ratio, γ, the ratio of the minority carrier current to the total current [33][34]—

$$\gamma = \frac{J_n}{J_n + J_p} \tag{2.16}$$

While the point contact junction as well as the early bulk Schottky junctions showed high minority carrier injection ratios, modern epitaxial diodes show a maximum minority carrier injection ratio < 10%. Therefore, these junctions cannot be used as a bipolar emitter like a point contact.

In the current study, we will reconsider the various minority carrier injection models and show that a high level of minority carrier injection is possible in the large barrier graphene/p-SiC Schottky junction.

2.3.4 Recombination effects

For minority carrier injecting Schottky junctions, Shockley-Reed-Hall (SRH) recombination in the trap sites at the forward bias junction can be significant. The maximum possible SRH recombination current (i.e., assuming a midgap trap level) in a junction takes the following form—

$$J_{rec} = \frac{qn_i W}{2\tau} \exp\left(\frac{qV}{2kT}\right) \tag{2.17}$$

Here, n_i is the intrinsic carrier concentration and τ is the recombination lifetime. The recombination current is particularly significant at low bias, when the SCR width W is significant, and the exponential factor is smaller in magnitude. It is to be noted that the recombination current (J_{rec}) has an inherent ideality factor of 2. In the presence of recombination, the total majority carrier current becomes a sum of J_{rec} and the thermionic

emission current described by equation (2.1). This leads to an equivalent exponential I-V characteristics with an ideality factor greater than 1.

Woods et al. [35] provided the condition for having a significant carrier recombination in a Schottky junction, which is given by—

$$\varphi_{bn} \geq \frac{E_g}{2} + \frac{1}{2}\frac{kT}{q}\ln(\frac{N_c}{N_v}) \tag{2.18}$$

According to this equation (2.18), the SRH recombination can account for a significant portion of the diode current in Schottky junctions with barrier heights greater than half of the semiconductor bandgap ($\varphi_{bn} > E_g/2$).

2.4 ELECTRICAL MEASUREMENT OF BARRIER HEIGHT

Schottky barrier height can be measured by various optical and electrical techniques. The barrier height measured in different techniques can give widely different values, depending on the experiment condition. The variability of the barrier height with applied bias and temperature further complicates the measurement.

The zero-bias barrier height (φ_{bo}) is typically determined from the intersect of the ln(I) vs V characteristics with the current axis at V = 0. The intersect provides the pre-exponential term of equation (2.1), from which the barrier height can be determined. This measurement is, however, affected by the interface effects, image force lowering, barrier inhomogeneity and SCR recombination, as all of these non-ideal effects are more significant at low bias. As a result, φ_{bo} underestimates the barrier height and, in non-ideal junctions, shows a value significantly lower than the Schottky-Mott limit.

As shown in equation (2.3), the Schottky barrier height is a sum of the zero-bias band bending (V_{bi}) and the position of the Fermi level with respect to the conduction

band, denoted by V_n. An estimation of the band bending can, therefore, provides a more accurate barrier height estimation. As the band-bending ($V_{bb}=V_{bi}-V$) is modified by the applied bias, this parameter can be extracted from the junction characteristics. A good measure for V_{bi} is the flat-band voltage V_{FB}, the amount of forward bias required to reduce the Schottky barrier to 0 eV (Fig-2.5).

The most common technique of the determination of the flat band voltage is the C-V characterization. In this technique, the junction is reverse biased, and the variation of capacitance with respect to an applied bias (dC/dV) is estimated by applying a high frequency (typically > 100 kHz) small signal on top of the bias. The junction capacitance is measured from the charge transferred through the displacement current over a range of reverse bias, and a C-V characteristics is obtained. The capacitance is given by—

$$C = A\sqrt{\frac{q\varepsilon Nd}{2(V_{bi}+V)}} \tag{2.19}$$

If the inverse square of the capacitance ($1/C^2$) is plotted against the reverse bias (V), the flat band voltage can be obtained from the intercept on the voltage axis (C=0), which denotes the disappearance of the SCR under forward bias.

From the I-V characteristics, an extrapolated flat-band barrier height (Φ_{bf}^{n}) can be determined by comparing equations (2.3) and (2.10) at the flat band condition [36]—

$$\phi_{bf}^{n} = n\phi_{bo} - (n-1)V_n \tag{2.20}$$

The underlying assumption behind this relation is that the true barrier height Φ_b has a linear dependence on the applied bias. The accuracy of this estimate depends on the accuracy of the estimate for the ideality factor (n) and the zero-bias barrier height (φ_{bo}).

In this dissertation, an alternative technique for determining the flat band barrier height (which we will call Φ_{bf}) from the experimental I-V characteristics is proposed, that does not need the ideality factor. A Schottky junction under forward bias can be modeled as a series combination of an ideal diode (D) and the series resistance (R_s), as shown in Fig-2.5. The applied voltage, V is shared between these two components. For low

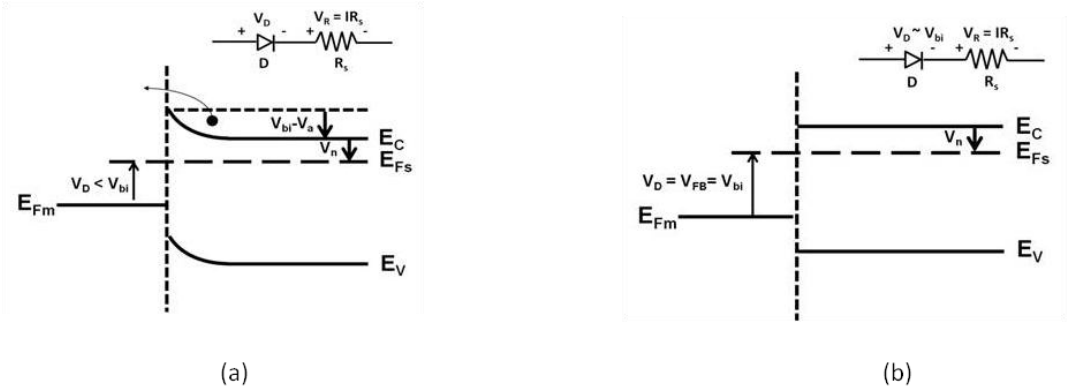

Figure 2.5 The band diagram of an n-Schottky junction under a forward bias (a) lower and (b) higher than required for achieving the flat-band condition.

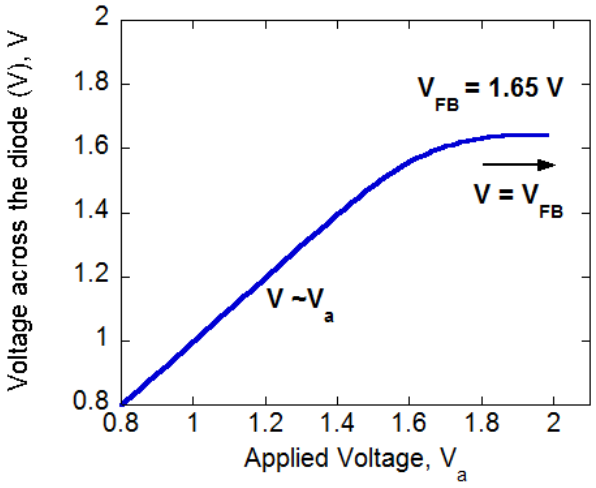

Figure 2.6 Voltage across SCR (V) vs applied bias plot for flat-band voltage determination.

forward bias levels ($V_D < V_{bi}$), the diode current (I) is small and $V_D \approx V$. As the forward bias is increased, the Schottky barrier is reduced (Fig-2.5) and the voltage drop across R_s, denoted by V_R in the figures, increases. At a certain forward bias (V_a), $V_D = V_{bi}$, the Schottky barrier disappears, and the flat-band condition is reached. It is to note that increasing V beyond this point does not alter V_D any more, as there is no barrier to overcome. The voltage across R_s, however, keeps increasing linearly. The constant diode voltage drop (V_D) is essentially the flat-band voltage (V_{FB}) for the diode, and can be estimated from a plot of V vs V_D, as shown in Fig-2.6. The equivalent diode voltage, V_D (which is nothing but the voltage across the SCR) can be estimated by experimentally determining the series resistance of the Schottky diode structure by a technique like the Norde plot, and then subtracting the voltage drop across the resistance from the total applied bias. As shown in Fig-2.6, V_D increases linearly with the applied bias, and saturates at the flat-band voltage (V_{FB}), at which point V_R becomes the dominant voltage drop. The I-V flat band barrier height (φ_{bf}) can then be determined by adding V_n to V_{FB}.

Apart from the theories discussed in this chapter, there exists a large body of work on the temperature dependence of the Schottky characteristics, which will not be discussed here, as the temperature effects are beyond the scope of this study.

CHAPTER 3

EPITAXIAL SILICON CARBIDE FOR SCHOTTKY DIODE FABRICATION: GROWTH AND CHARACTERIZATION

The first step toward the fabrication of a semiconductor device is the growth of the semiconductor crystal. The bulk and surface characteristics of the crystal is the major determinant of the device performance. In the novel compound semiconductor technologies, the material quality often becomes the bottleneck to optimized device performance. It is, therefore, necessary to have a well-tuned and reliable crystal growth process to begin with.

The experimental work in the current focuses on large barrier silicon carbide (SiC) Schottky junctions. The fabrication of the Schottky junction begins with the growth of epitaxial SiC crystal on bulk-grown substrate material. This chapter is devoted to the discussion of the growth process and its effect on crystal properties that influence the characteristics of the devices formed on the grown crystals.

3.1 A BRIEF OVERVIEW OF SIC EPITAXY BY CHEMICAL VAPOR DEPOSITION

Power electronic application of semiconductor devices require high purity crystal layers with large area and thickness, as well as high throughput. Chemical vapor deposition (CVD) has been the preferred growth technique for device grade silicon

carbide crystal, as this technique is capable of delivering all of the requirements mentioned above. CVD growth of SiC dates back to the 1960s when Jenning's et al. [37] and Campbell and Chu [38][39] demonstrated homoepitaxial (though highly inhomogeneous) growth of hexagonal SiC by CVD. The process, however, required very high temperatures, which resulted in a drastic reduction of growth rate.

The usefulness of SiC as a wide bandgap semiconductor for power electronics became apparent in the 1980s, leading to the rapid advancement of the bulk SiC growth technology. As a result, large area substrates became available, which created the need for a large area epitaxial growth technique. A number of growth techniques, including sublimation epitaxy, vapor phase deposition, were explored. In 1987 Kuroda et al. showed that homogeneous epitaxial growth on substrates cut at an angle required a growth lower temperature [40]. The development of the hot wall reactors in the 1990s rendered the chemical vapor deposition (CVD) a competitive edge over the other techniques. This development was combined with the use of substrates with surface offcut, facilitating high quality epitaxial growth of SiC.

3.1.1 The chemical vapor deposition process

The chemical vapor deposition of SiC is typically performed in hot-wall CVD reactors. The hot wall design ensures an even temperature distribution within the reactor, which minimizes parasitic deposition, and renders a controllable dissociation of the source gases. Typical Si and C sources are silane (SiH_4) and a light hydrocarbon, such as propane (C_3H_8) diluted in hydrogen (H_2), which is also used as a carrier gas.

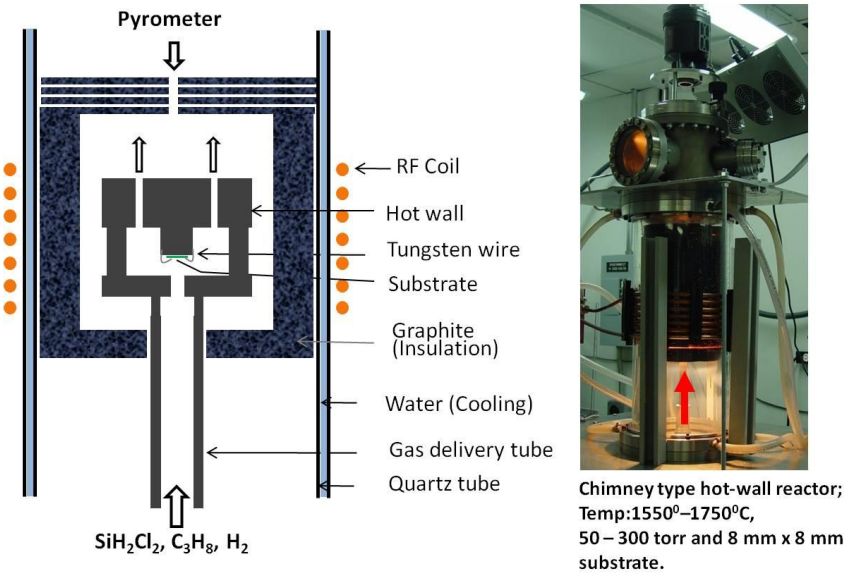

Figure 3.1 The CVD apparatus in the SiC lab, USC. (a) Anatomy of the growth chamber. (b) the reactor— a vertical, inductively heated, hot wall, chimney type reactor, supported by a high voltage generator and a high vacuum pump assembly.

In the SiC Lab of University of South Carolina, a vertical, hot wall, chimney type reactor is used for SiC homoepitaxy. The substrate is fixed on a tantalum carbide coated graphite susceptor (Fig-3.1a). A graphite cylinder around the susceptor serves as the hot wall. Graphite felt/foam insulators are used to minimize heat loss. The growth chamber resides within a two wall quartz enclosure with water flowing outside the inner wall. The hot wall is heated by induction using a high voltage generator. Typical growth temperature is 1500 – 1650^{o}C, while the typical chamber pressure used is ~80 torr. A pump assembly consisting of two mechanical pumps and a turbo pump is used for evacuating the chamber prior to the growth run. The lowest pressure achievable in the chamber is ~10^{-7} torr.

3.1.2 Polytype-matched growth of SiC: Step-controlled epitaxy

The SiC crystal has a Wurtzite structure with C-Si bilayers stacked along the c [0001] direction in hexagonal closed packed layers. Depending on the possible atomic sites, the layers may be one of the three orientations shown in Fig-3.2 (a). Depending on the stacking sequence SiC can be of many different polytypes. Fig-3.2(c) shows the most common polytypes— 3C, 4H and 6H. The first of the three, 3C-SiC is cubic, i.e., has a symmetrical atomic arrangements along the two directions shown (ABC…). On the other hand, 4H and 6H-SiC are hexagonal polytypes, with stacking sequences ABCB… and ABCACB… respectively. The physical properties of the polytypes can widely differ from one another. A comparison of the properties of the three common polytypes is given in Table-3.1. As can be seen from the table, the band gap of the hexagonal polytypes are larger than the 3C-SiC, for which reason 4H and 6H-SiC are technologically more important in power electronics.

The polytypism of SiC makes it difficult to grow homogeneous, polytype-matched crystal. On the c(0001) surface (the typical growth surface), 3C-SiC is the energetically favorable phase at low temperatures. Homoepitaxial growth of hexagonal SiC requires temperatures >1700^{o}C, at which point the desorption is so intense that the growth rate nearly vanishes. However, the step-controlled growth on an off cut surface (shown by Kuroda et al.) allows hexagonal SiC growth at temperatures ~ 1500^{o}C.

The step controlled growth or the step flow mechanism of the SiC growth by CVD was first extensively studied by Kimoto and Matsunami et al.[42][43]. In these studys, the surface diffusion lengths of the reactant species adsorbed on the step terraces

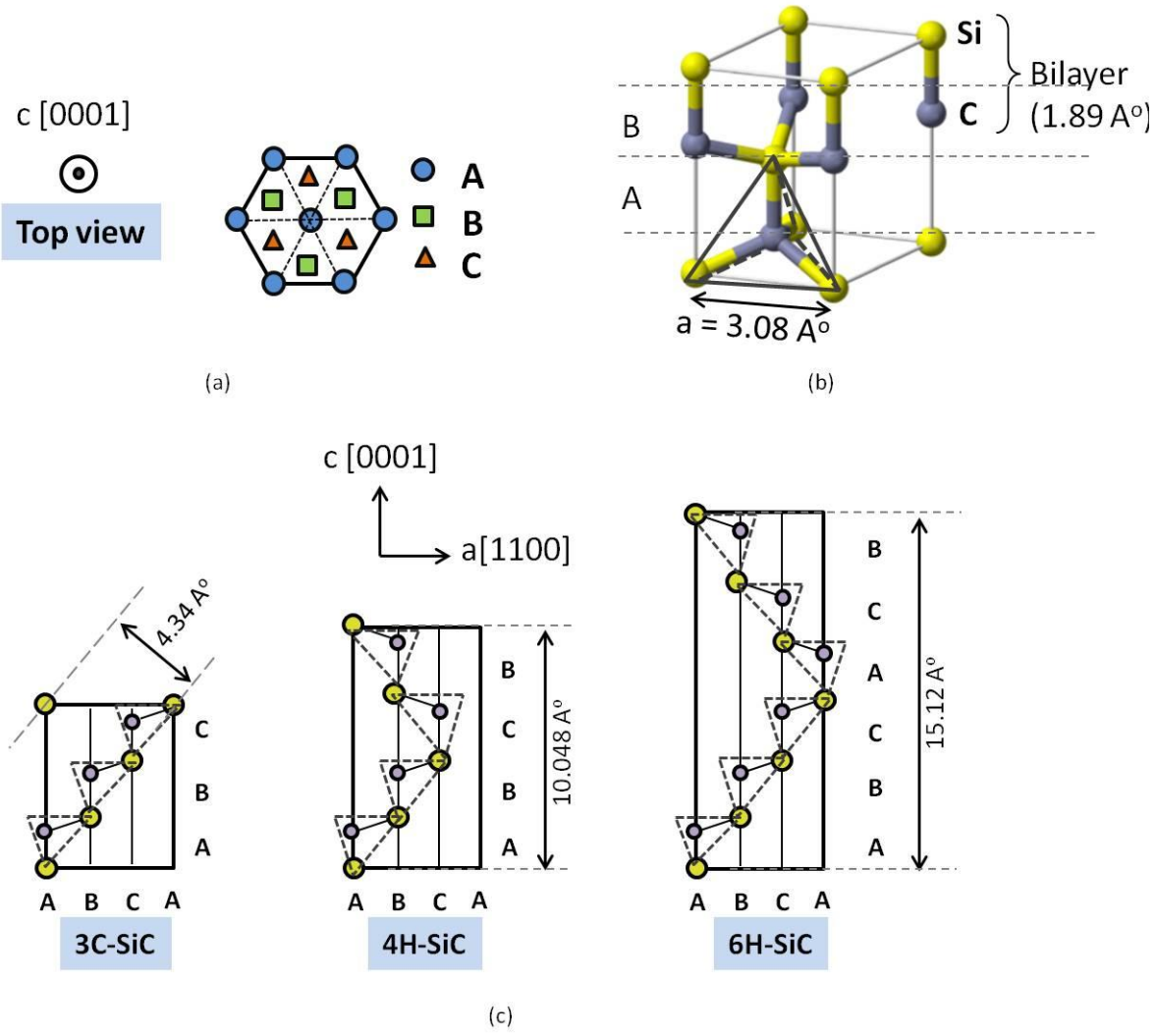

Figure 3.2 SiC polytypes. (a) The atomic sites on the hexagonal closed pack structure. (b) The Wurtzite SiC unit cell. (c) The stacking arrangement for 3C, 4H and 6H-SiC.

at different growth temperatures were extracted using a model based on the Burton-Cabrera-Frank (BCF) theory, as illustrated in Fig-3.3. The model described the step-flow growth mechanism in terms of two competing processes—incorporation of adatoms at the step edges and desorption of adatoms from the step terraces. However, the polytype inhomogeneity (3C-SiC inclusion) observed in the low offcut (< 4^{o}) epilayers suggests

Table 3.1 Physical properties of common SiC polytypes [41]

Properties	**3C-SiC**	**4H-SiC**	**6H-SiC**
Bandgap, eV	2.3	3.2	3.0
Electron mobility (μ_n), cm2/Vs	750	800	||c – 800 ⊥c-axis: 60
Hole mobility (μ_p), cm2/Vs	40	115	90
Critical electric field (E_c), MV/cm	~1.5	3	3.2
Saturation electron velocity (v_{sat}), x10^7cm/s	2.5	2	2

the existence of another process—nucleation of adatoms on the kink sites on the step terraces. Experimental results indicate that polytype-inhomogeneous growth on the low-offcut substrates could be suppressed by going into a 'desorption-controlled' growth regime. One way of doing this is using high growth temperatures (>1500^{o}C), which, however, reduces the growth rate significantly. Another way, as will be shown later is to use a chlorinated precursor that suppresses nucleation of adatoms on the step terraces through a controlled dissociation, thereby emulating a desorption-limited growth regime at regular (~1500^{o}C) growth temperatures.

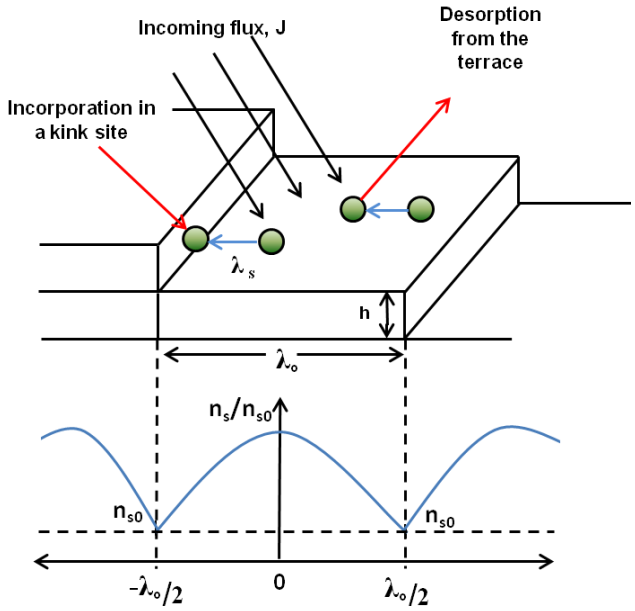

Figure 3.3 Step-flow epitaxial growth. The two competing processes are adsorption and diffusion of reaction species and thermal desorption of adsorbed species at the growth surface.

3.2 MAJOR CHALLENGES IN SIC CRYSTAL GROWTH: A DEVICE PERSPECTIVE

3.2.1 Defects in the SiC crystal

A crystal is a periodic arrangement of atoms. Any disruption to that periodicity is considered a defect. As the defects sites have different atomic arrangements and different bond structures, the electronic properties of these sites can be very different from the bulk of the crystal. This variation in electronic characteristic can introduce non-ideal effects in the device characteristics. Like any material system, the SiC crystal contains certain types of imperfections or defects that can influence the electrical performance of SiC devices. The growth of defect-free or at least low-defect crystal is, therefore, a major challenge in SiC electronics.

The structural defects observed in epitaxial SiC crystals be classified under two heads—(i) Extended defects and (ii) Point defects.

A *point defect* in a crystal is a consequence of one misplaced atom. The atom may be missing, in which case it is called a vacancy, or it may occupy a site in an interstitial position among the other atoms. Again, different types of point defects can bind together to form complexes. Point defects are associated with activation energies that fall inside the energy gap of the host SiC crystal and often form deep traps for charge carriers. These deep traps play an important role in determining the carrier lifetime and hence the switching speed of SiC devices.

The *extended defects* are not localized; rather they run through a considerable length in the crystal. In SiC, these defects have been identified to be the most electrically active defects and have been linked to different types of device degradation mechanism. The extended defects are of two types – (i) Line defects or dislocations and (ii) planar defects.

In the case of *line defects*, a series of atoms is misplaced. The two major types of dislocations observed in SiC epilayers are threading edge dislocations (TED) and threading screw dislocations (TSD).

Edge dislocations are formed when an atomic plane terminates halfway through the entire dimension of the crystal, deforming the surrounding planes around the 'edge' of the incomplete atomic plane. The edge of the incomplete plane forms the 'defect line' in the crystal along which the atoms are misplaced. The effect of edge dislocations on the device performance is not well-established, although surface features (nanopit) associated with edge dislocations have been linked to increased leakage current.

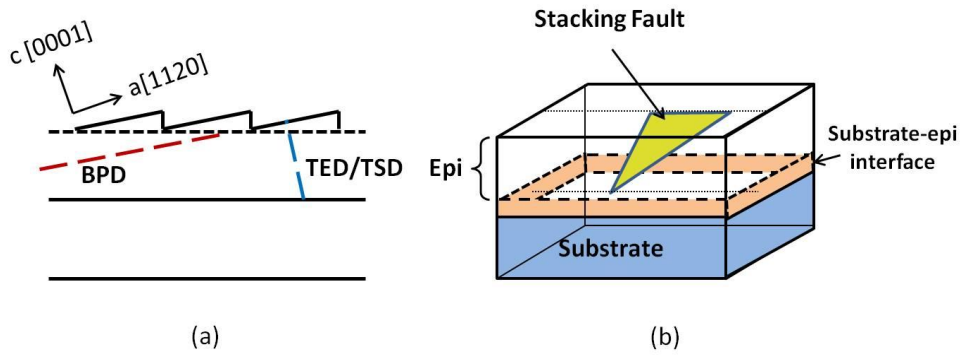

Figure 3.4 Defects in SiC crystal. (a) Line defects extend as threading dislocation lines. TSD = Threading screw dislocation, TED = Threading edge dislocation, BPD = Basal plane dislocation. (b) Stacking faults are planar defects covering an area inside the crystal.

Screw dislocations are formed when one of the atomic planes in the crystal has a twist with respect to the others. These defects create helical structures centered around the line of dislocation and hence gets the name 'screw' dislocation. Screw dislocation with a core is called a micropipe. The most meaningful way the screw dislocation of different types can be distinguished is the Burger's vector. A Burger's vector denotes the direction and extent of lattice distortion. In the case of a screw dislocation, the Burger's vector is parallel to the dislocation line, i.e., perpendicular to the crystal plane in the case of a SiC epilayer slightly off-oriented from the c-plane. A pure screw dislocation has a Burger's vector magnitude of one and is denoted by a 1c dislocation. Screw dislocations of higher magnitudes (2c, 3c etc.) can be combinations of screw dislocations and micropipes. The micropipes can have Burger's vectors from 2c to 7c. Screw dislocations are typically associated with premature breakdown of SiC devices, and in some cases high reverse leakage current. The higher the Burger's vector, the detrimental is its effect.

The existence of a single micropipe in a device area can render it non-functional by showing breakdown voltages as low as 20 V.

Because of the offcut angle of the SiC surface, a dislocation in the basal plane (0^o off-angle) becomes significant. These *basal plane dislocations***,** abbreviated BPD, can evolve into larger planar defects and can have significant impact on SiC device performance.

Planar defects are large area defects associated with a change in crystal orientation or stacking sequence over a large area. The most important planar defect in SiC is the *stacking fault*. These defects arise from a localized change of polytype in an otherwise polytype-homogenous crystal. Stacking faults can cause forward voltage drift in bipolar devices. They are also known to degrade carrier lifetime, as well as cause double barrier characteristics in Schottky diodes.

Table 3.2 summarizes the extent of the major crystallographic defects and their effect on SiC power device performance. Most of the defects (especially the sessile ones) cause an increase in reverse leakage current by providing a low resistance path for current flow during the device off-state. Also, the shape of the defects and the associated surface pits cause irregularities in the electric field distribution in the device.

3.2.2 Surface morphology

Surface sensitive devices, such as Schottky diodes and MOSFETs require smooth surfaces with a low density of surface defects and dangling bonds. In Schottky diodes, the surface defects expose more than one crystal face to the metal atoms deposited on the

surface, causing local variation of barrier heights. In power devices, the surface roughness can lead to electric field crowding, causing increased leakage.

Table 3.2 Impact of crystallographic defects on device performance

Defect type	Impact on device performance	Typical defect density
BPD	Forward voltage drift	0-20 cm^{-2}
IGSF	Breakdown voltage reduction and leakage current increase	5-30 cm^{-2}
TSD	Breakdown voltage reduction	10^2-10^3 cm^{-2} (from substrate)
Growth pit	Rough surface.Some pits may be associated with TSD/TEDs.	0-10^3 cm^{-2}
Carrot defect	Increase in reverse leakage current	0-2 cm^{-2}
Triangular Defect	Breakdown voltage reduction and leakage current increase	0-2 cm^{-2}
Step bunching	Rough surface, E-field crowding	RMS~2.2nm
Point defect	Minority carrier lifetime	0.25~10 μsec

Common surface defects on a SiC epi surface include step bunching, carrots and/or triangular defects and various types of pits (Fig-3.5). Carrots and triangular defects (shown in Fig-3.5b) are formed when the step flow growth is interrupted by adatom clusters or external particles on the crystal surface. These defect regions have different

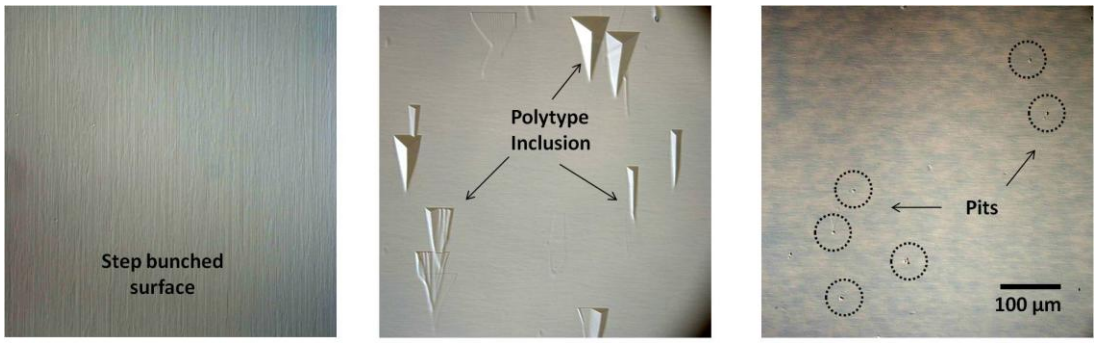

Figure 3.5 Common surface defects on SiC epilayer surface.

polytype than the substrate. In 4H and 6H-SiC these defects are typically of 3C or 8H type.

Surface pits of different size and shape are also formed on the surface (Fig-3.5c). These pits may or may not be associated with an extended defect running along the epilayer thickness. The effect of the surface pits on device performance is not well-known. However, surface nanopits related to threading edge dislocations have been associated with increased leakage current in SiC Schottky diodes.

However, the most conspicuous surface features on a SiC epilayer are the bunched steps. Step bunching on a SiC surface occurs on two different levels. The micro step bunching ocuurs at the Si-C bilayer level. As shown in Fig-3.6a, in 6H-SiC, the difference between the growth rates along the two groups of bilayers— ABC and ACB leads to a 3 bilayer micro-step bunching [44]. In 4H-SiC, the microstep is typically 4 bilayer high.

The macro step bunching, however, follows a different mechanism. As was shown in Fig-3.3, the step-controlled growth involves surface diffusion of adatoms followed by their capture at the step edges. Each step edge see two fluxes of adatoms, one

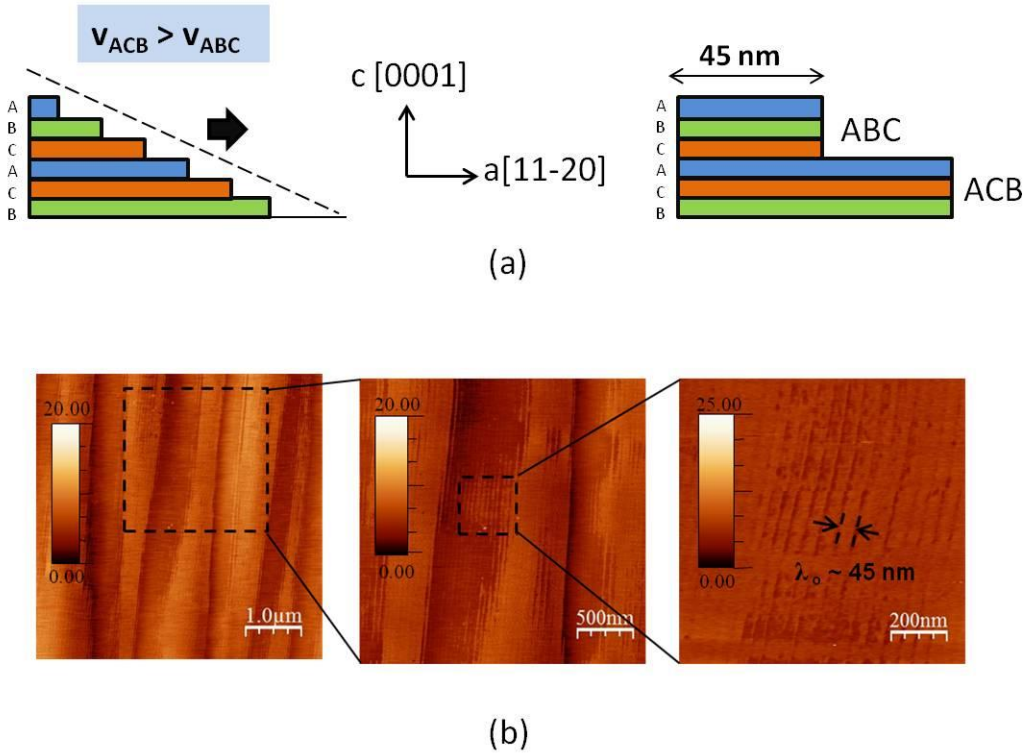

Figure 3.6 Step bunching in SiC epilayer surface. a) Micro and (b) macro step bunching on the surface of a 6H-SiC epilayer grown on a 1^o offcut substrate at a growth rate of 3.5 μm/hr. Each macro-step comprises of micro-steps of uniform terrace width of ~45 nm, which indicates 3-bilayer high 'micro' step-bunching with theoretically calculated step widths of 43.3 nm. The macrosteps are far wider, spanning > 0.5 μm across.

coming down from the upper terrace, one coming along the next terrace. The adatoms moving down to the next step faces an impedance against incorporating to the next step edge, which is known as a negative Ehrlich–Schwoebel barrier [45]. This barrier causes an imbalance in the adatom flux coming from the two directions, causing an asymmetry in the corresponding growth rates [46]. As a result, the growth rate in the lower terraces becomes larger than those on the upper terraces (with respect to the step flow direction). This asymmetry causes the steps to grow over each other, and form bunched macro steps.

Another type of step bunching is observed in a SiC that forms zigzag structures on the surface. This anisotropic step bunching is believed to be a consequence of the difference in growth rates in two possible growth directions along [10-10] and [11-20] [47], as shown in Fig-3.7. Since the [10-10] direction is a closed packed crystallographic direction, growth rate v_{step} along [10-10] is slower than that along [11-20] (v_{kink}), which is not a closed packed direction. Geometrically, the growth in the [10-10] direction has to cover a longer distance ($2/\sqrt{3}$ times that in [11-20] direction) for a complete step coverage

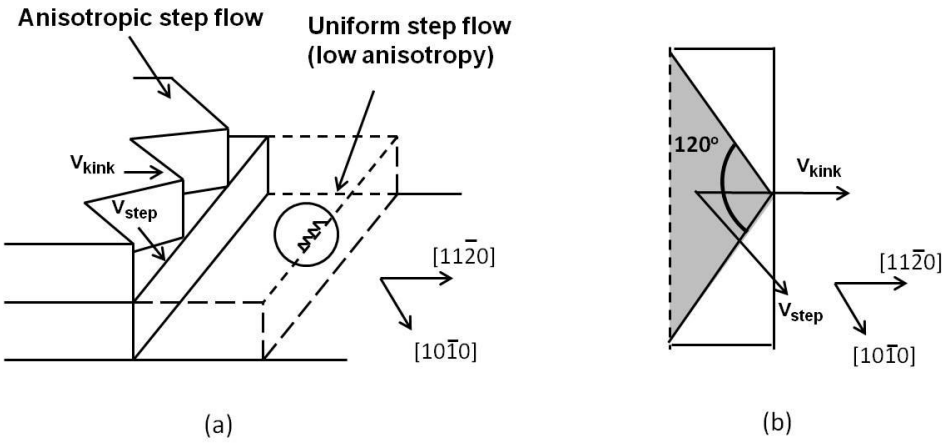

Figure 3.7 Step crossover in the epilayer surface by anisotropic step-flow. A uniform growth shows very low anisotropy. The grey region in (b) shows the region covered by epigrowth in both directions. The white region would have been grey too if the growth rate along [10-10] were high enough.

(as shown in Fig-3.7b). As the growth progresses, growth along the [11-20] direction overtakes growth along [1-100] and causes the zigzag crossover pattern. This phenomenon is expected to be more prominent for low offcut epitaxial growth as the step-flow growth has to traverse wider (43.3 nm in the present case) step terraces. Another important factor promoting anisotropic step bunching is poor quality sawing of

the substrate wafer that reveals open facets along both [10-10] and [11-20] directions, promoting step flow in both directions.

Although step bunching appears to be inevitable, it can be minimized by tuning the ratio of the carbon and silicon species on the step terrace, as the surface diffusivity of the two species are not identical. Experimental results show that the step bunching is typically smaller for low C/Si ratio growth. However, a Si rich environment promotes surface defects, such as polytype inclusion. Therefore, an optimum C/Si ratio needs to be found for the optimization of the surface morphology.

3.2.3 Growth on low offcut substrate

There has been significant interest in the epitaxial growth of SiC on low-offcut substrates owing to the observed reduction of defect density and the cost benefits[48][49]. As illustrated in Fig-3.8, the low offcut increases the probability of the conversion of basal plane dislocations (BPD) into more benign threading edge dislocations (TED), while the cost benefit comes in the form of low material wastage during creating the surface offcut.

Table 3.3 Terrace width for various offcut angles

Offcut angle (θ)	Terrace length (4H), nm	Terrace length (6H), nm
8^o	8	5
4^o	14	11
1^o	58	43

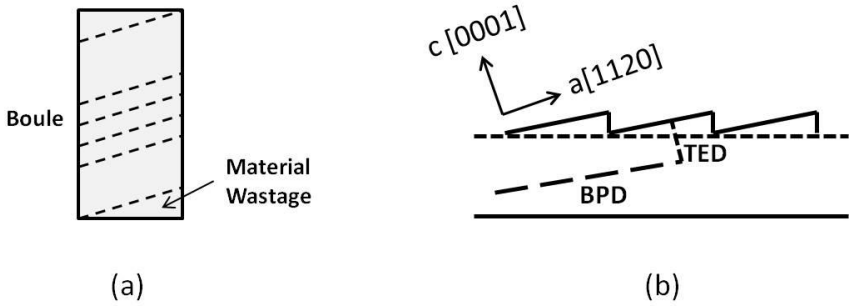

Figure 3.8 Motivation for low offcut growth. (a) Low offcut reduces material wastage. (b) A low offcut angle increases the distance traversed by the basal plane dislocation (BPD), and increases the probability to convert into a threading edge dislocation (TED).

The major challenge in the epitaxial growth on low offcut substrate is the increased terrace nucleation leading to polytype inhomogeneity in the crystal. Kimoto et al. [4] argued that the longer terrace width (see table-3.3) in lower offcut substrates increases the probability of adatom supersaturation on the terrace, creating island-like growth of a different polytype. However, recent studies indicate that the foreign polytype inclusion is caused by adatom nucleation in the defects or imperfections on the growth surface, rather than from island growth on the terrace [43]. Therefore, the key requirement for uninterrupted step-flow growth on low offcut substrates is to reduce the propensity of the adatoms being captured by the defect sites before reaching the step edges. This requirement can be fulfilled following a two-pronged

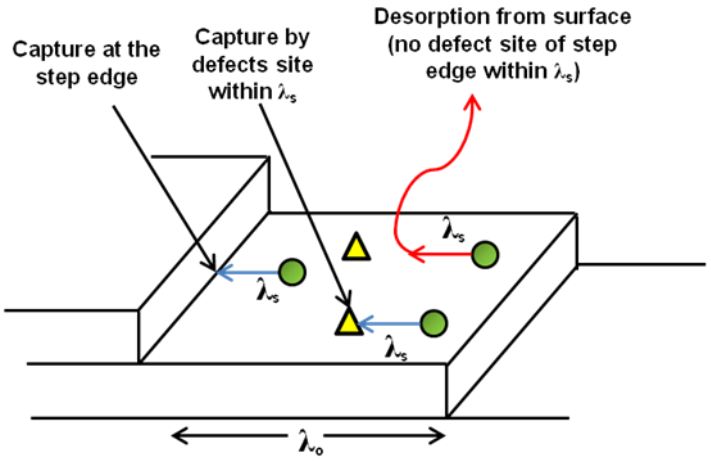

Figure 3.9 The individual adatoms nucleate at the step edge or a defect site on the terrace only if the nucleation site is within its diffusion length λ_s. In case of long λ_s, the adatoms have larger probabilities of being captured by the step edge or a defect site. A shorter λ_s reduces that probability. In this case, inhomogeneous nucleation at the defect sites becomes less severe, but at the expense of the growth rate, as the rate of nucleation at the step edges also decreases.

approach—by (i) reducing the density of crystallographic defects and surface imperfections (e.g., polishing damages) by proper surface preparation[51] and (ii) reducing the surface diffusion length of adatoms by employing a desorption-controlled growth condition.

It is to be noted that only the adatoms adsorbed within a diffusion length from the surface defect sites participate in polytype-inhomogeneous nucleation (Fig-3.9). In the case of a long diffusion length (in the order of the terrace length or longer), as in silane-precursor growth, all the adatoms adsorbed on the growth surface has a finite probability to meet any defect site present on the step-terrace before reaching the step edge. On the other hand, adatoms with shorter diffusion lengths, as in the case of DCS-precursor growth, participate in nucleation, whether in the step edge or at a defect site, only if the nucleation sites are within their respective diffusion lengths. Otherwise, they evaporate

from the surface. As a result, the propensity of adatoms being captured in the defect sites diminish considerably and the polytype homogeneity gets better.

3.2.4 Chlorinated precursor CVD of SiC: A solution

The conventional Si precursor for the epitaxial growth of SiC is silane (SiH_4). At the growth temperature, silane breaks into atomic Si by the following reaction—

$$SiH_4 \rightarrow SiH_x + H_2$$
$$SiH_x \rightarrow Si(g) + H_2$$

The atomic Si is highly reactive and is known to form Si clusters at the growth front, impeding the step-flow growth. One way of minimizing the cluster formation is raising the temperature, which again reduces the growth rate considerably.

Table 3.4 The dissociation energy of the various bonds present in the gas phase at the growth front (at 25^{o}C)

Bond	Dissociation energy kJ/mol
C=C	602
Si-Si	218.4
Si-H	318
Si-Cl	381

As Si forms a stronger bond with halogens (table-3.4), such as chlorine, addition of a halogenated species in the source gas can provide a more controllable supply of Si to the growth front. Addition of HCl during the epitaxial growth was reported to improve the surface morphology, and allow higher rate of flow of the source gases. Various

chlorinated silane precursors have also been investigated in 4H-SiC homoepitaxy. These include methyltrichlorosilane (CH_3SiCl_3, MTS), dichlorosilane (SiH_2Cl_2, DCS) and trichlorosilane ($SiHCl_3$, TCS) [52][53][54][55].

The chlorinated precursors are even more important for epitaxy on low offcut substrates, as the wide terraces increases the density of Si droplet formation, which may serve as the preferential nucleation sites for non-homogenous polytype inclusion. For the current study, the homoepitaxial growth of 6H-SiC on 1^o offcut substrate was performed using dichlorosilane (DCS) as the Si precursor. In the case of DCS precursor growth, the chlorinated species reaching the surface (e.g., $SiCl_2$) is more volatile compared to the atomic Si species produced by the conventional silane precursor [55][56]—

$$SiH_2Cl_2 \rightarrow SiCl_2 + H_2$$

The desorption of these species counteracts the reactant adsorption process at the growth surface, which is essential to step flow growth. Hence the use of DCS is expected to render lower crystal growth rates than that by silane precursor in similar growth conditions. However, it is to be noted that, in the case of DCS, the availability of the molecular species at the growth surface is enhanced by the suppression of precursor loss to gas phase nucleation and parasitic deposition on the reactor parts, which plague epitaxial growth using silane. As a consequence, despite higher desorption rate, the growth rates obtained using DCS precursor were found experimentally to be comparable to that obtained using silane [57]. Furthermore, for DCS precursor growth, the cleaner growth environment rendered by the suppression of gas phase nucleation and parasitic deposition allows high precursor flow rates, facilitating higher growth rates than

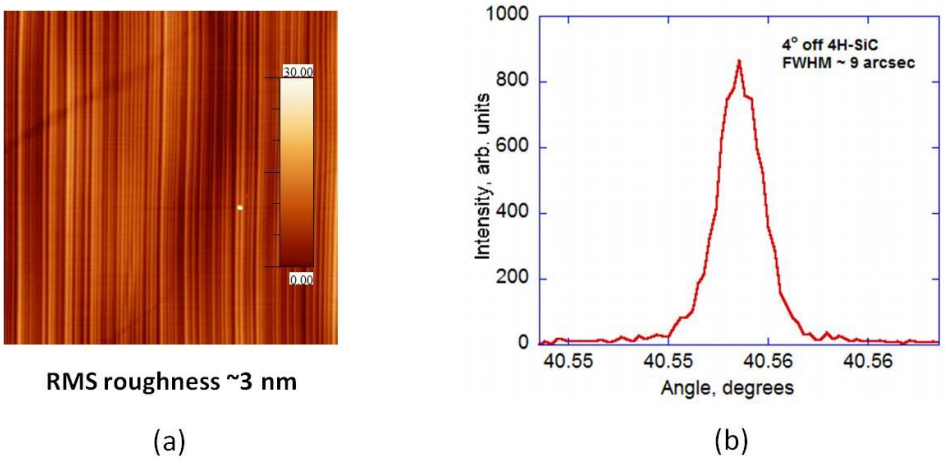

Figure 3.10 (a) A 20 μm x 20 μm AFM image of a 4° offcut 4H-SiC epilayer surface (R_g ~15 μm). (b) XRD rocking curve of the same crystal. The XRD resolution is ~7arcsec.

attainable using silane in similar growth conditions without introducing polytype inhomogeneity and surface defects in the grown crystal [55]. Fig-3.10 shows the AFM image and the XRD rocking curve of a 4° offcut substrate grown using DCS. The growth kinetics and grown the epilayer characteristics are discussed in detail in the next section.

3.3 EXPERIMENTAL RESULTS: CVD ON LOW OFFCUT SUBSTRATE USING DICHOLOROSIALANE

For this study, 1 cm x 1 cm samples cut out from a 1° offcut semi-insulating 6H-SiC substrate were used. Prior to growth, the substrate was cleaned using the RCA wafer cleaning procedure that involved sequential rinsing in trichloroethylene (TCE), acetonol, methanol and de-ionized water. The residual oxide layer on the wafer was etched by hydrofluoric acid (HF) before loading into the deposition reactor.

The reactor was evacuated to ~ 10^{-6} torr using high vacuum pumps. A degassing bake was performed at 800°C under vacuum to drive off water vapor and other gaseous impurity trapped in the insulators. A short duration (~5 min) H_2 etch was performed at the growth temperature (> 1500°C) before the Si precursor (DCS) was introduced. For the optimization of the CVD process, the temperature was varied from 1450°C to 1550°C. The best surface morphology and growth rate was observed in the low temperatures. The subsequent investigation of the C/Si ratio was performed at 1470°C. All growth was performed at a chamber pressure of 80 torr.

3.3.1 Effect of growth temperature

The dependence of growth rate on growth temperature was observed over a temperature range of 1470 - 1550°C. The C/Si ratio was kept fixed at ~1.5 for all temperatures. The growth rates measured by FTIR are plotted against the process temperature in Fig-3.11. The observed decrease in the growth rate with increased

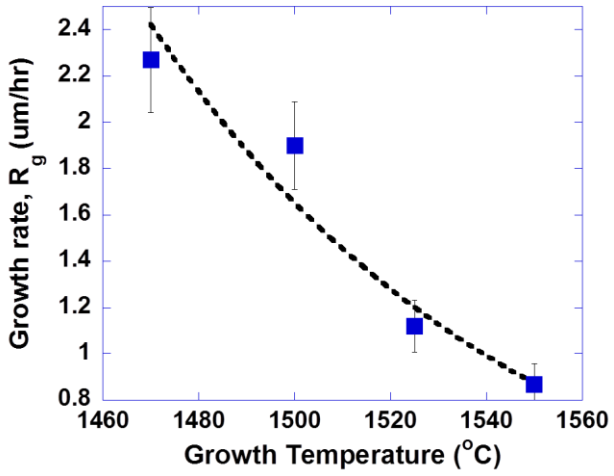

Figure 3.11 Growth rates of 1° 6H-SiC epilayers at different growth temperatures. The dotted line is intended to be a guide to the eye. The growth rate is limited by desorption at high temperatures and the rate decreases.

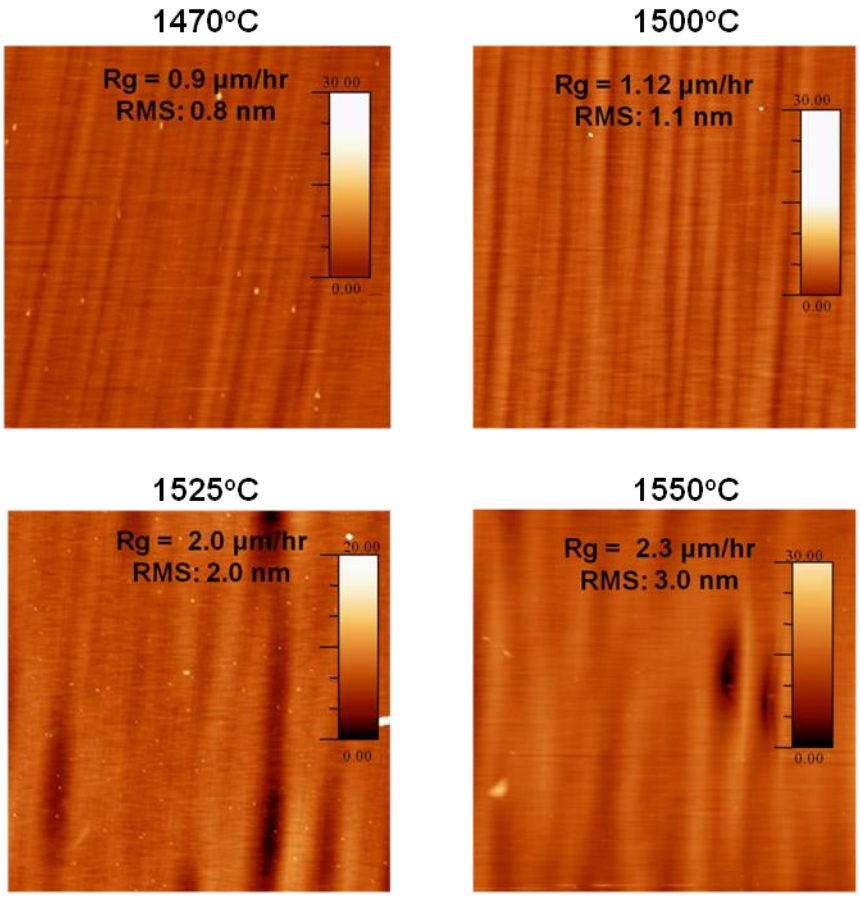

Figure 3.12 20 µm x 20 µm AFM images of 1° offcut epilayers grown at various temperatures. The epitaxial growth rate decreases as the growth temperature increases. The lower growth rate at higher temperatures, however, reduces step-bunching and improves the surface morphology.

temperature can be attributed to the increased rate of desorption of reactant atoms from the growth front.

The rms surface roughness showed a similar dependence on the growth temperature as the growth rates. However, the variation is very small and can be assumed to be a consequence of the growth rate variation. The AFM images in Fig-3.12 show the surface morphology of 6H-SiC epilayers grown at different temperatures. The epilayer surfaces showed uniform step-flow growth over the entire sample area despite heavy step-bunching and occasional step anisotropy. Step-bunching was observed at all four

growth temperatures and was the major determinant for the surface roughness. On the other hand, anisotropic step structures, commonly known as step crossovers, were observed at lower temperatures, which, can be assumed to be a consequence of the higher growth rates at these temperatures.

3.3.2 Estimation of the surface diffusion parameters

Kimoto et al. developed a theoretical framework based on the step controlled growth theory of Burton, Cabrera, and Frank (the BCF theory) that provides deeper insight into the experimental results [43][44]. The model assumes that the reactant atoms are adsorbed on the growth surface upon reaching the step terraces (Fig-3.3). When the adsorbed atoms reach the step edges, they are captured by the dangling bonds therein and the step-flow crystal growth process initiates. The step edges are considered perfect sinks for the adatoms, i.e., all the adatoms reaching the nearest step are assumed to incorporate into the growing step edge. However, owing to the concurrent thermal desorption process, not all adatoms on the step terrace can reach the step edges. The length an individual adatom can traverse on the step terrace before being desorbed from the surface is defined as the surface diffusion length, λ_s. Therefore, only the adatoms adsorbed within one surface diffusion length from the step edge will participate in step flow growth.

Kimoto et al. defined a condensation coefficient η that relates the growth rate with the incoming flux of reactant species,

$$R = \eta J\left(\frac{h}{n_o}\right) \tag{3.1}$$

Here, J is the incoming flux of adatoms, h is the surface step height and n_o is the density of adatom sites on the terrace. The 6H-SiC Si-face surface has a propensity to

form 3 bilayer high microsteps, which renders a microstep height (h) of 0.756 nm. The density of adatom sites (n_o) can be found by estimating the surface packing density on the [0001] plane, which amounts to ~10^{15} cm^{-2}. Assuming the supply of Si adatoms to the growth front to be the only limiting factor of the growth rate, the incoming adatom flux (J) in the experimental temperature range can be estimated using a gas diffusion model resembling Fick's Law,

$$J = \frac{-DN_o}{\delta} \tag{3.2}$$

Here, D is the diffusivity of DCS in hydrogen, δ is the thickness of the boundary layer and N_o is the inlet reactant concentration (cm^{-3}). As the growth rate is Si mass transfer limited, only the diffusion of DCS molecules through the hydrogen carrier gas has been considered in the calculation of adatom flux. The reactant concentration reaching the boundary layer can be estimated from the partial pressure of DCS in the flowing gas mixture using the ideal gas equation, PV = nRT. In the present case, N_o (=n/V) was in the order of 10^{13} cm^{-3}. The thickness of the stagnant layer δ, on the other hand, can be estimated using a boundary layer model resembling that used for horizontal CVD reactors, as described in [59]. For the present reactor design the stagnant layer thickness turned out to be ~ 1 mm. The diffusivity of DCS in hydrogen was calculated using the empirical expression developed by Reid and Sherwood [60],

$$D_{AB} = \frac{0.0018583T^{3/2}}{P(\sigma_{AB})^2\Omega_{D,AB}}\sqrt{\frac{1}{M_A}+\frac{1}{M_B}} \tag{3.3}$$

Table 3.5 Parameters used in the calculation of diffusivity of DCS through H_2.

Temperature (^oC)	Collision integral Ω_{AB}	Lennard-Jones potential, σ_{AB}	Diffusivity, D ($cm^{-2}s^{-1}$)
1470	0.721	12.29	7.00
1500	0.718	12.50	7.20
1525	0.717	12.68	7.32
1550	0.715	12.80	7.54

*A = DCS, B = H_2

Here, A and B subscripts denote the two species in the gas mixture. The Lennard-Jones potential function, σ_{AB} and the collision integral Ω_{AB} can be approximated from the critical constants (temperature and volume) of each gas [61]. Using equation (3.3), the value of diffusivity of DCS in H_2 carrier gas was calculated to be in the range of 7.0 – 7.5 $cm^{-2}s^{-1}$. Table-3.5 lists the various parameters used in this calculation.

Using the calculated values of the different parameters in equation (3.2), the adatom flux density was estimated to be around 1.5 x 10^{15} $cm^{-2}s^{-1}$ at all experimental growth temperatures, which was verified with a Virtual Reactor® simulation. The condensation coefficient, η at different growth temperatures can then be estimated by putting the experimental growth rate values found at different growth temperature into equation (3.1). The calculated values of η are shown in table-3.6. As can be seen from the table, the value of η decreases as the growth temperature is increased, which indicates less efficient adatom incorporation at higher temperatures.

Table-3.6 Effect of growth temperature on the growth rate determining parameters.

Growth Temp. (^oC)	Growth rate, R_g (μm/hr)	Condensation coefficient η	Surface diffusion length, λ_s (nm)
1470	2.3	0.54	13
1500	2.0	0.49	11
1525	1.1	0.27	9
1550	0.9	0.22	5

From a step flow growth point of view, the condensation ratio is defined as,

$$\eta = \left(1 - \frac{n_{so}}{J\tau}\right) \frac{\tanh\left(\frac{\lambda_o}{2\lambda_s}\right)}{\left(\frac{\lambda_o}{2\lambda_s}\right)} \tag{3.4}$$

Here, n_{so} is the adatom concentration in equilibrium and τ is the characteristic diffusion time of the adatoms on the surface. n_{so}/τ, therefore, denotes the desorption rate from the growth front.

Thus, the $\left(1 - \frac{n_{so}}{J\tau}\right)$ term quantifies the efficiency of the equilibrium diffusion process. This epitaxial growth process takes places under large supersaturation, to enable the growth process to proceed, leading to the boundary conditions used in the BCF model. At the step edges, where the adatoms are incorporated, the partial pressure of the silicon is the equilibrium partial pressure, which is much smaller than the partial pressure of silicon in the growth vapor. Furthermore, the mean free path of molecules at these conditions is ~μm's, while all the relevant dimensions, such as the reactor geometry, boundary layer thickness etc. are all mm's or larger, so the molecular transport is all Boltzmann in nature, as we assumed in equations (3.2) and (3.3). Therefore, the Knudsen transport at these temperatures and pressures is negligible, and the equilibrium rate of

Knudsen desorption is expected to be much lower than the incoming flux of 5 x 10^{15} $cm^{-2}s^{-1}$. Then the condensation coefficient is determined solely by the term $\frac{\tanh\left(\frac{\lambda_o}{2\lambda_s}\right)}{\left(\frac{\lambda_o}{2\lambda_s}\right)}$, which determines the probability of an adatom on the step terrace to migrate all the way to the step edge and get incorporated to the advancing growth front. It can take values ranging from 0 to 1 depending on the value of surface diffusion length (λ_s) relative to the terrace width (λ_o). The width of a typical microstep can be calculated to be h/tan(1^o) = 43.3 nm (h being the height of 3 bilayer high microsteps), which is in correspondence to the value obtained from AFM. A surface diffusion length shorter than half of the terrace width indicates a strong desorption process at the growth front and renders an η less than unity. On the other hand, if λ_s is comparable to or greater than half of the terrace width, η approaches unity, which is indicative of a weaker desorption process at the growth front.

Since the η values are known from equation (3.1), the surface diffusion lengths (λ_s) at the various growth temperatures can be extracted using equation (3.4). Table-3.6 lists the extracted λ_s values for each growth temperature along with the corresponding growth rates and condensation coefficients. As is shown in table-2, the surface diffusion lengths (λ_s) are shorter than half of the terrace width λ_o (~43.3 nm) at all the growth temperatures used in this study. As the growth temperature is increased, desorption from the growth front increases, which is reflected by the diminishing surface diffusion length. Fig-3.13 illustrates the Arrhenius dependence of λ_s on the growth temperature.

Fig-3.13 shows the λ_s values estimated in the present along with the values given by Kimoto et al. for a silane-based epigrowth process. As is obvious from the figure, the surface diffusion lengths obtained for DCS are an order of magnitude lower than those

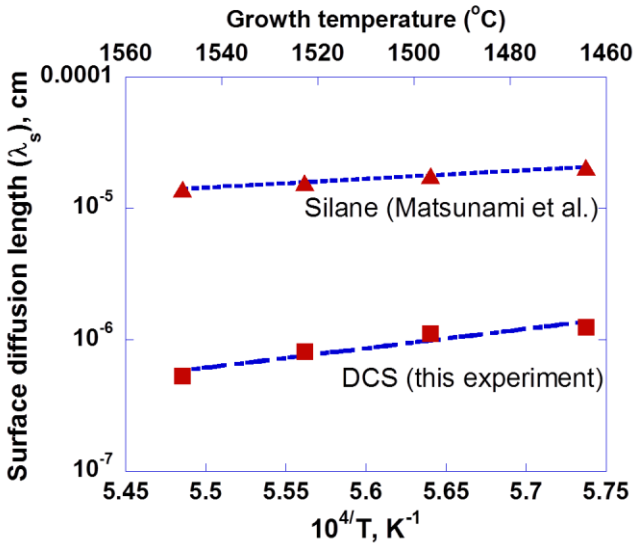

Figure 3.13 Effect of growth temperature on the surface diffusion length—comparison between silane (square) and DCS (triangle) precursor growth. The silane data is interpolated from the data reported in ref. 10 for the temperatures used in the current experiment. Both the DCS and silane data show a similar Arrhenius temperature dependence.

estimated for a silane precursor. The shorter λ_s for the chlorinated precursor reflects the higher rate of desorption of the Si containing species. As has been reported by various groups, epigrowth using a chlorinated species proceeds by a thermal dissociation of the chlorinated species into a more stable $SiCl_2$ [58], whereas in a silane-based process the epigrowth is dominated by atomic Si produced in the gas phase. Since $SiCl_2$ is a more stable species as compared to atomic silicon, the temperature window in which the vapor pressure over the substrate is dominated by atomic Si is shifted toward higher temperatures as compared to that in silane-precursor growth. This implies that the desorption process at the growth surface is stronger for the chlorinated epigrowth, which is manifested by a shorter diffusion length of the adatoms on the growth surface, as compared to silane-based epigrowth. As a consequence, the step-flow growth rate should be lower for DCS-precursor growth. However, as discussed in the introduction, the use of

DCS or other chlorinated precursors renders suppression of gas-phase nucleation and/or parasitic deposition, facilitating higher growth rates while maintaining surface and crystal quality.

3.3.3 Effect of the C/Si ratio at the source gas

The C/Si ratio of the source gas was varied from 0.9 to 2.2, while keeping the growth temperature fixed at 1470^{o}C. As can be seen in Fig-3.14, epilayer surfaces free of triangular or carrot defects were obtained over the whole C/Si ratio range.

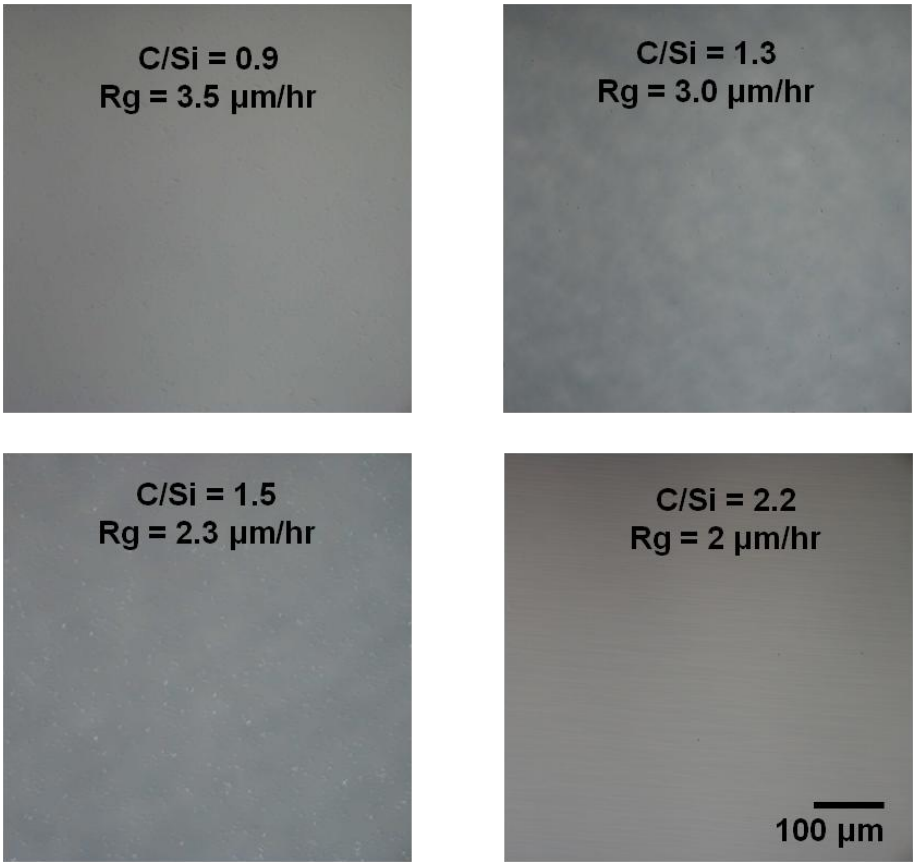

Figure 3.14 Nomarski optical images of 1^{o} offcut epilayers grown at various C/Si ratios. Carrot and triangular defects were very few and were observed only in the 1mm exclusion zone at the edge. The growth duration was 1 hour for all of the epilayers.

Step bunching was observed for all C/Si ratios. The AFM images in Fig-3.15 show the macro-step structures on the epilayer surfaces for various C/Si ratio. The rms roughness values and the epitaxial growth rates are also shown in the figure. Although the variation in the roughness values is not very significant, as a general trend, the values of surface rms roughness tended to increase with increasing C/Si ratio. Moreover, significant step crossover due to anisotropic step bunching was observed at all C/Si ratios, as shown by the arrows in Fig-3.15.

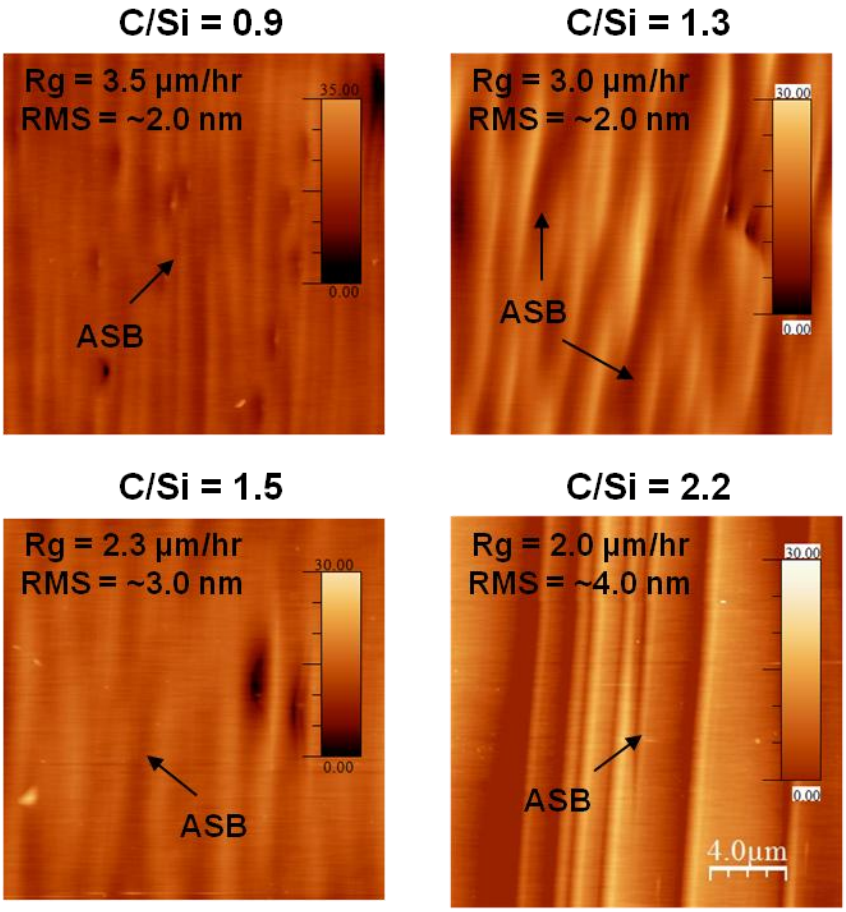

Figure 3.15 AFM images (20µm x 20µm) of 1° offcut epilayers grown at various C/Si ratios. The arrows show regions with anisotropic step bunching. The growth duration was 1 hour for all of the epilayers.

Doping of the epitaxial layers was achieved by site competition epitaxy [62], where nitrogen atoms substituted the carbon atoms and boron dopants substituted the silicon atoms in the SiC lattice. No external supply of dopant atoms was used. Doping levels were varied by changing C/Si ratio in the gas source, thereby suppressing or promoting the incorporation of desired dopant atoms. We observed the variation in doping level with C/Si ratio varying from 0.96 to 1.58.

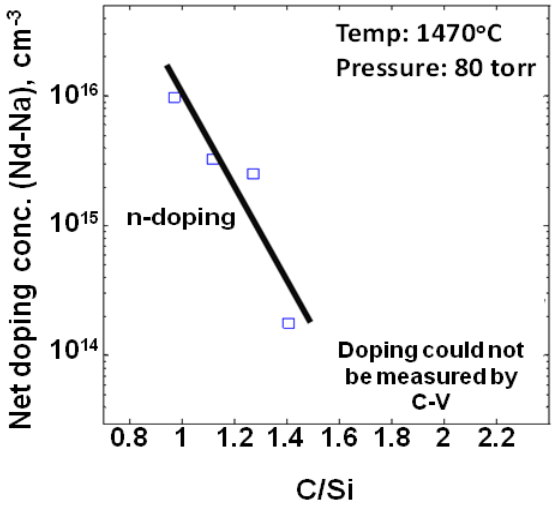

Figure 3.16 Net doping measured by C-V at various C/Si ratios for epilayers grown at 1470°C.

Fig-3.16 shows the variation of doping level of the 1° off epilayers with the increase in C/Si ratio. N-type doping was achieved at low C/Si ratios. The doping level showed a sharp dependence on the C/Si ratio, varying over two decades (~10^{16} to 10^{14}) in the C/Si ratio range of 0.96 – 1.53. Beyond a C/Si ratio of 1.53, the doping levels went below the detection limit of the Hg probe C-V measurement system (~10^{14}). In higher offcut epitaxy (4 and 8°) using DCS in the same reactor, site-competition at sufficiently high C/Si ratios produced p-doped epilayers. In the present series of experiments, however, no transition in the p-doping regime was observed. A further increase in C/Si

ratio (beyond ~1.4) kept producing very low-doped (immeasurable) epilayers. Although the absence of p-doping is not fully understood, it can be assumed that the sticking coefficient of B adatoms is significantly lower than that of N adatoms in 1^{o} epilayers. An alternative possibility is that boron dopants incorporated in the crystal may have been passivated by forming a B-H complex with hydrogen interstitials [63][64].

3.4 SiC EPILAYER CHARACTERIZATION

3.4.1 Crystal quality

X-ray diffraction and Raman spectroscopy were performed on the epilayers for evaluating the crystal quality and polytype uniformity. The X-ray diffraction rocking curves obtained from the (0006) plane of a typical 3.5 μm thick epilayer (Growth rate, R_g = 3.5 μm /hr) is shown in Fig-3.17a. The full width at half maxim of ~ 10 arcsec indicates a fairly good crystal quality since the system resolution permits FWHM values not less than 6-8 arcsec for pure crystals. Other epilayers studied in this work exhibited similar narrow rocking curves.

Raman shift spectra were obtained using a 25 mW 632 nm He-Ne laser excitation source and a Jobin-Yvon Raman spectrometer equipped with charge-coupled-detector array for emission detection at room temperature. As reported by Nakashima et al. [65], the phonon modes of interest in 6H-SiC include the planar TO modes at 797, 789 and 767 cm^{-1} respectively and an axial LO mode at 965 cm^{-1}. For cubic SiC, a dominant TO mode is found at 796 cm^{-1}. In case of a mixed polytype sample, the relative intensity between

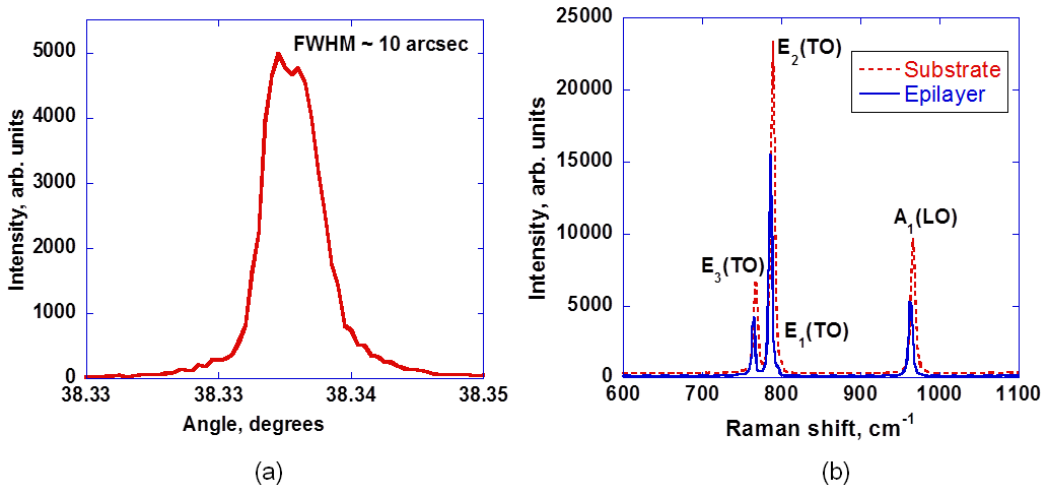

Figure 3.17(a) X-ray diffraction rocking curve from the (0006) plane of a 3.5 µm thick 6H-SiC epilayer grown on 1° off 6H-SiC substrate. (b) Typical room temperature Raman spectra from the same sample.

the peak at 796 cm^{-1} and the other characteristic peaks can be used as a measure of polytype uniformity.

Fig-3.17b shows the Raman spectrum averaged over an area of 40µm x 40µm of a typical 6H-SiC epilayer grown on a 1° off substrate alongside the Raman shift spectrum obtained from the bare substrate. The characteristic TO and LO modes are visible at 765, 786 and 963cm^{-1}. The very low intensity of the 797 cm^{-1} line indicates negligible 3C inclusion in the crystal structure, which is possibly a consequence of the desorption-limited growth mechanism by DCS.

3.4.2 Non-destructive defect characterization: Photoluminescence spectroscopy

The most common technique of defect study is KOH etching. This is a destructive process where a thin layer of material is etched off the surface of the crystal. The etching process is anisotropic in the various crystal planes and therefore, produce characteristic etch pits on the surface at the defects sites, as shown in fig-3.18. Because of the

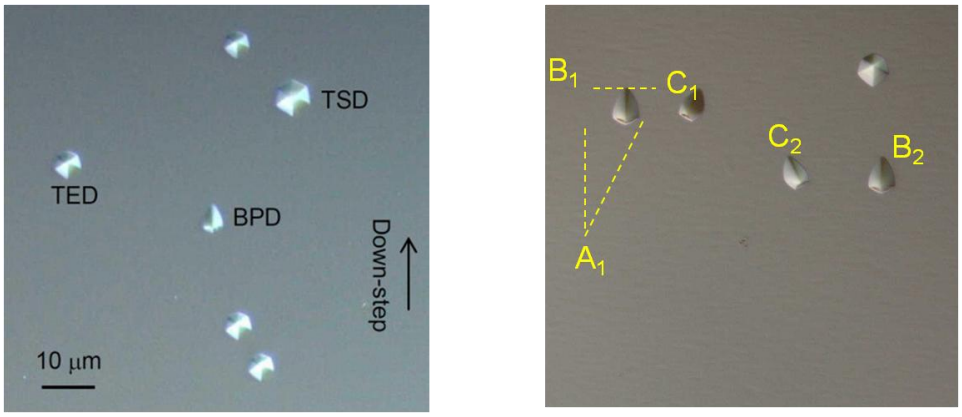

Figure 3.18 Defect delineation using KOH etching. As shown on the figure, the diamond shaped etch pits (B_1, C_1, B_2, C_2 in the figure to the right) originate from BPD's. The symmetric hexagonal pit comes from TED's and TSD's. The TED pits are smaller and do not show a core at the center. The TSD pits are large and show larger plateaus at the center. The triangular area $A_1B_1C_1$ denotes a stacking fault region.

destructive nature of this characterization scheme, the epilayer becomes unusable for further device fabrication.

A novel non-destructive technique for estimating the stacking fault density and the carrier lifetime in the epitaxial crystal is proposed here. The technique is based on room temperature UV photoluminescence spectroscopy. photoluminescence (PL) from SiC epilayers is a convenient tool for identifying the in-grown stacking faults (IGSF) in the epilayers. Microphotoluminiscence of the IGSF's show characteristic stacking fault emission lines at wavelengths of 420, 455, 480 and 500 nm along with the band edge emission peak at ~391nm [66][67]. For broad area measurements, however, these peaks may overlap with each other to create broad gaussian peaks rather than showing up as individual emission lines (fig-3.19). Also, for very thin samples (2~10μm), the PL spectrum shows significant emission from the substrate along with the epilayer PL. The room temperature PL spectrum of SiC is often dominated by green luminescence from

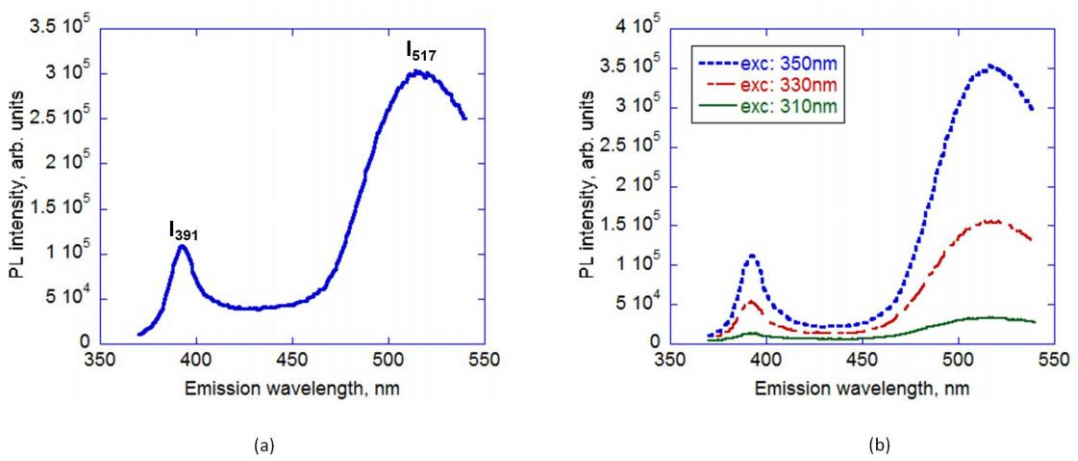

Figure 3.19 (a) Typical PL spectrum from a 4H-SiC substrate. The band-edge and boron related peaks are denoted as I_{391} and I_{517} respectively. (b) The peak ratio varies with excitation wavelength (mentioned in the legend).

boron related deep levels [68]. The deep levels are created by boron atoms sharing the same superlattice as a donor atom. Upon illumination by above bandgap wavelengths, the yellow-green luminescence is produced by nitrogen-boron donor-acceptor pair (DAP) recombination of the injected minority carriers [68].

The absorption coefficient α is proportional to $(E-E_g)^2$, where E is the excitation energy and E_g is the band gap of the material. Increasing the energy of the excitation UV light, therefore, decreases absorption length [69]. This change in absorption length of the excitation enables depth profiling of the epilayers. At long wavelengths the excitation can penetrate deep into the epilayers and even into the substrate. As a result the PL spectrum shows significant emission from the substrate material. On the other hand, short wavelengths are confined into the epilayers only, and the PL spectra at these wavelengths reflect characteristics of the epilayers material. The difference between the substrate emission and epilayers emission can be quantified in the form of intensity ratio of the band edge peak and the boron-related DAP emission peak. The dependence of this peak

ratio (I_{517}:I_{391}) on the excitation wavelength varies depending on the density of IGSF in the epilayers.

Room temperature PL spectrum was obtained using a Horiba Jobin Yvon PL spectrometer. The UV source was a 450W Xe lamp equipped with double grating monochromators for selecting a central excitation wavelength and its bandwidth. The excitation wavelength could be varied from 200 to 900nm. In our experiments excitation wavelengths of 275~360nm were used with a bandwidth of 5nm. The emission was collected by a photomultiplier tube coupled with single photon counting circuitry through an emission monochromator.

The room temperature PL spectra of the epilayers show teo characteristics peaks— the band-edge emission peak at 391nm and a broad boron-nitrogen donor-to-acceptor (DAP) pair recombination peak centered at ~517nm. Photoluminescence data were obtained for various excitation wavelengths from 270nm to 360nm. The DAP peak was present at all wavelengths, but its relative intensity with respect to the band-edge peak varied with excitation wavelength (fig-3.19b). The trend in the ratio change with excitation wavelength provides information about carrier diffusion length, which can be used for identifying in-grown stacking faults.

The epilayers grown on 8^o substrates were etched by molten KOH. The shell-like etch pits that mark the boundaries of the IGSF's reveal their locations in the epilayers. The density of stacking faults was estimated by counting the etch pits using a Nomarski optical microscope [70][71].

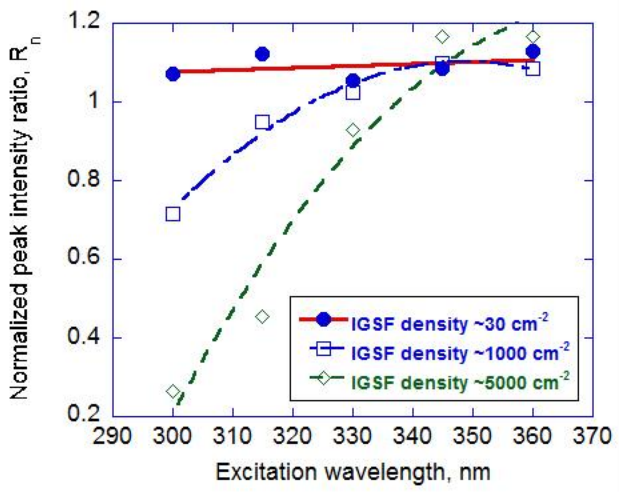

Figure 3.20 Peak intensity ratios for three 12 µm samples grown with IGSF densities of ~10cm^{-2} and >1000 cm^{-2}. The R value for the low IGSF sample follows the substrate profile (R~1). The ratio for the high IGSF sample goes down with decreased absorption length.

As mentioned earlier, for a given sample, the intensity ratio (R) of the boron peak (I_{517}) and the band-edge peak (I_{391}) is a function of excitation wavelength (λ_{ex}). For a bare substrate, these R values remain almost unchanged, although the nominal value of the ratio varies from substrate to substrate. For epilayers, however, this R-value shows a dependence on λ_{ex}. Fig-3.20 shows R vs. λ_{ex} profiles for three 12 µm epilayers with different stacking fault densities. The R values used here are normalized by substrate R values to eliminate spectral artifacts. As summarized in table-1, the R values decrease significantly with decreased λ_{ex} for the samples with high IGSF density. On the other hand, the low IGSF sample shows very little variation and follows the trend shown by the substrate (i.e., normalized R~1 for all λ_{ex}). Samples grown on the same substrate show similar R values as the substrate in the long λ_{ex} regime (i.e., greater absorption length). The overall decreasing trend in the R values with decreased λ_{ex} in all epilayers indicates that the boron deep level concentration in the epilayers is less than that in the substrate.

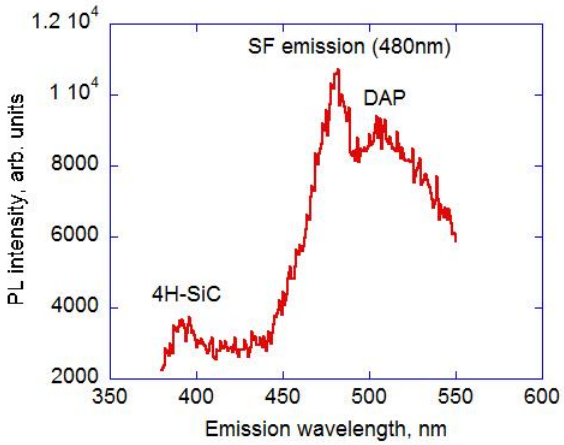

Figure 3.21 Emission line at 480nm from a 20um thick epilayer with IGSF density >10,000 cm^{-2} at an excitation wavelength of 310nm.

From these observations, it can be said that at longer wavelengths the emission from the substrate dominates the PL spectra. For the low IGSF sample the influence of the substrate persists even at shorter wavelengths, whereas for high IGSF samples, the emission from the epilayers dominates. For epilayers with very high IGSF densities (>10,000cm^{-2}) a sharp emission peak is observed at 480nm for short wavelength excitations (Fig-3.21).

The substrate dependence of the PL spectrum can be explained in terms of a carrier diffusion model, as illustrated in fig-3.22. For the low IGSF sample, the photogenerated carriers have long diffusion lengths (at least > 50µm), and they can move all the way to the substrate without being recombined in the epilayers. The carriers recombine at the substrate and give off PL emission. On the other hand, high IGSF density in the epilayers reduces the diffusion length of the photogenerated carriers. In this case, they recombine in the epilayers and show lower DAP emission from boron deep traps present mostly in the substrate. In the presence of very high density of IGSF in the

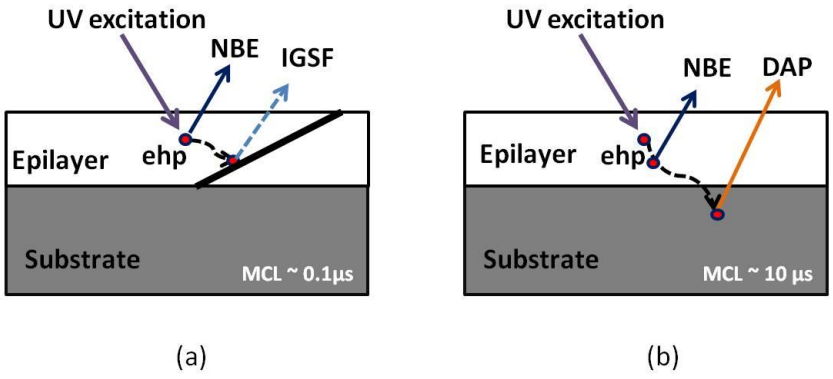

Figure 3.22 The photoluminescence technique of stacking fault density estimation. (a) In the presence of SF, the DAP intensity is lower (b) In a defect-free crystal DAP intensity is the same for all excitation wavelength.

epilayer, the average spectrum shows sharp peaks corresponding to that particular IGSF type, as shown in Fig-3.21.

The technique was applied to epitaxial layers of various thickness, and was found useful up to an epi thickness of 70 µm. No DAP peak was observed from a 100 µm thick epilayer. Therefore, in a defect-free crystal the bulk minority carrier diffusion length can be as high 70 µm, which corresponds to a bulk minority carrier lifetime of ~10 µs.

3.5 CHAPTER SUMMARY

In this chapter the epitaxial growth of hexagonal SiC epilayers by chlorinated precursor CVD is described. It is argued that the rate of step flow growth was determined by two competing processes, adsorption and desorption of reactant species from the step terraces, and the latter dominates in chlorinated precursor growth. The mean surface diffusion length of the adatoms is estimated to vary from 5 nm to 13 nm in the experimental temperature range by using a model based on the BCF theory. The estimated diffusion lengths are an order of magnitude shorter than that reported for

silane-precursor growth in literature, implying a ‘desorption-controlled’ growth mechanism for DCS, which is ideal for polytype-matched homoepitaxy on low offcut substrates. Characterization results from XRD, raman and PL spectroscopy are presented, which confirm the high quality of the bulk of the crystal. A non-destructive technique of estimating the stacking fault density is proposed based on room temperature broad area photoluminescence spectroscopy.

CHAPTER 4

THE NI/SIC SCHOTTKY JUNCTION: INHOMOGENEITY AND INTERFACE STATES

The **s**ilicon carbide Schottky barrier diode is considered an attractive alternative to Si p-i-n junction diode for high power, high frequency applications such as PV inverters, power factor correction and motor control circuits [72]. The wide band gap and high critical electric field of SiC allows the fabrication of low leakage Schottky diodes with on resistance comparable to Si p-i-n devices. On the other hand, the low (near-zero) reverse recovery time allows the SiC Schottky diode to operate faster than the Si p-i-n diodes at the same current levels. Fig-4.1 shows a typical operation range of SiC Schottky and Si p-i-n diodes. SiC Schottky diodes are expected to replace the Si p-i-n diodes in the overlap region.

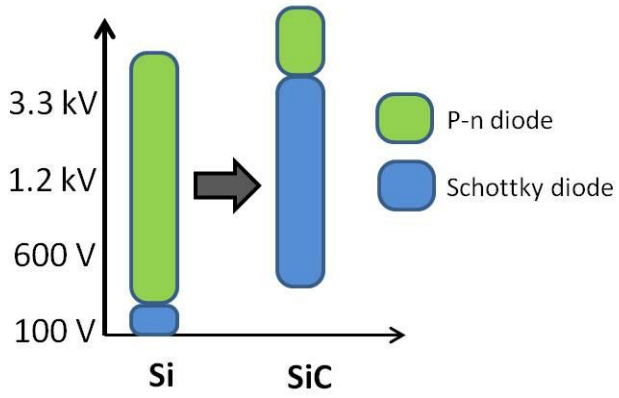

Figure 4.1 The application space of SiC Schottky diodes

Nickel is an attractive Schottky contact for SiC power electronics due to the large Schottky barrier it forms. The large barrier height offers very low reverse leakage, which is which is important for applications such as high frequency power switching [73] and solid-state sensors used in emission monitoring and nuclear radiation detection [74]. As deposited Ni was reported to form rectifying contact with 4H-SiC with barrier heights in the range of 1.3 – 1.6 eV [75]-[84], while the diode characteristics were found to be highly sensitive to the surface preparation prior to contact deposition [80][81].

Several groups reported formation of double barriers [80] and strong deviation from ideal thermionic emission behavior [81][84] in the as-deposited contacts. Annealing the Schottky interface in the temperature range of 600 – 800^{o}C was reported to flatten out double barriers and improve the ideality factor of the diodes. These annealed diodes also showed larger barrier heights than those for the as-deposited contacts. However, the statistical distribution of barrier heights over the entire substrate was not reported in most of these studies, and those reported showed significant 'inter-sample' variation [81]. Because of the technological significance of the Ni/SiC Schottky contact this type of non-uniformity and/or irreproducibility can be a bottleneck toward the realization of commercially viable high voltage Schottky devices. Moreover, the non-ideal behavior is not unique to the Ni/SiC interface. Similar issues exist with other high barrier junction metals such as palladium and platinum. Therefore, the interface effects that lead to non-ideality and non-uniformity in these junctions demand attention.

This chapter is devoted to the discussion on the fabrication and characterization of Ni/SiC Schottky barrier junction. The Schottky barrier inhomogeneity and interface effects are discussed based on the experimental results. In the discussion of Schottky

barrier inhomogeneity, Tung's interacting inhomogeneous barrier model is considered. The common pitfalls in the use of the theory are pointed out, and an applicability limit is drawn. The interface states are studied in relation to the anomaly in IV and C-V characteristics, and are identified to be a significant factor behind the experimentally observed non-ideality.

4.1 FABRICATION OF Ni/SiC SCHOTTKY BARRIER DIODES (SBD)

The fabrication of the SBD involves creating a metal/semiconducting junction by depositing metal on the surface of a semiconductor crystal. The fabrication process has been described in detail in fig-4.2. The process flow followed in the current study can be found in Appendices B and C.

The fabrication steps are as follows—

(a) *Growth of epitaxial layer*: Typical epilayers used in the study are 10~20 μm thick and lightly n-doped (~10^{15} cm^{-3}). Apart from the chlorinated precursor CVD described in last chapter, the novel low particulate fluorine chemistry was also used for growing low doped epitaxial layers for the Schottky junction study. Typical RMS roughness of the epilayer surfaces were 1 – 2 nm.

(b) *Sacrificial oxide*: The front-side is oxidized in air for 6-8 hrs at > 1100^{o}C for an oxide thickness of ~100 nm. Then the oxide is etched in 97% HF to get rid of the oxide. This step is necessary to clean up the epi surface which may have been contaminated by the end-growth conditions during epitaxy by CVD.

(c) *Back-side metallization*: The back side is lapped using diamond paste to get rid of any residual deposition and obtain a roughened surface for good ohmic contact

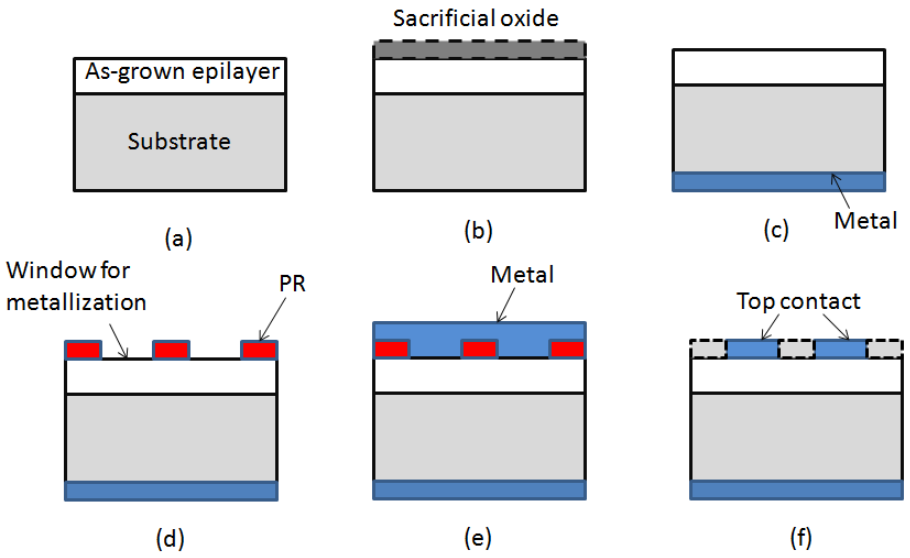

Figure 4.2 Fabrication steps of a schottky diode: (a) as-grown epilayer (b) Sacrificial oxide (c) Backside metallization (d) Photolithography and schottky dot formation (e) Front side metallization (f) Lift-off.

formation. Following an RCA cleaning procedure followed by an HF dip, an ohmic contact is formed on the backside by E-beam evaporation of a suitable metal. For an n+doped SiC substrate, the ohmic metal of choice is nickel. Nickel forms a large Schottky barrier with SiC, which makes it a good tunneling contact for the high doped substrate. However, the good ohmic property ($\rho_s \sim 10^{-5}\Omega cm^2$) comes from a 1000^{o}C anneal of the back contact. There is no unanimous agreement in the scientific community about the nature of the contact. However, it can be assumed that the annealing induced silicidation leaves behind clusters of C atoms at the interface, which together with the lapped, roughened surface provides the leakage path for the current.

(d) *Photolithography*: A photoresist (PR) layer is formed on the front surface (Si-face) of the epilayer by spin coating. The schottky dot patterns are transferred to the PR by UV exposure through a photo-mask and subsequent development of the PR film. Typical dot diameters used in the present study range from 50 μm to 250 μm.

(e) *Schottky contact deposition*: A Ni layer of thickness exceeding 100 nm is deposited on the resist-patterned front side. The deposition is done at pressure levels ~10^{-5} torr.

(f) *Lift-off*: The Schottky dots are formed by lifting-off the PR coating along with the undesirable metal film on top of it.

The Ni/4H-SiC diodes used in the current study were formed on 4H-SiC layers homoepitaxially grown by chemical vapor deposition in a hot-wall reactor. The epigrowth was performed on 2 cm x 2 cm pieces cut out of commercially available 4^{o} offcut Si-face 4H-SiC substrate wafers. 10 epilayers with thickness values of 10 ~ 25 μm and carrier concentrations ranging from 10^{14} to 10^{16} cm^{-3} were used in this study. The Schottky diodes were of three diameters-- 100, 150 and 250 μm. On each epitaxial wafer, a batch of 21 ~ 42 diodes were characterized.

4.2 RESULTS AND DISCUSSION: INTERFACE EFFECTS

4.2.1 The As-deposited characteristics

The as-deposited Schottky diodes showed highly non-ideal forward I-V characteristics with ideality factor values close to 2. Two types of I-V characteristics were observed— (i) single barrier and (ii) double barrier characteristics, as shown in Fig-4.3. The I-V characteristics shown in the figure were obtained from a batch of 21 diodes of the three different diameters. The epilayer thickness was ~25 μm and the carrier concentration was $5x10^{14}$ cm^{-3}. Of the > 20 diodes characterized on each wafer, 5 ~ 20% showed double barrier characteristics.

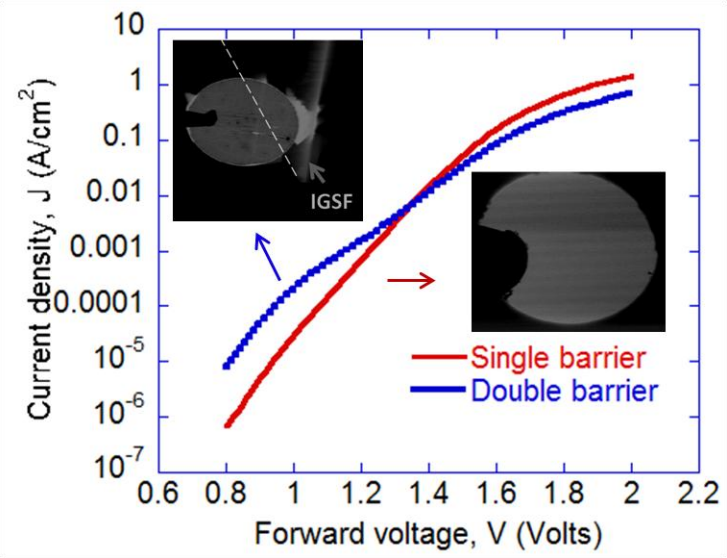

Figure 4.3 The correlation of the double barrier characteristics with the presence of stacking fault.

As the diode interfaces were studied by electron beam induced current (EBIC) measurement, a correlation was observed between the presence of stacking faults in the diode active area and the double barrier I-V characteristics. However, further study is required for establishing causation.

Majority of the diodes (> 80%), however, showed single barrier characteristics with tight statistical distribution. The barrier height and ideality factor extracted from the linear region of the ln(I) vs V characteristics shown in Fig-4.4a are 1.18 ± 0.043 eV and 2.02 ± 0.009 respectively. The low standard deviation of the single barrier characteristics indicate an interface anomaly that is evenly distributed across the wafer, e.g., interface traps, point defects, microscopic barrier inhomogeneity, surface roughness etc. On the other hand, the double barrier characteristics appear sporadically across the wafer, which can be attributed to interface anomaly with a non-uniform spatial distribution, such as surface and bulk crystal defects, as was also pointed out by Im et al..

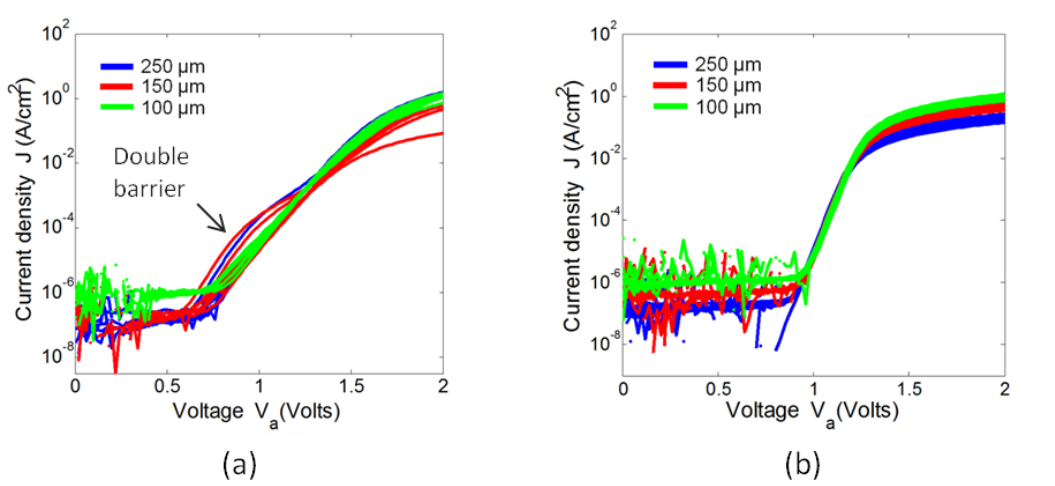

Figure 4.4 Forward J-V characteristics for (a) the as-deposited Schottky diodes (7 contacts of each size are shown, diameters shown in the legend) and (b) Schottky diodes annealed at 650°C for 120 sec. (14 contacts of each size shown).

4.2.2 Effect of post-deposition annealing

To study the effect of annealing on the diode I-V characteristics The as-deposited contacts were subject to 60 s rapid thermal annealing at 450°C and 650°C consecutively. Fig. 4.5 shows the effect of annealing on the forward I-V characteristics of a Schottky 'dot' of 150 µm diameter. From this point, the as-deposited characteristics will be referred to as D0, and the characteristics obtained after annealing at 450°C and 650°C will be referred to as D450 and D650 respectively. As can be seen in Fig-4.5, annealing at 450°C had no significant impact on the I-V characteristics, whereas a 650°C anneal dramatically improved the slope of the I-V curve. The ideality factor n and zero bias barrier height φ_{bo} obtained by fitting the linear part of the forward I-V characteristics are shown in Table 4.1. The 450°C anneal improved the ideality factor only slightly (from 2.14 for as-deposited to 1.78 after the 450°C anneal), whereas the 650°C anneal resulted a dramatic improvement in the diode characteristics and rendered near-ideal (n = 1.08),

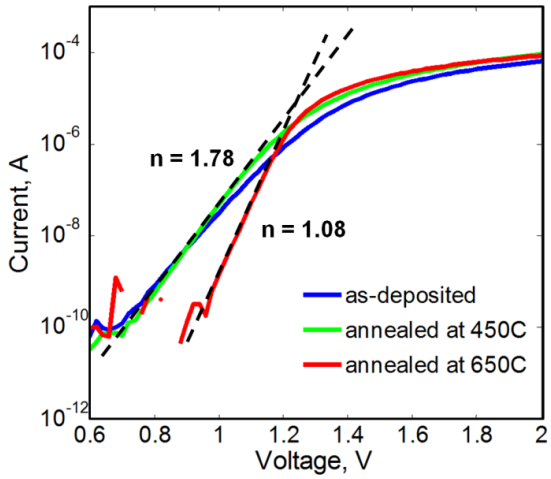

Figure 4.5 Effect of post-deposition annealing on forward I-V characteristics of a Schottky diode. The diode was fabricated on a 20 μm thick epilayer with n-doping density of $1x10^{15}cm^{-3}$. The I-V slopes are shown for D450 ($450^{o}C$ annealed) and D650 ($650^{o}C$ annealed).

high barrier (φ_{bo} = 1.65 eV) Schottky contact.

As stated earlier, annealing the Ni/SiC schottky junction improves the ideality of the thermionic emission characteristics. The improvement in ideality with annealing is often attributed to the formation of nickel silicide at the Ni/SiC interface. As shown by Roccaforte et al. [81], the Schottky characteristics obtained for the as-deposited contacts (Ni/SiC) were strongly dependent on the surface treatment prior to device fabrication, while the annealed (Nickel-silicide/SiC) contact characteristics were process-independent. This result infers that the surface defects and/or impurities introduced during the fabrication process may lead to the non-ideal behavior of the as-deposited contact. When the contact is annealed, Ni diffuses into the epilayer and reacts with the Si atoms, moving the metal/semiconductor interface beneath the epilayer surface, reducing the influence of surface impurities. The silicide formation is accompanied by precipitation of carbon at the Schottky interface. However, after annealing at

Table 4.1 Effect of annealing: Ideality factor and barrier height values obtained from linear fit of forward I-V curves.

Annealing temperature (^oC)	Ideality factor (n)	Zero-bias barrier height Φ_{bo} (eV)
As-deposited (D0)	2.14	1.12
450 (D450)	1.78	1.20
650 (D650)	1.08	1.65

temperatures < 900^{o}C does not show any significant degradation of the Schottky behavior. It can be assumed that the high solubility of carbon in Ni helps the carbon to diffuse away from the surface. In the case of high temperature annealing (> 900^{o}C) an abrupt Schottky to ohmic transition of the junction, especially in highly doped SiC. It is assumed that at this point, the carbon precipitation exceeds the solubility limit and accumulates at the junction. Some argue that the annealing leads to the graphitization of the interface, which forms a high leakage, low (< 1eV) barrier Schottky junction with the SiC layer underneath. However, the bonding structure of the accumulated carbon has not been determined conclusively.

For D650, the extracted φ_{bo} value is close to the Schottky-Mott limit (~1.76 eV), which can be estimated from the difference between the work function of Ni (~5 eV) and the electron affinity of 4H-SiC (~3.24 eV) [85], as shown in the band diagram in Fig. 4.6. This result implies that the annealed contact interface is possibly free from Fermi level pinning by the interface-related electronic states. It is to be noted that, for the Ni-rich Ni-Si phases, the work function values quoted in literature are typically > 4.8 eV [86][87]. The values are very close to the Ni work function ~5.0 eV, which allows us to use the

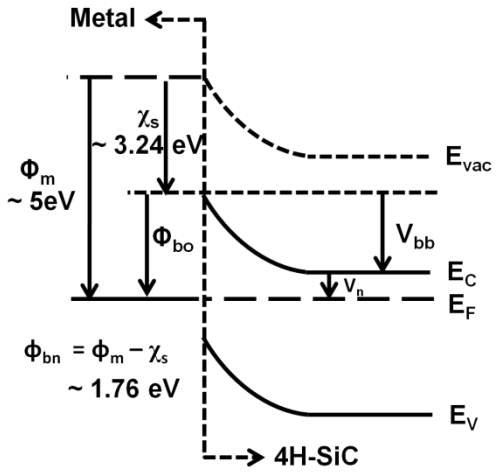

Figure 4.6 The zero bias energy band diagram for the Ni/SiC Schottky interface. The electron affinity value reported in ref. [14] was used for calculating the ideal barrier height value.

same band diagram to approximately describe the ideal barrier height for the annealed contacts too.

Fig. 4.7 shows a boxplot of the barrier heights obtained from the Schottky diodes fabricated on epilayers of different doping levels. Each box represents the distribution of barrier height values extracted from the J-V characteristics of 30 diodes of the same doping level. The mean (μ_φ) and standard deviation (σ_Φ) values are also shown next to each box (listed in Table 4.2). The spatial variation (σ_φ) of the barrier heights fell within the range of 8 – 36 mV (0.1 – 1.5% of the mean value), indicating a very 'uniform' barrier height distribution across the substrate. These data, to the best of the authors' knowledge, show the tightest distribution of Schottky parameters ever reported for Ni/SiC Schottky system.

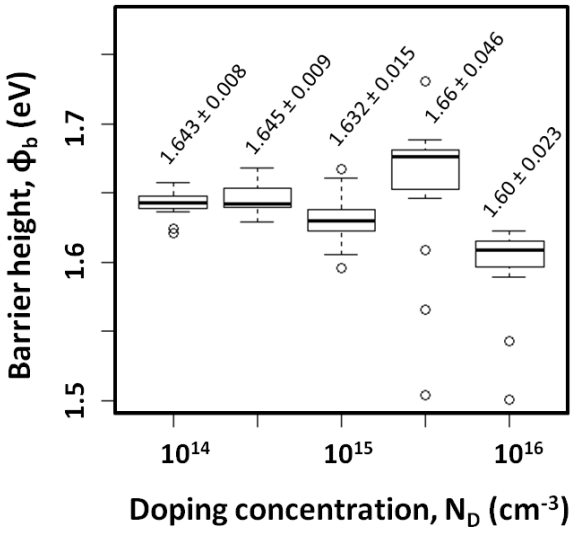

Figure 4.7 A boxplot of the Schottky barrier height vs epilayer doping concentration generated by R (v2.15.3), a statistical programming environment. > Each box represents 1st, 2nd and 3rd quartiles (Q1, Q2/median and Q3) of the barrier heights obtained from 30 diodes at the corresponding doping level. The whiskers denote the maximum values within 1.5x interquartile range (Q_3-Q_1). Outliers are shown as circles. The mean and standard deviation values are shown next to each box as $\mu \pm \sigma$.

At any given doping level, the spatial variation in both of the parameters are given in terms of the corresponding standard deviation, calculated over 21 ~ 42 Schottky 'dots' distributed across the entire substrate. The typical I-V characteristics obtained from the as-deposited and annealed Ni/4H-SiC contacts on an n-doped epilayer are shown in Fig. 4.4. The Figure shows I-V curves obtained from 21 Schottky 'dots' of three different sizes deposited on a 20 μm epitaxial layer with an n-doping density of $5x10^{14}$ cm^{-3}. All of these contacts showed highly non-ideal behavior with ideality factor n > 2, while few showed double barrier characteristics. However, apart from the double barrier diodes, the as- deposited contacts showed a tight distribution of diode parameters— ideality factor, n = 2.01 ± 0.04 and barrier height, φ_{bo} = 1.22 ± 0.09 eV. Annealing the contacts at 650°C for 120 s improved the ideality factor (n) to 1.095 ± 0.01 and the barrier height (φ_{bo})

Table 4.2 Spatial variation of Schottky barrier height, Φ_b, and ideality factor, n at various doping levels

Growth precursor	Doping N_D (cm^{-3})	Barrier height, $\Phi_b \pm \sigma_\Phi$ (eV)	Ideality factor, $n \pm \sigma_n$
TFS	1×10^{14}	1.643 ± 0.008	1.07 ± 0.007
	5×10^{14}	1.645 ± 0.009	1.095 ± 0.011
	1×10^{15}	1.632 ± 0.015	1.069 ± 0.006
DCS	1×10^{15}	1.667 ± 0.036	1.056 ± 0.034
	5×10^{15}	1.66 ± 0.046	1.059 ± 0.033
	1×10^{16}	1.60 ± 0.023	1.077±0.037

was increased to 1.645 ± 0.09 eV. Fig. 4.5b shows the I-V characteristics obtained from the same diodes after annealing. An important thing to note here is that, although the ideality factor and barrier height improved after annealing, the standard deviations of the diode parameters (n and φ_{bo}) were similar for both the as-deposited and annealed diodes. It can be inferred from the narrow distribution of the φ_{bo} values in the as- deposited contacts that the non-ideality in these diodes should be attributed to interface anomaly that is evenly distributed across the substrate (e.g., interface layer/traps etc.), and not to microscopic defects or surface impurities, which are likely to show a large scatter in their distribution.

It is interesting to note that the double barrier characteristics correlated with stacking faults flattened out upon annealing and the ideality and barrier heights improved significantly, as shown in Fig-4.8. Nevertheless, the barrier height parameters of these

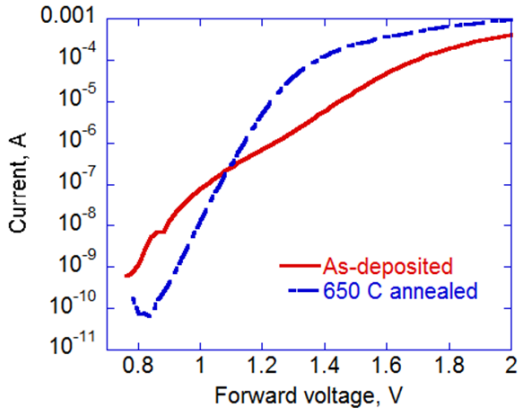

Figure 4.8 Effect of annealing on a double barrier diode.

diodes showed deviation from the regular diodes. In the boxplot shown in Fig-4.7, the outliers (open circles) correspond to these characteristics.

4.3 THE STUDY OF SCHOTTKY BARRIER INHOMOGENEITY

Non-ideal Schottky behavior is often described in terms of Schottky barrier inhomogeneity in the diode active area. It is assumed that the Schottky barrier height has a spatial variation across the interface. The total diode current is considered an aggregate of the current flowing through different regions in the interface with different barrier heights. The non-ideality in the diode characteristics arises from the low barrier regions turning on at a lower bias than the high barrier region. However, Tung et al.[24][25] and Werner et al.[28] pointed out that the small barrier regions can be in the form of patches with dimensions comparable to or less than the depletion width. In that case, these regions can be 'pinched off' by the surrounding high barrier regions at low bias, rendering a bias dependent barrier height. This additional bias dependence manifests as an additional voltage drop across the diode, leading to poorer ideality.

The Tung model, however, does not make any assumption on the nature or origin

of inhomogeneity at the Schottky interface. Rather, it defines an inhomogeneity parameter γ that encapsulates every form of non-ideality at the interface, e.g., surface roughness, grain boundaries, interface phases (i.e., silicides) etc. The conduction through each of the patches of the various barrier heights is, however, assumed to follow ideal thermionic emission behavior. Tung argues that almost all types of non-idealities in the I-V characteristics of 'real' Schottky diodes, including poor ideality and temperature effects, can be modeled by his analytical theory. However, Im at el. [88] experimentally showed that Tung's model works well only for diodes with near-ideal characteristics (n ~ 1.06), while it fails to model the I-V characteristics that widely deviate from the ideal thermionic emission behavior (double barrier, n ~ 1.5). In those cases, Tung's model obtained unphysical fitting parameters, which indicated that the possible source of inhomogeneity in those diodes was possibly extrinsic in nature, e.g. crystallographic defects and/or impurities introduced during surface preparation. Other groups have also attempted to fit the I-V characteristics and/or quantify the level of barrier inhomogeneity at various metal/SiC Schottky interfaces using Tung's model. However, in most of the studies, the bias-dependent local barrier height parameters in Tung's model are misunderstood for the overall diode barrier height, leading to an incorrect estimation of the γ parameter [89][90]. We discuss these issues in the following section and determine the limit of applicability of Tung's model.

4.3.1 Tung's model of Schottky barrier inhomogeneity

In Tung's model, the Schottky interface is described as a uniform 'high barrier' region with patches of lower barrier height embedded in it. The regions with different

barrier heights turn on at different bias voltages, leading to a deviation from ideal (n ~ 1) thermionic emission behavior. However, the low bias regions are not insensitive to the electric field in the surrounding high barrier region. The low barrier regions surrounded by higher barrier regions can undergo current pinch-off at low bias voltages. The effective barrier height of these pinched-off patches becomes a function of the applied voltage, which leads to a high ideality factor.

Tung's model describes the inhomogeneous barrier height distribution over the diode area in terms of a bias and temperature independent, inhomogeneity parameter, γ, which is intrinsic to the Schottky interface. In the microscopic level, γ is defined as —

$$\gamma = 3(\frac{\Delta R_o^2}{4})^{1/3} \tag{4.1}$$

Equation (4.1) assumes low barrier patches embedded in an otherwise high barrier (Φ_b^o) Schottky interface. The shape of the patch is circular with a radius of R_o and the barrier height of the patch is given as ($\Phi_b^o - \Delta$). As can be inferred from the equation, a high γ value indicates a 'deeper' (in terms of energy) and/or larger low barrier patch, leading to a higher degree of inhomogeneity.

The current through a single low barrier patch is given as—

$$I_{patch}(\gamma) = A^* A_{patch} \exp(-\beta\varphi_{eff}) \exp(\beta V_a - 1) \tag{4.2}$$

Here, A_{patch} is the effective area of current conduction for the patches and is given by $A_{patch} = \frac{4\pi\gamma\eta^{2/3}}{9\beta V_{bb}^{2/3}}$ and the effective barrier height of the patch is expressed as—

$$\varphi_{eff} = \varphi_{bulk} - \frac{\gamma V_{bb}^{1/3}}{\eta^{1/3}} \qquad (4.2a)$$

Assuming a sharp distribution of γ, (i.e. a single value of γ for all patches, rather than a distribution), for a patch density of c_1, the aggregate of the current flowing through individual patches is given by—

$$\Sigma I_{patch} = c_1 A I_{patch} \qquad (4.2b)$$

In the equations above, A is the total diode area, V_{bb} is the band bending under bias V_a, η is a constant equal to $2\varepsilon_s/qN_d$. It is to be noted that the effective barrier height for the low barrier patches, φ_{eff} given by (4.2a) is often inappropriately attributed to the diode as a whole and/or assumed equal to experimentally determined φ_{bo} values, whereas in reality, this parameter applies exclusively to the low barrier regions in the interface, and is a function of applied bias. The bias-dependent barrier lowering term in (4.2a), $\frac{\gamma V_{bb}^{1/3}}{\eta^{1/3}}$, will be referred to as δ in the subsequent analysis.

Assuming c_1 to be the low barrier patch concentration (with respect to total area A), the current through the 'high barrier' bulk region of the diode area (I_{bulk}) is given by the thermionic emission equation,

$$I_{bulk} = A(1 - c_1 A_{patch}) A^* T^2 \exp(-\beta\varphi_{bulk}) \exp(\beta V_a - 1) \qquad (4.3)$$

The total current through the diode is estimated as an aggregate of the low barrier patch current (I_{patch}) and the current through the uniform 'bulk' region (I_{bulk}) with barrier height φ_{bulk},

$$I_{tot} = \Sigma I_{patch} + I_{bulk} \tag{4.4}$$

The full expression is given by—

$$I_{tot} = AA^{*}T^{2} \exp(-\beta\varphi_{bulk}) \exp(\beta V_a - 1)[1 + \frac{4c_1\pi\eta^{2/3}\gamma}{9\beta V_{bb}^{2/3}} \exp(\frac{\beta\gamma V_{bb}^{1/3}}{\eta^{1/3}})] \tag{4.4a}$$

Fig. 4.9 shows the theoretical fits to the experimental I-V curves D450 and D650 previously shown in Fig. 4.2, using (4.4a). The fitting parameters are given in Table 4.3. For the D650 characteristics, a bulk barrier height of 1.75 eV and a homogeneity parameter $\gamma = 7 \times 10^{-4}$ $cm^{1/3}V^{2/3}$ provided the best fit. It can be noticed from the Figure that the current through the low barrier patches dominate the conduction at low bias (upto about Va = 1V), whereas the bulk current gradually catches up and dominates the conduction at high bias. Because of this general trend, in the literature, while modeling the I-V characteristics of near-ideal diodes, the bulk current term (I_{bulk}) is often ignored. Rather, the low barrier patches are assumed to carry the major portion of the total diode current $I_{total} \approx \sum I_{patch}$, and the patch barrier height is used as the overall barrier height ($\varphi_{eff} \approx \varphi_{bo}$) for calculating the ideality factor and/or the inhomogeneity parameter, γ. However, as shown, in Fig. 4.9b, a complete fit of the I-V characteristics (accounting for both I_{patch} and I_{bulk}) reveals that I_{bulk} cannot be ignored in these calculations, especially at high bias levels. Another interesting thing to note is that the bulk barrier height φ_b^{o} extracted from the fit is close to the theoretical Schottky-Mott limit of 1.76 eV (Fig. 4.6).

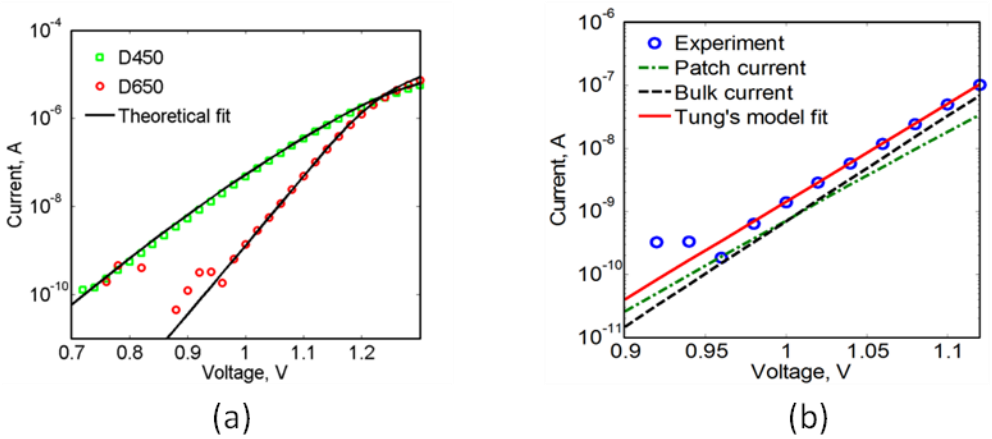

Figure 4.9 a) Theoretical fits (black solid lines) to the I-V characteristics D450 and D650 from Fig. 3 using Tung's model (equation 4.4a). The fitting parameters are shown in table-4.2. (b) A blown up view of the fit to the 650^{o}C annealed diode I-V characteristics and the corresponding theoretical fit. The patch current (dash-dotted green) and bulk current (dashed black) contributions are also shown.

This correspondence may have two implications— (i) the interface is free from interface states, i.e., no Fermi pinning or (ii) The Fermi level coincides with the charge neutrality level. In either case, the interface states will not affect the Schottky characteristics, which is a desirable characteristic.

The D0 (as-deposited) and D450 (450^{o}C annealed) I-V curves, were also fitted using (4.4a). In these fits, however, the patch current was the dominant component of the

Table 4.3 Schottky barrier characteristics extracted using Tung's Model

Annealing temperature (^{o}C)	Bulk barrier height φ_{bulk}, eV	Inhomogeneity parameter γ, $V^{1/3}cm^{2/3}$	Low barrier patch density (c_1), cm^{-2}
As-deposited (D0)	1.75	2.55×10^{-3}	3.48×10^{-5} (unphysical)
450 (D450)	1.75	2.15×10^{-3}	1.5×10^{-3} (unphysical)
650 (D650)	1.75	7×10^{-4}	2.49×10^{5}

total diode current up to bias levels as high as ~1.2 V. Only the fit to D450 is shown in Fig. 4.9a as the representative non-ideal characteristics. However, the fitting parameters obtained for both D0 and D450 are listed in Table 4.3. It was assumed that the bulk barrier heights (φ_{bulk}) were comparable at all stages of annealing, so we can still use $\Phi_{bo} \approx 1.75$ eV. However, the best fits to D0 and D450 using $\varphi_{bulk} \approx 1.75$ eV were obtained using c_1 values that were unphysically small (Table 4.3), as the minimum possible value of c_1 is 2.01×10^3 cm^{-2} (one patch per diode area). On the other hand, if we fix the c_1 value at its minimum, the closest (but not the best) fits required unphysically large φ_{bulk} values (~2.8 eV). These results indicate that the Tung's model is not adequate for modeling the highly non-ideal characteristics D0 and D450. For these diodes, Tung's model overestimates the current through the individual patches, which leads to unphysically small (less than one per diode) patch density. The overestimation of patch current density follows from the very high level of barrier inhomogeneity required to fit the experimental data. As will be discussed in the subsequent section, this high level of inhomogeneity goes beyond the scope of Tung's model which works with small perturbation to the bulk barrier potential. The question that follows is, "What is the highest degree of non-ideality that can be modeled using Tung's model?"

As seen in Table 4.3, the "good" close-to-ideal diodes are very well described using Tung's model. However, diodes with a large degree of non-ideality i.e. "bad" diodes are not effectively described by this model, as was demonstrated above. While good fits can be obtained if the variables in the model are unconstrained, the values of these parameters can be highly unphysical. Therefore, we will show below that using Tung's model, idealities $n > 1.21$ cannot be described with physically meaningful

parameters, setting a critical bound for the description of non-ideal Schottky diodes in any material system.

4.3.2 Applicability limit of Tung's model

As the patch current dominates in high γ, non-ideal diode I-V, the ideality of the patch current will give an approximate value for the overall ideality factor, which is given from (4.2) as—

$$n \approx \beta[\frac{\delta I_{patch}}{\delta V_a}]^{-1} = 1 + \frac{\gamma}{3\eta^{1/3}V_{bb}^{2/3}} \tag{4.5}$$

Here, the ideality is dependent on voltage, as V_{bb}, the amount of band bending, is a voltage dependent term. Therefore, if we want to ascribe a single ideality value to a diode over a large voltage range, as is done experimentally (e.g., Fig. 4.5), then the value of γ must be small, giving a second term in the RHS of (4.5) that is also small compared to unity so that a single ideality value is a reasonable approximation over the entire range of measurement. Otherwise, the model fails to describe the experimental ideality which is a single value extracted from the linear region of the I-V curve, which typically spans a measurement range of a few hundred mVs. The barrier lowering within a patch with respect to the surrounding high barrier Φ_b^o at a given bias is given by $\delta = \frac{\gamma V_{bb}^{1/3}}{\eta^{1/3}}$, i.e., $\varphi_{eff} = \varphi_{bulk} - \delta$ from (2a). If γ is small, then in (2a), δ must be small compared to φ_{bulk} in order for a single ideality factor to describe the entire voltage range of measurement. It is to be noted that δ is a bias-dependent parameter and is maximum at zero bias. In the discussion that follows, we will denote the zero-bias δ as δ_o.

Now, if we define a generously conservative limit of $\delta_o = 0.5\varphi_{bulk}$, the corresponding γ (the critical value, γ_{crit}) that can be described by Tung's model turns out to be ~2.1 x 10^{-3} $V^{1/3}cm^{2/3}$ for a bulk barrier height φ_{bulk} = 1.75eV. Using this value, from (4.5), we can determine the maximum possible patch ideality to be 1.42. In other words, Tung's model can be used to model only I-V characteristics with patch ideality $n \leq 1.42$ (at $V_a \sim 1V$). The overall ideality of the entire current (equation 4a) will be only slightly smaller, as I_{bulk} has ideality 1 by definition. The method to determine these limits more rigorously will be demonstrated in the numerical exercise below, where we see that in fact, the real limit on ideality in Tung's model is even less than n = 1.42. It is, however, interesting to note that this upper limit of n = 1.42 is applicable to inhomogeneous Schottky interfaces irrespective of the material system. The barrier lowering δ is a function of φ_{bulk}, as $\delta = \frac{\gamma V_{bb}^{1/3}}{\eta^{1/3}}$ and V_{bb} is φ_{bulk}-V_n (refer to the band diagram in Fig-4.6). The only material sensitive parameter in this dependence is η, a function of material dielectric constant ε, the value of which is of the same order of magnitude for the most common semiconductor materials.

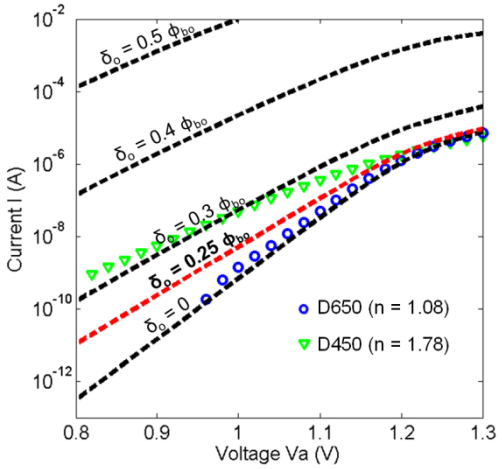

Figure 4.10 Diode current at various δ_o/ φ_{bulk} ratios. D450 and D650 are placed alongside for reference. The curve denoted by $\delta_o = 0$ curve shows the ideal thermionic emission characteristics (n = 1).

At sufficiently high forward bias voltage V_a, both low barrier patches and high barrier bulk regions of the diode are turned on. At this point the diode should conduct similar current levels irrespective of the degree of Schottky barrier inhomogeneity. Therefore, we can use this bias level as a reference point, where the total diode current for all degrees of inhomogeneity (i.e., irrespective of the γ value) become comparable to each other. As can be seen from Fig. 4.5, the current in the non-ideal D0 and D450 approach D650 at approximately $V_a \sim 1.2$ V. Therefore, based on the experimental data, the γ_{crit} (maximum level of inhomogeneity that can be modeled by Tung's model) can be estimated as the γ value for which I_{total} calculated from (4.4a), is comparable to the measured current at $V_a \approx 1.2$ V with a single low barrier patch (e.g., the lower limit of patch density c_1) in the diode area. Fig. 4.10 shows a family of I-V curves plotted using various $\delta_o < 0.5\varphi_{bulk}$, $\varphi_{bulk} = 1.75$ eV and $c_1 = 2.01 \times 10^3$ cm^{-2}, corresponding to a single patch in each diode. The closest match was obtained for $\delta_o = 0.25\Phi_{bulk}$, from which we can estimate $\gamma_{crit} = 1.1 \times 10^{-3}$ $V^{1/3}cm^{2/3}$ and the corresponding ideality factor $n_{max} = 1.21$

(from equation 4.5, at $V_a \sim 1V$). In the present study, only the D650 characteristics shows an ideality smaller than 1.21. The other two I-V curves show much higher n values (Table 4.1), and thereby cannot be modeled meaningfully within Tung's theoretical framework. These results show that the microscopic barrier inhomogeneity at the Schottky interface can produce a worst case ideality factor of no more than 1.21. Therefore, if experimentally, values of $n > 1.21$ are obtained, as in the case of D0 and D450, we can conclude that the Schottky barrier inhomogeneity is not alone responsible for the poor ideality. For explaining this type of highly non-ideal behavior ($n > 1.21$), other extrinsic reasons (such as interface traps, morphological defects, extrinsic impurities etc.) need to be considered, as also pointed out by Im et al.

4.4 THE STUDY OF INTERFACE STATES: I-V AND C-V HYSTERESIS

In the last section, it was shown that the highly non-ideal as-deposited diode characteristics could not be modeled within the theoretical framework of Tung's model. Rather, it was shown that Tung's model was not appropriate for characteristics with $n > 1.2$. Therefore, the Schottky barrier inhomogeneity cannot account for this type of non-ideal characteristics. As was stated in the section 4.4.1, in spite of the non-ideal characteristics, the as-deposited diodes showed a tight distribution of diode parameters. This rules out the possibility of the non-ideality coming from morphological defects, which have rather sporadic spatial distributions.

Next, we discuss the experimental observation of hysteresis in the I-V and C-V characteristics, which provides valuable insight into the origin of the non-ideality.

4.4.1 I-V Hysteresis

For the analysis of current hysteresis, a single staircase voltage ramp was used. The voltage was changed by 0.02 V steps and the duration of each step was 0.1 s. In the forward sweep, the forward bias was increased from 0 V to 2V. In the backward sweep, the sweep started at 2V, and was gradually decreased to 0V.

As shown in Fig-4.11a & b, the non-ideal diodes showed better (lower) ideality factor in the backward sweep. The ideal diodes (after annealing at > 650^{o}C), however, did not show any hysteresis (Fig-4.11c & d). Table-4.4 lists the n and Φ_{bo} values for the forward and reverse sweep of each diode.

Table 4.4 Hysteresis in the diode I-V characteristics

Annealing	Ideality factor, n		Φ_{IV} (eV)	
Temp., ^{o}C	Forward	backward	Forward	Backward
As-deposited	2.02	1.51	1.18	1.40
450	1.57	1.39	1.31	1.41
650	1.08	1.08	1.63	1.63
800	1.08	1.08	1.66	1.66

The improvement in diode imply that the Schottky interface shows a more ideal behavior if the junction is pre-stressed, and conducts current prior to the sweep. This behavior can be explained by considering the presence of positively charged majority carrier capture centers or traps at the interface. These interface states may be associated with interface dangling bonds that act as recombination centers for the electrons thermionically emitted from the SiC side of the junction.

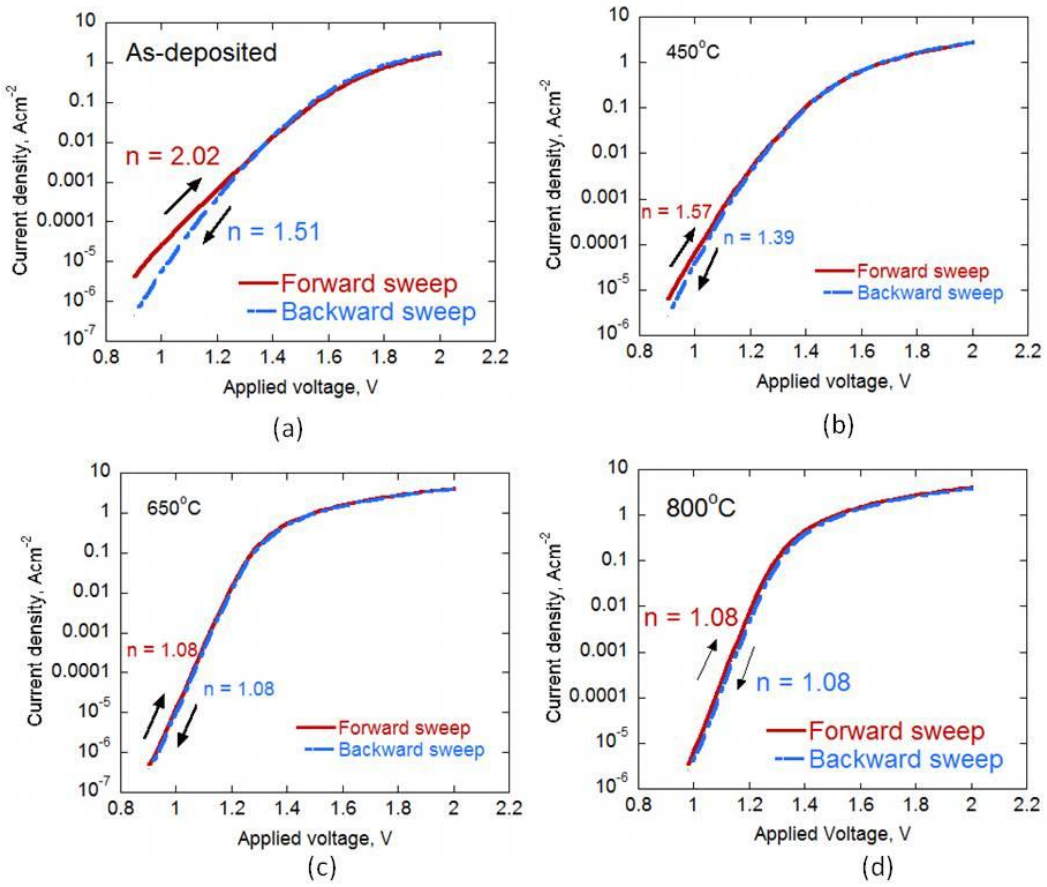

Figure 4.11 The I-V characteristics obtained under forward and backward voltage sweeps for (a) as-deposited, (b) 450°C annealed, (c) 650°C annealed, and (d) 800°C annealed diodes. The as-deposited and 450°C annealed diodes show I-V hysteresis, while the diodes annealed at higher temperatures (c & d) do not show this effect.

Fig-4.12 shows the electrostatic charge distribution and electric fields at the Schottky junction with and without the presence of traps. In the presence of traps at the interface, the charge balance can be written as—

$$Q_m = Q_t + Q_{SC} \tag{4.6}$$

Here, Q_m is the mirror charge on the metal side of the interface, $Q_t = qN_t$ is the trap sheet charge, where N_t is the trap density, and $Q_{SC} = qN_DW_D$ is the space charge in the

bulk of the semiconductor, where N_D is the doping and W_D is the width of the space-charge region.

The presence of the positively charged traps at the interface partially shields the electric field at the interface created by the Fermi-level mismatch between the metal and the semiconductor. As dictated by Gauss Law, the equilibrium space charge in the semiconductor, in this case, is lower, which is manifested by a narrower space-charge region (W_D) as compared to the ideal space-charge width (W_D^o). As a consequence, the band-bending on the semiconductor side, quantified by the built-in potential (V_{bi}) is reduced. As the barrier height determined from I-V corresponds to the band-bending at zero bias ($\Phi_{bo} = V_{bi}+V_n$), it strongly reflects the reduced band-bending caused by the interface traps. During the forward sweep, these traps are gradually filled up as the current increases with increasing bias. As the traps are neutralized by majority carrier electrons, at high bias levels, the sheet charge density at the interface is reduced, and the Schottky barrier height Φ_b increases (Fig-4.12). This non-ideal effect renders a bias-dependent barrier height $\Phi_b(V)$.

During the backward sweep, however, the initial high current (at $V_a = 2V$) fills up the interface traps, at least a fraction of which remain filled up (neutralized) during the rest of the sweep (to 0 V). As a result, the backward sweep encounters a lower density of interface traps, and produces an I-V characteristics closer to the ideal. As the sweep rate is very low (typically 0.2V/s or less), it can be inferred that the traps involved in the process have very slow re-emission/generation characteristics.

It can also be noticed in Fig-4.11 that annealing at 450^{o}C reduced the hysteresis by a noticeable amount, while the higher temperature anneals completely eliminated the

hysteresis. The silicide formation upon annealing consumes the interfacial layer that contains the traps, and renders a trap-free, intimate contact interface, which is corroborated by this result.

4.4.2 C-V Hysteresis

The reverse bias C-V characteristics (f = 100 kHz) of the diodes (both ideal and

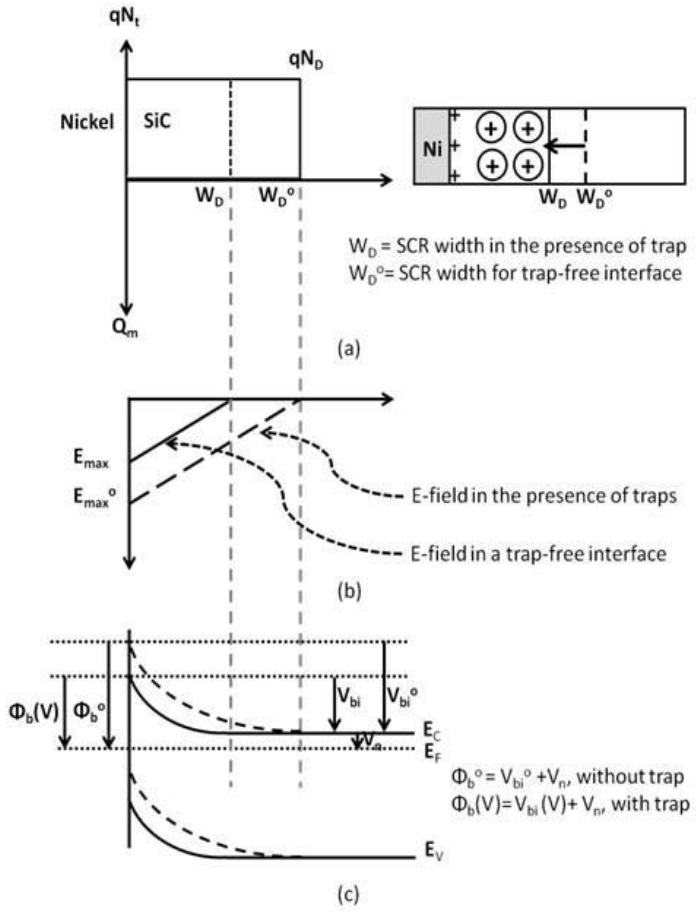

Figure 4.12 The effect of interface trap on (a) the charge distribution, (b) the electric field, and (c) the energy bands. In each case, the dotted profile shows the ideal, trap-free characteristics. In the presence of traps, the space-charge region (SCR) is narrower, the electric field in the semiconductor is lower, and so is the bending of the energy bands. The net effect is manifested as a lowering of the effective barrier height as compared to the ideal value.

non-ideal) did not show any hysteresis (Fig. 4.13), which is expected, as the diode does not conduct enough current in reverse bias to cause a significant change in the interface-trap charge density. However, as can be seen in Fig. 4.13, under forward bias, hysteresis was observed in the C-V characteristics of the non-ideal diodes (as-deposited and 450°C annealed). The C-V curve in the forward sweep showed a non-ideal hump at low dc bias, which disappeared at higher bias levels. During the forward sweep, the traps are

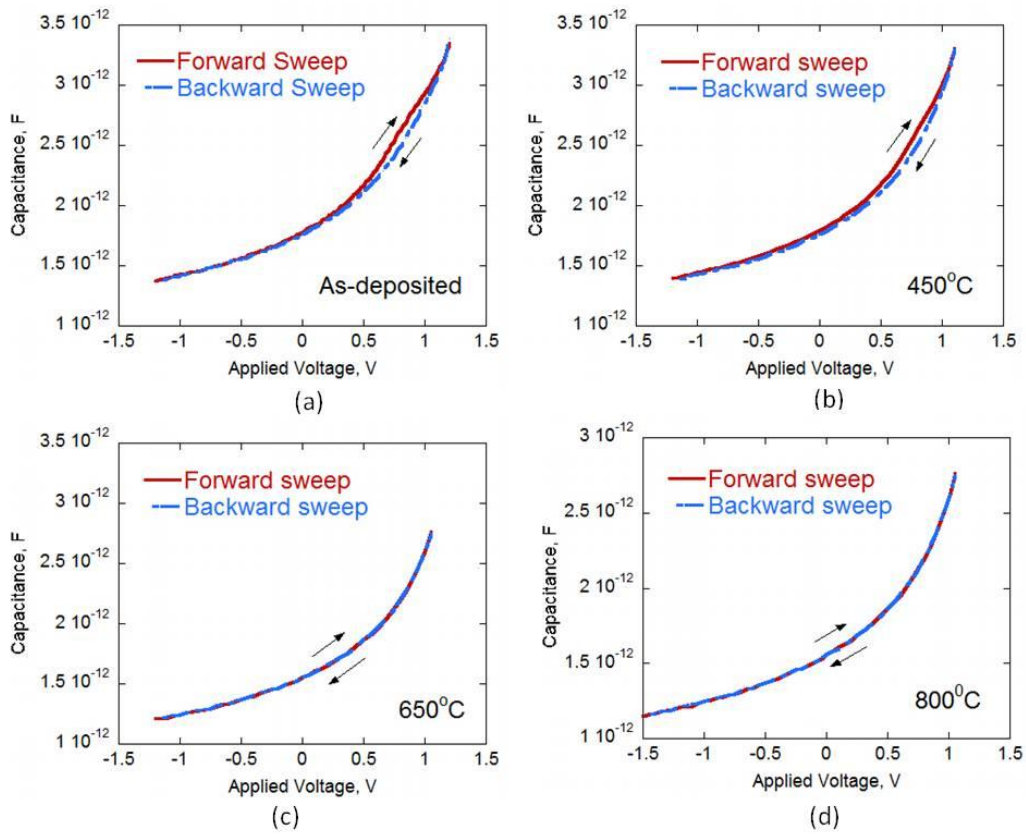

Figure 4.13 The C-V characteristics obtained under forward and backward voltage sweeps for (a) as-deposited, (b) 450°C annealed, (c) 650°C annealed, and (d) 800°C annealed diodes. The as-deposited and 450°C annealed diodes show C-V hysteresis, while the diodes annealed at higher temperatures (c & d) do not show this effect.

gradually neutralized as the bias is increased. As discussed in the previous section, the diode space charge width responds to the varying trap charge as well as the applied field. The trap-induced lowering in the space charge width (depicted in Fig-4.12) causes an increase of the diode capacitance from its ideal value, causing the hump in the forward sweep C-V characteristics. In the backward sweep, at least a fraction of the traps are neutralized, resulting in a more typical C-V curve.

As the total interface charge is conserved, the amount of trap charge neutralized by the backward sweep can be estimated from the area of the hysteresis. For the as-deposited diode (Fig-4.13a), the trap charge is estimated at ~$8x10^{-14}$ C, which corresponds to a trap density of ~$8.8x10^{8}$ cm-2. After annealing at 450^{o}C, the trap density is slightly reduced (halved), as manifested by ana neutralized charge density of 4.3 x 10^{-14} C, corresponding to a trap density of $4.4x10^{8}$ cm^{-2}. As the backward voltage sweep also renders non-ideal I-V characteristics, the filled trap density determined by C-V represents only a fraction of the total trap density. As will be shown later, the total trap density is about an order of magnitude higher.

4.4.3 Estimation of interface state/trap density

For the estimation of the trap density, we consider the interface trapping to be the sole reason for the high non-ideality. This is not entirely true, as the barrier inhomogeneity and other effects have their fair share in the non-ideal characteristics. However, this assumption can provide an upper bound of the interface state density.

To quantify the barrier lowering, we need to estimate the 'untrapped' barrier height (φ_b^{o}), i.e., the ideal barrier height that could be achieved in the absence of traps. As

the trap density diminishes at high bias levels, the flat band voltage (V_{FB}) can be used to estimate φ_b^o. The concept of the flat band voltage was discussed in detail in section 2.3, and a novel technique was

proposed. According to this technique, a plot of the junction voltage (V_D) vs the applied bias (V) is made, where—

$$V_D = V - IR_s \tag{4.7}$$

Here, I is the diode current obtained from the I-V characteristics, and R_s is the series resistance, which may be calculated from the slope of the I-V curve at high bias levels, or for more accurate estimation, from a Norde plot [92].

For determining the V_{FB} from the SiC diode characteristics, the series resistance was calculated from the slope of the I-V characteristics for $V_a > 2V$. The values were verified using the generalized Norde plot, and was found to be accurate within ±50Ω. The R_s value for each diode was used to determine the voltage drop across the space-charge region ($V_D = V_a - IR_s$). Fig-4.14 shows a plot of V_D vs V_a (the applied voltage) for each

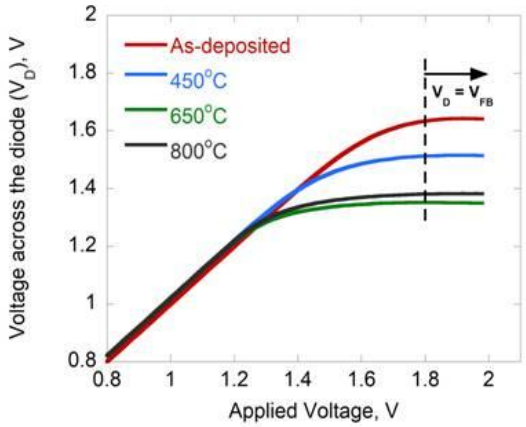

Figure 4.14 Determination of flat band voltage (V_{fb}) using an equivalent diode voltage (V_D) vs applied voltage (V_a) plot.

diode characteristic. The experimental flat-band barrier height values (φ_{bf}) calculated from this figure are listed in table 4.5.

As the deviation of the zero-bias barrier height (φ_{bo}) from the high bias or flat band barrier height (φ_{bf}) is caused by diode non-ideality, it can be expected that the φ_{bf} values will be close to φ_{IV} values for near-ideal diodes. As can be seen from the table, the proposed technique for the 650 and 800^{o}C annealed near-ideal diodes φ_{bf} becomes equal to φ_{bo}. The C-V barrier height (φ_{CV}), however, maintains a high, constant value regardless of the ideality of the junction, which warrants further investigation.

Table 4.5 Schottky barrier Parameters

Annealing Temp. ^{o}C	n	Φ_{bo}	Φ_{CV}	Φ_{bf}	R_s
As-dep	2.02	1.18	1.96	1.94	390
450	1.57	1.31	2.07	1.8	350
650	1.08	1.63	2.05	1.63	310
800	1.08	1.66	2.1	1.66	305

The charge balance at the Schottky interface is given by equation (4.6). If the interface sheet charge density qN_t is modeled with a Dirac delta function, solving the Poisson's equation, the electric field in the space charge region with and without interface traps can be respectively determined as—

$$E(x) = \frac{-qN_D}{\varepsilon}(W_D - x) \tag{4.8a}$$

$$E^o(x) = \frac{-qN_D}{\varepsilon}(W_D^o - x) \tag{4.8b}$$

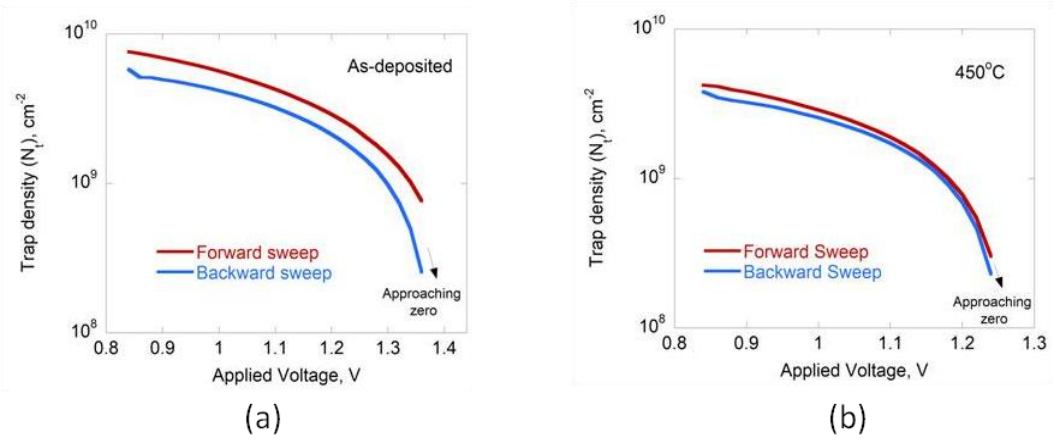

Figure 4.15 The plot of trap density N_t as a function of the applied bias, V obtained using (4.8a) and (4.8b).

Here, W_D is the space charge width with traps, and W_D^o is the same in the ideal case (without traps), as illustrated in Fig-4.15. The relation between the two widths are determined from (4.8a) and (4.8b) as—

$$W_D = W_D^o - \frac{N_t}{N_D} \tag{4.8c}$$

Again, W_D and W_D^o can be determined from the corresponding built-in potential (V_{bi}). For the ideal case (W_D^o), the flat band voltage (V_{FB}) was used for V_{bi}. W_D is, however, voltage dependent, and was determined using the voltage-dependent barrier height values $\Phi_b(V)$, as determined from the ideal thermionic emission equation for each bias level. The interface trap density N_t was then calculated using (4.8c). Fig-4.15 shows the trap density in the non-ideal diode interfaces as a function of applied voltage. In both cases, N_t decreases from 10^{10} cm^{-2} at 0.9 V to $<10^9$ cm^{-2} at higher voltages. It is to be noted that the initial trap density was reduced after the 450°C anneal, and was closer to the backward sweep (filled trap) values.

The physical origin of the traps, is however, not clear. The post-deposition surface treatments (RCA cleaning, photolithography, HF etch, back contact annealing etc.) can lead to ionic contamination on the SiC. The stoichiometry of the surface can also be altered during the back contact annealing [94]. UHV annealing of SiC surface has also been reported to cause surface reconstruction at temperatures as low as 800^{o}C [93][95], which may lead to the formation of charged surface states. Therefore, further study of surface structure and stoichiometry through the fabrication process is needed to gain insight into the nature of Schottky interface inhomogeneity in the highly non-ideal ($n > 1.21$) diodes.

4.5 CHAPTER SUMMARY

To summarize, this chapter discusses the non-ideality in the as-deposited Ni/SiC Schottky junction characteristics and the effect of annealing. It was shown that non-uniformity in a batch of diodes is caused by surface defects. Otherwise, the fabrication process can churn out Schottky junctions with reproducible characteristics.

The non-ideality of the diode characteristics was studied using Tung's model of barrier inhomogeneity. It was found that the lower measured barrier height and poor ideality factor ($n > 1.21$) in the as-deposited contact cannot be modeled by Tung's model for Schottky barrier inhomogeneity alone. Rather, extrinsic sources of non-ideality, such as interface layers and/or trap levels need to be considered. The hystereis in the I-V and C-V characteristics support the conclusion, as this type of anomaly can be modeled as the effect of interface states.

CHAPTER 5

MINORITY CARRIER INJECTION: THE GRAPHENE/P-SIC HETEROJUNCTION

The Schottky junction is generally considered a majority carrier interface. This is quite true for modern Schottky junction devices, in which noticeable minority carrier junction is rarely observed. However, as discussed in Chapter 2, in the early days of semiconductor electronics, highly efficient minority carrier injection was routinely observed, and utilized for fabricating bipolar Schottky emitters. However, there was no satisfactory theoretical understanding of the principles governing this phenomenon. Practical devices were fabricated with the qualitative understanding that the effect was more pronounced in large barrier junctions, whereas Bardeen, the inventor of the point contact transistor, argued that the surface states contributed to the minority carrier injection. The invention of the more controllable p-n junction shifted the research focus away from point contacts. The improvement of the crystal growth and surface preparation techniques might also have contributed as both the surface state density and pinning-induced high barrier formation became rarer. However, the advent of compound semiconductors with interesting surface characteristics has opened up the possibility to fabricate Schottky bipolar emitters using metal or hetero-junctions.

In this chapter the concept of minority carrier injection through the Schottky junction is re-visited in relation to the graphene/p-SiC Schottky heterojunction. A bipolar

photo-transistor structure is demonstrated that utilizes the bipolar transport capability of this heterojunction.

As the system under discussion is the graphene/p-doped SiC interface, all mathematical expressions presented in this chapter will use the notations appropriate for a Schottky interface between a metal and a p-doped semiconductor, i.e., the majority carriers are the holes, while electrons are the minority carriers. Care must be taken in interpreting this analysis, as this notation is contrary to that used in literature, which usually deals with n-Schottky interfaces where electrons are the majority carriers.

5.1 CONDITION FOR MINORITY CARRIER INJECTION

The degree of minority carrier injection in a Schottky junction is quantified by the parameter, injection ratio (γ), which is given by—

$$\gamma = \frac{J_n}{J_n + J_p} \tag{5.1}$$

Here, J_p is the hole current due to the majority carrier holes and J_n is the electron current due to the minority electrons in the QNR. This equation can also be written in terms of the ratio of J_n and J_p ($r = J_n/J_p$)--

$$\gamma = \frac{r}{r+1} \tag{5.1a}$$

In regular Schottky diodes, $J_n << J_p$, and $\gamma \sim 0$.

In a bipolar Schottky emitter, $J_p << J_n$, which renders $\gamma \sim 1$.

The first analytical expression for the injection ratio was given by Scharfetter [33]. For the derivation of γ, The electron and hole currents were written as a combination of drift and diffusion components--

$$J_p = q\mu_p pE - qD_p \frac{dp}{dx} \tag{5.2a}$$

$$J_n = q\mu_p pE - qD_p \frac{dp}{dx} \tag{5.2b}$$

The electric field is obtained as--

$$E = \frac{1}{p+n}\left(\frac{J_n}{q\mu_n} + \frac{J_p}{q\mu_p}\right) \tag{5.3}$$

Scharfetter, however, assumed a low-level injection of minority carriers ($J_n << J_p$) consistent with the conventional picture of negligible minority carrier transport through the Schottky barrier. The injection ratio in this case was given by—

$$\gamma_{J_p >> J_n} \approx r = \frac{J_n}{J_p} = \frac{D_n n_i^{\,2}}{D_p N_A^{\,2}} \frac{J_p}{J_{ps}} \tag{5.4}$$

Here, the J_n and J_p are the minority electron and majority hole currents respectively, where J_p is expressed as the thermionic emission current with J_{ps} as the zero-bias/saturation current--

$$J_p = J_{ps}\left\{\exp\left(\frac{qV}{kT}\right) - 1\right\} \tag{5.5}$$

As can be seen from equation (5.2), the minority injection increases linearly with the diode current ($J \approx J_p$). The model was experimentally validated by several groups for MS and MIS junctions using a diagnostic bipolar transistor structure with the Schottky interfaces as the emitter-base junctions [31]. These studies, however, showed γ values < 0.1 for all interfaces, and no bipolar gain was observed.

While equation (5.1) works well for the regular 'majority carrier' Schottky contacts, the approximation that $J_p >> J_n$, used in deriving (5.4) is not appropriate for a

bipolar Schottky interface. A similar analysis without assuming $J_n << J_p$ renders a minority carrier current governed by diffusion in the quasi-neutral region (QNR)--

$$J_n = \frac{\frac{2qn_i^2 D_n}{N_a L}}{1+\frac{2D_n}{LS}} \exp(\frac{qV}{kT}) \tag{5.6}$$

Here, L is the length of the quasi-neutral region and S is the recombination velocity at the back/collecting interface of the system (Fig-5.1). In the limit of $S \to 0$, the the minority carrier current (J_n) approaches 0 too. In most epitaxial diodes, the highly doped substrate acts as a reflecting boundary for the minority carriers, rendering a low surface recombination velocity and a very small J_n. In a bipolar junction transistor structure, however, the back interface is a collector junction with a non-zero S. The minority current in that case depends on the injected carrier concentration at the injector junction, denoted by n(0) as shown in Fig-5.1. Under low injection condition, n(0) is given by the law of junction--

$$n(0) = \frac{n_i^2}{N_a} e^{qV/kT} \tag{5.7}$$

In wide band gap semiconductors, such as SiC n_i is small (~10^{-8} cm^{-3}), rendering a diffusion current much lower than the experimentally observed current density. We, therefore, consider a high injection level of minority carriers.

Chuang provided an expression for the minority to majority current ratio (r) in the high injection condition ($n \approx p >> N_a$) [34]. The expression for r takes the following

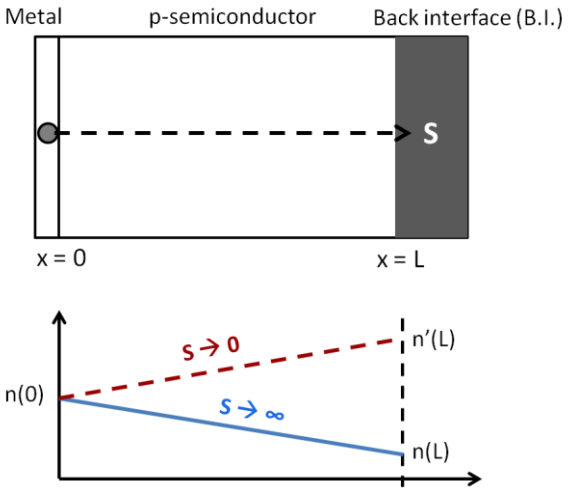

Figure 5.1 The qualitative picture of minority carrier injection.

form for a p-doped semiconductor —

$$r = \frac{\frac{D_n}{D_p} + \frac{2qD_n n_i}{L}\sqrt{\frac{1}{J_p J_{ps}}}}{1 + \frac{2D_n}{LS}} \tag{5.8}$$

In the high recombination/collection rate regime, $S \to \infty$ and the denominator of Chuang argued that under high injection condition, the majority carrier current (J_p) is large, and the second term of the numerator approaches zero. In that case, γ is solely determined by the ratio of minority carrier diffusivity to that of the majority carriers (D_n/D_p). Interestingly, in most semiconductors, the diffusivity of electrons is higher, i.e., $D_n > D_p$. Therefore, a J_n/J_p ratio greater than unity is possible only when electrons are minority carriers, i.e., in a p-type semiconductor.

Efficient bipolar emitter action at the Schottky junction, however, requires a J_n orders of magnitude higher than J_p. In that case, J_n will not be the major current component even at high overall current levels and equation (5.3) will govern the J_n/J_p

ratio in the given form. Assuming thermionic emission of the majority carriers, equation (5.3) can be written as—

$$\frac{Jn}{Jp} = \frac{\frac{D_n}{D_p} + \frac{2qD_n n_i}{A^* T^2 L} \exp(\frac{q\phi_p}{kT}) \exp(-\frac{qV}{2kT})}{1 + \frac{2D_n}{LS}} \tag{5.9}$$

Here, the symbols have their usual meanings. We denote the second term in the numerator by P(V), and notice from equation (5.4) that at moderate levels of junction voltage, P(V) can be higher than D_n/D_p. In that case, a high J_n/J_p ratio can be obtained rendering highly efficient bipolar emitter injection, with γ (as described in equation 5.1) approaching unity. Using the dependence of the intrinsic carrier concentration (n_i) on the material bandgap (E_g), equation (5.4) can be written as—

$$\frac{Jn}{Jp} = \frac{\frac{D_n}{D_p} + \frac{2qD_n \sqrt{N_c N_v}}{A^* T^2 L} \exp(\frac{\phi_p - E_g/2 - qV/2}{kT})}{1 + \frac{2D_p}{LS}} \tag{5.10}$$

Equation (5.4) gives us an upper limit of the voltage range (V_1) within which the condition $P(V) > D_n/D_p > 1$applies—

$$V_1 = 2\left\{\phi_p - \frac{E_g}{2} - \frac{kT}{q} \ln(\frac{A^* T^2 L}{2qD_p \sqrt{N_c N_v}})\right\} \tag{5.11}$$

As evident from equation (5.6), a highly efficient bipolar emitter action is possible for $V < V_1$ if the barrier height Φ_p is much larger than the midgap energy ($E_g/2$), and a high level of injection is achieved at that voltage.

5.2 GRAPHENE ON SiC

Graphene is a two dimensional allotrope of carbon with exceptional physical properties such as the linear energy dispersion and 'massless' Dirac Fermion transport, quantum hall effect, saturable optical absorption and a remarkably high mobility. These properties make graphene an attractive platform for developing novel nanoelectronic devices [96]. The electronic application of graphene requires large area sheets, which is produced by CVD on metal substrate or by the sublimation of the SiC crystal surface. High temperature (> 1300^{o}C) annealing of the SiC(0001) surface in vacuum or inert environment causes step controlled growth of few-to-monolayer graphene on the SiC substrate. The Si sublimation leaves behind non-volatile C atoms that rearrange themselves in the form of a graphene sheet. Upon annealing, the SiC surface reconstructs into a (6 $\sqrt{3}$x6 $\sqrt{3}$)R30^{o} arrangement, which acts as a growth template for the graphene growth (Fig-5.2).

The epitaxially grown graphene layer forms a Schottky type heterojunction with

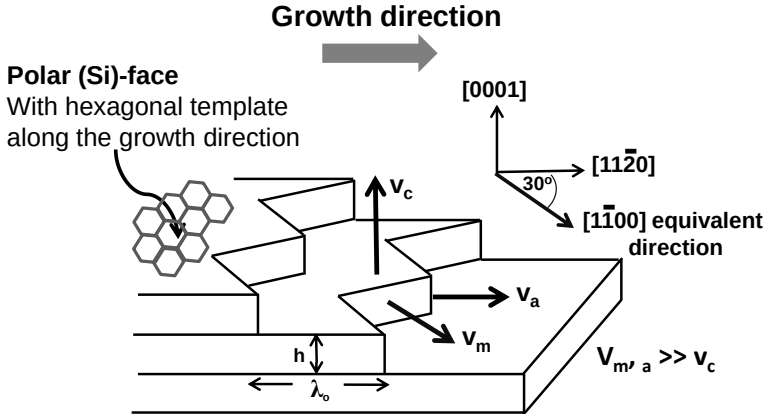

Figure 5.2 Epitaxial growth of graphene on SiC by sublimation of the (0001) surface.

the underlying SiC and show rectification properties. The epitaxial graphene (EG) film, however, does not directly sit on the SiC surface. In between the first 2D graphene layer and the SiC substrate exists a C rich buffer layer (often called the 0 layer) covalently bound with the SiC crystal. The presence of the buffer layer influences the electrical properties of the graphene layers on top of it as well as the graphene/SiC interface. The dangling bonds between the buffer layer and the SiC crystal act as donor states, and imparts a negative charge to the EG film [97].

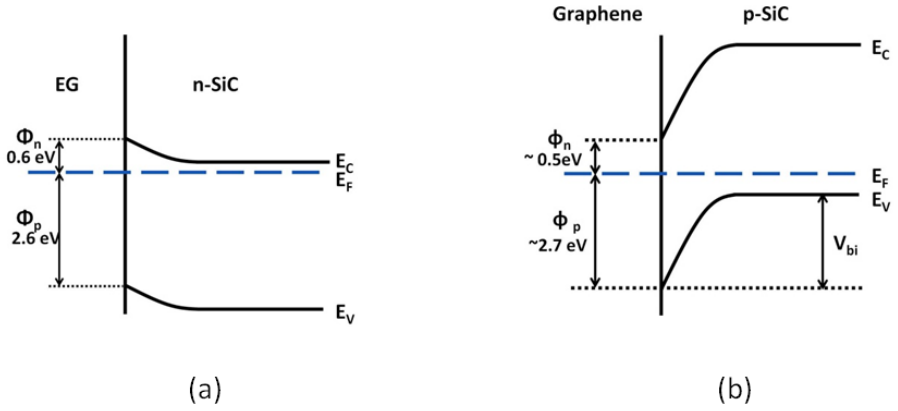

Figure 5.3 Energy band diagram of (a) graphene-nSiC and (b) graphene-p-SiC heterojunctions

This renders a low potential barrier of 0.3-1.1 eV to n-type SiC [98][99][100], but a barrier as high as 2.7 eV to p-SiC [98][101] on the SiC (0001) surface. Fig-5.3b shows the energy band diagram at the large barrier graphene/p-SiC interface. As the barrier resembles a Schottky barrier in energy characteristics, the carrier transport across the interface is expected to occur by thermionic emission of majority carriers. Graphene/n-SiC interfaces generally show near-ideal thermionic emission behavior. However, non-ideal characteristics were observed for the graphene/p-SiC junction, with ideality factor (n) values of 1.4 ~ 2 [101]. An electroluminescence study of the interface showed carrier

recombination at the heterojunction interface, indicating strong minority carrier injection across the EG/p-SiC interface.

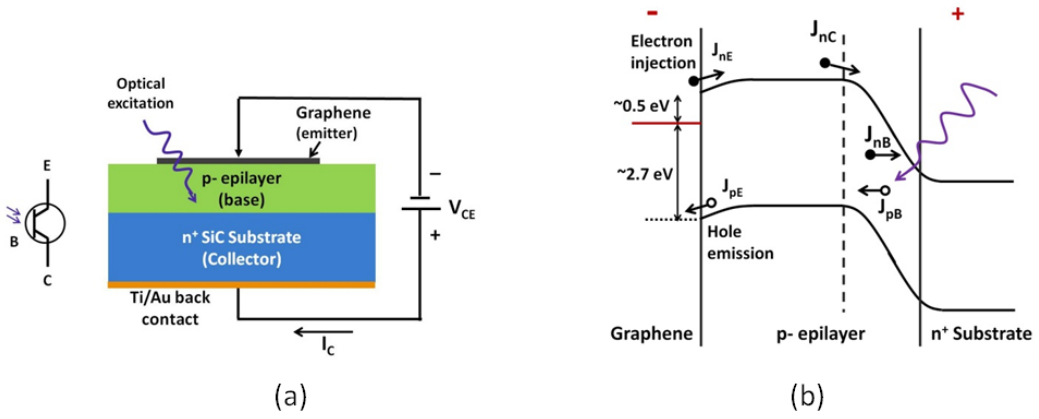

Figure 5.4 Graphene as an emitter. (a) The schematic structure of the graphene/SiC heterojunction bipolar phototransistor. (b) The energy band diagram at the two junctions of the device under collector-emitter bias. Electrons are depicted as closed circles and holes as open circles.

5.3 GRAPHENE/SIC HETEROJUNCTION BIPOLAR PHOTO-TRANSISTOR (GS-HBPT)

5.3.1 Graphene as the emitter

We study the bipolar injection efficiency of the EG/p-SiC interface using a photo-transistor structure with a graphene emitter, a p-SiC base, and an n+ SiC collector, as shown in Fig-5.4a. As mentioned earlier, a similar arrangement was also employed by Yu et al for the experimental evaluation of γ in various metal contacts to Si. The epitaxial p-SiC layer was grown by chemical vapor deposition (CVD) on a commercial n+ doped SiC (0001) substrate with an offcut angle of 4^{o}. The p-doping was achieved by maintaining a low C/Si ratio in the source gas for CVD growth. The resulting site competition epitaxy produced p-doped epilayers with carrier concentrations of ~$3x10^{14}$

cm^{-3}, as determined by mercury probe C-V. The epilayer thicknesses (i.e., the base width, W_B) was ~30 μm. The results were reproduced in a device with a 10 μm base also. The epitaxial graphene (EG) was grown by thermal sublimation of the p-SiC epilayer surface at 1350^{o}C. The presence of graphene was confirmed using the raman spectra obtained using a Horiba JY spectrometer with an excitation line of 631 nm. The D/G ratio was estimated at 0.06. Ellipsometry results showed EG thicknesses of 2-3 monolayer in similar growth conditions. The 250 μm diameter circular graphene mesa was defined using an O_2 plasma etch through a photoresist mask. A plasma sputtered Ti/Au film was used to form a large area ohmic contact on the back of the SiC substrate. The process flow is provided in Appendix-D.

For phototransistor operation, the graphene emitter was held at a negative bias with respect to the n+ SiC emitter layer by directly contacting the graphene layer with a tungsten probe. The base current was provided by optical excitation from an Omnicure S1000 Hg-vapor lamp with variable intensity. The lamp spectrum provided three sub-bandgap (for SiC) excitation lines at 312, 334 and 365 nm wavelengths. The optical power was measured using a Karl Suss i-line (365 nm) photo-detector, and the power densities in the other two lines were estimated by their relative intensities obtained from the lamp spectrum. Fig-5.5 shows the typical collector current (I_C) vs collector-emitter voltage (V_{CE}) characteristics for the graphene/SiC HBPT under different levels of illumination.

For the estimation of gain, the base photocurrent was determined by taking into consideration the generation rate from the incident photons over the base thickness as well as the absorption lengths for each of the three excitation lines (details provided in

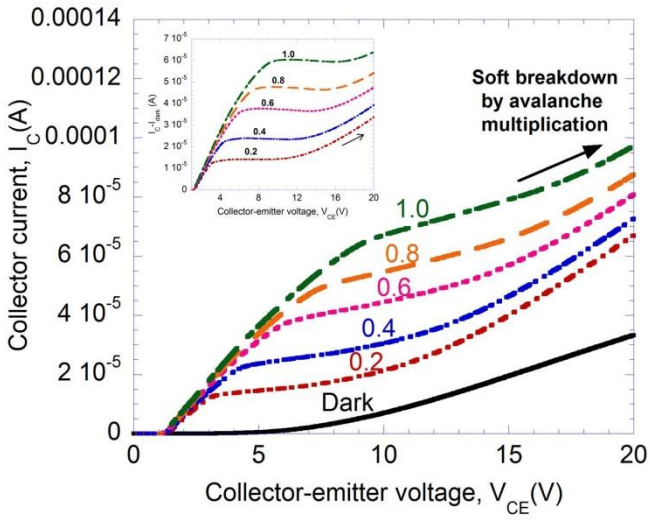

Figure 5.5 The I_C vs V_{CE} characteristics obtained under various levels of UV illumination. The numbers on the curves correspond to the relative optical power with P_{opt} = 1.0 denoting an incident power density of 3 mW/cm^2. The dark current subtracted characteristics are shown in the inset. The base width of the device was 30 μm.

Appendix-E). Nevertheless, the numbers obtained were only a rough estimate of the base current, I_B. According to the estimate, the characteristics in Fig-5.5 were obtained over one decade of base current density, ranging from 5x10^{-5} to 5x10^{-4} A/cm^2. The collector current corresponding to the photocurrent was obtained from the flat part of the dark current subtracted characteristics (inset of Fig 5.5). For the characteristics shown above, common emitter current gain values > 200 were observed. The gain showed slight decrease (from 300 at P_{opt} = 0.2 to 200 at P_{opt} = 1.0) with increasing light intensity, which is consistent with the expected increase in the recombination within the base region. It is to be noted that the in the HBPT structure under discussion, the p/n+ junction is not mesa isolated, which results in a large leakage current further enhanced by the transistor gain, as can be seen from the dark condition characteristic curve in Fig-5.4. The leakage,

however, can be reduced significantly by mesa isolation of the p/n junction, and can be minimized by forming the n+ collector layer by implantation in the p-doped epilayer.

Now, we consider the transport parameters at the EG/p-SiC junction. In p-SiC, electrons are the minority carriers, which enables a diffusivity ratio (D_n/D_p) greater than 1, as the electron and hole diffusivity in 4H-SiC are 25 and 3 cm^2/Vs respectively. Therefore, in the range $V > V_1$, J_n/J_p is expected to be ~7.4, which renders a γ of 0.88, assuming no back interface effect ($S \to \infty$). The observed β (~300), however, corresponds to an open-base current gain (α) of at least 0.996. The definition of γ used here allows us to assume a negligible base recombination and obtain the upper bound of γ to be 0.996. The device, therefore, operates in the $V < V_1$ regime, where a J_n/J_p ratio > D_n/D_p is possible. As the Schottky barrier height at the EG/p-SiC interface (~2.7 eV) is considerably larger than half of the 4H-SiC band gap (~1.6 eV), according to equation (5), this level of injection ($J_n/J_p \sim 10^2$) is theoretically possible for junction voltages < V_1 = 1.88 V in the $S \to \infty$ condition, i.e., the base current provided causes a voltage drop of < 1.88 V across the forward biased EG/p-SiC junction.

However, the majority carrier current obtained in this condition is found to be several orders of magnitude lower than the experimental current value. Looking back at equation (5.8), the minority carrier current, J_n can be written as--

$$J_n = \frac{\frac{D_n}{D_p} J_p + \frac{2qD_n}{L} n(0)}{1 + \frac{2D_n}{LS}} \tag{5.12}$$

For evaluating n(0) Chuang used the law of junction under high injection, which yielded--

$$n(0) = n_i e^{qV/2kT} \tag{5.13}$$

It is to be noted that the high injection condition is a highly non-equilibrium situation, for which the assumption of quasi-neutrality may render inaccurate results. Since the n_i of SiC is very low, the high injection condition requires a bias level as high as 2.7 V. While this is achievable in p-n junctions, the 2.7 eV barrier at the EG/p-SiC junction, which reaches the flat-band condition at < 2.45 eV, does not allow for such high voltage across the SCR. We argue that the high injection condition is reached at a bias level lower than the flat-band voltage, and the n(0) does not follow equation (5.13).

If we replace n(0) in equation (5.13) with the epilayer doping concentration N_a, which can be thought of as the onset of high injection, using a J_n equal to our experimental base current (~10^{-5} A/cm^2) and S $\rightarrow \infty$ we get a minority carrier current of 0.745 Acm^{-2}. Although this value is about an order of magnitude higher than the experimental collector current, this result shows that a the experimental current level can be achieved with minority carrier injection from the graphene emitter.

5.3.2 Graphene as a collector

The EG/p-SiC junction forms a Schottky barrier nearly as large as the SiC p-n junction barrier (~3 V). Therefore, the EG/p-SiC junction should be capable of serving as a collector too. Fig-5.6 (a) shows the biasing scheme for graphene collector operation, while the p-n+ junction forms the emitter-base junction. However, this configuration did

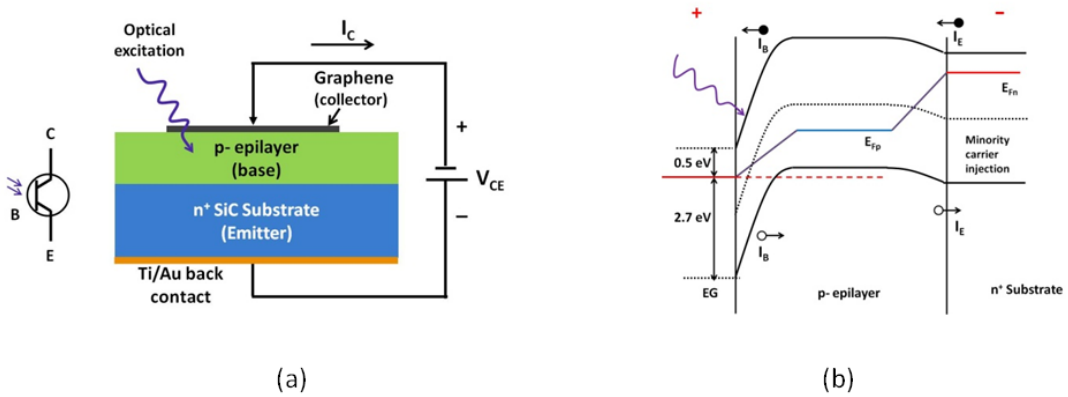

Figure 5.6 Graphene as a collector (a) The the biasing scheme, and (b) the band diagram.

not show any bipolar gain for the majority of the devices characterized in this study. Rather, the devices behaved like an MSM photo-detector, with two back to back junctions (Fig-5.6b). The I-V characteristics are shown in Fig-5.7, where (a) represents the I-V characteristics of the majority of the devices, while (b) was observed in a handful of randomly located devices. The gain values obtained from these devices were of the

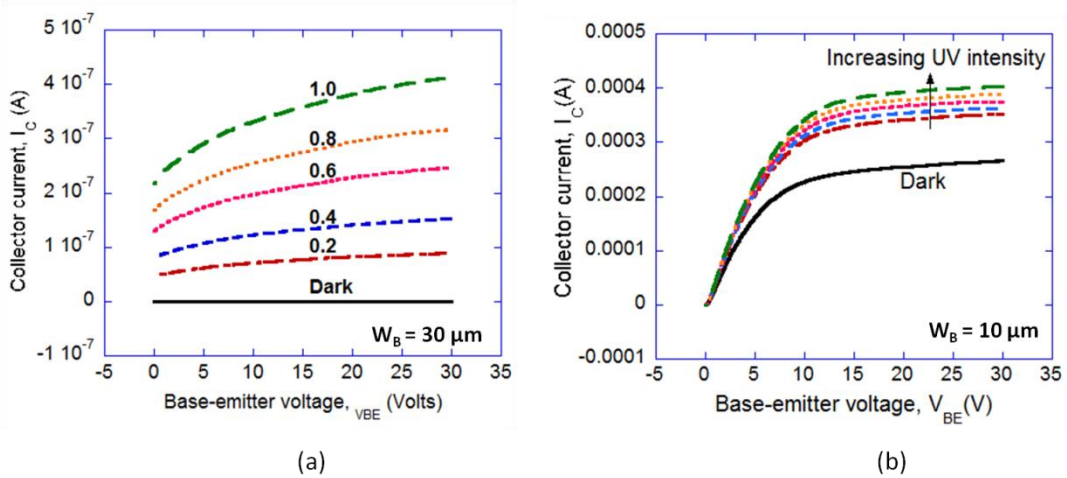

Figure 5.7 I_C vs VCE characteristics in the graphene collector mode. (a) the no-gain characteristics observed in the majority of the devices and (b) the BJT characteristics observed in few of the diodes. UV intensities are different in (a) and (b).

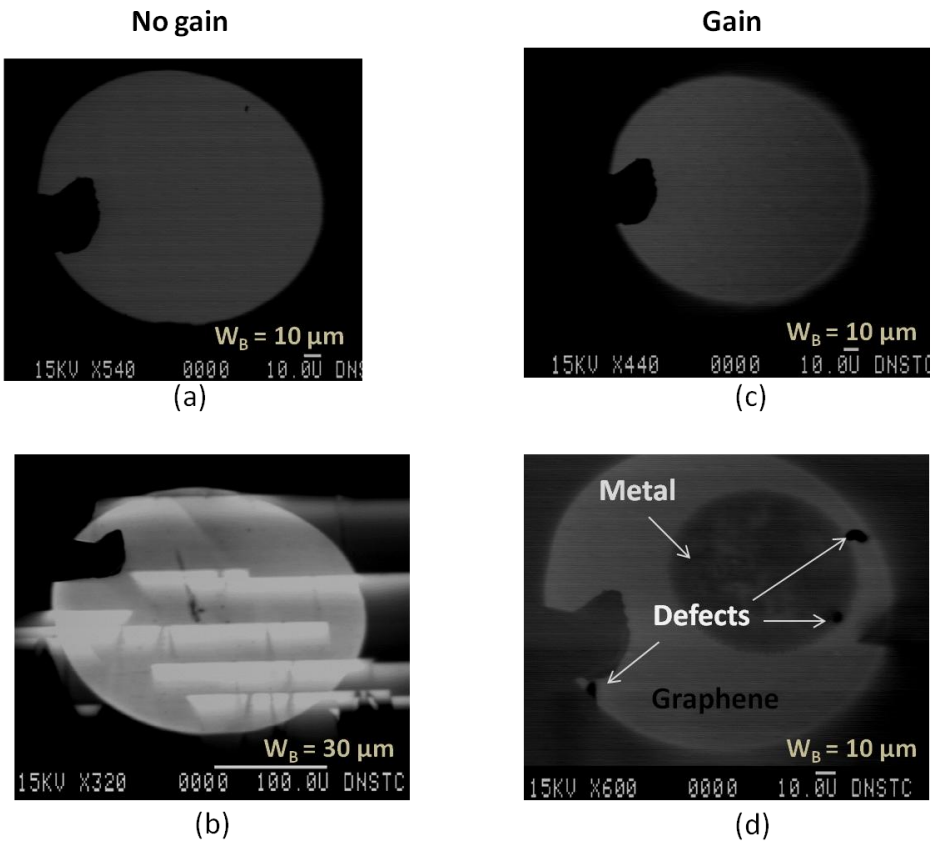

Figure 5.8 The EBIC images obtained from the HBPT devices. (a) No gain device with no electrically active defect at the heterojunction interface (b) No gain device with large density of stacking faults (c) A device with gain, but no EBIC feature (d) A device with gain with unknown interface defects.

same order as that in the common emitter configuration ($10^2 \sim 10^3$).

The devices were characterized by electron beam induced current (EBIC) for studying the the EG/p-SiC collector interface. The typical EBIC images obtained from the devices with and without bipolar gain are shown in Fig-5.8. No apparent correlation was found between the EBIC features associated with defects at the EG/SiC junction and the bipolar gain.

A possible explanation for the lack of gain in the majority of the devices is a high level of base recombination near the forward biased epilayer-substrate junction,

which is a large area junction with a large density of surface defects. The devices with gain are possibly located over a relatively low-defect patch of the back interface, enabling efficient minority carrier injection into the base. This limitation, however, can be overcome by epitaxially forming the emitter-base junction, or by forming a true graphene-SiC-graphene bipolar MSM structure.

5.3.3 The graphene advantage

The most important metric in a photo-transistor operation is the responsivity, defined as the ratio of the device current over the optical power of the excitation. As an added advantage of using a universally transparent EG layer as the emitter, a zero-bias responsivity of ~0.1 A/W is observed, compared to ~10^{-4} A/W for SiC p-n diodes and MSM devices at comparable wavelengths [102][103]. In the Schottky emitter mode, as the device bias was increased, and bipolar gain was achieved, responsivity values of > 30 were achieved. In the Schottky collector or MSM mode, the responsivity stays close to the zero bias value (0.16 A/W).

5.4 PHOTORESPONSE TO VISIBLE LIGHT

As the SiC polytype is 4H with a band gap of 3.23 eV (corresponing to ~385 nm), it is expected that the EG/SiC HBPT shows no response to an electromagnetic excitation

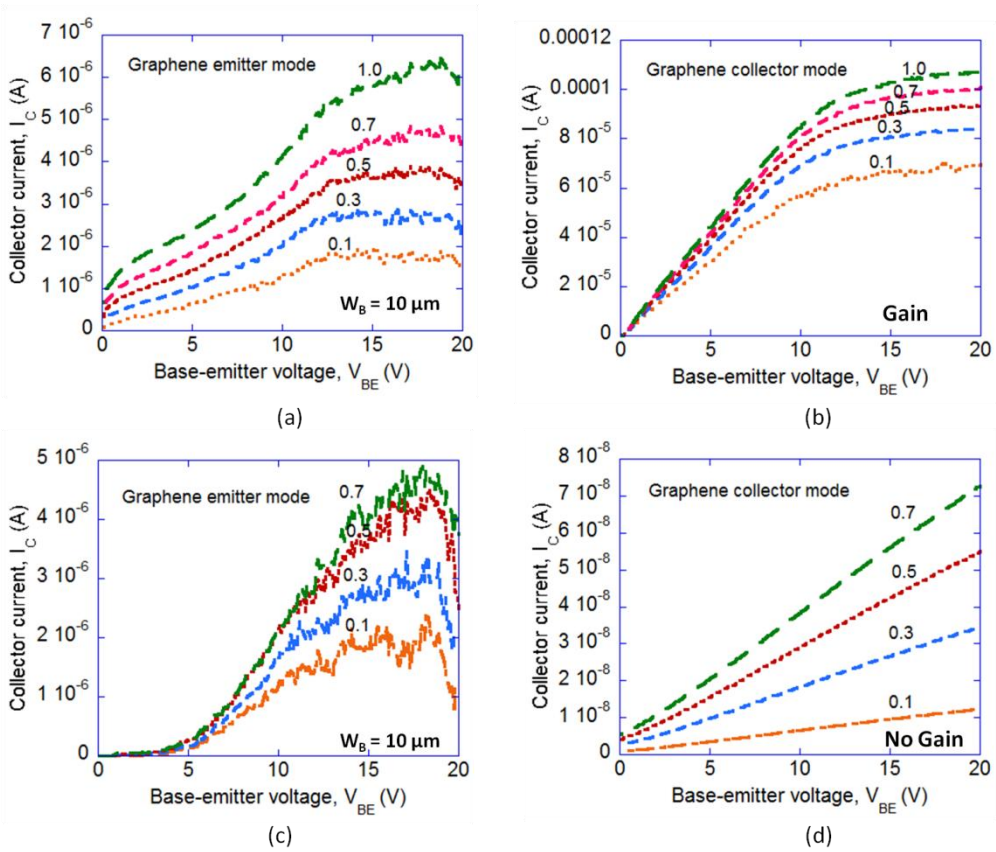

Figure 5.9 Photo-response of the EG/SiC HBPT to 441 nm excitation with dark current subtracted. (a) and (b) are obtained from the device shown in Fig- 5.8 (a). (c) and (d) are from the device shown in Fig-5.8(c). The relative power at each intensity level is given along the curves. P_{rel} = 1 corresponds to an incident power of 43.3 mW/cm^2.

in the visible range. However, the devices showed response to violet/blue excitation at 441 nm, as shown in Fig-5.9. As shown in the figure, the devices showed BJT characteristics in both graphene emitter and graphene collector (in the few devices with gain in this mode), which is puzzling, as the bandgap of 4H-SiC is higher than that required for absorbing a 441 nm excitation..

One possible source of the photocurrent are the stacking faults in the SiC epilayer. Although the bandgap of 4H-SiC is high (3.23 eV), stacking fault regions may be of 3C

or 8H polytype, which have lower band gap energies (2.42 and 2.86 eV respectively) and can absorb radiation in the visible range. However, the EBIC images in Fig-5.8 (a) and (c) show no feature that can be associated with a stacking fault. However, it is to be noted that the EBIC image would reveal the stacking faults only within the depletion region of the EG/SiC interface, not the buried ones. As the back junction is a large area substrate-epilayer junction, any polytype inhomogeneity (in the form of stacking faults) at this interface may be responsible for the observed photo-current.

The responsivity of the devices under visible 441 nm excitation were determined by dividing the active region current by the incident power measured using a handheld semiconductor photo-detector. The maximum responsivity found in the graphene emitter mode was $4.7x10^{-2}$ A/W. For the graphene collector mode the maximum responsivity was estimated at ~28 A/W. Table 5.1 lists the responsivity values obtained from the same device (shown in Fig-5.8c) under UV illumination of similar intensity.The visible rejection ratio is calculated as the ratio between the responsivity values obtained under UV and visible illumination of the same incident power density (4 mW/cm^2). As shown in table- 5.1, the visible rejection ratio is quite low in the graphene collector mode, which is a significant disadvantage in UV detection applications such as flame sensing. It is also interesting to note that the visible rejection ratio much higher for the graphene emitter mode.

The disparity between the visible rejection ratios for the two modes indicate that graphene collector mode is more prone to photo-current generation. If stacking faults are considered responsible for the absorption, the devices with high density of stacking faults near the collector junction are expected to generate a higher base current. It can be noted

Table 5.1 Responsivity to UV and visible illumination and the visible rejection ratio

Mode of operation	UV responsivity, A/W	Responsivity to 441 nm, A/W	Visible rejection ratio
Graphene emitter	20	4.7×10^{-2}	400
Graphene collector	~56	28	~2

that the stacking faults typically cover a wider area near the crystal surface, while the dimension of the fault region reduces with the depth from the surface. Therefore, the majority of the photo-current generation under visible excitation is expected to occur near the graphene/SiC interface. This qualitative argument is consistent with the results, as a high level of current is observed when the graphene/SiC junction acts as the collector-base junction, i.e., in the graphene collector mode.

5.5 CHAPTER SUMMARY

In this chapter, the conditions for highly efficient minority carrier injection are discussed. It is concluded that a near-unity injection ratio can be obtained only under high injection, which requires a high Schottky barrier as well as a collecting/recombining back interface. It is shown that the barrier characteristics of the EG/p-SiC interface is suitable for high level of minority carrier injection. A graphene/p-SiC heterojunction bipolar photo-transistor is reported that uses the semi-metallic graphene layer as the bipolar emitter. The transistor showed a gain of ~300 and responsivity values ~10^2A/W.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 MAJOR OUTCOMES OF THE STUDY

This dissertation studies two major non-ideal effects in SiC Schottky junctions—(i) Forward I-V non-ideality due to interface effects and (ii) Minority carrier injection in large barrier junctions. Large barrier, SiC Schottky junctions were used for this study. The motivation behind studying SiC Schottky junctions was their importance in power electronics and sensing applications.

The epitaxial SiC layers used for the junction formation were grown by a low-particulate halogenated precursor CVD process for ensuring optimum surface morphology and defect density. The step flow growth mechanism was studied in some detail and important reaction parameters were extracted. A PL-based technique was introduced for non-destructive estimation of extended defect density and estimation of carrier lifetime.

Ni/SiC Schottky diodes were fabricated using e-beam evaporation. The I-V characteristics of the as-deposited diodes were observed to deviate from the ideal thermionic emission characteristics. The ideality of the diode characteristics was improved by post-deposition rapid thermal annealing, identifying the interface effects as the source of non-ideality.

The interface effect most widely considered responsible for diode non-ideality is the barrier height inhomogeneity at the Schottky interface. Although the scale of the spatial inhomogeneity can be in the order of the diode dimension down to nanoscopic, the most widely used model for inhomogeneity is the Tung's model, which considers the electrical interaction between the regions of different barrier heights. While Tung's Model can be used with diodes with moderately non-ideal characteristics, the model produces unphysical fitting parameters while fitting highly non-ideal characteristics. The same was observed in the current study for the as-deposited Ni/SiC Schottky contacts. In chapter 4, the applicability limit of Tung's model is analytically studied. It is concluded that the model does not provide accurate results for diodes with ideality factor, $n > 1.2$. It is pointed out that the Tung's model is misused by a number of authors in semiconductor electronics literature, regardless of the ideality of the diodes being analyzed. A clarification is provided for the accurate use of the model parameters, which are, as apparent from the contemporary literature, widely misunderstood.

The non-applicability of Tung's model implies a different non-ideal interface effect in the as-deposited Ni/SiC Schottky diodes. A forward and backward direction bias sweep during the I-V and C-V measurements revealed a hysteresis pattern in the diode current, which supported this argument. In the last part of chapter 4 it is shown that the hysteresis can be explained by the assumption of positively charged interfacial trap centers at the Schottky junction. The dynamic neutralization of the trap centers during electrical characterization is shown to have a significant impact on the diode ideality factor determined from the I-V characteristics. An estimation of the trap density yields an

upper bound of 10^{10} traps/cm^{-2} at the interface. It is shown that the rapid thermal annealing reduced the trap density, resulting in the improvement in the ideality factor.

Chapter 5 discusses the experimental observation of high efficiency minority carrier injection in the epitaxial graphene (EG)/p-SiC interface. Minority carrier injection in Schottky junctions is a less explored territory, despite the widespread observation of this phenomenon in the first half of the twentieth century. The first transistor, developed in the Bell lbs in 1947 was based on this phenomenon. However, the rapid development of semiconductor p-n junction shifted attention from this type of conduction mode in Schottky junctions. The unreliable nature of the early Schottky contacts as well as an incomplete theoretical understanding of the metal point contact led to the development of epitaxial Schottky diodes in the late 1950s. This device scheme inhibits minority carrier injection, and therefore, the notion that Schottky diodes are predominantly majority carrier devices gained widespread acceptance in the scientific community, and the minority carrier injection remained unexplored.

A major accomplishment of this dissertation is the demonstration of a SiC bipolar photo-transistor structure with a EG/p-SiC Schottky emitter. It is to be noted that this is the third material system (after Bardeen's point contact transistor and high temperature diamond devices) to demonstrate Schottky bipolar emitter action. In chapter 5, the theory of minority carrier injection at the Schottky junction is re-visited and the conditions for highly efficient minority carrier injection are determined analytically.

High gain (>200) and high responsivity (~10^1 A/W) to UV radiation were obtained from the fabricated EG/p-SiC heterojunction bipolar photo-transistor (HBPT),

which exceeded those for the conventional UV photodiodes and MSM detectors by several orders of magnitude, and, thereby, showed great commercial prospect as well.

6.2 THE ROAD AHEAD

This dissertation opened up a number of doorways toward future investigation and innovation. Below is a list of interesting and scientifically or technologically important research topics that can draw upon this dissertation.

(a) Ni/SiC Schottky junction for high power devices and sensors

With the well-optimized process of fabricating large barrier Ni/SiC Schottky junctions, the logical step forward is the fabrication of high power Schottky diodes and the study of the blocking capabilities. SiC Schottky diodes have been shown superior performance than Si p-i-n diodes upto a voltage range of 1700 V. It would be interesting to find out the maximum voltage range at which SiC Schottky diodes can operate. The major challenge in this work would be the junction termination for the prevention of edge leakage and breakdown.

Another potential application for the Ni/SiC Schottky junction is nuclear radiation detection. The low z value of Ni makes it an attractive radiation window for nuclear detection applications.

(b) Graphene/p-SiC heterojunction for power switching

SiC power device technology has been focused on n-doped SiC. The large barrier between graphene and p-SiC as well as the bipolar injection capability makes p-SiC an

attractive option. The p-doped epitaxial layer is particularly attractive for bipolar operation because of the high mobility of the minority electrons (7x that of holes). In conventional SiC BJT structures, the p-region is used as a highly doped base, which puts a stringent requirement on the base width. The graphene/p-SiC junction allows a low doped, thick base region, which makes the device design far more flexible.

(c) Tunable graphene/SiC heterojunction sensors

The properties of the few layer epitaxial graphene can be tuned by external stimulus, such as chemi-doping. While most sensors based on this principle focus on lateral FET or metal/graphene Schottky design, the bipolar injection capability can be incorporated into it to increase the noise sensitivity.

Also, the study of the effect of hydrogen intercalation of the graphene layer on the bipolar injection efficiency of the junction seems quite appealing from a theoretical point of view, as this can reveal the interface state properties of the junction.

(d) Graphene-SiC-Graphene MSM phototransistor

The HBPT structure can be improved in a number of ways. However, the simplest form can be achieved by using graphene as both the emitter and the collector junction. The technical challenges toward achieving that includes optimization of the interface states at the EG/SiC junction for collector operation using hydrogen intercalation.

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PUBLICATION RELEVANT TO THIS DISSERTATION

PEER REVIEWED JOURNAL ARTICLES

[1] **S. U. Omar**, T. S. Sudarshan, T A Rana, H Song, MVS Chandrashekhar, "Large barrier, highly uniform and reproducible Ni-Si/4H-SiC forward Schottky diode characteristics: testing the limits of Tung's model", *J. Phys. D: Appl. Phys. 47 295102(29), 2014*.

[2] S. S. Shetu, **S. U. Omar**, K. M. Daniels, B. Daas, J. Andrews, S. Ma, , T. S. Sudarshan, MVS Chandrashekhar, "Si-adatom kinetics in defect mediated growth of multilayer epitaxial graphene films on 6H-SiC", *J. Appl.Phys. 114 (16), 164903 (2013)*.

[3] **S. U. Omar**, MVS Chandrashekhar, I. A. Chowdhury, T. A. Rana, T. S. Sudarshan, "Step dynamics in the homoepitaxial growth of 6H-SiC by chemical vapor deposition on 1° offcut substrate using dichlorosilane as Si precursor", *J. Appl. Phys. 113 (18), 184904 (2013)*.

[4] **S. U. Omar**, T. S. Sudarshan, T. A. Rana, H. Song, MVS Chandrashekhar, "Interface trap induced non-ideality in as-deposited Ni/4H-SiC Schottky barrier diode" (in review at IEEE Trans. Elect. Dev.).

[5] G. J. Brown, **S. U. Omar**, S. S. Shetu, T. S. Sudarshan, MVS Chandrashekhar "Epitaxial Graphene/SiC Schottky Collector Bipolar Photo-Transistor" (in review at IEEE Trans. Elect. Dev

[6] **S. U. Omar** et al., "Efficient minority carrier injection in Graphene/SiC Schottky junction: application to heterojunction bipolar transistor" (in preparation)

[7] **S. U. Omar** et al., "Tunable minority carrier injection characteristics of epitaxial graphene/silicon carbide interface: role of hydrogen intercalation" (study in progress)

CONFERENCE PROCEEDINGS AND TALKS

[1] MVS Chandrashekhar, **S. U. Omar**, G. Brown, S. S. Shetu, M. A. Uddin, H. Song, T. S. Sudarshan, G. Koley, "High Gain Bipolar Photo-Transistor Operation in Graphene/SiC Schottky interfaces: The Role of Minority Carriers.", *IEEE nano, 2014.*

[2] H. Song, T. Rana, MVS Chandrashekhar, **S. U. Omar**, T. S. Sudarshan, "Comparison of SiC epitaxial growth from dichlorosilane and tetrafluorosilane precursors", *ECS Transactions 58 (4), 97-109 (2013)*.

[3] **S. U. Omar**, H. Song, T. S. Sudarshan, MVS Chandrashekhar, "Room Temperature Photoluminescence from 4H-SiC Epilayers: Non-Destructive Estimation of In-Grown Stacking Fault Density", *Mater. Sci. Forum 717, 399-402 (2012).*

[4] H. Song, **S. U. Omar**, T. Rana, MVS Chandrashekhar, T. S. Sudarshan, "In-Grown Stacking Faults in SiC-CVD Using Dichlorosilane and Propane as Precursors", *Mater. Sci. Forum 717, 121-124 (2012)*.

[5] **S. U. Omar**, H. Song, I. Chowdhury, MVS Chandrashekhar, T. Sudarshan, "Step controlled Epitaxy on 4o and 1o offcut SiC substrate using dichlosilane", *Electronic Materials Conference, 2011*.

APPENDIX A – MATERIAL PROPERTIES OF POWER SEMICONDUCTORS

Table A.1 A comparison of Material properties of Si, GaN and SiC for power electronic applications [41]

Properties	**Silicon**	**2H-GaN**	**4H-SiC**
Energy band gap (eV)	1.11	3.4	**3.26**
Intrinsic carrier conc. @ 300K (cm^{-3})	10^{10}	10^{-10}	**10^{-7}**
Breakdown electric field @ $N_D = 10^{17}$ cm^{-3} (MV/cm)	0.3	3.5	**3**
Saturated electron drift velocity 10^7(cm/s)	1	2.5	**2**
Electron mobility @ $N_D = 10^{16}$ cm^{-3} (cm^2/Vs)	1450	900	**800**
Relative dielectric constant	11.7	7.8	**9.7**
Thermal conductivity (W/cm-K)	1.5	1.3	**3 ~ 5**
Vertical and bipolar current conduction	yes	no	**yes**
Commercial wafer diameter as of 2011 (mm)	300	none	**100**

APPENDIX B – PROCESS FLOW FOR BASIC LITHOGRAPHY

Task-0: Back side lapping for ohmic contact formation

1. Apply 9 μm diamond paste on a glass plate and add water
2. Hold sample by wax stick and lap on the paste
3. ~20 min required to get an uniformly opaque back side.

Task-1: Wafer cleaning

1. Organic (RCA) cleaning
    a. Pour trichloroethylene (TCE) in a beaker. Put beaker on the hot plate (> 150^{o}C), bring TCE to boil. Put the sample in the TCE and keep for 2-3 min.
    b. Boil/Sonicate acetone (ACE). Transfer the sample directly into the acetone beaker . Boil for 2-3 min.
    c. Boil methanol (METH) in a beaker. Transfer the sample directly into the METH beaker. Boil for 2-3 min.
    d. Pour DI water in the METH beaker. Change water for at least 20 times.
    e. Blow dry.

Things to note: Never expose sample to air during transfer between solvents or during boiling. Dispose of the used solution in the designated waste containers.

Task-1 continued...

2. RCA or standard solutions

The RCA or standrad solutions, developed by the researchers at the Radio Corporation of America (RCA) is used for removing organic and ionic residue. The process mildly oxidizes the wafer surface and needs to be followed by an HF/BOE etch.

- RCA-1 solution (organic decontamination):
    a. Add NH_4OH (1 part) with DI water (5 parts) and heat up to 70^oC (takes ~4 min on a 250^oC hot plate).
    b. Add 1 part of H_2O_2 at which point the solution starts bubbling. Put the wafer in and boil for 10 min. Covering the solution gives better result.
    c. Once the cleaning is done, rinse with DI water by water change.
    d. Dispose the used RCA solution in the designated waste container.
- RCA-2 solution (ionic/metallic decontamination)
    a. Add HCl (1 part) to DI water (4 parts) and heat up to 70^oC.
    b. Add 1 part of H_2O_2 at which point the solution starts bubbling. Put the wafer in and boil for 10 min.
    c. Once the cleaning is done, rinse with DI water by water change. No HF dip is necessary for RCA-2.
    d. Dispose the used RCA solution in the acid waste container.

3. Piranha solution (organic decontamination, alt. RCA-1)

a. Add 3 parts of H2SO4 in a beaker. Add 1 part of H2O¬2 (< 30%). The solution will be hot and bubbling.
b. Bring sample out and rinse with water. Teflon tweezers recommended.
c. Leave the solution in the beaker for a while, and dispose when cooled down.
d. Piranha attacks metal. Wafers with metal not recommended.
e. Sample is oxidized. Must be followed by HF dip.

4. Hydrofluoric acid (HF) dip (oxide etch)
    a. Dip the sample in 1:10 HF or BOE solution for 1 min. HF etches glass. Must use Teflon container and tweezers.
    b. Dip sample in water and rinse by water change for at least 30 times.
    c. Dispose HF solution in the designated waste container.

Task-2: Removal of the (possibly non-stoichiometric) surface layer

Reactive ion etching (RIE)

- Oxygen plasma etch for surface contamination removal
- SF_6 etch for removal of the surface layer altogether (250 mT, 300W, etc rate ~0.3 μm/min)
- Chamber cleaning is required after each use (360 mT, 400W, 10 min O_2 plasma).

Dry oxidation

- Sample must be cleaned by the RCA-2 before oxidation.
- Dry oxidation for 4 hrs at > 1100^{o}C
- Post oxidation HF dip (1 min)

Task-3: E-beam evaporation of metal

1. Sample loading and chamber evacuation
    a. Fill the chamber with N_2. Open the lid. Shut down N_2.
    b. Check the detector crystal status. Check deposition on the mirror. Clean deposits and dust inside the chamber using vacuum cleaner.
    c. Inspect metal boat. Load desired metal boat.
    d. Load sample using the Tungsten holders.
    e. Close lid and turn on mechanical pump. Open the roughing pump valve.
    f. Once the pressure reaches 10^{-2} torrs, close roughing pump valve.
    g. Open the high vacuum valve that connects the Turbo exhaust to the roughing pump.
    h. Turn on Turbo pump. Open the gate valve.
    i. Pump down for 6 ~ 7 hours.
2. Metal deposition
    a. Turn on water.
    b. Once the desired background pressure is reached, turn on the HV generator and the sweep controller.
    c. Set e-beam bias at 7.5 kV.
    d. Increase the filament current to the desired level. Check e-beam position on the boat. It should be at the center.
    e. Turn off vacuum gauge. Open shutter and start deposition. The parameters commonly used are as follows--

        Background pressure: ~ $2x10^{-6}$ torrs.

Filament current: 91 ~ 96 mA for Ni

~ 90 mA for Ti

105 ~ 110 mA for Au

Deposition rate : 1 ~ 4 A^o/s

Metal thickness: 80 ~ 110 nm (0.800 ~ 1.10 kA^o) for ohmic contacts. < 70 nm for Schottky contact formation.

Task-4: Mask aligner preparation

1. Turn on air compressor and N_2 valves
2. Turn on pump and vacuum valve
3. Switch on the module under the table
4. After several system checks it will show RDY
5. Push the Start button. The display will alternate between cold and hot, as it tries to fire the lamp on.
6. Once the lamp is on, the display will settle to 275W (may show 274 too). This may take more than 5 min.

Task-5: Photoresist coating

1. Turn on spin coater (small red switch and module power switch)
2. Dry sample on hot plate at 100^{o}C for 5 min.
3. Set recipe# to 0. Add one drop of HMDS on wafer and spin. (not recommended)
4. Set appropriate recipe for the resist (recipe#1 for AZ 1518 and 5214). Add one drop at the center of the sample ad spin immidiately.
5. Remove edge beads using a blade or the edge bead remover (EBR) solution.

6. Pre-exposure bake: On hot plate at 90^{o}C for 90 s (AZ1518) to drive away solvent.

   Follow recipe for other resists.

Task-6: UV Exposure

- Old/left MJB-3 mask aligner

  Exposure time: ~90s

- New/right MJB-3 mask aligner (i-line intensity 18 ~ 21 mW/cm^2)

  Exposure time: 3 ~ 5 sec (AZ1518)

  7 ~ 9 sec (AZ 5214)

Task-7: Photoresist development and loading into E-beam

1. Post bake for 60s @110^{o}C (AZ 1518). Follow recipe for other resists.
2. Prepare developer solution-- AZ400K: H2O = 1:4 (4:16 mL)
3. Dip sample in the developer (~60 sec for the old AZ1518, ~20 sec for AZ 5214)
4. Rinse in DI water. Add in small droplets
5. Blow dry.

Task-8: Metal lift-off (AZ1518 and AZ5214)

1. Heat up sample in Acetone for > 5min, shake the beaker gently.
2. Sonicate for ~5 min if metal remains.
3. Transfer sample in boiling methanol.
4. Rinse with DI water.

Task-9: Post-deposition annealing

- Ni ohmic contact: 1000^{o}C, 60 ~ 120 sec
- Ni Schottky contact: 650 - 800 ^{o}C, 60 ~ 120 sec

Task-10: Ni contact etch

1. Use the H_3PO_4 based Nickel etchant to etch away the front contacts.
2. Use HCl : HNO_3: HF = 1:1:1 to etch away the back contact. It will look dark.
3. Burn the black residue (graphite?) in the oxidation furnace for 1 hr.

APPENDIX C –PROCESS FLOW FOR THE FABRICATION OF NI/SIC SCHOTTKY DIODE

Process flow for Ni/SiC Schottky diode fabrication

1. Standard RCA cleaning of the substrate followed by HF dip
2. Epitaxial growth of n-doped SiC in the CVD furnace
3. Backside (C-face, substrate) lapping in diamond paste
4. Standard RCA cleaning (including RCA-2) of the substrate followed by HF dip.
5. Dry oxidation at 1150^{o}C for > 4 hrs
6. HF dip for removing oxide
7. Deposition of a 100 nm thick Ni film by e-beam evaporation on the backside for ohmic contact
8. Rapid thermal annealing at 1000^{o}C for 120 sec for ohmic contact formation.

   Caution: the top surface (Si-face) may get contaminated at this step.
9. Photolithography for Schottky contact area definition.
10. E-beam evaporation of the Schottky metal on the photo-masked top side.
11. Metal lift-off in acetone

APPENDIX D –PROCESS FLOW FOR THE FABRICATION OF EPITAXIAL GRAPHENE/SIC HETEROJUNCTION BIPOLAR PHOTOTRANSISTOR

Process flow for Ni/SiC Schottky diode fabrication–

1. Standard RCA cleaning of the substrate followed by HF dip
2. Epitaxial growth of lightly p-doped SiC on highly n-doped SiC in the CVD furnace
3. Backside (C-face, substrate) lapping in diamond paste
4. Standard RCA cleaning (including RCA-2) of the substrate followed by HF dip.
5. Growth of epitaxial graphene by thermal evaporation of the Si-face at > 1300^{o}C.
6. Deposition of a Ti(40 nm)/Au(20 nm) film by sputtering on the backside for ohmic contact
7. Photolithography for graphene contact area definition.
8. Oxygen plasma etch of the unmasked region. The parameters are as follows--
    - Power 150 W
    - Pressure: 300 mT
    - Duration: 45 sec
9. PR rinse in acetone. Rinse in methanol and then DI water.
10. An additional photolithography step for defining contact area on the graphene 'dots'.
11. E-beam evaporation of a 70 nm Ni film (poor adhesion).

APPENDIX E – BASE CURRENT MEASUREMENT FOR EG/SIC HETEROJUNCTION BIPOLAR PHOTOTRANSISTOR UNDER UV ILLUMINATION

An Omnicure S1000 UV curing lamp was used for the HBPT characterization. The lamp spectrum can be found in the user datasheet by the vendor. The lamp spectrum consists of four significant lines – 312, 334, 365 and 404 nm. The band gap energy of 4H-SiC is 3.23 eV, corresponding to a wavelength of ~385 nm. Therefore, we consider the intensities of the first three lines for the base current calculation.

The generation rate of photo-carriers at depth x is given by–

$$G = \frac{\alpha P_{opt}}{E_{ph} A} \exp(-\alpha x) \tag{E.1}$$

Here, α = absorption coefficient of 4H-SiC at that particular λ_{ex}, P_{opt} is the incident power, E_{ph} is the corresponding photon energy (hν), A is the device active area.

An estimate of the base current, I_B can be obtained by integrating the generation rate over the entire base width (W_B) –

$$I_{B,\lambda_{ex}} = q \int_0^{W_B} G(x) dx \tag{E.2}$$

Equation (E.2) can be solved as–

$$I_{B,\lambda_{ex}} = \frac{q P_{opt}}{E_{ph} A} \left\{1 - \exp\left(-\alpha W_B\right)\right\} \tag{E.3}$$

The detector used for power measurement was a 365 nm detector. For the other two wavelengths (312 and 334 nm), the relative lamp intensity was calculated from the lamp spectrum provided by the vendor, and the corresponding P_{opt} were obtained. The lineshape of the spectral lines were also considered by assuming a Gaussian shape. The right hand side of equation E.3 was evaluated for each wavelength using the corresponding α, and the total base current was determined as an aggregate of the three.