Heterogeneous Integration of AlN MEMS Contour-Mode Resonators and CMOS circuits

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Acknowledgments

"وَمَا تَوْفِيقِي إِلَّا بِاللَّهِ ۚ عَلَيْهِ تَوَكَّلْتُ وَإِلَيْهِ أُنِيبُ" (11:88)

My success lies only with Allah. In Him I trust and to Him I turn!

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Abstract

The increasing demand for high performance and miniature high frequency electronics has motivated the development of Micro-electro Mechanical Systems (MEMS) resonators, some of which have already become a commercial success for the making of filters, duplexers and oscillators used in radio frequency (RF) front-end systems for portable electronic devices. These MEMS components not only enable size, power and cost reduction with respect to their existing counterparts, but also open exciting opportunities for implementing new functionalities when used in large arrays. Almost all MEMS resonators require interfacing with one or more Complementary Metal Oxide Semiconductor (CMOS) integrated circuit components or modules in processing raw signals from individual MEMS devices. Hence, these devices should be integrated with CMOS circuits in an efficient and robust way in order to facilitate their deployment in large arrays with minimal parasitics, delay and power losses due to signal routing and CMOS-MEMS interconnects.

Among the MEMS resonators developed to date, Aluminum Nitride (AlN) MEMS Contour-Mode Resonators (CMRs) offer high electro-mechanical coupling coefficient (k_t^2) and quality factor (Q), and a center frequency (f_o) that can be set lithographically by varying the device in-plane dimensions. Also, AlN MEMS CMRs can be fabricated using state-of-the-art CMOS processes and micromachining techniques. These properties allow the synthesis of multi-

frequency band-pass filters (BPFs) on a single chip with a low insertion loss and the capability of direct matching to 50 Ω systems. All these advantages, along with a sufficiently mature fabrication process, make AlN CMRs one of the ideal candidates for pursuing their integration with CMOS technology and implement high performance filters with programming capability.

In this work we develop for the first time a three-dimensional (3D) heterogeneously integrated AlN MEMS-CMOS platform that enables the realization of such systems as self- healing filters for RF front-ends and programmable filter arrays for cognitive radios. We collaborated with the A*STAR, Institute of Microelectronics (IME), Singapore in the development of AlN MEMS platform on an 8" silicon (Si) wafer; on the other hand, CMOS chips were fabricated in 65 nm International Business Machines Corporation (IBM) and 28 nm Samsung processes. Solder bumps were placed on CMOS chips by Tag and Label Manufacturers Institute (TLMI) under the supervision of Metal Oxide Semiconductor Implementation Service (MOSIS). We demonstrated 3D integrated chip stacks with primary RF signal routing on MEMS and on CMOS for self-healing filters, and showcased the other system via wire-bonding to off-the-shelf CMOS components on a printed circuit board (PCB) because of the inability to continue to have access to the CMOS wafers and bumping processes over the last two years of the project.

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Chapter 1

Introduction

1.1 AlN Contour-Mode Resonators and Filters

The details of the operational principles of AlN MEMS CMRs can be found in [1]. Briefly, a piezoelectric AlN thin film plate is sandwiched between a bottom metal plate and interdigitated top metal electrodes to form the resonator body (see Figure 1-1). Each top metal electrode is connected alternatively to signal and ground voltages in a one-port configuration or to two different signals acting as actuating and sensing mechanisms in a two-port configuration. These signals and ground voltages generate an electric field across the piezoelectric material whose vertical component induces a lateral strain in the AlN thin film by means of the equivalent d_{31} component of the d-form piezoelectric matrix. The bottom metal plate here serves the purpose of directing the electric fields vertically rather than laterally which is required for efficient excitation of the contour-mode of vibration. To this end, the bottom metal plate is left floating in one-port configuration whereas it is grounded in the two-port implementation. The lateral strain in the direction of the resonator's width provides in-plane dilation or contraction of the structure, which resonates at f_o, as defined in [2]:

$$f_0 = \frac{1}{2\,P}\sqrt{\frac{E_{eff}}{\rho_{eff}}} \tag{1.1}$$

In Eq. (1.1), P is a geometrical property and represents the pitch of the electrodes; E_{eff} and ρ_{eff} are material properties and represent respectively the effective Young's modulus and effective mass density of the resonator body, which include combined effect of metal layers and AlN thin film. Note that E_{eff} and ρ_{eff} have secondary impacts in setting the center frequency of the device once the types of metal layers and thicknesses of all layers in the resonator body are set. Therefore, for AlN CMRs, we say that f_o is primarily set by a lithographically defined in-plane dimension, *i.e.* P.

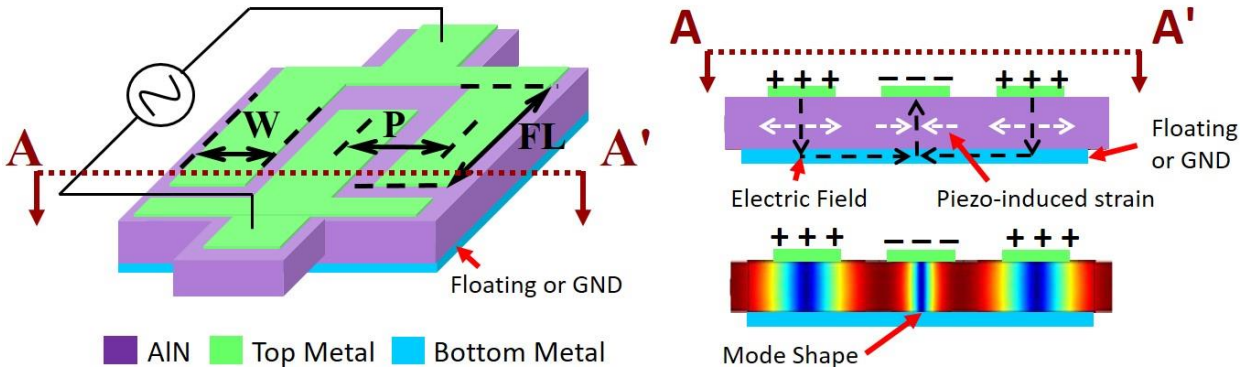


Figure 1-1. Three finger AlN CMR mock-up with its cross-sectional view and mode shape at f_o. Several critical geometrical resonator parameters such as electrode pitch (P), electrode coverage (W) and finger length (FL) are also shown on the resonator mock-up.

Both one-port and two-port equivalent circuit representations of AlN MEMS CMRs are shown in Figure 1-2. The series RLC characterizes the motional behavior of the resonator. On the other hand, the device capacitance (C_o) characterizes the capacitive behavior of a dielectric material, *i.e.* AlN. In the two-port configuration, the cross talking between signals in top metal interdigitated electrodes requires addition of a feed-through capacitance (C_f) to the circuit model for a better representation of the device behavior [1]. Additionally, the transformer turn ratio (N) in two-port

configuration represents the ratio of total metallized area at input (actuator) and output (sensor) of the resonator. Sample admittance response of these ideal models can be found in Figure 1-3.

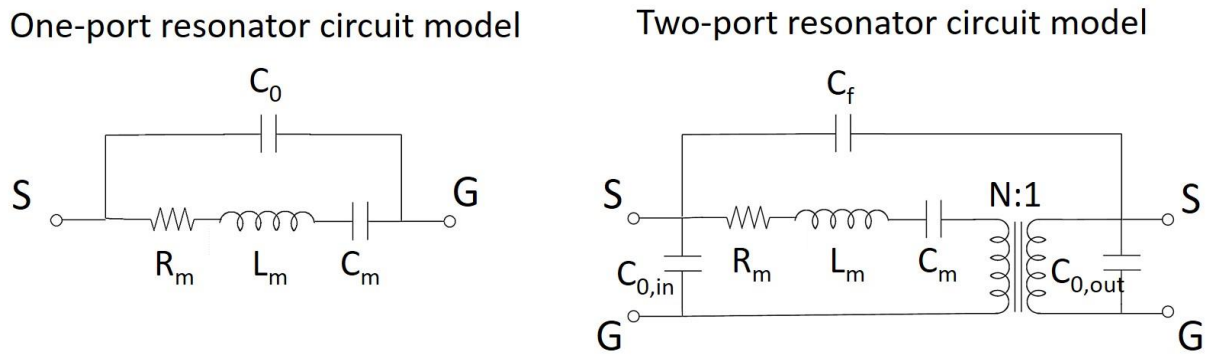


Figure 1-2. Equivalent circuit representation of one-port and two-port resonators using Butterworth-Van Dyke model.

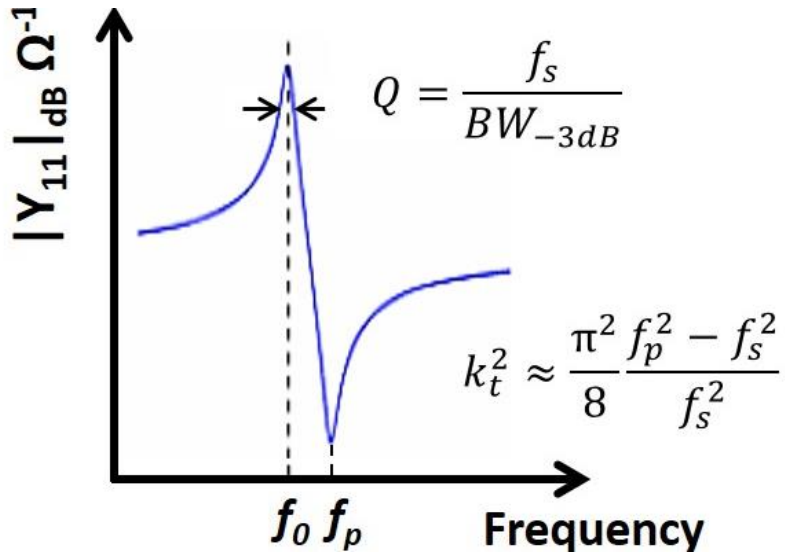


Figure 1-3. Ideal admittance frequency response of AlN MEMS CMRs.

Apart from the C_o and f_o, there are two other critical resonator parameters that are used to quantify the performance of the AlN MEMS CMRs and extract the circuit model parameters from the measurement data. These are Q and k_t^2, and both of them are defined in Figure 1-3 based on

[3]. The product of these two parameters are also known as the Figure of Merit ($FoM = k_t^2 \cdot Q$) for acoustic resonators used in filters [4]-[5]. We use this parameter too as a performance metric in the analysis of these resonators provided in this thesis. After the resonator geometry is defined, the motional circuit parameters can be calculated using only f_o, Q, k_t^2 and device capacitances (C_o, $C_{o,in}$ and $C_{o,out}$). The list of these equations are provided in Figure 1-4 for both one-port and two port AlN MEMS CMRs. Since we use relatively large number of fingers at input and output with the same amount of electroded area per each finger in the two-port resonators designed within the scope of this thesis, we assume n_{in}, n_{out} and N of 1 in the circuit simulations and report the average of $C_{o,in}$ and $C_{o,out}$ as C_o in the measured parameter extraction.

Equations for one-port resonator

$$L_m = \frac{\pi^2}{8}\frac{1}{\omega_0^2 C_0 k_t^2}$$

$$R_m = \frac{\pi^2}{8}\frac{1}{\omega_0 C_0 k_t^2 Q}$$

$$C_m = \frac{8}{\pi^2} C_0 k_t^2$$

Equations for two-port resonator

$$L_m = \frac{\pi^2}{8}\frac{1}{\omega_0^2 C_{0,in} k_t^2}\frac{n_{in}+n_{out}}{n_{in}}$$

$$R_m = \frac{\pi^2}{8}\frac{1}{\omega_0 C_{0,in} k_t^2 Q}\frac{n_{in}+n_{out}}{n_{in}} \qquad N = \frac{n_{in}}{n_{out}}$$

$$C_m = \frac{8}{\pi^2} C_{0,in} k_t^2 \frac{n_{in}}{n_{in}+n_{out}}$$

Figure 1-4. Equations that describe the motional parameters of one and two port AlN MEMS CMRs in the equivalent circuit model shown in Figure 1-2. Here n_{in} and n_{out} are the total number of fingers at input and output of two port resonator, respectively. They are assumed to be 1 in the circuit simulations. Co reported for two port resonators later in the thesis are the average of the extracted $C_{o,in}$ and $C_{o,out}$ from the measurements.

A sample filter response from three cascaded two-port resonators can be found in Figure 1-5. In this figure, the critical filter parameters that are used to quantify the performance of filters in this thesis are also shown. Among them are filter center frequency (f_o), insertion loss (IL), filter bandwidth (BW) and out-of-band rejection (OBR). The characteristics and detailed mathematical

and theoretical analysis of this type of filters can be found in [6]. This filter type has been chosen since two-port network configuration of the AlN MEMS CMR device enables direct synthesis of the filters without any additional design or geometrical changes in the resonators by means of self-coupling of resonators through device capacitance. We cascade three of the two-port resonators in series in order to widen the filter bandwidth by means of flattening the filter passband via extra poles [7].

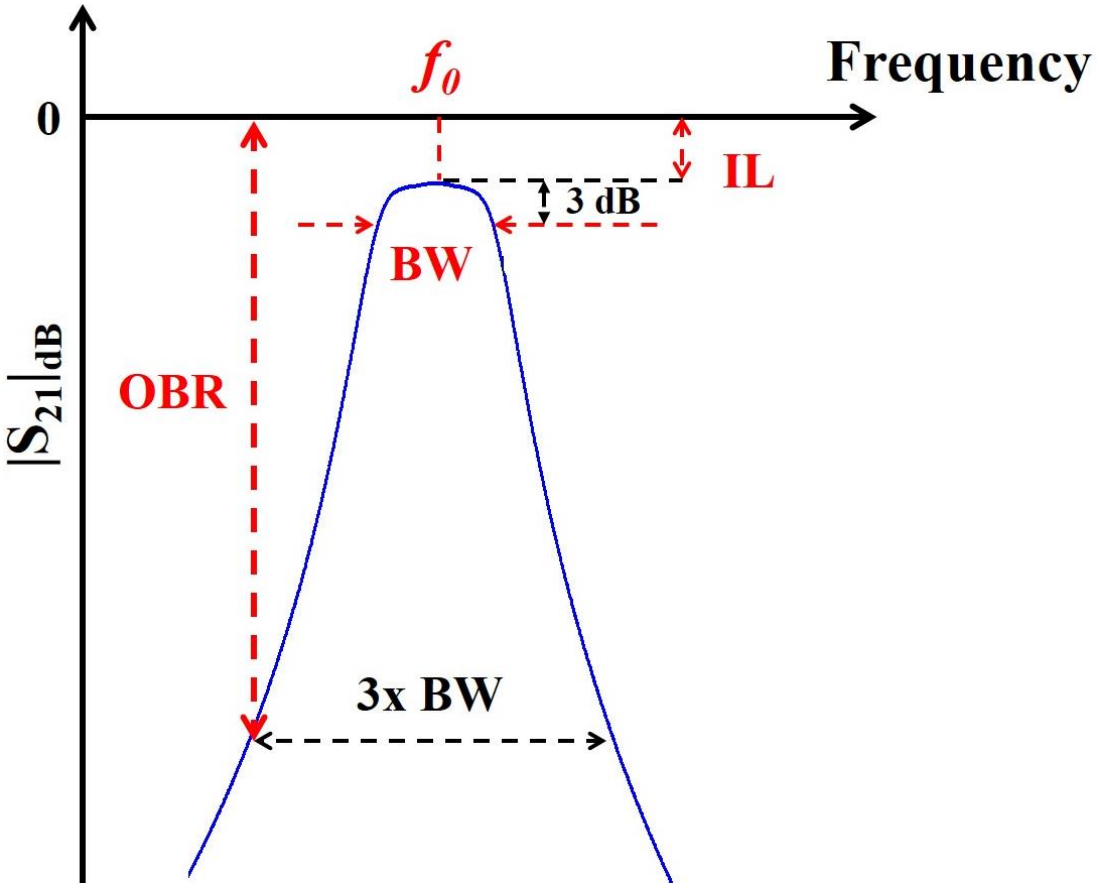


Figure 1-5. Ideal filter frequency response of AlN MEMS CMRs when three of two-port resonators are cascaded in series. Description of critical filter parameters that characterize the performance are also shown on the figure with red markers and red text color.

1.2 Approach for AlN MEMS-CMOS Integration

Various AlN MEMS-CMOS integration methods have been previously shown in [8]-[10]. Each approach has its own unique advantages and drawbacks. We can simply classify CMOS-MEMS integration methods as monolithic integration and hybrid (heterogeneous) integration in terms of the number of substrates used in the final integrated technology [11]. As the name suggests, monolithic integration has a single substrate and both technologies are fabricated on a single wafer; whereas, in hybrid integration there are two or more substrates in the final chip stack and each technology is processed individually up to a certain step, and then integrated to the other technology via bonding. Based on the application, any of these approaches can be more favorable [12], [13]. The superior advantage of the hybrid integration is that each technology can be developed, modified and upgraded independently from one another. This feature does not only decrease the fabrication complexity, development time and cost of integration but also provides more flexibility in choosing or advancing the technology of each chip in the stack [14].

Hybrid integration can be achieved via various bonding methods. Among them wafer level bonding, wire-bonding and flip-chip bonding are the most common ones. These bonds also serve as signal interconnects between the technologies in the integration. Each bonding type has its own unique advantages and drawbacks based on the application [8]-[10]. Since AlN MEMS resonators are much larger in size with respect to CMOS transistors in 28 nm and 65 nm technology nodes and fabrication costs are higher in CMOS, the wafer-bonding approach would result in inefficient use of the CMOS wafer area, and thereby, resources, for all the systems built in this thesis [15]. Moreover, we require high level of integration between AlN MEMS and CMOS technologies in order to employ large arrays of MEMS devices in an efficient and low loss manner. Thus, flip-chip bonding would be more favorable over wire-bonding approach considering the parasitics and efficient use of chip areas [16]. That is why we developed AlN MEMS platform for 3D hybrid integration with CMOS circuits using flip-chip bonding process.

1.3 Challenges in Development of AlN MEMS Platform for 3D Hybrid Integration with CMOS circuits

Despite the general maturity of the AlN MEMS resonator technology, there are some major challenges that have to be overcome in order to enable successful 3D integration of AlN MEMS with CMOS. Here is a list of the challenges we had to consider and overcome in this work:

1. The AlN MEMS fabrication platform needs to be developed on an 8" Si wafer for mass production and in a foundry fab line for better repeatability and success rate. This means that process steps, material stacks and yields have to be re-characterized with respect to the university-level demonstrations.

2. Suspended devices in the MEMS chip need to be protected from the environment and during the flip-chip bonding process, thus a hermetic thin-film encapsulation (TFE) of AlN CMRs has to be developed [16]. This would also allow growing additional layers on top of the resonators (*i.e.* signal re-distribution layers) which can be used for signal routing without affecting the device performance [17].

3. Parasitics coming from signal routing (due to device size mismatch in MEMS and CMOS technologies and placement of input/output, *i.e.* I/O pads) requires the development of low loss re-distribution layers (RDL) on top of AlN MEMS devices. It is well-known that signals working at RF are considerably sensitive to the routing parasitics and associated losses [18]. Since there are two different technologies in the integration, we have two possible platforms for the RF routing. We either use the default built-in relatively thick, but lossy, metal layers on CMOS or develop low loss RDL on AlN MEMS platform for RF signal routing. In CMOS, DC and logic routings are also distributed all over the chip, and thus parasitic coupling to RF is highly probable. Additionally, without RDL on MEMS, the CMOS die becomes the substrate chip in the 3D hybrid integration. This limits the MEMS

chip size and circuit complexity, and also causes a very inefficient occupancy of CMOS chip as the MEMS structures are much bigger in size. Since CMOS fabrication also costs more, in mass production the unit price for the 3D integrated chip stack would be higher if the CMOS chip is the substrate chip. Depending on the system, the RDL can also enable more flexibility in device placement and complexity of circuits. That is why we prefer to develop re-distribution layers on AlN MEMS platform.

4. In order to facilitate the AlN MEMS integration to the CMOS chips, bonding pads on both MEMS and CMOS chips should be covered with under-bump-metallization (UBM).

5. The AlN MEMS platform should allow for fabrication of large arrays of devices and minimize the cost of a single AlN MEMS device and AlN MEMS-CMOS chip stack, all of which are beneficial from both cost and area standpoints for system level approaches [19]. For this purpose, fabrication of AlN MEMS resonators and filters should allow dense population of these devices in small vicinity on the wafer. One way of achieving this is to use isolation trenches in the sacrificial material, which limit the size of the suspended area in each device. Thanks to the deterministic release barriers, supporting points for the suspended resonator body can also be clearly defined, which enables proper and efficient design of encapsulation layers. This does not only favor a more compact design of large arrays but also accommodates a significant reduction in parasitics and losses because of the reduced length in device interconnects and routing.

Chapter 2 describes how these challenges have been overcome, whereas the system level demonstrations of 3D hybrid integration are provided in Chapter 3 along with the detailed description of the proof-of-concept system application.

1.4 Thesis Contributions and Organization

The main goal of this thesis is to develop an AlN MEMS platform on an 8" Si wafer in collaboration with IME so that it can be 3D hybrid integrated with CMOS technology in an efficient and robust way for systems requiring large arrays of resonators. We also realized two prototypes of heterogeneously integrated AlN MEMS/CMOS systems, one of which was demonstrated on the 3D hybrid platform, and other was realized on a PCB via wire-bonding of CMOS components to the AlN MEMS. To itemize the complete list of contributions this thesis focuses on:

- Overcoming the challenges related to the synthesis of an AlN MEMS platform on an 8" Si wafer for 3D hybrid integration with CMOS, namely the realization of a high yield fabrication process with TFE and RDL.
- Achieving high FoM, Q, and k_t^2, and simultaneously pushing spurious modes away from bandwidth of interests in AlN CMRs operating at around 1 GHz.
- Designing high performance RDL on AlN MEMS platform to facilitate low loss signal routing.
- Validating the hermeticity of TFE for AlN MEMS CMRs through aging tests.
- Demonstrating self-healing AlN MEMS filters bank through 3D hybrid integration with CMOS circuits with and without the availability of MEMS front-end RDL.
- Designing and demonstrating programmable AlN MEMS filter arrays for cognitive radios.

The rest of the thesis is organized as follows. In Chapter 2, we define the fabrication process flow for AlN MEMS platform and provide design of experiments for individual MEMS only devices to achieve high performance resonators and filters. Then, we explain the development of wafer-level thin-film encapsulation of AlN MEMS devices to protect them environmentally and during bonding process, and describe the development of re-distribution metallization layers on top of encapsulated resonators and filters for low loss signal routing at radio frequencies. We also

detail the issues of each stage in the fabrication of AlN MEMS platform separately and discuss the techniques we employed to overcome such issues. Next, we analyze the lifespan of the encapsulated resonators under harsh environmental conditions by making an oscillator using the resonators and monitoring the frequency of oscillation over time till the oscillation stops. At the end of this chapter, the selected resonator geometry and corresponding resonator and filter responses are shown and their performances are assessed.

In Chapter 3, we describe a hybrid 3D integrated AlN MEMS and CMOS chip stack with which we demonstrate the application of statistical element selection technique (SES) on self-healing AlN MEMS filters with CMOS circuits. The details of the SES algorithm and its system-level application for the design of self-healing AlN MEMS filters and CMOS circuits are also provided in this chapter. We also make a comparison of RDL signal routing with primary RF routing on CMOS for a 3D integrated chip stack.

In Chapter 4, we talk about the design and related constraints of programmable filter arrays for cognitive radios which is the other heterogeneously integrated AlN MEMS and CMOS system studied in this thesis. By taking advantage of this system, we also explore another filter switching technique. First, we explain its beneficial advantages and associated challenges. Then, we provide our design approaches (*i.e.*, co-optimization of technology and architecture) to deal with them. Since we realized this system by wirebonding AlN MEMS devices to the over-the-counter CMOS components on a PCB, we also discuss the performance limits of this system realized without the availability of 3D integrated AlN MEMS-CMOS chip stacking platform.

Finally, we conclude the thesis in Chapter 5 with a brief summary of the main achievements and describe possible future research directions using the developed AlN MEMS platform for 3D heterogeneous integration to CMOS.

Chapter 2

Development of AlN MEMS Platform for 3D Hybrid Integration with CMOS Chip

In this chapter we provide the details of AlN MEMS platform developed on an 8" Si wafer in collaboration with A*STAR, IME, Singapore. The developed cross-sectional overview of AlN MEMS platform with 3D hybrid integration to CMOS is shown in Figure 2-1. The development of the platform can be divided into three main stages: (i) fabrication of MEMS devices (*i.e.* AlN CMRs and filters), (ii) thin-film encapsulation of the same, and (iii) growth of RDL for efficient and low loss signal routing. All of these processes are developed and characterized separately step-by-step during the course of this work. The unique challenges of and solutions for each stage are provided in the subsections below, as well as, the detailed description of the full fabrication process flow for the AlN MEMS platform.

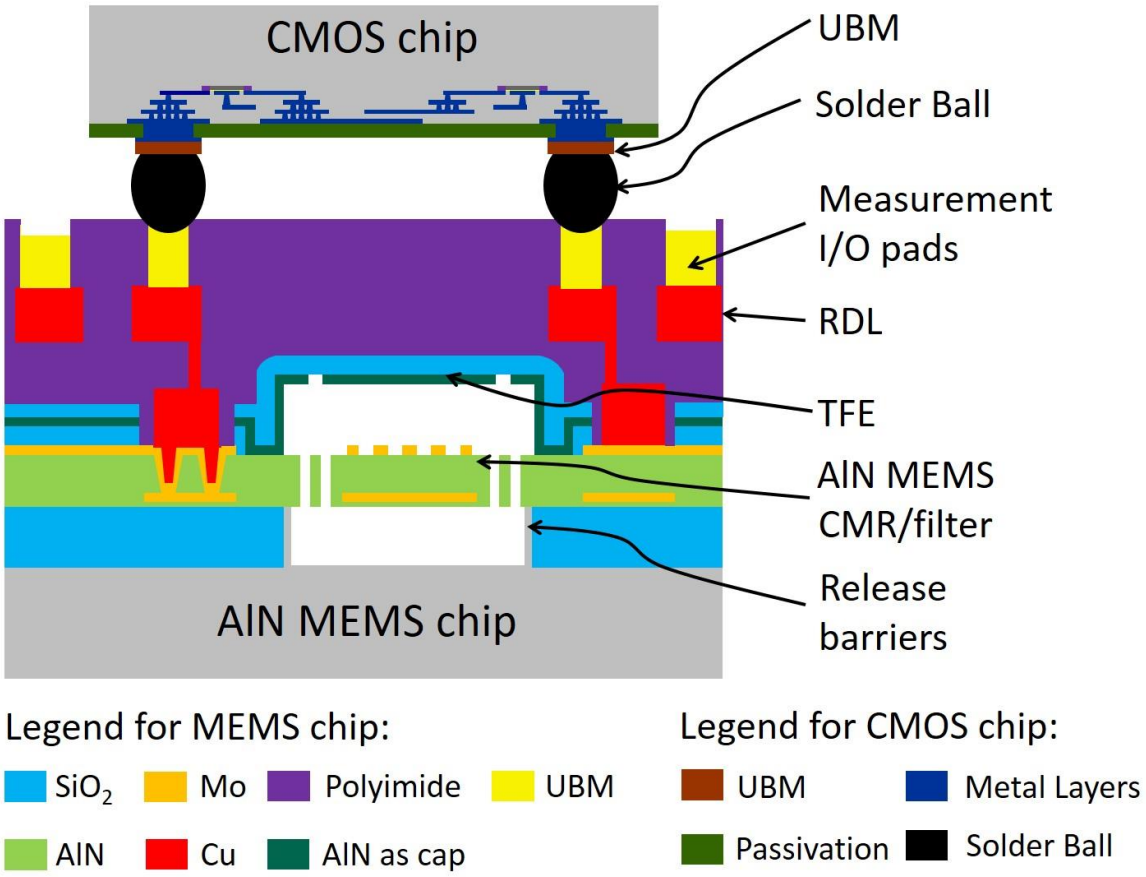


Figure 2-1. Cross-sectional cartoon view of the developed AlN MEMS platform with its 3D hybrid integration to a CMOS chip.

2.1 Fabrication of AlN MEMS Platform on an 8" Silicon Wafer

All the AlN MEMS fabrication is done by A*STAR, IME, Singapore. Figure 2-2 shows the developed fabrication process flow for the AlN MEMS platform that can be 3D hybrid integrated with CMOS dies. As previously noted, we can divide the fabrication flow in three main stages based on the purpose of each one of them and characteristic challenges. These stages are MEMS (to form the devices), TFE (to package the devices) and RDL (to provide low loss signal routing environment). We describe the process flow stage by stage based on the steps on Figure 2-2.

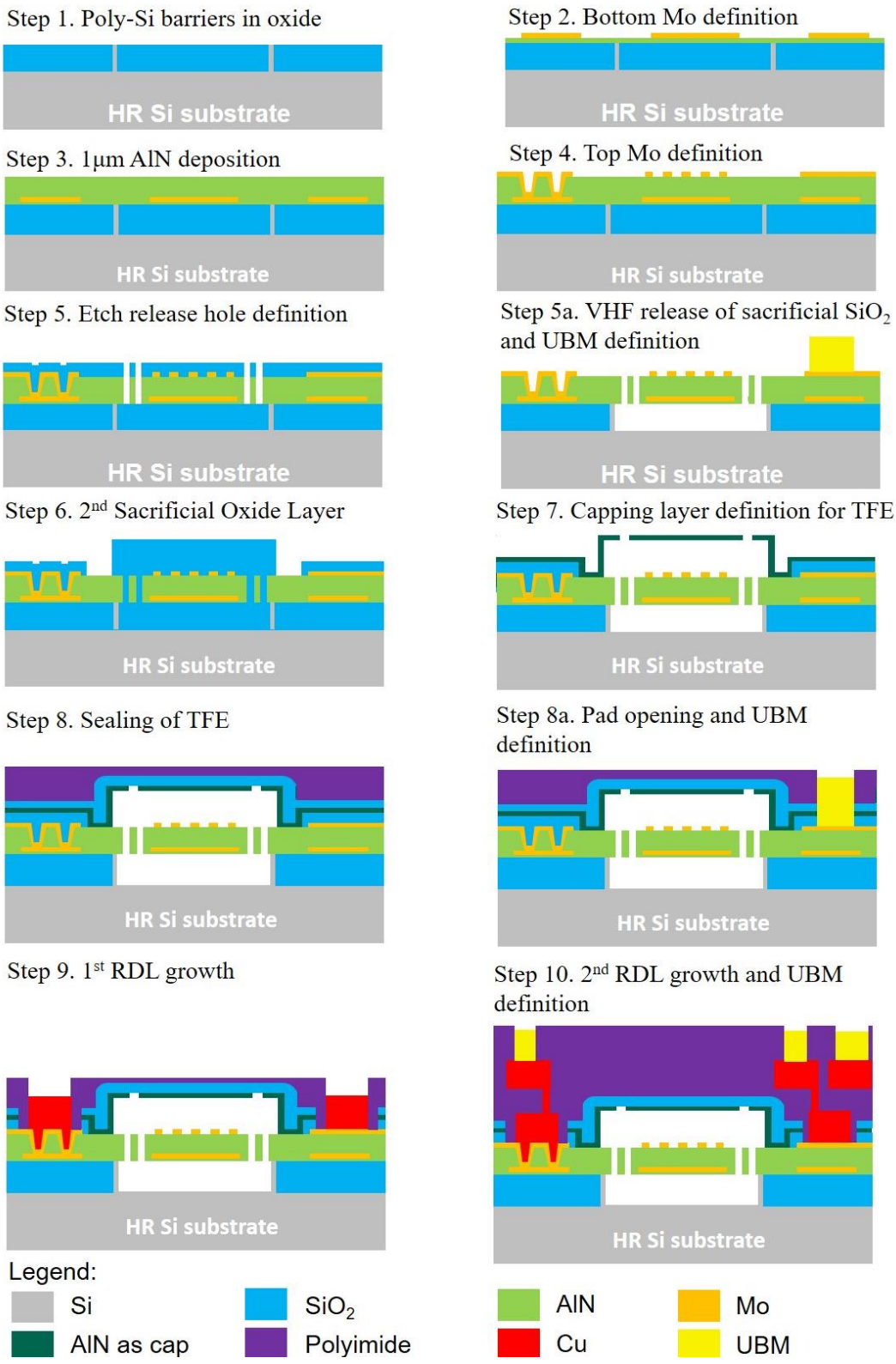


Figure 2-2. The developed fabrication process flow of AlN MEMS platform at A*STAR, IME, Singapore.

2.1.1 MEMS Fabrication

The MEMS fabrication starts with the deposition of a 3.5 μm thick PECVD SiO_2 on an 8" standard high-resistivity (HR) Si wafer. This oxide layer is later used as sacrificial material to release the device from the substrate. In order to isolate the released area, Si barriers of 2 μm width are defined inside the SiO_2 layer. This is done by deep trench etching of the oxide layer followed by Poly-Si filling using a low pressure chemical vapor deposition process. Then, excess Si is removed with a chemical mechanical planarization (CMP) step, which also minimizes the surface roughness of the oxide layer (*i.e.* Step 1). Next, the first layer of Molybdenum (Mo) in the amount of 150 nm is deposited on a 20 nm AlN seed layer, and then patterned to be used as bottom metal plate for AlN MEMS CMRs (*i.e.* Step 2). After the formation of bottom metal electrode, a 1 μm thick piezoelectric AlN is deposited to serve as the device layer (*i.e.* Step 3). Via holes to provide electrical connection between top and bottom Mo layers are defined in AlN with a Cl_2-based etch process. The second Mo layer of 150 nm is then deposited and patterned to define a set of top interdigitated electrodes for driving the resonators. The vias in AlN layer are also filled with Mo (*i.e.* Step 4). Note that this Mo layer is also used to make resonator interconnects to form the filters, which consist of three series cascaded AlN MEMS CMRs in this thesis. Then, the release holes are defined in the device layer AlN to be able to release the bottom sacrificial material lying underneath the resonator body (*i.e.* Step 5). The MEMS fabrication completes at this step as the sacrificial material is released after the encapsulation of AlN CMRs in the full process. In the MEMS only fabrication, though, the whole wafer is released by dry vaporized hydrofluoric acid (VHF) process at this step. If needed, a UBM can be also deposited and patterned before the release in order to ensure low contact resistance in the measurement I/O pads (*i.e.* Step 5.a).

2.1.2 TFE Fabrication

In the wafer level packaging process, the device is first capped with a thin-film before the release step. This allows the formation of a gap between the cap and the resonator, and thus

detaches the encapsulation layers from the suspended resonator body. Since the cap is an overarching structure on the resonator body, it also protects the resonator from possible contamination and damage in the following steps of the fabrication process. In order to make the capping layer, first a layer of SiO_2 is deposited on the MEMS device to form the top sacrificial layer and ultimately a gap between the cap and the suspended resonator body. After that, the SiO_2 layer is etched to define the anchor for the cap (*i.e.* Step 6). These anchors lie outside the release barriers defined in the MEMS only process in order to ensure sturdiness in the encapsulation after sacrificial material release. At the same time this layer also defines the release area on top of the resonator. In other words, the anchor surrounds the sacrificial release layer on top of the resonator body and the trenches forming the anchor act as etch stop barriers for the top oxide. The concept is similar to the initial silicon etch stop barrier in the MEMS fabrication, except that now the process isolates the top sacrificial material instead of the bottom one underneath the resonator body. After the formation of capping layer (a form of AlN) is completed with the definition of the capping release holes, all the devices on the wafer are simultaneously released by dry VHF (*i.e.* Step 7). With the etch stop barriers surrounding top and bottom sacrificial material, devices with different dimensions can be fully released without the concern of undercutting huge area under the pads and interconnects. From the design standpoint, this is very important since the effective anchor of the resonator can be predicted accurately and thus devices could be densely populated over the entire mask as much as the system permits. After the release, the wafer is coated with a dielectric to seal the openings in the capping layer formed for sacrificial material release. The release holes in the capping layer are placed in such a way that any material that might deposit inside the capping layer during the sealing process would go in regions that do not impact the device performance. In any case, in order to restrict the amount of dielectric over such areas, these holes are designed to be quite small so that they are rapidly sealed during the deposition of sealing layer SiO_2. Since the top Mo is now below a dielectric material, vias are defined through the seal and the cap layer at the locations of signal interconnects. Then, a layer

of photo-definable packaging polyimide is spin coated and cured on the sealed MEMS wafer. A final thickness of 5-7 μm is aimed in this polyimide layer after the curing process. The polyimide spin parameters are optimized so as to attain the desired thick levels after the curing process. The commercial grade wafer-level coating of polyimide is used to enhance the mechanical and chemical robustness of the overall MEMS wafer. With the deposition of the polyimide, TFE process completes (*i.e.* Step 8). To test the devices at this stage, openings should be formed around the pads. Similar to the MEMS only fabrication, UBM can be deposited on top of the pads to lower the contact resistance and make the pads more readily accessible (*i.e.* Step 8.a).

2.1.3 RDL Fabrication

RDL fabrication starts with via openings in the first polyimide layer which is already deposited as the last step of TFE fabrication. These via openings provide the electrical connection between the first re-distribution metal layer and top Mo. Then, a 3 μm thick copper (Cu) is deposited and patterned as first signal re-routing layer in the platform (*i.e.* Step 9). Next, another set of polyimide and Cu is deposited and patterned to form the second signal routing layer. After also covering this second Cu layer with polyimide, pad openings are defined and a standard commercial 3 μm thick UBM (i.e. Cu/Ni/Au) is deposited and patterned with lift-off process to facilitate flip chip solder-bump bonding from these MEMS chips to the CMOS chips. The polyimide layers in each step provide natural planarization for the platform and smoothen the overall wafer topography. After dicing the wafer into reticle-size chips and further sub-dicing these chips to get individual MEMS dies, the full AlN MEMS fabrication process completes (*i.e.* Step 10). Since there is no additional dielectric material deposition as a passivation layer after UBM deposition, use of the UBM layer for signal routing should be kept minimal in order both to ensure no short circuits in bonds during solder bump re-flow process, as well as, to extend the life-time of the MEMS chips by means of limiting the amount of metal exposed to air and external contaminants.

2.2 Design of AlN MEMS CMRs for Filter and Transformer Applications

2.2.1 AlN MEMS Resonator Design Considerations

In order to ensure the deployment of AlN MEMS CMRs in system level applications, it is important to attain high Q, high k_t^2 and thus high FoM, and simultaneously understand the origin of spurious modes (SM) to reduce ripple in the filter passband. Additionally, these resonators should be a specific size enough to directly match to 50 Ω termination as required by the system specs and can be readily fabricated with high device yield and reliability. Namely, the sacrificial material should be fully released in the area defined by the etch-stop barriers without causing any thin-film breaking after release even if large device sizes are required. Since we also aim for mass production in an 8" fab line, the processing time for each step should be reasonably short to reduce the cost of the fabrication. That is why we should also limit the amount of lateral release required for making the resonator body fully suspended. Because the location and size of release holes in the AlN layer set the amount of lateral etch needed in the sacrificial material, these release holes should be placed optimally considering both the FoM of the resonators and the amount of time required to complete the release.

2.2.2 DoE for MEMS only AlN resonators

To address all these challenges in the resonator design, we made a design of experiments (DoE) on MEMS only resonators in order to optimally choose the resonator geometry to be used in RF filter applications. We systematically studied the impact of resonator geometry and anchoring on Q, k_t^2, FoM and SM for 1.22 GHz resonators. Considering the material stack and thicknesses provided in Chapter 2.1, a P of 4 μm is used in the placement of top metal electrodes for frequency setting, and this parameter is kept constant for all the studied resonator geometries.

2.2.2.1 Design Variations

A total of 135 resonator variations are studied for four geometrical parameters that have previously shown to be critical in the performance of AlN MEMS CMRs. Among these are anchor of active resonator area, overhang extension (*OE*), top metal finger length (*FL*) and top metal finger number (*FN*) [20], [21].

The anchor here is described as formed by the tethers defined by etching the release holes in the AlN device layer, and thus acts as the supporting points for the resonator active area from the transverse sides. Since the anchor is defined by the device layer AlN release holes, the shape of it plays a critical role in the amount of lateral release needed for each device to make the resonator body fully suspended. Distribution of these holes across the width of the devices fixes the amount of lateral release needed for the devices with the same *FL* as *FN* increases. Thereby, distribution of etch release holes across the device width is more preferred from the standpoint of the amount of lateral release considering the large resonator sizes to match 50 Ω systems in the filters. Also, distributed etch release holes limit the amount of AlN deflection along device width due to AlN thin-film stress after the release and thus, significantly reduce the chances of device breaking during the fabrication and while handling the chips.

In this DoE run, we have five different variations for anchoring options as described by the scanning electron microscope (SEM) images given in Figure 2-3 a-e. Basically, we study the impact of anchor types with the distributed etch release holes across the device width (i.e. Figure 2-3 d-e) on the critical resonator parameters such *Q*, k_t^2 and *FoM* and location of SMs in comparison with more conventional anchor types for these types of resonators (i.e. Figure 2-3 a-c) [22]. The width of all the etch release holes are set to be 2 μm and unified among all the devices for their uniform sidewall definition across the whole wafer. The length, however, is set to 12 μm for the distributed etch release holes with 12 μm spaces (minimum design rules provided by A*STAR, IME, Singapore for targeted sidewall angles in the device layer AlN) whereas in the other

anchor types it is adjusted to ensure that the anchor width is in increments of λ/4 in order to limit the *Q* dependence on the inactive regions as discussed in [23].

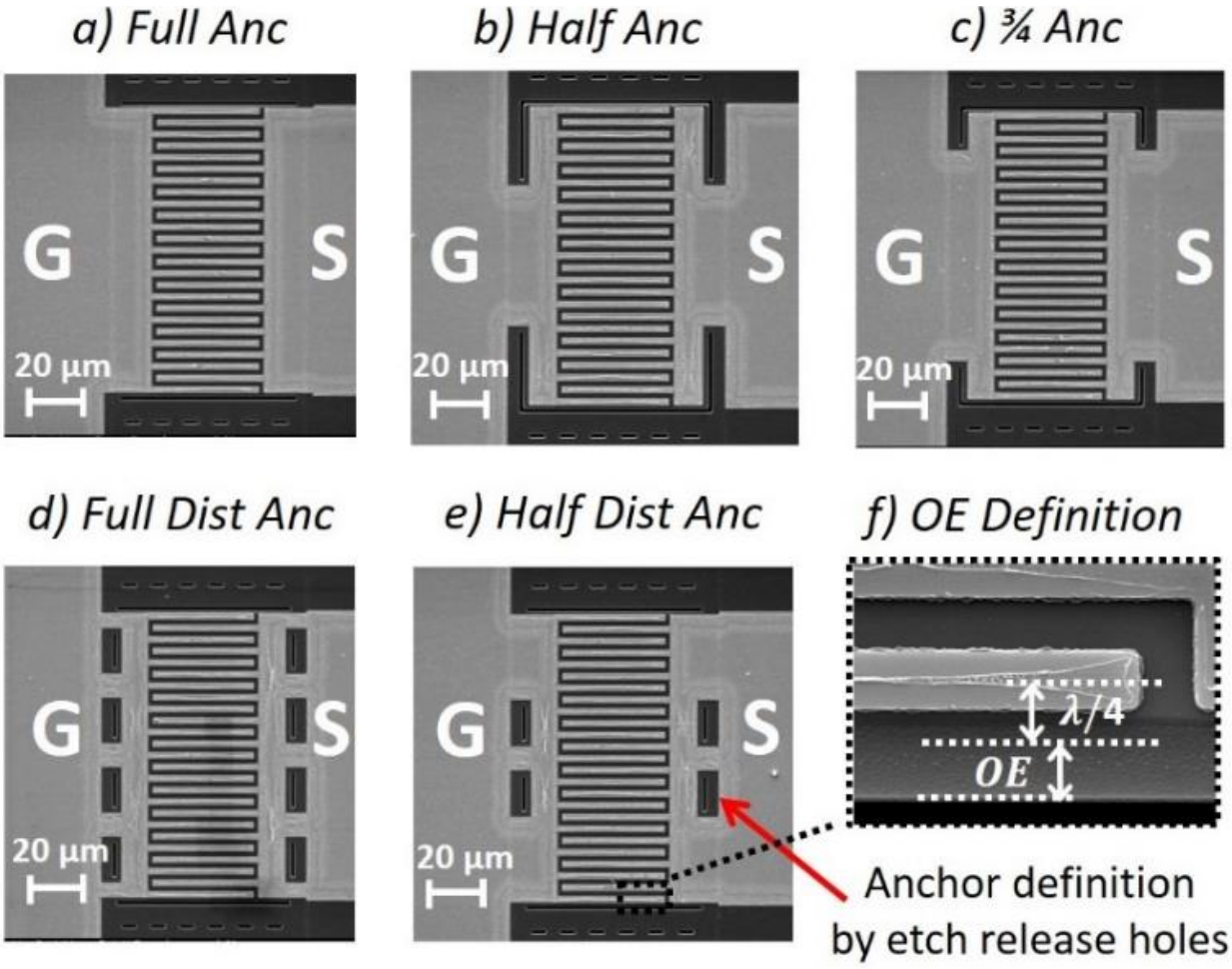


Figure 2-3. SEM images of studied anchor types and *OE* definition. a) *Full Anc*: Full anchor with no side release holes, b) *Half Anc*: Centralized anchor sized as half of the device width with corner etch release holes, c) *¾ Anc*: Centralized anchor sized as ¾ of the device width with corner etch release holes, d) *Full Dist Anc*: Anchor with distributed etch release holes across the full device width and e) *Half Dist Anc*: Anchor with distributed etch release holes across the half device width at the center. f) Definition of design parameter, *OE*. Note that each distributed etch release hole has width and spacing of 12 µm. The symbols "G" and "S" on the figures a-e stand for ground and signal electrical connections of the resonators, respectively. The symbol λ stands for the wavelength of the signal at f_o, i.e. twice the value of parameter, *P*.

We define *OE* as the amount of AlN film that extends beyond the regular size of a resonant cavity (see Figure 2-3.f), which has been previously used for fine frequency shift in resonators as described in [24]. On the other hand, *FN* and *FL* are used to set the characteristic impedance of the device based on the application [4]. Three different variations are used for both *FN* and *FL*. For *FL*, the minimum size (40 μm) is limited by the device active/non-active regions ratio for a reasonable *Q* due to anchor losses [25] whereas the maximum (100 μm) is limited by the fabrication process rules (as to ensure device flatness given a certain residual stress). For *FN*, the maximum value (75) is limited by the maximum release length that the fabrication process can accommodate. There is no limitation for the minimum value, but we set it to be 25 to ensure operation with an impedance that can be easily matched to 50 Ω with a few devices of the same size connected in parallel. Table 2.1 details all the parameters that were varied in this study.

Table 2.1. Studied geometrical parameters for AlN MEMS CMRs and their variations.

Parameter Name	**Parameter Variations**
Anchor Type	*Full Anc, Half Anc, ¾ Anc, Full Dist Anc, Half Dist Anc**
Overhang Extension (*OE*)	0, +1/8, +1/4 λ
Finger Number (*FN*)	25, 51, 75
Finger Length (*FL*)	40, 70, 100 μm

**The descriptions for each of the abbreviations used for anchor types are provided in Figure 2-3.*

2.2.2.2 Experimental Results and Data Analysis

All the resonator data in this subsection are collected on MEMS only devices without the presence of TFE and RDL. SEM images of some of the fabricated AlN CMRs are already shown in Figure 2-3. All the measurement data were taken on a single die. The inter-die variation data for A*STAR, IME process is provided later in Chapter 3.1.

The fabricated resonators were tested using an Agilent 5230A vector network analyzer under atmospheric pressure after standard one-port parameter calibration performed using short-open-load structures on a proper ceramic substrate. S-parameter data are then converted into admittance parameters using conversion equations. Measured pad and trace parasitics were also de-embedded using on-chip de-embedding structures. Q and k_t^2 values for each resonator were extracted from the admittance data using the equations provided in [25]. This methodology in testing applies to all the resonator and filter data provided in this thesis. Two-port calibration (short-open-load-thru) is used wherever two-port devices are being measured.

In the measurements, an unloaded Q of up to 3157, a k_t^2 of up to 2.3%, and a *FoM* of up to 61.6 were achieved in various resonator geometries. In order to better understand data and extrapolate trends, we study the change in Q, k_t^2 and *FoM* for all the various anchor types with respect to either *FL*, *FN* or *OE* while keeping the other two parameters constant. Since there are many variations, only a fraction of the most relevant ones are plotted in this paper (Figure 2-4).

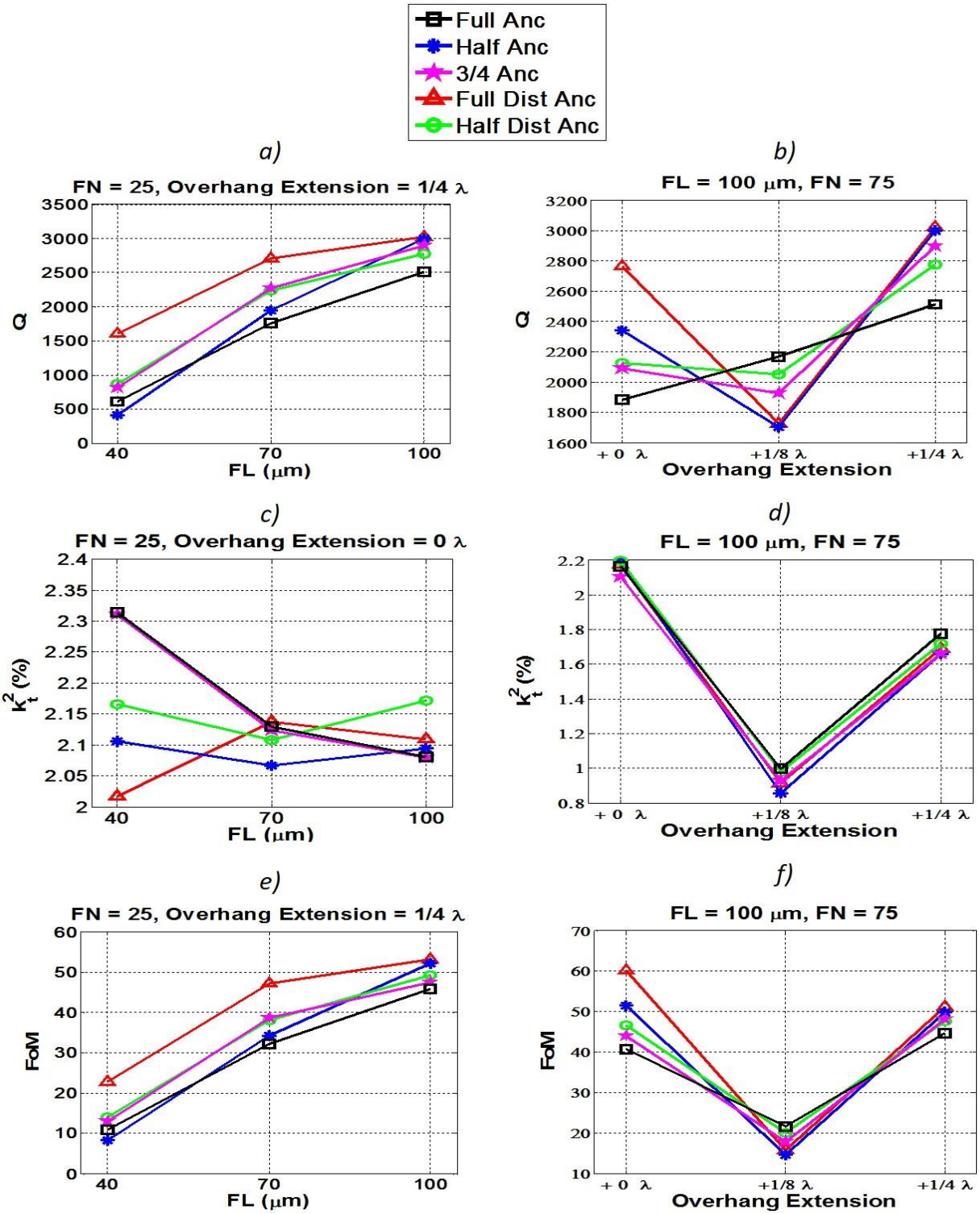


Figure 2-4. Effect of design variations on extracted Q, k_t^2 and *FoM* of AlN MEMS CMRs. In each sub-figure, either Q, k_t^2 or *FoM* is plotted for all the various anchor types with respect to either *FL*, *FN* or *OE* by keeping the other two parameters constant. We only provide the most relevant trends.

Based on the collected data we can conclude that:

- *Q* increases with *FL,* but for higher values of *FL* this increase gets limited most likely because of thermo-elastic damping (TED) in the metal electrodes as explained in [25]. Among the anchor types, *Full Dist Anc* exhibits the highest *Q* in all cases except for *OE* of 1/8 λ. The difference between anchor types becomes less obvious when *FL* increases (see Figure 2-4 a-b). This observation is in-line with outcomes of [20] that past a certain *FL* value anchor losses are not dominant in high frequency AlN MEMS CMRs.

- The resonators exhibit the minimum *Q* for *OE* of 1/8 λ except for the full anchor type. We believe that an *OE* of 1/8 λ results in an overall resonator cavity that is 1/4 λ longer, hence creating undesired reflections that alter the resonator mode shape and hence its losses through the anchors.

- The *FN* does not have a significant impact on *Q*.

- The dominant parameter affecting the device k_t^2 is the *OE* (see Figure 2-4 c-d). k_t^2 is minimum for *OE* of 1/8 λ. We believe that this is again due to the reflections from the edges, which permit the excitation of other lateral modes (symmetric modes) of vibrations, hence impeding to have all the energy coupled into the main desired mode of vibration. Also as *FN* increases, the k_t^2 decreases while the amplitude of SM increases. This change could be explained by the size of the resonator cavity, which strengthens the motion of modes in the out-of-plane direction (anti-symmetric modes). For most of the cases, *FL* has a negligible impact on k_t^2. As for the anchor type, it has a small impact on $k_t^2$and becomes negligible as *FL* and *FN* increase.

- The device *FoM* follows the combined trends of k_t^2 and *Q*. *FL* and *OE* have the utmost impact on the value of *FoM*. It is important to note that the *FoM* can vary by more than 4x depending on the specific design variation.

As for the relative location and amplitude of the SMs, it is observed that the amplitude of SM mostly follows the amplitude of the main mode of vibration. So, the amplitude of SM is higher whenever the *FoM* is higher. The location of SMs, though, primarily depend on *OE* and *FN*. According to Figure 2-5 and Figure 2-6, the separation between the SM and the main mode of resonance could be adjusted using either the *OE* or *FN*. This observation suggests that for the studied resonator geometries SMs in the transverse direction are not critical. Based on our observations on all the data, a reasonable amount of separation between the main mode and spurs might need a change in both of these parameters, *i.e.* *OE* and/or *FN*. *FL* and anchor type have unnoticeable impact on the location of any SMs in the studied geometries.

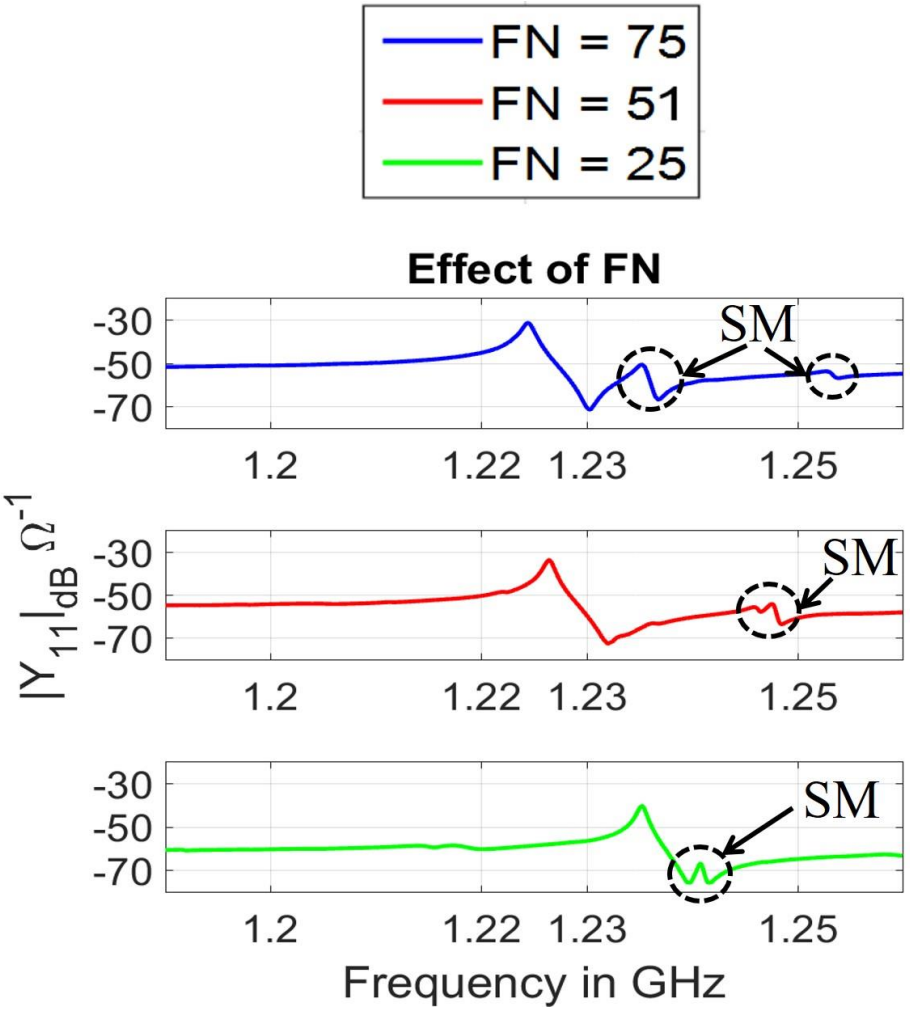


Figure 2-5. SM location change by *FN* with *OE* of 1/4 λ, *FL* of 40 µm with *Full Dist Anc*.

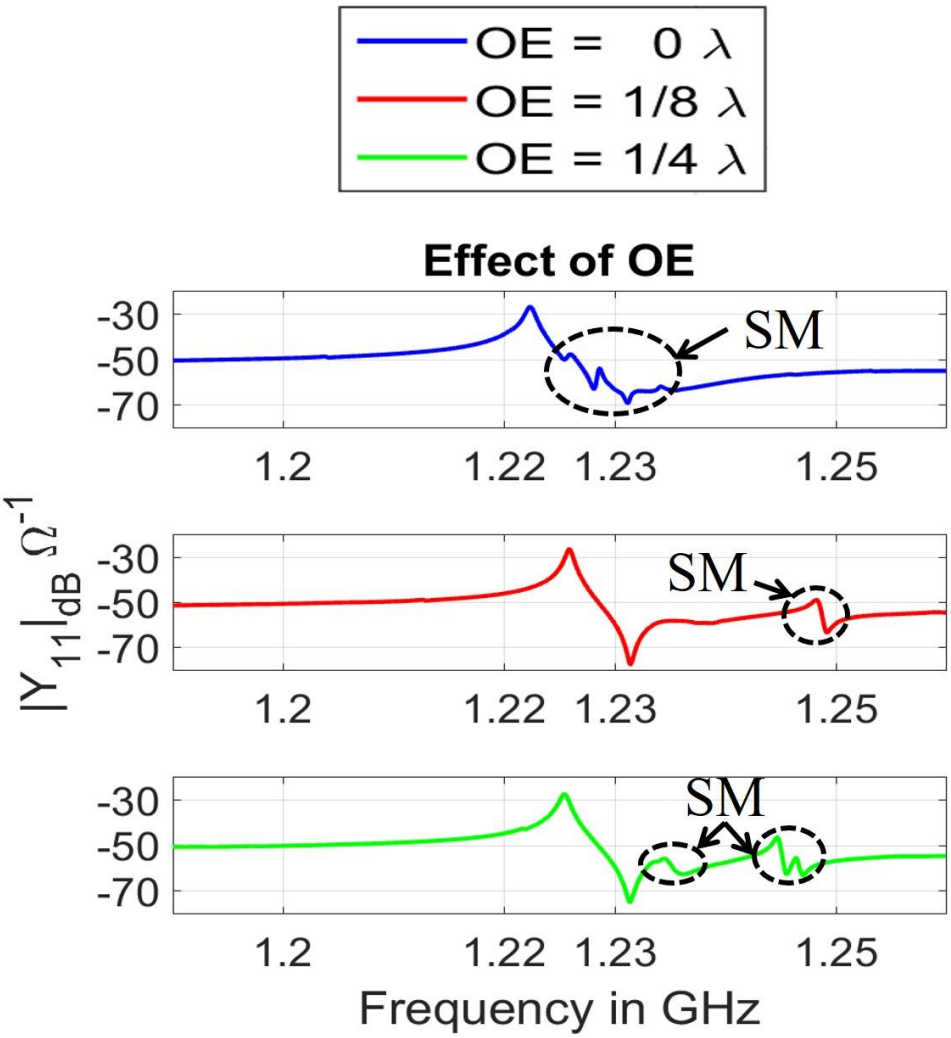
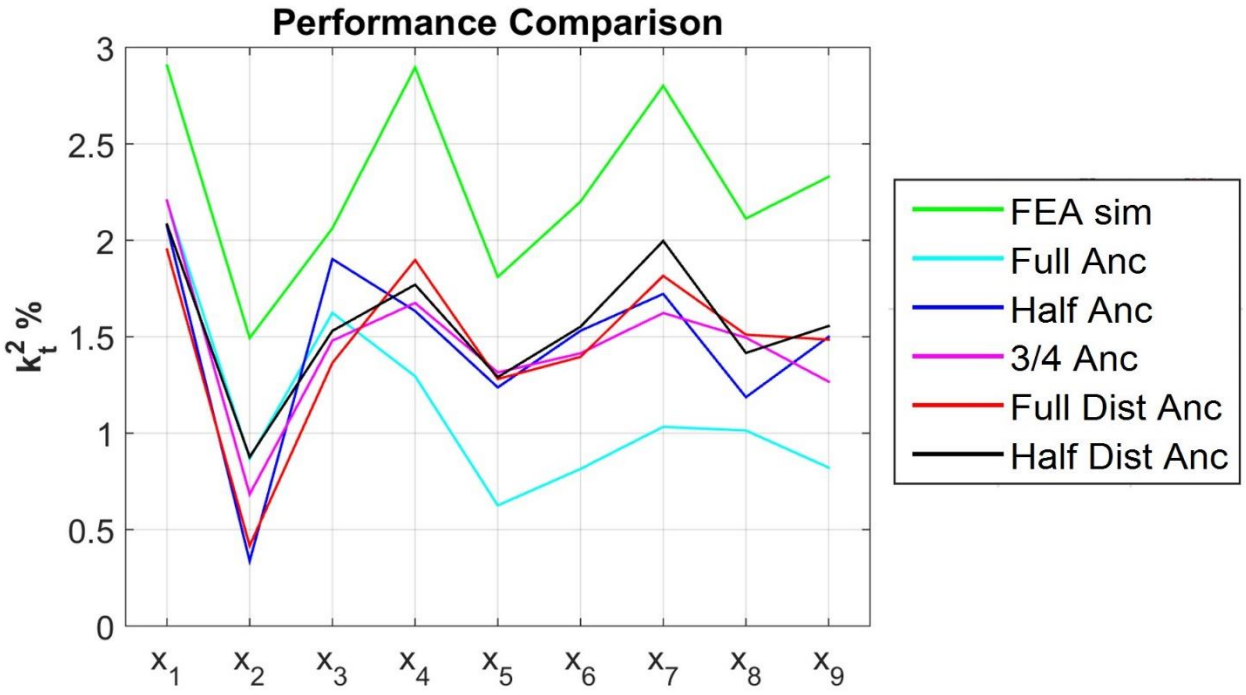


Figure 2-6. SM location change by *OE* with *FN* of 51, *FL* of 70 μm with *Full Dist Anc*.

We also confirm the experimental trend exhibited by the k_t^2 via finite element analysis (FEA). The material stack and thicknesses provided in Chapter 2.1 are used to create the models for the FEA simulations. Since k_t^2 is not significantly affected by *FL* and anchor type, we performed 2D FEA. The model includes the cross-section of the resonator body along with metallic interdigitated transducers/electrodes (IDTs) and bottom electrode. As seen from Figure 2-7 the simulation follows the trends of experimental data for all the anchor types except for the last item of *Full Anc* and *¾ Anc*. The last item among data points (*i.e.* x_9 on Figure 2-7) have the largest resonator cavity size whereas *Full Anc* and *¾ Anc* are the longest among the anchor selections. Thus, the

deflections in the resonator body due to residual stress are likely to be high for these particular variations and this could indeed lower k_t^2. The level of deflection in AlN thin film could also explain the numerical deviations among the simulated and experimental values for k_t^2 together with fabrication-induced process variations, defects in the device AlN thin film, and fringing electric fields from tip of the metallic IDTs towards interconnect buses.



Parameter	x_1	x_2	x_3	x_4	x_5	x_6	x_7	x_8	x_9
FN	25	25	25	51	51	51	75	75	75
***OE* (λ)**	0	1/8	1/4	0	1/8	1/4	0	1/8	1/4

Figure 2-7. k_t^2 comparison between 2D FEA simulation data and experimental data extracted for all the studied anchor types. *FL* is 40 µm for the experimental data. The legend for the data points on the x axis is provided in a table located at the bottom of the plot.

As concluding remarks, we can state that for large values of *FL* the distributed etch release holes in the definition of anchor for resonator body can be employed in the AlN MEMS CMR and filter designs without any degradation in *FoM*. Also, *FN*, *OE* or both need to be employed in resonator designs in order to push SMs away from bandwidths of interest and maintain a high *FoM* as the studied geometries are found to have no spurious mode coming from the transverse side.

2.3 Development of TFE for AlN MEMS CMRs

In order to protect suspended structures during flip-chip bonding process and provide hermetic seal to the environmental conditions, encapsulation of the AlN MEMS CMRs is needed.

2.3.1 TFE Structure

In the AlN MEMS platform, a novel wafer-level packaging technology is utilized that enables individual or group packaging of resonators and filters. It is aimed to achieve cost effective MEMS integration technology with a compact footprint.

The TFE of AlN CMRs contains two major layers that serve two distinct purposes. The first one is a thin layer that caps the entire moving resonator body. It is the overarching structure on the suspended devices with the anchors lying outside the suspended area. This layer has holes in it to let us later reach and release the sacrificial materials both on top and bottom of the device to make the resonator body fully suspended. A second layer is used to hermetically seal these holes in the cap after the release. This layer also includes thick polyimide to provide for additional structural rigidity and an overall smoothened topography across the wafer.

2.3.2 Fabrication Challenges

The main challenge in the development of TFE for AlN CMRs is to ensure the control of the stress levels in the thin films to minimize bending of the capping layer. The level to which the

stress can be controlled poses limitations on the device size and aspect ratio and effectively constrains the device optimization. The materials for the cap and seal also have to be compatible with the device operation at RF and should minimize signal feedthrough [26].

Several sources of failures were encountered during the development of TFE, such as insufficient release of sacrificial material, breaking of thin films, downward buckling of the capping layer and/or upward buckling of device layer AlN causing the cap to touch the resonator body. To address these challenges, the etch release holes in both device layer AlN and capping layer were made as small as possible and distributed as uniformly as possible without interfering with the resonator active area. Also, these two sets of etch release holes should not be overlapped in order to ensure minimal topography in the capping layer, and thus higher structural rigidity. Additionally, the thickness of the sacrificial material should ensure limited stress in thin-film encapsulation and also full detachment from the resonator body after its release. In order to set the thicknesses of sacrificial layer and material stack in the capping layer a DoE run is performed by A*STAR, IME, Singapore on the thin-film packaged AlN MEMS CMRs and filters.

2.3.3 TFE Fabrication

The results of the DoE run performed by A*STAR, IME, Singapore in the development of TFE shows that in order to increase the resilience of the capping layer in TFE and enhance yield in the devices, a material stack instead of only AlN needs to be deposited. The thicknesses of layers in the material stack with respect to capping layer AlN is kept small in order not to interfere with the wave propagation [27]. Another outcome of the study is that the sacrificial oxide layer should be made 3 μm thick in order to ensure full detachment from the resonator body after the release.

Additionally, as a result of the DoE run, two other design rules related to the TFE layers are set by A*STAR, IME, Singapore, which put constraints on the maximum device size and density. First, the distance between capping layer holes should be less than 110 μm to ensure full release of the sacrificial material. Second, the capping layer anchor width should be as minimum as 10

μm in width (this number should be 20 μm if anchor is shared between devices) to ensure a successful packaging of AlN MEMS resonators and filters.

The SEM images of successfully developed TFE for AlN MEMS CMRs and filters are shown in Figure 2-8. The encapsulated devices are reported to survive post CMOS assembly processes such as wafer level dicing and flip chip bonding (experimental testing results are shown in Chapter 3.2). Electrical test results at RF are provided in Chapter 2.6, which show that the TFE yielded functional devices after the encapsulation. Both fabrication outcome and measurement results indicate high possibility of cost effective MEMS integration technology within a very small footprint [28].

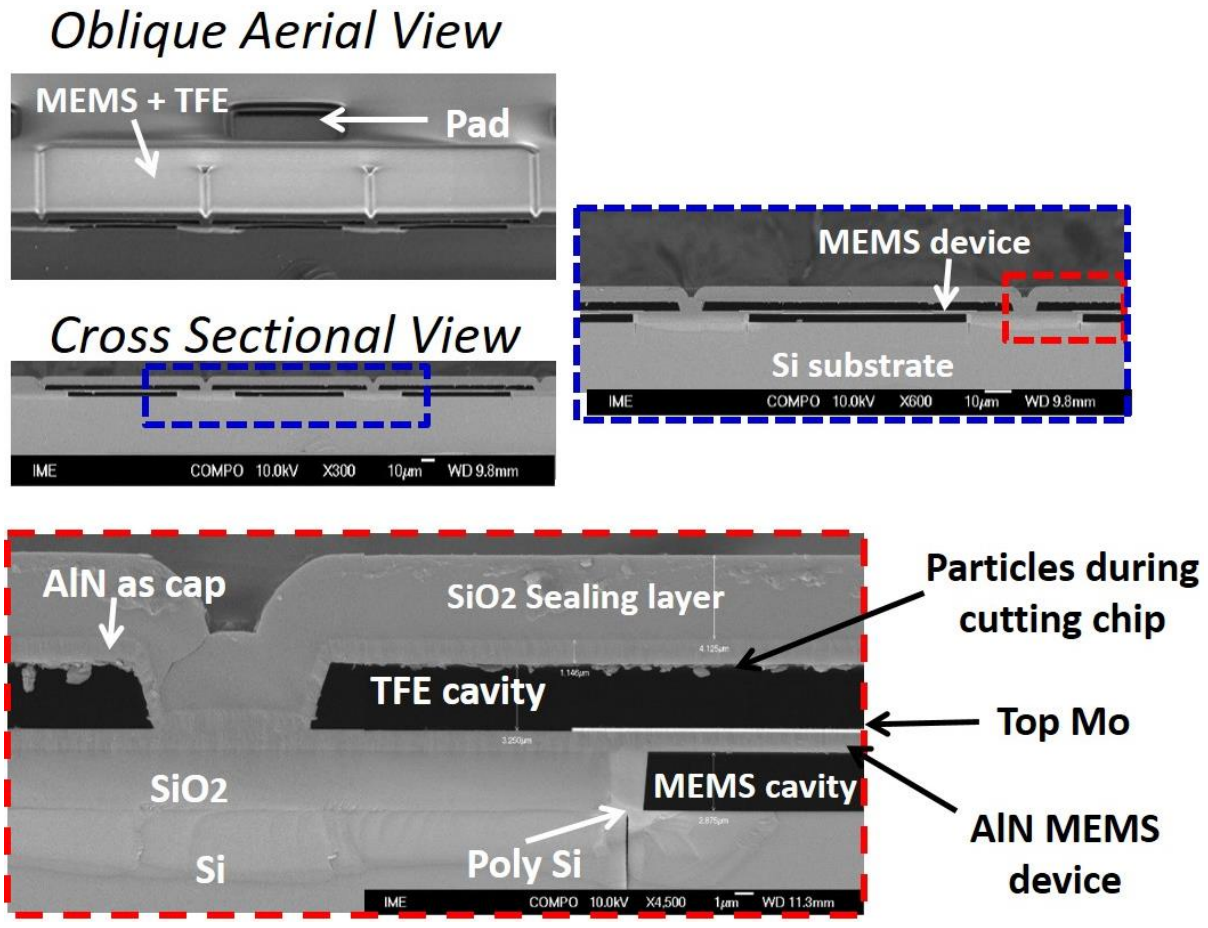


Figure 2-8. Oblique aerial and cross-sectional views of TFE for AlN MEMS CMRs thru SEM imagining (a courtesy of A*STAR, IME, Singapore).

2.4 Development of RDL on AlN MEMS Platform for Efficient 3D Hybrid Integration with CMOS Circuits

Developing low loss RDL on MEMS chips offers solutions to the issues associated with RF routing on CMOS as mentioned in Chapter 1.3, although it increases the overall fabrication complexity of the AlN MEMS platform. Here we discuss the structure of RDL and provide design of experiment test structures designed to determine the thicknesses of the material stack and model electrical characteristics of metallization layers used for signal routing.

2.4.1 RDL Structure

Our goal in RDL development is to ensure low loss and low parasitics metallization for signal interconnects and routing on AlN MEMS platform with limited additional fabrication complexity. This, in turn, helps us utilize the full potential of AlN MEMS CMRs as building blocks in the RF front-end applications, as well as, efficiently use the CMOS chips.

In addition to UBM, RDL includes two metal layers to ensure enough flexibility in routing for the 3D integrated systems. It is preferred that we do not use UBM layer in signal routing except for measurement I/O and bond pads because of two reasons. First, we do not want to jeopardize CMOS-MEMS integration by means of short circuits during solder bump re-flow process during flip-chip bonding. Second, we want to limit the amount of metal lines exposed to air oxidization as there is no dielectric passivation layer deposition after the UBM traces are defined.

2.4.2 DoE for Metallization Layers and Inter-metal Dielectrics

The development of RDL mostly consists of setting the right amount of thicknesses for metal layers and inter-metal dielectrics with the goal of minimizing the resistive losses and capacitive and inductive parasitics associated with routing of arrayed devices and circuits. In the meantime, we should also minimize the fabrication complexity and issues by means of keeping the thicknesses of these metal and dielectric layers as minimum as possible.

In this respect, we ran some FEA simulations to understand the needs for thicknesses of the material stack in RDL and made a DoE fabrication run on a variety of test structures for verification. In the DoE run, HR Si wafer with thick SiO_2 is used as the starting wafer as in the AlN device fabrication, but now we have only the top Mo layer with polyimide and no other MEMS or TFE layers. This DoE run also helps us model the capacitive, resistive and inductive characteristics of each RD metal layer and via interconnect. The model includes overlapping, non-overlapping and feed-thru capacitances for most of the possible combinations as well as sheet resistances and inductances of all metal layers and inter-metal vias. In order to de-embed any contact resistance in the test structures and improve modeling accuracy, we designed the I/O pads of resistive structures to be compatible with 4–point probe measurement techniques as suggested in [29], [30]. For test structures that model capacitive and inductive behaviors of RD layers, we designed three different lengths of the same shape in order to make recursive least square fitting [31] to increase accuracy in the parameter extraction. Some of the test structures drawn for the characterization and modeling of RDL are shown in Figure 2-9.

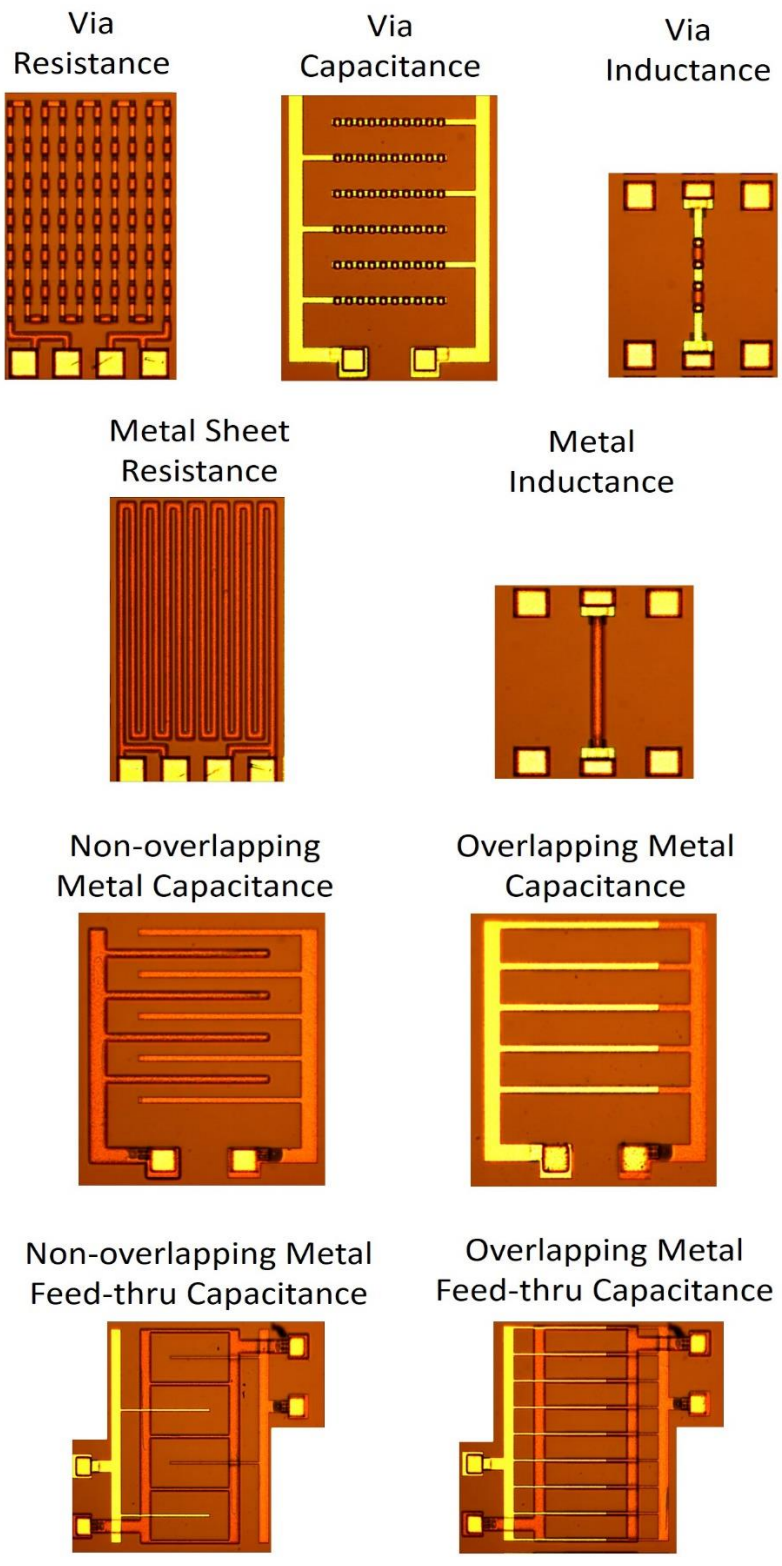


Figure 2-9. Optical images of a subset of test structures used in the characterization and modeling of RDL only fabrication.

2.4.3 DoE Results and Electrical Modeling of RDLs

For DoE run, RDL only material stack with a Mo layer was fabricated on a SiO_2/Si substrate by A*STAR, IME, Singapore. Here Mo layer represents the top Mo in the full process AlN MEMS platform (see Figure 2-1). A cross-sectional SEM image after laser FIB-cut on a sample of a successful RDL-only stack can be found in Figure 2-10. The routing metal layer (Cu) thicknesses are 3 μm whereas polyimide is about 5-7 μm thick each in this process. Since the polyimide layers also provide natural planarization for the platform, its thickness is lower around the metal strip lines when they overlap.

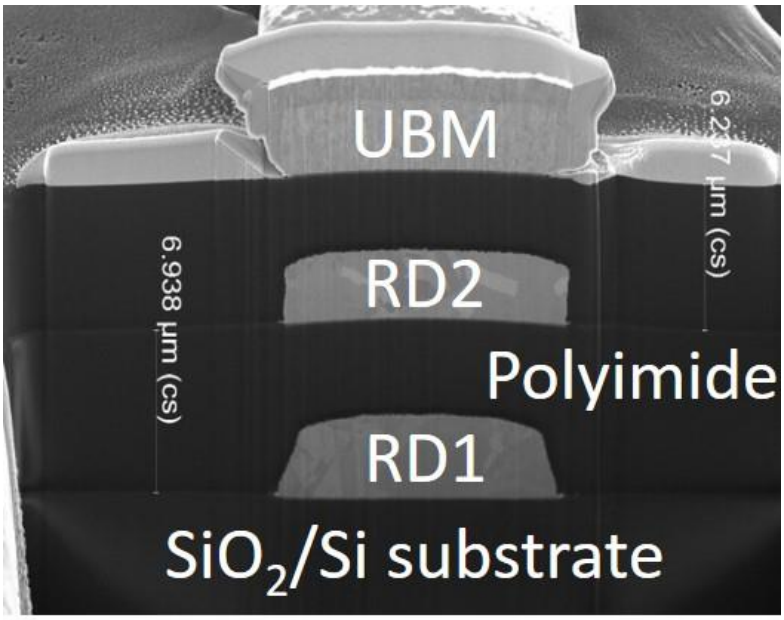
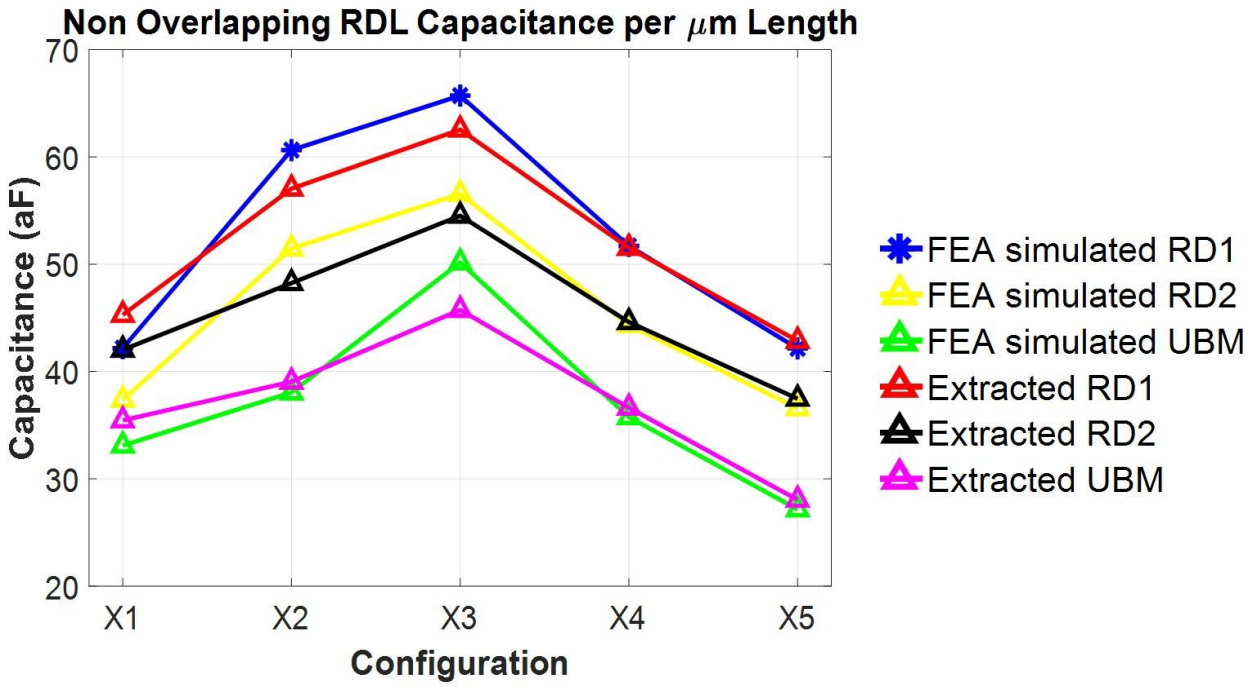


Figure 2-10. A cross-sectional SEM image of RDL only fabrication after a laser FIB-cut (a courtesy of A*STAR, IME, Singapore).

In general, measurement results are in good agreement with 2D FEA simulation results. A sample extraction set in comparison with 2D FEA simulated performance can be found in Figure 2-11. The full list of extracted properties of the RDL layers is provided in Table 2.2, Table 2.3 and Table 2.4. These properties are used to model the impact of signal routing on the filter

performance when making the MEMS layout design for CMOS integration. The beneficial effects of RDL routing are further showcased in Chapter 3.2.3.



Test Structure Configurations					
	x_1	x_2	x_3	x_4	x_5
Width of Lines (μm)	25	25	25	51	51
Separation of Lines (μm)	0	1/8	1/4	0	1/8

Figure 2-11. Non-overlapping metal capacitance test structure measurements from RDL only DoE run in comparison with those acquired from 2D FEA simulations of the same geometries with the same material stack.

Table 2.2. Electrical characteristics of RDL metal layers extracted from RDL DoE measurements.

	RD 1	***RD 2***	***UBM***
Sheet Resistance (mΩ/□)	5.17	5.67	5.44
Sheet Inductance (pH/μm)	0.768	0.558	0.550

"RD x" stands for metal layers in RDL. Each metal line is 20 μm wide in these structures. Capacitance extraction for RDL metal layers are made in a more detailed way and provided in Table 2.4.

Table 2.3. Electrical characteristics of RDL via interconnects extracted from RDL DoE measurements.

	Via 1	***Via 2***	***Via 3***
Resistance (mΩ/per via)	92.7	4.95	6.72
Inductance (pH/per via)	8.72	26.5	50.3
Capacitance (fF/per via)	0.32	0.27	0.22

"Via x" represents the corresponding via interconnects from Top Mo to RD x to UBM. The numbers increase from bottom to top in the cross-sectional view. In the extractions, the enclosing top and bottom metals are also included in the corresponding via models. For via capacitance the separation is set to be 100 μm. Via 2 and Via 3 are 10 μm x 10 μm whereas Via 1 was 20 μm x 20 μm. These via sizes are unified across the whole reticle among themselves.

Table 2.4. Non-overlapping, overlapping and feed-thru capacitance extraction for RDL metal layers per μm length.

		Capacitance (aF/μm)				
Test Configuration		***X1***	***X2***	***X3***	***X4***	***X5***
Non-overlapping	**RD1 – RD1**	45.28	57.04	62.54	51.52	42.86
	RD2 – RD2	42.03	48.24	54.52	44.61	37.47
	UBM-UBM	35.45	39.05	45.74	36.63	28.05
	RD1 – RD2	41.11	48.90	54.13	32.72	36.57
	RD2 – UBM	35.97	40.75	47.50	38.29	31.71
	RD1 – UBM	39.97	46.90	48.56	43.93	36.99

		Capacitance (aF/μm)				
Test Configuration		***X1***	***X2***	***X3***	***X4***	***X5***
Overlapping	**RD1 – RD2**	193.9	182.2	296.1	184.5	127.3
	RD2 – UBM	194.5	187.4	312.6	186.6	121.8
	RD1 – UBM	96.2	94.8	169.8	95.6	66.1
Feed-thru	**Non-Overlapping**	4.72	*	12.4	10.4	9.53
	Overlapping	115.8	*	142.7	116.4	100.9

*Description for X1-X5 is provided in the table in Figure 2-11. "RD x" stands for metal layers in RDL. *Because of lack of space on the mask the corresponding test structures were excluded.*

2.5 Accelerated Hermeticity Tests of a full process AlN MEMS CMR

In order to validate the hermeticity of the TFE for AlN MEMS CMRs in the developed full process AlN MEMS platform, we built a Pierce oscillator using one of the fabricated AlN MEMS resonators and monitored its frequency of oscillation through a frequency counter.

2.5.1 Making the Pierce Oscillator

The equations and design constraints for making the Pierce oscillator using AlN MEMS CMRs can be found in [32]. In order to easily start oscillations, we used a relatively large resonator (*FN* of 65, *FL* of 84 μm, *OE* of 0 μm, and anchor with a single side etch release hole). We had copies of the same resonator geometry on the same chip in close vicinity. This way, we can compare the performances of electrically active (used to make the oscillator) and electrically inactive resonators (no electrical connection made during the hermeticity tests) after the hermeticity tests. The schematic of the circuit for making the Pierce oscillator using AlN CMRs as resonant elements is shown in Figure 2-12. The selected parameter values are also shown on the same figure.

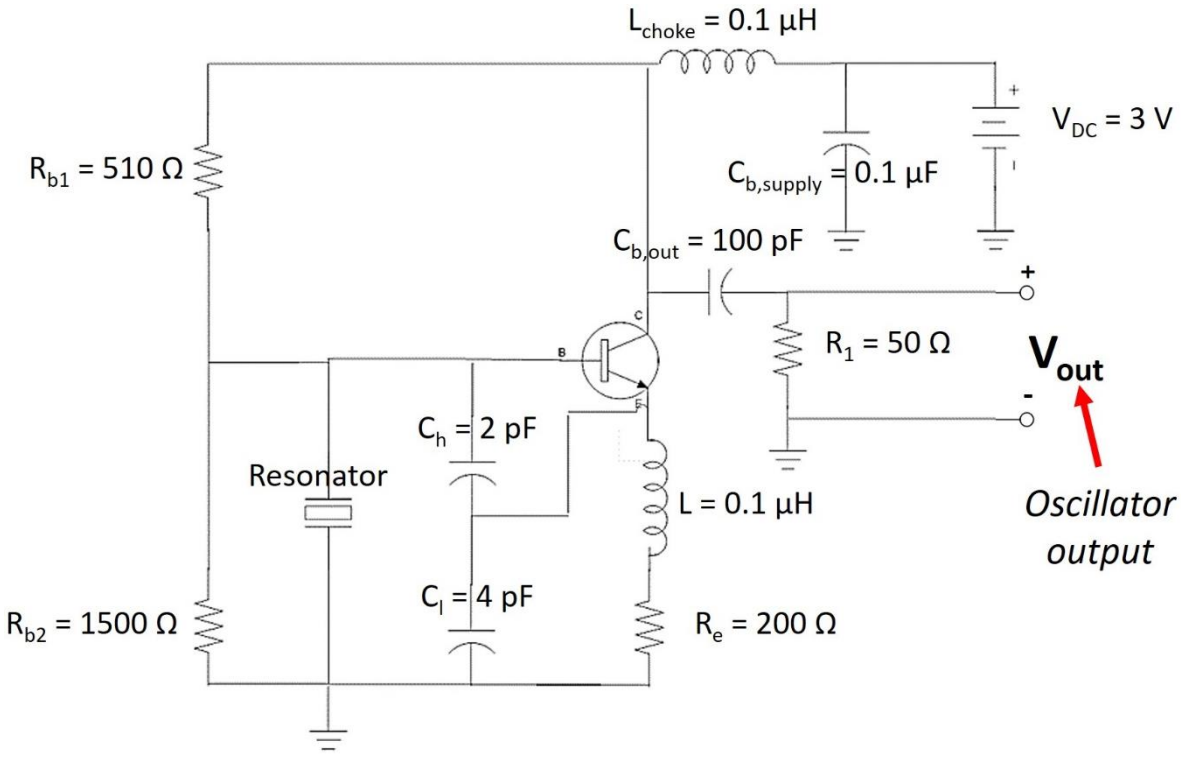


Figure 2-12. Circuit diagram for the Pierce oscillator circuit with the selected component values for oscillation at 1.16 GHz. The node of oscillator output is labelled as V_{out} on the circuit schematic.

We built a PCB with the selected components and wire-bonded the resonator to it (see Figure 2-13). The oscillation power spectrum density and phase noise of this oscillator circuit can be found in Figure 2-14 and Figure 2-15, respectively. The oscillator exhibits performance on a par with prior demonstrations [32].

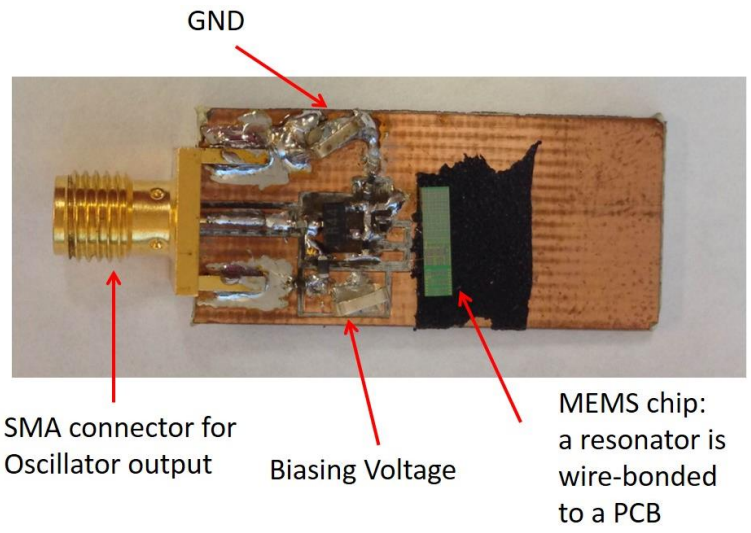


Figure 2-13. The Pierce oscillator on PCB with the AlN MEMS resonator wirebonded to it.

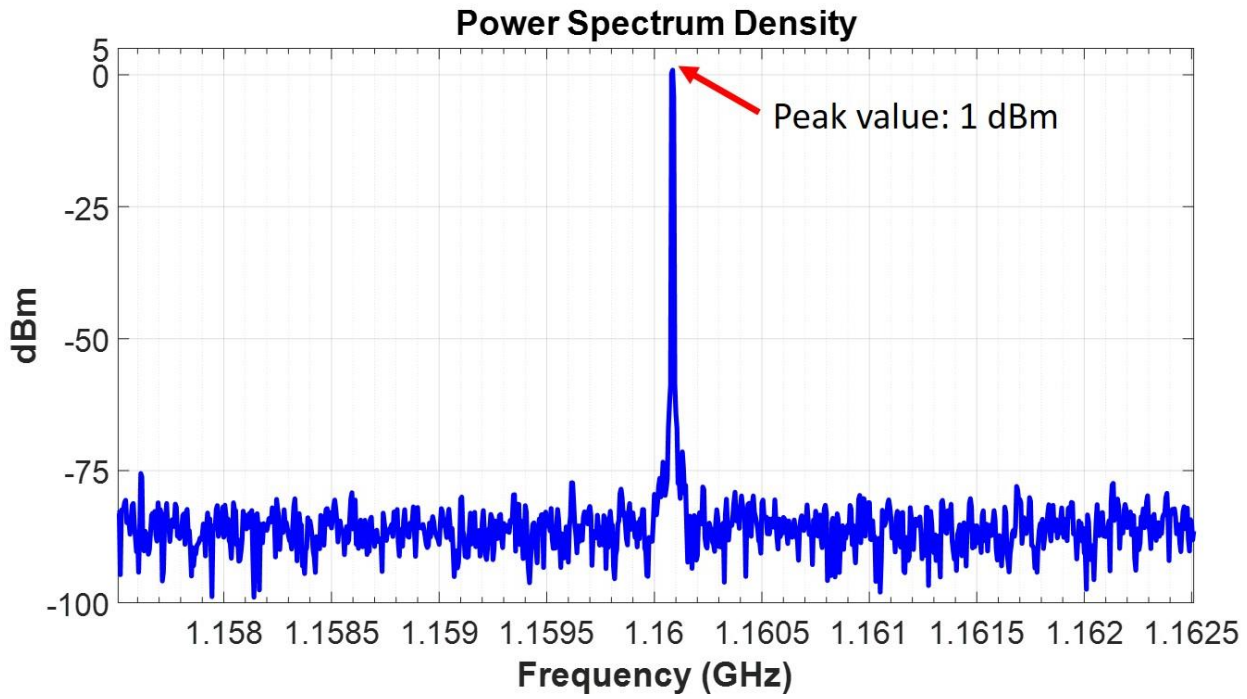


Figure 2-14. Power spectrum density measurement of the oscillator.

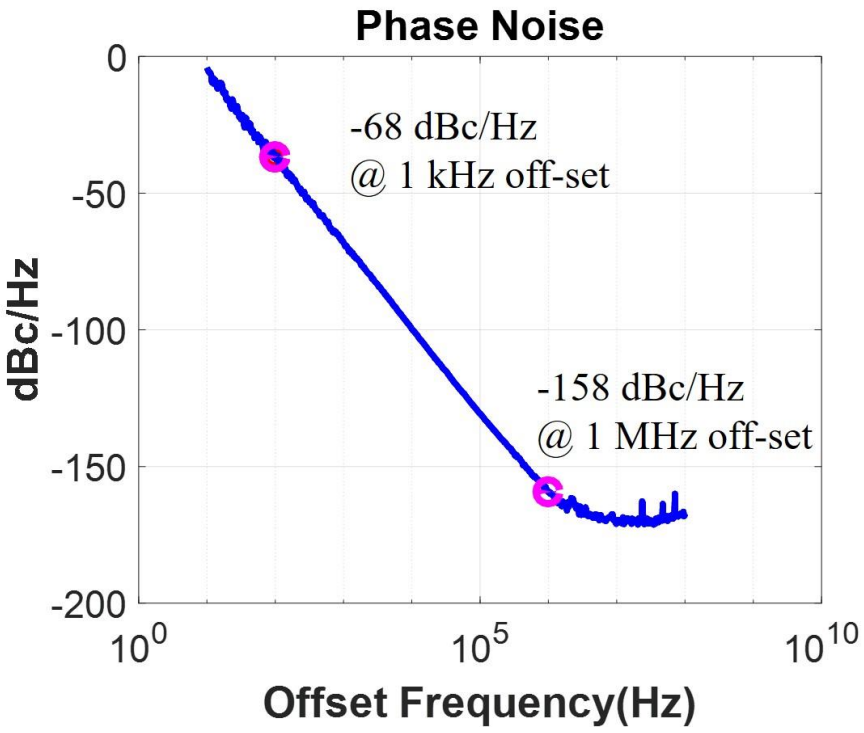


Figure 2-15. Phase noise versus offset frequency measurement of the oscillator.

2.5.2 Accelerated Hermeticity Tests of the Oscillator

The whole PCB board is placed into the climatic chamber (TestEquity Model 123H) and temperature and humidity rate are set to 85˚C and 85 %, respectively (*i.e.* harsh environment conditions [33]). The oscillation frequency is monitored with a Fluke PM6690 frequency counter. The oscillation frequency starts changing after 12237 sec (*i.e.* 203.95 mins) under harsh environmental conditions. Figure 2-16 and Figure 2-17 show the recorded humidity rate and temperature as well as frequency counter readings over time of oscillation, respectively, before and after the oscillation frequency starts changing abruptly. As seen from the figures, the frequency of oscillation is quite stable before the changes start. As the time passes by, the rate of change in the oscillation frequency increases significantly.

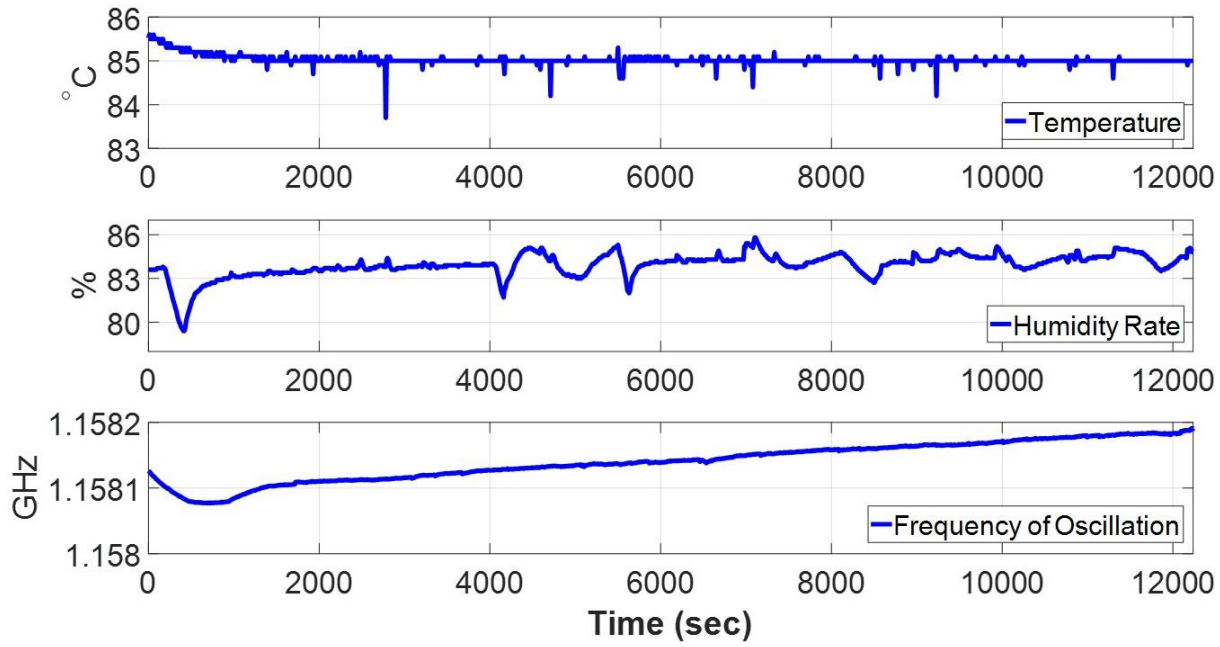


Figure 2-16. Frequency of oscillation, temperature and humidity rate readings versus time before the oscillation starts changing abruptly.

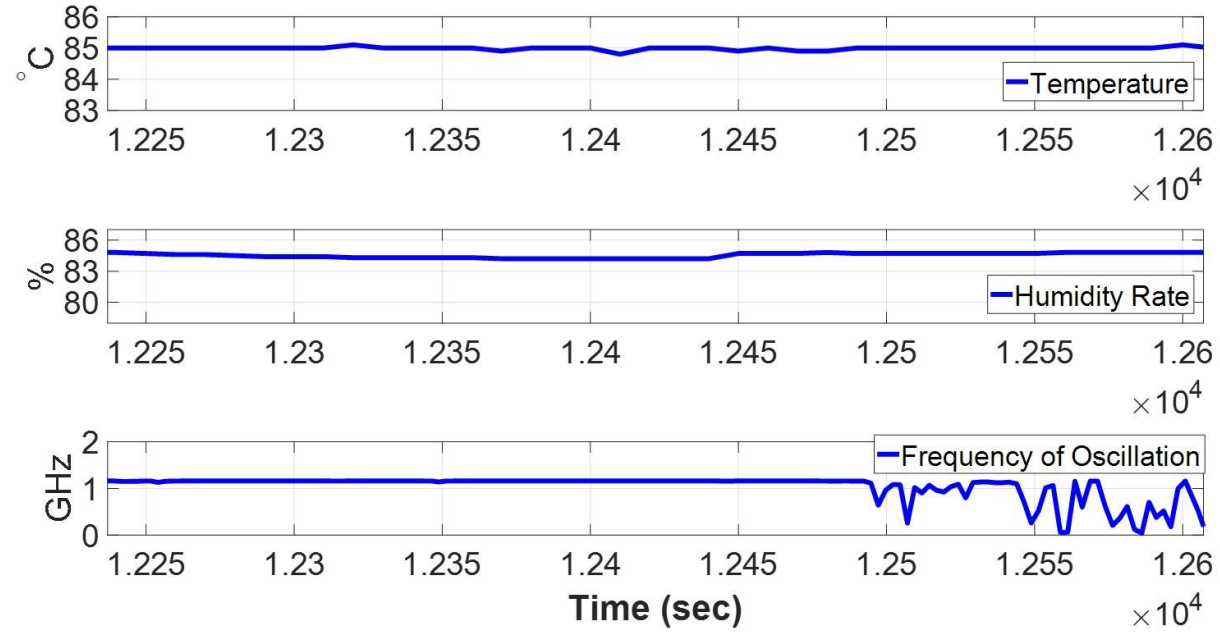


Figure 2-17. Frequency of oscillation, temperature and humidity rate readings versus time after the oscillation starts changing abruptly.

The admittance responses for the resonator that was placed in the Pierce oscillator is shown in Figure 2-18 before and after the hermeticity tests. Similarly, the admittance response of another identical resonator on the same die, but electrically inactive during the hermeticity tests, is shown in Figure 2-19 before and after the hermeticity tests. Table 2.5 shows the tabulated performance metrics of these resonators before and after the hermeticity tests.

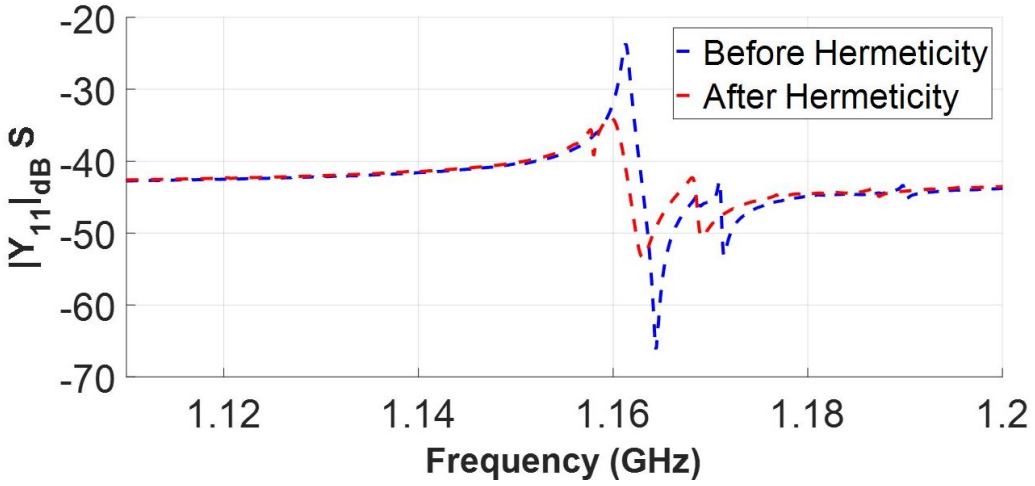


Figure 2-18. Admittance responses of an electrically active resonator during the hermeticity tests (*i.e.* the one making the oscillator).

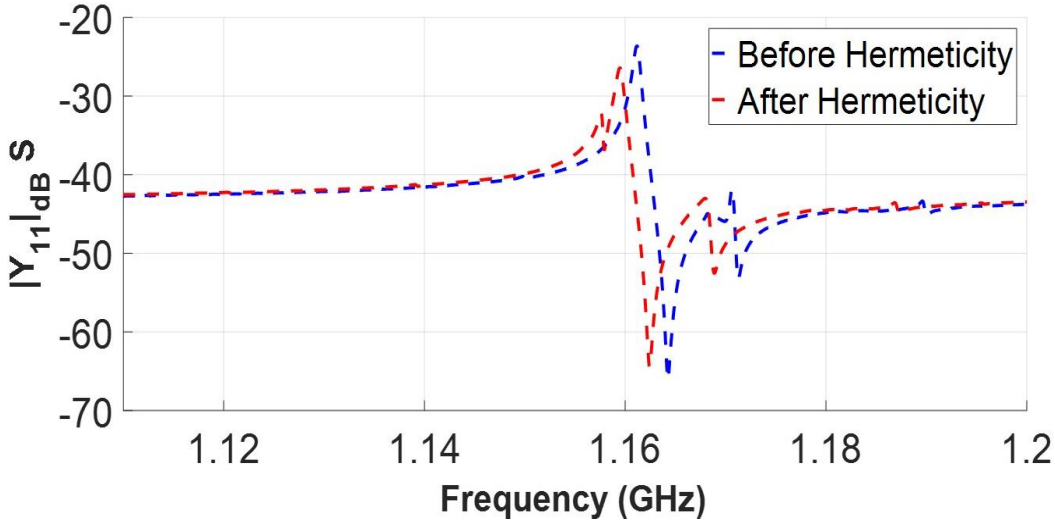


Figure 2-19. Admittance responses of an electrically inactive resonator during the hermeticity tests (*i.e.* no electrical connection during the hermeticity tests).

Table 2.5. Extracted performance comparison of electrically active and inactive full process AlN MEMS CMRs before and after the hermeticity tests.

Extracted Performance Comparison of AlN Resonators					
	Testing	f_o **(GHz)**	k_t^2 **[%]**	***Q***	***FoM***
Electrically Active	Before hermeticity	1.161	1.64	1427	23.4
	After hermeticity	1.160	1.34	448	6.0
Electrically Inactive	Before hermeticity	1.161	1.72	1374	23.7
	After hermeticity	1.160	1.32	1280	16.9

The admittance responses ($|Y_{11}|_{dB}$) of the corresponding two-port AlN MEMS resonators can be found in Figure 2-18 and Figure 2-19, respectively for electrically active and inactive resonators in the hermeticity tests.

In order to calculate the acceleration factor for extrapolating the lifespan of the encapsulated AlN MEMS CMRs under jungle conditions (*i.e.* 35˚C and 85 % [34]) we use the Arrhenius equation provided in [35]. For the thermal activation energy of AlN on SiO_2 we assumed an energy of 2.9 eV under the packaging conditions (this number is taken from [36], where thin film AlN is synthesized by physical vapor deposition techniques). For a more accurate estimation, this activation energy should be also experimentally acquired from the fabricated chips by repeating the tests at two different temperature levels until device failure and using the aforementioned Arrhenius equation.

Considering test conditions, we calculated the acceleration factor as 41.83 which results in approximately 5.92 days under the jungle conditions. These numbers suggest that the failure of the encapsulated resonators should be analyzed and improvements should be made in the fabrication process and/or related design rules. The potential failure mechanisms might be any

one or more of: i) the oxidization of copper layers in RDL, ii) failure of package or iii) degradation of MEMS only device (both metal layers and device level thin film AlN).

2.6 Selected Individual Resonator and Filter Frequency Responses

Based on findings of both MEMS and TFE DoE runs we design a two-port resonator having *FL* of 84 μm and *FN* of 25 with *full dist anc* and no *OE* extension. The encapsulated resonator frequency admittance response is shown in Figure 2-20 and filter frequency s-parameter response comprised of three cascaded resonators of this design is shown in Figure 2-21, respectively in comparison with their corresponding MEMS only fabrication frequency responses. The termination is set to 200 Ω in software to match the s-parameter response of filters. As seen from the figures, even though spurious modes appear in the frequency responses of this selected resonator geometry, they do not impact the passband of the filter formed by these resonators as they are sufficiently away from the bandwidth of interest. Note that these figures have different frequency scale than those provided in the MEMS DoE run.

The tabulated performance comparisons for MEMS only fab versus encapsulated fab for both individual resonators and filters are provided in Table 2.6 and Table 2.7, respectively; whereas, aerial SEM images of MEMS only fabricated resonator and filters are shown in Figure 2-22 and Figure 2-23, respectively.

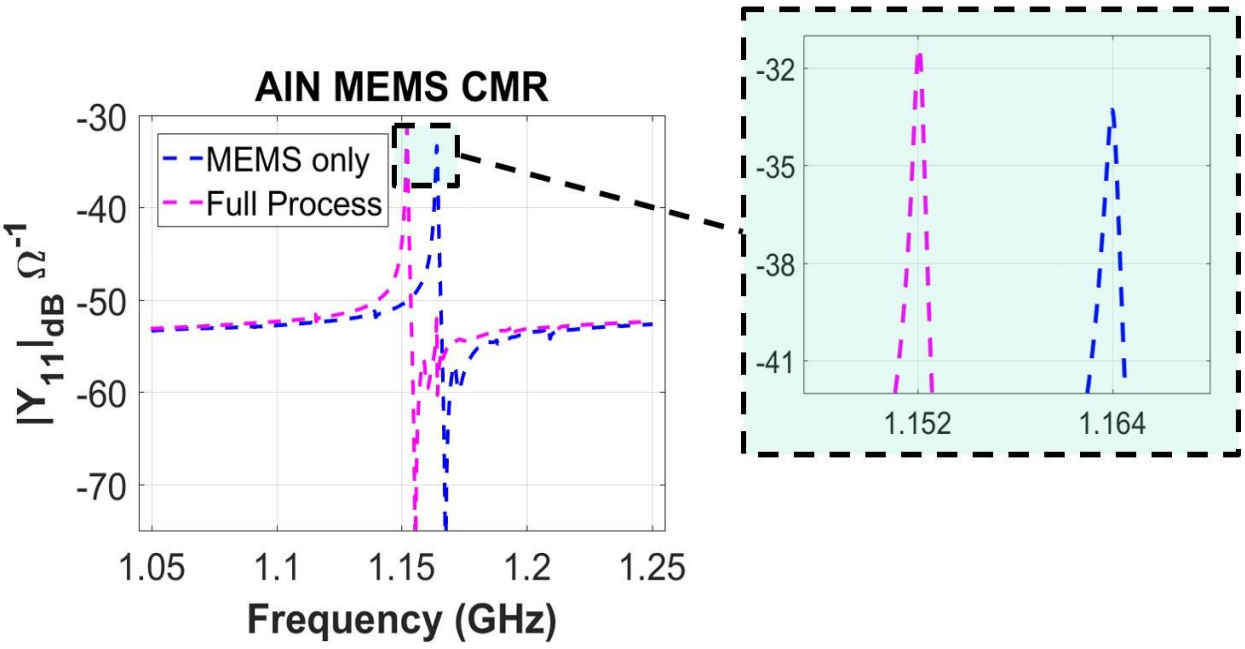


Figure 2-20. Selected two-port resonator frequency response for both MEMS only fab and encapsulated fab runs. Tabulated performance comparison for MEMS only fab versus encapsulated fab is provided in Table 2.6.

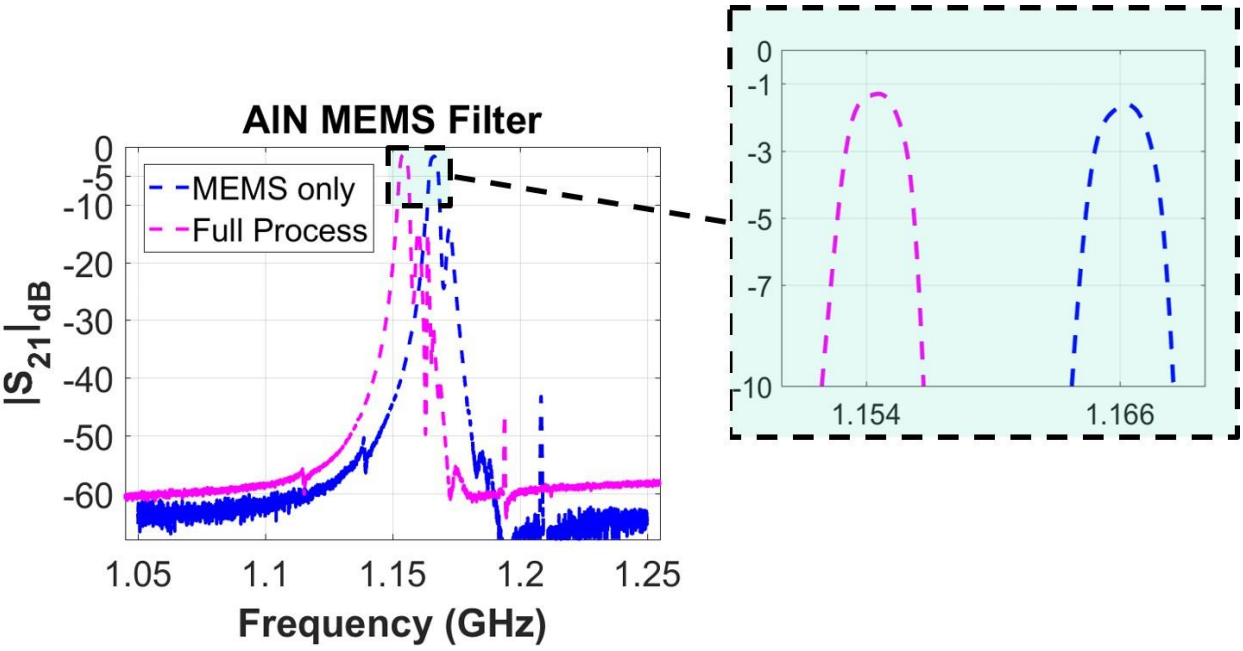


Figure 2-21. Filter frequency responses when three of the selected two-port resonators are cascaded for both MEMS only process and full process fabrication runs. Tabulated performance comparison for MEMS

only fab versus encapsulated fab is provided in Table 2.7. The termination is set to 200 ohm in software to match the s parameter response.

Table 2.6. Extracted performance comparison of AlN MEMS resonators after MEMS only and full fabrication process. Note that in the MEMS only there is no UBM formation.

Extracted Performance Comparison of AlN MEMS CMRs				
Fabrication Type	f_o **(GHz)**	k_t^2 **[%]**	Q	C_o **(fF)**
MEMS only process	1.164	1.68	1423	303
Full Process (MEMS+TFE+RDL)	1.152	1.61	1850	311

The admittance responses ($|Y_{11}|_{dB}S$) of the corresponding two-port AlN MEMS resonators can be found in Figure 2-20.

Table 2.7. Extracted performance comparison of AlN MEMS filters after MEMS only and full fabrication process. Note that in the MEMS only there is no UBM formation.

Extracted Performance Comparison of AlN MEMS Filters				
Fabrication Type	f_o **(GHz)**	***IL*** **(dB)**	***BW*** **(MHz)**	***OBR*** **(dB)**
MEMS only process	1.166	1.62	3.47	22.26
Full Process (MEMS+TFE+RDL)	1.164	1.30	3.38	23.58

The s-parameter response ($|S_{21}|_{dB}$) of the corresponding AlN MEMS filters can be found in Figure 2-21.

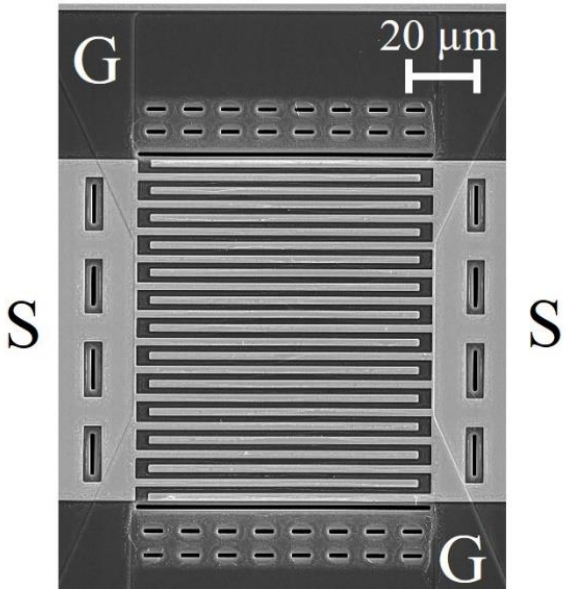


Figure 2-22. Aerial SEM image of selected two port AlN MEMS resonator. The image is taken from a die on MEMS only fabrication.

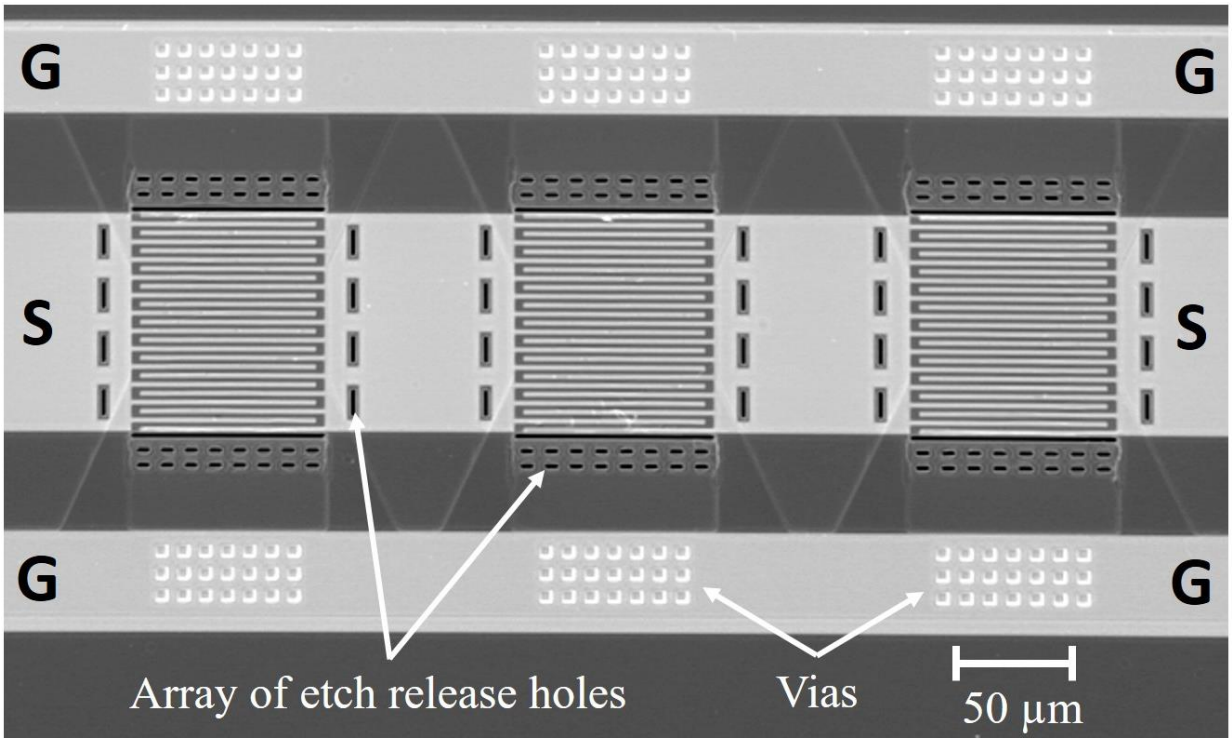


Figure 2-23. Aerial SEM image of filter consisting of three selected two port AlN MEMS resonators connected in series. The image is taken from a die on MEMS only fabrication.

2.7 Conclusions

A cross-sectional SEM image of an AlN MEMS filter with individually packaged resonators from a successful full process run can be found in Figure 2-24. In summary, TFE process along with RDL fabrication yields functional resonators and filters. Only minor changes are observed in critical resonator parameters such as k_t^2 and Q. The reason why Q gets higher and IL gets better after full process is likely related to the fact that the ground connection in the trace of each individual resonator and filter improves. The frequency variation from MEMS only fabrication to full process fabrication is within lot-to-lot variation. Location and amplitude of spurious modes are not significantly affected by packaging. It has been proven with the performance of the selected resonator and filter that the distributed etch release holes in the design of AlN MEMS CMRs do not impact the resonator *FoM* (since *FL* is large enough) and location and amplitude of the SMs. It also permits to keep the amount of lateral release the same for high FN devices and smoothen the overall topography for the TFE capping layer, and thus limiting the thin film stress in the device layer AlN and capping layers. Despite the success of the platform, the 2nd RDL via did not yield 100 %. This caused low yield in the arrayed filters as later described in Chapter 3.2.2.5. The success rate in the RDL vias could be improved by making the critical distance rules on the corresponding layer stricter (*i.e.* higher). Also, in the hermeticity tests we found out the life-time of the encapsulated resonators under harsh environmental conditions and thus at jungle conditions is limited. The potential source of the issue could be one or more of the oxidization of copper lines, failure in thin-film package and failure of the MEMS device itself due to increase in metal and AlN losses. Further studies are required for failure analysis and potential hermeticity upgrades in the encapsulated AlN MEMS CMRs and filters from both design and fabrication standpoints.

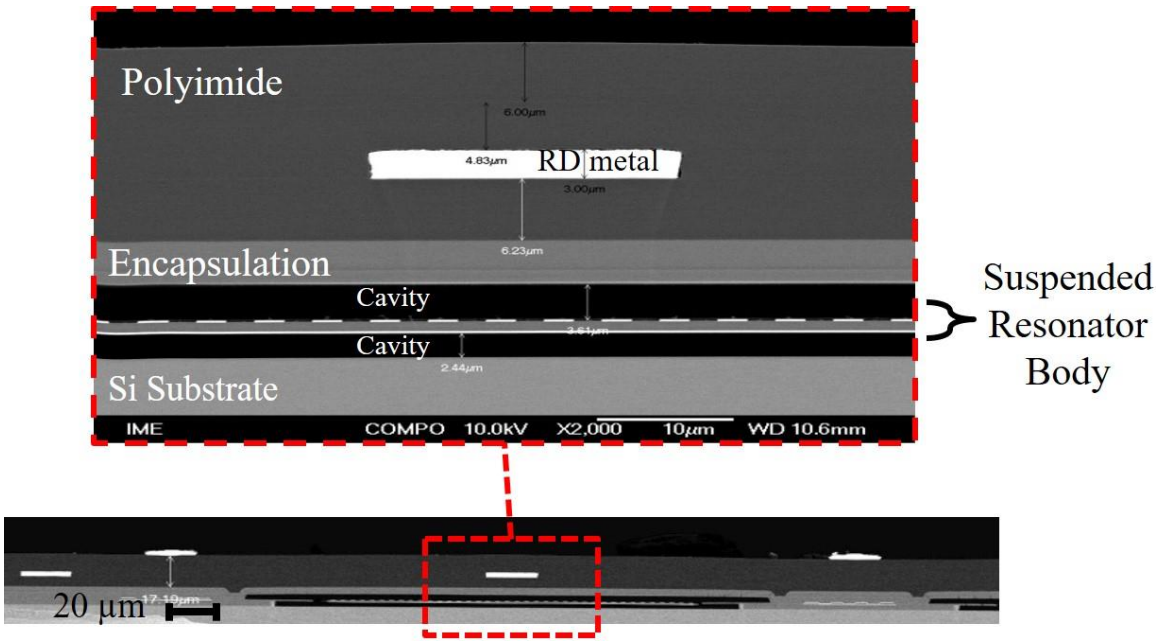


Figure 2-24. Cross-sectional SEM image of a device after full fabrication process. The image is taken from the side after focused-ion beam cut and mechanical polishing (a courtesy of A*STAR, IME, Singapore).

Chapter 3

Hybrid 3D Integration of AlN MEMS Chip with CMOS Die

In this chapter we provide the details of a proof-of-concept 3D hybrid integrated AlN MEMS/CMOS design via realization of self-healing AlN MEMS filters using the AlN MEMS platform developed in this work (see Figure 3-1). To demonstrate the beneficial effects of RDL routing, we also realized the same circuit with RF routing primarily made on the CMOS chip and used it to make a comparison with the primary RF routing made on MEMS RDL.

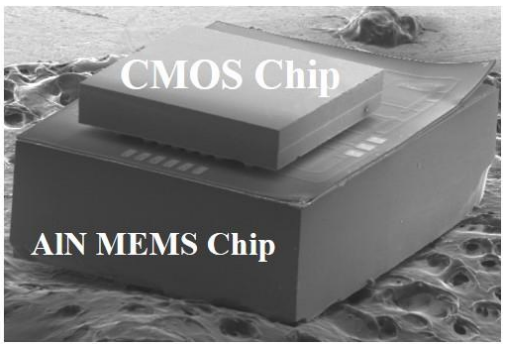


Figure 3-1. Flip-chip bonded AlN MEMS and CMOS chip-stack.

3.1 Proof-of-concept System Application for 3D Hybrid Integration

The beneficial advantages of AlN MEMS CMRs in the synthesis of high frequency BPFs are previously provided in Chapter 1.1. However, the practical implementation of the narrowband AlN CMRs filters is hindered by fabrication-induced process and mismatch variations [37].

Table 3.1 summarizes the performance statistics of standalone AlN MEMS filters comprising three cascaded two-port AlN MEMS CMRs with the geometry selected in Chapter 2.6 (for the individual AlN MEMS CMR statistics for the developed AlN MEMS platform, see [38]). The preeminent filter variation is in f_o, although *IL*, *BW* and *OBR* also vary due to resonator process-induced variations (these parameters characterizing the filters are already defined in Chapter 1.1). Variations in f_o is more critical in the filter performance formed by AlN MEMS CMRs because ± 0.02 % change in f_o corresponds to 13.9 % of the *BW* of these narrowband filters. These variations prevent the filters from achieving optimal performance and enable the implementation of more complex circuits where arrays of these filters are being used. Therefore, it is crucial to develop highly reliable and robust systems that can tolerate these variations.

Table 3.1. Measured statistics of encapsulated standalone AlN MEMS filters.

	f_o	*IL*	*BW*	*OBR*
Mean	1.152 GHz	1.27 dB	3.31 MHz	23.48 dB
STD as of % of mean	0.02 %	3.27 %	0.51 %	0.60 %

To get the statistics of AlN MEMS filters, 12 identically designed sub-filters were placed within 2 mm by 2 mm chip area as 3x4 matrix. Each sub-filter here comprises of three cascaded two-port AlN CMRs, each of which has FN of 25, FL of 84 µm and OE of 0 µm with 'full dist anc' (i.e. the selected resonator and filter in Chapter 2.6).

3.1.1 Application of Statistical Element Selection (SES) to AlN MEMS Filters with CMOS Circuits

In order to address the challenge posed by intra-die variations, we borrow and use the statistical element selection (SES) technique from [37]-[40]. In order to apply the algorithm, instead of using a single standalone filter, we divide the filter into its smaller versions (sub-filters) and create a bank of them by adding identical redundant elements to it. Via series CMOS switches at RF input and output of AlN MEMS sub-filters, a subset k from the bank of N nominally identical sub-filter elements are combinatorially selected in parallel in order to construct a high-yield, self-healing filter. Figure 3-2 shows the conceptual circuit diagram of self-healing filters. The details of the switching matrix on CMOS chip is later discussed in Chapter 3.1.3. For even a modest array size (N) and selection size (k), a large number of combinations is available, for example ${}^{12}C_4=495$.

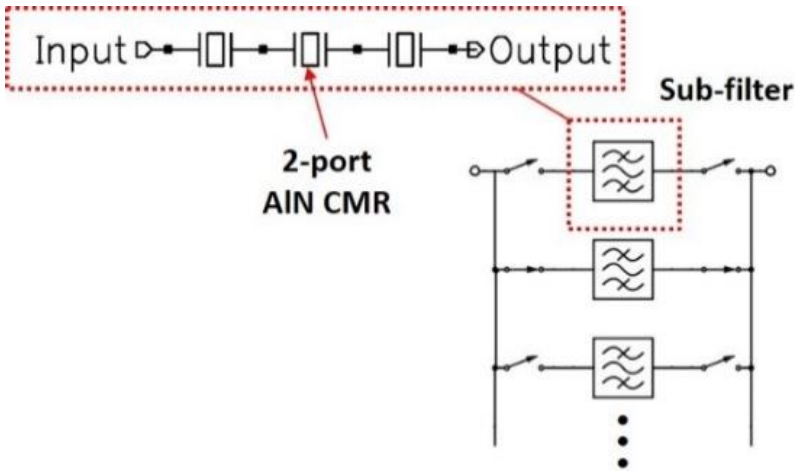


Figure 3-2. Conceptual circuit diagram for self-healing AlN MEMS filters using CMOS switches at the RF input and output.

In order to illustrate the beneficial effect of SES, by considering just the intra-die variation of f_o, we generated the probability density function (PDF) of a standalone filter versus application of SES with N of 12 and k of 4, hence providing 495 unique, selectable filtering components. In this comparison, a typical filter is designed to have f_o at 1.15 GHz and BW of 3.8 MHz. When we require

the f_o of these filters to be within 100 kHz of the targeted value, it can be easily observed that the SES technique provides a dramatic increase in the yield with respect to that of a standalone filter (less than 36%), as illustrated by Figure 3-3.

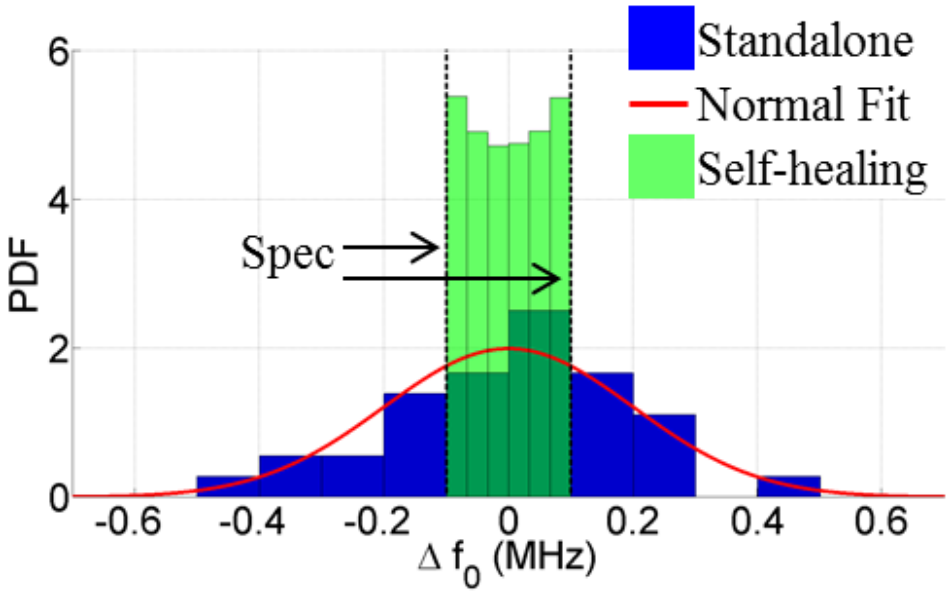


Figure 3-3. PDF of measured center frequency off-set (Δf_o) of standalone filters versus simulated distribution for a self-healing filters. The normal fit in the plot is drawn for standalone filters in order to verify the frequency distribution of the sampled filter responses.

3.1.2 AlN MEMS Chip Design for SES Algorithm

Regardless of the size of the filter bank, the selection size (k) in the demonstration of SES should be fixed to avoid having to change the filter termination impedance. In order to find the optimal selection size, we ran the Monte Carlo simulations for a variety of N and k. To this end, we used the ideal two-port resonator circuit model provided in Figure 1-2 with Q of 2,000, k_t^2 of 1.5 %, f_o of 1.15 GHz and C_o of 450 fF with no C_f (assumed a turns ratio of 1 for the transformer in the equivalent circuit model of two-port resonators). When three two-port resonators are cascaded in series, these resonator parameters result in a filter characteristics with IL of 2.1 dB, BW of 3.8 MHz and OBR of 27 dB. We set specifications on the filter performance as Δf_o < 100

kHz, *IL* < 3 dB, *BW* between 3 and 4 MHz, and *OBR* > 25 dB after the Gaussian distributed variations are introduced to each resonator based on the experimental data. The resulting filter yield versus *k* for various *N* can be found in Figure 3-4. Note that the matching impedance was adjusted for each *k* separately as it changes the effective C_o of the resulting filter. The optimum selection size for almost all array sizes was found to be four and the yield increased with array size. Interestingly, the same optimum value was observed in a quite different application of SES provided in [39]. Based on the matching impedance needs, resonator size can be altered as the selection size has a significant impact on yield. Note that in order to better represent the circuit in the estimation of overall yield, the CMOS switches and their respective statistical data should be also included in the Monte Carlo simulations along with the AlN MEMS CMRs and filters. Since variations in the MEMS devices have higher impact on the center frequency, we have only included the resonator statistics in the Monte Carlo analysis for simplicity.

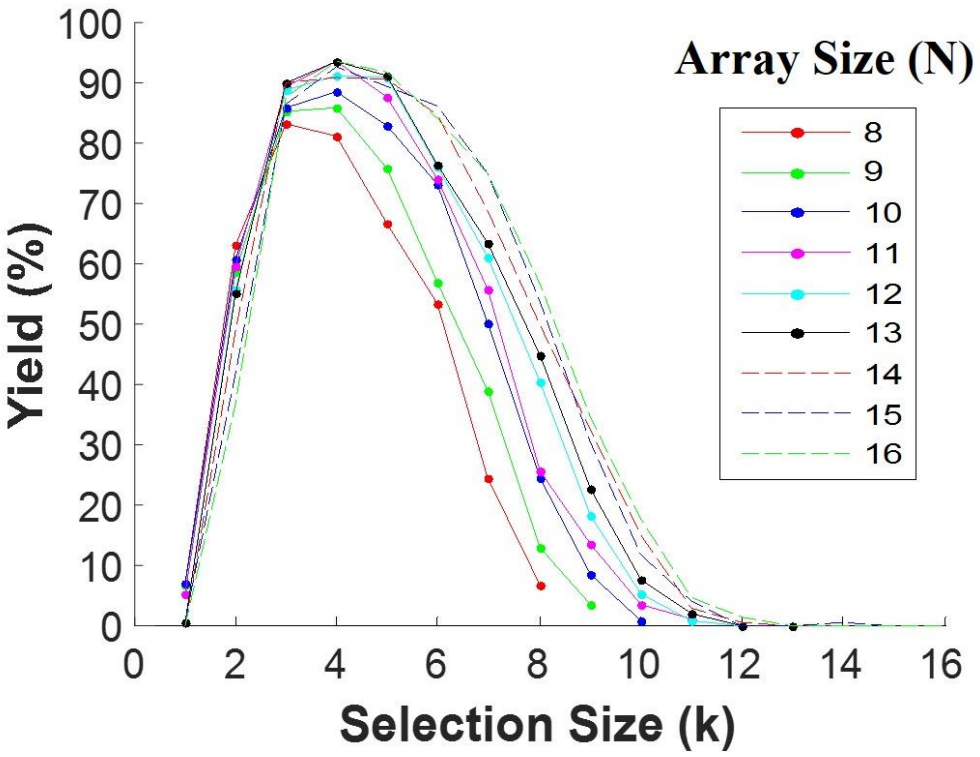


Figure 3-4. Parametric Monte Carlo simulation of self-healing AlN MEMS filters when applying SES. Yield is plotted versus selection size (*k*) for varying values of array size (*N*).

The Monte Carlo analysis suggests that we set the selection size to four and increase the array size as much as possible. Since we want to limit the filter area on the MEMS chip to 2x2 mm, the constraint on the maximum number of elements in the array becomes twelve so that the self-healing filter can simultaneously be matched to 50 Ω when four sub-filters are switched on.

3.1.3 CMOS Chip Design for SES Algorithm

In order to implement SES, we built a switching array on CMOS chip to turn each sub-filter branch on and off individually. Each RF switch is a single NMOS transistor, whose size was optimally determined based on the trade-off between its on series impedance and parasitic shunt capacitance using the post-layout parasitic extraction simulations performed in CADENCE. A set of D flip-flops was also built on CMOS chip and connected in series to control the switching matrix. On the layout, the output of each D flip-flop is connected to the CMOS switch pair located at the RF input and output of each sub-filter branch. The corresponding chip concept is shown in Figure 3-5. In this figure, the RF and digital signal routings are also highlighted based on which chip is used to do so.

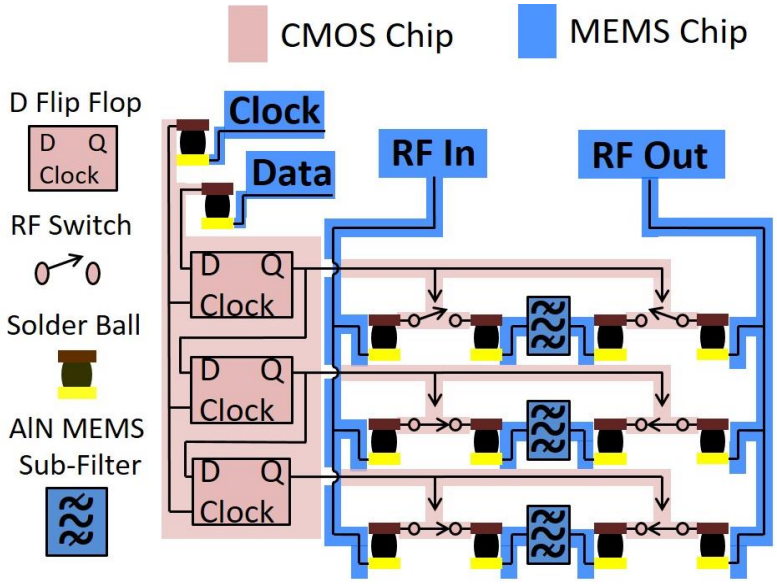


Figure 3-5. Conceptual circuit diagram of self-healing filter with highlighted DC and RF routings, whose color reflects which chip they were built in.

3.2 Proof-of-concept System Demo on a 3D Hybrid Integrated AlN MEMS/CMOS Chip Stack

3.2.1 Chip Fabrication and Integration

We realized the 3D hybrid integration of AlN MEMS/CMOS chip stack in a collaborative effort with several microelectronic foundries. The AlN MEMS chip of 2 x 2 mm filter array area is fabricated in the developed AlN MEMS platform at A*STAR, IME, Singapore; whereas the 1.35 x 1.35 mm CMOS chip is fabricated in a 28 nm process node fab line at Samsung, South Korea. 50 µm diameter solder balls were placed on the CMOS chips by TLMI, Texas, U.S.A. The final chip integration is done via flip-chip solder bump-bonding process at A*STAR, IME, Singapore. The optical microscope images of the fabricated standalone AlN MEMS and CMOS chips before the integration can be found in Figure 3-6 and Figure 3-7, respectively.

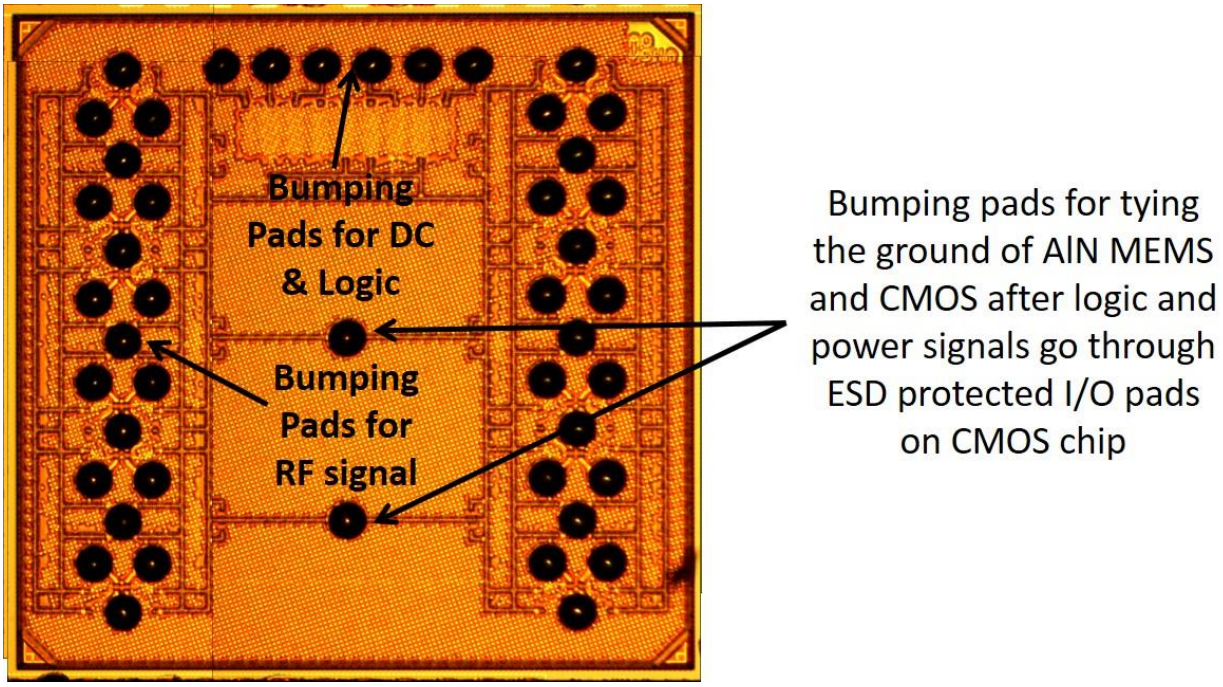


Figure 3-6. Optical microscope image for the designed CMOS chip (28 nm Samsung technology with solder bumps).

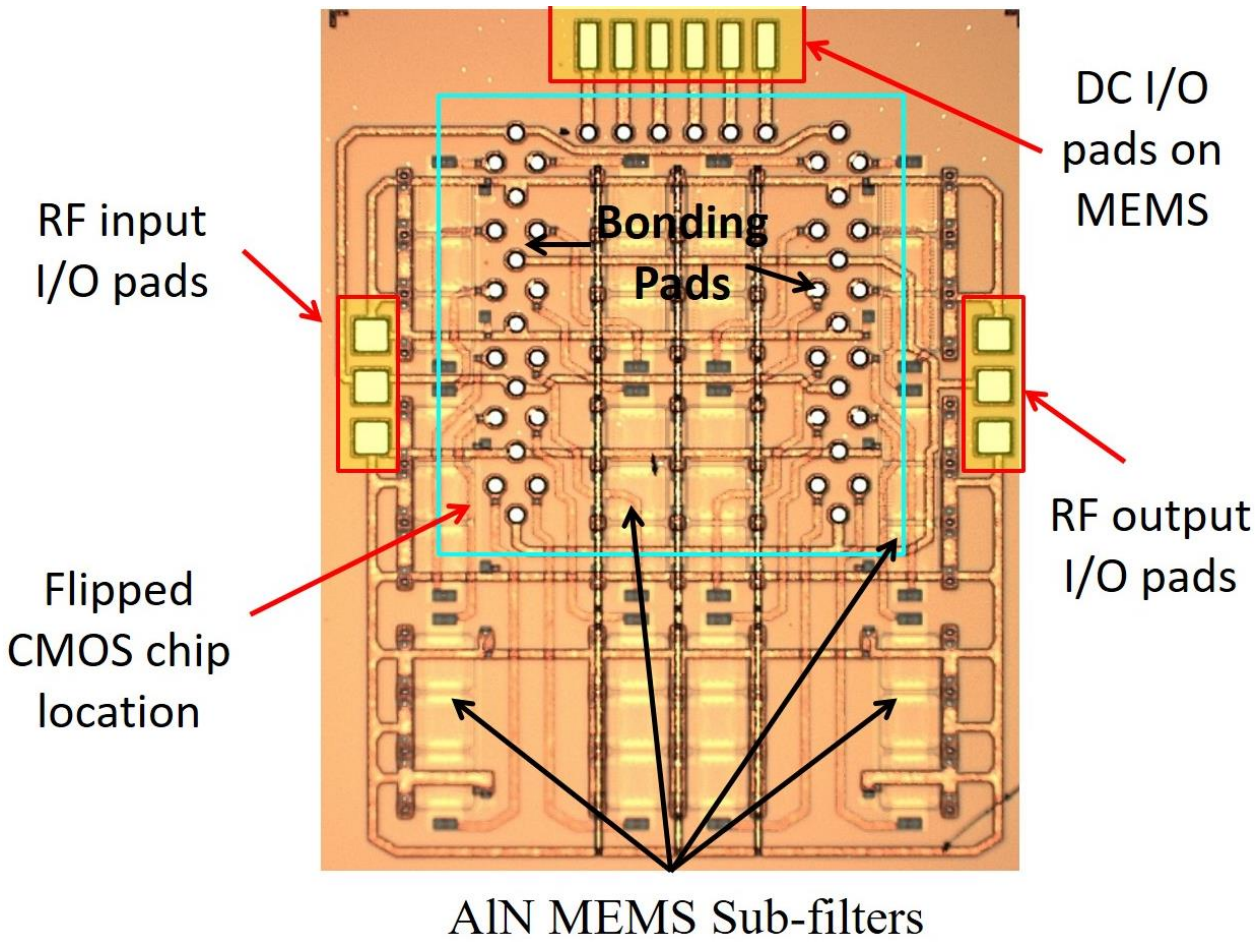


Figure 3-7. Optical microscope image for the designed AlN MEMS chip that corresponds to the CMOS chip design of Figure 3-6.

Figure 3-8 mimics the flip-chip bump-bonding process of a successfully integrated AlN MEMS/CMOS chip stack. Since RDL offers low-loss signal routing and flexibility in the size of AlN MEMS chip for I/O pad placement, we designed the MEMS chip as the substrate chip where we placed all the I/O pads for probe landing and electrical testing. The necessary DC power and digital logic signals, as well as, the interconnects between the CMOS switches and AlN MEMS sub-filters are going from the MEMS to the CMOS through solder-bump bonding pads.

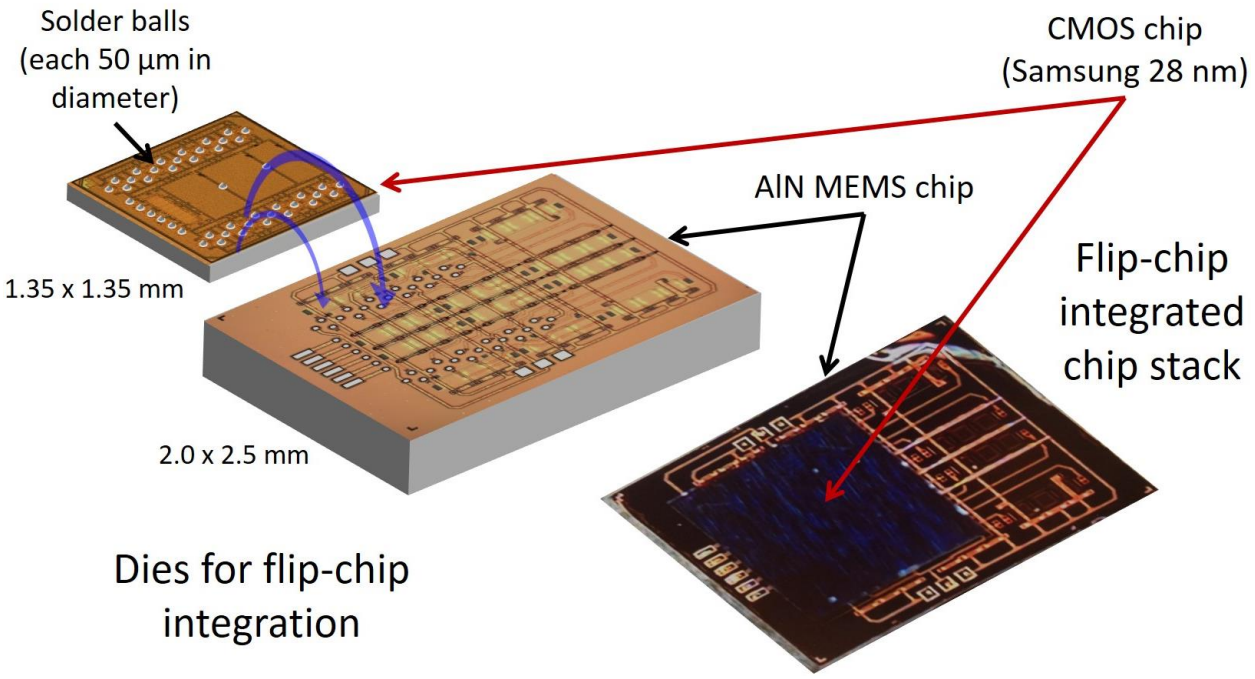


Figure 3-8. Mimicking of the flip-chip integration process of a successfully integrated AlN MEMS/CMOS chip stack.

3.2.2 Experimental Results and System Demo

We demonstrated the SES technique with an array of 1.15 GHz AlN MEMS sub-filters with the aforementioned CMOS circuits via 3D hybrid integration of AlN MEMS and CMOS chip stack.

3.2.2.1 Experimental Setup

Figure 3-9 shows the experimental setup to measure the 3D hybrid integrated AlN MEMS self-healing filters. We designed the AlN MEMS die in such a way that three sets of measurement I/O pads come at three sides of the MEMS chip for convenient probe landing. Two Ground-Signal-Ground (GSG) probes for RF input, output and ground, and one 6-pin multi-contact wedge probe for DC power, ground and logic are employed in the experimental testing. In order to generate a signal vector and a reference clock, we created a Labview model to send out the signals through a National Instrument Data Acquisition Board (NI DAQ). We had to also use a breadboard to condition the signal voltage levels coming out of the NI DAQ and adjust them according to the

voltage levels of the CMOS process node to activate the electrostatic discharge (ESD) protected I/O pads. Finally, the corresponding s-parameters of the self-healing filters are measured through an Agilent 5230A vector network analyzer.

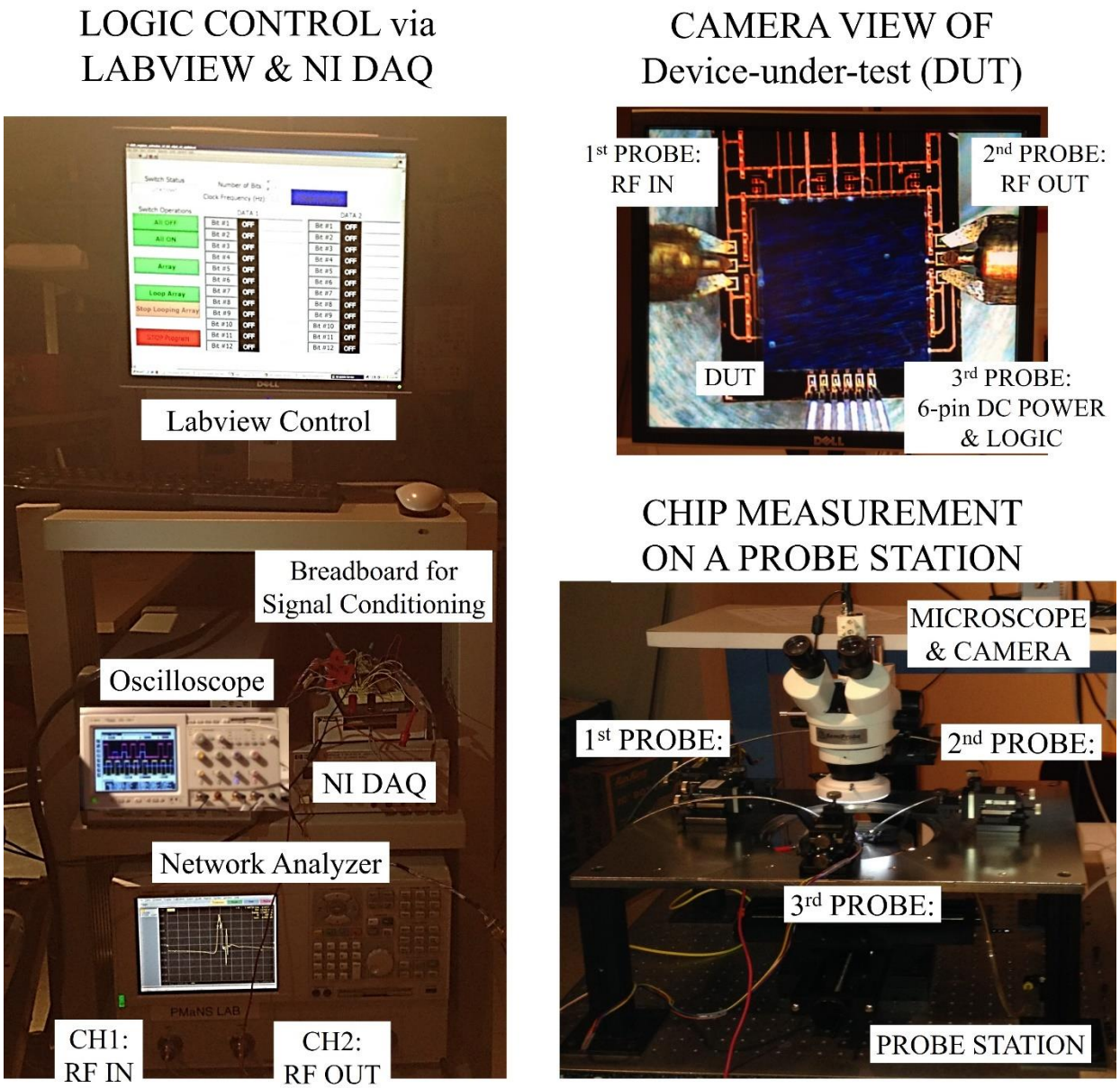


Figure 3-9. Experimental setup to test a 3D hybrid integrated AlN MEMS/CMOS chip stack.

3.2.2.2 Standalone CMOS switch characterization

The resistive characteristics of the designed CMOS switches are presented in Table 3.2. In the experimental measurements of CMOS switches we used a single standalone CMOS chip without solder bumps and MEMS integration, and activated the chip with DC ground and power, and digital logic signals. Then, we measured the resistance at DC across the source and drain connections of a turned-on CMOS switch. In this switch resistance measurement, we used a pair of 5 μm diameter probe tips instead of the pair of GSG probes shown in Figure 3-9.

Table 3.2. Resistive characteristics of the CMOS switch designed in the 28 nm Samsung process.

DC characteristics of CMOS switch fabricated on 28 nm Samsung process	
Type	Resistance per switch (Ω)
Simulation of transistor	5.9
Post-layout parasitic extraction including up to bumping pads	9.8
Measurement with DC probes	10.7*

** The accuracy of the DC measurement was limited because of the contact issue due to small passivation openings designed for flip-chip solder bump bonding integration. We had planned an RF electrical characterization of the switches, but the bumping pad design rules on the pad sizes and passivation openings made it too difficult to land the probe in the designated pads. So, we took measurements with needle probes at DC, instead, without the presence of 4-point probe pad configuration for off-set cancellation.*

3.2.2.3 Measurement of 3D Hybrid Integrated Chip Stack

Responses of several possible combinations based on the measurements taken from one of the 3D integrated chip stacks are provided along with matched and unmatched single standalone

filter responses in Figure 3-10 and Figure 3-11. By matching we mean in the 3D integrated chip stack the capacitive parasitics at RF input and output were resonated out in software with a shunt inductance. For our case, we had to use an inductor of 16 nH with a *Q* of 100 at both RF input and output for matching (Abracon AISC-0805HQ). An *IL* of as low as 3.50 dB and an *OBR* of as high as 28.9 dB were achieved without the presence of these inductors; whereas these parameters get 3.15 dB and 25.1 dB, respectively, after resonating parasitic capacitance out with the inductor to ground at RF input and output.

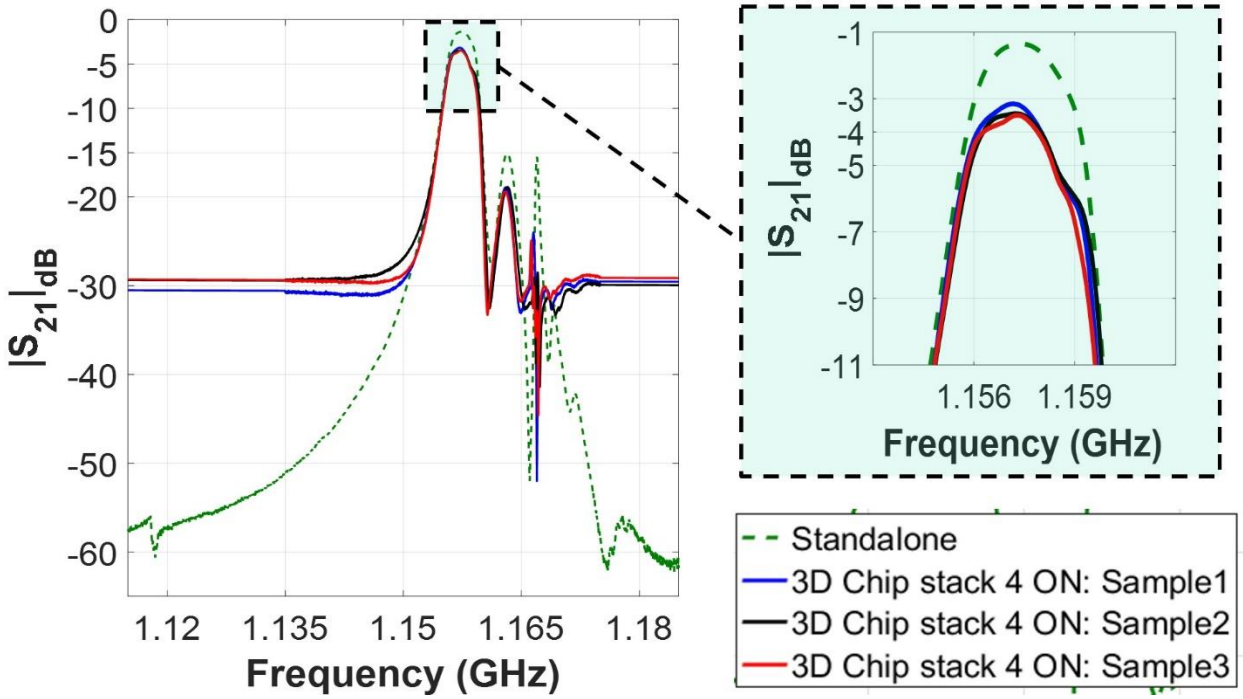


Figure 3-10. Matched frequency response of three possible self-healing filters (red, blue and black) versus a standalone filter (dashed green).

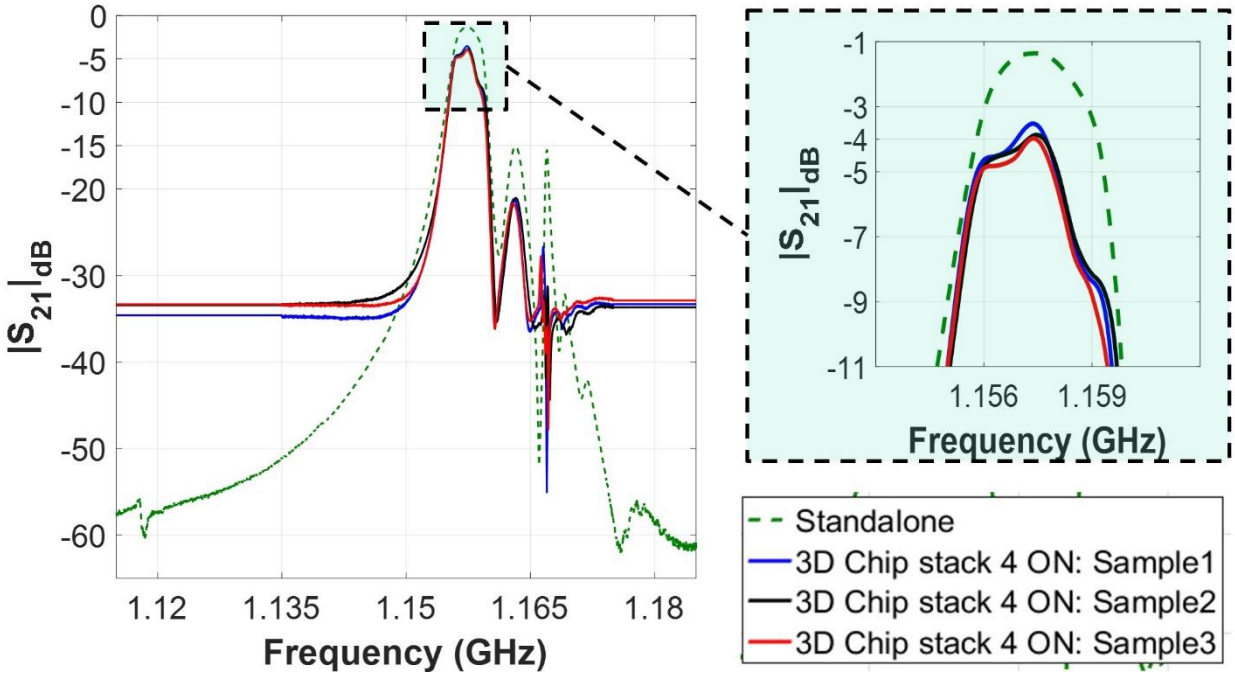


Figure 3-11. Unmatched frequency response of three possible self-healing filters (red, blue and black) versus a standalone filter (dashed green).

The additional 2 dB *IL* in the self-healing filters with respect to that of a standalone filter comes from the CMOS switch in-series resistance (~10.7 Ω per switch), the partial signal routing on CMOS and signal interconnects between the chips via the solder balls. Among the available sub-filters in the bank of the measured 3D chip stack, we identified that 3 out of 12 of them had a poor filter behavior because of the low yield in the 2nd layer RDL via. As discussed in Chapter 2.7, it could be easily improved with more strict design rules on the masks that define the RDL via interconnects. The out-of-band performance of the chips (*i.e.* the response at frequencies further away from the passband of the filters) could also be further improved and made even closer to the individual standalone filter response by making the ground connection better distributed across

the chips in a low loss manner using the RDL routing more effectively and putting more pads for the chip signal interconnects (discussed in Chapter 3.2.2.4 in detail).

3.2.2.4 Ground Electrical Connection in the Chip Stack

One important aspect in the chip integration and experimental testing is the proper grounding of both AlN MEMS and CMOS chips as the operation frequency is high and even small amount of parasitics have a big impact on the filter performance. For example, the same chip stack was also realized without tying the ground pads of CMOS and AlN MEMS together after digital logic and power signals go through ESD protected I/O pads. Figure 3-12 shows the block diagram of the change in electrical connections in the 3D integrated chip stack; whereas, the corresponding CMOS chip design could be seen in Figure 3-13 (for CMOS chip design comparison, see also Figure 3-6).

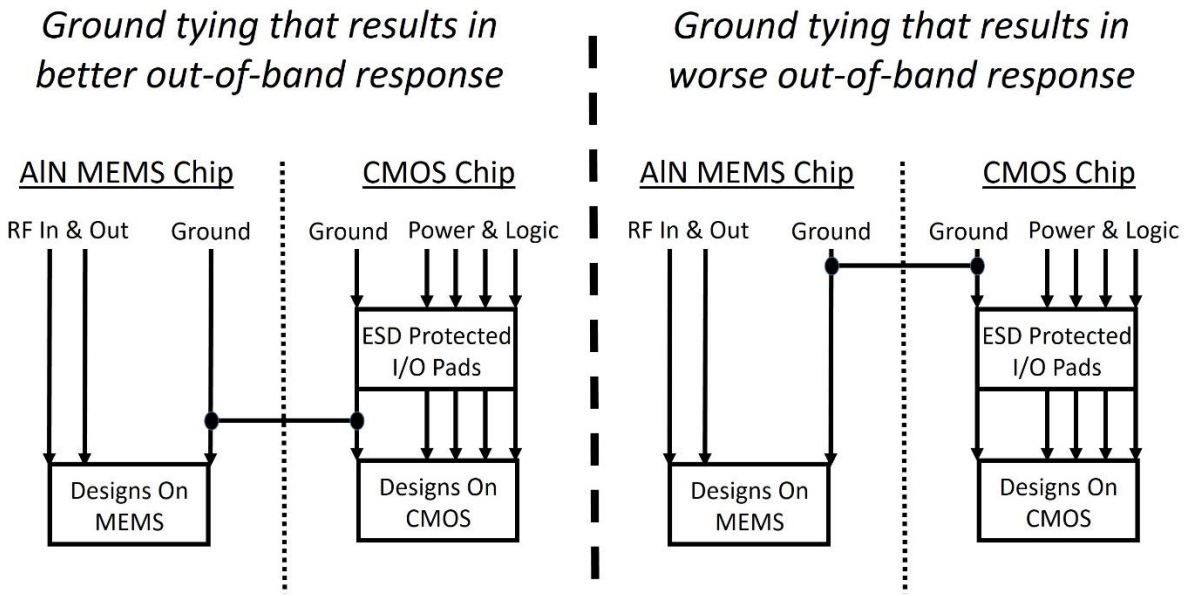


Figure 3-12. Two different block diagrams for electrical connections of I/O signals on AlN MEMS and CMOS chips in the 3D integrated stack. The diagram located at the left hand-side is the original configuration (see Figure 3-6 for the corresponding CMOS chip design); whereas the diagram on the right hand-side showcases a poor grounding of the devices due to the parasitics associated with the ESD pads not designed for RF (see Figure 3-13 for the corresponding CMOS chip design).

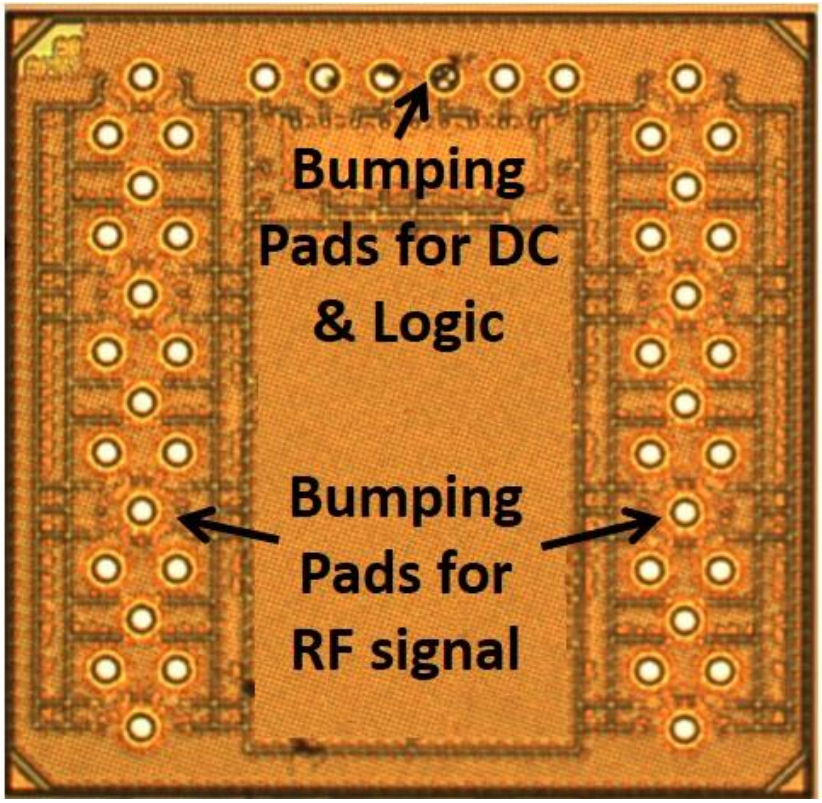


Figure 3-13. Optical microscope image for the designed CMOS chip (28 nm Samsung technology with solder bumps) without tying the grounds of CMOS to AlN MEMS after power and logic signals on CMOS chip goes through ESD protected I/O pads.

As seen from Figure 3-14, the out-of-band-rejection increased significantly as the ESD pads, not designed for RF, have a capacitance to ground, which makes the ground different than AlN MEMS chip. As a solution to this problem, either the ESD protected I/O pads should be designed in conjunction with the self-healing filters or ground of CMOS and MEMS should be tied together after ESD protected I/O pads in order to minimize the ESD interference on the performance of the components operating at RF as in the original results we provided in Figure 3-10 and Figure 3-11. There is still room for improvement in the out-of-band rejection of the original design by making the ground interconnects between AlN MEMS and CMOS chips better distributed across the chip and thus by decreasing the series resistance and inductance arising from the ground routing.

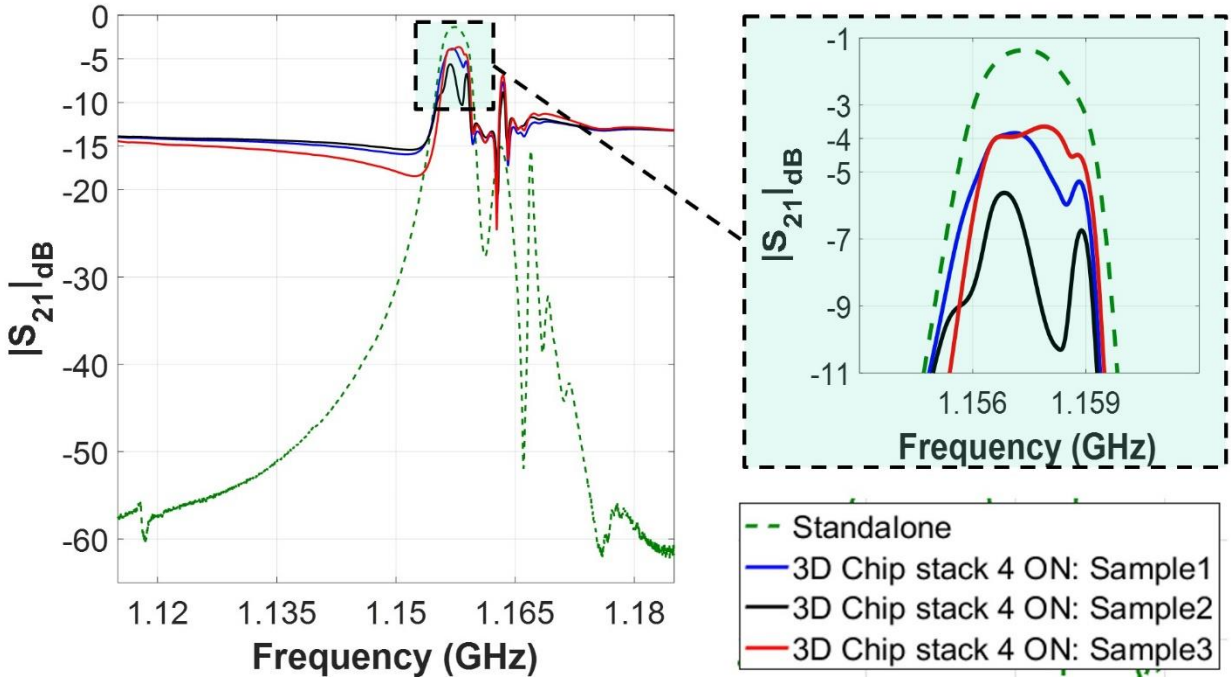


Figure 3-14. Matched frequency response of three possible self-healing filters (red, blue and black) versus a standalone filter (dashed green) without tying the grounds of AlN MEMS and CMOS chips after signals go through ESD protected I/O pads.

3.2.2.5 Application of SES Algorithm to Experimental Data

The application of the SES technique on the experimental data taken from a 3D hybrid integrated chip stack is shown in Figure 3-15. Considering the frequency responses of the self-healing filters, we set the parameter specifications on the filter performance as Δf_o <100 kHz, *IL* < 4 dB, *BW* between 2.75 and 3.25 MHz and *OBR* > 25 dB. In the figure, we marked the data points as green to indicate the devices that pass all the specs, as orange those, which fail in regards to f_o and BW specs but pass *IL* and *OBR* specs, and as red those, which fail in either *IL* or *OBR* specs.

Thanks to the beneficial effect enabled by the SES technique on the yield of self-healing filters, a tuning range of 300 kHz for f_o and 250 kHz for *BW* were achieved. Most of the red points in

Figure 3-15 are due to failing to satisfy the spec for *IL*. As discussed in Chapter 3.2.2.3, only 9 out of 12 subfilters in the filter bank exhibited performances on par with expectations. As a result of this, we had more failure data points among the 495 available filter combinations and the center frequency distribution was artificially wider than expected in the self-healing filters. With the improvement in the 2nd layer RDL via, we expect a smallernumber of failures among the available combinations, and thus a more uniform f_o distribution among the available responses and a wider tuning range for both f_o and *BW*.

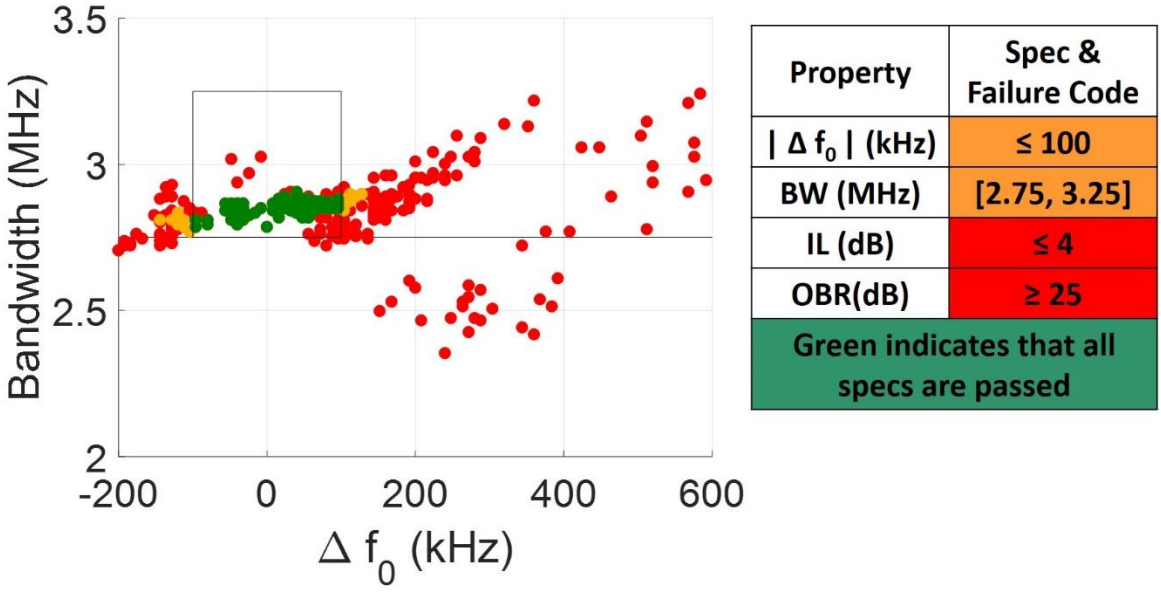


Figure 3-15. Application of SES algorithm on self-healing AlN MEMS filters with $N = 12$ and $k = 4$. Sub-filters on the AlN MEMS chip are combinatorially selected through CMOS switching matrix controlled by a chain of D flip-flops connected in series.

3.2.3 Comparison to a 3D Hybrid Integrated Chip Stack without RDL on MEMS

We also demonstrated how the signal routing could be achieved without RDL on AlN MEMS chip in the 3D hybrid integration of AlN MEMS/CMOS and discussed the differences in this section of the chapter.

3.2.3.1 Signal routing without RDL on MEMS chip

Figure 3-16 describes the conceptual circuit diagram with the RF signal routing on CMOS. Effectively, without the RDL we have only the sub-filter array and a pair of bonding pads for each sub-filter branch on the AlN MEMS chip.

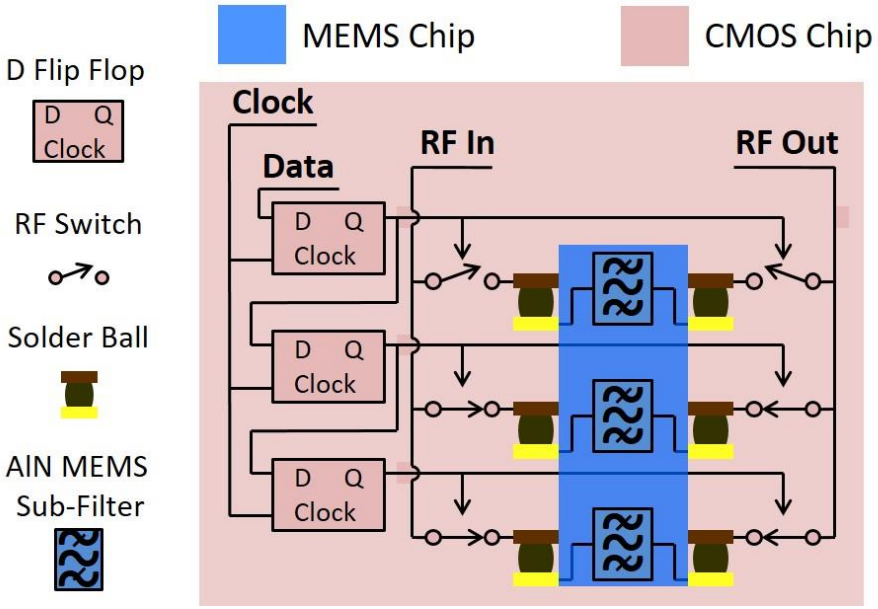


Figure 3-16. Conceptual circuit diagram of self-healing filter with highlighted DC and RF routings based on use of the chip technology without RDL on MEMS chip.

3.2.3.2 Changes in Design of AlN MEMS and CMOS Chips without RDL

Since the signal routing is made on the CMOS chip in this approach, all the measurement I/O pads should be placed on CMOS as it becomes the substrate chip. This limits the MEMS chip size and also causes a very inefficient occupancy of CMOS chip as the MEMS structures are much bigger in size. That is why we placed the I/O pads only on one side of the substrate chip in this CMOS chip design even though it increases the coupling between RF signals, and digital logic and power.

Additionally, given that we target for 50 Ω matching, the losses along the signal path increase as the routing metal layers are thinner in CMOS and have higher sheet resistances than re-

distribution metal layers on AlN MEMS (> 5 x when compared to 28 nm Samsung process node). In other words, the routing now might impact the response of each filter branch differently, and thus we need to make sure that the RF input and output signals are carried out to the center of the chip and distributed symmetrically to all the CMOS switches connected in parallel in order to minimize the routing variations between different branches. This symmetric routing does not only cause additional losses and parasitics, but also introduce potential feed-through between RF input and output as they have to cross each other at several locations given the high number of parallel branches (i.e. *N* equals to 12 in our case). In order to limit the feed-through at such circumstances, we put a ground shield (a grounded metal) between RF input and output.

As a small advantage, though, the substrate chip change in the AlN MEMS and CMOS chip stacks result in less number of bonding pads as DC power and digital signals are directly applied to the CMOS chip, and thus pad losses decrease as the CMOS switches are connected in series with the RF path in this application. Moreover, considering the conceptual circuit diagram previously shown in Figure 3-16 there are also less bonding pads required for each filter branch since the signal follows the path of CMOS switch–MEMS subfilter–CMOS switch.

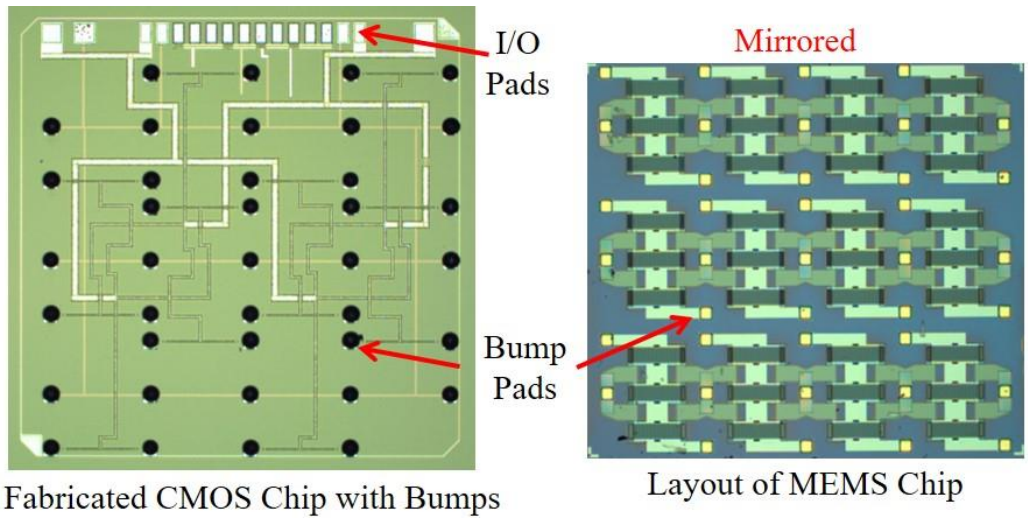


Figure 3-17. Conceptual circuit diagram of self-healing filter with highlighted DC and RF routings based on use of the chip technology without RDL on MEMS chip.

3.2.3.3 Flip-chip Integration with CMOS as Substrate Chip

A flip-chip bonded AlN MEMS-CMOS chip stack with CMOS as the substrate chip is shown in Figure 3-18. Because of the process availability, the 2 mm by 2 mm CMOS chip is fabricated in a 65 nm process node fab line at Global Foundries (GF), California, U.S.A. Again, 50 µm diameter solder balls were placed on CMOS chips by TLMI, Texas, U.S.A. and the AlN MEMS chip is fabricated at A*STAR, IME, Singapore. However, this time the AlN MEMS chip is made 1.8 mm by 2 mm in size in order to allow for probe landing on I/O pads on CMOS chip. The final chip integration is done via flip-chip solder bump-bonding processed by A*STAR, IME, Singapore.

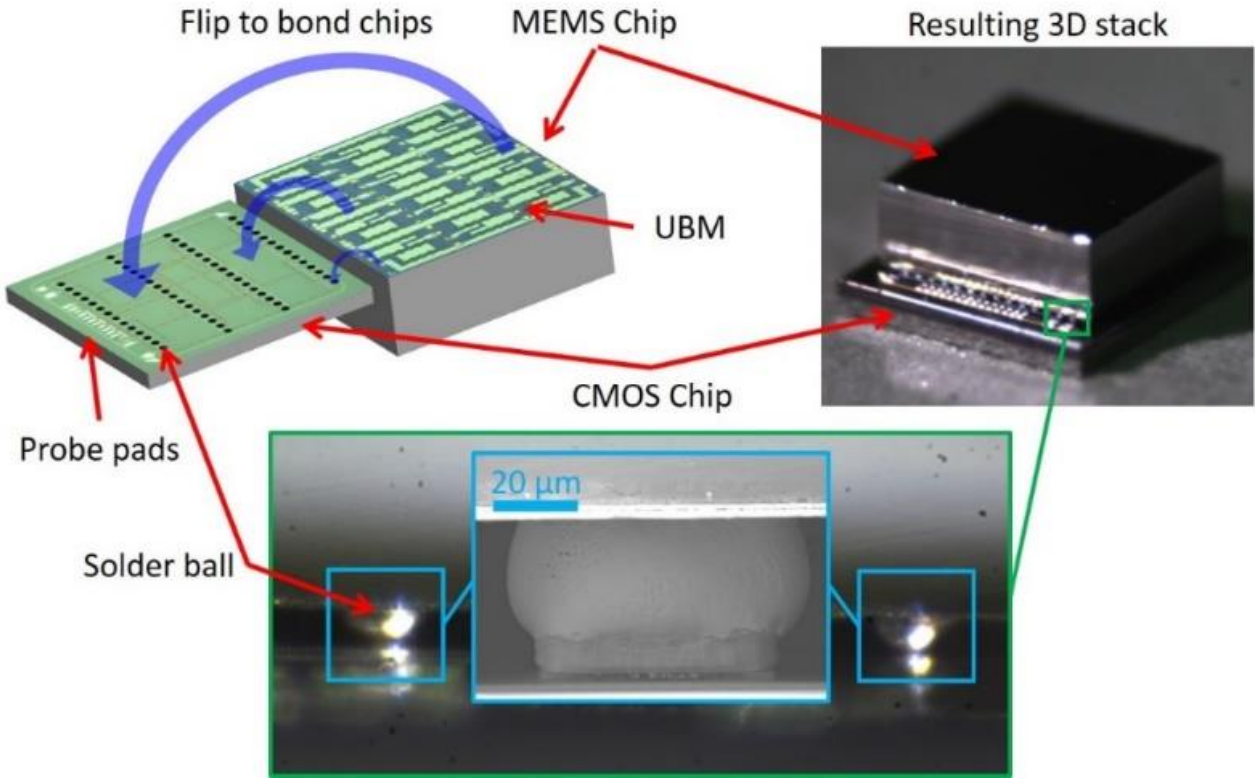


Figure 3-18. A flip-chip bonded AlN MEMS-CMOS chip stack with CMOS as substrate chip along with a cartoon mimicking the flip-chip integration of the chips in the chip stack.

3.2.3.4 Experimental Results of Self-healing AlN MEMS Filters without RDL on MEMS chip

We used a similar experimental test setup to Figure 3-9 in order to measure the 3D integrated chip stack. This time, though, we used a single customized mixed signal probe to apply RF, DC power and digital logic signals.

Figure 3-19 shows the responses of several possible combinations based on the measurements taken from one of the 3D integrated chip stacks along with a matched single standalone filter response. In the 3D integrated chip stack, the capacitive parasitics at RF input and output were resonated out in software again, but this time we had to use a shunt inductance of 5.2 nH at both RF input and output when a *Q* of 50 is assumed for these inductors (Abracon AISC-0805HQ). An *IL* of as low as 7.4 dB and an *OBR* of as high as 16 dB were also attained among the available chips.

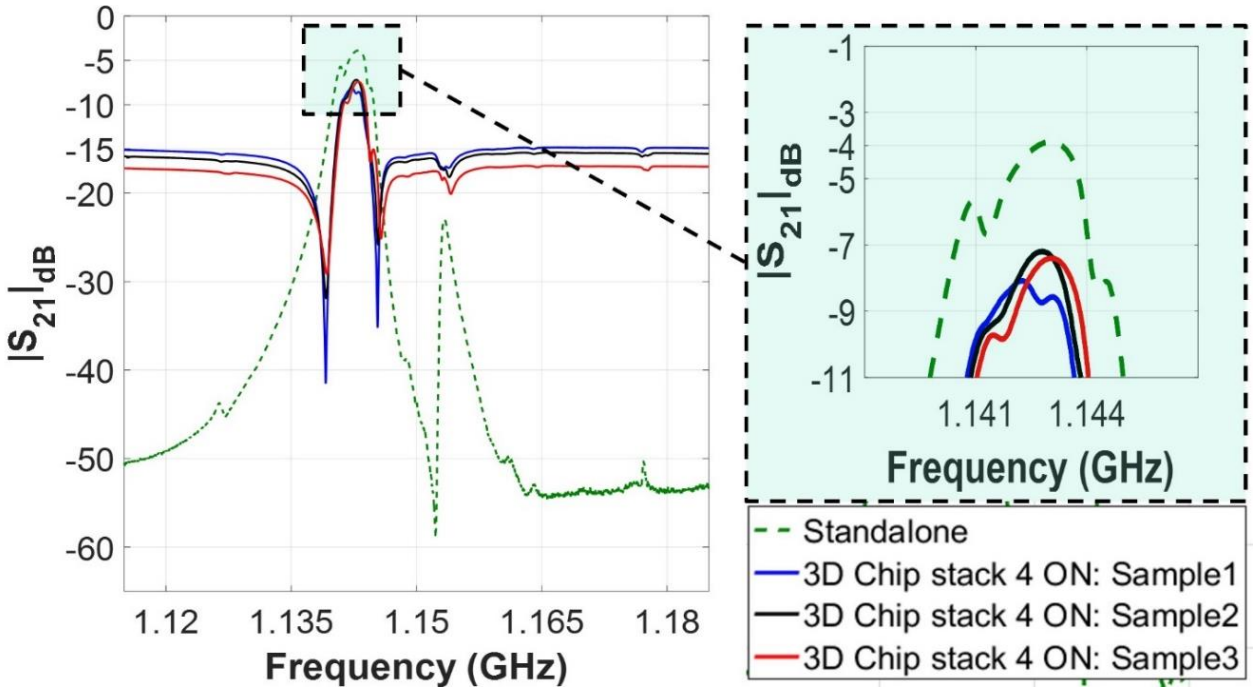


Figure 3-19. Frequency response of three possible self-healing filters (red, blue and black) versus a standalone filter (dashed green) for RF routing on 65-nm IBM process CMOS chip.

The application of the SES demonstrates that both filter f_o and BW may be finely adjusted over a span of around 500 kHz to enhance yield by tuning the self-healing filter into a set of specification bounds as shown in Figure 3-20.

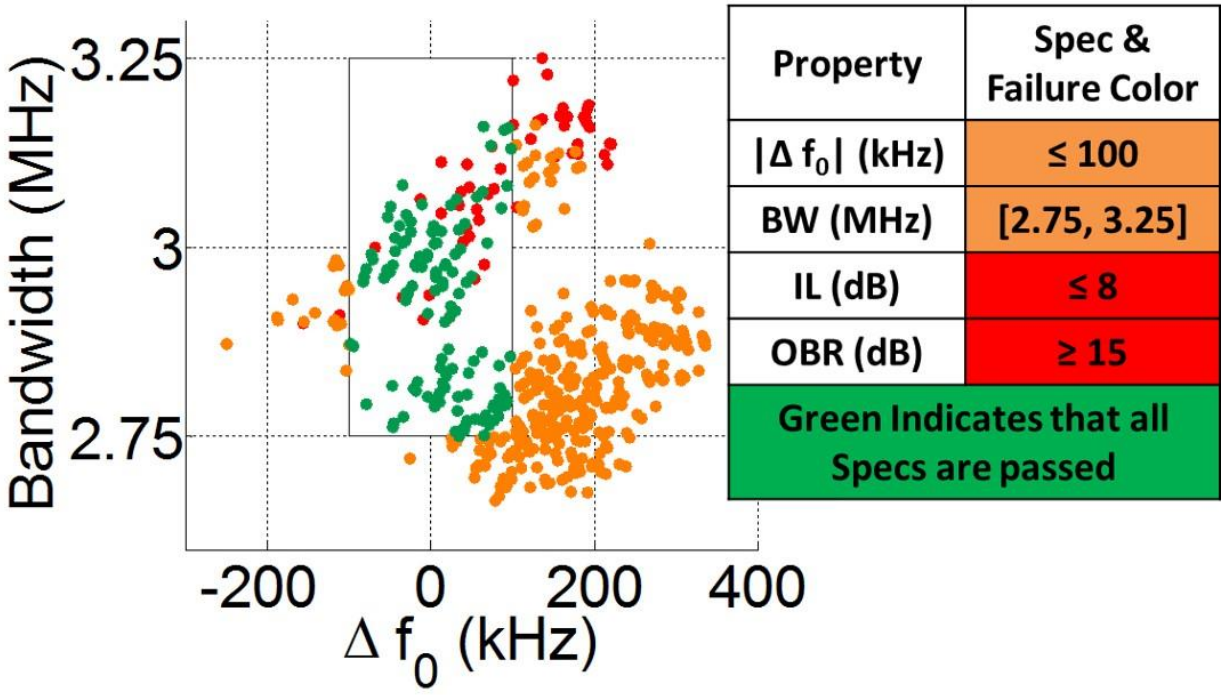


Figure 3-20. Application of SES algorithm on self-healing AlN MEMS filters with N = 12 and k = 4 with the AlN MEMS/CMOS chip stack without RDL.

3.2.3.5 Comparative Data Analysis

The beneficial advantages of RDL are evident when we compare the SES system response of the chip stack with RF routing on CMOS to the 3D integrated solution realized with RF routing primarily made on RDL (see Figure 3-14 and Figure 3-19). As seen from the figures, we have almost 4 dB more *IL* with RF routing on the CMOS chip even though the number of bump pads in series with the RF signal path gets half when the CMOS becomes the substrate chip in the stack. The improvement in *IL*, though, cannot be attributed solely to RDL as the filter performance also

improved with respect to the implementation with routing on CMOS. We estimate that approximately 1.5-2 dB of IL improvement come from RDL.

Additionally, we used a 5.2 nH of inductance with a *Q* of 50 at RF input and output with CMOS routing in order to resonate out the shunt capacitance to ground in the 3D integrated chip stack. When we exclude the simulated parasitics coming from the bonding pads and CMOS switches of both chips, we get almost 5.2 pF shunt capacitance at the RF input and output. In RDL routing approach, this number was only 270 fF, meaning that we achieved almost 20 x reduction in routing parasitics thanks to the RDL. Thereby, we can say for this self-healing filter application that with RDL the parasitic shunt capacitance at the RF input and output gets dominated by switch and bumping pads capacitances instead of capacitance due to the signal routing. Note that in addition to thick inter-metal dielectrics, we also have a floating substrate in MEMS chip, which helps decrease the capacitances to ground even further.

Finally, because of limited resistive losses in RDL routing, we did not have to bring the signals to the center of the chip and distribute it symmetrically between the different branches, and cause high levels of cross-talking between the input and output. Since we also made RF routing primarily on MEMS RDL and logic and power routing primarily on CMOS, we were able to successfully separate DC to RF coupling and provide a better electrical connection in the ground terminals of the chips in the stack. Because of these reasons, the feedthrough from RF input to output gets limited significantly which is made possible by the availability of low loss RDL signal routing in the 3D integrated chip stack.

Chapter 4

Programmable Filter Arrays for Cognitive Radios

In this chapter we describe the second heterogeneously integrated AlN MEMS/CMOS system, which is the programmable filter arrays for cognitive radios. Because of the inability to continue to access CMOS wafers and bumping process over the last two years of the project, we made the proof-of-concept hardware demonstrations of this system via wire-bonding AlN MEMS chip to off-chip CMOS components on a PCB.

4.1 Motivation

The need to efficiently use the electromagnetic spectrum has become a significant challenge for modern communication devices. One way to efficiently use the spectrum is to dynamically change the assignment of the licensed band to the users, hence addressing the issue of spectrum scarcity (see Figure 4-1). In this vision, as high level of interferences or high usage of one channel occurs, the filter needs to adaptively adjust and operate over vacant channels. This form of dynamic spectrum access is implemented in a “cognitive radio” [41]-[44]. In order to achieve such

a capability, we need to design a programmable filter array capable of operating selectively at multiple frequencies within a given frequency range.

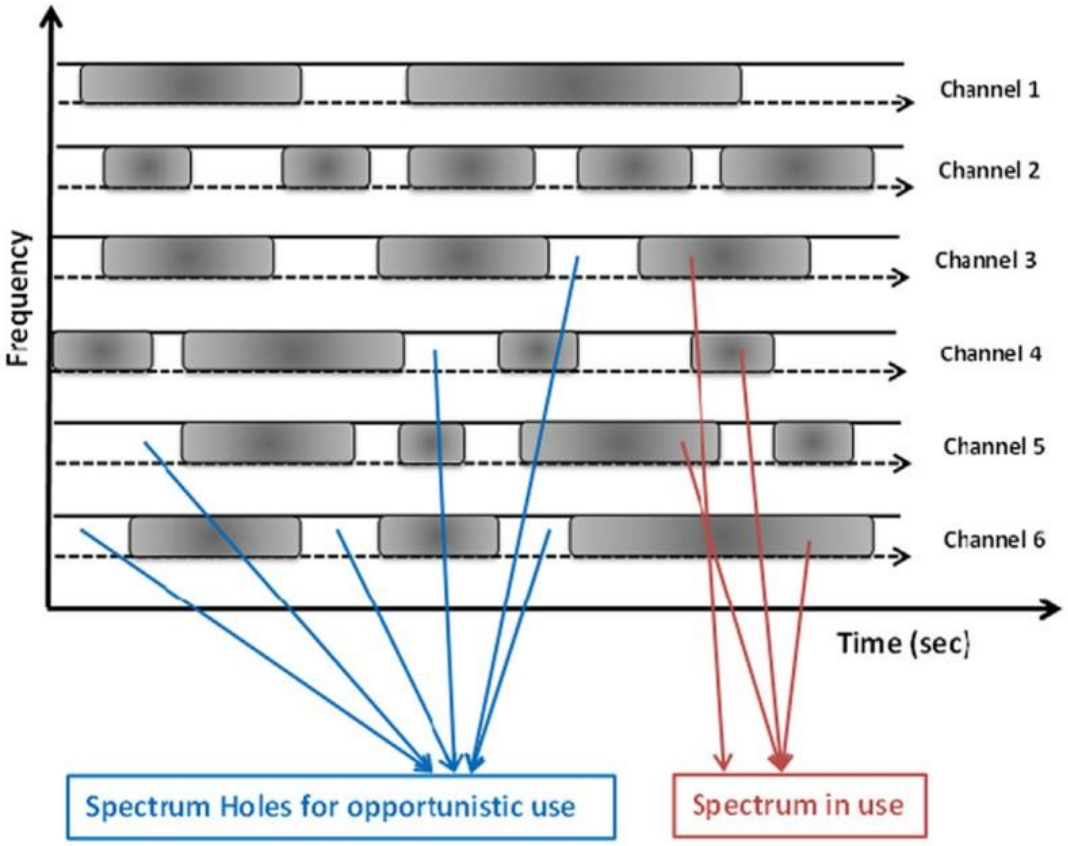


Figure 4-1. A strawman figure showing the inefficient spectrum occupancy, taken from [45].

4.2 Design

One way of designing mechanical filters for cognitive radios is to have parallel branches of filters in a bank similar to the self-healing filter concept. In this case, we introduce by design a frequency shift between each filter branch so as to enable filtering operations discretely at multiple neighboring frequencies so as to cover a wider frequency range. This very same system could also be realized fully via SES tuning, but in order to cover a wide frequency range via SES either a much larger array size or extended SES (ESES) technique proposed in [46] with a substantially large array would need to be employed as discussed in [38]. Since we demonstrate

this system on a PCB via wire-bonding and use MEMS only process for the fabrication of AlN MEMS filters, and considering the system complexity and high parasitics associated with PCB routing and off-chip CMOS components, we make the design of the system through an array of AlN MEMS filters operating at fixed discrete frequencies.

Conceptually, considering the variations in the center frequency of each of these filter branches in the programmable filter array, we would need to create a separate filter bank of identical sub-filter elements for each operating frequency. Then, we should apply the SES technique to each filter branch in order to be able to finely tune the center frequency of each filter channel in the programmable array. Again, because of the hardware demonstration complexity on a PCB, we realize this proof-of-concept system with a single set of filter bank consisting of channels designed to operate at multiple frequencies without the SES capability.

4.2.1 Conceptual Circuit Diagram

As discussed above, we design a programmable filter array covering discrete frequencies within a certain frequency range. The array consists of filter elements which can operate selectively at multiple frequencies. Similarly to previously shown filters in this thesis, each filter is comprised of three cascaded two-port AlN MEMS CMRs connected in series. In order to turn on/off the filters in the array, we use a switchable shunt capacitor (C_{off}) at the joint nodes of these cascaded resonators (see Figure 4-2). In order to resonate out the capacitive behaviors of the filters in the off-state and/or operating over different center frequencies, we need to use a shunt inductor to the ground at both RF input and output (see $L_{RF,inout}$ in Figure 4-2). Based on the number of channels this inductance value could be very small (*i.e.* in the order of 100s of pH to few nH) and might be easily designed on a CMOS chip. Though, as the operating frequency range increases, its value should increase accordingly (discussed in Chapter 4.2.2.2 in detail).

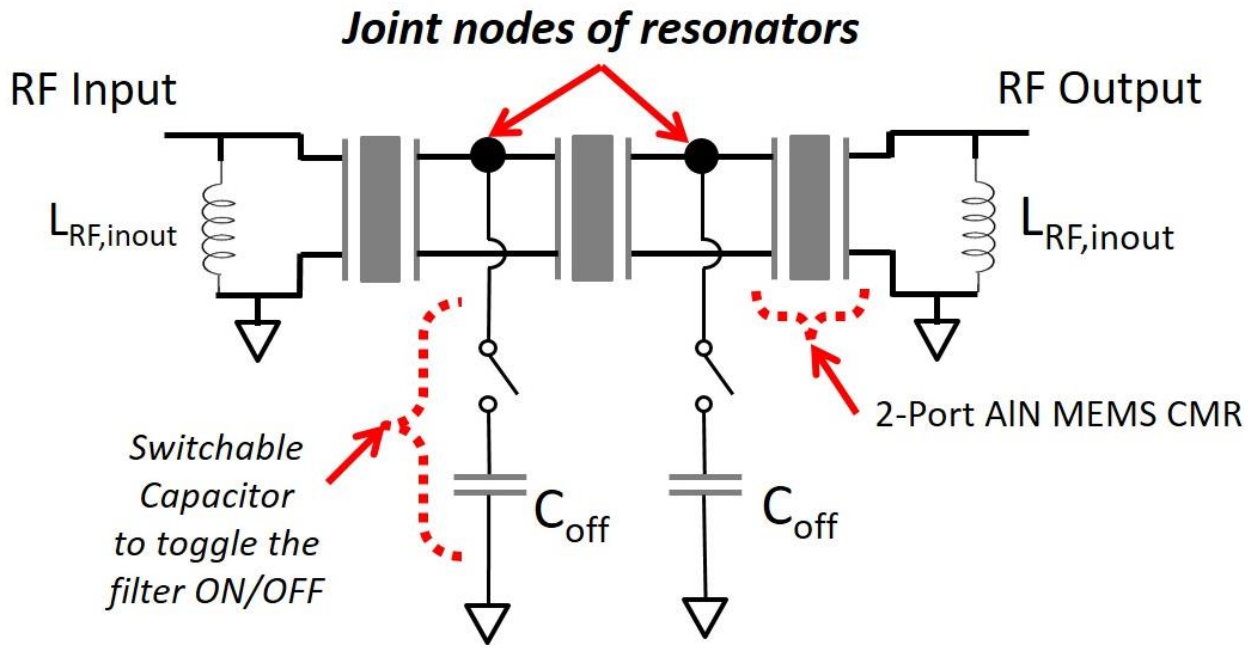


Figure 4-2. Switchable capacitor approach to toggle the filters on/off in each filter branch of the programmable filter array.

In this approach and differently from what shown in Chapter 3, we toggle the filter on/off by means of coupling/de-coupling the cascaded resonators in the filter. We accomplish this through the switchable shunt capacitors (C_{off}) following the methodology provided in [47]. In a way we can say that when the switches are turned on, C_{off} artificially reduces the k_t^2 of the resonators and thus lowers the amplitude of the second and third poles in the filter passband, effectively squeezing them closer to the first pole (see Figure 4-3 for the corresponding pole locations in the filter passband). In turn, this approach effectively degrades the performance of the filter passband. If the value of this shunt capacitance is properly adjusted in conjunction with the whole switching circuit (discussed in Chapter 4.2.2.2 in detail), the amplitude of the filter response associated with the first pole is also getting significantly degraded, hence effectively providing for sufficient signal rejection (*i.e.* the filter is turned off).

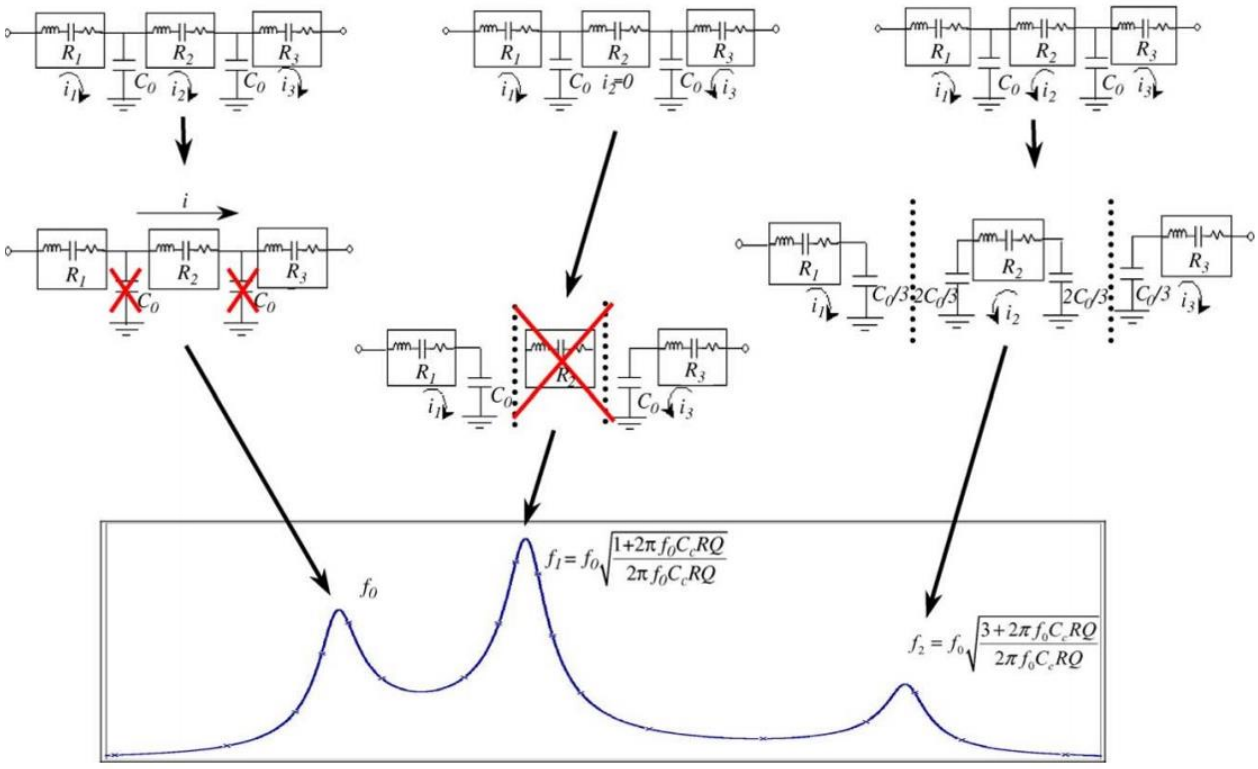


Figure 4-3. Electrical schematic diagram of three poles of the three cascaded resonator (third-order capacitively coupled) filter and the corresponding frequency response (taken from [6]). The resonant frequencies are also shown on the frequency response where f_0, f_1 and f_2 represent, in order, the frequency of first, second and third poles in the system.

When compared to the filter selection method provided in Chapter 3.1.1, the switchable shunt capacitor approach becomes more favorable since we eliminate the losses of series CMOS switches and series interconnect routing losses while electrically wiring the CMOS switches to the AlN MEMS chip. This does, in turn, lower the *IL* arising from the switching process and related signal routing when compared to the performance of the RF switches in-series with the RF signal path. Though, a shunt inductor at RF input and output is needed in order to resonate out the capacitive behavior of the filters in off-state and/or operating at other frequencies.

Note that the same switching technique could also be employed for the SES tuning self-healing filters demonstrated in Chapter 3. Considering the 3D hybrid AlN MEMS and CMOS chip stack

with MEMS RDL signal routing, this switching technique would result in fewer bonding pads (*i.e.* only two bonds per filter branch instead of four given that the ground connection is shared between AlN MEMS and CMOS chips in the stack). Additionally, this could even enable lower *IL* in filters as the bonding pads and CMOS switches are no longer in series with the RF input-to-output signal path as mentioned above. Furthermore, since in the self-healing filter that we demonstrated in Chapter 3 the bulk of the parasitic shunt capacitance to ground at the RF input and output comes from the CMOS switches and bumping pads, this filter switching technique would also help us decrease this capacitance significantly in the self-healing filters. However, the capacitance coming from the filters in the off-state and operating at other frequencies still requires a shunt inductor to ground. Another downside associated with capacitive switching is the reduction of the filter bandwidth and some degradation in *IL* because of the off-capacitance of the switchable shunt capacitor, which inevitably loads the individual two-port AlN MEMS CMRs forming the filter (see Chapter 4.2.2.2). Clearly, trade-offs exist between the two approaches. This thesis effectively offer an initial comparison of these two switching methodologies.

4.2.2 Design Considerations

4.2.2.1 Design of AlN MEMS Filters for Efficient Programmability

When it comes to the design of these filters, there are a few critical aspects that we need to consider. First, the resonators in all the filter branches should not have any SM over the entire bandwidth of operations of the channels in the programmable filter array. This aspect is of vital importance for the filters in the array so that they exhibit minimal passband ripple. In the worst case scenario, the SM of one branch interferes with the passband of the other and generate some ripple. In order to showcase the potential detrimental impact of the SM when it overlaps with the passband of the filter channels, we created a Verilog-A model of the spurious mode and introduced artificial spurs into the response of ideal resonators in the simulation environment. As a-proof-of-concept, we designed only two filter branches at 1.15 GHz and 1.18 GHz,

respectively, meaning that we introduced a frequency shift of 30 MHz between the channels. We also assumed a Q of 1500 and k_t^2 of 1.5 % for the resonators of both the filter branches. We made the amplitude of spur high enough to distort the filter response when it overlaps with the passband. The impact of the SM can be seen in Figure 4-4 and Figure 4-5 in which the SM of one filter is away from or overlaps with the passband of other filter. Since our selected resonator in Chapter 2.6 has only one SM and that lies just outside the passband (see Figure 2-20), it could be employed in the design of these discrete programmable filters in the array if the placement of filters in the frequency spectrum is made by keeping the location of these spurs in mind. However, if SES or ESES techniques were to be employed in the design of the programmable filter array, we would have required a different resonator design without any SMs in the operational span of frequency spectrum as it would have continuous coverage of the spectrum instead of a discrete one.

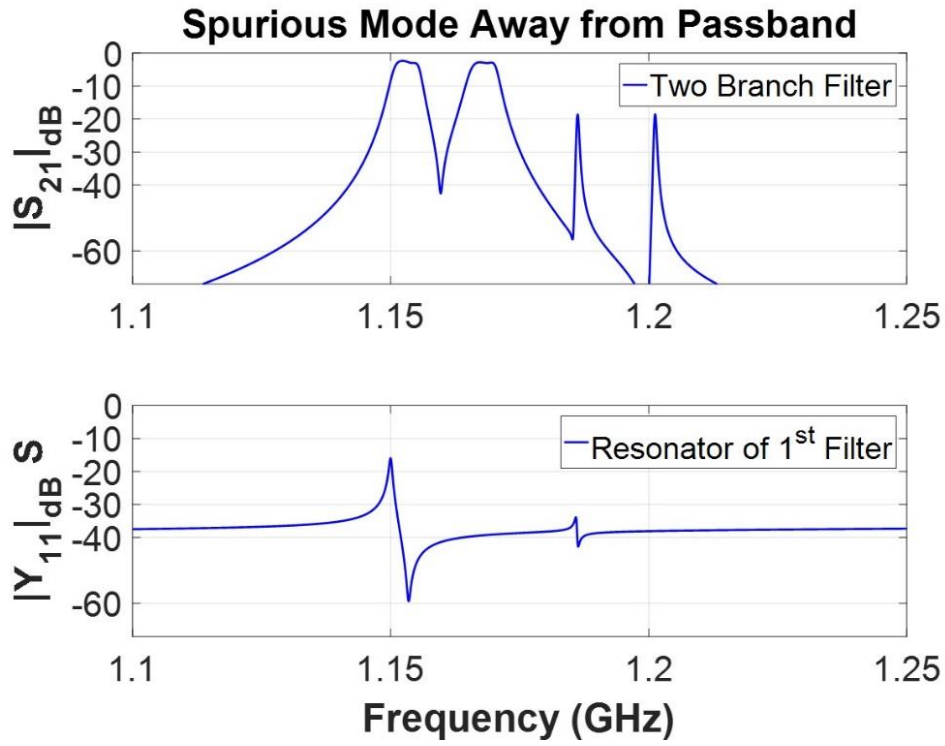


Figure 4-4. Two branch programmable filter array simulation with resonator spurious modes away from the passbands of the filters.

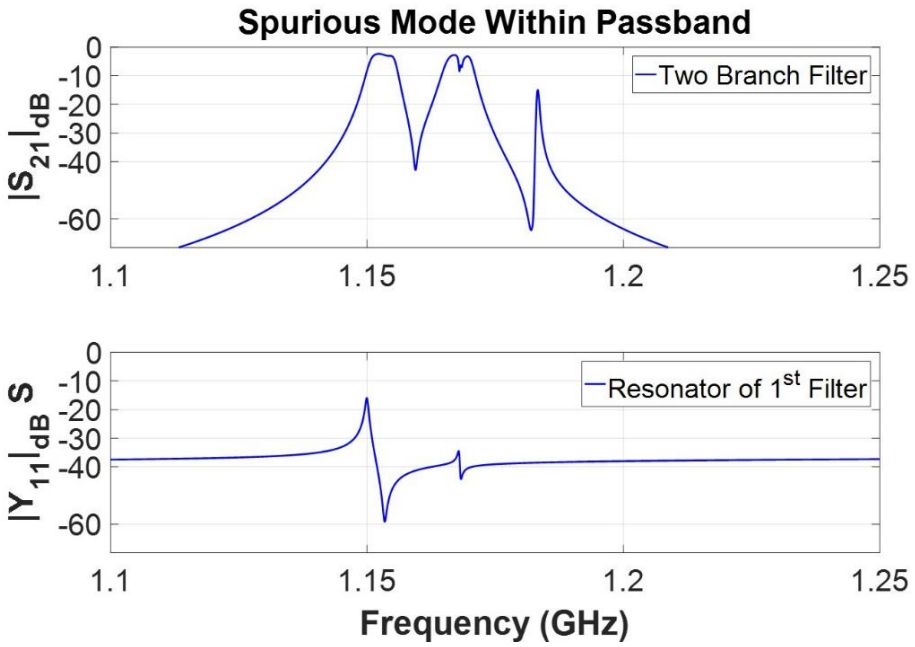


Figure 4-5. Two branch programmable filter array simulation with 1st filter resonator spurious mode within the passband of the second branch filter.

Secondly, we need to provide a certain frequency shift for each branch along with a C_o change in order to have similar matching network for each selectable filter branch. When we look at the frequency shift mechanisms provided in [48]-[53], we selected to analyze two geometrical parameters given the range of corresponding frequency shifts that can be achieved, the size of the resonators and related changes in C_o. These are i) electrode coverage, W, and ii) electrode pitch, P, which were previously shown in Figure 1-1. To this end, we ran FEA simulations on a 2D geometry based on the material stack provided in Figure 2-2. The model includes the cross-section of the resonator body along with metallic IDTs and bottom metal electrode of the selected resonator geometry. The geometrical parameters, W and P, were varied in these simulations in order to produce the required frequency shift. When P was varied, W was also altered to preserve 50% electrode coverage of AlN (so as to avoid variations in the device k_t^2 [21]). The resulting frequency shift and C_o change for each of the varied parameters are shown in Figure 4-6 and Figure 4-7. Since P has the primary effect on the frequency setting of these kinds of resonators, its

small changes cause higher frequency shift as expected. Opportunely, frequency shift is inversely proportional to the changes in C_o for both approaches (almost inverse linear relationship), so we do not have to modify the resonator further for impedance matching at different frequencies.

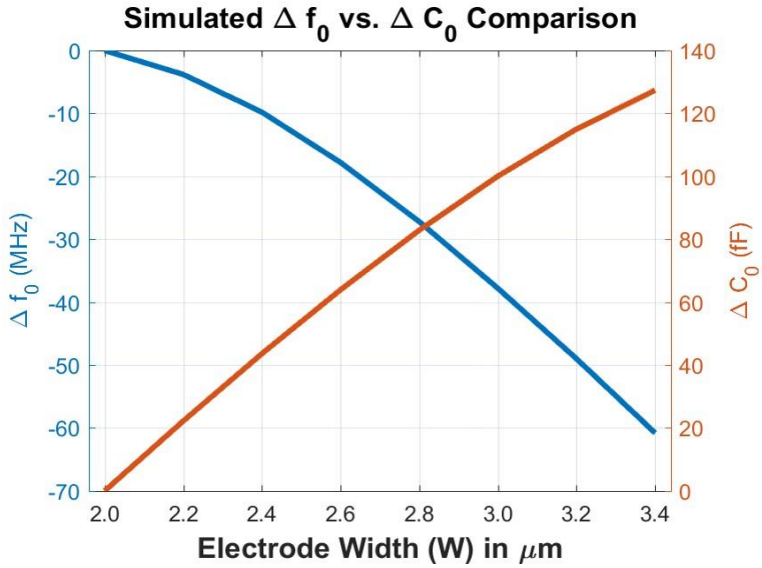


Figure 4-6. Center frequency shift and C_o change for various W values based on FEA simulated data using a cross-sectional 2-D model of a 2-port AlN MEMS CMR, having 25 fingers with *OE* of 0 μm.

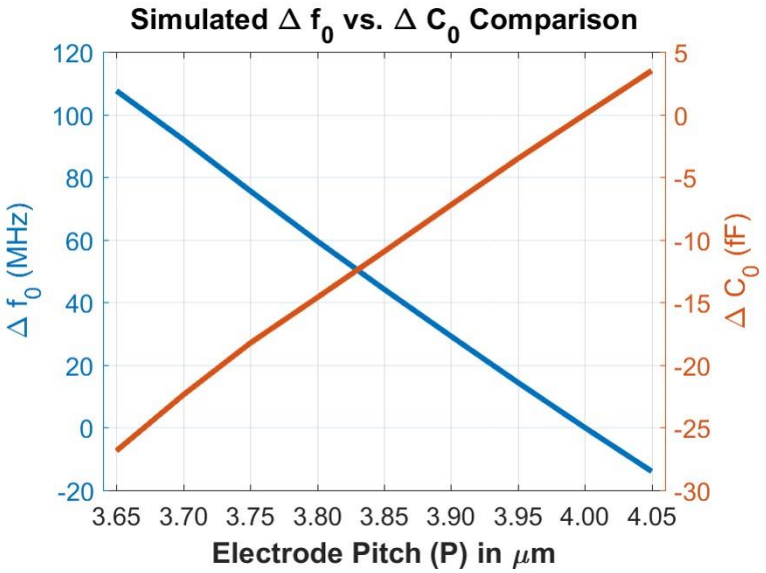


Figure 4-7. Center frequency shift and C_o change for various P values based on FEA simulated data using a cross-sectional 2-D model of a 2-port AlN MEMS CMR, having 25 fingers with *OE* of 0 μm.

Finally, in order to make sure that we do not introduce any new SM or move the existing one into the pass-bands of selectable channels while introducing the frequency shift, we also checked the admittance responses of these resonator geometries in the FEA analysis. In Chapter 2.2.2.2, we have shown that the parameters in the direction transverse to the main mode of vibration do not impact the relative location of SMs. Thus, we can use the same set of 2D FEA simulations also to analyze the SM location and amplitude changes as the resonator geometry is altered. Figure 4-8 and Figure 4-9 shows the resulting admittance responses of the resonators for varying *W* and *P* values, respectively. According to our circuit simulations, a 3 dB peak to peak amplitude of SM can cause a ripple of about 1 dB in the passband in the worst case scenario when it overlaps with the passband of other filter branches. As seen from the figures, SMs are within this limit for *P* from 3.75 μm to 4 μm and for all the simulated *W* values. Therefore, we can employ either parameters for this particular resonator design in setting the relative frequency shift in the filter branches.

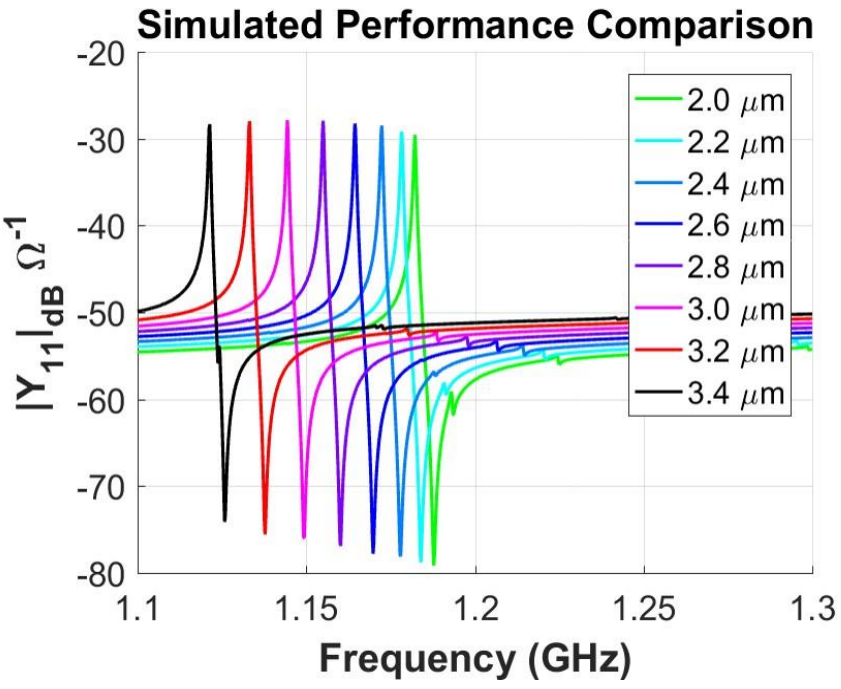


Figure 4-8. FEA simulated resonator admittance responses for varying *W* values.

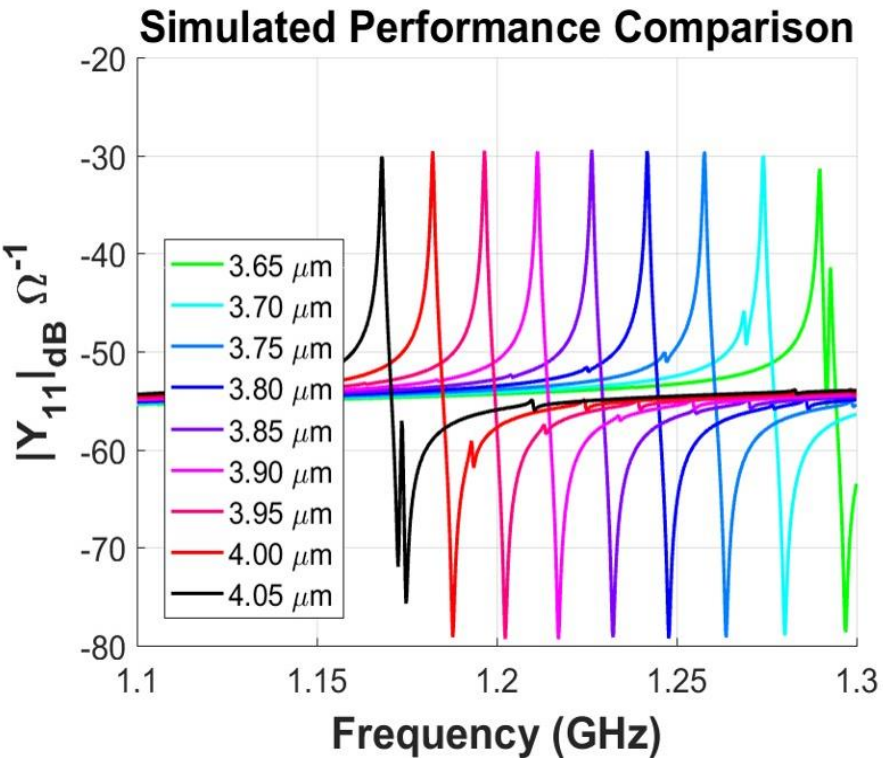


Figure 4-9. FEA simulated resonator admittance responses for varying *P* values.

4.2.2.2 Methodology to Select CMOS Components

First design constraint in the selection of CMOS components is the proper sizing of the transistors being used as a switch at the joint nodes of the resonators forming the filter. In order to ensure no performance degradation in the filter when the transistor is in the off-state, the shunt capacitance of the transistor should be either sufficiently small when compared to the combined capacitance of the resonators at the joint node ($\ll 2\ C_0$) or resonated out with a shunt inductor to ground at the same node. Similarly, in order to achieve the highest possible de-coupling between resonators when the transistor is in the on-state, the series impedance of the transistor should be as small as possible.

In order to showcase the impact of the series turn-on resistance of the switch on the filter off-state, we used the ideal circuit model for the switch and generated a set of filter rejection curves versus C_{off} for various values of the turn-on resistance of the switch, *i.e.* R_{switch} (see Figure 4-10 for

the simulated circuit model). For resonators, we used the equivalent circuit model provided previously in Figure 1-2 with turns ratio of 1 and without C_f and assumed Q of 2000 and k_t^2 of 1.5 %. The C_o of resonators is set to 1.8 pF in this simulation. The rejection in filters is defined with respect to 0 dB point in the $|S_{21}|_{dB}$ response versus frequency. As seen from Figure 4-11, the rejection in the filter saturates as the value of C_{off} increases when we have non-zero series resistance. Also, the rejection value decreases as the series resistance increases. This is in-line with theoretical expectations because the impedance of C_{off} becomes comparable to R_{switch} as the value of C_{off} increases and thus C_{off} has a limited control on the poles. Since the rejection requires capacitive behavior as discussed previously, the real part of the impedance of the switching circuit limits the highest achievable rejection by switchable shunt capacitors in turning the filter off.

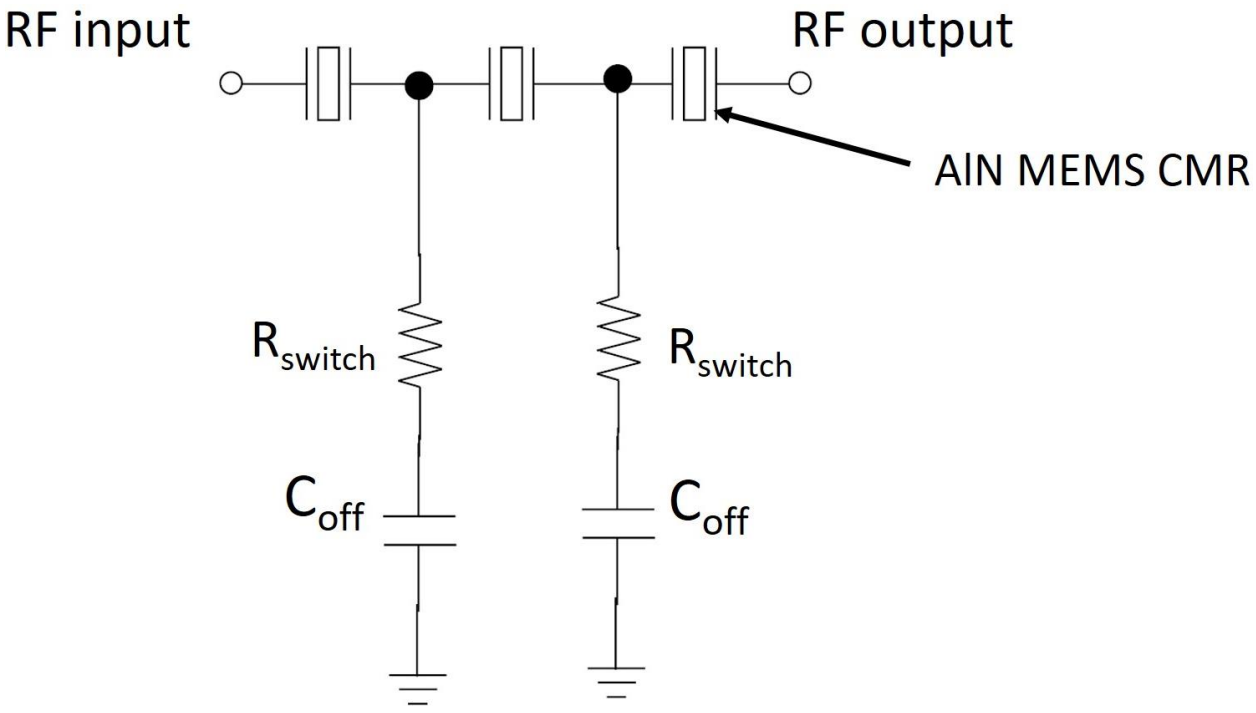


Figure 4-10. The schematic of the simulated circuit in the generation of rejection curves versus C_{off} for different values of switch on-state series resistance, R_{switch}. The corresponding simulation results are provided in Figure 4-11.

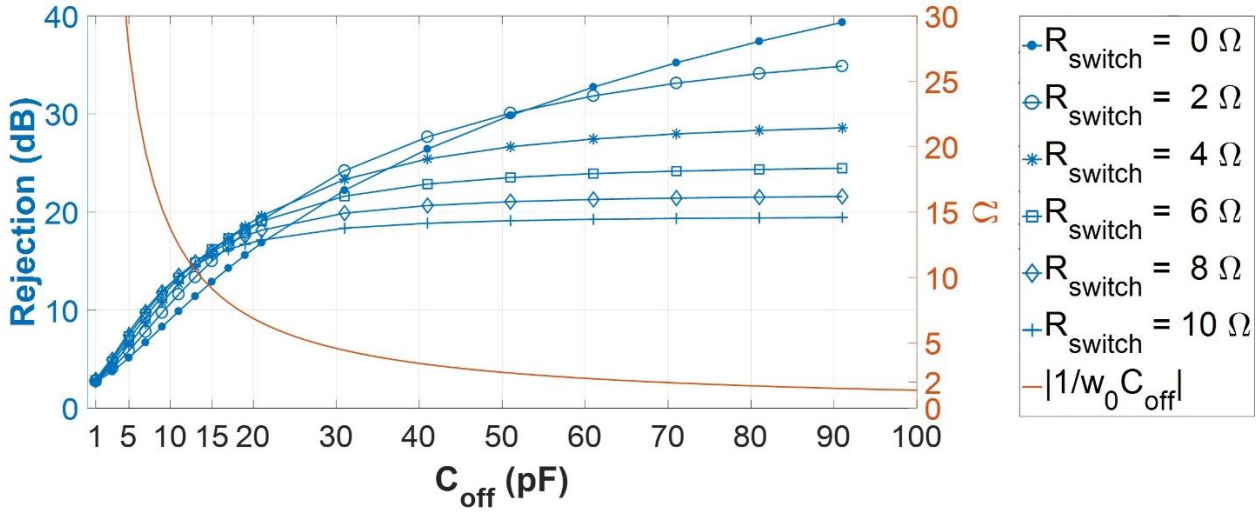


Figure 4-11. The filter rejection curves versus C_{off} for different values of switch on-state series resistance, R_{switch}. The absolute impedance of C_{off} at 1.16 GHz is also shown on the same graph.

Additionally, there should be a shunt inductance at the input and output port of this programmable filter array to resonate out the capacitive behavior of the filters operating at the other frequencies and provide appropriate matching to 50 Ω. Since the impedance of the inductor is also frequency dependent, the shunt inductor size should be determined separately for each operating frequency for ideal impedance matching. Though, if the frequency range covered by the programmable filters is kept within 10 % of f_o, the same shunt inductor value would provide similar impedance matching for each filter branch with a difference in *IL* of less than 0.3 dB between the worst and best matched filter branches. The losses of this inductor, which primarily impact the *IL* for all the filters in the arrray, should also be taken into account in the design. According to our circuit simulations, for a programmable filter array of five filter channels matched to 50 Ω, the shunt inductor with a *Q* of 100 (Abracon AISC-0805HQ) has an impact on the IL of all the filters of 0.3 dB

4.2.3 Design Implementation

4.2.3.1 Single Channel Filter Design

Considering the design constraints of AlN MEMS CMRs, we chose a frequency separation of 15 MHz between filters (channels) with five separate filter branches. The first filter operates at 1.105 GHz and the last one at 1.165 GHz (*W* equals to 2.0 μm in this case). In order to match to 50 Ω terminations we formed an array of four identical sub-filters connected in parallel to synthesize each filter branch. Because the pitch has a higher impact on the relative location of the SMs (see Figure 4-8 and Figure 4-9), we used *W* in setting the frequency shift. Since we have anti-symmetric modes in the selected resonator geometry (see Chapter 2.6), the increase in *W* would help reduce the amplitude of such spurs, as well [54]. The *W* values we used for the programmable filter array are 2.00, 2.53, 2.84, 3.11 and 3.36 μm, in order, for the five filter branches. As seen from Figure 4-9, these responses do not have SMs within the resulting passbands.

The devices are fabricated through a MEMS only process with Al UBM at A*STAR, IME, Singapore. A channel of the arrayed filter design can be found in Figure 4-12 where four identical sub-filters are connected in parallel to match 50 Ω termination. Since there is no RDL, we had to make the ground lines wide enough to limit the series resistance and provide good ground connection all around the devices. Similarly, we used UBM layer for the electrical connection of the joint nodes of resonators of parallel connected sub-filters so that the series resistance is minimized and higher rejection in the filter off-state could be achieved as discussed above. However, the critical distance for the width of the UBM was 20 μm and top Mo enclosure of UBM was 5 μm, which were dictated by the MEMS only process flow and provided by A*STAR, IME, Singapore. Because of these constraints and the need for low resistance both at the ground connections and joint nodes of the resonators, we had to route the signal and ground terminals in a way that they overlap at multiple locations and thus create a parasitic capacitance to ground at the nodes where we connect the CMOS circuits to AlN MEMS devices. This solution does not only

reduce the performance of the filter when it is in the on-state, but also decreases the amount of shunt capacitance needed at the joint node of the resonators to turn the filter off. This issue, which could be avoided if a full AlN MEMS process with RDL was available, becomes one of the limiting factors in the PCB level demonstration of this system (see discussion in Chapter 4.3.3).

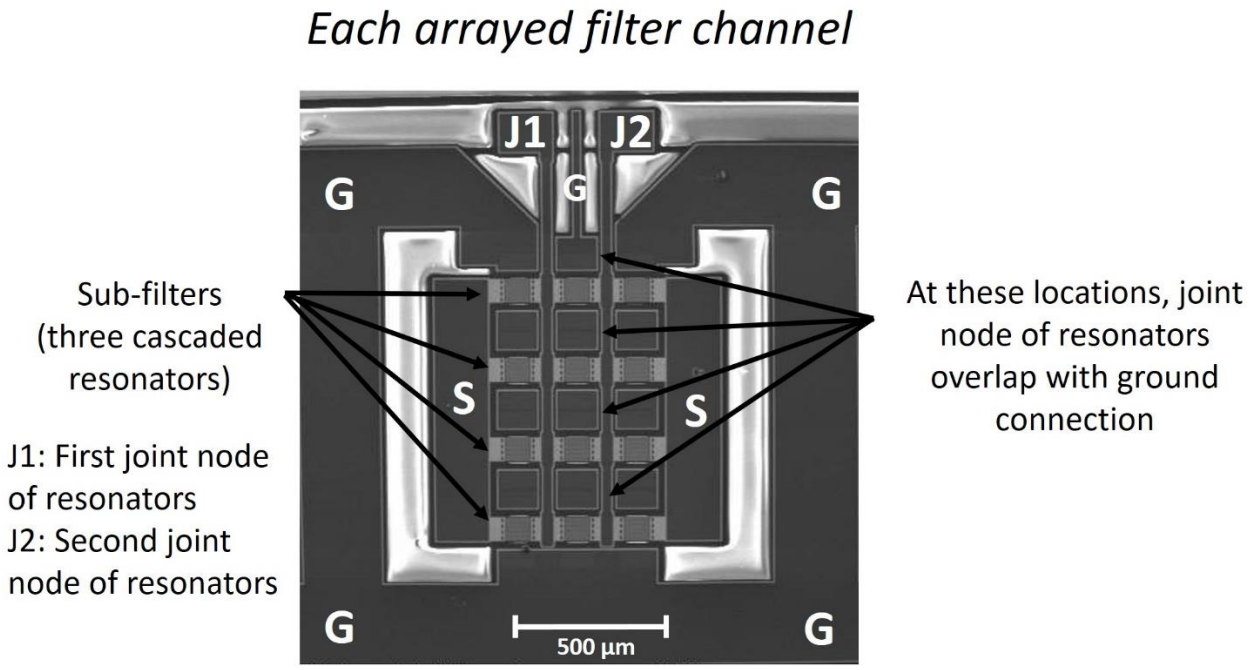


Figure 4-12. Aerial SEM image of a sample arrayed filter channel. On the figure, the electrical connections as well as subfilters are marked. Also, the high capacitance locations are clearly indicated. In these areas the RF signal overlaps with the ground terminal.

4.2.3.2 Realizing the Switching Circuit using off-chip CMOS Components

In the selection of switches, we looked for a single-pole double-throw (SPDT) configuration which has low turn-on series losses and high off-state isolation in order to toggle filters on/off effectively. The reason why we chose the SPDT vs. the SPST configuration is because it offered the lowest packaging parasitics.

We chose HMC194AMS8E from Analog Devices as the switch, which typically exhibits approximately 0.5 dB insertion loss and 45 dB isolation at the frequencies of interest (*i.e.* around

1.10 - 1.16 GHz). Using the measured s-parameter model of the switch provided by the vendor, we re-created the rejection curve in the filter off-state for various values of C_{off}. The simulated circuit can be found in Figure 4-13. For the resonators forming the filter, we used the equivalent circuit model provided previously in Figure 1-2 with turns ratio of 1 and without C_f and assumed Q of 2000 and k_t^2 of 1.5 %. The C_o of the resonators is also set to 1.8 pF in this simulation.

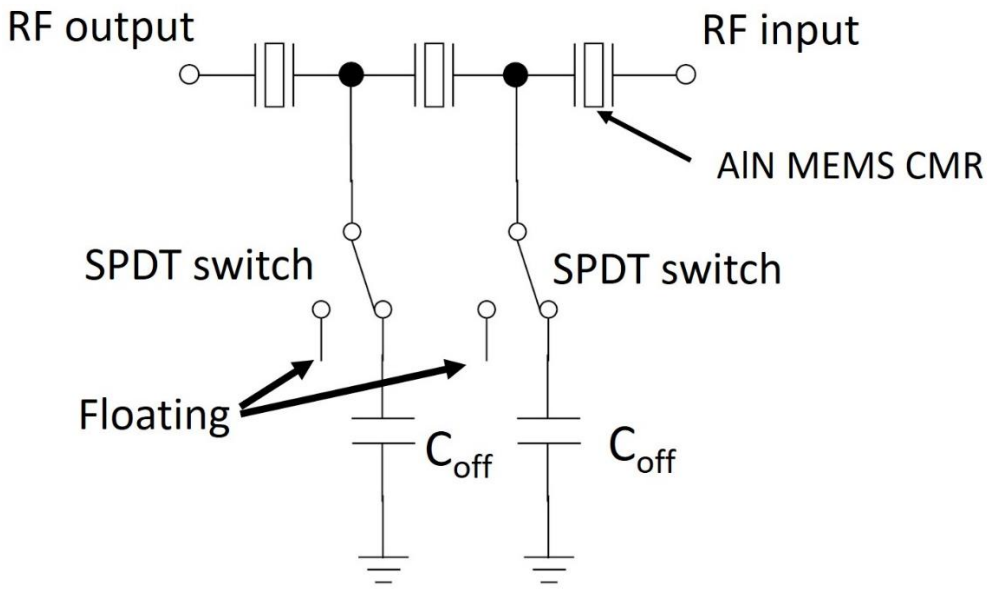


Figure 4-13. The schematic of the simulated circuit in the generation of rejection curve versus C_{off} in the presence of SPDT switch (measured s-parameter data obtained from the vendor were used). The corresponding simulation results are provided in Figure 4-14.

As seen from Figure 4-14, after reaching the upper limit in the rejection, the off-state performance of the filter degrades as C_{off} increases. This is because the switch also introduces some series inductance in the switch on-state, which makes the circuit appear inductive rather than capacitive as the C_{off} increases. Hence, while choosing the size of C_{off}, the series inductance coming from the signal routings, the wirebonds, the switch and the capacitor itself should be taken into account so as to attain the optimum rejection performance in the system level demonstration.

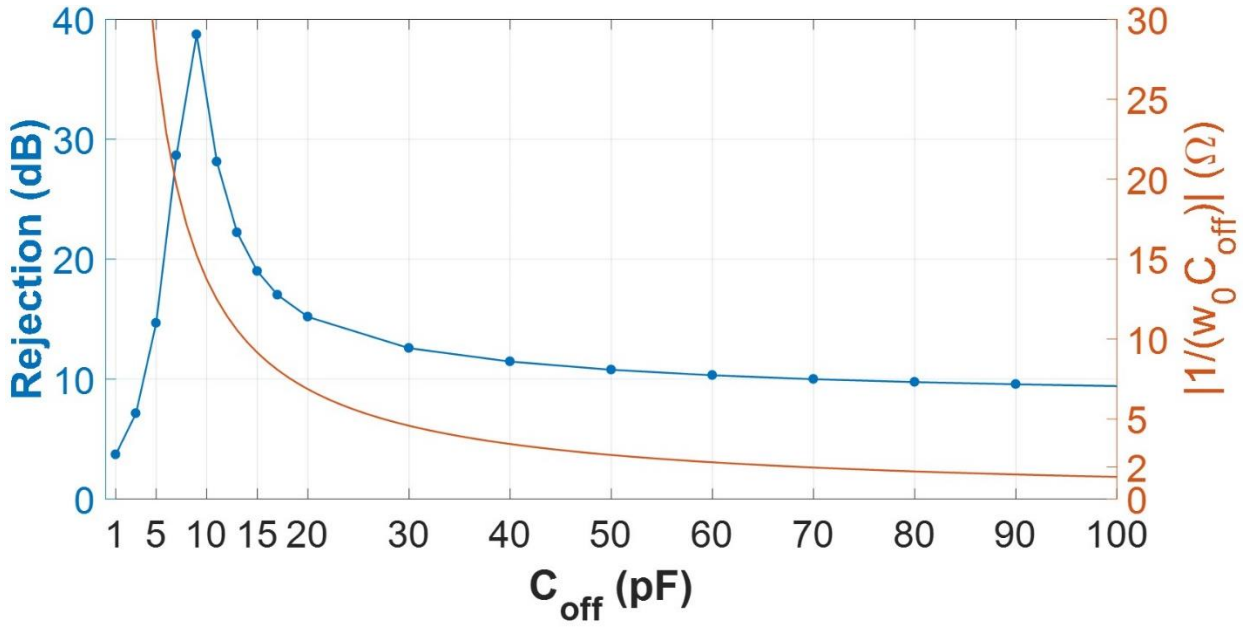


Figure 4-14. The filter rejection curve versus C_{off} when the measured s-parameter data of the selected switch is used in the simulation. The absolute impedance of C_{off} at 1.16 GHz is also shown on the same graph.

4.2.4 Full Circuit Simulation of the Designed Programmable Filter Array

We simulated the full circuit of the designed programmable filter array including the MEMS layout parasitics. In the simulations, we used ideal capacitors and measured s-parameters data for the selected off-the-shelf CMOS switches in the switching circuit. We also resonated out the capacitance at the RF input and output due to the filter channels. For this purpose we used a shunt inductor of 3 nH to ground at RF input and output ($L_{RF,inout}$). We assumed a Q of 100 (Abracon AISC-0805HQ) for these inductors and modeled the inductor loss with a resistance (R_{loss}) in series with the inductor based on the reported Q value at the center of the operational frequency, *i.e.* 1.135 GHz. We also included a feedthrough capacitance (C_{ff}) of 5 fF for each filter channel between RF input and output to reflect the non-idealities of the routing on AlN MEMS chip, as well as, a capacitor in parallel with the switching circuit ($C_{MEMS,\ layout}$) to represent the MEMS layout parasitics due to the unavailability of RDL layers as discussed in Chapter 4.2.3.1. We estimated

the value of $C_{MEMS,\,layout}$ to be in the amount of 1.5 pF for our MEMS chip design per filter channel. Again for the resonators forming the filter, we used the equivalent circuit model provided previously in Figure 1-2 with turns ratio of 1 and without C_f and assumed Q of 2000, k_t^2 of 1.5 %, and a C_o of 1.8 pF.

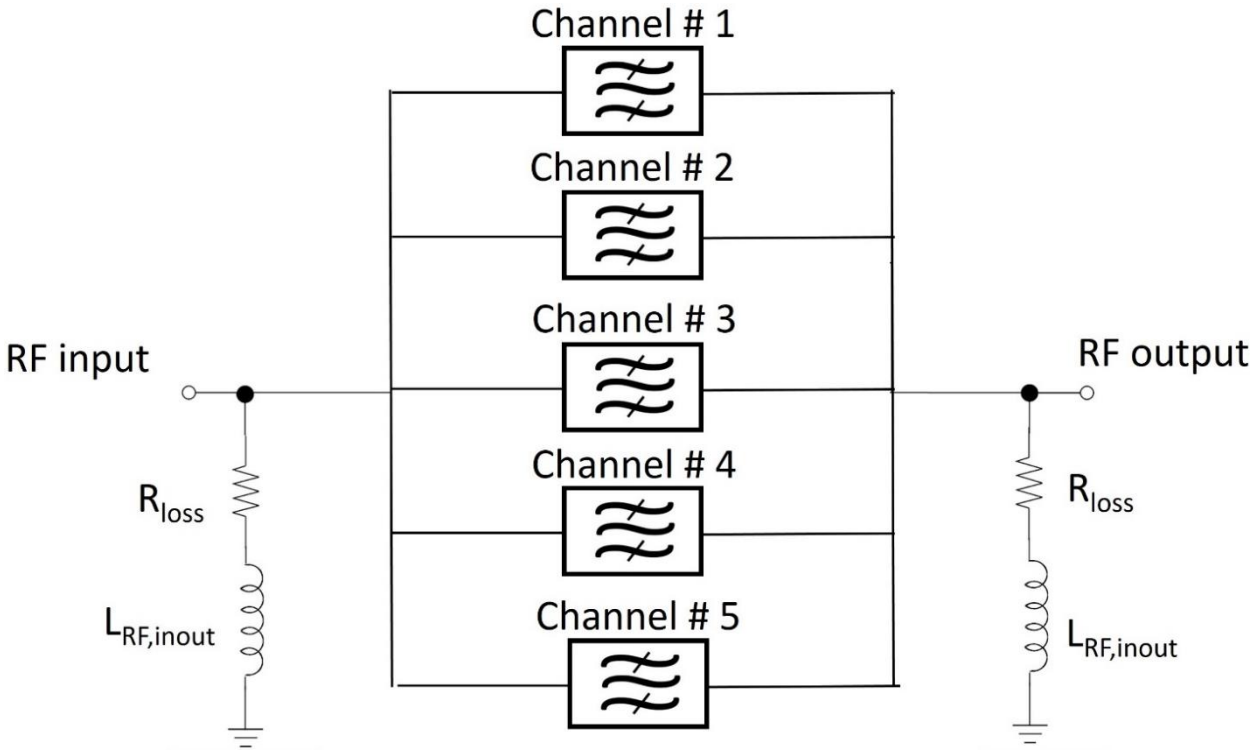


Figure 4-15. The schematic of the simulated full circuit including the AlN MEMS chip major layout parasitics. The schematic for each arrayed filter channel is provided in Figure 4-16. The corresponding simulation results are provided in Figure 4-17.

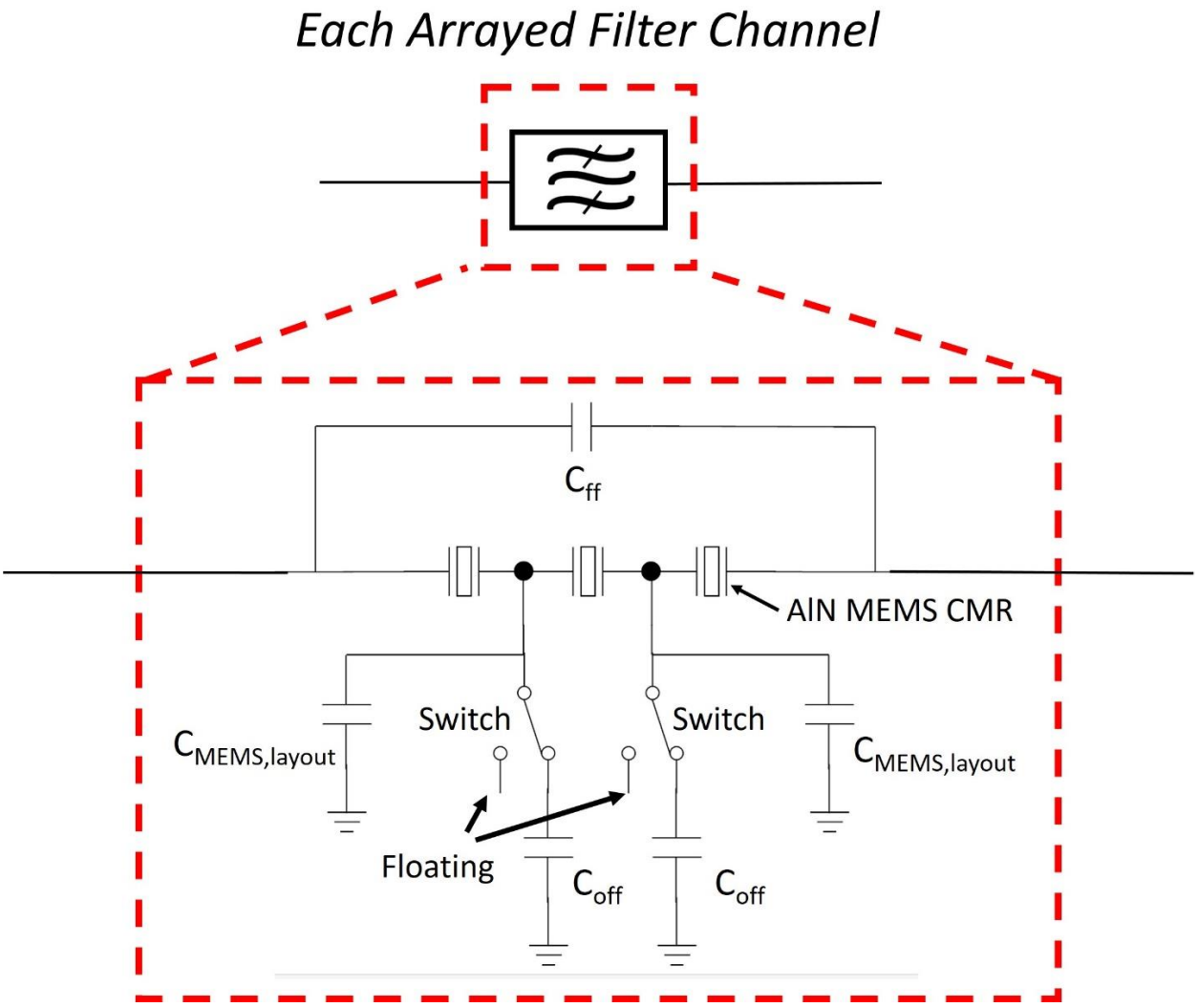


Figure 4-16. The simulation schematic for each arrayed filter channel. The schematic of the simulated full circuit including the AlN MEMS chip major layout parasitics are provided in Figure 4-15.

A couple of the available configurations in the simulated programmable filter array are shown in Figure 4-17. Considering all these parameters, we found out that C_{off} should be set to 8 pF for the optimum programmability performance in the filter channels. As seen from the figure, an *IL* of less than 4 dB for the on-state filter response and a rejection higher than 25 dB for the filters in the off-state are achieved in the circuit simulations for the designed programmable filter array at each operating frequency. Since the operating frequencies are limited to less than 10 % of the

center frequency, we also have the ability turn on/off multiple channels simultaneously with the same matching network with less than 0.1 dB difference in the *IL*s of the operating filter branches.

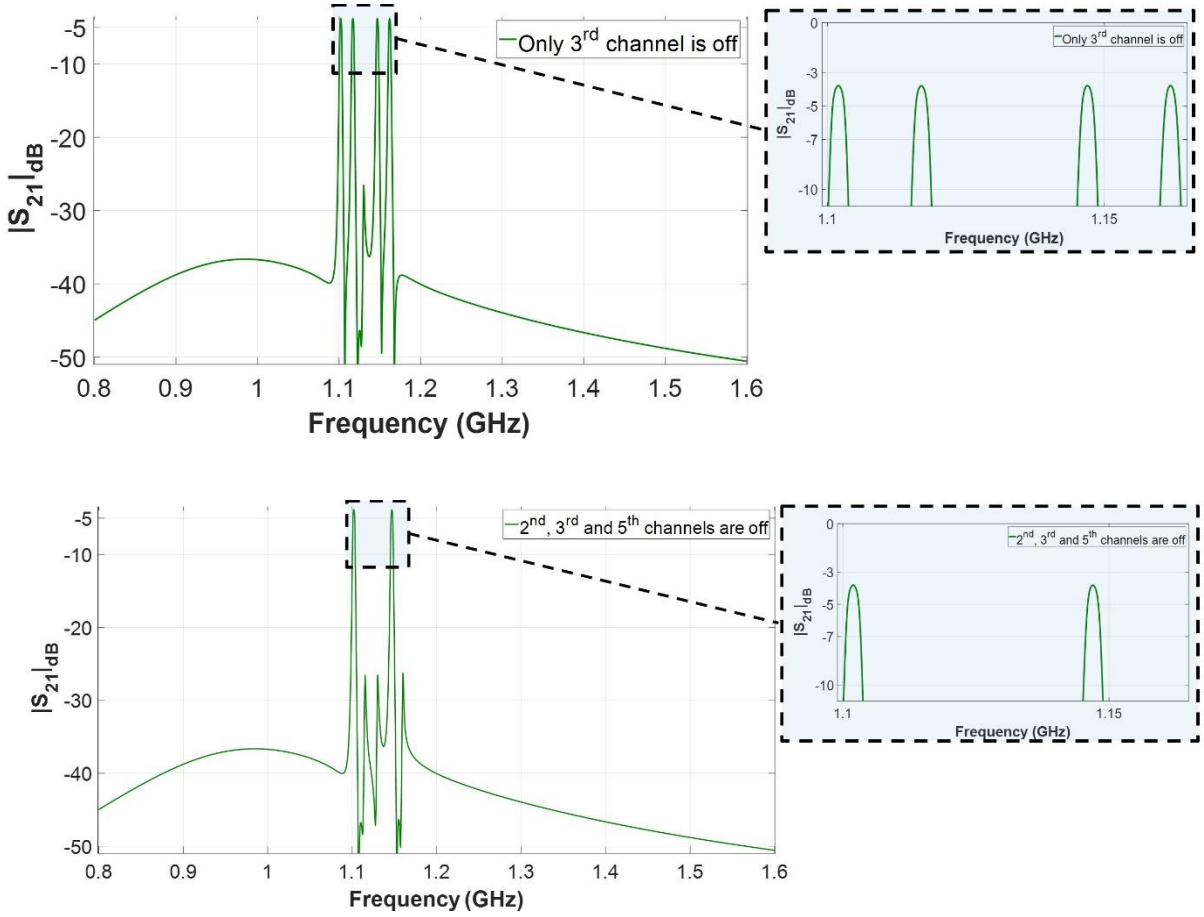


Figure 4-17. Simulated $|S_{21}|_{dB}$ responses of the full circuit including AlN MEMS chip layout parasitics versus frequency for a couple of configurations in programmable filter array when s-parameter data are used for the selected CMOS switches. The corresponding circuit schematics of full circuit and each arrayed filter channel in the full circuit are provided in Figure 4-15 and Figure 4-16, respectively.

4.2.5 PCB Design

The designed PCB layout and an SEM of the AlN MEMS filter mimicking the chip that will be wire-bonded to it are shown in Figure 4-18. In addition to the aforementioned circuit elements, we used RF/DC decoupling resistors of 50 kΩ in between the control voltages and the gate of the

SPDT switches. The manufactured PCB with AlN MEMS-CMOS signal interconnects via wirebonding is shown in Figure 4-19. We used a single sided PCB to limit the parasitics coming from the board (the board is made of FR4-G10 and has a thickness of 0.032" with 65 µm copper and gold coated contacts).

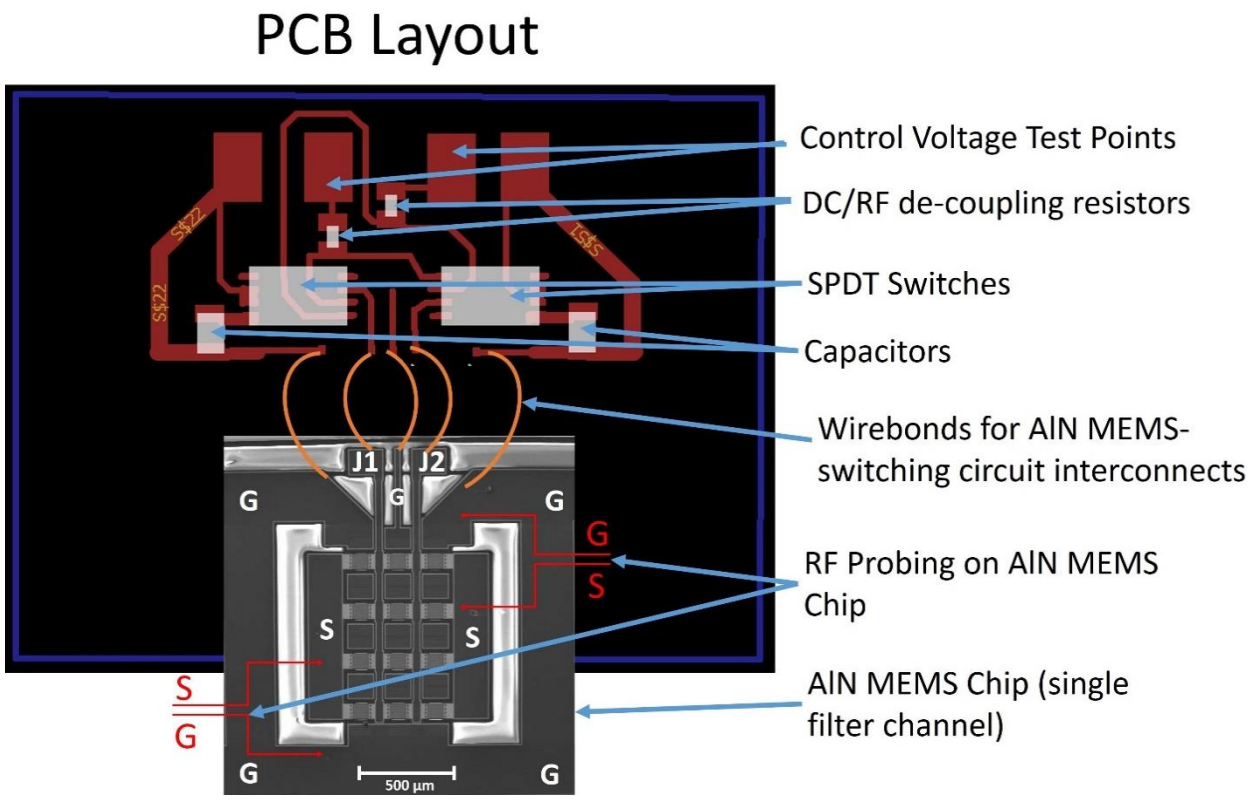


Figure 4-18. The designed PCB for turning on and off an individual filter array operating at a single frequency. Note that the drawings and AlN MEMS chip are not to scale.

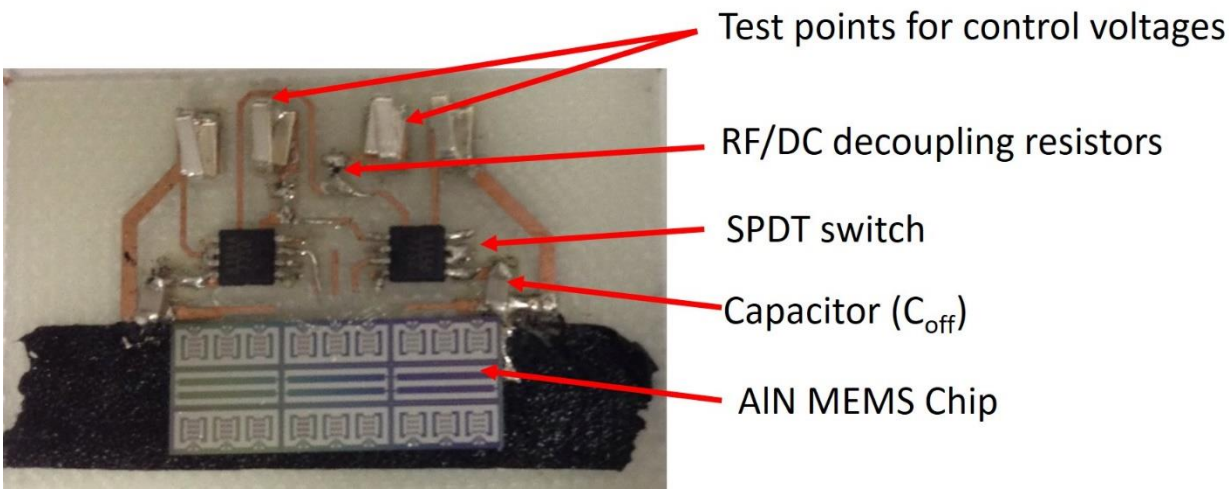


Figure 4-19. An image of the designed PCB with AlN MEMS chip wirebonded to it for turning on and off an individual filter array operating at a single frequency via the switchable shunt capacitors at the joint nodes of resonators forming the filter channel.

4.3 Experimental Measurements and System Demo

4.3.1 Fabricated Filter Channels

Figure 4-20 shows the individually measured arrayed filter channels designed with center frequencies ranging from 1.105 GHz to 1.160 GHz with the increments of 15 MHz. In other words, the center frequencies of channels ($f_{o,ch1}$, $f_{o,ch2}$, $f_{o,ch3}$, $f_{o,ch4}$, and $f_{o,ch5}$) are, in order, 1.100, 1.115, 1.130, 1.145 and 1.160 GHz. The frequency shift is provided with electrode coverage, W, which is set to 3.36, 3.11, 2.84, 2.53, and 2.00 μm, in order, for the five filter branches. All the other geometrical parameters are designed to be the same. All the measured filter data are acquired from the same die. Considering their relatively big size due to unavailability of the RDL process, the filter channels are placed in a 5 mm by 7 mm area on the AlN MEMS chip. This separation corresponds to statistical variations in the center frequencies of the filters, which indeed exhibited a non-uniform distribution of the center frequencies. As seen from Figure 4-20, the frequency separation between channels in the measured data ranges from 12 MHz to 15 MHz. For the other

parameters characterizing the filter behavior, Table 4.1 shows the extracted performance metrics of these filter channels.

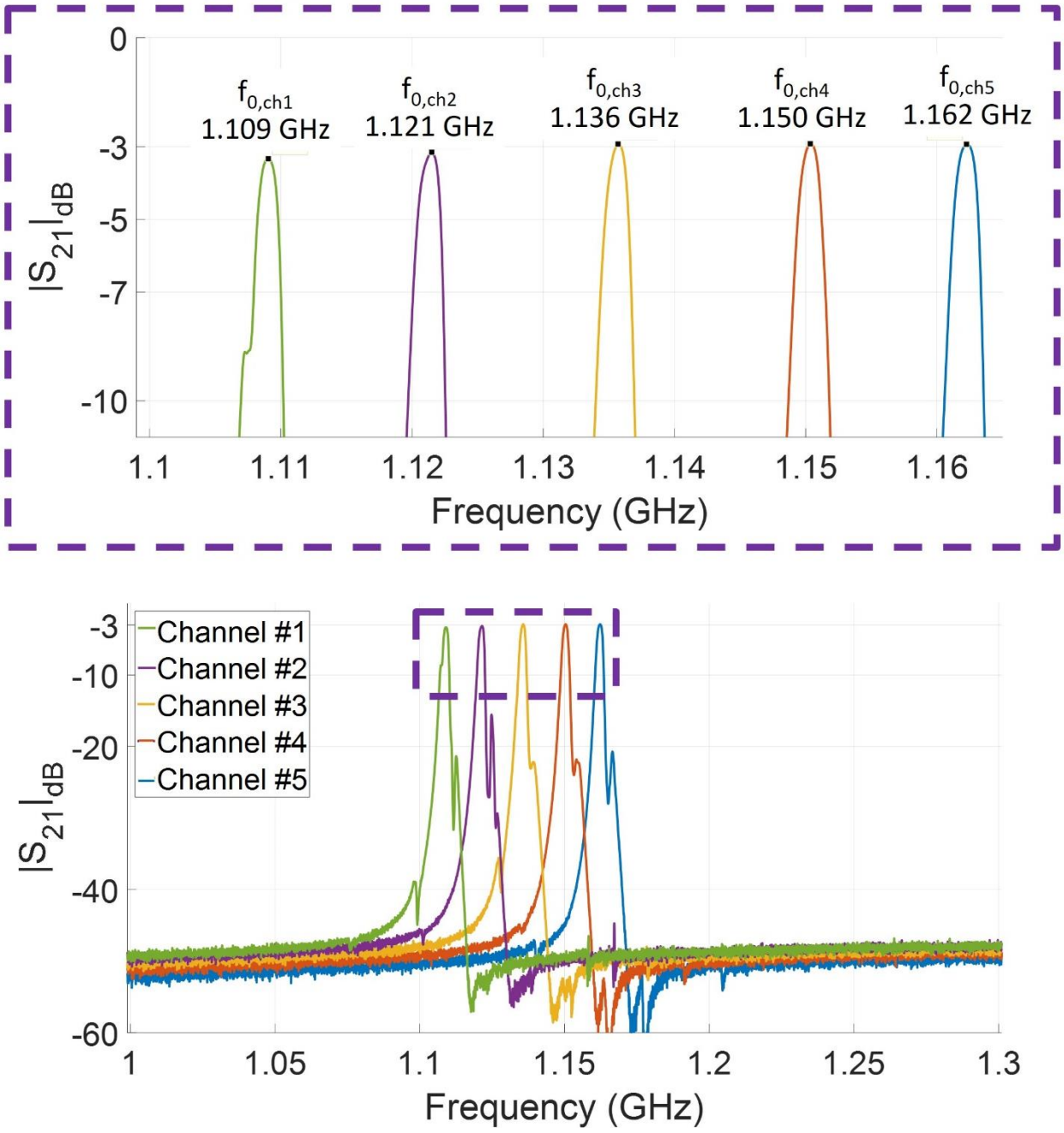


Figure 4-20. Frequency responses of individual arrayed filter channels with their corresponding center frequencies ($f_{o,ch1}$, $f_{o,ch2}$, $f_{o,ch3}$, $f_{o,ch4}$, and $f_{o,ch5}$) marked on the zoomed in $|S_{21}|_{dB}$ plot.

Table 4.1. Extracted performance comparison of AlN MEMS filter channels designed for the programmable filter arrays. The corresponding sample layout for each arrayed filter channel can be found in Figure 4-12.

Extracted Performance Metrics of the Arrayed AlN MEMS Filter Channels Designed for Programmable Filter Arrays				
Channel #	f_o **(GHz)**	***IL*** **(dB)**	***BW*** **(MHz)**	***OBR*** **(dB)**
Ch1	1.1090	3.23	1.90	17.39
Ch2	1.1213	3.05	2.05	20.63
Ch3	1.1356	2.93	2.05	20.30
Ch4	1.1503	2.92	2.10	21.24
Ch5	1.1622	2.93	2.10	22.31

The s-parameter response ($|S_{21}|_{dB}$) of the corresponding AlN MEMS filters can be found in Figure 4-20.

As seen from Figure 4-20 and Table 4.1, all the filter channels exhibit *IL* ranging from 2.9 dB to 3.3 dB. The main reason behind the additional losses with respect to the performance of the selected filter geometry (see Figure 2-21) is the aforementioned parasitic capacitance at the joint node of the cascaded resonators. Due to the unavailability of RDL routing, we used wide signal and ground metal lines overlapping each other at these locations in order to minimize the resistive differences among the sub-filters connected in parallel.

In order to illustrate the impact of the parasitic capacitance at the joint nodes of resonators to ground on the filter performance ($C_{MEMS,layout}$), we ran circuit simulations with the filters consisting of three cascaded two-port resonators by including these parasitic capacitances. We estimate the $C_{MEMS,layout}$ as 1.5 pF for this layout. We used the equivalent circuit model for the two port AlN MEMS resonators, which is provided previously in Figure 1-2. For simplicity, we

assumed a turn ratio of 1 (the exact value should be 0.923) for these resonators. As for the critical resonator parameters, we assumed a Q of 2500 and k_t^2 of 1.2 % for each of these resonators and set the C_o to 1.8 pF. In order to better showcase the out-of-band responses, instead of the resonator C_f, we introduced a feedthrough capacitance (C_{ff}) of 5 fF for the whole filter channel. The simulated circuit schematic in the presence of $C_{MEMS,layout}$ and C_{ff} is provided in Figure 4-21.

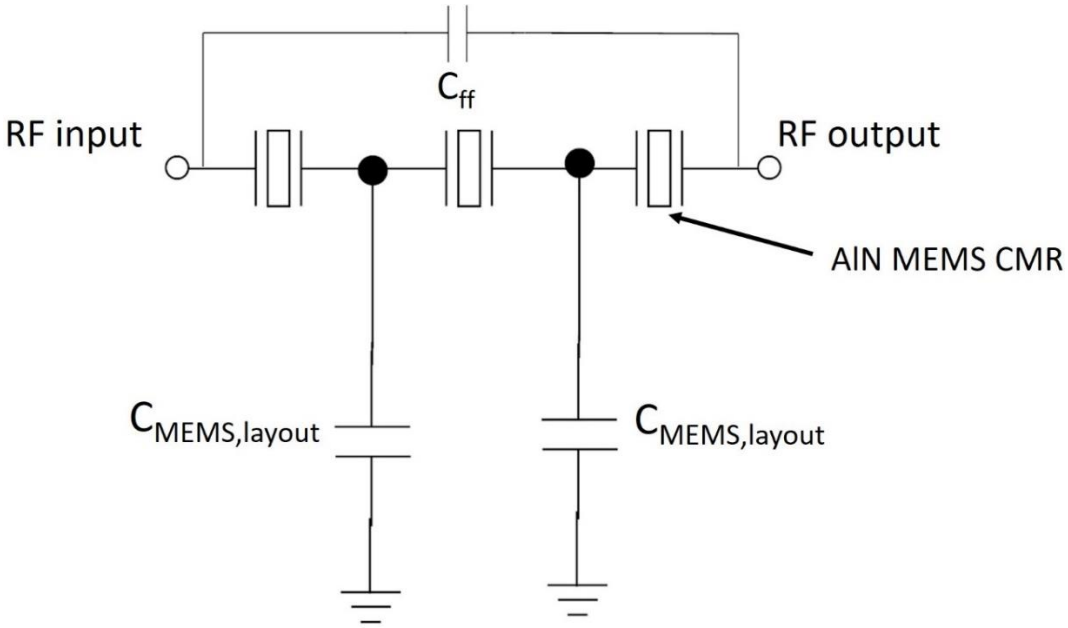


Figure 4-21. The schematic of the simulated circuit in the presence of the layout parasitic capacitance, $C_{MEMS,\ layout}$, at the joint node of cascaded resonators forming the filter. C_{ff} is also included in the model to better represent the out-of-band filter behavior when compared to the measured data. The corresponding simulation results are provided in Figure 4-22 in comparison with the measured ones.

The simulation data with and without the parasitic capacitance is provided in Figure 4-22 where the measured response of an arrayed filter channel is also plotted for comparison purposes. As seen from the figure, this capacitor degrades the filter *IL* and *BW*, which are in parallel with the measured response. This high parasitic capacitance issue at joint nodes of cascaded resonators is not relevant in the 3D integrated chip stack as it could be easily minimized with the use of RDL in AlN MEMS full process platform.

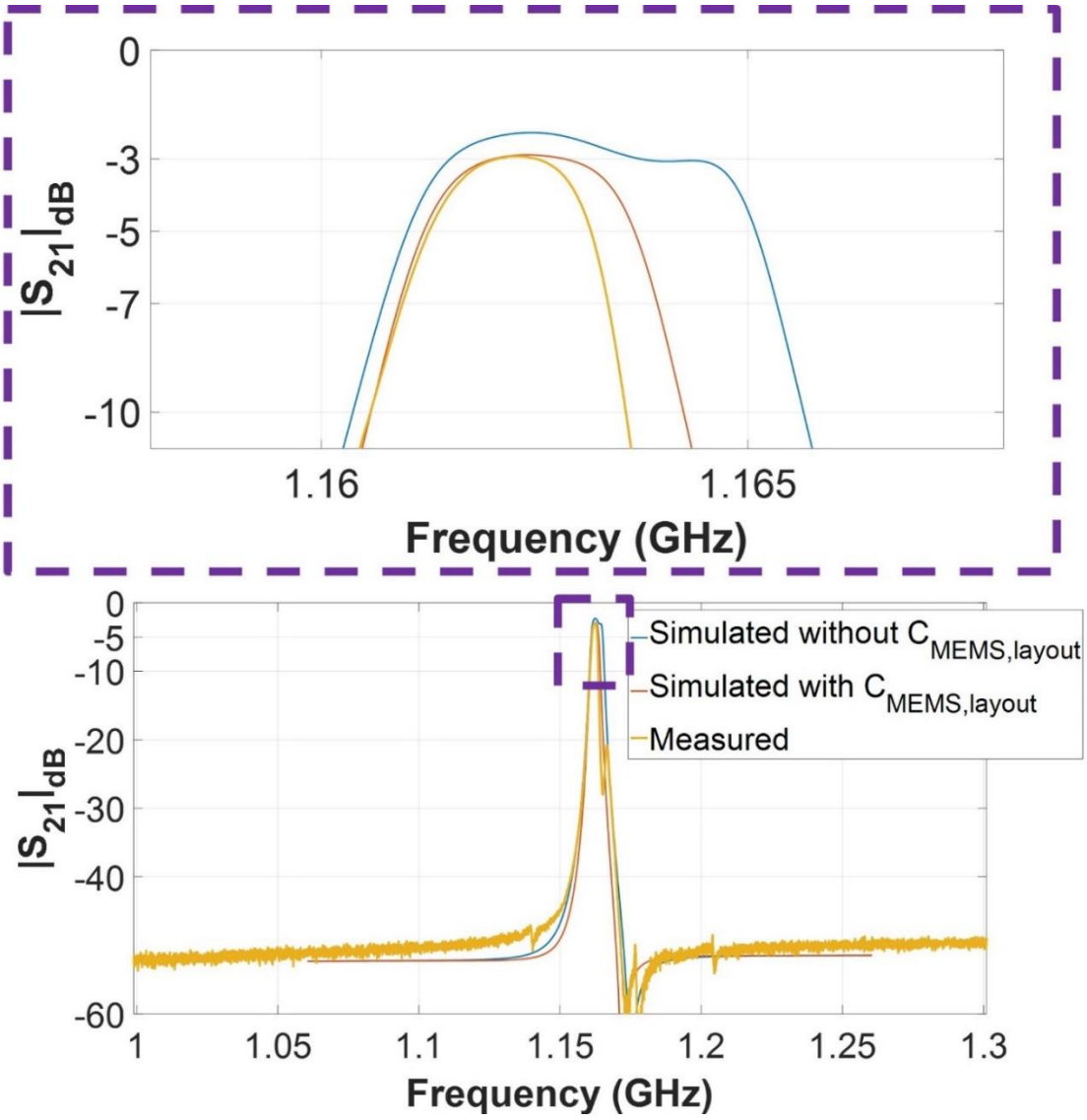


Figure 4-22. Simulated $|S_{21}|_{dB}$ responses of the filter channel with and without the estimated parasitic capacitance ($C_{MEMS,layout}$) at the joint nodes of resonators versus the experimentally acquired measured data. The corresponding circuit schematic of the filter with $C_{MEMS,layout}$ is provided in Figure 4-21.

There are also some secondary reasons for the lower performance in the filters, which are the shunt capacitance to ground at filter RF input and output and resistive losses coming from the signal interconnects and ground connections. We suspect that these could be the reasons behind the additional discrepancy between the simulated and measured data. Additional test structures modeling the quality of signal interconnects are needed for its verification.

4.3.2 Filter Array Response

The programmable filter array with five different operation channels is constructed using the experimental data of the individually measured arrayed filters in a simulation environment (see Figure 4-23). The extracted performance metrics of each channel filter after the integration are provided in Table 4.2. Basically, we have converted the s-parameters of the individually measured arrayed filter channels into y-parameters and summed them up since they are connected in parallel. We had to also include an inductor of 2.4 nH at the input and output of the RF signal to ground with a *Q* of 100 (Abracon AISC-0805HQ) in order to almost equally match the selectable filter channels (with an *IL* difference of less than 0.2 dB among the channels in the array). Since in the full circuit simulation provided in Chapter 4.2.4 we had to use a shunt inductor to ground at the RF input and output in the amount of 3 nH, we can say that the parasitics at these nodes are slightly higher than expected.

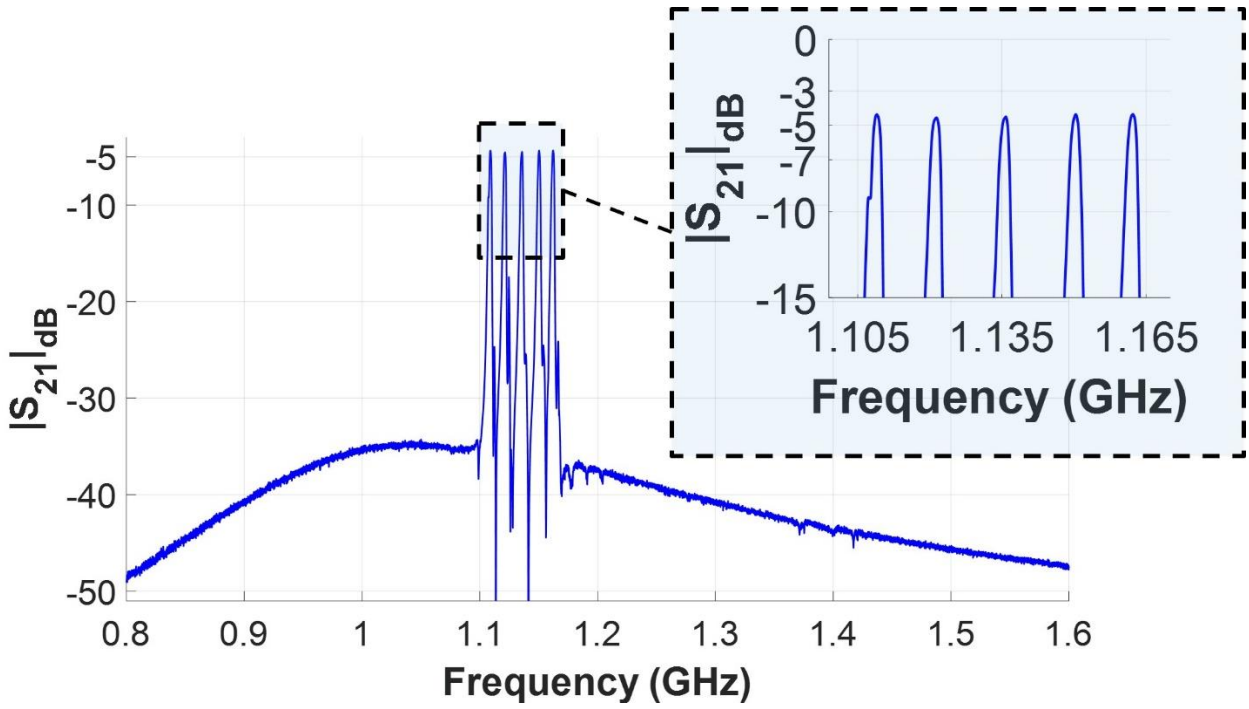


Figure 4-23. The programmable filter array with five different channels constructed using the experimental data of the individually measured arrayed filters.

Table 4.2. Extracted performances of the five AlN MEMS filter channel responses (shown in Figure 4-20) after they are integrated in a simulation environment with a shunt inductor of 2.4 nH whose Q is assumed to be 100.

Extracted Performance Metrics of the Measured Arrayed AlN MEMS Filter Channels after Their Integration in a Circuit Simulation				
Channel #	**f_o (GHz)**	***IL* (dB)**	***BW* (MHz)**	***OBR* (dB)**
Ch1	1.1090	4.37	1.94	18.15
Ch2	1.1212	4.54	2.16	21.57
Ch3	1.1355	4.49	2.16	21.31
Ch4	1.1502	4.36	2.18	21.67
Ch5	1.1621	4.35	2.18	22.47

The s-parameter response ($|S_{21}|_{dB}$) of the corresponding AlN MEMS filter array can be found in Figure 4-23.

As seen from Figure 4-23 and Table 4.2, the available filter channels are almost evenly distributed within the frequency range of interest (frequency separations are almost the same as those of the individual responses). *IL* of the channels increased by almost 1.5 dB when compared to the original individual response of each channel. The sources of this degradation are: 1) the loading due toother channels, 2) losses of the shunt inductors located at the RF input and output, and 3) matching to 50 Ω due to the use of a single inductor for all the channels. For all of these channels, the losses of shunt inductor have almost an impact of additional 0.3 dB in the *IL*. The impact of other two sources, though, are channel dependent. For example, for channel #3 (the filter in the center), the dominant contributor is the loading of other channels (1.2 dB); whereas, for the first filter matching contributes to the losses in *IL* in the amount of 0.4 dB while loading

causes a loss of 0.7 dB. In other words, as the separation of frequency between two filters decreases, the impact of loading increases.

The *BW* of the filters also slightly increased after the filter channels are integrated in the circuit simulation because the capacitive parasitics at the RF input and output were resonated out with the shunt inductors at the same nodes. As for the increase in *OBR*, since it is defined with respect to 0 dB, we can say that the sources are the same of those that cause the additional *IL* as the increase in *OBR* is comparable to the increase in *IL* of the filter channels.

As for the out-of-band response further away from the channel operation frequencies, almost 13.5 dB of the increase in the floor of the S_{21} comes from the feed-through add-up because of the parallel connections of the individual filters (in theory it should be almost $20\log_{10}(5)\approx14$ because of having five channels in the array). The rest of the change in the behavior (*i.e.* getting non-flat much sooner as getting away from the operating frequencies) comes from the presence of the shunt inductance at RF input and output ($L_{RF,inout}$) which is used to resonate out the channel capacitances and match the entire array. The floor in S_{21} just outside the filters response increases by an additional 4 dB because of the shunt inductance. These results and observations are in-line with the simulated channel array response shown in Figure 4-17 in the presence of C_{ff} and $L_{RF,inout}$. Small deviations arise from the values of inductances $L_{RF,inout}$ being different in the measurement integration (2.4 nH) and the circuit simulation (3 nH) due to the parasitics at these nodes being slightly higher than expected.

4.3.3 Switching Circuit Demonstration on a Single Filter Channel

Figure 4-24 demonstrates the turning on/off of a single channel filter using the switchable shunt capacitors built on the PCB with off-the-shelf CMOS components. The original filter channel response without the wire-bonding and PCB attachment is also shown on the same figure for comparison. As seen from the figure, the filter on-state response closely overlaps with the original filter response with no PCB attachment and wirebonding. Considering the operation

frequency, we might say that the small deviations in the performance come from the additional parasitics due to the PCB attachment. However, in the filter off-state response we achieved only a rejection of 18.4 dB (the upper limit was above 35 dB according to the simulation results provided in Figure 4-14). The reason was associated with the series resistive losses and series inductances of the wirebonds, PCB routing and CMOS capacitor along with the additional parasitic capacitance at the same node coming from the PCB routing. In order to minimize some of these losses, we did multiple wirebonds for each connection and used C_{off} of 0.2 pF (GJM15 series from Murata Electronics) in order to maximize the rejection in the filter off–state with the selected CMOS components and designed PCB. Given the level of inductances we had (8-10 nH at total) and additional parasitic capacitances, we could only achieve 18.4 dB rejection.

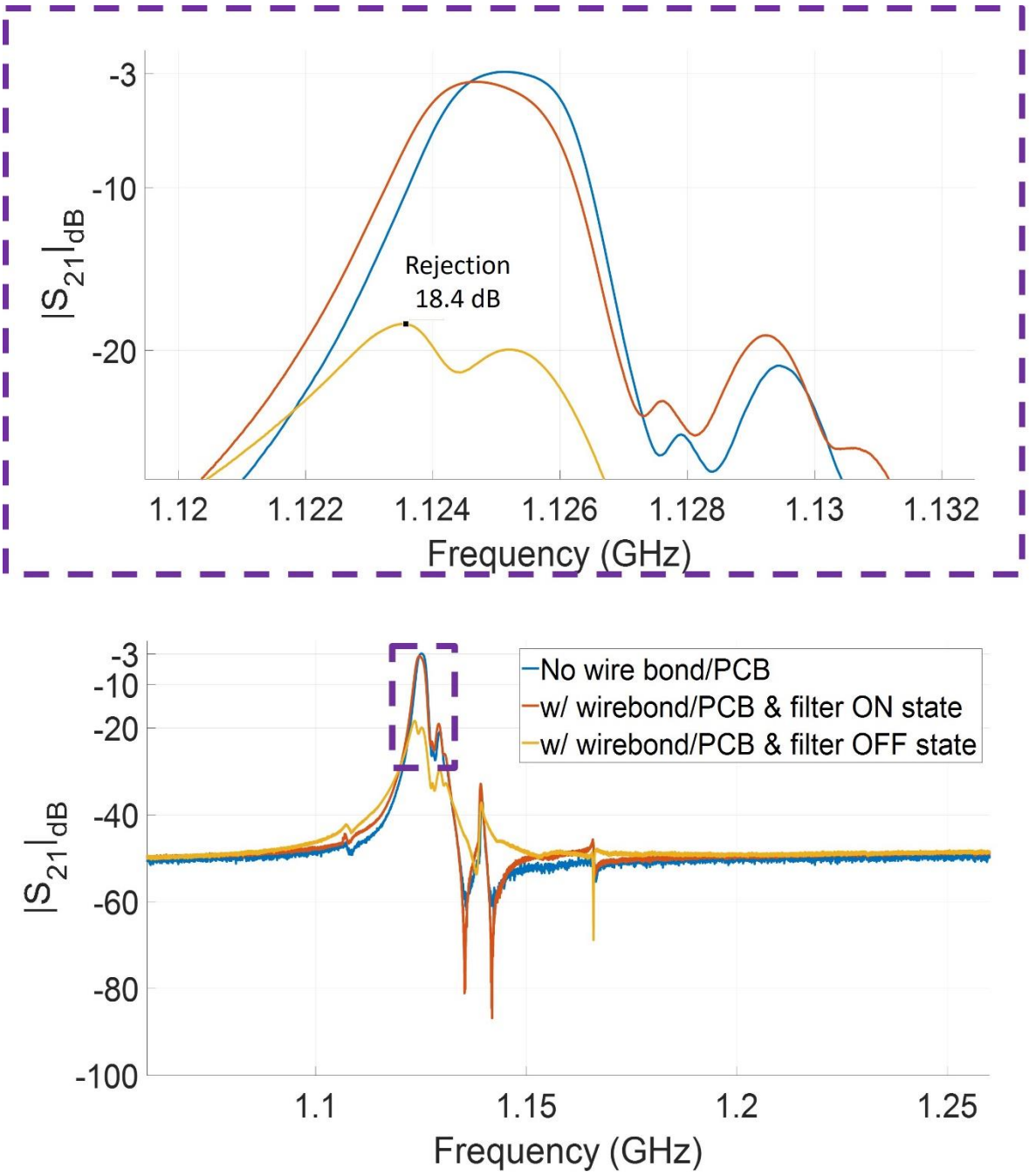


Figure 4-24. An individual arrayed filter turned on/off from the joint node of the resonators forming the filter. The original filter response without the wire-bonding and PCB attachment is also shown on the figure for performance assessment.

4.3.4 Discussions

In the process of finding this optimum value for the C_{off}, we also measured the level of filter rejections with various values of this capacitor (from the same class of these ceramic capacitors). The resulting curves can be seen in Figure 4-25 where the corresponding filter off-state responses are drawn along with the original filter response without the PCB attachment and the wirebonds. As seen from the figure, the rejection increases as the capacitor value decreases. We did not have a way to test for values of C_{off} between 0 and 200 fF, so we cannot exclude that a better rejection can be attained. Based on the acquired data points, we generated the rejection curve versus the value of C_{off} for the measured behavior as well (see Figure 4-26). Compared to the simulated one (*i.e.* Figure 4-14), the maximum rejection point moves toward lower values of C_{off}. As mentioned above, the reason behind this move is related to the level of series inductance and additional parasitic capacitance at this node. In other words, in order to get the same amount of negative reactance in the presence of these additional parasitics, the value of C_{off} should be decreased. Also, we do not see the optimum point (concave shape) in the rejection curve for the acquired data points. Therefore, there could be still some room for rejection improvement.

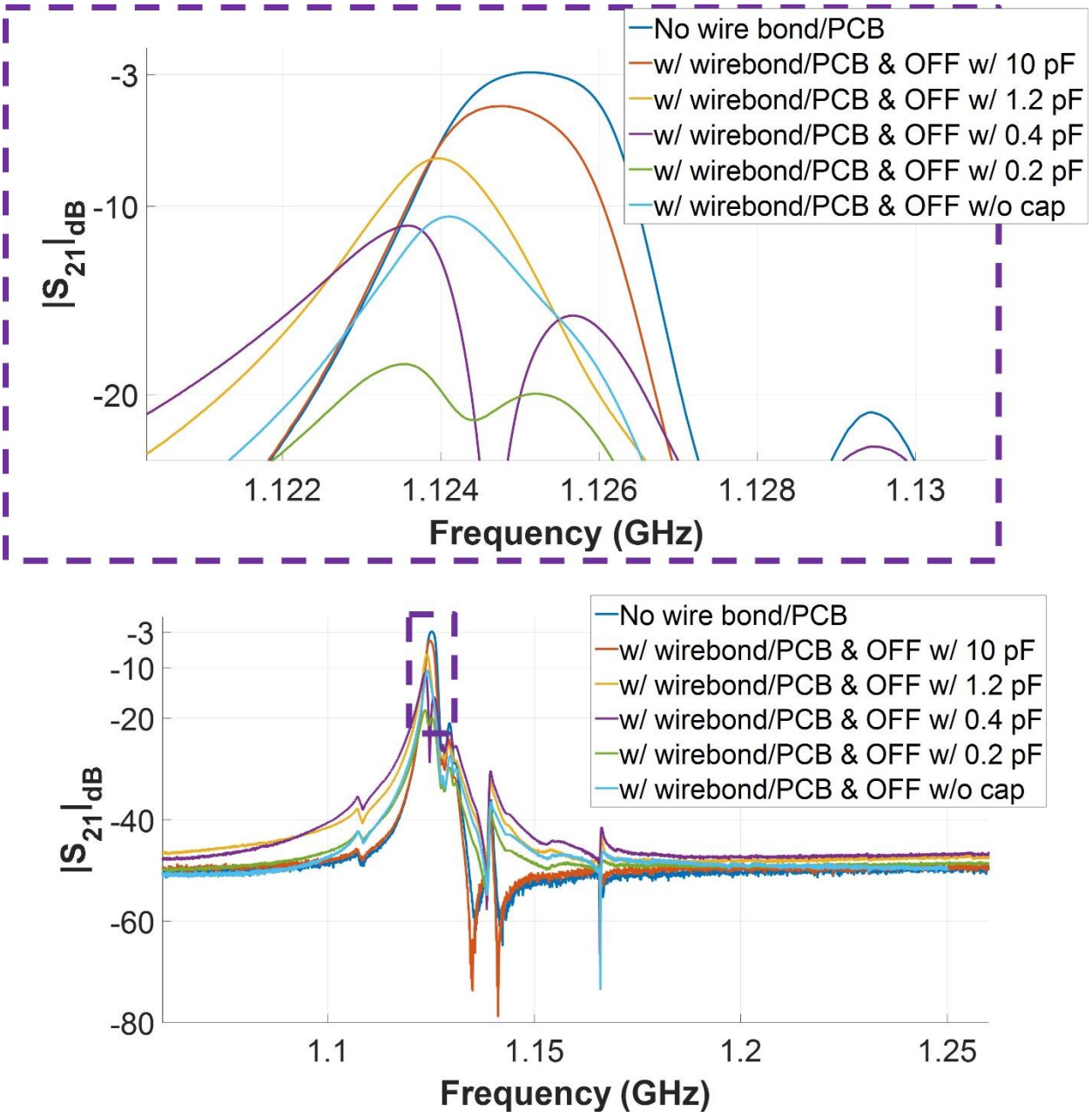


Figure 4-25. An individual arrayed filter turned off with different size capacitors from the joint node of the resonators forming the filter. The original filter response without the wire-bonding and PCB attachment is also shown on the figure for performance assessment.

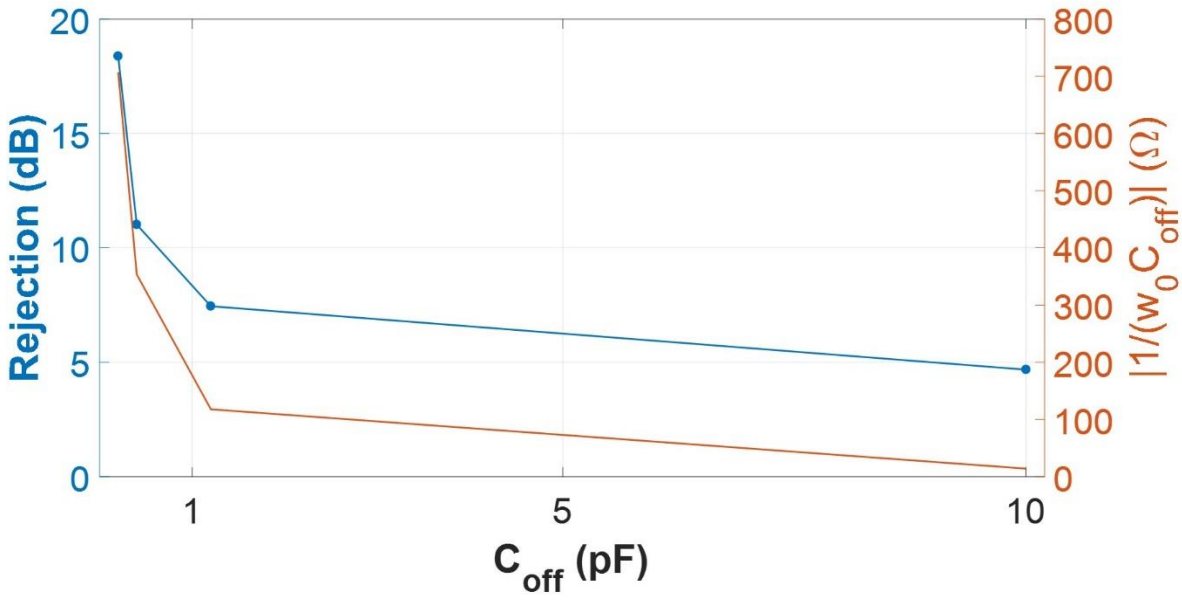


Figure 4-26. The filter rejection curve versus C_{off} generated using the measured responses provided in Figure 4-25. The absolute impedance of C_{off} at 1.125 GHz is also shown on the same graph.

In order to be able to quantify the amount of parasitics coming from different sources, we ran circuit simulations to match the measured responses. In this respect, we used the circuit schematic in Figure 4-27 where in addition to the previously defined parameters representing the losses, we also included the parasitics coming from the board, components and wirebonds, as well. Among these are series inductances ($L_{series,loss,before}$) and ($L_{series,loss,after}$) to represent the solder contact, PCB routing, wirebond and capacitor inductive losses before the switch and after the switch, a series resistance ($R_{series,loss}$) to represent the solder contact, PCB routing and wirebond resistive losses, a capacitance in parallel with C_{off} (C_{pcb}) to represent the additional parasitic capacitance coming from the board and soldering of the CMOS components, and a resistance in series with the ground terminal ($R_{gnd,loss}$) to represent the losses in this terminal connection.

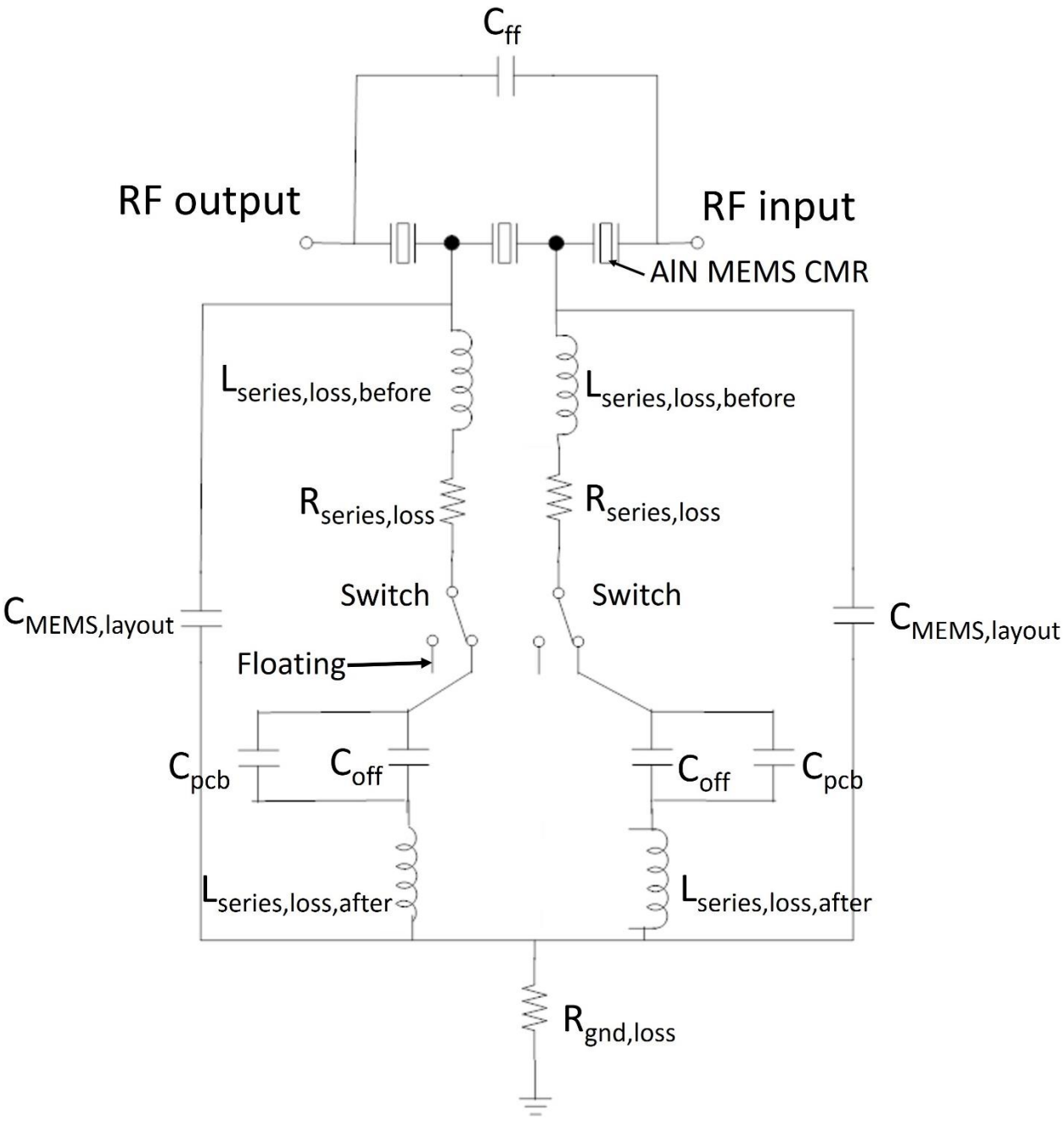


Figure 4-27. The schematic of the simulated circuit in the presence of the circuit parasitics, which is employed to match the response of the measured AlN filter channel attached to the switching circuit via wirebonds. The corresponding simulation results are provided in Figure 4-28, Figure 4-29 and Figure 4-30 in comparison with the measured ones.

Since we had to use a significantly smaller value for C_{off} in the experiments (we expected a C_{off} of 8 pF in the simulation without the PCB parasitics and wirebonds) in getting higher rejection in the filter off-state, we analyzed what level of parasitics are required for this to happen. Since we need a negative reactance in the switching circuit to turn off the filter efficiently, an increase in either parasitic inductance or capacitance would lead to a smaller size C_{off} in achieving the optimum performance. In the light of this circuit behavior, we included the circuit parasitics into the schematic and studied the filter responses for three different cases: i) filter on-state when C_{off} = 200 fF, ii) filter off-state when C_{off} = 200 fF and iii) filter off-state when C_{off} = 400 fF. By using these three cases, we can better estimate the value of each parasitic component shown in Figure 4-27. The values of the various components were selected by minimizing the error in the fitting of all three curves. The measured versus simulated responses for these three cases, in order, can be seen in Figure 4-28, Figure 4-29 and Figure 4-30; whereas, the parameter values used for fitting can be found in Table 4.3.

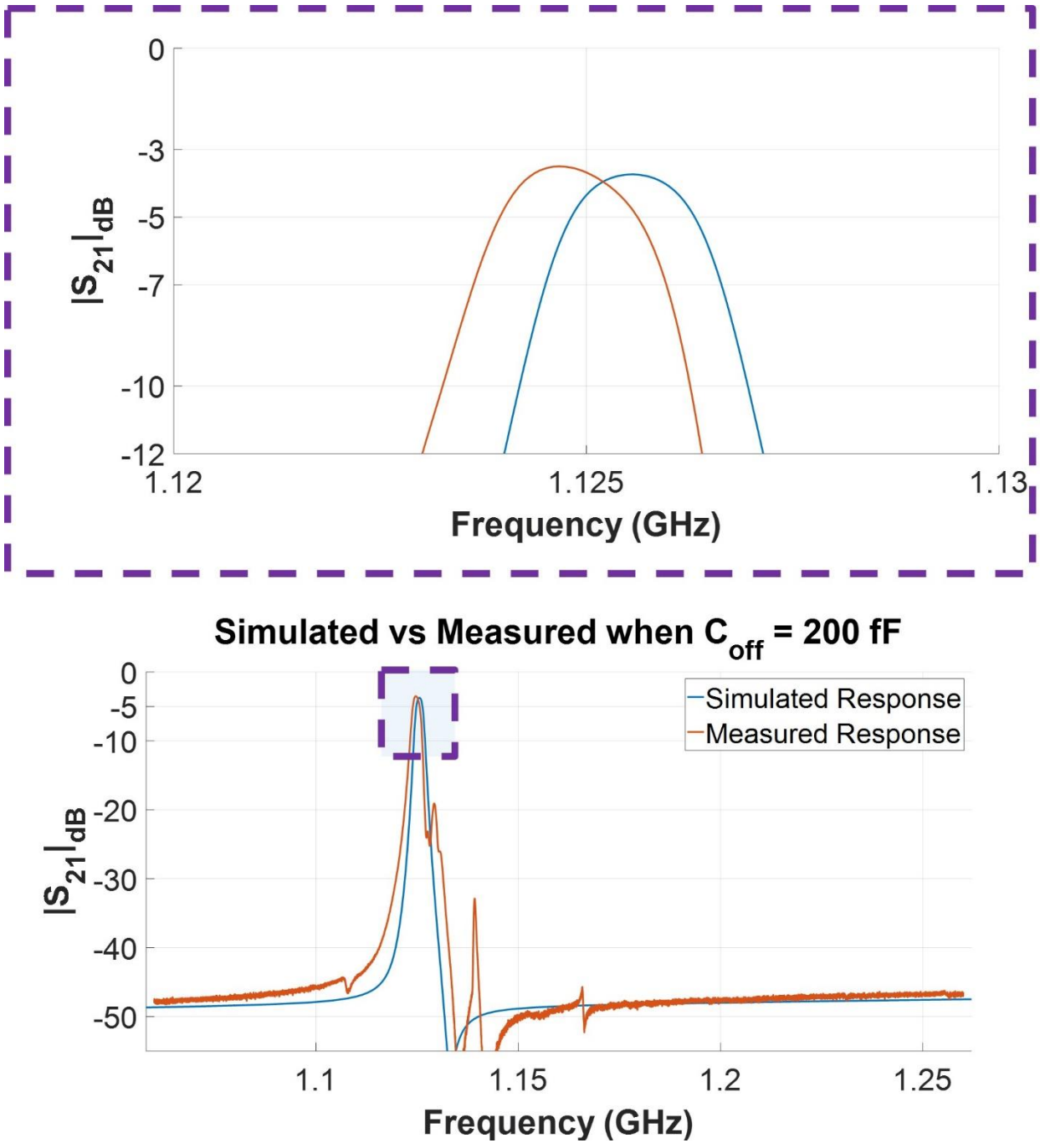


Figure 4-28. $|S_{21}|_{dB}$ of the simulated on-state filter response of the full circuit including the parasitics and that of measured one when C_{off} = 200 fF. The corresponding circuit schematics of the full circuit used in the simulation is provided in Figure 4-27; whereas, values for the parasitic components are provided in Table 4.3.

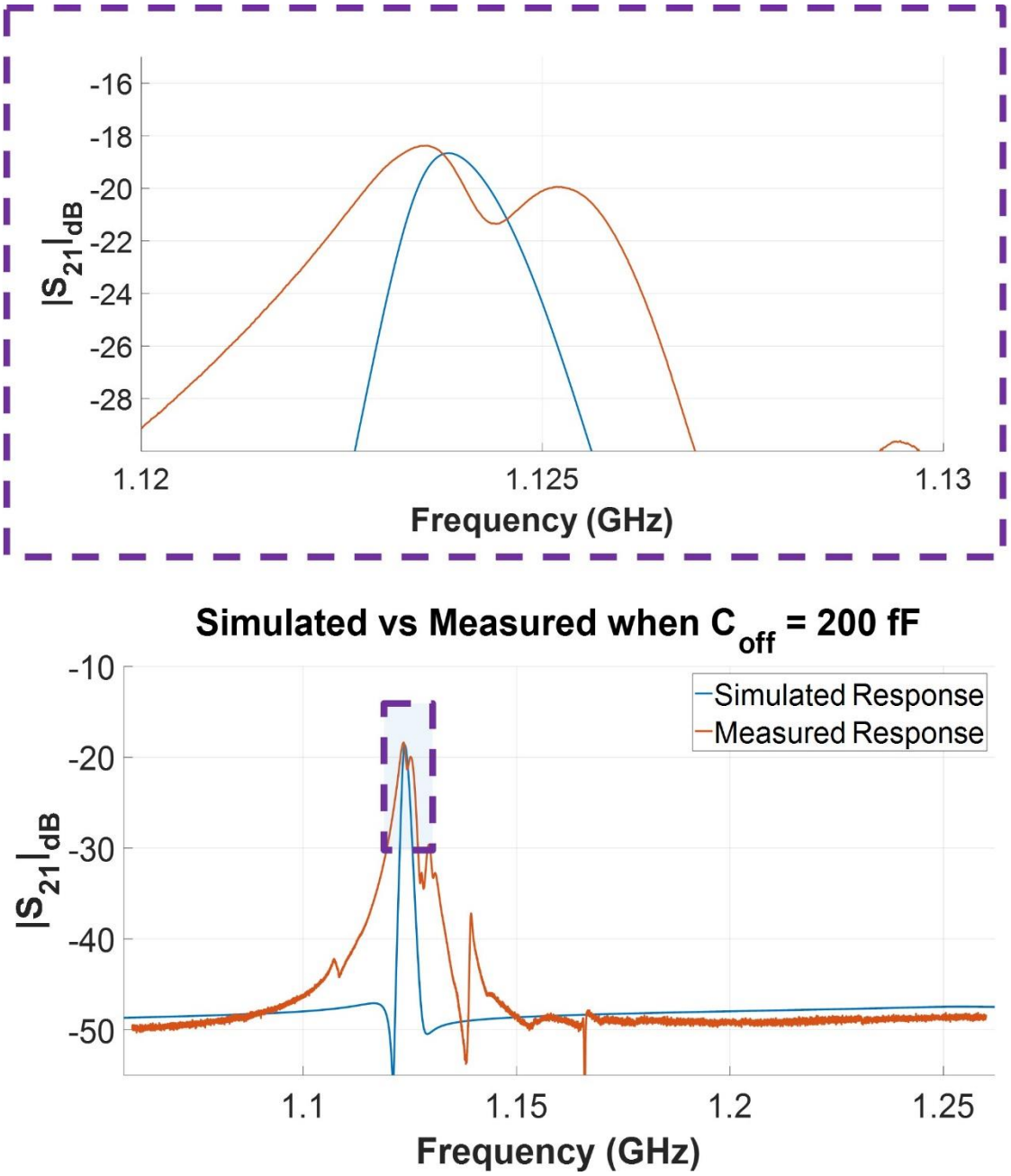


Figure 4-29. $|S_{21}|_{dB}$ of the simulated off-state filter response of the full circuit including the parasitics and that of measured one when C_{off} = 200 fF. The corresponding circuit schematics of the full circuit used in the simulation is provided in Figure 4-27; whereas, values for the parasitic components are provided in Table 4.3.

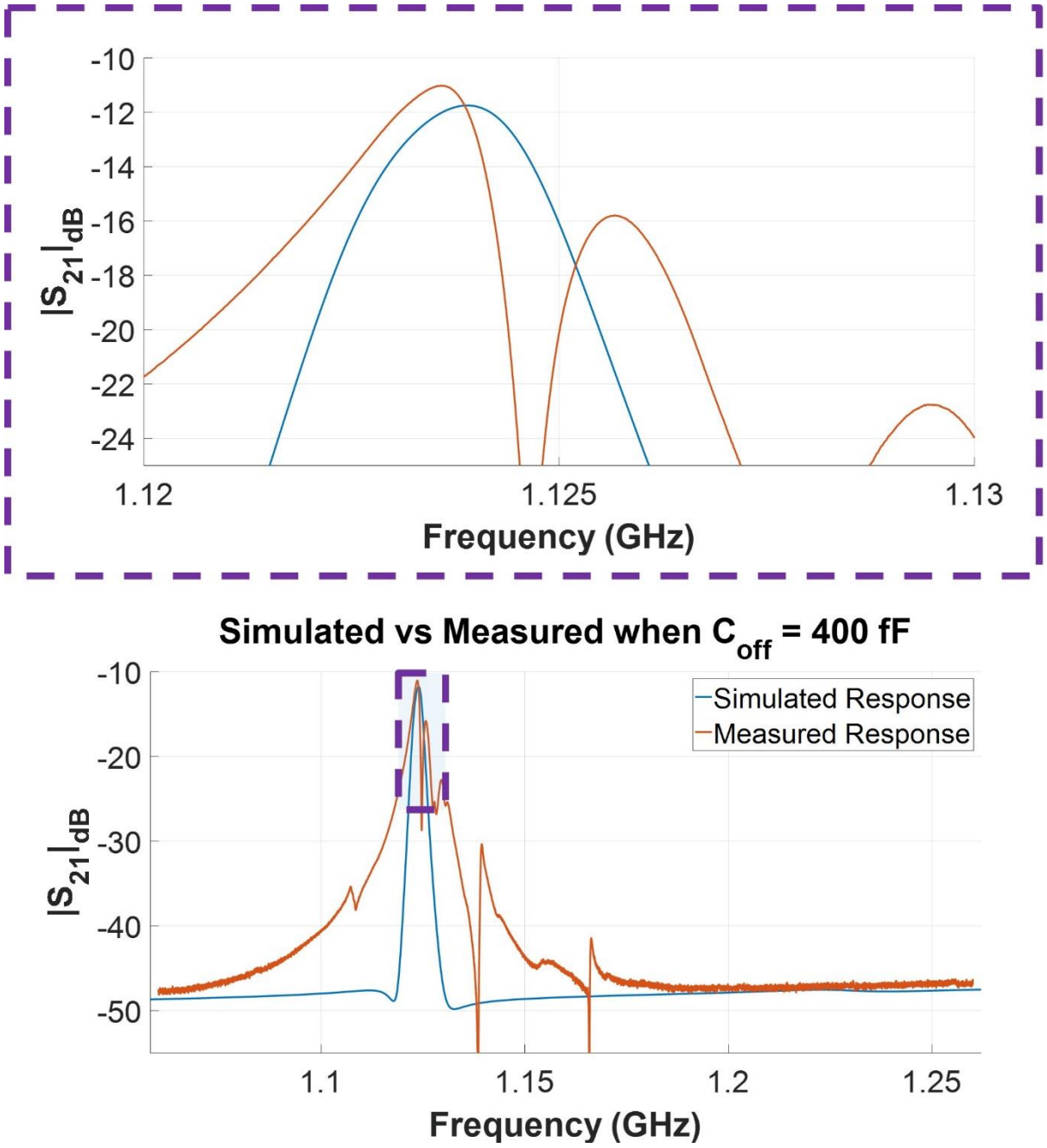


Figure 4-30. $|S_{21}|_{dB}$ of the simulated off-state filter response of the full circuit including the parasitics and that of measured one when C_{off} = 400 fF. The corresponding circuit schematics of the full circuit used in the simulation is provided in Figure 4-27; whereas, values for the parasitic components are provided in Table 4.3.

Table 4.3. The simulated values of the circuit parameters representing the parasitics coming from the AlN MEMS chip, CMOS components, wirebonds, and PCB. The circuit simulations are used to match the corresponding measured responses in three filter states for modeling the parasitics of the switching circuit.

Parameter Name	**Value When C_{off} = 200 fF**	**Value When C_{off} = 400 fF**
C_{ff}	5 fF	5 fF
$C_{MEMS,layout}$	1.5 pF	1.5 pF
$L_{series,loss,before}$	450 pH	450 pH
$L_{series,loss,after}$	8.6 nH	8.6 nH
$R_{series,loss}$	1 Ω	1 Ω
C_{PCB}	1.76 pF*	1.7 pF*
$R_{gnd,loss}$	0.25 Ω	0.25 Ω

**The C_{PCB} are different for these two cases because the capacitances we used to make the switching circuit on the PCB had a tolerance level of +/- 0.1 pF and we embedded the variances into this parasitic capacitance representing the PCB. The corresponding simulation results are provided in Figure 4-28, Figure 4-29 and Figure 4-30, respectively for filter on-state when C_{off} = 200 fF, filter off-state when C_{off} = 200 fF and filter off-state when C_{off} = 400 fF cases.*

As seen from Figure 4-28, Figure 4-29 and Figure 4-30, with the selected parasitic values, we were able to match the measured responses very well in the filter states except for the roll-off and mode splitting in the filter off-state. Since the capacitances we used to make the switching circuit on the PCB had a tolerance level of +/- 0.1 pF, we embedded the variances in the value of C_{off} into the PCB parasitic capacitance represented by C_{PCB}. $R_{series,loss}$ adjusts the Q of the switching circuit and thus its impact on the circuit is reflected primarily on IL in the filter off-state. $R_{gnd,loss}$ adjusts the floor in the out-of-band response away from the filter passband. Considering the values of each of these simulated parasitics, we can state that the additional parasitics associated with the

wirebonds and mounting of the switches on the PCB have a limited impact on the circuit behavior. However, the PCB routings after the capacitor connection (especially long ground lines as seen from Figure 4-19) are the dominant contributor for most of the additional parasitics.

In order to match the filter passband roll-off and mode splitting behaviors in the filter off-state responses, we also included into the circuit a feedthrough capacitance between the switch lower end terminals after tying the C_{off} capacitors ($C_{f,sw1sw2}$) to represent the signal cross-talking through the long signal routings on the PCB. We also put a resistance ($R_{f,sw1sw2}$) in series with $C_{f,sw1sw2}$ to represent the resistive losses in the feedthrough. The corresponding circuit schematic can be seen in Figure 4-31. We again ran the simulations and made the analysis for the aforementioned three filter-switching circuit responses. The measured versus simulated responses for these three cases, in order, can be seen from Figure 4-32, Figure 4-33, and Figure 4-34; whereas, the parameter values used for circuit simulations can be found in Table 4.4.

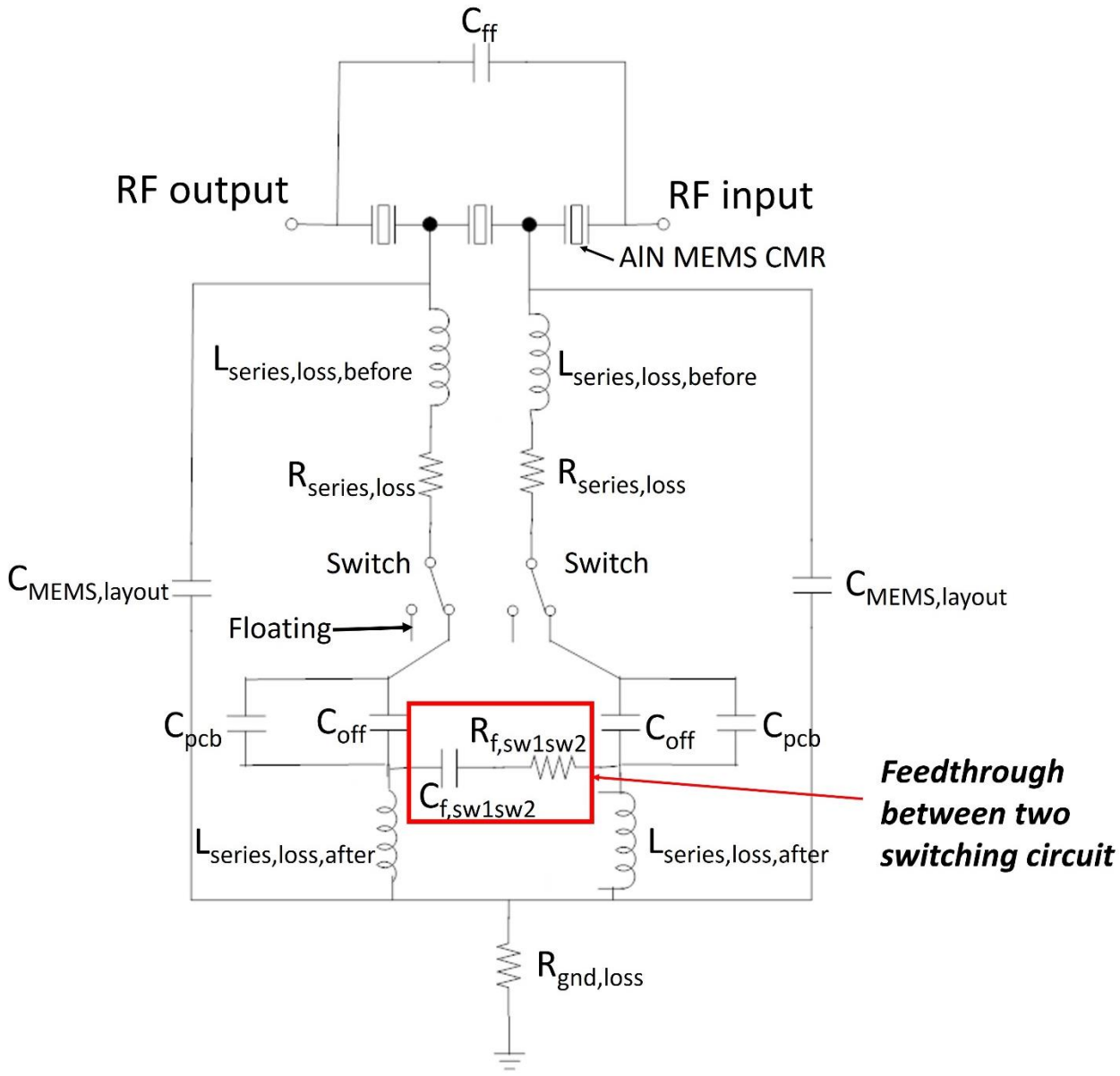


Figure 4-31. The schematic of the simulated circuit in the presence of the switch feedthrough parasitics, which is employed to match the response of the measured AlN filter channel indicating the mode splitting in the filter-off state after integrated with the switching circuit via wirebonds. The corresponding simulation results are provided in Figure 4-32, Figure 4-33, and Figure 4-34 in comparison with the measured ones.

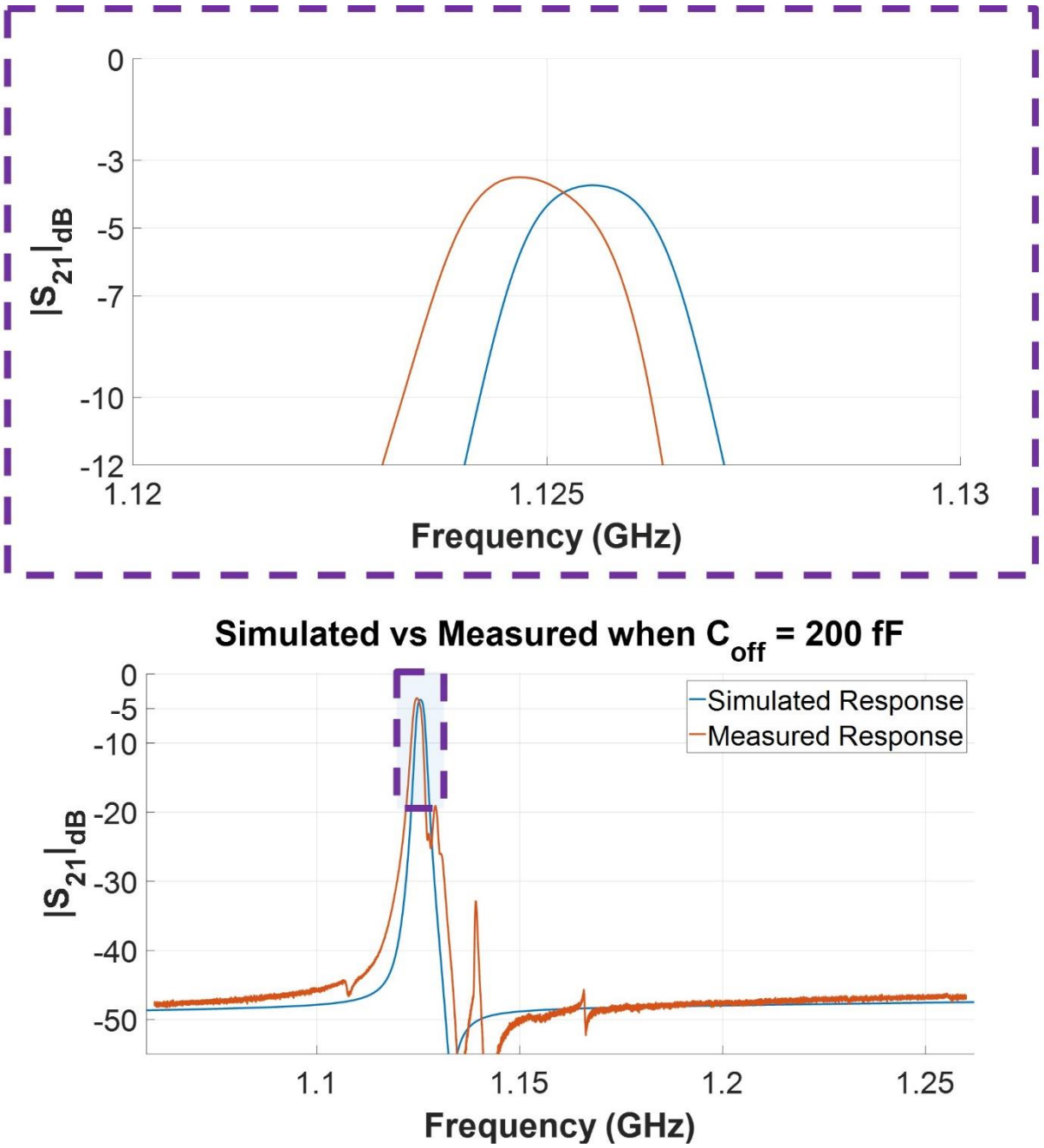


Figure 4-32. $|S_{21}|_{dB}$ of the simulated on-state filter response of the full circuit including the parasitics and that of measured one when C_{off} = 200 fF. The corresponding circuit schematics of the full circuit used in the simulation is provided in Figure 4-31; whereas, values for the parasitic components are provided in Table 4.4.

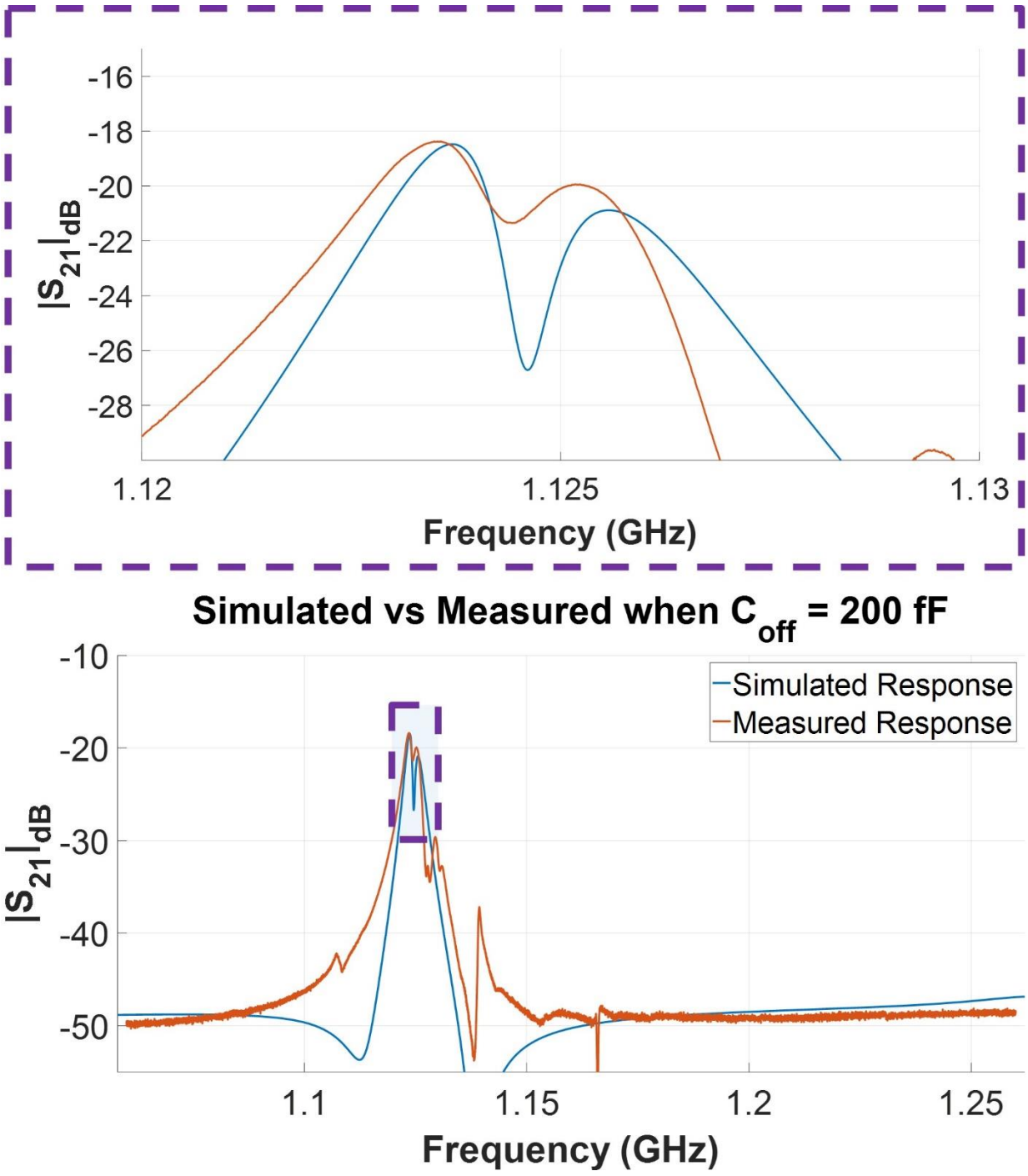


Figure 4-33. $|S_{21}|_{dB}$ of the simulated off-state filter response of the full circuit including the parasitics and that of measured one when C_{off} = 200 fF. The corresponding circuit schematics of the full circuit used in the simulation is provided in Figure 4-31; whereas, values for the parasitic components are provided in Table 4.4.

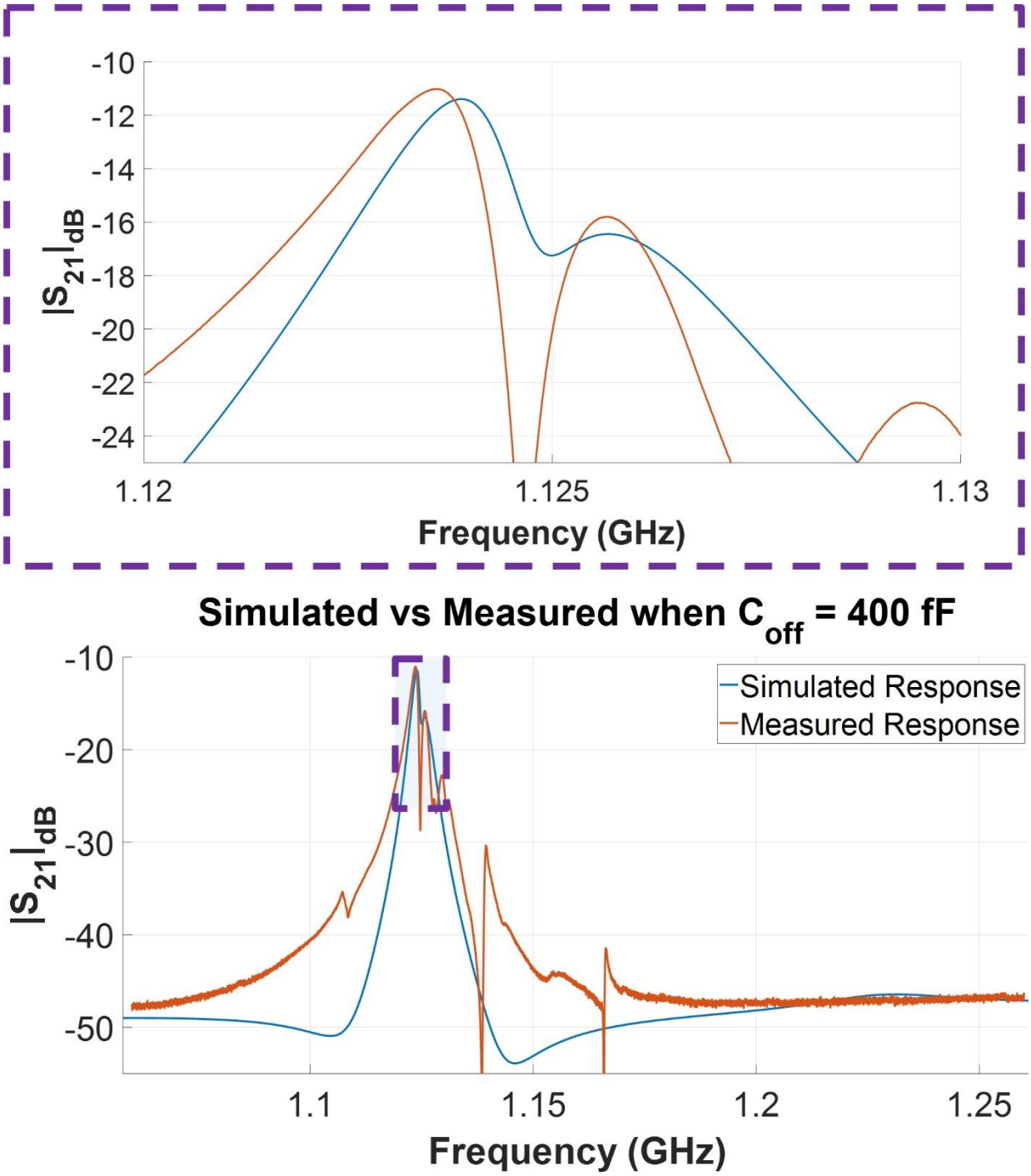


Figure 4-34. $|S_{21}|_{dB}$ of the simulated off-state filter response of the full circuit including the parasitics and that of measured one when C_{off} = 400 fF. The corresponding circuit schematics of the full circuit used in the simulation is provided in Figure 4-31; whereas, values for the parasitic components are provided in Table 4.4.

Table 4.4. The simulated values of the circuit parameters representing the parasitics coming from the AlN MEMS chip, CMOS components, wirebonds, and PCB. The circuit simulations are used to match the corresponding measured responses in three filter states for modeling the parasitics of the switching circuit.

Parameter Name	**Value When C_{off} = 200 fF**	**Value When C_{off} = 400 fF**
C_{ff}	5 fF	5 fF
$C_{MEMS,layout}$	1.5 pF	1.5 pF
$L_{series,loss,before}$	450 pH	450 pH
$L_{series,loss,after}$	8.6 nH	8.6 nH
$R_{series,loss}$	1 Ω	1 Ω
C_{PCB}	1.76 pF*	1.7 pF*
$R_{gnd,loss}$	0.25 Ω	0.25 Ω
$C_{f,sw1sw2}$	8.5 pF	8.5 pF
$R_{f,sw1sw2}$	0.5 kΩ**	0.3 kΩ**

**The C_{PCB} are different for these two cases because the capacitances we used in the measurement had a tolerance level of +/- 0.1 pF and we embedded the variances into this parasitic capacitance representing the PCB. ** $R_{f,sw1sw2}$ are made different to match the amplitude of the second peak in the passband. The corresponding simulation results are provided in Figure 4-28, Figure 4-29 and Figure 4-30, respectively for filter on-state when C_{off} = 200 fF, filter off-state when C_{off} = 200 fF and filter off-state when C_{off} = 400 fF cases.*

As seen from Figure 4-32, Figure 4-33, and Figure 4-34, with the added feedthrough parasitics, we were able to preserve the matching of filter on-state behavior (which was already in good agreement with the measured ones) while being able to better describe the filter off-state behaviors than the previous circuit parasitics model (*i.e.* mode splitting in the passband and poorer roll-off of the passband). In order to match the amplitude of the second peak in the rejected

passband in the filter off-state responses, we had to adjust $R_{f,sw1sw2}$. On the other hand, $C_{f,sw1sw2}$ causes the mode splitting behavior in the filter off-state passband when it is larger than few 100 s of fF. Its exact value determines the relative location of the first and second peaks in the filter passband with a minor impact on the response amplitude. As mentioned before we expect that this feedthrough parasitics come from the long routings on PCB to connect the capacitor to ground.

In summary, we can conclude that in order to achieve the upper limit in the rejection in the filter off-state, the PCB routings and placement of CMOS components on the PCB should be optimized for the level of parasitics, *i.e.* series inductances and resistances, and shunt capacitances, as well as, the cross talking of the two switching circuits on the board. Even so, our analysis over the measured data proves that this switching concept is definitely viable. With the use of the developed AlN MEMS platform and the low loss RDL, we can significantly reduce the parasitics coming from the PCB in the technology integration. Hence, we can enable the efficient realization of programmable filter array (or the self-healing filter with this switching technique) in which the filters in the bank could be turned on/off independently and simultaneously with low loss and high isolation.

Chapter 5

Conclusions

The goal of this thesis has been to develop an AlN MEMS platform on 8" Si wafer in collaboration with A*STAR, IME, Singapore that can be 3D heterogeneously integrated with CMOS circuits and used to build unique systems which are possible only when AlN MEMS and CMOS are intimately connected.

In order to realize such a platform, we first individually developed and characterized the three technological components of the AlN MEMS platform, respectively the MEMS, TFE and RDL. In this respect, we first studied the individual MEMS devices in order to get resonator frequency responses with spurious modes away from bandwidths of interest while maintaining high Q and k_t^2, and thus *FoM* for filters applications. We found out that *FL* plays critical role in the value of Q to limit the anchor losses while *OE* could have detrimental impact on the k_t^2 based on the corner points as the reflections from the resonator edges in the direction of vibration could permit the excitation of other lateral modes (symmetric modes) in the device. As for the SMs, we observed that *FN* and *OE* have the highest impact on the location of the spurs. Moreover, for the particular

resonator geometries we studied, transverse mode does not contribute to the SMs. To the best of our knowledge we attained the lowest *IL* in AlN MEMS narrowband filters reported to date.

As a proof-of-concept of the 3D integrated platform, we used SES to build self-healing filters that overcome challenges associated with random and systematic variations of the center frequency of AlN MEMS CMRs. In this regard, we built two different chip stack with primary RF routing on MEMS through the front-end RDL and CMOS through the built-in thick copper layers available in the process node. The chip integration is achieved through 3D heterogeneous integration process in which the hermetically thin film encapsulated MEMS resonators are solder-bump bonded to a CMOS chip after solder bumps are placed on the CMOS chips. We clearly demonstrated the advantages of RDL through which we achieved 4 dB less *IL* and 10 dB more *OBR* in the self-healing filters when compared to the CMOS routing (rejection is 30 dB more at frequencies further away from the filter passband). We estimated that RDL reduced the parasitic capacitance due to RF routing by ~20x and the resistance by ~5x when compared to signal routing on CMOS. Through RDL, the CMOS chip area can be employed more efficiently as it can be made smaller than the AlN MEMS filter array. Overall the application of SES yielded 495 unique filter frequency responses and offered a tuning range of 300 kHz for f_o and 250 kHz for the filter *BW*.

As for the programmable filter array, we were only able to demonstrate a proof-of-concept of it as we did not have anymore access to CMOS chips and bumping. Although the filter on-state response is not affected significantly by the PCB attachment and switching circuit, given the level of parasitics (both inductance and capacitance) due to off-chip routing, we could only turn the filter response off by almost 18.4 dB. Nonetheless, this demonstration proves that the switching concept is definitely viable and an integrated platform would enable a very interesting channelizer prototype.

5.1 Future Research Directions

Another emerging application for AlN MEMS CMRs, which would benefit from the tight integration with CMOS is the realization of DC-DC power converters, in which the high *Q* and small form factor inductance of the resonators can be an efficient substitute for magnetic components in resonant converters.

5.1.1 Motivation for using AlN MEMS CMRs as transformers in power converter applications

Over the last few decades mesoscale piezoelectric transformers (PTs) have been used in power converter technology as a replacement for magnetic transformers in some specific applications [57]. In particular they have been used in the liquid crystal display (LCD) backlighting inverter modules of laptop computers and flat panel displays in order to power up light-emitting diodes (LED) or cold cathode fluorescent lamps (CCFL) requiring high ignition voltages (from 3 V up to 40 V_{DC} or 500 V_{AC}) [58] and power capabilities up to 10 s of Watts [59], [60]. They had been a preferred choice over magnetic transformer because PTs offer high inherent open circuit voltage gain, tunable voltage gain via load, no electromagnetic interference, high *Q*, small size and weight when compared to their magnetic counterparts [59]. Though, for low power-low voltage applications PTs have failed to keep up with the market's demand for more compact sizes, higher efficiencies and power densities at high frequencies [61], [62].

AlN CMRs, when used as transformers in their inductive region, are promising candidates to address the aforementioned demands of next generation low power and low voltage power supply on chip (PwrSoC) roadmap. Since they offer power densities in excess of 10 $\mu W/\mu m^3$ [63] (more than a 1,000 better than the PTs presented in [64]), high performance at frequencies up to several GHz [65] and can be 3D hybrid integrated with CMOS circuits, they have the potential to be a disruptive solution for Power Supplies on Chip.

A sample circuit diagram for the envisioned DC-DC power converters by using AlN MEMS CMRs as transformers without any external magnetic components is shown in Figure 5-1. The topology consists of a half bridge inverter for DC-AC conversion, a two-port AlN CMR for AC-AC power transformation, a full bridge rectifier for AC-DC conversion and a load circuit. Each of the three power conversion stages (DC-AC, AC-AC and AC-DC) could be analyzed individually in the presence of a two-port AlN MEMS CMR as a transformer. Since the performance of CMOS components would be technology dependent and their design would require a specific target application, we only point out the advantages of the AlN MEMS CMRs as transformers (*i.e.* AC-AC power converters).

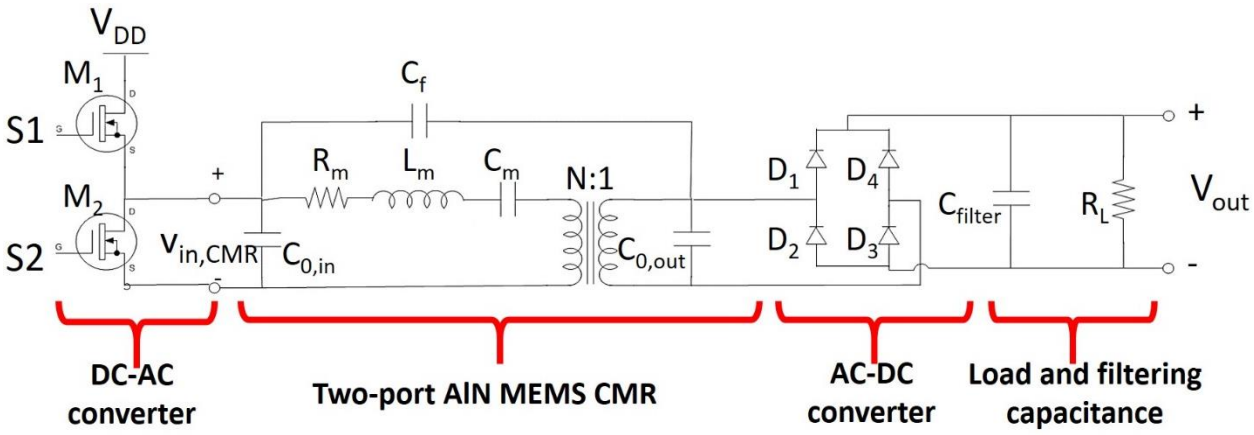


Figure 5-1. Proposed high frequency inductor-less DC-DC power converter topology by using AlN MEMS CMR as transformer in its inductive region of operation.

5.1.2 Analysis of two-port AlN MEMS CMRs as Transformers

In this section we derive the generalized equations of the AlN MEMS CMRs as transformers by using the equivalent resonator parameters. We also make projected performance analysis of these devices since these critical resonator parameters could be improved by design (such as two-dimensional mode [66] or Lamé mode resonators [67]-[68]) or material property enhancement (such as ScAlN [69]).

The methodology to derive the analytical expressions for power conversion efficiency (η) of a MEMS transformer with the same lumped element circuit model has been previously provided in [56]. Using the same methodology and simplification of the circuit model (see Figure 5-2), we analytically derived the same parameters for AlN MEMS CMRs by including also the impact of the transformer ratio, *N,* in the expressions (see Figure 5-3). To simplify the analysis, C_f of AlN MEMS CMR is neglected as it would be small for the range of frequencies these device are shown to work with good performances (*i.e.* from 10 s of MHz up to 9.9 GHz [65]).

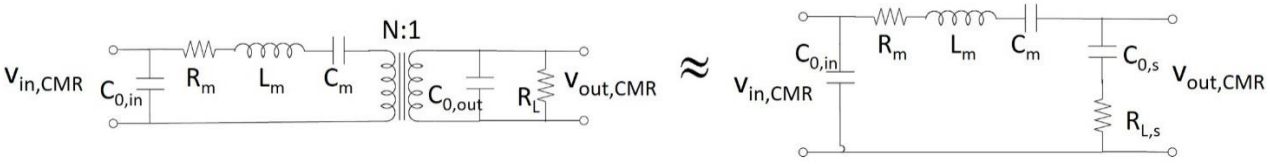


Figure 5-2. Simplification of circuit model by means of converting parallel components into series ones and transferring all the components into one side of the transformer based on the transformer turns ratio, *N*.

The derivation starts with the parallel to series circuit conversion at the output and referring this circuit into the input side of the transformer as seen in Figure 5-2. The corresponding set of equations for this conversion is provided in Figure 5-3 where ω_{res} (frequency in radiance) represents the resonance of series motional impedance of the AlN CMR with input referred series conversion of the load with output device capacitance.

$$\omega_{res} = \sqrt{\frac{C_m + C_{0,s}}{L_m C_m C_{0,s}}} = \omega_0 \sqrt{1 + \frac{C_m}{C_{0,s}}} \qquad Q_{load} = \frac{R_L}{\omega_{res} C_{0,out}} \qquad R_{L,s} = \frac{R_L}{N^2(1 + Q_{load}^2)} \qquad C_{0,s} = N^2 C_{0,out}\left(1 + \frac{1}{Q_{load}^2}\right)$$

Figure 5-3. Set of expressions for series to parallel conversion of output load circuit and its referral into the input side of the transformer.

5.1.2.1 Power Conversion Efficiency

For AC-AC power conversion, the AlN MEMS CMRs operate in their inductive regime (*i.e.* in-between series, f_o, and parallel resonances, f_p, seen in Figure 1-3) in order to have considerable amount of power transferred to the load. The power conversion efficiency of the AlN MEMS CMRs as a transformer (η_{CMR}) can be calculated as:

$$\eta_{CMR} = \frac{I_{rms}^2 R_{L,s}}{I_{rms}^2 R_{L,s} + I_{rms}^2 R_m} = \frac{1}{1 + \frac{R_m}{R_{L,s}}} \tag{5.1}$$

Note that the matching condition ($R_{L,s}$=R_m) ensures maximum power transfer to the load, which corresponds to an efficiency of 50 %. When we take the derivative of Eq. (5.1) with respect to R_L (after inserting $R_{L,s}$ expression in terms of R_L in Figure 5-3 into η_{CMR} expression) we can calculate the peak efficiency ($\eta_{CMR,peak}$) with the set of equations provided in Figure 5-4.

At $\eta_{CMR,peak}$

$$\frac{\partial \eta_{CMR}}{\partial R_L} = 0 \Rightarrow R_{L_{peak}} = \frac{1}{\omega_{res} C_{0,out} R_L} \Rightarrow R_{L,s_{peak}} = \frac{R_L}{1 + \left(\omega_{res} C_{0,out} R_L\right)^2}$$

$$\Rightarrow \eta_{CMR,peak} = \frac{1}{1 + \frac{\pi^2}{4} \frac{(N+1)}{k_t^2 Q} \frac{\omega_{res}}{\omega_0}} \quad \text{where} \quad \frac{\omega_{res}}{\omega_0} = \sqrt{\frac{4}{\pi^2} k_t^2 \frac{1}{(N+1)} + 1}$$

Figure 5-4. Expressions for peak efficiency ($\eta_{CMR,peak}$) calculation of the AlN MEMS CMRs as power transformers.

Since the motional lumped elements in the circuit model of AlN CMRs can be calculated by knowing only N, Q, k_t^2, f_o, and $C_{o,in}$ as previously discussed in Chapter 1.1, we generated the efficiency figures based on these resonator parameters. Figure 5-5 showcases the η_{CMR} dependency

on device sizing (*i.e.* $C_{o,in}$) when k_t^2 is 1.5 %, N is 1 and R_L is assumed to be 2.75 kΩ; whereas, $\eta_{CMR,peak}$ dependency on Q and k_t^2 (N is set to 1) is shown in Figure 5-6.

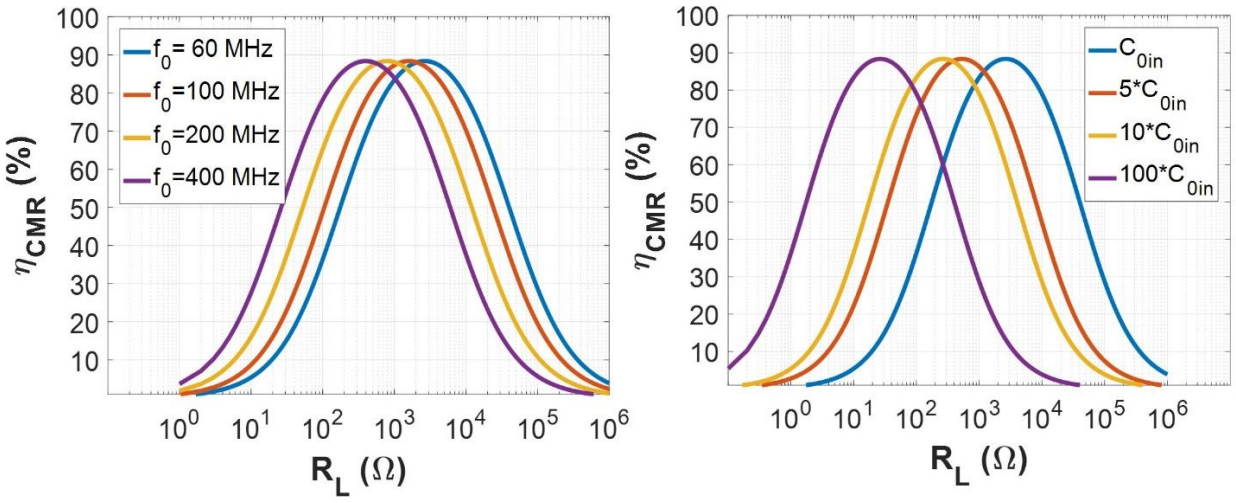


Figure 5-5. η_{CMR} dependency on f_o, $C_{o,in}$ and R_L.

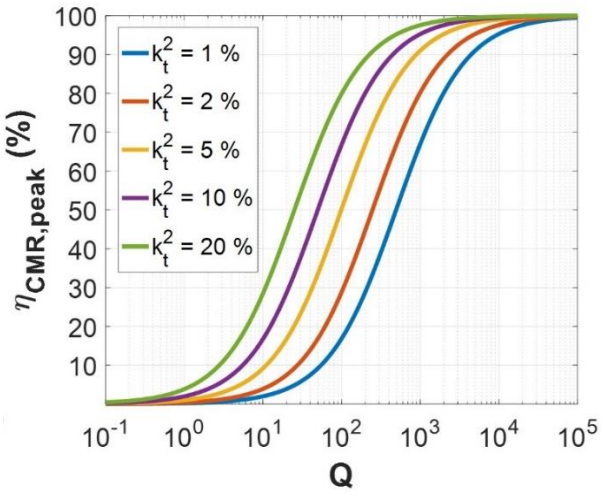


Figure 5-6. $\eta_{CMR,peak}$ dependency on Q and k_t^2, and thus, *FoM*.

We can make observations from the derived expression and the drawn figures for the AlN MEMS CMR efficiency when used as power transformer. First, the $\eta_{CMR,peak}$ is independent of the device resonant frequency (f_o), device size (C_o) and load resistance (R_L). This is particularly important, as increasing the frequency or size of the transformer is not accompanied by a

degradation in the transformer performance as we can always find a combination of f_o, C_o and R_L that would give us the best power conversion efficiency possible. This is particularly important from the design standpoint because once f_o, N and load are set, we should only play with $C_{o,in}$ in the design of AlN CMRs as transformers (by means of changing the resonator size) to achieve the peak efficiency in the transformer (Q and k_t^2 are primarily set by material properties and mode of vibration). Second, $\eta_{CMR,peak}$ increases with multiplication of Q and k_t^2. In other words, the *FoM* for AlN MEMS CMRs as transformers is also defined by the same *FoM* used in filters (*i.e.* $FoM = k_t^2 \cdot Q$).

With the selected resonator geometry performance provided in Table 2.6, a peak efficiency of more than 85 % could be achieved for AlN MEMS CMRs when used as transformers. In order to reach the level efficiencies achieved for PT transformers (*i.e.* 93.4 % [70]) and go beyond, the Lamé mode resonators [67]-[68] could be employed in the transformer design. With the demonstrated Q and k_t^2 for this device (*i.e.* 1750 and 6.2 %, respectively), an efficiency of 95.6 % in the transformer can be attained.

The low loss RDL on the developed AlN MEMS platform offers to connect multiple resonators on the same chip in an efficient way that series or parallel combination of these resonators can be achieved without any significant performance degradation in the power converter based on, respectively, the voltage or current handling needs of the target application. The developed platform also offers efficient and robust integration of the AlN MEMS resonator with the CMOS circuits. Considering the envisioned circuit topology shown in Figure 5-1, the whole circuit for the high frequency inductor-less DC-DC power converter might be easily realized on-chip where the CMOS devices can be designed efficiently and the losses of signal interconnects and parasitic capacitances compared to resonator device capacitance might be kept within the limits for the ultimate efficiency offered by these devices.

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