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# Polarization Imaging Sensors in Advanced Feature CMOS Technologies

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Polarization Imaging Sensors in Advanced Feature CMOS Technologies

by

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<div align="right">Raphael Njuguna</div>

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**ABSTRACT OF THE DISSERTATION**

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Professor Viktor Gruev, Chair

The scaling of CMOS technology, as predicted by Moore's law, has allowed for realization of high resolution imaging sensors and for the emergence of multi-mega-pixel imagers. Designing imaging sensors in advanced feature technologies poses many challenges especially since transistor models do not accurately portray their performance in these technologies. Furthermore, transistors fabricated in advanced feature technologies operate in a non-conventional mode known as velocity saturation. Traditionally, analog designers have been discouraged from designing circuits in this mode of operation due to the low gain properties in single transistor amplifiers. Nevertheless, velocity saturation will become even more prominent mode of operation as transistors continue to shrink and warrants careful design of circuits that can exploit this mode of operation.

In this research endeavor, I have utilized velocity saturation mode of operation in order to realize low noise imaging sensors. These imaging sensors incorporate low noise analog circuits at the focal plane in order to improve the signal to noise ratio and are fabricated in 0.18 micron technology. Furthermore, I have explored nanofabrication techniques for realizing metallic nanowires acting as polarization filters. These nanoscopic metallic wires are deposited on the surface of the CMOS imaging sensor in order to add polarization sensitivity to the CMOS imaging sensor. This hybrid sensor will serve as a test bed for exploring the next generation of low noise and highly sensitive polarization imaging sensors.

# Chapter 1

# Introduction

## 1.1    Problem, Definition, and Motivation

The inception of solid state imaging devices dates back to the early 1960's when the first 10-by-10 CMOS imaging array was reported in the literature [1-3]. Although this pioneer work is associated with the dawn of digital imaging sensors era, the poor image quality produced by the early CMOS imagers encouraged scientists to explore other venues for replicating the imaged environment with high spatial and temporal fidelity. CCD imaging technology was introduced in the late 1960's [4] and provided superior image quality compared to the CMOS imaging technology at that time [5]. During the next two and a half decades, CCD imaging technology would capture majority of the imaging market due to its low noise imaging capabilities and high signal to noise ratio performance. With the emergence of cell phone cameras in the mid 1990's, CMOS imagers were reintroduced in the imaging market due to their low power consumption capabilities. A typical CMOS imaging sensor consumes one to two orders of magnitude less power and offers higher integration capabilities, such as inclusion of analog to digital conversion, signal processing, and other processing blocks on the same chip, than an average CCD imaging sensor [6, 7]. During the last decade, CMOS imaging sensors have regained the market share hold and today they account for more than 90% of the imaging market [6].

The scaling of CMOS technology, as predicted by Moore's law, has allowed for realization of high resolution imaging sensors and for the emergence of multi-mega-pixel imagers. Today's imaging sensors are typically fabricated in 110 nm technology, while

digital circuits are fabricated in 32 nm technology. The gap between the two technologies is primarily due to the fact that imaging sensors employ analog circuits in order to realize many of the building blocks and the transistor models for advanced feature technologies are not well modeled for SPICE simulations. Hence, an analog designer cannot reliably predict the performance of these circuits before fabricating the device in advanced feature technologies. Furthermore, it has been observed that transistors when fabricated in advanced feature technologies no longer operate in the traditional modes of operation, such as: cut-off, sub-threshold, linear, and saturation modes. Instead, transistors can also operate in velocity saturation mode when fabricated in 180 nm feature technologies or smaller. Traditionally analog designers have been discouraged from designing circuits in this mode of operation due to the low gain properties of single transistor amplifiers [8]. Nevertheless, velocity saturation will become even more prevalent mode of operation as transistors continue to shrink and warrants careful design of circuits that can exploit this mode of operation.

Today's CMOS and CCD imaging sensors capture two of the three fundamental properties of the imaged environment and they are intensity and color [7]. The third property of light, namely polarization, has been ignored by the imaging industry partly because of the human inability to discriminate polarization [9]. Nevertheless, exploiting the polarization properties of light has been an active area of research. Polarization contrast imaging has proven to be very useful in gaining additional visual information in many biomedical applications, such as imaging for early skin cancer [10], cervical cancer [11], and retinal surgery [12]. In addition, polarization imaging has been used to enhance targets in scattered environments, such as underwater imaging [13-15] and visibility in hazy conditions [16]. Polarization has also been exploited for fingerprint identification [17], material detection [18], classification of chemical isomers [19], and 3-D shape reconstruction from a single camera view [20, 21]. One of the major challenges in the proliferation of polarization imaging research is the lack of robust and compact sensors that capture polarization properties of light in real-time and in high-resolution.

In this dissertation, I will explore realization of imaging sensors fabricated in advanced feature technologies that exploit velocity saturation mode of operation in transistors and are capable of extracting polarization information from the imaged environment. In particular, I will address the following research questions:

1) Can we utilize transistors operating in velocity saturation in order to design mixed-mode circuits and systems for imaging sensors? Can the performance of these new circuits be on par or perform better than current circuits used for imaging sensors?

2) Can we monolithically combine current mode imaging elements with current mode analog computational circuitry to perform image processing at the focal plane of an imaging sensor? What are the noise performance and power consumption of such an implementation?

3) Can we develop and fabricate carefully designed optical nano-structures that will behave as linear polarization filters with high contrast ratios? Can we design these structures from materials compatible with semiconductor fabs?

4) Can we develop hybrid sensors by monolithically integrating optical nano-structures with CMOS technology to enhance or filter the optical signals?

## 1.2    Contributions of This Dissertation

In order to address the above mentioned research questions, I have designed, fabricated and tested a custom imaging sensor in 0.18 micron process and utilized the small feature technology in order to realize circuits that operate in velocity saturation mode of operation. Furthermore, I have combined imaging and analog signal processing on the same chip in order to realize low power sensor capable of realizing real-time parallel image processing. This imaging sensor is also used as a substrate for depositing

aluminum nanowire in the clean room facilities at Washington Universities in order to realize monolithic integration of CMOS technology with custom fabricated nanostructures. I further investigated the impact of nanowire sizes on the sensitivity of the imaging sensor to polarization information. The following is a detailed list of my contributions:

1)      I have designed, fabricated, and tested a novel CMOS imaging sensor in 0.18 micron technology. This imaging sensor utilizes the velocity saturation mode of operation in the in-pixel transconductor transistor in order to perform linear conversion between accumulated photo voltage and output current. This imaging sensor is the first one reported in the literature that utilizes velocity saturation mode of operation together with noise correction circuitry in order to realize a low noise 2-D imaging sensor.

2)      I have combined an array of imaging elements with image processing circuitry at the focal plane in order to realize smart, low power imaging sensors. The sensor is capable of performing both imaging and image processing using low power analog circuits. The pixel's read-out transistor operates in the triode mode, providing linear relationship between accumulated photovoltage and output current. Neighborhood of pixels is simultaneously accessed and provided to a digitally programmable analog processor, where four parallel convolution operations are executed. The imaging sensor can compute various edge detector filters or compute the first three Stokes parameters for polarization imaging at 100 frames per second with ~5mW of power consumption. An equivalent digital system will typically consume two orders of magnitude higher power consumption.

3)      I have fabricated an array of pixelated aluminum polarization filters with different pitches and orientations using electron beam lithography and reactive ion etching processes. The polarization filters contain nanowires with minimum pitch of 50nm, which is about two times smaller (better) than the current state-of-the-art nanowire

polarization filters. The small pixel pitch of the aluminum nanowire improves the sensitivity of these filters to polarization filters by a factor of 5 compared to other filters reported in the literature.

4) I have monolithically integrated aluminum nanowires with my custom CMOS imaging sensor. The aluminum nanowires, which are fabricated in the cleanroom facilities at Washington University, act as polarization filters and are deposited directly on the surface of the CMOS imaging sensor. This monolithic integration allows for evaluation of key advancements in the imaging research: the polarization sensitivity of an imaging array operating in the velocity saturation mode. This hybrid system will serve as a test bed for future polarization designs utilizing advanced CMOS and nano-fabrication processes.

# 1.3  Organization of This Dissertation

The dissertation is organized as follows. The design of an imaging sensor operating in velocity saturation mode is described in Chapter 2. This imaging sensor is fabricated in 180 nm CMOS process with dedicated pinned photodiodes. The analog read-out circuitry interfaces with the pixel's read-out transistor which operated in the velocity saturation mode. Measurements from the fabricated test chip are provided at the end of the chapter. The integration of an imaging array with low power analog processing unit at the focal plane is discussed in Chapter 3. This imaging sensor combines a low noise pixel designed, composed of two transistors and a photodiode, with digitally programmable analog circuits. Experimental results from the fabricated imaging sensor in 0.6 μm technology are provided at the end of the chapter. Nanofabrication of aluminum nanowire polarization filters and monolithic integration a custom CMOS imaging sensor are described in Chapter 4. Summary of research described in this dissertation and possible future research directions are discussed in Chapter 5.

# Chapter 2

# Current-mode CMOS Imaging Sensor with Velocity Saturation Mode of Operation

## 2.1    Background

The inception of solid state imaging devices dates back to the early 1960's when the first 10-by-10 CMOS imaging array with in-pixel source follower was reported in the literature [1-3]. Although this pioneer work is associated with the dawn of digital imaging sensors era, the poor image quality produced by the early CMOS imagers encouraged scientists to explore other venues for replicating the imaged environment with high spatial and temporal fidelity. CCD imaging technology was introduced in the late 1960's [22] and provided superior image quality compared to the CMOS imaging technology at that time [23]. During the next two and a half decades, CCD imaging technology would capture majority of the imaging market due to its low noise imaging capabilities and high signal-to-noise ratio (SNR) performance. With the emergence of cell phone cameras in the mid 1990's, CMOS imagers were reintroduced in the imaging market due to their low power consumption capabilities. During the last decade, CMOS imaging sensors have regained the market share hold and today they account for more than 90% of the imaging market [24].

Active pixel sensors are fabricated in standard CMOS technologies, which offer higher integration capabilities such as analog sensing, analog to digital conversion, signal processing, and other processing blocks on the same chip [25-27]. The integration capabilities provided by CMOS technology contribute to miniaturization, low power

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consumption, increased functionality, and cost effective imaging solutions [6, 7]. Furthermore, CMOS imaging sensors can employ random access readout schemes that are suitable for high speed imaging, computational photography and compressive sensing.

CMOS imaging sensors can be classified into voltage-mode and current-mode depending on the type of output signal obtained from the pixel. Voltage-mode imaging sensors [7, 28-35] employ a source follower transistor that buffers photo accumulated voltage on a photodiode and outputs a voltage signal on a readout bus. Voltage-mode imagers have a major stronghold in today's imaging industry primarily because of their low spatial and temporal noise performance. Current-mode imaging sensors [36-46] employ in-pixel transconductor transistor that converts photo accumulated voltage into a current signal that flows on a readout bus. Current-mode imagers have been primarily used as computational sensors [41, 44, 45] since they can support high frame rate read-out and computation-for-free during read-out of the sensors. However, these sensors have lower image quality due to large spatial and temporal noise compared to voltage mode imagers.

The scaling of CMOS technology, as predicted by Moore's law [47], has allowed for realization of high resolution imaging sensors and for emergence of multi-megapixel imagers. However, the operational characteristics of transistors have changed with scaling of CMOS technology. Transistors no longer operate only in the traditional modes of operation, such as cut-off, sub-threshold, linear, and saturation modes. Instead, transistors are starting to operate in a new mode of operation, called velocity saturation mode. Traditionally, analog designers have been discouraged from designing circuits in this mode of operation due to the low gain properties in single transistor amplifiers [8]. Nevertheless, velocity saturation will become even more prominent mode of operation as transistors continue to shrink and warrants careful design of circuits that can exploit this mode of operation.

In this chapter, I present a current-mode CMOS imaging sensor whose in-pixel readout transistor operates in velocity saturation mode and thus allows for high linearity between integrated photo charges and output current of the pixel. Furthermore, I have employed a feedback mechanism within every pixel in the imaging array in order to ensure that all readout transistors operate in velocity saturation mode, and improve linearity and matching of output currents across the imaging array. The performance of the proposed image sensor is validated by empirical results from a fabricated chip. Preliminary results from the proposed imaging sensor are presented in [48]. In this chapter, I have expanded the previously published results and have included additional measurements from the fabricated image sensor. Specifically, I have included: temporal and spatial noise performance i.e. signal-to-noise ratio (SNR) and fixed pattern noise (FPN), accuracy of analog memory cell used for correlated double sampling operation, and read-out frame rate of the image sensor. I have also provided in depth theoretical overview of the image sensor operation and the circuits used to realize this sensor.

The rest of this chapter is organized as follows. In Section 2.2, I present theoretical overview of velocity saturation as a prominent operation mode of transistors in small feature technologies. In Section 2.3, I describe the architecture of the proposed CMOS imaging sensor and describe all the circuits implemented in the fabricated chip. In Section 2.4, I present measurements from single transistors fabricated in 0.18 micron process and discuss the velocity saturation mode of operation. In Section 2.5, I present measurements from the fabricated imaging sensor. Concluding remarks are presented in Section 2.6.

## 2.2     Theoretical Overview of Velocity Saturation

As CMOS technology continues to scale down according to Moore's law, transistors are starting to deviate from the traditional modes of operation such as cut-off, sub-threshold, linear, and saturation modes. For example, short channel transistors

implemented in small feature technologies are also observed to operate in velocity saturation mode. The velocity saturation mode of operation can be explained as follows. Assume that an NMOS transistor operates in the saturation mode. The drain current $I_{ds}$ of this transistor can be described by equation (2.1).

$$I_{ds} = \frac{\mu C_{ox} W}{2L} (V_{gs} - V_T)^2 (1 + \lambda V_{ds})$$

(2.1)

In equation (2.1), W is the channel width of the transistor, L is the channel length, $\mu$ is the carrier mobility, $V_{gs}$ is gate-to-source voltage, $V_{ds}$ is drain-to-source voltage, $V_T$ is threshold voltage, and $C_{ox}$ is the gate oxide capacitance per unit area. The drain current of the transistor has a square relationship with the overdrive voltage ($V_{gs}$-$V_T$). An increase in drain-to-source voltage ($V_{ds}$) contributes to the reduction of effective channel length, a condition referred to as channel length modulation that is modeled by the $\lambda$ term in equation (2.1). The channel length modulation effect makes the drain current of a transistor operating in the saturation mode to be dependent on the drain to source ($V_{ds}$) potential.

The velocity of mobile electron carriers ($v$) in the inverted channel layer of the transistor is a function of electron mobility ($\mu$) and electric field (E), i.e. $v = \mu E$. As transistors are scaled down, the effective channel length decreases, which causes the lateral electric field ($E_y$) along the channel to increase. Consequently, the velocity of mobile electron carriers increases proportionally to the increasing lateral electric field in transistors. When the electric field is higher than a critical value $E_C$, then the carrier velocity approaches a saturated velocity $v_{sat}$ due to collision and scattering among electron carriers. If the lateral electric field is increased above the critical value, the carrier velocity remains constant. Hence, the drain potential, $V_{ds}$, which sets the lateral electric field to $E_C$ is typically denoted as $V_{ds,sat}$. The carriers may achieve the saturated velocity at some point along the channel or throughout the entire channel as they propagate from source diffusion region to drain diffusion region. When this phenomenon

is achieved, the transistor is said to operate in velocity saturation mode. The drain current $I_{ds}$ for a transistor operating in velocity saturation mode is described by (2.2) as modeled in [49-52].

$$I_{ds} \approx WC_{ox}v_{sat}(V_{gs} - V_T - V_{ds,sat})$$
(2.2)

In equation (2.2), the drain current is a linear function of the overdrive voltage ($V_{gs}$-$V_T$) and transistor's width. The drain current is independent of the transistor's channel length. This leads to the conclusion that the output impedance is infinite for a transistor operating in velocity saturation mode. In reality, the transistor has high impedance and experiences "channel length modulation" effects similar as in the normal saturation mode of operation. These channel length modulation effects are due to the fact that the electrons traveling across the channel can operate in velocity saturation only through part of the channel and operate in traditional saturation mode of operation through the rest of the channel. Modeling these higher order effects in the drain current of a transistor operating in velocity saturation are under an active area of research and are currently determined empirically.

# 2.3 Utilizing Velocity Saturation for Imager Design

The velocity saturation mode of operation provides a linear relationship between the gate potential and drain current. This property can be utilized in the pixel design of current mode image sensors. In such a design, the pixel's read-out transistor can operate in the velocity saturation mode and an output current proportional to an integrated photo voltage is provided to a read-out circuitry. Hence, the output current from a pixel is linearly dependent on the accumulated photo voltage across a photodiode, as described by equation (2.2). This linear relationship can be used to correct for threshold voltage

variations across the imaging array by employing correlated or double delta sampling techniques.

When designing a large array of pixels, where individual pixel's read-out transistors operate in the velocity saturation mode of operation, the parasitic impedance on the read-out bus has to be taken into account for the correct operation of the imaging sensor. For example, assume that an imaging array is composed of 1000 by 1000 pixels, with column parallel read-out scheme. Let's take into consideration two pixels in a single column of pixels. The first pixel is located at the beginning of the column and the second pixel is located at the end of the column. Both pixels are connected to the same read-out bus and the read-out circuitry will be approximated as a serial connection of a voltage source and a current meter as shown in Figure 2.1. Note, a typical read-out circuit for current mode imagers is a current conveyor and I have approximated part of the functionality of this circuit as it pertains to my discussion with a voltage source and a current meter. The last pixel in the column will be closest to the read-out circuit. Therefore, the parasitic impedance between the pixel and the read-out circuit is close to 0 $\Omega$. The drain potential of the read-out transistor in this pixel will be $V_{ref}$.

The first pixel in the column will be placed furthest from the read-out circuit and this pixel "will see" large parasitic impedance between the read-out transistor and read-out circuitry, i.e. the current conveyor. For example, if the read-out bus is implemented in metal 3-layer in 0.18 micron technology and the pixel pitch is set to 25 microns, then the parasitic impedance per pixel is ~5 $\Omega$. For an imaging array of 1000 pixels and average output current of 200µA per pixel, the voltage drop across the parasitic impedances on the read-out bus is ~1V. Such a large voltage drop across the read-out bus, which is further exacerbated due to the photo dependent output current, can push the read-out transistor away from velocity saturation into the traditional saturation mode of operation and increase the non-linearity of the output current.

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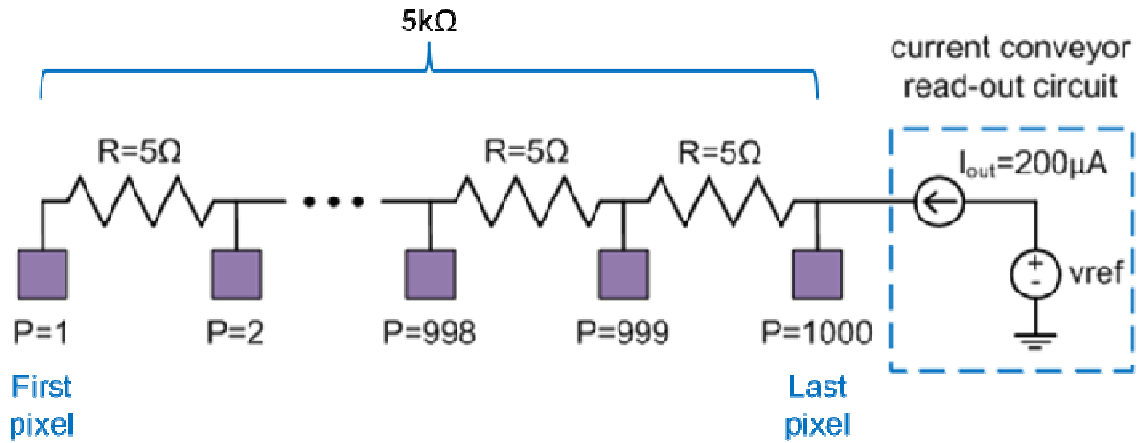
Figure 2.1. Parasitic impedance on the read-out bus that connects read-out transistors of 1000 pixels in a column to a current conveyor read-out circuit.

In order to mitigate this side effect in current mode imaging sensors, I propose a read-out circuitry that employs a feedback mechanism in order to compensate for the voltage drops across the read-out bus. The proposed read-out circuitry pins the drain potential of the read-out transistor and maintains a constant potential independent of the pixel's position or the amount of output current. The details of the current conveyor with feedback mechanism together with the pixel design are explained in the next section.

## 2.4 Imaging Sensor's Block Level Organization

I have designed, fabricated and tested a prototype imaging sensor in 0.18 micron technology. A micrograph of the imaging sensor prototype is presented in Figure 2.2. The imaging sensor is composed of two separate imaging arrays, which are labeled A and B respectively. Both imaging arrays are composed of 54-by-60 photo pixels and column parallel read-out circuitry respectively. The imaging arrays share a set of common digital registers for accessing pixels in their respective photo arrays. The column parallel read-out circuitry is composed of a current conveyor circuit and an analog memory cell for performing correlated double sampling (CDS).

The first imaging array (A) contains a current conveyor circuit with feedback mechanism in order to ensure that all read-out transistors operate in velocity saturation mode. In contrast, the second imaging array (B) contains a current conveyor without feedback mechanism. Therefore, the second imaging array serves as a basis for comparison when evaluating performance of the feedback mechanism in the first imaging array.
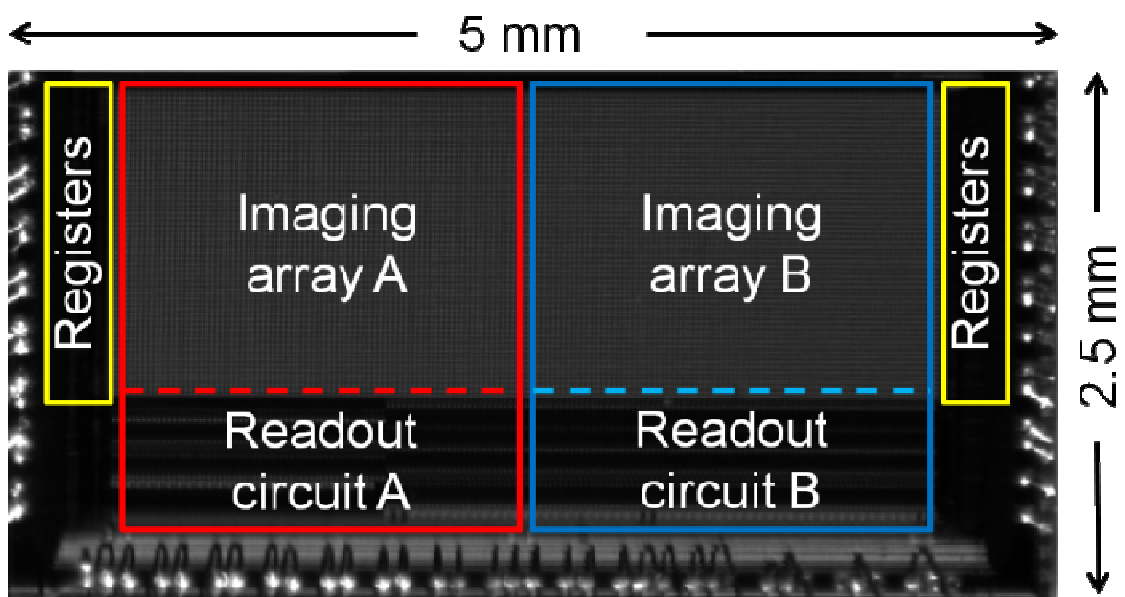


Figure 2.2. Micrograph of the fabricated CMOS imaging sensor.

The entire signal processing paths starting from the pixel circuitry all the way to the read-out circuitry for both imaging arrays are presented in Figure 2.3 and Figure 2.4 respectively. Next, I will discuss in detail the functionality of each circuit block for both imaging arrays.

## 2.4.1      Photo Pixel

Schematic diagrams of the photo pixel implemented in the imaging array A and imaging array B are presented in Figure 2.3a and Figure 2.4a respectively. The photo

pixel is composed of a pinned photodiode (PD), charge transfer transistor (T1), reset transistor (T2), readout transistor (T3), and feedback switch transistor (T4). The feedback switch transistor controls access to the feedback bus of the current conveyor. However, the pixel does not contain a switch transistor in order to control access to the readout drain bus. Instead, the gate voltage of the pixel's readout transistor (T3) is set to zero potential in order to turn-off a pixel. Eliminating the access switch has the benefit of decreasing read-out noise and improved SNR for low light conditions as discussed in reference [36].

The readout transistor T3 is biased in velocity saturation mode in order to provide a linear relationship between the accumulated photo charges at the photodiode node and output current that flows through T3. The length of the read-out transistor is 0.35µm; i.e. minimum size, and has an additional channel implant layer. The channel implantation layer shifts the formation of the channel in the transistor a few nanometers below the interface of $Si\text{-}SiO_2$, such that the flicker noise is effectively reduced.

During the integration mode of operation, the transfer transistor is turned off in order to isolate the photodiode (PD) from the floating diffusion node (FD). The FD node is set to ground potential via the reset transistor during the integration period to turn-off a pixel. During the read-out phase, the FD node is set above the threshold voltage of T3, effectively providing a current on the read-out drain bus. The FD node is set to 2.5 V during the reset phase. The minimum voltage on the FD node is limited to 1.5 V to maintain high linearity, i.e. constant transconductance, $g_m$, of the read-out transistor.
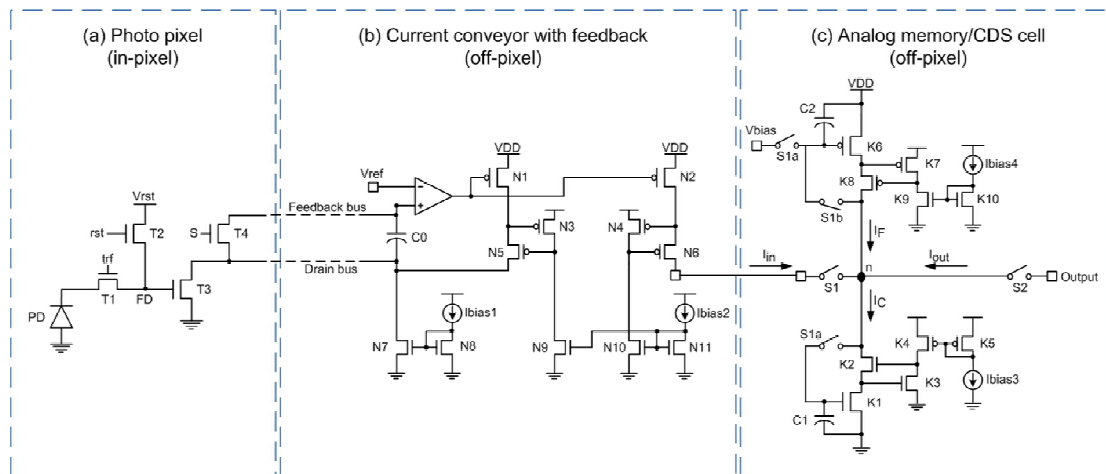
Figure 2.3. Schematics of photo pixel (a), current conveyor with feedback mechanism (b), and analog memory/CDS cell (c).
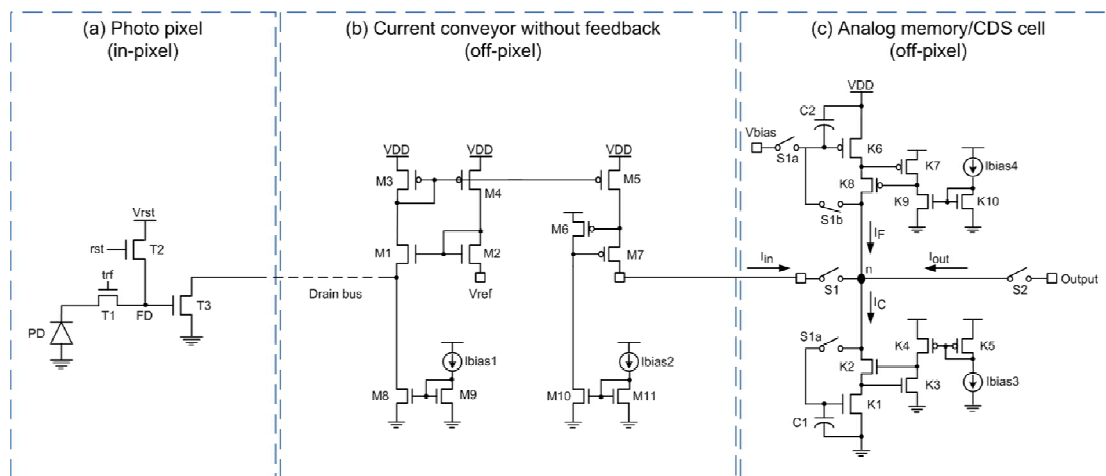


Figure 2.4. Schematics of photo pixel (a), current conveyor without feedback mechanism (b), and analog memory/CDS cell (c).

## 2.4.2 Current Conveyor with Feedback Mechanism

The current conveyor circuit with feedback mechanism is presented in Figure 2.3b. It is composed of a two stage operational amplifier (op-amp) connected in a negative feedback configuration via transistors N1, N3 and N5. The current conveyor

senses the potential on the drain node of the read-out transistor T3 via the feedback bus and compares it against the $V_{ref}$ potential applied at the negative terminal of the op-amp. The difference between the input nodes of the positive gain op-amp is amplified and sets the gate potential of transistor N1, which acts as a negative gain stage. The current supplied by transistor N1 charges or discharges the drain potential of read-out transistor T3 so that it matches $V_{ref}$ potential.

For example, assume that the current conveyor circuit is at a steady state and the positive terminal of the op-amp matches the $V_{ref}$ potential of 1.8V. The FD potential is set to 2V via the integrating photodiode, and thus a current of 100µA is flowing on the drain bus. If the FD node is set to 2.5V during the reset mode, the drain current of transistor T3 will increase to 200µA. However, the current flowing through N1, which is biased in the saturation regime, would remain at 100µA because $V_{sg}$ and $V_{sd}$ of N1 remain unchanged. In order to equalize the two currents, transistor T3 will start to discharge its drain potential due to the excess current demanded by this transistor. Hence, the potential on the positive terminal of the op-amp will start to decrease, which will further decrease the output of the op-amp. The gate-to-source potential of PMOS transistor N1 will therefore increase and cause the current flowing through transistor N1 to increase. Transistor T3 will start to charge its drain potential and eventually set it to 1.8V. The drain potential of T3 would then match the $V_{ref}$ potential applied on the negative terminal of the op-amp. Since one end of the feedback bus is connected to the gate terminal of the input transistor in the op-amp, the current in this bus is zero. Therefore, the parasitic impedance across the feedback bus does not affect the drain potential on the read-out transistor. In other words, the drain potential on the read-out transistor is always equal to the $V_{ref}$ potential applied at the negative terminal of the op-amp.

PMOS transistors N1 and N2 form a current mirror and effectively replicate the current flowing on the read-out drain bus to the output branch of the current conveyor. The output current from the current conveyor serves as an input to the analog memory

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cell. Regulating structures implemented using transistors N3 through N6 pin the drain node potentials of N1 and N2 in order to mitigate channel length modulation effects and thus improve current copying capability of the current conveyor. NMOS transistors N7 through N11 form current mirrors which supply the biasing currents to the current conveyor circuit. The current mirrors are implemented as cascode structures in order to mitigate channel length modulation effects.

## 2.4.3  Current Conveyor without Feedback Mechanism

The current conveyor circuit without feedback mechanism is presented in Figure 2.4b. The conveyor circuit is interfaced to the photo pixel's read-out transistor without utilizing the feedback switch transistor (T4). The conveyor circuit is implemented using a pair of PMOS and NMOS current mirrors. PMOS transistors M3, M4, and M5 form a current mirror that ensure currents flowing through transistors M1, M2, and M7 are equal. The output current from the accessed pixel is mirrored using PMOS transistors M3 and M5, and supplied to the analog memory cell. Similarly, NMOS transistors M1 and M2 form a current mirror. Hence, potential at the source terminal of M1 will be the same as the reference potential, $V_{ref}$, applied at the source terminal of M2. Consequently, drain node potential of the read-out transistor (T3) is set to $V_{ref}$ potential. The current conveyor also includes a regulating structure implemented using transistors M6 and M7 that pins the drain node potential of M5 in order to mitigate channel length modulation effects and thus improve current copying capability of the current conveyor. Similarly, NMOS transistors M8 through M11 form current mirrors that supply biasing currents to the current conveyor circuit.

## 2.4.4  Analog Memory Cell

The analog memory cell is the last block in the image processing pipeline prior to

digitization of the current signals, which is performed by an off-chip current-to-voltage converter and a 14-bit analog to digital converter (ADC). Schematic diagrams of the analog memory cell are presented in Figure 2.3c and Figure 2.4c. The analog memory cell is based on a two-step switched-current design [53]. The input current signal is memorized in two steps: coarse and fine memorization steps. The timing diagram for memorizing an input is shown in Figure 2.5.
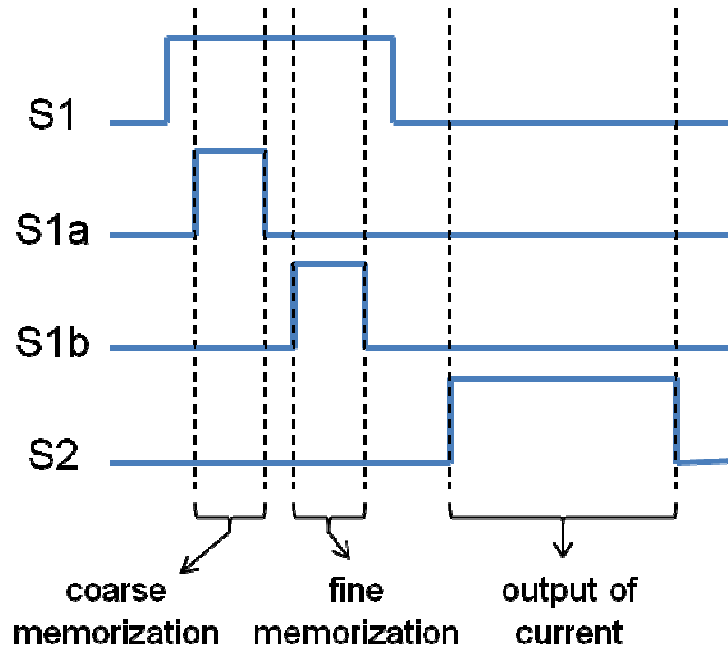


Figure 2.5. Timing diagram of memorizing an integrated output current.

The coarse memorization step is initialized by first closing switch S1, which allows the integrated output current, $I_{int}$, from the accessed pixel to flow into the memory cell as $I_{in}$. Next, switch transistor S1a is closed and the gate of transistor K6 is connected to $V_{bias}$ potential. Hence, a bias current, $I_{bias}$, is supplied by transistor K6. The input current, $I_{in}$, is summed with the bias current, $I_{bias}$, and the summed current, $I_C$, flows through the diode connected transistor K1. The current $I_C$ is sampled and memorized by opening the switch S1a. As the switch S1a is opened, an error current, $I_{error\_coarse}$, due to charge injections and clock feedthrough is introduced into the memorized current. This

error current is proportional to the input current and therefore introduces an offset which is related to the magnitude of the input current. The memorized current in the coarse cell is shown by equation (2.3).

The fine memorization step occurs when the switch S1b is closed. The bias current, $I_{bias}$, and the coarse memorization error current, $I_{error\_coarse}$, are sampled and memorized by the fine memory cell implemented via a diode-connected transistor K6 and storage capacitor C2. During the sampling phase, charge injection errors and clock feed through errors are introduced in the current memorized in the fine cell and is described by equation (2.4).

Finally, the memorized current signals are delivered simultaneously from both coarse and fine memories when switch S2 is closed and switch S1 is open. The final output current from the analog memory cell, $I_{out}$, is approximately equal to the integrated output current from the accessed pixel. The coarse memorization error cancels out as shown by equation (2.5). Since the current that is memorized during the fine stage is much smaller than the current memorized during the coarse stage, the error introduced during the fine memorization stage is much smaller than the error introduced during the coarse memorization stage. Therefore, the output current from the memory cell has a small error current associated with the sampling of the input current [53].

$$I_C = I_{int} + I_{bias} + I_{error\_coarse} \tag{2.3}$$

$$I_F = I_{bias} + I_{error\_coarse} + I_{error\_fine} \tag{2.4}$$

$$I_{OUT} = I_C - I_F = I_{int} + I_{error\_fine} \tag{2.5}$$

The current memory cell allows for an on-chip implementation of CDS, which involves subtracting the integrated photocurrent ($I_{int}$) from the reset current ($I_{rst}$) of the accessed pixel as shown by equations (2.6) through (2.8). In order to implement the CDS operation, switch S1 remains closed throughout the entire mode of operation.

Switch S2 is open during the memorization stage of the integrated photocurrent, which is performed at the end of the integration period. After the integrated photocurrent is memorized in the analog memory cell (see equation 2.6), the pixel is reset to $V_{rst}$ potential and a reset current flows in the memory cell (see equation 2.7). At this point, switch S2 is opened and the output current from the memory cell is the difference between the reset current and the integrated photocurrent. The output current is described by equation (2.8).

$$I_{int} \approx W C_{ox} v_{sat} (V_{int} - V_T - V_{ds,sat})$$ (2.6)

$$I_{rst} \approx W C_{ox} v_{sat} (V_{rst} - V_T - V_{ds,sat})$$ (2.7)

$$I_{rst} - I_{int} = W C_{ox} v_{sat} (V_{rst} - V_{int})$$ (2.8)

The threshold voltage of the read-out transistor, $V_T$, which is unique and different for each pixel in the imaging array, is eliminated during the CDS operation as shown by equation (2.8). Therefore, the CDS operation improves noise characteristics of the imager by suppressing fixed pattern noise caused by threshold voltage variation in read-out transistors.

The analog memory cell also includes regulating structures implemented using transistors K2, K3, K7, and K8 in order to mitigate channel length modulation effects and thus improve accuracy of the memory cell. Similarly, transistors K4, K5, K9, and K10 form current mirrors that supply biasing currents to the regulating structures of the memory cell.

## 2.4.5  Column Parallel Readout Scheme

The imaging sensor employs column parallel readout scheme in order to access and process pixel values. Integrated output currents from all pixels within the same row

are read out simultaneously using their respective current conveyors located at the end of each column. The readout integrated output currents are then memorized simultaneously using analog memory cells that are also located at the end of each column. CDS signals are then computed in parallel and stored by the respective analog memory cells. The CDS values held in memory cells are then accessed sequentially and digitized by an off-chip ADC.

## 2.5    Measurements of Velocity Saturation Mode of Operation

The fabricated test imager contains several minimum size transistors placed at the periphery of the imaging array. Figure 2.6a presents the measured drain-to-source current of the test transistors as a function of the gate voltage for several different drain potentials. The test transistors have threshold voltage of 0.4V. When the drain voltage is set to 0.3V and 1V respectively, the transistor operates in the saturation (linear) region for $V_{gs}$ potential less (larger) than 0.7V and 1.4V respectively. For $V_{ds}$ potential above 1.6V, the transistor enters velocity saturation when the gate voltage is between 1V and 3V. In this region, the drain current is linearly proportional with respect to the gate potential as described by equation (2.2).

The velocity mode of operation can be also verified from the transconductance plot presented in Figure 2.6b. The transconductance, $g_m = \partial I_{ds} \big/ \partial V_{gs}$ , is relatively constant for drain potentials between 1.6V and 2V and gate potentials between 1.3V and 3V. In this region, the transistor operates in velocity saturation and the transconductance is constant. In the other region, the transistor operates in regular saturation mode and the transconductance is linearly dependent on the gate potential. From these measurements, I can conclude that the read-out transistor in the pixel should be biased such that the drain potential is set between 1.6V and 2V and gate potential, i.e. the integrated photo voltage,

range should be between 1.3V and 3V.
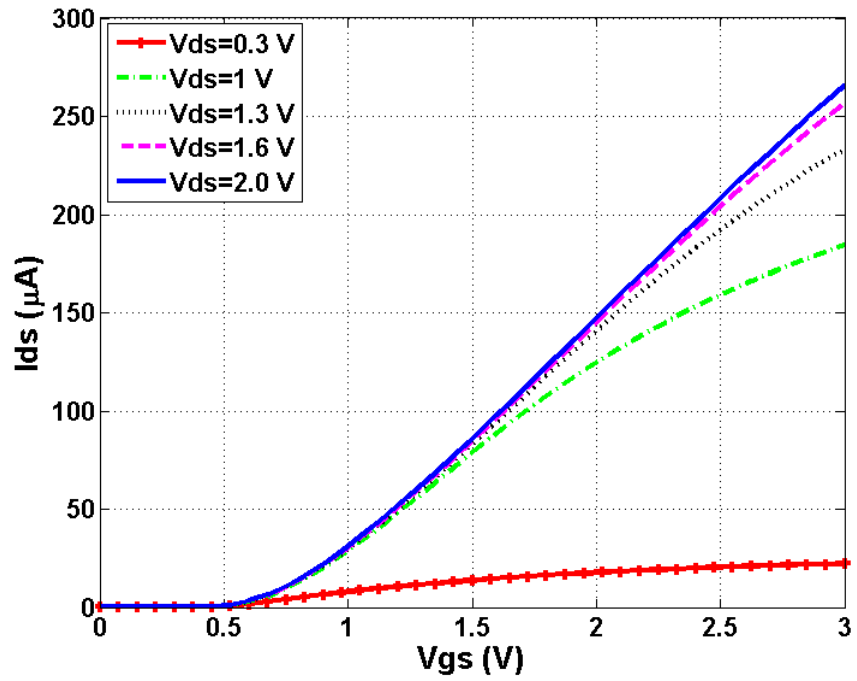


Figure 2.6. (a) Measured current-voltage for a short channel transistor (W=L=0.35µm) fabricated in 0.18µm process.
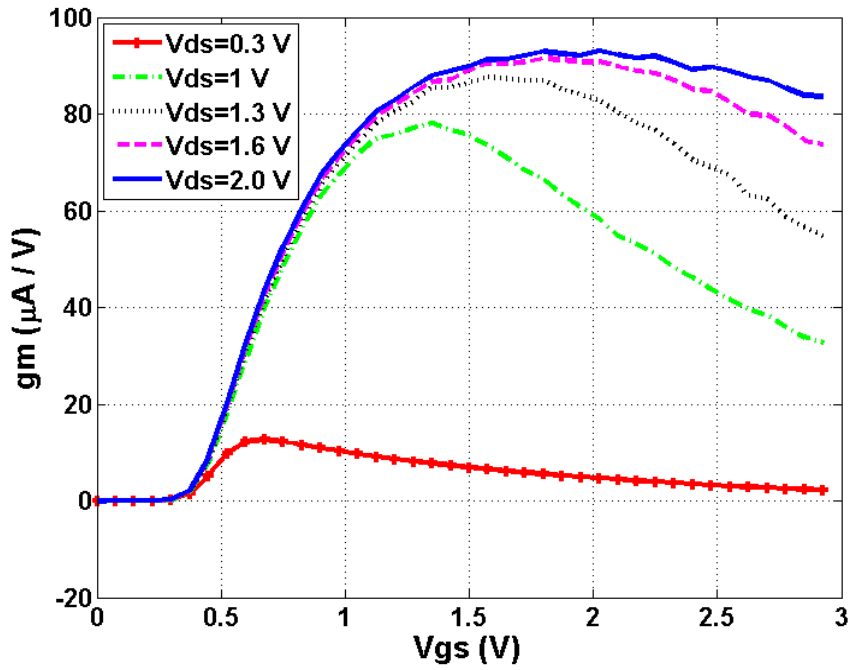
Figure 2.6. (b) Measured transconductance for a short channel transistor (W=L=0.35µm) fabricated in 0.18µm process.

# 2.6    Experiments and Results

## 2.6.1  Electro-optical Setup
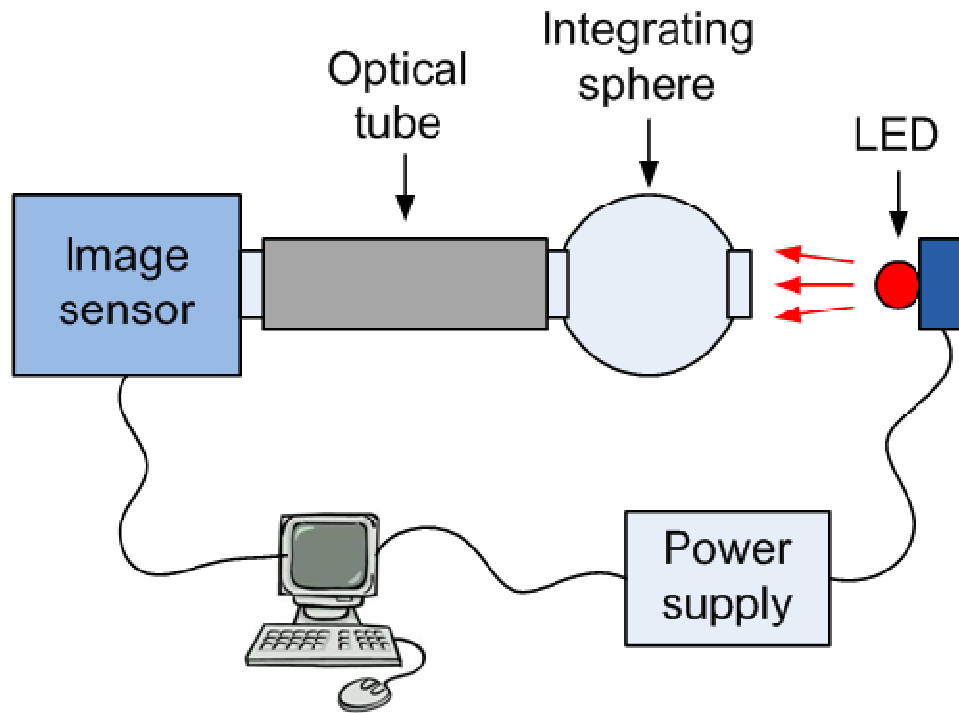
Figure 2.7. Electro-optical setup for evaluation of the fabricated image sensor.

Electro-optical setup for evaluating the performance of the fabricated CMOS image sensor is shown in Figure 2.7. The image sensor is illuminated with uniform light of 625nm supplied by narrow band OVTL01LGA LED via an integrating sphere. Optical power of the LED is modulated using a GPIB programmable Agilent E3631A power supply. The optical power of the illuminating light is verified using a calibrated photodiode. The setup is used to evaluate photo response of pixels, temporal noise performance, and spatial noise performance.

## 2.6.2 Performance of Analog Memory Cell

Performance of the analog memory cell is crucial to the overall performance of the fabricated imaging sensor. As the last block in the imaging pipeline, the analog memory cell memorizes the integrated photocurrent signal of the accessed pixel and computes a CDS current signal.

I have evaluated the accuracy of the analog memory cell by measuring the CDS output current for a pixel that is continuously in a reset mode. The reset voltage is varied throughout the experiment in order to simulate different levels of input currents to the memory cell. The CDS output current is expected to be zero because both the reset and integrated photocurrent currents are equal in this experiment. A non-zero CDS signal would indicate an error that is introduced by the memory cell. In Figure 2.8, I present the measured CDS error plotted as a function of the pixel output current. The memory cell has an average CDS error of 0.58µA for an output current range of 0µA to 180µA produced by the pixel that is continuously reset. The standard deviation of the CDS error is 0.022µA. The average CDS error can be subtracted off-chip as an offset from the output current.
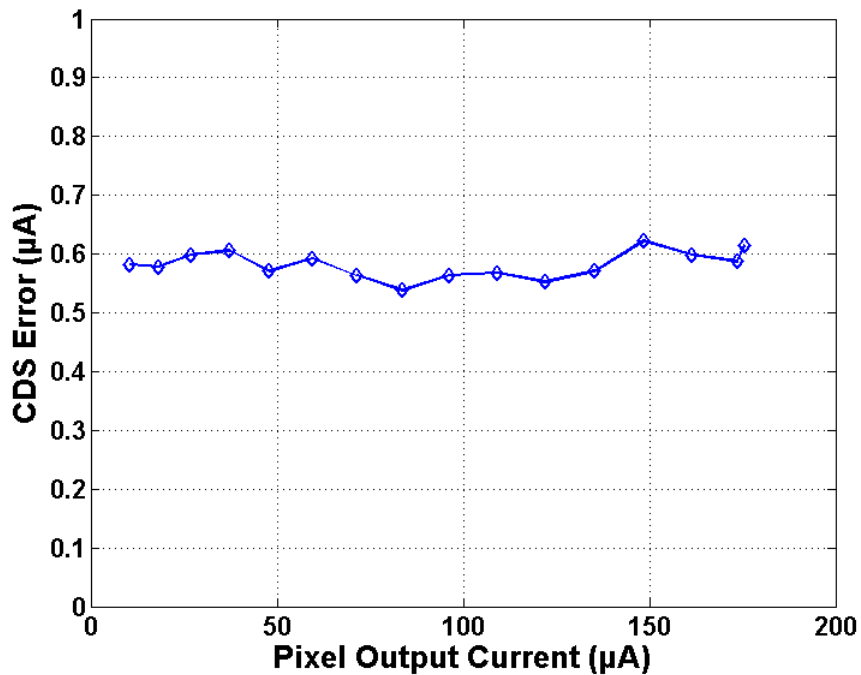


Figure 2.8. CDS error as a function of pixel output current.

# 2.6.3  Photo Response of a Pixel

The photo responses from a single pixel with and without feedback in the readout circuitry are evaluated using the setup shown in Figure 2.7. The photodiode of the pixel is reset to 2.5V and then allowed to integrate photo charges for 15ms for light intensity of $0.5mW/cm^2$. A total of 128 image frames are recorded and averaged to eliminate temporal fluctuations. The output current from the pixel with feedback and without feedback as a function of the integration time are shown in Figure 2.9. The linearity of the output current is evaluated for a pixel furthest from the current-conveyor, i.e. the first pixel in the column. Linearity of the output current for a pixel with feedback is 99.49% and for a pixel without feedback is 98.28%. The nonlinearity is computed as root mean square value of residuals normalized to the output current. The mean output referred conversion gain of the pixel is $2.09x10^{-4}\,\mu A/e^-$.

The improved linearity of the pixel's output current with feedback is due to the fact that the drain potential of the readout transistor is kept constant at 1.8V for the entire integration period. For the pixel without feedback, the drain potential on the readout transistor is a function of the output current and varies during the integration period. This effect is further exacerbated in large imaging arrays, where the parasitic impedance on the readout bus can be much larger than my fabricated imager. Spice simulations indicate that the linearity of a pixel in an imaging array of 1000 by 1000 pixels will drop to 91% if the current conveyor does not employ a feedback mechanism. The linearity remains higher than 99% when feedback is used in large imaging array of 1000 by 1000 pixels, as indicated by Spice simulations.
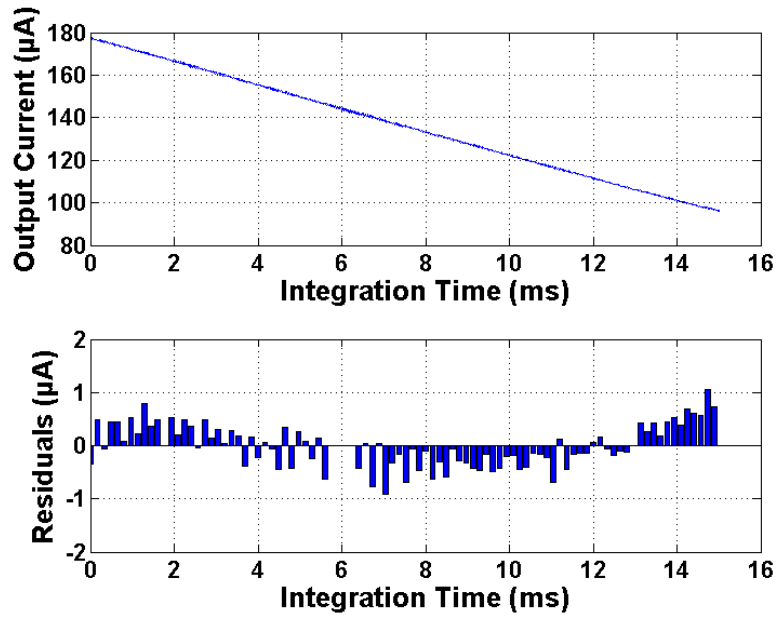
Figure 2.9. (a) Output current of a pixel with feedback is plotted as a function of integration time. Residuals from linear fit of the output current are also plotted.
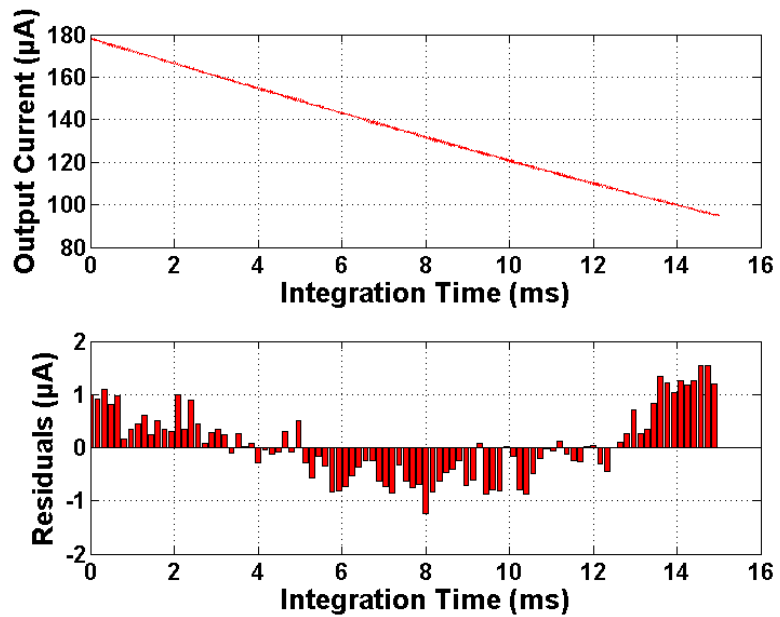


Figure 2.9. (b) Output current of a pixel without feedback is plotted as a function of integration time. Residuals from linear fit of the output current are also plotted.

The photo response of the pixel array is evaluated as a function of optical power. For this study, the image sensor is exposed to uniform light intensity that is modulated from 0.012µW/cm$^2$ to 1.85µW/cm$^2$. A total of 128 image frames are recorded for each of the light intensities with an integration period of 167ms. The image frames are averaged for every pixel in order to eliminate temporal fluctuations. Output currents from all pixels of the imaging arrays are averaged and plotted as function of optical power as shown in Figure 2.10.
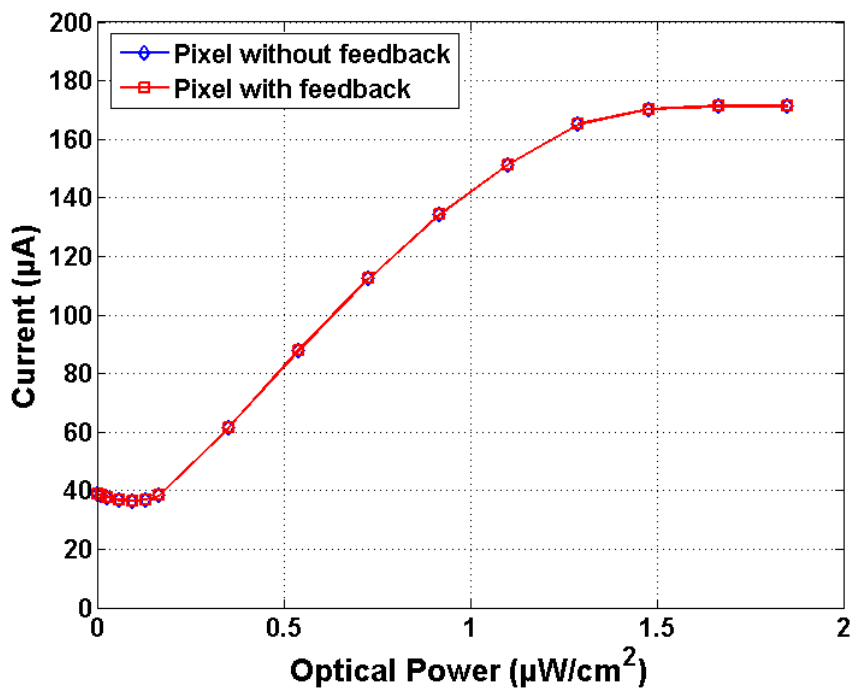


Figure 2.10.  Average output CDS currents from imaging arrays are plotted as function of optical power.

The pixels produce an average CDS output current of 40µA immediately after the reset event in dark conditions. The CDS value of 40µA is computed on-chip as reset output current of 200µA less the integrated output current of 160µA that is recorded immediately after the reset event. The abrupt drop of 40µA in the output current occurs immediately after the reset event when the reset transistor is turned off. The abrupt drop in output current is due to charge injection from the channel in the reset transistor and

from the clock coupling via gate-to-source overlap capacitance in the reset transistor. The pixels produce an average CDS output current of 180µA when they become saturated. The performance of both pixels with and without feedback employed in the readout circuitry is virtually the same. This is due to the fact that the imaging array is small and the parasitic impedance on the readout bus is small. Hence, the difference in the current levels in both pixels is minimal.

# 2.6.4  Temporal Noise Performance

Temporal noise performance of the fabricated image sensor is characterized using signal to noise ratio (SNR), which compares level of desired signal relative to noise level. Similarly, a total of 128 image frames are recorded for each of the light intensities using the aforementioned experimental setup and light conditions. SNR of a single pixel is computed as a ratio of the average output current signal over the standard deviation of the output current signal across the 128 image frames. Average SNR from the imaging arrays are plotted as a function of optical power as shown in Figure 2.11. The SNR at low light intensities for the imaging array with feedback vs. the imaging array without a feedback is about 2dB higher. The feedback readout circuitry employs a low noise op-amp, which leads to high SNR measurements of the corresponding imaging array. The input refereed noise of the amplifier is 0.1662 mV. At low light intensities the imaging sensor is limited by the read-out electronics thermal and 1/f noise. For medium to high light intensities, the SNR is the same for both readout circuits. For these light intensities, the imaging sensor is limited by the shot noise of the photodiode. Since the photodiode area for both imaging arrays is the same, the SNR is the same for these pixels. The pixels achieve maximum SNR of 58dB.
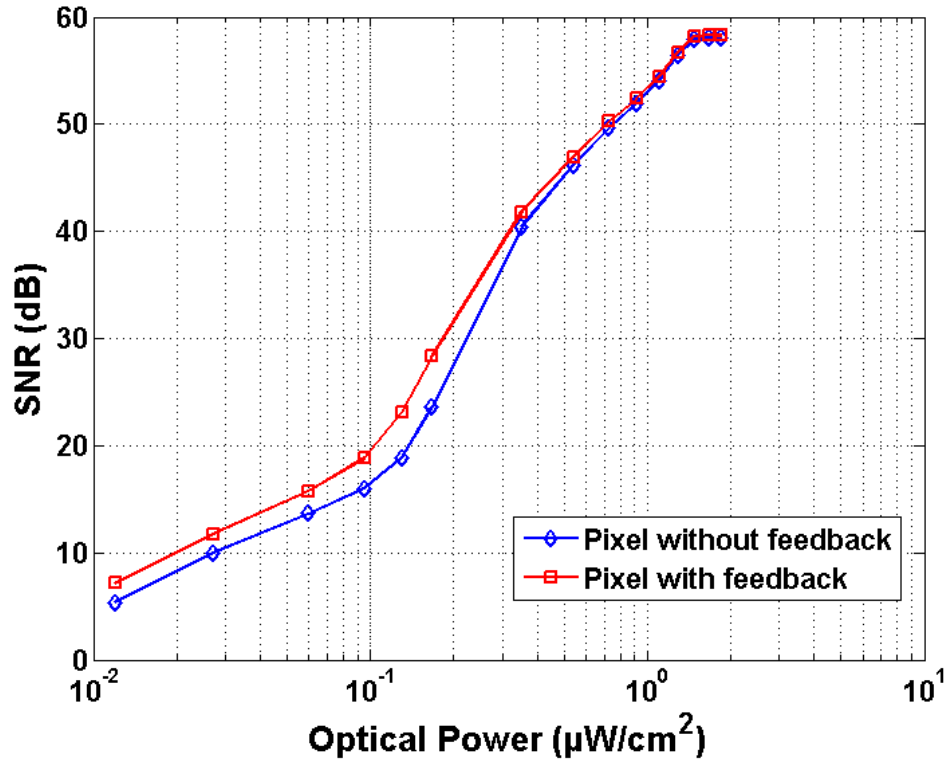
Figure 2.11.  SNR of pixels as a function of optical power.

# 2.6.5  Spatial Noise Performance

Spatial noise performance of the fabricated image sensor is characterized using fixed pattern noise (FPN). Similarly, a total of 128 image frames are recorded for each of the light intensities using the aforementioned experimental setup and light conditions. The image frames are averaged for every pixel in order to eliminate temporal fluctuations. FPN is computed as a ratio of standard deviation of output current across the average image frame, which is then normalized to the saturated output current. FPN measurements from the imaging arrays are plotted as a function of optical power as shown in Figure 2.12.
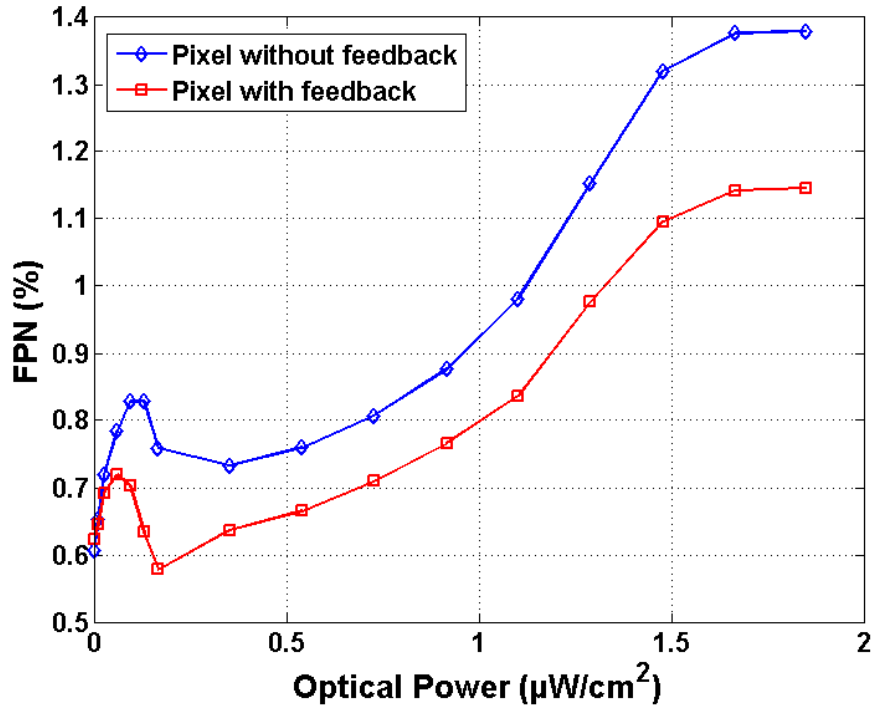
Figure 2.12. FPN of pixels as a function of optical power.

The imaging array with feedback mechanism has relatively lower FPN and therefore it has better spatial noise performance than the imaging array without feedback mechanism. The feedback mechanism ensures that all read-out transistors operate in velocity saturation mode and hence it improves linearity of the pixel's output current compared to the ones without feedback, as shown in Figure 2.9. Due to the improved linearity of the output current, the on-chip CDS circuits reduce spatial noise better for the imaging array that employs feedback readout circuits over the imaging array without feedback readout circuitry. The measured FPN in the dark is 0.6% for both imaging arrays.

## 2.6.6  Performance of Readout Speed

The image sensor implements column parallel readout scheme in order to access and process pixel values from the imaging array. Integrated output currents from pixels

within the same row are read out simultaneously. Their CDS values are computed in parallel and stored by their respective analog memory cells. The final current outputs are then accessed sequentially. The read-out speed of the image sensor is limited by the bandwidth of the current conveyor and analog memory cell. The time required to read out a single CDS value of a pixel with feedback from the memory cell is 647ns as shown in Figure 2.13. Therefore, the imaging array of 54x60 pixels can be accessed in 2.1ms.
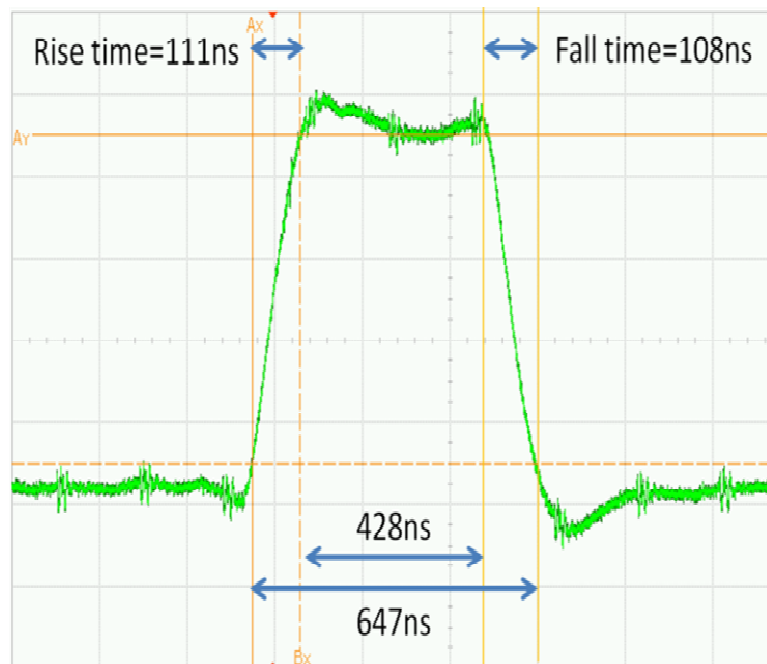


Figure 2.13.  Time to read out a single CDS from analog memory cell.

## 2.6.7  Sample Intensity Images

I present intensity images recorded with the fabricated image sensor in Figure 2.14. The intensity image obtained with implementation of both feedback mechanism and CDS techniques show improved spatial noise performance relative to the intensity image obtained with neither of the techniques.

<center>(a)                               (b)</center>
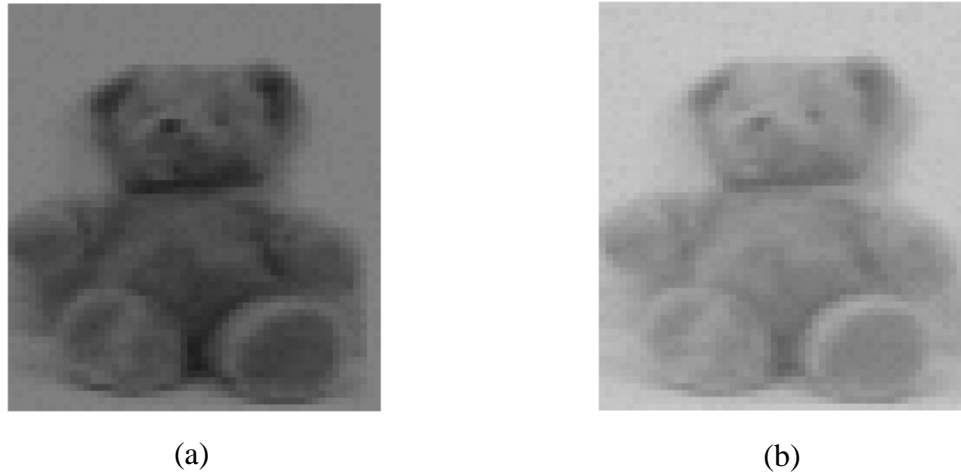
Figure 2.14. Intensity images recorded by the fabricated image sensor: Without feedback and without CDS (a); with feedback and with CDS (b).

# 2.7     Conclusion

In this chapter, I investigated whether we can utilize transistors operating in velocity saturation to design mixed mode circuits and systems for imaging sensors. I presented a current mode CMOS imaging sensor with in-pixel read-out transistor operating in velocity saturation mode. The sensor employs a novel current conveyor circuitry that pins the drain potential on the read-out transistor of individual pixels using a feedback mechanism and improves spatial matching across the imaging array. The imager has pixel pitch of 25µm, and frame rate of 100 fps for imaging array of 54-by-60 pixels. Experimental results indicate that the output current from the pixel is 99.49% linear for 1V range on the photo diode, i.e. on the gate terminal of the read-out transistor. The total power consumption of the imager is 270mW. The summary of the imaging sensor is provided in Table 2.1.

<center>33</center>

**TABLE 2.1 Summary of the imaging sensor performance**

| | |
|---|---|
| Technology | 0.18µm triple well CMOS |
| Array Size | 54 x 60 |
| Pixel Size (Fill Factor) | 25µm x 25µm (68%) |
| Chip Size | 5 mm x 2.5 mm |
| FPN without CDS | 0.70% of sat. level |
| FPN with CDS | 0.60% of sat. level |
| SNR | 58 dB |
| Pixel's linearity output | 99.49% |
| Frame rate | 100 fps |
| Conversion Gain | $2.09 \times 10^{-4} \mu A/e^{-}$ |
| Dynamic range | 52dB |
| Power Consumption @ 100 fps | 270 mW |

# Chapter 3

# Low Power Programmable Current-mode Computational Imaging Sensor

## 3.1    Background

Low power real-time image processing is crucial for many computer vision and robotics applications [54]. For these applications, real-time feature extraction and identification are critical tasks in order to establish a more reliable human-computer interface. Feature extraction algorithms are typically implemented by filtering the intensity image with a series of filters and performing these operations on per-pixel neighborhood over the entire imaging array. This operation is computationally expensive and requires high power processing units. For example, filtering a mega pixel imaging sensor with a kernel of size 5-by-5 pixels at 50fps would require 2.5GOPS.

CMOS imaging sensors have become an attractive choice for low power imaging and low power image processing due to the ability to monolithically integrate imaging elements and processing circuitry at the focal plane. The state-of-the-art computational imaging sensors can be divided into two groups of sensors. The first group of sensors incorporates imaging and digital signal processing on the same imaging chip [25-27]. For example, Cheng *et al.* presents a sensor composed of 128-by-128 imaging elements, 8 digital processing units, and one digital decision processing unit that aggregates the results from the other 8 processing units. In this imaging architecture, the digital processing units occupy more than 90% of the entire silicon area and the power consumption is 374mW for imaging at 2790 frames per second [27].

The second group of computational imaging sensors incorporates imaging and mixed-signal image processing on the same chip. This group of sensors can further be subdivided into three categories. The first category includes sensors that combine voltage mode active-pixel sensor (APS) with signal processing circuitry [32-35]. The signal processing circuitry is implemented with switch capacitors [33-35] or incorporated as part of the analog-to-digital converter [32]. In [32], spatiotemporal image processing is performed at the focal plane with variable size kernels (up to 8 by 8 pixels) at 30 frames per second with 26.2mW power consumption. This imaging sensor computes discrete wavelet transform video compression at video frame rates.

The second category of sensors incorporates image processing circuitry within the pixel [55-61]. This category of sensors, which has been inspired by biology [55, 56], realizes ultra low power image processing sensors at the expense of large pixel pitch, large temporal noise, and large spatial noise. The third category of sensors incorporates current mode imaging elements with current mode processing circuitry [36, 38-40, 42-46]. Some of the strongholds for current mode imaging sensors are high frame rate read-out, and computation-for-free during the read-out of the sensors.

Examples of current mode computational sensors include motion estimation [44], contour detection [39], and polarization sensors [45], to name but a few. The main limiting factor in current mode image sensors is low image quality due to the large fixed pattern noise (FPN) and large temporal noise. The computational imaging sensor presented in [44], performs convolution on the incident image with variable size kernels using low power analog circuits. The pixel pitch of this sensor is 30µm with fill factor of 20% implemented in 1.2µm CMOS process. This imaging sensor has relatively high fixed pattern noise of 2.5% and SNR of 38dB. The low power consumption of 1mW at 30fps for both imaging and on-chip image processing is a key stronghold for this computational imaging sensor architecture (see Table 3.1).

Dudek et al. [62] presented a SIMD image processing sensor employing current mode signal processing. Processing circuitry is embedded in each pixel and information is exchanged with nearest neighbors in order to perform efficient and low power convolution. The sensor computes 1.1 giga-instructions per second at 40mW of power consumption.

**Table 3.1 Performance Comparison of this Work with other Computational CMOS Imagers**

|  | **This work** | Gruev et al. [44] | Nilchi et al. [32] | Dudek et al. [62] | Wei et al. [63] |
|---|---|---|---|---|---|
| Technology | **0.6µm 3M2P CMOS** | 1.2µm NWELL CMOS | 0.35µm CMOS | 0.6µm CMOS | 0.18µm CMOS |
| Array size | **128 x 109** | 16 x 16 | 128 x 128 | 21 x 21 | 16 x 16 |
| Pixel size | **10µm x 10µm** | 30µm x 30µm | 15.4µm x 15.4µm | 98.6µm x 98.6µm | 30µm x 40µm |
| Fill factor | **30%** | 20% | 28% | 8.4% | 3% |
| Kernel size | **1x2-whole array** | 2x2-whole array | 2x2 – 8x8 | N/A | N/A |
| Kernel coefficients | **+/-3.9375 by 0.0625** | +/- 3.75 by 0.25 | 256 | N/A | N/A |
| FPN | **0.22% (DDS)** | 2.5% average (STD/mean) | N/A | 1% rms (FPN reduction) | N/A |
| SNR | **44dB** | 38dB | 32dB peak SNR | N/A | N/A |
| Dynamic range | **55dB** | 1 – 6000 Lux | N/A | N/A | N/A |
| Power consumption | **50mW** | 1mW @ 30fps, 5x5 kernel | 26.2mW total power (8x8 kernel) | 85µW per PE 40mW 1.1GIPS | 8.72mW @ 1.8V |
| Frame rate | **50fps** | DC - 400KHz | 30fps | 25fps @ 1000 Lux | 1000 fps |

The in-pixel analog image processing circuitry reduces the spatial sampling resolution of the imaged environment due to the large pixel pitch of 98.6µm. A similar SIMD image processing architecture was presented in [63], where row and column

parallel image processing at high frame rate was achieved. High pixel pitch of 30µm x 40µm due to in-pixel image processing circuitry limits the spatial sampling resolution of this sensor. The imaging sensor consumes 8.72mW power with 1.8V power supply while performing morphological image operations on the incident image (see Table 3.1).

Current mode imaging sensors are an alternative for low power and low noise imaging and image processing applications. Low FPN measurements of 0.7% [39] and 0.4% [36], based on saturated values, were achieved using integrative linear current mode and switchless APS. Implementations of velocity saturation current mode APS in [40, 64] have also shown reduction in spatial variation among pixels.

In this chapter, I present a linear current mode CMOS APS that performs spatial image processing at the focal plane. The imaging sensor combines current mode pixels with digitally programmable analog processing unit in order to compute convolution of the incident image at 50fps using 50mW of power. The sensor performs real-time image convolution via low power analog circuits. The low power imaging and image processing implemented on the same chip is an attractive solution for applications where convolution is a significant portion of the signal processing algorithm. On the other hand, the low power performance of this sensor may be less beneficial for applications where more sophisticated image processing are required. For these applications, additional image processing might be required to be implemented in power hungry digital signal processing units; hence marginalizing the benefits of low power image processing front ends for these applications.

Due to the implementation of a switchless pixel paradigm, spatial and temporal noise performance of the sensor has been improved compared to previous designs [44]. The image sensor has 128-by-109 pixel array, current conveyors, digital scanning registers, and digitally programmable analog processing units. Architecture and operation of the image sensor are validated by empirical results from a fabricated chip. Preliminary

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results of the proposed imaging sensor are presented in [65, 66]. In this chapter I have expanded the previously published results and have included additional measurements from the sensor. Specifically, I have included: linearity measurements of the pixel, linearity of the processing analog scaling unit, spatial and temporal noise measurements i.e. fixed pattern noise (FPN) and signal to noise ratio (SNR) measurement, timing diagram and real-life examples of imaging and on-chip image processing.

The rest of this chapter is organized as follows. The architectural overview of the image sensor as well as timing information of the operation of the sensor is presented in Section 3.2. Opto-electronic characterizations of the imaging sensor that include linearity, SNR, FPN, and sample images are presented in Section 3.3. Concluding remarks are presented in Section 3.4.

# 3.2    Architecture

A block diagram of the imaging sensor is presented in Figure 3.1. The imaging sensor is organized into an array of 128-by-109 photo pixels, column parallel readout circuitry, and a digitally programmable analog processing unit.
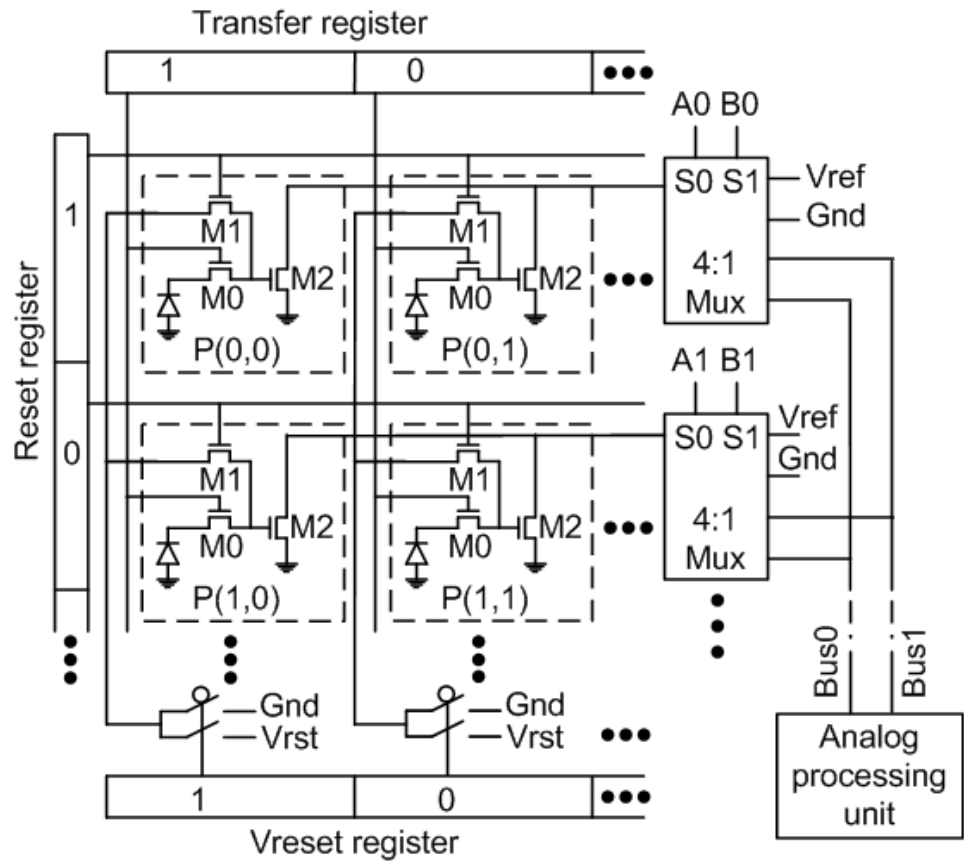
Figure 3.1. Block diagram of the imaging sensor. The sensor is composed of an array of pixels, column parallel readout circuitry and digitally programmable analog processing unit.

# 3.2.1  Photo Pixel

The photo pixel is based on the switchless linear current mode APS topology [36]. In this pixel topology, the switch transistor is eliminated from the pixel and the access of a pixel is controlled via the peripheral read-out circuitry.

The pixel is composed of three transistors: transfer transistor ($M_0$), reset transistor ($M_1$), and readout transistor ($M_2$). The transfer transistor has two purposes. First, it isolates the floating diffusion (FD) node from the photodiode when it is turned off. Hence, while the photodiode is integrating photo-generated electron-hole pairs, the FD

node can be set to an arbitrary potential without affecting the operation of the photodiode. The manipulation of the FD node potential allows for controlling the access of individual pixels in the imaging array as explained in the next section. Second, when the transfer transistor is turned on, the photodiode charges are transferred to the FD node. The photodiode is implemented as an n-diffusion/p-substrate with an area of $30\mu m^2$. The extracted photodiode capacitance is 19fF, while the floating diffusion capacitance, which is due to the gate capacitance of the read-out transistor, gate-to-source overlap capacitance of the transfer and reset transistors, and various metal interconnect capacitances, is ~3fF. Hence, about 86% of the accumulated photo generated charges are transferred to the FD node. The implementation of a pinned photodiode will facilitate this drawback and allow for full transfer of charges from the photodiode node to the FD node.

The reset transistor sets the FD node and the photodiode node to a predetermined potential ($V_r$). If $V_r$ is set to 3V, i.e. $V_r=V_{rH}$, the pixel is in the reset mode. The photodiode starts to accumulate photo-generated charges on its parasitic capacitance when the reset transistor is turned off, i.e. the pixel is in the integration mode of operation. The accumulation period for photo generated charges, i.e. integration period, is around 20 ms, which allows for imaging at 50 fps. The transfer transistor is turned off during the entire integration period of the pixel. At the end of the integration phase, the transfer transistor is turned on and the photo generated charges accumulated at the photodiode node are transferred to the FD node.

The readout transistor converts the accumulated charges at the FD node to an output current. The source node of the readout transistor is grounded and the drain node is connected to a column parallel readout circuitry, which allows for the manipulation of the drain potential of this transistor. The readout transistor in the pixel is biased in the triode region by ensuring that the drain potential during the reset and integration phases is always at least a threshold voltage below the gate potential. Hence, the output current during both reset and integration phases is described by equation (3.1).

$$I_{out} = \mu_n C_{ox} \frac{W}{L} \left[ \left(V_{FD} - V_t\right)^2 V_{ref} - \frac{V_{ref}^2}{2} \right]$$

<div align="right">(3.1)</div>

In equation (3.1), $V_{FD}$ is the FD node potential, $V_{ref}$ is set to ~0.2V, and the aspect ratio of the read-out transistor (W/L) is 1. The pixel outputs a maximum current during the reset phase, i.e. $V_{rH}=3V$, and is around 20μA. The minimum output current is achieved when the photodiode node is discharged to 1V and is ~1μA. Difference double sampling (DDS) is computed off-chip by first memorizing the integrated photo-current and then subtracting the reset photo current. The DDS operation eliminates the threshold voltage dependency on the final output current and improves spatial matching between the pixels' output currents in the imaging array.

## 3.2.2  Pixel Layout and Timing Control

The schematic of the pixel is shown in Figure 3.1. The pixel has two horizontal and two vertical buses. The directionality of these buses is imperative for the correct operation of the imaging sensor. First, the drain node of the readout transistor and the gate of the reset transistor are both connected to horizontal buses. Second, the drain node of the reset transistor and the gate of the transfer transistor are both connected to vertical buses. The directionality of these buses allow individual pixels to be accessed, i.e. individual integrated photocurrents to be readout and individual photodiodes to be reset without disturbing the photodiode charges of other pixels in the imaging array.

Since the switch transistor is eliminated from the pixel, the gate and drain potentials of the readout transistor are used to control the access of pixels on the output bus. For example, in order to turn off a pixel, the gate and/or drain potentials of the readout transistor are set to ground potential. In order to achieve this, the transfer transistor is turned off and FD node is set to ground potential via reset transistor, i.e. the drain of the reset transistor is set to ground potential ($V_{rL}$). Turning off the transfer

transistor shields the FD node from the photodiode and the collection of photo charges on the photodiode is not compromised as the FD node potential is set to ground potential. The drain of the readout transistor is set to ground potential via the row parallel multiplexer. In order to access a pixel, the potential at the FD node has to be at least one threshold above ground and the potential at the drain node of the readout transistor has to be above ground. A current conveyor is used to set the drain potential of the readout transistor to 0.2V.

All pixels in the imaging array are readout in series and the timing diagram is presented in Figure 3.2. A current-to-voltage converter and an analog-to-digital converter, which are implemented off-chip, are used to convert the output current to a voltage and digitize the result respectively. The addressing of the imaging array is performed as follows. First, the FD nodes in the first column of pixels are preset to $V_{rH}$ potential and the FD nodes of all other pixels in the array are set to ground potential. This is achieved by setting the potential on the reset bus of the first column to $V_{rH}$, while the potentials on the rest of the column reset buses are set to $V_{rL}$ potential. The gates of all reset transistors in the imaging array are pulsed and the presetting of the FD nodes is completed.
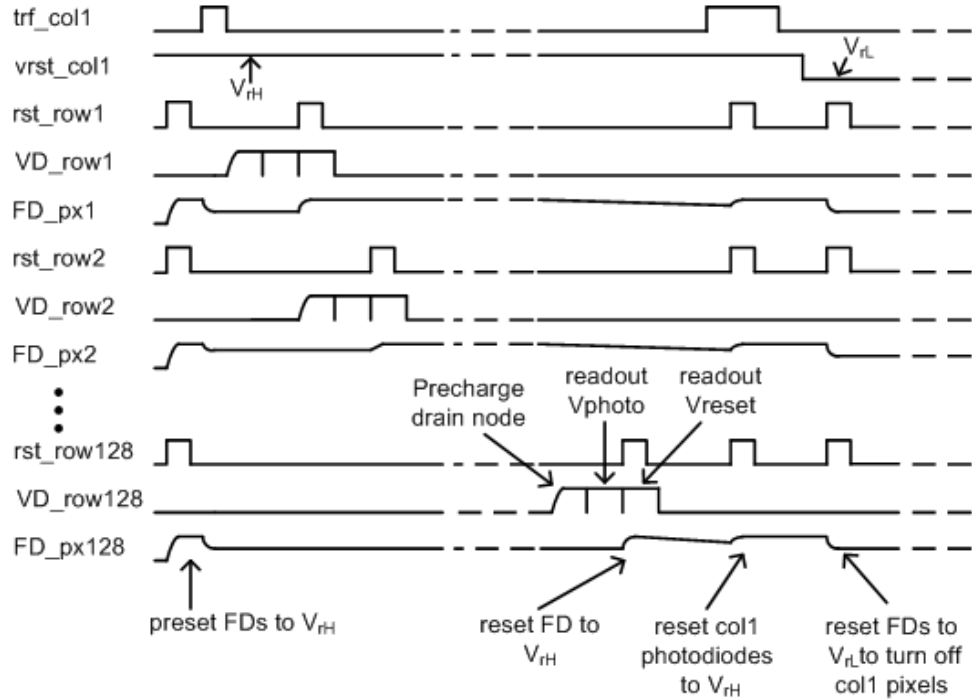
Figure 3.2.  Timing diagram of imaging sensor readout state machine.

The drain line of the first row of pixels is connected to a current conveyor via a row parallel analog multiplexer and the integrated current of the first pixel is readout. Next, reset transistors of all pixels in the first row are turned on and reset current from the first pixel is readout. The FD nodes for the rest of the pixels in the first row are set to ground potential and these pixels do not contribute to the final output current. While the reset current from the first row is readout, the drain potential of the second row is pre-charged to 0.2V in order to speed up the access time of the next pixel. The second pixel in the first column is addressed next and its integrated current is readout by the current conveyor. The rest of the pixels in the first column are accessed in the same manner as described for the first two pixels in the column.

After the last pixel in the first column has been accessed, both reset and transfer transistors are turned on and all pixels in the first column are reset to $V_{rH}$ potential. The transfer transistors are turned off next and the pixels in the first column start to integrate

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the photo-generated charges. The drain potential on the reset transistors are set to $V_{rL}$ potential and the FD nodes are set to ground potential accordingly. Hence, the gates of the readout transistors in the pixels of the first column are below the threshold potential and all pixels in the first column are turned off. The second column of pixels is activated next and its pixels are readout in the same manner as the pixels in the first column.

## 3.2.3  Analog Processing Unit

The analog processing unit, located at the periphery of the imaging array, facilitates on-chip computation and image processing. The analog processing unit is composed of two identical computational blocks, whose output currents flow into a common bus, i.e. common node, which can be accessed off-chip. Due to Kirchhoff current law, the currents from the two independent computational blocks are added together to generate a final output current. Schematic of one of the computational blocks is presented in Figure 3.3.
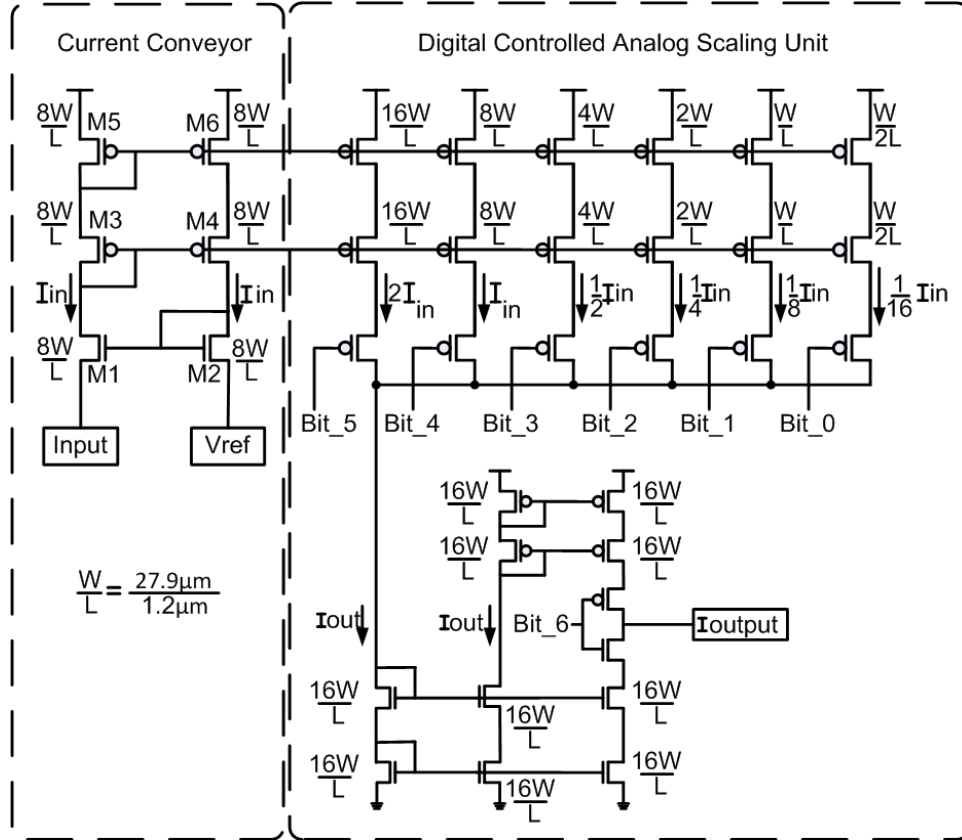
Figure 3.3. Schematic diagram of the digitally controlled analog scaling computational block.

The analog computational block has two components: a current conveyor and a digitally programmable scaling unit. The drain bus of the readout transistor is connected to the current conveyor via an analog multiplexer. The purpose of the current conveyor is to set the drain potential of the pixel's readout transistor to a reference potential and copy the current that flows through the readout transistor to an output branch.

The current conveyor operates as follows. All transistors in the current conveyor have the same aspect ratio and operate in the saturation region. The p-channel transistors $M_3$ through $M_6$ form a cascode current mirror since transistors $M_3$ and $M_5$ are diode connected and the gates of transistors $M_3$ and $M_5$ are connected to the gates of transistors $M_4$ and $M_6$ respectively. The current mirror formed by the four p-channel transistors

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requires that an equal current should flow through both branches of the current conveyor. Hence, the currents that flow through transistors $M_1$ and $M_2$ are equal. Since transistor $M_2$ is diode connected and its gate is connected to the gate of transistor $M_1$, the two n-channel transistors form a current mirror. Hence, the potential at the source terminal of transistor $M_1$ will be the same as the reference potential, $V_{ref}$, applied at the source of transistor $M_2$. The cascode p-channel current mirror mitigates the channel length modulation effects and helps to improve the current coping properties of the current conveyor.

The input current of the current conveyor is mirrored six times in the digitally controlled analog scaling unit. The aspect ratios of the transistors in the output branches are scaled logarithmically, as shown in Figure 3.3. The six scaled currents are summed together via the access switch transistors, whose gates are controlled by a digital register. The scaled current is passed through positive/negative selection circuitry which selects the directionality flow of the output current. The final output current from the processing unit is a signed magnitude scaled current which is controlled by a 7-bit digital register and it is described by equation (3.2).

$$I_{out} = (-1)^j * I_{in} \sum_{i=0}^{5} 2^{(i-4)} \qquad (3.2)$$

In equation (3.2), j is the value of the seventh bit (Bit_6) in the digital register i.e. the sign bit of the register. For example, if the seventh bit is one, the output current will be negative, i.e. it will sink to ground from the output node. If the seventh bit is zero, the output current is positive and it will be sourced from $V_{dd}$.

The two computational blocks in the analog processing unit are programmed independently, and their output currents flow into a common bus that can be accessed off-chip. These two blocks receive two different currents from the imaging array via the 4:1 analog multiplexer, scale these currents via the 7-bit digitally programmable analog

scaling unit and add their final currents together in order to provide a processed image. Expanding the analog multiplexer in order to handle larger number of input currents will allow for more currents to be selected from the imaging array and more complex image processing filters to be computed on-chip. The current mode domain imaging and image processing can compute addition of different pixels in the same row for free by simply turning on multiple pixels to access the readout bus. The architecture presented in this chapter, allows for implementation of one and two dimensional convolution kernels with two different coefficients in the filter.

This architecture can be extended to compute one and two dimensional kernels with N different coefficients by implementing (N+2):1 column parallel analog multiplexer at the periphery of the imaging array and extending the analog processing unit to contain N computational blocks.

The transistor matching in the current mirrors of the N computational blocks will be critical in order to achieve a 7-bit precision in the image processing computation. In order to maintain high computational precision, calibration schemes have to be incorporated in each computational block (i.e. current mirrors) such that matching between transistors is maintained. Calibration techniques have been employed in current-steering DACs, where digital [67] or self calibrating circuits [68] are used to reduce the mismatching between transistors to less than 0.1% across the entire chip. These calibration techniques will have to be incorporated as part of the computational blocks in future realization of the imaging chip in order to realize larger computational kernel with 7-bit precision.

More elaborate kernels, such as Gabor filter with N coefficients, may require on-chip or off-chip memory to temporarily save filtered pixel information that is needed for computation at a later stage. For such implementation, as the imaging array is scanned, a region of pixels is convolved with several smaller kernels with different coefficients and

the results are temporary stored in memory. The final kernel composed of N coefficients is assembled from the temporary stored information of the smaller size kernels. This is a common technique implemented in FPGA in order to realize high resolution kernels in real-time [69] and can be implemented with my imaging sensor with the addition of memory.

# 3.3    Experiments and Results

A prototype of the imaging sensor was fabricated in 0.6µm 3M2P CMOS process via MOSIS educational program [70]. The micrograph of the image sensor die is shown in Figure 3.4.
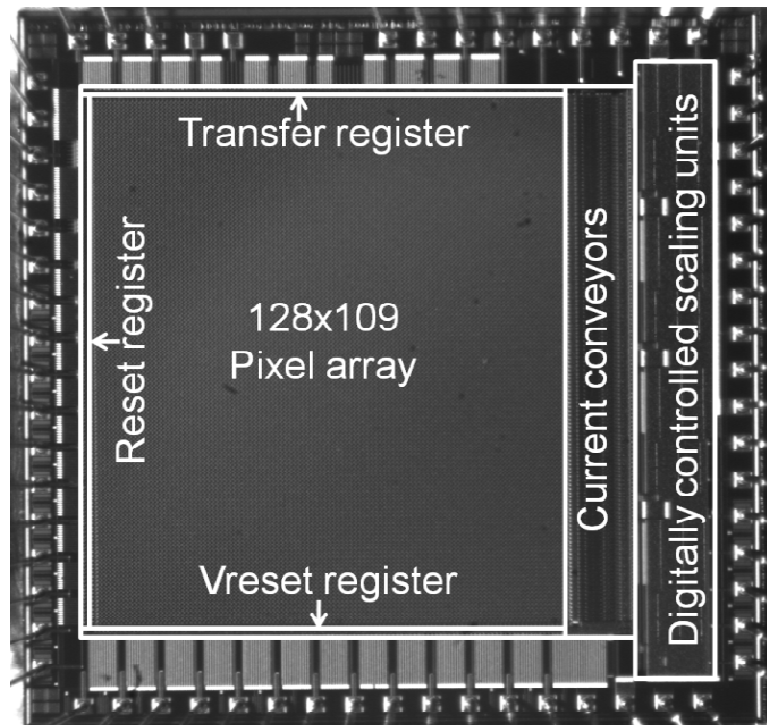


Figure 3.4.  Micrograph of the image sensor.

The prototype is used to demonstrate the feasibility of the imaging sensor and on-chip image processing paradigms. The electro-optical characteristics of the imaging

sensor are carefully evaluated and presented next.

## 3.3.1  Photo Response and Linearity of a Pixel

The imaging sensor is evaluated with a uniform light intensity at 515nm±15nm using a narrowband LED coupled with a 2" integrating sphere. The light intensity of the LED is controlled from the PC via a GPIB programmable power supply. The photo response from a single pixel as a function of both light intensity and integration time is evaluated and presented in Figure 3.5. The pixel's photodiode is first reset to 3V and after 2 ms the integration of photo generated charges is initiated. The duration of the integration cycle is 13 ms. The output photo current is sampled at every 10µs and a total of 1500 samples are obtained during the reset and integration cycle. The pixel's output current is recorded for light intensities between $0.01\mu W/cm^2$ to $5\mu W/cm^2$ and 1024 reset-integration cycles are obtained for all light intensities. An average photo response of the pixel over time is computed and presented in Figure 3.5. The average response minimizes variations due to thermal and shot noise in the sensor.
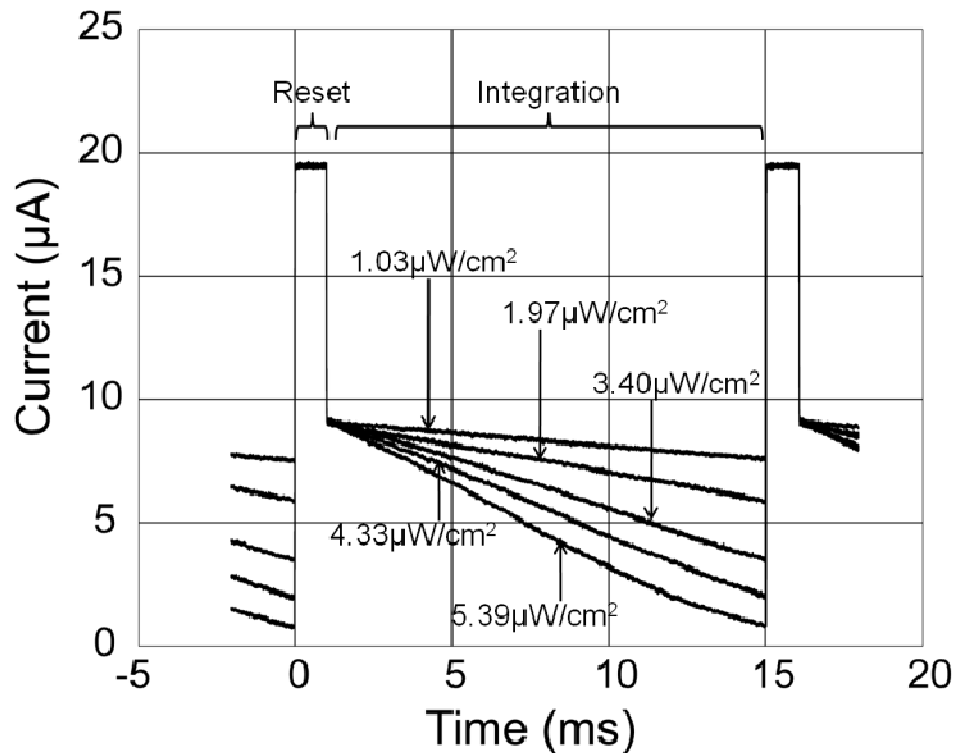
Figure 3.5. The output current from a single pixel as a function of time and light intensity. The pixel reset period is 2 msec and integration time is complete at 15 msec.

During the reset period, the photodiode is reset to 3V and pixel's output current is ~19.5μA. When the reset period is completed, the reset transistor in the pixel is turned off. The output current abruptly drops by ~10μA due to the charge injection charges from the channel in the reset transistor and from the clock coupling via gate-to-source overlap capacitance in the reset transistor. For minimum sized reset and transfer transistors, the charge injection charges are estimated to be ~10 nC.

From Figure 3.5, we can observe that the linearity of the output current is maintained for the entire integration period (~13 ms) and for light intensities between $0.01 \mu W/cm^2$ to $5 \mu W/cm^2$. The linearity of the pixel's output current is computed as the root mean square value of the residuals normalized to the output current and is 99.1% for light intensities up to $4 \mu W/cm^2$. The photodiode node potential is estimated to discharge

from 3V down to ~1.4V for light intensity of 4μW/cm$^2$ and integration time of 13ms. The linearity of the output drops to 98.2% when the pixel is illuminated with light intensity of 5μW/cm$^2$ and integration time of 13ms. For this light intensity, the photodiode node potential is estimated to be around 0.9V and the readout transistor of the pixel enters sub-threshold value at the end of the integration cycle. Hence, the non-linearity of the output current is increased as the readout transistor enters sub-threshold mode of operation.

## 3.3.2  Photo Response Variations across the Imaging Array

The average and standard deviation of photo response from all pixels in the imaging array are recorded and presented in Figure 3.6.
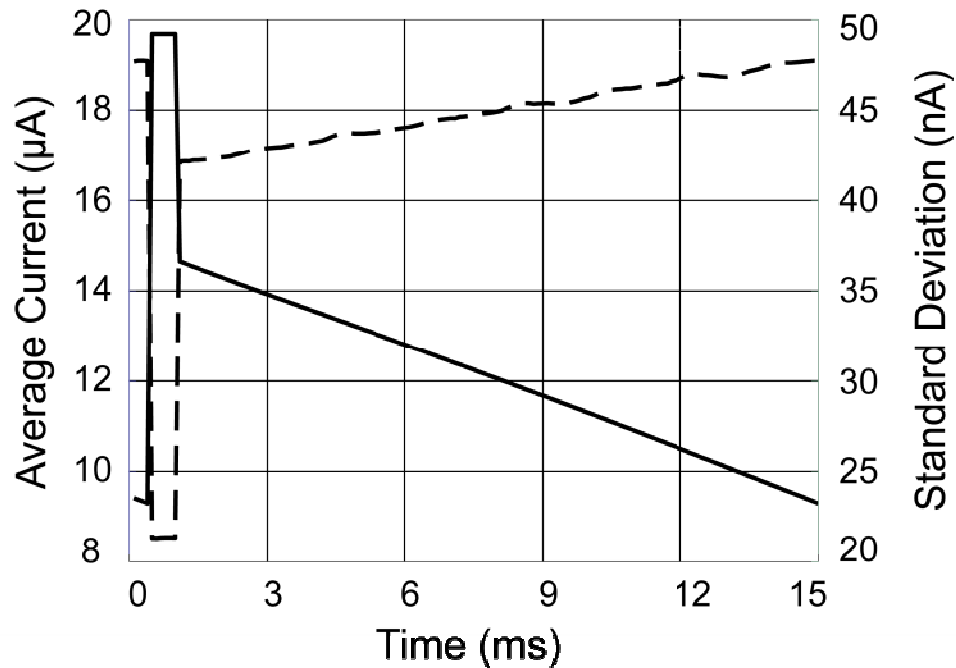


Figure 3.6.  Average and standard deviation of photo response.

For this experiment, initially the FD and photodiode nodes for all pixels are set to

ground potential. Next, the pixel of interest is reset and then integrates photo generated charges for 13ms. A total of 1024 reset-integration cycles per pixel are recorded and averaged for every pixel. Hence the temporal variations due to the thermal noise of the pixel and readout circuitry are reduced and spatial variations between pixels in the imager are evaluated.

The standard deviation is 0.1% during the reset phase and it increases with the integration period. During the reset period, the FD node and the photodiode potentials are set to 3V. Mismatches between the readout transistors are the main cause for the variations between the reset currents in the imaging array. During the integration period, the photodiode mismatches also contribute to the increased variation between the pixels' output currents across the imaging array.

## 3.3.3  Fixed Pattern Noise and Signal-to-Noise Ratio Measurements

Spatial and temporal noise performances are evaluated using the same optical set-up as described in the previous subsection. The integration period for the imaging sensor is set to 20 ms and a total of 10K frames are collected for every light intensity level between $0.01\mu W/cm^2$ to $5\mu W/cm^2$. The signal-to-noise ratio (SNR) and fixed pattern noise (FPN) measurements are presented in Figure 3.7 and Figure 3.8 respectively.

SNR for the imaging sensor is computed as the average SNR of all pixels in the array. SNR of a single pixel is computed as a ratio of the average current output signal over the standard deviations of the current output signal across all 10K frames. As for the FPN of the imaging sensor, first an average image is computed by taking the mean of current output values for every pixel across the 10K frames to eliminate temporal fluctuations. The final FPN is computed as the ratio of the standard variations across all pixels in the averaged image normalized to the saturated pixel's output current.

Difference double sampling (DDS) operation is computed off-chip in order to improve the FPN performance [36].
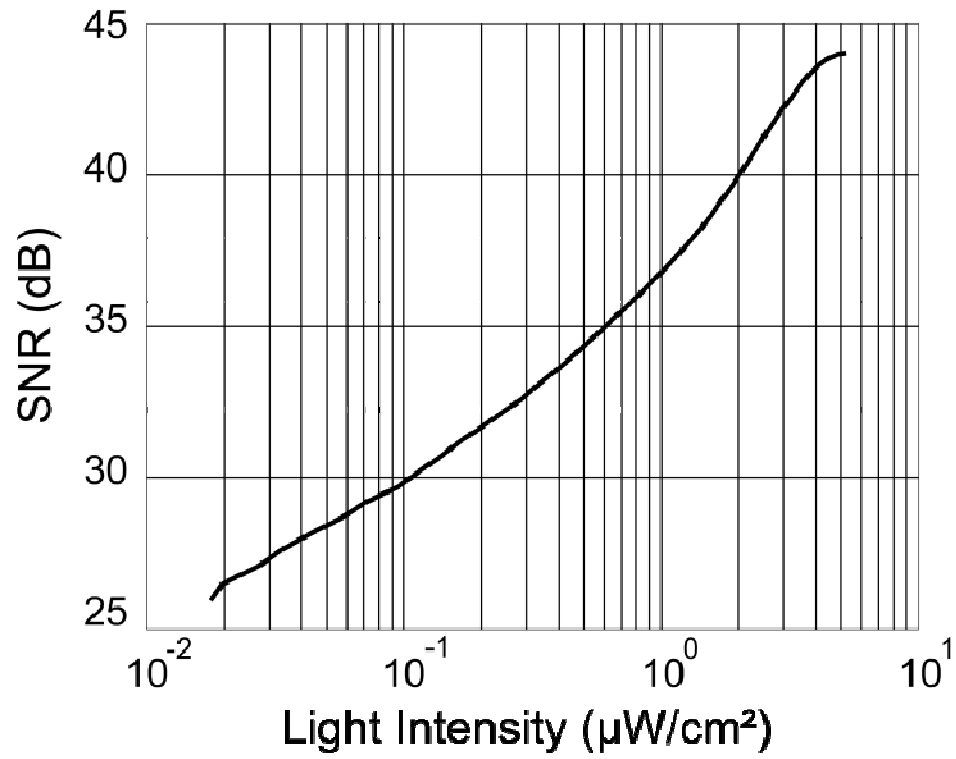


Figure 3.7. Measured SNR as a function of light intensity.
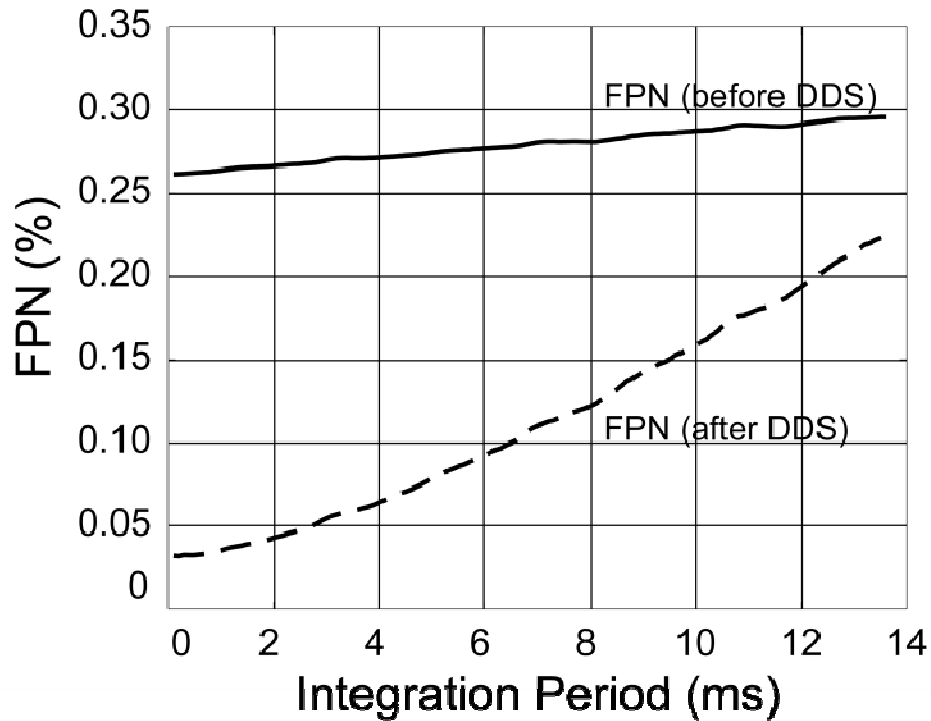
Figure 3.8. Measured FPN before and after DDS as a function of integration time.

Temporal noise is dominated by thermal noise of the readout transistor and current conveyor circuitry for light intensities below $0.01\mu W/cm^2$ and integration period of 20ms. On the other hand, shot noise is the dominant source of temporal noise for light intensities brighter than $0.01\mu W/cm^2$ and integration period of 20ms. The elimination of the switch transistor reduces the temporal noise of the imaging sensor and increases the SNR [36].

Spatial variations which are manifested in the FPN increase with light intensity in the imaging sensor. This is due to the fact that as light intensity increases, the gate voltage at the read-out transistor decreases and the read-out current decreases as well. Variations between pixels, which are due to aspect ratio variations, threshold voltage variations and mobility variations among others, as a percentage of the mean pixel current are increased when the pixel currents are small. The FPN without DDS operation

is around 0.25% and independent of light intensity. Implementation of DDS improves spatial noise performance to FPN measurements lower than 0.22%.

## 3.3.4  Analog Signal Processing Linearity

Measurements of three processed output currents from three different pixels with different reset voltages are presented in Figure 3.9. Residuals from linear fits of the processed output currents are presented in Figure 3.10.
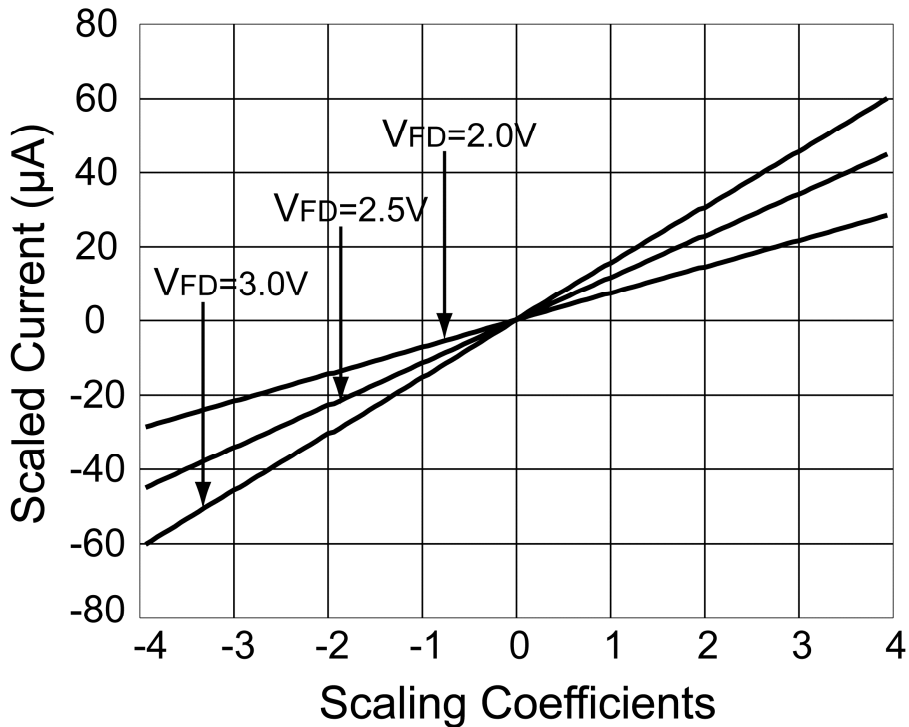


Figure 3.9.  Processed output currents for three pixel intensity values.
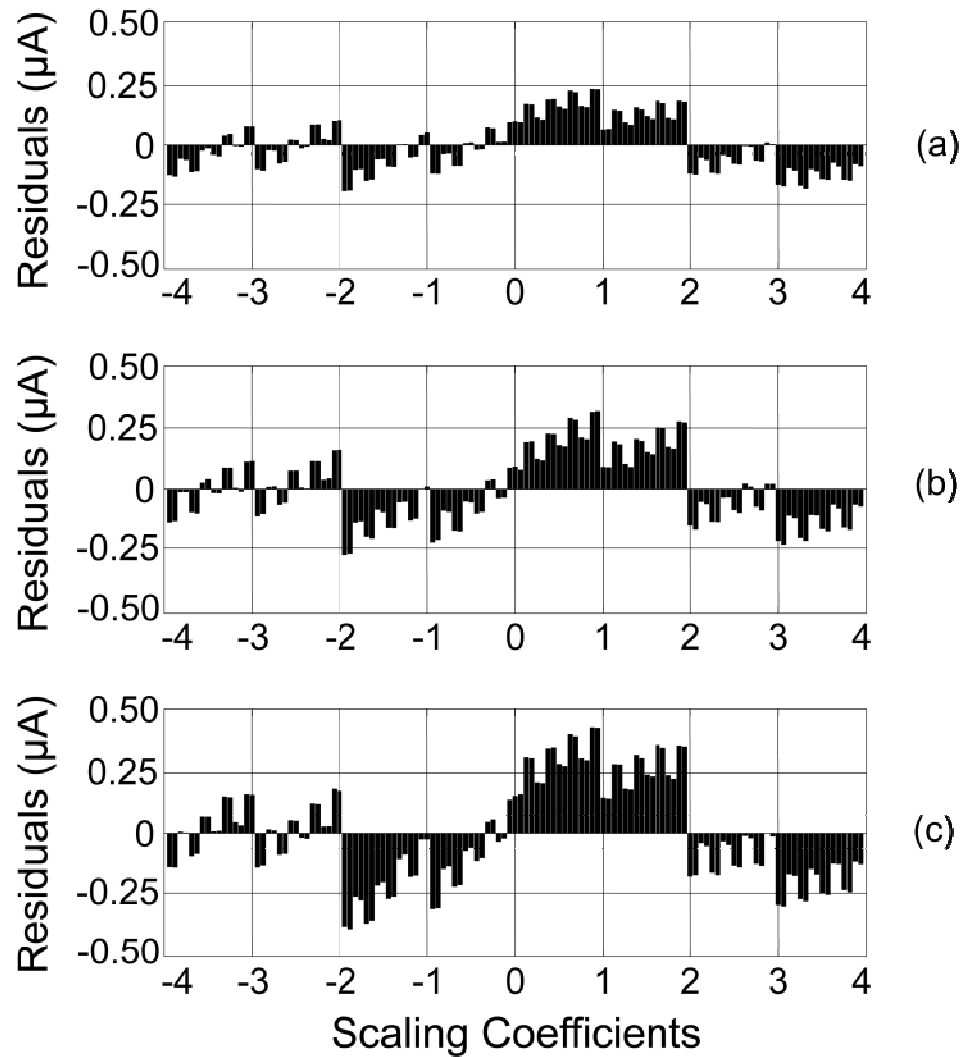
Figure 3.10. Residuals from linear fits of the processed output currents from pixels with
(a) $V_{FD}$=2.0V, (b) $V_{FD}$ =2.5V, and (c) $V_{FD}$ =3.0V.

For this experiment, the shutter of the image sensor is closed to prevent photo
charge from being integrated at the photodiode node. Three pixels are selected and their
photodiodes are continuously reset to 2.0V, 2.5V, and 3.0V respectively to ensure
constant readout output currents. The output currents are steered to a computational block
and individually scaled with each of the 128 possible signed magnitude scaling
coefficients.

The raw pixel output currents corresponding to the three photodiode potentials of 2.0V, 2.5V, and 3.0V are 7.40µA, 11.60µA, and 15.54µA respectively. The residuals from the linear fits of the scaled output currents are presented in Figure 3.10. The RMS values of the residuals for the three pixels are 0.11µA, 0.14µA, and 0.20µA respectively. The range values of output currents for the three pixels are 57.01µA, 89.93µA, and 120.29µA respectively. Non-linearity of each graph is computed as a ratio of the RMS of residuals to current range recorded for the pixel output current. Non-linearity measurements of the three scaled output currents are 0.19%, 0.16%, and 0.17% respectively. The non-linearity of the graphs is due to mismatches of transistors in the processing unit that occurred during the fabrication process.

# 3.3.5  Sample Images and Focal Plane Convolution

Samples of intensity and processed images of a couple of targets obtained using the fabricated imaging sensor are presented in Figure 3.11 and Figure 3.12.



(a)                    (b)                    (c)
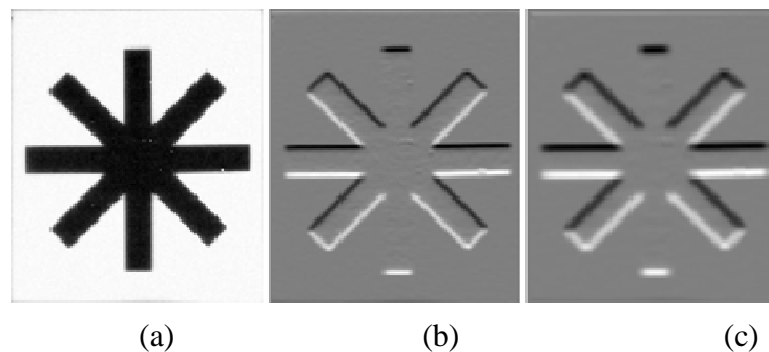
Figure 3.11.  Intensity image (a), 3 x 3 convolved image (b), and 5-by-5 convolved image (c).

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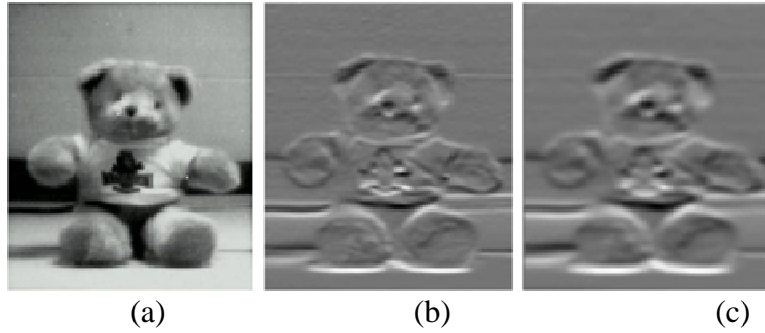
Figure 3.12. Intensity image (a), 3 x3 convolved image (b), and 5-by-5 convolved image (c).

In both Figure 3.11 and Figure 3.12, image (a) is the DDS corrected image, image (b) is the convolved image with 3-by-3 convolution filter, and image (c) is the convolved with 5-by-5 convolution filter. The convolved images are obtained by programming the analog scaling unit with the appropriate kernel coefficients and are obtained in parallel with the intensity image. The 3-by-3 and 5-by-5 convolution filters that were implemented to detect horizontal edges are presented in Figure 3.13. The choice of coefficients in the kernel window is such that the convolution kernel allows for good detection of edges, good localization of the edges and minimum response to edges in the image. Theoretical details for selecting coefficients for edge detection kernels are described in [71, 72].



| -1 | -1 | -1 |
|----|----|----|
| 0  | 0  | 0  |
| +1 | +1 | +1 |

(a)

| -1 | -1 | -1 | -1 | -1 |
|----|----|----|----|----|
| -1 | -1 | -1 | -1 | -1 |
| 0  | 0  | 0  | 0  | 0  |
| +1 | +1 | +1 | +1 | +1 |
| +1 | +1 | +1 | +1 | +1 |

(b)

Figure 3.13.  3-by-3 convolution filter (a), 5-by-5 convolution filter (b).

The DDS corrected intensity image exhibits low spatial variations across the imaging array due to low FPN. In the convolved images, horizontal edges are highlighted with bright and dark intensity values that represent positive and negative edges respectively. The convolution kernels filter the intensity image with a first derivative function along the vertical direction. Pixels of adjacent rows with different intensities produce positive or negative derivative values, therefore highlight horizontal edges. On the other hand, pixels of adjacent rows with equal light intensities produce zero derivatives, therefore, assume an average gray color. Diagonal edges are also highlighted because they contain both horizontal and vertical components. However, their resultant intensities are less significant than those of horizontal edges. The 5-by-5 convolved images are smoother than 3-by-3 convolved images, because the intensity value assigned to each pixel in a 5-by-5 convolved image is based on the intensity of a larger pixel neighborhood than that of a 3-by-3 convolved image.

The precision of the horizontal edge filters is evaluated with a calibrated gray scale target presented in Figure 3.14. The calibrated target contains four shades of gray: 10%, 60%, 90%, and 100%. Figure 3.14-a presents the intensity image recorded by the imaging sensor. The horizontal edge computed image is presented in Figure 3.14-b. The different intensities of the horizontal edges correspond to the difference between two neighboring gray scale regions. A single line inset through the cross-section of the edge-detected image is presented in Figure 3.14-c.

A filter implemented as a first derivative function operating along the vertical direction computes difference of currents from adjacent pixels to generate a horizontal edge-detected image. A region on the intensity image with the same gray shade produces a spatial derivative of zero, which corresponds to a non-edge in the edge-detected image. A transition between two neighboring gray scale regions with different shades of gray

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produces a non-zero spatial derivative that is proportional to the difference of the two shades. The non-zero spatial derivative may be associated with either a positive or a negative edge depending on the direction of the derivative function. A positive edge is represented by a positive spatial derivative on the cross-section graph and by a bright edge on the edge-detected image. On the other hand, a negative edge is represented by a negative spatial derivative on the cross-section graph and by a dark edge on the edge-detected image.
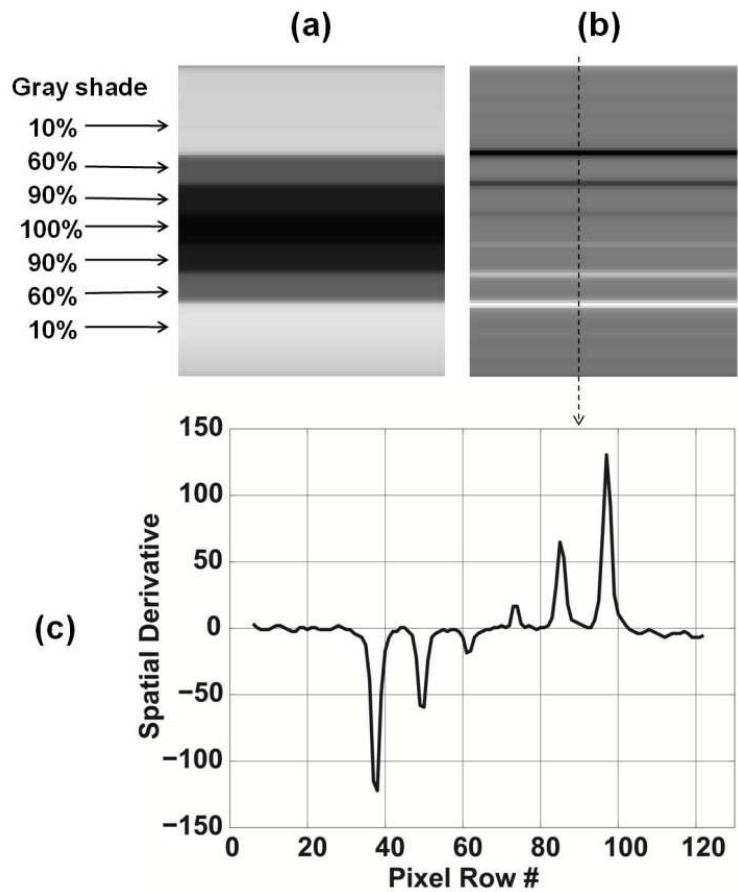


Figure 3.14.  Intensity image (a), edge-detected image (b), and cross-section of edge-detected image (c).

# 3.3.6 Power Consumption

Simulation results of the analog and digital power consumption as function of frame rate are presented in Figure 3.15. The simulation results are based on the final extracted view of the complete imaging chip. The five digital scanning registers for the imaging array contribute to the total digital power consumption (see Figure 3.1). The analog processing unit, which is composed of current conveyors and current mirrors (see Figure 3.3), together with input current from 5 by 5 pixel neighborhood contribute to the total analog power consumption. The analog processing unit performs horizontal edge detection on a neighborhood of 5 by 5 pixels.

The analog power consumption remains relatively constant at 17.06mW for different frame rates. On the other hand, digital power consumption is proportional to the frame rate (i.e. operational frequency of the imaging array) and follows the $CV^2f$ model. When the imaging sensor operates at 50 frames per second, 17.06mW and 30mW of power are consumed due to analog and digital circuitry respectively. At 350 frames per second, the digital power consumption increases to 92mW.
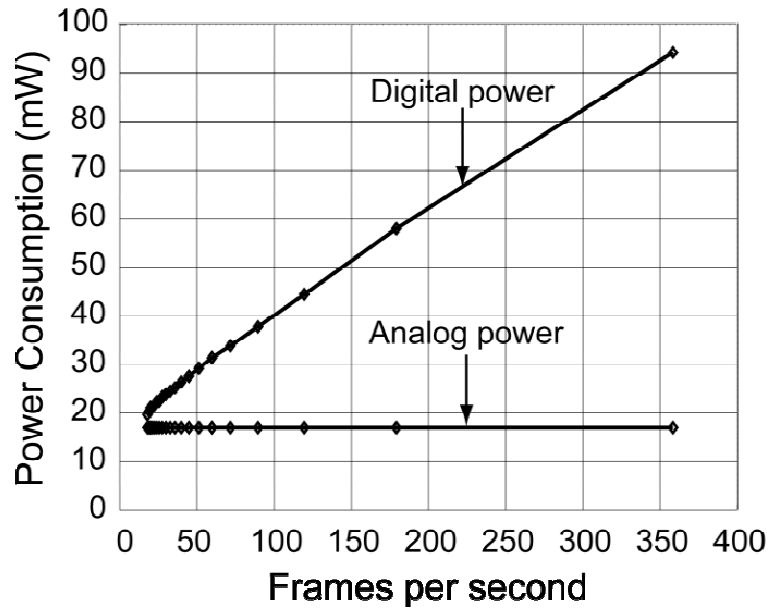
Figure 3.15. Simulated power consumption as a function of frame rate.

# 3.4 Conclusion

In this chapter, I investigated whether we can monolithically combine current mode imaging elements with current mode analog computational circuitry to perform image processing at the focal plane of an imaging sensor. I presented a programmable current mode computational imaging sensor that was implemented in 0.6µm 3M2P CMOS process. The imaging sensor is based on switchless linear current mode APS paradigm and allows for low spatial and low temporal noise imaging, leading to lower FPN and higher SNR compared to previously published sensors.

Compared to the imaging sensor presented in [44], the sensor presented in this chapter has two major improvements. The first improvement is in the pixel size and fill factor. In the imaging sensor presented in this chapter, the pixel design is based on the switchless paradigm, where one of the switch transistors is eliminated from the pixel.

This has the advantage of achieving smaller pixel pitch and higher fill factor. The pixel pitch of my sensor is 10µm with fill factor of 30% in 0.6µm CMOS technology compared to the imaging sensor in [44] which has pixel pitch of 30µm with fill factor of 20% in 1.5µm CMOS technology. The second improvement is related to spatial and temporal noise performance of the sensor. The elimination of the switch transistor increases the linearity of the pixel output current and decreases spatial and temporal noise in the imaging sensor [36]. The improved linearity of the pixel output current allows for implementation of difference double sampling technique which helps in reducing the spatial noise variations across the imaging array. Therefore, the maximum SNR and FPN (after DDS) for my imaging sensor is 44dB and 0.22% respectively compared to 38dB and 2.5% respectively for the one presented in reference [44].

The imaging sensor presented in this chapter performs image processing at the focal plane via low power analog circuits. The digitally programmable scaling unit computes one and two dimensional kernels with two distinct coefficients per convolution window. Noise-corrected intensity image and convolved image were processed at a frame rate of 50 fps with 50 mW of power consumption. Performance comparison of the image sensor with other computational CMOS imagers is summarized in Table 3.1.

# Chapter 4

# Fabrication and Performance Evaluation of Pixelated Nanowire Polarization Filters

## 4.1    Background

Light is a transverse wave that is fully characterized by the intensity, wavelength and polarization of the wave [9]. Transverse waves vibrate in a plane perpendicular to their direction of propagation. For example in Figure 4.1, the transverse wave propagates perpendicular to this page and the vibrations on the X-Y plane are plotted on the graph.

Depending on the direction of the vibrations described on the X-Y plane, a transverse wave can be linearly polarized, partially linearly polarized, circularly polarized or unpolarized. For instance, if the vibrations of the wave are consistent in a particular direction, the electromagnetic wave, i.e. the light wave, is linearly polarized. If the vibrations of the wave are predominant in a particular direction and vibrations in other directions are present as well, the light wave is partially linearly polarized. Circularly polarized light describes circular vibrations in the X-Y plane due to the $+/-\pi/2$ phase difference between the two orthogonal components of the electric-field vector. Unpolarized light vibrates randomly in the plane of propagation and does not form any particular shape on the X-Y plane. In Figure 4.1, linearly polarized light describes a line, partially polarized light describes an ellipse, and circularly polarized light describes a circle on the X-Y plane.
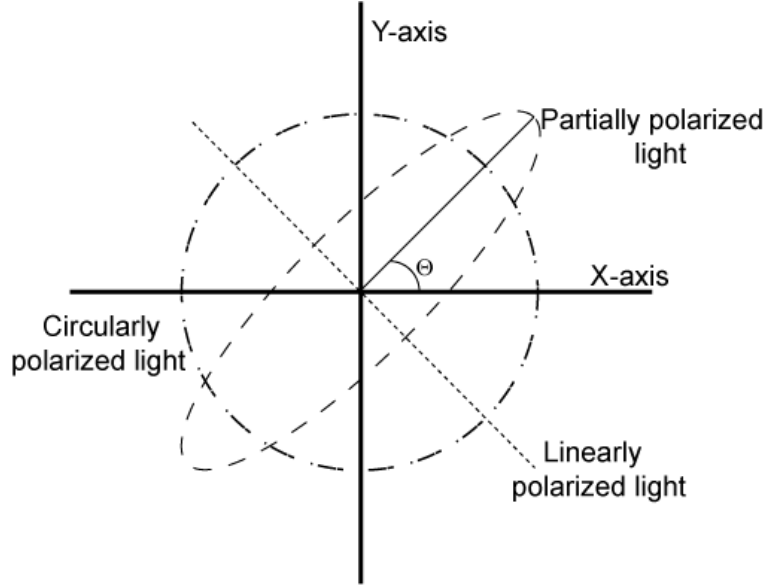
Figure 4.1. Light can be linearly polarized, partially linearly polarized, circularly polarized or unpolarized.

In order to capture the polarization properties of light, two parameters are of importance: the angle of polarization (AoP) and the degree of linear polarization (DoLP). There are different ways of computing DoLP and AoP of the electric-field vector, one of which is presented by equations (4.1) and (4.2).

$$\text{DoLP}=\sqrt{S_1^2 + S_2^2} \,/\, S_0 \tag{4.1}$$

$$\text{AoP}=1/2*\arctan\left(S_2/S_1\right) \tag{4.2}$$

In equations (4.1) and (4.2), $S_0$, $S_1$ and $S_2$ are known as the Stokes parameters and are defined by equations (4.3) through (4.5):

$$S_0 = I(0^\circ) + I(90^\circ) \tag{4.3}$$

$$S_1 = I(0^\circ) - I(90^\circ) \tag{4.4}$$

$$S_2 = I(45^\circ) - I(135^\circ) \tag{4.5}$$

In equations (4.3) through (4.5), $I(0^o)$ is the intensity of the e-vector filtered with a 0 degree linear polarization filter and no phase retardation; $I(45^o)$ is the intensity of the e-vector filtered with a 45 degree linear polarization filter and no phase retardation; and so on. In order to compute the three Stokes parameters, the incoming light wave must be filtered with four linear polarization filters offset by $45^o$. Hence, an imaging sensor capable of characterizing optical properties of polarized light has to employ four linear polarization filters offset by $45^o$ together with an array of imaging elements.

In this chapter, I present nano-scale and pixelated aluminum nanowire polarization filters fabricated using electron beam lithography (EBL) and reactive ion etching (RIE) methods. I am going to evaluate the influence of pitch and orientation on the performance of the pixelated nanowire polarization filters. The rest of the chapter is organized as follows. Section 4.2 describes overview of current state-of-the-art polarization imaging sensors. Section 4.3 describes overview of nanowire polarization filters. Section 4.4 describes methods utilized to fabricate the polarization filters. Section 4.5 presents performance measurements of the filters. Section 4.6 presents concluding remarks.

# 4.2    Overview of Current State-of-the-art Polarization Imaging Sensors

The current state-of-the-art polarization imaging sensors can be divided into division of time [73, 74], division of amplitude [75, 76], division of aperture [77, 78] and division of focal plane polarimeters [60]. One of the first approaches toward polarization imaging included standard CMOS or CCD imaging sensors coupled with electrically or mechanically controlled polarization filters and a processing unit  [73, 79]. These imaging systems, known as division of time polarimeters, sample the imaged environment with a minimum of three polarization filters offset by either 45 or 60 degrees and polarization information, i.e. degree and angle of linear polarization, is

computed off-chip by a processing unit. Shortcomings of these systems are reduction of frame rate by factor of 3, high power consumption associated with both the processing unit and the electronically/mechanically controllable polarization filters, and polarization information errors due to motion in the scene during the sampling of the three polarization filtered images.

Division of focal plane (DoFP) polarimeters include imaging and micropolarization filters on the same substrate [60, 61, 80-82]. The sampling of the imaged environment is achieved with spatially distributed micropolarization filters over a neighborhood of pixels. Incorporating pixel-pitch-matched polarization filters at the focal plane has been explored with birefringent materials [60, 61] and thin film polarizers [60, 80-83]. The pixel pitch of the birefringent and thin film micropolarizer arrays were reported to be 128 μm [61] and 50 μm [60], respectively. The large pixel pitch of these sensors has limited their use for real-time polarization imaging applications due to the low spatial resolution.

The low resolution problems of DoFP polarimeters are addressed by: 1) monolithically integrating CMOS imaging sensor with polymer polarization filters [82-88] and 2) integrating CCD imaging sensors with aluminum nanowires polarization filters [89-96]. The polymer polarization imaging sensor is composed of a 60 by 20 pixel array with 18 µm pixel-pitch, low noise current mode pixels and focal plane analog processing for real-time computation of polarimetric parameters [83]. The array of polymer polarization filters is designed via an optimized microfabrication procedure and is deposit directly on the surface of the CMOS imaging sensor in order to design a compact and robust polarization sensor. This imaging sensor is the first DoFP polarimeter for the visible spectrum published in the literature capable of sensing the first three Stokes parameters in real-time and is used for automatic detection and classification of five flat surfaces based on the computed indices of refraction from the sensed polarization information.

The first high resolution polarization CCD imaging sensor is reported in [90]. The polarization sensor reported in [90] monolithically integrates aluminum nanowires polarization filters with an array of 1 Mega pixels CCD imaging elements. Each pixel consists of a photodiode with a well capacity of 20K electrons and two light shielded buried channel CCDs. The read-out noise of the CCD imaging sensor is 16 e$^-$ and has conversion gain of 30 $\mu$V/e$^-$. The custom CCD imaging sensor is optimized for low noise read-out and fabricated it in 180 nm image specific process. An array of pixel-pitch matched aluminum nanowire polarization filters covers the CCD array of photo elements. The pixelated polarization filter array is composed of four distinct filters offset by 45$^o$. The aluminum nanowires in each individual filter of the micropolarization array are 70 nm wide, 70 nm high and have a pitch of 140 nm. This unique polarization imaging sensor has a signal-to-noise ratio of 45dB and captures intensity, angle and degree of linear polarization in the visible spectrum at 40 frames per second with total power consumption of 5W for the entire imaging system.

Although this is the first high resolution division of focal plane polarization imaging sensor for the visible spectrum reported in the literature, there are two shortcomings with this sensor. First, the extinction ratios of the polarization filters are low due to the size of the metallic nanowires that constitute the optical filters. The size of the metallic nanowires is inversely proportional to the extinction ratio performance of the filter. Low extinction ratios can limit the sensitivity of the camera to polarization information and it is desirable that the extinction ratios are as high as possible i.e. the size of the nanowires in the optical filters to be as small as possible. Second, the high power consumption associated with the CCD sensor increases the operational temperature of the camera to 45$^o$C (or 113$^o$F). The elevated operational temperature of the CCD sensor increases the thermal noise of the sensor and the signal to noise ratio of the sensor is degraded. Hence, the quality of the acquired polarization information is compromised due to these two limiting factors and I plan to address them in this dissertation.

# 4.3    Overview of Nanowire Polarization Filters

Nanowire polarization filter is a grid of periodic and parallel metallic wires that transmits parallel polarized light and reflects cross polarized light as shown in Figure 4.2. An array of such filters oriented at 0, 45, 90, and 135 degrees may be integrated onto an image sensor to capture polarization information of the imaged environment [91]. Performance of nanowire polarization filters is influenced by the following parameters: period, width, height, and grating material [97]. A rule of thumb for the period of wire gratings is that the shortest operating wavelength that can be effectively filtered is approximately three times the period of wire gratings. Furthermore, thin and tall nanowires effectively block cross polarized light. Aluminum is a preferred choice for fabricating nano-structures because it has high conductivity, compatible with most of fabrication techniques, oxidization resistance, and wide operating wavelength.
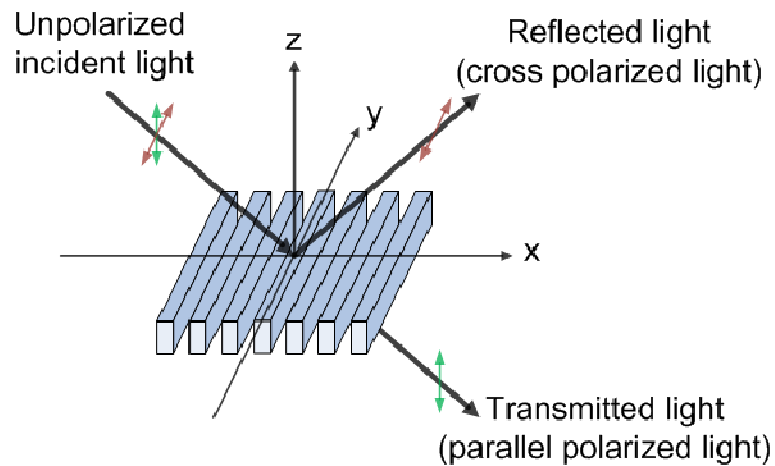


Figure 4.2. Operation of nanowire polarization filter

Various fabrication techniques have been employed to realize nanowire polarization filters. Ultra violet (UV) photolithography uses UV light to transfer a pattern from a predefined mask onto a photo resist material. It is limited to large features, which is mainly due to the effects of diffraction. Interference lithography uses a system of two

beams to produce an interference pattern onto a substrate. The beam setup may be immersed in a liquid to achieve smaller grating period. Nanoimprint lithography involves fabricating a stamp with desired pattern and then repeatedly stamping the pattern onto a substrate [98]. The technique has the advantage of producing low cost and high throughput filters.

**Table 4.1 Reactive Ion Etching Recipe for Etching Aluminum Nanowires**

|  | Step 1 | Step 2 | Step 3 | Step 4 | Step 5 |
|---|---|---|---|---|---|
| Pressure (mTorr) | 50 | 10 | 10 | 10 | 50 |
| RIE (W) | 0 | 150 | 200 | 100 | 0 |
| ICP (W) | 0 | 300 | 300 | 300 | 0 |
| Time (s) | 60 | 5 | 16 | 40 | 30 |
| Gas 1 (scmm) | Ar: 50 | $O_2$: 1 | $CHF_3$: 10 | $BCl_3$: 40 | Ar: 50 |
| Gas 2 (scmm) |  | He: 1 |  | $Cl_2$: 15 |  |
| Comment | Purge the chamber | Remove residues | $SiO_2$ etching | Al etching | Purge the chamber |

Electron beam lithography (EBL) uses a focused beam of electrons to draw patterns on photo resist material. EBL has a benefit of achieving very high resolution features at nano-scale level, and large freedom to customize the shape of the nano-structure. However, it is limited to low throughput due to slow serial writing process.

# 4.4    Methods

The procedure used for fabricating nanowire polarization filters is described in Figure 4.3.
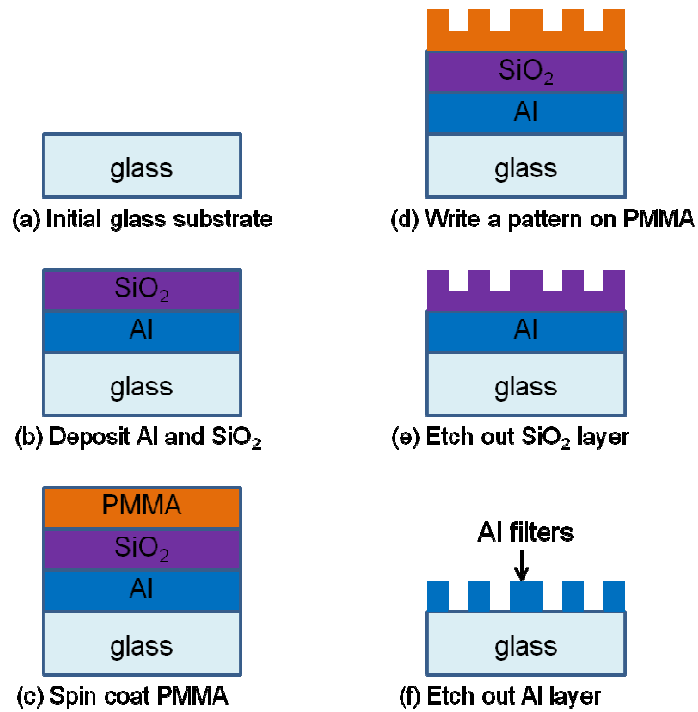
Figure 4.3. Fabrication of nanowire polarization filters

A microscope glass slide is the initial substrate for the nanowire polarization filters. The glass substrate is coated with 100nm Al and 20nm $SiO_2$ via e-beam evaporation and film deposition respectively. A 200nm layer of poly methyl methacrylate (PMMA) photoresist is spin coated on the surface of the sample at 2500rpm for 60s, and post-baked at $180^o$c for 70s. Filter patterns are drawn on the PMMA-coated sample using electron beam lithography (EBL) via a scanning electron microscope (SEM). The sample is developed using methyl isobutyl ketone (MIBK): isopropyl alcohol (IPA) 1:3 solution for 60s, and post-baked at $90^o$C for 70s.

Reactive ion etching (RIE) method is used to transfer the PMMA pattern to the Al film. The RIE method is detailed in Table 4.1. The RIE chamber is set to $70^o$C. In step 1, RIE chamber is purged with Ar gas to remove residual gasses. The sample is inserted into the RIE chamber. In step 2, residuals of PMMA are removed from the sample using $O_2$ and He gasses to ensure smooth surfaces and the $SiO_2$ layer got exposed. In step 3, $SiO_2$

is etched out using $CHF_3$ gas. The patterned PMMA acts as mask for $SiO_2$ etch. In step 4, $AlO_2$ and Al are etched out using $BCl_3$ and $Cl_2$ gasses. The etched $SiO_2$ acts as a hard mask in order to transfer the pattern to Al. Lastly, RIE chamber is purged with Ar gas to remove residual gasses in step 5. The resulting sample consists of Al nanowires on the glass substrate.

# 4.5 Measurements

I have fabricated aluminum nanowire polarization filters on a glass substrate using electron beam lithography and reactive ion etching process. Each filter occupies an area of 7.4μm by 7.4μm, which matches pixel size of the custom CMOS imaging sensor where these filters will be deposited. I fabricated several different pixelated nanowire filters, where the pitch of the aluminum nanowires is varied between 50nm and 500nm. Also I fabricated filters with four different orientations of the nanowires offset by 45 degrees. The duty cycle for the nanowire filters is set to 50% for all filters.

## 4.5.1 Observation of Filters using SEM

Geometry and spacing of the fabricated filters are verified by observing the samples under SEM, as shown in Figure 4.4. The filters are relatively smooth, straight, and have height of 80nm.
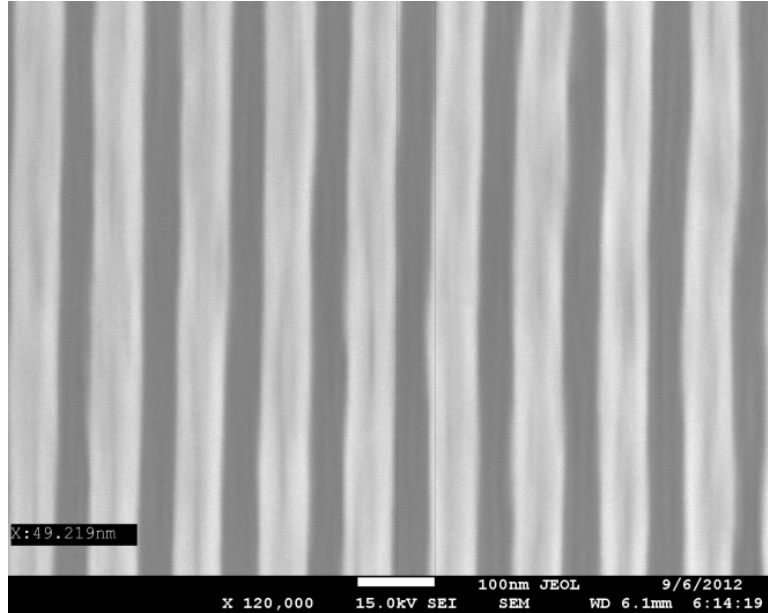
(a)
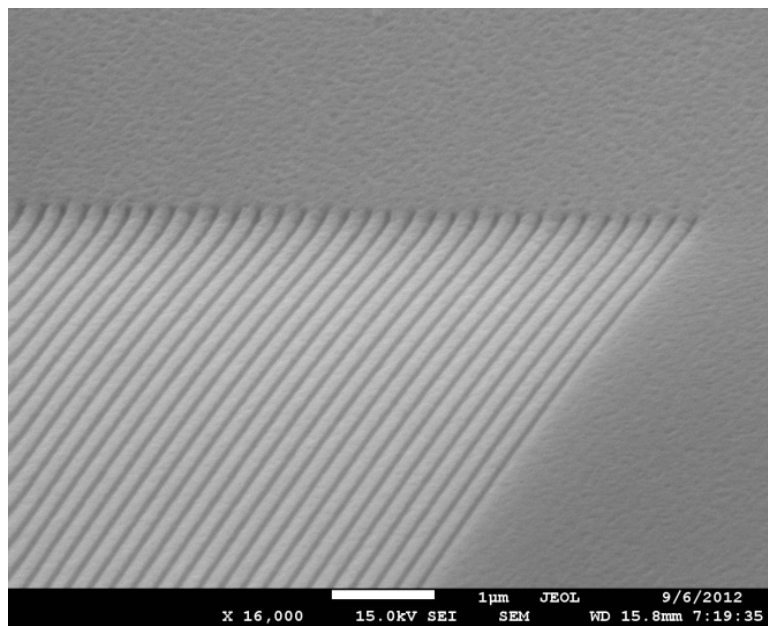


(b)

Figure 4.4. Fabricated nanowire polarization filters. (a) Top view; (b) side view.

# 4.5.2  Observation of Filters under Optical Microscope

Spectral response of the fabricated filters is verified by illuminating the filters with $0^o$ and $90^o$ polarized light and observing the samples under an optical microscope, as shown in Figure 4.5.
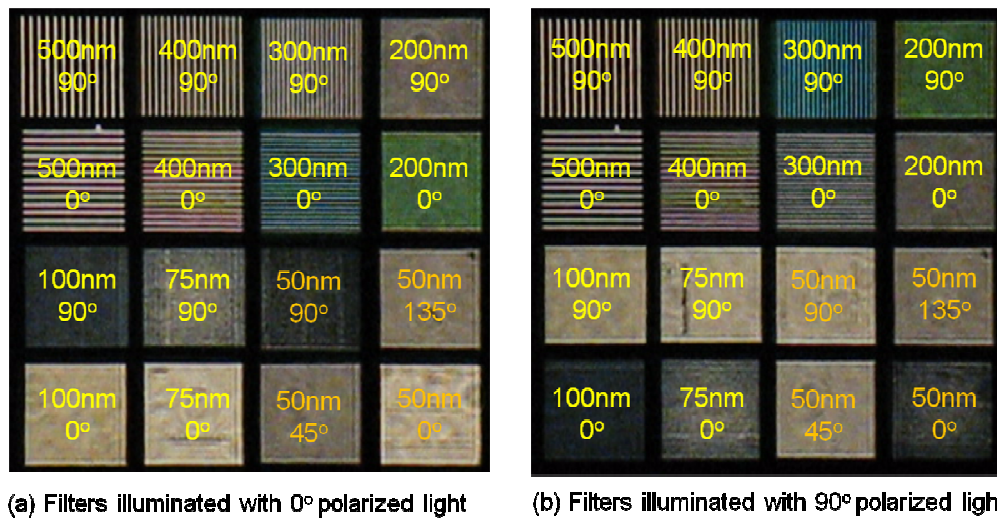


Figure 4.5. Fabricated polarization filters observed under an optical microscope.

Fabricated polarization filters, whose polarization axes are parallel to polarization axis of illuminating light, transmit the light otherwise they block it. Filters with smaller pitch size demonstrate higher contrast ratios than filters with larger pitch size. For instance, filter with 50nm pitch transmits parallel polarized light and blocks cross polarized light more effectively than filter with 100nm pitch. I also observed that filters with different pitch size transmitted light with different frequency components, an effect referred to as plasmon resonance. For instance, filter with 200nm pitch size transmitted mostly green light, while filter with 300nm pitch size transmitted mostly blue light. This indicates that we can fabricate polarization filters that respond to incident light of particular wavelength.

# 4.5.3  Optical Setup

The optical setup for evaluation of the fabricated nanowire polarization filters is shown in Figure 4.6. The fabricated filter is mounted onto a microscope glass slide and illuminated with uniform light supplied by narrow band OVTL01LGA LED via an integrating sphere. Optical power intensity of the LED is controlled by a GPIB programmable Agilent E3631A power supply. Light from the integrating sphere is transmitted through a linear polarizer that is rotated by a motor controlled by PC. Optical tube and objective lens are used to focus the light transmitted through the fabricated filter onto a CCD imaging sensor.
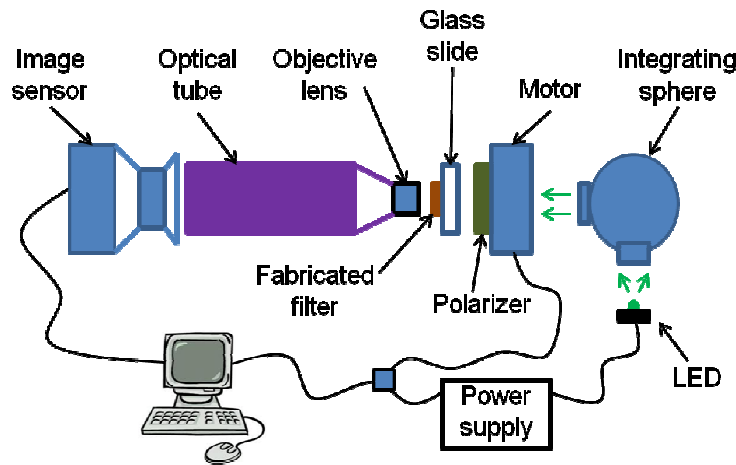


Figure 4.6. Optical setup for evaluation of fabricated polarization filters

# 4.5.4  Optical Performance Evaluation

An array of four nanowire polarization filters fabricated on the same glass substrate and oriented at $0^o$, $45^o$, $90^o$, and $135^o$ were evaluated using the setup described in Figure 4.6. The pitch of nanowires in the pixelated polarization filter is 50nm. Each filter occupies an area of 7.4μm by 7.4μm. The filter array is illuminated with light of

625nm supplied by an LED. The linear polarizer is rotated in order to expose the filter array with uniform linearly polarized light oriented at $0^o$, $45^o$, $90^o$, and $135^o$. Image frames recorded by the CCD imaging sensor are shown in Figure 4.7.

The fabricated filters have highest transmission response when they are illuminated with light whose angle of polarization matches their transmission axis, and have lowest transmission response when they are illuminated with light whose angle of polarization is perpendicular to their transmission axis. For instance, filter oriented at $0^o$ is brightest when illuminated with $0^o$ polarized light as shown in Figure 4.7a and it is darkest when illuminated with $90^o$ polarized light as shown in Figure 4.7c. This behavior agrees with the operation of polarization filters, i.e. they transmit parallel polarized light and reflect cross polarized light.

The experiment was repeated to encompass angle of polarization that range from $0^o$ to $180^o$ with increments of $10^o$. Recorded frames were analyzed to show intensity response of the four filters as presented in Figure 4.8.
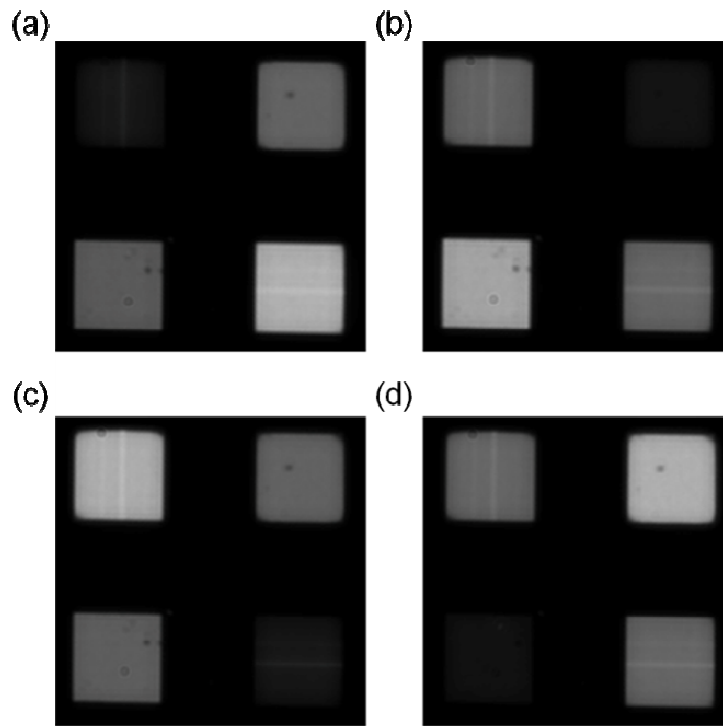
Figure 4.7. Fabricated filters oriented at 0°, 45°, 90°, and 135°. The filters are illuminated with (a) 0° polarized light; (b) 45° polarized light; (c) 90° polarized light; (d) 135° polarized light.
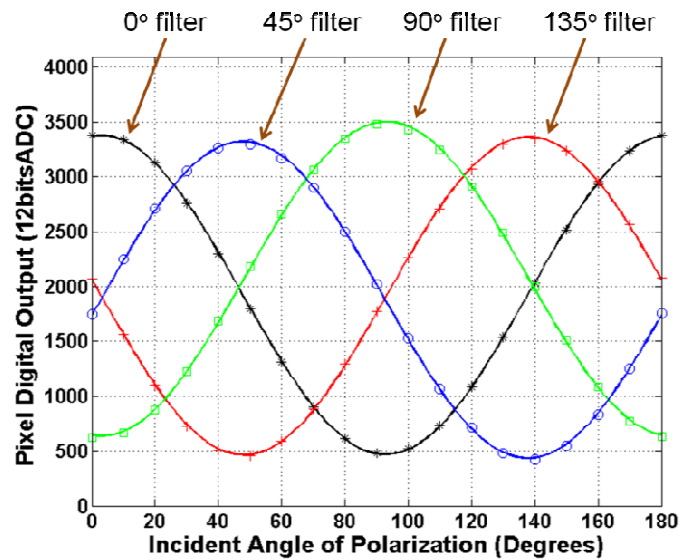


Figure 4.8. Intensity response of four filters oriented at 0°, 45°, 90°, and 135°.

Similarly, the fabricated filters have highest transmission response when they are illuminated with light whose angle of polarization matches their transmission axis, and have lowest transmission response when they are illuminated with light whose angle of polarization is perpendicular to their transmission axis. For instance, the filter oriented at $45^o$ has maximum and minimum peaks at $45^o$ and $135^o$ respectively.

# 4.5.5  Extinction Ratio

The extinction ratio is widely used to evaluate the performance of the polarization filters. It is defined as the polarization filter response ratio of the parallel polarized light (the maximum response) to the cross polarized light (the minimum response), as shown in Eq. (4.6).

$$Extinction\ Ratio = {I_{max}}\big/{I_{min}}$$ (4.6)
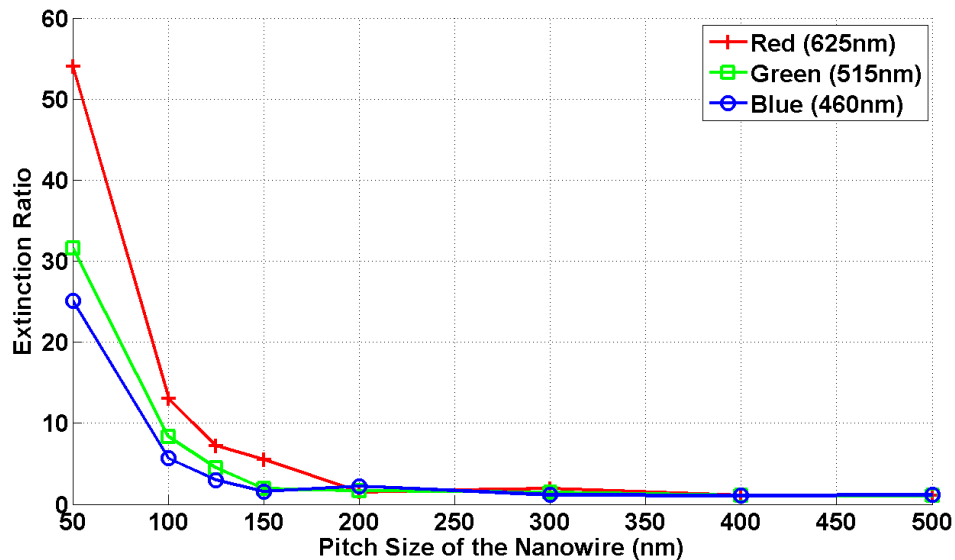


Figure 4.9. Measured extinction ratio for different nanowire sizes.

The measured extinction ratios of the pixelated polarization filters for different pitch sizes are shown in the Figure 4.9. Filter with nanowire pitch of 50nm and 50nm spacing have maximum extinction ratio of 55 at 625nm incident light. The same filters have extinction ratio of 25 for incident light at 460nm, i.e. 25~55 extinction ratio in visible spectrum. Nanowire polarization filters have spectral dependent extinction ratios as predicted by electromagnetic simulations [97]. The extinction ratio drops exponentially as pitch increases. Polarization information cannot be discerned with nanowire polarization filters whose pitch is larger than 150nm.

# 4.5.6 Transmittance

Furthermore, I evaluated the transmission properties of the different nanowire polarization filters. The transmittance is the amount of the parallel polarized light passing through the polarization filter.
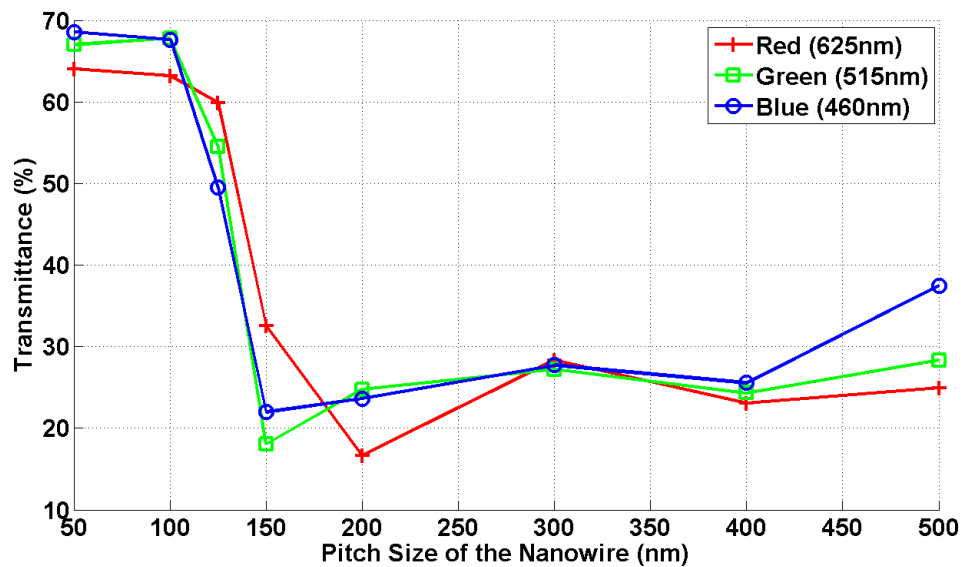


Figure 4.10. Measured transmittance for different nanowire sizes.

The measured transmittance of the pixelated polarization filters with different pitch of the nanowires is shown in the Figure 4.10. More than 60% transmittance can be achieved for the minimum pitch polarized filters. Once the pitch is larger than 150nm, transmittance drops to 20-30%.

## 4.5.7 Comparison of Measurement with Simulation Results

The rigorous coupled-wave analysis (RCWA) based electromagnetic simulation is widely used for analyzing periodic structures. I have simulated performance of polarization filters using RCWA method and compared the simulation results with my measurements as shown in Table 4.2. Both simulation and measurement results have similar trend for different nanowire pitches. The differences between the simulation and measurement results is mainly due to the fact that electromagnetic simulation is based on infinite periodic structure, while my pixelated polarization filters have finite grating structure, and brings strong boundary effects.

**Table 4.2Comparison between Measurement and Simulation (625nM)**

| Pitch Size | Extinction Ratio (Measured) | Extinction Ratio (Simulated) | Transmittance (Measured) | Transmittance (Simulated) |
|---|---|---|---|---|
| 50nm | 54.1 | 831.2 | 64.0% | 99.6% |
| 100nm | 13.1 | 70.5 | 63.2% | 97.2% |
| 150nm | 7.17 | 11.7 | 59.9% | 84.3% |

# 4.6    Conclusion

In this chapter, I investigated whether we can develop optical nano-structures that behave as linear polarization filters and monolithically integrate them with custom CMOS imaging sensor in order to realize a hybrid system capable of extracting polarization information from the imaged environment. I presented a fabrication procedure to realize pixelated nanowire polarization filter by using electron beam lithography and reactive ion etching. An array of pixelated polarization filters with different pitches and orientations were fabricated. The fabricated polarization filter achieved minimum pitch of 50nm, and its extinction ratio is up to 55 in visible spectrum. The influence of pitch and orientation on the performance of the pixelated polarization filter is also explored. In future, I will explore performance of pixelated polarization filter fabricated directly on the surface of the custom CMOS imaging sensor.

# Chapter 5

# Conclusion and Future Work

## 5.1    Conclusion

In this dissertation, I have explored realization of imaging sensors fabricated in advanced feature technologies that exploit velocity saturation mode of operation in transistors and are capable of extracting polarization information from the imaged environment.

In chapter 2, I investigated the employment of transistors operating in velocity saturation to design mixed mode circuits and systems for imaging sensors. I presented a CMOS imaging sensor containing two novelties in the field of current mode sensing. First the in-pixel read-out transistor operates in velocity saturation mode, which allows for high linearity between integrated photo charges and output current of the pixel. Second, the sensor employs a current conveyor circuitry that pins the drain potential on the read-out transistor of individual pixels using a feedback mechanism, which improves linearity of output current and spatial matching across the imaging array. This work demonstrates that we can exploit velocity saturation mode of transistor operation to design novel pixels, and improve noise characteristics and frame rate of current mode imaging sensors.

In chapter 3, I investigated monolithic integration of current mode imaging elements with current mode analog computational circuitry in order to perform image processing at the focal plane of an imaging sensor. I presented a linear current mode computational imaging sensor. The sensor monolithically combines current mode pixels

with current mode digitally programmable analog computational circuitry to perform spatial image processing at the focal plane. The image sensor provides a noise-corrected incident image in conjunction with a convolved image in parallel at 50 frames per second, and consumes 50mW of power. This work demonstrates real-time imaging and image processing implemented on the same chip via low power analog circuits. It is an attractive solution for applications where convolution is a significant portion of the signal processing algorithm.

In chapter 4, I investigated development of optical nano structures that behave as linear polarization filters and monolithically integrated them with custom CMOS imaging sensor in order to realize a hybrid system capable of extracting polarization information from the imaged environment. I presented a fabrication procedure to realize pixelated nanowire polarization filters by using electron beam lithography and reactive ion etching processes, which are compatible with semiconductor fabrication standards. I fabricated an array of pixelated aluminum polarization filters with different pitches and orientations. The fabricated polarization filters achieved minimum pitch of 50nm, which is about two times smaller (better) than the current state-of-the-art nanowire polarization filters. I integrated the polarization filters with custom CMOS and CCD imaging sensors to develop division of focal plane polarization imaging sensors.

# 5.2 Future Work

One of the challenges that remain to be addressed is that transistor models for advanced feature technologies are not well modeled for SPICE simulations. In future, I will incorporate my empirical results into existing transistor models. The improved transistor models will enable analog designers to reliably predict performance of circuits that exploit velocity saturation mode of transistor operation.

Another challenge that remains to be addressed relates to the errors that are introduced during the integration of the filters with imaging sensors. To mitigate these integration errors, I plan to fabricate the nano-structure polarization filters directly on the surface of custom CMOS imaging sensors. This will improve performance of hybrid sensors in accurately extracting polarization information from the imaged environment.

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