METAL CONTACTS ON LOW-DIMENSIONAL MATERIALS

by

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ABSTRACT

METAL CONTACTS ON LOW-DIMENSIONAL MATERIALS

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George Mason University, 2014

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As the scaling of the microelectronics is reaching nano regime, low-dimensional materials have been of increasing interest for future electronics applications. The low-dimensional materials, such as Si nanowires (SiNWs), carbon nanotubes (CNTs), graphene and transition metal dichalcogenides (TMDs), not only provide small body for further-scaled devices but also bring about new intrinsic properties for application in future optoelectronics, spintronics and so on. However, the small dimensions add significant difficulty for reducing contact resistance in the nanoelectronic devices. This dissertation presents a study of the metal contacts on low-dimensional materials. The focus of this work is on SiNWs and monolayer or few-layer MoS_2.

First, the metal contact on SiNW field effect transistors (FETs) was studied with a gate assisted Kelvin structure. In this work, I fabricated ambipolar SiNW FETs with Al contacts. The ambipolar characteristics and the gate assisted Kelvin structure enabled the

measurement of the contact properties of both electron and hole flows at the same contact. In this work I found that the contact performance is affected by the carrier type that flows in the channel as well as the current direction. In addition, an inverter was designed and realized on a single SiNW leveraged by the ambipolar FET characteristics.

Then, I have studied metal contacts on MoS_2, which is one of typical two-dimensional semiconductors. In the first part of this work, Ag and Ti contacts on exfoliated MoS_2 monolayers and few-layers are fabricated, characterized and analyzed. Based on the current-voltage (I-V) measurement, surface morphology and Raman spectroscopic measurement, I found that interface morphology plays an important role on the contact performance in MoS_2 FETs. In the second part of this work, gate-assisted contact measurement was carried out on chemical vapor deposited low-dimensional MoS_2 layers. The contact resistance and current crowding have been measured and analyzed at different gate bias. All these findings contribute to the understanding of metal contact on MoS_2.

SiNWs and MoS_2 are well-representative examples of emerging low-dimensional materials. The gate assisted contact measurement and metrology can also be applied to understand the metal contacts on other emerging low-dimensional materials.

CHAPTER 1: BACKGROUND AND INTRODUCTION

1.1 Emerging Applications of Low-Dimensional Materials in MOSFETs

As the dimensional scaling of the microelectronics is reaching the fundamental physical and economic limits, more and more low-dimensional materials have been studied for future applications. The representative materials include (but not limited to) semiconductor nanowires (NWs) [1-3], carbon nanotubes (CNTs) [4, 5], graphene [6-8] and transition metal dichalcogenides (TMDs) [9-11]. They not only provide a small body for further down-scaled device, but also bring about new physical properties to be integrated into future optoelectronics, spintronics and so on. The nanowires, such as Si nanowires (SiNWs), can be used in electronic devices for the application of 3-dimensional (3D) device morphology like FinFET [12] in current device technology. Others like III-V compound nanowires have been studied for future photonics applications. The small body with unique properties provides an excellent platform for down-scaling the devices to overcome the physical limit of the conventional 3-dimensional materials.

The surface roughness of ultra-thin body Si on insulator (UTSOI) becomes very large when the thickness approaches to 5 nm. Besides, the quantum confinement significantly enlarges the bandgap of Si when its thickness decreased to 5 nm and below. These situations limit UTSOI applications in further scaled electronics. Fortunately, 2-

dimensional (2D) semiconductors, such as TMDs [13-15] and black phosphorus, [16-18] have an intrinsic thin body with robust crystal structure. Their thickness is normally atomically thin (just couple of atom layers). But they still boast semiconducting properties with a scalable bandgap. In addition, the ultra-thin body and high mechanic strength of 2D materials are advantageous for the flexible and stretchable electronic devices. [19, 20] Also, in recent years, these devices gained much attention for medical applications.

Furthermore, the low-dimensional nature brings about attractive materials properties. For example, CNTs can be conductor or semiconductor according to their charity. [4] The semiconducting CNTs have a high carrier mobility which is attractive for high-frequency applications. [21] Like CNTs, graphene also has a high mobility because carriers in graphene are the massless Dirac fermions. [22] It has also attracted intensive attention for high-frequency applications [8]. Graphene radio frequency (RF) devices with cutoff frequency (f_T) of 300 GHz have also been demonstrated. [23] The long spin coherence time exhibited by graphene makes it also an interesting material to be used in spintronics and quantum computing. [24-26]

Unlike the bulk TMDs which are indirect bandgap semiconductor, the monolayer TMDs are usually direct bandgap semiconductor. [27, 28] As a result, they are preferred for both electronics and optoelectronic devices. More recently, researchers demonstrated significant valley polarization in graphene [29, 30] and MoS_2. [31, 32] This physical property might bring about a new concept of valleytronics into devices.

1.2 Challenges in Metal Contacts on Low-Dimensional Materials

Though low-dimensional materials have above-mentioned advantages and prospective for future applications, the small dimensions place significant obstacles on achieving low contact resistance in the electronic devices. As stated in International Technology Roadmap for Semiconductors, 2013 Edition, contact resistance has a large impact on device performance as devices are scaled to smaller dimensions. [33] Theoretically, the contact resistance is determined by the energy alignment between the metal work function and the semiconductor bandgap. However, metal/semiconductor interface usually forms Schottky barrier. Its barrier height cannot be effectively tuned by the metal Fermi level because of Fermi level pinning. [34] In the past, the contact resistance can be reduced with heavily doped semiconductor. In this way, the width of the Schottky barrier at the metal semiconductor interface is greatly reduced so that the tunneling through the barrier is highly enhanced. However, this is not possible in many nanoscale devices as the doping is difficult to control at that small dimensions. In addition, the alloy formed at the contact between metal contacts and semiconductor would consume considerable channel thickness in a nanoscale multigate FET, (e.g., FinFET). Furthermore, for nanomaterial based devices such as carbon nanotube, graphene, or other 2D materials, reducing the barrier height is the only option since the material is extremely thin. Ideally, in order to obtain ultra-low-resistance contacts the metal work function should be aligned with the semiconductor Fermi level. However, Fermi level pinning often has a strong effect on the interface of metal/semiconductor contact. [35-38] Thus, metal Fermi level should not be the only consideration for low

contact resistance. Other factors of the contact interface should also be considered to achieve low contact resistance.

1.2.1 CMOS Scaling and SiNW Contact Characterization

As the dimensional scaling of conventional metal-oxide-semiconductor field effect transistors (MOSFETs) is approaching the fundamental limits, several device structures have been explored to further extend the functionality of complementary metal–oxide–semiconductor (CMOS) technology. [39] Among them, the most attractive devices are nanowire / nanotube field effect transistors (FETs), FinFETs and junction-less FETs.[12, 40-42] For thin, nanoscale sidewall contacts, the contact resistance can be very large and behave differently than in planar devices. The contact mechanism in one-dimensional (1D) electronic system [4, 43] and method to minimize contact resistance in Si nanowire transistors [44, 45] have been previously reported. However, proper contact characterization metrology is still an important and urgent issue in nanoelectronics. [41] For a nanoscale channel with low or even intrinsic doping, the resistance of the channel (e.g., ungated current < 1 fA) is too large for conventional measurements. The conventional transfer length method (TLM) [46] and Kelvin test structure [47] are no longer suitable. Also, the conventional cross-bridge Kelvin test structure cannot be fabricated on a one dimensional nanowire. In addition, the resistance of the nanoscale source/drain (S/D) contacts is quite different to the contact measured in the absence of gate electric field, which if present will affect the current crowding at the contact. [48] Furthermore, the extremely small device dimensions will introduce poor doping

uniformity, and the S/D asymmetry can be formed under sufficient bias. The conventional metrologies, such as TLM and 4-probe methods, cannot efficiently and precisely extract the contact resistance of a single contact. [49]

To meet these challenges, we designed a gate-assisted Kelvin test structure based on Si nanowire (SiNW) FETs to study the properties of nanoscale S/D contacts. With the SiNW FET based Kelvin test structure, we can select and measure the contact resistance (R_C) of a single contact. Also, we can investigate the contact characteristics for pure electron or hole flow at the same contact, and study the effect of carrier flow direction on the contact properties. We selected Si nanowires as a test platform, but the metrology can be applied to other nanoscale devices, such as nanotube FETs and FinFETs.

1.2.2 Interface Impacts in MoS_2 Metal Contacts

Recently, layered materials, such as MoS_2 and WSe_2, have attracted intensive attention for electronic and optoelectronic applications. [10, 11, 50-52] Monolayer and few-layer MoS_2 can be treated as 2-dimensional (2D) semiconductor. Their bandgap ranges from 1.2 eV to 1.8 eV depending on the number of layers. [14, 15, 27] In particular, monolayer MoS_2 has a direct bandgap of 1.8 eV, very attractive for applications in optoelectronics. [27, 53, 54] In addition, the 2D MoS_2 is attractive for flexible electronic applications because of its intrinsic ultrathin body and robust lattice structure. [19, 20, 55] In the consideration of short channel effects in metal-oxide-semiconductor field effect transistors (MOSFETs), the 2D intrinsic ultrathin body represents the ultimately small scale. [56] Moreover, its inert surface has no dangling

bonds, which is advantageous for forming the channel-gate dielectric interface in MOSFETs. Monolayer MoS_2 MOSFET was the first demonstrated 2D TMD semiconductor MOSFET. [9] Such transistors have exhibited a high ON/OFF ratio of 10^8 and decent subthreshold slope of 74 mV/dec which are competent with state of art CMOS technology. [9]

Significant amount of work has been done to understand the transport mechanism in MoS_2 transistors and to improve their performance for future applications. [57-61] The Source/Drain (S/D) contacts are very important factors for device performance. Several contact structures have been used and studied to achieve a good Ohmic contact on MoS_2. [37, 38, 55, 62-64] It was expected that a metal with lower work function leads to a lower Schottky barrier for electron transport and results in a good n-type contact. [37]

However, the properties of metal contacts on MoS_2 is complicated and often suffers from Fermi level pinning which results in a Schottky barrier not fully tuned by the metal Fermi level. As shown in Fig. 1.1(a), the experimental results from S. Das et al. show that the barrier height between the MoS_2 channel and the metal contact is only weakly influenced by the metal work function and that an n-type barrier is formed between MoS_2 and a high work function metal such as Pt. [37] The theoretical work by C. Gong et al. confirms that partial Fermi level pinning in metal-MoS_2 contacts makes the Fermi levels in all studied metal-MoS_2 complexes except Pt are situated above the midgap of MoS_2, as shown in Fig. 1.1(b) [38] Additionally, S. McDonnell et al. demonstrated that intrinsic defects in MoS_2 dominated the metal-MoS_2 contact resistance and provide a low Schottky barrier independent of metal contact work function (Fig.

1.1(c)). [62] All above-mentioned results show that metal work function is not a good indicator for forming an Ohmic contact with MoS_2.

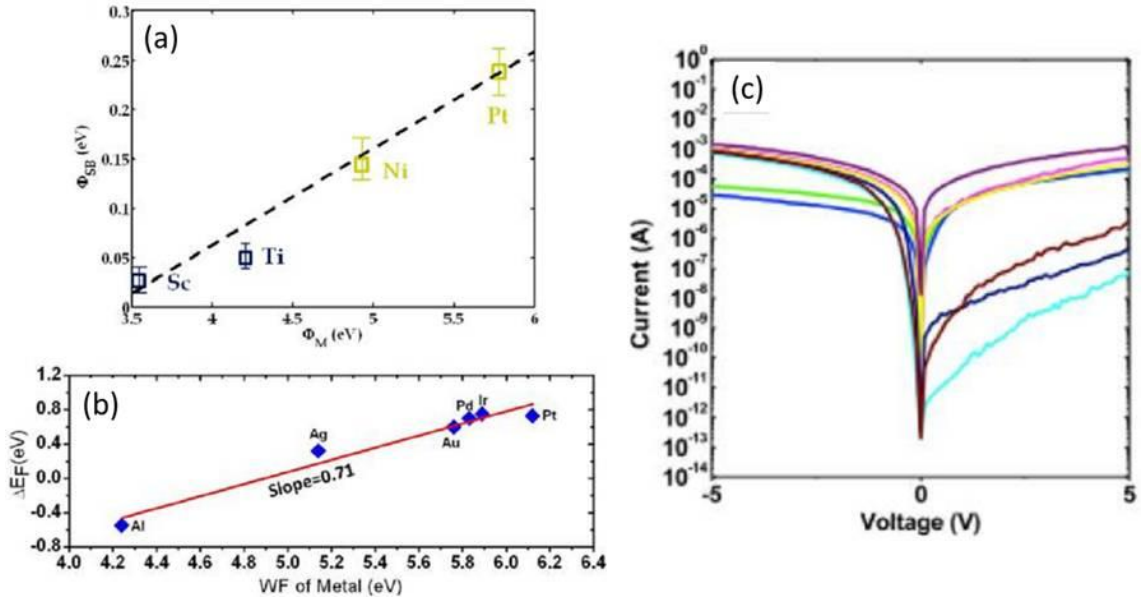

Figure 1.1 Complications in metal contacts on MoS_2. (a) Schottky barrier height changes in experiment where metals with different Fermi levels are used. The Fermi level is pinned to the edge of conduction band. (b) MoS_2 Fermi level changes after different metal contacts are applied in theoretical simulations. (c) I-V characteristics measured at different locations on a single piece of MoS2with the tungsten probe directly contacting the MoS_2

Previous studies on metal contacts to graphene or carbon nanotube indicated that the morphology of metal contacts and the interaction between these carbon-based materials and metal play important roles in contact resistance. [64, 65] Although it is well recognized that metal wettability plays an role in metal-MoS_2 contacts, [37] to our best knowledge, there is no work showing the direct evidence on how the metal contact

morphology affects the metal-MoS_2 contacts. In this work, for the first time, we have shown how the metal-MoS_2 interface influences the MoS_2 FET performance.

Ag was chosen because it has been reported to form a good contact on WSe_2, [66] which is a similar material to MoS_2. Previous work also shows that Ag has excellent wettability on bulk MoS_2. [67] We compare the results from Ag contacts with those from Ti contacts, which are commonly-used metal contacts on MoS_2 in the literature. [9, 37, 54, 68-71] Our results show that, despite of the similar work function around 4.3 eV for both metals,[72] monolayer and few-layer MoS_2 transistors with Ag contacts show significantly better electrical characteristics with more than 60-time higher ON-state current density and steeper subthreshold slopes.

The surface morphology of the metal films was then investigated. 5 nm thin layer of contact metal (Ag or Ti) capped with a 5 nm Au protection layer was deposited on top of MoS_2. Scanning electron microscopy (SEM) shows that Au/Ag formed a smoother and denser film on MoS_2. The surface roughness analysis was carried out by atomic force microscopy (AFM). The metal-MoS_2 interface was then investigated by Raman spectroscopy. The Raman spectra reveal that the contacting interface is between MoS_2 and Ag or Ti. The better wettability between Ag and MoS_2 is essential to form smoother and denser Au/Ag contacts on MoS_2, resulting in a better device performance. The strain effect introduced by Ag and heating effect introduced by Ti to monolayer MoS_2 are also revealed by the Raman spectroscopy.

1.2.3 Current Crowding in Metal Contacts on MoS_2

The current distribution under the metal contacts is an important property of the metal contacts. Some results show that the current would penetrate into the contact on a distance as large as several hundred of nanometers. [70, 73] However, their results are based on back-gated devices in which the channel current was not effectively tuned by the gate, and the Fermi level of MoS_2 under the contacts will be coupled to the back gate voltage. Here, we will present our work on the current crowding effect in metal-MoS_2 contacts which are affected significantly by a top gate. Our previous work shows that gate-assisted test structure is a good approach to test the contacts in low-dimensional electronic system. [74] We will extend the method to MoS_2 and do a cross comparison between Kelvin test structure and 4-probe method.

We fabricated Ag contacted bilayer MoS_2 transistors with 30 nm Al_2O_3 top gate on 300 nm SiO_2/Si substrate. The dimensions of our transistors are: 0.5 μm channel length, 4 μm channel width and 1 μm contact length. Ag was chosen because it has been reported to form a good contact on WSe_2, [66] which is a similar material to MoS_2. And our previous work shows Ag forms smooth and solid film on MoS_2 which makes the carrier transport efficiently across the contacts. Our devices show good n-type current-voltage (I-V) characteristics. Then gate assisted Kelvin structure and 4-probe method was used to analyze the contacts. The contact resistance extracted from the both methods is significantly different due to the difference in position where the voltage is sampled in each method. By comparing the contact resistance extracted from two methods, we found the current transfer length (L_T) of Ag-contact MoS_2 transistors is from 137 nm to 206 nm

(increased with the increasing gate voltage). The channel sheet resistance is measured by 4-probe method. It is much larger than the contact resistance which indicates that the MoS_2 transistors are channel dominant. The contact resistivity is then extracted from our data. It can be effectively tuned by the gate as well. Our result indicates that the gate affects the current crowding in the contacts, so as the contact resistivity.

1.3 Overview of Dissertation

In this dissertation, I will first present my work on the characterization of metal contacts on SiNW field effect transistors (FETs). In this work, metal contacts on SiNW FETs were studied with a gate assisted Kelvin structure. The SiNW devices were fabricated from chemical vapor deposited (CVD) SiNWs with conventional lithographic approaches. Al was used to form source/drain (S/D) contacts to SiNW transistors. The transistors exhibit ambipolar characteristics. The application of gate assisted Kelvin structure enabled the measurement of the contact characteristics of both electron- and hole-flow at the same contact. In this work, we found that the contact performance is affected by the carrier type that transport in the channel and also by the current transport direction. Also, based on the ambipolar characteristics of the transistors, an inverter was fabricated on a single SiNW.

Then, I will present an analysis of metal contacts on MoS_2, which is a 2D semiconductor. This work is divided into two parts. In the first part of this work, Ag and Ti contacts on exfoliated MoS_2 films are compared. Based on the current-voltage (I-V) measurement, surface morphology and Raman spectroscope, I found interface

morphology plays an important role on the contact performance in MoS_2 FETs. In the second part of this work, gated assisted contact measurement was carried out on CVD MoS_2 transistors. The contact resistance and current crowding were measured and analyzed under different gate bias. Our results show that the gate voltage influences both contact resistivity and transfer length of the contacts. This indicates that contact resistance changes with gate voltage. This work also indicates that in our MoS_2, the contacts play an important role in device performance. All these findings contribute to understanding the metal contact mechanism on MoS_2 as well as the MoS_2 transistor performance.

Finally, a brief summary of my work on the metal contacts is drawn and future plan of this work is laid out. It should be pointed out that although SiNWs and MoS_2 are good examples for low-dimensional materials, the gate assisted contact measurement can be applied on other emerging low-dimensional materials. The contact characterization metrology discussed in this thesis is very useful to many other applications such as in light emitting diode (LED) and photovoltaic devices where contacts are important.

CHAPTER 2: CONTACT CHARACTERIZATION ON AMBIPOLAR SINW FETS BASED ON GATE-ASSISTED KELVIN STRUCTURE

2.1 Introduction

In this work, a gate assisted Kelvin test structure based on Si nanowire field effect transistors has been designed and fabricated for the characterization of the transistor source/drain contacts. Because the Si nanowire field effect transistors exhibit ambipolar characteristics with electron current slightly lower than the hole current, we can select the type of carriers (electrons or holes) flowing through the same contacts and adjust the current by the applied gate voltage. With this method, we are able to measure the characteristics of the same contact with either pure electron or hole flow. In addition, we found that the nanowire contacts behave very differently depending on the current flow directions. This indicates that the source and drain contact resistance can be dramatically different. Such a gate assisted Kelvin Test structure will lead to future metrology and applications in nanoelectronics.

Then, an inverter based on ambipolar Si nanowire FETs was integrated on to a single SiNW. The inverter is consisted of two identical nanowire FETs on a single Si nanowire. The engaged FETs showed asymmetric ambipolar characteristics under positive and negative gate bias. A CMOS-like inverter can be realized on the single

nanowire, where one of the devices behaves as an nMOSFET and the other behaves as a pMOSFET.

2.2 Contact Resistance Dependence on Electron Transport Direction in Ambipolar SiNW FET

In this work, a gate assisted Kelvin test structure based on Si nanowire (SiNW) FETs has been designed and fabricated to study the properties of nanoscale S/D contacts. Although a Kelvin test structure based on planar MOSFETs has been previously reported,[75] the three-dimensional nanoscale contact presents an exciting challenge. With this SiNW FET based Kelvin test structure, we can select and measure the contact resistance (R_C) of a single contact. We can also investigate the contact characteristics for pure electron or hole flow, and study the effect of carrier flow direction influencing on the contact behavior. We selected Si nanowires as a test platform, but the metrology can be applied to other nanoscale devices, such as nanotube FETs and FinFETs.

2.2.1 Device Structure and Fabrication

The fabrication process can be summarized in Fig. 2.1.

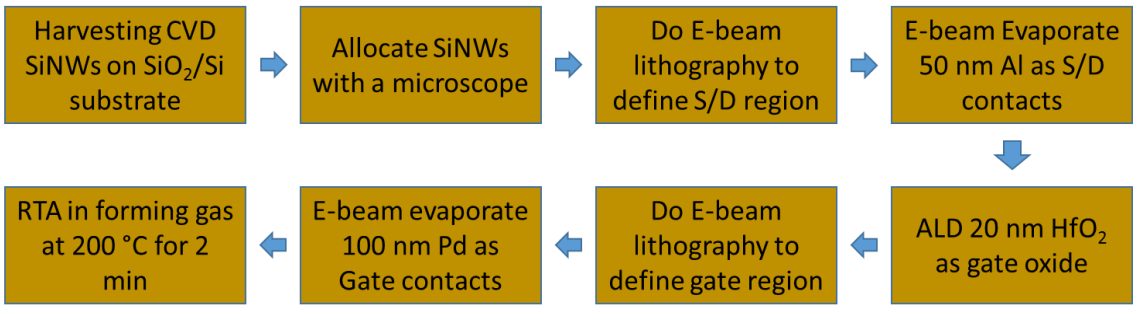

Figure 2.1 Fabrication process of SiNW transistors.

For the device reported here, the SiNWs were grown from Au catalyst by low pressure chemical vapor deposition (LPCVD) with SiH_4 as precursor. The SiNWs were grown at 450 ℃ for 2 hours with SiH_4 partial pressure of 500 mTorr. The resulting nanowires are in <111> orientation with an average diameter of the nanowires is 50 nm.

Then, the nanowires were harvested into methanol and dispersed on a Si substrate with 300 nm thermal SiO_2. The nanowires were oxidized at 750 °C to grow ≈ 2nm SiO_2, followed by e-beam lithography and metal formation. The S/D contact metal is Al of 1 μm width and 50 nm thickness. The gate/dielectric stack consists of 100 nm Pd on 20 nm HfO_2, deposited by atomic layer deposition (ALD) at 300 ℃. The samples were then annealed at 200 ℃ in forming gas for 2 minutes to improve the interface and metal

contacts. In the test structure, there are three identical contacts on a single SiNW, separated by two short channels (50 nm long) sharing a common gate.

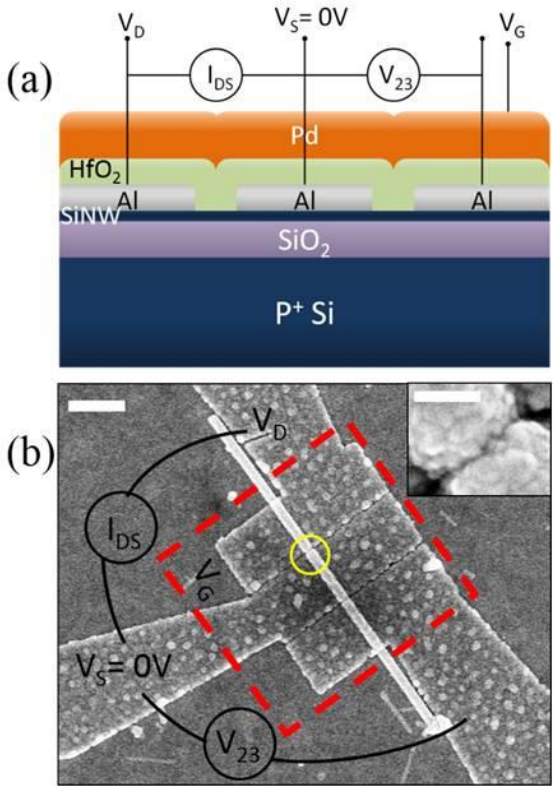

Figure 2.2 Device structure and measurement set-up. (a) Schematic of device structure and measurement set-up. (b) Scanning electron microscopic image of the SiNW gate assisted Kelvin test structure. Yellow circle shows the SiNW FET (channel length: 50 nm). The inset in (b) shows the magnified image of the yellow circled region. Scale bars in (b) and inset are 1 μm and 100 nm long, respectively.

As shown in Fig. 2.2, the gated Kelvin test structure consists of two SiNW FETs, sharing a common source, on a single nanowire. The resulting device scanning electron

microscopic (SEM) images and test setup is shown in Fig. 2.2. Even after the gate dielectric and contact formation, the position of the SiNW is still clear.

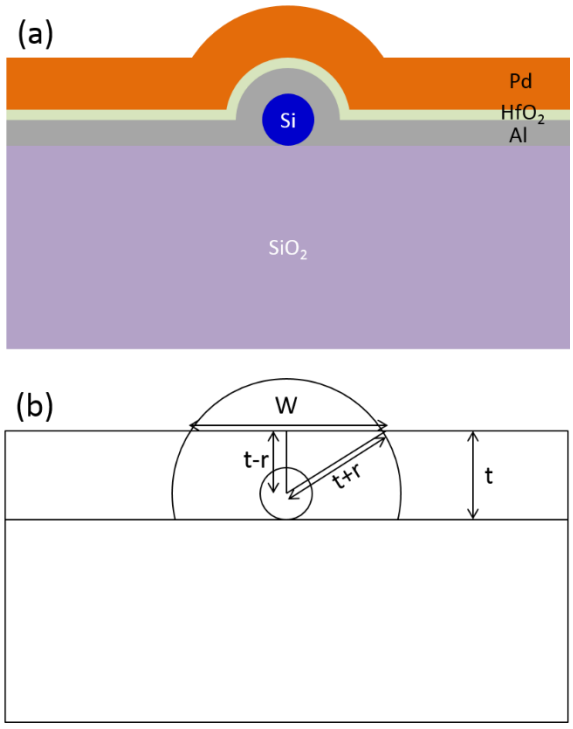

Figure 2.3 Scheme of the cross section off the SiNW under S/D contacts.

However, the dimension, especially diameter of the nanowire is obscured by the top layers. The width of the brighter pattern (202 nm in width) measured under SEM should be larger than the real diameter of the nanowire. As illustrated in Fig. 2.3(a), the measured width (W) is the width of the protrude region where the Si nanowire is covered by layers of Al, HfO_2 and Pd, totally 170 nm (≈ 50nm Al + 20nm HfO_2 + 100nm Pd). The width (W) in SiNW SEM image is not the SiNW diameter. The radius (r) can be

calculated following the schematic shown in Fig. 2.3(b), where t is the total thickness of the covering layers (170 nm).

The correlation between W and the radius of the Si nanowire can be estimated as:

$$\left(\frac{W}{2}\right)^2 + (t-r)^2 = (t+r)^2, \quad (1.1)$$

$$r = W^2/16t. \quad (1.2)$$

Therefore, the radius (r) and diameter of the Si nanowire are 15 nm and 30 nm, respectively. We drew this schematic of the cross section based on the cross section transmission electron microscopy (TEM) image of our previous devices. [76] The value of estimated diameter is quite consistent with our previous experiment where we used the same conditions to grow Si nanowires. [76]

2.2.2 Results and Discussion

The non-local voltage, V_{23} (Fig. 2.1) between the middle (2, the source: S) and one of the side contacts (3) is measured while a current (I_{DS}) is forced between the middle (2) and the other side contact (1, the drain: D), and thus the resistance of the middle contact is given by $R_C = V_{23}/I_{DS}$.

Fig. 2.4 shows the electrical measurements obtained with the above gate assisted Kelvin test structure. Fig. 2.4 (a) shows the drain current (I_{DS}) vs. gate voltage (V_{GS}) of the SiNW FETs at two source-to-drain voltage (V_{DS}) values. The SiNW FETs exhibit short-channel FET behavior with ambipolar characteristics. The electron current (positive V_{GS}) is lower than the hole current (negative V_{GS}). We did not intentionally dope the

SiNWs, therefore, the ambipolar behavior arises from the S/D contact properties. We believe the SiNW surface at the S/D contacts was doped p-type by Al diffusion during ALD of gate dielectric and these S/D junctions favor hole over electron flow (just one dopant atom in such a small nanowire body would be significant). [77]

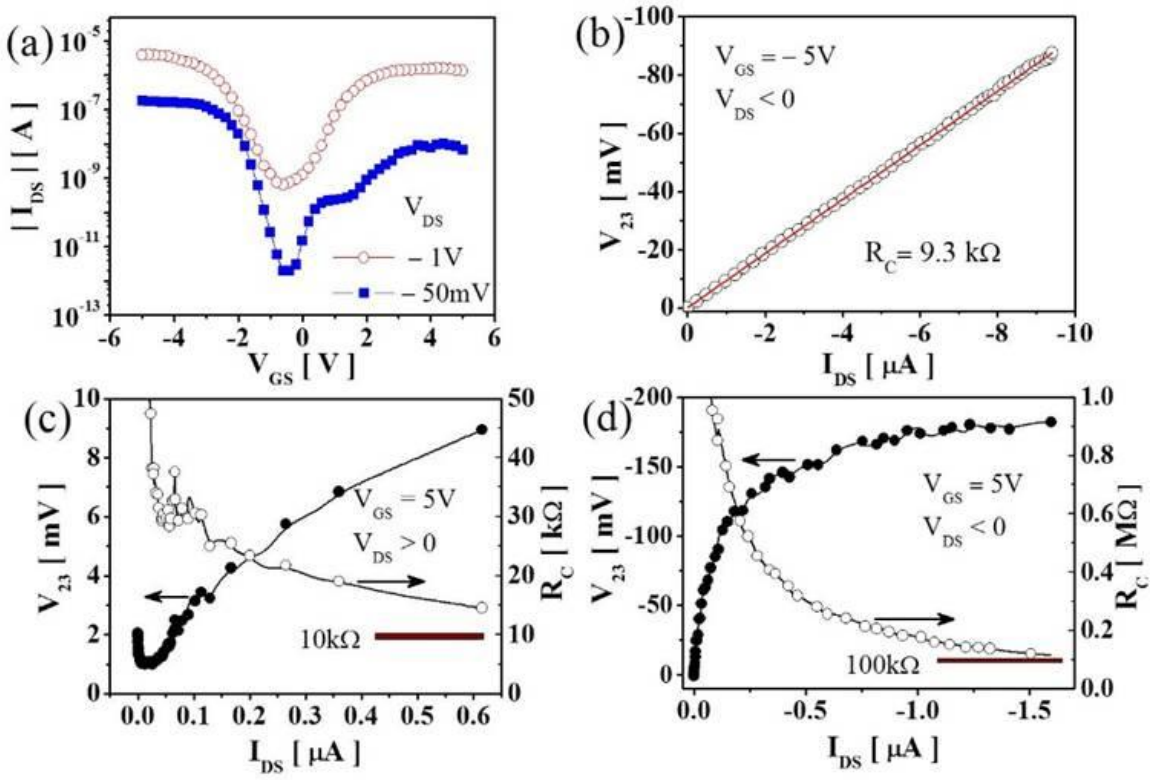

Figure 2. 4 Electric characterization: (a) Ambipolar I_{DS} vs. V_{GS} characteristics. (b) Hole contact characteristics selected by negative V_{GS}. Electron contact characteristics selected by positive V_{GS}: (c) electrons flow from Al to the SiNW channel; (d) electrons flow from the SiNW channel to Al.

To verify this, the electrical characteristics of the contacts are measured with the help of the gate assisted Kelvin test structure. Fig. 2.4(b) shows V_{23} versus I_{DS} at $V_{GS} = -5.0$

V (hole current) is linear, indicating the contact is Ohmic. The slope of the line shows $R_C \approx 9.3$ kΩ. For a Si nanowire of 30 nm in diameter and the contact of 1 μm in length, the specific contact resistivity for holes is thus $\rho_C \approx 8.8\times10^{-6}$ Ω•cm^2. This specific contact resistivity is estimated by $\rho_C = R_C A$, where A is the contact area. (A is estimated to be πDl, where D is the diameter of the nanowire and l is the length of the contact.) [78] Fig. 2.4 also shows the contact resistance R_C for electron conduction from the SiNW to Al (Fig. 2.4(c)) and from Al to the SiNW (Fig. 2.4(d)), respectively. As expected for this contact, the resistance for electron flow (e-flow) is larger than that for hole flow (h-flow) and exhibits diode-like current-voltage behavior. It is interesting to see that R_C depends on the e-flow direction. The R_C value for e-flow from Al to SiNW decreases with increasing I_{DS} and approaches the hole R_C at large I_{DS}. But the R_C value for e-flow from SiNW to Al is >10 times larger than the hole contact resistance. Such difference due to carrier flow direction is not seen in the h-flow contact resistance in these devices. The value of contact resistance and contact resistivity extracted by this gate assisted Kelvin structure can be much smaller than the value extracted by TLM method. [79] However, the distinct behavior of the contact responding to h- and e-flow is clearly seen. Especially for e-flow, the contact characteristics exhibit a diode-like pattern. The contact behaves significantly different depending on different carrier transport direction. It should be noted that the R_C dependence on e-flow direction indicates the asymmetry in source and drain contacts. The contact we tested is source contact for the e-flow from Al to SiNW, while it is drain contact for the e-flow from SiNW to Al. According to our I_{DS}-V_{GS} characteristics, under a sufficient drain voltage $|V_{DS}| = 1$ V, for the e-flow, the voltage

drop is ≈ 2% or ≈ 30% on this contact when it acts as source or drain contact respectively. Hence, from our results, R_C of drain contact is much higher (> 10 times) than that of source even if both contacts have identical physical characteristics. The conventional contact resistance characterization methods, such as TLM and 4-point measurement, cannot separate electron and hole flows or tell the difference between carrier flow directions.

The different contact behavior between h-flow and e-flow can be understood by the effects introduced by Al diffusion in Si. SiNW under the contact was doped into p-type because of the Al diffusion during the fabrication process. So that an Ohmic contact is expected for h-flow and a diode-like performance expected for the e-flow. To evaluate Al diffusion, we simulated Al diffusion in Si by using TCAD Sentaurus. Fig. 2.5 compares the Al concentration in the device before and after annealing. We generate a square Si nanowire with a high concentration of Al on the surface (Fig. 2.5(a)). The diameter of the Si nanowire is 50 nm. Our result shows after annealing the nanowire at 300 ℃ in O_2 ambient for 30 minutes sufficient Al diffused from surface into the Si (Fig. 2.5(b)). Like boron diffusion, O_2 enhancement of the Al diffusion is essential for the diffusion to happen at this low temperature. [80, 81] As O_2 plasma instead of H_2O was used as oxidant in ALD, it is reasonable to believe Al diffusion happened in our SiNW FET S/D contact.

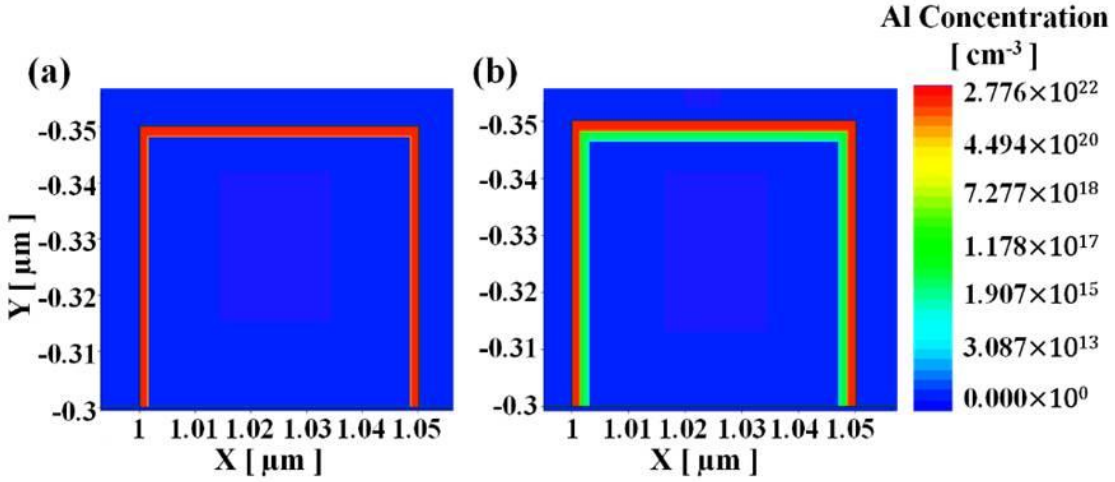

Figure 2. 5 Diffusion of Al in silicon: (a) Al concentration before annealing at 300˚C for 30 minutes in O_2. (b) Al concentration after annealing at 300˚C for 30 minutes in O_2.

Based on the doping concentration obtained from the diffusion simulation, the SiNW band diagram on the source contact adjacent under various bias conditions is generated by Sentaurus (see Fig. 2.6). The band bending is effectively tuned by V_{GS}. At negative V_{GS}, holes transport through the channel. It is clear an Ohmic contact is formed between channel and the source (Fig. 2.6(b)). At positive V_{GS} = 5.0 V, when V_{DS} = 1 V, electrons flow from Al contact to the SiNW channel (Fig. 2.6(c)), and vice versa for V_{DS} = −1V (Fig. 4d). The electrons going down the hill (Fig. 2.6(c)) will experience less resistance than the electrons climbing up the barrier hill to reach the Al contact (Fig. 2.6(d)). We believe that the R_C for electrons flow from Al to SiNW at large I_{DS} and the hole R_C represents the net contact resistance excluding the effect of junction below the contact. This result proves that the gate assisted Kelvin test structure based on nanoscale FETs can measure not only the R_C of high resistance materials, but also the net R_C for both

Ohmic and diode-like contacts because it can separate and select the electron and hole flow.

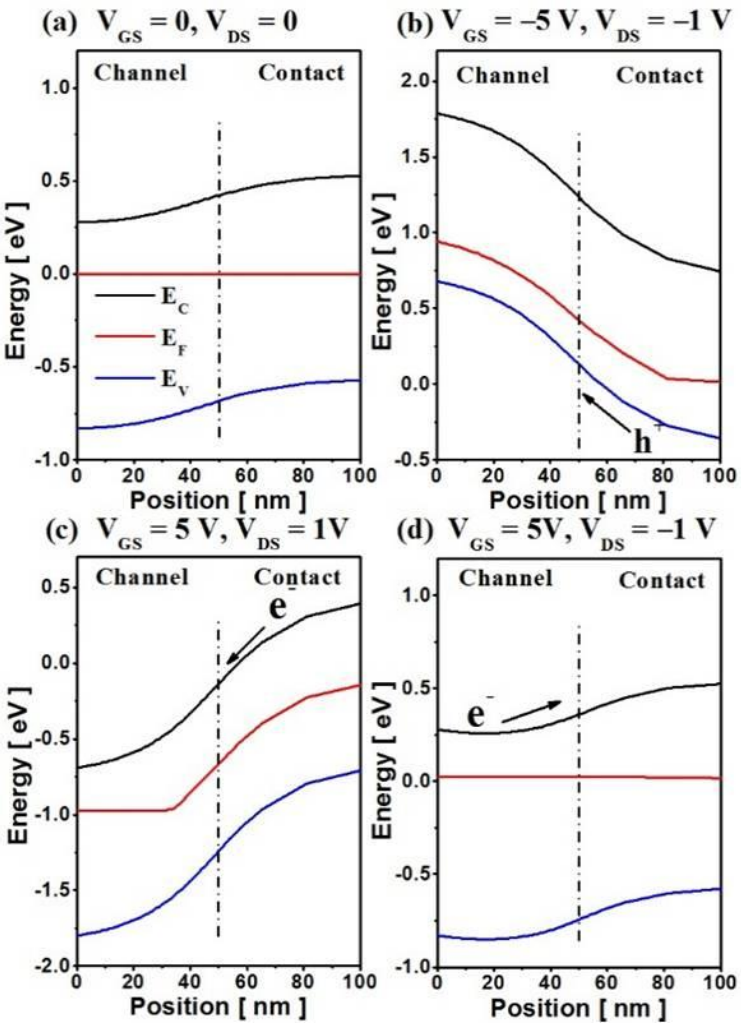

Figure 2.6 Band diagram from channel center to the contact at different conditions: (a) Equilibrium state. (b) $V_{DS} < 0$ and $V_{DS} < 0$: hole flow from Al to SiNW. (c) $V_{GS} > 0$ and $V_{DS} > 0$: electrons flow from Al to SiNW (d) $V_{GS} > 0$ and $V_{DS} < 0$: electrons flow from SiNW to Al.

2.2.3 Conclusion

In summary, we have designed and fabricated the gate assisted Kelvin test structure based on SiNW FETs. This test structure can efficiently detect the properties of electron and hole flows at the same nanoscale contacts. It has been found that the electron and hole flow resistances are very different; and the non-Ohmic contact resistance has a strong dependence on current direction. Also, the asymmetry between the source and drain contacts in a nanoscale FET can be determined by the gate assisted structure. Such an interesting gate assisted Kelvin test structure will lead to expand characterization metrology and may have important applications in nanoelectronics.

2.3 Inverter on a Single SiNW

As the scaling of Complementary Metal-Oxide-Semiconductor Field Effect Transistor (CMOS FET) continues, the challenge of short-channel effects (SCE) and exponentially increasing cost has almost become an impossible task for conventional bulk-Si based CMOS technology. [82] Several novel channel materials such as III-V compounds and graphene, and device structures including multi-gate and FinFETs were investigated to achieve better device performance like extended high frequency respond or lower subthreshold slope. Among these candidates, Si nanowire (SiNW) is the most attractive channel materials for future CMOS FET due to its intrinsic semiconductor properties, small dimension and fully CMOS compatibility. We have been engaged in the research of bottom-up Si nanowire FETs with gate-all-around (GAA) structure for high performance. [76, 83] GAA structure provides excellent electrostatic gate control over transistor

channel even when channel length down to below 10 nm. [82] The SiNW based electronics built on a bottom-up self-assembly will have the advantage of low cost and high density.

However, the difficulties in controlling the doping level of SiNW make it too complicated to make traditional FETs with n-p-n or p-n-p doping structure. [2, 3] SiNWs with Schottky contacts (also indicated as Schottky barrier FETs) were demonstrated that they can work as enhancement-mode FETs. [43] In this case, the drain current level depends on the contact metal work function. The different conduction mechanisms for accumulation- and inversion-mode operation make it possible to make FETs with ideal ambipolar characteristics, so that an inverter can be integrated onto just one single nanowire with two identical MOSFETs one of which works as pMOS and the other as nMOS. In this work, we have designed a single-nanowire CMOS inverter based on ambipolar SiNW FETs with 50 nm channel length which we used in gate assisted Kelvin contact characterization.

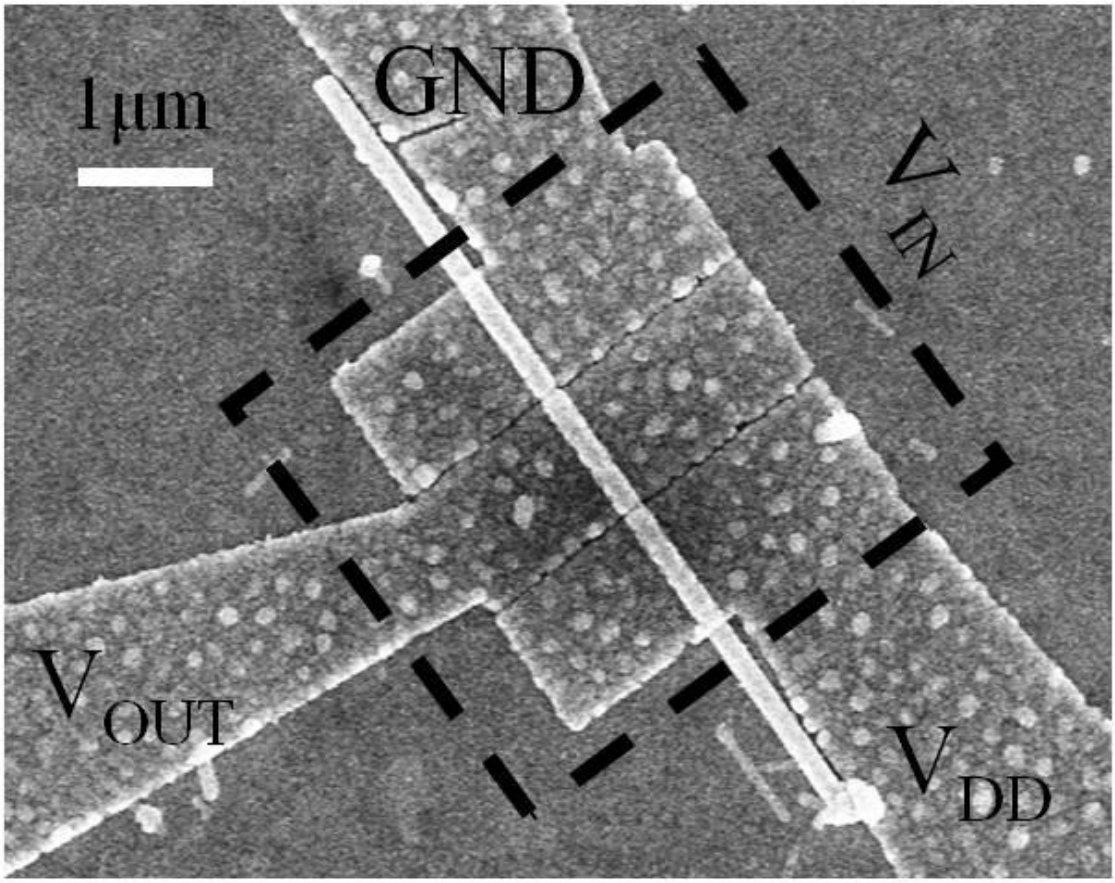

Figure 2. 7 SEM image and measure set-up of the inverter

The fabrication process and device structure are the same as previous SiNW FETs we used in contact characterization. The measurement set-up is illustrated in SEM image Fig. 2.7. The ambipolar I-V characteristics of the transistors inspired the possibility of fabricating CMOS logic gates using these SiNW FETs. A CMOS inverter based on two identical ambipolar SiNW FETs with 50-nm channel length built on one single nanowire (see Fig. 2.4). We measured the device with voltage supply (V_{DD}) of 2 V, and swept the input voltage from 0 to 4V (Fig. 2.8). The voltage transfer curve is slightly asymmetry in

this input range, but has small noise margin. The transfer happens mostly from 1V to 3V. So if we bias the input voltage to around 2V, we can get a symmetric output in a 2V input range from (2-1) V to (2+1) V.

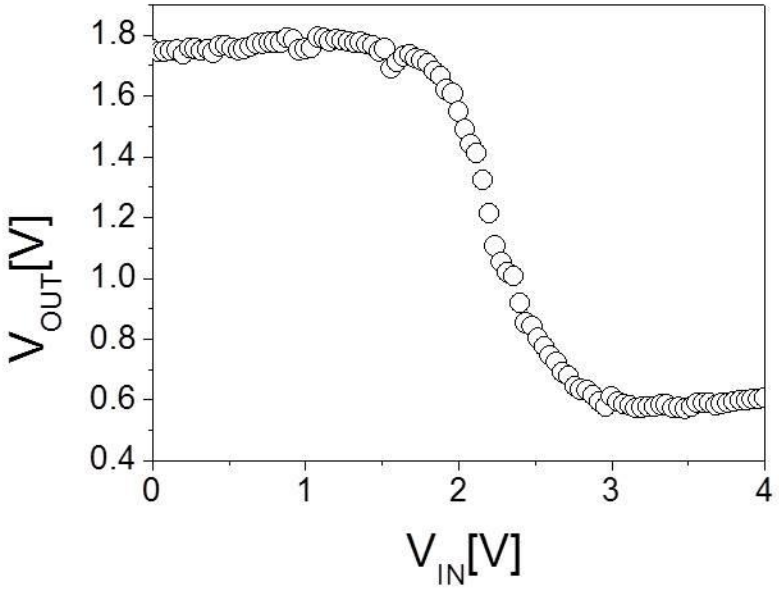

Figure 2.8 Voltage transfer characteristics of single nanowire CMOS inverter under V_{DD} = 2 V and V_{IN} = 0~4 V.

The inverter works properly with slightly asymmetric behaviors and a small noise margin in voltage transfer. These issues can be resolved by engineering the threshold voltages and decreasing off-state current. In addition, the inverter has a very simple and yet very efficient structure. Various logic gates based on ambipolar SiNW FETs can be fabricated in two lithographic steps. Due to the scalability of nanowires and the

advantage of bottom-up process, this approach can lead to low-cost, high-density nanoelectronics circuitry.

CHAPTER 3: ROLE OF INTERFACE MORPHOLOGY ON METAL CONTACTS TO MoS_2

3.1 Introduction

Recently, MoS_2 has attracted a lot of attention for electronic and optoelectronic applications. [10, 11, 50-52] Layered MoS_2 is a 2-dimensional (2D) semiconductor which has a bandgap ranging from 1.2 eV to 1.8 eV depending on its thickness. [14, 15, 27] In particular, monolayer MoS_2 with a direct bandgap of 1.8 eV shows promising applications in optoelectronics. [27, 53, 54] 2D MoS_2 is also attractive for flexible electronic applications because of its intrinsic ultrathin body, and robust lattice structure.[19, 20, 55] Considering short channel effects in metal-oxide-semiconductor field effect transistors (MOSFETs), this intrinsic ultrathin body also represents the ultimate in scaling. [56] Moreover, its inert surface has no dangling bonds, which is advantageous for forming the channel-gate dielectric interface in MOSFETs. Monolayer MoS_2 MOSFET was the first demonstrated 2D TMD semiconductor MOSFET. [9] Such transistors have exhibited a high ON/OFF ratio of 10^8 and decent subthreshold slopes of 74 mV/dec which is compatible with current state of art CMOS technology.

Various work has been done to understand the transport mechanism in MoS_2 transistors and to improve their performance for future applications. [57-61] The Source/Drain (S/D) contacts are very important factors for device performance. A variety

of contacts have been used and studied to achieve a good Ohmic contact on MoS_2. [37, 38, 55, 62-64] It was originally expected that a low work function metal may lead to a lower Schottky barrier for electron transport and result in a good n-type contact. [37] However, the experimental results from S. Das et al. show that the barrier height between the MoS_2 channel and the metal contact is only weakly influenced by the metal work function and that an n-type barrier even forms between MoS_2 and high-work function metal such as Pt. [37] The theoretical work by C. Gong et al. confirms that partial Fermi level pinning in metal-MoS_2 contacts makes the Fermi levels in all studied metal-MoS_2 complexes except Pt are situated above the midgap of MoS_2. [38] Additionally, S. McDonnell et al. demonstrate that intrinsic defects in MoS_2 dominate the metal-MoS_2 contact resistance and provide a low Schottky barrier independent of metal contact work function. [62] All these complications show that metal work function is not a good indicator for forming an Ohmic contact with MoS_2.

Previous studies on metal contacts to graphene or carbon nanotube demonstrate that the morphology of metal contacts and the interaction between these carbon materials and metal contacts play important roles in contact resistance. [64, 65] Although it is well believed that metal wettability plays an important role in metal-MoS_2 contacts, [37] to our best knowledge, there is no work showing the direct evidence on how the metal contact morphology affects the metal-MoS_2 contacts. In this work, for the first time, we have shown how the metal-MoS_2 interface influences the MoS_2 FET performance.

Ag was chosen because it has been reported to form a good contact on WSe_2, [66] which is a similar material to MoS_2. Previous work also shows that Ag has excellent

wettability on bulk MoS_2. [67] We compare the results from Ag contacts with those from Ti contacts, which are commonly-used metal contacts with MoS_2 in the literature. [9, 37, 54, 68-71] Our results show that, despite of the similar work function around 4.3 eV for both metals, [72] mono- and few-layer MoS_2 transistors with Ag contacts show significantly better electrical characteristics with more than 60-time higher ON-state current density and steeper subthreshold slopes.

The surface morphology of the metal films was then investigated by depositing 5 nm thin layer of contact metal (Ag or Ti) capped with a 5 nm Au protection layer on top of MoS_2. Scanning electron microscopy (SEM) shows that smoother and denser Au/Ag film is formed on top of MoS_2. The surface roughness analysis was carried out by atomic force microscopy (AFM). The metal-MoS_2 interface was then investigated by Raman spectroscopy and the Raman spectra reveal that the contacting interface is between MoS_2 and Ag or Ti. The better wettability between Ag and MoS_2 is essential to form smoother and denser Au/Ag contacts on MoS_2, resulting in a better device performance. The strain effect introduced by Ag and heating effect introduced by Ti to monolayer MoS_2 are also revealed by the Raman spectroscopy.

3.2 Experimental Methods

3.2.1 Sample Preparation:

The sample preparation starts with exfoliating bulk MoS_2 (SPI® small crystals) into mono- and few-layer films on 280nm SiO_2 / Si. The MoS_2 film thickness was confirmed by the color, Raman spectroscopy and AFM. (Figure 3.1) As seen in Figure

3.1(c), the distance between the two characteristic Raman peaks increases as the thickness of MoS_2 increases. This trend has been published repeatedly and widely accepted as a method the determine MoS_2 film thickness when it is only a few layers thick.[84] This thickness is also compared to AFM results to set a reference to identify MoS_2 thickness.

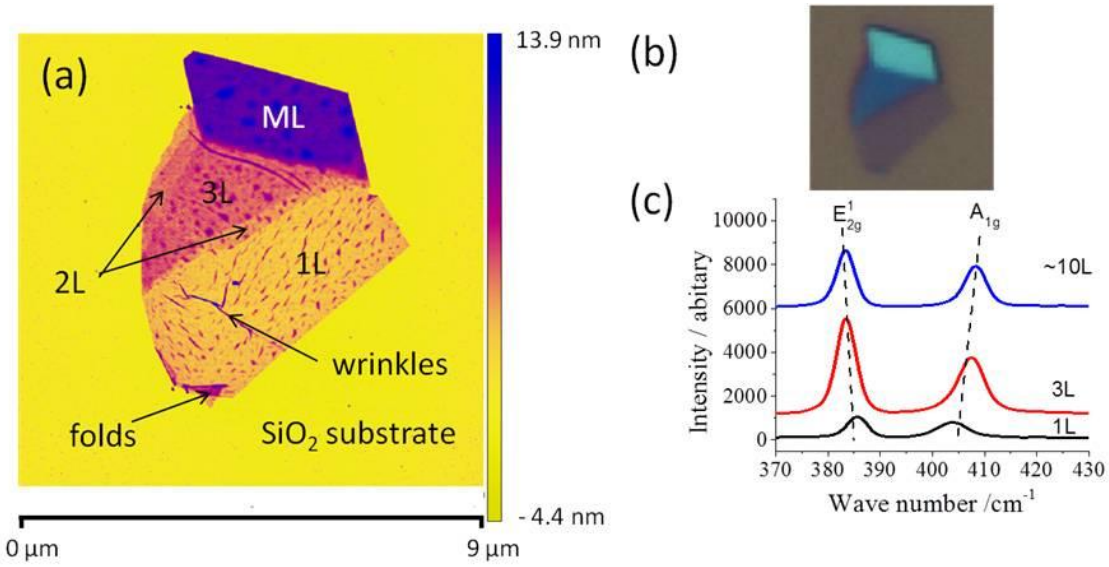

Figure 3.1 MoS_2 flake on SiO_2/Si substrate. (a) AFM image of a MoS_2 flake which includes monolayer, trilayer and multiple layer regions. (b) Optical image of the same flake. (c) Raman spectra of different thickness MoS_2 which is collected from the different positions on the same flake of MoS_2.

Then the back-gated mono- and few-layer MoS_2 transistors were fabricated for electric measurement. The detailed fabrication process is as following.

1. The MoS_2 flake positions are identified with pre-designed alignment marks by an optical microscope.

2. Pattern the source/drain contacts with electron-beam lithography. 495 PMMA A4 resist was used as resist. The resist was coated by spinning it onto the substrate at rotation speed of 3000 rpm for 45 sec. Then the substrate was heated on a hot plate at 180 ˚C for 2 min. The accelerate voltage of the e-beam was 20 kV in the e-beam lithography system. And the exposure dose was 160 $\mu As/cm^2$.
3. Metal deposition to form S/D contacts by e-beam evaporation. We deposited 30nm Au / 30nm Ag (contact layer) for Ag contacted MoS_2 FETs and 30nm Au / 30nm Ti for Ti contacted ones as the contact metals. The system pressure was kept at $\approx 1\times10^{-6}$Torr during the metal deposition. The first 5nm of metal which directly contacted to MoS_2 was deposited at a lower rate of ≈0.2Å / sec to improve the interface roughness, and rest of metal was deposited at a higher rate of ≈1Å / sec.
4. Lift off the metal by soak the sample into acetone over night at room temperature. The sample was rinsed with IPA and DI water after the acetone bath. The resulting devices have a channel length of 1 μm and contact width of 1 μm as well.

We also prepared samples for the interface characteristics. To do so much thinner metal film was e-beam evaporated on to exfoliated MoS_2. Samples for SEM, AFM and Raman spectroscopy are prepared in the same way except no e-beam lithography and lift off step and the thickness of metal deposited is thinner. 5nm Au / 5nm Ag and 5nm Au / 5nm Ti was deposited by e-beam evaporation. The top 5 nm Au is used as a capping layer

which protects the bottom contact layer from oxidizing. The e-beam evaporation conditions used are the same with device fabrication except that the deposition rate was kept at ≈0.2Å / sec for the whole metal deposition process to mimic the device fabrication.

3.2.2 Characterizations:

The electric properties of MoS_2 FETs were tested in a vacuum probe-station. The system was kept at $\approx 1\times10^{-6}$ Torr during the measurement. A semiconductor parameter analyzer (HP 4156C) was used to carry out the electric measurement. The SEM is done with Zeiss Ultra-60 Field Emission SEM. An accelerate voltage of 5kV was used to capture the images. AFM images are taken with Dimension system controlled by Nanoscope V (Bruker, Santa Barbara, CA). All AFM experiments are performed with SCANANASYST-AIR tip (Bruker, Santa Barbara, CA) with a radius of 10nm. AFM data are analyzed with WSxM software.[85] Raman spectra were acquired under ambient conditions with a micro-Raman spectrometer (Renishaw InVia Raman system) equipped with a 514.5nm (2.41 eV) wavelength excitation laser and an 1800 lines/mm grating while operating in 180 °backscattering geometry. A 50X objective was used to focus the excitation laser to an approximately 1μm spot onto the sample. The 100% laser power is 4.8mW. We typically used 50% power to collect the signal for 1 second to compare the Raman spectra before and after metal deposition.

3.3 Results and Discussion

3.3.1 Electrical Characterization of MoS_2 transistors

Our devices were fabricated with exfoliated MoS_2 on 280 nm SiO_2/Si substrate. We deposited 30 nm Au/30 nm Ag for Ag contacted MoS_2 FETs and 30 nm Au/30 nm Ti for Ti contacted ones by e-beam evaporation. The resulting devices have a channel length of 1μm and a contact width of 1μm as well (**Figure 3.2**(a)).

Figure 3.2(b-d) shows the electric characteristics of monolayer MoS_2 transistors. We normalized the drain current (I_D) to the current density per 1 μm channel width (J_D) to compare the electrical characteristics of transistors with different channel width. Figure 3.2(b) compares the characteristics of J_D versus back gate voltage (V_{BG}) (J_D-V_{BG} characteristics) in monolayer MoS_2 transistors with Ag and Ti contacts. The devices were tested with V_{BG} varying from -100 V to 0 V and drain to source voltage (V_{DS}) equals to 50 mV or 1 V. All our devices show n-type MOSFET behaviours. The threshold voltage of the devices was extracted from the linear fitting of the ON-current versus V_{BG} with V_{DS} = 50 mV. The device threshold voltages are equal to −36.6 V and −45.4 V for Ag and Ti contacts, respectively. These results are reasonable since Ag and Ti have similar work functions. The devices with Ti contacts show a typical ON-current density, which is comparable to other back gated MoS_2 transistors without high-k dielectric passivation. [68-70] Most importantly, the devices with Ag contacts exhibit almost two orders of magnitude larger on-state current density than those with Ti contacts. We extracted subthreshold slope (SS) of the devices, which is given by:

$$SS = \frac{dV_{BG}}{d(\lg(I_D))}\Big|_{V_{DS}} \quad (1)$$

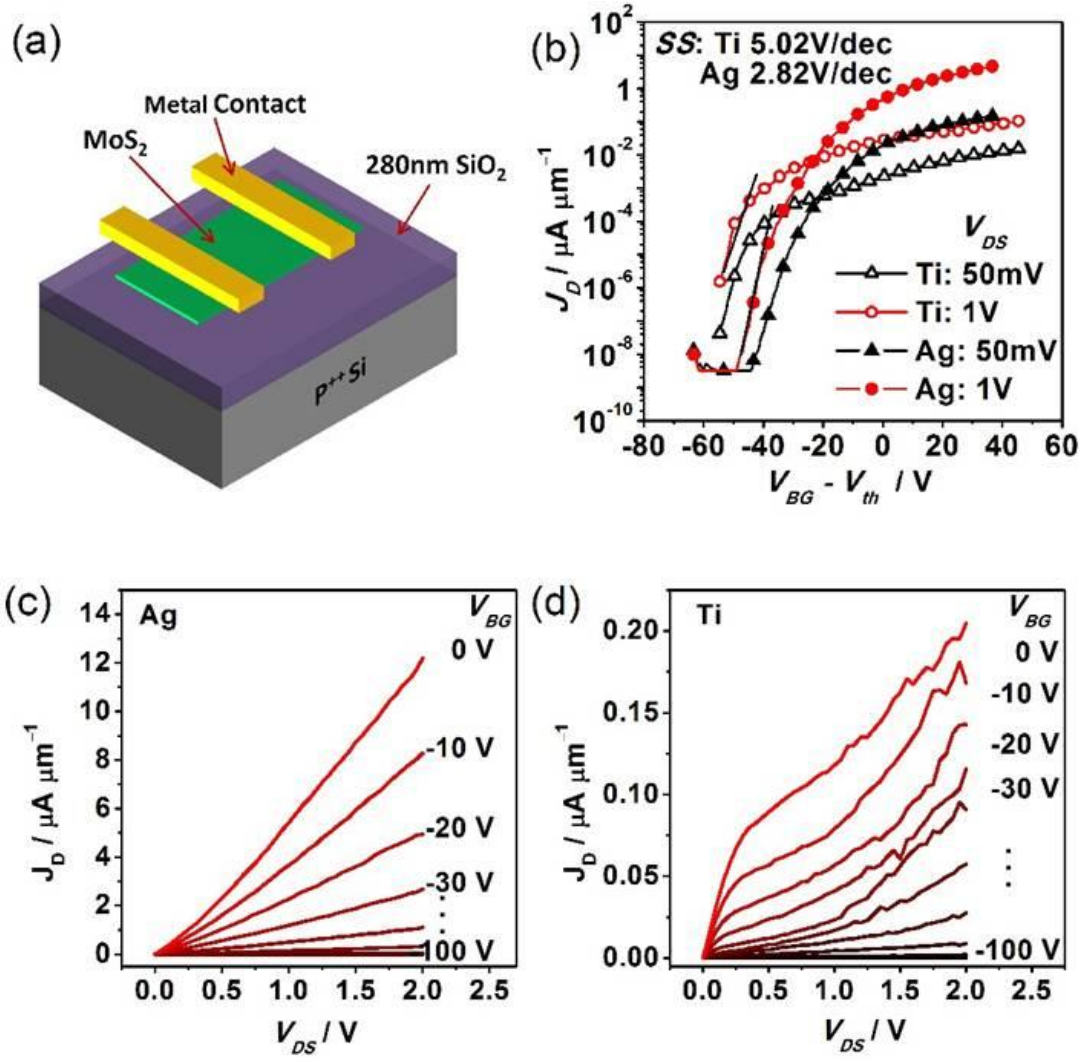

Figure 3. 2 MoS_2 transistor diagram and Drain current density of single-layer MoS_2 transistors: (a) MoS_2 transistor diagram Drain current density of single-layer MoS_2 transistors versus (b) V_G-V_{th} with Ag or Ti contacts, and (c, d) drain voltage (V_{DS}) with (c) Ag or (d) Ti contacts.

SS was extracted from J_D-V_{BG} characterization at V_{DS} = 1 V. For devices with Ag contacts, the SS is 2.82 V/dec, and with Ti contacts, it is 5.02 V/dec. The large SS is partially due to the large thickness (280 nm) of back gate oxide. Similar SS value was also reported in the back-gated MoS_2 FETs in previous publications. [68, 70] The lower SS of devices with Ag contacts indicates the improved contact quality. It is clear that the device performance is significantly affected by the contacts. Better contacts bring about better electrostatics so that devices with Ag contacts show a lower subthreshold slope.

Figure 3.2(c) and (d) compare J_D-V_{DS} (source-drain voltage) characteristics of monolayer MoS_2 FETs with Ag and Ti contacts, respectively. The drain current was measured with V_{DS} varying from 0 to 2 V with V_{BG} varying from 0 to −100 V with a −10 V step. In Figure 3.2(c), the super-linear relationship between ON-state J_D and V_{DS} near zero in monolayer MoS_2 FETs with Ag contacts indicates the Schottky barrier transistor behaviour. In figure 3.2(d), the ON-state current density of MoS_2 FETs with Ti contacts is consistent with previous publications, [68, 70] and significantly smaller than the ones with Ag contacts. The linear dependence of J_D on V_{DS} could be a result of thermally assisted tunnelling, and may not necessarily indicate an Ohmic contact. [37] The current density of monolayer MoS_2 FET with Ag contacts is 60 times larger at V_{BG} = 0 V and V_{DS} = 2 V than that with Ti contacts. This larger magnitude of ON-current density reflects the higher carrier injection efficiency.

Figure 3.3 shows electrical properties of few-layer (2 to 3 layers) MoS_2 FETs. The drain current in these few-layer MoS_2 FETs was measured under the same bias conditions as the monolayer devices. In Figure 3.3(a), J_D-V_{BG} characteristics of few-layer

MoS_2 FET with Ag and Ti contacts were compared. All the devices show n-type MOSFET behaviour. The threshold voltage is −35.0 V for devices with Ag and Ti contacts. The subthreshold slope of transistors with Ag contacts is 5.42 V/dec. The devices with Ti contacts also show typical performance reported in previous publications. [68-70] The few-layer MoS_2 transistors with Ti contacts cannot be turned off completely even at V_{BG} = −100 V. Therefore, the subthreshold slope cannot be precisely extracted. Nonetheless, the comparison between these two devices does show improved current density and subthreshold slope with the Ag contacts.

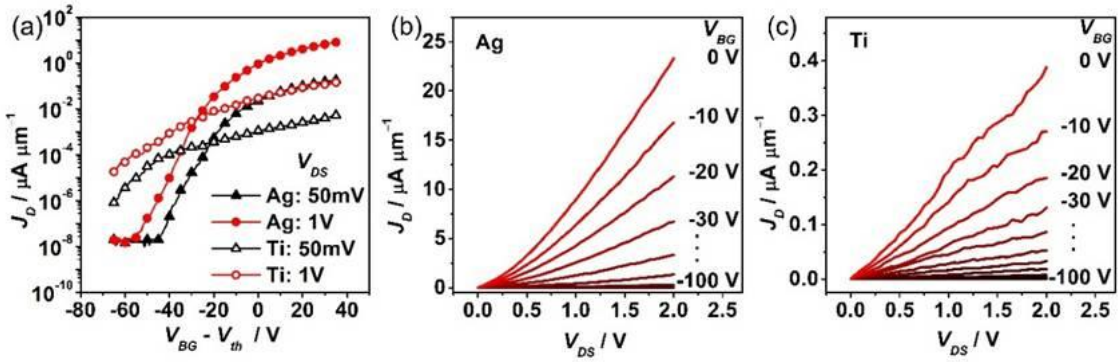

Figure 3.3 Drain current density of few-layer MoS_2 transistors versus (a) V_G-V_{th} with Ag or Ti contacts, and (b, c) drain voltage (V_D) with (b) Ag or (c) Ti contacts.

Figure 3.3(b) and (c) show J_D-V_{DS} characteristics of few-layer MoS_2 FETs with Ag and Ti contacts, respectively. Similar to monolayer MoS_2 FETs, a 60-time ON-state current enhancement is also shown in few-layer MoS_2 FETs with V_{BG} = 0 V and V_{DS} = 2 V.

As the contacting metal, Ag or Ti, is thick enough, the barrier height between MoS_2 and metal is dominated by the interaction between MoS_2 and the direct contact metal layer. Here, Ag and Ti have very similar work functions (4.26 eV for Ag and 4.33 eV for Ti). [72] Interestingly, theoretical simulations have shown that Ti is a better contact with WSe_2 than Ag, [66, 71] experimental results show that the devices with Ag contacts perform much better than those with Ti. [66] To gain a better understanding, we performed the surface and interface characterization on our metal contacts.

3.3.2 Surface Morphology of Metal Thin Films on MoS_2

To understand the performance difference, we deposited 5 nm Ag or 5 nm Ti on top of exfoliated MoS_2 followed by the deposition of 5 nm Au as protection layer. The conditions used are the same with device fabrication except that the deposition rate was kept at ≈ 0.2 Å/sec for the whole metal deposition process to mimic the device fabrication.

Then, SEM was carried out to characterize their surface morphology. From SEM images (**Figure 3.4**), the morphology of Au/Ag or Au/Ti films on MoS_2 is found to be significantly different. Figure 3.3(a) shows that the Au/Ag morphology on MoS_2 and on SiO_2/Si substrate is so distinct that MoS_2 area can be clearly identified. Au/Ag forms surprisingly a much smoother and denser film on MoS_2 than on SiO_2/Si. In contrast, with the appearance of pinholes, Au/Ti film shows quite similar morphology on both MoS_2 and SiO_2/Si (Figure 3.4(b)). Therefore, the location of monolayer MoS_2 is very difficult to identify, though we can still identify it through its edges.

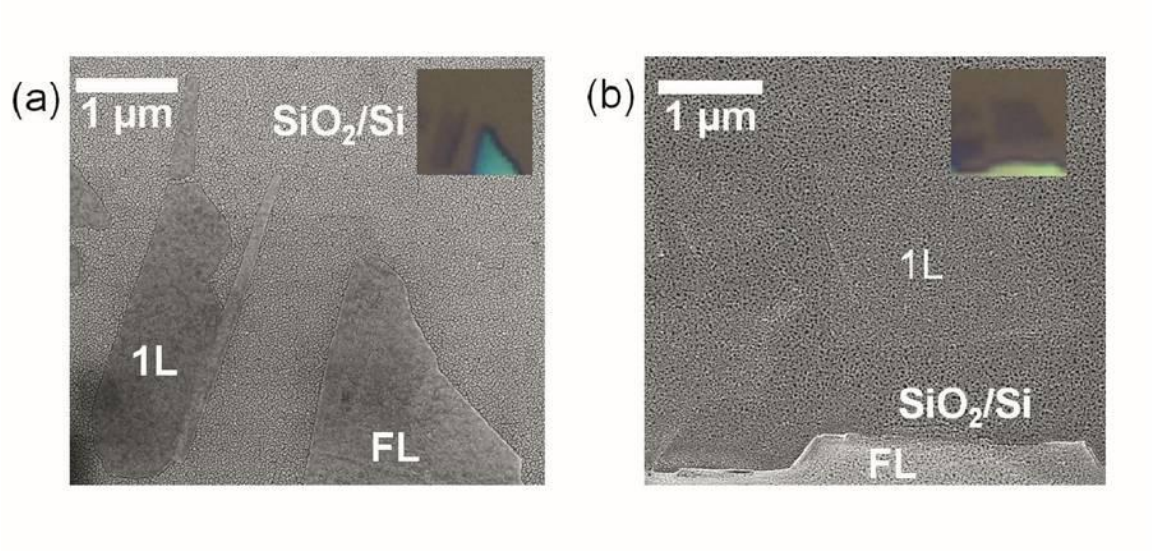

Figure 3.4 SEM images of MoS_2 on SiO_2/Si substrate after (a) Au / Ag deposition and (b) Au/Ti deposition. The insets show corresponding optical image of pristine MoS_2 before metal deposition. The locations of monolayer MoS_2 (1L) and few-layer MoS_2 (FL) are identified after metal deposition.

AFM was used to further analyze the surface roughness of the metal films. As seen in the AFM images (**Figure 3.5**), topography of the metals on MoS_2 and SiO_2/Si substrate exhibits significant difference. Au/Ag on MoS_2 is smoother than on SiO_2/Si (Figure 3.5(a)). A line profile shows that the surface of Au/Ag on monolayer MoS_2 is 0.54 nm lower than on SiO_2/Si on average (Figure 3.5(b)). Since the same amount of metal is deposited on the surface, a smoother and denser metal film (Au/Ag) on MoS_2 results in a thinner film than that on SiO_2/Si, even with the additional layer of MoS_2 underneath. The normalized height histograms of Au/Ag also show a narrower height distribution on MoS_2 than on SiO_2/Si (Figure 3.5(c)). The root mean squared (RMS) surface roughness is 0.37 nm on MoS_2, but 0.61 nm on SiO_2/Si. For Au/Ti, however,

pinholes are clearly seen on both MoS_2 and SiO_2/Si (Figure 3.5(d)). The surface of Au/Ti on MoS_2 is 2.18 nm higher than that on SiO_2/Si (Figure 3.5(e)). This is reasonable by considering the height of MoS_2 and its interfaces. The metal surface roughness is almost the same on MoS_2 and on SiO_2/Si (Figure 3.5(f)): RMS roughness is 1.08 nm and 1.09 nm on MoS_2 and on SiO_2/Si, respectively. Clearly, the Au/Ag film is much smoother than the Au/Ti film on MoS_2.

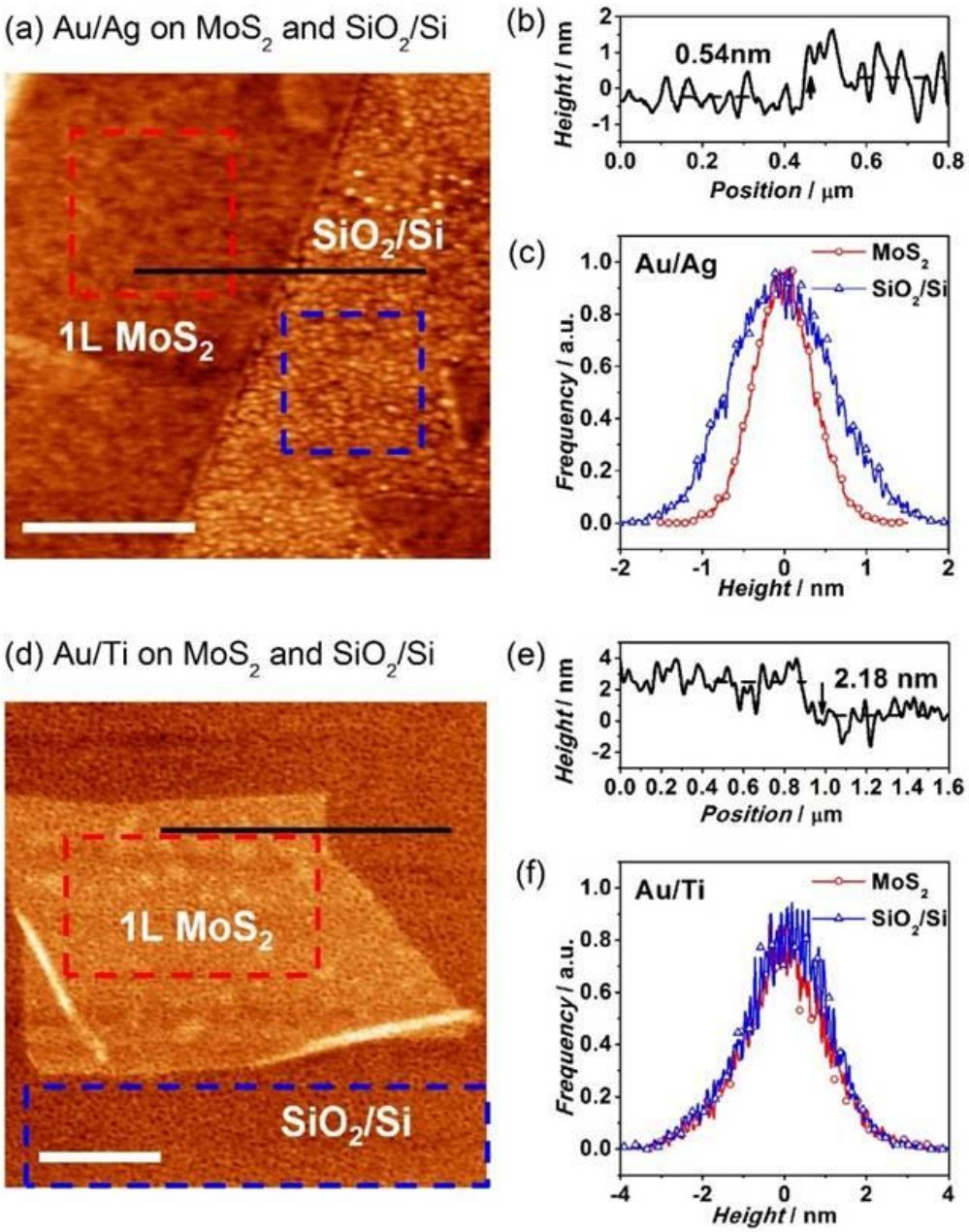

Figure3.5 AFM and roughness analysis of metal on MoS_2 and SiO_2/Si substrate: (a) Topography of Au/Ag on MoS_2 and SiO_2/Si. (b) A topographic line profile of the height along the slide line indicated in figure (a). (c) Normalized histograms of height distribution of areas indicated by the square in figure (a). (d) Topography of Au/Ti on MoS_2 and SiO_2/Si. (e) A topographic line profile of the height along the slide line indicated in figure (d). (f) Normalized histograms of height distribution of areas indicated by the square in figure (c). Scale bars are 500nm long for image (a) and (d).

3.3.3 Raman Spectroscopy of MoS_2 Covered with Metal

Recently, Raman spectroscopy has been used to investigate the effects of metal-MoS_2 interface on the electronic and phonon properties of MoS_2. [86] We carried out our Raman spectroscopy measurements on mono- and few-layer MoS_2 before and after deposition of the thin metal films (5 nm Au/5 nm Ag or 5 nm Au/5 nm Ti).

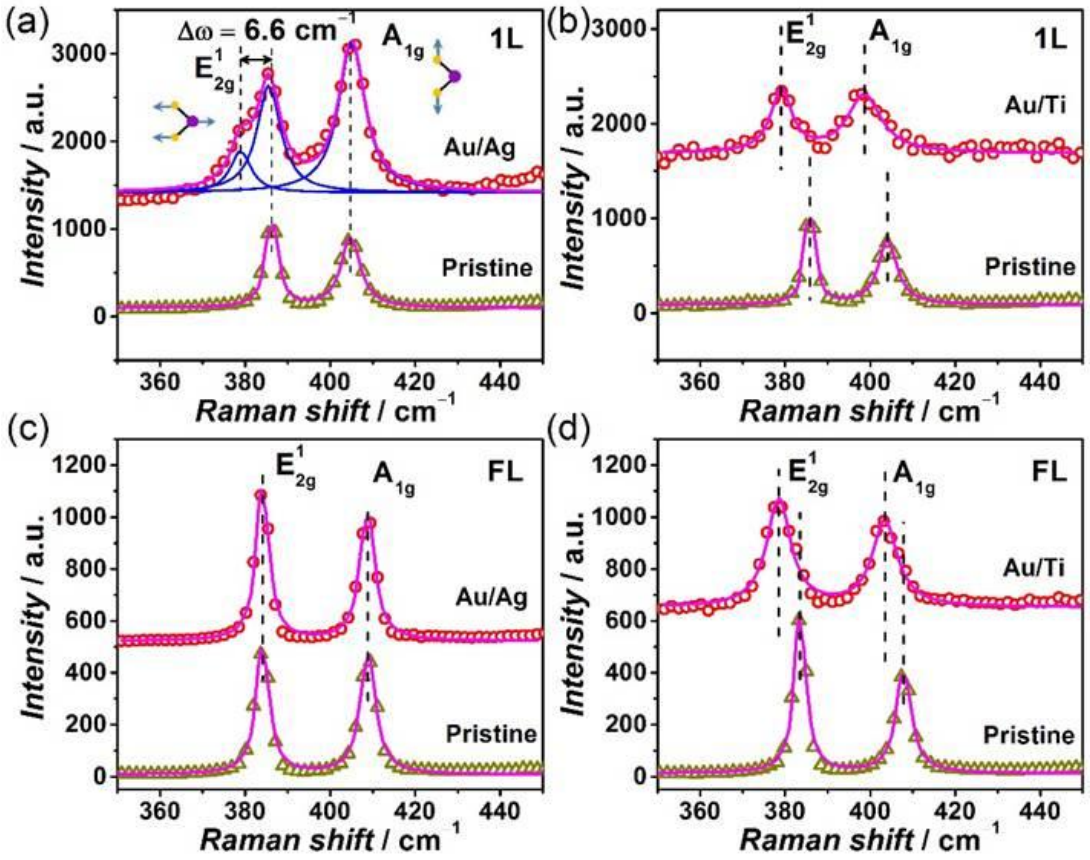

Figure3.6 Comparison of Raman spectra before and after (a) Au/Ag or (b) Au/Ti deposition on monolayer (1L) MoS_2 and before and after (c) Au/Ag or (d)Au/Ti deposition on few-layer (FL) MoS_2. The scatters are real data and solid lines are fitted Lorentz peaks.

Figure 3.6 shows the representative Raman spectra of MoS_2 before and after metal deposition. Before metal deposition, the Raman spectrum of the pristine MoS_2 shows E_{2g}^1 mode and A_{1g} mode peaks (Figure 3.6(a)). The E_{2g}^1 mode is the in-plane MoS_2 lattice vibration mode where the two sulfur layers move in the same direction collectively parallel to the lattice plane while the Mo moves in the opposite direction. These two peaks are symmetric and each is fitted well with a single Lorentz peak. And the A_{1g} mode represents the out-of-plane lattice vibration with the sulfur atoms on both sides of Mo atoms moving in the opposite directions vertical to the lattice plane while keeping Mo atoms in place. For pristine monolayer MoS_2, the Raman shift difference between these two peaks is 18.6 cm^{-1} for the Au/Ag sample and 18.3 cm^{-1} for the Au/Ti sample (Figure 3.6(a) and (b)). After Au/Ag deposition, there is no significant change in peak position for A_{1g} mode (Figure 3.6(a)). However, the E_{2g}^1 mode of MoS_2 splits into two peaks with a separation of 6.6 cm^{-1}. Also the higher frequency peak of E_{2g}^1 mode red shifts by 0.7 cm^{-1} compared to pristine monolayer MoS_2. The more significant effects of Au/Ag deposition on E_{2g}^1 mode indicate that the metal deposition affects the in-plane lattice vibration more than the out-of-plane. C. Gong *et al*. compared Raman spectra of monolayer MoS_2 with different metal depositions,[86] and their results show stronger effects on E_{2g}^1 mode than on A_{1g} mode by Au and Ag deposition. In Ag covered monolayer MoS_2, E_{2g}^1 peak splits into two peaks. The peak at higher frequency remains in the same position with the E_{2g}^1 peak of pristine MoS_2 and the other red-shifts by 6.38 cm^{-1}. [86] But, in their Au covered monolayer MoS_2, the E_{2g}^1 peak is broadened and red-

shifts with only 3.8 cm^{-1} peak split. [86] In our Au/Ag covered monolayer MoS_2, the E_{2g}^1 peak split is 6.6 cm^{-1} and the peak at high frequency red-shifts very little compared to the pristine monolayer MoS_2. This peak splitting is very similar to the Ag covered monolayer MoS_2 sample observed by C. Gong *et al*. [86] It indicates that in our sample, Au does not penetrate through Ag to make a direct contact with MoS_2 and Ag is indeed the contact metal.

After the deposition of Au/Ti film on monolayer MoS_2, both E_{2g}^1 and A_{1g} peaks red-shift and are broadened significantly (Figure 3.6(b)). However, each peak still remains symmetric and can be fitted with a single Lorentz peak. Even though there are pinholes in Au/Ti film on MoS_2, on the basis of the work by C. Gong *et al.*, [86] the absence of E_{2g}^1 peak splitting indicates that the contacting layer is Ti instead of Au.

We can now explain the dramatic topographic difference between Au/Ag and Au/Ti films on MoS_2. It is reasonable to correlate this difference with the roughness of the contact layer. Raman spectroscopy reveals that the contact layer with MoS_2 is Ag and Ti for Au/Ag and Au/Ti films, respectively. As a result, the smoother topography observed with the Au/Ag film indicates the smoother Ag contacting layer with MoS_2. Ag has exhibited a good wettability on bulk MoS_2. [67] Our results show that this good wettability is preserved on mono- and few-layer MoS_2 as well.

As we did not anneal our devices for the electrical measurements, the performance difference cannot be simply attributed to the chemical react between Ag and MoS_2 because previous work has shown that Ag does not react with MoS_2 at room

temperature. [87] Therefore, it is reasonable to believe that the MoS_2 FET performance is enhanced by the better contacting interface between Ag and MoS_2.

For the Au/Ag covered monolayer MoS_2, the in-plane E_{2g}^1 mode splits while the out-of-plane A_{1g} mode keeps its place. This change in Raman spectra after metal deposition is unlikely due to some vertical perturbations such as the pressure introduced by top metal and chemical bonds formed with metal atoms deposited on top. These vertical perturbations would affect out-of-plane A_{1g} mode more than E_{2g}^1 mode which is not complied with our results. The E_{2g}^1 peak splitting should be the result of the in-plane strain introduced by metal deposition. Previous studies [86, 88, 89] demonstrated the influence of uniaxial tensile strain on MoS_2 phonon modes. Their results showed that the out-of-plane A_{1g} mode was not shifted by strain while the in-plane E_{2g}^1 mode was split 4.5cm^{-1} by 1% strain. Therefore, we estimate that the Au/Ag film introduces 1.46% strain into our MoS_2 sample (6.6 cm^{-1} ÷ (4.5 cm^{-1}/1%) = 1.46%). In contrast to monolayer MoS_2, few-layer MoS_2 did not show such significant changes in the Raman spectrum after Au/Ag deposition (Figure 3.6(c)) and both peaks stay at almost same positions. A. Castellanos-Gomez *et al*. studied the localized uniaxial strain influences on the few-layer MoS_2 Raman spectra. [90] They found that in few-layer (3~5 layers) MoS_2, both E_{2g}^1 and A_{1g} modes red-shift with strain, whereas E_{2g}^1 mode shifts larger, about 1.7 cm^{-1} per 1% strain. The absence of the peak shift in our Au/Ag covered few-layer MoS_2 indicates that the tensile strain introduced by metal deposition might be thickness dependent.

On the monolayer MoS_2 after Au/Ti deposition, the E_{2g}^1 peak red-shifts by 6.7 cm^{-1}, and A_{1g} by 5.5 cm^{-1} (Figure 3.6(b)). The simultaneous peak shifts of E_{2g}^1 and A_{1g}modes clearly indicate the temperature increase in the samples during the Raman measurement. The Raman modes of monolayer MoS_2 affected by temperature have been investigated in the literature: Both E_{2g}^1 and A_{1g} peaks red-shift when temperature increases. [91-95] From the red-shifts of the both peaks in our samples, the temperature of Ag/Ti covered monolayer MoS_2 increased significantly during the Raman measurement. This heating effect was also observed in the Raman spectrum of few-layer MoS_2: the two peaks also red-shift simultaneously after Au/Ti film deposition (Figure 3.6(d)). The peak red-shifts are 5.0 cm^{-1} for E_{2g}^1 mode and 4.2 cm^{-1} for A_{1g} mode.

The temperature increase in Au/Ti coated MoS_2 is due to the laser heating during Raman measurement. To confirm this, we performed Raman measurements with different power and signal collection time on monolayer MoS_2 covered by thin layer Au/Ti (**Figure 3.7**). When the power is as low as 10% of the total laser power, and the signal collection time is 10 seconds, no significant peak shift was observed. However, as the laser power increases or signal collection time gets longer, the peak shift becomes more significant. This indicates that the peak shift is a result of the laser heating of the sample.

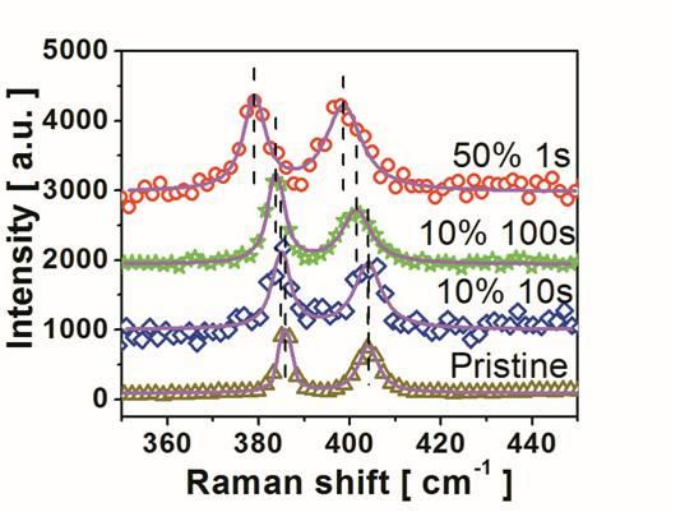

Figure 3. 7 Raman spectra on Au/Ti covered MoS_2 with different power and signal collection time. Scatters are experimental data and solid lines are fitted curves.

It is interesting to see that the heating effect is not seen in pristine and Au/Ag covered MoS_2. The dramatic difference of thermal conductivity between Ag and Ti could contribute to the difference in heating effect between Au/Ag covered MoS_2 samples and Au/Ti covered ones. At room temperature, the thermal conductivity of Ag is almost 20 times larger than Ti. [96] The higher thermal conductivity of Ag and the smoother and denser morphology of the Ag film enhance the heat dissipation efficiency. Therefore, the heating effect is weaker in Au/Ag covered MoS_2 samples. We also notice that the heating effect occurs on on mono- and few-layer MoS_2 covered with Au/Ti. On the thicker MoS_2, the heating effect is not significant. This phenomena probably is related to the strong photoluminescence from mono- and few-layer MoS_2 and its interaction with Ti under ambient conditions.

3.4 Conclusion

In summary, both monolayer and few-layer MoS_2 FETs with Ag source/drain contacts show 60-time larger on-state current and a steeper subthreshold slope than those with Ti contacts. SEM and AFM both show that the topography of Au/Ag film on MoS_2 is significantly smoother and denser than Au/Ti film. Raman spectroscopy revealed that the contact layers are Ag and Ti in these two cases. It is reasonable to conclude that the smoother and denser Ag contact leads to higher carrier transport efficiency, and is the main reason for the performance enhancement. Also, the high thermal conductivity can be a benefit for the heat dissipation during device operation. Considering that proper source/drain metal contacts are crucial for forming higher quality MoS_2 transistors, our result indicates that the metal/MoS_2 interface morphology is a crucial parameter to consider when optimizing electrical contacts.

CHAPTER 4: GATE EFFECTS AND CURRENT CROWDING IN METAL/MoS_2 CONTACTS

4.1 Introduction

Recently, mono- and multi-layer MoS_2 have attracted a lot of attention for future electronic and photonic applications. [10, 11] MoS_2 is a 2-dimensional (2D) semiconductor which has a bandgap ranging from 1.2 eV to 1.8 eV depending on its thickness. [14, 15, 27] In particular, monolayer MoS_2 with a direct bandgap of 1.8 eV shows promising electric and optoelectronic applications. [9, 50-54] In addition, considering short channel effects in metal-oxide-semiconductor field effect transistors (MOSFETs), the intrinsic ultrathin body of mono-layer MoS_2 also represents the ultimate in scaling. [56] The intrinsic ultrathin body and robust lattice structure in 2D MoS_2 are also attractive for flexible electronic applications.[19, 20, 55]

However, MoS_2 transistor performance remains a bottleneck for MoS_2 future applications. To improve MoS_2 transistor performance, the Source/Drain (S/D) contacts are very important factors to consider. A variety of contacts have been used and studied to achieve a good Ohmic contact on MoS_2. [37, 38, 55, 62-64, 71, 97] At beginning the research is focused more on the mechanism at the barrier in metal-MoS_2 interface. [37, 38, 62, 71, 97] Fermi level pinning in metal contacts makes the MoS_2 FETs mainly n-type. [37, 38] And the intrinsic defects in MoS_2 leads to significant variation in contact

behaviour even when same metal contacts are used. [62] Later the current distribution under the metal contacts is also considered. [70, 73] However, their results are based on back-gate devices where the channel current was not well tuned by the gate. Moreover, in bottom-gate MoS_2 transistors, the Fermi level of MoS_2 under the contacts is not screened from the gate bias by the metal which is not the case in top-gate transistors. Our previous work shows that gate-assisted test structure is a good approach to test the contacts in low-dimensional electric system. [74] In this article, we present our work on the current crowding effect in metal-MoS_2 contacts which is affected significantly by a top gate.

We fabricated Ag contacted bilayer MoS_2 transistors with 30 nm Al_2O_3 top gate on 300 nm SiO_2/Si substrate. The dimensions of our transistors are: 0.5 μm channel length, 4 μm channel width and 1 μm contact length. Ag was chosen because it has been reported to form a good contact on WSe_2,[66] which is a similar material to MoS_2. And our previous work shows Ag forms smooth and solid film on MoS_2 which makes the carrier transport efficiently across the contacts. Our devices show good n-type current-voltage (I-V) characteristics. Then gate assisted Kelvin structure and 4-probe method was used to analyze the contacts. The contact resistance extracted from the both methods is significantly different due to the difference in position where the voltage is sampled in both methods. By comparing the contact resistance extracted from both methods, we find the current transfer length (L_T) of Ag-contact MoS_2 transistors is 137 nm to 206 nm which increased with the increase of gate voltage. The channel sheet resistance is also measured by 4-probe method. It is much larger than the contact resistance which indicates that the MoS_2 transistors are channel-dominant. The contact resistivity is also

extracted from our data. It is effectively tuned by the gate as well. Our result shows that considering the contact resistance, the gate affects not only the contact resistivity but also the current crowding in the contacts.

4.2 Growth of MoS_2 and Device Fabrication

Our MoS_2 transistors were fabricated with chemical vapour deposited (CVD) MoS_2 on 285nm SiO_2/Si substrate. The CVD was performed with MoO_3 and sulfur as the precursor. About 5 mg MoO_3 was placed in an alumina crucible in the center a tube furnace. Then abundant amount (1~2 g) of sulphur in alumina crucible was allocated at the entrance of the furnace. And the 285 nm SiO_2/Si substrate was place 2 cm downstream to MoO_3. The furnace set-up was illustrated in Fig. 4.1(a). 100 sccm Ar was used as carrier gas and the pressure was kept at 800 Torr during the CVD. Before the heating process, the whole system was pumped to 200 mTorr and then flushed with Ar to achieve the set-up pressure. The pump-down and flush process was repeated 3 times and a stable pressure of 800 Torr was achieved before the heating process started. The heating process includes 30 minutes ramping up to 850 ℃ and a hold at 850 ℃ for 30 minutes. After heating, the tube furnace was naturally cooled down to below 200 ℃ before the samples were replaced from the furnace.

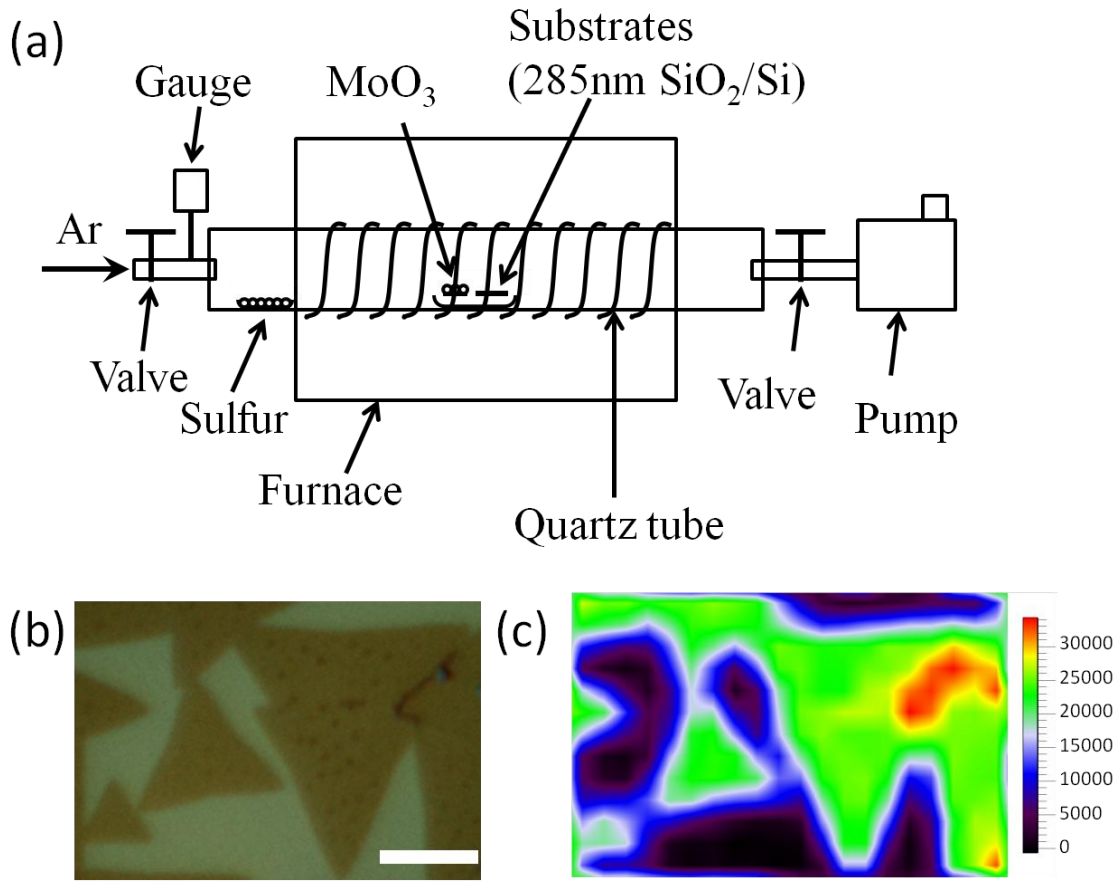

Figure 4. 1 (a) System set-up for MoS_2 CVD. (b) Image of typical MoS_2 flakes grown on SiO2/Si substrate. The scale bar is 5 µm. (c) Device schematic.

The resulting samples are MoS_2 flakes spreading over the 285 nm SiO_2/Si substrate. The MoS_2 flakes are typically triangular or hexagonal shaped. (Fig. 4.1(b)) The Raman mapping of the intensity of two representative peaks shown in Fig. 1(c) indicates the MoS_2 flake thickness is uniform. The Raman spectra of a representative point on the MoS_2 flakes shows the distance between the two major peaks is 21 cm^{-1}, indicating they are 2 layers in thickness. For the contact measurement, only Ag contacts are used. As discussed in Chapter 3, Ag is a much better material to form S/D contacts.

The MoS_2 flakes were allocated with a microscope and then conventional lithography process was used to define the devices. 50 nm Au/ 5nm Ag was used as the source/drain (S/D) contacts. 5 S/D contacts were parallel placed on a same triangle flake of MoS_2 so that contact test can be carried with these contacts later. The channel length of the transistors is 0.5 μm and the contact length is 1 μm. Then the rectangular channel was defined by O_2 plasma etching. 1 nm Al was deposited and then oxidized in air as seeding layer for atomic deposition (ALD) of 30 nm Al_2O_3 to promote the gate dielectric quality.[98] Al_2O_3 ALD was performed at 300 C with trimethylaluminum (TMA) and H_2O as precursor. Finally, 50 nm Au / 5 nm Ti was used as top gate electrode. The top gate covers the whole region where the 5 S/D contacts are placed so that the channels are common gated. The resulting device structure is illustrate in Fig. 4.2(a). Fig. 4.2(b) shows the scanning electron microscopic image of two adjacent channel with three contacts. The channel length and contact length are measured to be 370 nm and 1.09 μm respectively.

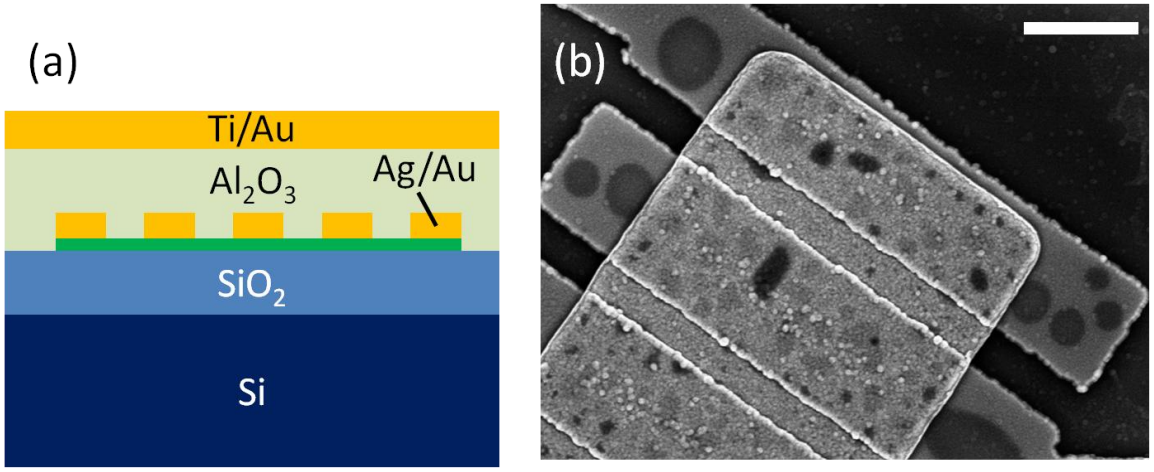

Figure 4.2 Device structure: (a) Schematics of MoS_2 FETs (b) SEM image of a MoS_2 transistor. Scale bar in this image is 1 μm.

4.3 Results and Discussion

The devices were then tested with a semiconductor parameter analyser (Hewlett-Packard® 4156) in a probe station (Cascade® summit semi-automated probe station) at room temperature.

The I-V characterization of a typical MoS_2 with 30 nm Al_2O_3 gate dielectric was shown in Fig. 2. The channel current is normalized to the current per 1 μm channel width. From Fig. 4.3(a), the transistor shows a strong n-type behaviour which is consistent with previous papers.[19, 37, 50, 55] In Fig. 4.3(b), the ON-current of our device is quite high compared to the devices in previous demonstrations. And the linear relationship between drain current (I_D) and applied drain voltage (V_D) at low voltage voltage indicates good S/D contacts for the transistors.

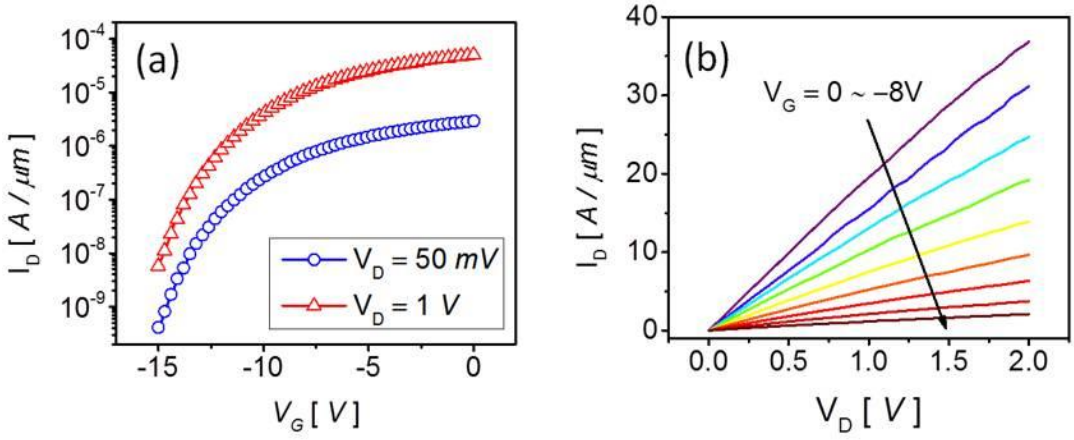

Figure 4.3 I-V characterization of a representative MoS_2 FET: (a) I_D-V_G, and (b) I_D-V_D characteristic.

To evaluate the metal contacts on MoS_2, gated assisted Kelvin test and 4-probe test were done on the MoS_2 transistors. Fig. 4.4 shows the result of the gate assisted Kelvin test. The measurement set-up is illustrated in the inset of Fig. 4.4(a). In Kelvin test structure, the current (I_D) is driven by a current source which is applied between source and drain contact, and the non-locate voltage (V_{23}) was read from the grounded source contact and an extra electrode which is connect to MoS_2 across another channel. Since a common gate is applied to our transistors, the both channel should be conducting simultaneously. As no current flows through the extra contact, the voltage on it should be equal to the voltage on MoS_2 at the end of source contact. So V_{23} is the voltage drop on the end of MoS_2 under the contact on source electrode. V_{23} versus I_D at different gate voltage is shown in Fig. 4.4(a). The linear relationship between V_{23} and I_D indicates an Ohmic contact. The overlap of the V_{23} curve at different V_G shows the contact resistance extracted by Kelvin test method ($R_{C\text{-}K}$) is not strongly affected by V_G. Figure 4.4(b) shows

the $R_{C\text{-}K}$ which is extracted from the linear fitting of V_{23} on I_D. The value of $R_{C\text{-}K}$ is slightly larger than 20 Ω, which is much lower than the contact resistance extracted from other methods in previous publications. [70, 73, 97]

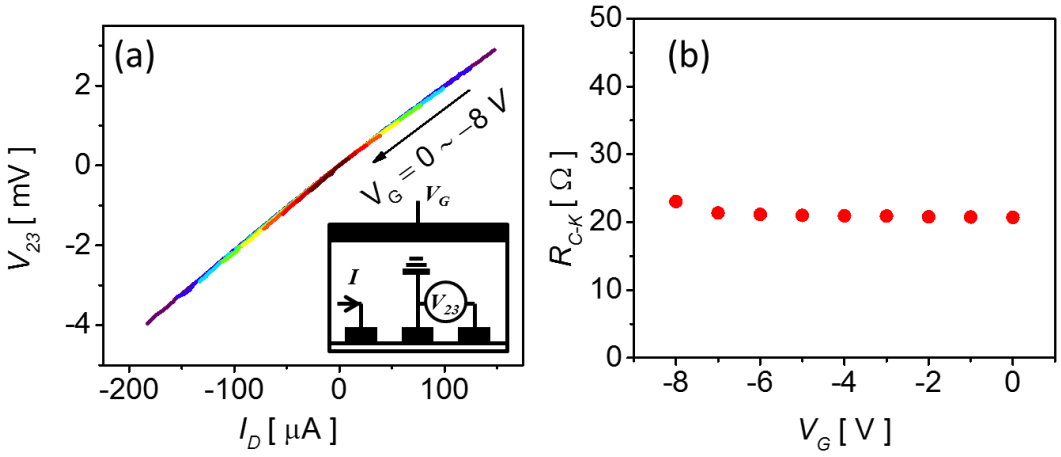

Figure 4.4 Gate assisted Kelvin test: (a) V_{23}-I_D measured at different V_G, inset is the illustration of the measurement set-up; (b) $R_{C\text{-}K}$ extracted from the linear fitting of V_{23} and I_D at different V_G.

Then a 4-probe measurement was done to extract the contact resistance and further understand the contact behaviour. The measurement set-up is shown in inset of Fig. 4.5(a). A voltage source was connected to the S/D contacts at the ends to drive the current through the channel under the gate voltage varying from -5 V to 0 V. The I_D and the voltage difference between two middle contacts is measured at the same time so that the channel sheet resistance can be extracted by the linear fitting of voltage drop between two middle contacts and I_D in linear region. The contact resistance (R_C) can be evaluated

by subtracting the channel resistance (R_{ch}) from the total resistance (R_{tot}), which can be expressed as:

$$R_c = \frac{1}{2}(R_{tot} - R_{ch}). \tag{4.1}$$

Here, the channel resistance is estimated from the channel sheet resistance.

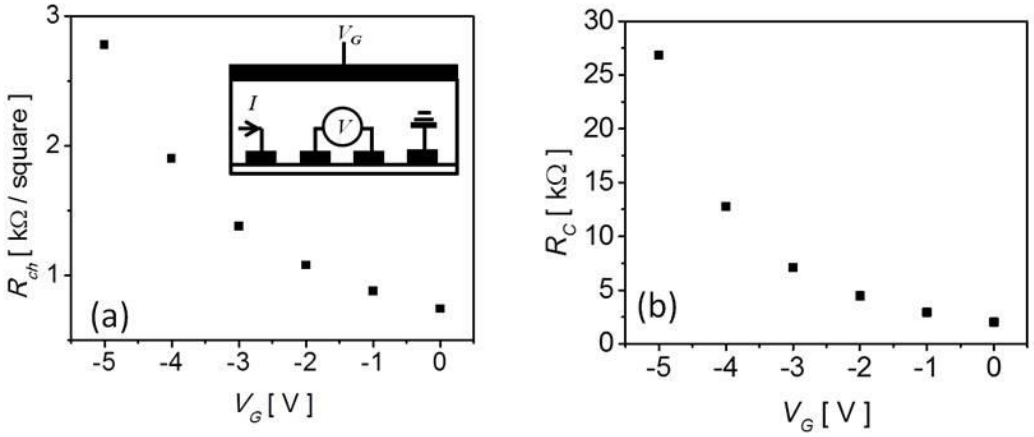

Figure 4.5 Gate assisted 4-probe measurement. (a) Channel sheet resistance at different V_G, inset is the measurement set-up for gate assisted 4-probe measurement. (b) Contact resistance (R_C) extracted from 4-probe measurement.

Fig. 4.5 shows that both the channel sheet resistance and contact resistance changes with gate voltage. As shown in Fig. 4.5(a), the channel conductance is effectively tuned by the gate, which is expected. As shown in Fig 4.5(b), it is interesting that the contact resistance is also affected by the gate. Compared to channel resistance, the contact resistance is much lower in our transistors. This indicates that the channel properties dominate our MoS_2 transistor performance.

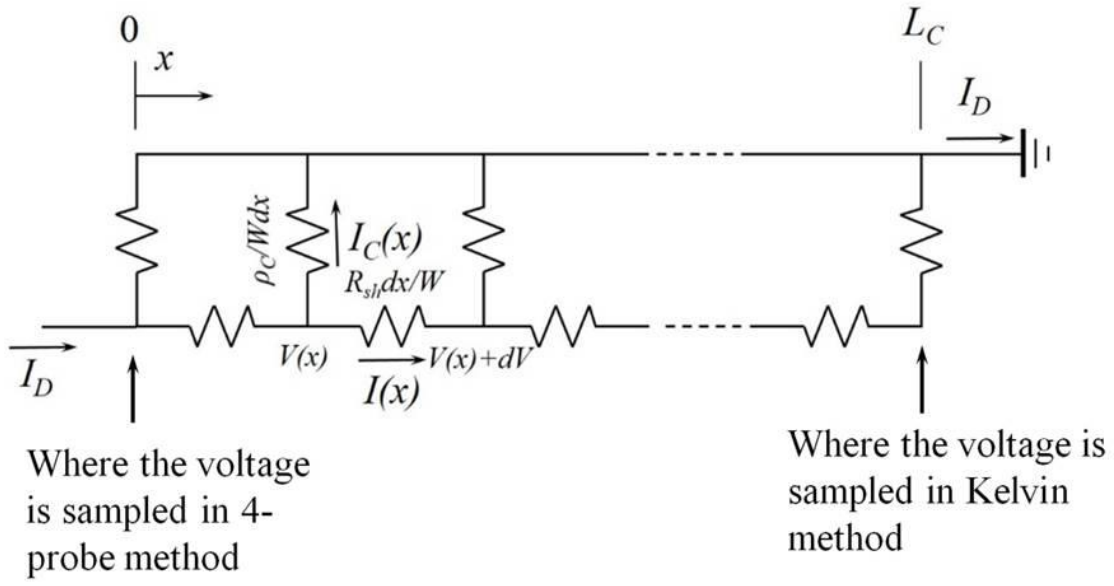

Figure 4.6 TLM model for contact resistance. The positions where the voltage is sampled in Kelvin method and 4-probe measurement are pointed.

Furthermore, compared to $R_{C\text{-}K}$, R_C is much larger and changes with the gate voltage. This difference is due to the difference in position where the voltage is sampled in these two contact characterization method. According to transmission line model (TLM, illustrated in Fig. 4.6), the current ($I(x)$) and voltage ($V(x)$) at position x have the relation as: [46, 75, 79, 99]

$$-dI(x) = I_C(x) = \frac{WV(x)dx}{\rho_C} \tag{4.2}$$

$$\frac{R_{Sh}dx}{W} I(x) = -dV(x) \tag{4.3}$$

where R_{sh} is the sheet resistance of the semiconductor under the contact, and $I_C(x)$ is the current transport from the semiconductor to the contact at position x, W is the contact width, and L_C is the contact length.

Substitute eq. (4.2) into Eq. (4.3), we get,

$$\frac{\rho_C}{R_{sh}} d^2I(x)/dx^2 = I(x) \tag{4.4}$$

Let $L_T = \sqrt{\rho_C/R_{sh}}$, L_T is the current transfer length in the contact, then we can solve Eq. (4.4), and get,

$$I(x) = Ae^{x/L_T} + Be^{-x/L_T} \tag{4.5}$$

At the boundaries of $x = 0$ and $x = L_C$, we have the current $I(0)$ and $I(L_C)$ which are:

$$I(0) = I_D \tag{4.6}$$

$$I(L_C) = 0 \tag{4.7}$$

So the expression for current at position x is,

$$I(x) = I_D \frac{sinh\,[(L_C - x)/L_T]}{sinh\,(L_C/L_T)} \tag{4.8}$$

Then we can get the voltage at position x as,

$$V(x) = -\frac{\frac{\rho_C}{W} dI(x)}{dx} = \frac{\sqrt{\rho_C R_{sh}}\,cosh\,((L_C - x)/L_T)}{W sinh(L_C/L_T)} I_D \tag{4.9}$$

In Kelvin test structure, the voltage on the contact is sampled at the end of the contact, so,

$$R_{C-K} = \frac{V(L_C)}{I_D} = \frac{\sqrt{\rho_C R_{sh}}}{W sinh(L_C/L_T)}. \quad (4.10)$$

However, in 4-probe method, the voltage on the contact is sampled in the front of the contact, so,

$$R_C = \frac{V(0)}{I_D} = \frac{\sqrt{\rho_C R_{sh}} cosh\,(L_C/L_T)}{W sinh\,(L_C/L_T)}, \quad (4.11)$$

It is clear that the ratio of R_C to $R_{C\text{-}K}$ can be expressed as:

$$\frac{R_C}{R_{C-K}} = cosh\,(L_C/L_T). \quad (4.12)$$

So, compare the contact resistance we got from both methods, we can extracted L_T in our devices. The result is shown in Fig. 4.7(a). It is clear that the transfer length is also affected by the gate voltage. The value increases from 138 nm when V_G equals to -5 V to 206 nm when V_G equals to 0 V. These values are consistent with the previous work. [73] It is clear that the L_C is much longer than L_T in our devices. The voltage drops as long as the current is concentrated at the front part of the contact. The R_C can be approximately expressed as:

$$R_C \approx \frac{\sqrt{\rho_C R_{sh}}}{W} = \frac{\rho_C}{W L_T}. \quad (4.13)$$

So the contact resistivity ρ_C can be extracted. As shown in Fig. 4.7(b), it decreased with the increase of gate voltage. As the contact resistivity is concerned with the barrier between MoS_2 and the metal, the gate voltage also modulate the barrier at the contact.

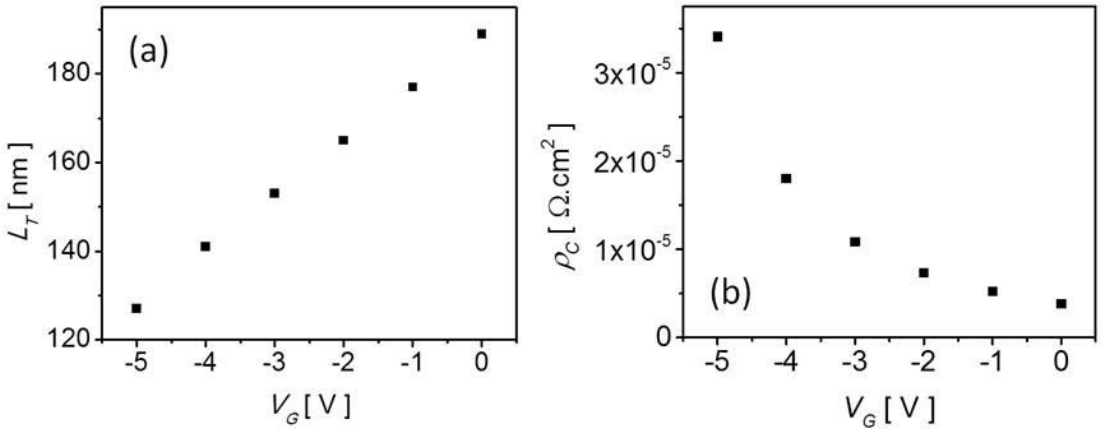

Figure 4.7 (a) Current transfer length and (b) Contact resistivity at different V_G.

In general, the gate has strong effects on contact resistance of MoS_2 transistors. The transfer length increases and contact resistivity decreases when gate voltage increases, so that the contact resistance decreases as a result.

4.4 Conclusion

In summary, n-type MoS_2 FETs were fabricated with a conventional lithography process. All MoS_2 transistors show good I-V characterizations. The contacts of the MoS_2 transistors were then analyzed with gate assisted contact measurement including Kelvin structure and 4-probe methods. The contact resistance extracted from these two methods is significantly different. According to TLM model, this difference is due to the current crowding and the difference in positions where the voltage is sampled in both methods. The current transfer length is extracted based on the ratio of the contact resistance extracted from these two methods. Transfer length increases with the increase of the gate

voltage. Channel resistance which is measured by the 4-probe method is much larger than the contact resistance. It indicates that our MoS_2 transistors are channel dominant devices. Our result also shows that the gate also tunes the contact resistivity which decreases with the increase of the gate voltage. So the whole contact resistance decreases by the increase of current transfer length and the decrease of contact resistivity when the gate voltage increases.

CHAPTER 5: SUMMARY AND PROSPECTIV FUTURE PLAN

5.1 Summary of the Dissertation

In this dissertation, my study on metal contacts on low-dimensional materials has been presented, with a focus on metal contacts on SiNW and MoS_2.

First, the metal contact on SiNW field effect transistors (FETs) was studied with a gate assisted Kelvin structure. SiNW is an example of one-dimensional semiconductor. In this work, I fabricated ambipolar SiNW FETs with Al contacts. The ambipolar behavior of the SiNW FETs and the gate assisted Kelvin structure enabled the measurement of contact properties of electron- and hole-flow at the same contact. We found that the contact performance is significantly affected by the type of carriers that flow in the channel as well as the current direction. Also, an inverter was obtained on a single SiNW.

Then, metal contacts on MoS_2, which is a two-dimensional semiconductor, are studied. In the first part of this work, Ag and Ti contacts on exfoliated MoS_2 flakes are compared. Based on the current-voltage (I-V) measurement, surface morphology and Raman spectroscope, we found that interface morphology plays an important role on the contact performance in MoS_2 FETs. In the second part of this work, gated assisted contact measurement was carried out on chemical vapor deposited MoS_2. The contact resistance and current crowding were analyzed under different gate bias. All these

findings contribute to understanding the properties and mechanism of metal contact on MoS_2.

5.2 Prospective Future Plan

SiNWs and MoS_2 are good examples of emerging low-dimensional materials. The gate assisted contact measurement can also be applied on other emerging materials to characterize the contacts in electronic devices, to understand the mechanism in such contacts and to reduce contact resistance. As the devices are further scaled down, the issues of metal contacts in the electronic devices are increasingly important. It is important to study the mechanism of the metal contacts on low-dimensional materials.

Furthermore, my work will expand to all aspects of the contacts on the low-dimensional materials. For MoS_2 and other 2D semiconductors (e.g., h-BN and black phosphorus), the details in the contact performance such as the band alignment and the evolution of the band bending under sufficient bias have not been much explored. I will continue the work on the characterization of metal contacts, and try to develop deeper understanding of the modeling of the contacts. I hope my work will lead to understanding the contact mechanism and finding the way to reduce contact resistance or maintain low contact resistance for low-dimensional materials.

Also, I plan to apply the knowledge from my current research to new materials. Black phosphorus, for example, is a good platform to investigate the contacts as well. It attracts quite a lot of attention for the electronic applications for better carrier mobility. I

would like focus on this research and help to enhance the device performance by reducing the contact resistance.

Moreover, because Fermi level pinning not only increases the contact resistance but also decreases the barrier which is needed in photovoltaic and solar cell devices. The Fermi level pinning makes it difficult to form a high barrier between different contacts. In order to improve the efficiency of the photovoltaic devices, it will be equally important to find a way to maintain good energy barriers.

APPENDIX: POLARIZATION OF BI2TE3 THIN FILM IN A FLOATING-GATE CAPACITOR STRUCTURE

A.1 Introduction

Topological insulators (TIs) are materials that have an insulator (or semiconductor) bulk and gapless surfaces which are protected by time reversal symmetry.[100] These materials have a Dirac cone at the surface that can be detected by angle resolved photo emission spectroscope (ARPES).[101, 102] The electrons at the TI surface can be considered as massless Dirac fermions.[103, 104] Therefore, carriers in these surface states have fast response and high mobility.[105] The robustness of the TI surface states is protected by time reversal symmetry and is resistant to external perturbations such as defects and electric field.[106]

Several groups have recently reported the surfaces state analysis and the magneto-electric effects of the TI materials.[107-110] They found that different quantum states can coexist in the surface and can be changed by external magnetic field which breaks the time reversal symmetry. However, these studies were mostly based on theoretical approach, delicate surface characterization method (e.g. ARPES) or scanning tunneling microscopy (STM). There is limited progress in the study of device applications. It would be very important and interesting to study how the TI materials behave in a device structure. We have previously reported a study of high-performance TI nanowire field

effect transistor (FET) in which the TI materials acted as a conducting medium.[111] FETs based on topological crystalline insulator SnTe thin film have also been recently demonstrated.[112] However, the study of floating-gate structure in which TI materials are surrounded by dielectric has not yet been reported. It would be very interesting to see how the TI materials behave with a vertical electric field across them, as well as how they act as an information storage medium.

Information storage is of great interest in microelectronics. It is well recognized that the future information technology relies on novel electrically accessible non-volatile memory (NVM) with high speed and high density.[33] There are several NVM candidates, including ferroelectric NVM, charge-storage memory (e.g., flash memory), molecular memory and resistance random-access memory (RRAM).[113-116] Among them, ferroelectric NVM is very attractive for its low power consumption, fast write / erase and good endurance.[11] However, the conventional perovskite ferroelectric materials are disadvantageous for low storage density and high integration cost.[117, 118]

In this work, we fabricated Metal-Oxide-Semiconductor (MOS) capacitors with a Bi_2Te_3 thin film sandwiched by two oxide layers. The Bi_2Te_3 film acts as a "floating gate" similar to the poly-Si floating gate in a FLASH memory. We have studied the polarization of the Bi_2Te_3 thin film for memory application. Such a hybrid MOS structure is very interesting for information storage and can also provide a good platform to study the properties of TI materials.

A.2. Experimental

The schematic of the MOS capacitor structure is shown in Fig. A.1(a). The Bi_2Te_3 film was inserted in between the SiO_2 and Al_2O_3, forming a metal/Al_2O_3/Bi_2Te_3/SiO_2/Si (MABOS) capacitor structure. The substrate is low doped (doping concentration about10^{15} cm^{-3}) n-type Si wafers with 300 nm thermally grown SiO_2. The fabrication of these MABOS capacitors followed a conventional photolithographic procedure. First, an active area (100 μm × 100 μm, 50 μm × 50 μm, 25 μm × 25 μm or 10 μm × 10 μm) was defined and etched through a layer of 300 nm SiO_2 thermally grown on n-Si wafers. The wafers were then oxidized at 900˚C for 22 minutes to achieve 11 nm dry SiO_2. The dry oxide is thinned down to 6 nm by 2% HF etch for 60 seconds. Then, atomic layer deposition (ALD) was used to deposit 30 nm Bi_2Te_3 and 30 nm Al_2O_3 on the samples followed by the formation of top Al gate. The extra Bi_2Te_3, Al_2O_3, and Al top gate beyond the active region were removed by ion mill before electrical measurement. Finally, the samples were annealed at 300 ˚C in Ar by using rapid thermal annealing (RTA).

The detail ALD conditions for Bi_2Te_3 and Al_2O_3 are as following. The Bi_2Te_3 thin films were synthesized using bismuth trichloride ($BiCl_3$) and (trimethylsilyl) telluride ($(Me_3Si)_2Te$) as chemical ALD precursors. The growth temperature was 170 ^oC. The $BiCl_3$ precursor was volatilized at a temperature of 140 ^oC and the Te precursor was heated at 45 ^oC. Furthermore 10 sccm of N_2 was used as a carrier gas flow for the precursors. The ALD reaction chamber base pressure was kept at 40 mTorr. The deposition of Al_2O_3 thin film followed a conventional ALD procedure which uses

trimethylaluminum (TMA, $Al(CH_3)_3$) and O_2 plasma as precursors. The growth temperature was 300 ^oC. N_2 was also used as a carrier gas and the ALD reaction chamber base pressure was kept at 20 mTorr.

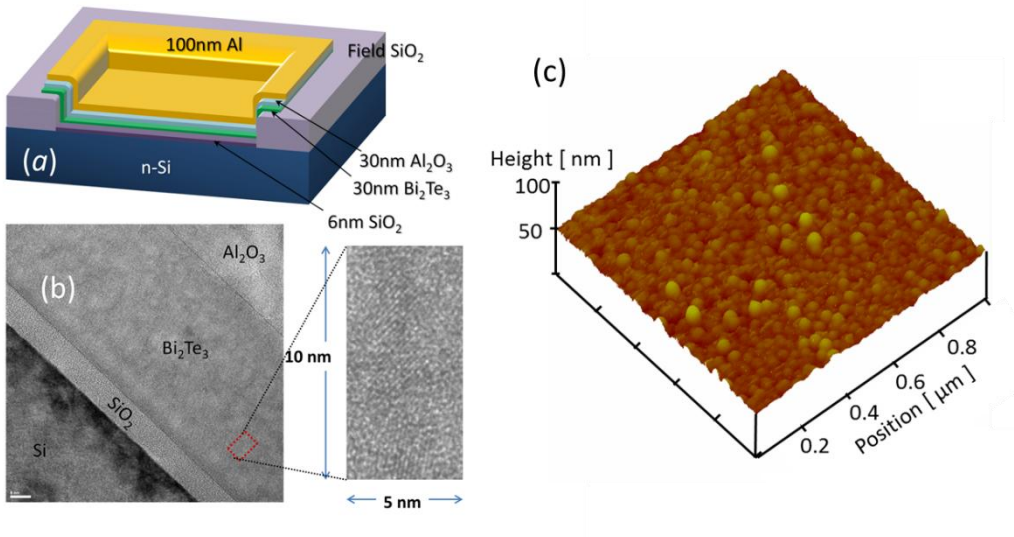

Figure A.1 (a) Schematic of the capacitor with $Al/Al_2O_3/Bi_2Te_3/SiO_2/Si$ structure. (b) High-resolution transmission electron microscopy (HRTEM) image of the capacitor cross-section. The scale bar is 5 nm in the image. The rectangular HRTEM image (10nm × 5nm) on the right is an amplification of the Bi_2Te_3 film within the red rectangle on the left image, showing the polycrystalline structure in the film. (c) AFM image of Bi_2Te_3 film grown on SiO_2 with OH-hydroxyl groups by ALD.

The resulting devices were first characterized with the transmission electron microscope (TEM) image of the MOS capacitor cross-section is shown in Fig. A.1(b), indicating that the Bi_2Te_3 is poly-crystalline. Atomic force microscopic (AFM) image of the Bi_2Te_3 film grown by ALD on SiO_2 is shown in Fig. A.1(c). It clear shows that the Bi_2Te_3 is poly-crystalline and the film is uniform with a smooth surface. The whole

process we used is compatible with complementary metal-oxide-semiconductor (CMOS) protocol, which provides a smooth transition to the application in microelectronics.

Capacitance-voltage (C-V) characterization was carried out by using an impedance analyzer and a vacuum probe station. During the measurement, the samples were kept in 4×10^{-7} Torr vacuum.

A.3 Results and discussion

Fig. A. 2 shows the C-V characteristics of MABOS capacitors with an area of 100 $\mu m \times 100\ \mu m$. The C-V measurement was carried out at 1 MHz. These capacitors exhibit a hysteresis in C-V characteristics at room temperature. The hysteresis has a same direction of ferroelectric base capacitors.[119, 120] As shown in Fig. A.2(a), the flat-band voltage (V_{FB}) of the C-V curve shifted to positive as the gate voltage was scanned from negative to positive. The hysteresis is larger when a larger range of gate voltage was scanned. But the hysteresis did not disappear even during a low voltage scan. The same hysteresis also shows in the MABOS capacitors with smaller area.

The hysteresis of MABOS capacitors is different from the hysteresis of a floating-gate memory cell. First, this hysteresis shift is opposite to that of a floating-gate memory device based on charge-trapping mechanism.[121, 122] As shown in insect of Fig. A.2(a), in a floating-gate memory cell, positive charges (holes) will tunnel from Si into the floating gate after gate voltage sweeps from negative to positive, resulting in V_{FB} shift to negative. Second, the hysteresis of MABOS capacitors exists in all sweep ranges, even in a small voltage sweep range from -3V to 3V. This is different from the charge-trapping

devices of which the hysteresis is present only when gate voltage exceeds tunneling threshold voltage.[121, 123]

In these MABOS capacitor devices, 6nm SiO_2 is thick enough to prevent the electron/hole tunneling between the Bi_2Te_3 and Si at such a low electric field. Even in the worst case that a small amount of charges tunnel through the 6nm SiO_2, the hysteresis shift should be in the opposite direction as mentioned above. Also, the Al_2O_3 layer is about 30nm, thick enough to block the charge transfer between Bi_2Te_3 and the gate metal. Therefore, the hysteresis shift must be resulted by the polarization of Bi_2Te_3 film. In detail, the polarization is a result of charge accumulation on the two surfaces of Bi_2Te_3: the electrons and holes within the Bi_2Te_3 film are separated and driven by the electric field; and then, they are accumulated on either surfaces of the Bi_2Te_3 film, building an internal electrical field in the opposite direction to the external electrical field. This is quite similar to the polarization of metals and semiconductors in an electrical field.

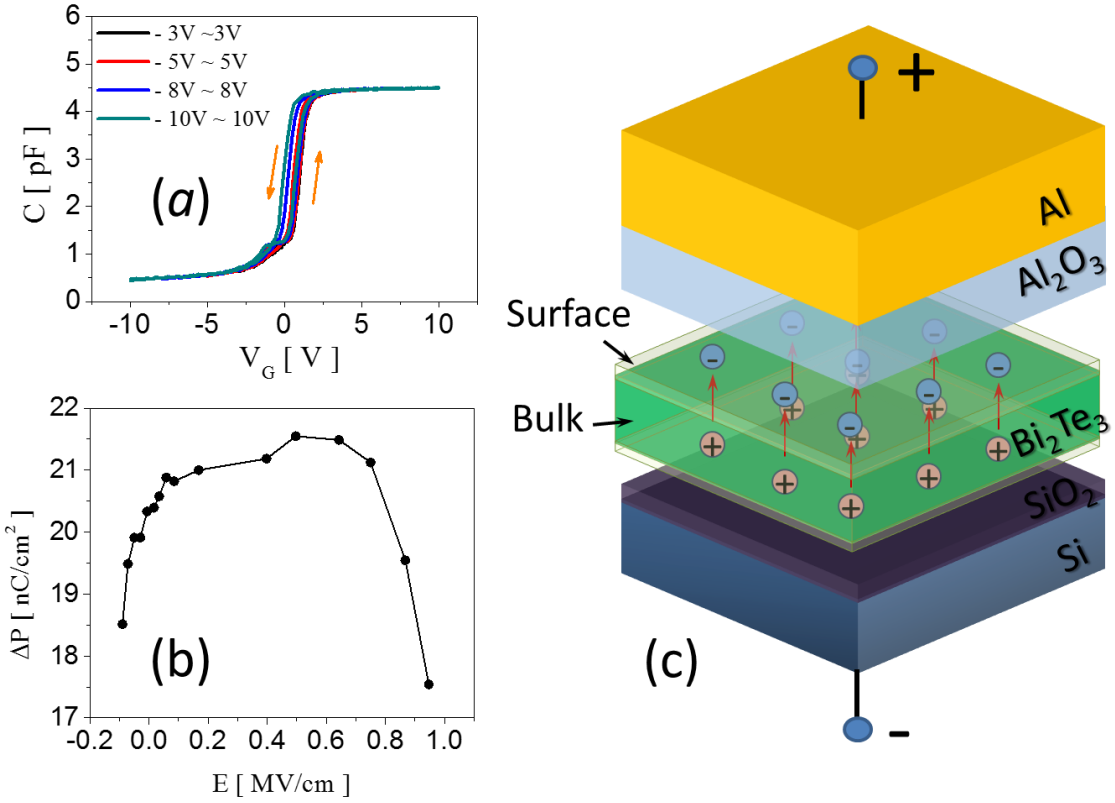

Figure A.2 (a) Capacitance-Voltage (C-V) characteristics of the Bi_2Te_3 capacitor structure at 1 MHz with different voltage sweep ranges. The area of the capacitor is 100 μm × 100 μm. (b) The polarization difference changes versus the applied voltage. (c) Illustration of the charge separation and polarization of Bi_2Te_3 when an external field is applied.

The movement of carriers is much faster than the displacement of atoms/ions in the ferroelectric materials. The polarization shown in the C-V hysteresis is a result of accumulation of charge carriers on the surfaces. Unlike ferroelectrics where the polarization is due to the displacement of ions in the crystal, the polarization of Bi_2Te_3 film is induced by the accumulation of carriers (electrons and holes). Therefore, the polarization of the Bi_2Te_3 film in the MABOS structure should be much faster than that of normal ferroelectric films. Also, compared to the ion displacement in conventional

ferroelectric materials, the electron movement should have less damage on the materials, leading to better device endurance.

To extract the polarization of Bi_2Te_3, we estimated the capacitance of dielectric layers based on the conventional model of MOS capacitor at high frequency. We can consider the polarized Bi_2Te_3 as a parallel-plate capacitor with opposite polarized carriers (electrons or holes) on each surface. So, the capacitance of insulating layers can be obtained from the capacitance in accumulation region ($100\ \mu m \times 100\ \mu m$ capacitors), that is:

$$C_{INS} = 4.6\,pF \tag{A.1}$$

Because the capacitance was measured with a small signal method, the transient polarized charges do not contribute to the total capacitance. However, this charge separation (or polarization) shift V_{FB} of the MABOS capacitor to negative or positive directions so that the hysteresis in the C-V measurement appears. The value of the applied gate voltages at the same capacitance in forward and reverse sweep directions can be obtained. As discussed above, the difference between these two gate voltage values (ΔV_G) is due to the difference in polarization (ΔP) of Bi_2Te_3 between the two sweep directions. Their relationship can be expressed as:

$$\Delta V_G = \frac{\Delta Q_P}{C_{Bi2Te3}} = \frac{\Delta P \cdot A}{C_{Bi2Te3}}, \tag{A.2}$$

Here, ΔQ_P stands for the polarized charge difference, A for area of the capacitor, and the capacitance of Bi_2Te_3 (C_{Bi2Te3} = 6.07pF) is calculated from the total insulator

capacitance which is assumed to be the total capacitance of SiO_2, Bi_2Te_3 and Al_2O_3 in serial.

Fig. A.2(b) shows the ΔP at different electric field. To calculate the electric field, a standard MOS capacitor with the same insulating layer capacitance (the capacitances of Al_2O_3, Bi_2Te_3 and SiO_2 in series, ≈ 4.6 pF) and doping concentration (1×10^{15} cm^{-3}) as the measured capacitors was designed for simulation. The applied voltage of the standard MOS capacitor is recorded at the same value of capacitance measured in the experiment. This recorded voltage is over flat band voltage, i.e. gate voltage (V_G) - flat band voltage (V_{FB}). The net voltage drop across Bi_2Te_3, V_{BT}, which is partial of ($V_G - V_{FB}$), can be extracted from the serial capacitor model. The electric field is V_{BT} divided by the thickness of Bi_2Te_3. We extract the ΔP in depletion-accumulation transition region when the capacitance changes dramatic with applied voltage. In the depletion or accumulation region the capacitance changes little with the applied voltage, the extraction of the ΔP would be inaccurate. The result indicates that the ΔP is largest around the flat-band voltage when the when the voltage drop across Bi_2Te_3 is small..

The memory window ΔV_{FB} is the ΔV_G when the capacitance is equal to the flat band capacitance (C_{FB}). C_{FB} can be expressed as:[124]

$$C_{FB} = \frac{C_{SFB}.C_{INS}}{C_{SFB} + C_{INS}} = 2.92\,pF \tag{A.3a}$$

$$C_{SFB} = \frac{\varepsilon_S \varepsilon_0 A}{\lambda_n} = A\sqrt{\frac{q^2 N_D \varepsilon_S \varepsilon_0}{kT}} = 8\times10^{-12}F \tag{A.3b}$$

where the flat-band condition capacitance of Si (C_{SFB}) is the capacitance of Si (C_S) at flat-band condition, λ_n is the depletion width in Si at flat-band condition, A is the area of the capacitor, N_D is the doping concentration (10^{15} cm^{-3} in our Si wafer), ε_S and ε_0 are Si relative permittivity and vacuum permittivity, respectively.

We have also performed temperature-dependent C-V characterization to study the polarization formation. The sample was measured at temperatures from 80K to 290K. As shown in Fig. A.3, the hysteresis decreases as the temperature decreases. Below 250K, the hysteresis is very small, almost negligible (Fig. A.3(d)). At each temperature, the C-V curves measured at different frequencies are approximately the same. Also, the hysteresis of the C-V curves at different frequencies is the same. This indicates that there is negligible frequency-dependence in the C-V measurement when frequency $\leq$ 1 MHz. In addition, the devices have been repeatedly tested for many times over a long period of duration (> 6 months). The measured results are very reproducible in all these tests. The devices exhibit better programming/erasing characteristics than conventional poly-Si Flash memory (1×10^6 cycles). This is because the polarization of surface state in Bi_2Te_3 causes much less damage than hot-electron injection in conventional Flash memory cells.

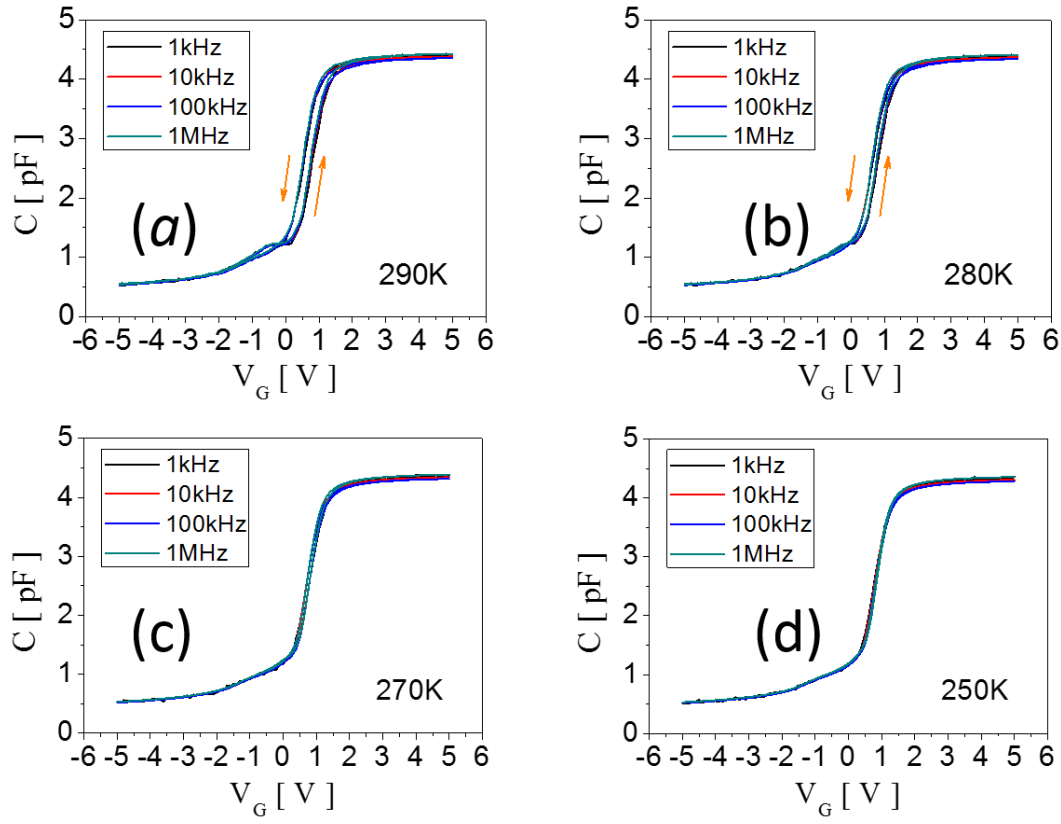

Figure A.3 C-V characteristics the Bi_2Te_3 capacitor structure at different frequencies (1 kHz to 1 MHz) at different temperatures: (a) 290K, (b) 280K, (c) 270K and (d) 250K. The hysteresis shift decreases as the temperature decreases.

Fig. A.4(a) showed that ΔP changes with electric field at different temperatures. The ΔP is eliminated when the temperature decreases. But the largest value of ΔP always shows around flat-band voltage. Fig A.4(b) shows the memory window (ΔV_{FB}) changes versus the temperature.

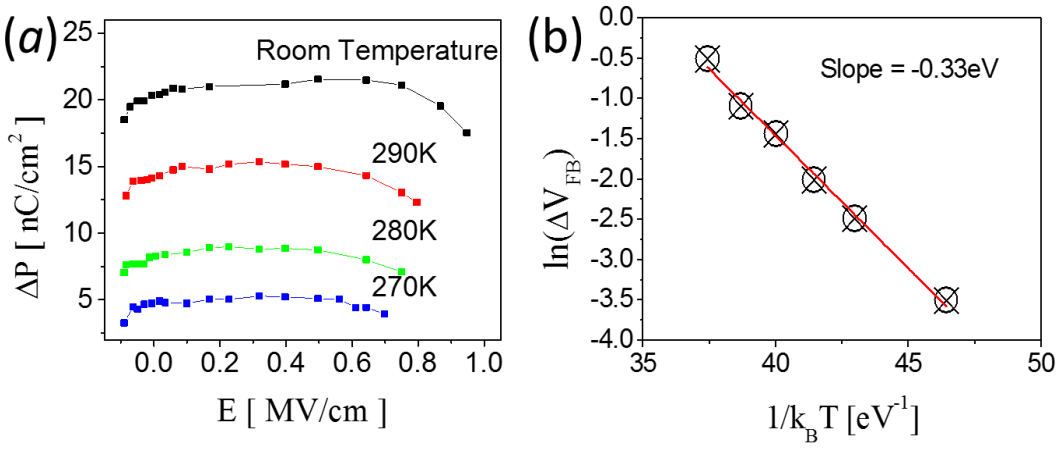

Figure A.4 (a) Polarization difference at vs. applied voltage different temperatures. (b) Memory window vs. temperature. The memory window is shrunk as the temperature decreases, indicating that the remnant polarization becomes smaller at lower temperature. The memory window is fitted as an exponential function of $1/k_BT$ (k_BT is the thermal activation energy), agreeing well with both the linear- and log-scale experimental data. The activation energy is 0.33eV according to the fitting.

The quantitative analysis of polarization of Bi_2Te_3 indicates thermal activation of the surface carriers is the origin of polarization. In this case, ΔV_{FB} can be written as:

$$\Delta V_{FB} = \frac{A\Delta P}{C_{Bi2Te3}} = \frac{A}{C_{Bi2Te3}} \Delta P_0 e^{-\frac{q\phi_B}{kT}}, \tag{A.4a}$$

$$\ln \Delta V_{FB} = C_0 + \frac{q\phi_B}{k_B T}, \tag{A.4b}$$

where ΔP_0 is a fitting parameter, and $q\Phi_B$ is the activation energy. Fig. A.4(b) clearly shows the ΔV_{FB} is exponential to $1/k_BT$. We can get $q\Phi_B$ equals to 0.33eV from linear fitting of $\ln(\Delta V_{FB})$ versus $1/k_BT$. This relationship between ΔV_{FB} and temperature indicates the carriers were thermal activated from surface state to bulk, and then moved and accumulated on the other surface when an external electric field was applied.

In addition, we have also fabricated and measured MOS capacitors with different thickness of Bi_2Te_3. We found that MOS capacitors with Bi_2Te_3 thinner than 15nm did not exhibit significant hysteresis. It seems that the thin Bi_2Te_3 in the capacitor behaves as a conductor. On the other hand, thick Bi_2Te_3 will significantly decrease the electric field across it, resulting in small polarization and memory window.

A.4 Conclusion

We have fabricated and characterized floating-gate-like MOS capacitors with topological insulator (Bi_2Te_3) thin film sandwiched between insulating dielectric layers. The capacitors exhibited ferroelectric-like hysteresis. We have fully characterized and analyzed the hysteresis, and confirmed that it was a result of the polarization of Bi_2Te_3 under vertical electric field. Also, the polarization was identified as a result of carrier separation under vertical electric field, which is different with ferroelectrics. The thermal activation energy for the carriers (electron and hole) to separate and accumulate at the top and bottom surface of Bi_2Te_3 was extracted to be 0.33eV. Due to the fast polarization speed and excellent endurance insured by the protected surface states, as well as the CMOS compatibility, the Bi_2Te_3 embedded MOS structures are very interesting for memory application. Besides, this work demonstrated that the floating-gate capacitor structure is an effective platform to study the properties of topological insulator thin films.

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BIOGRAPHY

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LIST OF PUBLICATIONS

Journal Publications

1. **H. Yuan**, A. Badwan, C. A. Richter, H. Zhu, O. Kirillov, D. E. Ioannou, and Q. Li, "Gate assisted Kelvin test structure to measure the electron and hole flows at the same nanowire contacts," Appl. Phys. Lett., 105(13), 133513 (2014).

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4. **H. Yuan**, K. Zhang, H. Li, H. Zhu, J. E. Bonevich, H. Baumgart, C. A. Richter, and Q. Li, "Polarization of Bi2Te3 Thin Film in a Floating-Gate Capacitor Structure," submitted to Appl. Phys. Lett.

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