SINGLE-PHASE LIQUID COOLING FOR THERMAL MANAGEMENT OF POWER ELECTRONIC DEVICES

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SINLGE-PHASE LIQUID COOLING FOR THERMAL MANAGEMENT OF POWER ELECTRONIC DEVICES

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NOMENCLATURE

A	Area, m^2
A_{jet}	Area of the jet, m^2
$A_{jet\ array}$	Area of the jet array, m^2
$A_{surf,fin}$	Surface Area of the Fin, m^2
A_{total}	Total Surface Area of the Fin and Base, m^2
A_b	Area of Finned Base, m^2
A_{fin}	Area of the Fin, m^2
$Ar_{staggered}$	Area for staggered array of jets, m^2
$Ar_{aligned}$	Area for aligned array of jets, m^2
$D_{available}$	Available Diameter for Jet Array Placement, m
D	Diameter, m
D_h	Hydraulic Diameter, m
f	Friction factor
H	Height from jet to impingement surface, m
H_{fin}	Height of Pin Fin, m
HTC	Heat Transfer Coefficient, W/m^2 -K
k_f	Thermal Conductivity of the Fluid, W/m-K
K_c	Pressure Drop Contraction Correction Factor
K_e	Pressure Drop Expansion Correction Factor
$K_{staggered}$, $K_{aligned}$	Correction Factor for Jet Array Nusselt Number Calculation
$G_{staggered}$, $G_{aligned}$	Correction Factor for Jet Array Nusselt Number Calculation

L	Length of heat sink, m
L_c	Corrected Length, m
N_{jets}	Number of Jets
N_T	Number of Pin Fins in Transverse Direction
N_L	Number of Pin Fins in Longitudinal Direction
N	Number of Jets
Nus	Nusselt Number
Pr	Prandtl Number
Re	Reynolds Number
Re_{max}	Maximum Reynolds Number Between Pins
S_T	Spacing in Transverse Direction, m
S_L	Spacing in Longitudinal Direction, m
S	Jet Spacing, m
Q_{total}	Total Heat Transfer Rate, W
Q_{max}	Maximum Heat Transfer Rate, W
V_{jet}	Velocity of Individual Jet, m/s
$\dot{V}$	Volumetric Flow Rate, m^3/s

Greek Symbols

α	Height-to-diameter aspect ratio
β	Transverse Spacing – to – Diameter ($\beta = S_T/D$)
Θ_b	Temperature Difference Between Heat Sink Base and Fluid
η_{fin}	Fin Efficiency
η_o, η_{HS}	Overall Heat Sink Efficiency
λ	Longitudinal Spacing – to – Diameter ($\lambda = S_L/D$)

ρ	Density, kg/m^3
σ	Correction Factor for Spacing in Pressure Drop
ν	Kinematic Viscosity, m^2/s

SUMMARY

Power electronic devices such as MOSFETs, HEMTs, and IGBTs often face reliability challenges due to poor thermal management during device operation at high power densities. In the conventional approach, such devices are packaged on power electronic substrates (e.g., direct bonded copper (DBC)) which is then attached to heat spreaders and ultimately cold plates to remove dissipated thermal energy. Thus, there are several critical layers that add to the thermal resistance of the overall design that limit the heat dissipation from power electronic devices. By eliminating layers, the integration of liquid cooling techniques has shown promise to significantly reduce (up to 25% reduction) in the thermal resistance in power electronic cooling systems as compared to the thermal resistance found using a conventional cold plate cooler design. Thus, the main objective of this work is to evaluate vertical (perpendicular fluid flow) and horizontal (parallel fluid flow) cooling schemes with integrated cooling on the backside of the DBC substrate. The cooling systems in this work utilize directly integrated cooling of electronics (DICE) techniques with enhanced heat transfer through micro-structured features integrated into the DBC. For this work, each cooling method underwent a pseudo-optimization design analysis to identify the relevant contributors to the performance of the heat sink designs. Parameters such as pressure drop, pumping power, and heat transfer coefficient were used to assess industry and manufacturing tradeoffs associated with each design. Through experiments, the pressure drop, chip junction temperature, and inlet and outlet temperatures were measured and will be presented. To validate the experimental results, numerical and analytical models were developed to

simulate the experimental environment and will be presented. Finally, the prospects for integrating these techniques into real power electronic packaging architectures will be discussed.

CHAPTER 1. INTRODUCTION

Power electronic devices enable the smart conversion and distribution of power for electric systems by changing the waveform and voltages of power sources. The Department of Energy (DOE) projects that by 2030, over 80% of all electricity in the U.S. will flow through some type of power electronic circuit [1]. Power electronics can be found in various industries including: renewable energy companies, transportation, electric machines, smart electrical grids, military fighter jets, manned and unmanned vehicles, computers, industrial automation, communication and lighting. As such there are performance and efficiency requirements set by each of these applications that drive innovation in the power electronics market. Across all sectors, there is a push for power electronics to minimize size, weight, power required and cost (SWaP-C). In order to achieve this, researchers have explored different tactics to reduce SWaP-C while increasing the efficiency, performance and reliability of power electronic devices.

1.1 Transportation Requirements

In transportation, studies show that 93% of fuel used in transportation comes from petroleum [2]. As a result, there has been increased dependency on oil imports, and concern for the increase of greenhouse gas (GHG) emissions. To disengage consumer mobility from its dependence on oil, there is a push for more environmentally-friendly, fuel-efficient vehicles to eliminate the use of fossil fuels, and development GHGs. The volatility of oil prices has also increased demand for exploration of alternatives to diesel engines and gasoline. One approach is through the conversion of mechanical systems to electrical systems in vehicles such as the Electric Vehicle (EV) and Hybrid Electric

Vehicle (HEV). EVs and HEVs are expected to reduce petroleum consumption by over 40% and reduce GHG emissions by over 30% and significantly shape the automotive industry [3]. In 2012, President Obama presented the EV Everywhere Grand Challenge to encourage production of plug-in electric vehicles (PEVs) that will be market-competitive compared to traditional gasoline vehicles for American families by 2022 [2].

The DOE has developed strategies and technical targets to meet this demand for PEVs, and there are four major target areas: 1) Battery R&D, 2) Electric Drive System R&D, 3) Vehicle Lightweighting, and 4) Advanced Climate Control [2]. It is expected that meeting these goals will allow for the levelized cost of a 280-mile drive range EV to be comparable to a similarly sized internal combustion engine (ICE) vehicle [2] In the electric drive, there is a target system cost reduction from $30/kW to $8/kW, a specific power target increase from 1.1 to 1.4 kW/kg, power density target increase from 2.6 to 4.0 kW/L, and an overall peak efficiency target increase from 90 to 94% by 2020 [2].

Research completed at Oak Ridge National Laboratory (ORNL) has identified target areas to meet the DOE's 2020 goals. To reduce the cost of power converters, the functionality of components must be implemented through advanced electrical architecture to support miniaturization of the devices and parasitics. As the inverter contributes to 40-50% of the power module, this cost can be reduced through advanced packaging and high temperature designs. The capacitor contributes to about 20 % of the inverter cost. Thus, the DOE's Vehicle Technologies Office (VTO) Advanced Power Electronics and Electric Motors (APEEM) program has developed motor drive system targets for a 35% size reduction, 40% weight reduction and 40% loss reduction that can

be achieved using wide bandgap (WBG) materials [4]. A schematic of the program's targets can be found in **Figure 1**.

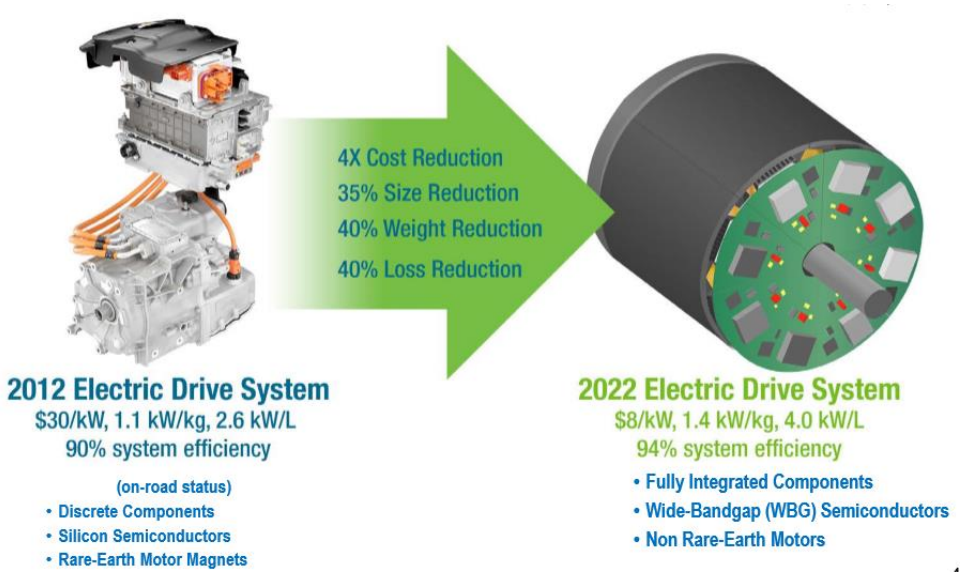


Figure 1 – DOE Vehicle Technologies Office APEEM Motor Drive Systems Targets [4]

From **Figure 1**, it can be seen that WBG materials play a major role in reducing the size and cost of motor drive systems while significantly increasing the ability of the motor drives to push higher power out of the systems. Although power devices are being developed to operate with very high efficiencies (up to 96-99%), these devices are not perfect [5]. Given the way power devices operate, the power losses generated due to inefficiencies will become more significant as these devices are run at high power conditions. Additionally, the performance of power electronic devices can be impacted by poor thermal management strategies. Thus, to minimize any additional losses from the device, there is a need to apply effective thermal management techniques to high power devices. Moreover, the use of WBG materials coupled with heat rejection systems could allow for high power devices that operate with a longer lifetime while further driving

down maintenance costs. Finally, for minimization efforts, compact designs must be developed with these innovative materials [6].

1.2 Thermal Management Challenges

Conventionally, silicon has been used for power devices because of its versatility of use. However, in electronic devices, silicon faces a temperature limit on 150˚C [7]. Consequently, the push for higher power density desired by society does not allow silicon to adequately meet the material performance needs of high power devices. Thus, thermal management techniques are needed to aid in improving the reliability and stability of these devices. A few thermal management strategies have been studied towards this end. One approach has been to address thermal management challenges associated with device package materials and package designs. **Figure 2** shows a power electronics module with an array of electronic devices.

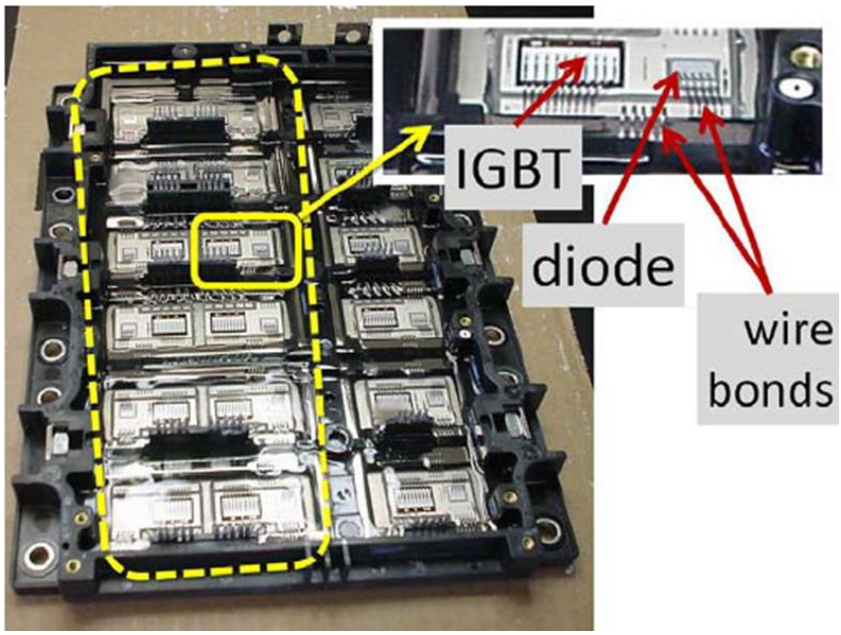


Figure 2 – 2004 Toyota Prius HEV Inverter [8]

Temperature and thermal cycling are some of the chief stressors that cause device failure and impact the performance, reliability and efficiency of power electronic devices; thus reducing machine operation time and generating high maintenance costs. Moreover, without thermal stability, the performance of power devices degrades overtime. **Figure 3** shows the impact of temperature on the performance of power electronics modules.

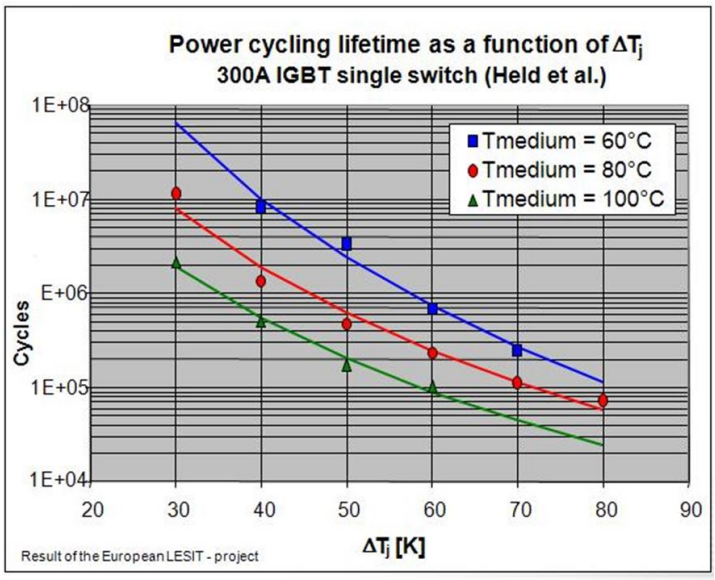


Figure 3 – Power Device Cycle Operation vs Junction Temperature [9]

As shown in **Figure 3**, the number of cycles for which a power electronics module can operate significantly decreases as the junction (chip) temperature increases. For power electronic modules, this reduction in performance limits the ability of the module to operate effectively. For EV traction drive inverters, this reduction in performance impacts fuel efficiency, limits the driving range of the vehicles and necessitates more frequent charging. Therefore, effective thermal management of power electronics could improve the fuel efficiency and reduce the amount of GHGs in the environment. The use of wide bandgap materials coupled with innovative heat dissipation

techniques will allow for increased power density and reductions in volume and weight of the power devices [6]. Thus, the driving and operation range can be improved.

Power devices also often face the challenges of delamination, detached wire bonds, substrate fracture and fatigue, and fracture and fatigue of the die attach (interface material) [10]. Each of these device degradation methods occurs as a result of thermal cycling and thermal stresses put on the devices. These stressors are generated due to the high heat fluxes that arise due to the increased power densities of the electronic devices. Narumanchi [4] shows the significant increase in the chip temperature from the thermal resistance buildup through the material layers that make up the power device stack. **Figure 4** shows the impact of thermal interface materials on the chip temperature in power electronics.

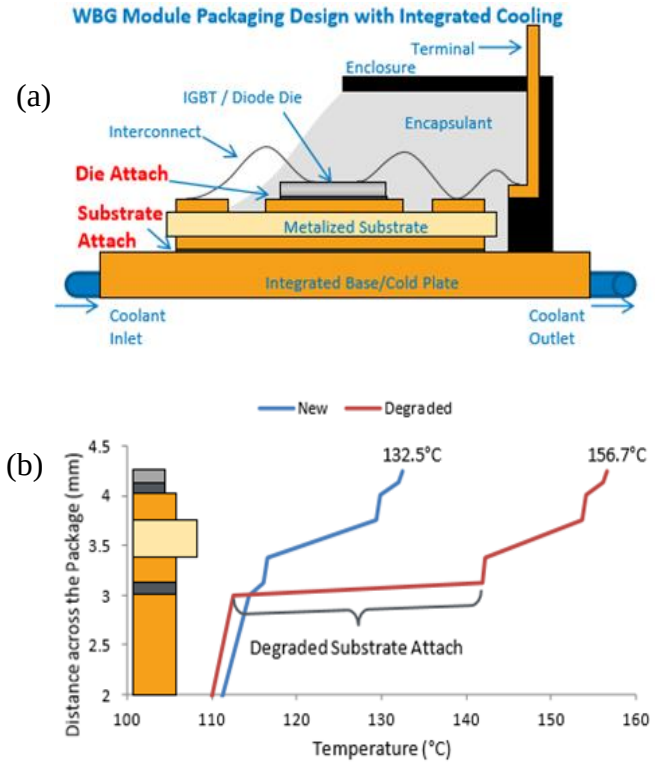


Figure 4 – (a) Integrated Cooling Power Electronics Module Stack, (b) Temperature Profile Through Device Stack [4]

From **Figure 4**, it can be seen that as the interface materials degrade in a power module, the chip temperature is significantly higher that the chip temperature in a device with new interface materials. These interface materials are needed to provide mechanical stability, and many interface materials also aid in improving the electrical performance of the device. However, new interface materials have been studied to mitigate their tradeoff of high thermal resistance in a power electronics stack [11]. Conventional power devices often have a stack thermal resistivity of 0.7 C/W-cm^2 [11]. Through different thermal management strategies, this total package resistivity can be reduced to 0.11 - 0.7 C/W-cm^2 [11]. Through this work, a directly integrated cooling of electronics (DICE) strategy is introduced to eliminate some of the interface layers that generate high thermal resistance and reduce the overall thermal resistance of the power device stack below the current thermal resistance values.

1.2.1 Current Work Motivation and Objectives

In hybrid electric vehicles (HEVs), air-cooling via finned surfaces is the common heat dissipation technique for thermal management of power electronic modules due to its simplicity of installation. However, these cooling systems are often designed to be very bulky in order to transfer more heat out of the system. Thus, these heat sinks add weight and occupy more space in the hooded-area of HEVs. Liquid cooling techniques have been explored because of the improved heat transfer capabilities of liquid coolants over gas coolants (such as air). However, a number of the air-cooling techniques have reached their thermal limit for high heat flux applications. **Figure 5** shows an IGBT power module mounted to a finned heat sink.

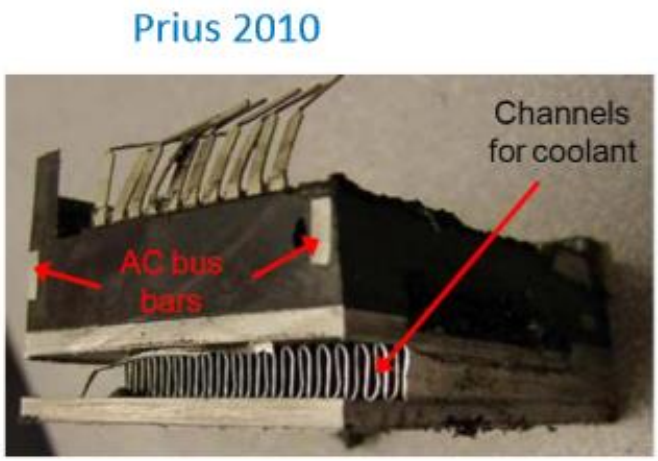


Figure 5 – 2010 Toyota Prius Power Module with Finned Channels for Coolant Flow [4]

Following the work of Tuckerman and Pease [12], horizontal cooling techniques were first studied for liquid cooling loops. The cooling systems in this work were able to dissipate heat from heat fluxes up to 790 W/m^2. However, cooling systems in this work were developed through silicon etching. For high heat flux IGBT applications, this

cooling method introduces the challenge of achieving optimal electrical performance due to the flow of current in these systems during operation. Thus, different cooling strategies must be explored instead those implemented in the work by Tuckerman and Pease [12].

This work explores single-phase liquid cooling techniques that not only address heat dissipation through the device stack, but it also applies a directly integrated cooling of electronics (DICE) method to reduce the thermal resistance often built in power device operation. Throughout the literature, it has been found that integrated cooling methods generally perform better than conventional cooling techniques [13]. Thus, this work explores integrated cooling through micro-structured heat sinks built into the direct bond copper (DBC) substrate of power electronic modules. By bringing the cooling chamber of the power electronics closer to the chip, layers that contribute to the thermal resistance (and consequently limit effective heat dissipation) can be eliminated.

The first objective of this work is to test this concept experimentally and validate the results numerically and analytically. Aside from thermal resistance, literature has identified pressure drop as another major consideration in heat sink design. Pressure drop most directly impacts the pumping power. This parameter is important because pumping power is the power required to effectively flow the coolant through the closed loop to cool the device. If this value is too high, the system has to operate at lower than optimal power to account for what is needed by the cooling loop. Thus, design choices are often made with these two parameters in mind. The second and third objectives of this work are to apply horizontal cooling and vertical cooling to the DICE concept for better heat dissipation and thermal management of power devices. Both the horizontal and vertical cooling studies will be validated experimentally, numerically and analytically. A fourth

objective of this work is to test each of these cooling designs at higher heat fluxes, and model the device stack using different semiconducting materials. This objective will provide insight to the effectiveness of the DICE cooling technique and provide a foundation for future exploration of DICE coupled with WBG materials. As the heat fluxes that come from these devices is not always uniform, this objective will also provide a foundation to address localized hot-spot cooling through numerical and experimental models.

Chapter 2 of this thesis reviews the components and manufacturing of conventional power electronics. Following this, the thermal management and heat dissipation challenges associated with power electronics are discussed. Then, a literature review of horizontal (microchannel, micro-pin-fin etc.) and vertical (jet impingement, spray cooling, etc.) methods are reviewed. With each cooling method, the limitations of the techniques are reviewed and a brief description of the project objectives on both horizontal and vertical cooling methods are discussed. Finally, the chapter highlights the impacts of warpage in device development and reflow of the thermal interface materials, and the importance of manufacturing processes that minimize the impacts of warpage.

The next chapter discusses the DICE cooling approach as well as the design analyses completed to implement the DICE concept. Following this, the chapter highlights pseudo-optimization approaches taken to design various heat sinks used in the horizontal cooling experiments and numerical models, as well as those taken to design the jet impingement array test coupons developed to assess the performance of a vertical cooling method. The chapter also provides a brief review of the chip heater design used for this work. Then the calibration methods for the experimental test set up equipment are

reviewed. Next, the numerical modeling methodology for the vertical cooling schemes is reviewed. Finally, a literature review on warpage challenges associated with power electronics manufacturing is discussed, and the chapter concludes with a brief numerical study of warpage impacts in manufacturing of the DICE stack is reviewed.

Chapter 4 reviews the experimental results from the horizontal and vertical cooling schemes. The horizontal cooling experimental results for each of the heat sink designs are reviewed first. Then the results from the jet impingement cooling methods are reviewed. In each of the experiments, the inlet and outlet temperatures, pressure drop, and chip temperature are measured. From this, the measured parameters are used to evaluate the performance of the heat sink designs. Then the performance of vertical cooling schemes are compared to the performance of the horizontal cooling schemes. To validate the experimental models, analytical models were developed for the horizontal cooling scheme, and numerical models were developed for the vertical cooling scheme. Following this, the numerical models developed to study warpage impacts on the DICE device manufacturing, and the results of these numerical models are used to gain insight to the feasibility of a reduced power stack on conventional manufacturing.

The next chapter reviews the objectives of this work, and discusses results obtained through the experimental and numerical modeling evaluating the DICE concept. performance of each of the DICE concept cooling schemes and provides comparisons between the horizontal and vertical cooling methods. The aim of the study was to determine the feasibility of implementing the DICE concept in conventional power electronic modules. To do this, the DICE stack eliminates some of the layers in a conventional stack that lead to high thermal resistance and thus poor thermal

management of the power electronic module. Through this work, the DICE concept was evaluated through horizontal and vertical cooling schemes, and the impacts of warpage on the device during manufacturing are reviewed to test different interface materials commonly used in power module chip and substrate interfaces.

Chapter 6 discusses modifications that can be made to further improve this work. In this chapter, the discrepancies in the numerical, experimental, and analytical models are discussed. In the experimental models, the contributions of uncertainty to each of the measured parameters are discussed. Next, the changes that can be made to the experimental test-set up in order to minimize the uncertainty and losses are discussed. Moreover, improvements that can be made to the test section design are reviewed. In the numerical models, strategies to optimize the models are briefly discussed and additional modeling. Next, the chapter reviews future studies and applications of the DICE concept to be completed for higher heat flux device packages and various heat sink geometries on full array power modules.

CHAPTER 2. BACKGROUND

This first part of this chapter provides a brief overview of power electronic devices, the materials used in power devices and their limitations of these materials. After this, the manufacturing of a conventional power module stack is briefly reviewed, and the need for improved thermal management for the devices in operation is discussed. Next, the chapter reviews studies completed that assess various cooling techniques (air-cooling, liquid cooling, horizontal and vertical cooling), the benefits and limitations associated with each cooling strategy are identified. Finally, the chapter highlights the impacts of warpage in device development and reflow of the thermal interface materials, and the importance of manufacturing processes that minimize the impacts of warpage.

2.1 Power Electronic Devices

Power electronic devices are often some form of a transistor and they are designed to turn on and off rapidly, thus switching the electrical power electronic circuits. A standard transistor functions as a switch to enable or prevent current from flowing through a device. In an integrated circuit, these transistors are necessary to prevent large currents from flowing into stages of a circuit that require small amounts of current.

Insulated Gate Bipolar Transistors (IGBTs) integrate compound waveforms with low pass filters and pulse width modulation and they are used to create or block electrical paths in circuits used in electric vehicles, solar inverters, and appliance motor drives, etc. [14]. In transportation, power electronic devices such as: IGBTs, Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), and High Electron Mobility

Transistors (HEMTs) are used to supply power for the inverter drives in switchmode DC-DC converters, battery chargers, and control of brushed DC motors, etc. [15]. Silicon has traditionally been used for IGBT power electronics modules. It has a bandgap energy of 1.1 eV and an operating temperature limit of 150˚C [7]. Today, power electronic devices are increasingly challenged to achieve higher power densities, and consequently, maintain higher temperature limits. Thus, there is a need to explore other materials that can operate at higher temperatures and achieve greater power dissipation.

To date, there are power electronic device materials that can operate at higher temperatures such as 200˚C, but these devices are more costly to implement [16]. Thus, wide bandgap (WBG) materials were introduced to accommodate high temperatures while maintaining the reliability of the devices. Due to their improved thermal properties and increased temperature limits, WBG materials (such as silicon carbide (SiC) and gallium nitride (GaN)) are expected to replace their conventional Si counterparts in power devices, reduce the size, weight and cost of components used for various machines, while increasing energy efficiency. **Table 1** highlights various properties of WBG materials compared to conventional Si material.

Table 1 – Semiconductor Material Properties [17], [7], [18], [19], [20]

Parameter	*Si*	*4H-SiC*	*6H-SiC*	*GaN (Wurtzite)*
Bandgap, E_g (eV)	1.12	3.26	3.03	3.45
Electric Breakdown Field, E_c (kV/cm)	300	2200	2500	2000
Electron Mobility, μ_m (cm^2/V-s)	1500	1000	500 , 80	1250
Thermal Conductivity, k (W/cm-K)	1.5	4.9	4.9	1.3
Coefficient of Thermal Expansion (1/˚C)	2.6×10^{-6}	$\alpha_{11} = 3.21 \times 10^{-6} + 3.56 \times 10^{-9}T - 1.62 \times 10^{-13}T^2$ $\alpha_{33} = 3.09 \times 10^{-6} + 2.63 \times 10^{-9}T - 1.08 \times 10^{-12}T^2$	$\alpha_a = 4.2 \times 10^{-6}$ $\alpha_c = 4.6 \times 10^{-6}$	$\alpha_a = 5.59 \times 10^{-6}$ $\alpha_c = 3.17 \times 10^{-6}$

From the table, it can be noted that WBG materials generally have higher thermal conductivities than silicon, with GaN as an exception. As such, WBG materials can significantly enhance heat dissipation from the device stack. The bandgap is much higher

in both SiC and GaN, so these materials offer improved electrical performance. WBG materials also have higher electron mobility and higher breakdown voltages which enable faster transmission of electrical current through semiconducting materials, and a larger resistance to reverse conduction possibilities in the device respectively. This suggests that WBG devices can have an increased lifetime over Si devices.

Although WBG materials can improve the performance of power devices, they are still met with thermal challenges that can limit their performance due to mismatch of the coefficient of thermal expansion (CTE) variations in their semiconductor bodies. Thus, for optimal device performance, the homogeneity and heterogeneity in the semiconductor layers must be studied to better identify areas of potential device failure.

2.1.1 Power Electronic Device Stability and Reliability

The stability and reliability of power devices can be compromised, mainly through avenues such as: mismatch of the CTE, and thermal stresses. As seen from table 1, the CTE varies between Si, SiC and GaN. Due to the CTE mismatch found in heteroepitaxial growth of SiC and GaN on Si, and SiC substrates, there is a need for nucleation layers (buffer layers) to address some of the stresses that would occur in the device. Without a buffer layer, cracks can form in the substrate and lead to reduced device performance. Other defects that can occur in SiC substrates include lattice warping, inclusions, and edge and screw defects. **Figure 6** shows some modes of device failure due to cracking, voiding and delamination due to increased thermal stress.

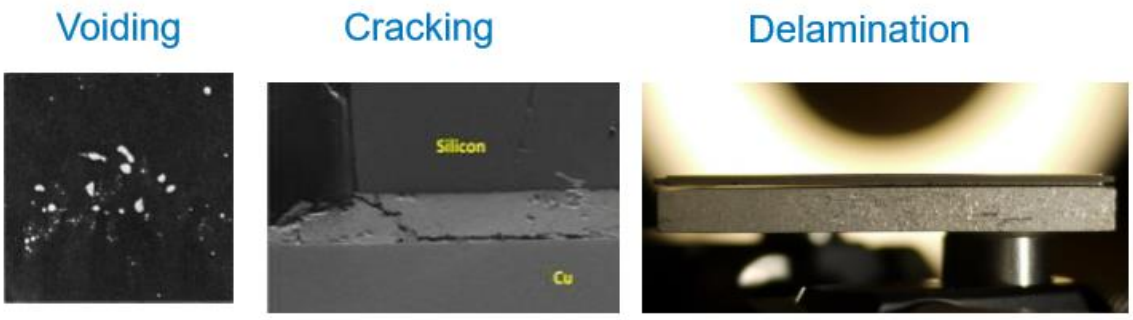


Figure 6 – Some Modes of Power Device Failure in direct bond copper (DBC) Substrate (voiding is generally due to poor chip to substrate attachment; cracking usually occurs in the substrate; delamination is usually between the DBC stack layers) [4]

The use of WBG materials for power electronic devices in transportation introduces the possibility of smaller more efficient inverter devices. However, as mentioned earlier, defects that can occur due to material expansion under heat loads still need to be addressed for widespread adoption of these materials. To this end, manufacturing techniques such as sublimation epitaxy and other seed positioning methods have been used to minimize the frequency of defect occurrence [21], [22]. Although beneficial, manufacturing techniques cannot meet all of the thermal management challenges associated with power devices. Thus, there is still a need for improved thermal management through the device package, and with effective heat dissipation techniques.

2.1.2 Conventional Device Manufacturing

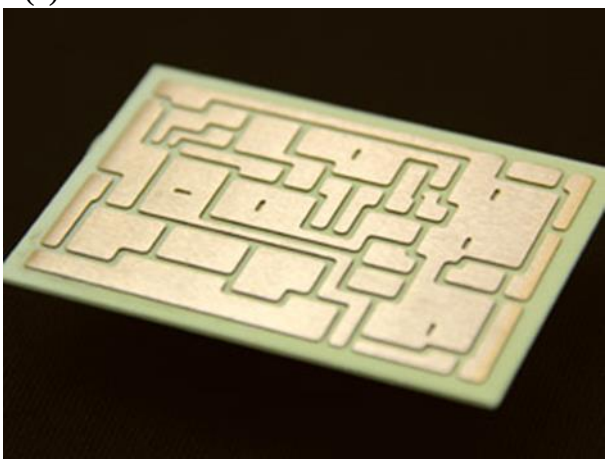
Conventional power devices for HEVs incorporate an IGBT chip and/or diodes, direct bond copper (DBC) substrate layers, a copper baseplate, heat sink cooler (or a cold plate), and coolant layer all attached using interface materials. This section reviews the

manufacturing processes for these layers as they relate to thermal management and device reliability.

2.1.2.1 Direct-Bond Copper (DBC) Substrate

DBC substrates are often made from flat copper pieces separated by a ceramic (aluminum or alumina) layer. This ceramic layer is used to provide electrical isolation when the device is in operation. According to Schulz-Harder [19], ceramic layers are also beneficial to use in DBC substrates because of their high stiffness as compared to other materials. Therefore, the ceramic layers will need large forces to generate damages, and the plastic deformation of the material allows for it overcome tensile stresses developed with increased loads [19]. **Figure 7** shows a pre-mounted DBC substrate and a mounted IGBT and diode chip DBC substrate.

(a)



(b)

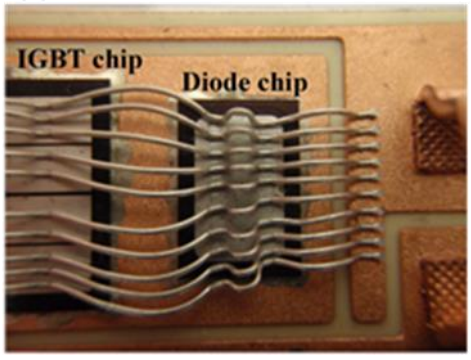


Figure 7 – (a) DBC Substrate [23], (b) IGBT and Diode on Power Electronics Module [24] ((a) shows DBC Substrate that has been etched for mounting power devices in a circuit array)

Due to the CTE mismatch of the different materials, researchers have studied the ability of these devices to undergo thermal cycling, and Schulz-Harder [19] suggests that the reliability can be improved through dimpling at the edges of the copper plate before welding the layers together. This allows for DBC substrate-based packages to have "high current capability, low thermal resistance, low weight, and small volume as compared to metal packages" [19]. Furthermore, Schulz-Harder [19] suggests that fusing the copper and ceramic in a DBC stack allows for direct application of complex 3D liquid cooling structures for improved heat dissipation at high temperatures [19]. Due to its ability to maintain its electrical performance through thermal cycling and its ability to be produced on a massive scale, DBC is commonly used for power electronics packages [19],[20].

2.2 Thermal Management

In the transportation industry, there has been greater push for smaller power electronic devices due to the limited size in the hooded chamber of electric vehicles, and the impacts on fuel efficiency heavier vehicle components can have. To meet the size and weight requirements, designers have explored more efficient materials and cooling methods to address the challenges met in the area of thermal management.

The high temperatures in power electronic devices are driven by the high heat fluxes generated as the device operates. According to Dang [25], these high temperatures cause device failure because of electro-migration. As the material moves, the layers of the device degrade, thus limiting the use of the device. Some considerations in effective thermal management include: thermal resistance, heat dissipation and pumping power. The thermal resistance and heat dissipation are better understood by exploring the layers

that make up the device stack, while the pumping power impact is more driven by the heat sink design.

2.2.1.1 Thermal Interface Challenges

When developing the IGBT power electronics package, the DBC layer is soldered to the IGBT chip, and the chip is wire-bonded to complete the power module. The other side of the substrate is attached with another thermal interface material (often solder) to a metal heat spreader. Following this, the package is attached to a heat-sink with a thermal interface material (often thermal grease) that is used to isolate high temperature regions from low temperature zones [6]. Given the material property variations, these numerous layers can lead to increased thermal resistance through the layers in the device stack. **Figure 8** provides a schematic of an IGBT power electronics stack.

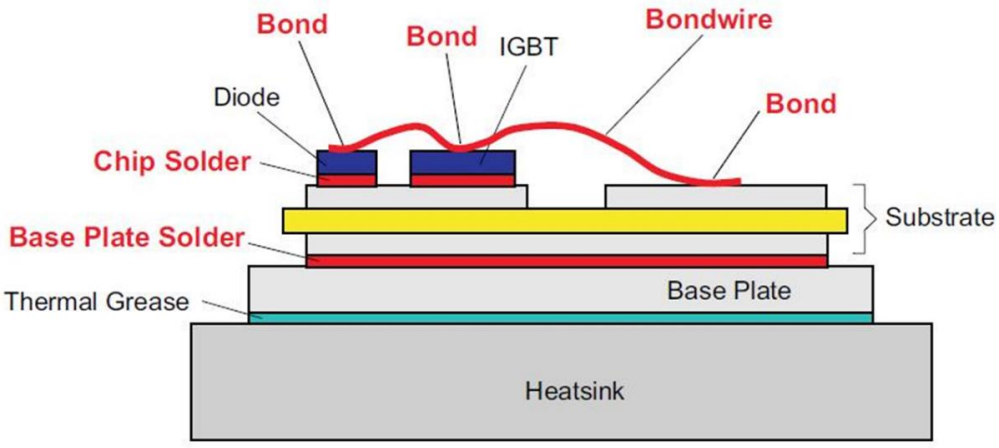


Figure 8 – IGBT and Diode on Power Electronics Module [26]

The thermal resistance is important to quantify because it impacts how easily the heat is dissipated through the layers of the electronic device. Low thermal resistance is preferred because it allows for better heat dissipation and prevents the device layers from

retaining the heat that causes the components to deteriorate due to high temperatures seen in operation. **Figure 9** gives a schematic of the device stack with the interface, chip and substrate layers that contribute to the thermal resistance in power modules.

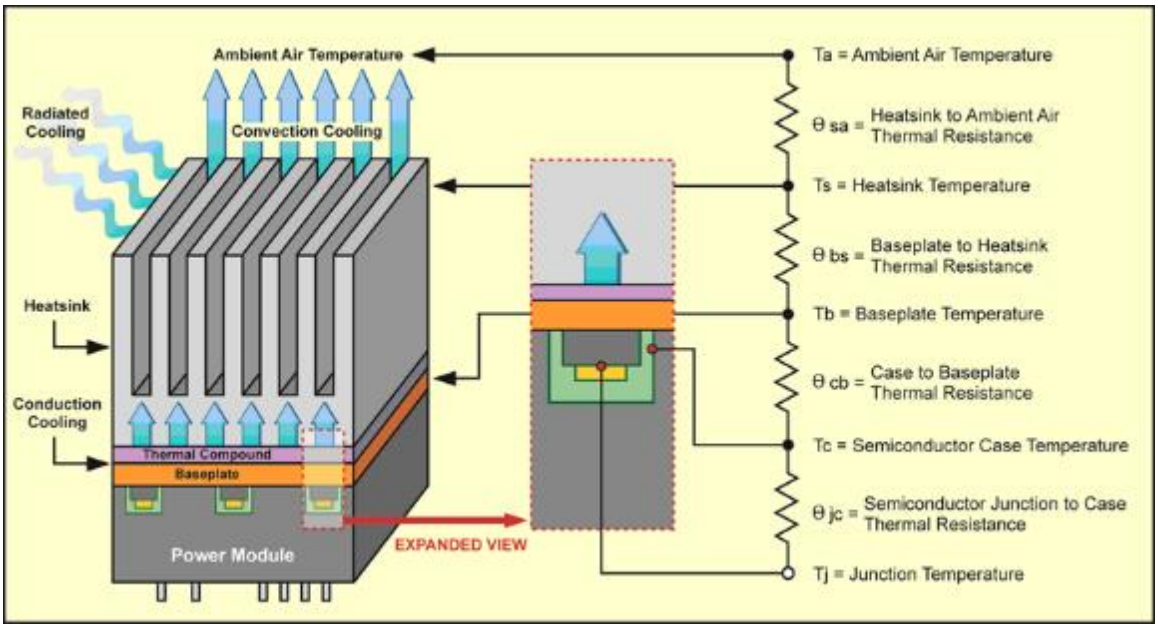


Figure 9 – Schematic of Conventional Power Device Package and Resistance Network for an Air-Cooled Power Module [27]

Valenzuela *et al.* [11] identified the main contributors to thermal resistance in conventional devices: die attach structure, spreader, cold plate, thermal interface material (TIM) and the fluid. Of these layers, the components that most influence the thermal resistivity are the spreader, cold plate and TIM (making up approximately 72% of the total package resistivity) [11]. From this work, it was found that a conventional device stack develops a total package IGBT thermal resistivity of 0.70 C/(W/cm^2). The work also analyzed single-sided and double-sided cooling methods and found thermal resistivity of 0.19 C/(W/cm^2) and 0.110 C/(W/cm^2), respectively for a 200 µm silicon die. Valenzuela *et al.* [11] also found that a spreading resistance develops in the spreader that

has significant impact on the overall thermal resistivity. The elimination of that spreader necessitated another cold plate that could be directly bonded to the DBC.

Narumanchi *et al.* [28] explored various thermal interface materials and thermal greases to determine the impact of that layer on the overall thermal resistance. Experimental tests were completed for silicon die and silicon carbide (SiC) devices. It was found that the choice of thermal grease has significant influence on the overall thermal resistance, as it was concluded that the TIM layer is the largest contributor to the thermal resistance. The power modules used in this work were 134.2 mm^2, with a 0.51 mm silicon die.

Another challenge that arises with thermal interface materials is the development of intermetallic compound (IMC) layers. When these IGBT modules are solder-mounted to the DBC substrate, there are often intermetallic compound (IMC) layers that are developed due to chemical reactions in the solder and metal layer contacts [29]. According to Hsu *et al.* [29], the IMC layer is more prone to thermal or mechanical stresses and cracks are often initiated at the interfaces of the solder/IMC or substrate/IMC. Therefore, it is critical to either reduce the number of interface layers needed to mount the electronics package, or limit the CTE mismatch between the materials used to mount the chip to the substrate to improve of the power device reliability, and minimize the thermal resistance through the device.

2.2.2 Heat Dissipation

As power electronics technologies have become more advanced, researchers have met a heat flux challenge on the order of 600-1000 W/cm^2 [30]. The use of WBG materials has aided in this achievement in power electronic device technology, but if the high heat fluxes and temperatures generated by increased power density are not addressed through effective heat dissipation techniques, they can be detrimental to device reliability. The heat dissipation is met by an effective cooling technique. With the introduction of microchannel cooling by Dr. Tuckerman and Pease, there has been much exploration of linear fins, micro pin fins, and offset plate fins. Such designs have been incorporated into developing single-sided and double-sided cooling as well as microfabrication methods that employ different geometries.

2.2.2.1 Cooling Methods

There are two main cooling techniques: passive and active cooling. Passive cooling schemes avoid the need for pumps and motors, as they operate by employing the heat transfer concept of natural convection. These systems are sometimes preferred because of the reduction of necessary components for effective cooling. Active cooling is a cooling method such as forced air convection, or forced liquid convection. These systems usually provide higher heat transfer coefficients (HTCs), thus increasing the heat dissipation rate. Both cooling techniques have been studied, and face different challenges: passive cooling systems are often big and bulky, and liquid-cooled active cooling systems often require high pumping power to effectively flow the coolant throughout the heat sink.

As there is a drive to make the power electronic devices smaller, there is also motivation to make the cooling channels small. Kandlikar *et al.* [30] suggested three explanations for the shift in cooler design. Microscale coolers have been studied to meet heat transfer enhancement requirements, microelectronic device heat flux dissipation increases, and the provide cooling for the plethora of microscale electronic devices requiring cooling [30].

2.2.2.2 Cooler Designs

Conventionally, an air-cooled design is used to cool power electronic devices because of its simplicity and practicality. Air-cooled designs often recycle air flowing throughout the vehicle, capture the heat surrounding the device and dissipate it through finned heat sinks. However, air-cooling designs are usually too bulky and contribute to the increased weight of the vehicles and reduction in the performance of the vehicle.

To improve the cooling of the power electronic systems, liquid cooling schemes have been introduced because many coolants such as: water, ethylene-glycol-water, etc. have higher HTCs than air. Due to the higher HTCs, liquid coolants can more effectively transfer heat through their material. With more efficient heat removal, liquid cooling allows for heat sinks to be made smaller and lighter than air-cooled heat sinks. In literature, there have been various liquid cooling methods to dissipate high heat fluxes such as: straight channel cooling, linear channel cooling, jet impingement, direct immersion cooling, and spray cooling, to name a few [31].

A few liquid cooling strategies include single-phase cooling, cold-plate cooling, base-plate cooling and double-sided cooling. Each of these cooling strategies aims to improve the heat dissipated from the device stack by bringing the cooling closer to the chip. However, these methods are usually connected to the power device with interface materials that can contribute to the overall thermal resistance in the device stack. **Figure 10** shows the cold plate, base plate and double sided cooling methods.

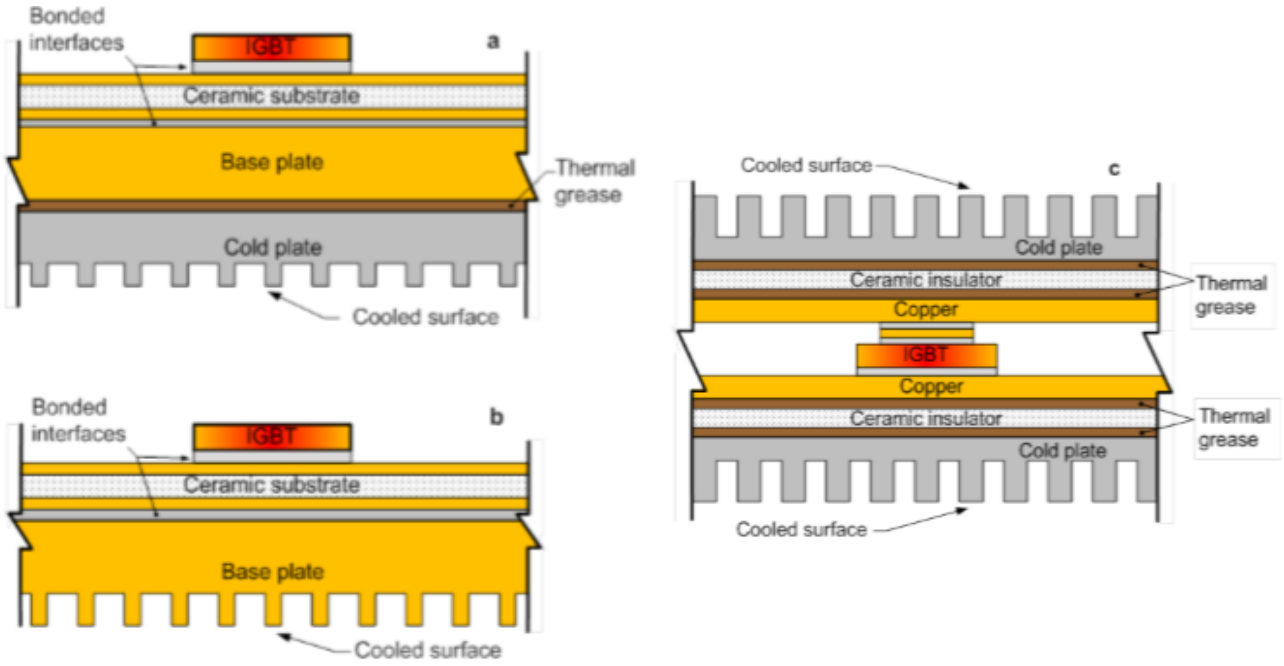


Figure 10 – (a) Cold-Plate Cooling, (b) Base-Plate Cooling, (c) Double-Sided Cooling [4]

To minimize the number of layers needed to provide cooling to the system, researchers have also explored integrated heat exchangers for improved thermal management of power electronic devices [4, 13]. Integrated cooling methods have been found to perform better than conventional cooling methods, and they can allow for complex cooling designs in the heat exchanger [4, 13]. **Figure 11** shows an integrated cooling heat exchanger.

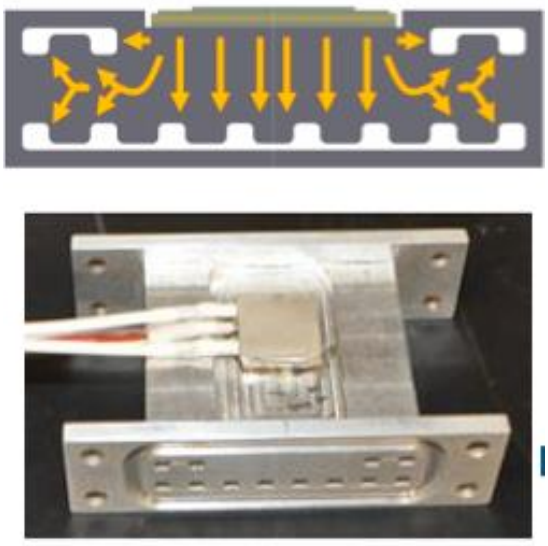


Figure 11 – Integrated Heat Exchanger Mounted to a Power Electronics Substrate and Power Electronics Chip [4]

Through integrated cooling, Narumanchi [4] cited a 55% increase in the inverter power with a 100% increase in power per die area. Additionally, integrated cooling methods introduce the possibility of localized cooling for hot spots. Bar-Cohen *et al.* [13] explores integrated cooling methods aimed to dissipate heat fluxes of 1kW/cm^2 through intrachip/interchip enhanced cooling (ICECool) methods. In this cooling strategy, convective and evaporative heat transfer methods are used to remove heat from micro- and nano-grid thermal interconnects made from high thermal conductivity materials [13].

Additionally, the work is expected to address the thermal management needs of 2.5D and 3D electronic devices. **Figure 12** provides a schematic of the ICECool concept for improved heat transfer from power devices.

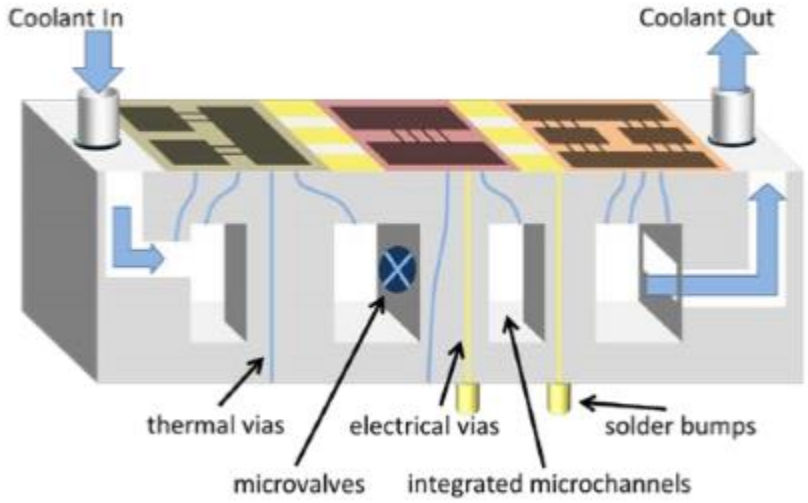


Figure 12 – Defense Advanced Research Projects Agency ICECool Integrated Cooling Concept [13]

As the heat fluxes are not always uniform from the power device, liquid cooling techniques can also enhance device reliability when coupled with localized hot spot cooling methods. By concentrating the cooling of the device to the regions most impacted by temperature, the device junction and overall temperatures can be more effectively controlled, which improves the thermal management of the device, and allows for much reduction in size and weight of the cooling device.

2.3 Horizontal Cooling Methods

Based on the heat exchanger concept of extended surfaces, horizontal cooling techniques were first explored to flow coolant over an area more easily. Horizontal

cooling describes flow patterns that move parallel to the heat flux surface. Generally, this design is simple and easy to manufacture. However, one challenge that arises with this technique is the development of a boundary layer thickness over the cooling surfaces. Over the past few decades, various horizontal cooling techniques have been explored such as: straight channel duct coolers, linear channel coolers and micro-pin fin coolers. Each of these heat sinks is reviewed in the sections below, and the challenges in horizontal coolers are identified.

2.3.1 Microgap Channel Cooler

A microgap channel cooler is the most commonly studied in heat transfer. These coolers simply provide an opening for flowing coolant over a hydraulic diameter. As these coolers resemble a duct, the hydraulic diameter, pressure drop and heat transfer properties vary for the geometry of the microgap channel cooler.

Morini [32] studied the differences in various microchannel geometries such as: micro pipes, trapezoidal, triangular and rectangular channels. The author completed a review of literature, and it was found that some of the biggest influencers on the microchannel performance are the aspect ratio of the channels, the friction factor, and surface roughness of the duct. The surface roughness and friction factor are determined from the microchannel material and manufacturing process. The paper listed numerous variations in pressure drop and heat transfer due to the geometry and surface roughness of each channel design. The straight microchannel cooler allows for coolant to flow easily through a duct or channel. However, the boundary layer thickness that develops as the coolant flows limits the effective cooling of this schematic, and other cooling channel

designs such as linear channels or micro-pin fin coolers should be explored. Microgap coolers can be shaped in different geometries, but **Figure 13** provides a schematic of one microgap channel cooler design.

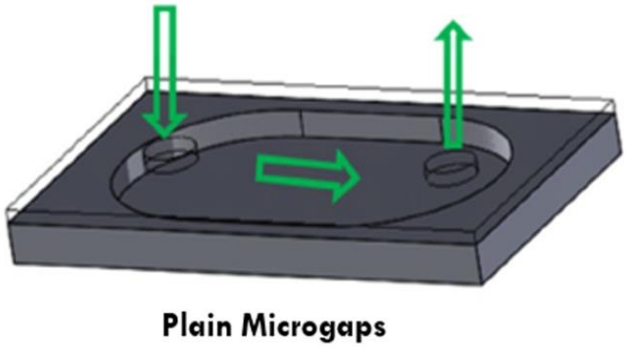


Figure 13 – Microgap Channel Cooler [33]

2.3.2 Linear Channel

The pioneering study of linear channel liquid cooling was completed by Tuckerman *et al.* [12]. The study sought to reduce the thermal resistance to improve the performance of rectangular channel heat sink incorporated into an integrated circuit chip. The heat sinks were developed by etching into silicon, and deionized water at 23˚C was used as a coolant, to dissipate a heat flux up to 790 W/cm^2. The thermal resistances this work were between 0.09-0.113˚C- cm^2/W. Although the heat flux generated was much higher than any other published work, the heat sinks were machined in silicon. Silicon etching is not optimal for power electronics modules due to the method of current flow during device operation. Furthermore, the pressure drop developed with such a design drove researchers to explore other linear channel geometries that produce low thermal resistance while minimizing high pumping power requirements. **Figure 14** provides a schematic of a linear microchannel cooler.

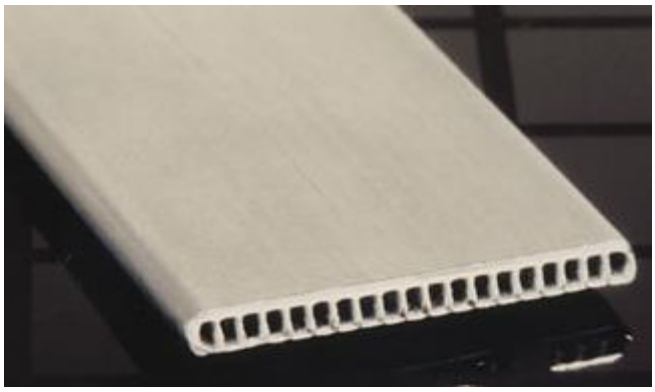


Figure 14 –Linear Microchannel Cooler [34]

Stevanovic *et al.* [35] developed an integral microchannel cooler that incorporated manifolds and linear channels in the bottom copper layer of a direct bond copper (DBC) substrate. The devices used in these experiments were 200 A, 1200 V power modules composed of IGBTs and diodes. The heat sinks were manufactured using laser ablation and micro milling techniques. **Figure 15** shows the microchannels developed using laser ablation and the channels developed using micro machining.

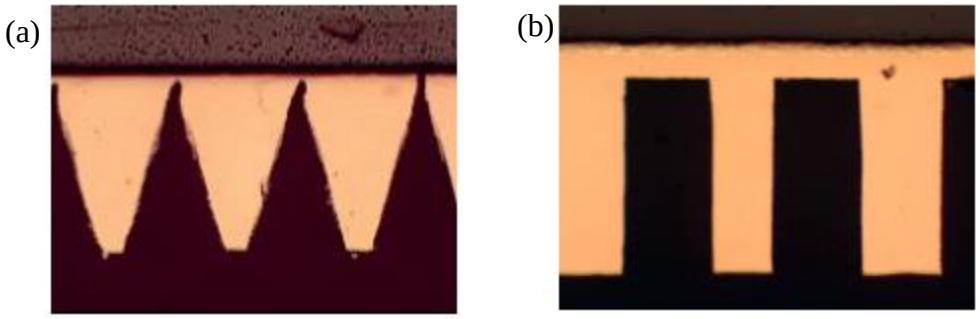


Figure 15 – Cross-Section of Integrated Microchannel Manufactured using (a) Laser Ablation, and (b) Micro-milling [35]

Through this work, it was determined that the micro-milling manufacturing technique provided greater precision for the heat sinks because the laser ablation made triangular channels instead of the rectangular channels Stevanovic *et al.*[35] intended to

design. The channels in this work had a pressure drop between 17-133 kPa, and the channels manufactured using laser ablation generated a higher pressure drop than the pressure drop generated in the micro-milled channels. The thermal resistance was 0.076 and 0.136˚C/W for the diodes and IGBT respectively.

Zhang *et al.* [36] completed a study exploring single-phase liquid cooling microchannel aluminum heat sinks for two electronic devices. Two 12 mm x 15 mm aluminum heat sinks were manufactured using a micro-end milling technique. The two heat sinks were attached to flip chip ball grid array (FCBGA) packages. Inlet and outlet manifolds were also designed to allow the fluid to flow over the microchannels. The 12 mm x 12 mm FCBGA chips were given a power input of 40W and 60W. The thermal resistance seen by both arrays ranged from 0.32-0.44˚C/W, and the cooling channels generated pressure drops between 5-100 Pa. **Figure 16** shows the microchannel heat sink and flow pattern used in this work.

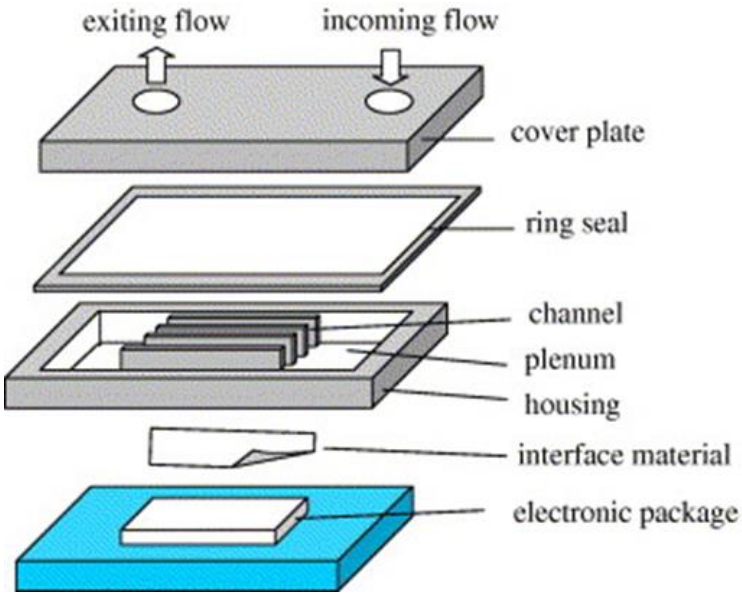


Figure 16 – Microchannel Cooling Heat Sink Design and Flow Pattern [36]

2.3.3 Non-linear Fin Channels

The design of the finned heat sink impacts the pumping power and heat transfer rate. The parameters that influence the pumping power and heat transfer rate are: the geometry of the fins, the arrangement of the fins, the fin-to-fin spacing, fin diameter and the fin height, etc. As each of these significantly influences the efficiency of the finned heat sinks, much research has been completed in this area.

Remsburg [37] studied nonlinear fin patterns such as: pin fins, louvered fins, offset fins, wavy fins and straight fins. The author compared each fin design, and it was found that as the Reynolds number increased, the heat transfer per unit height decreased. The pin fins achieved the highest heat transfer per unit area, while the straight fins achieved the lowest heat transfer per unit area. It was concluded that the nonlinear fin designs had the greatest thermal performance. **Figure 17** shows nonlinear fin patterns.

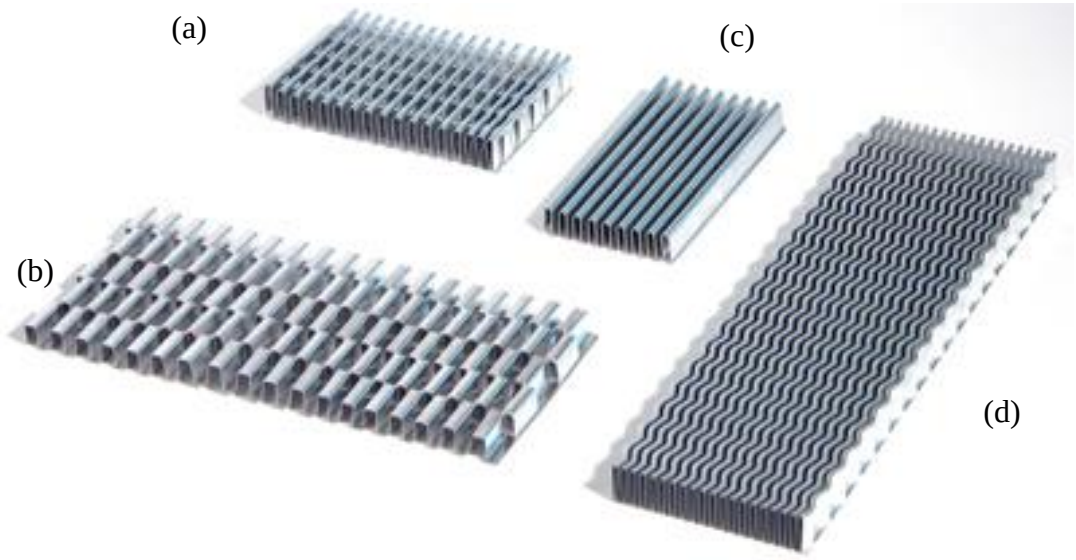


Figure 17 – Various Finned Heat Sink Geometries (a) Louvered Fins, (b) Lanced Offset Fins, (c) Straight Channel Fins, (d) Wavy Fins [38]

2.3.4 Pin Fin Channels

Pin fins have been found to meet the high heat flux dissipation requirements while minimizing the pressure drop associated with linear channels. There are two pin fin array types commonly studied: staggered and aligned pin fins. Researchers have tested various pin fin designs, considering the pin fin spacing, aspect ratio considerations such as: fin height-to-diameter ratios, tip clearance, and length-to-width ratios of the cooling surface.

Ndao [39] conducted experiments on various fin geometries including arrays of circular pin fins, square pin fins, elliptical and hydrofoil pin fins. These arrays were manufacturing using thin film deposition, photolithography, etching, bonding, dicing, and

chemical mechanical polishing microfabrication techniques. It was found that the hydrofoil and elliptical designs offered less heat transfer than the circular or square geometries. **Figure 18** shows machine milled circular, elliptical, square, diamond, and triangular pin fins.

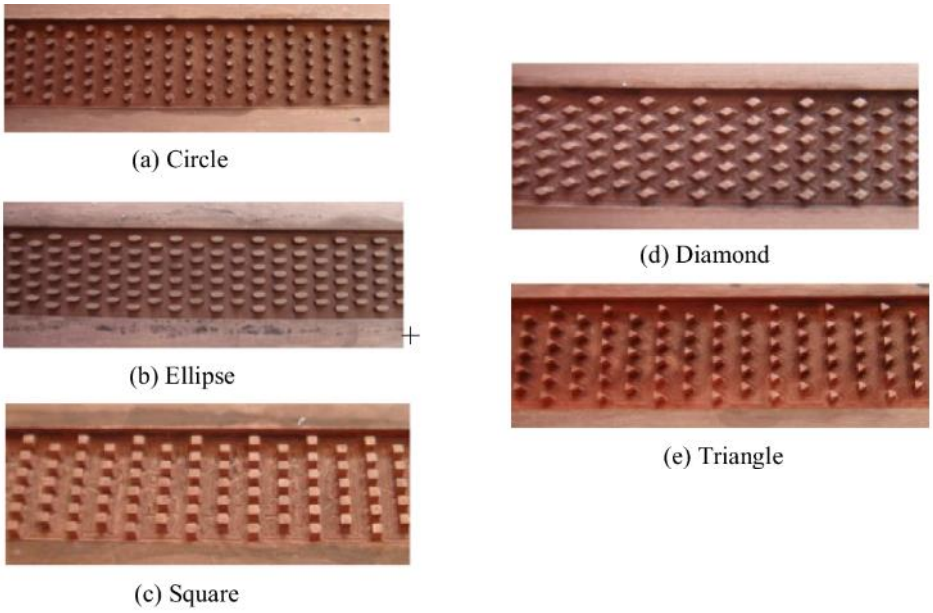


Figure 18 – Staggered Array Pin fins of (a) Circular, (b) Elliptical, (c) Square, (d) Diamond, and Triangle Geometries [40]

Chyu *et al.* [41] published work on the influence of pin fin spacing in staggered and in-line arrays for fillet and straight cylinders. The aluminum pin fins had a height to-diameter aspect ratio of 0.5 and 1 and the transverse (S_T/D) and longitudinal (S_L/D) each had spacing ratios of 2.5. The experiments were completed for Reynolds numbers between 5,000 and 30,000. The study concluded that a staggered pin fin geometry has a higher 'array-averaged HTC', thus making it a more promising geometry for micro cooler design.

Moores *et al.* [42] published a work showing the variation in cooling for various tip clearances. It was found that a tip clearance provided more effective cooling. His study explored tip clearances including: 0, 6, 12, 18 and 25% of the pin height. It was found that a tip clearance of 6% gave the greatest increase in Nusselt Number, thus a higher HTC increases to 25% significantly reduced the heat transfer in the cooler because of the introduction of coolant bypass at higher tip clearances. Thus, incorporating a tip clearance in a microchannel cooler could result in improved heat transfer.

Koşar *et al.* [43] completed a study of laminar flow across a bank of micro-pin fins of varying height to diameter aspect ratios between ½ and 8. The micro pin fins were arranged in an in-line and staggered arrangement and the Reynolds number ranged from 5 to 128. The experiments were conducted over circular and diamond shaped micro-pin fins using adiabatic conditions and no heat was supplied to the system. The heat sinks were fabricated using deep reactive ion etching (DRIE) and reactive ion etching processes. Various correlations for pressure drop and friction factor were explored and the paper concluded that conventional correlations do not work for micro pin fin geometries. It was also noted that the pin height-to-diameter aspect ratio has a significant effect on friction factor. However, as the Reynolds number increased, the height-to-diameter influence diminished. Furthermore, the microchannels with staggered arrays and diamond pin shapes were seen to have a higher friction factor than the in-line arrays and circular pin shape.

2.3.4.1 Aligned Fins

Aligned, or in-line fin geometries are more commonly designed and studied because of the ease of manufacturing such cooling designs, and the low manufacturing costs associated with this geometry. These designs arrange fins in equidistant rows spanning the length and the width of the micro cooler. Thus, the channels are manufactured by simply cutting channels into a metal block to design the heat sink. However, the aligned fin geometry has limited heat transfer capability. When introduced into the pin fin array, the coolant fluid forms boundary layers along the walls of the channel. As these boundary layers develop, the flow is guided in between the pin fins and relatively no mixing occurs. Thus, the pins are bypassed and the coolant could have little to no impact on the dissipation of heat throughout the channel. **Figure 19** gives a schematic of an aligned pin fin array.

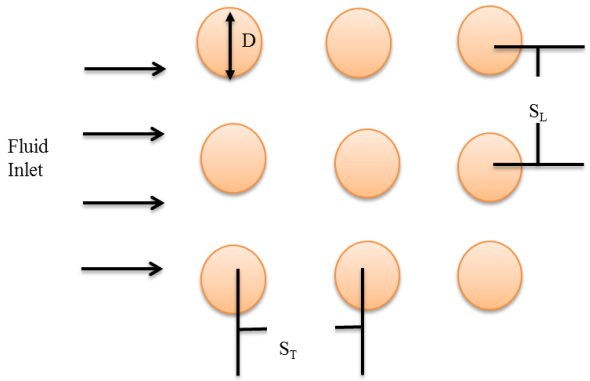


Figure 19 – Schematic of an Aligned Pin Fin Array

2.3.4.2 Staggered Fins

Staggered fins can be designed in an array of micro-pin fins or offset linear fins. Researchers have studied both array types, and it has been found that the heat transfer characteristics of each heat sink design vary based on the arrangement, fin packing density, and geometry of the fins. Staggered pin fin arrangements introduce mixing into a micro-pin fin cooler. This enhances heat transfer because the flow is broken up, and can cover a larger surface area. **Figure 20** gives a schematic of a staggered pin fin array.

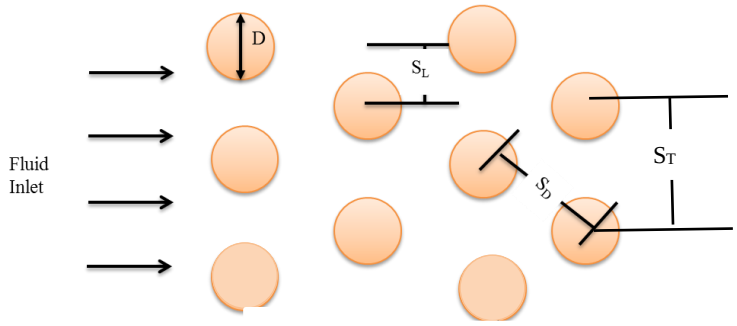


Figure 20 – Schematic of a Staggered Pin Fin Array

Khan *et al.* [44] studied an entropy generation minimization technique for optimizing pin fin heat sink designs. This three-parameter optimization considered heat sink resistance, pressure drop, and fluid properties. Testing over in-line and staggered pin fin heat sinks, it was found that the fin arrangements used different optimization parameters to achieve effective cooling. Correlations for these designs were developed by [45] for ranges of diameters, approach velocities and fin arrangements. It was found that there was lower entropy generation for in-line arrays. An optimum pin density could be determined for a staggered arrangement aluminum heat sink because of the existence of

an optimal entropy generation rate. An optimal entropy generation rate was not found for low thermal conductivity heat sinks. However, it was found that heat sinks with low and high thermal conductivities and high pin densities are still superior to other conventional heat sinks.

2.3.5 Microfabrication Techniques

Kandlikar *et al.* [46] explored microfabrication techniques that allow for flexibility in guiding the coolant to be concentrated in various hot spots of the microchannel cooler. This deep reactive ion etching (DRIE) technique allows for variation in microstructure features throughout the channel. Therefore, the channels can have areas of shorter fin lengths, aligned, and staggered fins. Variability in the fin heights and geometries allows for concentrated cooling. Concentration of the fluid allows for greater heat dissipation directly below the hot spots where the chips are located. Although this process improves the heat transfer in high heat flux cooling applications, this manufacturing scheme results in inaccuracies in the fin geometries and spacing. This occurs because of the inability to etch perfect angles, etc. **Figure 21** shows an SEM image of the DRIE manufactured heat sinks.

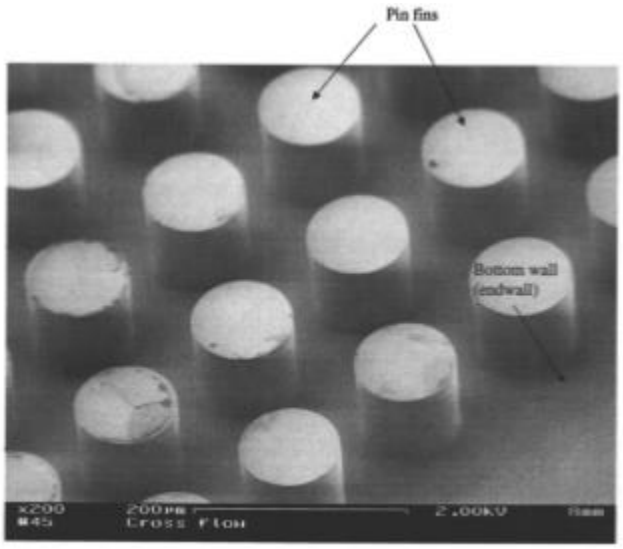


Figure 21 – SEM Image of Pin Fin Heat Sinks Manufactured with DRIE Methods [43]

2.3.5.1 Additive Manufacturing Technique

To combat accuracy issues associated with the above etching methods, an additive manufacturing technique has been introduced. 3D printing allows for flexibility in microchannel geometry while minimizing the inaccuracies from machining or etching. Although there are tolerances associated with 3D printing, the design uncertainty is lower than that of a conventionally manufactured channel design.

Chintavali *et al.* [16] developed an aluminum printed metal power module cooler for a 10kW SiC inverter. 3D printed modules are a promising technology because they allow for complex geometries and concentrated heating. The single sided cooler employs complex internal features and the printed aluminum was found to have comparable thermal conductivity to 6061 Aluminum. Manufactured using a fused deposition melting (FDM) process, the microchannel cooler also showed consistency in strength compared

to 6061 Aluminum. Furthermore, the performance of the inverter device with a printed aluminum cooler was comparable to the performance of a 6061 aluminum cooler. With the development of this additive manufacturing technology, there is new capability to print in various materials including: plastic, metals, and ceramics. **Figure 22** shows the additive manufacturing heat sink developed by Chintavali *et al.* [16]

Figure 22 – Power Electronics Module mounted to 3D printed Metal Heat Sink [16]

2.3.5.2 Double-Sided and Multi-Layer Cooling

Double-sided coolers were developed on the premise that applying cooling to both surfaces of power electronic devices will allow for more efficient device cooling and increased heat transfer rate. This cooling technique has also been explored for more rapid efficient cooling of power electronic devices because it allows for stacking of multiple devices.

Wei *et al.* [47] published a work on stacked microchannel techniques and found that because the coolant could flow in opposite directions, the temperature control through the heat sink could be improved. The paper also suggested that a two-layered microchannel resulted in a decrease of thermal resistance of approximately 30%. Testing

both parallel flow and counter-flow geometries, it was found that the total thermal resistance was lowered, but there were significant increases in pressure drop.

O'Keefe *et al.* [48] analyzed three package designs—Baseline (BL), Direct Backside Cooling (DBSC), Integrated Heat Sink (IHS)—varying the coolant choice, coolant temperature, semiconductor temperature, effective convective HTCs, and thermal interface materials for IGBTs [48]. The power module used in the work incorporated one IGBT and two diodes. Each single-sided cooling design assembly was also compared to a similar double-sided cooling design with similar BL, DBSC, and IHS configurations. For the work, a heat flux dissipation target of 200 W/cm^2 was set. This value was the accepted goal for the FreedomCAR program based on a Toyota Prius 50 kW traction motor inverter. Overall, the study found that the IHS design had an improved heat dissipation potential over the other designs for use at lower convective HTCs due to its effective heat spreading and use of surface area [48]. The low heat dissipation capability of the BL design was attributed to the changes in the thermal resistance for the interface material. This impact was better identified at higher values of the convective HTC [48]. The results of the double-sided cooling configurations suggested that the double-sided cooling method outperformed the single-sided cooling for each design assembly. **Figure 23** shows the difference in single-sided and double-sided cooling configurations with their respective resistance networks.

(a)

(b)

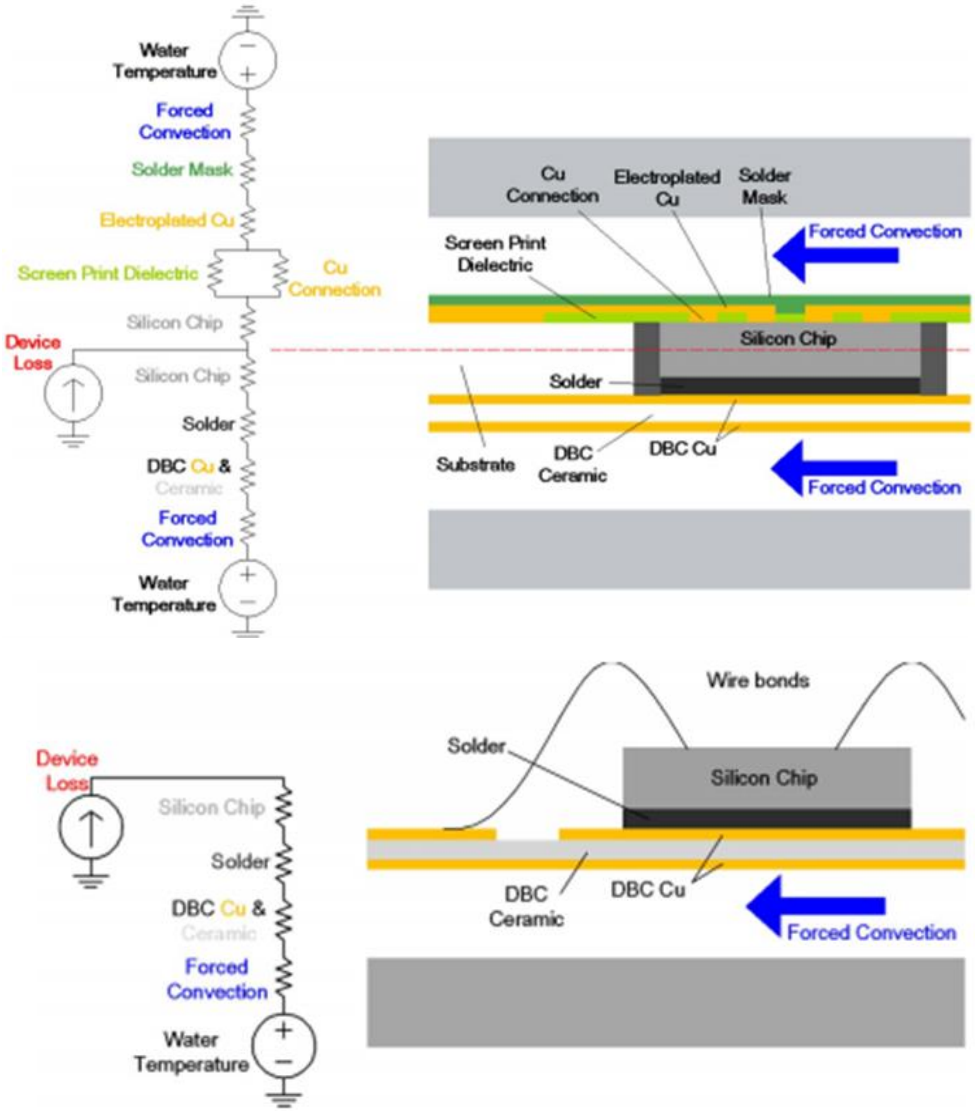


Figure 23 – Power Electronics Module with (a) Double-Sided Cooling, (b) Single-Sided Cooling [49]

Schulz-Harder [50] reviewed numerous solutions for power electronic device cooling. The paper explored thermal greases and the materials for other power electronic device layers, stacked in-line cooling, double-sided cooling, and the use of metal base plates for cooling. The heat sink design was determined to be the second most influential in achieving high thermal resistances after the removal of the thermal grease layer. The

cooling options include a base plate liquid cooler with direct integration of the cooler into the direct bond copper (DBC) substrate, a double sided cooler, and stacked microcoolers. A double-sided cooling technique helps reduce the size of the cooler, and coupled with a jet impingement scheme, this method could help reduce the overall pressure drop. The double-sided technique mentioned in this work was designed with pins on the two backsides of a sandwich stack with a jet impinging on each side. This reduced the weight of one device from 56 kg to 3 kg. The two interlayers were isolated using ceramics and an overall power density of greater than 50 kW/l was achieved for a 1100 kW/l power module for 5% of the total inverter volume.

2.3.6 Limitations in Linear Channel Cooling

Much work has been done in the area of linear channel cooling. This technique has proven effective, but there are limitations met with these designs such as: pumping power, micro-pin fin offset fluid flow, and manufacturing considerations.

2.3.6.1 Pumping Power

Liquid cooling schemes can have an additional design challenge over air-cooling schemes due to pumping power. Pumping power is the power required to pump the fluid through the cooling loop for effective thermal management. Pumping power is an important consideration because a higher pumping power could increase the power requirements of the vehicle or cooling system, and further limit the amount of power that can be used by the power electronic device. The pumping power for an electronics cooling system is determined via equation 1

$$W_{pump} = \Delta P * \dot{V} \quad (1)$$

where, ΔP is the pressure drop in the system, and $\dot{V}$ is the volumetric flow rate to effectively cool the system. As the flow rate and pressure drop are inversely proportional in this equation, the pressure drop must be minimized to maintain the same volumetric flow rate yielding a lower pumping power. Tuckerman *et al.* [12] suggest that fundamental limits on channel size are of greater consideration when the pumping power reaches comparability to the power dissipation generated from the circuit. Although this is more common at higher pressures, this limit serves as a measure of the influence of pressure drop. The pumping power is especially important in micro-channel design because if the design is such that there is a high pressure drop, the pumping power requirements will be greater and the energy consumed in operation limits the power that could be supplied to improving the fuel efficiency of the car. Furthermore, a lower pumping power will reduce the maintenance needed for the pump over time.

2.3.6.2 Micro-pin Fin Offset Coolant Flow

The offset coolant flow occurs in the areas outside of the pin and plate fins. As the coolant enters the channel, the fluid moves across the boundaries and often seeks out areas of least resistance. Once these sections are found, more coolant migrates to these areas and the fluid can begin to move away from the areas of high heat.

To combat the offset in fin arrays, designs have been developed to include pins along the walls to interrupt the flow and guide it back towards the hot spots, thus improving overall heat transfer. As the fluid develops vortices and eddies in the channel,

the heat transfer rate improves significantly because of the flow mixing allowing the fluid to cover a greater surface area.

2.3.6.3 Manufacturing Challenges

As these devices are developed on a small scale, the cost of manufacturing is much greater compared to macroscale designs. To meet the size and weight goals of the industry, the heat sink coolers are often built to be much larger than the power electronic devices. However, to more effectively meet design expectations, the heat sinks must be built to mitigate accuracy concerns that impact the time to machine and build the parts, while being able to concentrate the cooling at localized hot spots. This results in high costs to the manufacturer and consumer. There are also concerns with microchannel clogging when other coolants such as ethylene-glycol-water are used in linear cooling designs [35]. This usually results on the need for a microchannel filtration system.

2.3.7 Horizontal Cooling Objectives

From the literature, it has been seen that the thermal cycling and thermal stresses developed in power electronic devices often generate device failure, and reduced performance of the devices. Numerous cooling methods have been studied to address these thermal challenges, such as cold plate cooling, base-plate cooling and double sided cooling. As integrated heat sinks have been found to be a more effective cooling strategy, this work seeks to apply integrated cooling techniques to effectively dissipate the heat from a power device. Research has also shown that finned heat sinks enhance heat transfer because of the increase in heat transfer surface area they provide in addition to the encouragement of mixing in pin fin heat sinks. Thus, the integrated cooling systems

developed in this work will incorporate micro-structure features to enhance heat transfer from the power devices. The main inhibitor of effective heat dissipation is thermal resistance. From the literature, it has been found that the thermal resistance limits effective cooling because of the interface materials needed to provide device mechanical stability. Furthermore, as these materials start to degrade overtime, the ability of the power device to operate with many cycles is limited. Thus, this work explores the feasibility of eliminating the some of the device package layers that contribute to this high thermal resistance and bringing the coolant closer to the chip.

2.4 Vertical Cooling Methods

Vertical cooling techniques have been developed to avoid pressure drop issues and combat other issues identified in the horizontal cooling section. Vertical cooling is used to describe fluid flow that moves perpendicular to the heat flux surface. Researchers have explored vertical impingement on flat surfaces, enhanced surfaces and on micro-structured surfaces. There has also been work completed in the area of boiling jet impingement heat transfer. Each of these methods has been deemed effective in providing cooling for power electronic devices and they typically generate higher HTCs than microchannel coolers. However, there are some limitations in vertical cooling methods such as non-uniform temperature gradients, the development of spent flow regimes that counteract the effects of the impinging jet, and clogging in a spray cooling technique.

2.4.1 Jet Impingement

Jet impingement is a cooling technique used to improve the heat transfer rate in cooling systems. The jets may be used to dissipate heat from flat, enhanced, or micro-structured surfaces. Impingement cooler designs are usually either a single jet or an array of jets, and there are a few considerations for this technique. In jet impingement, as the fluid flows from the nozzle to the surface and across the surface, thermal and hydrodynamic boundary layers form on the orders of 0.1 and 0.01 mm, respectively [51]. These boundary layers form due to the changes in fluid pressure and deceleration of the fluid in the jet stream [52]. This generates high HTCs in the stagnation zone. **Figure 24** gives a schematic of a jet impingement cooling scheme for electronics cooling.

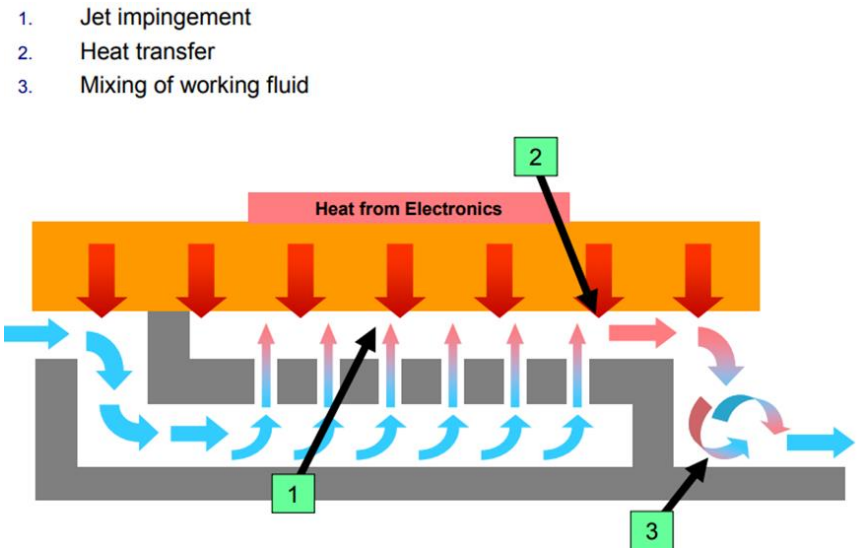


Figure 24 – Schematic of a Jet Impingement Cooling Scheme [53]

There are numerous jet designs, such as circular and rectangular jets, and the jet configurations can be either a free-surface jet, submerged jet, or confined jet. A free-surface jet is a jet where the liquid comes into direct contact with a gaseous environment when it leaves the nozzle. A submerged jet is developed when the fluid in the jet operates

under the same conditions as the ambient fluid (i.e. liquid jet flows into a liquid ambient environment). A confined jet is one where the jet is confined between a nozzle and a heated wall [54]. **Figure 25** gives a schematic of the various regions that develop in jet impingement.

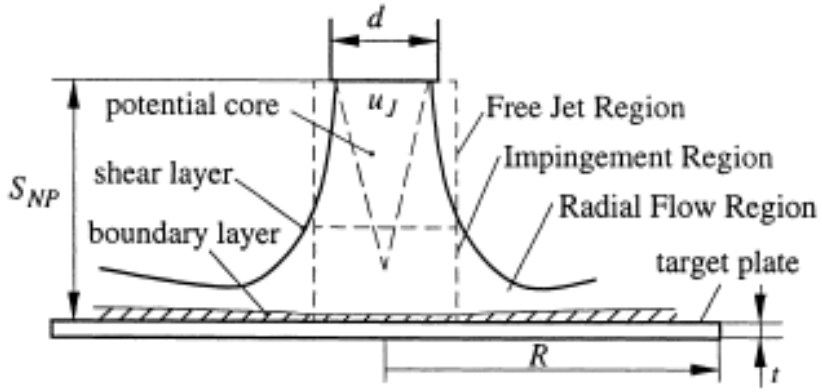


Figure 25 – Schematic of Impingement Regions [52]

2.4.1.1 Free-Surface and Submerged Jet Impingement

In a free-surface jet, the stagnation zone is developed as a result of the jet fluid decelerating and accelerating normal and parallel to the impingement surface [51]. As flow moves beyond the jet, it interacts with three regions: free jet region, impingement region and the radial region. The free jet region is subdivided into two zones: potential core and shear layer. In the potential core, the velocity of the fluid is equal to the jet exit velocity. The shear layer begins to form as the fluid moves downstream of the nozzle. Thus, the potential core velocity is offset and the fluid flows into the centerline region of the jet. In the shear layer, the velocity of the fluid is much lower. **Figure 26** gives a schematic of a free surface jet and a submerged jet.

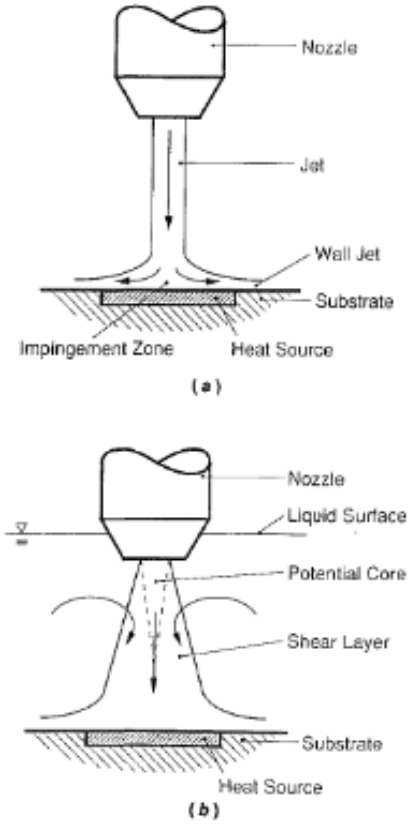


Figure 26 – Schematic of a) Free-Surface and b) Submerged Jet Configurations [55]

2.4.1.2 Influence of Spacing on Heat Transfer

According to Lee *et al.* [52], the impingement region is approximately 1.2 nozzle diameters away from a surface, and the flow decreases in the axial direction and increases in the radial direction. This relationship gives a high HTC in the relationship: h $\propto \sqrt{\frac{u}{d_n}}$. Where u is the axial velocity, and is the d_n nozzle diameter [52].

The radial region is the region closest to the impinging surface plate where the flow increases in the radial region and decreases in the axial region. The nozzle-to-plate (S_{NP}) spacing relative to the potential core also influences the HTC. Lee *et al.* [52] found that when the S_{NP} is less than the potential core length, the impingement region velocity

is often the same as the velocity from the nozzle. Thus, the HTC will be constant regardless of the S_{NP}. When the nozzle-to-plate spacing is greater than the potential core length, the velocity decreases with increased spacing, and the heat transfer coefficient is lowered.

There were a few other geometric parameters Lee *et al.* [52] suggested influence the average heat transfer coefficient over an impingement surface including: the distance from the jet centerline to the end of the jet target plate, the relative nozzle area (ratio of nozzle exit cross sections to surrounding area corresponding to a single jet), the jet diameter, spatial arrangement of the nozzles and the jet velocity. The paper referenced Martin [56] and listed correlations for calculating the Nusselt and Reynolds numbers.

Lee *et al.* [52] also discussed the impact spent flow has on the thermal performance of a multi-jet impingement cooling devices. The spent fluid is the fluid that flows outward from the exit of the impingement surface, or upward through outlets in between the nozzles. The paper suggests that without control of the spent flow, the heat transfer rate is reduced. This occurs because as the spent flow region develops, there is greater influence of crossflow. The crossflow hinders heat transfer by deflecting the jet and dispersing the impingement momentum. When designing an optimal jet impingement configuration, Lee *et al.* [52] suggests that the nozzle diameter, nozzle-to-nozzle separation, and nozzle-to-plate spacing should be considered for maximizing heat dissipation. There should also be constraints placed on the pumping power and nozzle-to-plate spacing while minimizing cross flow effects. **Figure 27** gives a schematic of a multiple jet impingement array.

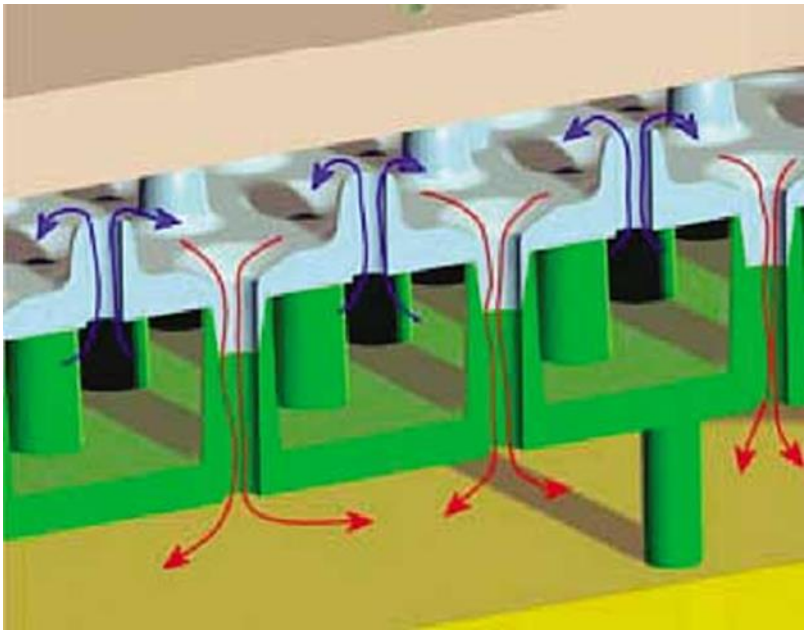


Figure 27 – Schematic of a Multi-Jet Array. (The red arrows indicate the flow of liquid from the inlet manifold of the jet array, and the blue arrows show the flow of fluid from the microchannels (dark green) to the inlet manifold) [57]

Fabbri *et al.* [58] studied methods of optimization in heat transfer for free-surface micro-jet power electronic cooling. The experimental study tested ten arrays of micro-jet coolers with jet diameters from 60-250 μm and Reynolds numbers between 73 and 3813. Through the study, maximum surface heat fluxes of 310 W/cm^2 were found using water jets on a less than 20 mm diameter copper surface. The plates used in the experimental apparatus were laser drilled for the jet holes, and the test setup employed a copper cylinder to simulate an electronic microchip. It was found that the pitch (spacing) of the jets impacted the impingement of the jets and some rings in the system hit the enclosing surface rather than the copper surface. In determining the optimal jet configuration, many parameters such as nozzle diameter, nozzle- to-heater distance, and the number of jets were considered. From this, it was found that the optimum jet diameter increased with

increases in pitch. The paper concluded that the Nusselt number improved with an increase in Reynolds number and Prandtl number with a decreasing ratio of jet pitch to jet diameter. Fabbri *et al.* [58] was able to design an optimal configuration that gave a pumping power of 2.53 E-2 W, with jet spacing of 2 mm and jet diameter of 325 μm. Lastly, it was found that at a constant flow rate, the configuration with the highest heat removal rate had the largest number of small diameter jets. Therefore, a multiple jet design may be more promising for microchannel jet impingement cooling.

Womac *et al.* [55] compared correlations between multiple free surface and submerged jets with nozzles in 2 x 2 and 3 x 3 arrays of straight tubes. The experiments used water and a fluorocarbon liquid (FC-77). Tests were run over a Reynolds numbers between 500 and 20,000 and volumetric flow rates between 0.2 and 5 liters/min. Womac *et al.* [55] also characterized unit cells for the multiple jet arrangements by determining different heater lengths for free surface and submerged jets.

For the free surface jet configuration, Womac *et al.* [55] found that the highest average heat transfer coefficients were found in arrays with the smallest nozzle diameter and fewest number of nozzles for a given volumetric flow rate. For both configurations, the experiments run showed that the heat transfer coefficient decreased with decreasing volumetric flow rate, and the influence on the heat transfer coefficient was more noticeable when the thermal boundary layer met the free-surface of the jet. In a submerged jet configuration, Womac *et al.* [55] noted that the momentum of the jet shifted from the jet tip to the ambient region. When the volumetric flow rate was fixed, the HTC increased as the number of jets, nozzle diameter and effective heater length decreased.

Maddox *et al.* [59] published a work on design optimization for jet impingement coolers. The article suggested that the most significant ratios in jet impingement design that influence heat transfer rate are: the jet aspect ratio (jet length/jet diameter) and jet area ratio (nozzle diameter/ heater area). It was found that as the jet diameter decreased, there was an increase in flow velocity. This influenced the heat transfer coefficient and flow rate constraints. Maddox *et al.* [59] also observed that the relationship between velocity and diameter varied inversely. Thus, the fluid velocity was increased as a direct result of a decrease in jet diameter. The article concluded that an increase in the number of jets would decrease the velocity and jet diameter, thus improving the pumping power. Therefore, a multi-jet cooler design may be a more promising method for effective heat dissipation. The article referenced Martin [56]. Martin *et al.* [56] determined an optimal jet array and suggested that an increase in the number of jets substantially reduces the required pumping power. Furthermore, an increase in Nusselt number resulted in an increase in the Reynolds and Prandtl numbers.

2.4.1.3 Influence of Variations on Jet Impingement Surface

Narumanchi *et al.* [60] published a work exploring jet impingement with water-ethylene glycol as a design solution for a light-weight, low-cost, single-phase, liquid-cooled heat exchanger compared to conventional heat exchangers. Narumanchi *et al.* [60] studied flow in a channel, jet impingement on plain surfaces and jet impingement on micro-finned surfaces using CFD modeling, and it was found that the pressure drop in the channel flow was lower than in the jet impingement designs, and the pressure drop did not change with or without the microfins. It was also found that the thermal resistance was lowest in the micro-finned impingement configuration, followed by the plain surface

impingement, and then the channel flow. The temperature uniformity was greatest for the linear channel design. The paper concluded that through a jet impingement scheme, the heat sink performance could incur an increase in the COP of approximately 71% with a 79% increase in power density and a 118% increase in specific power when compared to the conventional linear channel. Thus, an impingement design could be more promising for high heat flux applications for a lower cost than conventional channels.

Ndao [39] published work assessing the differences in multi-optimization liquid cooling using linear and vertical cooling. The jet impingement work was found to be the most optimal design to use because it avoided the pressure drop challenges and provided more direct cooling over the surfaces. The study explored jet diameter, the ratio of jet-to-jet spacing to jet diameter, heat transfer area, and the ratio of the distance between the orifice plate and impingement surface to jet diameter parameters. It was found that the heat sink performance was increased with the use of multiple jets and the work was in good agreement with the above literature in that the heat transfer coefficient was found to be high at the stagnation zone, and dissipated as the flow moved from the stagnation point. The article concluded that the heat transfer area impacted the jet impingement cooler performance, and that the jet impingement cooler performed better or worse than the microchannel cooler depending on the heat source base area. Moreover, it was found that the impinging jets performed comparably to the circular pin-fins at high pumping power even with a smaller heat transfer area.

Ndao [61] explored the heat transfer properties of different micro-cooler designs including (square, elliptical, hydrofoil, and circular micro-pin fins). Each micro-cooler geometry was experimentally tested using jet impingement and flow boiling heat transfer

techniques for high heat flux microelectronics. The silicon-based heat sinks were manufactured using thin film deposition, photolithography, etching, chemical mechanical polishing (CMP), bonding and dicing [61]. Refrigerant R-134a was used as the cooling fluid, and the single jets impinged onto 2 x 2 mm micro pin fin arrays while varying the jet velocity. The parameters compared for each design were: the heat flux, jet velocities, pin fin geometry, and pin-fin array configuration. It was found that the micro pin fins enhanced the heat transfer in impingement cooling devices and heat fluxes of approximately 450 W/cm^2 were expected for thermal resistances of 0.11 cm^2-K/W. Moreover, it was found that the circular and square pin fin arrays produced a higher heat transfer rate than that of the elliptical and hydrofoil designs. With the addition of multiple jets, the heat transfer rate could be improved even more. **Figure 28** provides a schematic of the jet impingement test section developed in this work.

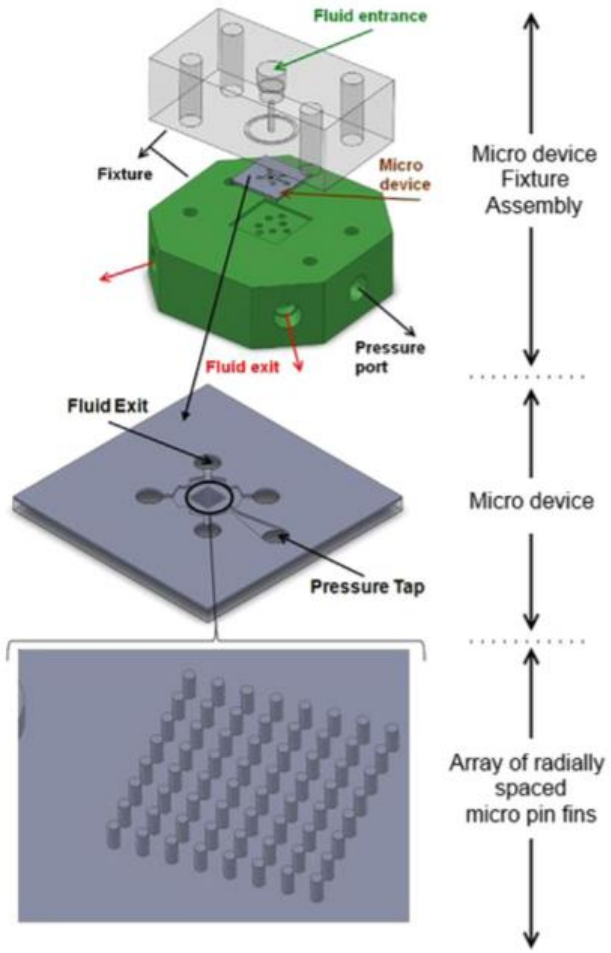


Figure 28 – Schematic of Jet Impingement Cooling on Microstructure Enhanced Surfaces [61]

Moreno *et al.* [62] published a work on single-phase jet impingement on square pin, microporous and radial finned surfaces. Submerged and free-surface jets were used on the geometries manufactured in oxygen-free copper plates. Experiments were run over Reynolds numbers of 3,300 to 18,700. The test sections were powered using a resistance heater at 70 W (55 W/cm^2). As the Reynolds numbers were increased, the Nusselt number increased to over 1000 in the base case flat plate impingement design. In the free surface jet configurations, the microporous surface (enhanced using a sandpaper technique) achieved the highest Nusselt number of over 2000, while the base-case plate

achieved the lowest Nusselt number. The surface enhancement in the free-jet configuration increased the heat transfer capabilities by approximately 130% over the base-case flat surface. In the submerged jet configurations, the surface enhancement did not have significant effect on the heat transfer in the Reynolds number range explored. For the submerged jets, the radial pin fins performed the best, followed by the square pin fins, and micro-enhanced surfaces.

2.4.2 Jet Impingement Manufacturing

2.4.2.1 Commercial Manufacturing

Currently, many jet impingement devices are made using a laser cutting or drilling technique for jets. The manufacturer simply designs a pattern and machines holes to insert the fluid in a top-down or bottom-up fashion. As the jet forms, there are crossflow considerations that impact the heat transfer rate of the impingement cooler. To combat this issue, some researchers have designed cooling chambers with tapered holes to better guide the flow. However, studies show that this is not enough to fully enhance the heat transfer in the cooling devices.

Kercher *et al.* [63] completed a study on miniature synthetic jets. The work was motivated by the possible elimination of pumps, and the need for a fluid source. These jets eliminate the need for a pump and fluid source because a gathering and dispersing process of the fluid create the jet. This avoids the need for input piping and reduces the complexity in the packaging. The jets are designed using a cavity that is bound on one side by an orifice and on the other by a flexible membrane [63]. Therefore, a momentum transfer is generated in the surrounding fluid without a net mass injection. An orifice

plate was used to secure the membrane, and diameter of the orifice plates varied from: 1.98 mm to 2.78 mm. For a 12.5 mm diameter and 25 mm diameter micro-jet device, the power used was approximately 200 mW. In experiments run over a 2" heater test piece, the synthetic jets were seen to produce heat transfer coefficients between 24.19 and 411.16 W/m^2-K. **Figure 29** shows the differences between the synthetic jets studied in this work.

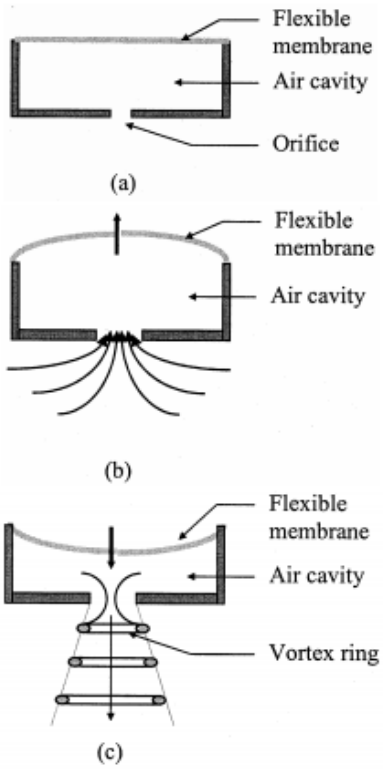


Figure 29 – Schematic of the Synthetic Jets Designed to Eliminate the Need for Pumping [63]

2.4.2.2 Additive Manufacturing

An additive manufacturing scheme could better guide the flow to mitigate the problems associated with the spent flow in an impingement device because of the

flexibility of designs and the ability to 3D print complex geometries. These designs can help guide the flow more rapidly to apply concentrated cooling to various hot spots of high temperature from the chip in operation and improve overall heat transfer. Material properties such as thermal conductivity can also be achieved with an additive manufacturing technique as more materials are developed for 3D printing.

2.4.3 Spray Cooling

Spray cooling is another vertical cooling technique that has been studied because according to Anandan *et al.* [31], the thermal resistance developed in the bonding layer between the heat source and the heat spreader is eliminated by a direct spraying onto the heat source. Anandan *et al.* [31] also suggests that the ratio of power spent in cooling and heat removed decreases at a more rapid rate than it does for a channel cooling technique. The method is completed using either liquid jets or liquid droplets, and the cooling fluid meets the power electronic devices through nozzles or orifices. Spray and jet impingement cooling techniques differ in the way the fluid hits the surface. The spray impinging onto the surface forms a thin liquid film because of the pressure drop across the nozzle. As the fluid touches the surface, boiling occurs because of the heat dissipated by the equipment. **Figure 30** provides a schematic of spray cooling and jet impingement respectively.

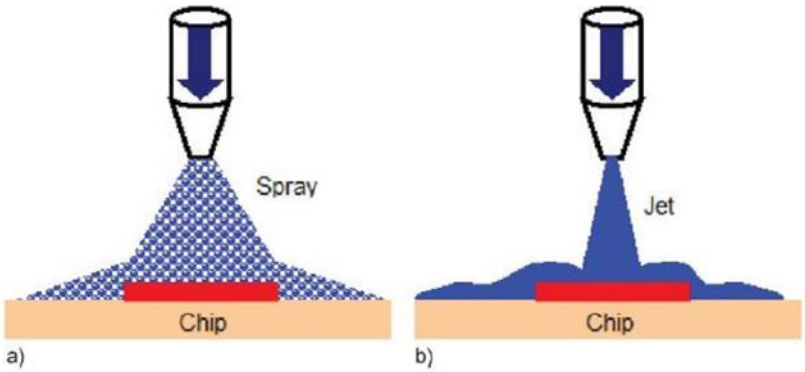


Figure 30 – Schematic of Jet and Spray Cooling on a Chip [64]

Mudawar [65] published a work reviewing multiple cooling schemes such as two-phase heat transfer, jet impingement, spray cooling, etc. for high heat flux electronic devices. According to Mudawar [65], spray cooling is divided into two regions: pressure sprays or atomized sprays. The pressure spray supplied the coolant at a high pressure in a small opening. The atomized spray uses high-pressure air to help breakup the coolant sprayed onto the cooling surface. Thus, Mudawar [65] suggests that spray cooling techniques minimize the flow rate needed for cooling, but induce a higher pressure drop. The spray cooling devices studied by Mudawar [65] were found to dissipate more than 100 W/cm^2 by using dielectric coolants notorious for having low thermal transport characteristics.

Mudawar *et al.* [54] studied two-phase spray cooling using coolant HFE-7100 as a method to combat thermal management issues associated with power electronic devices. Mudawar *et al.* [54] suggested that spray cooling is in demand for high heat flux cooling because of how the sprays employ liquid momentum rather than using secondary air to disperse the liquid into small droplets. While maintaining device temperature below 125℃, a spray cooling technique has been found to dissipate between 150-200 W/cm^2 in hybrid electric vehicle configurations.

2.4.4 Comparison of Jet Impingement Techniques to Microchannel Heat Sinks

Lee *et al.* [52] compared microchannel coolers to jet impingement designs to determine the parameters that influence heat transfer. In microchannel cooling, it was found that these designs usually have high pressure drop while maintaining a low volumetric flow rate. A jet impingement configuration exhibits the opposite trend where the coolers usually have low pressure drops and high volumetric flow rates. The paper concluded that when the spent flow is treated properly, the jet impingement technique is comparable to microchannel cooling. It was found that the jet impingement heat flux is greater than that of the microchannel cooler when there are larger target dimensions. When there are smaller target dimensions the trend is reversed.

Robinson [66] completed a thermal-hydraulic comparison of impinging jets to laminar flow microchannel arrays. Robinson [66] tested over 2 x 2 cm square-shaped devices dissipating a heat flux of 250 W/cm^2. The devices used a pumping power of less than 0.1 W for both methods. The dimensionless jet-to-jet spacing ranged from 3 to 7. The jet-to-target spacing ranged from 2 to 3. The heat transfer coefficients over volumetric flow rates from approximately 0.5 to 3.75 lpm ranged from less than 20,000 to over 100,000 W/m^2-K. Similar trends to Womac *et al.* [55] and Lee *et al.* [52] were found between the flow rates and pressure drop for each design.

In the impinging jet configuration, a higher flow rate produced a uniform temperature distribution, and occupied much less space compared to microchannel coolers. Robinson [66] concluded that liquid jet impingement devices show better thermal performance as the jet diameter and jet population are decreased because of the

increased jet velocity. It was also found that a reduction in jet diameter with an increase in the number of jets resulted in reduced pumping power. Lastly, in the microchannel geometry, it was found that there is significant sensitivity to any changes in the hydraulic diameter. When comparing costs, it was estimated that a jet impingement design would be more cost efficient because the simplicity of drilling or punching holes, etc. resulted in a reduction in manufacturing costs.

2.4.5 Limitations in Vertical Channel Cooling

Vertical channel cooling has been found to have much higher pressure drops than linear channel devices while improving the heat transfer coefficient in cooling. However, some studies have shown that there is great dependence on the heat transfer area, number of jets in an array, amongst other parameters that can cause a jet impingement scheme to perform better or worse than a conventional microchannel heat sink.

The cost of a jet impingement device can also be much less than the cost of a microchannel cooler, which makes it a more promising option for high heat flux applications. With the limited literature available about single-phase vertical cooling schemes, there is much room for study in this area and improvement in jet impingement design.

In the area of spray cooling, Mudawar [65], jet impingement designs concentrate the heat dissipation in the impingement region, and induce large temperature gradients. Mudawar [65] also suggests that spray cooling has not been adopted because the complex features in the cooler nozzle design increase the possibility of clogging in the heat sink.

There is also concern that there is limited predictability and repeatability if spray nozzle designs are not tested periodically.

2.4.6 Vertical Cooling Objectives

From the literature, it has been seen that jet impingement cooling methods produce high heat transfer coefficients as compared to horizontal cooling schemes. The highest heat transfer coefficient values are found at the stagnation zone (center of the jet on the impingement surface). To realize the potential of jet impingement cooling methods, some parameters must be optimized for effective jet cooling. Such parameters include: the jet height-to-diameter aspect ratio, jet-to-jet spacing, and length of the impingement surface. As each of these parameters are interdependent, there are tradeoffs that arise in designing jet impingement cooling schemes. Some researchers have applied jet impingement methods to micro-structured surfaces. The expectation of this approach is that the heat sinks will get the benefit of both the jet impingement and the micro-structures that enhance heat transfer. For this work, jet impingement schemes will be applied to flat plate (unstructured) DBC substrates. Different jet array test coupons will be developed to compare the influence of the jet design parameters on the effectiveness of the cooling technique.

2.5 Warpage Challenges and Device Mounting

Conventional power electronics package and printed circuit board manufacturing processes are often met with the challenge of warpage in the device package. This warpage is usually induced in the direct-bond copper (DBC) substrate due to the CTE

mismatch found in the materials [20]. Many researchers have explored the impacts of warpage when these electronics packages are developed.

Zhou *et al.* [20] completed a study to identify a new method to reduce warpage in IGBT modules. According to Zhou *et al.* [20], warpage in IGBT modules occurs during reflow of the solder during attachment. If this warpage is less than 50 μm, it is acceptable in the IGBT industry. To combat warpage challenges, manufacturers often pre-warp the copper plates before developing the device package. The work by Zhou *et al.* [20] suggests that the impacts of warpage can be reduced through the development of an integrated base plate manufacturing process. In this process, the copper base plate is made thicker than the bottoms plate in a conventional DBC stack. This increased thickness allows for the material to better absorb some of the stresses induced in manufacturing the substrates. The work by Zhou *et al.* [20] suggested that using an integrated base plate (IBP) method with pre-warped copper significantly reduces the warpage effects during reflow of the solder material. However, the manufacturing time and cost were much higher for an IBP design as compared to the conventional DBC substrate stack. **Figure 31** shows the impacts of warpage during reflow on a power electronics module.

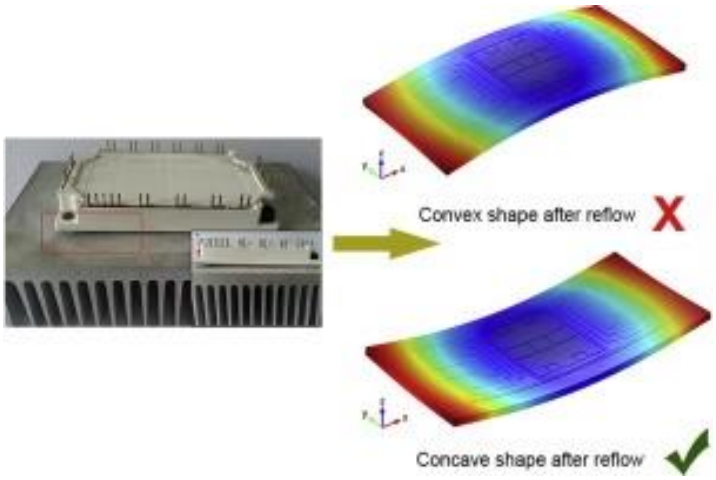


Figure 31 – Impacts of Warpage on Pre-Warped and Un-Warped Power Substrate After Reflow [67]

The mounting process for each chip in the power electronics module can also impact the warpage and reliability of the devices. In a study completed by Yu *et al.* [68], the diodes and chips were mounted to the copper substrates using a "pressure-less silver-sintering process". As Yu *et al.* [68] was developing a multi-chip embedded printed circuit board (PCB) method, the same mounting process was used for each of the diodes. First, the silver paste was screen-printed to a thickness of 50 μm. Following this, the dies were placed on the paste using a JPF Microtechnic PPOne die bonder with a force of 0.1 N applied to the die [68]. Following this, the paste was dried at 85℃ for 30 minutes. Then, the paste was sintered with a fast ramp-up to 240℃ and maintained there for 30 minutes before the die and paste are cooled down naturally. This process allowed for the development of the embedded die method studied for the work, and the screen-printing process is one that is commonly used for device mounting.

CHAPTER 3. METHODOLOGY

This chapter covers the experimental and numerical methods used throughout the horizontal and vertical cooling schemes. First, the directly integrated cooling of electronics (DICE) methods are reviewed. Then, the microcooler design analysis, and the heater design are reviewed. Following the design analysis, the experimental test set-up, calibration methods, and experimental methodology for both the horizontal and vertical cooling schemes is reviewed. Next, the numerical modeling inputs and references are detailed for both the horizontal and vertical cooling schemes. Finally, a brief numerical study of warpage impacts in manufacturing of the DICE stack is reviewed.

3.1 Directly Integrated Cooling of Electronics (DICE)

To mitigate the thermal resistance and heat dissipation challenges associated with numerous device layers, this study applies DICE methods that reduce the stack and move the cooling fluid closer to the chip. This allows for more effective heat dissipation, reduces the size and manufacturing requirements for the power modules. **Figure 32** gives a schematic of the size reduction in power device stack.

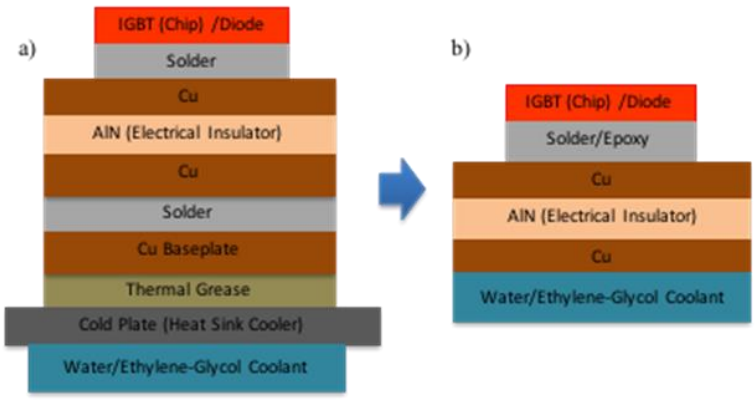


Figure 32 – (a) Conventional Power Electronic Device Stack and (b) DICE stack

Building the microcooler heat exchanger directly into the DBC eliminates the need for a baseplate, a cold plate, and more thermal interface materials. With this, the device stack is significantly reduced and the size and weight of the power electronic device are minimized. A schematic of a power electronics module with heat transfer enhancement features is given in **Figure 33**. With this novel DICE method, it is expected that complex heat sink geometries can be built into the heat sink area to address localized and uniform heat flux areas.

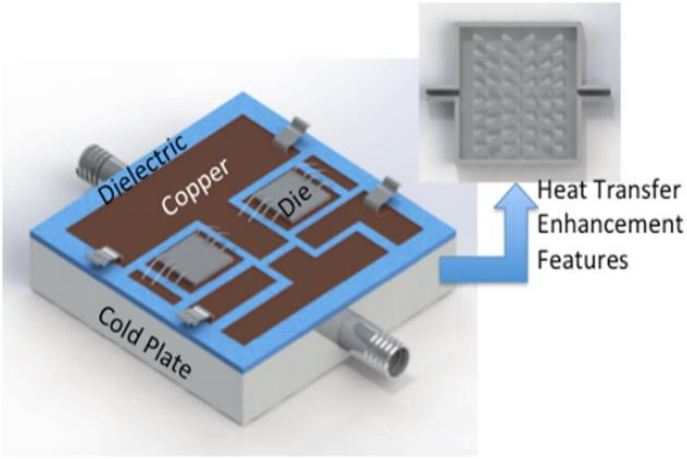


Figure 33 – Schematic of DICE Power Module with Heat Transfer Enhancement Features

The present work explored the effects of varying different design parameters in the micro-structure heat sinks including: pin fin arrangement, fin heights, fin diameter, longitudinal and transverse spacing, tip clearance, and fin geometries using various manufacturing techniques. Through this work, the expected package thermal resistance (with an estimated spreading resistance) is approximately 0.53 K/W for a HTC value of 10,000W/m^2-K at an ambient temperature of 26.85°C. This represents a 25% decrease in package thermal resistance over a conventional stack with thermal resistivity of 0.7 °C/W/cm^2 [11]. The DICE stack also occupies a thickness that is 1/5 the thickness of a conventional stack. To determine the actual performance of the DICE concept, there were

three validation techniques: experimental, analytical and numerical. Straight channels, linear flow channels and vertical cooling methods were explored.

3.2 Micro-cooler Design

This section reviews the pseudo-optimization method used to develop the micro-pin fin and linear channel heat sink designs. The parameters considered for the heat sink designs were pressure drop, heat transfer coefficient, fin efficiency, heat sink efficiency, and thermal resistance. Following the review of this heat sink design analysis, manufacturing methods are considered and reviewed. Then, final heat sink designs are tabulated and the potential microchannel heat sink enclosure designs are detailed.

3.2.1 Micro-Pin Fin Heat Sink Geometry

In pin fin microchannel heat exchangers, the pressure drop is commonly calculated through considering the number of pin fin rows, the maximum velocity, density of the fluid, and friction factor. In a duct, the friction factor is determined from the surface roughness of the duct compared to the diameter of the duct. In a microchannel heat exchanger, this friction factor is based on the manufacturing of the micro pin fin heat sink, and the overall geometry of the channel. As such, many researchers have developed correlations for the friction factor used in pressure drop equations. This work explored a few of these correlations and compares this data to experimental and numerical tests.

To aid in the designing of micro pin fin heat sinks, this work reviewed the work of Chyu *et al.* [41] and Moores *et al.* [42] that discussed the importance of the pin fin spacing, pin height and offset in a microchannel heat sink. To assess the performance of

each pin fin array, an analytical model exploring multiple objectives was applied to determine which designs would be better for increasing heat transfer.

3.2.2 Micro-Pin Fin Design Analysis

To develop the pin fin array design matrix, the variable and constraining parameters were first identified. The relevant pin fin array parameters are diameter (D), transverse spacing (S_T), longitudinal spacing (S_L), and pin height (H_{fin}). From these values, aspect ratios were computed to evaluate the expected performance of the pin fin array as well as provide a better understanding of the interdependencies of one parameter on the entire pseudo-optimization matrix. Through this work, and from literature, it was found that the aspect ratios for fin height-to-diameter ($\alpha = \frac{H}{D}$), and longitudinal spacing-to-pin diameter ($\lambda = \frac{S_L}{D}$), play a significant role in fin heat sink design. For this work, α was kept between 0.2 and 1.0, and λ was kept between 1.5 and 2.75. To further constrain the design options, the transverse spacing-over-pin diameter ($\beta = \frac{S_T}{D}$) was kept constant with the values for λ, and the heat transfer coefficient was set to a value in the forced convection range (10,000 W/m^{2}K). **Figure 34** provides a schematic of the relevant design parameters for pin fin arrays in a staggered and an aligned fin array.

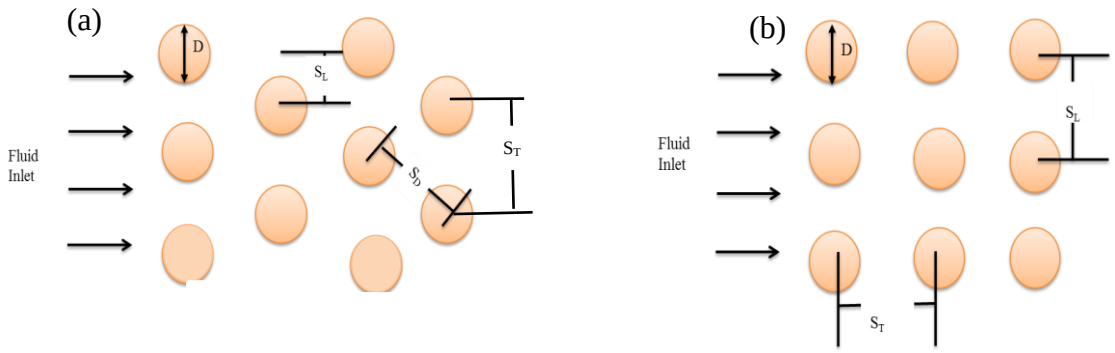


Figure 34 – Schematic of (a) a Staggered MPF array, (b) Aligned MPF array

To meet the small form factors relevant to the power modules in this work, a square matrix of pin fins was desired for uniform cooling in the heat sink design. As described earlier, the DICE method seeks to integrate micro-structured heat sinks into the back-side of a DBC substrate. Thus, 3 x 3 cm DBC substrates were obtained to develop and test various heat sink designs in this work.

The pin fin design analysis began with an assessment of various pin heights and diameters to meet an acceptable aspect ratio (α = H/D) to apply the Zhukauskas [69] correlations for flow over tube banks. Following this, two fin diameters were chosen. In order to maintain pin fins on the microscale, the height of the pin fins should be limited to 1000 µm. Fin heights beyond this not only exceeded the microscale, but they also resulted in low fin efficiencies. Equation 2 below was used to compute the fin efficiency for a convective fin tip boundary condition.

$$\eta_{fin} = \frac{\tanh(m * L_c)}{m * L_c} \tag{2}$$

This equation employs a corrected fin length (L_C) for a convective tip boundary condition and parameter (m) derived from the fin energy balance for a fin with uniform cross section. These two parameters are computed as shown in equations (3) and (4).

$$L_c = H_{fin} + (\frac{D_{fin}}{4}) \tag{3}$$

$$m = \frac{4 * HTC}{k_s * D_{fin}} \tag{4}$$

The overall heat sink efficiency is computed via equation 5 and it compares the total heat transfer afforded by the array of pins to the maximum heat transfer from the entire heat sink area.

$$\eta_o = \frac{q_{total}}{q_{max}} \tag{5}$$

The equations and parameters used in this calculation of the overall heat sink efficiency are found in equations 6 and 7 below.

$$q_{total} = (N_{total} * \eta_{fin} * HTC * A_{fin} * \theta_b) + (HTC * A_b * \theta_b) \tag{6}$$

$$q_{max} = HTC * A_{total} * \theta_b \tag{7}$$

As q_{max} calculates the maximum heat transfer rate considering the total area of the base and the fin surface area, it is expected that an increase in any of the parameters in the total heat sink area (equation 12) would yield a higher maximum heat transfer rate, and total heat transfer rate. The relevant parameters that drive this trend are the area of

the fin coupled with the number of fins. The area of the fin is computed using equation 11, and it is largely driven by the fin diameter. Thus, an increase in the fin diameter yields an increase in the maximum heat transfer rate, and an increase in the total heat transfer rate. These trends can be seen in **Figure 37**, below. For this work, the total heat transfer rate and maximum heat transfer rate varied as the pin diameters varied between the final designs. Once the initial pin fin diameters were chosen, the impact of increased longitudinal spacing between the pins on the overall heat sink efficiency was determined. As shown in **Figure 35**, this calculation was completed at various α values.

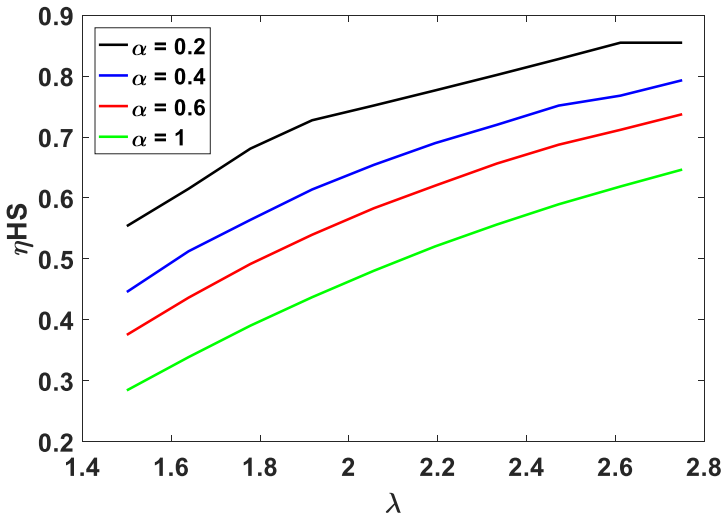


Figure 35 – Heat Sink Efficiency (η_{HS}) vs. Longitudinal Spacing (λ) at Various α

As seen from **Figure 35**, the overall efficiency of the heat sink improved with increased longitudinal spacing. However, as the ratio of height-to-diameter increased the efficiency of the heat sink decreased. This indicated that for improved heat sink performance, the height of the fins should be less than the diameter of the fins. From this

analysis, a longitudinal spacing of 2.75 was chosen for the final pin design. As stated earlier, this value was also used for the transverse spacing dimension.

After the longitudinal spacing was chosen, an appropriate aspect ratio was determined through an assessment of the impact of increasing the aspect ratio on the fin efficiency at different pin heights. **Figure 36** shows the interdependency of pin fin aspect ratio on overall heat sink efficiency.

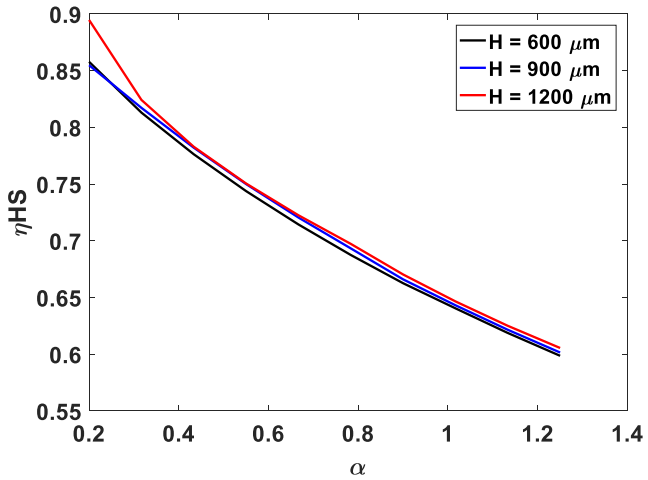


Figure 36 – Heat Sink Efficiency (η_{HS}) vs. α at Various Pin Heights (H_{fin})

As shown in **Figure 36**, the overall heat sink efficiency significantly decreases with increased aspect ratio. Additionally, at aspect ratios greater than 0.3, the overall heat sink efficiency does not vary much with increased fin height. Furthermore, this assessment suggests that better performing pin fin heat sinks would employ a pin height of 1200 μm with an aspect ratio of 0.2. However, as stated earlier, a pin height of 1200 μm places the array on the mini-scale rather than the micro-scale and results in a heat sink array with fewer than 5 fins at a diameter of 6000 μm. Thus, the aspect ratio for this design needed to be greater than 0.2 but less than 1. As the aspect ratio is varied, one must also consider the manufacturability of the heat sink, considering the machining

tolerances and material properties of the heat sink material. For this work, a fin height of 900 µm was chosen.

Finally, an assessment of fin diameter and its impact on overall heat sink efficiency was completed. For each of the fin heights in **Figure 36**, the aspect ratio (α) was varied to determine optimal fin diameters. This calculation was done to verify that the fin diameters selected initially provided sufficient heat sink performance considering the tradeoffs of manufacturability, durability of heat sink materials, and scaling of the heat sink. **Figure 37** provides a review of the overall heat sink efficiency as fin diameters were varied.

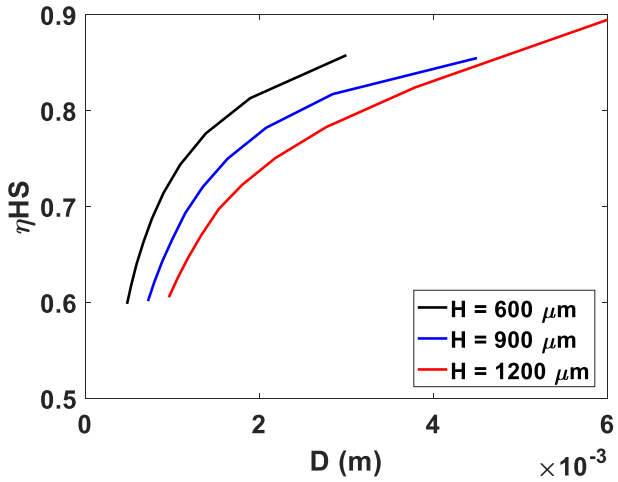


Figure 37 – Heat Sink Efficiency (η_{HS}) vs. Fin Diameter (D) at Various Pin Heights (H_{fin})

From this assessment, it was found that increased fin diameters corresponded to improved heat sink performance. Thus, for the pin height of 900 µm, diameters of 950 µm and 1500 µm were chosen. After these parameters were determined, the number of transverse pin fins and longitudinal pin fins for the array was calculated from equations 8 and 9, respectively.

$$N_T = (2 * N_L) - 1 \tag{8}$$

$$N_L = \frac{L}{\lambda * D_{fin}} \tag{9}$$

Equations 8 and 9 show the interdependencies of the fin spacing on the maximum allowable pins in the heat sink array. From this, an estimate of the total number of pin fins can be computed via equation 10.

$$N_{total} = floor(\left(\frac{N_T+1}{2} * \frac{N_L+1}{2}\right) + (\frac{N_T-1}{2} * \frac{N_L-1}{2})) \tag{10}$$

From equation 10, an approximate number of pin fins can be determined. However, this calculation employed the entire heat sink area, so the actual number of fins that could be used for each design was dependent upon the spacing from the edge of the heat sink to the first pin in the row or column. To determine the total heat sink area used in the fin efficiency calculations, the area of each fin, along with the number of fins must be calculated for each heat sink array. These parameters were computed using equations 11 and 12.

$$A_{fin} = \frac{\pi * {D_{fin}}^2}{4} \tag{11}$$

$$A_{total} = \left(N_{total} * A_{fin}\right) + A_b \tag{12}$$

For this work, two pin fin array geometries were chosen. For comparison with conventional heat sink designs, a linear channel fin geometry was also developed to occupy the same heat sink area as the micro-pin fin heat sink arrays. Furthermore, an unstructured heat sink was used for comparison between heat sinks with micro-structures

and heat sinks with no additional surface area for enhanced heat transfer. The parameters associated with each heat sink design can be found in **Table 2**. The longitudinal spacing ratio (λ) for each of the pin fin arrays was kept constant (2.75) between the two designs. However, due to the variations in the design pin fin diameter, the aspect ratios varied, and the spacing between each of the pins varied. Thus, design 1 was coined medium density (MD) micro pin fins (MPF) and design 2 was coined high density (HD) micro pin fins (MPF) because of the increase in number of fins in the same heat sink area for design 2 as compared to the number of pin fins in the same heat sink area in design 1. As the longitudinal spacing impacted the overall heat sink efficiency significantly, this value was the dominating spacing ratio term between the longitudinal and transverse spacing ratios. Therefore, the transverse spacing ratio was kept equal to the longitudinal spacing ratio for simplicity.

Table 2 – Final Heat Sink Designs

Parameter	**Design 1 MD Pins N_T =13 N_L = 7**	**Design 2 HD Pins N_T = 21 N_L = 11**	**Design 3 Linear Channel 14 cols**	**Design 4 Straight (unstructured) Channel 900 µm gap**
Number of Pins/ Fins	46	116	14	---------
Pin Diameter/Thickness	1500 µm	950 µm	1125 µm	---------
Pin Height	900 µm	900 µm	900 µm	----------
Transverse Spacing [$\boldsymbol{\beta = \frac{S_T}{D}}$]	2.75	2.75	---------	---------
Longitudinal Spacing [$\boldsymbol{\lambda = \frac{S_L}{D}}$]	2.75	2.75	---------	---------
Aspect Ratio [$\boldsymbol{\alpha = \frac{H}{D}}$]	0.6	0.9473	---------	---------

For the horizontal cooling tests, designs 1-4 were used to compare the conventional cooling method and linear channels to an enhanced structure design of medium-density and high-density pin arrays. For the vertical cooling tests, only design 4 (unstructured channel) was employed to analyze the cooling performance of a jet impingement cooling scheme. The expected overall heat sink efficiency for the MD MPF heat sink is 75%, and the expected overall heat sink efficiency for the HD MPF heat sink is 68%. These efficiency values for the pin fin designs were determined using equation 5 above. The efficiency value for the linear channels was determined via a similar equation with the area computed for a rectangular fin. From **Figure 36**, it can be seen that the highest achieved overall heat sink efficiency occurs at low aspect ratios for the MPF designs. However, a higher MPF aspect ratio was chosen for this work to allow for ease of the heat sink manufacturing. The linear channels in this work were also designed to allow for ease of manufacturing. For simplicity, the spacing between each of the fins in the linear channel design was kept equal to the thickness of the fins. The final fin spacing for the linear channels was chosen to allow for similar spacing dimensions between the micro-structured heat sink geometries. Once all designs were determined, various manufacturing techniques were considered for developing the heat sinks. The final four heat sink designs machined into the DBC substrate are shown in **Figure 38**.

Figure 38 – DBC HS Designs, (a) Design 1 (MD MPF), (b) Design 2 (HD MPF), (c) Design 3 (Linear Channels), (d) Design 4 (Unstructured Channels)

3.2.3 Micro-Pin Fin Channel Enclosure

To develop a testing chamber, an aluminum enclosure was machined from two aluminum plates. These plates were 0.25” thick, and they were machined to have a 900 µm gap for which fluid could travel through the heat sinks. The machined DBC heat sinks were then attached to the enclosure for one test section (**Figure 39**). The aluminum enclosure and DBC were connected using a Loctite RTV Gasket Material. **Figure 40** provides a schematic of the flow though the horizontal cooling test sections.

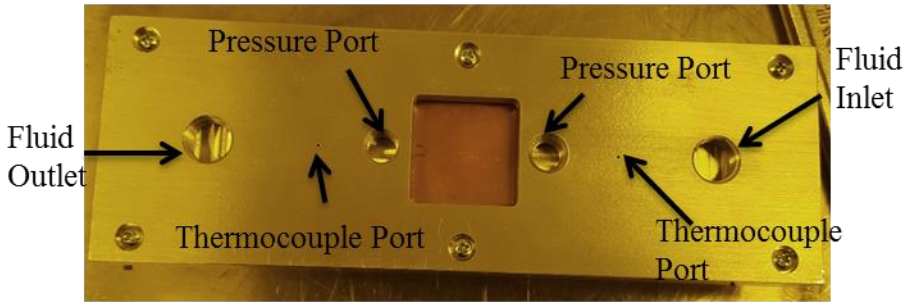


Figure 39 – Al and DBC Test Section

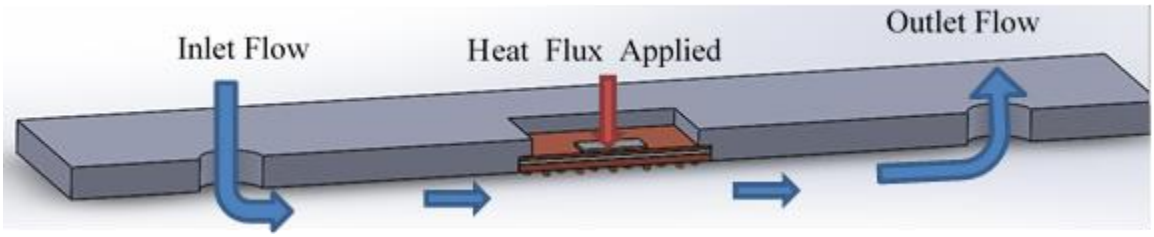


Figure 40 – Flow Pattern for Horizontal Cooling Test Sections (the bottom plate of the aluminum is removed to show the pin fins in the channel)

Pressure and thermocouple ports were placed around the micro pin fin test section to provide a more accurate measurement of these parameters. Four aluminum test sections were manufactured for each of the designs, and this manufacturing technique proved the most effective for testing each of the designs. Following this, each DBC test section was machined to fit the drawing specifications in the SolidWorks model and the analytical models.

The next step was to determine how to attach the DBC to aluminum without compromising the electrical isolation in the DBC stack. After the DBC was machined to fit the gap of each aluminum test section. To ensure that the DBC sat flush with the aluminum test section, an oil-resistant gasket was inserted between the DBC test section and aluminum as needed. Then, each section was tested for leaking and Loctite high-temperature RTV gasket material was applied to the top of the DBC test section at the joint of the copper and aluminum. To seal the entire test section, 3/32” rubber o-ring cord material was inserted between the two aluminum plates that build the test section, and the two aluminum plates were secured with machine screws. After this, each test section was evaluated for leaking.

3.3 Heater Design

3.3.1 Heater Manufacturing

The RTD chip heaters were manufactured from a 300 μm silicon wafer with 2 μm of silicon dioxide (used as a passivation layer). This was then followed by a 200 Å layer of platinum and finally a 500 Å layer of copper. To allow for chip heater operation, a serpentine pattern was made with the platinum heaters to allow for the flow of current through the devices. The entire chip heater (**Figure 41**) was then coated to prevent damage to the chip, and to allow for ease of cleaning and mounting the chip heaters to the test sections.

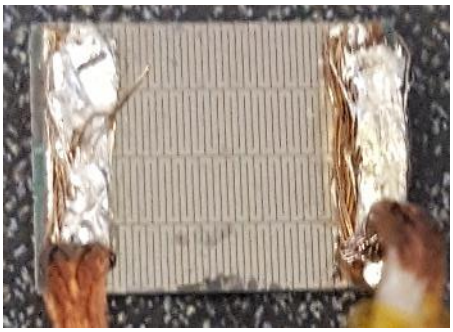


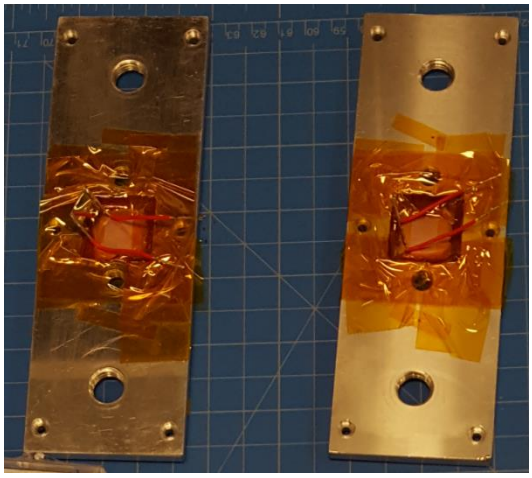
Figure 41 – Platinum Heater with Serpentine Pattern (the left and right edges of the heater show copper wire mounted to the heater with solder)

3.3.2 Heater Mounting Method

The RTD chip heaters were mounted using Epotek H2OE silver-based epoxy. Parts A and B of the epoxy were mixed with a 1:1 ratio of material weight. After preparation of the epoxy solution, a 60 μm mask was screen-printed to center the heater onto the thin side of the DBC. To ensure a uniform thickness of the epoxy under each heater, the mask was developed to span the dimensions of 13.5 x 10.49 mm. The epoxy

was concentrated in one corner of the mask and spread using plastic to match the 60 µm thickness of the Kapton® tape. **Figure 42** shows the mask and epoxy spreading methods respectively.

(a)



(b)

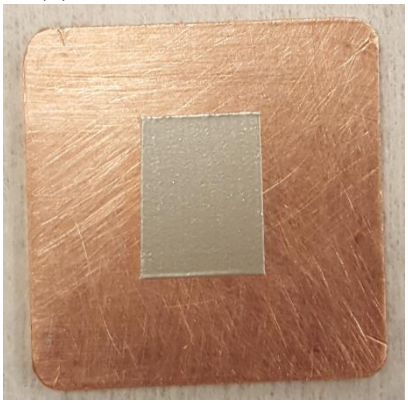


Figure 42 – (a) Epoxy Screen Printing Mask, (b) Final Epoxy Screenprint

Once the epoxy spread was deemed uniform and acceptable, the DBC and chip heaters were placed on a Finetech attachment rig where a tool arm was used to center the heater onto the epoxy. Once the epoxy and heater were deemed centered, a pressure between 0.1 and 0.7 N was applied to each heater to spread the epoxy evenly under the heaters. To avoid creep-up of the epoxy onto the heater and solder joints, the pressure was applied incrementally until the heater was secure to the DBC. As pressure was applied to secure the heater, a vacuum was applied to avoid any shifting of the heater or DBC. After everything was aligned, a temperature of 175°C was applied for 6 minutes (with approximately 15 sec ramp up) to allow for reflow and curing of the thermal epoxy to ensure a thin bond-line. This time for reflow significantly exceeded the manufacturer

required 45 seconds. However, as the mounting was done on machined heat sink DBC pieces, a longer reflow was applied to ensure a secure bond.

The first iteration of this bonding technique was done on a blank piece of DBC substrate material. After the test heater was mounted to the DBC, a confocal scanning acoustic microscopy (CSAM) machine was used to ensure that there were no voids in the epoxy bond. This assessment was critical because if there are voids in the epoxy bond, the voids introduce added thermal resistance and prevent the RTD chip heater from being able to operate at high power conditions due to the increased chip temperature. Once it was determined that there were no voids in bond of this test piece, the same process for heater mounting was applied to each test section. **Figure 43** and **Figure 44** show the heater attached to the finned and unstructured DBC substrates after the Finetech system connected the heater and DBC substrate, respectively.

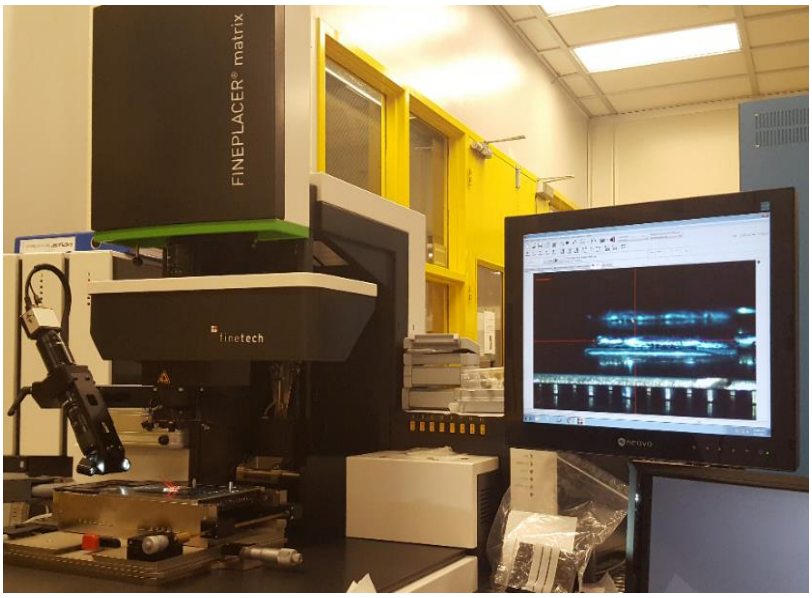


Figure 43 – Heater Mounting to HD MPF Array using Finetech FINEPLACER® Matrix Device

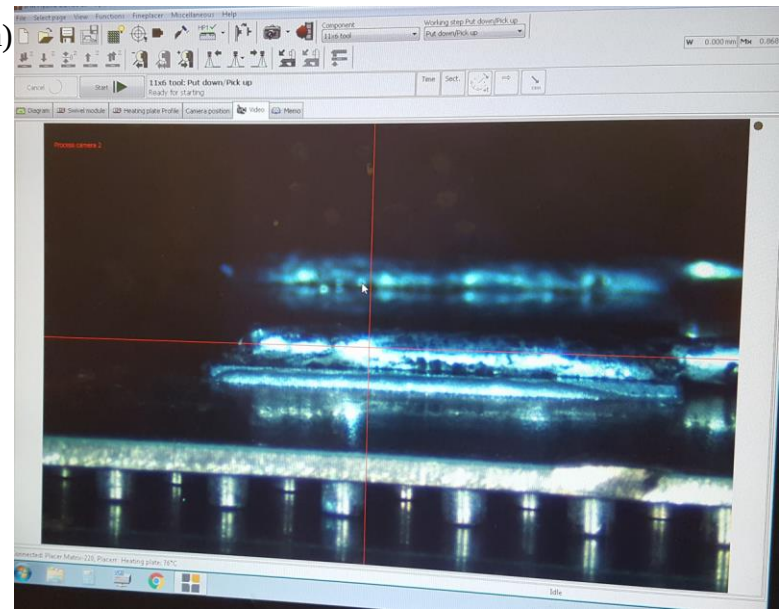
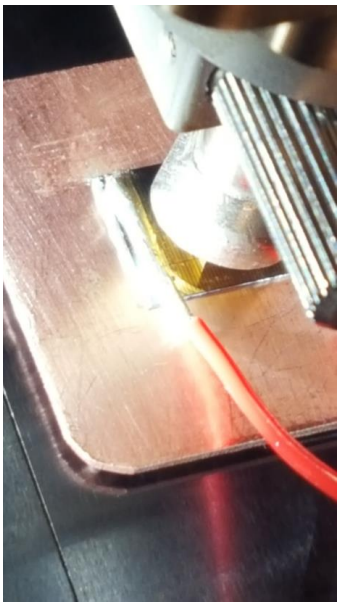
(a)   (b)

Figure 44 – (a) Finetech Mounted HD Pin Fin Heat Sink Array, (b) Finetech Mounting Process for Unstructured Heat Sink

As stated earlier, the bond-line was important to maintain across each of the pin fin, linear channel, and unstructured test sections so that each RTD chip heater can be operated using the same power conditions.

3.4 Warpage Impacts

As this work seeks to eliminate some of the interface layers, it is important to quantify estimated warpage impacts with a reduced substrate stack. To complete this, solid models were developed and analyzed using ANSYS Workbench™. For each design geometry, a solid model was developed with IGBT, thermal interface material (TIM), and DBC layers. To test for warpage during reflow, the solid models employed the conventional and DICE configurations. Given that the material that undergoes reflow in mounting is the interface material, the deformation induced because of the CTE

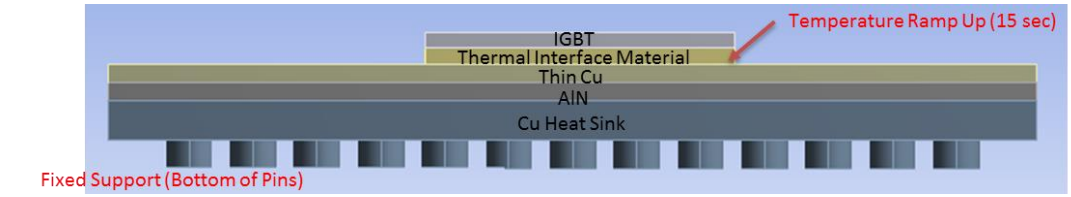
mismatch in the materials was the main focus of the warpage study. Table 3 lists the material properties applied to these thermal models.

Table 3 – Material Properties for Warpage Study [20], [70], [71], [72], [73], [74], [75], [76]

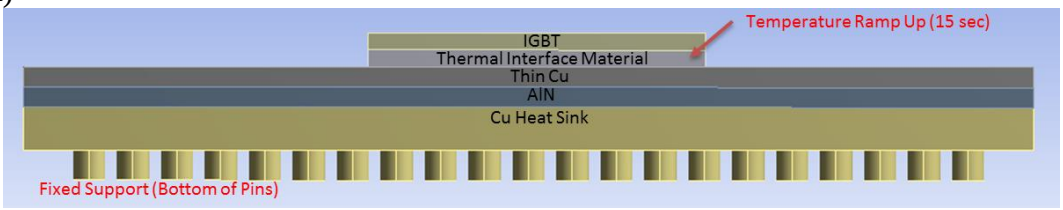
Materials	**Young's Modulus (Pa)**		**Poisson's Ratio**	**Density (kg/m^3)**	**Coefficient of Thermal Expansion (1/℃)**	
Copper	Temp (℃)	Young's Modulus	0.34	8933	Temp (℃)	CTE
	20	96.89			20	16.4e-6
	50	92.106			50	16.7e-6
	150	89.503			150	17.9e-6
	250	79.762			250	18.5e-6
	500	63.991			500	20.2e-6
SAC 305	50E9		0.36	7380	2.16E-5	
AlN	3.3E11		0.24	3260	4.5E-6	
Silicon	1.31E11		0.27	2329	2.6E-6	
Aluminum	2.6E10		0.33	2700	2.52E-5	
Arctic Silver 5 Thermal Paste	8.3E10		0.37	10490	1.4565E-6	
Sintered Silver Paste	72E9		0.37	10070	20E-6	
Epotek H20E Epoxy	5.576E9		0.3	2600	1.58E-6	

The three interface materials applied to this analysis were chosen to compare the impacts of warpage using materials with varying thermal conductivities and electrical properties. The Epotek H20E epoxy is a silver-based, electrically conductive epoxy. It is

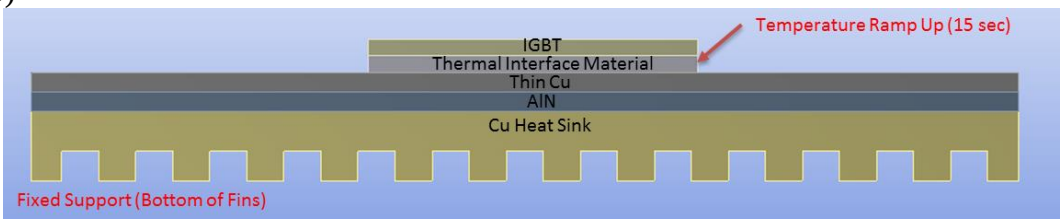
commonly used for electronics, but it has a lower thermal conductivity as compared to other silver-based interface materials. The experiments conducted in this work employ the Epotek epoxy. For conventional device configurations, SAC305 or other metallic solders are used. Sintered silver paste has also been explored because of the improved thermal and electrical materials properties over other conventional interface materials. Thus, it was important to include both the SAC305 solder and the sintered silver paste in the warpage studies. For each of these interface materials, it was assumed that the manufacturing would follow the same screen-printing method as described above with a reflow time of 15 seconds at 175°C. In industry, the SAC305 and sintered silver use higher reflow temperatures, but for the initial models, a reflow temperature of 175°C was used. For the conventional device stack, dimension similar to those in [28] were used for the IGBT, heat spreader, interface and heat sink materials. Additional modeling was completed over a range of reflow temperatures (220°C and 240°C) to cover the possible range of reflow temperatures used for the solder and sintered silver paste. **Figure 45** provides a schematic of the conventional and DICE stacks and loading conditions modeled for the warpage studies.



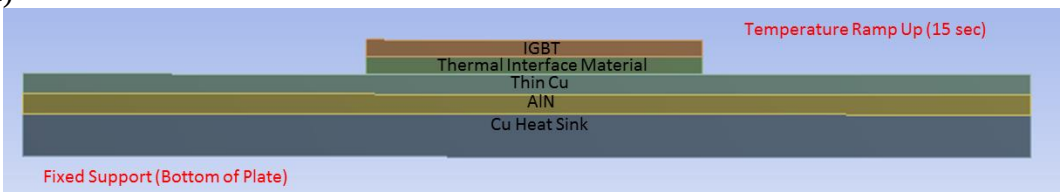
(a)



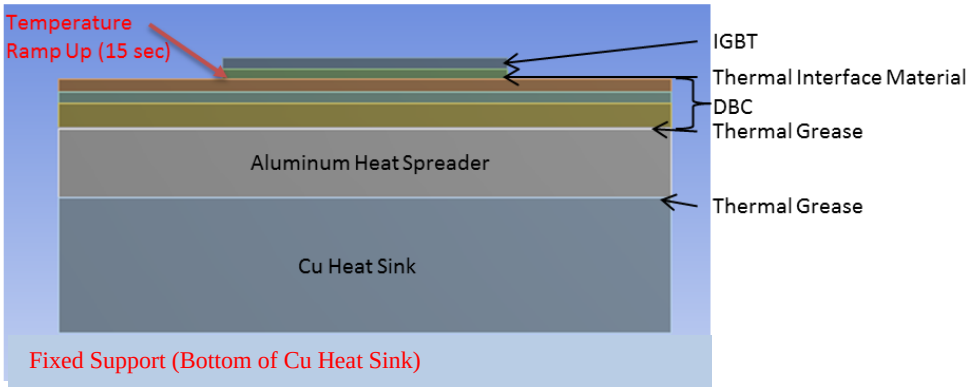
(b)



(c)



(d)



(e)

Figure 45 – Loading and Boundary Conditions for Warpage Studies for (a) MD MPF, (b) HD MPF, (c) Linear Channels, (d) Unstructured Channel, (e) Conventional Stack

Each of the numerical models employed a 0.51 mm silicon IGBT centered on the DBC to allow for uniform cooling. The additional dimensions used in these models are listed in **Table 4**.

Table 4 – DICE Power Module Modeling Dimensions

Material	***Dimension***
Silicon IGBT	0.51 mm
Thermal Interface Material Layer	60 µm
DBC Thin (Top) Copper Layer	300 µm
Aluminum Nitride (AlN)	600 µm
DBC Thick (Bottom) Copper Layer	1200µm
Cu Heat Spreader	3000µm
Aluminum Heat Sink	6000µm

3.5 System Calibrations

3.5.1 Heater Calibration

The RTD chip heaters were calibrated using a 2-wire calibration method. The heaters were mounted to a thermal stage attached to the INSTEC mk2000 temperature controller with a thermocouple connected to a FLUKE 54IIB thermometer using a silicone-based thermal grease. To ensure an accurate reading from the thermal stage, a Raman microscopy calibration method was completed first using silicon. The variations in this data were tabulated to create a curve to adjust the temperatures for accurate temperature readings. During calibration of the heaters, the electrical resistance and temperatures were read at ambient, and temperatures ranging from 30-160℃ in increments of 15℃. As each temperature set, the corresponding resistance value was measured across each heater using a Keithley 2425 100W Sourcemeter. At each temperature set-point, the temperature readings from the INSTEC mk2000 temperature

controller and FLUKE 54IIB thermometer were also recorded. After this, the temperatures and resistances were plotted to create a calibration curve for the heaters.

3.5.2 Thermocouple Calibration

Each thermocouple was calibrated using the OMEGA CL122 calibration device. Using the hot side of the device, temperatures were set from 30℃ to 80℃. The corresponding thermocouple readings from the Agilent 34970A data acquisition device were read into the Agilent software. The temperature readings for each thermocouple were measured and a calibration curve was developed to determine the uncertainty contribution of the temperature readings.

3.6 Vertical Cooling Design Analysis

For the vertical cooling scheme, a pseudo-optimization study was performed to design jet arrays to effectively apply cooling to the unstructured channel test section. In jet impingement, the critical parameters are the jet spacing, the height between the impingement surface and the jet orifices and the jet diameters.

To begin this design analysis, a few parameters were constrained. First, given that the vertical cooling would be applied to the chip heater mounted DBC/aluminum test sections, the height between the impingement surface and the jet orifices was set constant. This height covered the gap in the channel (900 μm), the thickness of the aluminum plate used for the enclosure of the test sections (0.00635 m), and the height of the jet array (0.0024 m). Following this, diameters of jets were chosen to fit the acceptable aspect ratio, $\alpha_{jet} = \frac{H}{D_{jet}}$. For the design analysis, correlations from Martin [56]

were used. These correlations were applicable for 2,000 < Re < 100,000, 2 < α_{jet} < 12, and 0.004 < A_r < 0.04 [56].

Once the acceptable jet diameters were chosen, a study was completed on the influence on HTC in either a staggered or aligned array. As laminar, transition, and turbulent flow drive variations in HTC, the flow rate was held constant and limited by the manufacturer's limits on the flowmeter and gear pump used in these experiments. For the design analysis, flow rates of 1.3 lpm and 4.9 lpm were applied. These values represented a low and high range of flowrates that generated Reynolds numbers in the acceptable range set by Martin [56]. However, for initial guesses of flow rate, the minimum and maximum allowed velocities were calculated to fit the range of Reynolds numbers. The last constraint applied to the jet array analysis was the allowable jet area. This area indicates the amount of space available to apply jets to avoid interference with the sealing material or opening of the aluminum enclosure area. To compute the HTC, first the area of each jet was computed via equation 13.

$$A_{jet} = \pi * \frac{{D_{jet}}^2}{4} \tag{13}$$

This area was fed into the velocity found at each individual jet and the expected corresponding Reynolds number. The individual jet velocity considered the total number of jets and the area of each jet as shown in equation 14.

$$V_{jet} = \frac{V_{dot}}{(N_{jets} * A_{jet})} \tag{14}$$

The number of allowable jets was dependent upon the spacing of the jets. Thus, the diameter of the jets and spacing became the two independent design parameters used to analyze each jet array design. Equation 15 shows the interdependency of the jet spacing and available jet area on the number of jets,

$$N_{jets} = \frac{A_{jet\ array}}{S^2} \tag{15}$$

where, the available area for the jet array is computed via equation 16.

$$A_{jet\ array} = \frac{\pi * D_{available}}{4} \tag{16}$$

With these equations presenting various tradeoffs in the jet array design, the areas for an array of staggered and aligned jets was computed via equations 17 and 18 respectively.

$$Ar_{staggered} = \frac{\pi * {D_{jet}}^2}{2\sqrt{3}\, S^2} \tag{17}$$

$$Ar_{aligned} = \frac{\pi * {D_{jet}}^2}{4 * S^2} \tag{18}$$

With these equations, the corresponding Nusselt number and HTC were computed via equations 19-22.

$$\overline{Nus_{staggered}} = 0.5 * K_{staggered} * G_{staggered} * Re^{\left(\frac{2}{3}\right)} * Pr^{0.42} \tag{19}$$

$$\overline{Nus_{aligned}} = 0.5 * K_{aligned} * G_{aligned} * Re^{\left(\frac{2}{3}\right)} * Pr^{0.42} \tag{20}$$

$$HTC_{Staggered} = \frac{\overline{Nus}_{staggered} * k_f}{D_h} \tag{21}$$

$$HTC_{Aligned} = \frac{\overline{Nus}_{aligned} * k_f}{D_h} \tag{22}$$

The correction factors K and G for each both the aligned and staggered array jets were calculated via equations 23-26.

$$K_{aligned} = (1 + (\frac{\alpha}{0.6 / Ar_{aligned}^{0.5}})^6)^{-0.05} \tag{23}$$

$$K_{staggered} = (1 + (\frac{\alpha}{0.6 / Ar_{staggered}^{0.5}})^6)^{-0.05} \tag{24}$$

$$G_{aligned} = \frac{(2 * Ar_{aligned}^{0.5} * (1 - 2.2 * Ar_{aligned}^{0.5}))}{(1 + 0.2 * (\alpha - 6) * Ar_{aligned}^{0.5})} \tag{25}$$

$$G_{staggered} = \frac{(2*Ar_{staggered}^{0.5}*(1-2.2*Ar_{staggered}^{0.5}))}{(1+0.2*(\alpha-6)*Ar_{staggered}^{0.5})} \tag{26}$$

From this study, it was found that the variation in heat transfer coefficient between the staggered and aligned jet array designs was minimal. However, with increased jet spacing, the staggered jet array design performed better than aligned jet array design. **Figure 46** shows the influence of jet spacing on the heat transfer coefficient at an acceptable jet diameter to fit α_{jet}.

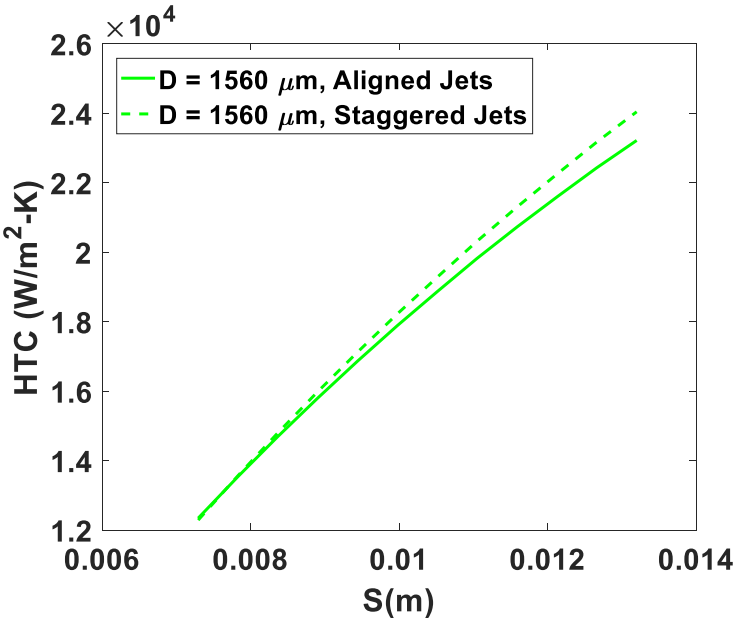


Figure 46 – HTC vs Jet Spacing for a specified jet height to impingement surface aspect ratio

From **Figure 46** it can be noted that an increase in jet spacing significantly increases HTC. Therefore, the analysis suggests that jet spacing greater than 0.012m will provide better performance. Thus, a study of the influence on HTC of an increase in jet diameter at spacing values greater than 0.012 m was completed. **Figure 47** shows the interdependencies of the jet diameter on the HTC.

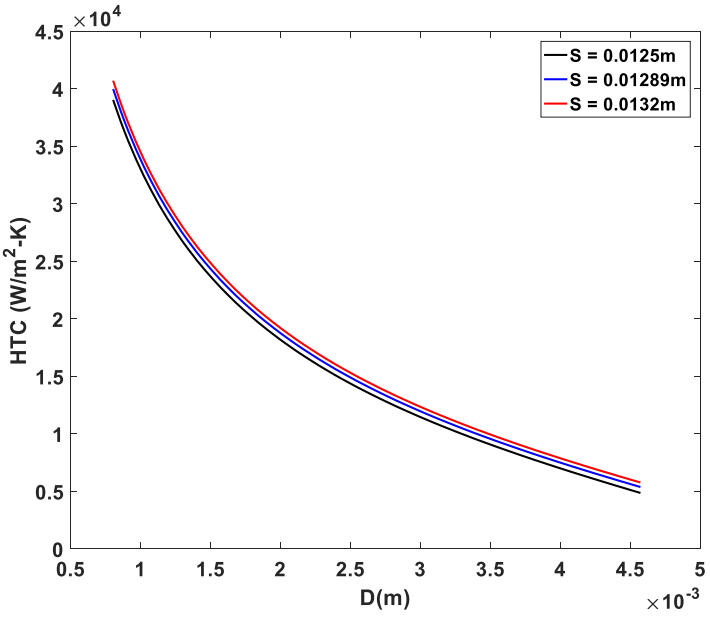


Figure 47 – HTC vs Jet Diameter at Various Spacing Dimensions

Figure 47 shows that increased jet diameters not only lead to fewer jets in the array, but it also lead to low HTCs. It can also be seen that the performance of the staggered jet array does not vary much between spacing dimensions of 0.0125 m, 0.01289 m, and 0.0132 m. These spacing values were chosen because they were on the higher end of the range of spacing values that provided higher HTC values for a staggered jet array. To aid in making the final jet array decision, an analysis of influence of jet spacing on HTC at jet diameter values in an acceptable range for α_{jet} and Ar was completed. **Figure 48** shows how the HTC is impacted by the jet spacing and diameter.

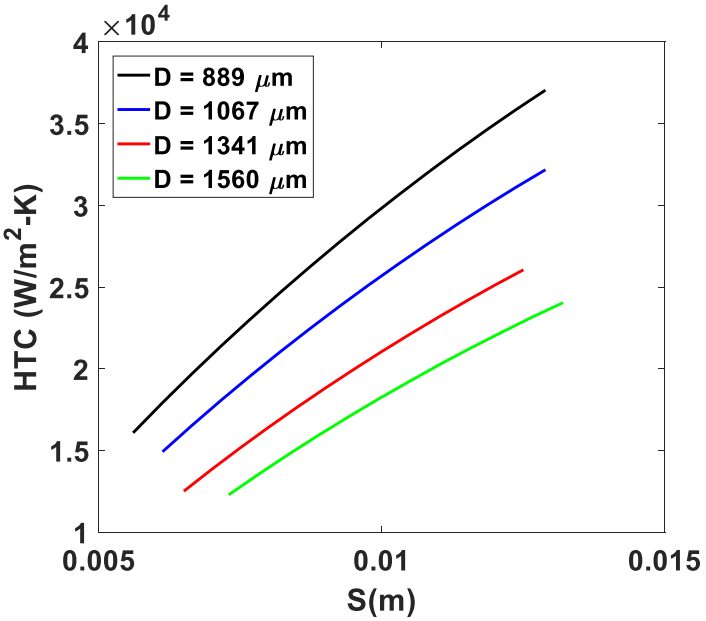


Figure 48 – HTC vs Jet Spacing at Different Jet Diameters

From **Figure 48**, it can be seen that as jet spacing increased, the HTC also increased. However, as the jet diameter increased the corresponding HTC decreased. According to **Figure 48**, optimal jet performance would be found at a jet diameter of 889 μm with a jet spacing greater than 0.01 m. However, manufacturing a jet array of this design could prove to be difficult. The final jet array design parameters used in this work are listed in **Table 5**. The maximum HTC values listed in this table were computed via equation 21.

Table 5 – Final Jet Array Designs

Parameter	Design 1	Design 2	Design 3
Jet Diameter (μm)	889	889	1560
Aspect Ratio (H/D)	10.81	10.81	6.162
Spacing (m)	0.006644	0.0097670	0.01052
Number of Jets	17	8	7
Heat Transfer Coefficient (W/m^2-K)	19,694	29,205	19,289

Once the jet designs were developed, the manufacturing method was analyzed. The first iteration of the jet arrays employed a 0.016” thick sheet of aluminum. Each design was developed in SolidWorks and the test sections were machined using a high pressure waterjet tool. The aluminum test coupons were expected to allow for ease of switching out jet designs for experiment efficiency. However, the precision of the waterjet on very small diameter holes was not accurate enough to ensure optimal jet performance or repeatability in the jet array manufacturing. Thus, the final jet designs were manufactured using a laser cutter. **Figure 49** shows the final jet array test coupons.

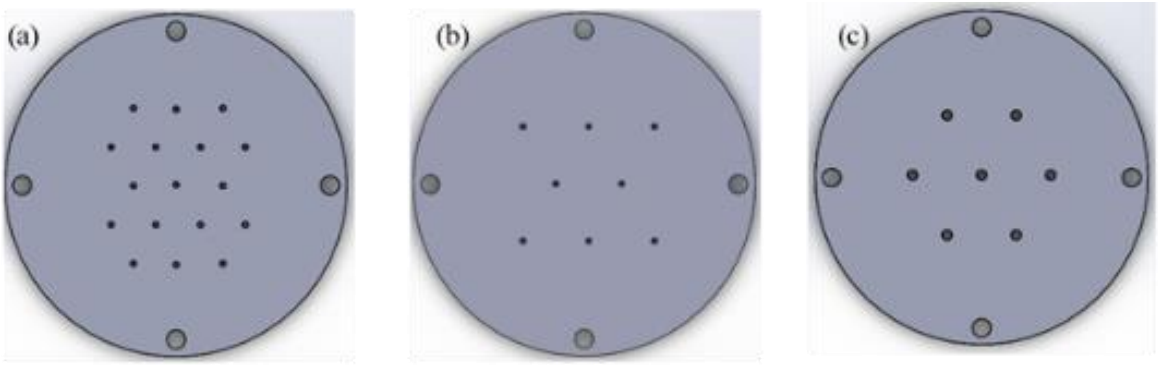


Figure 49 – Final Jet Array Designs (a) Design 1, (b) Design 2, (c) Design 3

3.6.1 Jet Array Enclosure

Each jet array test coupon was mounted to an acrylic spray chamber with layers of thermal grease and silicone rubber gaskets to ensure that there would be no leaking through the test section. **Figure 50** and **Figure 51** shows the actual jet test section, and a schematic of the fluid flow through the jets, respectively.

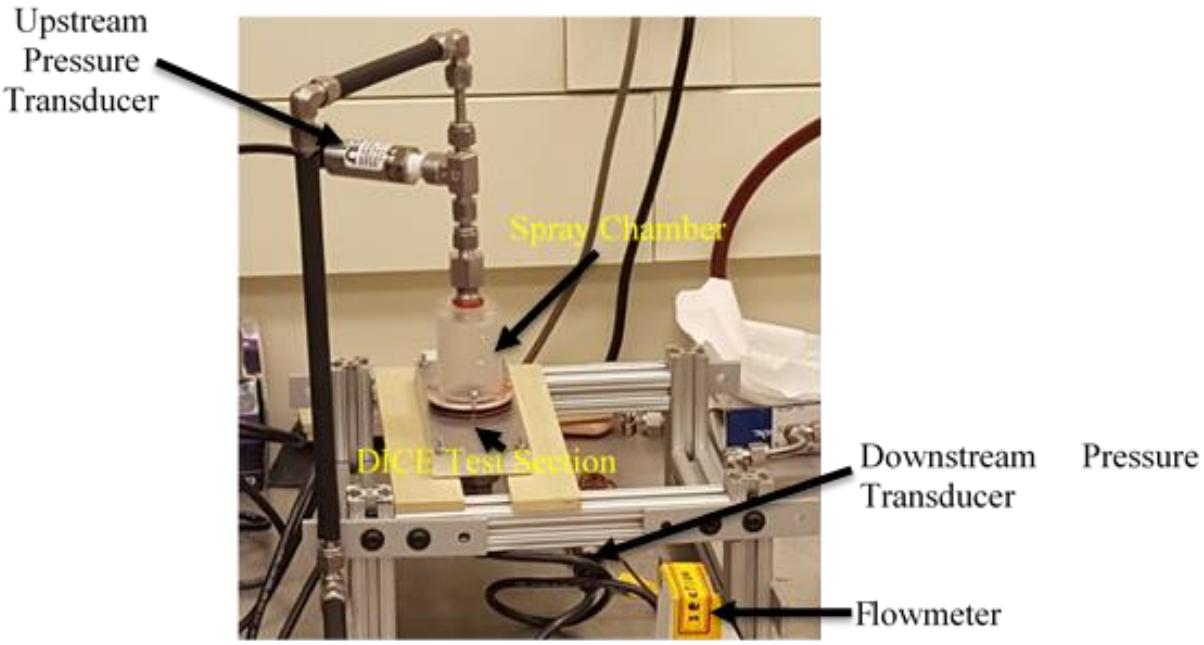


Figure 50 – Jet Array Experimental DICE Test Section

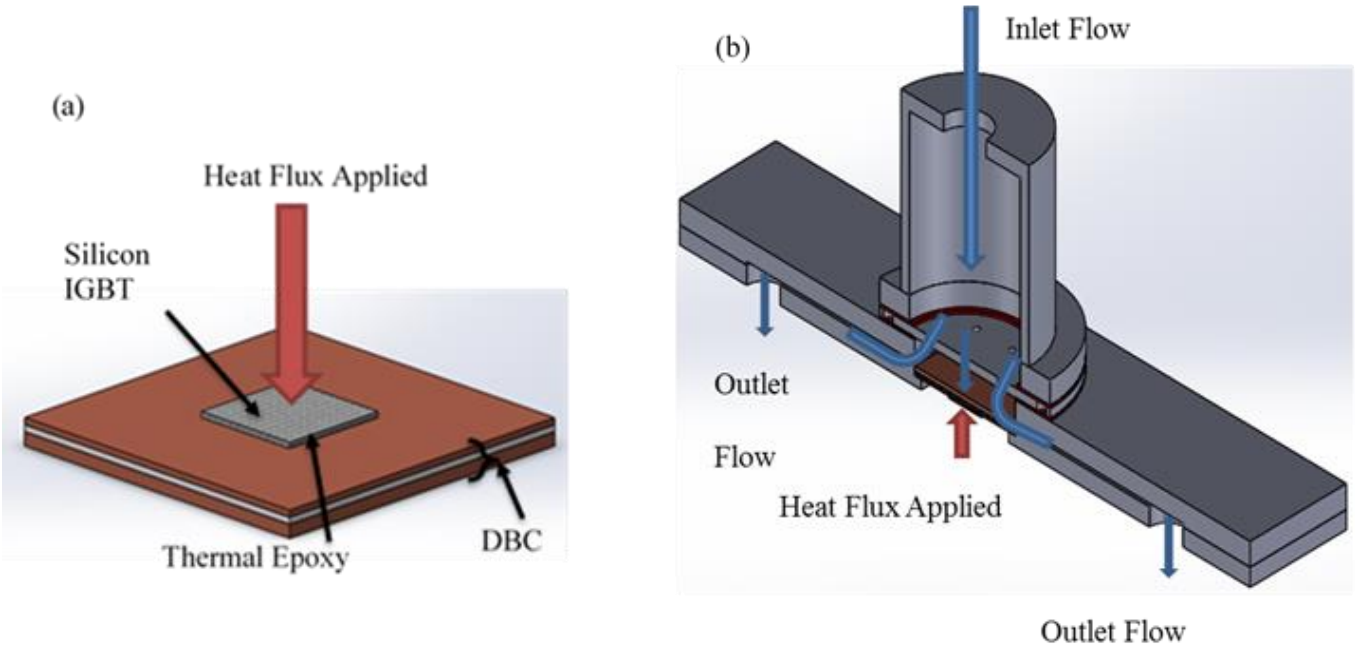


Figure 51 – (a) Schematic Cross-Section of the Jet Array DICE DBC (the jet fluid is applied to flat underside of the DBC), (b) Fluid flow pattern through the vertical cooling test section with interchangeable jet arrays

3.7 Experimental and Numerical Methods

For both the horizontal cooling and vertical cooling schemes, the test loop employed a McMillan S114 flowmeter, a Brazetek heat exchanger, an OMEGA gear pump drive, a Cole-Palmer Polystat chiller, Keithley 2425 100W Sourcemeter, a high-pressure water vessel, Agilent 34970A data acquisition unit and an Agilent E3649A power supply in addition to the test section. The Keithley Sourcemeter was used for 4-wire power measurement for improved accuracy in power supplied to the heater device, while the Agilent E3649A power supply was used to power the pressure transducers and flowmeter. To test each cooling method, deionized water was supplied at 26.85°C to the test sections at different flowrates.

3.7.1 Horizontal Cooling

3.7.1.1 Experiments

For the horizontal cooling experiments, a first-principle energy balance was completed to determine acceptable ranges of flow rate and expected temperature rise given an estimated power condition. Using equation 27, a power condition of 100 W was applied to the left-hand side of the equation. As the 1 cm^2 RTD chip heater was expected to drive in a heat flux of 100 W/cm^2, this estimate in the equation assumed an ideal heat dissipation scenario.

$$Q_{dissipated} = \dot{m} * C * \Delta T \tag{27}$$

From this, it was determined that a flow rate range of 0.28 lpm – 0.60 lpm resulted in a greater temperature difference across the test sections as compared to experiments run at higher flowrates. **Figure 52** provides a schematic of the cooling loop.

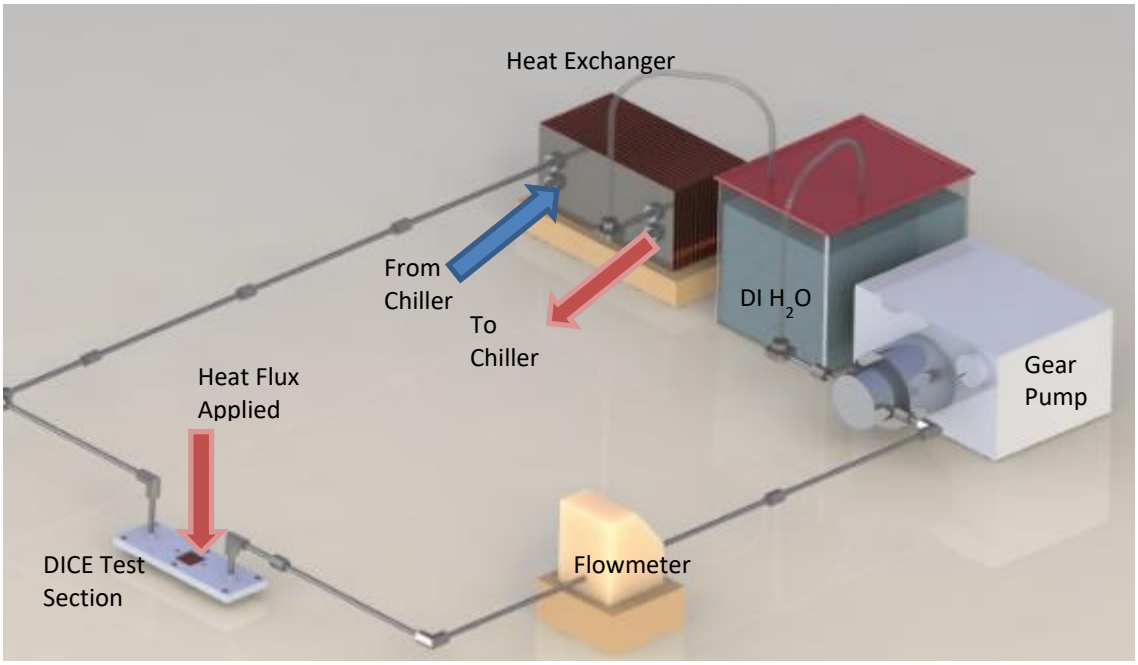


Figure 52 – Horizontal Cooling Test Loop

Once each test section was attached to the test loop, the entire system was vacuumed for 10 minutes. After this, the system was charged with water for about 5 seconds using compressed air and a stainless steel water pressure vessel tank. Then water was sent through the loop using the gear pump at flowrates in the range of 0.28-0.60 lpm respectively. For each flowrate, the system was allowed to reach steady-state after 5 minutes. While the system reached steady state, the electrical resistance of the heaters was measured at ambient, and the ambient temperature was measured. After the flowrates reached steady state, a voltage was applied starting at 10 V and increasing by 10 V until 100 V was applied to each test section. As each voltage was applied the actual voltage

and current readings were measured to determine the power applied to the test section. Each power setting was held for 5 minutes and the inlet and outlet temperatures were measured. After about 2 minutes, the current reading through the device stopped fluctuating. At this time, temperature readings using a thermocouple and FLUKE 54IIB thermometer were taken on the chip, top layer of DBC and top aluminum plate. Each of these values was recorded. **Figure 53** shows the relative location of each temperature reading.

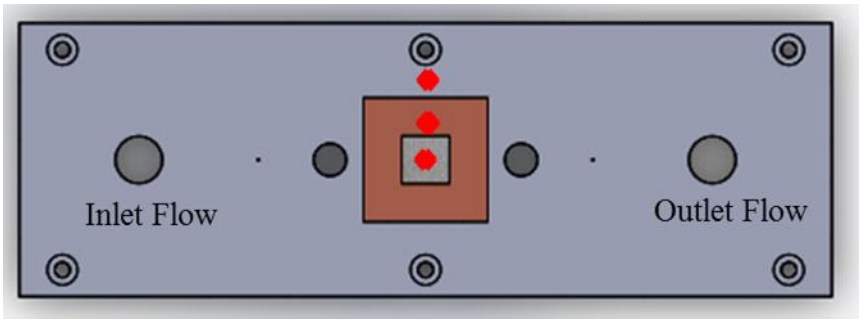


Figure 53 – Diagram of Temperature Reading Locations for DICE Test Sections (the red marks were thermocouple readings were taken); inlet and outlet temperatures were also taken at the inlet flow and outlet flow areas.

3.7.2 Vertical Cooling

3.7.2.1 Vertical Cooling Experiments

For the vertical impingement tests, only the unstructured heat sink was used. However, the enclosure base was re-designed to guide the flow from the top of the test section, with an outlet through the bottom ports. The three different showerhead spray geometries were developed to better understand which parameters provide the most effective heat removal system for the RTD chip heater. As stated earlier, each jet array

was manufactured from a 0.093” acrylic sheet using a laser-cutting technique and attached to the spray cooling test section high-temperature thermal grease and machine screws. **Figure 54** provides a graphic of the vertical cooling test section and test loop.

(a) (b)

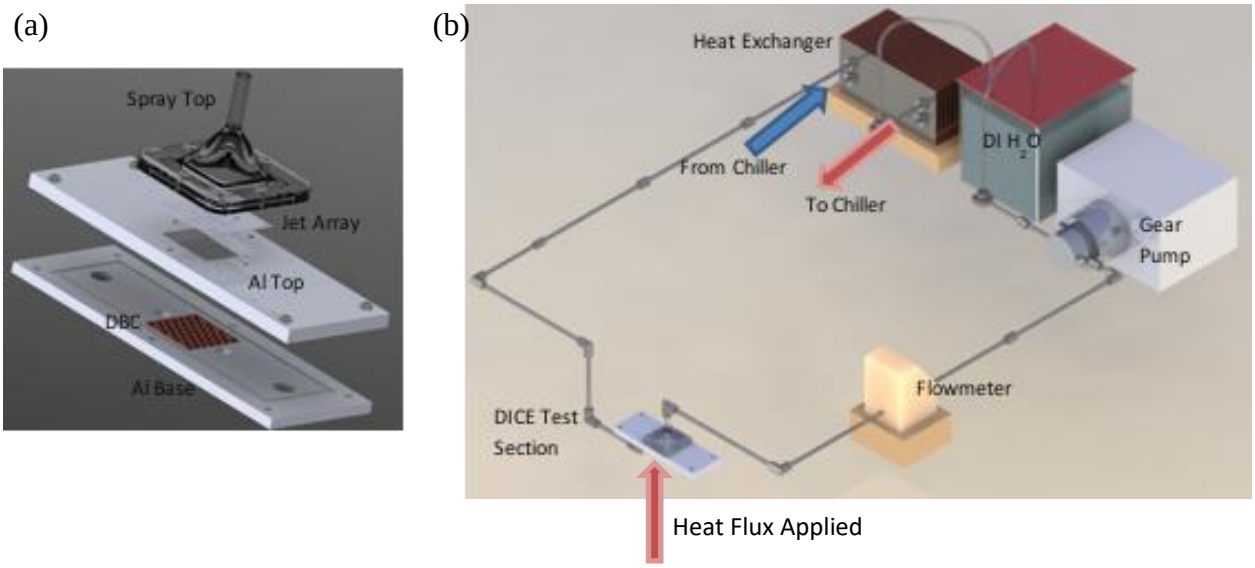


Figure 54 – (a) Vertical Cooling DICE Test Section, (b)Vertical Cooling Loop

The experiment procedure for the vertical cooling scheme was very similar to that of the horizontal cooling scheme. However, in the vertical cooling, the water reservoir allowed for an open system where fluid was drawn in with the gear pump. To apply the spray to the surfaces of the test sections, a 2” diameter spray chamber was machined from solid acrylic stock material using lathe and milling machines. A 0.08” diameter full cone spray nozzle was then inserted into the acrylic spray chamber and the nozzle was sealed to the acrylic using both RTV gasket material and JB Weld.

To begin each experiment, the spray chamber was left empty and values for temperature and resistance were taken at the ambient state. Following this, the gear pump was used to pump water through the system at incremental flowrates. After the gear

pump was set to the desired flowrate, the system was left for approximately 2 minutes to reach steady state. During this time, the spray chamber was completely filled with water. Then, the Keithley power supply supplied a voltage to the RTD heater starting at 30 V and scaling to 100 V in increments of 10 V. At each applied voltage, measurements of inlet and outlet temperature, chip temperature, and pressure drop through the test section were taken using the Agilent data acquisition unit. Each power condition was read for 4 minutes before the power was ramped up to the next voltage level. During this time, steady state was reached within about 2-3 minutes. At the end of the 4 minutes, values for voltage and current were tabulated to determine the actual power supplied to the system.

Before each test was run, the aluminum enclosure plates, silicone rubber gaskets, and jet arrays were sealed using DOW Corning high-temperature vacuum grease. In addition to this, vacuum grease was applied to the holes where the machine screws were inserted to seal the test section and prevent leaking. Before each jet experiment was run, and excess water was forced out of the test section using compressed air. To begin the experiments, the spray chamber was filled until a steady state flow condition was reached. After this, the voltage was applied to the RTD chip heaters, and once the current stopped fluctuating, the actual supplied power is recorded. Additional sets of jet experiments were run for repeatability.

3.7.2.2 Vertical Cooling Numerical Modeling

Numerical models were developed in ANSYS® Fluent® version 17.0 for the vertical cooling test sections. Conditions similar to those seen experimentally were applied as boundary conditions in the models. For the vertical cooling test sections, the

aluminum enclosure, chip mounted DBC, gasket layers, acrylic spray chamber, and acrylic jet array designs were modeled. To reduce computational effort, the vertical cooling schemes were modeled with a half-symmetry boundary condition. Following this, pieces of equipment that were exposed to the ambient environment were given a natural convection boundary condition with HTC of 5 W/m^2-K at an atmospheric temperature of 20℃. This outside condition matched what was calculated and measured at ambient conditions by the FLUKE 54IIB thermocouple.

Each numerical model was meshed to ensure an initial quality of 0.1 or greater, with minimal orthogonal skewness and low aspect ratios. The limit on quality of 0.1 generally gives more accurate and realistic results for the simulations, so this criteria was a requirement for each of the models developed in this work. Once each model was meshed in the main ANSYS® Workbench™, the models were imported into ANSYS® ICEM for further refinement. After further improving the mesh, the model was fed into the ANSYS® Fluent® solver where material properties were assigned to each body in the model, and boundary conditions of heat flux, mass flow rate, outlet pressure, and convection were applied to the models as shown in **Figure 55**.

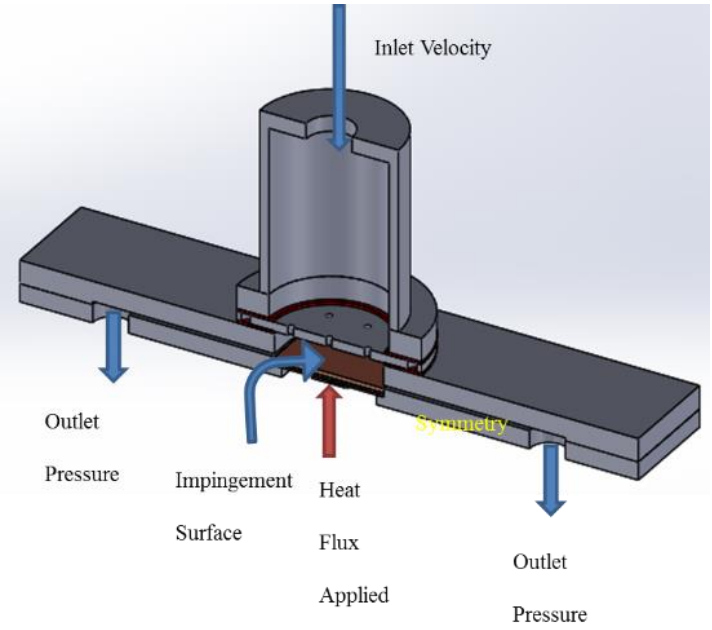


Figure 55 – Diagram of Loading and Boundary Conditions (Vertical Cooling)

In the vertical cooling models, a natural convection boundary condition was applied to all exposed surfaces of the test section. Inlet and outlet flow temperature measurements were taken at the inlet velocity and outlet pressure locations. For the models, the pressure drop was taken across the symmetry boundary condition of the water. This differed from the experimental test section where the pressure transducers were placed before and after the entire test section.

For each of the numerical models, a thermal resistance layer was applied between the silicon IGBT and thin Cu layers for a thermal epoxy thickness of 60 µm. This was done to allow for better meshing of the entire test chamber models. To determine absolute convergence of the models, the mass flow rate and total heat transfer rate were required to meet a convergence limit of 0.1% of the inlet mass flow rate and applied power. Once the models met the convergence criteria, the results were accepted as accurate.

Separate numerical models were developed to study the impacts of warpage on device development. This study was completed to see what tradeoffs arise when manufacturing the DICE stack using conventional manufacturing methods. For this work, common interface materials are applied to each of the four heat sink test sections, as well as a conventional device stack to determine how much deformation and stress is induced during reflow of the interface material. As this work uses EPOTEK H2OE epoxy, this interface material was also applied for comparison. Each ANSYS® Workbench™ model was run with tetrahedral mesh elements where applicable, and each interface material was allowed to reflow for the same amount of time.

3.7.3 Numerical Modeling for Thermal Resistance

A parametric study using ANSYS® Workbench™ was completed to determine the range of thermal resistance values each heat sink design develops over a range of heat transfer coefficient values. As there are expected ranges of heat transfer coefficients based on the cooling scheme used (e.g. natural convection, forced convection, boiling heat transfer), this parametric study was completed to determine the heat transfer coefficient required by the DICE test sections to produce a thermal resistance that is lower than the thermal resistance of the conventional stack. With this information, the HTC value needed will inform the type of cooling technique to apply to each test section. The models in this parametric study used the dimensions listed in **Table 4** to simulate the behavior of each test section with a uniform heat transfer coefficient (2,000-200,000 W/m^2-K) on the bottom surface (with the microstructures) at an ambient temperature of 26.85°C, and an applied heat flux of 100 W/cm^2. This range of HTC covered the range of forced convection and boiling HTC values.

Figure 56 shows a schematic of the loading conditions used for the parametric studies of heat transfer coefficient and thermal resistance. The same conditions were applied to each of the DICE test sections and the conventional stack.

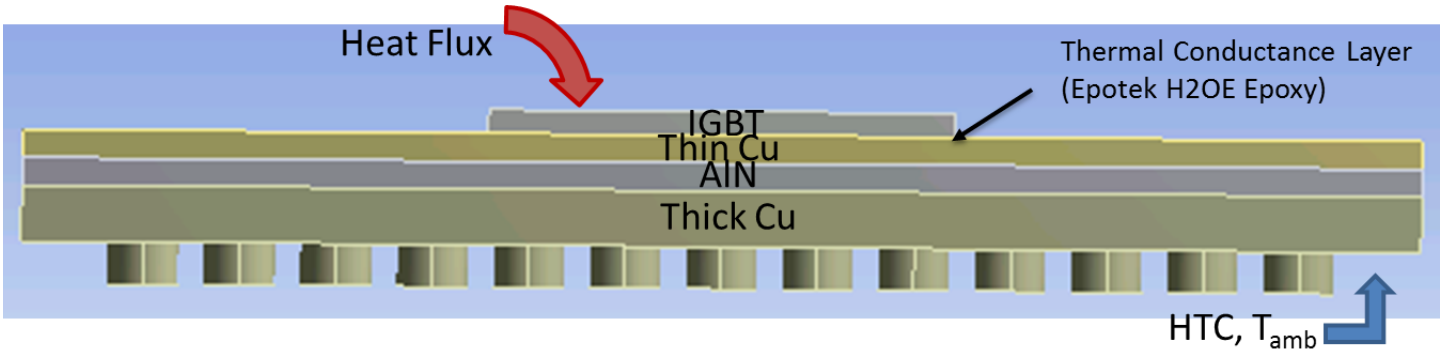


Figure 56 – Loading and Boundary Conditions for Parametric HTC Study (MD MPF)

CHAPTER 4. RESULTS

This chapter details the experiment results from the horizontal and vertical DICE cooling schemes. These results are validated by the values found in the numerical and analytical models. First, the horizontal cooling test section is reviewed for each of the fin designs, followed by the vertical cooling test section. For each cooling scheme the chip temperature, pressure drop, and the change of temperature between the inlet and outlet were measured. This data was plotted against the applied power range 1 W - 103 W at flow rates ranging from 0.28 lpm – 0.60 lpm for the horizontal cooling scheme. The vertical cooling scheme applied a power range of 1 W - 103 W over a flowrate range of 1.3-1.9 lpm. The heat dissipation from each test section was also computed using the change of temperature measured experimentally.

For both the horizontal cooling and vertical cooling schemes, a thermal resistance was determined for the DICE test sections. This thermal resistance considered the chip temperature, ambient fluid temperature and power supplied to the chip. For each of the DICE test sections, a parametric study was completed using numerical modeling to determine the full range of expected thermal resistance values one could obtain using various cooling techniques and HTC values. These thermal resistance values were compared to those computed through the experiments to better inform the cooling scheme needed to achieve low thermal resistance values. The parametric study allowed for comparison between the heat sink designs and it gave insight into the expected performance of the DICE heat sink as compared to a conventional stack.

This chapter ends with a review of the potential impacts of warpage on the novel DICE stack developed through numerical modeling.

4.1 Horizontal Cooling Results

4.1.1 Experimental Study

As stated earlier, measurements of inlet and outlet flow temperature were taken as well as the pressure drop along the heat sinks. Additionally, the chip temperatures were recorded for each power condition applied to the RTD chip heater. The inlet and outlet fluid temperatures and pressure values were read into the Agilent data acquisition device. From this, the maximum change in fluid temperature was calculated at each power level for each flow rate, and the pressure drop and flow rate were averaged over each flow rate. For each power condition, the measured change in temperature was used to compute the heat dissipated through the heat sink design. This value was then compared to the power supplied to the system to determine how well the heat was dissipated by the heat sink.

The maximum applied power for each of the heat sink designs was 102.5 W (design 1), 102.3 W (design 2), 94.09 W (design 3) and 101.3 W (design 4). The power input values were not consistent across the four designs likely due to the solder wire connection process used for each of the chip heaters. As these are RTD devices, variations in their resistance at ambient temperatures can impact their ability to generate power across the device. The available power input is also impacted by the mounting process to attach the heaters to the DBC. Thus, careful consideration during the mounting process was critical. As the heater connections were made through a screen-printing process, the likelihood of dissimilar bonds between the heaters is not very high. **Figure**

57 - **Figure 60** show the performance of heat sink designs 1-4 based on the measured chip temperature.

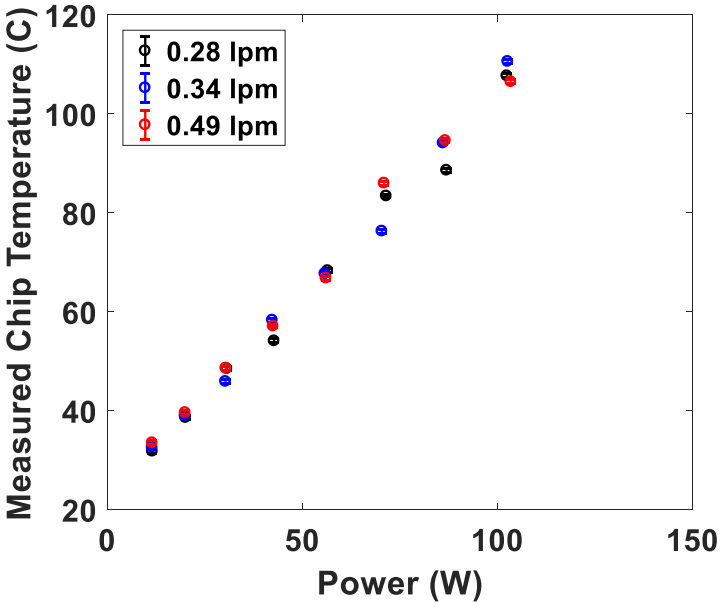


Figure 57 – Measured Chip Temperature at Various Power Conditions (MD MPF)

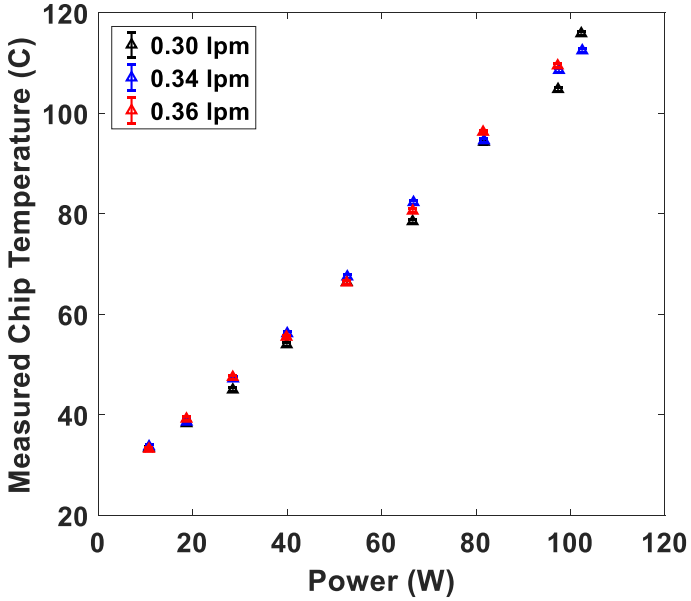


Figure 58 – Maximum Chip Temperature at Various Power Conditions (HD MPF)

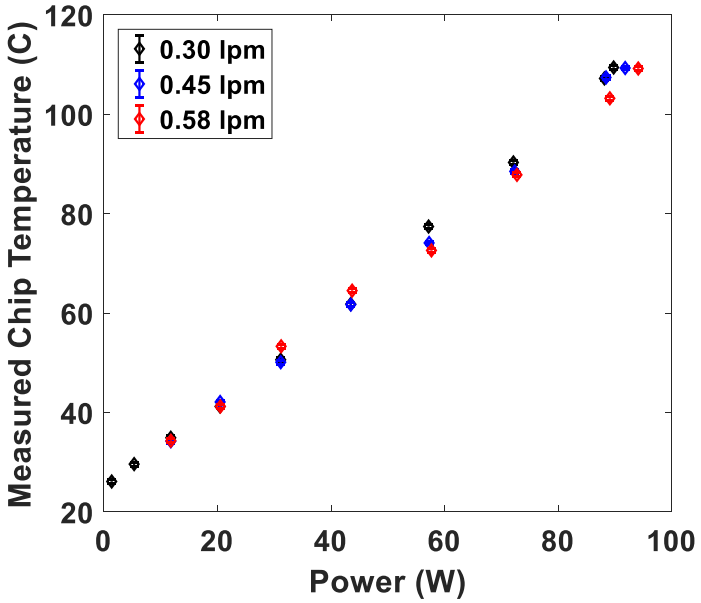


Figure 59 – Measured Chip Temperature at Various Power Conditions (Linear Channel)

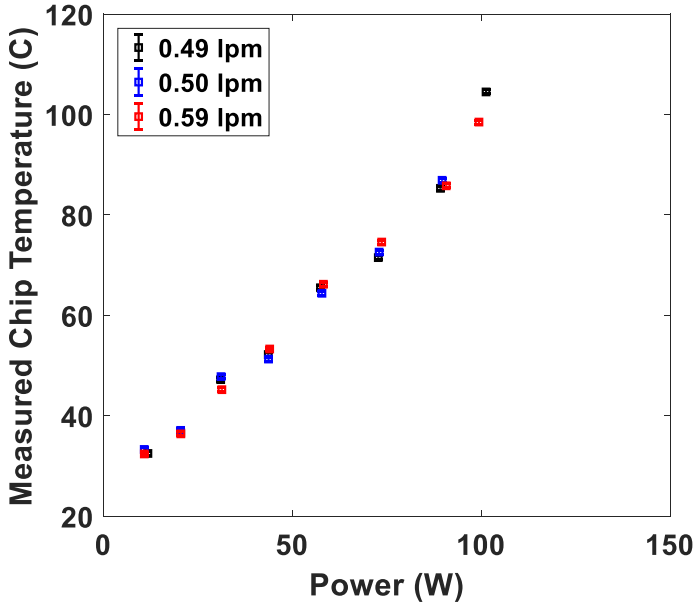


Figure 60 – Measured Chip Temperature at Various Power Conditions (Unstructured Channel)

The highest maximum chip temperature (115.6℃) across the four designs was found at a power condition of 102.3W for design 2 (HD MPF). This occurred at a flow

rate of 0.30 lpm. From **Figure 57 - Figure 60**, it can be noted that the measured chip temperature does not change significantly with changes in flowrate due at each power condition. This behavior can likely be attributed to the fact that each of these flowrates keeps the fluid behavior in the laminar regime ($350 < Re < 800$). Consequently, the heat transfer coefficient does not change significantly in laminar low, so an increase in flow rate will not generate significant changes in the chip temperature. Thus, the changes in chip temperature are solely a function of the power. Furthermore, the thermal resistance across the chip heater and DBC stack for each test section may be too large to allow for effective heat dissipation from the chip.

During the experiments, a change in temperature was measured across the inlet and outlet sections of the heat sinks. This value was used to compute the heat dissipated due to the presence of the heat sink. **Figure 61 - Figure 64** show the performance of heat sink designs 1-4 based on the change in temperature through each test section.

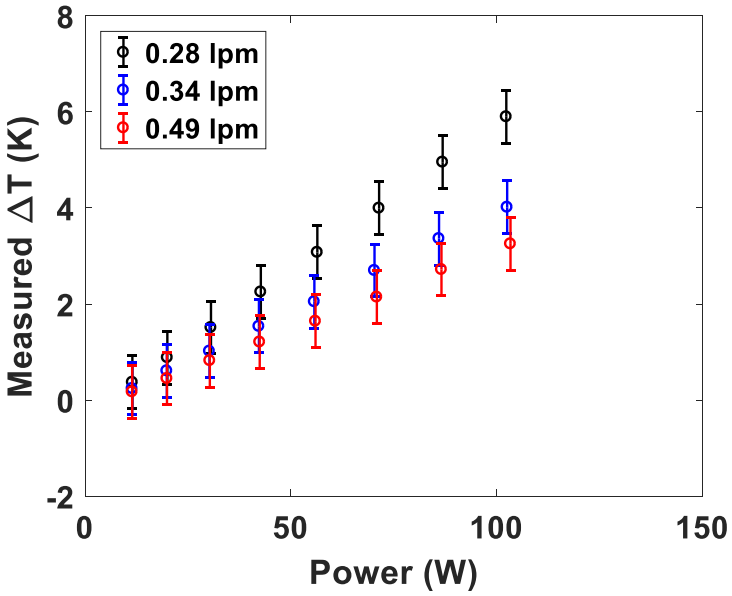


Figure 61 – Measured ΔT at Various Power Conditions and Flowrates (MD MPF)

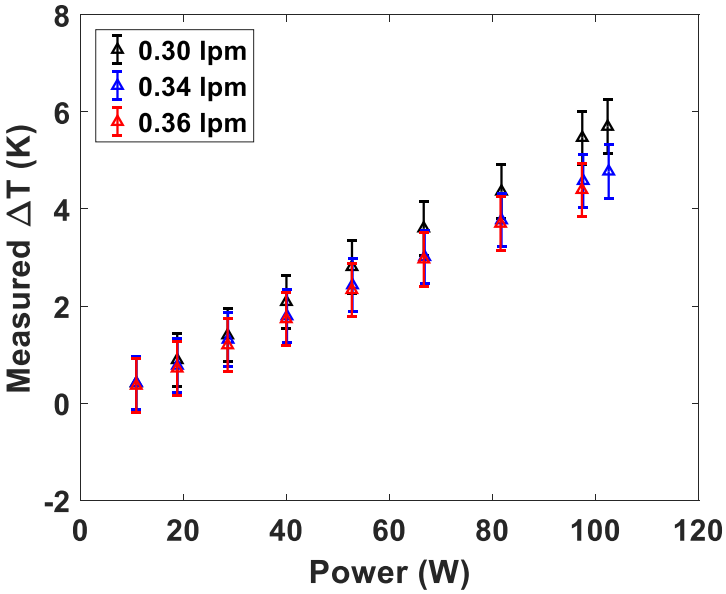


Figure 62 – Measured ΔT at Various Power Conditions and Flow Rates (HD MPF)

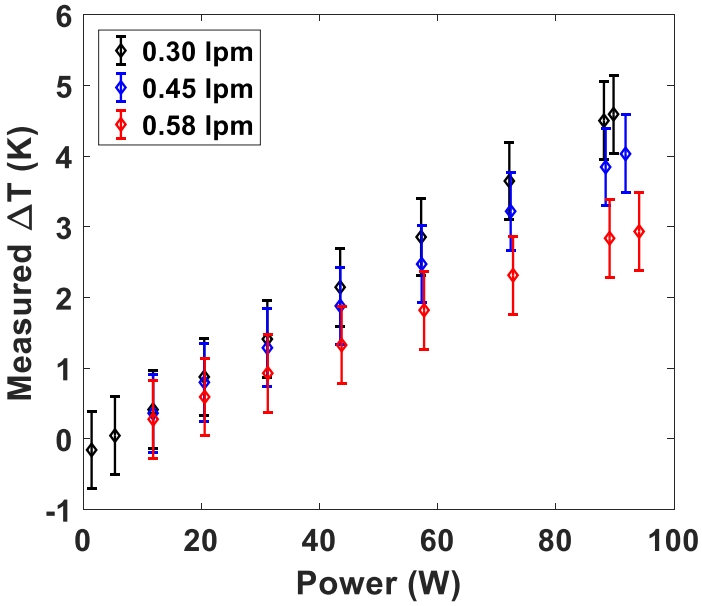


Figure 63 – Measured ΔT at Various Power Conditions and Flow Rates (Linear Channel)

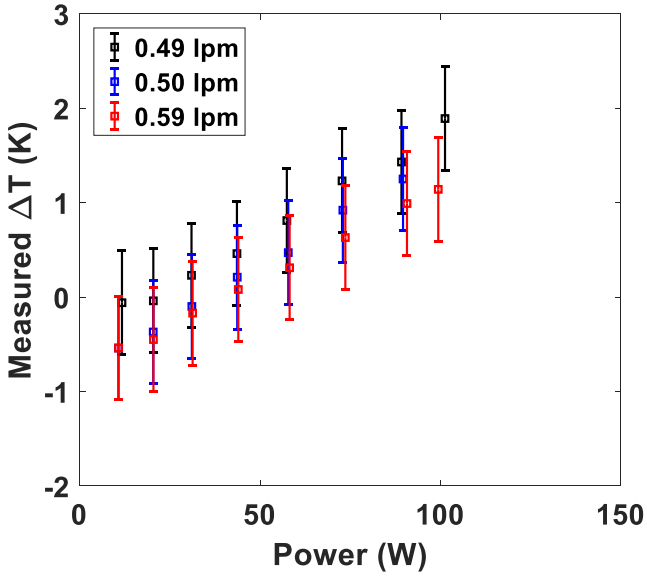


Figure 64 – Measured ΔT at Various Power Conditions and Flow Rates (Unstructured Channel)

The highest change in temperature across the inlet and outlet of the test sections was found in the pin fin designs at the lowest flow rates and highest power conditions.

This followed first principle expectations of total heat rate based on power supplied and considering heat losses from the test section through natural convection. The upward trend for increased change in temperature from the inlet to the outlet of the test section also confirm the intuition that heat sinks with microstructures perform better than heat sinks without microstructures. This is because heat sinks with microstructures have increased heat transfer area that allows for greater heat dissipation. Furthermore, microstructures induce mixing as the flow moves through the heat sink allowing for greater heat dissipation.

To evaluate the performance of each heat sink designed for the DICE concept, a measure of thermal resistance was taken. The thermal resistance essentially gives insight into how well the heat sink is able to drive out heat for given flowrates. For this work, the thermal resistance was plotted as a function of the inlet temperature, measured chip temperature and the power supplied to the system at given flow rates. The plots corresponded to the measured chip temperature at different powers in **Figure 57** - **Figure 60**. With the collected data, a curve was fit to the change in temperature against the power to determine the variations in the change of temperature with increased power for given flowrates. The results of these calculations are tabulated in **Table 6**.

Table 6 – DICE Test Section Thermal Resistance (Horizontal Cooling)

Design	***Flowrate***	***Thermal Resistance***
MD MPF	0.28 – 0.49 lpm	0.81 – 0.84 ºC/W
HD MPF	0.30 – 0.36 lpm	0.88 – 0.89 ºC/W
LC	0.30 – 0.58 lpm	0.89 – 0.95 ºC/W
UC	0.49 – 0.59 lpm	0.68 – 0.75 ºC/W

From **Table 6**, it can be seen that the MD MPF heat sink design had a maximum thermal resistance of 0.84ºC/W for a flowrate 0.49 lpm. The HD MPF heat sink design had a maximum thermal resistance of 0.89ºC/W for a flowrate range of 0.36 lpm. The maximum linear channel thermal resistance was 0.95ºC/W for a flowrate of 0.58 lpm. Finally, the unstructured channel maximum thermal resistance was 0.75ºC/W for a flow rate of 0.59 lpm. Again, these values are only applicable to the power conditions and flowrates used in this work. However, from **Figure 57** - **Figure 60**, it can be seen that the measured chip temperature does not vary much with changes in flowrate. Thus, at higher flowrate values with the same power conditions, the thermal resistance should remain comparable to the thermal resistance at lower flowrate values. From **Table 6**, it can be seen that the thermal resistance for the unstructured channel design was lower than the heat sink designs with micro-structures. As this work sought to reduce the thermal resistance by eliminating some of the interface material layers, this trend was not consistent with the performance expectations of this work. To better understand this

trend, a parametric study was completed for varied thicknesses of the DBC substrate. The parametric study was completed for bottom copper layer DBC thicknesses of 900 µm, 1200 µm, 1400 µm, and 1800 µm. For each bottom copper layer thickness, a convective heat transfer coefficient (8,000 W/m^2-K) with an ambient temperature of 20ºC was applied to the bottom side, and a heat flux of 100 W/cm^2 was applied to the chip. For each model, the heat spreading was evaluated and plotted with a contour plot. The results indicated that the 1800 µm thick bottom copper layer had the most heat spreading through the stack. Thus, the parametric study showed that reducing the DBC stack thickness allowed for machining into the substrate to increase the convective heat transfer area, but implementing the DICE method may increase the thermal resistance because of the lack of available space for heat spreading. The additional heat spreading area that the thicker substrate materials provides, reduces the thermal resistance of the stack. Due to this, the thermal resistance in the unstructured channel was lower for this work, and the reduction in thermal resistance can likely be explained by the inability of the DICE stack to spread the heat well throughout the substrate. Through further simulations, an exploration of the optimal DBC thickness can be found.

As stated earlier, another major consideration in microchannel heatsink design is the pressure drop. The pressure drop is important because it impacts the pumping power. The pumping power provides insight in how much power the pump would need to drive the fluid over the heat sink in order to provide effective heat dissipation. Once the pumping power is calculated, this value is compared to the total power input because in actual power electronic modules, the power supplied to the device will be partitioned off to accommodate the pump. Thus, it is important to understand how much power will be

loss to operate the pump. **Figure 65 - Figure 68** show the performance of each of the four heat sink designs in the area of pressure drop.

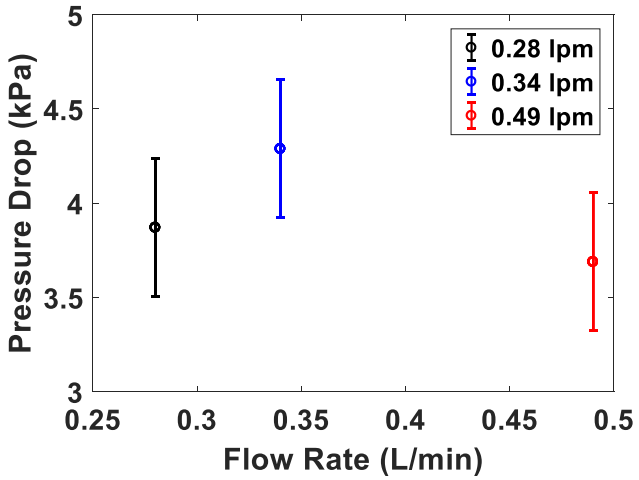


Figure 65 – Pressure Drop Across the Medium Density (MD) MPF Heat Sink

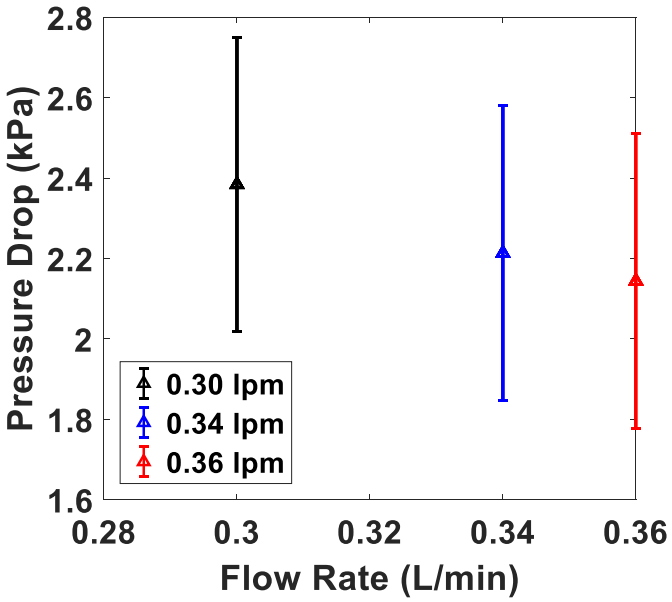


Figure 66 – Pressure Drop Across the High Density (HD) MPF Heat Sink

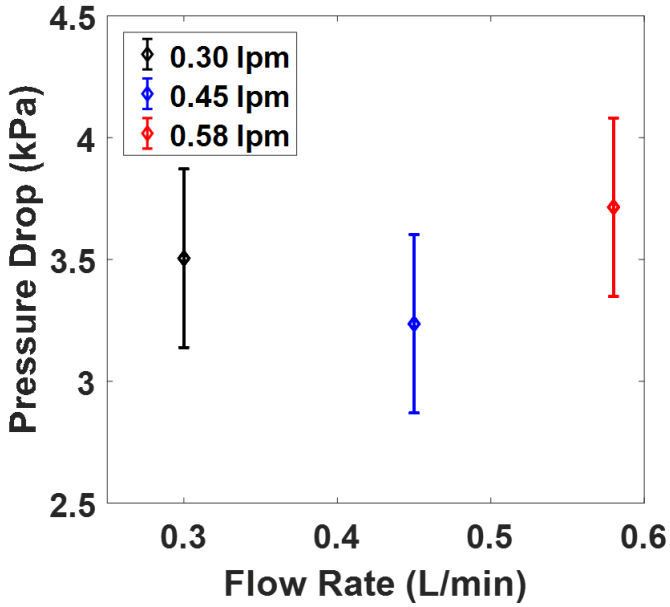


Figure 67 – Pressure Drop Across the Linear Channel Heat Sink

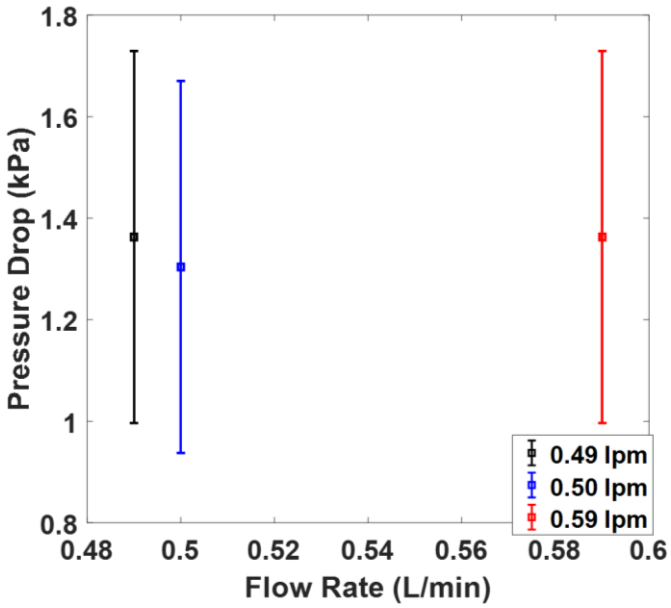


Figure 68 – Pressure Drop Across the Unstructured Channel Heat Sink

From **Figure 65** - **Figure 68**, it can be seen that the pressure drop was highest for heat sink design 1 (MD MPF) and lowest for design 4 (unstructured channel). This trend follows intuition because with additional micro-structures, the pressure that needs to be

overcome for effective fluid flow is greater. The pressure drop values across each heat sink were compared to those found analytically. Although the pressure drop values are less than 5 kPa (acceptable industry standard), their values are somewhat higher than the expected values and the downward trend of pressure drop for increased flowrate counteracts the intuition of the dependence of the velocity on pressure drop. These can likely be attributed to tolerances in the machining of the test sections and substrate material, and possible blockages in due to any unevenness found in the channel or test section.

Through literature, it is commonly seen that linear channels produce high pressure drop values. Thus, researchers have explored pin fin arrays instead. Though this work, the pressure drop in the linear channels is actually slightly lower than that of the micro-pin fins. **Figure 69** shows a comparison between the pressure drop values found with the various heat sink designs.

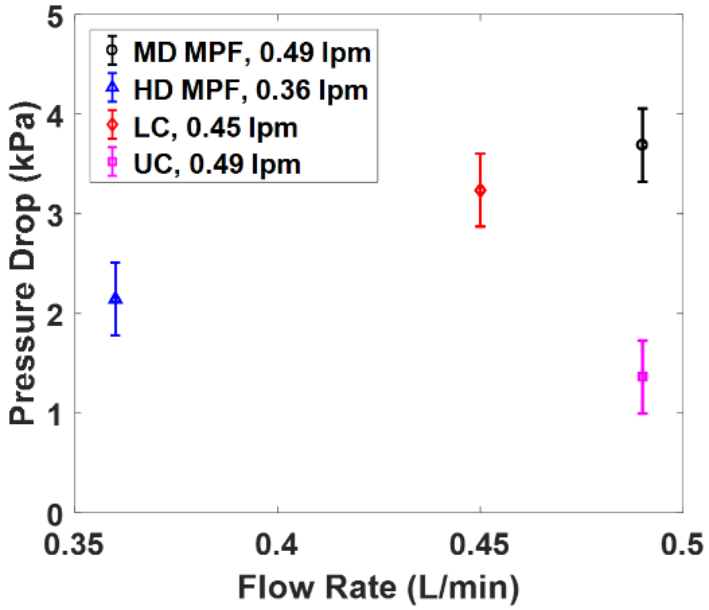


Figure 69 – Pressure Drop Comparisons between the Heat Sink Designs (approximately 0.4 lpm); MD MPF-Medium Density Micro-Pin Fins; HD MPF-High Density Micro-Pin Fins; LC-Linear Channel; UC-Unstructured Channel

From **Figure 69**, it can be seen that the pressure drop in the linear channels falls within the range of uncertainty for the MD MPF. This suggests that the performance in both is somewhat similar in the area of pressure drop. Furthermore, the comparison of pressure drop across the heat sink designs shows that the pressure drop is higher for the micro-structured channels as compared to the pressure drop through the unstructured channels. Although the flowrates are not exactly equal to one another in this plot, this trend follows the expectation that the addition of microstructures introduces flow blockage as the fluid hits the microstructures. Given that the performance of the heat sink is interdependent upon the thermal, hydrodynamic, and electrical performance of the system, there are the increase in pressure drop for an increase in heat transfer shows one of the tradeoffs that arises throughout the design analysis.

4.2 Vertical Cooling Results

4.2.1 Experimental Study

A vertical cooling approach was taken through this work to determine the thermal resistance achievable with higher heat transfer coefficient values as compared to those found in the horizontal cooling methods. The vertical cooling experiments were completed for the 889 µm and 1560 µm diameter jet arrays. The measured values were chip temperature, inlet and outlet temperature, and the pressure drop. Once steady state was reached for each experiment, the measured temperature values beyond this point were averaged for a final temperature reading. As steady-state for flow was reached very quickly, the pressure drop and flowrates were averaged over the varied power conditions applied to each test section. **Figure 70** - **Figure 72** show the variations in chip temperature for each jet array at different flow rates and power conditions.

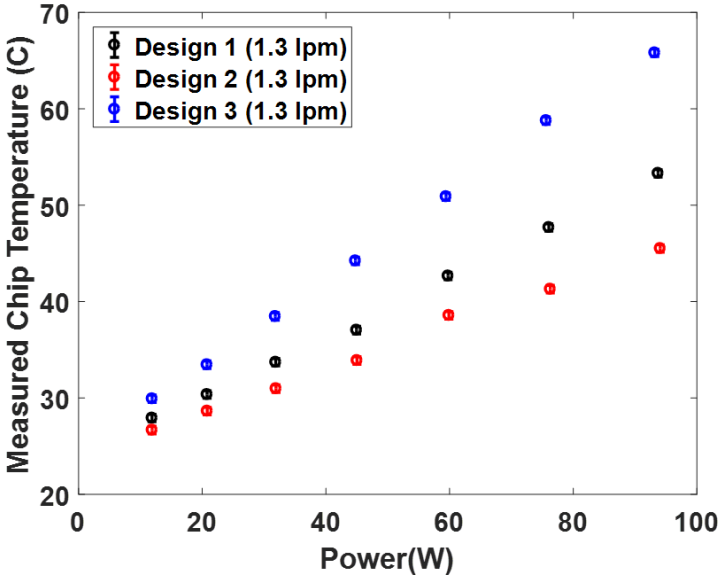


Figure 70 – Experimental Result Comparison between Jet Array Test Coupons on Chip Temperature (1.3 lpm)

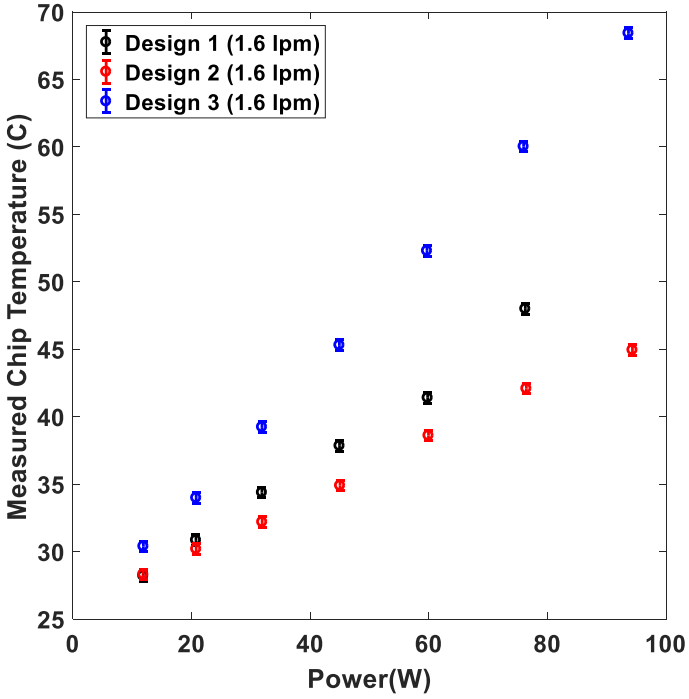


Figure 71 – Experimental Result Comparison between Jet Array Test Coupons on Chip Temperature (1.6 lpm)

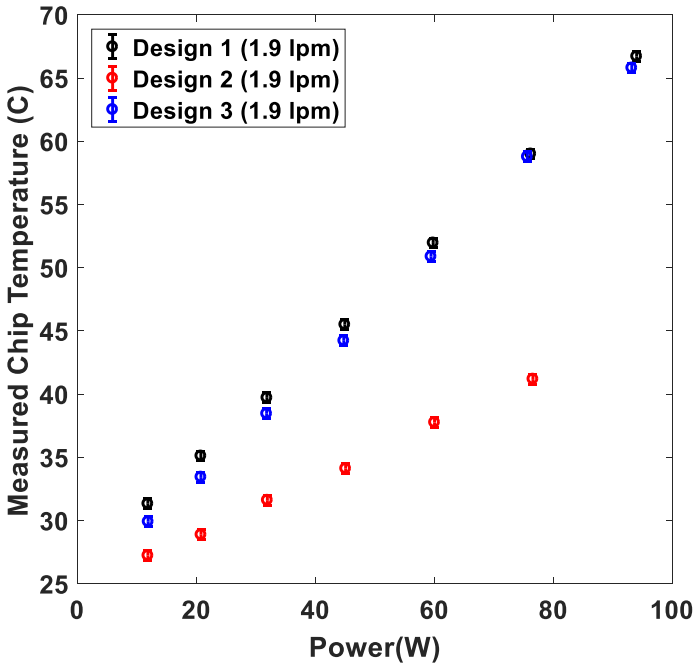


Figure 72 – Experimental Result Comparison between Jet Array Test Coupons on Chip Temperature (1.9 lpm)

As seen in **Figure 70** - **Figure 72**, the measured chip temperature was lowest for design 2 at 27.23℃, at a flow rate of 1.9 lpm. At the highest flow rate, the measured chip temperature was highest in design 1 (31.33℃). This trend closely matched the heat transfer performance expectation of the jet arrays for each design from the analytical model used to design the jet arrays because this array had the smallest diameter with larger spacing between the jets. As stated earlier, designs 1 and 2 employ the same jet diameter, but with increase jet spacing the chip temperature reduces significantly. As the designs varied in jet diameter and spacing, the pressure drop was held somewhat constant through the line and the spray chamber. This conclusion was drawn from the fact that each design had a similar pressure drop from the location above the inlet to the outlet of the test section (after the flow is mixed). Thus, the major pressure drop variations in each

design would likely be found in between the jet array test coupon and the impingement surface.

Through the experiments, it was noted that the temperature difference between the inlet and outlet was very minimal through each test section. This variation in temperature was so small that it fell within the bounds of uncertainty. Thus, the heat dissipated through each of the test sections was unable to be calculated accurately.

To evaluate the performance of each jet array, a thermal resistance calculation was also performed. For the vertical cooling test sections, this value was determined by the change in temperature between the chip and the inlet of the fluid at various power conditions for each jet array. The data for this calculation was taken from the measured chip temperature found in **Figure 70 - Figure 72** for the power conditions applied to each design. The results from this calculation are listed in **Table 7** below.

Table 7 – DICE Test Section Thermal Resistance (Vertical Cooling)

	Flowrate	***Thermal Resistance***
Design 1	1.3 – 1.9 lpm	0.29 – 0.31 ºC/W
Design 2	1.3 – 1.9 lpm	0.21 – 0.23 ºC/W
Design 3	1.3 – 1.9 lpm	0.43 – 0.47 ºC/W

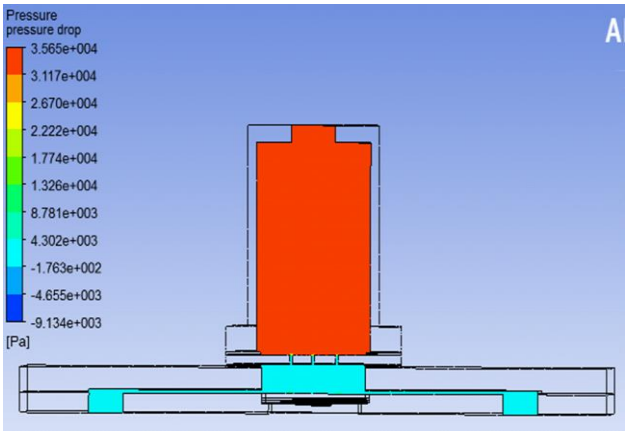
From **Table 7**, it can be seen that the maximum thermal resistance for jet array design 1 was 0.31ºC/W at a flowrate of 1.3 lpm. Design 2 also had a maximum thermal

resistance (0.23ºC/W) at 1.3 lpm. Design 3 has a maximum thermal resistance of 0.47ºC/W at a flowrate of 1.6lpm. As stated earlier, these values are only applicable to the range of flowrates and power conditions applied in this study. In the jet impingement work, the measured chip temperature varied with changes in flowrate. Thus, the thermal resistance of the test section is dependent upon the flowrate though the system. However, for these jet array designs, the thermal resistance is less than 0.5ºC/W. Further study should be completed to determine the thermal resistance outside of these flowrates.

4.2.2 Numerical Models

As stated earlier, the numerical models included the spray chamber, gasket materials, acrylic jet array test coupons, aluminum plates, DBC, and silicon chip heaters. For each model, a half symmetry condition was applied to each test section along the longitudinal axis. A convergence limit of 0.1% of the applied heat flux, and 0.1% of the mass flow rate was used to determine the accuracy of the simulations. After this, the pressure drop was measured across the symmetry plane of the water body. **Figure 73** shows how the pressure and velocity varied across the test section (Design 1).

(a)



(b)

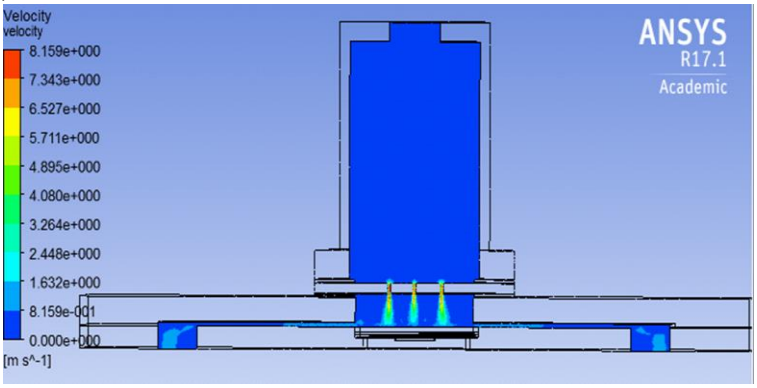


Figure 73 – (a) Pressure Contour through Vertical Cooling Test Section, (b) Velocity Contour through Vertical Cooling Test Section

As shown in **Figure 73**, the behavior of the pressure followed the trends found in the experiments. The maximum pressure was uniform and was found in the spray chamber. Thus, the variations of the pressure were found across the jet array test coupons. As pressure drop is largely a function of the flow velocity, it is expected that the jet arrays with the smaller jet diameters will yield the largest pressure drop across the test section. This expectation comes from the fact that the flow has to contract significantly as it enters the jet array in order to flow across the impingement surface. From jet design, the goal is to make this velocity high to allow for greater heat transfer on the impingement surface. Initially, the pressure drop was simulated across the entire flow

area. However, given the trends seen in the pressure contours, measuring the pressure drop across the jet array and impingement surface was far more beneficial.

4.2.3 Comparison between Experimental and Numerical Models

The experimental and numerical models were in close agreement for the measured chip temperature and the change of temperature between the inlet and outlet of the test sections. **Figure 74** - **Figure 75** show the chip temperatures found numerically and experimentally for designs 1 and 3 respectively. The highest flow rate (1.9 lpm) was chosen for comparison because this flow rate provides the highest HTC in the jet array designs. Designs 1 and 3 were chosen for experimental and numerical modeling comparisons.

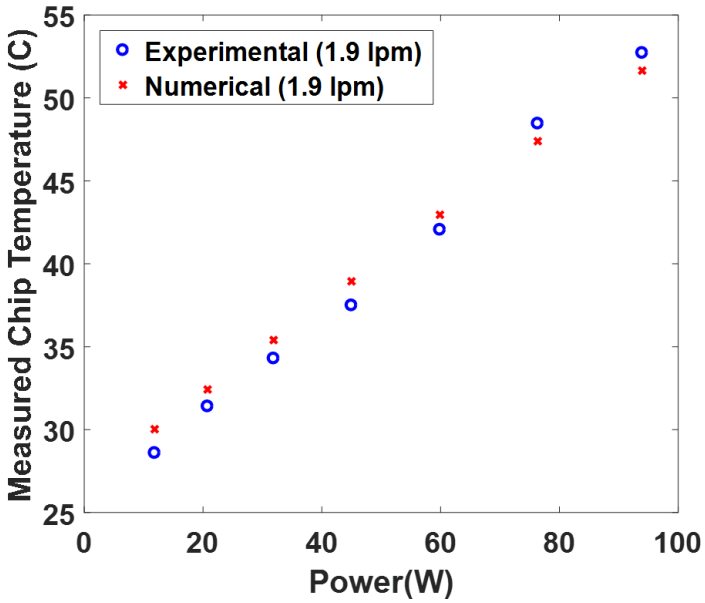


Figure 74 – Chip Temperature Comparison between Numerical Models and Experiments (Design 1)

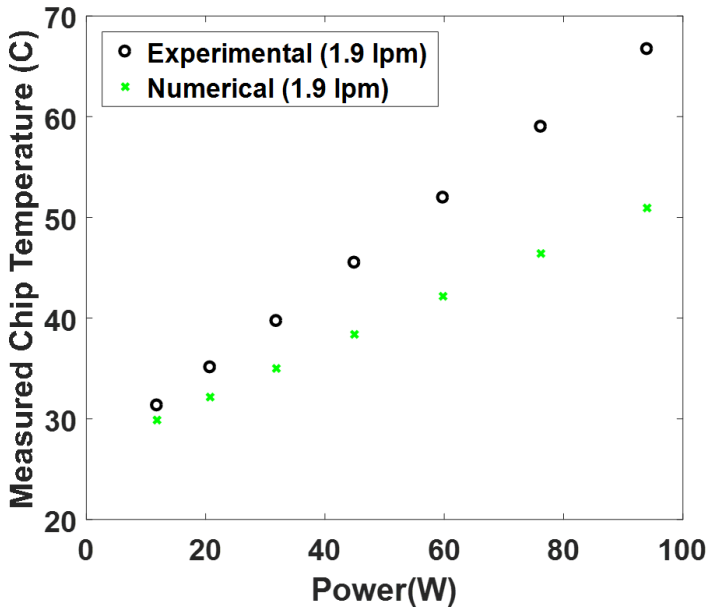


Figure 75 – Chip Temperature Comparison between Numerical Models and Experiments (Design 3)

As seen in **Figure 74** and **Figure 75**, the temperatures for each of the chips in each jet design closely correlated to those measured experimentally. Although the variations in these values were minimal, further refinement of the mesh could allow for more accurate convergence in the modeling.

The temperature difference between the inlet and outlet of test sections in the numerical models was very small and closely correlated to the change in temperatures seen experimentally. As these were on the order of a one-, or two-tenths of a degree, and the uncertainty of the thermocouples was approximately three- to-four-tenths of a degree, a more accurate thermocouple would need to be used to calculate the heat dissipation from each jet array configuration. As the trends were similar across all flow rates, **Table 8** lists the final values for pressure drop, maximum velocity, and maximum area-averaged chip temperature.

Table 8 – Jet Array Numerical Model Results (1.9 lpm)

	Design 1	***Design 3***
Pressure Drop (kPa)	35	15
Maximum Velocity (m/s)	8.159	4.985
Maximum Chip Temperature (°C)	52	50
Maximum Reynolds Number	8462	9071
Nusselt Number	55.09	79.47
Heat Transfer Coefficient (W/m^2-K)	35,699	30,461

For each of the parameters in the above table, a flow rate of 1.9 lpm was used because this flow condition yielded increased turbulence; thus improved heat dissipation. The maximum velocity was used to determine the maximum Reynolds number for each jet array. This value is used to compute the nusselt number using correlations by Martin [56] and consequently the heat transfer coefficient. Equation 19 above was used to compute the nusselt number for each of the staggered jet arrays. The above calculations of nusselt number and HTC are based on the maximum Reynolds number and the Prandtl number. Thus, the values may overestimate the heat transfer coefficient found through the experiments on the impingement surface.

4.3 Numerical Modeling for Thermal Resistance

The parametric study completed over the forced convection and boiling heat transfer regions showed the heat transfer coefficient value required for the DICE test sections to develop a thermal resistance value that overcame that of the conventional stack. This study gave insight into the type of cooling scheme needed for this work to make the thermal resistance produced with the DICE concept heat sinks comparable to

the thermal resistance produced using conventional cooling methods on the conventional stack. For each model, a heat flux of 100 W/cm^2 was applied to the silicon IGBT chip. A thermal conductance for the thermal epoxy layer (thermal conductivity, K = 2.5 W/m-K, epoxy thickness of 60 μm) was set between the chip and the top-side of the DBC. Each model was run to achieve an element quality of 0.1 or greater to ensure that the results were accurate. For each DICE test section and the conventional stack, the thermal resistance was calculated using equation 28,

$$\sum R = \frac{\Delta T}{Q} \tag{28}$$

where, ΣR is the thermal resistance, ΔT is the difference in temperature between the average chip temperature and the fluid ($T_{ambient}$ = 26.85°C), and Q is the heat applied to the chip. **Figure 76** shows the performance of each of the DICE test sections as compared to that of the conventional stack in terms of the thermal resistance.

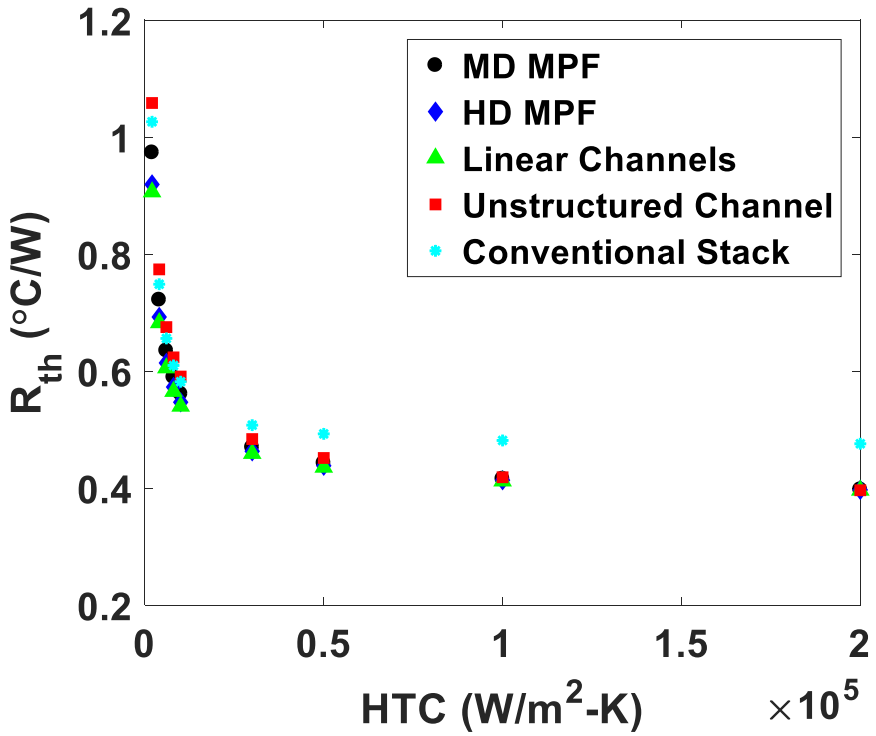


Figure 76 – Parametric Study Results for DICE test section and Conventional Stack Thermal Resistance at Various Heat Transfer Coefficient Values

From **Figure 76**, it can be seen that the thermal resistance of the unstructured channel is highest at the lower HTC values. This lower range of HTC values covers the natural convection through the lower range of forced convection. Also in this range of HTC values, the thermal resistance decreases between the resistance value of the medium density (MD) micro-pin fin (MPF), the high density (HD) MPF, and the liner channels. At lower HTC values, the conventional stack thermal resistance is in the same range as the DICE test sections. Thus, at low HTC values, the conventional stack and the DICE test sections perform comparably, and the DICE stack offers little to no improvement over the conventional stack. At 3,000 W/m^2-K, the thermal resistance is reduced in the DICE test sections; thus, the performance of the DICE test section is superior to the performance of the conventional stack. Beyond 3,000 W/m^2-K, the conventional stack

generated an increasingly higher thermal resistance than the DICE test sections as the heat transfer coefficient is increased. Additionally, as the heat transfer coefficient is increased to 200,000 W/m^2-K, the performance of the DICE test sections does not vary much as the heat sink area is varied. This trend is as expected because the thermal resistance is inversely proportional to the heat transfer coefficient and the area of the heat sink. Equation 29 describes this relationship,

$$\sum R = \frac{\Delta T}{Q} = \frac{1}{HTCxA} \tag{29}$$

where, ΣR is the thermal resistance, Q is the power supplied, ΔT is the change in temperature between the chip and the ambient fluid, HTC is the heat transfer coefficient, and A is the area of the heat sink. With this, at low HTC values, any changes made to the heat transfer surface area will directly affect the thermal resistance. However, at high HTC values, an increase in the area does not contribute much to the thermal resistance. Thus, as HTC values are increased, the thermal resistance is largely driven by the HTC rather than the heat sink area. **Figure 76** also confirms our initial expectation that a higher HTC value would be needed in the DICE test sections to achieve a lower thermal resistance as compared to the conventional stack. At higher HTC values, the improvement of the thermal resistance in the conventional stack is limited. Thus, **Figure 76** shows that there is a HTC limit for which the conventional stack thermal resistance can no longer be improved. However, as the HTC is increased, the thermal resistance for the DICE stack can continue to decrease. Overall, **Figure 76** suggests that the DICE test section will continually outperform the conventional stack in terms of thermal resistance for HTC values from 3,000 W/m^2-K and beyond.

The DICE test section thermal resistance values found via the horizontal cooling experiments were also in the range of thermal resistances found in the parametric study. As the HTC value was increased (as seen with the vertical cooling scheme), the chip temperatures, thus thermal resistance, was significantly lowered. If the thermal resistance of the vertical cooling scheme is compared to those in **Figure 76**, the thermal resistance values fall below all of the horizontal cooling DICE test sections and the conventional stack. As the vertical cooling scheme used the unstructured channel DICE test section, **Figure 76** also shows that the thermal resistance can be reduced by shifting to a vertical cooling method.

4.4 Warpage Impact on DICE Stack

In conventional power modules, the numerous layers in a power electronics package provide additional materials for thermal and mechanical stability and reliability. Thus, although eliminating some of these layers improves the thermal resistance, there are tradeoffs that need to be considered before implementing DICE methods in industrial packages.

From the numerical modeling, it was found that the deformation was greatest in the linear channel power device stacks where the chip heater was mounted using sintered silver. As stated earlier, this overall deformation value of 55.579 μm was found for a fraction of the size of the actual power electronics module, and this space occupied only one chip heater. In conventional power modules, the full array with multiple IGBT and diode devices mounted in the module can span 134.2 mm^2 [28]. As these numerical models do not extend the full range of industrial power modules, their deformation values

can only be used as estimates of deformation to determine which materials are less or more likely to induce warpage in the power module.

Through this warpage study, it was found that the sintered silver mounted devices resulted in the largest amount of deformation at the edges of the silicon chip heater, as well as the highest von-mises stresses. **Figure 77** provides images of the deformation between the four heat sink designs attached using Epotek H2OE epoxy. For each of these designs, a support condition was applied to the bottom of the pin/ plates/ linear channels. A fixed support was applied here because during reflow, the substrate is usually held to the mounting system using a vacuum holding the pieces down on this side.

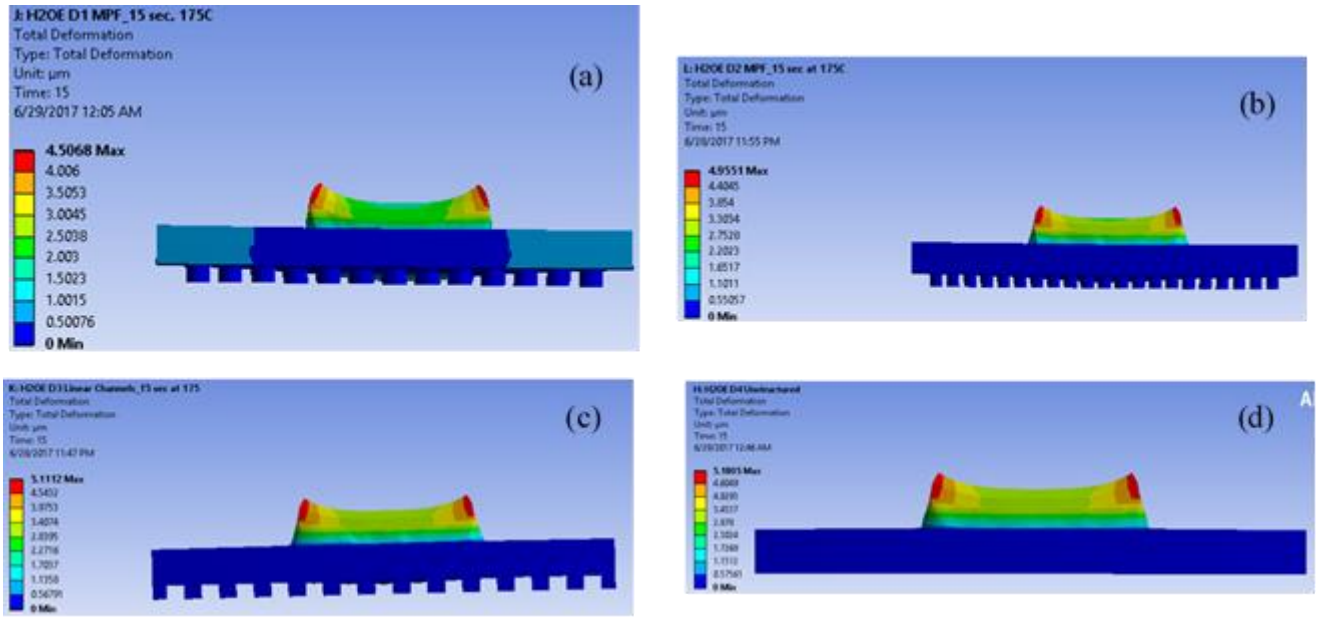


Figure 77 – Warpage in Power Modules with Epotek H2OE Mounted Chip Heaters (a) MD MPF, (b) HD MPF, (c) Linear Channel, (d) Unstructured Channel

As the models followed a similar deformation pattern with an increase in magnitude of deformation, only plots from the Epotek H2OE Epoxy are plotted. The deformation values for all of the materials are listed in **Table 9**.

Table 9 – Warpage Analysis Values for Heat Sink Designs with Different Thermal Interface Materials

	Total Deformation	**Von Mises Stress**
Epotek H2OE Epoxy		
MD MPF	4.5068 µm	49.924 MPa
HD MPF	4.9551 µm	36.478 MPa
Linear Channel	5.1112 µm	34.562 MPa
Unstructured Channel	5.1805 µm	34.377 MPa
Conventional Stack	15.279 µm	129.49 MPa
SAC 305 Solder		
MD MPF	15.109 µm	30.317 MPa
HD MPF	15.871 µm	24.075 MPa
Linear Channel	16.008 µm	18.649 MPa
Unstructured Channel	15.993 µm	15.307 MPa
Conventional Stack	15.25 µm	30.42 MPa
Sintered Silver Paste		
MD MPF	52.919 µm	219.92 MPa
HD MPF	51.196 µm	268.5 MPa
Linear Channel	55.579 µm	267.47 MPa
Unstructured Channel	57.283 µm	271.43 MPa
Conventional Stack	57.042 µm	220.74 MPa

From the table, it can be seen that using sintered silver paste could induce the most amount of warpage in the DICE stack. However, the deformation is about 50 µm. As the industry accepted deformation is 50 µm, the difference in the deformation is not very significant.

Considering the larger deformation and stress values found in the models that used sintered silver as compared to those in the epoxy-mounted models, it appears the epoxy would be a better interface material to use for mounting these chip heaters. However, the epoxy presents higher thermal resistance challenges that impact effective heat dissipation from the power stack as compared to the thermal resistance of sintered silver. The thermal resistance is inversely proportional to the thermal conductivity. The thermal conductivity of the H2OE epoxy is 2.5 W/m-K while that of the silver paste is 200 W/m-K [77]. Thus, a higher thermal conductivity material will result in low thermal resistance. Furthermore, through the warpage studies, it can be noted that the conventional stack yielded lower total deformation in the solder and sintered silver-mounted models over the DICE stack with the same materials. Overall, the highest deformation and von-mises stresses were found in the silicon chip for the chip mounting with sintered silver, then SAC305 and lastly the epoxy. However, as stated earlier, these deformation values are within the industry accepted deformation values. Furthermore, as thermal resistance and thermal conductivity are closely related, the tradeoff found in using this material may be in the area of deformation as long as the chip performs optimally.

To better simulate the warpage impacts of the various thermal interface materials, additional warpage studies completed over the range of reflow temperatures (220°C - 240°C) were completed for the SAC305 solder and the sintered silver paste. The reflow temperature of SAC305 solder is between 217°C - 220°C, so a reflow temperature of 220°C was applied with a temperature ramp up of 15 seconds [78]. The reflow temperature of sintered silver paste is 240°C, so a reflow temperature of 240°C was

applied with a temperature ramp-up of 15 seconds [68]. The results from these additional studies are listed in **Table 10**.

Table 10 – Warpage Analysis for SAC305 and Sintered Silver at Reflow Temperatures of 220°C and 240 °C

	Total Deformation	**Von Mises Stress**
SAC 305 Solder at 220°C		
MD MPF	19.57 µm	39.17 MPa
HD MPF	19.58 µm	39.23 MPa
Linear Channel	19.68 µm	39.36 MPa
Unstructured Channel	19.69 µm	39.46 MPa
Conventional Stack	19.65 µm	39.34 MPa
Sintered Silver Paste at 240°C		
MD MPF	75.84 µm	313.46 MPa
HD MPF	73.69 µm	381.92 MPa
Linear Channel	79.96 µm	381.75 MPa
Unstructured Channel	82.41 µm	387.25 MPa
Conventional Stack	81.74 µm	314.59 MPa

From **Table 10**, it can seen that the SAC305 solder produced a higher deformation value and higher von-mises stress value at the higher reflow temperature of 240°C as compared to the deformation and von-mises stresses at a reflow temperature of 175°C. In the models, it can also be seen that the conventional model yielded a slightly higher deformation value as compared to the DICE test section values.

In the sintered silver mounted heater models, the deformation was greatest for the unstructured heat sink test section. Overall, the sintered silver mounted heater models had

much higher deformation and von-mises stresses than the deformation and stress values of the SAC305 solder mounted models. This trend followed expectation because the reflow temperature was higher than that used in the solder and epoxy models. However, sintered silver has superior thermal and electrical properties as compared to those of the epoxy and solder. Again, each of these models represents only a portion of the full power module array, the actual deformation expectation may be different from those reported here.

CHAPTER 5. CONCLUSION

This work explored two cooling schemes (horizontal and vertical cooling) to improve heat dissipation from a power electronic device. A number of conventional cooling methods employ air cooling, but liquid cooling schemes have been analyzed because of the increased HTC found in fluids other than air. For this work, single-phase liquid cooling was applied to a chip heater attached through a directly integrated cooling of electronics (DICE) method. The expectation was that a reduction in the number of interface materials would result in a reduced thermal resistance through the stack, and enhance heat transfer through the use of microstructure features machined into the backside of a direct bond copper substrate. A pseudo-optimization method was used to design the micro-structured heat sinks as well as the jet array test coupons used in the vertical cooling methods. Numerical models were developed to validate the experimental results and provide estimates of performance if various materials were changed in the stack.

Through this work, it was found that the vertical cooling test sections generated a lower thermal resistance as compared to the horizontal cooling test sections. Thus, the measured chip temperature for the vertical cooling schemes was lower than the chip temperature of the horizontal cooling schemes. This result suggested that vertical cooling (perpendicular fluid flow) could be a more promising cooling technique to adequately dissipate heat from a power electronics chip as compared to horizontal cooling (parallel fluid flow). This trend also confirmed the intuition of better heat transfer capability with vertical cooling as compared to the heat transfer capability of the horizontal cooling

scheme. This intuition was drawn from the fact that turbulent flow (seen in the vertical cooling methods) allows for higher HTC values than laminar flow (seen in the horizontal cooling methods); thus, better heat transfer from a surface.

A parametric study was completed over HTC values from 2,000 W/m^2-K – 200,000 W/m^2-K, to validate this expectation. Through this, it was found that at an HTC value of 3,000 W/m^2-K, and a heat flux of 100 W/m^2, the thermal resistance of the DICE test sections was lower (0.459°C/W) than the thermal resistance of the conventional stack (0.508°C/W) with the same loading conditions. This study confirmed the intuition of this work (the thermal resistance was reduced through the elimination of interface material layers). Additionally, the study gave insight to the HTC limits faced by both the conventional stack and the DICE test sections. This chapter reviews the experimental and numerical results, the parametric study and draws conclusions about each of cooling schemes.

5.1 Horizontal Cooling

Through the horizontal cooling experiments, it was found that the values for inlet and outlet temperatures varied slightly with changes in flow rate. However, the chip temperatures did not change much with increased flow rates. As stated earlier, this trend is likely explained by the fact that the flow over the micro-structured heat sinks was maintained in the laminar flow regime. Here, the heat transfer coefficient does not vary drastically, so increased in flow will likely not produce significant reduction in the chip temperature. Thus, the chip temperature is largely a function of the resistance found in

the stack based on how the wires were mounted to the chip, and how the chip was assembled in the DICE stack.

The pressure drop through each of the heat sinks followed an increasing trend from the unstructured surface heat sink, the MD MPF, the HD MPF, and finally the linear channels. This trend was expected because as structures are inserted into a flow region, they induce mixing. This improves heat transfer, but it generates a higher pressure drop. The pressure drop though the linear channels was highest likely due to the fact that the flow has no space to release some of the pressure buildup before the flow leaves the channel. Across all horizontal cooling designs, however, the pressure drop and change in temperature were all on the same order of magnitude.

5.2 Vertical Cooling

Through the vertical cooling experiments, it was found that although the heat dissipation could not be measured exactly, the cooling method was effective in significantly reducing the measured chip temperature. This chip temperature reduction increased as the flow rate increased through each of the vertical cooling configurations. This trend is likely explained by the fact that the flow rates applied to these test sections allowed for the system to induce turbulent mixing. In turbulent flow, the heat transfer improves as more mixing is induced. Thus, at higher flowrates, the chip temperature was its lowest as compared to the chip temperature at lower flowrates.

The pressure drop across each of the jet configurations was somewhat constant at each flowrate in the experiments. Thus, once deemed accurate, numerical models were used to determine the actual pressure drop across the test section (including the spray

chamber) and the pressure drop between the jet array test coupon and the impingement surface. From this, it was found that the lowest overall pressure drop was found in the jet array with the largest jet diameter (design 3), while the highest pressure drop was found in the jet array with the smallest jet diameter (designs 1 and 2). This trend follows the intuition that if flow is expected to pass through smaller areas, the pressure buildup will be greater than the pressure buildup in a larger area space. Another note to consider is that the although the number of jets plays a role in the performance of the jet array, the spacing between each jet plays a more significant role in removing heat effectively (as shown by the minimum chip temperature found using the jet array with the largest diameter, and fewest number of holes).

5.3 Cooling Scheme Comparison

5.3.1 Chip Temperature

Through the experiments and numerical models, it was found that the measured chip temperature using a vertical cooling scheme was reduced by 42% at one power level as compared to the chip temperature in a horizontal cooling scheme at the same power condition. The numerical modeling correlated well with the experimental results for the vertical cooling DICE test section at a flow rate of 1.3 lpm, and the lower power conditions of the DICE system with 1.9 lpm. Through numerical model optimization, the differences in the chip temperature could be better explained.

5.3.2 Pressure Drop

Although the pressure drop was similar across the various jet array test coupons, the overall pressure drop found in vertical cooling was significantly higher than those seen in the horizontal cooling. As pressure drop is a function of the flow rate, it is intuitive that the vertical cooling schemes would generate a higher pressure drop. This is one of the tradeoffs associated with vertical cooling as compared to horizontal cooling.

5.3.3 Thermal Resistance

As expected, if using a 1D conduction model, the thermal resistance through the stack should remain constant once the chip is mounted to the DBC heat sink. Accounting for spreading resistance, and convective heat transfer, this value would vary. Using the pin fin arrays, the anticipated reduction in thermal resistance as compared to a conventional stack was approximately 25%. This calculation included the spreading resistance through the IGBT, epoxy and DBC layers. This estimate applied the thicknesses of the materials referenced in [23] where a resistance of 0.53 K/W for a stack that reduced the package thickness by 1/5 was found with a heat transfer coefficient of approximately 10,000 W/m^2-K. This estimated heat transfer coefficient was determined from the initial modeling of the horizontal cooling test sections.

In the horizontal cooling experiments, the flow was maintained in the laminar regime, so the resistance in each test section attachment reduced the ability of the heat sink to remove heat effectively. However, in the vertical cooling experiments, the flow was turbulent, and the vertical cooling methods were able to remove heat from the chips more effectively. The maximum thermal resistance in the horizontal cooling work was on

the order of 0.95ºC/W, while the maximum thermal resistance in the vertical cooling work was on the order of 0.30ºC/W.

A parametric study was completed in this work to determine the HTC requirements for the DICE test section to outperform the conventional stack. To evaluate this, numerical models were developed for each of the heat sink designs, and for the conventional stack. The thermal resistance was calculated using the chip temperature, ambient fluid temperature, and the power supplied to the heater. With this, it was found that the DICE stack outperforms the conventional stack thermal resistance at an HTC of 3,000 W/m^2-K and beyond. The parametric study also showed that at 100,000 W/m^2-K and beyond, an increase in HTC does not change the thermal resistance of the stack. Thus, there is an HTC limit to improving the performance of the conventional stack. Beyond which, the device thermal resistance cannot be overcome by any increase in the convective thermal resistance. Additionally, the parametric study suggested that as the heat sink area was increased, the thermal resistance was decreased in the lower ranged of forced convection HTC values. Overall, the study confirmed that the DICE concept is best used with high HTC values to overcome the thermal resistance developed in the stack layers.

5.4 Warpage and Manufacturing

The warpage between the various DICE configurations was compared across SAC305, Epotek H2OE epoxy, and sintered silver. These materials were chosen because of their frequent use in industry, and their material properties as compared to other interface materials. Through the studies of material warpage, it was found that reducing

the stack using the DICE method may induce some manufacturing challenges that consequently impact device reliability. As the stack is significantly reduced in the DICE configuration, the high temperatures used to allow for material reflow during mounting of the device on the DBC were not easily dissipated through the layers below the thermal interface material in the stack. Thus, in order for this method to be implemented in industry, further study needs to be completed for other chip connection techniques and other materials to allow for adequate heat spreading through the stack during reflow.

Implementing the DICE concept in industry would require additional design considerations to allow for the integration of the heat sink with the power module. As stated earlier, conventional power modules are generally developed by mounting the IGBT/diode chips onto the DBC substrate. From this, the chips are wire-bonded to develop the circuitry of the module. Once each of the chips is mounted, overflow material is poured into the power module casing and on top of the chips. This allows for the chips to remain in place and the overflow provides a sealant for the chips. After the module is built, the heat sink, thermal interface materials and heat spreaders are mounted to the module. Finally, the heat sink is attached using another interface material to allow for heat dissipation. The DICE concept reduces the number of interface and material layers needed in the stack, and it applies the heat sink to the bottom surface of the DBC. Thus, in order to implement the DICE concept in industrial power modules, a co-design approach will need to be taken.

Currently, the electronics and thermal components are developed separately. To allow for co-design, a few boundary conditions need to be shared across the industries. The available spacing, size, and weight of the power module/heat sink would be shared

boundary conditions. Each of these conditions will limit how large and how bulky the designers can make their parts. In developing the power module array, the electrical team would need to space their chips in such a way that there is no electrical interference/cross-over between the chips. This interaction between the chips is also a thermal issue because, as the chips get hot, and the heat spreads, the heat from one chip can impact the overall temperature of an adjacent chip. Thus, effective cooling needs to be applied to ensure that chips are not overheating due to surrounding chips.

For EVs, the IGBT chips used in the power modules are vertical devices. Thus, as the devices operate, the current flows in a vertical pattern. This flow of the current allows for the devices to perform electrically as optimally as possible. However, this flow of current impacts the design choices of the thermal teams developing the cooling systems. If the cooling systems are made in such a way that they interfere with the flow of the current, the devices can become damaged. Thus, the thermal teams need to coordinate with the electrical teams when designing the heat sink coolers.

Another consideration in DICE concept implementation for conventional power modules is in the area of localized cooling. Power module arrays are usually developed from multiple IGBT chips and diode chips. As these are not arranged directly next to one another, there are areas of high temperature throughout the power module. Given this, there are hot spots that are formed at these locations that need to be met by effective cooling. To address these areas specifically, the thermal team needs to be familiar with the arrangement of the chips in the module to develop heat sinks that provide cooling to these specified areas. Thus, the implementation of the DICE concept will only be made possible through the co-design efforts of both the electrical and thermal teams.

CHAPTER 6. FUTURE WORK

Although this work provided much insight into the implementation and design of integrated cooling for power electronic devices, there are a few areas that should still be analyzed and optimized. This chapter reviews the changes that could be made to further improve the work.

6.1 Experiments

In the experiments, the largest contribution to uncertainty was found in the measurements for change in temperature across the inlet and outlet ports of each test section. The thermocouples used in this work were OMEGA K-type thermocouples (generally with an uncertainty of ±2.2°C) and they were re-calibrated upon purchase to reduce the uncertainty associated with the measurements. The final uncertainty values were (±0.3889°C) for each thermocouple. This uncertainty is not too large, but when applied to determine the change in temperature, the uncertainty propagates to a level that is too high for small changes in temperature. This was seen particularly with the jet impingement work, as the change in temperature was too small to capture using the thermocouples. Thus, more accurate thermocouples should be used for future studies of this work.

Another change to be made in the experiments is to minimize the losses through the test section materials. Through analytical calculations, the heat lost to the environment was deemed minimal. However, as the experimental models did not always match perfectly with the numerical models, covering the entire test section with

insulation would have minimized the heat lost to the environment, and this step would have given a better understanding of the sources of error in the results. Furthermore, the chip temperature for the horizontal cooling was taken at relatively the same location through each power condition of each experiment. However, if a thermocouple was permanently attached to this surface, the readings could have been more accurate. To check for this, a repeatability study was completed to ensure that the same readings were found during each experiment. Although the results were the same each time the experiment were the same, affixing a thermocouple would possibly yield better results.

A parametric study was completed to assess the heat spreading in a DICE stack with various bottom layer DBC thicknesses. From this study, it was found that the thicker the bottom layer of the DBC was, the better the heat was spread through the stack. This study was explored because of the low thermal resistance found in the unstructured channel heat sink as compared to the thermal resistance in the heat sinks with microstructures. From this study, it was found that thicker bottom layer DBC substrates yielded lower maximum surface temperatures; thus, better heat spreading. In future studies of the DICE concept, the test sections should be made to either be thicker, or a heat spreader layer should be applied to the bottom of the DBC before the system is cooled.

As stated earlier, there was some variability in the pressure drop values measured in the horizontal cooling test sections as compared to those estimated through the analytical modeling. The overall difference between the analytical models and the experimental models was about 2 kPa. The increase in pressure drop in the experimental models can possibly be explained by the design of the test section. The DBC substrates

were cut into 3 x 3 cm test pieces. This cutting process may have induced slight warpage in the substrate. Thus, although the DBC substrate was meant to seat flush in the test section, any un-evenness in the DBC or test section channel could introduce additional sources of flow blockage that would result in an increase of pressure drop. To address this, future studies should measure and minimize any warpage in the substrate, and tighter tolerances should be applied to the heat sink design.

The heat sink designs used in the horizontal cooling experiments were developed using a pseudo-optimization technique. The design analysis allowed for only a partial optimization because of the constraints placed on the available material and heat sink size. Thus, to account for manufacturability, and material availability, the heat sink designs used aspect ratios that produced a lower overall heat sink efficiency than those found at alternate aspect ratios and spacing. For future studies of this work, a full optimization for the heat sink designs should be completed to develop high efficiency heat sink geometries. Through analytical models for the linear channel heat sinks completed in this work, it was found that the heat sink efficiency could be increased by changing the spacing dimensions and the number of channels. Thus, future studies of this work could explore different linear channel heat sinks accounting for variations in these parameters.

For the horizontal and vertical cooling experiments, the test section was initially designed in such a way that the heat sinks plates could be attached and removed to minimize the variation in machined components for the test section. This decision was made because of the tolerances that are required in machining. By using the same test sections, there was greater assurance that the results would be comparable. Furthermore,

this design allowed the fluid to flow throughout the test section with no blockages that could impact the pressure drop or thermocouple readings. However, designing the test section in this manner lead to leaking challenges through the top of the test section and through the sides where the plates were joined. Thus, in the future, the enclosure should be made where there are minimal locations of potential leakage.

One method to address the test section leakage could be through designing a 3D printed cooler system. This would allow for complex geometries, but it would provide a complete seal for the system. This concept was initially reviewed in the first iteration of the microchannels cooler. The micro pin fins were designed in SolidWorks, and the test section was printed using a high temperature acrylic plastic. The challenge with this manufacturing method was in cleaning out the support material, and the ability of the material to maintain its integrity at very high temperatures. The expectation with this enclosure geometry was that the enclosure would be a proof of concept model that could suggest the ability of metal-based additive manufacturing techniques for increased design complexity and variability. However, one challenge with this design could be in the electrical isolation layer (typically aluminum nitride) placed between the copper plates in the DBC. Additionally, 3D printing could be used to develop the jet impingement cooling design to better integrate the cooling method without multiple components (e.g. spray chamber, base plates, gasket materials).

Lastly, to simulate actual high-power device conditions, the experiments could be run at higher heat duties. The goal of power electronic devices is to meet high heat fluxes. With the advancements in technology and literature, this range is expected to be about 100 W/cm^2 up to a few kW/cm^2. The, DICE concept has been tested at the lower end of

this range, but further work should be done to explore higher heat fluxes. Additionally, localized cooling scenarios should be tested because hot spots are usually formed in actual power devices.

6.2 Numerical Modeling

The numerical models completed in this work provide a basis for validating the experimental models testing the DICE concept.

In the warpage studies, numerical models were developed to compare different interface material behavior during reflow. The results from these models provided insight to deformation and stress induced as a result of the structural and thermal properties of the interface materials. From this, tradeoffs with using various materials were identified. However, these models just provided a basis of comparison. For future studies of warpage, a full array of power electronics devices should be modeled with the exact spacing and thickness of the devices developed in industry. Furthermore, with a full model, a mesh independence study should be completed to ensure that the final deformation values are accurate.

The results from the jet impingement work corresponded well with expectations and the experimental models. However, a mesh independence study should be run on these models to ensure that improvements to the mesh will not yield significantly different results from models with fewer elements in the mesh. Additionally, the numerical models developed for the horizontal flow channels should be optimized to validate the experimental work.

APPENDIX A. TEST SECTION EQUIPMENT MANUFACTURER'S UNCERTAINTY

Pressure Transducers (OMEGA PX309-015GV)	±0.25% FS
Flow Meter (McMillan S114-4E-S4) [0.2-2.0 lpm]	±1% FS
Flow Meter (McMillan S114-8E-S4) [0.5-5.0 lpm]	±1% FS
Thermocouples (OMEGA K-Type)	±2.2ºC
Thermocouple Calibrator (OMEGA CL122)	±0.7ºF
Keithley 2450 Sourcemeter	±0.012%
FLUKE 54IIB Thermometer	0.05% ± 3ºC

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