# PHYSICS AND DESIGN OF SOI FED BASED MEMORY CELLS

by

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# Physics and Design of SOI FED Based Memory Cells

A Dissertation submitted in partial fulfillment of the requirements for the degree of Doctor of Philosophy at George Mason University

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## DEDICATION

This is dedicated to my father, Zuhdi Badwan. This work would not have been completed without his unlimited support and encouragement.

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**ABSTRACT**

PHYSICS AND DESIGN OF SOI FED BASED MEMORY CELLS

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Memory arrays occupy a very large area in chip designs; yet memory cell scaling lags significantly transistor scaling. With transistor channel lengths in the nanoscale regime, the six transistor static random access memory (6T-SRAM) and the single transistor dynamic random access memory (DRAM) cells both suffer from excessive leakage current. Therefore, there is a widely recognized need for urgent progress in memory technology to meet the increasing demand for highly for compact, high density and low power memory arrays.

Several new memory device approaches are currently under extensive investigation around the world. One such approach is the thin capacitively coupled thyristor (TCCT) memory cell where a gate assisted PNPN thyristor is utilized as a memory cell, which exploits the ON and the OFF states of the thyristor. TCCT breaks through the performance density trade-off of conventional SRAM and DRAM and it is compatible with CMOS process which make it a promising alternative to the current memory cells.

In this dissertation we present a new volatile memory cell with promising characteristics, which improves on the TCCT concept above. The proposed cell is based on the field effect diode (FED), and it is essentially a p-i-n diode to which two closely spaced, independent gates have been added between the anode and the cathode. This new cell is similar to the TCCT in concept and operation, however, the thyristor-like structure is gate-induced in the FED cell whereas it is built-in in the TCCT cell. TCAD simulation results showed that the FED cell has important advantages such as high read 0/1 margins, fast write/read, thermal stability and good retention time.

We also re-evaluate the recent interpretation of the physical storage mechanism of the thyristor based memories as the presence (state "1") or absence (state "0") of charge under the gate: we demonstrate that this interpretation is incorrect, and we describe the correct physical mechanism, by carefully studying the carrier profiles within the TCCT and FED memory cell structures. This new understanding should result in better cell design and feasibility analysis.

# CHAPTER 1 INTRODUCTION

## 1.1 Semiconductor Memories

Semiconductor memory arrays capable of storing large quantities of information are essential to all systems. The amount of memory required in a particular system depends on the type of application, but, in general, the number of transistors utilized for the data storage function is much larger than the number of transistors used in logic operations. The ever-increasing demand for larger data storage capacity has driven the fabrication technology and memory development towards more compact design rules and, consequently, toward higher data storage densities [1].

The 2013 International Technology Roadmap for Semiconductors (ITRS) stated that the scaling of metal-oxide-semiconductor field-effect transistor (MOSFET) continues with the emergence of new technologies to extend complementary metal-oxide semiconductor (CMOS) down to and beyond 22-nm technology node [2]. However, the CMOS scaling has deviated from the trends predicted by Moore and the scaling rules set forth by Dennard et al. due to fundamental physical and technical limitations in recent decades [3, 4]. The pace of future CMOS scaling will inevitably slow down and eventually stop probably at a 5-nm node where the lithography scale approaches a few times of atomic dimension [5-7]. Scaling limitations of ultra-thin gate oxide, channel length modulation, and FET series resistance have become a growing concern on

maintaining speed, density, reliability and power dissipation. Recent logic device research and development to enable solutions toward CMOS scaling challenges has taken the torch and carried it forward thus far. For example, barriers such as doping, carrier transport and series resistance scaling have been effectively avoided by innovations such as source/drain processes upon silicon-on-insulator (SOI) structure, multi-gate FET, and Bipolar-CMOS (BiCMOS) technologies [8-12].

Semiconductor memories are generally classified according to the type of data storage and the type of data access. Read only memory (ROM) circuits allow, as the name implies, only the retrieval of previously stored data and do not permit modifications of the stored information contents during normal operation. ROMs are non-volatile memories, i.e., the data storage function is not lost even when the power supply voltage is off. Currently, main types of non-volatile memory technology have been investigated, including ferroelectric random-access memory (FeRAM), magnetic random-access memory (MRAM), resistive random-access memory (RRAM), phase-change random-access memory (PCRAM), and Flash memory [13-17]. Non-volatile memory is typically employed for the task of secondary storage or long-term storage, which usually does not require fast operation speed or integration 3 density. Most types of non-volatile memory have limitations and are not suitable for use as primary storage or on-chip memory,

Read/write (R/W) memory circuits, on the other hand, must permit the modification (writing) of data bits stored in the memory array, as well as their retrieval (reading) on demand. This requires the data storage function to be volatile, i.e., the stored data are lost when the power supply voltage is turned off. The R/W memory circuit is

commonly called random access memory (RAM). Compared to sequential-access memories such as magnetic tapes, any cell in the R/W memory array can be accessed with nearly equal access time. Based on the operation type of individual data storage cells, RAMs are classified into two main categories: static RAMs (SRAM) and dynamic RAMs (DRAM) [1].

The SRAM cell consists of a latch, therefore, the cell data is kept as long as the power in turned on. During the past decades, the size of cache memory (SRAM) in the central processing unit (CPU) has been doubled several times as a feasible strategy to increase the CPU capability and performance. However, increasing SRAM will decrease CPU net information throughput because it is volatile and occupies a large chip floor space. The DRAM cell consists of a capacitor to store data and a transistor to access the capacitor (1T-1C). Cell content is degraded mostly due to junction leakage current in the storage node. Therefore, the cell data must be read and rewritten periodically (refresh operation) even when memory arrays are not accessed. The DRAM has lower cost and higher density than the SRAM, DRAM but the operation speed is slower in DRAM than in SRAM. Figure 1.1 shows the basic DRAM and SARM memory cells.

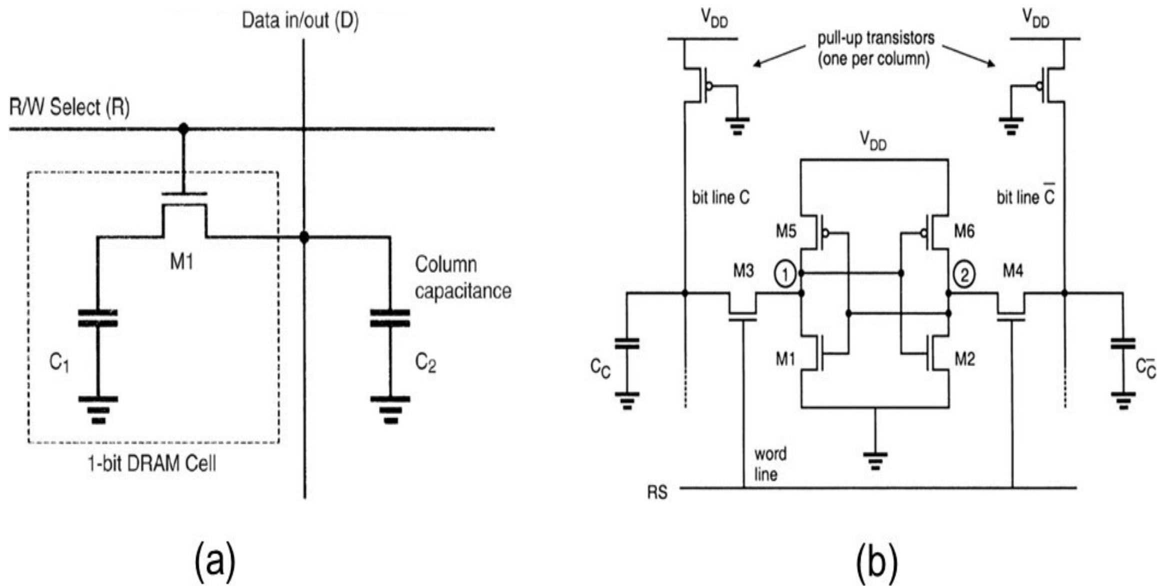



**Figure 1.1 1T-1C DRAM (a) and 6T SRAM (b) [1]**

## 1.2 Floating Body Memory Cells

The floating body memory cell (FBC) is considered one of the simplest semiconductor memory cells ever proposed. It consists only of a single MOSFET with its body floating. Similar to the flash memory, FBC memory mechanism is based on changing the threshold voltage ($V_{th}$) of the MOSFET. However, the storage node is different; $V_{th}$ in FBC is changed through electrical charges stored in the floating body; whereas $V_{th}$ in the flash memory is changed by the charges stored in the floating gate. This difference in the storage node is what makes the FBC a volatile memory and the flash memory a none volatile one [18].

FBC is commonly realized using an n-type MOSFET built on SOI substrate. Data "1" is written by injecting holes to the p-type body of the MOSFET, while Data "0" is

written by pulling the holes out. When “1” is stored, the holes accumulated in the p-Body will reduce $V_{th}$ of the FET due to the body effect. Thus for the same gate voltage; more drain current will flow from the cell when “1” is stored than when”0” is stored. This is shown in Figure 1.2.

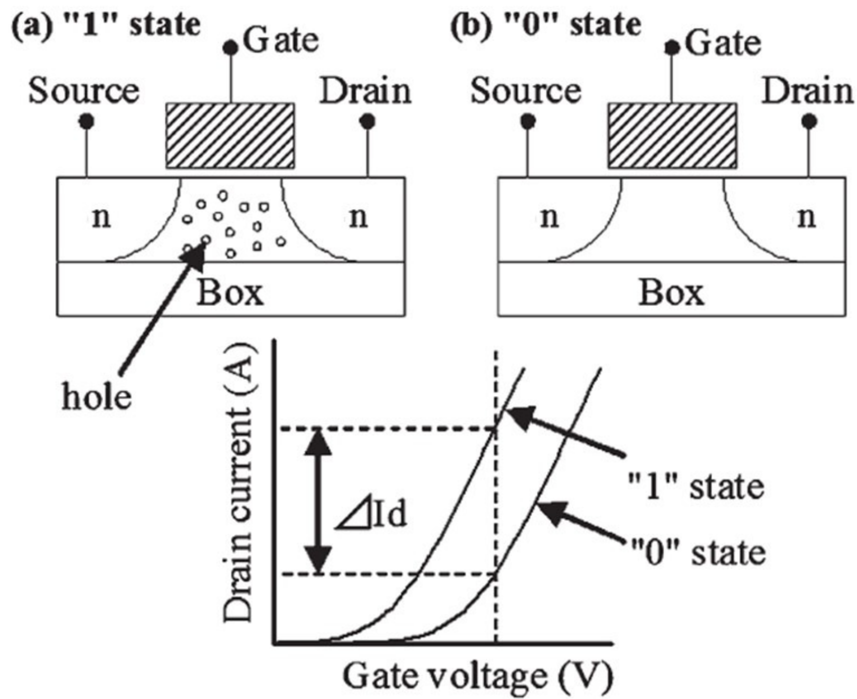



**Figure 1.2 FBC memory concept: data “1” is stored when holes are accumulated in the body (a) while data “0” is stored when holes are removed (b) [19]**

To write “1”, holes are pushed to the p-body by impact ionization [20] (for high speed applications) or by using the gate induced drain leakage effect (GIDL) [19] (for low power applications). To write “0”, the p-n junction between the body and the drain is

forward-biased, ejecting the stored holes from the body. The cell content is read by observing the drain current while the MOSFET is operating in the linear current mode.

The FBC has small cell size (only 1 transistor) and its process is almost compatible with the standard CMOS. Furthermore, FBC is a gain cell with nearly nondestructive read operation. This makes it capable of escaping from scaling limit that conventional DRAM cells face because of the explicit capacitor [18-21]. All these features make the FBC an attractive option especially for embedded memory.

## 1.3 Silicon on Insulator (SOI)

The idea of realizing semiconductor devices in a thin silicon film that is mechanically supported by an insulating substrate has been around for several decades [22]. The first description of the insulated-gate field effect transistor (IGFET) which evolved into the modern MOSFET is found in the patent of Lilienfield dating from 1926 [23]. This patent depicts 3 terminals: source, drain and gate. The source to drain current is controlled by a field effect from a gate dielectrically insulated from the rest of the device. The piece of semiconductor that constituted the active part of the device was a thin semiconductor film deposited on an insulator. In a sense, it thus can be said that the first MOSFET was semiconductor on insulator device. The technology of that time was not mature enough to produce a successfully operating Lilienfield device. IGFET technology was then forgotten for a while, completely overshadowed by the enormous success of the bipolar junction transistor (BJT) discovered in 1947 [22].

It was only years later, 1960, when technology had reached a level of advancement sufficient for the fabrication of good quality oxides. The advent of the

monolithic integrated circuits gave MOSFET technology an increasingly important role in the world of microelectronics. CMOS technology is currently the driving technology of the whole microelectronics industry.

CMOS integrated circuits are almost exclusively fabricated on bulk silicon for two well-known reasons: the availability of the electronic-grade material produced by either the Czochralski or by the float zone technique and because a good quality oxide can be readily grown on silicon, a process which is not possible on germanium or on compound semiconductors. Yet, modern MOSFETs made in bulk silicon are far from the ideal structure described by Lilienfield. Bulk MOSFETs are made in silicon wafers having a thickness of a few hundreds of micrometers, but only the first micrometer at the top of the wafer is used for transistor fabrication. Interactions between the devices and the substrate give rise to a range of unwanted parasitic effects.

One of these parasitics is the capacitance between diffused source and drain and the substrate. This capacitance increases with increasing substrate doping. As a result, it becomes larger in modern submicron devices where the doping concentration in the substrate is higher than the previous MOS technologies. Source and drain capacitance is not limited to the obvious capacitance of the depletion regions associated with the junction but it also includes the capacitance between the junctions and the heavily-doped channel stop located underneath the field oxide. In addition, latch-up, which consists of the unwanted triggering of a PNPN thyristor structure inherently present in all bulk CMOS structures, becomes a severe problem in devices with small dimensions.

Some workarounds have been found to reduce the parasitic components. The area of the source and drain junctions can be minimized by creating local interconnections and placing contacts over the field area. Furthermore, the occurrence of latch up can be reduced by using epitaxial substrates or deep trench isolation. These techniques, however, necessitate sophisticated processing, which impacts both the cost and the yield of manufacturing.

If an SOI substrate is used, quasi-ideal MOS devices can be fabricated. The SOI MOSFET contains the traditional three terminals, however, the full dielectric isolation of the devices prevents the occurrence of most of the parasitic effects experienced in bulk silicon devices. To illustrate this, Figure 1.3 schematically represents the cross-sections of both bulk CMOS inverter and an SOI CMOS inverter. Most parasitic effects in bulk CMOS devices find their origin in the interaction between the device and the substrate. Latch up in bulk device finds its origin in the parasitic PNPN structure of the CMOS inverter represented in Figure 1.3 (a). The latch up path can be symbolized by two BJTs formed by the substrate, the well and the source and the drain junction. Latch up can be triggered by different mechanisms such as node voltage overshoots, displacement current, junction avalanching and photocurrents. For latch up to occur, the gain of the loop formed by the two BJTs should be larger than unity. In an SOI CMOS inverter the silicon film containing the active devices is thin enough for the junction to reach through the buried insulator. Latch up path is rule out because there is no current path to the substrate. In addition, the lateral PNPN structures contain heavily doped bases (the N+ and P+ drains) that virtually reduce the gain of the bipolar devices to zero.

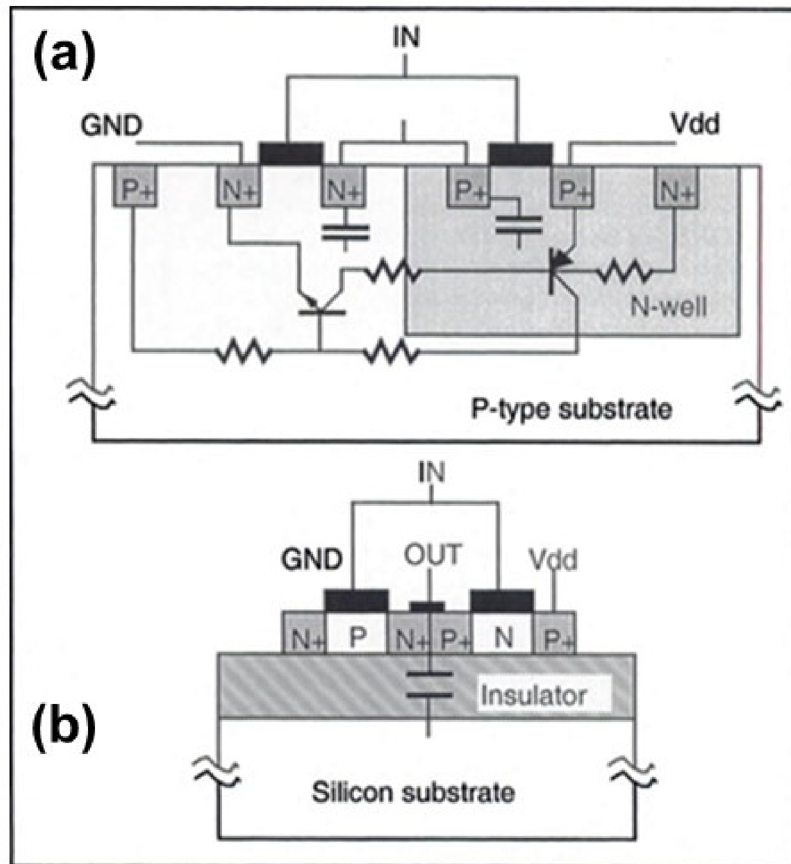



**Figure 1.3 A cross-section of CMOS inverter, bulk (a), and SOI (b) [22]**

Bulk circuits utilize reverse biased junctions to isolate device from one another. In n-type MOSFET, for example, the drain is always positively biased or zero biased with respect to the substrate. The depletion capacitance of the drain junction reaches a maximum value when the drain voltage is zero and it increases with increased substrate doping concentration. Modern submicron circuits use high substrate doping concentrations which contributes to an increase in the junction capacitance. In addition,

an added parasitic capacitance occurs between the junctions and the channel stop implant underneath the field oxide. In SOI circuits the maximum capacitance between the junctions and the substrate is the capacitance of the buried insulator, which tends toward zero if thick insulators are used. This capacitance is proportional to the dielectric constant of the insulator material. Silicon dioxide is used as a buried insulator and it has a dielectric constant three times smaller than silicon, therefore, a junction located on a buried oxide layer is approximately three times smaller than that of a bulk junction. In addition, a lightly doped, p-type silicon wafer can be utilized as mechanical support. In that case, a depletion region can be created beneath the insulator, which further contributed to a reduction in junction-to-substrate capacitance.

SOI CMOS technology is also attractive because it involves fewer processing steps than bulk CMOS technology and because it suppresses some yield hazards factors present in bulk CMOS. This can be illustrated by taking the example of realizing a shallow junction and making contact to it, Figure 1.4. Fabricating a shallow junction is not a simple task in CMOS, if a thin SOI substrate is used, on the other hand, the depth of the junction will automatically be equal to the thickness of the silicon film. Electrical contact to a shallow junction can be made using a metal or an alloy. In bulk silicon devices, unwanted reactions can take place between the silicon and the contact, such that the contact punches through the junction. This effect is well-known in the case of aluminum (aluminum spiking), but it can also occur with other materials. Such a junction punch through gives rise to uncontrolled leakage currents. If the devices are realized in thin SOI material, the N+ or P+ source and drain diffusions extend to the buried insulator.

In that case, there is no metallurgical junction underneath the metal-silicon contact area, and hence no leakage will be produced if some uncontrolled metal-silicon reaction occurs.

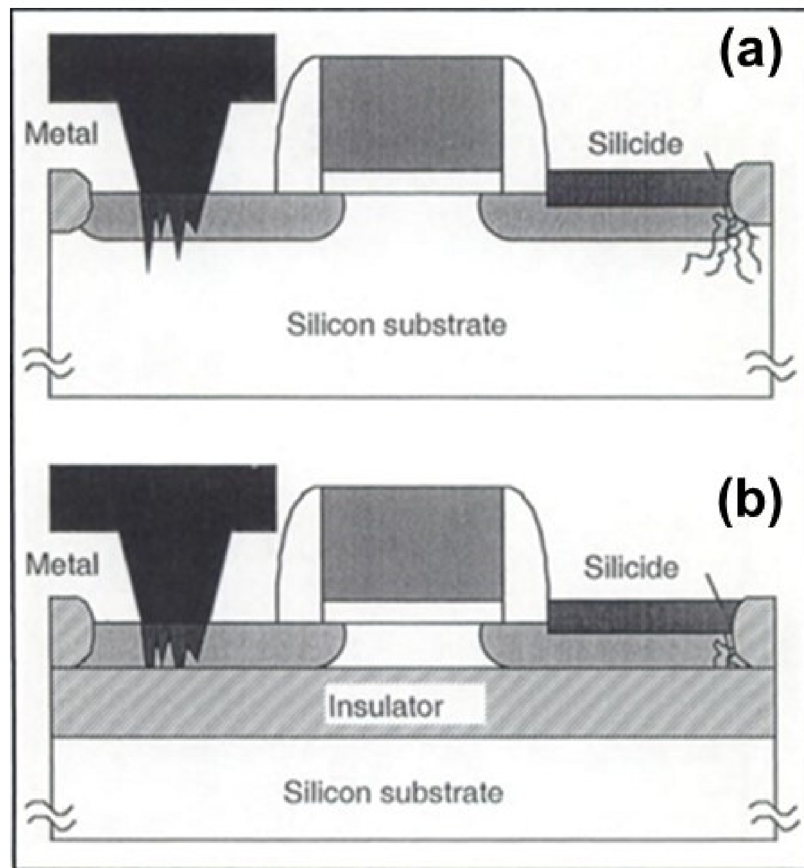



**Figure 1.4 Contact punch through in bulk CMOS due shallow junctions (a). This problem does not exist in SOI CMOS because the junctions extend to the buried insulator (b) [22]**

It is a fact that the SOI integrated circuits are a commercial success. One of the reasons for this success is the availability of large quantities of high-quality SOI wafers.

## 1.4 Technology Computer Aided Design (TCAD)

TCAD refers to using computer simulations to develop and optimize semiconductor processing technologies and devices. TCAD simulation tools solve numerically the fundamental physical equations, such as the Poisson and the Continuity equations [24] that characterize the semiconductor devices properties and predict their behavior under different bias conditions. These equations are solved for discretized geometries that imitate the silicon wafer or the layer system within the device.

TCAD simulations are used widely in the semiconductor industry. As technologies become more complex, the semiconductor industry relies increasingly more on TCAD to cut costs and speed up the research and development process. In addition, semiconductor manufacturers use TCAD for yield analysis which includes monitoring, analyzing, and optimizing their process flows, as well as analyzing the impact of process variation.

### 1.4.1 Simulation Space of the Memories Structures

Design and optimization of the memory cells presented in this dissertation was implemented using Sentaurus TCAD simulation tools by Synopsis.

Cell structures and operations were carried out using two dimensional (2D) isothermal numerical simulations where the model for carrier transport is the drift diffusion model [25, 26].

The mobility models used account for the effect of impurity, surface roughness, carrier-carrier scattering, and high field velocity saturation [27, 28].

Electron and hole lifetimes were modeled according to the Shockley-Read-Hall (SRH) model and were assumed to be equal. Their doping dependence was according to the Scharfetter relation [28] (with $\tau_{max}$ = 10 ns, $\tau_{min}$ = 0 ns, $N_{reff}$ = 5x$10^{16}$ $cm^{-3}$ and $\gamma$ = 1) and the temperature dependence was as described in [29].

## 1.5 Dissertation Organization

This dissertation will focus on utilizing the field effect diode (FED) as a random access memory cell. It will also propose a novel interpretation of the memory (storage) mechanism for the thyristor based memory. The dissertation is organized as follows:

Chapter 2 presents the thyristor and the thyristor based memory cells. The thyristor structure, properties, and the device physics behind its modes of operation are discussed in the first part of the chapter. The second part of the chapter reviews the concept of the thyristor based memory and the various methods used to implement and optimize this type of memories.

Chapter 3 provides an overview of the FED structure and its modes of operation. It also explores the required bias conditions to operate the FED as a thyristor. Then, the forward breakdown of properties the FED based thyristor are considered.

The FED SRAM cell is introduced in chapter 4. First, the cell structure and its basic operation is explained. After that, multiple writing and holding schemes for the cell as well as the memory array are examined.

Chapter 5 focuses on enabling the FED as a DRAM cell. Chapter 6 revisits the operation of the dynamic thyristor based memory; in an effort to provide an alternative

understanding for the physical memory mechanism based by studying the carrier profiles in the cell structure.

Finally, a summary of the dissertation and a discussion for future research will be presented in Chapter 7.

# CHAPTER 2 THYRISTOR BASED MEMORY CELLS

## 2.1 The PNPN Thyristor

A thyristor is a four layer pnpn structure. The outer p- and n- type regions serve as emitters or injectors for minority carriers. The n- and p- sandwiched between the emitters are the n- and the p- bases. The basic structure and the typical doping profiles of the thyristor are shown in Figure 2.1 and Figure 2.2, respectively, the n-base is usually wider than the other layers and it has the lowest doping for high breakdown voltages.

The principal current flows into the anode (A), connected to the p- emitter, through the four layer structure and out of the cathode (K), connected to the n-emitter. Holes are injected across the p-emitter junction (J1) into the n-base. Some of these holes diffuse to the collector junction (J2) where they are swept into the p-type base region as majority carriers. These injected holes replenish the hole population of the p-base replacing holes lost to recombination in the neutral base or in the n-emitter junction space charge region and to injection into the n-emitter. Similarly, electrons are injected into the p-base by the n-emitter junction (J3). Some of these electrons also diffuse to the collector junction and are swept to the n-type base, where they replenish the electron population of the n-base. Additional control electrodes are sometimes used to contact the base layers when the application requires them. Base electrodes are generally used to: suppress high-

frequency transient switching effects, initiate switching (cause the device to turn on) or to assist the turn off process [30].

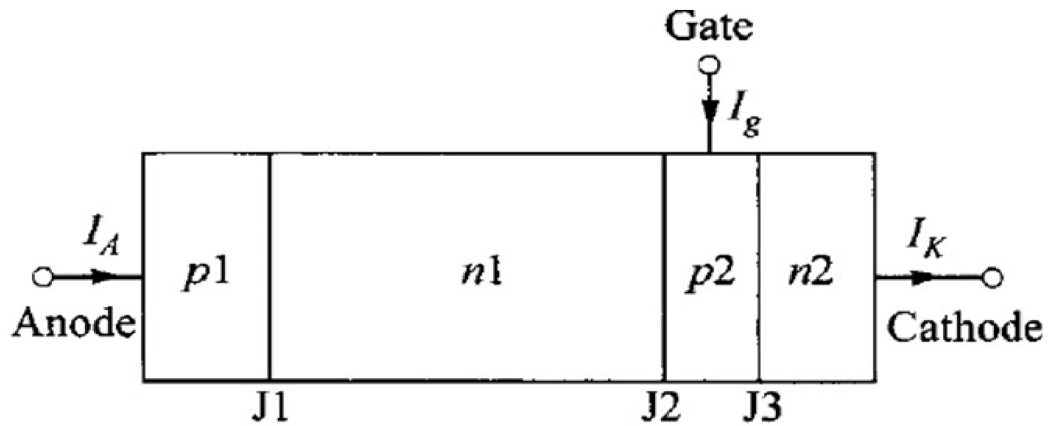



**Figure 2.1 Schematic diagram of basic thyristor [31]**

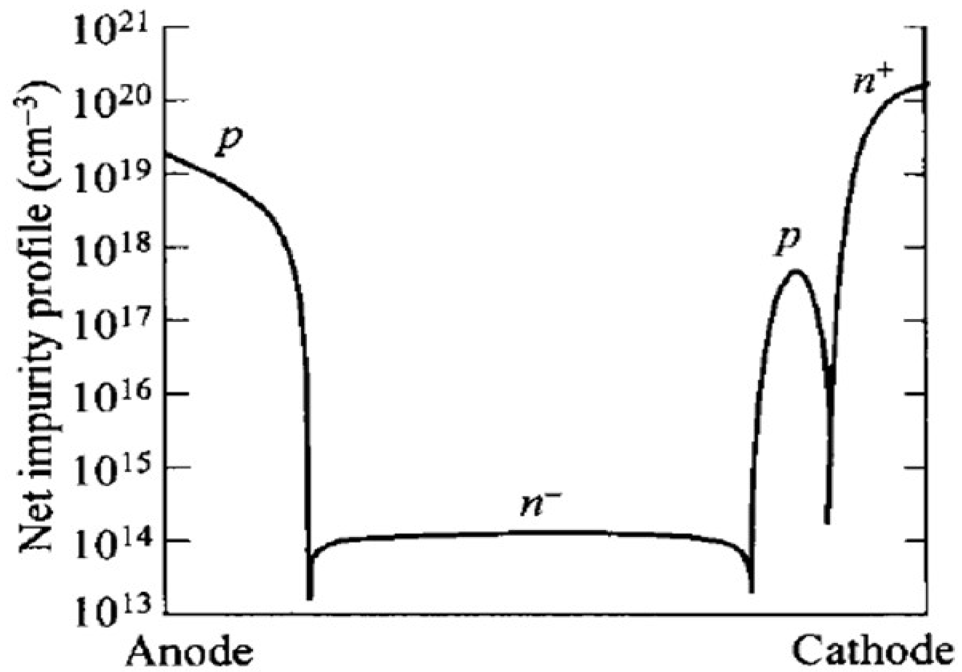



**Figure 2.2 Thyristor doping profiles [31]**

Thyristors are bi-stable with respect to their operation voltage, such that two stable operating currents exist for a range of anode voltages. Since nearly all electronic circuits are voltage controlled, thyristors are useful for switching applications. Thyristors are most easily described as current controlled devices, because the anode potential is a single-valued function of the current.

The current – voltage characteristics of the thyristor are shown in Figure 2.3. The voltage at the forward breakdown point ($dV/dI = 0$) is the forward break-down voltage ($V_{FB}$). The switching current ($I_s$) is the current corresponding to the forward break-down voltage. The smallest current for which the thyristor remains in low impedance, forward current conducting state is the holding current ($I_h$). The anode voltage increases rapidly for currents lower than the holding current. The minimum anode voltage of the thyristor in the forward current conducting state is the ON-state voltage ($V_{on}$). $V_{rb}$ is the reverse breakdown voltage and the region for which $0 < V < V_{rb}$ is the reverse blocking state. The forward current blocking state is the region for which $0 < I < I_s$. The forward current conducting state is the region for which $I > I_h$. The forward current blocking and the forward current conducting states are often referred to as the OFF and the ON states, respectively. The forward current blocking and the forward current conducting states are separated by a transition region ($I_s < I < I_h$) known as the negative differential resistance region (NDR) [30].

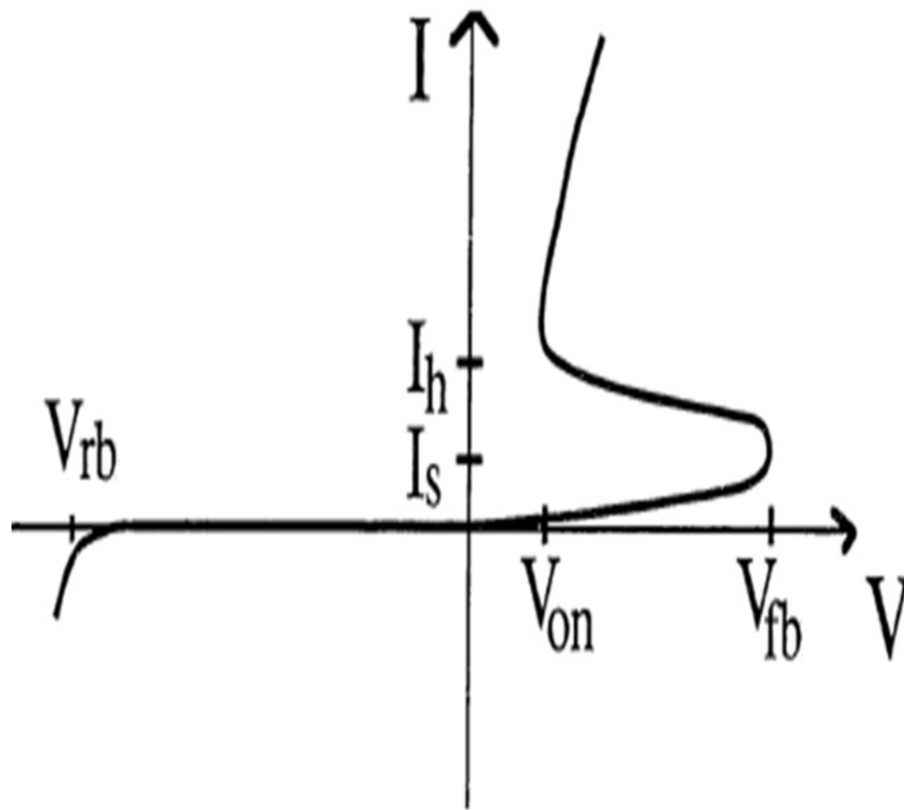



**Figure 2.3 Typical I-V characteristics of the thyristor [30]**

The operation of thyristors is intimately related to the BJT action in which both electrons and holes interact with each other in the transport processes. The two BJTs model developed by Ebers [32] is widely used to explain the characteristics of a basic thyristor.

### 2.1.1 Thyristor at Equilibrium State

When no voltage is applied to the thyristor electrodes, the thyristor will be in equilibrium. However, each of the three junctions (J1, J2, and J3) has a depletion region with a built-in potential that is determined by the impurity doping profile. The band diagram of the thyristor in the equilibrium state is shown in Figure 2.4.

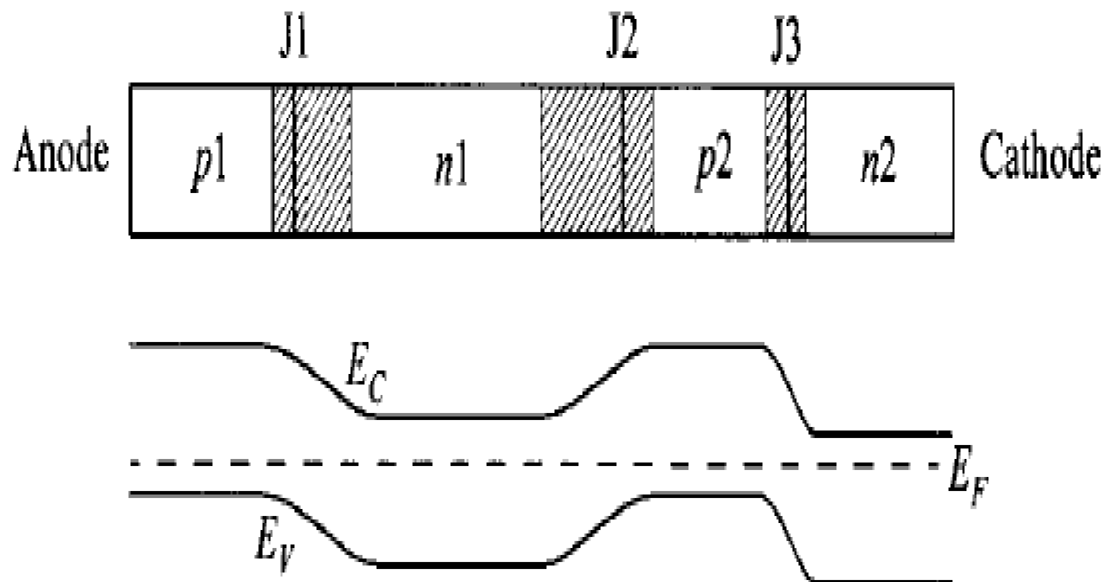



**Figure 2.4 Band diagram of thyristor in equilibrium state [31]**

### 2.1.2 Reverse Blocking State

Both $V_{FB}$ and $V_{BR}$ are controlled by two basic factors: the avalanche breakdown and the depletion-layer punch-through. When a negative voltage is applied to the anode ($V_{AK} < 0$) the thyristor operates in the reverse-blocking mode; junctions J1 and J3 will

be reverse biased while J2 is forward biased. Most of the applied reverse voltage will drop across J1 and the n-base region because of its low doping. Reverse breakdown mechanism depends on the width of the n-base ($W_{n1}$). It will be triggered by avalanche multiplication if the depletion-layer width at breakdown is less than $W_{n1}$. Otherwise, reverse breakdown will be initiated by punch-through if the whole of $W_{n1}$ is consumed first by the depletion layer, at which the junction J1 is effectively shorted to J2. For lower dopings, the break down voltage is limited by punch-through and for higher dopings by avalanche multiplication.

The reverse breakdown condition corresponds to that for the common-emitter configuration, which is $M = 1/\alpha_1$ where M is the avalanche multiplication factor and $\alpha_1$ is the p-n-p common-base current gain. The reverse breakdown voltage is given by

$$V_{br} = V_b \,(1 - \alpha_1)^{1/n}$$

where $V_b$ is the avalanche breakdown voltage of the J1 junction, and n is a constant (= 6 for Si $p^+$-n diodes). Since $(1 - \alpha_1)^{1/n}$ is less than unity, the reverse breakdown voltage of a thyristor will be less than $V_b$.

### 2.1.3 Forward Blocking State

Figure 2.5 shows the band diagram of the thyristor while operating in the forward blocking region; if the applied voltage to the anode is positive ($V_{AK} > 0$), the thyristor operates in the forward blocking region.

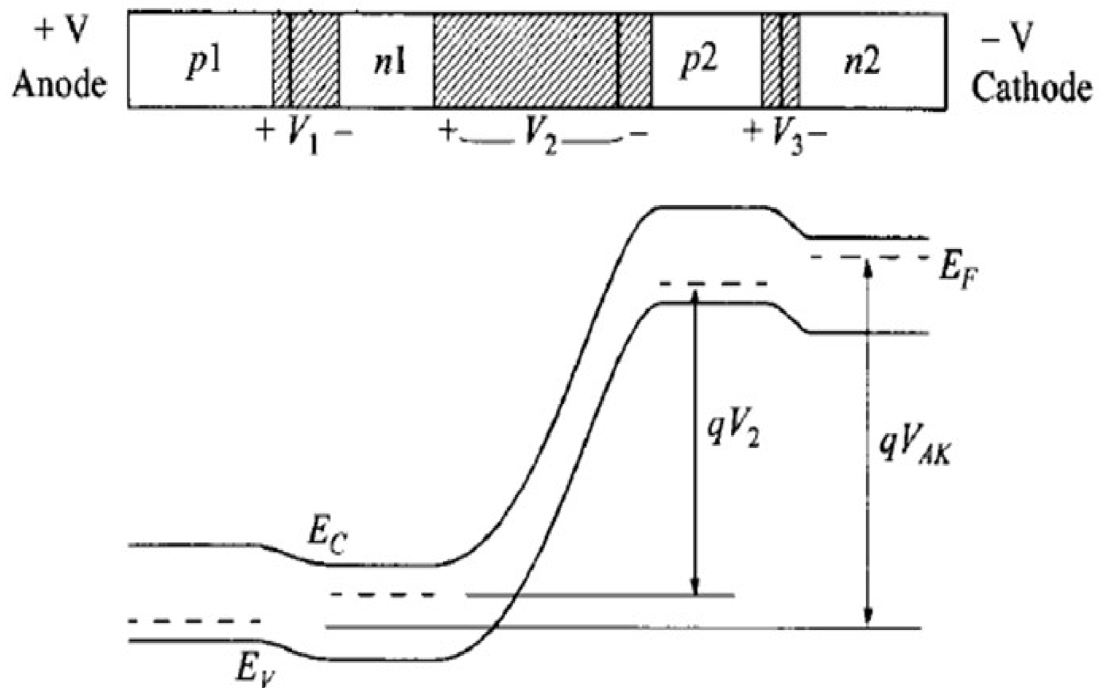



**Figure 2.5 Band diagram of thyristor in forward blocking state [31]**

Junctions J1 and J3 are forward biased but junction J2 will be reverse biased. Hence, most of the applied voltage will drop across J2. The forward blocking characteristics can be understood with the help of the two BJTs model. As shown in Figure 2.6, the thyristor can be considered as a p-n-p transistor and an n-p-n transistor connected such that collector of one BJT is attached to the base of the other, and vice versa. The center junction J2 acts as the collector of holes from J1 (p-n-p) and of electrons from J3 (n-p-n).

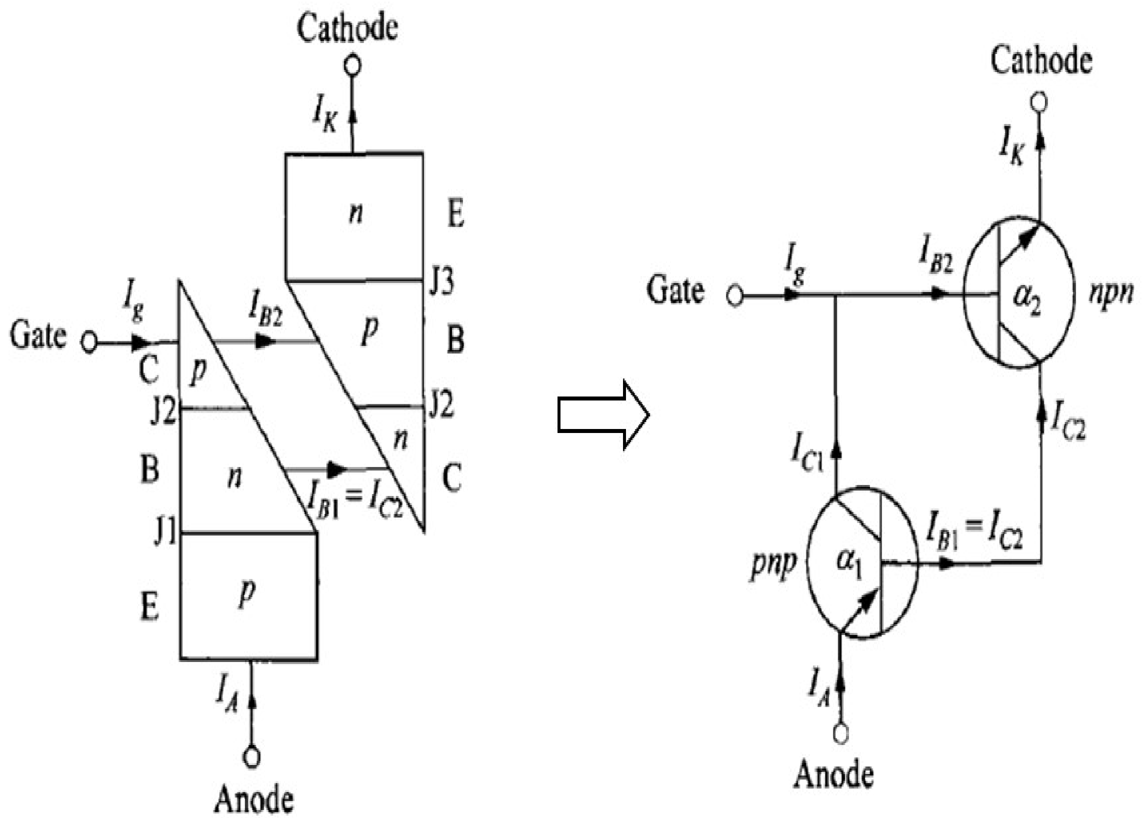



**Figure 2.6 Two BJTs model of the thyristor [31]**

The relationship between emitter, collector, and base currents ($I_E$, $I_C$ and $I_B$, respectively) and the dc common-base current gain (α) for a BJT transistor is given by:

$$I_C = \alpha I_E + I_{CO}$$

$$I_E = I_C + I_B$$

where $I_{CO}$ is the reverse bias current of the collector junction. From Figure 2.6: the collector current of the n-p-n transistor provides the base current for the p-n-p transistor. Also, the collector current of the p-n-p transistor along with gate current Ig supplies the base drive for the n-p-n transistor. Thus a regeneration situation results when the total loop gain exceeds unity.

The base current of the p-n-p BJT is:

$$I_{B1} = (1 - \alpha_1)I_A + I_{CO1}$$

This is driven by the collector current of the n-p-n transistor. The collector current of the n-p-n BJT is given by:

$$I_{C2} = \alpha_2 I_K + I_{CO2}$$

Since $I_{C2} = I_{B1}$ and $I_k = I_A$ and $I_g$:

$$I_A = \frac{\alpha_2 I_g + I_{CO1} + I_{CO2}}{1 - (\alpha_1 + \alpha_2)}$$

This equation provides the anode current of the thyristor while operating in the forward blocking region up to the forward breakdown voltage, it can be seen that this current is small (especially if $I_g = 0$).

As $V_{AK}$ increases, the total current passing through both p-n-p and n-p-n BJTs will also increase. The higher current will cause $\alpha_1$ and $\alpha_2$ to go up. Higher current gain will induce even higher current. Because of the regenerative nature of these processes, $\alpha_1$ and $\alpha_2$ keep increasing until $(\alpha_1 + \alpha_2)$ reaches unity (the switching condition). At this point the forward breakdown will occur and the device will switch to its on-state. This can be seen from the anode current equation above, for the condition of $(\alpha_1 + \alpha_2) = 1$, the anode current will be infinite, i.e., an unstable state where switching occurs. An increase of $\alpha_2$ can also be induced by injecting $I_g$, which is the base current for the n-p-n BJT, i.e., the switching voltage can be lowered by increasing $I_g$ [31].

If $V_{AK}$ continues to increase, not only will $\alpha_1$ and $\alpha_2$, increase towards the condition of ($\alpha_1 + \alpha_2$), the high field also initiates carrier multiplication. The interaction of gain and multiplication will decide $V_{FB}$ and the switching condition. $V_{FB}$ is given by:

$$V_{FB} = V_B(1 - \alpha_1 - \alpha_2)^{\frac{1}{n}}$$

Where $V_B$ is the avalanche breakdown voltage of the J2 junction and n is constant ≈ 1.

### 2.1.4 Forward Conduction State

In the on-state, J2 is changed from being reverse biased to forward biased, as shown in the band diagram in Figure 2.7, and the net voltage drop across the thyristor is given by ( V1 – V2 + V3) which is approximately equal to the voltage drop across one forward-biased p-n junction plus a saturated BJT.

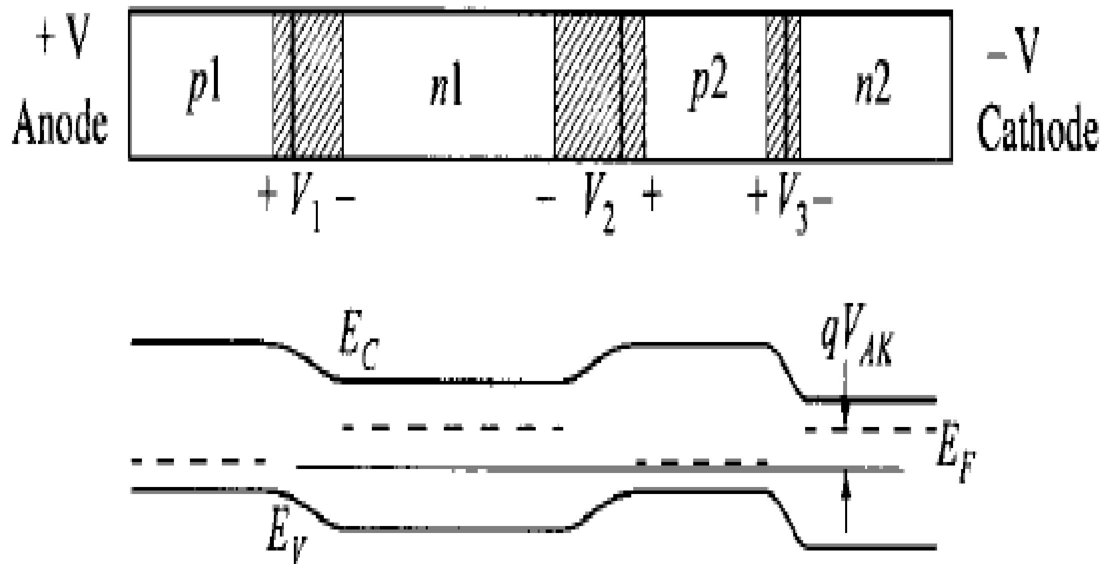



**Figure 2.7 Band diagram of thyristor in forward conduction state [31]**

All of the three junctions are forward biased; holes are injected from the p emitter region and electrons from the n emitter. These carriers flood the n- and the p- base regions which are relatively lightly doped. Therefore, the device behaves like a p-i-n diode.

### 2.1.5 Switching Times of Thyristor

The thyristor turns on if the condition ($\alpha_1 + \alpha_2$) = 1 is satisfied. This is accomplished by voltage triggering, where the forward voltage is raised slowly until the breakdown voltage is reached. The thyristor can also be turned on by applying gate current (gate-current triggering). When a gate current is applied, the anode current through a thyristor does not respond immediately. The anode current is approximately the geometric mean of the diffusion times of the n- base and p- base regions: $\tau_{on} = \sqrt{\tau_1 \tau_2}$ Where $\tau_1 = W_{n1}^2/2D_p$ and $\tau_2 = W_{p2}^2/2D_n$ , $W_{n1}$ and $W_{p2}$ are the widths of the n-base and p-base regions, respectively, and $D_n$ and $D_p$ are the electron and hole diffusion coefficients, respectively [31].

To turn the thyristor off, the excess minority carriers in the n-base and p-base regions must be swept out by an electric field or must decay by recombination. To shorten the turn-off time, a common circuit practice is to apply a reverse bias between the gate and the cathode in addition to reversing the polarity of $V_{AK}$. This method is called gate-assisted turn-off. The improvement comes about because the reverse-biased gate can divert most of the forward recovery current which would otherwise flow through the cathode during the reapplication of the forward anode voltage.

## 2.2 Thyristor Based RAM (T-RAM)

T-RAM is volatile memory based on the pnpn structure. T-RAM utilizes the bi-stable nature and the excellent on/off current ratio of the thyristor [33, 34] as the storage mechanism of the memory cell. The content of the cell is represented by the state of the thyristor, Data "1" is defined by the high current, ON state while Data "0" is stored when the thyristor is in the low current, OFF state. The slow turn off of the thyristor as well as the high voltage required to turn it on are avoided by augmenting the thyristor with a MOS-like gate over the p-base.

### 2.2.1 T-RAM Based SRAM

The first T-RAM based SRAM was introduced about fifteen years ago [35, 36]. It consisted of a vertical pnpn structure with, initially, a surrounding gate around the p-base and a pass MOSFET as shown in Figure 2.8. The purpose of having the surrounding gate was to improve the controllability over the p-base for low turn on voltage and fast switching.

The cell basic read and write operation and the load line diagram is illustrated in Figure 2.9, asserting word line1 (WL1) provides read and write access to the memory cell and WL2 is used only during the write operation. During writing "1" the bit line (BL) is kept at low voltage level and the rising edge of WL2 pulse forward biases the n-p-n BJT which starts the regenerative process and the thyristor turns on. For writing "0", the BL is biased to high voltage and the falling edge of WL2 pulse pulls out the minority carriers from the n- and the p- bases which turns off the device quickly [35]. The reading operation is done by monitoring the device current after enabling the access FET.

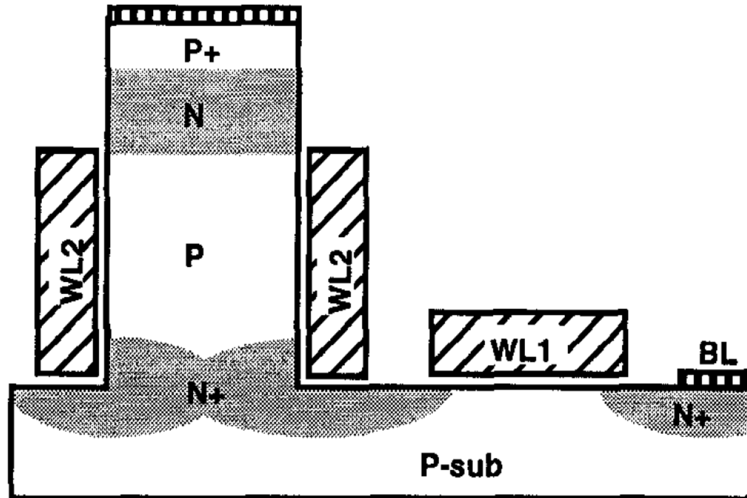



**Figure 2.8 T-RAM based SRAM structure. WL2 is a vertical surrounding gate [35]**

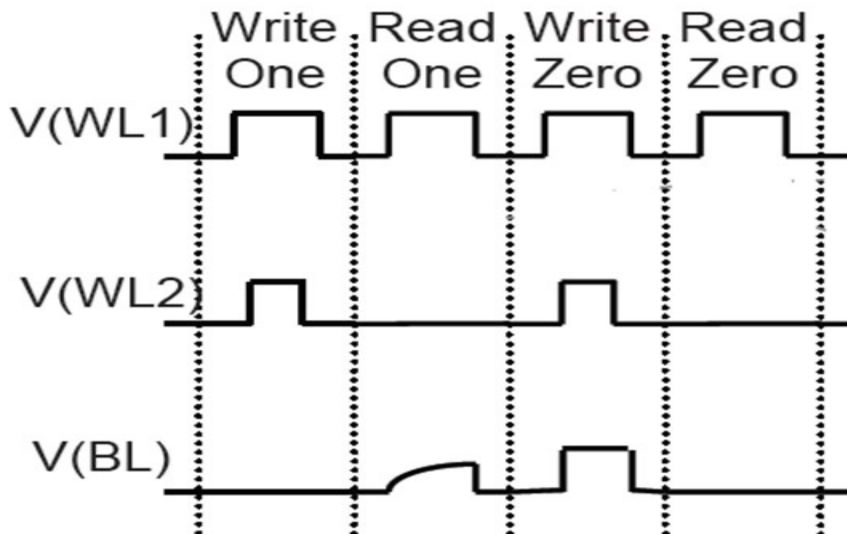



**Figure 2.9 Basic read/write diagram for T-RAM based SRAM [33]**

The DC load line of the SRAM cell for all memory operations are shown in Figure 2.10. The pass transistor during standby mode is partially on (Figure 2.10 (a)); such that it supports the minimum current required to keep the thyristor operating in the forward conduction region (the holding current). This condition should be satisfied in order to keep data “1” stored in the cell, otherwise, the thyristor will turn off and the data will be lost. The thyristor acts a regular pin diode while writing “1” (Figure 2.10 (c)) whereas it is reversed biased during writing “0” (Figure 2.10 (d)). As mentioned earlier, the reading operation is performed by turning the pass transistor on. If data “1” is stored, high current will flow because the thyristor is in the ON state. On the hand, if data “0” is stored; there will be a very small current as the thyristor is in the forward blocking state. The operating points corresponds to data reading are marked in Figure 2.10 (b).

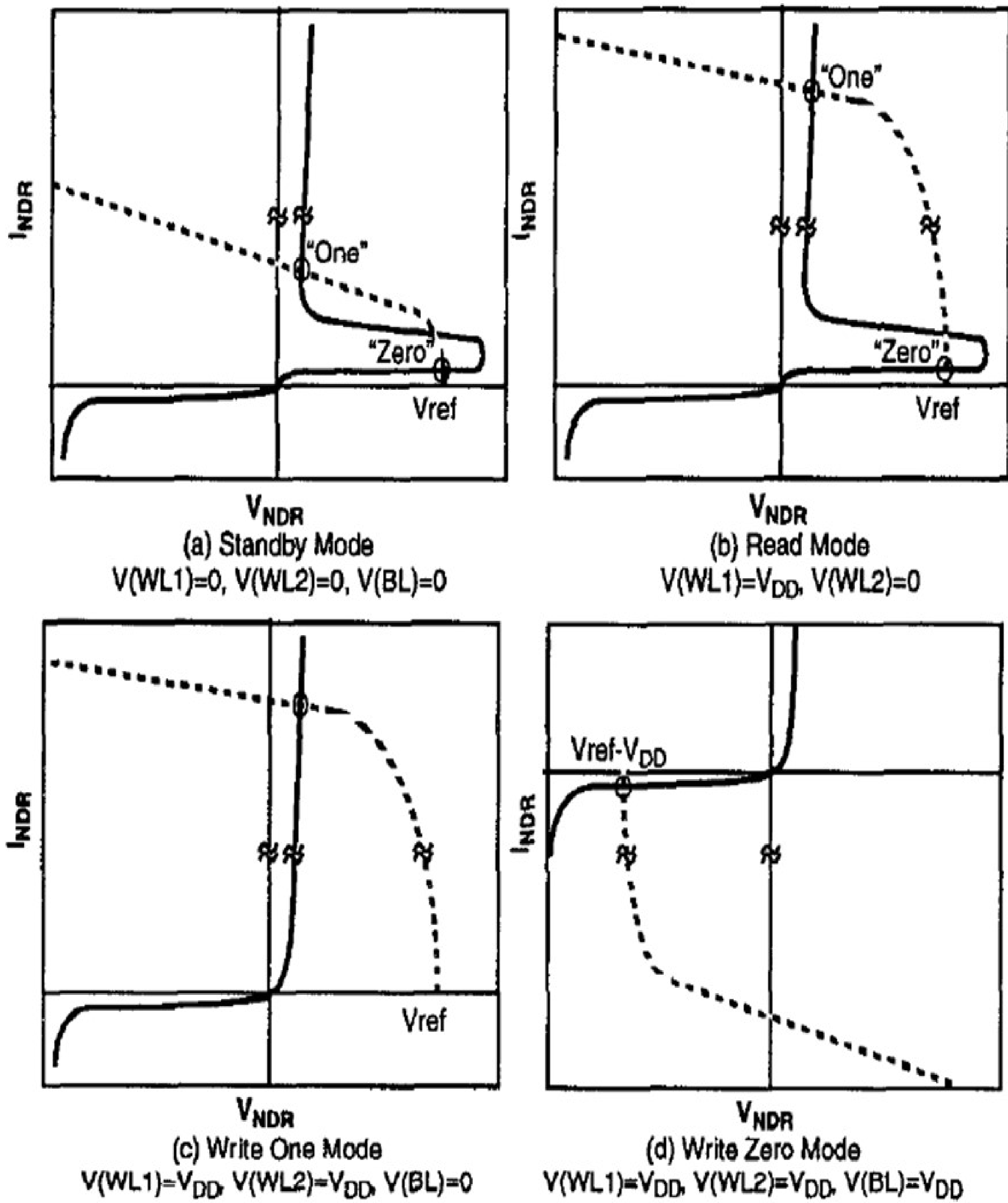



**Figure 2.10 DC load lines for SRAM during memory operations [35]**

### 2.2.2 Thin Capacitively Coupled Thyristor (TCCT)

The SOI TCCT structure was introduced to replace the vertical pnpn device with the surrounding gate as the active storage element. Unlike the previous implementation, the gate does not surround the p-base of the TCCT. However, the silicon of the SOI is sufficiently thin to allow for fast operation with capacitive coupling from a single sided gate [33].

Figure 2.11 shows the TCCT SRAM cell structure and the equivalent circuit model. The TCCT is modeled by a pair of interconnected p-n-p and n-p-n BJTs in a positive feedback loop providing bi-stable characteristics and a MOS-like gate providing capacitive coupling to the base of the n-p-n device.

**Figure 2.11 TCCT SRAM along with its equivalent circuit model [33]**

### 2.2.3 T-RAM Based DRAM

Unlike the conventional 1T-1C DRAM cell, the TCCT DRAM cell is capacitor-less and the MOSFET is replaced by the TCCT. Non-destructive read, high speed writing, solid retention characteristics, and the high “1” / ”0” currents ratio are among the advantages that make the TCCT-DRAM a promising alternative to the current 1T-1C DRAM. The equivalent of the TCCT memory cell and schematic of memory structure built on conventional SOI is shown in Figure 2.12.

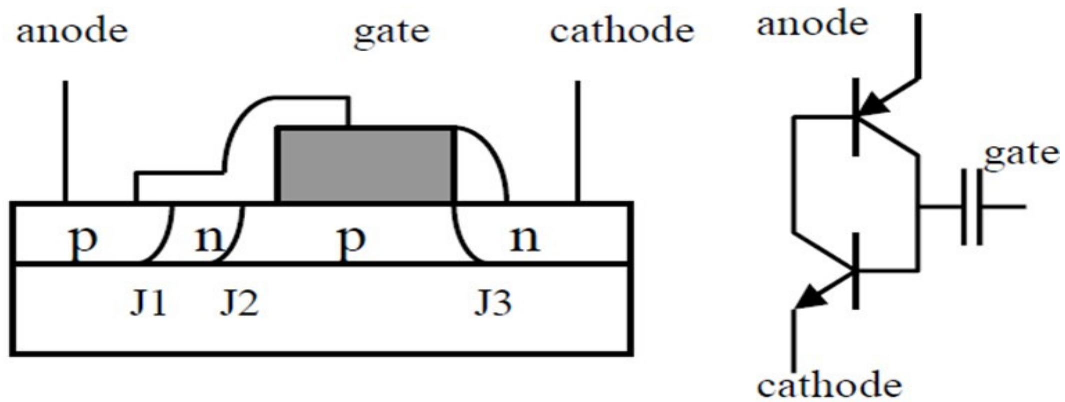



**Figure 2.12 TCCT DRAM structure schematic and circuit model [34]**

The basic read/write operations are illustrated in Figure 2.13. In standby mode, both anode and cathode lines are at Vdd and the stored cell data is maintained by the charge state of the p-base of the TCCT. The cathode line functions as the WL in TCCT DRAM and activates the TCCT cells along the gate line. For write “1”, gate line is pulsed while cathode line is held at ground level, triggering the TCCT device to latch. The bias scheme for write “0” operation is the same as write “1” except that the anode line voltage

is kept low so that pulsing of the gate line switches the TCCT into its blocking state. For read operation, the cathode line is held low and the change in the current of the anode line is read into a sense amplifier [34].

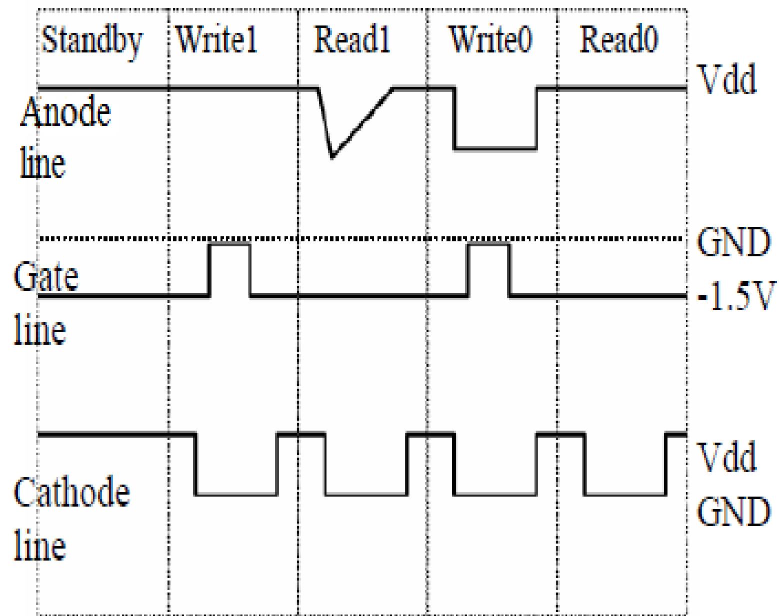



**Figure 2.13 Basic write/read diagram for TCCT DRAM [34]**

A high speed and high density DRAM cell based on TRAM was implemented in 32 nm SOI logic process [37]. A schematic of this cell is shown in Figure 2.14. The BL is connected to the anode while WL1 and WL2 are connected to the cathode and the gate respectively.

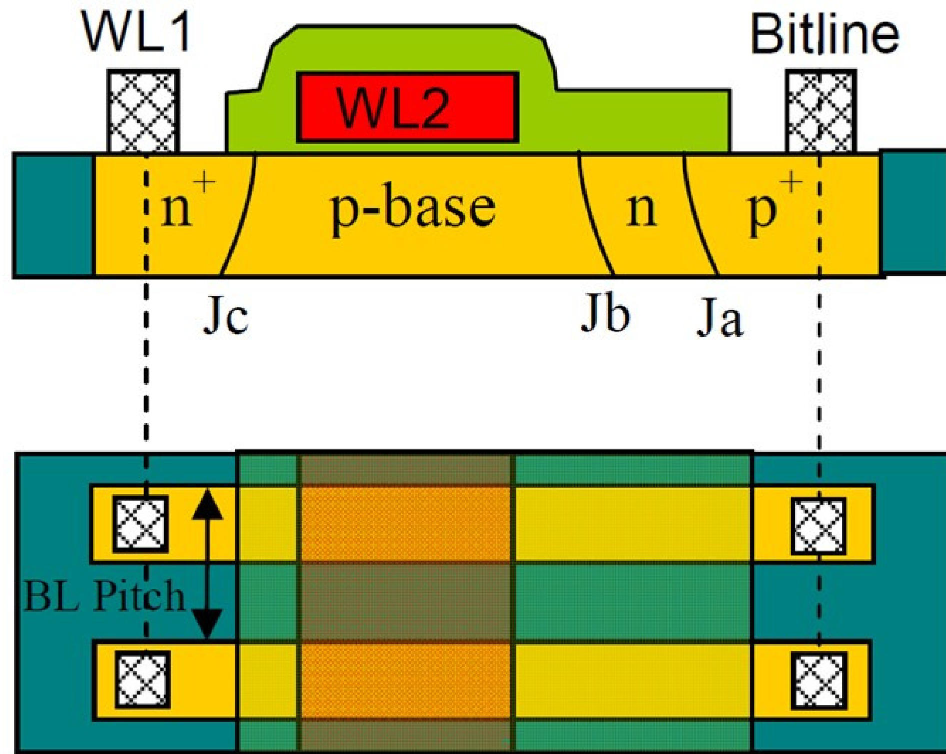



**Figure 2.14 Schematic cross section and planar view of the new TRAM. BL is connected to the anode, WL1 and WL2 are connected to the cathode and the gate, respectively [37]**

The concept behind the writing and reading operations for the cell is still the same but it is performed using a different waveforms scheme. The timing diagram of the memory operations is shown in Figure 2.15. At stand by, the BL and WL1 are kept 0.7 V while WL2 is kept low at -0.8 V. Writing “1” is done by pulsing WL2 and BL up to 1.5 V while WL1 is pulsed down to 0 V. Writing “0” is done by pulsing BL to 0.4 V, WL1 to 0 V and WL2 to 1.5 V. Read operation is performed dynamically with the help of the gate (gate assisted turn on mechanism): the BL is pre-charged to 1.5 V, and WL1 is pulsed down to 0 V then WL2 is pulsed up to 0.1 V, if cell content is “1”, then WL2

pulse will be enough to turn the thyristor on, otherwise it will stay off, i.e., the cell content is “0”.

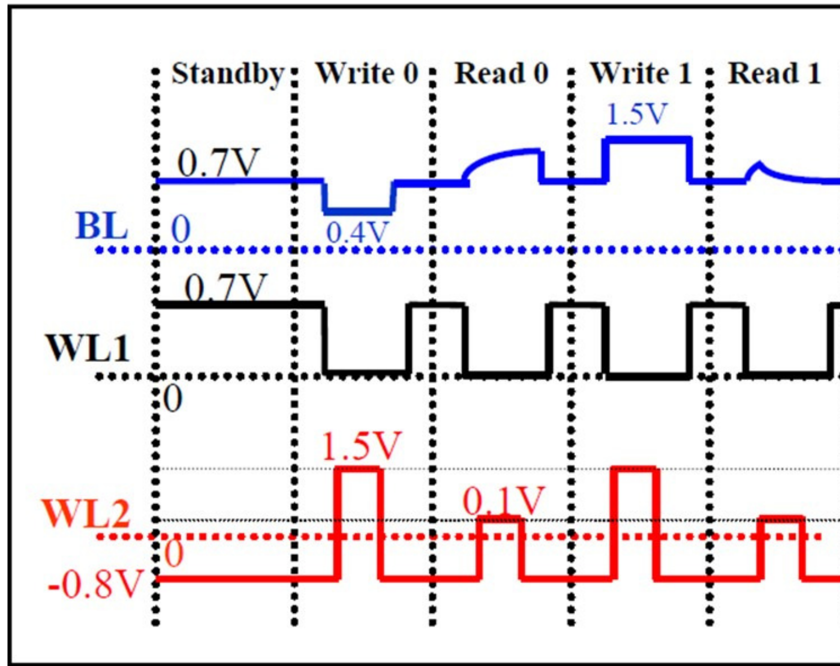


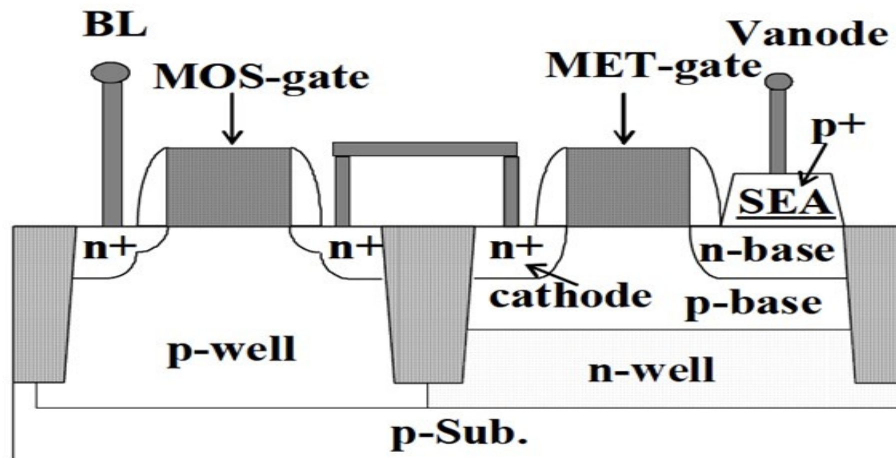

**Figure 2.15 Memory operations diagram for the new TRAM cell, the read operation is performed “dynamically”, by pulsing the gate (WL2) [37]**

This cell is characterized by high speed write and read operations, good retention times and excellent array efficiency. However, the writing and the reading operations are more complicated.

### 2.2.4 T-RAM on Bulk Silicon

Multiple implementations of TRAM based SRAMs on bulk silicon, instead of SOI, have been reported [38-40]. These memory cells where fabricated with selective epitaxy layer anode and also with triple selective layers for the anode, the n-base and cathode as shown in Figure 2.16.

The reported cells were fabricated using 45 nm and 35 nm process technologies which proves superior scaling characteristics. Furthermore, they showed excellent performance such as low voltage / high speed operation, low standby current, and high thermal stability. Compared to the SOI, the cells built on bulk have faster turn off speed at lower voltages. This is achieved by controlling the n-well bias to shunt the excess carriers to the substrate. As a result, the turn-off times are faster than the life-time of the minority carrier in the p-base region. However, it is very difficult to control the doping profiles of the pnpn structures in Si wafers both vertically and laterally. This control is necessary to suppress punch-through between the p-anode and p-base, as well as between the n-base and n-well.



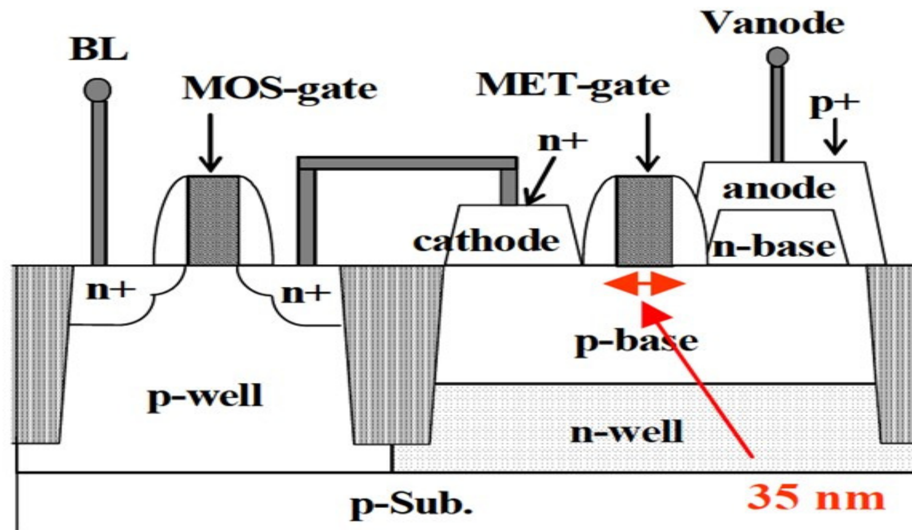




**Figure 2.16 TRAM based SRAM on bulk silicon: (a) with selective epitaxy anode (SEA) [38], (b) with triple selective epitaxy (anode, n-base, and cathode) [40]**

### 2.2.5 Optimization Techniques for T-RAM

The carriers' life times and the base gains of the p-n-p and the n-p-n BJTs constituting the thyristor in the T-RAM structures play a vital role in the memory functionality. Therefore, optimizing these parameters can significantly improve the cell performance and stability. Back-gate control [41] and carrier life adjustment by leakage implant [42] are two effective methods that have been applied to control these parameters in the SOI TCCT structures.

Back-gate control is based on applying voltage to the substrate, Figure 2.17. This voltage induces an electric field in the buried oxide (BOX), which modulates the hole concentration in the p-base.

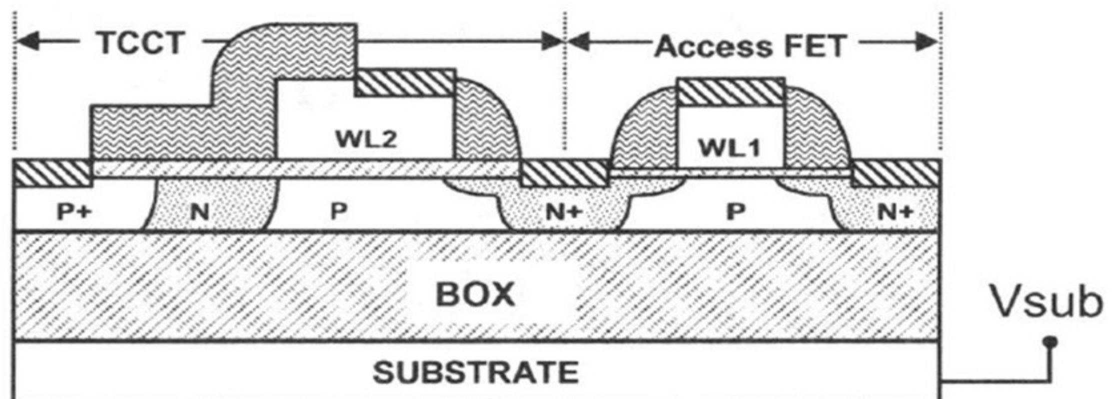



**Figure 2.17 SOI TRAM with substrate bias for back gate control [41]**

However, applying voltage to the substrate may lead parasitic slow transient effects because of substrate depletion and inversion due to its low doping. To suppress parasitic slow transients, substrate inversion should be avoided. This can be done by high

doping of the substrate near its interface with the BOX. High doping can be achieved either by using SOI wafers with heavily doped substrate, or by ion implantation of impurities into substrate through the top layers.

Carrier lifetime adjustment is accomplished through leakage implant at the anode / n-base (JI) junction, Figure 2.18, to improve cell speed and thermal stability.

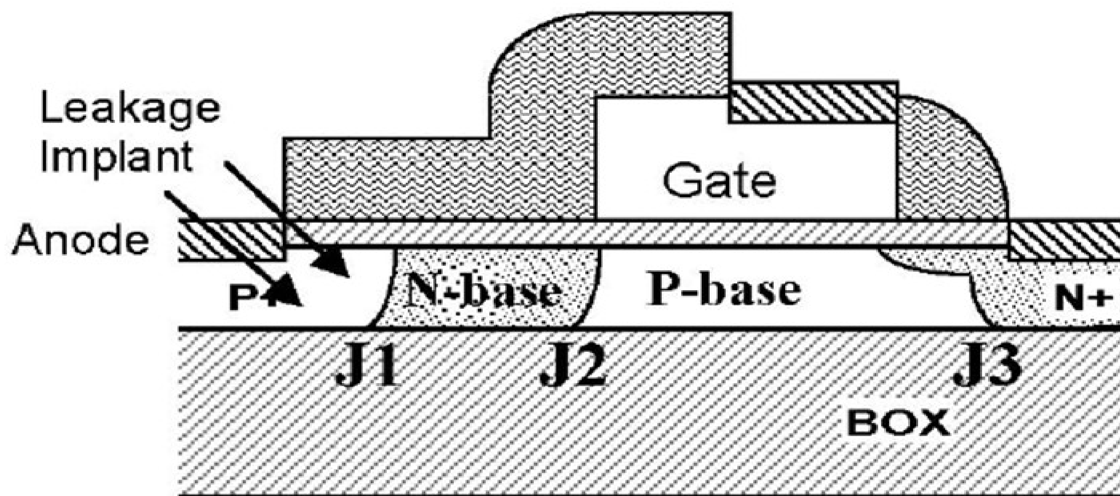



**Figure 2.18 Leakage implant on SOI TCCT [42]**

In TRAM cell, writing “0” is performed by the gate assisted turning off process of the thyristor. The falling edge of the gate pulse removes the extra minority carries from the n- and p- bases. The excess carriers in the p-base are pushed to the n-emitter (the cathode) and the n-base without carrier recombination; however, carriers in the n-base need to be removed by recombination. Therefore, the carrier lifetime in the J1 becomes a limiting factor for the switching speed. When the carrier life time is reduced by leakage

implant, carriers in the n-base are more quickly recombined, resulting in improved turn-off speed.

### 2.2.6 Storage Mechanism in T-RAM

Detailed researches and studies have been done to understand the working principles of the TRAM cells. These studies concluded that the hole concentration in the p-base is the physical element that determines the storage mechanism in the TRAM cell. Data “1” is defined by the accumulation of holes in the p-base; while data “0” corresponds to a depleted p-base [43-48]. Furthermore, the static and the dynamic characteristics of the memory cells were explained with assumption that the cell content is determined by the presence or absence of holes in the p-base.

The $V_{FB}$ voltage of the thyristor decreases as the gate voltage bias increases (Figure 2.19). This is explained by the enhancement of electron flow from the cathode to the n-base due the weak inversion resulted from increasing the gate bias. In other words, increasing the gate voltage lowers the energy barrier for the electrons to flow from the cathode to the n-base [43-48].

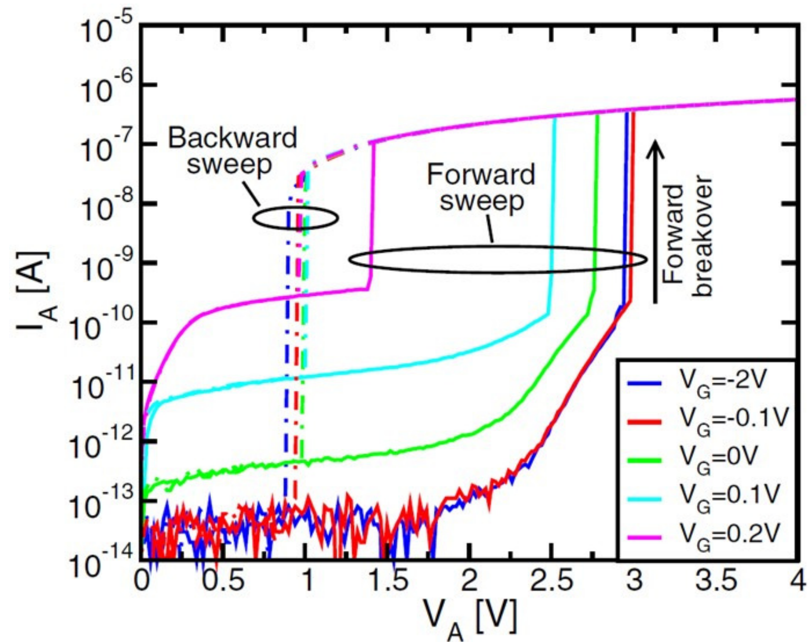



**Figure 2.19 $V_{FB}$ as a function of the gate voltage (Vg) [44]**

This is the concept used to justify the interpretation of the store mechanism as the accumulation ("1") or depletion ("0") of holes in the p-base. As seen Figure 2.20, when the p-base region is depleted of holes (Figure 2.20 (a)), the energy barrier limiting electron injection from the cathode to the n-base is raised and the T-RAM cell turns on at higher $V_A$. On the other hand, if a high hole concentration is present in the p-base, the energy barrier is reduced (Figure 2.20 (b)) and more electrons can flow from the cathode to the n-base. As result, the regenerative process will trigger and the thyristor will turn on at lower $V_A$ [43-48].

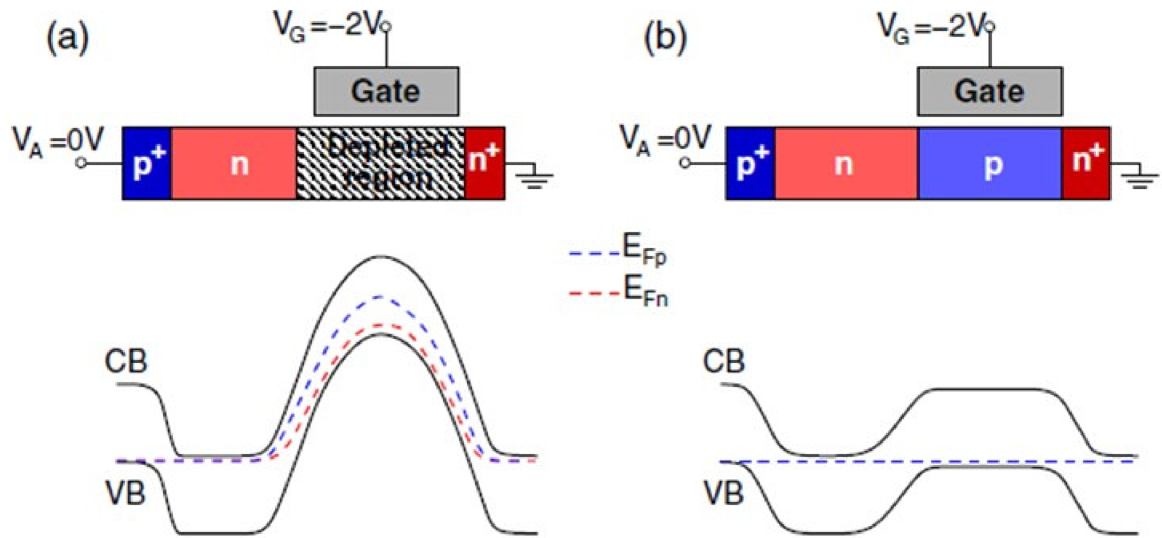



**Figure 2.20 Energy band diagrams of the T-RAM: (a) when the p-base is depleted from holes, (b) when holes are accumulated in the p-base [44]**

The assumption that the data storage in the TRAM cells is determined by the accumulation (“1”) or depletion (“0”) of holes in the *p*-base (under the gate) is seemingly correct and consisted with the operation of the device. However, a closer look at the memory operations proved that this assumption is incorrect. An alternative description to the physical memory mechanism will be presented in chapter 6 of this dissertation.

## 2.3 Summary

In this chapter, two closely related topics were reviewed, the pnpn thyristor and the T-RAM cells.

In the first half of the chapter, the thyristor structure and its bi-stable nature were presented. Also, the device physics behind its modes of operation were explained with

the help of the relevant band diagrams. Based on the two BJTs model, the forward break-down mechanism as well as the switching times and conditions were discussed. This review revealed the high dependence of the thyristor functionality on the n- and p- base gains, and eventually the carrier's life time. Modulating these significant parameters is the key to control the thyristor operation.

The second half of the chapter introduced the T-RAM cells. These cells exploit the thyristor as a storage element based on its bi-stable nature. SRAM and DRAM cells on SOI were presented and their concept of operation was explained. TRAM cells on Bulk silicon were also reviewed and compared to the SOI implementation. Finally, some of the methods used to optimize the memory operation were discussed.

The TRAM cells have excellent performance and superior scalability. However, the need for precise doping techniques and the fabrication process complexity pose a serious challenge for this type of memories as the process scales down.

# CHAPTER 3 THE FIELD EFFECT DIODE (FED)

The FED structure, shown in Figure 3.1 resembles a p-i-n diode to which two closely spaced independent gates were added between the anode and the cathode. Biasing these two gates creates electric fields that induce carriers inside the intrinsic region. Based on the applied bias (the type of carriers induced under each gate), the diode can be operated as a regular pin diode or as a Silicon-Controlled-Rectifier (SRC). The semiconductor layer must be either intrinsic or thin enough to reduce the effect of the shunt resistor under the channel from the anode to the cathode [49].

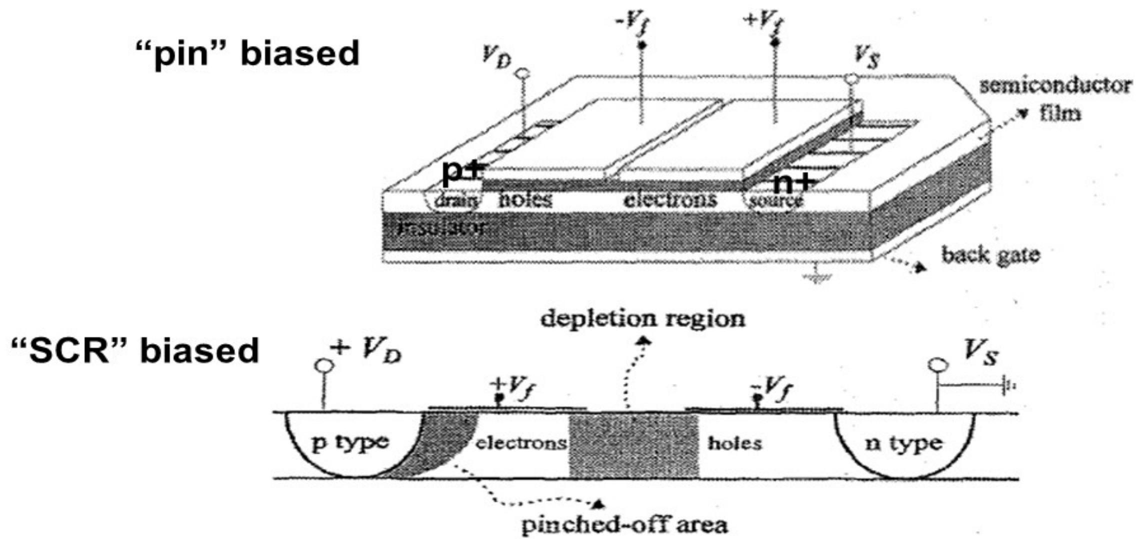



Figure 3.1 FED Diode [49]

## 3.1 SOI FED Based Thyristor

A cross-section of the SOI-FED is shown in Figure 3.2. By suitably biasing gate1, G1 (next to anode A) positively at $V_{G1}$ and gate2, G2 (next to cathode K) negatively at $V_{G2}$, electrons accumulate in the silicon film beneath G1 and holes beneath G2, and the FED acts like a pnpn thyristor. The device has three p-n junctions: an induced junction (J1) between the anode and the induced n-region beneath G1, an induced junction (J2) between the induce n-region beneath G1 and the induced p-region beneath G2, and a built in junction (J3) between the induced p-region beneath G2 and the cathode. The absence of latch-up, the reduced of parasitic capacitances, and the ease of making shallow junctions are merely three obvious examples of the advantages presented by SOI technology over bulk. There are many other properties allowing SOI devices and circuits to exhibit performances superior to those of their bulk counterparts; these properties include: radiation hardness, high-temperature operation, improved trans-conductance and sharper subthreshold slope [22].

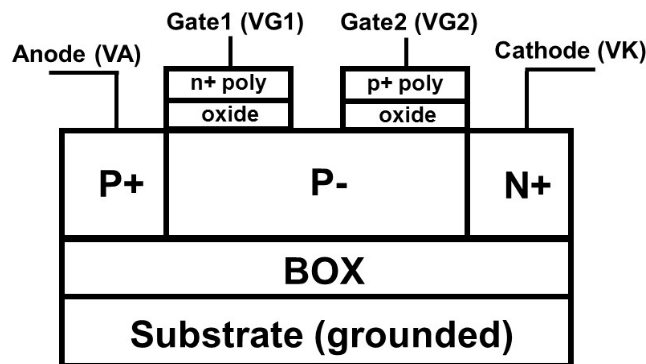



**Figure 3.2 SOI-FED based thyristor**

Figure 3.3 shows the band diagram of device in the OFF state. When a small positive bias $V_A$ is applied to the anode with cathode grounded ($V_K = 0$ V), almost all of that voltage will drop across the reverse biased junction (J2) and the anode current through the device is very small. However as $V_A$ is ramped-up, the device eventually breaks down at $V_{FB}$, goes through the NDR region, and finally snaps-back to the ON-state whereby large anode current $I_A$ flows. Simulated $I_A$-$V_A$ characteristics of an FED based thyristor are shown in Figure 3.4; they corresponds to an FED with slightly p-type doped ($10^{16}$ $cm^{-3}$), 20 nm thick SOI film, gate lengths $L_{G1} = L_{G2} = 400$ nm, and ungated gap length between the gates $L_{gap} = 40$ nm.

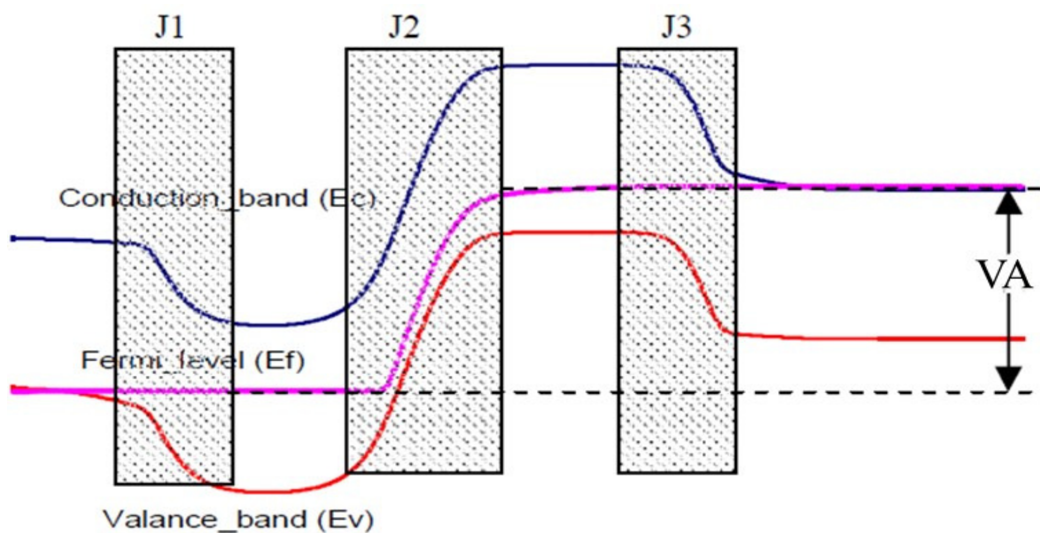



**Figure 3.3 Band diagram of the thyristor at off state [50]**

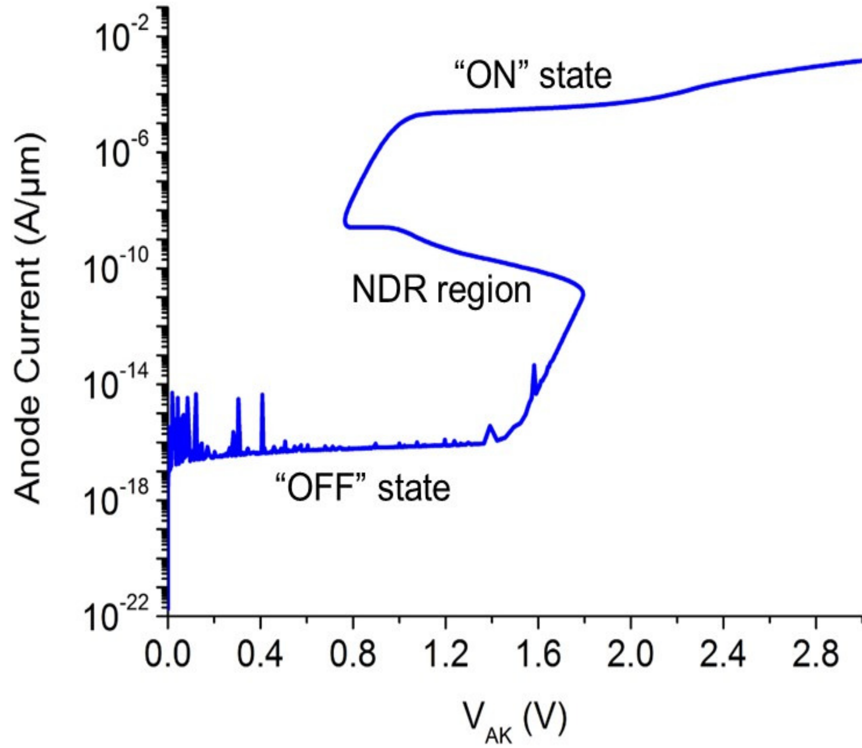



**Figure 3.4 I-V Characteristics of SOI FED based thyristor. VG1 = 1.2V, VG2 = -1.2V**

## 3.2 Forward Break-Down Properties of the FED Thyristor

The forward breakdown voltage ($V_{FB}$) can be expressed as [31]:

$$V_{FB} = V_B * (1 - \alpha_1 - \alpha_2)$$

where $V_B$ is the breakdown voltage of the p-n junction (J2) between the two gates and $\alpha_1$ and $\alpha_2$ are the DC common base gains of the p-n-p and n-p-n BJTs intrinsic to the FED structure. Because $\alpha_1$ and $\alpha_2$ are strongly dependent on the carrier lifetime, $V_{FB}$ also depends strongly on lifetime and is actually expected to increase by reducing the lifetime.

Figure 3.5 shows the I-V characteristics of the FED at multiple values for $V_{G1}$; the forward breakdown voltage $V_{FB}$ increases as $V_{G1}$ increases. This is because of the

reduction in carrier lifetime due to the rise in carrier recombination in the induced n-region beneath G1 as $V_{G1}$ increases.

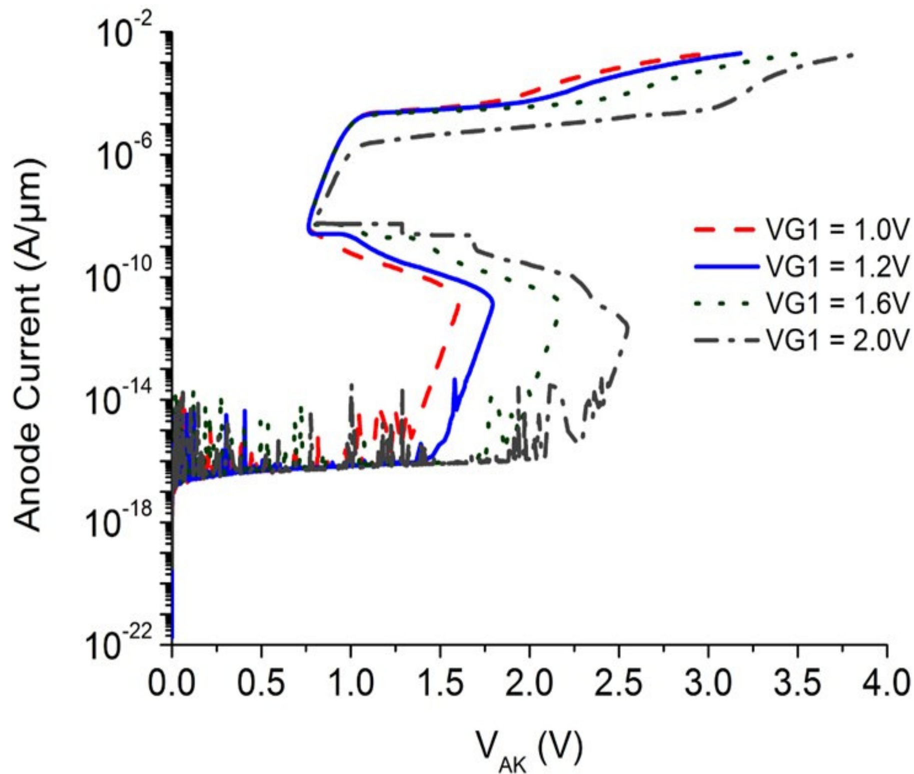



**Figure 3.5 Simulated anode current–voltage characteristics (IA versus VA) at VG1 = 1.0, 1.2, 1.6, and 2.0 V with gate VG2 = -1.2 V and cathode K grounded. (20-nm-thick SOI, slightly p-type; LG1 = LG2 = 400 nm, and Lgap = 40 nm)**

The forward breakdown voltage also increases with decreasing the SOI layer thickness as shown Figure 3.6. This can be explained by the increasing control of the gates over the channels with decreasing SOI thickness. As suggested by Figure 3.7, the I-V of the FED characteristics depend only weakly on the length of the gap between the

gates [51, 52] hence this gap can be kept as small as lithographically possible and improve scaling.

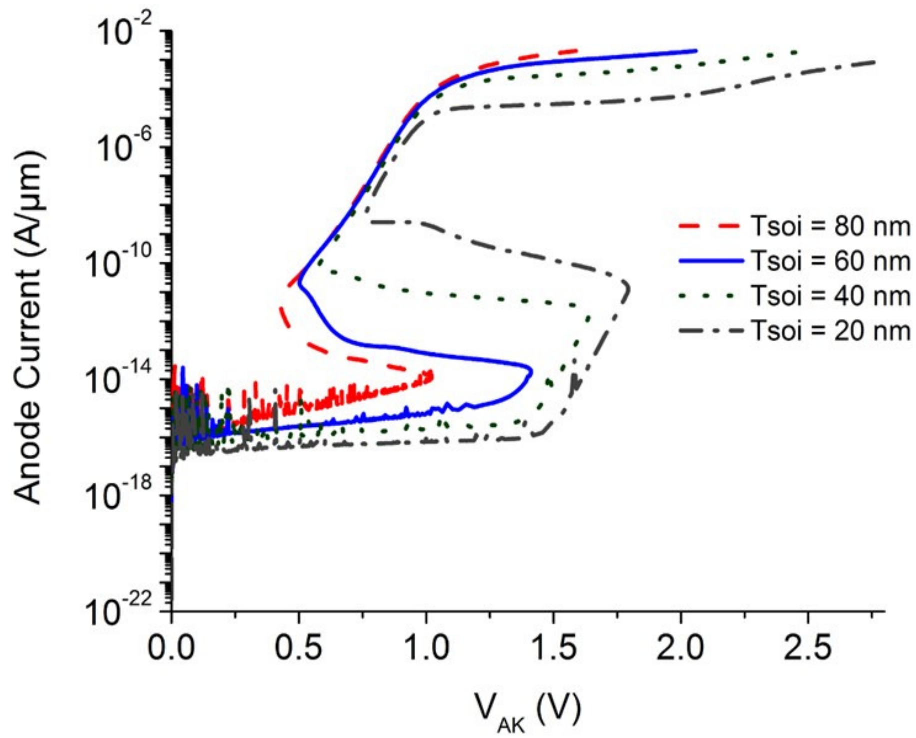



**Figure 3.6 VFB as a function of SOI layer thickness (Tsoi). VG1 = 1.2V, VG2 = -1.2V, slightly p-type SOI; LG1 = LG2 = 400 nm, and Lgap = 40 nm. VFB increase as Tsoi decreases.**

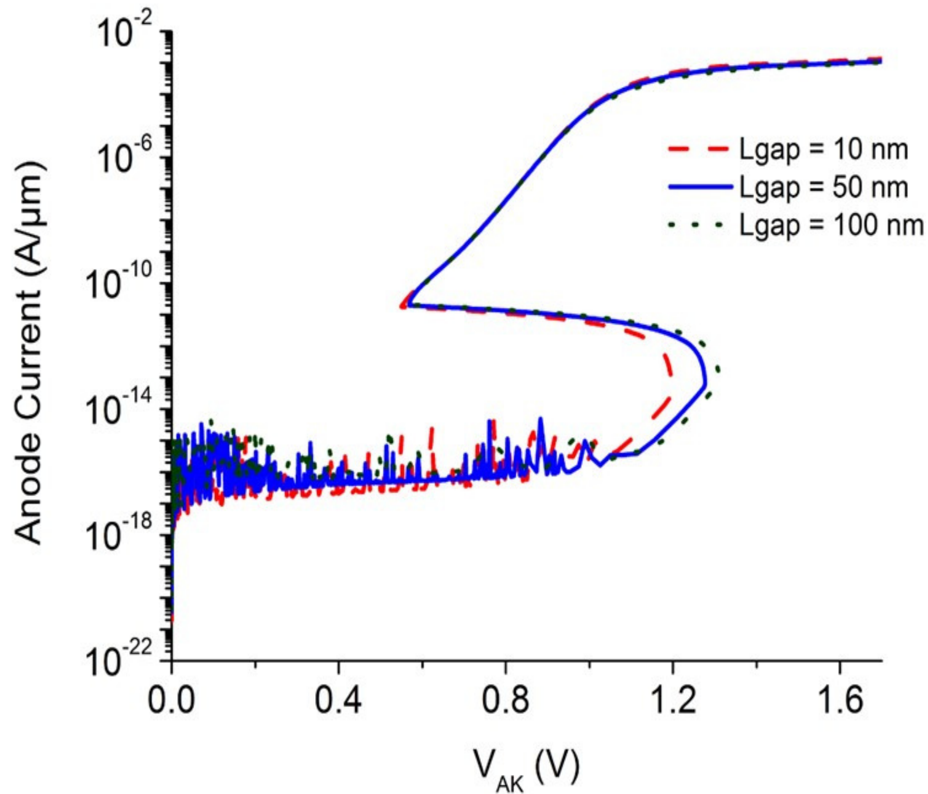



**Figure 3.7 VFB as a function of the gap length (Lgap) between the two gates. VG1 = 1.0V, VG2 = -1.0V, slightly p-type SOI; LG1 = LG2 = 100 nm. VFB depends only weakly on Lgap**

## 3.3 Summary and Discussion

In this chapter, the FED structure was presented. It was also shown that, depending on the bias applied to the gates, the FED can operate as regular pin diode or as a thyristor. The characteristics of the FED based thyristor were reviewed. Furthermore, the effect of the device parameters on the thyristor behavior have been explored.

The FED properties have been exploited for electrostatic discharge (ESD) to design Electrostatic-Discharge-Protection (ESD) of SOI CMOS chips [26, 50, 53].

On the other hand, it is possible to utilize the FED operation as a thyristor for memory applications. This is based on the TRAM concept but with the distinctive difference that the thyristor action in the FED is induced by the gates bias, whereas it is built in the TRAM.

# CHAPTER 4 SOI FED-SRAM: STRUCTURE AND OPERATION

## 4.1 Introduction

The need for progress in all types of memory technologies is well recognized and they are vigorously researched around the world. For example, in each of the three most recent IEEE IEDM meetings there were multiple sessions dedicated to new memory devices and approaches.

A quasi-static memory cell based on the FED is presented and its operation explained with the help of numerical device simulations. Although this new cell resembles the TCCT quasi-SRAM cell in concept and operation, it is nevertheless characterized by significant advantages. These advantages derive from the fact that the "thyristor- like" mode of operation of the FED is gate-induced, whereas the TCCT is an actual "built-in" thyristor. The operation of the cell is explained with the help of suitable timing diagrams, and the mechanisms of storing "1" and "0" are analyzed in detail.

High read "0"/"1" current margin, fast write/read time and densely packed cell are among the cell advantages obtained.

The basic FED-SRAM structure and operation is presented first; this is followed by improving the "Hold" state with the addition of a "Restore" pulse, and an alternate write "1" scheme. A memory array arrangement for disturbance control is then explained, and finally the conclusions are presented.

## 4.2 Cell Structure and Basic Operation

The FED-SRAM cell consists of two elements, an FED and an access MOSFET, integrated as shown in Figure 4.1, n- and p- regions are induced below gates G1 and G2, respectively, by biasing positively the former and negatively the latter. These induced n- and p- regions and the p- anode form two (induced) p-n junctions, which together with the (built-in) p-body/n-cathode junction form the (induced) FED-PNPN thyristor.

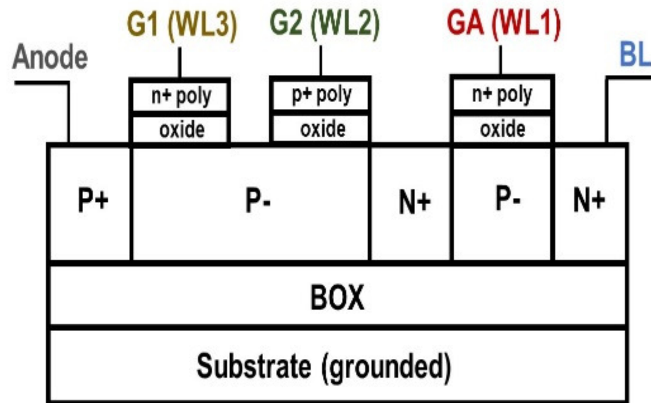



**Figure 4.1 The FED-SRAM structure consists of an FED and an (access) MOSFET, integrated as shown.**

The FED-SRAM is rather similar to the TCCT-SRAM [33], and they both share several features such as high density and high ON/OFF current margin. However, the FED-SRAM is easier to fabricate since there is no need for additional implantation for the formation of the p and n bases, which is necessary for the fabrication of the TCCT-SRAM. Moreover, a certain level of flexibility and control is afforded over the induced n- and p- FED regions under gates G1 and G2, respectively, by suitably adjusting the gate voltages, which of course is not available in the TCCT-SRAM.

Figure 4.2 shows the dc I-V characteristics (FED) and the load line (MOSFET) of the FED-SRAM. For proof of concept purposes, a somewhat relaxed geometry is used as follows: slightly p type ($10^{16}$ $cm^{-3}$), 20 nm thick SOI, FED and MOSFET gate lengths of 400 nm each, un-gated gap (between the FED gates) length of 40 nm, and gate oxide of thickness 2.5 nm. The two stable Read states "0" (R0) and "1" (R1) of the cell are clearly marked in Figure 4.2: low current, FED OFF-state and high current, FED ON-state. The memory operation relies on the possibility to reach either one of these two stable states by means of fast gate switching [33, 46].

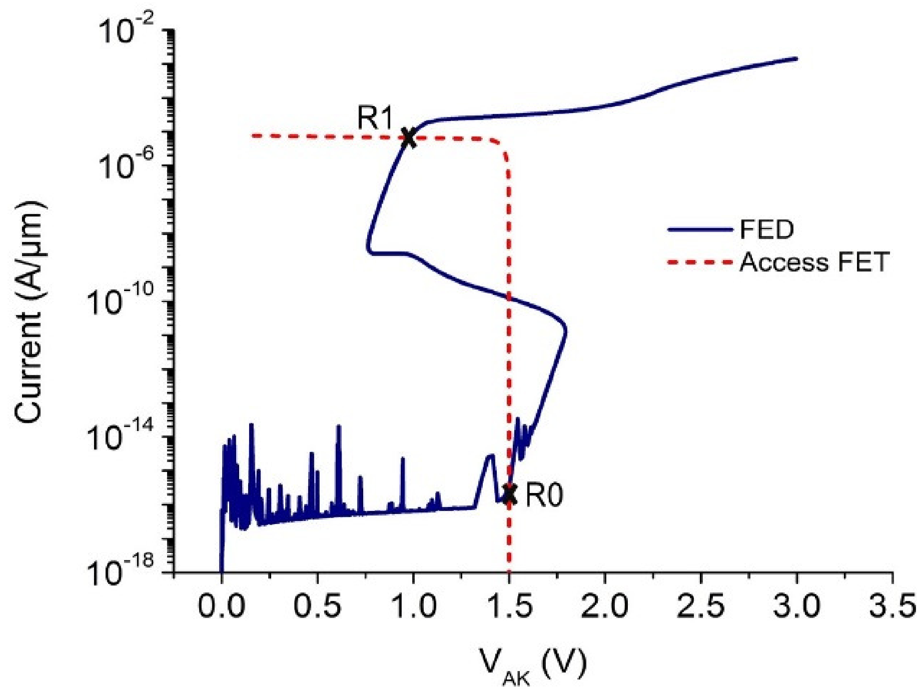



**Figure 4.2 DC I-V characteristics of the FED and the access MOSFET load line, plotted against the Anode to Cathode voltage (VAK): the read "1" (FED ON) and read "0" (FED OFF) points are clearly marked.VG1 = 1.2V, VG2 = -1.2V, VGA = 0V and the bit line is grounded (VBL = 0V). Load line at VA = 1.5V.**

The basic operation of the memory cell (write "1"/"0" (W1/W0), hold "1"/"0" (H1/H0) and read "1"/ "0" (R1/R0)) is explained with the help of Timing Diagram I, shown in Figure 4.3; to write "1", the thyristor is turned on by forward-biasing the middle junction through the application of a pulse on word line 2 (WL2). This pulse should be adjusted so that its rising edge is sufficiently fast and its falling edge somewhat slower. To write "0", the thyristor is turned off by a fast falling edge WL2 pulse. The voltage pulse magnitudes are shown in Figure 4.3 and explicitly given in Table 4.1; in all operations the anode and WL3 voltages are kept fixed. An asymmetrical WL2 pulse is used for W1 (width = 1 ns, rise time = 0.5 ns, fall time = 2 ns), whereas a symmetrical pulse is used for W0 (width = rise time = fall time = 1 ns).

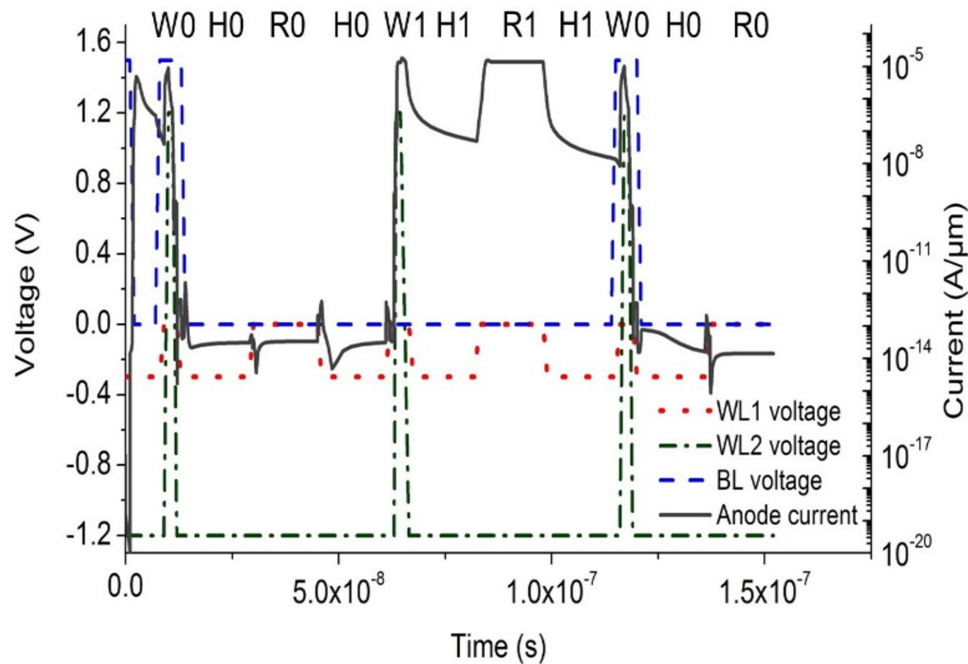



**Figure 4.3 Timing Diagram I: basic memory cell operation (W0/W1, H0/H1, R0/R1)**

**Table 4.1 Timing Diagram I voltages**

| Operation | WL1 (V) | WL2 (V) | BL (V) | WL3 (V) | Anode (V) |
| --- | --- | --- | --- | --- | --- |
| Hold | -0.3 | -1.2 | 0.0 | 1.2 | 1.5 |
| Write “0” | 0.0 | 1.2 | 1.5 | 1.2 | 1.5 |
| Write “1” | 0.0 | 1.2 | 0.0 | 1.2 | 1.5 |
| Read | 0.0 | -1.2 | 0.0 | 1.2 | 1.5 |

To examine the W1/W0 operations more carefully, Figure 4.4 shows the carrier density profiles across the FED device immediately following the write operation. The observed high carrier densities in the gap area (between the gates) after W1 indicate that the middle junction is forward biased and thereby the thyristor is in its ON state. On the other hand, the low carrier densities (in the same gap area) after W0 indicate that the middle junction is reverse biased and thereby the thyristor is in its OFF state.

The Hold state is controlled by the voltage applied on WL1. For Timing Diagram I this voltage is selected such that the “leakage” current of the access transistor can support the hold current of the thyristor in the H1 state. Under this condition, once turned on the thyristor stays on, and thus once written, data “1” remains valid indefinitely [35]. This however is achieved at the expense of considerable standby power dissipation due to the elevated H1 current (more than four orders of magnitude higher than the H0 current; see Figure 4.3).

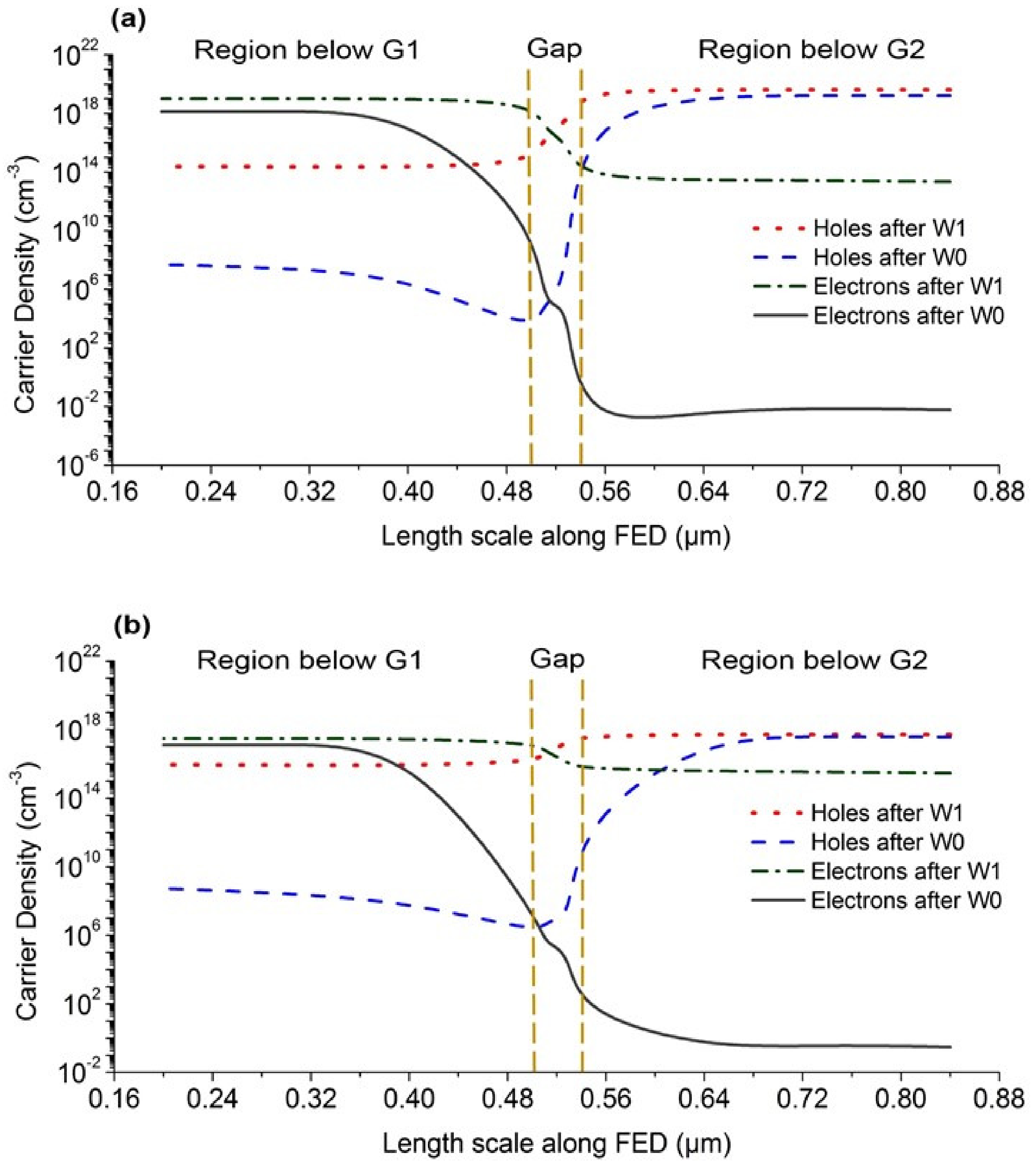



**Figure 4.4 Carrier density profiles following W1 and W0 at a depth of 1nm (a) and at 10nm (b). These profiles suggest that following W1, the middle junction is forward biased, whereas following W0, the junction is reverse biased.**

## 4.3 Hold and Restore

An improved Hold scheme (Timing Diagram II) which significantly reduces the H1 current and consequently the power dissipation is shown in Figure 4.5.

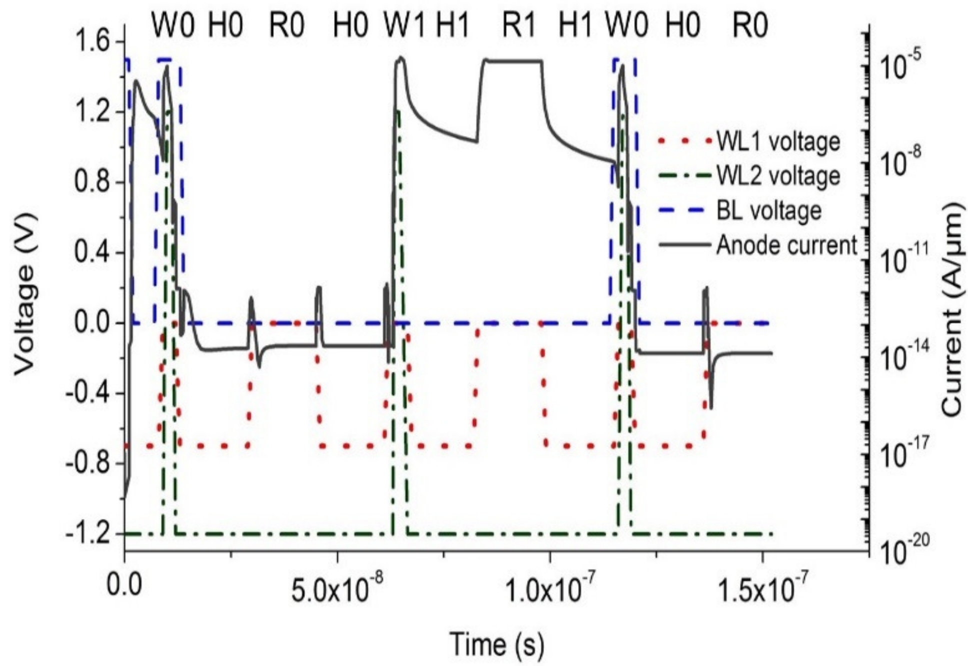



**Figure 4.5 Timing Diagram II: memory cell operation with improved hold scheme. WL1 voltage = -0.7V during hold**

**Table 4.2 Timing diagram II voltages**

| Operation | WL1 (V) | WL2 (V) | BL (V) | WL3 (V) | Anode (V) |
|---|---|---|---|---|---|
| Hold | -0.7 | -1.2 | 0.0 | 1.2 | 1.5 |
| Write “0” | 0.0 | 1.2 | 1.5 | 1.2 | 1.5 |
| Write “1” | 0.0 | 1.2 | 0.0 | 1.2 | 1.5 |
| Read | 0.0 | -1.2 | 0.0 | 1.2 | 1.5 |

The reduction in the power dissipation is accomplished by selecting WL1 voltage such that the access transistor is kept completely OFF during both H1 and H0. Table 4.2 lists the voltages pulse magnitudes for timing diagram II; WL1 voltage during Hold is the only difference between Timing Diagram I and Timing Diagram II, all the other pulses are similar.

The dc I-V characteristics of the FED and the access MOSFET load lines under both hold schemes are shown in Figure 4.6: hold scheme I current is seen to be many orders of magnitude higher than hold scheme II current. Also, the hold current following W1 for both hold schemes is plotted vs time in Figure 4.7: the hold current for scheme II decays rather fast, quickly reaching H0 current levels. However these benefits of low hold current and reduced power dissipation come at the expense of the need to augment the Hold operation by a “Restore” pulse [33], which must be applied periodically while on Hold.

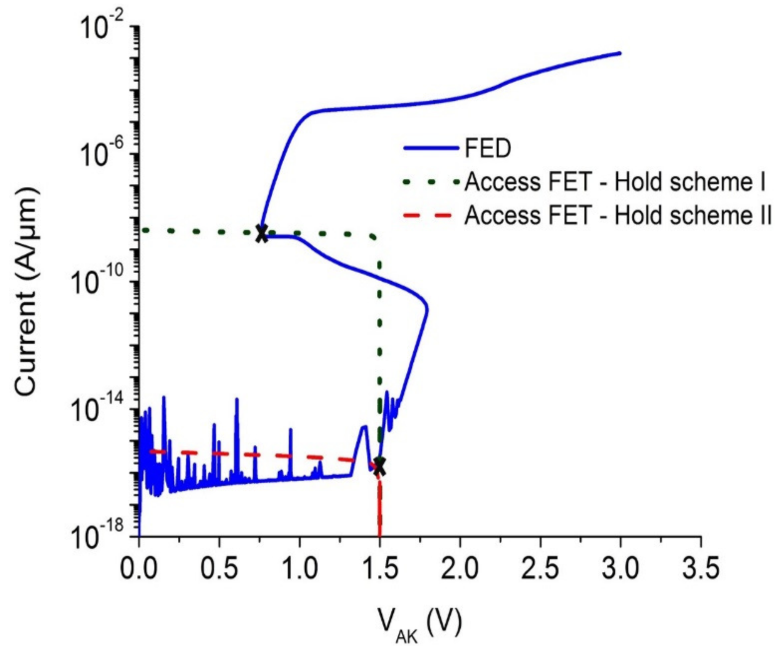



**Figure 4.6 DC I-V characteristics of the FED and the access MOSFET load lines under Hold scheme I (WL1 voltage = -0.3V) and Hold scheme II (WL1 voltage = -0.7V). VG1= 1.2V, VG2 = -1.2V, and the bit line is grounded (VBL = 0V). Load line at VA=1.5V.**

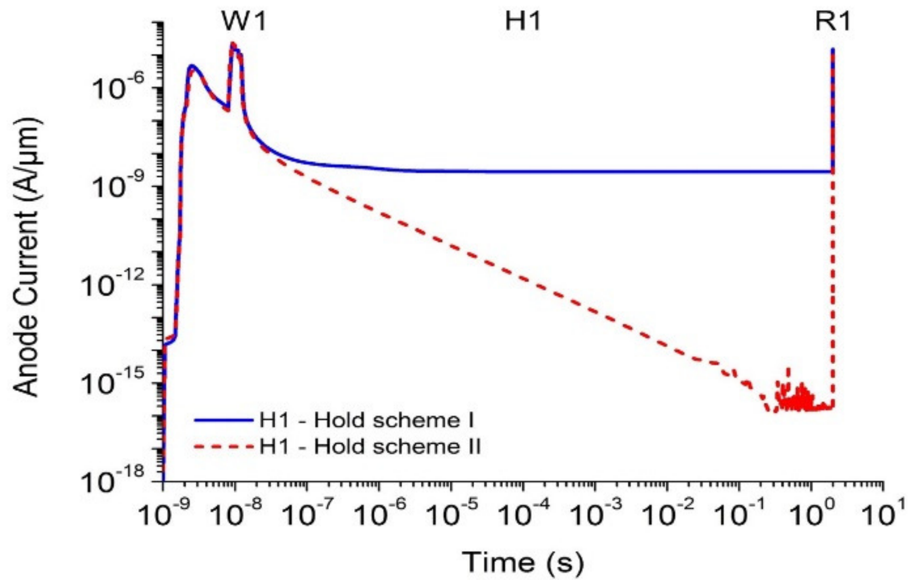



**Figure 4.7 Comparison of H1 schemes: in the first method state “1” is held by allowing the minimum leakage current through the access MOSFET necessary to keep the FED in the ON state. In the second the access MOSFET is OFF and state “1” is held by the addition of a restore pulse.**

The need for “Restore” operations can be understood with the help of the carrier density profiles shown in Figure 4.8, which demonstrate that following W1 the carrier densities decrease with time and data”1” is lost. A short restore pulse must therefore be applied, which leads to the activation of the internal regenerative feedback loop of the thyristor [33] and the full recovery of the stored data.

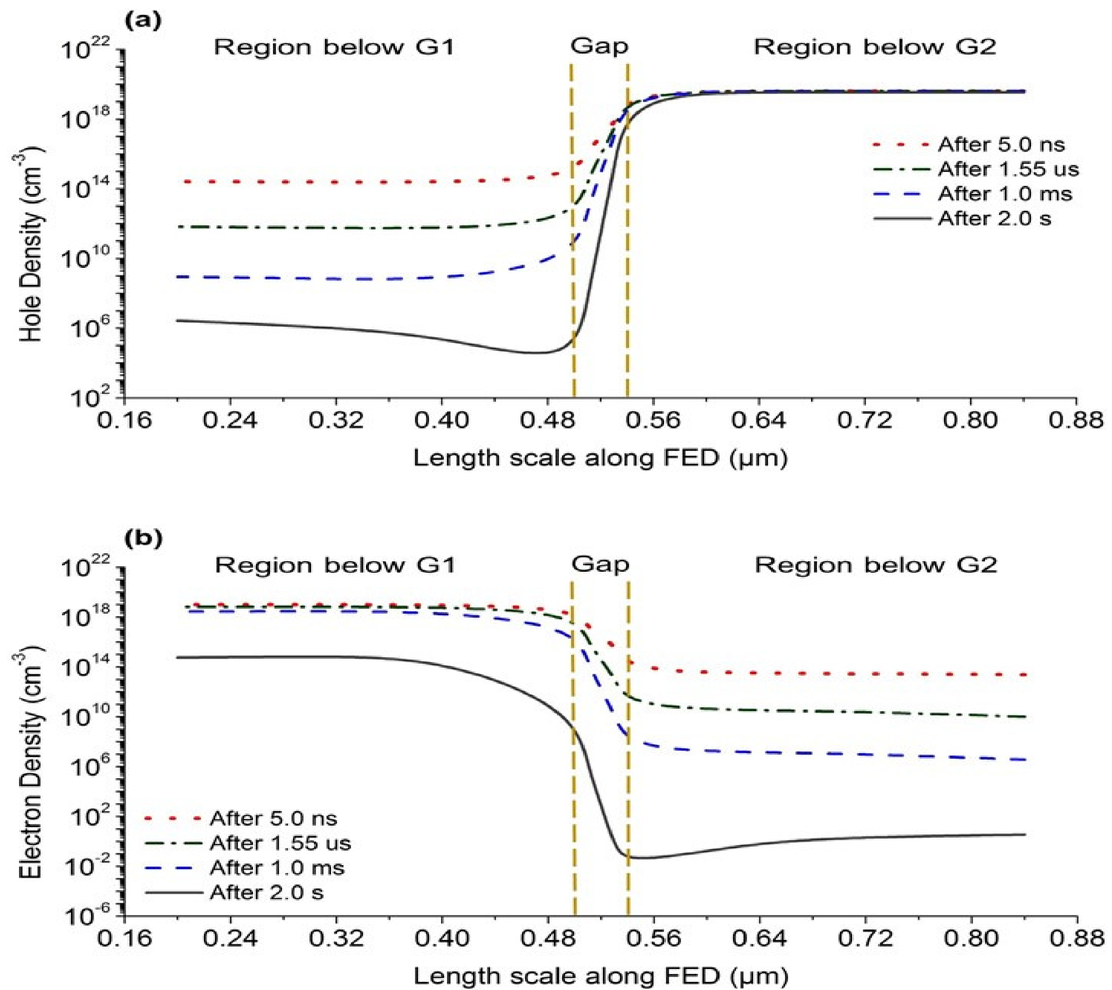



**Figure 4.8 Carrier density profiles across the FED at a depth of 1nm, taken at different times following H1 using Hold scheme II: (a) holes and (b) electrons. The carrier densities decrease with time, especially in the gap region between the two gates, which means that state “1” will be lost unless a restore operation is executed.**

An implementation of the restore operation is shown in Figure 4.9. It is performed by pulsing WL1 to 0.0 V for 1 ns while keeping the other lines at their hold voltage levels. It can be clearly seen that state “1” is successfully held and that restore pulse does not affect state “0”.

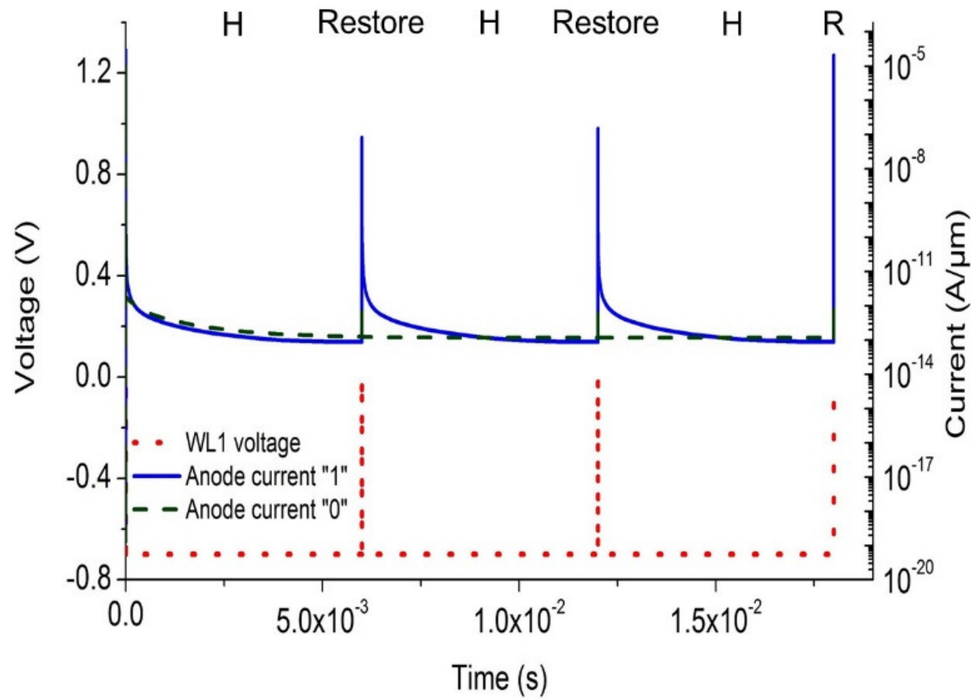



**Figure 4.9 H1/H0 restore operations at T = 378K: First “1”/”0” were written, followed by two successive restore pulses and a read operation, all spaced 6ms apart.**

The restore time ($t_{rest}$), is defined as the time period, with the cell on Hold, after which each successive restore pulse must be applied. Figure 4.10 shows that $t_{rest}$ varies exponentially with the inverse of the temperature with an activation energy $E_A \approx 0.7$ eV,

ranging from 2 s at room temperature to 6 ms at T = 378 K. This is consistent with the fact that:

$$t_{rest} \propto R^{-1} \propto (np)^{-1}$$

$$np = n_i^2 * e^{V_f} = N_c N_v \, e^{\frac{V_f - E_g}{KT}}$$

$$t_{rest} \propto N_c N_v \, e^{\frac{E_g - V_f}{KT}}$$

where $V_F$ is the "average" forward bias of the middle junction (≈ 0.4 V from Figure 4.8) and the rest of the symbols have their usual meanings [24].

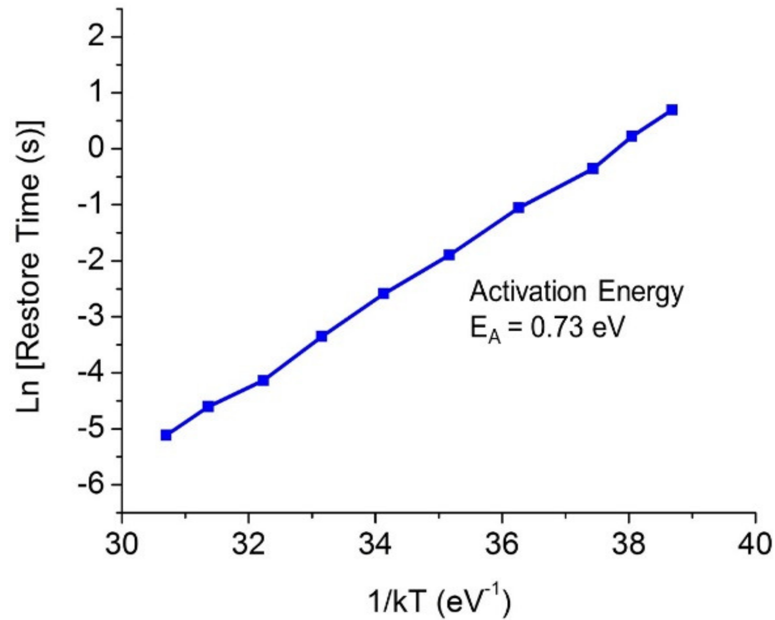



**Figure 4.10 Arrhenius plot of the restore time vs. temperature, where the activation energy EA ≈ 0.7eV: the restore time drops exponentially with rising temperature due to increased carrier recombination at higher temperatures.**

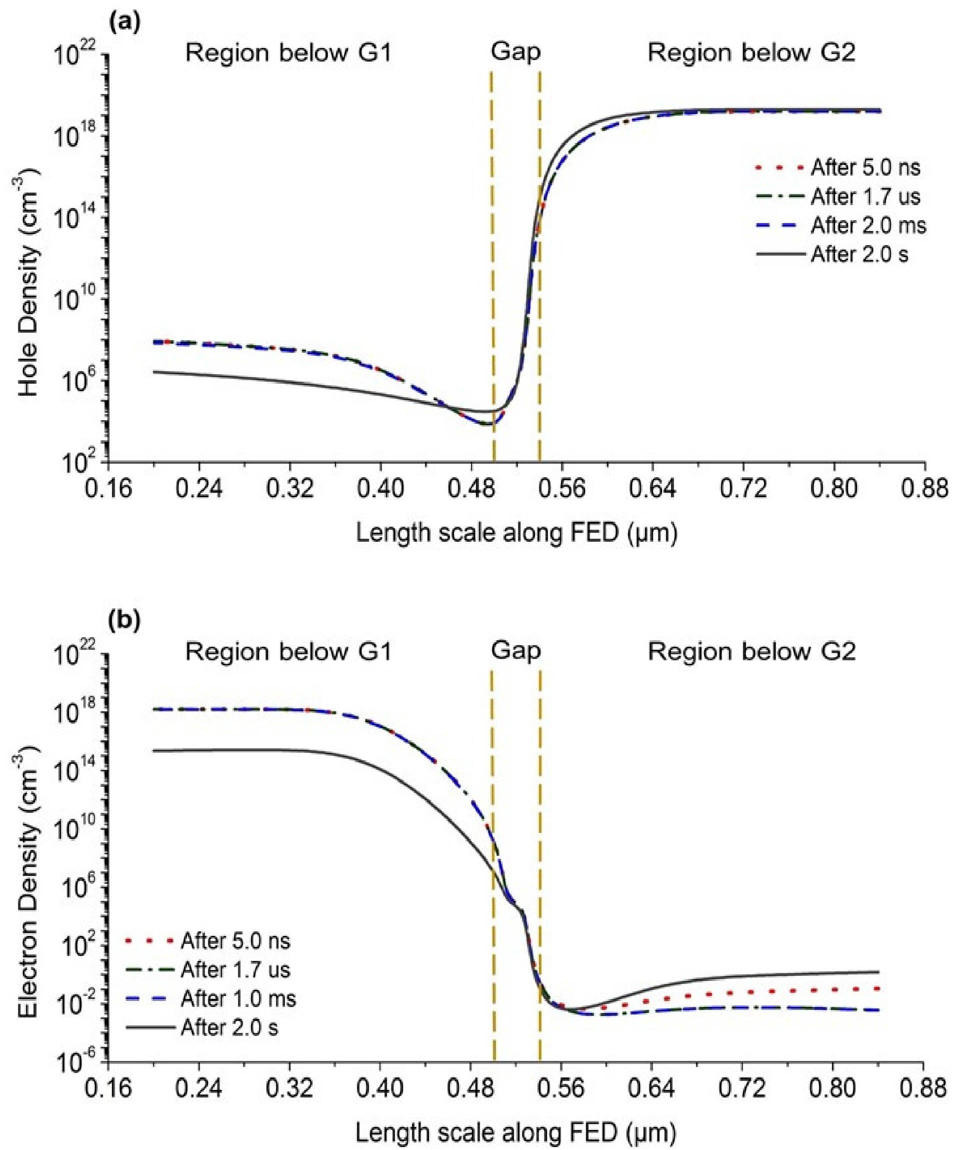



**Figure 4.11 Carrier density profiles across the FED at a depth of 1nm, taken at different times following H0 (valid for both Hold schemes): (a) holes and (b) electrons.**

With regard to data “0”, it is seen from Figure 4.9 that it is not affected by the restore pulse. In fact, once “0” is written, it is maintained indefinitely as seen from the carrier profiles in Figure 4.11. These profiles show that following W0, the carrier densities remain constant with time in the gap region and therefore the middle junction remains reverse biased and FED in OFF, and as a result, the “0” states is held indefinitely, even at elevated temperatures as can be seen in Figure 4.12.

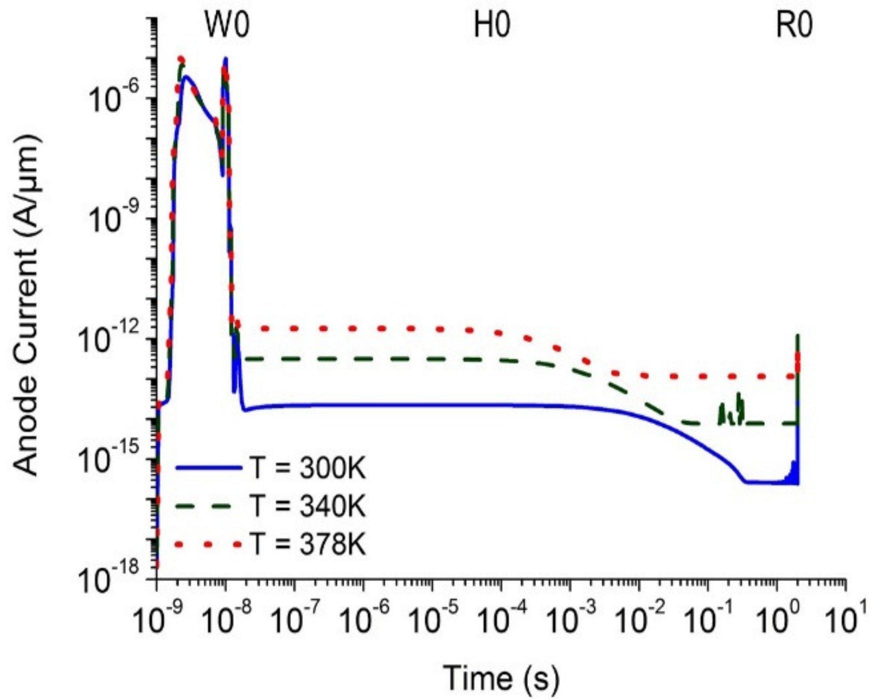



**Figure 4.12 W0, followed by H0 for 2s, then R0 at three different temperatures: once written, data “0” is maintained indefinitely**

## 4.4 Alternate Write "1" Scheme

In Timing Diagrams I and II above, the bias on gate G1 (next to the anode) was kept fixed at $V_{G1}$ = 1.2 V throughout the cell operation. In an alternate cell operation method (Timing Diagram III) the bias on gate G1 is no longer kept constant, but instead during W1 a pulse is applied to it as shown in Figure 4.13 [54], which temporarily eliminates the middle junction [26]. The requirements on this pulse magnitude and the rise/fall times are more relaxed compared to G2 pulses above. However, pulsing gate G1 necessitates the addition of a third word line (WL3), which makes the memory array more complicated. The voltage pulse magnitudes for this timing diagram are in Table 4.3.

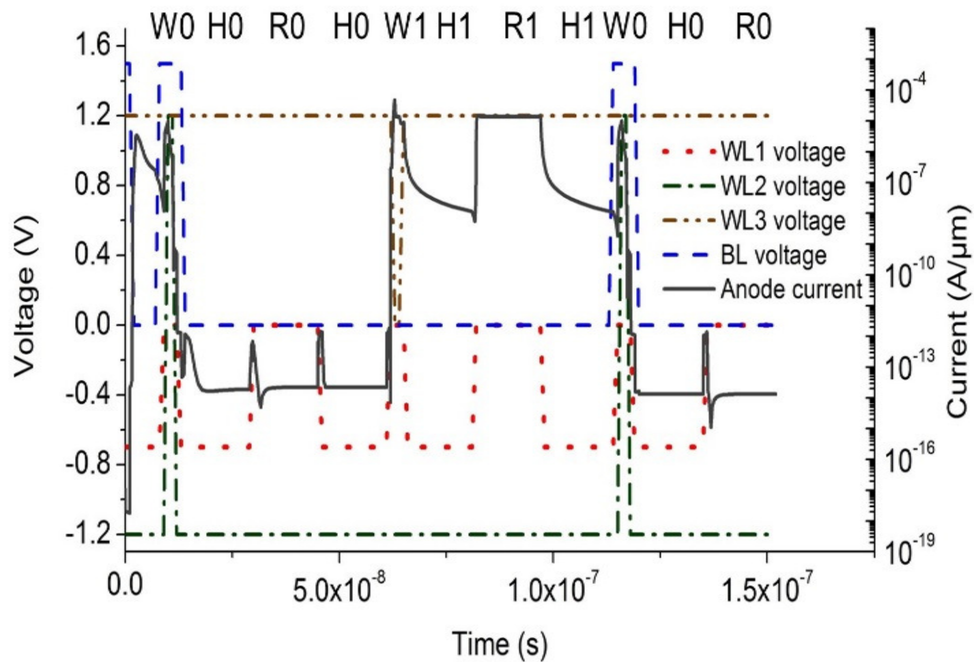



**Figure 4.13 Timing Diagram III: memory cell operation incorporating pulsing gate G1 for W1. For both G1 and G2 pulses: width 1ns, rise time = fall time = 1ns.**

**Table 4.3 Timing diagram III voltages**

| Operation | WL1 (V) | WL2 (V) | BL (V) | WL3 (V) | Anode (V) |
|---|---|---|---|---|---|
| Hold | -0.7 | -1.2 | 0.0 | 1.2 | 1.5 |
| Write “0” | 0.0 | 1.2 | 1.5 | 1.2 | 1.5 |
| Write “1” | 0.0 | -1.2 | 0.0 | 0 | 1.5 |
| Read | 0.0 | -1.2 | 0.0 | 1.2 | 1.5 |

## 4.5 Memory Array and Disturbance Control

Achieving robust “disturb” control is an important and challenging issue when the cells are arranged in memory arrays [18]. For FED SRAM, the disturb control issue can be addressed using the circuit techniques and methodology suggested by Roy et al. [55].

The proposed memory array is shown in Figure 4.14. The bit lines are labeled as odd (O) or even (E); cells in the same row have the same bit line while cells in the same column share the word lines.

The read operation is performed through a sense amplifier (comparator), the bit lines are fed to one input while the other input is tied to a reference voltage. The BL is kept at low voltage level while the cell in the hold state and the read operation is triggered by asserting WL1. Based on the cell content, the BL is either pulled up (higher than the reference voltage) by the high R1 current or stays at the low voltage level due to the very low R0 current. The capacitive coupling between the adjacent bit lines increases the required reference voltage which leads to longer read time. This problem is tackled by using a shielding technique where the adjacent bit lines of the target cell are held to ground when the cell is being read. i.e., when an even (odd) BL is being read, the

adjacent odd (even) bit lines are held at ground. This is shown in the Read Cycle of the timing diagram in Figure 4.15

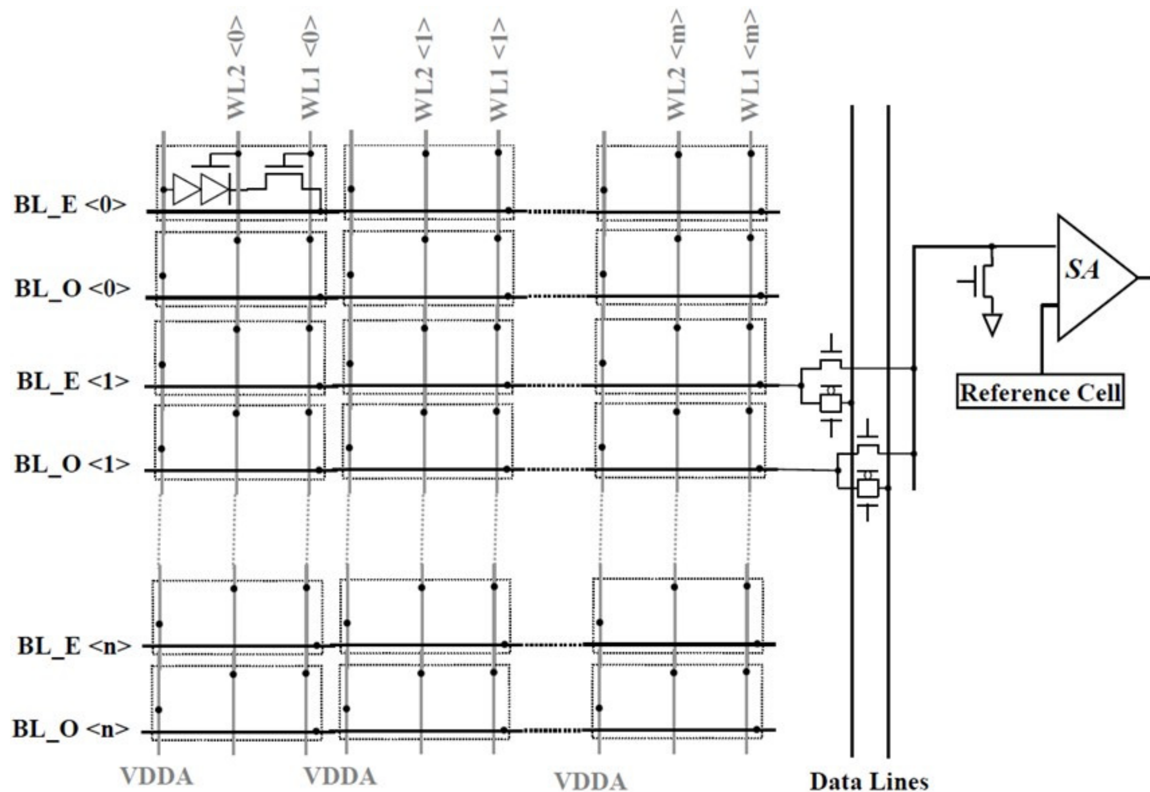



**Figure 4.14 Memory array for SRAM cells [55]**

Since all cells in the same column have the same WL2, all of these cells will get written non-selectively by pulsing WL2 to write the target cell. This issue is solved through a pre-read operation with taking the shielding technique into consideration. Given that only every other BL can be read simultaneously, a pre-read operation should be performed on the interleaved cells that are not intended to be read. i.e., writing on even

bit lines should be preceded by a pre-read on the odd bit lines as shown in the Write Cycle of the timing diagram in Figure 4.15.

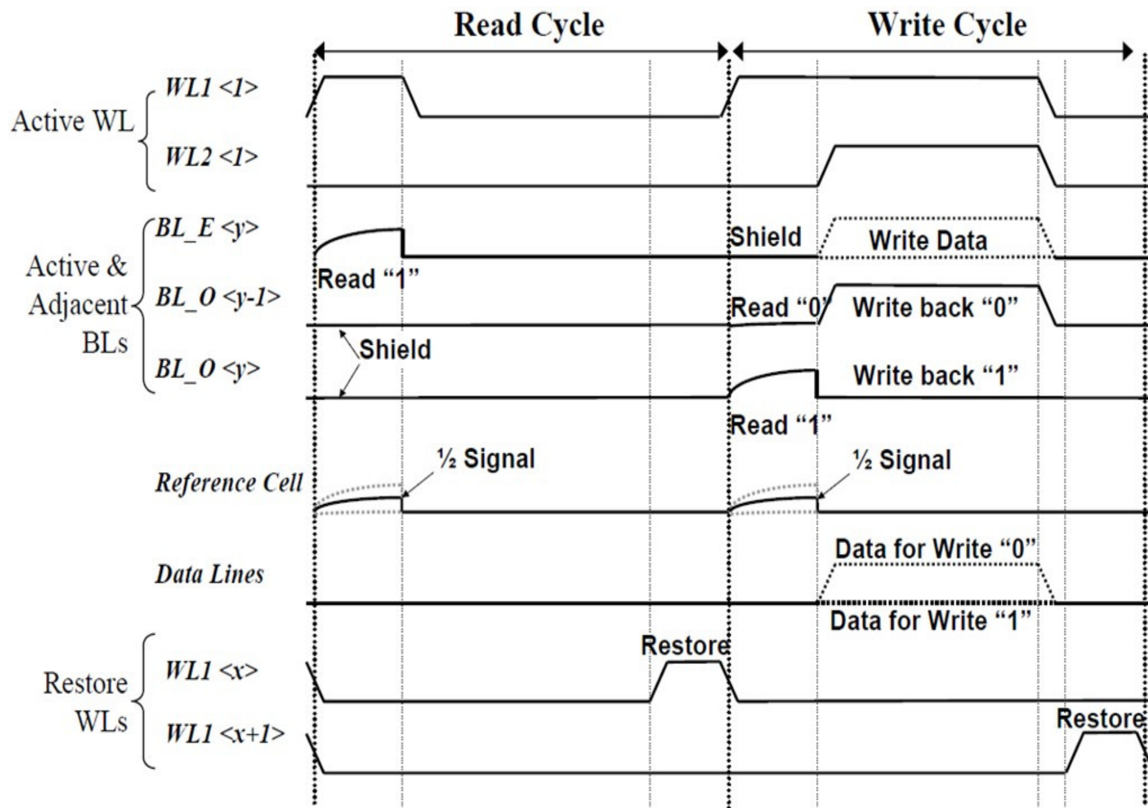



**Figure 4.15 Timing diagram including "shield" and "pre-read" operations for disturb control [55].**

## 4.6 Conclusion

A well behaved new SRAM cell, based on the SOI FED, has been described and its operation explained. It relies on the ability to bias the FED in the "induced thyristor" mode of operation and the exploitation of the bi-stable nature of the thyristor characteristics. The new FED SRAM is more flexible than the TCCT SRAM, and its

retention superior: here the p-n junctions “sandwiched” between anode and cathode are gate-induced, rather than built-in (“doped-in”), and thus there is no need for precise control of the film doping profile and the nearly intrinsic SOI film has higher carrier lifetime and improves the state “1” retention (i.e., $t_{rest}$). Although a somewhat “relaxed” geometry FED was used here for “proof of concept” purposes, our previous results [50, 52] suggest that it should be possible to design FED memory cells of superior scalability and performance. The gap length between gates G1 and G2 can be shrunk down to the technological limit without affecting the FED properties very much [51]. In fact it is possible to push scaling even further (down to the 20 nm node according to our simulations [52]) by using advanced FEDs such as Double-Gate (DG), Gate-All-Around (GAA) and other Multi-Gate (MuG) structures, where the gate control of the channel is stronger. In these cells, each of the two FED gates G1 and G2 will be replaced by a DG, a GAA, or a MuG, leading among other things to a shorter total device length and ultimately faster operation.

# CHAPTER 5 DESIGN AND OPERATION OF FED BASED DRAM CELL

## 5.1 Introduction

The current 1T-1C DRAM cell faces serious challenges in scaling and leakage that are difficult to overcome. Therefore, there is currently an urgent need for new memory devices and several alternative approaches are under aggressive investigation in laboratories around the world [56]. One approach based on the floating body effect of the MOSFET has gained a lot of attention and multiple implementations of capacitor-less floating body memory cell (FBC) have been reported [18-21,57]. Although the FBC has small cell size and it is CMOS compatible, it has small “1”/”0” currents ratio and slow read and write operation.

With the help of numerical device simulations, a dynamic RAM cell with excellent characteristics based on the FED is presented, and the design guidelines and timing diagrams for correct operation, speed, and retention are established. High read “0”/”1” current margin, fast write/read time, good retention, and densely packed cells are obtained.

The FED DRAM cell is similar the TCCT DRAM cell in theory and operation [34], however thyristor-like mode of operation of the FED is gate induced, whereas it is built-in in TCCT.

## 5.2 FED DRAM Cell: Structure and Operation

A cross-section of the SOI FED is shown in Figure 5.1. Through suitably biasing G1 positively at $V_{G1}$ and G2 negatively at $V_{G2}$, electrons will accumulate in the silicon film below G1 and holes below G2, and thus the FED acts like a pnpn thyristor. The simulated $I_A$–$V_A$ characteristics of the FED under these bias conditions are shown in Figure 5.2. The target operating points of the FED as a memory cell are also clearly marked: the FED, biased as pnpn thyristor, is operated as a memory cell by using the 2 stable regions of the thyristor to define the stored data.

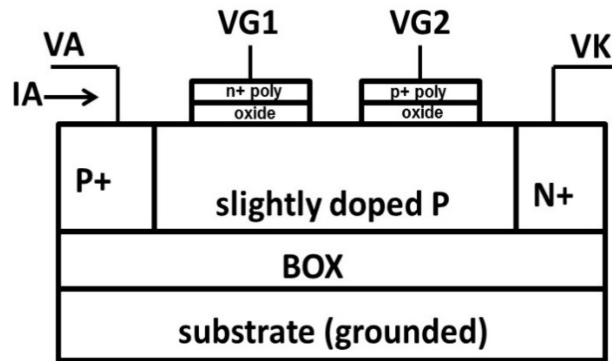



**Figure 5.1 FED resembles a p-i-n diode augmented by two closely spaced gates, G1 next to the anode A and G2 next to the cathode K. It behaves as a pnpn-induced thyristor when G1 is biased positive and G2 is biased negative or grounded**

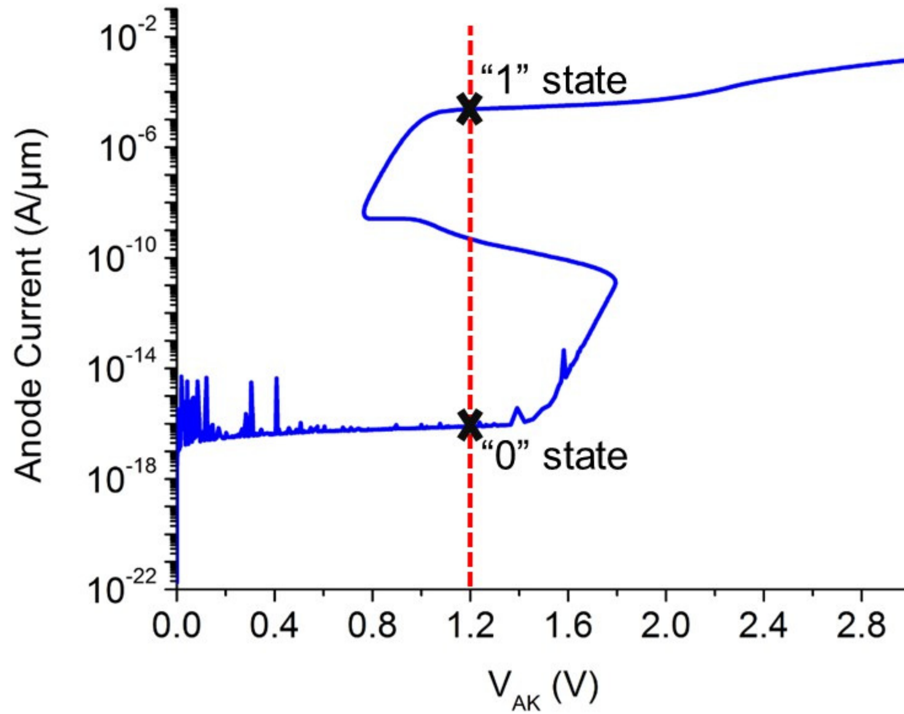



**Figure 5.2 Simulated anode current–voltage characteristics (IA versus VA) at VG1 = 1.2V, VG2 = -1.2V and cathode K grounded. 20nm-thick SOI, slightly p-type ($10^{16}$ $cm^{-3}$); equal gate lengths LG1 = LG2 = 400nm, and Lgap = 40nm.**

To operate the device as a memory cell, it must be possible to write and read 1 (W1/R1), write and read 0 (W0/R0), and hold 1 and 0 (H1/H0) with sufficient margin, speed, and retention time. With the simple timing diagram [58] shown in Figure 5.3, standby (hold) H1/H0 is achieved with $V_A = V_K = V_{G1} = 1.2$ V and $V_{G2} = -1.2$ V. To write "1", $V_K$ is briefly pulsed down to ground while simultaneously $V_{G2}$ is pulsed up to ground. To write "0", gate G2 is briefly grounded. To read the cell, the cathode is grounded and the current through the anode is monitored.

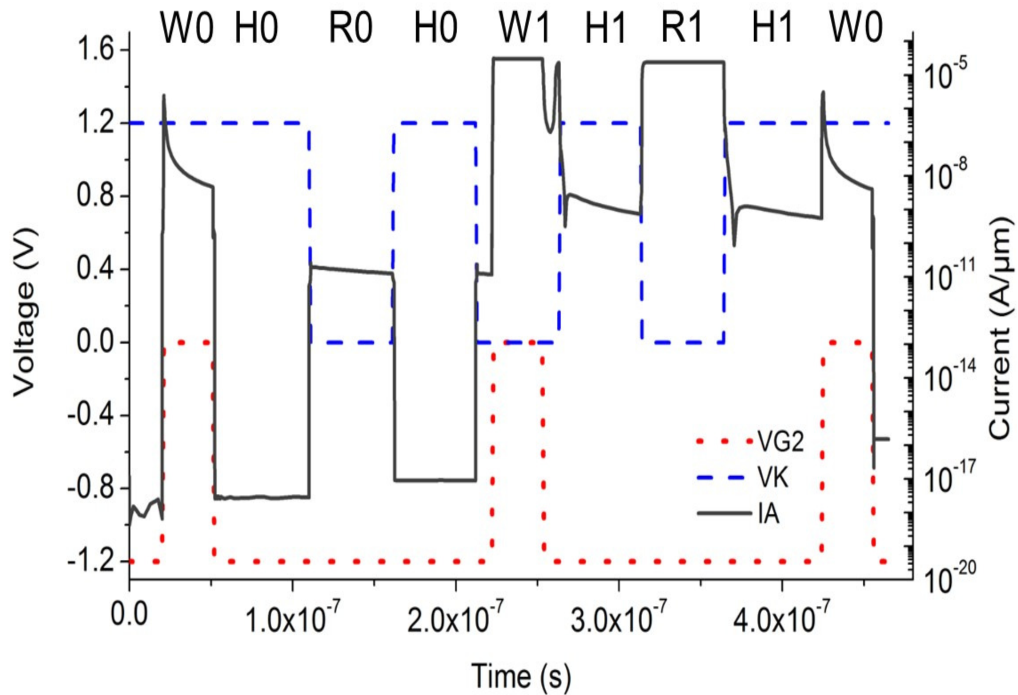



**Figure 5.3 Simple cell operation timing diagram. At standby, VA = VG1 = VK = 1.2V and VG2 = -1.2V. To write "0" gate G2 is briefly pulsed to 0 V. To write "1", cathode K and gate G2 are both briefly pulsed to 0 V. To read "1"/"0", cathode K is grounded and the anode current IA is monitored.**

## 5.3 Demonstration and Discussion

A more optimized timing diagram, with both gates G1 and G2 pulsed, is shown in Figure 5.4 where, starting from an undefined state, a complete W/H/R/H/W sequence demonstrates the correct cell functionality, and the ON/OFF current margin is more than 10 orders of magnitude. The read R1 current may appear a little low, but if needed, it can be adjusted by choosing the right SOI film thickness [50]. The advantages of this method include high speed writing and reading operations, High read "0"/"1" current margin, and high retention time.

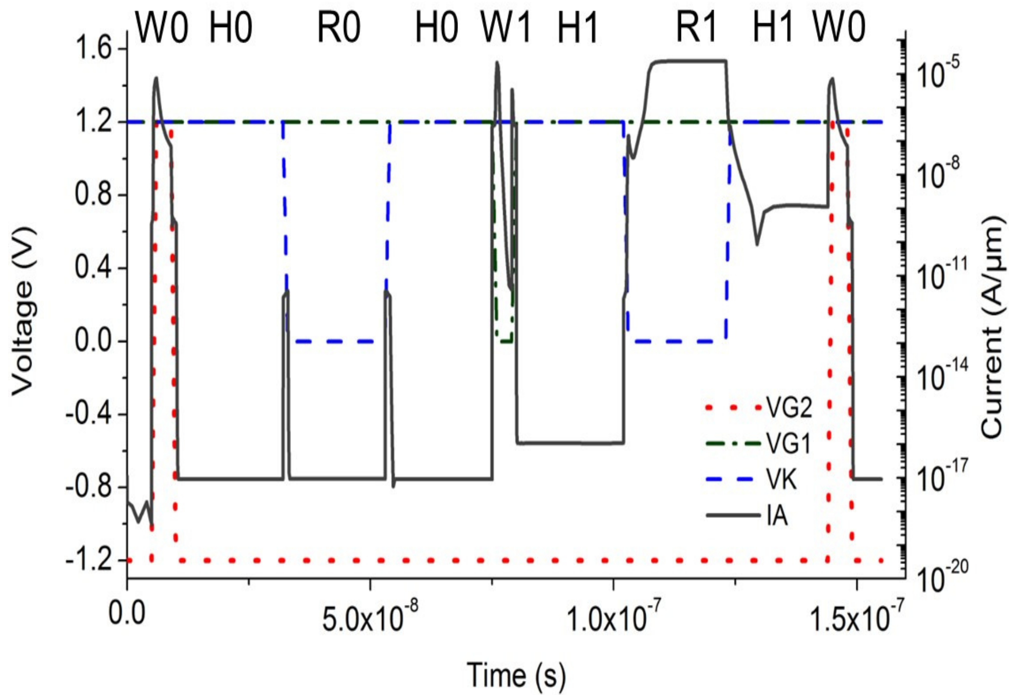



**Figure 5.4 Complete cell timing sequence. Hold: VA = VK = VG1 = 1.2V, VG2 = -1.2 V; W1: VA = VK = 1.2V, VG2 = -1.2V, VG1 is pulsed down to 0V for 3ns and then back to 1.2V; W0: VA = VK = VG1 = 1.2V, VG2 is pulsed for 3ns up to 1.2V and then back to -1.2V; Read: Monitor IA at VA = VG1 = 1.2V, VG2 = -1.2V, VK= 0V.**

## 5.4 Retention Time Characteristics

The stored data on the FED memory cell would eventually be lost due to the leakage currents in the cell while it is in the hold state. Retention time can be defined by how long the memory cell can keep its data before it is lost.

Data “0” is defined by the OFF state of the thyristor; the leakage current due to carrier generation in the cathode and the middle junction [59] leads to data “0” to be lost thus a refresh operation is required. However, the FED cell has long retention “0” time (1 sec for T = 300 K). This is shown in Figure 5.5 where the electrostatic potential in the p -

base region is plotted. When the potential reaches 0.4 V the cell loses the “0” state and data refresh is required.

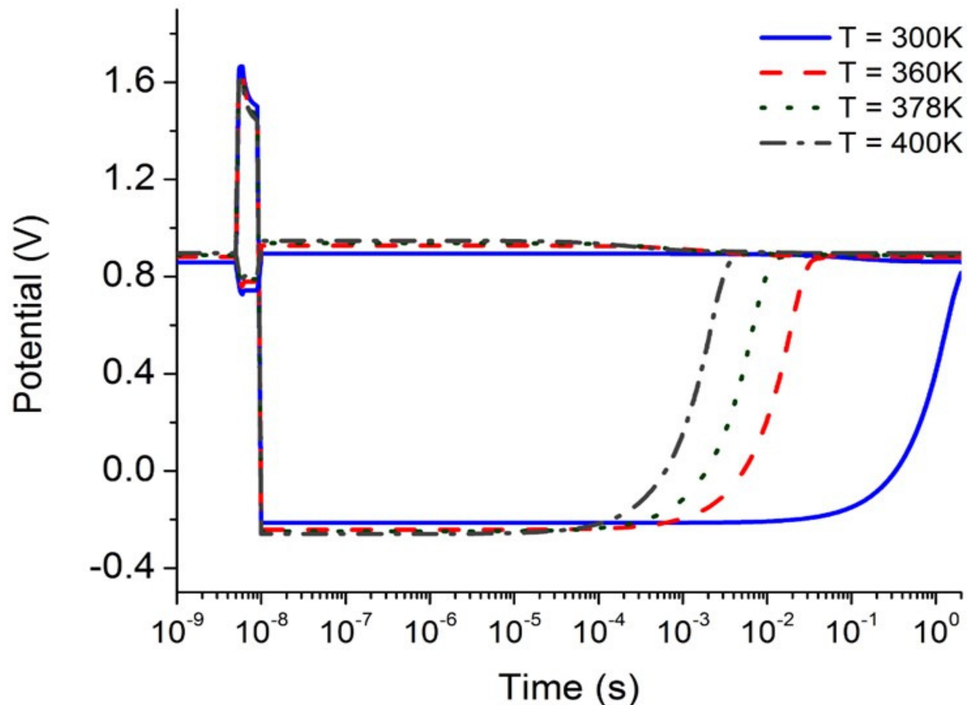



**Figure 5.5 numerically simulated electrostatic potential versus time plots in the p- base region following W0 (lower family of curves) and W1 (upper family of curves) at four different temperatures. Long retention time is observed in both cases: up to 1 s for data “0” whereas data “1” is retained for as long as power is on.**

In fact, the retention time for Data “0” is highly relevant to the characteristic time to form the surface inversion layer in the MOSFET which is in order of [$2N\tau / n_i$] where “$\tau$” is the carrier life time and “$N$” is the doping concentration [24]. Retention time for the “0” state is temperature dependent. As shown in Figure 5.6, the relationship between the “0” retention time and temperature can be characterized based on previously

mentioned equation of characteristic time to form the surface inversion layer in the MOSFET and the equation of the intrinsic carrier concentration: $n_i = \sqrt{NcNv}\ e^{-Eg/2KT}$

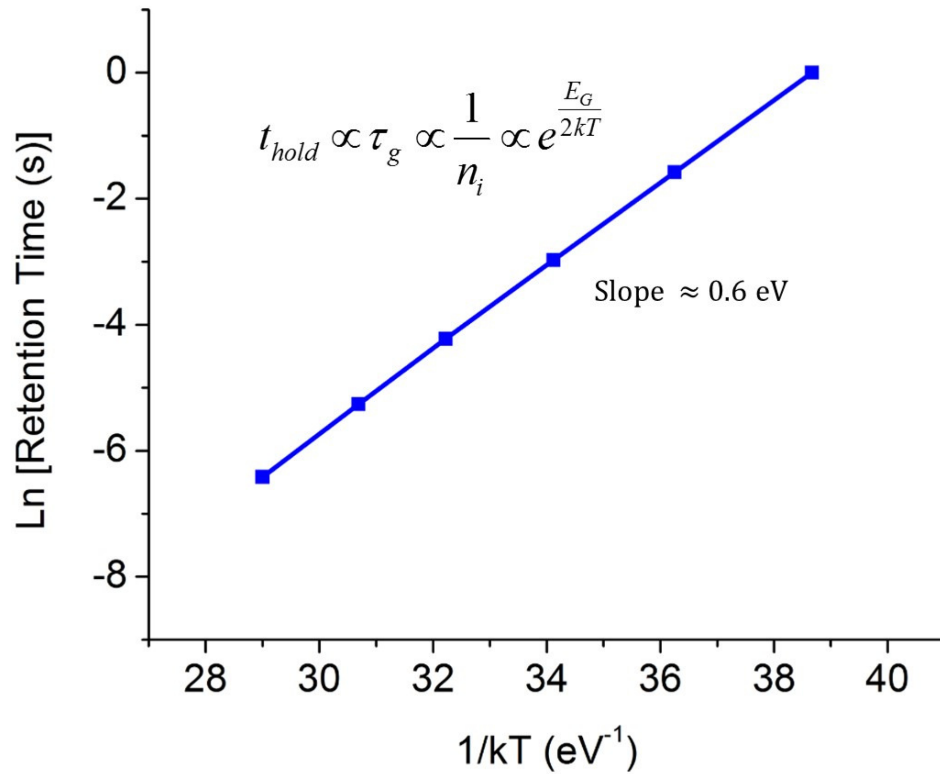



**Figure 5.6 Straight line Arrhenius plot with slope 0.6 eV, typical for thermal carrier generation**

The FED memory cell shows also excellent retention characteristics under repetitive readings, i.e. the reading operation is not destructive. This is shown in Figure 5.7.

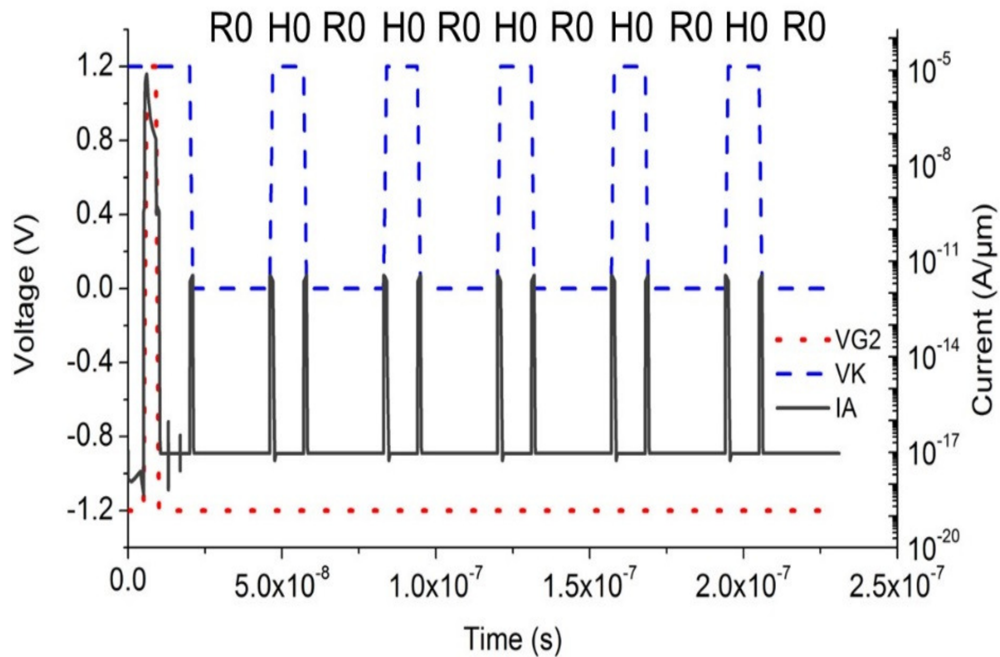



**Figure 5.7 H0/R0 sequence demonstrates that once written, 0 may be repeatedly read nondestructively.**

In the FED memory, data "1" is defined by the ON stable state of the thyristor which leads for data "1" to be retained as long as the power is on. This is shown in Figure 5.5 (upper family of curves). Figure 5.8 shows that R1 is a self-refresh operation and can therefore be repeatedly read without any degradation it also shows the hold current H1 following read R1 in Figure 5.3 and Figure 5.4 is a fast decaying current and is a result of the floating body nature of the cell.

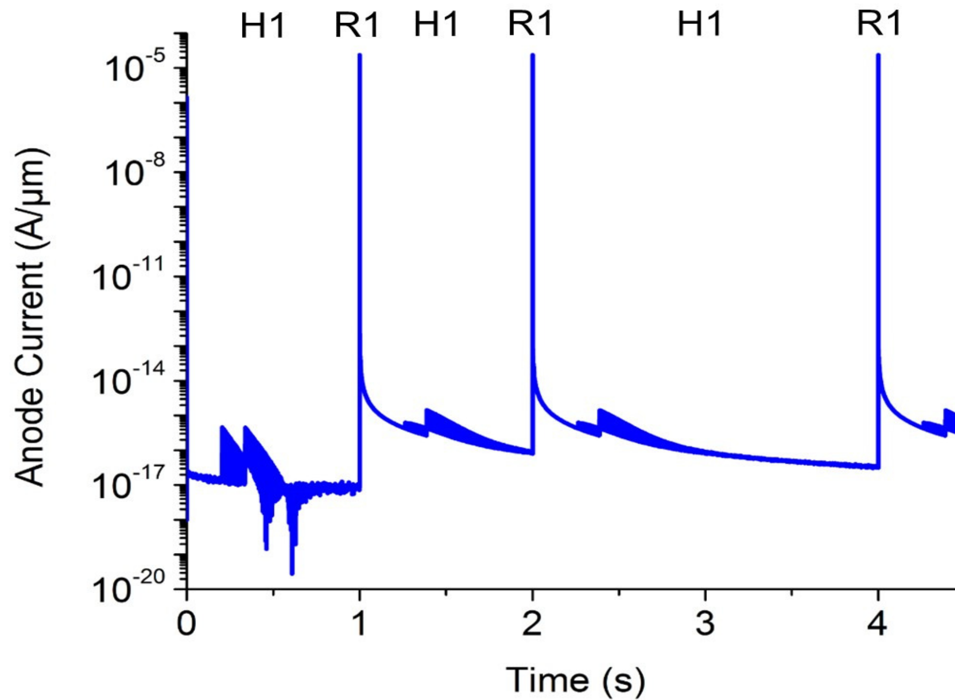



**Figure 5.8 H1/R1 sequence demonstrates that once written, 1 may be read repeatedly nondestructively for a long time, as a matter of fact, R1 is self-refreshing. It also demonstrates the fast decaying nature of the hold current.**

An important issue with floating body cells is that they generally face serious challenges in achieving robust disturb control when used in a memory array [20]. This remains the case with our cell, too, and we are currently investigating various timing schemes to resolve this problem. The FED memory cell is more flexible than the TCCT cell, and its performance is superior: here the p-n junctions sandwiched between anode and cathode are gate induced, rather than built-in (doped-in), and thus there is no need for precise control of the film doping profile; on the contrary, the nearly intrinsic film has higher carrier lifetime and improves the 0 state retention (H0). Similarly to the TCCT cell, several other operation schemes are possible [33, 34, 60].

## 5.5 Conclusion

A well-behaved memory cell based on the SOI FED was described and its operation was explained. Its operation relied on modifying the conductivity of the SOI film locally by suitably biasing the gates. It is more flexible and easier to fabricate than the TCCT memory cell and its performance was superior: the nearly intrinsic film had higher carrier lifetime which improved the “0” retention, whereas once written, “1” was retained for as long as the power was on.

# CHAPTER 6 MEMORY MECHANISM OF THE GATED-THYRISTOR DRAM CELLS

The operation of dynamic TRAM and FED-RAM cells is revisited to clarify the memory mechanism. The resulting carrier profiles demonstrate that the recently advanced interpretation of the physical memory (i.e. store) mechanism, as the accumulation (for data "1") or depletion (for data "0") of holes in the p-base (under the gate), is incorrect. Instead, it turns out that it is the presence (for data "0") or absence (for data"1") of deeply depleted regions within the cell structure, associated with the two p-n-junctions on the sides of the p-base that determines the stored data of the cell.

## 6.1 Introduction

Research on new memory cell technologies has been aggressively pursued for a long time, and there are no signs of it slowing down. This is in response to the ever increasing need to manipulate and store a perpetually growing volume of data. Among the various memory types currently under research (resistive random access memory (RRAM), magnetic random access memory (MRAM), etc.), the one most related to CMOS is the TCCT RAM (TRAM) cell. As seen in Figure 6.1 (a), the TRAM cell structure is simply a SOI pnpn thyristor augmented by a regular MOS gate over the p-base, which exploits the bi-stable nature of the thyristor characteristics to store data. The MOS gate provides capacitive coupling to the p-base of the TCCT, which enables

switching speeds orders of magnitude faster than conventional thyristors [33]. One drawback of the TRAM cell is that it is a “built-in” structure, requiring precise and tight control of the doping profiles during fabrication. To solve this problem, we have proposed an “induced” thyristor version of the memory cell, whereby an SOI FED is used instead of a built-in thyristor a schematic of which is shown in Figure 6.1 (b): by keeping gate G2 negatively biased and applying positive bias on gate G1 the device operates as a pnpn thyristor, whereas by applying negative bias it operates as a pin diode [54].

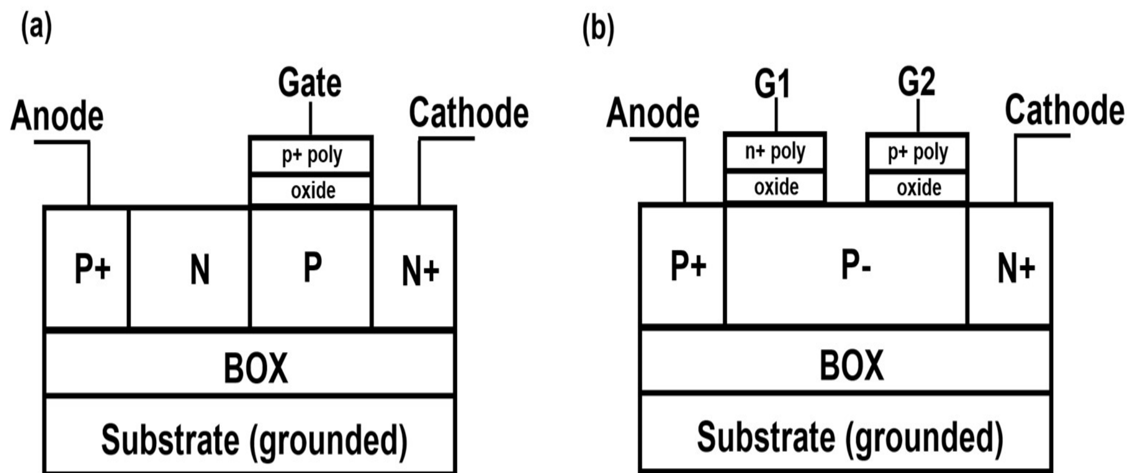



**Figure 6.1 Schematic diagrams of the TCCT (a) and FED (b) structures. The FED can be made to behave as an “induced” pnpn thyristor under suitable bias conditions. The main difference between the two structures is that all the p-n junctions are built-in in the TCCT, but only one (cathode) is built-in in the FED, the other two being bias-induced.**

A detailed investigation of the TRAM operation and design recently ([43-48]) concluded that “holes in the p-base under the gate represent the physical parameter determining the memory state of the cell” [47]: accumulation of holes for state “1”,

depletion of holes for state “0”. The emphasis of these papers ([43-48]) was mainly on the process of the so called “dynamic sensing”. Thus the above conclusion was actually not based on studying the carrier profiles in the memory HOLD (i.e. store) state. Instead, it was largely reached on the basis of phenomenological arguments, and although seemingly consisted with the operation of the device, this conclusion will be shown to be incorrect. The operation of the FED-RAM is very similar to that of TRAM, and it was also erroneously implied earlier [54, 61-65] that the memory mechanism is accumulation (for “1”) or depletion (for “0”) of holes in the p-base, under the G2 gate. The purpose is therefore to identify the real nature of this mechanism with the help of numerical simulations of the operation of the TRAM and the FED memory cells and provide the basis for optimizing their design

## 6.2 Results and Discussion

A complete timing diagram of the TRAM cell was simulated (Figure 6.2), making sure that exactly the same (physical and geometrical) device parameter values and gate voltage ($V_G$) and anode voltage ($V_A$) waveforms were used as those in [46,47]. The SOI film thickness was 30 nm, the BOX thickness 200 nm, the gate oxide thickness 5 nm, the p-base doped at $10^{17}$ cm$^{-3}$, the n-base at $10^{19}$ cm$^{-3}$ and each base was 100 nm long.

The voltage waveforms used are as the following: hold (H0/H1) state: the anode voltage is kept at 0 V and the gate voltage at -2 V; write “0” (W0): the gate is pulsed to 2 V while the anode is kept on HOLD; write “1” (W1): the gate and anode are pulsed simultaneously, to 2 V and 1.1 V, respectively. Dynamic Sensing: starting from hold state, the anode is first pulsed to 1.2 V, then the gate is pulsed to 0 V after some delay

time, and the stored state is determined by sensing the current flowing into the anode terminal. In all operations the cathode is kept grounded. All the writing pulse widths are 50 μs each, and all the rise and fall times are 50 ns each. The rather long pulses during writing were chosen by the authors of [46, 47] in order to facilitate the comparison of their simulated and experimental results.

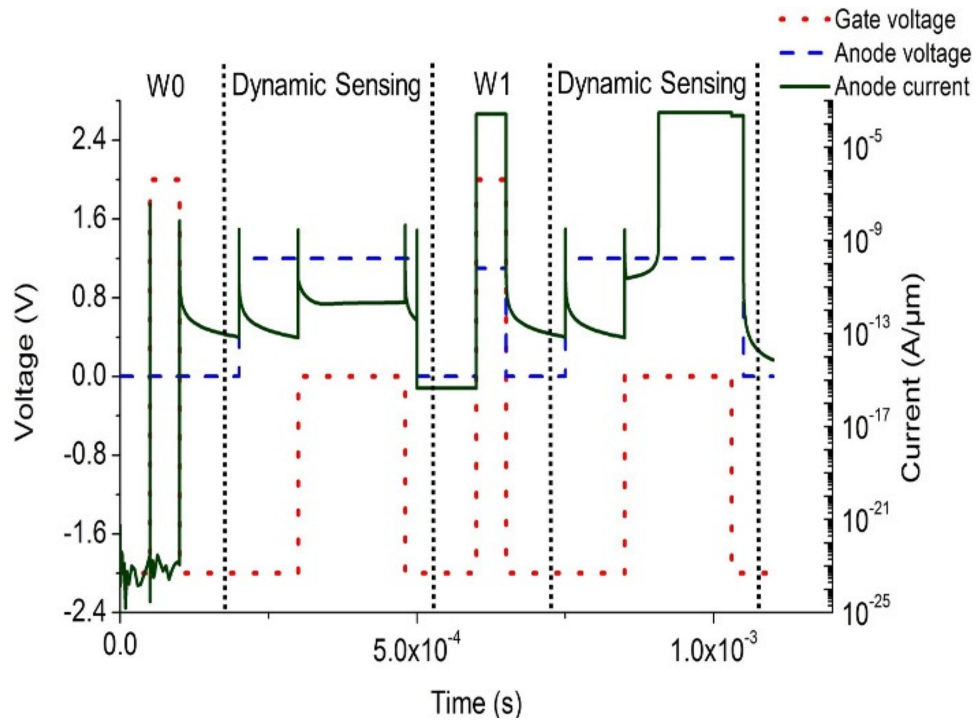



**Figure 6.2 TRAM writing and dynamic sensing diagram similar to that in [46, 47].**

Figure 6.3 shows the carrier profiles along this TRAM at a depth of 1 nm below the SOI film surface, immediately after the cell is put on hold (i.e. at times orders of magnitude shorter than the "0" retention time), following W1 and W0. From the carrier profiles in Figure 6.3, contrary to the above conclusion ([43-48]), accumulation of holes

is actually observed in the p-base, under the gate, for both memory states “1” (p ~$4.2x10^{18}$ $cm^{-3}$) and “0” (~$3.4x10^{17}$ $cm^{-3}$). This means that the physical memory mechanism cannot be the accumulation or depletion of holes in the base, under the gate, as claimed in [43-48].

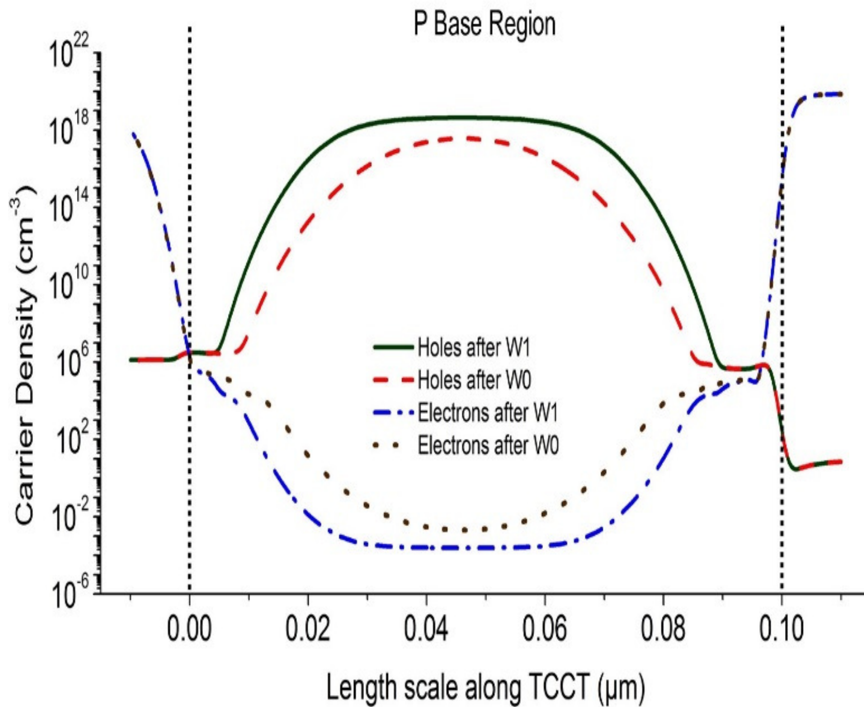



**Figure 6.3 TRAM carrier density profiles at a depth of 1nm with the cell on HOLD (i.e., store), immediately after WRITE “1” (W1) and after WRITE “0” (W0). Accumulation of holes is observed in the p-base under the gate for both states.**

It is also observed from these carrier profiles that what differentiates the two states is instead the presence (“0”) or absence (“1”) of deeply-depleted regions within the TRAM structure, associated with the two p-n junctions on the sides of the p-base. Under H1 these depletion regions are at equilibrium and state “1” is retained until power-down.

Under H0 they are deeply-depleted, and “0” can only be retained until transient carrier generation [59], [66] within these regions restores equilibrium.

The storage mechanism of the T-RAM cell can also be described by comparing the gate capacitance (Cg) to the junction capacitances on the sides of the p-base shown in Figure 6.4

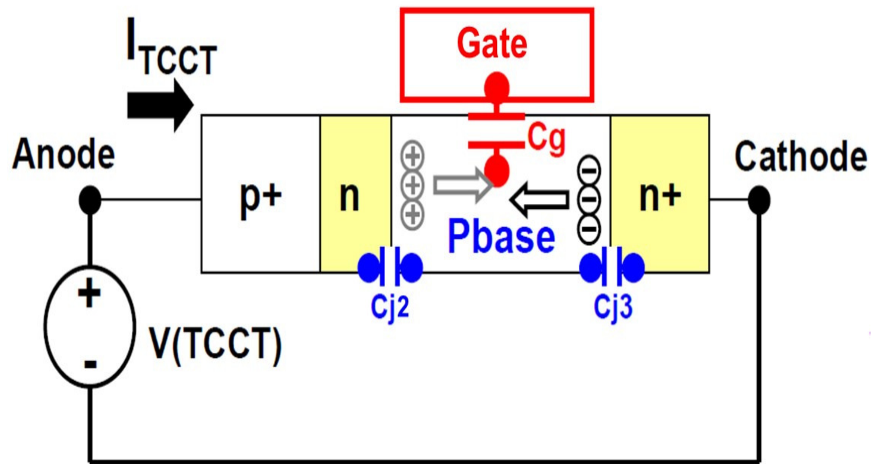



**Figure 6.4 Illustration of gate capacitance and the junction capacitances of the P-base in the T-RAM [67]**

The gate capacitance (Cg) and the junction capacitances ($Cj_2$, $Cj_3$) are defined as:

$$Cj_{1,2} = \frac{\varepsilon_s}{x_{d1,2}}$$

$$C_g \approx \frac{\varepsilon_{ox}}{t_{gox}}$$

where $x_d$ is the junction depletion region width, $t_{gox}$ is the gate oxide thickness, $\varepsilon_s$ and $\varepsilon_{ox}$ are the permittivity for the silicon and the oxide respectively.

If $(C_{j2} + C_{j3}) < C_g$, then data “0” is stored the cell, if $\left(C_{j2} + C_{j3}\right) > C_g$, then data “1” is stored.

This is consistent with previous explanation that defines the data stored in the cell based on the presence or absence of wide depletion regions on the p-base sides. From the above equations: the junction capacitance is inversely proportional to the depletion width, consequently, wide depletion regions (data “0”) corresponds to small junction capacitances that are less than the gate capacitance. The same logic applies when data “1” is stored; the decreased depletion widths leads to large junction capacitances (more than the gate capacitance).

Figure 6.5 shows a simulated timing diagram of the FED-DRAM, it should be noted that the time scale here is shorter and the pulse magnitudes are smaller than those in the TRAM timing diagram (Figure 6.2). The SOI film was slightly p-type ($10^{16}$ $cm^{-3}$) and 20 nm thick, the BOX thickness was 200 nm, and the gate oxide 2.5 nm thick. The gate lengths were 400 nm each and the length of the gap between the gates was 40 nm.

The waveforms for the FED-DRAM operation are as the following: hold (H0/H1): $V_{G2}$ = -1.2 V and $V_K$ = 1.2 V; write “0” (W0): $V_K$ = 1.2V and $V_{G2}$ pulsed to 1.2V (starting from the hold state); write “1” (W1): $V_K$ pulsed to 0 V and $V_{G2}$ pulsed to 1.2 V (starting from the hold state); read “1”/read “0” (R0/R1): $V_{G2}$ = -1.2 V, $V_K$ pulsed to 0 V (starting from the hold state), and sense anode current ($I_A$). In all operations $V_A$ and $V_{G1}$ are fixed at 1.2 V. $V_{G1}$ and $V_{G2}$ are the gate voltages, $V_A$ and $I_A$ are the anode voltage and current, and $V_K$ is the cathode voltage. An asymmetrical $V_{G2}$ pulse is used for

W1 (width = 4 ns, rise time = 1 ns, fall time = 4 ns) whereas a symmetrical pulse is used for W0 (width = 3 ns, rise time = fall time = 1 ns).

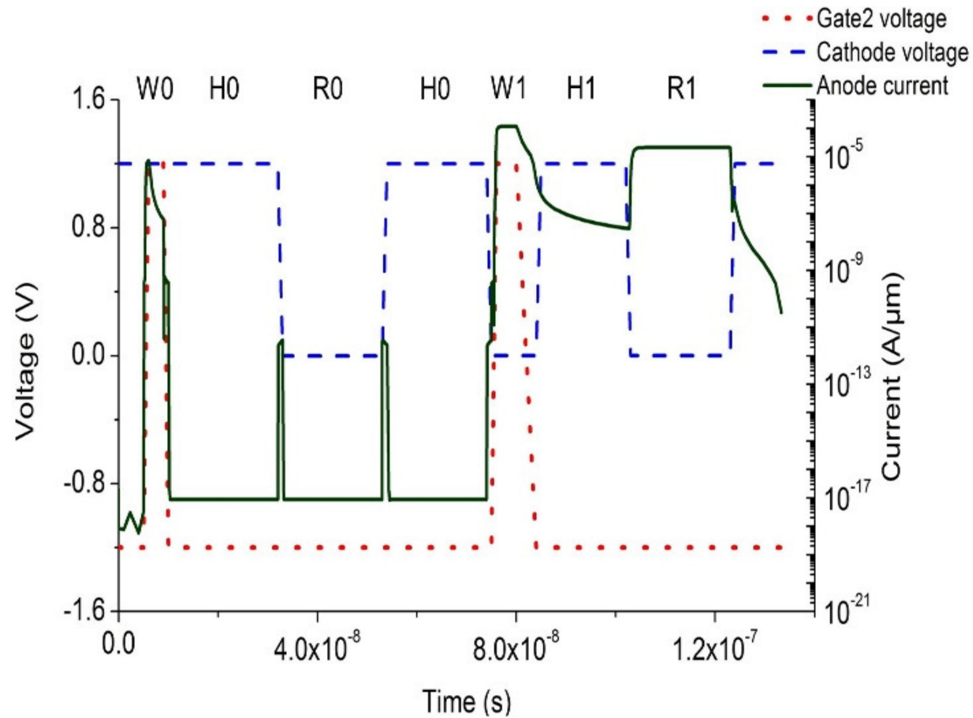



**Figure 6.5 FED-DRAM timing diagram similar to that in [54].**

Figure 6.6 shows the carrier profiles along this FED-RAM at a depth of 1 nm below the SOI film surface, immediately after the cell is put on the hold state, i.e. at times orders of magnitude shorter than the "0" retention time, following W1 and W0. The same conclusion for the nature of the memory mechanism as for the TRAM, can be drawn about the FED-RAM cell from these carrier profiles. It is clear that accumulation of holes is observed in the p-base under the gate for both memory states "1" (p ~$3\times10^{19}$ $cm^{-3}$) and "0" (~$10^{19}$ $cm^{-3}$) and what differentiates the states (and thus constitutes the physical

memory mechanism) is the presence ("0") or absence ("1") of deeply depleted regions within the FED-DRAM structure, associated with the induced p-n junction (left) and the built-in cathode p-n junction (right), on the sides of the p-base under gate G2.

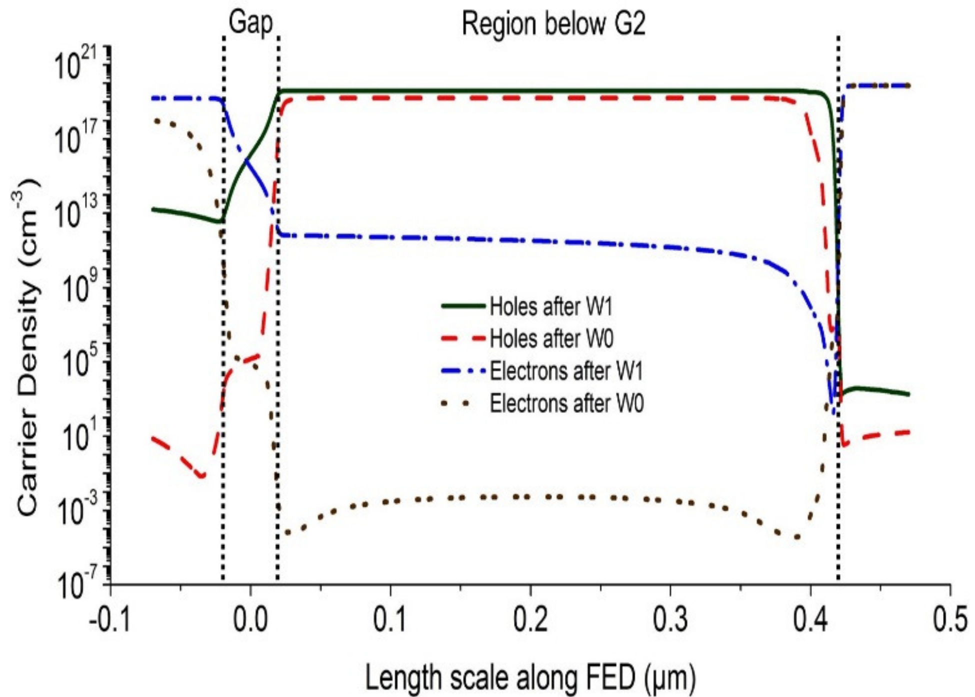



**Figure 6.6 FED-RAM carrier density profiles at a depth of 1nm immediately after WRITE "1" (W1) and after WRITE "0" (W0). Accumulation of holes is observed in the p-base under gate G2 for both states.**

This is different from the conventional Capacitor-Less One-Transistor DRAM (1T-DRAM) cell [18], [57] were the data is indeed stored by accumulation ("1") or depletion ("0") of holes. Just like the TRAM and the FED-DRAM cells, the 1T-DRAM cell is also a floating body cell (FBC), and what actually differentiates them is the anode

p-n junction, which is part of the structure of the former two cells but not of the 1T-DRAM cell.

To understand how this important structural difference impacts the memory mechanism and explain the presence of high hole-densities for both states “1” and “0” in the p-base of the TRAM and FED-RAM cells, we take a closer look at the part of the TRAM timing diagram in Figure 6.2 that corresponds to the W0 operation. It is observed that during this time a positive $I_A$ current is flowing from the anode to the cathode through the TRAM structure, both during the falling edge of the gate pulse and immediately afterwards for a brief time. Figure 6.7 shows the simulated hole- and electron-current components of this current more clearly, where it is seen that the electron-current component is much smaller, and that the hole-current component is almost constant during the falling edge of the gate pulse and then gradually decays within about 500 ns.

This current transient results from the dynamic forward biasing of the anode, through capacitive coupling by the falling edge of the gate pulse applied during the W0 operation. During this transient, many of the holes injected from the p-side to the n-side of the anode reach the reverse biased (by capacitive coupling) p-base/n-base p-n junction and, as in the collector of a BJT, they reach the TCCT p-base where they accumulate. This is the origin of the accumulated holes in the p-base following the W0 operation.

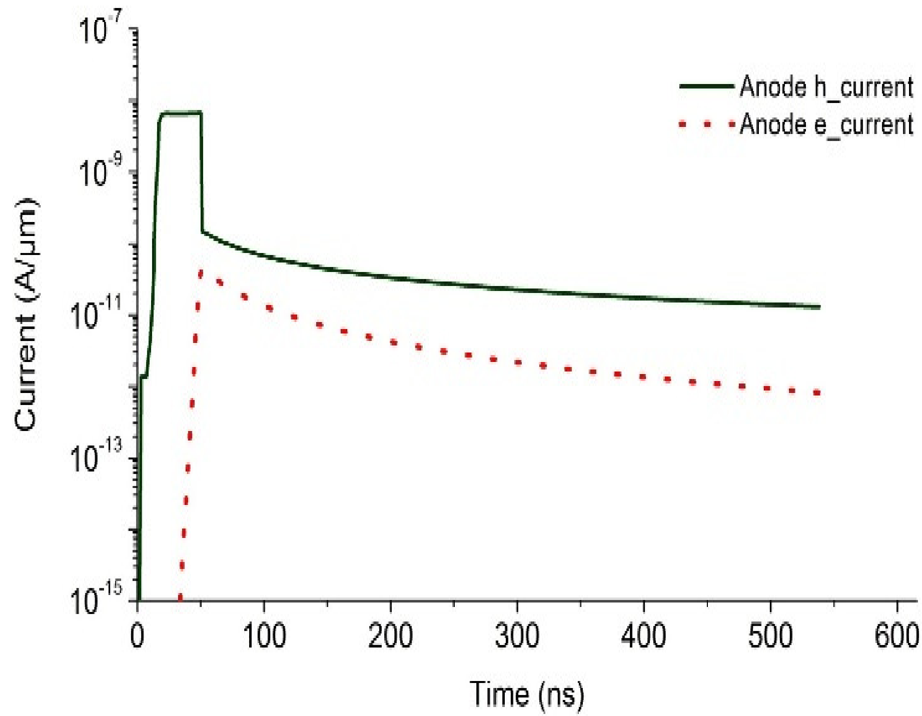



**Figure 6.7 Hole- and electron- currents flowing from the anode to cathode through the TCCT structure during and immediately after the falling edge of the W0 gate pulse.**

## 6.3 Conclusion

The physical memory (i.e., store) mechanism of the TRAM and FED-RAM cells is found to be the presence ("0") or absence ("1") of deeply-depleted regions within the TRAM structure associated with the p-n junctions on the sides of the p-base, and not the accumulation or depletion of holes in the p-base as previously believed. These deeply-depleted regions are formed during the W0 operation, by the dynamic reverse bias applied to the p-n junctions on the sides of the p-base by the falling edge of the W0 gate pulse, and they then gradually return to equilibrium over time ("0" retention time). This new understanding of the dynamic TRAM/FED-RAM memory mechanism should result

in better cell design, and hopefully their adoption by the semiconductor memory industry and their commercialization.

# CHAPTER 7 SUMMARY

## 7.1 Conclusions

In this dissertation, with the help of TCAD device simulation, we have utilized the field effect diode as a non-volatile memory cell based on the thyristor "mode of operation" of the FED. We also provide an alternative explanation to the physical storage mechanism of the thyristor based memories. The most important conclusions of this work can be summarized as follows:

1. The field effect structure and its bias condition to operate as a thyristor have been investigated. Also, the effect of device physical parameters and the gates bias amplitude on the break down characteristics of the FED were studied. $V_{FB}$ is strongly dependent on $V_{G1}$ which provides flexibility in modulating $V_{FB}$ of the thyristor without the need to change the physical parameters. From the other hand, $V_{FB}$ depends only very weakly on the gap length. Hence, this gap can be kept as small as possible.
2. A two element SRAM memory cell with the FED as the storage unit was introduced. The proposed memory cell is similar to the TCCT based memory cell. However, the FED based cell is easier to fabricate and more control is granted over the induced N and P regions in the FED by adjusting the gates

voltages. Also multiple holding schemes and writing method were presented and compared.

3. It should be possible to address the disturb control problem for the FED SRAM memory arrays using the techniques suggested by Roy et al. [55]; the capacitive coupling between the adjacent bit lines can be overcome by using the “Shield” technique. Also, for the cells sharing the same word lines; the non-selective writing issue can be avoided by applying a “pre-read” operation.
4. The FED was exploited as a DRAM memory cell with excellent characteristics such as non-destructive read, high speed read and write operations, and High 0/1 current margin.
5. We re-examined the recent interpretation of the physical storage mechanism of the thyristor based memories and provided an alternative description of the storage mechanism based on studying the carrier profiles in the memories structures. It was found that the Data storage is defined by the presence (“0”) or absence (“1”) of deeply depleted regions within the TRAM structure, associated with the two p-n junctions on the sides of the p-base.

## 7.2 Future Work

There are a few areas that need further investigations and improvements in our Research. However, two important issues need to be addressed in the near future research on the FED based memory cells: the disturb control in the memory array and the effect of FED scaling on the memory operation.

So far, the FED DRAM operation has been demonstrated on a single cell only. However, any practical application of the FED DRAM requires successful array operation, with cells connected together. The operation on a selected cell should not cause the failure or disturbance of other cells sharing the same signal lines [64]. Consequently, more efforts are needed to study the disturb effects in the FED based memories as the floating body cells generally face serious challenges in achieving robust disturb control when used in a memory array.

The disturbance caused by the write operation in the FED memory is mainly due to the gates pulses, while the read disturb is due to the cathode pluses. Read disturb has lower effects on the memory cells content and it should be possible to address it using the shielding technique discussed previously. On the other hand, write disturb is more destructive: cells that share the same gate line with the target cell get written non-selectively during performing write operation on the target cell.

To solve the write disturb problem, the bias magnitudes of the cell electrodes should be revised and investigated. Special care should be given to the bias condition during the stand-by state of the cell and shmoo plots for the cathode and the gates lines, similar to those discussed in [34], should obtained. This analysis should be accompanied with applying the "dynamic read" concept [37, 43-48]. Dynamic read includes pulsing the gates during the read operation (gate assisted turn on process); if the data stored in the cell is "1", then the gate pulse will be enough to turn the thyristor on. Otherwise, the thyristor will stay in the OFF state, i.e., data "0" is stored in the cell. Performing the read

operation “dynamically” should help relaxing the pulse magnitudes required during the write operations and hopefully will help in solving disturbance problems.

Fairly relaxed structure dimensions and device parameters were selected for proof of concept purpose. Although our previous results [50, 52] suggest that it should be possible to design FED memory cells of superior scalability, more research is needed to study the effect of scaling on the memory characteristic of the FED. This is should be done by running the simulations of memory operations on devices with scaled feature size and with more suitable device parameters, especially the doping profiles, in an effort to improve the performance.

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