5-2017

# Design and Simulation a Novel Three-Phase, Five-Level Inverter Topology

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# DESIGN AND SIMULATION

# A NOVEL THREE-PHASE, FIVE-LEVEL INVERTER TOPOLOGY

By

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A THESIS

Presented to the Faculty of

The Graduate College at the University of Nebraska

In Partial Fulfillment of Requirements

For the Degree of Master of Science

Major: Architectural Engineering

Under the Supervision of Professor Dale Tiller

Lincoln, Nebraska

May 2017

# DESIGN AND SIMULATION

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University of Nebraska, 2017

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There is a high integration of renewable energy sources in modern building electrical systems. The main components of these new systems are power electronics switches that inherit their foundations from signal amplifier technologies and then developed to drive high powers. Nowadays, the static converter can connect systems with different electrical characteristics. For instance, choppers connect two DC systems with different voltage levels, whereas inverters transform power from DC to AC with variable amplitude and frequency. Since multilevel inverters offer a better quality of the output waveforms than standard inverters, a novel three-phase, five-level inverter topology is proposed. The goal of this work is to conserve energy and enhance the electrical system quality when it is converted from DC to AC voltage by increasing the efficiency of inverter voltage output with a new proposed topology and proposed modulation technique. The main advantages of this novel topology are overall reduction in the number of power electronics components when compared with traditional designs; reduction in the total price of the inverter components; reduction in the total volume and weight; reduction in the total pre-calculated switching angles using the proposed modulation technique, and eliminating the maximum harmonics in the output waveform, while at the same time, minimizes the total harmonics distortion THD in the output.

# ACKNOWLEDGEMENTS

I would like to thank my advisors, Professor Mahmoud Alahmad, Professor Dale Tiller, and Professor Lamar Yang for their continuous helpful and inspiring feedback throughout the period of my MS studies. Also I would like to show my deepest gratitude and respect to my family, especially my parents, Mohamad and Nadiah Al Juheshi, the ones to whom I owe all success in my life and my brothers and sister.

My appreciation is also extended to all colleagues in the Architectural Engineering especially Amro and Ala'a for their help and their support. Finally, I give thanks to all the faculty and staff in the Architectural Engineering department who do a great job to make this program one of the best in the nation.

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# CHAPTER 1

# *INTRODUCTION*

## 1.1 General

This chapter presents the motivation for the research addressed in this thesis. The chapter also describes the main objectives of the research and the outline and structure of each chapter in the document.

## 1.2 Motivation

Converters, which are used to change direct current (DC) into alternative current (AC) or vice versa, for electric drive controls will continue to develop in the future. From the early stages, electric machines used to be controlled by mechanical converters. At that time the best known and most widespread mechanical converters were the Ward Leonard drive system and, later, the rotary converters [1]. In 1902, the first electrical converter, a mercury rectifier, was invented and was widely used. It was made obsolete by a semiconductor converter in the 1960s [2]. As the technological progress of semiconductor devices improved, the voltage and current ranges of applications grew rapidly [3-4]. Today, four types of semiconductor devices are available for use in medium or high voltage (MV or HV) industrial applications: 1) gate turn-off (GTO) thyristor; 2) integrated gate commutated thyristor (IGCT); 3) insulated gate bipolar transistor in press-pack (PP-IGBT) or 4) module (IGBT-Module). Semiconductor devices have a variety of voltage and current range, such as PP-IGBTs by Westcode Toshiba reach 4.5 kV / 4.8 kA, and Mitsubishi produces GTO thyristors on 6 kV / 6 kA. IGBT-Modules manufactured by ABB reached

6.5 kV / 1.5 kA and 4.5 kV / 2.4 kA.Tthe same devices developed by Infineon and Hitachi are on 3.3 kV / 3 kA and 1.7 kV/ 7.2 kA. IGCTs by ABB exceed the border of 6 kV / 3.2 kA [5]. In addition, ABB manufactured a prototype of IGCT on 10 kV and 1 kA [6]. Unfortunately, the dynamic parameters, above all the switching frequency, do not reach the values of low voltage devices. Nevertheless, it can be generally said that the rapid development in the semiconductor industry produces devices for higher and higher voltage and current area with better and better dynamic properties.

Despite the progress, the parameters of all these devices are still not high enough for use in “classical” three-phase inverters with six power semiconductor devices for the MV or HV applications [7], e.g. for variable speed drives (the electric traction, winding engines, pumps for long-distance transport of gas and liquid mediums etc.) [8-9] and for compensatory and filtration applications [10]. With the growth of non-linear loads such as cycloconverters, rectifiers, arc furnaces and asymmetrical loads, the active power filters are widely used due to the clearing of high disturbances in the power supply system [11-13]. Classical semiconductor inverters switch on high frequency between the positive and the negative pole and have high conduction losses. Both the voltage step between two poles and the higher switching frequency exert influence over the quality of an output voltage waveform. If the required output voltage is higher than the rate value of power electronic devices available on market, then some method of voltage reduction per device must be used. This method has been widely used for more than 35 years, e.g. in the first light high voltage direct current (HVDC) transmission with input DC voltage of both inverters is ±10 kV, i.e. 20 kV between levels and output RMS line-to-line voltage of inverter is 10 kV where in each arm there are 22 in series connected IGBTs [14]. The IGBTs were selected

according to small deviation of parameters. This selection allows a uniform voltage distribution between the transistors. The advantage of this method is simple control strategy; the disadvantages are the selection of transistors and the high voltage changes caused by the switching of one arm. In addition, to connect IGBTs in series is possible only with auxiliary circuits [15]. For these reasons, this method is not practically used.

Since the output power of micro-sources (photovoltaic, wind energy etc.) is dependent on environmental conditions, such as solar irradiance and wind, it is necessary to use some specific control strategies with an energy storage system (battery, super-capacitor etc.) in order to compensate for the fluctuations. One traditional way is to use different converters to integrate the microsources, energy storage and different types of loads into a common DC bus [16-17], which has some problems such as:

- Since there are many power electronics converters in the system, the harmonics components will be very high, which increases the cost and size of the harmonics filter;
- If the voltage level is very high, the switching stress of the power electronic device will increase;
- The efficiency will be low due to the power losses in different converters.

The modern solution for these problems is to feed the electric drives from multilevel converters (MCs), mostly from multilevel inverters (MIs). MIs provide the possibility to eliminate series connected semiconductor devices in the MV and HV applications which is considered the main problem.

Using MI in these applications resolves not only the problem of voltage equable distribution across semiconductor switches but also makes it possible to [18-19]:

- Eliminate the need of bulky and expensive step-down transformers;
- Reduce the connection cables cross-sections;
- Improve the harmonic content of output voltage and phase current consequently to output quantity waveforms, resulting in better electromagnetic compatibility;
- Lower dv/dt stress of semiconductor switches, reducing the costs of output filters;
- Operate in medium to high power applications where semiconductor switches are not able to operate at high switching frequencies;
- Minimize switching frequency, increasing their efficiency (>98%);
- Operate with high switching frequencies and operation using pulse-width modulation technique PWM.

## 1.3 Thesis Objective

The integration of renewable energy sources to the electricity grid has become interesting and increasingly pertinent to research and application. In order to maintain or improve power supply reliability and quality new strategies for the operation and management of the electrical grid would be useful. To serve that purpose, this thesis proposes a novel three-phase, five-level multilevel inverter with a new proposed modulation technique. The focus of this research will be on the advantages of this proposed topology compared to traditional designs with the number of power electronics components. The advantages of the proposed modulation technique are the reduction in the total pre-calculated switching angles. The proposed design will eliminate the total harmonics distortion (THD) in the inverter's output.

## 1.4 Thesis Outline

The literature view provides the background to the research and the topic. After the literature review, the topology is introduced and proposed along with the new proposed modulation technique. Next, simulation results are presented for different cases to demonstrate the advantages of the proposed topology and modulation technique; portions of this work have already been published [20]. A brief outline of the thesis is given below.

1. Chapter 2 provides a general overview of the inverter and multilevel inverter concepts and their topologies;
2. Chapter 3 offers a general overview of the modulation techniques that will be used along with MIs;
3. Chapter 4 introduces the proposed three-phase five-levels topology, and the operation of this topology;
4. Chapter 5 explains the modulation technique of the pre-calculated switching angles in the interval [0 $\pi/3$];
5. Chapter 6 discusses the simulation results of the new proposed topology with different cases as well as with the traditional modulation technique;
6. Chapter 6 introduces future work and offers a summary of what has been achieved with this research.

# CHAPTER 2

# *INVERTER TOPOLOGIES*

## 2.1 General

Increasing demand for electricity led to the fast-growing availability of renewable energy sources, such as solar and wind energy, seen today. While the energy conversion process of these devices produces little to no pollution, the power generated is often intermittent and unreliable.

Inverters are commonly a part of renewable energy systems. An inverter is an electronic device that changes direct current (DC) to alternative current (AC) [21]. There are three types of inverters based on type of output waveform: square wave, modified-sine wave, and pure sine wave. A square wave is non-sinusoidal waveform, most typically seen in electronics and signal processing. Square wave has two levels (positive and negative) and alternates regularly between these two levels. The output of a modified sine wave inverter is similar to a square wave output except that it has one more level (i.e., before switching positive or negative the output goes to zero volts). Most AC motors work with the modified-sine wave inverter, due to its simple design. The main problem with this inverter is that it does not create a pure sine wave, which creates unwanted noise during operation.

A pure or true sine wave inverter changes or converts the DC supply into a near perfect sine wave. The sine wave has minimal harmonic distortion, resulting in a very clean energy supply. This makes it suitable for electronic systems such as computers, motors and microwave ovens and other sensitive equipment without causing problems like sound. Main battery chargers also run better on pure sine wave converters.

Ideally, the output waveforms of an inverter should be sinusoidal. This can be seen in Figure 2.1, which displays how a modified sine wave tries to emulate the sine wave itself. The waveform is easy to produce because it is just the product of switching between three values at set frequencies, thereby leaving out the more complicated circuitry needed for a pure sine wave. The modified sine wave inverter provides a cheap and easy solution to powering devices that need AC power. It does have some drawbacks as not all devices work properly on a modified sine wave, for example, computers and medical equipment must be run off of a pure sine wave power source [22].

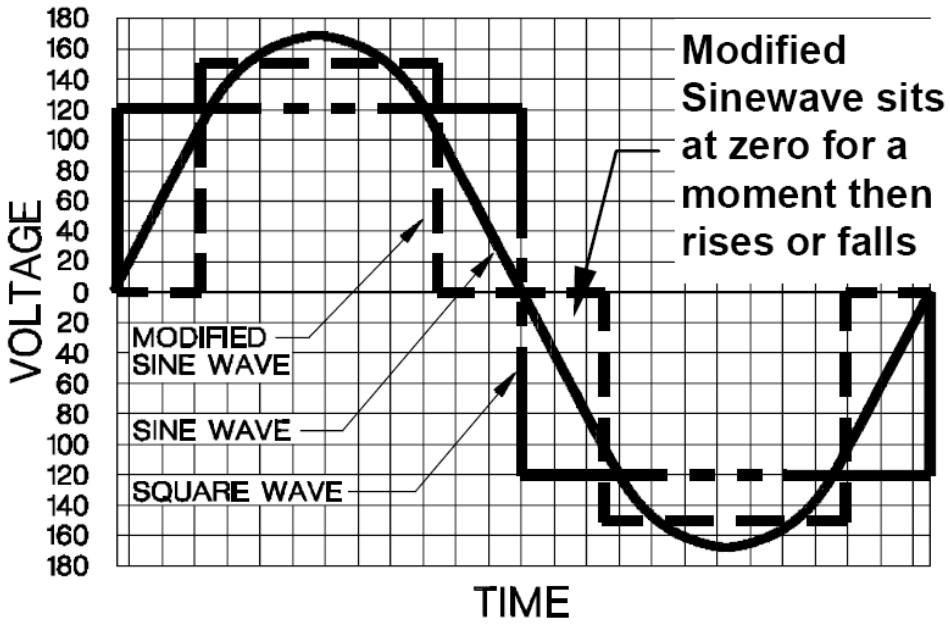



**Figure 2.1 Square, Modified, and Pure Sine Wave [22]**

Two-level inverters, as seen in Figure 2.2 where a) shows the topology design and b) shows the voltage output of this inverter, are mostly used today to generate an AC voltage from an DC voltage. The two-level inverter can only create two different output voltages for the

load, $V_{dc}/2$ or $-V_{dc}/2$ (when the inverter is fed with $V_{dc}$) To build up an AC output voltage, these two voltages are usually switched using the traditional PWM technique (PWM will be discussed in more details in Chapter 3) as shown in Figure 2.3. Though this method is effective, it creates harmonic distortions in the output voltage, EMI and high $d_v/d_t$ (compared to multilevel inverters) [23]. While this may not always be a problem, some applications may need a low distortion in the output voltage.

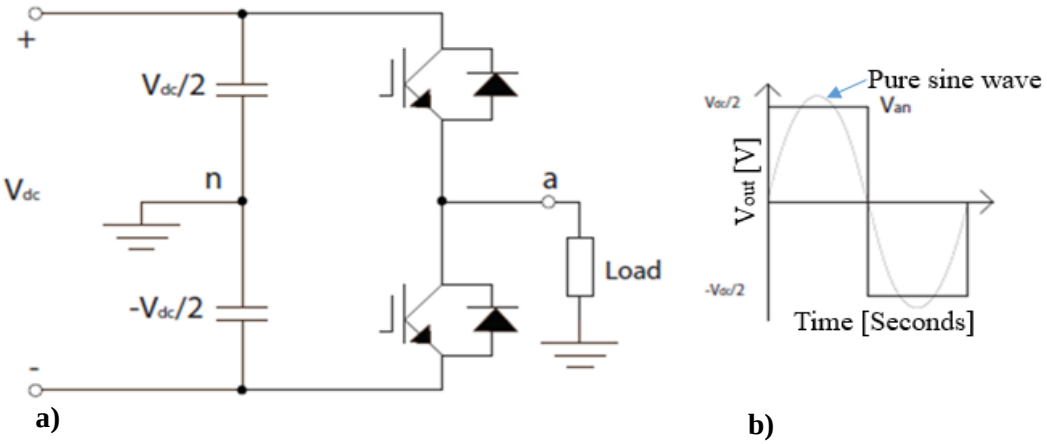



**Figure 2.2 One phase of a two-level inverter: a) the topology, b) the output voltage [23]**

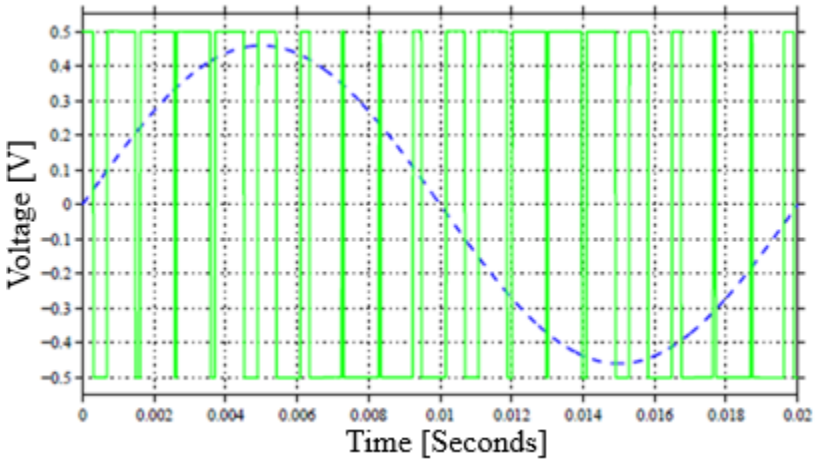



**Figure 2.3 PWM voltage output, reference wave in dashed blue**

## 2.2 Multilevel Inverter (MI)

Recently, renewable energy systems have become a major part of modern power systems. The two major renewable energy sources are wind and solar. In grid-connected applications, a power converter is needed between the renewable energy source and the main grid in order to improve the quality of output renewable energy source's power in terms of voltage and frequency. MI technologies are often employed to produce higher quality power, improve electromagnetic compatibility, lower switching losses, increase the voltage capability, and eliminate the need for a transformer, thereby reducing costs [24-26]. MI technologies were first introduced to the field of electronics in 1975 [27]. The essence of the MI is to divide the output phase voltage range (bordered by two levels – upper and lower) into several inner levels with an equal voltage distance from each level. The magnitude of this distance determines the permitted voltage stress of the semiconductor devices used. If this distance gets wider, the voltage stress increases across the first device and decreases across the second one. When this deviation becomes excessively large, the device can be endangered and the core of the MI gets lost. Ensuring correct and constant voltage levels, known as voltage balancing, is one of the most important control tasks.

The first and the simplest MIs were not based on the semiconductor technique but rather on a magnetic coupling. The waveform of the output multilevel voltage is obtained by adding several rectangle voltages produced by classical inverters under square-wave control. Their rectangle phase shifted output voltages supplied the coupling transformers and the voltages summed on the secondary sides of these transformers were added into a staircase multilevel waveform. Generally, MIs are classified as one of three main types

[28-29]: Cascaded H-Bridge inverters, Neutral-Point-Clamped (NPC) inverters, and Flying Capacitor inverters. These will be discussed further in the following subsections.

### 2.2.1 Multilevel Inverters Concept

This section will describe the general principle of the MI. Figure 2.4 demonstrates how ML work. The two level inverter with two voltage output “0” and “E” levels is shown in Figure 2.4a. Considering Figure 2.4b, the voltage output of a three level inverter leg can assume three vales “0”, “E” or “2E”. In Figure 2.4c, an n-level inverter leg is presented with “n” voltage output. In particular, it is considered that the DC voltage sources have the same value and are series connected. In practice with non-ideal components there are no such limits, then the voltage levels can be different [29].

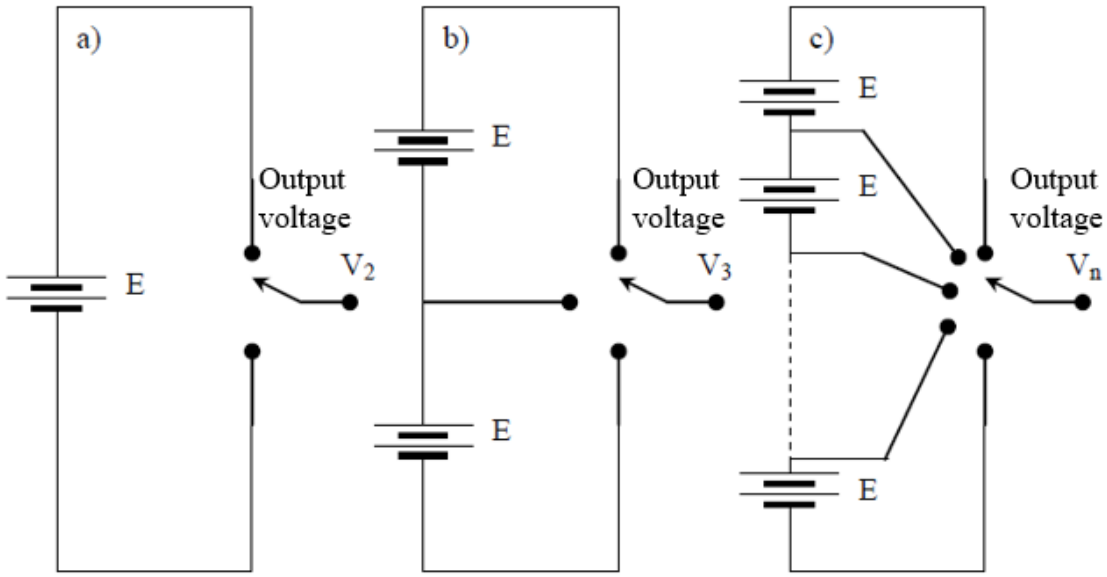



**Figure 2.4: a) two-level inverter, b) three-level inverter, c) n-level inverter [29]**

The concept of MI does not depend on just two levels of voltage to create an AC signal. Instead several voltage levels are added to each other to create a smoother stepped waveform with lower $d_v/d_t$ and lower harmonic distortions as number of steps increases, as shown in Figure 2.5 where a) a three-level waveform, b) a five-level waveform, and c) a seven-level waveform. With more voltage levels in the inverter, the waveform it creates becomes smoother. However, with many levels, the design becomes more complicated, with more components and a more complicated controller for the inverter [30]. This introduces a further possibility which can be useful in multiphase inverters, as it will be shown later when discussing the different types of MIs among with their operations and the advantages/disadvantages of each topology and focusing on the five-level topologies to compare them with the proposed topology.

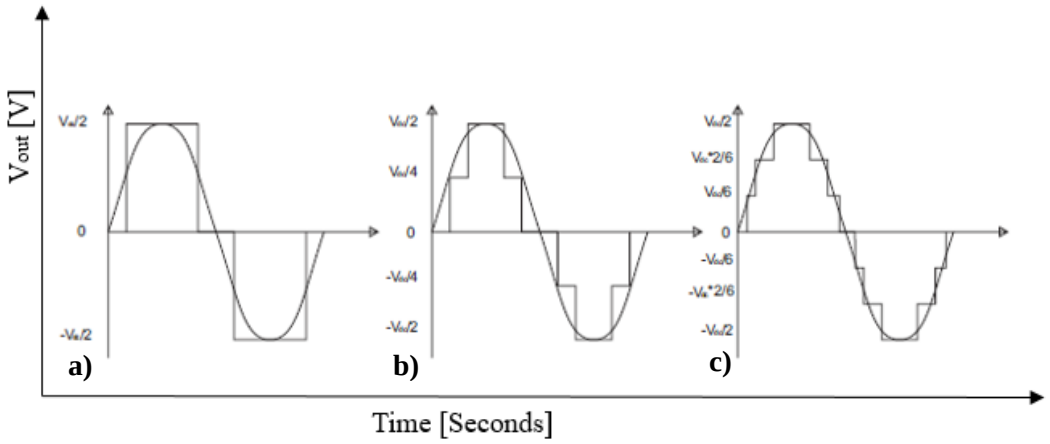



**Figure 2.5 Multilevel waveform switched at fundamental frequency: a) a three-level waveform, b) a five-level waveform, c) a seven-level waveform [30]**

### 2.2.2 Cascaded H-Bridge Multilevel Inverter (CHB)

The first MIs based on semiconductors were described and constructed by Baker and Bannister (1975). It was a cascaded topology which is a serial connection of one-phase

inverter. The Cascaded H-Bridge (CHB) MI is based on the series connection of single phase H-Bridge inverters with separate DC sources [31]. The following two subsections will show the operation of the Cascaded H-Bridge for three and five level inverter and discuss the features of this topology.

### 2.2.2.1 Cascaded H-Bridge Operation

The output phase voltage of this topology is synthesized by the addition of the voltages that are generated by different modules. A basic scheme of a three-phase five-level Cascaded H-Bridge multilevel inverter is shown in Figure 2.6. Each leg is composed of one phase full bridge that is connected in chain [32]. Each bridge consists of four switches with their diodes $S_1$, $S_2$, $S_3$, $S_4$ and one independent voltage source "$V_d$". The voltage sources can be batteries, fuel cells or solar. All the voltage sources have an identical voltage. The output voltage of each bridge can obtain values "$-V_d$", "0" or "$+V_d$" where ($V_d = E$) [33-34].

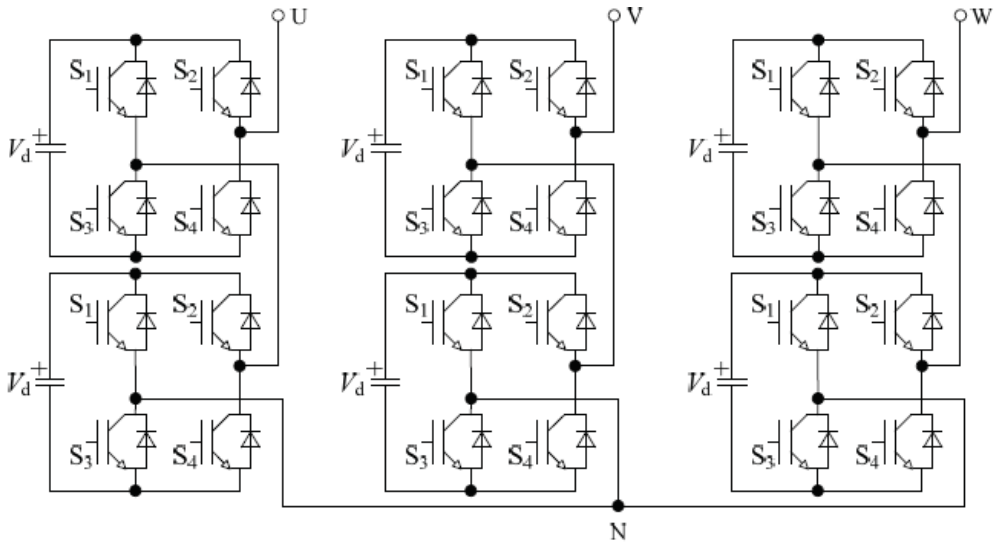



**Figure 2.6 The scheme of a three-phase five-level cascaded H-Bridge multilevel inverter [32]**

Figure 2.7 shows a three-level Cascaded H-Bridge leg that a) depicts the topology design, and b) depicts the output voltage waveform. Figure 2.8 shows a five-level Cascaded H-Bridge leg (one-phase) that a) depicts the topology design and b) depicts the output voltage waveform. The three-level inverter analysis is the simplest. It is well known that H-Bridge inverter can be modulated with tow-level or three-level output. In this kind of multilevel inverter, all the possible cell output levels are exploited. Some switch configurations are damaging for the converter and must be avoided; for instance, the switches $S_1$ and $S_3$ or $S_2$ and $S_4$ are not allowed to be turned on at the same time because this situation causes a short-circuit of the source. Table 2.1 (P.15) shows the relationship between the allowed switch configurations and associate output for the three-level Cascaded H-Bridge inverter [35].

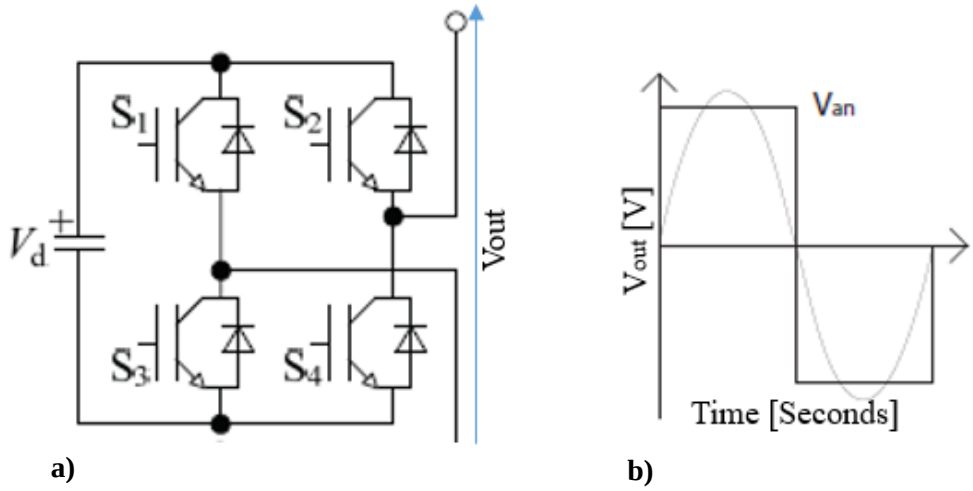



**Figure 2.7 The three-level cascaded H-Bridge multilevel inverter; a) topology, b) the output voltage waveform [35]**

**Table 2.1 Three-level Cascaded H-Bridge leg relationships between configurations and output voltages**

| $S_1$ | $S_2$ | $S_3$ | $S_4$ | $V_{out}$ |
|---|---|---|---|---|
| ON | OFF | OFF | ON | $V_d$ |
| ON | ON | OFF | OFF | 0 |
| OFF | OFF | ON | ON | 0 |
| OFF | ON | ON | OFF | $-V_d$ |

In order to increase the number of levels, more bridges have to be cascaded. In addition, high and low couples of switching can be defined with respect to the voltage output direction. Considering Figure 2.8 with two bridges, the high output of one bridge is shortcut to the low output of another one, realizing a cascade connection between two bridges. Each bridge in the cascade adds two more levels to the output waveform, as shown in Table 2.2, the switches state for a one-phase, five-level [35].

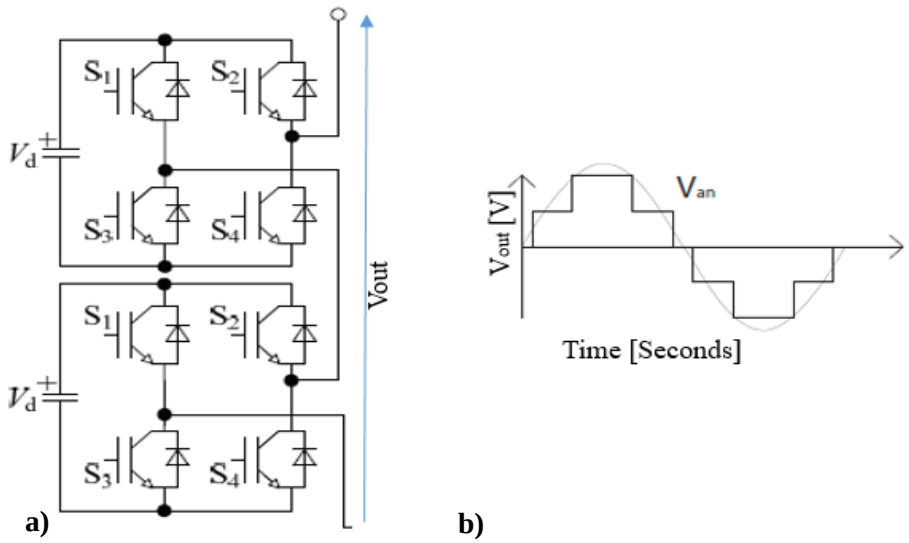



**Figure 2.8 The five-level Cascaded H-Bridge multilevel inverter: a) topology, b) the output voltage waveform [35]**

**Table 2.2 Five-level Cascaded H-Bridge leg relationships between configurations and output voltages**

| The Upper cell | | | | The lower cell | | | | $V_{out}$ |
|---|---|---|---|---|---|---|---|---|
| $S_1$ | $S_2$ | $S_3$ | $S_4$ | $S_1$ | $S_2$ | $S_3$ | $S_4$ | |
| ON | OFF | OFF | ON | ON | OFF | OFF | ON | $2V_d$ |
| ON | ON | OFF | OFF | ON | OFF | OFF | ON | $V_d$ |
| ON | OFF | OFF | ON | OFF | OFF | ON | ON | $V_d$ |
| ON | OFF | OFF | ON | ON | ON | OFF | OFF | $V_d$ |
| OFF | OFF | ON | ON | ON | OFF | OFF | ON | $V_d$ |
| ON | ON | OFF | OFF | ON | ON | OFF | OFF | 0 |
| ON | ON | OFF | OFF | OFF | OFF | ON | ON | 0 |
| ON | OFF | OFF | ON | OFF | ON | ON | OFF | 0 |
| OFF | ON | ON | OFF | ON | OFF | OFF | ON | 0 |
| OFF | OFF | ON | ON | ON | ON | OFF | OFF | 0 |
| OFF | OFF | ON | ON | OFF | OFF | ON | ON | 0 |
| OFF | ON | ON | OFF | ON | ON | OFF | OFF | $-V_d$ |
| OFF | OFF | ON | ON | OFF | ON | ON | OFF | $-V_d$ |
| OFF | ON | ON | OFF | OFF | OFF | ON | ON | $-V_d$ |
| ON | ON | OFF | OFF | OFF | ON | ON | OFF | $-V_d$ |
| OFF | ON | ON | OFF | OFF | ON | ON | OFF | $-2V_d$ |

Applying Kirchhoff's voltage law to the one-phase, five-level, the total output voltage "$V_{out}$" is the sum of the signal cell output voltages. Equation 2.1 is the general equation for a multilevel inverter composed of "n" bridges, where each bridge supplies an output voltage "$V_{out}$" [36].

$$V_{out} = \sum_{j}^{n} V_{out\ j} \qquad (2.1)$$

### 2.2.2.2 Cascaded H-Bridge Features

A Cascaded H-Bridge converter is a very modular solution, based on a widely commercialized product, with good availability, intrinsic reliability and relatively low cost [37].

The main disadvantage of this inverter type consists in requiring several separated sources that are not available in all applications. For instance, there are high costs in making insolated sources for induction motor drive systems because these require isolation transformers. At the same time, this disadvantage makes CHB inverters more suitable for photovoltaic or battery fed applications. Indeed, photovoltaic panels can easily be rearranged in several separated sources to feed Cascade H-Bridge bridges. A similar operation can even be done with battery banks [38].

Moreover, the separated sources can be substituted with capacitors when the inverter is used as an active filter. In such applications, the active power through the inverter is theoretically zero, so there is no need to have a power source. Anyway, the converter has its own losses and the capacitors have to supply a little active power that discharges them.

A simple control, sensing the voltage of each capacitor and exploiting either the intra-phase or joint-phase redundancies, can be applied to avoid this problem. In this way, the active power to feed the converter is absorbed from the net and the capacitors feed reactive power only [39].

There are other several application dependent ways to exploit intra-phase redundancy property of this inverter. As an example, consider a three-phase system and a vector modulation. The vector control can choose among the redundant configurations to find the one that has the fewest commutations.

While there are no limitations on the level of Diode-Clamped or Flying-Capacitor, which can be even or odd, cascade H-Bridge can have only odd numbers of levels; indeed, the first bridge gives three levels whereas the others always add two levels more.

### 2.2.3 Natural-Point-Clamped Multilevel Inverter (NPC)

Five years after the description and realization of the first CHB, Baker (1980) proposed a new topology, a Neutral-Point-Clamped multilevel inverter, namely a three-level and a five-level connection [40]. Just one year later (1981), an article was published concerning the implementation of pulse-width modulation for this topology and they introduced their first results of the three-level performance [41]. This topology was the first one that made it possible to produce an output voltage from only one DC source.

### 2.2.3.1 NPC Operation

In Figure 2.9, a three-level (a), and a five-level NPC topology (b) are shown. It is easy to extend the scheme to a generic n-level topology [42-43]. The DC bus voltage is split in two and four equal steps respectively by capacitor banks. In this way, no extra DC sources are needed with respect to the standard two-level inverter. The voltage between two switches is clamped through the diodes in the middle of the structure, called clamping diodes. Considering the five-level NPC multilevel inverter, it is possible to note that the number of diodes required to clamp the voltage changes point by point [44].

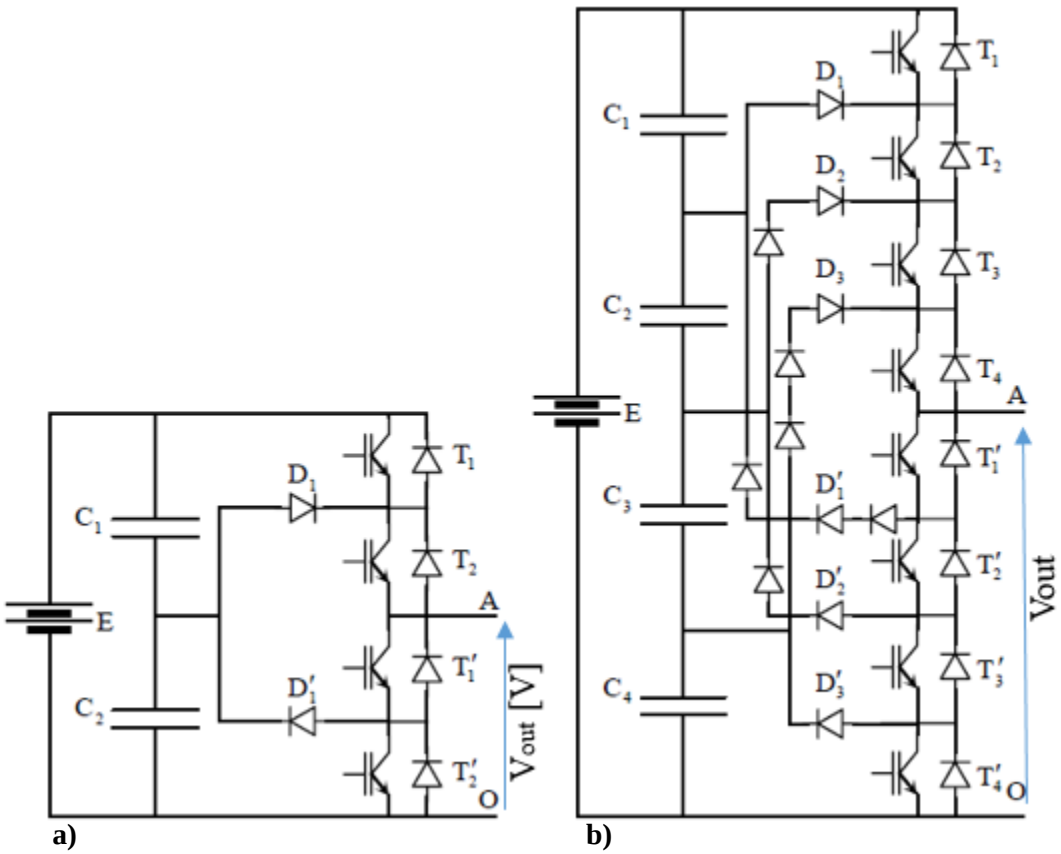



**Figure 2.9 NPC multilevel inverter: a) the three-level, b) the five-level [42-43]**

For instance, $D_1$ is composed of one diode, whereas $D_1'$ is a series of three diodes. This does not mean that the diode series connection is needed in the implementation, but it simply means that the reverse voltage drop caused by $D_1'$ is three times the backward voltage drop over $D_1$. In the final implementation either one diode with higher blocking capability or three diodes series connected can be used. Anyway, to better understand how a Diode-Clamped works, it is preferred to use series connected diodes; in this way, the reverse voltage drop of all the diodes is the same and is equal to the voltage fixed by a capacitor. For a generic n-level NPC the diode reverse voltage is given by (2.2) [45]:

$$V_r = \frac{E}{N-1} \qquad (2.2)$$

So, in three-level Diode-Clamped it is $V_r = \frac{E}{2}$ while in five-level it is $V_r = \frac{E}{4}$ . Furthermore, this voltage drop is also the reverse voltage each switch has to block. Increasing the voltage levels means a reduction of the stress over the components, considering the same DC bus voltage. Unfortunately, more levels mean more components. Increasing one level involves one capacitor, two switches, and two diodes. In fact, the number of clamping diodes used in a Diode-Clamped inverter is related to the number of level by the following expression (2.3) [46]:

$$N_{Diodes} = (n-1)\,(n-2) \qquad (2.3)$$

Focusing attention to the three-level leg, it is possible to find the relationship between the state of the switches and the output voltage $V_{out.}$ It is important to note that a right switch configuration must be used to avoid any kind of shortcut. So, it is simple to understand that all the switches cannot be simultaneously turned on. There are also other dangerous configurations, but they can be avoided by switching $T_1$ and $T'_1$ in a complementary way. The same has to happen for $T_2$ and $T'_{2.}$ Considering these conditions, there are only four

possible configurations that a one-phase three-level Diode-Clamped can assume, and these are shown in Table 2.3. Not all four configurations lead to a proper output voltage. When $T_1$ is on and $T_2$ is off, there is no defined path for the load current. It does not matter whether $T_2$ or $T'_1$ are not conducting, so the current flows throughout the free-willing diodes. The output voltage depends on the outcome of the configuration. As it is possible to see from Table 2.3, there are no intra-phase redundant states in three-level Diode-Clamped [47].

**Table 2.3 Three-level NPC leg relationships between configurations and output voltages**

| $T_1$ | $T_2$ | $T'_1$ | $T'_2$ | $V_{out}$ |
|---|---|---|---|---|
| ON | ON | OFF | OFF | E |
| OFF | ON | ON | OFF | E/2 |
| OFF | OFF | ON | ON | 0 |
| ON | OFF | OFF | ON | undefined |

Similarly, the five-level Diode-Clamped leg does not present redundant states and only five different configurations are allowed for the switches as shown in Table 2.4.

**Table 2.4 Five-level NPC leg relationships between configurations and output voltages**

| $T_1$ | $T_2$ | $T_3$ | $T_4$ | $T'_1$ | $T'_2$ | $T'_3$ | $T'_4$ | $V_{out}$ |
|---|---|---|---|---|---|---|---|---|
| ON | ON | ON | ON | OFF | OFF | OFF | OFF | E |
| OFF | ON | ON | ON | ON | OFF | OFF | OFF | 3E/4 |
| OFF | OFF | ON | ON | ON | ON | OFF | OFF | E/2 |
| OFF | OFF | OFF | ON | ON | ON | ON | OFF | E/4 |
| OFF | OFF | OFF | OFF | ON | ON | ON | ON | 0 |

### 2.2.3.2 NPC Features

NPC or Diode-Clamped inverters present some peculiarities which other multilevel topologies do not have. First of all, it is quite simple to control. Indeed, a simple extension of a traditional analog PWM control can directly gate the switches. The main control problems arise from digital controllers, which are suited for traditional two-level inverters and may not have outputs enough to drive all the semiconductors in the leg. But it is quite easy to implement a digital control system over a Diode-Clamped with commercial parts only, using some external hardware and a proper code [48].

Unfortunately, the reverse voltage drop changes among the components. The minimum reverse voltage drop is given by Equation (2.2) (p.20) and it is related to all the switches and some clamping diodes. For instance, considering the five-level inverter in Figure 2.9, the diode $D'_1$ is subjected to three times the minimum reverse voltage drop when $T'_2$, $T'_3$ and $T'_4$ are conducting. Considering the five-level leg, $T_1$ is conducting only when the required output voltage is “E”, while $T_4$ is always conducting but when the required voltage

is “0”. Furthermore, the current flowing throughout $T_4$ is always flowing even through T. So it is possible to assert that $T_4$ average current is smaller than $T_1$ average current. Choosing different switches with the same reverse voltage and similar dynamic performances, but with different rated currents, is quite difficult using commercial parts. Manufacturers prefer to use the same switch for every position even if they are not fully exploited somewhere in the leg. Diode-Clamped does not require insulated DC sources to create the voltage level, but exploits several capacitors to equally split a single DC source. This is a great advantage because it makes the circuitry topology suitable for use in all kinds of applications: to upgrade an existing system it is necessary only to design a proper Diode-Clamped, take out the old converter and use the new one in its place. Unfortunately, some capacitor voltage imbalance can occur, and the control must account for this. Single legs are not subject to them, because there are no intra-phase redundant states. On the other hands, multi-phase Diode-Clamped converter can balance the capacitors voltages using joint-phase redundant states. Furthermore, when this kind of inverter is connected in a back-to-back configuration, a proper synchronization between inverter and rectifier controls is sufficient to keep the capacitors balanced [48-50].

### 2.2.4 Flying-Capacitor Multilevel Inverter (FC)

During the 1980s the development of MI did not progress. The Flying-Capacitor converter as a multilevel chopper and a multilevel inverter was presented at the beginning of the 1990s [51]. Just as the output voltage is clamped by diodes in the case of a Diode-Clamped MI, it is clamped by capacitors in the case of Flying-Capacitor multilevel inverter (FC). Compared to the earth this capacitor seems to be floating, therefore it is called the Flying-Capacitor (FC) [52]. Furthermore, compared to a Diode-Clamped inverter, the suitable control enables voltage stabilization across the flying capacitors without any auxiliary power circuits thanks to phase redundancies [53].

#### 2.2.4.1 FC Operation

In Figure 2.10, a) three-level and b) five-level Flying-Capacitor topologies are shown. Both topologies are similar to a Diode-Clamped topology NPC [54-55]. The extension to more than five levels is easy even for Flying-Capacitor. As for the diodes in Diode-Clamped NPC, the capacitors series are drawn to highlight the voltage drop they have to tolerate. Indeed, the voltage over the capacitors nearer to the switches is lower than the voltage over the ones nearer to the source in steady-state. The voltage over each capacitor in Figure 2.10 is given by (2.4) [56].

$$V_c = \frac{E}{n-1} \qquad (2.4)$$

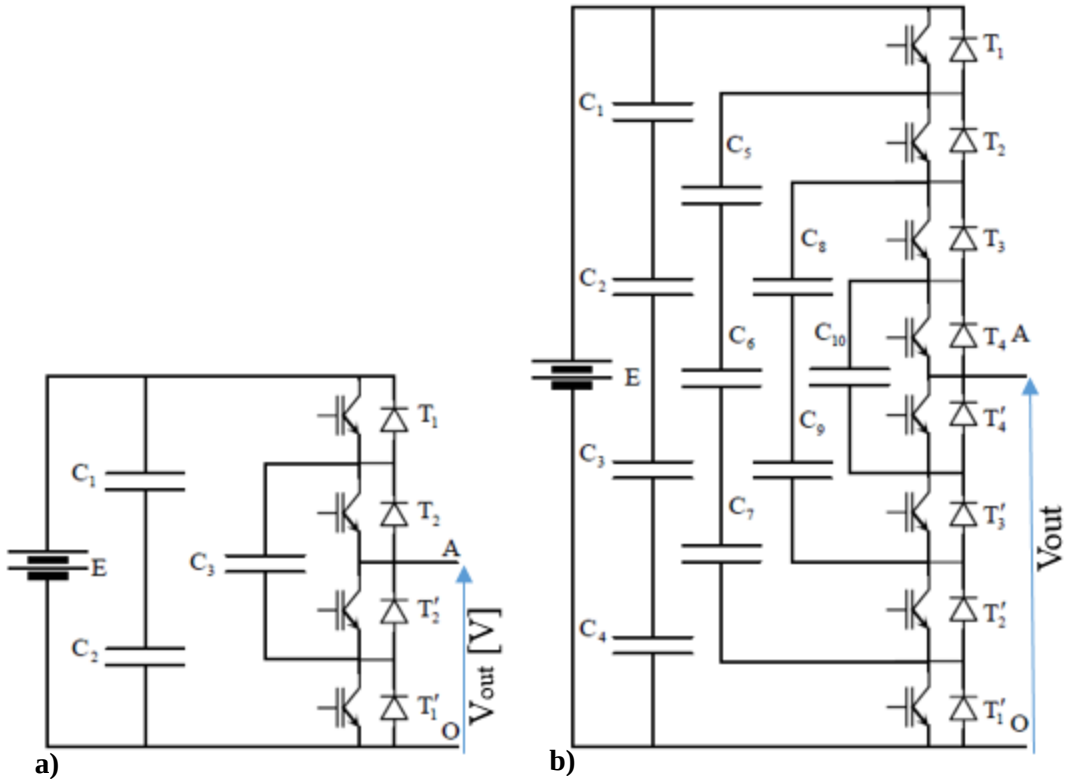



**Figure 2.10 FC multilevel inverter: a) the three-level, b) the five-level [54-55]**

Furthermore, these capacitors have the same function as the clamping diodes in a diode clamped converter: they keep constant the voltage drop between the busses to which they are connected. For this reason, they are called clamping capacitors. The voltage given by Equation (2.4) is also the reverse voltage drop each switch must bear when all capacitors are fully charged as it can be seen applying Kirchhoff's voltage law to the circuit in Figure 2.10. As in every inverter, some leg switches configurations are not allowed. For instance, considering the three-level inverter, $T_2$ and $T'_2$ cannot be simultaneously closed because this means a shortcut of $C_3$. To avoid any problem coming from a possible shortcut of capacitors or sources, $T_m$ and $T'_m$ (where the subscript m substitutes the number of a generic switch) must be in a complementary state. In this way the possible configurations for an n-level leg are given by Equation (2.5) [57]:

$$N_{Configuration} = 2^{n-1} \qquad (2.5)$$

Obviously, Flying-Capacitor leg presents intra-phase redundancy because the number of allowed configurations is greater than the number of possible voltage output levels. In Table 2.5 the three-level inverter switching Table is presented [57].

**Table 2.5 Three-level FC leg relationships between configurations and output voltages**

| $T_1$ | $T_2$ | $T'_1$ | $T'_2$ | $V_{out}$ |
|---|---|---|---|---|
| ON | ON | OFF | OFF | E |
| ON | OFF | OFF | ON | E/2 |
| OFF | ON | ON | OFF | E/2 |
| OFF | OFF | ON | ON | 0 |

For a three-level FC, there are four possible leg configurations and two of them give the same voltage level, presenting intra-phase redundancy as expected. These two configurations have different effects on the capacitor $C_3$. Indeed, considering an outgoing output current, the configuration with $T_1$ turned off and $T_2$ turned on makes $C_3$ discharging, because the capacitor has to feed the load. Whereas, when $T_1$ is turned off and $T_2$ is turned off, $C_3$ and the load are series connected to the source, and the current flowing into the capacitor charges it. Proper control can keep the capacitor balanced monitoring its state and choosing the right configuration each time the middle output is required [58]. A similar analysis can be done for the five-level inverter taking into account the effects of all the sixteen configurations shown in Table 2.6.

Considering Table 2.5 and Table 2.6, it is possible to deduce that the voltage applied is proportional to the sum of upper switches states. Assuming that $T_m$ represents the state of a generic upper switch, (2.6) shows this relationship.

$$V_{out} = \frac{E}{n-1} \sum_{m=1}^{n-1} T_m \qquad (2.6)$$

**Table 2.6 Five-level FC leg relationships between configurations and output voltages**

| $T_1$ | $T_2$ | $T_3$ | $T_4$ | $T'_1$ | $T'_2$ | $T'_3$ | $T'_4$ | $V_{out}$ |
|---|---|---|---|---|---|---|---|---|
| ON | ON | ON | ON | OFF | OFF | OFF | OFF | E |
| ON | ON | ON | OFF | OFF | OFF | OFF | ON | 3E/4 |
| ON | ON | OFF | ON | OFF | OFF | ON | OFF | 3E/4 |
| ON | OFF | ON | ON | OFF | ON | OFF | OFF | 3E/4 |
| OFF | ON | ON | ON | ON | OFF | OFF | OFF | 3E/4 |
| ON | ON | OFF | OFF | OFF | OFF | ON | ON | E/2 |
| ON | OFF | ON | OFF | OFF | ON | OFF | ON | E/2 |
| ON | OFF | OFF | ON | OFF | ON | ON | OFF | E/2 |
| OFF | ON | ON | OFF | ON | OFF | OFF | ON | E/2 |
| OFF | ON | OFF | ON | ON | OFF | ON | OFF | E/2 |
| OFF | OFF | ON | ON | ON | ON | OFF | OFF | E/2 |
| ON | OFF | OFF | OFF | OFF | ON | ON | ON | E/2 |
| ON | ON | OFF | OFF | ON | OFF | ON | ON | E/2 |
| ON | OFF | ON | OFF | ON | ON | OFF | ON | E/2 |
| ON | OFF | OFF | ON | ON | ON | ON | OFF | E/2 |
| ON | OFF | OFF | OFF | ON | ON | ON | ON | 0 |

### 2.2.4.2 FC Features

Looking at the voltage rating of the devices in the FC circuit, it can be seen that the number of capacitors which are used to clamp voltage are very high. If it is assumed that the voltage rating for all the capacitors is the same as the main dc-bus capacitors, the number of additional capacitors besides the main dc-bus capacitor can be expressed as $(l-1) \times (l-2)/2$, where "*l"* is the level of the inverter [59]. Hence, the Capacitor-Clamped multilevel inverter has the same problem as the diode-clamped multilevel inverter when the level of the inverter is high. The main disadvantage of the Flying-Capacitor architecture is capacitor balance. In a three-level inverter there is only one capacitor to keep balanced and the implementation of the control algorithm is quite easy. When the number of levels rise, the controlled voltages increase: more voltage sensors and more complicated controls are needed [60]. Even for this topology, the switch average currents might be different because they strictly depend on the control choice of redundant states. Some estimations of this value can be done, but is difficult to rate each switch for the exact current value. As with Diode-Clamped implementation, a switch that is not completely used is preferred. Another important advantage of this inverter is its portability. The FC can substitute a standard two-level inverter better than the NPC, because the DC bus capacitor is still present and correctly rated. This means there is no need to change it.

## 2.3 Conclusion

The integration of renewable energy sources to the electricity grid is an appealing opportunity. Over the past two decades, multilevel inverters (MIs) have attracted wide interest both in the scientific community and in the industry. The reason for the increased interest is that the MIs are a viable technology to implement controlled rotational movement in high-power applications. Therefore, the principle function of the Cascaded H-Bridge (CHB), Natural-Point-Camped (NPC), and Flying Capacitor inverter (FC) were explained in this chapter.

The advantages and disadvantages of the main three types of MIs topologies were addressed in this chapter. Generally, in the theory of multilevel inverters, the power circuit and control become more complex as an additional level is added. This is the main disadvantage for the MIs that have been discussed earlier in this chapter.

# CHAPTER 3

## *MIs MODULATION TECHNIQUES*

### 3.1 General

In this chapter, MI modulation techniques are discussed, to introduce the different control strategies that are used with MIs. Basically, all MIs operate in switch mode [61], which means that the semiconductor switched-OFF device is either turned ON or OFF with a small voltage drop. This process of switching the electronic device ON and OFF is called the modulation. Research has been done over 40 years on developing the optimum strategies to implement the multilevel inverters [62]. The control pulses for the devices arise in the modulator, and they are produced quickly enough that the capacitors and inductors can filter or average this alternated signal. There are many particular modulation techniques suitable for various types of inverters, and their mutual comparison can be carried out from several points of view (e.g., the switching losses, distortion and harmonic generation, complexity of algorithms, or speed of response.) Very often, the quality of modulation technique is determined by the total harmonic distortion (THD). The factor THD expresses the content of harmonics in the waveform, and it can be mathematically shown as in equation (3.1) [63]:

$$\text{THD} = \sqrt{\sum_{h=2,3,\dots}^{\infty} \left(\frac{V_h}{V_1}\right)^2} \qquad (3.1)$$

Where $V_h$ and $V_1$ are the RMS values of the monitored quantities, and “h” is the harmonic rank.

An inverter with a higher number of power electronic switches might need a modulation control with complex algorithms. When it comes to MI modulation, there are basically two groups of methods: modulation with fundamental switching frequency and high switching frequency as shown in Figure 3.1 [64].

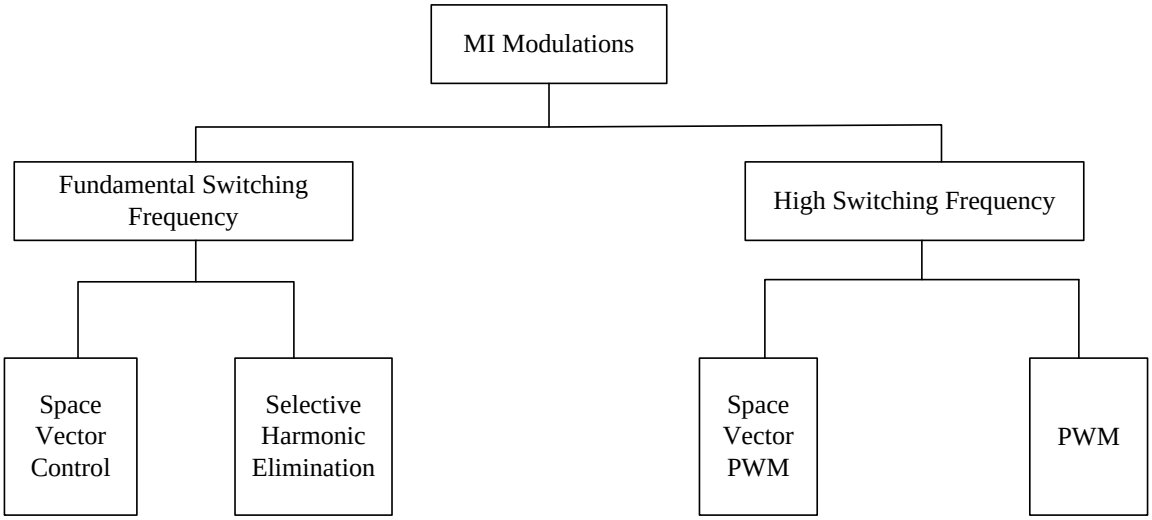



**Figure 3.1 MI modulations**

## 3.2 Fundamental Switching Frequency

Fundamental switching frequency modulations produce switch commutations at output fundamental frequency and can be aimed to cancel some particular low-frequency harmonics. These harmonics are dangerous to any system. In this modulation type, there is space vector control and selective harmonic elimination. In space vector control, the complex plane is divided into several hexagonal zones, defining the proximity of the reference to the nearest generable vector that is applied [65]. In selective harmonic elimination, the output is a staircase wave with the duration of steps optimized to cancel

the specified harmonics; however, the number of harmonics that can be eliminated simultaneously is proportional to the number of MI levels [66].

### 3.2.1 Space Vector Control

Space vector control (SVC) is a low (fundamental) frequency space vector modulation method that generates the desired mean load voltage value in every switching interval; however, for inverters with a higher number of voltage levels, the errors will be small in comparison to the reference vector [65]. SVC may, therefore, be adequate for an inverter with a higher number of voltage levels. SVC is a vector modulation technique, so the possible vectors can be seen as vertices of a triangular grid. In Figure 3.2a, a single element of this grid — an equilateral triangle — is highlighted. The medians drawn in the figure possess a particular property: they subdivide the triangle into three zones, defining the sets of points that are the nearest to one of the vertices [67]. Drawing the medians of all the triangles creates hexagonal meshes centered in each vertex and determines the sets of points closest to each generable vector. In Figure 3.2b, the hexagonal meshes of a five-level converter are shown together with all the equilateral triangles of the grid and a generic vector $\vec{V}$. The vector $\vec{V}$ will lay in one of the hexagonal regions, determining its closest generable vector that must be applied to the output [67]. In a period of time, as in a PWM cycle, SVC does not produce an output vector with the same DC value of the reference. This determines an error that is not compensated for, but the aim of the modulation is to choose the one generable vector that minimizes it. If the reference is a vector rotating at a constant angular speed, the output voltage waveform will be a symmetric staircase [68]. This kind of modulation is particularly suited for multilevel converters with a high number

of levels because the error gets smaller and smaller, which increases the levels. Thus, it is unnecessary to use a more complex modulation scheme involving the three vectors adjacent to the reference due to the high density of vectors the MIs present when their number of levels is high. Obviously, SVC is unreliable when applied to a standard two-level — or even a three-level — inverter because the ripple on the output voltage becomes unacceptable. Also, SVC can be used to control even-current source converters using current vectors instead of voltage vectors [69].

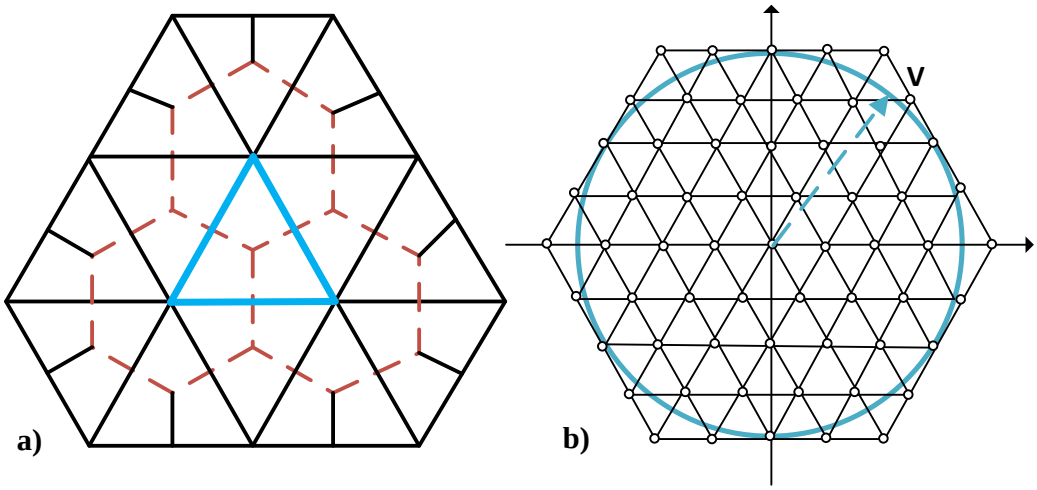



**Figure 3.2 SVC principle for a five-level inverter: a) Proximity zones definition, b) Vector choice**

### 3.2.2 Selective Harmonic Elimination

Selective harmonic elimination (SHE) is a low switching frequency modulation that uses pre-calculated switching angles to eliminate certain harmonics in the output voltage. By using and applying Fourier series analysis, the amplitude of any odd harmonic in the

output signal can be calculated, whereas the amplitudes of all even harmonics are zero. Normally, the switching angles are chosen so that the fundamental is set to the desired output amplitude and the other harmonics to zero. According to this method, and as shown in Figure 3.3, the switching angles must be in the interval [0 π/2]. For the number of switching angles, the harmonic components can be affected where (a-1) is the number of harmonics that can be eliminated [29] (one angle to set the fundamental) and a is the total number of harmonics.

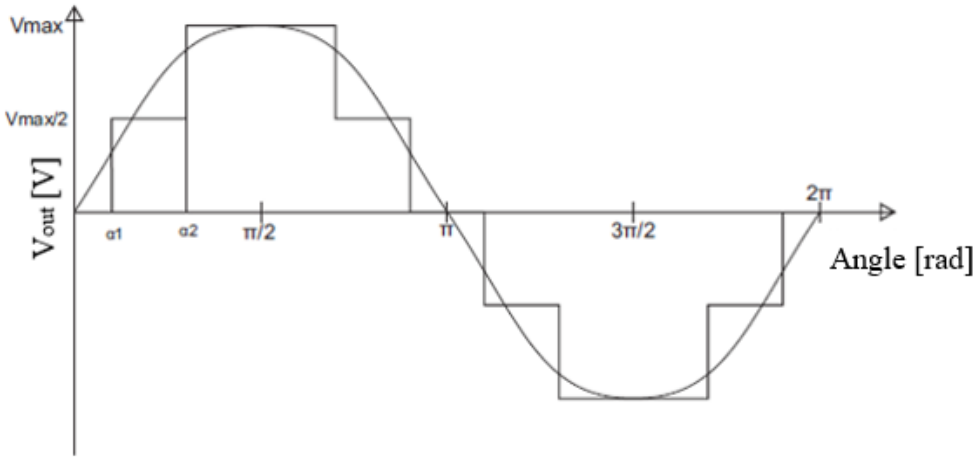



**Figure 3.3 SHE modulation to determine the switching of five-level inverter**

In this method, the number of switching angles in the interval [0 π/2] can be found from Equation (3.2), where "*m"* is the number of the inverter's levels [70].

$$a = \frac{m-1}{2} \qquad (3.2)$$

Using this method for the five-level inverter that is shown in Figure 3.3, and by applying "*m* "equal to 5 and found a=2, which means there are two switching angles. In the case of a five-level inverter, the first angle, $\alpha_1$, is set to modulate the fundamental signal amplitude, and the second angle, $\alpha_2$, is set to eliminate a chosen harmonic rank. The Fourier series equations for these signals are the following equations (3.3), (3.4), and (3.5) where "$m_i$" is the modulation index [71-72]:

$$\frac{m_i * V_{max} * \pi}{4} = \frac{V_{max}}{2}\cos(\alpha 1) + \frac{V_{max}}{2}\cos(\alpha 2) \quad (3.3)$$

$$0 = \cos(n * \alpha 1) + \cos(n * \alpha 2) \quad (3.4)$$

$$m_i = \frac{V_{ref}}{\sqrt{2}\, V_{max}} \quad (3.5)$$

The variable "n" as in previous equations, is the harmonic rank that is to be eliminated. For every switch angle available, one cosine term is added to each equation, and there are also as many equations as there are switching angles. Thus, for a situation with a number of switching angles, there is an equal number of equations and cosine terms. As for this five-level inverter situation, there are two switching angles [71], two equations and two cosine terms in every equation. Using this method with a seven-level inverter, the equation setup would instead be as follows. Variables "n1" and "n2" are the ranks of the two harmonics to be eliminated [72].

$$\frac{m_i * V_{max} * \pi}{4} = \frac{V_{max}}{3}\cos(\alpha 1) + \frac{V_{max}}{3}\cos(\alpha 2) + \frac{V_{max}}{3}\cos(\alpha 3) \quad (3.6)$$

$$0 = \cos(n1 * \alpha 1) + \cos(n1 * \alpha 2) + \cos(n1 * \alpha 3) \quad (3.7)$$

$$0 = \cos(n2 * \alpha 1) + \cos(n2 * \alpha 2) + \cos(n2 * \alpha 3) \quad (3.8)$$

So to generalize this methods and equations for “m” level inverter the equation become as following:

$$\frac{m_i * V_{max} * \pi}{4} = \frac{V_{max}}{n}\cos(\alpha 1) + \frac{V_{max}}{n}\cos(\alpha 2) + \cdots + \frac{V_{max}}{n}\cos(\alpha m) \quad (3.9)$$

The number of the cosine equations will be equal to (n-1).

## 3.3 High Switching Frequency

The other type of modulation, high switching frequency modulation, is the adaptation of a standard pulse-width modulation (PWM) to multi levels, and it is meant to switch at a high frequency [73]. Among high switching frequency modulation, there is a space vector PWM, phase-shifted PWM, and another subclass called level-shifted PWM. Phase-shifted PWM is the extension of the standard two-level space vector modulation to a greater number of levels. In phase-shifted PWM, several phase-shifted references are used to generate the control pulses [29]. The modulations of PWM and space vector PWM will be discussed in detail in the following sections.

### 3.3.1 PWM

Pulse-width modulation (PWM) is a method of controlling the output voltage of an inverter. PWM control requires the generation of both reference and carrier signals that feed into a comparator that creates output signals based on the difference between the signals. In this method, a control signal is compared with a repetitive signal — typically a triangular signal. To make the converter work in an inverter mode, the control signal should have a sinusoidal shape [74]. At a constant switching frequency, the time period of the

triangular signal is also constant since this signal gives the switching frequency. This is given in equation (3.6).

$$f_{sw} = \frac{1}{T_{tri}} \qquad (3.10)$$

The frequency of the control signal gives the frequency of the desired fundamental output voltage. For a two-level inverter, there are two switches in one bridge leg, and the upper switch will be on when the control signal is greater than the triangular signal. If unipolar switching is chosen, the lower switch will be off when the upper is on, which means that it will be off when the control signal is greater than the triangular signal. Switch number two will be on when the control signal is lower than the triangular signal, and, hence, the upper switch will be off (see Figure 3.4).

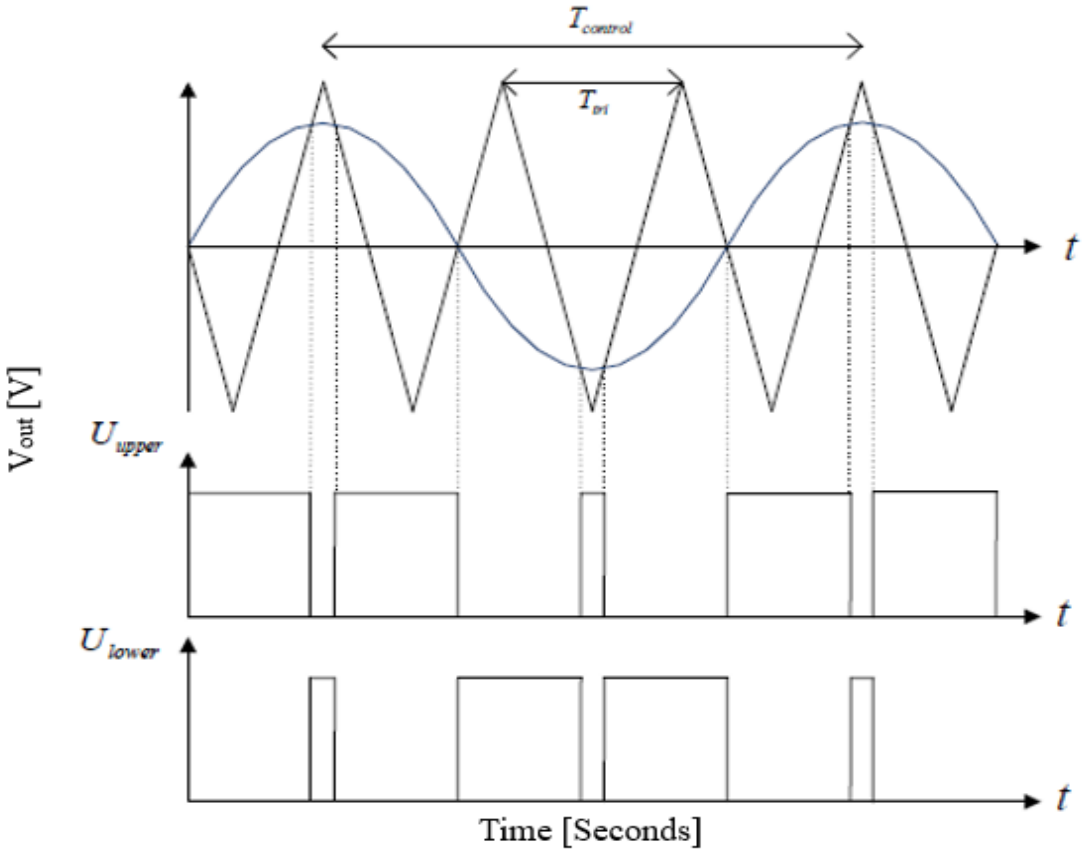



**Figure 3.4 The principle PWM**

When it comes to MIs, the PWM control is more complicated than a two-level inverter [75]. There are other parameters that need to be defined in the case of MIs with PWM control. The amplitude ratio "$m_a$" is given as following:

$$m_a = \frac{U_{control}}{U_{triangle}} \quad (3.11)$$

This ratio gives the values of the amplitude of the inverter leg voltage compared with $U_{Dc}/2$, where the leg voltages will be given in the following equation:

$$U_a = m_a * \cos(wt) \quad (3.12)$$

$$U_b = m_a * \cos(wt - \frac{2\pi}{3}) \quad (3.13)$$

$$U_c = m_a * \cos(wt - \frac{4\pi}{3}) \quad (3.14)$$

These voltages are the bridge-leg voltages that are desired on the AC side of the converter. When normal sinusoidal modulation is used, these signals are also the control signals that are compared with the triangular signal [75]. The other parameter that is important to be defined is the ratio between the frequency of the control signal and the triangular signal, as shown below:

$$m_f = \frac{f_{sw}}{f_{control}} \quad (3.15)$$

It is common to divide the modulation strategies into two strategies and the preferred strategy is dependent on "$m_f$". In [75], it is recommended to use synchronous modulation if "$m_f$" is lower or equal to 21, and asynchronous modulation if "$m_f$" is higher than 21. The definition of synchronous modulation is that "$m_f$" is an integer, which means that the control signal is sampled at the same angles every fundamental period. Asynchronous modulation is when "$m_f$" is not an integer. Asynchronous modulation will create undesirable subharmonics, but due to the high frequency, the difference in amplitude

between synchronous and asynchronous subharmonics will be marginal [75]. The major drawback of synchronous modulation is that it is not very flexible, and, hence, there will be challenges in applications with variable speed drives. This should not cause problems with asynchronous modulation as long as "$m_f$" is large. The application studied in this report is to be used in the medium voltage range, and the switching frequency will be in the range of 300-1100 Hz, which indicates that synchronous modulation should be used. Having a low switching frequency will increase the amplitude of the lower harmonics. This occurs because the harmonic distortion has the greatest values around "$m_f$", "$2m_f$", "$3m_f$", and so on, and since the switching frequency is reduced, "$m_f$" is also reduced.

### 3.3.2 Space Vector PWM

Space vector PWM (SVPWM) is a popular modulation method for converters due to its low harmonics. The theory of space vector is that phase A, B, and C have a permanent position next to each other in the vector space, phase shifted with 120° degrees. Since the late 1990s, several SVPWM schemes for MIs have been introduced [76-78]. The SVPWM schemes are developed to find the three nearest nodes on the voltage hexagon lattice with respect to the reference vector. The mathematical formulation of the early SVPWM methods was quite complex because the voltage hexagon lattice was used in the Cartesian coordinate system [79]. The coordinates of the nodes on the lattice are fractional numbers, which made the node selection difficult. This was until a coordinate transformation was introduced to be applied to the reference vector [78]. The idea was that the reference vector was transformed from the Cartesian coordinate system (where the voltage vector is usually attached to a stationary stator reference frame) to the 60° coordinate system. The 60°

coordinate system represents one sector on the lattice, and its benefit is that the coordinates for the nodes can be presented by integers. Therefore, determination of the nodes could be accomplished by simple rounding functions and integer calculation. The use of the phase voltages was not very efficient in the method proposed in [78]. The three nearest nodes were used, but only in such a way that no switching state redundancies were exploited. This resulted in phase voltages where one phase did not change its state at all during one switching period. The method of using four switching states during the switching period to minimize the harmonic content of the voltage is proposed in [80]. The fourth switching state is redundant with the first state, and, therefore, only the three nearest nodes were used. An explicit description of an algorithm for the SVPWM scheme based on the above-mentioned methodology is given in [81]. The advantage of determining the switching states according to the vector location on the voltage hexagon lattice is that the whole area covered by the lattice can be used without needing to consider modulation indices. With symmetric sinusoidal phase references, the carrier-based modulation schemes achieve 75% of the maximum vector length 2*Mu* dc. To exceed this limit, a third harmonic has to be added to the references. With the SVPWM, the modulation is successful as long as the reference vector is located inside the voltage hexagon. The addition of a third harmonic does not have to be considered separately.

## 3.4 Conclusion

Modern power electronic technology is an important part in distributed generation and the integration of the renewable energy to the power grid, which makes it important to introduce the modulation control of this technology. This chapter discussed the most important and most used modulation techniques for MIs. In this thesis, the PWM technique will be used to compare with the proposed modulation technique. The proposed modulation technique is listed under the fundamental switching frequency because it uses low switching frequency. The proposed modulation technique will be shown in Chapter 4.

# CHAPTER 4

## *DESIGN AND METHODOLOGY*

### 4.1 Introduction

In the theory of the multilevel inverters, the complexity of the power circuit as well as the control increases rapidly with every additional level. A new three-phase, five-level inverter design topology has been proposed and simulated. The topology offers smaller number of power electronics switches when compared with other topologies. This chapter will present the design of a new topology and the advantages of this topology by comparing it with other existing topologies and provide new modulation technique derived for a pre-calculated switching angles that offer additional benefits.

### 4.2 The Proposed Three-Phase, Five-Level Topology Description

A three-phase five-level inverter with two input DC voltage sources, $E_1$ and $E_2$, and nine power switches is being proposed as shown in Figure 4.1, where:

$\begin{Bmatrix} TaH \\ \text{TbH} \\ \text{TcH} \end{Bmatrix}$ Are power rated switches that connect to the positive side of the input;

$\begin{Bmatrix} TaL \\ \text{TbL} \\ \text{TcL} \end{Bmatrix}$ Are Bi-directional power rated switches that connect to the low input voltage;

$\begin{Bmatrix} Ta0 \\ \text{Tb0} \\ \text{Tc0} \end{Bmatrix}$ Are power rated switches that connect to the negative side of the input.

The leg voltage $V_{i0}$, which is the output voltage during the positive half-cycles, can be found when i = a, b, and c. This can also be controlled by the switch control signals that

will be used in Chapter 5 in order to compare the simulation for the proposed control results with the traditional control. $E_1$ and $E_2$ are the DC input voltages from a variety of sources that include batteries and photovoltaics. In this Chapter, the analysis will assume that $E_1 = E_2 = E$; however, the topology is designed to accept different input values as when utilizing adaptive reconfigurable sources. The power switches are controlled in the on-off state, and assumed to be ideal. Let "$f_{ij}$" represent the input control function of the switches mode (ON/OFF), with $f_{ij} \in \{0, 1\}$, i ∈ {a, b, c}, j∈ {H, L, 0}, and where

$$f_{ij} = \begin{cases} 0 \; if \; T_{ij} \; is \; off \\ 1 \; if \; T_{ij} \; is \; on \end{cases} \tag{4.1}$$

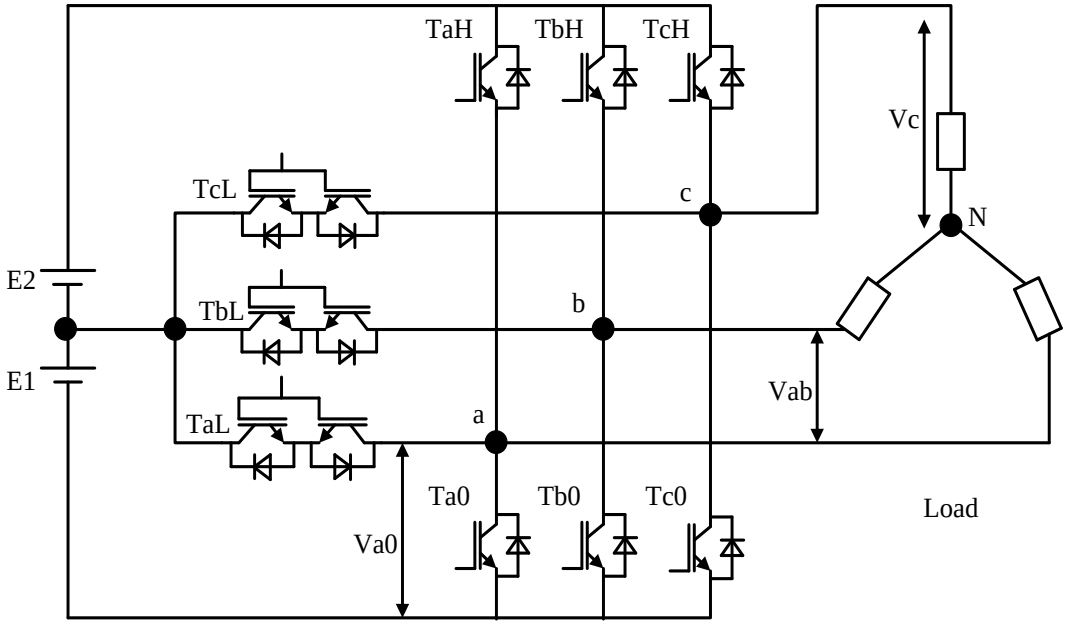



**Figure 4.1 Proposed three-phase, five-level inverter topology**

By controlling "$f_{ij}$", the phase voltage $v_{i0}$ across the output terminals a, b, c can be determined by (4.2) and (4.3):

$$\begin{cases} v_{i0} = 2E \; if \; T_{iH} \; on \; and \; \{T_{iL}, T_{i0}\} \; off \\ v_{i0} = E \; if \; T_{iL} \; on \; and \; \{T_{iH}, T_{i0}\} \; off \\ v_{i0} = 0 \; if \; T_{i0} \; on \; and \; \{T_{iH}, T_{iL}\} \; off \end{cases} \quad (4.2)$$

$$\begin{bmatrix} v_{a0} \\ v_{b0} \\ v_{c0} \end{bmatrix} = \begin{bmatrix} f_{aH} & f_{aL} & f_{a0} \\ f_{bH} & f_{bL} & f_{b0} \\ f_{cH} & f_{cL} & f_{c0} \end{bmatrix} \begin{bmatrix} 2E \\ E \\ 0 \end{bmatrix} \quad (4.3)$$

To find the phase-to-phase voltage, and example is provided with $v_{ab}$ defined as,

$$v_{ab} = v_{a0} - v_{b0} \quad (4.4)$$

From (4.3) the voltages $v_{a0}$, $v_{b0}$ and $v_{c0}$ will be found as,

$$v_{a0} = f_{aH}.2E + f_{aL}.E + f_{a0}.0 \quad (4.5)$$

$$v_{b0} = f_{bH}.2E + f_{bL}.E + f_{b0}.0 \quad (4.6)$$

$$v_{c0} = f_{cH}.2E + f_{cL}.E + f_{c0}.0 \quad (4.7)$$

$$v_{ab} = (f_{aH} - f_{bH}).2E + (f_{aL} - f_{bL}).E + (f_{a0} - f_{b0}).0 \quad (4.8)$$

$$v_{bc} = (f_{bH} - f_{cH}).2E + (f_{bL} - f_{cL}).E + (f_{b0} - f_{c0}).0 \quad (4.9)$$

$$v_{ca} = (f_{cH} - f_{aH}).2E + (f_{cL} - f_{aL}).E + (f_{c0} - f_{a0}).0 \quad (4.10)$$

According to the following analysis, the phase to phase output voltage can be given by (4.11):

$$\begin{bmatrix} v_{ab} \\ v_{bc} \\ v_{ca} \end{bmatrix} = \begin{bmatrix} f_{aH} - f_{bH} & f_{aL} - f_{bL} & f_{a0} - f_{b0} \\ f_{bH} - f_{cH} & f_{bL} - f_{cL} & f_{b0} - f_{c0} \\ f_{cH} - f_{aH} & f_{cL} - f_{aL} & f_{c0} - f_{a0} \end{bmatrix} . \begin{bmatrix} 2E \\ E \\ 0 \end{bmatrix} \quad (4.11)$$

The voltage output of the proposed topology has five level voltages as shown in Figure 4.2, and in order to get these five level voltages the switches should be in specific mode (ON/OFF) for each level based on Equations (4.3) and (4.11).

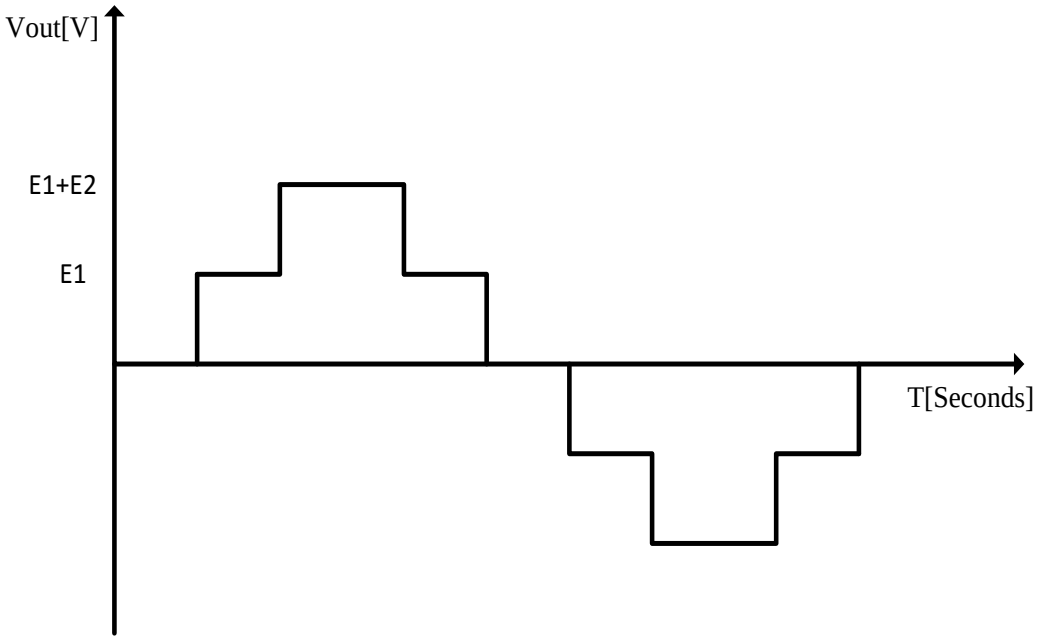



**Figure 4.2 The voltage output of the five-level inverter topology**

The switches states to get $v_{ab}$ in the inverter voltage output is shown in Figure 4.3 as an example to show the topology operation with different voltage levels. Figure 4.3a shows that the output voltage $v_{ab}$ will be $(E_1 + E_2)$ when the switches $T_{aH}$ and $T_{b0}$ are the only

ON switches. Where Figure 4.3b shows that the output voltage $v_{ab}$ will be $(-E_1 - E_2)$ when the switches $T_{bH}$ and $T_{a0}$ are the only ON switches. Also Figure 4.3c shows that the output voltage $v_{ab}$ will be $(E_2)$ when the switches $T_{aH}$ and $T_{bL}$ are the switches in ON state. Where Figure 4.3d shows that the output voltage $v_{ab}$ will be $(-E_1)$ when the switches $T_{bL}$ and $T_{a0}$ are the only on switches. The same thing in Figure 4.3e shows that in order to get output voltage $v_{ab}$ with value of $(0\,V)$ the switches $T_{b0}$ and $T_{a0}$ are in ON state. The other voltage levels and phase to phase voltages will be found by using the same method with Equation (4.11).

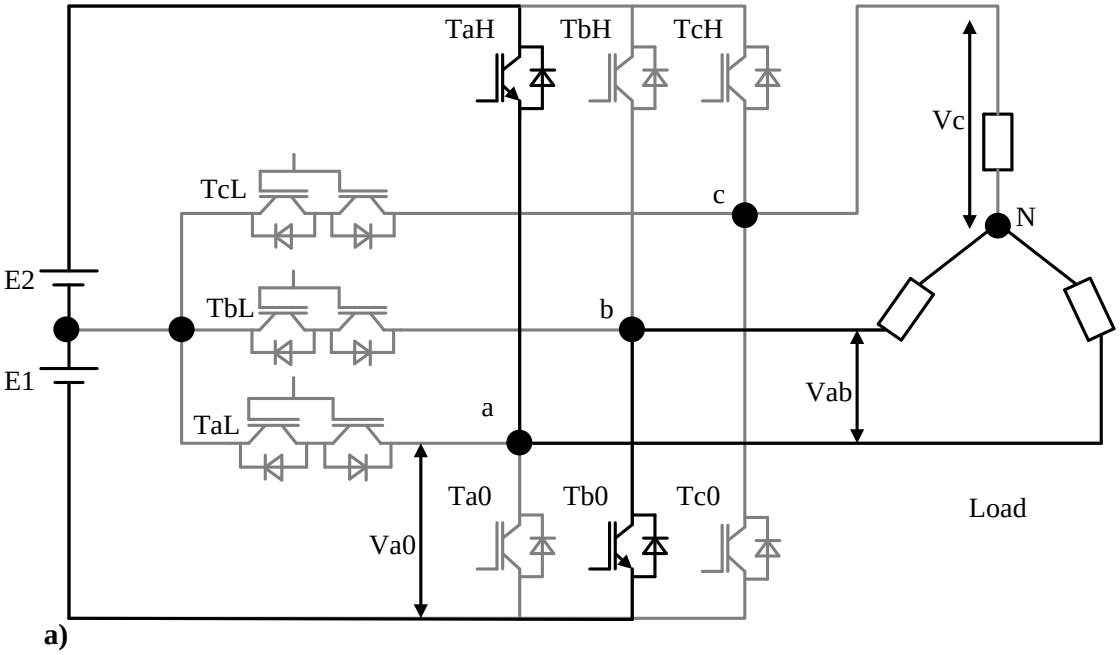



**Figure 4.3 The output voltage phase to phase is: a) $E_1$+$E_2$**

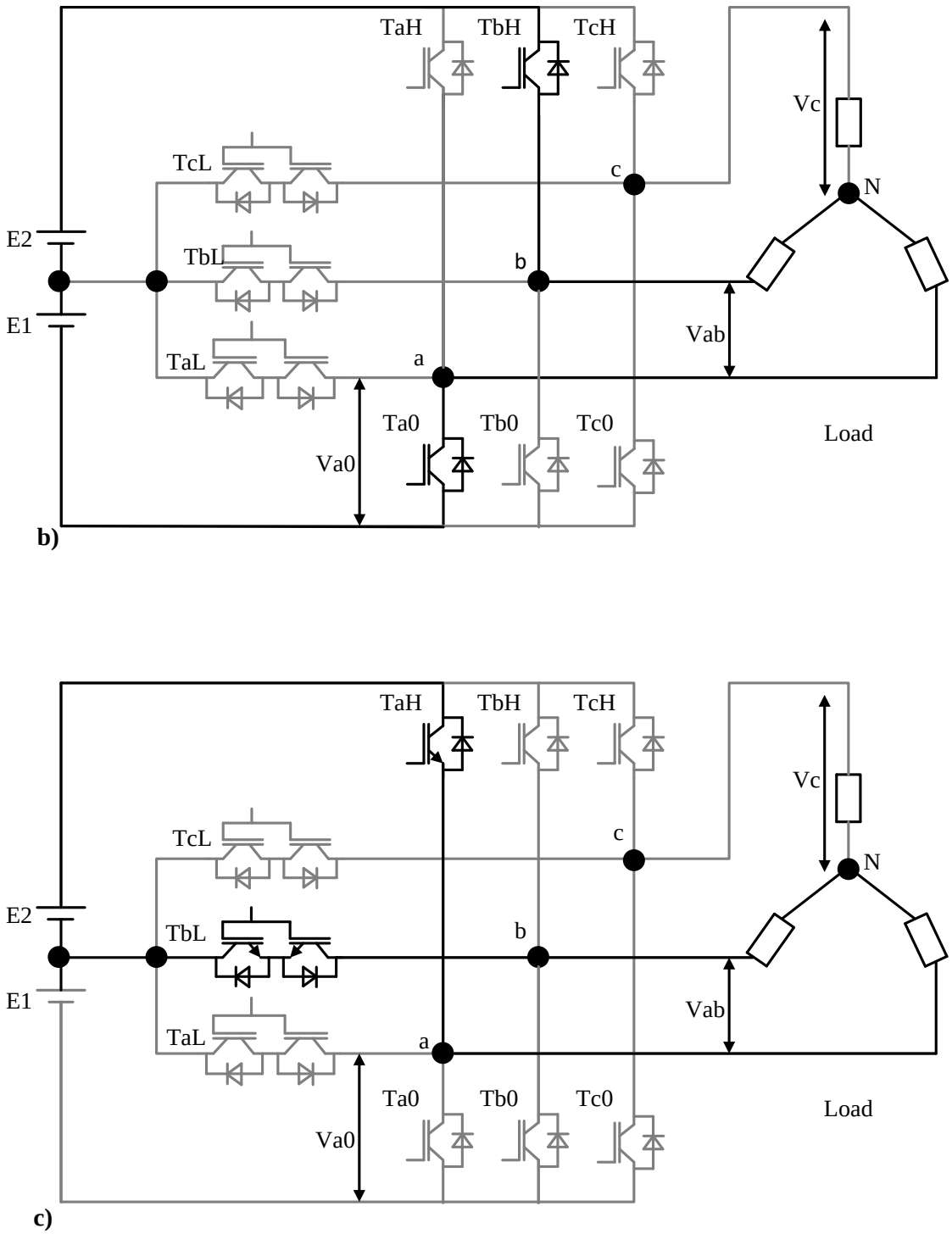
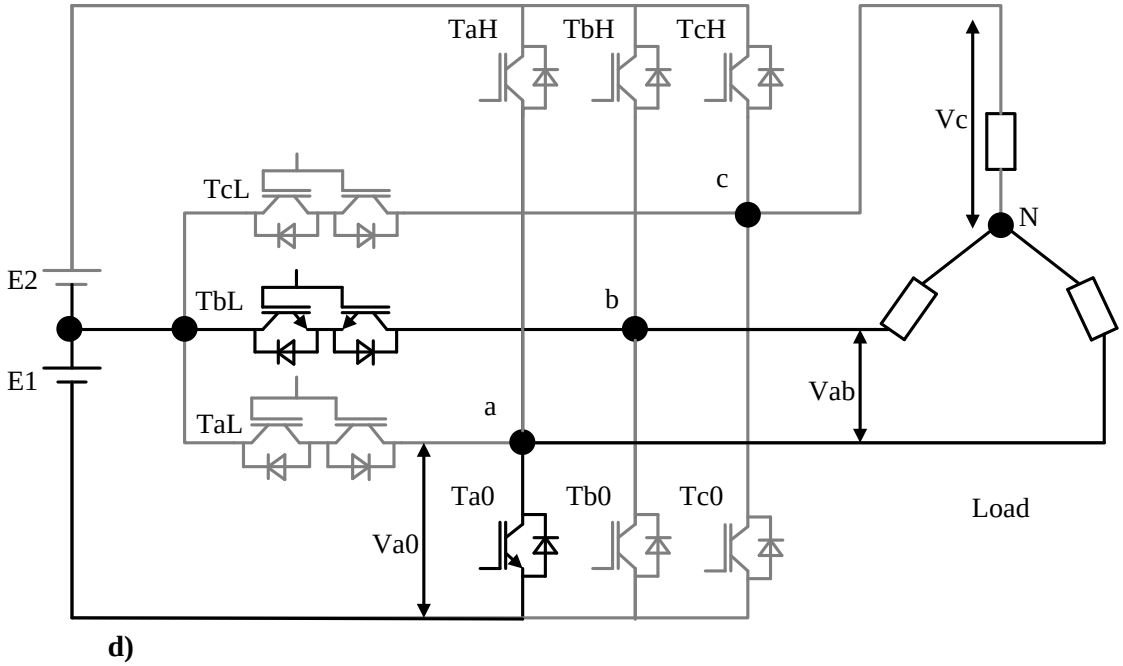
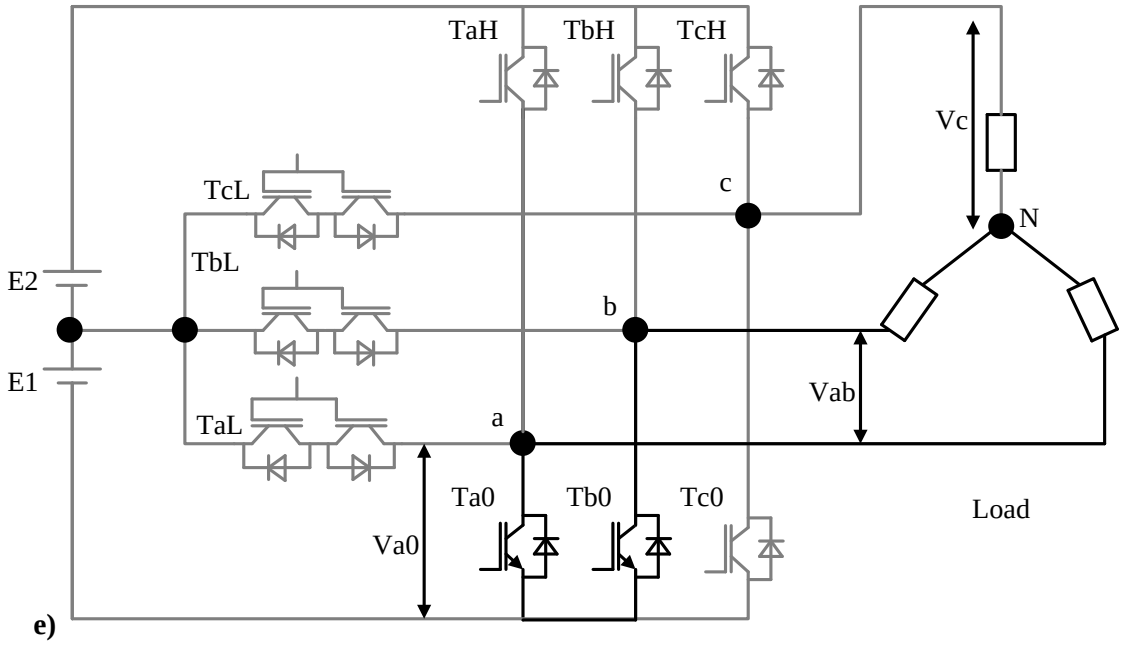



**Figure 4.3 The output voltage phase to phase is: b) - ($E_1$+$E_2$), c) $E_2$**




**d)**




**e)**

**Figure 4.3 The output voltage phase to phase is: d) - $E_1$, e) 0**

## 4.3 Advantages and Comparison of the Proposed Topology with Existing Topologies

Traditional MIs have disadvantages in the number of power electronics switches, diodes, filters, and high switching frequency as the number of levels increase, for example in five-level H-Bridge topology will requires a high number of switches which is 24 power electronic switches.

Therefore, the main characteristics and features of this topology are listed as following:

- Fewer power electronic switches;
- Fewer input DC sources;
- High efficiency;
- Filterless;
- Reduction the total volume, weight and the losses;
- Lower price.

The proposed topology is far better than other current models because of the overall reduction in the required components. Table 4.1 shows the number of switches, diodes, and capacitors that are required for different topologies where “N” is the number of levels [82].

**Table 4.1. The total number of components required for different topologies in three phase circuit [82]**

| Inverter Type | NPC | FC | CHB | Voltage Reversal |
|---|---|---|---|---|
| **Main switches** | 6(N-1) | 6(N-1) | 6(N-1) | 3((N-1)+2) |
| **Main diode** | 6(N-1) | 6(N-1) | 0 | 0 |
| **Clamping diode** | 3(N-1)(N-2) | 0 | 0 | 0 |
| **DC bus/ capacitors Isolated Supplies** | (N-1) | (N-1) | $\frac{3}{2}$(N-1) | (N-1)/2 |
| **Flying capacitors** | 0 | $\frac{3}{2}$(N-1)*(N-2) | 0 | 0 |
| **Total** | (N-1) (3N+7) | (N-1) * (3N+20)/2 | $\frac{27}{2}$(N-1) | (13N+11)/2 |

The proposed inverter has been developed using five levels (2E, E and 0), so in order to compare this topology with other five level models, a new Table has been developed with N=5. Table 4.2 shows that the new topology requires fewer power electronic switches.

**Table 4.2 The comparison of total number of components required for existing topologies with the new topology in three-phase circuit**

| Inverter Type | NPC | FC | CHB | Voltage Reversal | Proposed |
|---|---|---|---|---|---|
| **Main switches** | 24 | 24 | 24 | 18 | **9** |
| **Main diode** | 24 | 24 | 0 | 0 | **0** |
| **Clamping diode** | 36 | 0 | 0 | 0 | **0** |
| **DC bus/ capacitors Isolated Supplies** | 4 | 4 | 6 | 2 | **0** |
| **Flying capacitors** | 0 | 18 | 0 | 0 | **0** |
| **Total** | 88 | 70 | 30 | 20 | **9** |

## 4.4 The Modulation/Control Technique

The operation of all MIs was discussed in Chapter 3. The switch operation is either OFF or ON with a little voltage drop across it. The coordination between switch operations is called the modulation like the fundamental switching frequency or the high switching frequency modulations as explained in Chapter 3. A novel inverter modulation technique has been developed and applied with the proposed topology. The new approach is proposed to calculate the switching angles in the range [0 $\pi/3$] to improve the total harmonic distortion (THD) by eliminating the low harmonics order. Current approaches to improve the THD is based on pre-calculated switching angles in the range [0 $\pi/2$] [83].

The main feature of the modulation is that, unlike PWM methods or the pre-calculated [0, π/2] as discussed in Chapter 3, the switching angles are computed offline and are designed in such a way that arbitrary harmonics (usually of low order) are eliminated since the lower harmonics rank are the most dangerous to the system. This method also has the advantage of having few commutations per cycle and achieves better efficiency and working with low frequency.

### 4.4.1 Pre-Calculated Technique Development

This section presents the mathematical development of the switching angles calculation in the interval [0 π/3]. The steps are shown as following:

- Start with listing the properties and characteristics of the ideal voltage waveform of the three balanced voltages as shown in Figure 4.4a, and when analysis this waveform and zooming on the [0 π] range as shown in Figure 4.4b we find:

  1. Property (1): $v_{ab}$ is an even function with respect to zero

$$\forall \alpha \in \left[0 , \frac{\pi}{2}\right], v_{ab}(-\alpha) = v_{ab}(\alpha) \tag{4.12}$$

  2. Property (2): $v_{ab}$ is an odd function with respect π/2

$$\forall \alpha \in \left[0 , \frac{\pi}{2}\right], v_{ab}\left(\frac{\pi}{2} + \alpha\right) = -v_{ab}\left(\frac{\pi}{2} - \alpha\right) \tag{4.13}$$

  3. Property (3): $v_{bc}$ is symmetrical to $v_{ab}$with respect to π/3

$$\forall \alpha \in \left[0 , \frac{\pi}{3}\right], v_{bc}\left(\frac{\pi}{3} + \alpha\right) = -v_{ab}\left(\frac{\pi}{3} - \alpha\right) \tag{4.14}$$

4. Property (4): $v_{ca}$ is an inverted and shifted version of $v_{ab}$

$$\forall \alpha \in \left[0\ , \frac{\pi}{3}\right], v_{ca}\left(\frac{\pi}{3}+\alpha\right) = -v_{ab}(\alpha) \tag{4.15}$$

5. Property (5): $v_{ab}$, $v_{bc}$ and $v_{ca}$ are balanced three-phase voltages

$$\forall \alpha \in [0\ , 2\pi], v_{ab}(\alpha) + v_{bc}(\alpha) + v_{ca}(\alpha) = 0 \tag{4.16}$$

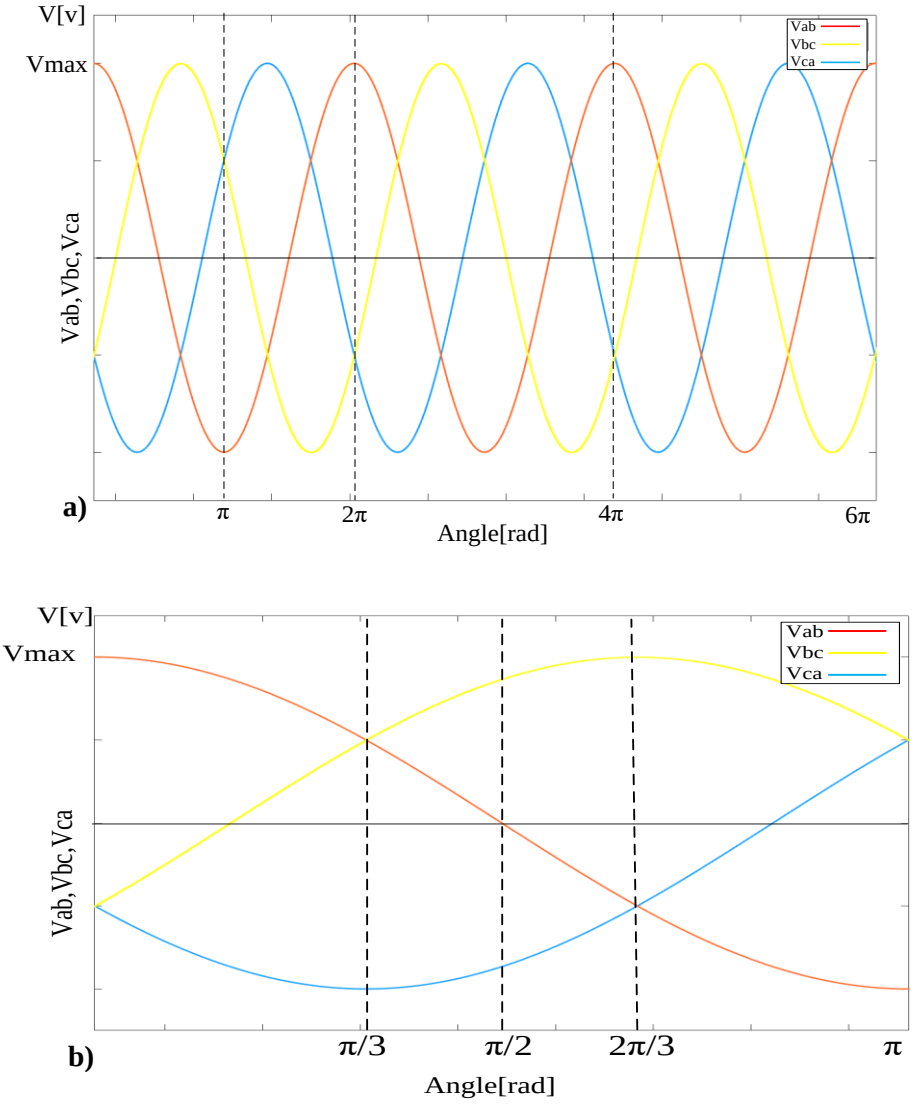



**Figure 4.4 Ideal Balanced Three Phase System waves: a) in the interval [0 6π], b) in the interval [0 π]**

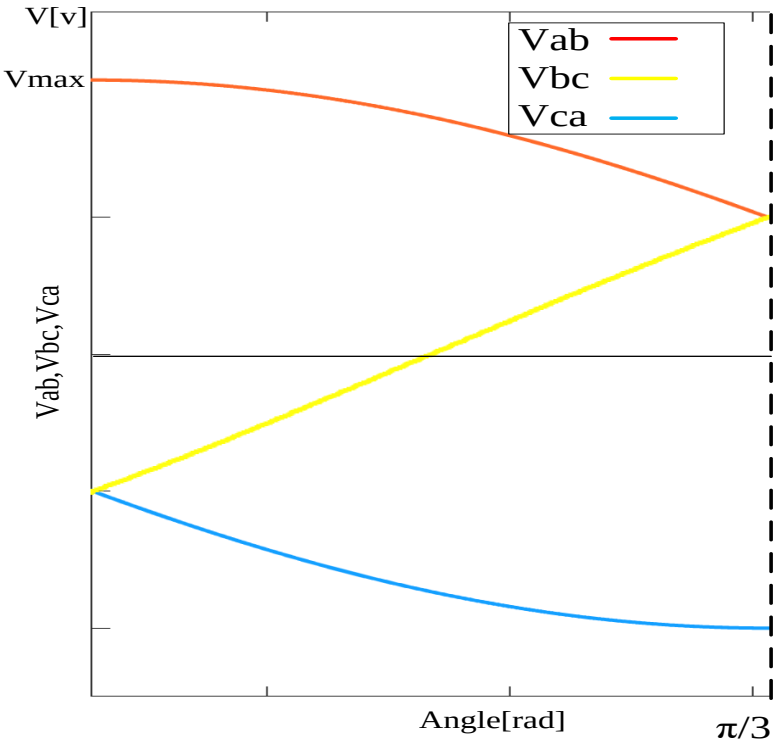



**Figure 4.5 Ideal Balanced Three Phase System in interval [0 π/3]**

- Assign the above properties of the ideal voltage waveform of the three balanced voltages to the inverter's output voltage by focusing in the [0, π/3] range as shown in Figure 4.5, and use the Fourier coefficients of the phase-to-phase output voltage that is given by (4.17) because it is well known that each periodic function of variable can be composed of a set of sine and cosine functions [84-86]:

$$\begin{cases} a_k = \frac{1}{\pi}\int_{-\pi}^{\pi} v_{ab}(\alpha).\cos(k\alpha)d\alpha \\ b_k = \frac{1}{\pi}\int_{-\pi}^{\pi} v_{ab}(\alpha).\sin(k\alpha)d\alpha \end{cases} \quad (4.17)$$

Use property (1) and apply it to the Fourier coefficients to become:

$$\forall k \quad b_k = 0 \; et \; a_k = \frac{2}{\pi}\int_0^{\pi} v_{ab}(\alpha).\cos(k\alpha)d\alpha \tag{4.18}$$

Use property (2) and apply it to the Fourier coefficients to become:

$$a_k = 0 \qquad \text{if k is an even} \tag{4.19}$$

$$a_k = \frac{4}{\pi}\int_0^{\pi/2} v_{ab}(\alpha)\cos(k\alpha)d\alpha \qquad \text{if k is an odd} \tag{4.20}$$

Use the property (5) and apply it to the Fourier coefficients to become:

$$a_{k=2p+1} = \frac{4}{\pi}\left[\int_0^{\pi/3} v_{ab}(\alpha)\cos(k\alpha)d\alpha - \int_{\pi/3}^{\pi/2}\left\{v_{bc}(\alpha)+v_{ca}(\alpha)\right\}\cos(k\alpha)d\alpha\right] \tag{4.21}$$

Using the property (3), (4) and applying it to the Fourier coefficients to become:

$$a_{k=2p+1} = \frac{4}{\pi}\left(\int_0^{\pi/3} v_{ab}(\alpha).\cos(k\alpha)d\alpha - \int_{\pi/3}^{\pi/2}\left\{v_{ab}(2\frac{\pi}{3}-\alpha)-v_{ab}(\alpha-\frac{\pi}{3})\right\}\cos(k\alpha)d\alpha\right) \tag{4.22}$$

$$a_{k=2p+1} = \frac{4}{\pi}\left(\int_0^{\pi/3} v_{ab}(\alpha).\cos(k\alpha)d\alpha - \underbrace{\int_{\pi/3}^{\pi/2} v_{ab}(2\frac{\pi}{3}-\alpha)\cos(k\alpha)d\alpha}_{1} + \underbrace{\int_{\pi/3}^{\pi/2} v_{ab}(\alpha-\frac{\pi}{3})\cos(k\alpha)d\alpha}_{2}\right) \tag{4.23}$$

Making the following changes to the variables:

$\frac{2\pi}{3} - \alpha = \beta$ , whether $d\alpha = -d\beta$ , in term 1, (4.24)

$\alpha - \frac{\pi}{3} = \beta$ , Whether $d\alpha = d\beta$ , in term 2, (4.25)

The Fourier coefficients become as following:

$$a_{k=2p+1} = \frac{4}{\pi}\left( \int_0^{\pi/3} v_{ab}(\alpha)\cos(k\alpha)d\alpha + \int_{\pi/3}^{\pi/6} v_{ab}(\beta)\cos\left(k\left(2\frac{\pi}{3} - \beta\right)\right)d\beta + \int_0^{\pi/6} v_{ab}(\beta)\cos\left(k\left(\frac{\pi}{3} + \beta\right)\right)d\beta \right) \quad (4.26)$$

$$a_{k=2p+1} = \frac{4}{\pi}\left( \int_0^{\pi/3} v_{ab}(\alpha)\cos(k\alpha)d\alpha - \int_{\pi/6}^{\pi/3} v_{ab}(\alpha)\cos\left(k\left(2\frac{\pi}{3} - \alpha\right)\right)d\alpha + \int_0^{\pi/6} v_{ab}(\alpha)\cos\left(k\left(\frac{\pi}{3} + \alpha\right)\right)d\alpha \right) \quad (4.27)$$

$$a_{k=2p+1} = \frac{4}{\pi}\left( \int_0^{\pi/3} v_{ab}(\alpha)\cos(k\alpha)d\alpha - \int_{\pi/6}^{\pi/3} v_{ab}(\alpha)\cos\left(k\left(\pi - \frac{\pi}{3} - \alpha\right)\right)d\alpha + \int_0^{\pi/6} v_{ab}(\alpha)\cos\left(k\left(\frac{\pi}{3} + \alpha\right)\right)d\alpha \right) \quad (4.28)$$

$$a_{k=2p+1} = \frac{4}{\pi}\left( \int_0^{\pi/3} v_{ab}(\alpha)\cos(k\alpha)d\alpha - \int_{\pi/6}^{\pi/3} v_{ab}(\alpha)\cos(k\pi)\cos\left(k\left(\frac{\pi}{3} + \alpha\right)\right)d\alpha + \int_0^{\pi/6} v_{ab}(\alpha)\cos\left(k\left(\frac{\pi}{3} + \alpha\right)\right)d\alpha \right) \quad (4.29)$$

Since K is an odd number, $\cos(K\pi) = -1$ (4.30)

$$a_{k=2p+1}=\frac{4}{\pi}\left(\int_{0}^{\pi/3}v_{ab}(\alpha)\cos(k\alpha)d\alpha+\int_{\pi/6}^{\pi/3}v_{ab}(\alpha)\cos\left(k\left(\frac{\pi}{3}+\alpha\right)\right)d\alpha+\int_{0}^{\pi/6}v_{ab}(\alpha)\cos\left(k\left(\frac{\pi}{3}+\alpha\right)\right)d\alpha\right) \quad (4.31)$$

$$a_{k=2p+1}=\frac{4}{\pi}\left(\int_{0}^{\pi/3}v_{ab}(\alpha)\cos(k\alpha)d\alpha+\int_{0}^{\pi/3}v_{ab}(\alpha)\cos\left(k\left(\frac{\pi}{3}+\alpha\right)\right)d\alpha\right) \quad (4.32)$$

$$a_{k=2p+1}=\frac{4}{\pi}\left(\int_{0}^{\pi/3}v_{ab}(\alpha)\left\{\cos(k\alpha)+\cos\left(k\left(\frac{\pi}{3}+\alpha\right)\right)\right\}d\alpha\right) \quad (4.33)$$

$$a_{k=2p+1}=\frac{8}{\pi}\cos\left(k\frac{\pi}{6}\right)\int_{0}^{\pi/3}v_{ab}(\alpha)\cos\left(k\left(\frac{\pi}{6}+\alpha\right)\right)d\alpha \quad (4.34)$$

After assigning the characteristics of the ideal voltage waveform of three balanced voltages and completing the mathematical manipulations as shown above, the last modified version of Fourier coefficient is given in (4.35) and (4.36).

$\forall\, k,p \in N$, $b_k=0$ and $a_{k=2p}=0$ (4.35)

$$a_{k=2p+1}=\frac{8}{\pi}\cos\left(k\frac{\pi}{6}\right)\int_{0}^{\pi/3}v_{ab}(\alpha)\cos\left(k\left(\frac{\pi}{6}+\alpha\right)\right)d\alpha \quad (4.36)$$

All even harmonics are intrinsically null. Equation (4.36) clearly indicates that all triple harmonics are also null. The inverter's output voltage will only contain the remaining non

triple odd harmonics that can be eliminated by adjusting the switching angles $\alpha_i$ which will be shown and discussed in the next section.

## 4.5 Switching Angles Determination

This section will show the method to find the switching angles in the interval [0, $\pi/3$]. Two cases are being discussed and simulated:

1) In this thesis the first case if there is just one switching angle in the interval [0, $\pi/3$] as shown in Figure 4.6 (p.59);
2) The second one when there are three switching angles in the interval [0, $\pi/3$] as shown in Figure 4.7 (p.61).

The following subsections will describe each case in more details.

### 1) One switching angle in the interval [0, π/3]

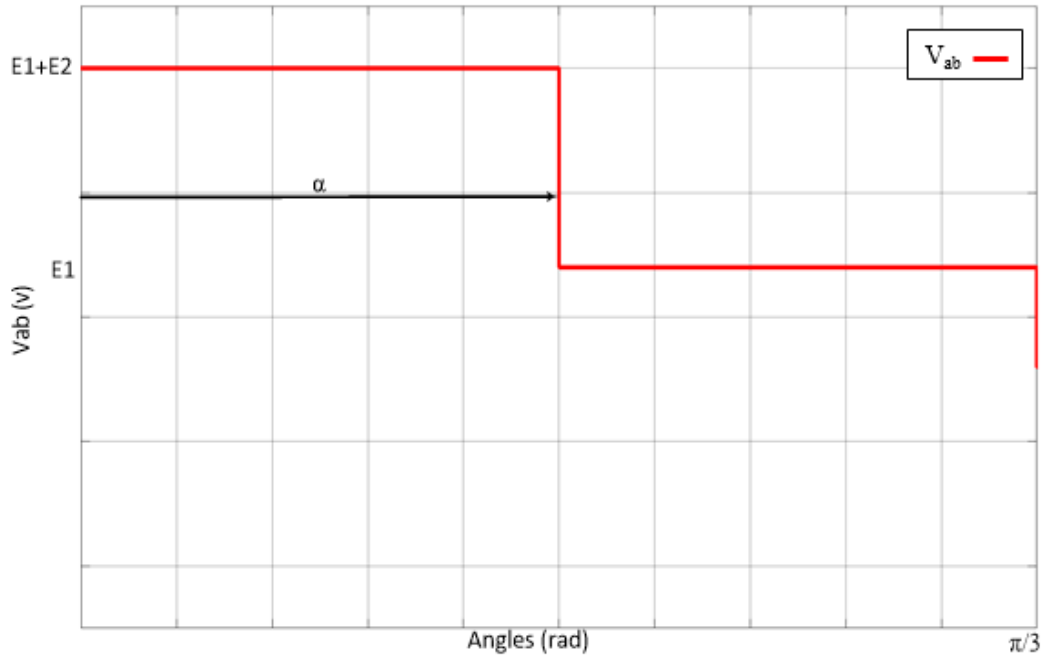



**Figure 4.6 Phase to phase voltage ($v_{ab}$) in [0, π/3] for one switching angle**

Start with using the modified Fourier coefficient in equation (4.36) (P.57) that has been found in the previous section for the ideal voltage waveform of three phase balanced voltages. Then, use this equation to find the switching angle "α" for $v_{ab}$ that is shown in Figure 4.6.

$$a_{k=2p+1} = \frac{8}{\pi}\cos\left(k\frac{\pi}{6}\right)\int_0^{\pi/3} v_{ab}(\alpha)\cos\left(k\left(\frac{\pi}{6}+\alpha\right)\right)d\alpha \qquad (4.37)$$

$$a_{k=2p+1} = \frac{8}{\pi}\cos\left(k\frac{\pi}{6}\right) \int_0^{\alpha} v_{ab}(\alpha)\cos\left(k\left(\frac{\pi}{6}+\alpha\right)\right)d\alpha + \frac{8}{\pi}\cos\left(k\frac{\pi}{6}\right) \int_{\alpha}^{\pi/3} v_{ab}(\alpha)\cos\left(k\left(\frac{\pi}{6}+\alpha\right)\right)d\alpha \quad (4.38)$$

Where $v_{ab}$=E1+E2 in the interval [0, α] and $v_{ab}$=E1 [α, π/3]. After plugging in these values, the Fourier coefficients of the inverter output voltage become as shown in Equation (4.39):

$$a_{k=2p+1} = \frac{8}{\pi}\cos\left(k\frac{\pi}{6}\right) \int_0^{\alpha} \mathrm{E1}+\mathrm{E2}\cos\left(k\left(\frac{\pi}{6}+\alpha\right)\right)d\alpha + \frac{8}{\pi}\cos\left(k\frac{\pi}{6}\right) \int_{\alpha}^{\pi/3} \mathrm{E1}\cos\left(k\left(\frac{\pi}{6}+\alpha\right)\right)d\alpha \quad (4.39)$$

Equation (4.39) indicates that all even harmonics, and all harmonics with a rank that is a multiple of three, are nulls. The inverter output voltage in the case of one switching angle in the interval [0, π/3] contains only harmonics that have an odd rank and does not increase by a factor of three. These harmonics can be eliminated by adjusting the switching angle α in the interval [0, π/3]. By considering the desired fundamental of the voltage output wanting to be 100% and eliminate the first two harmonics as shown in (4.40):

$$\begin{aligned} a_1 &= 1 \\ a_5 &= 0 \\ a_7 &= 0 \end{aligned} \quad (4.40)$$

The non-linear set of equations that are shown in Equations (4.39) and (4.40) can be solved by using an iterative method, such as Newton- Raphson. (MATLAB software has been used to solve the non-linear system in this thesis). The following Table presents the state of the switches of the inverter output voltage inverter for one switching angle.

**Table 4.3 State of power electronic switches for one switching angle**

| | $T_{aH}$ | $T_{bH}$ | $T_{cH}$ | $T_{aL}$ | $T_{bL}$ | $T_{cL}$ | $T_{a0}$ | $T_{b0}$ | $T_{c0}$ | $v_{ab}$ | $v_{ca}$ | $v_{bc}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| [0 α] | ON | OFF | OFF | OFF | OFF | ON | OFF | ON | OFF | 2E | -E | -E |
| [α π/3] | ON | OFF | OFF | OFF | ON | OFF | OFF | OFF | ON | E | -2E | E |

### 1) Three switching angles in the interval [0, π/3]

The inverter output voltage has three switching angles in the interval [0, π/3] in the second case, as shown in Figure 4.7.

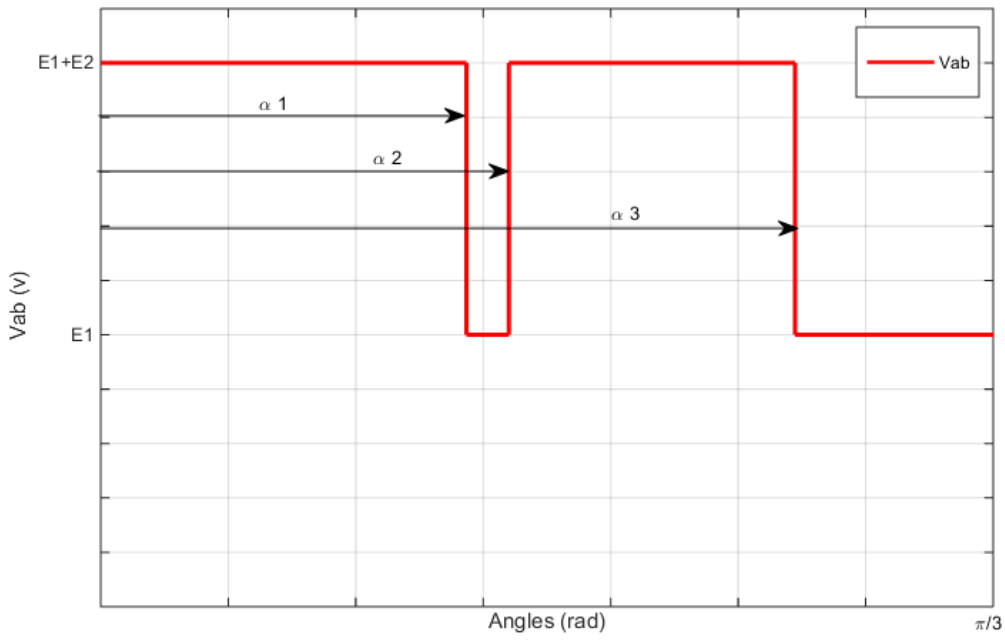



**Figure 4.7 Phase to phase voltage ($v_{ab}$) in [0, π/3] for three switching angles**

- Start again with using the modified Fourier coefficient in equation (4.36) (p.57) that has been found to adjust the switching angles $\alpha_1$, $\alpha_2$, and $\alpha_3$.for $v_{ab}$ that is shown in Figure 4.6.

$$a_{k=2p+1} = \frac{8}{\pi}\cos\left(k\frac{\pi}{6}\right) \int_0^{\pi/3} v_{ab}(\alpha)\cos\left(k\left(\frac{\pi}{6}+\alpha\right)\right)d\alpha$$

$$\begin{aligned} a_{k=2p+1} = {} & \frac{8}{\pi}\cos\left(k\frac{\pi}{6}\right) \int_0^{\alpha 1} v_{ab}(\alpha)\cos\left(k\left(\frac{\pi}{6}+\alpha\right)\right)d\alpha + \\ & \frac{8}{\pi}\cos\left(k\frac{\pi}{6}\right) \int_{\alpha 1}^{\alpha 2} v_{ab}(\alpha)\cos\left(k\left(\frac{\pi}{6}+\alpha\right)\right)d\alpha + \\ & \frac{8}{\pi}\cos\left(k\frac{\pi}{6}\right) \int_{\alpha 3}^{\pi/3} v_{ab}(\alpha)\cos\left(k\left(\frac{\pi}{6}+\alpha\right)\right)d\alpha \end{aligned} \quad (4.42)$$

In the following equations, $vab$=E1+E2 in the interval [0, $\alpha_1$], $v_{ab}$=E1 in [$\alpha_1$, $\alpha_2$], $v_{ab}$=E1+E2 in [$\alpha_2$, $\alpha_3$] and $v_{ab}$=E1 in [$\alpha_3$, $\pi/3$]. After plugging in these values, the Fourier coefficients of the inverter output voltage in the case of three switching angles is shown in Equation (4.42):

$$a_{k=2p+1} = \frac{8}{\pi}\cos\left(k\frac{\pi}{6}\right) \int_0^{\pi/3} \mathrm{E1} + \mathrm{E2}\cos\left(k\left(\frac{\pi}{6}+\alpha\right)\right)d\alpha$$

$$\begin{aligned} a_{k=2p+1} = {} & \frac{8}{\pi}\cos\left(k\frac{\pi}{6}\right) \int_0^{\alpha 1} \mathrm{E1}\cos\left(k\left(\frac{\pi}{6}+\alpha\right)\right)d\alpha + \\ & \frac{8}{\pi}\cos\left(k\frac{\pi}{6}\right) \int_{\alpha 1}^{\alpha 2} \mathrm{E1}+\mathrm{E2}\cos\left(k\left(\frac{\pi}{6}+\alpha\right)\right)d\alpha + \\ & \frac{8}{\pi}\cos\left(k\frac{\pi}{6}\right) \int_{\alpha 3}^{\pi/3} \mathrm{E1}+\mathrm{E2}\,(\alpha)\cos\left(k\left(\frac{\pi}{6}+\alpha\right)\right)d\alpha \end{aligned} \quad (4.42)$$

From equation (4.42) it can be seen that all even harmonics, and all harmonics with a rank that is a multiple of three are nulls. The inverter output voltage in the case of three switching angles contains only harmonics with an odd rank and does not increase by a factor of three These harmonics can be eliminated by adjusting the switching angles $\alpha_1$, $\alpha_2$, and $\alpha_3$ in the interval [0, $\pi$/3]. By considering the desired fundamental of the voltage output to be 100% and eliminating the first two harmonics as shown in (4.40) (p.60):

$$\begin{aligned} a_1 &= 1 \\ a_5 &= 0 \\ a_7 &= 0 \end{aligned} \qquad (4.40)$$

Solving the non-linear set of equations that are shown in (4.40) and (4.42) can be solved by using an iterative method such as Newton- Raphson (again MATLAB software has been used to solve the non-linear set in this thesis). The first and second non-zero harmonic ranks are D1 = 3M +2 and D2 = 3M+4, respectively. Where M is the number of switching angles in [0, $\pi$/3]. The following Figure 4.8 shows the inverter output voltage for three switching angles and describe the relationship between $\alpha$ and $\beta$. Where is $\beta$ has is defined in (4.43) and it used to describe the operation of the topology in the interval [0, $\pi$/3] for the case of switching angles as shown in Table 4.4.

$$\beta_i = \pi/_3 - \alpha_{3-i+1} \qquad (4.43)$$

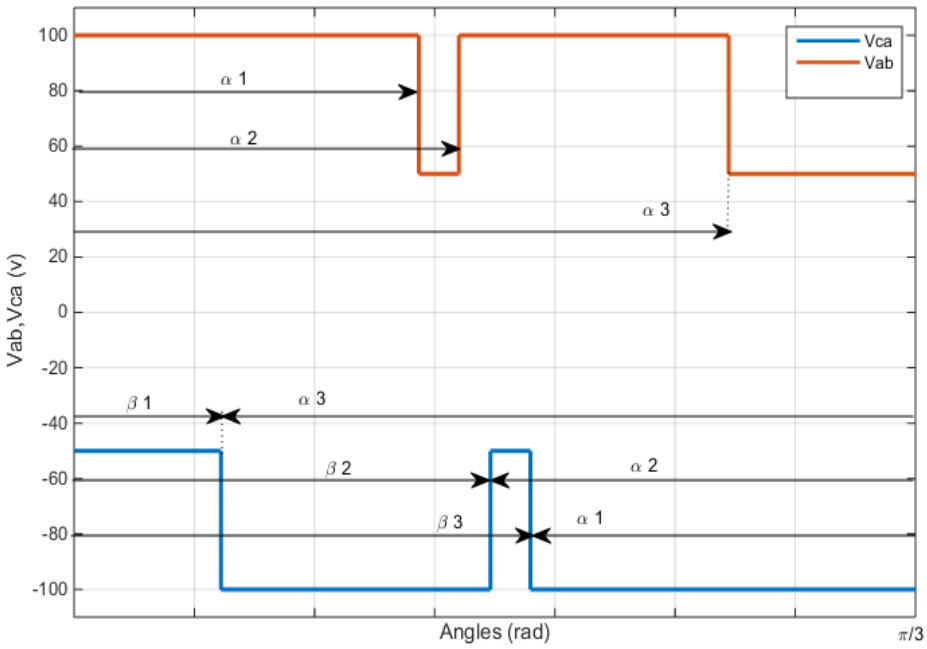



**Figure 4.8 Relationship between α and β in [0, π/3]**

**Table 4.4 State of power electronic switches for three switching angles**

| | $T_{aH}$ | $T_{bH}$ | $T_{cH}$ | $T_{aL}$ | $T_{bL}$ | $T_{cL}$ | $T_{a0}$ | $T_{b0}$ | $T_{c0}$ | $v_{ab}$ | $v_{ca}$ | $v_{bc}$ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| [0 β1] | ON | OFF | OFF | OFF | OFF | ON | OFF | ON | OFF | 2E | -E | -E |
| [$\beta_1$ $\beta_2$ ] | ON | OFF | OFF | OFF | OFF | OFF | OFF | ON | ON | 2E | -2E | 0 |
| [$\beta_2$ $\beta_3$ ] | ON | OFF | OFF | OFF | OFF | ON | OFF | ON | OFF | 2E | -E | -E |
| [$\beta_3$ $\alpha_1$ ] | ON | OFF | OFF | OFF | OFF | OFF | OFF | ON | ON | 2E | -2E | 0 |
| [$\alpha_1$ $\alpha_2$] | ON | OFF | OFF | OFF | ON | OFF | OFF | OFF | ON | E | -2E | E |
| [$\alpha_2$ $\alpha_3$] | ON | OFF | OFF | OFF | OFF | OFF | OFF | ON | ON | 2E | -2E | 0 |
| [$\alpha_3$ π/3] | ON | OFF | OFF | OFF | ON | OFF | OFF | OFF | ON | E | -2E | E |

## 4.6 Conclusion

A new three-phase, five-level multilevel inverter topology is being proposed and introduced in this chapter. The advantages and features of this topology is discussed and compared with other existing multilevel inverter topologies. The main advantages of the topology were, first of all the high output efficiency that makes the renewable energy sources more useable since one of the challenging in renewable energy is the losses when the energy is converted from DC to AC, and the second important advantage is the reduction in the number of the total required components which make it cheaper because in the savings in the components costs as was showed in a research study [78]. Also, a new modulation technique proposed is called pre-calculated switching angles in the interval [0 $\pi/3$]. It shows the mathematical derivation of the equation for the two cases, one switching angle and three switching angles, that have been discussed. The proposed modulation technique is to work with low frequency instead of higher ones as PWM works.

# CHAPTER 5

## *SIMULATION RESULTS AND ANYLASIS*

### 5.1 Introduction

The simulation results of the proposed three-phase, five-level inverter are explained and illustrated in this chapter. Furthermore, the proposed topology output results have been simulated using two different modulation techniques, the proposed modulation technique and the traditional PWM. This is done for the two cases (one switching angle and three switching angles) presented in Chapter 4 by computing the pre-calculated switching angles in the interval [0 $\pi$/3]. A comparison between the two cases with the two modulation techniques is also presented. All the simulations and results in this thesis have been done using a MATLAB simulation software, with ideal condition for the switches and diodes. This will never be the case in real-life implementation. Overshoots in the voltages will occur when a power diode is turned on according to [87]. On-state losses will also occur for both the diodes and switches.

### 5.2 Simulation Model of a Novel Three-Phase Five-Level Inverter

To verify the feasibility and advantages of the proposed topology, the novel three-phase five-level inverter with two DC inputs has been simulated using equal DC sources each at 50V based on the previous analysis and the proposed control technique that are shown in Chapter 4. Figure 5.18 (p.83) shows the topology model, built using MATLAB, using the pre-calculated modulation and Figure 5.3 shows the same topology using PWM. Another

set of simulations have been done for $E_1 = E_2 = 200V$ as an example to show that this topology is valid for any equal two DC sources.

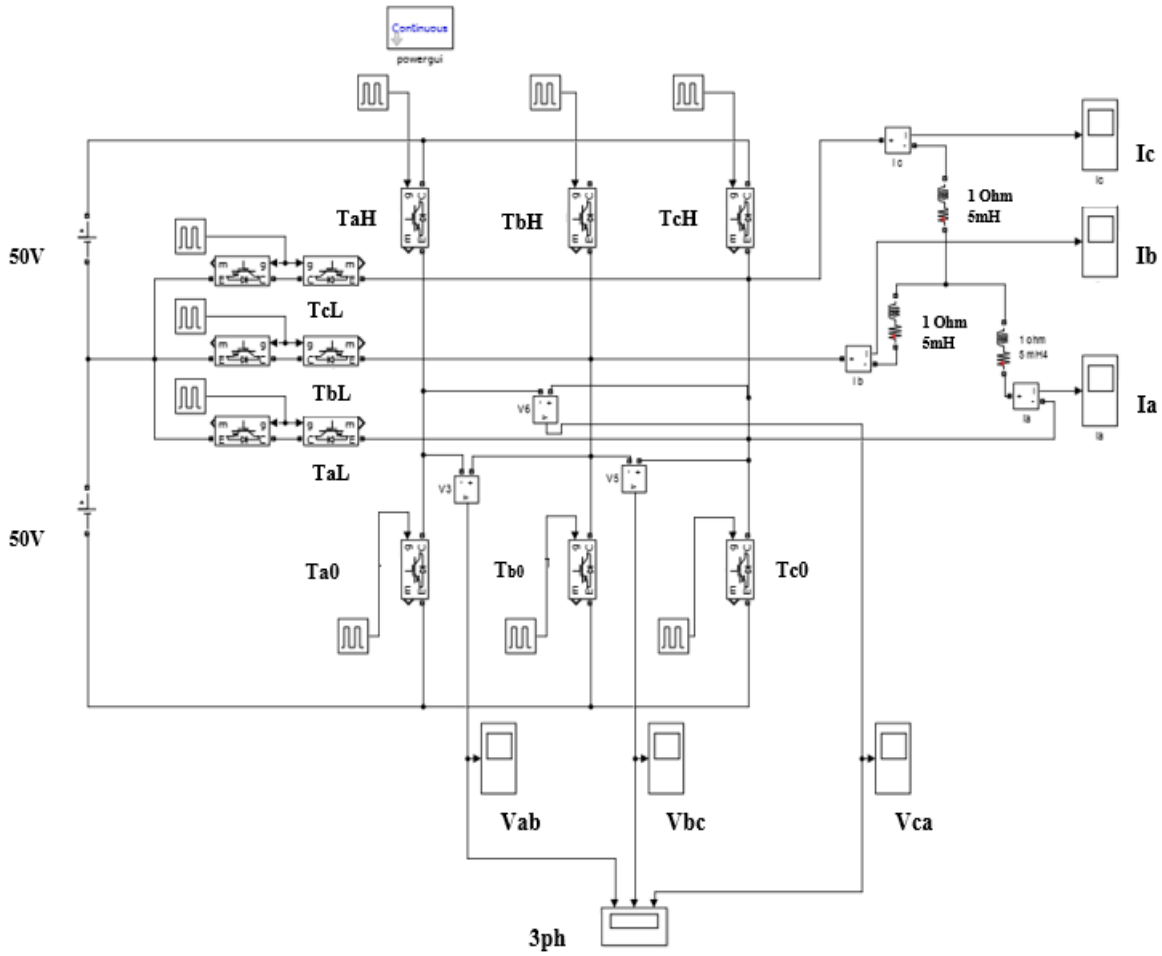



**Figure 5.1 The novel three-phase five-level topology MATLAB model with pre-calculated modulation**

## 5.3 Simulation Results for One Switching Angle

Starting the simulation processing with one switching angle "α" exists in the interval [0 π/3] as shown in Figure 4.5 (p.59). Using the developed Fourier coefficients of the inverter output voltage from Equation (4.39) (p.60) and by solving this non-linear

equation in MATLAB software to eliminate the $5^{th}$ for both cases with the fundamental equal to 1, the switching angle is:

$$\alpha = 42° \text{ OR } 0.733 \text{ rad} \quad (5.1)$$

### 5.3.1 The Switches Operation for One Switching Angle

The state (ON/OFF) of the novel three-phase, five-level inverter switches are shown in Figures 5.2a, 5.2b and 5.2c after using the proposed pre-calculated switching angles method. The Figures show that by taking $V_{ab}$ as an example when the switches $T_{aH}$ and $T_{b0}$ are ON, the voltage output $V_{ab}$ will be $V_{ab}$ =2E=100V. When the switches $T_{aH}$ and $T_{bL}$ are ON the voltage output $V_{ab}$ will be $V_{ab}$ =$E_2$=100V or $V_{ab}$ =$E_1$=100V when $T_{a0}$ and $T_{bL}$ are ON. When the switches $T_{a0}$ and $T_{b0}$ are ON the voltage output $V_{ab}$ will be $V_{ab}$ = 0V. By using the same method $V_{bc}$ and $V_{ca}$ can be obtained in the inverter voltage output.

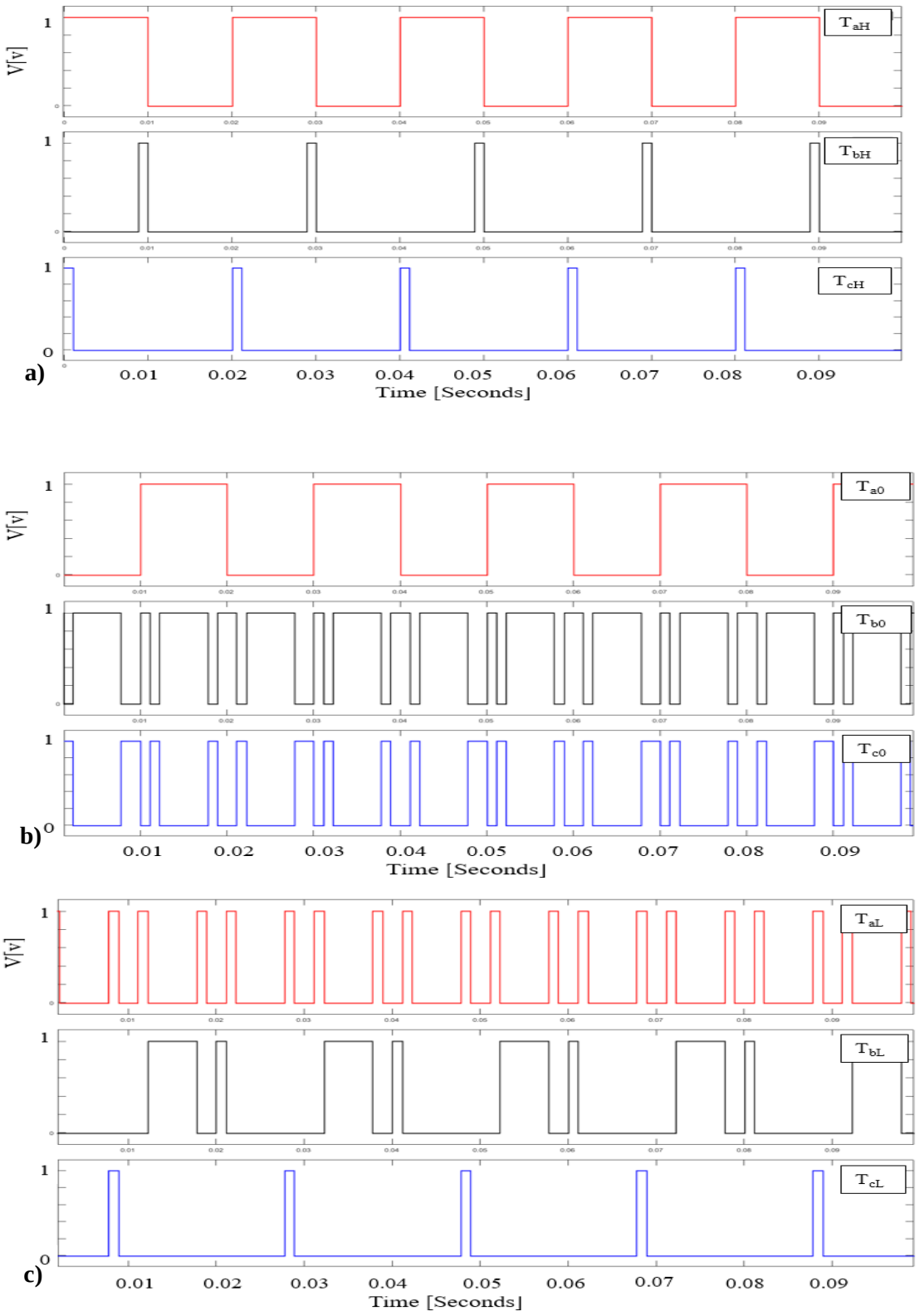



**Figure 5.2 Operation of the switches for one switching angle: a) $T_{aH}$, $T_{bH}$ and $T_{cH}$, b) $T_{a0}$, $T_{b0}$ and $T_{c0}$, c) $T_{aL}$, $T_{bL}$ and $T_{cL}$**

### 5.3.2 The Inverter Output Results for One Switching Angle

The pre-calculated switching angles technique, explained in Chapter 4, is used for the novel one switching angle topology. The switching frequency is set at 60Hz and the load consists of a resistor with 1 Ohm and inductor with 5 mH. Figure 5.3 shows the voltage phase to phase $V_{ab}$ for one period of time and we can notice that there is one switching angle in the interval [0 π/3]. The five voltage levels output can be clearly noticed at 100V, 50V, 0V, -50V and -100V. Figure 5.4 is showing the phase to phase voltages $V_{ab}$, $V_{bc}$, $V_{ca}$ in the case of one switching angle, and Figure 5.5 is showing the three phase to phase voltage for one switching angle. Also it can be noticed from these figures that the output waveforms are close to the sinusoidal waveform which is always the desired waveform in all inverters. Figure 5.6 shows the result of the phase leg voltage where the three level voltages (2E, E, and 0) can be easily identified. The number of changes on the phase voltage between 2E, E and 0 in the interval [0,2π] is 5.

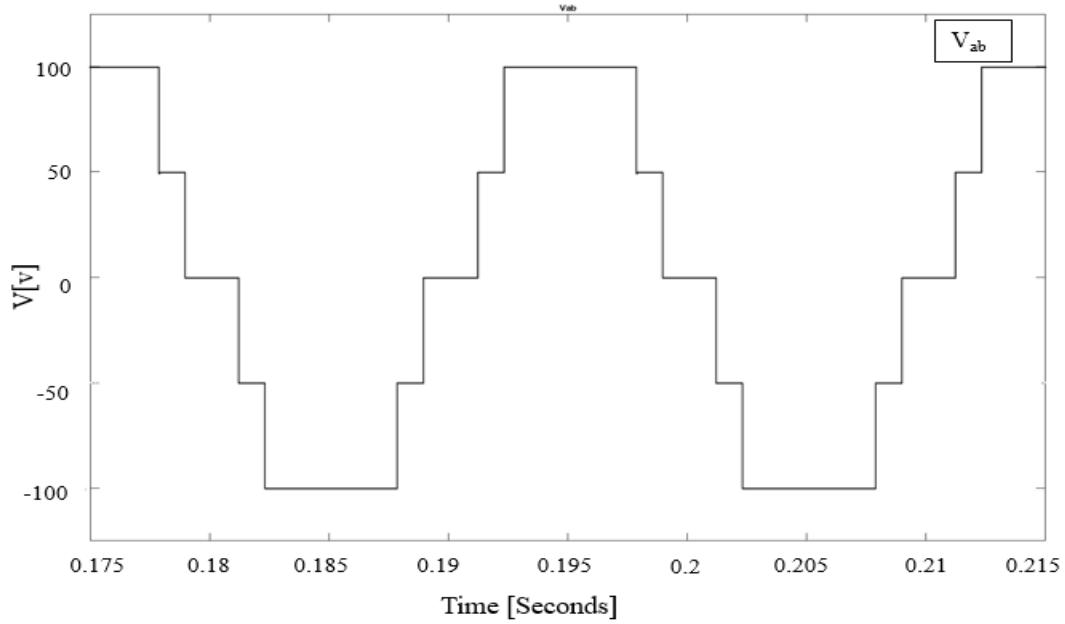



**Figure 5.3 The phase to phase $V_{ab}$ voltage in the case of one switching angle**

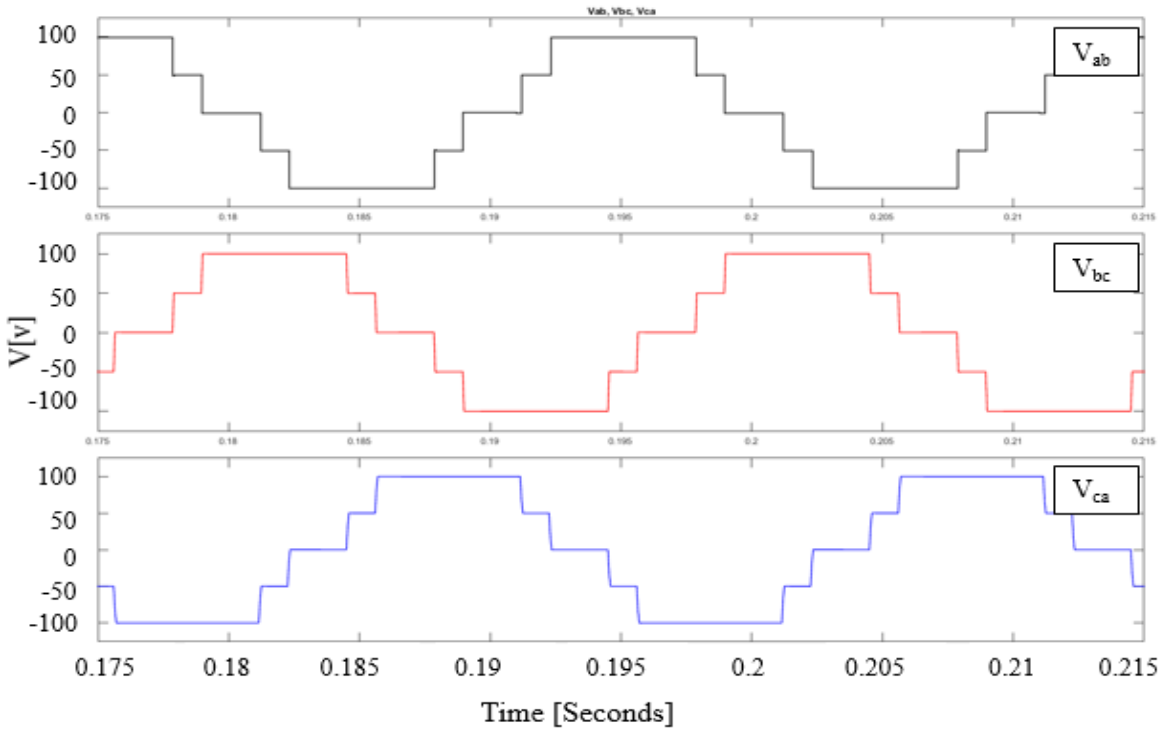



**Figure 5.4 The phase to phase voltages $V_{ab}$, $V_{bc}$, $V_{ca}$ in the case of one switching angle**

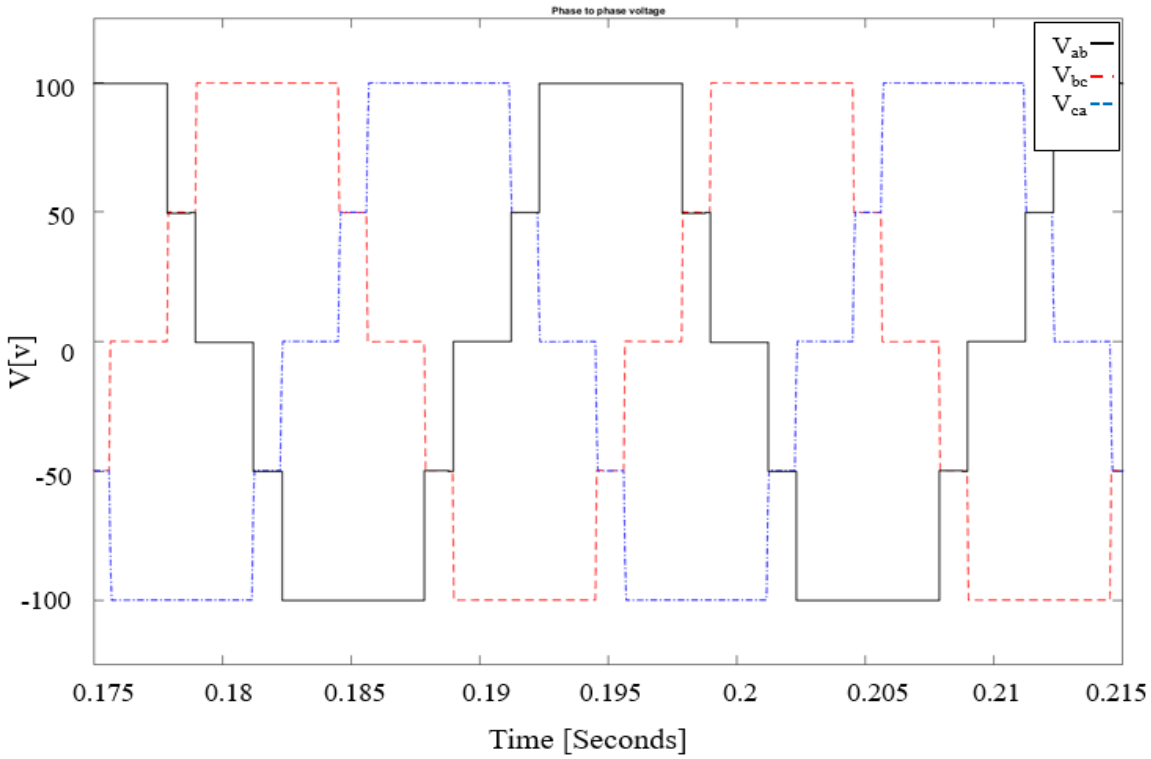



**Figure 5.5 The three phase to phase in the case of one switching angle**

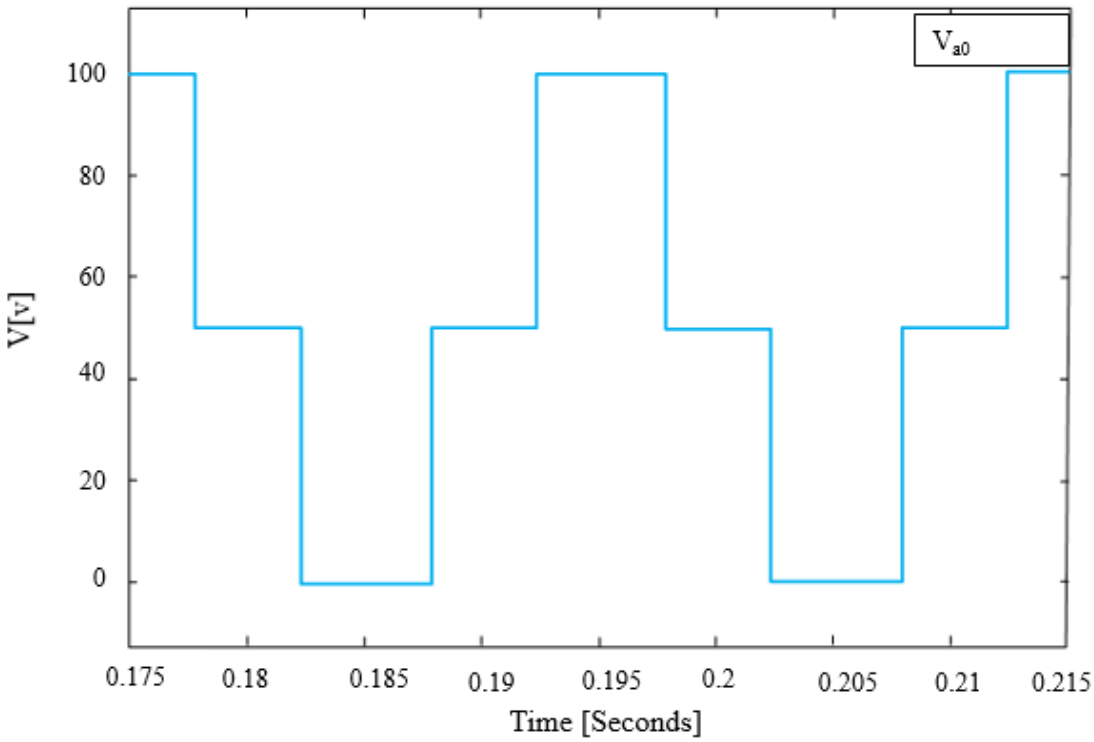



**Figure 5.6 The leg voltage $V_{a0}$ in the case of one switching angle**

The phase to phase current $I_{ab}$ is shown in Figure 5.7. The values of the current demonstrate the advantages of the proposed topology, as the desired current is obtained for the DC input 100V is 100% with a load of 1 Ohm and 5mH. The output results of the current is close to a sinusodial waveform. This indicates the proposed topology is very efficient.

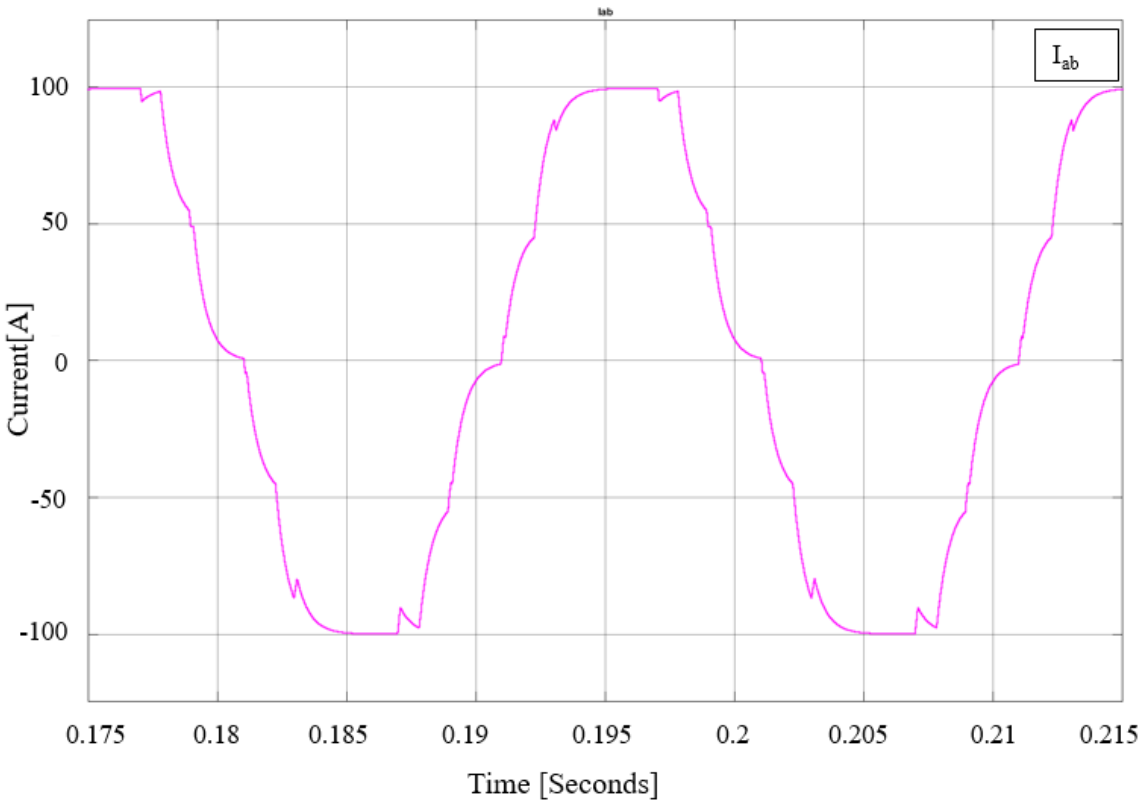



**Figure 5.7 The phase to phase current $I_{ab}$ in the case of one switching angle**

Harmonic analysis results of the phase to phase output voltage and the line current are shown in Figure 5.8 and 5.9 respectively for one switching angle. The analysis has been focused on the lower harmonic till $16^{th}$, because the lower harmonics are the most harmful for all electrical systems. The THD of the output voltage waveform is 19.13% and the amplitude of the the fundamental is 100 which is the inverter efficiency. The THD of the output current is 10.73%. The first nonzero harmonic is the $11^{th}$ and the zero harmonics are the $5^{th}$ and $7^{th}$. These harmonics were selected to be zero according to the proposed modulation techinque. The triple harmonics were canceled, because the inverter outputs a phase to phase voltage.

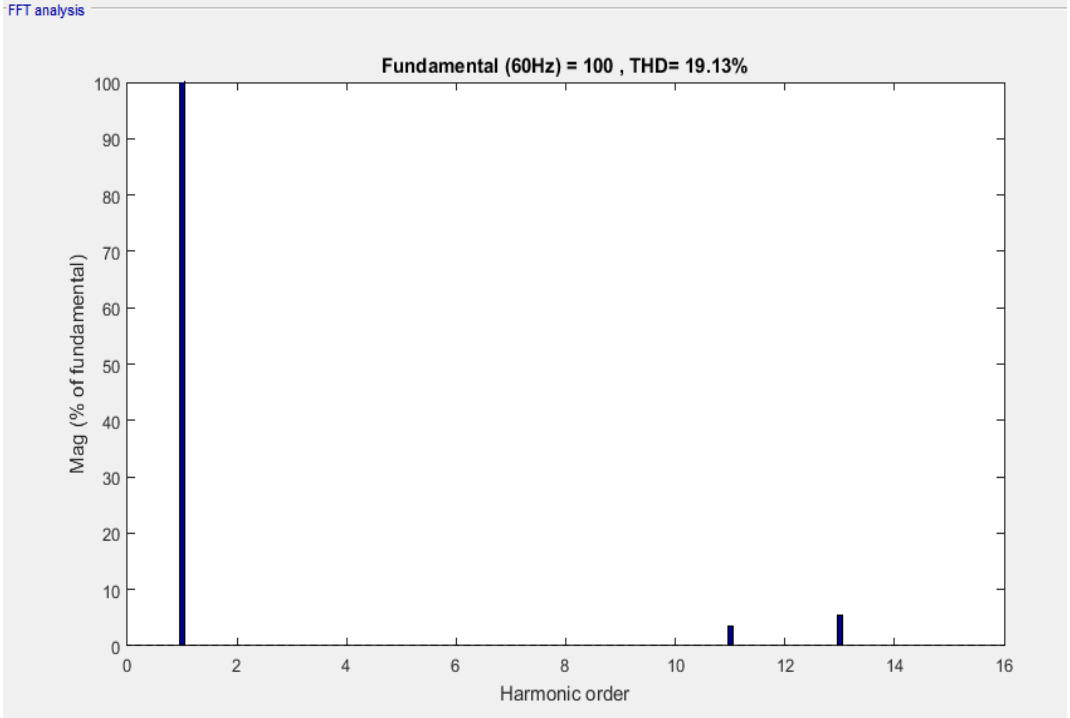



**Figure 5.8 The phase to phase voltage THD spectrum in the case of one switching angle**

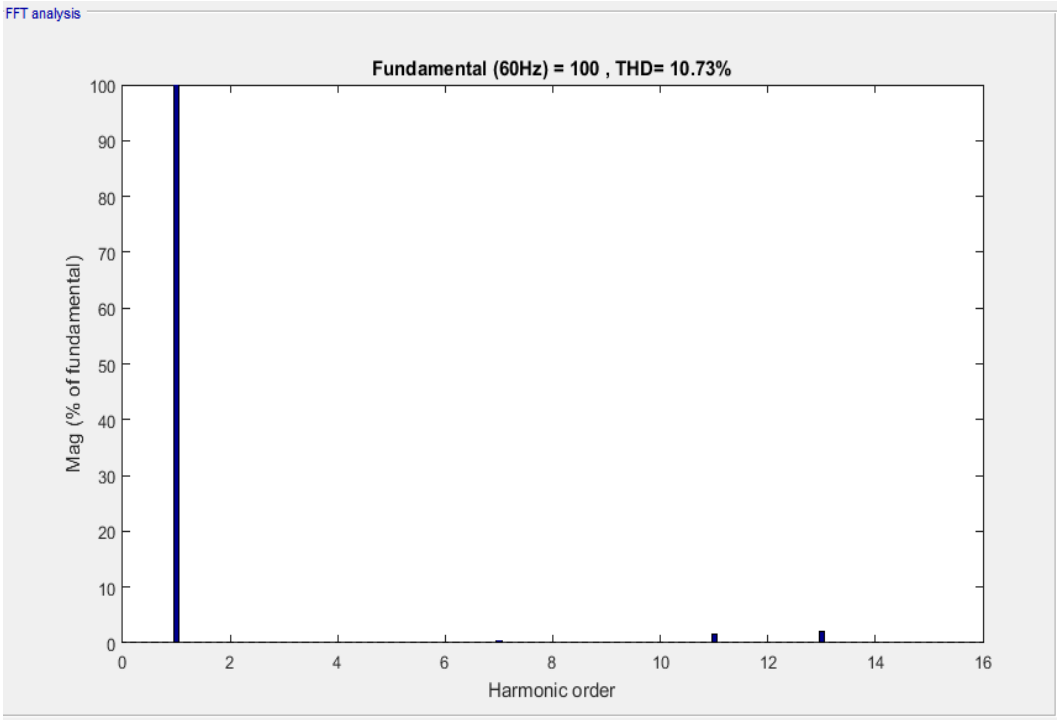



**Figure 5.9 The phase to phase current THD spectrum in the case of one switching angle**

### 5.4 Simulation Results for Three Switching Angles

This case of the inverter output voltage is simulated using the same MATLAB model in Figure 5.1 (p.67). In the case of three switching angles, the switching angles $\alpha_1$, $\alpha_2$ and $\alpha_3$ in the interval [0 $\pi$/3] make the inverter output voltage appear similar to the Figure 4.7 (p.61). Before starting simulating this case, the switching angles should be pre-calculated using the Fourier coefficients of the inverter output voltage from Equations (4.40) and (4.42) (p.60,62). By solving these non-linear equations in MATLAB software the pre-calculated switching angles will be ready to be inserted in the simulation model. The values of the switching angles are found to be:

$$\alpha_1=18.95° \text{ or } 0.33 \text{ rad} \quad (5.2)$$

$$\alpha_2=22.94° \text{ or } 0.4 \text{ rad} \quad (5.3)$$

$$\alpha_3=34.49° \text{ or } 0.602 \text{ rad} \quad (5.4)$$

According to the calculated values the following intervals are defined as:

$$\alpha_2 - \alpha_1 = 3.99° \text{ or } 0.069 \text{ rad} \quad (5.5)$$

$$\alpha_3 - \alpha_2 = 11.55° \text{ or } 0.201 \text{ rad} \quad (5.6)$$

$$\pi/3 - \alpha_3 = 25.51° \text{ or } 0.445 \text{ rad} \quad (5.7)$$

### 5.4.1 The Switches Operation for Three Switching Angles

The state (ON/OFF) of the novel three-phase, five-level inverter switches are shown in Figures 5.10a, 5.10b and 5.10c where they are the high input switches, the DC negative terminal bus switches, and the low input switches respectively. The operation of the switches is shown according the proposed pre-calculated switching angle method. The Figures show that by taking $V_{ab}$ as an example when the switches $T_{aH}$ and $T_{b0}$ are ON the voltage output $V_{ab}$ will be $V_{ab}$ =2E=100V. When the switches $T_{aH}$ and $T_{bL}$ are ON the voltage output $V_{ab}$ will be $V_{ab}$ =$E_2$=100V or $V_{ab}$ =$E_1$=100V. When $T_{a0}$ and $T_{bL}$ are ON, and when the switches $T_{a0}$ and $T_{b0}$ are ON the voltage output $V_{ab}$ will be $V_{ab}$ = 0V. By using this same method, $V_{bc}$ and $Vc_a$ can be obtained in the inverter voltage output.

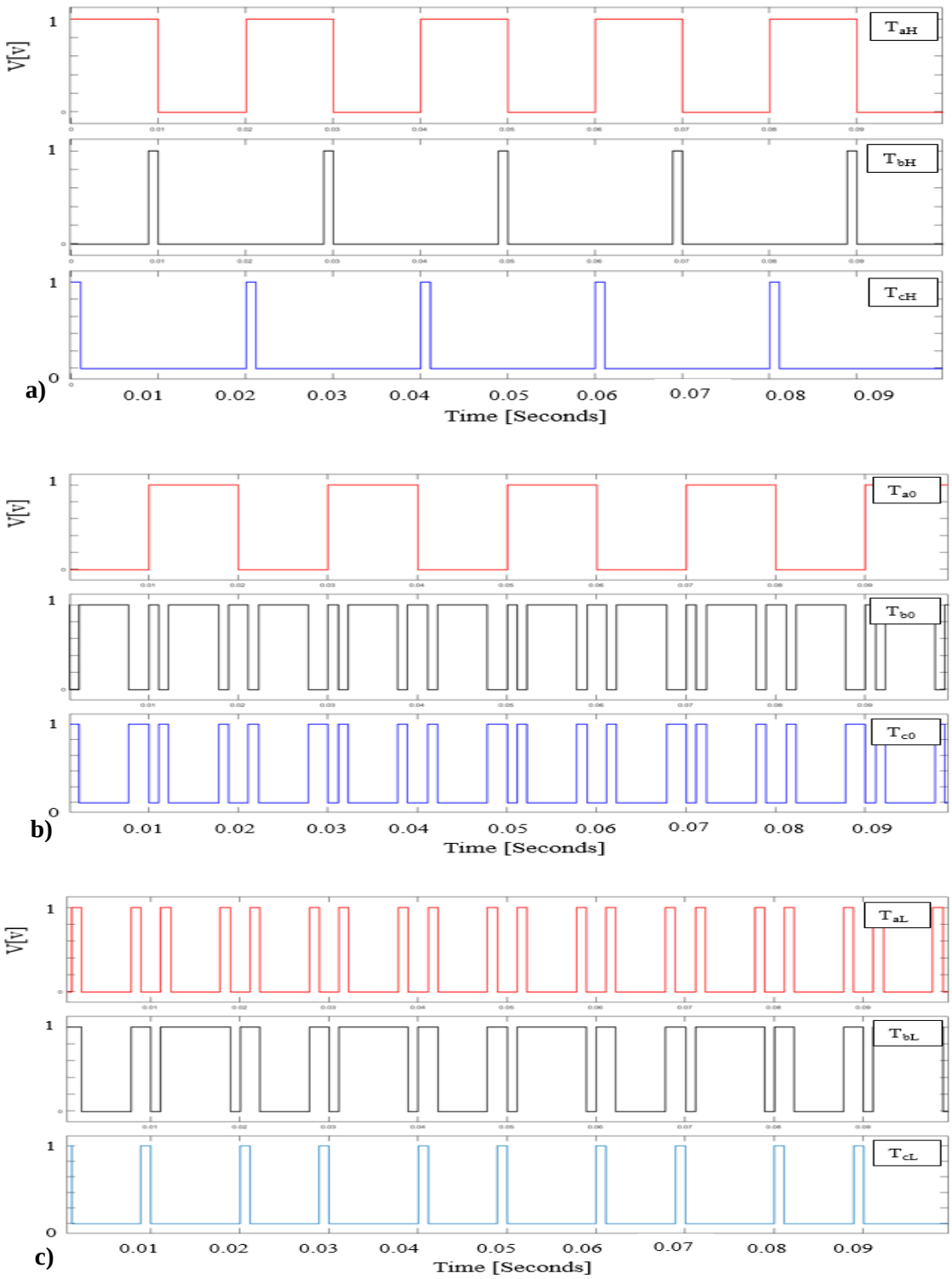



**Figure 5.10 Operation of the switches for three switching angles: a) $T_{aH}$, $T_{bH}$ and $T_{cH}$, b) $T_{a0}$, $T_{b0}$ and $T_{c0}$, c) $T_{aL}$, $T_{bL}$ and $T_{cL}$**

### 5.4.2 The Inverter Output Results for Three Switching Angles

The simulation for the case of three switching angles used the same switching frequency (60Hz as in the case of one switching angle), and the same load, which is a resistor with 1 Ohm and inductor with 5 mH. Figure 5.11 shows the voltage phase to phase $V_{ab}$ for one period of time and one can notice the three switching angles in the interval [0 $\pi/3$]. The five voltage level outputs can be clearly seen at 100V, 50V, 0V, -50V and -100V. Figures 5.12 and 5.13 depict the phase to phase voltages $V_{ab}$, $V_{bc}$, $V_{ca}$ for three switching angles, and the three phase to phase voltages for three switching angles. The output waveforms portrayed in these figures are close to the sinusoidal waveform, which is always the desired waveform in all inverters. Figure 5.14 shows the result of the phase leg $v_{a0}$ voltage where the three level voltages (2E, E, and 0) can be easily identified. The number of changes on the phase voltage between 2E, E and 0 in the interval [0,2$\pi$] is 12.

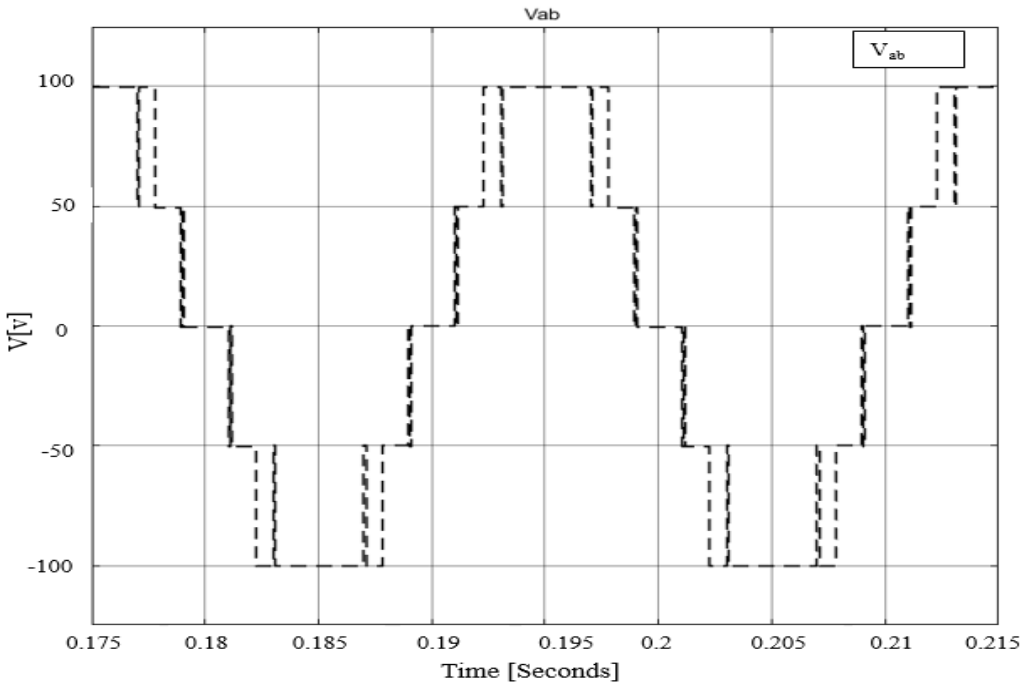



**Figure 5.11 The phase to phase $V_{ab}$ voltage in the case of three switching angles**

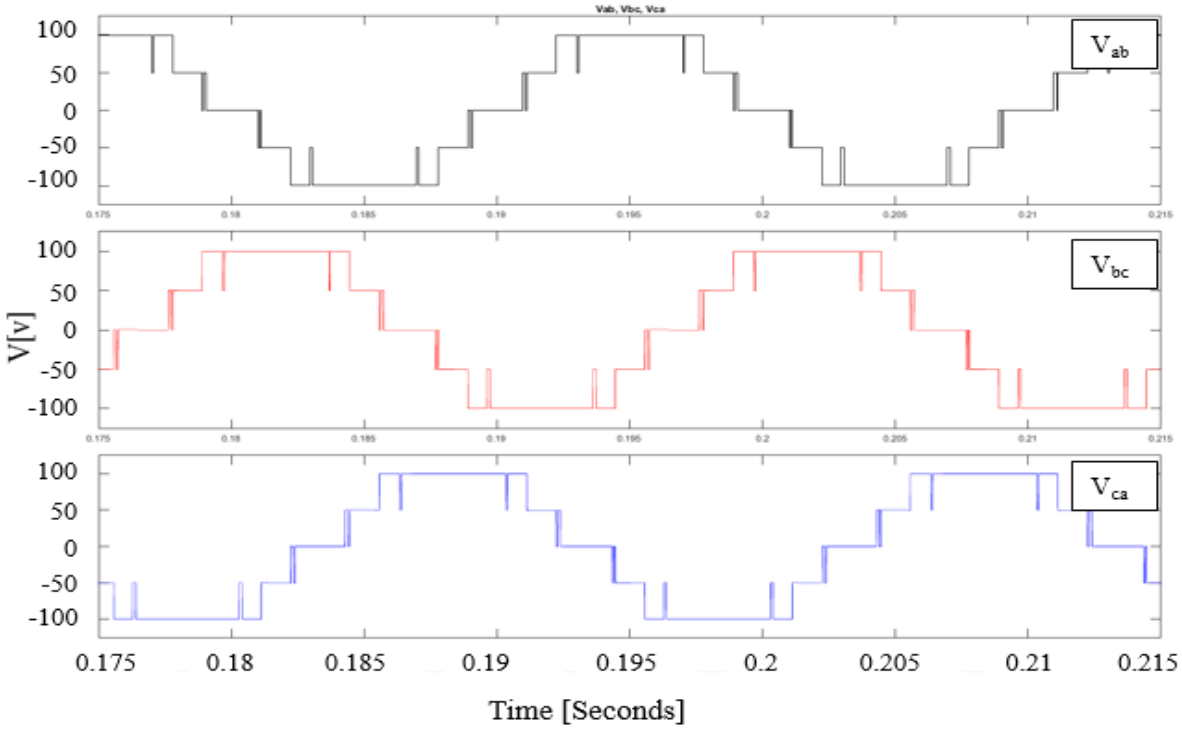



**Figure 5.12 The phase to phase voltages $V_{ab}$, $V_{bc}$, $V_{ca}$ in the case of three switching angles**

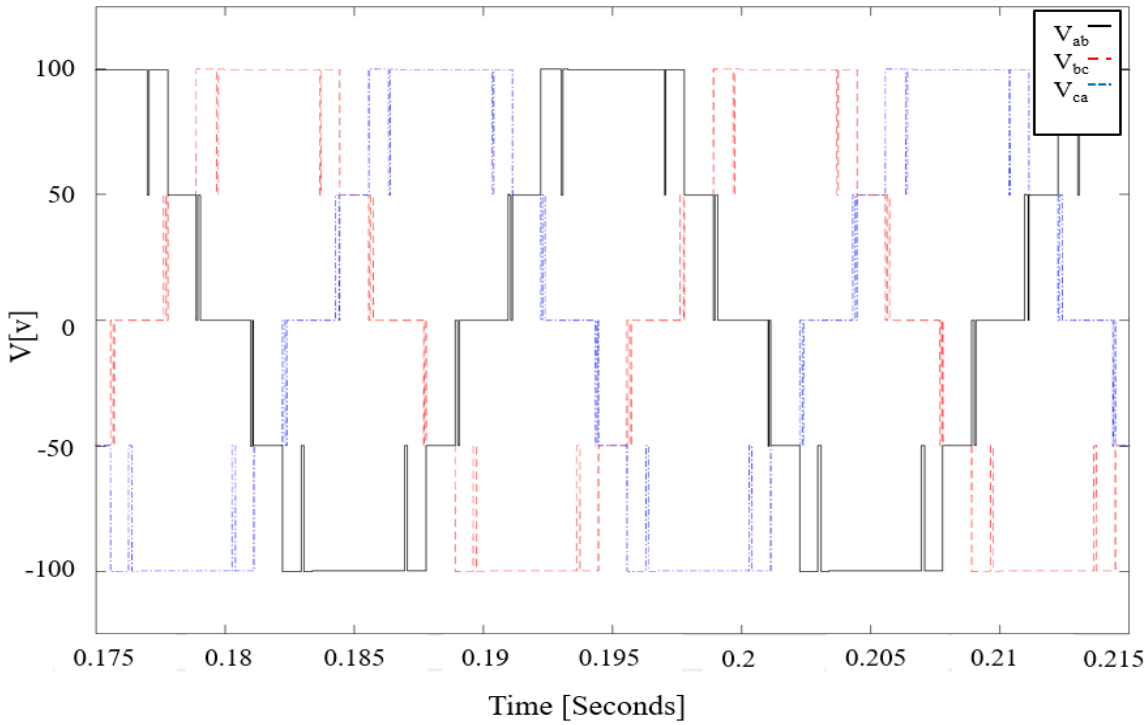



**Figure 5.13 The three phase to phase voltage in the case of three switching angles**

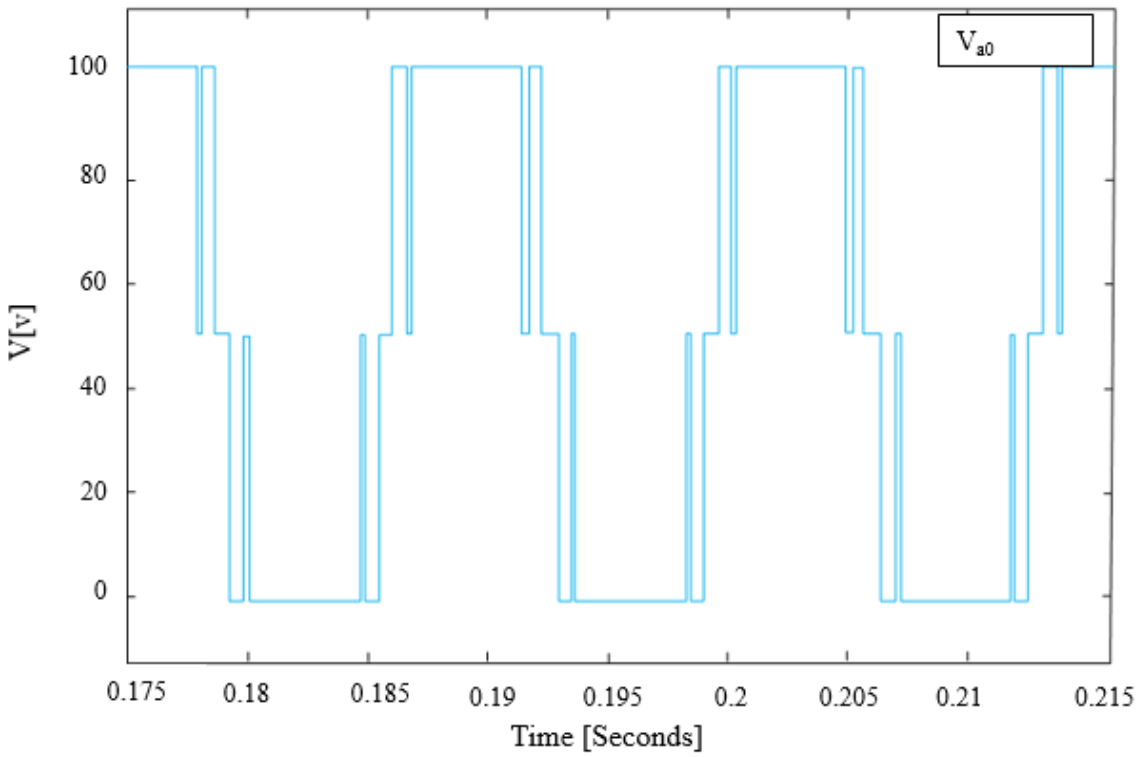



**Figure 5.14 The phase voltage $V_{a0}$ in the case of three switching angles**

Figure 5.15 shows the line current $I_{ab}$, note that the values of the current also demonstrates the advantages of the proposed topology, as the desired current is obtained for the DC input 100V is 100% with the same load of 1 Ohm and 5mH. The output results of the current is also close to a sinusodial waveform that suerly indicates a high efficiency of the proposed topology.

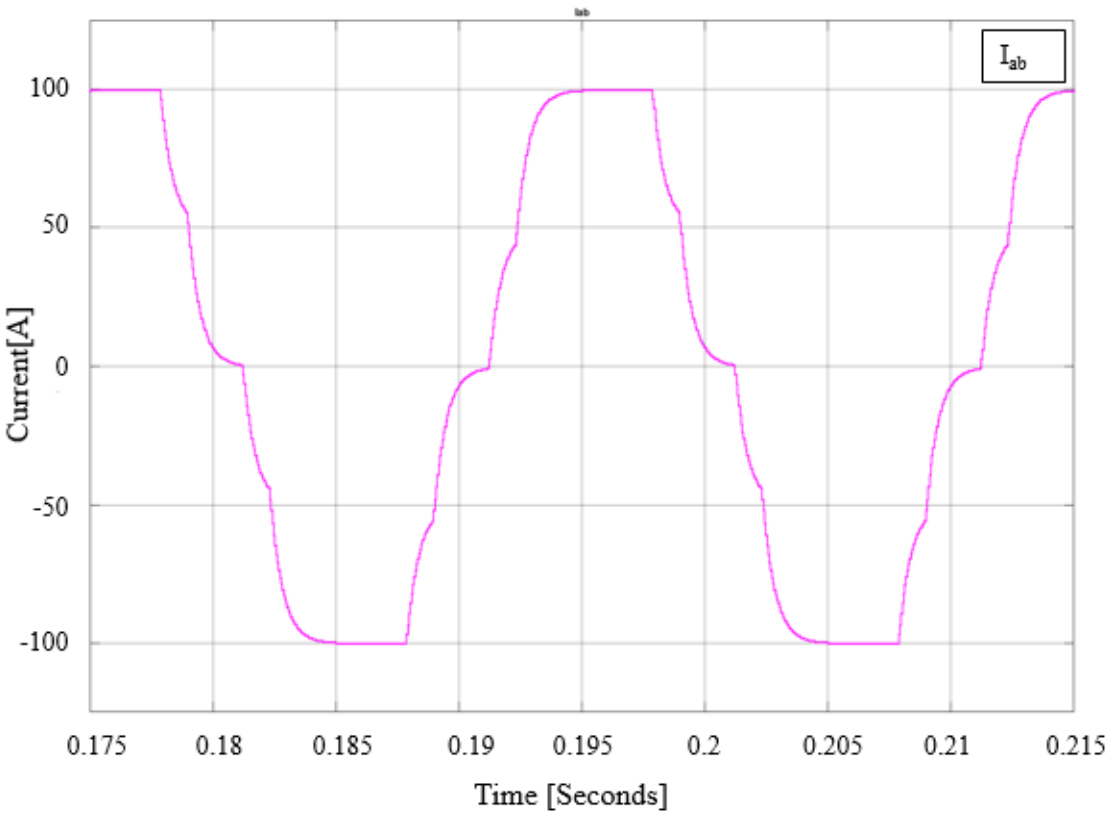



**Figure 5.15 The phase to phase current $I_{ab}$ in the case of three switching angles**

Figure 5.16 and 5.17 show the harmonic analysis results of the phase to phase output voltage and current respectly for three switching angles. The THD of the output voltage waveform is 18.11% and the amplitude of the the fundamental is 100%. The THD of the output current is 9.1%. The analysis also shows that the first nonzero harmonic is $11^{th}$ with, the $5^{th}$ and $7^{th}$ harmonics are zero which were selected to be zero according to the proposed modultion techinque. The simulation results for three switching angles indicate that they are much better than the case of one switching angle, because the lower THD values of voltage and current, so having three pre-calculated switching angles in the desired inverter output voltage that reduce the THD of the volatge as well as of the current.

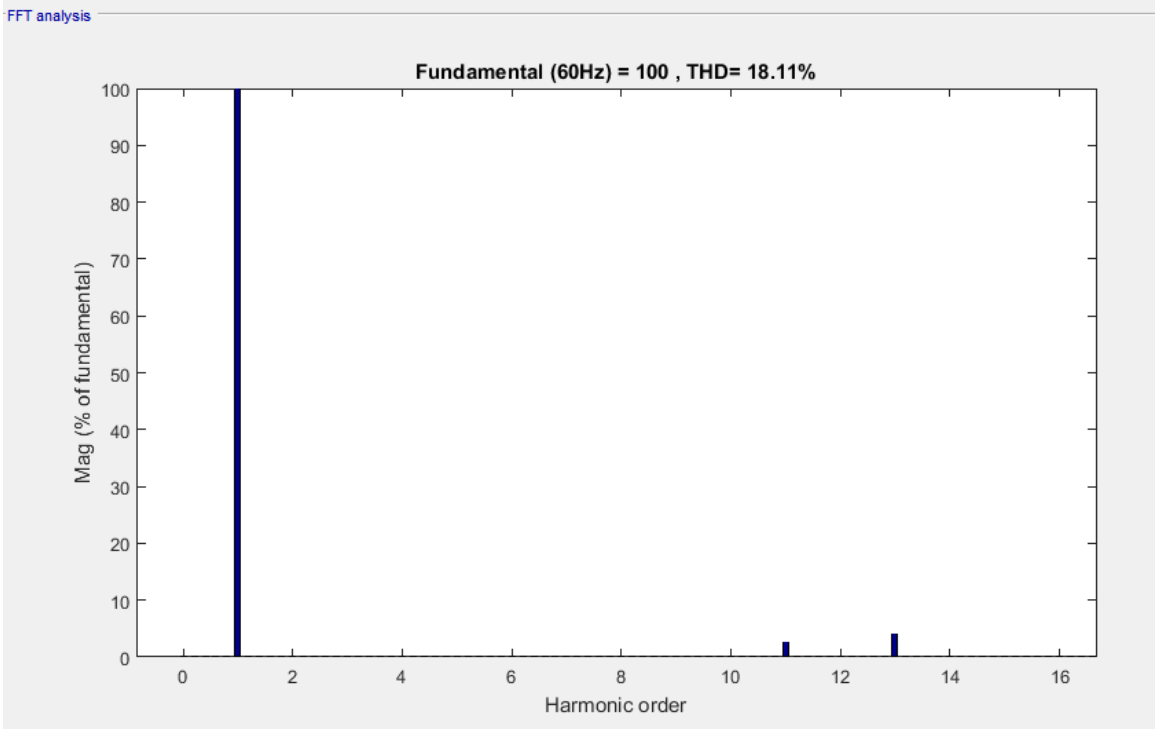



**Figure 5.16 The phase to phase voltage THD spectrum in the case of three switching angles**

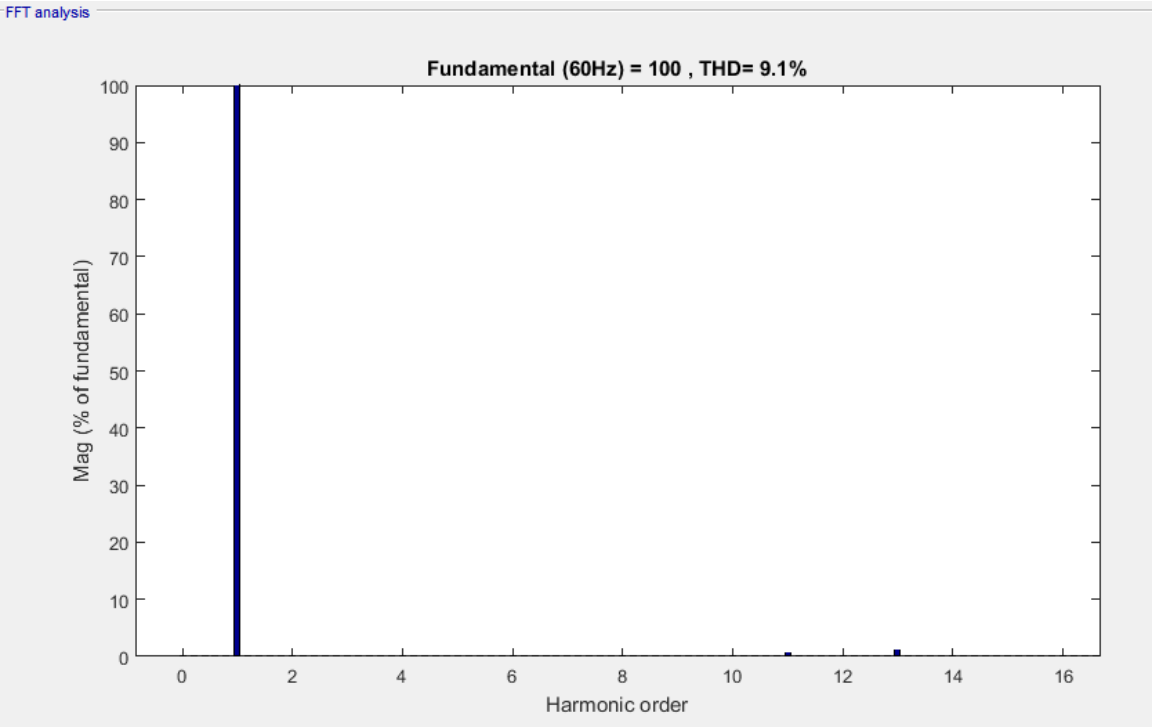



**Figure 5.17 The phase to phase current THD spectrum in the case of three switching angles**

## 5.5 Simulation Model of the Novel Three-Phase Five-Level Inverter using PWM

To demonstrate the benefits of using the pre-calculated switching angle method with the novel topology in comparison with the PWM, a MATLAB simulation was completed using PWM as shown in Fugure 5.18. PWM is one of the famous modulation techniques in power electronics and in this section a comparison is done between the inverter output results of the two cases (one switching angle and three switching angles) that discussed above, and for two different modulation controls.

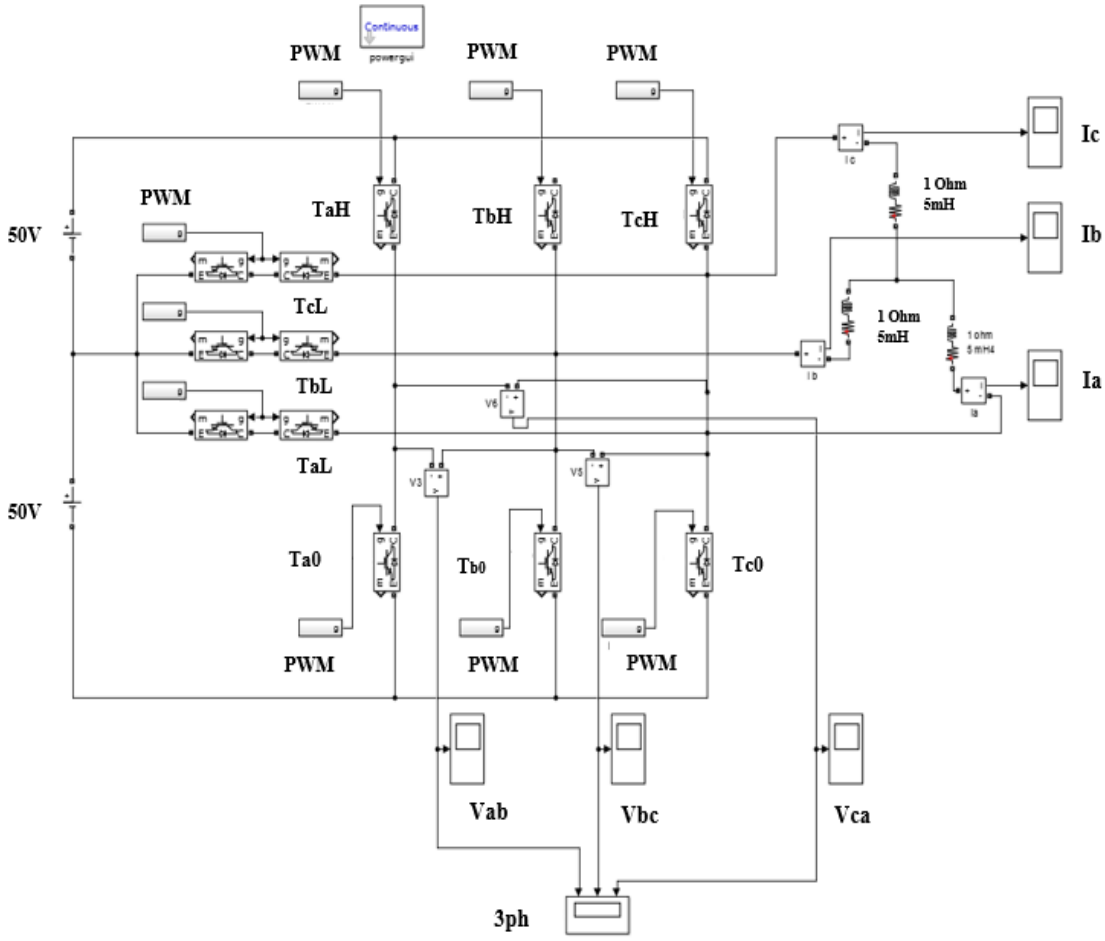



**Figure 5.18 The novel three-phase, five-level topology model using PWM**

### 5.5.1 Simulation Results of One Switching Angle and Three Switching Angles using PWM

In order to compare the proposed modulation with the traditional PWM modulation technique, a PWM control is used in the proposed topology. Obtaining the same inverter output voltage as shown in Figure 5.4 (p.71) and 5.12 (p.79) for one switching angle and three switching angles respectively, the switching frequency should be found. The number of switching between voltage levels (2E, E, 0) multiplied by the frequency will be the switching frequency of PWM [75].

Figure 5.6 (p.72) shows that the number of switching between the voltage levels is 5 and the frequency used is 60Hz, so The PWM switching frequency for one switching angle will be:

$$\text{The PWM Frequency} = 5*60 = 300\text{Hz} \qquad (5.8)$$

Figure 5.14 (p.80) also shows that the number of switching between the voltage levels is 12 and frequency was 60Hz, so the PWM switching frequency for three switching angles will be:

$$\text{The PWM Frequency} = 12*60 = 720\text{Hz} \qquad (5.9)$$

By starting the simulation for one switching angle with a frequency equal to 300Hz, and the operation of the switches as shown in Figure 5.19 (p.86), the inverter output will be roughly the same as in case of one switching angle, but the THD will not be the same as will be shown in the THD spectrums (p.92,93).

#### 5.5.1.1 The Switches Operation using PWM for One Switching Angle

To operate the topology with PWM control, a sine wave is used as a reference and triangle waves as carriers. PWM method uses high switching frequency carrier waves in comparison to the reference wave. For one switching angle a 300Hz triangle carrier waves are used with a sine reference wave to obtain the states of the topology switches that generate the five levels voltage in the output. Figures 5.19, 5.20 and 5.21 show the state of the switches, with Figure 5.19 showing the reference sine wave and the triangle carrier waves used to determine the operation of $T_{aH}$, $T_{bH}$ and $T_{cH}$ switches. Consider the Figure 5.19 as an example to explain the operation of the $T_{aH}$, $T_{bH}$ and $T_{Ch}$ switches. $T_{aH}$ will be in the ON state when the triangular carrier wave (red) is bigger than the reference sine wave (blue). $T_{bH}$ will be in the ON state when the reference sine wave (black) is bigger than the triangular wave (green), and $T_{cH}$ will be in ON state when the reference sine wave (black) is bigger than the triangular wave (pink). By using this same method, the operation of switches will be defined as shown in Figures 5.20 (p.87) and 5.21 (p.88).

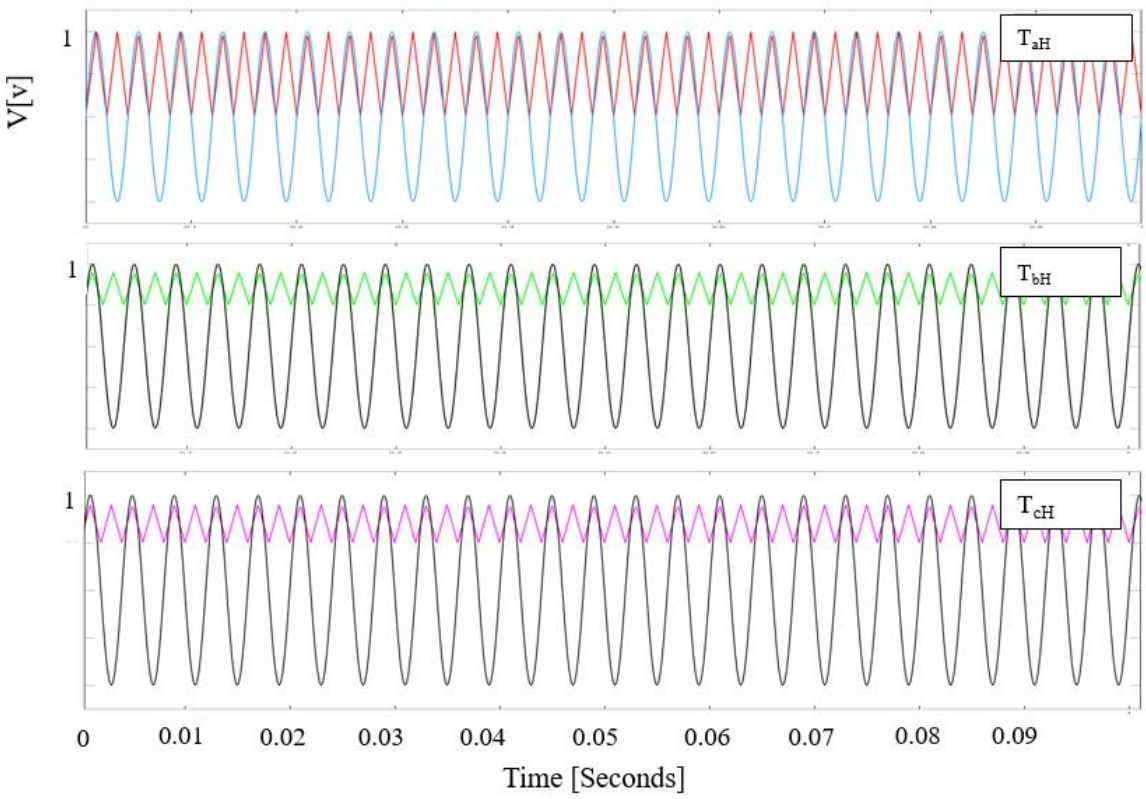



**Figure 5.19 PWM reference and triangular carrier waves that define the operation of the switches $T_{aH}$, $T_{bH}$, and $T_{cH}$ respectively for one switching angle**

Figure 5.20 shows that $T_{a0}$ will be ON when the reference sine wave (blue) is bigger the than triangular carrier wave (red). $T_{b0}$ will be ON when the reference sine wave (black) is bigger than the triangular wave1 (dashed green) and when the triangular wave2 (red) is bigger than the reference sine wave (black), $T_{c0}$ will operate the opposite way of $T_{b0}$.

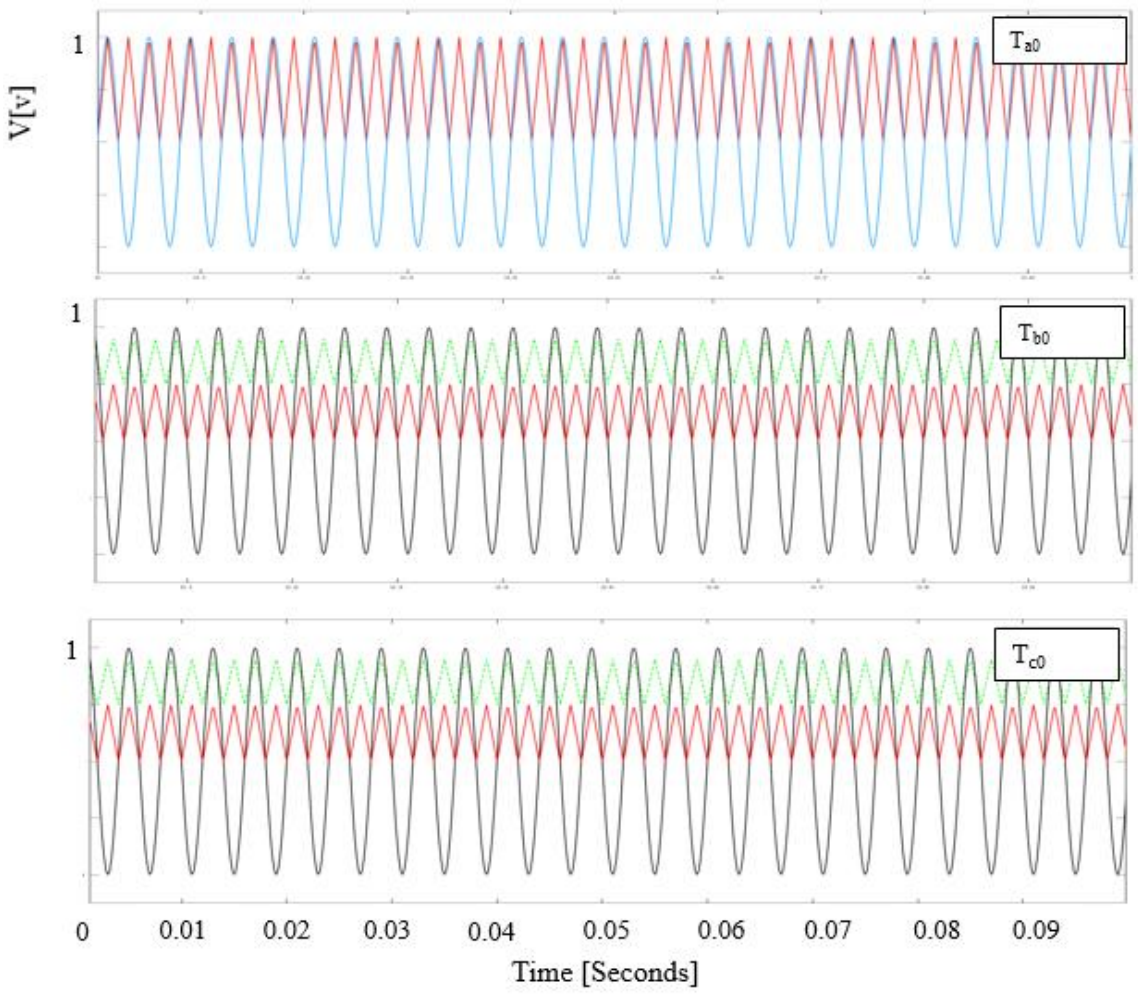



**Figure 5.20 PWM reference and triangular carrier waves that define the operation of the switches $T_{a0}$, $T_{b0}$, and $T_{c0}$ respectively for one switching angle**

Figure 5.21 shows the waves used to generate the switches operating with PWM. $T_{aL}$ will be turned ON when the reference sine wave (black) is bigger than the triangular carrier wave1 (dashed green), and when than triangular carrier wave2 (red) is bigger than the reference sine wave, $T_{bL}$ will be turned ON when the reference sine wave (black) is bigger than the triangular carrier wave1 (dashed green), and smaller than the triangular carrier wave2 (red). $T_{cL}$ will be turned ON when the reference sine wave (red) is bigger than the triangular carrier wave (dashed blue).

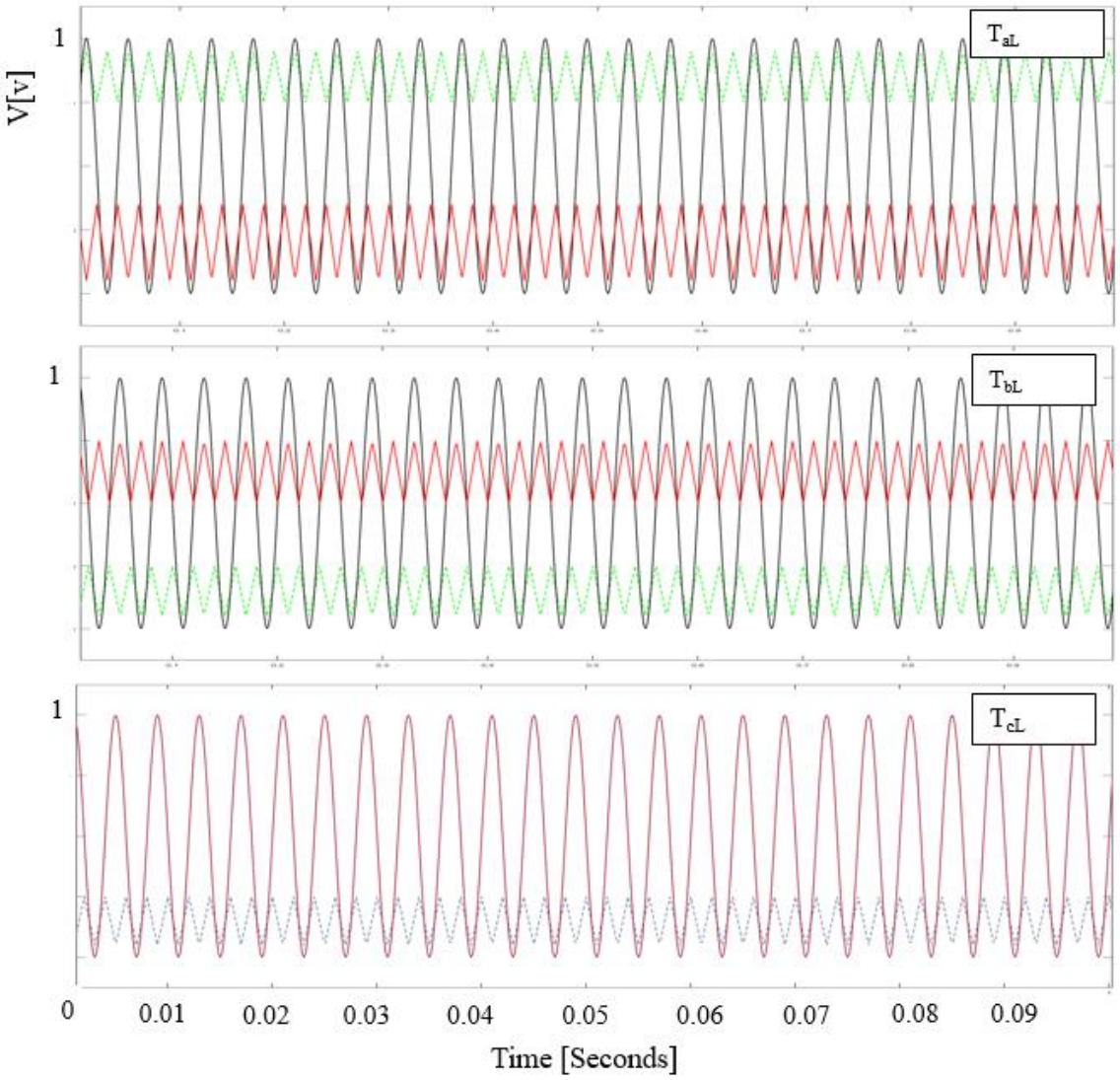



**Figure 5.21 PWM reference and triangular carrier waves that define the operation of the switches $T_{aL}$, $T_{bL}$, and $T_{cL}$ respectively for one switching angle**

#### 5.5.1.2 The Simulation Results using PWM for One Switching Angle

The results of using the PWM technique are shown in the following figures where the inverter phase to phase output voltage is less than 100V as shown in Figure 5.22 and still there are five level voltages.

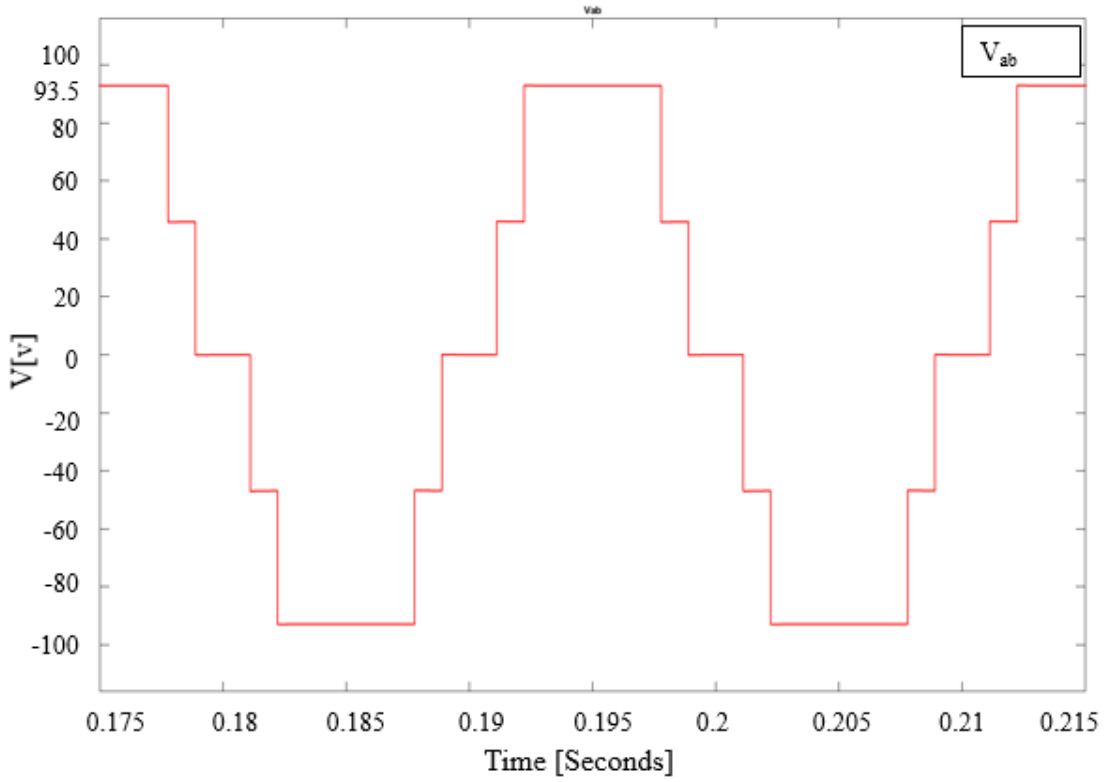



**Figure 5.22 The phase to phase $V_{ab}$ voltage for one switching angle using PWM**

In Figure 5.23 the phase to phase voltages $V_{ab}$, $V_{bc}$, $V_{ca}$ are shown still as a sinusoidal wave.

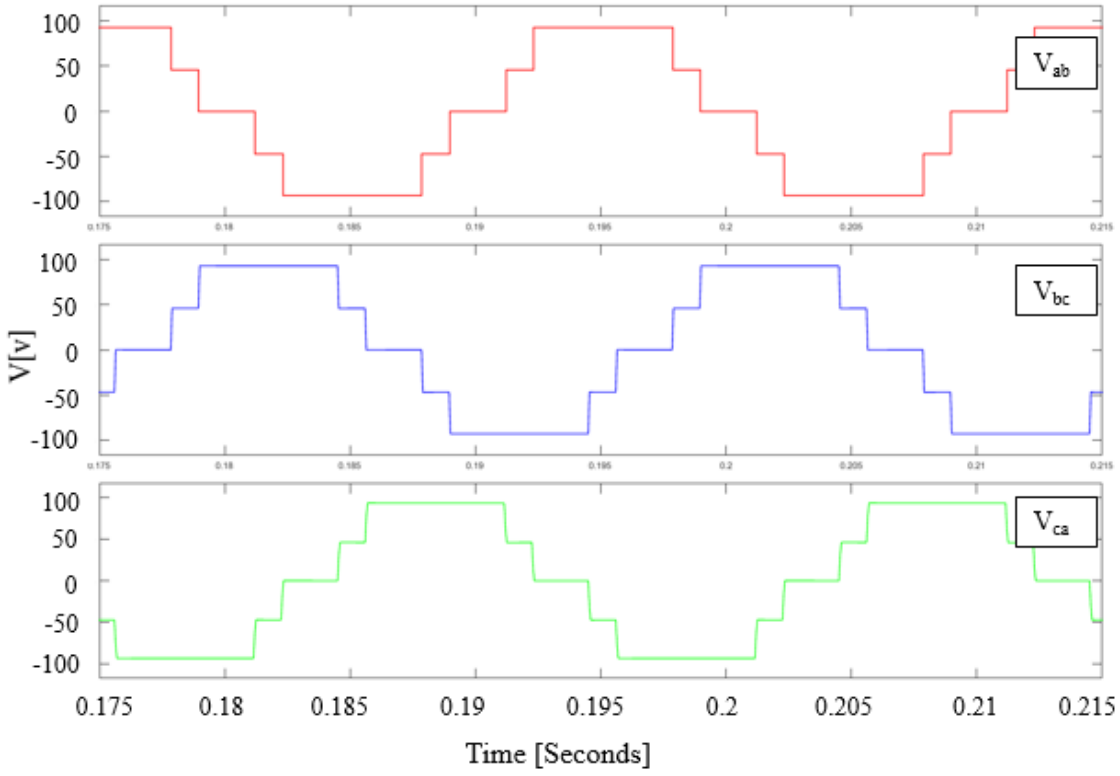



**Figure 5.23 The phase to phase voltages $V_{ab}$, $V_{bc}$, $V_{ca}$ for one switching angle using PWM**

Figure 5.24 shows the three phase to phase voltage in case of one switching angle with PWM, and Figure 5.25 shows line current for one switching angle with PWM. The phase to phase voltages and the line current still have a decent sinusoidal similar to the one shown for the same case with the proposed modulation technique. This means the topology can be operated using the PWM to have the same output waves with some different values of the voltage levels than the expected ones.

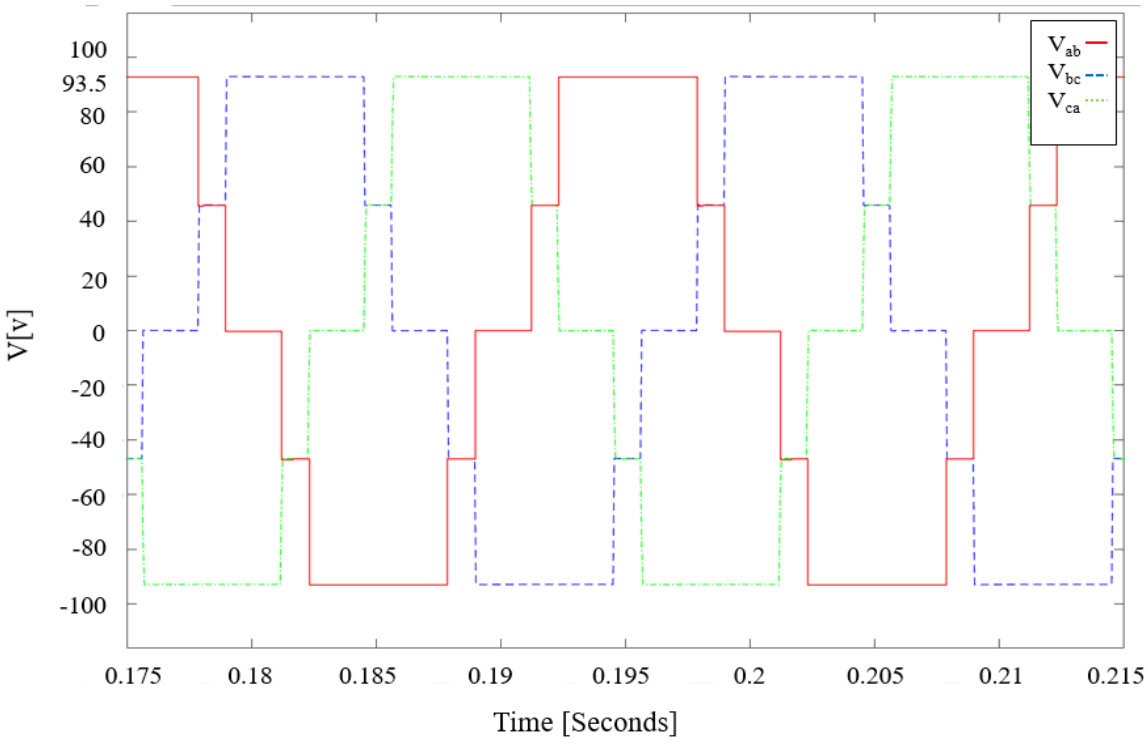



**Figure 5.24 The three phase to phase voltage for one switching angle using PWM**

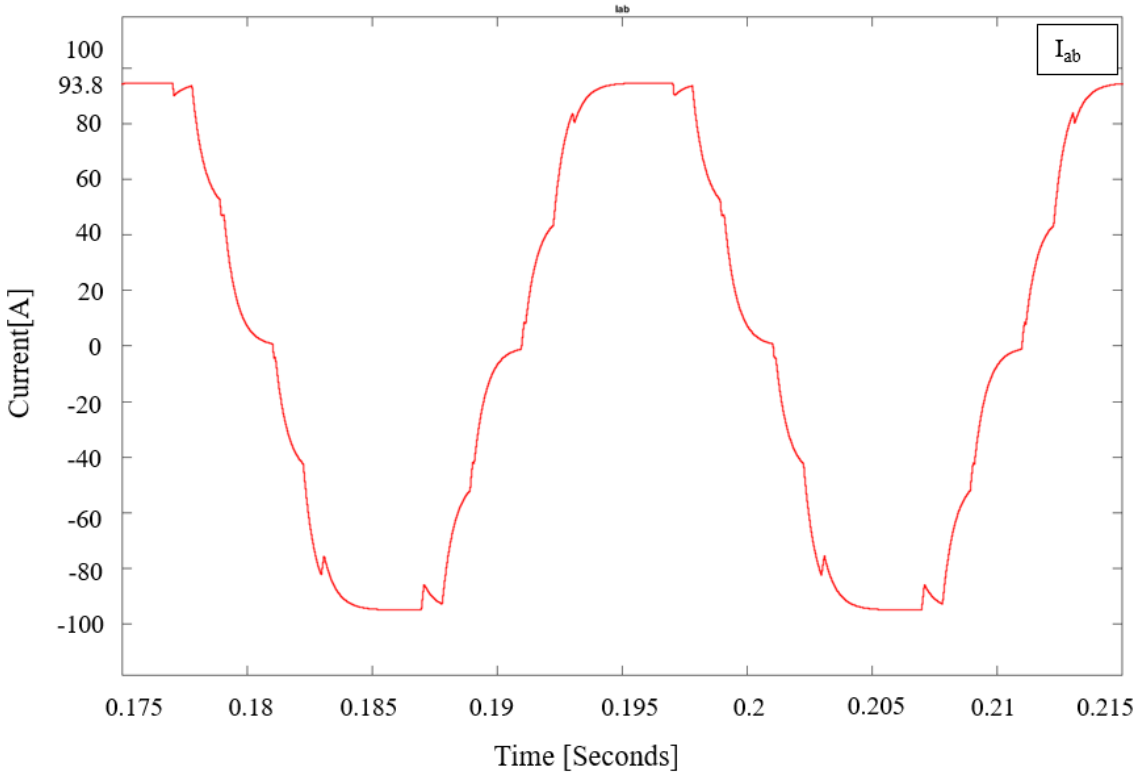



**Figure 5.25 The phase to phase current $I_{ab}$ for one switching angle using PWM**

The harmonic analyses for one switching angle with PWM technique are shown in Figures 5.26 and 5.27, for the phase to phase voltage and current respectively. The results do not seem to be very positive compared to using the proposed modulation technique. The harmonic spectrum for both the phase to phase voltage and current show that the $5^{th}$ and $7^{th}$ harmonics are very noticeable. The THD of phase to phase voltage was 27.1%. This is higher than the THD for the same case with the proposed modulation. The harmonic spectrum of the phase to phase current was 13.2%, which is also greater than the THD found using the proposed technique. This indicates the proposed modulation technique can be recommended to be used in this case to obtain better THD.

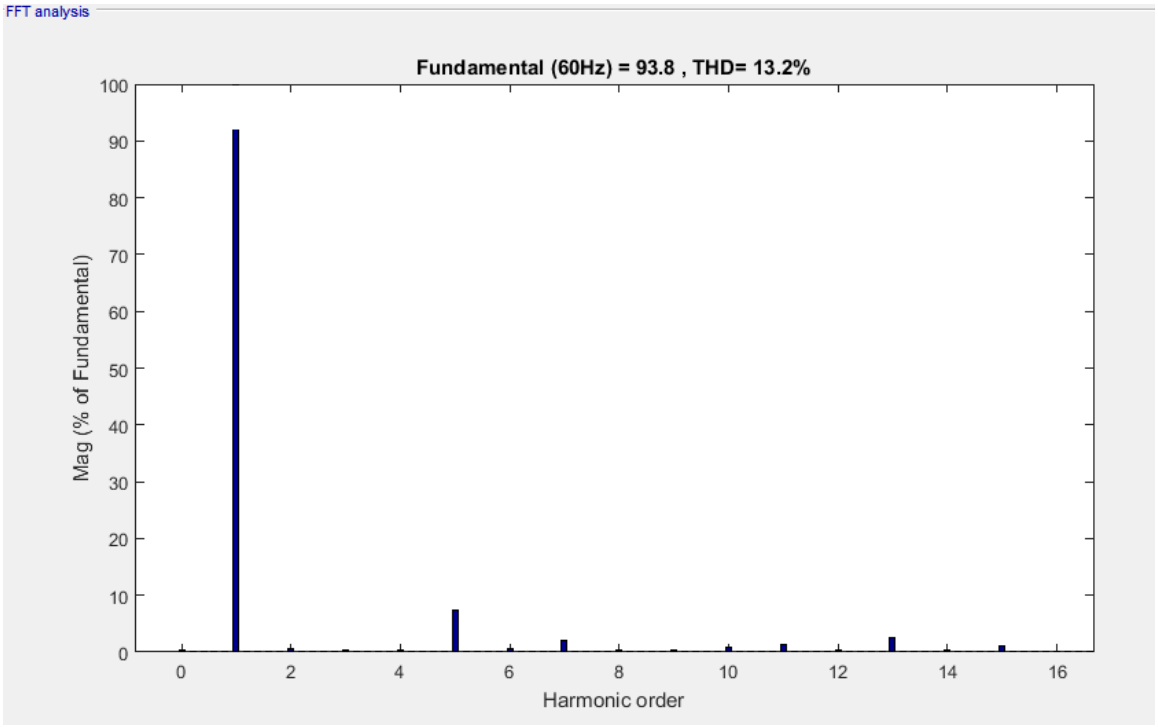



**Figure 5.26 The phase to phase current THD spectrum for one switching angle using PWM**

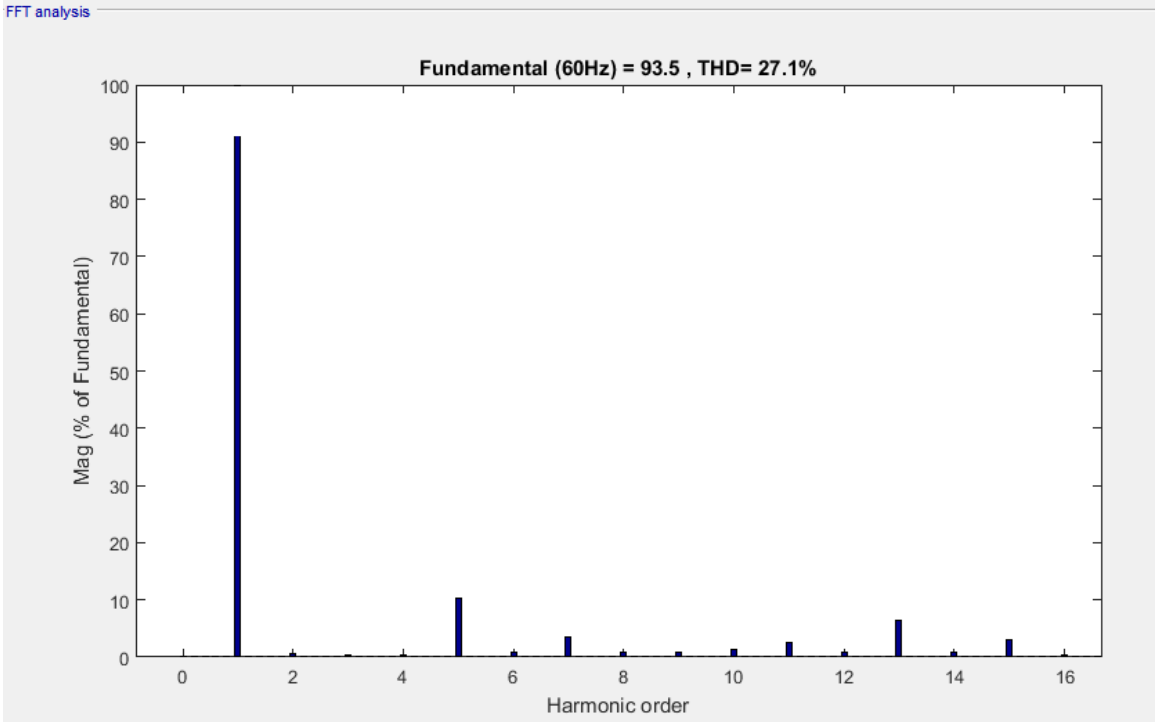



**Figure 5.27 The phase to phase voltage THD spectrum for one switching angle using PWM**

#### 5.5.1.3 The Switches Operation using PWM for Three Switching Angles

The case of three switching angles is also simulated by using PWM to find where the proposed topology works with PWM modulation. If modulation PWM works the simulation will show the difference in results for one switching angle in the previous section. The operation of the proposed topology with PWM control requires a sine wave as a reference wave, and triangle waves as carrier waves. The PWM method uses high switching frequency carrier waves in comparison to the reference wave. For three switching angles, 720Hz triangle carrier waves are used with a reference sine wave to

obtain the states of the topology switches that generate the five different level voltages in the output. The Figures 5.28, 5.29 and 5.30 show the state of the switches, where Figure 5.28 shows the reference sine wave and the triangle carrier waves that are used to determine the operation of $T_{aH}$, $T_{bH}$ and $T_{Ch}$, switches. The operation of the $T_{aH}$, $T_{Bh}$, and $T_{Ch}$ switches are depicted in Figure 5.28. $T_{aH}$ will be in ON state when the triangular carrier wave (red) is smaller than the reference sine wave (blue). $T_{bH}$ will be in ON state when the reference sine wave (black) is bigger than the triangular wave (green). $T_{cH}$ will be in ON state when the reference sine wave (black) is bigger than the triangular wave (pink), by using the same method the operation of switches will be defined as shown in Figures 5.29 and 5.30.

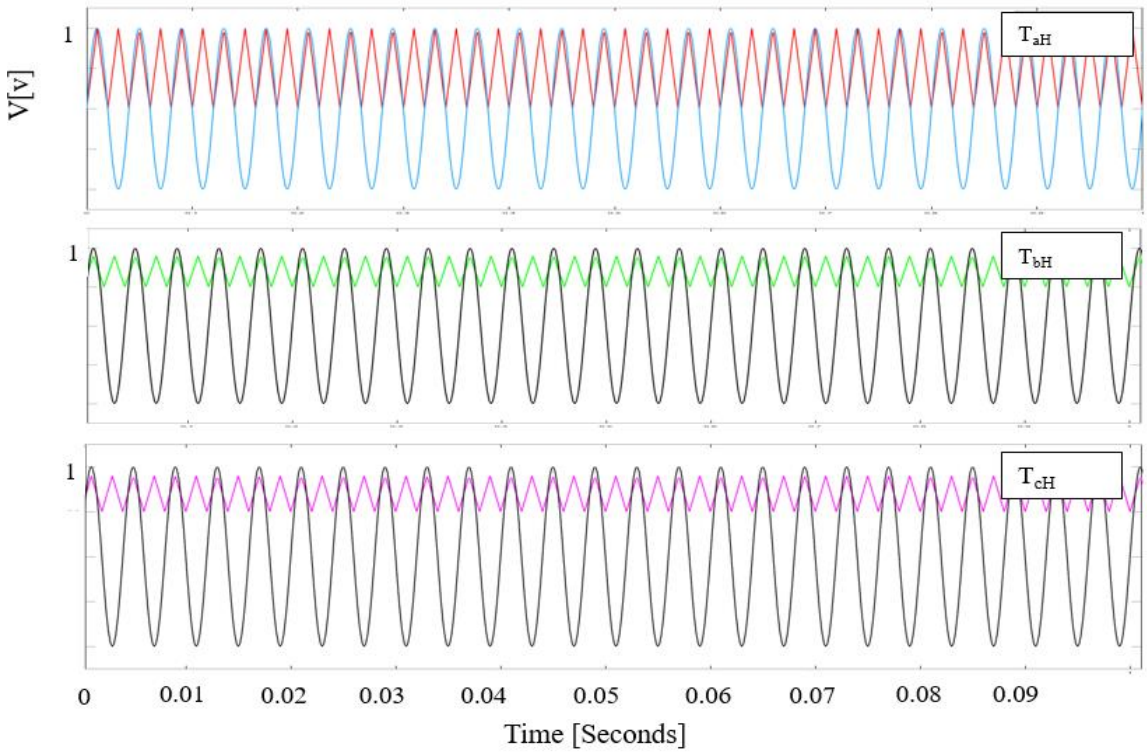



**Figure 5.28 PWM reference and triangular carrier waves that define the operation of the switches $T_{aH}$, $T_{bH}$ and $T_{cH}$ respectively for three switching angles**

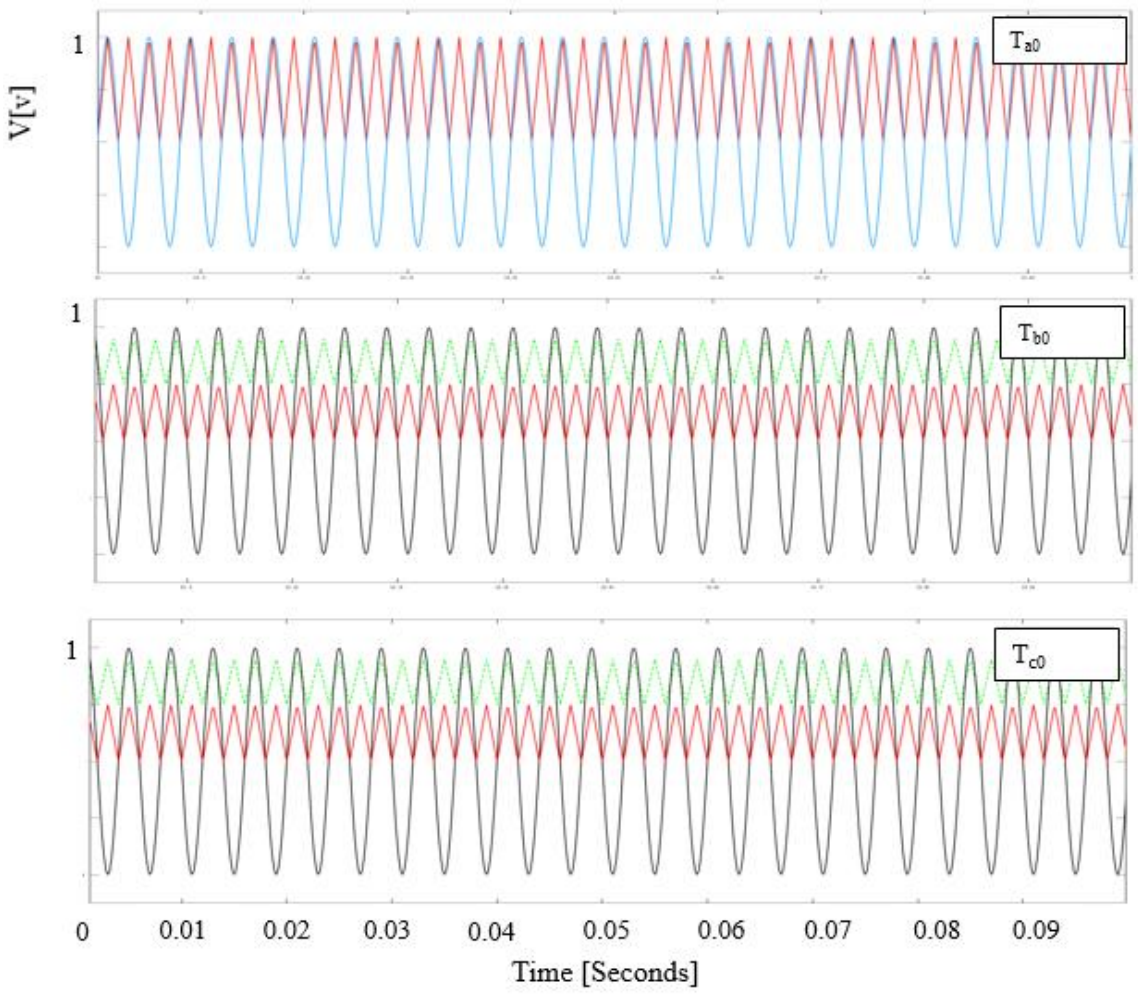



**Figure 5.29 PWM reference and triangular carrier waves that define the operation of the switches $T_{a0}$, $T_{b0}$, and $T_{c0}$ respectively for three switching angles**

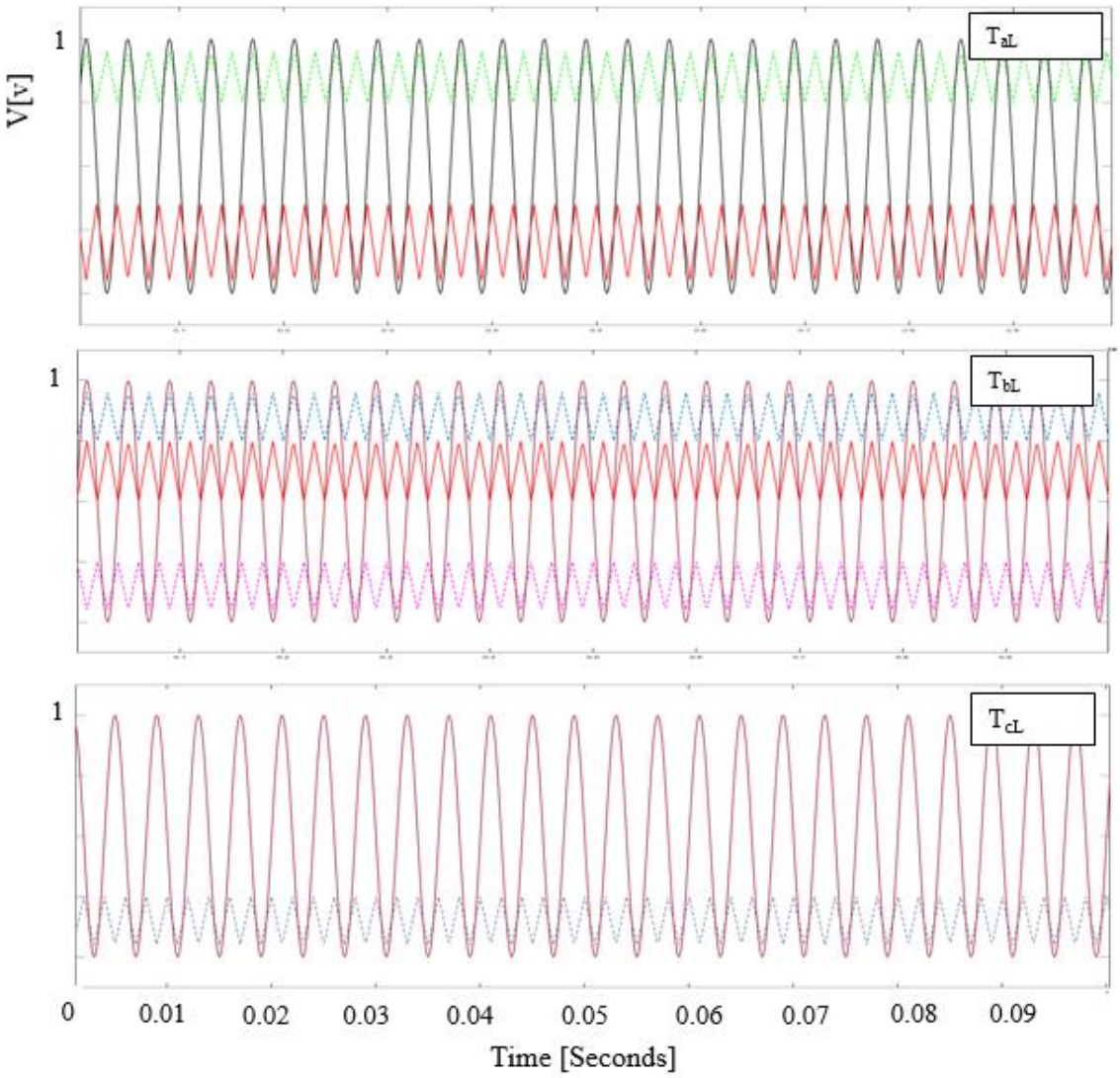



**Figure 5.30 PWM reference and triangular carrier waves that define the operation of the switches $T_{aL}$, $T_{bL}$, and $T_{cL}$ respectively for three switching angles**

#### 5.5.1.4 The Simulation Results using PWM for Three Switching Angles

After using PWM to simulate the second case, the proposed topology output voltage $V_{ab}$ is shown in Figure 5.31. The output voltage results are shown in the Figures 5.32 (p.98) as the phase to phase voltages Vab, Vbc, Vca. Figure 5.33 (p.98) shows the three phase to phase voltages Vab, Vbc, Vca in the case of three switching angles with PWM. This output results have the sinusoidal wave, but one can notice that the higher voltage level is smaller than 100V, so the voltage levels were slightly smaller than the case of three switching angles with using the proposed modulation technique.

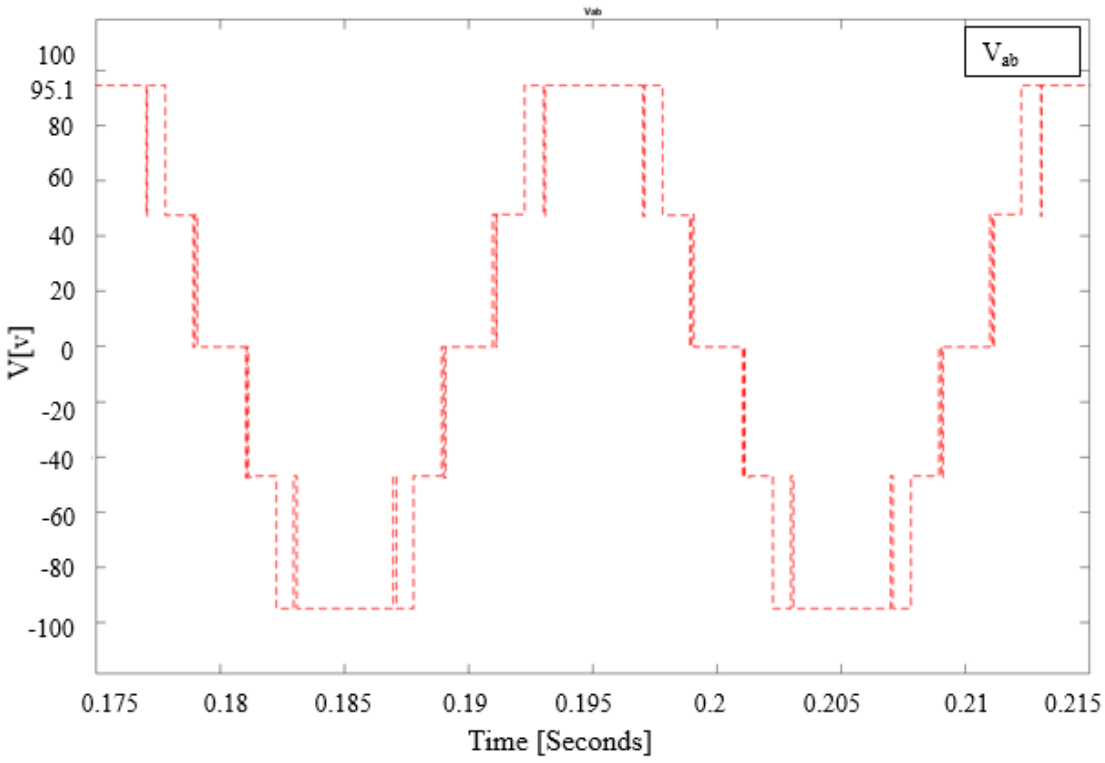



**Figure 5.31 The phase to phase $V_{ab}$ voltage for three switching angles using PWM**

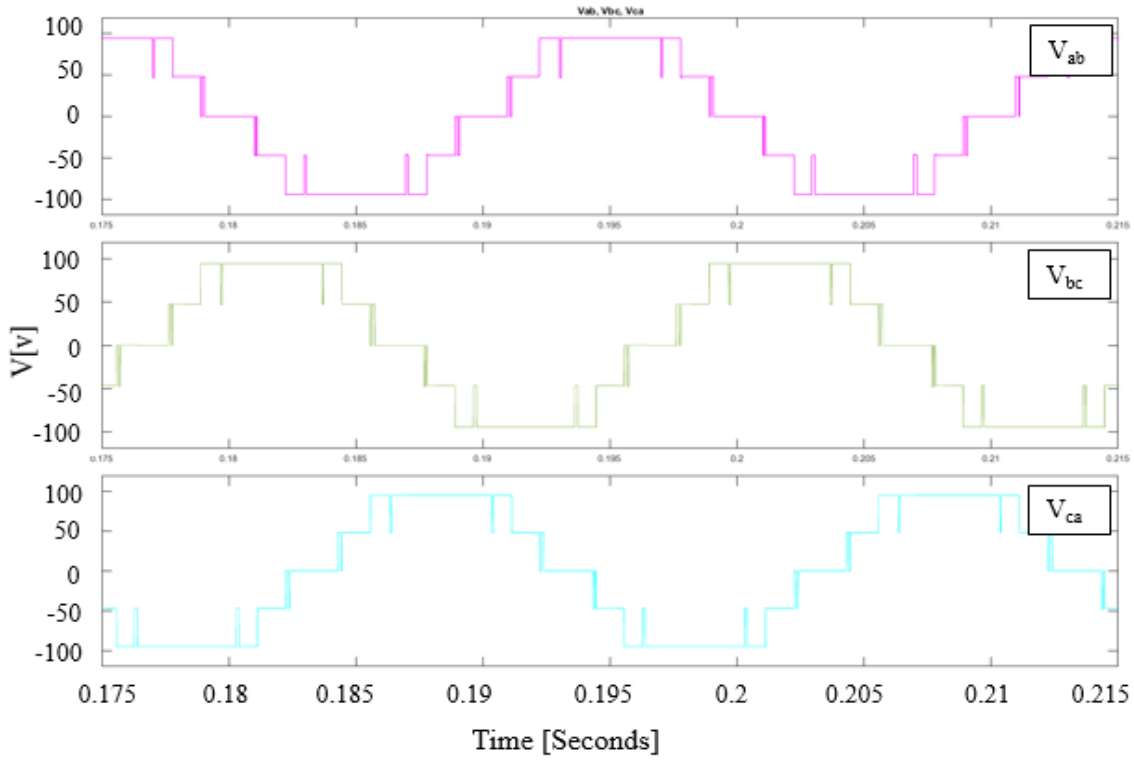



**Figure 5.32 The phase to phase voltages $V_{ab}$, $V_{bc}$, $V_{ca}$ for three switching angles using PWM**

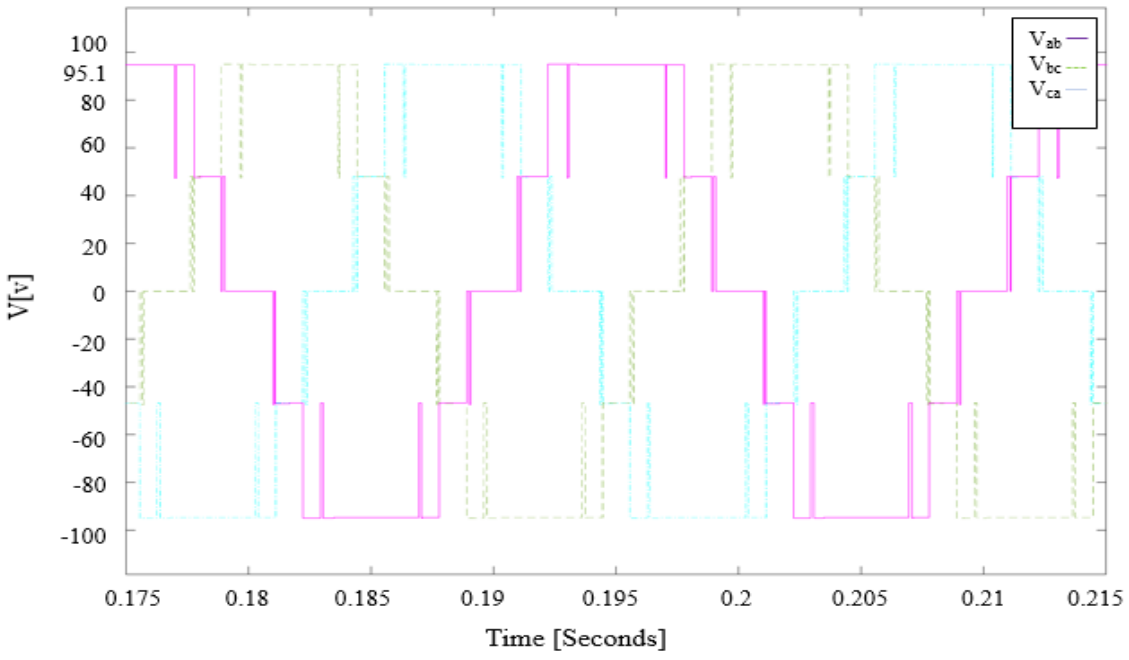



**Figure 5.33 The three phase to phase voltages $V_{ab}$, $V_{bc}$, $V_{ca}$ for three switching angles using PWM**

Figure 5.34 shows the line current $I_{ab}$ in the case of three switching angles with PWM. The current wave is similar to the one found for the same case, but with the other modulation. The fundamental of the current value is actually smaller than 100A and this is a noticeable difference from the phase to phase current when the proposed modulation technique was introduced. The only differences that one from comparing the phase to phase voltage and current of this case by using the proposed modulation and PWM is the fundamental of the output value is less.

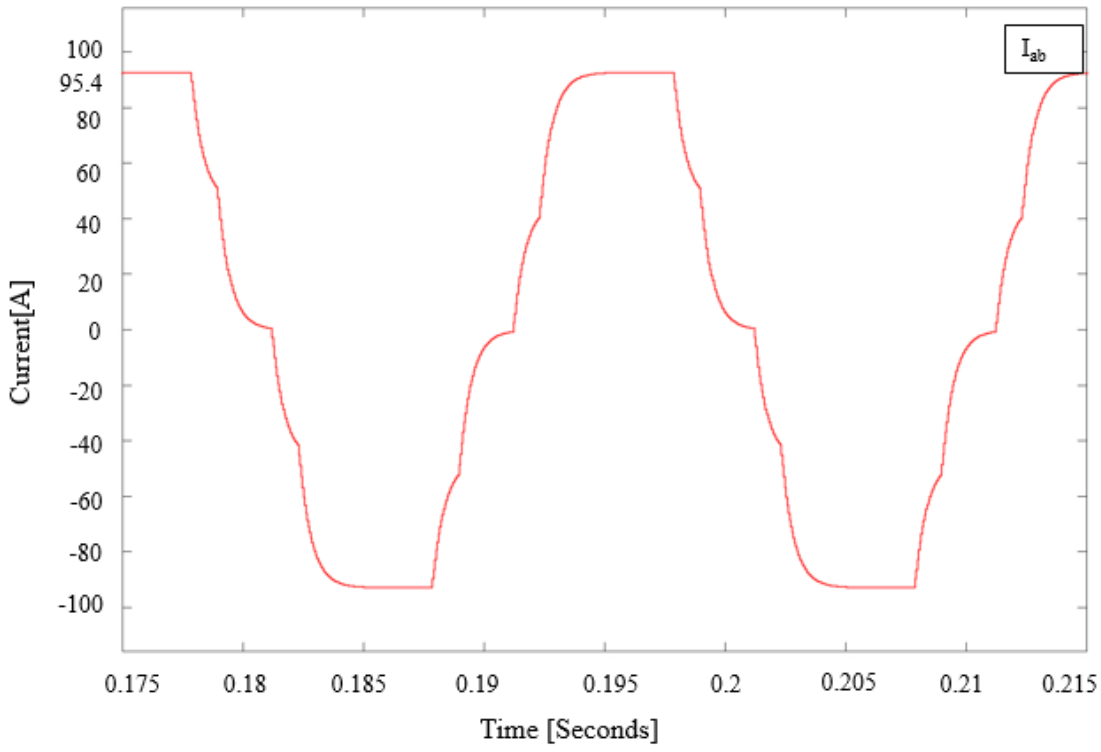



**Figure 5.34 The phase to phase current $I_{ab}$ for three switching angles using PWM**

The harmonics analysis for this case when using PWM is shown in Figure 5.35 and Figure 5.36 (p.101) for the line current and phase to phase voltage respectively. From the harmonics spectrum, the lower harmonics is seen the 3rd, 5th, and 7th, which are known as harmful harmonics for the inverter as well as its load. The THD of the line current is 11.62% and the THD of the phase to phase voltage is 25.5%. The THD values for both the voltage and current are greater than those found when the proposed modulation was used previously.

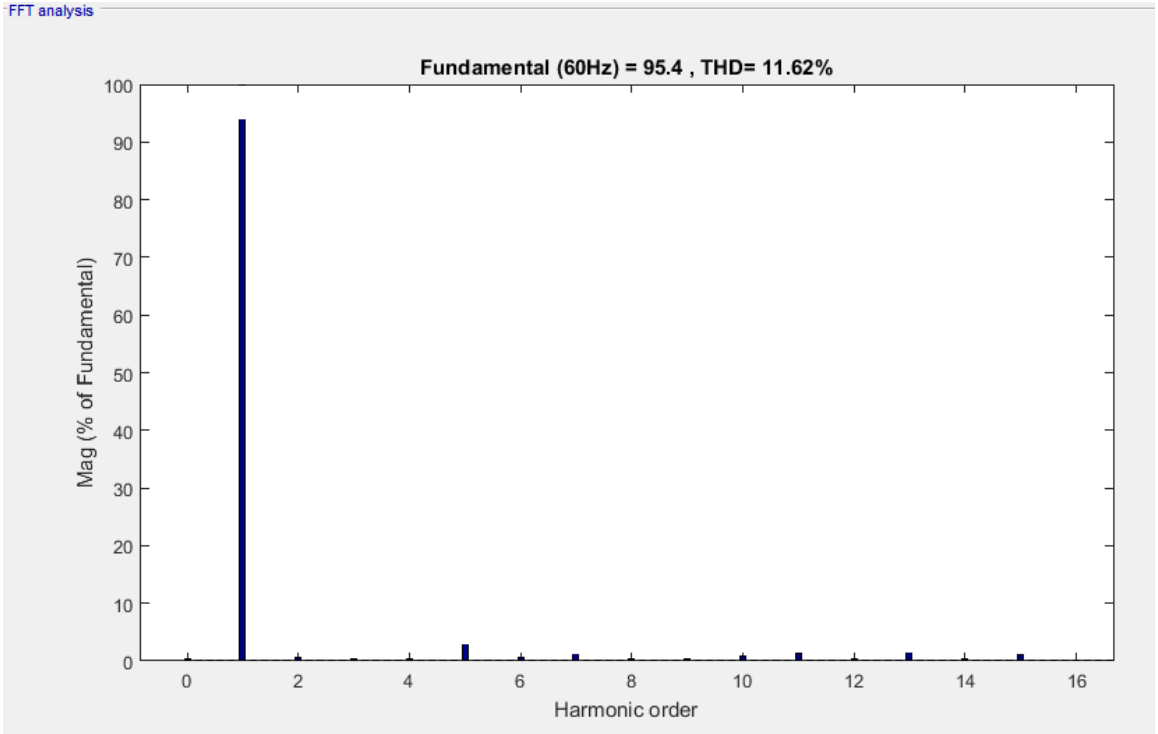



**Figure 5.35 The phase to phase current THD spectrum for three switching angles using PWM**

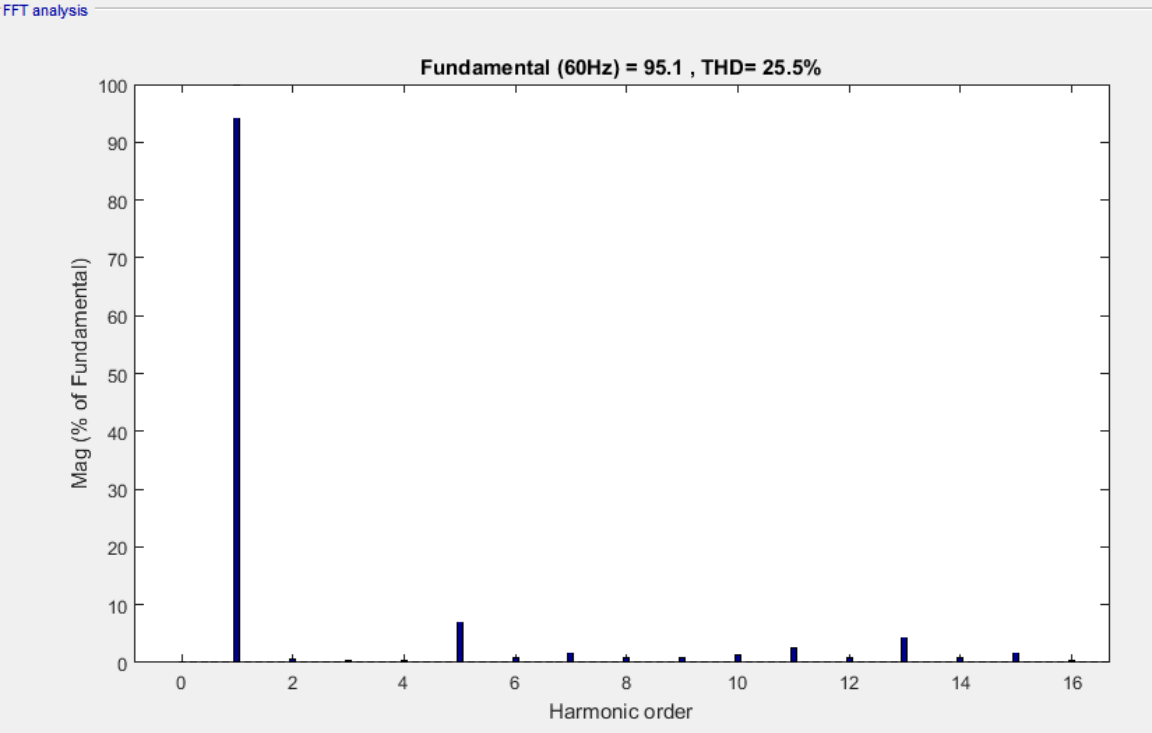



**Figure 5.36 The phase to phase voltage THD spectrum for three switching angles using PWM**

### 5.6 Simulation Results for another set of DC Sources ($E_1 = E_2 = 200$)

To validate that the proposed topology will work for any other equal two DC sources inputs, a simulation for higher DC input voltages is completed using $E_1$=$E_2$=200V as an example. The simulation again has been done for the two cases with one switching angle or with three switching angles. The following section discusses the results.

#### 5.6.1 Simulation Results for another set of DC Sources ($E_1 = E_2 = 200$) for One Switching Angle

The simulation results of switching angle for $E_1 = E_2 = 200$V are shown in Figure 5.37, which is the phase to phase voltage with the five voltage levels (400V, 200V, 0V, -200V, -400V). Figures 5.38 (p.103) and 5.39 (p.103) show the phase to phase voltages $V_{ab}$,

$V_{bc}$, $V_{ca}$ and the three phase to phase voltages $V_{ab}$, $V_{bc}$, $V_{ca}$ for one switching angle respectively. The phase to phase current is shown in Figure 5.40 (p.104) with its greatest value of a 400A and a similar sinusoidal wave. Figure 5.41 (p.104) shows the harmonics spectrum of the line current $I_{ab}$ where there is the $5^{th}$, and $7^{th}$ harmonics are zero, the triple harmonics are zero and the first nonzero harmonic is $11^{th}$ with THD 10.74% almost matches the THD was found for one switching angle when $E_1 = E_2 = 50V$. Figure 5.42 (p.105) shows the harmonic spectrum of the phase to phase voltage with THD equal to 19.13% also as was noticed in the current spectrum. The first nonzero harmonic is the $11^{th}$. The output results for one switching angle validate that the proposed topology will work for any equal DC inputs by applying the case of one switching angle.

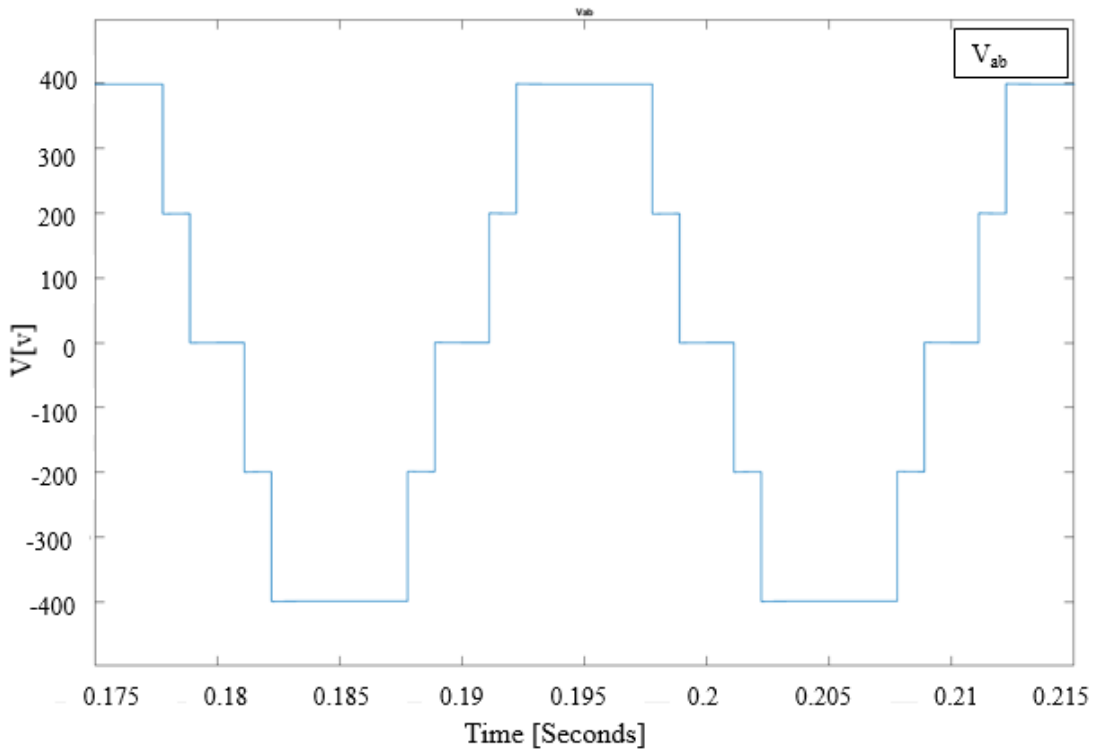



**Figure 5.37 The phase to phase $V_{ab}$ voltage for one switching angle ($E_1 = E_2 = 200V$)**

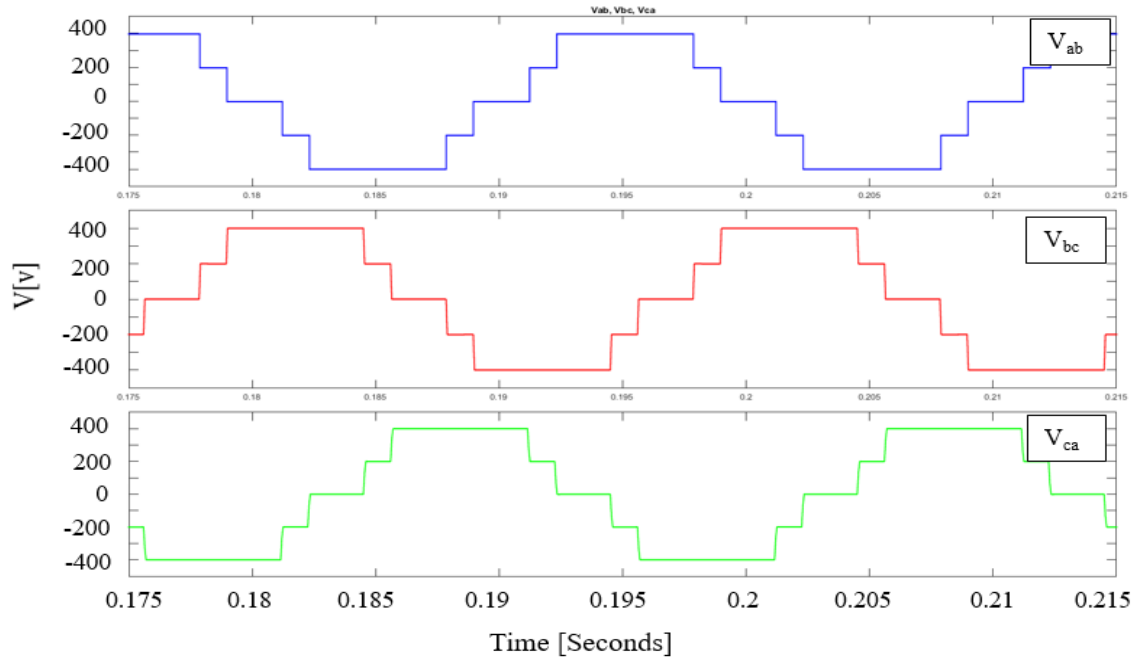



**Figure 5.38 The phase to phase voltages $V_{ab}$, $V_{bc}$, $V_{ca}$ for one switching angle ($E_1$=$E_2$=200V)**

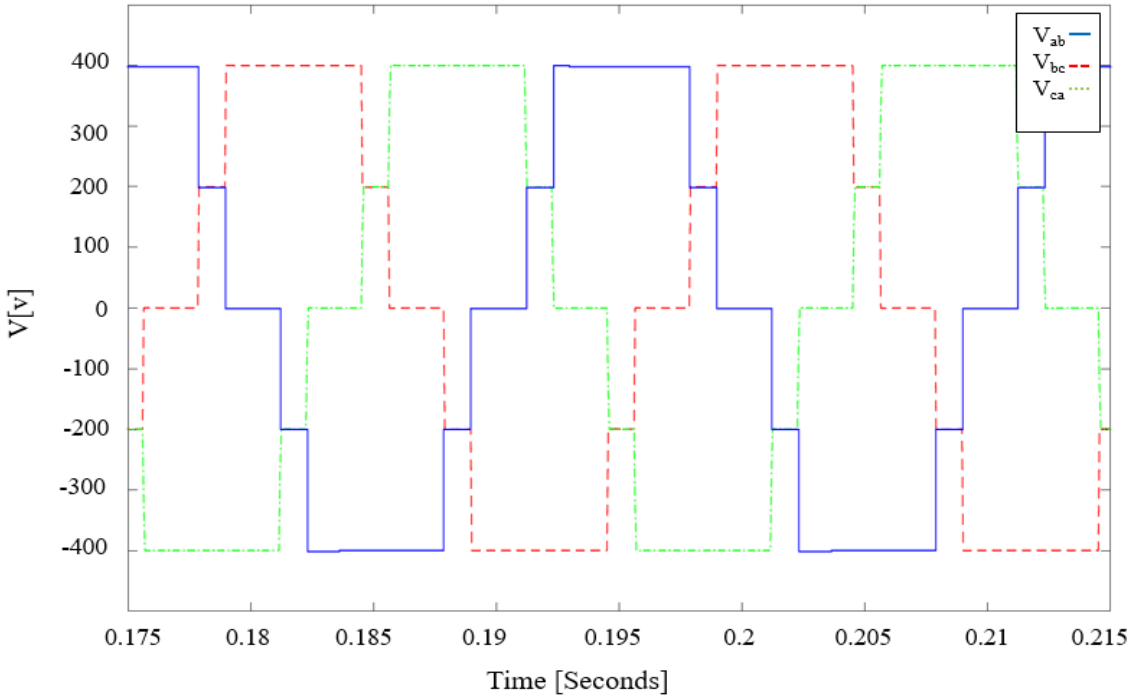



**Figure 5.39 The three phase to phase voltages $V_{ab}$, $V_{bc}$, $V_{ca}$ for one switching angle ($E_1$ = $E_2$ = 200V)**

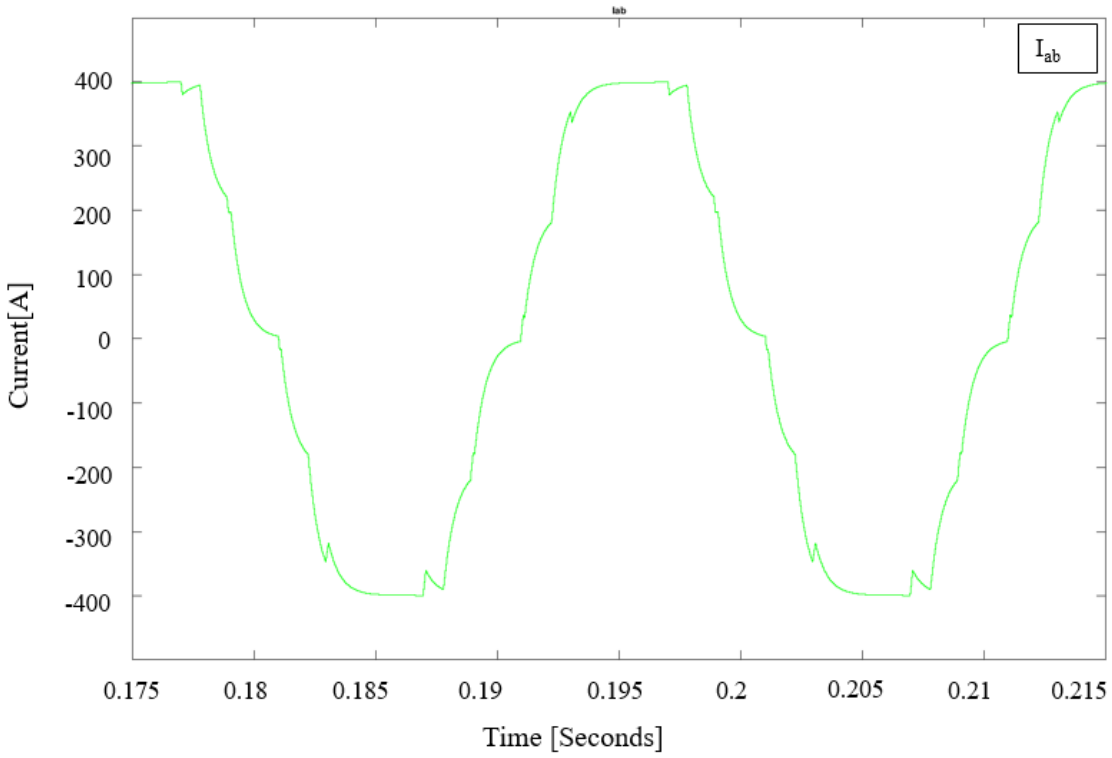



**Figure 5.40 The phase to phase current $I_{ab}$ for one switching angle ($E_1 = E_2 = 200V$)**

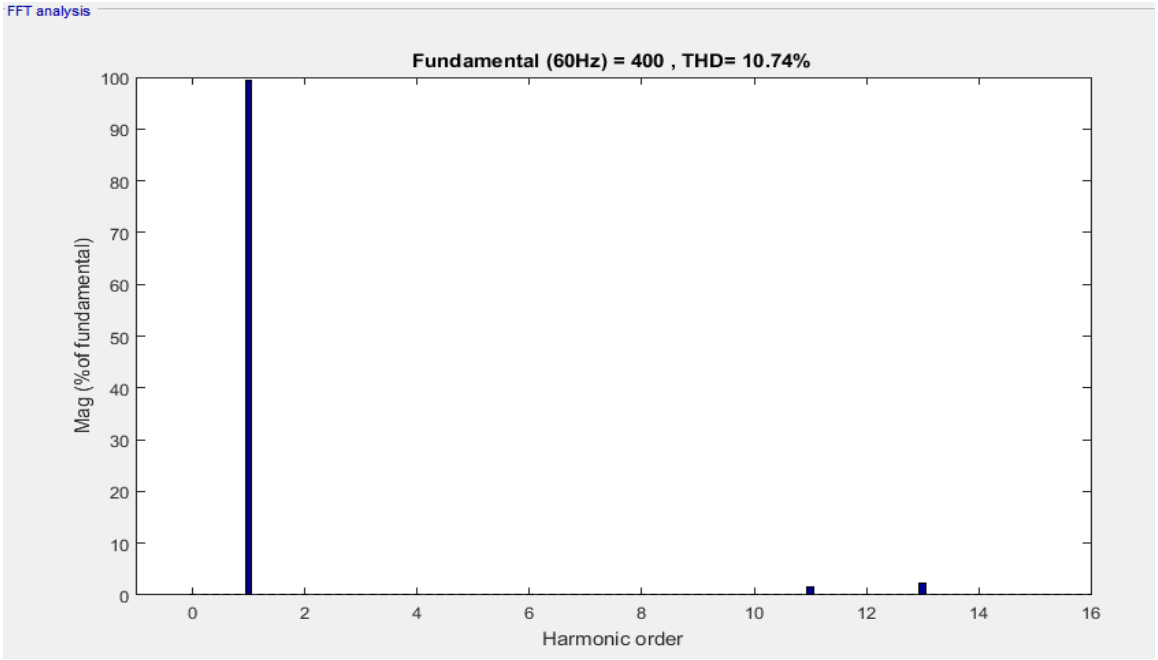



**Figure 5.41 The phase to phase current THD spectrum for one switching angle ($E_1=E_2=200V$)**

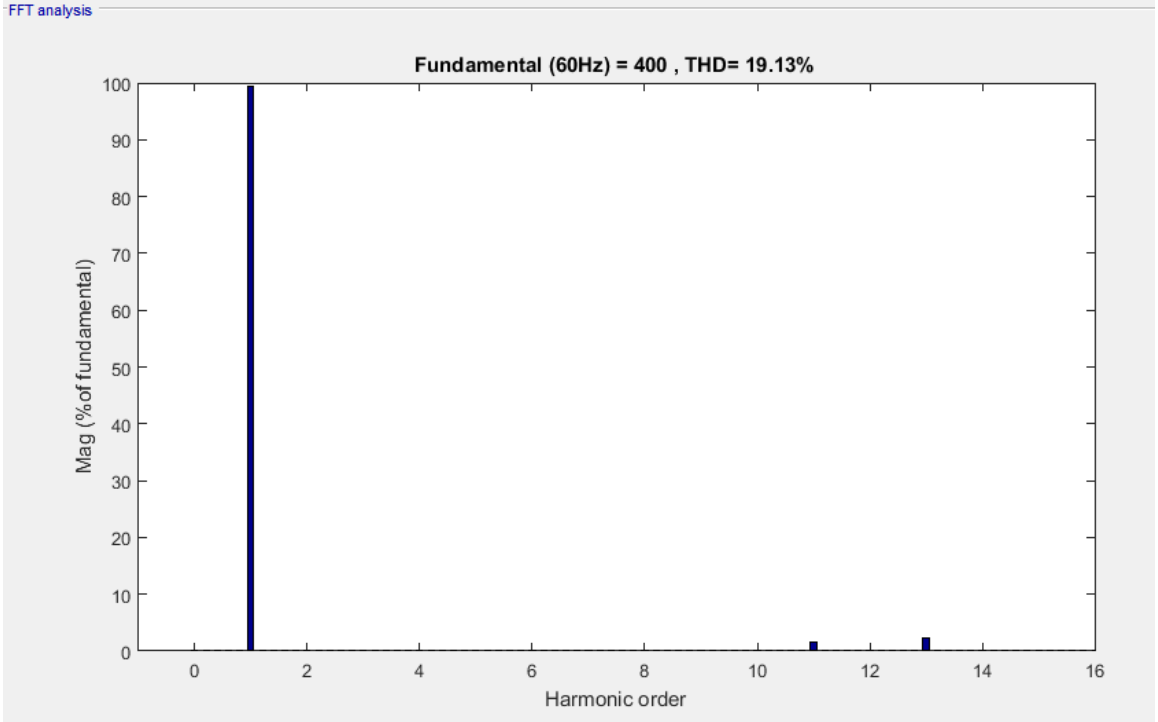



**Figure 5.42 The phase to phase voltage THD spectrum for one switching angle ($E_1 = E_2 = 200V$)**

### 5.6.2 Simulation results for another set of DC sources ($E_1 = E_2 = 200$) for Three Switching Angles

The results of this case when $E_1 = E_2 = 200$ shows that the proposed topology would also work for any two equaled DC inputs with the operation of three switching angles and its modulation technique. The following Figures show the ability of the proposed topology with other DC sources that is taken as an example with E1 = E2 = 200V. Figure 5.43 shows the phase to phase $V_{ab}$ voltage with the five voltage levels of the topology working appropriately with three switching angles introduced in this case. Figure 5.44 (p.107) and Figure 4.45 (p.107) show the phase to phase voltages $V_{ab}$, $V_{bc}$, $V_{ca}$ and the three phase to phase voltages $V_{ab}$, $V_{bc}$, $V_{ca}$ respectively with the new two DC inputs where the waves are

close to the sinusoidal wave as well as the phase to phase current wave as shown in Figure 5.46 (P.108).

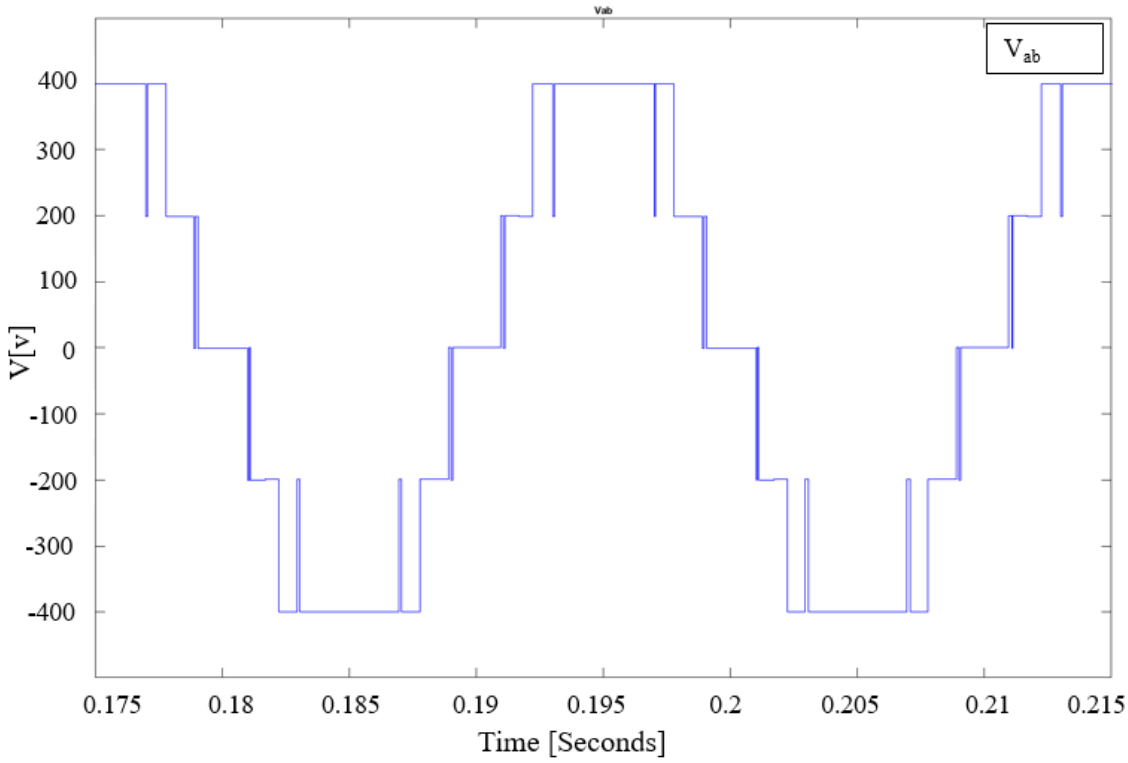



**Figure 5.43 The phase to phase $V_{ab}$ voltage for three switching angles ($E_1 = E_2 = 200V$)**

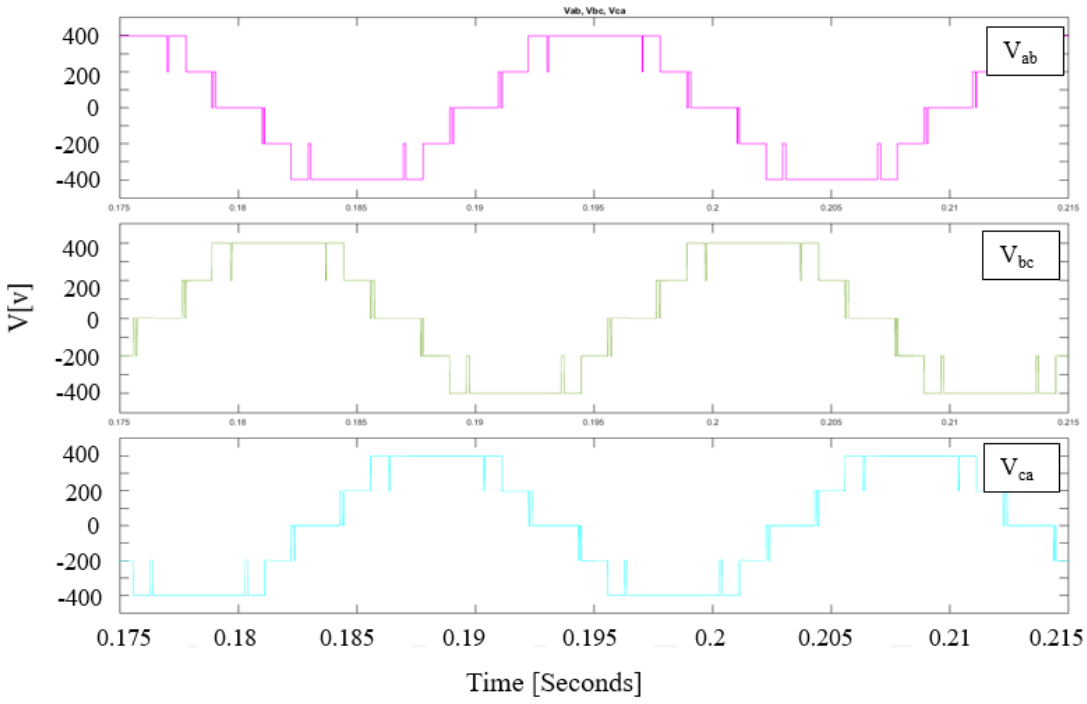



**Figure 5.44 The phase to phase voltages $V_{ab}$, $V_{bc}$, $V_{ca}$ for three switching angles ($E_1 = E_2 = 200V$)**

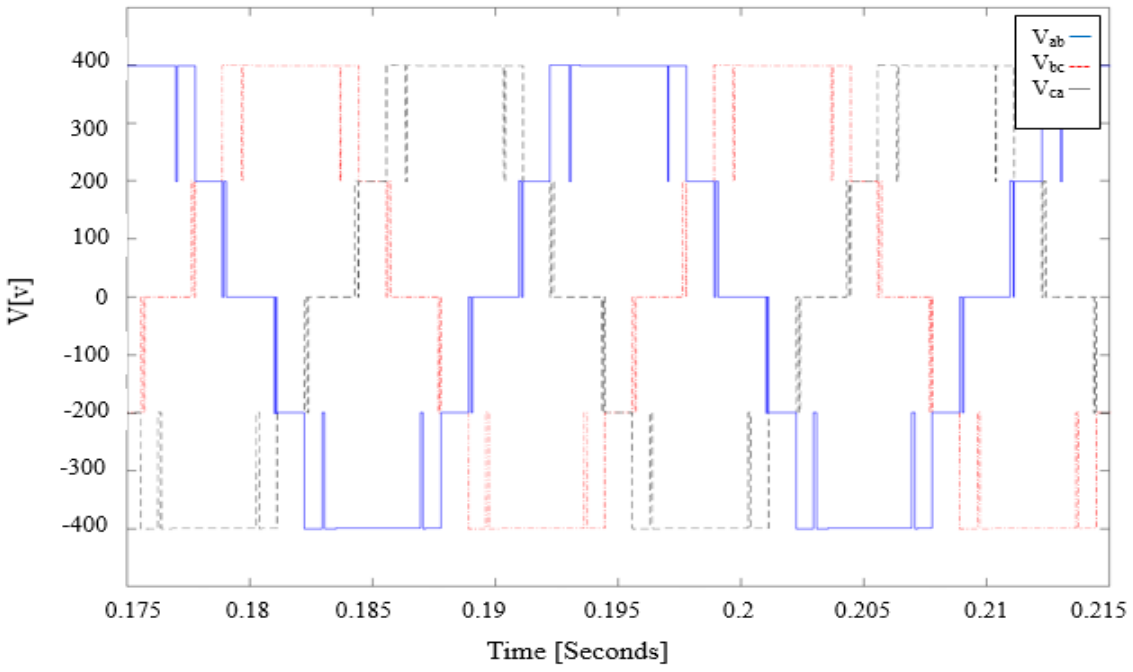



**Figure 5.45 The three phase to phase voltages $V_{ab}$, $V_{bc}$, $V_{ca}$ for three switching angles ($E_1 = E_2 = 200V$)**

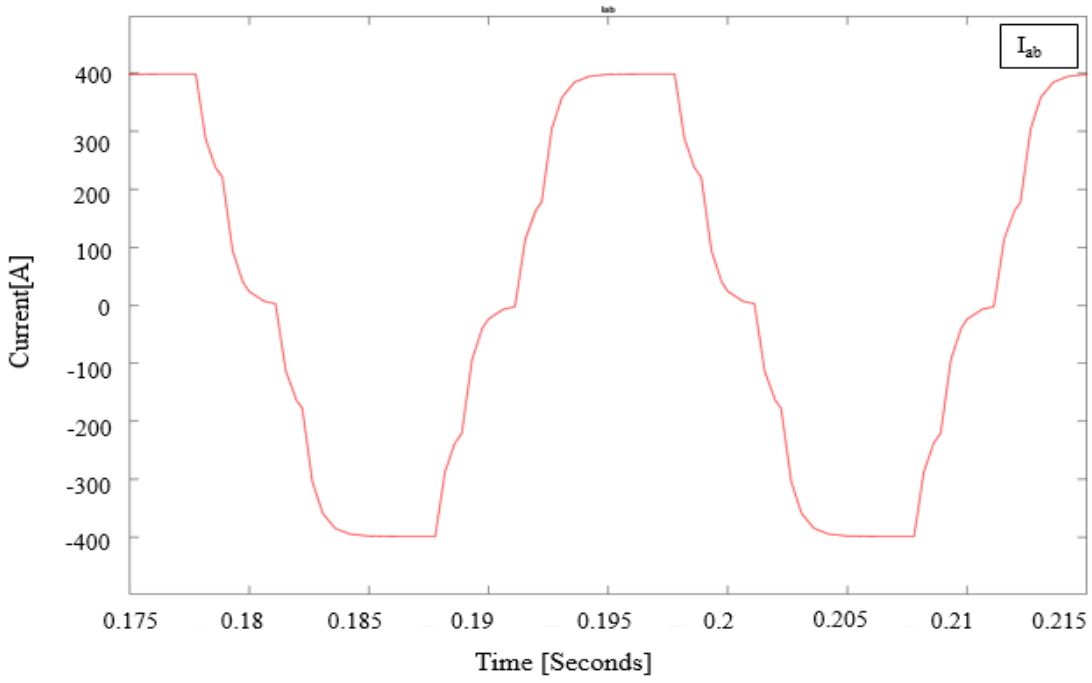



**Figure 5.46 The phase to phase current $I_{ab}$ for three switching angles ($E_1 = E_2 = 200V$)**

The harmonics analysis for this case also is lower and is shown in Figure 5.47 for the phase to phase current with the THD of 9.12%. Figure 5.48 shows the harmonics spectrum of the phase to phase voltage with the THD equal to 18.12%. The harmonic spectrum shows that the THD still is as low as the two DC inputs ($E_1 = E_2 = 50V$), which validates the proposed topology to be working perfectly with any equal two DC inputs.

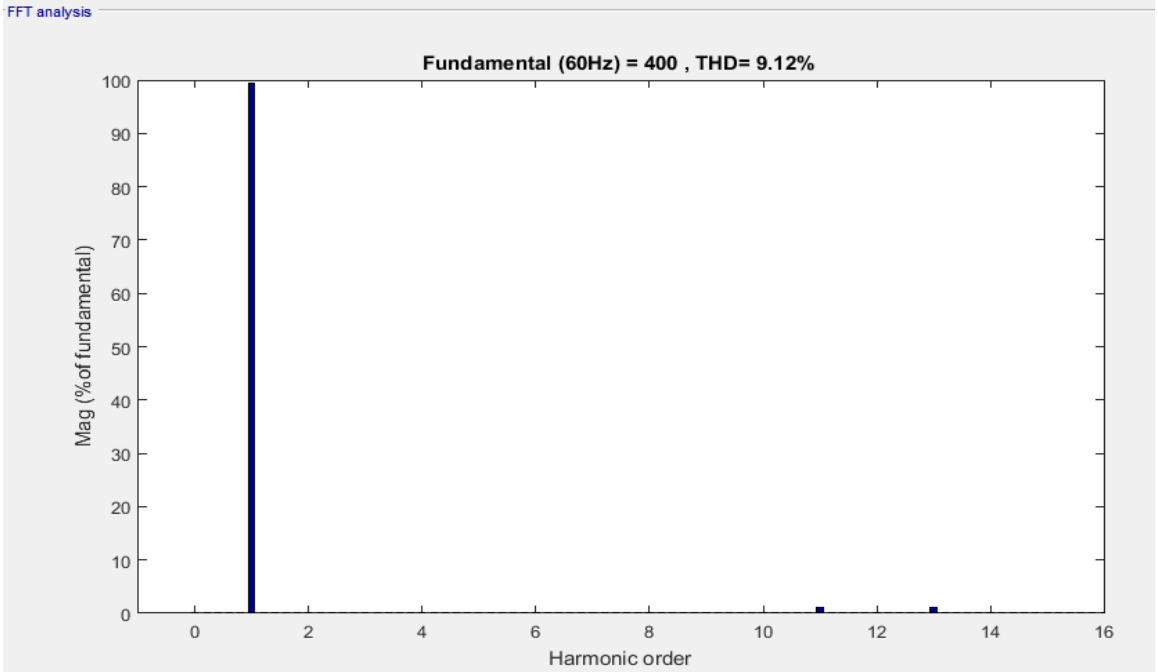



**Figure 5.47 The phase to phase current THD spectrum for three switching angles ($E_1 = E_2 = 200V$)**

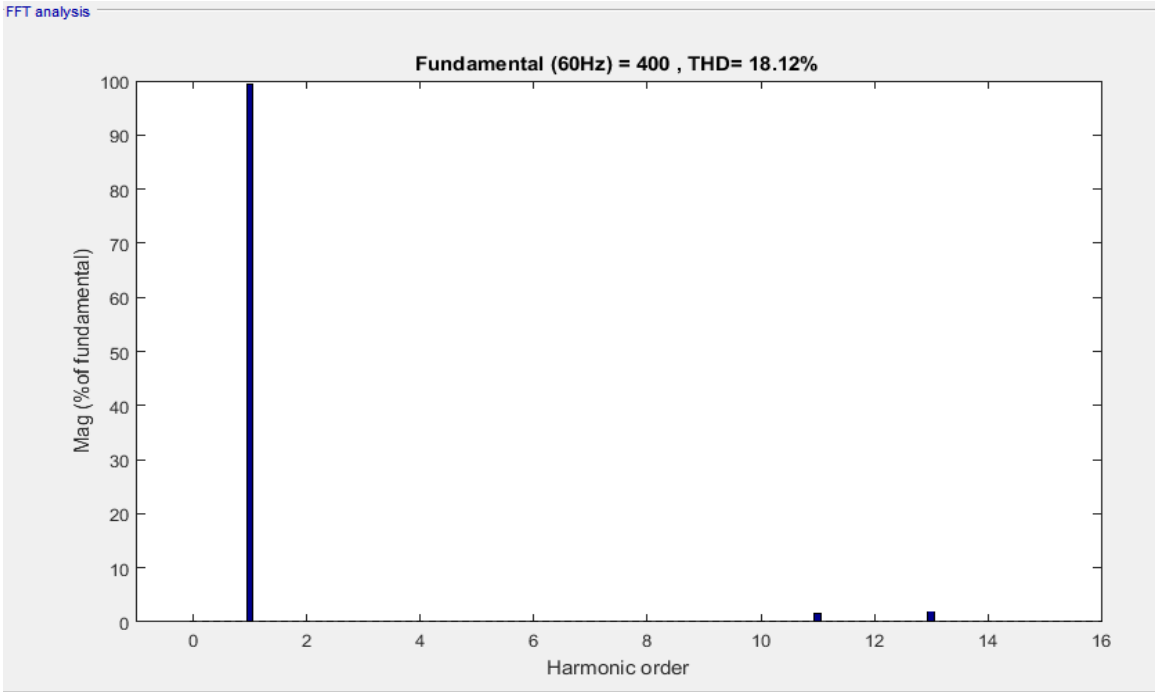



**Figure 5.48 The phase to phase voltage THD spectrum for three switching angles ($E_1 = E_2 = 200V$)**

## 5.7 Conclusion

This Chapter presents the simulation results of this thesis where the two cases (one switching angle and three switching angles) of the inverter output voltage were modeled using MATLAB software. Simulation was completed for the proposed modulation technique, and for the traditional PWM technique.

Using the proposed modulation technique with a frequency of 60Hz, the results for one switching angle show that the inverter output voltage and current were similar to the sinusoidal wave when there is just one switching angle "α". The THD for the phase to phase voltage and the current are 19.3% and 10.73%, respectively. In the case of three switching angles, the inverter output voltage and current is also a better sinusoidal wave than the ones in the case of one switching angle. The THD of the phase to phase voltage and current was 18.11% and 9.1%, respectively.

Using the PWM modulation technique with a frequency of 300Hz for one switching angle and 720Hz for three switching angles shows that all PWM requires a higher frequency than the proposed modulation. A greater THD appears for both cases when using the PWM modulation technique. This illustrates the advantage of the proposed technique by eliminating the THD and the lower frequency, which are harmful for any electrical system.

The simulation results show that two cases (one switching angle and three switching angles) are consistent with the above theoretical analysis in Chapter 4. The case of three switching angles is better than the case of one switching angle, because the case of three switching angles has a lower THD and a better sinusoidal. Overall, the proposed topology would work better when it is controlled according to the case of three switching angles.

The simulation results show that the proposed circuit topology is operating properly. Another set of simulations was completed for two DC sources ($E_1 = E_2 = 200V$) using the proposed control. The simulation results show no difference in the inverter output voltage and current when the two DC sources are changed to different equal values ($E_1 = E_2 = 200V$). This should not influence the inverter outputs and this also means that there is no difference in the spectral harmonic and the THD.

Table 5.1 summarizes the findings of THD for the case of one switching angle and the case of three switching angles with $E_1 = E_2 = 50V$. As can be seen and already discussed, the proposed modulation technique with the case of three switching angles has the best (lowest) THD content.

**Table 5.1 Summery of the THD findings**

| THD% | Using the proposed modulation technique | | Using the traditional modulation technique PWM | |
|---|---|---|---|---|
| | one switching angle | Three switching angles | one switching angle | Three switching angles |
| Current $I_{ab}$ | 10.73% | 9.1% | 13.2% | 11.62% |
| Voltage $V_{ab}$ | 19.13% | 18.11% | 27.1 % | 25.5% |

# CHAPTER 6

## *SUMMARY AND FUTURE WORK*

### 6.1 Introduction and Project Summary

This chapter presents a summary of the research addressed in this thesis and a description of future work. The main objective of this thesis was to increase the efficiency of multilevel inverters, reduce the THD, and increase its adoption with a wide range of multiple source inputs. The thesis proposes two novel concepts: a novel five-level inverter topology with two equal input DC sources, and a novel pre-calculated angle modulation technique with the two cases of switching angles in the interval [0 $\pi/3$]. The main advantages of the novel topology are overall reduction in the number of power electronic components when compared with traditional designs; reduction in the total price of the inverter components; reduction in the total volume and weight; reduction in the total pre-calculated switching angles using the proposed modulation technique; and, an overall THD reduction. The topology has been simulated with the modulation technique for the two cases of the switching angles in the interval [0 $\pi/3$]: one switching angle and three switching angles. The simulation results show a lower THD value using the proposed modulation technique when compared with the traditional technique. Specifically, the results for the one switching angle modulation technique shows the THD to be 19.13% in the phase to phase output voltage and 10.73% in the phase-to-phase current. The results for the three switching angles modulation technique shows the THD to be 18.11% in the phase-to-phase output voltage and 9.1% in the phase to phase current. Using the traditional modulation technique with one switching angle increases the THD to 27.1% in the phase

to phase output voltage and 13.2% in the phase to phase current. Using the traditional modulation technique with three switching angles increases the THD to 25.5% in the phase to phase output voltage and 11.62% in the phase to phase current.

## 6.2 Future Work

The following subsections will discuss additional research topics as they relate to the work presented in this thesis, including the proposed MI topology, its input side, and its output side. More specifically, the following topics will be discussed: validation of the proposed topology, alternative topologies, alternative switching angles for the modulation technique, alternative input sources, and the proposed topology with unequal DC sources.

### 6.2.1 Validation of the Proposed Topology

A prototype system can be designed and built to validate the operation and advantages of the proposed topology. Laboratory experiments can be conducted for the different cases discussed in this thesis. Specifically, the proposed modulation technique with the two cases of the switching angles can be tested and verified. The experiments will be conducted again by using the traditional modulation technique (PWM) to compare with the proposed modulation technique. The results will then be analyzed and compared with the simulation results. Depending on the results, additional research opportunities may develop.

### 6.2.2 Alternative Topologies

Improving the inverter operation and performance can be achieved by increasing the number of voltage levels in the output waveform. This is possible by increasing the number of switches, increasing the number of input DC sources, or a combination of both. The proposed inverter topology in this thesis can be modified with additional switches to have one more voltage level as shown in Figure 6.1. This topology then becomes a three-phase, six-level topology. A total of 12 switches ($A_1$, $A_2$, $A_3$, $A_1'$, $A_2'$, $A_3'$, $B_1$, $B_2$, $B_3$, $B_1'$, $B_2'$, and $B_3'$) and two DC ($E_1$ and $E_2$) sources will be required in this modified configuration, as can be seen in Figure 6.1. The output voltage levels in this topology are $E_1$, $E_2$, $E_1+E_2$, $-E_1$, $-E_2$, and $-E_1-E_2$, as depicted in Figure 6.2. These levels will be obtained according to the controlling sequence of the topology's switches.

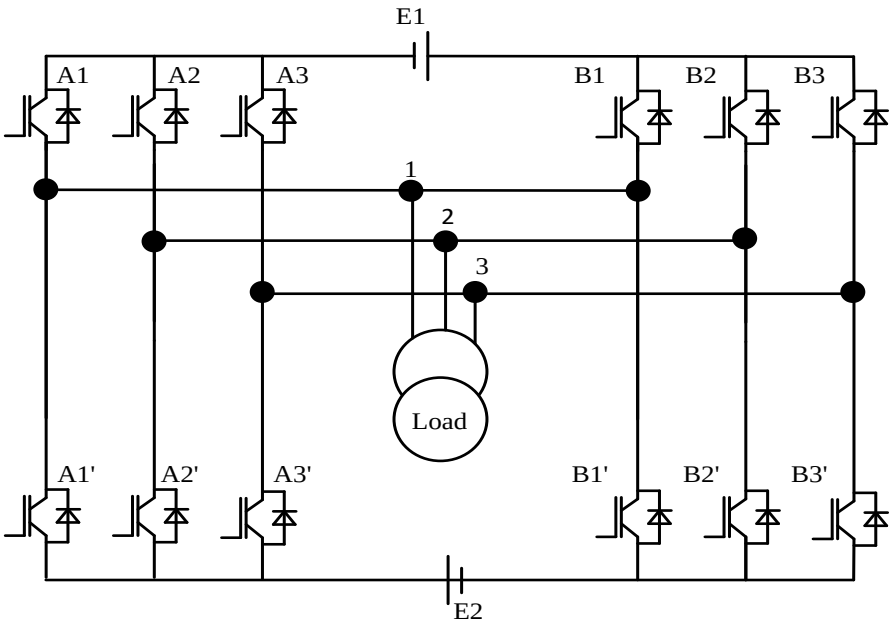



**Figure 6.1 Modified MI topology to provide three-phase, six-level output**

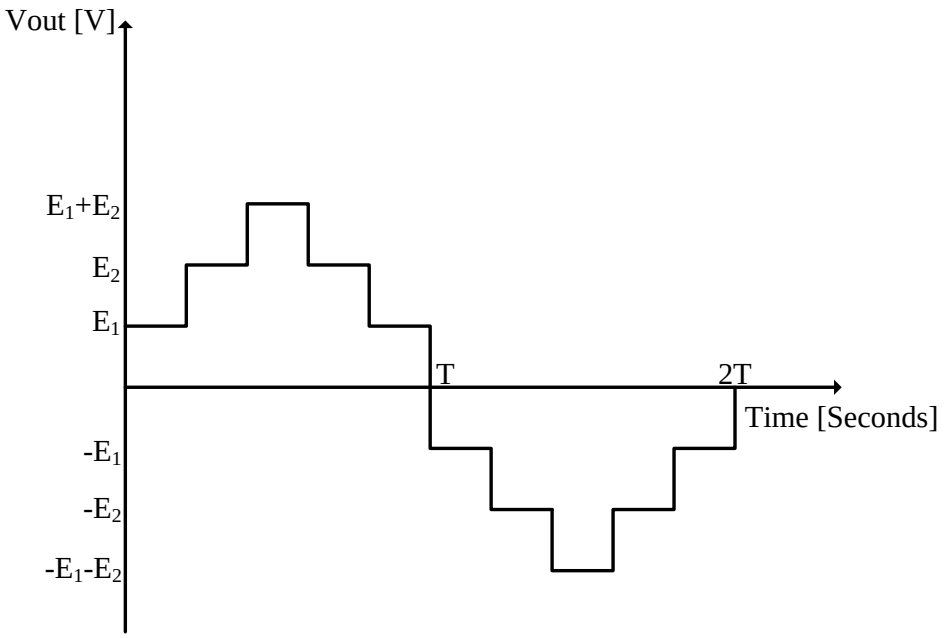



**Figure 6.2 The output voltage of the three-phase, six-level topology**

The proposed topology can be modified with two additional DC input sources and additional switches to have twelve voltage levels in the inverter's voltage output. This three-phase, twelve-level inverter topology will have 16 power rated switches and four DC sources, as shown in Figure 6.3. The topology's DC sources are $E_1$, $E_2$, $E_3$, and $E_3$ and the 16 power rated switches are A1, A2, A3, A1', A2', A3', B1, B2, B3, B1', B2', B3', T1, T1', T2, and T2'. As shown in Figure 6.4, controlling these switches will create the twelve voltage levels in the output voltage, which are $E_1$, $E_2$, $E_3$, $E_4$, $E_1+E_2$, $E_3+E_4$, $-E_1$, $-E_2$, $-E_3$, $-E_4$, $-E_1-E_2$, $-E_3-E_4$.

Future work will include developing mathematical models as well as THD results. Finally, developing models using MATLAB software and building prototype circuits will provide the validation for the results.

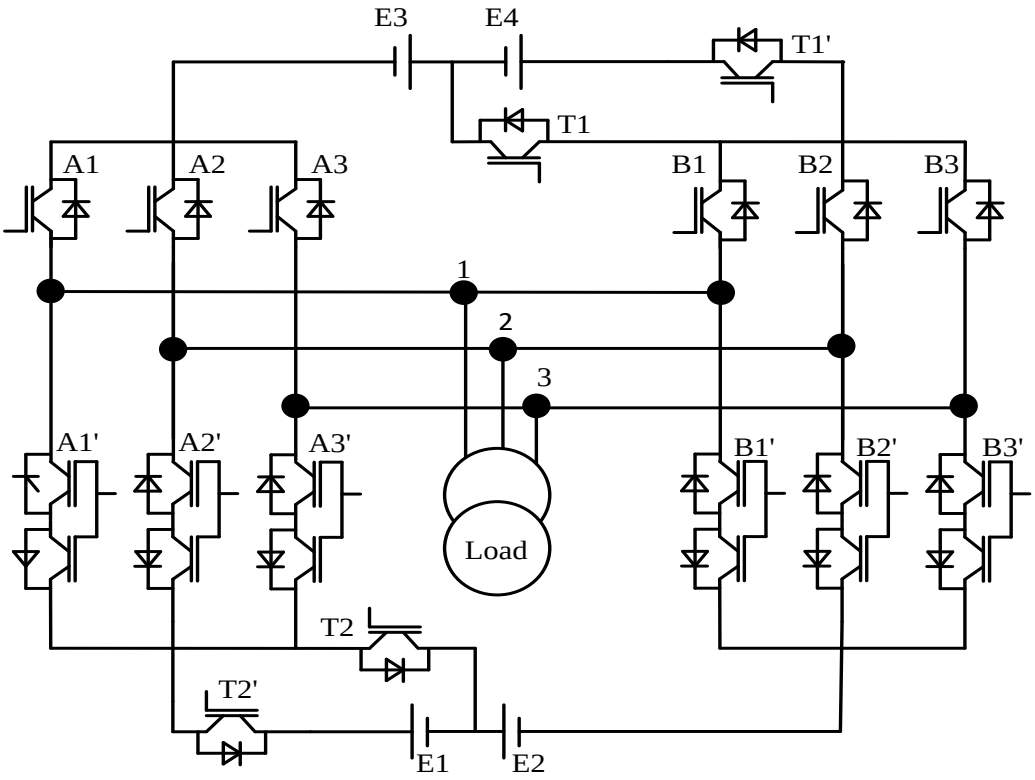



**Figure 6.3 Three-phase, twelve-level topology**

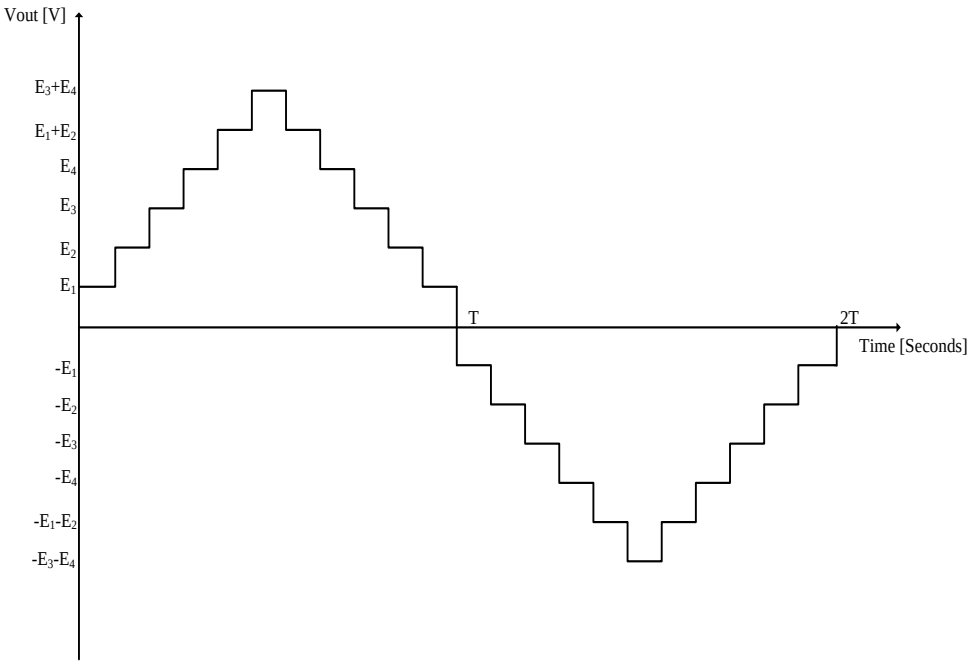



**Figure 6.4 The output voltage of the three-phase, twelve-level topology**

### 6.2.3 Alternative Switching Angles for the Modulation Technique

The proposed modulation technique was completed for two cases, one switching angle and three switching angles. Future work will investigate the effect of having more than three switching angles in the interval [0 π/3]. Figure 6.5 depicts one of the possible scenarios of having six switching angles and shows three levels with two pulses introduced in the second level. The pre-calculated technique will be developed for this case and will be implemented into the multilevel inverter topology. The proposed modulation technique can focus more on studying the effect of switching angles being in the low voltage level or the high voltage level in the inverter phase to phase output voltage. Figure 6.6 shows: a) when the switching angles are in the low voltage level ($L_1$), and b) when the switching angles are in the high voltage level ($L_2$).

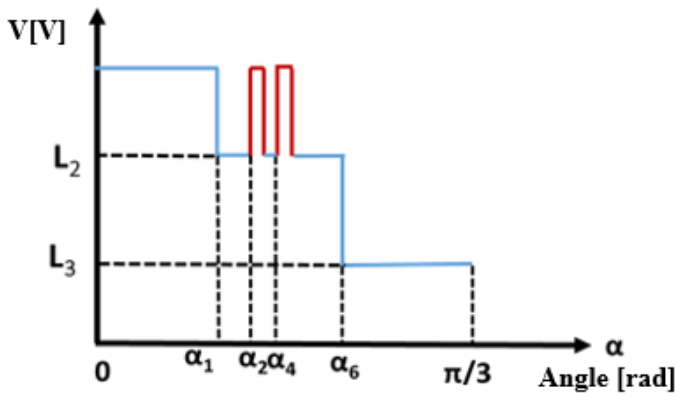



**Figure 6.5 Six switching angles in [0 π/3]**

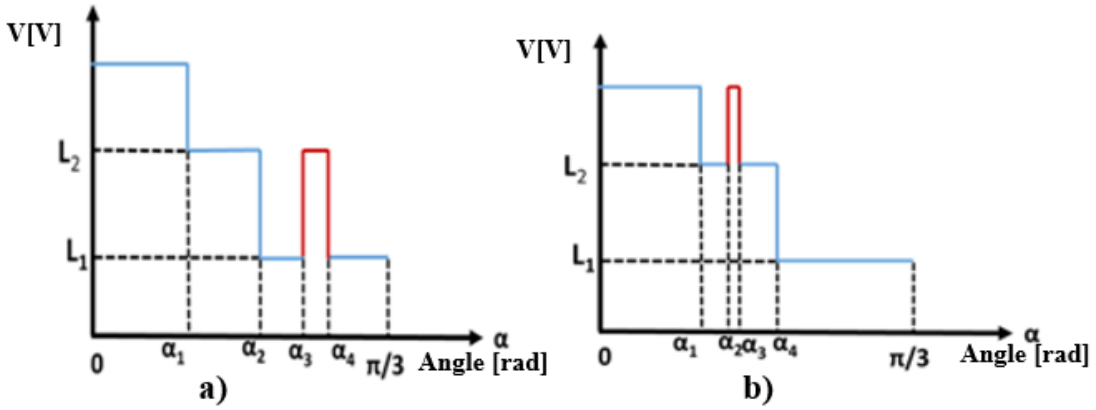



**Figure 6.6 The switching angles are: a) in the low voltage level; b) in the high voltage level**

### 6.2.4 Alternative Input Sources

The inverter's inputs are usually DC sources, including batteries, as was demonstrated in this thesis. A combined adaptive battery system along with the MI topology can be used to improve the state of charge (SOC), the state of health (SOH), and the overall performance of the battery system. A proposed adaptive battery system with two battery elements ($B_1$, $B_2$), where each element can be a single cell, string, or bank configured with eight power switches is shown in Figure 6.7. A power management system will manage each battery and controls the switches depending on the desired outcome.

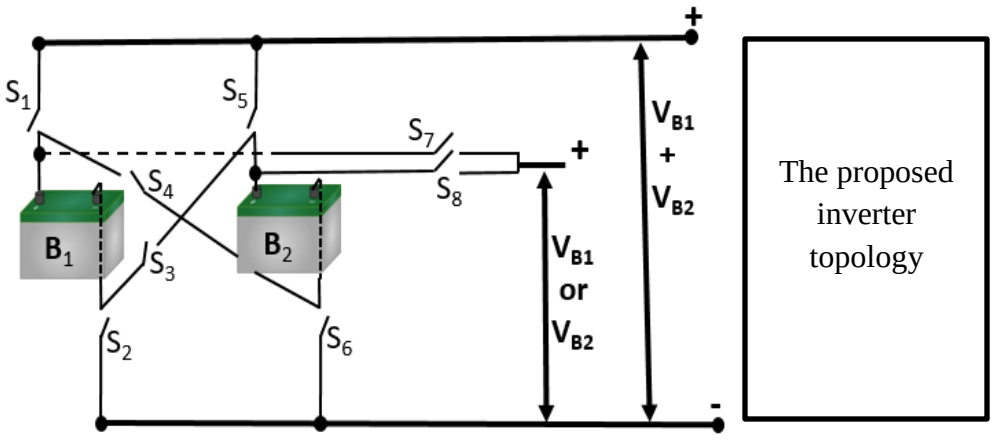



**Figure 6.7 An adaptive battery system**

A full system vision of this adaptive battery system, along with potential applications is shown in Figure 6.8. This system can be used with MI and DC applications for charging or discharging.

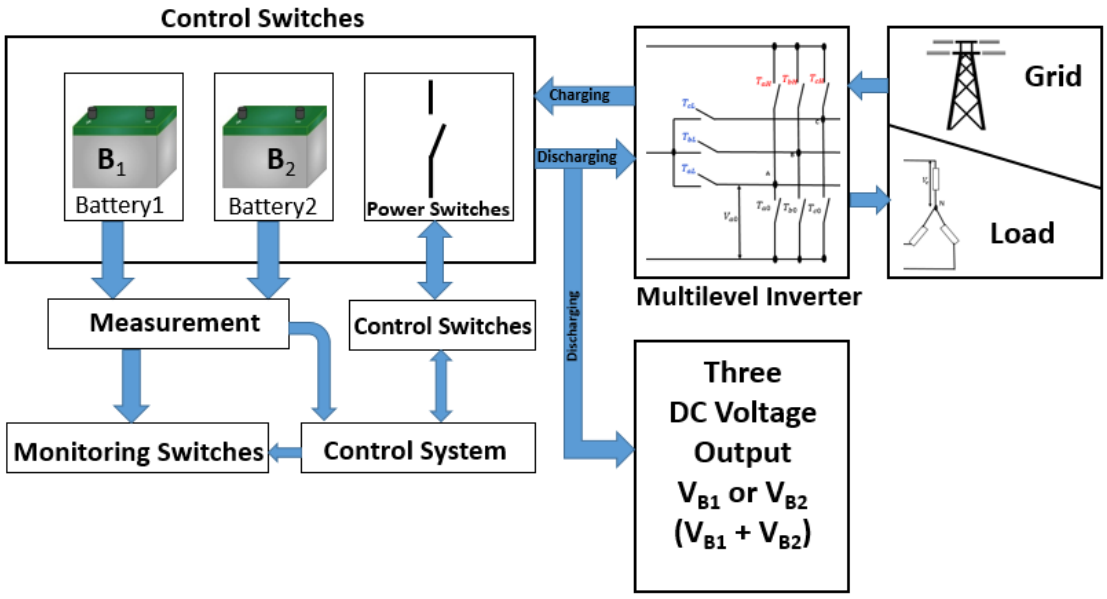



**Figure 6.8 An adaptive battery storage system**

The adaptive nature of this system gives rise to two prominent benefits: a multiple voltage level output and an improved battery performance. The first benefit provides for an equal discharge pattern when it is used with multilevel inverters to increase the system efficiency and operation time, and to control, monitor, and exploit the existing energy in the batteries until 100% as depicted in Figure 6.9. Figure 6.9 also shows the battery bank discharging current after applying the adaptive battery storage system. Using this approach, the discharging current will be equal between the battery banks, which will improve the system performance and battery bank lifetime.

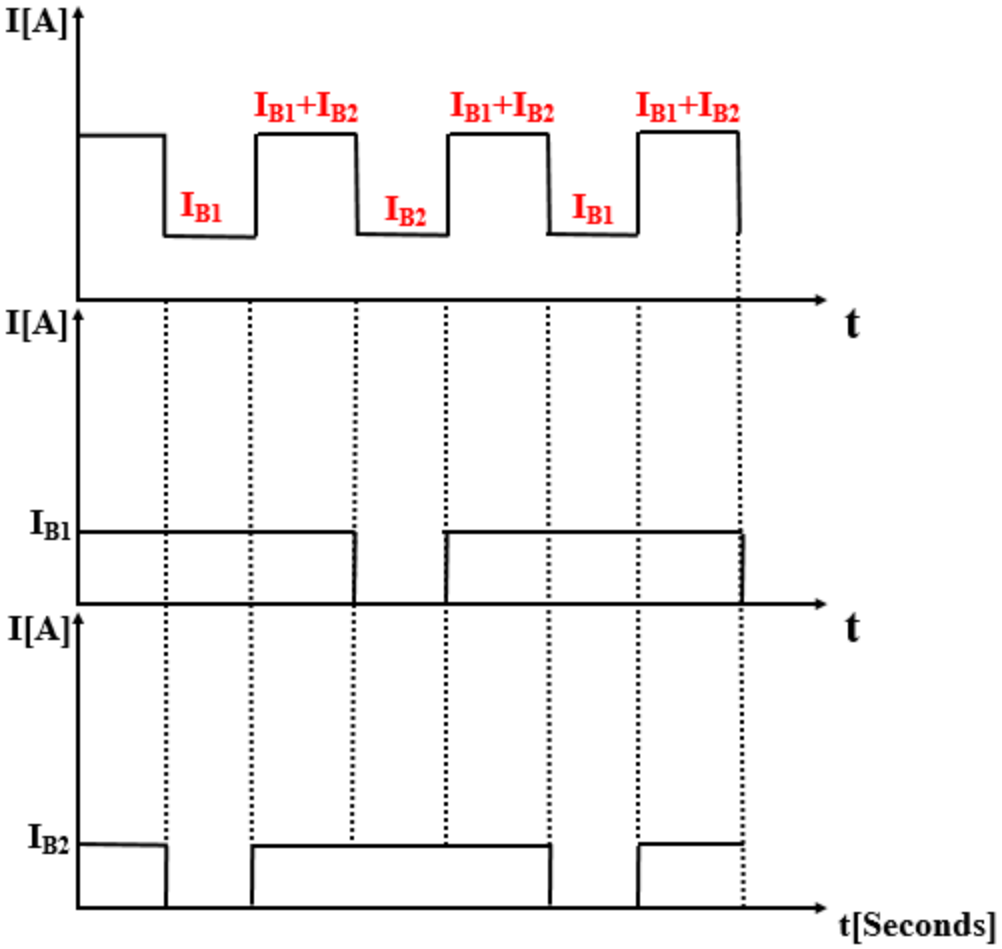



**Figure 6.9 Battery discharging current for the adaptive battery system**

The second benefit of the adaptive battery system is the ability to provide two different voltage levels at the same time. Figure 6.10 shows the first possible configuration for the switches to provide V and 2V voltage levels (when $V_{B1}$ and $V_{B2}$ are equal). In this configuration, the switches $S_2$, $S_4$, $S_5$, and $S_7$ are closed, and switches $S_1$, $S_3$, $S_6$, and $S_8$ are open. The first voltage level can be obtained from $V_{B1}$.

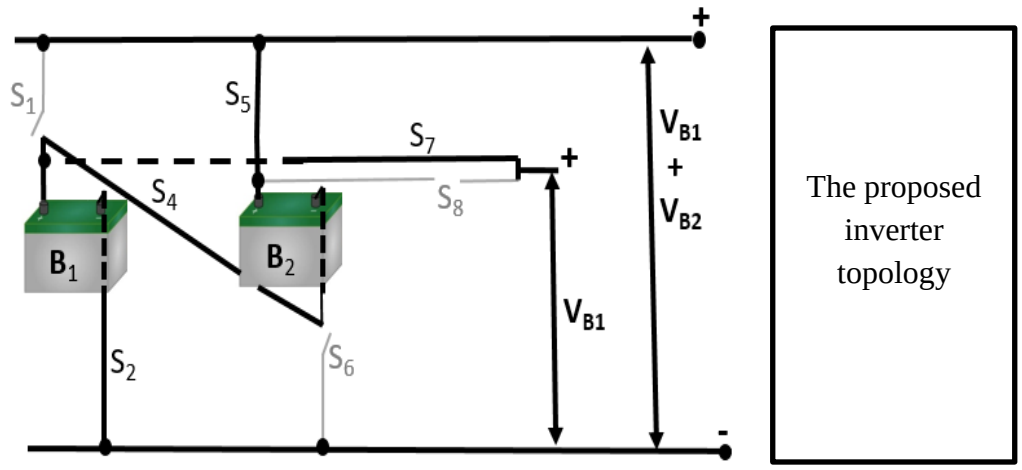



**Figure 6.10 First battery banks configuration**

Figure 6.11 shows the second possible configuration for the switches to give V and 2V voltage levels. In this configuration, the switches $S_2$, $S_4$, $S_5$, and $S_7$ are open, and the switches $S_1$, $S_3$, $S_6$, and $S_8$ are closed. The first voltage level can be obtained from $V_{B2}$.

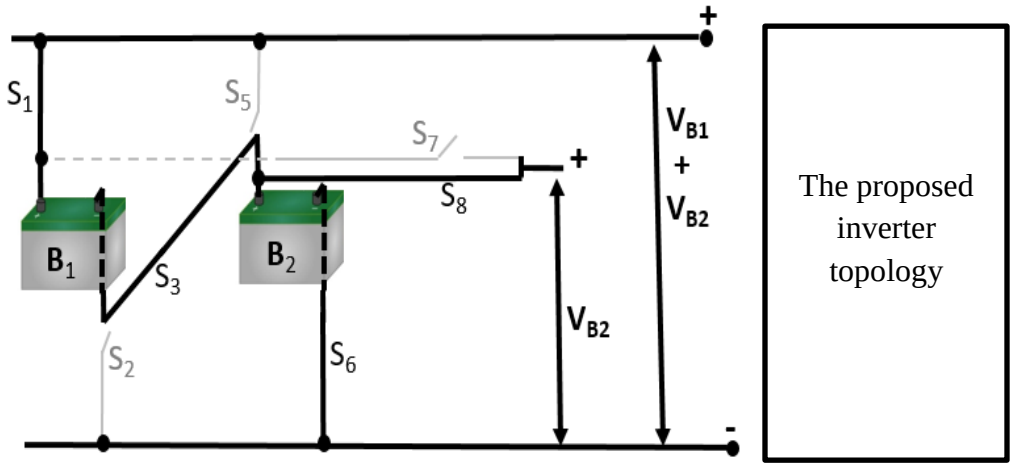



**Figure 6.11 Second battery banks configuration**

The whole system will be tested by connecting the adaptive battery system with a MI inverter. A simulation model of the whole system can be developed, modeled, and simulated, and the results will be analyzed. The goal of future work is to improve the SOC

and the SOH of the battery. It is likely that the overall system operation, performance, and quality of the output voltage and generated power will also improve.

### 6.2.5 Proposed Topology with Unequal DC Sources

This thesis focuses on the analyses of the results with equal DC sources ($E_1=E_2=50V$). Future work will include modeling and simulation with unequal sources ($E_1 \neq E_2$). The simulation results will investigate how unequal DC sources will affect the performance and THD impact. The adaptive battery system mentioned in section 6.2.4 will be beneficial for equal and unequal sources. These cases can be modeled and analyzed.

Other DC sources, such as solar panels (photovoltaic systems), wind turbines, fuel cells, and other sources can also be used with the proposed topology.

# REFERENCES


[1] The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition, IEEE Press, 2000,ISBN 0-7381-2601-2, page 588

[2] "History | IEEE Power & Energy Magazine". magazine.ieee-pes.org. Retrieved 17 January 2017.

[3] Rahimo, M. T. "Ultra high voltage semiconductor power devices for grid applications." In Electron Devices Meeting (IEDM), 2010 IEEE International, pp. 13-4. IEEE, 2010.

[4] Welleman, A., R. Leutwyler, and J. Waldmeyer. "High current, high voltage solid state discharge switches for electromagnetic launch applications." In Electromagnetic Launch Technology, 2008 14th Symposium on, pp. 1-5. IEEE, 2008.

[5] Rahimo, M. "Power semiconductors as a key enabler for modern and future power electronics systems." Energy and Power (2011).

[6] BERNET, S., SOMMER, R., 2010. Multi-Level Converters for Industrial Applications. ECPE-Workshop Advanced Multilevel Converter System, Västerås, September 2010.

[7] Thielemans, Steven, Alex Ruderman, and J. A. Melkebeek. "Flying-capacitor multilevel converter voltage balance dynamics for pure resistive load." In Advanced Electromechanical Motion Systems & Electric Drives Joint Symposium, 2009. ELECTROMOTION 2009. 8th International Symposium on, pp. 1-6. IEEE, 2009.

[8] Stemmler, H. "Power electronics in electric traction applications." In Industrial Electronics, Control, and Instrumentation, 1993. Proceedings of the IECON'93., International Conference on, pp. 707-713. IEEE, 1993.

[9] Hammond, Peter W. "A new approach to enhance power quality for medium voltage drives." In Petroleum and Chemical Industry Conference, 1995. Record of Conference Papers., Industry Applications Society 42nd Annual, pp. 231-235. IEEE, 1995.

[10] Fujita, Hideaki, Shinji Tominaga, and Hirofumi Akagi. "Analysis and design of an advanced static VAR compensator using quad-series voltage-source inverters." In Industry Applications Conference, 1995. Thirtieth IAS Annual Meeting, IAS'95., Conference Record of the 1995 IEEE, vol. 3, pp. 2565-2572. IEEE, 1995.

[11] Yoshioka, Y., S. Konishi, N. Eguchi, M. Yamamoto, K. Endo, K. Maruyama, and K. Hino. "Self-commutated static flicker compensator for arc furnaces." In Applied Power Electronics Conference and Exposition, 1996. APEC'96. Conference Proceedings 1996., Eleventh Annual, vol. 2, pp. 891-897. IEEE, 1996.

[12] Martins, António, Helder Azevedo, and José Ferreira. Active Power Filters for Harmonic Elimination and Power Quality Improvement. INTECH Open Access Publisher, 2011.

[13] Martins, António, Helder Azevedo, and José Ferreira. Active Power Filters for Harmonic Elimination and Power Quality Improvement. INTECH Open Access Publisher, 2011.

[14] Eriksson, Kjell, Tomas Jonsson, and Ove Tollerz. "Small scale transmission to AC networks by HVDC Light." In 12th Cepsi Conference, Pattaya, Thailand. 1998.

[15] Baek, Ju Won, Dong-Wook Yoo, and Heung-Geun Kim. "High-voltage switch using series-connected IGBTs with simple auxiliary circuit." IEEE Transactions on Industry Applications 37, no. 6 (2001): 1832-1839.

[16] Honghai, Kuang, and Wu Zhengqiu. "Research of super capacitor energy storage system based on DG connected to power grid." In Sustainable Power Generation and Supply, 2009. SUPERGEN'09. International Conference on, pp. 1-6. IEEE, 2009.

[17] Xisheng, Tang. "Study on SCES systems used in distributed generation system." PhD diss., Master thesis, Chinese Academy of Sciences, 2006.

[18] Najafi, Ehsan, and Abdul Halim Mohamed Yatim. "Design and implementation of a new multilevel inverter topology." IEEE Transactions on industrial electronics 59, no. 11 (2012): 4148-4154.

[19] Urmila, B., and R. Rohit. "Performance evaluation of multilevel inverter based on total harmonic distortion (THD)." International journal of engineering science & advanced technology 2 (2012): 587-593.

[20] Aljuhishi, Fares, Hosen Hasna, Nasser Aljuhaishi, Mohannad Khair Allah, Mahmoud Alahmad, and Herbert Hess. "Novel multilevel inverter topology design for adaptive dynamic systems." In Electro/Information Technology (EIT), 2015 IEEE International Conference on, pp. 410-414. IEEE, 2015.

[21] The Authoritative Dictionary of IEEE Standards Terms, Seventh Edition, IEEE Press, 2000,ISBN 0-7381-2601-2, page 588

[22] Doucet, Jim, Dan Eggleston, and Jeremy Shaw. "www. neoenerji. com." (2007).

[23] Baiju, M. R., K. K. Mohapatra, R. S. Kanchan, and K. Gopakumar. "A dual two-level inverter scheme with common mode voltage elimination for an induction motor drive." IEEE Transactions on Power Electronics 19, no. 3 (2004): 794-805.

[24] Rodríguez, José, Steffen Bernet, Bin Wu, Jorge O. Pontt, and Samir Kouro. "Multilevel voltage-source-converter topologies for industrial medium-voltage drives." IEEE Transactions on industrial electronics 54, no. 6 (2007): 2930-2945.

[25] Shukla, Anshuman, Arindam Ghosh, and Avinash Joshi. "State feedback control of multilevel inverters for DSTATCOM applications." IEEE Transactions on Power Delivery 22, no. 4 (2007): 2409-2418.

[26] Carrasco, Juan Manuel, Leopoldo Garcia Franquelo, Jan T. Bialasiewicz, Eduardo Galván, Ramón Carlos PortilloGuisado, MA Martin Prats, José Ignacio León, and Narciso Moreno-Alfonso. "Power-electronic systems for the grid integration of renewable energy sources: A survey." IEEE Transactions on industrial electronics 53, no. 4 (2006): 1002-1016.

[27] Baker, R. H., and L. H. Bannister. "Electric Power Converter. US Patent 3 867 643." Electric Power Converter. US Patent 3 867 643 (1975).

[28] Tolbert, Leon M., Fang Zheng Peng, and Thomas G. Habetler. "Multilevel converters for large electric drives." IEEE Transactions on Industry Applications 35, no. 1 (1999): 36-44.

[29] Rodriguez, Jose, Jih-Sheng Lai, and Fang Zheng Peng. "Multilevel inverters: a survey of topologies, controls, and applications." IEEE Transactions on industrial electronics 49, no. 4 (2002): 724-738.

[30] Hingorani, Narain G., and Laszlo Gyugyi. Understanding facts. IEEE press, 2000.

[31] Lai, Jih-Sheng, and Fang Zheng Peng. "Multilevel converters-a new breed of power converters." IEEE Transactions on industry applications 32, no. 3 (1996): 509-517.

[32] Baier, Carlos R., Johan I. Guzman, José R. Espinoza, Marcelo A. Pérez, and José R. Rodríguez. "Performance evaluation of a multicell topology implemented with single-phase nonregenerative cells under unbalanced supply voltages." IEEE Transactions on Industrial Electronics 54, no. 6 (2007): 2969-2978.

[33] Flores, Patricio, Juan Dixon, Micah Ortúzar, Rodrigo Carmi, Pablo Barriuso, and Luis Morán. "Static var compensator and active power filter with power injection capability, using 27-level inverters and photovoltaic cells." IEEE Transactions on Industrial Electronics 56, no. 1 (2009): 130-138.

[34] Escalante, Miguel F., and Juan Jose Arellano. "Harmonics and reactive power compensation using a cascaded H-bridge multilevel inverter." In Industrial Electronics, 2006 IEEE International Symposium on, vol. 3, pp. 1966-1971. IEEE, 2006.

[35] Malinowski, Mariusz, K. Gopakumar, Jose Rodriguez, and Marcelo A. Perez. "A survey on cascaded multilevel inverters." IEEE transactions on industrial electronics 57, no. 7 (2010): 2197-2206.

[36] Iman-Eini, Hossein, Jean-Luc Schanen, Shahrokh Farhangi, and James Roudet. "A modular strategy for control and voltage balancing of cascaded H-bridge rectifiers." IEEE Transactions on Power Electronics 23, no. 5 (2008): 2428-2442.

[37] Corzine, Keith, and Yakov Familiant. "A new cascaded multilevel H-bridge drive." IEEE Transactions on power electronics 17, no. 1 (2002): 125-131.

[38] Babaei, Ebrahim, Sara Laali, and Somayeh Alilu. "Cascaded multilevel inverter with series connection of novel H-bridge basic units." IEEE Transactions on Industrial Electronics 61, no. 12 (2014): 6664-6671.

[39] Sun, Dongsen, Baoming Ge, Fang Zheng Peng, Abu Rub Haitham, Daqiang Bi, and Yushan Liu. "A new grid-connected PV system based on cascaded H-bridge quasi-Z source inverter." In Industrial Electronics (ISIE), 2012 IEEE International Symposium on, pp. 951-956. IEEE, 2012.

[40] BAKER, R. H., 1980. Switching Circuit, U.S. Patent 4 210 826.

[41] Nabae, Akira, Isao Takahashi, and Hirofumi Akagi. "A new neutral-point-clamped PWM inverter." IEEE Transactions on industry applications 5 (1981): 518-523.

[42] Li, Jun, Subhashish Bhattacharya, and Alex Huang. "Performance comparison of a new current regulator for 3-level NPC inverter for sinusoidal and non-sinusoidal current tracking applications." In Industrial ElectroniCS, 2008. IECON 2008. 34th Annual Conference of IEEE, pp. 879-884. IEEE, 2008.

[43] Guedouani, R., B. Fiala, E. M. Berkouk, and M. S. Boucherit. "Control of capacitor voltage of three phase five-level NPC voltage source inverter. Application to inductor motor drive." In Electrical Machines and Power Electronics, 2007. ACEMP'07. International Aegean Conference on, pp. 794-799. IEEE, 2007.

[44] Dai, Ning-Yi, Man-Chung Wong, and Ying-Duo Han. "Application of a three-level NPC inverter as a three-phase four-wire power quality compensator by generalized 3DSVM." IEEE Transactions on power electronics 21, no. 2 (2006): 440-449.

[45] Rodriguez, Jose, Steffen Bernet, Peter K. Steimer, and Ignacio E. Lizama. "A survey on neutral-point-clamped inverters." IEEE transactions on Industrial Electronics 57, no. 7 (2010): 2219-2230.

[46] McGrath, Brendan Peter, and D. Grahame Holmes. "A comparison of multicarrier PWM strategies for cascaded and neutral point clamped multilevel inverters." In Power Electronics Specialists Conference, 2000. PESC 00. 2000 IEEE 31st Annual, vol. 2, pp. 674-679. IEEE, 2000.

[47] du Toit Mouton, H. "Natural balancing of three-level neutral-point-clamped PWM inverters." IEEE transactions on industrial electronics 49, no. 5 (2002): 1017-1025.

[48] Zhang, Li, Kai Sun, Lanlan Feng, Hongfei Wu, and Yan Xing. "A family of neutral point clamped full-bridge topologies for transformerless photovoltaic grid-tied inverters." IEEE Transactions on Power Electronics 28, no. 2 (2013): 730-739.

[49] Krug, H-P., Tsuneo Kume, and Mahesh Swamy. "Neutral-point clamped three-level general purpose inverter-features, benefits and applications." In Power Electronics Specialists Conference, 2004. PESC 04. 2004 IEEE 35th Annual, vol. 1, pp. 323-328. IEEE, 2004.

[50] Miyazaki, Satoshi, Shinji Tatara, and Kosaku Ichikawa. "Neutral point clamped (NPC) inverter control system." U.S. Patent 5,790,396, issued August 4, 1998.

[51] Meynard, T. A., and Henry Foch. "Multi-level conversion: high voltage choppers and voltage-source inverters." In Power Electronics Specialists Conference, 1992. PESC'92 Record., 23rd Annual IEEE, pp. 397-403. IEEE, 1992.

[52] Dijkhuizen, F. R., and J. L. Duarte. "Proper choice of flying capacitors based on distinct power dissipation models." In Industry Applications Conference, 1998. Thirty-Third IAS Annual Meeting. The 1998 IEEE, vol. 2, pp. 1174-1180. IEEE, 1998.

[53] Sinha, Gautam, and Thomas A. Lipo. "A new modulation strategy for improved DC bus utilization in hard and soft switched multilevel inverters." In Industrial Electronics, Control and Instrumentation, 1997. IECON 97. 23rd International Conference on, vol. 2, pp. 670-675. IEEE, 1997.

[54] Lee, Dong Ho, Seong R. Lee, and Fred C. Lee. "An analysis of midpoint balance for the neutral-point-clamped three-level VSI." In Power Electronics Specialists Conference, 1998. PESC 98 Record. 29th Annual IEEE, vol. 1, pp. 193-199. IEEE, 1998.

[55] Roshankumar, P., P. P. Rajeevan, K. Mathew, K. Gopakumar, Jose I. Leon, and Leopoldo G. Franquelo. "A five-level inverter topology with single-DC supply by cascading a flying capacitor inverter and an H-bridge." IEEE Transactions on Power Electronics 27, no. 8 (2012): 3505-3512.

[56] Zhang, Richard, Dushan Boroyevich, V. Himamshu Prasad, H-C. Mao, Fred C. Lee, and Stephen Dubovsky. "A three-phase inverter with a neutral leg with space vector modulation." In Applied Power Electronics Conference and Exposition, 1997. APEC'97 Conference Proceedings 1997., Twelfth Annual, vol. 2, pp. 857-863. IEEE, 1997.

[57] Thielemans, Steven, T. J. Vyncke, and J. A. A. Melkebeek. "Voltage quality analysis of a three-level flying capacitor inverter with model based predictive control." In Power Electronics and ECCE Asia (ICPE & ECCE), 2011 IEEE 8th International Conference on, pp. 124-131. IEEE, 2011.

[58] Escalante, Miguel F., J-C. Vannier, and Amir Arzandé. "Flying capacitor multilevel inverters and DTC motor drive applications." IEEE Transactions on Industrial Electronics 49, no. 4 (2002): 809-815.

[59] Davoodnezhad, Reza, Donald Grahame Holmes, and Brendan P. McGrath. "A novel three-level hysteresis current regulation strategy for three-phase three-level inverters." IEEE Transactions on Power Electronics 29, no. 11 (2014): 6100-6109.

[60] Peng, F.Z., Lai, J.S., McKeever, J.W. and VanCoevering, J., 1996. A multilevel voltage-source inverter with separate DC sources for static var generation. IEEE Transactions on Industry Applications, 32(5), pp.1130-1138.

[61] Newton, C., and M. Summer. "Multi-level convertors a real solution to medium/high-voltage drives?." Power Engineering Journal 12, no. 1 (1998): 21-26.

[62] Holmes, D. Grahame, and Thomas A. Lipo. Pulse width modulation for power converters: principles and practice. Vol. 18. John Wiley & Sons, 2003.

[63] Axelrod, Boris, Yefim Berkovich, and Adrian Ioinovici. "A cascade boost-switched-capacitor-converter-two level inverter with an optimized multilevel output waveform." IEEE Transactions on Circuits and Systems I: Regular Papers 52, no. 12 (2005): 2763-2770.

[64] Rodríguez, José, Jorge Pontt, Pablo Lezana, and Samir Kouro. "Tutorial on multilevel converters." In International Conference on Power Electronics and Indtelligent Control for Energy Conservation. 2005.

[65] Rodríguez, José, Luis Morán, Pablo Correa, and Cesar Silva. "A vector control technique for medium-voltage multilevel inverters." IEEE Transactions on Industrial Electronics 49, no. 4 (2002): 882-888.

[66] Chiasson, John N., Leon M. Tolbert, Keith J. McKenzie, and Zhong Du. "A unified approach to solving the harmonic elimination equations in multilevel converters." IEEE Transactions on power electronics 19, no. 2 (2004): 478-490.

[67] Rodríguez, José, Luis Morán, Pablo Correa, and Cesar Silva. "A vector control technique for medium-voltage multilevel inverters." IEEE Transactions on Industrial Electronics 49, no. 4 (2002): 882-888.

[68] Kazerani, Mehrdad, and B-T. Ooi. "Feasibility of both vector control and displacement factor correction by voltage source type AC-AC matrix converter." IEEE Transactions on Industrial Electronics 42, no. 5 (1995): 524-530.

[69] Abe, R., Y. Nagai, K. Tsuyuki, H. Nishikawa, T. Shimamura, A. Kawaguchi, and K. Shimada. "Development of multiple space vector control for direct connected parallel current source power converters." In Power Conversion Conference-Nagaoka 1997., Proceedings of the, vol. 1, pp. 283-288. IEEE, 1997.

[70] Li, Li, Dariusz Czarkowski, Yaguang Liu, and Pragasen Pillay. "Multilevel selective harmonic elimination PWM technique in series-connected voltage inverters." IEEE Transactions on Industry Applications 36, no. 1 (2000): 160-170.

[71] Agelidis, Vassilios G., Anastasios I. Balouktsis, and Mohamed SA Dahidah. "A five-level symmetrically defined selective harmonic elimination PWM strategy: Analysis and experimental validation." IEEE Transactions on Power Electronics 23, no. 1 (2008): 19-26.

[72] Kavousi, Ayoub, Behrooz Vahidi, Reza Salehi, Mohammad Kazem Bakhshizadeh, Naeem Farokhnia, and S. Hamid Fathi. "Application of the bee algorithm for selective harmonic elimination strategy in multilevel inverters." IEEE Transactions on power electronics 27, no. 4 (2012): 1689-1696.

[73] Nabae, Akira, Isao Takahashi, and Hirofumi Akagi. "A new neutral-point-clamped PWM inverter." IEEE Transactions on industry applications 5 (1981): 518-523.

[74] Rotella, Mauricio, Gonzalo Peñailillo, Javier Pereda, and Juan Dixon. "PWM method to eliminate power sources in a nonredundant 27-level inverter for machine drive applications." IEEE Transactions on Industrial Electronics 56, no. 1 (2009): 194-201.

[75] Mohan, Ned, and Tore M. Undeland. Power electronics: converters, applications, and design. John Wiley & Sons, 2007.

[76] Mahdavi, J., A. Agah, A. M. Ranjbar, and H. A. Toliyat. "Extension of PWM space vector technique for multilevel current-controlled voltage source inverters." In Industrial Electronics Society, 1999. IECON'99 Proceedings. The 25th Annual Conference of the IEEE, vol. 2, pp. 583-588. IEEE, 1999.

[77] Celanovic, Nikola, and Dushan Boroyevich. "A fast space-vector modulation algorithm for multilevel three-phase converters." IEEE transactions on industry applications 37, no. 2 (2001): 637-641.

[78] Wei, Sanmin, Bin Wu, Fahai Li, and Congwei Liu. "A general space vector PWM control algorithm for multilevel inverters." In Applied Power Electronics Conference and Exposition, 2003. APEC'03. Eighteenth Annual IEEE, vol. 1, pp. 562-568. IEEE, 2003.

[79] Strom, J-P., J. Tyster, J. Korhonen, K. Rauma, H. Sarén, and P. Silventoinen. "Active du/dt filtering for variable-speed AC drives." In Power Electronics and Applications, 2009. EPE'09. 13th European Conference on, pp. 1-10. IEEE, 2009.

[80] McGrath, Brendan Peter, Donald Grahame Holmes, and Thomas Lipo. "Optimized space vector switching sequences for multilevel inverters." IEEE Transactions on power electronics 18, no. 6 (2003): 1293-1301.

[81] Lauttamus, P., and H. Tuusa. "Unified space-vector modulation scheme for multilevel inverters." In Power Conversion Conference-Nagoya, 2007. PCC'07, pp. 1464-1471. IEEE, 2007.

[82] Kumar, A. Rakesh, V. Karthikeyan, and V. Jamuna. "A MULTILEVEL INVERTER WITH REDUCED NUMBER OF SWITCHES."

[83] Song, Qiang, Wenhua Liu, and Zhichang Yuan. "Multilevel optimal modulation and dynamic control strategies for STATCOMs using cascaded multilevel inverters." IEEE transactions on power delivery 22, no. 3 (2007): 1937-1946.

[84] Bracewell, Ronald Newbold, and Ronald N. Bracewell. The Fourier transform and its applications. Vol. 31999. New York: McGraw-Hill, 1986.

[85] Abulma'atti, M. T. "Simple method for calculating Fourier coefficients of experimentally obtained waveforms." IEE Proceedings-Science, Measurement and Technology 141, no. 3 (1994): 177-178.

[86] McLaren, Peter Grant, and M. A. Redfern. "Fourier-series techniques applied to distance protection." In Proceedings of the Institution of Electrical Engineers, vol. 122, no. 11, pp. 1301-1305. IET Digital Library, 1975.

[87] Mohan, Ned, and Tore M. Undeland. Power electronics: converters, applications, and design. John Wiley & Sons, 2007.