VIBRATION ANALYSIS OF ELECTROPLATED COPPER COMPLIANT INTERCONNECTS

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VIBRATION ANALYSIS OF ELECTROPLATED COPPER COMPLIANT INTERCONNECTS

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LIST OF SYMBOLS AND ABBREVIATIONS

IC	Integrated Circuit
RF	Radio Frequency
I/O	Input/Output
BGA	Ball Grid Array
CTE	Coefficient of Thermal Expansion
LCF	Low Cycle Fatigue
HCF	High Cycle Fatigue
TAB	Tape Automated Bonding
CPB	Copper Pillar Bump
CNT	Carbon Nanotube
WAVE	Wide Area Vertical Expansion
FEA	Finite Element Analysis
SEM	Scanning Electron Microscope
TSV	Through Silicon Via
PSD	Power Spectral Density
RMS	Root Mean Square
PDF	Probability Density Function
FFT	Fast Fourier Transform
ω	Angular Frequency
Q	Q Factor
RPSD	Response Power Spectral Density
CDI	Cumulative Damage Index

S-N	Stress-Life
SAC	Tin-Silver-Solder (Sn-Ag-Cu)
E-N	Strain-Life
PCB	Printed Circuit Board
TCB	Thermo-Compression Bonding
NSMD	Non-Solder Mask Defined
SMD	Solder Mask Defined
ENEPIG	Electroless Nickel Electroless Palladium Immersion Gold
IPA	Isopropyl Alcohol
LDV	Laser Doppler Vibrometer
DAQ	Data Acquisition
E	Young's/Elastic Modulus
G	Shear Modulus
v	Poisson's Ratio
C	Compliance
δ	Displacement
ρ	Density
V_p	Percent Volume
DOF	Degrees of Freedom
ξ	Damping Ratio
Δf	Half Power Bandwidth
f_n	Natural Frequency
σ_f'	Fatigue Strength Coefficient
b	Fatigue Strength Exponent

SUMMARY

Microelectronic packaging interconnects are subjected to mechanical damage due to thermal and power cycles, drop impact shock, and various vibration loads during application. As traditional microelectronic packaging interconnects are rigid, compliant interconnects are being pursued to facilitate more independent deformation between the substrate and the die while experiencing lower stress and strain, thus improving the overall mechanical reliability. However, though there have been studies that examine these interconnects under thermal fatigue and drop testing, the literature on vibration loading is scarce.

This thesis characterizes the response of a compliant microelectronic packaging interconnect under random vibration loading and develops an assembly process flow that produces the most reliable bonded structures for testing. The interconnect used in the study is a 3-arc electroplated copper structure that serves as the Second-Level packaging interconnect. Random vibration loading is selected instead of sine sweep loading, as it produces a more realistic simulation of the conditions during application. A power spectral density spectrum analysis is used to calculate the stresses experienced under such fatigue loading through finite-element simulations. In parallel, silicon dies with compliant interconnects are assembled on organic substrates, and experimental vibration testing is conducted to determine the interconnect fatigue life. Based on simulations and experiments, a high cycle fatigue prediction methodology is developed for the compliant interconnect that can be employed for future design and analysis of compliant interconnects for various applications.

CHAPTER 1

INTRODUCTION

Microelectronics is a branch within the electronics industry that studies and fabricates miniaturized devices. These devices combine transistors, capacitors, inductors, resistors, semiconductors, diodes, and many other components to form integrated circuits (IC) that provide a variety of functions such as signal processing, radio frequency (RF) amplifying, and sensing [1]. Microelectronic packaging is an important area of microelectronics that which focuses on integrating ICs into a single system and protecting it from damage. By packaging microelectronics, power and signal distribution, structural protection, thermal regulation, electrical interconnection, and input/output (I/O) scaling of the system can be achieved [2]. Advances in semiconductor technology for the last few decades have continuously pushed the microelectronic industry towards producing smaller and denser packages, which provide better performance at a fraction of the previous size. This trend was first observed by Gordon Moore of Intel in 1965, who predicted that the number of transistors on an IC would double every year [3]. Known as Moore's law, the time prediction was later revised to approximately every two years as seen in Figure 1-1.

The rapid development in the miniaturization of microelectronics is achieved through technological advancements in every aspect of packaging. This involves material research, fabrication and assembly process development, substrate and interposer improvement, mechanical reliability, electrical performance, and cost analysis. One such area is the interconnect that provide both mechanical and electrical connections between

the different components of the package [4]. These interconnections are vital at all packaging levels and come in many forms.

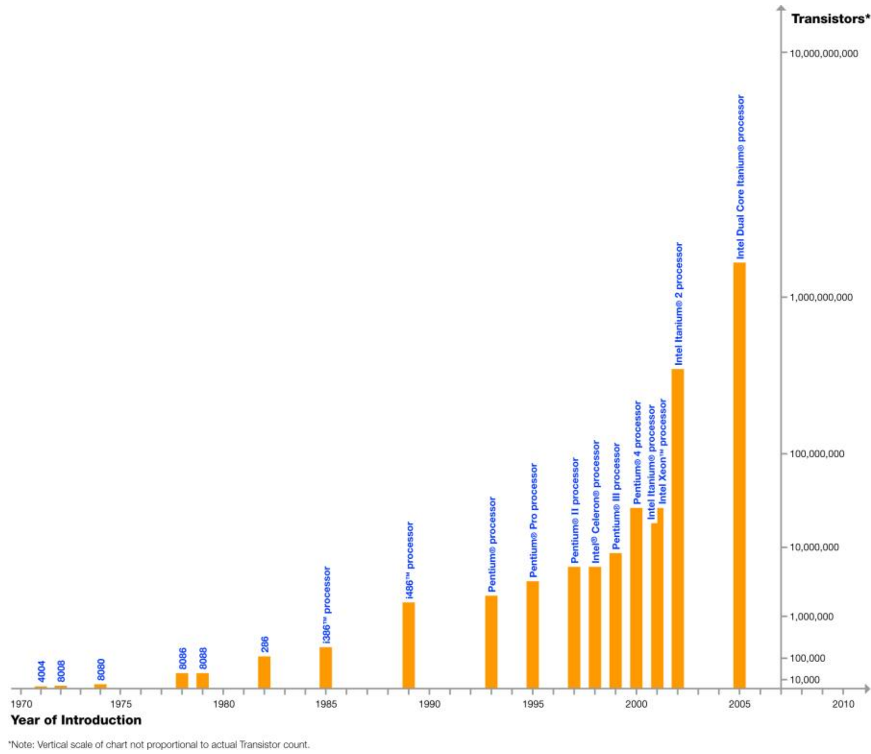


Figure 1-1 Moore's Law [5]

There are four main levels in the interconnect packaging hierarchy starting at the Zeroth-Level (Wafer-Level), which form gate-to-gate interconnection directly on the silicon wafer [6]. The First-Level (Chip/IC-Level) interconnects provide chip-to-substrate package connections. The Second-Level (Board/System-Level) interconnects provide substrate-to-board connections [7]. And the Third-Level interconnects provide system-to-system connections between motherboards. In some classifications, an additional level is added above the Third-Level to indicate the connection between subassemblies. Figure 1-2 displays the integration of different interconnect levels into a single microelectronic

package. A microelectronic package with multiple levels benefits from interchangeability, manufacturability, I/O redistribution, and higher reliability.

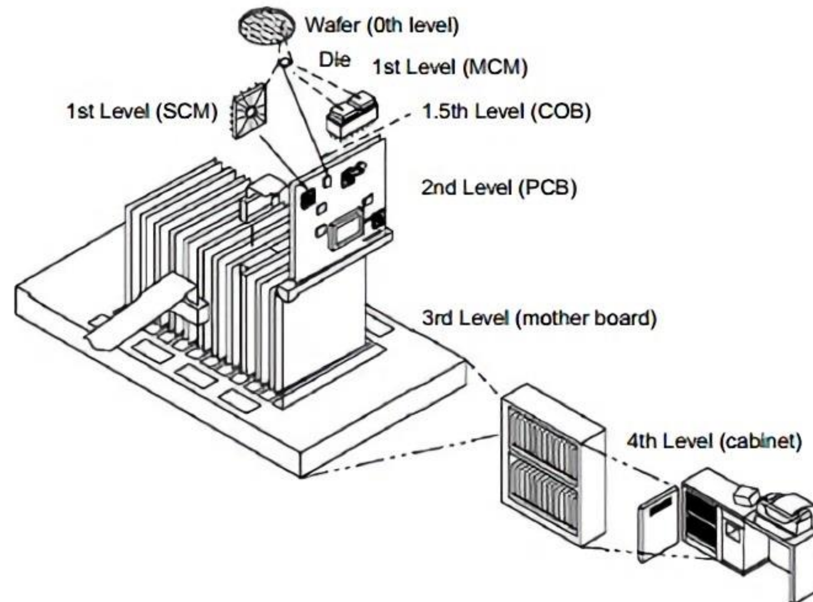


Figure 1-2 Interconnect Packaging Levels [8]

There are many types of interconnects, each with its own advantages and disadvantages that make them suitable for specific applications. Common types of interconnects include, wires, pins, solder balls, and thin films. The connections at each level can be joined or bonded through a variety of methods, such as epoxy bonding, thermo-compression bonding, laser welding, and low temperature glass bonding through processes like reflow, flip chip, and wire bonding [9]. For the microelectronic package to continuously function, interconnects must be robust and reliable enough to maintain both the electrical and mechanical connection under damaging situations. Unfortunately, the interconnect structures experience significant amounts of mechanical stress compared to

other locations in the package, making it one of the most common causes of failure for microelectronics.

Traditional rigid ball grid array (BGA) solder balls are the primary type of Second-Level interconnects used in microelectronic packages. Under normal application, the BGA is subject to mechanical damage accumulated through thermal and power cycles, bending loads, drop impact shock, and vibration loads. Thermal and power cycles are one of the most studied aspect of interconnect failure because of its prevalence [10]. The package is put through cycles of heating and cooling either through environmental factors or the usage of the system itself. The difference in material and coefficient of thermal expansion (CTE) between two components will incur mechanical stresses and eventual low cycle fatigue (LCF) failure by stretching and compressing the interconnects that connect them. This holds especially true for Second-Level interconnects between the board and substrate due to the relatively large scale variance of the bonded components. Figure 1-3 demonstrates this warpage caused by CTE mismatch during thermal cycling. Bending stresses contribute another type of damage to the interconnect that causes crack propagation and delamination. Drop impact shock occurs in situations such as accidentally dropping a smartphone onto a hard surface, where the entire package experiences intense peaks of stress and strain that causes fast fracture. And in the case of vibration loads, which happens frequently during shipping and regular use, the microelectronic package undergoes high cycle fatigue (HCF) that further harms the interconnect. Other non-mechanical forms of failure include moisture absorption and electromigration [11].

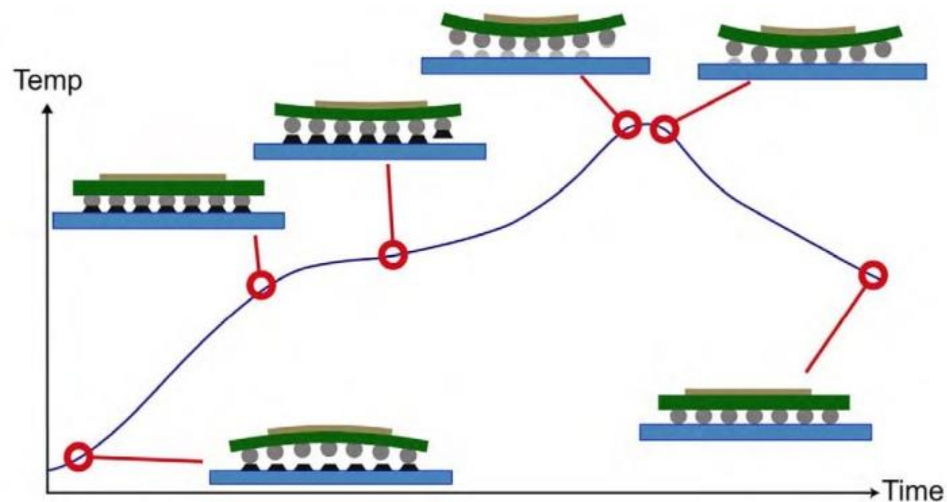


Figure 1-3 CTE Mismatch from Thermal Cycle [12]

Therefore, continuous efforts have been made to reinforce the interconnect structures and extend the life of microelectronic packages. One solution is to fill the gap between the substrate and package with organic support material through capillary flow in a process known as underfilling [13]. Material research on interconnects as well as the substrate and interposer are also being conducted to increase the adhesion strength due to the recent integration of low-k dielectrics [14]. Another area focuses on developing different types of surface finishes and solder dopants used in the fabrication and assembly process that produces stronger intermetallic layers during bonding [15]. However, most of these methods do not completely eliminate the reliability issue of interconnects and introduce problems in other regions. Thus, in recent years, compliant interconnects are being explored as an alternative to traditional BGAs to increase the mechanical reliability of microelectronic packages.

Compliant interconnects offer additional mechanical reliability to microelectronic packages by providing a spring-like effect during package warpage and deformation, which

reduces the overall stresses and strains experienced by the system. The added compliance is achieved through changes in material, geometry, structure, or a combination of them. A variety of compliant interconnect designs have already been proposed and analyzed. For example, pillar bumps, micro-springs, and helix-shaped compliant interconnects. Figure 1-4 shows a type of helix-shaped compliant interconnect. However, compliant interconnects are not without its drawbacks. Because of their relatively complex structure, additional time and steps need to be implemented in both fabrication and assembly in the manufacturing process, which increases production cost, especially when there can be well over thousands of interconnects on a single chip. Compliant interconnects also suffer from a decrease in electrical performance, usually due to the smaller cross sectional area and longer length for current flow, inducing higher electrical parasitics [16]. This tradeoff between mechanical reliability, electrical performance, and cost is one of the main reasons compliant interconnects have not been widely adopted by industry today.

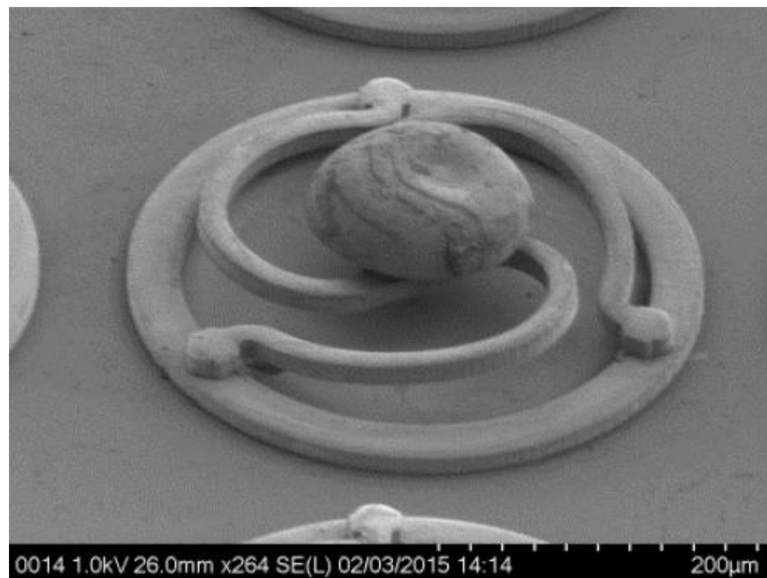


Figure 1-4 SEM Image of 3-Arc-Fan Compliant Interconnect [17]

To summarize, the continuous miniaturization of microelectronic packages, as predicted by Moore's law, requires advancements in interconnect technology. Second-Level interconnects are often the primary mode of failure in these packages from CTE mismatch and other forms of stress inducing loads. In order to increase mechanical reliability, compliant interconnects are being examined as an alternative to replace traditional rigid solder ball BGAs and alleviate the high loads placed on the system. To accomplish this, further reliability studies and analyzes need to be performed to characterize the different compliant interconnect designs.

CHAPTER 2

LITERATURE REVIEW

An overview of existing Second-Level compliant interconnect designs and mechanisms as well as various reliability testing methods will be reviewed in this chapter. In particular, the 3-Arc-Fan compliant interconnect design chosen for this research and vibration fatigue testing methods will be examined in greater detail.

2.1. Compliant Interconnects

Most compliant interconnects are being developed for the First and Second-Level of the packaging hierarchy. As explained previously, First-Level packaging interconnects are the level of interconnections between the chip and the substrate. While those at the Second-Level are between the substrate and board. These interconnects are typically bonded through methods like wire bonding, tape automated bonding (TAB), and flip chip technology [18]. This section will focus on three main categories of compliant interconnects, pillars, intrinsically strained, and 3D.

2.1.1. Pillar Interconnects

Compliant interconnects in the form of columns or pillars are among the first type of alternatives introduced to improve mechanical reliability. These structures are usually fabricated as a single metallic column, though more recent designs have examined the possible use of carbon and polymer nanowires. One of the first forays into pillar bump design was Topper's double ball structure developed in 2000, which attempted to reduce interconnect stress by stacking two solder balls together [19]. Shortly after, IBM patented

a pillar bump design in 2001 that featured a two layer copper pillar bump (CPB) as seen in Figure 2-1 [20]. Some other similar CPBs include Wang's structure developed in 2001 [21], Srinivasa et al.'s Bed of Nails design from 2004 [22], and Intel's CPB patent issued in 2007 [23].

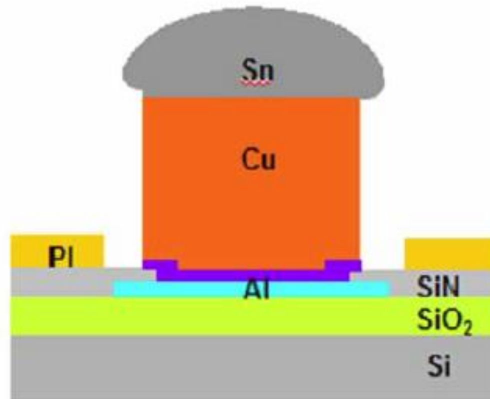


Figure 2-1 IBM's First CPB Structure [24]

Nanowire pillars are a more recent advancement that evolved from CPBs. These pillars are classified by their higher aspect ratio, where several nano-scale wires are grouped together in an array to form a single larger pillar. Due to their structural design and thinner individual column, the overall compliance of nano-pillars tend to be higher than those of CPB. Several types of nano-pillars have been studied, including the copper microwire array developed by Georgia Tech presented in Figure 2-2 [25], Liao et al.'s multicopper-column presented in Figure 2-3 [26], and Chow and Sitaraman's copper nanowires, which also act as high performance thermal interface material [27]. Both the CPBs and nano-pillars mentioned up to this point have been fabricated from electroplated copper because of its superior electrical, thermal, and structural material properties [24].

However, another type of material that has seen widespread use in nanowires are carbon nanotubes (CNT) [28]. Ginga has implemented low-modulus CNT forests that increases reliability [29]. Generally, CNTs offer excellent compliance, thermal, and electrical performance, but are harder to fabricate and assemble [30].

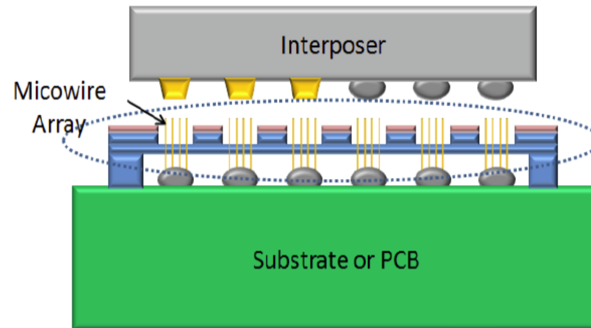


Figure 2-2 Schematic of Copper Microwire Array Interconnects [25]

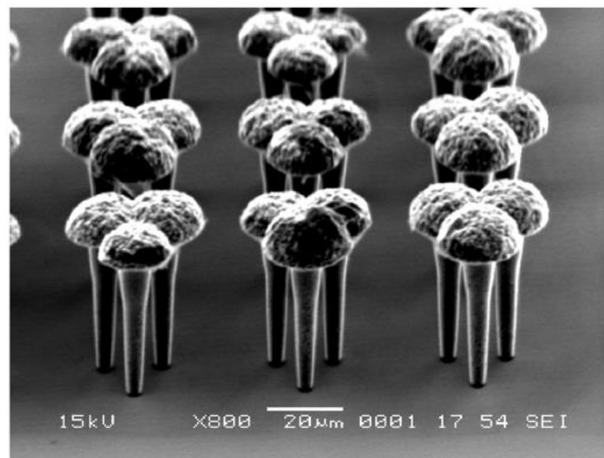


Figure 2-3 SEM Image of Multicopper-column Interconnects [26]

Various reliability studies have been conducted on pillar interconnects in the form of shear and drop impact failure tests [31], crack analysis [32], and thermal fatigue prediction models [33]. In general, pillar interconnects have higher electrical and thermal

conductance and mechanical reliability than traditional BGAs and aids in the miniaturization of packages with smaller pitches. However, they lack the self-alignment of solder balls during assembly and also introduce new forms of failure with the incorporation of copper and low-k dielectrics into the interconnect.

2.1.2. Intrinsically Strained Interconnects

Another classification of compliant interconnects is intrinsically strained interconnects. These compliant interconnects share the same fabrication method known as the stress-engineered thin film process, which builds up intrinsic strains during metal sputter deposition through a pressure gradient that, when released, causes the interconnect structure to curl up and acts as a spring [34]. Some interconnects designed with this method are the J-Springs shown in Figure 2-4 proposed by Georgia Tech in 2002 [35] and the Microsprings developed by Xerox in 2012 [36].

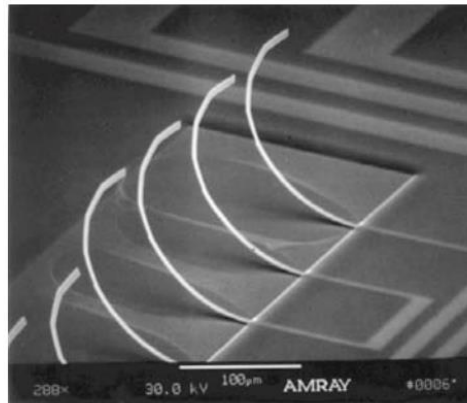


Figure 2-4 SEM Image of J-Spring Interconnects [34]

Overall, intrinsically strained interconnects provide the highest compliance out of the three main types of compliant interconnects. The long and slender profile allows the

material to freely deform during loading with minimal transfer of stresses. However, this same profile also causes it to have the worst electrical performance out of the three types. In addition, similar to pillar interconnects, the fabrication and assembly process require greater investment, which makes it unappealing for industrial use. For these types of interconnects to be viable alternatives, more testing and analyzes need to be conducted.

2.1.3. 3D Interconnects

3D interconnects is the final category of compliant interconnects. These interconnects are, as their name suggests, identified by their free standing and out-of-plane 3-dimensinoal structures. The complex geometries of 3D compliant interconnects allow for greater variance in their design, which is evident in their diverse form factors. A few example of 3D interconnects are Tessera's Wide Area Vertical Expansion (WAVE) interconnects [37], Georgia Tech's Sea of Leads seen in Figure 2-5 [38], and NASA's Micro-coil Spring interconnects [39].

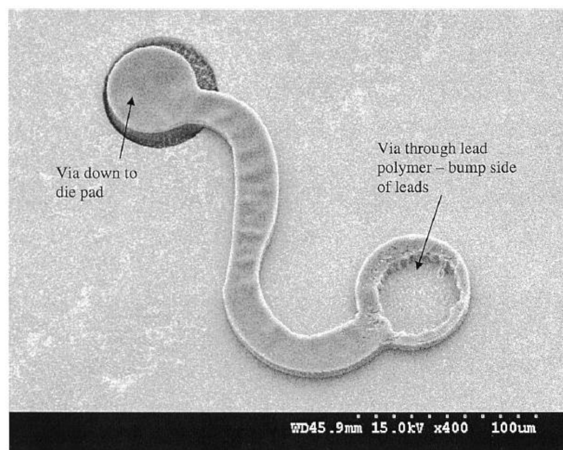


Figure 2-5 SEM Image of Sea of Leads Interconnect [40]

A subcategory of 3D interconnects are the helix-shaped interconnects being developed at Georgia Tech. This includes the β–Helix [41], G–Helix [42], and FlexConnects [43]. These structures are fabricated through a series of laminating, patterning, electroplating, etching, and masking, and feature multiple arcuate beams that provide the additional compliance. Figure 2-6 exhibits the helical nature of these 3D interconnects. A wide range of thermal, structural, and electrical tests in combination with finite element analysis (FEA) have been performed for these compliant interconnects. It is demonstrated that this type of design successfully transfers the stresses from the solder bonding interface to the arcuate arms, and the incorporation of multiple arms in later iterations improves electrical performance [44].

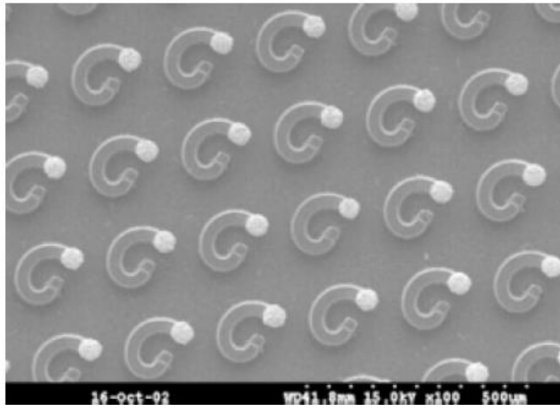


Figure 2-6 SEM Image of G–Helix Interconnects [45]

Due to the complex structures of 3D compliant interconnects, fabrication at a smaller scale is more difficult when compared to pillar and intrinsically strained interconnects. Therefore, they are more suitable for use in Second-Level packaging. The latest iteration of 3D interconnects that progressed from previous designs is the 3-Arc-Fan compliant interconnect undergoing research at Georgia Tech.

2.1.4. 3-Arc-Fan Compliant Interconnect

The 3-Arc-Fan, or TriDelta, compliant interconnect is an interconnect design with three electroplated copper arcuate beams that connect to an annular copper pad above and a Tin-Silver (SnAg) solder ball below. Scanning electron microscope (SEM) images that show this structure can be viewed in Figure 2-7. The three arms provide higher compliance than solder balls and create redundant electrical paths for higher electrical performance. The width of these arcuate beams can be adjusted to alter compliance, mechanical reliability, and electrical performance. The multiple path design also adds additional reliability by maintaining both mechanical and electrical connection in the event of failure in one or two paths. These arcuate beams effectively decouple the substrate and board and minimizes the stress experienced by the package.

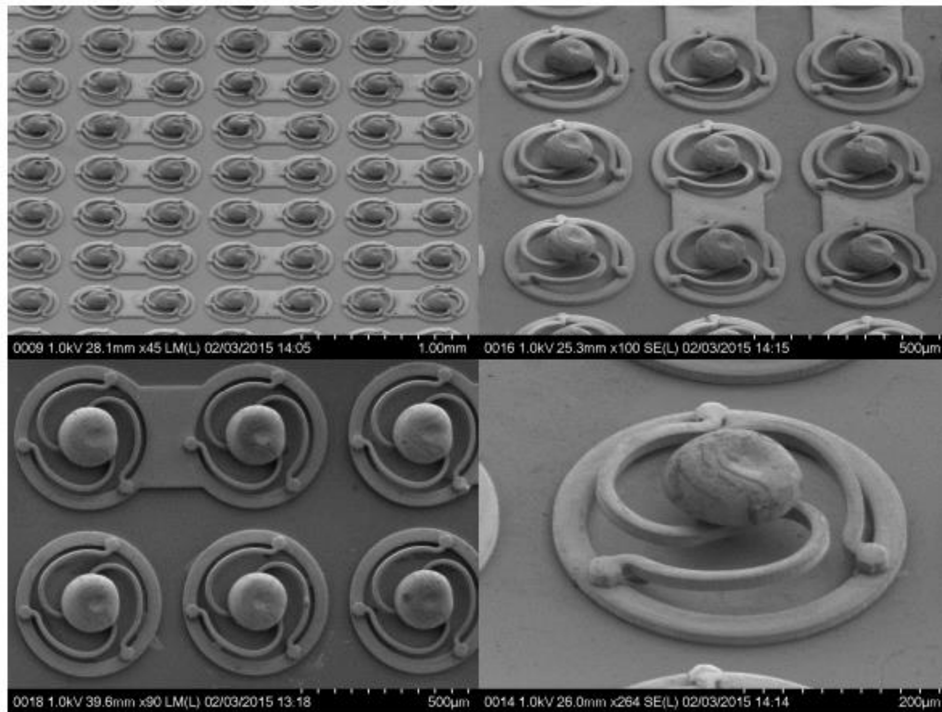


Figure 2-7 SEM Images of 3-Arc-Fan Compliant Interconnects with 15 µm Beam Width [17]

During the design of 3-Arc-Fan interconnects, similar structures with two and four arcuate beams were also proposed. However, the 3-Arc-Fan design was ultimately chosen as the superior proposal in terms of the balance between mechanical and electrical performance [46]. Analytical compliant studies have been performed on the 3-Arc-Fan with FEA and 3D printed scaled-up models for design validation and geometrical parameterization [47]. A total of eight design variables were identified for the design and optimized for mechanical and electrical performance through response surface methodology and the method of global criterion [48]. This led to the development of three main types of samples with different arcuate beam widths, 10, 15, and 20 μm for use in Second-Level packaging. The design variables are given in Figure 2-8 with their optimized values provided in Table 2-1. Additionally, a set of normalized design variables were calculated to allow for scaling and use as First-Level packaging interconnects.

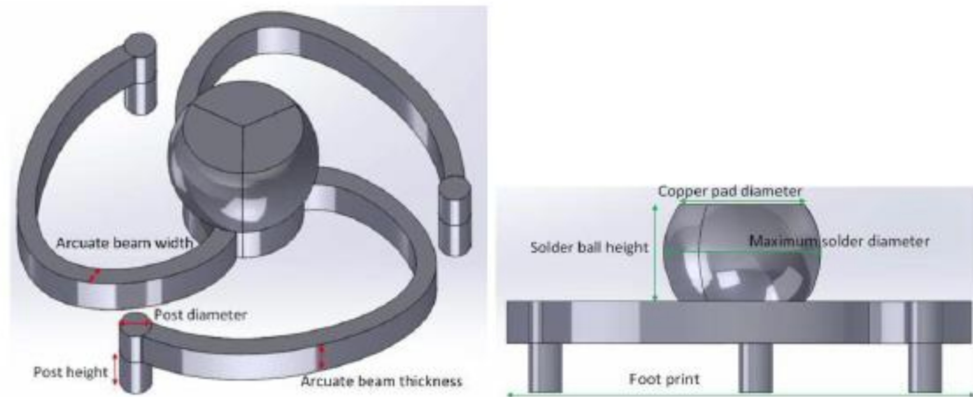


Figure 2-8 Design Variables for 3-Arc-Fan Compliant Interconnect [48]

Table 2-1 Optimized 3-Arc-Fan Interconnect Geometry (Unit: μm) [48]

Arcuate Beam Width	Arcuate Beam Thickness	Post Height	Post Diameter	Cu Pad Diameter	Solder Ball Height	Max Solder Diameter	Footprint
10/15/20	13.2	23.7	10.6	40	30	50	140

Several tests, simulations, and analyses have already been performed for the 3-Arc-Fan compliant interconnects. As mentioned in the previous chapter, thermal cycling is the primary mode of failure in most microelectronic packages and the most studied aspect of mechanical failure. The 3-Arc-Fan has been tested for thermal cycling fatigue using JEDEC standard JESD22-A104D and a low cycle thermal fatigue life prediction model was developed in conjunction with FEA simulations using a modified Coffin-Manson equation [17]. Drop testing utilizing the Input-G method has also been conducted under JEDEC standard JESD22-B111 to demonstrate the impact isolating effects of the 3-Arc-Fan interconnect [49]. Various electrical and compliance tests have been studied as well. Overall, the 3-Arc-Fan compliant interconnects are a viable alternative to traditional solder ball BGAs and offer compliance values that are several times higher. The multi-path design also allows it to perform better electrically than the other types of compliant interconnects discussed in this chapter. Therefore, the integration of 3-Arc-Fan interconnects into Second-Level packaging will significantly enhance the reliability of microelectronic packages.

2.2. Mechanical Reliability Testing of Interconnects

Reliability testing of both rigid and compliant interconnects are necessary in order to verify the integrity of microelectronic packages. In terms of mechanical reliability, thermal cycling and drop testing are the predominant methods and are well established in literature. However, microelectronic packages also experience vibration loads during application and transportation. Typically, the failure location of traditional BGAs occur at the interface or joint where the solder bonds to the die, substrate, or board. Compliant interconnects seek to increase reliability by reducing and transferring the stresses at these

interfaces to the compliant structures. This section will cover three types of testing, thermal, drop, and vibration as well as the different methods applied to analyze each failure mode.

2.2.1. Thermal Cycling

Thermal and power cycling are very similar in the sense that the package undergoes periods of heating and cooling for both cycles and will be jointly discussed for the purposes of this review. The changes in temperature causes warpage in the die, substrate, and board, and the difference in material and dimensions cases CTE mismatch where one component deforms more than the other. This difference in deformation between the top and bottom component will apply high stresses onto the interconnects, especially at the corners of the array, where the differential displacement is more pronounced. As the interconnect experiences these cycles, they will eventually fail under thermos-mechanical fatigue. The prevalence of thermal cycles in most microelectronic packages makes it one of the most common forms of failure and is the primary method for testing interconnect reliability.

Many testing methods have been employed to investigate the thermo-mechanical reliability of various interconnects, from rigid solder balls and compliant interconnects to through silicon vias (TSV) and thin films [50-52]. Accelerated thermal testing standards are typically utilized with a combination of FEA [10, 53]. Both lead free solder and copper materials used in compliant interconnects are well defined in terms of thermal analysis. Strain-life relationships, such as the Coffin-Manson equation, are most commonly used to predict fatigue failure [54-56].

2.2.2. Drop Testing

Drop testing is another frequently applied method to determine the reliability of solder joints and compliant interconnects. It has risen to prominence with the increased popularity of handheld electronics, such as smartphones, that are extremely susceptible to accidental drops. Instead of characterizing fatigue failure like thermal cycling, drop testing emphasizes fast fracture and impact isolation analysis. Explicit dynamic FEA with submodeling is used to simulate these drop events [57, 58]. Recent efforts have also applied the implicit Input-G method to perform simulations [59, 60]. Various effects of material composition, surface finish, and interconnect geometry have been extensively studied [61, 62]. Other structural loads, such as shear and bending, are often combined alongside drop testing for analysis.

2.2.3. Vibration Loading

Compared to thermal cycling and drop testing, vibration loading is a much less studied area of microelectronic package failure. However, it is just as important as the other two types of reliability testing, especially when the package is used in vehicles, aircraft, and spacecraft, where intense vibrations are continuous. Traditionally, vibration analysis have mostly been investigated in the field of civil engineering, which includes structures like train bridges and wind turbines [63, 64]. These structures experience large sinusoidal excitations during operation that can potentially lead to fatigue failure. Only recently has vibration loading been studied in the field of microelectronic packaging.

One of the earliest vibrations research in microelectronic packages was conducted in 1999 by Wong et al., which modeled a strain-life prediction for solder BGAs under vibration fatigue [65]. More vibration reliability testing was performed by Yang et al. in 2002 on plastic BGAs [66], and Pang et al. in 2004 on flip chips [67]. Another more recent

trend is to simultaneously apply thermal and vibration loads in combined loading to mimic situations such as cooling a computer with a spinning fan [68-70]. Most of the earlier methods excited the interconnects through steady sine waves or sinusoidal sweeps, and predicted fatigue life with strain-life relationships. The FEA simulations focused on global-local models and transient analysis in the time domain [71, 72]. However, the past couple of years has seen an increase in testing with random vibrations characterized in the frequency domain, which provide a more realistic simulation of the actual vibration loads experienced by microelectronic packages during their lifespan.

2.3. Random Vibration Loading

The theory of random vibration was first introduced by Albert Einstein in 1905 in his paper on Brownian motion [73] and later expanded upon by Norbert Weiner with his theory of power spectral density (PSD) in 1930 [74]. Random vibration testing was first used in the civil and aerospace industry to simulate the vibrations experienced by buildings during earthquakes and aircraft during takeoff and landing. It was not until recently that microelectronic packages were tested under random vibration conditions. This section will discuss the difference between random and sine vibration and the theory and analysis behind it.

2.3.1. Sine vs. Random Vibration Testing

The main difference between sine and random vibration testing is the input waveform used to excite the test sample. Sine testing is performed with steady sine waves at a set frequency, usually at the major natural frequency of the sample. On the other hand,

random vibration excites the sample in a set bandwidth, which simultaneously hits all the natural frequencies of the sample. A comparison of the time history plots of sine and random vibration can be seen in Figure 2-9. These time histories can be transformed into frequency spectrums through Fourier transforms. A comparison of the two frequency spectrums can be seen in Figure 2-10. For sine vibration testing, the displacement time history is commonly used in transient analyses; for random vibration testing, the acceleration frequency spectrum is typically used in spectrum analyses. Besides the difference in the time and frequency domain, sine wave intensity is parameterized by peak values, while random vibration intensity is parameterized by root mean square (RMS) values. In addition to pure sine and random vibrations, sine-on-random loading is also sometimes used to characterize situations such as helicopters, where smaller random vibrations occur alongside larger sine vibrations caused by the rotor.

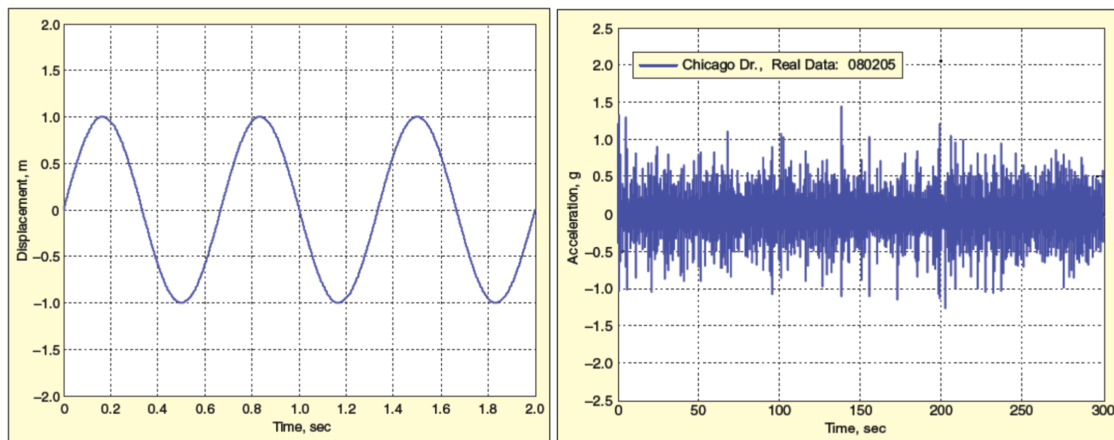


Figure 2-9 Comparison of Sine (Left) and Random (Right) Vibration Time History [75]

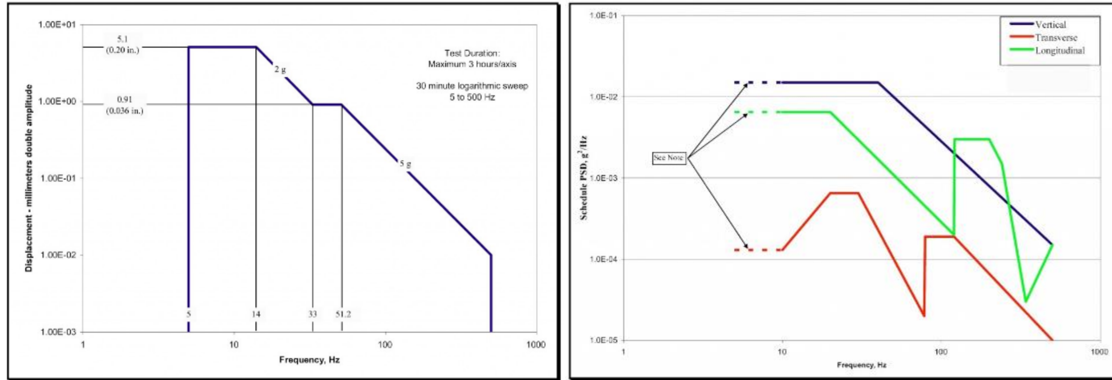


Figure 2-10 Comparison of Sine (Left) and Random (Right) Frequency Spectrums [76]

Sine and random vibration testing each have their own specific uses. Sine testing in the form of swept sine tests is an efficient method of identifying the resonant or natural frequencies of a system. It is also utilized to simulate vibration environments with repeating motions, such as motors or turbines. Random vibration testing, on the other hand, is a more realistic simulation of the loads experienced by microelectronic packages under daily application. Therefore, it is more suitable for accelerated fatigue testing of interconnect reliability than sine vibration [75, 77].

2.3.2. Power Spectral Density

Power spectral density is a statistical measurement of a signal's power distribution in the frequency domain. This concept is the primary method used to analyze random vibrations. To understand PSD, the mechanics behind random vibrations must first be investigated. Most random vibration signals used for testing follow a Gaussian distribution, though there are a few that follow Weibull distributions. The probability density function (PDF) of a Gaussian distribution is plotted in Figure 2-11. It follows a bell curve where 68.27% of values fall within one standard deviation of the mean value, 95.45% fall within

two standard deviations, and 99.73% fall within three standard deviations. In a random vibration, the magnitude of excitation is approximated by this distribution over a large time interval.

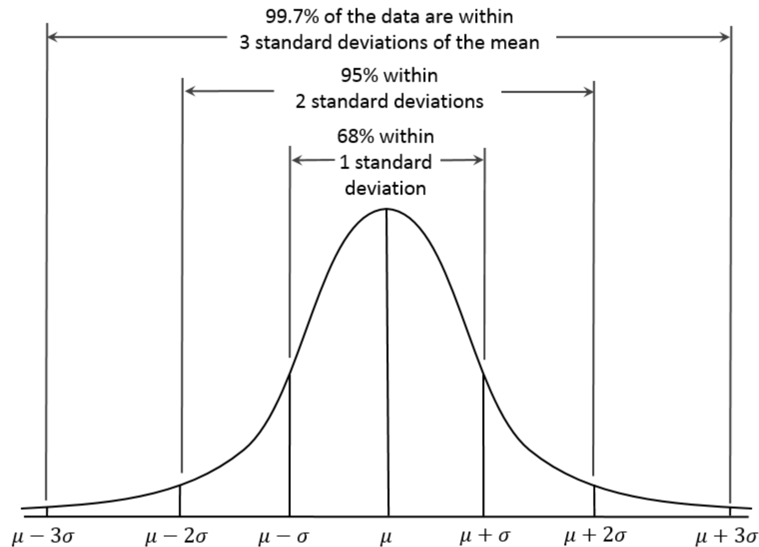


Figure 2-11 PDF of Gaussian Distribution [78]

The PSD of a continuous signal plots the power distribution of the signal over the frequency range. PSD can be quantified differently for different purposes, this includes displacement, velocity, acceleration, and force PSD curves. Typically for random vibration testing, acceleration PSD is used with the unit g^2/Hz. As the PSD is an averaging process, the values are statistical in nature, and there is an infinite amount of possible input time histories [75]. The measurements of a signal, $f(t)$, is transformed into PSD through a fast Fourier transforms (FFT) shown in Equation 1.111

$$PSD = \frac{\left|\tilde{f}(\omega)\right|^2}{\omega Q} \quad (1)$$

Where $\tilde{f}(\omega)$ is the FFT of the signal, ω is the angular frequency, and Q is the dimensionless Q factor that defines the damping of the system. The FFT transfer function is given in Equation 2.

$$\tilde{f}(\omega) = \frac{1}{2\pi}\int_{-\infty}^{\infty} f(t)e^{-i\omega t}dt \tag{2}$$

As shown, the FFT transforms the time domain function with respect to t to a frequency domain function with respect to ω. For a plotted PSD graph, the area under the curve will be the mean square of the measured metric [79].

A typical structural analysis will calculate the input PSD by transforming the random vibration time history and outputting a response PSD (RPSD) that determines how the test sample reacts. RMS stresses and strains are calculated using numerical models or FEA. These results are probabilistic in nature and will vary at each level following Gaussian distribution. To determine the fatigue life of a sample under random vibration, Steinberg's 3-band method with Miner's cumulative damage ratio is most commonly applied [80]. The 3-band method takes into account the stresses from the first level (1σ) to third level (3σ). The number of cycles to failure at each level can be determined based on literature values, such as stress-life (S-N) curves. These cycles are then used in Miner's Rule to calculate the damage ratio as shown in Equation 3.

$$CDI = \sum_{i=1}^{k} \frac{n_i}{N_i} \tag{3}$$

Where *CDI* is the cumulative damage index, n_i is the total number of cycles tested at each stress level from one to three, and N_i is the cycles to failure at each stress level. The damage ratio will indicate the expected percentage of life used or that the sample has failed. It should be noted that both stress- and strain-life methods can be used for the HCF conditions

under random vibration tests. The vibrations levels are on a scale where the stresses in the package do not ordinarily exceed the yield strength of the material.

2.3.3. Microelectronic Packaging Interconnect Testing

Random vibration testing has only begun to see more use in the past decade, and standardized testing and analysis methods have not yet been developed. Zhou et al. performed both harmonic and random vibration on tin-silver-copper (SAC) 305 solder and observed the strain-life (E-N) relationship [81]. Yu et al. predicted HCF failure of lead-free BGAs using rainflow counting methods and Miner's cumulative damage ratio [82]. Che et al. tested SAC solder through dynamic analysis and modelled fatigue through the Coffin-Manson equation [83]. And Liu et al. estimated BGA HCF for random vibrations using the Weibull distribution, Miner's rule, and Basquin's equation [84]. All of these mentioned tests use different input random vibrations. The input PSD bandwidth can be 500, 1000, or 2000 Hz and the maximum acceleration ranges from 0.1 to 120 g^2/Hz. The profile of the PSD also varies in the form of constant acceleration, curves with ramp ups and downs, and stepped curves. Few standards exist for random vibration testing of microelectronic packages and are rarely used in literature. The current most detailed standard is JEDEC's JESD22-B103B, which outlines several test levels and their corresponding PSD profiles shown in Figure 2-12 [85]. However, the given PSD profiles are often difficult to achieve with conventional lab-scale equipment and the magnitude of acceleration can be insufficient. Other standards only provide general guidelines, such as MIL-STD-810G Method 513 [86] and IEC 60068-2-64 [87].

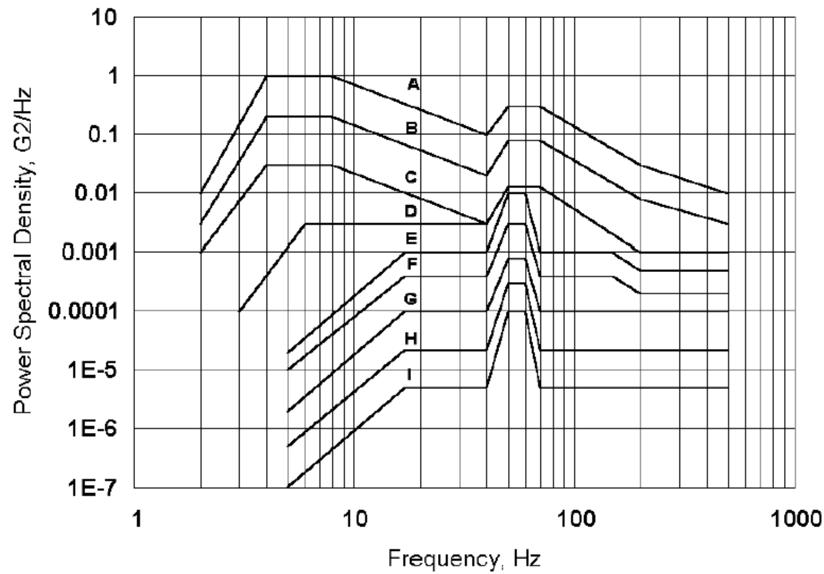


Figure 2-12 JEDEC Random Vibration PSD Test Levels [85]

Overall, random vibration loading is an alternative to sinusoidal loading that offers more realistic simulations of microelectronic packages and interconnects in their applicable environments. It allows for the simultaneous excitation of all modes in a given bandwidth and provides faster FEA calculations through the frequency domain spectrum analysis. However, there is a dire need for more established testing and fatigue prediction methods for random vibration testing of microelectronic packaging interconnects.

2.4. Summary

With the continuous miniaturization of microelectronic packages, traditional solder BGA interconnects have been identified as a key failure location. To increase the mechanical reliability of packages, compliant interconnects are being developed. The latest iteration is a multi-path interconnect with electroplated copper arcuate beams known as the 3-Arc-Fan compliant interconnect. Reliability testing in terms of thermal cycling and drop testing are already well established, but vibration testing methods require further

investigation. Random vibration loads are preferable to sine vibration due to the more accurate simulation of real life events and faster computation time. Thus, the response of 3-Arc-Fan compliant interconnects under random vibration will be examined.

CHAPTER 3

OBJECTIVES AND APPROACH

This section will state the main objectives of this thesis by identifying existing gaps in research and providing the approach to achieving them. A general outline of the thesis is also presented.

3.1. Research Gaps in Existing Literature

Based on the thorough literature review of past work, four overarching gaps in existing research are identified as follows:

1. Besides the complex fabrication process, the main reason compliant interconnects have not seen widespread adoption in industry is due to the increased production cost caused by nonconventional assembly processes. Improved assembly processes are required to conform to industry standards.
2. Compliant interconnects require more reliability testing to prove their viability. Thermal cycling and drop testing have already been performed on the 3-Arc-Fan interconnect, but only simple vibration characterization have been conducted.
3. Random vibration testing is an improvement from sine testing. However, test condition and analysis methods are not well established for microelectronic packaging, especially for Second-Level interconnects.
4. Electroplated copper is a non-ferrous material often used in the fabrication of compliant structures. Yet, fatigue prediction data and damage metrics are not well defined compared to SAC solder and other metals.

3.2. Objectives and Scope of Research

To address the issues listed previously, the primary objectives of this research is as follows:

1. Optimize assembly process of 3-Arc-Fan compliant interconnects for ease-of-assembly and improved bonded structures for higher reliability.
2. Characterize the vibration response of assembled 3-Arc-Fan microelectronic packages through modal and harmonic testing and analysis. In addition, develop models for use in FEA software and validate with experimental results.
3. Establish a random vibration HCF testing methodology for microelectronic packaging interconnects.
4. Develop an S-N fatigue prediction curve for 3-Arc-Fan interconnects undergoing random vibration loads through results obtained in both experiments and simulations.

3.3. Approach and Methodology

Before experimental testing can begin, the 3-Arc-Fan compliant interconnect must first be assembled onto printed circuit boards (PCB) through a flip chip process. The current method produces unreliable results and unsatisfactory structures that cannot be used for testing. Iterative parameter changes in the assembly profile are introduced and the resulting assembly is inspected with a combination of electrical tests, X-ray imaging, and cross sectioning. Particular focus is placed on solder wetting and bond formation during assembly.

Once the microelectronic package is assembled, preliminary vibration testing can be performed. The natural/resonant frequency and mode shape is captured to characterize

the vibration response. FEA models are developed simultaneously using ANSYS® Mechanical™ 17.1. Due to the large amount of interconnects in each package, the model is simplified through compliance calculations and symmetry. By comparing the results from modal and harmonic simulations to the experimental data, the FEA model is validated.

Random vibration fatigue tests are performed at varying intensities and characterized with PSDs. The testing methodology is based off a mixture of prior research and standards most suitable for the scale and behavior of compliant interconnects. Fatigue failure is indicated by an increase in resistance due to arcuate beam fracture.

Finally, the stresses and strains in the compliant interconnects are determined through a PSD spectrum FEA analysis with the same boundary conditions and input loads as the experiment. Based off of the life observed by the interconnects during experimental testing and the stresses calculated from FEA, an S-N relationship for HCF failure prediction is developed for 3-Arc-Fan interconnects under random vibration and, in extension, electroplated copper.

The first 2 chapters of this thesis, thus far, has introduced the concept of compliant interconnects and the various types of mechanical reliability testing methods. This chapter identifies the areas in need of additional research, outlines the objectives designed to satisfy those needs, and plans out the methods to solve them. Chapter 4 covers the assembly optimization of 3-Arc-Fan compliant interconnects. Chapter 5 provides the procedure and results of the various experiments. Chapter 6 discusses the development and validation of the FEA model along with the different analytical methods. Chapter 7 compares the fatigue life results to literature values and demonstrates the increase in reliability due to

compliance, and, additionally, develops a preliminary fatigue life prediction model. Lastly, Chapter 8 concludes the research and gives insight into future work.

CHAPTER 4

ASSEMBLY OPTIMIZATION OF 3-ARC-FAN INTERCONNECTS

As mentioned in the previous chapter, one of the key bottlenecks of compliant interconnect technology is the complexity of the assembly process. In surface mounting, traditional solder BGAs are commonly assembled using a flip chip process, where the solder bonds are formed through reflow. However, the mechanical properties of the 3-Arc-Fan interconnect creates difficulties in solder bond formation; the compliant arms combined with the non-coplanarities on both the substrate and board causes gaps between the solder ball and landing pad. Therefore, a thermo-compression bonding (TCB) process is required to apply a compression force during assembly to ensure planarization and bond formation. For TCB, pressure, temperature, and time are all parameters that need optimization to produce the most reliable bonds for use in testing.

4.1. Prior Interconnect Fabrication

The samples used in this thesis were previously fabricated by Chen [88], who improved upon the earlier positive liquid photoresist fabrication process by Okereke [89]. By switching to a negative dry-film photoresist, Chen simplified the fabrication process and increased the overall yield. In addition, the newer fabrication method is more cost effective as the process can be performed at a class 1000 cleanroom instead of class 100 [17]. Three types of samples with 10, 15, and 20 μm beam widths were fabricated on a 6 inch silicon wafer with a 0.675 mm thickness. One wafer contains a total of 32 18 mm × 18 mm substrates that each carried 2016 3-Arc-Fan compliant interconnects with a 400 μm

pitch in an area array [17]. Figure 4-1 shows the sequential fabrication process for the 3-Arc-Fan compliant interconnects.

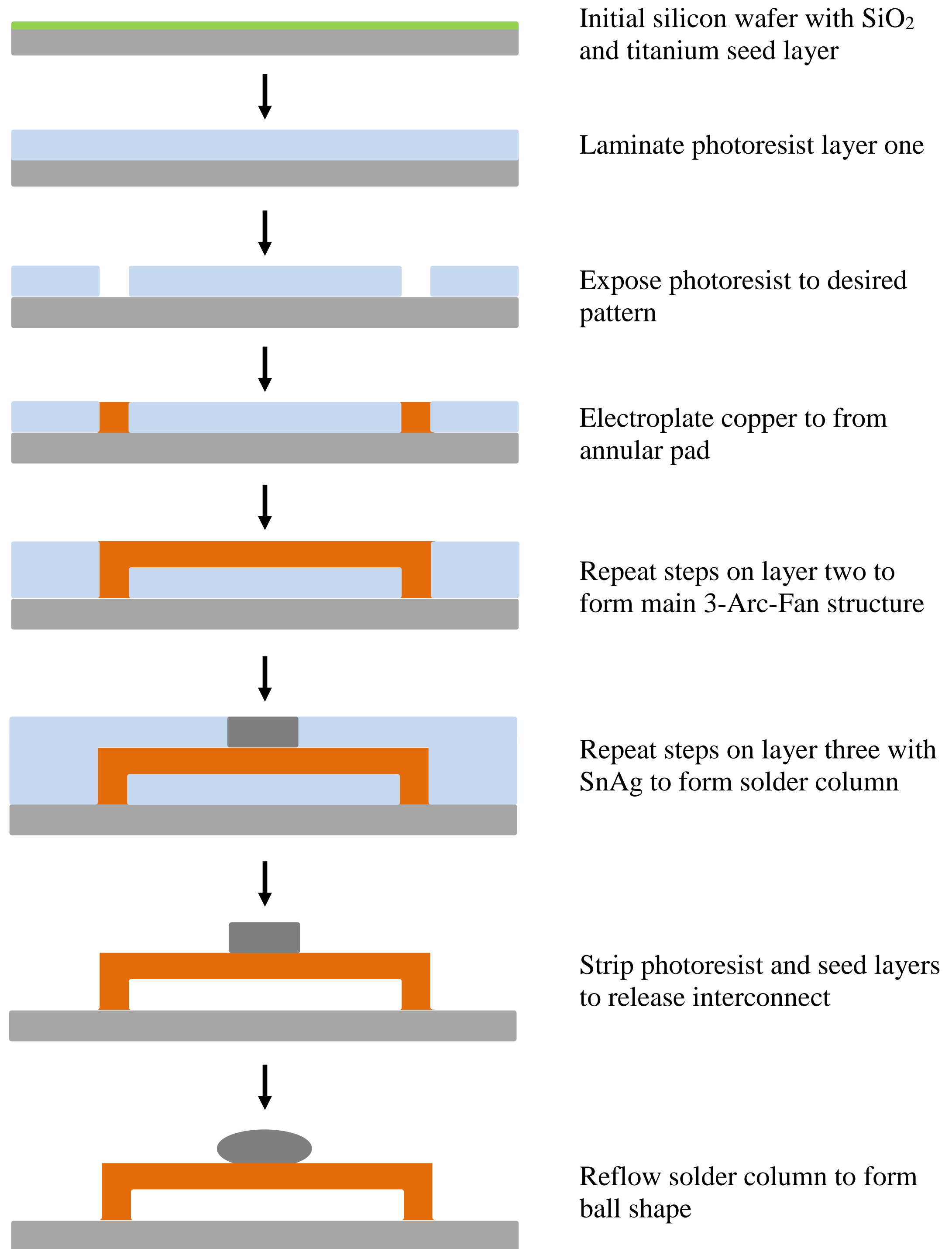


Figure 4-1 Fabrication Process of 3-Arc-Fan Interconnects [17]

The fabrication process begins by insulating a blank silicon wafer with a layer of SiO_2, and sputtering a titanium seed layer for increased adhesion. The next step is to laminate, expose, then develop the first layer of negative dry-film photoresist into the pattern of the annular substrate pads. The photoresist chosen for this purpose is Dupont™ Riston® FX920. With the pattern exposed, the wafer is now ready for electroplating. This is done in Technic™ CU 2800, a copper sulfate plating bath. Once the annular substrate pads are constructed, these steps are repeated for the multi-path arm fabrication. Similarly, the solder layer is electroplated in Technic™'s lead-free eutectic tin-silver solution [88]. The compliant interconnect structure is thus formed with the completion of the solder layer. And the extra material is removed through standard stripping and etching processes, in doing so, the interconnect is released. The last step is to reflow the electroplated solder column to form a solder ball more suitable for assembly purposes. Figure 4-2 presents a completed sample, and Figure 4-3 shows the quarter symmetrical orientation of the interconnects corresponding to each quadrant.

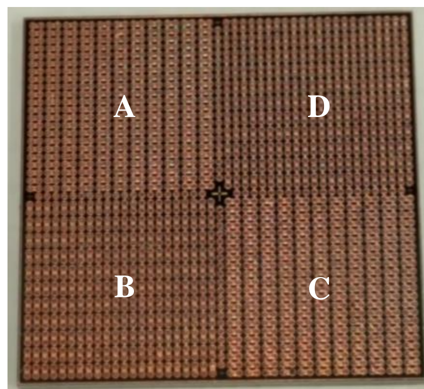


Figure 4-2 18×18 mm Silicon Substrate with 3-Arc-Fan Interconnects with Marked Quadrants

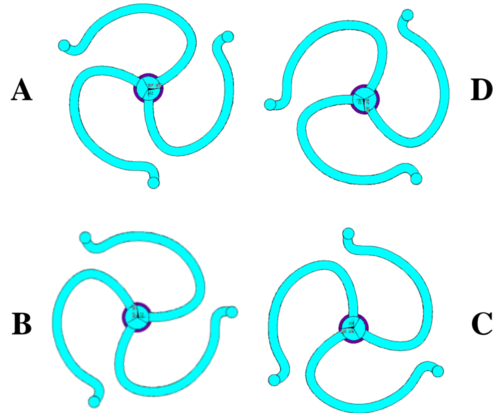


Figure 4-3 Quarter Symmetrical Orientation of Interconnects at Each Quadrant

4.2. Board Design and Selection

A Second-Level interconnect forms connections between the substrate and board. With fabrication completed, the substrate parameters have been decided. Thus, consideration now moves to the board. The organic FR-4 boards used for assembly optimization were ordered from PCB Universe™. Figure 4-4 shows the 132 mm × 77 mm × 1 mm board with drilled pin holes for mounting. The substrate is assembled at the center, where it will form daisy chains with the copper traces. These chains are designed to provide various probing pads for electrical resistance testing, the most important being the 4×4 interconnect chain at each corner where failure is most likely to occur. Figure 4-5 illustrates the daisy chain configuration and indicates the primary testing sites.

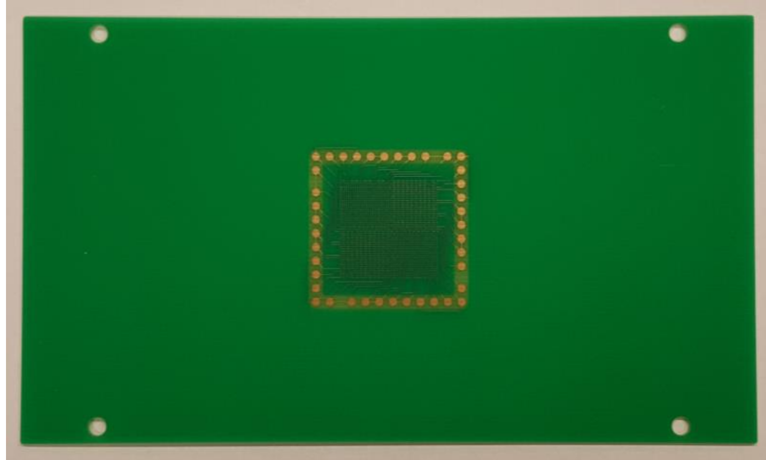


Figure 4-4 FR-4 Board

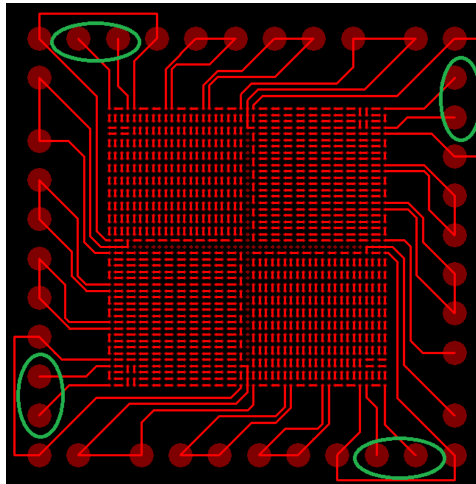


Figure 4-5 Copper Trace Pattern on FR-4 Board with Marked Corner Testing Pads

The main design parameters of the PCB for assembly are the contact pad areas where solder bonds and intermetallics are formed. Two designs are used throughout the assembly optimization process. The first is non-solder mask defined (NSMD), where the solder mask opening (150 μm) is larger than the copper pad (100 μm). This allows for ease of alignment during flip chip assembly and higher contact accuracy. The second design is solder mask defined (SMD) and features a smaller mask opening (116 μm) than the copper

pad (145 µm). SMD designs generally improve mechanical reliability and prevents solder runoff, but increases assembly difficulty. Figure 4-6 compares schematic diagrams of the two types of pad definitions. The first design is built at IPC Class II standards, while the second is at Class III. Both designs have surface finishes of electroless nickel electroless palladium immersion gold (ENEPIG) to prevent oxidation.

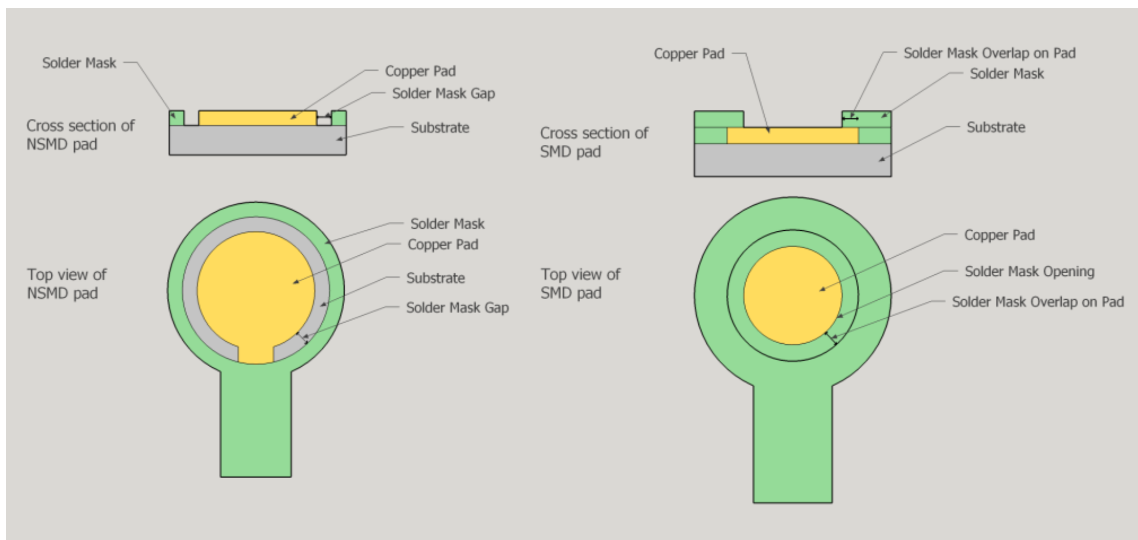


Figure 4-6 NSMD (Left) vs. SMD (Right) [90]

4.3. Assembly Process

An overview of the assembly process will be outlined in this section, which consists of pre-assembly preparations, equipment setup, TCB profile parameterization, and post-assembly inspection.

4.3.1. Assembly Preparations

Before the actual assembly process can begin, the samples are first cleaned and inspected. The silicon substrates with the compliant interconnects are placed in an acetone bath inside a mini ultrasonic cleaner for 12 minutes. The PCBs are scrubbed with acetone

and isopropyl alcohol (IPA) and baked at 110 °C for 30 minutes on a hot plate. Both components are then rinsed with acetone and IPA and dried using a nitrogen gun immediately prior to assembly.

To check for defects from fabrication and handling, the interconnect samples are examined under optical microscope and X-ray. Though the dry-film photoresist layers were stripped during the fabrication process, the microscope images show that some residue are still trapped by the arms. In addition, the combination of photoresist release and ultrasonic cleaning causes some interconnects to detach or bend as indicated in Figure 4-7. These defects are noted prior to assembly. X-ray imaging is also used to confirm that no voiding exists in the solder balls before the bonding process as supported by Figure 4-8.

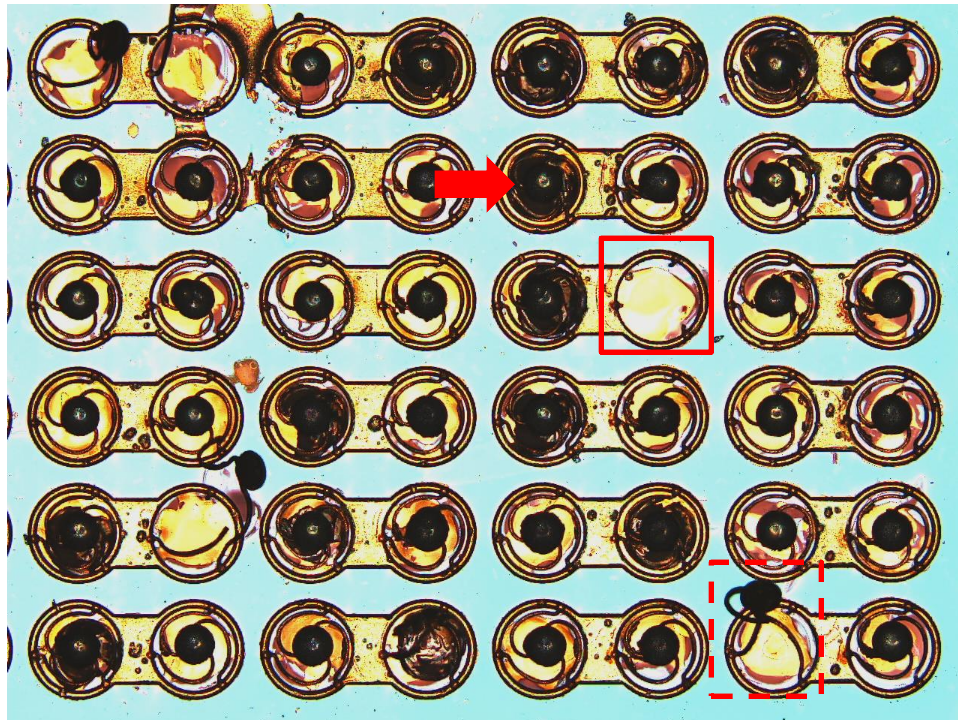


Figure 4-7 Microscope Image Showing Pre-assembly Defects. Including photoresist residue (Arrow), detached interconnect (Box), and bent interconnect (Dash Box).

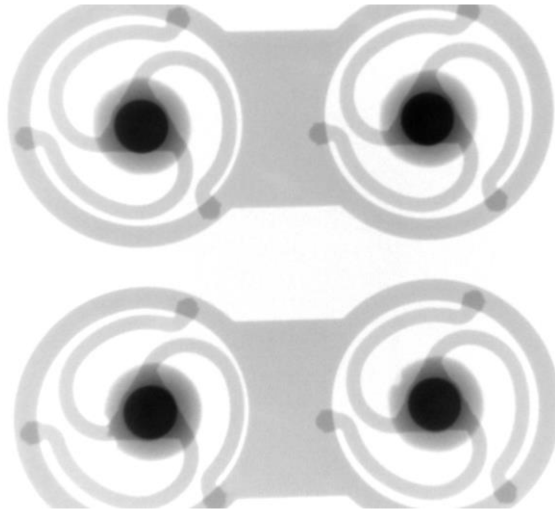


Figure 4-8 X-ray Image of Pre-assembly Interconnects. Uniform dark circles in the center of each interconnect confirms no voiding.

4.3.2. Flip Chip Bonder Setup and Flux Selection

The assemblies are performed with the Finetech™ FINEPLACER® matrix flip chip bonder shown in Figure 4-9, which offers increased accuracy and precision from the Finetech™ FINEPLACER® lambda used for previous assemblies. Alignment between the substrate and board is achieved using the built-in optics and program. In addition, the quarter symmetry design of both the substrate and board allows for any 90° rotation. A 10 mm × 10 mm tool head is selected to pick and place the 18 mm × 18 mm silicon substrate, and 0.25 mm spacers were selected for the appropriate height during bonding, which was later switched to 0.30 mm due to polishing of the tool head. Following the flip chip bonder initialization, flux is applied on the contact surfaces of both the substrate and board to prevent oxidation at high temperatures during bonding. The flux chosen for this assembly is ALPHA® NR-200, a liquid no-clean flux. A water soluble paste flux, INDIUM® WS-446, was also tested in an attempt to improve solder voiding issues, but did not have any significant effect.

Figure 4-9 Finetech™ FINEPLACER® matrix [91]

4.3.3. Initial Assembly Profile and Parameters

The initial TCB assembly profile was outlined by Chen based on an altered JEDEC J-STD-020D standard [17]. Assembly is performed through a TCB flip chip process where heat is applied to both the substrate and board, and pressure is applied from the top of the substrate. The temperature profile is plotted in Figure 4-10 with a preheat temperature of 180 °C for 30 s and a peak reflow temperature of 270 °C for 50 s. The preheat temperature activates the flux, while the reflow temperature wets the solder and allows it to form connections with the copper pads on the board.

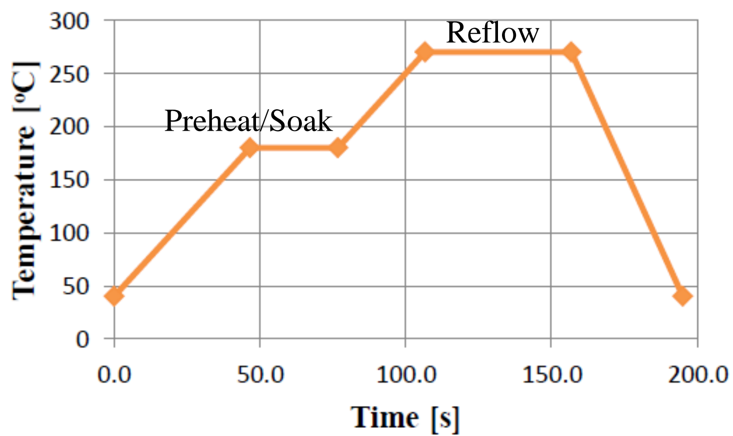


Figure 4-10 Initial TCB Temperature Profile [17]

Determining the amount of pressure to apply to the substrate is another major parameter for TCB assemblies. As briefly mentioned earlier, the compliance of the arms and warpage of the PCB at room temperature creates non-coplanarities between the two components. Additionally, the electroplated interconnects have a standoff height variance of 10% [17]. Therefore, it is difficult to achieve uniform bonding through pure reflow without any compressive force application. For 3-Arc-Fan interconnects, each beam width has its own compliance value that the compressive force is derived from. Equation 4 provides the calculation used to obtain the compressive force values.

$$F = \frac{d_{desired}}{C} \times N \tag{4}$$

Where F is the total compressive force applied to the silicon substrate, $d_{desired}$ is the desired compressed distance, C is the compliance of the interconnect, and N is the total number of interconnects on one silicon substrate sample. For a standoff discrepancy of 10% and board warpage at room temperatures, the desired distance is 3 μm according to Chen [17]. Given this value, the compressive force is calculated for each beam width based on their measured compliance listed in Table 4-1.

Table 4-1 Measured Compliance and Calculated Total Compressive Force for Each Beam Width Sample [17]

Beam Width (μm)	Compliance (mm/N)	Compressive Force (N)
10	5.52	1.1
15	2.97	2.0
20	2.31	2.6

This compressive force is identified as one of the primary variables during assembly as the shape of the solder bump is extremely sensitive to force application. Excessive force will squish the solder and cause leakage and runoff that can potentially bond to the arcuate beams of the 3-Arc-Fan structure, while insufficient force may lead to unbonded solder balls. The angle of force application is another important factor during assembly; it must remain perfectly perpendicular to the substrate and board to avoid any tilt in the sample where only one side of the substrate and interconnect makes contact with the board side pads.

4.3.4. Assembly Inspection

After assembly is completed, the quality of the assembled samples need to be inspected. Non-destructive methods via electrical daisy chain testing and X-ray examinations are performed first. The resistance of each critical corner daisy chain containing the 4×4 interconnects shown in Figure 4-11 are checked through a digital multimeter. An uncharacteristically large resistance or open circuit indicates bond formation issues. Intermediate daisy chains can also be tested for more insight into the overall bonding process during assembly. X-ray images are captured by the Nordson DAGE XD7600NT™ Diamond X-ray Inspection System. These images can easily identify solder bump defects such as void formation, runoff, and deformation.

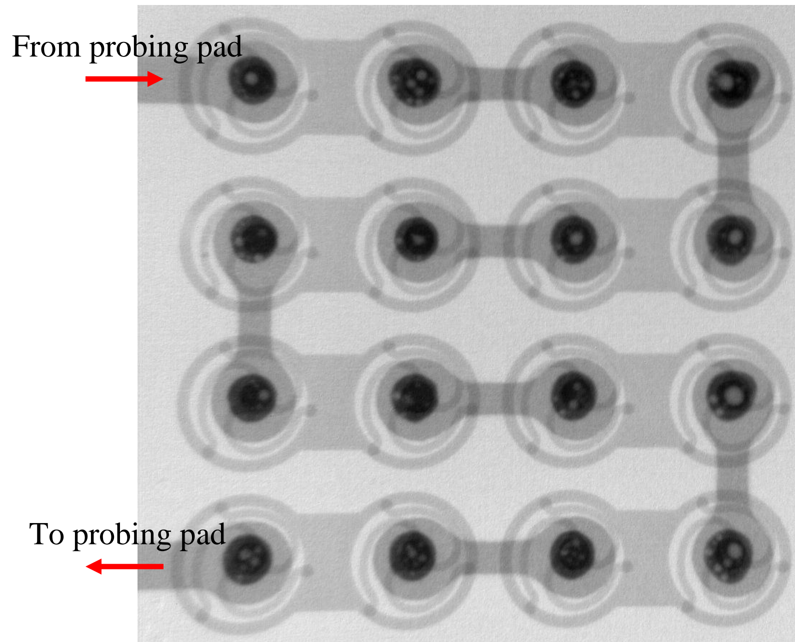


Figure 4-11 Corner Daisy Chain Configuration

Cross-sectioning is destructive method that renders the sample unusable. The sample is rinsed with acetone and IPA to remove any flux residue, and underfilled with organic polymer to protect the interconnect structures during the process. The underfill selected for this purpose is NAMICS® U8410-219. The sample is then placed in an acrylic plastic mold and polished through increasingly fine sandpaper to the desired level to expose the solder bumps. The resulting cross-section of the solder bumps is observed under microscopes and measured under optical profilers to inspect the bonded areas, solder bump shape, and overall tilt of the sample. A typical cross-section image for 3-Arc-Fan interconnects is shown in Figure 4-12 with labeled components. A schematic of the cross section viewing angle is demonstrated in Figure 4-13.

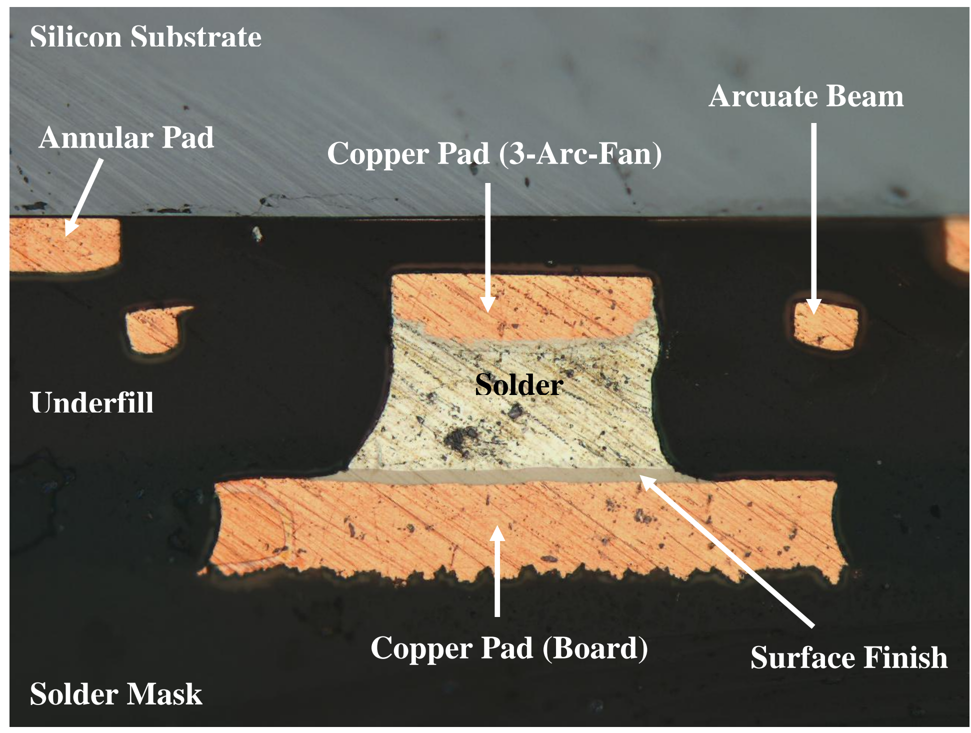


Figure 4-12 Labeled SMD Cross-Section Image

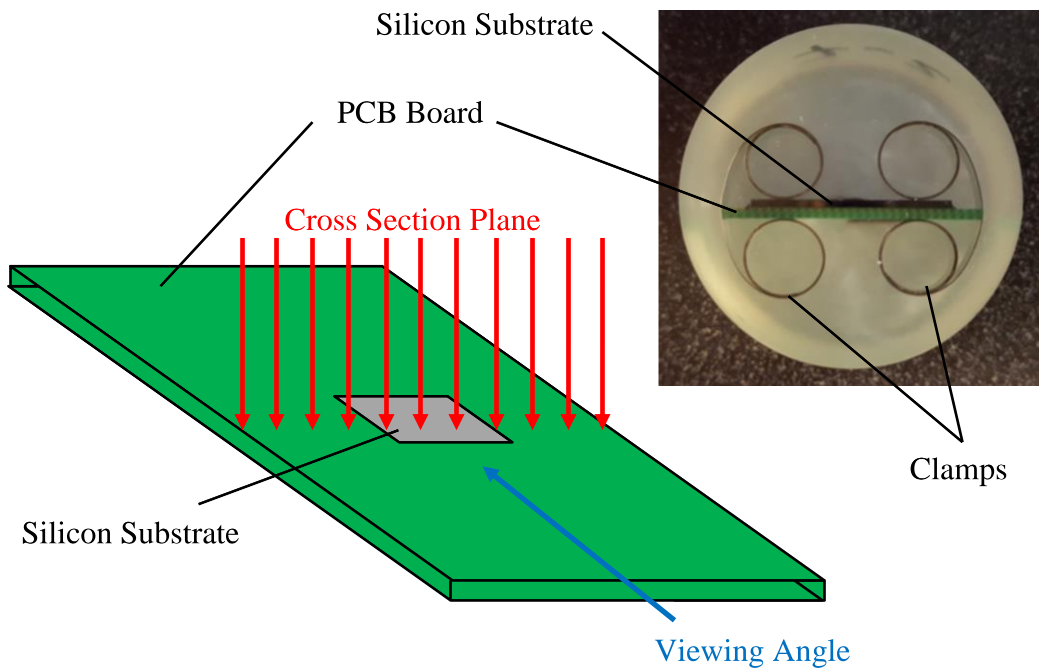


Figure 4-13 Cross Section Plane Schematic (Left) and Molded Sample (Right)

4.4. Optimization Trials

A total of nine trials were completed over the course of the optimization process. Each trial adjusted parameters, redesigned components, or altered pre-assembly steps in an attempt to produce the most reliable solder bonds for use in testing. The available samples were prefabricated and limited in number, becoming a major consideration for the optimization process. After inspection of the initial sample pool, only twelve 20 µm, seven 15 µm, and three 10 µm samples qualified for assembly and future testing.

4.4.1. Optimization Overview

An overview of the setup, profile, and parameters for each assembly trial is listed in Table 4-2. The assembly parameters are defined by board selection (NSMD vs. SMD), the type of flux applied (liquid vs. paste), and the assembly process (TCB vs. reflow). The preheat parameters refer to the soak temperature, duration, and force applied during the flux activation process, which differs depending on the type of flux applied. The reflow parameters refer to the peak reflow period and is the most critical to bond formation. Changes from one trial to the next are marked in red. It should be noted that the samples in trial three were taken from the inspected samples that did not qualify for testing, but could be used for assembly optimization. Trials seven to nine also include reworks if necessary to connect the unbonded solder balls after initial assembly.

Table 4-2 Assembly Optimization Profile Parameters

<table>
<tr><th>Trial</th><th>Samples</th><th>Assembly Parameters</th><th>Preheat Parameters</th><th colspan="2">Reflow Parameters</th><th>Comments</th></tr>
<tr><td>1</td><td>20 µm</td><td>NSMD
Liquid
TCB</td><td>110 °C
60 s
2.6 N</td><td colspan="2">260 °C
60 s
2.6 N</td><td>Prevalent solder runoff and voiding</td></tr>
<tr><td rowspan="2">2</td><td rowspan="2">20 µm</td><td rowspan="2">NSMD
Liquid
TCB</td><td rowspan="2">110 °C
60 s
2.6 N</td><td colspan="2">250 °C
15 s
2.6 N</td><td>Decreased reflow duration to contain runoff</td></tr>
<tr><td colspan="2">240 °C
5 s
2.6 N</td><td>Further decreased reflow duration; runoff still present</td></tr>
<tr><td>3</td><td>20 µm</td><td>NSMD
Liquid
TCB</td><td>110 °C
60 s
2.6 N</td><td colspan="2">240 °C
7 s
1.0 N</td><td>Reduced reflow force to contain runoff; runoff still present</td></tr>
<tr><td rowspan="2">4</td><td rowspan="2">20 µm</td><td rowspan="2">SMD
Liquid
TCB</td><td rowspan="2">110 °C
60 s
2.6 N</td><td colspan="2">240 °C
10 s
2.6 N</td><td>Control sample for new SMD board</td></tr>
<tr><td colspan="2">240 °C
15 s
1.5 N</td><td>Reduced reflow force to control leakage</td></tr>
<tr><td>5</td><td>20 µm</td><td>SMD
Liquid
TCB</td><td>110 °C
60 s
2.6 N</td><td colspan="2">240 °C
15 s
0.2 N</td><td>Further reduced reflow force to control leakage</td></tr>
<tr><td rowspan="2">6</td><td rowspan="2">15 µm</td><td>SMD
Paste
TCB</td><td>160 °C
30 s
2.0 N</td><td colspan="2">240 °C
15 s
2.0 N</td><td>Trial with different flux for voiding issue</td></tr>
<tr><td>SMD
Paste
Reflow</td><td>160 °C
30 s
0 N</td><td colspan="2">240 °C
15 s
0 N</td><td>Pure reflow trial with no compression force</td></tr>
<tr><td rowspan="2">7</td><td rowspan="2">15 µm</td><td>SMD
Paste
TCB</td><td>160 °C
30 s
2.0 N</td><td colspan="2">240 °C
15 s
0.2 N</td><td>Control sample for reflow comparison</td></tr>
<tr><td>SMD
Paste
Reflow</td><td>160 °C
30 s
0 N</td><td>250 °C
30 s
0 N</td><td>Rework
+ 45 s</td><td>Best solder bump shape out of all trials</td></tr>
<tr><td>8</td><td rowspan="2">10 µm × 3
15 µm × 3
20 µm × 4</td><td>SMD
Paste
Reflow</td><td>160 °C
10 s
0 N</td><td>250 °C
60 s
0 N</td><td>Rework
+ 60 s</td><td>Lift off issue during reflow; reworked to form bonds</td></tr>
<tr><td>9</td><td>SMD
Liquid
TCB</td><td>110 °C
60 s
1.1/2.0/2.6 N</td><td>250 °C
30 s
0.2 N</td><td>Rework
+ 30 s</td><td>TCB process for consistent bonding; assembled test samples</td></tr>
</table>

4.4.2. Trial One

The first TCB assembly trial was performed on a 20 µm beam width sample using the initial assembly profile previously outlined. For 20 µm samples, a compressive force of 2.6 N was applied throughout. Only the soak temperature was adjusted to 110 °C for 60 s to match flux activation as shown in Figure 4-14. The resulting X-ray and cross-section images are presented in Figure 4-15 and Figure 4-16.

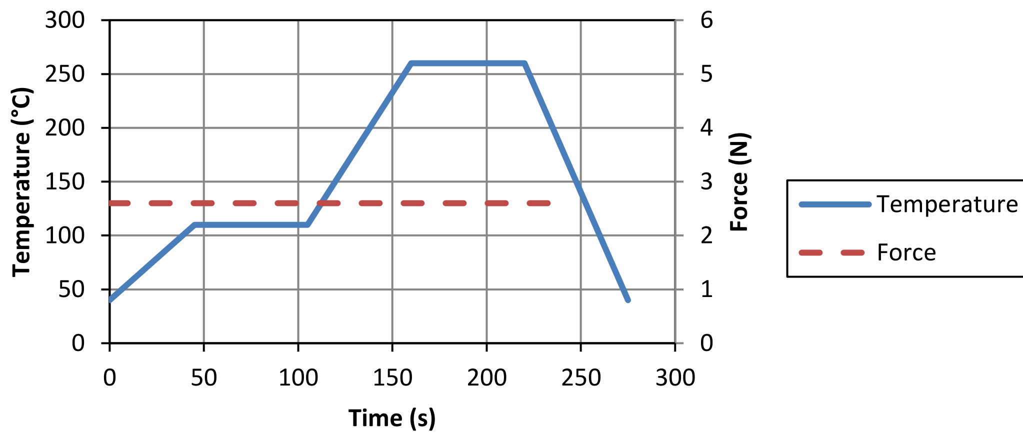


Figure 4-14 Assembly Profile of First Optimization Trial

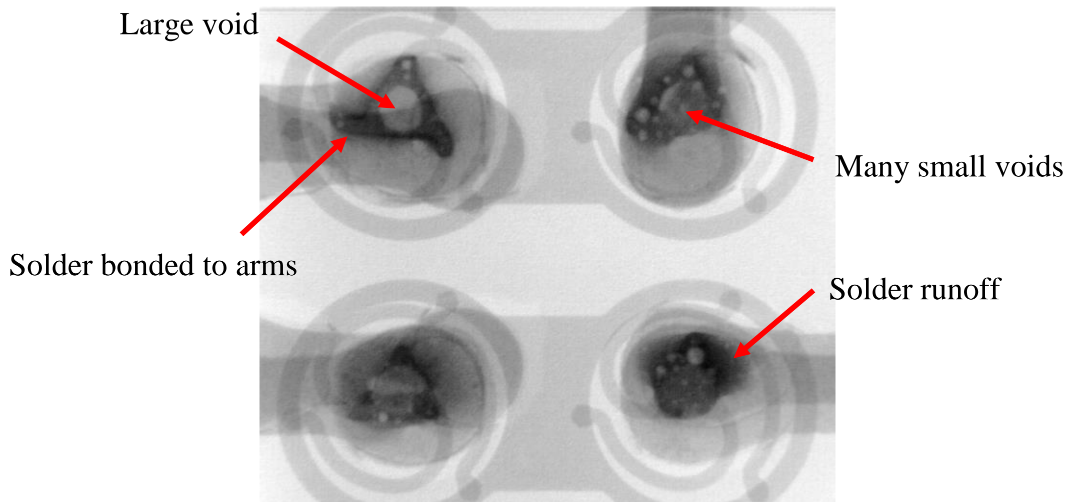


Figure 4-15 Trial One X-ray Image of Corner Interconnects

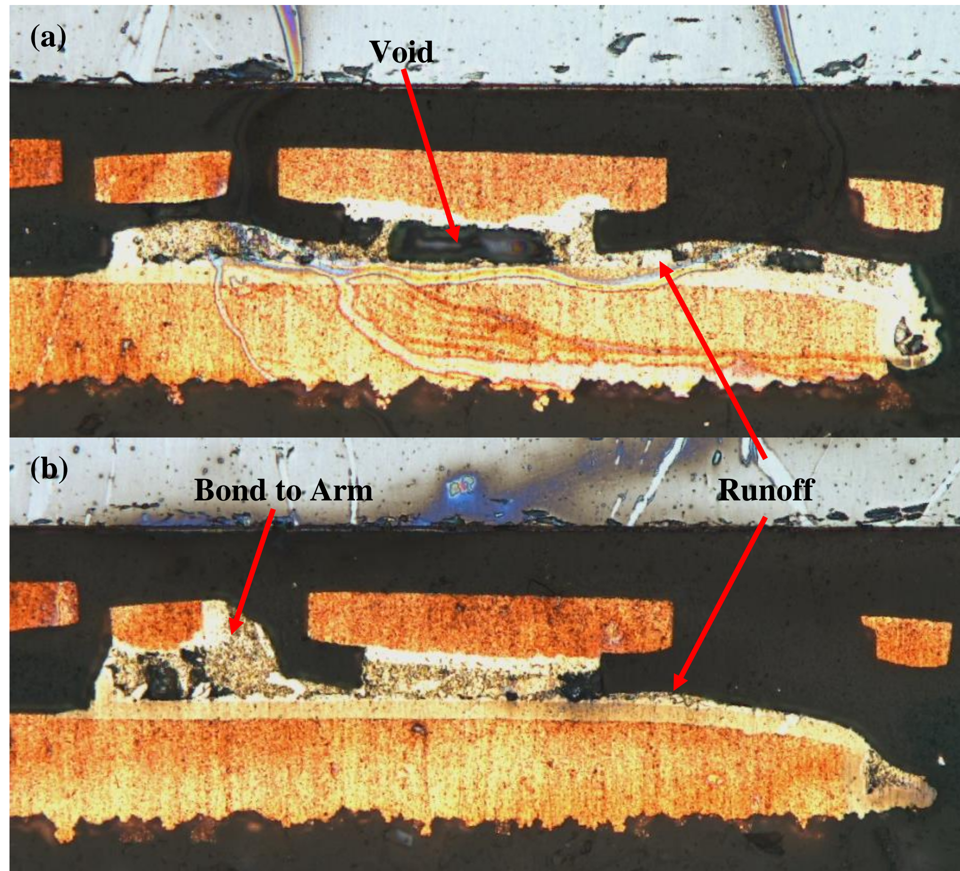


Figure 4-16 Trial One NSMD Cross-Section Images. (a) Voiding and runoff. (b) Bond to Arm and Runoff

The inspection images show that many defects are present on the sample, causing it to be unsuitable for reliability testing. Both singular large voids and multiple small voids exist in the BGA. The wetted solder is seen running off to the sides of the copper pad and, in some cases, bonds to the arcuate beams. This issue is critical as it will affect the compliance of the 3-Arc-Fan interconnect and produce inaccurate testing results. Therefore, the assembly profile must be altered to reliably provide satisfactory solder bump formation.

4.4.3. Trial Two and Three

As the first assembly optimization trial demonstrated excessive solder runoff, the peak reflow temperature and time were reduced for the second trial in an attempt to contain the solder by decreasing the duration of the solder paste in its liquid state. The amount of applied flux was also reduced to decrease flux degassing at higher temperatures that leads to voiding. However, changes in only the temperature profile proved insufficient to effectively contain the solder, and further changes were made to the force profile by reducing the amount from 2.6 N to 1.0 N during peak reflow for trial three. Figure 4-17 displays the cross-section image of a sample assembled during trial three. It is evident that solder runoff has been significantly reduced but not completely eliminated. Therefore, different adjustments need to be made besides the TCB profile.

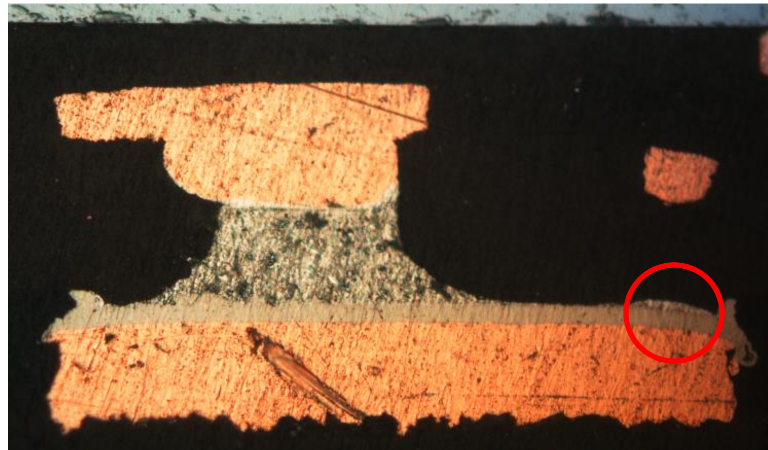


Figure 4-17 Trial Three Cross-Section Image

4.4.4. Board Redesign

The first iteration of the FR-4 PCB was an IPC Class II NSMD design with a 150 µm solder mask opening diameter and a 100 µm copper pad diameter. However, the actual

boards featured much larger dimensions shown in Figure 4-18 due to the looser tolerances of a Class II build. In addition, the shape of the solder mask openings are rectangular instead of circular. These flaws allowed the wetted solder, which has an average diameter of 130 µm, to flow unrestricted on the copper pads and cause runoff during the assembly. This initial NSMD design was chosen to compensate for the alignment difficulty of compliant interconnects and ensure that all solder balls in the BGA make contact with the copper pads on the board. With the integration of the Finetech™ FINEPLACER® matrix in the optimized assembly process, alignment issues have been completely eliminated, and allows the PCB to be redesigned to provide more reliable solder bonds.

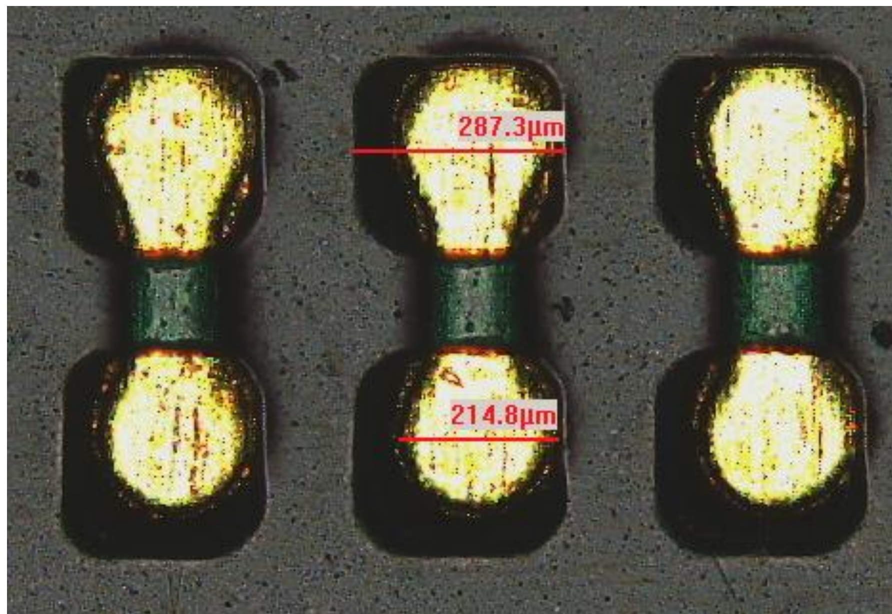


Figure 4-18 Actual Dimensions of Initial Board Design

The redesigned PCB features an IPC Class III SMD design with a solder mask opening diameter of 116 µm and a copper pad diameter of 145 µm. These dimensions are based on standard assembly recommendations where the contact surface of the copper pad

should be 10% smaller than the solder ball diameter, which has an average diameter of 128 µm in this case. A Class III build tightens the tolerance and quality of the board, making it more suitable for reliability testing. While the SMD design effectively restricts the solder runoff as demonstrated in Figure 4-19. The actual board shows good adherence to design specifications, evident in Figure 4-20, and are used for the remaining optimization trials.

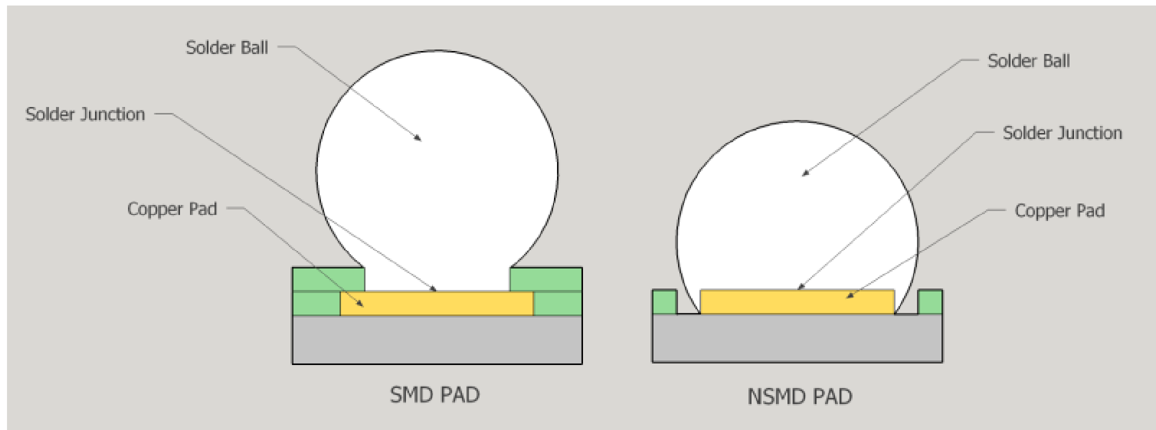


Figure 4-19 Solder Bonding in SMD vs. NSMD [90]

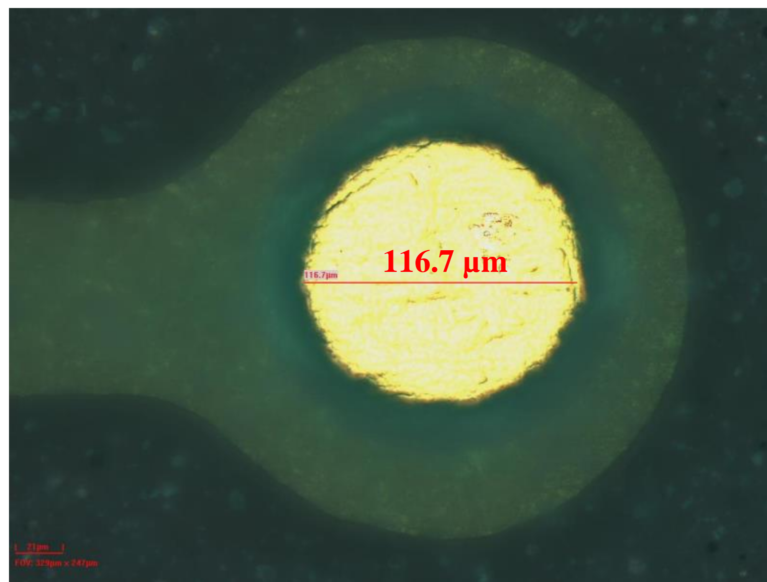


Figure 4-20 New SMD Board Design

4.4.5. Trial Four and Five

Two samples were assembled during optimization trial four. One sample utilized the original proposed assembly profile, while the other utilized the newly adjusted assembly profile with decreased force to compare the effects of the SMD board. The X-ray image seen in Figure 4-21 proves that the compression force is still excessive, causing solder to leak out from the mask opening. Therefore, it was reduced significantly to only 0.2 N during reflow. Essentially, the force is applied to keep the substrate in place and prevent lift off from flux degassing. A cross-section image of trial five shown in Figure 4-22 displays a much improved solder bump shape. However, the bump remains slightly squished and can be further optimized.

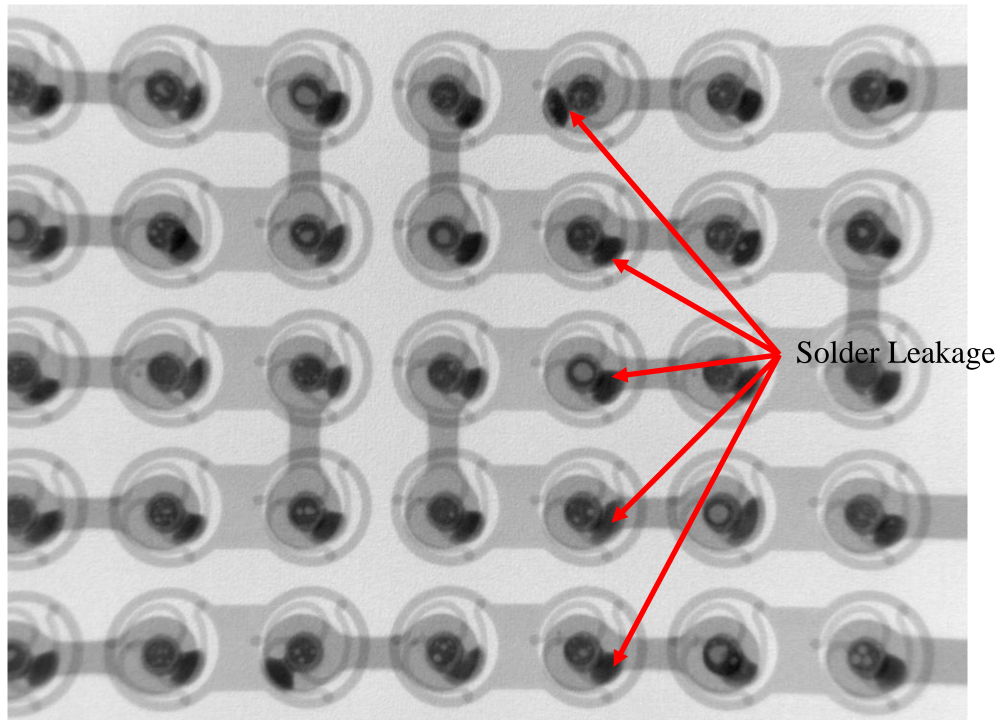


Figure 4-21 Trial Four X-ray Image with Solder Leakage

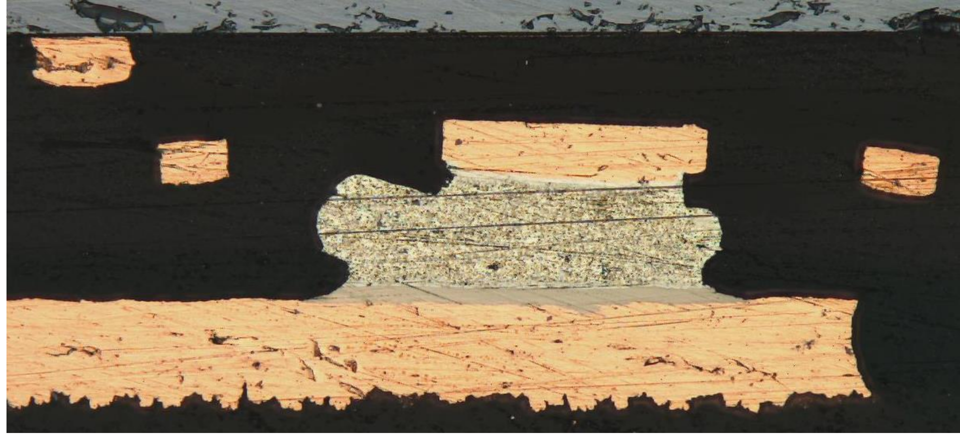


Figure 4-22 Trial Five Cross-Section Image of Slightly Squished Interconnect

4.4.6. Trial Six and Seven

Assembly trials six and seven investigated a pure reflow bonding process where no force is applied during bond formation as opposed to the previous trials that utilized a TCB process. The only compressive force applied in these trials are before the assembly process with moderate heat to planarize the solder balls and ensure contact. In addition, as only plate heat is applied during reflow, the peak temperature duration is extended to fully wet the solder. Trial seven by far produced the best solder bump shape as seen in Figure 4-23. However, it is also discovered that without a compressive force, some solder balls initialize contact with the pad, but is later lifted off due to the pressure build up in the gap between the substrate and board from degassing. Figure 4-24 shows that the solder ball deformed at the bottom from contact with the copper pad, but did not form a bond at the end of reflow. This generates an overall tilt in the sample where one side is bonded and the other is not.

Figure 4-23 Trial Seven Cross-Section Image

Figure 4-24 Reflow Assembly Issue. The flat surface underneath the solder ball indicates prior contact, which was later severed due to substrate lift off.

4.4.7. Trial Eight and Nine

The last two trials assembled the remaining samples for reliability testing. Trial eight followed the reflow process where no force was applied, and trial nine reworked the samples with unbonded interconnects with the adjusted TCB profile. Only non-destructive inspection methods were used since the samples needed to be intact for testing. X-ray imagining in Figure 4-25 shows that voiding is still a prevalent issue due to the intense degassing observed during assembly. Initially, the degassing was assumed to result from excessive flux, but the source was later identified as the organic material of the FR-4 PCBs that begin burning at 210 °C. Figure 4-26 supports this observation by comparing the discoloration of the boards after several cycles of the TCB temperature profile; the area where plate heat is applied is noticeably darker in color. This degassing issue can be alleviated by baking the PCBs at higher temperatures of 150 °C for 1 hour, but will not be completely eradicated.

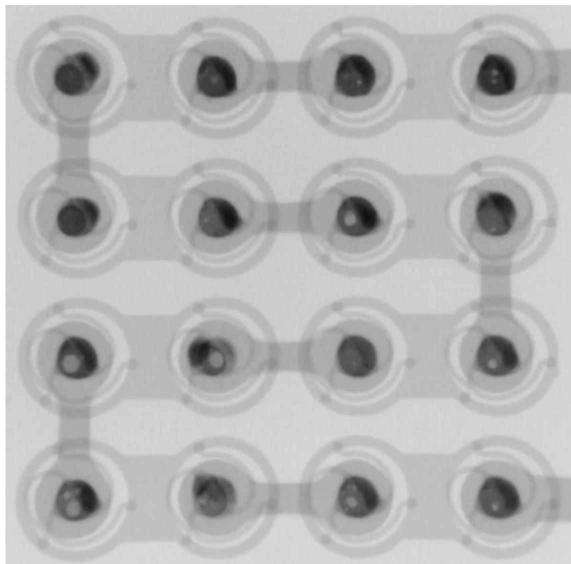


Figure 4-25 X-ray Image of Final Assembled Interconnects for Testing

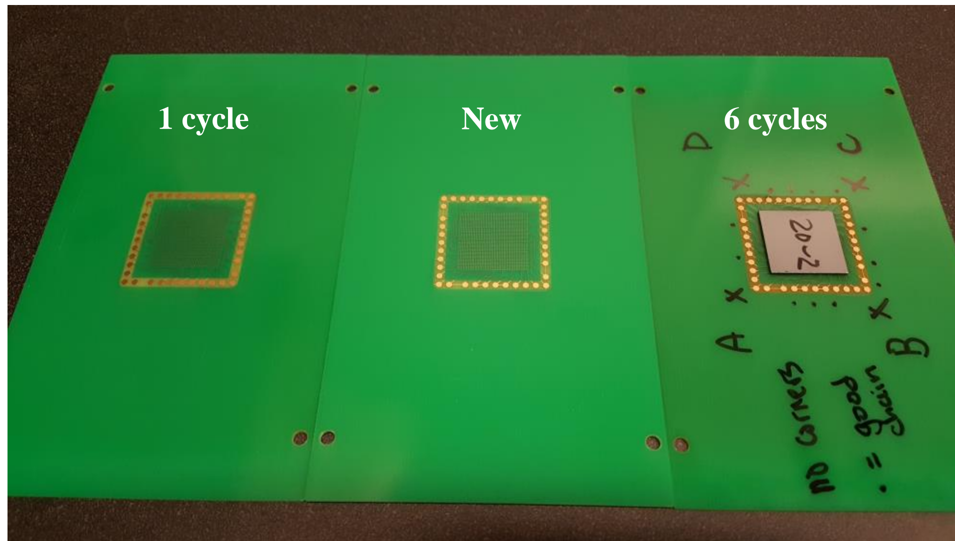


Figure 4-26 Board Discoloration after TCB Rework

4.5. Final Assembly Profile and Reflow Viability

The final recommended assembly profile to ensure solder bond formation across the entire BGA for 3-Arc-Fan compliant interconnects is outlined in Figure 4-27. The preheat temperature and time are based on the selected flux, ALPHA® NR-200, and the planarization force is based on the calculated compressive force for each beam width sample. The peak reflow temperature is placed at 250 °C for 30 s to fully wet all solders, and the force during this period is decreased to 0.2 N to avoid solder bump leakage and prevent substrate lift off or tilt.

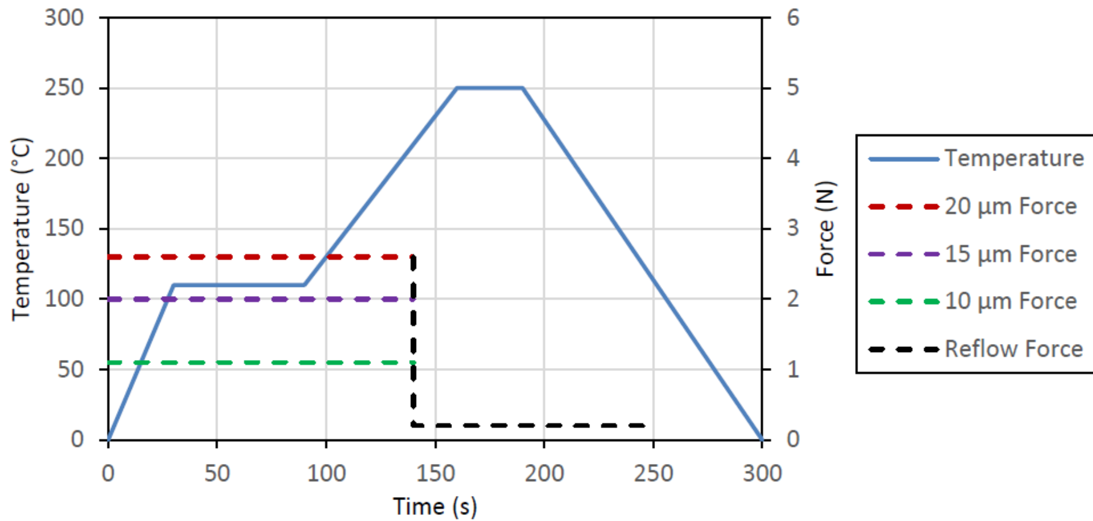


Figure 4-27 Final TCB Assembly Profile

However, TCB processes are uncommon in industry due to the increases in cost. Generally, a standard reflow process without compressive force is preferred. The assembly optimization results show that pure reflow is definitely achievable for 3-Arc-Fan interconnects and actually provides the best solder bump shapes for reliability testing. The only disadvantage of reflow, in this case, is the substrate lift off caused by board degassing. This issue can be easily resolved for future assemblies by decreasing the substrate area, allowing more gas to escape, and purchasing PCBs fabricated with different or higher quality material that exhibit less degassing at operating temperatures for assembly, which will also significantly decrease void formation. Therefore, future assemblies should follow the reflow parameters outlined in assembly trial eight.

CHAPTER 5

EXPERIMENTAL VIBRATION TESTING OF ASSEMBLED 3-ARC-FAN INTERCONNECTS

A total of ten 3-Arc-Fan compliant interconnects are assembled with the optimized assembly process outlined in the previous chapter. There are four 20 µm beam width samples, and three samples each for 15 and 10 µm beam widths. Two main types of testing are performed, vibration characterization and random vibration fatigue.

5.1. Test Sample Electrical Measurements and X-ray Inspection

During fatigue testing, the electrical resistance of the corner daisy chains will be monitored to indicate any failures. Their initial values are recorded in Table 5-1. Cells marked by an “X” indicate overloaded chains. These chains correspond to the fabrication defects that were documented during pre-assembly inspection and are not a result of the assembly process. The samples are also inspected using X-ray to note any assembly defects, such as voiding, prior to testing.

5.2. Experimental Vibration Characterization

Two types of experiments are performed to characterize the vibration response of 3-Arc-Fan compliant interconnect samples. The natural frequencies are measured through sine sweeps, and the mode shape is captured through a constant sine wave input. This data provides a better understanding of the package under vibration loads for fatigue analysis.

Table 5-1 Initial Corner Daisy Chain Resistance

Beam Width (µm)	Sample	Corner Resistance (Ω)			
		A	B	C	D
20	1	X	X	0.461	X
	2	X	X	X	X
	3	0.373	0.381	0.380	X
	4	0.400	X	0.387	0.375
15	1	0.475	0.458	X	X
	2	0.507	X	0.425	0.424
	3	0.470	0.398	X	0.509
10	1	X	X	X	X
	2	0.477	X	0.502	X
	3	X	X	X	X

5.2.1. Experiment Setup

A schematic of the setup for natural frequency measurements is shown in Figure 5-1. The shaker used for vibration input is the Brüel & Kjær® Type 4810 mini shaker, which has a force rating of 10 N, a frequency range up to 18 kHz, and bare table acceleration of 550 m/s^2 [92]. A Hewlett-Packard® 33120A function generator produces the sine sweep signal that feeds into the Brüel & Kjær® Type 2718 power amplifier, which drives the shaker to excite the sample in the out-of-plane direction. A Polytec® PDV-100 laser doppler vibrometer (LDV) is redirected to the center of the silicon substrate to measure the output velocity as seen in Figure 5-2, and a Tektronix® TDS3032B digital oscilloscope records both the generated signal and velocity response. The sample is rigidly fixed onto a mount via four standoff screws according to JEDEC JESD22-B103B standards [85]. The mount is machined from Aluminum 6061 alloy with the dimensions illustrated

in Figure 5-3 and attached to the shaker at the center pin hole. All experiments are performed on optical tables that damp and isolate vibration for higher accuracy measurements.

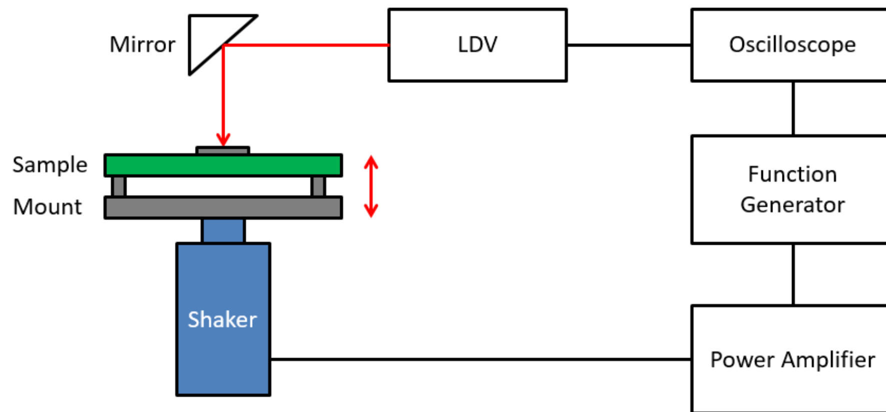


Figure 5-1 Experiment Schematic for Natural Frequency Measurements

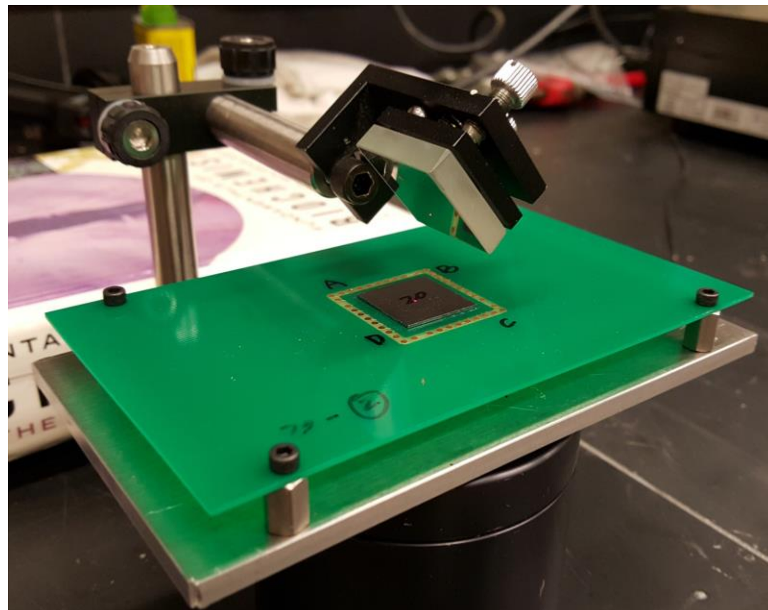


Figure 5-2 Natural Frequency Measurement Point

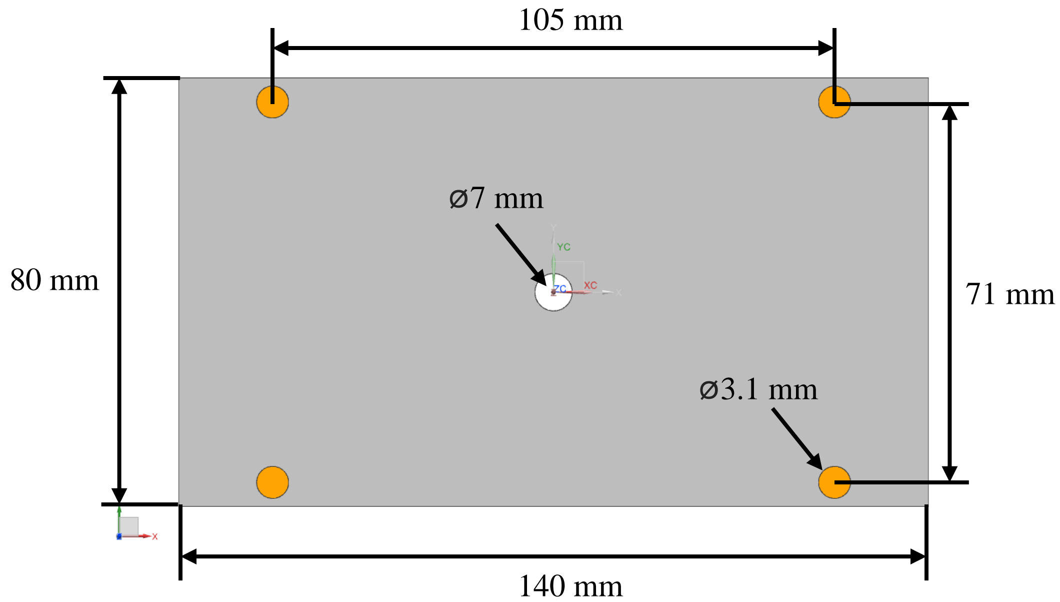


Figure 5-3 Sample Mount Dimensions (Thickness: 1 mm)

5.2.2. Natural Frequency Measurements and Results

The natural or resonant frequency measurements are obtained by generating the sine sweep signal from 1 to 1000 Hz seen in Figure 5-4 and recording the response with the LDV at the center of the substrate. At a setting of 100, the measured LDV voltage is converted to velocity with the conversion 1 V = 25 mm/s. The measurement point is taken at the substrate to include the effect of the compliant interconnects; measurements taken on other areas of the board will produce slightly different results. Two second samples are recorded with a sampling rate of 5000 Hz, allowing for frequency measurements of up to 2500 Hz as stated by the Nyquist theorem.

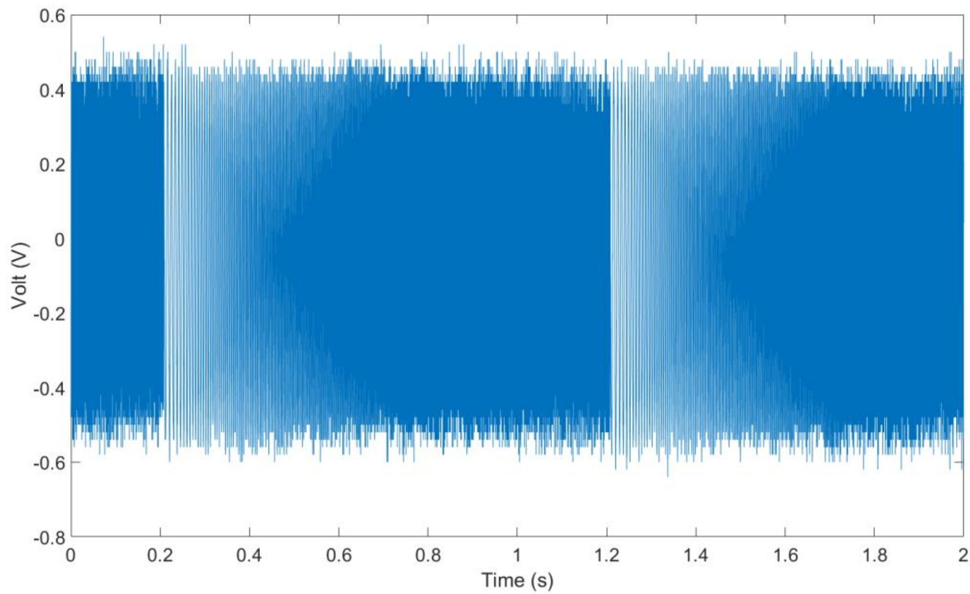


Figure 5-4 Two Second Sample of Sine Sweep Input for Natural Frequency Measurements

A total of nine samples are tested for natural frequency measurements, three for each sample beam width. The recorded velocity data in the time domain are transformed into the frequency domain through the FFT function in MATLAB® R2016a. The natural frequencies are determined by identifying the local maximums and their respective frequencies. Figure 5-5. Figure 5-6, and Figure 5-7 plot the FFT results and marks the velocity peaks. Table 5-2 displays the first three natural frequencies and their means and standard deviations. It is evident from the figures and table that the 20 µm sample has the highest statistical variance out of all sample types. Likewise, the third natural frequency or mode has the highest variance out of all modes. Interconnect beam width have little effect on the overall natural frequencies of the structure due to their relatively small scale. Instead, the board and substrate dominate the vibration response, causing all three sample types to have similar modes.

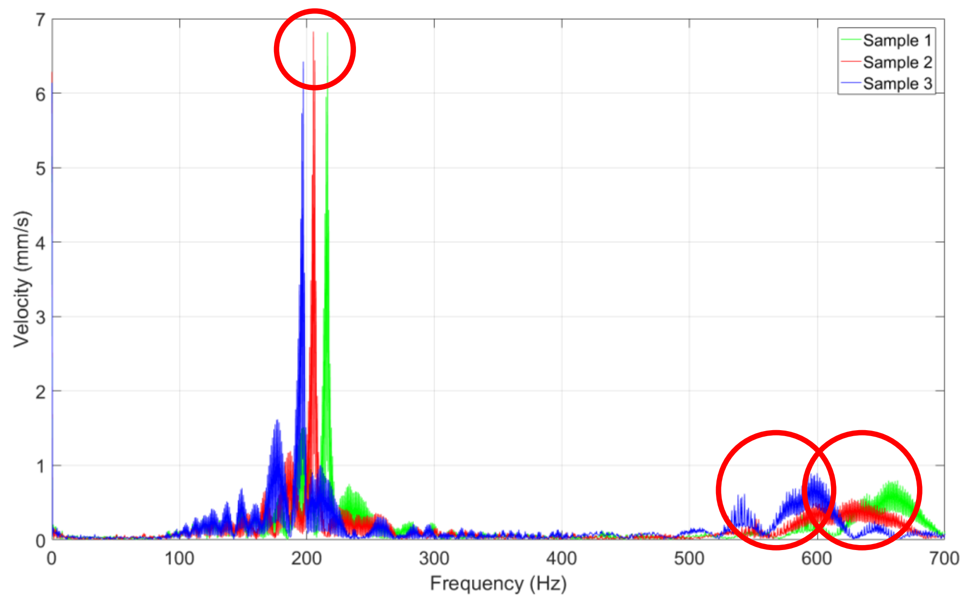


Figure 5-5 FFT of Velocity Measurements (20 µm Sample)

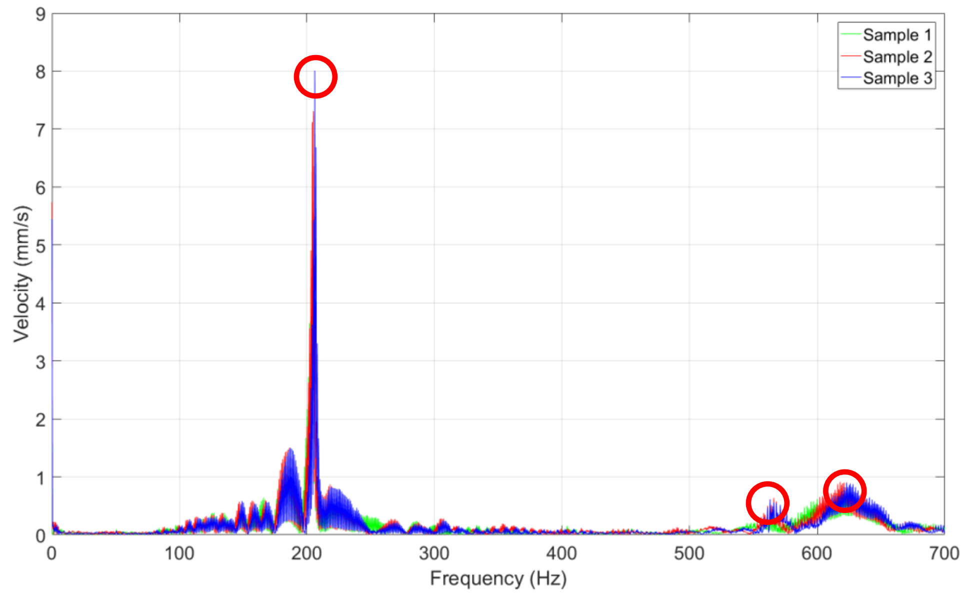


Figure 5-6 FFT of Velocity Measurements (15 µm Sample)

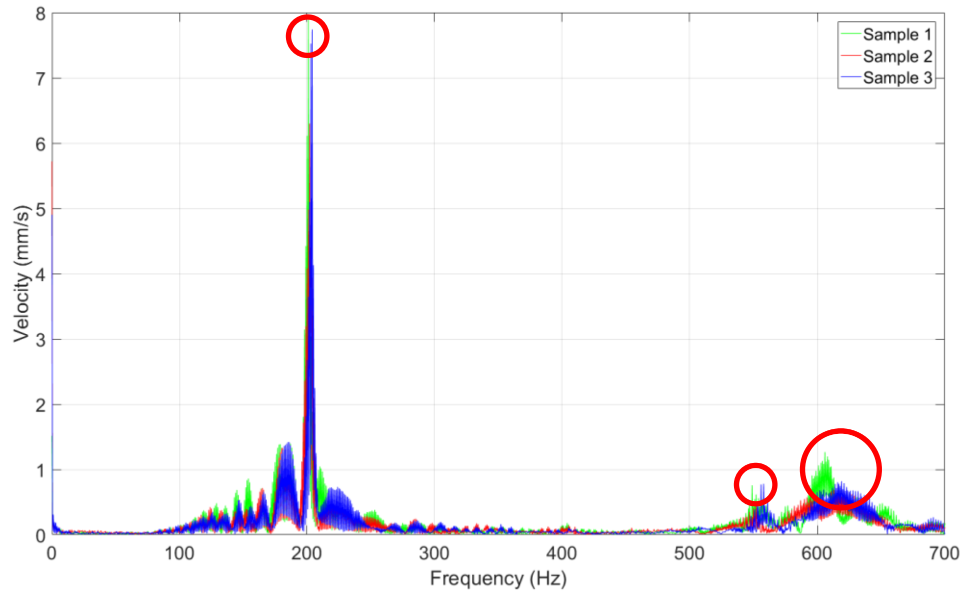


Figure 5-7 FFT of Velocity Measurements (10 μm Sample)

Table 5-2 First Three Natural Frequencies of Test Samples (Unit: Hz)

Beam Width	20 μm			15 μm			10 μm		
Mode	1	2	3	1	2	3	1	2	3
Sample 1	216.5	588.5	663.5	205.5	563.5	621.5	201.5	549.5	606.5
Sample 2	197.5	543.5	600.5	205.5	566.5	618.5	203.5	552.5	616.5
Sample 3	205.5	552.5	627.5	206.5	563.5	623.5	204.5	558.5	619.5
Mean	**206.5**	**561.5**	**630.5**	**205.8**	**564.5**	**621.2**	**203.2**	**553.5**	**614.2**
Standard Deviation	7.789	19.44	25.81	0.471	1.414	2.055	1.247	3.742	5.558

5.2.3. Mode Shape Measurements and Results

The mode shape measurements are performed using the same experiment setup as the natural frequency measurements. The input excitation signal to the shaker is a 200 Hz sine wave with an 11 mm/s peak-to-peak velocity. The frequency of 200 Hz is selected to capture the first mode shape. This value is slightly offset from the exact first natural

frequency to avoid excessive resonance response and nodal lines. By integrating one cycle of the input signal shown in Figure 5-8, the displacement is calculated to be 0.0176 mm.

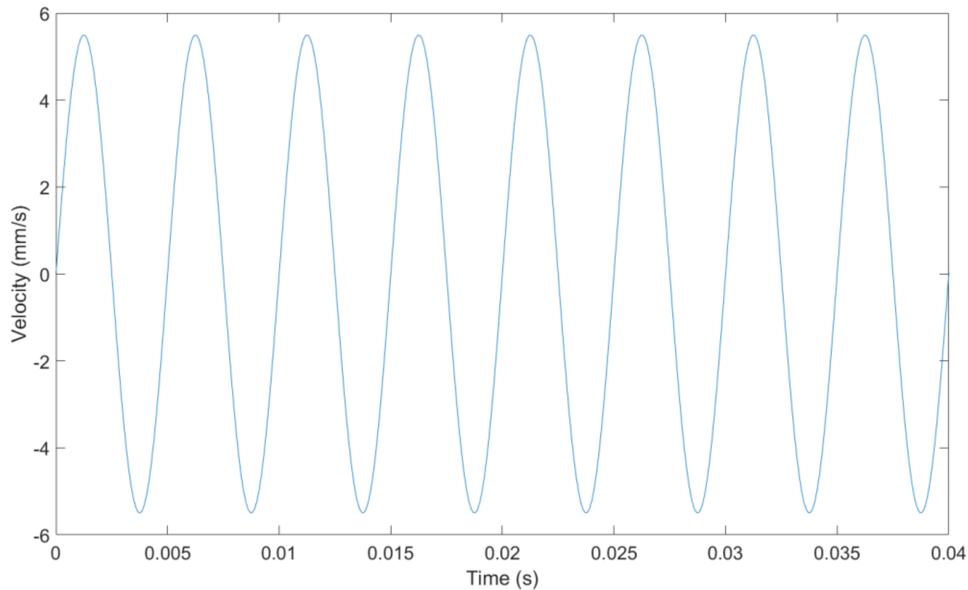


Figure 5-8 Sine Wave Input for First Mode Shape Measurements

Peak-to-peak voltage measurements are recorded for a quadrant of a 20 µm sample at 1 mm intervals as marked in Figure 5-9. Points near the very edge are avoided due to free end effects. Similar to the input, the displacement at each point is calculated based on simple harmonic motion at 200 Hz by integrating the measured velocity sine wave. These values are then meshed in a 500 × 500 point grid in MATLAB®, and the intermediate points are cubically interpolated. The resulting displacement color map of the first mode is presented in Figure 5-10. As expected, the parts of the board furthest away from the fixed pins experience the most displacement. Both the experimental natural frequency and mode shape will be used to validate the simulation models in the next chapter.

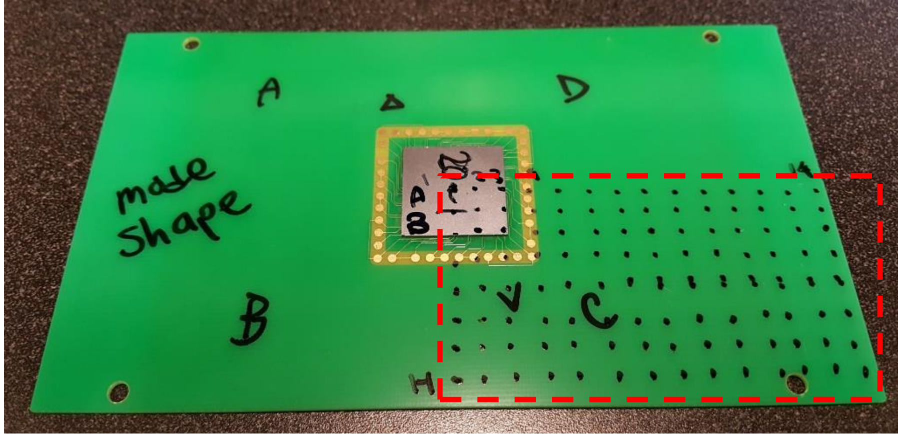


Figure 5-9 Mode Shape Measurement Points (Black Dots on Quadrant C)

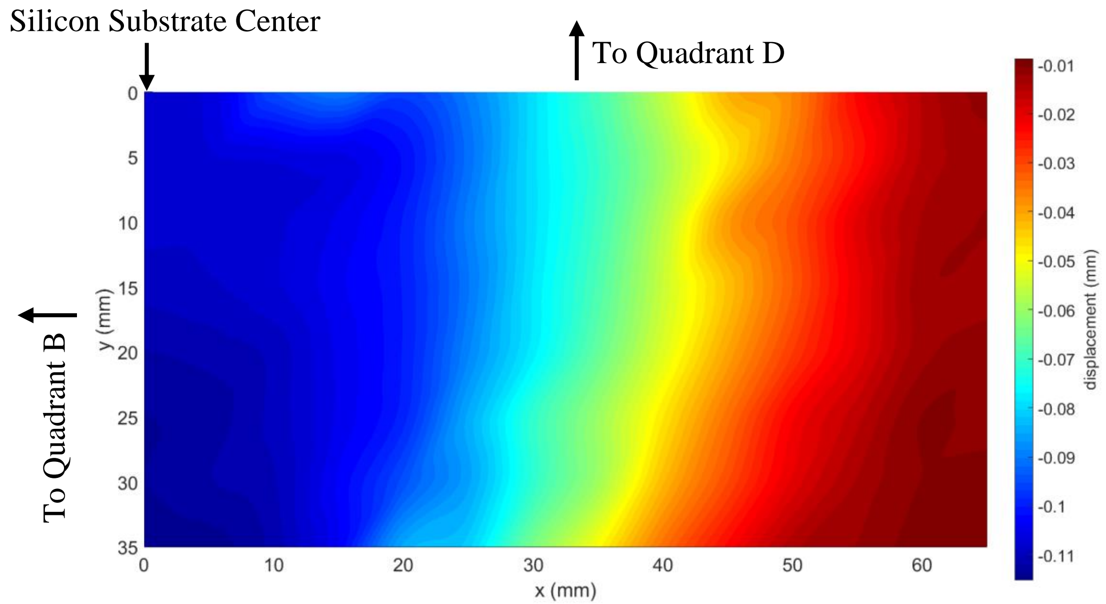


Figure 5-10 Experimental Displacement Mode Shape of Quadrant C at 200 Hz

5.3. Random Vibration Fatigue Experiments

For the various reasons listed in Chapter 2, random vibration loading is chosen as the preferred method of fatigue testing. A total of four samples are tested at a constant

acceleration input and monitored at each corner. The failure locations are then inspected and will be compared to simulation results.

5.3.1. Experiment Setup

The equipment setup for random vibration fatigue tests shares the same components as the one used for vibration characterization. A schematic is shown in Figure 5-11. When available, the function generator and oscilloscope are replaced by a National Instruments® USB-4431 data acquisition (DAQ) system with built in LabVIEW® software that allows for increased control and accuracy over the input random vibration signal. The software is also able to directly transform the measured values from the LDV into acceleration PSD spectrums, saving time on post-processing steps. The Brüel & Kjær® Type 4809 shaker, shown in Figure 5-12, is used in addition to the Type 4810 from previous experiments. The maximum output of the Type 4809 is 4.5 times stronger than the 4810, producing more damaging environments for accelerated fatigue testing.

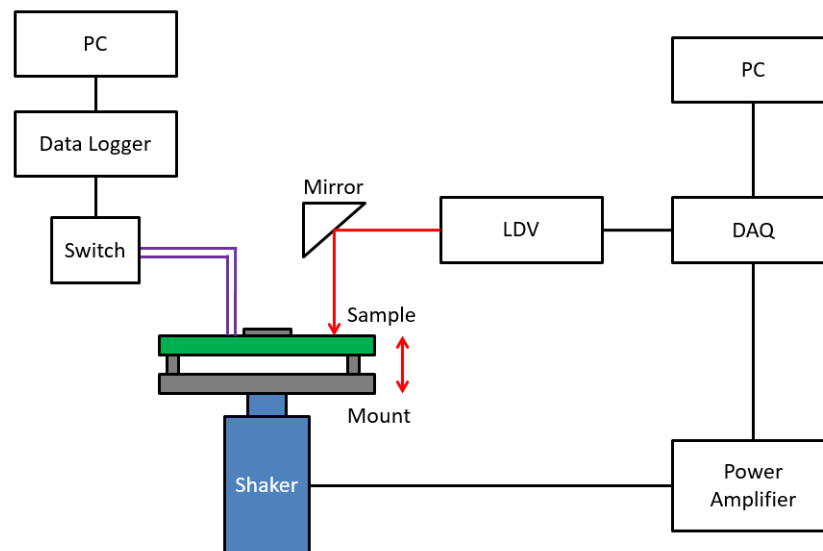


Figure 5-11 Experiment Schematic for Random Vibration Tests

Figure 5-12 B&K Shaker Type 4810 (Left) and 4809 (Right)

Besides the signal input and output setup displayed on the right side of the schematic figure, another set of equipment is integrated into the system to monitor the resistance values at each working corner daisy chain to indicate the time of failure. The probing pads are soldered to wires with no-clean lead-free solder as seen in Figure 5-13. Each corner is connected via an input and output to a 20 channel switch using ultra-flexible silicone rubber wire to reduce interference during vibration. These resistance measurements are recorded with a Keithley® 2700 data logger outfitted with a 7700 multiplexer module card. The data logger is configured through ExcelLINX® software to take measurements at set intervals. A view of this setup is presented in Figure 5-14. The four corner daisy chains are labeled A through D in the counter clockwise direction starting from the top right quadrant as indicated in Figure 5-15.

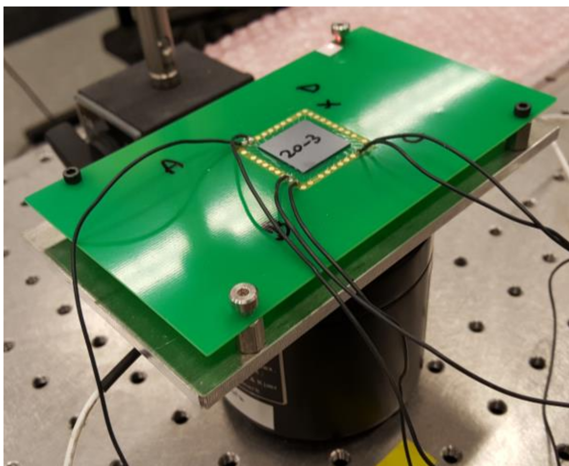


Figure 5-13 Test Sample Monitored at Corner Daisy Chains

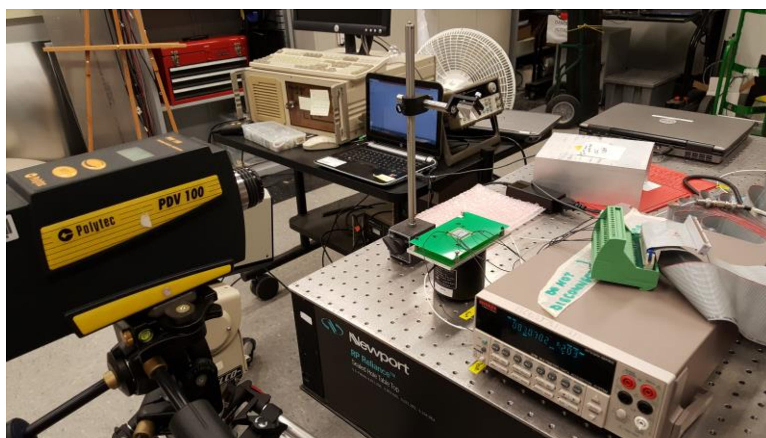


Figure 5-14 Image of Equipment Setup

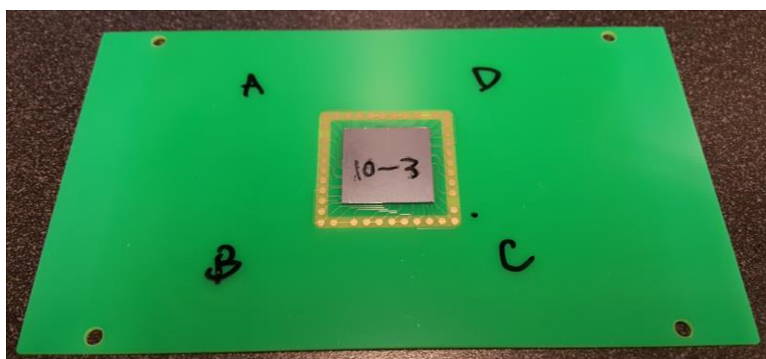


Figure 5-15 Corner Daisy Chain Labels

5.3.2. Sample One

The first sample tested is number four of the 20 μm beam width samples with initial resistance measurements listed previously in Table 5-1. A random signal with a constant acceleration PSD of 1 g^2/Hz is generated by the DAQ and input into the Type 4810 shaker near its max setting. However, due to cut offs, filters, and distortion throughout the amplifier and shaker, the actual resulting input acceleration measurement taken at the shaker table is significantly lower as seen in Figure 5-16. This graph shows a constant acceleration PSD of approximately 0.015 g^2/Hz and a quick ramp up at the beginning. Due to the plate modes inherent to the aluminium mount, the acceleration PSD at each pin hole of the PCB is transformed even further to the graph plotted in Figure 5-17. The acceleration is generally lower at the pins than the center of the shaker, but high peaks exist at frequencies that match the plate modes. An RPSD measurement, shown in Figure 5-18, is also taken at the center of the silicon substrate that will be compared to simulation results.

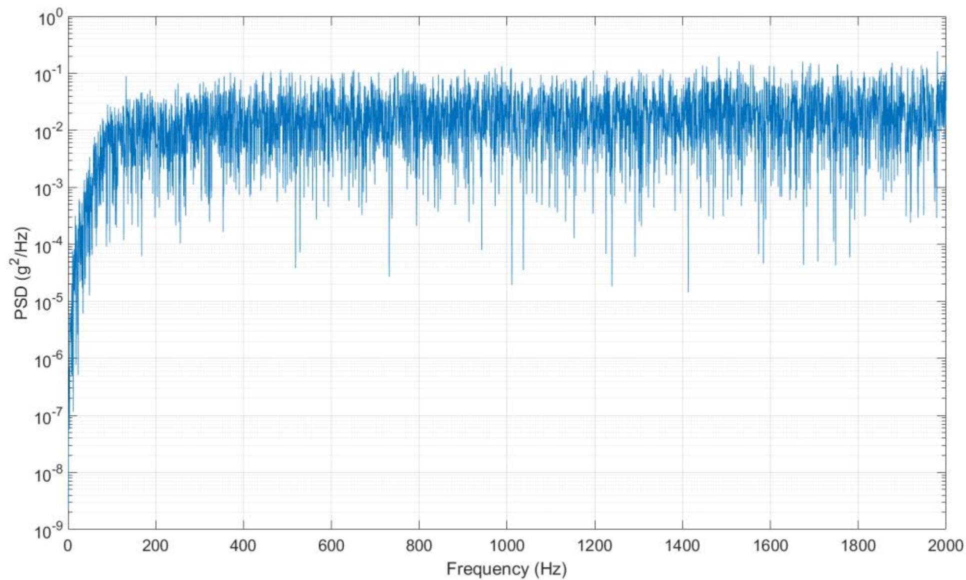


Figure 5-16 Acceleration PSD at Shaker Center for Test One

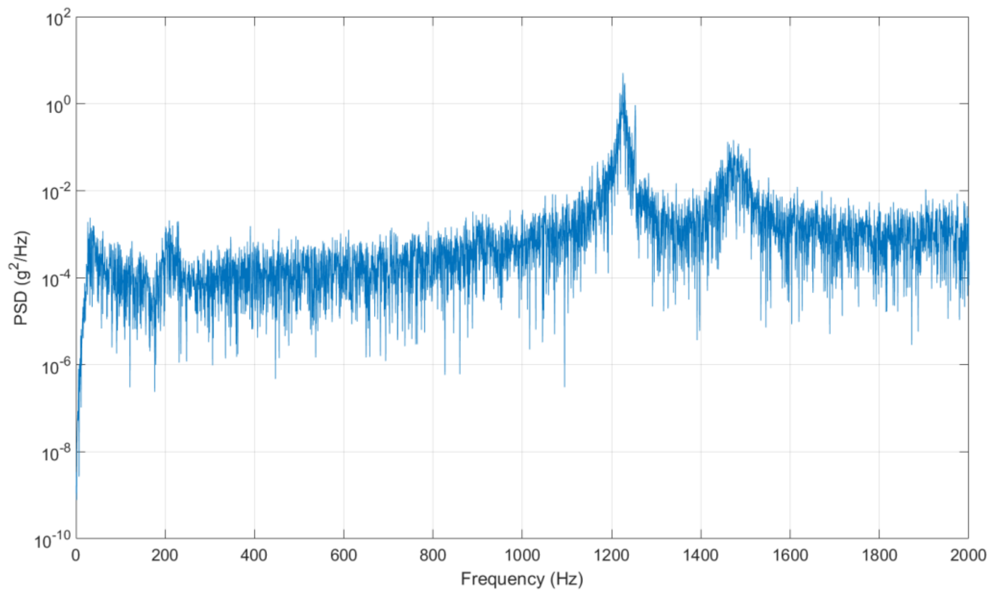


Figure 5-17 Acceleration PSD at Pins for Test One

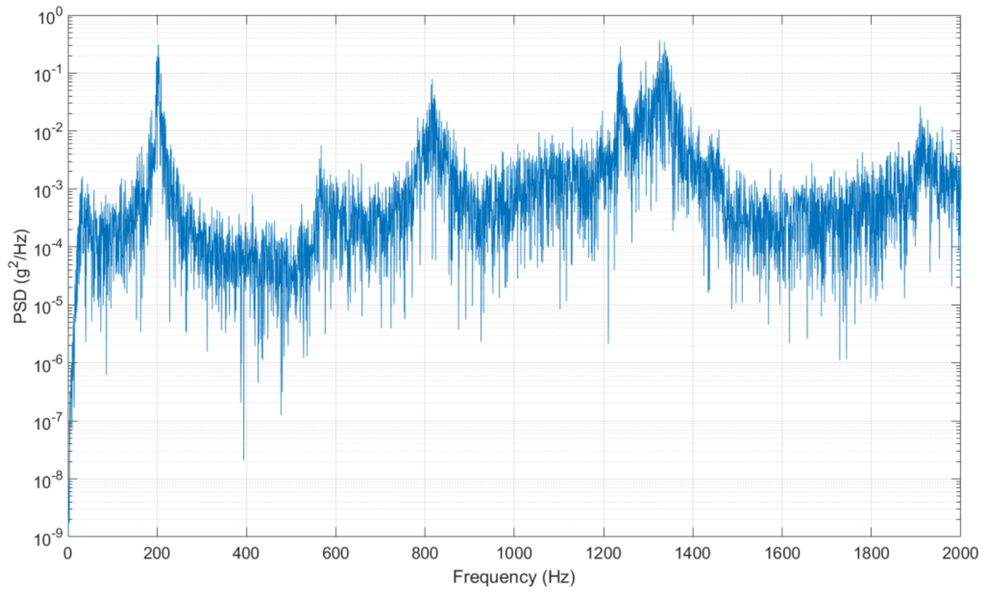


Figure 5-18 Acceleration RPSD at Substrate Center for Test One

Sample one was tested for a total of more than 26 hours over the course of three separate days. The resistance of the three working corner daisy chains are monitored throughout testing. According to IPC/JEDEC-9702 standards, the failure of Second-Level interconnects are indicated by a 20% increase in electrical resistance [93]. Due to instabilities in the data logger that caused large fluctuations, only the measurements for corners A and C are considered and plotted in Figure 5-19. The resistance remains within 20% of the initial value throughout the test and demonstrates an overall decrease due to temperature changes overnight.

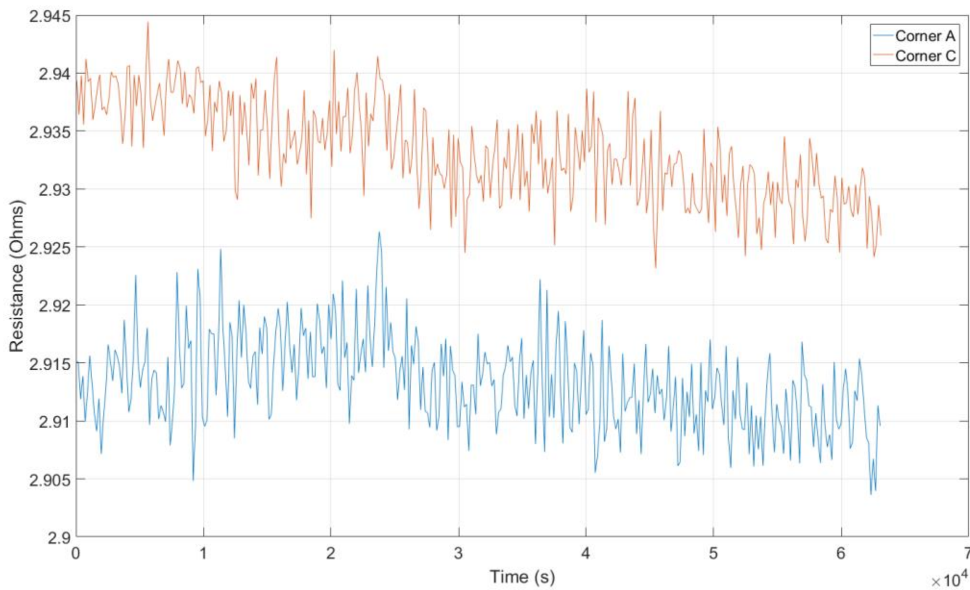


Figure 5-19 Resistance Values of Corner Daisy Chains for Sample One during Random Vibration Fatigue Test on Day Three

Upon X-ray inspection, two compliant interconnects are discovered to have failed. Both interconnects failures occurred on the same arcuate beam and at the same location where the beam attaches to the post as indicated in Figure 5-20. The multi-path electrical

redundancy is demonstrated for this test, since the resistance of Corner A displays little to no change even after failure in the 3-Arc-Fan interconnects. However, the exact time of failure is also difficult to distinguish.

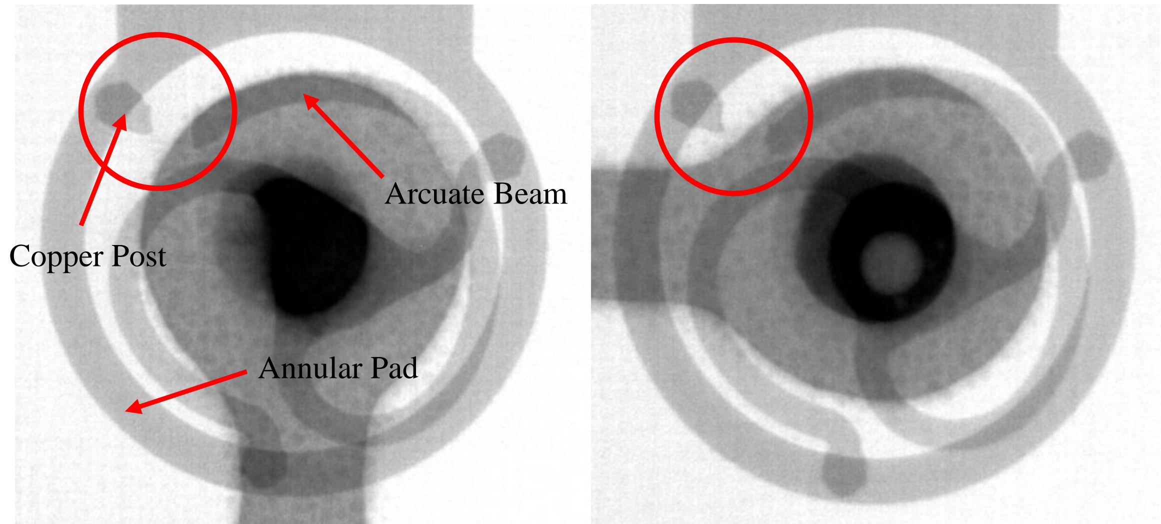


Figure 5-20 Arm Failures of Sample One Corner A

5.3.3. Sample Two

As only two interconnects out of 2000 failed at the max setting of the Type 4810 shaker for sample one, the remaining fatigue tests are performed with the Type 4809. The shaker is adjusted to output a higher excitation as shown in Figure 5-21. Sample two of the random vibration test is also a 20 μm sample with 3 monitored corners. The resistance values at each corner is recorded in Figure 5-22 with failure times indicated by the significant increases in resistance. The fluctuation at the beginning of Corner C is due to the instability and sensitivity of the switch and wire connection, which later stabilizes until failure.

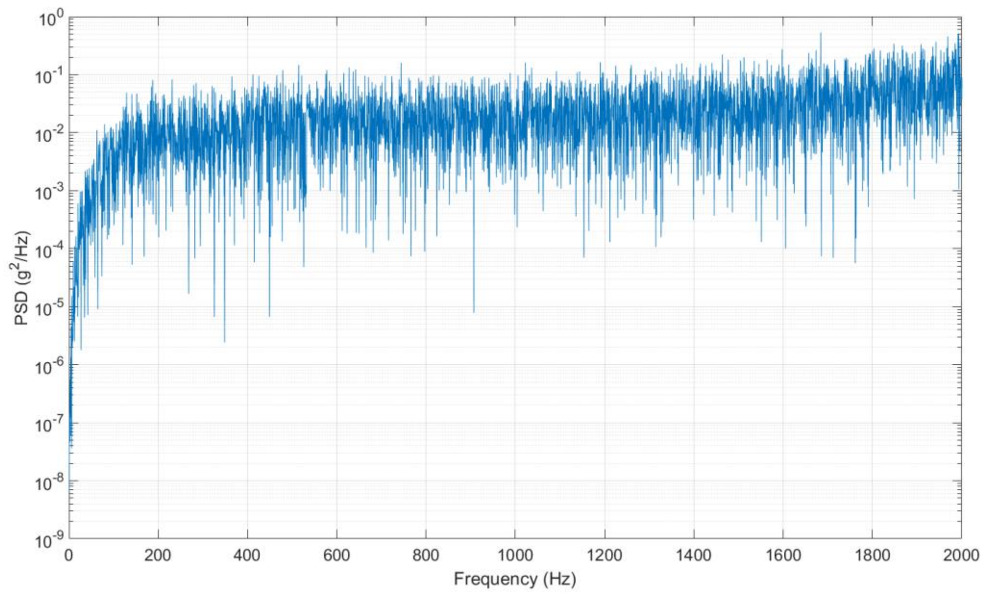


Figure 5-21 Acceleration PSD at Shaker Center for Test Two

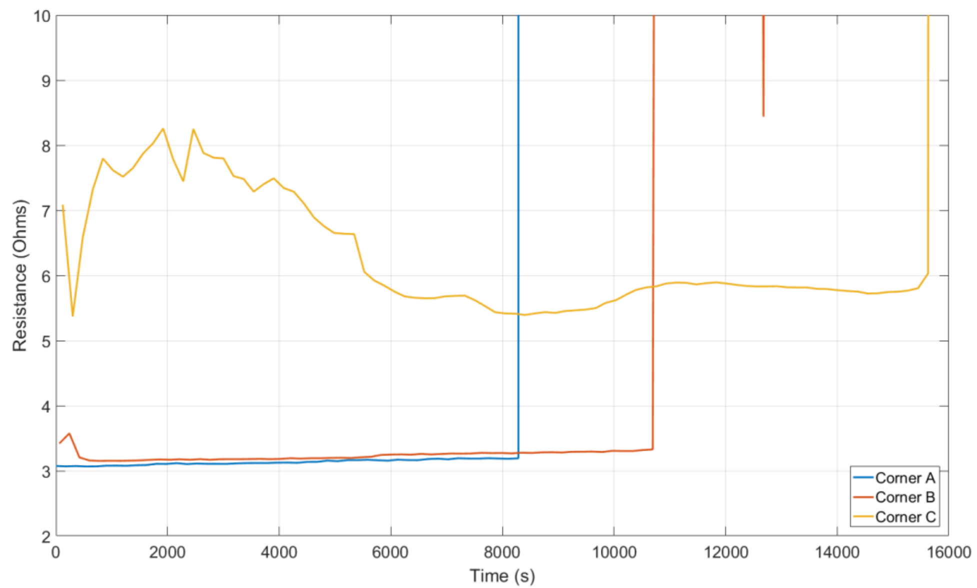


Figure 5-22 Resistance Values of Corner Daisy Chains for Sample Two during Random Vibration Fatigue Testing

Images of the HCF failure locations are viewable in Figure 5-23. Only the interconnects at the 4 × 4 corner daisy chains failed, supporting previous evidence of critical failure joints. In addition, the failures occur consistently in the arcuate beams with the same orientation across each corner. Typically, the one furthest away from the center is the first to fail. Figure 5-24 shows intact interconnects closer to the center of the silicon substrate where failure did not occur after the fatigue test.

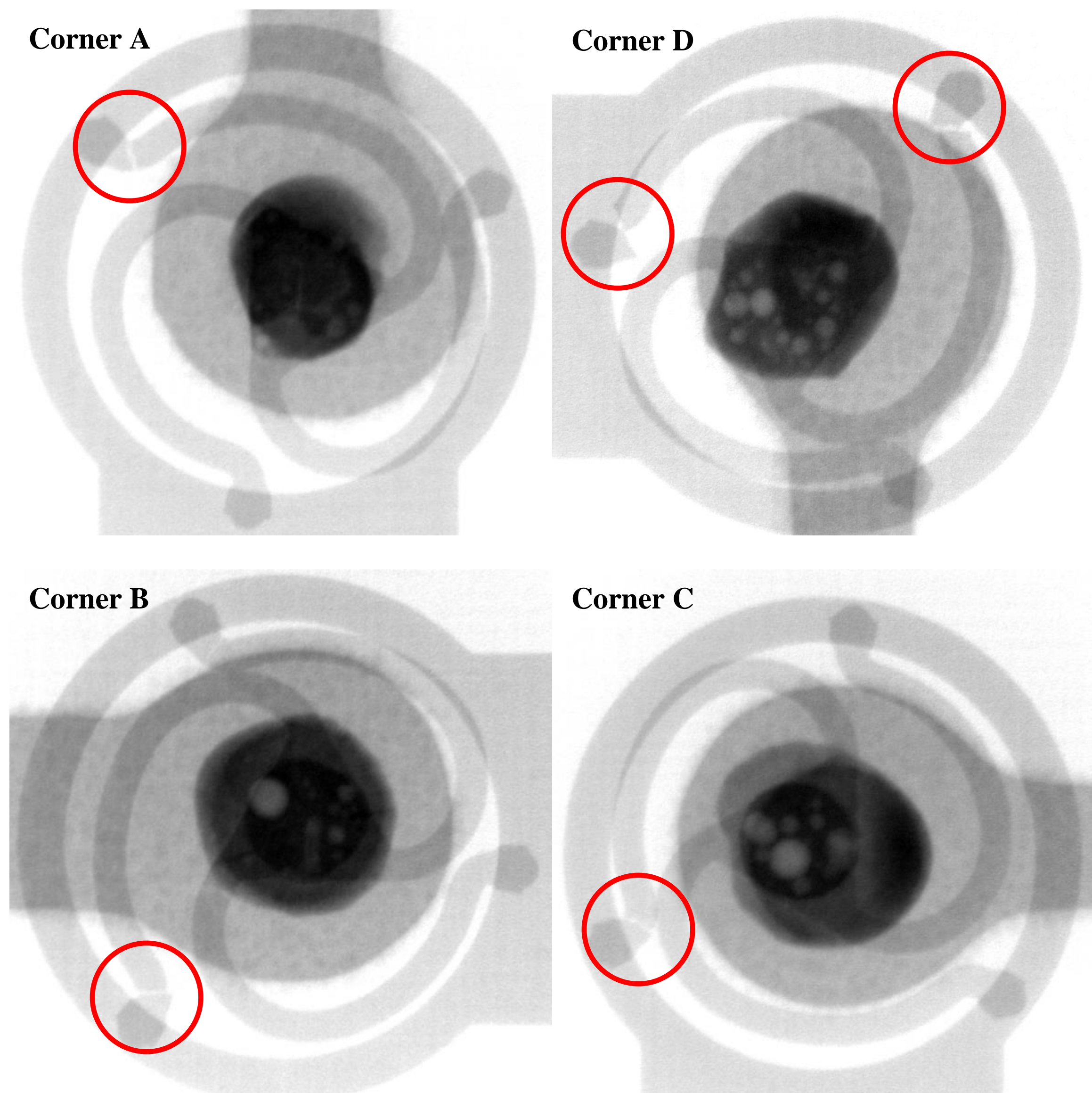


Figure 5-23 X-ray Images of Arm Failures for Sample Two

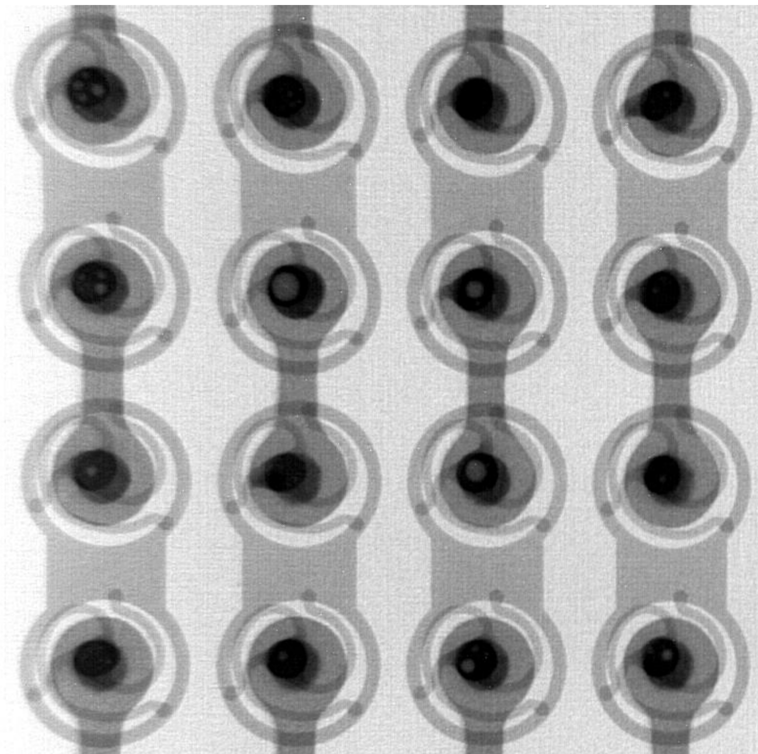


Figure 5-24 Intact Interconnects of Sample Two after Random Vibration Fatigue

5.3.4. Sample Three

To compare the reliability of the different beam widths, a 15 μm interconnect is tested as sample three with the same input excitation from the previous test. The resulting resistance measurements is plotted in Figure 5-25. Corner A is shown to have failed after several minutes and should be considered an outlier. This is possibly due to weakened interconnect arms from the fabrication and assembly process. Corner D also demonstrates resistance spikes prior to failure, which is caused by the sensitivity of the data logger connection. The actual failure times are marked by red arrows in the figure. X-ray images of arm failures at one corner are indicated in Figure 5-26. These failures locations are not only consistent within each corner, but are also consistent when compared to prior failure locations for the 20 μm samples. Based on the average time to failure of the corners, 15

μm interconnects demonstrate better reliability than their 20 μm counterparts under vibration loads.

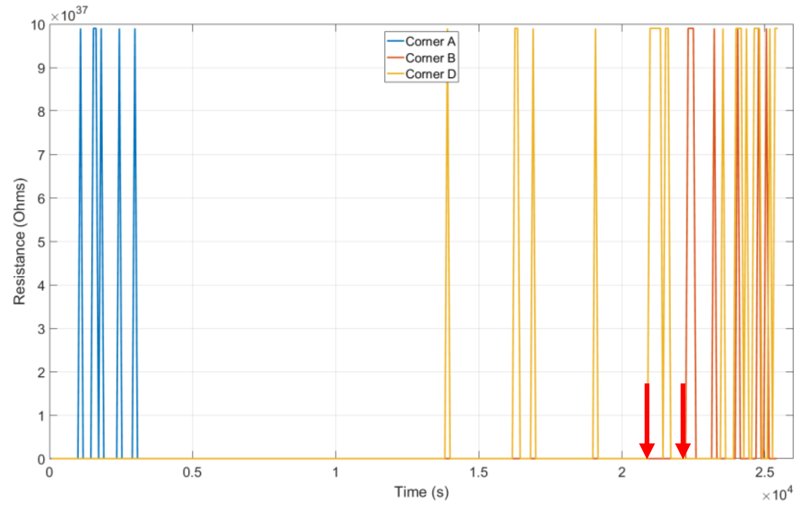


Figure 5-25 Resistance Values of Corner Daisy Chains for Sample Three during Random Vibration Fatigue Testing

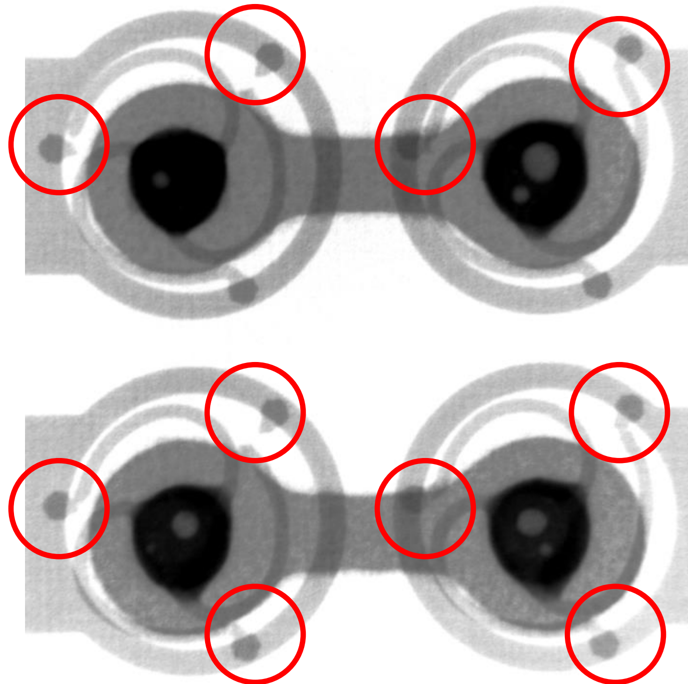


Figure 5-26 X-ray Image of Arm Failures for Sample Three Corner D

5.3.5. *Sample Four*

The last random vibration fatigue test is performed on a 15 μm sample at an intermediate level of excitation. The input acceleration PSD of both the center of the shaker and top surface of the pins are graphed in Figure 5-27. The resulting resistance curves for fatigue life are shown in Figure 5-28. The failures of the monitored corners occur at close intervals and are consistent in location upon inspection. In addition, the multi-path arms of the 3-Arc-Fan at Corner D allows the daisy chains to continue operation even after fracture has occurred in several arms; the resistance change remains within the JEDEC operable standards even after the conclusion of the test.

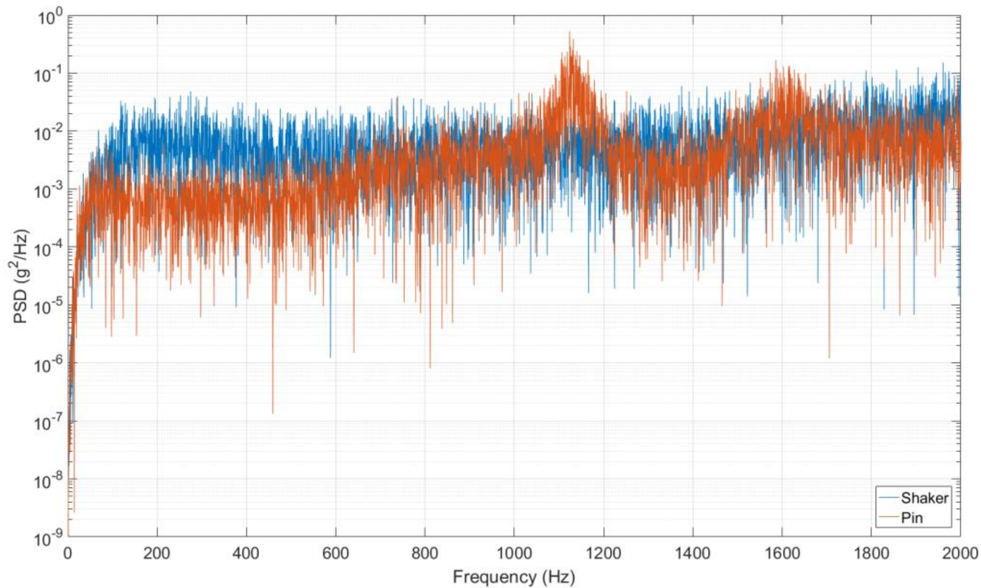


Figure 5-27 Acceleration PSD at Shaker Center and Pins for Test Four

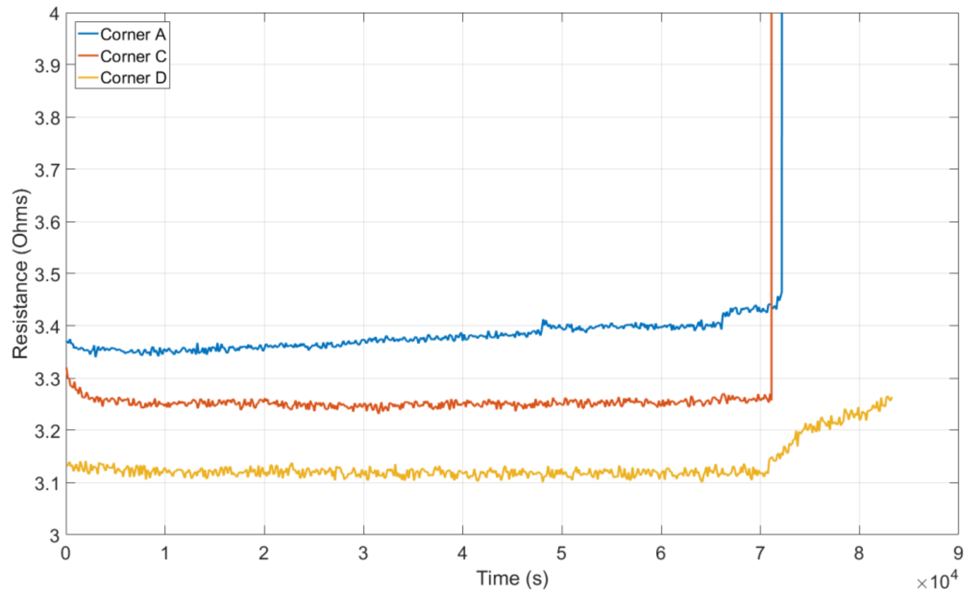


Figure 5-28 Resistance Values of Corner Daisy Chains for Sample Four during Random Vibration Fatigue Testing

5.4. Summary

The natural frequency and mode shape tests provided insight into the vibration response of 3-Arc-Fan compliant interconnect packages, which allowed for the development of a random vibration fatigue test methodology. Random vibration signals at a constant spectral acceleration of different magnitudes are applied in the out-of-plane direction. The HCF fatigue life is captured through electrical resistance monitoring, and failure locations are examined via X-ray inspection. Four major observations are made for 3-Arc-Fan interconnects under random vibration loads:

1. The high cycle vibration fatigue life is inversely related to beam width. The larger beam width samples fail earlier due to higher stiffness. This is consistent with thermal cycling results [17].

2. The primary failure location is the stress concentration located at the area where the arcuate beams attach to the annular pad via the copper post. The arm location and crack propagation direction remains consistent within the interconnects at the same corner and also with those on other samples.
3. The rotational orientation of the interconnects factors into the fatigue life of 3-Arc-Fan interconnects. The first arcuate beam to fail is typically the one furthest away from the center.
4. The multi-path structure creates redundancies in both the electrical and mechanical connection of the package. Even after the failure of several arms, the interconnect still maintains a low resistance within operational standards. This significantly improves packaging reliability when compared to traditional BGAs where the fracture of a single solder bump can lead to failures in the entire system.

Overall, the experimental vibration testing results are recorded through the different tests. They will be compared to the simulation results obtained in the next chapter and act as model validation. The fatigue life monitored through resistance will also be implemented to calculate a preliminary HCF life prediction model.

CHAPTER 6

SIMULATION AND FINITE ELEMENT ANALYSIS OF 3-ARC-FAN COMPLIANT INTERCONNECTS UNDER VIBRATION LOADS

The location and scale of microelectronic packaging interconnects create difficulties in experimentally capturing their structural behavior during testing. Therefore, computer simulations using FEA is a common method incorporated to analyze interconnects. For vibration loading of 3-Arc-Fan compliant interconnects, several different models are developed and validated through structural, modal, harmonic, and spectrum analysis with ANSYS® Mechanical™ 17.1 to ultimately determine their vibration response.

6.1. Finite Element Model Development

One of the key challenges of constructing a finite element model for the 3-Arc-Fan interconnect package is the amount of elements needed. Due to the relative scale of the package and individual interconnect, the entire package cannot be modeled and will require simplification while maintaining result accuracy.

6.1.1. Material Models and Element Selection

Four main types of materials are present in the assembled 3-Arc-Fan package, copper, SnAg solder, silicon, and FR-4. As the strains experienced during vibration testing are extremely small, these materials will remain in the elastic regime and will behave linearly. Due to the composite fibers that are used to strengthen the epoxy resin in FR-4, the material properties are direction dependant with respect to the fibers. Therefore, FR-4

is considered orthotropic, while all other materials are isotropic. Table 6-1 and Table 6-2 lists the corresponding material properties of each material, where *y* is the out-of-plane direction.

Table 6-1 Linear Isotropic Material Properties [17]

	Copper	Solder	Silicon
Young's Modulus (GPa)	117	47.5	130
Poisson's Ratio	0.34	0.35	0.28
Density (g/cm^3)	8.96	7.36	2.32

Table 6-2 Linear Orthotropic Material Properties for FR-4 (*E*: Young's Modulus, *G*: Shear Modulus, *v*: Poisson's Ratio) [17]

	FR4
E_x **(GPa)**	22.4
E_y **(GPa)**	1.6
E_z **(GPa)**	22.4
G_{xy} **(GPa)**	0.199
G_{xz} **(GPa)**	0.630
G_{yz} **(GPa)**	0.199
v_{xy}	0.143
v_{xz}	0.136
v_{yz}	0.143
Density (g/cm^3)	1.898

The element types selected for meshing these materials are solid 185, solid 186, and mesh 200 elements. Solid 185 elements are 3D rectangular 8-node homogeneous structural elements that offer greater accuracy than tetrahedral elements and balanced computational time. The majority of the model is meshed with this type of element. Solid

186, on the other hand, are 3D 20-node homogeneous structural elements that allows a combination of rectangular, tetrahedral, and pyramidal elements. These elements are used to efficiently transition from a fine to coarse mesh in the regions around the compliant interconnect. Lastly, mesh 200 elements are integrated into the volume meshing process as intermediate steps and do not factor into the calculations or solutions.

6.1.2. Interconnect Geometry and Equivalent Column

An isometric view of an individual 3-Arc-Fan compliant interconnect model is presented in Figure 6-1. The model is constructed based on the optimized geometry used for fabrication and has adjustable beam widths of 10, 15, and 20 μm as seen in Figure 6-2. However, a single meshed interconnect model easily exceeds 1500 elements, which quickly becomes unmanageable with over 2000 interconnects per package. Therefore, it is critical to simplify the interconnect geometry for analysis.

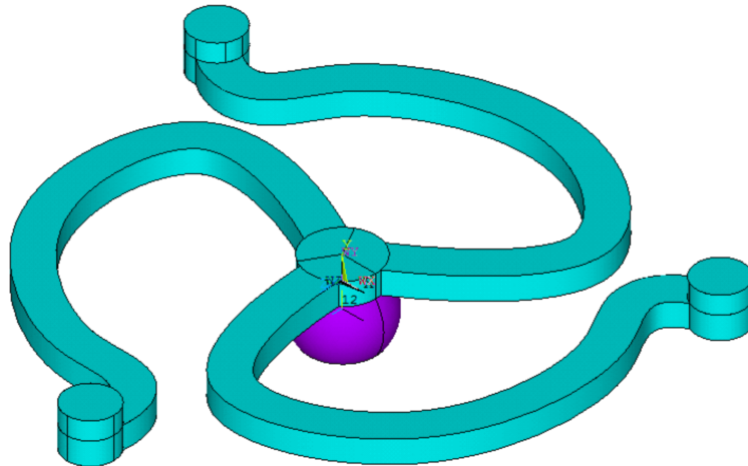


Figure 6-1 ANSYS® Model of Individual 3-Arc-Fan Interconnect

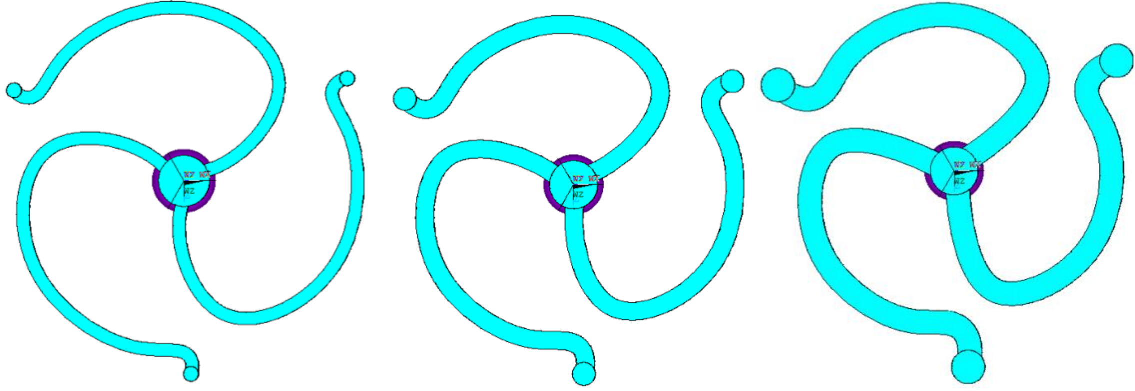


Figure 6-2 Top View of 10 (Left), 15 (Middle), and 20 (Right) µm Model

An equivalent cylindrical column model is proposed and investigated as a simplification to replace the full interconnect model. This model must exhibit the same structural and compliant material properties as the interconnect during vibration loads, which is primarily determined by the Young's modulus. Therefore, a compliance analysis is performed on both the full interconnect and simplified column model to calculate the equivalent Young's modulus. This involves a static structural analysis by fixing the displacement of the full interconnect model at the three copper posts and applying a pressure from the bottom surface of the solder ball as shown in Figure 6-3. The resulting maximum displacement is used to calculate the out-of-plane compliance with Equation 5.

$$C_{out-of-plane} = \frac{\delta_{max}}{F} \tag{5}$$

Where C is the compliance, δ is the displacement, and F is the input force. The equivalent Young's modulus, E, can then be calculated with Equation 6.

$$C_{out-of-plane} = \frac{h}{E\pi r^2} \tag{6}$$

Where h is the height of the equivalent cylinder and interconnect at 54 µm and r is the radius of the cylinder at 140 µm. In addition to Young's modulus, Poisson's ratio and

density are also required for linear isotropic models. A zero value for Poisson's ratio is used for this case as there is no load applied in the in-plane direction and only out-of-plane loads are considered. The density is obtained through the rule of mixtures with copper and SnAg solder calculated in Equation 7.

$$\rho_{equivalent} = V_{p1}\rho_1 + V_{p2}\rho_2 \tag{7}$$

Where ρ is the density and V_p is the percent volume of the material. The resulting material properties and compliance comparison are presented in Table 6-3.

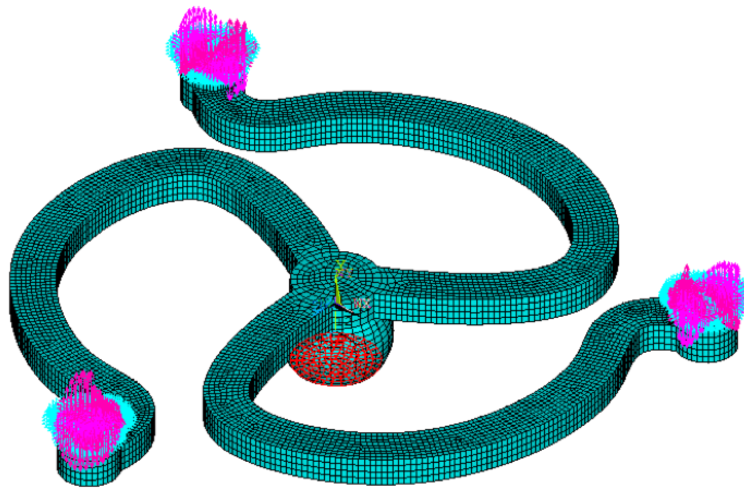


Figure 6-3 Boundary Condition and Loads for Compliance Analysis

Table 6-3 Equivalent Column Material Properties and Comparison

Beam Width (μm)	Equivalent Modulus (MPa)	Density (g/cm^3)	Simulation Compliance (mm/N)	Experimental Compliance (mm/N) [17]
20	0.601	8.69	1.46	2.31
15	0.361	8.63	2.43	2.97
10	0.157	8.53	5.57	5.52

The Young's modulus is several orders of magnitude less than the other materials due to the high compliance provided by the copper arcuate beams. It is also observed that the larger beam width models have higher errors between simulation and experimental compliance. This error stems from the geometric discrepancies between the optimized model and actual fabricated interconnect, which becomes more prevalent at the arcuate beams with respect to increasing width.

6.1.3. Equivalent Column Model Validation

Validation of the simplified equivalent column model is achieved through mesh convergence studies and harmonic result comparisons with the full interconnect model. A 400 μm × 400 μm vertical section is extracted from the package containing the silicon substrate, FR-4 board, and a single interconnect. The boundary conditions are fixed in all degrees of freedom (DOF) at the bottom of the board and only allowed in the out-of-plane direction at the top of the substrate. A surface pressure of 4 kPa is applied to the top of the chip at 400 Hz in a harmonic analysis, and the max peak-to-peak out-of-plane displacement data is compared as seen in Figure 6-4.

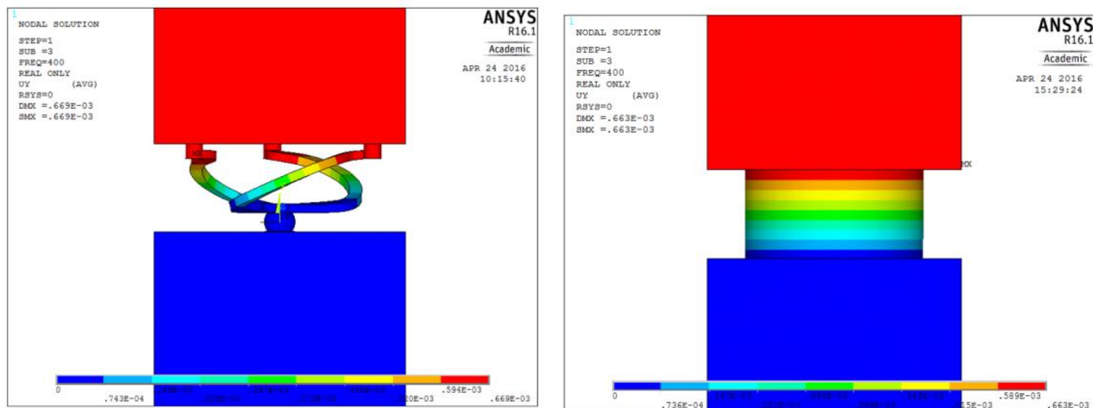


Figure 6-4 Harmonic Displacement Contour Plot Comparison of Vertical Columns

By gradually increasing mesh density until convergence, the equivalent model is proved to demonstrate the same displacement at a much lower mesh density as shown in Figure 6-5. Therefore, the accuracy of the results are maintained, while the number of elements are significantly decreased from close to 40000 elements to under 1000 elements. The displacement value is further verified through finite element hand calculations using the three element simple beam model in Figure 6-6. The subsequent assembled 4×4 stiffness matrix produces results within 1% error for all three beam widths. Thus, the proposed equivalent cylindrical model successfully simplifies the full geometry of the 3-Arc-Fan compliant interconnect.

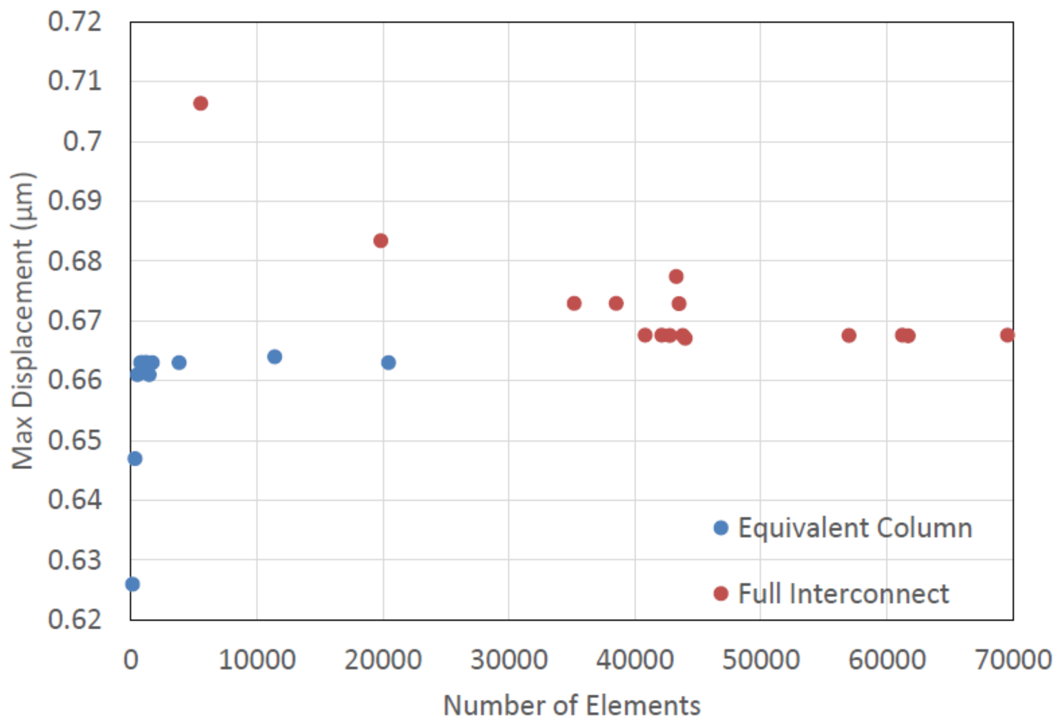


Figure 6-5 Mesh Convergence Comparison

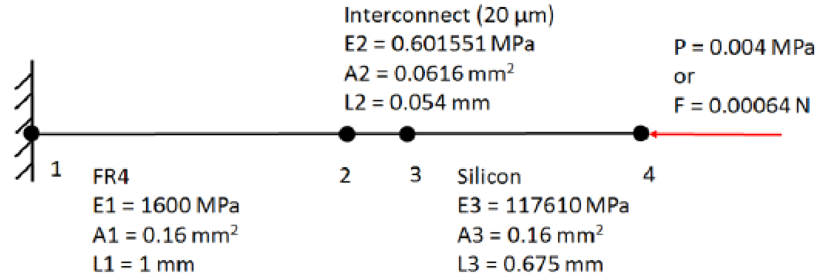


Figure 6-6 Simple Beam Model for Validation

6.1.4. Quarter Symmetry Model

As the assembled 3-Arc-Fan package is quarter symmetrical, the same can be stated for the FEA model. Therefore, the various vibration simulations will be performed using the quarter symmetry model shown in Figure 6-7. This model contains a 22 × 22 area array of interconnects. All but two are modeled using the simplified equivalent column; the two interconnects at the locations marked in Figure 6-8 are modeled fully. One of the two is the corner interconnect furthest away from the center, which is identified as the critical failure location from many literature sources and previous testing of the 3-Arc-Fan compliant interconnect. The other is the interconnect closest to the center, which experiences the largest peak-to-peak displacement as measured during experimental testing.

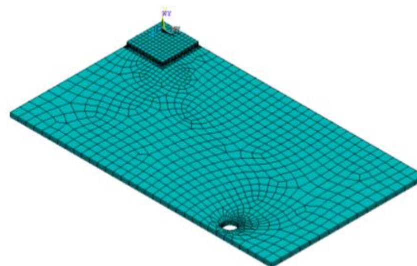


Figure 6-7 ANSYS® Model of Quarter Symmetrical 3-Arc-Fan Package

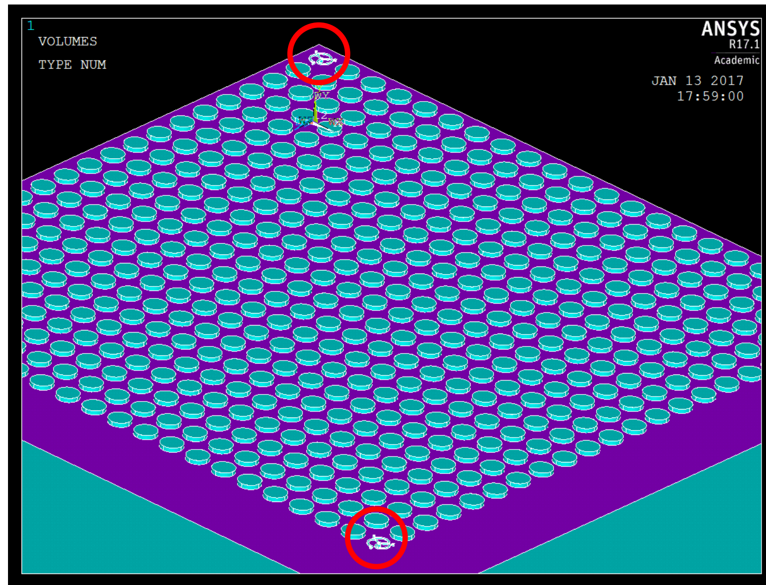


Figure 6-8 Interconnect Area Array on Quarter Symmetry Model

As mentioned earlier, solid 186 transition elements are used in the areas with interconnects to convert from a fine interconnect scale mesh to a coarse board and substrate scale mesh. Different views of the transition mesh area are illustrated in Figure 6-9 and Figure 6-10. Areas where the 3-Arc-Fan interconnect are modeled fully also demonstrate considerably denser transitions as seen in Figure 6-11. Without these transition elements, the mesh at each interconnect will extend through the layers of the substrate and board, significantly increasing the computation time. With transition elements, the total number of elements is decreased from the 179,456 of previous models to only 79,187 elements, a decrease of more than 50%. This reduction allows for faster build and run times, while maintaining the same level of accuracy in results.

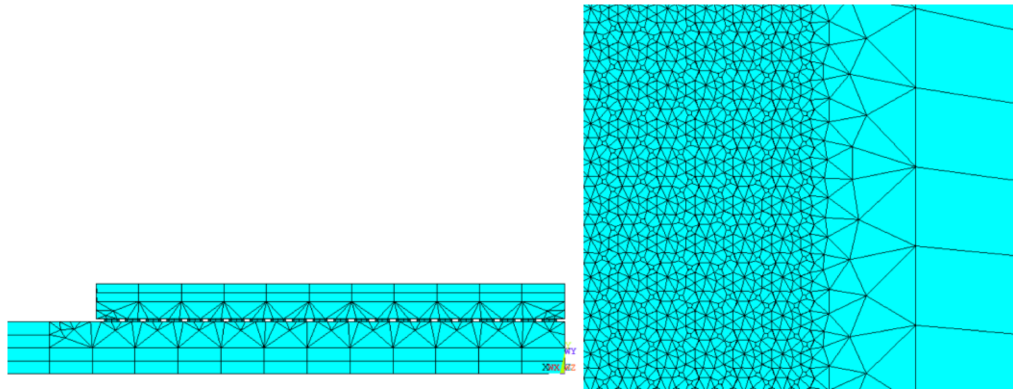


Figure 6-9 Transition from Fine to Coarse Mesh. Side View (Left) and Top View (Right)

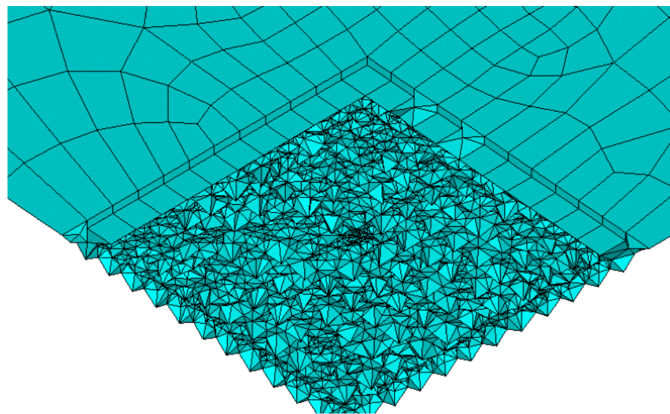


Figure 6-10 Isometric Cut-out of Transition Area Showing a Mix of Element Shapes

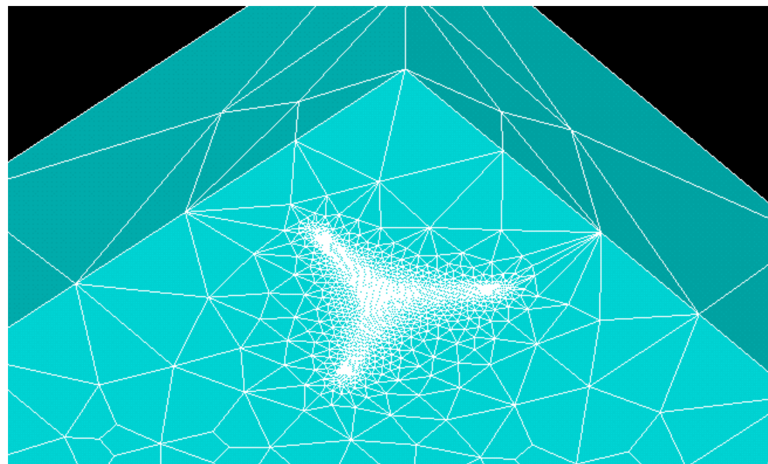


Figure 6-11 Transition Area of Full Interconnect Model at the Substrate

6.1.5. Boundary Conditions and Loads

Standard symmetry boundary conditions are applied to the appropriate surfaces of the package to fix the displacement in the perpendicular to the face. For modal analysis, the pin is also fixed in all DOFs and no additional load is needed. In the case of harmonic and spectrum analysis, the pin is used as the input load location. A displacement profile is specified for harmonic analysis, while an acceleration PSD base excitation is specified for spectrum analysis. Figure 6-12 shows the locations for the boundary conditions and loads applied on the symmetry faces and pin.

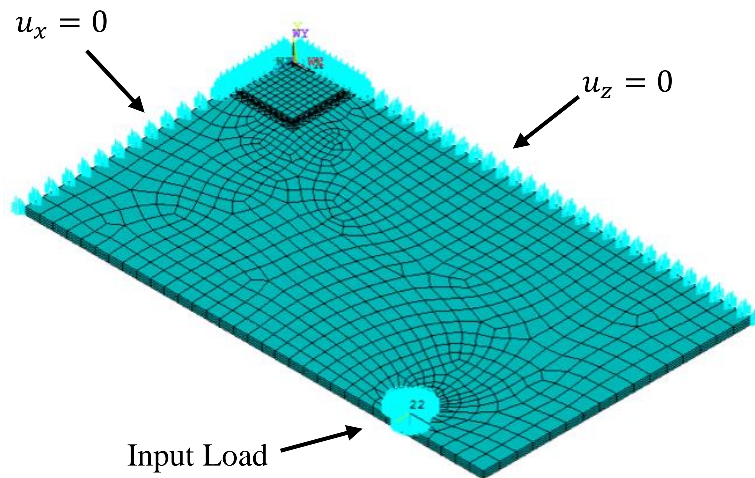


Figure 6-12 Boundary Condition and Loads for Quarter Symmetry Model

6.2. Simulated Vibration Characterization

Similar to the experimental procedure, an initial vibration characterization is performed on the quarter symmetry model to observe its response before proceeding with more in depth forms of analysis. Two types of analysis are used in this process, modal and harmonic. The results of these two analyses will be compared with the experimental results to validate the quarter symmetry model.

6.2.1. *Modal Analysis and Natural Frequency Validation*

A modal analysis is performed on the quarter symmetry with the aforementioned boundary conditions. A Block Lanczos eigenvalue solver is used to determine the first 12 natural frequencies of the model. These values are tabulated in Table 6-4. The scaled displacement mode shape of the first six modes for the 20 μm beam width are also compared in Figure 6-13 to demonstrate the effect of frequency on deformation. As identified by the experiments, the first three modes under 1000 Hz are the most prominent during vibration loading and are selected to validate the FEA model. Table 6-5 compares the average experimental natural frequencies to the modal analysis results. The errors of each mode are all within acceptable ranges, thus, validating the quarter symmetry model.

Table 6-4 First 12 Natural Frequencies (Unit: Hz)

Mode	Beam Width (μm)		
	10	**15**	**20**
1	192.87	193.15	193.39
2	511.44	511.71	511.94
3	654.90	659.38	663.18
4	1112.5	1118.8	1123.3
5	1661.2	1664.3	1666.2
6	2311.2	2313.0	2313.7
7	2510.2	2557.6	2577.6
8	2912.9	2954.6	2975.0
9	3170.3	3180.0	3185.6
10	3529.2	3567.1	3580.3
11	3812.1	3819.7	3822.1
12	4251.0	4376.6	4398.0

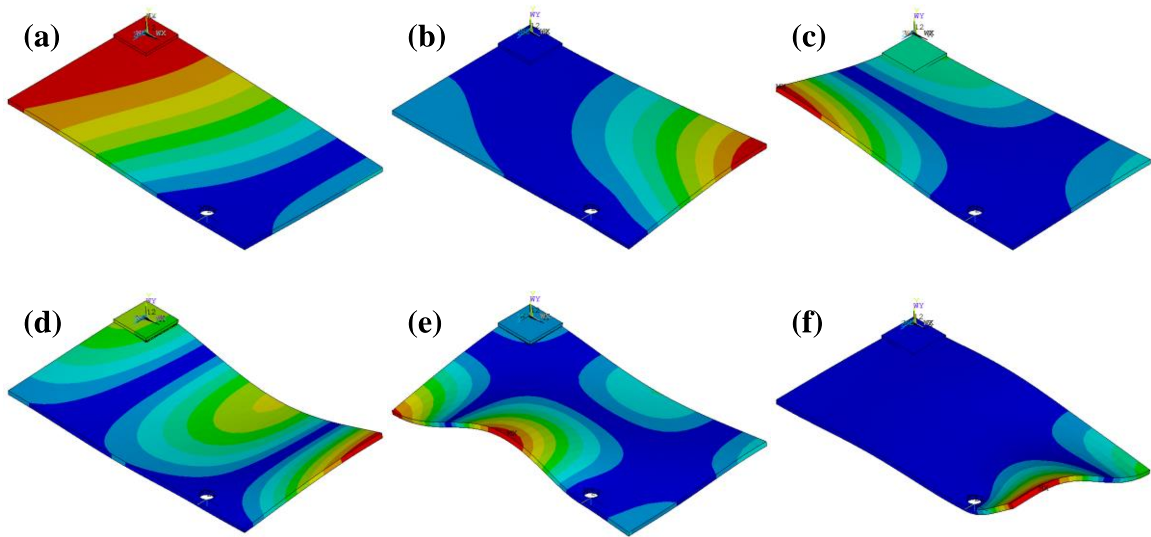


Figure 6-13 Simulated Mode Shape of (a) First Mode to (f) Sixth Mode

Table 6-5 Natural Frequency Validation

Beam Width (μm)	Mode	Natural Frequency (Hz)		Error (%)
		Experimental Average	Modal Simulation	
20	**1**	206.5	193.4	6.3
	2	561.5	511.9	8.8
	3	630.5	663.2	5.2
15	**1**	205.8	193.2	6.2
	2	564.5	511.7	9.4
	3	621.2	659.4	6.2
10	**1**	203.2	192.9	5.1
	2	553.5	511.4	7.6
	3	614.2	654.9	6.6

6.2.2. Harmonic Analysis and Mode Shape Validation

To compare against the experimental mode shape measured previously, a harmonic analysis of the quarter symmetry model is also performed. The pins are excited via

sinusoidal displacement, with a peak-to-peak value of 0.0176 mm, matching that of the input during the experiment. The harmonic analysis is performed for a frequency of 200 Hz, and the resulting contour plot is compared to the experimental mode shape in Figure 6-14. Both the contours and magnitude are in good agreement, further verifying the accuracy of the quarter symmetry model.

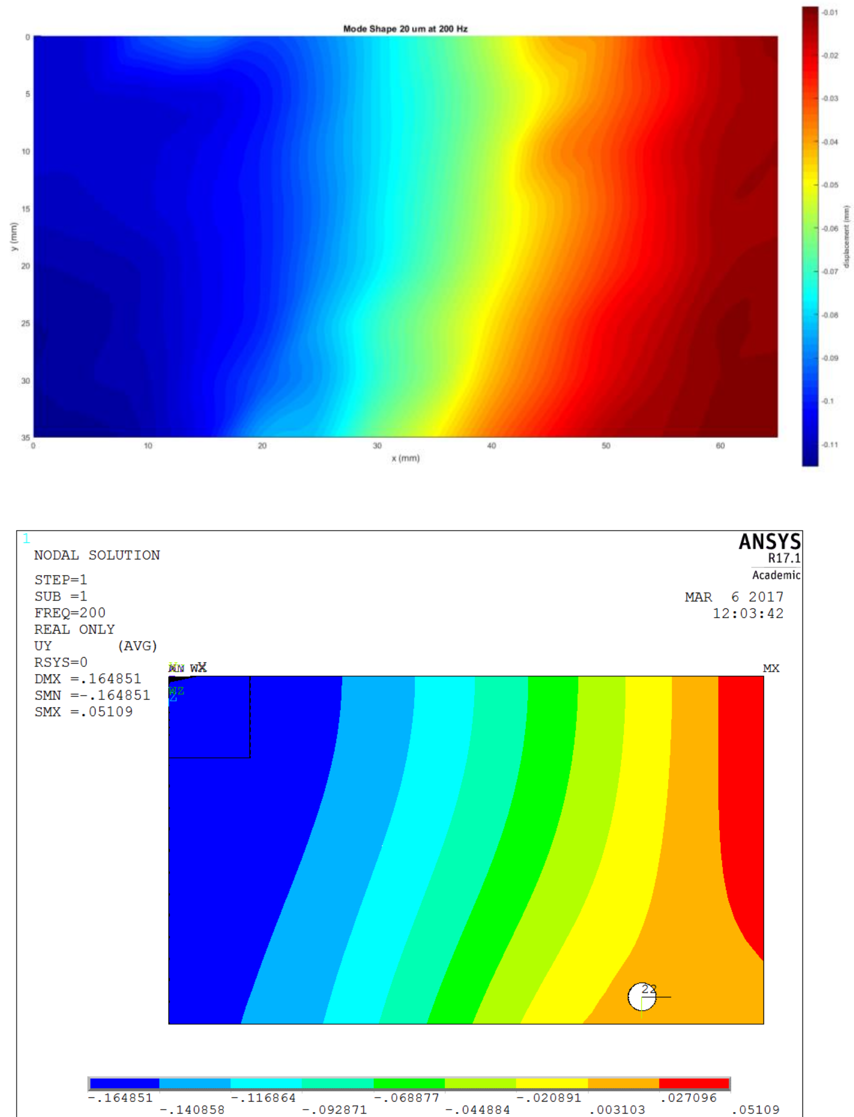


Figure 6-14 Displacement Mode Shape Comparison of Experimental Measurement (Top) and Simulation Results (Bottom) at 200 Hz.

6.3. Random Vibration Fatigue Simulation

With the quarter symmetry model validated to produce accurate results through the compliance analysis, mesh convergence studies, and experimental comparisons, simulations for the random vibration tests are performed. These simulations are conducted through PSD spectrum analyses in the frequency domain, which significantly reduces computation time when compared to transient time domain methods.

6.3.1. Spectrum Analysis Setup

The PSD spectrum analysis is performed on the same quarter symmetry model with 2 fully modeled interconnects as the previous modal and harmonic analyses. As the different modes are integrated into the calculations, an initial modal analysis to solve for the first 6 natural frequencies is simulated. These frequencies encompass the critical bandwidth from 1-2000 Hz where most fatigue damage occurs. The damping ratio, ξ, of the system is calculated with Equation 8.88

$$\xi = \frac{\Delta f}{2 f_n} \tag{8}$$

Where Δf is the bandwidth of the half power points at the dominant first natural frequency, f_n. The half power points are determined through Equation 9.

$$V_{\Delta f} = \frac{V_{f_n}}{\sqrt{2}} \tag{9}$$

Where V is the experimental voltage measured by the LDV, which is proportional to the velocity and acceleration. Based on the FFT performed during the experimental phase, the damping ratio is 0.008, indicative of an underdamped system.

An input acceleration PSD base excitation is applied at the pin location based on the measured experimental values. The PSD of the pin is selected instead of the constant

value at the shaker to better reflect actual conditions. A comparison of the simulation input and a two second sample experimental measurement for the second test is displayed in Figure 6-15. The RPSD at each mode is then determined and used to calculate analytical results, which are combined to form the overall solution.

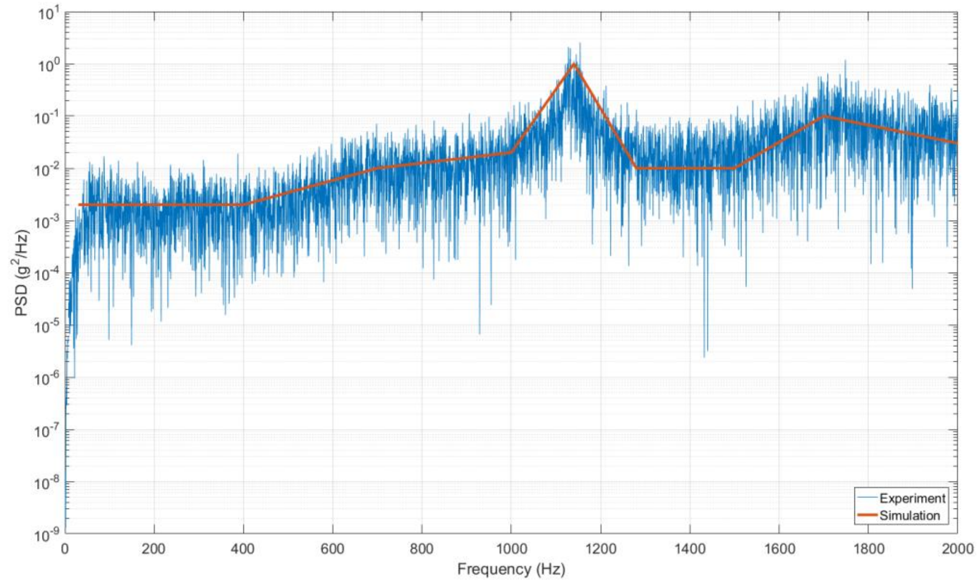


Figure 6-15 Acceleration PSD at Pin of Experiment vs. Simulation

6.3.2. Spectrum Analysis Results and Validation

Due to the inherent probabilistic nature of random vibrations, the input acceleration PSD is statistically based on a Gaussian/normal distribution. This also extends to the output analytical results, which include stresses, strains, and displacements. Therefore, the solutions are provided in one, two, and three sigma forms, each with its own probability of occurrence as explained previously in Chapter 2. The maximum von Mises stress is predicted to be at the corners of the electroplated copper arcuate beam and post, seen in Figure 6-16, and is caused by the geometrical stress concentration. These locations are in

great agreement with the inspected failure sites from the experimental vibration tests. Figure 6-17 provides further validation by comparing the acceleration RPSD at the center of the silicon substrate top surface. Both the magnitude and frequency of the peaks match with the exception of the null at 1000 Hz from the simulation. This discrepancy is caused by the presence of the plate mode from the aluminium mount, which is captured in the experiments, but not reflected in the simulations.

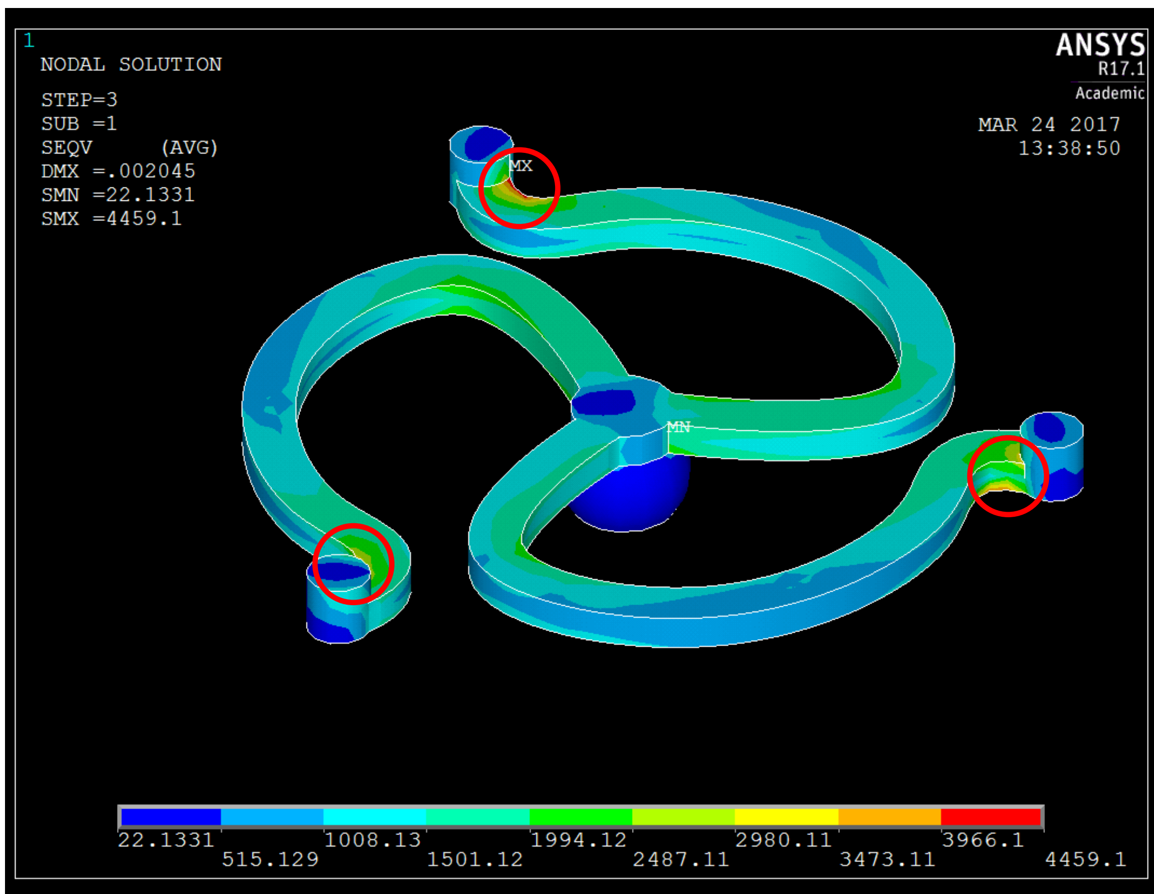
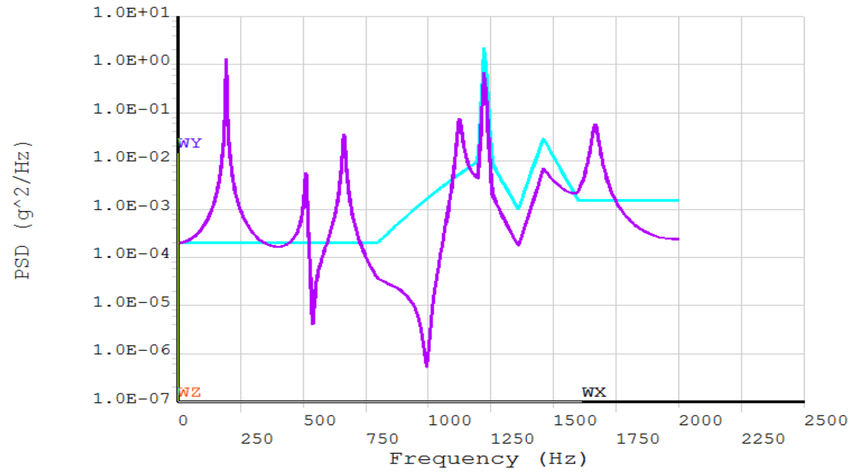


Figure 6-16 Simulation One Sigma von Mises Stress Result of Test Two with Marked Stress Concentrations

BASE
CENTER



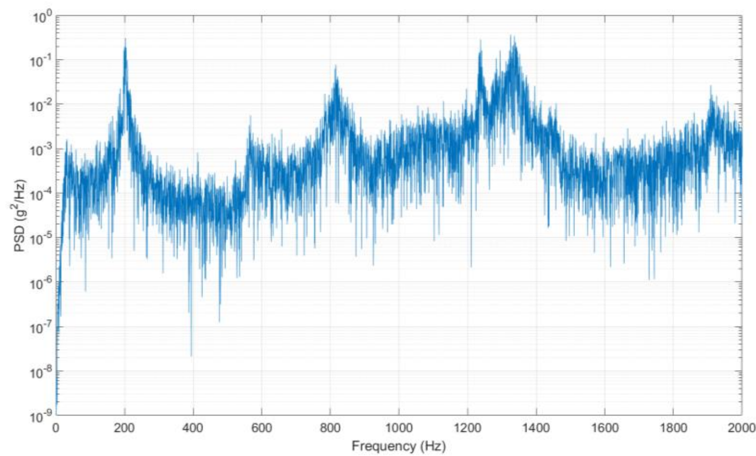


Figure 6-17 RPSD Comparison at Silicon Substrate Center of Simulation (Top) and Experiment (Bottom)

Four PSD spectrum analyses are performed to match the conditions of each experimental random vibration fatigue tests. The main variables are the sample beam width and base acceleration PSD input at the pin. The max RMS von Mises stresses at different sigma levels for each test are listed in Table 6-6 along with their probability of occurrence based on Gaussian PDF. The stress distribution at each sigma level is the same, with only

the magnitude increasing at higher levels. Smaller beam width samples also display slightly higher maximum stresses.

Table 6-6 Simulation Stress Results for Random Vibration Fatigue Tests

	Beam Width (μm)	Input PSD (g^2/Hz)	1σ Stress (MPa)	2σ Stress (MPa)	3σ Stress (MPa)
Test 1	20	0.01	1.27	2.54	3.81
Test 2	20	0.05	4.46	8.92	13.4
Test 3	15	0.05	4.66	9.32	14.0
Test 4	15	0.03	2.48	4.96	7.44
Probability (%)			68.27	27.18	4.28

6.4. Summary

Through the use of simplified equivalent columns as interconnects and transition elements for meshing, the simulation time is significantly reduced from previous iterations. By comparing to the experimental modes, the quarter symmetry model is validated to produce accurate results to reflect testing conditions. A PSD spectrum analysis is selected to simulate random vibration fatigue, which employs a statistical approach as opposed to transient time domain analyses. This not only provides even faster computation times, but also provides insight into the vibration response at different frequencies. The resulting sigma stress results corresponding to the experimental tests will be used to form a preliminary fatigue life prediction model.

CHAPTER 7

DEVELOPMENT OF PRELIMINARY FATIGUE LIFE PREDICTION MODEL

The primary HCF failure location of 3-Arc-Fan interconnects under random vibration loads are on the electroplated copper arcuate beams. The fatigue properties of annealed and cold worked copper are widely available, but less established than structural metals such as steel and titanium. However, electroplated metals are considered porous and are weaker in strength. Therefore, traditional copper fatigue models generally do not offer accurate predictions and separate models for electroplated copper need to be developed.

7.1. Electroplated Copper Fatigue

The most common uses of plated metals are to form protective layers or provide additional properties such as electrical conductivity, heat resistance, or visual appeal. Only in rare instances are these metals used for pure structural purposes. Consequently, fatigue life studies of plated metals are few and far between.

7.1.1. Literature Models

Most of the literature data for electroplated copper fatigue life are based on uniaxial fatigue of copper thin films. The different loading types, mean stresses, surface treatment, and material composition all factor into the prediction when compared with 3-Arc-Fan interconnects. However, fatigue life comparison can still provide valuable insight. Song et al. developed the equation and S-N curve in Figure 7-1 [94], while Murata et al. developed the S-N curve in Figure 7-2 [95]. These two models will be used to form initial predictions.

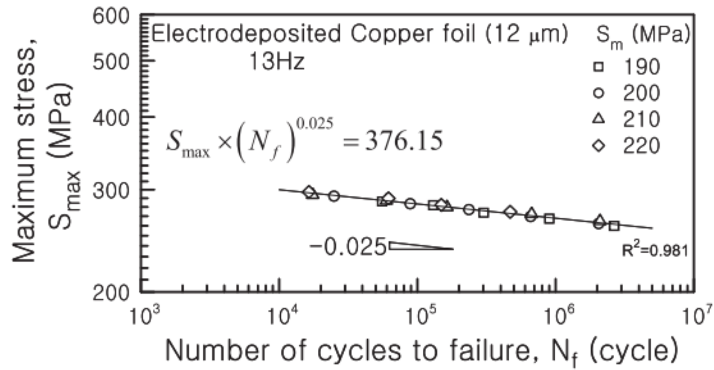


Figure 7-1 Literature Fatigue Model One [94]

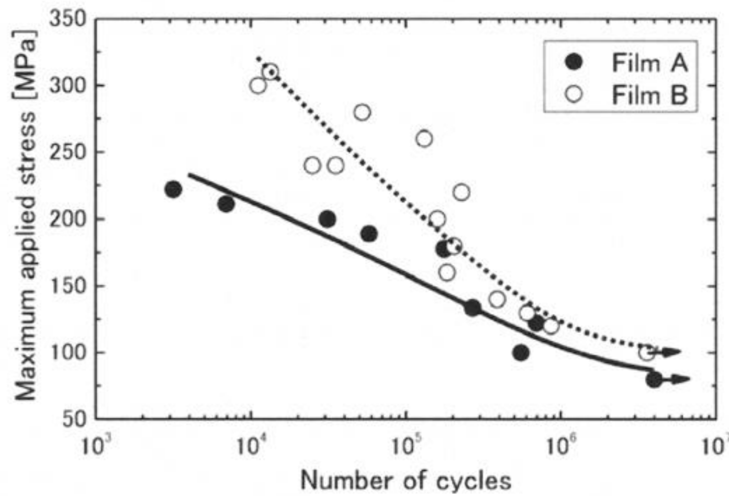


Figure 7-2 Literature Fatigue Model Two [95]

The random vibration fatigue tests are fully reversible, thus, the stress amplitude is equivalent to the maximum stress, and the data in the literature models are applicable. A spectrum analysis simulation with constant acceleration PSD at 1 g^2/Hz for three hours is performed to produce stresses at a comparable level as those in the models. The resulting sigma stresses and actual cycles based on a Gaussian distribution, *n*, are listed in Table 7-1. The cycles to failure, *N*, for each stress level are derived from the literature models. And

Steinberg's 3-band method and Miner's rule are used to calculate the CDI. Based on the CDI, one model shows that very little life has been used, while the other predicts failure. Evidently, a new model is required to accurately predict the fatigue life of the electroplated copper arms in 3-Arc-Fan compliant interconnects.

Table 7-1 Literature Failure Prediction for 3 Hours at 1 PSD

Stress (MPa)		*n* (cycles)	Literature Model 1		Literature Model 2	
			N (cycles)	Damage Ratio	*N* (cycles)	Damage Ratio
1σ	**81.65**	1.47×10^{6}	3.5×10^{26}	4.2×10^{-21}	1×10^{7}	0.147
2σ	**163.3**	5.83×10^{5}	3.1×10^{14}	1.9×10^{-9}	4×10^{5}	1.458
3σ	**244.9**	9.29×10^{4}	2.9×10^{7}	0.003	9×10^{5}	0.103
			CDI	0.003	***CDI***	1.708

7.1.2. 3-Arc-Fan Random Vibration Fatigue Model

By combining the resistance monitoring data from the experimental random vibration tests and the stress data from the PSD spectrum analysis of simulated random vibrations, a preliminary HCF fatigue life prediction model can be developed for 3-Arc-Fan compliant interconnects in the form of an S-N curve as shown in Figure 7-3. The stresses are taken from the probability average of the three distribution levels and the cycles are determined from the resistance measurements and converted at 200 Hz from the dominating natural frequency. As the first sample did not fail, the data point is taken at the fatigue strength cycle of 5×10^{8} for non-ferrous metals.

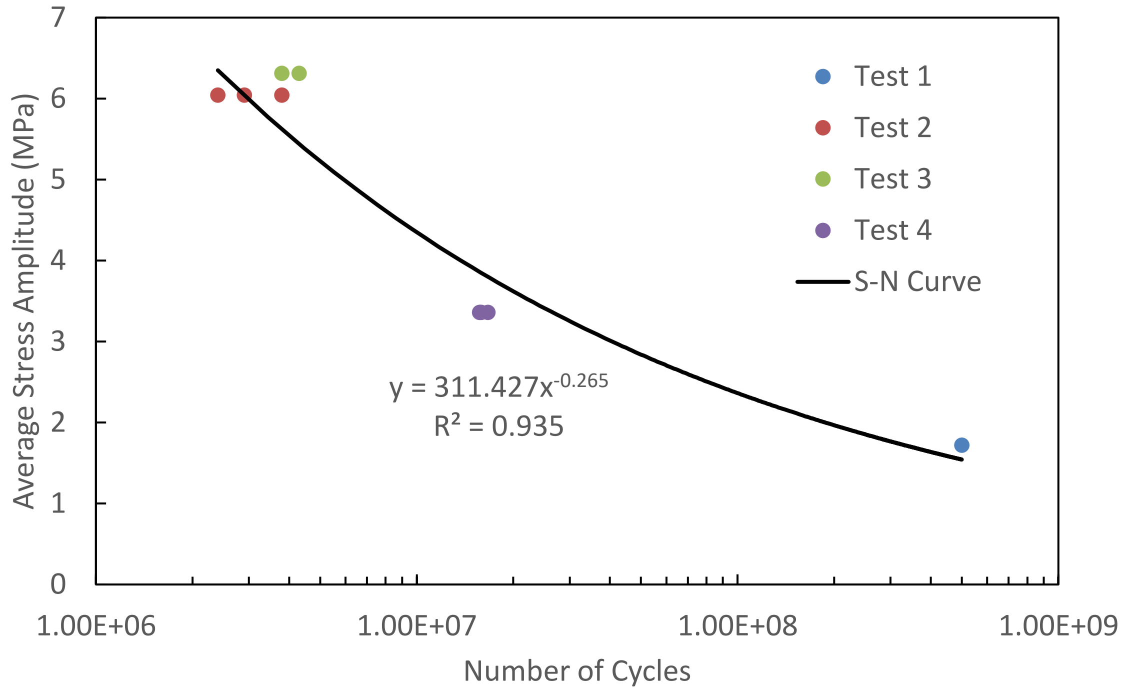


Figure 7-3 S-N Curve for 3-Arc-Fan Interconnects

With these data points, a model based on Basquin's power law is determined using Equation 10.

$$\sigma_a = \sigma_f'(2N_f)^b \quad (10)$$

Where σ_a is the stress amplitude, σ_f' is the fatigue strength coefficient, b is the fatigue strength exponent, and N_f is the number of reversals to failure, where one reversal is equal to a half cycle. From the trendline equation, σ_f' is calculated to be 311 MPa and b is calculated to be -0.265. This model is applicable for the given stress range, but should not be extended to large stresses. In addition, the prediction is based on the 4 × 4 daisy chain and not the individual electroplated copper arms.

7.2. Vibrational Reliability Comparison to Solder

The 3-Arc-Fan compliant interconnect demonstrates increased reliability when compared to vibration tests performed on traditional solder BGAs [67, 82, 84]. This is evident by comparing the developed 3-Arc-Fan S-N curve to a standard SAC solder S-N curve seen in Figure 7-4. Overall, the additional compliance offered by the electroplated copper arms achieve the desired reliability increase.

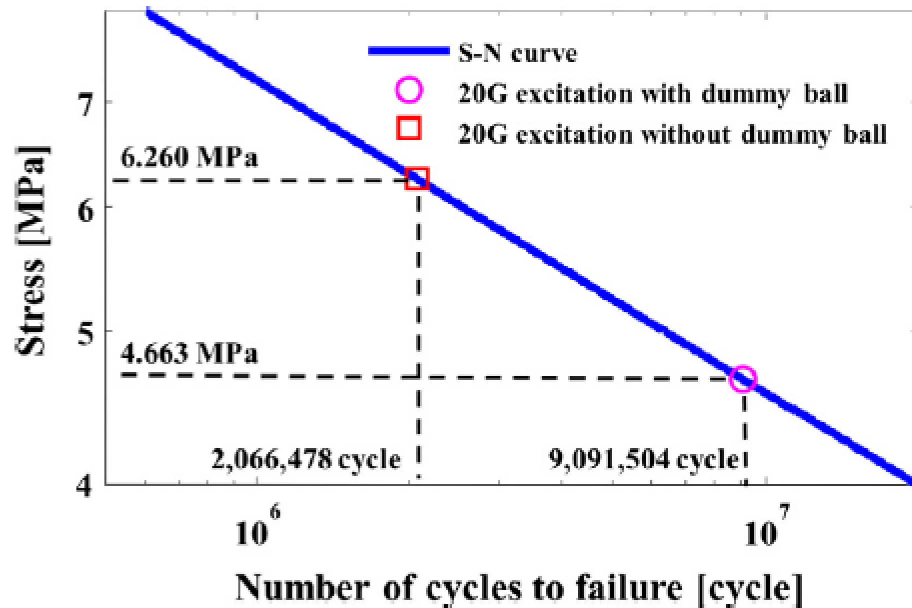


Figure 7-4 Literature S-N Curve of Vibration Fatigue [72]

CHAPTER 8

SUMMARY AND FUTURE WORK

8.1. Summary

Interconnect failure is common in microelectronic packaging due to the difference in material properties and geometry between various components, which induce high stress concentrations at the interconnect areas during application. A potential solution is the replacement of traditional solder BGAs with compliant interconnects that allow for high deformation with minimal stress transfer. One such design is a Second-Level multi-path electroplated 3D structure known as the 3-Arc-Fan compliant interconnect.

However, the increase in mechanical reliability of compliant interconnects introduce trade-offs in the form of electrical performance and cost, and more optimization and testing is required for proof of concept. As thermal cycling and drop testing are already well established, vibration loading is selected to investigate the performance of 3-Arc-Fan interconnects under common random vibration environments.

An optimized assembly process is developed to assemble the interconnects. This TCB profile allows for the formation of reliable and consistent solder bumps. A reflow process is also proven to be viable, which can further reduce the cost of assembly by following industry standard. The assembled 3-Arc-Fan packages are used for testing that characterized the vibration response through mode measurements. A random vibration fatigue environment is selected instead of sine vibration to provide more realistic loads experienced during application. The resistance of the critical corner daisy chains are monitored and the failure times and locations are recorded.

A quarter symmetry FEA model is developed by simplifying the interconnect models into an equivalent column through compliance analysis. This model is validated by conducting modal and harmonic simulations and comparing the vibration response with those measured from the experiments. In addition, a PSD spectrum analysis is performed to simulate the stresses experienced by the 3-Arc-Fan interconnect during random vibration testing. This method allows for faster computation times than transient time domain analysis and incorporates the entire frequency domain to provide accurate results.

From the experiments and simulations, the primary failure location of the 3-Arc-Fan interconnects is identified to be at the electroplated copper arm. Specifically, the area where the arm connects to the annular pad. These failure locations are consistent across each corner and sample, with results from both the tests and FEA in good agreement. From these observations, interconnects with higher compliance are shown to be more reliable. The multi-path structure of the interconnect also demonstrate electrical redundancies, as electrical connection and low resistivity are still maintained even after failure occurs in one arm. Finally, the rotational placement of the interconnect is seen to factor into reliability calculations.

A preliminary fatigue life prediction model is developed for the 3-Arc-Fan packages since existing models do not provide accurate predictions. This model is based on Steinberg's 3-band method on Gaussian distributions, Miner's cumulative damage ratio, and Basquin's power law for HCF. Overall, 3-Arc-Fan compliant interconnects are proven to be more reliable than their traditional solder BGA counterparts.

8.2. Research Contributions

This work has investigated the vibration response of a compliant interconnect and its mechanical reliability. The major research contributions are as follows:

- Developed an optimized TCB assembly profile that produces reliable solder bonds and demonstrated reflow viability.
- Characterized the vibration response for 3-Arc-Fan compliant interconnects through experimental measurements.
- Developed a random vibration fatigue testing methodology that successfully drives components to failure.
- Created and validated a simplified quarter symmetry model through compliance analysis that displayed accurate results when compared to experimental data.
- Performed FEA simulations with PSD spectrum analysis and established a methodology for investigating random vibration fatigue.
- Developed a preliminary fatigue life prediction model for 3D electroplated copper structures under fully reversible high cycle fatigue in vibration environments.
- Demonstrated increased reliability and good electrical performance of 3-Arc-Fan compliant interconnects when compared to solder BGAs.

8.3. Future Work

There are still many different areas of research requiring further investigation that could improve the understanding and design of 3-Arc-Fan compliant interconnects. These are as follows:

- Examine material of the bonding sites between solder and copper, including intermetallic formation and environmental effects.

- Redesign test vehicle with higher quality material and design to reduce assembly interference and improve in-situ resistance monitoring.
- Test reliability of samples assembled under pure reflow conditions and comparison to TCB assembly.
- Perform random vibration fatigue tests of varying input loads on many more samples to refine the preliminary prediction model and develop a comprehensive model suitable for broader usage.
- Test with different loading types such as sine-on-random loading or combined loading in the form of simultaneous thermal and vibration input to simulate actual application environments.
- Optimize rotational orientation of the electroplated copper arms to match vibrational modes and further reduce stress concentrations.
- Perform additional structural optimization to reduce stress concentrations at critical locations. Possibilities include filleting and altering the curvature of arcuate beams.
- Analyze moisture, oxidation, and aging of samples and its effects on the overall life and reliability, and determine whether a surface finish is required and how compliance is affected.
- Optimize interconnects in terms of the relative scale between the solder ball and multi-path structure and determine the effect it has on compliance and reliability. Additionally, scale interconnects to reduce pitch at board level.
- Fabricate samples with different techniques to decrease standoff height discrepancy for more consistency at pure reflow conditions. Then perform overall cost analysis in terms of fabrication and assembly and compare to current industry standards.

APPENDIX A: RANDOM VIBRATION FATIGUE TEST RESISTANCE MONITORING DATA

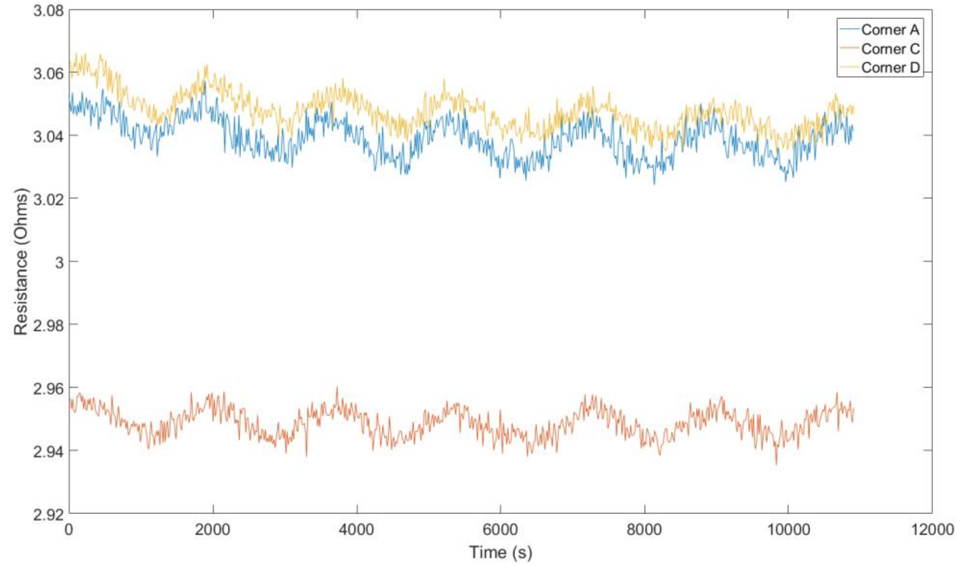


Figure A-1 Sample 1 Trial 1

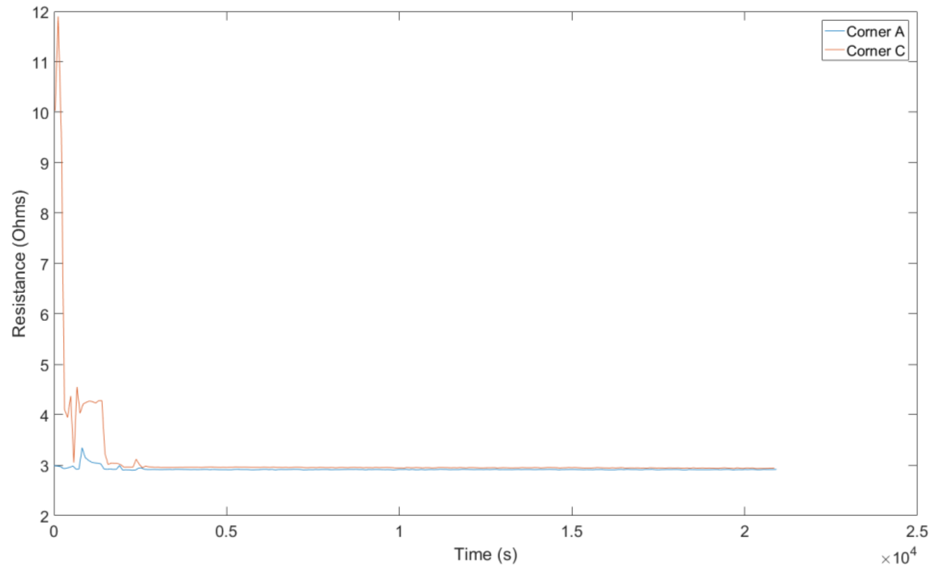


Figure A-2 Sample 1 Trial 2 Corner A and C

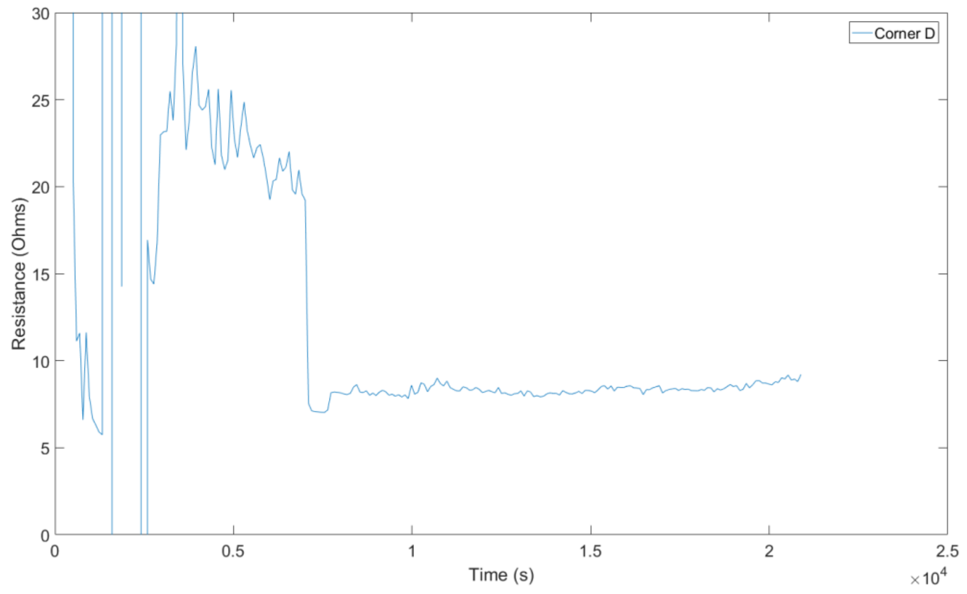


Figure A-3 Sample 1 Trial 2 Corner D

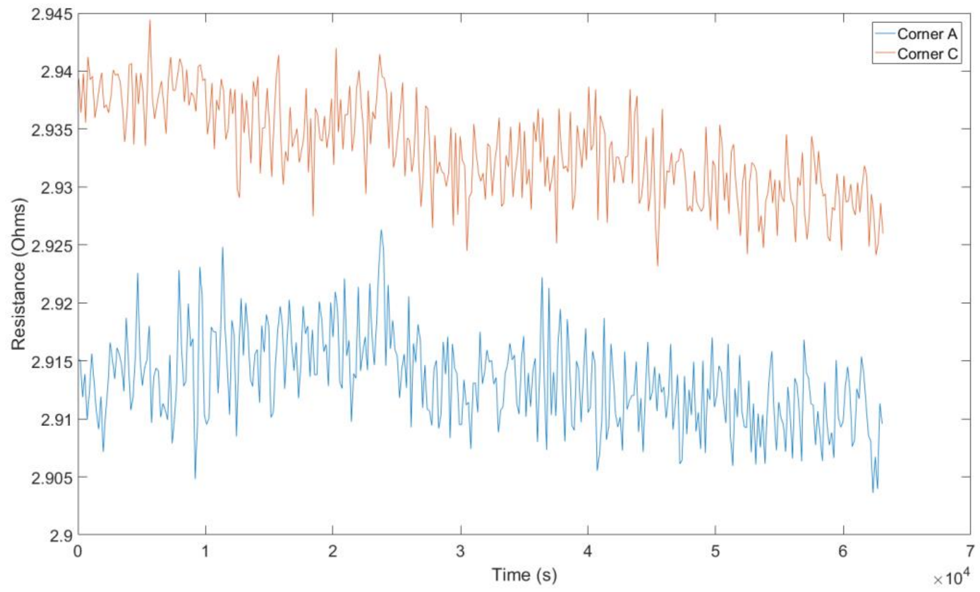


Figure A-4 Sample 1 Trial 3 Corner A and C

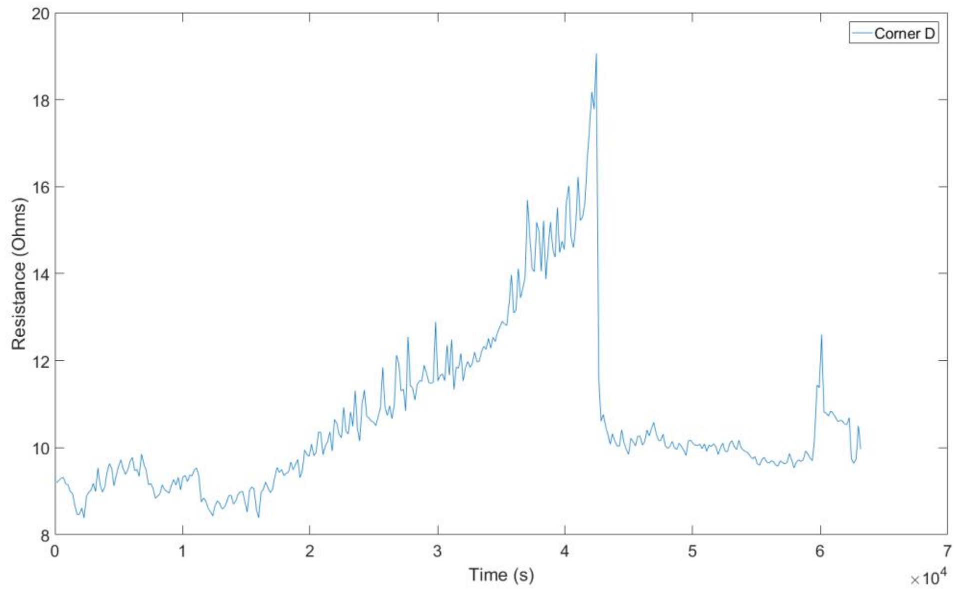


Figure A-5 Sample 1 Trial 3 Corner D

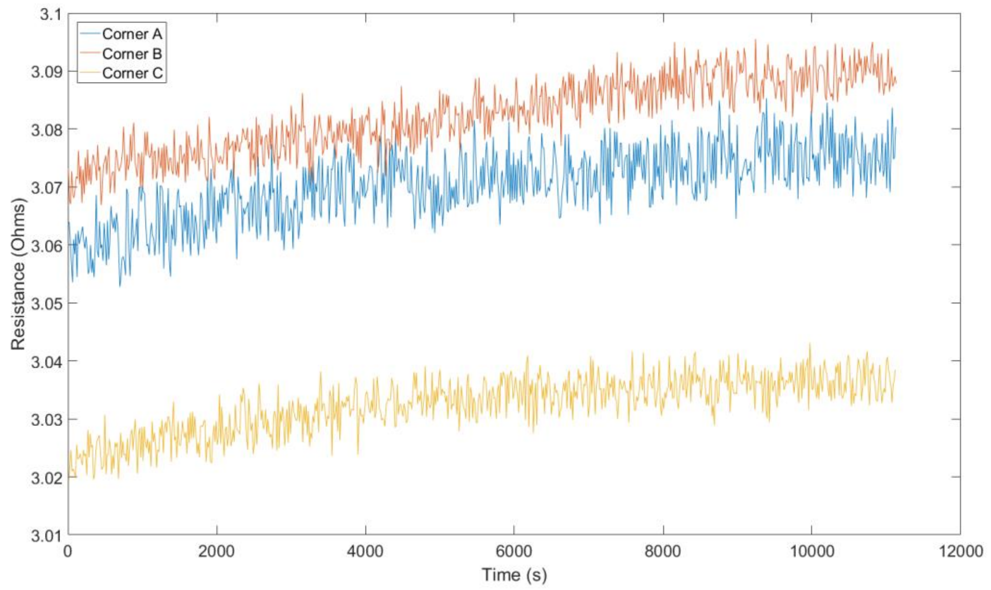


Figure A-6 Sample 2 Trial 1

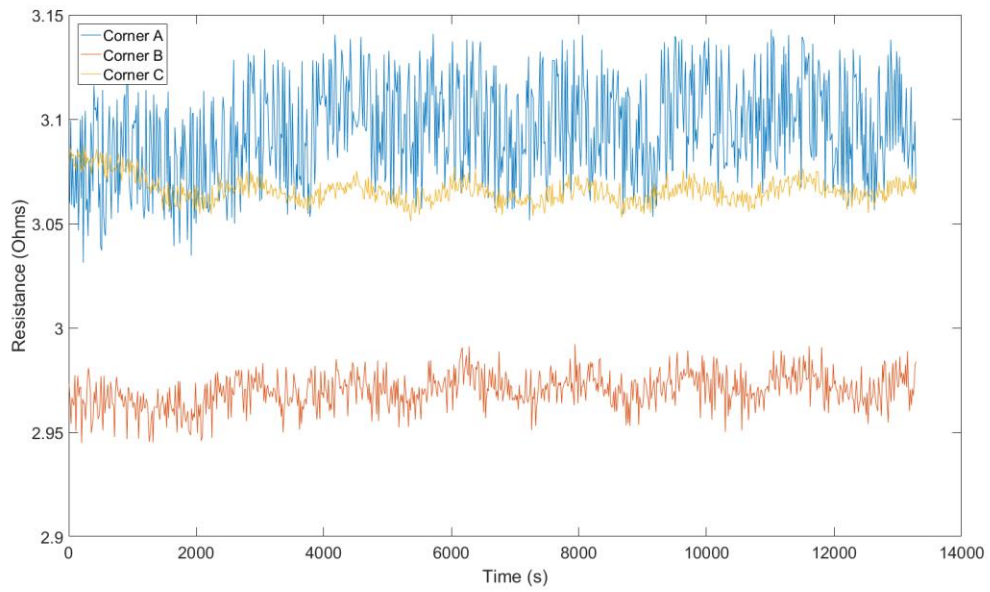


Figure A-7 Sample 2 Trial 2

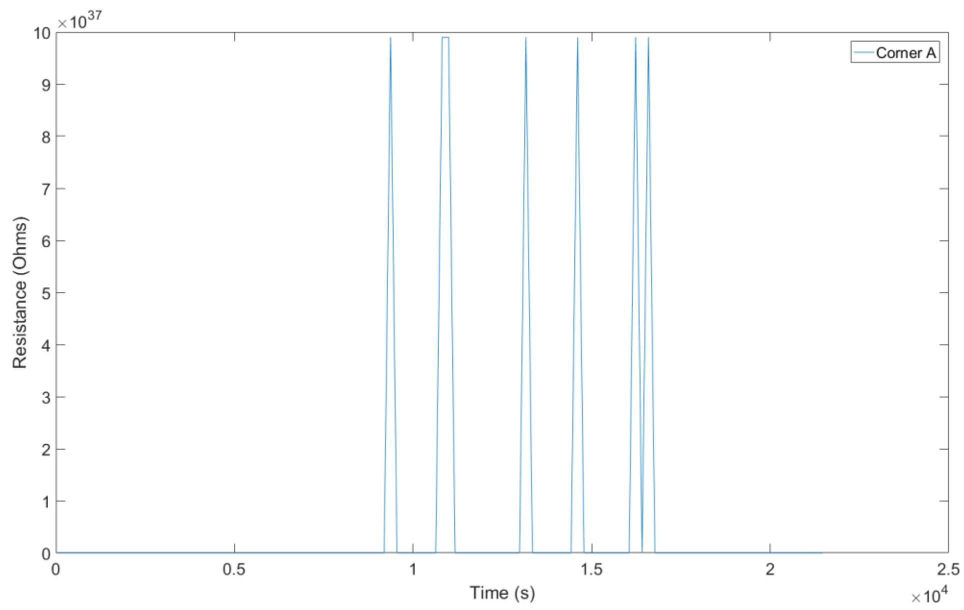


Figure A-8 Sample 2 Trial 3 Corner A

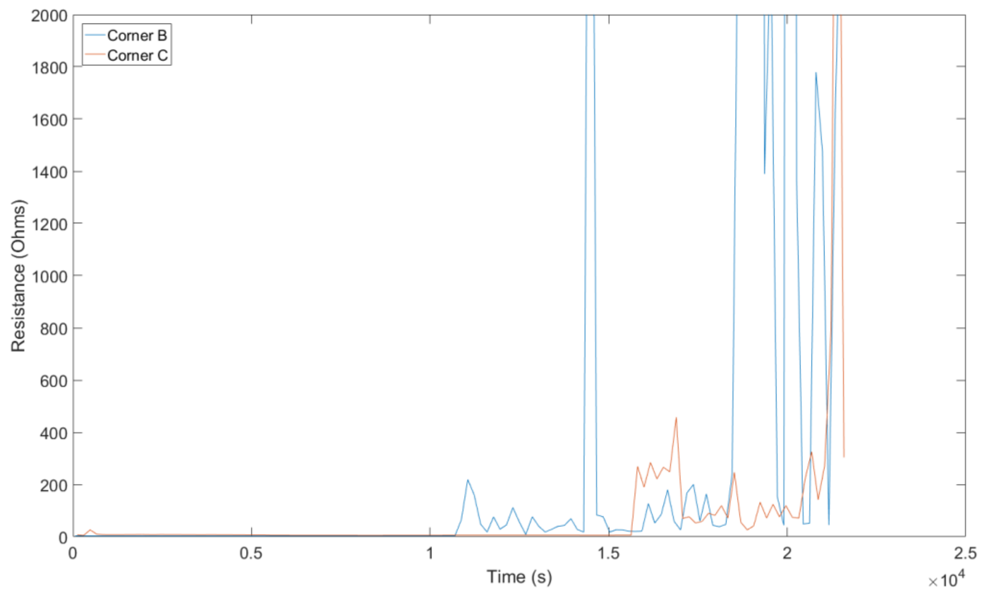


Figure A-9 Sample 2 Trial 3 Corner B and C

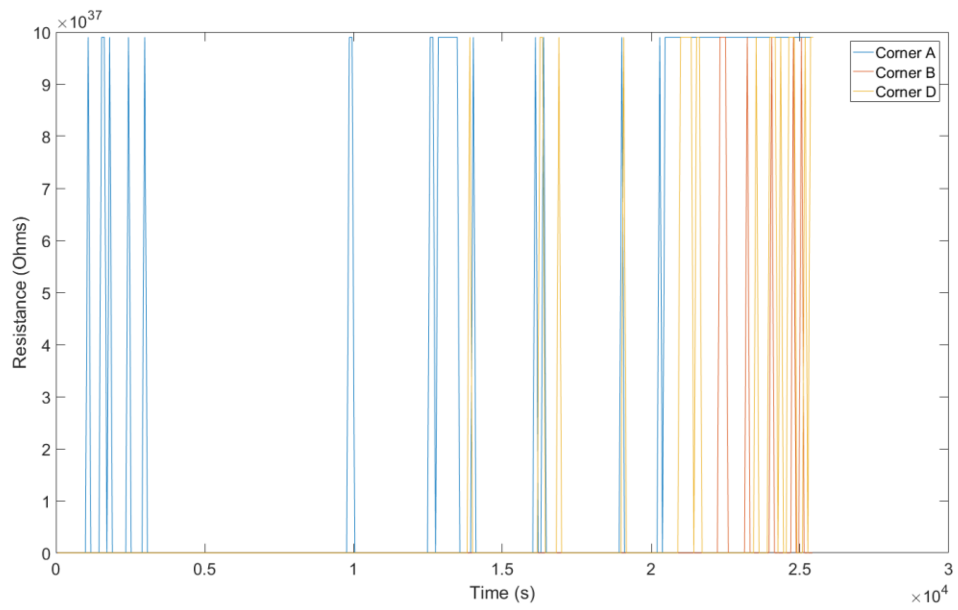


Figure A-10 Sample 3 Trial 1

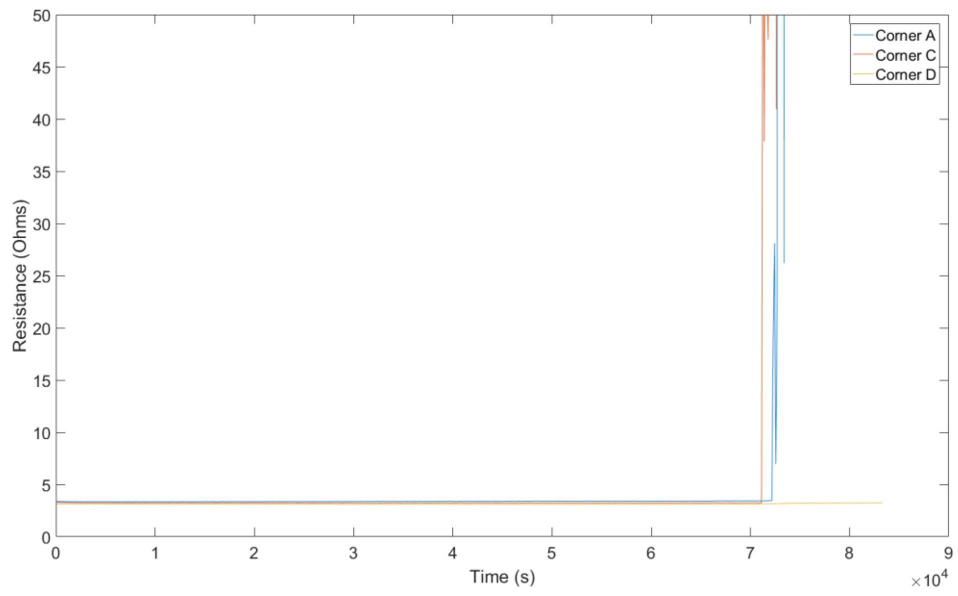


Figure A-11 Sample 4 Trial 1

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