THERMAL ANNEALING AND MECHANICAL CHARACTERIZATION STUDY OF ELECTROPLATED COPPER IN SILICON TRENCHES

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THERMAL ANNEALING AND MECHANICAL CHARACTERIZATION STUDY OF ELECTROPLATED COPPER IN SILICON TRENCHES

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To my parents

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LIST OF SYMBOLS AND ABBREVIATIONS

2.5-D	Two-and-a-half-dimensional
2-D	Two dimensional
3-D	Three dimensional
AFM	Atomic force microscopy
ALD	Atomic layer deposition
CTE	Coefficient of thermal expansion
Cu	Copper
CVD	Chemical vapor deposition
DC	Direct current
DI	Deionized
EBSD	Electron backscatter diffraction
FCC	Face-centered cubic
H	Hardness
I/O	Input/output
IC	Integrated circuit
ICP	Inductively coupled plasma
IPF	Inverse pole figure
OIM	Orientation imaging microscopy
PECVD	Plasma-enhanced chemical vapor deposition
PiP	Package in package
PoP	Package on package
SEM	Scanning electron microscope

Si	Silicon
SiP	System in package
TEM	Transmission electron microscopy
Ti	Titanium
TSV	Through-silicon via
UV	Ultraviolet
W	Tungsten
XRD	X-ray diffraction

SUMMARY

Microelectronic systems continue to move to towards 3-D integration to meet the increasing demands, Through-Silicon Vias (TSVs) play an important role in interconnecting stacked silicon dies. Various 3-D integration technologies have been proposed for microelectronic devices. TSV is the technology that can achieve the ultimate goal of 3-D integration. Although progress is being make in the fabrication of TSVs, experimental and theoretical study of their thermomechanical reliability have been widely studied. There still a gap to understand the copper microstructure in TSVs and similar structure. This work focus on how mechanical properties and microstructure change with thermal aging and thermal annealing in copper-filled TSVs and copper-plated silicon trenches. Both samples are fabricated in the cleanroom. Nano-indentation technique is applied to characterize mechanical properties and Electron backscatter diffraction (EBSD) technique used to characterize copper microstructure. Numerical models are created to simulate the thermo-mechanical stresses of copper with isotropic and anisotropic material property.

CHAPTER 1. INTRODUCTION

1.1 Background

In 1965, Gordon Moore observed that the number of transistors per square inch on integrated circuits (IC) doubles approximately every two years [1]. Academia and industry have followed this empirical assessment for over last 50 years. As IC/transistors keep getting smaller, industry and academia have to deal with the constant miniaturization and rising costs of this technology. Both academia and industry put tremendous amount resources to find a way to keep up with Moore's Law and search for a more cost-effective innovation to continue advances in microelectronics [2-4]. 3-D package integration is one of the innovations that has garnered great interest in recent years.

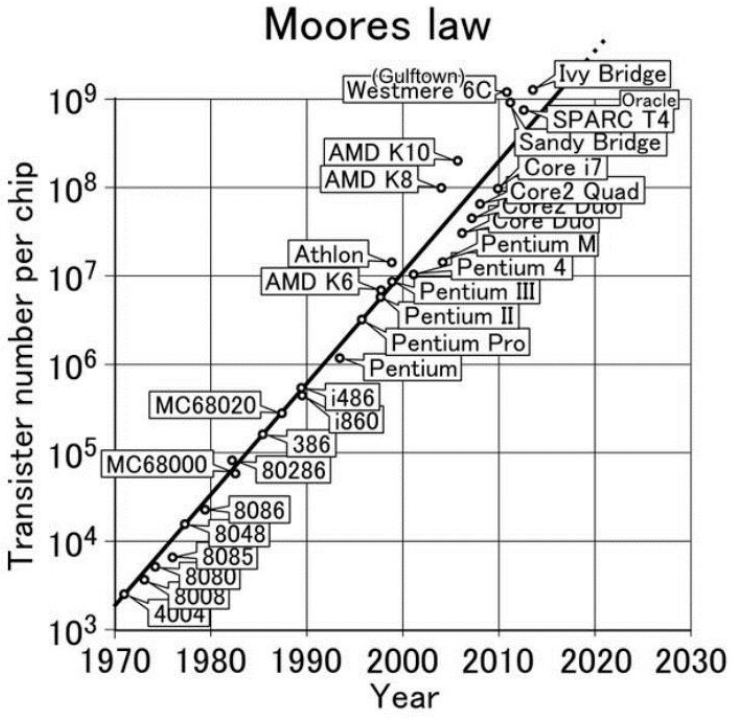


Figure 1.1: Moore's law (Source: Wikimedia)

1.2 Motivation for 3D integrated packaging with TSVs

Microelectronic systems continue to move towards 3-D integration to meet the increasing demands for better performance, more functionality, higher bandwidth, higher I/O density, lower power consumption, and reduced costs [2, 3, 5, 6]. Current IC technology cannot meet these requirements.

Various 3-D integration technologies have been proposed for microelectronic devices. This includes system technologies such as, Package on Package (PoP) (Figure 1.2), System in Package (SiP) (Figure 1.3 and Figure 1.4), 3-D IC integration (Figure 1.5, Figure 1.6 and Figure 1.8), 3D silicon integration (Figure 1.7). All of these technologies are already in production, however, PoP, PiP, and die stack with wire bonds are commonly used, cost-efficient technologies. 3-D stacked die with through-silicon vias (TSVs) (Figure 1.8) and 3-D silicon integration are technologies currently not in high demand due to low yield and high-cost. These technologies are still in the research and development phase to try and solve production yield problems and reduce costs.

Among the various 3-D integration technologies, stacked dies with through-silicon vias provide the highest density and shortest interconnection between different tiers. TSV is the technology that can achieve the ultimate goal of 3-D integration.

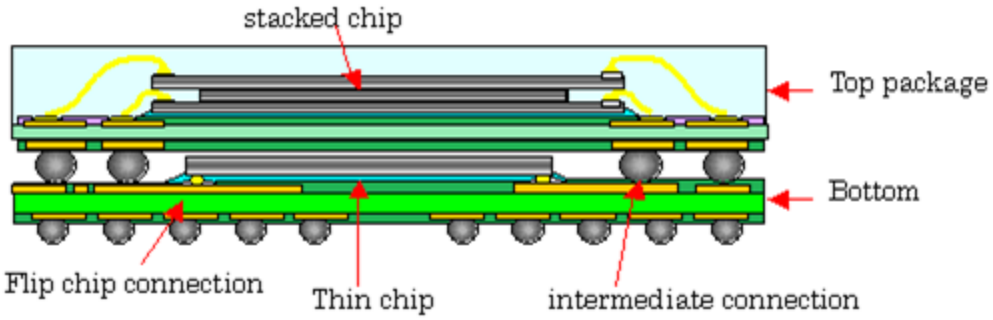


Figure 1.2: Package on package (Source: SHINKO)

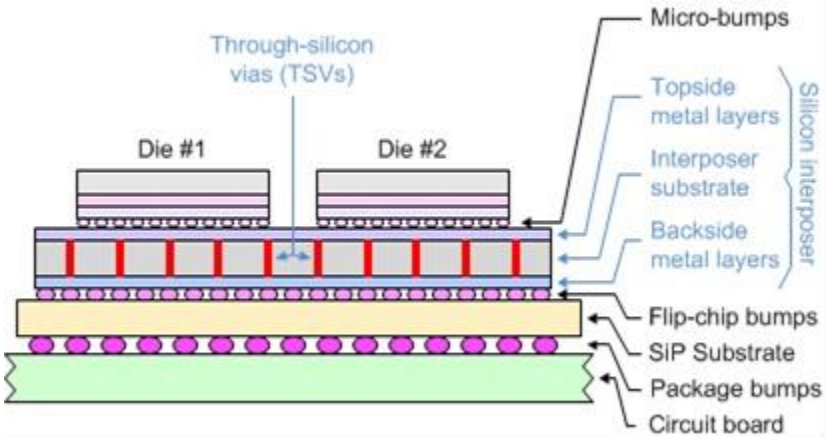


Figure 1.3: 2.5D IC System in package (Source: Clive Maxfield)

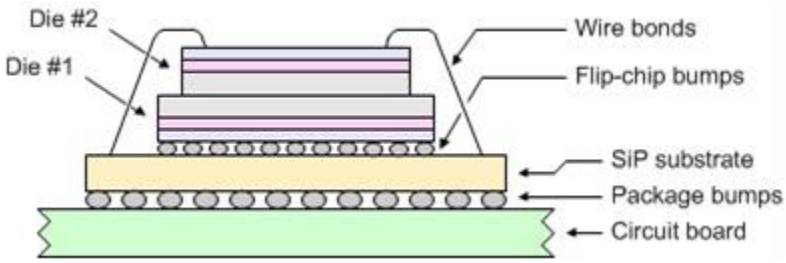


Figure 1.4: 3D IC System in package (Source: Clive Maxfield)

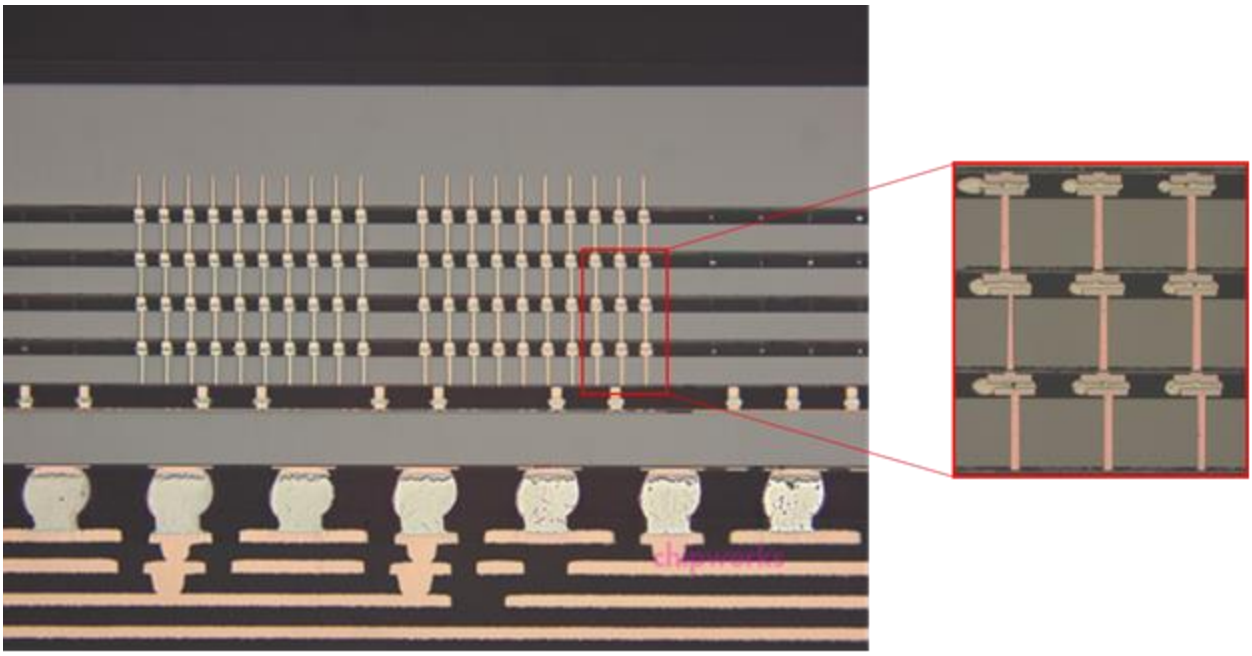


Figure 1.5: Die stack with TSVs (Source: SK Hynix)

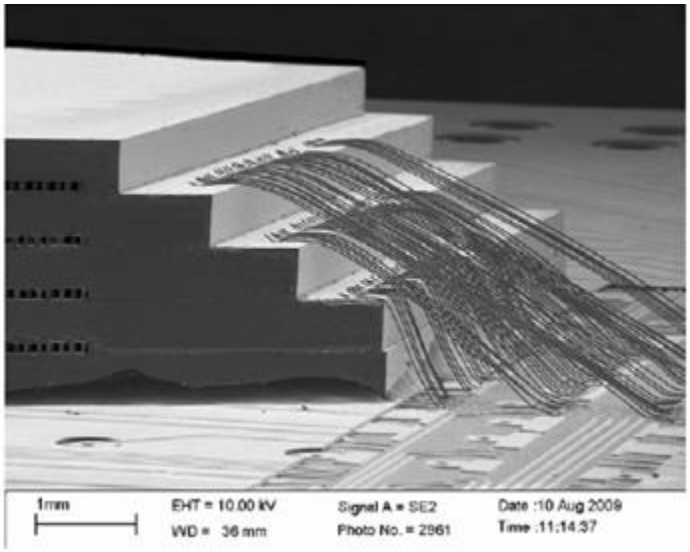


Figure 1.6: Die stack with wire bonds (Sources: ESL)

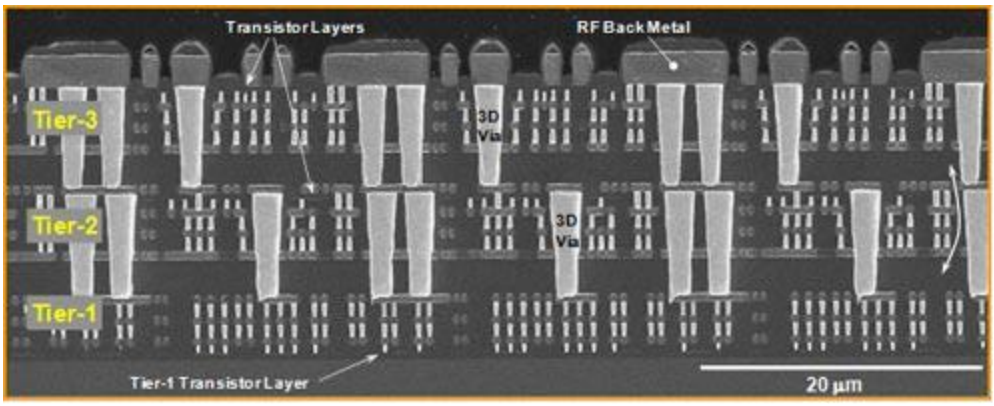


Figure 1.7: 3D silicon integration (Source: MIT)

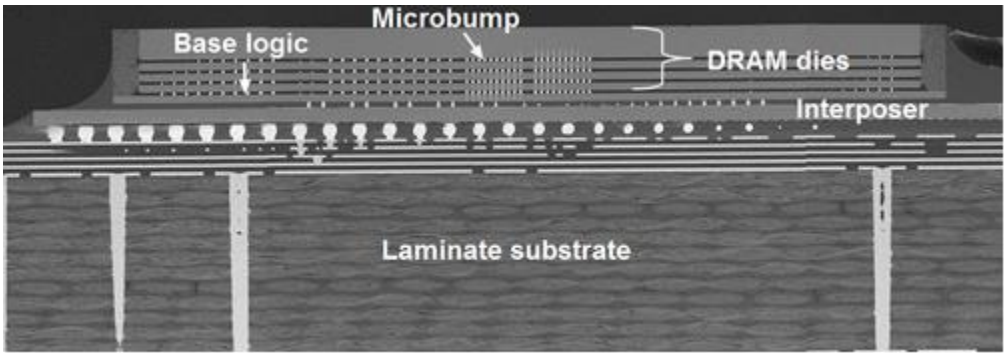


Figure 1.8: Substrate and interposer layer and stacked DRAM of high bandwidth memory (Source: Hynix)

1.3 Through-Silicon Via (TSV)

TSV's are electrical interconnects that are etched into a silicon wafer. It provides vertical electrical paths between the two layers above and below wafer. The vertical through silicon design can provide the highest interconnection density and shortest electrical path between these two layers. There are multiple fabrication methods that have developed during the past few years for TSVs. The most common way to fabricate TSVs is use the Bosch process to etch a hole in the silicon wafer. After this is a wet thermal

oxidation process is used to form a dielectric isolation layer on the surface of the silicon wafer. The last step in the fabrication of TSVs is to electroplate copper to fill up the hole.

1.4 Challenges with TSVs

TSVs are a great solution to meet the customer demand for high-performance, however this technology has numerous challenges. Significant research efforts has been devoted to solve challenges such as fabrication, assembly, thermal management issues, and reliability problems [3-19]. Industry has already introduced 3-D IC products in the market (Figure 1.8). There still are barriers with this technology including cost, process, yield, assembly, reliability and infrastructure that need to be solved.

Reliability of TSVs has garnered a lot of attention. Due to the nature of the materials and structures used in TSVs, there is a high mismatch in the coefficient of thermal expansion (CTE) between the silicon wafer, dielectric layer and metal via. As a result, this can develop large thermo-mechanical stresses during different phases of the manufacturing process and during customer use. (Figure 1.9). These stresses may lead to various reliability issues, such as cohesive cracking (Figure 1.10), interfacial separation, and warpage. The large amount of silicon in the 2.5-D and 3-D packages introduces new challenges in the reliability of TSVs. This is because multilayer assemblies may induce residual stresses that complicate the TSV reliability analysis.

Copper is the most common material to fill TSVs. Material properties are the key to predict the CTE mismatch induced stresses in the TSV structure. Copper is a face-centered cubic (FCC) crystal structure and it is an isometric crystal system. As the TSV size shrinks, the commonly used isotropic copper material property shows its shortcoming.

To have more precision prediction, copper anisotropic material properties need to be considered.

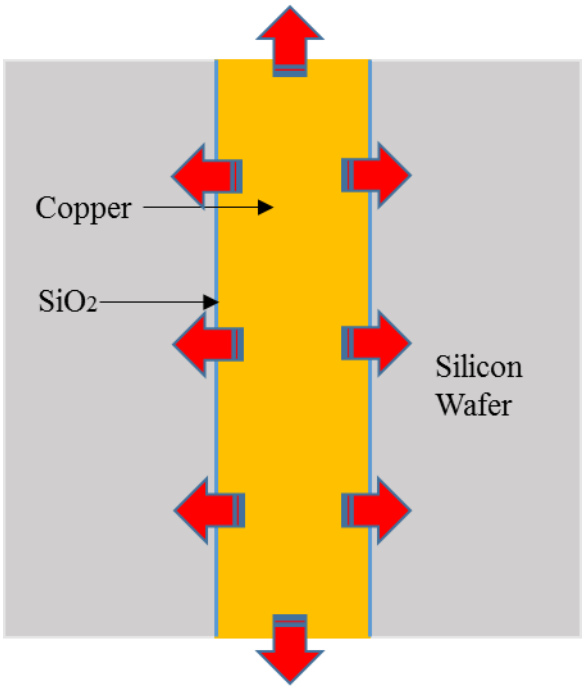


Figure 1.9: CTE mismatch induced stress in TSV structure

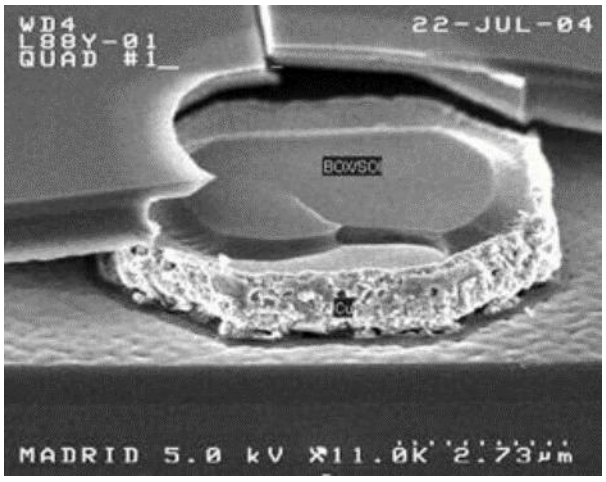


Figure 1.10: CTE mismatch induced dielectric cracking (Source: Tezzaron)

CHAPTER 2. LITERATURE REVIEW

Industry and academia have put tremendous resources into the development and improvement of copper-filled TSV fabrication processes and reliability issues [3, 8, 13, 14, 17, 20-24]. Different fabrication methods have been developed and optimized to obtain TSV interconnects. The electrical performance and mechanical reliability issues of TSVs have been studied using different methods.

2.1 TSV fabrication method

Fabricating TSV interconnects successfully is a challenging task. Different fabrication methods have been proposed and implemented in the past few years. The two main steps to fabricate TSV interconnects are the drilling process and via filling technique. These two techniques will be discussed in the following sections.

2.1.1 Silicon Drilling technique

There are two common methods to etch silicon via, including a laser drilling technology and a deep reactive ion etching technology.

TSV interconnects are initially created using laser ablation. This process is cost-effective when a small number of vias are present in a chip. Laser drilling is a single-point operation, and the surface condition of the laser drilled vias is very rough. The excessive heat from laser drilling can damage the surrounding crystalline silicon and recast debris around the hole. As industry pushed for high density vias and high aspect ratio vias,

concerns for damage and defects in the vias was an issue. Hence, deep reactive ion etch technology was introduced [25, 26].

Deep reactive ion etch technology is also known as the Bosch dry-etching process. The bosch dry-etching process uses a photoresist mask that can etch many vias at the same time as opposed to the laser ablation process which only drills one via at a time. Dimensions of vias are dependent on the mask design of the via geometry. The bosch dry-etching process is the most commonly used technology to form TSV holes currently due to its excellent process controllability, its capability to create high aspect ratio vias, and its ability to adopt sidewall profiles and topographies [25, 26].

2.1.2 Via fill technique

The filling material selection is crucial for TSVs in 3-D integration technology. The most common materials for TSV filling are poly-Si, tungsten (W) and copper (Cu). Depending on the material used, different TSV filling techniques should be applied accordingly.

Low resistive poly-Si is a stable material and affects the device characteristics less than other materials such as copper and tungsten. However, the resistance of low resistive poly-Si is much higher than tungsten and copper. The coefficient of thermal expansion (CTE) of tungsten is 4.4ppm/K compared to that of copper which is 17 ppm/K. In addition, the CTE of silicon is 2.3 ppm/K. The CTE mismatch is much smaller between tungsten and silicon compare to that of copper and silicon. The advantage of tungsten over copper is balanced by its brittleness and lack of plasticity in deformation. The copper has the highest electrical conductivity amongst the three materials. In addition copper has a well-

known electroplating technique, a higher electro-migration resistance and a higher current-carrying capacity than tungsten which is why it is the mainstream approach today [26].

Different methods are proposed to fill up vias including filling up vias using conductive paste, chemical vapor deposition (CVD) of copper in vias, CVD and electroplating of copper in vias. Filling up vias with conductive paste has been proposed because the paste shows excellent filling characteristics for low to medium via densities. This method has a shorter turnaround time and lower machine cost compared with electroplating and metal CVD. However, this approach is restricted to TSVs aspect ratios up to1.8 [17, 27]. CVD are mostly used to produce thin films. There have been some studies that have used CVD to fill up vias. The CVD method works well for small TSV diameters in the range up to 3 μm, especially at high aspect ratios. The precursor cost and relatively long processing time limits the application of the CVD method. The electroplating method is the most common approach used to fill up TSVs. It is known to be the fastest, least complex and more stable approach to deposit metal. Also, electroplating requires less costly equipment than CVD, and the processes are more easily controlled and maintained. Electroplating is applicable over a wide range of features. The dimension size available varies from hundreds of microns to tens of microns and the aspect ratio of the vias can be up to 20. However, proper optimization of chemistries in combination with reactor design and process parameters need to be calibrated for different via sizes and aspect ratios [28]. By comparing all via filling methods, electroplating is the most applicable and low cost solution available currently.

2.2 TSV reliability study

Copper TSVs have been fabricated successfully after numerous research efforts and industry input into this technology. Before copper TSVs goes through large volume production, its mechanical reliability issues need to be understood. Due to the large CTE mismatch between silicon and copper, the thermo-mechanical stresses in the TSV needs to be analyzed. Warpage issues, copper protrusion, interfacial delamination and cohesive cracking in TSVs has already been studied [11, 20, 21, 29-38]. The thermo-mechanical stresses have played an important role in addressing mechanical reliability issues. Copper material properties such as strength, hardness, elastic modulus and CTE can be strongly influenced by the copper's microstructure. Mechanical and material properties of electroplated copper play a critical role to achieve good mechanical and electrical system level performance [39]. Copper microstructures properties such as grain size, texture, and grain size distributions have been reported to have a huge influence on the TSVs electrical resistivity and reliability. However, there have limited studies that have been done on copper microstructure properties in TSVs [39-46]. Limited work has been done on the thermal aging effects on the copper microstructure of TSVs and the microstructure evolution.

Various experimental techniques have been applied to study the stresses and strains developed in TSVs including synchrotron x-ray diffraction (XRD), micro-Raman spectroscopy, beam bending technique and piezo stress sensor measurements of TSV [33-36]. Other tools have been developed to measure copper protrusion in TSVs including profilometer, confocal microscope, atomic force microscopy (AFM), and scanning electron

microscope (SEM) [37, 38]. All of these studies have been done on TSVs and silicon layers found in wafer level packages

After copper-filled TSVs are fabricated, TSVs then go through an annealing process to reduce the residual stress in the structure and prevent copper pumping and associated reliability issues in subsequent thermal excursions. However, there are limited studies that have addressed how the copper microstructure changes after thermally annealing the TSVs and how this affects thermo-mechanical stresses in the structure as well as reliability and mechanical properties of the TSVs.

2.2.1 Copper mechanical properties

Hardness and elastic modulus are critical material properties required to characterize a material. There have multiple ways to characterize hardness and elastic modulus. Different characterization methods are reviewed to find the best fit for this study.

Hardness is defined as the resistance of metal to plastic deformation. Scratch, rebound and indentation are three general experiment methods to get hardness value for metal materials. Table 2.1 shows the comparison between different hardness test methods. Scratch hardness test is when an object made of a harder material will scratch an object made of a softer material. The limitation of this method is that it requires considerable experience and some skill by operators to ensure that sensible results are obtained. Scratch test equipment also requires that the sample has hard coatings on softer substrates, (e.g. ceramic coatings onto metallic substrate) which doesn't work for copper on silicon substrates [47]. Also, it is not applicable to micron level scale samples. The rebound method is essentially a dynamic indentation test. A diamond-tipped hammer is dropped

from a fixed height onto the surface of the material. The height of the hammer rebound is a measure of the material hardness[48]. The rebound method usually used to test concrete. However, it is not applicable to materials used in microelectronic devices. The indentation method uses a hard tip with mechanical properties that are known. This hard tip is pressed into the sample being tested. The applied load and indenter displacement are monitored until it reaches a user-defined value. At this point, the load may be held constant for a period of time or removed. The load-displacement curve obtained is the important material characteristic in indentation which will used to calculate hardness and elastic modulus [48-52].

Table 2.1: Comparison between different hardness test methods

Characteristics	Scratch test	Rebound test	Indentation test
Total test load	High	High	Low
Accuracy	Low	Low	High
Economic aspects	Low cost	Low cost	Expensive
Applicable for micron level sample	No	No	Yes

Elastic modulus is a number that measures a materials ability to deform elastically when a force is applied to it. Tensile test, frequency response, bending test and indentation are the four most popular methods used to determine a material's elastic modulus. Table 2.2 shows the comparison between different elastic modulus test methods. Tensile test,

bending test and indentation are static test method and frequency response is a dynamic test method. The procedure used will depend on the intended material application. [53]. Due to the dimension and geometry of copper-filled TSVs and copper-plated silicon trenches, however, a tensile test, frequency response and bending test are not applicable.

Table 2.2: Comparison between different elastic modulus test methods

Characteristics	Tensile test	Bending test	Frequency response test	Indentation
Accuracy	High	High	High	Ultra-high
Economic aspects	Low cost	Low cost	Low cost	High cost
Applicable for micron level sample	No	No	No	Yes

Indentation techniques work on the principle of analyzing the residual-stress-induced normal load to measure localized stress in copper [34]. The indentation test is divided into two categories based on the load applied including macro-indentation and micro-indentation / nano-indentation. Macro-indentation is applied to tests with a larger test load, such as a 1 kilogram-force (Kgf) or more. Micro-indentation and nano-indentation refers to an applied force less than a 1000 gram-force (gf). Due to the nature of the sample, copper-filled TSVs and copper-plated silicon trenches are considered to be a thin film. Nano-indentation for measuring thin film mechanical properties is probably the

most popular method used currently [49, 50, 54]. However, nano-indentation also has some limitations, particularly in materials that pile-up [55-57]. The basic assumption for indentation is that the contact periphery sinks in without any pile-up of material. It is in a manner that can be described by models for indentation of a flat elastic half-space by rigid punches of simple geometry [58-62]. In most indentation experiments, the pile-up effect is negligible [49]. Prior efforts in copper-filled TSVs and thin-film hardness and elastic modulus measurements for understanding the mechanical properties in this structure have been done in several studies [39, 42, 44, 45, 63, 64]. The well-established technique and procedure in hardness and elastic modulus measurement of thin-film structures is by using a nano-indentation. This method provides the most accurate results.

2.2.2 Copper microstructure

The microstructure of a material can strongly influence physical properties such as hardness, elastic modulus, tensile strength and electrical resistance. These properties in turn govern the application of copper. Copper has a high thermal and electrical resistance and low electron migration properties that subsequently make it a good candidate as interconnect material. Electron microscopy and x-ray diffraction (XRD) are the most common techniques to characterize metal microstructure. An electron microscopy technique usually uses transmission electron microscopy (TEM), and scanning electron microscopy (SEM) with electron backscatter diffraction (EBSD) detector to characterize material microstructures. TEM technique includes a beam of electrons transmitted through an ultra-thin specimen, interacting with the specimen as it passes through it. The resolution for TEM can be as low as 0.004nm, which is much smaller than the diameter of an atom and with really good magnification up to 5,000,000x [65]. Luhua and other researchers

have used TEM to characterize the copper microstructure in TSV and other thin film structure from different perspectives [39, 44, 66-69]. A major limitation of the TEM is we need thin specimens due to the requirements of a TEM. The thinning processes does affect the specimens, changing both their structure and chemistry. The images from TEM are in black and white. However, TEM is ultra-expensive and hard get access [65]. EBSD is an additional characterization technique in SEM, which can characterize individual grain orientations, local texture, point-to-point orientation correlations, and phase identification and distributions on the surface of the material. The wide availability of SEMs, the ease of sample preparation, the high speed of data acquisition, and the access to complementary information about the microstructure on a submicron scale make EBSD the most popular microstructure technique used [70]. Okoro and other researchers have used the EBSD technique to characterize the copper microstructure in TSVs and other copper thin film structures [40-43, 45]. The limitations of the EBSD technique are worse spatial resolution, inability to image individual dislocations and microstructure defects [71]. XRD is a rapid analytical technique used for phase identification of a crystalline material. It is based on constructive interference of monochromatic x-rays and a crystalline sample. The electrons accelerating to dislodge inner shell electrons in the material, generate characteristic x-ray spectra. The specific wavelengths are characteristic of the material being tested [72]. XRD is mostly used for determining lattice mismatch between film and substrates, in inferring stress and strain, and dislocation density and quality of the film of thin film samples. The limitation of XRD is that it must have access to a standard reference file of inorganic compounds (d-spacings, hlks) and peak overlay may occur for high angle reflections. Table

2.3 compares three different microstructure characterization methods. SEM-EBSD method turns out to be the most suitable technique for this study.

Table 2.3: Comparison between different microstructure characterize methods

Characteristics	TEM	SEM-EBSD	XRD
Sample size requirement	Thin foils	Bulk	Bulk
Working area	Small areas	Large areas	large
Sample preparation	Extremely hard	Easier than TEM	Easiest
Data acquisition and analysis	Slow	Rapid and automated	Ultra-rapid
Spatial resolution	Ultra-high	Less than TEM	N/A
Localize accuracy	High	High	Low
Accessibility	Hard get access	Very common	Widely available
Economic aspects	Extremely expensive	Less expensive than TEM	Cost effective

Normally at room-temperature, copper is electroplated to fill the silicon via. After copper TSV fabrication, there are subsequent steps that copper TSVs will go through that will expose them to higher temperature, such as flip-chip bonding and solder reflow. Due to exposure at high temperatures copper material properties will change. There have been several studies that have looked into the annealing effect of copper for as-plated TSVs by using the EBSD method [40-43, 45]. There have also been several studies that compare the annealing effect of the copper microstructure with different samples. The texture of copper analyzed in random in general. The grain orientations when compared before and after annealing show no preferable orientation that exist by inverse pole figure (IPF) mapping. Comparing different samples cannot eliminate sample to sample variation [41-43, 45]. Some studies compare the grain size change before and after annealing treatment. These studies didn't take twin boundaries into consideration. One grain might contain multiple twins. "Twin boundaries have emerged as the second most important interface in materials science, after grain boundaries," says Lawrence Livermore materials scientist Morris Wang. "They can affect many fundamental applications and projects." Electron transmission is much easier through twin boundaries than grain boundaries. Grain size comparison needs to take twins into consideration in copper TSVs. Hardness and elastic modulus are obtained and compared from an indentation test. A general trend shows that for high temperature annealing there is a decreases in hardness and elastic modulus [45].

2.2.3 Numerical study

There have various numerical studies of copper-filled TSV that have done by other researchers. Copper protrusion, the effect of void in copper, and fracture analysis, including cohesive and interfacial cracks have been modeled [11, 20, 30-32, 42, 43, 73-75].

Numerical fracture models have been developed to analysis the fundamental cause of different failure mechanisms by Liu [11, 20, 31, 32, 75]. Numerical models have also been developed for the warpage issue of 3-D packages interconnected with TSVs by Liu [29-31]. These studies help understand the reliability issue of copper-filled TSVs under different thermal and mechanical loads. However, there is limited work about the microstructure of copper.

Most of the copper-filled TSV modeling is based on copper as a pure isotropic material. Many materials show isotropic material properties on a macroscopic scale. In a polycrystalline material like copper, anisotropy is statistically averaged and approximately isotropic properties can be assumed. This assumption is acceptable under several requirements; when the grains are small in comparison to the examined part. If only a few grains are present in the component, isotropy cannot be assumed, because an adequate averaging does not occur [76]. Real materials are never perfectly isotropic. As the TSV size keeps shrinking, the macroscopic material behavior cannot be verified and assumed. Saettler found out that assuming copper bulk modulus for finite element method calculations will become a critical source of error for TSV diameters smaller than 10 μm [76]. Jiang and Wu have studied the copper grain microstructure on TSV extrusion [77-79]. Since there are different copper fill up techniques, the copper texture might vary from sample to sample because of a lack of experimental work done on copper-filled TSVs. There are only a few studies that show the anisotropic modeling of the thermomechanical behavior in copper-filled TSVs.

CHAPTER 3. OBJECTIVES AND APPROACH

3.1 Introduction

There are many studies that have been done towards the development and improvement of copper-filled TSV fabrication processes and reliability issues [3, 8, 13, 14, 17, 20-24]. In reliability studies of copper-filled TSVs, the primary focus has been on thermal cycling and thermal-shock induced high thermo-mechanical stresses that cause copper protrusion, interfacial delamination, cohesive cracks and warpage issues [6, 10, 24, 32, 33, 35, 37, 38, 43, 64, 66, 75, 80, 81]. Limited studies have been done on thermal aging effects in copper-filled TSVs [45, 82, 83]. There are a lack of studies on the copper microstructure after long-term aging. Also, there have been limited studies on copper microstructure evolution after its have been plated. Therefore, there is a need to fabricate and determine how mechanical properties and microstructure change with thermal aging and thermal annealing.

3.2 Objectives and Approach

The primary objective of this work is to understand copper misconstrue evolution in copper-filled TSVs and copper-plated silicon trenches. This work focuses on experimentally analyzing copper mechanical properties and microstructure in copper-filled TSVs and copper-plated silicon trenches to gain a fundamental understanding into thermal annealing effect on copper microstructure. Numerical models have also been developed to study the thermo-mechanical behavior of copper-filled TSVs with anisotropic material properties.

To approach this goal, the copper-filled TSVs and copper-plated silicon trenches in free-standing wafers have been fabricated in the cleanroom by using the standard lithography process followed by dry etching and electroplating copper to fill the hole. Fabrication processes and parameters will be optimized to achieve high yield and high quality.

Nano-indentation technique is applied to characterize mechanical properties, such as hardness and elastic modulus of both copper-filled TSVs and copper-plated silicon trenches. Copper-filled TSVs are tested after one-year room temperature aging and after each pre-set thermal annealing treatment intervals. Copper-plated silicon trenches are tested right after plating and after each pre-set thermal annealing interval. A continuous stiffness measurement method will be used for data acquisition. Comparing the mechanical properties for all the conditions will be evaluated to understand the copper property evolution.

Electron backscatter diffraction (EBSD) technique will be used to characterize copper microstructure in both copper-filled TSVs and copper-plated silicon trenches. EBSD measurements have been taken after each regular pre-determined thermal annealing intervals. The inverse pole figure (IPF) map shows the grain orientation and the unique grain map shows the different grains that will be used to analysis the copper microstructure evolution at regular pre-determined intervals. An evolution metric will be used to determine the actual change in the copper microstructure.

Numerical models are created to simulate the thermomechanical stresses of copper with isotropic and anisotropic material property models. Comparing how different copper

material properties effect the thermo-mechanical stresses and associated reliability issues will be studied.

3.3 Outline of the Thesis

This thesis is organized as follows:

CHAPTER 1 briefly introduces the background of this work. Provides an introduction to TSVs and motivation for this work.

CHAPTER 2 talks about existing research studies that have been done on TSVs. Gaps and challenges of existing studies and the scope of this work.

CHAPTER 3 presents the objective and approach of this work.

CHAPTER 4 presents the process of fabricating copper-filled TSVs and copper-plated silicon trenches on free-standing wafers. Fabrication optimization and yield analysis is also discussed.

CHAPTER 5 discusses the mechanical properties and microstructure characterization of one-year aged copper-filled TSV samples. Nano-indentation and EBSD test is conducted on the test samples before and after regular pre-determined thermal annealing treatment intervals.

CHAPTER 6 analyzes the mechanical properties and microstructure characterization on copper-plated silicon trenches samples. Nano-indentation and EBSD tests are conducted on the test samples before and after regular pre-determined thermal annealing treatment intervals.

CHAPTER 7 shows the numerical analysis of the copper anisotropic material effect on thermo-mechanical stresses in copper TSVs under high temperature working conditions.

CHAPTER 8 summaries the findings from this work and provides an outline of potential future work.

CHAPTER 4. TEST VEHICLE FABRICATION

To experimentally study electroplated copper's mechanical properties and microstructure in silicon trenches as reviewed discussed in Chapter 1, two types of test vehicles—copper-filled TSVs and copper-plated silicon trenches were fabricated[1]. The fabrication process of the test vehicles is divided into 5 sections. The first section describes the geometry of copper filled TSVs and copper-plated silicon trenches. The second and third section focuses on their fabrication processes. The fourth and fifth section presents the effect of process variables, process optimization and yield analysis..

4.1 Test Vehicles Description

There are two types of test vehicles to be fabricated, and both of them are explained in this section. The first test vehicle type contains copper filled TSVs. Figure 4.1 shows the schematic top view of TSVs and Figure 4.2 shows the cross-section schematic view of TSVs. Copper filled TSVs are 50 μm in diameter, 250 μm in depth and 100 μm in pitch. The copper filled TSVs samples are fabricated in collaboration with the Integrated 3D Systems Group at Georgia Institute of Technolody. The second type is electroplated copper in a silicon trench, as shown in Figure 4.3 and Figure 4.4. Both the width and the height of the trenches are 100 μm, and the length is 5 cm longer than the width and the height. Upon fabrication, the test vehicles are diced into small pieces for the purpose of characterization. Although not illustrated in the schematics, the copper inside the trenches is surrounded by copper seed layer and titanium barrier layer.

Both types of samples have a similar material layout, namely copper surrounded by copper seed layer, titanium barrier layer, dielectric layer and silicon at the bottom and the sidewall.

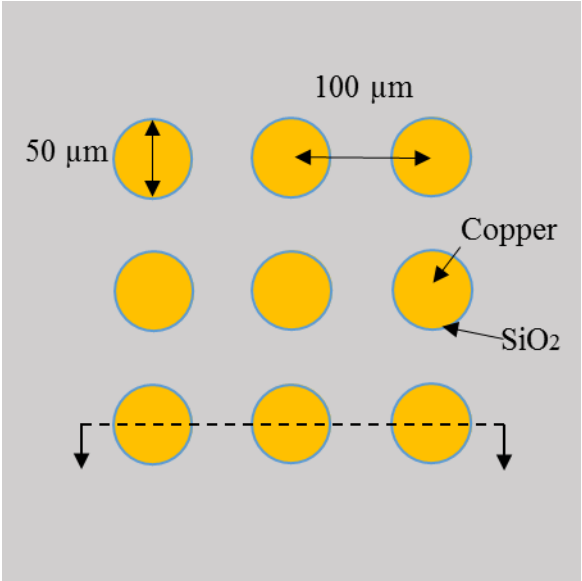


Figure 4.1: Top view of copper filled TSVs

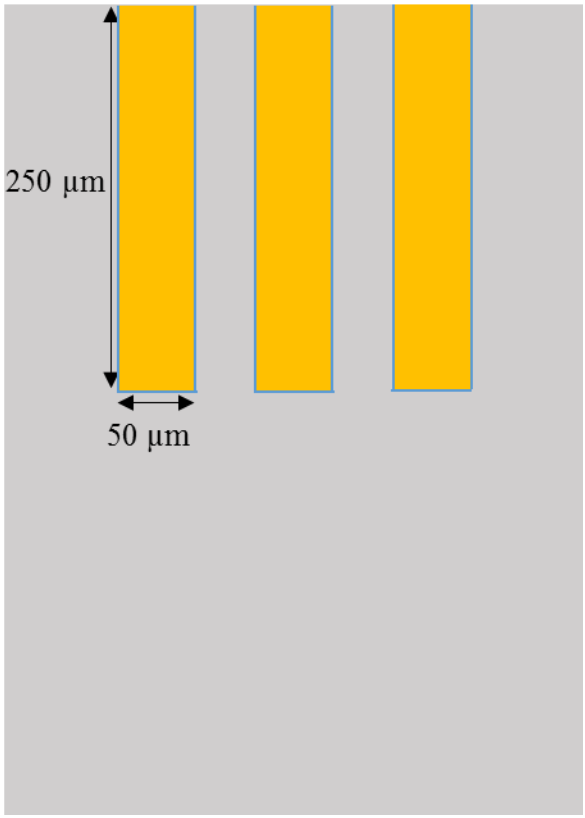


Figure 4.2: Cross-section view of a copper filled TSVs

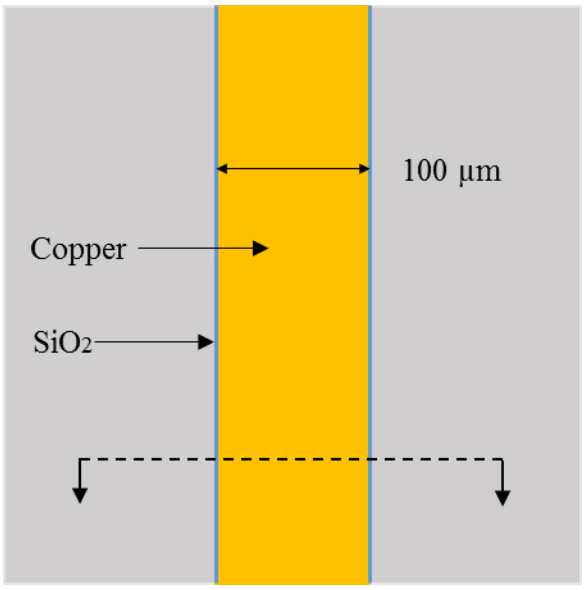


Figure 4.3: Top-view of a copper trench

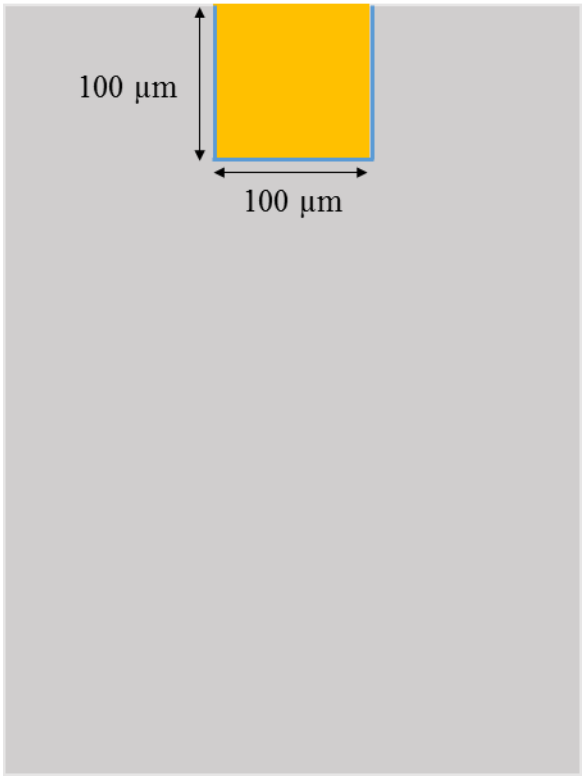


Figure 4.4: Cross-section view of a copper trench

4.2 Copper-filled TSV Fabrication

The copper TSV test vehicles are fabricated using standard lithography process. Copper TSVs are fabricated on commercially available 4-inch silicon wafers based on the process flow shown in Figure 4.5. As seen, a photoresist is spun on the silicon wafer such that the negative photoresist has a thickness of 7.5 µm. Then followed ultraviolet (UV) exposure and development. Then the wafer placed into STS-ICP® machine to etch the silicon used Bosch process. A 400 nm thick SiO_2 dielectric isolation layer was grown out of silicon using a wet thermal oxidation process from Mini Tystar Tube® at 1000 °C for 1 hour. Titanium barrier layer and copper seed layer were deposited using glancing angle

depositing evaporation process. The electroplating process fills the silicon trench using the pulse reverse plating technique.

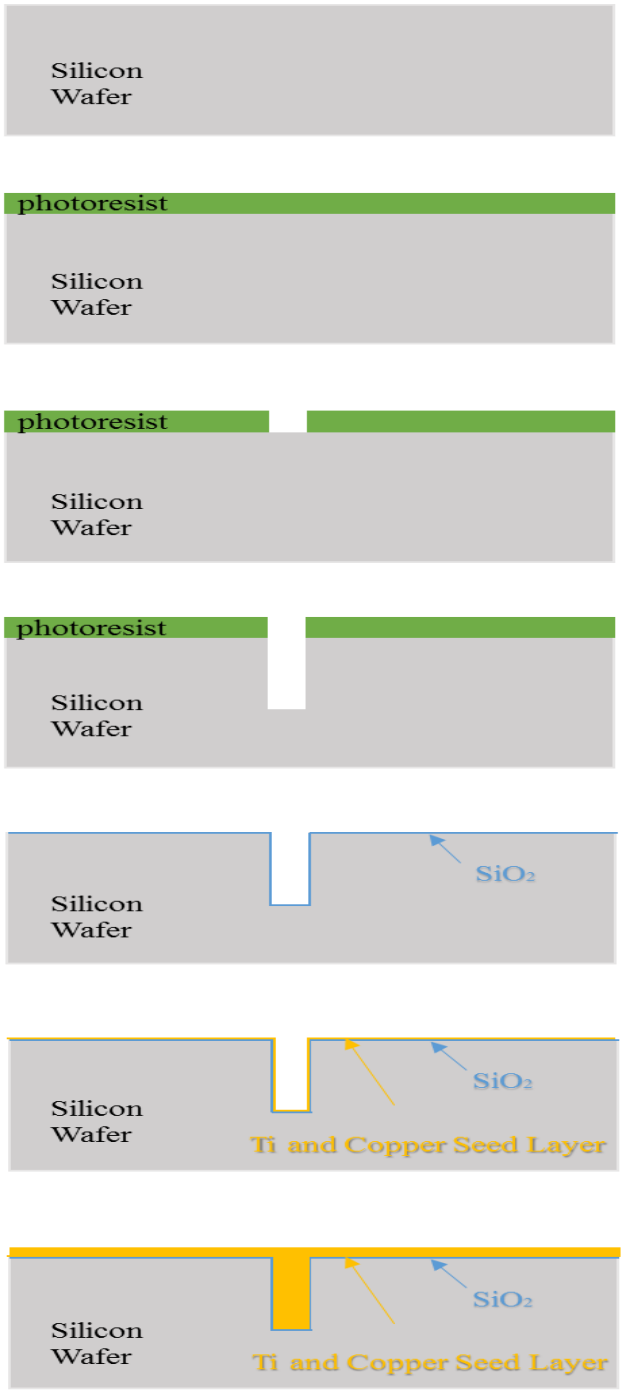


Figure 4.5: Process flow to fabricate copper filled TSVs

4.3 Copper Trench Fabrication

Copper trenches are fabricated on a commercially available double-sided polished 4-inch silicon wafers based on the process flow shown in Figure 4.6. The wafer was first cleaned using acetone, methanol, and isopropyl alcohol and deionized (DI) water. After a 7.5 μm thick Futurrex® NR5-8000 negative tone photoresist was spun coated at 3000 rpm by a BLE spinner® and soft bake at 150°C for 60 seconds, lithography was performed to pattern the trench The photoresist was exposed to a 365 nm light at a total exposure dose of 157.5 mW/cm^2 from MA6 Mask Aligner® in the Marcus Inorganic cleanroom at the Georgia Institute of Technology. After exposure, the sample was baked at 100°C for 60 seconds. Finally, the photoresist was developed using a photoresist developer RD6 for 60 seconds at the room temperature to remove the unexposed photoresist.

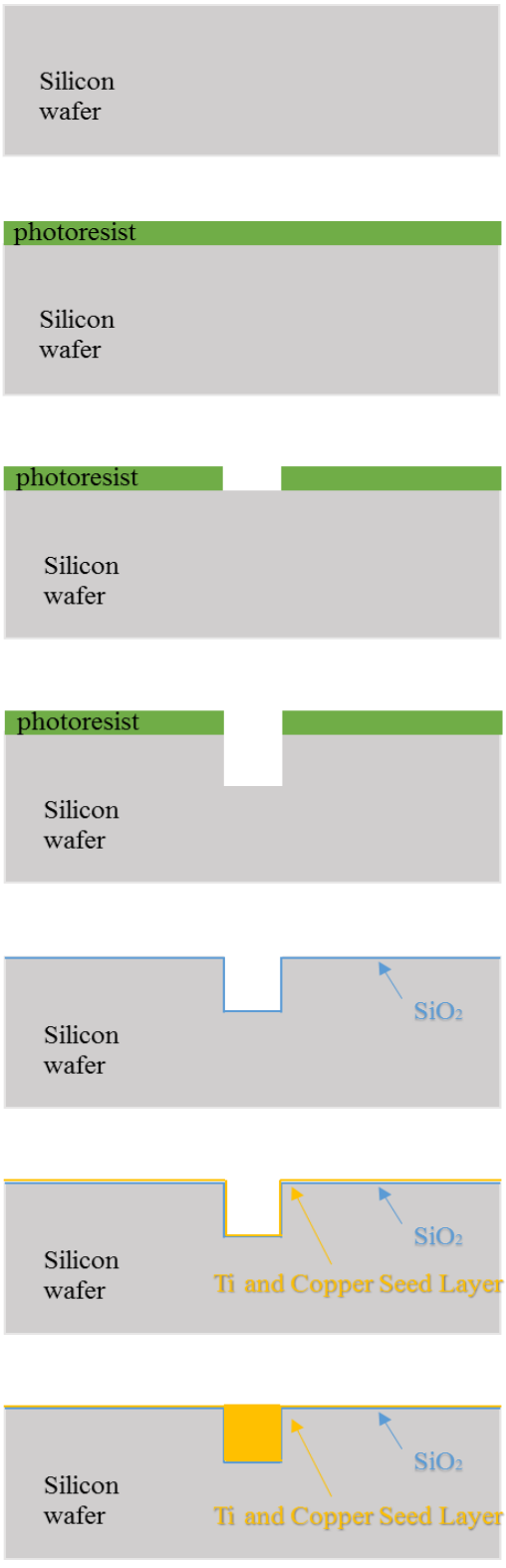


Figure 4.6: Process flow to fabricate copper trenches

After the lithography processes, the sample was placed into the inductively coupled plasma machine (STS-ICP®) to form the trench using Bosch dry etching process. Each Bosch process cycle consists of a passivation and an etching step, with the passivation time and the etching time being 17.5 and 14 seconds, respectively. Each cycle etched around 1 μm silicon in depth, and the sample was etched for 100 cycles, resulting in 100 μm deep silicon trenches. A profilometer was used to verify the trench depth. After cleaning the etching and photoresist residuals using acetone, methanol, and isopropyl alcohol, a 400 nm thick SiO_2 dielectric isolation layer was grown out of silicon using a wet thermal oxidation process from Mini Tystar Tube® at 1000 °C for 1 hour. The wet oxidation has better device isolation, contact isolation, and uniformity, compared to the plasma enhanced chemical vapor deposition (PECVD). A 100 nm Ti and 200 nm copper seed layer was sputtered using Unifilm DC Sputterer®.(Figure 4.7) The Ti layer was used to prevent copper from diffusing into Si and also to provide better adhesion between the copper seed layer and SiO_2.

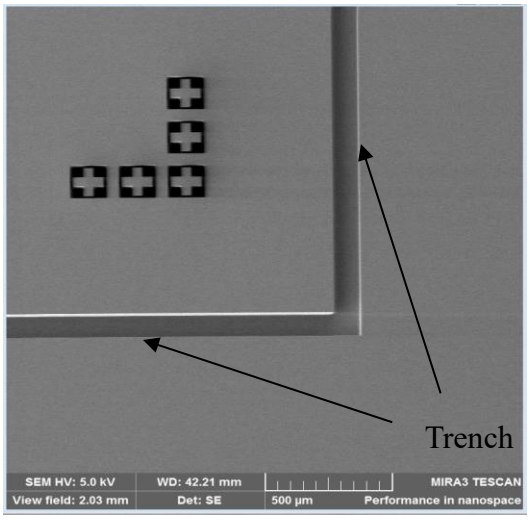


Figure 4.7: Top-view of silicon trench

Due to its high electrical conductivity and low electro migration characteristics, copper is used to fill the silicon trench by an electroplating process. Choosing proper equipment, plating chemistries, and plating receipt are the key ingredients to achieve void-free copper trench. As the electroplating process is very sensitive to the plating bath, it is important to control the plating chemistries constituents in the range and to prevent contaminants from entering the bath. Copper plating additives were used to prevented "pinch-off" voiding. This is the key to get void-free copper trench. The copper plating bath synthesizes multiple additives to optimize the polarization and depolarization balance to achieve void-free copper trench.

The plating power supply equipment is Dynatronix DuPR10-0.1-3®, which is a microprocessor-based programmable model with 10 different process steps. This product has a DC output ranging from 0.1 to 3 ampere at 10 Volts. In addition, it can supply a high-frequency pulse with 0.3-6 amps peak pulse current at 0-5000 Hz. The VELP Scientifica AREC® digital ceramic hot plate stirrer was used to make plating solution evenly and to achieve the planar surface finish.

The electroplating process fills the silicon trench using the pulse reverse plating technique. The plating receipt was optimized to achieve void-free copper trenches and to minimize the plating time. The receipt was to have three pulse on each cycles and with one reverse pulse cycle, the total time period for one cycle is 8 ms. The pulse on current is 15 mA for 1 ms, followed by a pulse off current of 0 mA for 1 ms, while the reverse pulse is negative 3 mA for 0.2 ms, followed a pulse off current of 0 mA for 1.8 ms. The plating process takes 48 hours to fill up silicon trench. The top view and cross-section view of copper-plated silicon trenches after electroplating as shown in Figure 4.8 and Figure 4.9.

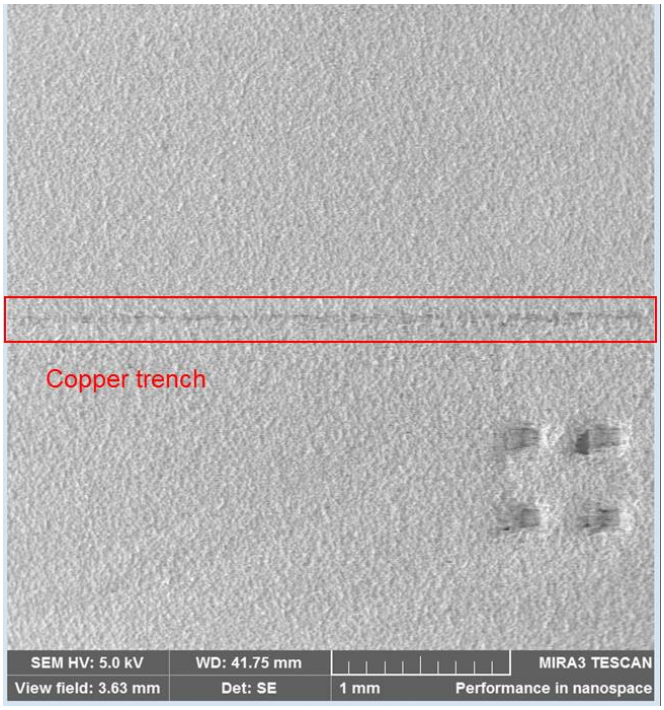


Figure 4.8: Fabricated copper trench

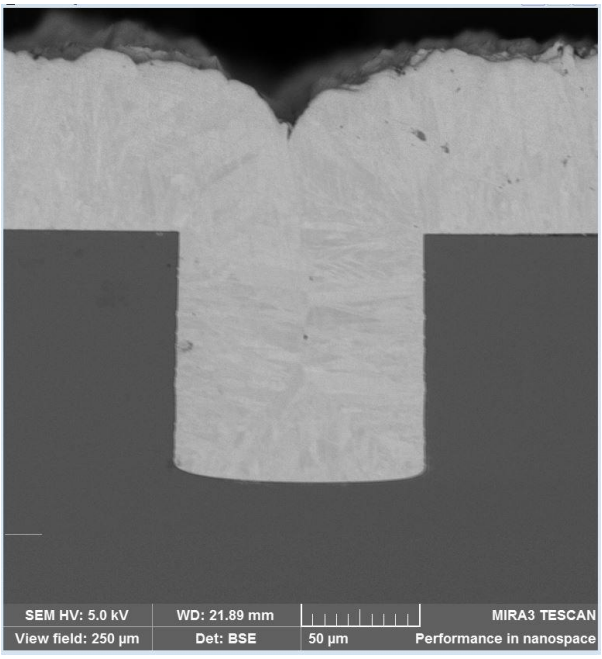


Figure 4.9: SEM cross-section view of a copper-plated silicon trench

4.4 Effect of Process Variables and Process Optimization

Process parameters are important to get successful output. The first step is to spin coat a photoresist layer on the silicon wafer. The process parameters include the amount of photoresist for a 4-inch wafer, spin speed and spin time. Based on the process guideline provided by the photoresist manufacturer, the optimization had performed to meet the needs for this application. The photoresist thickness attained by spin coating represents the equilibration between centrifugal force and solvent evaporation, both of which increase with the spin speed. There are some common spin coating defects during the fabrication process, including the bubbles on the surface, swirling pattern, uncoated areas, and unevenly surfaces, which would cause poor lithography results. The spin coating process had been optimized to get constant and controllable yield. The softbake procedure also followed the photoresist manufacturer's guideline.

The UV exposure intensity was checked per usage because the UV intensity changed each time. Then, the required exposure time was calculated. Hot plate bake and photoresist development followed the photoresist manufacturer's guidelines.

The dry etching process used STS-ICP® machine. As the machine performance varied each time, a dummy sample with the same pattern was used to calibrate the recipe. The Bosch process has scallops formed on the sidewalls which may reduce the reliability of the devices due to the leakage current. As the scallops size is proportional to the etching time, the passivation time and etching time were shortened to get faster gas switching to shorten process times for each cycle.

A dielectric layer, titanium barrier layer, and copper seed layer were deposited by well-known processes. The DC type sputtering process are used, it is had an additional axis of rotation which would create a more uniform thin-film gives good and controllable results.

Electroplating was used to fill up the copper trench. The copper trench was plated from the bottom and the side wall of the trench. The pinch-off voiding was a common problem for copper-plating. The plating step is one of the most expensive steps in manufacturing, and optimizing the plating recipe to minimize plating time can reduce the cost and also increase the reliability. DC reverse pulse electroplating process and additives can prevent the faster copper plating at the trench corner. Current with 15 mA was used to get slow plating speed to get void-free copper trench. Figure 4.10 shows a common problem for electroplating defects.

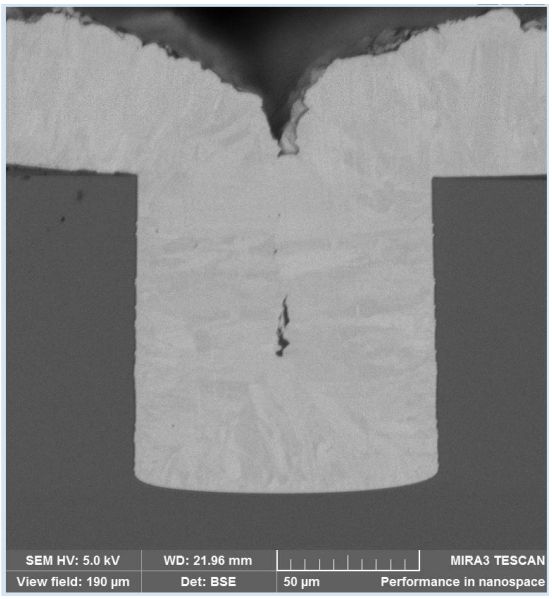


Figure 4.10: Copper trench with a void in the center

4.5 Yield Analysis

After fabricating copper-filled trenches, the sample was cross-sectioned to exam the fabrication quality. The first couple of batches of test vehicles had very low yield because the titanium barrier layer and the copper seed layer were deposited by an evaporation method. Evaporation is a directional method, and so the sidewalls are less likely to be covered. The bottom copper seed layer is not connected to DC source. So, after electroplating, there was no copper plated in the silicon trench. Hence, sputtering process was used to deposit titanium and copper at the bottom as well as the side wall of silicon trench. After electroplating, the first test vehicle showed there are voids in the copper trenches, which could be attributed to the gas trapped in the trench and pinch-off voiding. Therefore, the copper electroplating chemistries and plating recipe were optimized to get void-free copper trench.

CHAPTER 5. MECHANICAL PROPERTY AND MICROSTRUCTURE CHARACTERIZATION OF AGED COPPER-FILLED TSVS

This chapter presents the experiments that were conducted to characterize the mechanical properties and microstructures of aged copper-filled TSVs. The first section of this chapter focuses on the study of the hardness and elastic modulus of the copper TSVs using nano-indentation technique. The second section of this chapter focuses on the characterization of the grain size and texture of copper microstructure using electron backscatter diffraction (EBSD).

5.1 Sample Preparation for Nano-Indentation

This section describes the critical test vehicle preparation procedures before mechanical characterization and microstructure analysis. Wafers are kept at room temperature for about one year before cross-sectioning analysis is done. This is to understand whether there is any further microstructure change after long-term temperature thermal storage.

The silicon wafer is first diced into a number of samples after electroplating, while the over-plated Cu was not polished off. The Cu TSV samples were stored at room temperature for one year, e.g. 25 ºC, and then were cross-sectioned for characterization. Figure 5.1 shows a schematic view of the TSVs' cross-section view. Aged copper TSV samples are then adhered to a standard glass slide by Loctite® glass glue, as shows in

Figure 5.2. Then the test vehicle is then ground and polished to get the cross-section for subsequent characterization.

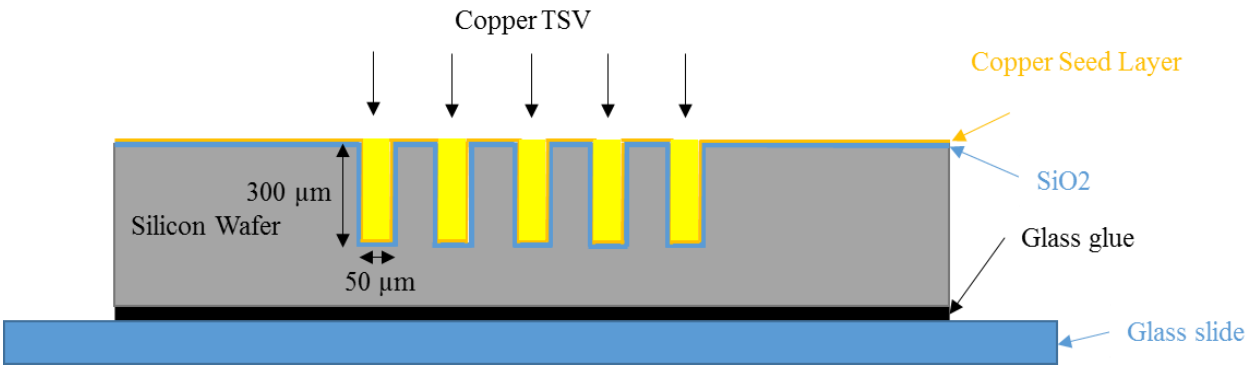


Figure 5.1: Schematic view of copper TSVs cross-section view

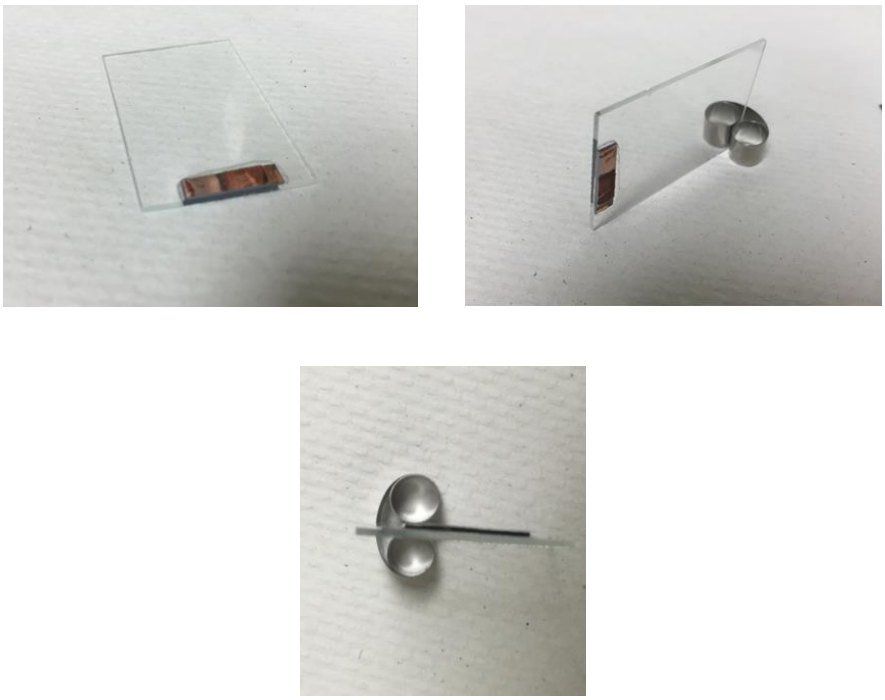


Figure 5.2: Copper TSVs glued to glass slide

The TSVs are polished using colloidal silica solution and mechanical planarization to obtain a smooth planar surface. Table 5.1 shows the polish consumables and polishing procedures used in polishing process.

Table 5.1: Polishing consumables and procedures

Steps	Description	Nominal Mircon Size	Company
1	400 Grit SiC Plain Backed	21.8	Pace Technologies®
2	600 Grit SiC Plain Backed	15.3	Pace Technologies®
3	800 Grit SiC Plain Backed	6.5	Pace Technologies®
4	1200 Grit SiC Plain Backed	2.5	Pace Technologies®
5	MetaDi® Diamond Suspension	1	Buehler®
5	Texmet C®	NA	Buehler®
6	MasterMet® Polishing Suspension	0.06	Buehler®
6	ChemoMet®	NA	Buehler®

Figure 5.3 shows a TSV cross-section after polished. The flatness and smoothness of the finishing surface is crucial for later experiments. This finishes the review of the sample preparation for nano-indentation experiment to characterize the hardness and elastic modulus

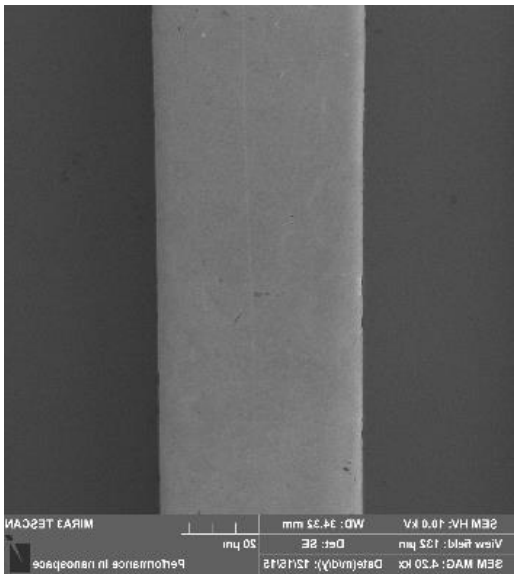


Figure 5.3: SEM cross-section image of copper TSVs

5.2 Nano-indentation Experiments

Annealing effects are studied by nano-indentation analysis. Since copper recrystallization occurs at 250 °C [84], annealing temperature was chosen above 250 °C. This ensures that the temperature is high enough to let microstructure recrystallization. Three annealing temperatures were 300 °C, 400 °C and 500 °C with 180 minutes of annealing for each temperature. Nano-indentation are performed before and after thermal annealing treatment. The purpose is compare the hardness and E-modulus difference between them. Figure 5.4 shows the Agilent® Nano-indenter G200 used for copper mechanical properties characterization. Figure 5.5 shows the Cambridge Fiji Plasma® atomic layer deposition (ALD) tool used for annealing treatment.

Figure 5.4: Agilent® nano-indenter

Figure 5.5: Cambridge Fiji Plasma® atomic layer deposition (ALD) tool

Nano-indentation is one of the most commonly used methods to test the mechanical properties of materials. It is usually used to measure the hardness and elastic modulus of small volumes of material. Nano-indentations are carried out using a Nano-indenter MTS XP System® which is equipped with a continuous stiffness measurement attachment and attached with a three-sided pyramidal diamond Berkovich tip. The continuous stiffness measurement with the harmonic depth and frequency were 2nm and 45 Hz, respectively. The indentation strain rate was $0.05s^{-1}$. During the indentation process, the applied load and the displacement were continuously recorded as the displacement was controlled to a maximum depth of 1000 nm. Figure 5.6 shows sample molded in epoxy before indentation experiment. There are six indentations, starting at 5 μm from the top edge with a spacing of 20 μm along the axis of the TSVs (Figure 5.7). The spacing is selected so as to minimize the influence from other neighboring indents, as well as the influence of surrounding silicon walls. The elastic modulus and hardness values were obtained from the test by using the Oliver-Pharr relation [85].

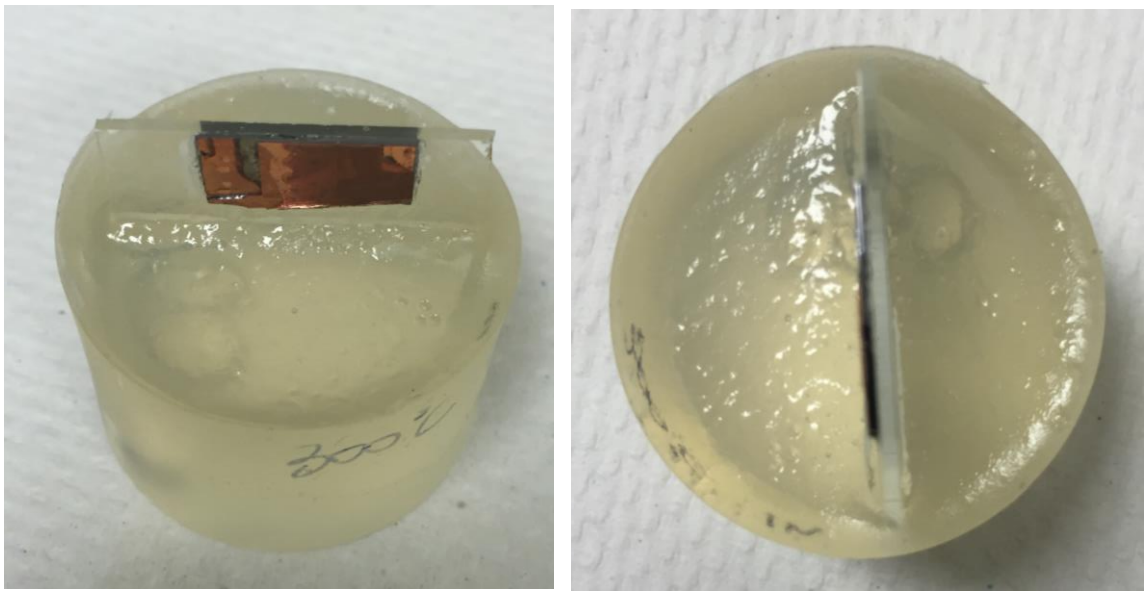


Figure 5.6: Images showing the sample before indentation

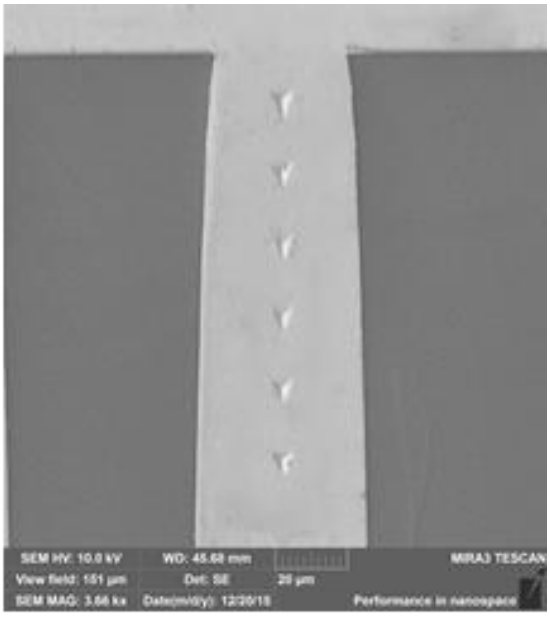


Figure 5.7: SEM image showing the indentation spots along the axis of a polished blind TSV

The hardness values of the Cu TSVs under one-year room-temperature-aged condition as well as after three high-temperature annealing conditions were measured and compared. Fifteen Cu TSVs with six indentations per TSV were studied for each annealing condition. Thus, 90 indentation measurements are averaged and compared. Figure 5.8 shows a schematic representation of a section through an indentation: h is the total displacement; h_c is the vertical distance along which contact is made; and h_s is the displacement of the surface at the perimeter of the contact; P is the load and the radius of the contact circle. The elastic displacement is recovered after unloading, and the final depth of the residual hardness impression is h_f. Figure 5.9 shows the load and displacement plot for a standard indentation test. h_{max} is the maximum displacement at peak load.

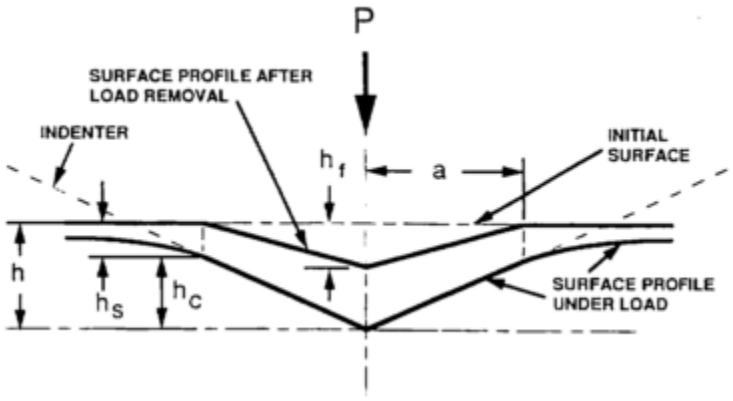


Figure 5.8: A schematic representation of a section through an indentation showing various quantities used in the analysis [Source: Oliver] [85]

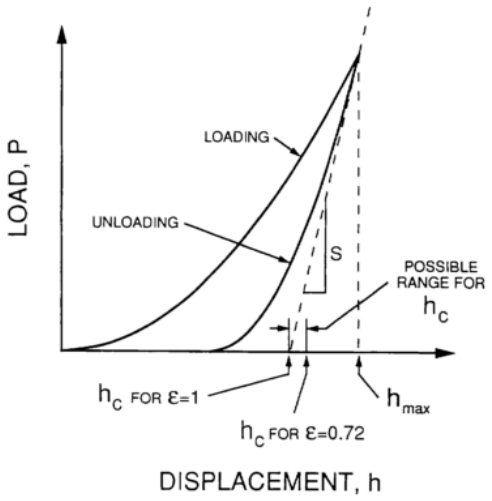


Figure 5.9: A schematic representation of load versus indenter displacement showing quantities used in the analysis as well as a graphical interpretation of the contact depth [Source: Oliver] [85]

$$\frac{1}{E_r} = \frac{(1-v^2)}{E} + \frac{(1-v_i^2)}{E_i} \qquad \textbf{5.1}$$

$$E_r = \frac{\sqrt{\pi}}{2}\frac{S}{\sqrt{A}} \qquad \textbf{5.2}$$

$$A(h_c) = 24.5h_c^2 + C_1h_c^1 + C_2h_c^{\frac{1}{2}} + C_3h_c^{\frac{1}{4}} + C_4h_c^{\frac{1}{8}} \qquad \textbf{5.3}$$

Eq. 5.1 is used to calculate the modulus of the sample. The E and v are elastic modulus and Poisson's ratio for the sample, respectively, and E_i and v_i are the elastic

modulus and Poisson's ratio for the indenter tip, respectively. The E_r is the reduced modulus which can be calculated by Eq. 5.2. In Eq.5.2, the S is the measured stiffness, and A is the contact area that is calculated by Eq. 5.3. The relationship between the indentation load and the depth is illustrated in Figure 5.10. It shows six consistent indentation measurements on one TSV sample.

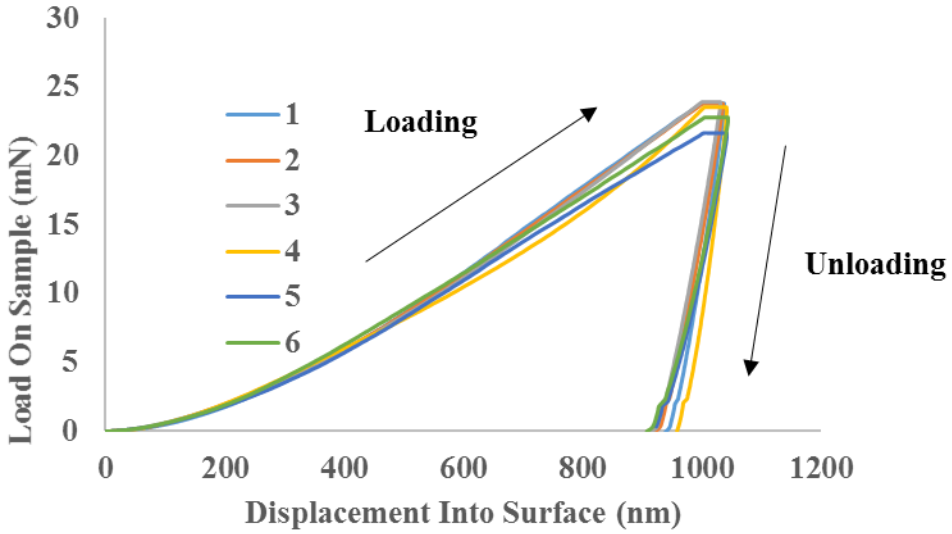


Figure 5.10: Displacement into surface and load on sample

The one-year room-temperature-aged samples had the highest hardness value of 1.4 GPa, which is higher than the reported values of bulk copper (H ~ 1.0-1.2 GPa). The higher hardness value can be explained by factors such as induced residual stress during electroplating, inclusion of additives during electroplating process [44, 86, 87], and smaller copper grain size in TSV trench compared to bulk copper. Figure 5.11 compares the average hardness values for as-received, one-year room-temperature-aged samples, and three high-temperature-annealed samples. After annealing, the hardness value decreases to 1.2 GPa, 1.1 GPa and 1.0 GPa as the annealing temperature increases. The reduction in

hardness can be explained by the reduced residual stress. Hall-Petch relation cannot be applied [88], since the grain size did not increase, as shows in Figure 5.16, Figure 5.17 and Figure 5.18 in the following section.

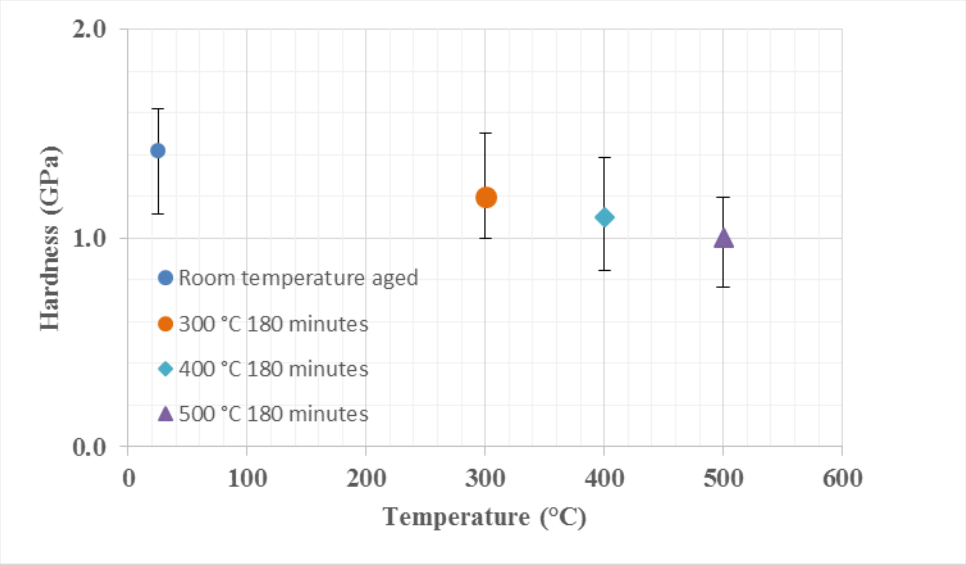


Figure 5.11: Average hardness values before and after high-temperature annealing

Figure 5.12 compares the average E-modulus values for as-received one-year-aged samples and three high-temperature-annealed samples. E-modulus before high-temperature aging was 111 GPa, but it decreased to 102 GPa, 96 Gpa, and 94 GPa after 300 °C, 400 °C, and 500 °C thermal aging, respectively. As mentioned earlier, the grain size did not change, and there was minor change in the grain orientation. This grain orientation change is driven by the decrease in total free energy since microstructures tend to reach to lowest total free energy for maintaining stable states [1].

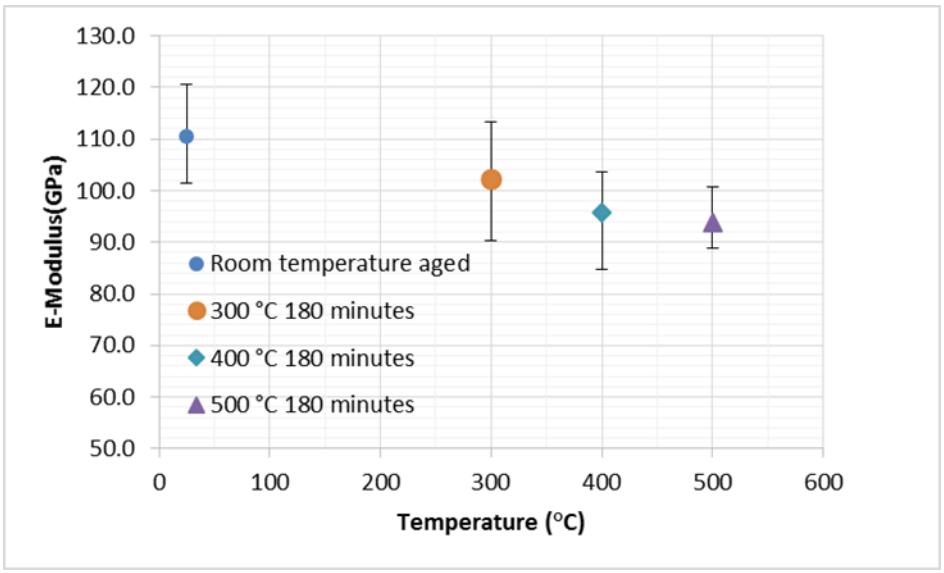


Figure 5.12: Average elastic modulus values before and after high-temperature annealing

5.3 Sample Preparation for Electron Backscatter Diffraction

The sample preparation process for EBSD is used the same process as for nano-indentation experiment. After polished, the sample is washed by acetone to dissolve glass glue to release sample.

5.4 Electron Backscatter Diffraction Experiments

EBSD, as a microstructural-crystallographic characterization technique, is the most common technique to study the structure, crystal orientation and phase of any crystalline or polycrystalline material in SEM. EBSD measurements were carried out using a TESCAN SEM® equipped with an EBSD detector shows in Figure 5.13. The samples are angled 70° towards the electron-scanning microscopy (SEM) detector while taking the EBSD measurements Figure 5.14 shows the experimental setup inside SEM.

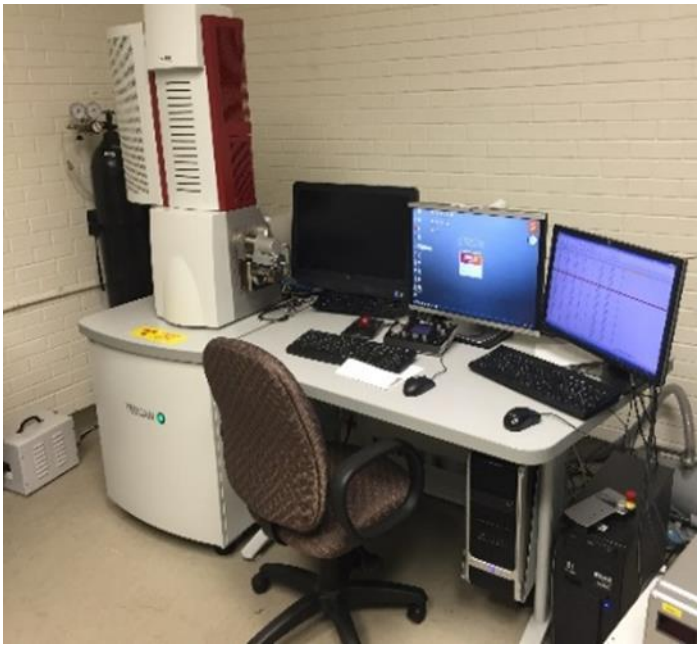


Figure 5.13: TESCAN® SEM with an EBSD detector

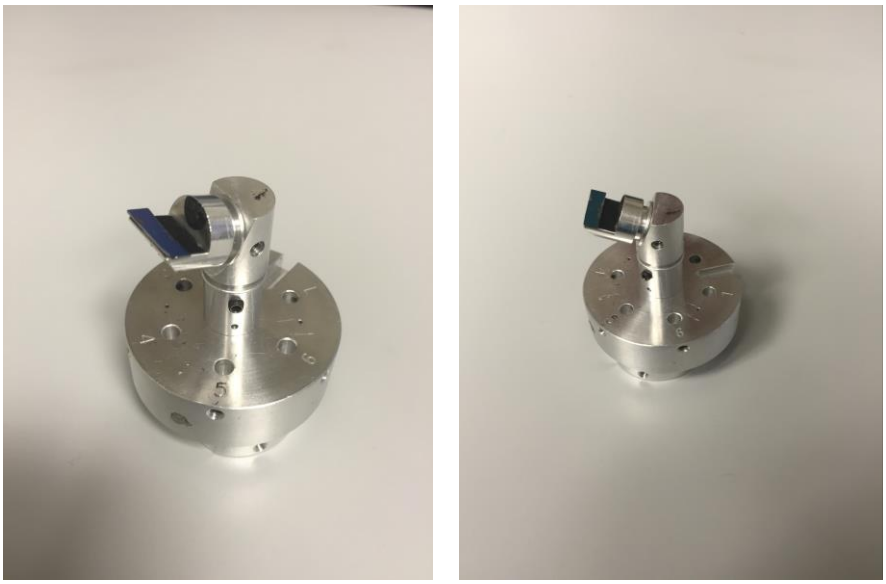


Figure 5.14: Image of EBSD scan set up

All EBSD images are rectangular in shape with 120 um length along the axis of the TSV and 60 um width along the transverse width or radial direction of the TSV. EBSD

measurements are first taken on the cross-sectioned samples, and then the samples are subjected to high-temperature annealing treatments. It is important to study the cross-sectioned samples under vacuum condition or flowing argon gas to prevent copper oxidization. Therefore, the annealing treatments are accomplished using Cambridge Fiji Plasma® atomic layer deposition (ALD) tool. Figure 5.5 shows the tool for annealing treatment. The cross-sectioned copper TSVs are placed in the chamber with a ramp of 13 °C/minute under vacuum and flowing argon gas at 20 sccm throughout the annealing process. After letting the copper TSVs cool down under vacuum environment, the second post-annealing EBSD measurement is conducted on the same TSV. By comparing the two EBSD images, before and after annealing, the crystal structure changes due to annealing could be determined.

The EBSD scan are performed on copper TSVs before and after annealing treatment. After the data collection, the EDAX® Orientation Imaging Microscopy (OIM) Data Analysis software is used to analyze the copper microstructure. The inverse pole figure map shows the distribution of crystallographic directions parallel to certain sample directions and can show some texture clearly. Figure 5.15 shows the steps to get inverse pole figure map. The first step is a cubic crystal unit cell oriented with respect to the sample axes. The second step is the same sample axes oriented with respect to the crystal unit cell. The third step is the crystallographic direction parallel to normal direction plotted on a stereographic projection with axes parallel to the edges of the crystal unit cell. The direction is repeated because, for cubic materials, it could be anyone of 48 symmetrically equivalent crystal directions. The last step is the light blue area from the stereographic projection in the previous step is extracted to form the normal direction inverse pole figure [89].

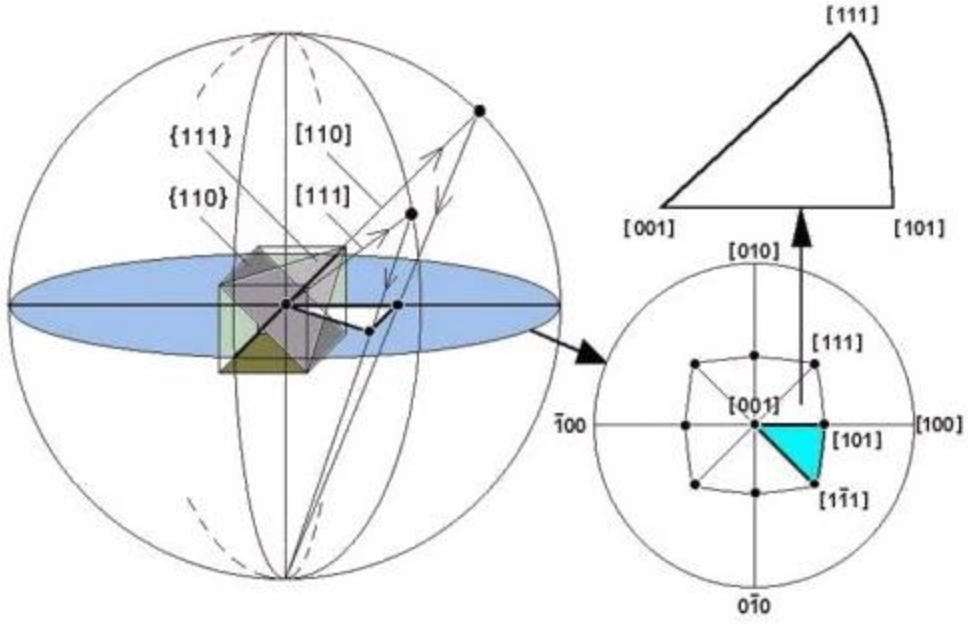
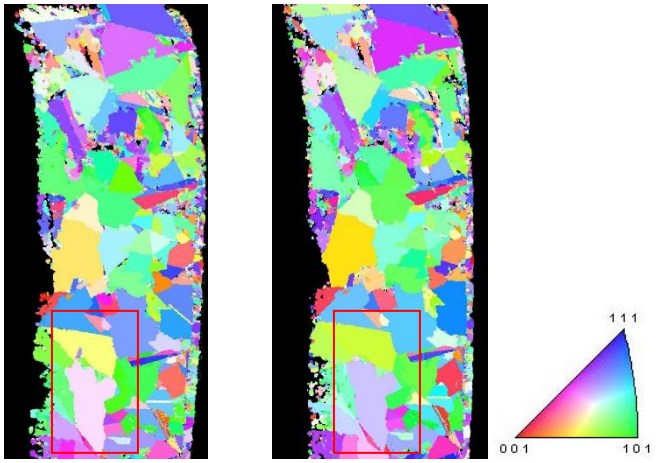


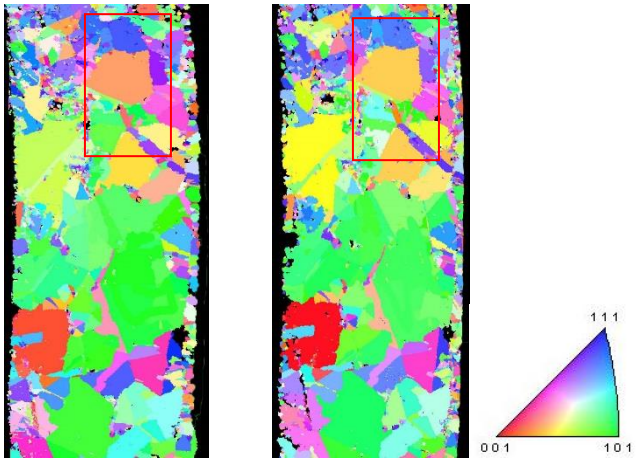
Figure 5.15: Summary of the steps involved in forming an inverse pole figure [89]

Figure 5.16, Figure 5.17 and Figure 5.18 show the inverse pole figure map for three copper TSVs samples before and after annealing treatment. The grain size does not increase, as shown in Figure 5.16, Figure 5.17 and Figure 5.18. Since the samples are room-temperature aged for one year, it is possible that copper microstructure had already fully stabilized, and no further grain growth occurred due to high-temperature annealing. Only minor changes in grains orientation were observed after high-temperature annealing. Here, the explanation for reduction in measured hardness values lies in the presence of residual stresses after electroplating, and these residual stresses decrease due to high-temperature annealing. Thus, the hardness values seem to be more influenced by the residual stresses rather than by the grain size.



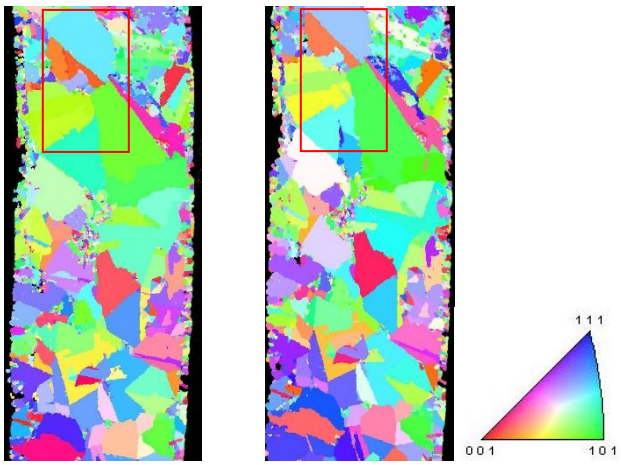
(a) (b)

Figure 5.16: EBSD images: (a) aged at room temperature for one year, and (b) annealed at 300 °C for 180 minutes



(a) (b

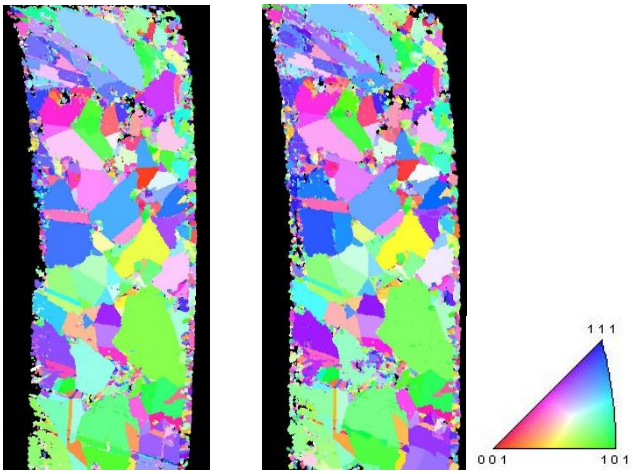
Figure 5.17: EBSD images: (a) aged at room temperature for one year, and (b) annealed at 400 °C for 180 minutes



(a) (b)

Figure 5.18: EBSD images: (a) aged at room temperature for one year, and (b) annealed at 500 °C for 180 minutes

To ensure that the annealing duration is not the limiting factor for grain growth, the copper TSVs are annealed at 400 °C for 30 hours. Figure 5.19 compares the sample before and after annealing. There is no significant grain growth observed. Again, only limited changes in grain orientation were observed. Based on this, it can be concluded that the annealing duration is not the limiting factor for grain growth. This confirms after one-year room-temperature aging, grain growth will not happen.



(a) (b)

Figure 5.19: EBSD images: (a) aged at room temperature for one year, and (b) annealed at 400 °C for 30 hours

Additionally, the one-year-aged samples show a significant difference in grain size near the silicon walls and near the center of the TSVs, away from the silicon walls (Figure 5.20). The grains near the center of TSVs are about 10 – 20 μm in size, while the grains near the silicon walls were much smaller, about 2 μm in size.

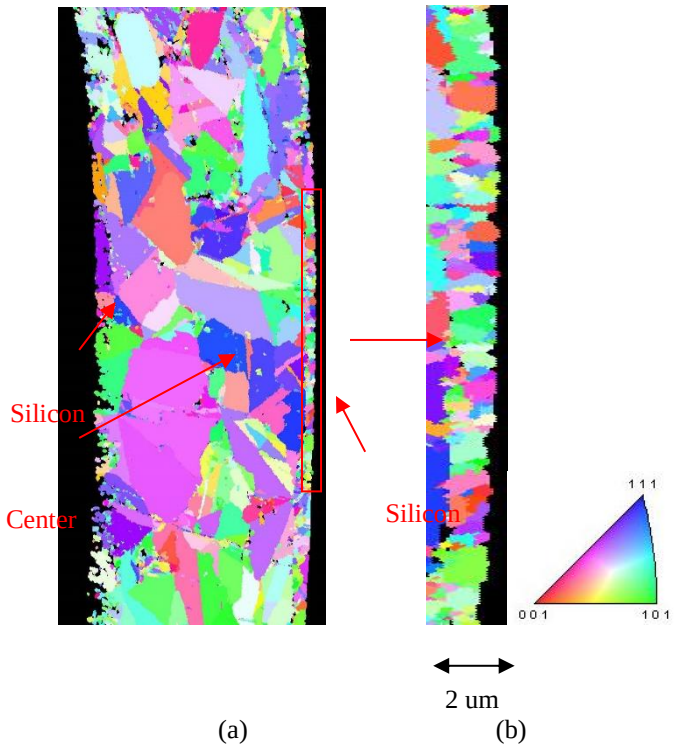


Figure 5.20: EBSD images: (a) aged at room temperature for one year, and (b) detail of edge

5.5 Discussion

Copper TSVs that were aged at room temperature were used as starting samples in this study. The samples were then annealed at three temperatures 300, 400, and 500 °C over 180 minutes. The copper grain size distribution and texture were investigated using EBSD. The mechanical properties of copper were investigated using Nano-indentation to get hardness and elastic modulus values.

1. After one-year room-temperature aging, no further significant grain growth was observed after high-temperature annealing treatments.

2. After annealing treatments, the hardness and the elastic modulus decreased by 28% and 15% respectively. This reduction could be explained by possible relaxation of residual stresses enabled through the rotation of copper grains.

CHAPTER 6. MECHANICAL PROPERTY AND MICROSTRUCTURE CHARACTERIZATION OF COPPER-PLATED SILICON TRENCHES

This chapter presents the experiments that are conducted to characterize the mechanical properties and microstructures of copper-plated trenches. The first section of this chapter focuses on the study of the hardness and elastic modulus of the copper-plated silicon trenches using the nano-indentation technique. The second section of this chapter focuses on the characterization of the grain size and texture of the copper microstructure using electron backscatter diffraction (EBSD).

6.1 Sample Preparation for Nano-indentation

The copper plated silicon trenches are prepared using the steps outlined in Chapter 5. Figure 6.1 shows a schematic of the copper-plated silicon trench attached to a glass slide by Loctite® glass glue. Figure 6.2 shows an SEM image of the copper-plated silicon trench after grounding and polishing. The polished sample is molded in the epoxy to hold it in place and is then put in the nano-indenter to perform the indentation test.

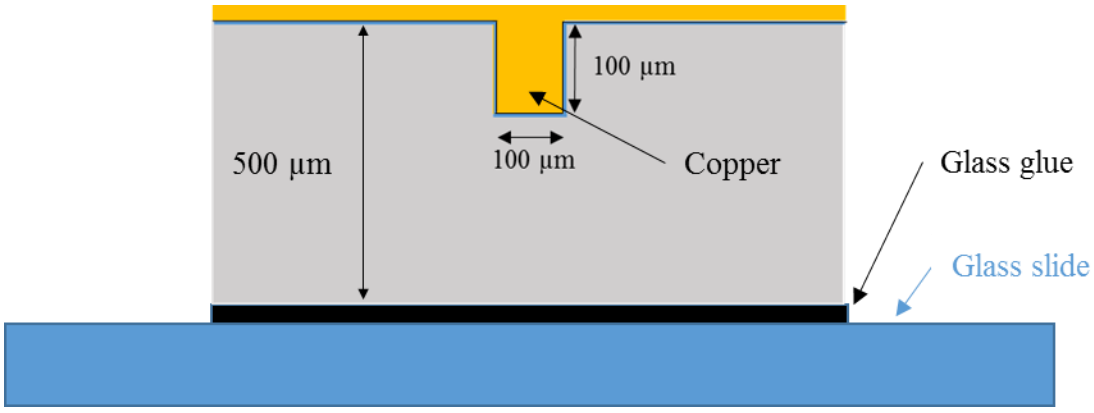


Figure 6.1: Schematic of copper-plated silicon trench

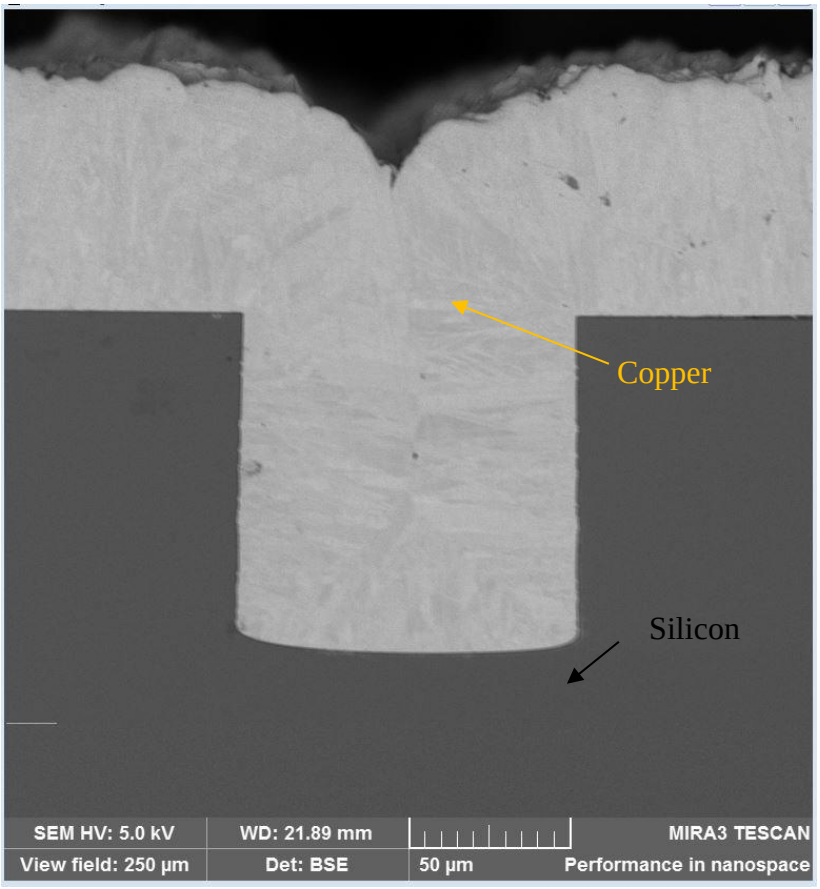


Figure 6.2: SEM cross-section of a copper-plated silicon trench

6.2 Nano-indentation Experiments

Samples are created by cleanroom fabricate have discussed in Chapter 4. Annealing effects are studied by nano-indentation analysis. The equipment used for characterization of copper fill TSVs is also used for analyzing copper plated silicon trenches. Nano-indentation is performed to obtain mechanical properties of as-electroplated sample and after different thermal annealing conditions. Table 6.1 shows all the annealing conditions of copper-plated silicon trenches for the nano-indentation experiment. Five indentation experiments on each sample and three samples for each conditions have performed. The copper-plated silicon trenches are polished right after it has been fabricated. Nano-indentation measurements are made on the copper after electroplating. Subsequently, annealing is performed on the copper plated silicon trenches for 1 hour and 24 hours at temperatures of 300 °C, 400 °C and 450 °C.

Table 6.1: Copper-plated silicon trench annealing conditions for nano-indentation experiment

Temperature (°C) / Duration	RT	300	400	450
As-plated	3	N/A	N/A	N/A
1 hour	N/A	3	3	3
24 hours	N/A	3	3	3

The Nano-indentation experiment set up for copper-plated trenches uses a three-sided pyramidal diamond Berkovich tip. The continuous stiffness measurement is measured at a harmonic depth of 2nm and a frequency of 45 Hz. The indentation strain rate

for the experiment is $0.05s^{-1}$. During the indentation process, the applied load and the displacement are continuously recorded until a displacement is depth of 1000 nm is reached. Five indentations are made such that the indentation location is at least couple micron away from the surrounding silicon with a spacing of 20 μm along the axis of the copper-plated silicon trenches (Figure 6.3). The spacing is selected to minimize the influence from other neighboring indents, as well as the influence of surrounding silicon walls. The elastic modulus and hardness values are obtained from the test by using the Oliver-Pharr relation [85]. It has been explained in detail in Chapter 5.

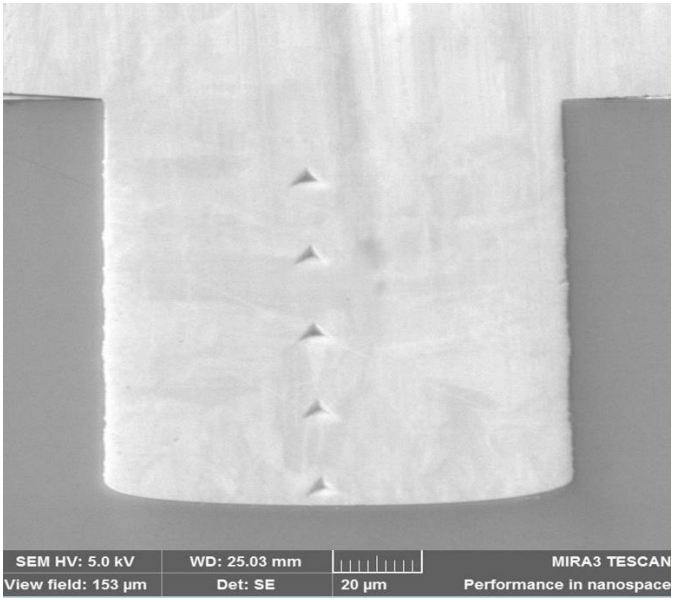


Figure 6.3: SEM image showing the indentation spots along the axis of a polished copper plated silicon trench

The hardness values of the copper-plated silicon trenches is measured and compared after electroplating and after thermal annealing. The measurements are made after 1 hour and after 24 hours high-temperature annealing treatment. Three samples with

copper-plated silicon trenches with five indentations per trench were studied for each annealing condition. Thus, 15 indentation measurements are averaged and compared. Figure 6.4, Figure 6.5, Figure 6.6 and Figure 6.7 shows the relationship between the indentation load and displacement graph obtained for copper-plated silicon trenches under different conditions.

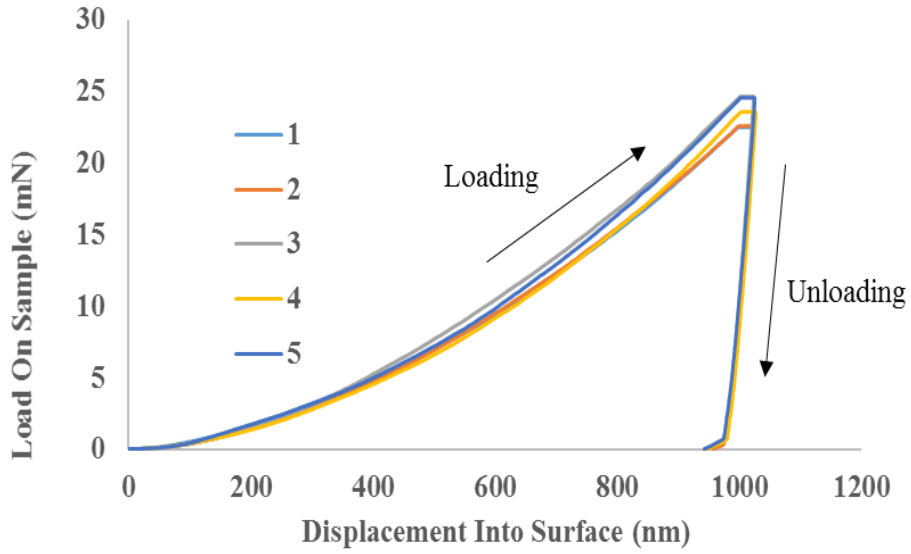


Figure 6.4: Displacement into surface and load on sample of as-plated sample

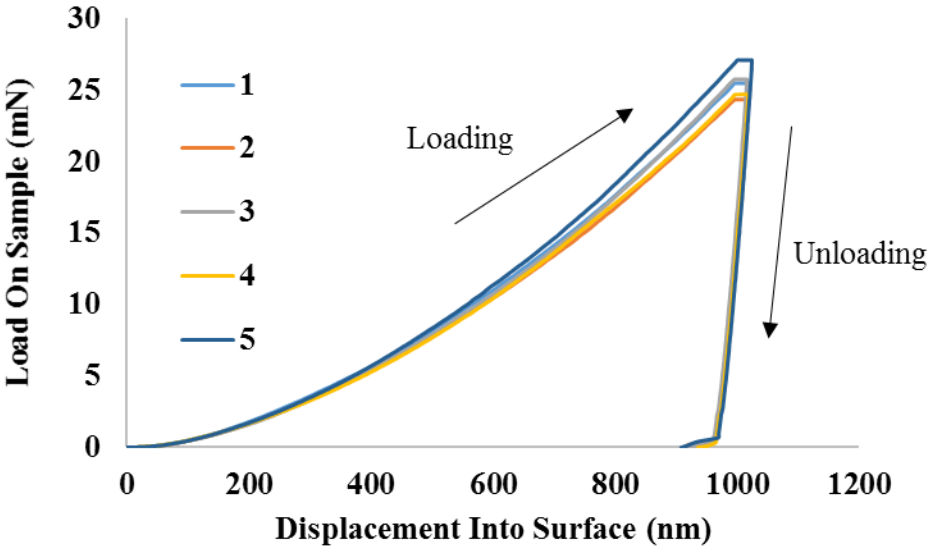


Figure 6.5: Displacement into surface and load on sample of annealed sample for 1 hour at 300°C

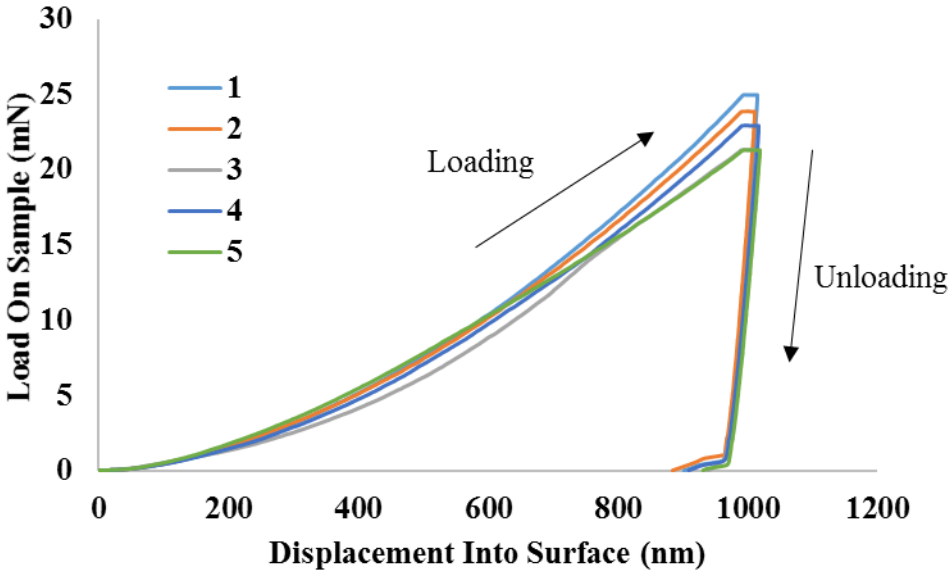


Figure 6.6: Displacement into surface and load on sample of annealed sample for 1 hour at 400°C

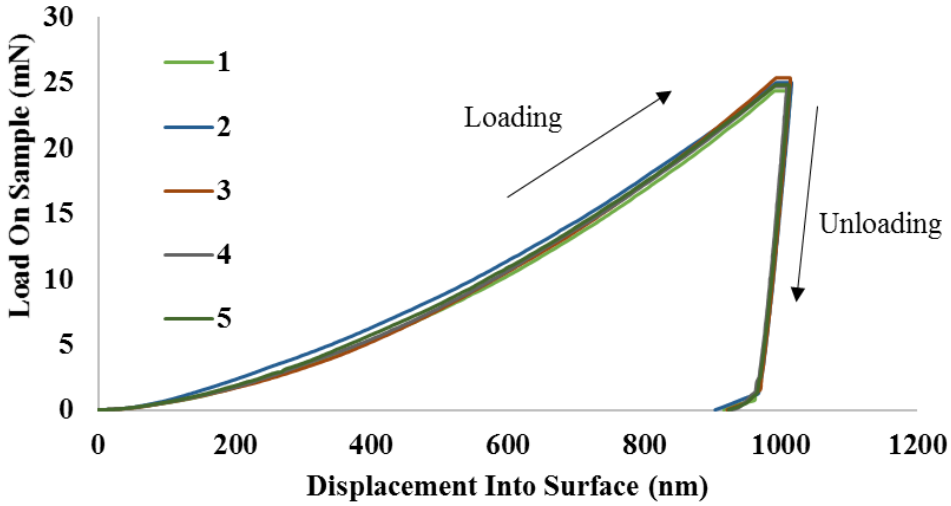


Figure 6.7: Displacement into surface and load on sample of annealed sample for 1 hour at 450°C

The as-plated samples have the highest hardness value of 1.20 GPa, which is within the reported values of bulk copper (H ~ 1.00-1.20 GPa). Figure 6.8 compares the average hardness values for as-plated, and high-temperature-annealed samples. Figure 6.9, Figure 6.10 and Figure 6.11 compares the average hardness values for as-plated and thermal annealed sample at different temperature for different annealing durations. After one-hour annealing at 300 °C, 400 °C, and 450 °C, all of the hardness value decreases to 1.05 GPa. Annealing is also performed for 24 hours at 300°C, 400°C and 450°C. This additional annealing step is done to study how annealing duration affects the mechanical properties of copper plated silicon trenches. After 24 hours of annealing, the hardness value continues to decrease further. The hardness value obtained was 1.00 GPa at 300 °C, 1.00 GPa at 400

°C and 0.95 GPa at 450 °C. Hardness value decreases more for longer annealing durations, however the absolute hardness value obtained is small in magnitude. Therefore, one-hour high-temperature annealing is sufficient for the hardness value of copper to stabilize. The reduction in hardness of the copper plated silicon trenches can be explained by the reduced residual stress in the copper. The Hall-Petch relation cannot be applied to the hardness value [88], since the grain size does not increase, as shows in Figure 6.19, Figure 6.21 and Figure 6.23 in the following section.

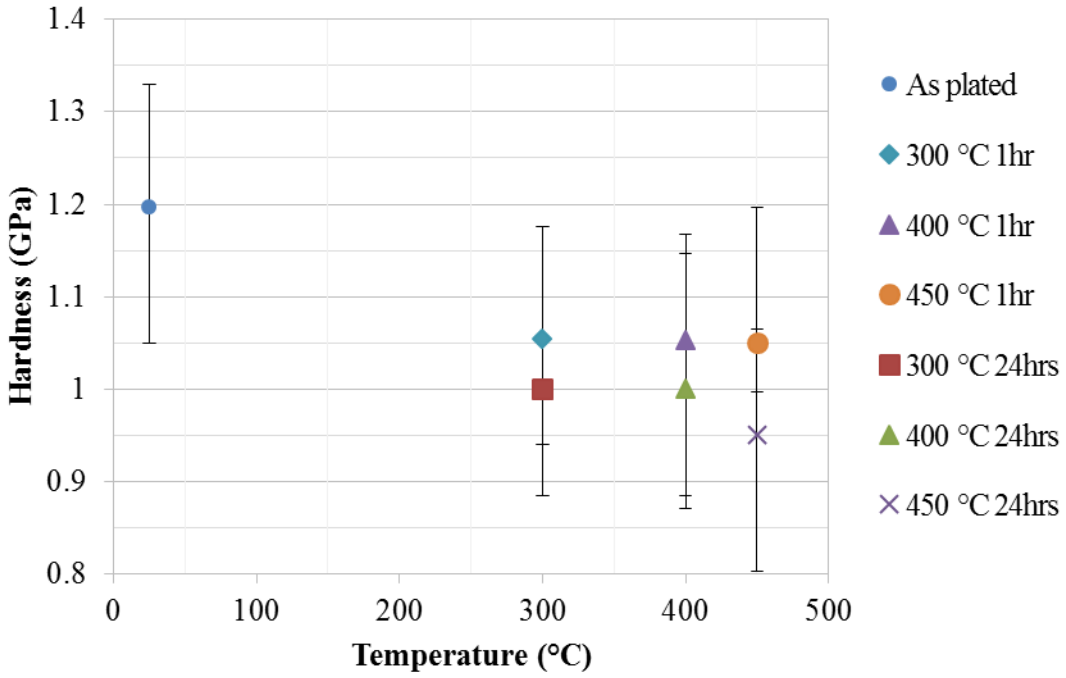


Figure 6.8: Average hardness values before and after thermal annealing

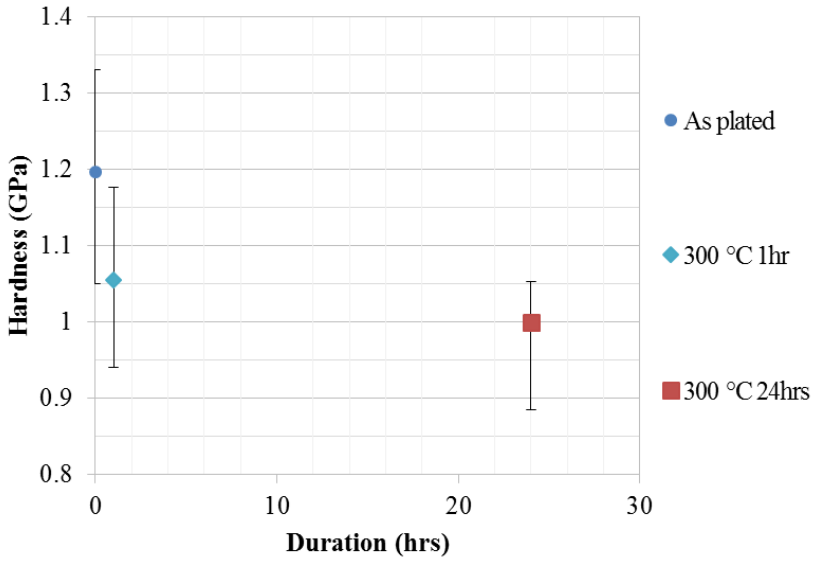


Figure 6.9: Average hardness values before and after 300 °C annealing of different durations

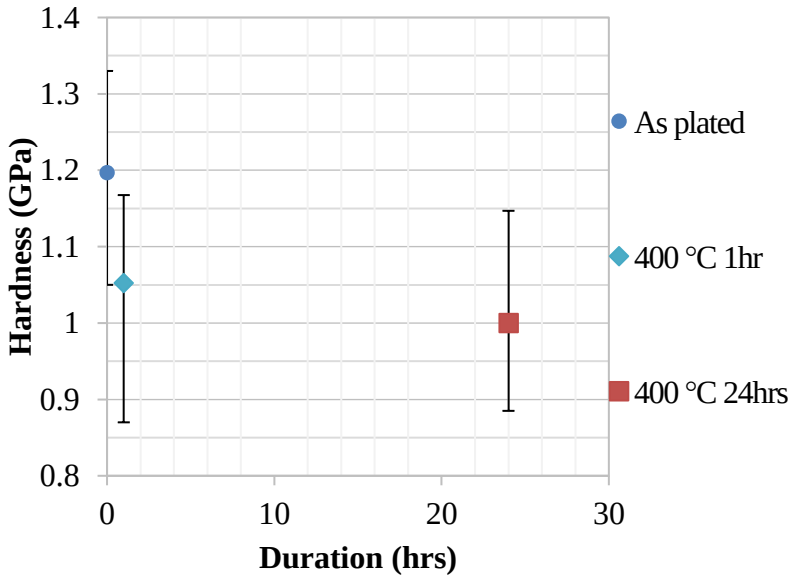


Figure 6.10: Average hardness values before and after 400 °C annealing of different durations

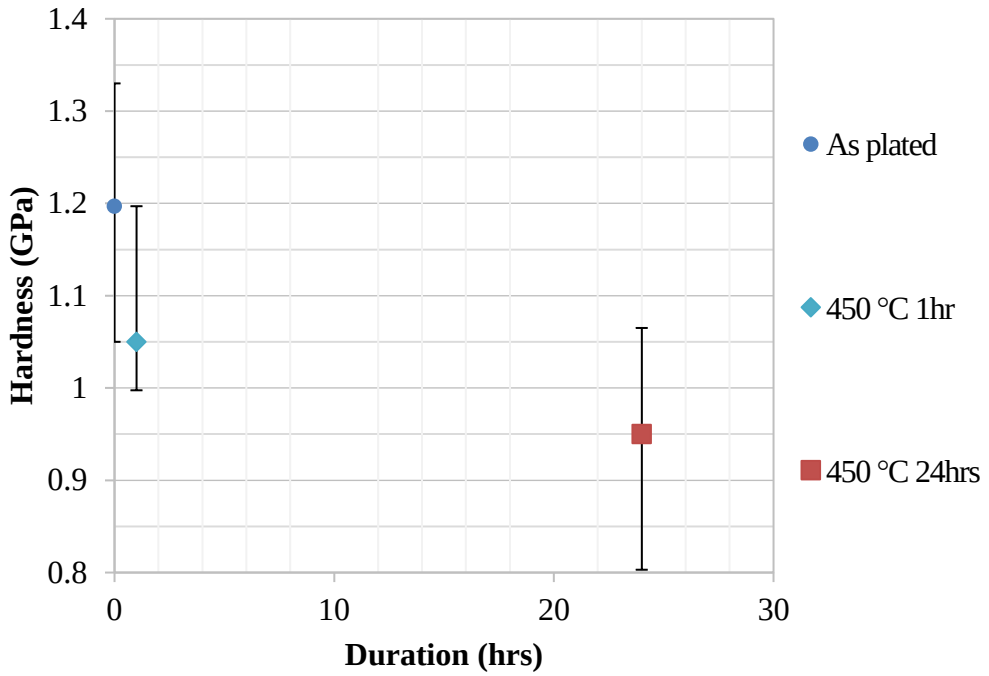


Figure 6.11: Average hardness values before and after 450 °C annealing of different durations

Figure 6.12 compares the average elastic-modulus value for as-plated copper plated samples and six high-temperature-annealed copper plated samples. Figure 6.13, Figure 6.14 and Figure 6.15 compares the average elastic modulus values for as-plated and thermal annealed sample at different temperature for different annealing durations. The elastic-modulus for as-plated samples is 118 GPa, but this value decreases to 109 GPa at 300 °C, 107 GPa at 400 °C, and 106 GPa at 450 °C after thermal aging for one-hour, Afterwards, three copper plated samples are put through 24 hours high-temperature annealing treatments for 300 °C, 400 °C, and 450 °C, respectively. The elastic-modulus value decreases to 107 GPa at 300 °C, 105 GPa at 400 °C, and 103 GPa at 450 °C, respectively. Kumon [90] based on surface acoustic wave spectroscopy experiments showed that residual stresses affect the elastic modulus of a material. The elastic modulus decreases as

annealing temperature and duration increases may be linked to the presence of residual stresses.

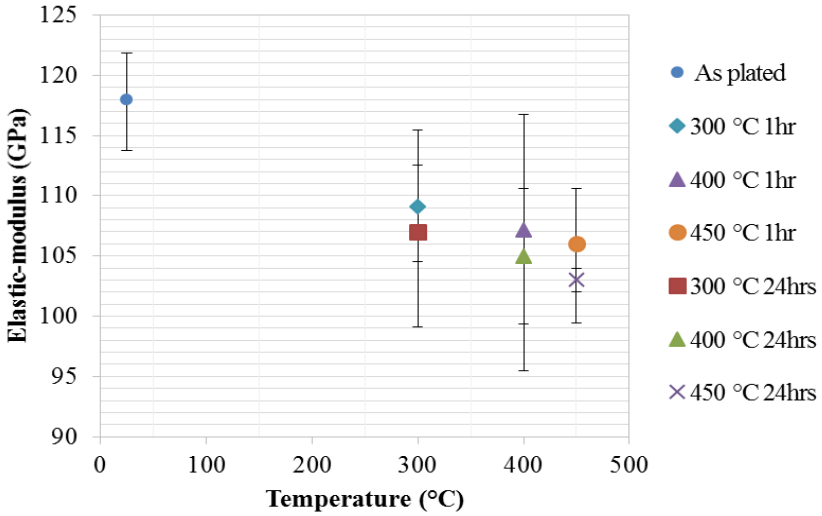


Figure 6.12: Average elastic-modulus values before and after high-temperature annealing

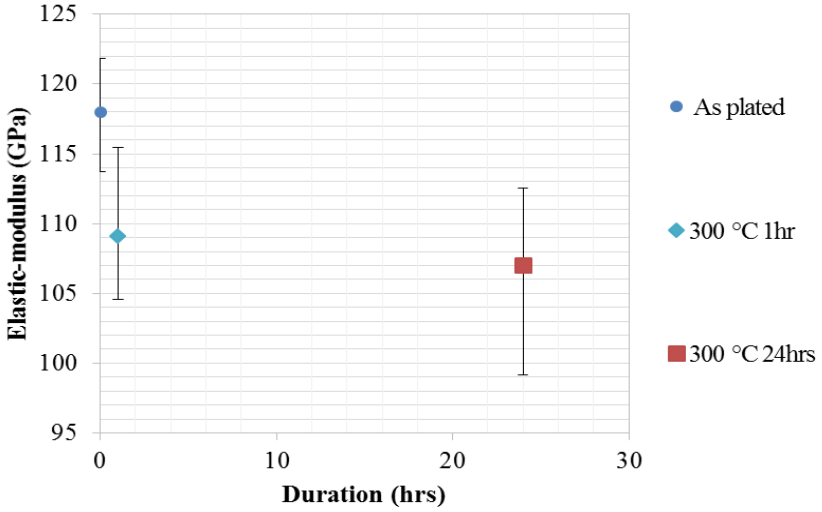


Figure 6.13: Average elastic modulus values before and after 300 °C annealing of different durations

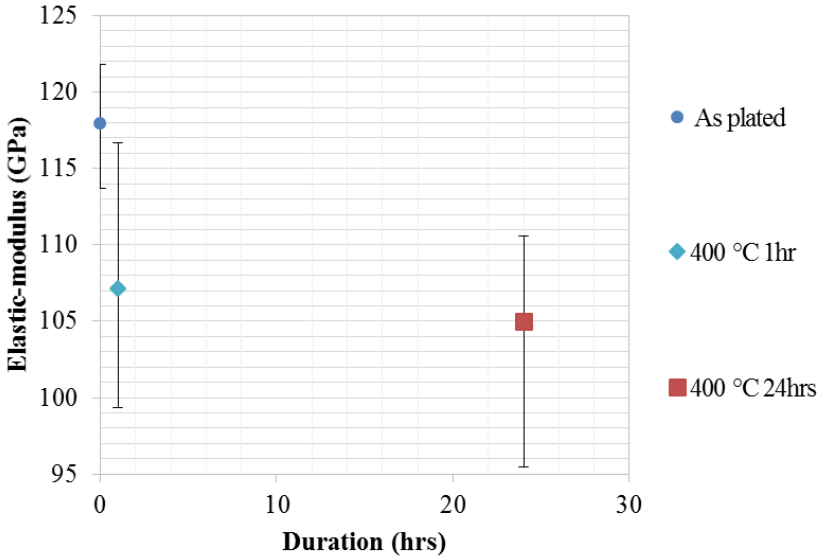


Figure 6.14: Average elastic modulus values before and after 400 °C annealing of different durations

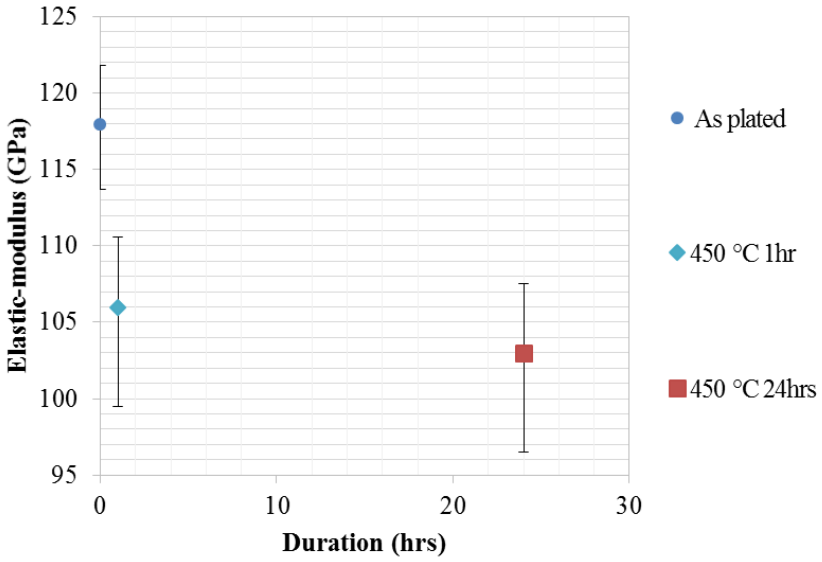


Figure 6.15: Average elastic modulus values before and after 450 °C annealing of different durations

6.3 Sample Preparation for Electron Backscatter Diffraction

The sample preparation process for Electron Backscatter Diffraction (EBSD) uses the same process as the nano-indentation experiment. After polishing, the sample is washed using acetone to dissolve glass glue to release the sample.

6.4 Electron Backscatter Diffraction Experiments

The EBSD experiment set up for copper-plated silicon trenches is the same as that used for copper-filled TSVs. EBSD scan has performed on copper-plated silicon trenches right after they have been plated. Then the samples go through thermal annealing treatment using the Cambridge Fiji Plasma® atomic layer deposition (ALD) tool with the same parameters for copper-filled TSVs. The EBSD experiments uses the same TESCAN SEM® equipment with an EBSD detector. The EBSD scan is taken each time after the same sample goes through 30 minutes, 1 hour, 10 hours and 24 hours high-temperature annealing. There are three samples used for each annealing temperature to make sure there is consistency in the sample conditions used. EBSD experiments are performed for all conditions in Table 6.2. The texture and grain size of copper are compared horizontally and vertically according to Table 6.2.

Table 6.2: Copper-plated silicon trench annealing conditions for EBSD experiment

Temperature (°C) / Duration	RT	300	400	450
As plated	3	N/A	N/A	N/A
30 minutes	N/A	3	3	3
1.5 hours	N/A	3	3	3
11.5 hours	N/A	3	3	3
35.5 hours	N/A	3	3	3

The inverse pole figures (IPF) derived from EBSD measurements for as plated copper-plated silicon trenches is shown in Figure 6.16. The IPF map shows that there are interface lines between grains as shown in the black line in Figure 6.16. This black line divides the cross-section into three sections. The copper-plated silicon trench is electroplated from the bottom and side wall so the grain is grown from the bottom and side wall to the center. As the copper fills up the silicon trench, the interface between the copper grain from the bottom and side walls is formed. Based on this IPF map, it clearly shows the grain is grown along the electroplating direction. The grain is highly orientated to its growth direction which leaves more grain boundaries along the transverse direction of the electroplating direction.

Kim[91] has reported that there has been large discrete resistance jumps at grain boundaries in copper wire structures [91]. Copper-plated silicon trenches is studied to mimic a copper-filled TSVs. The TSV is used as an interconnect to connect chips in

packages, so based on this fabrication process it is expected to have a higher resistance than bottom up plated interconnects.

Figure 6.17 shows the grain map of as-plated silicon trenches. The copper grain is made up by multiple twins. The orientation of the twin is related to the parent through a specific misorientation. The recrystallization twin in a face-centered-cubic material is related to the parent by a 60-degree rotation about the <111> crystal direction. The secondary twin for copper is related to the parent by a 38.9-degree rotation about the <110> crystal direction. Two neighboring points separated by a twin boundary will be considered to belong to the same grain instead of separate grains [92]. The grain grouping algorithm will group all the twins after inputting the twin criterions which gives more accurate data about grain size and distribution. Figure 6.17 shows that the grains close to the bottom and side walls are relatively smaller than the grains at the center. The maximum grain size is found to occur at the center of trench.

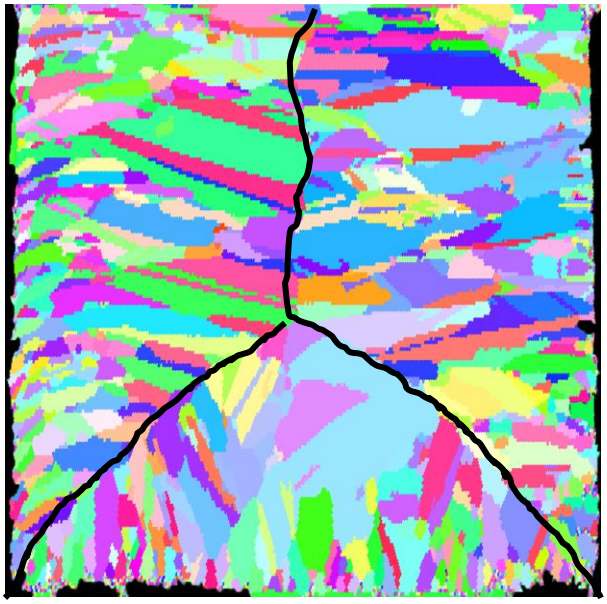


Figure 6.16: EBSD images of as-plated sample shows grain orientation

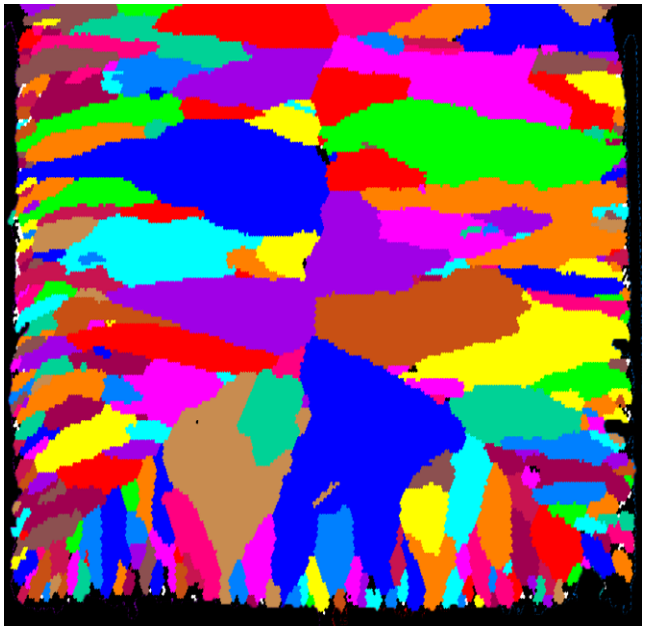


Figure 6.17: Grain map of as-plated sample shows grains

The IPF map and unique grain map is used to compare the copper texture and grain size under different annealing treatment conditions. Figure 6.18, Figure 6.20 and Figure 6.22 show the IPF map for three copper-plated silicon trenches samples before and after 5 rounds of annealing treatment on the same sample. Based on these IPF maps, the orientation of grain is not changed dramatically. Figure 6.19, Figure 6.21 and Figure 6.23 show the grain map for three copper-plated silicon trenches samples before and after 5 rounds of annealing treatments on the same sample. The colors in the grain map are used to distinguish different grains that do not represent grain orientation information. According to the grain map, there is no grain growth observed for all annealing treatment conditions. The average grain size for copper-plated silicon trenches is 15.58 μm in diameter.

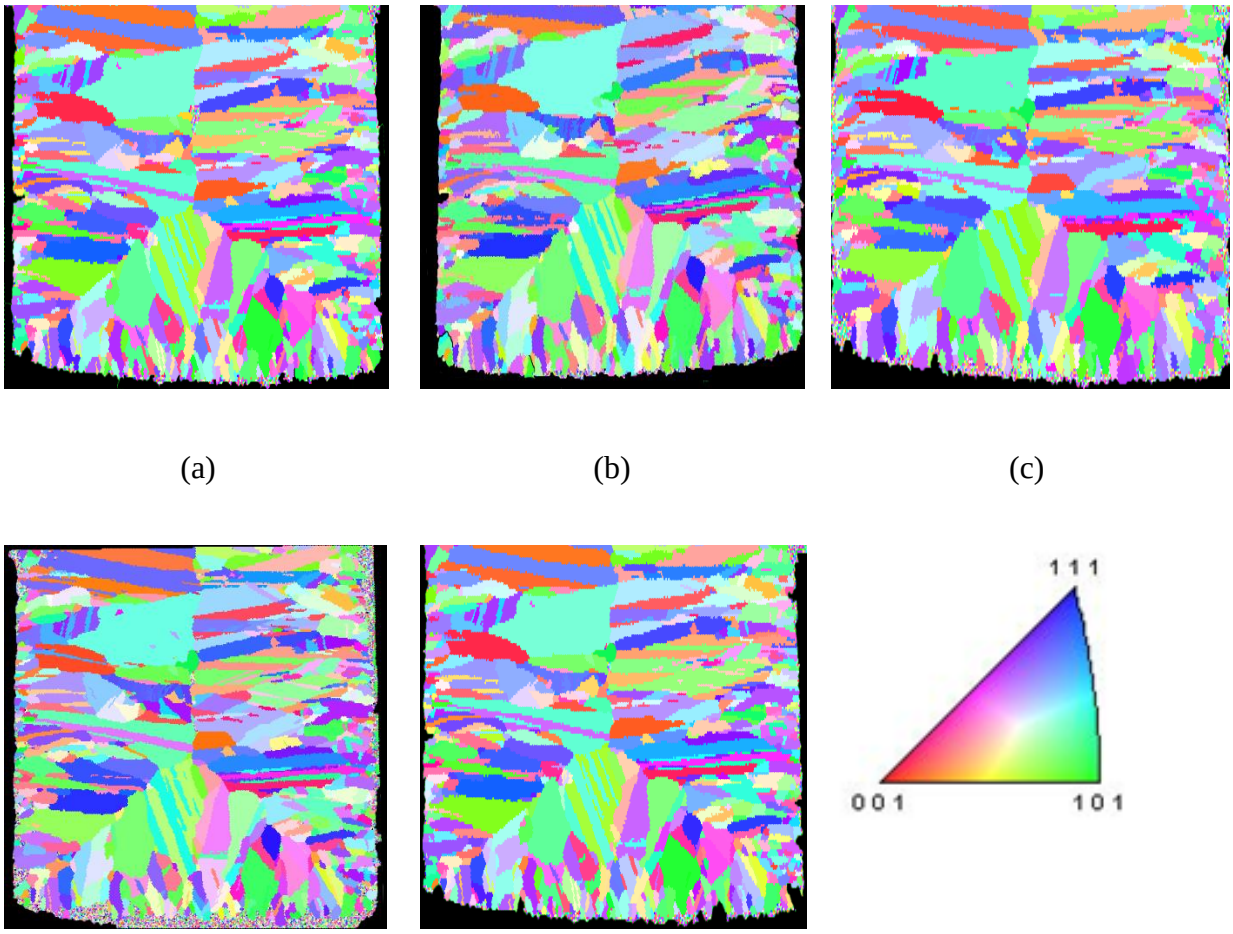
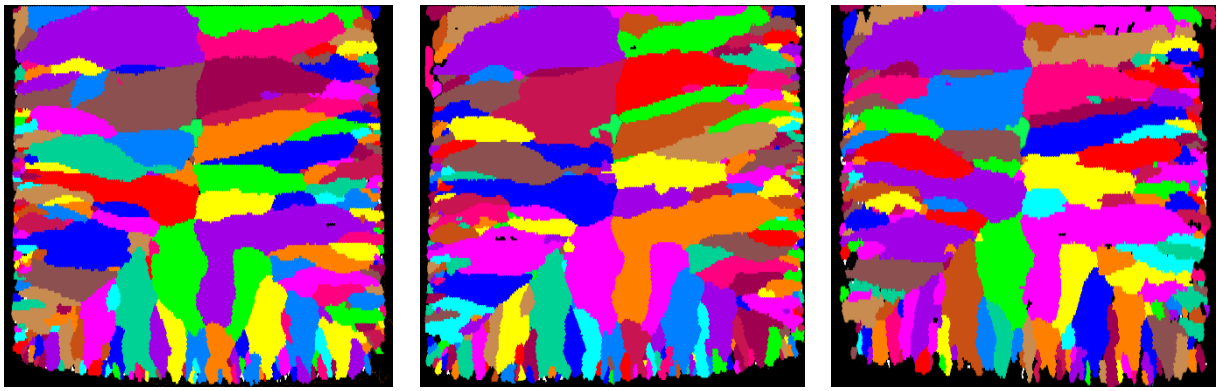
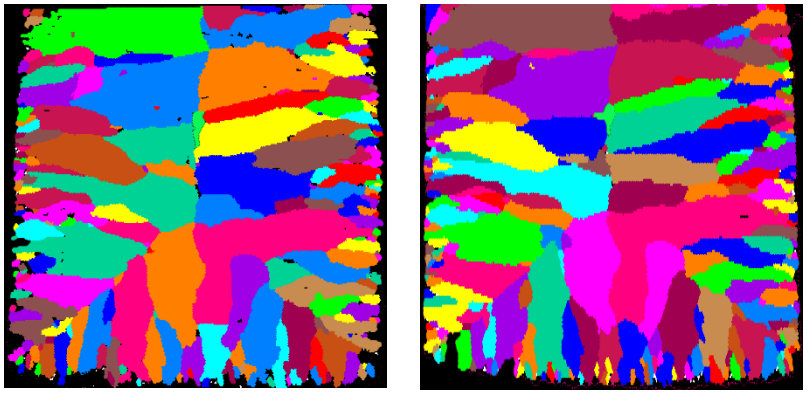


Figure 6.18: EBSD images of annealing temperature is 300 °C (a) As-plated sample, (b) 30 minutes, (c) Additional 60 minutes, (d) Additional 10 hours, and (e) Additional 24 hours



(a) (b) (c)



(d) (e)

Figure 6.19: Grain map of annealing temperature is 300 °C (a) As-plated sample, (b) 30 minutes, (c) Additional 60 minutes, (d) Additional 10 hours, and (e) Additional 24 hours

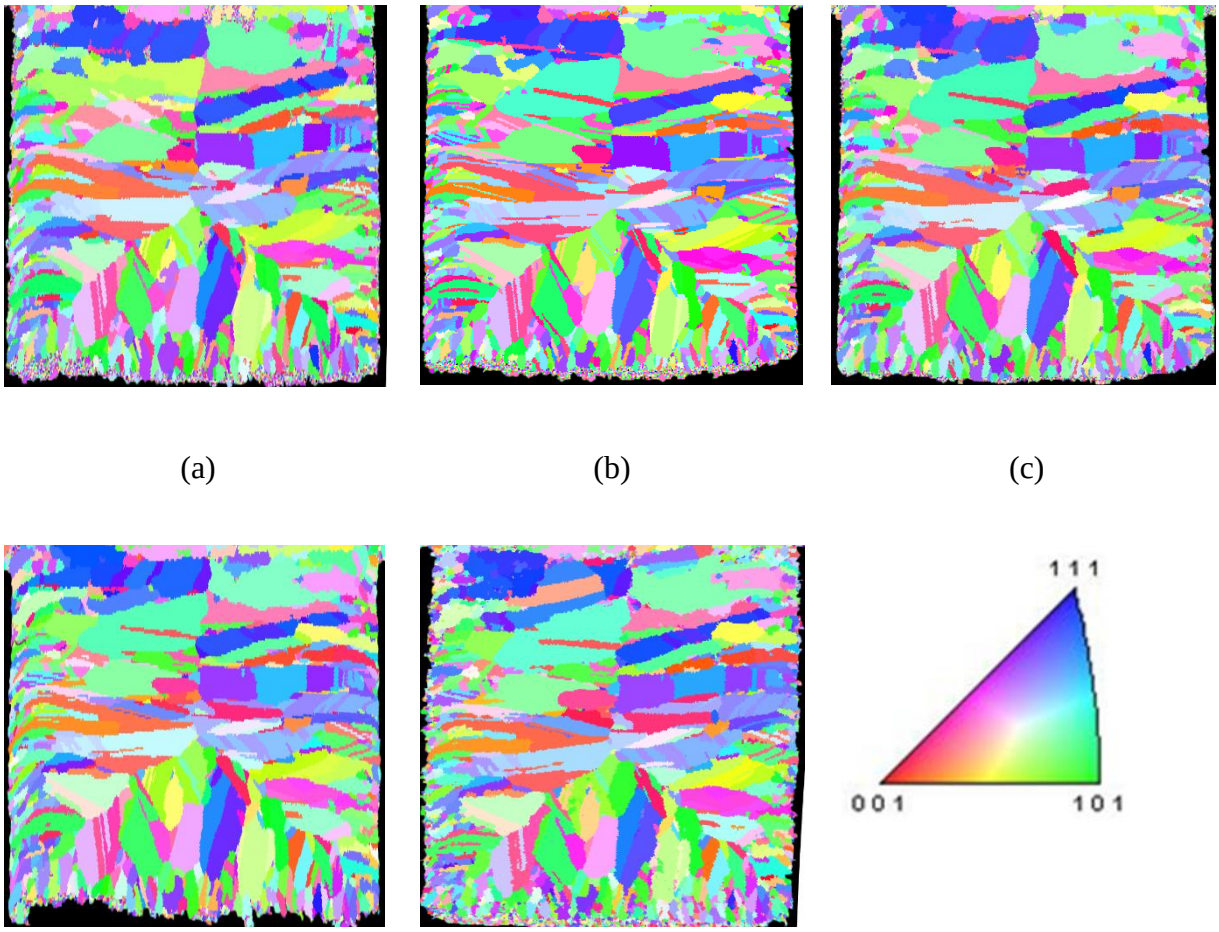
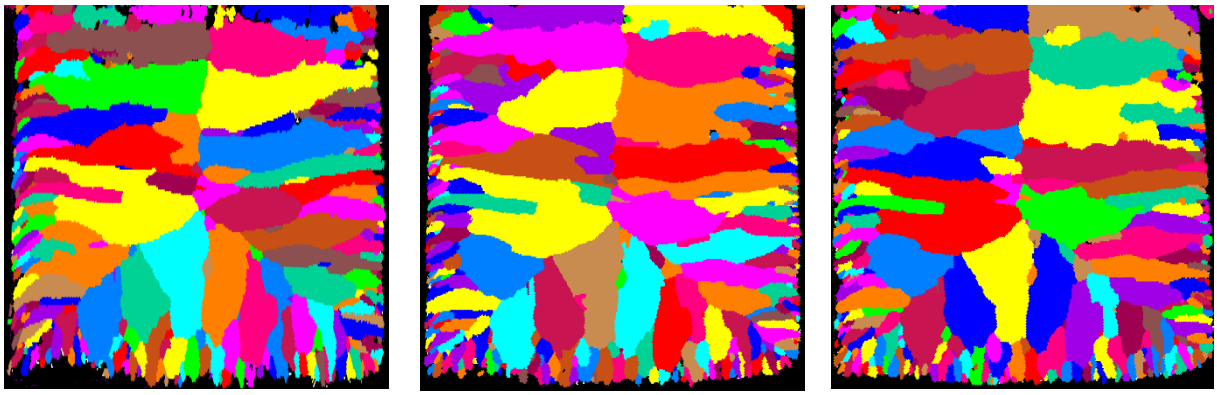
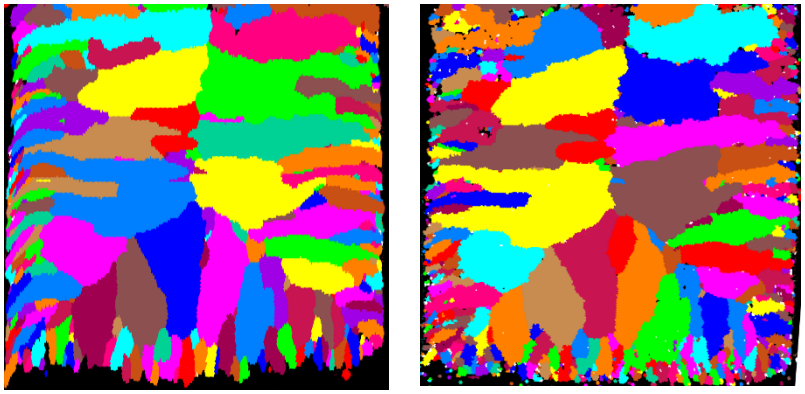


Figure 6.20: EBSD images of annealing temperature is 400 °C (a) As-plated sample, (b) 30 minutes, (c) Additional 60 minutes, (d) Additional 10 hours, and (e) Additional 24 hours

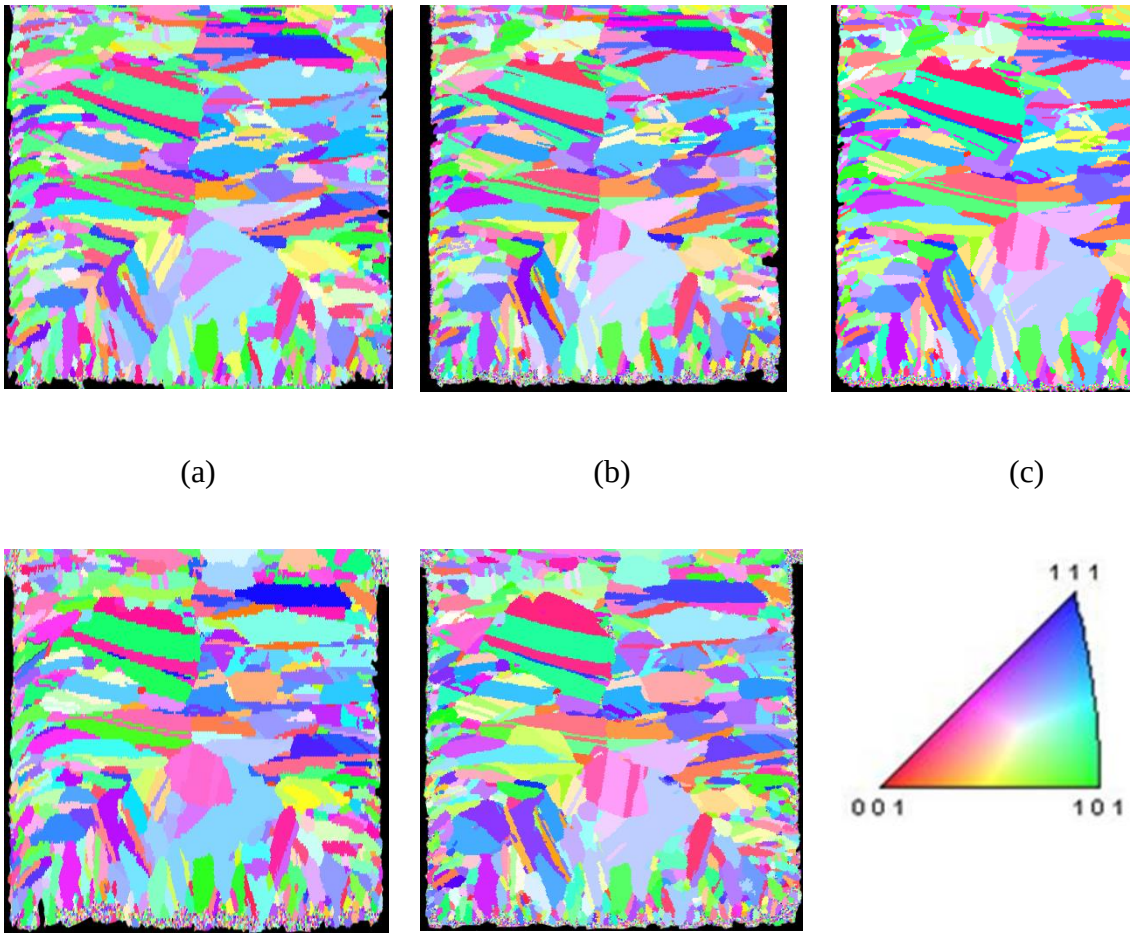


(a) (b) (c)



(d) (e)

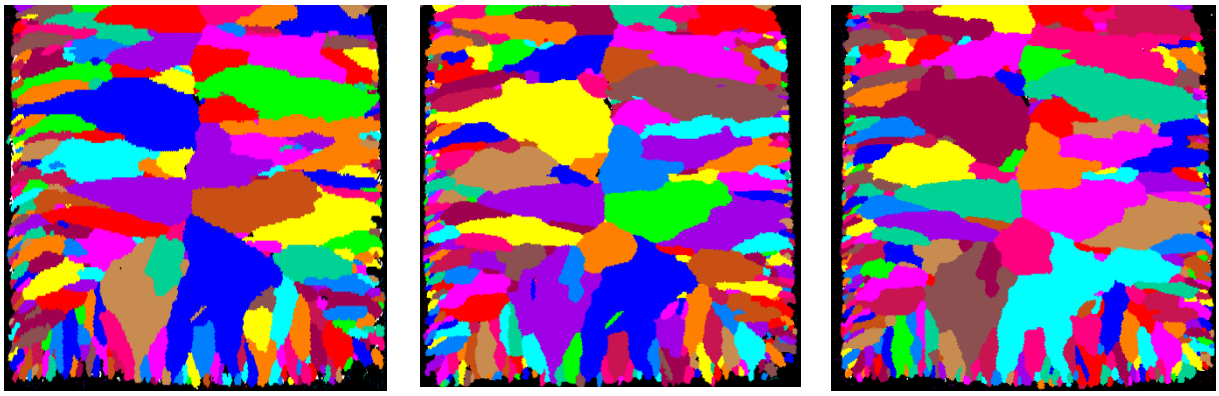
Figure 6.21: Grain map of annealing temperature is 400 °C (a) As-plated sample, (b) 30 minutes, (c) Additional 60 minutes, (d) Additional 10 hours, and (e) Additional 24 hours



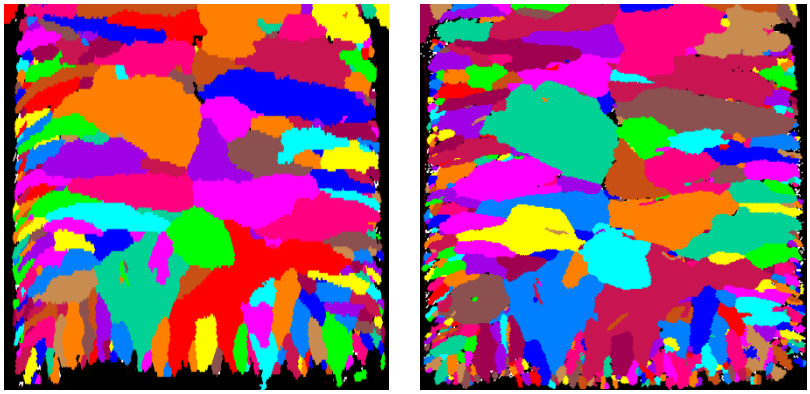
(a) (b) (c)

(d) (e)

Figure 6.22: EBSD images of annealing temperature is 450 °C (a) As-plated sample, (b) 30 minutes, (c) Additional 60 minutes, (d) Additional 10 hours, and (e) Additional 24 hours



(a) (b) (c)

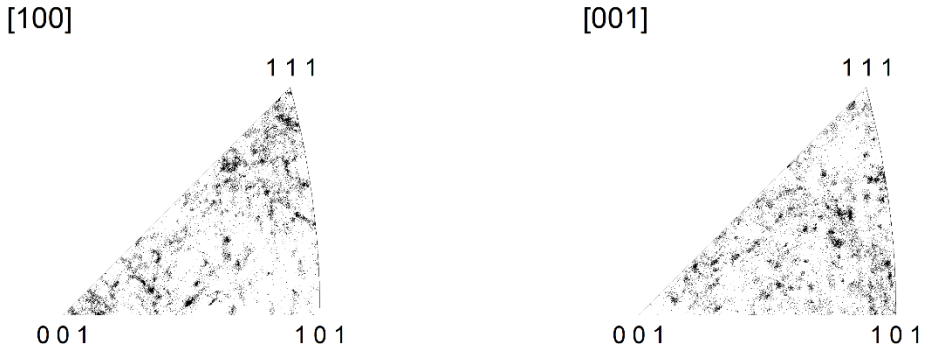


(d) (e)

Figure 6.23: Grain map of annealing temperature is 450 °C (a) As-plated sample, (b) 30 minutes, (c) Additional 60 minutes, (d) Additional 10 hours, and (e) Additional 24 hours

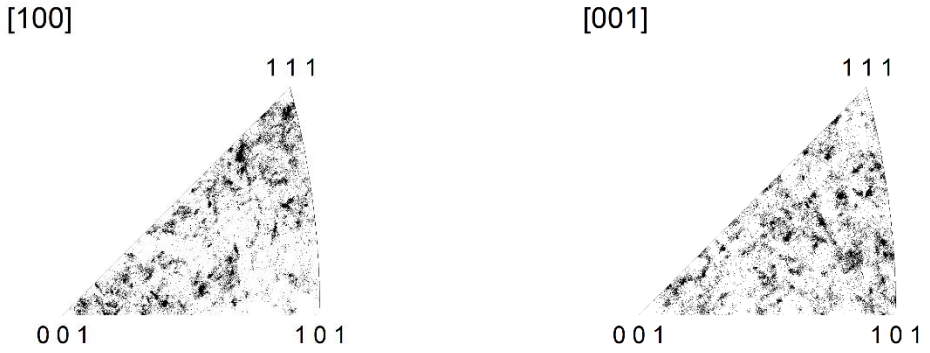
From the IPFs derived from EBSD measurements as shown in Figure 6.24, Figure 6.25, Figure 6.26, Figure 6.27, and Figure 6.28, no preferred texture is observed under the various annealing duration after annealing at 450 °C for different durations Electroplated copper annealed at higher temperatures is expected to see more change in its microstructure. Additional IPFs for different annealing temperatures and durations are

shown in APPENDIX. The grains are observed to exhibit a random behavior all throughout the copper-plated silicon trench length and width.



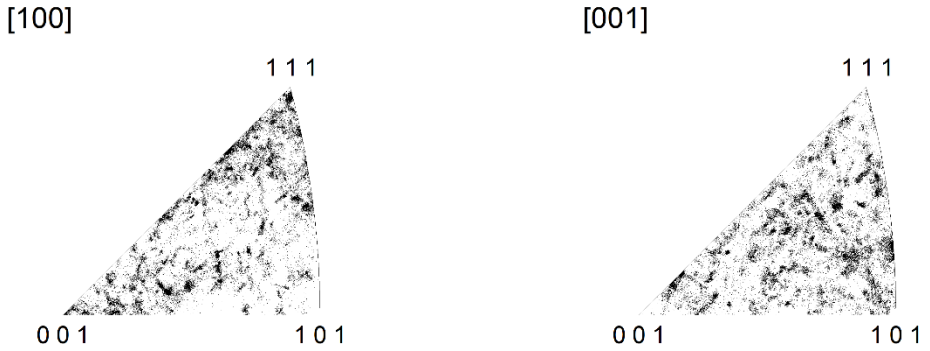
(a) (b)

Figure 6.24: Inverse pole figures for as-plated sample (a) parallel to the copper-plated silicon trench and (b) normal to the copper-plated silicon trench



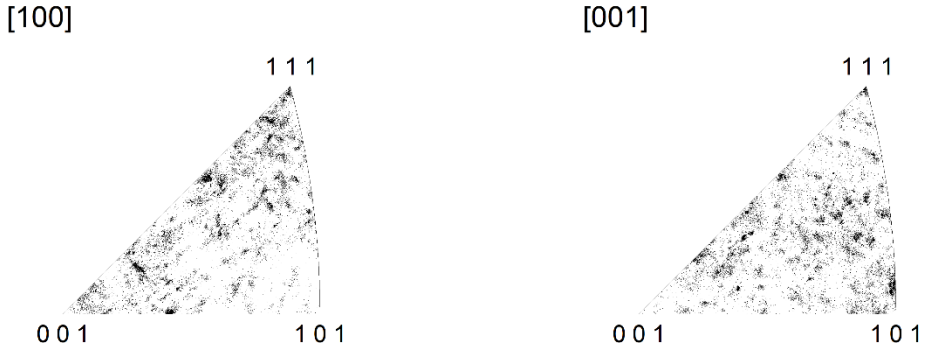
(a) (b)

Figure 6.25: Inverse pole figures for annealed at 450 °C for 30 minutes (a) parallel to the copper-plated silicon trench and (b) normal to the copper-plated silicon trench



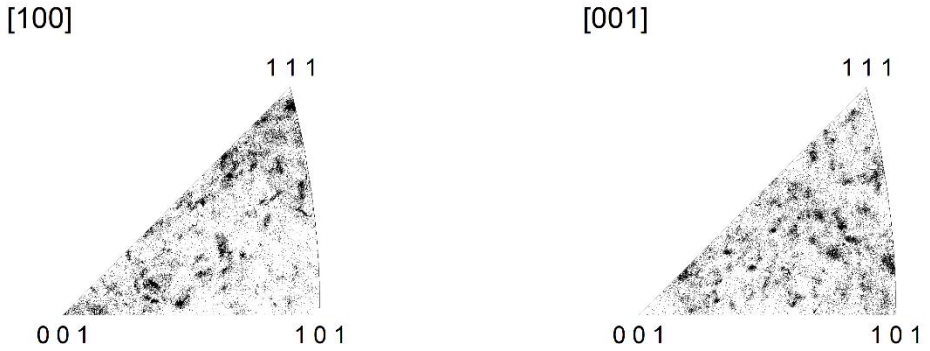
(a) (b)

Figure 6.26: Inverse pole figures for annealed at 450 °C for 1.5 hours (a) parallel to the copper-plated silicon trench and (b) normal to the copper-plated silicon trench



(a) (b)

Figure 6.27: Inverse pole figures for annealed at 450 °C for 11.5 hours (a) parallel to the copper-plated silicon trench and (b) normal to the copper-plated silicon trench



(a) (b)

Figure 6.28: Inverse pole figures for annealed at 450 °C for 35.5 hours (a) parallel to the copper-plated silicon trench and (b) normal to the copper-plated silicon trench

As discussed above, there is no grain growth found in copper-plated silicon trenches. However, there are few studies found that will show copper grain growth after annealing treatment [41-43, 45]. These studies compare different samples before and after annealing treatment. This study compares the same sample and the exact same location before and after annealing treatments are applied. Based on this study no grain growth observed. The electroplating may affect the stability of the copper microstructure. Copper-plated silicon trench is electroplated for 48 hours to fill up the trench. The long electroplating process might affect the copper microstructure stability.

CHAPTER 7. MATERIAL AND GEOMETRY MODELING

This chapter presents the numerical analysis that were conducted to characterize the thermo-mechanical stresses of copper plated trenches. The first section of this chapter focuses on the 2D model based on copper as isotropic material. The second section of this chapter focuses on the 2D model based on copper as anisotropic material. Two models have developed: the grain structure in first model is based on EBSD measurement data and the grain structure in second model is based on Voronoi algorithm.

7.1 Two-dimensional isotropic copper model

A 2D model with isotropic copper is developed as reference to 2D anisotropic copper model. Figure 7.1 shows the schematic of copper-plated trench. Figure 7.4 shows 2D model for copper plated trenches. The dimensions in the model are the same as electroplated copper plated trenches in chapter 6. The bottom silicon and over-plated copper removed in the model. A 2D model with 200 μm silicon shows in Figure 7.3. Comparing 2D model with100 μm and 200 μm, there only have 0.241MPa difference in von Mises stress. To improve computational efficiency and also to capture the detailed stresses in the model. Copper trench width is 100 um and the depth is 100 μm with 1 μm thickness SiO_2 between copper and silicon. Silicon width of 100 μm is modeled, although silicon width is significantly larger than 100 um. The materials properties are listed in Table 7.1 and Table 7.2 . In the models, the left middle node was constrained in the x and y direction to prevent rigid body motion. The assumptions made in this model are: 1) all materials are isotropic, and thus the properties are assumed to be independent of direction or orientation, 2) Si and SiO_2 are assumed to be thermo-elastic, 3) thin barrier Ti and copper

seed layer can be neglected, 4) stress-free temperature for material are taken to be 50°C to mimic plating temperature, and 5) perfect bonding is assumed at all interfaces.

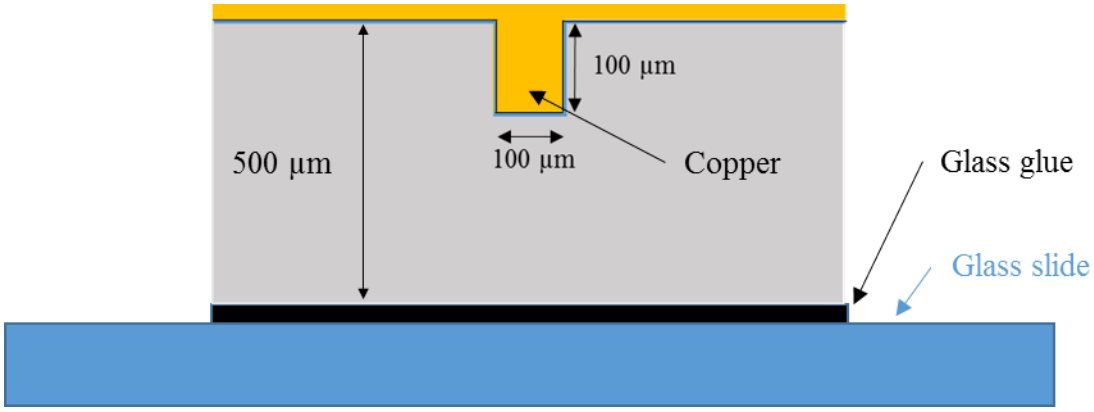


Figure 7.1: Schematic of copper-plated silicon trench

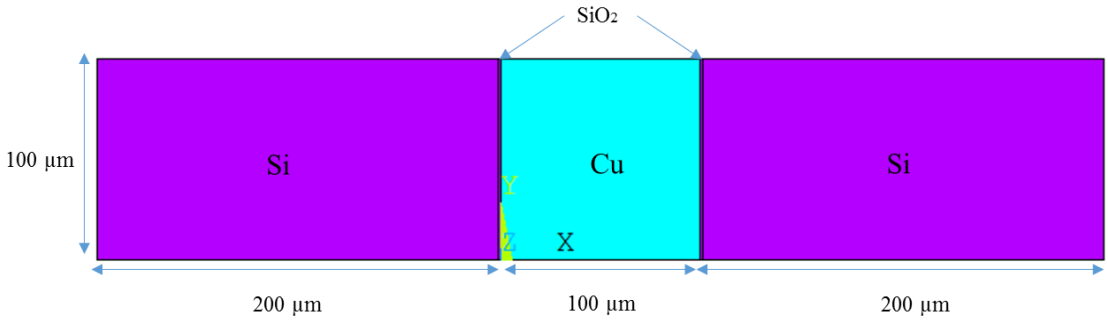


Figure 7.2: 2D isotropic copper model of copper trench with 200 µm silicon

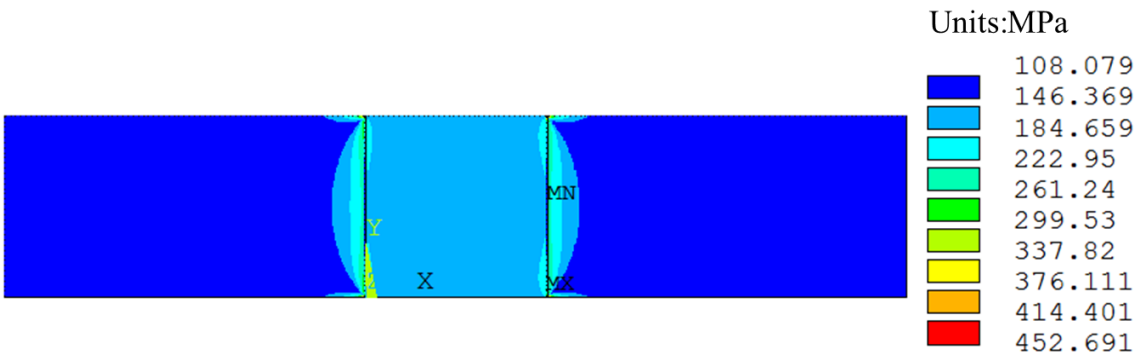


Figure 7.3: von Mises stress in 2D model with 200 µm silicon

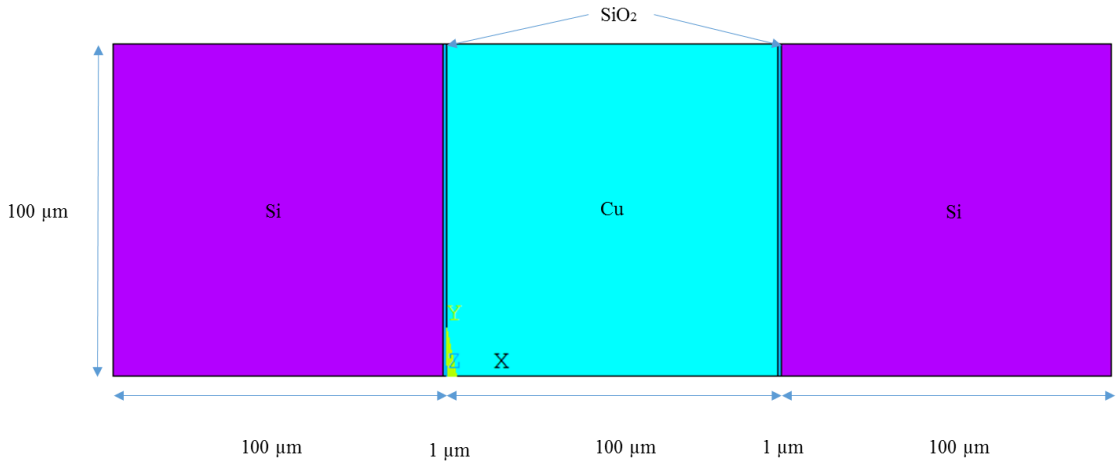


Figure 7.4: 2D isotropic copper model of copper trench with 100 µm silicon

Table 7.1: Material properties [93]

	Cu	SiO_2	Si
Young's Modulus (GPa)	See Table 7.2	71.4	131.00
Poison ratio	0.3	0.16	0.28

CTE (ppm/°C)	17.3	0.5	2.6

Table 7.2: Material properties of Cu [94]

Temperature (°C)	27	38	95
Young's Modulus (GPa)	121.00	120.48	117.88
Temperature (°C)	149	204	260
Young's Modulus (GPa)	115.24	112.64	110.00
Temperature (°C)	27		
Plastic Curve –stress (MPa) vs. strain	121@0.001ε 186@0.004ε 217@0.01ε 234@0.02ε 248@0.04ε		

Thermo-mechanical analysis of electroplated copper trenches is starting with a stress-free temperature of 50 °C and the structure is simulated to be heated to 250 °C. A multilinear kinematic hardening material model is used for copper. The distributions of the

von Mises stress, 1st principal stress and shear stress of the model are shown in Figure 7.5, Figure 7.6 and Figure 7.7. As shown in Figure 7.6 and Figure 7.7, because the CTE of Cu is about 5 times the CTE of Si, Cu tends to expand more than the surrounding Si. This high CTE mismatch results in high stress at the Cu/SiO_2/Si interface. This high stress at interface could lead to dielectric layer failure [3-11, 20, 21, 29-32, 73, 75]. Cohesive cracking of SiO_2, interfacial cracking of Cu/SiO_2 interface needs attention. The plot of 1st principal stress in the dielectric layer (Figure 7.6) near the trench top edge may cause interfacial debonding (Figure 7.7) or crack the dielectric layer.

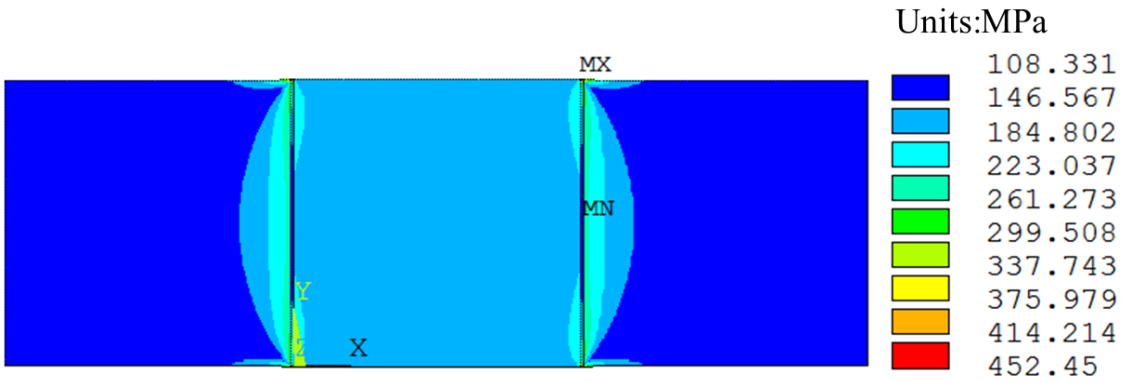


Figure 7.5: von Mises stress

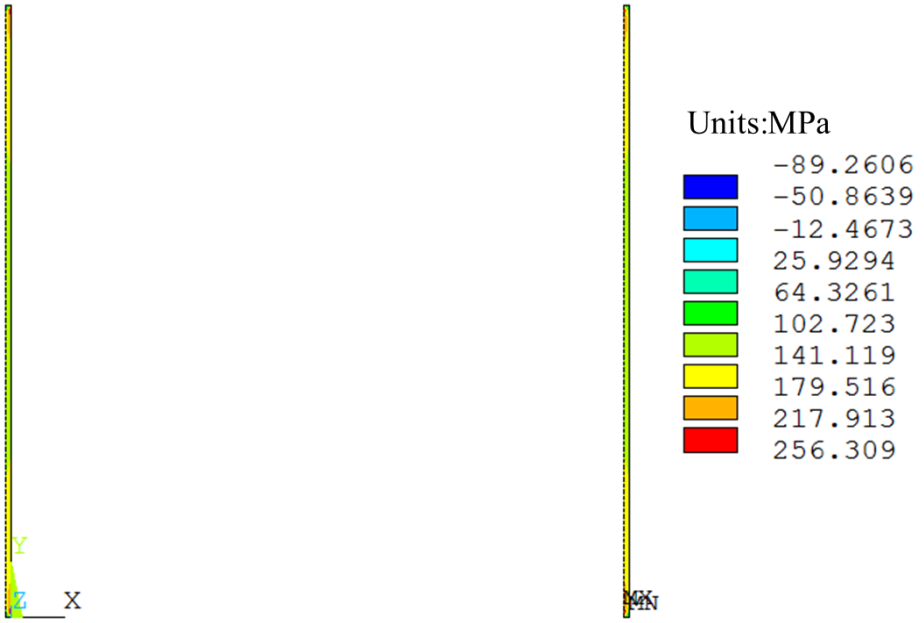


Figure 7.6: 1st principal stress in dielectric layer

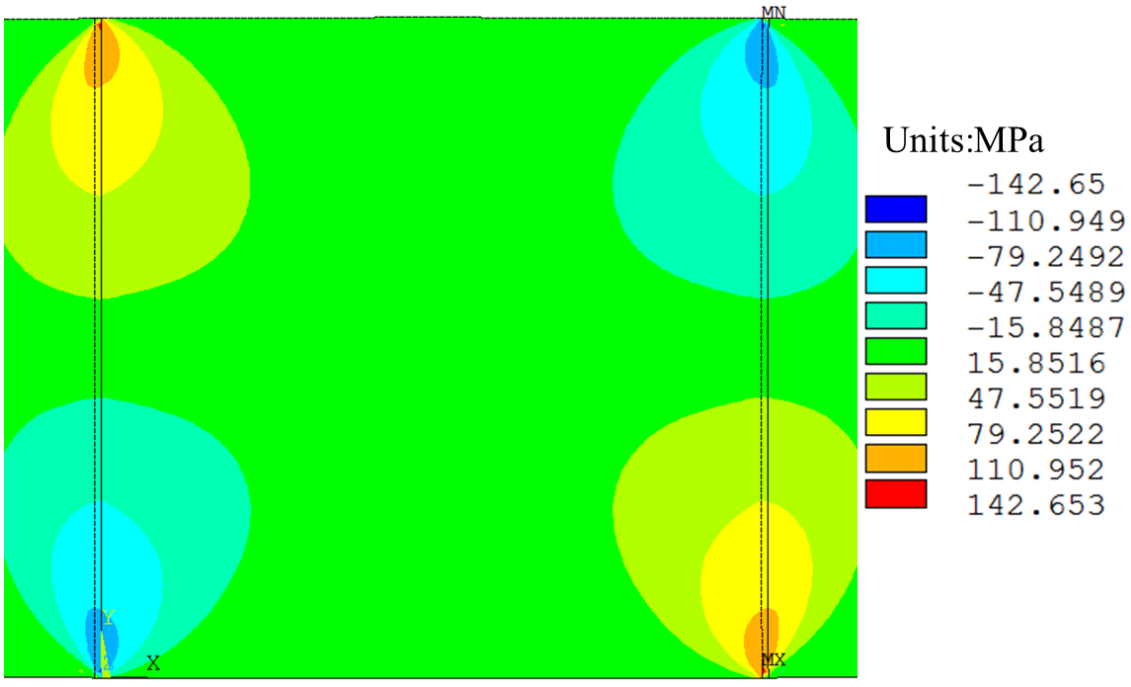


Figure 7.7: Shear stress σ_{xy}

7.2 Two-dimensional anisotropic copper model

In this work, two 2D models with anisotropic copper have developed. The first model is based on the data collected from EBSD measurement. Copper grains in the trench are generated base on the IPF shows in Figure 7.8. The grain orientation are extract from the OIM software and assigned in the model. Figure 7.9 shows the grain structure in FEA model based on EBSD measurement in Figure 7.8. The assumptions made in the model are Si and SiO_2 materials properties are same as isotropic model, perfect bonding is assumed at the grain boundaries and Cu material properties is anisotropic listed are described by Eq. (1) , where C_{11} = 168.4GPa, C_{12} = 121.1GPa, and C_{44} = 75.4GPa.

$$C_{ijkl} = \begin{pmatrix} C_{11} & C_{12} & C_{12} & 0 & 0 & 0 \\ . & C_{11} & C_{12} & 0 & 0 & 0 \\ . & . & C_{11} & 0 & 0 & 0 \\ . & . & . & C_{44} & 0 & 0 \\ . & . & . & . & C_{44} & 0 \\ . & . & . & . & . & C_{44} \end{pmatrix} \qquad (1)$$

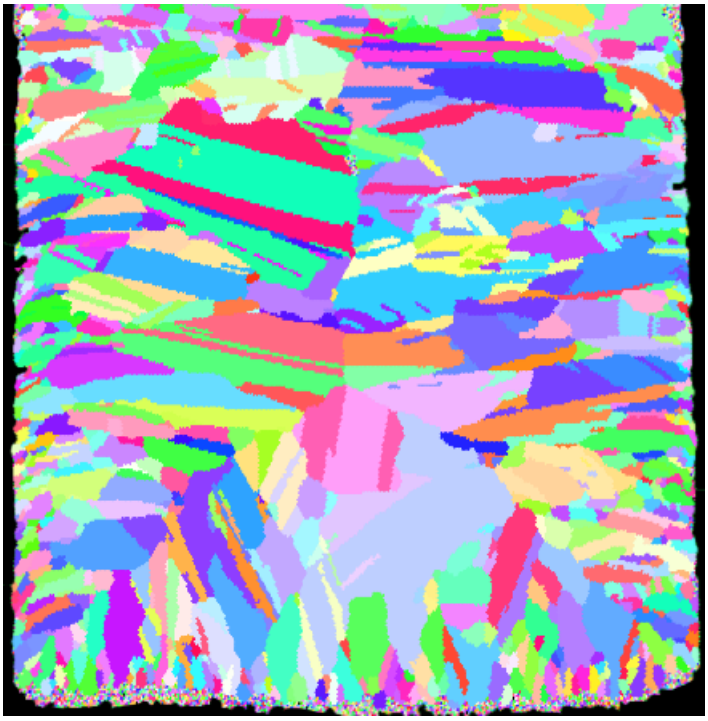


Figure 7.8: EBSD image of the grain structure

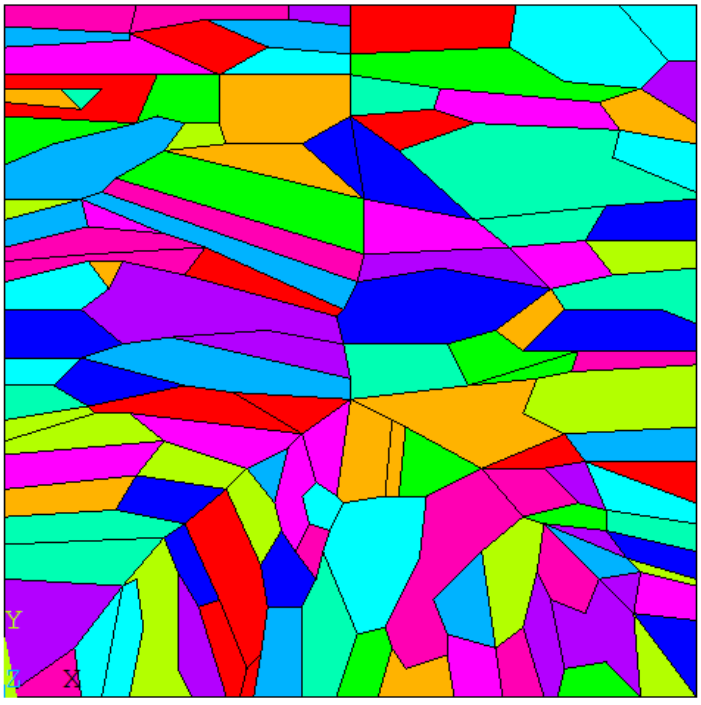


Figure 7.9: FEA model based on EBSD measurement in Figure 7.8

The generalized Hill plasticity model and multilinear kinematic hardening model are used for anisotropic copper models. The Hill yield criterion is an anisotropic criterion that depends on the orientation of the stress relative to the axis of anisotropy. It can be used to model materials in which the microstructure influences the macroscopic behavior of the material. Figure 7.10 and Figure 7.11 shows the von Mises stress in the structure and 1st principal stress at the SiO_2 and Si interface. The maximum 1st principal stress and shear stress in dielectric layer is also located at the corner of the dielectric layer.

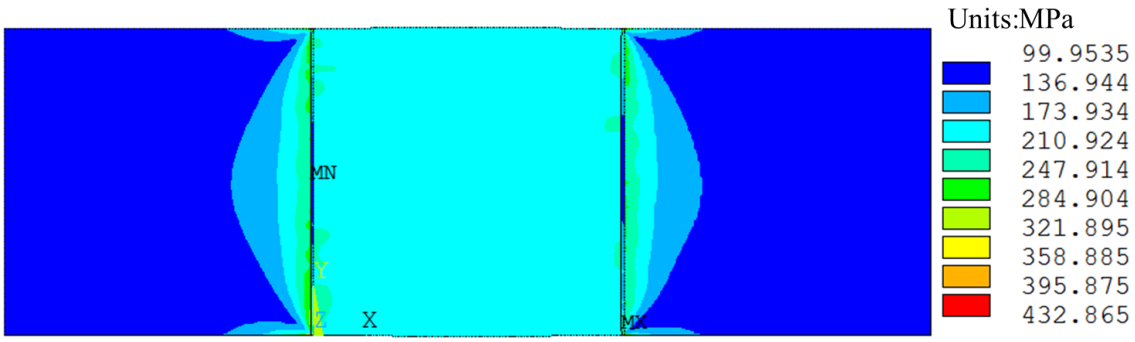


Figure 7.10: Von Mises stress

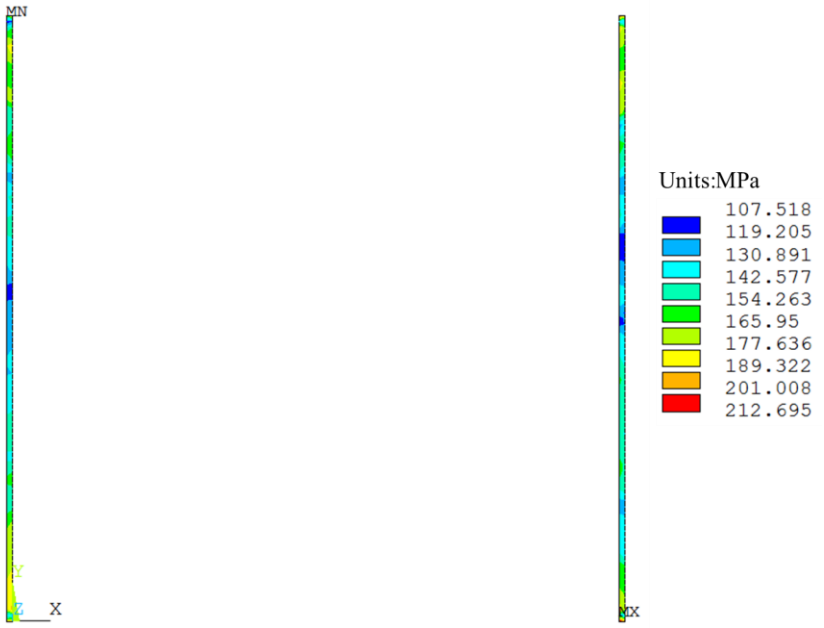


Figure 7.11: 1st principal stress in dielectric layer

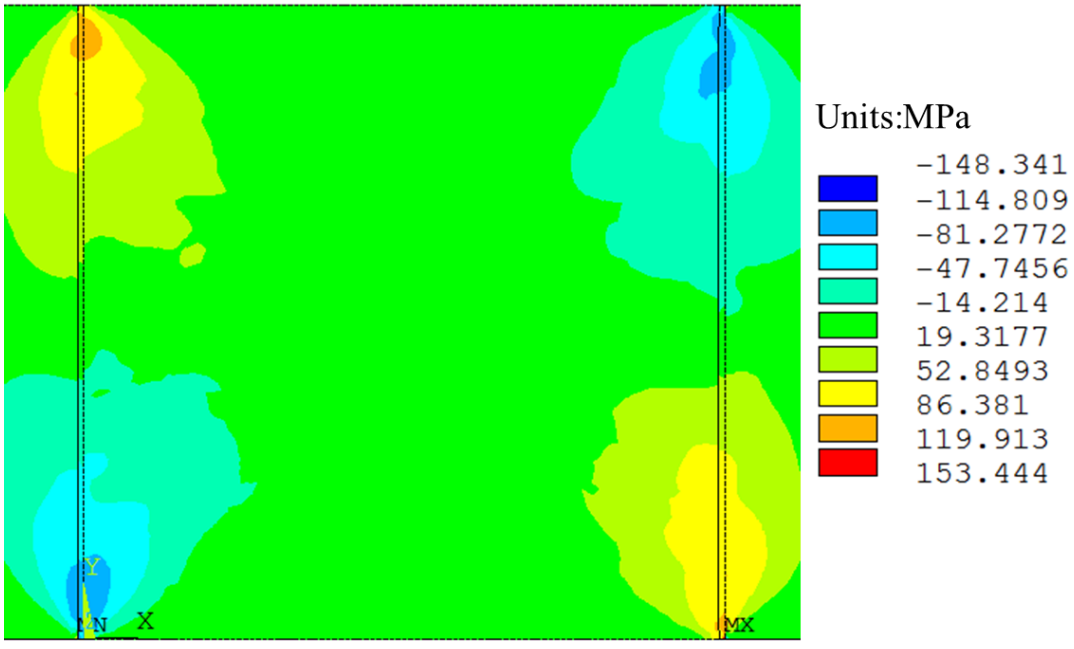


Figure 7.12: Shear stress σ_{xy}

In the second anisotropic copper model, the grain is generated by Voronoi algorithm. Based on the EBSD measurement sample, there are 125 grains constructed copper microstructure. The Voronoi algorithm generated 125 grains shows in Figure 7.13. Based on the EBSD measurement data from chapter 6, there is no preference orientation for copper grains. The grain orientation are random generated by Matlab and assign to 125 grains. Figure 7.14, Figure 7.15 and Figure 7.16 shows the von Mises stress in the structure, 1st principal stress at the SiO_2 dielectric layer and shear stress at the Cu/SiO_2 interface.

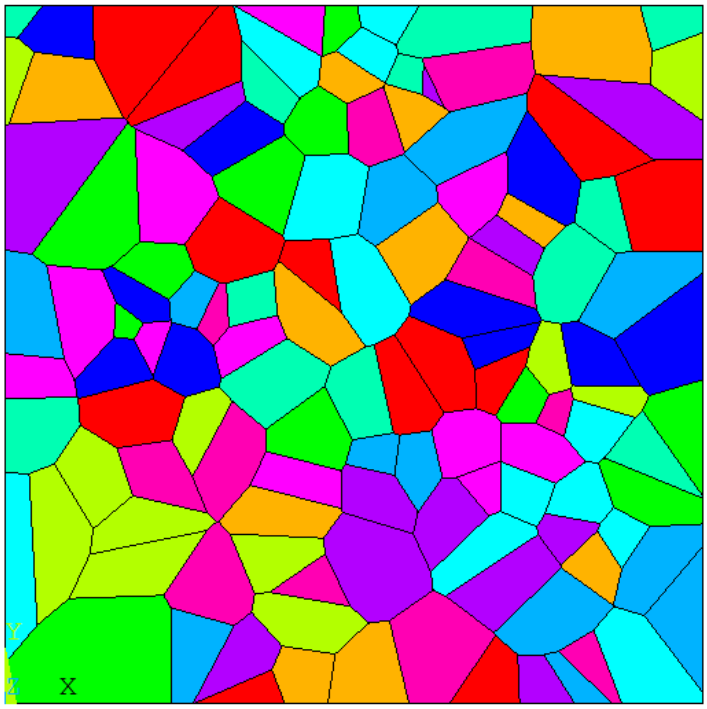


Figure 7.13: Voronoi algorithm generated 125 grains

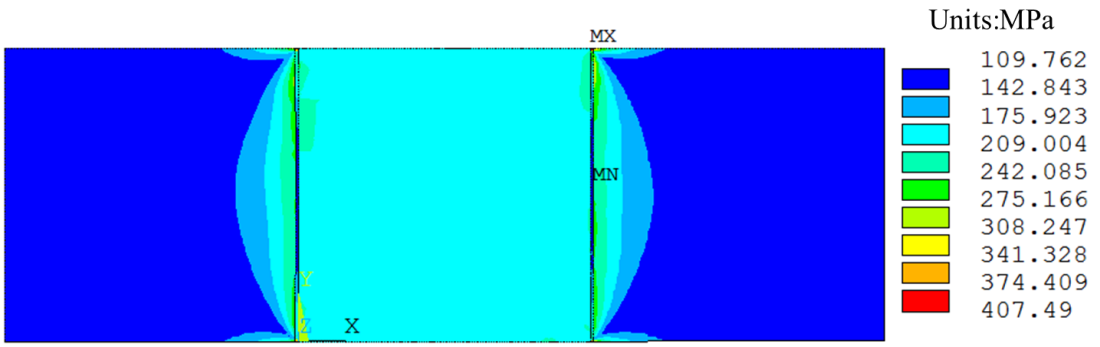


Figure 7.14: Von Mises stress

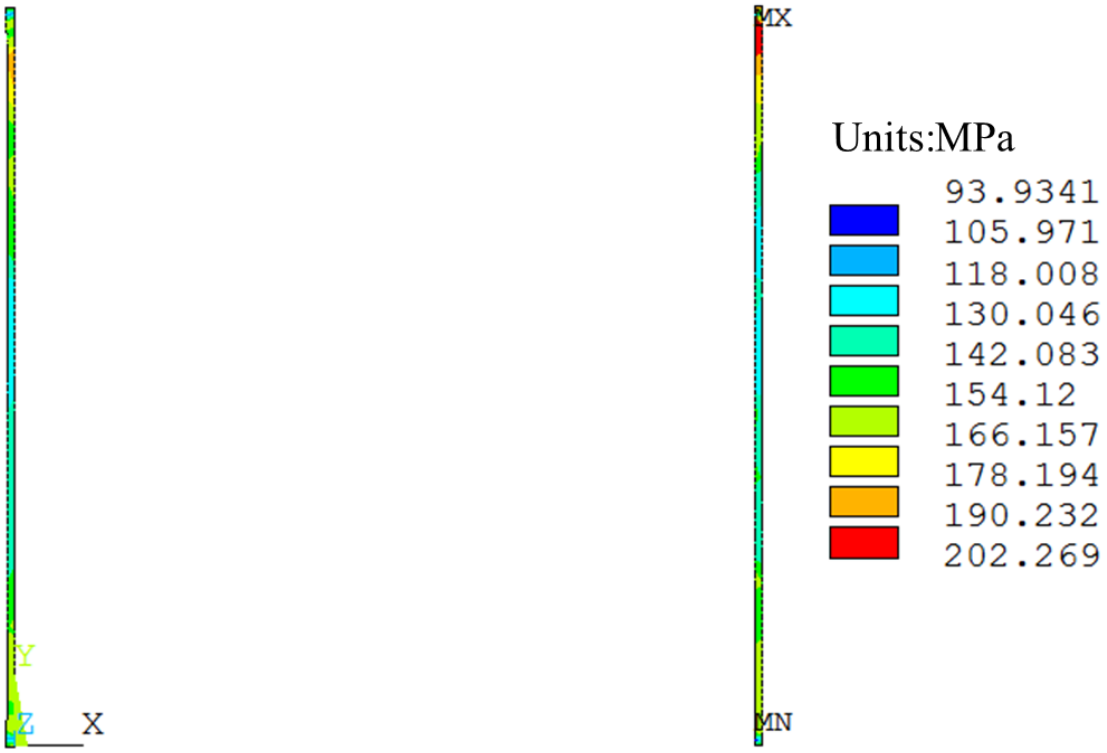


Figure 7.15: 1st principal stress in dielectric layer

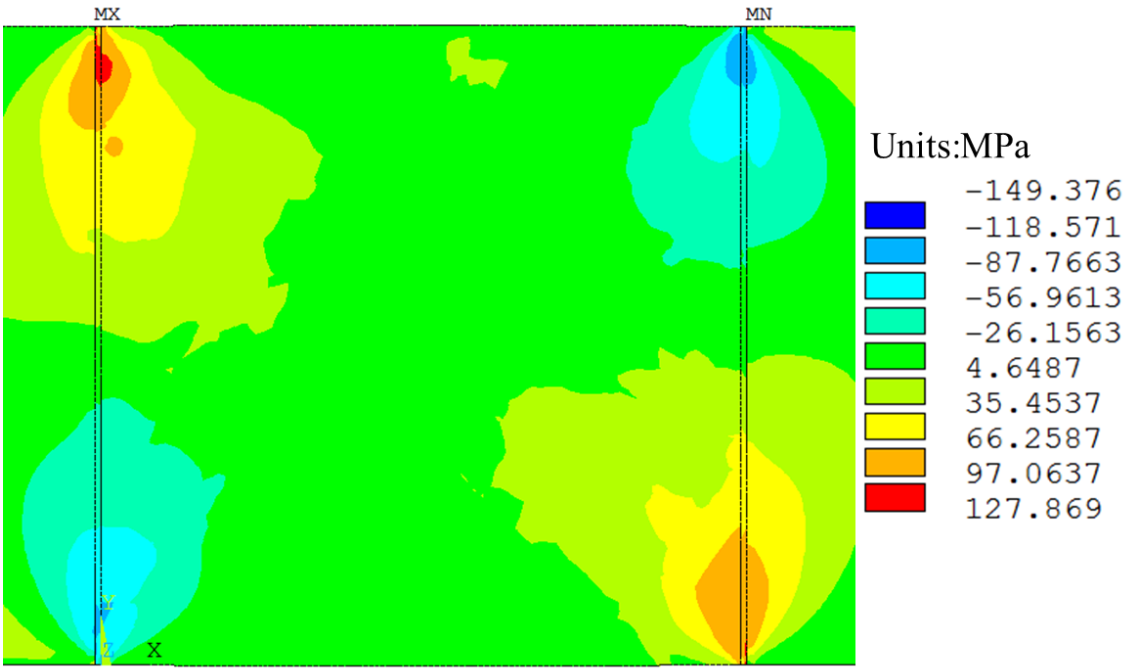


Figure 7.16: Shear stress σ_{xy}

Table 7.3: Maximum von Mises stress in model, maximum 1st principal stress in dielectric layer and maximum shear stress at interface

	Max. von Mises stress (MPa)	Relative change	Max. 1st Principal stress at interface (MPa)	Relative change	Max. shear stress	Relative change
Isotropic model	452.450	/	256.309	/	142.653	/
Model based on EBSD measurement	432.865	-4.3%	212.695	-17.0%	153.444	7.6%

Model based on Voronoi algorithm generated	407.490	-9.9%	202.269	-21.1%	127.869	-10.3%

Table 7.3 compares maximum von Mises stress, maximum 1st principal stress in SiO_2 layer and maximum shear stress at Cu/SiO_2 interface. The stresses are of the same order of magnitude across the three models. In two anisotropic copper models, the copper grains are random distributed based on conclusion from chapter 6. If copper do not have a preferred grain orientation, it is sufficient to use isotropic model to do thermo-mechanical analysis of TSVs and copper-plated trenches. Copper anisotropic model might be valuable when TSVs are small or copper grains have preferred orientation. Under this condition, the stress contours are likely to be different from the stress contours obtained using an isotropic copper model.

CHAPTER 8. CONCLUSIONS AND FUTURE WORK

8.1 Conclusions

Various experimental techniques and numerical analysis have been applied to understand mechanical properties and microstructure of aged copper filled TSVs and electroplated copper trenches.

Room temperature aged copper TSVs were used as samples in this study. After one-year room-temperature aging, no further significant grain growth was observed after high-temperature annealing treatments. After annealing treatments, the hardness and the elastic modulus decreased by 28% and 15% respectively. This reduction could be explained by possible relaxation of residual stresses enabled through the rotation of copper grains.

Electroplated copper trenches have been fabricated and then annealed at high temperatures for different durations. The hardness and the elastic-modulus values decrease as annealing temperature increases and annealing duration increases. The copper trenches cross-section shows the copper grains divided into three sections. This is caused by the electroplating process is from the bottom and side wall. The grain structure did not change before and after annealing at different temperature and durations. The orientation of the grain is random and does not have a preferred direction.

Isotropic and anisotropic models for copper are used to determine the thermo-mechanical stresses in copper in silicon trenches. The anisotropic models have two different bases for the copper microstructure texture. It is seen that the thermos-mechanical

stresses for different models are of the same order of magnitude. This is because the copper grains in the trenches do not have any preferred orientation, and thus, isotropic model is sufficient to do thermo-mechanical analysis of TSVs and copper-plated trenches.

8.2 Future work

This study can be extended in the following aspects:

- The models used in this study are two-dimensional. However, three-dimensional models with 3D grains could offer more insight into the stress distribution.
- It may be possible to fabricate samples with a preferred grain orientation, and such samples could be thermal-aged and the results can be compared against random orientation. Also, the models with preferred grain orientation can provide additional insight into the thermo-mechanical behavior of copper in silicon trenches.
- No thermal cycling effect on grain growth has been studied in this work. This is another possible area of study and exploration.
- This work is primarily limited to copper vias, and it can be extended to other conductive materials in the vias.

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