

ELECTRONIC TRANSPORT AND LOW FREQUENCY NOISE
CHARACTERIZATION IN SI NANOWIRE AND 2-DIMENSIONAL MOS2 BASED
FIELD-EFFECT TRANSISTORS

by

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DEDICATION

This is dedicated to my loving wife Shreya, my two wonderful brothers Roopak and Shivam, and my caring Parents.

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ABSTRACT

ELECTRONIC TRANSPORT AND LOW FREQUENCY NOISE CHARACTERIZATION IN SI NANOWIRE AND 2-DIMENSIONAL MOS2 BASED FIELD-EFFECT TRANSISTORS

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George Mason University, 2014

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The dimensional scaling of Complementary Metal-Oxide-Semiconductor devices for better performance cannot continue indefinitely. One of the predominant factors is the increasing statistical fluctuation with the down-scaling dimensions. As the dimension shrinks, number of free charge carriers within the device decreases. Consequently, statistical fluctuation in the number becomes an increasing fraction of the total free charge carriers, limiting device performance by adversely affecting its electrical transport properties and eventually makes circuit design more challenging.

Low frequency noise (LFN) is one of the major sources of statistical fluctuation in materials. The goal of my work is to study the nature of electrical transport, and the cause/effect of low frequency noise in these reduced-dimension devices. Following is the arrangement of my research project to reach the goal.

First, I designed and installed an efficient and precise noise measurement system based on cross correlation technique. This is crucial because device noise, especially when the current signal is low (which is the case with small dimension devices) can be very difficult to accurately measure since it is affected by many other sources, such as amplifiers, cables, connectors, AC power supplies, mechanical vibrations, etc.

Second, I fabricated and measured Silicon Nanowire field-effect transistors (SiNW FETs). Temperature-dependent (77 K – 300 K) LFN measurement revealed the presence of generation-recombination (*G-R*) related Lorentzian-type peaks along with $1/f$ -type noise in these SiNW FETs. I have successfully detected the presence of electrically active deep-levels associated with Gold and Nickel metals in the SiNWs by using LFN measurements.

Third, I performed temperature dependent (77 K – 300 K) electrical transport and LFN measurement on monolayer layer Molybdenum disulfide (MoS_2) FETs grown by chemical vapor deposition method. The effect of high- κ dielectric passivation on the electrical transport properties revealed key aspects related to activation energy. The observed channel current noise revealed different trapping states in passivated devices when compared to the devices without high- κ dielectric passivation. For both passivated and etched devices, the bias-dependent LFN at 300 K was explained by carrier number fluctuation and correlated mobility fluctuation; both related to surface effects.

Fourth, I studied electrical transport LFN in FETs consisting of different number of MoS_2 layers. Free carrier transport in the channel was explained using a model incorporating Thomas-Fermi charge screening and inter-layer coupling. Based on my

comparative analysis of both electrical transport and LFN on the MoS₂ devices with different number of layers, I found that devices containing 4 to 7 layers may provide the optimum FET performance. Devices with thick MoS₂ suffers from low mobility values, weak dependence of channel current on gate voltage and increase in normalized LFN value, while conduction in mono- and few-layer devices is affected by surface states at oxide-semiconductor interface and therefore, exhibiting much higher LFN and lower mobility values.

In summary, my thesis has presented a study on the electrical transport and low frequency noise of FETs based on Si NW and two-dimensional MoS₂ with focus on understanding the role of defects and surface states on the overall carrier transport.

CHAPTER 1 INTRODUCTION

1.1 Semiconductor: Integral Part of Modern World

There is no doubt that semiconductor electronics has dramatically changed the world we live in. The first documented observation of semiconductor effect was by Michael Faraday (1833) when he noticed that the resistance of silver sulfide decreases with increasing temperature, which was different than the dependence observed in metals. [1] Since then we have made leap and bound progress in utilizing the unique properties of semiconductors. Now, semiconductor devices are integral part of the modern day world, which includes computers, televisions, mobile phones, digital audio players, medical instruments, radar systems, space shuttles, airplanes, and many more. Silicon is used in most of the commercially available semiconductor devices, and dozens of other materials are used as well.

Advancements in various technologies mean that there is a vital need to continuously improve the semiconductor technology. Size of the semiconductor devices are shrinking continuously as predicted by Moore in 1965. [2] Nanoscale devices have opened up a whole lot of new challenges related to the new understanding of physics and novel fabrication processes. A few of the low dimension structures which have attracted great attention recently due to their unique properties are [3-6]

- (a) Quantum dots (QD): It is a 0-dimensional (0-D) structure, confined in all the dimensions. Diameter of these structures is typically in the range of few nanometers (10^{-9} meters).
- (b) Nanowire (NW): It is a 1-dimensional (1-D) structure. These are Solid cylindrical nanostructures, with the diameter of the order of nanometers and length typically in the order of micrometers (10^{-6} meters).
- (c) Nanotubes (NT): It is also considered as a 1-dimensional structure. It is similar to a hollow NW, typically with similar dimensions.
- (d) 2-D materials: As the name suggests, it is a 2-dimensional (2-D) structure. These are nanostructures with thickness less than 2 nm, and have relatively large areas.

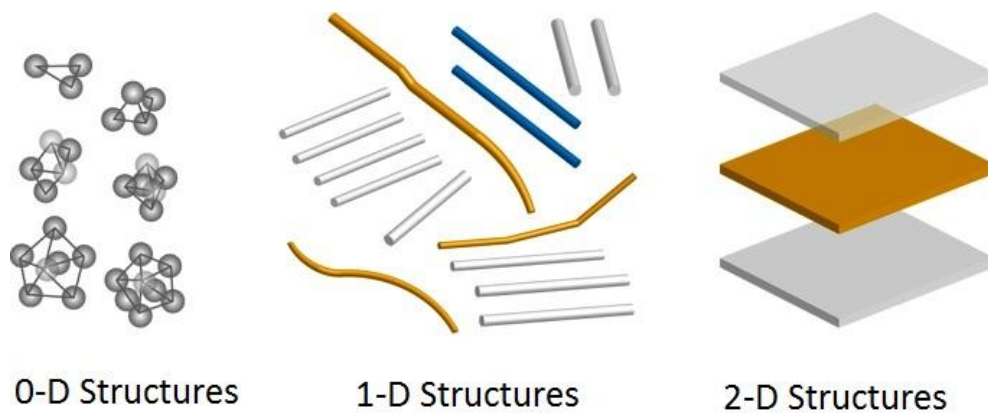


Figure 1 Types of low dimension nanocrystalline materials by size relative to their structural geometry.

1.2 Charge Carrier Fluctuations in Semiconductors

Understanding the true nature of carrier transport in low dimension structures is often challenging. Moreover one of the predominant factors is the increase in statistical fluctuation. As the dimension shrinks, the number of free charge carriers within the device decreases, consequently statistical fluctuation in the number becomes an increasing fraction of the total free charge carriers, limiting device performance by affecting its transport properties. The true nature of these fluctuations depends on the device type, its manufacturing process and operating conditions. These fluctuations are often referred as inherent noise of semiconductor devices and are generally considered as an undesirable effect. Sometimes, inherent noise of a semiconductor device can also be used for the classification of semiconductor devices into groups with different quality and reliability. I have discussed the types of noise observed in semiconductor materials and devices in the following sections.

1.3 Noise

Noise is a fundamental problem in many scientific areas since it cannot be completely eliminated. It limits the accuracy of measurements and sets a lower limit on low level signals that can be detected and processed in an electronic circuit. Characterization of the low-frequency noise in semiconductor devices gives crucial information about the device physics and reliability such as scattering processes, traps and defects. The fundamental noise mechanisms, thermal noise, generation-recombination noise, random-telegraph signal noise and $1/f$ noise, are discussed in the

next. [7] In general, the noise spectrum in a semiconductor device has typically the appearance depicted in figure 2.

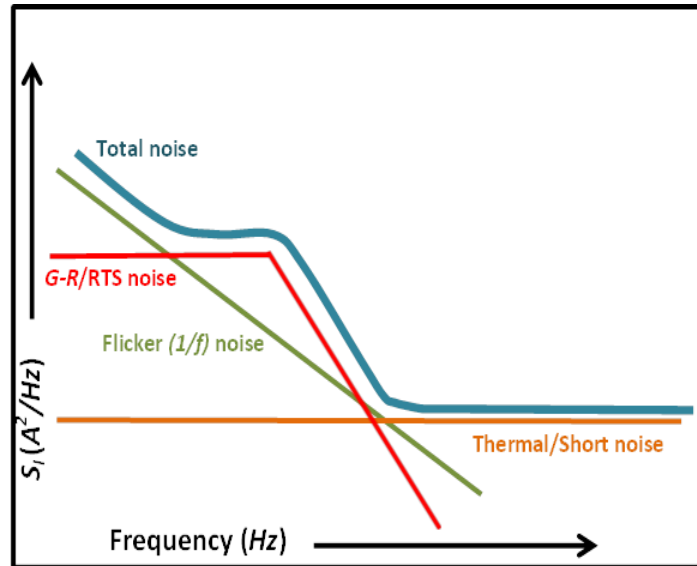


Figure 2 Schematic representation of a general noise spectrum in semiconductor devices. The total noise is a superposition of all the different noise sources. The typical cutoff frequencies are (i) over the THz region for thermal/short noise, (ii) below the GHz region for G-R noise, and (iii) below the MHz region for $1/f$ noise.

1.3.1 Thermal Noise

Thermal noise (Nyquist, Johnson, diffusion, velocity fluctuation noise) stems from the random thermal motion of electrons in a material. Thermal noise is dependent from the random thermal motion of electrons in a material. Thermal noise is dependent on the resistance of the material, but independent of the nature of the material itself. It is also constant with frequency of the applied signal up to microwave frequencies but at higher frequencies the quantum energy of the oscillations becomes comparable with $k_B T$

requiring modification of equation (1). If a material has resistance R and temperature T , the power spectral density, PSD of the thermal noise current ($= S_I$) is given by

$$S_I = 4k_B T/R \quad (\text{or } S_V = 4k_B TR) \quad (1)$$

where k is Boltzmann's constant and S_V is the voltage power spectral density. [8, 9] Thermal noise is intrinsic to any material and sets a lower limit on noise levels in any electric circuit.

1.3.2 Shot Noise

Shot noise in semiconductor devices result from unavoidable random statistical fluctuations of the electric current when the charge carriers like electrons traverse a potential barrier like pn -junction. Current is a flow of discrete charges, and a fluctuation in the arrival of those charges across a potential barrier creates shot noise. The current across a potential barrier is proportional to the number of charge carriers, each carrying a charge q , over a period of time. The current fluctuates with a PSD [10]

$$S_I = 2qI \quad (2)$$

Because the electron has a tiny charge, shot noise is of relative insignificance in most cases of electrical conduction. For example, $1 \mu\text{A}$ of current consists of about 6×10^{12} electrons per second. Even though this number may randomly vary by

several millions in any given second, such a fluctuation is minuscule compared to the current itself. Shot noise is often less significant as compared with other noise sources.

1.3.3 Generation-recombination (*G-R*) Noise

Generation-recombination noise is due to fluctuations in the number of free carriers in a semiconductor device associated with random transitions of charge carriers between different energy states within the forbidden bandgap. Energy states within the forbidden bandgap basically act as traps and exist due to the presence of defects or impurities in the crystal. It represents a typical noise source in semiconductor materials where carrier concentration can vary over many orders of magnitude. Typical examples of transitions are between conduction band and localized levels in the energy gap, conduction and valence bands, etc. Therefore, *G-R* noise is inherently due to fluctuations of carrier number, usually keeping charge neutrality of the sample. The nature of the trap may be neutral or charged in its empty state. Figure 3 shows the types of transitions that occur in a semiconductor resulting in variation in the number of charge carriers.

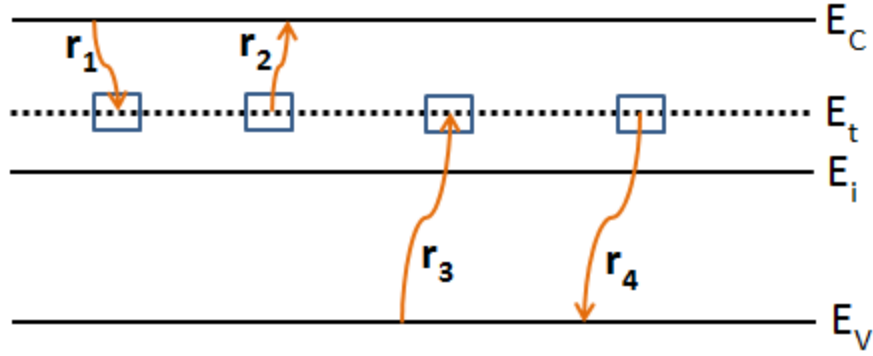


Figure 3 Free carriers can interact with traps by four processes: r_1 electron capture, r_2 electron emission, r_3 hole capture, r_4 hole emission. E_C , E_V , E_i and E_t represents conduction band edge, valance band edge, intrinsic Fermi level and localized trap state (acceptor type) energy level respectively.

These variations in the number of carriers, N lead to changes in device conductance. G - R noise is a function of both temperature and biasing conditions. Variation in N , as a function of time is given by Langevin differential equation,

$$\frac{d\Delta N}{dt} = -\frac{\Delta N}{\tau} + H(t) \quad (3)$$

where ΔN is the fluctuation in the number of carriers, $H(t)$ is a random noise term, and τ is the time constant. The PSD of the carrier fluctuation due to the G - R process can be derived as, [11]

$$S_I(f) = 4\overline{\Delta N^2} \frac{\tau}{1+(2\pi f)^2\tau^2} \quad (4)$$

Here, $\overline{\Delta N^2}$ is the variance of the number of carriers N , f is the frequency. The shape of the spectrum given by equation (4) is Lorentzian in nature (same as figure 4(b)). From equation (4), it is clear that when $2\pi f\tau \ll 1$, the spectrum becomes independent of frequency, while at high frequencies well above the corner frequency ($f_0 = 1/2\pi\tau$) where, $2\pi f\tau \gg 1$ the spectral density falls off with $1/f^2$. The location of the trap level is crucial in determining the presence of a $G-R$ noise. When the trap level is very close to the Fermi-level (within a few $k_B T$ in energy), the capture time τ_c and the emission time τ_e are almost equal and the $G-R$ noise is prominent. If the Fermi-level is far above or below the trap level, the trap will be filled or empty most of the time and consequently a few transitions takes place that produce noise. When there are several $G-R$ centers with different carrier life times, the resultant noise spectrum will be a superposition of several distributions (discussed in section 1.3.5).

1.3.4 Random Telegraph Signal (RTS)

In devices with relatively small areas, very few traps remain within a few $k_B T$ of the Fermi level, and these give rise to RTS noise (burst, popcorn noise). RTS noise is a special case of $G-R$ noise which is displayed as discrete switching events in the time domain (figure 4). [7] The PSD for the RTS noise and the $G-R$ noise are both of the Lorentzian type. The capture time and emission time, as well as the magnitude of the voltage or drain current fluctuations determine the characteristics of the RTS noise. When an electron is captured by a trap, the current switches to the lower value and remains at the same state as long as the electron remains trapped. When the trapped electron is

released, the current jumps to the high value and remains at the same state as long as another electron is captured by the trap. For two-level pulses with equal height ΔI and Poisson distributed time durations in the lower state τ_l and in the higher state τ_h , the PSD of the current fluctuations is derived as, [12]

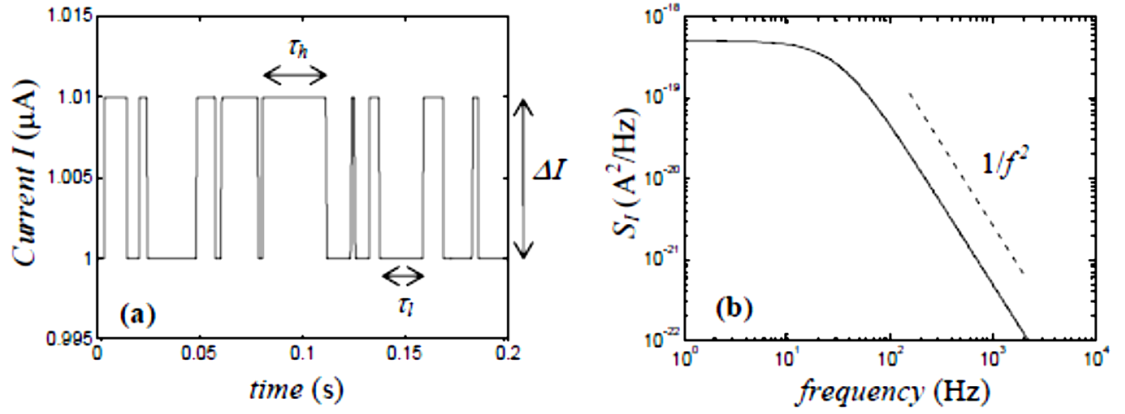


Figure 4 (a) RTS noise in time domain. (b) Lorentzian shaped power spectral density of the fluctuations in the time domain plotted vs. frequency.

$$S_I(f) = \frac{4(\Delta I)^2}{(\bar{\tau}_l + \bar{\tau}_h) \left[\left(\frac{1}{\bar{\tau}_l} + \frac{1}{\bar{\tau}_h} \right)^2 + (2\pi f)^2 \right]} \quad (5)$$

RTS noise is a special case of *G-R* noise where only one kind of trap level is present. It also depends on the location of the trap center with reference to the Fermi level with centers in close proximity of Fermi levels giving rise to *RTS* noise. Statistically it can be shown that *RTS* noise is a result of single carrier, controlling the flow of a large number of carriers instead of a large number of carriers being involved in the

trapping/detrapping process. [13] *RTS* noise characterization can give important information about the trap energy, capture and emission kinetics and spatial location of the trap. *RTS* noise has significant effect at low frequencies. It is a function of temperature, induced mechanical stress, and radiation. In audio amplifiers, the *RTS* noise sounds as random shots, which are similar to the sound associated with making popcorn. Also, the *RTS* behavior in sub-micrometer area MOSFETs, originating from trapping and de-trapping of an electron provides a strong base to support the carrier fluctuation model, explained in the next section.

1.3.5 $1/f$ Noise

$1/f$ noise (flicker noise) is the most dominant noise in the low frequency range. This noise is present in all semiconductor devices under biasing and cannot be eliminated completely. This kind of noise is usually associated with material failures or with imperfections of a fabrication process. $1/f$ noise PSD is proportional to $1/f^\gamma$ with γ close to 1, usually in the range 0.7-1.3. The PSD for $1/f$ noise is given by

$$S_I = \frac{KI^\beta}{f^\gamma} \quad (6)$$

where K is a constant and β is a current exponent. $1/f$ fluctuations in conductance have been observed in the low-frequency part of the spectrum (10^{-6} to 10^6 Hz) in most of the conducting materials and in a wide variety of semiconductor devices [14-16]. From equation (6) it is clear that there are essentially two physical mechanisms behind any

fluctuations in current (since current can be given by equation (12)). i.e., fluctuations in the number of carriers and fluctuations in the mobility of carriers. Based on these fluctuations, there are two major models of $1/f$ noise:

- Surface model developed by McWhorter in 1957 [17]
- Bulk model developed by Hooge in 1969 [18]

According to McWhorter model, $1/f$ noise spectrum can be generated by superposing many different $G-R$ noise spectra, where free carriers are randomly trapped and released by centers with different time constants. To produce $1/f$ noise like spectrum, the time constants of the traps have distribution function as, [19]

$$a(\tau) = 1/\ln(\tau_2/\tau_1) \tau \text{ for } \tau_1 < \tau < \tau_2, \quad a(\tau) = 0 \text{ otherwise} \quad (7)$$

where $\ln(\tau_2/\tau_1)$ is used for the normalization. The superposition of the $G-R$ noise from traps distributed according to $a(\tau)$ will result in PSD given by:

$$S_{tot}(f) = \int_0^{\infty} a(\tau) S_{G-R}(\tau) d\tau = \frac{1}{\ln(\tau_2/\tau_1)} \int_{\tau_1}^{\tau_2} \frac{1}{\tau} \frac{K\tau}{1 + (2\pi f\tau)^2} d\tau \quad (8)$$

$$= \frac{1}{\ln(\tau_2/\tau_1)} \frac{K}{2\pi f} [\arctan(2\pi f\tau)]_{\tau_1}^{\tau_2} \quad (9)$$

$$S_{tot} = \frac{K}{4\ln(\tau_2/\tau_1)f} \quad \text{for} \quad 1/2\pi f\tau_2 \ll f \ll 1/2\pi f\tau_1 \quad (10)$$

An example is given in figure 5, where $G-R$ noises from six distinct traps with different time constants add up to a $1/f^\gamma$ spectrum. This model assumes that traps are isolated from each other and capture or emission of charge carriers by one does not affect the capture and emission of the other. If interaction occurs, $G-R$ noise is obtained with a time constant given by the reciprocal sum of all time constants. [20] It is also assumed that the traps couple in the same way as the output current (same K value for all traps).

The second explanation for $1/f$ noise is based on mobility fluctuations, given by Hooge and has originally been formulated for metal films. [18] According to Hooge, the $1/f$ noise is a bulk effect. Generally, there are two dominant scattering mechanisms of charge carriers; scattering on the crystal lattice and scattering on impurities. In this model it is assumed that only scattering on the crystal lattice is the origin of the $1/f$ noise, while scattering on the impurities has no effect on $1/f$ noise. All imperfections of the crystal lattice leads to large $1/f$ noise. The PSD for the Hooge model is given by

$$S_I = \frac{\alpha_H}{f^{\gamma_N}} I^\alpha \quad (11)$$

The dimensionless parameter α_H , referred to as the Hooge constant, was first suggested to be constant and equal to 2×10^{-3} . Later, it was found that α_H depends on the crystal quality.

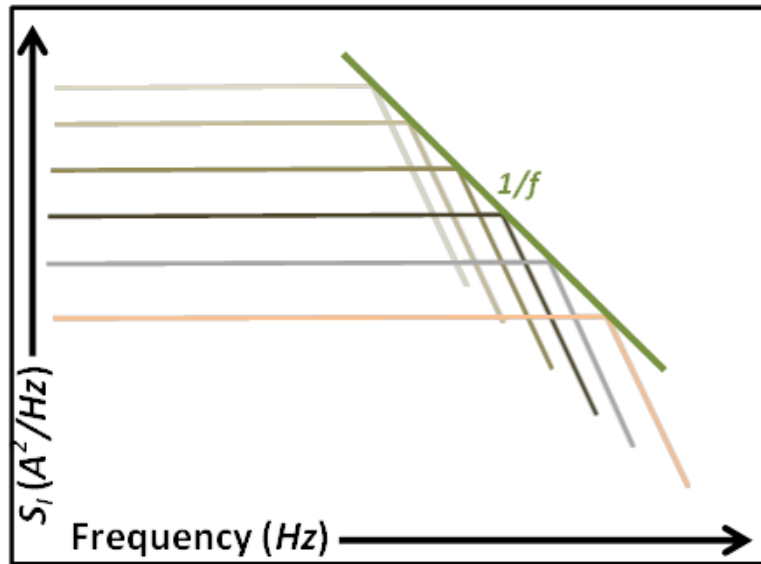


Figure 5 Superposition of different Lorentzians (6 are shown here) can produce $1/f$ like spectrum.

There is enough evidence to suggest that $1/f$ noise in metals and bulk semiconductors is dominated by mobility fluctuations. [16] In case of MOS-transistors where current flows in close proximity of surface under the gate oxide, most experimental data point to traps in the gate oxide as the dominant $1/f$ noise source; although in case of p -channel MOSFETs the mobility fluctuation noise model tends to better explain the origin of $1/f$ noise. [21-24]

There are several other models and theories explaining the origin of $1/f$ noise. Hung proposed a unified model where he proposed that $1/f$ noise in MOS transistors can be completely explained by trap charge fluctuation mechanism, which produces mobile carrier number fluctuation and correlated surface mobility fluctuation. [25] Unified model was further improved by Ghibaudo. [26] This idea can be attributed to Jayaraman

and Sodini, their model is often used as the basis for circuit simulations. [27] Quantum noise theory was proposed by Handel. [28, 29] This theory explains $1/f$ noise as fluctuations in the electron scattering due to infrared photon emission. This theory was criticized by both practical and theoretical researchers. [30, 31] A survey paper by Van Vilet discusses the history and critical review of quantum $1/f$ noise research. [32] Another mobility fluctuation noise theory was proposed by Musha and Tacano, it suggests that energy partition among weakly coupled harmonic oscillators in an equilibrium system is subjected to $1/f$ fluctuations. [33] Jindal and Van der Ziel suggested that the phonon population exhibits $G-R$ noise which is transferred to mobility fluctuation noise through a fluctuating phonon scattering. [34] Other ideas like inelastic tunneling process involving excitation of phonons for the origin of both the mobility and number fluctuation noise are also suggested. [35]

In addition to these fundamental or intrinsic noise sources, there are other noise sources across different frequency ranges. These include noise from the AC power line (and its harmonics), AM and FM broadcast stations, TV broadcasts, microwaves, etc. Noise from these sources is generally called interfering noise or non-essential noise sources because they can be minimized with good laboratory practices.

1.4 Low-frequency Noise in Nanoscale Devices

The higher demand for semiconductor devices with smaller area, higher speed and lower costs have led to a tremendous geometrical downscaling of devices. Higher density leads to more functionality on a smaller area at a lower cost, but at the same time scaling has a tremendous impact on low frequency noise. This can be shown from the $1/N$ factor

in the Hooge relation [18], since smaller geometries means lower number of carriers N . The normalized current noise in MOSFETs scales with $I/(WL)$, W and L being the width and length of the transistor. [36] For bipolar transistors, the normalized current noise scales with I/A_E , where A_E is the emitter area [37-39]. Therefore, there is a physical noise limit to geometrical downscaling of semiconductor devices.

The current noise is the superposition of several noise sources with different spatial location and different physical origins. The lower limit of noise is generally set by (white) thermal noise. In addition to the thermal noise, $1/f$ noise always exists, and G - R noise can also be present, especially in MOSFETs with a very small gate area ($\sim 0.1 \mu\text{m}^2$). The current density in n-type bulk semiconductor is given by

$$J = \sigma E = (qn\mu_n + qp\mu_p)E \approx nq\mu_n E \quad (12)$$

If n fluctuates ($n = N/V$, where V is the volume), the current density fluctuates as

$$S_J(f) = \frac{S_I(f)}{N^2} J^2 \quad (13)$$

Thus, S_J decreases with increasing N as $1/N^2$. The variation of the PSD with the number of carriers is one way to distinguish the noise originating from traps or from the noise related to the fluctuations in the mobility.

1.5 Low-frequency Noise in Circuits

The RF and analog circuits design requires several considerations and trade-offs such as gain, power dissipation, linearity, noise, speed, voltage swings, input/output

impedance and supply voltage. [40] The complexity of the RF design requires specialized characterization and accurate modeling of the RF devices. On the other hand digital circuits are primarily optimized by the trade-off between speed and power consumption. [41, 42]

In order to realize the potential of digital and analog circuit applications of devices, the impact of fabrication technology on the device performance has to be examined. It is well known that processing issues can result in undesirable threshold voltages and $1/f$ noise values. [43, 44] For deeply-scaled devices $1/f$ noise becomes even bigger concern as it is proportional to the reciprocal of the device area. [36] $1/f$ noise puts a limitation on RF circuit design as it gives rise to phase noise in oscillators, amplifiers and mixers. [45-50] Hence, to alleviate the design constraints imposed by the device noise, it is essential to examine the $1/f$ noise characteristics affected by the device design.

1.6 Noise Characterization

The measurement of noise is a complex task as the noise signal is usually very weak (down to ~ 1 pA). Moreover, a DC bias current is usually present as well as the disturbances from electronic equipment, which complicates the task even more. The measurement setup must be designed carefully with appropriate shielding and preferably using batteries as power sources to avoid disturbances to be injected in the circuits. The typical low-frequency noise measurement setups used in this thesis are described in section 1.6.1. The measurements are performed in the frequency domain by measuring the power spectral density with a spectrum analyzer.

1.6.1 Measurement Setup

The low-frequency noise in this work was typically measured using the two configurations depicted in figures 6 and 7.

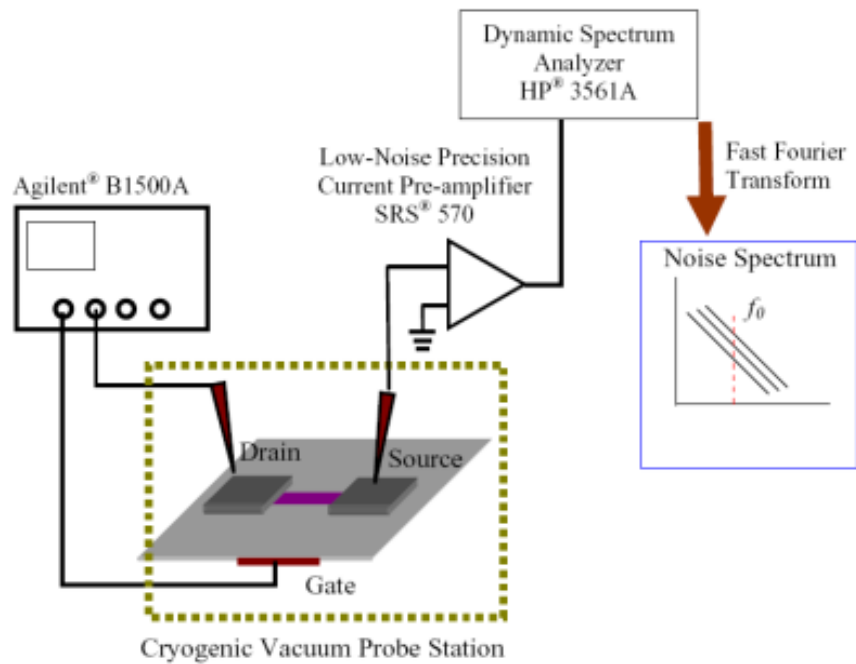


Figure 6 Schematic representation of the conventional single-channel LFN measurement setup.

1.6.1.1 Single-Channel Noise Measurement Setup

Figure 6 represents single channel convention noise measurement setup. In our case, the LFN measurement was done in an open-cycle cryogenic probe station. The drain and gate bias was provided by the Agilent B1500A semiconductor parameter analyzer, and the channel current was amplified and converted to voltage using SRS 570

low-noise current amplifier. The voltage output from the amplifier was connected to a HP 3561A dynamic signal analyzer. Note that the setup in figure 6 is operated with a low-noise current amplifier, which amplifies the current through its low-impedance input and gives a voltage at the output amplified by the trans-impedance gain G . The amplifier inevitably adds noise to the circuit. Therefore, the internal noise of the amplifier sets the measurement limit of the system and must be minimized. The requirements on a good low-noise amplifier to be used for sensitive noise measurements include properties such as ultra-low front end internal noise.

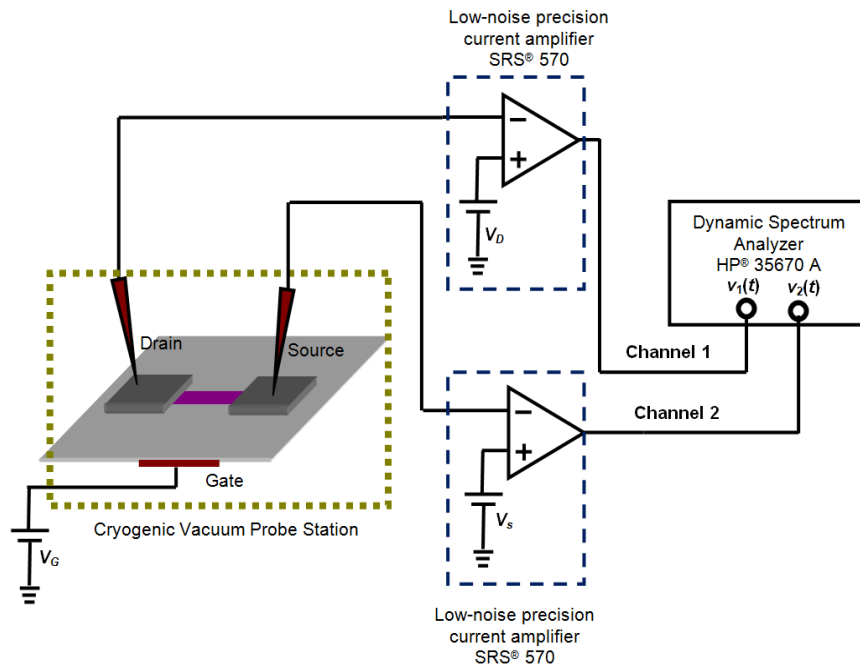


Figure 7 Schematic representation of the double-channel cross spectrum LFN measurement setup.

In single channel noise measurement system as shown in figure 6, the accurate measurements of the noise signal in low-current devices such as nanoscale FETs are challenging because the device noise, which is proportional to the dc current, becomes comparable with the instrumental noise of the measurement setup.

1.6.1.2 Double-Channel Correlated Noise Measurement Setup

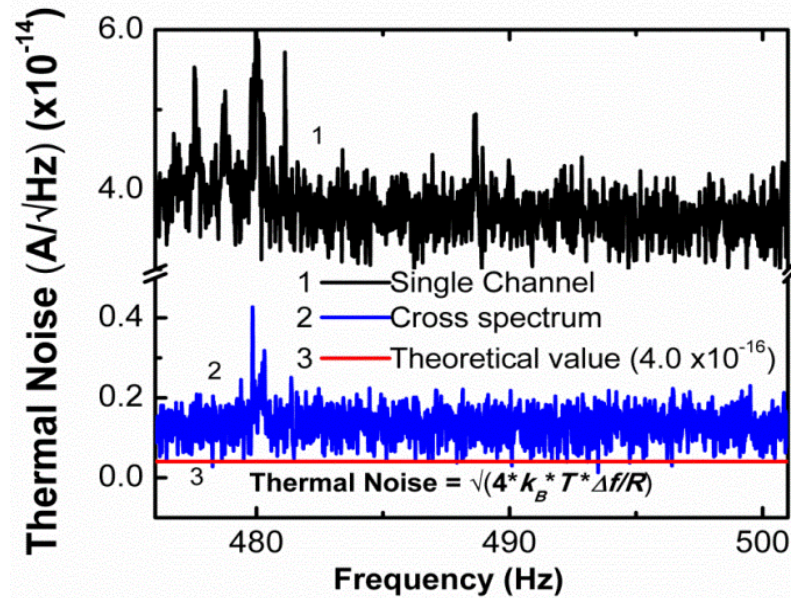


Figure 8 Current noise of 100 GΩ resistor at 290 K measured using single-channel and double-channel setup, and compared with theoretical thermal noise values.

The noise of the current amplifiers often sets the lower limit of detection in conventional single-channel LFN measurements. Sampietro and coworkers demonstrated subtraction of the instrument noise using cross-correlation technique. [51] Two independent current amplifiers (SR570 from Stanford Research Systems) provide the

source-drain bias and the gate bias is provided by an independent battery. In time-domain, the cross-correlation of two signals is defined as, [52]

$$Rv_1v_2(\tau) = \lim_{T \rightarrow \infty} \int v_1(t) v_2(t + \tau) dt, \quad (14)$$

where v_1 and v_2 are the time-variant signals, which in our case is the voltage outputs from two current amplifiers as shown in figure 7. In frequency-domain, the equivalent cross power spectrum of the two-signals is expressed as,

$$Gv_1v_2(f) = V_1(f)V_2(f)^*, \quad (15)$$

where $V(f)$ and $V(f)^*$ indicate Fourier transform of the signal $v(t)$ and its complex conjugate, respectively. However, $v_1(t) = c_1(t) + s(t)$, and $v_2(t) = c_2(t) + s(t)$, where $s(t)$ is the correlated component - mostly the device-under-test (DUT) noise, and $c_1(t)$ and $c_2(t)$ are the uncorrelated noise in channel 1 and 2, respectively - due to current amplifiers and analyzer front-end circuits. Considering orthogonality relationship of Fourier transform, it can be shown that the expected value of equation 18 is,

$$Re\{Gv_1v_2(f)\} = Re\{S(f)S^*(f)\} \quad (16)$$

where $S(f)$ is the Fourier transform of the DUT noise. Thus by performing cross-correlation on two separate channels, theoretically we can completely eliminate

instrumental noise. In figure 8, the difference between the single-channel and double-channel LFN measurements obtained on a 100 GOhm resistor at room temperature is shown. Current noise as low as $1 \text{ fA}/\sqrt{\text{Hz}}$ was consistently obtained with only 1 hour of acquisition time using double-channel configuration. The main point here is that the difference between the noise measurements taken using the single- versus double-channel setup is more pronounced when the DUT resistance is higher, as seen in figure 9. For nanoscale devices, the DUT resistances often are in excess of 100 MOhms, and accurate measurement of LFN is not possible using a single-channel setup. It is worth noting that lock-in noise reduction techniques cannot be used, as opposed to the correlation technique, to measure noise spectral densities from a generic DUT. The lock-in technique makes it possible to extract only deterministic signals from a noise background, whose frequency is known and is also available as an additional reference for demodulation purposes, but does not allow us to extract an unknown noise signal from a noise background to make a spectrum over any desired frequency range, as in our case.

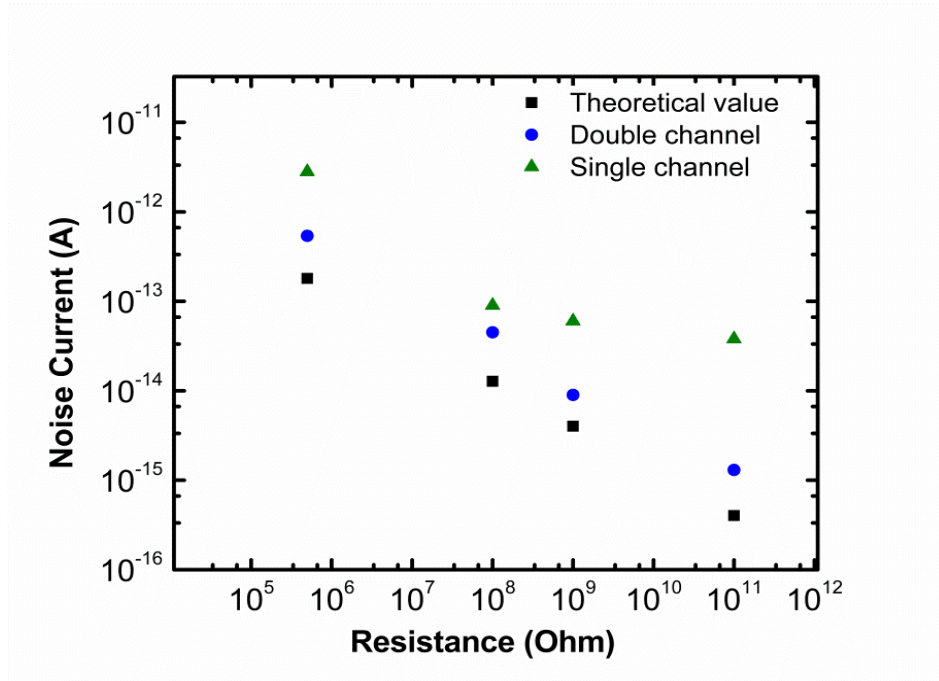


Figure 9 Current noise at 290 K measured for various resistors using single-channel and double-channel setup, and compared with theoretical thermal noise values.

1.7 Conclusion

In summary, chapter 1 primarily focuses on the study of occurring noise phenomena and its characterization in semiconductor devices. In the next chapter, I will discuss about the material properties and its applications. In the later chapters, attention will be shifted on device fabrication, transport measurements and low-frequency noise measurements. I will also discuss about the nature of traps, defects, contacts and surface states based on the knowledge gained from the experiments.

CHAPTER 2 SI NANOWIRE AND 2-DIMENSIONAL MOS₂ STRUCTURAL PROPERTIES AND THEIR APPLICATIONS

2.1 Introduction

For entire span of my PhD research work, I primarily focused on studying Field-effect Transistors (FETs) fabricated from Si nanowire and 2-dimensional MoS₂. I would like to review the properties and applications of these low-dimensional materials before the detailed analysis of my experimental results. This review will be helpful to better understand the results and discussions from the next chapters.

2.2 Silicon Nanowires (SiNWs)

SiNWs are very promising low-dimension materials due to their several unique properties and applications. Foremost, SiNWs have a technological edge over other types of low-dimension structures since they provide the ideal transition with the existing Si technology. Some important properties and applications of SiNWs are discussed next.

2.2.1 Growth and Material Properties

SiNWs are commonly grown by the vapor-liquid-solid (VLS) technique. Generally Au nanoparticles are used as the catalyst for the decomposition of SiCl₄ (or SiH₄) gas. The Au particles are deposited onto a Si substrate so that at high temperatures they re-act

with the Si atoms, forming Au-Si alloy eutectic droplets. These droplets adsorb Si from the vapor phase, resulting in a supersaturated state where the Si atoms precipitate and the SiNW starts nucleating as shown in figure 10. Also, the common approach to grow doped SiNWs is to offer dopant precursors such as PH_3 or B_2H_6 along with SiCl_4 or SiH_4 in a proper ratio and growth conditions. This technique gives better control on dopant type and density. [53-55]

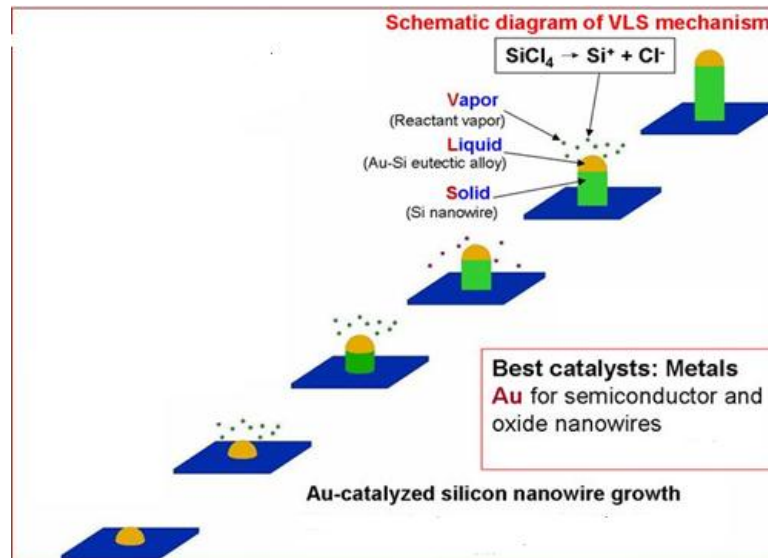


Figure 10 Schematic diagram showing the various steps in the VLS growth of a SiNW. [54, 55]

SiNWs can lead to additional benefits due to its bottom-up growth rather than commonly used but often challenging top-down lithography-based approach. SiNWs have single crystal structures and generally grow along very well defined crystalline directions. Study shows that there is a correlation between the diameter and the crystal

axis orientation in the Au catalyst assisted grown SiNWs. The smaller diameter (< 10 nm) nanowires tend to grow along $\langle 110 \rangle$ direction, and larger diameter (> 20 nm) nanowires prefer $\langle 111 \rangle$ direction while intermediate diameter (10 nm to 20 nm) nanowires prefer $\langle 112 \rangle$ direction. [56] Interestingly, it is also demonstrated that growth orientation can be externally controlled by adjusting the growth pressure. [57, 58]

Catalysts used in VLS technique can also serve as a source of impurities in SiNWs since they can easily diffuse into the Si matrix during the VLS growth process (discussed in next chapter). Since catalysts used are generally metals, they act as deep level impurities. More information about the impurity levels in silicon can be found in reference [59]. Apart from that, SiNWs always have some passivated facets since Si atoms at the surface are highly reactive due to presence of dangling bonds. Generally, SiNWs get passivation layer in two ways (i) the growth of a thin layer of SiO_2 by thermal oxidation of silicon; (ii) or forming a stable Si-H bond in the presence of Hydrogen.

Si has a unique property which makes it distinct apart from other materials. It possesses a chemically stable oxide, SiO_2 , which can be used to passivate Si surface without any major compatibility issues. Nevertheless, the quality of the oxide and Si/oxide interface is very critical for SiNWs especially when surface to volume ratio becomes large. Interface trap states (density D_{it}) are the most detrimental when it comes to impacting the electrical properties. These interface states are amphoteric, i.e., they can act as donors or acceptors depending on the position of the Si Fermi level at the surface. For example, if n -type Si with their Fermi level located in the upper half of the band-gap, all interface trap states between the Fermi level and the band-gap middle will look to get

negatively charged by acquiring electrons. Unfortunately, *n*-type silicon loses electrons to those interface traps, and in the process depleting itself. [60] Figure 11 shows a very interesting plot where average electron density n of an *n*-type SiNW as a function of the NW diameter is plotted for a given donor density N_D , ionization energy N_I , interface trap-level density D_{it} and temperature T . [61] It is quite evident from the discussion that free carrier concentration can change dramatically in SiNWs based on the quality of the Si/oxide interface.

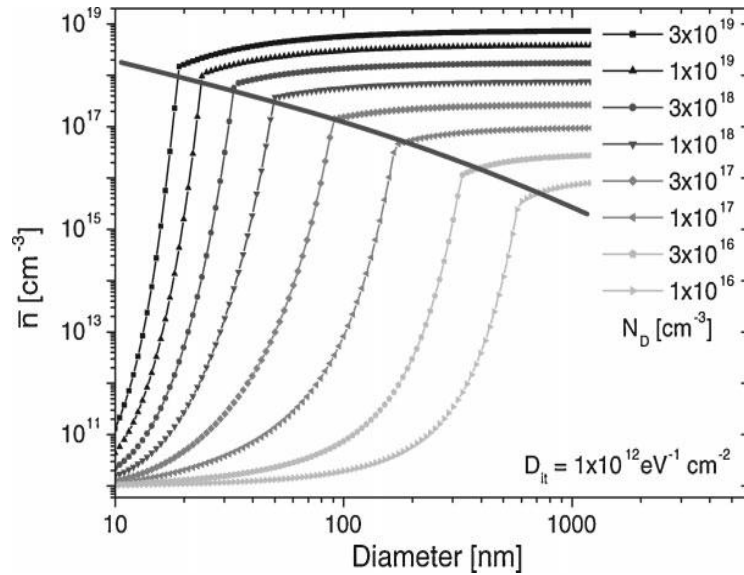


Figure 11 Average electron concentration at 300 K (averaged over the cross-section area) in a SiNW as a function of the NW diameter, for various donor concentrations N_D . The dopant is P with a bulk ionization energy of 45 meV. The interface trap level density $D_{it} = 1 \times 10^{12} \text{ eV}^{-1} \text{ cm}^{-2}$, [61]

The effect of the surface-to-volume ratio on the band gap can be described by the universal expression

$$E_{gap} = E_{gap}^{bulk} + aS \quad (17)$$

where E_{gap}^{bulk} is the gap of the bulk silicon, a is an adjustable parameter and S is the surface-to-volume ratio. It is clear from equation (17) that wires with totally different diameters can have the same band gap if their surface-to-volume ratio is the same. This has also been demonstrated experimentally. [62] Quantum confinements play an important role when diameter (d) < 10 nm, and equation (17) needs to be modified accordingly, i.e S is replaced by $(1/d)^t$ where t a fitting parameter. [63]

Mobility in thin nanowires, which have a high surface-to-volume ratio, is expected to be reduced due to the surface scattering. Simulation results show that surface scattering becomes dominant in SiNWs smaller than 5 nm × 5 nm, leading to a decrease in the electron mobility with decreasing NW cross section. [64] 100 cm²Vs⁻¹ is the reported mobility value for highly p -doped (10¹⁸ cm⁻³) 30 nm × 17 nm SiNWs prepared by top-down etching of SOI wafers. [65] For undoped SiNWs of 20 nm × 20 nm, prepared by top-down etching of SOI wafers, reported mobility was about 370 cm²Vs⁻¹ for the electrons and 130 cm²Vs⁻¹ for the holes. [66]

Estimation of mobility for grown SiNWs is done by first fabricating SiNW FETs and then estimating its trans-conductance and gate capacitance by electrical measurements. Often, accurate estimation of these parameters is difficult and ultimately

can lead to over- or under-estimation of mobility values. For grown *p*-type SiNWs, reported mobility values ranges from $3 \text{ cm}^2\text{Vs}^{-1}$ (for highly B doped 10^{20} cm^{-3}) to about $560 \text{ cm}^2\text{Vs}^{-1}$ for annealed and surface passivated *p*-type NW with diameter between 10 nm and 20 nm and $\langle 110 \rangle$ orientation . [67, 68] It is suggested that $\langle 110 \rangle$ orientated SiNWs have enhanced hole mobility. [69]

Large number of SiNW mobility values are reported in the literature with higher as well as lower than the bulk Si. Based on the reported works, it is safe to suggest that NW growth conditions, surface morphology, structural geometry and orientation, dopant concentration, play an important role in determining its electrical transport properties.

2.2.2 Applications

Taking advantage of the SiNW properties discussed so far, it may be an excellent candidate for several applications.

Foremost, its compatibility with CMOS technology means that it can be used as interconnects in integrated circuits. These new circuits could be easily reconfigured to perform different operations, achieving a much higher level of integration. [70] Additionally, compared to classical planar device technology, NWs are more suitable for all-around gate structures, which improve efficiency and device performances. [71, 72]

From the material and device structure standpoint, high-aspect-ratio nanowires are promising candidates to convert photons to charges efficiently. [73-75] Solar cell based on SiNWs has shown to have efficient absorption of sunlight by using only 1% of the

active material required in a conventional solar cell. [76] The energy conversion efficiency of an optimal SiNW-based solar cell may reach 12%. [77]

It is known that bulk Si has little or no catalytic activity. Remarkably, Hydrogen terminated SiNWs (H- SiNWs) were found to exhibit excellent photocatalytic activity in the degradation of rhodamine B. H-SiNWs showed even better photocatalytic activities than Pd-, Au-, Rh-, or Ag-modified SiNWs. [78]

SiNWs can improve the storage capacity for the lithium ion- battery anode, since storage of a lithium ion generally needs six carbon atoms while four lithium ions can be stored in one silicon atom. SiNW array was shown to be a promising for the scalable anode of rechargeable lithium batteries. [79]

Quasi 1-D Ni nanostructures were synthesized by SiNW templating. [80] SiNWs were also used as templates to grow silica nanotubes, and high-purity, single-crystalline beta-Si₃N₄ nanowires with diameters of 30 nm. [81, 82] SiNWs were also used as templates to prepare gold nanowires (AuNWs). [83]

SiNWs are good candidates for biological applications such as tissue engineering, biosensors and drug delivery. The SiNWs have high aspect ratio ($< 10^3$) and yet are sufficiently mechanically robust. The nanometer-scale diameter and the high aspect ratio of SiNWs make them readily accessible to the interiors of living cells, which may facilitate the study of the complex regulatory and signaling patterns at the molecular level. [84] SiNWs are believed to be excellent candidates for sensor applications. They are environmentally friendly, biologically compatible, easy to prepare, and convenient to modify. Sensors made up of SiNWs have been demonstrated in various fields. [85-89]

Finally, in the quantum confinement regime the band gap width depend critically on the diameter. Not only SiNWs can have a direct band gap for better photoelectric efficiency, their width can be manipulated to attain suitable bandgap. [90, 91]

2.3 Molybdenum disulfide (MoS₂)

Molybdenum disulfide (MoS₂) belongs to a family of transition metal dichalcogenides (TMDCs) which are among the most studied 2-dimensional compounds after graphene. Important properties and applications of MoS₂ are discussed next.

2.3.1 Material properties

MoS₂ monolayer is a hexagonally ordered plane of Molybdenum atoms sandwiched between two hexagonally ordered planes of Sulphur atoms as shown in figure 12. [92] The structure of layered TMDCs is similar to that of graphite, and each layer has a thickness of around 6.5 Å with strong in-plane covalent bonding and weak out-of-plane van der Waals forces. Van der Waals forces between adjacent MoS₂ layers are weak enough to isolate it via mechanical [93, 94] or chemical exfoliation. [95, 96, 97] The electrical properties of semiconducting MoS₂ also depend on the number of adjacent

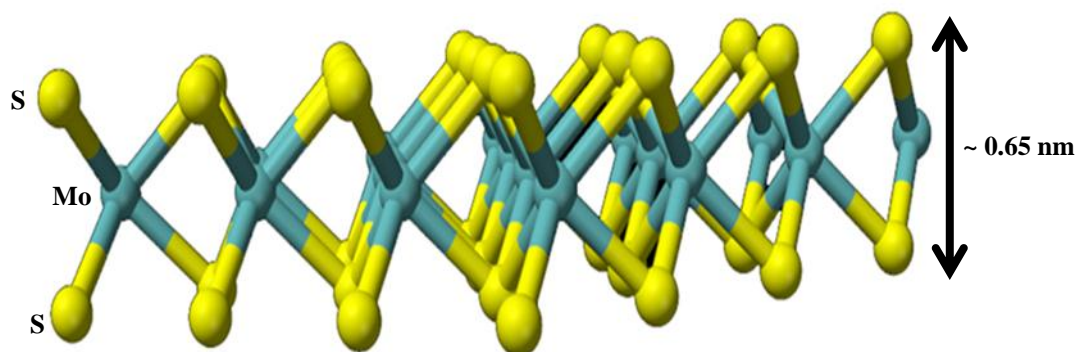


Figure 12 Schematics of chemical structure of mono layer MoS₂.

layers due to quantum confinements and changes in symmetry. [98, 99] Bulk MoS₂ has an indirect band gap of 1.2 eV, whereas single-layer MoS₂ has a direct band gap of 1.9 that results in enhanced photoluminescence (PL) by up to 4 orders of magnitude. [98] Theoretical and experimental studies [100-102] suggest that optical transitions in ultrathin MoS₂ samples are dominated by excitons rather than direct inter-band transitions. Unique structural symmetry of MoS₂ can make it possible to define a new state variable in valleytronic devices. [103]

Theoretical Simulation results show that ultimate performance of MoS₂ transistors lies in its large on/off current ratio ($>10^{10}$), immunity to short channel effects, (drain

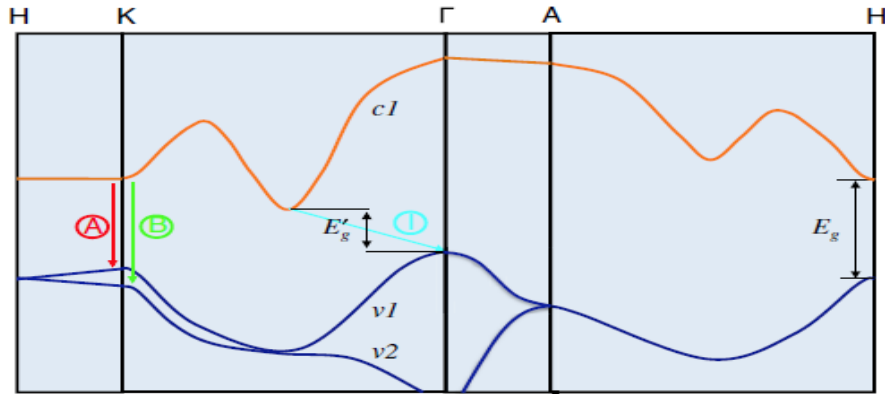


Figure 13 Simplified band structure of bulk MoS₂, showing the lowest conduction band c_1 and the highest split valence bands v_1 and v_2 . A and B are the direct-gap transitions, and I is the indirect-gap transition. E'_g is the indirect gap for the bulk, and E_g is the direct gap for the monolayer. [98]

induced barrier lowering ~ 10 mV/V), and abrupt switching with sub-threshold swing as low as 60 mV/decade. [104] Several studies have also revealed excellent mechanical properties of MoS₂ 2-D crystals.[105-107] In case of MoS₂ FETs, two-dimensional channel coupled with a large band gap (>1 eV) and ultrathin top gate dielectric allows superior gate control, thus enabling small Off-currents and large switching ratios. This work also suggested that the presence of the top dielectric enhanced the carrier mobility. [108]

2.3.2 Applications

From circuit design point of view, 2-D MoS₂ has a great advantage over other nanostructures (nanowires, nanotubes) as they are easier to fabricate into desired forms and structures. Radisavljevic *et.al* have experimentally demonstrated MoS₂ based integrated circuits, such as inverters, converting logical “1” into logical “0”,

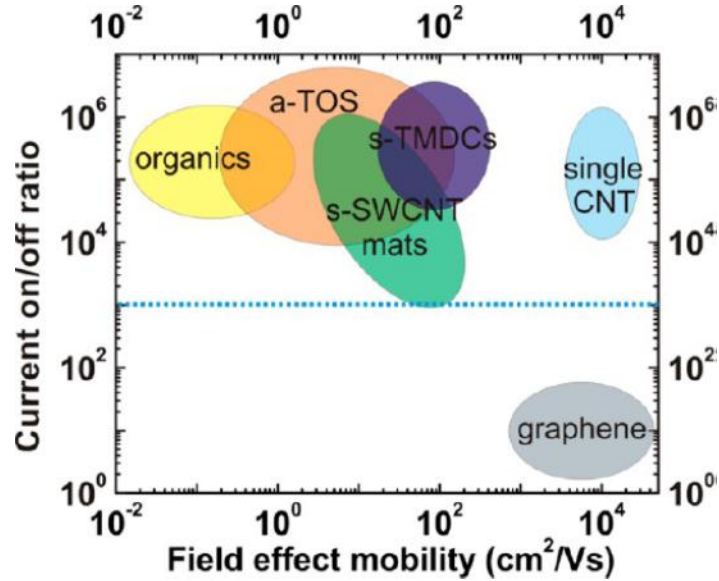


Figure 14 Comparison of field-effect mobility and on/off ratios of semiconductors for unconventional electronics. High on/off ratios ($>10^3$) are essential for digital electronics applications while maintaining the highest mobility possible. Semiconducting TMDCs (MoS_2 belongs to this TMDCs group) lie on a favorable position on this plot compared to the semiconductors that are currently under consideration for large-area flexible electronics. [112]

with voltage gain higher than 1, making them suitable for digital circuits. They also showed that electrical circuits composed of single-layer MoS_2 transistors can perform the NOR logic operation, the basis from which all logical operations and full digital functionality can be deduced. [109] Wang *et al* also demonstrated an inverter, a NAND gate, and static random access memory circuits. Their circuits comprised between 2 to 12 transistors seamlessly integrated side-by-side on a single sheet of bilayer MoS_2 . They successfully fabricated both enhancement-mode and depletion-mode transistors by using gate metals with different work functions. [110] Apart from these developments,

Ambipolar transport in a multilayer MoS₂ double-layer transistor has been demonstrated, suggesting the feasibility to develop *p-n* junction-based devices. [111]

Figure 15 shows a comparison of field-effect mobility and on/off ratios for all the competing semiconductors candidates. [112] Although comparison with state-of-the-art III-V materials may suggest that MoS₂ transistors are not ideal for high-performance applications, it can still be an excellent candidate for low cost, large area devices, currently dominated by very low mobility amorphous silicon and organic semiconductors. Wang *et al* in their paper [110] demonstrated a five-stage ring oscillator to assess the high frequency switching capability of MoS₂ and for evaluating the material's ultimate compatibility with conventional circuit architecture. Their reported frequency performance of ring oscillator (at a much lower V_{dd}) was at least an order of magnitude better than the fastest integrated organic semiconductor ring oscillators. [113] Moreover, its speed was high enough to compete with ring oscillators constructed from the printed ribbons of single-crystalline silicon reported in the literature. [114]

MoS₂ monolayer is a promising candidate for Solar Cells and Light-Emitting devices applications. It has a direct bandgap and better mobility values when compared to organic materials; as shown in figure 9. [112]

Due to its large surface to bulk ratio, MoS₂ is also a potential candidate for different kinds of sensor applications.

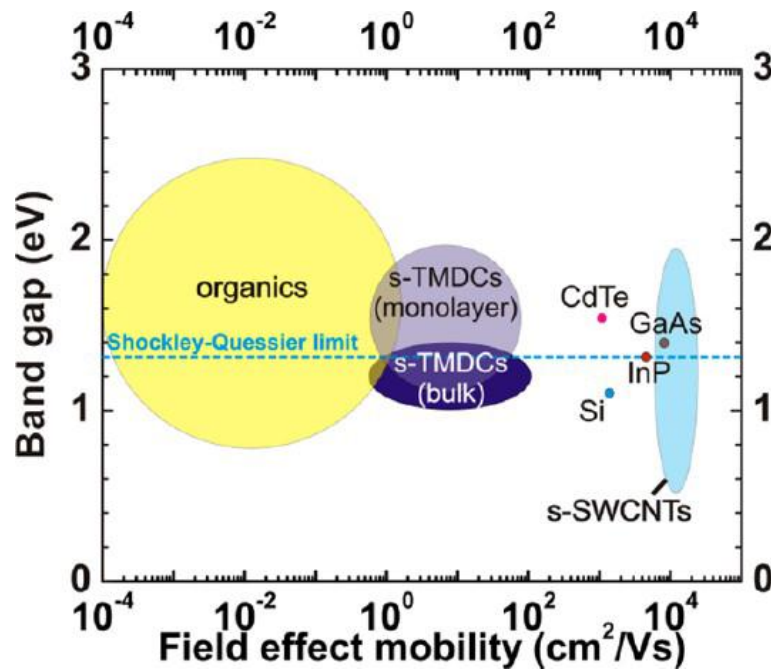


Figure 15 Band gap versus field-effect mobility for important semiconductors used in current generation photovoltaic technologies. A band gap near the Shockley-Quessier limit (~ 1.3 eV) and high mobilities are expected to lead to high-efficiency photovoltaic devices. Semiconducting TMDCs (MoS_2 belongs to this TMDCs group) are favorably placed in comparison to organic semiconductors for flexible photovoltaic cells. [112]

2.4 Conclusion

In summary, I discussed many important properties and applications of SiNW and MoS_2 . SiNW is a good candidate for large number of applications and one of the key strengths is its compatibility with conventional Si technology. On the other hand MoS_2 has a unique bandgap features, chemical robustness and remarkable structural geometry which make it a promising candidate for low power, large area electronics.

CHAPTER 3 TRANSPORT AND LOW-FREQUENCY NOISE IN SILICON NANOWIRES FIELD-EFFECT TRANSISTORS

In this chapter the detailed characterization of electrically active deep-levels in doped Si nanowires (SiNWs) grown using catalyst-assisted vapor–liquid–solid (VLS) technique are discussed. Temperature-dependent low-frequency noise (LFN) spectroscopy was used to reveal the presence of generation-recombination related Lorentzian-type peaks along with $1/f$ -type noise in these NWs. In Ni-catalyzed SiNWs, the correlated LFN spectroscopy detected electrically active deep-levels with ionization energies of 0.42 eV for the n -type and 0.22 eV for the p -type SiNWs, respectively. In Au-catalyzed n - and p -type SiNWs, the energies of the deep-levels were estimated to be 0.44 and 0.38 eV, respectively. These values are in good agreement with the known ionization energies of deep-levels introduced by Ni and Au in Si. Associated trap concentrations and hole and electron capture cross sections were also estimated. This data clearly indicated the presence of electrically active deep-levels associated with unintentional incorporation of catalyst atoms in the VLS-grown SiNWs.

3.1 Introduction

Semiconductor nanostructures are revolutionizing the field of electronics through realization of high performance devices and development of new understanding of transport mechanisms in such confined geometries. [115-121] Due to the small number of

charge carriers present in such nanostructures, understanding the role of defects, whether present in the bulk or at the interface, in charge carrier transport becomes increasingly important. [122-124] It is well-known that the electrically active defects in semiconductors often act as unintended generation-recombination ($G-R$) centers, adversely affecting the carrier lifetimes and device performance. [125] Despite tremendous advances made in the fabrication techniques of such nanostructures, both top-down [126] and bottom-up [127] approaches, there is still a vital need for measurement techniques for characterization of electrically active defects in nanoscale devices. This stems from the fact that the conventional methods to study deep-levels such as deep-level transient spectroscopy (DLTS) and photoinduced current transient spectroscopy (PICTS) become impractical for nanoscale devices. [128] Recently, Sato *et al.* [129] demonstrated DLTS and PICTS measurements on Si nanowire (SiNW) arrays using top-contact geometry for contacting large number of NWs. Applying those measurements on single NW devices is difficult.

In [130], our group showed the use of low-frequency noise (LFN) spectroscopy to characterize $G-R$ centers in SiNWs grown using catalyst-assisted chemical vapor deposition (CVD). In this work, I have implemented LFN spectroscopy using technique, which utilizes cross-correlation method to reduce instrument noise (explained in section 1.6). [131] This method was applied to probe deep-levels in p - and n -type SiNWs grown by the vapor-liquid-solid (VLS) mechanism using Au and Ni catalysts. Noise measurements were performed in 160- to 320-K temperature range. The power spectrum density (PSD) spectra showed clear Lorentzian behavior in all NW Field-effect

transistors (FETs) due to the *G-R* processes. Temperature- dependent noise analysis strongly indicated that the traps responsible for the *G-R* noise are due to the deep-levels introduced by Ni and Au atoms, which diffused unintentionally into the Si lattice during the VLS growth.

3.2 Material & Methods

3.2.1 NW Growth and Doping

The VLS growth of Au- and Ni-catalyzed SiNWs was carried out in a custom-built hot wall CVD system at a reactor pressure of 80 kPa (600 Torr) using 30 sccm of silicon tetrachloride (SiCl_4) and 200 sccm of hydrogen further diluted with nitrogen to a total flow rate of 1000 sccm. For gold-catalyzed NWs, 100-nm Au nanoparticles were cast on poly-L-lysine-functionalized Si (111) substrates. The NWs were then grown at 900 °C for 10 min, resulting in ≈ 25 - μm -long SiNWs with an average diameter of 130 nm. To minimize post growth migration of the Au catalyst from the tips of SiNWs, the samples were rapidly cooled to ≈ 550 °C by transferring them to the cold zone of the reactor. The Ni-catalyzed SiNWs were grown at 1000 °C for 5 min. The Ni islands, which served as nucleation sites for the NW growth, were performed on Si (111) substrate by thermal dewetting of e-beam deposited 2-nm-thick Ni film. Diameters of these NWs varied between 100 and 600 nm and the growth rate was 10 $\mu\text{m}/\text{min}$.

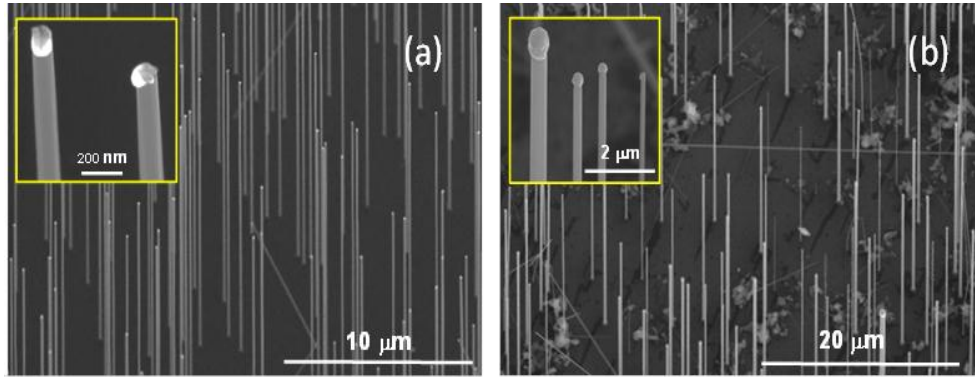


Figure 16 (a) and (b) Bird's-eye view SEM images of Au- and Ni-catalyzed Si NWs grown at 900 °C and 1000 °C, respectively. Insets show magnified top sections of the NWs capped with the metal catalyst tips.

The *n*- and *p*-type doping was achieved by adding PH₃ (100 ppm in N₂) and BCl₃ (2% in N₂), respectively, to the gas mixture with P(B)/Si ratio of 1.3×10^{-6} (3.3×10^{-4}). Representative scanning electron microscope (SEM) images of vertical array of Au- and Ni-catalyzed SiNWs are shown in figure 16 (a) and (b), respectively. The hexagonal-prism-shaped NWs grew normal to the Si (111) substrate along the <111> direction and were bound by six {1 1 2} sidewall facets as confirmed by transmission electron microscopy (TEM) (data not shown). The TEM also revealed that the NWs were free from extended structural defects.

3.2.2 Si NW Device Fabrication

A suspension of NWs was formed by sonicating the growth substrate in isopropanol. FET devices were fabricated by randomly dispersing the SiNWs on a heavily doped *p*-type Si substrate with 1-μm-thick SiO₂ layer deposited using plasma-enhanced chemical vapor deposition (PECVD). The dispersed NW samples were cleaned

in O₂:Ar (1:5) plasma and conformally coated with 50 nm of PECVD SiO₂ layer. The top oxide layer that passivates the NW surface was found to be crucial for enabling reproducible device measurements. Photolithography was done on the oxide coated NWs to define the source and drain contact openings. The oxide on the openings was etched using reactive ion etching with CF₄/CHF₃/O₂ (50/25/5 sccm) gas mixture. The source/drain metallization stack Ti (70 nm)/Al (70 nm)/Ti (30 nm)/Au (30 nm) was deposited using an e-beam system and annealed in a rapid thermal processing system at 550 °C for 30 s with 6000-sccm flow of Ar. The back-gate contact was formed by e-beam depositing 200-nm-thick Al layer onto the back side of the Si substrate. Four sets of FETs were fabricated: 1) *n*-type SiNWs grown using Ni catalysts; 2) *n*-type SiNWs grown using Au catalysts; 3) *p*-type SiNWs grown using Ni catalysts; and 4) *p*-type Si NWs grown using Au catalysts.

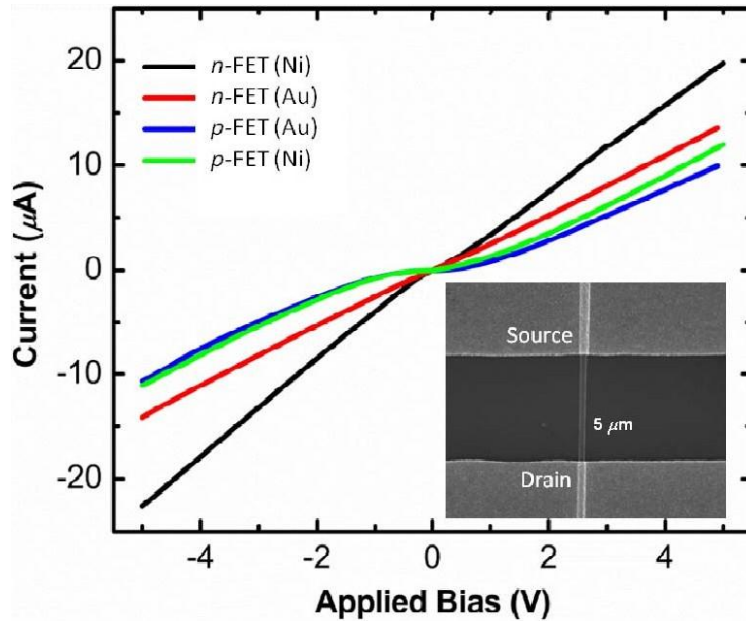


Figure 17 Room-temperature I - V curves of four different types of SiNW FETs. The I - V curves were taken at zero gate-source voltage (V_{GS}). The inset is a plan-view SEM image of representative NWFET with channel length of 5 μm and NW diameter 140 nm.

3.2.3 Parametric Measurements and LFN Spectroscopy

The temperature-dependent parametric measurement was done in an open-cycle cryogenic probe station using Agilent B1500A semiconductor parameter analyzer. The noise of the current amplifiers often sets the lower limit of detection in conventional LFN measurements. Our LFN measurement setup is based on the work done by Sampietro *et al.* (shown in figure 7), who demonstrated subtraction of the instrument noise using cross correlation technique. [51] The temperature-dependent measurements were performed from 160 to 320 K, starting from the lowest temperature. The LFN measurements were conducted between 1 and 1000 Hz with frequency resolution of 0.25 Hz. The dynamic signal analyzer had maximum of 4096 fast Fourier transform points, which resulted in

1600 frequency resolution lines for a given time record. Thus, in order to obtain 0.25-Hz resolution, the measurement span of 1000 Hz was broken down into three smaller spans of 400 Hz. Measurement in each 400-Hz span was root-mean-square averaged, which resulted in 4 min of total data acquisition time for the entire 1000-Hz span. The increased frequency resolution was essential for determining the G - R peaks appearing on the I/f spectra.

3.3 Results and Discussion

3.3.1 Device Characterization

The current–voltage (I – V) curves of different NW FETs are shown in figure 17. Inset in figure 17 shows an SEM image of a complete SiNW FET. It is worth noting that the n -type NWs always had linear I – V characteristics, whereas p -type devices showed nonlinearity in ± 0.3 V range. This most likely resulted from the fact that the doping levels in n -type NWs were slightly higher than the p -type NWs. The drain–source current (I_{DS}) as a function of gate–source voltage (V_{GS}) for n - and p -type Ni-catalyzed SiNWs is shown in figure 18. The slopes of the plots are consistent with the dopant types in both types of NWs, i.e., reduction in channel current with decreasing gate voltage for n -type NWs and vice versa for p -type NWs. Similar trends were observed for Au-catalyzed wires (not shown). The calculated field-effect carrier mobilities at 300 K for p FET (Ni) and n FET (Ni) are in the range of 25 – 40 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$ and 5 – 15 $\text{cm}^2 \text{V}^{-1} \text{s}^{-1}$, respectively. The mobility values are consistent with the calculated dopant density of 1 – $5 \times 10^{18} \text{cm}^{-3}$ for p -type and 1 – $5 \times 10^{19} \text{cm}^{-3}$ for n -type NWs for both Ni- and Au-catalyzed NWs.

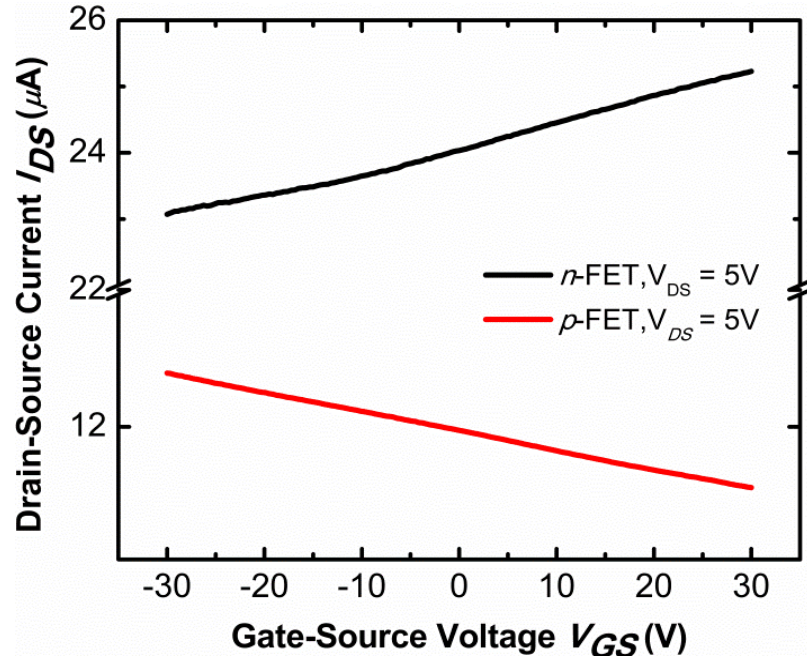


Figure 18 I_{DS} vs. V_{GS} plot of n -type and p -type Ni-catalyzed SiNW FETs.

3.3.2 Temperature-Dependent Resistivity

Figure 19 shows the source–drain resistance for SiNW FETs as a function of measurement temperature. Arrhenius plot shows semiconducting behavior in all NWs. Using the relationship $\ln(R) = \ln(R_0) + E_a/(2k_B T)$ (where R_0 is the intercept, E_a is the activation energy, k_B is the Boltzmann’s constant, and T is the absolute temperature), I calculated the activation energy for conduction in all four types of SiNWs. For Au-catalyzed NWs, activation energies obtained for p - and n -FETs were 0.06 and 0.04 eV, respectively. For Ni-catalyzed NWs, the estimated activation energies were 0.09 eV for

n-type and 0.06 eV for *p*-type FETs. [132] A close match with expected activation energy of shallow-dopant related conduction is only found in the case of Au-catalyzed *p*-type NWs. Higher values obtained for the rest of the NWs could have been influenced by contribution from the contact resistances, as these measurements were conducted using two-terminal structures. Nevertheless, these results point to the fact that the dc conduction in these NWs is dominated by shallow dopants.

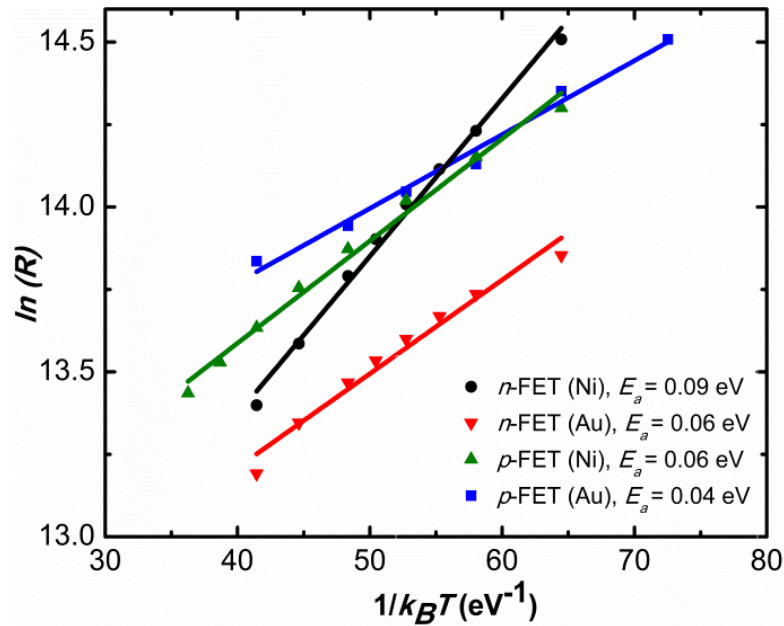


Figure 19 Arrhenius plot of the drain-source resistance in the linear region of the four different SiNW FETs shown in Fig. 6. For all four types of NWs good fit to the activation energy model is evident.

3.4 LFN Spectroscopy

The normalized drain-current noise PSD is defined as $S_I(f)/I_{DS}^2 = \langle i_{ds}(f)^2 \rangle / \Delta f I_{DS}^2$, where $\langle i_{ds}(f)^2 \rangle$ is the mean-square value of the current fluctuations with a particular frequency, Δf is the effective measurement bandwidth for the discrete frequency point, and I_{DS} is the dc value of the drain current. Normalized PSD for four different SiNW

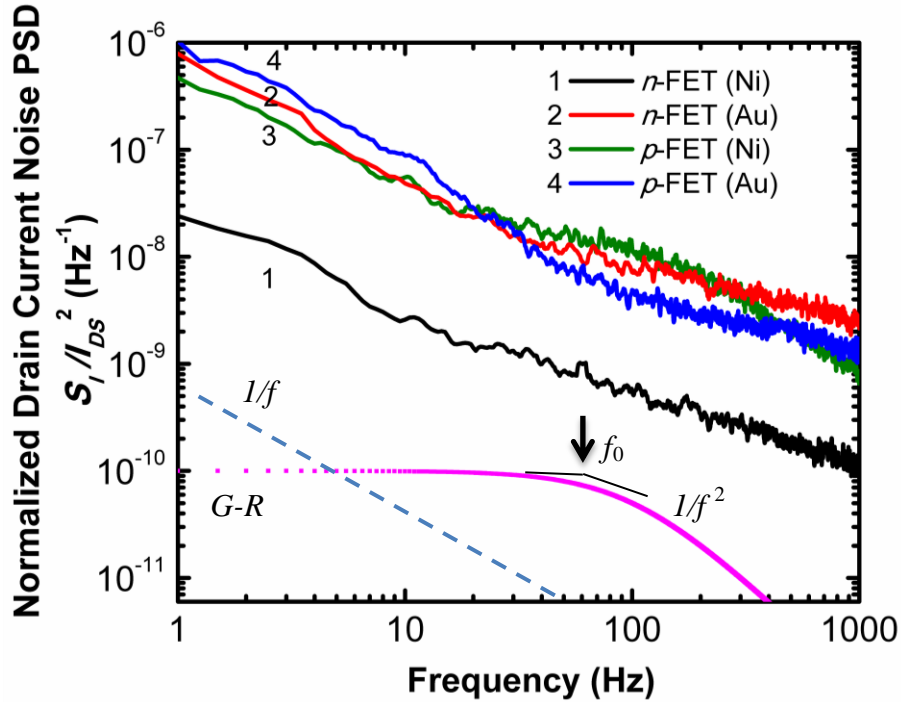


Figure 20 Normalized PSD of the drain current noise of four types of SiNW FETs (same as shown in figure 11) at 290 K. The $1/f$ trend is shown by the blue dotted line. The ideal single-time constant Lorentzian-type PSD is shown by the dotted magenta line.

FETs are shown in figure 20. For reference, the $1/f$ trend line is also shown, and deviation from the $1/f$ behavior is clearly seen in all the curves.

The curves in figure 20 are the representatives of ~ 10 NW devices of each type. Significantly, lower level of noise has been systematically observed for Ni-catalyzed n -type NWs (curve 1 in figure 20).

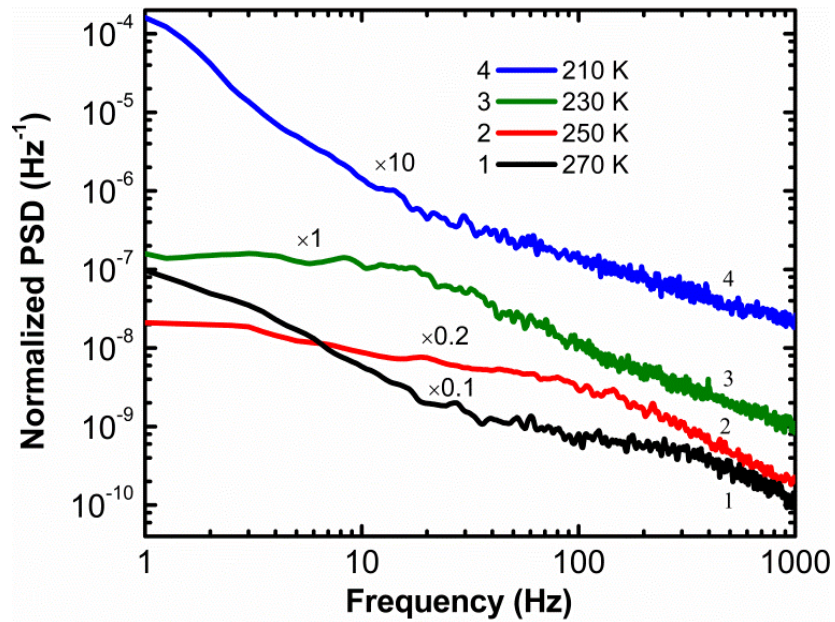


Figure 21 Normalized PSD of the drain current noise of Ni-catalyzed p -type wires taken at different temperatures.

The shift of the characteristics corner frequency of the Lorentzian-type PSD with decreasing temperature can be clearly seen. The curves are scaled for better visualization, with the scaling factor indicated above each curve.

Typically for a device that exhibits $1/f$ -type noise, irrespective of the cause of the noise, the normalized noise PSD can be described by the relationship $S_I/I_{DS}^2 = \alpha_H/Nf\beta$, where α_H is the Hooge's constant, N is the total number of carriers, and the exponential factor β is ideally 1. [133] The Hooge's constant is a generally accepted indicator of the quality of materials in terms of noise, i.e., the lower the Hooge's constant, the higher the material quality. I have estimated the Hooge's constant for all the NWs at 1 Hz, where the PSD is nearly $1/f$. For all the NWs, except Au-catalyzed n -type NWs, the estimated Hooge's constant was in the range of 0.07–0.04, with the lowest values estimated for Ni-catalyzed n -type NWs. This is consistent with the lower PSD values observed in these NWs. The estimated Hooge's constant value for Au-catalyzed n -type NWs was in the range of 0.2–0.6. Our previously reported value on p -type Au-catalyzed wires was in the same range. [130] At room-temperature, the drain-current noise PSD in SiNWs clearly showed a Lorentzian-behavior

$$S_I \propto \tau/(1+\omega^2\tau^2) \quad (18)$$

where τ is the relaxation time of the G - R process, and ω is related to the measurement frequency ($\omega = 2\pi f$). [134] The noise PSD due to a pure single time-constant G - R process is constant till the cutoff frequency f_0 ($\tau = 1/f_0$), above which it rolls off as $1/f^2$ (the theoretical G - R PSD characteristic is shown in figure 14 by the dotted magenta line. It is well-known that the Lorentzian-type PSD is due to the fluctuations of the charge states of the Shockley–Reed–Hall G - R centers present in bulk material. [125] There could be other mechanisms in NWs that generate LFN such as surface noise, contact noise,

shallow dopant fluctuation noise, and Auger $G-R$ noise. Band-bending at the surface provides continually varying time-constants associated with the $G-R$ centers resulting in a $1/f$ -type noise distribution. [135] Contact noise either due to thermal activation or tunneling would yield a $1/f$ -type LFN as well. [136] The shallow dopant-related capture and emission events are rare at the measurement temperature range. Although trap-assisted Auger $G-R$ process becomes significant at high dopant concentrations, the time-constants associated with such processes will be in the range of 10^{-5} s, [137] whereas the time-constants observed here are in range of 10^{-3} s. Thus, it is most likely that the Lorentzian-type PSD seen in these NWs is associated with single time-constant $G-R$ processes happening at the discrete states within the bandgap inside the NW.

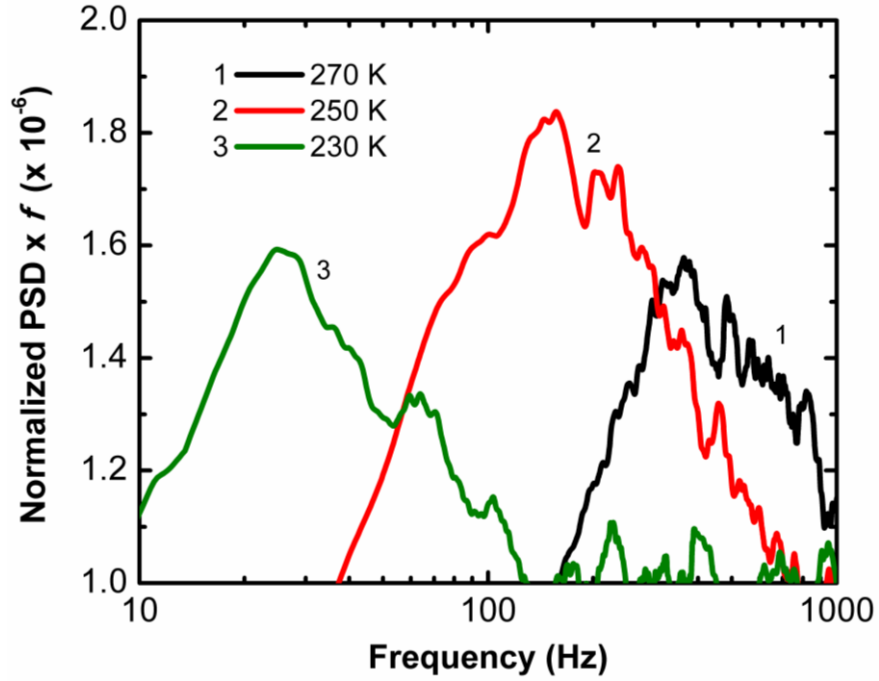


Figure 22 Semi-log plot of $\text{PSD} \times f$ for Ni-catalyzed *p*-type SiNW at different temperatures. The Lorentzian shape of the peak and its shift with temperature can be clearly seen. Normalize PSD is taken from figure 15

However, often deviation from the single-time constant curve is observed, especially at low frequencies, where surface-related $1/f$ noise dominates. [138] In reference [130], LFN in Au catalyzed boron-doped NWs was presented, which exhibited the ideal single-time constant behavior. The characteristic time-constant τ in equation (18) associated with fluctuations of the *G-R* process is given by [139]

$$\tau = 1/(c_n n + e_n + c_p p + e_p), \quad (19)$$

where c_n , c_p are the electron and hole capture coefficients, e_n , e_p are the electron and hole emission coefficients, and n , p are the equilibrium electron and hole concentrations, respectively.

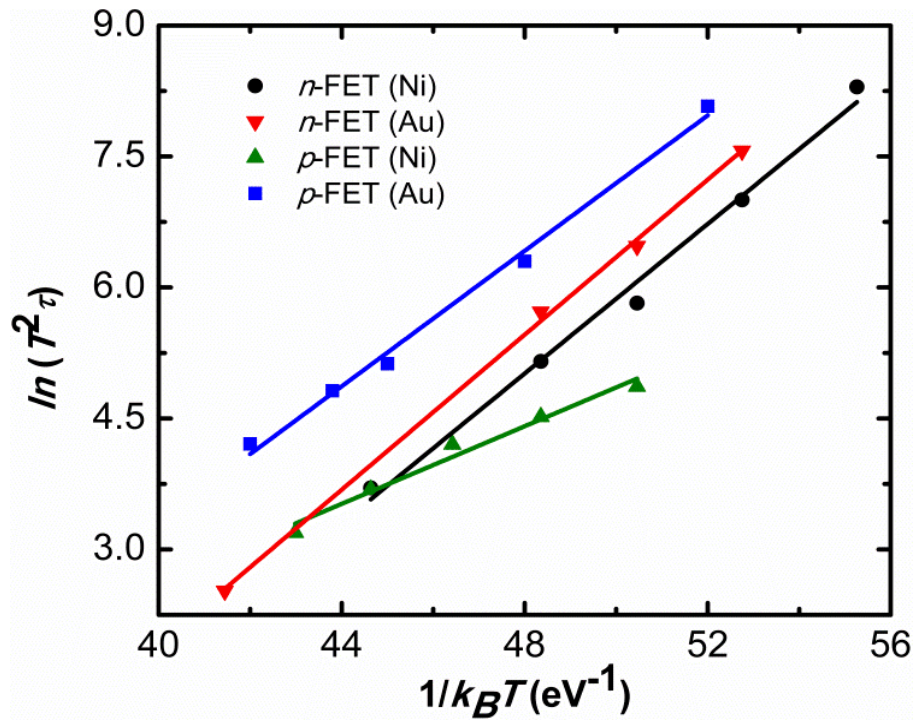


Figure 23 The Arrhenius plot of the $\ln(T^2\tau)$ vs. $1/k_B T$ of different types Si NW FETs.

Table 1 Estimated Energies, Capture Cross-Sections, and Concentrations of traps in SiNWs

Catalyst	Doping	Calculated Trap Energy (eV)	Calculated Capture Cross-sections (cm ²)		Estimated Trap Concentration (cm ⁻³)
			Electron	Hole	
Ni	n-type	0.42	6.1×10^{-15}	5.3×10^{-15}	1.0×10^{12}
Ni	p-type	0.22	5.7×10^{-19}	5.0×10^{-19}	1.0×10^{16}
Au	n-type	0.44	8.4×10^{-15}	7.3×10^{-15}	1.8×10^{12}
Au	p-type	0.38	9.5×10^{-17}	1.4×10^{-16}	2.0×10^{12}

Table 2 Energy Levels in Bulk Si Introduced by Ni and Au [68]

Metal	Type	Trap Energy (eV)
Ni	Acceptor	$E_c - 0.41$
	Donor	$E_v + 0.34$
Au	Acceptor	$E_c - 0.55$
	Donor	$E_v + 0.34$

Temperature-dependence of τ comes from the temperature dependence of carrier concentration, and from equation (19), it is easy to see that the decrease in carrier concentrations with decreasing temperature will result in an increase in the time constant, i.e., in a decrease of the rollover frequency f_0 . This is exemplified in figure 21, which shows normalized PSD of the drain-current noise for *p*-type Ni-catalyzed SiNW FETs taken at different temperatures. As expected, we can see the decrease in the rollover frequency as the temperature is decreased. For determination of the characteristic (rollover) frequency, it is very convenient to plot the product of normalized PSD $\times f$ in a linear scale as a function of the frequency in a log scale as shown in figure 22. In this representation, the PSD $\times f$ product appears as a Lorentzian-shaped symmetric peak centered at f_0 . The characteristic frequency f_0 (and hence the time-constant τ) for each temperature can be determined by fitting the corresponding curve to a Lorentzian function. Using this method, I found temperature dependences of the time-constants for all types of SiNWs studied here. The time constant τ associated with current fluctuations due to a *G-R* process can be related to the trap energy-level and capture cross section by the relationships [140], [141]

$$\ln(T^2\tau) \approx \left(\frac{\Delta E}{k_B T}\right) - \ln\left[\left(\frac{4k_B^2\sigma_n}{gh^3}\right)\left(6\pi^3 m_e^{1/2} m_h^{3/2}\right)^{1/2}\right] \quad (20)$$

$$\ln(T^2\tau) \approx \left(\frac{\Delta E}{k_B T}\right) - \ln\left[\left(\frac{4k_B^2\sigma_p}{gh^3}\right)\left(6\pi^3 m_e^{3/2} m_h^{1/2}\right)^{1/2}\right] \quad (21)$$

where ΔE is the trap-energy, σ_n , σ_p are the electron and hole capture cross sections, g is the degeneracy factor, and m_e , m_h are the electron and hole effective masses, respectively. For these relationships, it is assumed that the semiconductor is at or near thermal equilibrium, which is the case for low applied biases. Dependences of $\ln(T^2\tau)$ versus $1/k_B T$ are shown in figure 8 for all the four types of NWs; a good agreement to the theory is seen for all FETs. From the slope of the plot in figure 23, we can extract the energy position of the trap level and the intercept will give us the capture cross sections. Once energy level and capture cross sections are determined from the slope and the intercept of the curves in figure 17, the trap concentration N_T can be estimated using the following simplified relationship $\tau \approx 1/(\sigma_e v_e N_T)$, where v_e is the thermal velocity of the electrons given by [142]

$$v_e = \sqrt{3k_B T / m_e} \quad (22)$$

The estimated energy levels, electron and hole capture cross sections, and concentrations of the traps are listed in Table I. There are few key points worth mentioning about the estimates obtained using LFN spectroscopy: 1) unlike DLTS, LFN

spectroscopy cannot determine specifically the position of the trap relative to the conduction or valence bands and 2) the degeneracy factors in equations (20) and (21) introduce uncertainty in the determination of the capture cross sections and trap density, as the degeneracy factors for transition metals in silicon can vary from fractional values to integers. [143-145] However, this error should be small compared with the magnitudes of capture cross sections and trap densities. I have assumed $g = 1$ for the calculations. The most established data on the energy levels introduced by Ni and Au impurities in Si are listed in Table II after [146]. Comparing Tables I and II, we see a good agreement between our estimated values of the traps in SiNWs and the accepted literature data for Ni and Au impurities. The only exception is the estimated Au-acceptor level. Our results also agree with the report by Sato *et al.* [129] who detected two levels with activation energy of 0.36 and 0.38 eV in *p*-type and *n*-type VLS grown Si NWs, respectively, and associated them with electrically active Au–H complexes. As for Ni-catalyzed SiNWs, I believe that this is the first report on detection of deep levels introduced by Ni in SiNWs. Data on capture cross sections of Ni traps in Si are limited. Capture cross sections in the range of $1\text{--}5 \times 10^{-16} \text{ cm}^{-2}$ were estimated for a Ni electron trap at $(E_c - 0.48 \text{ eV})$ in *n*-Si [147]. Using DLTS technique, Tavendale and Pearton [148] determined capture cross section in the range 10^{-20} cm^{-2} for a Ni hole trap at $(E_v + 0.33 \text{ eV})$ in *p*-type Si. This is in line with the capture cross sections associated with Ni levels estimated in this paper. The electron and hole capture cross sections for the Au donor state were reported in the range $2\text{--}6 \times 10^{-15} \text{ cm}^{-2}$. [149] By combining DLTS and PICTS, Sato *et al.* determined hole and electron capture cross sections of the Au–H complex (0.36 eV) to be $3 \times 10^{-18} \text{ cm}^{-2}$

and $1 \times 10^{-15} \text{ cm}^{-2}$, respectively. Ni is a fast diffuser in Si with large fraction of Ni atoms occupying the interstitial sites. It has been established that only $\sim 0.1\%$ of dissolved Ni atoms occupy substitutional sites and are electrically active [150]. Istratov *et al.* [151] found that Ni solubility does not vary significantly for *n*-type and *p*-type silicon. For diffusion temperatures between 900 °C and 1000 °C, the Ni concentration was in the range $7\text{--}20 \times 10^{16} \text{ cm}^{-3}$. Thus, expected concentration of substitutional Ni atoms, i.e., traps, would be in the range $10^{13}\text{--}10^{14} \text{ cm}^{-3}$. Our estimated trap concentration for Ni-catalyzed *n*-type is slightly lower than that range, however for *p*-type wires estimated trap concentration is approximately two orders higher. Our estimated Au-related trap concentration value is roughly three orders of magnitude lower than the equilibrium solubility of gold in silicon at 850 °C ($\approx 2 \times 10^{15} \text{ cm}^{-3}$) as calculated from the thermal diffusion data. [152] The lower trap density could be either due to the actual lower Au concentration in the SiNW matrix or due to the hydrogen passivation of Au traps. [153]

3.5 Summary

In this work four different sets of FETs were fabricated using Au and Ni-catalyzed *n*- and *p*-doped SiNWs. Correlated noise measurement technique enabled us to perform accurate noise measurements on these low current nanoscale devices by effectively reducing the instrument noise. I have identified deep levels in these Ni and Au catalyzed *n*- and *p*-doped SiNWs, which matches very closely the known ionization energies of Ni and Au impurities in Si. To the best of our knowledge, this is the first report of deep-levels introduced by Ni-catalyst in SiNWs. In summary, our study

demonstrates that optimized LFN measurement can be a powerful tool for studying electrically active defects in nanoscale devices, especially when conventional defect characterization techniques cannot be implemented.

CHAPTER 4 ELECTRICAL TRANSPORT AND LOW-FREQUENCY NOISE IN CHEMICAL VAPOR DEPOSITED SINGLE-LAYER MOS₂ FETS

I have studied temperature-dependent (77 K - 300 K) electrical characteristics and low-frequency noise (LFN) in chemical vapor deposited (CVD) single layer molybdenum disulfide (MoS₂) based back-gated field-effect transistors (FETs). Electrical characterization and LFN measurements were conducted on MoS₂ FETs with Al₂O₃ top-surface passivation. I also studied the effect of top-surface passivation etching on the electrical characteristics of the device. Significant decrease in channel current and transconductance was observed in these devices after the etching of Al₂O₃ passivation. For passivated devices, the two-terminal resistance variation with temperature showed good fit to the activation energy model, whereas for the etched devices the trend indicated a hopping transport mechanism. A significant increase in the normalized drain current noise power spectral density (PSD) was observed after the etching of the top passivation layer. The observed channel current noise was explained using standard unified model incorporating carrier number fluctuation and correlated surface mobility fluctuation mechanisms. Detailed analysis of the gate-referred noise voltage PSD indicated the presence of different trapping states in passivated devices when compared to the etched devices. Etched devices showed weak temperature-dependence of the

channel current noise, whereas passivated devices exhibited near-linear temperature-dependence.

4.1 Introduction

Graphene's high carrier mobility and saturation velocity are very attractive, but the lack of inherent band gap is a challenge for switching applications and low-power electronics. [154] This has led to an exploration of alternative two-dimensional (2D) semiconductor materials. In recent years, molybdenum disulphide (MoS_2) has attracted significant interest due to the observation of indirect (1.29 eV) to direct (1.8 eV) band gap transition in monolayer films [155], which opens up exciting possibilities of realizing low-power, high-speed electronic, and optical devices on flexible substrates. MoS_2 transistors have exhibited high on-off ratios ($\sim 10^7$), and has shown subthreshold swing of 74 mV/decade. [156] Combined with high thermal stability and chemical robustness [153, 157], it promises to play an important role in future generation electronics. Few of the recently explored fields include digital electronics [158-160], chemical sensing [161], valley-polarization [162, 163], photovoltaics, and photocatalysis. [164, 165] Most of these applications require low distortions in the conduction process and often $1/f$ noise is the most dominant noise mechanism at low frequencies. Numerous studies have been conducted to understand and reduce $1/f$ noise in conventional metal-oxide field-effect transistors (MOSFETs). [166-170] Recently, various groups have also studied $1/f$ noise in graphene devices [171-173], and lately on MoS_2 FETs. [174] Particularly for MoS_2 devices, there exists a lack of understanding of the dominant mechanisms responsible for the observed current noise. The study of the effect of passivation on LFN in these 2-D

materials is critical for understanding the current noise, which is essential for future device applications.

In this chapter, I have explored the effect of top-surface passivation on the transport and LFN in single-layer MoS₂ FETs. Temperature-dependent (300 K to 77 K) transport and LFN measurements in single layer MoS₂ back-gated FETs with and after etching Al₂O₃ passivation are presented. I observed significant nonlinearity and an order of magnitude reduction of the channel current after top passivation layer was etched. Temperature-dependent two-terminal resistance of the passivated devices showed a clear fit to the activation energy model for the entire temperature range (77 – 300 K), suggesting a band-like transport. For the etched devices two different regimes were identified, indicating a defect-mediated transport. LFN measurements were conducted at various temperatures on both the passivated and etched devices at various back-gate biases. I have calculated Hooge parameters in the range of 0.01 to 0.0001 and 5 to 0.01 for passivated and etched devices, respectively. The observed gate-dependent noise in both passivated and etched devices could be explained by carrier number fluctuation arising from random trapping and detrapping of the channel charge carriers by the oxide interface traps and correlated surface mobility fluctuation arising from fluctuation of the scattering rates of these traps. [175, 176] Temperature-dependent noise measurement also showed very different behavior for passivated and etched devices.

4.2 Material and Methods

Monolayer MoS₂ films were grown directly on a SiO₂-coated (285 nm) Si substrate using the procedure described in detail by Najmaei *et al.* [177] In brief, high

aspect-ratio MoO₃ nanoribbons were used as precursor along with sublimated sulfur in a chemical vapor deposition chamber. The growth process resulted in single crystal MoS₂ triangles with a side length of $(13 \pm 2.5) \mu\text{m}$. Electron-beam lithography (EBL) was used to fabricate variable channel length FETs directly onto the single layer material avoiding grain boundaries and other defects. The MoS₂ layer was patterned using a CH₄/O₂ plasma etch, and source and drain contacts were formed by depositing Ti/Au (15 nm/85 nm) using an electron-beam evaporator. A 20 nm thick Al₂O₃ dielectric was deposited over the samples using atomic layer deposition (ALD), with O₂ plasma and tetramethyl aluminum (TMA) precursors. For the measurements on unpassivated devices, Al₂O₃ selectively etched by placing it in MIF300 developer (tetramethylammonium hydroxide based metal-ion free developer) for 30 min at room-temperature, followed by a de-ionized water / acetone / isopropanol rinse. Additional details about the processing steps can be found in the reference [178].

The temperature-dependent parametric measurements were done in an open-cycle cryogenic probe station from Lakeshore using an Agilent B1500A semiconductor parameter analyzer. LFN measurements were performed using cross-correlation technique to minimize the effect of instrument noise (shown in figure 7). The source-drain bias was provided by the internal batteries of the two independent SRS 570 amplifiers and the gate bias was provided using an independent battery source. Double channel dynamic spectrum analyzer HP 35670A was used in cross-spectrum mode to measure the PSD of the channel current. The LFN measurements were conducted between 1 Hz and 1000 Hz, with frequency resolution of 0.25 Hz and the data was averaged over 20 sets of

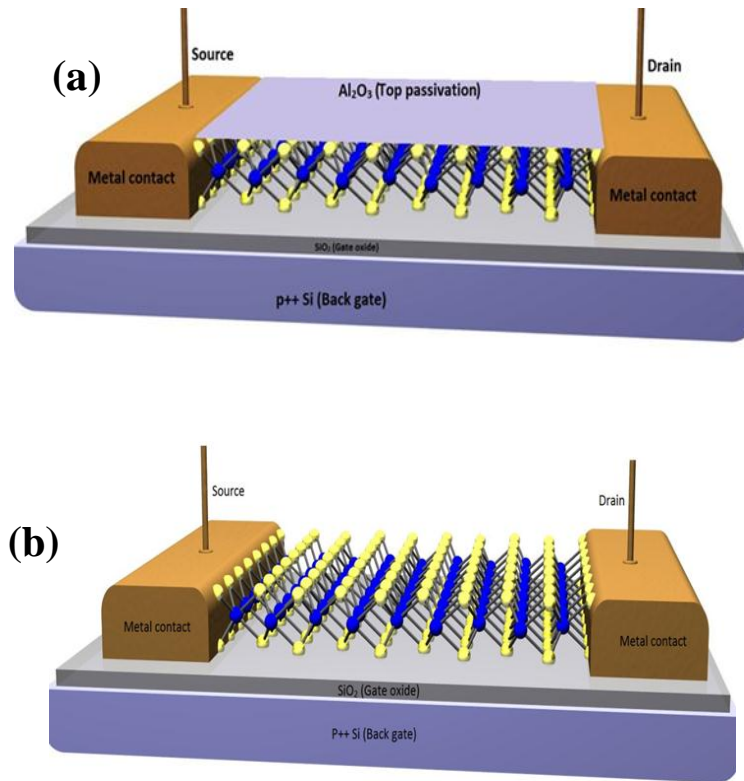


Figure 24 Schematics of (a) MoS₂ FET with Al₂O₃ top surface passivation; (b) MoS₂ FET with etched Al₂O₃ top passivation. Figure is adapted from reference [161] with few modifications.

readings. The temperature-dependent LFN measurements were performed from 77 K to 300 K, starting from the lowest temperature.

4.3 Raman measurements

Raman measurements were performed on exfoliated 1H-MoS₂ in order to assess potential changes in the quality of these molecular layers after deposition of the ALD oxide and its removal using a MIF300 developer. The measurements were performed with

a WITec Alpha 300RA system using the 532 nm line of a frequency-doubled Nd:YAG laser as the excitation source. The spectra were measured in the backscattering configuration using a 100x objective and either a 600 or 1800 grooves/mm grating. The spot size of the laser was ~342 nm resulting in an incident laser power density ~280 $\mu\text{W}/\mu\text{m}^2$. No time dependent shifting of the in-plane (E_{2g}^1) or out-of-plane (A_{1g}) modes was produced during testing.

The resulting spectra are shown in figure 25 and key parameters for the E_{2g}^1 and A_{1g} peaks were extracted using Lorentzian fits and are listed in table 3. While some variation (< 1 1/cm) in the E_{2g}^1 mode was observed after the deposition, the primary shift occurred in the A_{1g} mode, similar to what has been observed after the deposition of HfO_2 on MoS_2 by ALD. [179] I found that the position of this peak partially recovered to its original value. Additionally, the deposition of the oxide resulted in a decrease of the A_{1g}/E_{2g}^1 intensity ratio which fully recovered after its removal. Some studies have linked the intensity ratio to the quality of the MoS_2 film, [180] however a detailed discussion of this effect is beyond the scope of this work.

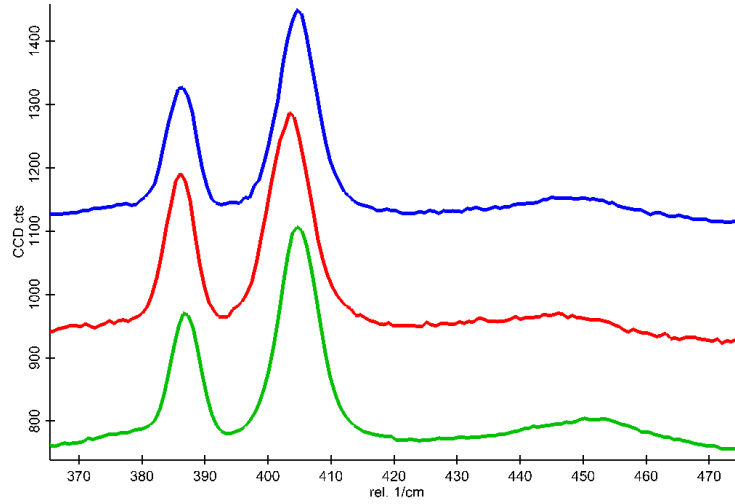


Figure 25 Raman spectra for monolayer MoS₂ prior to ALD deposition of Al₂O₃ (blue), after ALD deposition of Al₂O₃ (red), and after removal of Al₂O₃ (green).

Table 3 Raman peak position, separation, and intensity ratio for monolayer MoS₂ at the various processing stages.

	Pristine	w/Al ₂ O ₃	After Al ₂ O ₃ Etch
E _{2g} ¹ frequency (1/cm)	386.19	386.05	386.88
A _{1g} frequency (1/cm)	404.69	403.47	404.87
Δω (1/cm)	18.50	17.42	17.99
A _{1g} /E _{2g} ¹ intensity ratio	1.61	1.46	1.67

4.4 Results and Discussion

Figure 26 shows the drain-source current (I_{DS}) versus drain-source voltage (V_{DS}) characteristics of a MoS₂ transistor at 300 K with gate length (L) and width (W) of 400 nm and 1000 nm, respectively, before and after etching of the top Al₂O₃ passivation layer. Measurements were done on both passivated and etched devices in vacuum with

chamber pressure in the range of 10^{-3} Pa. The insert of figure 19(a) shows a scanning electron microscope (SEM) image of a typical device. Significant reduction of the channel current (almost an order of magnitude) and non-linearity in the current-voltage characteristics were observed for devices after the passivation was removed as shown in figure 26(b).

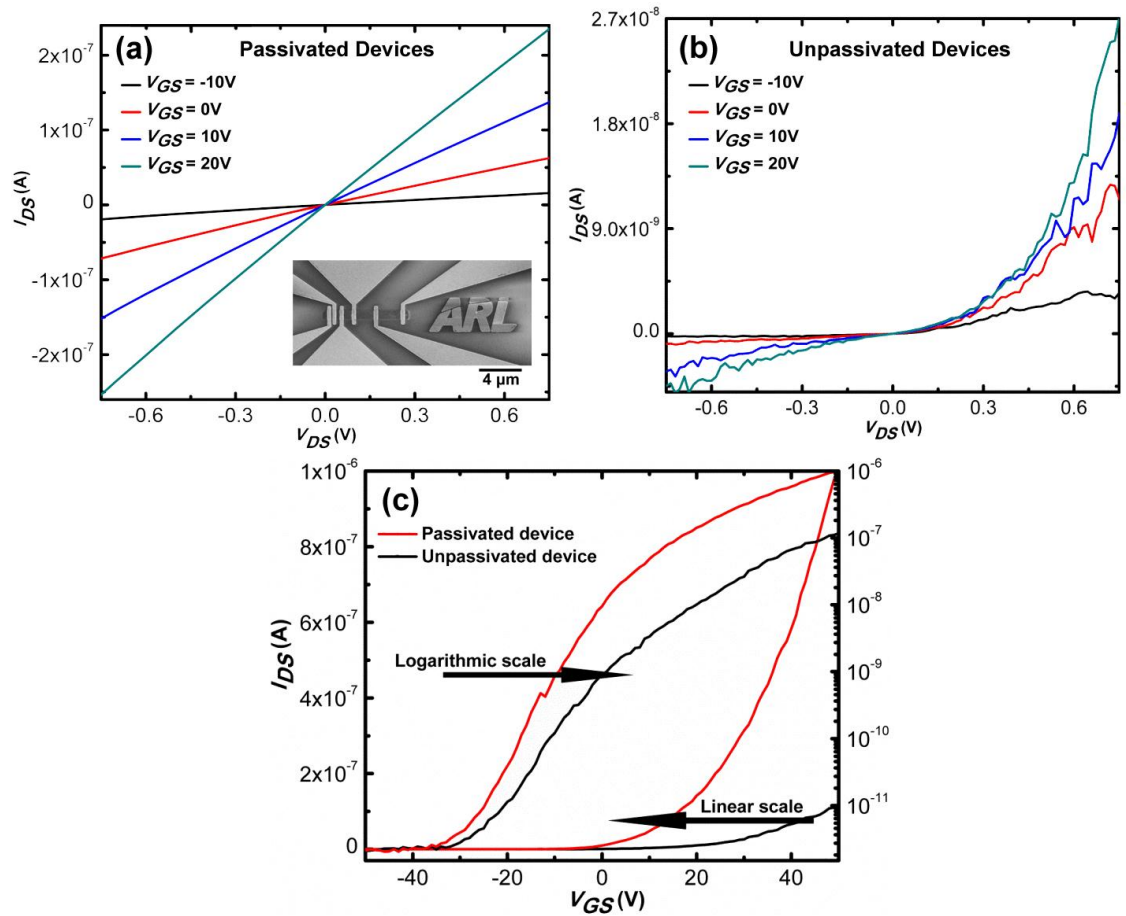


Figure 26 I_{DS} - V_{DS} plot at 300 K for MoS₂ FET (a) before and (b) after etching of the top passivation. All the I - V curves were taken at constant drain-source voltage ($V_{DS} = 0.5$ V). Inset in (a) shows an SEM micrograph of a typical device. (c) I_{DS} - V_{GS} plot of the passivated and unpassivated devices plotted in both linear and logarithmic-linear scales at 300 K.

A transfer characteristics plot (I_{DS} versus V_{GS} at $V_{DS} = 0.5$ V) is shown in figure 26(c) for the same device with passivation and after passivation has been removed. Clear depletion mode n -channel behavior can be seen in these devices, which is in good agreement with what has been also observed by other groups. [155, 156, 181] The field-effect mobility (μ_{FE}) for these devices was calculated using the following equation:

$$\mu_{FE} = \frac{\partial I_{DS}}{\partial V_{GS}} \cdot \frac{L}{WC_{OX}V_{DS}} \quad (23)$$

where C_{OX} is the gate capacitance per unit area, L is the channel length, W is the channel width, V_{DS} is the source-drain voltage, and $\partial I_{DS}/\partial V_{GS}$ is the slope of the I_{DS} - V_{GS} characteristics taken in the linear region. At 300K the measured field-effect mobility values were $(35.5 \pm 2.5) \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ and $(12.1 \pm 1.9) \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ for passivated and etched FETs, respectively. All mobility values were measured using four probe measurement techniques on Hall bar devices at a I_{DS} of 500 fA, to reduce the contribution of the contact resistances.

The two-terminal channel resistance for these MoS₂ FETs as a function of measurement temperature is shown for both passivated and etched samples in figures 27 and 28. The passivated devices exhibited a good fit to the activation energy model at different gate biases over the entire measurement temperature range, i.e., 77 K to 300 K, as evident in figure 27.

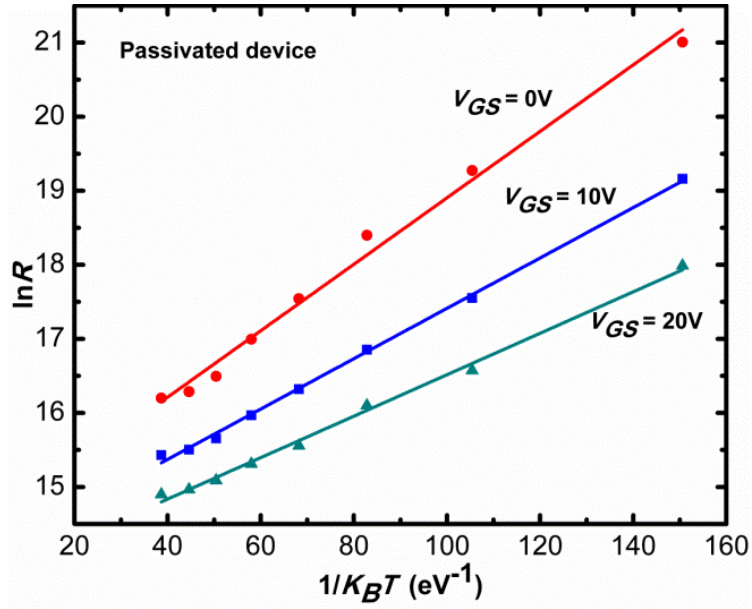


Figure 27 Arrhenius plot of the drain-source resistance of the passivated FETs at three different gate biases is shown in (a) and (b), respectively. Temperature is in the range of 77 K to 300 K. All the readings were taken at a constant drain-source voltage ($V_{DS} = 0.5$ V).

This indicates a transport mechanism involving well-defined bands. Using the relationship: [174]

$$\ln(R) = \ln(R_0) + E_a/2k_B T \quad (24)$$

where R_0 is the intercept, E_a is the thermal activation energy of the dopant, k_B is the Boltzmann's constant, and T is the absolute temperature, we can calculate the activation energy for conduction in these devices. From the slopes of different curves at different back-gate biases and it is clear that the activation energy decreases with increasing back-

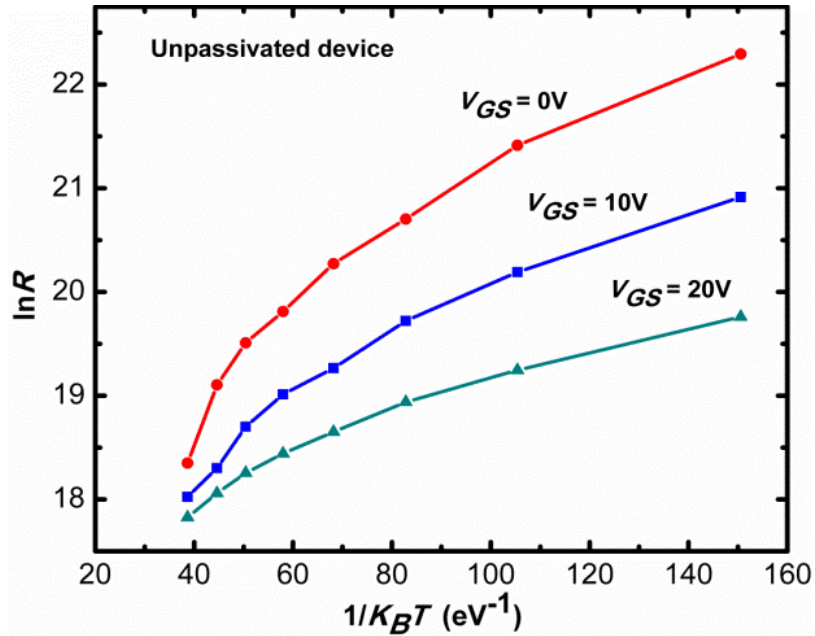


Figure 28 Arrhenius plot of the drain-source resistance of the unpassivated (after etching of the top passivation) FETs at three different gate biases. Temperature is in the range of 77 K to 300 K. All the readings were taken at a constant drain-source voltage ($V_{DS} = 0.5$ V).

gate bias (figure 27). On the other hand, etched devices showed two different regimes of conduction for the entire investigated temperature range, with higher activation energy between 200 and 300 K, and weaker temperature-dependence between 77 and 200 K, for all three back-gate biases (figure 28). The calculated activation energies at 20 V back-gate bias were ≈ 56 meV for passivated devices and ≈ 32 meV (in the 200 K – 300 K temperature range) for etched devices. In a recent report, Radisavljevic and Kis measured the temperature dependence of the conductance in monolayer MoS₂ back-gated FETs (unpassivated) as a function of back-gate bias. [182] Although thermally-activated transport model was used to explain the trend, the fit was evident only for temperatures between 166 K and 250 K, below which the conductance showed very weak temperature

dependence. Surprisingly, the activation energy (computed from their data) is in the range of 20 - 60 meV for back-gate biases ranging from 2 to 40 V. Very similar trend was also observed by Ayari *et al.* for two-probe conductance variation with temperature for unpassivated MoS₂ monolayers [183]. The calculated activation energy for their result is close to 50 meV for 9 V back-gate bias. The close agreement of the activation energy values for conduction obtained in MoS₂ samples fabricated by different methods might indicate the presence of a native defect, which manifests as shallow donor in monolayer materials. Qiu *et al.*, reported a very similar trend for temperature-dependent conduction in single-layer MoS₂ FETs and successfully explained the observed trend using hopping conduction through defect-induced localized states [184], they concluded that the responsible defects were sulfur vacancies. Comparing our results on passivated devices, it is clear that the top-surface passivation renders these surface-defects inactive and could be partially responsible for the improved electrical characteristics observed for MoS₂ devices. Raman spectroscopy measurements (see supplemental section) on etched devices did not indicate any significant structural damage to the MoS₂ layer due to passivation etch. The normalized drain current PSD ($= S_{ID}/I_{DS}^2$) for both passivated and etched devices measured at 300 K at three different gate biases are shown in figure 29 and 30. An increase of almost two orders of magnitude in the normalized drain current PSD was observed after the etching of the passivation layer. When V_{DS} was varied from 0.2 V to 2 V, the normalized PSD did not change, indicating that the measured noise is originating from the channel, with minimal contribution from the contacts. The S_{ID}/I_{DS}^2 at 10 Hz were in the range of $(1 - 10) \times 10^{-8} \text{ Hz}^{-1}$ and $(1 - 10) \times 10^{-5} \text{ Hz}^{-1}$ for passivated and etched

devices, respectively. In case of Graphene devices, several groups have reported S_{ID}/I_{DS}^2 in the range of 10^{-9} Hz^{-1} to 10^{-7} Hz^{-1} at 10 Hz. [172, 173, 185]

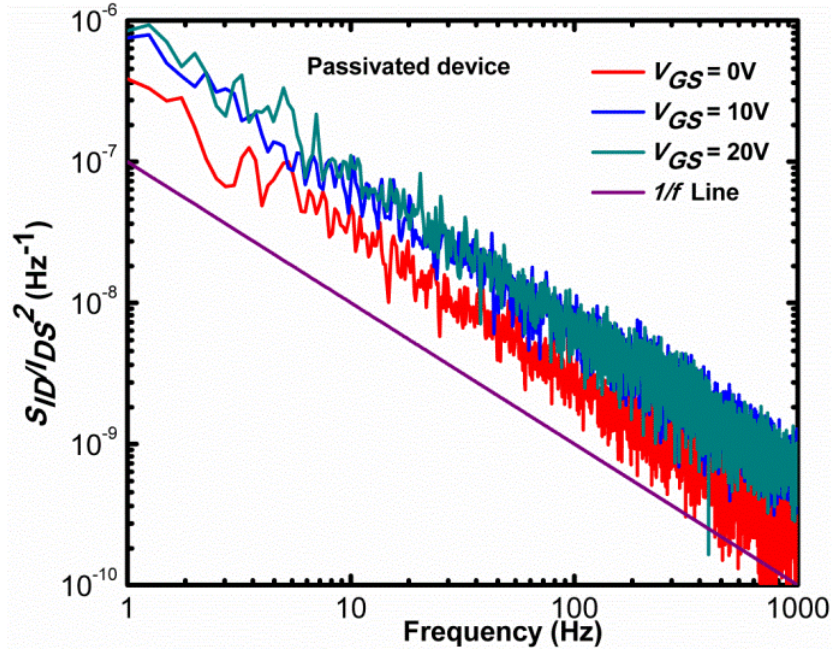


Figure 29 Room temperature ($T = 300 \text{ K}$) normalized PSD of the drain current for passivated devices at different V_{GS} . A $1/f$ trend line is shown for comparison. All the readings were taken at a constant drain-source voltage ($V_{DS} = 0.5 \text{ V}$).

Irrespective of the mechanisms responsible for the noise, for a device exhibiting $1/f$ -type noise, the measured PSD can always be described using the Hooge's empirical relationship (explained in section 1.3):

$$S_{ID}/I_{DS}^2 = \alpha_H/Nf^\beta, \quad (25)$$

where α_H is the Hooge constant, β (exponential factor) is ideally 1 and N is the total number of carriers approximated as $N = (V_{GS} - V_T) \times L \times W \times C_{OX} / q$ where q is the charge of an electron, V_{GS} is gate to source voltage, and V_T is the estimated threshold voltage. Although for 2-D materials, the validity of the model is questionable, it provides a figure of merit, i.e., Hooge constant, which allows for direct comparison of the noise levels in various devices. In our case the calculated variation in β is 1 ± 0.2 for etched devices and

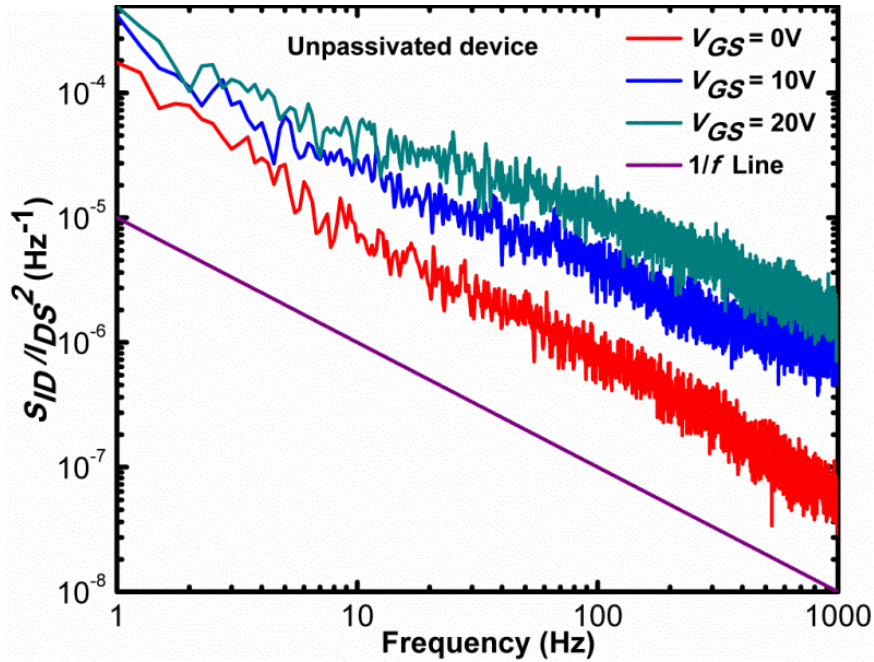


Figure 30 Room temperature ($T = 300$ K) normalized PSD of the drain current for unpassivated (after etching of the top passivation) devices at different V_{GS} . A $1/f$ trend line is shown for comparison. All the readings were taken at a constant drain-source voltage ($V_{DS} = 0.5$ V).

1 ± 0.09 for passivated devices. The calculated Hooge parameter ranges are between (0.01 and 0.0001) and (5 and 0.01) for passivated and etched devices, respectively. Recently, Hooge parameter ranging between 0.005 and 2 has been reported for unpassivated MoS₂ FETs. [174]

I have used the “unified model” which takes into account both carrier number fluctuation along with correlated mobility fluctuation to explain the observed LFN trends in these devices. Carrier number fluctuations arise from dynamic trapping and de-trapping of free-carriers by the oxide-semiconductor interface traps. In addition, trap charge fluctuations may result in scattering rate fluctuations, which causes fluctuations of the inversion layer mobility. It is worth pointing out that the Hooge’s mobility fluctuation is a bulk-effect, whereas the correlated mobility fluctuation is a surface effect resulting from carrier number fluctuation through interface traps. In analyzing the noise, I have used the framework proposed by Ghibaudo *et al.*, where normalized drain current spectral density (S_{ID}/I_D^2) and input-referred gate voltage spectral density (S_{VG}) are given by the following relationships [175, 176]:

$$\frac{S_{ID}}{I_D^2} = \left(1 + \alpha \mu_{eff} C_{OX} \frac{I_D}{g_m}\right)^2 \left(\frac{g_m}{I_D}\right)^2 (S_{VFB}) \quad (26)$$

$$S_{VG} = S_{VFB} [1 + \alpha \mu_{eff} C_{OX} (V_{GS} - V_T)]^2 \quad (27)$$

where α is the Coulomb scattering coefficient ($\approx 10^4 \text{ V}\cdot\text{s}\cdot\text{C}^{-1}$ for electrons and $\approx 10^5 \text{ V}\cdot\text{s}\cdot\text{C}^{-1}$ for holes), μ_{eff} is the low-field effective mobility, C_{OX} is the gate capacitance, V_T is the

threshold voltage, S_{VFB} is the flat-band voltage spectral density, respectively. The S_{VFB} is related to interface charge spectral density per unit area (S_{Qit}) as $S_{VFB} = S_{Qit}/(WLC_{OX}^2)$. It should be mentioned that equations (26) and (27) are generally valid for inversion-mode MOSFETs. [175, 176] Although MoS₂ FETs presented in this study are *n*-channel depletion-mode devices, the close proximity of the channel charge carriers to the interface can lead to similar fluctuation mechanisms as in inversion-mode FETs. The dominant mechanism can be highlighted by plotting the normalized drain current spectral density as a function of drain current (I_{DS}) in a log-log scale. In case of Hooge's mobility fluctuation, i.e., bulk mobility fluctuation, the normalized drain-current PSD should be proportional to $1/I_{DS}$. If the normalized drain-current PSD varies with the drain current as $(g_m/I_{DS})^2$, i.e., $S_{ID}/I_{DS}^2 \propto (g_m/I_{DS})^2$, then it is likely that the carrier number fluctuation is the dominant source of the $1/f$ noise. Moreover, if the associated gate-referred voltage PSD (S_{VG}) exhibits parabolic gate-voltage dependence, then correlated mobility fluctuation is also present.

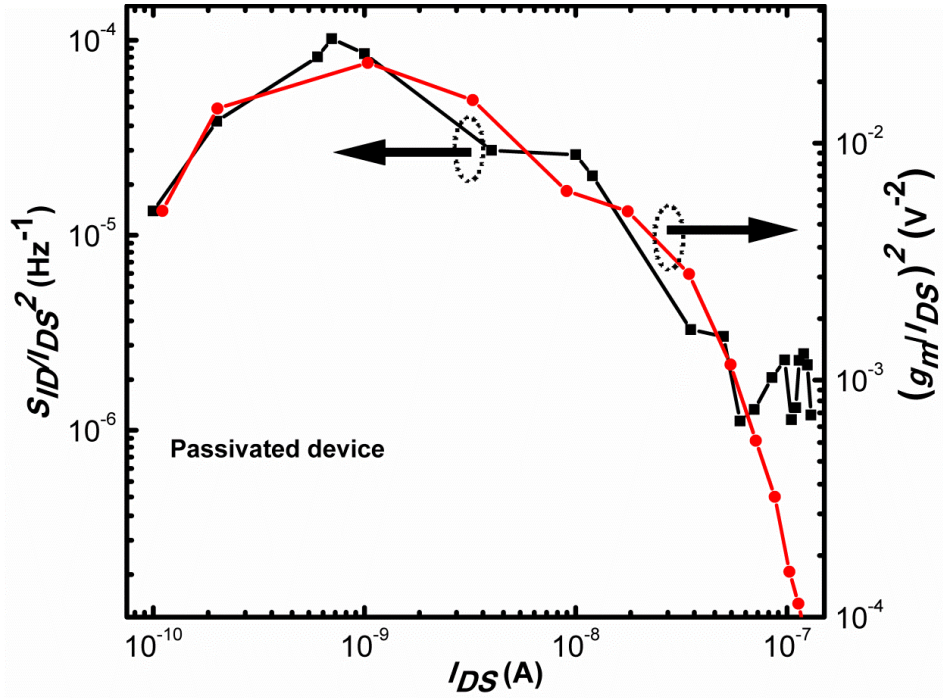


Figure 31 Comparison of normalized PSD of the drain current at $f = 1$ Hz and $(g_m/I_{DS})^2$ at different I_{DS} for passivated. All the readings were taken at a constant drain-source voltage ($V_{DS} = 0.5$ V).

Figure 31 and 32 present S_I/I_{DS}^2 as a function of drain current in a log-log plot. It is worth pointing out here that significant variation in S_I/I_{DS}^2 as a function of I_{DS} is observed by varying V_{GS} in wide range of values. As evident from figure 31 the passivated device demonstrates near-ideal fit. The deviation at higher drain currents is due to the excess noise from the source/drain contact resistances. [175] For etched devices (figure 32) the agreement is not exact. Figure 33 and 34 presents gate-referred voltage PSD (S_{VG}) as a function of $(V_{GS}-V_T)$. For both passivated and etched devices the parabolic dependence is evident, indicating the correlated mobility fluctuation is also present. In the absence of correlated mobility fluctuation, the gate-referred noise voltage

will be constant as a function of gate bias. For passivated devices, a minima in the plot of gate-referred voltage PSD as a function of $(V_{GS}-V_T)$ is observed. Interestingly, Ghibaudo *et al.*, demonstrated that by mixing acceptor- and donor-like traps in the noise model, one can

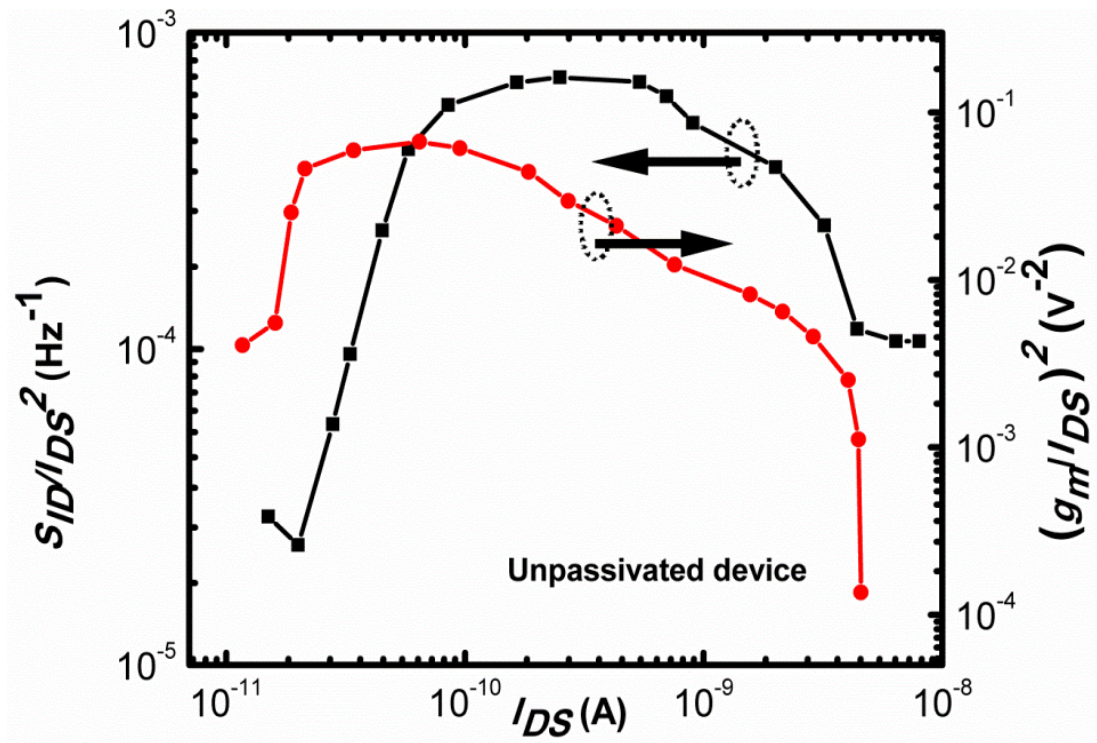


Figure 32 Comparison of normalized PSD of the drain current at $f = 1$ Hz and $(g_m/I_{DS})^2$ at different I_{DS} for unpassivated devices. All the readings were taken at a constant drain-source voltage ($V_{DS} = 0.5$ V).

generate minima in the parabolic plot of gate-referred voltage PSD, where as a pure acceptor-like trap has no minima, as seen in the case of the etched devices. [176]

Figure 35 presents temperature-dependent S_I/I_{DS}^2 at 10 Hz for both etched and passivated devices at three different gate biases. The drain current noise in etched device shows very weak temperature dependence at all three gate biases. This could indicate that the physical trapping mechanism responsible for $1/f$ noise is dominated by a tunneling process. In contrast, the nearly linear normalized drain current spectral density at 0 V gate bias indicates a more thermally-activated trapping process. [175, 176] However, the reason behind the increase in noise due to positive gate bias in the case of passivated devices is not clear. It is also interesting to note that the temperature-dependent field-effect mobility measured on passivated and etched devices showed very similar trends, i.e., the measured field-effect mobility had linear dependence with temperature for the passivated devices, whereas for the etched devices the mobility showed very weak temperature dependence. [178] We can speculate that the nature of transport is different in passivated and etched devices, which ultimately determines the temperature-dependent characteristics of noise in the single-layer MoS₂ devices.

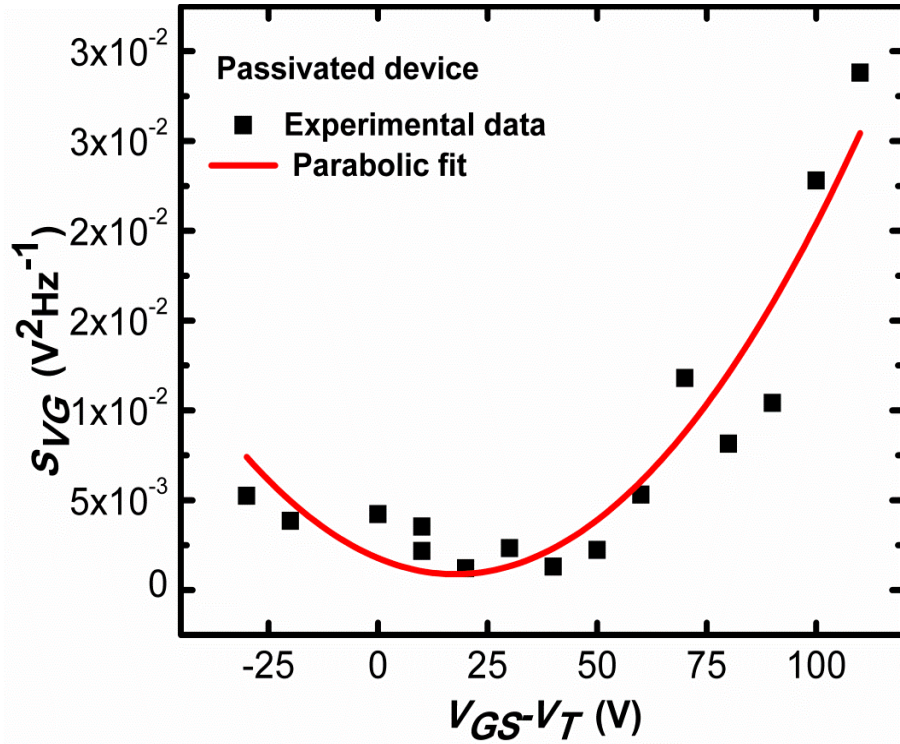


Figure 33 (shows the experimental input gate-referred PSD voltage obtained at different V_{GS} values for passivated devices. Parabolic fit to the measured data points is also shown. All the readings were taken at a constant drain-source voltage ($V_{DS} = 0.5$ V).

Etched devices showed the presence of Lorentian peaks associated with generation-recombination ($G-R$) noise in addition to $1/f$ noise. However, for all the etched devices, transition from $G-R$ to $1/f$ and vice versa was observed during the course of repeated measurements. The PSD associated with $G-R$ noise exhibits a Lorentzian-behavior, i.e., $S_{ID} = A / (1 + (f/f_0)^2)$, where A is the low-frequency amplitude and f_0 is the characteristic frequency. Figure 36 shows the PSD of etched device at 170 K exhibiting $G-R$ related Lorentzian shape in addition to the excess $1/f$ noise. In case of Graphene, few

groups have reported G - R noise and it is attributed to defects on the edges of Graphene channels giving rise to a characteristics time constant in the fluctuations of carriers. [173]

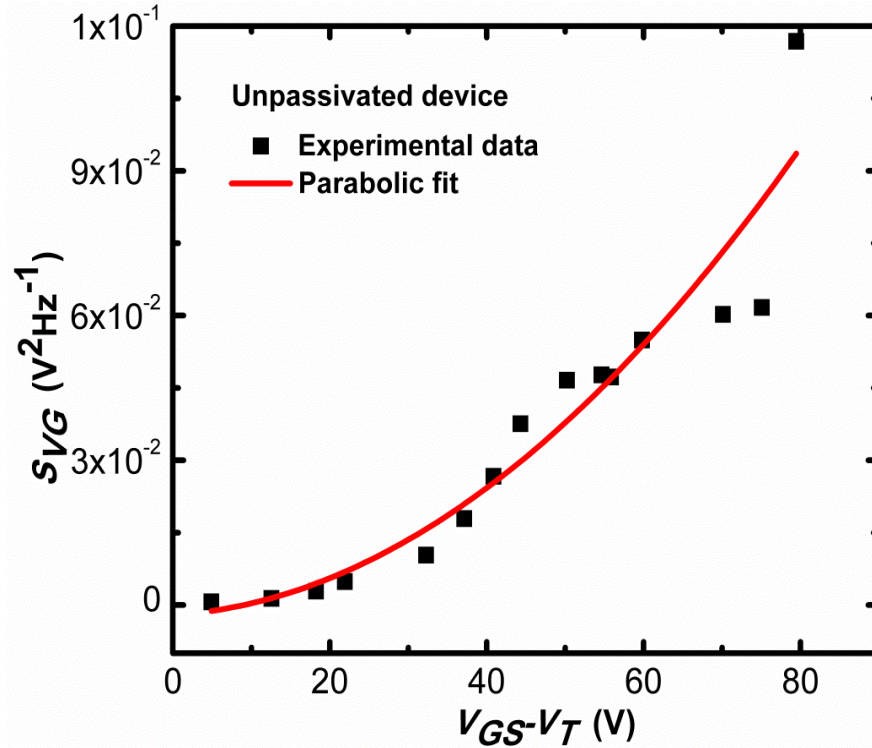


Figure 34 shows the experimental input gate-referred PSD voltage obtained at different V_{GS} values for unpassivated (after etching of the top passivation) devices. Parabolic fit to the measured data points is also shown. All the readings were taken at a constant drain-source voltage ($V_{DS} = 0.5$ V).

Recent report by Sangwan *et al.*, also showed the presence of G - R peaks at low temperature in unpassivated MoS₂ devices. [174] Single time-constant Lorentzian peaks in $1/f$ PSD is due to the presence of discrete traps or G - R centers within the band. For

unpassivated devices this could result from the defect sites on the top surface of the MoS₂ film. However, the unstable nature of the G - R peaks observed in unpassivated devices might be associated with adsorption of molecules at surface defects sites. For example, Balandin *et al.* clearly showed the evolution of characteristic Lorentzian peaks in $1/f$ spectra in graphene devices, due to the adsorption of specific molecules. [171]

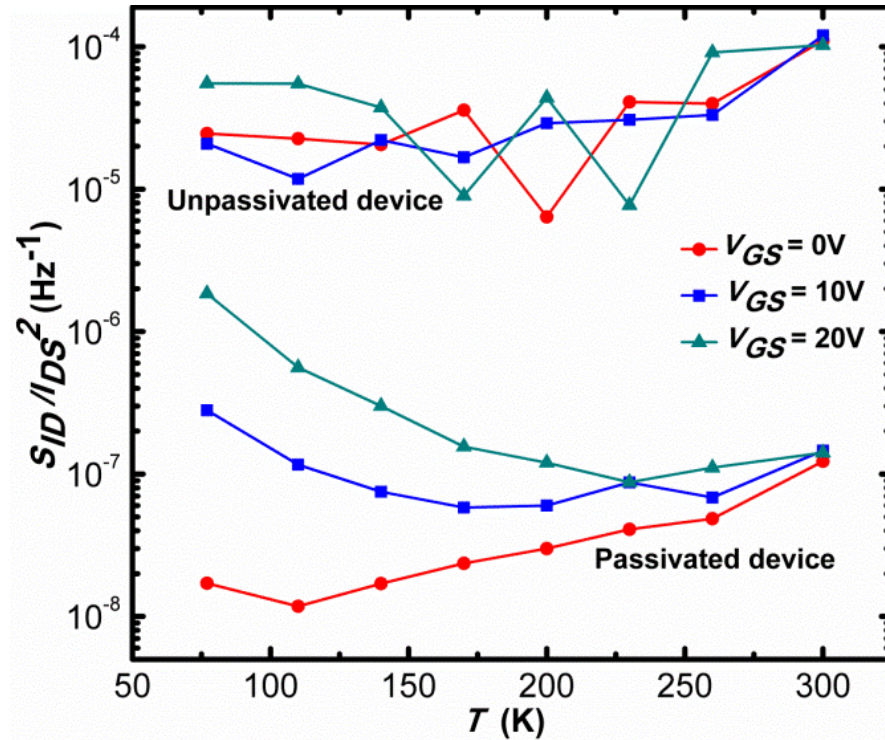


Figure 35 Temperature dependent (77 K to 300 K) normalized PSD of the drain current noise at $f = 10$ Hz at different temperatures for passivated and unpassivated (after etching of the top passivation) devices. All the readings were taken at constant drain-source voltage ($V_{DS} = 0.5$ V).

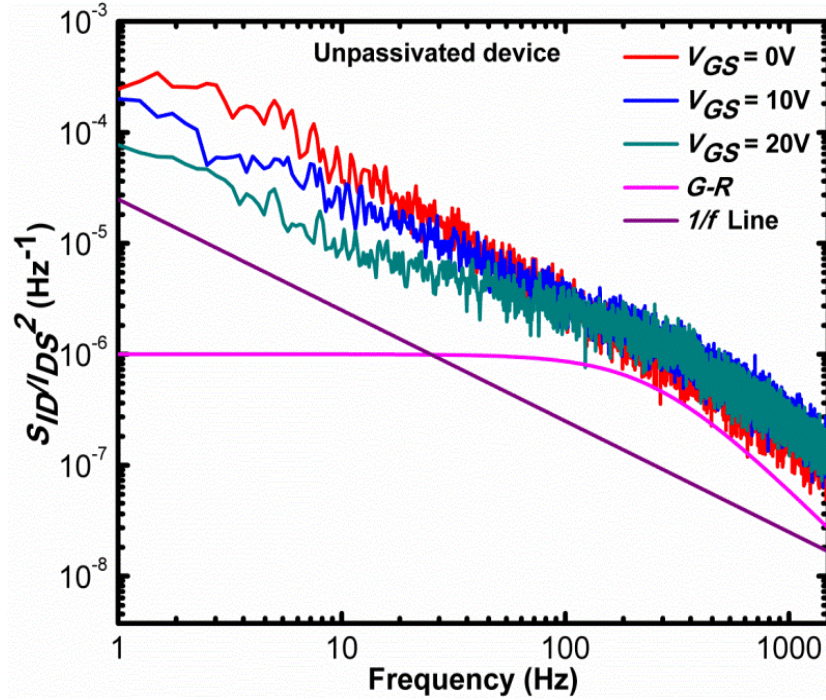


Figure 36 Normalized PSD of the drain current noise for unpassivated (after etching of the top passivation) devices at $T = 170\text{K}$. The $1/f$ trend line as well as ideal single-time constant Lorentzian-type PSD i.e., $S_I = A/(1+(f/f_0)^2)$ due to $G-R$ noise are shown for illustration. Green line (PSD at $V_{GS} = 20\text{V}$) clearly indicates the presence of $G-R$ noise in addition to excess $1/f$ noise. All the readings were taken at constant drain-source voltage ($V_{DS} = 0.5\text{ V}$).

4.5 Conclusion

In summary, I have examined the effects of passivation on transport and LFN in single layer MoS_2 FETs. Temperature-dependent resistance measurements in single layer MoS_2 FETs passivated with ALD-deposited Al_2O_3 indicated a band-like transport mechanism, whereas for etched devices weak temperature dependence of the resistance pointed to a defect-mediated transport mechanism. It was clear that top-surface passivation significantly reduces the drain current noise. For both passivated and etched devices, the bias-dependent LFN at 300 K can be explained by carrier number fluctuation

and correlated mobility fluctuation; both related to surface effects. Correlation to bulk mobility fluctuation model (Hooge's model) was not observed. Temperature-dependent noise measurements showed very weak dependence for etched devices compared to passivated devices. In general, the findings presented in this chapter should contribute to the much needed advancements in 2-D material interface engineering for device applications.

CHAPTER 5 TRANSFER CHARACTERISTICS AND LOW FREQUENCY NOISE IN SINGLE AND MULTI-LAYER MoS_2 FIELD EFFECT TRANSISTORS

In this chapter I have studied electrical transport and low-frequency noise (LFN) in field-effect transistors (FETs) fabricated with different Molybdenum disulfide (MoS_2) layer counts. Free carrier transport in the channel was explained using a model incorporating Thomas-Fermi charge screening and inter-layer coupling. Devices with fewer than 6 layers showed good back gate control over the channel current, while devices with higher MoS_2 layer count had weak dependence. LFN in few layer MoS_2 devices satisfied carrier number fluctuation (CNF) model; on the other hand devices with more MoS_2 layers (approaching bulk) tend to follow Hooge's mobility fluctuation model in the sub-threshold regime, while in strong accumulation regime it still follows Carrier fluctuation model. Based on comparative analysis of both electrical transport and LFN measurements on different layered MoS_2 devices, I found that devices containing 4 to 7 MoS_2 layers may provide the optimum FET performance.

5.1 Introduction

Two-dimension (2-D) materials are gaining considerable attention due to their usefulness in several fields. [186-191] These single and few atom thick layers of van der Waals materials have lots to offer, provided we can overcome the key challenges related

to its growth and device fabrication processes. For several electronic applications, field-effect transistors (FETs) made up of a 2-D material like MoS₂ is considered to be a good candidate, primarily due to its inherent band gap (ranging from 1.8 eV to 1.2 eV for single and multi-layer films respectively), large mobility values (200–500 cm²V⁻¹s⁻¹), high current on/off ratio (<10⁸) and good interface quality with the gate dielectric (≈ 60 mV/decade sub-threshold swing). [186-193] These values for MoS₂ FETs are encouraging from circuit design point of view. One other rudimentary requirement for efficient FETs is the low magnitude of low frequency noise (LFN). Flicker ($1/f$) noise is a major contributor to the LFN and it increases as the reciprocal of the device area and becomes a major concern for deeply-scaled devices (see chapter 1). [194] Moreover, excessive LFN adversely impacts the performance of analog and digital circuits. The $1/f$ noise also puts a limitation on RF circuit design as it gives rise to phase noise in oscillators and multiplexers. [195, 196] Lately, few groups have studied LFN in MoS₂ FETs. [197-200] These results suggest that in single and few layers MoS₂ FETs, LFN is dominated by trapping and de-trapping the charge carriers at the interface and is described by carrier number fluctuation (CNF) model. Notably, Sangwan *et al* explained the LFN using Hooge mobility fluctuation (HMF) model implying the bulk conduction in single layer MoS₂ FETs. [198] Kim *et al* explained LFN in thick MoS₂ (~40nm) using combination of HMF and CNF models. [199] Although these results are insightful, there has been little effort towards optimization of FETs with respect to MoS₂ layer count taking both LFN and I_{DS} - V_{GS} properties into account. In this work I systematically study the transport and low frequency noise properties in back-gate controlled FETs fabricated

from mechanically exfoliated MoS₂. Different sets of FETs were fabricated based on the MoS₂ layer count, ranging from single layer to bulk. Electrical transport and LFN measurements suggest that 4 to 7 layers have relatively good transport and LFN characteristics. Layers less than 4 have relatively higher magnitude of LFN while layers over 6 have weaker back gate voltage (V_{GS}) control over the channel current (I_{DS}) since magnitude of off current is higher (< one order of magnitude) compared to mono- and bilayer devices.

5.2 Experimental details

MoS₂ films of various thicknesses were prepared by micromechanical exfoliation via the scotch tape method on a heavily doped Si substrate with a 300 nm SiO₂ back gate. Films with various thicknesses were located by optical microscopy and the layer count was estimated by Raman and PL spectroscopy. Back gated transistors were then fabricated on various MoS₂ flakes using electron-beam lithography processes (EBL). Devices were patterned using a low power reactive ion etch in a CH₄/O₂ plasma and Ti/Au (15/85 nm) contacts were subsequently deposited using electron beam evaporation.

The LFN measurement was done in an open-cycle cryogenic probe station. The drain and gate bias was provided by the Agilent B1500A semiconductor parameter analyzer, and the channel current was converted to voltage using SRS 570 low-noise current amplifier. The experimental setup is shown in figure 6.

5.3 Results & Discussion

Figure 37 shows the I_{DS} vs. V_{DS} characteristics at $V_{GS} = 30$ V for different MoS₂ layer FETs at 300 K. It clearly shows that there is a gradual increase in the magnitude of I_{DS} (vs V_{DS} in strong accumulation region) as the number of MoS₂ layers is increased, although current tends to decrease in devices approaching bulk MoS₂.

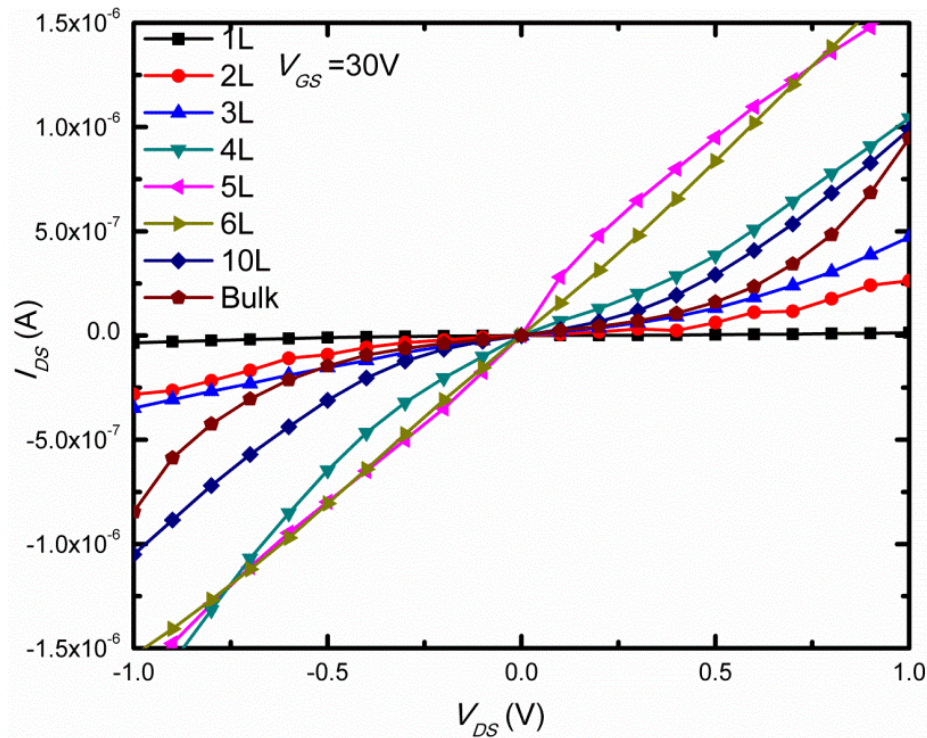


Figure 37 I_{DS} - V_{DS} plot at 300 K for FETs with different number of MoS₂ layers. All the I - V curves were taken at constant gate-source voltage ($V_{GS} = 30$ V).

It is worth pointing out here that multilayer MoS₂ has large current density due to its lower band-gap and triple density of states at the conduction band minima when compared to monolayer MoS₂. [201, 202] Also, two terminal resistance for these MoS₂ FETs as a function of measurement temperature is shown in figure 38. Using the relationship:

$$\ln(R) = \ln(R_0) + E_a/2k + k_B T \quad (28)$$

where R_0 is the intercept, E_a is the thermal activation energy of the dopant, k_B is the Boltzmann's constant, and T is the absolute temperature, we can compute the activation energy for conduction in these devices. Calculations showed two different regimes of activation energy in 77K to 320K temperature range, with weaker temperature dependence at low temperatures. The calculated activation energy (between 200 K to 320 K) at 60 V back-gate bias was in the range of 70 meV to 140 meV for different FETs. This variation in activation energy may be well due to variation in contact resistances from device to device. We have also shown in our previous work that activation energy is dependent on the back gate voltage variations. [197, 203]

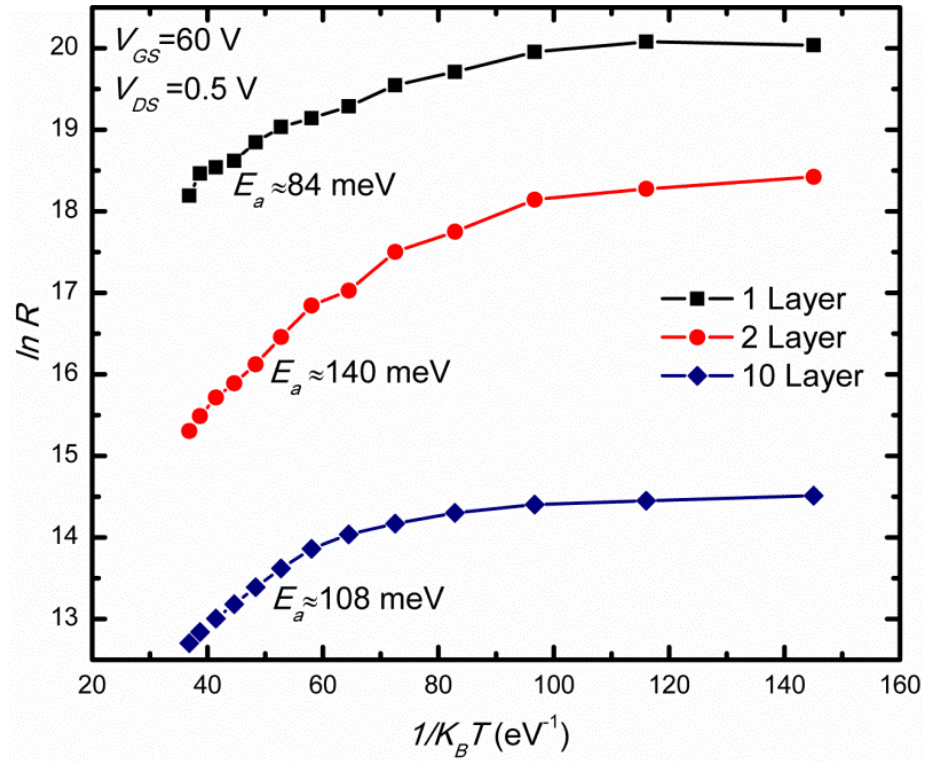


Figure 38 Arrhenius plot of the drain-source resistance of the drain current for FETs with different number of MoS₂ layers.. Temperature is in the range of 77 K to 300 K. All the readings were taken at a constant drain-source voltage ($V_{DS} = 0.5$ V) and gate-source voltage ($V_{GS} = 60$ V).

A measured transfer characteristics plot (I_{DS} versus V_{GS}) for different FETs is shown in figure 39. It is evident that all the devices show depletion mode n -channel behavior. Comparing these devices with respect to turn *on/off* behavior it is clear that thicker channel devices have weak gate voltage control over the channel current. On the other hand, single and few-layers devices show strong gate voltage control over the channel current. Also, bulk MoS₂ devices showed saturation in the strong accumulation regime as evident in the figure 39. This observation, i.e., channel thickness dependent transfer characteristic is important for the optimization of FET's operation. Estimated

field-effect mobility values of 14.7, 16.7, and 15.3 $\text{cm}^2/\text{V}\cdot\text{s}$ for monolayer, bilayer, and bulk devices respectively via four point probe measurements which remove the effect of

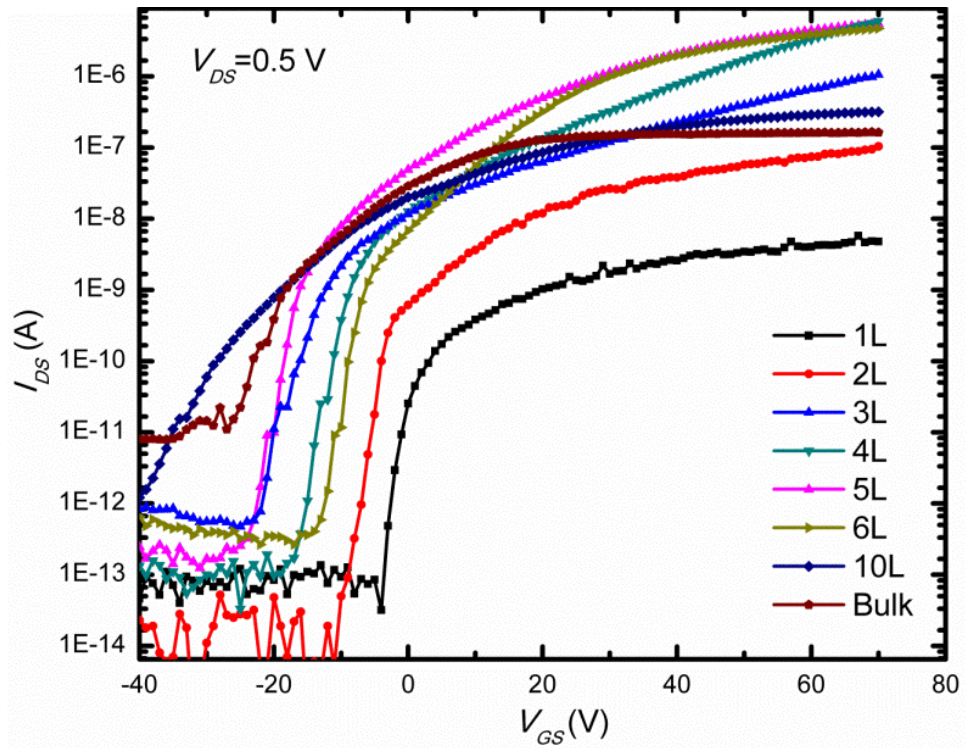


Figure 39 I_{DS} - V_{GS} plot of the FETs with different number of MoS₂ layers. logarithmic-linear scales at 300 K.

contact resistance using the known relationships.[197] Intrinsic mobility measurement values of MoS₂ FETs are highly prone to errors due to factors such as the contribution of high contact resistances and accurate estimation of gate capacitance. A better

understanding of the device behavior under on-state can be obtained from figure 40 which is based on the model incorporating Thomas-Fermi charge screening and inter-layer coupling. [205, 206] This model assumes that total charge on the gate is given by $Q_{Gate} = C_{OX} (V_{GS} - V_{TH})$ (C_{OX} is the gate oxide capacitance, V_{GS} is gate bias and V_{TH} represents threshold voltage) will be mirrored by the total induced charge in the channel, irrespective of the number of MoS₂ layers. Exact distribution of the charge in the channel depends on the total number of layers and screened coulomb potential distribution function. Two adjacent layers of MoS₂ are held together by van der Waals forces giving rise to weak electronic coupling between them. This weak coupling results in higher resistive path for conduction across the layers than within the layer. It can also be assumed that the source and drain contacts inject charge carriers from the top MoS₂ layer only, which is a reasonable assumption, since top surface contact area is significantly higher than metal contacts with the edges of the MoS₂ layers. In addition to that, the contact metals were evaporated at around room temperature and did not undergo any high temperature annealing which makes diffusion of the metal into the MoS₂ layers or any chemical reaction of the metal with the MoS₂ highly unlikely. Therefore, our source and drain metal electrodes form surface contacts to MoS₂ instead of volume contacts.

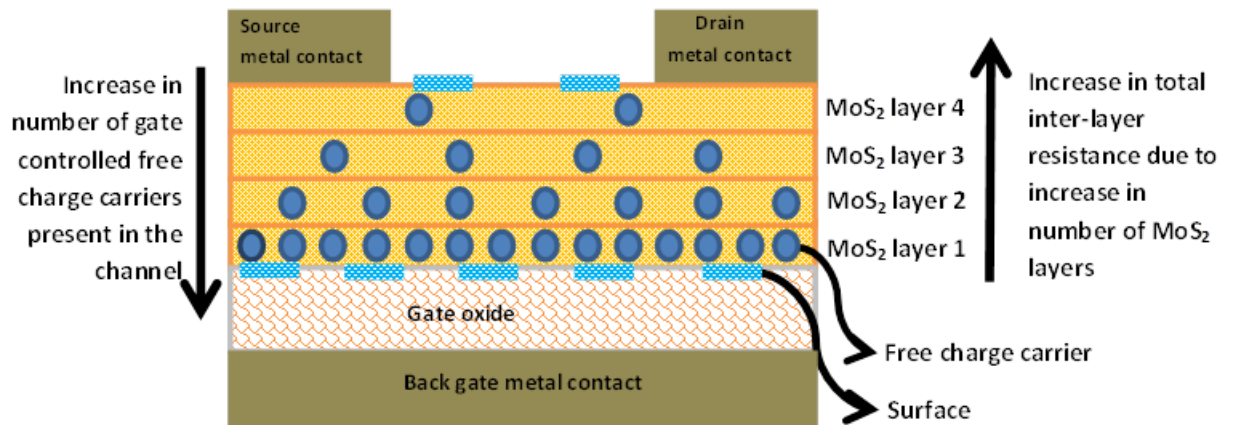


Figure 40 shows the back gated FET device structure with different MoS₂ layers (4 layers are shown here). It also gives the trend in free carrier distribution among the channels when FETs is turned on. Surface states are also shown to foster better understanding of the conduction mechanism.

When a positive back gate voltage is applied, most of the free carriers are accumulated in the MoS₂ layer closest to the gate oxide and decreases in a progressive manner in the subsequent layers due to screening of the gate voltage as well as inter layer resistance contributions. Hence, flow of I_{DS} in the device is largely due to conduction in the bottom most layer of MoS₂, closest to the gate oxide. Hence, the channel current making its way to source and drain contacts have to flow across several layers of MoS₂ in multilayer devices. For large number of MoS₂ layers the interlayer resistance increases significantly, in addition to the contact resistance, effectively decreasing the devices mobility. [193, 205] Similarly, in the off state it is difficult to turn off the FET completely due to weak gate voltage (due to high inter layer resistance and screening of the gate voltage) control over the layers relatively far from gate oxide. Since layer closest to gate oxide acts as the most conductive layer, surface states at the gate oxide interface greatly affect the mobility

values by scattering of charge carriers. Top layer surface states will have little impact on the thicker devices, but plays important role in few layer devices as it is a significant addition to the total number of surface states present in the device. [197] As mentioned earlier, contact resistance is also a critical issue in these devices and Scandium has proven to be a better candidate for source and drain metal due to low Schottky barrier height. [193] Overall, these results show that multi-layer device performance is limited by total interlayer resistances and surface charge screening, while surface states dictate the performance of few layer devices.

To gain more insight into the nature of conduction and the effects of surface states and the multilayer MoS₂, I performed LFN on these devices. The normalized drain current PSD $(S_{ID}/I_{DS})^2$ at $V_{DS} = 0.5\text{V}$ and $V_{GS} = 60\text{ V}$ for different layer thicknesses is shown in figure 41. There was no significant decrease in the normalized drain current noise for mono- and bi-layer thick MoS₂, suggesting that the LFN is mainly dominated by surface states. For thicker devices (≈ 2 to 7 layers thick), the normalized drain current PSD decreased by as much as two orders of magnitude, suggesting conduction occurs in layers relatively far from gate oxide. For very thick devices approaching bulk material, the normalized drain current PSD showed an overall decrease in magnitude. This is probably because of increase in overall interlayer resistance which result in decreased

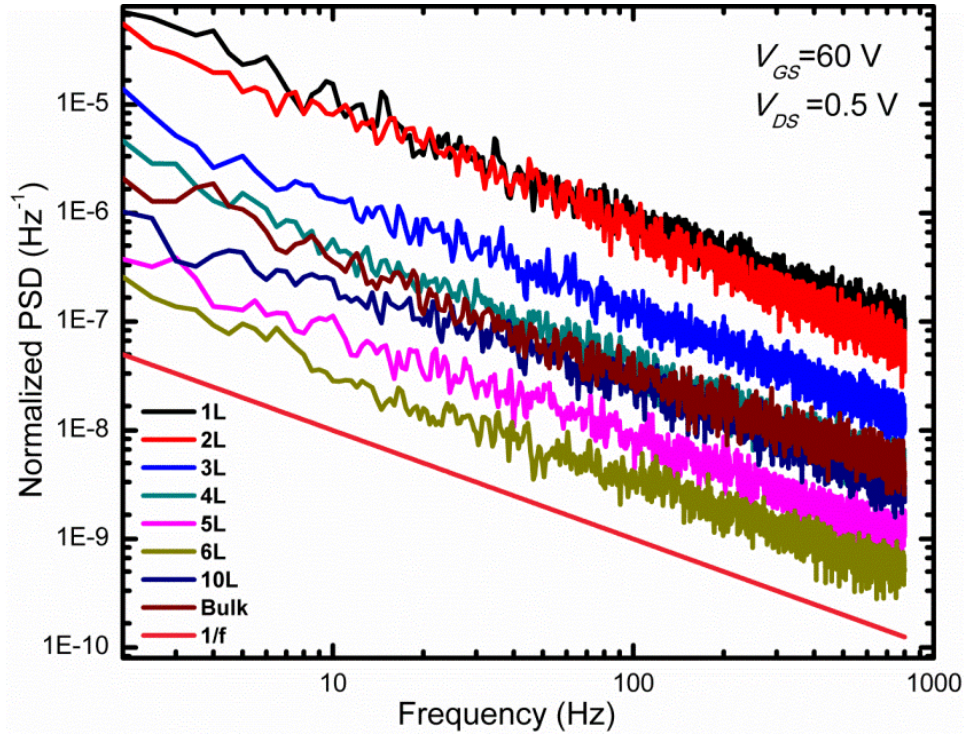


Figure 41 Room temperature ($T = 300$ K) normalized PSD of the drain current for FETs with different number of MoS_2 layers. A $1/f$ trend line is shown for comparison. All the readings were taken at a constant drain-source voltage ($V_{DS} = 0.5$ V) and gate-source voltage ($V_{GS} = 60$ V).

channel current in bulk devices. More insight into the cause of LFN mechanisms can be gained if we plot normalized drain current spectral density as a function of drain current (I_{DS}) in a log-log scale. If the normalized drain-current PSD (S_{ID}/I_{DS}^2) varies with the drain current as $(gm/I_{DS})^2$, i.e., $S_{ID}/I_{DS}^2 \propto (gm/I_{DS})^2$, the CNF is the dominant source of the $1/f$ noise. CNF occurs due to the trapping and de-trapping of free-carriers by the oxide-semiconductor interface traps and is given by relation:

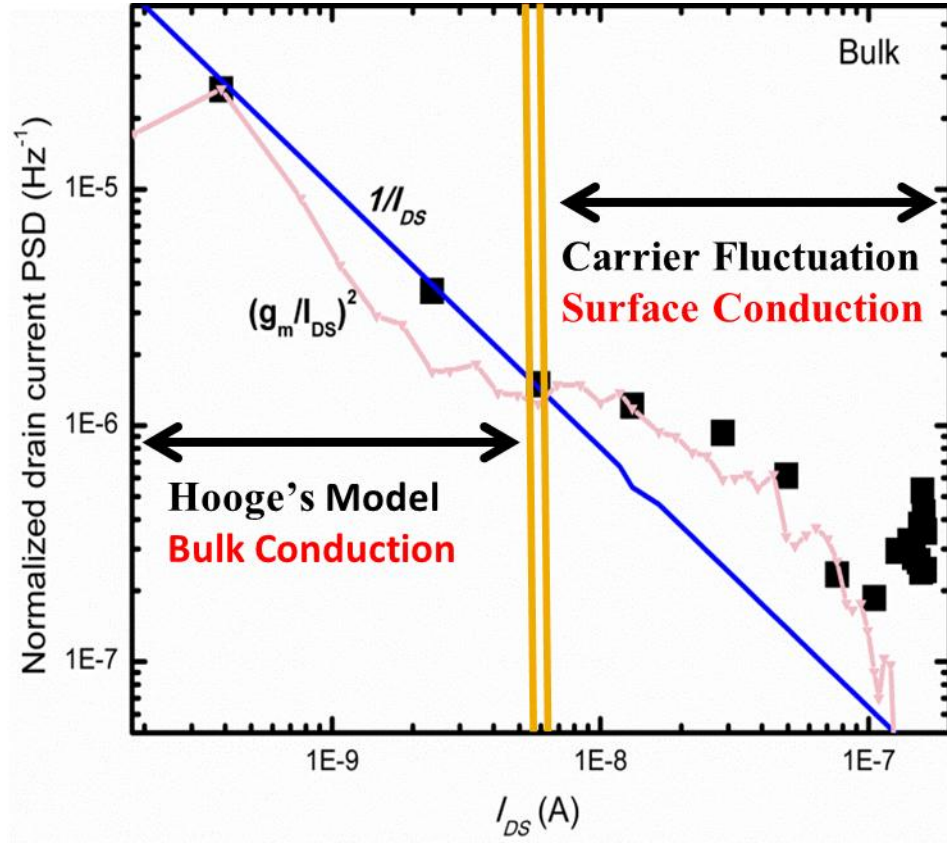


Figure 42 Comparison of normalized PSD of the drain current at $f = 10$ Hz, $(g_m/I_{DS})^2$ and $1/I_{DS}$ at different I_{DS} for 10+ Layers thick MoS₂ FET. All the readings were taken at a constant drain-source voltage ($V_{DS} = 0.5$ V). $(g_m/I_{DS})^2$ and $1/I_{DS}$ Y-axis data is scaled by a constant factor to fit the normalized PSD data.

$$\frac{S_I}{I_{DS}^2} = \left(\frac{g_m}{I_{DS}}\right)^2 S_{V_{fb}} \quad (29)$$

where g_m is the gate transconductance and $S_{V_{fb}}$ is the flat band voltage spectral density, given by relationship:

$$S_{V_{fb}} = \frac{q^2 k_B T N_{it}}{W L C_{ox}^2 f} \quad (30)$$

where q is the electronic charge, k_B is the Boltzmann constant, T is the Temperature in kelvin, W and L are width and length of the channel, respectively, N_{it} is the interface trap density, C_{ox} is the gate capacitance per unit area, and f is the frequency. On the other hand if the normalized drain-current PSD is proportional to I/I_{DS} the HMF is dominant. Hooge's mobility fluctuation model is given by relation (explained in section 1.6):

$$\frac{S_I}{I_{DS}^2} = \frac{q \alpha_H}{f W L Q} \quad (31)$$

where α_H is the Hooge constant, and Q is the total charge. It is worth pointing out that HMF is a bulk-effect while CNF is a surface effect. Figure 42 and 43 shows the measurement data for bi-layer and bulk MoS₂ FETs respectively. It was evident from the figure that in the strong accumulation and in sub-threshold regime, mono- and few-layers devices followed CNF model more accurately. In the strong accumulation region, bulk devices satisfied CNF model but in sub-threshold regime S_{ID}/I_{DS}^2 clearly followed HMF model. If we look at the $I_{DS}-V_{GS}$ of relatively thick devices, it is clear that *off* current is significantly higher (almost by two orders of magnitude) than the few layer devices. These findings indicate that there is conduction in the layers that are not in the proximity of the gate oxide, resulting in weak gate control (due to high inter-layer resistance) and low level of LFN (due to conduction far from the gate oxide interface).

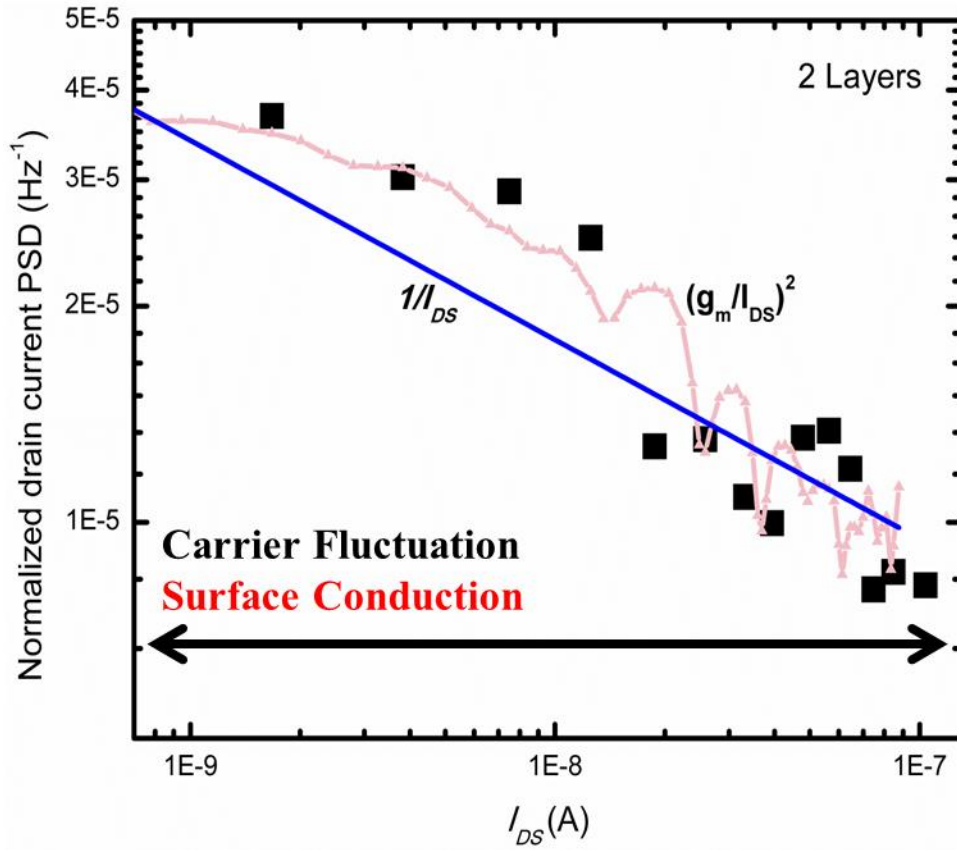


Figure 43 Comparison of normalized PSD of the drain current at $f = 10 \text{ Hz}$, $(g_m/I_{DS})^2$ and $1/I_{DS}$ at different I_{DS} for 2 Layers thick MoS₂ FET. All the readings were taken at a constant drain-source voltage ($V_{DS} = 0.5 \text{ V}$). $(g_m/I_{DS})^2$ and $1/I_{DS}$ Y-axis data is scaled by a constant factor to fit the normalized PSD data.

Also due to saturation of channel current in bulk devices, normalized LFN (S_{ID}/I_{DS}^2) showed increase in the magnitude as shown in figure 41. Further investigation is needed to understand these transport phenomena.

5.4 Conclusion

I have performed electrical transport and LFN measurements on different FETs with varying number of MoS₂ layers. The measurements related to transport and LFN

suggest that optimum device performance can be achieved by few-layer MoS₂ device rather than through monolayer or very thick MoS₂ devices. Devices ranging between 4 to 7 layers thick showed good I_{DS} - V_{GS} characteristics as well as relatively low $1/f$ noise. Devices with thick MoS₂ suffers from low mobility values, weak dependence of channel current on V_{GS} , and increase in LFN value due to increase in inter layer resistances, while conduction in mono- and few-layer devices suffer from surface states at oxide-semiconductor interface and shows higher LFN. Presented results are crucial in optimizing two dimensional devices.

CHAPTER 6 SUMMARY AND FUTURE WORK

6.1 Summary

My research has primarily focused on understanding the nature and impact of defects and surface states on the overall carrier transport in silicon nanowire and MoS₂ based Field-effect transistors. For my study, I have primarily used low frequency noise (LFN) as a diagnostic tool. This study emphasizes the role and importance of precise low frequency noise studies on nanoscale semiconductor devices. Two types of devices used in my studies are:

6.1.1 Silicon Nanowire FETs

I have used correlated LFN method to probe deep-levels in *p*- and *n*-type SiNWs grown by the vapor–liquid–solid (VLS) mechanism using Au and Ni catalysts. The power spectrum density (PSD) spectra showed clear Lorentzian behavior in all NW FETs due to the *G-R* processes. Temperature dependent noise analysis clearly indicated that the traps responsible for the *G-R* noise are due to the deep-levels introduced by Ni and Au atoms, which diffused unintentionally into the Si lattice during the VLS growth. The trap concentration, hole and electron capture cross-section were also estimated for all four sets of FETs. This study identifies the LFN spectroscopy as an alternative to DLTS and optical measurements for characterization of deep-levels in semiconductor nanowire

materials. This work shows that optimized noise measurement technique can be very useful in estimating the quality of semiconductor nanoscale devices in general.

6.1.2 Molybdenum Disulfide FETs

I performed temperature dependent electrical transport and LFN measurement on monolayer-layer MoS₂ FETs prepared by chemical vapor deposition (CVD). The effect of high- κ dielectric passivation on the electrical transport properties revealed key aspects related to activation energy. Devices passivated with ALD-deposited Al₂O₃ indicated a band-like transport mechanism. Devices with etched top surface passivation showed weak temperature dependence of the resistance pointed to a defect-mediated transport mechanism. The observed channel current noise revealed different trapping states in passivated devices when compared to the devices without high- κ dielectric passivation. For both passivated and etched devices, noise can be explained by carrier number fluctuation and correlated mobility fluctuation; both surface effects. I also studied electrical transport and LFN characteristics in FETs consisting of different number of MoS₂ layers. Based on comparative analysis of both electrical transport and LFN on the MoS₂ FETs with different number of layers, I found that devices containing 4 to 7 layers provided optimum FET performance. Devices with thick MoS₂ (approaching bulk) suffers from low mobility values, weak dependence of channel current on gate voltage and increase in normalized LFN value, while conduction in mono- and few-layer devices is affected by surface states at oxide-semiconductor interface and shows much higher normalized LFN.

6.2 Future Work

Although my work has shown that low frequency noise serves as an effective diagnostic tool to understand the quality of semiconductor nanoscale devices, there are many aspects to it that needs to be addressed.

6.2.1 From Noise Perspective

From noise point of view, this study suggests that the $1/f$ noise can be significantly reduced by clever approaches which in part include better material growth techniques, better interface quality by improved fabrication techniques and smart choice of materials. In addition, reduced low frequency noise and $1/f$ in particular improves devices performance and encourages further scaling down of the devices. Since noise is one of the key difficulties in the RF and analog circuit design, reduction in intrinsic noise at transistor level becomes extremely important. From the noise theory point of view, in order to minimize the device $1/f$ noise, an understanding of the noise mechanisms, the underlying physics and the location of the sources is necessary. For example, after several decades of debate, the exact origin of the $1/f$ noise is in many aspects an open question.

6.2.2 From Material Perspective

My study revealed the presence of deep levels in SiNWs. They are detrimental to the material quality and device performance. In that regard, different growth methods also need further exploration to get better and reproducible material quality and device characteristics. Also, it is suggested that careful production of nanowires of desired size

and shape would make it possible to tune the properties like band-gap, effective mass and optical absorption. There is still a large amount of work to be done to make it viable. High- κ dielectrics (HfO_2 , Al_2O_3 , ZrO_2 , Y_2O_3) for gate oxide and surface passivation is already being explored for better control over channel current, high gate capacitance, low leakage when compared to SiO_2 .

In case of 2D material like MoS_2 I observed different trapping states due to presence of different nature of interfaces. I have further showed how the back gate voltage is capable of tuning the electronic properties like the activation energy of the MoS_2 FETs. From my observations, it is possible to dynamically tailor device characteristics. Since the gate tunability does not exist in bulk semiconductors, devices that exploit it are unlikely to face competition from conventional bulk materials.

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