NOVEL NON-VOLATILE MEMORY AND TOPOLOGICAL INSULATOR FIELD-EFFECT TRANSISTORS

by

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Abstract

NOVEL NON-VOLATILE MEMORY AND TOPOLOGICAL INSULATOR FIELD-EFFECT TRANSISTORS

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The dimensional scaling of microelectronics to increase the ability of central process unit (CPU) is facing fundamental and physical challenges. The integration of high-performance non-volatile memory as the local memory in CPU will have a transformative impact on mobile electronics and portable systems. This dissertation proposes replacing the static random-access memory (SRAM) which is currently used as the local cache memory in CPU with high-performance Flash-like non-volatile memory for the consideration of memory density and power consumption. I have fabricated, fully characterized and compared different kinds of Flash-like charge-trapping non-volatile memory devices, including high-*k* dielectric charge-trapping devices, multi-stack discrete memory devices and molecular memory devices. The devices containing redox-active molecules exhibit excellent Program/Erase (P/E) speed, good retention and excellent P/E endurance for more than 10^9 cycles. The charge storage in these molecule-containing memory devices is naturally derived from the intrinsic redox processes of the molecules

under a voltage bias. This is very different with other charge storage mediums in which the charge is stored in the trap centers or as a carrier. The intrinsic redox properties and the naturally derived, stable molecular structure make this memory very robust and reliable.

The second part of the dissertation will discuss my research on one of the most attractive emerging materials: topological insulators. I have used the nanowire growth method and self-alignment processes developed by us for the non-volatile memory to fabricate the topological insulator nanowire field-effect transistors. This work experimentally demonstrates that the conduction of bulk Bi_2Se_3 and surface gapless conduction are apparently separated; the current of these devices can be tuned to have large On/Off ratio and close-to-zero Off state; and the carrier transport on the surface is mainly affected by the Columbic scattering. We have also observed the anomalous Aharonov-Bohm oscillation in these topological insulator nanowire field-effect transistors, which leads to new understanding about the quantum phenomena in these materials. All the above findings will open up a suite of potential applications in nanoelectronics and spintronics.

Chapter 1 Introduction

1.1 CMOS Scaling and Impact on Non-Volatile Memory

The *2013 International Technology Roadmap for Semiconductors* (ITRS) stated that the scaling of metal-oxide-semiconductor field-effect transistor (MOSFET) continues with the emergence of new technologies to extend complementary metal-oxide-semiconductor (CMOS) down to and beyond 22-nm technology node. [1] However, the CMOS scaling has deviated from the trends predicted by Moore and the scaling rules set forth by Dennard *et al.* due to fundamental physical and technical limitations in recent decades. [2, 3] The pace of future CMOS scaling will inevitably slow down and eventually stop probably at a 5-nm node where the lithography scale approaches a few times of atomic dimension. [4-6] Scaling limitations of ultra-thin gate oxide, channel length modulation, and FET series resistance have become a growing concern on maintaining speed, density, reliability and power dissipation.

Recent logic device research and development to enable solutions toward CMOS scaling challenges has taken the torch and carried it forward thus far. For example, barriers such as doping, carrier transport and series resistance scaling have been effectively avoided by innovations such as source/drain processes upon silicon-on-insulator (SOI) structure, multi-gate FET, and SiGe BiCMOS technologies. [7-11]

Today, computing architectures and electronic systems built on CMOS components are still pursuing without signs of slowing down of requirements for low power, fast speed and high density alternatives. [12, 13] Despite the lagging development behind the CMOS logic device scaling, exponential growth of the semiconductor industry has proceeded in recent years upon the progress of the former. Various scenarios of technology with new materials and structures have been proposed and studied for real device applications. Such approaches toward fundamentally new technologies mainly include quantum computing, DNA computing, single/few electron devices, spin transistor and molecular electronics for the applications in logic and memory devices.

Electronic systems whose main functions lie in data computing and data storage take up more than half of the semiconductor market, and the demand is still growing explosively in areas such as portable electronic devices and systems. Solid-state mass storage occupies a large portion of this market, due to their compatibility with CMOS scaling technology, suitability for harsh environment without mechanical parts, and the fact that most types of memory are non-volatile, which means that the data information can be maintained even without power supply. Currently, main types of non-volatile memory technology have been investigated, including ferroelectric random-access memory (FeRAM), magnetic random-access memory (MRAM), resistive random-access memory (RRAM), phase-change random-access memory (PCRAM), and Flash memory. [14-18]

Non-volatile memory is typically employed for the task of secondary storage or long-term storage, which usually does not require fast operation speed or integration

density. Most types of non-volatile memory have limitations and are not suitable for use as primary storage or on-chip memory, which currently relies upon volatile forms of random-access memory. During the past decades, the size of cache memory in the central processing unit (CPU), which is also known as the static random-access memory (SRAM) has been doubled several times as a feasible strategy to increase the CPU capability and performance. However, increasing SRAM will decrease CPU net information throughput because it is volatile and occupies a large chip floor space. Dynamic random-access memory (DRAM) is the other on-chip memory in CPU. Unlike SRAM which usually consists of four or six transistors, a DRAM cell consists of only one transistor and one capacitor (1T1C). Thus its cell size is much smaller than that of SRAM. However, the operation speed is slower in DRAM than in SRAM, and moreover, DRAM is also a volatile memory, so periodic refreshing is required for DRAM to retain the data. As a result, it will be a revolutionary breakthrough in microelectronics if a truly non-volatile memory can be implemented as the on-chip memory in CPUs replacing both SRAM and DRAM. Because CPUs with high-performance on-chip non-volatile memory will have more cache memory and consumes less operation power, they can enable the next-generation of low-power portable electronics. Table 1.1 compares the mainstream non-volatile memory technologies.

Table 1.1 Comparison of emerging non-volatile memory technologies

	NOR Flash	NAND Flash	PCRAM	FeRAM	MRAM	RRAM
Cell	1T	1T	1T1R	1T1C	1T1R	1T1R
Program voltage	7-9 V	15 V	< 3 V	1 ~ 3 V	~ 2 V	< 1 V
Read voltage	2	2	~ 3	1 ~ 3	1.5	0.5
Speed	μs / ms	ms	ns	ns	ns	ns
Endurance	10^5	10^5	10^9	10^{12}	10^{15}	10^6
Retention	10 years	10 years	10 years	10 years	10 years	10 years
CMOS compatibility	/	/	No	No	No	Good

From Table 1.1, it is not difficult to find out that there currently is no best candidate for next-generation non-volatile memory applications which requires a combination of fast speed, low working voltage, high endurance and CMOS compatibility. Up to now, based on these emerging non-volatile memory, scientists and engineers have been devoting great effort on optimizing the memory technologies through various approaches for new high-performance memory device. [19]

1.2 Flash Non-Volatile Memory

Among all the non-volatile memory candidates for primary storage applications, Flash memory is the most widely studied and electrically accessible form, and is the most promising non-volatile memory in the electronics market. Flash memory has fast read access times, good retention and reliability, and CMOS compatible fabrication process. [20-22] A Flash-like non-volatile memory with better endurance may be considered for the local memory in CPU.

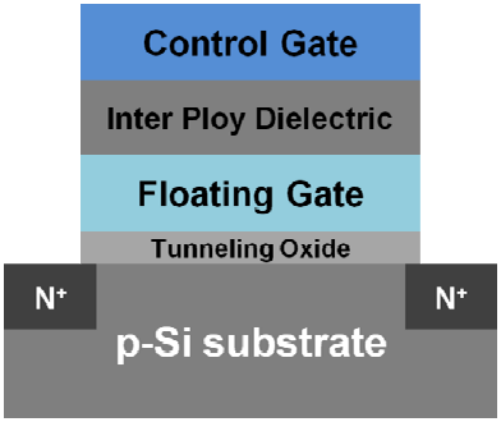

Fig. 1.1 Schematic diagram of a floating-gate Flash memory

Fig. 1.1 illustrates the schematic structure of a Flash memory. Also known as the floating-gate memory, a Flash memory device stored the trapped electrons in the floating gate, which is insulated from the control gate and the MOSFET channel by a relatively thick blocking oxide and a thin tunneling oxide, respectively. Because the floating gate is electrically isolated, the trapped electrons can be retained for many years. Two main types of Flash memory have been put into commercial production according to different logic architectures – NOR type and NAND type, as demonstrated in Fig. 1.2.

NAND Flash architecture was introduced by Toshiba in 1989, while Intel put NOR Flash into commercial production earlier in 1988. In a NAND Flash, transistors are connected in series, resembling a NAND gate. The series connection characterized by longer access times occupies less space than parallel counterparts, reducing the cell size and cost of NAND Flash, and is mainly used for data storage. In a NOR Flash, cells are

connected in parallel to the bit lines, enabling individual reading and writing of the cells. NOR Flash has larger cell size, but faster access, and is mainly used for code storage.

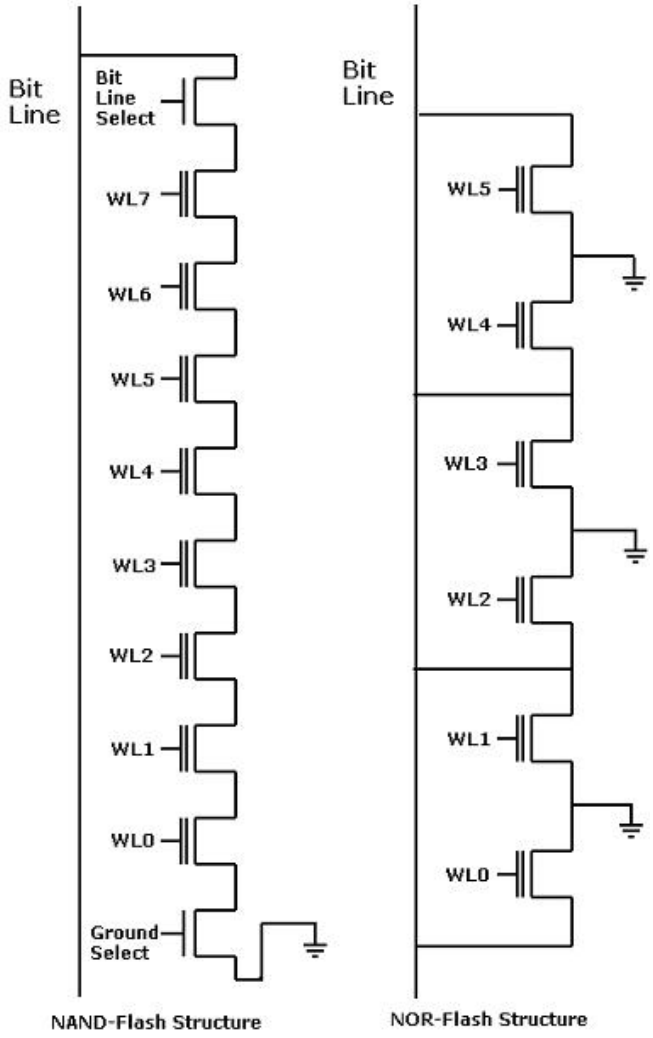

Fig. 1.2 Type NAND and type NOR Flash structures

Different from the regular electrically erasable programmable read-only memory (EEPROM) which erases its content one byte at a time, Flash memory erases its information by entire blocks, making it much faster to update data than EEPROM. Flash

memory has been a preferable technology for many years for applications that require frequent reading and writing of large amounts of data, such as memory stick and other solid-state storage for digital electronic devices. The capacity, integrated density and performance have been continued to increase for Flash memory with dropping manufacture cost and price. The floating-gate transistor architecture of a Flash memory is compatible with conventional CMOS process. It is easier and more reliable to integrate Flash memory than other forms of non-volatile memory in logic and analog devices with increasing embedded and stand-alone memory to achieve higher chip performance.

However, current Flash memory also exhibits disadvantages such as relatively slow program/erase (P/E) speed and to be improved endurance, which are still far below the standards of on-chip memory. With the scaling of semiconductor Flash memory, which is far behind CMOS scaling, the floating-gate memory will suffer from short-channel effects when the channel length is scaled below 100 nm. Leakage current will be significant during P/E operations due to both drain-induced barrier lowering (DIBL) and sub-surface punch-through effects.

In a conventional floating-gate Flash memory, the tunneling oxide in the gate stack can hardly be scaled below 7-8 nm due to the requirement of data retention. On the other hand, floating-gate memory with ultra-thin tunneling oxide layer suffers from severe stress-induced leakage current (SILC) issue. Thus it is difficult to decrease the programming voltage due to the relatively thick tunneling oxide in conventional floating-gate memory. In addition, the conventional floating-gate materials, poly Si and oxynitride operate at large programming voltages too, and endure only 10^5 P/E cycles. Typically, the

programming voltages are in the order of 4-9 V for NOR and 18-20 V for NAND. Even though some new Flash technologies are promising for low-voltage operations, the voltage supply is in excess of the working voltage standard of advanced processes, and the gap between the operation voltage of memory device and CMOS logic continues to be broadened.

1.2.1 Dielectric Charge-Trapping Flash Memory

In recent decades, charge-trapping non-volatile memory has attracted intensive attention to replace the conventional floating-gate memory, due to their advantages such as better scalability, lower power consumption, improved reliability, and simpler structure and fabrication process. [23-26] In a charge-trapping Flash, the electrons are stored in a trapping layer, instead of a conducting floating gate in the Flash memory. Generally, the charge-trapping memory can be mainly classified as three types: polysilicon-oxide-nitride-oxide-silicon (SONOS), nitride-based read-only memory (NROM), and nanocrystal memory (NCM). [27-32] The NROM has good data retention due to thicker tunneling layer. However, thicker tunneling layer requires higher P/E voltages, resulting in larger power consumption during the operations. The NROM also has drawbacks such as erase saturation and vertical stored charge migration. NCM has been considered as a promising non-volatile memory. However, to control the size, density and uniformity of nanocrystal distribution are still challenging concerns. Much more delicate fabrication process is still to be developed for realizing real applicable NCM.

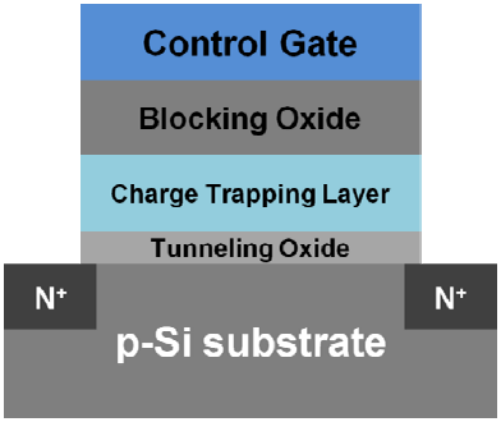

Fig. 1.3 Schematic diagram of a SONOS charge-trapping memory

SONOS is one of the earliest forms of charge-trapping memory. [33] Evolving from the traditional metal-nitride-oxide-silicon (MNOS) devices that lead the semiconductor memory in 1960's, SONOS has been studied and optimized for decades. [34] Fig. 1.3 demonstrated the schematic structure of a SONOS charge-trapping memory. In SONOS devices, the electrons tunnel through the tunneling layer and are stored in the nitride layer. Unlike the conventional floating-gate memory in which a single defect may discharge the stored charge in the device due to the conductive floating polysilicon gate, SONOS devices store charges in the discrete traps where a single defect will not discharge the whole memory. The conventional charge trapping materials in traditional SONOS memory, however, are not compatible with dimensional scaling, and lead to poor performance in P/E speed, retention and endurance. [32, 35, 36] Furthermore, to achieve faster P/E speed, the tunneling oxide must be shrunk to enhance the electric field across it while the blocking oxide should be thicker to suppress the leakage current through the

blocking oxide. [37] However, thinner tunneling layer may in turn cause poor stability and reliability; and thicker blocking layer requires larger working voltages. [38, 39]

Up to now, great efforts have been made for good memory characteristics via various approaches to gain a trade-off between the P/E speed and data retention, which are remaining bottlenecks for on-chip memory applications. Various new high-*k* materials have recently been proposed and studied as the charge-trapping layer for good memory characteristics. For example, HfO_2, TiO_2, and ZrO_2, which have good thermo-dynamical stability compatible with Si and high dielectric constant, have been studied to replace the Si_3N_4 layer for faster P/E speed and better retention as compared with the conventional SONOS devices. [40-47] The charge retention and P/E speed can be further improved by employing thicker high-*k* dielectric with larger band gap as the blocking layer material. Al_2O_3 has been proved to be a good blocking oxide candidate to lower the electric field across the blocking oxide. [48, 49] Table 1.2 lists and compares the properties of some high-*k* materials including dielectric constant, band gap, conduction band offset with respect to Si, and crystal structure. [50]

Table 1.2 Comparison of properties among some high-*k* materials

Material	Dielectric Constant	Band gap (eV)	ΔE_C to Si (eV)	Crystal Structure
SiO_2	3.9	8.9	3.2	Amorphous
Si_3N_4	7	5.1	2.4	Amorphous
Al_2O_3	9	8.7	2.8	Amorphous
HfO_2	25	5.7	1.4	Mono., tetrag., cubic
ZrO_2	25	5.5-7.8	1.5	Mono., tetrag., cubic
TiO_2	83-100	3.5	1.2	Tetragonal
Ta_2O_5	26	4.5	1.3	Orthorhombic
Y_2O_3	15	5.6	2.3	Cubic

In addition, new structures of dielectric stacks have also been explored to improve the device speed and reliability. For example, as compared with the conventional SONOS devices in which the charge retention capability degrades with decreasing tunneling oxide thickness, the symmetric (low-*k*/high-*k*/low-*k*) or asymmetric (low-*k*/high-*k*) tunneling layer stack has been proved to show either lower voltage or higher programming speed due to the engineered tunneling barriers with lower barrier height and smaller effective tunneling thickness. [51-54]

Storage of multiple bits on a single memory cell for enhanced integrated memory density has always been a concern with the development of both CMOS scaling and Flash memory scaling. It is also a technical issue that must be dealt with for the applications of novel non-volatile memory for future on-chip memory. However, not all strategies to increase memory density have been fully explored. For example, the number of devices per unit of volume can be increased by using 3D integration which however requires a complicated and high-cost process; [55] multi-bit memory is also proposed with embedded nanocrystal. [56] However, as mentioned above, the control of nanocrystal density and size will be a concern. As for the conventional floating-gate memory, different memory states can be theoretically presented by different amount of stored charges. Further cell scaling or increasing the number of memory levels will be extremely difficult, as the complicated top-down device fabrication and device structure will inevitably lead to significant device variation and a blurring of the multiple storage states. [57]

An effective and perhaps simpler strategy to achieve multi-bit cells is to use multiple charge storage layers in SONOS Flash structure. Unlike the floating-gate memory, multiple charge storage layers in a SONOS device can separate the stored charges by the physically present insulating layers capped between charge-trapping layers. These electrically insulating layers defined the P/E voltages required to achieve different memory states in corresponding charge storage layer. This is a much more reliable and stable approach for realizing multiple levels in one unit memory cell. This thesis investigates the design and characterization of the novel non-volatile memory cells containing Ta_2O_5 as charge trapping medium to achieve discrete multi-bit charge storage with good speed and reliability characteristics. Ta_2O_5 is a robust high-*k* dielectric with good thermal stability, high permittivity and relatively small band gap (4.5 eV) as compared with other commonly used dielectrics such as SiO_2 and Al_2O_3. [58] In addition, Ta_2O_5 has been previously suggested as a non-volatile memory charge storage material. [36] Our results demonstrated that Ta_2O_5 is an excellent charge-trapping medium and that a multiple-layer charge-storage dielectric stack based on Ta_2O_5 is attractive for multi-bit Flash memory applications.

1.2.2 Molecular Flash Memory

CMOS and semiconductor non-volatile memory scaling have generated various approaches toward building memory devices with higher scalability and better performance. The hybrid silicon/molecular approach is attractive as a technology that

leverages advantages afforded by a molecule-based active medium with the vast infrastructure of traditional metal-oxide-semiconductor (MOS) technology. [59-62]

Reduction-oxidation (redox)-active molecules can be attached on various surfaces such as Si and SiO_2 by forming a self-assembled monolayer (SAM) or multiple layers with simple and low-cost processes. [63, 64] Due to the inherent reduction and oxidation of the redox centers, redox-active molecules can exhibit distinct charged and discharged states, and can present logic On and Off states when incorporated in semiconductor memory devices, while enabling the device scaling ability down to the molecular level. Typically, when applying an oxidizing voltage, the molecules will lose electrons, giving a positively charged SAM. On the contrary, a reducing voltage will cause electrons transfer back into molecules, resulting a neutral discharged states.

Incorporating redox-active molecules as charge-storage medium in a Si-based Flash non-volatile memory is thus quite interesting. It has been demonstrated that the redox-active molecules attached on Si structures are stable and can endure more than 10^{12} P/E cycles. [65] This excellent performance is naturally derived from the intrinsic properties of redox molecules, and provides quite promising basis for fast speed, low P/E voltage, and reliable on-chip memory applications. [66-68] In a molecular Flash memory, redox-active molecules embedded in an insulating dielectric are attached on semiconductor or oxide surfaces through the molecule linkers, which also works as the tunnel barrier and can be optimized by variation in structure and connectivity to obtain the desired tunneling probability, redox potential, and retention time.

More importantly, redox molecules with multiple redox centers can enable multi-bit storage at distinct voltages. This strategy to increase memory density is advantageous than conventional memory technologies due to the naturally-derived multiple redox states for robust charge storage and the scalability of molecules for prominent cell dimension.

Memory based on redox-active molecules also enables the "bottom-up" approach to molecular electronics by taking the advantages of self-assembly process. Bottom-up, different from top-down which includes making nano-scale structures by machining and etching techniques, refers to building organic or inorganic structures by atom-by-atom or molecule-by-molecule techniques. The self-assembly process of the redox-active molecules in a molecular Flash memory enables not only high-quality attachment of molecules on semiconductor surfaces, but also uniform and high-density fabrication of low cost devices and circuits.

The disadvantages of molecular Flash memory mainly lie in their reliability at high temperature and volatile environments. Some redox molecules are instable or even not functioning at temperatures higher than 200 ^{o}C due to evaporation or redox center reaction. Under volatile environments with oxygen or water, the molecule's bond might be broken leading to poor redox behavior. As a result, some specific condition and environment need to be taken care of when integrating such redox molecules in CMOS devices and circuits. Further molecular technology development requires advancement in both molecular properties and device integration processes.

Nevertheless, molecular Flash memory with the integration of redox-active molecules into a solid-state structure has still attracted intensive attention lately, due to its

excellent performance and compatibility with the CMOS fabrication process. For instance, devices with metal-molecule-metal structure have been well studied, but this structure is vulnerable to defects and metal penetration. Chen *et al.* reported a study on preventing contact metal penetration into the molecular layer in the metal-insulator-molecule-metal structure. But this structure suffers from a series of gate leakage problems. [69] Shaw *et al.* reported a study on a metal-oxide-semiconductor structure with molecules encapsulated in gate dielectrics. But the device reliability was not well investigated. [70, 71] Up to now, no study has yet been reported of the solid-state molecular Flash memory device P/E endurance at fast speed. This dissertation focuses on developing hybrid molecular Flash memory containing redox molecules as active component for charge storage medium to replace on-chip SRAM and DRAM. We have developed a Si-molecular integration process to preserve the intrinsic redox properties and studied the charge storage properties of the molecular memory. The devices exhibit high P/E speed at low operation voltages and excellent endurance: the devices remain well-functional after 10^9 P/E cycles. Multiple charge storage behavior can be obtained by employing redox-active molecules with discrete redox states, enabling multi-bit storage in a given memory storage location. In this thesis, we have demonstrated that the hybrid integration of redox-active molecules on a semiconductor platform is very attractive for high-performance non-volatile memory applications.

1.2.3 Si Nanowire Field-effect Transistor Based Flash Memory

In addition to the physical and economic improvement, to break through the conventional microelectronics technology scaling limits is also very important for the development of future Si-based non-volatile memory devices. During the past decades, semiconductor nanowire and nanotube synthesized by bottom-up techniques and derivative field-effect transistor (FET) devices have been intensively studied as fundamental building blocks for nanoelectronic devices and circuit technologies. [72-75] Si nanowire FETs (SiNW FETs) with single or multiple nanowire channels are very attractive as they have better performance than planer bulk Si, such as high surface-to-volume ratio and lower power consumption. Employing SiNW as FET channel can enable gate-surrounding structure, allowing excellent electrostatic gate control over the channel for reducing the short-channel effects. The following equations define the minimum gate length to avoid short-channel effects for single-gate, double-gate and surrounding-gate structures:

$$\lambda_{single-gate} = \sqrt{\frac{\varepsilon_{Si} t_{ox} t_{Si}}{\varepsilon_{ox}}}$$

$$\lambda_{double-gate} = \sqrt{\frac{\varepsilon_{Si} t_{ox} t_{Si}}{2\varepsilon_{ox}}}$$

$$\lambda_{surrounding-gate} = \sqrt{\frac{2\varepsilon_{Si} {t_{Si}}^2 ln\left(1 + \frac{2t_{ox}}{t_{Si}}\right) + \varepsilon_{ox} {t_{Si}}^2}{16\varepsilon_{ox}}}$$

where t_{Si} , ε_{Si} , t_{ox} , ε_{ox} are thickness and permittivity of silicon and gate oxide, respectively. [76] The equations demonstrate that the surrounding-gate structure offers the best characteristics for controlling the short-channel effects.

Employing SiNW as an alternative for the bulk Si in novel non-volatile memory promises advanced device performance and provides new solutions toward the design and optimization for future memory technology. Due to the cylindrical symmetry of the NW channel, Flash memory scaling can be achieved easier by scaling the channel from planar bulk Si to nano-scale SiNW. This type of scaling strategy with least requirement of gate dielectric shrinking, especially the tunneling oxide thickness, will retain the memory performance such as the data retention. On the other hand, the electric field introduced by the control gate across the tunneling oxide surrounding a SiNW channel is much larger than that of conventional planar memory cell. This will lead to faster P/E operations at lower P/E voltages.

In a Flash memory based on semiconductor NW FET, multi-bit storage at discrete levels can be carried out because of the high sensitivity of the NW FET conductance to the charges in the surrounding environment. This dissertation investigates the design and fabrication of high-performance SiNW FETs prepared by using a self-alignment technique, and its applications toward the Flash non-volatile memory. By integrating the high-*k* dielectric and redox-active molecule gate stacks on SiNW FETs, we have studied the Flash-like non-volatile memory devices and have achieved significant memory performance improvement as compared with capacitor structure counterparts. We demonstrate that the integration of novel charge-trapping mediums in a solid-state SiNW FET will generate high-performance Flash memory which will enable a vast opportunity for on-chip and local memory applications.

1.3 Topological Insulators

Throughout most of the 20th century, fundamental science has never stopped searching for elementary particle. In condensed matter physics, instead of dealing with the atoms and electrons that were found centuries ago, there is growing interest in how these fundamental elements are put together to form a new state of matter (*e.g.* insulators, conductors, semiconductors, superconductors, and magnets). In 1980, Klitzing *et al.* discovered the quantum Hall (QH) state, which describes the insulating bulk of a two-dimensional (2D) sample while the electric current flows along the 2D sample edges. [77] The QH state, the simplest topologically ordered state, is the first example of a quantum state which is topologically different from all known states of matter.

Recent research has discovered a new electronic phase – topological insulator. This type of state of matter has insulating bulk inside and conducting surface outside. [78-81] More interestingly, the conducting spin-up and spin-down electrons are travelling in opposite directions when strong magnetic field is present, resulting in the spin current which may be attractive to modern spintronics.

Different from superconductors and magnets which have an "order" associated with broken symmetry, topological insulator exhibits a topological order which is invariant by symmetry under the reversal of the direction of time, similar to the QH state. However, unlike the QH state which requires the presence of a strong magnetic field, topological insulators can be observed without magnetic field. Instead, the spin-orbit coupling plays an important role, which is the interaction of electron's intrinsic spin with the orbital motion. For heavy elements such as Hg and Bi, spin-orbit coupling is strong

and plays the role of a magnetic field as in the QH state when electrons are travelling through the topological insulator materials. The quantum spin Hall (QSH) state was proposed upon the above basis in 2D topological insulators, whereas the spin-up and spin-down electrons propagate at the edges along in opposite direction, and therefore cancel each other, resulting in a zero Hall conductance. [78, 82-84] These QSH edge states are protected from backscattering and the protection arises from the time-reversal symmetry.

Theoretical concepts developed from 2D topological insulators soon gave birth to the 3D topological insulators. [85, 86] Resembling the edge states of the 2D topological insulator, the surface states of 3D topological insulator where the electron propagates are protected by time-reversal symmetry from backscattering. [87, 88] The topologically non-trivial state has an insulating gap in the bulk, but conducting surface states consisting of an odd number of Dirac fermions. The dispersion forms a so-called Dirac cone, whose crossing point is located at a time-reversal-invariant point, and the degeneracy is protected by the time-reversal symmetry.

Both the 2D and 3D topological insulators were predicted theoretically prior to experimental discovery. In 2006, less than one year after the theoretical prediction, the 2D topological insulator exhibiting QSH effect was experimentally observed in HgTe quantum wells. [78, 82] The two edges of the QSH insulator work as two conducting channels, with each contributing one quantum of conductance e^2/h, independent of the width of the sample. The 3D topological insulator was predicted in Bi_xSb_{1-x} alloy with different composition in 2007. [89] Shortly, an odd number of topologically non-trivial

surface states have been mapped with angle-resolved photoemission spectroscopy (ARPES). [90, 91] Even though the observed surface structure was found to be quite complicated, this research initiated the search for other topological insulators and experimental work on these materials.

1.3.1 Topological Insulator Materials

Soon after the ARPES mapping on Bi_xSb_{1-x} compounds, simpler structure binary chalcogenide compounds Bi_2Se_3, Bi_2Te_3, and Sb_2Te_3 were predicted as 3D topological insulators. [92, 93] All of them share a rhombohedral quintuple layer structure, with five atomic layers in one unit cell, as shown in Fig. 1.4. These quintuple layers are linked by van der Waals interactions. [94]

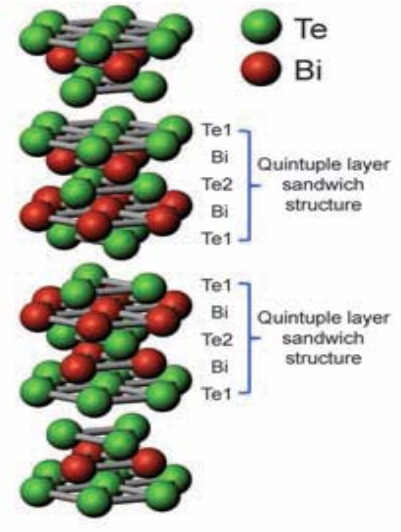

Fig. 1.4 Tetradymite-type crystal structure of the topological insulator Bi_2Te_3 [95]

Traditionally, topological insulators such as Bi_2Se_3 and Bi_2Te_3 are well known as thermoelectric materials due to their high figure-of-merit coefficient among bulk thermoelectric materials. In the first stage of experiments on topological insulators, thin films of Bi_2Se_3 and Bi_2Te_3 were typically fabricated by molecular beam epitaxy (MBE). Nominally stoichiometric single crystalline films by this method could easily be prepared. More significantly, these thin films are deposited with a growth unit of 1 quintuple layer (QL). Upon ARPES and scanning tunneling microscopy (STM) measurements, as-grown thin film Bi_2Se_3 and Bi_2Te_3 materials without any doping were found to be an intrinsic topological insulator with its Fermi level intersecting only the metallic surface states, which is quite different from the bulk material. [95-100] It has been demonstrated by both experimentally ARPES mapping and theoretically first-principle calculation that topological features of MBE grown thin films start to appear from the sample with 2 QL thickness. [101] This is because for the 1 QL film, the coupling between top and bottom surface is strong enough to open up a whole insulating gap at the surface. Starting from the 2 QL film, the inter-surface coupling becomes significantly weaker, and the topological features will appear. These several-QLs thin film might not be a good candidate to define the concept of a 3D topological insulator, but is good for 2D characterizations similar to the HgTe quantum well. [101]

Referring the above method, 3D topological insulators have been explored extensively by studying nano-scale topological insulator structure down to the thickness limit when retaining its 3D topological insulator character and stoichiometry, as the experimental realization of predictions and applications about 3D topological insulator

has been hampered by the large conduction contribution from the bulk in small band-gap semiconductors. In recent years, 3D topological insulators have been investigated independently. It has been demonstrated that due to a large surface-to-volume ratio, ultra-thin nanostructure Bi_2Se_3 samples can significantly enhance the surface conduction. Particularly, the surface states of Bi_2Se_3 form the single Dirac cone inside a relatively larger bulk band gap of 0.35 eV as compared with other potential 3D topological insulators, thus Bi_2Se_3 has been suggested as the reference material for 3D topological insulators.

1.3.2 Topological Insulator Devices

The significance of topological insulators has been more and more recognized in different areas and applications. [102-112] Especially, the nanostructures of topological insulators have provided stimulating platforms for creative and innovative research ideas and applications on 3D topological insulators, such as spintronics. [113-116] For example, a topological insulator and a ferromagnet heterostructure can enable switching of the ferromagnet by passing a current through the topological insulator's surfaces. [102] This strategy has been proposed as a new form of spin torque device for future magnetic memory applications.

Another appealing application to physicists would be the potential of topological insulators to realize the elusive Majorana fermions, which has half-integer spin, but has antiparticles identical to itself. [103] It is predicted to arise from a combination of a topological insulator and a superconductor, and the key step to seek the Majorana

fermions is the unequivocal observation of supercurrent in a topological phase. [103-106] There has been demonstration of direct evidence for Josephson supercurrents in superconductor-topological insulator-superconductor junctions. [107] The realization of supercurrents through topological surface states would be a significant step toward the detection of Majorana fermions.

So far, MBE grown topological insulators and related inspection instruments such as *in-situ* STM and *in-situ* ARPES have been proved to be of great value in characterizing the surface states. Due to the high surface-to-volume ratio, MBE grown high-quality crystalline topological insulator thin films are good approaches to manifest the gapless surface states featuring the helical Dirac electrons. However, these techniques did not provide an electrically accessible device platform, such as field-effect transistors, for investigations on topological insulators via characterizations with electrical, magnetic, or optical signals.

Later on, mechanical exfoliation approach similar to that on Graphene, has been introduced to fabricate simple topological insulator device at low cost. [108-111] Significant progress has been achieved to show the first stage of understanding and applications of topological insulators. For example, it has been demonstrated recently by magnetotransport experiments on exfoliated Bi_2Te_3 bulk materials which suggest that 2D conduction channels originate from the surface states. [112] An insulating behavior and a close to bulk band gap energy barrier were also observed in a FET based on exfoliated Bi_2Se_3 films, due to the top and bottom surface states coupling. [109] In addition to the electrical and magnetic study, the optical effect on topological insulators has also been

conducted on exfoliated topological insulator films. Mclver *et al.* have experimentally studied the spin of the electrons on the surface states that is perpendicular to the direction of motion to access and control them by using circularly polarized light on exfoliated Bi_2Se_3 thin film. [110] Studying the surface states and the spin of electrons can effectively avoid any significant conduction contribution from the bulk, demonstrating the helicity of the surface states, as only the electrons with particular spin orientation will be selectively excited by circularly polarized laser light. [113]

However, despite the findings about composition doping, simple electrical gating, and nanostructure devices, the challenge for modulating the surface states of mechanically exfoliated topological insulators is to minimize the bulk conduction contribution, which basically arises from defects such as Se vacancies or anti-site defects. Moreover, like the Scotch-taped Graphene device, exfoliated topological insulator device also suffers from low yield and poor control over the film uniformity and sample size and morphology.

Great efforts have been made to synthesize novel nanostructure topological insulators such as high-quality single crystal nanowires, nanoribbons, nanoplates, and nanobelts, which can enable more delicate devices to access and manipulate the surface states by external means, while maintaining high surface-to-volume ratio. [114-116] Experimental evidence of manipulating surface states of a Bi_2Te_3 nanoribbon by electrical gating to control the quantum oscillations has been reported recently. [117] Enhanced surface conduction taking up more than half of the total conduction has been achieved by gate voltage. Transport measurements carried out on topological insulator

nanoribbons demonstrating coherent propagation of 2D electrons around the circumference of the nanoribbon surface by prominent Aharonov-Bohm oscillations in magnetoresistance, provide profound evidence to separate the conduction of surface states from bulk conduction. [118] The observations of $h/2e$ oscillations indicate the robustness of the states and further confirm the presence of time-reversed perimeter paths with the same relative zero phase at the interference point. Such innovative researches on topological insulator nanostructures are more close to real device applications.

Although the bulk conduction can be reduced by techniques such as substitutional doping and electrical gating in topological insulator nanostructures, these materials might still be sensitive to the environment. It has been found that topological insulator materials usually become heavily doped when exposed to air. More refined and CMOS compatible technique with the topological insulator surface states being protected by insulating materials needs to be developed and studied. In this thesis, we propose, fabricate and characterize surrounding-gate Bi_2Se_3 nanowire FETs with high-quality single crystal Bi_2Se_3 nanowire embedded in HfO_2 high-k dielectric. Their current-voltage characteristics are superior to many of those reported for semiconductor nanowire transistors, including sharp turn-on, nearly zero cutoff current, very large On/Off current ratio, and well-saturated output current. The metallic electron transport at the surface with good FET effective mobility can be effectively separated from the conduction of bulk Bi_2Se_3 and adjusted by field effect at a small gate voltage. The integration of topological insulator as the active conduction channel in MOSFETs is very attractive because it will

leverage the advantages afforded by the novel topological insulator materials with the vast infrastructure of current semiconductor technology.

1.4 Overview of Dissertation

This dissertation addresses the issues of gate stack engineering on Flash non-volatile memory for high-performance on-chip memory applications. New approaches toward the next-generation non-volatile memory technology have been proposed and investigated. This dissertation also proposes and characterizes the electron transport at the surface states on high-performance topological insulator nanowire FETs. The magnetotransport properties lead to new understanding about the quantum phenomena in these materials.

Following the introduction chapter, Chapter 2 introduces the novel dielectric and molecular non-volatile memory structure, and fabrication methodologies with different gate stack. The fabrication of self-aligned SiNW FETs for Flash memory application will also be presented. Chapter 3 explores the electrical characterizations of dielectric charge-trapping memory and the Flash memory based on the application of the dielectric stack on SiNW FET. Chapter 4 presents the molecular charge-trapping memory with redox molecules as charge storage medium. The gate stack including the redox molecules has also been applied on SiNW FETs for fast speed and high endurance Flash memory. Chapter 5 describes the details of building a high-performance topological insulator FET based on the self-aligned NW FET architecture. The surface conduction separation at

small gate voltage and magnetotransport study will be demonstrated. Finally, a summary of the dissertation and a discussion for future research will be presented in Chapter 6.

Chapter 2 Flash Memory Fabrication and Characterization Techniques

2.1 Introduction

We focused on the gate stack engineering with novel high-*k* dielectric materials and redox-active molecules for realizing fast speed Flash memory with excellent reliability and multi-bit storage. In the first step, we developed planar capacitor structure memory cells which can enable straightforward insight into the charging, discharging, and other memory characteristics of the dielectric and molecular stacks. Then, upon developing high-performance Si nanowire field-effect transistor (SiNW FET) as a platform to integrate the stacks as gate stack, we can study the real dielectric- and molecular-based Flash memory with a nano-scale channel. Integration of the dielectric and molecular charge storage medium in the MOSFET technique allows the using of current semiconductor electronics characterization metrologies.

2.2 Fabrication of Charge-Trapping Non-Volatile Memory

2.2.1 Dielectric Charge-Trapping Memory

Planar capacitor structure dielectric charge-trapping memory cells were fabricated by using standard photolithography and deposition procedures. Dielectric stacks including the tunneling oxide, charge trapping materials, and blocking oxide with

different high-*k* materials and engineered combinations were fabricated and compared. The process steps are listed below:

1) A 110 nm SiO_2 field-oxide was grown on low-doped p-type Si substrates (Boron doped, about 10^{15} cm^{-3}) by dry oxidation.

2) Arrays of squares with different active area ranging from 20 to 10^4 μm^2 were defined on the wafer by photolithography (Suss MA-6 aligner).

3) Buffered oxide etch (BOE) and 2% hydrofluoric (HF) acid were used to remove the oxide defined by the squares to form the arrays of active areas in the 110 nm thermal SiO_2.

4) The tunneling oxide (typically SiO_2) was obtained through rapid thermal oxidation (RTO) for various times under varying thermal conditions to obtain different oxide thickness.

5) The charge-trapping layers were then deposited by methods varying with the materials. High-*k* dielectrics Ta_2O_5 and ZrO_2 were deposited by RF sputtering with ambient Ar at room temperature under a pressure of 4×10^{-4} Pa, while the Al_2O_3 and HfO_2 dielectrics were deposited by atomic layer deposition (ALD) at 300 ^oC with trimethylaluminium (TMA) and tetrakisethylmethylaminohafnium (TEMAH) as the precursors, respectively.

6) Al_2O_3 was selected as the material for blocking layer in all memory cells, and was deposited by ALD with the same parameters as above.

7) Photolithography was employed to define the gate electrode. Pd was then deposited by using E-beam evaporation in 4×10^{-4} Pa on the blocking layer followed by the lift-off process.

8) Finally, the devices were annealed in Ar at 250 ^{o}C for 10 minutes to improve the Pd contact.

The active area, tunneling oxide, blocking oxide, and the top gate were fabricated at the same time for all of our dielectric charge-trapping memory samples, in order to obtain a uniform cell size, film thickness, quality, and surface conditions.

2.2.2 Molecular Charge-Trapping Memory

The attachment of redox-active molecules on active surfaces was carried out by forming the self-assembled monolayers (SAMs) on Si-based structures. The SAMs attach on active surfaces via a covalent bond to the atoms on the surface, which enables selective attachment on specific surfaces by using specific tether groups. Our project focused on the attachment of molecules with different amount of redox centers for single-bit and multi-bit memory applications. The molecule attachment was characterized by using techniques including cyclic voltammetry (CyV) and X-ray photoelectron spectroscopy (XPS), prior to the fabrication of a memory cell. The processing procedures are as follows:

1) A 110 nm SiO_2 was grown on low-doped p-type Si substrates, followed by defining active areas through photolithography and wet etching, similar to the beginning steps for dielectric charge-trapping memory cells.

2) A layer of SiO_2 (thinner than 3 nm) was grown by RTO as the tunneling layer.

3) Some of the samples from the previous step were prepared for the characterization of molecule attachment on SiO_2 surface, while the samples for attachment on Si surface were prepared by using 2% HF to etch the tunneling oxide on the active areas. The samples were kept in an inert atmosphere once the Si and SiO_2 surfaces were prepared for attachment.

4) The solutions containing the redox molecules were prepared by dissolving the molecules in proper solvent. Dichloromethane (DCM) was used to dissolve redox molecules to be attached in our work.

5) The self-assembling process of the molecules on active areas were then carried out by immersing the wafer into the molecular solution or by placing droplets of the molecular solution on the active areas with each drop being placed for 5 min. A saturated SAM was formed by immersing the wafer for 20-30 min in the molecular solution or by placing 8 droplets of the solution on active areas. The attachment was performed in a glovebox with inert environment under either Ar or N_2. The temperature of the attachment on Si structures of molecules dissolved in DCM was maintained at 90 ^{o}C to 100 ^{o}C. The attachment conditions were the same for both attachments on Si and SiO_2 surfaces.

6) After the SAM was formed, DCM was used to rinse the attached sample to remove any physisorbed residuals on the surface for two to three cycles of sonication with 1 min each.

7) The attached samples were then separated into two groups: one group for attachment characterizations through CyV; the other group for molecular memory cell fabrications. The samples prepared for memory devices were immediately loaded into the ALD vacuum chamber after the DCM rinsing to deposit the blocking layer Al_2O_3. Due to the uncertainty of the stability of redox molecules at high temperature, the ALD deposition temperature was set to 100 ^oC, with TMA and H_2O as precursors.

8) In the final step, Pd was deposited and patterned on Al_2O_3 as the top gate by photolithography and E-beam evaporation, followed by the lift-off.

The samples for XPS measurements were prepared by formation of SAM on highly doped p-type Si wafers without patterned structures, by using the same attaching methods described above.

The essential steps in the molecular memory fabrication process are the formation of SAM on active surfaces and the deposition of Al_2O_3 encapsulating the molecules. The SAM formation was examined by the CyV and XPS measurements. In order to ascertain whether the molecular SAM survives the ALD process, some test samples with a thin layer of ALD Al_2O_3 covering the SAM were also measured by XPS, and the results demonstrated that the SAM successfully survived in the ALD process, thus it proves that Al_2O_3 can be deposited on SAMs with hydrophilic end groups by using TMA and H_2O vapor as precursors at relatively low temperature.

2.3 Flash Memory Based on Self-Aligned SiNW FET

Semiconductor nanowire and nanotube FETs have been intensively studied as fundamental building blocks for nanoelectronic device and circuit technologies. Incorporating SiNW as the conducting channel in the modern Flash memory can be expected to outperform conventional planar silicon Flash memory, due to better scalability, lower power consumption, and better electrostatic gate control over the channel by enabling the gate-all-around structure. To date, devices used to study nanowire FETs and their applications have mainly been fabricated by using top-down approaches based on advanced lithography with multiple nanowires prepared by dry/wet etching. [119, 120] It has been well recognized that synthesizing nanowires by bottom-up techniques such as chemical vapor deposition (CVD) can have lower cost and higher quality compared to the top-down methods. [121, 122] It would be very attractive to develop an approach to manufacture such self-assembled nanowire FETs with excellent performance. However, the technique to fabricate FETs from CVD grown SiNWs remains a barrier to the development of devices with optimized performance. Current approaches are primarily based on harvesting and positioning the as-grown semiconductor nanowires by using aligning methods such as fluidic alignment, dielectrophoresis, or nano-scale probe methods. [123-128] These methods may introduce contaminants surrounding the surface of the nanowires. This contamination will adversely influence the device interface state density (D_{it}) and possibly the nanowire surface roughness, which will significantly degrade the final device performance.

In our work, we designed and fabricated self-aligned SiNW FETs with excellent current-voltage (*I*-*V*) characteristics, high On/Off ratio and small subthreshold slopes (*S*), providing an excellent platform for novel Flash non-volatile memory applications.

2.3.1 Self-Alignment Fabrication

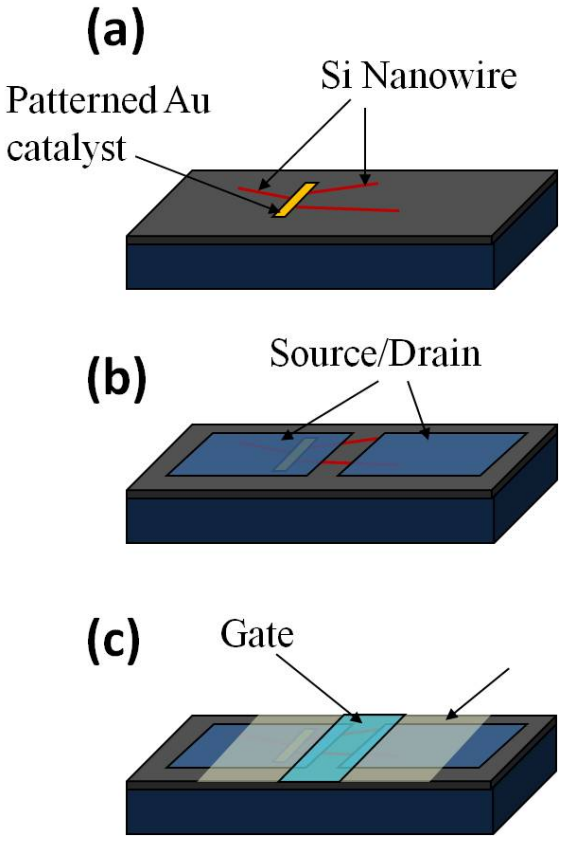

Fig. 2.1 Self-alignment fabrication process for SiNW FETs: (a) patterned Au on SiO_2 and synthesis of SiNW from the Au catalyst; (b) SiNW oxidation and formation of source/drain contacts; (c) deposition of gate dielectric and pattern of top gate.

SiNW FETs were fabricated by using a directed "self-alignment" process shown in Fig. 2.1. [129] The main concept of this fabrication approach is that silicon nanowires

are grown from Au catalysts on predefined locations on wafers and aligned with the source/drain and gate electrodes by photolithographic processes without harvesting the nanowires. This approach enables simultaneous batch fabrication of large numbers of nanowire devices, while effectively reducing the processing steps in which nanowire surfaces might be contaminated.

As the first step of the fabrication process, a layer of SiO_2 (300 nm) was thermally grown on a silicon wafer as the insulator of the bottom gate by using dry oxidation. Then a thin film of Au catalyst (~ 1 nm) was deposited on the SiO_2 and patterned by photo-lithography and lift-off processes. The Si nanowires were grown from the catalyst at the defined locations in a low-pressure chemical vapor deposition (LPCVD) furnace at 440 ^oC for 2 hours with an ambient SiH_4 stream under a pressure of 500 mTorr (Fig. 2.1(a)). The nanowire growth followed the vapor-liquid-solid (VLS) mechanism. [121, 127, 130] The Si nanowires were typically 20 μm in length and 20 nm in diameter. Immediately after the growth step, the Si nanowires were oxidized at 750 ^oC for 30 min in O_2 to form a ≈ 3 nm thick SiO_2 which was expected to provide a good interface between the Si nanowire and the gate dielectric stack that is completed after the formation of source/drain contacts. [131] The following fabrication processes were used to pattern the metal contacts (*i.e.* source, drain and top gate electrodes) on the Si nanowires. First a lift-off resist / photoresist bilayer was spun on the wafer (with nanowires) and the patterns for the source and drain contacts for the Si nanowire FET were defined with photolithography (Fig. 2.1(b)). To facilitate proper contact formation, a 2% HF wet etch was applied to remove the oxide from the Si nanowires immediately before Al was

deposited by thermal evaporation and lifted-off to form the source and drain electrodes. The next step is to deposit top gate dielectric (a layer of 25 nm HfO_2 in our FETs) by ALD at 250 ^oC, followed by a deposition of 5 nm of Al_2O_3 to improve the interface with the subsequently deposited Al gate. The top Al gate was formed by the same lift-off process as the source/drain electrodes (Fig. 2.1(c)). The completed devices were annealed in forming gas (5% H_2 in N_2) at 325 ^oC for 5 min. This final annealing step was found to be of significant importance because it will reduce the D_{it} between the Si nanowires and dielectric layers, as well as improve contact between the Al metal to the Si nanowire and HfO_2. [45, 130] With this fabrication method, about 90% of the pre-defined locations successfully formed the expected Si nanowire devices with single or multiple nanowires.

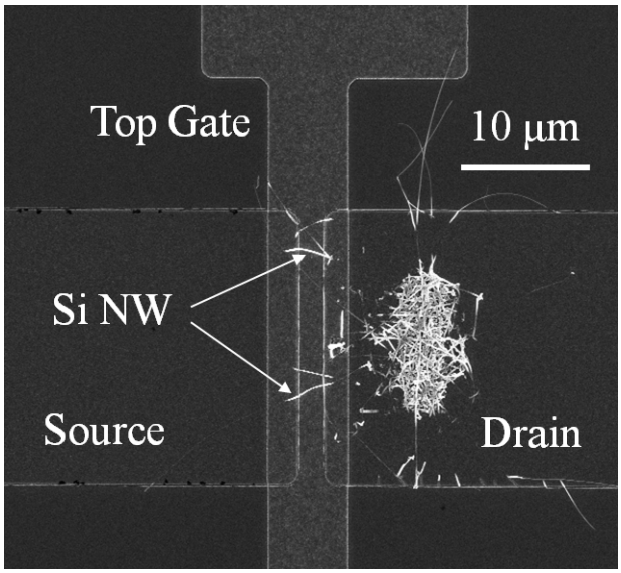

Fig. 2.2 SEM image of a typical self-aligned SiNW FET with gate length of 2 μm

The self-alignment fabrication process used in this work is promising compared to regular nanowire harvesting and manipulation processes. It not only enables simultaneous batch fabrication of high quality, reproducible and homogeneous nanowire devices at the wafer scale, but also limits the fabrication steps in which the nanowires can be contaminated. Fig. 2.2 shows the scanning electron microscopy (SEM) image of a typical SiNW FET with 2-μm gate length.

2.3.2 Electrical Characterizations of Self-Aligned SiNW FETs

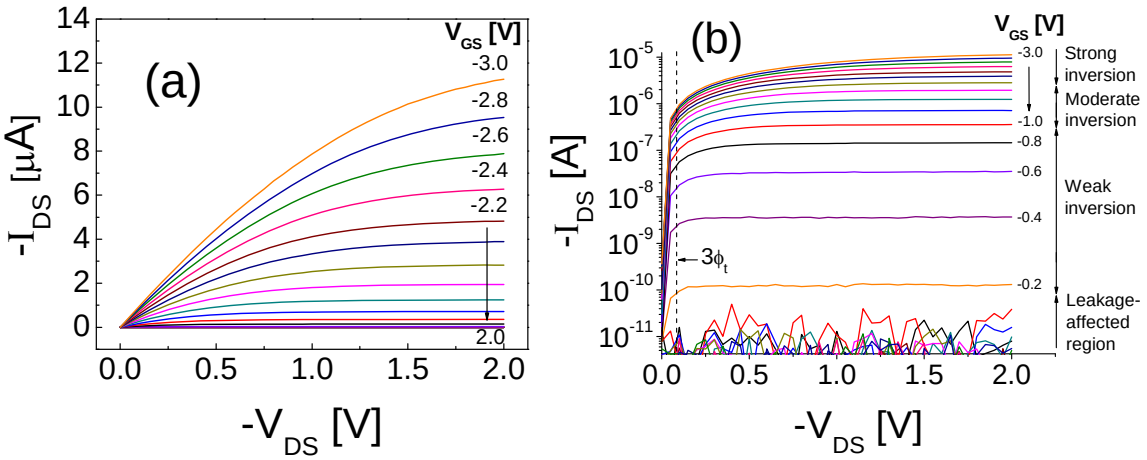

Fig. 2.3 (a) Output characteristics of self-aligned SiNW FET in linear scale, with V_{GS} varies from 2 V to -3 V, with step of -0.2 V; (b) Log-scale output characteristics with clearly shown strong, moderate, weak inversion, and leakage-affected regions, which is similar to that of an ideal conventional MOSFET.

Fig. 2.3(a) and 2.3(b) show the output characteristics (I_{DS}-V_{DS}, where I_{DS} and V_{DS} are the current and voltage between the drain and the source) of a self-aligned SiNW FET in both the linear and logarithmic scale. The leakage-affected region, weak, moderate,

and strong inversion operation regions of the nanowire FET are clearly shown in Fig. 2.3(b). In the weak inversion region, I_{DS} increases exponentially with V_{GS} due to the diffusion of carriers (holes), and is saturated at $3\phi_t$ (~ 78 mV at room temperature, $\phi_t = kT/q$ is the thermal voltage). In moderate inversion region, I_{DS} is neither exponential nor polynomial, but its behavior changes gradually from one form of functional dependence to the other. Within the moderate region, the current varies by a couple of orders of magnitude. In strong inversion region, I_{DS} approximately follows the quadratic law ($I_{DS} \sim (V_{GS} - V_{TH})^2$), and is saturated at $V_{DS} = V_{GS} - V_{TH}$. These curves demonstrate that the self-aligned SiNW FET has similar behaviors of conventional MOSFETs, even though it has much simpler device structure and no source/drain junction doping. It should also be noted that, the I_{DS}-V_{DS} curves increase sharply in the linear region, indicating a small source and drain contact resistance.

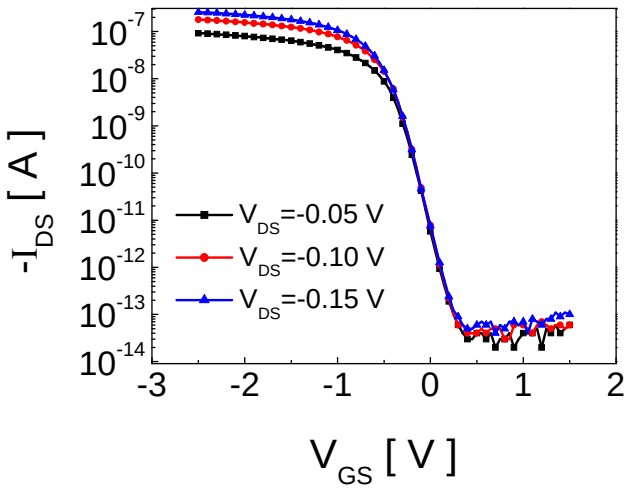

Fig. 2.4 Transfer characteristics of the SiNW FET, with V_{DS} value of -50 mV, -100 mV, and -150 mV, respectively.

Typical transfer characteristics of self-aligned SiNW FETs are shown in Figs. 2.4, for V_{DS} values of -50 mV, -100 mV and -150 mV, respectively. Due to the Schottky contacts between the Al contacts and the intrinsic SiNW, Schottky-barrier pMOSFET characteristics are expected for these SiNW FETs. No ambipolar behavior was observed; the FETs stay in the Off state when V_{GS} is higher than a specific threshold value. The On/Off current ratio is on the level of 10^8 for a 1.2 V V_{GS} window. The subthreshold swing (S) can be extracted from the subthreshold region of I_{DS} in the log-scale I_{DS}-V_{GS} curves. The S values of the SiNW FETs are as low as 75 mV/dec, which is small compared to many recent results on nanowire FETs and poly-Si thin-film transistors (110-200 mV/dec). [72, 132, 133]

So, prototypical SiNW FETs have been fabricated through a self-alignment approach, exhibiting excellent performance as indicated by a high On/Off current ratio (~ 10^8), small subthreshold slope (as low as 75 mV/dec) and small leakage current (< 10^{-14} A). These excellent characteristics are due to the clean interfaces formed in the self-alignment fabrication process and the presence of Schottky barriers between the source/drain and SiNW channel. Such self-aligned SiNW FETs are very attractive for future nanoelectronic device and circuit applications.

2.3.3 Application of Charge-Trapping Gate Stacks on SiNW FETs for Flash Memory

Integrating the charge-trapping stacks on the high-performance self-aligned SiNW FETs enables the study on real Flash memory which can be expected to have better

memory performance than the planar memory devices, making them quite attractive for future memory technology toward on-chip memory applications.

The dielectric stacks and top gate materials on SiNW FETs were deposited by using the same methods as capacitor structure memory cells, except the tunneling oxide which utilizes the ~ 3 nm SiO_2 surround the nanowire in the SiNW FETs. Similarly, redox-active molecules were also attached on this tunneling layer as charge storage medium in molecular Flash memory after forming the source/drain electrodes, followed by the same fabrication and deposition processes as the capacitor counterparts. Ti/Pt with a typical thickness of 3 nm / 100 nm was deposited as the source/drain electrodes on both dielectric and molecular Flash memory forming the Schottky barrier contacts.

2.4 Characterization Techniques

Upon the formation of SAM on Si and SiO_2 active areas in the planar capacitor structures, CyV measurements were carried out to characterize the attachment quality and surface coverage of the molecules. Fig. 2.5 shows the schematic diagram of the electrolyte-molecule-SiO_2-Si (EMOS) setup for CyV measurements, in which a solution of 1.0-M tetrabutylammonium hexafluorophosphate (TBAH) in propylene carbonate (PC) was used as the conducting gate electrolyte. Backside contact to the samples was made via the chuck of the probe station. The ~ 5 μL electrolyte was then moved by the motion of the silver counter electrode on the top of active areas. The surface tension of the electrode tip and the highly viscous electrolyte allow a small amount of electrolyte

covering the active area. The CyV current-voltage characteristics at various voltage scan rates were then measured by using a CHI600 electrochemical analyzer.

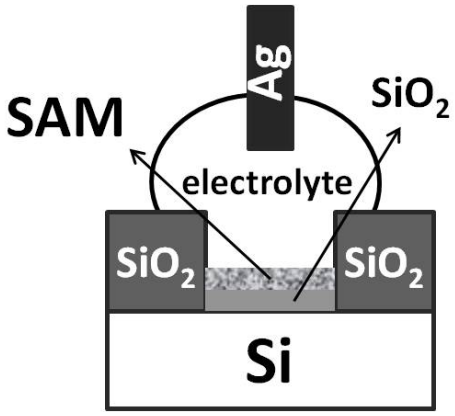

Fig. 2.5 Schematic of electrolyte-molecule-SiO_2-Si (EMOS) structure for CyV measurements

The memory performance of the planar dielectric and molecular memory devices was investigated by studying the flat-band voltage shift under different program/erase (P/E) conditions. An Agilent E4980A LCR meter was employed to perform the capacitance-voltage (C-V) measurements on the capacitor structure memory devices. The gate current-voltage characteristics were measured using an Agilent 4156C semiconductor parameter analyzer, which also performed the I-V measurements on the Flash memory based on SiNW FETs. An Agilent 33120A waveform generator was used to provide voltage pulses for the programming and erasing operations.

Chapter 3 Dielectric Charge-Trapping Non-Volatile Memory

3.1 Introduction

The conventional polysilicon floating-gate Flash memory has benefited the semiconductor memory technology for decades, due to their scalability, compatibility with CMOS process, and so forth. However, the extremely fast developing semiconductor technology recently has created huge demands for novel non-volatile memory with smaller cell size, higher storage density, lower power consumption, and better retention and endurance. Due to the ultra-thin tunneling oxide, the stress-induced leakage current (SILC) has failed the further applications of floating-gate Flash memory in sub-100 nm technologies. In recent decades, the polysilicon-oxide-nitride-oxide-silicon (SONOS) type charge-trapping non-volatile memory has attracted more and more attention, and has been regarded as a very promising candidate to overcome the challenges of high density and high speed memory development, and to gain a breakthrough in modern electronics of accessibility of an on-chip memory, such as static random-access memory (SRAM) and dynamic random-access memory (DRAM). [134-136]

However, the traditional SONOS charge-trapping memory still suffers drawbacks such as poor program/erase (P/E) speed, retention and endurance resulted from the nitride layer and the thin tunneling layer. [137, 138] To achieve faster P/E speed, the tunneling

oxide must be shrunk to enhance the electric field across it while the blocking oxide should be thicker to suppress the leakage current through the blocking layer. But thinner tunneling oxide may cause poor stability and reliability; and thicker blocking oxide requires larger operation voltages. Recently, different high-*k* materials and stacks have been studied to be implemented in novel SONOS-like memory structure. For example, HfO_2, Y_2O_3, Gd_2O_3, and ZrO_2 have been applied as charge-trapping layer to replace the Si_3N_4 for better retention and faster speed. [44, 139-141] In addition, the memory retention and speed can be further enhanced by employing thicker high-*k* dielectric with relatively larger band gap as the blocking oxide to lower the electric field across the blocking layer. [37] To explore new strategies to increase charge storage density is another important issue. A simple and feasible approach on SONOS-like charge-trapping memory is to use multiple charge-trapping layers to achieve multi-bit storage in one unit cell.

This chapter demonstrates our work on dielectric stack engineering for non-volatile memory applications. A multiple Ta_2O_5 charge-trapping layer stack provides discrete multi-bit charge storage with good P/E characteristics. Si nanowire field-effect transistor (SiNW FET) based Flash memory with such novel dielectric gate stacks shows fast P/E speed, good retention and endurance, and multi-bit charge storage at lower operation voltages.

3.2 Ta_2O_5 Stacks toward Discrete Multi-Bit Memory Application

Ta_2O_5 is a robust high-*k* dielectric with good thermal stability, high permittivity and relatively small band gap (4.5 eV) as compared with other commonly used dielectrics such as SiO_2 and Al_2O_3. The major focus of our work is on the application of multi-layer of Ta_2O_5 for multi-bit storage application. Our results demonstrate that Ta_2O_5 is an excellent charge-trapping medium and that a multiple charge-storage layer dielectric stack based on Ta_2O_5 is attractive for multi-bit memory applications.

3.2.1 Experimental Details

Fig. 3.1(a) - (d) show the four capacitor structures fabricated and studied in our work: Metal/Al_2O_3/Ta_2O_5/Al_2O_3/Ta_2O_5/SiO_2/Si (MATATOS), Metal/Al_2O_3/Ta_2O_5/SiO_2/Si (MATOS), Metal/Al_2O_3/HfO_2/SiO_2/Si (MAHOS) and Metal/Al_2O_3/ZrO_2/SiO_2/Si (MAZOS). Capacitors with the charge-trapping dielectric stacks were fabricated on low-doped p-type Si substrates. First, a 110 nm SiO_2 field-oxide was grown on the Si substrate by dry oxidation. Then, arrays of squares with 100 μm×100 μm active area were defined by photolithography. The oxide in the squares was removed by hydrofluoric (HF) acid etching, followed by the growth of ≈ 3 nm thermal SiO_2 as the tunneling oxide using rapid thermal oxidation at 850 ^oC for 5 min. Ta_2O_5 and ZrO_2 layers were deposited by sputtering at room temperature, while the Al_2O_3 and HfO_2 layers were deposited by atomic layer deposition (ALD) at 300 ^oC with trimethylaluminium (TMA) and tetrakisethylmethylaminohafnium (TEMAH) as the precursors, respectively. A layer of 100 nm Pd was then deposited by using E-beam evaporation and defined on the Al_2O_3 as the gate electrode. Finally, the devices were

annealed in Ar at 250 °C for 10 minutes. The nominal thickness of the Ta_2O_5, HfO_2, and ZrO_2 charge-trapping layers was selected as 20 nm in the MATOS, MAHOS and MAZOS structures, respectively. For the MATATOS structure, the nominal thickness of the $Ta_2O_5/Al_2O_3/Ta_2O_5$ (TAT) layers has three combinations 6/8/6, 3/4/3 and 3/2/3 (unit: nm). Although the range of dielectric layer combinations and thickness could be extended, our results nevertheless support and justify our conclusions.

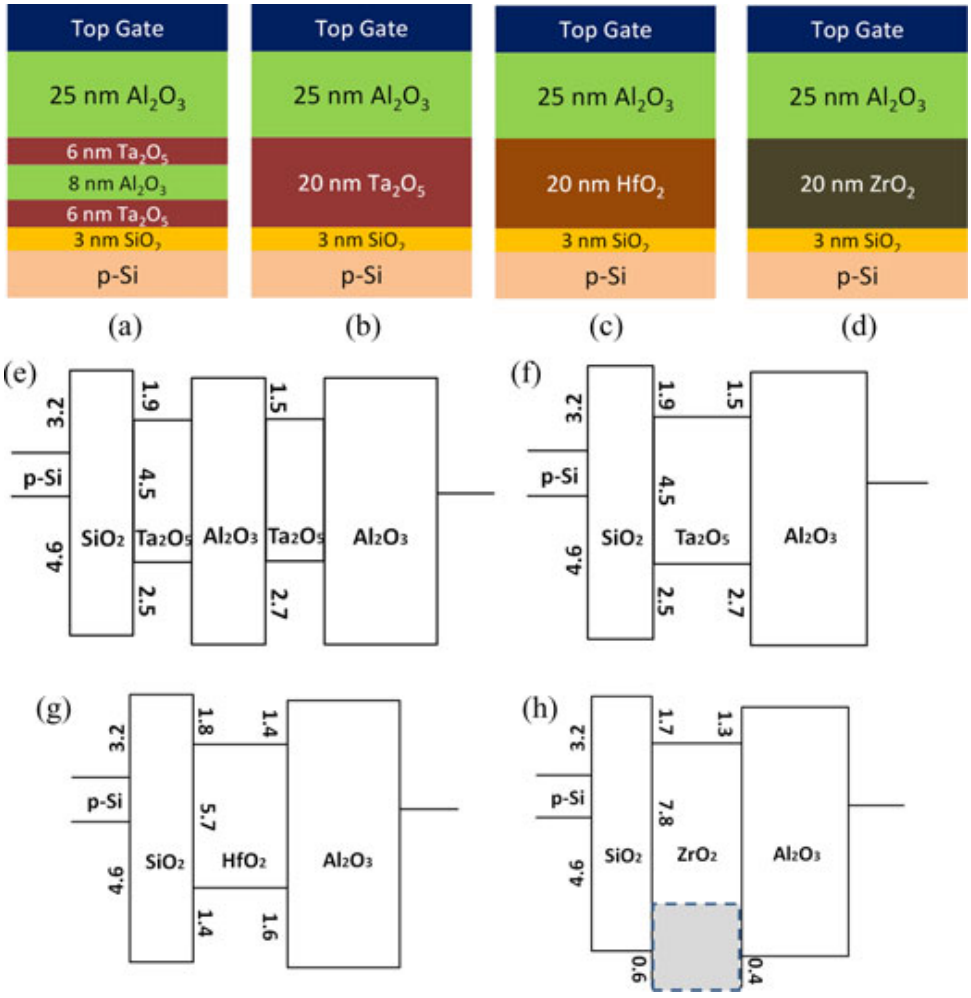

Fig. 3.1 (a) - (d) Schematic structures and (e) - (h) theoretical band diagrams without external electric field (unit: eV) of four proposed and fabricated capacitor devices MATATOS, MATOS, MAHOS, and MAZOS, respectively.

Fig. 3.1(e) - (h) show the theoretical band diagrams of the four devices in the flat-band condition, indicating the band gap and band offset of the four heterostructures. The Al_2O_3 has a large band gap of 8.9 eV and a dielectric constant of 9, making it a very good blocking layer material. The band gap of ZrO_2 is dependent on deposition methods, ranging from 5.5 eV to 7.8 eV. [142, 143] The Pd metal gate replacing poly-Si is deposited on Al_2O_3 for better contact and less resistance.

3.2.2 P/E Operation Characterizations and Discussion

High frequency (at 1 MHz) capacitance-voltage (C - V) hysteresis curves corresponding to different gate voltage sweep ranges for the four devices are shown in Fig. 3.2. Among all the fabricated devices, the MATATOS device exhibits the largest memory window (about 13.0 V) for a sweep of -17.0 V to +17.0 V, which is promising for practical memory applications. With the same sweep range (same ramp rate and time for all the sweeps), the MATOS, MAHOS and MAZOS devices exhibit memory windows of ≈ 11.0 V, ≈ 7.0 V, and ≈ 9.0 V, respectively. It should be noted that contact between different dielectrics often leads to electrical dipoles which may slightly shift the C-V curves. [144]

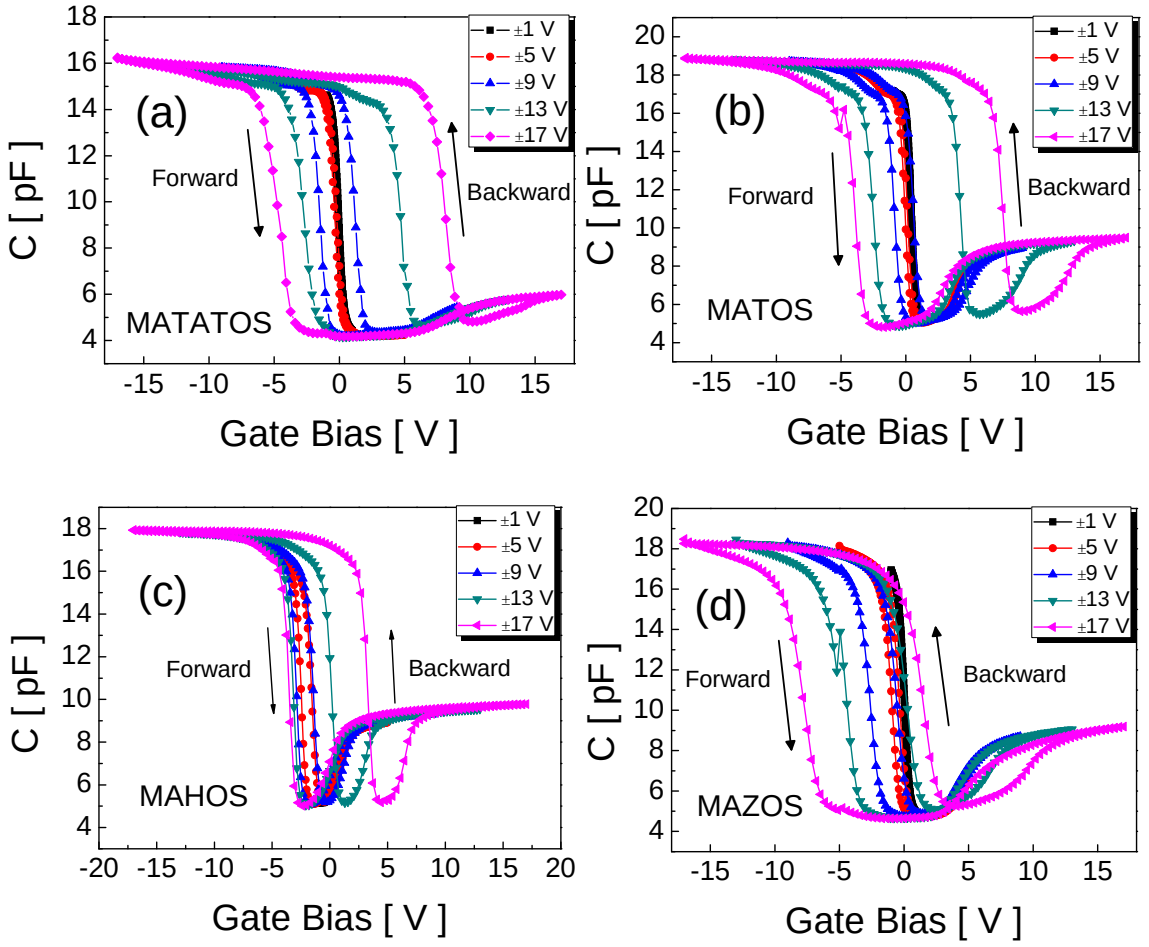

Fig. 3.2 High frequency (1 MHz) C-V hysteresis curves corresponding to different gate voltage sweep ranges for four devices: (a) MATATOS; (b) MATOS; (c) MAHOS; (d) MAZOS. The arrows indicate the directions.

Fig. 3.3 illustrates the P/E operations of the memory devices under different voltage pulses (sweeping direction from negative to positive gate voltage). The P/E characteristics were measured by studying the flat-band voltage shift (ΔV_{FB}) of the C-V hysteresis curves at 10^6 Hz. When the capacitor is stressed at a positive voltage, electrons in Si will tunnel through the tunneling layer (3 nm SiO_2) and get trapped in the charge trapping layer, which corresponds to a programming operation. After applying 10 V

pulses with different width, C-V curves were subsequently swept to study the electron injection, followed by applying -10 V pulses corresponding to erasing operation, during which the holes in Si will tunnel through the tunneling layer into the charge-trapping layer and the electrons in the trapping layer will tunnel back to Si.

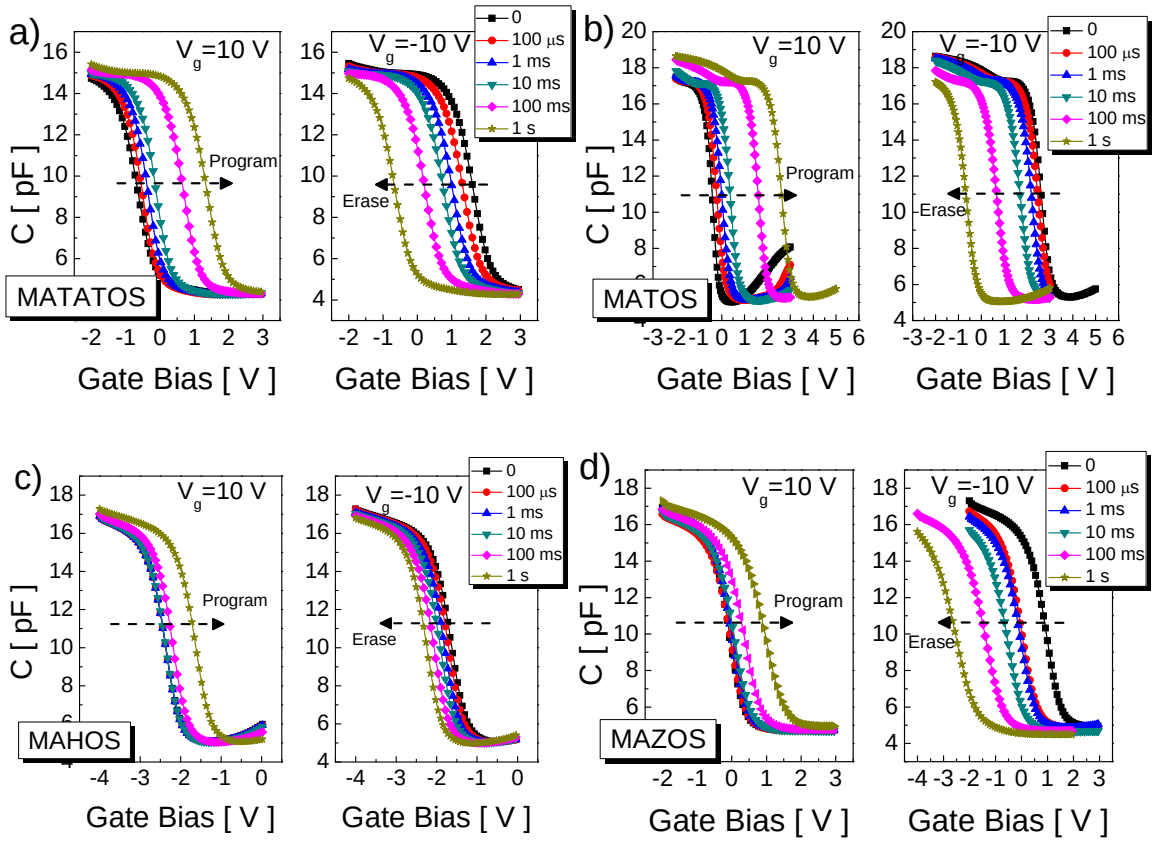

Fig. 3.3 Programming and erasing C-V measurements with different P/E time at ±10 V gate voltage pulses on (a) MATATOS; (b) MATOS; (c) MAHOS; (d) MAZOS devices, respectively.

As shown in Fig. 3.3, the C-V curves at high frequency (10^6 Hz) for various pulse widths, a significant ΔV_{FB} has been observed for the MATATOS and MATOS devices (0.24 V and 0.11 V, respectively) under a rectangular programming pulse of (+10 V, 100

μs), while a pulse of (+10 V, 100 ms) is required to effectively program the MAHOS and MAZOS devices for the same ΔV_{FB}. During the erasing operations, voltage pulses of -10 V were applied and all the devices exhibited negative ΔV_{FB}, indicating that the holes in Si have been injected and stored in the charge-trapping layer. The ΔV_{FB} does not saturate with long pulse width (up to the measurement limit, 1 s) at pulse voltage ±10 V. This means that the Ta_2O_5, HfO_2 and ZrO_2 trapping mediums offer sufficient density of trapping centers for both injected electrons and holes in programming and erasing operations, respectively.

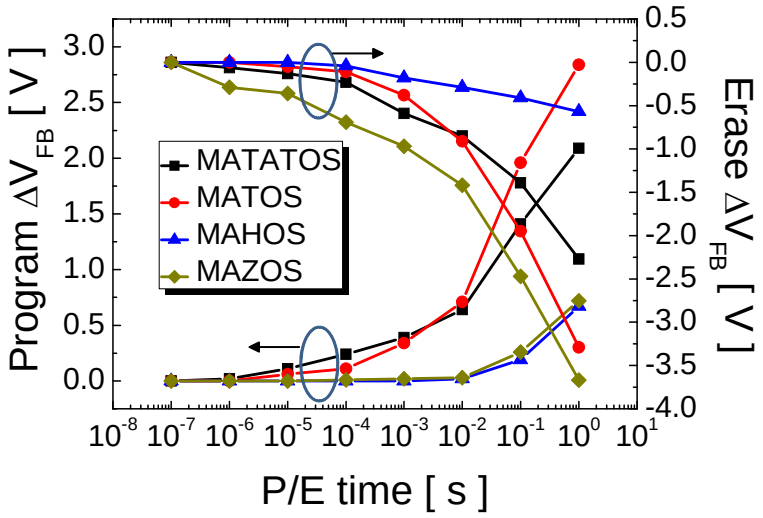

Fig. 3.4 Programming and erasing speed characterization of four memory devices at different P/E time. The P/E gate voltage is ±10 V.

The P/E characteristics of four devices are shown in Fig. 3.4. Both the MATATOS and MATOS devices exhibit excellent P/E speed, with significant ΔV_{FB} at a short pulse width (10 μs), while the MAHOS device exhibits smaller ΔV_{FB}. This indicates

that the sputtered Ta_2O_5 has larger trapping density than the ALD HfO_2 in this work. It should be noted that the properties of these high-*k* dielectric materials are dependent on the preparation methods. For example, the MAZOS devices have the poor programming speed but fast erasing speed. One possible reason is that the ZrO_2 deposited by sputtering at room temperature has a large band gap (about 7.8 eV) leading to a small valence band offset relative to the SiO_2 and Al_2O_3 (see Fig. 3.1(h)), which will be easier for holes to tunnel through the tunneling layer and get trapped in the ZrO_2. It is also possible that the traps in ZrO_2 are distributed at higher energy position for electrons or lower energy position for holes. Since the MAZOS devices have poor programming characteristics and resemble to MAHOS devices, they will not be included in the following discussion.

For short P/E operations, the same amount of charges (electrons or holes) stored in the first Ta_2O_5 layer of MATATOS structure see smaller capacitance between the charges and the top gate as compared with the charges stored in MATOS (Al_2O_3 has smaller dielectric constant than Ta_2O_5). As a result, the ΔV_{FB} of MATATOS devices is larger than that of MATOS devices for a short P/E pulse. This means the MATATOS devices has faster P/E speed than MATOS device. For a long P/E pulse, the MATATOS devices have a smaller ΔV_{FB} because the MATOS structure has a thicker charge-trapping layer (20 nm Ta_2O_5) than the MATATOS structure.

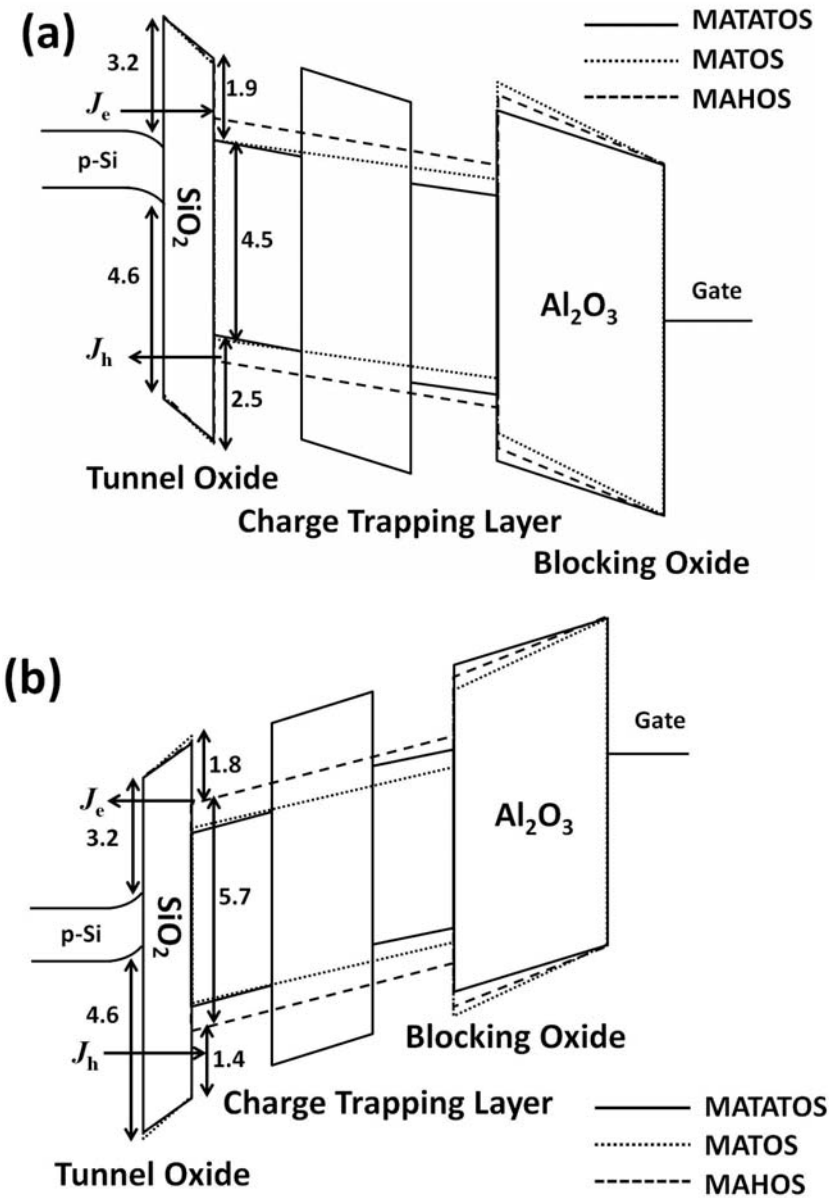

Fig. 3.5 Schematic band diagrams of three device structures under (a) programming and (b) erasing operations. The solid line represents MATATOS structure; the dotted line represents the MATOS structure; the dashed line represents the MAHOS structure.

The P/E characteristics of the three devices, MATATOS, MATOS and MAHOS, can be better understood by their schematic band diagrams shown in Fig. 3.5. In the programming operation, electrons from the Si substrate tunnel through the 3.2 eV barrier

between the conduction band of Si and SiO_2 and are stored in the dielectric charge-trapping layer (electron current: J_e). Meanwhile, holes in the charge-trapping layer will tunnel to the Si substrate (hole current: J_h). J_h is much less than J_e because the barrier between the charge-trapping layer (Ta_2O_5 or HfO_2) and SiO_2 is thick, and the hole density in the trapping layer is very low. In the erasing operation, the pre-stored electrons tunnel back to Si (J_e) and the holes in Si tunnel into the charge-trapping layer (J_h). J_h is much smaller than J_e because the hole barrier between the valence bands of Si and SiO_2 is much larger than the electron barrier. Therefore, electron (instead of hole) plays the key role in the programming and erasing operations.

3.2.3 Retention and Endurance

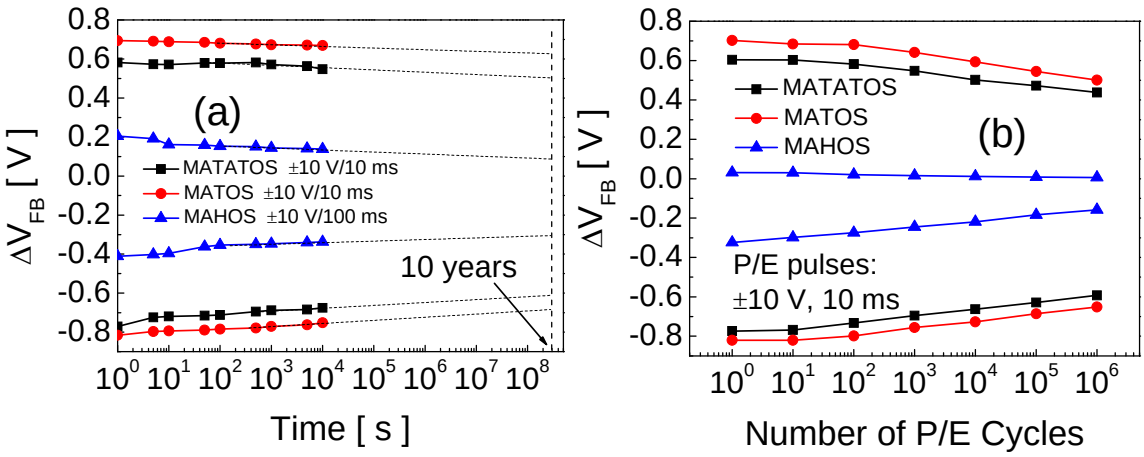

Fig. 3.6 (a) Retention characteristics at room temperature of three memory devices. MATATOS and MATOS devices were initially programmed and erased by ±10 V, 10 ms pulses; MAHOS device was initially programmed and erased by ±10 V, 100 ms pulses; (b) Endurance characteristics of three memory devices.

The MATATOS, MATOS and MAHOS devices exhibit 10-year memory windows of 1.12 V, 1.31 V, and 0.39 V, respectively as illustrated by the retention measurements shown in Fig. 3.6(a). The loss of charge in the MATATOS and MATOS devices is less than 15% with respect to the initial value, while the loss of charge is greater in the MAHOS devices (≈ 40%). The good retention characteristics of MATATOS and MATOS devices are due to the smaller band gap and deep trap level in Ta_2O_5 (~ 2.7 eV). [145, 146] Fig. 3.6(b) shows the endurance measurement of these three types of devices. The P/E voltage pulses were ±10 V, 10 ms. Less than 30% memory window degradation was observed for MATATOS and MATOS devices after 10^6 P/E cycles, and memory window decreased about 45% for the MAHOS device. We attribute the good endurance characteristics of the MATATOS and MATOS devices to the intrinsic stability of the material properties of Ta_2O_5 and the high-quality dielectric stack interfaces.

In addition, in order to convince that the C-V sweep experiment is repeatable and reliable, multiple consecutive sweeps in the same direction have been carried out on MATATOS and MATOS sample. As shown in Fig. 3.7, no flat band voltage shift was observed. This indicates that the small V_{FB} shift in the previous experiment is not a result of measurement sweep.

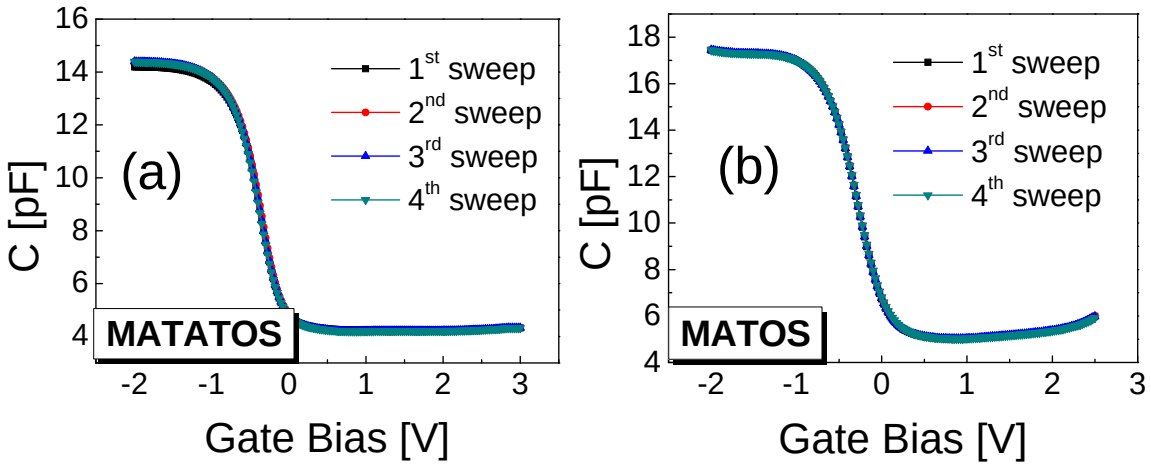

Fig. 3.7 Multiple consecutive C-V sweeps of (a) MATATOS and (b) MATOS devices. No flat band voltage shift was observed in the C-V sweep measurement.

3.2.4 Multi-Bit Storage

The characteristics of ΔV_{FB} as a function of programming voltage were measured with 100 ms pulses as shown in Fig. 3.8. Clear staircase memory characteristics have been observed for both MATOS and MATATOS devices. For the MATOS devices, as the programming voltage increases, the flat-band voltage begins to shift at ≈ 8.0 V, indicating the start of electron tunneling from the Si through the tunneling layer to the Ta_2O_5 layer. By treating the high-k layers as capacitors connected in series, the electric field across the tunneling oxide at this starting voltage (8.0 V) is estimated to be ≈ 4.7×10^6 V/cm. The dielectric constants of SiO_2, Ta_2O_5, and Al_2O_3 used in the calculation are 3.9, 25, and 9, respectively. The ΔV_{FB} for the MATOS devices is saturated (ΔV_{FB} ≈ 16.0 V) by ≈ 40.0 V programming gate voltage, indicating that all the charge storage centers in the 20 nm Ta_2O_5 layer have been filled with electrons. The ΔV_{FB} of MATATOS devices appears at a slightly smaller gate voltage (≈ 6.0 V), indicating the

electrons in Si start to tunnel through the tunneling layer to the first Ta_2O_5 layer. The electric field across the tunneling layer at this starting voltage (6.0 V) is ≈ 3.7×10^6 V/cm.

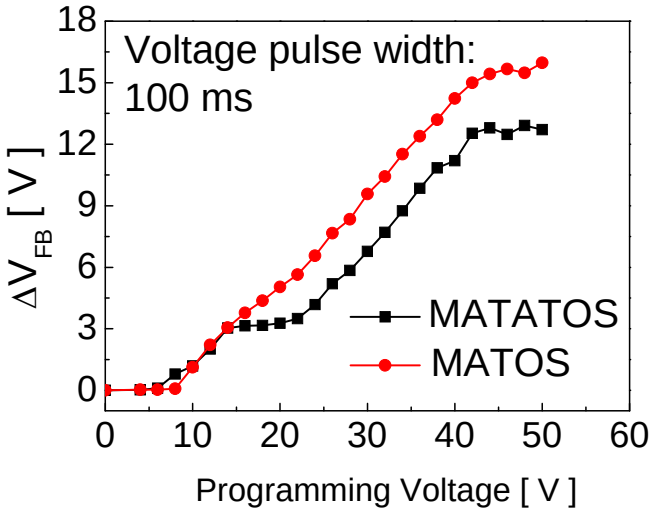

Fig. 3.8 ΔV_{FB} as a function of programming voltage of MATATOS and MATOS devices. Multiple staircase steps were observed for MATATOS device.

The MATATOS devices were designed to give multiple charge storage states. The first charged state arises from charge storage in the first Ta_2O_5 layer (adjacent to the tunneling layer) and a second staircase occurs due to the charge storage in the second Ta_2O_5 layer. Multiple staircase steps were experimentally observed in MATATOS devices (Fig. 3.8), indicating the multiple discrete charge storage states as designed and expected. The initial step at ≈ 7 V programming voltage is due to charge storage in the first Ta_2O_5 layer and the second staircase step at larger programming voltage (≈ 16 V) is due to the charge storage in the second Ta_2O_5 layer. These two charge storage layers are separated by an 8 nm Al_2O_3 layer which acts as the blocking oxide for the first Ta_2O_5

layer and the tunneling oxide for the second Ta_2O_5 layer. This Al_2O_3 separation layer is important to realize multiple discrete charge-storage states. With the assumption that charges are distributed evenly in each Ta_2O_5 layer (the charge densities in the first and second Ta_2O_5 layers are n_{s1} and n_{s2}, respectively), the ΔV_{FB} at the staircase steps can be determined:

$$\Delta V_{FB1} = \frac{q \cdot n_{s1}}{C_1} = q \cdot n_{s1} \cdot \left(\frac{0.5\, t_{TaO}}{\varepsilon_0 \varepsilon_{TaO}} + \frac{t_{AlO1}}{\varepsilon_0 \varepsilon_{AlO}} + \frac{t_{TaO}}{\varepsilon_0 \varepsilon_{TaO}} + \frac{t_{AlO2}}{\varepsilon_0 \varepsilon_{AlO}} \right)$$

$$\Delta V_{FB2} = \frac{q \cdot n_{s2}}{C_2} + \Delta V_{FB1} = q \cdot n_{s2} \cdot \left(\frac{0.5\, t_{TaO}}{\varepsilon_0 \varepsilon_{TaO}} + \frac{t_{AlO2}}{\varepsilon_0 \varepsilon_{AlO}} \right) + \Delta V_{FB1}$$

where ΔV_{FB1} and ΔV_{FB2} are the flat-band voltage shift obtained at the first and second staircase steps, respectively; q is elementary charge; t_{TaO} and ε_{TaO} are thickness (6 nm for both layers) and dielectric constant of Ta_2O_5; t_{AlO1} and t_{AlO2} are the thickness of the middle (8 nm) and top (25 nm) layers of Al_2O_3, respectively; ε_{AlO} is the dielectric constant of Al_2O_3. From the data in Fig. 3.8, the charge densities of the first and second Ta_2O_5 layer are $\approx 4.3\times10^{12}$ cm^{-2} and $\approx 1.8\times10^{13}$ cm^{-2}, respectively. The calculation used the values ΔV_{FB1} = 3.1 V and ΔV_{FB2} = 12.7 V. The result indicates that the second Ta_2O_5 layer can store more charges than the first layer in this case ($\approx$ 4 times as much). Because the SiO_2 tunneling barrier between the first Ta_2O_5 layer and Si is thinner than that for the second Ta_2O_5 layer, a small amount of charges stored in the first Ta_2O_5 layer will induce a large electric field in the thin SiO_2 tunneling barrier and more electrons tunnel out of the first layer than tunnel out of the more electrically isolated second layer. It should be noted that the trap density (1.8×10^{13} cm^{-2}) in the 6 nm Ta_2O_5 layer are quite high. It could

be resulted by the room temperature sputtering and the interface defect between Ta_2O_5 and Al_2O_3.

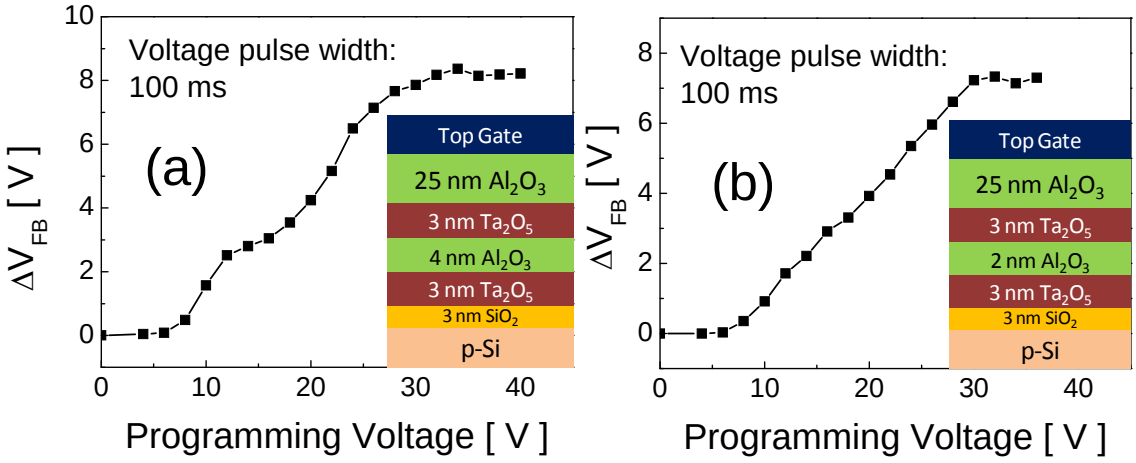

Fig. 3.9 ΔV_{FB} as a function of programming voltage of MATATOS device with thinner TAT stacks: (a) 3 nm / 4 nm / 3 nm; (b) 3 nm / 2 nm / 3 nm. Insets: schematic structure of the devices. Staircase behavior was not as clear as previous devices.

The ΔV_{FB} that arises from the charging of each of the two Ta_2O_5 layers is quite large, indicating that the Ta_2O_5 layer offers sufficient charge storage centers in these MATATOS devices. While these results illustrate the potential of multiple trapping layers based upon Ta_2O_5, further engineering of the dielectric stack and shrinking of the thickness of the Ta_2O_5 and Al_2O_3 layers is necessary to achieve technologically attractive write/erase voltages. As shown in Fig. 3.9(a) with a 3 nm / 4 nm / 3 nm and Fig. 3.9(b) a 3 nm / 2 nm / 3 nm TAT stack, multiple charge storage can also be achieved at smaller voltage, but the staircase behavior is not as well-defined relative to the device shown in Fig. 3.8. The multistate behavior almost disappears when the middle Al_2O_3 layer

thickness in the stack is further decreased to 2 nm due to coupling between the two Ta_2O_5 layers. These data illustrate the importance of properly designing the separation layer.

3.2.5 Summary

In summary, we have fabricated and studied Ta_2O_5 containing charge-trapping dielectric stacks for discrete multi-bit non-volatile memory applications. As compared to the charge-trapping non-volatile memory made with HfO_2 and ZrO_2 materials, the MATATOS and MATOS devices showed excellent P/E characteristics, good retention and endurance. The MATATOS and MATOS devices exhibit less than 15% charge loss over a projected period of 10-years and less than 30% memory window degradation after 10^6 P/E cycles. These excellent characteristics are due to both the intrinsic material properties of Ta_2O_5 and the overall structure of the Ta_2O_5-containing dielectric stacks. Thus, we have successfully designed and fabricated MATATOS devices with multiple discrete charge-storage states. Such devices are very attractive for multi-bit non-volatile memory applications.

3.3 Ta_2O_5 Stacks on SiNW FET for Multi-Bit Flash Memory Application

With the knowledge and understanding we have developed above for multi-bit memory application, we studied the integration of multiple Ta_2O_5 stack on SiNW FETs for three-terminal, transistor-level Flash memory. Semiconductor nanotube and nanowire FETs have been regarded as building blocks for nanoelectronic device, and they will provide solution for future memory technology. For instance, SiNW FET with single or

multiple nanowire channels can enable gate-surrounding structure, allowing excellent electrostatic gate control. Employing Si nanowire as an alternative for bulk silicon will be useful for the design and optimization of nanowire FETs and related nanoelectronic devices. In this work, we report Flash memory devices with Ta_2O_5 and $Ta_2O_5/Al_2O_3/Ta_2O_5$ stack as charge-trapping layer based on SiNW FETs which have been prepared by using the self-alignment method. Our results demonstrate that the Ta_2O_5 stacks on SiNW FETs charge-trapping Flash memory exhibit better performance as compared with the capacitor memory cells, and are prominent candidates for future real Flash memory implementation.

3.3.1 Experimental Details

Our SiNW FETs were prepared by following the self-alignment method described in the previous chapter. Typically, a 300 nm SiO_2 was first grown on a highly doped p-type Si (100) wafer by dry oxidization. Then a thin film of Au catalyst (2 nm to 4 nm) was deposited on patterned area pre-defined by photolithography. Then the Si nanowires were grown from the catalyst in a low-pressure chemical vapor deposition (LPCVD) furnace at 440 ^oC for 2 h with an ambient SiH_4 stream under a pressure of 500 mTorr. The Si nanowires growth followed the vapor-liquid-solid (VLS) mechanism, with typical length of 20 μm and 20 nm in diameter. Immediately after the growth step, the Si nanowires were oxidized at 750 ^oC for 30 min to form a ≈ 3 nm SiO_2 which will function as tunneling oxide. The next step is to pattern the source/drain (S/D) electrodes with photolithography. A 2% HF wet etching was applied to remove the oxide from the Si

nanowire at patterned S/D area immediately before the 3/100 (unit: nm) Ti/Pt was deposited by E-beam evaporation and lift-off process to form the Schottky barrier S/D contacts. The channel length between the S/D electrodes was controlled to be 5 μm. The following process is the deposition of charge-trapping layer and blocking oxide dielectric stacks. We fabricated Ta_2O_5, $Ta_2O_5/Al_2O_3/Ta_2O_5$ (TAT), and a reference HfO_2 covering the tunneling oxide on Si nanowire as charge-trapping layer, with thickness of 20, 6/8/6, 20 (unit: nm), respectively. And the blocking oxide for all the memory devices was selected to be 25 nm Al_2O_3. Ta_2O_5 layers were deposited by sputtering, while the Al_2O_3 and HfO_2 layers were deposited by ALD with TMA and TEMAH as the precursors, respectively. Finally, a 100 nm Pd top gate was formed by the same lift-off process as the S/D electrodes. A schematic of the SiNW FET based dielectric Flash memory is shown in Fig. 3.10(a).

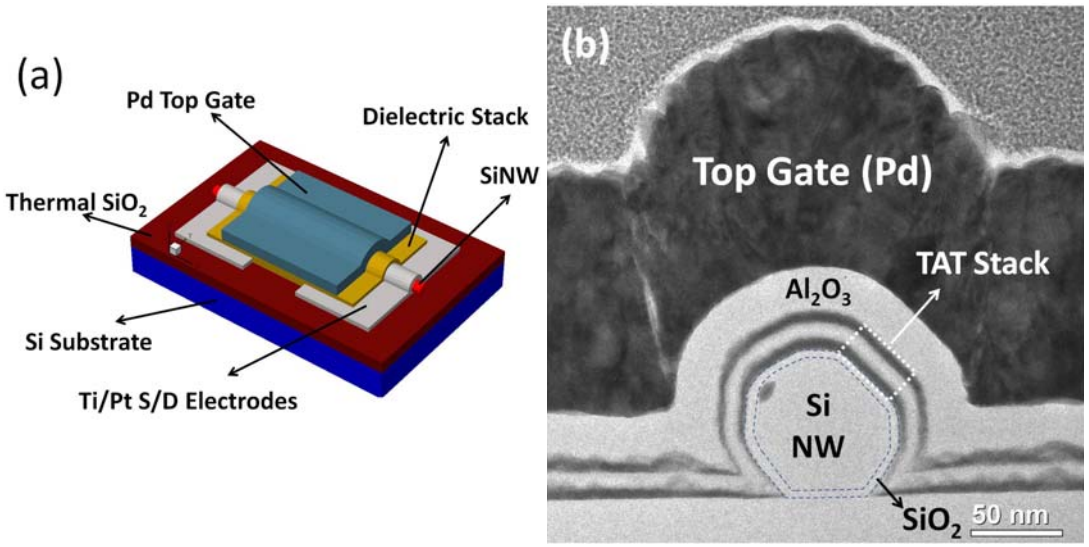

Fig. 3.10 (a) Schematic of top view of the dielectric charge-trapping Flash memory; (b) TEM image of the cross section of a SiNW FET based dielectric Flash memory with TAT charge-trapping layer.

The self-alignment fabrication process used in this work is promising compared to regular nanowire harvesting and manipulation processes. It not only enables simultaneous batch fabrication of high quality, reproducible, and homogeneous nanowire devices at the wafer scale, but also limits the fabrication steps in which the nanowires can be contaminated.

3.3.2 Electrical Characterizations and Memory Performance

As mentioned above, three SONOS-like charge-trapping Flash memory devices with structures of Metal/Al_2O_3/Ta_2O_5/Al_2O_3/Ta_2O_5/SiO_2/Si (MATATOS), Metal/Al_2O_3/Ta_2O_5/SiO_2/Si (MATOS), Metal/Al_2O_3/HfO_2/SiO_2/Si (MAHOS) have been fabricated, similar to the stacks in the previous capacitor structure memory cells. A TEM image of the cross section of a MATATOS device is shown in Fig. 3.10(b). The SiNW core is surrounded by the dielectric stack and top gate.

Typical output characteristics (source-drain current vs. source-drain voltage I_{DS}-V_{DS}) of the self-aligned SiNW FET based Flash memory are shown in Fig. 3.11(a) (MATATOS). Due to the Schottky contacts between the S/D contacts and the intrinsic SiNW, Schottky-barrier pMOSFET characteristics are expected. As shown in Fig. 3.11(a), the drain current keeps increasing with V_{DS} when V_{GS} is higher than threshold voltage (V_{Th}), and gets well saturated beyond a certain V_{DS}. It should also be noted that the I_{DS}-V_{DS} curves increased sharply in the linear region, indicating a small source and drain contact resistance.

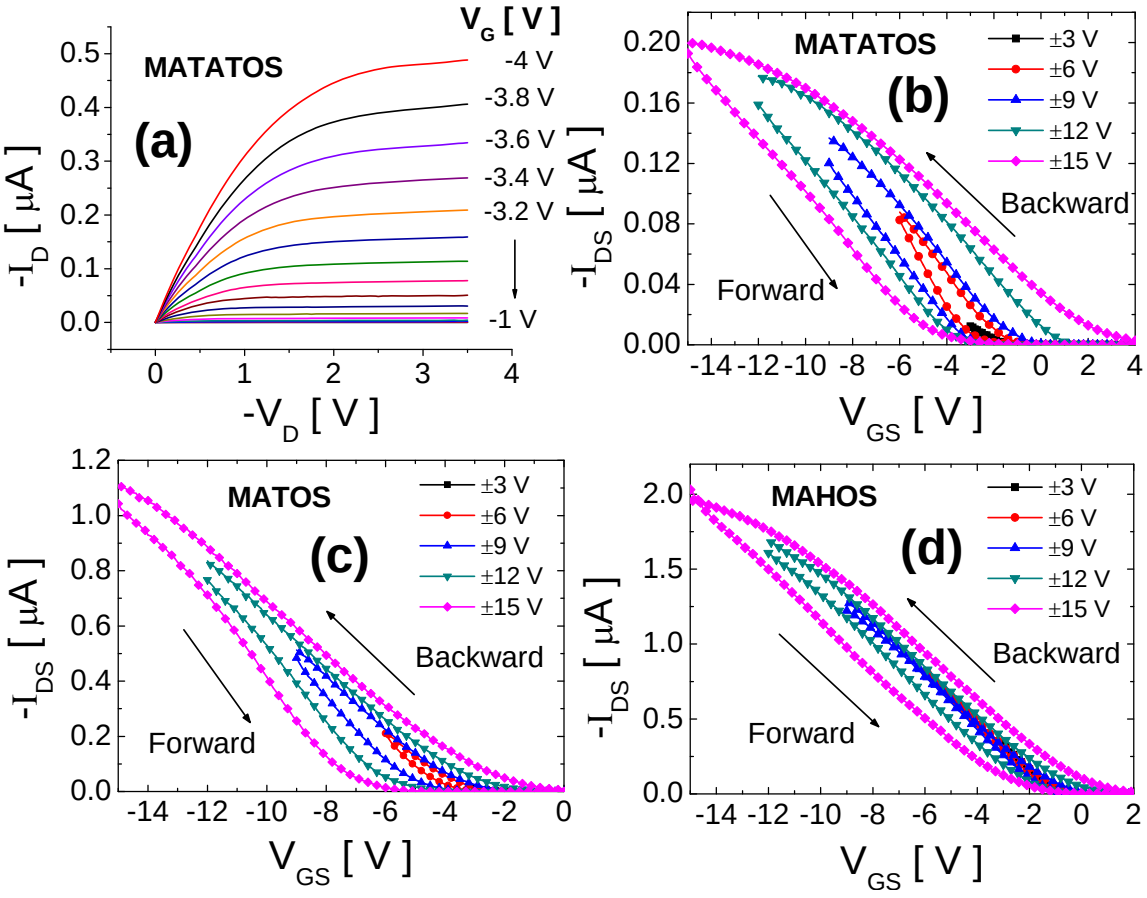

Fig. 3.11 (a) Output characteristics of MATATOS device for V_{GS} from -4 V to -1 V; Transfer characteristics of (b) MATATOS, (c) MATOS, and (d) MAHOS devices, showing counterclockwise hysteresis loops under different V_{GS} sweep ranges of ±3 V, ±6 V, ±9 V, ±12 V, and ±15 V, respectively. The arrows indicate the directions.

Transfer characteristics of three structure memory devices are shown in Fig. 3.11(b) - (d), respectively. The hysteresis curves corresponding to different gate voltage sweep ranges clearly demonstrated counterclockwise loops, suggesting the charging and discharging in the charge-trapping layers in the memory cells. By comparing the memory window of the three devices, the MATATOS and MATOS devices show the larger values

of 3.8 V and 2.7 V with ±12 V gate voltage scan range, while the MAHOS device shows hysteresis memory window of 0.9 V with the same measurement condition.

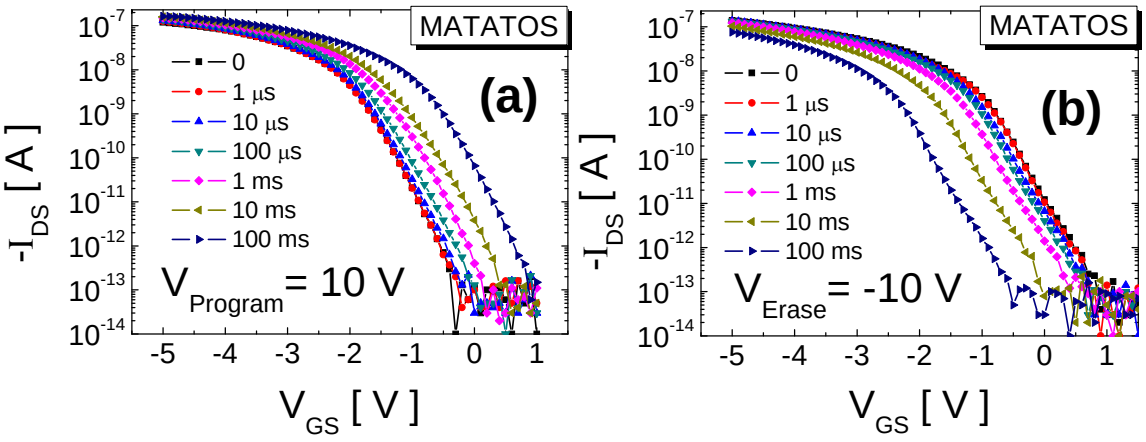

Fig. 3.12 (a) Programming and (b) erasing operations with accumulated P/E time at ±10 V gate voltage pulses on MATATOS Flash memory device.

The programming and erasing operations on MATATOS were measured by studying the threshold voltage shift (ΔV_{Th}) under different P/E operations, and are illustrated in Fig. 3.12. The I_{DS}-V_{GS} curves showed clear ΔV_{Th} under accumulative rectangular gate voltage pulses with increasing pulse width. The curves obtained before and after the programming or erasing operations have almost the same subthreshold slope ($S \approx 300$ mV/dec), indicating that the ΔV_{Th} is due to the fixed charges in the charge-trapping layers, instead of the interface states. By stressing a positive gate voltage, the electrons will tunnel through the tunneling oxide from the Si nanowire and get trapped in the charge-trapping layers, corresponding to programming operations, which will result in a V_{Th} shift toward the positive direction. The following application of a negative gate

voltage will then enable the back tunneling of the pre-trapped electrons from the charge-trapping layer to the Si nanowire, and the V_{Th} will be shifted in the opposite direction, defined as erasing operations. As discussed in the previous section on the band diagram of the dielectric stacks, the conduction band offset of Ta_2O_5 with respect to Si (1.3 eV) is smaller than that of HfO_2, resulting in a shorter tunneling distance from Si nanowire to the conduction band of the charge storage dielectric due to the modified Fowler-Nordheim (FN) tunneling mechanism. Furthermore, the 2.7 eV deep trap energy level of Ta_2O_5 is more favorable than that of HfO_2 which is about 1.5 eV for the consideration of charge storage retention. The 1.9 eV conduction band offset between SiO_2 and Ta_2O_5 with respect to Si also inhibits the back tunneling of electrons to the nanowire more effectively than that between the SiO_2 and HfO_2. Thick (25 nm) and high quality Al_2O_3 deposited by ALD with large barrier height was used as blocking oxide in all of our devices. So the back tunneling of hole in programming operations and electron in erasing operations from the top gate were not considered in our discussion.

From Fig. 3.12, MATATOS memory shows significant ΔV_{Th} (0.32 V) with +10 V, 100 μs rectangular programming pulses; while in the erasing operations, -10 V, 100 μs pulses would effectively erase the programmed MATATOS devices, with clear ΔV_{Th} of -0.19 V, showing fast P/E speed. The ΔV_{Th} along positive and negative directions demonstrate the trapping and detrapping of the electrons during the programming and erasing operations.

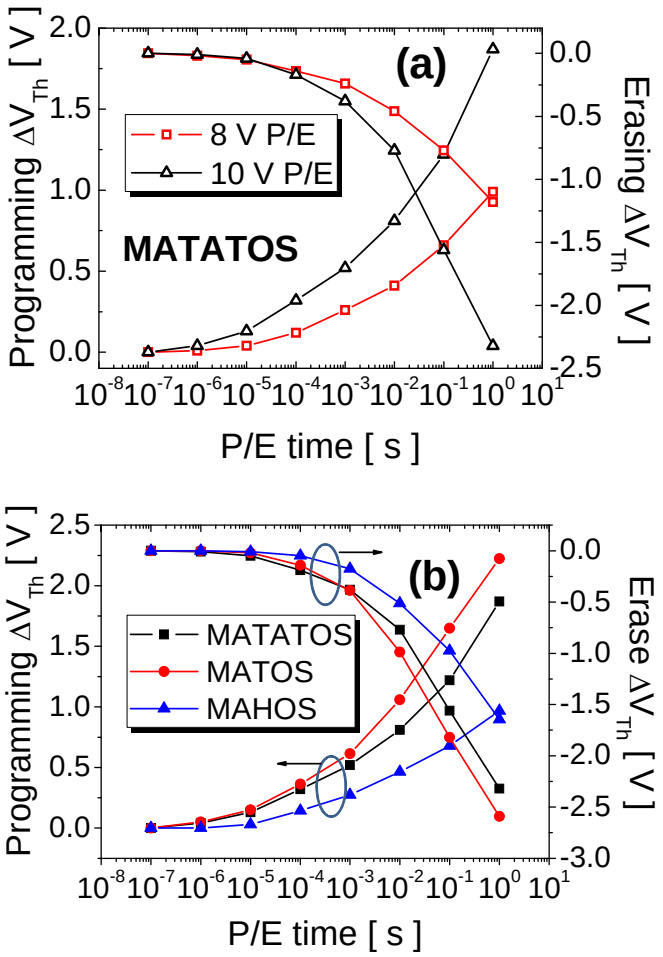

Fig. 3.13 (a) P/E speed characterization of the MATATOS device with ±8 V and ±10 V P/E voltages at different P/E time; (b) P/E speed characterizations of the MATATOS, MATOS, and MAHOS devices at different P/E time. The P/E gate voltage is ±10 V.

By comparing the ΔV_{Th} under different P/E gate voltage, the P/E speed characterization of the memory cells are summarized in Fig. 3.13. As shown in Fig. 3.13(a), the MATATOS device shows sufficiently fast P/E speed with ±8 V P/E pulses as indicated by ΔV_{Th} vs. P/E time. Fig. 3.13(b) compares the P/E operations among the three devices. Both MATATOS and MATOS devices show faster P/E speed than MAHOS device. It was observed that for a long P/E time, the MATOS device shows a larger ΔV_{Th}

than MATATOS device, which is due to the thicker charge-trapping layer in MATOS device (20 nm Ta_2O_5 layer). However, this is not important for fast P/E speed applications. It is worth to mention that all the memory devices show ΔV_{Th} without saturation under long P/E pulse width up to 1 s at pulse voltage ±10 V, indicating that the Ta_2O_5, TAT stack and HfO_2 functioning as storage medium can offer sufficient charge-trapping density for both electrons and holes.

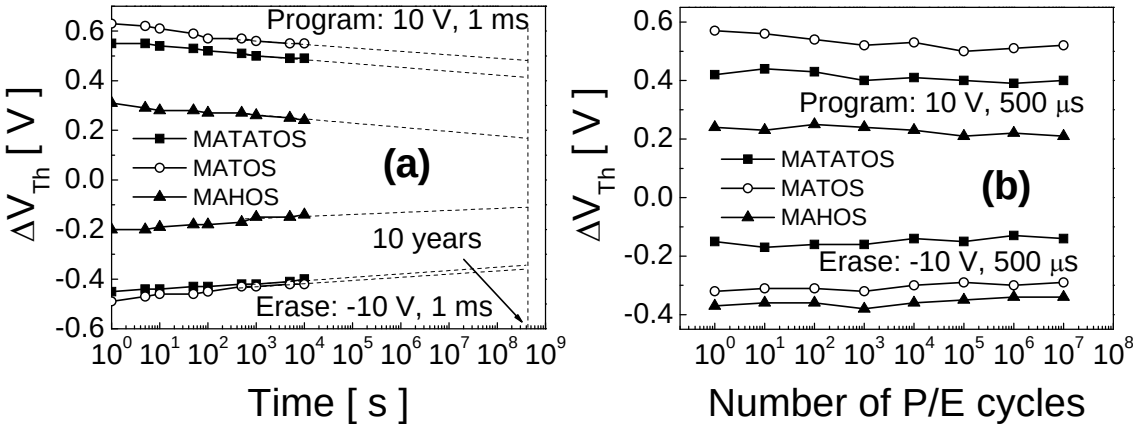

Fig. 3.14 (a) Retention characteristics of three Flash memory devices. The devices were initially programmed and erased by ±10 V, 1 ms pulses; (b) Endurance characteristics of three Flash memory devices. The P/E gate voltage was ±10 V with 500 μs pulse width.

The charge retention properties of the devices are illustrated in Fig. 3.14(a). The memory cells were initially programmed/erased by ±10 V, 1 ms pulses. The MATATOS, MATOS, and MAHOS devices exhibit 10-year memory windows of 0.75 V, 0.84 V, and 0.28 V, respectively. As compared with the initial value, the charge loss of MATATOS and MATOS devices is less than 25%, while the charge loss is around 45% for MAHOS device. The good retention characteristics of MATATOS and MATOS devices could be

attributed to the smaller band gap and deeper trapping level of Ta_2O_5. The endurance characteristics of three devices are shown in Fig. 3.14(b). The P/E voltage pulses were ±10 V, 500 μs. Very small memory window degradations were observed for all devices after 10^7 P/E cycles. This good endurance behavior arises from the good interface between the Si nanowire and the high-*k* stacks formed in the self-alignment fabrication process.

3.3.3 Multi-Bit Storage

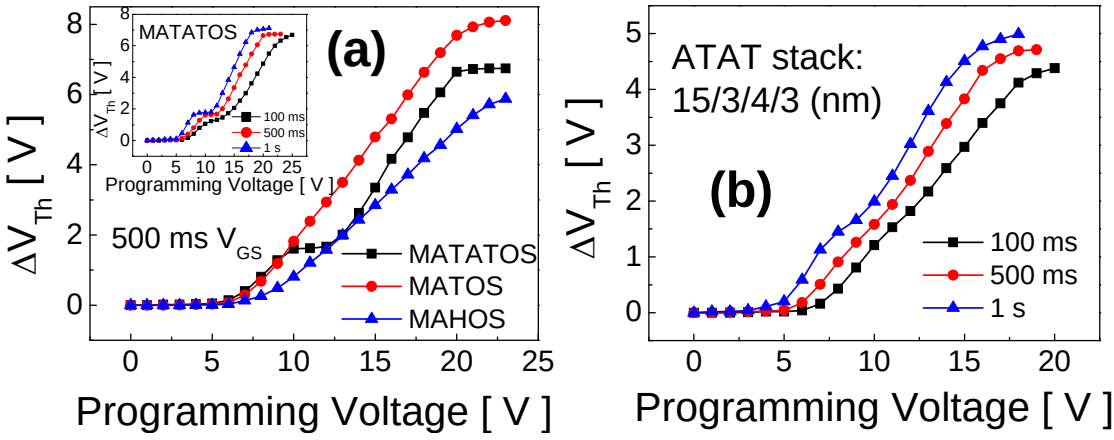

Fig. 3.15 (a) ΔV_{Th} as a function of programming voltage of the MATATOS, MATOS, and MAHOS devices. Two-step charging storage behavior was observed for MATATOS device. Inset: ΔV_{Th} vs. programming voltage of the MATATOS device under gate voltage pulse with different width; (b) ΔV_{Th} as a function of programming voltage of the MATATOS device with thinner ATAT stack.

As discussed in previous section, a discrete multiple charge storage memory characteristics has been observed for capacitor structure TAT stack memory cell with effective cell area of 100 μm×100 μm during the accumulative programming operations. These multiple charge storage states can be designed for multi-bit memory applications.

However, the operation voltage to achieve both charge storage states was very high for applicable electrical characterizations. Using low-dimensional Si nanowire as conducting channel to replace the conventional planar Si substrate can be expected to effectively reduce the operation voltage due to the enhancement in gate electric field introduced by the gate-surrounding structure, and the clean self-alignment fabrication process will further improve the device reliability and overall performance. As shown in the plot of ΔV_{Th} as a function of programming voltage in Fig. 3.15(a), clear staircase characteristics have been observed on MATATOS, MATOS, and MAHOS devices. By applying accumulative programming voltage at a constant rectangular pulse width (500 ms) with increasing pulse height, three devices start to show V_{Th} shift at around 7 V, with ΔV_{Th} of 0.4 V, 0.29 V, 0.13 V for MATATOS, MATOS, and MAHOS, respectively, indicating electrons tunnel from the nanowire through the tunneling oxide and get trapped in the charge-trapping layers. By treating the high-k dielectric as cylindrical capacitors connected in series, and a presumed diameter of 20 nm for Si nanowire channel, the electric field across the tunneling oxide at the voltage 7 V for MATATOS, MATOS, and MAHOS are estimated to be 8.20×10^6 V/cm, 9.47×10^6 V/cm, and 9.38×10^6 V/cm, respectively. For the MATOS and MAHOS devices, ΔV_{Th} keeps increasing with increasing gate voltage, and get nearly saturated beyond 23 V gate voltage, indicating that all the charging centers in the 20 nm Ta_2O_5 and HfO_2 layers have been filled with electrons. For the MATATOS device, after the initial stage which is due to the charge storage in the first Ta_2O_5 layer, a step at around 10 V gate voltage was observed, arising from the charge storage in the second Ta_2O_5 layer. The second step was observed at 20 V

programming gate voltage at which ΔV_{Th} was saturated ($\Delta V_{Th} \approx 6.7$ V), indicating that the charge-trapping centers in both Ta_2O_5 layers have been filled with electrons. These multiple charge storage behavior is due to the 8 nm Al_2O_3 layer sandwiched between the two Ta_2O_5 layers, which functions as the blocking oxide for the first Ta_2O_5 layer and tunneling oxide for the second Ta_2O_5 layer. As compared with our previous capacitor structure memory cells, the two-step storage states in MATATOS device can be achieved by a much lower gate voltage of ~ 20 V. By assuming a uniform trap distribution in the Ta_2O_5 layers, in which case the charge centroid will be about half of the charge-trapping layer thickness, the ΔV_{Th} at charge storage steps can be determined by the following equations:

$$\Delta V_{Th1} = q \cdot n_{s1} \cdot V_1 \cdot \left(\frac{ln\left(\frac{t_{T1in} + 0.5t_{T1}}{t_{T1in}}\right)}{2\pi\varepsilon_0\varepsilon_T L} + \frac{ln\left(\frac{t_{A1out}}{t_{A1in}}\right)}{2\pi\varepsilon_0\varepsilon_A L} + \frac{ln\left(\frac{t_{T2out}}{t_{T2in}}\right)}{2\pi\varepsilon_0\varepsilon_T L} + \frac{ln\left(\frac{t_{A2out}}{t_{A2in}}\right)}{2\pi\varepsilon_0\varepsilon_A L} \right)$$

$$\Delta V_{Th2} = q \cdot n_{s2} \cdot V_2 \cdot \left(\frac{ln\left(\frac{t_{T2in} + 0.5t_{T2}}{t_{T2in}}\right)}{2\pi\varepsilon_0\varepsilon_T L} + \frac{ln\left(\frac{t_{A2out}}{t_{A2in}}\right)}{2\pi\varepsilon_0\varepsilon_A L} \right) + \Delta V_{Th1}$$

where ΔV_{Th1} and ΔV_{Th2} are threshold voltage shift obtained from the two charge storage steps; q is the elementary charge; n_{s1} and n_{s2} are charge density in each Ta_2O_5 layer; V_1 and V_2 are the charge storage volume of two Ta_2O_5 layers; t_{T1in}, t_{T2out}, t_{T2in}, t_{A1out}, t_{A1in}, t_{A2out}, t_{A2in} are distances from the center of Si nanowire to the inside and outside surfaces of each high-k layer (T stands for Ta_2O_5, A stands for Al_2O_3, 1 and 2 stand for the first and second layer of each material); t_{T1} and t_{T2} are the thickness of the two Ta_2O_5 layers; ε_T and ε_A are dielectric constant of Ta_2O_5 and Al_2O_3, respectively; L is the

Si nanowire channel length. With the ΔV_{Th1} (1.61 V) and ΔV_{Th2} (6.73 V) obtained from Fig. 3.15(a), the charge density of the first and second Ta_2O_5 layers are calculated to be 1.75×10^{19} cm^{-3} and 4.98×10^{19} cm^{-3}, respectively. It also corresponds to our results from the capacitor structure memory cells that the second Ta_2O_5 layer exhibits larger charging density, which is due to fact that the second Ta_2O_5 layer is more electrically isolated than the first Ta_2O_5 layer. The above results demonstrate that the self-aligned SiNW FET based Flash memory with TAT stack as charge-trapping layer can offer sufficient charge density, and is very promising to realize the multi-bit memory application in one unit cell. The inset in Fig. 3.15(a) shows the ΔV_{Th} of MATATOS device under accumulative programming voltage with different pulse width. Comparing with the 500 ms programming voltage operations, the 1 s pulse operations lead to the appearance of the two charge storage states at a smaller gate voltage, while with 100 ms pulses, the two charge storage states are less clear. This is because the large amount of charge trapping centers in the first Ta_2O_5 layer are not totally occupied by the injected electrons before the electrons tunneling to the second Ta_2O_5 layer under shorter programming operations. Further engineering of the dielectric stack in MATATOS devices was performed afterwards in order to minimize the device size and to obtain smaller P/E voltages. As shown in Fig. 3.15(b), the multi-state behavior almost disappears with shrunk ATAT stack thickness of 15 nm / 3 nm / 4 nm / 3 nm. Further engineering the structures and materials of the multi-layer dielectric stacks will be able to achieve multi-bit memory combining low operation voltage, fast P/E speed, and good retention.

3.3.4 Summary and Comparison with Capacitor Dielectric Charge-Trapping Memory Device

In summary, SiNW FETs were prepared by self-alignment method for the basis of the charge-trapping Flash memory with novel high-*k* material and dielectric stack for fast speed, reliable, and multi-bit memory applications. The MATATOS and MATOS Flash memory show excellent P/E speed, and good retention and endurance. The MATATOS and MATOS devices exhibit less than 25% charge loss over a projected 10-year period, and negligible memory window degradation after 10^7 P/E cycles. The prominent characteristics are due to the intrinsic properties of Ta_2O_5 material and clean dielectric interfaces formed by self-alignment fabrication process.

Compared to the capacitor charge-trapping memory devices, the SiNW FET based Flash memory with same thickness dielectric gate stack exhibits faster speed, better endurance, and more remarkable discrete multi-bit memory storage at lower operation voltages. The scaling from planar Si to nano-scale SiNW channel effectively enhances the top gate electric field due to the gate-surrounding structure, enabling faster speed at lower voltage. The device reliability is improved with the clean nanowire surface and dielectric interfaces formed by using the self-alignment technique. Such a high-performance and CMOS compatible Flash memory is very attractive for future multi-bit non-volatile memory application.

Chapter 4 Molecular Charge-Trapping Non-Volatile Memory

4.1 Introduction

The continuous CMOS scaling to achieve more powerful central processing unit (CPU) is reaching the fundamental limits imposed by heat dissipation and short-channel effects. This will finally stop the increase of integration density of transistors in the logic circuit of CPU which was predicted by Moore's Law. In order to increase the ability of CPU, extensive motivation and efforts have been stimulated for developing high-performance non-volatile memory as local CPU memory, replacing the conventional on-chip cache memory – static random-access memory (SRAM), which is volatile and usually occupies a large floor space.

Molecular technology has been aggressively pursued for their potential impact in future nano-scale electronics since early 1970's due to the inherent scalability and intrinsic properties. [147-149] Molecular memory, among all the new emerging candidates in recent years, is considered promising, particularly in the aim of reducing the size per cell, and enhancing the memory speed, density, and reliability. [150] It has been demonstrated that the redox-active molecules attached on Si structures are stable and can endure more than 10^{12} program/erase (P/E) cycles. [65] This excellent performance is naturally derived from the intrinsic properties of redox molecules. Such molecular electronic devices are typically fabricated by forming a self-assembled

monolayer (SAM) or multi-layer on different surfaces with very cheap and simple processing methods. Moreover, molecular memory works on the controlling of fewer electrons in molecule scale, and therefore has potential for low power and ultra-high density memory applications with lower fabrication cost. Typically, applying an oxidation voltage will cause electron loss in redox molecules; reversely, under a reduction voltage, electrons will be driven back to the molecules. Due to oxidation and reduction of the redox centers, these redox molecules can exhibit distinct charged or discharged states, which can be deemed as logic On and Off states, at different voltages with very fast write and erase speed. These advantageous properties of redox molecules make them very promising candidates for future applications on on-chip non-volatile memory, such as SRAM and dynamic random-access memory (DRAM). In addition, due to the scalability of molecules and the naturally-derived multiple redox states for robust charge storage, the molecular memory density can be much higher than the conventional memory devices. [63, 66, 151]

The CMOS-compatible integration of redox-active molecules into a solid-state structure is very attractive. [69, 152] This chapter describes the characterizations of redox-active molecules attached on Si and SiO_2 active surfaces, and explores the memory performance of the molecules as charge storage medium in non-volatile memory. Self-aligned Si nanowire field-effect transistors (SiNW FETs) were also prepared for novel molecular Flash memory with molecules attached on the tunneling oxide for charge storage. The results demonstrate that molecular Flash memory is very promising for future on-chip memory applications due to their fast P/E speed at low P/E voltages and

excellent endurance over 10^9 P/E cycles. Multi-bit storage can be achieved by employing redox molecules with multiple redox centers as charge storage medium in a Flash memory.

4.2 Redox-Active Molecules toward Non-Volatile Memory Application

In our work, we have developed a Si-molecular integration process to preserve the intrinsic redox properties and studied the charge storage properties of the molecular memory capacitor. The devices exhibit high P/E speed and excellent endurance. We demonstrate that the hybrid integration of redox-active molecules on a semiconductor platform is very attractive for high-performance non-volatile memory applications.

4.2.1 Experimental Details

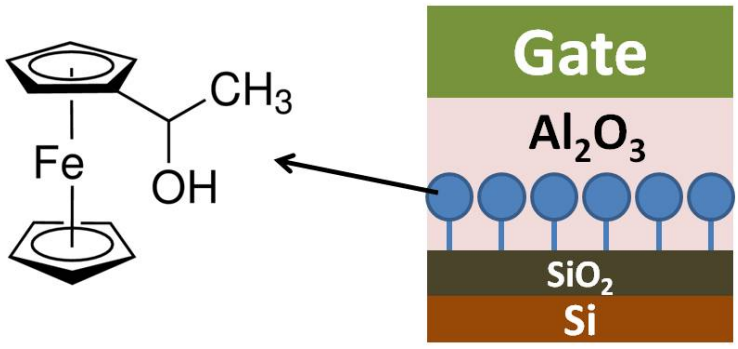

Fig. 4.1 Molecule structure of α-Ferrocenylethanol and schematic of MAFOS capacitor structure

We have fabricated and measured non-volatile memory cells with a metal-Al_2O_3-ferrocene-SiO_2-silicon (MAFOS) structure incorporating a ferrocene SAM on SiO_2. Fig.

4.1 shows the structure of the α-Ferrocenylethanol molecule, and a schematic of the MAFOS structure. The most important fabrication process steps are the attachment of the molecules on SiO_2 and the formation of Al_2O_3 encapsulating the molecules. First, SiO_2 (110 nm) was thermally grown on p-Si substrate followed by the definition of square-shaped active areas (100 μm wide) using photolithography and wet etching. Next, a thin SiO_2 (1.5 nm) was grown on Si in the active area by rapid thermal oxidation at 850 ^oC for 2 min. The molecules were then self-assembled on the SiO_2 by immersing the wafer into a solution of 3 mM α-Ferrocenylethanol in dichloromethane (DCM) at 100 ^oC in a N_2 environment for 20 min. During the attachment process, redox molecules are covalently bonded to the SiO_2 surface through the –OH linker. [70] After the attachment of molecules, DCM was used to rinse the wafer to remove any physisorbed residuals on the surface.

As part of the attached samples were to be characterized by cyclic voltammetry (CyV), other device substrates were immediately loaded into the atomic layer deposition (ALD) vacuum chamber to deposit 20 nm Al_2O_3 at 100 ^oC. The ALD uses trimethyl aluminium (TMA) and H_2O as precursors. In order to ascertain whether the molecular SAM survives the ALD process, some test samples with ALD Al_2O_3 covering the molecular layer were measured by X-ray photoelectron spectroscopy (XPS). In the final step, a layer of 80 nm Pd was deposited and patterned on Al_2O_3 as the top gate. We fabricated three additional structures for comparison: Metal/Al_2O_3/ferrocene/Si (MAFS), Metal/Al_2O_3/SiO_2/Si (MAOS), and Metal/Al_2O_3/Si (MAS). For the fabrication of MAFS structure, hydrogen-terminated Si (H-Si) surface is obtained by dipping the wafers into 2%

hydrofluoric acid for 30 s. The molecular attachment on the H-Si surface was achieved similarly as on the SiO_2 surface.

4.2.2 Molecule Attachment Characterizations

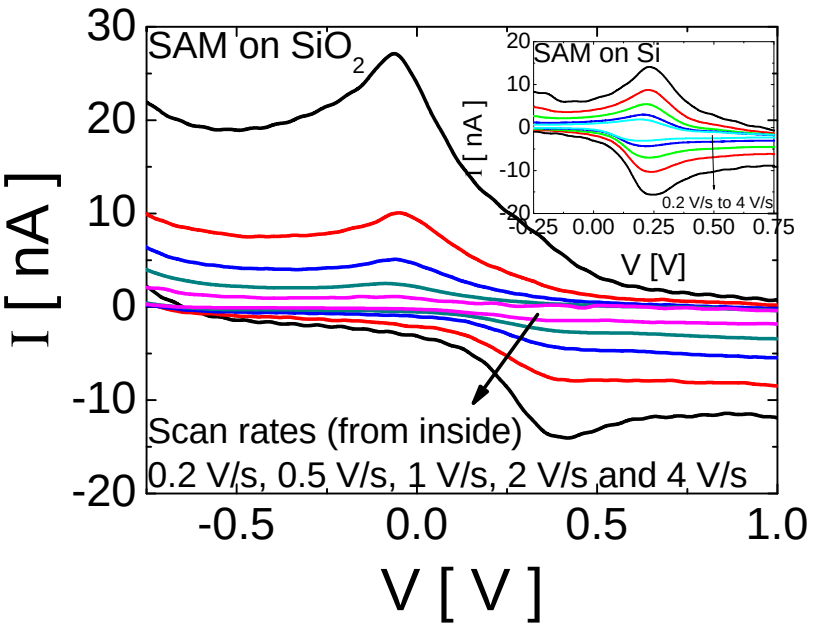

Fig. 4.2 CyV of the EMOS capacitor at different scan rates. Inset: CyV of the EMS capacitor at the same scan rates.

In order to monitor the attachment quality, we used CyV to measure the molecule surface density of some device substrates. For CyV measurement, a solution of 1.0-M tetrabutylammonium hexafluorophosphate (TBAH) in propylene carbonate (PC) was used as the conducting electrolyte. Fig. 4.2 shows the CyV of the electrolyte-molecule-oxide-Si (EMOS) structure with α-Ferrocenylethanol SAM on SiO_2 at various scan rates. Oxidation peaks at negative gate voltage (V_G) and reduction peaks at positive V_G are

observed in the top and bottom curves, respectively. When oxidation (or reduction) voltage is applied, the electrons are removed from (or restored into) the molecular SAM. The inset in Fig. 4.2 shows the CyV measurements of the electrolyte-molecule-Si (EMS) structure with α-Ferrocenylethanol SAM directly attaching onto Si. Oxidation and reduction peaks are also clearly observed, with much smaller peak separation than that of the EMOS structure. The peak separation of EMOS structures increases with increasing scan rate due to the tunneling barrier (1.5 nm SiO_2) and molecular linker between α-Ferrocenylethanol and SiO_2. The redox voltage and peak separation will increase as the thickness of tunneling barrier increases. [64, 153] This provides an opportunity to tune the operation voltage by adjusting the oxide thickness and molecule linker length. The surface coverage of α-Ferrocenylethanol can be calculated from the oxidation peak, and the values are found to be 5.23×10^{13} cm^{-2} and 3.14×10^{13} cm^{-2} for the ferrocene SAM on Si and SiO_2 surface, respectively.

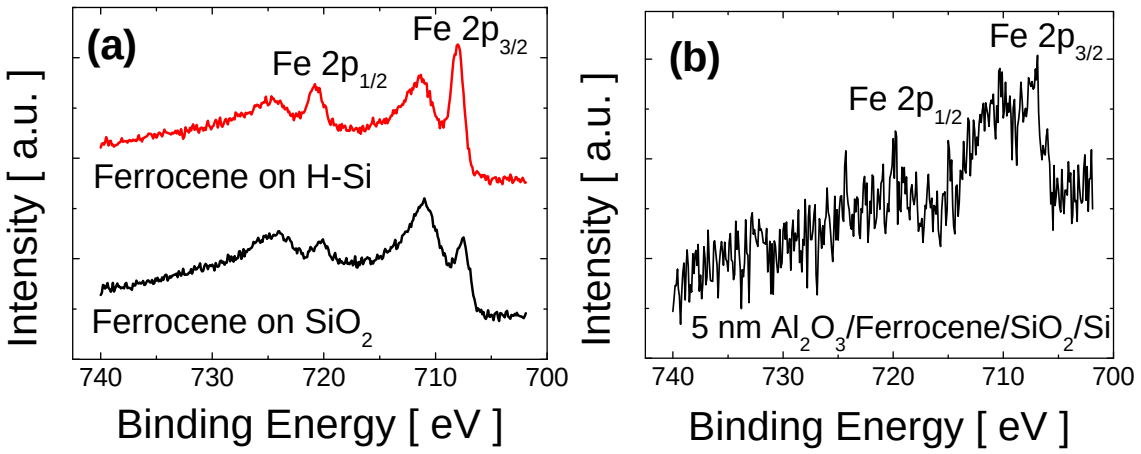

Fig. 4.3 (a) XPS of the samples with ferrocene attached on H-Si and SiO_2 surfaces; (b) XPS of the sample with ferrocene attached on SiO_2 and then covered by 5 nm Al_2O_3.

XPS measurements were performed on the samples with α-Ferrocenylethanol SAM on the SiO_2 and Si surfaces, and the sample with thinner ALD Al_2O_3 (5 nm) covering the SAM on SiO_2. As shown in Fig. 4.3, Fe 2p peaks were clearly observed in all samples. This indicates that the α-Ferrocenylethanol SAM successfully attaches on both SiO_2 and Si surfaces, and the SAM survives the deposition of Al_2O_3. This agrees with the previously reported results that Al_2O_3 could be deposited on SAMs with hydrophilic end groups by using TMA and H_2O vapor as precursors at relatively low temperature. [70, 154] As the thickness of Al_2O_3 increases (to 20 nm), the Fe 2p peak is no longer detected at the surface as a result of forming a thick and closed Al_2O_3 layer.

4.2.3 P/E Operation Characterizations and Discussion

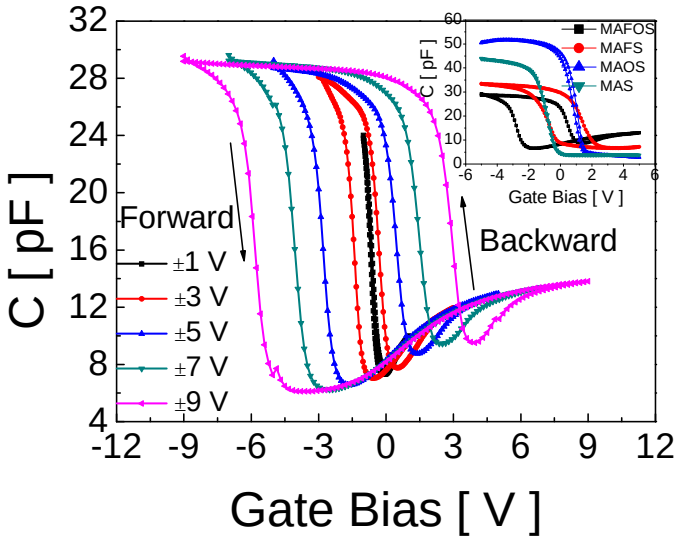

Fig. 4.4 C-V hysteresis curves of the MAFOS device at 1MHz with different V_G sweep ranges: ±1 V, ±3 V, ±5 V, ±7 V, and ±9 V. Counterclockwise hysteresis loops indicated by the arrow were clearly shown. Inset: Hysteresis of MAFOS and three control samples with gate voltage sweep ranges of ±5 V.

The behavior of the molecular memory is measured by capacitance-voltage (C-V) hysteresis at 1 MHz. As shown in Fig. 4.4, a large memory window (≈ 9 V) was observed with the V_G of MAFOS device being swept between 9 V and – 9 V. The memory window is defined as the flat-band voltage (V_{FB}) difference between oxidation and reduction C-V curves. The counterclockwise hysteresis loop is due to the charge storage in the α-Ferrocenylethanol SAM: electrons tunnel out of the molecules to Si at negative V_G (*i.e.*, oxidation) and tunnel back into the molecules at positive V_G (*i.e.*, reduction). The large memory window indicates high density of available charge storage centers, which is attractive for memory applications. The C-V hysteresis curves of MAFOS and three control structures are compared in the inset in Fig. 4.4, where the difference between the samples with and without α-Ferrocenylethanol SAM is clearly observed.

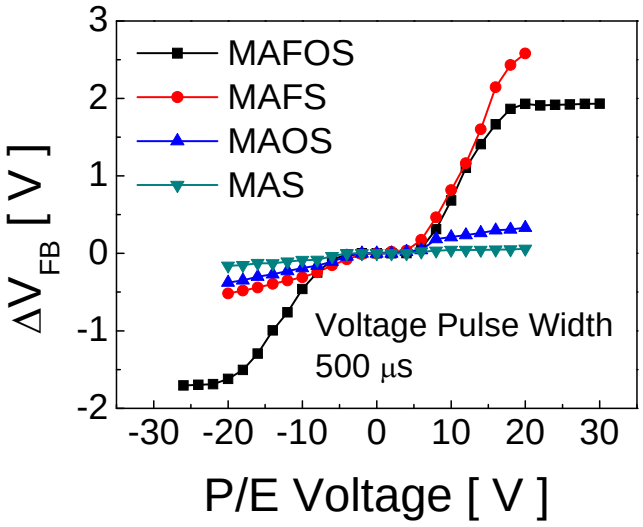

Fig. 4.5 ΔV_{FB} of MAFOS and three control samples as a function of P/E voltage with 500 μs pulse width

Fig. 4.5 shows the flat-band voltage shift (ΔV_{FB}) of the four structures as a function of applied P/E voltages (500 μs square pulse). We define positive (or negative) ΔV_{FB} at positive (or negative) V_G as programming (or erasing) operation, corresponding to electron gain (or loss) in α-Ferrocenylethanol SAM, corresponding to reduction and oxidation of the molecules, respectively. Usually, the interface traps in the Al_2O_3 will also cause charge storage, inducing a ΔV_{FB}. As shown in Fig. 4.5, the ΔV_{FB} of MAOS and MAS devices is much smaller than that of MAFOS and MAFS devices, indicating that the contribution of interface traps in the Al_2O_3 is insignificant. MAFOS devices exhibit a symmetric, staircase curve of ΔV_{FB} vs. P/E voltage, which is not observed in MAFS devices. This is a result of the effective charge separation by SiO_2 tunneling barrier. The MAFS sample shows a larger ΔV_{FB} during program process due to the higher molecular coverage on the Si and thinner tunnel barrier (no SiO_2). But for the erase process (oxidation), it showed much smaller ΔV_{FB} compared to MAFOS devices, indicating that the absence of the SiO_2 tunnel barrier increases difficulty of maintaining molecules positively charged. The staircase ΔV_{FB} of MAFOS devices is caused by the charging / discharging balance in the α-Ferrocenylethanol SAM at this P/E condition (V_G = ± 20 V, pulse width = 500 μs). We can calculate the charge density in the SAM at this P/E condition by using the following equation:

$$\Delta V_{FB} = \frac{e \cdot n}{C} = e \cdot n \cdot \left(\frac{T_{Al_2O_3}}{\varepsilon_0 \varepsilon_{Al_2O_3}} \right)$$

where e is elementary charge, n is the number of stored (or missing) electrons, $T_{Al_2O_3}$ and $\varepsilon_{Al_2O_3}$ are thickness and dielectric constant (≈ 9) of Al_2O_3 layer. We neglect the contribution of molecular component (< 0.5 nm) between the redox center and SiO_2 as it is much shorter than the Al_2O_3 (20 nm). With ΔV_{FB} = 1.93 V, the effective charge density is calculated as 4.82×10^{12} cm^{-2}. Compared to the surface coverage of molecules obtained from the CyV measurements, only 15% of the molecules are positively charged (*i.e.*, oxidized). This indicates that effective memory can be realized even with a partial (*i.e.*, non-continuous) α-Ferrocenylethanol SAM.

Fig. 4.6 shows the programming and erasing operations of the MAFOS and MAFS device. After applying 10 V pulses with different width, which corresponds to the programming operation, C-V curves were subsequently swept from positive to negative to study electron injection; while -10 V erasing pulses were applied, followed by sweeping C-V curves from negative to positive to study the hole injection. The high-frequency (1 MHz) C-V curves in Fig. 4.6 demonstrate that MAFOS device shows obvious ΔV_{FB} with 10 V, 10 μs programming pulse and -10 V, 1 μs erasing pulse; MAFS device shows fast programming speed but poor erasing behavior.

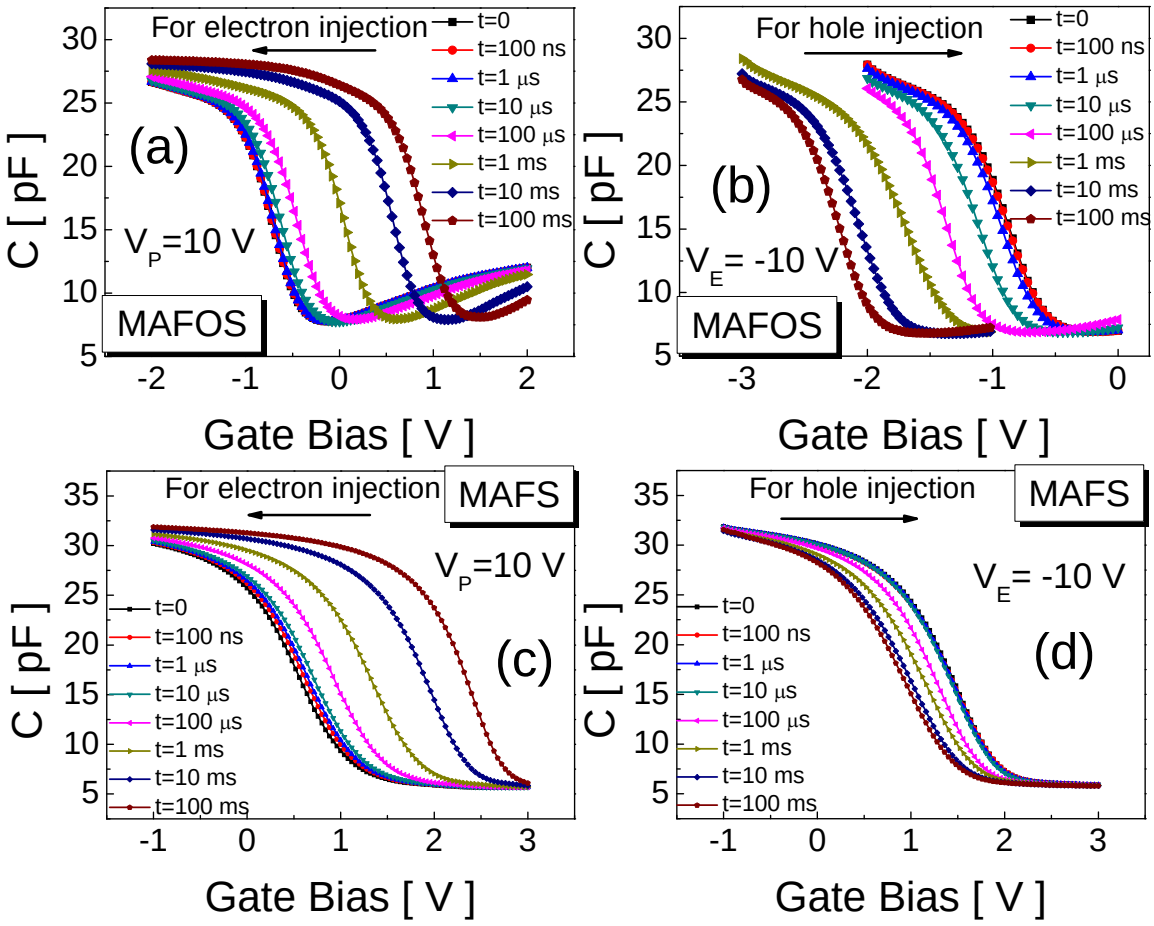

Fig. 4.6 Programming and erasing operations on (a) - (b) MAFOS and (c) - (d) MAFS devices. The P/E voltage pulse is ±10 V, with different pulse width. The arrows indicate sweeping directions: for programming, gate bias was swept from positive to negative; for erasing, gate bias was swept from negative to positive.

Fig. 4.7 compares the P/E speeds of the MAFOS and MAFS devices. The MAFOS memory devices exhibit excellent P/E speed in both program and erase operations. Significant ΔV_{FB} can be achieved by a short pulse (1 μs) at V_G = 10 V. For comparison, MAFS devices have similarly good program speed but not as good erase speed, indicating that it is more difficult for the SAM on Si to stay positively charged without the isolation layer (SiO_2), in agreement with the above discussion.

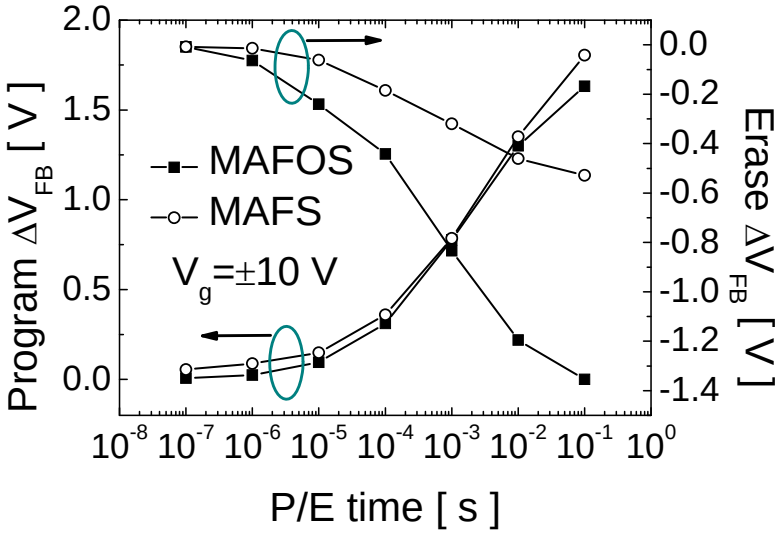

Fig. 4.7 P/E speed characterizations of MAFOS and MAFS with P/E voltage = ±10 V

4.2.4 Retention and Endurance

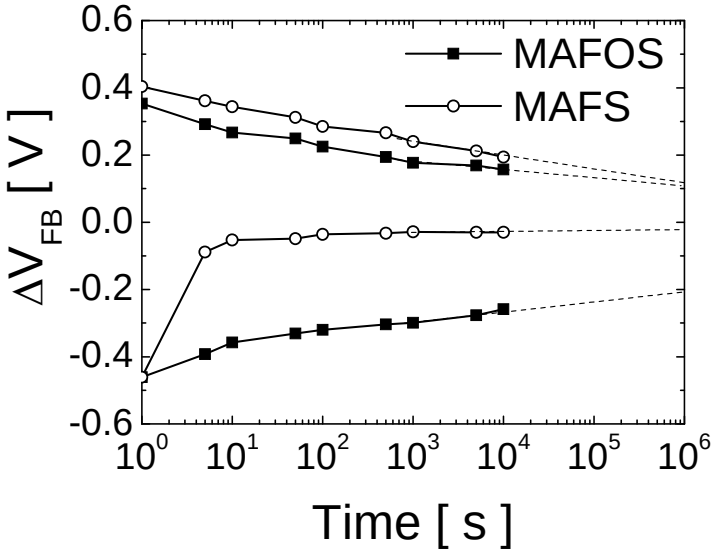

Fig. 4.8 Retention of MAFOS and MAFS devices at room temperature

Fig. 4.8 shows the retention characteristics of both MAFOS and MAFS devices at room temperature. For retention measurement, the MAFOS devices were programmed/erased at V_G = ±10 V for 100 μs; and the MAFS devices were programmed at V_G = 10 V for 100 μs, and erased at V_G = -10 V for 10 ms to obtain enough initial erasing ΔV_{FB}. The projected memory window of MAFOS device for retention time = 10^6 s is about 0.32 V, which is still good for non-volatile memory application. Compared to the initial memory window (≈ 0.81 V), about 60% charge is lost, mainly due to the thin SiO_2 layer. The retention of MAFS device is worse. In this work, thin SiO_2 layer was used in MAFOS devices in order to improve P/E speed and endurance at low V_G. Although the retention decreases, the non-volatile memory cells will have fast P/E speed and much better P/E endurance for on-chip memory application.

As shown in Fig. 4.9(a), the endurance characteristics of MAFOS and MAFS devices were measured and compared with P/E operations at V_G = ±10 V for 500 μs. The MAFS devices fail after 10^7 P/E cycles, while the MAFOS devices show only negligible degradation in ΔV_{FB} after 10^8 P/E cycles, indicating that the SiO_2 tunneling barrier plays an important role. Fig. 4.9(b) shows the endurance of MAFOS devices at shorter P/E pulses. The devices continue to behave well after 10^9 P/E cycles: the memory window remains the same and the ΔV_{FB} of P/E shows a slight up-shift (more positive). This slight up-shift is due to the accumulation of electron in deep traps. [139, 155] This problem can be solved by eliminating the interface traps via annealing the devices in NH_3. [156] For comparison, conventional Flash memory devices based on poly-Si endure only 10^5 P/E cycles. Since the only difference between our device and conventional Flash memory is

replacing poly-Si with α-Ferrocenylethanol molecules, we can conclude that such excellent endurance characteristics are naturally derived from the intrinsic redox properties of the α-Ferrocenylethanol molecules. In addition, good gate stack interfaces are very important to preserve the intrinsic properties of redox molecules. We have paid a great deal of attention on engineering the integration of molecules and dielectrics that encapsulate the molecules. The excellent endurance obtained shows that the device fabrication successfully protects the redox molecules.

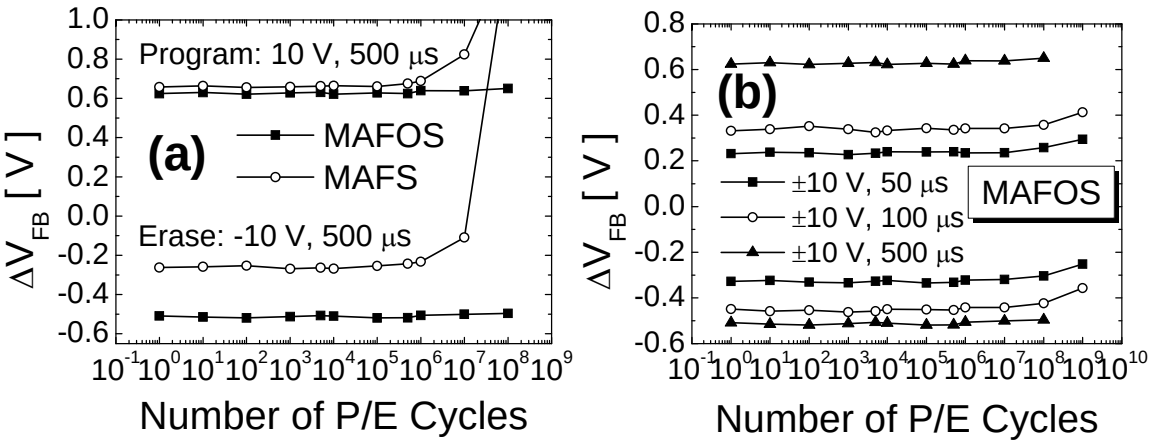

Fig. 4.9 (a) Endurance characteristics of MAFOS and MAFS devices under P/E pulses of V_G = ±10 V for 500 μs; (b) Endurance of MAFOS under P/E voltage = ±10 V with different pulse width: 50 μs, 100 μs, and 500 μs.

Our group previously showed that the charge-trapping Flash memory devices can be programmed and erased within 1 ns by carefully designed tunneling barrier and channel structure. [45] The Flash memory will have both fast P/E speed and excellent endurance when the charge-storage layer is replaced with redox-active Ferrocene molecules. This new type of molecular non-volatile memory will be very attractive for

next-generation memory application, especially for the application in embedded or stand-alone memory.

4.2.5 Summary

In summary, we have fabricated solid-state Si-molecular hybrid structures with α-Ferrocenylethanol SAM encapsulated in the gate dielectrics for memory application. These Si-molecular structures exhibit excellent program and erase characteristics for non-volatile memory application. The endurance of MAFOS devices is about 10,000 times better than that of the conventional floating-gate memory (1×10^5 P/E cycles). This is a significant breakthrough in the quest of charge-storage non-volatile memory and will enable the application of Flash-like devices for future on-chip memory application.

4.3 Multiple Redox Center Molecule for Multi-Bit Non-Volatile Memory

In order to obtain multi-bit storage in molecular non-volatile memory unit cell, a redox-active molecule with two or more redox states will be utilized. Fig. 4.10 demonstrates the structure of the $Ru_2(ap)_4C_2C_6H_4P(O)(OH)_2$ redox molecule with two Ru redox centers. The phosphonic tether on this $(Ru)_2$ redox molecule is designed for the attachment on SiO_2 surfaces. The two redox centers in this $(Ru)_2$ molecules can exhibit stable and distinct charged states at distinct voltage level, enabling multiple-state memory.

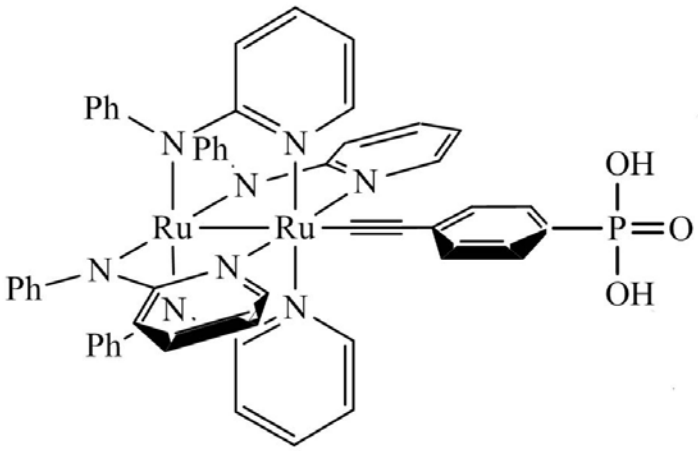

Fig. 4.10 Molecule structure of $Ru_2(ap)_4C_2C_6H_4P(O)(OH)_2$

4.3.1 Attachment methods

The same solvent – DCM as that for ferrocene molecule attachment was used to dissolve the $(Ru)_2$ redox molecule. The attachment on SiO_2 surfaces was carried out in a glovebox with inert environment of N_2. By dropping droplets of the top clear molecular solution on the active areas with each drop being placed for 5 min, a saturated SAM was formed with 8 solution droplets. The sample was kept at the temperature of 100 ^{o}C during the attachment process.

After the SAM was formed, DCM was used to rinse the attached sample to remove any un-bonded residuals on the surface for two to three cycles of sonication with 1 min each.

4.3.2 Attachment Characterizations

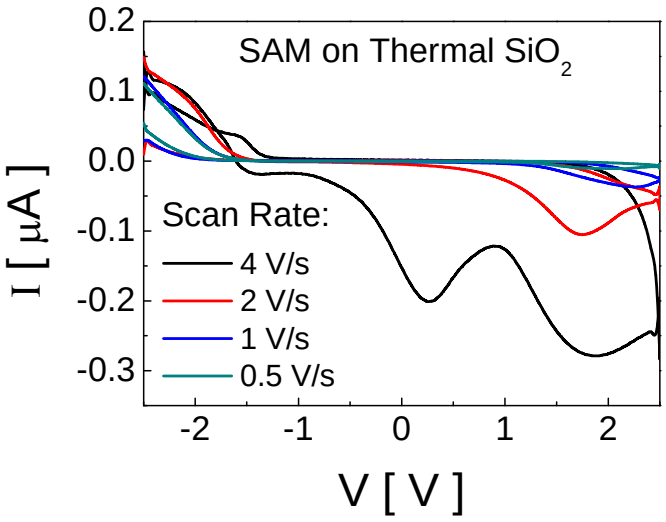

Fig. 4.11 CyV of the EMOS capacitor with $(Ru)_2$ redox molecules attached on SiO_2 surfaces at different scan rates

CyV measurements were performed on the $(Ru)_2$ attached electrolyte-molecule-SiO_2-Si (EMOS) capacitors fabricated on lightly-doped Si (100) wafers. The CyV curves are shown in Fig. 4.11. As expected, two reduction peaks were observed at positive gate voltage region, due to the two distinct redox centers in $(Ru)_2$ molecules. However, the oxidation peaks are absent even at scan rate as high as 4 V/s. This is due to the relatively large molecule weight of $(Ru)_2$ (or molecule volume more precisely), which makes the kinetic rate slower. Under voltage scan rates applied in our work, the charges in the redox centers will need more time to move into the Si substrate, leading to the absence of the oxidation peaks at negative gate voltage region. Nevertheless, the CyV results have positively confirmed the attachment of $(Ru)_2$ molecules on SiO_2 surfaces.

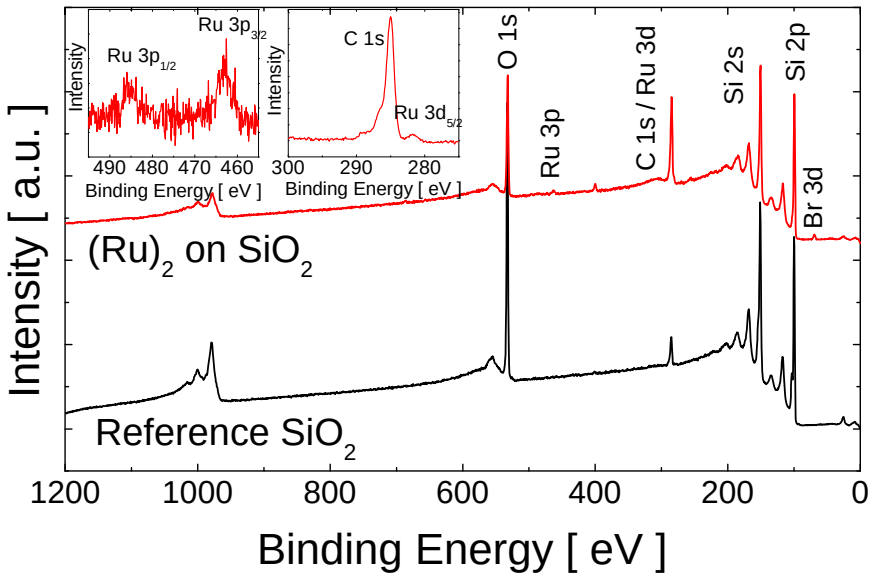

Fig. 4.12 XPS of the sample with $(Ru)_2$ molecules attached on SiO_2 and a SiO_2 reference sample

We also performed the XPS measurements on the $(Ru)_2$ attached SiO_2 sample. As shown in Fig. 4.12, Ru 3p and Ru 3d peaks were clearly observed in the attached sample, and from the contrast between the Ru peaks and C 1s peaks, we can confirm that the $(Ru)_2$ molecules have been successfully attached on SiO_2 surfaces by forming a uniform monolayer. Further XPS characterizations on the $(Ru)_2$ attached samples with a thin layer of ALD Al_2O_3 covering the molecule layer are currently under study, to ensure that the attached $(Ru)_2$ molecules can survive the ALD process, and can still function perfectly in solid-state molecular memory devices.

4.3.3 In-Progress Molecular Memory Device Fabrication

We are currently working on the fabrication and characterization of the planar molecular non-volatile memory cell with $(Ru)_2$ molecules as the charge trapping medium.

Similarly, the $(Ru)_2$ molecules will be attached on the tunneling oxide and embedded in a high-*k* dielectric (Al_2O_3 preferred). By the gate voltage control, the two redox centers in $(Ru)_2$ molecules can charge and discharge at discrete voltage levels, enabling a multi-bit memory storage in a unit cell. Such a molecular non-volatile memory combining the advantageous properties of redox molecules and multi-bit memory storage will be very attractive for novel non-volatile memory applications with fast speed, low power, high density, and excellent reliability.

4.4 SiNW FET Based Ferrocene Molecular Flash Non-Volatile Memory

Integration of the redox molecules in the semiconductor FET technique to realize a solid-state molecular Flash memory will not only enhance the memory performance and device reliability but also allow us to use regular electronics characterization metrologies to measure the charge storage of redox molecules, compared to the usual way involving liquid electrolyte. In our work, we demonstrate a CMOS-compatible self-aligned SiNW FET based molecular Flash memory. SAM of ferrocene redox molecules is formed on the SiNW with easy and cheap method. Memory behavior of the molecular structure has been systematically characterized. Such molecular Flash memory shows fast P/E speed, excellent reliability, and can offer sufficient charge trapping density.

4.4.1 Experimental Details

Our ferrocene-attached SiNW FET molecular Flash memory was built by following the self-alignment method described previously. Typically, a 300 nm SiO_2 was

first grown on a highly doped p-type Si (100) wafer by dry oxidization. Then a thin film of Au catalyst (2 nm to 4 nm) was deposited on patterned area pre-defined by photolithography. Then the Si nanowires were grown from the Au catalyst in a low-pressure chemical vapor deposition (LPCVD) furnace at 440 ^{o}C for 2 h with an ambient SiH_4 stream under a pressure of 500 mTorr. The Si nanowires growth followed the vapor-liquid-solid (VLS) mechanism, with typical length of 20 μm and 20 nm in diameter. Immediately after the growth step, the Si nanowires were oxidized at 750 ^{o}C for 30 min to form a ~ 3 nm SiO_2 on which the α-Ferrocenylethanol SAM will be formed subsequently. This thin layer of SiO_2 was also expected to provide a good interface between the SiNW and the Al_2O_3-based gate dielectric which was completed after the SAM was formed. The next step was to pattern the source/drain (S/D) electrodes with photolithography. A 2% HF wet etching was applied to remove the oxide from the Si nanowire at patterned S/D area immediately before the 5/100 (unit: nm) Ti/Pt was deposited by E-beam evaporation and lift-off process to form the Schottky barrier S/D contacts. The channel length between the S/D electrodes was controlled to be 5 μm. The ferrocene SAM on the SiO_2 surface was prepared by placing droplets of a solution of dichloromethane (DCM) with 3-mM ferrocene on active areas with each drop being placed for 4-5 minutes. The sample was held at 100 ^{o}C in an N_2 environment during the attachment process. A saturated SAM was formed after 8 droplets in about 30 minutes, and the redox molecules were linked to the SiO_2 surface through the –OH terminal. After the self-assembly process, DCM was used to rinse the wafer in order to remove any residual molecules that are not bonded to the SiO_2 surface. Then, the samples were

immediately loaded into the ALD chamber. A layer of 25 nm Al_2O_3 was deposited with TMA and H_2O as precursors at 100 ^oC. Finally, a 100 nm Pd top gate electrode was formed with the similar photolithographic and lift-off processes as S/D electrodes. The schematic structure of a completed molecular memory device is shown in Fig. 4.13. A reference sample without redox molecules was fabricated at the same time for comparison.

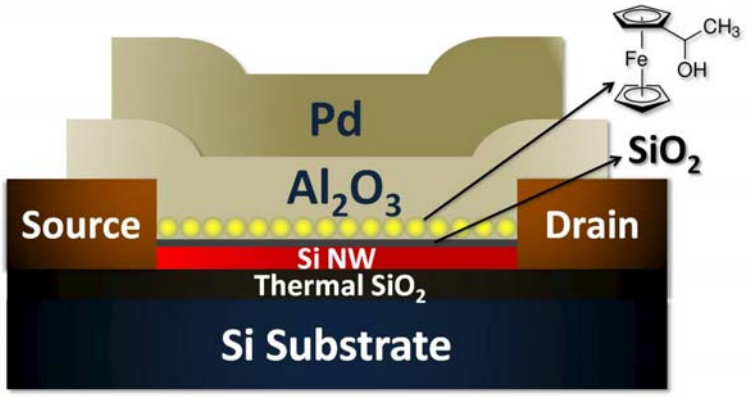

Fig. 4.13 Schematic of a completed ferrocene-attached molecular Flash memory

The technology to fabricate FETs based on CVD grown nanowires or electronic circuits is still under intensive study. The self-alignment fabrication process used in this work is attractive compared to regular nanowire harvesting and manipulation processes as it effectively limits the fabrication steps in which the nanowires can be contaminated, and enables simultaneous batch fabrication of high quality, reproducible, and homogeneous nanowire devices at the wafer scale.

4.4.2 Memory Performance and P/E operation Characterizations

In previous section, we have characterized the attachment of ferrocene on SiO_2 surface with CyV and XPS measurements, showing that the molecule coverage density is 3.14×10^{13} cm^{-2}, and the molecules can survive in the subsequent Al_2O_3 deposition process. The molecular Flash memory based on SiNW FET with ferrocene molecules embedded in Al_2O_3 dielectric can be expected to inherit the excellent intrinsic properties derived from the redox molecules.

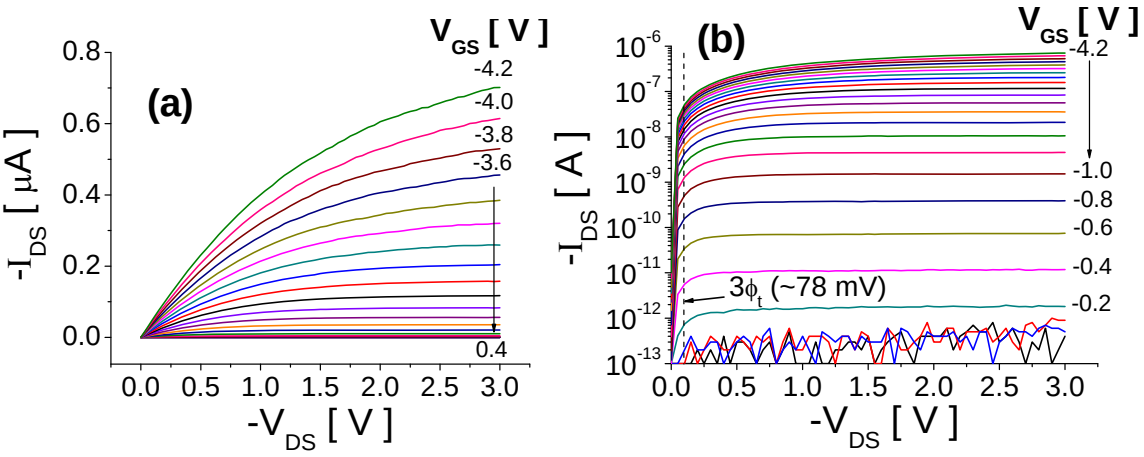

Fig. 4.14 (a) Output characteristics of ferrocene molecular Flash memory with V_{GS} varies from 0.4 V to -4.2 V, with step of -0.2 V; (b) Log-scale output characteristics, with leakage-affected region, weak, moderate, and strong inversion regions clearly shown.

Due to the Schottky contacts between the S/D electrodes and the intrinsic SiNW, Schottky-barrier p-type MOSFET characteristics are expected for the ferrocene-attached SiNW FET devices. Fig. 4.14 shows the output characteristics of the molecular FET devices in both linear and logarithmic scale. Smooth, well saturated I_{DS}-V_{DS} (source-drain current vs. source-drain voltage) curves with negligible contact resistance have been

obtained. The leakage-affected region, weak, moderate, and strong inversion operation regions are clearly shown in Fig. 4.14(b). In the weak inversion region, the drain current increases exponentially with V_{GS} and is saturated at $3\phi_t$ (≈ 78 mV at room temperature), where ϕ_t is thermal voltage, indicating the molecular memory device functions as an ideal conventional MOSFET.

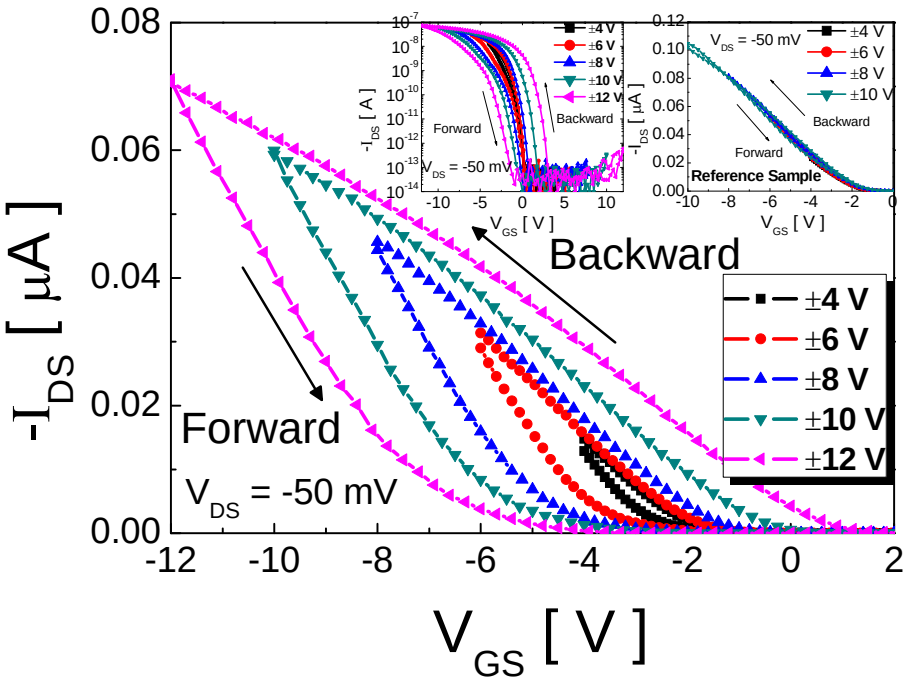

Fig. 4.15 Transfer characteristics of ferrocene molecular Flash memory, with clearly shown counterclockwise hysteresis loops corresponding to gate voltage sweep ranges of ±4 V, ± 6 V, ± 8 V, ± 10 V, and ± 12 V, respectively. The arrows indicate the directions. V_{DS} was set to -50 mV. Inset: (i) transfer characteristics of the molecular memory device in log-scale; (ii) I_{DS}-V_{GS} hysteresis loops of the reference sample with the same gate voltage sweep ranges.

Typical transfer characteristics I_{DS}-V_{GS} (source-drain current vs. gate voltage) of the molecular memory are shown in Fig. 4.15. Counterclockwise hysteresis loops were observed at different gate voltage sweep ranges, indicating the charge storage between

the molecules and SiNW channel. The memory window starts to appear at gate voltage as low as 4 V. The log-scale of the transfer characteristics of the molecular Flash memory are shown in the inset (i) in Fig. 4.15. Clear Off state was observed, and the On/Off ratio is as high as ~ 10^7. The inset (ii) of Fig. 4.15 shows the I_{DS}-V_{GS} curves of the reference sample at the same V_{GS} sweep ranges. Negligible memory window was observed on the reference sample, ruling out the doubt of charge storage in Al_2O_3 layer. This indicates that the molecules play a key role in the charge storage of the memory devices.

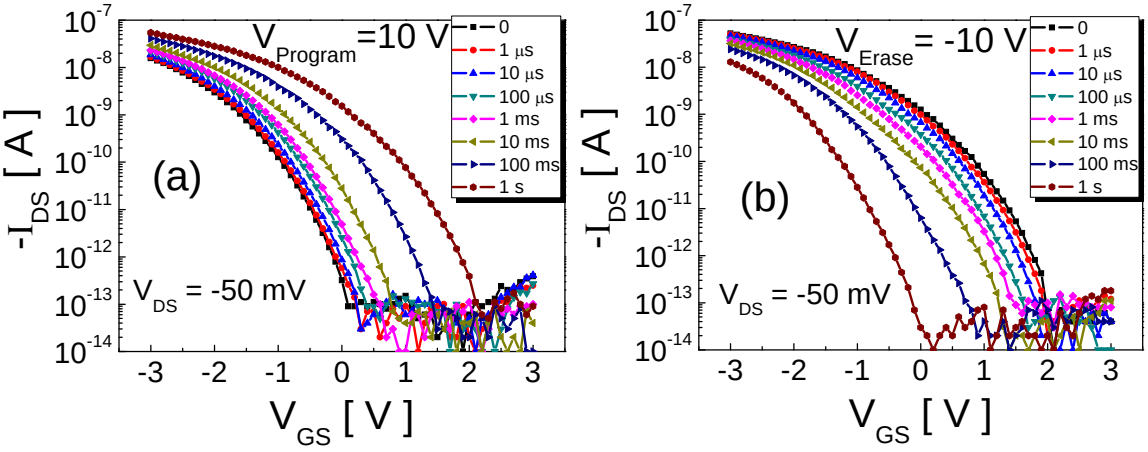

Fig. 4.16 (a) Programming and (b) erasing operations of the ferrocene molecular Flash memory under accumulative rectangular P/E gate voltage pulses. The gate voltage was set to ±10 V respectively with increasing pulse width.

Fig. 4.16(a) and 4.16(b) show the memory device programming and erasing characteristics demonstrated by the threshold voltage shift (ΔV_{Th}) under different P/E gate voltage pulses. The P/E operations were performed by applying gate voltage rectangular pulses while the source and drain electrodes were both grounded. As shown in Fig. 4.16(a), I_{DS}-V_{GS} curves are swept after applying +10 V programming gate voltage

pulses with increasing pulse width. The threshold voltage shows a clear shift toward the positive direction, indicating the electrons are injected from the SiNW through the SiO_2 and stored in the redox centers in the ferrocene molecules. Subsequently, V_{GS} = -10 V with increasing pulse width was applied, corresponding to the erasing operations, followed by I_{DS}-V_{GS} sweepings. The back shift of the threshold voltage toward the negative direction suggests the hole injection from the SiNW during the erasing operations.

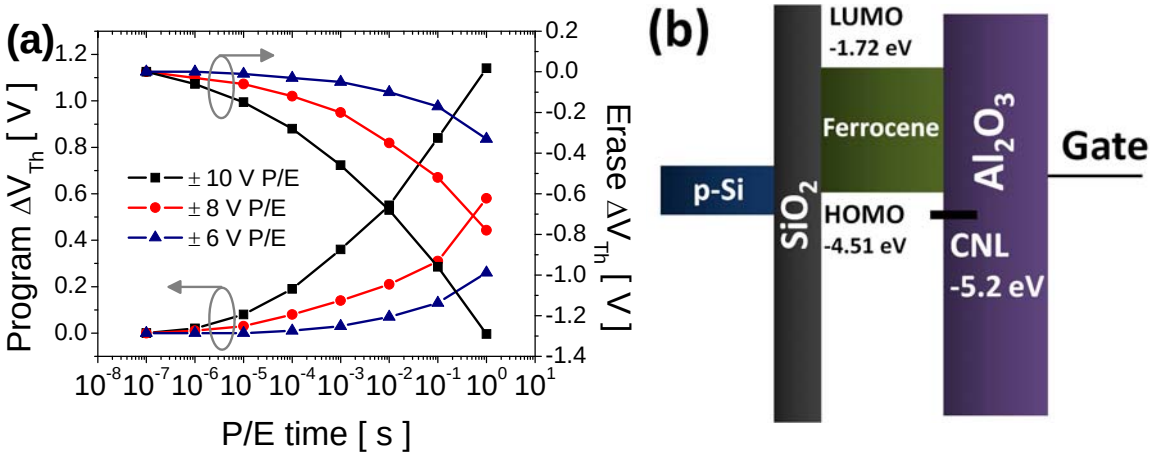

Fig. 4.17 (a) P/E speed characterization of ferrocene molecular Flash memory; (b) Schematic band diagram of the p-Si/SiO_2/ferrocene/Al_2O_3/gate system.

The P/E speed characterizations of the ferrocene molecular Flash memory are summarized in Fig. 4.17(a), with ±6 V, ±8 V, and ±10 V P/E gate voltages, respectively. This molecular memory shows fast P/E speed, which arises from the intrinsic fast speed charging and discharging of ferrocene molecule. As shown in Fig. 4.17(a), the device shows a clear ΔV_{Th} with a +10 V, 10 µs programming gate voltage, but for the erasing

operation, a -10 V, 10 μs erasing gate voltage shifts the V_{Th} more significantly. We attribute the faster erasing speed, *i.e.* more favorable hole injection, in the Si/SiO_2/ferrocene/Al_2O_3/gate system to the charging at the ferrocene/Al_2O_3 interface states. Apart from the possible Al_2O_3 dielectric traps which have been ruled out from above discussion, the injected electrons and holes can be stored at the redox centers of the ferrocene molecule and the possible ferrocene/Al_2O_3 interface traps, which might be due to the natural property of the molecule and dielectric, or might be introduced during the SAM forming process. [70, 157] Fig. 4.17(b) shows the schematic band diagram of the Si/SiO_2/ferrocene/Al_2O_3/gate structure. The highest occupied molecular orbital (HOMO) / lowest unoccupied molecular orbital (LUMO) for ferrocene are calculated by density functional theory (DFT) to be -4.51 eV / -1.72 eV, and the charge neutrality level (CNL) of Al_2O_3 deposited by ALD is -5.2 eV, which can be taken as a local Fermi level of the interface states. [158-160] For electron injection, the extra energy for electrons to get injected into ferrocene LUMO is $E_{LUMO} - E_C$ = 2.28 eV, where E_C is the Si conduction band edge. The injected electrons will be relaxed into interface states surrounding the CNL due to the lower energy level. On the other hand, the extra energy for holes to be injected into ferrocene HOMO is $E_V - E_{HOMO}$ = -0.59 eV, where E_V is the Si valance band edge. Therefore, hole injection is more favorable than electron injection from the standpoint of storage in the interface states.

The charge storage in the interface states can also be derived from the transfer characteristics in programming and erasing operations. The subthreshold slope (S) of the

molecular memory after each programming and erasing operation can be estimated by using the following equation:

$$S = ln10\frac{kT}{q}\left(1 + \frac{C_{ch-gnd} + C_{it}}{C_{ox}}\right)$$

where C_{ch-gnd} is the capacitance between the nanowire channel which is in weak inversion region and ground, C_{it} is the interface state capacitance, C_{ox} is the capacitance of the gate dielectric, respectively. [161] Extracted from the I_{DS}-V_{GS} curves in Fig. 4.16(a) and 4.16(b), the S undergoes a slight increasing during the accumulative programming process from ≈ 368 mV/dec at fresh state to ≈ 389 mV/dec after a +10 V, 1 s gate voltage stressing. The following accumulative erasing operations reversely decreases the S value from ≈ 382 mV/dec at programmed state to ≈ 355 mV/dec after the -10 V, 1 s stressing. By assuming the change in S is due to the interface state charging of electrons and holes during the programming and erasing operations respectively, the ferrocene/Al_2O_3 interface trapped charges only introduce very small amount of charge even by a ±10 V, 1 s voltage stressing as compared with the initial state in the P/E operations. However, this injected interface trapped charges would have impact on the P/E speed at low gate voltage or short P/E time, in which conditions the chargers cannot have sufficient energy or amount to tunnel through barrier formed by the SiO_2 underneath the molecules together with the linker component part of the molecules.

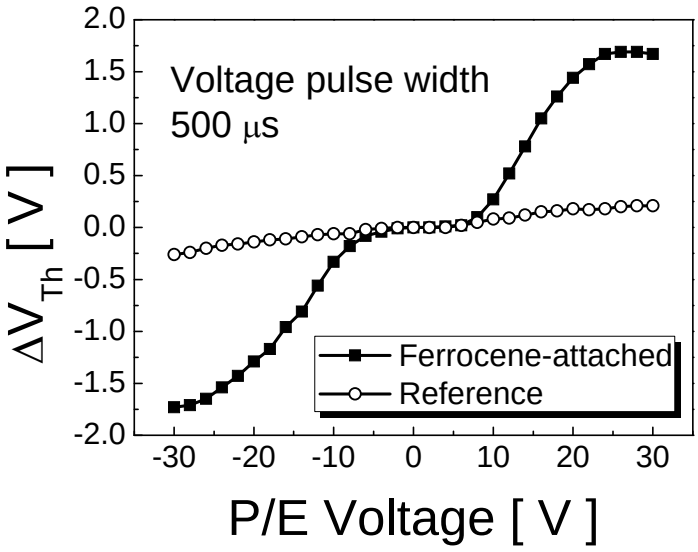

Fig. 4.18 ΔV_{Th} of the molecular memory and reference sample as a function of P/E voltage with 500 μs pulse width and increasing pulse height.

Fig. 4.18 shows the ΔV_{Th} of the ferrocene molecular Flash memory and the reference sample as a function of applied P/E voltages. The P/E pulses width was set to 500 μs. With increasing P/E voltage pulse height, very small ΔV_{Th} was observed for the reference sample, which again proves that the negligible charges are stored in the traps of the Al_2O_3 dielectric or the SiO_2/Al_2O_3 interface. For the ferrocene molecular Flash memory, large ΔV_{Th} and a clear staircase behavior demonstrating discrete energy levels were observed. The hole injection starts to show clear ΔV_{Th} at lower than -6 V gate voltage, while the ≈ 8 V gate voltage is required for electron injection to show a clear ΔV_{Th}. This trace difference of ΔV_{Th} at low gate voltage is partly due to the small amount but more preferred hole storage than electron at the ferrocene/Al_2O_3 interface. With increasing P/E voltages, the ferrocene molecular memory shows larger ΔV_{Th}, indicating the charges are injected and stored in the redox centers of ferrocene. ΔV_{Th} gets saturated

at around ±24 V gate voltages, suggesting that all the available redox centers in the ferrocene SAM attached on the nanowire channel have all been occupied by the chargers. With this saturation condition, we can calculate the charging density in the SAM by using the following equation:

$$\Delta V_{Th} = q \cdot N \cdot \left(\frac{1}{C_T} + \frac{1}{C_{link}}\right) = q \cdot N \cdot \left(\frac{ln\left(\frac{t_{Tout}}{t_{Tin}}\right)}{2\pi\varepsilon_0\varepsilon_T L} + \frac{ln\left(\frac{t_{link-out}}{t_{link-in}}\right)}{2\pi\varepsilon_0\varepsilon_{link} L}\right)$$

where q is the elementary charge, N is the total charge stored in the redox centers, C_T and C_{link} are capacitance of the tunnel oxide and the linker part of ferrocene; t_{Tout}, t_{Tin}, $t_{link-out}$, and $t_{link-in}$ are the distances from the center of SiNW to the outside and inside surfaces of the tunnel oxide layer and the ferrocene linker; ε_T and ε_{link} are dielectric constant of SiO_2 and the ferrocene linker; L is the channel length. With saturated ΔV_{Th} obtained from Fig. 4.18 (≈ 1.69 V) and a presumed ferrocene linker with a length of 0.5 nm and 2.5 dielectric constant, the charge density of the SAM can be calculated by dividing N by the SiO_2/ferrocene interface area. The charge density is around 6.96×10^{12} cm^{-2}, which is at the same level as the results obtained from the capacitor structure. Such a high charge trapping density is very important for fast speed, low power and high integration density of a non-volatile memory aiming at on-chip memory applications.

4.4.3 Retention and Endurance

The room temperature retention properties of the ferrocene molecular Flash memory are illustrated in Fig. 4.19(a). The device was initially programmed / erased by ±10 V gate voltage with 500 μs and 100 μs pulse width, respectively. Good charge

retention characteristics were observed, and projected 10-year memory windows with ~ 20% charge loss were obtained for both states. The good retention is due to the intrinsic redox behavior of ferrocene and the high-quality tunneling oxide with clean dielectric interface formed by using the self-alignment fabrication process. This also provides evidence that the injected charge storage location mainly lies in the redox centers in the molecules instead of the ferrocene/Al_2O_3 interface states, the recovery process of which is quite fast leading to a poor retention.

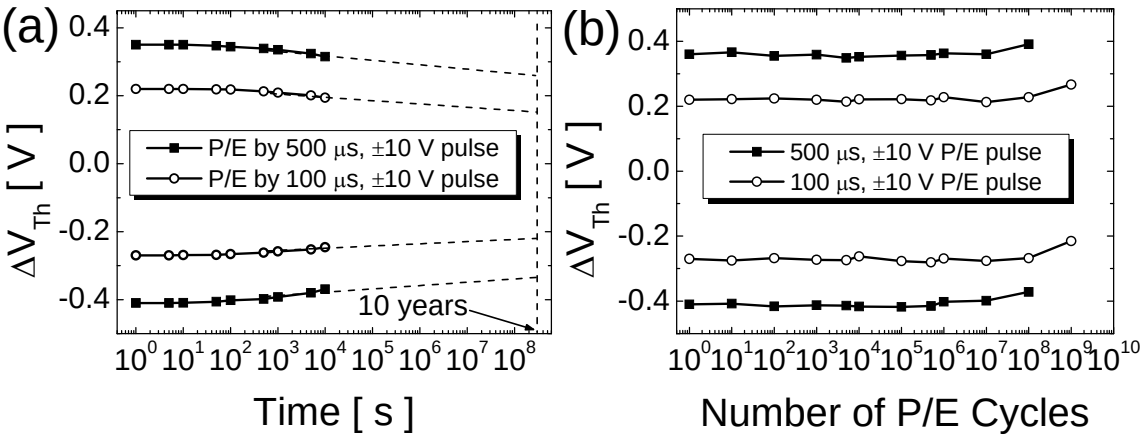

Fig. 4.19 (a) Room temperature retention characteristics of ferrocene molecular Flash memory. The device was initially programmed / erased by ±10 V gate voltage pulses with 500 μs and 100 μs width, respectively; (b) Endurance property of ferrocene molecular Flash memory. ±10 V gate voltage pulses with 500 μs and 100 μs pulse width were applied. Negligible memory window degradation was observed after 10^9 P/E cycles.

The endurance properties of the molecular memory were characterized by applying ±10 V P/E gate voltages with 500 μs and 100 μs pulse width, respectively. Both states show excellent endurance characteristics. Negligible memory window degradation was observed after 10^8 P/E cycles by using 500 μs gate voltages. With 100 μs P/E

voltages, the device still functions perfectly even after 10^9 P/E cycles. Such excellent endurance characteristics arise from the excellent reliability of the intrinsic redox property of ferrocene molecule, which makes such molecular Flash memory very attractive for future non-volatile memory technology.

4.4.4 Summary and Comparison with Capacitor Molecular Memory Devices

In summary, novel ferrocene-attached SiNW FET based molecular Flash memory has been fabricated and studied. Excellent memory performance has been obtained: fast P/E speed, sufficient memory window, good retention, and excellent endurance. Charge storage mechanism has been investigated. The injected chargers are mainly located in the redox centers of ferrocene molecules, with trace amount stored in the ferrocene/Al_2O_3 interface states. Negligible memory window degradation was observed after 10^9 P/E cycles. These excellent characteristics are inherently resulted from both the good intrinsic charging property of redox-active ferrocene molecules and the protection of good device structure obtained by the self-alignment fabrication.

Compared with the capacitor molecular memory with ferrocene SAM as charge storage medium, the molecular Flash memory based on self-aligned SiNW FET demonstrates better data retention due to the thicker tunneling oxide (~ 3 nm). The high quality dielectric and molecule/dielectric interface formed in the self-alignment process is very promising with the modern CMOS and Flash memory scaling. Such a high-performance molecular Flash non-volatile memory is thus very attractive for future on-

chip non-volatile memory applications, and it will enable a series of fast speed and low power mobile electronic devices and systems.

4.5 Comparison between Dielectric and Molecular Non-Volatile Memory

We have designed, fabricated, and investigated capacitor structure and SiNW FET based dielectric and molecular charge-trapping non-volatile memory devices. Both dielectric and molecular Flash memory devices were fabricated by integrating the dielectric and molecular stack as top gate stack in the self-aligned SiNW FETs, maintaining the engineered stack structure and thickness. Thus, it is worth to compare the performance between the dielectric and redox-molecule charge-trapping medium, and the improvement brought by introducing the high-performance SiNW FET platform with nano-scale channel and surrounding gate. Table 4.1 illustrates the memory performance of the dielectric and molecular memory devices in both capacitor and Flash device architecture, including operation voltage, P/E speed, retention, endurance, and so forth.

Table 4.1 Comparison between dielectric and molecular non-volatile memory

	Dielectric Capacitor	Molecular Capacitor	Dielectric Flash	Molecular Flash
Operation voltage	High	Low	Medium	Low
P/E speed	Good	Excellent	Good	Excellent
Retention	> 10 years	~ 10 years	> 10 years	> 10 years
Endurance	$> 10^6$	$> 10^9$	$> 10^7$	$> 10^9$
Charge trapping density	10^{12} cm^{-2}	10^{12} cm^{-2}	10^{12} cm^{-2}	10^{12} cm^{-2}
Fabrication CMOS compatibility	Excellent	Good	Excellent	Good

From the above comparison, we can find out that all of the four types of non-volatile memory show good data retention and sufficient charge trapping density. Employing the high-performance SiNW FET as platform for real Flash memory has greatly enhanced the memory performance in memory density, P/E operation voltage, and device reliability. The self-aligned SiNW FET provides promising approaches to realize concepts of future Flash memory with novel engineered gate stack upon clean, fast, reliable, and low-cost FETs. It paves the way for the novel Flash memory toward the on-chip memory applications.

By comparing the molecular and the dielectric non-volatile memory, it is obvious that the redox-molecule charge-trapping medium is more attractive as they demonstrate lower operation voltage, higher P/E speed, and much better endurance. One of the major drawbacks of molecular Flash memory for large-scale and on-chip memory application is the limited stability in harsh environment such as high temperature and presence of oxygen or water. More delicate CMOS fabrication process is required for integrating redox molecules in CMOS devices and circuits. Nevertheless, further molecular technology will advance both molecular properties with enhanced adaptability to harsh environment and molecular device integration processes. We believe that such molecular Flash with fast speed, low voltage, high reliability, and simple fabrication is still very promising candidate for on-chip non-volatile memory applications.

Chapter 5 Topological Insulator Nanowire Field-Effect Transistors

5.1 Introduction

Topological insulators (TI) are characterized as a new class of materials which have insulating band gaps in the bulk but gapless surface states topologically protected by time-reversal symmetry. Recently discovered three-dimensional (3D) TI materials, such as Bi_2Se_3, Bi_2Te_3 and Sb_2Te_3, have been intensively investigated both theoretically and experimentally. [79, 162] The gapless surface states featuring helical Dirac electrons have been observed by angle-resolved photoemission spectroscopy (ARPES) and scanning tunneling microscopy (STM) techniques. Thin films and nanoribbons of TI show anomalous high-field magnetoresistance, coherent surface transport induced by Aharonov-Bohm interference, and optoelectronic properties due to the spin-polarized surface states. [110, 117, 118]

Bi_2Se_3, a well-known thermoelectric material, is a 3D TI with a bulk band gap of 0.35 eV and a single Dirac cone on the surface. Most current experimental research focuses on the surface states of thin film samples grown by molecular beam epitaxy (MBE) or mechanically exfoliated from bulk material. A few groups have reported modification of the surface conduction of such TI samples by doping, electrical gating or polarized light. [109-111, 113, 163] Yet, up to now, no high-performance microelectric devices based on TIs such as the analog of metal-oxide-semiconductor field-effect

transistors (MOSFETs) have been reported. The MOSFET is the basic building block in complementary metal-oxide-semiconductor (CMOS) technology, the fundamental basis for digital and analog circuits. For conventional CMOS devices, the surface conduction of Si is protected by thermal SiO_2 to optimize its inversion properties for good transistor performance. This is one of the primary reasons why Si is preferred over other semiconductor materials for CMOS technology. For a TI material, the gapless surface state is derived from its inherent material properties, and maintains a robust surface conduction. Therefore the integration of TI as the active conduction channel in MOSFETs is very attractive because it will leverage the advantages afforded by the novel TI materials with the vast infrastructure of current semiconductor technology.

In our work, we fabricated and measured surrounding-gate Bi_2Se_3 nanowire field-effect transistors. [164] The nanowires were grown from Au catalyst and integrated by using a self-alignment technique. The FET current-voltage (I-V) characteristics were measured at different temperatures, exhibiting excellent performance. We have studied the separation of surface metallic conduction from bulk semiconductor conduction with gate electric field at different temperatures. The activation energy of bulk conduction was found to be very close to the band gap of bulk Bi_2Se_3. We have also studied the effective electron mobility and scattering mechanism in the devices.

5.2 Experimental Details

Bi_2Se_3 nanowire FETs were built up on the basis of our self-aligned nanowire FET architecture. The essential steps are as follows: first, a layer of thermal SiO_2 (300

nm) was grown by dry oxidation on a Si wafer. On the top of the wafer, the Bi_2Se_3 nanowires were grown from Au catalyst deposited by sputtering in pre-defined locations. The nanowire growth followed a solid-vapor-solid route. The wafers (with Au) were loaded at the downstream end in a horizontal tube furnace while Bi_2Se_3 source powder was located at the heat center of the furnace. Then the furnace is heated to a temperature in a range of 500 ^oC to 550 ^oC and kept in that temperature for 2 h under a flow of 50 standard cubic centimeters (sccm) Ar as carrier gas. The as-grown Bi_2Se_3 nanowires were about 20 μm in length and 50 nm to 150 nm in diameter. Then 3 nm / 100 nm Ti/Pt source/drain (S/D) electrodes were patterned on the nanowires at the growth location by photolithography, forming Pt/Bi_2Se_3 Schottky junctions at both source and drain. The channel length was defined to be 2 μm. A layer of 30 nm HfO_2 was then deposited at 250 ^oC by atomic layer deposition (ALD) with precursors of Tetrakis(ethylmethylamino)hafnium and water covering the nanowire channel and also part of S/D electrodes. The last step was the formation of a 100 nm Pd top gate by a lift-off process. Unlike the traditional nanowire harvesting and alignment methods, our self-alignment approach not only enables simultaneous batch fabrication of reproducible and homogeneous nanowire devices of high quality, but also limits the contamination of the nanowire during the fabrication process.

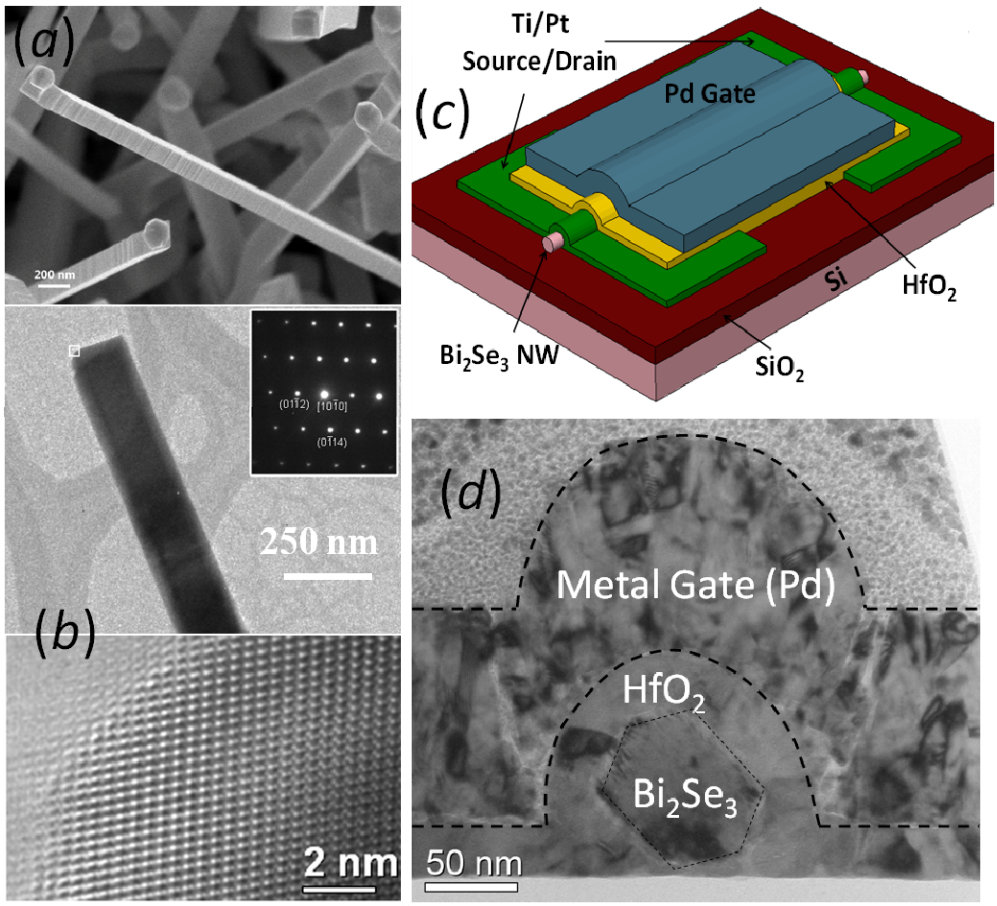

Fig. 5.1 (a) SEM image of Bi_2Se_3 nanowires; (b) HRTEM image of Bi_2Se_3 nanowires showing that the nanowire growth direction is close to$[11\bar{2}0]$, the inset above shows a magnified region of the nanowire; (c) Schematic of a Bi_2Se_3 nanowire FET and (d) TEM image of the cross-section of a Bi_2Se_3 nanowire FET.

Fig. 5.1(a) shows a scanning electron microscopy (SEM) image of the as-synthesized Bi_2Se_3 nanowires which are about 50 nm to 150 nm wide and 10 μm long. Au nanoparticles were found at the top end of each nanowire. This indicates that Bi_2Se_3 vapor is first absorbed by Au catalyst to form a Bi_2Se_3 and Au eutectic; then Bi_2Se_3 diffuses through Au to form the single-crystal nanowires. This process is similar to the growth of Si nanowires governed by vapor-liquid-solid (VLS) mechanism. Bi_2Se_3 has a

layered rhombohedral crystal structure with five covalently bonded atoms in one unit cell. These quintuple layers are linked by van der Waals interactions. The high-resolution transmission electron microscopy (HRTEM) image shown in Fig. 5.1(b) demonstrates that the Bi_2Se_3 nanowires are in a well-defined single-crystal rhombohedral phase and the growth direction is close to $[11\bar{2}0]$. A schematic of the Bi_2Se_3 nanowire FET is shown in Fig. 5.1(c) and a TEM image of the cross-section in Fig. 5.1(d). The hexagonal nanowire core is surrounded first by the insulating HfO_2 layer and then by the Omega-shaped top gate.

5.3 Electrical Characterizations and Discussion

5.3.1 Current-Voltage Characteristics

The electrical characterization was carried out on a probe station inside a vacuum chamber. As shown in Fig. 5.2, the transistor has excellent drain current (I_{DS}) vs. top gate voltage (V_{GS}) transfer characteristics: cutoff current close to zero, strong-inversion-like on-state current and current On/Off ratio larger than 10^8 at a V_{GS} swing of 1.0 V. The backside Si was grounded during all the measurements. The transistor has unipolar current dominated by electron conduction. This is similar to a conventional long-channel Schottky-barrier MOSFET with either electron or hole conduction determined by the unipolar Schottky junctions at the source and drain. No hysteresis was observed in the I_{DS}-V_{GS} curves at 77 K. A hysteresis shift was observed at higher temperatures (T > 240 K), most likely due to the activation of traps in the HfO_2. Very similar device

characteristics were observed for the drain voltage (V_{DS}) in the range 0.05 V - 4.0 V used in the study.

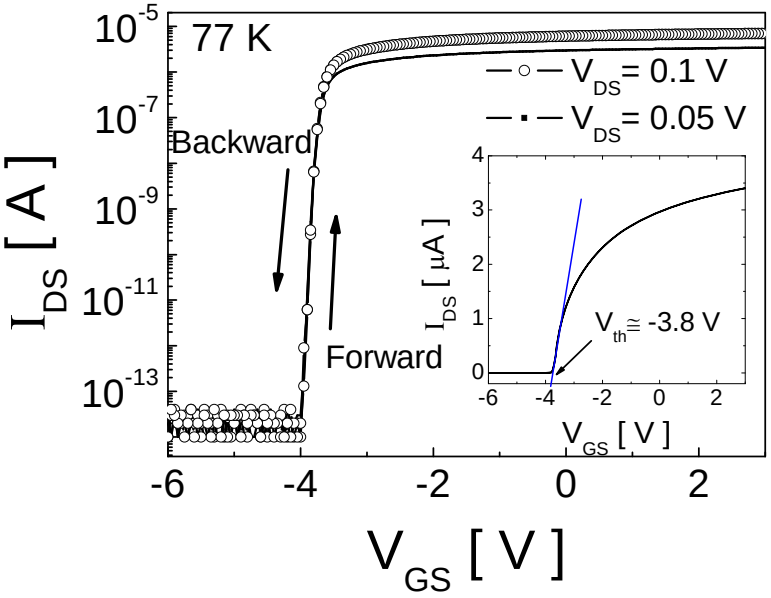

Fig. 5.2 Transfer characteristics (I_{DS}-V_{GS}) of Bi_2Se_3 nanowire FET at 77 K; inset is the linear-scale plot showing V_{th} = -3.8 V.

As shown in Fig. 5.3, the Bi_2Se_3 nanowire FET exhibits well-saturated, smooth I_{DS} vs. V_{DS} curves with negligible contact resistance. The transistor output characteristics clearly demonstrate cutoff, weak, moderate and highly conductive regions at different V_{GS}, similar to the cutoff (leakage), weak, moderate and strong inversion regions of conventional MOSFETs. The I_{DS} saturates roughly at $V_{DS} = V_{GS} - V_{th}$ in the highly conductive region but does not saturate at $V_{DS} \approx 3\,\phi_t$ in the weak/moderate conductive regions ($\phi_t = kT/q$). I_{DS} keeps increasing significantly after $3\phi_t$. This means that the Bi_2Se_3 nanowire FET does not follow the diffusion current model as described for

conventional MOSFETs. We believe I_{DS} in the weak/moderate conductive regions is also dominated by drift current.

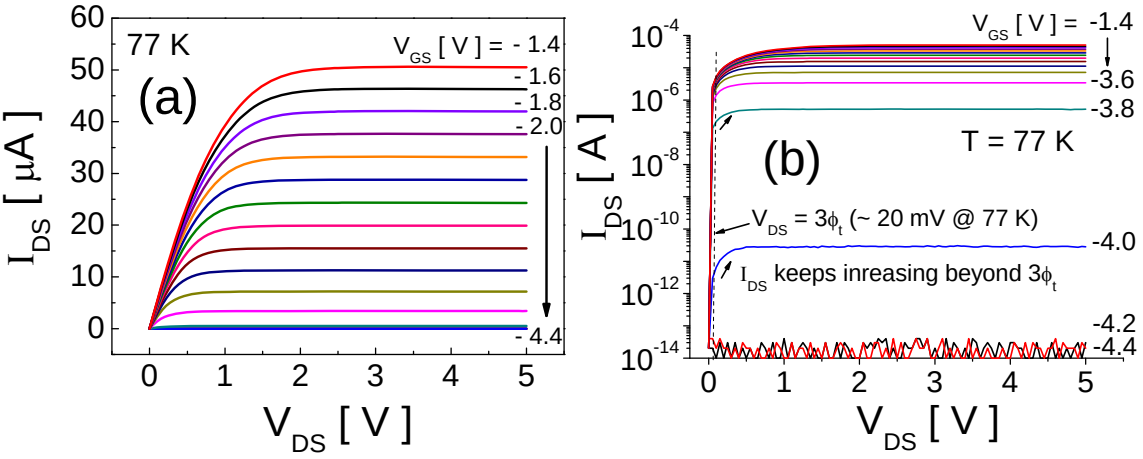

Fig. 5.3 (a) linear-scale and (b) log-scale I_{DS}-V_{DS} for V_{GS} from -4.4 V to -1.4 V at 77 K.

Similar I_{DS}-V_{DS} characteristics have been obtained at different temperatures. We observed that the saturation current I_{Dsat} at various V_{GS} does not follow the quadratic law which predicts that I_{Dsat} varies linearly with $(V_{GS} - V_{th})^2$ as it does in conventional long-channel MOSFETs. Rather, as shown in Fig. 5.4, I_{Dsat} varies linearly with the over-threshold voltage $(V_{GS} - V_{th})$ at different temperatures for V_{GS} in the range -3.8 V to -1.4 V.

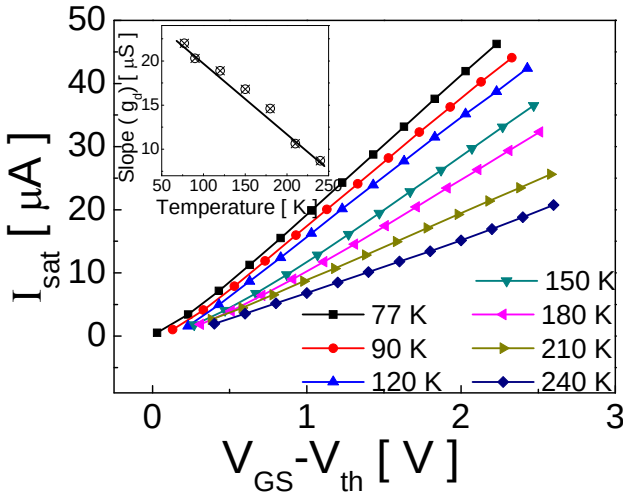

Fig. 5.4 I_{Dsat} as a function of over-threshold voltage ($V_{GS} - V_{th}$) and inset: its linear fit slope vs. temperature.

The saturation current can be expressed by the drift current model as a product of the number of electrons and their velocity at the source end of the nanowire:

$$I_{Dsat} = Aqn_s v_s = \frac{C_{ox}}{L}(V_{GS} - V_{th})v_s$$

where A, n_s, C_{ox}, L and v_s are nanowire cross-section area, electron concentration at source end, gate capacitance, channel length and electron velocity at the source end of Bi_2Se_3 nanowire, respectively. Therefore this linear relationship suggests that the saturation of I_{DS} is due to electron velocity saturation at the source end of the channel instead of pinch-off at the drain end of the nanowire channel. The slope of each I_{Dsat} vs. ($V_{GS} - V_{th}$) curve is saturation channel conductance (g_{dsat}); its value at different temperatures is extracted from Fig. 5.4 and plotted in the inset, showing that the electron velocity at the source end increases linearly with decreasing temperature. The capacitance per unit length C_{ox}/L = 1.3×10^{-9} F/m was given by numerical calculation using a

Synopsis TCAD program based on the cross-section size of the TEM image in Fig. 5.1(d). The calculated value of v_s is from 1×10^6 cm/s to 2×10^6 cm/s for temperatures from 240 K to 77 K, which is of the same order of magnitude as the Fermi velocity of Ti in the source and drain contacts. [165]

5.3.2 Electron Transport Effective Mobility and Surface Conduction Separation

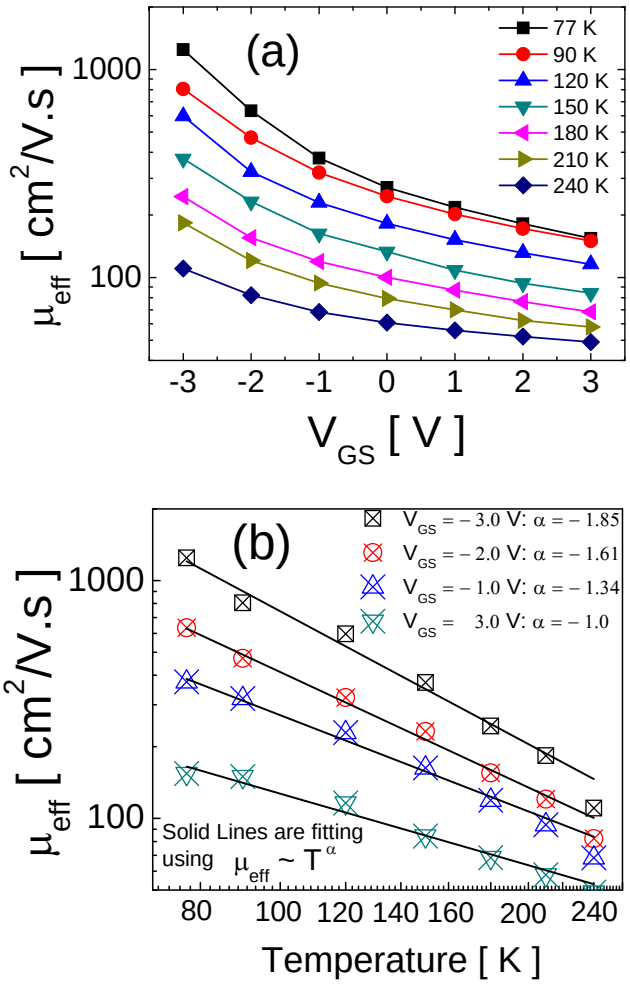

Fig. 5.5 (a) Electron effective mobility vs. gate voltage at different temperatures in a range 77 K – 240 K; (b) Electron effective mobility as a function of temperature in different device operation regions and the fits to $\mu_{eff} \sim T^{\alpha}$.

Fig. 5.5(a) shows the electron effective mobility (μ_{eff}) of Bi_2Se_3 nanowire FET as a function of applied gate voltage at different temperatures. The field-effect mobility extracted from the I_{DS}-V_{GS} curves shows a similar result. The effective mobility values were extracted from the linear region of I_{DS}-V_{DS} curves by using the following equation:

$$\frac{\partial I_{DS}}{\partial V_{DS}} = \mu_{eff} \frac{C_{ox}}{L^2} (V_{GS} - V_{th})$$

The electron effective mobility decreases with increasing gate voltage in the range 200 cm^2/Vs to 1300 cm^2/Vs at 77 K. It should be noted that the precision of effective mobility estimation can be affected by the numerically calculated gate capacitance due to the top and bottom gate coupling. In Fig. 5.5(b), electron effective mobility as a function of temperature at different gate voltages is plotted and fitted using $\mu_{eff} \sim T^{\alpha}$. The value of α is about -1.85 at small over-threshold voltage and increases to -1.0 at large over-threshold voltage. Larger over-threshold voltage will induce higher vertical electric fields. These mobility-temperature relationships suggest that electron-phonon scattering is a dominating factor in low-field conduction (optical phonon scattering for $-2.0 > \alpha > -1.5$, acoustic phonon scattering for $\alpha \approx -1.5$), and as the gate electric field increases, interface charge Columbic scattering limits electron mobility in the Bi_2Se_3 nanowire FETs with $\alpha \sim -1$. [166]

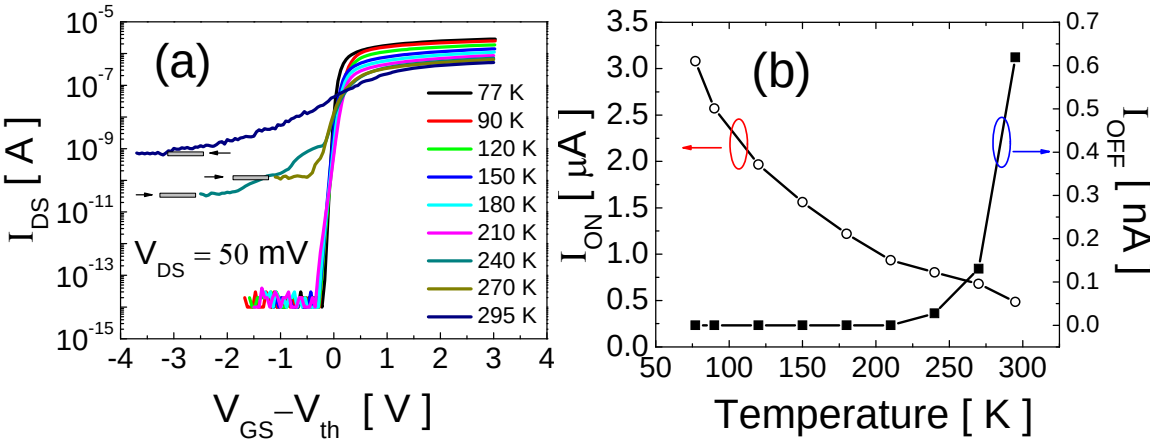

Fig. 5.6 (a) I_{DS}-V_{GS} at different temperature from 77 K to 295 K with V_{DS} = 50 mV; (b) Data extracted from (a): On-state and Off-state current as a function of temperature.

Fig. 5.6(a) compares the transfer characteristics (I_{DS}-V_{GS}) of a Bi_2Se_3 nanowire FET at different temperatures, all of which show unipolar, n-type, field effect behaviors. The I_{DS}-V_{GS} curves obtained at temperatures lower than 240 K show a clear cutoff region ($I_{DS} \approx 0$) in the subthreshold region ($V_{GS} < V_{th}$) and a large On/Off current ratio reaching 10^8. The Off-state current for temperatures > 240 K flattens and saturates at negative voltages much below V_{th}. The temperature dependence of currents in the On and Off states are summarized in Fig. 5.6(b). The Off-state current for temperatures above 240 K was taken from the flat region while the On-state current was taken at V_{GS} = 2.0 V. The Off state current starts increasing rapidly as the temperature increases above 240 K, while the On-state current keeps decreasing as the temperature increases. Such temperature dependence indicates metallic conduction in the On state and insulating behavior in the Off state.

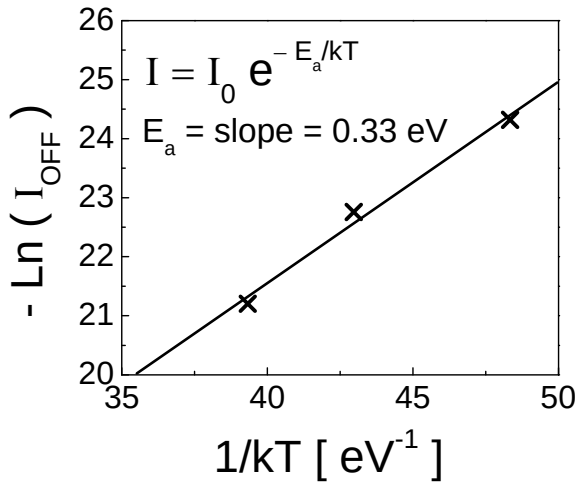

Fig. 5.7 $ln(I_{DS})$ at Off state vs. $1/kT$ above 240 K and its fit to $I_{DS,Off} = I_0 e^{-E_a/kT}$.

Fig. 5.7 shows a fitting of the strongly activated temperature-dependent current to $I_{DS,Off} = I_0 e^{-E_a/kT}$ where E_a is the activation energy, k is Boltzmann's constant, and I_0 is a constant prefactor. The fit shows that E_a is about 0.33 eV which is very close to reported bandgap value of bulk Bi_2Se_3.

5.3.3 Discussion

These results can be interpreted phenomenologically as follows. In the Off state, the gate voltage is large enough to deplete the electrons from the nanowire. The small, temperature dependent Off-state current is due to thermal excitations across the energy band gap of the bulk of Bi_2Se_3. It also indicates that the electric field generated by the gate voltage below the threshold is likely to be strong enough to modify the spectrum of the nanowire and destroy the surface conduction channels. Numerical simulation has demonstrated that electric field could drive a topological insulator across a quantum

phase transition to become a trivial band insulator. [167] In contrast to conventional semiconductor nanowires, the saturated current in the On-state is linear in gate voltage, indicating metallic conduction, and is most likely flowing at the surface of the nanowire. This interpretation is also consistent with the temperature dependence of the saturated conductance. These two regimes, the surface metallic conduction and the insulating switch-off, can be controlled by a surprisingly small gate voltage (a few Volts). Our data cannot unambiguously confirm or rule out the presence of Helical Dirac fermions. Future spectroscopic experiments and theoretical simulations on the spectrum and transport properties of Bi_2Se_3 nanowire FETs will shed more light on the phenomena reported here.

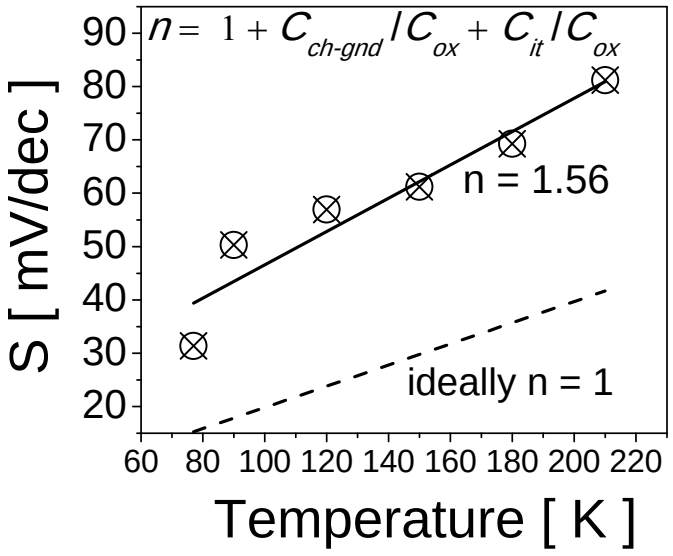

Fig. 5.8 Subthreshold slope as a function of temperature, its fit to $S = ln10\frac{kT}{q}(1 + \frac{C_{ch-gnd}}{C_{ox}} + \frac{C_{it}}{C_{ox}})$ and ideal subthreshold slope $S = ln10\frac{kT}{q}$ which is defined by thermal emission.

The switching performance of a FET is characterized by its subthreshold swing (S) which is defined as the V_{GS} swing to achieve 10 time increase of I_{DS} in the subthreshold region. While these Bi_2Se_3 nanowire FETs have a larger S value than the ideal thermodynamic limit, it is still much smaller than those often reported for nanowire-FETs based on conventional semiconductors. Fig. 5.8 shows the subthreshold swing of the Bi_2Se_3 nanowire FET at different temperatures and its fit to:

$$S = ln10\frac{kT}{q}n = ln10\frac{kT}{q}(1 + \frac{C_{ch-gnd}}{C_{ox}} + \frac{C_{it}}{C_{ox}})$$

where C_{ch-gnd} is the capacitance between the nanowire surface and ground, and C_{it} is interface state capacitance. [161] It should be noted that the effect of dielectric interface states is negligible at low temperature because I_{DS}-V_{GS} has almost zero hysteresis. From the fitting which assumes C_{ch-gnd}/C_{ox} has no temperature dependence, C_{ch-gnd} is about $0.56C_{ox}$ or 7.3×10^{-10} F/m for the Bi_2Se_3 nanowire.

5.4 Magnetotransport Measurements and Discussion

Up to now, more and deeper research have been carried out on the topological surface states with the help of emerging advanced devices based on topological insulator nanostructure materials, which have large surface-to-volume ratio and can therefore manifest the surface effects. Transport measurements have been proved to be a straightforward approach to study the properties of low-dimensional electronic states.

Magnetotransport study on topological insulator nanostructures to identify the surface states through the observation of quantum oscillations such as Shubnikov-de

Haas (SdH) oscillation and Aharonov-Bohm (AB) oscillation will be an effective approach for understanding the quantum phenomena in these materials. By applying magnetic field along the length of the quasi-1D nanostructures, the quantum interference effects will be observed when the electrons on the topological insulator surface states propagate in complete closed trajectories encircling a certain amount of magnetic flux (multiple of $\frac{1}{2}\Phi_0 = h/2e$). With the presence of strong surface disorder, even multiples of $\frac{1}{2}\Phi_0$ flux can lead to a fully localized state while odd multiples of $\frac{1}{2}\Phi_0$ flux will lead to a π AB phase resulting in a metallic state, demonstrated by conductance maxima in the h/e oscillations. [168, 169] Recent transport measurements on topological insulator nanoribbons reported the AB interference with h/e oscillations. [117, 118] However, the conductance has been found to be minima instead of maxima at the predicted locations in the h/e flux period AB oscillations in these experiments. Such primary h/e oscillations as well as the secondary $h/2e$ oscillations are most likely arising from the weakly disordered regime, resembling the h/e and $h/2e$ AB oscillations in individual normal-metal rings.

In our work, we demonstrate the first experimental observation of the anomalous AB effect with strong disorder on the surface in high performance gate-surrounding Bi_2Se_3 nanowire FETs. We believe that the pronounced oscillations are due to the strong surface disorder introduced by tuning chemical potential through the surrounding top gate.

The magnetotransport measurements of the Bi_2Se_3 nanowire FETs were carried out in a cryostat with magnetic field up to 9 T and temperature as low as 1.5 K (Fig. 5.9(a)). As shown in Fig. 5.9(b), by turning On the Bi_2Se_3 nanowire FET through gate

biasing, pronounced oscillations in magnetoresistance have been observed by sweeping the magnetic field in the direction along the length of nanowire channel. The oscillations in channel resistance obtained at different gate voltage demonstrate an average oscillation period of ~ 1.92 T. For the h/e AB interference effect, such period corresponds to a cross section area of 2.15×10^{-15} m^2 (~ 52 nm in diameter by assuming a cylindrical nanowire channel). This diameter is to be confirmed by further TEM measurements. In addition, a sharp localization peak was observed at zero-field, different from the antilocalization features demonstrated in Ref. [117] and [118]. This is probably due to different physics observed in these two experiments, more likely based on weak surface disorder, analogous to the AB oscillations in normal metal rings. [168] Further measurements and analysis would be necessary to confirm the origin of this phenomenon.

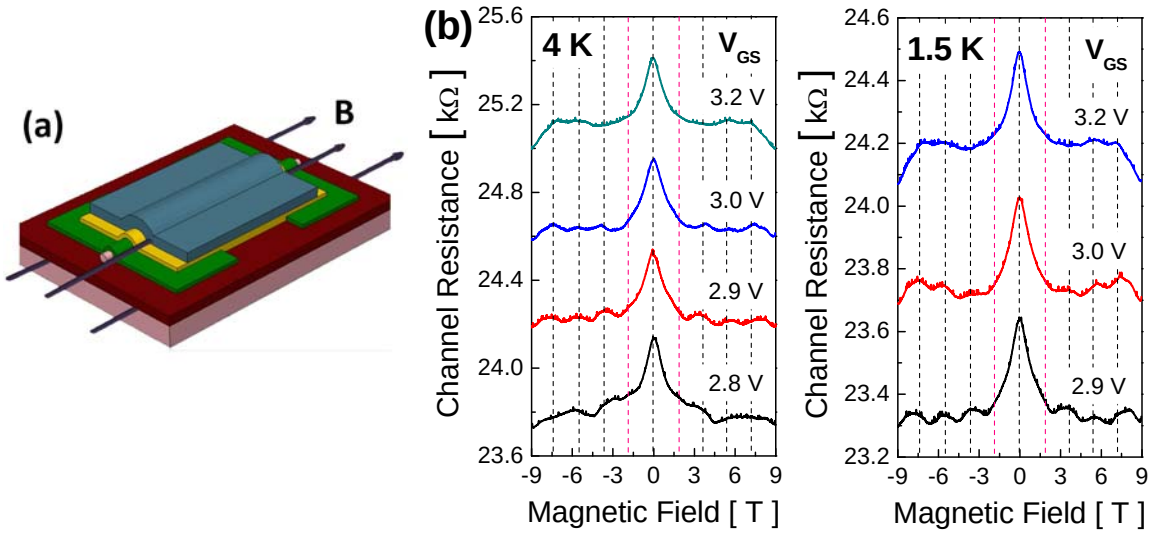

Fig. 5.9 (a) Schematic diagram of a Bi_2Se_3 nanowire FET in magnetic field along the length of nanowire channel; (b) Magnetoresistance vs. magnetic field under different gate voltage at 4 K and 1.5 K.

We also characterized the AB oscillations when the Bi_2Se_3 nanowire FET was tuned to work in different regions by gate biases. But no periodic behavior was observed for the Off state, and diminished oscillations with only clear zero-field localization peak was observed for the subthreshold region. Enhanced AB oscillations were obtained only at gate biases in a small range around 3 V. It is also interesting to find out that when the gate voltage was biased below or beyond the range around 3 V while remaining the FET On state, the oscillation behavior faded to some extent, and there was a small shift in the location of the conductance maxima as well as the oscillation period. Similar trend was observed at T = 1.5 K, as shown in Fig. 5.9(b). This is probably due to the chemical potential's position in the bulk gap tuned by the gate voltage. With varying chemical potential of the surface states, the conductance maxima will be shifted, corresponding to the fluctuation of the oscillation period. The oscillation amplitude would also show a dependence on the chemical potential and disorder strength which needs to be further confirmed. Nevertheless, these results might provide an effective approach to tune the AB oscillation through gate modulation. We believe that the magnetotransport properties of the topological insulator nanostructure involved in such a high performance semiconductor FET is very attractive for future applications in spintronics and sensing devices.

5.5 Summary

In summary, we have fabricated Bi_2Se_3 nanowire field-effect transistors by using a self-alignment technique and observed excellent device characteristics. The FETs show

unipolar, n-type behavior with a clear cutoff in the Off state with only thermally activated conduction at relatively high temperatures, and a well-saturated output current indicating surface metallic conduction. The effective mobility extracted for different gate voltages and temperatures indicates phonon scattering at low electric fields and surface Columbic scattering at larger electric fields. The achievement of sharp switching from cutoff to surface conduction and saturation current by a gate voltage of a few volts is neither expected nor has been previously reported. The different scaling behavior of the saturation current versus gate voltage in these devices relative to most conventional semiconductor nanowire FETs may lead to novel circuit applications. The magnetotransport properties of the Bi_2Se_3 nanowire FETs have been studied and experimental observation of the anomalous AB oscillation has been demonstrated. AB interference under strong surface disorder has been observed, different from the recently reported results which are more likely to be observed in weak disorder region. Gate voltage dependence of the AB oscillation in the surrounding-gate FET is probably due to the changing in chemical potential of surface states. Our results in the electrical and magnetotransport characteristics of the Bi_2Se_3 nanomaterials will open up the possibility of electric manipulation of spin current and transport properties using gate voltage.

Chapter 6 Summary and Prospects for Future Work

6.1 Concluding Remarks for the Dissertation

My research has been focused on novel non-volatile memory and topological insulator nanowire FETs. First, dielectric stack engineering including multiple dielectric layers and redox-active molecules for charge storage have been designed, fabricated and fully characterized. Second, high-performance topological insulator nanowire FETs have been fabricated and characterized for understanding the principles and mechanism of the material and applications for future devices. The major findings of this dissertation are summarized in the following:

1) The dielectric stacks in SONOS-like structure charge-trapping non-volatile memory have been engineered with prominent charge trapping materials and multiple stacks. Good memory behaviors including fast operation speed, good reliability, and sufficient charge storage density have been obtained. Multi-bit memory has been achieved through using novel dielectric stack with multiple charge-trapping layers.

2) Hybrid silicon/molecular Flash memory have been fabricated and studied for high-performance non-volatile memory application. Redox molecule attachments have been characterized by CyV and XPS measurements. The molecular memory has demonstrated excellent P/E speed and endurance properties, making it very promising for on-chip memory applications. Multi-bit memory can also be achieved by utilizing

molecules with multiple redox centers, the attachment of which has been confirmed to be successful on Si structures.

3) High-performance SiNW FETs have been fabricated. They exhibit excellent performance: high On/Off current ratio, small subthreshold slope and small leakage current. These self-aligned SiNW FETs provide good platform to realize real dielectric charge-trapping and molecular Flash memories in our research.

4) Multiple dielectric stacks and redox-active molecules have been integrated into the gate stacks in Flash memory devices based on self-aligned SiNW FETs. Due to the scaling from the planar Si channel to SiNW, enhanced memory performance has been achieved in Flash memory devices. Multi-bit storage has been obtained in the dielectric Flash memory, and the molecular Flash memory demonstrates excellent endurance.

5) Novel topological insulator Bi_2Se_3 nanowire FETs have been fabricated by using the self-alignment technique. Excellent device performance has been observed. Physics and mechanism of the material and electrical behavior have been analyzed. The separation of surface conduction from the bulk and the carrier scattering mechanism have been studied.

6) Magnetotransport measurements of Bi_2Se_3 nanowire FETs have been carried out. First experimental observation of anomalous Aharonov-Bohm oscillation related to strong surface disorder has been demonstrated. Carrier propagation on the surface has been studied. Quantum mechanisms of the carrier transport and magnetoresistance oscillation have been preliminarily analyzed.

6.2 Prospects for Future Work

There are a few areas that need further investigations and improvements in our research. First, new materials and device structures are keys for the future development of CMOS devices and Flash-like non-volatile memory. Gate stacks and charge storage materials need to be further engineered for better performance and distinct multi-bit memory. Second, integration of molecules with multiple redox centers on SiNW FETs for multi-bit Flash memory applications will further improve the memory density in molecular memory cells. Third, we will study the integration of the molecular Flash memory cells into programmable circuit arrays for microprocessors. Fourth, we need to develop further understanding of the fundamental principles behind the electrical characteristics shown in the topological insulator materials and devices in our experiments. For this task, we may need to analyze the topological insulator nanowire FETs by using other measurement methods, such as optical measurement, SdH oscillations and more AB interference studies.

References

[1] S. I. Assoc., "*International Technology Roadmap for Semiconductors* (2013 Update)."

[2] R. H. Dennard, F. H. Gaensslen, H. N. Yu, V. L. Rideout, E. Bassous, and A. R. Leblanc, "Design of ion-implanted MOSFET's with very small physical dimensions (Reprinted from IEEE Journal of Solid-State Circuits, vol 9, pg 256-268, 1974)," *Proceedings of the IEEE,* vol. 87, pp. 668-678, Apr 1999.

[3] G. E. Moore, "Progress in digital integrated electronics," *IEDM Technical Digest,* pp. 11-13, 1975.

[4] E. J. Nowak, "Maintaining the benefits of CMOS scaling when scaling bogs down," *IBM Journal of Research and Development,* vol. 46, pp. 169-180, Mar-May 2002.

[5] L. Baldi and R. Bez, "The scaling challenges of CMOS and the impact on high-density non-volatile memories," *Microsystem Technologies-Micro-and Nanosystems-Information Storage and Processing Systems,* vol. 13, pp. 133-138, Jan 2007.

[6] D. K. Sadana, S. W. Bedell, J. P. de Souza, Y. Sun, E. Kiewra, A. Reznicek*, et al.*, "CMOS Scaling Beyond 22 nm Node," in *Graphene and Emerging Materials for Post-Cmos Applications*. vol. 19, Y. Obeng, S. DeGendt, P. Srinivasan, D. Misra, H. Iwai, Z. Karim*, et al.*, Eds., ed, 2009, pp. 267-274.

[7] K. Sukegawa, M. Yamaji, K. Yoshie, K. Furumochi, T. Maruyama, H. Morioka*, et al.*, "High-performance 80-nm gate length SOI-CMOS technology with copper and very-low-k interconnects," *Symposium on VLSI Technology, Digest of Technical Papers*, pp. 186-189, Jun 2000.

[8] M. Ino, H. Sawada, K. Nishimura, M. Urano, H. Suto, S. Date*, et al.*, "0.25 μm CMOS/SIMOX gate array LSI," in *1996 Ieee International Solid-State Circuits Conference, Digest of Technical Papers*. vol. 39, J. H. Wuorinen, Ed., ed, 1996, pp. 86-87.

[9] R. Chau, J. Kavalieros, B. Roberds, R. Schenker, D. Lionberger, D. Barlage*, et al.*, "*30nm physical gate length CMOS transistors with 1.0 ps n-MOS and 1.7 ps p-MOS gate delays*," *IEDM Tech. Dig.,* pp. 45-48, 2000.

[10] X. J. Huang, W. C. Lee, C. Kuo, D. Hisamoto, L. L. Chang, J. Kedzierski*, et al.*, "Sub-50 nm p-channel FinFET," *IEEE Transactions on Electron Devices,* vol. 48, pp. 880-886, May 2001.

[11] D. Gan, C. Hu, G. E. Parker, H. H. Pao, and G. Jolly, "n-p-n Array Yield Improvement in a 0.18-μm Deep Trench SiGe BiCMOS Process," *IEEE Transactions on Electron Devices,* vol. 59, pp. 590-595, Mar 2012.

[12] M. Horowitz and W. Daily, "How scaling will change processor architecture," in *2004 IEEE International Solid-State Circuits Conference, Digest of Technical Papers*. vol. 47, L. C. Fujino, Ed., ed, 2004, pp. 132-133.

[13] L. Chang, D. J. Frank, R. K. Montoye, S. J. Koester, B. L. Ji, P. W. Coteus*, et al.*, "Practical Strategies for Power-Efficient Computing Technologies," *Proceedings of the IEEE,* vol. 98, pp. 215-236, Feb 2010.

[14] L. R. Carley, J. A. Bain, G. K. Fedder, D. W. Greve, D. F. Guillou, M. S. C. Lu*, et al.*, "Single-chip computers with microelectromechanical systems-based magnetic memory (invited)," *Journal of Applied Physics,* vol. 87, pp. 6680-6685, May 2000.

[15] C. Yoshida, K. Tsunoda, H. Noshiro, and Y. Sugiyama, "High speed resistive switching in Pt/TiO_2/TiN film for nonvolatile memory application," *Applied Physics Letters,* vol. 91, p. 223510, Nov 2007.

[16] M. H. R. Lankhorst, B. Ketelaars, and R. A. M. Wolters, "Low-cost and nanoscale non-volatile memory concept for future silicon chips," *Nature Materials,* vol. 4, pp. 347-352, Apr 2005.

[17] R. Waser, R. Dittmann, G. Staikov, and K. Szot, "Redox-Based Resistive Switching Memories - Nanoionic Mechanisms, Prospects, and Challenges," *Advanced Materials,* vol. 21, pp. 2632-2663, Jul 2009.

[18] N. Inoue, N. Furutake, A. Toda, M. Tada, and Y. Hayashi, "PZT MIM capacitor with oxygen-doped Ru-electrodes for embedded FeRAM devices," *IEEE Transactions on Electron Devices,* vol. 52, pp. 2227-2235, Oct 2005.

[19] S. Lai, "Non-Volatile Memory Technologies: The Quest for Ever Lower Cost," *IEDM Tech. Dig.,* pp. 11-16, 2008.

[20] G. Atwood, "Future directions and challenges for ETox flash memory scaling," *IEEE Transactions on Device and Materials Reliability,* vol. 4, pp. 301-305, Sep 2004.

[21] S. K. Lai, "Flash memories: Successes and challenges," *IBM Journal of Research and Development,* vol. 52, pp. 529-535, Jul-Sep 2008.

[22] P. Pavan, R. Bez, P. Olivo, and E. Zanoni, "Flash memory cells - An overview," *Proceedings of the IEEE,* vol. 85, pp. 1248-1271, Aug 1997.

[23] K. H. Wu, H. C. Chien, C. C. Chan, T. S. Chen, and C. H. Kao, "SONOS device with tapered bandgap nitride layer," *IEEE Transactions on Electron Devices,* vol. 52, pp. 987-992, May 2005.

[24] K. Honda, S. Hashimoto, and Y. Cho, "Visualization of electrons and holes localized in gate thin film of metal SiO_2-Si_3N_4-SiO_2 semiconductor-type flash memory using scanning nonlinear dielectric microscopy after writing-erasing cycling," *Applied Physics Letters,* vol. 86, p. 063515, Feb 2005.

[25] S. J. Wrazien, Y. J. Zhao, J. D. Krayer, and M. H. White, "Characterization of SONOS oxynitride nonvolatile semiconductor memory devices," *Solid-State Electronics,* vol. 47, pp. 885-891, May 2003.

[26] T. S. Chen, K. H. Wu, H. Chung, and C. H. Kao, "Performance improvement of SONOS memory by bandgap engineering of charge-trapping layer," *IEEE Electron Device Letters,* vol. 25, pp. 205-207, Apr 2004.

[27] J. J. Welser, S. Tiwari, S. Rishton, K. Y. Lee, and Y. Lee, "Room temperature operation of a quantum-dot flash memory," *IEEE Electron Device Letters,* vol. 18, pp. 278-280, Jun 1997.

[28] T. Baron, B. Pelissier, L. Perniola, F. Mazen, J. M. Hartmann, and G. Rolland, "Chemical vapor deposition of Ge nanocrystals on SiO_2," *Applied Physics Letters,* vol. 83, pp. 1444-1446, Aug 2003.

[29] Y. M. Niquet, G. Allan, C. Delerue, and M. Lannoo, "Quantum confinement in germanium nanocrystals," *Applied Physics Letters,* vol. 77, pp. 1182-1184, Aug 2000.

[30] B. Eitan, P. Pavan, I. Bloom, E. Aloni, A. Frommer, and D. Finzi, "NROM: A novel localized trapping, 2-bit nonvolatile memory cell," *IEEE Electron Device Letters,* vol. 21, pp. 543-545, Nov 2000.

[31] I. Bloom, P. Pavan, and B. Eitan, "NROM^{TM} - a new non-volatile memory technology: from device to products," *Microelectronic Engineering,* vol. 59, pp. 213-223, Nov 2001.

[32] M. H. White, D. A. Adams, and J. K. Bu, "On the go with SONOS," *IEEE Circuits & Devices,* vol. 16, pp. 22-31, Jul 2000.

[33] P. C. Y. Chen, " Threshold-alterable Si-gate MOS devices," *IEEE Transactions on Electron Devices,* vol. 24, pp. 584-586, May 1977.

[34] J. K. Bu and M. H. White, "Design considerations in scaled SONOS nonvolatile memory devices," *Solid-State Electronics,* vol. 45, pp. 113-120, Jan 2001.

[35] P. H. Tsai, K. S. Chang-Liao, T. Y. Wu, T. K. Wang, P. J. Tzeng, C. H. Lin*, et al.*, "Novel SONOS - type nonvolatile memory device with stacked tunneling and charge trapping layers," *Solid-State Electronics,* vol. 52, pp. 1573-1577, Oct 2008.

[36] X. G. Wang, J. Liu, W. P. Bai, and D. L. Kwong, "A novel MONOS-type nonvolatile memory using high-k dielectrics for improved data retention and programming speed," *IEEE Transactions on Electron Devices,* vol. 51, pp. 597-602, Apr 2004.

[37] S. Maikap, H. Y. Lee, T. Y. Wang, P. J. Tzeng, C. C. Wang, L. S. Lee*, et al.*, "Charge trapping characteristics of atomic-layer-deposited HfO_2 films with Al_2O_3 as a blocking oxide for high-density non-volatile memory device applications," *Semiconductor Science and Technology,* vol. 22, pp. 884-889, Jun 2007.

[38] C. C. Yeh, T. P. Ma, N. Ramaswamy, N. Rocklein, D. Gealy, T. Graettinger*, et al.*, "Frenkel-Poole trap energy extraction of atomic layer deposited Al_2O_3 and Hf_xAl_yO thin films," *Applied Physics Letters,* vol. 91, p. 113521, Sep 2007.

[39] M. Lisiansky, A. Heiman, M. Kovler, A. Fenigstein, Y. Roizin, I. Levin*, et al.*, "$SiO_2/Si_3N_4/Al_2O_3$ stacks for scaled-down memory devices: Effects of interfaces and thermal annealing," *Applied Physics Letters,* vol. 89, p. 153506, Oct 2006.

[40] S. Choi, M. Cho, H. Hwang, and J. W. Kim, "Improved metal-oxide-nitride-oxide-silicon-type flash device with high-k dielectrics for blocking layer," *Journal of Applied Physics,* vol. 94, pp. 5408-5410, Oct 2003.

[41] J. Zhu and Z. G. Liu, "Comparative study of pulsed laser deposited HfO_2 and Hf-aluminate films for high-k gate dielectric applications," *Applied Physics a-Materials Science & Processing,* vol. 80, pp. 1769-1773, May 2005.

[42] M. Specht, H. Reisinger, F. Hofmann, T. Schulz, E. Landgraf, R. J. Luyken*, et al.*, "Charge trapping memory structures with Al_2O_3 trapping dielectric for high-temperature applications," *Solid-State Electronics,* vol. 49, pp. 716-720, May 2005.

[43] H. W. You and W. J. Cho, "Charge trapping properties of the HfO_2 layer with various thicknesses for charge trap flash memory applications," *Applied Physics Letters,* vol. 96, p. 093506, Mar 2010.

[44] J. Liu, Q. Wang, S. Long, M. Zhang, and M. Liu, "A metal/Al_2O_3/ZrO_2/SiO_2/Si (MAZOS) structure for high-performance non-volatile memory application," *Semiconductor Science and Technology,* vol. 25, p. 055013, Apr 2010.

[45] X. Zhu, Q. Li, D. E. Ioannou, D. Gu, J. E. Bonevich, H. Baumgart*, et al.*, "Fabrication, characterization and simulation of high performance Si nanowire-based non-volatile memory cells," *Nanotechnology,* vol. 22, p. 254020, Jun 24 2011.

[46] G. Congedo, A. Lamperti, L. Lamagna, and S. Spiga, "Stack engineering of TANOS charge-trap flash memory cell using high-κ ZrO_2 grown by ALD as charge trapping layer," *Microelectronic Engineering,* vol. 88, pp. 1174-1177, Jul 2011.

[47] M. Specht, H. Reisinger, M. Stadele, F. Hofmann, A. Gschwandtner, E. Landgraf*, et al.*, "Retention time of novel charge trapping memories using Al_2O_3 dielectrics," ESSDERC 2003: Proceedings of the 33rd European Solid-State Device Research Conference, pp. 155-158, Sep 2003.

[48] C. H. Lee, S. H. Hur, Y. C. Shin, J. H. Choi, D. G. Park, and K. Kim, "Charge-trapping device structure of SiO_2/SiN/high-k dielectric Al_2O_3 for high-density flash memory," *Applied Physics Letters,* vol. 86, p. 152908, Apr 2005.

[49] X. Wang and D.-L. Kwong, "A Novel High-k SONOS Memory Using TaN/Al_2O_3/Ta_2O_5/HfO_2/Si Structure for Fast Speed and Long Retention Operation," *IEEE Transactions on Electron Devices,* vol. 53, pp. 78-82, Jan 2006.

[50] Z. Tang, Z. Liu, and X. Zhu, "Progress of High-k Dielectrics Applicable to SONOS-Type Nonvolatile Semiconductor Memories," *Transactions on Electrical and Electronic Materials,* vol. 11, pp. 155-165, Aug 2010.

[51] G.-H. Park and W.-J. Cho, "Reliability of modified tunneling barriers for high performance nonvolatile charge trap flash memory application," *Applied Physics Letters,* vol. 96, p. 043503, Jan 2010.

[52] K. K. Likharev, "Layered tunnel barriers for nonvolatile memory devices," *Applied Physics Letters,* vol. 73, pp. 2137-2139, Oct 1998.

[53] B. Govoreanu, P. Blomme, M. Rosmeulen, J. Van Houdt, and K. De Meyer, "VARIOT: A novel multilayer tunnel barrier concept, for low-voltage nonvolatile memory devices," *IEEE Electron Device Letters,* vol. 24, pp. 99-101, Feb 2003.

[54] W. Chen, W.-J. Liu, M. Zhang, S.-J. Ding, D. W. Zhang, and M.-F. Li, "Multistacked $Al_2O_3/HfO_2/SiO_2$ tunnel layer for high-density nonvolatile memory application," *Applied Physics Letters,* vol. 91, p. 022908, Jul 2007.

[55] J. Kim, A. J. Hong, M. Ogawa, S. Ma, E. B. Song, Y. S. Lin*, et al.*, "Novel 3-D structure for ultra high density Flash memory with VRAT (Vertical-Recess-Array-Transistor) and PIPE (Planarized Integration on the same PlanE)," *Symposium on VLSI Technology, Digest of Technical Papers*, pp. 122-123, Jun 2008.

[56] Z. T. Liu, C. Lee, V. Narayanan, G. Pei, and E. C. Kan, "A novel quad source/drain metal nanocrystal memory device for multibit-per-cell storage," *IEEE Electron Device Letters,* vol. 24, pp. 345-347, May 2003.

[57] B. Ricco, G. Torelli, M. Lanzoni, A. Manstretta, H. E. Maes, D. Montanari*, et al.*, "Nonvolatile multilevel memories for digital applications," *Proceedings of the IEEE,* vol. 86, pp. 2399-2421, Dec 1998.

[58] N. V. Nguyen, C. A. Richter, Y. J. Cho, G. B. Alers, and L. A. Stirling, "Effects of high-temperature annealing on the dielectric function of Ta_2O_5 films observed by spectroscopic ellipsometry," *Applied Physics Letters,* vol. 77, pp. 3012-3014, Nov 2000.

[59] R. L. McCreery, "Molecular Electronic Junctions," *Chem. Mater.,* vol. 16, pp. 4477-4496, Aug 2004.

[60] A. H. Flood, E. W. Wong, and J. F. Stoddart, "Models of charge transport and transfer in molecular switch tunnel junctions of bistable catenanes and rotaxanes," *Chemical Physics,* vol. 324, pp. 280-290, May 2006.

[61] R. L. McCreery and A. J. Bergren, "Progress with Molecular Electronic Junctions: Meeting Experimental Challenges in Design and Fabrication," *Advanced Materials,* vol. 21, pp. 4303-4322, Nov 2009.

[62] D. Vuillaume, "Molecular Nanoelectronics," *Proceedings of the IEEE,* vol. 98, pp. 2111-2123, Dec 2010.

[63] Q. L. Li, G. Mathur, S. Gowda, S. Surthi, Q. Zhao, L. H. Yu, *et al.*, "Multibit memory using self-assembly of mixed ferrocene/porphyrin monolayers on silicon," *Advanced Materials,* vol. 16, pp. 133-137, Jan 2004.

[64] Q. Li, S. Surthi, G. Mathur, S. Gowda, V. Misra, T. A. Sorenson, *et al.*, "Electrical characterization of redox-active molecular monolayers on SiO_2 for memory applications," *Applied Physics Letters,* vol. 83, pp. 198-200, Jul 2003.

[65] Z. M. Liu, A. A. Yasseri, J. S. Lindsey, and D. F. Bocian, "Molecular memories that survive silicon device processing and real-world operation," *Science,* vol. 302, pp. 1543-1545, Nov 2003.

[66] Q. L. Li, S. Surthi, G. Mathur, S. Gowda, Q. Zhao, T. A. Sorenson, *et al.*, "Multiple-bit storage properties of porphyrin monolayers on SiO_2," *Applied Physics Letters,* vol. 85, pp. 1829-1831, Sep 2004.

[67] K. M. Roth, A. A. Yasseri, Z. M. Liu, R. B. Dabke, V. Malinovskii, K. H. Schweikart, *et al.*, "Measurements of electron-transfer rates of charge-storage molecular monolayers on Si(100). Toward hybrid molecular/semiconductor information storage devices," *Journal of the American Chemical Society,* vol. 125, pp. 505-517, Jan 2003.

[68] S. Gowda, G. Mathur, Q. L. Li, S. Surthi, and V. Misra, "Hybrid silicon/molecular FETs: A study of the interaction of redox-active molecules with silicon MOSFETs," *IEEE Transactions on Nanotechnology,* vol. 5, pp. 258-264, May 2006.

[69] Z. Chen, B. Lee, S. Sarkar, S. Gowda, and V. Misra, "A molecular memory device formed by HfO_2 encapsulation of redox-active molecules," *Applied Physics Letters,* vol. 91, p. 173111, Oct 2007.

[70] J. Shaw, Y. W. Zhong, K. J. Hughes, T. H. Hou, H. Raza, S. Rajwade, *et al.*, "Integration of Self-Assembled Redox Molecules in Flash Memory Devices," *IEEE Transactions on Electron Devices,* vol. 58, pp. 826-834, Mar 2011.

[71] J. Shaw, Q. Y. Xu, S. Rajwade, T. H. Hou, and E. C. Kan, "Redox Molecules for a Resonant Tunneling Barrier in Nonvolatile Memory," *IEEE Transactions on Electron Devices,* vol. 59, pp. 1189-1198, Apr 2012.

[72] J. Xiang, W. Lu, Y. J. Hu, Y. Wu, H. Yan, and C. M. Lieber, "Ge/Si nanowire heterostructures as high-performance field-effect transistors," *Nature,* vol. 441, pp. 489-493, May 2006.

[73] Y. Cui, Z. H. Zhong, D. L. Wang, W. U. Wang, and C. M. Lieber, "High performance silicon nanowire field effect transistors," *Nano Letters,* vol. 3, pp. 149-152, Feb 2003.

[74] S. J. Tans, A. R. M. Verschueren, and C. Dekker, "Room-temperature transistor based on a single carbon nanotube," *Nature,* vol. 393, pp. 49-52, Apr 1998.

[75] S. Uchikoga, "Low-temperature polycrystalline silicon thin-film transistor technologies for system-on-glass displays," *MRS Bulletin,* vol. 27, pp. 881-886, Nov 2002.

[76] J. P. Colinge, "Multiple-gate SOI MOSFETs," *Solid-State Electronics,* vol. 48, pp. 897-905, Jun 2004.

[77] K. Vonklitzing, G. Dorda, and M. Pepper, " New Method for High-Accuracy Determination of the Fine-Structure Constant Based on Quantized Hall Resistance," *Physical Review Letters,* vol. 45, pp. 494-497, Aug 1980.

[78] B. A. Bernevig, T. L. Hughes, and S. C. Zhang, "Quantum spin Hall effect and topological phase transition in HgTe quantum wells," *Science,* vol. 314, pp. 1757-61, Dec 2006.

[79] H. Zhang, C.-X. Liu, X.-L. Qi, X. Dai, Z. Fang, and S.-C. Zhang, "Topological insulators in Bi_2Se_3, Bi_2Te_3 and Sb_2Te_3 with a single Dirac cone on the surface," *Nature Physics,* vol. 5, pp. 438-442, Jun 2009.

[80] J. E. Moore, "The birth of topological insulators," *Nature,* vol. 464, pp. 194-198, Mar 2010.

[81] J. Moore, "Topological insulators: The next generation," *Nature Physics,* vol. 5, pp. 378-380, Jun 2009.

[82] M. Koenig, S. Wiedmann, C. Bruene, A. Roth, H. Buhmann, L. W. Molenkamp, *et al.*, "Quantum spin hall insulator state in HgTe quantum wells," *Science,* vol. 318, pp. 766-770, Nov 2007.

[83] C. L. Kane and E. J. Mele, "Z_2 Topological Order and the Quantum Spin Hall Effect," *Physical Review Letters,* vol. 95, p. 146802, Sep 2005.

[84] B. A. Bernevig and S. C. Zhang, "Quantum spin hall effect," *Physical Review Letters,* vol. 96, p. 106802, Mar 2006.

[85] L. Fu, C. L. Kane, and E. J. Mele, "Topological insulators in three dimensions," *Physical Review Letters,* vol. 98, p. 106803, Mar 2007.

[86] R. Roy, "Topological phases and the quantum spin Hall effect in three dimensions," *Physical Review B,* vol. 79, p. 195322, May 2009.

[87] J. E. Moore and L. Balents, "Topological invariants of time-reversal-invariant band structures," *Physical Review B,* vol. 75, p. 121306, Mar 2007.

[88] X.-L. Qi, T. L. Hughes, and S.-C. Zhang, "Topological field theory of time-reversal invariant insulators," *Physical Review B,* vol. 78, p. 195424, Nov 2008.

[89] L. Fu and C. L. Kane, "Topological insulators with inversion symmetry," *Physical Review B,* vol. 76, p. 045302, Jul 2007.

[90] D. Hsieh, D. Qian, L. Wray, Y. Xia, Y. S. Hor, R. J. Cava*, et al.*, "A topological Dirac insulator in a quantum spin Hall phase," *Nature,* vol. 452, pp. 970-974, Apr 2008.

[91] D. Hsieh, Y. Xia, L. Wray, D. Qian, A. Pal, J. H. Dil*, et al.*, "Observation of Unconventional Quantum Spin Textures in Topological Insulators," *Science,* vol. 323, pp. 919-922, Feb 2009.

[92] M. Z. Hasan and C. L. Kane, "Colloquium: Topological insulators," *Reviews of Modern Physics,* vol. 82, pp. 3045-3067, Nov 2010.

[93] X.-L. Qi and S.-C. Zhang, "Topological insulators and superconductors," *Reviews of Modern Physics,* vol. 83, pp. 1057-1110, Oct 2011.

[94] H. Lind, S. Lidin, and U. Haussermann, "Structure and bonding properties of $(Bi_2Se_3)_m(Bi_2)_n$ stacks by first-principles density functional theory," *Physical Review B,* vol. 72, p. 184101, Nov 2005.

[95] Y. L. Chen, J. G. Analytis, J. H. Chu, Z. K. Liu, S. K. Mo, X. L. Qi*, et al.*, "Experimental realization of a three-dimensional topological insulator, Bi_2Te_3," *Science,* vol. 325, pp. 178-181, Jul 2009.

[96] D. Hsieh, Y. Xia, D. Qian, L. Wray, J. H. Dil, F. Meier*, et al.*, "A tunable topological insulator in the spin helical Dirac transport regime," *Nature,* vol. 460, pp. 1101-1105, Aug 2009.

[97] Y. Xia, D. Qian, D. Hsieh, L. Wray, A. Pal, H. Lin*, et al.*, "Observation of a large-gap topological-insulator class with a single Dirac cone on the surface," *Nature Physics,* vol. 5, pp. 398-402, Jun 2009.

[98] T. Hanaguri, K. Igarashi, M. Kawamura, H. Takagi, and T. Sasagawa, "Momentum-resolved Landau-level spectroscopy of Dirac surface state in Bi_2Se_3," *Physical Review B,* vol. 82, p. 081305, Aug 2010.

[99] P. Roushan, J. Seo, C. V. Parker, Y. S. Hor, D. Hsieh, D. Qian, *et al.*, "Topological surface states protected from backscattering by chiral spin texture," *Nature,* vol. 460, pp. 1106-1109, Aug 2009.

[100] T. Zhang, P. Cheng, X. Chen, J. F. Jia, X. C. Ma, K. He, *et al.*, "Experimental Demonstration of Topological Surface States Protected by Time-Reversal Symmetry," *Physical Review Letters,* vol. 103, p. 266803, Dec 2009.

[101] Y. Y. Li, G. Wang, X. G. Zhu, M. H. Liu, C. Ye, X. Chen, *et al.*, "Intrinsic topological insulator Bi_2Te_3 thin films on Si and their thickness limit," *Advanced Materials,* vol. 22, pp. 4002-4007, Sep 2010.

[102] I. Garate and M. Franz, "Inverse Spin-Galvanic Effect in the Interface between a Topological Insulator and a Ferromagnet," *Physical Review Letters,* vol. 104, p. 146802, Apr 2010.

[103] F. Wilczek, "Majorana returns," *Nature Physics,* vol. 5, pp. 614-618, Sep 2009.

[104] L. Fu and C. Kane, "Superconducting Proximity Effect and Majorana Fermions at the Surface of a Topological Insulator," *Physical Review Letters,* vol. 100, p. 096407, Mar 2008.

[105] V. Mourik, K. Zuo, S. M. Frolov, S. R. Plissard, E. P. Bakkers, and L. P. Kouwenhoven, "Signatures of Majorana fermions in hybrid superconductor-semiconductor nanowire devices," *Science,* vol. 336, pp. 1003-1007, May 2012.

[106] M. X. Wang, C. Liu, J. P. Xu, F. Yang, L. Miao, M. Y. Yao, *et al.*, "The coexistence of superconductivity and topological order in the Bi_2Se_3 thin films," *Science,* vol. 336, pp. 52-55, Apr 2012.

[107] M. Veldhorst, M. Snelder, M. Hoek, T. Gang, V. K. Guduru, X. L. Wang, *et al.*, "Josephson supercurrent through a topological insulator surface state," *Nature Materials,* vol. 11, pp. 417-421, May 2012.

[108] V. Goyal, D. Teweldebrhan, and A. A. Balandin, "Mechanically-exfoliated stacks of thin films of Bi_2Te_3 topological insulators with enhanced thermoelectric performance," *Applied Physics Letters,* vol. 97, p. 133117, Sep 2010.

[109] S. Cho, N. P. Butch, J. Paglione, and M. S. Fuhrer, "Insulating behavior in ultrathin bismuth selenide field effect transistors," *Nano Letters,* vol. 11, pp. 1925-1927, May 2011.

[110] J. W. McIver, D. Hsieh, H. Steinberg, P. Jarillo-Herrero, and N. Gedik, "Control over topological insulator photocurrents with light polarization," *Nature Nanotechnology,* vol. 7, pp. 96-100, Feb 2012.

[111] S. Cho, D. Kim, P. Syers, N. P. Butch, J. Paglione, and M. S. Fuhrer, "Topological insulator quantum dot with tunable barriers," *Nano Letters,* vol. 12, pp. 469-472, Jan 2012.

[112] D. X. Qu, Y. S. Hor, J. Xiong, R. J. Cava, and N. P. Ong, "Quantum oscillations and hall anomaly of surface states in the topological insulator Bi_2Te_3," *Science,* vol. 329, pp. 821-824, Aug 2010.

[113] J. J. Cha and Y. Cui, "Topological insulators: The surface surfaces," *Nature Nanotechnology,* vol. 7, pp. 85-86, Feb 2012.

[114] Y. Yan, Z. M. Liao, Y. B. Zhou, H. C. Wu, Y. Q. Bie, J. J. Chen*, et al.*, "Synthesis and quantum transport properties of Bi_2Se_3 topological insulator nanostructures," *Scientific Reports,* vol. 3, p. 1264, Feb 2013.

[115] J. J. Cha, K. J. Koski, and Y. Cui, "Topological insulator nanostructures," *physica status solidi (RRL) - Rapid Research Letters,* vol. 7, pp. 15-25, Oct 2013.

[116] D. Kong, J. C. Randel, H. Peng, J. J. Cha, S. Meister, K. Lai*, et al.*, "Topological insulator nanowires and nanoribbons," *Nano Letters,* vol. 10, pp. 329-333, Jan 2010.

[117] F. X. Xiu, L. A. He, Y. Wang, L. N. Cheng, L. T. Chang, M. R. Lang*, et al.*, "Manipulating surface states in topological insulator nanoribbons," *Nature Nanotechnology,* vol. 6, pp. 216-221, Apr 2011.

[118] H. L. Peng, K. J. Lai, D. S. Kong, S. Meister, Y. L. Chen, X. L. Qi*, et al.*, "Aharonov-Bohm interference in topological insulator nanoribbons," *Nature Materials,* vol. 9, pp. 225-229, Mar 2010.

[119] O. Gunawan, L. Sekaric, A. Majumdar, M. Rooks, J. Appenzeller, J. W. Sleight*, et al.*, "Measurement of carrier mobility in silicon nanowires," *Nano Letters,* vol. 8, pp. 1566-1571, Jun 2008.

[120] M. Zervas, D. Sacchetto, G. De Micheli, and Y. Leblebici, "Top-down fabrication of very-high density vertically stacked silicon nanowire arrays with low

temperature budget," *Microelectronic Engineering,* vol. 88, pp. 3127-3132, Oct 2011.

[121] R. S. Wagner and W. C. Ellis, " Vapor-Liquid-Solid Mechanism Of Single Crystal Growth," *Applied Physics Letters,* vol. 4, pp. 89-90, Mar 1964.

[122] J. Westwater, D. P. Gosain, S. Tomiya, S. Usui, and H. Ruda, "Growth of silicon nanowires via gold/silane vapor-liquid-solid reaction," *Journal of Vacuum Science & Technology B,* vol. 15, pp. 554-557, May 1997.

[123] Y. Huang, X. F. Duan, Q. Q. Wei, and C. M. Lieber, "Directed assembly of one-dimensional nanostructures into functional networks," *Science,* vol. 291, pp. 630-633, Jan 2001.

[124] W. Salalha and E. Zussman, "Investigation of fluidic assembly of nanowires using a droplet inside microchannels," *Physics of Fluids,* vol. 17, p. 063301, Jun 2005.

[125] S. Evoy, N. DiLello, V. Deshpande, A. Narayanan, H. Liu, M. Riegelman*, et al.*, "Dielectrophoretic assembly and integration of nanowire devices with functional CMOS operating circuitry," *Microelectronic Engineering,* vol. 75, pp. 31-42, Jul 2004.

[126] S. J. Papadakis, J. A. Hoffmann, D. Deglau, A. Chen, P. Tyagi, and D. H. Gracias, "Quantitative analysis of parallel nanowire array assembly by dielectrophoresis," *Nanoscale,* vol. 3, pp. 1059-1065, Mar 2011.

[127] Q. L. Li, S. M. Koo, M. D. Edelstein, J. S. Suehle, and C. A. Richter, "Silicon nanowire electromechanical switches for logic device application," *Nanotechnology,* vol. 18, p. 315202, Aug 2007.

[128] T. Hertel, R. Martel, and P. Avouris, "Manipulation of individual carbon nanotubes and their interaction with surfaces," *Journal of Physical Chemistry B,* vol. 102, pp. 910-915, Feb 1998.

[129] H. Zhu, Q. Li, H. Yuan, H. Baumgart, D. E. Ioannou, and C. A. Richter, "Self-aligned multi-channel silicon nanowire field-effect transistors," *Solid-State Electronics,* vol. 78, pp. 92-96, Dec 2012.

[130] X. Zhu, Y. Yang, Q. Li, D. E. Ioannou, J. S. Suehle, and C. A. Richter, "Silicon nanowire NVM cell using high-k dielectric charge storage layer," *Microelectronic Engineering,* vol. 85, pp. 2403-2405, Dec 2008.

[131] B. Z. Liu, Y. F. Wang, T. T. Ho, K. K. Lew, S. M. Eichfeld, J. M. Redwing*, et al.*, "Oxidation of silicon nanowires for top-gated field effect transistors," *Journal of Vacuum Science & Technology A,* vol. 26, pp. 370-374, May 2008.

[132] Y. H. Wu, P. Y. Kuo, Y. H. Lu, Y. H. Chen, and T. S. Chao, "Novel Symmetric Vertical-Channel Ni-Salicided Poly-Si Thin-Film Transistors With High ON/OFF-Current Ratio," *IEEE Electron Device Letters,* vol. 31, pp. 1233-1235, Nov 2010.

[133] X. F. Duan, "Nanowire Thin-Film Transistors: A New Avenue to High-Performance Macroelectronics," *IEEE Transactions on Electron Devices,* vol. 55, pp. 3056-3062, Nov 2008.

[134] M. K. Kim, S. D. Chae, H. S. Chae, J. H. Kim, Y. S. Jeong, J. W. Lee*, et al.*, "Ultrashort SONOS memories," *IEEE Transactions on Nanotechnology,* vol. 3, pp. 417-424, Dec 2004.

[135] C. H. Lee, K. I. Choi, M. K. Cho, Y. H. Song, K. C. Park, K. Kim, *et al.*, A novel SONOS structure of $SiO_2/SiN/Al_2O_3$ with TaN metal gate for multi-giga bit flash memeries, *IEDM Technical Digest,* pp. 613-616, Dec 2003.

[136] M. Specht, R. Kommling, L. Dreeskornfeld, W. Weber, F. Hofmann, D. Alvarez*, et al.*, "Sub-40nm tri-gate charge trapping nonvolatile memory cells for high-density applications," *Symposium on VLSI Technology, Digest of Technical Papers*, pp. 244-245, Jun 2004.

[137] G. Zhang and W. J. Yoo, "V_{th} Control by Complementary Hot-Carrier Injection for SONOS Multi-Level Cell Flash Memory," *IEEE Transactions on Electron Devices,* vol. 56, pp. 3027-3032, Dec 2009.

[138] S.-H. Gu, T. Wang, W.-P. Lu, Y.-H. J. Ku, and C.-Y. Lu, "Extraction of nitride trap density from stress induced leakage current in silicon-oxide-nitride-oxide-silicon flash memory," *Applied Physics Letters,* vol. 89, p. 163514, Oct 2006.

[139] Y. Q. Wang, W. S. Hwang, G. Zhang, G. Samudra, Y. C. Yeo, and W. J. Yoo, "Electrical characteristics of memory devices with a high-k HfO_2 trapping layer and dual SiO_2/Si_3N_4 tunneling layer," *IEEE Transactions on Electron Devices,* vol. 54, pp. 2699-2705, Oct 2007.

[140] X. D. Huang, P. T. Lai, L. Liu, and J. P. Xu, "Nitrided $SrTiO_3$ as charge-trapping layer for nonvolatile memory applications," *Applied Physics Letters,* vol. 98, p. 242905, Jun 2011.

[141] X. D. Huang, L. Liu, J. P. Xu, and P. T. Lai, "Improved charge-trapping properties of HfYON film for nonvolatile memory applications in comparison with HfON and Y_2O_3 films," *Applied Physics Letters,* vol. 99, p. 112903, Sep 2011.

[142] H. F. Zhang, S. P. Ruan, C. H. Feng, B. K. Xu, W. Y. Chen, and W. Dong, "Photoelectric Properties of TiO_2-ZrO_2 Thin Films Prepared by Sol-Gel Method," *Journal of Nanoscience and Nanotechnology,* vol. 11, pp. 10003-10006, Nov 2011.

[143] E. Bersch, S. Rangan, R. A. Bartynski, E. Garfunkel, and E. Vescovo, "Band offsets of ultrathin high-kappa oxide films with Si," *Physical Review B,* vol. 78, Aug 2008.

[144] O. Sharia, A. A. Demkov, G. Bersuker, and B. H. Lee, "Theoretical study of the insulator/insulator interface: Band alignment at the SiO_2/HfO_2 junction," *Physical Review B,* vol. 75, p. 035306, Jan 2007.

[145] S. Seki, T. Unagami, and B. Tsujiyama, "Electron trapping levels in rf-sputtered Ta_2O_5 films," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films,* vol. 1, pp. 1825-1830, Oct 1983.

[146] W. J. Zhu, T. P. Ma, T. Tamagawa, J. Kim, and Y. Di, "Current transport in metal/hafnium oxide/silicon structure," *IEEE Electron Device Letters,* vol. 23, pp. 97-99, Feb 2002.

[147] B. Mann and H. Kuhn, "Tunneling through Fatty Acid Salt Monolayers," *Journal of Applied Physics,* vol. 42, pp. 4398-4405, Oct 1971.

[148] A. Aviram and M. A. Ratner, "Molecular Rectifiers," *Chemical Physics Letters,* vol. 29, pp. 277-283, Nov 1974.

[149] H. Kuhn and D. Mobius, "Systems of Monomolecular Layers-Assembling and Physico-Chemical Behavior," *Angewandte Chemie-International Edition,* vol. 10, pp. 620-637, Sep 1971.

[150] J. R. Heath, "Molecular Electronics," in *Annual Review of Materials Research*. vol. 39, ed, 2009, pp. 1-23.

[151] C. Li, W. Fan, B. Lei, D. Zhang, S. Han, T. Tang*, et al.*, "Multilevel memory based on molecular devices," *Applied Physics Letters,* vol. 84, p. 1949-1951, Mar 2004.

[152] H. Zhu, C. A. Hacker, S. J. Pookpanratana, C. A. Richter, H. Yuan, H. Li*, et al.*, "Non-volatile memory with self-assembled ferrocene charge trapping layer," *Applied Physics Letters,* vol. 103, p. 053102, 2013.

[153] G. Mathur, S. Gowda, Q. L. Li, S. Surthi, Q. Zhao, and V. Misra, "Properties of functionalized redox-active monolayers on thin silicon dioxide - A study of the. dependence of retention time on oxide thickness," *IEEE Transactions on Nanotechnology,* vol. 4, pp. 278-283, Mar 2005.

[154] M. J. Preiner and N. A. Melosh, "Creating large area molecular electronic junctions using atomic layer deposition," *Applied Physics Letters,* vol. 92, p. 213301, May 2008.

[155] B. Govoreanu, P. Blomme, J. Van Houdt, and K. De Meyer, "Enhanced tunneling current effect for nonvolatile memory applications," *Japanese Journal of Applied Physics Part 1-Regular Papers Short Notes & Review Papers,* vol. 42, pp. 2020-2024, Apr 2003.

[156] L. Liu, J. P. Xu, F. Ji, J. X. Chen, and P. T. Lai, "Improved memory characteristics by NH_3-nitrided GdO as charge storage layer for nonvolatile memory applications," *Applied Physics Letters,* vol. 101, p. 033501, Jul 2012.

[157] T.-H. Hou, U. Ganguly, and E. C. Kan, "Programable molecular orbital states of C_{60} from integrated circuits," *Applied Physics Letters,* vol. 89, p. 253113, Dec 2006.

[158] M. G. Grigorov, J. Weber, N. Vulliermet, H. Chermette, and J. M. J. Tronchet, "Numerical evaluation of the internal orbitally resolved chemical hardness tensor: Second order chemical reactivity through thermal density functional theory," *Journal of Chemical Physics,* vol. 108, pp. 8790-8798, Jun 1998.

[159] C. C. Hobbs, L. R. C. Fonseca, A. Knizhnik, V. Dhandapani, S. B. Samavedam, W. J. Taylor*, et al.*, "Fermi-level pinning at the polysilicon/metal oxide interface - Part I," *IEEE Transactions on Electron Devices,* vol. 51, pp. 971-977, Jun 2004.

[160] C. C. Hobbs, L. R. C. Fonseca, A. Knizhnik, V. Dhandapani, S. B. Samavedam, W. J. Taylor*, et al.*, "Fermi-level pinning at the polysilicon metal oxide interface - Part II," *IEEE Transactions on Electron Devices,* vol. 51, pp. 978-984, Jun 2004.

[161] J. Frei, C. Johns, A. Vazquez, W. Z. Xiong, C. R. Cleavelin, T. Schulz*, et al.*, "Body effect in tri- and pi-gate SOI MOSFETs," *IEEE Electron Device Letters,* vol. 25, pp. 813-815, Dec 2004.

[162] G. Wang, X. G. Zhu, Y. Y. Sun, Y. Y. Li, T. Zhang, J. Wen, *et al.*, "Topological insulator thin films of Bi_2Te_3 with controlled electronic structure," *Advanced Materials,* vol. 23, pp. 2929-2932, Jul 2011.

[163] L. He, F. Xiu, X. Yu, M. Teague, W. Jiang, Y. Fan, *et al.*, "Surface-dominated conduction in a 6 nm thick Bi_2Se_3 thin film," *Nano Letters,* vol. 12, pp. 1486-1490, Mar 2012.

[164] H. Zhu, C. A. Richter, E. Zhao, J. E. Bonevich, W. A. Kimes, H. J. Jang, *et al.*, "Topological insulator Bi_2Se_3 nanowire high performance field-effect transistors," *Scientific Reports,* vol. 3, p. 1757, Apr 2013.

[165] D. L. Zhang, S. M. Liu, X. N. Jing, J. L. Luo, X. G. Zhang, R. J. Wang, *et al.*, "Electronic transport properties of α-TiAl alloys," *International Journal of Modern Physics B,* vol. 19, pp. 3869-3895, Oct 2005.

[166] D. S. Jeon and D. E. Burk, "MOSFET electron inversion layer mobilities-a physically based semi-empirical model for a wide temperature range," *IEEE Transactions on Electron Devices,* vol. 36, pp. 1456-1463, Aug 1989.

[167] J. Li and K. Chang, "Electric field driven quantum phase transition between band insulator and topological insulator," *Applied Physics Letters,* vol. 95, p. 222110, Nov 2009.

[168] Y. Zhang and A. Vishwanath, "Anomalous Aharonov-Bohm conductance oscillations from topological insulator surface states," *Physical Review Letters,* vol. 105, p. 206601, Nov 2010.

[169] J. H. Bardarson, P. W. Brouwer, and J. E. Moore, "Aharonov-Bohm oscillations in disordered topological insulator nanowires," *Physical Review Letters,* vol. 105, p. 156803, Oct 2010.

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