COMPACT MODELING OF MULTI GATE AND OTHER EMERGING TRANSISTORS

by

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A thesis submitted in partial fulfillment of the requirements for the degree of Master of Science at George Mason University

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DEDICATION

This is dedicated to those who expand upon this survey, and my parents.

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ABSTRACT

COMPACT MODELING OF MULTI GATE AND OTHER EMERGING TRANSISTORS

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With the advent of multi gate and nanoscale fabrication techniques, several new transistor topographies have been proposed and manufactured in the past decade. In parallel, accurate and efficient compact models for these devices have been likewise developed. This paper summarizes the major topographies and their associated compact models with a focus toward computationally efficient models constructed for implementation in common modeling languages such as Verilog-A and SPICE. Common physical and mathematical modeling techniques have also been reviewed as has the evolution from simple multi gate devices to nanoscale structures.

Chapter 1 – Introduction

1. 1 – Motivation

With the advent of nanoscale fabrication techniques, a transition from planar to multi gate transistor topographies has been observed. These devices are currently moving from concept to industry and, as such, the need for accurate models describing their electrical properties exists. This survey presents an overview of device compact models from the earliest multi gate devices to contemporary structures concluding with an exploration of nanoscale transistors reliant on ballistic vice traditional solid state transport.

As computationally accurate models are seldom computationally efficient, more so in cases where thousands of devices are concurrently simulated, an attempt has been made to outline a path from physically or mathematically derived expressions to approximated expressions more conducive to software modeling. In particular, cases where models have been parameterized for implementation in modeling software, such as Verilog-A, SPICE, or BSIM, are given special attention.

Additionally, symmetries between topographies as reflected in both derived expressions and compact modeling techniques have been considered in this survey. Seldom are

these topographies, in structure or in model, independent from all others, a reality that is reflected in the use of common derivation methods and, in some cases, the extension of models between different topographies.

Finally, topics for further research have been noted throughout and will be summarized in both chapter remarks and survey conclusion.

1.2 – Dissertation Organization

The academic and professional world of compact modeling is divided among several largely independent groups that exhibit little coordination in their research topics and modeling methods. As such, there is not a smooth flow between physically/mathematically derived models, computationally efficient approximations, or parameterized software models. Therefore, while each chapter attempts a transition between each of these modeling areas, jumps often occur. However, as this survey aims to present as complete a picture of contemporary device modeling as possible, these discontinuities have been tolerated for the sake of the whole.

Toward a unified view of contemporary compact modeling, each chapter aims to conform to the following structure:

1. Physically or mathematically derived compact models; often described in the literature as “analytic”, these models derive from fundamental expressions, such as the Poisson equation or the generalized parabola equation.

2. Computationally efficient models; also described as “numeric”, these models are logical approximations of the analytic models toward the development of expressions that may be easily simulated.

3. Software models; extensions of numeric models that are meant for implementation in common compact modeling software (Verilog-A, SPICE, BSIM). These models are discretely parameterized with instructions regarding parameter extraction.

Note that not all chapters include each of the above model types; this is dependent upon research per device type.

The chapters themselves are organized in device chronological order. Chapters 2 and 3 review double gate device models beginning with JFET devices (JFET and MESFET: Chapter 2) and continuing to MOSFET devices (SOI and standard: Chapter 3). Chapter 4 introduces triple gate MOSFET topographies and extends their analysis to a universal multi gate model while additionally noting their similarities to double gate fin-type MOSFETs. Chapter 5 briefly covers the quadruple gate MOSFET, modeled in recent literature as a special case of the cylindrical gate MOSFET, which is the topic of Chapter 6. Transitioning to Chapter 7, the cylindrical gate MOSFET is reduced in radius until its form is that of a one dimensional nanowire. Nanowire structures are further analyzed per their exhibition of strictly solid-state effects (i.e., drift/diffusion current), mixed solid-state and ballistic effects (where the formulation per Landauer of ballistic current

is presented), and finally purely ballistic effects. This analysis is carried into Chapter 8 where the carbon nanotube FET is explored, a device that exhibits ballistic effects only.

Chapter 9 concludes this survey with a review, observations, and recommendations for further research. Appendices reviewing multi gate BSIM software models and listing common expression variables follow.

1.3 – Conventions

This survey inherits variable symbols per the source cited, leading to multiple symbols representing the same concept. For example, ϕ, ψ, and Ψ each represent surface potential, depending on the source cited. Similarly, both r and R represent an object radius, again depending on source cited. These replications have been captured in the glossary of common variables (Appendix II).

A change in symbol employed in this survey is the use of $E_{f(S)}$ and $E_{f(D)}$ to represent the Fermi levels at nanowire/nanotube source/drain Schottky contacts vice source symbols μ_S and μ_D; this was done to prevent confusion with the more common MOSFET convention of μ as carrier mobility.

Finally, distinction between short channel and nanoscale devices was based on source cited, though the accepted convention seems to be that “nano-“ applies to cases where the device may be modeled as a one dimensional object.

Chapter 2 – Compact Models of Double Gate FET Topographies

2.1 – Double Gate JFET

2.1.1 – Introduction

The JFET (Junction gate Field Effect Transistor) is comprised of p-type islands parallel-imbedded in an n-type body. Each island is gate-biased to constrict, via depletion regions, the channel between the source/drain terminals of the n-type body (Figure 1). (Note this describes an n-channel JFET; p-channel would be constructed similarly, reversing the doping of each region).

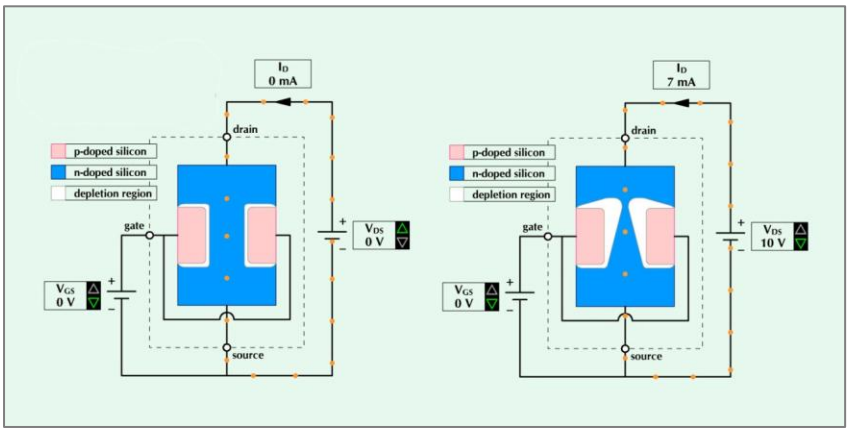

Figure 1 - JFET under equilibrium (left) and 10V drain bias (right) [1].

Circa 1990, existing SPICE models assumed both gates in a JFET were biased simultaneously, operating as a single element. Van Halen et al. [2] addressed this issue per their implementation of independently biased gate equations and parameters.

2.1.2 – Theory

Considering top and bottom gates to be biased simultaneously, current is as:

$$I_{DS(lin)} = \frac{\mu\varepsilon W}{2L}(2(V_{GS} - V_T)V_{DS} - V_{DS}^2) \tag{2.1}$$

$$I_{DS(sat)} = \frac{\mu\varepsilon W}{2L}(V_{GS} - V_T)^2 \tag{2.2}$$

Note the treatment of V_{GS} as a single element; the equations are as we would expect for a standard, single gate FET. A more complete form of $I_{DS(lin)}$ follows, inclusive of independent gate bias; from this, V_{GS} will be extracted and broken into its constituent top and bottom gate components via $V_{DS(sat)}$ and $I_{DS(sat)}$ [3]:

$$I_{DS} = G_0\left(V_{DS} - \frac{2V_{pT}^{-1/2}}{3}\left[(V_{DS} + V_{BIT} - V_{GST})^{3/2} - (V_{BIT} - V_{GST})^{3/2}\right] - \frac{2V_{pB}^{-1/2}}{3}\left[(V_{DS} + V_{BIB} - V_{GSB})^{3/2} - (V_{BIB} - V_{GSB})^{3/2}\right]\right) \tag{2.3}$$

Where $V_{p(i)}$ is the pinch-off voltage and $V_{BI(i)}$ is the built-in voltage. Differentiating I_{DS} with respect to V_{DS} and calculating V_{DS} for $\frac{dI_{DS}}{dV_{DS}} = 0$ (note only the shown quadratic term of (2.4) is considered in (2.5)):

$$V_{DS(sat)} = \frac{(V_{GST} - V_{GSB} - V_{BIT} + V_{BIB})^2}{4V_{pT}V_{pB}} + \ \ldots \tag{2.4}$$

$$I_{DS(sat)} = \frac{\mu\epsilon W}{2L}(P_1V_{GST} + P_2V_{GSB} + P_3V_{GST}V_{GSB} + P_4V_{GSB}^2 + P_5V_{GST}^2 - V_T)^2 \tag{2.5}$$

From which V_{GS} is extracted from the dominant term of (2.4):

$$V_{GS} = P_1V_{GST} + P_2V_{GSB} + P_3V_{GST}V_{GSB} + P_4V_{GSB}^2 + P_5V_{GST}^2 \tag{2.6}$$

Where the trailing "T or "B" in the subscripts indicates top or bottom gate, respectively, and $P_{1\ldots5}$ are the $V_{GS(i)}$ coefficients.

2.1.3 – Model

2.1.3.1 – Drain Current Parameters

Extraction of the $P_{1\ldots5}$ coefficients is sufficient to model independent gate biases. $P_{1\ldots3}$ are functions of top pinch-off voltage V_{TT}, bottom pinch-off voltage V_{TB}, and simultaneous pinch-off voltage V_{TS}:

$$P_1 = \frac{V_T}{V_{TT}} \tag{2.7}$$

$$P_2 = \frac{V_T}{V_{TB}} \tag{2.8}$$

$$P_3 = \frac{V_T}{V_{TS}^2} - \frac{V_T}{V_{TS}V_{TT}} - \frac{V_T}{V_{TS}V_{TB}} \tag{2.9}$$

With voltages V_{TT}, V_{TB}, and V_{TS} determined by driving equation (2.5) with top gate only, bottom gate only, and both gates until $I_{DS(sat)} = 0$. Quadratic coefficients $P_{4,5}$ are determined through fitting the complete measured $\sqrt{I_{DS}}$ versus V_{TT}, V_{TB}, and V_{TS} per equation (2.5) using singular value decomposition [2].

2.1.3.2 – Channel Length Modulation and Source/Drain Resistance Parameters

Channel length modulation parameter λ follows via determination of source/drain resistance parameters $R_{S,D}$ from measured transconductances $g_{(i)}$:

$$\lambda = \frac{1}{\frac{I_{DS}}{g_{DS}} - V_{DS}} \tag{2.10}$$

$$\frac{1}{g_{DS}} = \frac{1}{g_{DS0}} + (R_S + R_D) \tag{2.11}$$

$$\frac{1}{g_m} = \frac{1}{g_{m0}} + R_S \tag{2.12}$$

$$g_{DS0} = g_{m0} = \beta(V_{GS} - V_T) \tag{2.13}$$

Where $\beta = \frac{\mu\epsilon W}{2L}$ and V_{GS} is composed per above. As parameters β and V_T are known, R_S and R_D may be calculated via simultaneous solution of (2.11) and (2.12).

2.2 – Double Gate MESFET

2.2.1 – Introduction

The MESFET (MEtal Semiconductor Field Effect Transistor) is similar in design to the JFET, replacing the p-n junction gates with Schottky junction gates. Double gate theory and modeling is extended to the multi gate case by Iniguez et al. [4].

2.2.2 – Theory

A charge-based physical approach is employed in constructing the MESFET model. Double gate effects are derived by splitting single gate results. Beginning with charge density per unit length for a single gate MESFET:

$$q_c = qn_s\left(W - 4\varepsilon\frac{V_{bi} - V_{GC}}{qn_s}\right) \tag{2.14}$$

Where n_s is sheet electron density, V_{bi} is the built-in voltage, and V_{GC} is the voltage between the gate and some channel position ($V_{GC} = V_{GS}$ at the source and V_{GD} at the drain). Splitting V_{GC} between two gates yields the following analogous double gate charge density per unit length with total voltage calculated via averaging in the new numerator:

$$q_c = qn_s\left(W - 2\varepsilon\frac{2V_{bi} - V_{GC1} - V_{GC2}}{qn_s}\right) \tag{2.15}$$

For $c_{eff} = 4\varepsilon$ (capacitance per unit length) and $V_T = V_{bi} - \frac{qn_sW}{4\varepsilon}$ (threshold voltage), we have:

$$q_c = c_{eff}\left(\frac{V_{GC1} + V_{GC2}}{2} - V_T\right) \tag{2.16}$$

Note that for $V_{GC1} = V_{GC2}$, (2.3) reduces to the single gate case $q_c = c_{eff}(V_{GC} - V_T)$.

Further, as expected $I_D \propto \left(\frac{V_{GC1}+V_{GC2}}{2} - V_T\right)$ for the double gate subthreshold region, again analogous to the single gate case [4 pp. 1744-1745].

A new effect that requires consideration in a double gate system is nonlinear coupling between the gates. Two variables affect this coupling; the expected asymmetry of the depletion regions and the nonlinear relationship between depletion charge and gate voltage. This is modeled as parameter ξ:

$$\xi = \frac{\Delta \mathrm{V_T}}{(V_{G1} - V_{G2})^2} \tag{2.17}$$

System capacitances (2.18) and (2.19) are derived from fitting factors m_c (transition region fitting factor), γ, γ_c, and η (subthreshold ideality factor), which are determined based on numerical analysis, and nested factors that are ultimately functions of V_G, V_T, and thermal voltage V_{th} (analogous to the HFET approach per [5]):

$$C_{gs} = C_f + \frac{2}{3} C_{gc} \left[1 - \left(\frac{\mathrm{V_{sat\,e}} - \mathrm{V_{ds\,e}}}{2\mathrm{V_{sat\,e}} - \mathrm{V_{ds\,e}}} \right)^2 \right] \tag{2.18}$$

$$C_{gd} = C_f + \frac{2}{3} C_{gc} \left[1 - \left(\frac{\mathrm{V_{sat\,e}}}{2\mathrm{V_{sat\,e}} - \mathrm{V_{ds\,e}}} \right) \right] \tag{2.19}$$

$$\mathrm{V_{ds\,e}} = V_{DS} \left[1 + \left(\frac{V_{DS}}{\mathrm{V_{sat\,e}}} \right)^{m_c} \right]^{-1/m_c} \tag{2.20}$$

$$C_{gc} = L \frac{c_{gc}}{\left[1 + \left(\frac{n_l'}{n_{max}} \right)^{\gamma_c} \right]^{1+1/\gamma}} \tag{2.21}$$

$$n_l' = \frac{2 c_{eff} \eta V_{th}}{q} \log \left[1 + \frac{1}{2} \exp \left(\frac{V_{GS} - V_T}{\eta V_{th}} \right) \right] \tag{2.22}$$

Where effective saturation voltage $\mathrm{V_{sat\,e}} = \frac{\mathrm{I_{sat}}}{\mathrm{g_{ch}}}$, C_f is the fringe capacitance, and $c_{gc} = \frac{dn_l'}{dV_{GT}}$ [4 p. 1743 and 1747]. Extrinsic conductance g_{ch} will be treated separately as it is a function of extracted parameter α as well as (2.22) above.

2.2.2.1 – Extension to Multi Gate Case

The extension to a multi gate model is achieved by splitting each device into a set of double gate models, each modeled per above. Though [4] does not give multi gate

equation extensions, it is conjectured that the resulting equations would still hold to the above established rules (V_G effects would be averaged for q_c and I_D calculations and would reduce under equal bias to the single gate case):

$$q_c = c_{eff}\left(\frac{V_{GC1} + \cdots + V_{GCn}}{n} - V_T\right) \tag{2.23}$$

$$I_D \propto \left(\frac{V_{GC1} + \cdots + V_{GCn}}{n} - V_T\right) \tag{2.24}$$

Similarly, a multi gate extension to (2.17) was not given; to conjecture, it would perhaps be the average ξ over all unique $V_{Gi,j}$, ΔV_T combinations $\{(V_{Gi}, V_{Gj}), (\Delta V_{Tij} = |V_{Ti} - V_{Tj}|) : i \neq j, i < j\}$.

2.2.3 – Compact Model

Parameter extraction follows procedures developed for HFETs [5]; specific to V_{Gi}, we have the following parameter set:

2.2.3.1 – V_T

V_T is extracted per established $\sqrt{I_{DS}}$ vs. V_{GS} procedures.

2.2.3.2 – α

Parameter α is extracted from measurements on short channel devices and acts to adjust I_{DS} as a function of g_{ch} (see [4] equation (5)) for nonlinear effects as follows:

$$g_{ch} = \frac{g_{chi}}{1 + g_{chi}(R_s + R_d)} \tag{2.25}$$

$$g_{chi} = \frac{qn_l\mu}{L + \alpha d_{dep}} \tag{2.26}$$

Where d_{dep} is the average depletion depth and $d_{dep(i)} = 2\varepsilon\frac{V_{bi}-V_{GS(i)}}{qn_s}$ and n_l is a fitting function of n_l' and γ ([4] equation (7)).

2.2.3.3 – ξ

Parameter ξ is calculated as a function of $V_{Gi,j}$ and ΔV_T per above.

2.3 – Remarks

The JFET model introduces gate voltage averaging as a calculation technique and second order polynomial coefficients as extractable parameters, methods that will be seen in later models. Significant model error is noted in the linear/saturation transition region, a failure of the model mathematics and not of the extraction routines [2]. Binomial expansion truncations in (2.4) are noted as the cause of this transition region error; [2 p. 99] recommends development of "a better JFET model primitive" to best model the transition region.

The MESFET model is unique as it accounts for a theoretically unlimited number of gates in its channel region, though not all parameters have been explicitly extended to this case. Submicron issues have been observed in the linear region as effective length decreases per increases in gate voltage, though this effect has been controlled somewhat by the α parameter.

Chapter 3 – Compact Models of Double Gate MOSFET Topographies

3.1 – Silicon-on-Insulator MOSFET

3.1.1 – Introduction

Designed in part as a response to the inability of older technologies to meet Moore's Law, the SOI MOSFET (Silicon On Insulator Metal Oxide Semiconductor Field Effect Transistor) employs a thin, in this case undoped, body resting on some insulating material to negate device parasitic capacitances and short channel effects. Ortiz-Conde et al. [6] surveyed physical compact models of such emerging nanodevices for both symmetric and asymmetric cases based on either surface potential, where V_G is an explicit variable as in the previous models, or charge, where it is not.

3.1.2 – General Theory

3.1.2.1 – Surface Potential Model

Let x be the vertical plane perpendicular to the body intersecting both gates and their oxides and y be the horizontal plane parallel to the body intersecting source, drain, and body. For the symmetric case, it is assumed the gates are biased simultaneously, have the same oxide thickness, and have the same V_T. Solution of the one-dimensional Poisson equation yields the following expression [4 p. 132]:

$$V_G = V_{GS} - V_{FB} = \psi_S + \frac{\sqrt{2kTn_i\varepsilon_s}}{C_0}\sqrt{e^{-\beta V}(e^{\beta\psi_S} - e^{\beta\psi_0})} \tag{3.1}$$

$$\psi_S = \psi_0 - \frac{2}{\beta}\ln\left\{\cos\left[\sqrt{\frac{q^2 n_i}{2kT\varepsilon_s}}\, e^{\frac{(\beta(\psi_0 - V))}{2}}\frac{(t_{Si} - x_0)}{2}\right]\right\} \tag{3.2}$$

Where V_{FB} is the flatband voltage, n_i is the intrinsic free carrier density, C_0 is gate oxide capacitance per unit area, ψ_S is the surface potential, ψ_0 is the potential at the center $(x = 0)$ of the silicon film, and $\beta = \frac{q}{kT}$. Note this method employs an explicit solution for V_G vice a polynomial approximation or arithmetic mean.

3.1.2.2 – General Drain Current Integral

Compact models reviewed in [6] are distinguished from each other based on current expressions that manipulate the above standardized V_G and ψ_i variables within different polynomial/trigonometric expressions vice each compact model accounting for differences in V_G within the model-specific equation for V_G. Further, proof of equality between the different approaches was provided. The drain current expression is evaluated via the Pao-Sah integral (3.3) with SOI-specific derivation presented below followed by solutions:

$$I_D = \mu\frac{W}{L}\int_0^{V_{DS}} Q_I dV \tag{3.3}$$

$$Q_I \equiv \int_{\psi_0}^{\psi_S} \frac{n - n_i}{F} d\psi \tag{3.4}$$

Where F is the electric field in the semiconductor film [6 p. 133]; (3.3) and (3.4) are combined to give the general double integral formulation of the SOI MOSFET drain current:

$$I_D = 2\mu \frac{W}{L} \int_0^{V_{DS}} \int_{\psi_0}^{\psi_S} \frac{qn}{F} d\psi dV \tag{3.5}$$

3.1.3 – Symmetric Models

3.1.3.1 – Surface Potential-based Models

Two equivalent surface potential-based models are given in [6]; the results are summarized below. Note that while these models present physically accurate descriptions, neither go on to define extractable parameters for software implementation. Both models are equivalent per [6 p. 134].

First, (3.5) is transformed without approximations into the following expression:

$$I_D = \mu \frac{W}{L} \Big\{ 2C_0 \left[V_{GF}(\psi_{SL} - \psi_{S0}) - \frac{1}{2}(\psi_{SL}^2 - \psi_{S0}^2) \right] + 4\frac{kT}{q} C_o(\psi_{SL} - \psi_{S0}) + t_{Si} kT n_i \left[e^{\beta(\psi_{oL} - V_{DS})} - e^{\beta\psi_{oo}} \right] \Big\} \tag{3.6}$$

Where ψ_i are obtained from numerical solutions of (3.1) and (3.2) at the V-limits of (3.3). It is noted that the final term (t_{Si} …) is negligible [6 p. 133].

The second model introduces a summary variable β_T (further defined [6 p. 134]) to arrive at another form of the symmetric surface potential drain current:

$$I_D = 16\mu\frac{W}{L}\frac{\varepsilon_s}{t_{Si}}\left(\frac{kT}{q}\right)^2\left\{\frac{1}{2}\left(\beta_{TL}^2-\beta_{T0}^2\right)+\beta_{T0}\tan\left(\beta_{T0}\right)-\beta_{TL}\tan\left(\beta_{TL}\right)+\frac{\varepsilon_s}{t_{Si}C_o}\left[\beta_{T0}^2\tan^2\left(\beta_{T0}\right)-\beta_{TL}^2\tan^2\left(\beta_{TL}\right)\right]\right\} \tag{3.7}$$

With β_{Ti} evaluated at the V-limits of (3.3), as were the ψ_i above. Ortiz-Conde et al. give equivalency between (3.6) and (3.7) per the following relationship [6 p. 134]:

$$\beta_{T0}^2 \equiv \frac{\alpha}{\left(4\frac{kT}{qt_{Si}}\right)^2} \tag{3.8}$$

$$\alpha \equiv -\frac{2kTn_i}{\varepsilon_s}e^{\beta(\psi_o-V)} \tag{3.9}$$

3.1.3.2 – Charge-Based Models

Correlation between charge and surface potential is obtained from the following expression [6]:

$$Q_I = 2\varepsilon_s F_s = -2C_0\left(V_{GF}-\psi_S\right) \tag{3.10}$$

From this, the additional approximation $t_{Si}qn_ie^{\beta(\psi_o-V)} \ll \frac{\varepsilon_s}{t_{Si}}\frac{kT}{q}$, and a "smoothing function [6 p. 134]", He et al. [7] developed the following analytic charge-based expression:

$$I_D = \mu\frac{W}{L}\left[\frac{2kT}{q}\left(Q_{IL}-Q_{I0}\right)-\frac{\left(Q_{IL}^2-Q_{I0}^2\right)}{4C_0}\right] \tag{3.11}$$

Note that due to the approximations, this expression is not equivalent via (3.10) with the previously discussed surface potential-based expressions.

Another approximate solution that expands on (3.11) is given by Salesse et al. [8]. In this case, the approximation is $\alpha \approx -\frac{2Q_I}{\beta\varepsilon_s t_{Si}}$:

$$I_D = \mu\frac{W}{L}\frac{2kT}{q}(Q_{IL} - Q_{I0}) - \frac{(Q_{IL}^2 - Q_{I0}^2)}{4C_0} + 8\left(\frac{kT}{q}\right)^2\frac{\varepsilon_s}{t_{Si}}\ln\left[1 - \frac{q t_{Si}(Q_{IL} - Q_{I0})}{8\varepsilon_s kT}\right] \tag{3.12}$$

3.1.3.3 – Correlation between Surface Potential and Charge-Based Models

A transformation of (3.6) from a surface potential to charge-based model is additionally given. Beginning with explicit surface potential expressions as functions of charge:

$$\psi_{oL} = V_{DS} + \frac{kT}{q}\ln\left[e^{\beta(\psi_{SL} - V_{DS})} - \frac{Q_{IL}^2}{8kTn_i\varepsilon_s}\right] \tag{3.13}$$

$$\psi_{o0} = \frac{kT}{q}\ln\left(e^{\beta\psi_{S0}} - \frac{Q_{I0}^2}{8kTn_i\varepsilon_s}\right) \tag{3.14}$$

Combining these with (3.6) yields the following complete charge-based model:

$$I_D = \mu\frac{W}{L}\left\{\frac{2kT}{q}(Q_{IL} - Q_{I0}) - \frac{1}{4}\left(\frac{1}{C_0} + \frac{t_{Si}}{2\varepsilon_s}\right)(Q_{IL}^2 - Q_{I0}^2) + t_{Si}kTn_i e^{\beta V_{GF}}\left[e^{\beta\left(\frac{Q_{IL}}{2C_0} - V_{DS}\right)} - e^{\beta\left(\frac{Q_{IL}}{2C_0}\right)}\right]\right\} \tag{3.15}$$

Note that under their respective charge-based model assumptions, (3.15) reduces to (3.11) and (3.12) [6 p. 134]; additionally, for $t_{Si} \to 0$, (3.15) and (3.12) reduce to (3.11).

3.1.3.4 – Comparison of Surface Potential and Charge-Based Models

Exceptional accuracy (voltage error below 10^{-17}) has been achieved via the non-approximated surface potential-based model developed by Ortiz-Conde et al. (3.6). Similar accuracies have been obtained using the derived non-approximated charge-based model (3.15) as well. The strength of the non-approximate charge model is especially acute at subthreshold voltages and weak inversion (effectively described by the third terms of (3.6) and (3.12)), where the approximated charge models display error factors of 0.5 (3.12) to 1.0 (3.11) for $V_{GF} = (0.2 \dots 0.5)V$. Acceptable error percentages were seen for both (3.11) and (3.12) at approximately $0.7V$ with convergence between predictions and measurements thereafter; unfortunately [6] did not explicitly provide V_T for the test SOI transistor, though it would be expected that V_T (and strong inversion) occur in the range $(0.6 \dots 0.8)V$.

3.1.4 – Asymmetric Theory Extension

Asymmetry in a SOI device introduces several new considerations for compact modeling. Results from Ortiz-Conde et al. are summarized here; for full treatment, see [6 pp. 136-138].

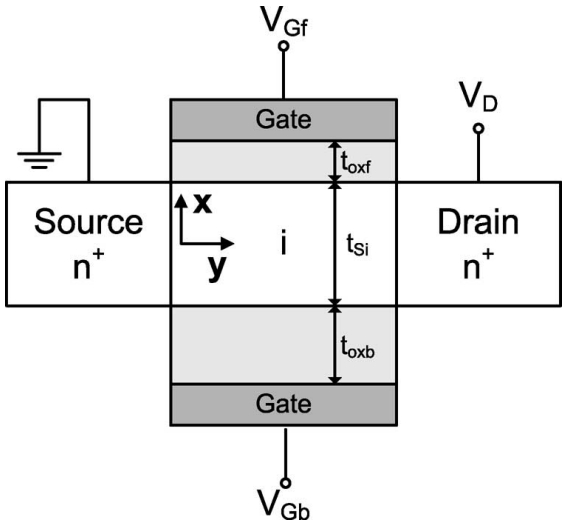

Figure 2 - The generalized asymmetric double gate SOI MOSFET [6].

Asymmetry is defined (Figure 2) as the case where $V_{Gf} \neq V_{Gb}$ and $t_{oxf} \neq t_{oxb}$. In such a case, it is not practical to define the x-axis origin at the center of the silicon. Instead, origin x_0 is taken at the front surface (t_{oxf}/Gf interface) and α, previously defined in (3.9) becomes a key parameter (vice surface potential or charge). After normalization is performed with respect to t_{Si}, ψ_i, and V_i, we arrive at the integral form for an arbitrary distance x_n from x_0:

$$x_n = \int_{\psi_n}^{\psi_{sfn}} \frac{d\psi_n}{\sqrt{\alpha_n + Ke^{(\psi_n - V_n)}}} \tag{3.16}$$

From this, $\alpha_n \equiv \alpha(\beta t_{Si})^2$ is extracted (definitions for K and C_0 are given in [6 p. 136]):

$$\alpha_n = \left(\frac{C_{0f}}{C_{Si}}\right)^2 \left(V_{Gfn} - \psi_{sfn}\right)^2 - Ke^{(\psi_{sfn} - V_n)} \tag{3.17}$$

With a similar result for α_n evaluated from the back gate (f subscripts replaced with b subscripts).

The sign of α_n (positive, negative, or zero) yields three possible solutions for the potential; additionally, two cases exist for the electric field within the silicon film, either it (1) vanishes at some point or (2) is positive everywhere. Combinations of these cases are given below.

3.1.4.1 – α_n Negative with a Nonvanishing Electric Field

The integration of (3.16) for this case presents a solution in $\arcsin(\alpha_n, \psi_i)$ bounding x_n to $[0,1]$. For a nonvanishing electric field within the silicon film, x_n is modeled as equal to 1 leading to the following surface potential expression:

$$1 = \frac{2}{\sqrt{\alpha_n}}\left\{\arcsin\left[\sqrt{-\frac{\alpha_n}{K}e^{(-\psi_{sbn}+V_n)}}\right] - \arcsin\left[\sqrt{-\frac{\alpha_n}{K}e^{(-\psi_{sfn}+V_n)}}\right]\right\} \tag{3.18}$$

3.1.4.2 – α_n Negative with a Vanishing Electric Field

Here, the existence of a point within the silicon film where the potential magnitude maximizes due to the vanishing of the electric field implies the existence of an arbitrary point $x_n = x_{0n}$ such that [6 pp. 136-137]:

$$x_{0n} = \frac{2}{\sqrt{\alpha_n}}\left\{\frac{\pi}{2} - \arcsin\left[\sqrt{-\frac{\alpha_n}{K}e^{(-\psi_{sfn}+V_n)}}\right]\right\} \tag{3.19}$$

Similarly, an expression for $1 - x_{0n}$ in ψ_{sbn} is obtained:

$$1 - x_{0n} = \frac{2}{\sqrt{\alpha_n}}\left\{\frac{\pi}{2} - \arcsin\left[\sqrt{-\frac{\alpha_n}{K}e^{(-\psi_{sbn}+V_n)}}\right]\right\} \tag{3.20}$$

Adding (3.19) and (3.20) yields the following surface potential expression:

$$1 = \frac{2}{\sqrt{\alpha_n}}\left\{\arcsin\left[\sqrt{-\frac{\alpha_n}{K}e^{(-\psi_{sbn}+V_n)}}\right] + \arcsin\left[\sqrt{-\frac{\alpha_n}{K}e^{(-\psi_{sfn}+V_n)}}\right]\right\} \tag{3.21}$$

3.1.4.3 – α_n Positive

Integration of (3.16) for positive α_n yields the following expression:

$$1 = \frac{2}{\sqrt{\alpha_n}}\left\{\operatorname{arcsinh}\left[\sqrt{-\frac{\alpha_n}{K}e^{(-\psi_{sbn}+V_n)}}\right] - \operatorname{arcsinh}\left[\sqrt{-\frac{\alpha_n}{K}e^{(-\psi_{sfn}+V_n)}}\right]\right\} \tag{3.22}$$

3.1.4.4 – α_n is Zero

Integration of (3.16) for $\alpha_n = 0$ yields the following expression:

$$x_n = 2\sqrt{\frac{e^{(-\psi_{sbn}+V_n)}}{K}} - 2\sqrt{\frac{e^{(-\psi_{sfn}+V_n)}}{K}} \tag{3.23}$$

Which is equivalent to analysis of the limit of (3.22) for $\alpha_n \to 0$.

3.1.5 – Asymmetric Models

Two explicit models for the asymmetric drain current were presented in [6]; the results are summarized with reference below:

3.1.5.1 – Ortiz-Conde et al. Model

Calculated in [9], this model follows the same non-approximate evaluation method of (3.5) as seen in (3.6):

$$I_D = \mu \frac{W}{L}\Big\{C_{0f}\left[\left(V_{GF}+\frac{2}{\beta}\right)(\psi_{sfL}-\psi_{sf0})-\frac{1}{2}(\psi_{sfL}^2-\psi_{sf0}^2)\right] + \frac{\varepsilon_s t_{Si}}{2}(\alpha_0 - \alpha_L) + C_{0b}\left[\left(V_{Gb}+\frac{2}{\beta}\right)(\psi_{sbL}-\psi_{sb0})-\frac{1}{2}(\psi_{sbL}^2-\psi_{sb0}^2)\right] - n_i t_{Si} kT(\beta V_D + \exp(-\beta V_D) - 1)\Big\} \quad (3.24)$$

Noting as above that the final bracket term ($n_i t_{Si} kT$ …) is negligible for most practical purposes.

3.1.5.2 – Roy et al. Model

The other explicit model listed by Ortiz-Conde et al. is a semi-empirical expression derived by Roy et al. [10] that incorporates several different regional expressions toward constructing a continuous analytical formulation for a wide range of bias conditions [6 p. 138]:

$$I_D = \mu \frac{W}{L}\Big\{\frac{2}{\beta}(Q_{I0}-Q_{IL})-\frac{(Q_{IL}^2-Q_{I0}^2)}{4C_0} + \left(\frac{4}{\beta}\right)\frac{\varepsilon_s}{t_{Si}}\left(V_{dm}+\frac{1}{\beta}\right)\ln\left[\frac{\beta Q_{IL}}{C_0}+\frac{\varepsilon_s}{C_0 t_{Si}}\left(V_{dm}+\frac{1}{\beta}\right)\right] + \sqrt{2}\left(\frac{1}{2}-\frac{1}{1+\lambda}\right)C_0 V_{dm}^2 \arctan\left(\frac{Q_{IL}}{2\sqrt{2}\beta C_0 V_{dm}^2}\right) - \sqrt{2}\left(\frac{1}{2}-\frac{1}{1+\lambda}\right)C_0 V_{dm}^2 \arctan\left(\frac{Q_{I0}}{2\sqrt{2}\beta C_0 V_{dm}^2}\right)\Big\} \quad (3.25)$$

With $\lambda \equiv \frac{\varepsilon_s/t_{Si}}{\left(\varepsilon_s/t_{Si}+C_0\right)}$ and $V_{dm} \equiv \frac{V_{Gf}-V_{Gb}}{2}$, another instance of gate voltage averaging.

3.1.6 –Computational Efficient Models

As noted especially in the asymmetric cases, the exact equations take forms that while exact to "$10^{-17}V$" [6] are nonetheless somewhat unwieldy for general use. Jurczak et al. [11] present several alternative less rigorous models based on iterated approximations. A summary of these reductions is given with details.

The first simplification introduced is a transformation of the double integral (3.5) into a single integral, albeit still a numerical form not conducive to circuit simulation [12]. Mallikarjan and Bhat [13] next approximated the inversion layer thickness at zero and considered a depletion approximation across the silicon layer resulting in a simplified Kingston function ([11] equations (2) and (8)). Additional separation of device operating regions into (1) source and drain accumulation, (2) source accumulation, drain depletion, and (3) source and drain depletion regions dependent on back gate bias was introduced by [13]. One notable importance of this approach was the removal of integral expressions from drain current descriptions, though the overall model remained numerical.

Continuing analysis of the three operating regions of [13] was performed by Yang and Li [14]. Here, inversion layer charge was approximated as the difference between total semiconductor film charge and the depletion layer charge. Again, results were presented in the three regions defined by [13]. Further work on the back gate depletion region was accomplished by McKitterick and Caviglia [15] who considered the silicon

sheet to be of zero thickness (an extension of [13]'s inversion layer approximation). Again, the overall model remained numerical.

Lim and Fossum [16] presented an analytic model based on several assumptions that lead to less accurate though computationally efficient results. The assumptions are that inversion charge is a linear function and that in strong inversion the surface potential is equal to twice the Fermi potential (a standard MOSFET assumption). Results were presented in each of [13]'s operating regions for both linear and saturation currents:

3.1.6.1 Source/Drain Accumulation

$$I_{D(lin)} = \mu C_{0f} \frac{W}{L}\left[(V_{Gf} - V_{Tf}^{A})V_{DS} - \left(1 + \frac{C_b}{C_{0f}}\right)\frac{V_{DS}^2}{2}\right] \tag{3.26}$$

$$I_{D(sat)} = \mu C_{0f} \frac{W}{L}\frac{1}{2\left(1 + \frac{C_b}{C_{0f}}\right)}\left(V_{Gf} - V_{Tf}^{A}\right)^2 \tag{3.27}$$

Where V_{Tf}^{A} is front gate threshold voltage in accumulation ([11] equation (38)). This assumes, per above, that back surface potential at accumulation is zero.

3.1.6.2 Source Accumulation, Drain Depletion

$$I_{D(lin)} = \mu C_{0f} \frac{W}{L}\left[(V_{Gf} - V_{Tf}^{A})V_{DS} - \left(1 + \frac{C_{bb}}{C_{0f}}\right)\frac{V_{DS}^2}{2} - \frac{C_{bb}}{C_{0f}}V_{DS}\left(V_{Gb}^{A} - V_{Gb}\right) + \frac{C_{bb}C_{0b}}{2C_{0f}C_b}\left(V_{Gb}^{A} - V_{Gb}\right)^2\right] \tag{3.28}$$

$$I_{D(sat)} = \mu C_{0f} \frac{W}{L} \frac{1}{2\left(1 + \frac{C_b}{C_{0f}}\right)} \left[\left(V_{Gf} - V_{Tf}^A\right)^2 - 2\frac{C_{bb}}{C_{0f}} \left(V_{Gf} - V_{Tf}^A\right)\left(V_{Gb}^A - V_{Gb}\right) \right. \\ \left. + \frac{C_{bb}C_{0b}}{C_{0f}C_{bf}} \left(V_{Gb}^A - V_{Gb}\right)^2 \right] \tag{3.29}$$

Where $C_{bf=} \frac{C_{0f}C_b}{C_{0f}+C_b}$ and the A superscript, as before, indicates accumulation.

3.1.6.3 Source/Drain Depletion

$$I_{D(lin)} = \mu C_{0f} \frac{W}{L} \left[\left(V_{Gf} - V_{Tf}\right)V_{DS} - \left(1 + \frac{C_{bb}}{C_{0f}}\right)\frac{V_{DS}^2}{2} \right] \tag{3.30}$$

$$I_{D(sat)} = \mu C_{0f} \frac{W}{L} \frac{1}{2\left(1 + \frac{C_{bb}}{C_{0f}}\right)} \left(V_{Gf} - V_{Tf}\right)^2 \tag{3.31}$$

At this point, we now have a fully analytical and computationally efficient model of the SOI transistor, albeit with some simplifications that reduce its validity in subthreshold, near-threshold, and saturation regions.

Further, per analysis [11 pp. 643-644], it is noted the error for the Lim-Fossum equations is excellent in the above-threshold to sub-saturation region, better even than some numerical models, and this validity combined with the noted computational efficiency leads to the conclusion that this model is sufficient for circuit simulation purposes.

A final modification to the Lim-Fossum model was explored by Jurczak et al. [17]. Identifying the main source of error in the Lim-Fossum model as the assumption of constant front surface potential vice front surface potential dependence on front gate voltage, [17] introduced a correcting analytic front surface potential expression:

$$\phi_{Sf} = 2\phi_F + \frac{1}{\beta}\ln\left|\frac{L_B^2\beta^2}{2}\left[\frac{C_{0f}^2}{\varepsilon_S^2}\left(V_{Gf} - V_{FBf} - 2\phi_F\right)^2 - \alpha\left(\phi_{Sf}, \phi_{Sb}\right)\right] - 2\phi_F + \frac{1}{\beta}\right| \quad (3.32)$$

(Note the Lim-Fossum approximation took (3.32) to be equal to $2\phi_F$).

As no additional numeric forms have been introduced, the revised Lim-Fossum model continues to be analytic. With increased surface potential accuracy, the revised model displays error factor no greater than 0.1 for $\left(V_{Gf} - V_T\right) > 1V$ with increased accuracy in cases that consider back gate accumulation [17 p. 182]. However, as this analytic model continues to not take into account diffusion currents, its accuracy is still poor in the near-threshold region.

3.2 – Double Gate MOSFET

3.2.1 – Introduction

Having considered the specific case of the double gate SOI MOSFET, the standard double gate MOSFET compact model will now be discussed, beginning as before with physically accurate compact models reducing to computationally efficient models from which implementation via BSIM MG will be examined, both for symmetric and asymmetric cases. Device structure may be considered as Figure 2, albeit without the body resting on some insulating layer. No distinction has been made between back gated and fin gated models.

3.2.2 – Symmetric Theory

Taur [18] has developed analytic charge and capacitance models for both symmetric and asymmetric cases from Poisson's equation in one dimension. The symmetric charge/surface potential case is summarized first, originating with the one-dimensional Poisson equation for double gate MOSFETs:

$$\frac{d^2\psi}{dx^2} = \frac{q}{\varepsilon_{Si}} n_i e^{\frac{q\psi}{kT}} \tag{3.33}$$

Integrating the above with symmetric boundary condition $\left.\frac{d\psi}{dx}\right|_{x=0} = 0$ yields:

$$\frac{d\psi}{dx} = \sqrt{\frac{2kTn_i}{\varepsilon_{Si}}\left(e^{\frac{q\psi}{kT}} - e^{\frac{q\psi_0}{kT}}\right)} \tag{3.34}$$

Note the factor of two in the radicand reflects that there are two gates in our system; this factor is inherent in all derived expressions. Integrating again and solving for the symmetric condition $\psi_s \equiv \psi\left(x = \pm\frac{W}{2}\right)$, we arrive at the symmetric case surface potential:

$$\psi_s = \psi_0 - \frac{2kT}{2}\ln\left[\cos\left(\frac{W}{2}\sqrt{\frac{q^2 n_i}{2\varepsilon_{Si}kT}}e^{\frac{q\psi_0}{2kT}}\right)\right] \tag{3.35}$$

Additionally, ψ_s may be expressed as a function of V_G and t_{ox} ([18] equation (5)):

$$\varepsilon_{ox}\frac{V_G - \Delta\phi_i - \psi_s}{t_{ox}} = \pm\varepsilon_{Si}\left.\frac{d\psi}{dx}\right|_{x=\pm\frac{W}{2}} = \sqrt{2\varepsilon_{Si}kTn_i\left(e^{\frac{q\psi}{kT}} - e^{\frac{q\psi_0}{kT}}\right)} \tag{3.36}$$

From these results and some approximations, a relationship between bias and surface potential is obtained. For the approximations $\Delta\phi_i \approx V_T - \frac{E_g}{2q}$ in the neighborhood $\psi_s \approx \frac{E_g}{2q}$ and $\left(e^{\frac{q\psi}{kT}} - e^{\frac{q\psi_0}{kT}}\right) \to 1$, bias may be related to surface potential and charge as (adapted from [18] equation (12)):

$$V_G - V_T = 2\psi_s + \frac{\frac{Q_i}{2}}{C_{ox}} \approx 2\psi_s + \frac{\sqrt{2\varepsilon_{Si}kTn_i}}{C_{ox}} e^{\frac{q\psi_s}{kT}} \tag{3.37}$$

Note the second term, as a function of surface potential, grows much faster than the first. Additionally note this expression is independent of oxide thickness, a property confirmed experimentally for on-state current (but not subthreshold) [18 p. 2864].

3.2.3 – Symmetric Models

Building upon a similarly developed analytic model [19], Cerdeira et al. extend the above theory into a compact model that accounts for variances in mobility, doping, and short channel effect including velocity saturation, DIBL, V_T roll-off, channel-length shortening, and series resistance [20].

3.2.3.1 – Numeric Potential Expressions

An aggressive numerical approach was taken to develop expressions for surface potentials in subthreshold, threshold, and above threshold regions. Culminating in an expression inclusive of all regions by way of averaging per region potentials, [20]

develops a deceptively simple model for center-Silicon potential composed of surface potential ϕ_S and regional potential differences ϕ_d:

$$\phi_0 = \phi_S - \phi_d \tag{3.38}$$

With ϕ_S and ϕ_d as:

$$\phi_S = \phi_{SBT}\frac{1-\tanh[10(V_G - V_T - V)]}{2} + \phi_{SAT}\frac{1+\tanh[10(V_G - V_T - V)]}{2} \tag{3.39}$$

$$\phi_d = \phi_{d1}\frac{1-\tanh[30(V_G - V_T - V)]}{2} + \phi_{d2}\frac{1-\tanh[30(V_G - V_T - V)]}{2} \tag{3.40}$$

Where ϕ_{SBT} is the subthreshold surface potential, ϕ_{SAT} is the surface potential above-threshold, ϕ_{d1} expresses subthreshold potential differences as a function of surface and center potentials, and ϕ_{d2} expresses above-threshold potential differences as a function of surface and center subthreshold, maximum, and at-threshold potentials. More details of each constituent term may be found in [20], equations (6) – (15).

3.2.3.2 – Long Channel Drain Current Model

Beginning with the Pao-Sah integral (3.3) adapted to the double gate MOSFET case:

$$I_{DS} = 2\frac{W}{L}\mu C_{ox}\phi_t \int_{V_S}^{V_D} q_n(V)dV \tag{3.41}$$

First, an approximate expression for V_G is developed toward defining a proper expression for dV, noting that the full expression for q_n was developed via electric field expressions (3), (4), and (18) in [20]:

$$V_G - V_{FB} - 2\phi_F - V - \phi_t \frac{q_b}{2} + \phi_t \ln\left(\frac{1-e^{-\alpha}}{\alpha}\right) \tag{3.42}$$

$$= \phi_t q_n + \phi_t \ln\left[\frac{\alpha_{BT}}{\alpha}\frac{4q_n}{q_b}\left(1+\frac{q_n}{q_b}\right)\right]$$

Note α was note defined; it is assumed to be some fitting parameter. Deriving with respect to V and q and removing "low weight" logarithmic terms [20 p. 1066] yields our expression for dV:

$$dV = -\phi_t\left[1+\left(\frac{1}{q_n}+\frac{1}{q_n+q_b}\right)\right]dq_n \tag{3.43}$$

Substituting (3.43) into (3.41), we have the drain current for a long channel double gate MOSFET:

$$I_D = 2\frac{W}{L}\mu C_{ox}\phi_t^2\left[\frac{q_s^2-q_b^2}{2}+2(q_s-q_d)-q_b\ln\left(\frac{q_s+q_b}{q_d-q_b}\right)\right] \tag{3.44}$$

3.2.3.3 – Variable Mobility Model

Cerdeira et al. [20] selected a surface mobility model from Shirahata [21]:

$$\mu_S = \frac{\mu_0}{\left(1+\frac{\overline{\mathcal{E}}}{\mathcal{E}_1}\right)^{P_1}+\left(\frac{\overline{\mathcal{E}}}{\mathcal{E}_2}\right)^{P_2}} \tag{3.45}$$

Where $\mathcal{E}_i$, P_i are adjusting parameters, μ_0 is maximum mobility, and mean electric field $\overline{\mathcal{E}}$ is equal to:

$$\overline{\mathcal{E}} = \frac{C_{ox}\phi_t}{\varepsilon_S}\left(\frac{q_s+q_d}{2}+\frac{q_b}{2}\right) \tag{3.46}$$

With regard to mobility degradation encountered in velocity saturation, again Shirahata has been selected:

$$\mu = \frac{\mu_S}{\sqrt{1 + \left(\frac{\mu_S V_{D(eff)}}{v_{sat} L}\right)^2}} \tag{3.47}$$

Where $V_{D(eff)}$ is the effective drain voltage.

3.2.3.4 – Short Channel Effects

Both threshold voltage roll-off and DIBL are modeled through a threshold voltage modification obtained by [20] (presumably through numerical methods similar to their potential expressions, though no supporting data is given beyond the final expression):

$$\Delta V_T = 2.2 \cdot \phi_t \left(\frac{t_n}{L}\right)^2 \left(1 - e^{3e6 \cdot L\ (in\ meters)}\right) \ln\left(\frac{N_a}{n_{ia}}\right)\left(1 + \frac{|V|}{39 \cdot \phi_t} - e^{\frac{|V|}{2.5 \cdot \phi_t}}\right) \tag{3.48}$$

Where t_n is the "natural length of symmetric double-gate structures" discussed further in [20]. This adjustment is included in the final short channel effect drain current expression below as $q_{s,d} = (V_G - \Delta V_T)|_{V=0, V_{D(effs)}}$ where $V_{D(effs)}$ is the effective drain voltage in the subthreshold region (defined below).

Effective drain voltages in both above and sub-threshold regions are obtained as functions of the saturation velocity and applied drain voltage as follows:

$$V_{D(effs)} = \frac{V_D}{2}\left[1 - \tanh\left[3\left(1 - \frac{V_G}{V_T}\right)\right]\right] + \frac{V_{D(eff)}}{2}\left[1 - \tanh\left[3\left(1 + \frac{V_G}{V_T}\right)\right]\right] \tag{3.49}$$

$$V_{D(eff)} = V_{sat} + \frac{1}{2}\left[\left(V_D - V_{sat} + \frac{\phi_t}{3}\right)\right. \tag{3.50}$$

$$\left. - \sqrt{\left(V_D - V_{D(sat)} + \frac{\phi_t}{3}\right)^2 + 4\frac{\phi_t}{3}V_{sat}}\right]$$

$$V_{sat} = \frac{\phi_t}{\tau}\left[q_s - q_{sat} + 2\ln\left(\frac{q_s + \frac{q_b}{2}}{q_{sat} + \frac{q_b}{2}}\right)\right] \tag{3.51}$$

Finally, the channel shortening effect is defined as ([20]; again, without supporting details, assuming derivation via the rigorous numerical methods employed in prior cases):

$$\frac{\Delta L}{L} = \lambda\frac{t_c}{L}\left[\ln\left(\frac{L}{t_c}\right) - 1\right]\ln\left[1 + \frac{\mu_0\left|V_D - V_{D(effs)}\right|}{v_{sat}t_c}\right] \tag{3.52}$$

In the above set of short channel effect expressions, two fitting parameters are introduced, τ and λ, both requiring extraction.

3.2.3.5 – Short Channel Drain Current Model

Inclusive of variable mobility and all noted short channel effects, the final numerically derived drain current model proposed by [20] is:

$$I_{DS} \tag{3.53}$$

$$= \frac{2\frac{W}{L}\mu_0 C_{ox}\phi_t^2\left[\frac{q_s^2 - q_b^2}{2} + 2(q_s - q_d) - q_b \ln\left(\frac{q_s + q_b}{q_d - q_b}\right)\right]}{\left(1 - \frac{\Delta L}{L}\right)\left[\left(1 + \frac{\overline{\mathcal{E}}}{\mathcal{E}_1}\right)^{P_1} + \left(\frac{\overline{\mathcal{E}}}{\mathcal{E}_2}\right)^{P_2}\right]}$$

$$\cdot \frac{1}{\left\{\left[\sqrt{1 + \left(\frac{\mu_0 V_{D(eff)}}{v_{sat}L}\right)^2} + 2\frac{W}{L}\mu_0 C_{ox} R\left|V_G - V_T - \left(\frac{1}{2} + \frac{C_s}{C_s + C_0}\right)|V_{D(eff)}|\right|\right]\right\}}$$

From this numerically accurate but computationally inefficient expression, four parameters require extraction: the above-noted τ and λ as well as R and μ_0. [20] notes excellent agreement (exact error not provided) with experimental results and additionally notes the preservation of continuity in the linear/saturation transition region.

3.2.4 – Asymmetric Theory

Prior to extending double gate MOSFET results into computationally efficient models, asymmetric theory (again from Taur [18]) and models will be reviewed. Taur uses a double gate MOSFET model with one gate n^+ type Silicon, the other gate p^+ type Silicon (Figure 3).

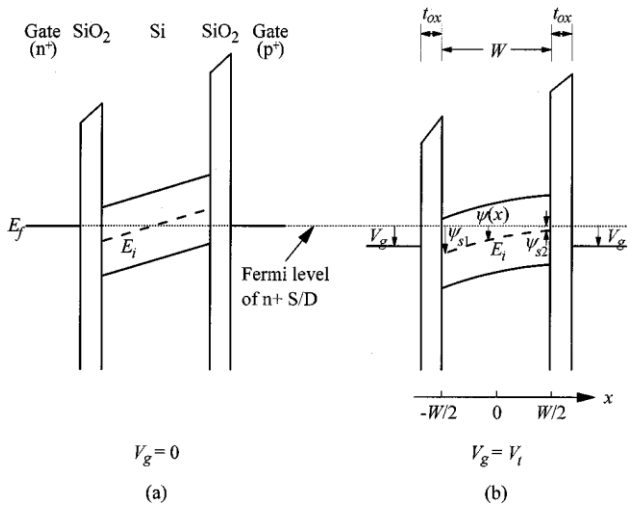

Figure 3 - Asymmetric double gate MOSFET at equilibrium (a) and threshold gate bias (b) [18].

Note that in this model, oxide thickness t_{ox} is the same value for both gates vice the SOI model encountered in [6]. Repeating the integration of (3.33) with asymmetric boundary conditions:

$$\varepsilon_{ox}\frac{V_G-\Delta\phi_2-\psi_{s2}}{t_{ox}}=\varepsilon_{Si}\left.\frac{d\psi}{dx}\right|_{x=\frac{W}{2}}\equiv-\varepsilon_{Si}\mathcal{E}_2 \tag{3.54}$$

$$\varepsilon_{ox}\frac{V_G-\Delta\phi_1-\psi_{s1}}{t_{ox}}=-\varepsilon_{Si}\left.\frac{d\psi}{dx}\right|_{x=-\frac{W}{2}}\equiv\varepsilon_{Si}\mathcal{E}_1 \tag{3.55}$$

Where [18]:

$\Delta\phi_1,\Delta\phi_2$	Work function difference between the left or right gate and intrinsic silicon.
$\psi_{s1}\equiv\psi\left(x=-\frac{W}{2}\right)$	Surface potential at the left oxide interface
$\psi_{s2}\equiv\psi\left(x=\frac{W}{2}\right)$	Surface potential at the right oxide interface
$\mathcal{E}_1$	Electric field at $x=-\frac{W}{2}$
$\mathcal{E}_2$	Electric field at $x=\frac{W}{2}$

Additionally, it is assumed the potential symmetry point shifts from $x = 0$ to some arbitrary $x = x_0$ such that $\frac{d\psi}{dx}\Big|_{x=x_0} = 0$. Equation (3.35) adapts to the asymmetric case as:

$$\psi(x) = \psi_0 - \frac{2kT}{2}\ln\left[\cos\left(\sqrt{\frac{q^2 n_i}{2\varepsilon_{Si}kT}}\, e^{\frac{q\psi_0}{2kT}}(x - x_0)\right)\right] \tag{3.56}$$

Where $\psi_0 \equiv \psi(x - x_0)$, the minimal potential [18]. This solution works for both the case where $x_0 \in \left[-\frac{W}{2}, \frac{W}{2}\right]$ and the case where x_0 is outside the transistor body. However, for low gate bias, the right side of differential equation (3.34) becomes negative as $\psi \to 0$ and the resultant electric field is constant, noted in [18] as $\mathcal{E}_0$:

$$\lim_{\psi\to 0}\frac{d\psi}{dx} = \sqrt{\frac{2kTn_i}{\varepsilon_{Si}}\left(e^{\frac{q\psi}{kT}} - e^{\frac{q\psi_0}{kT}}\right)} = \sqrt{-\frac{2kTn_i}{\varepsilon_{Si}}e^{\frac{q\psi_0}{kT}}} = \sqrt{\mathcal{E}_0^2} = -\mathcal{E}_0 \tag{3.57}$$

$\mathcal{E}_0$ is further approximated as $-\mathcal{E}_0 \approx \frac{\psi_{s2} - \psi_{s1}}{W}$, which when substituted into (3.54) and (3.55) yields:

$$\mathcal{E}_0 = \frac{\Delta\phi_2 - \Delta\phi_1}{W + \frac{\varepsilon_{Si}}{\varepsilon_{ox}}2t_{ox}} \tag{3.58}$$

Substituting (3.58) into (3.57) and integrating, a subthreshold form for $\psi(x)$ is derived:

$$\psi(x) = \frac{2kT}{2}\ln\left\{\frac{\sqrt{\frac{\varepsilon_{Si}}{2kTn_i}}\mathcal{E}_0}{\sinh\left[\frac{q\mathcal{E}_0(x - x_0)}{2kT}\right]}\right\} \tag{3.59}$$

Note that as V_G increases, $\mathcal{E}_0$ decreases until, for some V_{G0}, $\mathcal{E}_0 = 0$ and (3.59) becomes (3.56).

In addition to the asymmetric solutions for surface potential, Taur [18] presents a numerical approximation of V_T based upon the threshold definition $\psi_{s1} = \frac{E_g}{2q}$:

$$V_T \approx \frac{E_g}{2q} + \frac{\frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{ox}}{W + \frac{\varepsilon_{Si}}{\varepsilon_{ox}} 2t_{ox}} \Delta\phi_2 + \frac{W + \frac{\varepsilon_{Si}}{\varepsilon_{ox}} t_{ox}}{W + \frac{\varepsilon_{Si}}{\varepsilon_{ox}} 2t_{ox}} \Delta\phi_1 \tag{3.60}$$

Both (3.60) and (3.59)/(3.56) may be used to extend (3.37) to the asymmetric case.

3.2.5 – Asymmetric Models

Vishvakarma et al. [22] present an analytical model for the double gate MOSFET derived from a two dimensional partial derivative form of the Poisson equation:

$$\frac{\partial^2 \phi(x,y)}{\partial x^2} + \frac{\partial^2 \phi(x,y)}{\partial y^2} = \frac{qN_A}{\varepsilon_{Si}} \tag{3.61}$$

With x-dimension being channel length and y-dimension being channel thickness (opposite the standard dimensional designations). Given the parabolic shape (Figure 3(b)) of charge distribution as a function of y, it is assumed $\phi(x,y)$ is governed by three x-function coefficients $D_1(x) \ldots D_3(x)$ such that:

$$\phi(x,y) = D_1(x) + D_2(x)y + D_3(x)y^2 \tag{3.62}$$

Four boundary conditions are assumed toward the solution of (3.62) [22]:

(1) $\phi_c(x) = \phi(x,y)|_{y=0}$; center potential

(2.a) $\phi_{s1}(x) = \phi(x,y)|_{y=\frac{+t_{Si}}{2}}$; top gate/oxide potential

(2.b) $\phi_{s2}(x) = \phi(x,y)|_{y=\frac{-t_{Si}}{2}}$; bottom gate/oxide potential

(3) $$\varepsilon_{Si}\frac{\partial\phi(x,y)}{\partial y}\bigg|_{y=\frac{+t_{Si}}{2}} = \varepsilon_{ox}\left(\frac{V_{GS1}-\phi_{s1}(x)-\phi_{ms1}}{t_{ox1}}\right)$$

(4) $$\varepsilon_{Si}\frac{\partial\phi(x,y)}{\partial y}\bigg|_{y=\frac{-t_{Si}}{2}} = -\varepsilon_{ox}\left(\frac{V_{GS2}-\phi_{s2}(x)-\phi_{ms2}}{t_{ox2}}\right)$$

First solving the gate/oxide interface potentials, we have [22]:

$$\phi_{s1}(x) = \frac{2\varepsilon_{Si}t_{ox1}\phi_c(x) + \varepsilon_{ox}t_{Si}(V_{GS1}-\phi_{ms1})}{(2\varepsilon_{Si}t_{ox1}+\varepsilon_{ox}t_{Si})} \quad (3.63)$$

$$\phi_{s2}(x) = \frac{2\varepsilon_{Si}t_{ox2}\phi_c(x) + \varepsilon_{ox}t_{Si}(V_{GS2}-\phi_{ms2})}{(2\varepsilon_{Si}t_{ox2}+\varepsilon_{ox}t_{Si})} \quad (3.64)$$

Parabolic coefficients $D_1(x) \dots D_3(x)$ may now be calculated (with organizational variables $g_1 = \frac{\varepsilon_{ox}}{(2\varepsilon_{Si}t_{ox1}+\varepsilon_{ox}t_{Si})}$ and $g_2 = \frac{\varepsilon_{ox}}{(2\varepsilon_{Si}t_{ox2}+\varepsilon_{ox}t_{Si})}$):

$$D_1(x) = \phi_c(x) \quad (3.65)$$

$$D_2(x) = (V_{GS1}-\phi_{ms1})g_1 - (V_{GS2}-\phi_{ms2})g_2 - \phi_c(x)(g_1-g_2) \quad (3.66)$$

$$D_3(x) = \frac{2}{t_{Si}}\left[(V_{GS1}-\phi_{ms1})g_1 + (V_{GS2}-\phi_{ms2})g_2 - \phi_c(x)(g_1+g_2)\right] \quad (3.67)$$

From these and (3.62), $\phi_c(x)$ may be found by taking the partial derivative of (3.62) with coefficients (3.65) – (3.67) with respect to x twice (3.68) and y twice (3.69):

$$\frac{\partial^2\phi(x,y)}{\partial x^2} = \frac{\partial^2\phi_c(x)}{\partial x^2} \quad (3.68)$$

$$\frac{\partial^2\phi(x,y)}{\partial y^2} = \frac{4}{t_{Si}}\left[\left(V_{GS1} - \phi_{ms1}\right)g_1 + \left(V_{GS2} - \phi_{ms2}\right)g_2 - \phi_c(x)\left(g_1 + g_2\right)\right] \tag{3.69}$$

Both expressions may now be substituted into (3.61) and twice integrated to solve for $\phi_c(x)$ (for full derivation see [22]):

$$\phi_c(x) = m - \frac{\Phi_S \sinh\left(K\frac{L}{2}\right) + \Phi_D \sinh\left(K\frac{L}{2}\right)}{\sinh(KL)} \tag{3.70}$$

Where:

$$m = (V_{GS1} - \phi_{ms1})\frac{g_1}{(g_1 + g_2)} + (V_{GS2} - \phi_{ms2})\frac{g_2}{(g_1 + g_2)} - \frac{qN_A t_{Si}}{4\varepsilon_{Si}(g_1 + g_2)}$$

$$\Phi(x) = (V_{GS1} - \phi_{ms1})\frac{g_1}{(g_1 + g_2)} + (V_{GS2} - \phi_{ms2})\frac{g_2}{(g_1 + g_2)} - \phi_c(x) - \frac{qN_A t_{Si}}{4\varepsilon_{Si}(g_1 + g_2)}$$

$$K = \sqrt{\frac{4(g_1 + g_2)}{t_{Si}}}$$

Further, $\Phi(x = 0) = \Phi_S$ and $\Phi(x = L) = \Phi_D$, where L is the channel length.

Assembling all of the above and substituting as appropriate into (3.62), the final asymmetric surface potential derived by [22] is:

$$\begin{aligned}\phi(x,y) = \phi_c(x)\left[1 - (g_1 - g_2)y - \frac{2}{t_{Si}}(g_1 + g_2)y^2\right] \\ + [(V_{GS1} - \phi_{ms1})g_1 - (V_{GS2} - \phi_{ms2})g_2]y \\ + \frac{2}{t_{Si}}[(V_{GS1} - \phi_{ms1})g_1 + (V_{GS2} - \phi_{ms2})g_2]y^2\end{aligned} \tag{3.71}$$

Further analysis by way of imbedded variables was performed to determine an analytic form for V_T, though the solution is not as concise as (3.60) and there was no supporting experimental data to determine if [22]'s V_T was any more precise than [18]'s.

3.2.6 – Computationally Efficient Models

3.2.6.1 – A Computationally Efficient Single Implicit Equation Model

Sahoo et al. [23], recognizing multiple implicit equations in the solutions of asymmetric independent double gate MOSFETs presented by Taur [18] and Oritz-Conde et al. [9], have developed a model based on a single implicit equation. This reduction in implicit equations is shown to increase the computational efficiency of the prior models. [23] presents four surface potential cases derived via two G-factors, functions of applied gate voltage and gate/oxide interface potential, that control the interaction between the four continuous segments of the surface potential profile.

The G-factors and their surface potential cases will be given first followed by a brief demonstration of the functional continuity between the potentials; full derivation of the reproduced functions and variables may be found in [23]. Note that as the surface potential cases are determined by gate bias, expressions are given with respect to this condition.

$$G_1 = \left[-\frac{C_{ox1}}{\varepsilon_{Si}}(V_{GS1} - \psi_1)\right]^2 - Ae^{(\beta\psi_1)} \tag{3.72}$$

$$G_2 = \left[-\frac{C_{ox2}}{\varepsilon_{Si}}(\psi_2 - V_{GS2})\right]^2 - Ae^{(\beta\psi_2)} \tag{3.73}$$

(3.72) generates two $\psi(y)$ cases:

$$\psi(y)|_{G_1>0} = -\frac{2}{\beta}\ln\left\{\sqrt{R_1}\sinh\left[\frac{\beta\sqrt{G_1}}{2}\left(y+\frac{t_{Si}}{2}\right) + \operatorname{arcsinh}\left(\frac{e^{\left(-\frac{\beta\psi_1}{2}\right)}}{\sqrt{R_1}}\right)\right]\right\} \tag{3.74}$$

$$\psi(y)|_{G_1<0} = -\frac{2}{\beta}\ln\left\{\sqrt{-R_1}\sin\left[\frac{\beta\sqrt{-G_1}}{2}\left(y+\frac{t_{Si}}{2}\right) + \arcsin\left(\frac{e^{\left(-\frac{\beta\psi_1}{2}\right)}}{\sqrt{-R_1}}\right)\right]\right\} \tag{3.75}$$

(3.73) generates two $\psi(y)$ cases:

$$\psi(y)|_{G_2>0} = -\frac{2}{\beta}\ln\left\{\sqrt{R_2}\sinh\left[\frac{\beta\sqrt{G_2}}{2}\left(y+\frac{t_{Si}}{2}\right) + \operatorname{arcsinh}\left(\frac{e^{\left(-\frac{\beta\psi_2}{2}\right)}}{\sqrt{R_2}}\right)\right]\right\} \tag{3.76}$$

$$\psi(y)|_{G_2<0} = -\frac{2}{\beta}\ln\left\{\sqrt{-R_2}\sin\left[\frac{\beta\sqrt{-G_2}}{2}\left(y+\frac{t_{Si}}{2}\right) + \arcsin\left(\frac{e^{\left(-\frac{\beta\psi_2}{2}\right)}}{\sqrt{-R_2}}\right)\right]\right\} \tag{3.77}$$

A demonstration of continuity within and between equations (3.74) and (3.77) will now be outlined (full proof asserted in [23]). Beginning with limit functions:

$$\lim_{G_1\to 0}\psi(y) = -\frac{2}{\beta}\ln\left[e^{\left(-\frac{\beta\psi_1}{2}\right)} + \frac{\beta\sqrt{A}}{2}\left(y+\frac{t_{Si}}{2}\right)\right] \tag{3.78}$$

$$\lim_{G_2\to 0}\psi(y) = -\frac{2}{\beta}\ln\left[e^{\left(-\frac{\beta\psi_2}{2}\right)} + \frac{\beta\sqrt{A}}{2}\left(-y+\frac{t_{Si}}{2}\right)\right] \tag{3.79}$$

Thus G_i approach the same limits from both the negative and positive sides of zero. Further, as $\frac{d\psi}{dy}\to 0$, $\psi(y)\to\psi_{1,2}$ depending on gate bias, and for $\frac{d\psi}{dy}=0$, $\psi_1=\psi_2$.

From the shown continuities in both $\psi(y)$ and its derivative, we may conclude the continuity of both $\psi(y)$ and its gate bias forms $G_{1,2}$.

Also noted by [23] was the use of both hyperbolic and trigonometric expressions in their solutions. This implies validity under all bias conditions vice strictly trigonometric solutions previously derived ([9], [18]) that are not valid under all bias conditions.

When computational times for [23] and [18] were compared, the former model resulted in an average improvement factor of five versus the latter [23 p. 635 Fig. 4].

3.2.6.2 – A Drain Current Model and Its Implementation into BSIM-IMG

Lu et al. [24] provide a very basic drain current model of a double gate MOSFET with independent gate bias; the strength of their model is its generality and thus applicability to a range of double gate topographies including SOI FinFET, back gated SOI, and "bulk" FinFET. The device structure is as follows (Figure 4):

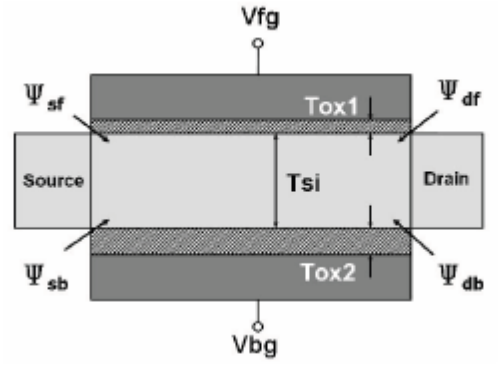

Figure 4 - Core double gate MOSFET structure [24].

The I-V model derives from the charge sheet approximation at the front and back surfaces of the FET:

$$I_D = I_{Df} + I_{Db} \tag{3.80}$$

$$I_{Df} = \mu \frac{W}{L}\left(\frac{q_{Sf} + q_{Df}}{2} + C_{ox1}\frac{kT}{q}\right)\left(\psi_{Sf} - \psi_{Df}\right) \tag{3.81}$$

$$I_{Db} = \mu \frac{W}{L}\left(\frac{q_{Sb} + q_{Db}}{2} + C_{ox2}\frac{kT}{q}\right)\left(\psi_{Sb} - \psi_{Db}\right) \tag{3.82}$$

With subscripts S (source), D (drain), f (front gate), b (back). This model is built on the assumption that inversion charge at the back surface of the FET is negligible; additionally note the use of arithmetic mean to calculate front and back inversion charge.

Given the negligibility of back surface inversion charge, a further simplification may be introduced by assuming significant current conduction at the front surface:

$$I_{DS} = \mu \frac{W}{L}\left(\frac{q_{S(tot)} + q_{D(tot)}}{2}\left(\psi_{Df} - \psi_{Sf}\right) + C_{ox1}\frac{kT}{q}\left(q_{S(tot)} - q_{D(tot)}\right)\right) \tag{3.83}$$

This model, developed for BSIM-IMG (Berkeley Short-channel Insulated gate FET Model, Independent Multi Gate, full specification not yet published), was compared without the use of fitting parameters versus TCAD simulations with favorable results [24 p. 566]. In addition to closely matching I-V and C-V curves, several real-device effects were also captured including V_T roll-off, subthreshold and mobility degradation, and DIBL.

3.3 – Remarks

Double gate models again use gate voltage averaging, though now we see increasingly rigorous compact modeling techniques that seek to accurately replicate device characteristics via well-founded physical and mathematical techniques. Additionally, transitions from long channel to short channel models are seen, relying on short channel effect modulations that amend or expand upon components of long channel expressions. Here are also observed methods of bridging analytic and numerical expressions such that acceptable results are still produced from more computationally efficient expressions. Other common device attributes first seen modeled here include doping and gate coupling, the latter an important effect that increases in impact as devices miniaturize due to reduction in the space between concurrently operating gates.

Incorporation of these second order effects and numeric approximations introduces what will be a recurring challenge, the maintenance of mathematical continuity in the resulting expressions, especially in drain current transition regions where the characteristics migrate from linear to quadratic forms. Maintaining this continuity is required for calculation of additional device characteristics, in particular transconductance. As has been seen, at times this preservation of continuity can be complicated, as with the “single implicit equation” method [23], which while accurate introduces degrees of complication not best suited for computationally efficient models. One widely applicable approach that circumvents this issue while still maintaining

functional continuity is the use of mathematically derived vice physically derived expressions to describe observed device characteristics. Here, and in later devices, we see the use of the general parabola expression as a fundamental continuous function, a convention that yields coefficient parameters useful for software implementation.

Our double gate survey also makes, for the first time, explicit reference to compact modeling software, BSIM-IMG, which is briefly discussed above and is detailed further in Appendix I. Compact models parameterized for this software package allow multi transistor models to be constructed, in the case of [24] and [25] a SRAM cell that was shown to output results consistent with TCAD.

Chapter 4 – Compact Models of Triple Gate MOSFET Topographies

4.1 – Triple Gate FinFET

4.1.1 - Introduction

Literature regarding triple gate structures is limited based on the novelty of such devices and the fact that, as fin-body thicknesses degenerate, top gate current is negligible. In fact, under such conditions, triple gate FinFET devices closely approximate double gate FinFET device and are modeled accordingly. Still, compact models for triple gate devices continue to be developed and have been successfully used in modeling digital applications, particularly SRAM cells.

Of the triple gate FinFETs there are two primary cases, the “true” triple gate, where the gate electric field is perpendicular to some channel segment at all points, and the pi gate, where the gate extends below the channel into the substrate, thus yielding a pseudo-quadruple gate effect [26 pp. 901-902].

4.1.2 –Drain Current Model

Yu et al. [27] have built a unified drain current model for all multiple gate MOSFETs; here, we will examine and extract only the cases for triple and pi gate MOSFETs.

[27] builds a unified drain current model via structural parameters imbedded in a generalized pi gate mobile charge per unit gate length expression $Q_m(\Pi G)$ derived from both double and quadruple gate expressions:

$$Q_m(\Pi G) \approx \frac{1-C_2}{2} Q_m(2G) + \frac{1+C_2}{2} Q_m(4G) \tag{4.1}$$

$$Q_m(2G) = 8\varepsilon_{Si} \frac{W}{t_{Si}} \frac{kT}{q} \beta \tan(\beta) \tag{4.2}$$

$$Q_m(4G) = 8\pi\varepsilon_{Si} \frac{kT}{q} \frac{1-\alpha}{\alpha} [1 + C_1(1-\alpha)] \tag{4.3}$$

Where Q_m is the total mobile charge per unit gate length (a function of V_G and V), $C_{1,2}$ are extractable parameters, and α and β are determined per boundary conditions and also vary per V_G and V [27].

Combining (4.1) – (4.3), the full analytic expression for $Q_m(\Pi G)$ is:

$$Q_m(\Pi G) = (1+C_2) 4\pi\varepsilon_{Si} \frac{kT}{q} \frac{1-\alpha}{\alpha} [1 + C_1(1-\alpha)] \tag{4.4}$$

$$+ (1-C_2) 4\varepsilon_{Si} \frac{H}{t_{Si}} \frac{kT}{q} \beta \tan(\beta)$$

Via the Pao-Sah integral (3.3) [27], we have the final general pi gate drain current expression:

$$I_{DS}(\Pi G) = 4\pi\varepsilon_{Si}\frac{kT}{q}\frac{\mu}{L}(1+C_2)\int_{\alpha_S}^{\alpha_D}[1+C_1(1-\alpha)]\frac{1-\alpha}{\alpha}\frac{dV}{d\alpha}d\alpha \tag{4.5}$$

$$+(1-C_2)4\varepsilon_{Si}\frac{H}{t_{Si}}\frac{kT}{q}\int_{\beta_S}^{\beta_D}\beta\tan(\beta)\frac{dV}{d\beta}d\beta$$

Evaluated:

$$I_{DS}(\Pi G) = 4\pi\varepsilon_{Si}\frac{\mu}{L}\left(\frac{kT}{q}\right)^2(1+C_2)f(\alpha)+C_1 d(\alpha)|_{\alpha_S}^{\alpha_D} \tag{4.6}$$

$$+(1-C_2)4\varepsilon_{Si}\frac{H}{t_{Si}}\left(\frac{kT}{q}\right)^2 p(\beta)|_{\beta_S}^{\beta_D}$$

Where $f(\alpha)$ and $d(\alpha)$ are logarithmic functions and $p(\beta)$ is a function quadratic in β and $\tan(\beta)$ [27].

This form may be further specified to other multi gate cases per parameter substitutions; for our purposes, only the triple gate case will be given (triple gate table extracted from [27], Table I).

Table 1 - Structure parameters for triple gate MOSFETs [27].

Device	H	t_{Si}	t_{ox}	C_1	C_2
$3G$	H	t_{Si}	t_{ox}	C_1	0
ΠG	H	t_{Si}	t_{ox}	C_1	C_2

For the C_2 adjustment, (4.6) condenses to:

$$I_{DS}(3G) = 4\pi\varepsilon_{Si}\frac{\mu}{L}\left(\frac{kT}{q}\right)^2 f(\alpha) + C_1 d(\alpha)|_{\alpha_S}^{\alpha_D} + 4\varepsilon_{Si}\frac{H}{t_{Si}}\left(\frac{kT}{q}\right)^2 p(\beta)|_{\beta_S}^{\beta_D} \quad (4.7)$$

Thus for both pi gate and triple gate MOSFETs, we have long-channel drain current models. We now adapt these models for second order effects.

4.1.3 – Second Order Effect Modeling

Song et al. [28] extend [27] to reflect quantum mechanical, mobility, and short channel effects. The device modeled, while technically a triple gate FinFET, displays double gate FinFET characteristics as the fin height/thickness ratio $\frac{H}{t_{Si}} \to H$; for the experimental device used in [28], these effects were modeled for a ratio of $\frac{H}{t_{Si}} = \frac{60nm}{30nm} = 2$.

4.1.3.1 – Quantum Mechanical Effects and Effective Oxide Thickness

Classical models non-inclusive of quantum mechanical effects significantly overestimate gate capacitance; a correction to inversion layer thickness has been introduced via an empirical model:

$$t_{ox}^{QM} = t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\delta t_{inv} = t_{ox} + \frac{\varepsilon_{ox}}{\varepsilon_{Si}}\left(\frac{7\varepsilon_{Si}\hbar^2}{m^* q Q_i}\right)^{\frac{1}{3}} \quad (4.8)$$

Where δt_{inv} represents the difference between classical and quantum inversion layer thicknesses [28]. It is noted that for quantum effects in height, especially for heights $H < 5nm$, additional confinement effects may arise, though no explicit or qualitative solution for this effect was given. Additionally, it is noted that for experimental device thickness $30nm$, there is no appreciable threshold voltage shift.

4.1.3.2 – Effective Mobility Model and Trends

It was found [28] that the standard phonon scattering-based effective mobility model did not properly describe mobility degradation in low electric field regions; a second Coulomb scattering term was included to account for the difference:

$$\mu_{eff} = \left(\frac{1}{\mu_{eff}^{photon}} + \frac{1}{\mu_{eff}^{Coulomb}} \right)^{-1} \tag{4.9}$$

This inclusion has a stabilizing effect on μ_{eff} as while effective mobility with respect to phonon components varies inversely with electric field, effective mobility with respect to Coulomb scattering varies directly with electric field.

Of additional interest is the phenomenon of electron and hole mobility convergence for short gate lengths; qualitatively described as an effect of relaxed tensile strain in short gate devices, electron mobility degrades while hole mobility enhances. This effect largely disappears for gate lengths below $100nm$. Additional information regarding this phenomenon may be found in references [13] and [14] of [28].

4.1.3.3 – Short Channel Effects

For gate lengths below $100nm$, short channel effects increase in significance; analysis of these effects proceeds from an analytic solution of the 2-D Poisson equation in the subthreshold region [28]:

$$I_{DS} = \frac{\mu_{eff} W \frac{kT}{q}\left(1 - e^{-\frac{qV_{DS}}{kT}}\right)}{\int_0^{L_{eff}} \left\{ \frac{dy}{\int_{-\frac{t_{Si}}{2}}^{\frac{t_{Si}}{2}} \left[n_i e^{\frac{q\psi(x,y)}{kT}} dx \right]} \right\}} \tag{4.10}$$

Where the 2-D analytic potential $\psi(x, y)$ is given by:

$$\psi(x, y) = V_{GS} - \Delta\phi + \cos\left(\frac{\pi x}{\lambda_1}\right) \times \frac{b_1 \sinh\left[\frac{\pi\left(L_{eff} - y\right)}{\lambda_1}\right] + c_1 \sinh\left(\frac{\pi y}{\lambda_1}\right)}{\sinh\left(\frac{\pi L_{eff}}{\lambda_1}\right)} \tag{4.11}$$

With b_1, c_1 first-order coefficients of the 2-D potential and λ_1 is the largest value that satisfies the eigenvalue expression [28]:

$$\tan\left(\frac{\pi t_{ox}}{\lambda_1}\right) \tan\left(\frac{\pi t_{Si}}{\lambda_1}\right) = \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \tag{4.12}$$

DIBL is captured via c_1 dependence (4.11) with explicit expressions for threshold voltage rolloff and subthreshold slope determined as per double gate FinFET methods (Liang and Taur, [29]). Due to removal of higher-order terms, these short channel effect models are less accurate for short effective channel lengths, though it is noted any physical device built to these specifications would suffer too greatly from overall short channel effects to be of practical use [28].

4.1.4 – Compact Model with Parameter Extraction

Chevillion et al. [30] present an alternative triple gate FinFET compact model, also deriving from Liang and Taur's work on double gate FinFETs [29]. [30] takes an aggressive semi-empirical approach to the same effects quantified above [28], resulting

in several extractable parameters. Effect expressions will be presented first followed by a discussion regarding parameters and extraction.

4.1.4.1 – Quantum Mechanical Effects and Threshold Voltage

For reference, the long channel drain current expression cited in [30]:

$$I_{DS} = -q_m^2 + 2q_m + \frac{2C_{Si}}{C_{ox}} \ln\left(1 - \frac{C_{ox}}{2C_{Si}} q_m\right)\Big|_{q_{mS}}^{q_{mD}} \tag{4.13}$$

Where q_m is the normalized mobile charge density and capacitances are per unit area.

Quantum mechanical effects are considered first on threshold voltage via a semi-empirical expression:

$$V_{T0(QM)} = V_{T0} + \frac{E(W_{Si})[1 + g(W_{Si}, V_G)]}{q} \tag{4.14}$$

This expression accounts for variability in $V_{T0(QM)}$ caused by both silicon width (W_{Si}) and gate voltage. Three quantum mechanical effect coefficient functions $\alpha_{qm1,2,3}(W_{Si})$ parameterize $g(W_{Si}, V_G)$ and will be detailed later; $E(W_{Si})$ is defined in [31].

4.1.4.2 – Short Channel Effects

Threshold voltage roll-off and DIBL are likewise represented by semi-empirical expressions as functions of fin width W_{Si}. Modifying parameter γ, first introduced in [31], a general short channel effect relationship is defined:

$$\gamma_i = \left\{\alpha_{i1}(W_{Si})\cosh\left[\frac{\alpha_{i2}(W_{Si})L}{l}\right]\right\}^{-1} \tag{4.15}$$

$$+\,\alpha_{i3}(W_{Si})\left\{1 - 0.000555\left[(L-100) + \sqrt{(L-100)^2}\right]\right\}$$

Where i may be short channel effects or DIBL and l is the natural length (note that l and L are in nanometers) [30]. Note again the use of coefficient functions $\alpha_{ij}(W_{Si})$ in the parameterization of γ_i.

Threshold voltage roll-off is adjusted via both γ_{SCE} and γ_{DIBL}:

$$\Delta V_T = 2\gamma_{SCE}\left(V_{bi} - \phi_f - V_{T0}\right) + \gamma_{DIBL}V_{DS} \tag{4.16}$$

4.1.4.3 – Combined Drain Current Expression

Incorporation of the above quantum mechanical and short channel effects into equation (4.13) yields a model both correct in strong and weak inversion and functionally continuous:

$$I_{DS} = -q_{m0}^2(V_G, V_{ch}) + 2q_m(V_G + \Delta V_T, V_{ch}) \tag{4.17}$$

$$+\,\frac{2C_{Si}}{C_{ox}}\ln\left(1 - \frac{C_{ox}}{2C_{Si}}q_m(V_G + \Delta V_T, V_{ch})\right)\Bigg|_{q_{mS}}^{q_{mD}}$$

Adjustments to q_m and introduction of q_{m0} are covered in [30] and [31]; V_{ch} is the normalized channel voltage.

4.1.4.4 – Parameter Extraction

Per above, the compact model described by [30] relies on a set of parameter functions $\{\alpha_{ij}(W_{Si}): i = QM, SCE, or\ DIBL, j = 1,2, or\ 3\}$. Each α is a polynomial of order 2 with computationally extracted scalar coefficients $c_{ij1\ldots3}$ such that:

$$\alpha_{ij}(W_{Si}) = c_{ij1} + c_{ij2}W_{Si} + c_{ij3}W_{Si}^2 \tag{4.18}$$

The extraction procedure will now be summarized.

Per each technology, three parameter sets are generated for three different fin widths and solved to yield a coefficient set for the entire technology. This is accomplished through a combination of physical simulation data and a set of Python scripts that enable data conversion and computation leading to coefficient extraction. Physical modeling is in three dimensions, initially computed via Silvaco TCAD simulator (commercial software), translated into a format compatible with Verilog-A and IC-CAP (proprietary extraction software developed by the authors of [30]) via Python scripts. After initial coefficient extractions have occurred, a series of routines are initiated that manage execution and timing optimization.

Optimization of each parameter occurs by stepping each coefficient while measuring a certain characteristic under certain conditions to properly isolate, in order, each parameter. Order is determined based on device channel type (long or short channel) and in such a manner that no non-optimized parameter influences any other non-optimized parameter (parameter optimization sequence chart reproduced from [30]):

Table 2 - Optimization hierarchy [30].

Step	Device Size	Characteristic	Condition(s)	Parameter
1	Long channel, all widths	$\log(I_{DS})\ vs. V_{GS}$	Weak Inversion (WI) at low V_{DS}	α_{QM1}
		$I_{DS}\ vs. V_{GS}$	Strong Inversion (SI) at low V_{DS}	$\alpha_{QM2,3}$
		$\log(I_{DS})\ , I_{DS}\ vs. V_G$	Low V_{DS}	$\alpha_{QM1,2,3}$
2	100nm channel, all widths	$\log(I_{DS})\ vs. V_{GS}$	WI at low V_{DS}	α_{SCE3}
			WI at high V_{DS}	α_{DIBL3}
3	Short channel, all widths	$\log(I_{DS})\ vs. V_{GS}$	WI at low V_{DS}	$\alpha_{SCE1,2}$
			WI at high V_{DS}	$\alpha_{DIBL1,2}$
4	Shortest channel, narrow width	$I_{DS}\ vs. V_{DS}$	Saturated at high V_{GS}	v_{sat}

For long channel devices, only quantum mechanical effects require optimization. Of these parameters, QM2 and QM3 only impact strong inversion while QM1 impacts all voltage ranges, thus QM1 is optimized first in weak inversion prior to optimizing QM2 and QM3 in strong inversion (with QM1 held constant per weak inversion results).

For short channel devices, SCE3 and DIBL3 are optimized in weak inversion via a low drain voltage and a high drain voltage, respectively, before simultaneously optimizing the remaining SCE and DIBL parameters under similar bias conditions. Though not explored in depth here (see [30] for full details), v_{sat} is an additional short channel

parameter optimized after all other parameters under high gate bias over the range of drain voltages.

4.1.5 – Qualitative Discussions

Though not presented with the mathematical rigor of previous subjects, two additional triple gate compact modeling topics are here noted.

4.1.5.1 – Threshold Voltage Modeling in Triple- and Pi- Gate Transistors

Ritzenthaler et al. [32] have studied threshold voltage effects in long-channel triple gate MOSFETs. Assuming undoped channels, negligible quantum effects, and subthreshold approximation (negligible carrier concentration) in addition to long channel assumptions and relying on geometric fitting parameters vice explicit solutions of pertaining equations, in particular the 2D Laplace equation, [32] developed a modeling approach that yielded "perfectly adjusted" solutions.

Separating threshold voltage regions per back gate conditions (accumulation, depletion, and inversion), a general model previously developed for thin film SOI [33] has been utilized for triple gate devices. The regional separation acts such that as gate width W decreases, the model shifts from 1D to 2D interface coupling between front and back gates, leading to a gradual reduction of the coupling coefficient (defined by [32] as the slope of the function $V_{TH1}(V_{G2})$). Displaying excellent results (when geometric fitting parameters are introduced) for triple gate MOSFETs, the model is extended to be inclusive of pi gate MOSFETs by considering the 2D potential in the buried oxide overlap

zone. It is also noted this 2D potential allows the pi gate MOSFETs a greater degree of insensitivity to back gate biases due to a reduced coupling coefficient.

4.1.5.2 – Performance variance in Metal Gate FinFETs

O'uchi et al. [34] present a characterization of metal gate FinFETs based on compact model analysis. This analysis is performed for both n- and p-type FinFETs based on a set of sixteen (16) parameters; a brief discussion regarding "parameter extraction fundamentals" is also given.

For the study, n-type TiN gate and p-type Mo gate undoped FinFETs were considered; performance variance was organized based on the following sixteen parameters (reproduced from [34]):

Table 3 - Model parameter list [34].

Parameter (unit, where applicable)	Description
$L_{G(eff)}(nm)$	Effective gate length
$H_{Si}(nm)$	Fin height
$T_{Si}(nm)$	Fin thickness
$T_{ox1}(nm)$, $T_{ox2}(nm)$	Oxide thickness of $G1$, $G2$
k_{ox1}, k_{ox2}	Relative dielectric constants of $G1$, $G2$
$V_{FB1}(V)$, $V_{FB2}(V)$	Flatband voltage of $G1$, $G2$
$\mu_0\left(\frac{cm^2}{V \cdot s}\right)$	Bulk mobility

Parameter (unit, where applicable)	Description
$\alpha_{PH}\left(\frac{cm^{\frac{5}{3}}}{V^{\frac{2}{3}} \cdot s}\right)$	Phonon scattering factor
$\alpha_{SR}\left(\frac{V}{s}\right)$	Surface roughness scattering factor
$v_{sat}\left(\frac{cm}{s}\right)$	Saturation carrier velocity
α_{DIBL}	DIBL factor
$R_S(\Omega \cdot \mu m)$, $R_D(\Omega \cdot \mu m)$	S/D series resistance

Parameter extraction resulted from varying L_G and T_{Si} in fabricated FinFETs; effective oxide thicknesses $T_{ox1}(nm)$, $T_{ox2}(nm)$ and mobility μ_0 were extracted from long-channel devices, saturation velocity v_{sat}, source/drain resistances R_S, R_D, and DIBL factor α_{DIBL} were extracted from short-channel devices. Model calibration followed from these initial extractions [34].

From these variability aware models, produced I_D/V_G curves matched experimentally measured curves and additionally were able to reproduce linear V_T distributions. These results were then extended to FinFET-based SRAM models that likewise successfully modeled fabricated device results.

4.2 – Remarks

This chapter introduces the concept of a unified drain current model based on pi gate characteristics and extensible to many other MOSFET topographies [27]. We shall

return to this model in our analysis of quadruple and cylindrical gate devices as it is one of the best compact modeling utilities available, revealing via parameterization of the pi gate model the symmetries between several topographies.

Also notable is the first occurrence of explicit parameter extraction routines and further qualitative descriptions of each parameter. These parameters, in addition to their utility in compact modeling, were additionally used for classification of n- and p-type triple gate MOSFETs, illustrating a non-traditional but still practical use of compact models. New quantum effect parameters have also been introduced to further extend long channel models into the short channel realm; these effects will increase in importance as our models continue into the short channel and eventually the nano region. Other calculation techniques that bolster a model's continuity and efficiency requirement begin to emerge here as well, in particular the use of geometric fitting expressions vice the physically accurate expressions seen previous. It is noted that these fitting techniques have been selected so as to maintain functional continuity.

It is observed that as FinFET devices miniaturize, the proportional reduction of top gate area versus lateral gate leads to the convention of using double gate models vice triple gate models. This has an additional benefit as, per the absence of this topic in recent literature, the corner current effect, where current in devices where gates meet perpendicular forms prior to forming in the main channels, is no longer discussed as an effect.

Chapter 5 – Compact Models of Quadruple Gate MOSFET Topographies

5.1 – Quadruple Gate MOSFET

5.1.1 – Introduction

With the advent of cylindrical FET topographies (Chapter 6) and their extension to nanowire and nanotube topographies (Chapter 7), the academic and industrial desire to continue development of quadruple gate MOSFET technologies has waned as evidenced by the lack of literature regarding their theory, modeling, and fabrication. As regards their compact models, there is little reference, and that which is made is restricted to articles that summarize all multi gate models vice dedicated publications. In fact, the only quantitative treatment found was given by the Y. Taur research group, already encountered in our analysis of double gate MOSFETs [27] (section 4.1.2 above). This work was likewise presented by another member of the Taur group (Song et al., [35]). Note that below, references common to both [27] and [35] will be referred to as belonging to the "Taur group".

5.1.2 – Surround Gate Theory

The Taur group has derived their quadruple gate model from their surround gate (i.e., cylindrical gate) model. As such, the surround gate theory will first be developed prior to adapting it to the quadruple gate compact model.

[35] constructs a drain current theory from Poisson's equation, evaluated with respect to cylindrical symmetry:

$$\frac{d^2\psi}{d\rho^2}+\frac{1}{\rho}\frac{d\psi}{d\rho}=\frac{q}{\varepsilon_{Si}}n_i e^{\frac{q(\psi-V)}{kT}} \tag{5.1}$$

Solving for ψ, the potential is expressed as:

$$\psi(\rho)=V-\frac{2kT}{q}\ln\left\{\frac{R}{2L_{Di}\sqrt{1-\alpha}}\left[1-\frac{(1-\alpha)\rho^2}{R^2}\right]\right\} \tag{5.2}$$

Where R is the radius of the surround gate device, α is given via solution of:

$$\frac{q(V_G-\Delta\phi-V)}{2kT}-\ln\left(\frac{2L_{Di}}{R}\right)=\ln\left(\sqrt{1-\alpha}\right)-\ln(\alpha)+s\frac{(1-\alpha)}{\alpha} \tag{5.3}$$

And s is the structural parameter for the surround gate MOSFET:

$$s\equiv 2\frac{\varepsilon_{Si}}{\varepsilon_{ox}}\ln\left(1+\frac{t_{ox}}{R}\right) \tag{5.4}$$

Also note surround gate inversion charge density $Q_m(SG)$ is given by:

$$Q_m(SG)=8\frac{\varepsilon_{Si}}{R}\frac{kT}{q}\frac{(1-\alpha)}{\alpha} \tag{5.5}$$

[35] furthers this model to include a drain current expression for surround gate MOSFETs; however, as we already have the general pi gate based drain current model

from (4.6) above, we will first develop an explicit inversion charge expression for quadruple gate MOSFETs before exploring the quadruple gate drain current model.

5.1.3 – Quadruple Gate Model

The Taur group, noting inherent similarities between surround gate and quadruple gate MOSFET topographies (one being a continuous approximation of the discrete other), extends their surround gate theory into a valid compact model for quadruple gate devices.

First, noting that the radius R of a surround gate MOSFET may be made dependent on quadruple gate height to obtain a surround gate device with equivalent cross-sectional area, R now becomes a function of H:

$$R = \sqrt{\frac{t_{Si}H}{\pi}} \tag{5.6}$$

Perimeter difference effects are negated via the following parameterized inversion charge function:

$$\frac{Q_m(4G)}{Q_m(SG)} \approx 1 + C_1(1-\alpha) \tag{5.7}$$

Where $\{\alpha \in (0,1)\}$ such that for $\alpha \to 0$, the device is in above-threshold and for $\alpha \to 1$, the device is in subthreshold. Expressing (5.7) in terms of (5.5), the final form for $Q_m(4G)$ is derived:

$$Q_m(4G) = 8\pi\varepsilon_{Si}\frac{kT}{q}\frac{(1-\alpha)}{\alpha}[1 + C_1(1-\alpha)] \tag{5.8}$$

(For an explanation of the approximation $\frac{1}{R} \to \pi$, see [27 p. 2159]).

From this inversion charge model, integration per the Pao-Sah long-channel drain current equation [27] yields the final quadruple gate drain current expression. However, with our previously established result in expression (4.6) and parameter information available from the Taur group, the same expression may be derived without explicitly evaluating the Pao-Sah integral:

$$I_{DS}(\Pi G) = 4\pi\varepsilon_{Si}\frac{\mu}{L}\left(\frac{kT}{q}\right)^2 (1 + C_2)f(\alpha) + C_1 d(\alpha)|_{\alpha_S}^{\alpha_D} \tag{5.9}$$

$$+ (1 - C_2)4\varepsilon_{Si}\frac{H}{t_{Si}}\left(\frac{kT}{q}\right)^2 p(\beta)|_{\beta_S}^{\beta_D}$$

With quadruple gate parameter information per Taur group:

Table 4 - Structure parameters for the quadruple gate MOSFET [27].

Device	H	t_{Si}	t_{ox}	C_1	C_2
$4G$	H	t_{Si}	t_{ox}	C_1	1

Finally, we arrive at the drain current model for the quadruple gate MOSFET:

$$I_{DS}(4G) = 8\pi\varepsilon_{Si}\frac{\mu}{L}\left(\frac{kT}{q}\right)^2 f(\alpha) + C_1 d(\alpha)|_{\alpha_S}^{\alpha_D} \tag{5.10}$$

With $f(\alpha)$ and $d(\alpha)$ logarithmic functions per [27].

5.2 – Remarks

As previously noted in the chapter introduction, interest in quadruple gate MOSFETs appears to be waning, though not so much that compact model development has completely stopped. Even at the nanoscale level, some degree of interest is maintained as evidenced by the presentation earlier this year at the IEEE AK-MOS workshop of a compact model, still in development and not yet published, for quadruple gate nano-MOSFETs .

Similar to the use of double gate expressions to model triple gate devices, we see here the treatment of the cylindrical gate model to describe the quadruple gate case. As with the triple gate cases, this device symmetry is likewise reflected in the unified model [27].

Chapter 6 – Compact Models of Cylindrical Gate MOSFET Topographies

6.1 – Cylindrical Gate MOSFET

6.1.1 – Introduction

Introduced in the last chapter as a starting point in our analysis of quadruple gate compact modeling, there has been much interest in recent years regarding cylindrical topographies, due in no small part to the proliferation of nanotubes and nanowires as candidates for next-generation FET devices. The final three chapters will deal with these devices, first with standard cylindrical gate (or gate all around, a term here avoided to prevent confusion with quadruple gate devices) MOSFETs before exploring nanowire and nanotube devices. As to what constitutes a standard MOSFET vice a wire MOSFET, I have let the authors of the considered papers define their work as they will and present it as such. Examination of standard cylindrical MOSFETs has been broken into two parts, general and nanoscale.

6.1.2 – General Models

Liu et al. [36] present a general model for cylindrical gate MOSFETs of arbitrary doping. Beginning with the Poisson equation for cylindrical topographies, inclusive of both fixed and mobile charge:

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\phi}{dr}\right)=\frac{qN_a}{\varepsilon_{Si}}\left[e^{\beta(\phi-V_{ch}-2\phi_f)}+1\right] \tag{6.1}$$

Where $=\frac{q}{kT}$, V_{ch} is the quasi-Fermi potential along the channel, and r is the radius of the cylinder. Evaluation of (6.1) with respect to boundary conditions [36 p. 1] yields a complete, though as yet unsolved expression valid for all doping profiles:

$$\frac{1}{2}\left(r\frac{d\phi}{dr}\right)^2=\frac{qN_a}{\varepsilon_{Si}}\int_{\phi_0}^{\phi} r^2 d\phi+\frac{qN_a}{\varepsilon_{Si}\beta}\left[r^2e^{\beta(\phi-V_{ch}-2\phi_f)}-\int_0^r e^{\beta(\phi-V_{ch}-2\phi_f)}dr^2\right] \tag{6.2}$$

For heavy doping ($N_a \geq 10^{17}cm^{-3}$), approximations may be made by neglecting the exponential term in (6.1), simplifying (6.2):

$$\phi(r)=\phi_0+\frac{qN_ar^2}{4\varepsilon_{Si}} \tag{6.3}$$

Due to the unknown solvability of (6.2), the high doping approximation (6.3) was used throughout [36]. Evaluation of the electric field at the silicon-oxide interface follows via differentiation of (6.3) and solution of (6.2):

$$\mathcal{E}_s=\sqrt{\left\{\frac{Q_{dep}}{\varepsilon_{Si}}-\frac{2}{\beta r}[1-e^{\beta(\phi_0-\phi_s)}]\right\}\frac{4}{\beta r}e^{\beta(\phi_s-V_{ch}-2\phi_f)}+\left(\frac{Q_{dep}}{\varepsilon_{Si}}\right)^2} \tag{6.4}$$

Where fixed charge density $Q_{dep}=\frac{qN_ar}{2}$. Taking (6.4) in conjunction with boundary condition $C_{ox}(V_{GS}-\Delta\phi-\phi_s)=Q_{inv}+Q_{dep}=\varepsilon_{Si}\mathcal{E}_s$, we arrive at a normalized equation in terms of inversion charge:

$$V_{GS}-V_{TH0}-\Delta V_{TH}-V_{ch}=\ln\left(Q_{inv}\right)+\ln\left(\frac{1+Q_{inv}}{2Q_{dep}}\right) \tag{6.5}$$

With V_{TH0} and ΔV_{TH} further defined in [36].

At this point, [36] declares a fixing term for Q_{dep} to again align their expressions with both the doped and undoped case:

$$Q'_{dep} = Q_{dep} + \frac{4\varepsilon_{Si}}{rC_{ox}} \tag{6.6}$$

Note that for high Q_{dep}, $Q'_{dep} \rightarrow Q_{dep}$, and for low Q_{dep}, $Q'_{dep} \rightarrow \left(\frac{4\varepsilon_{Si}}{rC_{ox}}\right)$.

Evaluation of the Pao-Sah integral (3.3) for cylindrical topographies follows:

$$I_{DS} = \mu(2\pi r)C_{ox}\left(\frac{kT}{q}\right)^2 Q_{inv}\frac{dV_{ch}}{dy} \tag{6.7}$$

Where dV_{ch} follows from (6.5) and I_{DS} is ultimately expressed in terms of Q_{inv}:

$$I_{DS} = \frac{\mu(2\pi r)}{L}C_{ox}\left(\frac{kT}{q}\right)^2 [f(Q_D) - f(Q_S)] \tag{6.8}$$

With

$$f\left(Q_{inv(D,S)}\right) = -\frac{Q_{inv}^2}{2} - 2Q_{inv} + 2Q'_{dep}\ln\left(Q_{inv} + 2Q'_{dep}\right) \tag{6.9}$$

An extension of this theory to capacitance-voltage characteristics was additionally given [36], based on linear algebraic and partial differential techniques.

6.1.3 – Nanoscale Models

Iniguez et al. [37] jointly model the symmetric double gate MOSFET and cylindrical MOSFET, noting the inherent similarity in their cross-sections (the double gate being a linear extension of its cross-section, the cylindrical gate a rotation). Relying on complex

analytical mathematics and elliptical integrals to explore short channel/quantum mechanical effects, their analysis is not as simple as others encountered and will thus be summarized toward final expressions vice solution techniques.

Long channel devices were considered first. As with [36]'s analysis, a normalized charge expression (6.10) with associated expressions for charge sheet density, with (6.11) and without (6.12) respect to threshold voltage shift ΔV, are developed prior to evaluating drain current:

$$(V_{GS} - \phi_{MS} - V) - \frac{kT}{q}\log\left(\frac{8}{\delta r^2}\right) = \frac{Q}{C_{ox}} + \frac{kT}{q}\log\left(\frac{Q}{Q_0}\right) + \frac{kT}{q}\log\left(\frac{Q+Q_0}{Q_0}\right) \tag{6.10}$$

$$Q = C_{ox}\left\{\frac{2C_{ox}V_{TH}^2}{Q_0} + \sqrt{\left(\frac{2C_{ox}V_{TH}^2}{Q_0}\right)^2 + 4V_{TH}^2\log^2\left[1 + e^{\left(\frac{V_{GS}-V_{TH}+\Delta V_{TH}-V}{2V_{TH}}\right)}\right]}\right\} \tag{6.11}$$

Short channel effects, restricted to discussions regarding 2D double gate analysis in the complex plane expressed via Laplace's equation (with an appropriate Schwartz-Cristoffel elliptical integral coordinate transformation for $(x, y) \leftrightarrow (u, iv)$) and non-determinacy of quantum confinement effects, were not explicitly considered in the initial drift/diffusion (vice ballistic; see below) drain current model:

$$I_{DS(DD)} = W\mu Q(x)\frac{d\phi_F(x)}{dx} \tag{6.12}$$

Evaluated with respect to cylindrical topography:

$$I_{DS(DD)} = \frac{\mu(2\pi r)}{L}\left[\frac{2kT}{q}(Q_S - Q_D) + \frac{Q_D^2 - Q_S^2}{2C_{ox}} + \frac{kT}{q}Q_0\log\left(\frac{Q_D+Q_0}{Q_S+Q_0}\right)\right] \tag{6.13}$$

Where $Q_0 = \left(\frac{4kTC_{ox}}{q}\right)$ and $Q_{S,D}$ are evaluated via (6.11).

Beyond drift/diffusion current (6.13), nanoscale effects (distinct from quantum effects) of small (less than $50nm$) cylindrical devices must be considered; [37] introduces consideration of ballistic current effects, a nanoscale aspect that will become more and more prevalent as we discuss nanowire and nanotube devices. In the case of cylindrical topographies, the ballistic current is modeled as [37]:

$$I_{DS(B)} = \frac{qkT}{\pi\hbar}\sum_{v}\sum_{n} g_v \ln\left[\frac{1+e^{\left(\frac{E_{F(S)}-E_n^v(x_{max})}{kT}\right)}}{1+e^{\left(\frac{E_{F(D)}-E_n^v(x_{max})}{kT}\right)}}\right] \tag{6.14}$$

Where $E_{F(S,D)}$ are the Fermi levels at source/drain, respectively. The backscattering component of the ballistic effect is also considered for carrier reflections within long channels of length l_{kT}, the distance over which the channel potential drops by $\left(\frac{kT}{q}\right)$ from the height of the barrier [37 p. 2134]. Backscattering is modeled as:

$$r_{bs} = \frac{l_{kT}}{l_{kT}+\lambda} \tag{6.15}$$

Where λ is the mean free path of backscattering.

Thus the ballistic drain current model for a nanoscale cylindrical MOSFET, with respect to backscattering, may be expressed as:

$$I_{DS(bal)} = (1-r_{bs})I_{DS(B)} \tag{6.16}$$

From which we finally arrive at a cumulative drift/diffusion/ballistic drain current expression:

$$I_{DS} = I_{DS(DD)} + I_{DS(bal)} \tag{6.17}$$

6.2 – Remarks

Here, we note the first appearance of ballistic effects. These effects will be of continuing importance for the rest of this survey, eventually dominating before entirely replacing drift/diffusion current. While physically this yields much higher current results, computationally it introduces difficulties as expressions come to rely on discrete summations vice continuous integrals. An additional effect introduced by ballistics, particularly in long (i.e., greater than the carrier phase breaking mean path) devices is backscattering.

Symmetrically, it is notable that in cross section cylindrical devices are identical to double gate devices, implying the possibility that all models for each topography may be adaptable to the other. Further, the natural reduction of the three dimensional cylindrical topography to the one dimensional nanowire topography is implied, a topic to be fully explored in the next chapter.

As regards further research, [36] notes that as yet there has been no solution to (6.2) for a general doping profile.

Chapter 7 - Compact Models of Nanowire MOSFET Topographies

7.1 – Nanowire MOSFET

7.1.1 – Introduction

At some indeterminate point, a combination of scale and the shift in dominant current from drift/diffusion to ballistic necessitates the introduction of the 'nanowire' classification into MOSFET analysis. At present a popular topic (based on paper volume, at least on par if not superseding research on double gate devices), nanowire devices represent an area of analysis where traditional, solid-state methods of modeling give way to ballistic modeling, in whole or in part, as has already been seen in our analysis of cylindrical MOSFETs (section 6.1.3). Here, a transition will be observed from strictly solid state models that model ballistics indirectly to models more explicit in their treatment of ballistic effects, presaging analysis of nanotube devices in chapter 8 where ballistic effects dominate. Following inspection of these models, parameter extraction and SPICE compatibility will be explored.

7.2 – Solid-State Nanowire MOSFET Models

7.2.1 – Introduction

Within strictly solid-state nanowire MOSFET models, there are two distinct device topographies, cylindrical gate devices where the gate surrounds the body, and omega gate devices, where the gate partially surrounds the body. Two cylindrical cases will be presented, the first a familiar treatment based on previous work from Liu et al. [36], here extended to the nanowire case. The second, presented by Ray and Mahapatra [38], derives as [39] but with different boundary conditions. [38]'s analysis is then extended to the omega gate case, followed by a qualitative analysis of both cases (Tang et al. [40]).

7.2.2 – Solid-State Cylindrical Gate Nanowire Models

7.2.2.1 – Liu et al.

Continuing their work on cylindrical gate MOSFETs , Liu et al. [39] first build a cylindrical gate nanowire model inclusive of doping and "advanced physical effects" before extending their model for practical implementation in circuit simulation via Verilog-A. Starting with the Poisson equation for 3D silicon nanowire structures, body potential is first derived with drain current following via the Pao-Sah integral. First, the Poisson equation for nanowire devices:

$$\frac{1}{r}\frac{d}{dr}\left(r\frac{d\phi}{dr}\right)+\frac{d^2\phi}{dy^2}=\frac{1}{L_D^2}\left[e^{(\phi-V_{ch}-2\phi_f)}+1\right] \tag{7.1}$$

Note here all potentials are normalized by thermal voltage β and all charges are normalized by $\left(\frac{\beta}{C_{ox}}\right)$ with L_D^2 the Debye length; all other quantities as they were in 6.1.2.

A charge density expression with respect to initial conditions ([39], equations (2a) and (2b)) follows:

$$V_{GS}-\left(V_{T0}+\Delta V_{T(NW)}\right)-V_{ch}=Q_{in}+\ln(Q_{in})+\ln(1+H\cdot Q_{in}) \tag{7.2}$$

Where, due to the geometry of nanowires, new terms have been introduced; $\Delta V_{T(NW)}$ is additional threshold voltage and $H=e^{\left(-\Delta V_{T(NW)}\right)}$ describes the "transistor volume inversion effect" seen in strong inversion [39 pp. P-9-2]. From this expression derive differential values required in the Pao-Sah integral (3.3) for nanowire devices:

$$I_{DS}=\frac{\mu(2\pi r)}{L}\frac{C_{ox}}{\beta^2}\int_{Q_S}^{Q_D}Q_{in}\frac{dV_{ch}}{dQ_{in}}dQ_{in} \tag{7.3}$$

Which evaluates as:

$$I_{DS}=\frac{\mu(2\pi r)}{L}\frac{C_{ox}}{\beta^2}\left[\frac{-Q_{in(x)}^2}{2}-2Q_{in(x)}+\frac{\ln\left(1+H\cdot Q_{in(x)}\right)}{H}\right]\Bigg|_{Q_{in(S)}}^{Q_{in(D)}} \tag{7.4}$$

[39] continues this analysis to a straightforward derivation of transconductance and additionally presents a linear algebraic/partial differential method of capacitance modeling deriving from (7.4) above.

Advanced physical effect models follow; short channel effects are described via an α parameter that effects both inversion charge and threshold voltage:

$$\alpha = 1 + 2\left[\frac{1}{2\cosh\left(\frac{L}{2\lambda}\right) - 2}\right] \tag{7.5}$$

Changing (7.2) as:

$$\frac{V_{GS} - \left(V_{T0} + \Delta V_{T(NW)} + \Delta V_{T(SCE)}\right) - \alpha V_{ch}}{\alpha} = \frac{Q_{in}}{\alpha} + \ln(Q_{in}) + \ln(1 + H \cdot Q_{in}) \tag{7.6}$$

With $\Delta V_{TH(SCE)}$ threshold voltage change due to short channel effects further described in [39 pp. P-9-3]. This alters (7.4) as:

$$I_{DS} = \frac{\mu(2\pi r)}{L}\frac{C_{ox}}{\beta^2}\left[\frac{-Q_{in(x)}^2}{2\alpha} - 2Q_{in(x)} + \frac{\ln\left(1 + H \cdot Q_{in(x)}\right)}{H}\right]\Bigg|_{Q_{in(S)}}^{Q_{in(D)}} \tag{7.7}$$

Though not explicitly modeled as in later examples, ballistic current is accounted in an effective inversion charge expression that is also inclusive of velocity saturation and overshoot that operates via fitting parameters n and m; note this non-explicit ballistic term is continuous vice previous discrete expressions:

$$Q_{in(eff)} = \sqrt[m]{\left[\frac{Q_{D,S}}{1 + 2\beta n v_{sat}\frac{L}{\mu}\left(2n + k_{sat,iv}Q_{D,S}\right)}\right]^m + (Q_{in})^m} \tag{7.8}$$

Quantum effects were likewise considered, in particular effects on gate capacitance [39 pp. P-9-4] and channel voltage:

$$V_{ch(QM)} = V_{ch} + \frac{\lambda_q \hbar^2 \pi^2}{4 q m_e r^2} \tag{7.9}$$

7.2.2.2 – Ray and Mahapatra

Ray and Mahapatra [38] leverage partial differential techniques across a system of equations to explicitly model body potential in a cylindrical nanowire MOSFET. Included here due to its techniques and intuitive approach to boundary conditions, it does not go as far as [39] in developing its model though it does lead into additional discussions of omega gate nanowire devices.

Starting again with the Poisson equation for nanowire devices:

$$\nabla^2 \Psi(r,x) = \frac{q}{\varepsilon_{Si}} n_i e^{\frac{\Psi(r,x) - \Psi_F}{U_T}} \tag{7.10}$$

[38] considers a general partial differential solution split into three pieces with appropriate boundary conditions:

$$\Psi(r,x) = \Psi_0(r) + \Psi_L(r,x) + \Psi_N(r,x) \tag{7.11}$$

Where $\Psi_0(r)$ is the long channel potential profile, $\Psi_L(r,x)$ is the Laplacian with regard to all boundary conditions and $\Psi_N(r,x)$ models all remaining nonlinear aspects with boundary conditions at zero. Boundary conditions are as follows (Figure 5):

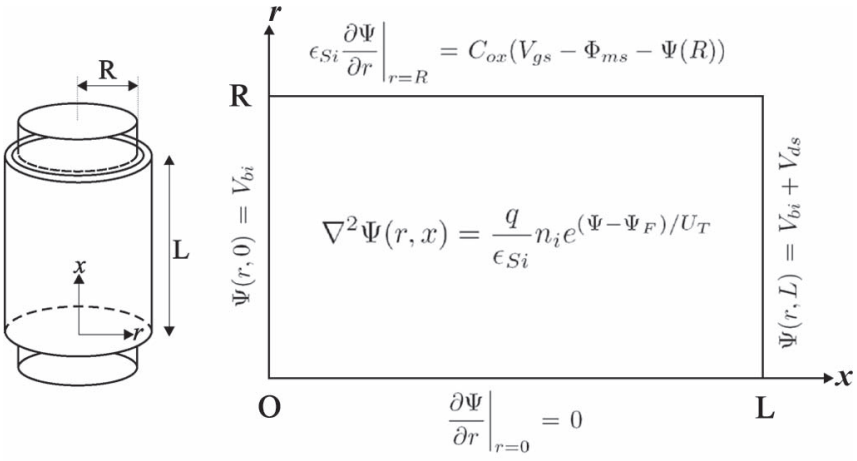

Figure 5 - Cylindrical nanowire MOSFET schematic and boundary conditions for (7.10), (7.11) [38].

[38 pp. 2410-2411] presents a detailed solution of the resulting set of equations; the final forms of each segment of (7.11) is presented below:

$$\Psi_0(r) = U_T \ln\left[\frac{8B}{\delta(1 - Br^2)^2}\right] \tag{7.12}$$

$$\Psi_{\mathrm{L}}(r,x) = \sum_{n=1}^{\infty}\left\{A_n \sinh\left(\frac{\mu_n x}{R}\right) + B_n \sinh\left[\frac{\mu_n(L-x)}{R}\right] \times J_0\left(\frac{\mu_n r}{R}\right)\right\} \tag{7.13}$$

$$\Psi_{\mathrm{N}}(r,x) = [\Psi_{\mathrm{L}}(r,x) - V_0]\left\{\frac{\cosh\left[P\left(\frac{L}{2} - x\right)\right]}{\cosh\left(\frac{PL}{2}\right)} - 1\right\} \tag{7.14}$$

With constituent functions and variables as per [38]. Additional short channel and quantum effects are discussed in both qualitative and quantitative terms.

7.2.3 - Solid-State Omega Gate Nanowire Models

Ray and Mahapatra continue their analysis of cylindrical nanowires to the omega gate case (Figure 6), where the gate does not fully surround the cylindrical body [41]:

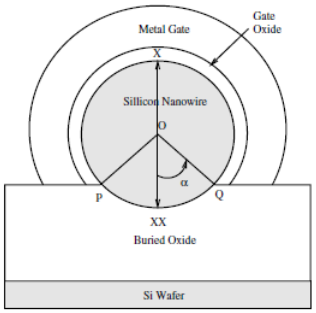

Figure 6 - Omega gate cylindrical nanowire MOSFET schematic [41].

Specifically focusing on threshold voltage modeling, [41] nonetheless derives a surface potential model via methods similar to their cylindrical gate analysis above (7.10). Initially considering two surface potential regions, $\Psi_1(r)$ for the gate-covered region and $\Psi_2(r)$ for the uncovered region (for potential solution details, see [41 pp. 447-450]):

$$\Psi_1(r) = V_T \log\left[\frac{8B}{\delta(1-Br^2)^2}\right] \tag{7.15}$$

$$\Psi_2(r,\theta) = \lambda_n g(\theta) r^{2k} e^{-2Br^2} M(k+1, 2k+1, 4Br^2) \tag{7.16}$$

Where λ_n is a normalizing parameter, M is Kummer's function of the first kind, and all other functions are defined per [41 pp. 448-449]. Parameter k is a constant determined by angle α above:

$$k = \frac{\pi}{4\alpha} \tag{7.17}$$

Thus for $\alpha = \frac{\pi}{4}$ radians, $k = 1$ and (7.16) reduces to (after parameter change $z = 2Br^2$):

$$\Psi_2(z = 2Br^2, \theta) = \frac{\lambda_n}{2B} g(\theta) \left[e^z - \frac{\sinh(z)}{z} \right] \tag{7.18}$$

From here, threshold voltage modeling follows from inversion charge and oxide capacitance calculations:

$$V_T = V_{FB} + \frac{E_G}{2} + \frac{Q}{C_{ox}} \tag{7.19}$$

Surface charge density is presented below for the cases $\alpha = \frac{\pi}{4}$ and $z = 2Br^2$ with surface charge following from Gauss's law:

$$Q_T = \varepsilon_{Si} \oint_S \mathcal{E} \cdot dS \tag{7.20}$$

With surface charge density on a cylindrical surface as:

$$Q = \frac{Q_T}{2\pi RL} = \frac{\varepsilon_{Si}}{2\pi} \int_0^{2\pi} \mathcal{E} \cdot d\theta \tag{7.21}$$

Thus we have our charge expression, here simplified per $\alpha = \frac{\pi}{4}$ and $z = 2Br^2$ (for general solution, see [41] equation (21)):

$$Q = \frac{2\varepsilon_{Si} V_T}{R} \left[\frac{z}{\left(1 - \frac{z}{2}\right)} + \frac{\lambda C R^2}{2\pi z} [z e^z - \cosh(z)] + \frac{\sinh(z)}{z} \right] \tag{7.22}$$

Finally, oxide capacitance, here noted per its relation to threshold voltage, is likewise evaluated per $\alpha = \frac{\pi}{4}$ (adapted from the general solution, [41] equation (24)):

$$C_{ox} = \frac{4\varepsilon_{ox}}{3R \log\left(1 + \frac{t_{ox}}{R}\right)} \tag{7.23}$$

7.3 – Ballistic Nanowire MOSFET Models

7.3.1 – Introduction: The Landauer Formalism

Per researched literature, the contemporary method for evaluation of ballistic current derives from a 1957 proposal by Rolf Landauer [42] [43]. Known as the Landauer formalism, it posits that conduction in a one dimensional system, such as nanowires or nanotubes, may be constructed as a transmission problem. Specifically, it leads to a formulation of ballistic current as a function of transconductance and applied voltage:

$$I_{bal} = GV \tag{7.24}$$

Applied to a system of two contacts terminating a one dimensional channel ($L \leftrightarrow R$) and considering current due to probabilities of transmission ($I_R^{\rightarrow}$) and reflection ($I_L^{\leftarrow}$) for an electron ($I_L^{\rightarrow}$) transiting this channel, we have the following current expressions:

$$I_{bal} = I_L^{\rightarrow} - I_L^{\leftarrow} = I_R^{\rightarrow} = \frac{2q^2}{h} M\tau \frac{\left(E_{f(L)} - E_{f(R)}\right)}{q} \tag{7.25}$$

Where M is a function of intra-contact energy $E \in \left[E_{f(L)}, E_{f(R)}\right]$ that determines carrier energy, τ is the carrier transmission probability, and $E_{f(i)}$ is the Fermi level at the left/right contact, respectively (in practice, this becomes source/drain). Specifically, G in (7.24) is as:

$$G = \frac{2q^2}{h} M\tau \tag{7.26}$$

And is known as the Landauer formula.

The Landauer formalism holds as long as the length of the active channel is less than the phase-breaking mean path, a requirement known as "coherence," and the transmission probability τ can be calculated from Schrodinger's equation or the WKB approximation [43] [44]. It will be noted when this formalism is assumed in modeling of ballistic effects.

7.3.2 – Ballistic Double and Cylindrical Gate Nanowire Models

7.3.2.1 – Natori

Natori [45] explores two related nanowire MOSFET topographies, the already encountered cylindrical topography and an adapted double gate device where a nanowire is imbedded between two parallel planar gates (which may or may not be the same distance from the nanowire). He makes no effort to differentiate the two devices and treats model result as applicable regardless of gate topography.

From the Landauer formalism, [45] begins his analysis of ballistic drain current under drain bias as:

$$I_D = \frac{q}{\pi\hbar}\sum_i \int \left[f\left(E, E_{f(S)}\right) - f\left(E, E_{f(D)}\right)\right] T_i(E)\, dE \qquad (7.27)$$

With $f\left(E, E_{f(S,D)}\right) = \frac{1}{1+e^{\left(\frac{E-E_{f(S,D)}}{kT}\right)}}$ where E is energy, $E_{f(S,D)}$ is the Fermi level at source and drain, respectively, and summation over i represents contributions from the i^{th} subband and $T_i(E)$ is the carrier transmission probability coefficient for the i^{th}

subband. Two cases are fully evaluated, that where the maximum subband energy is less or near mobility, and that where the maximum subband energy is much larger than mobility; the latter is assumed for the duration of our analysis and is given below:

$$I_D = G_0 \frac{kT}{q} \sum_i g_i \ln \left[\frac{1 + e^{\left(\frac{E_{f(S)} - E_{i0}}{kT}\right)}}{1 + e^{\left(\frac{E_{f(D)} - E_{i0}}{kT}\right)}} \right] \tag{7.28}$$

Where G_0 is quantum conductance (taken as $\frac{2q^2}{\hbar} = 77.8\mu S$) and g_i represent conductance degeneracy in the i^{th} subbands. E_{i0} is the minimum energy of the i^{th} subband at channel terminals. (7.25) is further analyzed with regard to electrostatics toward evaluation of $\left(E_{f(S,D)} - E_{i0}\right)$. The results of this analysis, with additional consideration of internal capacitances and several work functions [45 pp. 2879-2880], lead to the final drain current expression:

$$I_D = G_0 \frac{kT}{q} e^{\left(\frac{E_{f(S)} - E_{f(0)}}{kT}\right)} \sum_i g_i \left[e^{\left(\frac{E_{f(0)} - E_{i0}}{kT}\right)} - e^{\left(\frac{E_{f(0)} - E_{i0} - qV_D}{kT}\right)} \right] \tag{7.29}$$

Where $E_{f(0)}$ is the bottom energy of the lowest subband. Additionally, $E_{f(S)} - E_{f(0)}$ may be approximated as $\left[\frac{q}{\alpha}(V_G - V_T)\right]$ where $\alpha = \left(1 + \frac{C_p}{C_G}\right)$, with C_p and C_G internal capacitances. In the case where $C_p \to 0$, $E_{f(S)} - E_{f(0)} \to q(V_G - V_T)$.

Natori continues analysis of short channel effects and their effect upon charge and threshold voltage; he further presents an analysis of quantum capacitance. To explicitly

state the Fermi relation with respect to gate and threshold voltage discussed above, we begin with:

$$(V_G - V_T) - \frac{\alpha}{q}\left(E_{f(S)} - E_{f(0)}\right) = 0 \tag{7.30}$$

In real cases, this difference is nonzero, modeled in [45] as $|Q'| = |Q| + \Delta Q$; effects of this addition are now incorporated in the calculation of V_T:

$$\left[V_G - \left(V_T - \frac{\Delta Q}{C_G}\right)\right] - \frac{\alpha}{q}\left(E_{f(S)} - E_{f(0)}\right) = \frac{|Q'|}{C_G} \tag{7.31}$$

An adaptation to subthreshold modeling is additionally presented [45 p. 2881].

Finally, an analysis of quantum capacitance, leading to an expression of $\frac{d|Q|}{dV_G}$, is presented, though is disregarded here as it has yet to be included in any compact model.

7.4 – Nanowire Compact Model Implementation and Parameter Extraction

7.4.1 – Introduction

Yang et al. [46] (an extension of Liu et al. [39]) successfully implemented their cylindrical nanowire MOSFET model into Verilog-A so as to best model analog functions; a qualitative description of their model and its extension to circuit modeling is given. More in-depth, quantitative presentations of compact model implementation, regarding both parameter extraction and SPICE compatibility, are also included.

Ortiz-Conde et al. [47] present a double-integral method toward better drain current parameter extraction, though only extending their analysis to a regional single gate drain current compact model. It is recent enough to elicit mention, though limited such that we will not explore it in-depth. Though not explicitly noted by the authors, the nanowire parameter extraction techniques developed in [47] may be extensible to multi gate cases.

Of additional interest is the work of Lee et al. [48], which implements a single planar gate nanowire compact model into SPICE. Again, while not a true multigate model, their methods provide a starting point and introduce the convention of modeling nanowire/metal source/drain contacts as Schottky diodes with barrier functions constructed with respect to nanowire potential. This technique will be seen again in our analysis of carbon nanotube structures.

7.4.2 – SPICE Model of a Single Planar Gate Nanowire MOSFET

[48] considers a device where a nanowire is terminated with metal contacts with a single planar polysilicon gate controlling nanowire potential, here modeled as a set of source/drain Schottky diodes with an n-type single gate MOSFET between (Figure 7):

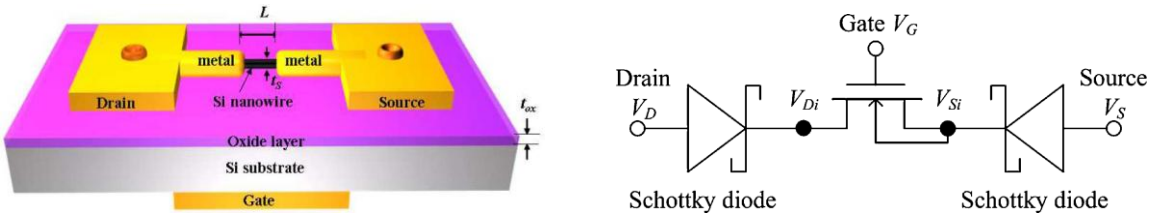

Figure 7 - (Left) Schematic of a single planar gate nanowire MOSFET. (Right) Equivalent circuit [48].

A set of five expressions describe Schottky diode current in reverse bias:

$$I_D = SJ_S e^{\left(\frac{-qV}{\varepsilon'}\right)} \tag{7.32}$$

$$\varepsilon' = E_{00}\left[\frac{E_{00}}{kT} - \tanh\left(\frac{E_{00}}{kT}\right)\right] \tag{7.33}$$

$$J_S = \frac{A^* T^2 \sqrt{\pi E_{00}}}{kT} \sqrt{-qV + \frac{\phi_B}{\cosh\left(\frac{E_{00}}{kT}\right)}}\, e^{\left(-\frac{\phi_B}{E_0}\right)} \tag{7.34}$$

$$E_{00} = \frac{\hbar}{2\sqrt{\frac{N_d}{m^* \varepsilon_S}}} \tag{7.35}$$

$$E_0 = E_{00} \coth\left(\frac{E_{00}}{kT}\right) \tag{7.36}$$

Where V is the voltage drop across the Schottky diode(s), S is the diode area, and A^* is the Richardson constant [48]. Schottky barrier lowering is modeled as:

$$\phi_B = \phi_{B0} - q\sqrt{\frac{q\mathcal{E}_{max}}{4\pi\varepsilon_S}} \tag{7.37}$$

Determination of the maximum electric field $\mathcal{E}_{max}$ requires solution of the Poisson equation. As the three dimensional equation is too difficult to solve analytically for this topography, a one dimensional estimate is used instead:

$$\frac{d^2\Phi}{dx^2} - \frac{\Phi(x) - V_G + V_{bi}}{\lambda^2} = \frac{qN_d}{\varepsilon_S} \tag{7.38}$$

Where λ is the effective screening length [48]. Estimating $\Phi(x)$ via a standard parabolic function, a solution is achieved (equation (8), [48]) with electric field extracted via negative differentiation (equation (9), [48]). From this, $\mathcal{E}_{max}$ follows, parameterized per the parabolic estimation of $\Phi(x)$:

$$\mathcal{E}_{max} = C_1 V_{DS} + C_2 V_{GS} + C_3 \tag{7.39}$$

Where C_i are fitting parameters. Substituting (7.36) into (7.34), we have the final parameterized form of the Schottky barrier lowering expression:

$$\phi_B = \phi_{B0} - \sqrt{AV_{DS} + BV_{GS} + C} \tag{7.40}$$

Where $A = \frac{q^3 C_1}{4\pi\varepsilon_S}$, $B = \frac{q^3 C_2}{4\pi\varepsilon_S}$, and $C = \frac{q^3 C_3}{4\pi\varepsilon_S}$. With this Schottky diode model, inclusive of effects induced by the connected nanowire, the equivalent circuit nanowire MOSFET model (Figure 7) may be built and evaluated via SPICE.

7.5 – Remarks

In nanowires, the transition from solid state to ballistic effects occurs. Beginning with solid state models derived from the reduction of cylindrical models, ballistic effects, when included, are modeled as continuous functions allowing for further differential

analysis. In cases where ballistic effects are equivalent to or dominate solid state effects, the Landauer formalism dictates ballistic interactions.

Even with this shift, modeling techniques common to other previous devices are still observed. Parabolic parameterization of quantities continues as does the reliance on the Poisson equation, albeit now calculated per nanowire conditions.

As nanowires exhibit several short channel/quantum effects, these, too, have been explored in increasing detail as they come to dominate. Noted nanoscale effects include weak dependence on temperature and the rise of quantum conductance in parallel with dominance of ballistic current [45].

With regard to fabrication realities, the omega gate case has been explored as an extension of the cylindrical gate topography with particular attention given to the 0.75 coverage gate. This topography has been noted by others [40] as closely approximating the characteristics of cylindrical gates, especially in the $(0.7 - 0.8)$ coverage range.

As before, software implementable compact models again have been modulated per nanoscale effects with new extraction techniques being developed to cope with nanodevice measurements [47]. A unique method of nanowire model implementation via extant SPICE components is the use of Schottky diode models adapted per nanowire conditions. When these adapted Schottky models are integrated into the nanowire equivalent circuit model via SPICE, error factor improvements of 0.05 are observed,

leading to the conjecture that similar effect adaptation in the single gate MOSFET model may yield comparable improvement.

Chapter 8 - Compact Models of Nanotube MOSFET Topographies

8.1 – Carbon Nanotube MOSFET

8.1.1 – Introduction

The carbon nanotube MOSFET is a promising candidate for future technologies; with a diameter approximately three times the size of an electron wavefunction [43] and no interior lattice to impair electron movement, their ballistic carrier mobility has attracted considerable attention, though their design and fabrication are not without issue. Still, they represent an area of considerable research and growth and, with regard to compact modeling techniques, represent an extension to ideas developed in previous chapters.

As previously noted, there are no solid-state effects in the hollow interior of a carbon nanotube; the electrons display ballistic effects only in their movement from source to drain. Additionally, in modeling the carbon nanotube MOSFET device, we will again see the convention of source/drain Schottky barrier models to best replicate laboratory results. First, however, a review of the physics behind the carbon nanotube MOSFET will be outlined toward a computationally efficient compact model.

8.1.2 – Linear Charge Density Based Modeling

Fregonese et al. [49] present an excellent overview of the physical world of the carbon nanotube MOSFET and further develop this theory into a computationally efficient compact model. As this ballistic (vice drift/diffusion) MOSFET theory is probably unfamiliar to many readers, it will be treated in some detail before analysis of the compact model.

[49] first notes several aspects of carbon nanotube MOSFETs considered in their compact model:

- Current flow is reliant on ballistic transport.
- Current flow is also reliant on electron confinement in and along the nanotube.
- Current is calculated at the top of the energy barrier at the beginning of the channel; it is assumed this barrier remains constant throughout the channel.
- At the top of the barrier, source electrons fill the $+k$ states and drain electrons fill the – k states.
- Depending on nanotube chirality and radius, the periodic boundary conditions impose restrictions on available states resulting in a discrete set of energy subbands.

Additionally, a "self-consistent loop" is noted as being incorporated into their model, specifically that as V_{GS} is increased, channel potential V_{CNT} is lowered as a function of channel charge Q_{CNT}, which induces a voltage drop $V_G - V_{CNT}$ across the insulator.

8.1.2.1 – Linear Density of Charge

Beginning with a determination of the intrinsic nanotube charge, linear density of charge is first defined as the product of the Fermi-Dirac distribution and the density of states, expressed as an integral that considers both source and drain contributions:

$$n_{CNT} = \int_{E_g}^{+\infty} \frac{g(E)}{2}\left[f\left(E - E_{f(S)}\right) + f\left(E - E_{f(D)}\right)\right]dE \tag{8.1}$$

Where $f(E)$ is the Fermi-Dirac function and $g(E)$ is the density of states (equation (2), [49]). Solutions of (8.1) are derived per region with regard to parameter $sbbd[p]$, the minimum of the p^{th} energy subband, and are summarized below:

Region I (low bias): $qV < sbbd[p]$

$$n_{CNT(1)}(V, sbbd[p]) = \frac{8q(sbbd[p])}{3\pi b V_{pp\Pi}}\sqrt{\frac{\pi kT}{2sbbd[p]}} - \frac{sbbd[p] - qV}{kT} \tag{8.2}$$

Where $b = 0.142nm$ is the carbon-carbon bond distance and $V_{pp\Pi} = 3.033eV$ is the energy per carbon-carbon bond. Note that the sum of source and drain evaluations of (8.2) is equivalent to evaluating (8.1).

Region II (high bias): $qV > sbbd[p]$

Under high bias, an additional energy bound (Δ) is defined so as to provide a division between where the Fermi-Dirac function $f(E)$ is nearly constant (II.i) and where it is exponential (II.ii):

$$\Delta = qV + kT \ln\left[1 + e^{-\left(\frac{sbbd[p]-qV}{kT}\right)}\right] \tag{8.3}$$

II.i: From $sbbd[p]$ to Δ

Here, $f(E)$ varies little and may be modeled as a constant function; in particular, [49] models $f(E)$ as a two-term Taylor series expanded about $E = sbbd[p]$ introducing coefficients a_0 and a_1. As such, linear charge density in this region may be expressed as:

$$n_{CNT(2.1)}(V, sbbd[p]) \tag{8.4}$$
$$= \frac{8q}{3\pi b V_{pp\Pi}}\left[\left(\frac{a_1}{2}\Delta + a_0 - a_1 sbbd[p]\right)\sqrt{\Delta^2 - sbbd[p]^2}\right.$$
$$\left. + \frac{a_1}{2} sbbd[p]^2 \ln\left(\frac{\Delta + \sqrt{\Delta^2 - sbbd[p]^2}}{sbbd[p]}\right)\right]$$

II.ii: From Δ to $+\infty$

In this region, $f(E)$ is modeled exponentially and $g(E)$ is treated as a constant equal to $g(\Delta)$ with fitting coefficient $\alpha = 0.33$. It is noted that all chirality dependencies are considered in the values of $g(\Delta)$ and α. Under these conditions, we have linear charge density as:

$$n_{CNT(2.2)}(V, sbbd[p]) = \frac{8q}{3\pi b V_{pp\Pi}} \frac{\alpha\Delta}{\sqrt{\Delta^2 - sbbd[p]^2}} kT e^{-\left(\frac{\Delta - qV}{kT}\right)} \tag{8.5}$$

Finally, a smoothing function $f_{SMO}(V) = \frac{1}{1+e^{\left(1.3\frac{qV - sbbd[p]}{kT}\right)}}$ is provided to manage the transition from region I to region II:

$$n_{CNT} = n_{CNT(1)} f_{SM0} + \left(n_{CNT(2.1)} + n_{CNT(2.2)}\right)(1 - f_{SM0}) \tag{8.6}$$

Again, evaluation and summation of results at source and drain is sufficient to determine overall linear charge density.

8.1.2.2 – Source-Drain Current Calculation

Upon measurement of n_{CNT}, $V_{CNT(i)}$ is extracted from $V = V_{CNT(S)} - V_S$ (source) and $V = V_{CNT(D)} - V_S$ (drain). After extraction, source/drain current is calculated via these results and the Landauer formula (7.26); this ballistic transport expression considers contributions from the source to $E_{f(S)}$ and drain to $E_{f(D)}$ per subband. Thus, after integration over energy for all subbands, drain-source current is expressed as:

$$I_{S-D} = \frac{4qkT}{h} \sum_{p=1}^{+\infty} \left\{ \ln\left[1 + e^{\left(\frac{qV_{CNT(S)} - sbbd[p]}{kT}\right)}\right] - \ln\left[1 + e^{\left(\frac{qV_{CNT(D)} - sbbd[p]}{kT}\right)}\right] \right\} \tag{8.7}$$

Concurrent model induced variations in V_{CNT} and n_{CNT} have been successfully modeled via the SPICE-like simulator ADS [49].

8.1.3 – Surface Potential Based Modeling

Sinha et al. [50] build another surface potential model with an associated quantum capacitance model absent from [49]. In addition, modeling of source/drain Schottky diode contacts is included along with a source-drain current expression.

Beginning with surface potential, [50] derives a closed-form first-order approximation from the full expansion of $\phi_S = V_{GS} - \frac{|Q_{CNT}|}{C_{ins}}$:

$$\phi_S = \sum_n \left[\frac{V_T \frac{4q}{3\pi V_{pp\pi} b C_{ins}} \left(\xi_S \left| \xi_S \right| + \xi_D \left| \xi_D \right| \right)}{2\left(1 + 2\frac{4q}{3\pi V_{pp\pi} b C_{ins}} \right)} \right] - V_{GS} \tag{8.8}$$

Where $\left|\xi_{S,D}\right| = \begin{Bmatrix} 1, if\ \xi_{S,D} > 0 \\ 0, if\ \xi_{S,D} < 0 \end{Bmatrix}$ and $\xi_{S,D} = \left(\frac{E_f - V_{S,D} - E_{o,p} + V_{GS}}{V_T} \right)$. This expression forms the basis of their compact model [50 p. 2235]. An advantage of this expression is that quantum capacitance is implicit in its formulation and need not be treated separately.

Transmission coefficients with respect to Schottky barriers at either end of the carbon nanotube FET are calculated next; a triangular barrier profile is used to model transmission probability across both source and drain Schottky barriers; considering these triangular boundary conditions, the transmission coefficient is expressed as:

$$T(E) = e^{\left\{ \frac{-t_{ins} k_n}{\phi_{sb'}} \left[E' \sqrt{1 - K'^2} + \left(E - \phi_{sb'} \right) E_t \right] \right\}} \tag{8.9}$$

Where unknown variables may be found under equations (14) and (15) in [50 p. 2236]

This, in conjunction with the Fermi-Dirac function (derived from (8.8) as a component of Q_{CNT}), allows derivation of the source-drain current:

$$I_{S-D} = \frac{4q}{h} \sum_n \int_{E_n} \mathrm{sgn}(E)\, T(E) \left\{ F\left[\mathrm{sgn}(E), \left(E, E_{f(S)} \right) \right] + F\left[\mathrm{sgn}(E), \left(E, E_{f(S)} - V_{DS} \right) \right] \right\} dE \tag{8.10}$$

Where $\mathrm{sgn}(E) = \begin{Bmatrix} +1\ for\ conduction\ band \\ -1\ for\ valence\ band \end{Bmatrix}$ and the Fermi-Dirac function is given as equation (5) in [50].

8.1.4 – A SPICE-Compatible Compact Model

Deng and Wong [51] [52] present, in two parts, a well-developed SPICE compatible compact model of the carbon nanotube FET. Specifically, Deng and Wong chose to model the carbon nanotube FETs that resemble MOSFETs, dividing their model into three levels: the first being intrinsic channel charge and resulting current (akin to [49]), the second level considering the full device (channel resistance, source/drain doping, and Schottky barrier effects), and the third considering effects of multiple nanotubes within a common gate. The third case, being an instance of multiple devices, is outside the scope of this paper; the other levels will be summarized below.

Source-drain current is developed in three parts: semiconductor subband current, metallic subband current, and band-to-band tunneling current. Semiconductor current is constructed from summation over all subbands of contributions from current density and transmission probability:

$$I_{semi} = 2\sum_{\substack{k_m \\ m=1}}^{M}\sum_{\substack{k_l \\ l=1}}^{L}\left[T_{LR}J_{m,l}(0,\Delta\Phi_{\mathrm{B}})\Big|_{+k} - T_{RL}J_{m,l}\left(V_{ch,DS},\Delta\Phi_{B}\right)\Big|_{-k}\right] \tag{8.11}$$

Where T_{xy} is the transmission probability from x to y and $J_{m,l}$ is the current density contributed by subband (m,l). Further, summation limits $k_{m,l}$ are wavenumbers associated with the semiconducting subbands. [51] notes that, in practice, only the first two subbands are considered in calculations. A simplification for long-channel devices ($\gg 100nm$) is introduced by assuming a single transmission function T_m and a

continuous wavenumber k_l, replacing the associated summation with an integral, evaluated:

$$I_{semi(LC)} = \frac{4q^2}{h} \sum_{\substack{k_m \\ m=1}}^{M} T_m \left\{ V_{ch,DS} + \frac{kT}{q} \ln \left[\frac{1 + e^{\left(\frac{E_{m,0} - \Delta\Phi_B}{kT}\right)}}{1 + e^{\left(\frac{E_{m,0} - \Delta\Phi_B + qV_{ch,DS}}{kT}\right)}} \right] \right\} \tag{8.12}$$

The analogous model for metallic carbon nanotubes is inclusive of both electron and hole currents (hole currents being subdued by n-type doping in the semiconductor model) and neglects effects from channel surface potential $\Delta\Phi_B$ due to the metallic carbon nanotube's density of states function being independent from carrier energy [51 p. 3190]:

$$I_{metal} = 2(1 - m0) T_{metal} \sum_{\substack{k_l \\ l=1}}^{L} \left(J_{ele(0,l)} + J_{hole(0,l)} \right) \tag{8.13}$$

As in (8.12) above, long channel effects in metallic carbon nanotubes lead to a simplification via replacement of the summation with an integral, evaluated:

$$I_{metal} = (1 - m0) \frac{4q^2}{h} T_{metal} V_{ch,DS} \tag{8.14}$$

Finally, though in usual operation not significant, band-to-band tunneling current is significant in semiconductive nFET carbon nanotubes under negative gate bias. There are two regions of interest (Figure 8):

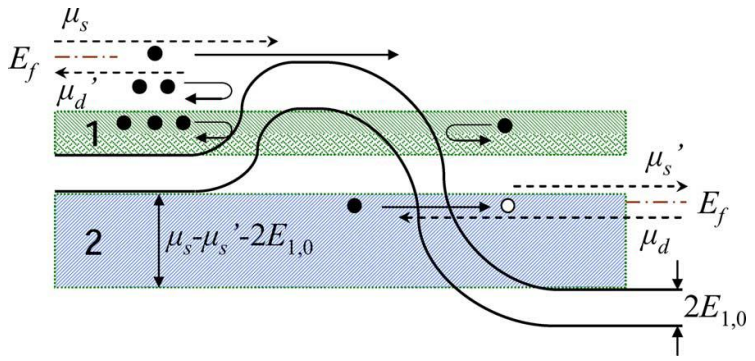

Figure 8 - Energy band diagram and associated Fermi levels at source/drain for carbon nanotube FET under moderate gate/drain bias [51].

In subband 1, holes accumulate in the nFET channel region due to the source junction preventing their exit. This lowers the surface potential leading to high current and thus poor subthreshold behavior; this effect is not observed in "well-tempered" devices [51 p. 3190]. In subband 2, there exists a possibility that a carrier may tunnel across the energy gap, modeled here as the product of tunneling probability and maximum tunneling current integrated from drain to source, a ballistic effect:

$$I_{btbt} \tag{8.15}$$

$$= \frac{4q}{h} kT \sum_{\substack{k_m \\ m=1}}^{M} \left\{ T_{btbt} \ln \left[\frac{1 + e^{\left(\frac{qV_{ch,DS} - E_{m,0} - E_f}{kT} \right)}}{1 + e^{\left(\frac{E_{m,0} - E_f}{kT} \right)}} \right] \left[\frac{\max\left(qV_{ch,DS} - 2E_{m,0}, 0 \right)}{qV_{ch,DS} - 2E_{m,0}} \right] \right\}$$

Completing their level 1 model, a comprehensive modeling of internal capacitances is presented [51 pp. 3191-3192].

Level 2 of Deng and Wong's model is comprised of second order effects, specifically channel resistance, source/drain doping, and Schottky barrier profiles. Channel

resistance is indirectly obtained as a function of channel voltage due to elastic charge scattering:

$$V_{ch,elsc} = \frac{L_g}{L_g + \frac{D_{CNT}}{1.5nm}\lambda_{eff}} V_{DS} \tag{8.16}$$

Where L_g is the channel length, D_{CNT} is the carbon nanotube diameter, and λ_{eff} is the elastic scattering mean free path, approximately $200nm$ for a $1.5nm$ diameter carbon nanotube [52].

Doping is modeled as an interaction between total charge Q and surface potential changes $\Delta\Phi$. In particular, two regions are modeled based on the bias difference between source and drain ($|V_S - V_D| = V_c$), the first region (linear) where $\left(V_c < E_f - E_{1,0} + \Delta\Phi_{s,max}\right)$ and the second (saturation) where $\left(V_c = E_f - E_{1,0} + \Delta\Phi_{s,max}\right)$. Beginning with the total carriers from semiconducting subbands per unit length:

$$Q_0 = \sum_{\substack{k_m \\ m=1}}^{M} \int_{E_{m,0}}^{E_{max}} \frac{D(E)}{2}\left[f\left(E - E_f - \Delta\Phi_s\right) + f\left(E - E_f - \Delta\Phi_s + V_c\right)\right]dE \tag{8.17}$$

Where $D(E)$ is the density of states function and $f(E)$ is the Fermi-Dirac function. Broken into regions and normalized per $Q_{Ef} = \frac{2Q_0}{D_0}$, where $D_0 = \frac{8}{3\pi b V_{pp\pi}}$, we have the following charge profile under doping (again considering only contributions from the first two subbands):

$$Q_{E_f(1)} = \begin{cases} 2\sqrt{E_f^2 - E_{1,0}^2} & : \quad E_{1,0} < E_f < E_{2,0} \\ 2\left(\sum_{k=1}^{2}\sqrt{E_f^2 - E_{k,0}^2}\right) & : \quad E_{2,0} \le E_f < E_{3,0} \end{cases} \tag{8.18}$$

$$Q_{E_f(2)} = \begin{cases} 2\sqrt{\left(E_f + \Delta\Phi_{s,max}\right)^2 - E_{1,0}^2} & : \quad E_{1,0} < E_f + \Delta\Phi_{s,max} < E_{2,0} \\ 2\left(\sum_{k=1}^{2}\sqrt{\left(E_f + \Delta\Phi_{s,max}\right)^2 - E_{k,0}^2}\right) & : \quad E_{2,0} \le E_f + \Delta\Phi_{s,max} < E_{3,0} \end{cases} \tag{8.19}$$

Equating (8.18) and (8.19), we arrive at an expression for $\Delta\Phi_{s,max}$:

$$\Delta\Phi_{s,max} = \begin{cases} \sqrt{Q_{E_f}^2 - E_{1,0}^2} - E_f & : \quad E_{1,0} < E_f + \Delta\Phi_{s,max} < E_{2,0} \\ \sqrt{\dfrac{\left[\left(E_{2,0}^2 - E_{1,0}^2\right) + Q_{E_f}^2\right]^2}{2Q_{E_f}}} - E_f & : \quad E_{2,0} \le E_f + \Delta\Phi_{s,max} < E_{3,0} \end{cases} \tag{8.20}$$

And from this expression, we obtain a normalized expression for $\Delta\Phi_s(V_c)$:

$$\Delta\Phi_s(V_c) = \Delta\Phi_{s,max}\frac{\min\left(V_c, E_f - E_{1,0} + \Delta\Phi_{s,max}\right)}{E_f - E_{1,0} + \Delta\Phi_{s,max}}V_{DS} \tag{8.21}$$

The final component of the second level of Deng and Wong's model is Schottky barrier effects. The transmission probability through this Schottky barrier is based on a triangular potential profile approximation [52] with two turning points $W_{1,2}$ (Figure 9):

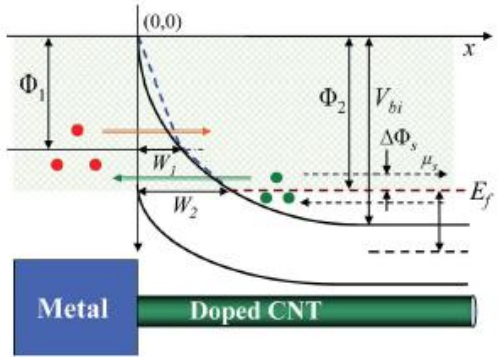

Figure 9 - Energy band diagram for Schottky barrier at the metal/doped carbon nanotube junction at equilibrium (W_1) and under bias (W_2) [52].

Turning point W_2 represents the case where bias is applied and is thus of interest to us regarding transmission probability. For this effect, only transmissions through the first subband have been considered:

$$T_{SB} = \frac{\int_{\Phi_1}^{\Phi_2} T dE}{\Phi_2 - \Phi_1} \tag{8.22}$$

An approximate solution is obtained with high degenerate doping assumed [52 p. 3200]:

$$T_{SB} = 0.5\left\{ e^{\left[-\tau\Phi_1^{\left(\frac{3}{2}\right)}\right]} + e^{\left[-\tau\Phi_2^{\left(\frac{3}{2}\right)}\right]} \right\} \tag{8.23}$$

Where $\tau = \frac{5.7W_2}{9r\Phi_2\sqrt{E_{1,0}}}$ (note that r was undefined; it may represent carbon nanotube radius or the backscattering coefficient).

8.2 – Remarks

With the hollow structure of the carbon nanotube FET channel vice previous crystalline structures, we now observe ballistic succeeding solid state effects. As such, the

Landauer formalism yields device current and dictates the derivation of probabilistic terms for our compact models. While subband expressions require the use of discrete summations, it has been seen that they may be replaced with continuous integrals, dependent upon certain conditions. New additions include loop algorithms to account for real time variations in carbon nanotube charge density and potential [49] and scalable models extensible to multichannel topographies [50].

Deng and Wong have developed a comprehensive compact model for these devices. Their intrinsic channel model incorporates several nonidealities and is applicable across nanotube chiralities and diameters. Noted anomalies that require additional attention include the modeling of degradations caused by source/drain Schottky barrier resistances and the extension beyond single walled nanotube channels. Also noted were improvements versus CMOS device characteristics for n- and p-type FET performance, speed, and power consumption.

A list of drawbacks was also composed, highlighting additional areas of carbon nanotube compact modeling research (replicated, [52 p. 3203]:

- This model uses a simplified band structure which restricts the use of this model for applications that require a high power supply and high CNT surface potential $(> 1.0eV)$. A more complete band structure model could alleviate this issue. Separating the operating region into multiple sections and deriving

approximated analytical equations in each section are additional methods to amend this shortcoming.

- Toward improved subthreshold behavior modeling, surface potential lowering and the consequent higher current caused by the carriers that accumulate in the channel should be considered, particularly in the high-bias region $\left(V_{ch,DS} > E_{1,0}\right)$.
- Diffusion capacitance was ignored due to minority carriers at the source/drain junctions, which may affect the AC response of small-signal analog circuits.
- Metallic CNTs, multiwalled CNTs, or large-diameter CNTs as interconnects could lead to improvements due to increased current density and reduced parasitic fringe capacitance.
- Most of the carrier scattering and thermal relaxation processes occur around the source/drain contact regions due to ballistic effects; thus, defects are likely to accumulate along the nanotubes, specifically around the contact region for short gate CNFETs. Model accuracy may be increased by inclusion of defect and device reliability analysis near source/drain terminals.

Chapter 9 - Conclusion

9.1 – Review

This survey has presented a comprehensive overview of contemporary compact modeling. Considering analytic models derived from fundamental expressions, computationally efficient numeric models approximating the analytic, and parameterized models specifically designed for software implementation, models for a variety of devices have been explored with symmetries and extensions noted.

The most striking symmetries have been revealed by [27] in their unified model. Parameterizing the pi gate model so that it extends to double, standard triple, quadruple, and cylindrical gate topographies provides us with the best illustration of the underlying commonalities of these multi gate MOSFETs. Further, the extension from solid state to ballistic effects begun in short channel cylindrical MOSFETs and completed in nanowire/nanotube FETs encapsulates what is perhaps the most radical change in FET design since the introduction of MOS gates.

Even among such different devices and models, some generalizations are observed. Foremost, the desire to construct mathematically continuous expressions in the most computationally efficient manner was a common goal throughout. Made most difficult

by the introduction of individual energy subband contributions in nanoscale devices, approximations leading to integral expressions were nonetheless derived by several authors. Most other shared methods acted to maintain this continuity; arithmetic and geometric fitting techniques and the use of fundamental physical and mathematical expressions, notably the Poisson equation and the general parabolic function, respectively, all served not only to model accurately and efficiently but to also preserve continuity of the end expression.

Another common modeling method was the modulation of short channel and quantum effects to refine long channel variables. As will be seen in the recommendations for further research, it is continued efforts at modulating as yet unmodulated quantities that present next steps for several models.

9.2 – Observations

While collecting data on compact models, certain compact modeling groups were contacted to better understand the methods of transitioning models from concept to industrial implementation. From these correspondences, the lack of a common roadmap, such as exists in the semiconductor industry [53], was noted. Rather, the various academic and industrial groups proceed largely of their own volition with incorporation and standardization occurring on an as needed basis.

While there are several academic and industrial colloquia and working groups dedicated to compact modeling, these do not seem to act in such a way as to align efforts toward

smooth transitions between analytic, numeric, and software implementable models. It seems that many of these discontinuities may be assisted by the formation of a common international compact modeling roadmap.

9.3 – Recommendations

Here are summarized individual model recommendations for further research, organized by device.

JFET

- Linear/saturation transition region errors persist; [2] recommends development of “a better JFET model primitive” to better model the transition region

Double Gate MOSFET/Cylindrical Gate MOSFET

- It is noted that in cross section, double gate and cylindrical gate devices are identical, implying their models may be mutually adaptable to each topography.

Cylindrical Gate MOSFET

- [36] notes that as yet there has been no solution, with regard to a general doping profile, to the Poisson equation for cylindrical topographies; the result presented here (6.2) assumes high degenerate doping.

Nanowire MOSFET

- Evaluation of the single gate MOSFET SPICE component per nanowire conditions may lead to improvements in the SPICE equivalent circuit model presented by [48].

Carbon Nanotube MOSFET

- A more complete band structure model could alleviate issues with high power supplies and high CNT surface potentials. Separating the operating region into multiple sections and deriving approximated analytical equations in each section may amend this.
- Toward improved subthreshold behavior modeling, surface potential lowering and the consequent higher current caused by carriers that accumulate in the channel need considered.
- Diffusion capacitance was ignored due to minority carriers at the source/drain junctions, which may affect the AC response of small-signal analog circuits.
- Metallic CNTs, multiwalled CNTs, or large-diameter CNTs as interconnects could lead to improvements due to increased current density and reduced parasitic fringe capacitance.
- Most carrier scattering and thermal relaxation processes occur around the source/drain contact regions due to ballistic effects; thus, defects are likely to accumulate along the nanotubes, specifically around the contact region for short

gate CNFETs. Model accuracy may be increased by inclusion of defect and device reliability analysis near source/drain terminals.

APPENDIX I – Multi Gate BSIM Models

At present, one of the most important compact models, both academically and industrially, is the Berkeley Short-channel Insulated gate FET Model (BSIM) [54]. There are presently three BSIM models, two for planar MOSFETs (BSIM3.3 and BSIM4.6.5) and one for planar SOI MOSFETs (BSIMSOI, no version control). Extension of this model to the multi gate case is ongoing. Described in various literature as BSIM-MG (BSIM Multi Gate), BSIM-CMG (BSIM Common Multi Gate), or BSIM-IMG (BSIM Independent Multi Gate), an official release has yet to occur, though several research groups are publishing their results regarding its development.

In particular, Silvaco, Inc. is advertising their involvement in this project [55]. As per their pamphlet, the Silvaco BSIMMG will support double, triple, quadruple, and cylindrical gate topographies upon completion. It appears, per references in [55], the Silvaco model is being largely driven by M. Dunga who has published other qualitative descriptions of this BSIM variant [56] [25].

Recently [57], a list of global parameters and extraction routines for BSIM-CMG was released. Specifically, this data set represents, without explicit definitions, channel length L-dependent parameters with associated functions (Table I, [57]), overall parameters grouped by length dependency (group A, Table II, [57]) and non-length

dependency (group B, Table II, [57]), and a 6-step extraction procedure, replicated below (Table III, [57]):

Table 5- BSIM-CMG extraction procedures with associated parameters [57].

Data Fitted	Parameters Extracted
1. $C-V$ data; $\Delta V_{th}(L)$ and $SS(L)$ at $V_D \sim 0.05V$ and V_{DD}; $\frac{V_{DS}(\sim 50mV)}{I_{DS}}$ vs. L at different $V_{GS}-V_{th}(L)$.	• Effective oxide thickness (EOT). • Parasitic capacitance. • SCE and DIBL parameters are initialized from $\Delta V_{th}(L)$ and $SS(L)$ at $V_D \sim 0.05V$ and V_{DD}. • ΔL and R_{series} are initialized from the intercept point.
2. I_D and G_m vs. V_G at $V_D \sim 0.05V$.	• Gate workfunction (PHIG). • Effective channel length (L_{eff}[L]). • Mobility degradation (U0[L], UA[L], UD[L], EU). • Series resistance (RDCW[L]). • Sub-threshold slope degradation. • V_{th} roll off (refinement step).
3. I_D and G_m vs. V_G at $V_D \sim V_{DD}$.	• Drain induce barrier lowering (refinement step). • Sub-threshold slope degradation at high V_{DS}. • Velocity saturation (VSAT[L], ΘSAT[L], PTWG[L]).
4. I_D and R_{out} vs. V_D.	• Gate induced drain leakage. • Source end velocity limit. • Output conductance due to DIBL and channel length modulation (CLM). • Linear/saturation smoothing function (MEXP[L]).
5. Temperature effects and self-heating.	• Parameters for temperature effects. • Thermal resistance (RTH0) and capacitances (CTH0) for the self-heating model.
6. Leakage current.	• Gate leakage current. • Impact ionization current (for bulk FinFETs only).

Appendix II – A Glossary of Common Variables

Common variables are noted below. For variables not listed, descriptions may be found either in this survey or in the source cited.

Variable	Description
c_i, C_i	Some capacitance quantity i.
E_i	Some energy quantity or level. Common subscripts are listed below.
E_F	Fermi level, sometimes accompanied by a subscript.
$E_{F(S,D)}$	Fermi level at source/drain terminals of a carbon nanotube FET.
E_g	Energy gap.
F, $\mathcal{E}$	Electric field, sometimes accompanied by a subscript.
g_m	Device transconductance, sometimes accompanied by additional subscript(s).
$\hbar$	Reduced Planck's constant.
H	Device height, sometimes accompanied by a subscript.
I_i	Device current, usually accompanied by a subscript.
J_i	Current density, usually accompanied by a subscript.
k	Boltzmann's constant.
L	Device length, sometimes accompanied by a subscript.
m_e	Effective electron mass.
n_{CNT}	Linear density of charge, carbon nanotube.
n_i	Intrinsic carrier concentration.
$N_{a,d}$	Doping concentration.
q	Electron charge.
q_i, Q_i	Some charge quantity i.
r, R	Device radius; situation dictates proper use of R.
R	Resistance parameter; situation dictates proper use of R.
R_i	Some resistance quantity i.

$sbbd[p]$	Minimum of p^{th} energy subband, carbon nanotube.
T_i	Transport probability for quantity i.
V	Voltage, usually accompanied by a subscript. Common subscripts are listed below.
V_{bi}, V_{BI}	Built-in voltage, sometimes accompanied by additional subscript(s).
V_{Di}	Device drain voltage, normalized with respect to subscript quantity.
V_{Gi}	Applied gate voltage; second subscript may either represent a normalizing quantity or a gate number.
V_p	Pinch-off voltage (FET devices only).
$V_{pp\Pi}$	Carbon-carbon bond energy $(= 3.033eV)$, carbon nanotube.
V_T, V_{TH}	Device threshold voltage.
V_{th}	Thermal voltage.
t_i	Thickness of quantity i.
T	Device temperature.
v_{sat}	Carrier saturation velocity.
W	Device width, sometimes accompanied by a subscript.
x	Generally refers to some physical location within the object of interest; sometimes accompanied by a subscript.
$\Delta\phi$, $\Delta\Phi$, Φ	Work function.
ε	Relative permittivity.
μ	Carrier lattice mobility, sometimes accompanied by subscript/superscript.
ϕ, ψ, Ψ	Surface potential, usually accompanied by a subscript.

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