STUDY OF RELIABILITY MECHANISMS AND THEIR INTERACTION IN NANOSCALE CMOSFETS

by

Rahul Mishra
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Committee:

D. E. Ioannou
Dr. Dimitris E. Ioannou,
Dissertation Director

Mulpuri, V. Rao
Dr. Rao V. Mulpuri, Committee Member

Nathalia N Peixoto.
Dr. Nathalia Peixoto, Committee Member

Yuri Mishin
Dr. Yuri Mishin, Committee Member

Dr. Andre Manitius, Department Chair

Dr. Lloyd J. Griffiths, Dean, The Volgenau
School of Information Technology and
Engineering

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George Mason University
Fairfax, VA

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By

Rahul Mishra
Master of Science Engineering
Indian Institute of Science, 2004
Bachelor of Engineering
Shri Vaishnav Institute of Technology and Science, 2001

Director: Dimitris E. Ioannou, Professor
Department of Electrical and Computer Engineering

Fall Semester 2008
George Mason University
Fairfax, VA

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LIST OF ABBREVIATIONS

ESD : ElectroStatic Discharge

NBTI: Negative Bias Temperature Instability

HCI: Hot Carrier Injection

SBlk: Silicide Blocked

TLP: Transmission Line Pulsing

DOP: Length of the silicide-blocking region on the drain side

SOP: Length of the silicide-blocking region on the source side

SG: Thin-oxide MOSFETs

EG: Intermediate-oxide MOSFETs

DG: Thick-Oxide MOSFETs

pBJT: parasitic Bipolar Junction Transistor

Vt1: Triggering voltage of pBJT

It1: Triggering current of pBJT

It2: ESD failure current normalized to width of the device

Vt2: ESD failure voltage

GS: Gate-silicided devices

GNS: Gate-non-silicided devices

ABSTRACT

STUDY OF RELIABILITY MECHANISMS AND THEIR INTERACTION IN NANO-SCALE CMOSFETS

Rahul Mishra, Ph.D.

George Mason University, 2008

Dissertation Director: Dr. Dimitris E. Ioannou

This dissertation is a study of device reliability issues and their interactions in nano-scale bulk and SOI CMOSFETs. As integrated circuits (ICs) become smaller and faster, susceptibility of devices to damage increases due to higher current densities, increased electric fields and lower voltage tolerances. With the technology scaling, not only the reliability problems are increasing but also the interaction between reliability mechanisms. This work focuses on understanding the major reliability concerns electrostatic discharge (ESD), negative bias temperature instability (NBTI) and hot carrier injection (HCI), and their interactions in both bulk and SOI MOSFETs.

In this dissertation, by investigating various aspects of ESD behavior involved in advanced 65nm CMOS technology, it is identified that the power dissipation volume, location of parasitic bipolar transistor (pBJT) formation, and the gain of pBJT plays a competitive role in determining the ESD robustness with technology scaling. From

leakages current measurements following ESD stress and device simulations, it is concluded that the thin gate-oxide MOSFETs fail due to both drain-to-source filamentation and oxide breakdown, whereas only drain-to-source filamentation occurs in thick gate-oxide MOSFETs.

The interaction between ESD and NBTI in bulk pMOSFETs is addressed next. Thick oxide devices that are subject to NBTI pre-stressing show increased ESD snapback on-resistance. Similarly, non-destructive ESD pre-stressing is shown to worsen the subsequent NBTI degradation of thin oxide devices.

The dissertation then focuses on the HCI and NBTI studies on bulk pMOSFETs as a function of channel length with various stress bias conditions at both room and high temperatures. The results reveal the increased influence of NBTI like degradation under hot carrier stress (HCS) condition at high temperature.

The dissertation then explores the ESD behavior of SOI n and p channel MOSFETs for various design (channel length and gate-oxide thickness) and layout parameters (gate-silicided and gate-non-silicided). The issues specific to SOI MOSFETs such as floating body and self-heating are studied to assess the ESD robustness of devices under investigation.

Finally, the dissertation presents a comprehensive study on the NBTI and HCI behavior of core logic/high speed (thin-oxide) and Input/Output (thick-oxide) SOI p-channel MOSFETs. The analysis of grounded body 65 nm SOI pMOSFETs show higher NBTI degradation than floating body devices due to the lowering of the oxide field in the floating body devices caused by the gate tunnel current.

1. Introduction

Advances in semiconductor manufacturing techniques and ever-increasing demand for faster and multi-functional integrated circuits (ICs) have driven the metal oxide semiconductor field effect transistor (MOSFET) sizes close to their physical limits. The number of transistor in the recently released Intel chip are approximately 2 billion [1]. The reduction in the operating voltage however has not been able to keep pace with the reduction in device dimensions. This is due to the various factors such as compatibility with previous generation circuits, noise margin, power and delay requirements, non-scaling of threshold voltage etc. The inability to reduce operating voltages has resulted in increase in electric fields in aggressively scaled MOSFETs thus presenting a major reliability problem for the long-term operation of these devices.

For every technology to be successful, it requires a thorough reliability analysis in terms of performance, protection level, and failure mechanism. The introduction of new device architectures, new gate-oxide materials and design of application specific devices require rigorous reliability analysis before they put in for the commercial production. Within the scope of these requirements, the motivation for this work is given in the following section.

1.1 Motivation

Aggressive scaling of device dimensions has enabled metal-oxide-semiconductor field effect transistors (MOSFETs) to keep the lead in very large scale integrated circuits (VLSI) [2]. As integrated circuits (ICs) become smaller and faster, susceptibility of devices to damage increases due to higher current densities, increased electric fields and lower voltage tolerances. In addition, with the scaling of technology the various mechanisms affecting transistor performance and reliability become more closely coupled. The common practice to improve transistor performance is to decrease the gate oxide thickness and channel length that helps to increase the drive current.

The downscaling of the gate-oxide poses serious concerns on electrostatic discharge (ESD) robustness of MOSFETs. ESD is a high current that affects circuits/wafers at different levels [3]. Thinner gate oxide reduces the design space for ESD protection device design [4, 5]. The standard device scaling practices that are optimized to achieve high performance have often been shown to have a negative impact on the ESD performance. The efforts to enhance the transistor performance such as lightly doped drain (LDD), shallow junction depth and silicidation of drain & source diffusion regions have adverse impact on ESD reliability of devices [3, 6]. The incorporation of LDD reduces the peak electric field at the drain which causes reduction in the avalanche multiplication factor and hence the number of generated hot carriers which are essential for efficient ESD behavior. Additionally, as a result of lower doping concentration, the resistance of LDD region is higher than the standard region. The combination of shallower MOSFET LDD and the lower doping concentration leads to a increase in the Joule heating during an ESD event [6]. The introduction of drain/source silicidation to reduce sheet resistance has shown to have worst impact on the ESD behavior. The biggest problem with silicided drain and source diffusion is the decrease in linear width dependence of the ESD devices [7].

Decreasing oxide thickness also leads to intolerable degradation in oxide reliability eg. thinner gate oxide is more susceptible to time-dependent-dielectric-breakdown (TDDB) [8] and bias temperature instabilities [9, 10]. The most important kind of bias temperature instability occurs in pMOSFETs under negative bias and high temperature, therefore, termed as negative bias temperature instability (NBTI) [10]. The application of negative voltage at the gate causes instabilities in the threshold voltage. The kinetics of this effect get accelerated by the temperature and the oxide electric field, making the NBTI presently one of the largest reliability concerns for the complementary metal-oxide-semiconductor (CMOS) technologies based on ultra-thin gate oxides.

Another important reliability mechanism is the hot carrier injection (HCI). Hot carriers cause impact ionization that leads to the injection of charge carriers in the gate oxide thus modifying the threshold voltage of the device and hence, the drain current and transconductance. As the channel length decreases and the operating voltage reduce, it was thought that the hot carrier effects would disappear when the supply voltages are reduced below the electron threshold energies for impact ionization (i.e. band-gap energy) and silicon – silicon-dioxide barrier height (3.1eV). Nevertheless, surprisingly it has been shown to be of concern for voltages well below 1.2 V. This is explained by the relatively recent discoveries that carriers can get hot by a two-step process through electron-electron scattering and by thermally assisted impact ionization at voltages well below 1.2 V [11, 12].

The above mentioned reliability mechanisms electrostatic discharge (ESD), negative bias temperature instability (NBTI), and hot carrier injection (HCI) impose new challenges in silicon-on-insulator (SOI) based MOSFETs. The SOI MOSFETs are of growing interest compared to bulk technology due to improved isolation, reduced parasitic capacitances, low sub-threshold slope, higher drive current, reduction of short channel effects, etc. [13, 14]. Central to SOI CMOS devices and technology is the inherent presence of two opposite channels (one on each side of the silicon film), the floating body, and the buried oxide. With SOI technologies reaching new levels of integration, there is also a renewed need to assess and control reliability in terms of ESD, NBTI and HCI.

As the technology scales, not only the reliability problems are increasing but also the interaction between reliability mechanisms. The various degradation mechanisms rarely of course take place in isolation and independently of each other in an operating device/circuit. Rather, they are often all active simultaneously to some degree, although the stress conditions in hand may favor a particular mechanism. This interdependence and interaction may be direct and easily identifiable, or it may act in subtler ways, for example by introducing latent damage which although not immediately observable, it may nevertheless affect the long-term operation and performance. A typical example is of MOSFETs used to protect the circuits against ESD, mostly in the so-called grounded-gate configuration, where the ESD current is discharged through the parasitic bipolar transistor (pBJT) of the MOSFET. The damage generated by hot carriers during normal operation and that generated during ESD event can influence each other. While the hot carrier reliability problem is caused by a slow injection, with the gradual build-up of interface and oxide damage, the ESD events are fast and random. The study of interaction between ESD, NBTI and HCI will also enhance the understanding of various degradation mechanisms and the device physics involved.

1.2 Dissertation organization

The purpose of this dissertation is to investigate the most serious reliability concerns and their interactions affecting the nano-scale bulk and SOI MOSFETs. Initially the work will focus on understanding the major reliability concerns: electrostatic discharge (ESD), negative bias temperature instability (NBTI) and hot carrier injection (HCI) in both bulk and SOI MOSFETs. The subsequent emphasis will be on investigating their interdependence and interaction. The reliability behavior of pMOSFETs will be studied with various stress conditions for a variety of design parameters. The proposed study will utilize devices from 65nm bulk [15] and SOI [16] technology to investigate their ESD, NBTI, and HCI reliability in terms of protection level, performance, failure mechanism and to understand their interdependence and interaction.

Chapter 2 will present a general overview of the ESD, NBTI and HCI as preliminary information for better understanding of the dissertation. The chapter will describe various ESD models, characterization method and basic MOSFET physics under high-current conditions. The basics of physics and modeling of NBTI and HCI will also be presented in this chapter. The new concerns arising with the technology scaling will be described for each reliability mechanism along with the description of the issues addressed in this dissertation. The chapter also covers the additional complexity with SOI devices when subjected to these reliability mechanisms. The chapter ends with the explanation of the importance of the study of interaction between these reliability mechanisms.

Chapter 3 will present the detailed study of ESD, NBTI, and HCI and their interactions on silicide blocked (SBlk) bulk pMOSFETs. The ESD study will concentrate on the ESD characterization of MOSFETs under investigation and will look at the effect of various design parameters on the ESD robustness of device. We will show with leakage current measurement and device simulations the competitive role of power dissipation volume, location of parasitic bipolar transistor (pBJT) formation, and the gain of pBJT in determining the ESD robustness with technology scaling. We will also look at the NBTI behavior as a function of channel length and the effect of ESD pre-stressing on subsequent NBTI behavior. The effect of NBTI pre-stressing on ESD will also be explored. The HCI and NBTI studies will be presented as a function of channel length with various stress bias condition at both room and high temperatures. The results reveal the increase influence of NBTI like degradation under hot carrier stress (HCS) condition at high temperature.

Chapter 4 will examine the ESD robustness for SOI technologies and highlight the difference between SOI and bulk technologies in terms of their ESD capability. The ESD behavior of silicide blocked (SBlk) n and p channel MOSFETs will be explored for various design (channel length and gate-oxide thickness) and layout parameters (gate-silicided and gate-non-silicided). The issues specific to SOI devices such as floating body and self-heating will be studied to assess the ESD robustness of devices under investigation. The study of ESD behavior with different stress pulse widths reveal the role of self-heating in SOI MOSFETs. This chapter will also present the comprehensive study on the NBTI and HCI behavior of core logic/high speed (thin-oxide) and Input/Output (thick-oxide) SOI p-channel MOSFETs. The effect of floating body, device temperature and gate tunneling current on NBTI and HCI performance will be explored.

Chapter 5 summarizes the contribution of the thesis and discusses the scope for the future work.

2. Review of reliability physics for nano-scale CMOSFETs

This chapter will provide the background and basic device physics needed in this research. The chapter begins with the introduction of electrostatic discharge (ESD) in devices followed by the ESD characterization models, physics of ESD in MOSFETs and new issues arising with the technology scaling. The next two sections will provide an introduction and basic physics necessary to understand negative bias temperature instability (NBTI), and hot carrier injection (HCI). The last section of this chapter will give an introduction and motivation to study the interaction between ESD, NBTI, and HCI in nano-scale devices. A brief background and the motivation to pursue the present research work will be presented in each case.

2.1 Electrostatic discharge (ESD)

Electrostatic discharge (ESD) refers to the transfer of static charge between objects at different electrostatic potentials [3]. Familiar examples of ESD include the shock that someone receives when he/she walks across a carpet and touches a metal doorknob or the static electricity that someone can feel after drying clothes in the dryer. While ESD events are often harmless in everyday life, they are the most important reliability concerns in the semiconductor technology. A substantial number of all field failures in integrated circuits (ICs) occur due to ESD. ESD damage becomes more prevalent as device dimension of ICs shrink. Great amount of progress has been made to understand the ESD failures through high current density testing and failure analysis. These efforts have resulted in producing robust ICs with fewer failures. Nevertheless, there are some ESD related problems that are not well understood yet such as latent damage.

ESD, a subset of broad spectrum of electrical stress called electrical overstress (EOS), is in the time scale of the 100ns range. The broad category of EOS family includes lightning and electromagnetic pulses (EMPs). ESD is a high current event that can affect wafers at various stages of processing and/or handling. An ESD pulse can cause damage that is determined by the device's ability to dissipate the energy received during discharge. In order to design devices with robust ESD strength, it is important to know the main design and process parameters that influence the function of device during ESD stress. Subsequently, the electrical and physical failure modes as well as the underlying failure mechanisms need to be fully analyzed. In general, device failures under ESD stress are classified as either catastrophic or latent [17-19].

Catastrophic failures under ESD stress include metal melting, junction filamentation or oxide failure. In this case, the device is permanently damaged due to the high power dissipation. In contrast to catastrophic failure, the latent damage due to ESD stress is more difficult to detect since a device can continue to perform its function regardless of partial or subtle degradation. However, a product containing such a device with latent damage may experience a premature failure or malfunction.

2.1.1 Electrostatic discharge (ESD) characterization models

There are several organizations such as electrostatic discharge association (ESDA), electronic industries alliance/joint electron device engineering council (EIA/JEDEC) that issue ESD test standards to predict the ESD immunity level. Specific tests are designed to reproduce typical discharge pulses to which the IC may be exposed during manufacturing or handling. The most common industrial models used to measure ESD robustness are the human body model (HBM), the machine model (MM) and the charged device model (CDM).

2.1.1.1 Human body model (HBM)

This model represents an ESD event from a charged human body to the pin of an integrated circuit [20]. The circuit used to model this event is shown in Figure 2-1. The pulse is generated by the discharge capacitor (C_c) of 100-pF through a 1.5kΩ resistor (R_s) into the device under test. L_s is the parasitic inductance, which determines the rise time of the discharging pulse together with the resistor R_s. C_s is the parasitic capacitance of R_s and the interconnect. C_t is the parasitic capacitance of the test board. Testing specifications usually require circuits to be able to have a minimum threshold of +/- 2kV HBM ESD stress on all pins. The typical current peak of 2kV HBM ESD event is ~1.3A with a rise time of 5~10ns and decay time of approximately 150ns as shown in Figure 2-2. HBM is the longest ESD event of the three primary models, but it has the lowest current.

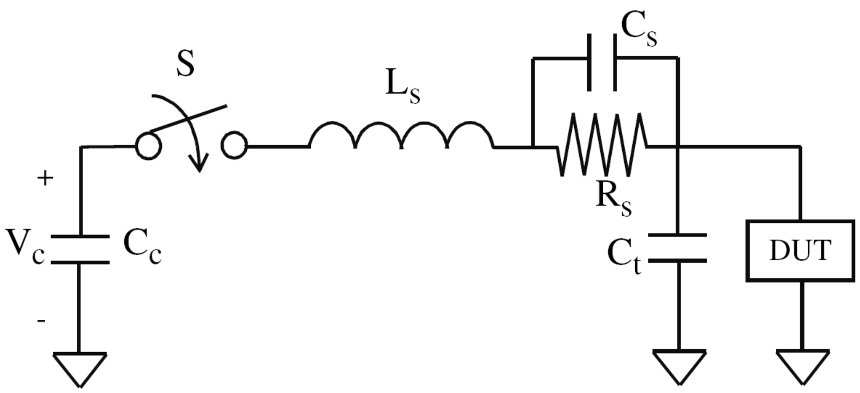

Figure 2-1: The lumped equivalent circuit model for the HBM and MM testers. Capacitor C_C is charged to the test voltage, V_C, and then discharged through R_S to the device under test (DUT) by closing switch S. Parasitic circuit elements are represented by series inductance L_S, stray capacitance C_S, and test-board capacitance C_t. The magnitude of each element is different for HBM and MM, resulting in different current waveforms. For HBM $C_C = 100\text{pF}$, $L_S = 7.5\mu\text{H}$, $R_S = 1500\Omega$, $C_S = 1\text{pF}$ and for MM $C_C = 200\text{pF}$, $L_S = 2.5\mu\text{H}$, $R_S = 5\Omega$, $C_S = 1\text{pF}$ [21].

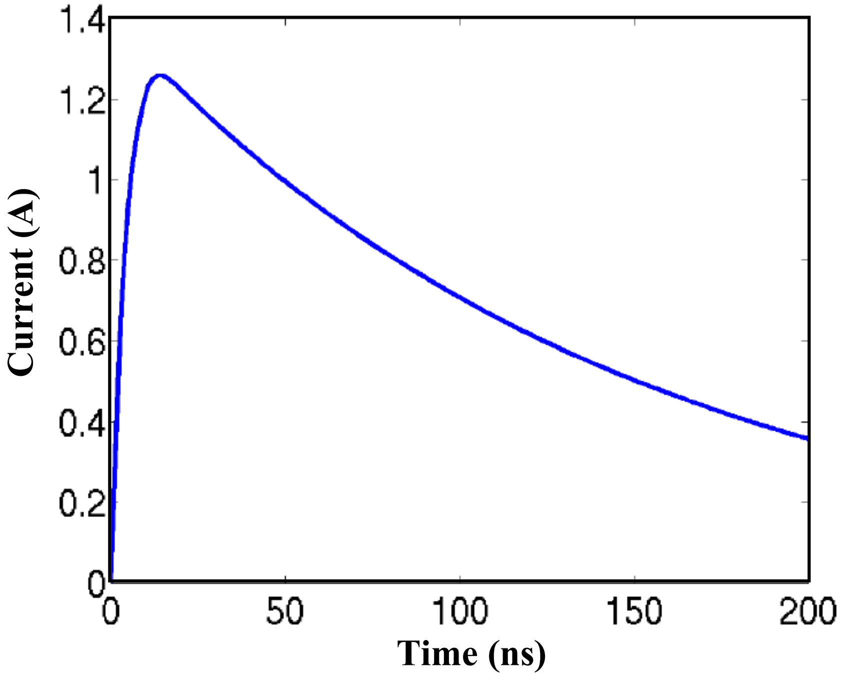

Figure 2-2: A typical human body model (HBM) current discharge waveform [22].

2.1.1.2 Machine model (MM)

In semiconductor industry, automatic machines are used to process IC products during fabrication, assembly and testing. This model simulates the discharge from a tool or machine as the machines could generate the ESD event to cause the ESD stress on IC products [20].

This event is faster than HBM and has a higher current level. The circuit for machine model is shown in the Figure 2-1. In this case, the 200pF capacitor (C_c) is tied directly to the device under test i.e. the resistance to discharge the charge is essentially zero (R_s=0Ω). The low impedance system means that the parasitic inductance and the stray capacitance will have a significant influence on the dynamic impedance, and therefore, on the amplitude and frequency of the discharge current waveform. In addition, due to the absence of the discharging resistance, the rise time of the discharging waveform is 1~3ns.

The pass threshold for the MM required for the commercial ICs is ~200V. The typical current peak of 200V MM ESD event is ~1.3A with a current ringing frequency of ~16MHz. The typical waveform shape is shown in Figure 2-3.

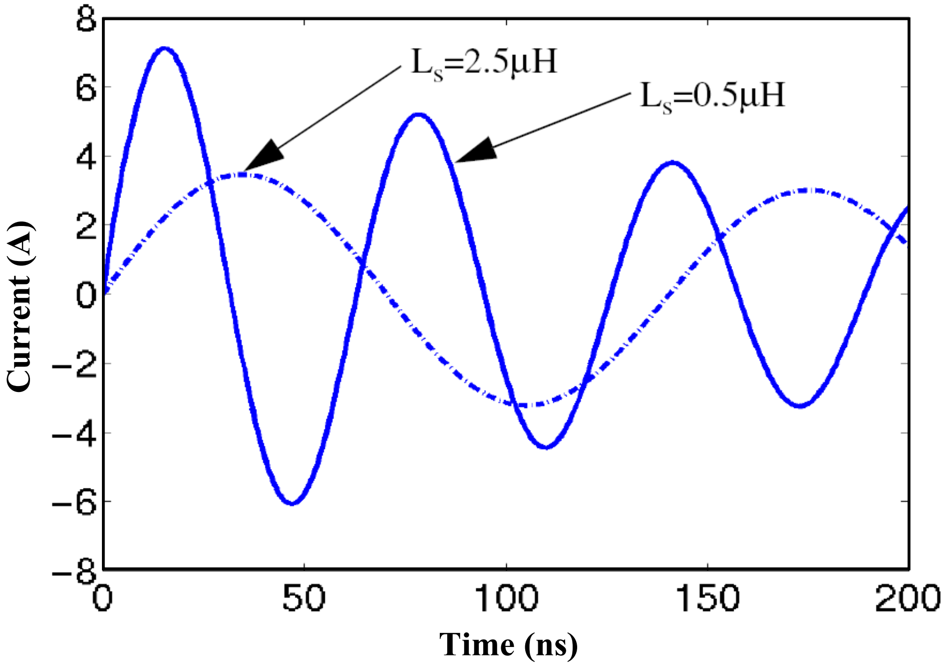

Figure 2-3: A typical machine model (MM) discharge current waveform with two different parasitic inductance L_S values [22].

2.1.1.3 Charged device model (CDM)

In this model, electrostatic charge builds up on a chip either due to improper grounding or during the fabrication/assembly/testing process [20]. The packaged ICs themselves get charged-up to high potentials, and the stored energy is discharged when one of the pins is grounded. The CDM event equivalent circuit is shown in the Figure 2-4. The charge to the IC is supplied via the switch S and resistor R_i. The discharge then takes place trough the R_s and L_s. The equivalent circuit of a CDM event cannot be standardized as the capacitance in the CDM to store the charge is dependent on the IC itself. CDM pulses have very fast durations (<1 ns) and current levels may reach several amperes for a single event. Since the turn-on time of MOS protection circuits is about 1ns, high voltages have a chance to build up across oxides during a CDM event. Thus, damage to the thin oxides is mostly the signature failure of CDM events. The turn-on speed of the ESD clamp device on the I/O pins is a key issue for CDM ESD protection as the CMOS scaling continues [5, 20, 23].

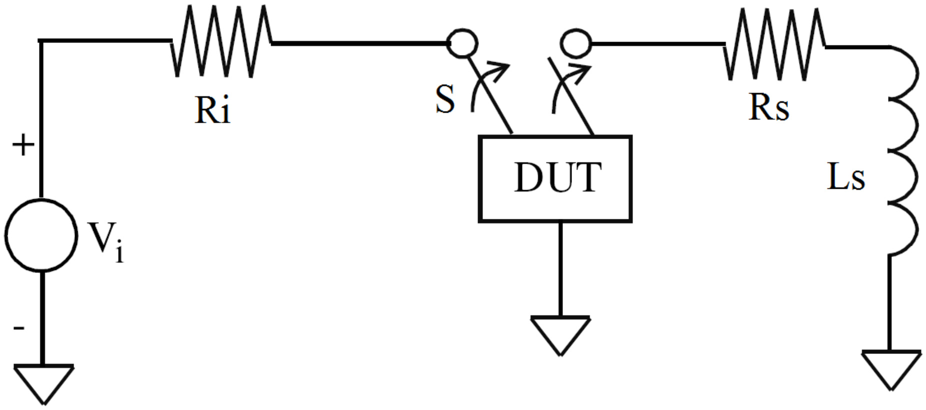

Figure 2-4: The lumped equivalent circuit model for the charge device model (CDM) tester. The device under test (DUT) is charged to voltage V_i through switch S, then the switch is thrown connecting a different pin of the device to the ground [21].

2.1.2 Transmission line pulsing (TLP) method

The classical characterization models, HBM, MM and CDM, mentioned above are not sufficient to guarantee robustness against all ESD induced failures. It is possible for a circuit to pass one type of test, while failing another. There are many limitations to using the classical models to characterize ESD robustness of circuits. Firstly, the models give a limited insight of how the protection circuit works, how and at what point they fail. Secondly, the input pulses of the HBM as well as other models are complex and brief, the response of circuit is also complex and hard to measure.

The transmission line pulsing (TLP) method is generally used to obtain current-voltage relationship for the semiconductor devices and circuits under ESD like conditions. The extraction of ESD relevant parameters in the high current regime is performed by short pulse measurements to avoid thermal overstress in the device. In this method, instead of duplicating the real life events such as HBM, MM or CDM, square-wave pulses of varying magnitude and length are applied to the device under test (DUT) and the current through and voltage across the device is measured. Different pulse widths can be used to simulate different ESD events. Generally, a 100ns pulse is used to simulate HBM, and a 30ns pulse is being evaluated for simulating MM. This technique was first introduced by Maloney [24]. There have been several modification to the testing set-up since then [25, 26].

In TLP method, after the application of each ESD stress pulse, the DC leakage current evolution of the device under test (DUT) is recorded. The dc leakage current measurement of the DUT after each stress pulse provides additional insight into minute changes in the damage of the protection device. Sometimes it is also useful to measure the full I-V characteristics such as Id-Vg in case of MOSFETs to get more insight on the effect of ESD stress pulses. The dc leakage current (or, device I-V) data combined with the TLP I-V curve provide electrical indications of where damage begins, and how rapidly it can evolve from soft to hard failure. A schematic drawing of the TLP set-up used in this work is shown in the Figure 2-5. A high current pulse generator (HP8114a) was used to send 100ns square current pulses through drain of a grounded-gate MOSFET. The digital oscilloscope (HP-Infinium) was then used to measure the instantaneous drain voltage and current, transmitting them to a PC controller, where they were used to construct the TLP I-V curve. The HP-4156B parameter analyzer was used to find the MOSFET channel off current after the application of each stress pulse.

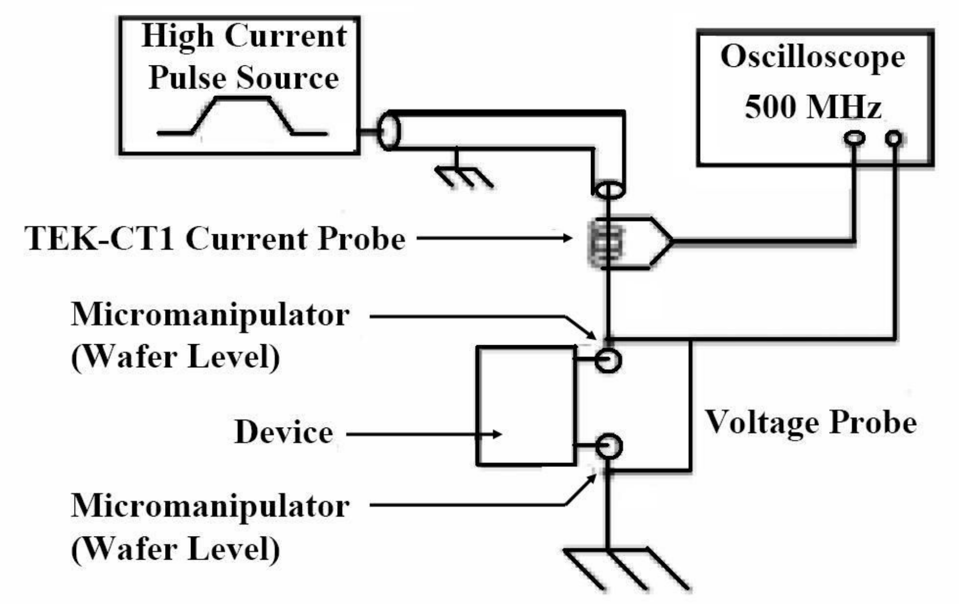

Figure 2-5: TLP schematic: Current pulses of fixed duration and increasing magnitude are applied on DUT and their effect measured until agreed fail criterion (e.g. a certain level of leakage) is reached.

2.1.3 Physics and operation of MOSFETs for ESD protection

As semiconductor devices and ICs are susceptible to ESD damage, preventive methods are required for protection against such high current events. The most sensitive areas of an IC are the devices that are directly connected to the bond pads. In order to protect the core circuits from the ESD stress, protection devices are placed in parallel with the I/O circuits as shown in Figure 2-6. These protection devices work as voltage clamps and current shunts. The purpose of the ESD protection device is to turn on during the ESD event and clamp the voltage across the internal devices to a value lower than their breakdown voltages. Ideal ESD protection device should have the following characteristics:

1. Zero clamp voltage
2. Zero on-resistance
3. Instantaneous turn-on time
4. Infinite power dissipation capability
5. No parasitics such as leakage, capacitive loading etc.
6. Only triggered during ESD event and never during normal operation

While in practice these kinds of ESD protection levels are impossible to achieve, nevertheless the above points provide a guideline towards a better design and optimization of the new devices. In a given IC, one type of protection circuit may not be suitable to all the pins because of the different voltage or current specifications. A variety of configuration needs to be explored. MOSFETs can be implemented in the protection circuits with several biasing configurations [27-30] such as the gate-grounded nMOSFETs (ggNMOS), the gate-coupled nMOSFETs [28], and the substrate-triggered nMOSFETs [27].

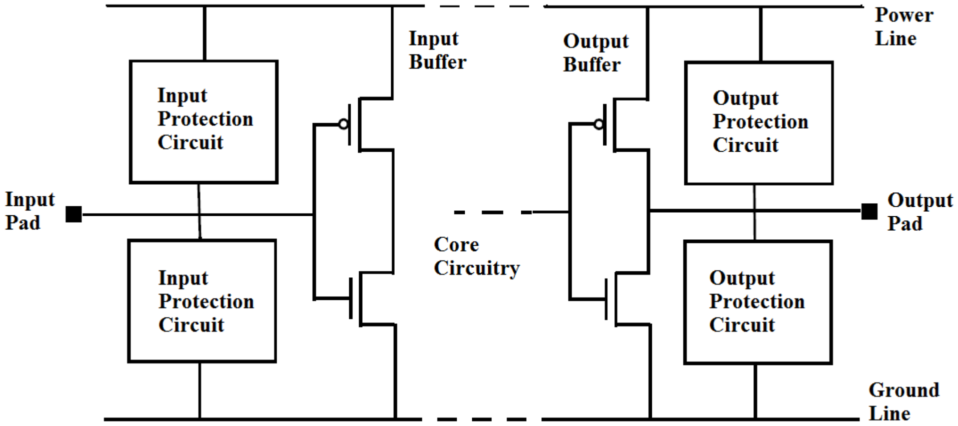

Figure 2-6: Block diagram of input and output ESD protection circuit in a CMOS technology.

2.1.3.1 MOSFET behavior under high current condition

ESD is a high-current event and semiconductor devices are not usually designed to operate under these conditions. The physics of operation of standard nMOSFET and pMOSFET transistors at such high current densities are not covered by the usual device equations. Impact ionization, parasitic device behavior, high-level carrier injection, thermal effects, and parasitic resistances and capacitances govern the high current operating region. Once impact ionization begins, the behavior of MOSFETs becomes bipolar and the models for this behavior need to be changed [4, 31, 32].

Mostly, MOSFETs in the grounded gate configuration are used to protect against the ESD event. This configuration is characterized by low voltage and low on-resistance, which imply low power dissipation during an ESD event. In this configuration, gate, source, and body are grounded and the drain is subjected to ESD stress. This kind of protection relies on the lateral parasitic bipolar transistor (pBJT) formation beneath the MOSFET channel and discharging the current from drain to source during the ESD event.

The typical operation of grounded-gate nMOSFET (ggNMOSFET) under an ESD event is explained with the help of Figure 2-7 [22]. The MOSFET utilizes parasitic bipolar turn-on as a means to switch from high impedance to low impedance during the ESD stress. An npn transistor can be formed with, the drain as the collector, the substrate as the base and the source as the emitter as shown Figure 2-7. If current pulse is applied to the drain of the nMOSFETs, the device will initially be in the high-impedance off state as indicated in Figure 2-8. Figure 2-8 shows the typical operating region of a protection element and the constraints on device engineering defined by ESD design window. As the current applied increases, the voltage rises at the drain, until the drain-substrate avalanche voltage (Vav) is reached, and the electron-hole pairs are generated by impact ionization. The electron component of the current travels into the drain terminal as, Id. The hole component, Igen, will drift towards the p-substrate contact resulting in a substrate current, Isub (Figure 2-7). As the substrate current, Isub, increases with increased drain current, it increases the local substrate potential with respect to the grounded source junction. The voltage drop across the substrate resistance, Rsub, (i.e., Vsub=Isub x Rsub) eventually reaches ~0.7 V, which is the turn-on voltage of the emitter-base (i.e. source-substrate) junction. This starts the bipolar action between source and the drain i.e. the electrons from the emitter (source) will traverse the base (channel) and cross the collector (drain) junction. If this parasitic bipolar structure has a forward gain high enough, it can provide its own base current, keeping the structure self-biased. The effectiveness of this parasitic BJT depends on two factors:

(a) emitter injection efficiency, and

(b) base transport factor which depends on the effective channel length.

Once the bipolar structure turns on, the voltage can decrease from pBJT triggering voltage (Vt1), to a minimum value (Vsp) as shown in Figure 2-8 because there is no need anymore to force the drain junction in deep breakdown to sustain the forced current. During the ESD event, the device operates mostly in snapback mode with Vsp as the clamping voltage. Once in the snapback region, Igen splits into two paths, one component is Isub and the other becomes base current, Ib, flowing in the opposite direction as shown in Figure 2-7. As the bipolar transistor turns on, the drain current is mainly sustained by bipolar action rather than on avalanche breakdown.

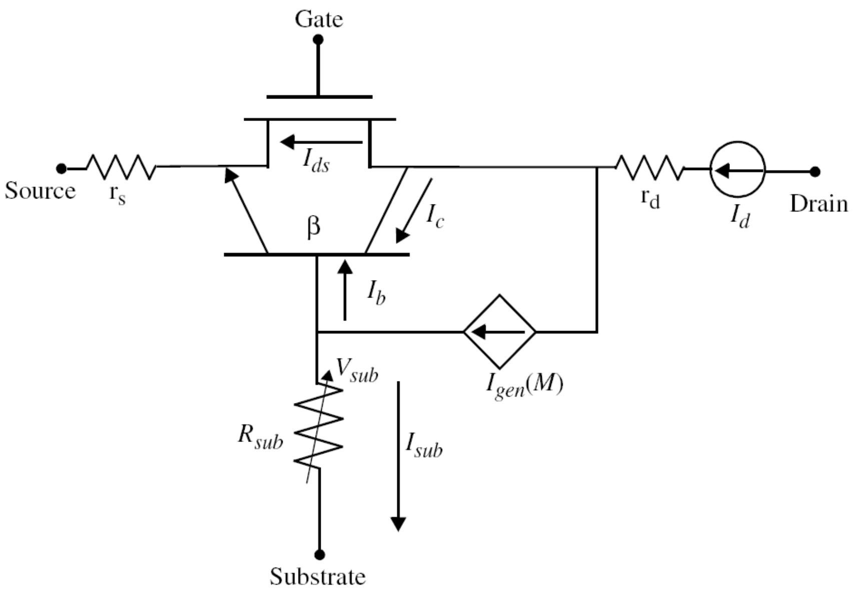

Figure 2-7: A compact model illustrating the nMOSFET operation under high current stress [22].

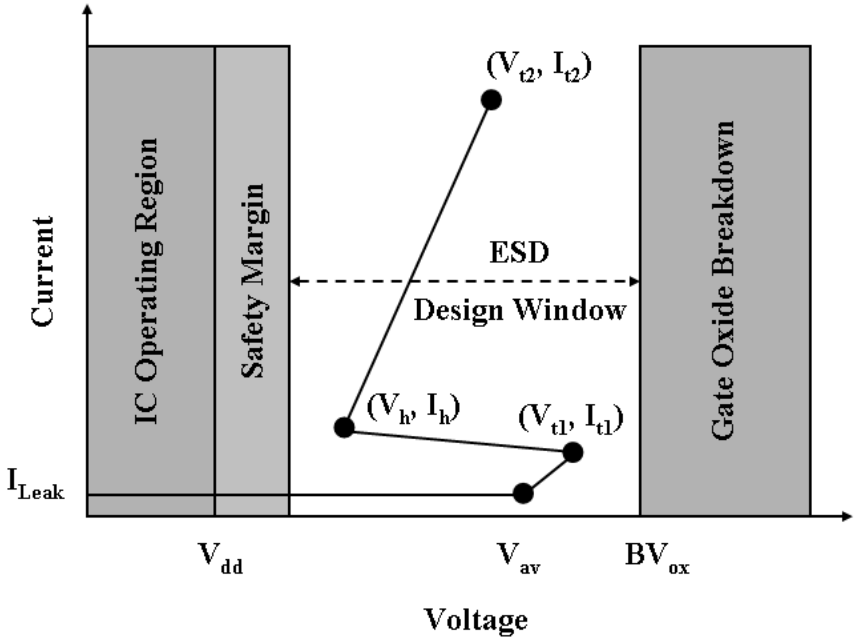

Figure 2-8: ESD design window for an ESD protection element.

2.1.3.2 Thermal breakdown

As the current injected at the drain is further increased beyond the snapback voltage the relationship between current and voltage depends on the high-current effects such as drain/source resistance, pBJT current gain (β) roll-off and substrate resistance modulation [22, 33]. The self-heating effects also come into play, increasing the internal device temperature. The hole current required to sustain bipolar action is initially avalanche-generated. As the temperature increases, the thermal generation current increases and the avalanche generated current decreases until eventually the bipolar action is being supported thermally. With further increase in the drain current, the device enters the thermal breakdown regime at It2, which is called second breakdown (an electro-thermal mechanism), distinguishing it from the avalanche breakdown (Vav) that occurs at lower injection currents. After second breakdown voltage decreases sharply and the device will show permanent damage in the form of increased leakage, or a short circuit, between the drain and substrate or oxide rupture. The failure current normalized to width (It2) is the parameter that is related to the ESD performance of the MOSFET.

2.1.4 ESD protection challenges and problem description

As mentioned in the previous section, during an ESD stress, current and voltage levels far exceed the regions of the normal transistor operation, which requires an accurate description of temperature-dependent device electrical behavior including breakdown phenomenon. High current models are required to enable circuit-level ESD reliability simulations, which are a major challenge for the industry nowadays. There has been good number of publications on the model development under ESD stress [34-37]. However, as the technology scales the model development becomes more complicated due to additional physical mechanism such as the junction (eg. drain-substrate) and oxide tunneling currents that begins to play an effective role in device operation [38].

An ESD protection circuit must provide a high current path during a high-current stress and clamp the voltage at the stressed pin below the gate-oxide breakdown level. As integrated circuits (ICs) becomes smaller and faster, susceptibility of the protection circuits to damage increases due to higher current densities and lower voltage tolerances. In addition, the thinner gate oxide in advanced nano-CMOS technology makes it more susceptible to high field stress. The effect of oxide scaling on the design of ESD protection devices is shown in Figure 2-9. The figure shows the oxide breakdown voltage (BV_{OX}) and the voltage at which drain-substrate avalanche (V_{AV}) begins as a function of oxide thickness, obtained with 200ns stress pulse [39]. The figure shows that as the oxide thickness decreases, the difference between BV_{OX} and V_{AV} also decreases. This reduction in difference between the two voltages makes the design of ESD protection elements very challenging. The designer has to ensure that the ESD protection element turns on at a voltage before the voltage at which drain node exceeds the gate breakdown voltage of the device to be protected.

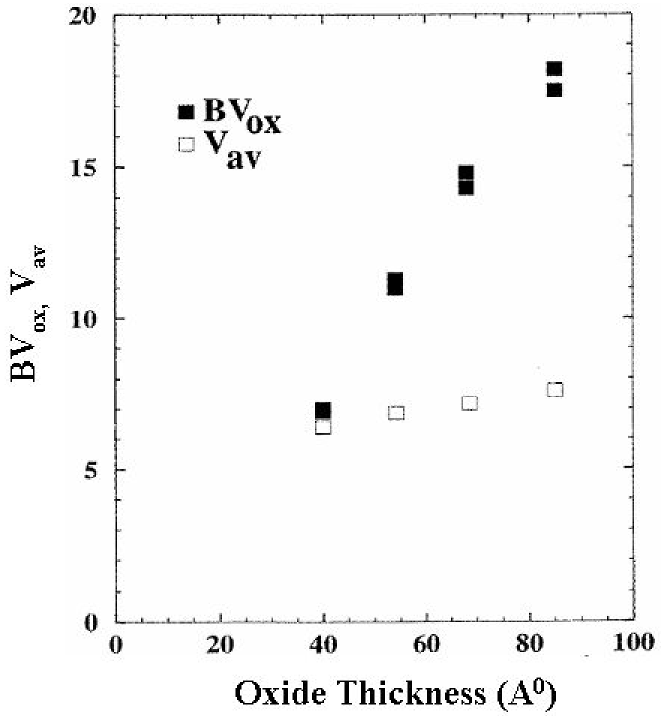

Figure 2-9: The difference between the oxide breakdown voltage (BV_{ox}) and drain-substrate avalanche voltage (V_{av}) decreases with the decrease in oxide thickness. This reduction in difference between the two voltages makes the design of the ESD protection element very challenging [39].

Moreover, silicon-on-insulator (SOI) devices face unique challenges with regard to ESD protection [30, 40, 41] due to the geometrical nature of the structure itself: the silicon film is separated from the substrate by the buried oxide layer, which has much lower thermal conductivity than silicon. The active layer, where the inversion channel forms, is thus both electrically as well thermally separated from the substrate.

The above mentioned effects such as technology scaling, structural effects in SOI devices make it necessary to understand the behavior of nano-scale MOSFETs under ESD stress. With this goal in mind, the following chapters will explore the ESD behavior of nano-scale MOSFETs for both bulk and SOI technologies.

2.2 Negative bias temperature instability (NBTI)

In recent years, negative bias temperature instability (NBTI) has become an important reliability concern both for the mainstream digital, as well as analog CMOS circuits. The name, negative bias temperature instability, refers to a buildup of interface traps and oxide trapped charge in Si/SiO_2 based devices when electric fields in the range of 2–6 MV/cm across the gate oxide are applied at temperatures of 100–200°C. Such high field and high temperature occur during burn in and in high performance ICs during routine operation. It is commonly accepted that the NBTI phenomenon generates interface states and positive fixed oxide charges at the Si/SiO_2 interface. This is due to a chemical reaction involving electric field, holes and temperature, where the Si-H bonds at the Si/SiO_2 interface are broken and the reaction is limited by the diffusion of hydrogen. The most impact of NBTI occurs on pMOSFET devices as only those experience a uniform negative bias condition during typical CMOS circuit operation as shown in Figure 2-10. When the input is low and output high, NBTI can occur in the pMOSFET.

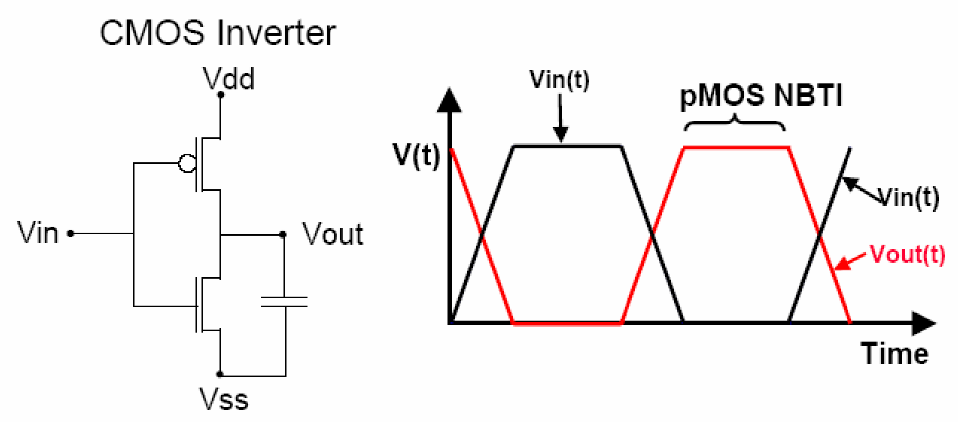

Figure 2-10: The circuit schematic of a CMOS inverter with capacitive load. NBTI can occur in pMOSFET when the input voltage is low.

NBTI has been known for quite a long time. Jeppson and Svensson [42] studied the process of trap formation at the Si/SiO_2 interface during NBT stress in MOS capacitors in 1977. They found that the NBTI-driven shift of the threshold voltage in p-MOSFETs depends on the applied gate voltage, temperature, and stress time. Later on, Blat et al [43] propose holes and water related species as primary mechanism for NBTI damage. According to their model, during the NBTI stress a hydrogen bond at the Si/gate-oxide is broken by interacting with some water related neutral species and a hole. Ogawa et al [44] have generalized the previous concepts and constructed a general mathematical scheme to understand NBTI. Their model is broken down into reaction-limited and diffusion-limited processes as will be explained in the next section.

As the technology scales (particularly as the oxide thickness decrease), several factors make NBTI the most serious reliability concern for the MOSFETs. Some of the factors contributing to the increase of NBTI effects are [9, 10, 45]:

(a) the operating voltage has not scaled as rapidly as gate oxide thickness, resulting in higher fields which enhance the NBTI.

(b) device threshold voltage scaling has not kept pace with operating voltage resulting in larger percentage degradation of drive current for the same ΔVt.

(c) the addition of nitrogen into the gate dielectric for gate leakage reduction and control of boron penetration has had the side effect of increasing NBTI.

(d) with the increase in the integration of number of transistors on a chip the power dissipation increases and the operating temperature of the device.

In pMOSFETs, NBTI typically manifests itself by a threshold voltage shift at elevated temperature. The characterization of NBTI is typically performed using standard MOS techniques, such as capacitance-voltage, charge pumping, MOSFET parameter extraction, etc. The goal of NBTI measurements is to characterize NBTI degradation as a function of time, stress conditions (stress voltage, temperature), and device architecture (gate length, gate oxide thickness etc.). The data thus obtained is used to estimate the NBTI lifetime by extrapolation of data at stress conditions to operating conditions. During NBTI stress, all the terminals (substrate, source, and drain) except gate are held at ground potential to simulate the device configuration under actual operating condition as shown in Figure 2-10. The gate voltage under stress condition is chosen be in the range 1.5-1.8 times the operating voltage to accelerate the NBTI mechanism. The threshold voltage shift is typically determined from the Id-Vg measurements taken by interrupting the NBTI stress at regular intervals. The criterion for device failure is generally circuit-dependent, but is often benchmarked at 50mV shift in threshold voltage or change in drain current ΔId/Id=10%.

This remarkably simple technique to characterize NBTI covers the fact that NBTI damage gets recovered once the stress voltage is removed [46] i.e. the interface states generated during the stress period are partially annealed when the stress is removed. In order to reduce the recovery it is important to decrease the time between stress termination and Id-Vg measurements. Recently, an on-the-fly measurement technique [47, 48] has been proposed to minimize the delay between stress and measurement time.

2.2.1 Physics and modeling of NBTI

Under NBTI stress, the threshold voltage shift (ΔVth) is observed to depend on the stress time t as $\Delta Vth \propto t^b$. Different values of b have been reported in the literature ranging from 0.2-0.35, but the commonly observed exponent b is around 0.25 [49]. This time dependence of NBTI is treated as a reaction–diffusion (R–D) process. It is widely accepted that interface traps are being generated by breaking of hydrogen passivated silicon bonds at the Si/SiO_2 interface and the subsequent diffusion of hydrogen. In this process the positive oxide charges are also generated in the oxide. The electrochemical equation describing this effect can be written as follows [50]:

$$Si_3{\equiv}Si\text{-}X + [\text{hole}]^+ \leftrightarrow Si_3{\equiv}Si\cdot + Y \ \textit{(for Nit generation)} \tag{2-1}$$

$$O_3{\equiv}Si\text{-}X + [\text{hole}]^+ \leftrightarrow O_3{\equiv}Si^+ + Y \ \textit{(for Nf generation)} \tag{2-2}$$

$$Y_{\text{interface}} \leftrightarrow Y_{\text{bulk}} \ \textit{(for Y diffusion)} \tag{2-3}$$

Where, Nit is the interface state at the Si/SiO_2 interface, Nf is the fixed oxide charge in SiO_2, X can be hydrogen or hydrogen related species and Y is a by-product neutral species. The reaction occurs when the by-product species (Y) diffuse away from the interface into the bulk of SiO_2. The rate at which the reaction causing the generation of interface traps takes place is controlled by the diffusion of hydrogen (Y) that has been released from hydrogen-passivated defect sites such as $Si_3{\equiv}Si\text{-}X$. The species released from the Si/SiO_2 interface to the bulk of SiO_2 can traverse back to the interface once the stress on the gate is removed. This re-passivation of bonds during the stress removal period is termed as recovery. There has been a lot of debate in the literature regarding the nature of Y (the released specie from the interface) [10, 44, 51]. Ogawa et al [44] have summarized possible diffusing species including interstitial atomic hydrogen, molecular hydrogen and hydroxyl group.

The following two coupled equations [52] describe the generation of interface traps mathematically through reaction and diffusion terms:

$$\frac{dN_{it}}{dt} = k_f \left[N_0 - N_{it}(t) \right] - k_r N_{it}(t) N_H(x = 0, t) \tag{2-4}$$

$$\frac{dN_H(x,t)}{dt} = D \frac{d^2 N_H(x,t)}{dx^2} \tag{2-5}$$

where x=0 is at the Si/SiO$_2$ interface and x>0 points toward SiO$_2$/poly interface. N$_{it}$ is the number of interface traps at any instant, N$_0$ is the initial number of unbroken Si-H bonds, N$_H$ is the hydrogen concentration, k$_F$ is the oxide field dependent forward dissociation rate constant, k$_R$ is the annealing rate constant, D, is the hydrogen diffusion constant.

The first term on the right hand side of Equation (2-4) comes from the dissociation of Si$_3$≡Si-H into Si$_3$≡Si·. The second term comes from the competing passivation of Si$_3$≡Si· by the released hydrogen related species. The Equation (2-5) governs the diffusion of hydrogen species away from the interface. The diffusion coefficient, D, is the average diffusivity of the assumed atomic/molecular hydrogen diffusing species. It has, however, been argued by Zafar [53] that one should consider the particle kinetics in a disordered system (such as SiO$_2$) as disperse and not Gaussian. Dispersive transport arises when the mobile species experiences a broad distribution of barrier heights, leading in turn to an exponentially broad distribution of hopping times. Kaczer et al [54] have also argued for particle kinetics to be dispersive and not Gaussian.

They have proposed a disordered-controlled kinetics model for NBTI assuming dispersive particle kinetics in the gate oxide.

There have been lots of refinements of R-D model reported in the literature. S. Ogawa & N. Shiono [44] generalized the R-D model equations and solved for finite oxide thicknesses with neutral and charged diffusing species. Alam [52] explained frequency independent recovery and performed numerical simulations for newer CMOS technologies. Chakravarthi et al [55] have developed a model that comprehends most of the unique characteristics of NBTI degradation and have calibrated the model over a range of stress voltages and temperatures. Aono et al [56] showed analytical formulation for saturation and Grasser et al [57] proposed a coupled modeling solution of the R-D model with the semiconductor current transport equations. Jha et al [58] extended the R-D model by including the effects of trapping of hydrogen species in the oxide. The R-D model does not predict the saturation in degradation characteristics after a prolonged stress time. In [53] Zafar has applied statistical mechanics to calculate the decrease interfacial Si-H density as a function of stressing conditions. Zafar also derived the equations for NBTI as a function of stress time, oxide field, oxide thickness and temperature using the principles of statistical mechanics and dispersive hydrogen diffusion.

2.2.2 NBTI challenges and problem description

Even though NBTI is an old mechanism, it is more important today because: electric fields in the gate oxide are higher, devices are operating at higher temperatures due to higher power dissipation, and voltage headroom is much smaller than in the past. Additionally, the introduction of nitrogen in the gate oxide to control the gate leakage and boron penetration has been found to lead to increased NBTI for same stress conditions [10, 59, 60]. The reliability and lifetime assessment of various circuits is seriously overestimated if done by measuring the hot carrier degradation of the nMOSFETs and neglect the simultaneous NBTI degradation of the pMOSFETs.

The mechanism by which NBTI generates interface states and trapped oxides is not completely and unambiguously clear yet, but is widely thought that dissociation of Si-H bonds plays a major role. A large number of literatures are available on the chemical behavior of NBTI [51, 61-63]. From the device reliability perspective, the issues that are not yet fully understood will be investigated in this work. Two most important concerns about NBTI are the effect of continuing dielectric (gate-oxide) scaling and the role (if any) of the resulting increase in gate current [64]. Although the primary degradation driving force is believed to be the electric field, the role of the tunneling gate current flowing during NBT stress will be investigated in this work, especially in SOI structures where this type of current can also interact with the floating body and be amplified by the parasitic bipolar transistor. NBTI reliability has not been studied yet as extensively in SOI technologies, but due to the SOI structure itself (self heating, floating body, channel coupling, BOX quality etc) it is expected to be of even greater importance than bulk, and harder to study.

2.3 Hot carrier injection (HCI)

The continuous downscaling of MOSFET dimensions without a corresponding reduction in the supply voltage has led to ever-increasing electric fields inside the transistor. The evolution of electric fields in the silicon and oxide is shown in Figure 2-11. The origins of hot carrier effects are related to the increased electric field occurring near the drain when a MOSFET operates in the saturation region. The presence of high electric field in a semiconductor leads to a condition of non-equilibrium. The charge carriers are accelerated under the influence of the electric field and at the same time suffer several kinds of collisions with other carriers or lattice atoms. When the average energy gained by the carriers exceeds the average energy lost by the carrier through scattering effects, the average carrier temperature will be larger than the lattice temperature. Such a carrier is termed as hot carrier. Electrons with an energy exceeding a threshold of about 1.6 eV (1.5 times the Si bandgap) can create an electron–hole pair in the silicon by a process called impact ionization. Impact ionization is characterized by an impact ionization rate, α, defined as the number of electron-hole pairs generated by a hot carrier in unit length. Carriers with sufficiently high energies (about 3eV for electrons and 4eV for holes) can get injected from the semiconductor into the surrounding dielectric films such as the gate and sidewall oxides.

There could be different injection mechanisms depending upon the pattern of electric field under different bias conditions [65]. The different injection mechanisms are:

(a) Channel hot-electron injection [66]

(b) Drain avalanche hot electron injection [67]

(c) Secondary generated hot electron injection [68]

(d) Substrate hot-electron injection [69]

(e) Fowler-Nordheim tunneling injection [70] and

(f) Direct tunneling injection [70].

Depending upon the mechanism determined by the bias mechanism the injected carriers can :

(a) get trapped in the oxide,

(b) create new traps (donor or acceptor like traps),

(c) create interface traps and

(d) pass through the oxide.

The injection of hot carriers into the oxide leads to a gradual degradation of the transistor characteristics. In general, the damage created under hot carrier stress is proved to be locally induced (near the drain) interface states and/or trapped charges. This degradation can be measured as a shift in threshold voltage, transconductance, drive current, subthreshold slope.

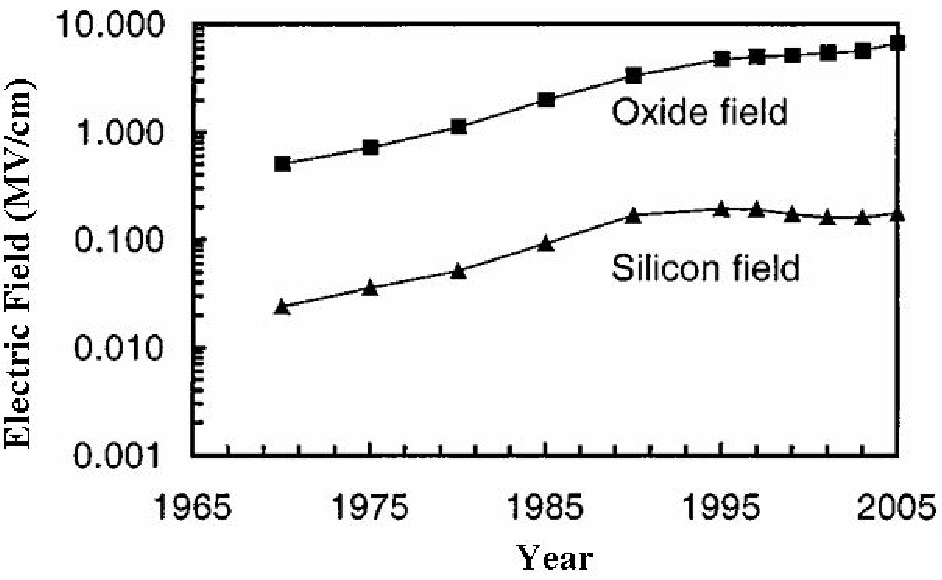

Figure 2-11: Evolution of electrical fields in oxide and silicon [71].

2.3.1 Physics and modeling of HCI

Under hot carrier injection (HCI) stress, the MOSFET is said to be degraded when a certain parameter changes by a pre-determined threshold value. The time required for this to occur is called hot-carrier induced failure time (τ). The lifetime prediction of MOSFETs from accelerated hot carrier stress (HCS) data is generally obtained by lucky electron model (LEM) [72]. The electrons which get injected into the oxide are termed as lucky electrons. The LEM approach of modeling the hot electron behavior was originated by Schokley [73]. This model has been applied to MOSFETs by Hu et al to model the channel hot electron injection in nMOSFETs [72]. In LEM, a general model for the hot-electron effects is formed by correlating the impact ionization substrate current, hot-electron injection into the oxide, and interface damage to the peak lateral electric field. The model is formulated though the following set of equations:

$$I_{sub} = C_1 I_d e^{-\phi_i / q\lambda E_m} \tag{2-6}$$

$$I_g = C_2 I_d e^{-\phi_b / q\lambda E_m} \tag{2-7}$$

$$\Delta N_{it} = C_3 \left[t \frac{Id}{W} e^{-\phi_{it} / q\lambda E_m} \right]^n \tag{2-8}$$

$$\tau = C_4 \frac{W}{I_d} e^{\phi_{it} / q\lambda E_m} \tag{2-9}$$

where, λ is the hot-electron mean path, E_m is the peak electric field, φ_i, φ_b, and φ_{it} represent critical energy thresholds that a hot electron must have in order to initiate impact ionization, surmount the effective barrier at Si-SiO_2 interface and create an interface state respectively. τ and n describe how interface states (ΔN_{it}) evolves with time. Equation (2-9) is derived by rewriting Equation 2-8 for the time τ at which ΔN_{it} reaches a chosen value.

From the first two equations it can be formulated that:

$$\frac{I_g}{I_d} = C \left[\frac{I_{sub}}{I_d} \right]^{\phi_b / \phi_i} \tag{2-10}$$

This relation has been verified experimentally. A log-log plot for different gate to drain bias Vgd results in lines with a slope of $\varphi_b(E_{ox})/\varphi_i$ where E_{ox} is the oxide field at the drain side.

Now by defining the lifetime as the time to reach a fixed amount of damage, and by combining Equation (2-6) and (2-9), the lifetime can be written as,

$$\frac{\tau I_d}{W} = C\left[\frac{I_{sub}}{I_d}\right]^{-\phi_{it}/\phi_i} \tag{2-11}$$

Thus, this equation shows that device lifetime is a decreasing function of the substrate current. The slope m=φ_{it}/φ_i has been experimentally verified is found to be on the order of order 3, independent of device and bias parameters. The slope m indicates the energy of the electrons that causes the damage.

As channel lengths approach the deep sub-micrometer regime and as the power supply voltage approaches the Si-SiO_2 barrier height, the validity of LEM has been debated over the research community. A simple lucky-electron model, in which carriers gain all their kinetic energy from the applied external potential, is not adequate to explain this low-voltage behavior. The classic LEM essentially treats the electron energy distribution function (EEDF) as Maxwellian with an effective temperature given by qλEm/K. However, the presence of electron-electron scattering (EES), which play an increasingly important role as the supply voltage is scaled down, significantly distorts the high-energy tail of the EEDF [11, 74]. Rauch et al [75] showed that the hot carrier degradation of short channel nMOSFETs do not obey LEM and they proposed a correction to it accounting for the e-e scattering effect.

Goldsman et al [76] define the limit of validity of LEM by comparing it with the physics based Monte Carlo calculations. The exponential form of LEM suggest that EEDF is Maxwellian, while Monte Carlo suggests that the EEDF is non-Maxwellian. They have shown that with the appropriate choice of mean-free path (λ), the exponential form of LEM can be made to agree with the results from Monte Carlo calculations.

2.3.2 HCI challenges and problem description

The hot carrier degradation mechanisms have been studied extensively for bulk and SOI MOSFETs and a good amount of information has been accumulated over the years. Significant progress has been made in establishing suitable device degradation monitors, understanding the physical mechanisms involved and device/process design to suppress these mechanisms. However, the continued scaling of MOSFETs has rendered hot carriers to the subject of continuous and intense investigations.

Hot carrier effects (HCE) and the corresponding device degradation are directly related to the processes of impact ionization and carrier injection into the gate dielectric. Hot carrier degradation of p-channel devices is much more complicated than n-channel. With the scaling of gate oxide thickness, pMOSFET hot carrier (HC) reliability departs from the electron trapping mechanism [77] to the hot-hole induced degradation [78, 79]. For the sub-0.25μm pMOSFETs, it has been concluded [78, 79] that the generation of interface states by hot-holes causes the most serious degradation. As these processes must meet minimum threshold energies, for low power supply voltages hot carrier reliability was thought not to be a problem. But surprisingly it has been shown to be concern for voltages well below 1.2V. This is explained by the relatively recent discoveries that carriers can get hot by a two-step process through electron-electron scattering [11], thermally assisted impact ionization [12], impact ionization feedback [80] and valence band tunneling [81], and inversion layer quantization as energy gain mechanism [74]. The situation is more complicated [82, 83] for SOI devices as both the worst case stress conditions and the interpretation of degradation are influenced by the intricate interdependences of stress bias level, floating or grounded body operation, channel-coupling strength, and device operation temperature. Device operation temperature is particularly important for the SOI devices due to the self-heating effect (SHE). In particular, as shown by Ioannou et al [84], SHE plays a major role in pMOSFET HC degradation because as the oxide field increases with the scaling of oxide thickness, NBTI activation takes place simultaneously. In addition, it has been shown [12] that the main driving force of impact ionization changes from the electric field to the lattice temperature with power-supply scaling below 1.2V. Self- heating is also found to be responsible for the excess substrate current observed.

Among the issues that will be investigated in this work are the effect of temperature, stress bias, floating or grounded body operation and channel length on the HCI behavior.

2.4 Interaction between ESD, NBTI and HCI

The electrostatic discharge (ESD) protection strategies for input/output (I/O) devices can be divided into two parts based on the implementation scheme: (a) non-self protecting strategy and (b) self-protecting strategy. In the non-self protecting strategy, additional ESD devices are added in parallel to the I/O circuits to shunt the current away from the I/O circuits to the power supply rails during an ESD event. In the self-protecting strategy, devices in the I/O itself are designed to handle the current supplied during an ESD event.

In self-protecting ESD strategies, silicide blocked (SBlk) MOSFETs are used both as the output driver as well as an ESD protection device, utilizing the drain/source ballast resistance to improve the parasitic bipolar junction transistor (pBJT) behavior. During an ESD event, non-destructive pulses can potentially induce latent damage into the output driver, whereas during the normal operation of the circuit it is subjected to various kinds of electrical stresses. Previous studies have concentrated on latent damage in nMOS devices due to ESD pre-stressing [17, 71, 85-88]. Aur et al [85] have shown that latent damage due to ESD pre-stressing could decrease the hot carrier injection (HCI) lifetime by as much as a factor of 4. It has been reported by Doyle et al [86] that nMOSFETs show change in the resistance in the I-V characteristics due to the injection of primary charge carriers in the oxide during high current stress. More recently, Salman et al [17] studied the effect of non-destructive ESD stress on deep submicron devices and concluded that ESD pulses cause a certain amount of hot electron (HE)-like degradation.

The present work will focus on the interaction between ESD, NBTI, and HCI in SBlk pMOSFETs, which are becoming very important in self-protection ESD circuit strategies as the reduction in channel length causes an increase in the gain of the PNP pBJT [89]. Recently, Li et al [90] have shown the use of pMOSFET based ESD protection devices in 65nm bulk CMOS technology for improved external latch-up robustness. Figure 2-12 shows the schematic of a whole chip ESD protection strategy based on Gate-tied-to-VDD pMOSFET (GVPMOS) and RC-triggered power clamp. In [91] the pMOSFET behavior under ESD conditions for three technological nodes is compared. It is argued that the improved PNP pBJT performance will result in a higher inadvertent triggering. Hence, there is a need to investigate the ESD behavior of pMOSFETs also.

Thus, due to the dual functionality of the pull-up pMOSFET, it can be subjected to either HCI or NBTI or both during its normal operation, whereas it is subjected to high current stress during an ESD event. In addition, due to the aggressive scaling of oxide thickness compared to the operating voltage, the field across the oxide increases, thus making the pMOSFETs vulnerable to NBTI as well as HCI. To predict the lifetime accurately it is necessary to study the interaction and interdependence between these degradation mechanisms. The study of interaction between different reliability mechanisms will also enhance the understanding of various degradation mechanisms and the device physics involved.

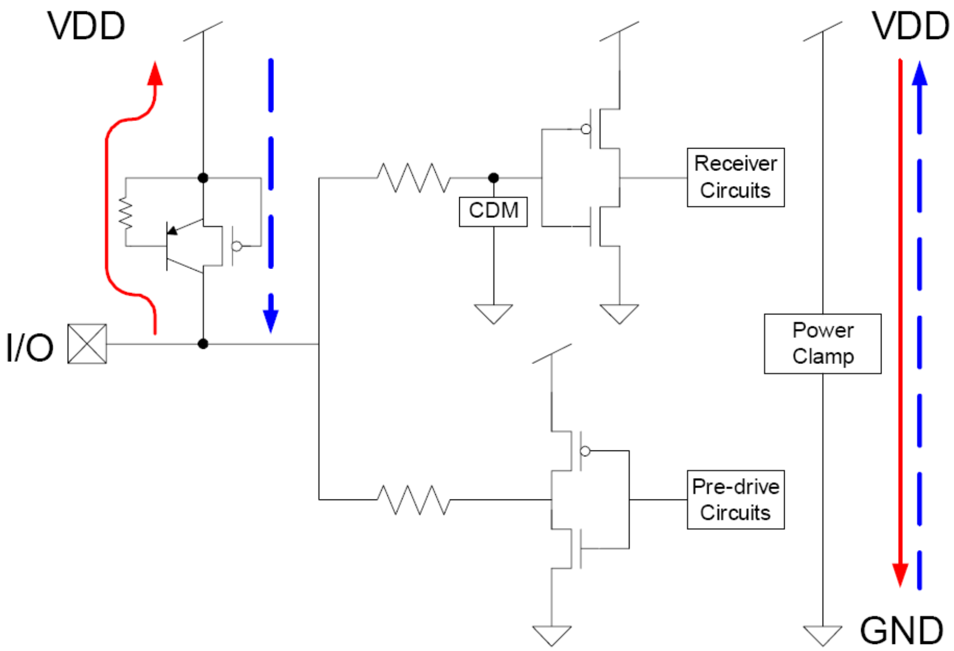

Figure 2-12: Whole chip ESD protection using Gate-tied-to-VDD pMOSFET (GVPMOS) and power clamp. Solid and dotted lines with arrows indicate the designed ESD current discharging paths of positive and negative ESD stresses from I/O pad to GND, respectively [90].

3. ESD, NBTI and HCI investigation of nano-scale bulk MOSFETs

The purpose of ESD protection circuit in a chip is to find an alternative path to the ground for high current signal away from the core operating devices. In general, there are two main purposes an ESD protection circuit must serve:

(a) It must provide a current path during a high-stress event, and

(b) It should clamp the voltage at the stressed pin below the gate-oxide breakdown level of the device to be protected.

Additionally, it is important that the protection circuit itself should not get damaged during an ESD event. Proper care should be taken to minimize the self-heating by lowering the current density and electric field through proper device design.

The ESD protection strategies used in input/output (I/O) circuits are divided into two categories: (a) non-self protecting strategy, and (b) self-protecting strategy. In the non-self protecting strategy, additional ESD devices are added in parallel to the I/O circuits to shunt the current away from the I/O circuits to the power supply rails during an ESD event. In the self-protecting strategy, devices in the I/O itself are designed to handle the current supplied during an ESD event. The self-protecting strategy is very attractive solution to implement the ESD protection due to the following reasons:

(1) The area saving of the protection circuit as the device in the I/O itself is used as a protection device, and

(2) Reduction of the capacitive loading on the output driver can help to achieve high-speed output circuits with the same level of ESD protection.

The disadvantage of the self-protecting strategy is that the protection circuit is a part of the operating device. So if any damage occurs due to ESD stress the circuit functionality will be affected as well. More importantly, this strategy entails the interaction between different reliability mechanisms [92]. During the normal operation, the protection device will be subjected to either NBTI or HCI and during ESD event it will be subjected to high current stress. This simultaneous and/or sequential occurrence of all the three mechanisms requires a good understanding of each individual phenomenon, their interaction, and interdependence as well. With this problem in perspective, this chapter will present a comprehensive study on the interaction between ESD, NBTI and HCI on silicide blocked (SBlk) pMOSFETs for a state-of-the-art 65nm bulk technology [15].

Historically, for ESD protection pMOSFETs have received less attention than the nMOSFETs. This is because of the poor performance of the lateral PNP parasitic bipolar transistor (pBJT). Now, as the technology scales the pMOSFETs are also becoming an attractive choice for implementing ESD protection because the reduction in channel length causes an increase in the gain of the pBJT [89]. Starting with 180nm technology, every new node featured a reduction of the pBJT trigger voltage, holding voltage and an increase of failure current [93]. As mentioned above, in a self-protection strategy, due to the dual functionality of the pull up pMOSFET, it can be subjected to either HCI or NBTI or both during its normal operation, whereas it is subjected to high current stress during an ESD event. To predict the lifetime accurately it is necessary to study the interaction and interdependence between these degradation mechanisms. In addition, due to the aggressive scaling of oxide thickness compared to the operating voltage, the field across the oxide increases, thus making the pMOSFETs vulnerable to NBTI as well as HCI.

The study of these three reliability mechanisms divides this work into three sections. The first section will present the ESD characterization of bulk CMOS 65nm technology for three groups of pMOSFET devices, with different oxide thicknesses and channel length as a parameter [15]. It will be shown that the thin and thick oxide devices exhibit different failure current (It2) behavior with respect to channel length. In particular, it is found that not only the high gain of the pBJT is an important factor in a short channel device in determining the ESD behavior, but also the power dissipation volume needs to be considered. The second section describes the interaction between ESD and NBTI. Since NBTI may occur before an (destructive or otherwise) ESD event or vice-versa during the lifetime of the device, it is important to study the ESD and NBTI interaction and ascertain whether there are any detrimental effects of one mechanism on the other. It is observed that thick oxide devices that are subjected to NBTI pre-stressing show increased ESD snapback on-resistance. Similarly, non-destructive ESD pre-stressing is shown to worsen the subsequent NBTI degradation of thin oxide devices. The third section reports the results of NBTI and hot carrier stress (HCS) of thin oxide devices at high temperature. A channel length dependent co-activation of NBTI during the HCS is observed.

3.1 Device details

The following three different device groups from the 65nm bulk CMOS technology [15] will be explored for their ESD, NBTI and HCI behavior:

(a) Thin oxide (SG) devices (Vdd=1.0V, Tox=1.25nm),

(b) Intermediate oxide (EG) devices (Vdd=1.5V, Tox=2.2nm), and

(c) Thick oxide (DG) devices (Vdd=2.5V, Tox=5.4nm).

The top-view of a generic MOSFET designed for ESD protection is shown in the Figure 3-1. The design has silicide blocked regions on the drain and the source to provide ballistic resistance to improve the ESD current uniformity across the width of the device [94]. Hence, these devices are called silicide blocked (SBlk) devices. The DOP and SOP in the Figure 3-1 are the lengths of the silicide blocked regions on the drain and source side respectively. This type of layout in which two small silicided regions, op-pc, exist between drain/source silicide blocking and the gate is called gate-silicided (GS) design. This layout design is different from the gate-non-silicided (GNS) design where the silicide-blocking layer is placed across the drain, gate and source thus, leaving both the gate and the op-pc area silicide blocked. The ESD behavior of GNS design is explored for SOI devices and will be explained in Chapter 4. The op-pc spacing in the GS designs is constant (=240nm) irrespective of the variations in DOP/SOP lengths. In SG devices the drain side silicide blocking length DOP=2μm and the source side SOP=0.4μm, whereas both EG and DG devices have DOP=4µm and SOP=0.4µm. All the devices are multi-fingered with 240µm of total width where each finger had a width of 20µm.

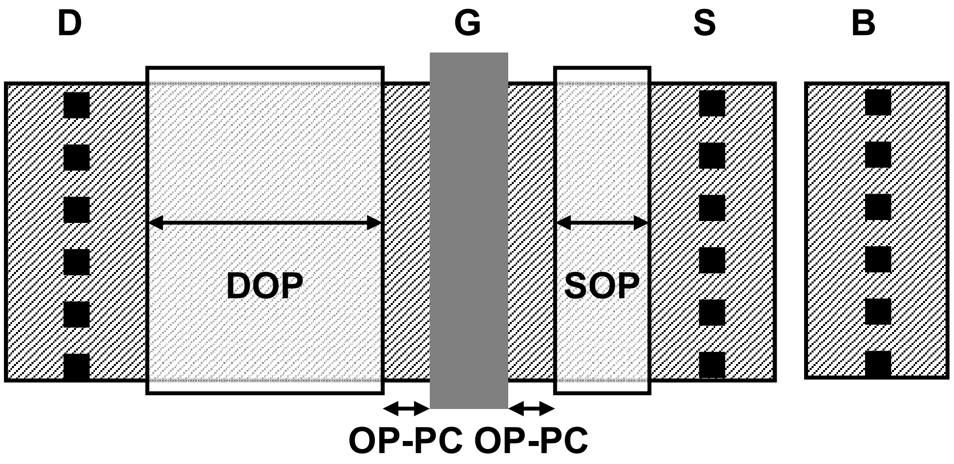

Figure 3-1: Top view of gate-silicided (GS) ESD MOSFETs. DOP and SOP are the drain and source side silicided-blocking lengths respectively. OP-PC represents the silicided region between silicide-blocked region and the poly-silicon gate.

3.2 Analysis of ESD behavior of bulk pMOSFETs

In order to design ICs with robust ESD strength, it is important to know the main design and process parameters that influence the device operation under ESD stress. The electrical and physical failure modes as well as the underlying failure mechanisms caused by the ESD stress need to be fully analyzed. Failure analysis allows insight into the influence of different process options on the robustness of the devices. In general, device damage under ESD conditions are classified as either catastrophic or latent. The catastrophic failure includes metal melting, junction breakdown or oxide failure. In contrast, latent damages cause either partial or subtle degradation.

3.2.1 ESD reliability and the underlying failure mechanisms

ESD characteristics are studied using transmission line pulsing (TLP) measurements with a 100ns rectangular pulse having 7ns rise-time, which emulates the Human Body Model (HBM), for three different device groups, mentioned above, from the 65nm bulk CMOS technology [15].

Figure 3-2 shows the variation of failure current (It2) vs. channel length for these devices. The data shown here is the average taken over 3 chips. It is seen from Figure 3-2 that the It2 of the thick-oxide (DG) devices increases with increasing channel length, while for intermediate-oxide (EG) devices the shortest channel device shows the highest It2. This behavior can be explained by the fact that with respect to channel length two competing factors play a role: First, the location of the pBJT, which forms deeper into the substrate as the channel length increases [95, 96], and second, the parasitic bipolar gain (β), which increases as the channel length decreases [89]. A schematic cross-section of the pMOSFET with parasitic PNP formed under ESD stress is shown in the Figure 3-3. For the EG devices β dominates over the pBJT location. As the channel length decreases, β increases which in turn results in higher It2. For the DG devices the pBJT forms deeper into the substrate, allowing more volume for heat to dissipate during an ESD event and thus resulting in higher It2.

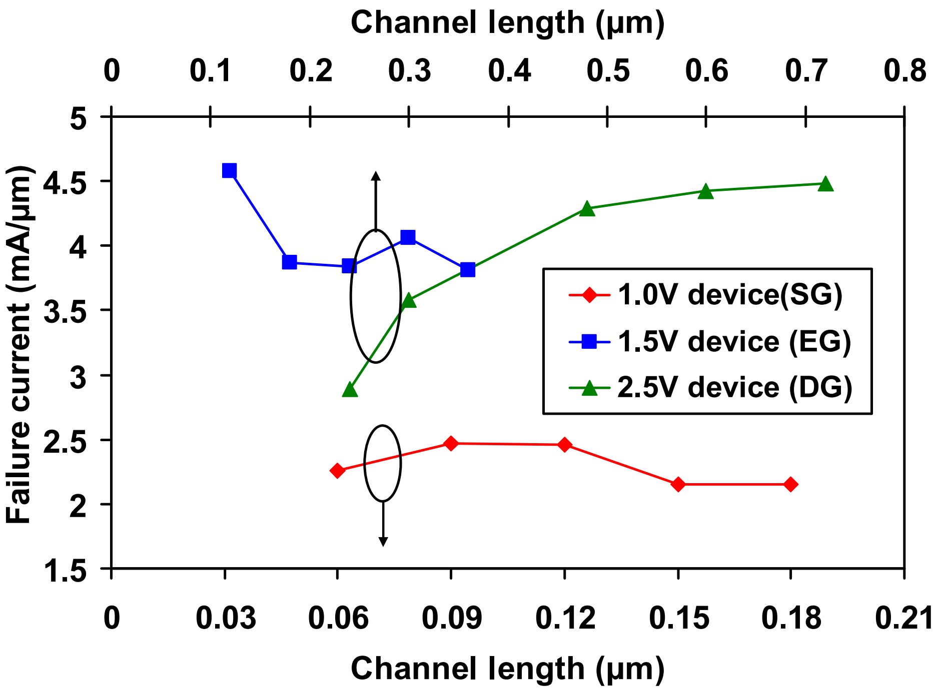

Figure 3-2: Dependence of failure current (It2) on channel length for 1.0V (Tox=1.25nm), 1.5V (Tox=2.2nm) and 2.5V (Tox=5.4nm) silicide blocked (SBlk) pMOSFET devices.

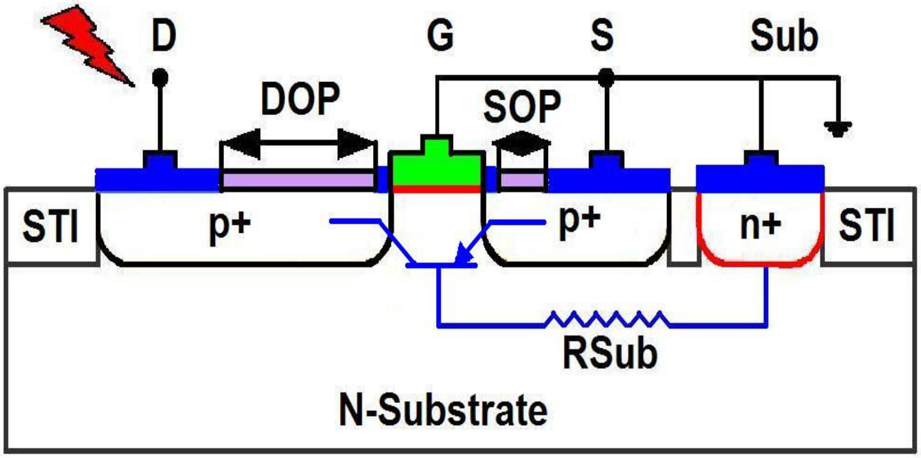

Figure 3-3: Cross-section of a silicide-blocked (SBlk) pMOSFET with a parasitic bipolar transistor (pBJT) formed under the application of negative ESD stress pulse at drain with all other terminals grounded.

To ascertain that the pBJT forms deeper into the substrate for longer channel devices, we performed device simulations using Sentaurus [97] on SG (L=0.06μm) and DG (L=0.24μm) devices, to look at the extent of the current flow lines under an applied ESD pulse at the drain. Figure 3-4 shows the simulated current density along the substrate depth by taking a cut-line at the center of the channel starting from the oxide/silicon interface. As is seen, for the DG device the current spreads much deeper into the substrate than in the SG device. This shows that in DG device due to the current spreading there is more volume for heat to dissipate through substrate.

For SG devices we expect higher It2 than for EG or DG devices, since the pBJT β increases for shorter channel devices. However, from the Figure 3-2 it is seen that the SG devices show the lowest It2. As has been argued by Bock et al [95], it may be that the power dissipation volume in the SG devices is so small, that the physical limit to hold current is reached well before the parasitic bipolar gain starts to play an effective role. This argument can be supported from Figure 3-4 where in the SG device as the current flows close to the oxide-silicon interface surface, the heat generated cannot dissipate easily through the oxide and hence, the lower power dissipation volume.

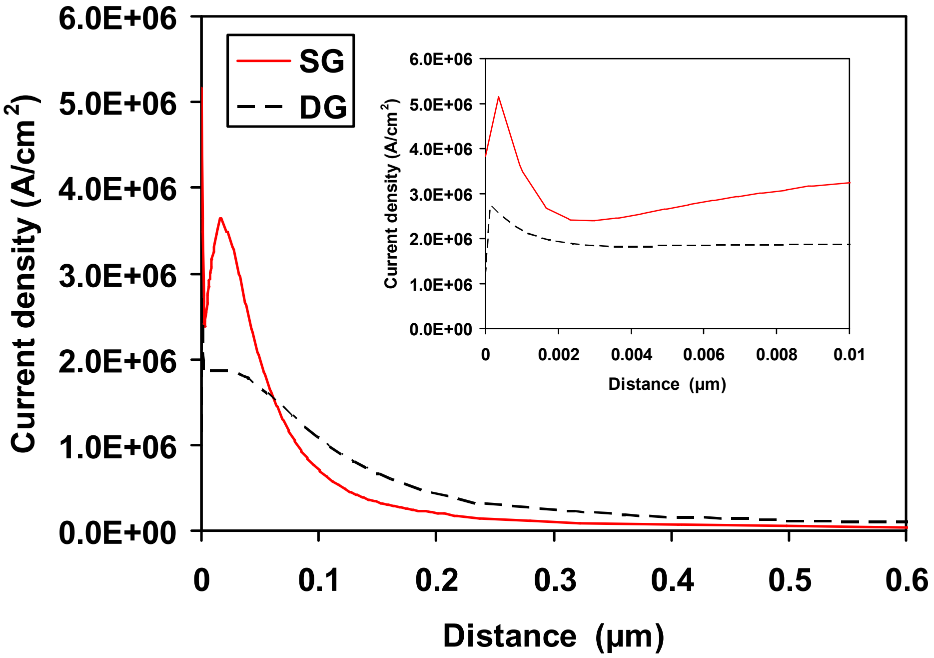

Figure 3-4: Simulated current density plotted along the substrate depth by drawing a cut line at the center of the channel, under an applied current pulse of 100ns duration at the drain for both DG (Itlp=3mA/µm) and SG (Itlp=2.3mA/µm) devices. The inset shows the current density close to the oxide/silicon interface.

3.2.2 Breakdown mode of thin-oxide pMOSFETs

In this sub-section, the breakdown mode (i.e. drain-to-source or gate oxide) of thin-oxide (SG) device under ESD stress will be determined. To determine the breakdown mode of the device, drain (Id) and gate (Ig) currents as a function of gate voltage are compared for the fresh and ESD stressed at It2 devices. As seen from Figure 3-5, an increase in both Id and Ig following stress shows that in SG devices drain to source filamentation occurs due to the thermal heating and the oxide also gets damaged as well. This mode of breakdown, where both the channel and the oxide get damaged, has been confirmed by measuring the various terminal currents after each TLP stress pulse, as shown in Figure 3-6: Id, Is and Ig all increase following ESD stress at It2.

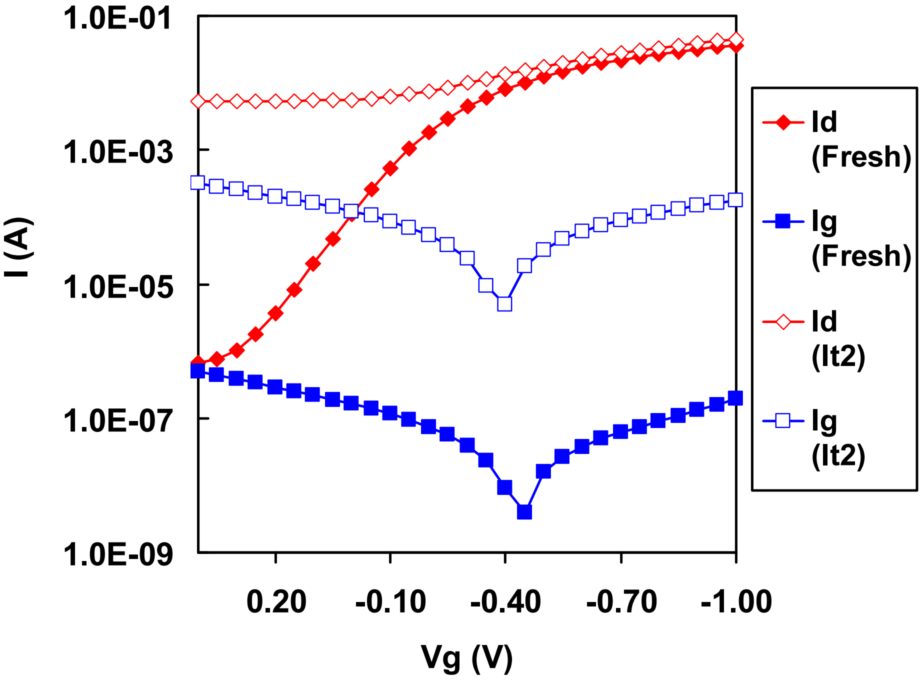

Figure 3-5: Id, Ig vs. Vg plotted for a fresh and an ESD stressed thin-oxide (SG) device with W/L=240/0.06. Both Id and Ig increase following stress at It2, indicating that both drain to source filamentation occurs due to the thermal heating and the oxide gets damaged.

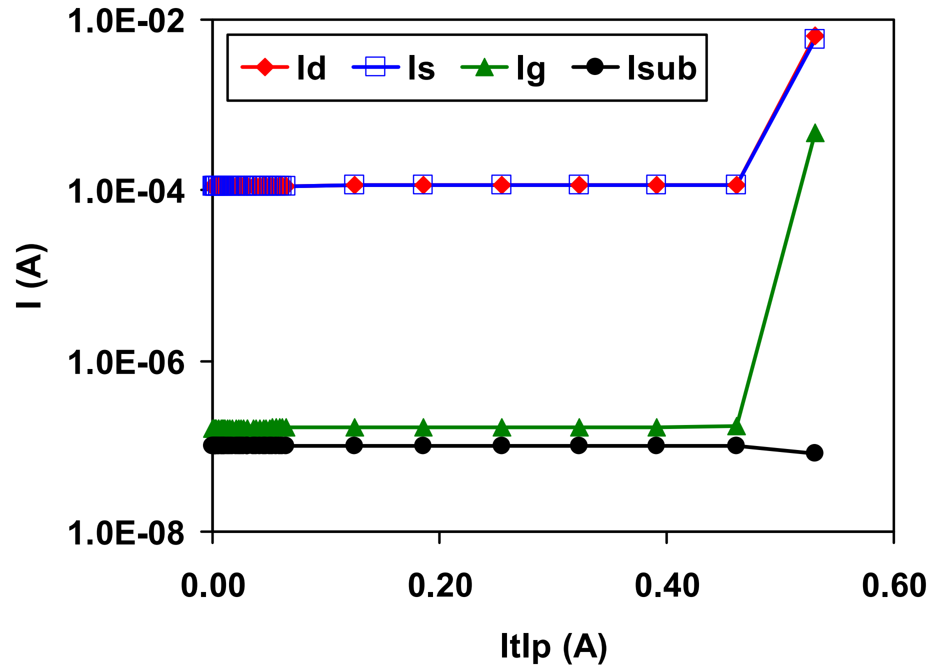

Figure 3-6: Terminal currents vs. Itlp measured after each TLP stress pulse at Vd = -1.0V for the SG device with W/L=240/0.06. Id, Is and Ig increase following stress at It2.

To probe further into the oxide breakdown in thin oxide devices we experimentally determined the electric field required to breakdown the gate oxide and compared the results with device simulation. Oxide breakdown electric field is determined by applying 100ns TLP pulses of increasing magnitude at the gate with all other terminals grounded. Following the application of each TLP pulse DC gate current was measured to know the breakdown voltage. Figure 3-7 shows such a TLP plot for a thin oxide device. It is seen that the gate oxide breaks down at a pulse magnitude of about 5V (i.e. oxide breakdown field = 5/1.25e-7cm = ~10MV/cm) and the gate current increases by more than an order of magnitude. Figure 3-8 shows the simulated electric field, using Sentaurus device simulator [97], under a current pulse (Itlp=It2=2.3mA/µm) of 100ns at drain for a thin oxide device. It is seen that the peak value of the electric field is around ~10MV/cm, which is of the same order of magnitude as determined through TLP measurements. The above analysis indicates that a combination of high temperature and high electric field leads to both drain to source and gate oxide breakdown in thin oxide devices.

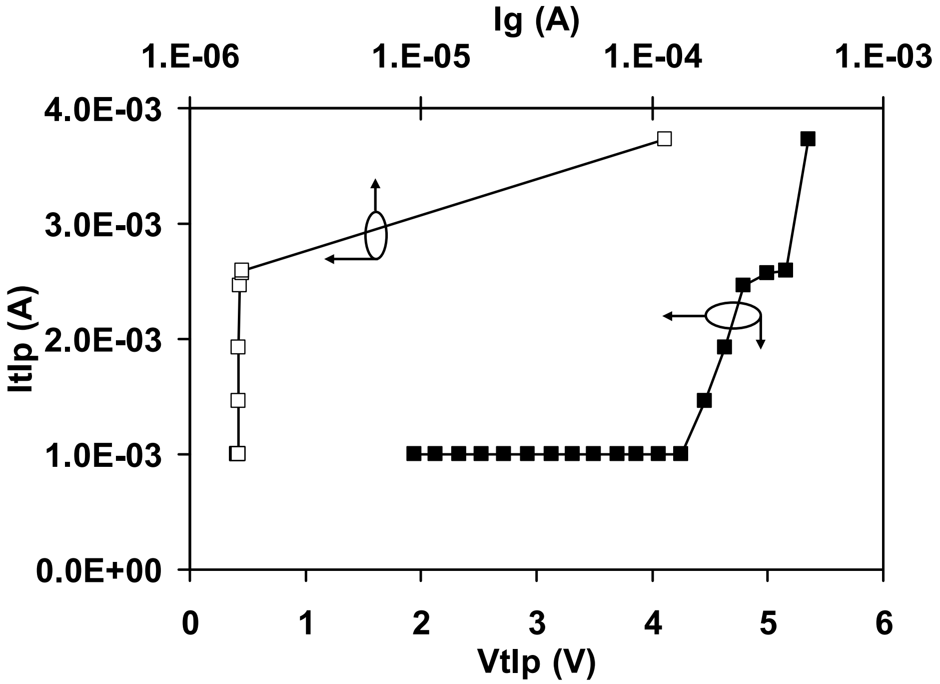

Figure 3-7: Itlp vs. Vtlp plot for a thin oxide device under the application of 100ns TLP pulses at the gate with all other terminals grounded. Also shown is the measured DC gate current at Vdd=-1.0V after the application of each TLP pulse.

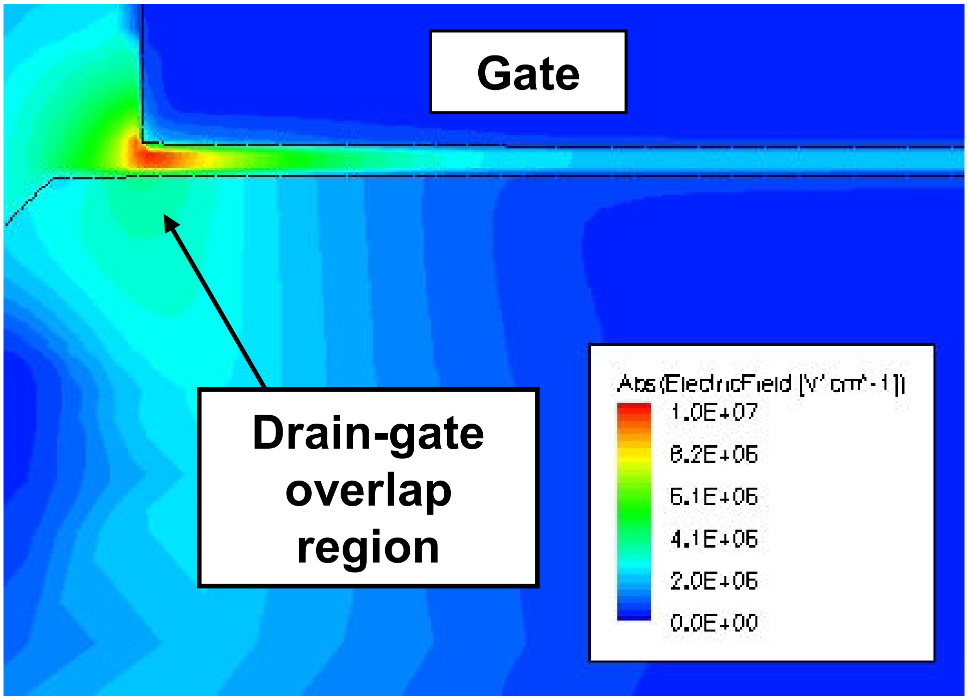

Figure 3-8: Simulated electric field under an applied current pulse (Itlp=2.3mA/µm) of 100ns duration at the drain for the SG device. The maximum electric field, which is near the edge of the gate is sufficient for oxide breakdown as determined by the measurements.

3.2.3 Breakdown mode determination of thick-oxide pMOSFETs

The breakdown mode of thick-oxide (DG) device is determined by following the same method as for thin-oxide devices. The breakdown mode of the thick-oxide (DG) device under an ESD stress at It2 is shown in Figure 3-9. An increase in Id following stress shows that only drain to source breakdown occurs. As the figure shows there is no change in Ig after the It2 stress, indicating that the gate oxide does not get damaged due to the thermal heating. This is again due to the fact that in long channel thick oxide devices the pBJT current spreads much deeper into the substrate (Figure 3-4) and gives more volume for heat dissipation through the substrate. Figure 3-10 also supports this mode of breakdown, where all the terminal currents after each TLP stress pulse are plotted vs. Itlp: only Id and Is are shown to increase.

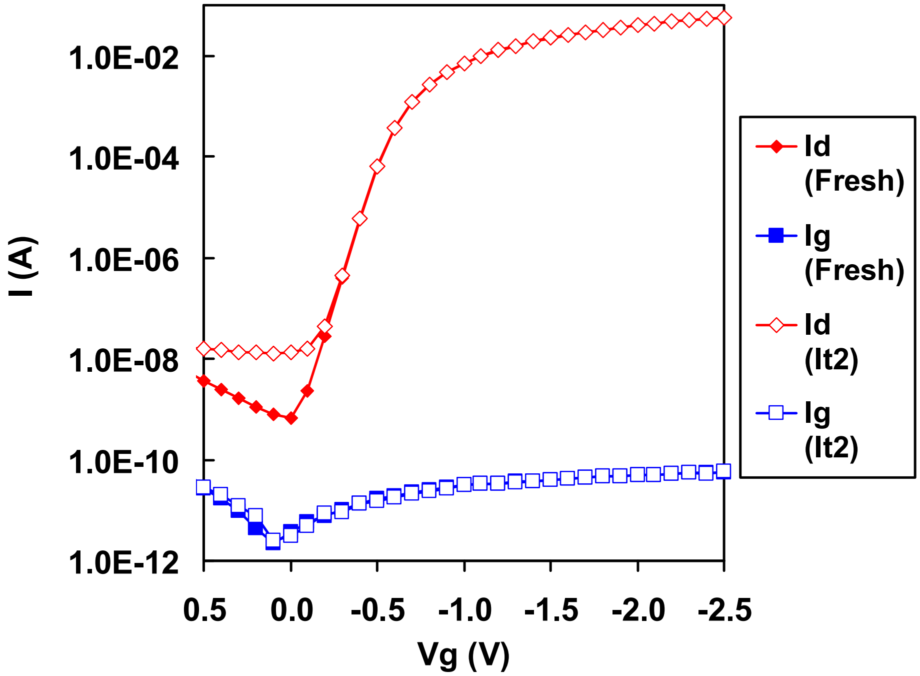

Figure 3-9: Id, Ig vs. Vg plotted for a fresh and an ESD stressed thick-oxide (DG) device with W/L=240/0.24. Only Id increases following stress at It2, indicating that only drain to source filamentation occurs due to the thermal heating.

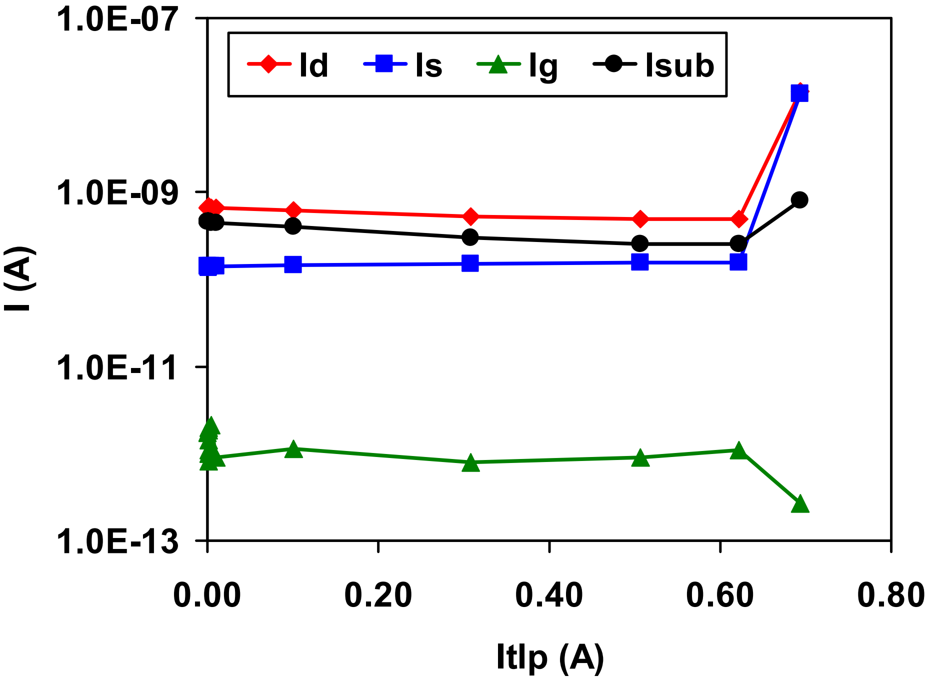

Figure 3-10: Terminal currents vs. Itlp measured after each TLP stress pulse at Vd=-2.5V for the DG device with W/L=240/0.24. Id and Is increase but Ig does not following stress at It2.

3.3 Interaction between ESD and NBTI

3.3.1 Effect of NBTI pre-stressing on ESD Characteristics

This sub-section will present the results on the effect of NBTI pre-stressing on the ESD performance. To study this interaction the devices were first NBTI stressed at high temperature. The system was then cooled down to room temperature and subsequently TLP measurements were done. DG devices were NBTI pre-stressed at Vg=-4.5V and 140^0C for 20ksec. The chuck was then allowed to cool down to room temperature and TLP stressing was done. Figure 3-11 compares the TLP I-V characteristics for a fresh and

NBTI pre-stressed SBlk pMOSFET with W/L=240/0.24. It can be seen that the NBTI pre-stressed device shows higher snapback on-resistance as compared to the fresh device. To examine the reason behind the increase in on-resistance the linear transconductance (GmLin) vs. Vg curve for the fresh and NBTI pre-stressed device is plotted in Figure 3-12. The figure shows four GmLin curves obtained sequentially from a single device:

(i) Fresh device at room temperature,

(ii) Fresh device at 140^0C,

(iii) NBTI stressed device at 140^0C, and

(iv) NBTI stressed device at room temperature.

As shown, the fresh device GmLin decreases at 140^0C and even further reduction is observed when the device is NBTI stressed. When the system is cooled down to room temperature the GmLin peak of the NBTI stressed device is lower than that of fresh device, i.e. the NBTI pre-stressed device has a higher resistance.

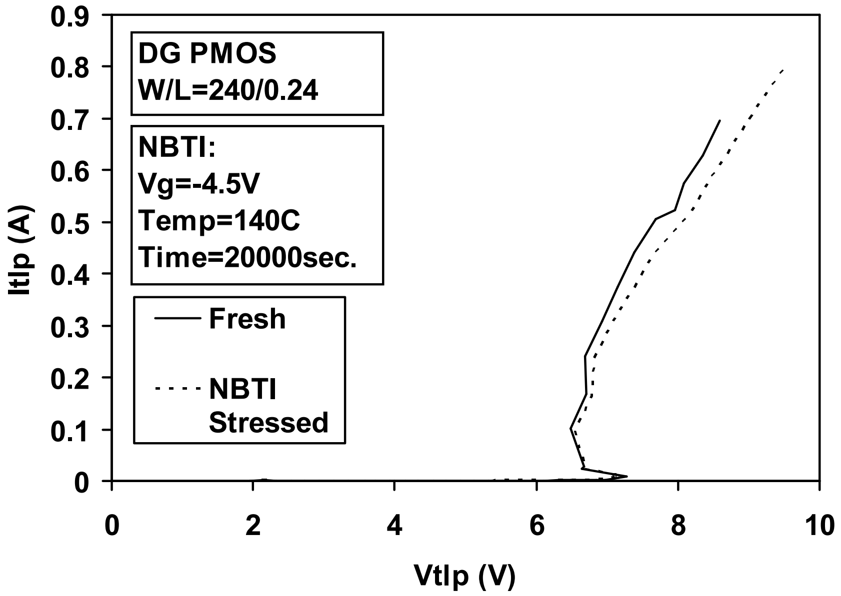

Figure 3-11: TLP I-V plots for a fresh and an NBTI pre-stressed DG device. Subsequent to NBTI stressing at high temperature, TLP was performed on the device at room temperature.

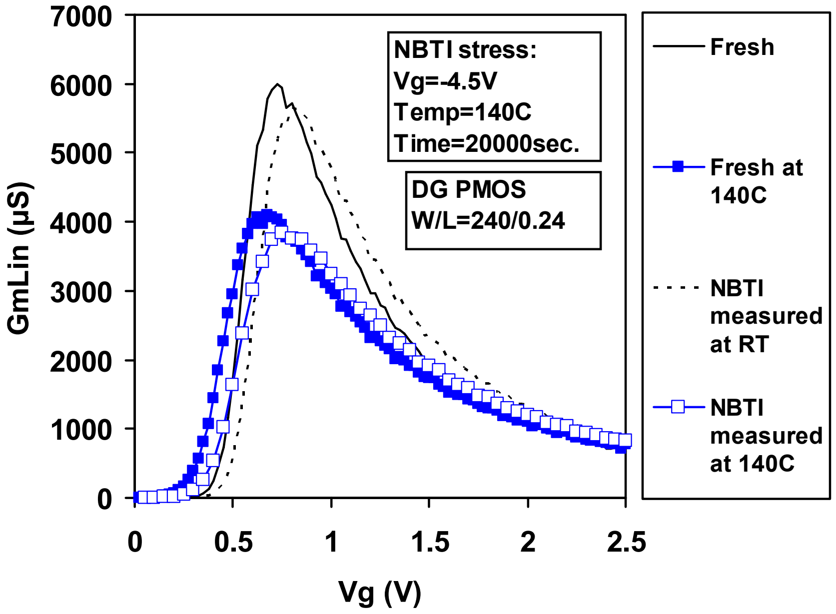

Figure 3-12: GmLin vs. Vg plots for a fresh, then NBTI stressed thick-oxide (DG) pMOSFET with W/L=240/0.24, measured at stress temperature as well as at room temperature.

Similar studies were also done on the SG and EG devices. However, the ESD behavior of SG and EG devices showed little dependence on NBTI pre-stressing, and at this point we speculate a couple of reasons that might explain this observation: NBTI pre-stressing typically introduces oxide charge and causes interface state generation in the device under stress [10]. However, whereas the effect of both these types of damage are detected on the I-V characteristics for the thick oxide (DG) devices, for the thin oxide (SG and EG) devices only the effect of the interface states is detected. This is because carrier tunneling during the I-V measurement performance in the case of thin oxide devices neutralizes the oxide charge [64]. Secondly, the resistance of the device increases as the channel length increases. In short channel devices, the resistance of the channel region constitutes a small fraction compared to what is contributed by the SBlk regions. The change in channel resistance caused by NBTI pre-stressing would therefore be small, and thus the ESD snapback on-resistance due to NBTI pre-stressing does not get affected in short channel devices.

3.3.2 Effect of ESD pre-stressing on NBTI characteristics

This sub-section will present the impact of ESD pre-stressing on the subsequent NBTI degradation behavior. This interaction is studied only for thin-oxide (SG) devices, as these devices are more prone to NBTI degradation compared to the thick oxide devices [10]. Following the non-destructive ESD pulses applied at the drain the devices were subjected to NBTI stress. In particular, SG SBlk pMOSFET with W/L=240/0.06 was ESD stressed at room temperature with non-destructive pulses up to 50% of It2

(~1.13mA/µm) and following this it was subjected to NBTI stress at Vg=-1.8V at T=140^{0}C. It can be seen from Figure 3-13 that the VtSat (saturation threshold voltage, defined as the gate voltage at which drain current equals 70 nA x (W/L) for drain voltage = Vdd) of the ESD pre-stressed device degrades ~10% more than when only NBTI stress is applied. This must be because high current stressing on the drain decreases the reliability of the oxide (e.g, by weakening the interface Si-H bonds [86]), which in turn leads to higher degradation in VtSat by the subsequent NBTI stress.

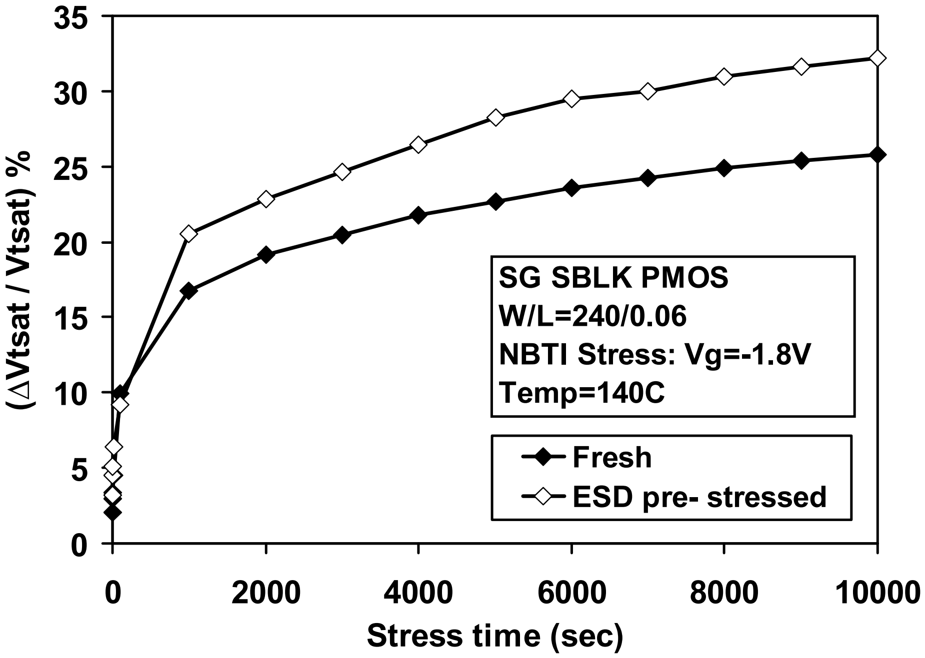

Figure 3-13: NBTI VtSat(%) shift vs. stress time, for a fresh and an ESD pre-stressed thin-oxide (SG) silicide-blocked (SBlk) pMOSFET with W/L=240/0.06.

The NBTI behavior of these devices with channel length as a parameter is shown in Figure 3-14. It shows that the nominal channel length device (L=0.06μm) degrades more as compared to longer channel length devices. Ideally, NBTI degradation should be independent of channel length as it is determined by the gate voltage alone. However, as pointed out by Yamamoto et al [50] for short channel devices, localized degradation of the oxide near the gate edge, due to the electrochemical reactions between holes and initial inactive oxide defects, can increase the NBTI. Also, Boron penetration from the source and drain diffusions into the oxide above the channel may causes generation of positive charges by electrical stress over an area which for short channel devices is a considerable part of the channel [10, 64].

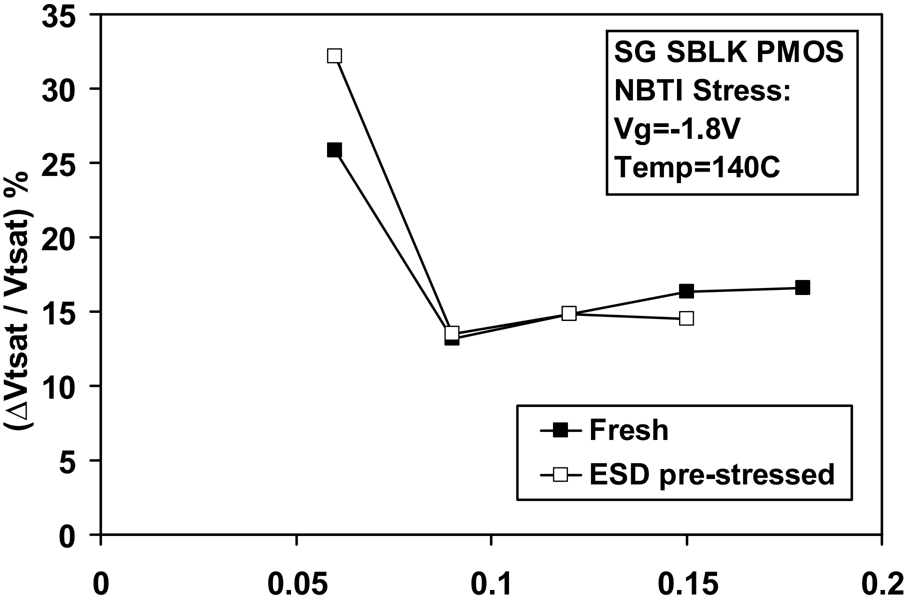

Figure 3-14: NBTI VtSat(%) shift for fresh and ESD pre-stressed thin-oxide (SG) silicide-blocked (SBlk) pMOSFETs vs. channel length.

The effect of ESD pre-stressing (~50% of It2) on NBTI behavior of the various channel lengths devices from the SG group is shown in Figure 3-14. It is found that the NBTI performance due to ESD pre-stressing gets affected only for the nominal channel length device. For longer channel length devices the ESD pre-stressing does not have significant effect on NBTI characteristics. This is because while for the nominal channel length device the turn-on region of pBJT is close to the gate oxide/channel interface, for the longer channel length devices it moves deeper towards the bottom of diffusion region [95, 96]. This prevents the oxide interface from being weakened by the ESD pre-stress for the long channel devices.

3.4 HCI and NBTI behavior of pMOSFETs and their interaction

NBTI and HC stressing were performed to identify the worst-case degradation mechanism for SBlk pMOSFETs. We chose 240μm wide SG SBlk pMOSFETs with channel length as a parameter. The three channel lengths of these devices are 0.06μm, 0.09μm, and 0.12μm. The identification of stress condition with worst degradation at the operating voltage is critical for proper selection of the bias conditions to be used during accelerated testing. Different stress conditions are explored for these devices to find the worst-case stress (WCS) configuration. The devices were NBTI stressed at 140^0C at Vg=-1.8V. The hot carrier stressing (HCS) was done under two different bias conditions at 140^0C: (a) Vg=Vd=-1.8V and (b) Vg@Isub(max.), Vd=-1.8V.

Figures 3-15, 3-16 and 3-17 show the saturation threshold voltage change (ΔVtSat) vs. stress time for L = 0.06μm, 0.09μm and 0.12μm respectively. As can be seen from these figures, under HCS at high temperature, worst degradation occurs at stress condition Vg=Vd and not at the maximum substrate current. An interesting observation from these figure is that the degradation at 140^0C in the case of L=0.09 and 0.12µm devices (Figs. 3-16 and 3-17) for stress under Vg=Vd parallels the NBTI degradation. The observed similar time dependence of NBTI and HCI (Vg=Vd stress) shows that at high temperature under Vg=Vd stress the degradation is induced by both NBTI and HCI simultaneously i.e. concurrent “HCI-NBTI” activation. It is also observed from Figures 3-16 and 3-17 that the degradation under NBTI stress dominates over degradation under HCS condition in these devices. For the short channel device (L=0.06µm), as shown in Figure 3-15, the degradation rate under HCS is higher than NBTI. Thus channel length dependent degradation mode at high temperature under Vg=Vd stress reveals that “NBTI-like” degradation dominates in long channel devices whereas concurrent “HCI-NBTI” degradation dominates in short channel devices.

The dominance of NBTI under Vg=Vd stress condition at high temperature for the long channel devices can be explained with the help of Figure 3-18. In long channel devices, during HCS, a large portion of channel on the source side remains populated with holes. These holes cover a substantial portion of the channel and cause NBTI like degradation whereas near the drain the oxide is damaged by hot carriers [98]. By contrast, in short channel devices, as shown in Figure 3-18 (b), the application of drain stress bias depletes most of the channel and the degradation is the result of the concurrent HCI and NBTI.

Guerin et al [99] have found that even at room temperature the degradation time dependence under Vg=Vd stress condition is same as that for NBTI stress. Hence, HCS was also performed at room temperature and the results are plotted in Figures 3-15, 3-16 and 3-17 for L = 0.06µm, 0.09µm and 0.12µm respectively. For these SBlk pMOSFET devices, it is found that degradation at room temperature is negligible for all the channel length devices and stress voltages examined.

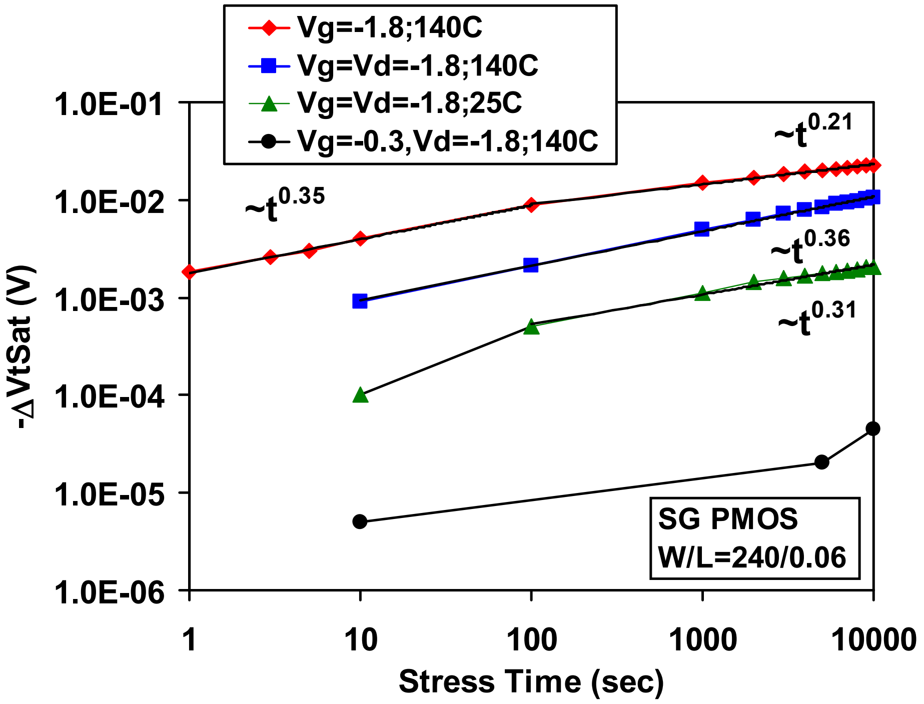

Figure 3-15: Saturation threshold voltage shift (ΔVtSat) vs. stress time for different stresses for thin-oxide (SG) silicide-blocked (SBlk) pMOSFETs with W/L=240/0.06.

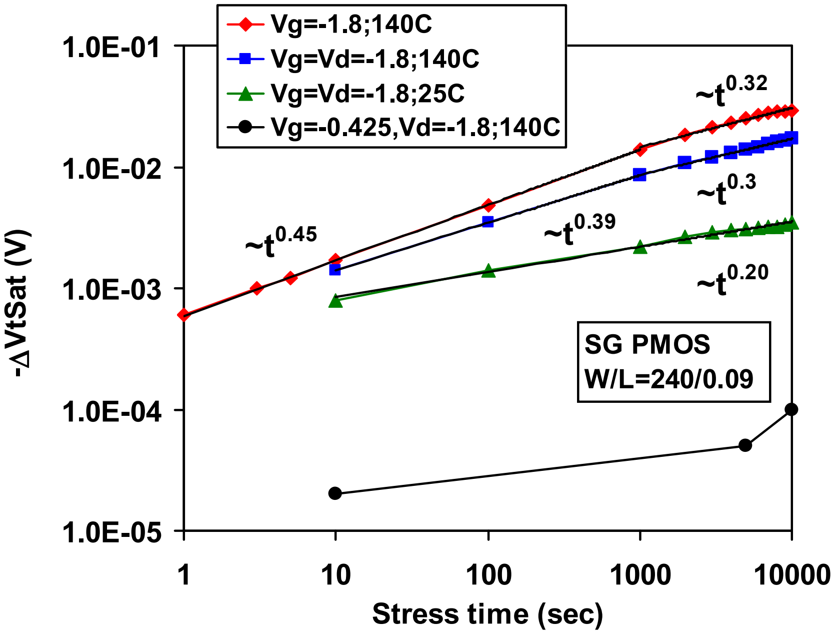

Figure 3-16: Saturation threshold voltage shift (ΔVtSat) vs. stress time for different stresses for thin-oxide (SG) silicide-blocked (SBlk) pMOSFETs with W/L=240/0.09.

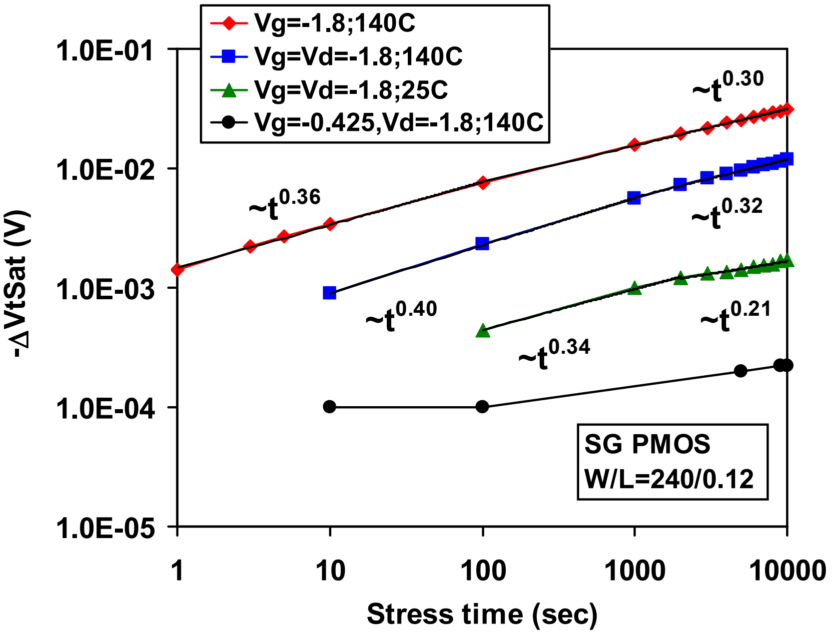

Figure 3-17: Saturation threshold voltage shift (ΔVtSat) vs. stress time for different stresses for thin-oxide (SG) silicide-blocked (SBlk) pMOSFETs with W/L=240/0.12.

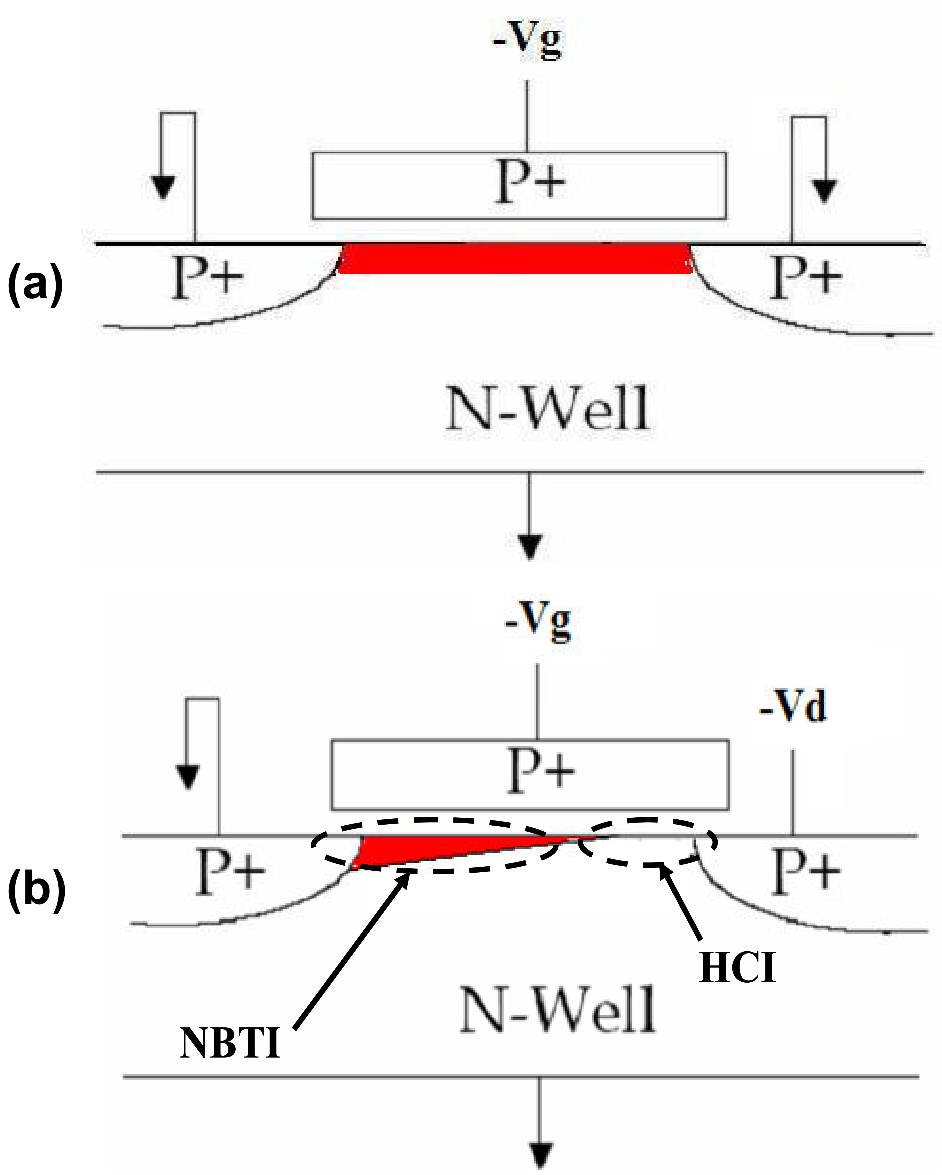

Figure 3-18: (a) pMOSFET under NBTI stress configuration- The complete channel is occupied by holes (b) pMOSFET under HCI stress configuration- The application of drain voltage depletes the channel and the rest of the channel region near the source is occupied by holes. These holes cause NBTI-like degradation near the source whereas near the drain the oxide is damaged by hot carriers.

3.5 Conclusion

A comprehensive study on the interaction between electrostatic discharge (ESD), negative bias temperature instability (NBTI) and hot carrier injection (HCI) on silicide-blocked (SBlk) pMOSFETs is presented for a state-of-the-art 65nm bulk CMOS technology, with three oxide thickness values and channel length as a parameter. It is found that the thin and thick oxide devices exhibit opposite ESD behavior with respect to channel length. The role of the gain of pBJT and its location during an ESD event is identified with respect to channel length variation. It is also found that as the channel length decreases the resulting small heat dissipation volume becomes a major ESD performance-limiting factor. The interaction between ESD and NBTI showed that the thick oxide when NBTI pre-stressed exhibit high ESD snapback on-resistance. Similarly, the NBTI characteristics of the thin oxide device degrade more when the device is pre-stressed with non-destructive ESD pulses. The saturation threshold voltage shift increases by ~10% due to ESD pre-stressing as compared to NBTI-only stressed device. NBTI studies on thin oxide devices revealed channel length dependent behavior, whereby the shortest channel length device shows the highest degradation. The NBTI and HCI studies on thin oxide devices with channel length as a parameter show that for long channel device NBTI stress at high temperature is the worst degradation mode, whereas for short channel device it is HCS at high temperature. It is found that degradation under HCS at high temperature is caused by both NBTI and HCI simultaneously (concurrent "HCI-NBTI") and the relative importance of these mechanisms depends on the channel length.

Additionally, it is shown that degradation under HCS at high temperature is worse than at room temperature due to this NBTI co-activation.

4. ESD, NBTI and HCI investigation of nano-scale SOI MOSFETs

The inherent structural advantages of SOI technology such as reduced parasitic capacitances, low sub-threshold slope, higher drive current, and reduction of short channel effects, makes it an attractive solution for VLSI circuits over bulk technology. However, the presence of the buried oxide undermines the electrostatic discharge (ESD) reliability of the SOI devices; this is because the heat generated during an ESD event cannot dissipate easily due to the low thermal conductivity of the buried oxide. Thus, SOI MOSFETs exhibit lower current handling capability than the corresponding bulk devices. Nevertheless, as the technology scales down, a growing interest in the SOI based circuit design makes it necessary to evaluate the ESD behavior of these devices. The next section will explore ESD robustness of silicide-blocked (SBlk) SOI MOSFETs from 65nm technology designed for SRAM and logic applications [16].

This chapter will also present the study of NBTI and HCI on high-speed/core-logic (thin-oxide) and input/output (thick-oxide) SOI pMOSFETs. These devices are silicided devices as opposed to SBlk devices used for ESD protection. Generally, for ESD protection, drain and source diffusion region are blocked during the silicidation process to provide the high resistance. This resistance, called ballistic resistance, helps to distribute current uniformly from drain to source during an ESD event. In case of high-speed/core devices or I/O devices the drain and source region are silicided to reduce the parasitic resistance, thus increasing the on-current of the device.

The NBTI and HCI reliability of high-speed/core-logic (thin-oxide) and input/output (thick-oxide) SOI pMOSFETs will be studied for both grounded-body and floating body devices. The role of gate-tunneling current, self-heating and stress bias is particularly explored.

4.1 Analysis of ESD behavior of SOI MOSFETs

Recently, there have been a number of publications [40, 41, 100-102] on the ESD behavior of SOI devices. Khazhinsky [100] has attempted to import the bulk-specific ESD network design to the SOI and showed that the distributed and boosted rail clamp ESD networks based on SOI are only slightly less area efficient than comparable bulk designs. Mitra et al [101] have shown that the inherent floating body effect (FBE) in SOI MOSFETs can be utilized for designing the input/output (I/O) circuits with improved ESD characteristics. They have also shown the superior performance of floating body SOI nMOSFETs compared to bulk and body-tied devices. In [103] the floating charge effect is considered in the design of ESD nMOSFETs from 90nm bulk technology. A significant improvement is demonstrated in the ESD robustness of devices with floating charge compared with the conventional structure. Now as the technology scales down, further studies are required to evaluate the ESD performance of SOI MOSFETs.

The ESD behavior of silicide-blocked (SBlk) SOI MOSFETs from 65 nm technology designed for SRAM and logic applications [16] will be studied using transmission line pulsing (TLP) measurements. From the ESD perspective, pMOSFETs have not received much attention due to the lower parasitic bipolar gain (pBJT) gain than the similar sized nMOSFETs. However, as the technology scales the pBJT characteristics improve and pMOSFETs begin to compete with nMOSFETs [90, 91]. In this study of the ESD behavior of SOI devices both n and p channel MOSFETs are studied. Both thin and thick oxide devices and the impact of device (silicide-blocking length) and layout (gate-silicided and gate-non-silicided) design on the ESD performance are explored. It is shown that inherent floating body charge in the SOI MOSFETs helps to improve the ESD characteristics. It is also observed that the thin oxide pMOSFETs exhibits failure current comparable to the corresponding nMOSFETs but at the expense of higher power dissipation. The comparison between gate-silicided (GS) and gate-non-silicided (GNS) nMOSFETs shows that the GNS devices have higher failure current. The ESD behavior of GNS devices with different stress pulse width shows that these devices suffer more from self-heating than the similar sized GS devices. The robustness of GS and GNS devices throughout the EOS/ESD regimes is also determined by generating the power-to-failure vs. time-to-failure curves over a wide spectrum of stress times.

4.1.1 Device details

ESD characteristics of MOSFETs from the 65nm SOI CMOS technology [15] are studied using transmission line pulsing (TLP) measurements. This is a twin well partially depleted SOI technology with two different gate oxide thicknesses: (a) Thin oxide (SG) devices (Vdd=1.0V, Tox=1.05nm), (b) Thick oxide (DG) devices (Vdd=1.5V, Tox=2.35nm). The nominal channel lengths for SG and DG devices are L=0.06µm and L=0.12µm respectively. ESD behaviors of both n and p channel MOSFETs are studied. Both devices that employed independently biased H-type body contacts (BCs) and floating body (FB) devices without BCs were available in each case. The ESD behavior of nMOSFETs is explored for gate-silicided (GS) and gate-non-silicided (GNS) designs. The top-views of the GS and GNS designs are shown in Figure 4-1(a) and 4-1(b) respectively. Both of these designs have silicide-blocked regions on the drain and the source to provide ballistic resistance [94] to improve the ESD current uniformity across the width of the device. The DOP and SOP in the Figure 4-1 are the lengths of the silicide blocked regions on the drain and source side respectively. In the GS design, two small silicided regions, op-pc, exist between drain/source silicide blocking and the gate. The op-pc spacing in the GS designs is constant (=240nm) irrespective of the variations in DOP/SOP lengths. In the GNS design, shown in Figure 4-1(b), the silicided blocking layer is placed across the drain, gate and source thus, leaving both the gate and the op-pc area silicide blocked.

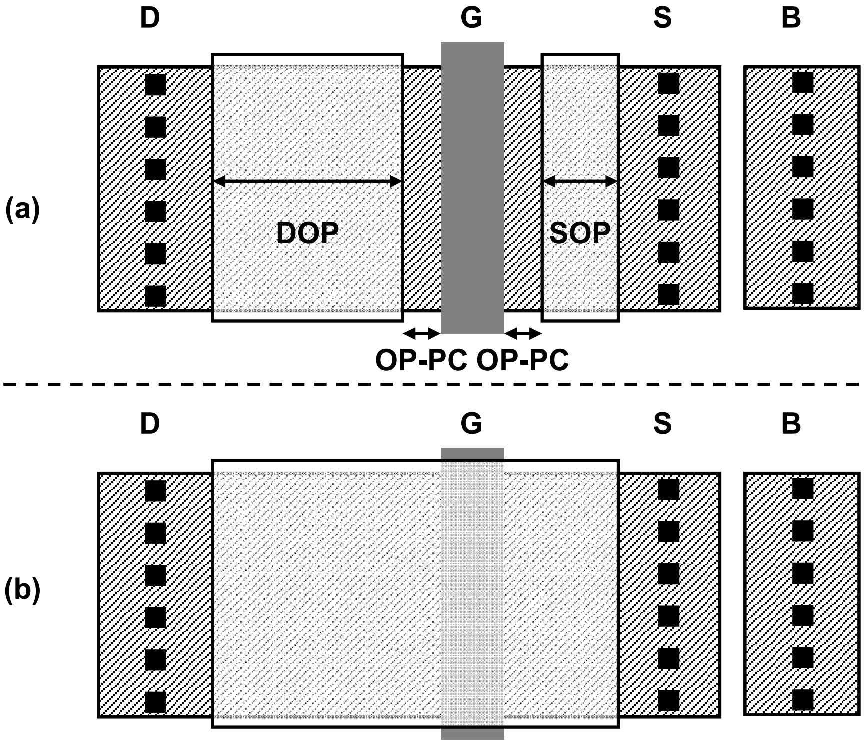

Figure 4-1: Top view of (a) gate-silicided (GS) and (b) gate-non-silicided (GNS) drain/source silicide-blocked (SBlk) MOSFETs. DOP and SOP are the drain and source side silicided-blocking lengths respectively. OP-PC represents the silicided region between silicide-blocked region and the poly-silicon gate.

4.1.2 ESD behavior of gate-silicide (GS) MOSFETs

4.1.2.1 Floating body vs. grounded body operation

This section will explore the effect of floating body and grounded body on the ESD robustness of gate-silicided (GS) SOI pMOSFETs. Figure 4-2 shows the TLP I-V curve, obtained with 100ns pulse width, for the BC device with grounded body (GB) and floating body (FB) pMOSFET device. It is seen that for the similar width devices the floating body reduces the turn on voltage and improves ESD performance compared to the grounded body device. The reduction in turn-on voltage in floating body device is due to the fact that the avalanche generation current required to turn on the pBJT will be lower than in the body grounded case. The floating body charge will supply the potential to turn-on the substrate-source junction. This decrease in turn-on voltage is useful for the ESD protection design in nano-scale MOSFETs. As the gate-oxide thickness decreases with technology scaling, the difference between the turn-on voltage of the pBJT and the gate-oxide breakdown voltage diminishes. This increases the probability of gate-oxide damage during ESD stressing. The decrease of turn-on voltage of pBJT in the floating body device will thus ensure that the ESD device will turn-on before the gate-oxide breakdown occurs. The GB device, as shown in Figure 4-2, holds almost no current and fails as soon as the device enters snapback. Similar behavior is observed between GB and FB nMOSFETs. Hence, the further ESD analysis was done only for the floating body n and p channel MOSFETs.

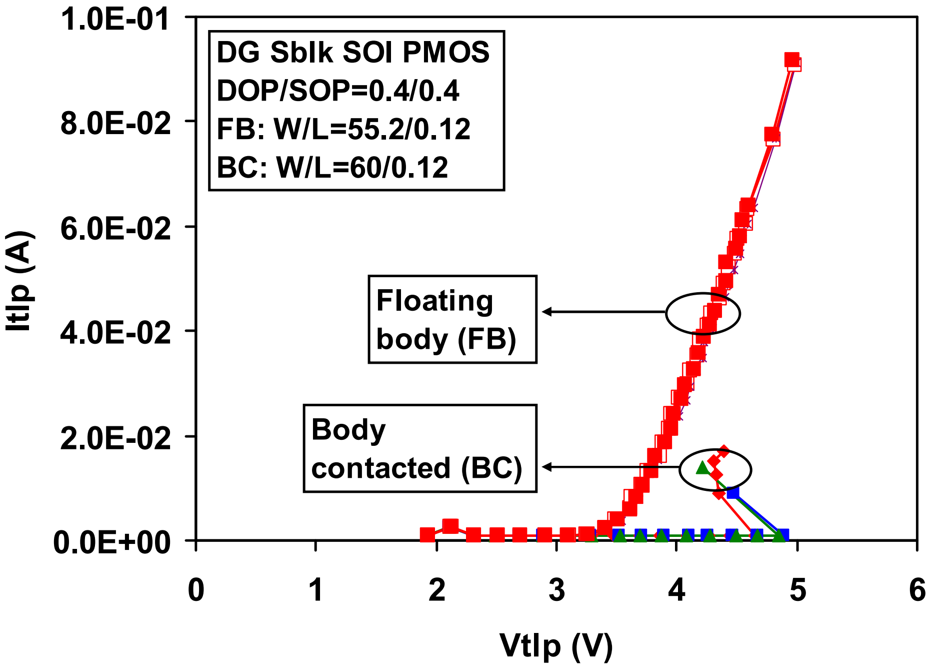

Figure 4-2: TLP I-V plots obtained with 100ns square pulse width for body contacted (grounded body) and floating body silicide-blocked (SBlk) thick-oxide (DG) SOI pMOSFETs.

4.1.2.2 ESD robustness of n and p SOI MOSFETs

Figure 4-3 shows the ESD characteristics of the n and p channel floating body SOI MOSFETs, obtained with 100ns TLP pulse, for both thin (SG) and thick (DG) oxide devices. As is seen from the figure, the turn-on voltage of the pMOSFETs is higher than the similar sized nMOSFETs. In addition, the pMOSFETs show higher on-resistance. The higher turn-on voltage and the higher on-resistance of the pMOSFETs compared to the similar sized nMOSFETs is due to the lower mobility of holes than electrons. Low hole mobility results in lower current gain of parasitic lateral PNP bipolar transistor and hence, failure at lower currents. Nevertheless, it is interesting to note from Figure 4-3 that the current handling capability of SG pMOSFET is almost same as that of SG nMOSFETs, though at the expense of higher power consumption.

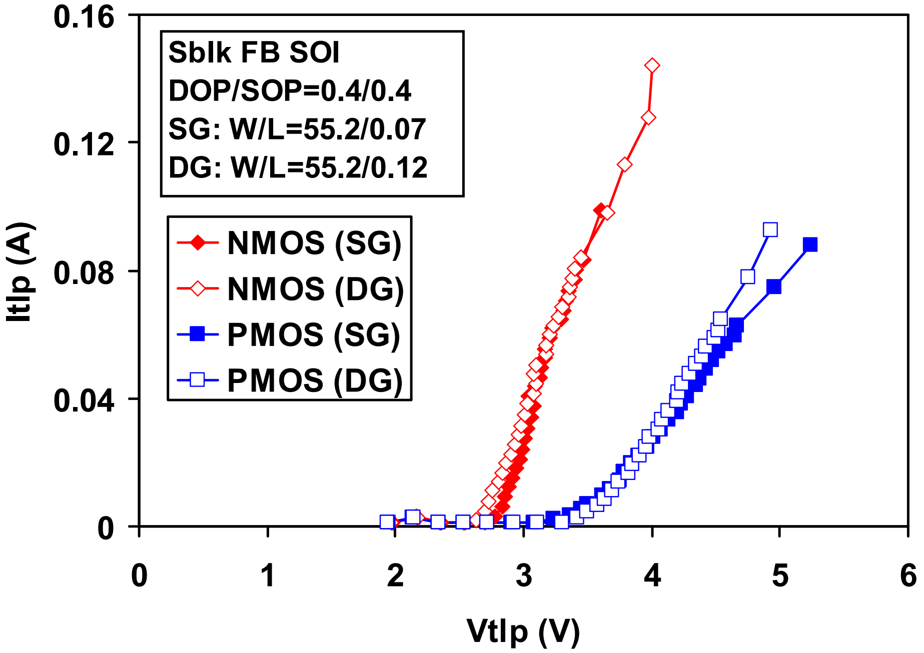

Figure 4-3: TLP I-V plots of the thin (SG) and thick (DG) oxide floating body silicide-blocked (SBlk) SOI n and p channel MOSFETs obtained with 100ns square pulse width.

4.1.2.3 Extraction of power-to-failure (Pf) vs. time-to-failure (tf) curves

The TLP measurements of these devices are compared further for different stress pulse widths to determine the overall EOS/ESD robustness. Figures 4-4 and 4-5 show the power-to-failure vs. time-to-failure curves for the SG and DG devices respectively. The power-to-failure is defined as the product of secondary breakdown voltage (Vt2) and current (It2). For SG devices, the pMOSFETs power dissipation is much more than the corresponding nMOSFETs. For DG devices, the power dissipation for pMOSFETs is slightly less than the nMOSFETs.

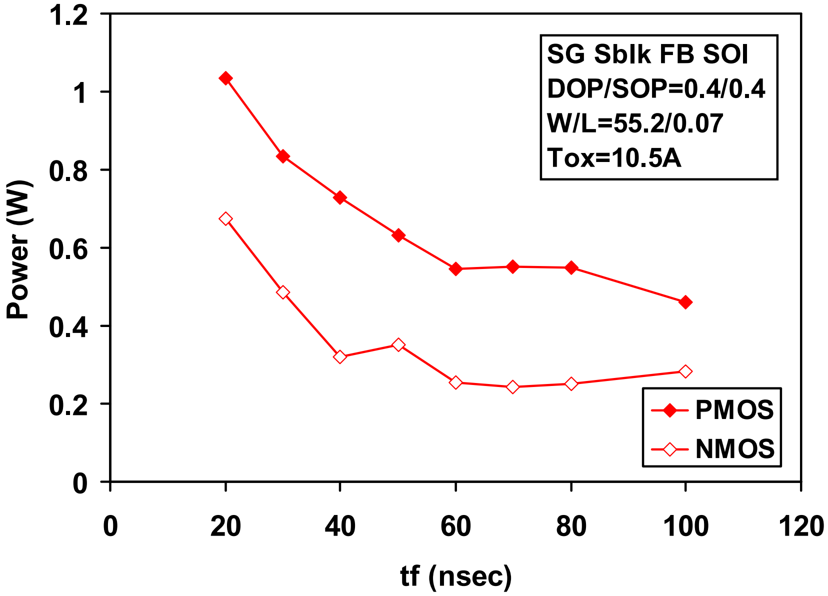

Figure 4-4: Power-to-failure (Pf) vs. time-to-failure (tf) curves for the thin-oxide (SG) floating body silicide-blocked (SBlk) SOI n and p channel MOSFETs.

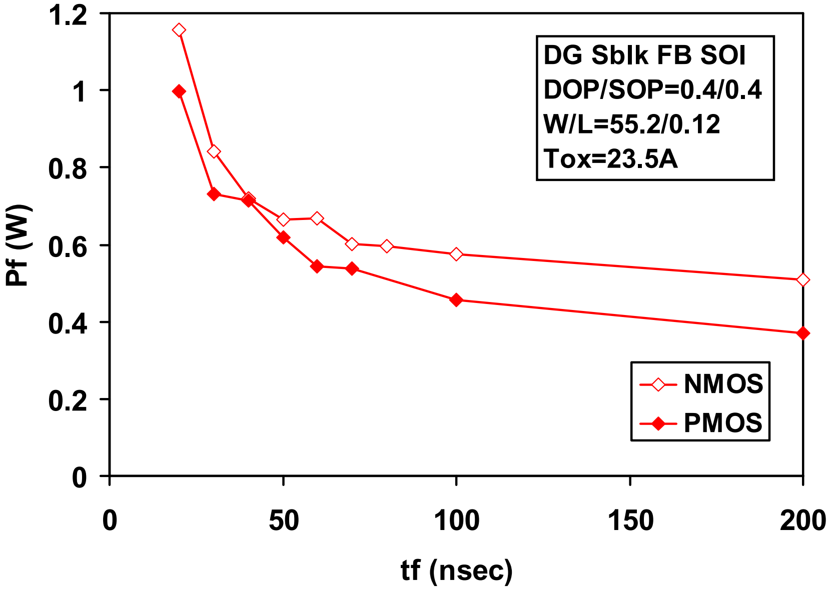

Figure 4-5: Power-to-failure (Pf) vs. time-to-failure (tf) curves for the thick-oxide (DG) floating body silicide-blocked (SBlk) SOI n and p channel MOSFETs.

4.1.2.4 ESD stress pulse width effect on GS SOI pMOSFETs

Figures 4-6 and 4-7 plots the TLP I-V curves for the SG and DG SOI nMOSFETs respectively, obtained with 30ns and 100ns pulse widths for different DOP and SOP values. As seen from the figures, in both devices, an increase in either DOP or SOP length increases the snapback on-resistance and hence, the power dissipation. TLP curves with short (30ns) and long (100ns) pulse width reveals self-heating in DG devices in Figure 4-7. The curve obtained with 100ns stress pulse width shows higher resistance than the one obtained with 30ns pulse width. This behavior is prominent for the devices with large DOP and/or SOP values. The pulse width dependent self-heating behavior is further illustrated in Figure 4-8 for the DG nMOSFETs with the largest available DOP/SOP=1.0/1.0 lengths. The figure shows that the device exhibits higher on-resistance as the stress pulse width increases. The device shows maximum on-resistance when the I-V curve is generated using DC measurements. The large lengths of DOP and/or SOP mean a higher resistive path for the current flow and hence, higher power dissipation. The generated heat cannot escape easily through the gate and the buried oxide which results in the decrease in the hole mobility and thus, higher on-resistance.

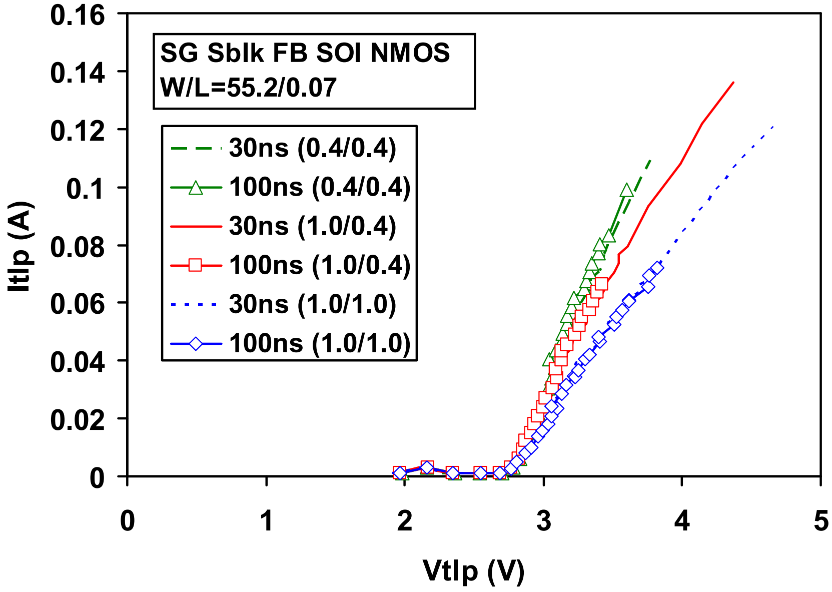

Figure 4-6: 30ns and 100ns TLP I-V plots for the thin-oxide (SG) floating body silicide-blocked (SBlk) SOI nMOSFETs with different DOP/SOP values.

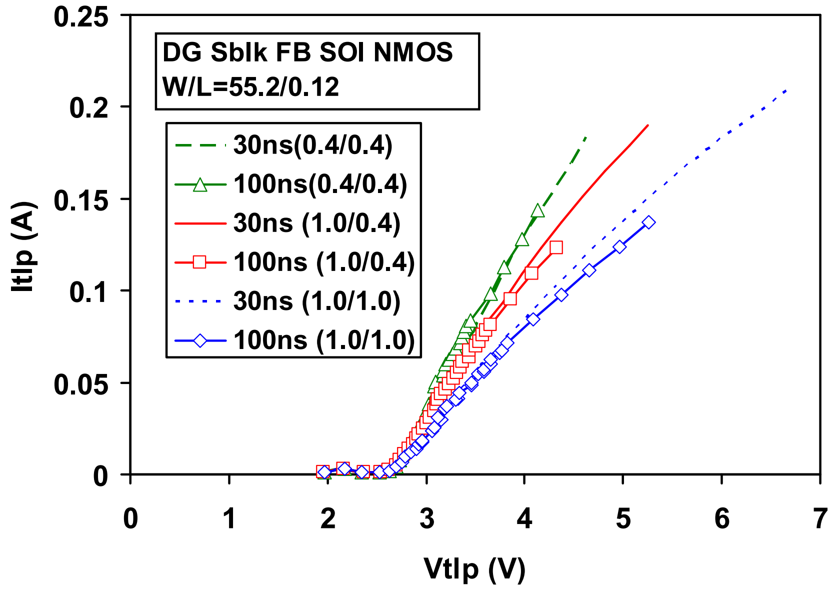

Figure 4-7: 30ns and 100ns TLP I-V plots for the thick-oxide (SG) floating body silicide-blocked (SBlk) SOI nMOSFETs with different DOP/SOP values.

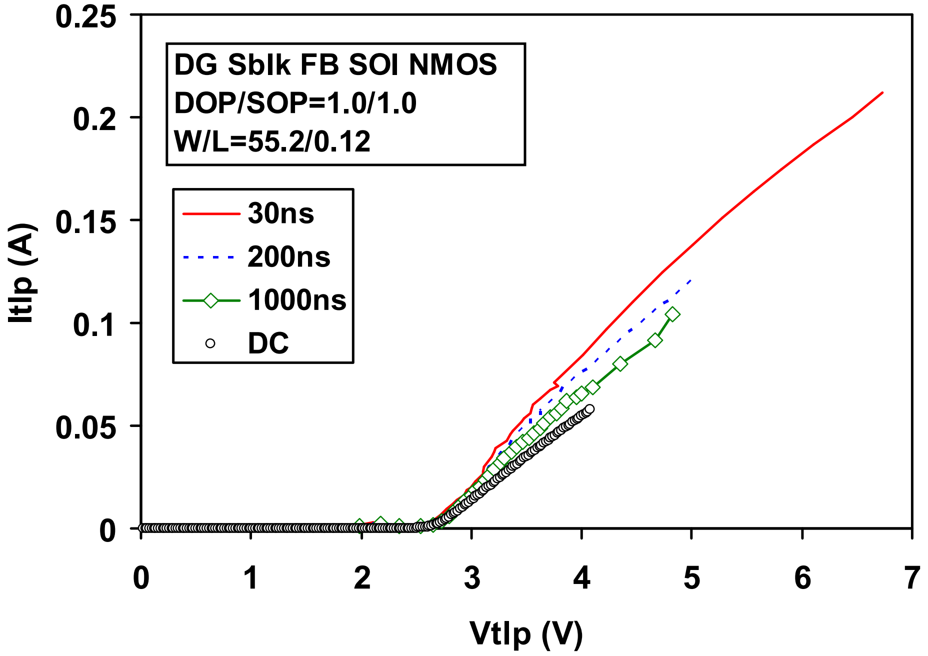

Figure 4-8: TLP I-V plots for thick-oxide (DG) floating body silicide-blocked (SBlk) SOI nMOSFETs obtained with different stress pulse widths. Also shown is the curve obtained under DC conditions.

4.1.3 ESD behavior of gate-non-silicided (GNS) MOSFETs

4.1.3.1 ESD reliability of GS and GNS MOSFETs

This section presents the results on the ESD behavior of gate-non-silicided (GNS) floating body SOI nMOSFETs. Figure 4-9 compares the TLP I-V curves obtained with 100ns pulse width for GS and GNS designs for both SG and DG SOI nMOSFETs. It is seen that, while GS nMOSFETs have same I-V characteristics as similar sized GNS nMOSFETs before they reach failure, the GNS devices give much higher failure current than GS devices. The GS designs of thin and thick oxide nMOSFETs show failure currents ~1.8mA/µm and ~3mA/µm, whereas, the GNS designs show failure currents of ~2.5mA/µm and ~4mA/µm respectively. Thus, an improvement in the failure current of about 70-75% is observed for both thin and thick oxide GNS devices over similar sized GS devices. The improvement in the failure current in GNS device is due to the elimination of the silicided region (i.e. OP-PC) between the source/drain silicide blocking and the poly-silicon gate. It was shown by Li et al [104] in bulk devices that due to the current crowding in the silicided OP-PC region of GS design a fast increase in lattice temperature is observed compared to the GNS design. The current crowding in GS design gives rise to higher peak temperature than in the GNS design and thus, results in the failure at lower current. They have also shown [104] through device simulations that, for the GNS design, the current density remains evenly distributed as the silicidation between drain/source and poly-silicon gate is blocked. The fast temperature increase due to current crowding will be more prominent in GS SOI devices due to the presence of buried oxide and hence, failure at lower current.

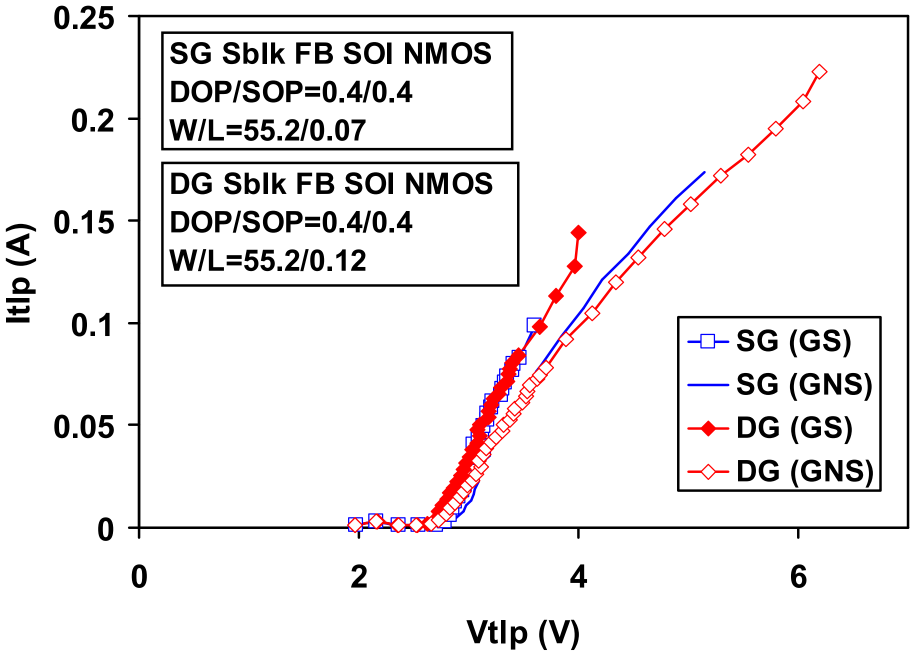

Figure 4-9: 100ns TLP I-V plots for thin (SG) and thick (DG) oxide floating body silicide-blocked (SBlk) SOI nMOSFETs with gate-silicided (GS) and gate-non-silicided (GNS) designs.

4.1.3.2 ESD stress pulse width effect on GNS MOSFETs

To further investigate the ESD behavior of GNS devices, the TLP measurements with stress pulse width variation were done on both SG and DG nMOSFETs. Figures 4-10 and 4-11 plot the TLP curve for SG and DG nMOSFETs respectively, with three different pulse widths. It is seen from the figures that both the SG and DG devices exhibit pulse width dependent self-heating behavior. The on-resistance of the device increases with increase in applied stress pulse width. The pulse width dependent behavior for gate-non-silicided SG devices (Figure 4-10) is different from the corresponding gate-silicided devices (Figure 4-6) in terms of self-heating. As seen earlier in Figure 4-6, the gate-silicided SG device did not exhibit self-heating, probably due to the lower current and voltage capability than the corresponding gate-non-silicided device. In DG devices, as shown in Figure 4-11, the effect of self-heating kicks-in once the applied ESD current crosses a threshold of 3.3V. The resistance increases with increasing pulse width and the curve tends to saturate at higher voltage values. The self-heating decreases the hole mobility and hence the higher on-resistance observed.

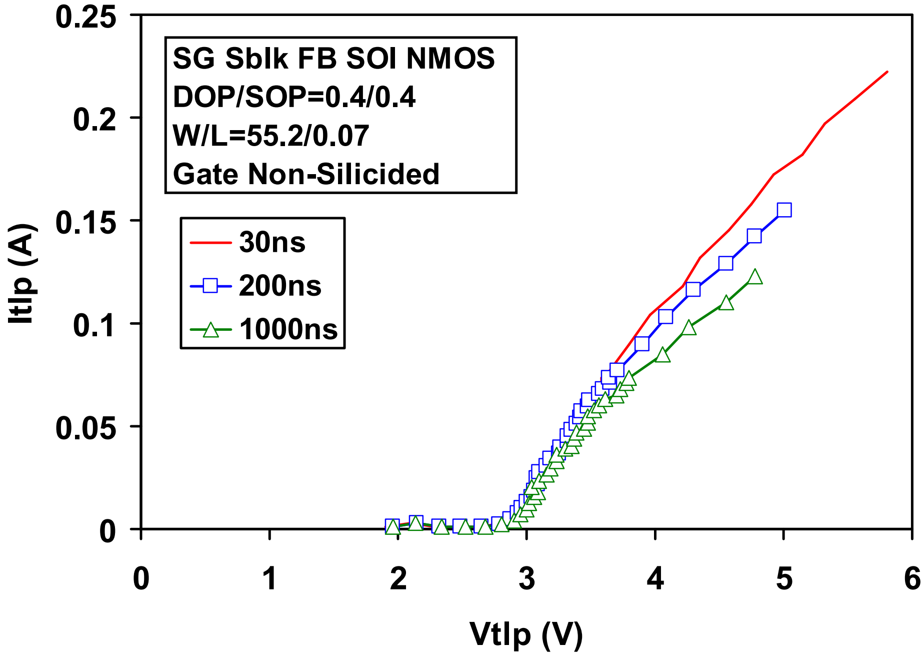

Figure 4-10: TLP I-V plots for thin-oxide (SG) floating body silicide-blocked (SBlk) SOI nMOSFETs obtained with different stress pulse widths.

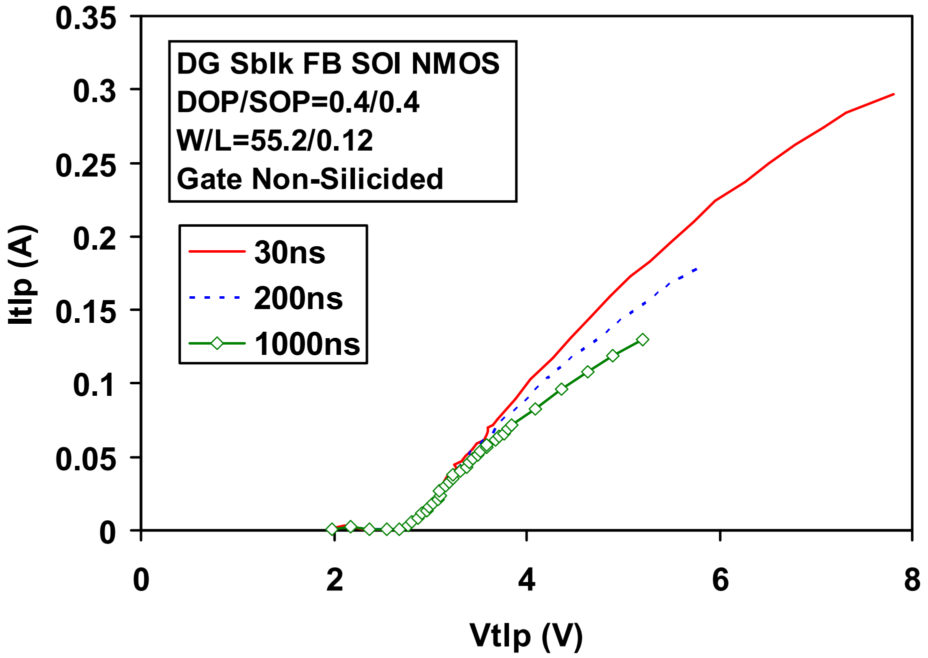

Figure 4-11: TLP I-V plots for thick-oxide (DG) floating body silicide-blocked (SBlk) SOI nMOSFETs obtained with different stress pulse widths.

4.1.3.3 Pf-tf analysis of GS and GNS MOSFETs

Next, the robustness of GS and GNS thick oxide (DG) floating body SOI nMOSFETs is examined throughout the EOS/ESD regimes by generating power-to-failure vs. time-to-failure curves. The figure 4-12 shows that the higher power dissipation occurs in GNS devices due to the higher current handling capability than similar sized GS device. In the figure, the experimental power-to-failure profiles for GS and GNS SOI nMOSFETs are compared with the analytical thermal model presented by Amerasekera et al [105] for the bulk MOSFETs.

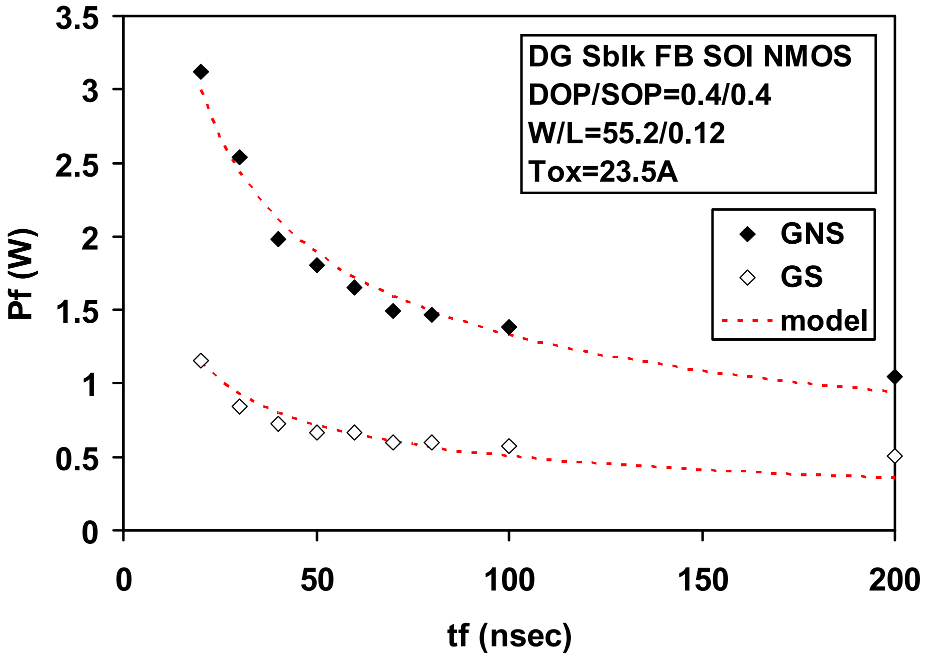

Figure 4-12: Experimental and theoretical power-to-failure (Pf) vs. time-to-failure (tf) profiles for thick-oxide (DG) floating body silicide-blocked (SBlk) SOI nMOSFETs with gate-silicided (GS) and gate-non-silicided (GNS) designs.

The modeling of device behavior at the onset of second breakdown (i.e. at Vt2 and It2) provides the limits of the operation of protection device. These models are based on the solutions to heat equation [106-109] considering the depletion region at the reverse bias drain-substrate junction as heat source as shown in Figure 4-13. The input power required to reach a given temperature is calculated as function of pulse applied is shown in Figure 4-14. The curve can be broken into four distinct regions each defined by the thermal diffusion time constant for that region as shown in the figure. Each region is approximated by a simple relationship. In the first region, the heating is adiabatic and described by P(t) α 1/t. In the second region, called Wunsch-Bell region [106], heating is described by P(t) α 1/√t. Region 3 together with region 2 describe the regions for ESD stress conditions. The region 4 is simply the d.c. or steady-state region, where the heat flow is a constant. The actual values of Pf-tf and the extents of each region are functions of both the device and the thermal boundary conditions. As we will see later in this section, the constants associated with these equations give information regarding the size, depth and location of heat spot during an ESD event. While applying these models to the experimental data, it should be kept in mind that these techniques require a prior knowledge of breakdown temperature [110].

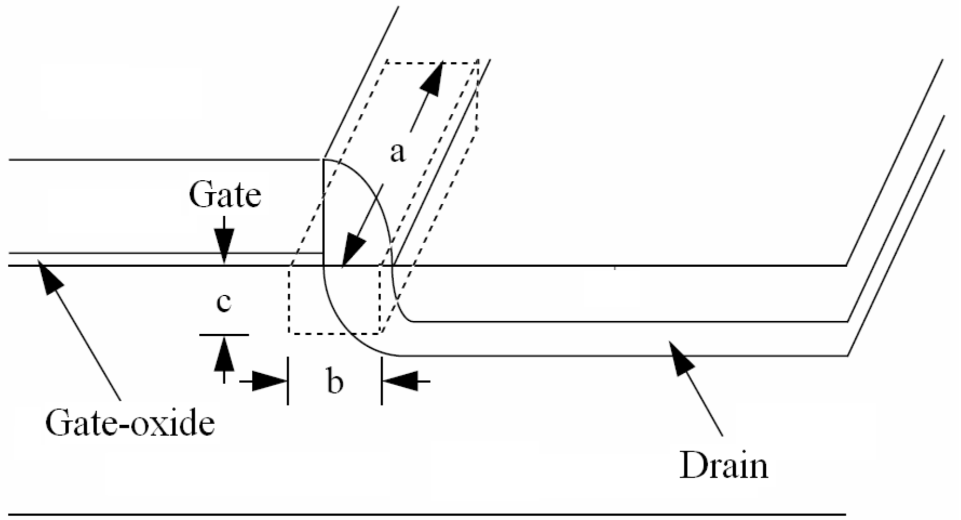

Figure 4-13: 3D thermal box region (dotted lines) of heat dissipation in MOSFET subjected to an ESD pulse at drain. The dimension 'a' is equal to the device width, 'b' is related to the gate length, and 'c' is approximately equal to the diffusion depth.

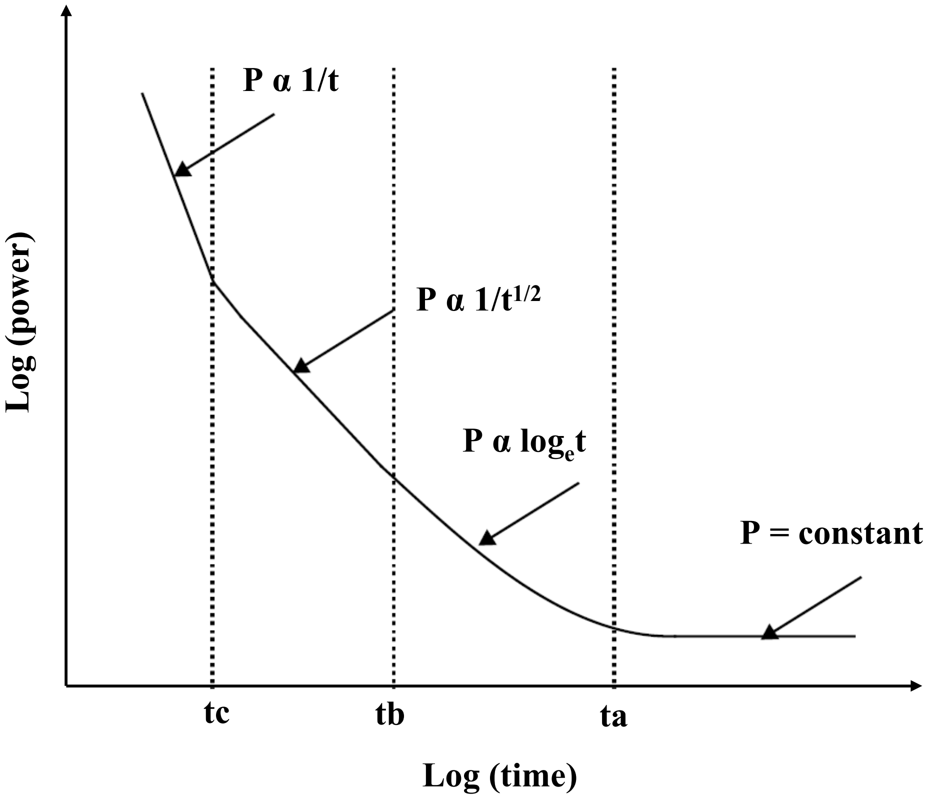

Figure 4-14: A qualitative schematic of input power-to-failure vs. time-to-failure predicted by an analytical thermal model [110].

In short, the model assumes (a) a rectangular-box region of device heating in the drain-side junction depletion region of a MOSFET, (b) constant temperature boundary conditions on all sides of the box (an infinite heat sink) and, (c) no heating outside the box. The length of the box, a, is equal to the width of the device, the dimension, b, is related to the gate length, and the depth, c, is approximately equal to the drain diffusion depth as shown in Figure 4-13.

The main problem with the infinite heat sink assumption is that the SiO_2 layer above the silicon is a thermal insulator and seriously degrades heat dissipation in the vertical direction. Moreover, in SOI devices the presence of buried oxide film aggravates the problem. Nevertheless, as seen from the Figure 4-13, surprisingly a good agreement between the experimental data and model is seen for both the designs. For a given temperature rise ΔT, the relationship between the input power P_f and the applied time t_f used to fit experimental data is given by:

$$P_f = \frac{ab\sqrt{\pi K \rho C_P}\,\Delta T}{\sqrt{t_f} - \sqrt{t_c}/2} \tag{4-1}$$

Where, a is equal to the width of device, b is related to gate length, $t_c = c^2/4\pi D$, c is approximately equal to drain diffusion depth, D, is thermal diffusivity ($K/\rho C_P$), K is thermal conductivity, C_P is the specific heat capacity at constant pressure, and ρ is the density of silicon.

The fitting parameters for GNS design are a=55.2μm, b=0.63μm, c=0.02μm and for GS design, a=55.2μm, b=0.24μm, c=0.02μm. Interestingly, in both the designs, the fitting parameter b which is along the channel length is greater than the channel length of the device (L=0.12μm). This indicates that the high temperature region during the breakdown is not only at the drain-substrate junction but extends into high resistive silicide blocked region under the DOP as shown in Figure 4-15.

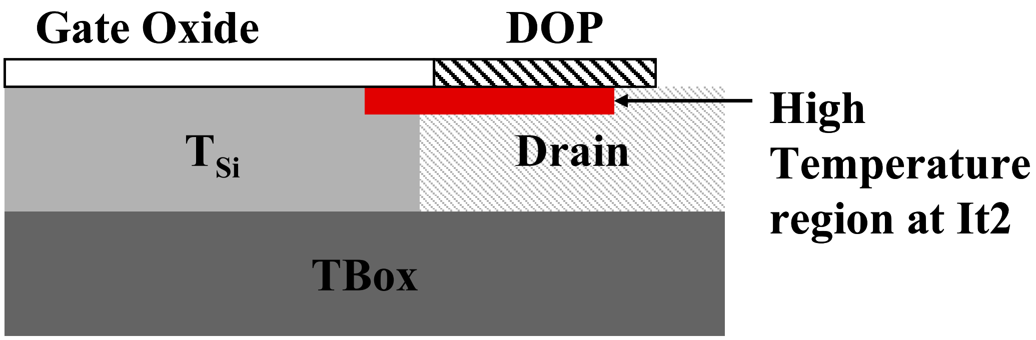

Figure 4-15: Drain-substrate junction side under an ESD pulse in SOI MOSFET. The thermal box region of heat dissipation extends from drain-substrate junction into the high resistive silicide blocked (SBlk) region under DOP.

4.2 HCI and NBTI behavior of SOI pMOSFETs and their interaction

4.2.1 Introduction to HCI and NBTI in SOI pMOSFETs

With the scaling of gate oxide thickness and channel length, pMOSFET hot carrier stress (HCS) induced degradation departs from the electron trapping mechanism, at low gate voltage Vg / high drain voltage Vd stress [77], to the hot-hole induced degradation, at Vg=Vd stress [78, 79]. For the sub-0.25µm pMOSFETs, it was concluded [78, 79] that the generation of interface states by hot-holes at Vg=Vd causes the most serious degradation. The situation is more complicated [83] for SOI devices as both the worst case stress (WCS) conditions and the interpretation of degradation are influenced by intricate interdependences of the stress bias level, floating body (FB) or grounded body (GB) operation, channel-coupling strength, and the self heating effect (SHE) and device operation temperature [111]. For SOI pMOSFETs under HCS it has been shown [84] that as the oxide thickness scales-down and the temperature increases (due to the SHE), negative bias temperature instability (NBTI) [10] is also activated, simultaneously with the hot carrier injection (HCI).

We will investigate NBTI induced degradation and its role on the HCS degradation of two families of partially depleted (PD) SOI pMOSFETs: core logic / high speed (HS) and input/output (I/O). It is found that, under NBTI stress with grounded body (GB) these devices degrade more than with floating body (FB). In general, concurrent NBTI-HC degradation was observed under HCS at Vg=Vd, except for I/O devices at high stress voltage where NBTI-like degradation dominated.

4.2.2 Device details

HS and I/O PD-SOI pMOSFETs were studied in this work based on high performance 65nm SOI CMOS technology [16]. Both devices that employed (H-gate) body contacts (BC) which could be independently biased and floating body (FB) devices without body contacts were available in each case. For HS devices power supply voltage Vdd=1.0V, gate oxide thickness tox=1.05 nm, channel width W=3μ, channel length L=0.06μ and for I/O devices Vdd=1.5V, tox=2.35 nm, W=3μ, L=0.12μ. Several HS devices were subjected to NBTI stress for a range of bias and temperature values, and several HS and I/O devices were subjected to HCS at Vg=Vd for a range of bias voltages. The stress was briefly interrupted to measure the device characteristics and the saturation threshold voltage VtSat in both the forward (FWD) and reverse (REV) mode (drain and source interchanged during measurement) to help probe the degradation mechanism. The saturation threshold voltage VtSat was defined as the gate voltage for which drain current equals 70 nA x (W/L) for drain voltage = Vdd.

4.2.2 NBTI behavior of thin and thick oxide devices

Figure 4-16 shows the shift of saturation threshold voltage (ΔVtSat) vs. temperature under different NBTI stress bias values for HS pMOSFET devices, where the body of the BC devices was grounded (GB operation) both during stress and during measurement. It is seen in this figure that the BC devices degrade more than the FB devices [112] for the higher stress bias and temperature values. This is due to the fact that for the FB devices, negative charge tunnels from the gate during stress and is being collected in the floating body, which effectively lowers the oxide field, thereby reducing NBTI. That the electric field is lowered in this case is supported by the fact that the (tunneling) gate current is lower in the FB device as shown in Figure 4-17.

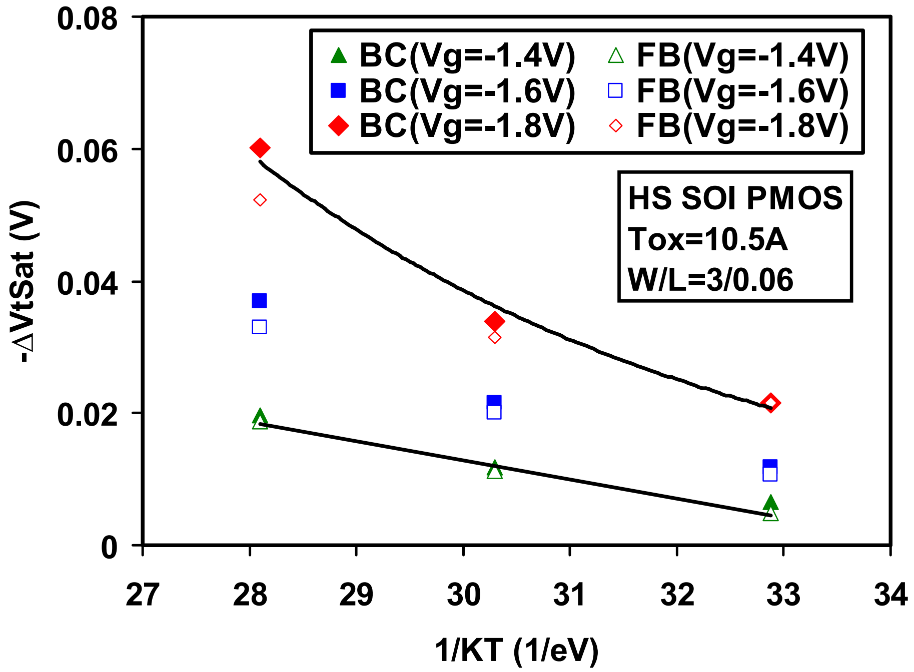

Figure 4-16: Saturation threshold voltage shift (ΔVtSat) vs. stress temperature for high-speed (HS) SOI pMOSFETs. Body contacted devices with grounded body (BC(GB)) show more degradation than the counterpart floating body (FB) devices as the stress bias and temperature value increase.

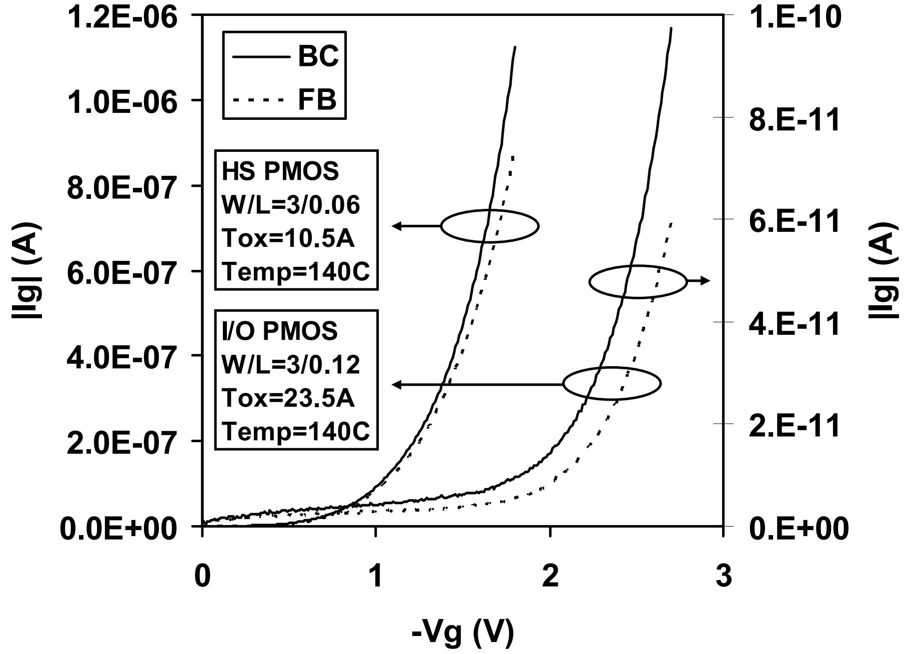

Figure 4-17: Gate current comparison of body contacted with grounded body BC(GB) and floating body (FB) devices for high-speed (HS) and input/output (I/O) SOI pMOSFETs vs. stress temperature. The gate current in FB device is smaller due to the accumulation of floating charge in the body, and the resulting electric field decrease.

During NBTI stress, holes and/or electrons can flow through the ultra-thin gate-oxide. Therefore, we also did carrier separation measurement to separate the hole and electron contributions from the total gate current [113-115]. In this measurement technique, gate voltage is varied from zero to negative value with all other terminals grounded. The current measurement though various terminals will reveal the kind of carrier flow during stress. Figure 4-18 shows the various possible scenarios of the type of carrier flow under a given stress. The channel current is due to the tunneling of hole from the Si substrate valence band, and the body current is due to the tunneling of electrons from the poly-Si gate valence band.

The carrier separation measurement was done at stress temperature (140^0C) by sweeping negative voltage at the gate and grounding all the terminals. As shown in the Figure 4-19, the channel current (Id+Is=Ids) equals the gate current (Ig). The body current (IBody) is much lower than either the Ids or Ig. This reveals that the main component of the gate current during stress are holes, which are injected from the Si substrate valence band into the gate-oxide.

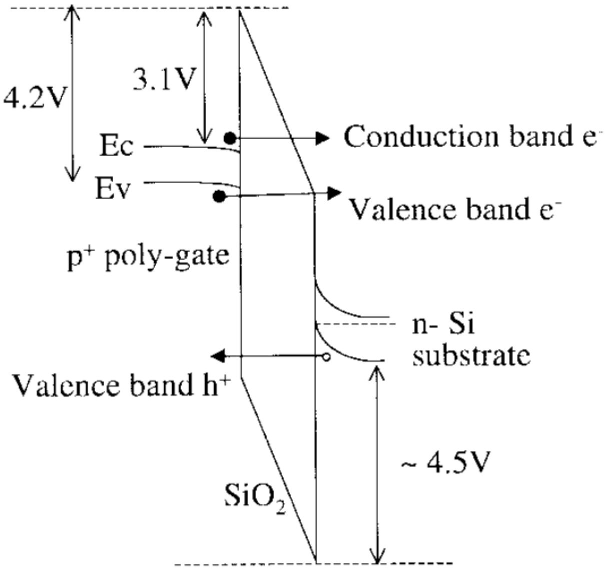

Figure 4-18: Three possible conduction processes in p+/pMOSFET: 1) valence band hole tunneling from the inverted Si substrate; 2) valence band electron tunneling from the p+ gate; and 3) conduction band electron tunneling from the p+ gate [113].

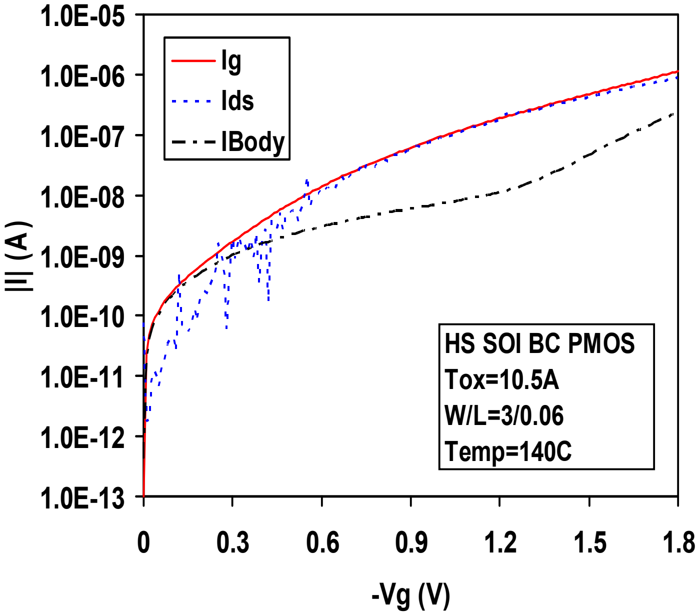

Figure 4-19: Carrier separation measurements performed on a pMOSFET under inversion conditions at 140^{0}C, showing the channel (Ids), gate (Ig) and body (IBody) currents through the gate-oxide as function of gate voltage (Vg). Since Ids equals Ig, the measurement reveals that holes are dominant during stress.

Figure 4-20 shows the NBTI degradation behavior for I/O devices stressed at Vg=-2.7V and temperature 140^{0}C. It is seen that the BC(GB) devices degrade more than the FB devices as was observed in thin-oxide devices. The higher degradation of body grounded device is also attributed to the lowered oxide field in the FB devices due to floating body charge, as demonstrated by the lower gate tunneling current in Figure 4-17.

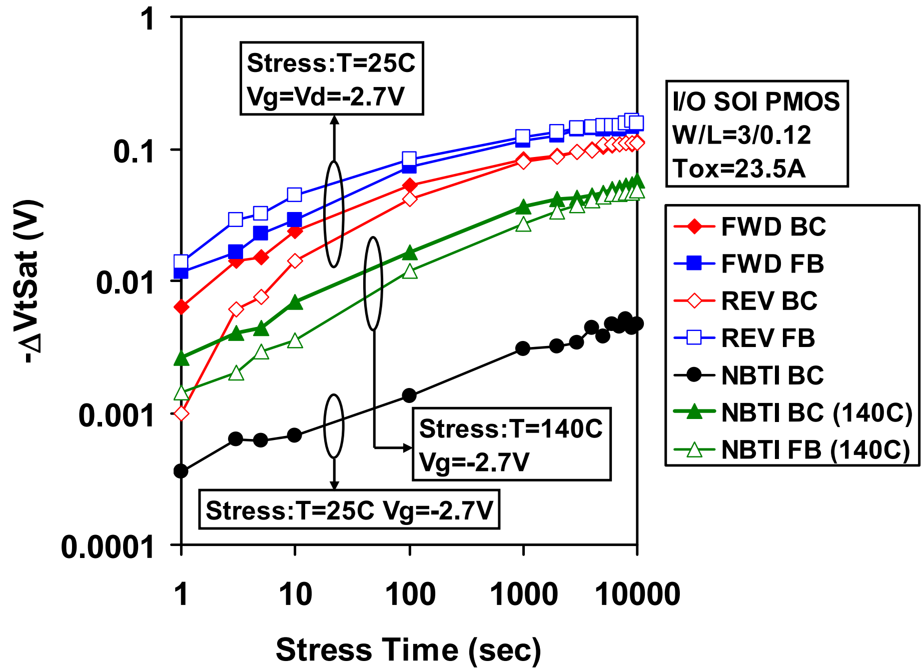

Figure 4-20: Saturation threshold voltage shift (ΔVtSat) vs. stress temperature for input/output (I/O) SOI pMOSFETs under HCS and NBTI stress. Forward (FWD) and reverse (REV) mode curves are on top of each other, demonstrating symmetric degradation along the channel under the present HCS condition. NBTI stress causes higher degradation in the body contacted with grounded body (BC(GB)) device than in the floating body (FB) device, whereas the FB device degrades more under HCS.

4.2.3 HCI behavior of thin and thick oxide devices

Figure 4-20 shows the ΔVtSat vs. stress time for both BC(GB) and FB I/O pMOSFETs under Vg=Vd=-2.7V HCI stress at room temperature. It is seen in this figure that for both the devices, the FWD and REV mode measurements are on top of each other at higher stress time. This demonstrates the symmetric degradation along the channel. This symmetric shift in VtSat reveals NBTI degradation dominance under the present HCS condition. For comparison, Figure 4-20 also shows degradation under NBTI stress at room temperature at Vg=-2.7V (all other terminals grounded). It is seen that degradation under Vg=Vd=-2.7V (HCI) is much higher than and parallels the degradation under Vg=-2.7V (NBTI) stress. This must mean that the self-heating, inherent to SOI devices when current flows, enhances NBTI degradation under HCS at Vg=Vd at room temperature. From Figure 4-20 it is seen that the FB device degrades more than the BC(GB) device under HCS. We believe that the higher degradation of FB devices under Vg=Vd=-2.7V stress must be due to the parasitic BJT (pBJT), which leads to higher current during stress, thus to higher self-heating and hence, higher NBTI activation. To verify this, the effect of externally applied body bias on the BC devices during stress was measured as shown in Figure 4-21. It is seen from this figure that the application of body bias (Vbody) enhances the degradation and with Vbody=-0.8V the degradation becomes similar to the FB device. This is due to the fact that the application of negative body bias in BC devices turns on the pBJT, which enhances the current and leads to higher self-heating and hence higher NBTI, just like in the FB devices.

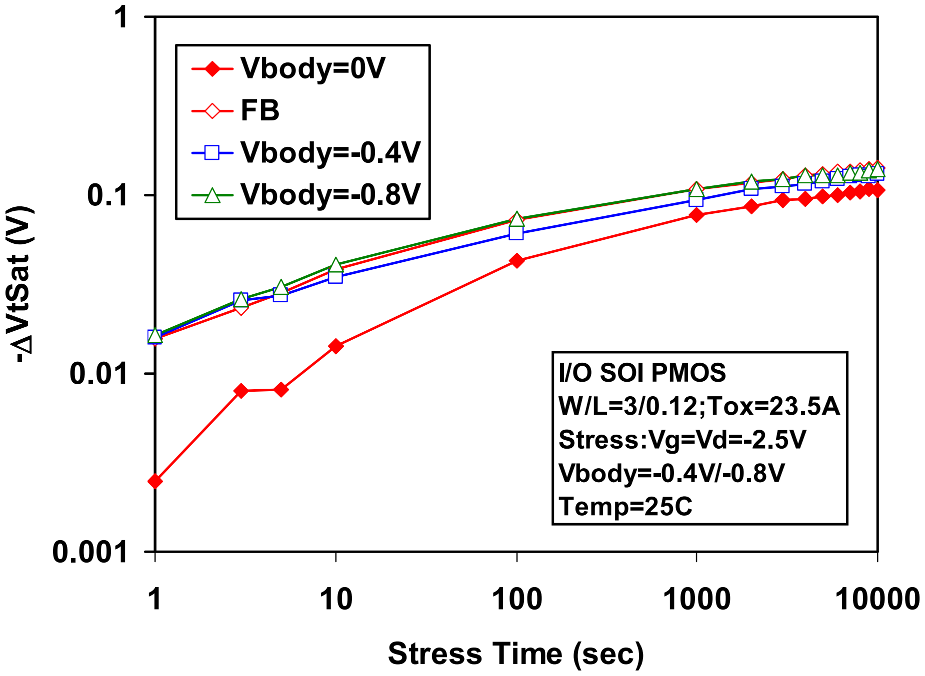

Figure 4-21: Saturation threshold voltage shift (ΔVtSat) vs. stress time for body contacted with grounded body (BC(GB)) input/output (I/O) SOI pMOSFETs for various body contact bias (Vbody) values during HCS. Increasing body bias increases the parasitic BJT current, leading to floating body like behavior and higher self-heating, and thus higher degradation than the grounded body device.

Figure 4-22 shows ΔVtSat for I/O devices following HCS at Vg=Vd over a stress bias range. It is observed that at higher stress voltages, the degradation is symmetric, and although there is an increasing difference between the FWD and REV ΔVtSat with decreasing stress voltage, NBTI plays a significant role over the entire bias range.

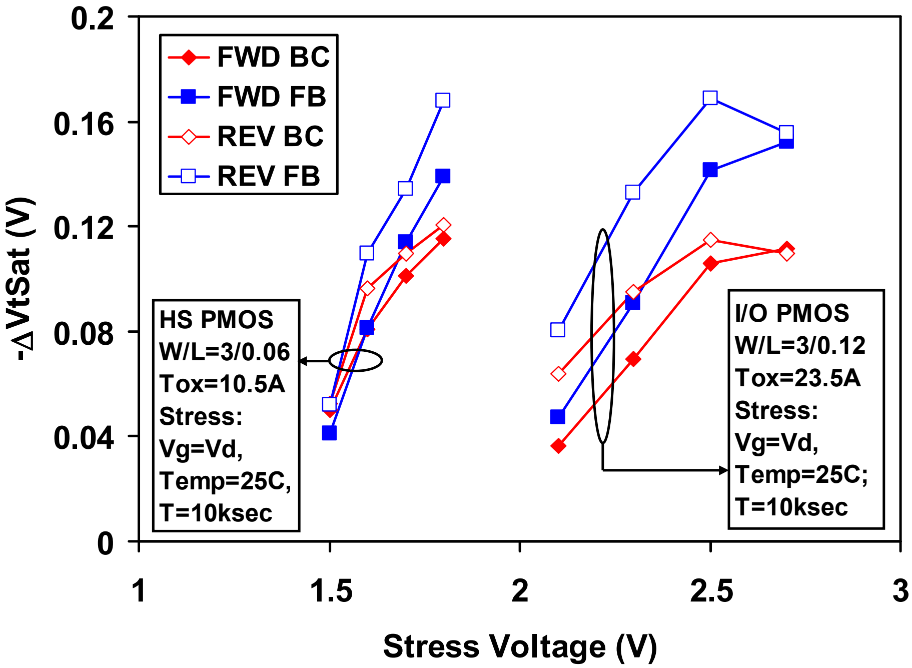

Figure 4-22: Saturation threshold voltage shift (ΔVtSat) vs. HCS stress voltage for high-speed (HS) and input/output (I/O) SOI pMOSFETs. For I/O devices the degradation is symmetric at higher stress voltages, but the difference between the forward (FWD) and reverse (REV) VtSat increases as the stress voltage decreases. In HS devices the degradation is asymmetric across the entire stress bias range.

Figure 4-23 shows ΔVtSat for HS devices following HCS at Vg=Vd=-1.8V as well as for NBTI stress (Vg=-1.8V). Similarly to I/O devices, due to self heating under Vg=Vd stress the degradation is higher than and it parallels the NBTI degradation. However here, the HCS degradation is not symmetric across the stress bias range, as in the case of the I/O devices (Figure 4-22). This demonstrates that although NBTI activates in HS devices under HCS as well, it is not as dominant as in the case of the I/O devices: in I/O devices most of the channel remains populated with holes during stress, which causes a NBTI like degradation near the source, and only a small part of the channel near the drain is degraded by hot carriers [98]. Figure 4-24 shows the effect of body bias in HS devices. It is seen that body bias does not seem to play an important role with Vbody=-0.4V. This body voltage may not be sufficient to turn on the pBJT effectively, and thus causes similar channel current as in the body grounded (Vbody=0V) device.

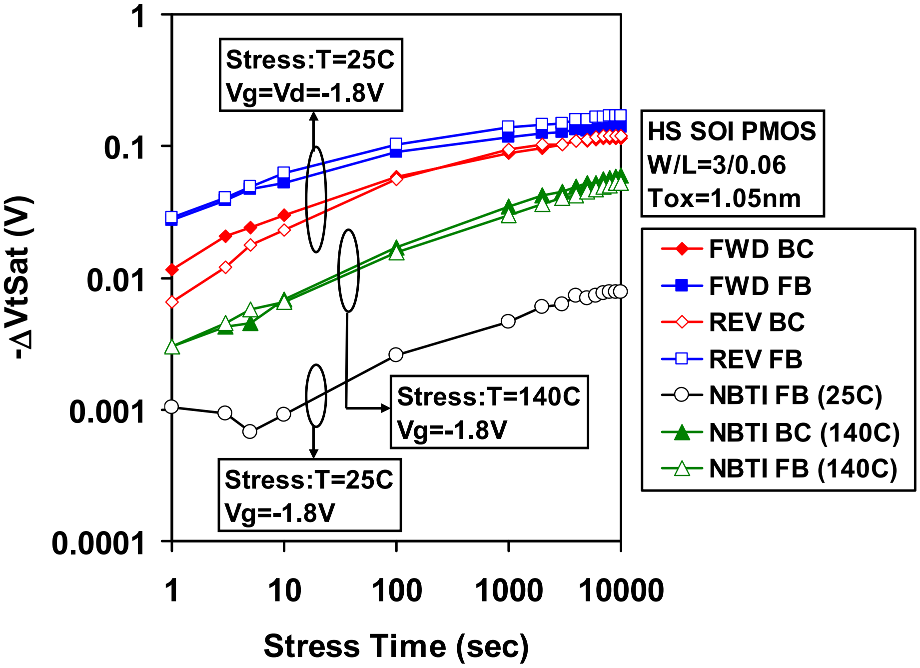

Figure 4-23: Saturation threshold voltage shift (ΔVtSat) vs. stress time for high-speed (HS) SOI pMOSFETs under HCS and NBTI stress. NBTI stress causes higher degradation in the body contacted with grounded body (BC(GB)) device than in the floating (FB) device, whereas the FB degrades more under HCS stress.

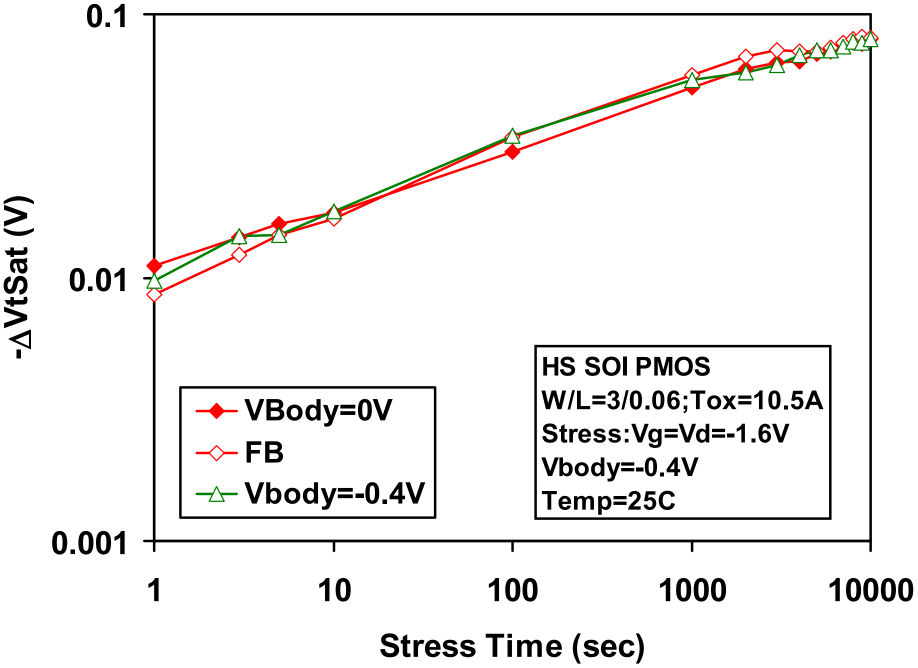

Figure 4-24: Saturation threshold voltage shift (ΔVtSat) vs. stress time for high-speed (HS) SOI pMOSFETs with body bias (Vbody).

4.3 Conclusion

A study on the electrostatic discharge (ESD) behaviors of silicide blocked (Sblk) n and p channel MOSFETs is presented for a state-of-the-art 65nm SOI technology. ESD characteristics of both thin and thick oxide MOSFETs were studied. Floating body charge in MOSFETs is shown to improve the ESD characteristics over a corresponding grounded body device. As observed, the grounded body SOI MOSFET holds almost no current and fails as soon as the device enters snapback. The ESD behavior of thin-oxide pMOSFET show failure current similar to the corresponding nMOSFET, but at the expense of higher power dissipation and higher parasitic bipolar (pBJT) turn-on voltage. The study of increasing either source or drain silicide blocking length shows higher on-resistance without significant improvement in the failure current. The effect of self-heating is observed for thick-oxide nMOSFETs with higher values of drain and/or source silicide blocking. The study of gate-silicided (GS) and gate-non-silicided (GNS) nMOSFETs show that the GNS devices have higher failure current. In particular, GNS devices exhibit approximately 70% higher failure current than the similar sized GS devices. GNS devices are shown to suffer more from self-heating effects than the similar sized GS devices as revealed from TLP measurements with different stress pulse widths. The analytical thermal model for bulk devices when applied to SOI devices indicates that the high temperature region during the breakdown is not only at the drain-substrate junction but extends into the highly resistive silicide blocked region under drain.

The analysis of grounded body 65 nm SOI pMOSFETs show higher NBTI degradation than floating body devices due to the lowering of the oxide field in the floating body devices caused by gate tunnel current. Both grounded body and floating body devices show worst case degradation under stress at Vg=Vd, caused by concurrent HCI and NBTI, with NBTI increasingly dominating with increasing bias due to self heating and for increasing channel length.

5. Conclusion and future work

5.1 Concluding remarks for the dissertation

In this dissertation, we have studied the device reliability mechanisms and their interactions in nano-scale MOSFETs. The study focused on understanding the major reliability concerns electrostatic discharge (ESD), negative bias temperature instability (NBTI), hot carrier injection (HCI), and their interactions in both bulk and SOI MOSFETs. The main findings of this dissertation can be summarized as follows:

(a) The dissertation begins with ESD study of bulk pMOSFETs and the effect of various design parameters such as gate length, gate oxide thickness on the ESD robustness of device. We showed with leakage current measurement and device simulations the competitive role of power dissipation volume, location of parasitic bipolar transistor (pBJT), and the gain of pBJT in determining the ESD robustness with technology scaling. It is also found that the thin and thick oxide devices exhibit different degradation/failure behavior with respect to channel length. Thick-oxide devices fail due to classical source-drain filamentation whereas in thin-oxide devices both the drain-source filamentation and oxide breakdown was observed.

(b) The NBTI behavior as a function of channel length and the interaction between ESD and NBTI was studied next. The study showed that thick oxide devices when NBTI pre-stressed exhibit high ESD snapback on-resistance. Similarly, the NBTI characteristics of the thin-oxide device degrade more when the device is pre-stressed with non-destructive ESD pulses.

(c) The HCI and NBTI on pMOSFETs was studied as a function of channel length with various stress bias condition at both room and high temperatures. The results reveal the increasing influence of NBTI like degradation under hot carrier stress (HCS) condition at high temperature.

(d) The dissertation then examines the ESD robustness of SOI MOSFETs and highlights the difference between SOI and bulk devices in terms of their ESD capability. Floating body charge in MOSFETs is shown to improve the ESD characteristics over a corresponding grounded body device. As observed, the grounded body SOI MOSFET holds almost no current and fails as soon as the device enters snapback. The ESD behavior of silicide-blocked (SBlk) n and p channel MOSFETs was then explored for various design (channel length and gate-oxide thickness) and layout parameters (gate-silicided and gate-non-silicided). The study of gate-silicided (GS) and gate-non-silicided (GNS) nMOSFETs show that the GNS devices have higher failure current. In particular, GNS devices exhibit approximately 70% higher failure current than the similar sized GS devices. GNS devices are also shown to suffer more from self-heating effects than the similar sized GS devices as revealed from TLP measurements with different stress pulse widths.

(e) Finally, the dissertation provides a comprehensive study on the NBTI and HCI behavior of core logic/high speed (thin-oxide) and Input/Output (thick-oxide) SOI p-channel MOSFETs. The effect of floating body, device temperature, and gate tunneling current on NBTI and HCI performance have been explored. It is found that grounded body pMOSFETs show higher NBTI degradation than floating body devices due to the lowering of the oxide field in the floating body devices caused by gate tunnel current. Both grounded body and floating body devices show worst case degradation under stress at Vg=Vd, caused by concurrent HCI and NBTI, with NBTI increasingly dominating with increasing bias due to self heating and for increasing channel length.

5.2 Suggestions for future work

The advances in device technology and scaling will create new concerns such as gate-oxide reliability under ESD stress, bias temperature instability (positive and/or negative), and hot carrier degradation for High-K dielectrics, and interaction among ESD, NBTI and HCI. The most important task would be the modeling of these mechanisms, as towards the end of the research cycle the device behavior degradation needs to be incorporated into circuit simulators. This would require a deep understanding of how aforementioned mechanisms degrade the device behavior. The modeling for future technologies is expected to get complicated due to the increase in gate tunneling current and junction leakage current. The tunneling and leakage current would especially be a problem for SOI based devices as these mechanisms would charge the body and change the electrostatics of the device. Additionally, the tunneling and junction leakage current would also require to devise new characterization techniques to examine the nature of damage generated. To model these mechanisms carefully and to predict the lifetime reliably it will first be necessary to understand the effects of temperature, stress bias and/or electric field, floating body charge, self-heating, recovery etc. on the behavior of these reliability mechanisms. The work done during this dissertation enhances the understanding of basic reliability mechanisms in these new technologies based on new devices, processes, and material engineering.

In case of ESD protection, as is known, the discharging speed of charge device model (CDM) event is much faster than the human body model (HBM) and machine model (MM) events. The typical current peak of CDM event is ~15A with a rise time of only ~200ps. The turn-on speed of ESD protection device will be a key issue for the future technologies with the ultra-thin gate-oxide in I/O devices. Such a fast discharging event can easily cause damage to the gate-oxide (either catastrophic or latent) of the I/O devices before the ESD protection device gets a chance to turn-on. Thus, there will be two issues regarding the CDM protection in future technologies:

(1) The turn-on speed of the ESD clamp device: It would be necessary for the designer to ensure that the ESD protection element turns-on before the voltage at which the protection node exceeds the gate breakdown voltage of the device to be protected, and

(2) More importantly, examine the effect of non-catastrophic CDM events on the gate-oxide reliability of the I/O devices.

Based on the above statements, few possible predictions regarding reliability of devices in I/O circuit can be made:

(a) The non-destructive CDM pulse at the gate can deteriorate the nominal behavior of the device eg. change in the on/off current, transconductance etc. which are especially worrisome for the analog technologies.

(b) The nature of the damage created by CDM pulse eg. interface states, oxide charges, increase in stress induced leakage current (SILC) etc. at gate-oxide needs to be identified carefully. The damage generated during ESD protection would play a significant role in determining the nature of subsequently occurring reliability mechanisms such as NBTI/HCI during normal circuit operation.

(c) This effect of one reliability mechanism on another needs to be looked in the reverse direction also i.e. how the degradation induced by NBTI/HCI during the normal circuit operation weakens the oxide and hence, plays a role during the subsequent ESD pulses.

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CURRICULUM VITAE

Rahul Mishra was born on 5th Dec1979 in Indore, M.P., India. He received his Bachelor of Engineering from Shri Vaishnav Institute of Science, Indore in 2001 in Electronics and Master of Science (Engg.) from Indian Institute of Science, Bangalore in 2004 in Instrumentation. While at George Mason University, he was doing research in the areas of ESD, NBTI and HCI reliability and their interactions in nano-scale CMOS technology. During the summer and fall 2006 he worked at IBM Microelectronics on a student internship in ESD/Latchup Development Group. In summer 2007 he went again to IBM Microelectronics on a student internship in TCAD Technology Enablement group.