

PERFORMANCE OF DEVICES MADE OF LARGE BAND-GAP
SEMICONDUCTORS, SIC AND GAN

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DEDICATION

This is dedicated to my loving girlfriend Akiko Nakazawa, who have supported for her understanding and constant support during my study years.

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ABSTRACT

PERFORMANCE OF DEVICES MADE OF LARGE BAND-GAP SEMICONDUCTORS, SIC AND GAN

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Silicon (Si) and gallium arsenide (GaAs) devices have limitations for certain applications such as high-power and/or high-frequency due to their material properties. As a partial fulfillment of the requirements for the degree of doctor of philosophy in electrical and computer engineering, devices made using two promising substrate materials: silicon carbide (SiC) and gallium nitride (GaN) were studied for high-power and high-frequency applications, respectively.

The SiC is considered as a suitable material for high-power devices such as double-implanted metal-oxide-semiconductor field-effect-transistor (DMOSFET), in which the current flows vertically to the substrate contact. The DMOSFET consists of several hundred cells connected in parallel, making it possible to sustain both high blocking voltage and high current. GaN grown on SiC is considered as a suitable material for high-frequency and high-power applications. High electron mobility transistor

(HEMT) fabricated with GaN and aluminum gallium nitride (AlGaN) utilizes a conduction band offset and piezoelectric polarization effect at the junction between these two materials to produce a highly conductive channel.

However, in spite of their promises, the performance of both SiC DMOSFET and GaN HEMT devices, with respect to their Si and GaAs counterparts are not well understood. In this work, first the SiC DMOSFET devices were characterized for their threshold voltage, drain current and breakdown voltage stability and then GaN devices for their efficiency and linearity performance at high-frequency. The results of SiC DMOSFETs were fitted with simulation to determine the location of the interface charge responsible for instability in device behavior. The charge at the inner region of the junction termination extension has the most pronounced effect on the breakdown voltage instability. The interlayer dielectric (ILD) composition that can minimize the SiC DMOSFET instability problem is also determined considering several limitations on the maximum weight percentages of the boron and phosphorous constituent dopants in the boro-phospho-silicate glass (BPSG) ILD layer. The BPSG with a composition of 2.4 weight percent B and 5 weight percent P is projected as optimum for the processing conditions used for making the SiC DMOSFET of this study. Results of GaN HEMTs were compared with those of GaAs pseudomorphic HEMTs.

1. Introduction

1.1. Properties of SiC and GaN

Silicon (Si) and gallium arsenide (GaAs) technologies are well matured and are widely available, but have limitations for certain applications such as high-power and high-frequency, especially in harsh environment (high-temperature). The Si loses its semiconducting property at 175 °C due to a small band-gap energy of 1.1 eV. The need for high temperature operation of devices is critical not simply for elevated ambient temperature operation, but also from reliability considerations at high power.

Silicon carbide (SiC) and gallium nitride (GaN) are wide band-gap semiconductors. The wide band-gap property of the material has consequences on transistor behavior. First, it leads to a high breakdown field, meaning devices based on wide band-gap semiconductors can withstand large voltages. Next, devices made from wide band-gap materials can be operated at much higher temperatures. The wider the band-gap, the higher the critical temperature, at which the onset of intrinsic conduction deteriorates the device performance. Material properties for SiC and GaN along with Si and GaAs are given in Table 1.1.

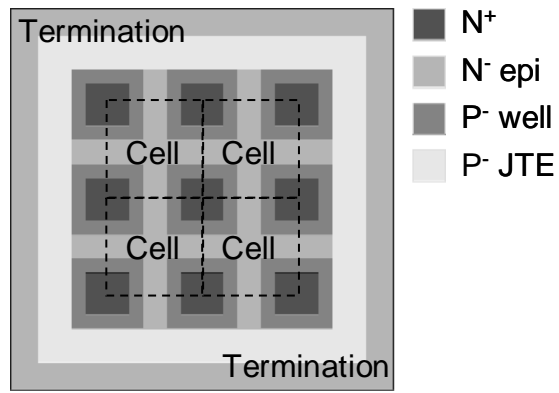
The SiC material has become the basis of high-power solid-state devices [1-3] due to its properties such as: a high breakdown field of 3 MV/cm, which is approximately five times larger than that of Si; an excellent thermal conductivity of 4.9 W/cm-K, which

Table 1.1: Major semiconductor materials and their attributes

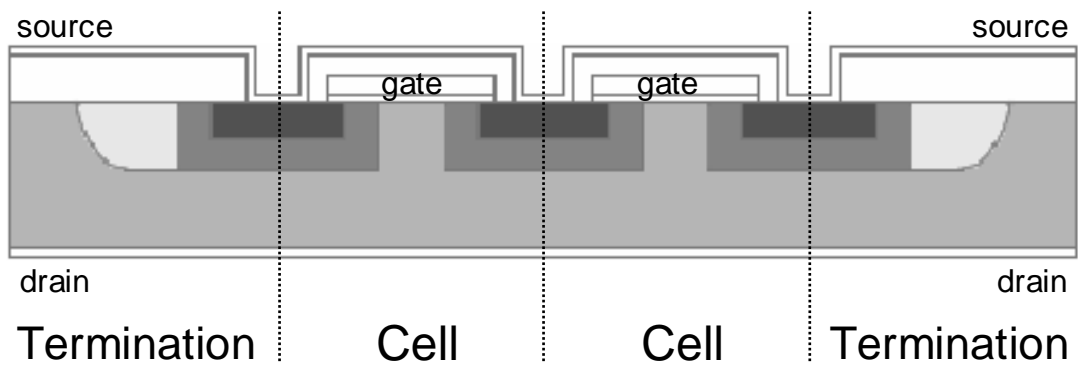
	Si	GaAs	4H-SiC	GaN
Band-gap Energy (eV)	1.1	1.4	3.2	3.4
Breakdown E-Field (V/cm)	6.0×10^5	6.5×10^5	3.0×10^6	3.0×10^6
Saturation Velocity (cm/s)	1.0×10^7	2.0×10^7	2.0×10^7	2.7×10^7
Thermal Conductivity (W/cm-K)	1.5	0.5	4.9	1.7

is better than copper at room temperature; a high saturated drift velocity; a high thermal stability; and chemical inertness. A high-power device is used for conducting high currents in the conducting mode and for blocking high voltages amounting to several kilovolts in the blocking mode. The simplest type of power device is a rectifier, which conducts in the forward direction and blocks voltages in the reverse direction. It is considerably more interesting to have a switching device with externally controlled conduction/blocking modes. An example of such a device is metal-oxide-semiconductor field-effect transistor (MOSFET), whose conductivity is controlled by the gate terminal. A lightly-doped layer will provide a large depletion layer width. In the case of SiC, the breakdown electric field strength is more than an order of magnitude higher than for Si. This means that for devices having similar blocking voltage capabilities, the doping level must be approximately two orders of magnitude lower in the Si device compared to the SiC device, in order to increase the depletion width. The thickness of the active base region over which the electric field gradients manifest must, thus, be made approximately 10 times thicker for a Si device when compared to a SiC device. A Si device with rectifying capabilities up to 5 kV would require a depletion width of approximately 350 μm and a doping level of approximately $2.5 \times 10^{13} \text{ cm}^{-3}$. Such a low doping level is very difficult to achieve. The same rectifier in SiC only needs a 25 μm thick active base layer with a doping level around $8 \times 10^{15} \text{ cm}^{-3}$. The layer thicknesses and doping levels required for high voltage SiC power devices can be easily obtained by epitaxially grown layers.

The GaN material has become the basis of an advanced microwave power device technology due to: a high breakdown field of 3 MV/cm, which is approximately five times larger than that of GaAs; a high peak electron velocity of 2.7×10^7 cm/s; and the capacity of this material system for supporting a hetero-structure device technology with a high two-dimensional electron gas (2-DEG) density and electron mobility. The high breakdown field in this material provides excellent high-power performance and the properties like high carrier velocity, high carrier density, and high carrier mobility offer excellent microwave performance making this material highly suitable for making high-power microwave devices. Another attractive feature of gallium nitride is the possible polarization induced bulk three-dimensional doping without physically introducing shallow donors. The strong piezoelectric effect and a large spontaneous polarization in gallium nitride allow one to incorporate a large electric field ($> 10^6$ V/cm) and a high sheet charge density ($> 10^{13}$ cm⁻²) without doping, which helps one to realize devices for a variety of high-frequency applications. Although, the thermal conductivity of GaN isn't great for high-power and high-temperature applications, GaN device can overcome the problem by fabricating it onto a SiC substrate, whose thermal conductivity is excellent. This can be possible because SiC is closely lattice matched to GaN, and also has a thermal expansion coefficient close to that of GaN. For these reasons, the gallium nitride grown on SiC substrates is a promising material for high-power and high-temperature solid-state devices, especially for those intended for microwave frequency range and also for high-temperature electronics.



(a)



(b)

Figure 1.1: (a) Top and (b) cross sectional views of simplified DMOSFET device

1.2. Why SiC DMOSFETs?

Double-implanted metal-oxide-semiconductor field-effect-transistors (DMOSFETs), made of 4H-SiC, are attractive for high-power switching application [1-3]. The structure of DMOSFET is vertical and not planar, and a DMOSFET is constituted of several hundred cells, making it possible to sustain both high blocking voltage and high current. Top and crosssectional views of a simplified DMOSFET structure constituting of 4 square cells are drawn in Figures 1.1(a) and 1.1(b), respectively. All MOSFET operations are taken place within cell structures of the DMOSFET. A termination structure, located along cell region perimeter, is intended to prevent premature breakdown due to electric field crowding at the periphery of the cell region. In a lateral structure, the current and breakdown voltage ratings are both functions of the channel width and length, resulting in inefficient use of the wafer real estate area. In a vertical structure, the n⁻-epitaxial layer thickness is chosen proportional to the required breakdown voltage. Also, by having a drain terminal on the back side of the wafer, several hundred cells (transistors) can be easily interconnected in parallel to sustain a large amount of current. The DMOSFETs have been fabricated using Si; however, 10 kV is the expected maximum limit on the blocking voltage of Si-based DMOSFETs, whereas, the SiC-based DMOSFET is expected to operate up to 50 kV.

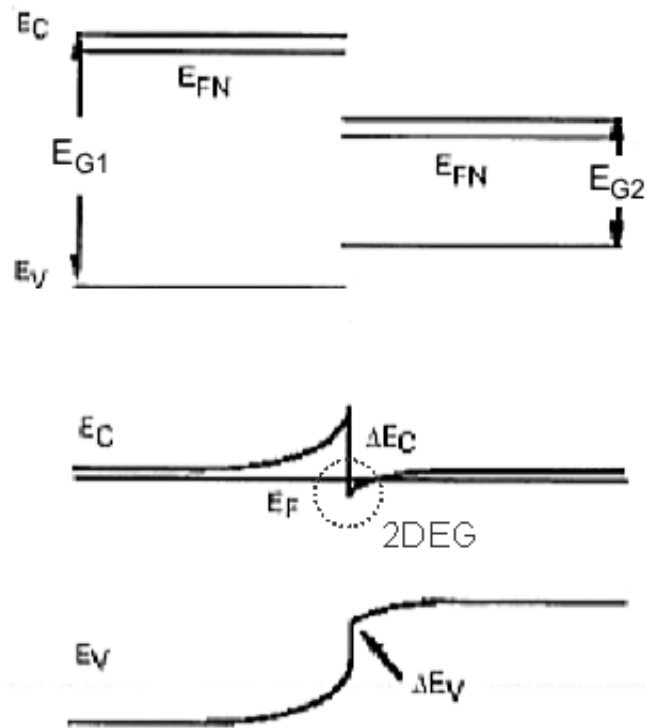
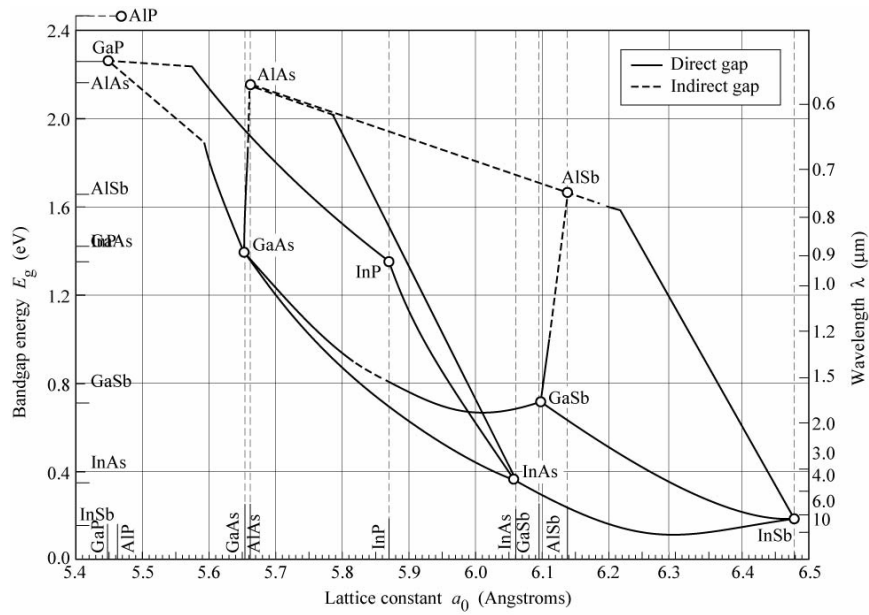
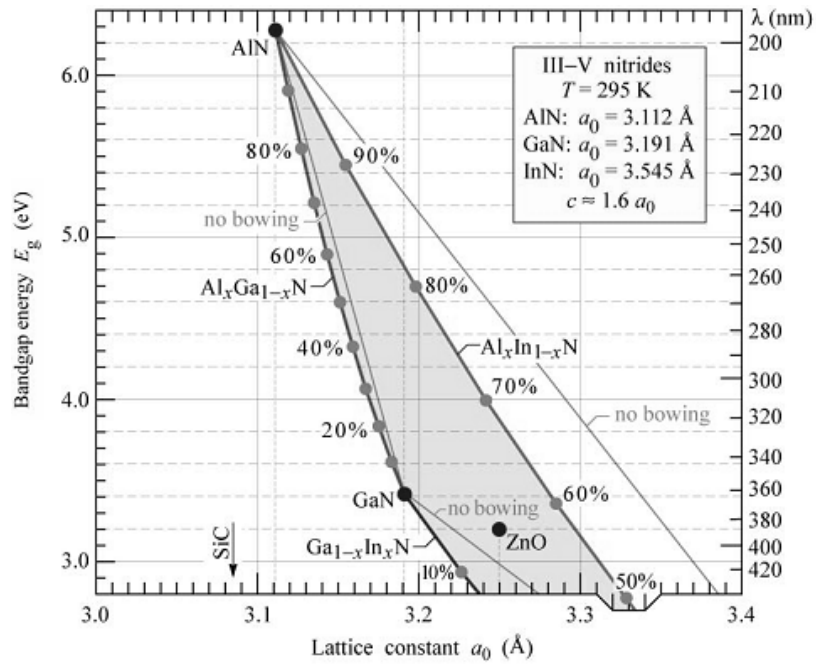


Figure 1.2: Heterojunction created when two semiconductors with different band-gap energies (E_{G1} and E_{G2}) are brought into physical contact

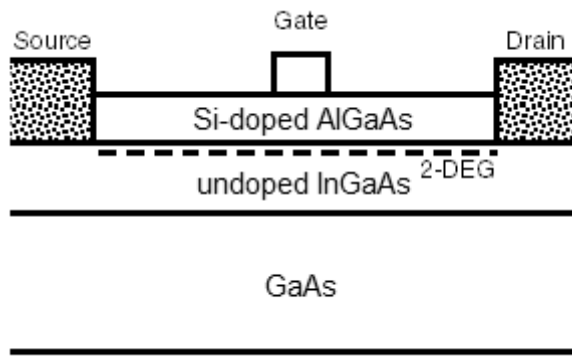


(a)

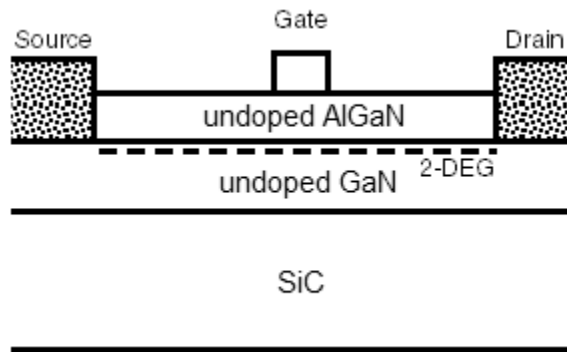


(b)

Figure 1.3: Band-gap energy versus lattice constant at room temperature of (a) various III-V semiconductors, not including nitrides, and (b) III- nitride semiconductors (adopted from Ref. [4])



(a)



(b)

Figure 1.4: Typical device structures of (a) GaAs pHEMT and (b) GaN HEMT

1.3. Why GaN HEMTs?

High electron mobility transistors (HEMTs) fabricated with III-V compound semiconductors, utilize a junction between two materials with different band gap (i.e. a heterojunction) to obtain a highly conductive channel in the smaller band-gap material without a loss of carrier mobility due to ionized impurity scattering. The effect of this heterojunction is to create a very thin conductive layer (popularly known as two-dimensional electron gas, 2-DEG) where the Fermi energy is above the conduction band, giving the channel very low resistance (see Fig. 1.2). Most III-V compounds are completely miscible in ternary crystals. In other words: from the two compounds GaN and AlN one can make ternary $\text{GaAl}_{1-x}\text{N}_x$ for $0 < x < 1$. Band-gap energy versus lattice constant for III-V compound semiconductors are shown in Figures 1.3(a) and 1.3(b) [4]. By examining Fig. 1.3(b), it can be figured out that the GaN and the AlN have almost the same lattice constant. Hence, one can combine these two binary materials to obtain any ternary composition without encountering lattice strain to either GaN or AlN. Important polytypes of SiC, such as 4H-SiC and 6H-SiC, unfortunately, do not have the zinc-blende type lattice, which is common to most of the III-Vs in the diagrams but have a hexagonal unit cell. Therefore, SiC does not easily mix with the other elemental or compound semiconductors, and hence, ternary system does not exist for SiC and the HEMT structure can not be realized.

At present, GaAs pseudomorphic HEMTs (pHEMTs) are widely used for microwave power applications [5-10]. A structure of GaAs pHEMT is drawn in Fig. 1.4(a). 2-DEG mobility of GaAs device has been improved by using a thin layer of

InGaAs. Such device is called pseudomorphic, because GaAs device is no longer constructed only with ternary of aluminum (Al), gallium (Ga), and arsenic (As), but also with indium (In). The GaAs pHEMTs are not operated in high-power Class A bias mode because of an excessive thermal dissipation at high Class A current levels. This may lead to the destruction of the device due to the GaAs substrate's poor thermal conductivity. As standard GaAs pHEMTs approach their theoretical power limits [11], new device technologies capable of high-voltage and high-power operation are required [12-15]. The GaN based HEMT devices made on SiC substrates have the potential to replace GaAs-based transistors for a number of high-power applications at high-frequencies, due to a high saturation velocity (2.7×10^7 cm/s vs. 1×10^7 cm/s) and a high breakdown voltage (3 MV/cm vs. 0.4 MV/cm) of GaN and a high thermal conductivity (4.9 W/cm-K vs. 0.5 W/cm-K) of the SiC substrate [16-18]. A structure of GaN HEMT is drawn in Fig. 1.4(b). In GaN HEMTs, a second effect contributes to the formation of the highly conductive channel. Both AlGaN and GaN are pyroelectric semiconductors showing strong spontaneous polarization, with the polarization in AlGaN being larger than in GaN [19]. Furthermore, AlGaN has a slightly smaller lattice constant than GaN, thus the AlGaN layer is under tensile strain. The strain causes an additional polarization component, which is called piezoelectric polarization. The combination of spontaneous and piezoelectric polarizations results in a large positive interface sheet charge at the heterojunction. Electrons tend to compensate this interface charge and consequently build up a 2-DEG in the GaN layer adjacent to the heterointerface [20].

1.4. What is done in this study

For high-power applications, SiC DMOSFETs were investigated, in terms of threshold voltage (V_{TH}) and breakdown voltage (BV) drifts as a result of bias and temperature stress. Stability of V_{TH} and BV of any transistor, which is intended for switching application, is important when the transistor is biased in on- and off-state, respectively.

The V_{TH} instability of SiC DMOSFETs was assessed by measuring V_{TH} before and after different gate bias stress durations of range 100 s – 5,500s. Since SiC DMOSFET's turn-on drain current (I_{DS}) increase with increasing gate-source voltage (V_{GS}) is rather gradual, unlike in Si MOSFET's, there isn't a widely accepted threshold voltage (V_{TH}) definition available for SiC DMOSFETs. Thus, in this work, based on the $i_{DS} - v_{GS}$ transfer characteristics obtained at $V_{DS} = 0.1$ V, the V_{TH} is defined in three ways (described later). In addition to studying the threshold voltage drift using the defined V_{TH} in three ways, the drain current transients during the stressing period at both room-temperature and elevated temperatures were also studied to see if monitoring of the drain current transient during stressing can be used to study on-state instability of SiC DMOSFETs.

The BV instability of SiC DMOSFETs was assessed by measuring BV before and after a fixed bias stress duration at room temperature or at a high temperature. A slump in BV was observed when the DMOSFET was bias stressed at a voltage less than the BV and at a high temperature, for a period of time. A dynamic recovery of the slumped BV to the pre-stress value during post-stress period was also observed. In order to quantify these

effects, the measurements were also performed on the devices with different design dimensions to determine if device dimensions and drifts in the breakdown voltage are related. In addition, electric field and voltage contours, and breakdown voltage simulations have been performed for different SiC/SiO₂ interface charge densities to study the mechanisms responsible for the BV instability of SiC DMOSFETs.

Possible causes for V_{TH} and BV instability of SiC DMOSFETs were sought, and a solution to suppress the V_{TH} and BV instability of DMOSFETs is suggested, by investigation of interlayer dielectric (ILD) of DMOSFETs, which were tested in this work for the V_{TH} and BV instability. The ILD films are widely used in semiconductor integrated circuit technologies to separate metal interconnect lines. The ILD film is also used in the DMOSFET discrete devices to separate gate and source metal contacts. Desirable characteristic of the ILD films, in addition to the ability to suppress the V_{TH} and BV instability of SiC DMOSFETs, is a gradually tapered step coverage over the patterned gate metal to ensure the continuous coverage of subsequently formed source metal contact over the stepped ILD. The X-ray photoelectron spectroscopy (XPS) was used to find the material composition of ILD, and the scanning electron microscopy (SEM) was used to analyze the step coverage of the ILD. Literature on materials and flow processes for the high quality ILD, mainly developed during 1980s for Si, is researched and improved materials and flow processes for ILD of SiC DMOSFETs are suggested.

For high-frequency applications, GaN HEMTs were investigated. For high-frequency application such as multi-tone and digital telecommunication systems, in addition to requirements for high efficiency, there is also an increasing demand for high

linearity [14, 21-23]. Thus, in this work the output power, efficiency, and linearity performance of GaN HEMTs were compared with state-of-the-art GaAs pHEMTs fabricated with a well matured GaAs technology. Input and output impedance matching techniques for obtaining high efficiency and linearity are fully developed for both GaN and GaAs devices. Efficiency and linearity trade-offs are studied for both GaN and GaAs devices under different biasing (Class A, AB and B) and impedance matching conditions (output power, efficiency, and linearity match). To the best of authors' knowledge, this work is the first comprehensive study where the efficiency and linearity performances of GaN HEMTs are directly compared with optimal GaAs pHEMT devices under similar measurement conditions.

2. Instability in the characteristic of 4H-SiC DMOSFETs

2.1. Introduction

Though, SiC DMOSFETs are beginning to be commercialized [24], there are still a number of issues that need to be solved to improve the performance of SiC DMOSFETs. The issues, attributed to the high density of SiC/SiO₂ interface traps and near-interface traps [25, 26], are a low inversion-channel mobility, a negative threshold voltage, and a threshold-voltage instability. The interface traps are negatively-charged, and numerous papers have addressed the effect of the interface traps on low inversion channel carrier mobility [27]. The interface traps also contribute to a shift in the threshold voltage. The near-interface traps are positively-charged, and thus the threshold voltage of some SiC MOSFETs is negative. These near-interface traps presumably lie in the oxide transition region that extends several nm into the oxide from the SiC interface, caused perhaps by the presence of C [28] and strained SiO₂ [29]. The rough balance between negatively charged interface traps and positively charged oxide traps has given way to a net positive trapped charge which in turn causes a negative threshold voltage shift. Thinning the gate oxide can reduce the effects of this trapped charge, but that invites long-term gate oxide reliability issues [30, 31].

In order for SiC DMOSFET to be useful in high-power switching applications, it is imperative to ensure its stable threshold voltage (V_{TH}) and breakdown voltage (BV)

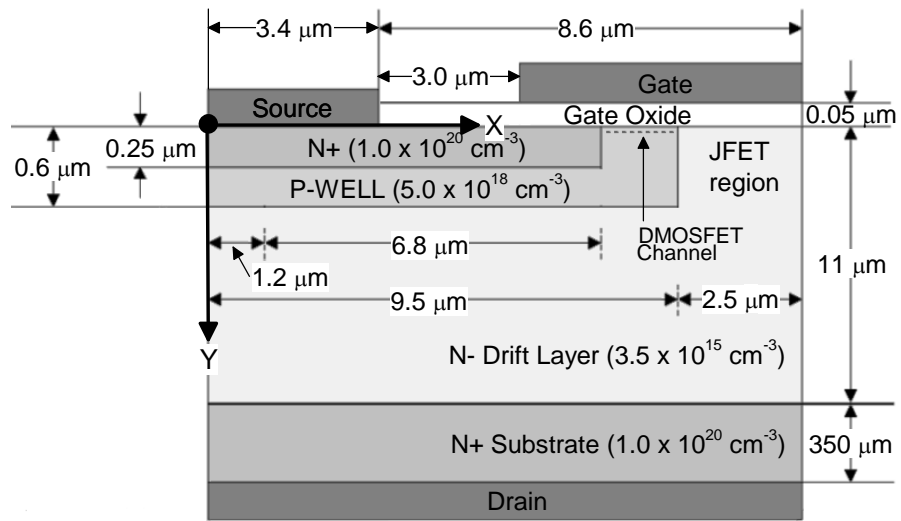
characteristics, when it is in “on” and “off” states, respectively. Thus, in this work the instability of SiC DMOSFETs was assessed by the V_{TH} and BV drifts as a result of bias and temperature stress.

For the threshold voltage instability measurement, the threshold voltages of SiC DMOSFETs were measured before and after different bias stress durations to determine if stress durations and amount of V_{TH} drifts are related. The measurements were also performed at elevated temperatures. The problem with using V_{TH} drift measurements alone as an indicator of magnitude of threshold voltage instability is the lack of consensus on the definition of threshold voltage for SiC DMOSFETs (as described later in the next section). In addition, if measurement sweep time to acquire transfer curves at the conclusion of bias-stress is long, the electrons may be trapped or detrapped during the sweep also, which may result in altered transfer curves and consequently an erroneous extraction of V_{TH} . Recent measurements by Gurfinkel et al. [32], driven by the interest in faster measurement, have shown a clear dependence between the measured magnitude of instability and the speed of the measurement. Due to this reason, in this work, in addition to studying the V_{TH} drift, the drain current transients during the stressing period at both room-temperature and elevated temperatures were also studied to see if monitoring of the drain current transient during stressing can be used to study SiC DMOSFET’s on-state instability.

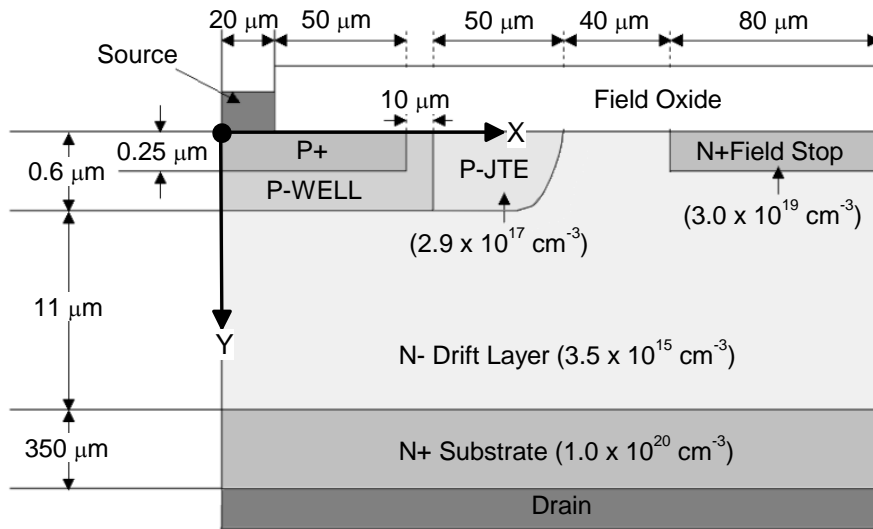
For the breakdown voltage instability measurements, the breakdown voltages of the same SiC DMOSFET devices, tested for the V_{TH} instability, were measured before and after a fixed bias stress duration. A slump in breakdown voltage (BV) was observed

when the DMOSFET was bias stressed at a voltage less than the BV at a high temperature for a period of time. A dynamic recovery of the slumped BV to the pre-stress value during post-stress period was also observed. In order to quantify these effects, the measurements were also performed on the devices with different design dimensions to determine if device dimensions and drifts in the breakdown voltage are related. In addition, electric field, voltage contours, and breakdown voltage simulations have been performed for different SiC/SiO₂ interface charge densities to study the mechanisms responsible for the BV-slump.

The V_{TH} and BV instabilities of DMOSFET may be caused by the mobile ionic charge trapping/detrapping at the SiC/SiO₂ interfaces in the device structure. One of the solutions to suppress the effect of ionic charges is to use a mobile ion gettering dielectric as an interlayer dielectric (ILD) in the DMOSFET structure. ILD films are widely used in semiconductor integrated circuit technologies to separate metal interconnect lines. ILD film is also used in the DMOSFET devices to separate gate and source metal contacts. Desirable characteristic of the ILD films, in addition to the ability to suppress the V_{TH} and BV instability of SiC DMOSFETs, is a gradually tapered step coverage over the patterned gate metal to ensure the continuous coverage of subsequently formed source metal contact over the stepped ILD. In this work, the X-ray photoelectron spectroscopy (XPS) was used to find the material composition of ILD of the DMOSFET previously examined for the V_{TH} and BV instabilities, and the scanning electron microscopy (SEM) was used to analyze the step coverage of the ILD. Literature on materials and flow



(a)



(b)

Figure 2.1: Schematic of (a) a DMOSFET half cell structure and (b) a DMOSFET junction termination extension (JTE) structure

processes for the high quality ILD, mainly developed during 1980s for Si, is researched and improved materials and flow processes for ILD of SiC DMOSFETs are suggested.

2.2. Experiment

2.2.1. DMOSFET under test:

The SiC DMOSFETs were fabricated on a 11 μm thick n-type epitaxial layer ($3.5 \times 10^{15} \text{ cm}^{-3}$) grown on an n-type 4H-SiC substrate. A schematics of the DMOSFET cell and junction termination extension (JTE) structure are shown in Figures 2.1(a) and 2.1(b), respectively. For the cell structure, due to the horizontal symmetry, only the left-half cell is depicted (Fig. 2.1(a)). Each DMOSFET of this work has 625 such cells. The p-well is formed with a multiple energy aluminum implant. Source region was implanted with nitrogen, and a body contact region was co-implanted with aluminum and carbon. The wafer was capped with graphite and annealed for 30 min at 1,675 $^{\circ}\text{C}$ for activating the implants. The graphite was removed with an ashing process and the SiC surface was further prepared by thermally growing a 300 \AA thick sacrificial oxide. The sacrificial oxide is thermally grown to remove (consume) a thin ($\sim 130 \text{ \AA}$) layer of SiC wafer surface, which may have defects created in it during graphite cap deposition, implant annealing, and cap removal steps. A 50 nm thick gate oxide was grown by successive 1,250 $^{\circ}\text{C}$ (in N_2O) and 1,175 $^{\circ}\text{C}$ (in NO) oxidation steps immediately after etching the sacrificial oxide. A liftoff process was used to form nickel ohmic contacts to n+ type regions. A 0.6 μm thick molybdenum gate metal was deposited and patterned and then the ohmic contacts

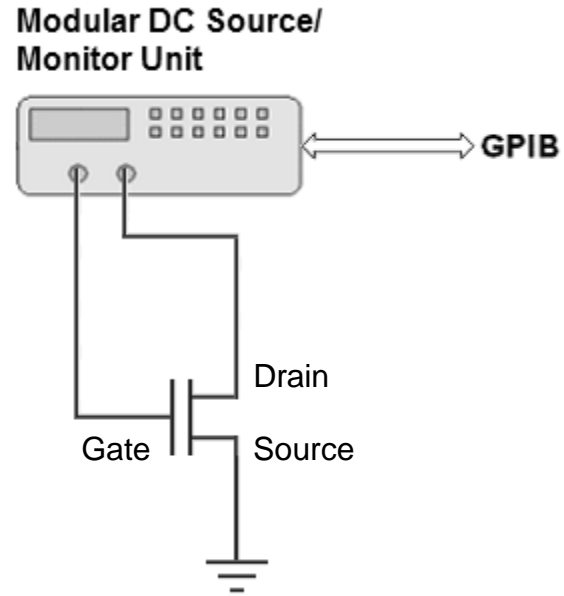
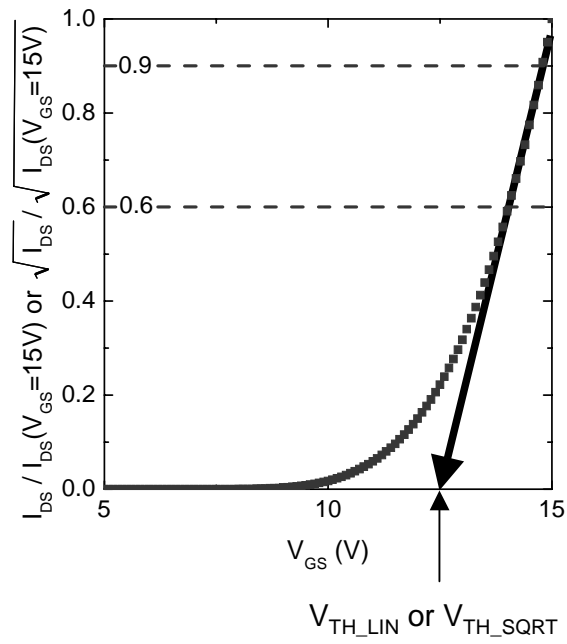
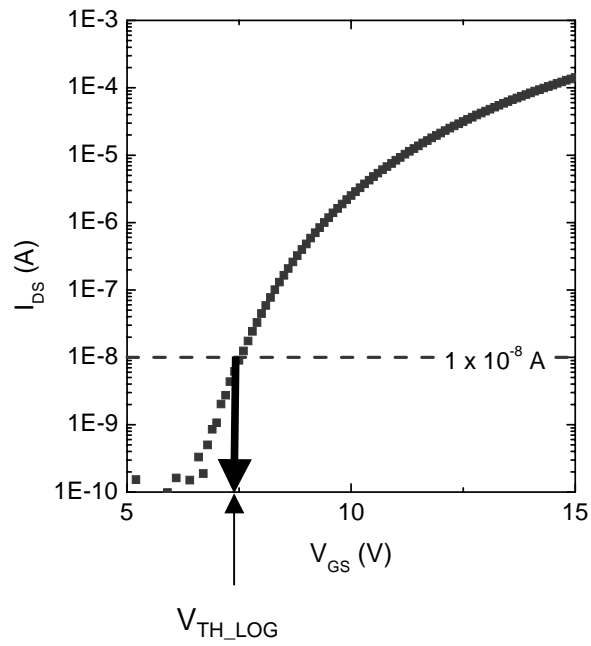


Figure 2.2: Schematic of bias stress induced V_{TH} instability measurement setup

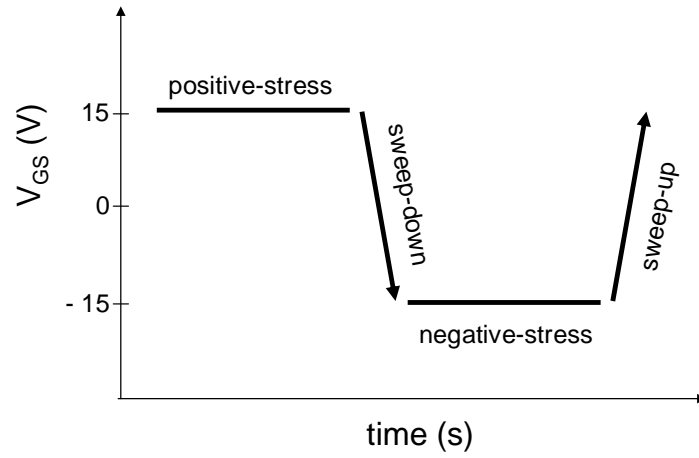


(a)

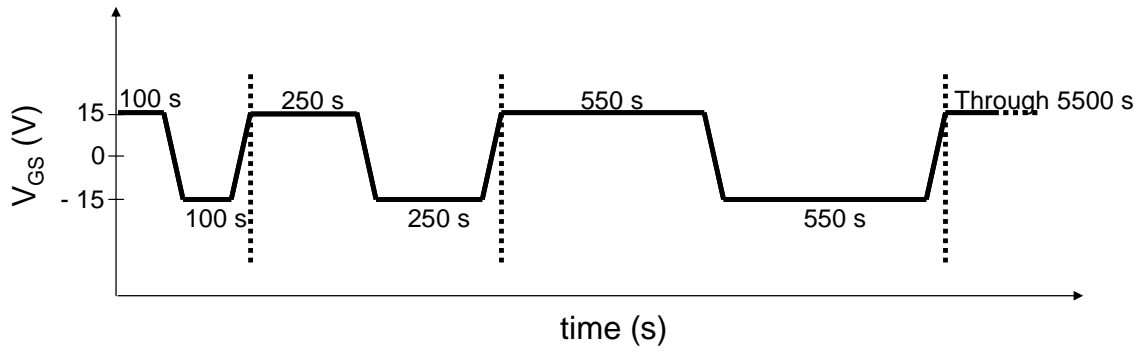


(b)

Figure 2.3: V_{TH} definitions used in this work: (a) V_{TH_LIN} and V_{TH_SQRT} and (b) V_{TH_LOG}



(a)



(b)

Figure 2.4: Schematic of (a) one typical V_{GS} bias-stress cycle indicating all four steps, and (b) series of bias stress cycles used for studying V_{TH} instability

were annealed at 1,050 °C for 3 min The devices were passivated with a silicon nitride film.

2.2.2. Threshold Voltage Instability:

Threshold voltage (V_{TH}) instability measurements on the four SiC DMOSFETs across the wafer were performed using a Hewlett Packard (Agilent) 4142B Modular DC Source/Monitor Unit and the Metrics Interactive Characterization Software (ICS), version 3.6.0. The schematic of the measurement setup is given in Fig. 2.2.

Since SiC DMOSFET's turn-on drain current (I_{DS}) increase with increasing gate-source voltage (V_{GS}) is rather gradual, unlike in Si MOSFET's, there isn't a widely accepted threshold voltage (V_{TH}) definition available for SiC DMOSFETs. Thus, in this work, based on the $i_{DS} - v_{GS}$ transfer characteristics obtained at $V_{DS} = 0.1$ V, the V_{TH} is defined in three ways: (1) V_{TH_SQRT} , which is the v_{GS} -axis intercept of a linear fit to the 90% and the 60% values of $\sqrt{I_{DS}}$ at $V_{GS} = 15$ V, (2) V_{TH_LIN} , which is the v_{GS} -axis intercept of a linear fit to the 90% and the 60% values of I_{DS} at $V_{GS} = 15$ V, and (3) V_{TH_LOG} , which is defined as the V_{GS} value at a drain current of 1×10^{-8} A. Diagrams describing three V_{TH} definitions used in this work are shown in Figures 2.3(a) and (b).

A cycle used for the bias-stress induced threshold voltage instability measurements, shown in Fig. 2.4(a), consists of four different gate biasing steps in the order: (1) keeping the gate-source voltage (V_{GS}) at +15 V (positive-stress) for a certain duration, (2) V_{GS} sweep from +15 V to -15 V (sweep-down), (3) keeping V_{GS} at -15 V

(negative-stress) for the same amount of duration as the positive-stress, and (4) V_{GS} sweep from -15 V to +15 V (sweep-up). During the entire cycle the drain-source voltage (V_{DS}) was kept small at 0.1 V, which ensures operation of the device in linear region. The Hewlett Packard 4142B with fast integration setting takes about 2 s to perform sweep-down and sweep-up (from +15 V to -15 V and -15 V to +15 V, respectively, with increments of 0.1 V). The sweep time of 2 s is relatively slow compared to ones reported for the threshold instability measurements (10 μ s – 1 s) [32-34]. At the end of each step in the bias-stress cycle, all terminals were returned to 0 V and it took about 2 s to setup and start the subsequent step.

First, a cycle for a stress duration of 180 s (each of positive- and negative-stress) was performed as an initialization step and then the cycle is repeated six more times for different stress durations of 100, 250, 550, 1,000, 2,500, and 5,500 s (see Fig. 2.4(b)). During sweep-down and sweep-up steps, the threshold-voltages (defined in three ways as explained above) were extracted from the resulting transfer curves (i_{DS} - v_{GS}). For all three threshold-voltage definitions (V_{TH_SQRT} , V_{TH_LIN} , and V_{TH_LOG}), the threshold-voltage drifts (ΔV_{TH}) for each cycle were calculated as the difference between the V_{TH} from the sweep-down step and the V_{TH} from the sweep-up step. The V_{TH} drifts (ΔV_{TH}) were plotted against the stress duration. In addition to the threshold-voltage drifts, the drain current (i_{DS}) transient recorded during the positive-stress is also used as an indicator of the magnitude of device instability. These measurements were repeated at different temperatures in the range 30 °C – 130 °C.

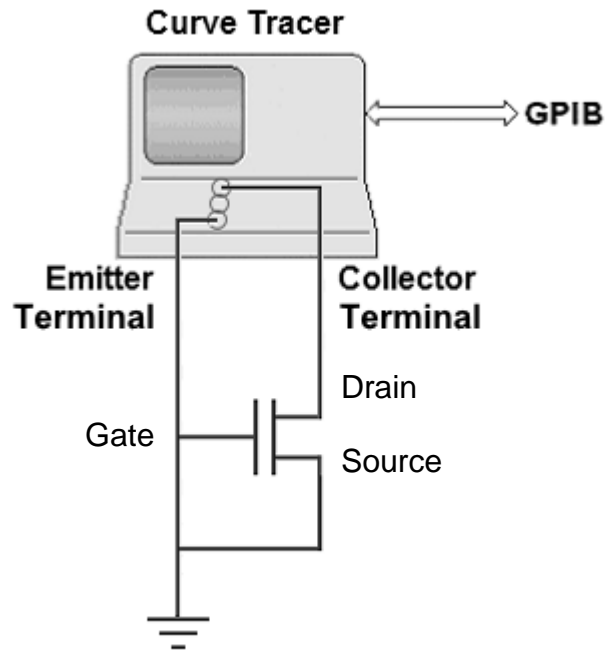


Figure 2.5: Schematic of bias stress induced BV instability measurement setup

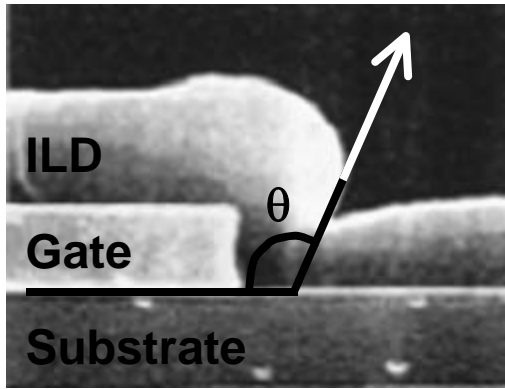
2.2.3. Breakdown Voltage Instability:

Breakdown voltage (BV) instability measurements on several SiC DMOSFET devices, some previously tested for the V_{TH} instability, were performed using a Sony/Tektronix 370A Digital Programmable Curve Tracer. The schematic of the measurement is given in Fig. 2.5.

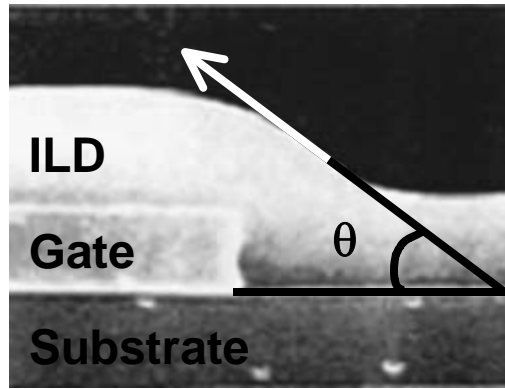
In a DMOSFET, the region encircled by the p-well is known as a JFET region because the p-well/n⁻-drift layer region below the gate oxide acts similar to the p-n junction gate region of JFET transistors (Fig. 2.1(a)). In this work, the avalanche breakdown characteristics of SiC DMOSFETs with different JFET region widths (4 μm , 5 μm , and 6 μm) have been studied. The experimental results were compared with computer simulation results.

The BV instability measurements were performed on DMOSFETs by applying a positive bias to the drain terminal while holding the gate and the source terminals at the ground potential. The avalanche breakdown voltage (BV) is defined as the bias voltage (V_{DS}) where the current (I_{DS}) is 10 μA . First, the breakdown voltage prior to the stress, BV_0 ($\sim 1,800$ V), was measured. The device is then stressed at $V_{DS} = 1,200$ V (approximately two-third of BV_0) for two hours. At the termination of the stress, the BV is measured again and was observed to be less than the BV_0 value. The slumped BV immediately starts recovering toward the BV_0 value in the avalanche region after the stress is removed. During the recovery time, I_{DS} would decrease for constant V_{DS} . In order to retain the $I_{DS} = 10\mu\text{A}$ needed to track the actual BV, V_{DS} was increased continuously.

The BV instability measurements were also simulated using a Synopsys's Medici version Y-2006.06 software. Medici is device simulation tool; which takes device parameters such as dimensions (x, y, and z) of composing material (SiC, SiO₂ and Ni), doping concentrations and/or trap charges in the materials into account; predicts electrical, thermal and optical characteristics of the device. First, the electric field distribution at the SiC/gate oxide interface region in the DMOSFET cell structure, for different JFET region widths, was modeled for the bias stress condition, $V_{DS} = 1200$ V. Due to the horizontally symmetrical cell structure, only left half of DMOSFET cell structure, shown in Fig. 2.1(a), is simulated. Later, the electric field distribution at the SiC/field oxide interface region in the DMOSFET junction termination extension (JTE) structure, shown in Fig. 2.1(b), was also modeled for the same bias stress condition. In the simulation, both the cell and JTE structures are described using the x-y coordinates, where x is the coordinate parallel to the channel and y is the coordinate perpendicular to the channel. The origin of x-y is the leftmost edge at the surface of the SiC, as indicated in Figures 2.1 (a) and 2.1(b). Once the directionality of the electric field distribution in both structures is studied at the bias stress condition, the BV for both structures is simulated using the same protocol used for the experimental part (V_{DS} where $I_{DS} = 10$ μ A). Then, the different amounts of SiC/SiO₂ interface charges are introduced in both the cell and the JTE structures, and the corresponding BV for both structures is simulated.



(a)



(b)

Figure 2.6: (a) Abrupt and (b) gradual step coverage of ILD (adopted from Ref. [35])

2.2.4.High quality interlayer dielectric for DMOSFET:

As one of solutions to suppress the V_{TH} and BV instabilities of SiC DMOSFET, realizing a high quality interlayer dielectric (ILD) in the DMOSFET is suggested. As mentioned earlier, desirable characteristic of the ILD films, in addition to the ability to suppress the V_{TH} and BV instability of the DMOSFETs, is a gradually tapered step coverage over the patterned gate metal, which ensures the continuous coverage of subsequently formed source metal contact over the stepped ILD.

As-deposited ILD film formed directly over patterned metal contacts have abrupt steps (Fig. 2.6(a)), but subjecting the film to heat treatment at a high temperature, where it undergoes a viscous glass flow, transforms the abrupt step coverage into a smooth step coverage (Fig. 2.6(b)). The extent of ILD flow is often measured by a step coverage angle [35], which is the angle between the ILD film surface at the step and the horizontal substrate (as shown in Figures 2.6(a) and 2.6(b)). The smaller the step coverage angle, the more successful the glass flow is. A high temperature heat treatment for a long duration improves the step coverage of the film; however, a prolonged high temperature process causes undesirable implant diffusion. In addition, once the gate oxide is formed, the temperature of any subsequent heat treatment should not exceed the gate oxidation temperature. Hence, it is desirable to find an ILD material, which flows at a low temperature.

Currently, the SiO_2 films doped with phosphorus (phospho-silicate glass, PSG) or boron (boro-silicate glass, BSG) or boron and phosphorus (boro-phospho-silicate glass, BPSG) are widely used as ILD material. Among the three widely used ILD materials,

PSG is known to be the best for the mobile ion gettering property, and BPSG is known to be the best for the low temperature flow property. If proper B and P concentrations are carefully chosen, BPSG can also be a mobile ion getter. Thus, BPSG is the most promising ILD material, which fulfills both mobile ion gettering and smooth step coverage requirements simultaneously.

Though, increasing the B and P concentrations of the BPSG film reduces the film's flow temperature, there are some constraints one should consider before fixing the B and P concentrations in the BPSG film. For high B and P concentration levels: (1) the BPSG may become hygroscopic [35-37]; (2) crystalline particles may form on the BPSG surface, during annealing in the nitrogen ambient [38, 39]; and (3) polarizing nature of the BPSG may cause a shift in the electrical behavior of the MOS devices [40-42]. Needless to say, mobile ion gettering requirement of BPSG must be fulfilled by maintaining a certain relationship between B and P concentrations.

In this work, first, the ILD of the SiC DMOSFETs, previously examined for their V_{TH} and BV instability, were analyzed for material composition and step coverage by the X-ray photoelectron spectroscopy (XPS) and the scanning electron microscopy (SEM), respectively. Then, literature on materials and flow processes for the high quality ILD, mostly developed during 1980s for Si, is researched to suggest improved materials and flow processes for the ILD of SiC DMOSFETs.

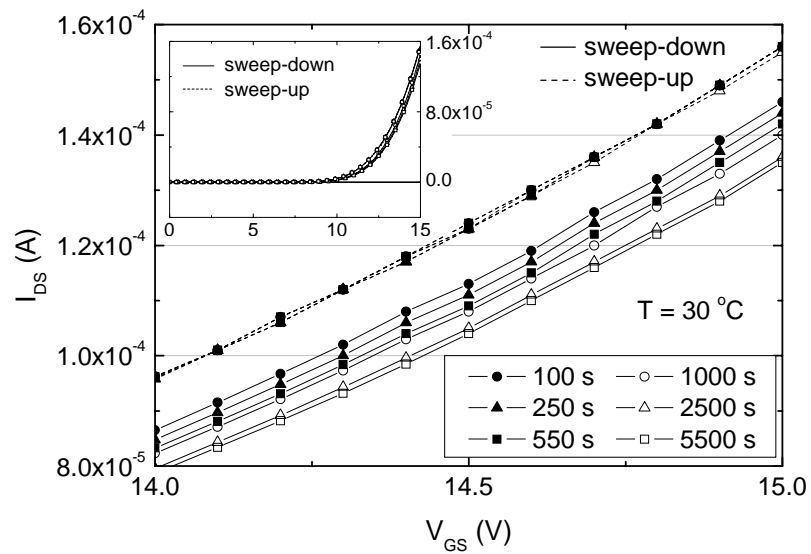


Figure 2.7: Transfer curves (i_{DS} vs. v_{GS}) at 30 °C, measured after different positive- and negative-stress durations

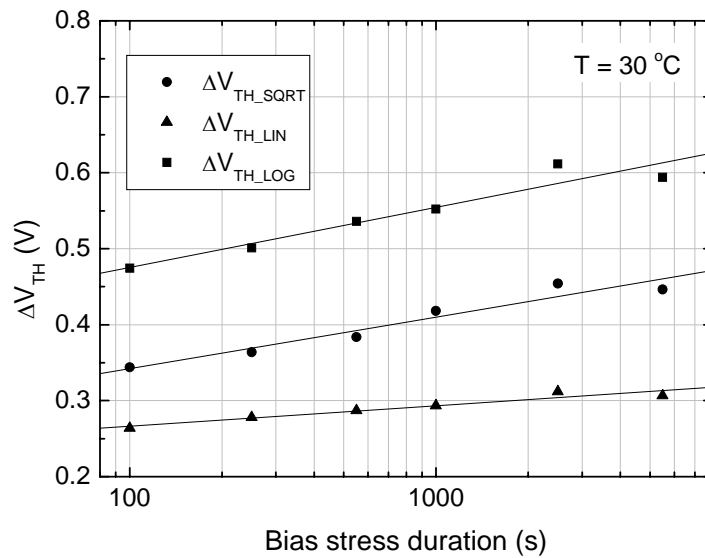


Figure 2.8: V_{TH} shifts (ΔV_{TH}), calculated for three definitions, versus stress duration, at 30 °C

Using the data published in the literature, BPSG flow temperature contours (for 30 min tube furnace heat treatment in dry N₂ at 1 atm pressure) are generated for different B and P concentrations in the BPSG film. The constraints on the maximum B and P concentrations, due to the above mentioned side-effects, are also developed using the data published in the literature, and they are superimposed on the flow temperature contours. By examining the contours and the constraints, the optimum B and P concentrations in the BPSG film, which provide problem-free viscous flow at a low temperature, can be established for the flow process considered (a 30 min tube furnace heat treatment in dry N₂ at 1 atm pressure). In order to reduce the flow temperature further and/or to shorten the time period of the flow process, for the established optimum B and P concentrations in the BPSG film, alternative flow processes are researched.

2.3. Results and Discussion

2.3.1. Threshold Voltage Instability:

Transfer curves, obtained by V_{GS} sweep-down and sweep-up after different positive- and negative-stress durations at 30 °C are shown in Fig. 2.7. Note that the V_{GS} sweep-down and sweep-up are performed following the positive-stress step and the negative-stress step, respectively (see Fig. 2.4(a)). Transfer curves recorded after positive-stress (during sweep-down) are at lower current levels than those recorded after the negative-stress (during sweep-up). As discussed later, it is because during positive-stress the SiC/SiO₂ interface traps and SiO₂ near interface traps are populated with

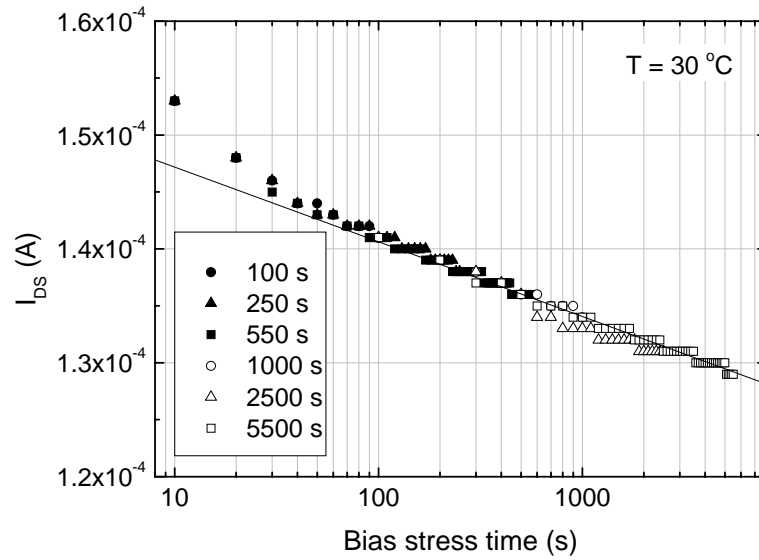


Figure 2.9: The I_{DS} transients, recorded during positive-stress step, at 30 °C, for different stress durations

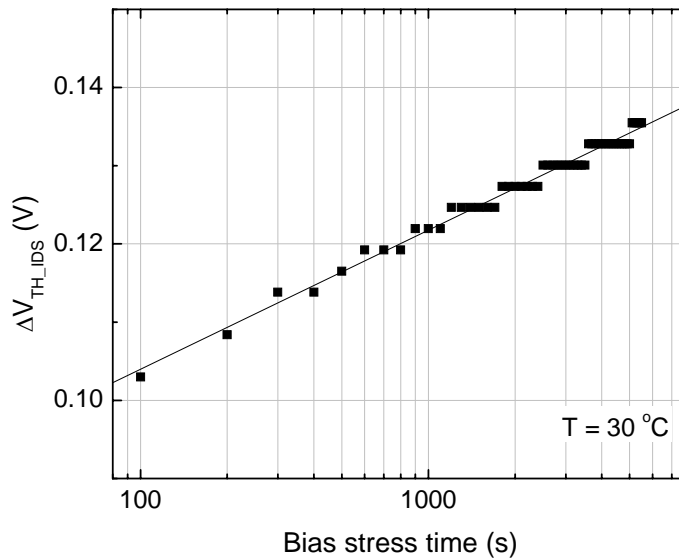


Figure 2.10: The ΔV_{TH_IDS} , calculated using the linear $i_{DS}-v_{DS}-v_{GS}$ equation of n-channel MOSFET with the 5500 s I_{DS} transient data in Fig. 2.9, versus stress time, at 30 °C

carriers (electrons), which increases the threshold voltage of the device, and during negative-stress they are emptied. The V_{GS} sweep-down yielded a smaller I_{DS} at any given V_{GS} with an increasing positive-stress duration (this is due to build-up of more interface and near interface trapped charge resulting in an increase in threshold voltage), and the V_{GS} sweep-up following the negative-stress presents the I_{DS} at its original value. As explained earlier, the threshold voltage shifts (ΔV_{TH}) are calculated as the difference between the threshold voltages extrapolated from the transfer curves of the sweep-down (V_{TH_DOWN}) and the sweep-up (V_{TH_UP}) steps. The ΔV_{TH} values obtained for all three definitions of V_{TH} are plotted against the stress duration in Fig. 2.8. The definition by which the threshold voltage is calculated makes a difference in the magnitude of the threshold voltage shift, but the shifts for all three different threshold voltage definitions show the same trend, where ΔV_{TH} is positive and increases almost linearly with the logarithmic stress time (t). Lelis et al. [33, 34] attribute this linear ΔV_{TH} shift with the logarithmic stress time to charge tunneling into the gate dielectric traps during the positive-stress, which later is emitted by the traps during the negative-stress. The traps are considered as uniformly distributed across the channel.

The drain currents recorded during positive-stress steps of six different durations, at 30 °C, are plotted in Fig. 2.9. Chronologically, the positive-stress for 100 s was performed first followed by the negative-stress for 100 s; then, the positive-stress for 250 s was followed by the negative-stress for 250 s, and so on until the positive-stress for 5,500 s is followed by the negative-stress for 5,500 s (Fig. 2.4(b)). For all stress durations there is a decay in the drain current transient. At 30 °C, the decayed current at the

completion of each positive-stress step is fully restored during the subsequent negative-stress step.

During positive-stress steps (where $V_{GS} = +15$ V and $V_{DS} = +0.1$ V), the devices under test are operated in linear region and the linear i_{DS} - v_{DS} - v_{GS} equation of n-channel

$$\text{MOSFET, } i_{DS} = \mu_n C_{OX} \frac{W}{L} \left[(v_{GS} - V_{TH})v_{DS} - \frac{v_{DS}^2}{2} \right], \text{ suggests that the } \Delta i_{DS} \text{ is proportional}$$

to $-\Delta V_{TH}$. Therefore, a linear decrease in I_{DS} with the logarithmic stress time (as seen in Fig. 2.9) corresponds to a linear increase in V_{TH} with the logarithmic stress time (as seen in Fig. 2.8).

As mentioned earlier, the experimental setup, used for this work, reset both V_{GS} and V_{DS} to 0 V at the end of each step in the bias-stress cycle, and there is an unintentional 2 s of relax time before the subsequent step starts. The 2 s of relax time, especially after the positive-stress, is problematic because some of the trapped electrons can escape before the acquisition of the transfer curve (at the following sweep-down step). Due to the escaped electrons, the V_{TH_DOWN} is underestimated. In addition, because of the slow V_{GS} sweep time of 2 s (instrument limitation), the electrons may be trapped or detrapped during the acquisition of the transfer curve, which results in further alteration in transfer curves and consequently result in an ambiguity of extracted V_{TH} . In order to ensure accuracy of ΔV_{TH} technique, a sophisticated experimental setup is required: the setup should be capable of applying V_{GS} and V_{DS} continuously without resetting them to 0 V between consecutive steps in the cycle, and should be capable of sweeping V_{GS} fast so that no electrons are trapped/detrapped during the sweep. The linear ΔV_{TH} shifts with

logarithmic stress time observed for three V_{TH} definitions (Fig. 2.8) convey that there is a threshold voltage instability problem in the SiC DMOSFET, but they are not used to quantify the actual amounts of ΔV_{TH} shifts due to the ambiguity of the transfer curves associated with slow V_{GS} sweep acquisition, and the usage of individually defined V_{TH} definitions.

On the other hand, the drain current transient technique, carried out in this work, is easy to implement with a less complicated experimental setup. Since the drain current transient technique does not suffer from the ambiguities discussed above, this technique is favorable over the ΔV_{TH} technique to study the on-state device instability of SiC DMOSFET. The threshold voltage drift, ΔV_{TH_IDS} , calculated using the 5500 s I_{DS} transient from Fig. 2.9, against bias stress time is shown in Fig. 2.10. The linear $i_{DS-v_{DS-v_{GS}}}$ equation of n-channel MOSFET (where $V_{GS} = 15$ V, $V_{DS} = 0.1$ V, and $\mu_n C_{ox} \frac{W}{L} = 0.00369$) is solved for a time dependent threshold voltage, $V_{TH_IDS}(t)$, using a time dependent drain current, $I_{DS}(t)$, and then the time dependent V_{TH_IDS} shift, $\Delta V_{TH_IDS}(t)$, is calculated as the difference between the threshold voltage at 't' seconds after the stress, $V_{TH_IDS}(t)$, and the initial threshold voltage, $V_{TH_IDS}(0)$. As shown in Fig. 2.10, the ΔV_{TH_IDS} is linear with logarithmic stress time, and the shift increases at a rate of 0.019 V/decade, which corresponds to 8.2×10^9 electrons/cm² being trapped every decade (ΔQ

$$(\text{electrons/cm}^2) = \left(\frac{\epsilon_{OX}}{t_{OX}} \cdot \Delta V_{TH_IDS} \right) / q, \text{ where } t_{OX} = 500 \text{ \AA}.$$

In this work, similar threshold voltage shift and drain current transient behavior were observed for all four devices tested across the wafer. A plausible cause for the V_{TH} instability, seen in Figures 2.8 and 2.10, has been believed to be the electrons being captured and released by the SiC/gate dielectric interface traps and the bulk gate dielectric near interface traps during the positive-stress and the negative-stress steps, respectively [33, 34]. This explains the I_{DS} decay during the positive-stress and the implicit recovery during the negative-stress step (as seen in Fig. 2.9). At 30 °C, the decay and the subsequent recovery are repeatable and there is no apparent saturation in decay even after the 5,500 s stress duration. At 30 °C, since the I_{DS} is observed to return to the same value at the start of each positive-stress following the negative-stress of the same duration as the previous positive-stress step, the electron emission rate of the traps located at the SiC/SiO₂ interface and near interface seem to be equal to or less than the capture rate of these traps. In conclusion, the increase in the threshold voltage and the decrease in drain current with the stress time at 30 °C are detrimental to the reliability of the SiC DMOSFET device. In addition, in this study, it was also found that monitoring of the drain current transient during the positive-stress step is simple and accurate and thus it is a favorable method for characterizing the bias stress induced on-state instability in the SiC DMOSFETs.

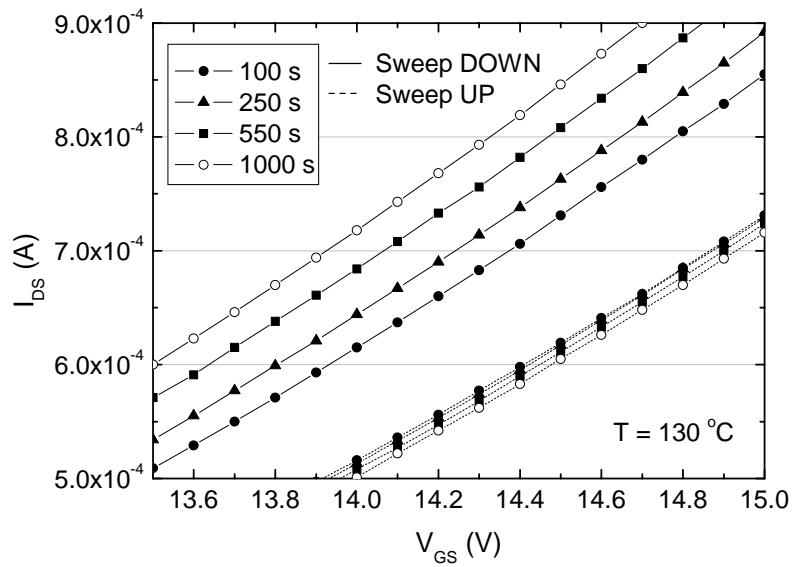


Figure 2.11: Transfer curves (i_{DS} vs. v_{GS}) at 130 °C, measured after different positive- and negative-stress durations

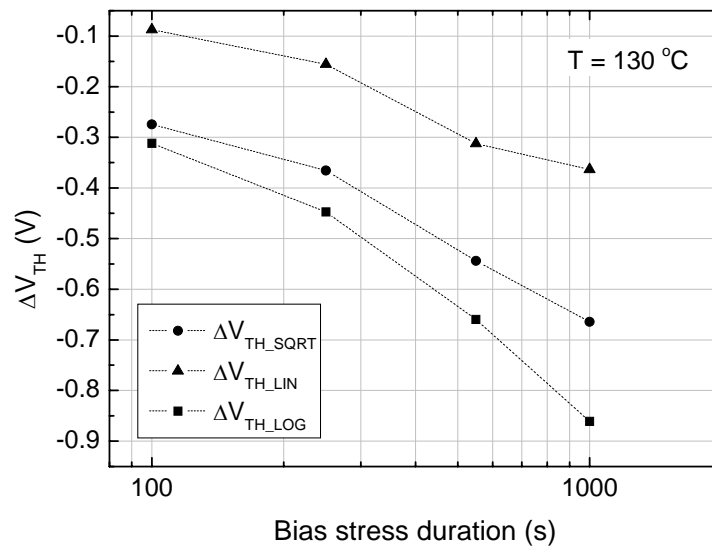


Figure 2.12: V_{TH} shift (ΔV_{TH}), calculated for three definitions, versus stress duration, at 130 °C

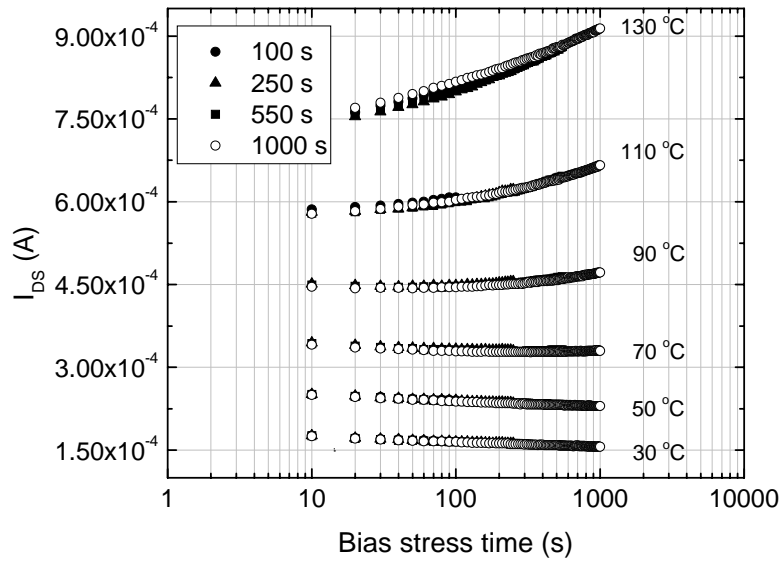


Figure 2.13: The I_{DS} transients, recorded for different positive-stress durations, at different device operating temperatures

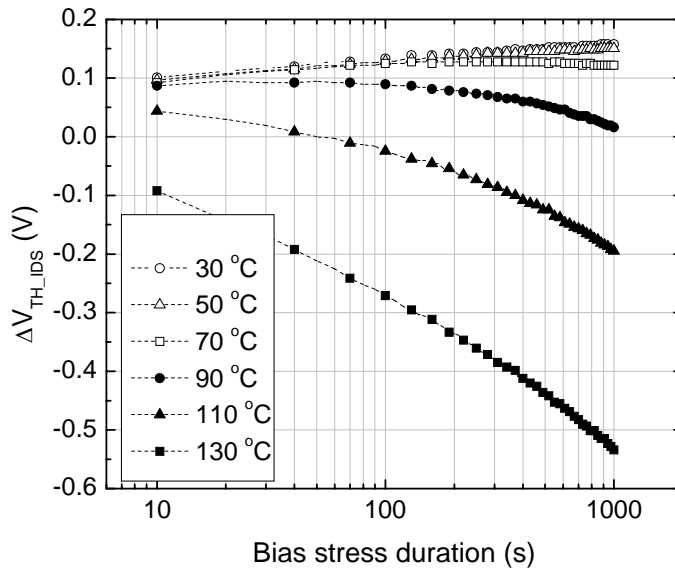


Figure 2.14: The ΔV_{TH_IDS} , calculated using the linear $i_{DS}-v_{DS}-v_{GS}$ equation of n-channel MOSFET with the 1000 s I_{DS} transient data in Fig. 2.13, versus stress time, at different device operating temperatures

Stress measurements as explained above were also performed at elevated temperatures on the same four devices, which were characterized at 30 °C. Similar threshold voltage shift and drain current transient behavior at elevated temperatures were observed for all four devices tested across the wafer. Transfer curves obtained after different positive- and negative-stress step durations, at 130 °C, are shown in Fig. 2.11. Transfer curves obtained after the positive-stress step (i.e. during the sweep-down step) are at a higher I_{DS} level than those obtained after the corresponding negative-stress step (i.e. during the sweep-up step), which is opposite to the case of 30 °C (Fig. 2.7). The V_{GS} sweep-down yielded a larger change (increase) in I_{DS} (for a given V_{GS}) for increasing positive-stress duration. The negative-stress always restored the I_{DS} close to its original value (for a given V_{GS}), but not quite as good as observed earlier for 30 °C in Fig. 2.7. The threshold voltage shifts (for all three V_{TH} definitions) observed after the positive-stress at 130 °C are shown in Fig. 2.12. The ΔV_{TH} is negative (which is opposite to what was observed at 30 °C in Fig. 2.8), with an increasing magnitude for longer stress durations.

The drain current transients, recorded during four positive-stress steps of 100, 250, 550, and 1000 s duration at six different temperatures in the range 30 °C – 130 °C, are shown in Fig. 2.13. The range of drain current variation has increased with increasing temperature. Unlike in the case of 30 °C, the drain current at 130 °C increased with an increasing positive-stress time. Also at 130 °C, the i_{DS} transients for four different stress durations are not quite on top of each other (unlike in Fig. 2.9 at 30 °C). It seems the negative-stress step which follows the positive-stress step is not resetting the traps,

located at the SiC/SiO₂ interface and also close to the interface in SiO₂, completely, as seen before at 30 °C in Fig. 2.9. The drain-currents decreased with an increasing stress time at low temperatures, but increased with the stress time at high temperatures. For example, the I_{DS} transient at 70 °C initially shows a decay but at around 300 s starts showing an increase in I_{DS} with increasing stress time. For the 90 °C temperature, the trend reversal occurred at around 70 s. If the stress time is extended beyond 5,500 s, a similar reversal in I_{DS} transient could have been seen even for the 30 °C temperature, too. The shift in ΔV_{TH_IDS} , calculated using the linear $i_{DS} \sim v_{DS} - v_{GS}$ equation of n-channel MOSFET with the 1000 s I_{DS} transient data in Fig. 2.13, with stress duration at different temperatures is shown in Fig. 2.14. The ΔV_{TH_IDS} shift is negative (at high temperatures) and the magnitude of the shift (V/°C) increased with an increasing temperature. Similar behavior is observed for three other definitions of V_{TH} as well.

The above drain current and threshold voltage shift behavior suggests that a mobile ion effect probably is appearing at the elevated temperatures. At the elevated temperatures, the mobile ions become active. When the positive bias is being applied to the gate at elevated temperatures, the positively charged ions become mobile and are repelled away from the gate electrode towards the SiC/SiO₂ interface. The number of mobile ions at the interface increases with the stress duration. The mobile positive charge at the interface decreases the threshold voltage and helps in increasing the channel carrier concentration and consequently the drain current. The threshold stress time, where the drain current slope changes from a negative value to a positive value decreased with increasing temperature, because a higher temperature promotes the mobility of positive

ions. The negative-stress of same duration as the positive-stress is very effective in emptying the interface and near interface oxide traps, which captured electrons during the positive-stress; but it is not equally effective in moving the mobile positive ions away from the SiC/SiO₂ interface toward the metal gate at high temperatures. Much longer negative stress duration than the positive-stress duration probably will reset the device at high device operating temperatures.

Triangle voltage sweep (TVS) measurements, which are traditionally used to identify the ionic contaminants [43, 44], were performed on the four DMOSFETs (at General Electric) and it was found that mobile ions in the order of $\sim 1 \times 10^{11} \text{ cm}^{-2}$ exist in the devices. The molybdenum sputter targets (a process from which the molybdenum gate metal is deposited) typically come with 99.95% purity, whereas really clean metals can be procured with "5-9s" purity, 99.999% pure. Unfortunately molybdenum is hard to refine to the 5-9s level so that the material is not usually as clean as it should be. It is believed that the molybdenum gate metal is responsible for introducing the mobile ions of density $\sim 1 \times 10^{11} \text{ cm}^{-2}$. The effect of mobile ions would be to shift the V_{TH} of the DMOSFET by Q/C_{ox} , where $Q = 1 \times 10^{11} \text{ charges/cm}^2$. The mobile ions can be pushed to the SiC/SiO₂ interface with positive gate bias, or be pulled to the gate with negative gate bias. For an inversion mode MOSFET with a p-type body region and a positive gate bias, the $1 \times 10^{11} \text{ cm}^{-2}$ mobile ionic charge should lower the V_{TH} voltage by 0.23 V.

A $V_{\text{TH_IDS}}$ shift at 130 °C after 1000 s stress duration is -0.53 V as seen in Fig. 2.14. The amount of shift getting larger for longer stress duration and at higher temperature suggests existence of a larger than $1 \times 10^{11} \text{ cm}^{-2}$ mobile ionic charge in the

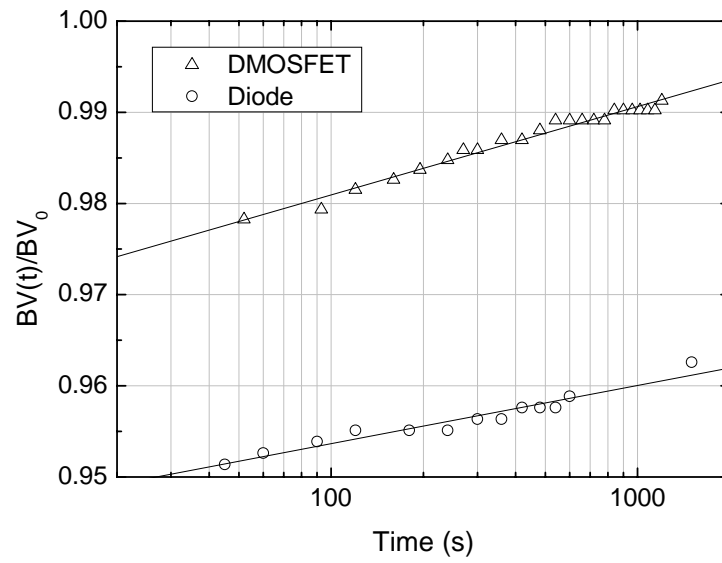
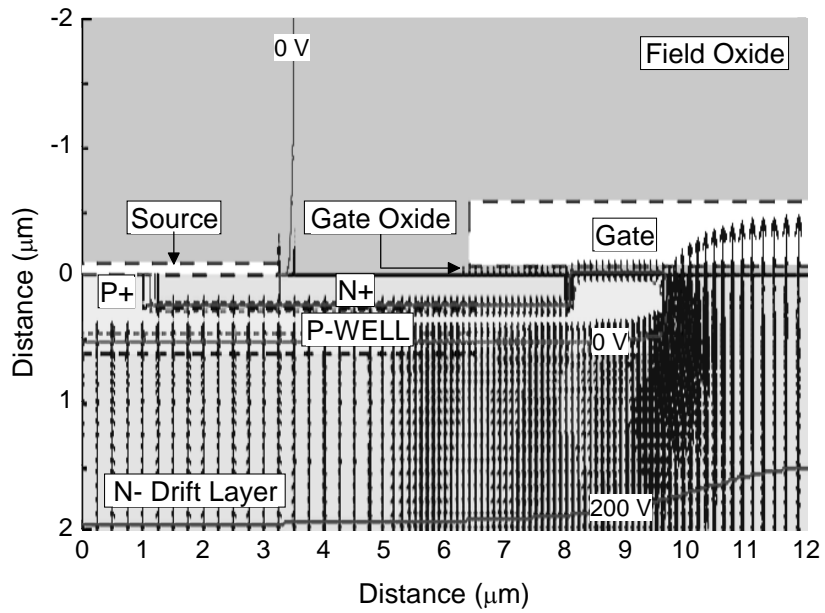


Figure 2.15: Recovery of the slumped BV after the removal of the bias stress at 175 °C for the DMOSFET and the p-n junction diode

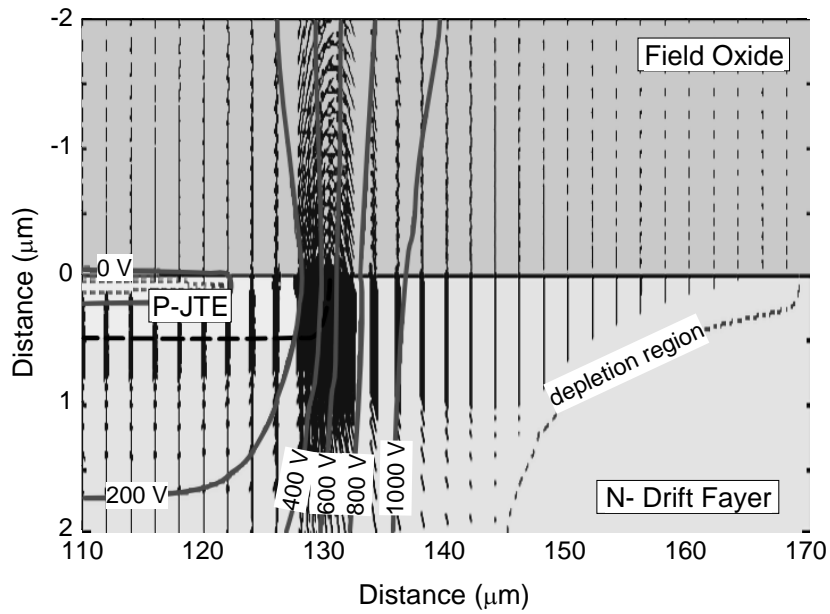
DMOSFET devices of this work. Trost et al. [45], who have investigated passivation dielectrics (silicon nitride) of Si power devices, observed a mobile charge density of $\geq 1 \times 10^{12} \text{ cm}^{-2}$ in the dielectrics. Although their investigation is on the Si power devices, the passivation of their Si power device is almost identical to that of SiC DMOSFET of this study. Hence, it is safe to assume that a mobile charge density of similar order exist in the DMOSFET device of this work as well. Trost et al. [45] hypothesizes that the charge may be due to hydrogen ions from a passivation film of silicon nitride. Unfortunately, the exact sources of the thermally activated ionic charges, which are responsible for the DMOSFET's V_{TH} instability in this work, are unknown at this time, and deserve further investigation.

2.3.2. Breakdown Voltage Instability:

First, the bias stress (2 hours at $V_{DS} = 1,200 \text{ V}$) induced BV-slump measurements were performed on five DMOSFET devices having a $5 \mu\text{m}$ JFET region width, whose typical pre-stressed breakdown voltage (BV_0) is about $1,800 \text{ V}$. For all five $5 \mu\text{m}$ JFET region width devices tested across the wafer, the measurements performed at room-temperature did not yield BV-slump, but the measurements performed at $175 \text{ }^\circ\text{C}$ yielded BV-slump. For the $175 \text{ }^\circ\text{C}$ case, the slumped BV values recovered toward the BV_0 value with time after termination of the stress. An example of dynamic BV recovery of the DMOSFET toward the BV_0 value with time is shown in Fig. 2.15. The vertical axis is the breakdown voltage, BV, normalized to the BV_0 value, and the horizontal axis is time



(a)



(b)

Figure 2.16: Simulated electric field vector and voltage contours in (a) the DMOSFET cell structure and in (b) the JTE structure

elapsed after termination of the stress. The recovery appears to be linear with logarithmic time. At 175 °C, for all five 5 μm JFET region width devices, a BV-slump ($\Delta BV = BV_0 - BV_{120\text{min}}$) of 170 ± 20 V (errors are relatively large due to the fast initial recovery of BV-slump and due to the manual adjustment of V_{DS} from 1200 V to capture the BV value) was observed and the recovery behavior after stress is similar. Because the BV instability (slump and recovery) are negligible at the room temperature and they are detectable only at a high temperature, as in case of V_{TH} instability of DMOSFET, mobile ionic charge trapping and detrapping at SiC/SiO₂ interface are the most plausible cause for BV instability as well. There are two SiC/SiO₂ interfaces in the DMOSFET structure: SiC/gate oxide interface in the cell structure and SiC/field oxide interface in the JTE structure. Thus, the charge trapping/detrapping phenomena is considered to have taken place at the (1) SiC/gate oxide interface in the cell structure, at the (2) SiC/field oxide interface in the JTE structure, or at (3) both locations.

First, in order to determine if the charge trapping/detrapping phenomena have taken place at the SiC/gate oxide interface in the cell structure, the electric field distribution at the SiC/gate oxide interface region in the cell structure was modeled for the different JFET region widths for the bias stress condition, $V_{DS} = 1,200$ V. With an intention of introducing interface charges later, the simulation was done initially with no interface charges. The simulated electric field flux and voltage contours are shown in Fig. 2.16(a) for the 5 μm device. The maximum electric field (E_{MAX}), to which the SiC/gate oxide interface region is subjected, is observed at the center of the JFET region (the right most edge of the horizontal axis in the half cell structure) for all devices regardless of

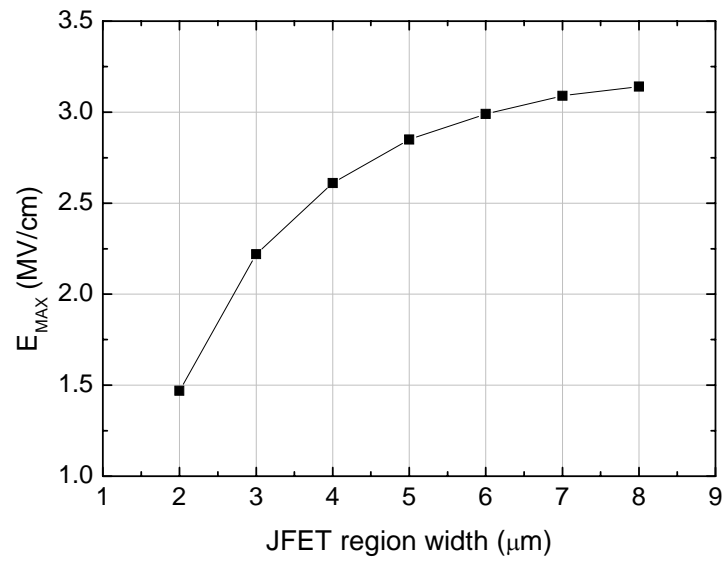


Figure 2.17: Plot of simulated E_{MAX} , at the SiC/gate oxide interface in the DMOSFET cell structure, as a function of JFET region width

their JFET region widths. The relationship between the simulated E_{MAX} and the JFET region width is plotted in Fig. 2.17. As seen in the figure, the E_{MAX} grows rapidly with the JFET region width at first, and then saturates as the JFET width increases. This behavior can be explained by the charge sharing among the depletion regions surrounding the JFET region for short JFET region widths. When the JFET region width is very wide, there is an electric field component entering straight up into the gate oxide from the bottom drain terminal, and the electric field component is at its maximum value, E_{MAX} , at the center of the JFET region. As the JFET region width becomes shorter, the depletion region (created at the p-well/ n⁻-drift region junction) surrounding the JFET region overlaps at the center of the JFET region, weakening the straight electric field component due to diversion of the electric field flux towards the charge shared among the depletion regions. The E_{MAX} for the 4 μm , 5 μm , and the 6 μm devices are 2.60, 2.85, and 3.00 MV/cm, respectively. Since, the maximum electric field into the gate-oxide at the bias stress is smaller for the device with shorter JFET region width, if the BV-slump is only due to the charge trapping at the SiC/gate oxide interface, then the magnitude of the BV-slump should be smaller for the shorter device.

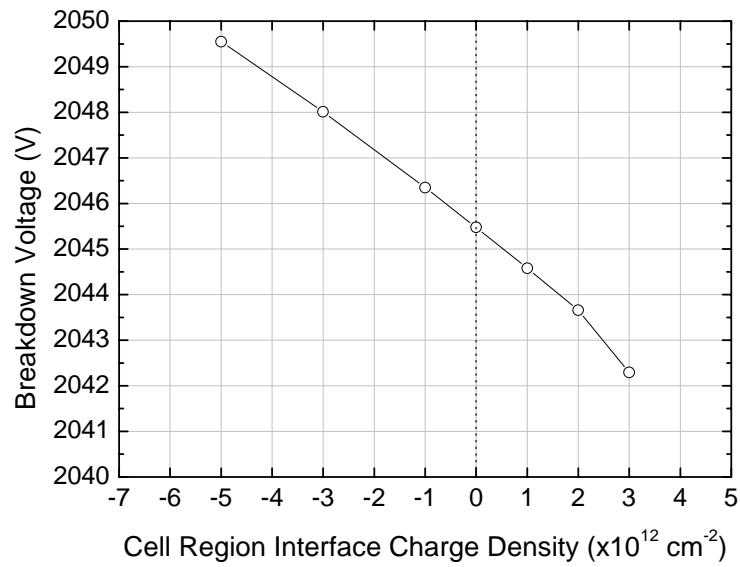
To verify the prediction of the simulation, the BV-slump was experimentally measured for two other DMOSFET devices having 4 μm and 6 μm JFET region widths using the same protocol as described above for the 5 μm JFET region width device ($V_{DS} = 1,200$ V, 2 hours, 175 °C). The BV-slump and their recovery after the stress termination observed for three 4 μm devices and three 6 μm devices are similar to those of the 5 μm device described earlier. The ΔBV is 142 ± 20 V and 150 ± 17 V,

respectively, for the 4 μm and 6 μm devices. Comparing these values with the ΔBV value of 170 ± 20 V for the 5 μm devices suggests that there isn't an apparent trend between the ΔBV value and the JFET region width as predicted by the simulation. In fact, the ΔBV is roughly the same for all devices. This suggests that the DMOSFET BV instability can not be assigned to its cell structure only.

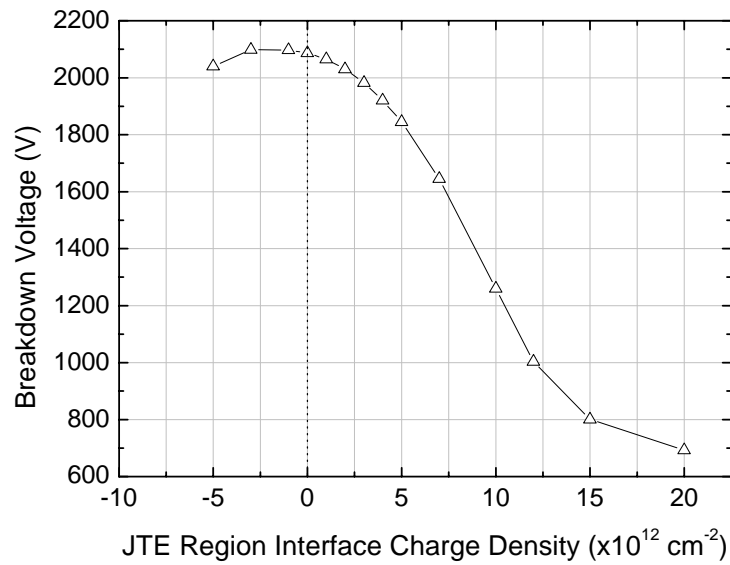
In order to determine if the BV-slump and its recovery are caused by the JTE structure, the BV-slump measurements were performed on four p-well/n⁻-drift layer SiC diodes at 175 °C. The SiC diodes, as name implies, have no SiC/gate oxide interface, but have the same termination design as the DMOSFET devices (Fig. 2.1(b)). The diodes were fabricated on a different wafer from the DMOSFETs, which has a higher n⁻-epi layer doping compared to the DMOSFET. The processing steps followed for the diode are same as those used for the JTE structure in the DMOSFET. The BV_0 of the diodes is smaller ($\sim 1,550$ V) than that of the DMOSFETs ($\sim 1,800$ V) due to a higher n⁻-epilayer doping. The BV-slump is prevalent in all four diodes across the wafer with approximately the same magnitude and the ΔBV is 137 ± 17 V, which is close to the ΔBV values (~ 150 V) measured for the DMOSFET devices. The slump recovery of the diode BV, after the removal of stress, is a function of time as shown in Fig. 2.15 for one of the diodes. The logarithmic recovery trend for the diode is consistent with the earlier observation for the DMOSFET (also in Fig. 2.15). The diode results suggest that the BV-slump and its recovery can be caused almost exclusively by the JTE structure, as the diodes which have no cell structure also exhibited similar BV instability.

The electric field distribution at the SiC/field oxide interface region in the JTE structure was modeled for the bias stress condition, $V_{DS} = 1,200$ V. With an intention of introducing interface charges later, the simulation was done initially with no interface charges. The simulated electric field flux and voltage contours are shown in Fig. 2.16(b). The simulated E_{MAX} , to which the SiC/field oxide interface region is subjected, is observed at the outer edge of the JTE region ($x = 130$ μm). The value of E_{MAX} is 1.8 MV/cm, and is same for all four devices (the 4 μm , 5 μm , and the 6 μm JFET region width DMOSFETs and the diode) because they have the same JTE structure. Thus, the gate oxide in the cell structure is subjected to a stronger electric field than the field oxide in the JTE structure during the bias stress (the smallest E_{MAX} of 2.6 MV/cm for the shortest 4 μm JFET region width DMOSFET device). What's interesting to mention is the directionality of the electric field flux in the field oxide. The electric field fluxes entering into the field oxide from the substrate ($x \geq 130$ μm and $y = 0$ μm) are bent toward the source terminal and revolved around $x = 130$ μm , as they arrive at the SiC/field oxide interface. Such field bending implies that the positive charges may be accumulated at the SiC/field oxide interface, and then may be pulled towards the source terminal due to the potential gradient in the negative x-direction.

In order to find the effect of the positive charges on the device breakdown voltage, initially, the BVs were simulated for the cell structure (5 μm JFET region width) and for the JTE structure without any contribution of the SiC/SiO₂ interface charges, and subsequently with the contribution of the interface charges. The introduced interface charge represents the net effect of charge from the interface traps, the fixed oxide charge,



(a)



(b)

Figure 2.18: Plot of simulated BV as a function of interface charge density for (a) the DMOSFET cell structure and (b) the JTE structure

the accumulated mobile ions, the oxide bulk charges, etc. The introduced interface charges (cm^{-2}) were uniformly distributed along the interface ($x = 3.4 \mu\text{m} - 12 \mu\text{m}$ for the cell structure in Fig. 2.1 (a) and $x = 20 \mu\text{m} - 250 \mu\text{m}$ for the JTE structure in Fig. 2.1 (b)). A plot between the simulated BV and the amount of interface charges introduced for the cell structure and for the JTE structure are shown in Figures 2.18(a) and 2.18(b), respectively. The simulated BV values (where $I_{\text{DS}} = 10 \mu\text{A}$) for the cell and for the JTE structures are 2,045 V and 2,087 V, respectively, for zero interface charges at the SiC/SiO₂ interfaces. Thus, the BV for the cell structure, which is lower than that of the JTE structure, will become the BV of the DMOSFET, if there are no charges at the SiC/SiO₂ interface. The variation in BV, for the cell structure, as a function of the interface charge density seems to be linear (see Fig. 2.18(a)). The p-well begins to be inverted creating a channel (even for $V_G = 0 \text{ V}$), if the interface charge density is $\geq 4 \times 10^{12} \text{ cm}^{-2}$, resulting in a current $> 10 \mu\text{A}$, which is the definition of BV current in this study. Thus, in Fig. 2.18(a), the simulated BV is shown only up to the interface charge density of $3 \times 10^{12} \text{ cm}^{-2}$.

The variation in BV, for the JTE structure, as a function of the interface charge density (see Fig. 2.18(b)) resembles the variation in BV as a function of the dopant dose of the JTE region, as simulated by Baliga [46]. For a large negative interface charge density, the breakdown is observed at the inner edge of the p⁻-type JTE region ($x = 80 \mu\text{m}$ and $y = 0.6 \mu\text{m}$ in Fig. 2.1(b)), and for a large positive interface charge density, the breakdown is observed at the outer edge of the p⁻-type JTE region ($x = 130 \mu\text{m}$ and $y = 0.6 \mu\text{m}$ in Fig. 2.1(b)). The introduced negative or positive interface charges at the

SiC/field oxide interface subtract from or add to the dopant sheet concentration of the JTE region ($1.2 \times 10^{13} \text{ cm}^{-2}$), proving the resemblance between the variation in BV as a function of the interface charge density and the variation in BV as a function of the dopant dose of the JTE region. The effect of positive interface charges is a slump in the BV for both the cell and the JTE structure, but the effect is nominal for the cell structure and is significant for the JTE structure. The interface charge density of $+3 \times 10^{12} \text{ cm}^{-2}$ slumps the BV of the cell structure by only 3 V (from the charge free value of 2,045 V), and the BV of the JTE structure by ~ 100 V (from the charge free value of 2,087 V). This simulation suggests that the measured BV-slumps for the SiC DMOSFET devices is caused almost exclusively by the SiC/field oxide interface charges in the JTE structure, implying that the JFET region width in the cell structure does not play a significant role in the BV instability as observed before for the measured slumped BV values of these devices. Simulation results indicate that the typical 150 V of BV-slump for the DMOSFETs and the diodes is caused by $\sim 4 \times 10^{12} \text{ cm}^{-2}$ of interface charges in the JTE structure (see Fig. 2.18(b)), which is one-third of the sheet dopant concentration ($1.2 \times 10^{13} \text{ cm}^{-2}$) of the p⁻-type JTE region.

In order to find the most vulnerable location for the interface charges within the JTE structure to decrease the BV, an interface charge of density $5 \times 10^{12} \text{ cm}^{-2}$ was selectively introduced along the SiC/field oxide interface, and the corresponding BV was simulated. The interface charges were distributed to cover a portion of the p-type JTE region (80 μm – 130 μm) from the rightmost edge of the device ($x = 250 \mu\text{m}$), i.e. from 120 μm to 250 μm , from 110 μm to 250 μm , from 100 μm and 250 μm , and so on.

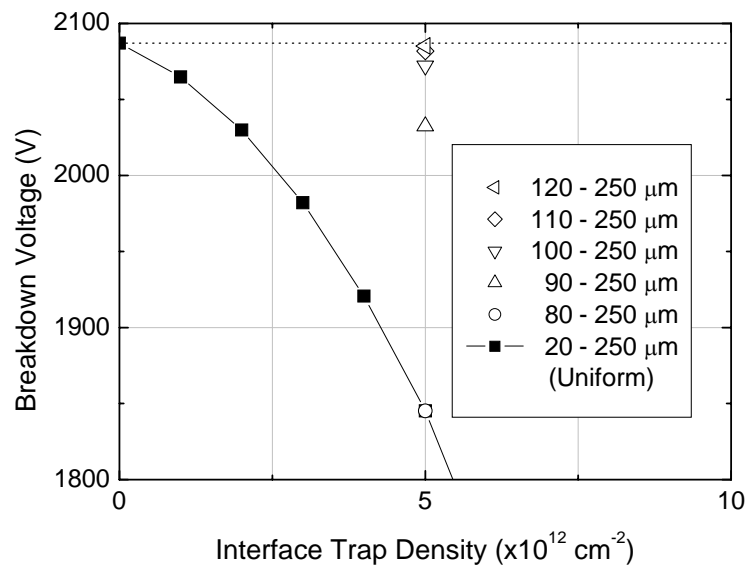
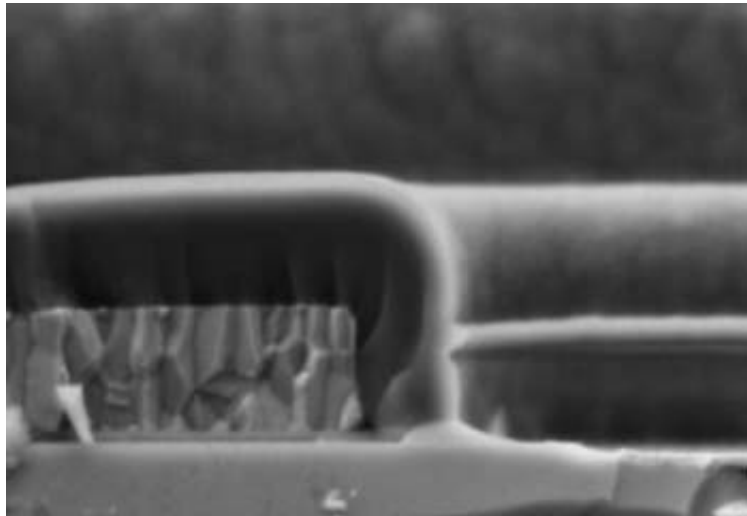


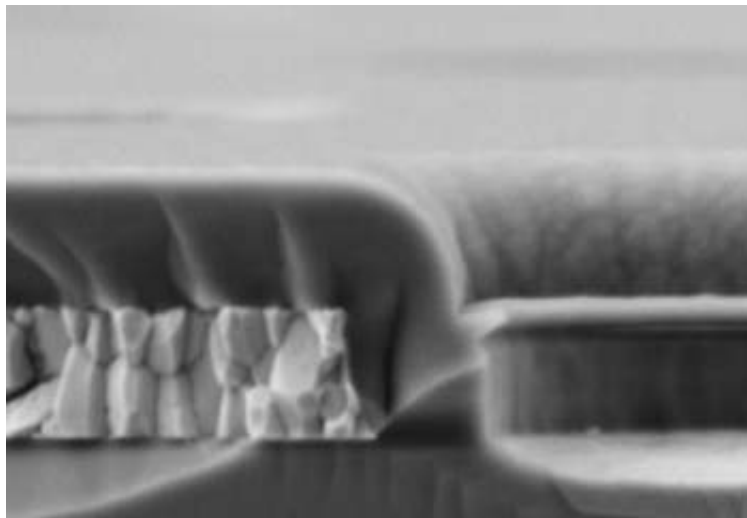
Figure 2.19: Plot of simulated BV as a function of the location of the SiC/field oxide interface charges in the JTE structure

Variation in BV as a function of the location of the interface charge density ($5 \times 10^{12} \text{ cm}^{-2}$) along with the variation in BV as a function of the interface charge density (part of Fig. 2.18(b)) are shown in Fig. 2.19. As seen in Fig. 2.19, the interface charges, distributed to cover the JTE structure between $100 \mu\text{m} - 250 \mu\text{m}$, lower the BV by only 15 V, whereas the interface charges, distributed between $90 \mu\text{m} - 250 \mu\text{m}$, lower the BV by 55 V. The interface charges, distributed between $80 \mu\text{m} - 250 \mu\text{m}$ (which includes the entire JTE region, $80 \mu\text{m} - 130 \mu\text{m}$), lower the BV by 242 V, which is the same amount of BV-slump value simulated for uniformly distributed interface charges ($20 \mu\text{m} - 250 \mu\text{m}$) earlier. Thus, the vulnerable location for the interface charges within the JTE structure to decrease the BV is between $80 \mu\text{m}$ to $100 \mu\text{m}$, especially around the inner edge of the JTE region ($80 \mu\text{m} \leq x \leq 90 \mu\text{m}$ in Fig. 2.1(b)). The directionality of the electric field in Fig. 2.16(b) suggests the possibility of positive charge accumulation around the inner edge of the p⁻-type JTE region during the bias stress at 1200 V.

Because the BV instability is negligible at the room temperature and is detectable only at a high temperature, as in case of V_{TH} instability of DMOSFET, positive mobile ionic charges are the most plausible cause for BV instability as well. As discussed earlier in the V_{TH} instability section, the thermally activated positive mobile ionic charges may be hydrogen ions ($\geq 1 \times 10^{12} \text{ cm}^{-2}$) from the device passivation film of silicon nitride and/or may be contaminants ($\sim 1 \times 10^{11} \text{ cm}^{-2}$) from molybdenum gate metal. As BV simulation results indicated, there are $\sim 4 \times 10^{12} \text{ cm}^{-2}$ of positive mobile ionic charges in the DMOSFET. The density of hydrogen ion ($\geq 1 \times 10^{12} \text{ cm}^{-2}$) is at the same order of



(a)



(b)

Figure 2.20: SEM image of the 3 wt % phosphorous doped ILD, (a) taken before (but after densification anneal at 925 °C for 30 min) and (b) after the 1,050 °C/3min RTA contact anneal

magnitude as our simulated result ($\sim 4 \times 10^{12} \text{ cm}^{-2}$). Unfortunately, the exact sources of the thermally activated ionic charges, which are responsible for the DMOSFETs' BV instability, are unknown at this time, and deserve further investigation.

2.3.3. High quality interlayer dielectric for DMOSFET:

The DMOSFET device, which has been examined for its V_{TH} and BV instabilities, had 6,000 Å thick phosphorus doped SiO_2 (phospho-silicate glass, PSG) previously deposited as an ILD over a patterned 0.65 μm thick gate structure step (0.6 μm thick molybdenum gate metal and 500 Å thick gate oxide). The PSG underwent two high temperature processes: an ILD densification anneal at 925 °C for 30 min (performed immediately after the PSG deposition) and a rapid thermal ohmic contact anneal at 1,050 °C for 3 min (performed immediately after source/drain Ni contact metallization), both in N_2 ambient. The X-ray photoelectron spectroscopy (XPS) of the film revealed that the PSG had a P concentration of 3 wt % (3 wt % PSG). Figure 2.20(a) is an SEM image of the DMOSFET device taken after the first heat treatment (the ILD densification anneal at 925 °C for 30 min) but before the second heat treatment (the rapid thermal ohmic contact anneal at 1,050 °C for 3 min). As seen in Fig. 2.20(a), the step coverage of the 3 wt % PSG has a large step coverage angle (in fact almost as abrupt as the as-deposited PSG) indicating that the temperature/time used for the densification anneal process (925 °C/30 min) was not high/long enough to flow the PSG. Figure 2.20(b) is an SEM image of the DMOSFET device taken after the second heat treatment. As seen in Fig. 2.20(b), the step

coverage of the PSG, though improved a bit compared to Fig. 2.20(a), still has a large step coverage angle indicating that the temperature/time used for the second high temperature process (1,050 °C/3 min) was not high/long enough to flow the PSG, either.

The 3 % PSG would have flowed if it were subjected to a heat treatment at a higher temperature than the 925 °C/1,050 °C and for a longer duration than the 30 min/3 min, used in this work. During an extended high temperature treatment, the ILD is expected to become into a viscous fluid minimizing defects such as seams, voids, and pinholes (which were formed during the ILD deposition) and transforming the abrupt step coverage into the gradual step coverage. The driving force behind the ILD flow is the minimization of surface tension, which is enhanced by a long duration high temperature treatment. However, the prolonged high temperature process can lead to implant diffusion, deepening the doping profiles of device active regions. Once the gate oxide is deposited, as a precaution, the temperature of any subsequent high temperature process should never exceed the gate oxidation temperature (1,250 °C is the gate oxide formation temperature used for the SiC DMOSFETs of this work). For these reasons, it is desirable to find an ILD material, which flows at a low temperature and over a short time period.

The V_{TH} and BV instabilities observed earlier and above SEM images indicate that the 3 wt % PSG is not good as an ILD material to meet the mobile ion gettering and the step coverage requirements. Therefore, the objective of this work is to figure out an improved ILD material for use in the SiC DMOSFET to meet the above mentioned requirements. Though this work was done for SiC DMOSFET, the results of this work

are applicable to Si and other semiconductor material device technologies as well, where the ILD films are used.

Before going into the details of the material aspects of ILD films for reducing the flow temperature, first the topological aspect of ILD film is discussed. As stated before, the extent of ILD film flow is measured by the step coverage angle (as defined in Figures 2.6(a) and 2.6(b)). The smaller the step coverage angle, the more successful the glass flow is. A thicker ILD over a given thickness of gate structure yields a smaller step coverage angle compared to a thinner ILD, which is a desired result, but, a thicker ILD is expensive in terms of materials used and the deposition time, and also prone to failure due to a high mechanical stress, which may lead to cracking of the ILD film. Hence, it is desirable to keep the ILD film thickness as minimal as possible while maintaining its electrical integrity. For reducing the required ILD film thickness (and for maintaining a small step coverage angle) the gate metal thickness should be made as small as possible.

The SiO_2 (a thermally grown natural dielectric on SiC and Si) flows at a temperature of $1,725\text{ }^\circ\text{C}$, which is very high for any semiconductor (SiC, Si, and III-V compound) device technology. In case of the SiC DMOSFET of this study, the ILD film's viscous flow temperature should be below $1,250\text{ }^\circ\text{C}$, because the DMOSFET's gate oxide is formed at $1,250\text{ }^\circ\text{C}$. The flow temperature of SiO_2 can be lowered by introducing phosphorus into the SiO_2 (which results in phospho-silicate glass, PSG). The PSG is known as a diffusion barrier to moisture and also as a mobile ion getter. Thus, PSG has been widely used as a threshold voltage stabilizer in MOS transistors. The good flow property of the PSG makes it also as a suitable material for the ILD film. The flow

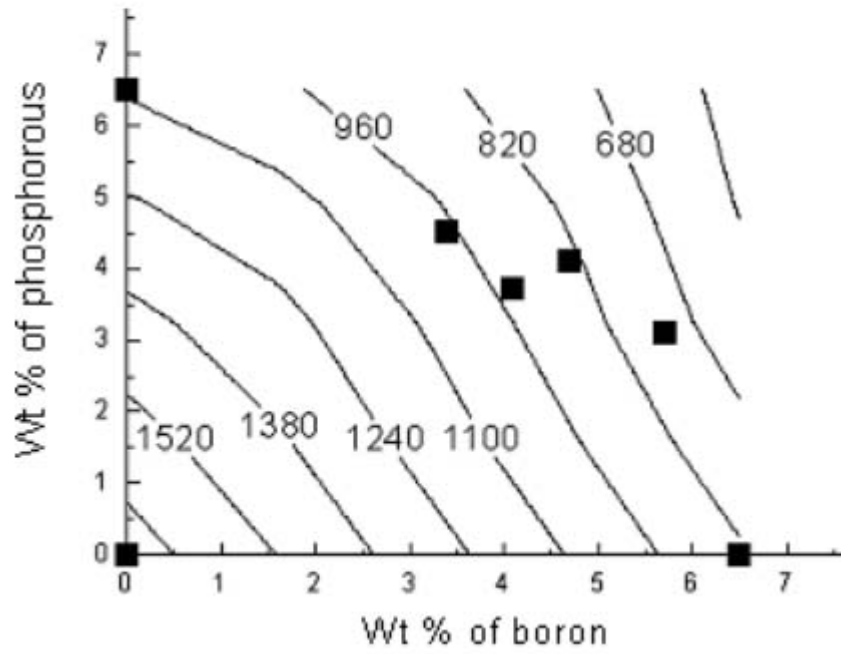


Figure 2.21: Flow temperature contours (tube furnace, 30 min, dry N₂, 1 atm) for different B and P wt percentages in BPSG film (the data points are taken from Ref. [36])

temperature of the PSG film can be lowered by increasing the phosphorus wt percentage, but, the upper limit on the phosphorus wt percentage is set by the hygroscopic nature of the PSG, which may lead to interconnect (aluminum) corrosion and/or electrical instability. Hence, excessive P wt percentage in the PSG film is undesirable. In addition, the benefit of decreasing glass flow temperature further by increasing the P wt percentage diminishes at high P wt percentage values [47]. The flow temperature of PSG can be reduced further, without using excessive P doping, by adding boric oxide (B_2O_3) to the PSG, which yields boro-phospho-silicate glass (BPSG). This means the flow temperature of the BPSG is significantly lower than that of the PSG. The BPSG films also have lower as-deposited intrinsic tensile stress and lesser defects (seams, voids, and pinholes) compared to the PSG, making the BPSG more favorable material over the PSG for ILD. Depending on the boron concentration, the flow temperature can be lowered by 150-350 °C. A high boron concentration makes the flow temperature of the BPSG low. A BPSG flow temperature as low as 700 °C has been reported [48]. Unfortunately, a large boron concentration in the BPSG makes it hygroscopic.

Flow temperatures for BPSG composed with different B and P concentrations are researched and the flow temperature contours are generated (Fig. 2.21) with an OriginLab's Origin version 7.0220 software. The contours were generated with Renka-Cline Gridding method using the experimental data published by Kern et al. [36], for different B and P concentrations in the BPSG film. A reasonable amount of BPSG flow temperature data is available in literatures for different B and P concentrations, but, this data is inconsistent, because the step coverage angle used to define the successful flow is

different for different authors. Also, the BPSG film thickness used for studying the flow is different among different reports and flow conditions (such as type of anneal, anneal duration, ambient, and pressure) are rarely matched between the reports. For these reasons, mixing of data published by different authors is avoided. After thorough literature search, it was found that Kern et al. [36] published the most amount of flow temperature data for the same heat treatment conditions (tube furnace, 30 min, dry N₂, and 1 atm) as used in this work on the 3 wt % PSG film. The seven data points from Kern et al. [36] may not be sufficient to generate precise contours; however, the contour should provide us an estimate of the necessary boron and phosphorus wt percentages in the BPSG film, for achieving a desired viscous flow temperature. By examining the contours, the 3 wt % PSG is expected to flow at around 1,450 °C. Hence, the 925 °C/30 min heat treatment, for the 3 P wt% PSG ILD film in the present DMOSFET process, was done at a temperature too low to flow the PSG, as seen in Fig. 2.20(a). The second short (3 min) heat treatment after source/drain Ni contact metallization at 1,050 °C was also insufficient to flow the PSG, as seen in Fig. 2.20(b). Hence, adding B to the PSG helps in reducing the flow temperature.

Although a higher phosphorous and boron concentrations in the BPSG allow us to achieve a lower BPSG flow temperature, there are some limitations to consider. As mentioned earlier, the PSG becomes increasingly hygroscopic at high phosphorus levels, resulting in phosphoric acid formation and consequent metal corrosion when the device using such PSG is operated in humid environment. Thus, it is recommended that the P concentration in the PSG film be limited to 7 wt % to minimize phosphoric acid

formation [35, 37]. There are no reports on the upper limit of phosphorus concentration in the BPSG, as related to its hygroscopic nature, but it is reasonable to assume that it should not exceed the limit established for the PSG. Therefore, an upper limit (or constraint) on the phosphorus concentration in the BPSG film is set at 7 wt %. The BPSG films containing over 5 wt % boron tend to be very hygroscopic, forming boronic acid and becoming unstable [35]. Therefore, an upper limit (or constraint) on the boron concentration is set at 5 wt %.

Constraint 1: $P \text{ wt } \% \leq 7$, To Avoid Phosphoric Acid Formation

Constraint 2: $B \text{ wt } \% \leq 5$, To Avoid Boronic Acid Formation

Yoshimaru et al. showed the growth of crystalline boron-phosphate (BPO_4) particles on the surface of the BPSG films having high total boron and phosphorus concentration, after they were subjected to annealing in nitrogen atmosphere at a temperature exceeding 900 °C [38]. These particles are formed during the cooling step of the annealing cycle by the gas-phase reaction of the boron and the phosphorus atoms (that have diffused out from the BPSG surface) with the trace amounts of oxygen in the nitrogen ambient. These particles are not acceptable because they cause metal residues to remain around them after the subtractive metal line process, thereby causing short circuits in the metallization [39]. Boron rich BPSG film surface, induced due to the different out-diffusion mechanisms of boron and phosphorus atoms in the BPSG film, supposedly acts as a nucleation site of the BPO_4 . The out-diffusion mechanisms of the boron and the

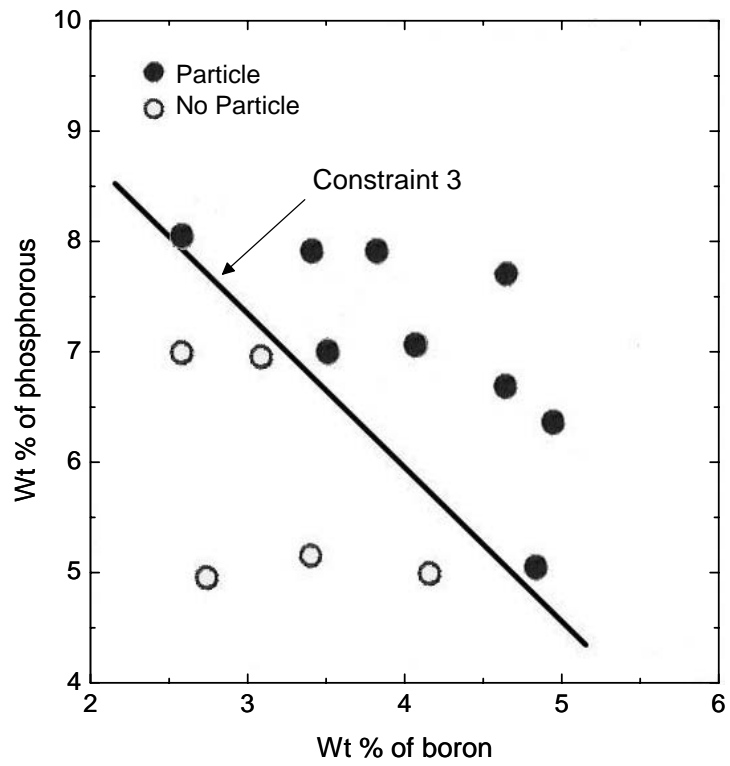


Figure 2.22: Effect of B and P wt percentages on the growth of particles after annealing at temperatures > 900 °C in nitrogen for 15 min (the data points are taken from Ref. [38])

phosphorus atoms in the BPSG film are different for different annealing (cooling) ambient conditions. For example, in the N₂ ambient, the out-diffusion of boron is low and phosphorus is high, making the surface concentration of boron high, consequently, providing an ideal condition for the formation of BPO₄ particles. Yoshimaru et al. [38] reported that the particle growth is suppressed in high N₂ pressure and is further suppressed in an O₂ ambient (because of a decrease in phosphorus out-diffusion), and the particle growth is completely eliminated in an oxygen-steam atmosphere. Since the BPO₄ particles are mainly formed during the cooling step of the annealing cycle, the rapid cooling rate of the RTA may help suppressing the particle growth. A dip in methanol readily dissolves the particles and restores the clear appearance of the films, but leaves the surface and the first few hundred angstroms of the film with a depleted boron concentration [36, 38]. Using the experimental data published by Yoshimaru et al. [38], the empirical relation, which provides a practical limit on the total boron and phosphorus concentrations in the BPSG film to avoid the BPO₄ particle formation for annealing in N₂, as shown in Fig. 2.22, was formulated. This empirical relation is given below.

Constraint 3: $[P \text{ wt \%} + 1.4 (B \text{ wt \%})] < 11.5$, To Avoid Boron Phosphate Particle Formation.

One of the most important objectives of this study is to incorporate mobile ion gettering characteristic to the BPSG in order to suppress the V_{TH} and BV instabilities of SiC DMOSFET. As stated before, the main reason for adding B into the PSG to form

BPSG is to reduce the glass flow temperature. There is no literature on the required B and P concentrations in the BPSG with regard to its gettering capability. The reason why BPSG has not been fully studied for its mobile ion gettering capability is because the mobile ion gettering capability of BPSG is inferior to that of PSG.

The PSG, known as an effective mobile ion getter, consists of a locally negatively charged pentavalent element phosphorus, which represents a favorable site for a mobile positive ion, such as sodium, to getter. On the other hand, the trivalent element boron in BPSG, which introduces an electron deficiency, could offset the gettering characteristics of pentavalent element phosphorus [47]. The P_2O_5 provides P and the B_2O_3 provides B in the silicate glass. The difference between the number of P_2O_5 in BPSG, n_P , and the number of B_2O_3 in BPSG, n_B , must be greater than the number of positive mobile ions, n_A , in order to guarantee the gettering capability of the BPSG film, and thus:

$$n_P - n_B > n_A.$$

Since the molecular weights of B_2O_3 and P_2O_5 are 70 g and 142 g, respectively, the inequality roughly becomes:

$$[P \text{ wt \%} - 2 (B \text{ wt \%})] > \text{Required net P wt \%}.$$

The minimum concentration of P in PSG required for mobile ion gettering during bias-temperature aging (10^6 V/cm gate stress over 10 years) used in a 200 Å thick gate oxide is 4 wt % [49]. Thus, assuming that (1) both PSG and BPSG film are mobile ion free at the time of their deposition and (2) the same exact number of mobile ions enter into the PSG or the BPSG film from outside sources during bias-temperature aging, then to ensure effective mobile ion gettering capability of BPSG during bias-temperature aging,

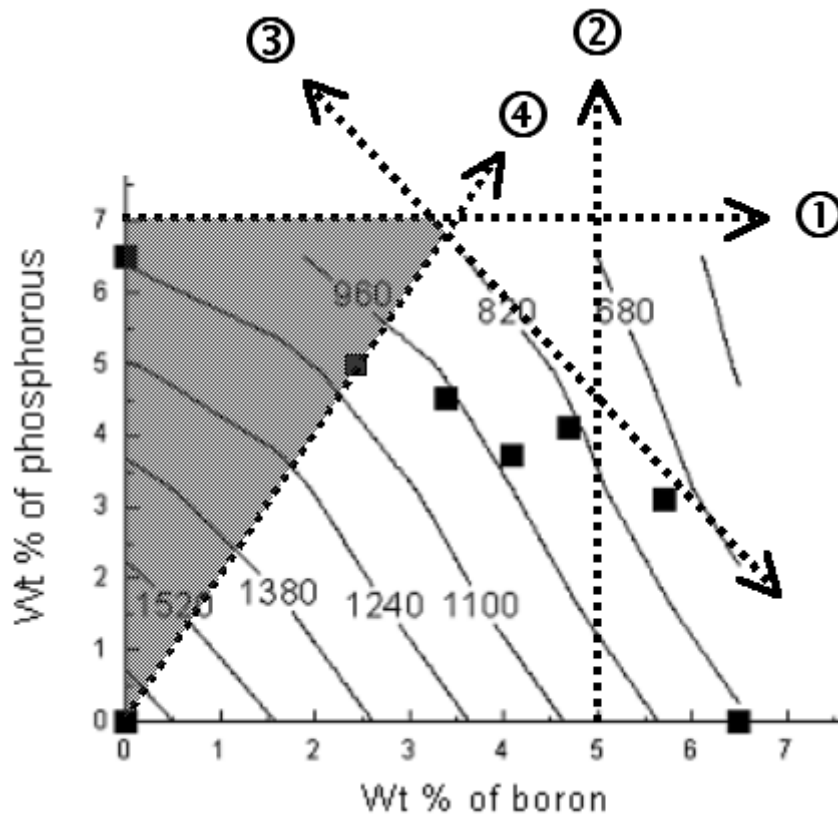


Figure 2.23: BPSG flow temperature contours (Fig. 2.21) including the four constraints, showing acceptable B and P wt percentages to form a problem-free BPSG

the same number of net P₂O₅ as in 200 Å thick 4 wt % PSG, must be realized in 6,000 Å thick BPSG as well. The required net P wt % for the 6,000 Å thick BPSG is determined by solving:

$$200 \text{ (Å)} \times 4 \text{ (wt \%)} = 6,000 \text{ (Å)} \times \text{net P (wt \%)}.$$

From this equation, the required net P wt % for the 6,000 Å thick BPSG is calculated as 0.13 wt %, and the above mentioned inequality then becomes:

$$[\text{P wt \%} - 2 \text{ (B wt \%)}] > 0.13$$

Constraint 4: $[\text{P wt \%} - 2 \text{ (B wt \%)}] > 0.13$, To Ensure Mobile Ion Gettering Capability

Figure 2.23 shows the BPSG flow temperature contours (shown in Fig. 2.22 for 30 min tube furnace heat treatment in dry N₂ at 1 atm pressure) including the four constraints discussed above. While the fourth constraint (for mobile gettering threshold) is specific for 6,000 Å thick BPSG, the rest of the constraints are valid for any BPSG film thickness. Although the fourth constraint is specific for 6,000 Å thick BPSG, the constraint is valid for practical ILD thicknesses used today, which are within few thousand Å of the 6,000 Å value. A ± 1,000 Å difference in ILD thickness will result in a ± 0.03 change in the value of the right-hand side of the fourth constraint. Acceptable B and P wt % combinations to form a problem-free BPSG can be selected from the shaded region of Fig. 2.23. By examining Fig. 2.23, the 3 % PSG is within the problem-free region, which unfortunately contradicts with the V_{TH} and BV instability results previously observed in the SiC DMOSFETs. It was reported that a P wt % of 4 in 200 Å

thick gate PSG can stabilize V_{TH} from bias-temperature aging [49] as long as the mobile ion density is less than $1 \times 10^{10} \text{ cm}^{-2}$. As V_{TH} and BV instability measurements in this thesis work revealed, the mobile ions of $\sim 4 \times 10^{12} \text{ cm}^{-2}$ exist in the SiC DMOSFET used in this work. To capture more mobile ions, P concentration can be increased up to 7 wt % before the film becomes hygroscopic. If the efficiency of capturing mobile ions is directly proportional to the P concentration in the 200 Å thick PSG, then a 200 Å, 7 wt % PSG can capture 1.75 times more mobile ions than the 200 Å thick 4 wt % PSG, which comes to a value of $1.75 \times 10^{10} \text{ cm}^{-2}$. A 6000 Å thick 7 wt % PSG can capture 30 times more mobile ions than the 200 Å thick 7 wt % PSG. This comes to about $5.25 \times 10^{11} \text{ cm}^{-2}$, which is approximately 10 times lower than the density of mobile ions measured in the SiC DMOSFET of this study ($\sim 4 \times 10^{12} \text{ cm}^{-2}$). Therefore, the source of the mobile ions existing in the DMOSFET needs to be clarified and the density of the mobile ion needs to be reduced down to the qualified MOS process level of $1 \times 10^{10} \text{ cm}^{-2}$, otherwise, none of the BPSG with any B and P wt % combinations selected within the problem-free region will satisfy the mobile ion gettering requirement. From this point on, let us assume that the density of mobile ions are successfully reduced down to the qualified MOS process level of $1 \times 10^{10} \text{ cm}^{-2}$. The commercially used 2.4 wt % B and 5 wt % P BPSG is found to be within the problem-free region and flows at 1,050 °C for a 30 min treatment in N_2 ambient at 1 atm pressure. Though, both the 7 % PSG and the 2.4 wt % B and 5 wt % P BPSG are problem-free ILDs, since the 2.4 wt % B and 5 wt % P BPSG flows at a lower temperature, the BPSG should be implemented next time when the DMOSFET is fabricated.

Before going into the details of the flow process for the optimized BPSG film, there are some other problems associated with high concentration of B and P in BPSG, which deserve attention. Another problem with high boron and phosphorus concentrations in the BPSG film is the possible polarization. Originally, PSG films were introduced in the MOS structures to stabilize the threshold voltage by gettering the mobile ions, but the polarizing nature of the film causes threshold voltage instabilities [40-42]. Boro-silicate glass (BSG) is also known to be polarizable as seen in its common usage for sunglasses, therefore, it is expected that the BPSG is also polarizable. However, the threshold voltage instability due to the polarization effect of BPSG has not been reported, because the BPSG has not been used as a gate dielectric. Therefore, it is not straightforward to predict the degree of polarization of a thick BPSG ILD film with the polarization data available in the literature for a thin PSG gate dielectric film. It is believed that an excessive usage of both B and P may result in polarization causing a shift in electrical behavior (ex.: threshold and breakdown voltages). The BPSG film can also be an unintended diffusion source of the B and P impurities for the underlying substrate (i.e. Si). It has been found that the BPSG is primarily a source of phosphorus, and the phosphorus out-diffusion from the film into the substrate is increased at a higher boron concentration [35]. Although, any dopants hardly diffuse into SiC, the minimum necessary amounts of B and P, for achieving a desired glass flow temperature, should be used.

Up to this point, the material aspects of BPSG with regard to reducing flow temperature were discussed. Further research to see if the viscous glass flow process can

be achieved at an even lower temperature than the 1,050 °C and over a shorter time period than the 30 min (for the 2.4 wt % B and 5 wt % P BPSG) was performed. According to Tong et al., a heat treatment in steam ambient (instead of N₂ ambient) at 1 atm of pressure allows for a reduction in the BPSG flow temperature by about 70 °C [50]. It is estimated that the flow temperature may be reduced even further by approximately 60 °C, if the BPSG were flowed in a high-pressure oxidation system at 10 atm pressure of water vapor [51]. Time can be traded for temperature, as it has been reported that a rapid thermal annealing (RTA) for 30 sec, at a temperature 100-175 °C higher than that used in a conventional furnace annealing, will result in an equivalent BPSG flow [48]. However, the RTA could affect the performance of MOS capacitors [52-56]. An anomalous threshold voltage shift due to strain resulting from the high temperature ramp rate of RTA was observed [52-56], but a post furnace annealing (900°C/40 min) can remove the RTA induced strain [57, 58].

Glass flow is a gradual and continuous process, which may depend on the prior thermal history of the glass film. A thermal treatment at a temperature below the flow temperature of the glass may have an additive effect, increasing the degree of flow during the actual flow step [35, 36]. For this reason, ILD flow processes are commonly performed twice in device manufacturing [35, 36]. The first thermal treatment is referred to as *densification* and is performed immediately after the ILD deposition. The second thermal treatment is referred to as *contact reflow* and is usually performed after the contact metal etch. After anisotropic etching of the ILD, the contact vias have sharp upper corners, which makes step coverage difficult during the subsequent metal

depositions. Therefore, the contact reflow is done to round these sharp edges, which improves the step coverage. The densification is frequently performed in steam, whereas the contact reflow is done in nitrogen to avoid oxidation of the exposed contacts [35, 36]. Hsieh et al. reported superiority of the RTA anneal over the furnace anneal in improving the contact resistance attributed to the less oxidation of contact window during annealing [58].

The ILD process used in this study for the SiC DMOSFETs went through two high temperature steps; an ILD densification anneal at 925 °C for 30 min, performed after the ILD deposition, and an RTA contact anneal at 1,050 °C for 3 min, performed after the source metallization, both in N₂ ambient. As mentioned earlier, the 925 °C anneal temperature for 3 wt % P PSG is too low compared to the required 1,450 °C for proper flow (see Fig. 2.21 or Fig. 2.23). Although the second high temperature process is intended for source contact (Ni-SiC) anneal, it would have been beneficial for the PSG flow if the temperature were near the PSG flow temperature. In this case, the contact anneal performed at 1,050 °C was not close to the 1,450 °C required for the glass flow of 3 wt % P PSG film (see Fig. 2.21 or Fig. 2.23).

As mentioned earlier both boron and phosphorus out-diffuse during a high temperature process [38]. All B₂O₃ in the BPSG film, independent of their location in the film, are subject to out-diffusion. The amount of B₂O₃ out-diffusion is large in steam, and is comparatively small in O₂ and N₂ ambients. In the case of P₂O₅, only the ones close to the film surface diffuse out, and the amount of P₂O₅ out-diffusion is low in O₂ and high in N₂ and steam ambients. Therefore, the B and P wt percentages must be adjusted in as-

deposited BPSG accordingly so that the post-flow BPSG satisfies the mobile ion gettering constraint: $[P \text{ wt \%} - 2 (B \text{ wt \%})] > 0.13$ (Constraint 4).

2.4. Conclusion

At low temperatures, the threshold voltage and drain current instability during the positive-stress can be attributed to the capture of electrons by the SiC/gate dielectric interface traps and/or near interface gate dielectric traps. The captured electrons are released during the negative-stress. Prolonged positive-stress results in the capture of more electrons, causing a larger V_{TH} increase, but the negative-stress of the same duration as the positive-stress releases the captured electrons fully, offsetting the increase in V_{TH} . However, this hypothesis fails to explain the I_{DS} transient behavior at elevated temperatures, where an additional gate dielectric mobile ionic charge effect appears causing a decrease in the threshold voltage and an increase in drain current transient with an increasing positive-stress time. This negative threshold voltage shift effect is more pronounced at high device operating temperatures. According to this study, the 4H-SiC DMOSFET suffers unstable device operation due to a positive or a negative threshold voltage shift during the positive-stress. The polarity and magnitude of the threshold voltage shift depends on the device operating temperature and the stress duration. As shown in the 30 °C stress tests the negative-stress is very effective in releasing the interface and near interface trap captured electrons; but as shown in the 130 °C stress tests it is not as effective in offsetting the effects of mobile positive ion gate oxide charges. The positive charges may be contaminants from the molybdenum gate metal or

may be hydrogen ions from device passivation film of silicon nitride. Verification of the exact sources of the thermally activated ionic charges needs further investigation.

The two signature characteristics of the high-temperature off-state voltage stress on DMOSFET devices are: (1) a slump in breakdown voltage and (2) the recovery of the breakdown voltage logarithmically with time in the avalanche region. A nominal variation in measured BV-slump is observed for DMOSFETs of different JFET region widths. The BV-slump and recovery are also observed in ungated p-well/n⁻-drift layer diode structures, which are similar to the JTE structure of the DMOSFETs. Computer simulation suggested that the BV-slump in the DMOSFETs and the diodes is caused almost exclusively by the SiC/field oxide interface charges in the JTE structure. Simulation results also indicated that the typical 150 V of measured BV-slump for the DMOSFETs and the diodes is caused by $\sim 4 \times 10^{12} \text{ cm}^{-2}$ of interface charges. It was found that the location of the charge within the SiC/field oxide interface in the JTE structure plays an important role in determining the magnitude of the BV-slump. The most vulnerable location for the interface charge to affect the BV-slump is around the inner edge of the JTE region, and the possibility of interface charge accumulation around the inner edge of the JTE region during the bias stress was suggested by the directionality of the electric field in the JTE structure. Because the BV instability is negligible at the room temperature and is detectable only at a high temperature, as in case of V_{TH} instability of DMOSFET, positive mobile ionic charges are the most plausible cause for BV instability as well. Unfortunately, the exact sources of the thermally activated ionic

charges, which are responsible both for the DMOSFETs' V_{TH} and BV instabilities, are unknown at this time, and deserve further investigation.

One of the solutions to suppress the V_{TH} and BV instabilities of DMOSFET is to realize a high quality ILD, which getters the mobile positive ionic charges. The search for appropriate ILD is directed at addressing the SiC DMOSFETs' V_{TH} and BV instability problems and step coverage problem, while considering factors such as: hygroscopic nature of the film, crystalline BPO_4 particle formation on the surface of the BPSG film, possible polarization; which may become important at high B and P concentrations. In this work, BPSG flow temperature contours for different B and P concentrations were developed and the problem-free region of the contours to avoid the above mentioned problems were identified. Based on this knowledge, it is possible to select appropriate B and P concentrations in the BPSG film for a particular glass flow temperature.

The 3 wt % PSG used for the SiC DMOSFETs of this work isn't optimum because the heat treatment temperature of 925 °C used for this device is not high enough to flow the glass. Although, the P concentration of 3 wt % is found to be within the problem-free region, such PSG film is not capable of suppressing the uncontrollably large density of mobile ions existing in the DMOSFET devices, as demonstrated by the V_{TH} and BV instability measurements. Unfortunately, none of the BPSG with any B and P wt % combinations selected within the problem-free region will solve the V_{TH} and BV instability problems in the SiC DMOSFET of this work, due to the uncontrollably large density of mobile ions. Assuming the density of mobile ions are successfully reduced down to the qualified MOS process level in near future, the 2.4 wt % B and 5 wt % P

BPSG should be implemented the next time the DMOSFET is fabricated, because it flows at a low temperature.

In order to improve the step coverage of the 2.4 wt % B and 5 wt % P BPSG for the SiC DMOSFET which will be fabricated in the future work, first of all, the molybdenum gate metal thickness should be reduced from the present 0.6 μm to a new 0.2 μm , because, for the same ILD thickness the thinner gate metal will result in a smaller step coverage angle. In addition, if the molybdenum gate metal is confirmed to be one of the sources for the mobile ions, its deposition amount, or its height, must be decreased to reduce the total number of mobile ions. For densification, present furnace anneal of 925 $^{\circ}\text{C}$ for 30 min in N_2 is satisfactory. For contact reflow, a 30 sec RTA step at a temperature, which is 100-175 $^{\circ}\text{C}$ higher than the 2.4 wt % B and 5 wt % P BPSG's flow temperature of 1,050 $^{\circ}\text{C}$, for 30 min in N_2 is suggested [48]. The contact reflow may be followed by a furnace treatment at 900 $^{\circ}\text{C}$ for 40 min in N_2 to remove the RTA induced strain [57, 58]. If high temperature or long duration processes, as suggested above are not possible, the B and P compositions may be increased up to 3 wt % and 6 wt %, respectively, maintaining the mobile ion gettering constraint of $[\text{P wt \%} - 2 (\text{B wt \%})] > 0.13$, in the post-flow BPSG film. This composition reduces the required glass flow temperature and time.

3. Characteristics of GaN HEMT devices

3.1. Introduction

At present, GaAs pHEMTs are widely used for microwave power applications [5-10]. As standard pHEMTs approach their theoretical power limits [11], new device technologies capable of high-voltage and high-power operation are required [12-15]. The GaN based HEMTs made on SiC substrates have the potential to replace GaAs-based HEMTs for a number of high-power applications at high-frequencies, due to a high saturation velocity (2.7×10^7 cm/s vs. 1×10^7 cm/s) and a high breakdown voltage (3 MV/cm vs. 0.4 MV/cm) of GaN and a high thermal conductivity (4.9 W/cm-K vs. 0.5 W/cm-K) of the SiC substrate [16-18].

In this work, a series of source/load-pull measurements and single-tone and two-tone power measurements have been carried out on GaN HEMTs and GaAs pHEMTs under different biasing conditions (Class A, AB, and B). Based on the results of these measurements, the biasing and tuning conditions, which maximize output power, efficiency, and linearity, have been determined. These measurements were performed on GaN and GaAs devices with different gate widths. Output power, efficiency, and linearity performance comparison between GaN HEMT and GaAs pHEMT is made for devices with similar DC power levels.

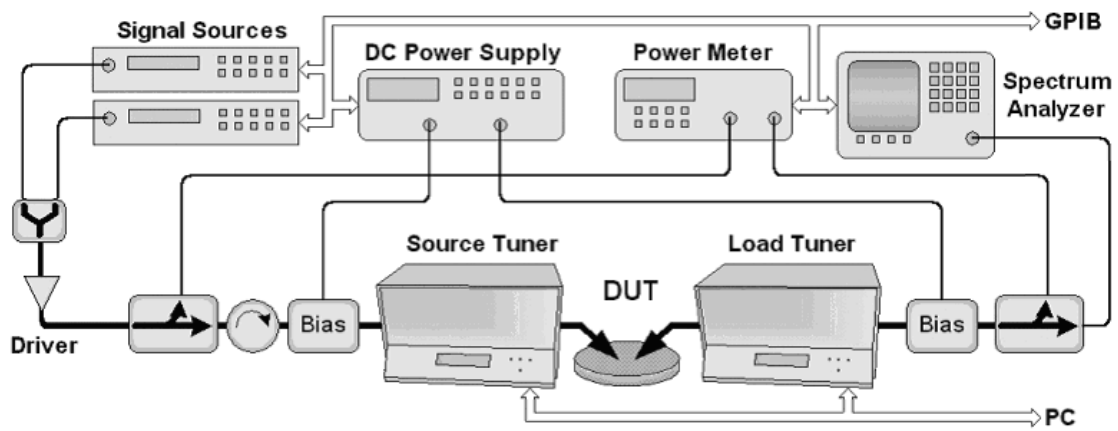


Figure 3.1: Schematic of source/load-pull measurement setup

3.2. Experiment

The GaN HEMTs examined in this study were grown by metal organic chemical vapor deposition (MOCVD) on semi-insulating SiC substrates. The gate lengths were 0.5 μm and the gate widths were 300 and 500 μm . The gate metal was Ni/Au and the ohmic contact metal was Ti/Al/Ni/Au. The GaAs devices were field plate based pHEMTs with gate lengths of 0.3 μm and total gate widths of 500, 700 and 900 μm . The gate metal for the GaAs pHEMTs was Ti/Pt/Au and the ohmic contact metal was Au/Ge/Ni. Cross-sectional views of the GaAs pHEMTs and the GaN HEMTs are shown in Figures 1.5(a) and 1.5(b), respectively.

A Focus Microwaves on-wafer source/load-pull measurement system capable of single-tone and two-tone excitation at frequencies between 0.8 and 18 GHz was used for the measurements in this work. With this system, DC bias control, RF excitation, source and load tuner positioning, and data acquisition were all under computer control. The required passive components such as probes, combiner, bias tees, isolator, and attenuators, are all covering the frequency range of interest. The schematic of the measurement setup is given in Fig. 3.1.

A series of single-tone measurement (to evaluate efficiency performance) and two-tone power measurement (to evaluate linearity performance) were performed on several GaN and GaAs devices under different DC bias conditions and different input/output impedance matching conditions in order to investigate output power, efficiency, and linearity performances of GaN HEMTs and GaAs pHEMTs as functions of bias and input/output impedance matching conditions.

Efficiency is evaluated in terms of power-added-efficiency (PAE) and linearity was evaluated in terms of third-order intercept point (IP3) or carrier to intermodulation ratio (C/I) at null. In a single-tone measurement, output power (P_{out}) in decibel milliwatts (dBm) and drain current (I_{DS}) in amps are recorded for different input power (P_{in}) levels in dBm and fixed drain voltage (V_{DS}) in volts. Power-added-efficiency (PAE) is calculated in terms of P_{out} in watts, P_{in} in watts, and DC power dissipation (product of DC drain-source voltage V_{DS} and drain-source current I_{DS}) in watts as:

$$PAE (\%) = \frac{P_{out} (W) - P_{in} (W)}{V_{DS} (V) \times I_{DS} (A)} \times 100.$$

In a two-tone measurement, output power at one of the fundamental frequencies ($P_{out, f1}$) in dBm and one of the third-order intermodulation distortion product (IM3) in dBm are recorded for different input power levels at one of the fundamental frequencies ($P_{in, f1}$) in dBm. Third-order intercept point (IP3) is calculated in terms of $P_{out, f1}$ and IM3 at a low input power level, where both $P_{out, f1}$ and IM3 are linear, as:

$$IP3 (dBm) = \frac{3 \times P_{out, f1} (dBm) - IM3 (dBm)}{2}.$$

For comparison among different gate width devices, a linearity figure of merit (LFOM) is defined as the ratio of IP3 to DC power dissipation. Carrier to intermodulation ratio (C/I) is defined as a dB separation between $P_{out, f1}$ and IM3. The C/I at null, where the IM3 curvature changes, is used as a linearity figure when the device is compressed even at a low input power level. In this case, both $P_{out, f1}$ and IM3 are nonlinear and IP3 extraction is not possible (i.e. Class B biased device). The IP3 or C/I enables specifying IM3 performance: the higher the IP3 or C/I, the lower the IM3 in the output, and better the

linearity. Detailed definitions for linearity performance parameters including IM3, IP3, LFOM, and C/I at null are given in Appendix A.

In this work, input/output impedance matching technique is fully developed for both GaN and GaAs devices. In the source/load-pull measurement, which is normally performed with a single-tone input signal, the source/load impedance seen by the input/output of device is varied to other than 50Ω value in order to seek maximum output power (P_{out}). In this work, Microsoft Excel Macro application is developed to calculate PAE from the recorded single-tone performance parameters (P_{out} , V_{DS} , and I_{DS}) as the source/load impedance is varied across the Smith chart. As a result, source/load impedance can be tuned not only for P_{out} , but also for optimum PAE. The source/load-pull measurements were also performed with two-tone input signal. Similarly, IP3 or C/I, is calculated from the recorded two-tone performance parameters ($P_{out,fl}$ and IM3), enabling one to tune source/load impedance for optimum IP3 or C/I, as well. The necessity of impedance matching for high-frequency measurements is explained in detail in Appendix B.

Single-tone power measurements were performed at 4.000 GHz, and two-tone power measurements were performed with tones at 4.000 and 4.001 GHz. All GaN HEMTs were biased at a fixed V_{DS} of 25 V and all GaAs pHEMTs were biased at a fixed V_{DS} of 15 V. The V_{DS} values for the two devices were selected in order to obtain optimum output power and linearity performances from each device and to limit excessive power dissipation. The gate voltages (V_{GS}) were adjusted for drain current: $I_{DS} = 0.7 I_{DSS}$ (which is drain-source current with zero applied gate voltage) for Class A,

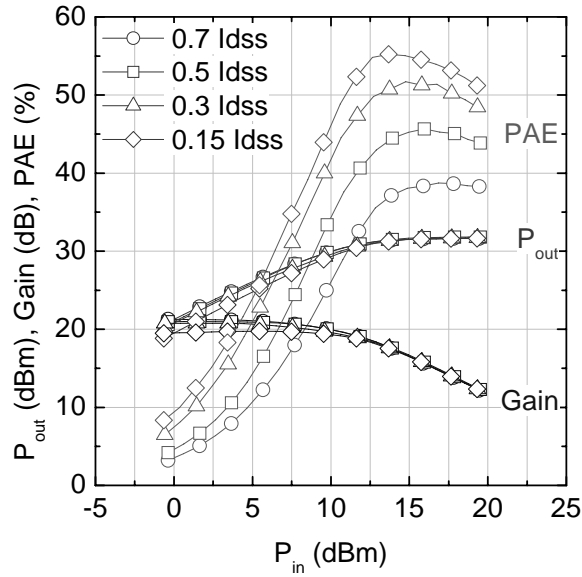


Figure 3.2: Bias effect on single-tone power performance of 300 μm GaN HEMT

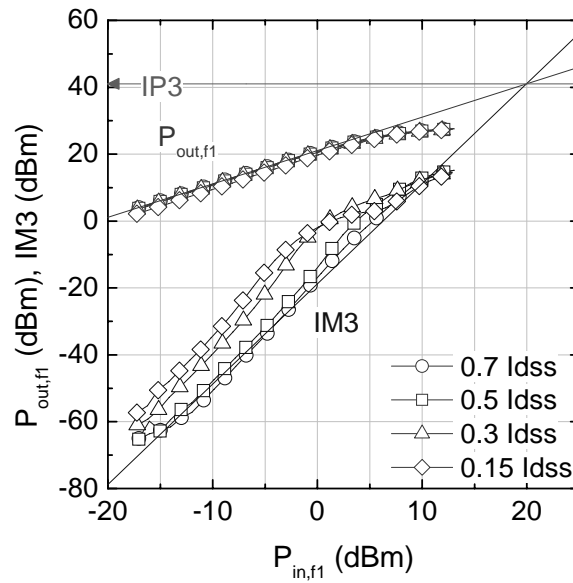


Figure 3.3: Bias effect on two-tone power performance of 300 μm GaN HEMT

$I_{DS} = 0.15 I_{DSS}$ for Class AB, and $I_{DS} = 0$ for Class B, for both GaN and GaAs devices. For each bias condition, single-tone and two-tone power measurements were performed, and the effect of bias condition on P_{out} , PAE, and linearity (IP3 or C/I) performances was studied. In order to further improve PAE and/or linearity (IP3 or C/I) performance, source/load pull measurements were performed, and source/load impedances for optimum PAE and optimum linearity (IP3 or C/I) were determined. Finally, power measurements were performed to study effects of optimum impedance conditions on the P_{out} , PAE, and linearity (IP3 or C/I) performances of the device.

3.3.Results and Discussion

3.3.1. Source/load pull and power measurements on 300 μm width GaN HEMT:

Keeping the drain voltage of 300 μm gate width GaN HEMTs at 25 V, gate voltage is adjusted to set drain-source current (I_{DS}) at 70, 50, 30, and 15 % of drain-source current with zero applied gate voltage (I_{DSS}). For each bias condition, both devices' input and output were power matched with fixed input power level at 15 dBm. Then, power measurements were performed. Variation of P_{out} , Gain, and PAE with P_{in} for single-tone operation and variation of $P_{out, f1}$ and $IM3_{2f1-f2}$ with $P_{in, f1}$ for two-tone operation are shown in Figures 3.2 and 3.3, respectively, for various bias conditions. As the bias current decreased from $0.7 I_{DSS}$ (Class A) to $0.15 I_{DSS}$ (Class AB), the peak PAE increased from 38.7 % to 55.2%, where as the IP3 decreased (not directly shown) from 41.0 dBm to 31.8 dBm. The PAE and IP3 values obtained for the $0.5 I_{DSS}$ and $0.3 I_{DSS}$

Table 3.1: Biasing conditions used for 300 μm GaN HEMT device

V_{GS}	V_{DS}	I_{DS}
-1.1 V	25 V	0.7 I_{DSS} (Class A)
-3.4 V	25 V	0.15 I_{DSS} (Class AB)
-4.1 V	25 V	0 (Class B)

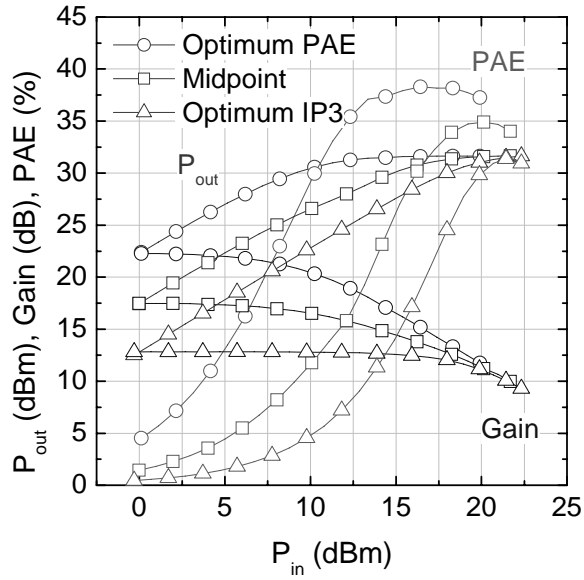


Figure 3.4: Single-tone power measurements on Class A biased 300 μm GaN HEMT when input is PAE or IP3 matched

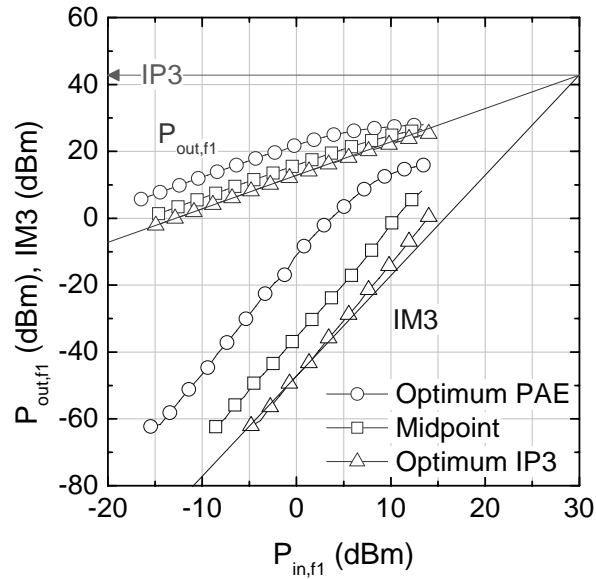


Figure 3.5: Two-tone power measurements on Class A biased 300 μm GaN HEMT when input is PAE or IP3 matched

bias currents are 45.6%, 40.0 dBm and 51.7%, 36.2 dBm, respectively. The direct tradeoff observed between efficiency and linearity is expected for a change in bias condition from Class A to Class AB [59, 60]. Though, at low P_{in} level, P_{out} , Gain, and IM3 performances are bias condition dependent, they converge at large P_{in} levels regardless of bias condition.

After studying the bias effect on efficiency and linearity, source-pull and then power measurements were performed on 300 μ m GaN HEMT for further evaluation of three bias conditions (0.7 I_{DSS} for Class A, 0.15 I_{DSS} for Class AB, and 0 for Class B). Bias conditions used to obtain the bias configurations are listed in Table 3.1.

For Class A bias condition, variation of P_{out} , Gain, and PAE with P_{in} for single-tone operation and variation of $P_{out, fl}$ and IM3 with $P_{in, fl}$ for two-tone operation are shown in Figures 3.4 and 3.5, respectively, at three different source impedance values including those corresponding to the optimum PAE and optimum IP3. The third impedance point marked as “midpoint” in Figures 3.4 and 3.5 corresponds to the source impedance where intermediate PAE and IP3 values are achieved. For Class A bias condition, the source tuning from the optimum PAE to the optimum IP3 resulted in a shift in the PAE peak towards higher P_{in} values (Fig. 3.4) and an increase/decrease in the IP3/IM3 value (Fig. 3.5). Though, a 11.0 dB (from 31.8 to 42.8 dBm) improvement in IP3 by source tuning is achieved, PAE is sacrificed from 38.4 % to 31.4 %, which indicates that the source tuning is not effective for Class A bias condition.

For Class AB bias condition, variation of P_{out} , Gain, and PAE with P_{in} for single-tone operation and variation of $P_{out, fl}$ and IM3 with $P_{in, fl}$ for two-tone operation are

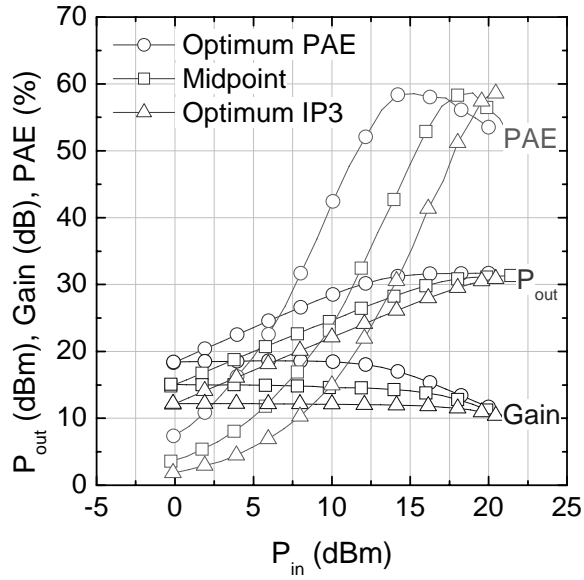


Figure 3.6: Single-tone power measurements on Class AB biased 300 μm GaN HEMT when input is PAE or IP3 matched

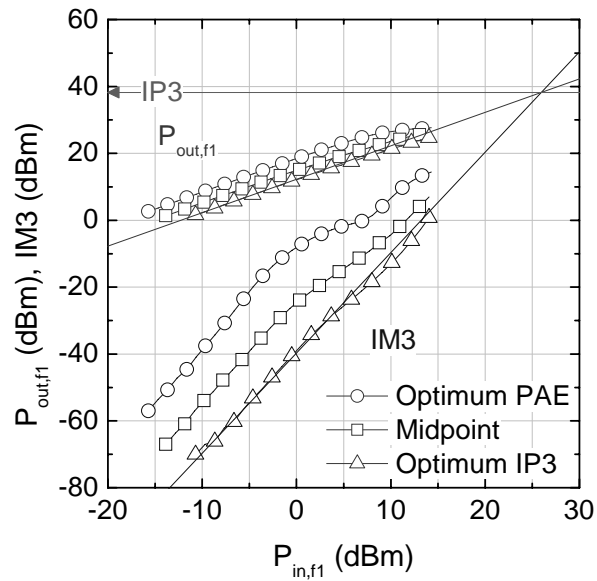


Figure 3.7: Two-tone power measurements on Class AB biased 300 μm GaN HEMT when input is PAE or IP3 matched

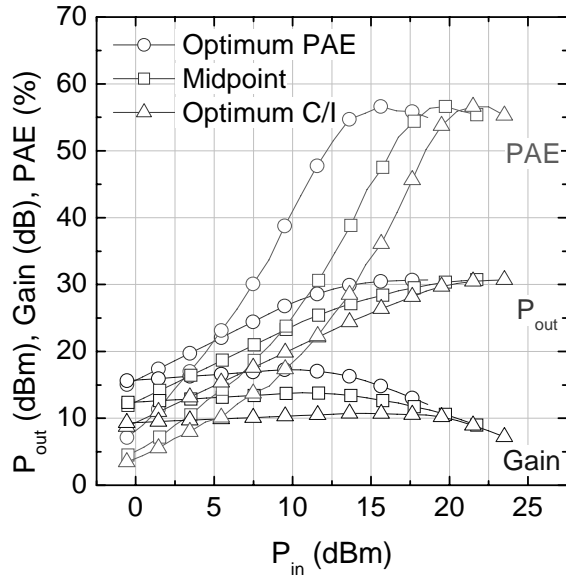


Figure 3.8: Single-tone power measurements on Class B biased 300 μm GaN HEMT when input is PAE or IP3 matched

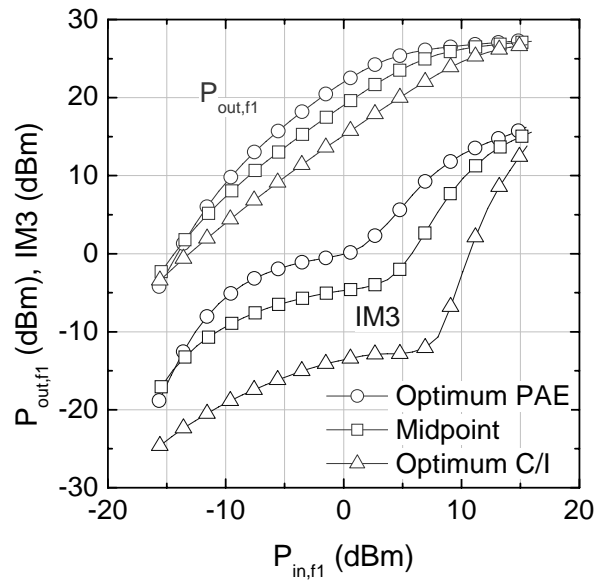


Figure 3.9: Two-tone power measurements on Class B biased 300 μm GaN HEMT when input is PAE or IP3 matched

shown in Figures 3.6 and 3.7, respectively, at three different source impedance values, including those corresponding to the optimum PAE and optimum IP3. As in case of Class A, for Class AB bias also, the source tuning from the optimum PAE to the optimum IP3 resulted in a shift in the PAE peak towards higher P_{in} values (Fig. 3.6) and a increase/decrease in IP3/IM3 value (Fig. 3.7). However, unlike in case of Class A, the peak PAE value stayed almost constant in the peak shift. All single-tone power measurement performance quantities become smaller at low input power level as source impedance is varied from PAE to IP3; however, at high input power level, P_{out} and Gain become comparable and PAE is greatly improved (Fig. 3.6). The IP3 measured for IP3-matched source impedance is 38.2 dBm, which is significantly better than 32.4 dBm obtained for PAE-matched source impedance. Results of Figures 3.6 and 3.7 convey that source tuning from PAE to IP3 for Class AB bias is effective in improving IP3 without sacrificing PAE and P_{out} .

For Class B bias condition, variation of P_{out} , Gain, and PAE with P_{in} for single-tone operation and variation of $P_{out, f1}$ and IM3 with $P_{in, f1}$ for two-tone operation are shown in Figures 3.8 and 3.9, respectively, at three different source impedance values including those corresponding to the optimum PAE and optimum linearity figure, carrier to intermodulation ratio (C/I) at null. As discussed earlier, IP3 extraction was not possible for Class B bias condition, and thus the linearity is measured instead by C/I at null. As in cases of Classes A and AB, for Class B bias also, the source tuning from the optimum PAE to the optimum C/I resulted in a shift in the PAE peak towards higher P_{in} values (Fig. 3.8), and a decrease in IM3 value. As in case of Class AB, for Class B bias also, the

source tuning improved linearity significantly without compromising maximum PAE (~58 %). The C/I at null improved from 22.5 dB to 34.1 dB as the source impedance is tuned from optimum PAE to optimum C/I (Fig. 3.9).

Source tuning on differently biased 300 μm GaN HEMT revealed the following. Regardless of source impedance value, P_{out} , Gain, $P_{\text{out,fl}}$ and IM3 converged at high input power levels. The peak PAE shifted toward higher P_{in} as source impedance is varied from optimum PAE to optimum linearity (IP3 or C/I). In Class A bias condition, the peak PAE decreases, whereas the peak PAE holds its maximum value in Class AB and Class B bias conditions. The 300 μm GaN HEMT when biased in Class AB exhibited a higher PAE and a lower IP3 than it was biased in Class A. However, the source tuning for IP3 on Class AB biased HEMT resulted in a comparable IP3 (with Class A) without sacrificing maximum achievable PAE. The increase in IP3 by source tuning for Class A biased GaN HEMT is only marginal at a cost of substantial decrease in PAE. The source tuning for optimum C/I on Class B biased device resulted in a great improvement in C/I at null, without sacrificing maximum achievable PAE. Hence, the source tuning for linearity improvement is effective for Class AB and Class B biased GaN HEMT devices.

After resetting the source impedance to the P_{out} matching value, the load-pull and then power measurements were performed on the 300 μm GaN HEMT biased under the same three conditions (as given in Table 3.1). For Class A bias condition, load impedances for optimum PAE and optimum IP3 are close to each other. Thus, associated P_{out} , Gain, PAE, IM3 and IP3 for these two output impedances are similar. The transistor output matched for optimum PAE exhibited a maximum PAE of 41.9 % and an optimum

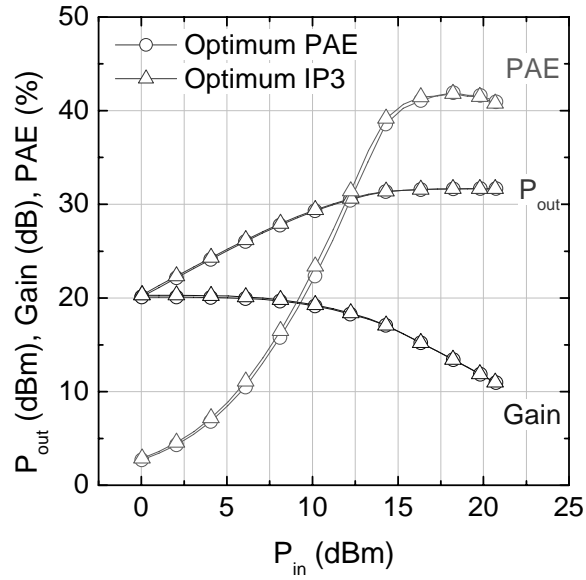


Figure 3.10: Single-tone power measurements on Class A biased 300 μm GaN HEMT when output is PAE or IP3 matched

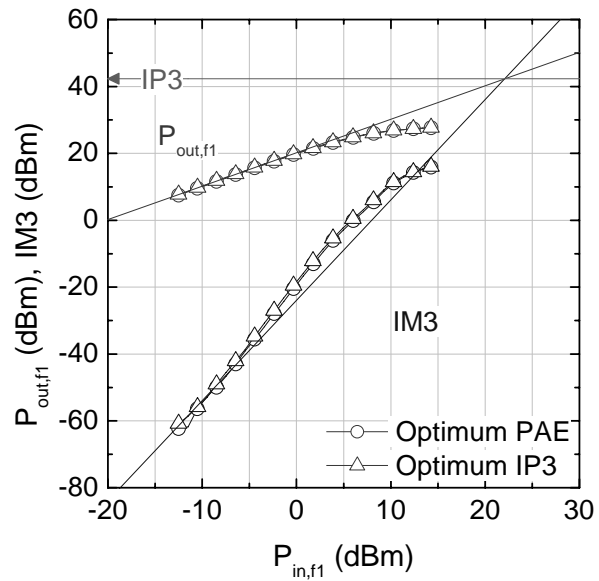


Figure 3.11: Two-tone power measurements on Class A biased 300 μm GaN HEMT when output is PAE or IP3 matched

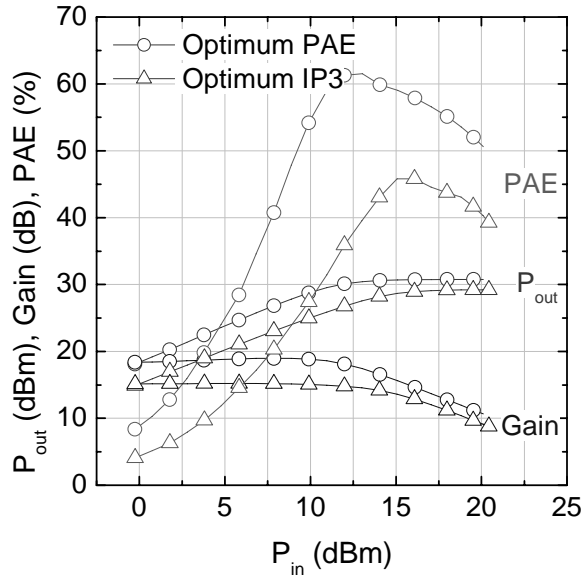


Figure 3.12: Single-tone power measurements on Class AB biased 300 μm GaN HEMT when output is PAE or IP3 matched

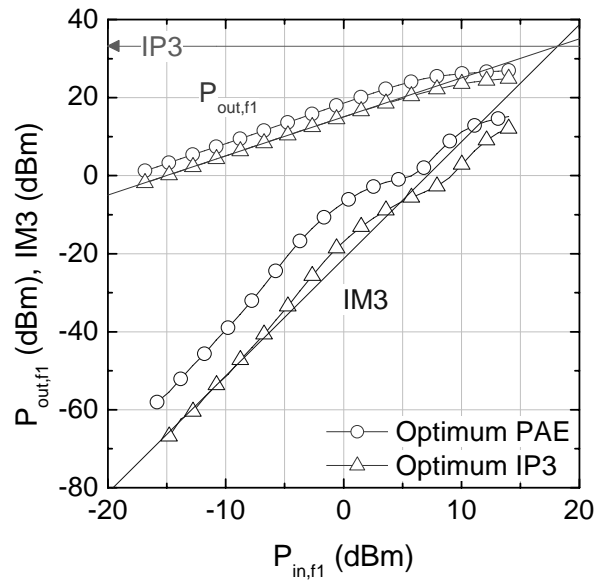


Figure 3.13: Two-tone power measurements on Class AB biased 300 μm GaN HEMT when output is PAE or IP3 matched

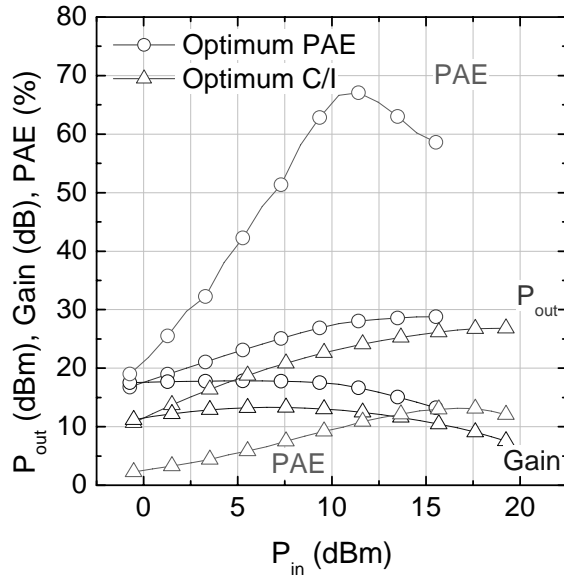


Figure 3.14: Single-tone power measurements on Class B biased 300 μm GaN HEMT when output is PAE or C/I matched

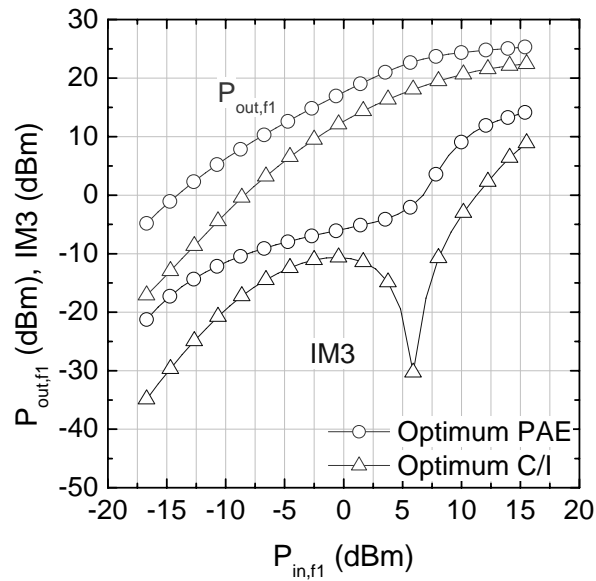


Figure 3.15: Two-tone power measurements on Class B biased 300 μm GaN HEMT when output is PAE or C/I matched

IP3 of 42.0 dBm, and the transistor output matched for optimum IP3 exhibited a maximum PAE of 41.8 % and an IP3 of 42.3 dBm (see Figures 3.10 and 3.11). The closeness of these results suggests that the load tuning is unnecessary for Class A operation of this device. For Class AB bias condition, the transistor output matched for PAE exhibited a maximum PAE of 61.5 % and an IP3 of 32.4 dBm, and the transistor output matched for IP3 exhibited a maximum PAE of 45.8 % and an IP3 of 33.2 dBm (see Figures 3.12 and 3.13). Load tuning for Class AB achieved a 0.8 dB increase in IP3, which is marginal at an expense of substantial sacrifice in PAE (61 % to 45 %). For Class B bias condition, the transistor output matched for optimum PAE exhibited a maximum PAE of 67.1 % and a C/I at null of 25.1 dB; and the transistor output matched for optimum C/I exhibited a maximum PAE of 13.2 % and a C/I at null of 43.5 dB (see Figures 3.14 and 3.15). Load tuning for C/I resulted in a 18.4 dB increase in C/I at null, sacrificing PAE by substantial amount (from 67.1 % to 13.2 %).

Load tuning for IP3 or C/I (at impedances away from optimum PAE) decreases all power performance parameters (P_{out} , Gain, PAE, $P_{out,fl}$, and IM3) even at high input power levels. This phenomenon is not prominent in Class A biased device, because the impedances for the optimum PAE and optimum IP3 are close to each other. For Class AB, the load tuning made a marginal improvement in IP3 at a cost of a substantial decrease in PAE. For Class B, though a great improvement in C/I at null is achieved, a large decrease in PAE is observed for load tuning. Hence, the load tuning is ineffective for all bias conditions.

Observations on differently biased 300 μm GaN HEMT are the following. The transistors biased in Class A possess a higher IP3 with respect to Class AB and Class B. For Class A, source tuning to gain more IP3 decreases PAE, and load impedance for optimum IP3 is similar to that of optimum PAE. Hence, both source and load tuning are not advantageous for Class A bias condition. Source tuning for Class AB biased transistor increases IP3 without sacrificing PAE. Load tuning in Class AB has only a marginal effect on IP3 with a substantial drop in PAE. Hence, load tuning is not advisable for Class AB. For Class B biased transistor, source tuning increases C/I without sacrificing PAE. Load tuning yields a substantial increase in C/I at null, but at a cost of large decrease in PAE. Hence, the load tuning isn't desirable for Class B bias condition as well. For all these bias configurations, the load tuning is not effective in improving linearity without a substantial decrease in PAE. Thus, the load impedance must be left at power matched condition to ensure the optimum power performance of the 300 μm gate width GaN HEMTs. The source tuning is effective for Class AB and Class B biased GaN HEMTs in improving linearity.

3.3.2. Source/load pull and power measurements on 500 μm width GaN HEMT:

The general source/load tuning effects on power performance of the 500 μm GaN HEMT is similar to that of the 300 μm device at all bias conditions. The source tuning resulted in a great improvement in IP3 without sacrificing maximum achievable PAE in Class AB configuration for both the devices. For Class A, the increase in IP3 is marginal

with a substantial decrease in PAE for both the devices, especially for the 500 μm GaN HEMT device. Based on these results, the Class AB is a better bias configuration compared to the Class A, with respect to source tuning irrespective of the device width.

The load tuning effects observed for both the 300 μm and the 500 μm GaN HEMT devices is similar as well. For all these bias configurations, the load tuning is not effective in improving linearity of the device without a substantial decrease in P_{out} and PAE for any bias condition. The power performance of both 300 and 500 μm gate width GaN HEMTs is at its optimum when the load impedance is power matched, and the source impedance is IP3 matched (for Class AB and Class B).

In this study, for the GaN devices, a higher IP3 value is observed for the bigger device. The LFOM ($= \text{IP3}/P_{\text{DC}}$) is smaller (4.29 for the 500 μm device vs. 8.05 for the 300 μm device, for IP3 matching) for the bigger device due to a larger drain current in the device, which leads to a greater DC power dissipation. The larger drain current in the bigger device also leads to a lower PAE compared to the smaller device. The 500 μm GaN HEMTs yielded a higher output power compared to the 300 μm GaN HEMT, but it is of smaller power density (W/mm).

3.3.3. Source/load pull and power measurements on GaAs pHEMTs:

As stated before, the GaAs pHEMTs are not operated in high-power Class A bias mode because of an excessive thermal dissipation at high Class A current levels. This may lead to the destruction of the device due to the GaAs substrate's poor thermal

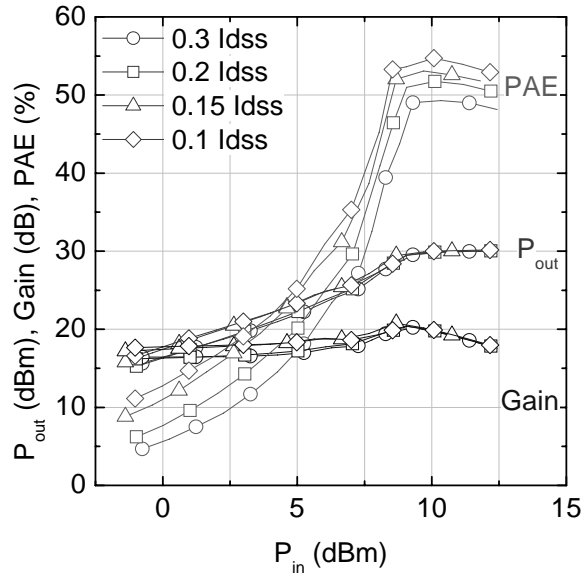


Figure 3.16: Bias effect on single-tone power performance of 500 μm GaAs pHEMT

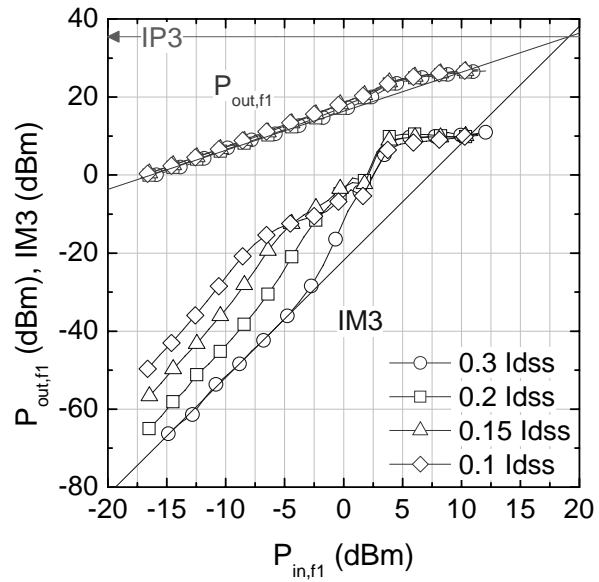


Figure 3.17: Bias effect on two-tone power performance of 500 μm GaAs pHEMT

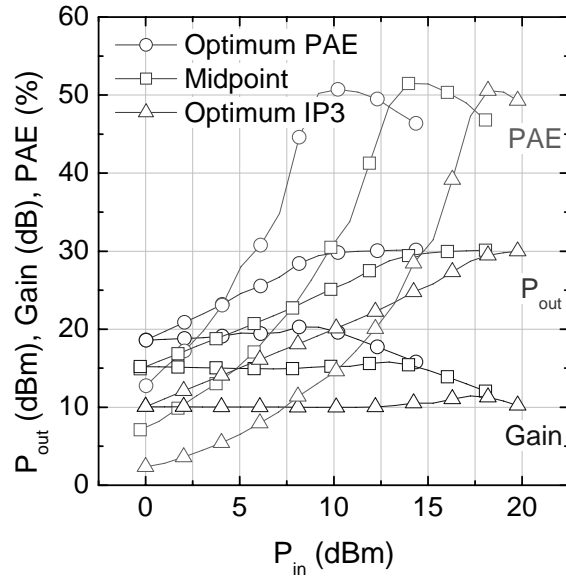


Figure 3.18: Single-tone power measurements on Class AB biased 500 μm GaAs pHEMT when input is PAE or IP3 matched

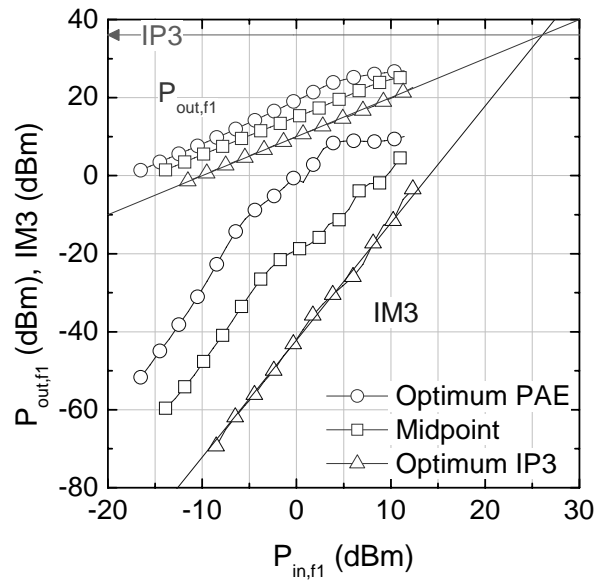


Figure 3.19: Two-tone power measurements on Class AB biased 500 μm GaAs pHEMT when input is PAE or IP3 matched

conductivity. For this reason, for GaAs pHEMT devices, maximum drain voltage was limited to 15 V, and they were not biased in Class A. The bias effect was examined first on 500 μm GaAs pHEMT. Keeping the drain voltage of 500 μm GaAs pHEMT at 15 V, gate voltage was adjusted to set I_{DS} at 30, 20, 15 and 10 % of I_{DSS} . For each bias condition, both device's input and output were power matched with fixed input power level at 10 dBm. Then, power measurements were performed. Variation of P_{out} , Gain, and PAE with P_{in} for single-tone operation and variation of $P_{\text{out}, f1}$ and IM3_{2f1-f2} with $P_{\text{in}, f1}$ for two-tone operation are shown in Figures 3.16 and 3.17, respectively, for differently biased 500 μm GaAs pHEMT. As in case of GaN HEMT, there is a direct tradeoff between efficiency and linearity for a change in bias current: decreasing I_{DS} leads to increasing PAE and decreasing IP3 (increasing IM3), as shown in Figures 3.16 and 3.17, respectively. Though, at low P_{in} level, the values of P_{out} , Gain, and IM3 are bias condition dependent, these values converge at large input signal levels regardless of the bias condition, as seen in GaN HEMT devices (Fig. 3.2 and Fig. 3.3). Similar bias effect results were observed for 700 μm and 900 μm gate width GaAs pHEMT devices as well.

Linearity and PAE tradeoffs with tuning for GaAs pHEMT devices are similar to those of GaN HEMT devices. Variation of P_{out} , Gain, and PAE with P_{in} for single-tone operation and variation of $P_{\text{out}, f1}$ and IM3_{2f1-f2} with $P_{\text{in}, f1}$ for two-tone operation are shown in Figures 3.18 and 3.19, respectively, for a Class AB biased 500 μm GaAs pHEMT device at three different source impedances including those corresponding to the optimum PAE and optimum IP3. The source tuning from optimum PAE to optimum IP3

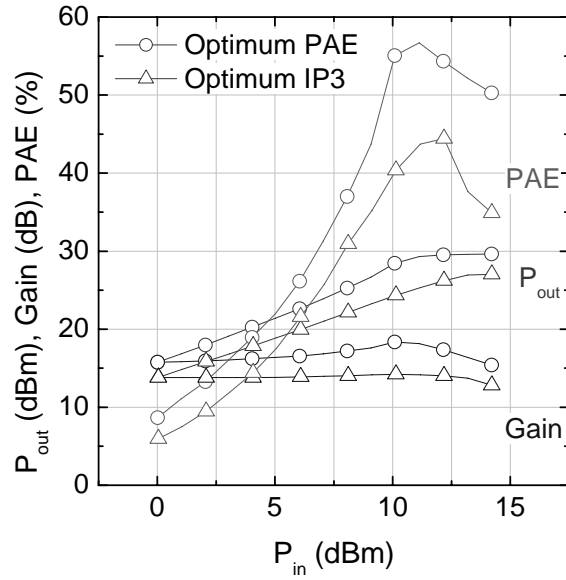


Figure 3.20: Single-tone power measurements on Class AB biased 500 μm GaAs pHEMT when output is PAE or IP3 matched

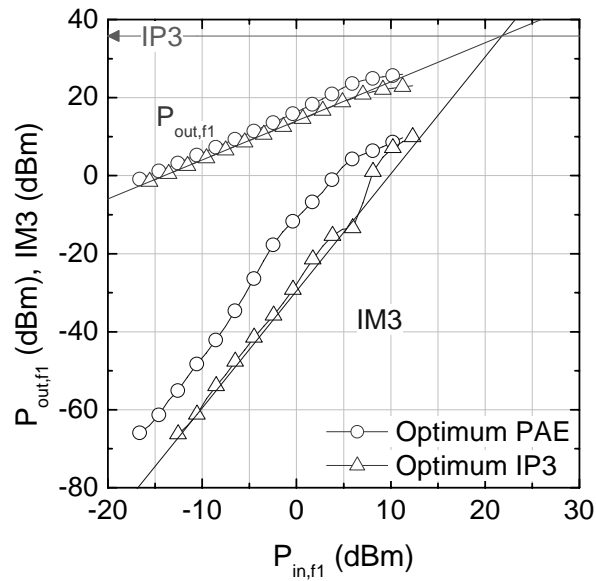


Figure 3.21: Two-tone power measurements on Class AB biased 500 μm GaAs pHEMT when output is PAE or IP3 matched

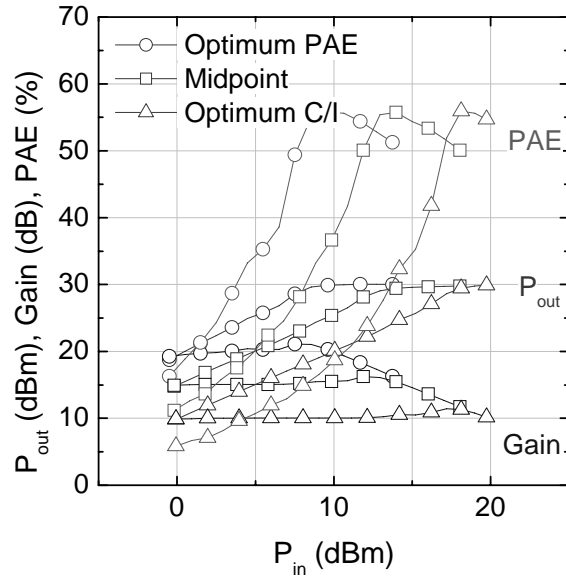


Figure 3.22: Single-tone power measurements on Class B biased 500 μm GaAs pHEMT when input is PAE or C/I matched

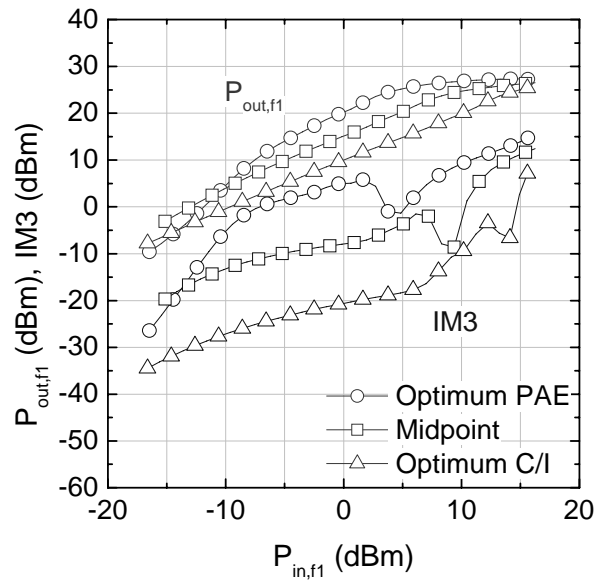


Figure 3.23: Two-tone power measurements on Class B biased 500 μm GaAs pHEMT when input is PAE or C/I matched

resulted in a shift in the PAE peak towards higher P_{in} values as in case of GaN. The source tuning improved IP3 (from 27.7 dBm to 36.7 dBm) without any significant change in peak PAE (~50 %). Similar source tuning effects were observed for the 700 and 900 μm GaAs pHEMT devices, as well.

For all three different gate width GaAs pHEMT devices, source tuning increased IP3 significantly (22 – 32 %), without sacrificing the maximum achievable PAE. The PAE values are almost similar (48.5 – 50.9 %), regardless of the gate width. As in the case of GaN devices, the IP3 values are higher for the larger GaAs device (39.8 dBm for the 900 μm device vs. 36.7 dBm for the 500 μm device, for optimum IP3 input match), but unlike in the case of GaN devices, the LFOM is larger (11.4, 12.2, and 13.5 for 500 μm , 700 μm , and 900 μm GaAs devices, respectively, for IP3 input match) for the bigger devices. This is because the increase in drain current of bigger devices is not to the same scale as the increase in IP3. As in case of GaN devices, for the GaAs devices also, the larger device yielded a higher P_{out} but lower output power density (W/mm).

The load tuning effects for Class AB biased GaAs pHEMT devices are similar to that of GaN devices requiring a substantial reduction (from 50.0 % to 41.6 %) in PAE even to obtain a small increase (2.5 dB) in IP3 for 500 μm gate width device (see Figures 3.20 and 3.21).

As in case of class AB, for class B bias also, the source tuning improved linearity (a C/I at null increase from 26.5 dB, for optimum PAE tuning, to 31.1 dB, for optimum C/I) without compromising PAE for GaAs pHEMT devices (see Figures 3.22 and 3.23).

The load tuning effect of class B biased GaAs pHEMT devices are similar to that of class AB bias requiring a substantial reduction in PAE even to obtain a small decrease in IM3.

Based on the results presented above, the general bias and tuning (source and load) effects on power performances (P_{out} , PAE and linearity) of the GaAs pHEMTs are similar to those of the GaN HEMTs. Source tuning for Class AB or B biased GaAs transistors successfully increased linearity (IP3 or C/I) without sacrificing the maximum achievable PAE. Load tuning to gain more IP3 or C/I for transistors in any bias condition results in some increases in IP3 or C/I; however, the achievements are much less significant than the source tuning for achieving optimum IP3 or C/I. In addition, for load tuning, substantial amount of PAE is sacrificed for the marginal improvements in IP3 or C/I. Thus, the source tuning is more effective than the load tuning for GaAs pHEMT devices under any biased condition, as in case of GaN HEMTs.

3.3.4. Comparison between GaN HEMTs and GaAs pHEMTs:

For Class AB biased GaN and GaAs devices, the source tuning resulted in a shift in the PAE peak, maintaining its peak value. The PAE peak values are smaller for larger gate width of the GaN HEMT devices, whereas, for GaAs pHEMTs, the PAE peak values are independent of the gate width of the devices. The LFOM values are smaller for increasing gate width of the GaN HEMT devices, whereas, the LFOM values are larger for increasing gate width of the GaAs pHEMT devices. Among different gate width devices, the larger gate-width devices yield higher IP3 than the smaller ones; however, the larger drain currents in the larger gate-width devices may lead to smaller LFOM, if

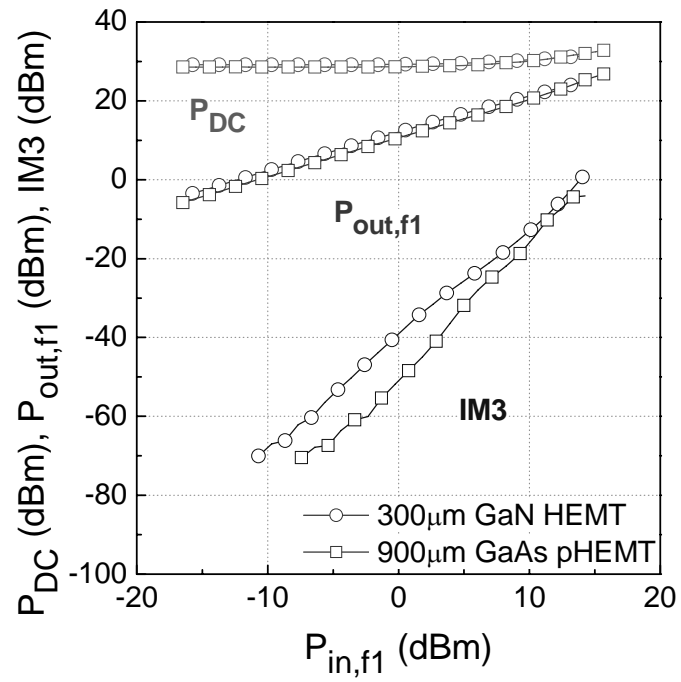


Figure 3.24: Linearity and power performance comparison between 300 μm GaN HEMT and 900 μm GaAs pHEMT in Class AB operation

Table 3.2: GaN HEMT power measurement results

Gate Width	300 μm												500 μm					
	A			AB			B			A			AB					
	SP	LP	LP	SP	LP	LP	SP	LP	LP	SP	LP	LP	SP	LP	LP			
PAE Match	P_{out} (W/mm)	4.83	4.87	4.69	3.70	3.71	2.14	4.89	4.75	4.49	4.05	4.89	4.75	4.49	4.05			
	PAE (%)	38.4	41.9	58.5	61.5	56.6	67.1	36.3	37.3	48.0	52.8	36.3	37.3	48.0	52.8			
	IP3 (dBm)	31.8	42.0	32.4	32.4	-	-	42.7	44.4	34.5	34.7	42.7	44.4	34.5	34.7			
	LFOM	4.00	4.24	2.13	2.38	-	-	2.95	4.50	1.80	1.84	2.95	4.50	1.80	1.84			
	C/I at null (dB)	-	-	-	-	22.5	25.1	-	-	-	-	-	-	-	-	-		
IP3 Match	P_{out} (W/mm)	4.69	4.71	4.08	2.62	3.71	1.49	n/a	4.50	n/a	1.66	n/a	4.50	n/a	1.66			
	PAE (%)	31.4	41.8	58.8	45.8	56.6	13.2	21.9	36.5	47.1	39.3	21.9	36.5	47.1	39.3			
	IP3 (dBm)	42.8	42.3	38.2	33.2	-	-	44.1	44.7	40.8	35.6	44.1	44.7	40.8	35.6			
	LFOM	4.99	4.53	8.05	2.86	-	-	4.10	4.73	6.29	2.32	4.10	4.73	6.29	2.32			
	C/I at null (dB)	-	-	-	-	34.1	43.5	-	-	-	-	-	-	-	-	-		

Table 3.3: GaAs pHEMT power measurement results

Gate Width	500 μm						700 μm		900 μm	
	AB			B			AB		AB	
Bias Configuration	SP	LP	SP	LP	SP	LP	SP	LP	SP	LP
P_{out} (W/mm)	1.90	1.47	1.95	1.51	1.72	1.33	1.60	1.59	1.60	1.59
PAE (%)	50.7	50.0	55.8	61.4	50.1	49.2	50.0	50.9	50.0	50.9
IP3 (dBm)	27.7	32.7	-	-	31.4	34.1	32.5	33.9	32.5	33.9
LFOM	1.50	4.19	-	-	2.45	4.04	2.57	3.25	2.57	3.25
C/I at null (dB)	-	-	26.5	24.4	-	-	-	-	-	-
P_{out} (W/mm)	1.80	0.80	1.76	-	1.56	0.65	1.63	0.78	1.63	0.78
PAE (%)	50.6	41.6	56.0	-	48.5	38.0	49.8	38.2	49.8	38.2
IP3 (dBm)	36.5	35.2	-	-	38.2	35.6	39.8	36.3	39.8	36.3
LFOM	11.4	7.19	-	-	12.2	5.93	13.5	5.83	13.5	5.83
C/I at null (dB)	-	-	31.1	-	-	-	-	-	-	-

PAE Match

IP3 Match

IP3 increase with respect to the gate-width increase of the device is not proportional to the I_{DS} increase with respect to the gate-width increase of the device. For the same reason, the larger gate-width devices may lead to smaller PAE. The larger gate-width transistor yields higher output power than smaller ones, but smaller power density (W/mm). All the power measurement results of GaN HEMTs and GaAs pHEMTs are summarized in Table 3.2 and Table 3.3, respectively.

The GaN HEMT device power and linearity characteristics are compared with those of GaAs pHEMT, by plotting P_{DC} ($= I_{DS} \times V_{DS}$), $P_{out, fl}$, and IM3 against $P_{in, fl}$, in Fig. 3.24, for comparable P_{DC} levels in class AB bias (i.e. comparing the 300 μm GaN HEMT with the 900 μm HV GaAs pHEMT, because both devices have similar P_{DC}). Both devices were tuned for maximum IP3. For the same P_{DC} , the $P_{out, fl}$ is similar for both devices, but the linearity properties are different. For input power levels ≥ 5 dBm, the IM products of the GaN device is very similar to that of the GaAs device, but at lower drive levels, the GaAs device has shown a better linearity (LFOM of 15 for GaAs compared to 8 for GaN). With respect to power density, the GaN devices are better because similar power levels are obtained for a third of the device size of GaAs.

3.4. Conclusion

In this work optimum tuning conditions for GaN HEMT and GaAs pHEMT devices are fully developed for high-frequency amplifier application. Most significant discovery of this work is that the source tuning of devices biased in Class AB or Class B for optimum IP3 improves IP3 without sacrificing maximum achievable PAE. It is

important to recall, the values of P_{out} , Gain, and IM3 converge at high input power levels regardless of source impedance values. The mismatched source impedance (matched for efficiency or linearity, not for output power) causes input power reflection at the device input, leading to smaller output power at specific input power levels. However, the output power increases with increasing input power and eventually saturates to the same output power as the power matched transistor would produce. On the other hand, the mismatched load impedance causes output power reflection at device output (back into the device), and in this case, the achievable maximum output power is decreased. Therefore, the load impedance must be always output power matched for any bias condition to ensure optimum power performance (P_{out} , PAE, linearity, etc.) for both GaN and GaAs devices.

The results of this study indicate superior power densities and only a marginal improvement in the PAE and the IP3 performance of GaN devices over the GaAs devices. Both output power and linearity of the device are known to improve with increasing V_{DS} [7, 61]. Therefore, there is a scope for improving the linearity performance of GaN HEMT devices over the GaAs pHEMT devices by biasing the GaN devices at a higher V_{DS} than 25 V, which is difficult to achieve with GaAs devices due to their poor thermal conductivity.

4. Conclusion

According to this work, the 4H-SiC double-implanted metal-oxide-semiconductor field-effect-transistor (DMOSFET) suffers unstable device operation due to a positive or a negative threshold voltage shift during the positive gate bias stress. The polarity and magnitude of the threshold voltage (V_{TH}) shift depends on the device operating temperature and the stress duration. The negative gate bias stress is very effective in releasing the interface and near interface trap captured electrons at 30 °C; but it is not as effective in offsetting the effects of mobile positive ion gate oxide charges at 130 °C. Positive mobile ionic charges may be the most plausible cause for the V_{TH} instability. According to this work, monitoring of the drain current transient during positive gate bias stressing is an effective method to study the 4H-SiC DMOSFET on-state instability.

Computer simulation suggested that the breakdown voltage (BV) slump in the DMOSFETs and the diodes is caused almost exclusively by the SiC/field oxide interface charges in the junction termination extension (JTE) structure. It was found that the location of the charge within the SiC/field oxide interface in the JTE structure plays an important role in determining the magnitude of the BV-slump. The most vulnerable location for the interface charge to affect the BV-slump is around the inner edge of the JTE region, and the possibility of interface charge accumulation around the inner edge of the JTE region during the bias stress was suggested by the directionality of the electric

field in the JTE structure. As in the case of the V_{TH} instability, positive mobile ionic charges may be the most plausible cause for the BV instability. The positive charges may be hydrogen ions from device passivation film of silicon nitride, or may be contaminants from the molybdenum gate metal. Verification of the exact sources of the thermally activated ionic charges, which are responsible for the V_{TH} and BV instabilities, needs further investigation.

In this work, the boro-phospho-silicate glass (BPSG) flow contours were developed with phosphorus (P) and boron (B) weight percentage constraints associated with hygroscopic nature of the BPSG, formation of crystalline boron-phosphate particles, and mobile ion trapping superimposed on the flow contours. Although one of the major objectives of finding an appropriate interlayer dielectric (ILD) is to solve SiC DMOSFET's V_{TH} and BV instability problems, it has turned out that the BPSG of any practical B and P wt % combinations will not solve these problems, due to the uncontrollably large density of mobile ions existing in the DMOSFTs of this study. The source of mobile ions must be identified and the density of the mobile ions must be reduced down to the qualified MOS process level of $1 \times 10^{10} \text{ cm}^{-2}$. Once the density of mobile ions is successfully reduced, it is possible to form a high quality ILD for a particular glass flow temperature by selecting appropriate B and P wt % combinations within the problem-free region enclosed by the developed four constraints. A smooth step coverage of the BPSG film can be achieved at further reduced temperature than the contour predicted temperature by selecting specific heat treatment conditions (for long duration, in O_2 and H_2O ambient, at high pressure, etc.).

In this work, optimum tuning conditions for GaN high electron mobility transistor (HEMT) and GaAs pseudomorphic HEMT (pHEMT) devices are fully developed for high-frequency amplifier application. Most significant discovery of this work is that the source tuning of devices biased in Class AB or Class B for optimum third-order intercept point (IP3) improves IP3 without sacrificing maximum achievable power-added-efficiency (PAE). The power performances (output power, PAE, linearity, etc.) of both GaN and GaAs devices biased in Class AB or Class B are at their optimum when the source impedance is linearity matched and load impedance is power matched. The results of this study indicate superior power densities and only a marginal improvement in the PAE and the IP3 performance of GaN devices over the GaAs devices. There is a scope for improving the linearity performance of GaN HEMT devices over the GaAs pHEMT devices by biasing the GaN devices at a higher V_{DS} than 25 V, which is difficult to achieve with GaAs devices due to their poor thermal conductivity.

5. Suggested Future Work

1. As the threshold voltage instability measurements revealed, the negative-stress of same duration as the positive-stress is very effective in emptying the interface and near interface oxide traps, which captured electrons during the positive-stress at 30 °C; but it is not equally effective in moving the mobile positive ions away from the SiC/SiO₂ interface toward the metal gate at 130 °C. Thus, a longer negative-stress duration than the positive-stress duration probably will reset the device at high device operating temperatures (like 130 °C) , and it should be verified.

2. Verification of the exact sources of the thermally activated ionic charges, which are responsible for the V_{TH} and BV instabilities, needs further investigation. Two major suspects are device passivation film and molybdenum gate metal. First, to see if the passivation film of silicon nitride is the source of mobile ions, the V_{TH} and BV instability measurements must be performed on the DMOSFET devices without any passivation film, immediately after they are fabricated. The same measurements must be performed on the DMOSFET with nickel (Ni) or aluminum (Al) gate metal instead of the molybdenum (Mo), in order to find out if the molybdenum is the source of mobile ions. Due to the difference in the work function of Ni, Al, and Mo, the V_{TH} (without any bias stressing) will be different from the V_{TH} for Mo, however, the V_{TH} shift is independent of

the work function but dependent on contaminants introduced when the corresponding metals are deposited.

3. In order to improve step coverage of ILD, use of the 2.4 wt % B and 5 wt % P BPSG as an ILD in 4H-SiC DMOSFET fabrication is proposed. For densification process, furnace anneal of 925 °C for 30 min in N₂ is suggested. For contact reflow, RTA anneal of 1150 °C for 30 sec in N₂ followed by a furnace treatment at 900 °C for 40 min in N₂ is suggested.

4. The GaN/AlGaN hetero-structure junctions have not reached their optimum performance yet. The growth conditions are being optimized by researchers to minimize substrate/GaN and GaN/AlGaN interface traps, which limit device power and linearity performance. Hence, HEMT devices made of newer GaN/AlGaN layers need to be characterized continuously to evaluate the potential of these devices for high-power amplification at high frequencies.

Appendix A

A.1. Nonlinearity

All physical systems have some degree of nonlinearity, and thus distort the signal amplification process. Very often the system nonlinearity is described with a third order polynomial:

$$y = a_1x + a_2x^2 + a_3x^3 . \quad \text{----- A.1}$$

When a sinusoidal signal at frequency f_1 ($x(t) = A_1 \cdot \cos 2\pi f_1 t$) is applied to a nonlinear system, an output spectrum of the system contains sinusoidal components at f_1 , $2f_1$ (second-order harmonic distortion), and $3f_1$ (third-order harmonic distortion). When two sinusoidal signals at frequencies f_1 and f_2 ($x(t) = A_1 \cdot \cos 2\pi f_1 t + A_2 \cdot \cos 2\pi f_2 t$) are applied to the system, the output spectrum contains not only fundamental components at f_1 and f_2 and harmonic distortion components at $2f_1$, $2f_2$, $3f_1$, and $3f_2$, but also intermodulation distortion components at $f_1 \pm f_2$ (second-order intermodulation distortion, IM2), and $2f_1 \pm f_2$ and $2f_2 \pm f_1$ (third-order intermodulation distortion, IM3). Most of these harmonic distortion and intermodulation components are easily suppressed by external filtering, but not the IM3s at $2f_1 - f_2$ and $2f_2 - f_1$. These IM3s are very close to the fundamental frequency components at f_1 and f_2 , and filtering them out requires a very narrow band-pass filter, which may be impractical. It is preferable for the IM3 generated by the system to be small, and thus, the device linearity is measured in terms of the magnitude of IM3.

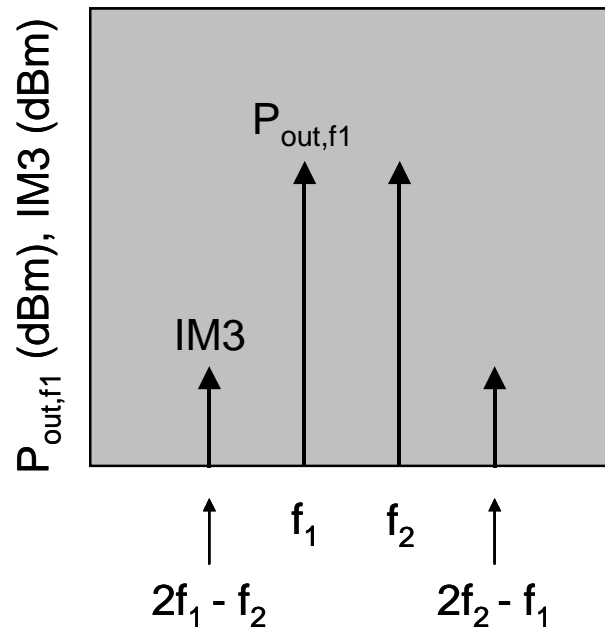


Figure A.1: Typical transistor output spectrum when two sinusoidal signals of equal magnitude at frequencies f_1 and f_2 are applied to its input

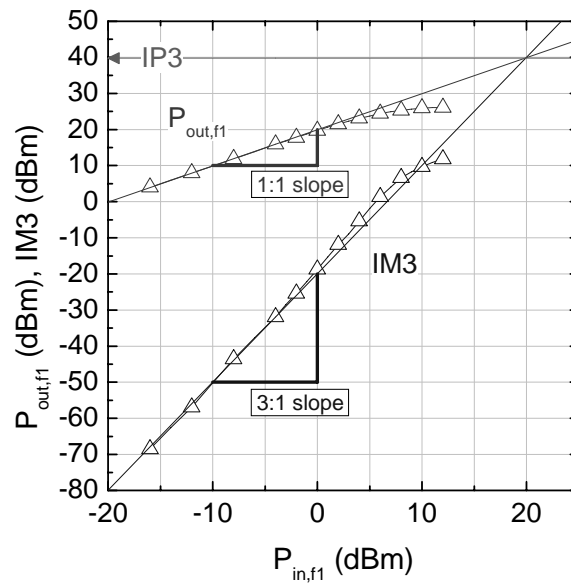


Figure A.2: Definition of the third order intercept point (IP3)

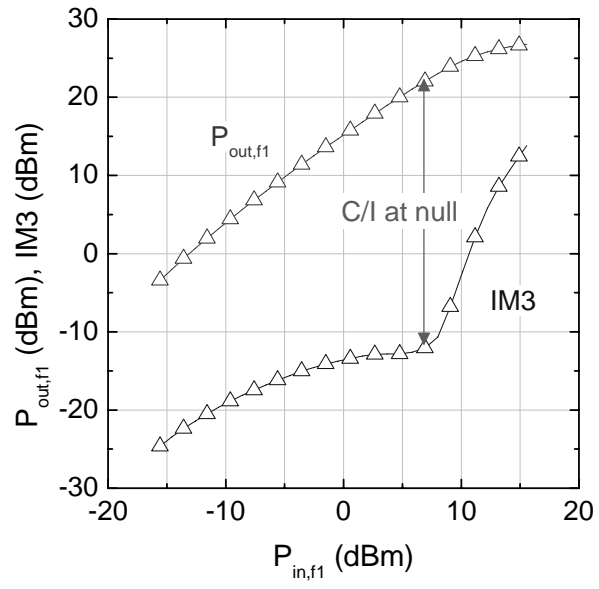


Figure A.3: Definition of C/I at null

Fig. A.1 is a typical transistor output spectrum when two sinusoidal signals of equal magnitude at frequencies f_1 and f_2 are applied to its input. As equation A.1 is solved for the two input signals at f_1 and f_2 , the coefficients of the fundamental components (at f_1 and f_2) and the third-order intermodulation components (at $2f_1 - f_2$ and $2f_2 - f_1$) are 1 and 2, respectively, which means the fundamental components and the third-order intermodulation components increase 1 dB and 3 dB ($= 10 \cdot \log 2$), respectively, for every 1 dB increase in input signals. Fig. A.2 is a typical two-tone power measurement result. One of the two fundamental output powers (usually P_{out} at f_1) and one of the two third-order intermodulation components (usually IM3 at $2f_1 - f_2$) are plotted as a function of one of the two fundamental input powers (usually P_{in} at f_1). Third-order intercept point (IP3) is defined as the interception formed by 1:1 and 3:1 slopes extrapolated from $P_{out,f1}$ and IM3, respectively. The IP3 is calculated in terms of $P_{out,f1}$ and IM3 at a low input power level, where device is not compressed and both $P_{out,f1}$ and IM3 are linear, as:

$$IP3 \text{ (dBm)} = \frac{3 \times P_{out,f1} \text{ (dBm)} - IM3 \text{ (dBm)}}{2}.$$

The IP3 enables specifying IM3 performance: the higher the IP3, the lower the IM3 for the incoming signals. For comparison among different size transistors, a linearity figure of merit (LFOM) is defined as the ratio of IP3 to DC power dissipation.

In this work, the IP3s are undetermined for the Class B biased transistors, because even at a low input power level, both $P_{out,f1}$ and IM3 are nonlinear. Therefore, linearity performance is measured instead by the carrier to intermodulation ratio (C/I), a dB separation between $P_{out,f1}$ and IM3, at null where the IM3 curvature in the Class B biased

transistor changes. As in case of IP3, the higher the C/I at null, the lower the IM3 for the incoming signals. An example two-tone power measurement result for the Class B biased transistors is given in Fig. A.3.

Appendix B

B.1. Impedance Matching

As input and output impedance matching circuitries are always incorporated in the integrated circuits built for high-frequency applications, the impedance matching is an important consideration for optimizing system specific performance.

It is not difficult to understand that the input and the output impedances of the transistor are frequency dependent, because the inductors and the capacitors, whose reactances are frequency dependant, are found in transistor's small signal model at its input and output ports. Thus, when the transistor is just placed on the probe station for the high-frequency power measurements, its input and output impedances are most likely mismatched to the source and load impedances, respectively. In this case, the measurement results are poor for all performance parameters. This situation can be improved by input and output impedance matching. The input and the output impedances of the transistor are also dependant on DC bias condition (V_{GS} and V_{DS}) and RF input power (P_{in}). Therefore, the impedance matching has to be performed even for the same transistor if biased differently.

The source/load impedance variation of the setup is achieved using tuners (see Fig. 3.1). Traditionally, source and load tuners are adjusted repeatedly until power meter reading reaches its optimum, and then the tuner losses are measured. However, this technique is not always accurate. The reason for this is the combination of tuners and

transistor is optimized, not the transistor itself. Thus, it is possible that the actual best performance of the device itself will not be revealed, if compensated with large tuner loss.

This problem can be circumvented using automated (programmable) tuners. The automated tuner can be calibrated and characterized ahead of time, and repeat its tuning conditions later during the measurement.

References

References:

- [1] K. Shenai, R. S. Scott, and B. J. Baliga, "Optimum Semiconductors for High-Power Electronics," *IEEE Trans. Elec. Dev.*, vol. 36, pp. 1811-1823, 1989.
- [2] J. W. Palmour, R. Singh, R. Glass, O. Kordina, and C. H. J. Carter, "Power Semiconductor Devices and IC's," presented at ISPSD, 1997.
- [3] J. B. Casady and R. W. Jonson, "Status of Silicon Carbide (SiC) as a Wide-Bandgap. Semiconductor for High Temperature Applications: A Review," *Solid-State Electronics*, vol. 39, pp. 1409-1422, 1996.
- [4] E. F. Schubert, *Light Emitting Diodes, Second edition*: Cambridge University Press, 2006.
- [5] F. Schwierz and J. J. Liou, *Modern Microwave Transistors - Theorie, Design, and Applications*. Hoboken: J. Wiley, 2003.
- [6] U. K. Mishra and A. S. Brown, "Microwave performance of AlInAs-GaInAs HEMTs with 0.2- and 0.1- μ m gate length," *IEEE Electron Device Lett.*, vol. 9, pp. 647-649, 1988.
- [7] F. Bue and C. Gaquiere, "A 26-40 GHz on wafer intermodulation measurement system," *Eur. Microw. Week.*, 1999.
- [8] S. L. G. Chu, J. Huang, W. Struble, and G. Jackson, "A highly linear MESFET," *IEEE MTT-S Tech. Dig.*, 1991.
- [9] M. J. Bailey, "Intermodulation distortion in pseudomorphic HEMTs and an extension of the classical theory," *IEEE Trans. Microwave Theory Tech.*, vol. 48, pp. 104-110, 2000.
- [10] H. C. Chiu, "Power and linearity comparisons of gate- and source-terminated field-plate pseudomorphic HEMTs," *Semicond. Sci. Technol.*, vol. 20, pp. 1183-1186, 2005.

- [11] N. Vellas and C. Gaquiere, "High Linearity Performances of GaN HEMT Devices on Silicon Substrate at 4 GHz," *IEEE Electron Device Lett.*, vol. 23, pp. 461-463, 2002.
- [12] Y. Wu and D. Kapolnek, "Very-High Power Density AlGaIn/GaN HEMTs," *IEEE Trans. Electron Dev.*, vol. 48, pp. 586-590, 2001.
- [13] Y. Wu, "GaN-based FET's for microwave power amplification," *IEICE Trans. Electron.*, vol. E-82-C, pp. 1895-1905, 1999.
- [14] S. Sheppard, "High-power microwave GaN/AlGaIn HEMT's on semi-insulating silicon carbide substrates," *IEEE Electron Device Lett.*, vol. 20, pp. 161-163, 1999.
- [15] J. Miller, "Design, Performance and Application of High Voltage GaAs FETs," *CSIC 2005 Digest*, pp. 236, 2005.
- [16] V. A. Dmitriev, "Electric breakdown in GaN p-n junctions," *Appl. Phys. Lett.*, vol. 68, pp. 229-231, 1996.
- [17] B. Gelmont, K. Kim, and M. Shur, "Monte Carlo simulation of electron transport in gallium nitride," *J. Appl. Phys.*, vol. 74, pp. 1818-1801, 1993.
- [18] G. J. Sullivan and M. Y. Chen, "High power 10 GHz operation of AlGaIn HFET's on insulating SiC," *IEEE Electron Device Lett.*, vol. 19, pp. 198-199, 1998.
- [19] O. Ambacher, J. Majewski, C. Miskys, A. Link, M. Hermann, M. Eickhoff, M. Stutzmann, F. Bernardini, V. Fiorentini, V. Tilak, B. Schaff, and L. F. Eastman, "Pyroelectric Properties of Al(In)GaIn/GaN Hetero- and Quantum Well Structures," *J. Phys.: Condens. Matter*, vol. 14, pp. 3399-3434, 2002.
- [20] F. Schwierz and O. Ambacher, "RECENT ADVANCES IN GaN HEMT DEVELOPMENT," *Electron Devices for Microwave and Optoelectronic Applications*, vol. 17-18, pp. 204-209, 2003.
- [21] Y. F. Wu and D. Kapolnek, "High-Al-content AlGaIn-GaN MODFETs for ultra high performance," *IEEE Electron Device Lett.*, vol. 19, pp. 50-53, 1998.
- [22] L. F. Eastman and V. Tilak, "Undoped AlGaIn-GaN HEMTs for microwave power amplification," *IEEE Trans. Electron Dev.*, vol. 48, pp. 479-485, 2001.
- [23] J. S. Moon and M. Micovic, "GaN/AlGaIn HEMTs operating at 20GHz with continuous-wave power density > 6W/mm," *Electron. Lett.*, vol. 37, pp. 528-530, 2001.

- [24] A. Agarwal and S. H. Ryu, "Status of SiC Power Devices and Manufacturing Issues," in *CS MANTECH*: Vancouver, British Columbia, Canada, 2006, pp. 215-218.
- [25] R. Schorner, P. Friedrichs, D. Peters, and D. Stephani, "Significantly improved performance of MOSFET's on silicon carbide using the 15R-SiC polytype," *IEEE Elec. Dev. Lett.*, vol. 20, pp. 241–244 1999.
- [26] E. Pippel, J. Woltersdorf, H.O.Olafson, and E.O.Sveinbjornsson, "Interfaces between 4H-SiC and SiO₂: Microstructure, nanochemistry, and near-interface traps," *J. Appl. Phys.*, vol. 97, pp. 034302, 2005.
- [27] G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, R. K. Chanana, R. A. Weller, S. T. Pantelides, L. C. Feldman, O. W. Holland, M. K. Das, and J.W. Palmour, "Improved inversion channel mobility for 4H-SiC MOSFETs following high temperature anneals in nitric oxide," *IEEE Elec. Dev. Lett.*, vol. 22, pp. 176, 2001.
- [28] K. C. Chang, N. T. Nuhfer, L. M. Porter, and Q. Wahab, "High Carbon Concentrations at the Silicon Dioxide – Silicon Carbide Interface Identified by Electron Energy Loss Spectroscopy," *Appl. Phys. Lett.*, vol. 77, pp. 2186-2188, 2000.
- [29] G. G. Jernigan, R. E. Stahlbush, M. K. Das, J. J.A. Cooper, and L. A. Lipkin, "Interfacial differences between SiO₂ grown on 6H-SiC and on Si(100)," *Appl. Phys. Lett.*, vol. 74, pp. 1448, 1999.
- [30] M. M. Maranowski and J. J.A. Cooper, "Time-Dependent-Dielectric-Breakdown Measurements of Thermal Oxides on N-Type 6H-SiC," *IEEE Trans. Elec. Dev.*, vol. 46, pp. 520-524, 1999.
- [31] L. A. Lipkin and J. W. Palmour, "Insulator investigation on SiC for improved reliability," *IEEE Trans. Elec. Dev.*, vol. 46, pp. 525, 1999.
- [32] M. Gurfinkel, J. Suehle, J. B. Bernstein, Y. Shapira, A. J. Lelis, D. Habersat, and N. Goldsman, "Ultra-Fast Measurements of VTH Instability in SiC MOSFETs due to Positive and Negative Constant Bias Stress," *IRPS*, 2007.
- [33] A. J. Lelis, D. Habersat, F. Olaniran, B. Simons, J. McGarrity, F. B. McLean, and N. Goldsman, "Time-Dependent Bias Stress-Induced Instability of SiC MOS Devices," presented at MRS Proceedings, 2006.

- [34] A. J. Lelis, D. Habersat, G. Lopez, J. M. McGarrity, F. B. McLean, and N. Goldsman, "Bias Stress-Induced Threshold-Voltage Instability of SiC MOSFETs," in *ICSCRM*. Pittsburgh, Pennsylvania, 2005.
- [35] S. Wolf and R. N. Tauber, *Silicon Processing for the VLSI Era, Vol 1: Process Technology*: Lattice Press, 1986.
- [36] W. Kern and G. L. Schnable, "Chemically Vapor-Deposited Borophosphosilicate Glasses for Silicon Device applications," *RCA Review*, vol. 43, pp. 423-457, 1982.
- [37] R. H. Dawson and G. L. Schnable, "Passivating Composite for a Semiconductor Device Comprising a Silicon Nitride (Si_3N_4) Layer and Phosphosilicate Glass (PSG) layer," U.S. Patent 4,273,805; June 16, 1981.
- [38] M. Yoshimaru and H. Wakamatsu, "Microcrystal Growth on Borophosphosilicate Glass Film during High-Temperature Annealing," *J. Electrochem. Soc.*, vol. 143, pp. 666-671, 1996.
- [39] L. Zambov, Y. Yanakiev, I. Nedev, and M. Anastassova, "Characterization of arsenphosphosilicate glass films for VLSI applications - Part II. Step coverage and planarization," *Solid-State Electronics*, vol. 34, pp. 1239-1246, 1991.
- [40] J. M. Eldridge, R. B. Laibowitz, and P. Balk, "Polarization of thin phosphosilicate glass in MGOS structures," *J. Appl. Phys.*, vol. 40, pp. 1922-1930, 1969.
- [41] P. Balk and J. M. Eldridge, "Phosphosilicate glass stabilization of FET devices," *Proceedings of the IEEE*, vol. 57, pp. 1558-1563, 1969.
- [42] E. H. Snow and B. E. Deal, "Polarization phenomena and other properties of phosphosilicate glass films on silicon," *J. Electrochem. Soc.*, vol. 133, pp. 263-269, 1966.
- [43] D. K. Schroder, *Semiconductor Material and Device Characterization*, 2nd ed. New York: Wiley-Interscience, 1998.
- [44] L. Stauffer and T. Wiley, "Mobile Ion Monitoring By Simultaneous Triangular Voltage Sweep," in *Solid State Technology - Metrology Supplement*, vol. 38, 1995.
- [45] J. R. Trost, S. R.S. Ridley, M. K. Khan, T. Grebs, H. Evans, and S. Arthur, "The Effect of Charge in Junction Termination Extension Passivation Dielectrics," presented at Proc. 11th Int. Symp. Power Semiconductor Devices and Ics, Toronto, Ont., Canada, 1999.

- [46] B. J. Baliga, *SILICON CARBIDE POWER DEVICES*: World Scientific Pub Co Inc 2006.
- [47] M. Yamin, "Observations on Phosphorus Stabilized SiO₂ Films," *IEEE Trans. Electron Devices*, vol. 13, pp. 256-259, 1966.
- [48] W. Kern and G. L. Schnable, "CVD BPSG for Si Devices," *RCA Review*, vol. 43, pp. 423-457, 1982.
- [49] J. K. Cramer, S. P. Murarka, K. V. Srikrishnan, and W. Patrick, "Sodium passivation dependence on phosphorus concentration in tetraethylorthosilicate plasma-enhanced chemical vapor deposited phosphosilicate glasses," *J. Appl. Phys.*, vol. 73, pp. 2458-2461 1993.
- [50] J. E. Tong, K. Schertenleib, and R. A. Carpio, "Process and Characterization of PECVD BPSG Films for VLSI Applications," *Solid State Technol.*, vol. 27, pp. 161, 1984.
- [51] J. C. Mikkelsen, F. L. Galeener, and W. J. Mosby, "Raman Characterization of Hydroxyl in Fused Silica and Thermally Grown SiO₂," *J. Electron. Mater.*, vol. 10, pp. 631, 1981.
- [52] N. E. McGruer and R. A. Oikari, "Polysilicon capacitor failure during rapid thermal processing," *IEEE Trans. Elec. Dev.*, vol. 33, pp. 929, 1986.
- [53] F. Hashemi, "Rapid Thermal Annealing Effects on Gate Oxide of Ion Implanted Devices," *Semiconductor Int.*, pp. 152, 1988.
- [54] R. G. Cosway and M. W. Hodel, "Effect of RTA on Thin Thermal Oxide," *J. Electrochem. Soc.*, vol. 135, pp. 533, 1988.
- [55] H. Wendt, A. Spitzer, W. Bensch, and K. V. Sichart, "Improvement of Oxide Quality by Rapid Thermal Annealing," *J. Appl. Phys.*, vol. 67, pp. 7531, 1990.
- [56] J. C. Hsieh, Y. K. Fang, C. W. Chen, N. S. Tsai, M. S. Lin, and F. C. Tseng, "Study and Improvement of Anomalous Interface state of Metal-Oxide-Semiconductor Structure induced by Rapid Thermal Post-Oxide Annealing," *J. Appl. Phys.*, vol. 73, pp. 5432, 1993.
- [57] P. L. Castro and B. E. Deal, "Low-Temperature reduction of Fast Surface States Associated with Thermally Oxidized Silicon," *J. Electrochem. Soc.*, vol. 118, pp. 280, 1971.

- [58] J. C. Hsieh, Y. K. Fang, C. W. Chen, N. S. Tsai, M. S. Lin, and F. C. Tseng, "The Anomalous Threshold Voltage Shift of N- and P-MOSFET Under Flow and Reflow of BPSG Film With RTA and/or Furnace," *IEEE Trans. Electron Devices*, vol. 41, pp. 458-460, 1994.
- [59] V. Paidi and S. Xie, "High Linearity and High Efficiency of Class-B Power Amplifiers in GaN HEMT Technology," *IEEE Transactions on Microwave Theory and Techniques*, vol. 51, pp. 643-652, 2003.
- [60] K. Krishnamurthy, "Broadband GaAs MESFET and GaN HEMT resistive feedback power amplifier," *IEEE J. Solid-State Circuits*, vol. 35, pp. 1285-1292, 2000.
- [61] M. Nagahara and T. Kikkawa, "Improved Intermodulation Distortion Profile of AlGaIn/GaN HEMT at High Drain Bias Voltage," *IEDM Tech. Digest*, pp. 693-696, 2002.

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