DESIGN, FABRICATION, AND RELIABILITY STUDY OF SECOND-LEVEL COMPLIANT MICROELECTRONIC INTERCONNECTS

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DESIGN, FABRICATION, AND RELIABILITY STUDY OF SECOND-LEVEL COMPLIANT MICROELECTRONIC INTERCONNECTS

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To my grandparents
To my parents
To my sisters
To my uncles and aunts

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CHAPTER 1 INTRODUCTION

1.1. BACKGROUND

Electronic packaging is an important discipline in the field of electronic engineering. The electronic devices typically refers to the integrated circuits that integrate resistors, capacitors, transistors, dielectrics and other elements into circuits in order to have particular functions. These integrated circuits (ICs) and other components are then interconnects by the carrier – “Packaging”, which provides the functions of cooling, powering, communicating signals, protecting ICs, etc. The electronic packaging is mainly categorized into three levels: (1) IC level (referred to as First-Level) packaging a single IC; (2) system level (referred to as Second-Level) packaging multiple ICs and different types of components on the system-level board (3) Third-Level packaging that connects several system-level boards to form a larger system.

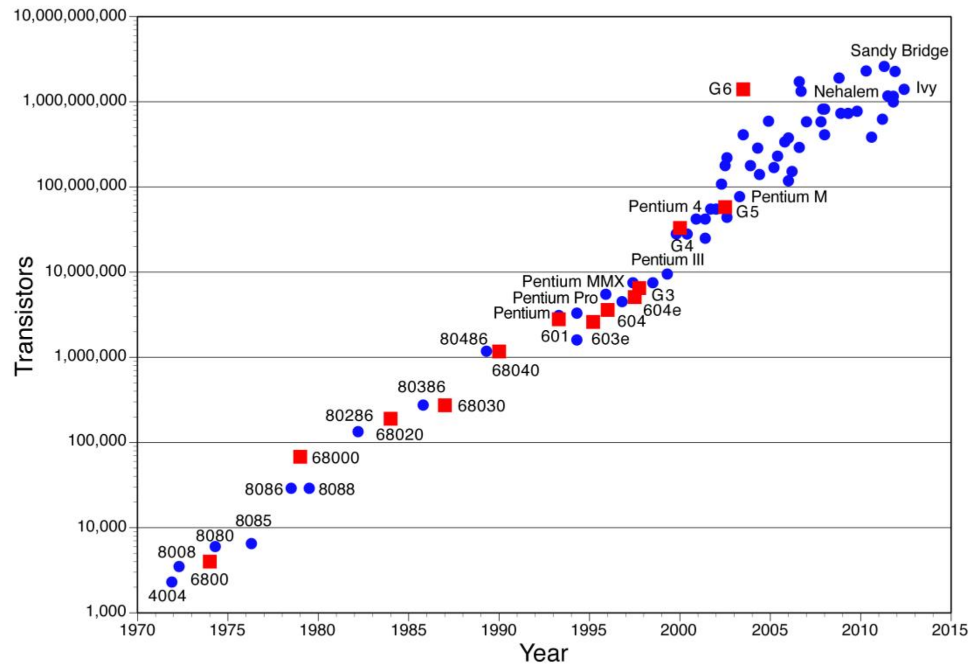


Figure 1-1 Moore’s Law (http://chemistry.beloit.edu/edetc/SlideShow/slides/contents/computer.html)

There are many parameters to be considered in the electronic packaging including input/output (I/O) connections, size, materials, bonding technologies, fabrication

methodology, thermal management, integrated functions, reliability, cost, etc. With continued evolution of functionality and performance, the number of I/O's has continued to increase. This means that with further miniaturization, the I/O density has continued to increase even faster. All of these requirements facilitate the use of area-array interconnections throughout the various levels of the packages. Moore's law states that the number of transistors in an integrated circuit doubles approximately every 18 - 24 months [1].

The Second-Level Interconnect, also known as substrate-to-board interconnect technology, allows communication between an interposer and a board. Ball Grid Array (BGA) solder balls are the most commonly used Area-array Second-Level Interconnects. An interposer is an electrical interface used to redistribute I/O from a smaller pitch to a larger pitch. The interposer materials can be organic, ceramic, metal, single crystal silicon, polysilicon or glass [2]. The organic interposers is currently one of the most commonly used types of interposers in the electronic packaging, but they have four main shortcomings: (1) low I/O pitch; (2) low thermal conductivity resulting in poor thermal performance; (3) large coefficient of thermal expansion (CTE) mismatch between the organic material and silicon die; (4) large warpage due to low Young's modulus. The interposers made from silicon and glass that are able to address all of the problems stated above are getting more and more popular [2, 3]. Both the silicon interposer and the glass interposer have very close CTE to the silicon die because of the same or similar material properties. The silicon interposer has much higher thermal conductivity than that of the organic interposer, while the glass interposer has relatively low thermal conductivity but it can be overcome if a large number of copper-vias are embedded, and this can be easily achieved by laser and electrical discharge processes. Both the silicon interposer and the glass interposer have very good surface finish and flatness, and can provide much finer I/O pitches. In addition, the glass is the cheapest package material among all of them and is isotropic leading to some other advantages when used as the interposer.

Therefore, with the switch from organic interposer to silicon/glass interposer technology, the CTE mismatch originally happened between a silicon die and an organic interposer is now existing in the silicon/glass interposer-organic board level (Second-Level packaging). The CTE mismatch between the interposer and the board causes thermo-mechanical strains on solder balls under thermal excursions. These solder ball strains can be reduced with the application of an epoxy-based underfill. The underfill acts as an extension of the solder ball, sharing the thermo-mechanical loads to ensure that the solder balls are not stressed under the loads and thus protect the solder balls. However, the inclusion of underfills tightly couples the interposer to the board and induces very high stresses within the interposer, especially when the interposer is silicon. To reduce these stresses and thus to address associated reliability issues, researchers have sought various packaging interconnect solutions. A logical first step will be the elimination of the underfill or by substituting the solder interconnect with a compliant interconnect. However, the removal of the underfill renders the solder balls vulnerable to premature fatigue failure. Hence a compliant substitute for the otherwise rigid solder balls is needed. This need has led to the exploration of compliant interconnects as substitutes for solder balls.

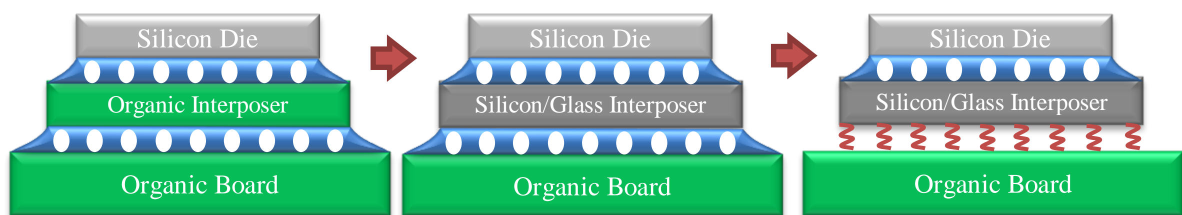


Figure 1-2 Shift from organic to silicon/glass interposer technology facilitates the use of compliant interconnects (white: solder balls; blue: underfill; red: compliant interconnects)

On the other hand, over the last decade, the 3D packaging and 3D ICs are becoming more and more popular due to the ever-increasing demand of reduced power consumption, smaller footprint, higher I/O density, short path length and hence better performance [4-7]. The 3D packaging uses traditional methods of interconnection to

achieve the stacks in the vertical direction. System in Package (SiP, Figure 1-3) and Package on Package (PoP, Figure 1-4) are the most commonly used 3D integration technologies. The 3D ICs (Figure 1-5 and Figure 1-6) usually refers to 3D die stacking using wire bonding (Figure 1-5), TSV interconnects (Figure 1-6) or monolithic approach [8].

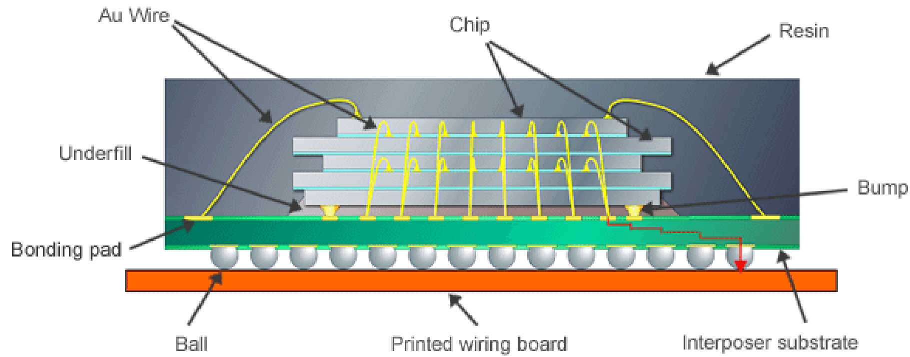


Figure 1-3 System in Package (Source: Renesas Electronics Co.)

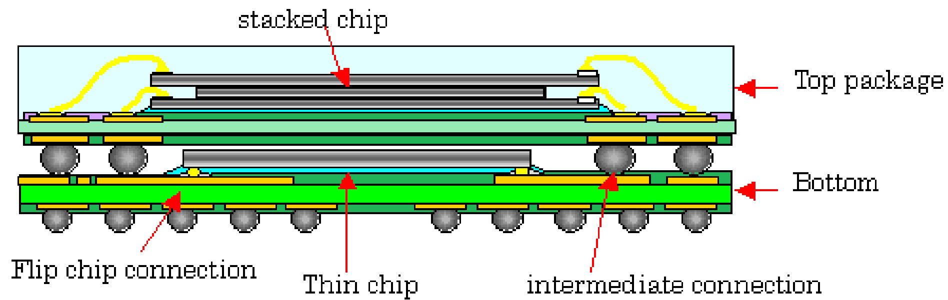


Figure 1-4 Package on Package (Source: Shinko Electric Industries Co., LTD)

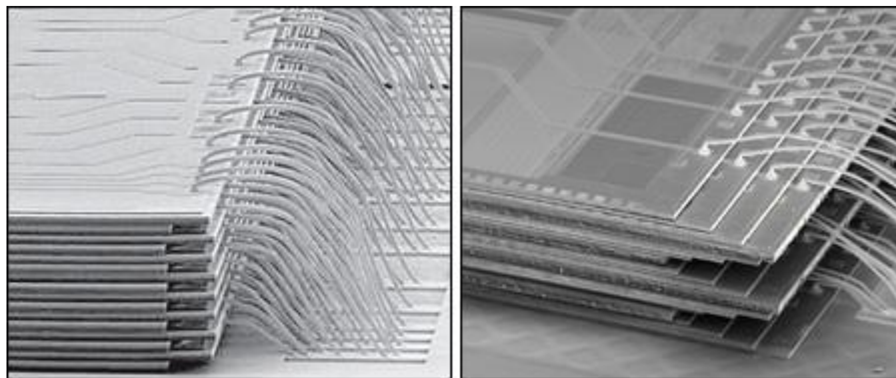


Figure 1-5 3D die stacking using wire bonding (Source: The Korea Times)

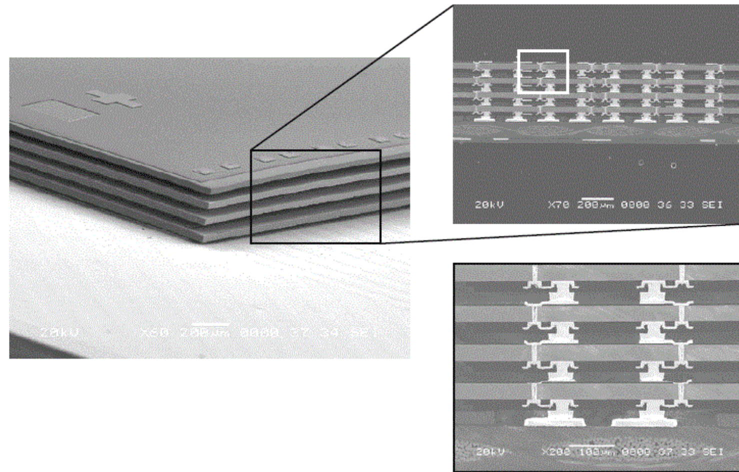


Figure 1-6 3D die stacking using TSVs (Source: Amkor Technology)

However, the stacked 3D structure in the vertical direction, although improves the electrical performance, makes the whole structure much stiffer and more difficult to bend in order to relieve the stresses carried by the solder balls when subjected to the external loads. Since the solder balls are mostly not protected by the underfill in the Second-Level packaging, this can result in premature failure of the solder balls. Therefore, the increasingly popular use of 3D packaging and 3D ICs facilitate the application of the compliant interconnects.

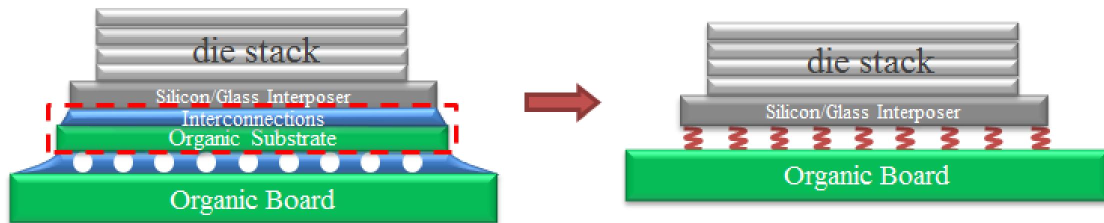


Figure 1-7 3D packaging and 3D ICs facilitate the use of compliant interconnects (white: solder balls; blue: underfill; red: compliant interconnects)

Additionally, for applications where the devices are subjected to the repetitive impact loads, e.g. the landing gears, the semiconductor devices in the automotive and the handheld devices that are more vulnerable to the drops, the rigid solder ball interconnects may transmit the impact loads from the devices to the interposer and furthermore to the sensitive elements mounted on the interposer, which might lead to the mechanical failure

of the elements. The compliant interconnects can be used as effective impact isolators under such circumstances. Lastly, the compliant interconnects can be applied as vibration isolators in some MEMs that are sensitive to vibration to enhance the performance.

1.2. LITERATURE REVIEW

This section will outline some of the main compliant interconnects that are being pursued in universities and industry, and the strengths and weaknesses associated with them. It is important to point out that most of the compliant interconnects developed so far are applied as the First-Level interconnects.

1.2.1. Copper Pillar Bumps

Copper pillar bumps are one of the earliest developed interconnects among all of the substitutes of the solder ball interconnects. Copper is an ideal material for the interconnects due to its good electrical and thermal properties, as well as the cost, although some other materials can also be used as the pillar bumps. The copper pillar bumps are usually formed as slender column structure to reduce the pitch size and increase the compliance values, but they are relatively stiff compared with the true compliant interconnects due to their bulk shapes although they have more slender shapes than the solder balls in general. IBM was firstly issued a patent of a bump structure on 8 May 2011 [9]. This bump structure consists of two layers with the upper layer (3b in Figure 1-8) that fuses in soldering and connects the bump to the substrate and the lower layer (3a in Figure 1-8) that has at least 20ºC higher melting point than that of the upper layer and is generally made of copper or gold. This bump structure is called metal post solder chip connection (MPS-C2) by IBM.

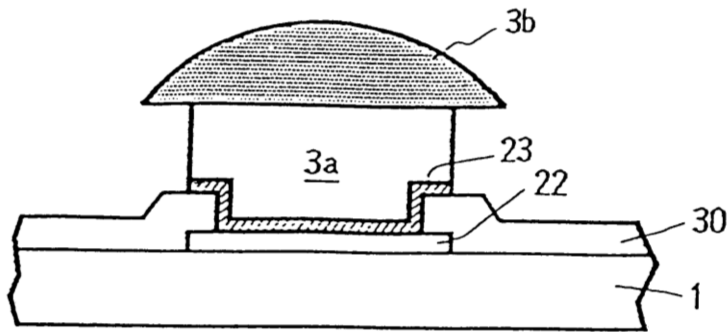


Figure 1-8 IBM MPS-C2 Design (Source: http://www.google.com/patents/US6229220)

Another copper pillar bump interconnect with similar structure as IBM MPS-C2 was proposed by Francisca Tung of Advanpack Solutions (APS) in 2003[10, 11]. Intel was issued another pillar bump patent in 2007 [12]. Compared to the two pillar bumps introduced above, the lower layer in this pillar bump includes a diffusion barrier and a wetting layer wrapping the base metal, as shown in Figure 1-9.

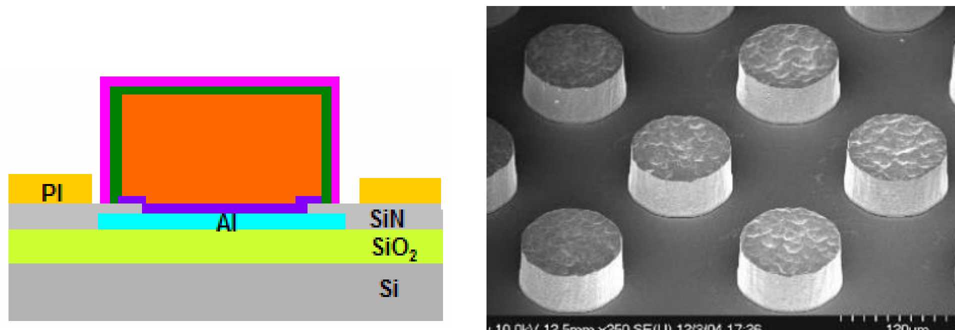


Figure 1-9 Left: Intel bump with external coating over pillar; right: Intel Electroplated Copper Bumps on Die. (Source: [13])

Although to achieve high volume manufacturing (HVM) for the copper pillar bumps is more difficult than the solder ball interconnects, its fabrication process is much easier than other types compliant interconnect owing to its simple pillar geometry. Both the copper pillar and the solder cap can be electroplated after the features are patterned. The copper bump pillars are usually in a slender post shape and therefore they can be used as fine-pitch interconnects. However, because the copper pillar bumps are much less compliant than the other kinds of compliant interconnects, they are likely to fail

prematurely under the thermal cycling loads if not underfilled [14]. The copper microwire arrays pursued at Georgia Tech [15] use a design of higher aspect ratio to improve the mechanical reliability.

1.2.2. Nano-pillar Interconnects

The compliant interconnects categorized in this part are similar to the copper pillar bumps in shape, but have much higher aspect ratios. The high aspect ratio significantly increases the compliance values of the interconnects owing to the much smaller bending stiffness as well as the axial stiffness if the same material is used. The high aspect ratio also makes the structure easier to buckle under axial compression load. Based on the application of the interconnects and the loads applied on the interconnects, beam bending is the primary deformation of the pillar-shaped interconnects. According to the structural mechanics, for two beams with same length and material properties, as well as under the same deformation, the stresses induced within the slender beam are smaller in general. Therefore, the nano-pillar interconnects have better mechanical reliability than the copper pillar bumps.

One of the most commonly explored types of nano-pillar interconnects is the carbon nanotube (CNT) interconnect [16-19]. The CNTs have very high elastic modulus, tensile and flexural strengths, but the effective modulus of the CNTs is 4-5 orders of magnitude lower than a straight CNT due to its wavy geometry [20]. This mechanical compliance property of the CNTs together with its excellent electrical and thermal conductance in the form of vertically aligned forests make them as ideal candidates as compliant interconnects. However, fabricating the carbon nanotube interconnects and reliably assembling them are generally much more complicated than those of the other compliant interconnects.

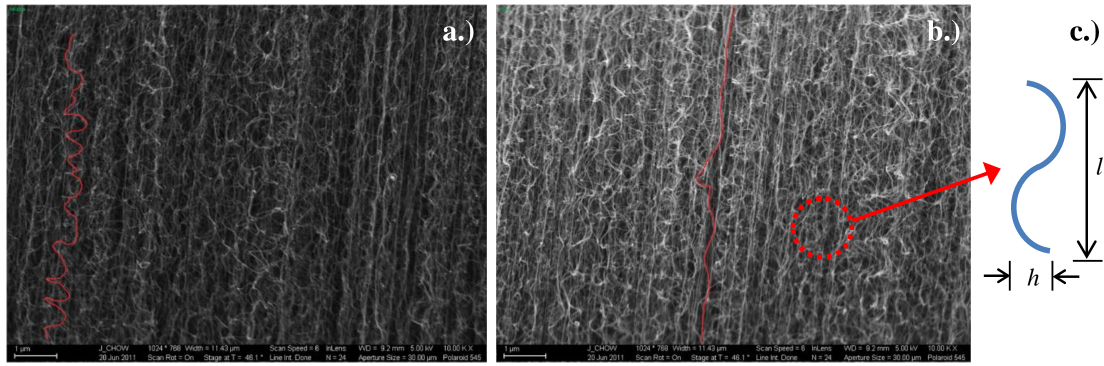


Figure 1-10 SEM images showing the waviness of the vertically aligned CNTs (Source: [20])

Copper nanowire bumps [21-23] and multicopper-column interconnects [24] are the other two kinds of nano-pillar that are relatively easy to fabricate and assemble compared to the CNTs. However, it can be seen from Figure 1-11and Figure 1-12 that both nanowire bumps and multicopper-column interconnects although have larger aspect ratio than the copper pillar bumps, their aspect ratios are much inferior to the CNTs. And their cross-section dimension, especially that of the multicopper-column interconnects, is “micro” while it is “nano” for the CNTs. Since the nanowire bumps and multicopper-column interconnects are made of copper and consist of a large number of slim pillars, they tend to have very high self and mutual inductance.

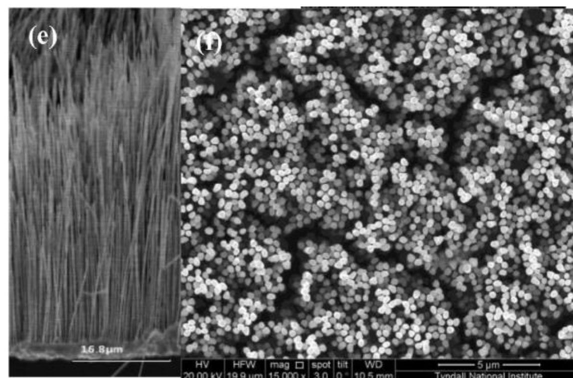


Figure 1-11 Copper nanowire array bumps (Source: [22])

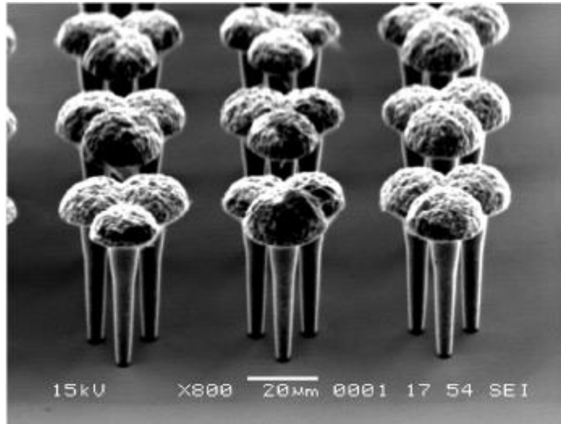


Figure 1-12 Multicopper-Column interconnects (Source: [24])

1.2.3. Intrinsically Strained Interconnects

The compliant interconnects to be introduced in this part were named intrinsically strained interconnects because of the way they are fabricated and formed – the intrinsic stresses.

The Micro-Spring [25], J-spring[26] and Stress-Engineered compliant interconnect [27] are fabricated essentially using the same method – the stress-engineered thin film fabrication process. The molybdenumchromium (MoCr) with a large stress gradient (≈ 2GPa/µm) was used as the stressed spring metal because of its high yield stress. An adhesive layer is first deposited onto the substrate to enhance the adhesion between the stressed metal and the substrate. This adhesive layer is to be partially removed after the entire fabrication process. The MoCr is then sputtered onto the adhesive layer, during which the pressure in the sputtering chamber is adjusted to form the intrinsic stress within the MoCr. The adhesive layer is then selectively etched to release the stressed metal which curls up to form the compliant interconnects. Those released compliant interconnects can be sputtered with conductive metal layer to improve the electrical performance and mechanical strength.

The Smart Three Axis compliant interconnect [28] is fabricated by using two disimilar metals with different coefficients of thermal expansion (CTE's) to form the intrinsic stresses. These two metal layers with different CTE's, when fabricated under

certain different tempratures, expend differently and therefore form the curled shape of the compliant interconnect.

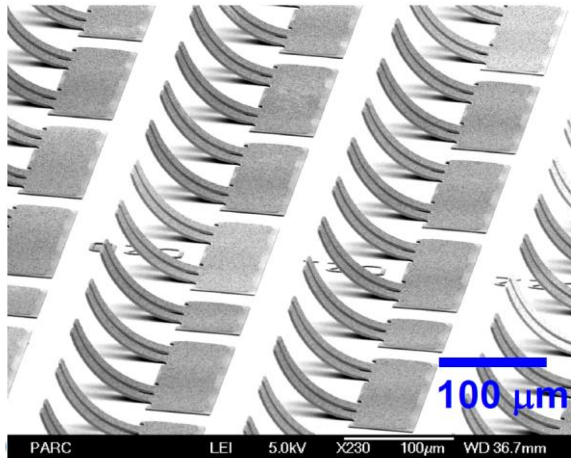


Figure 1-13 Micro-Spring interconnects (Source: [25])

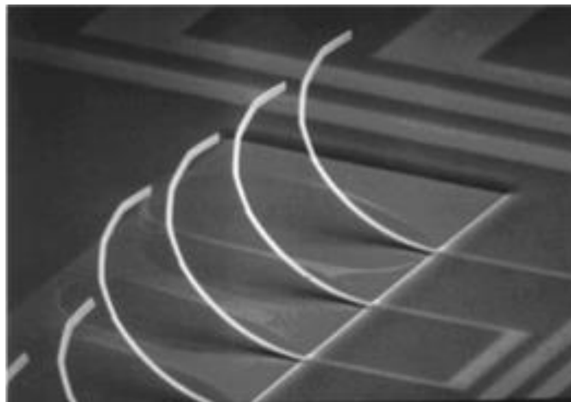


Figure 1-14 J-Springs (Source: [26])

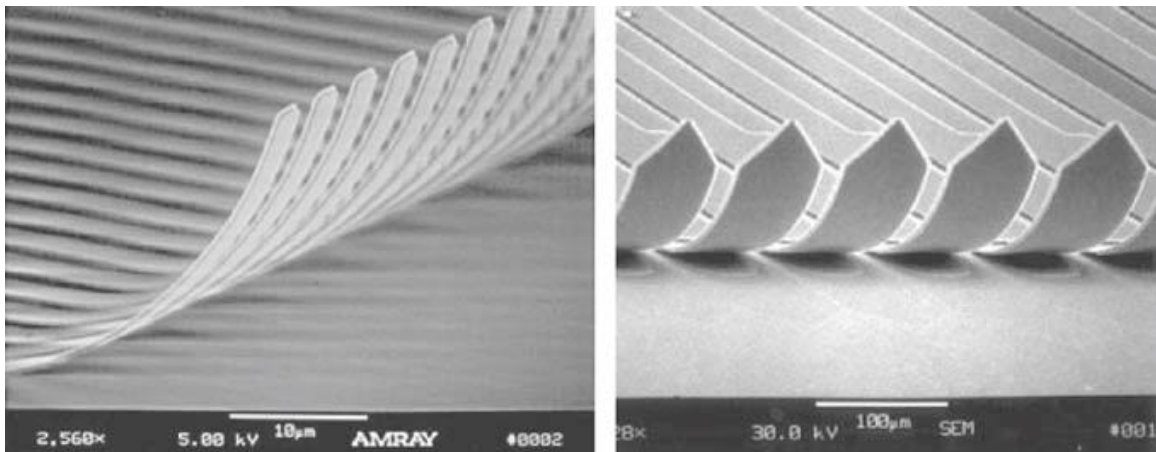


Figure 1-15 Stress-Engineered compliant interconnects (Source: [27])

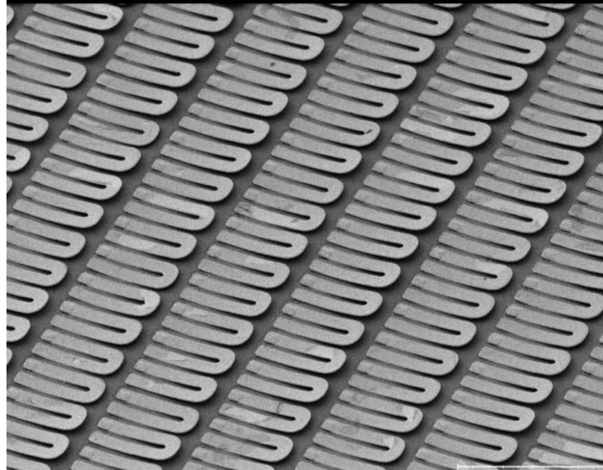


Figure 1-16 Smart Three Axis Compliant Interconnect (Source: [28])

The intrinsically strained interconnects are very compliant due to their long slender geometries. But the weakness of these long slender shapes is that it also results in the longest electric path and thus highest resistance of all the types of the compliant interconnects. Moreover, this type of compliant interconnects use simple contact to the substrate pad for the assembly which is less reliable unless an adhesive is used, and the contact approach increases the electric resistance as well.

1.2.4. Free-standing interconnects

The compliant interconnects categorized in this group have free-standing structures and complex curvilinear structure in the 3-dimentional space. This is different from the pillar-strutures that do not have free-standing geometry or the instrinsically strained interconnects that only have curvilinear structure in one plane. However, becaue of the complexity of the structure, they are inferior to the copper pillar bumps or the nano-pillar interconnects in the aspect of scalability. The following are the major free-standing interconnects pursued recently.

1.2.4.1. Wide Area Vertical Expansion Interconnect

The "Wide Area Vertical Expansion" (WAVE) interconnects developed by Tessera [29, 30] places a low modulus and low CTE encapsulant between the die and the

substrate to mechanically decouple the die from the substrate to a certain extent. This encapsulant encapsulates the flexible copper leads interconnecting the die and the substrate. The gap distance bteween the die and the substrate is set in the range of 100µm to 150µm. The WAVE interconnects show very good reliability under the thermal cycling tests due to the protection of the encapsulant. However, the assembly process involves more steps than those of other compliant interconects and the copper leads increase the electrical path and thus reduce the electrical performance.

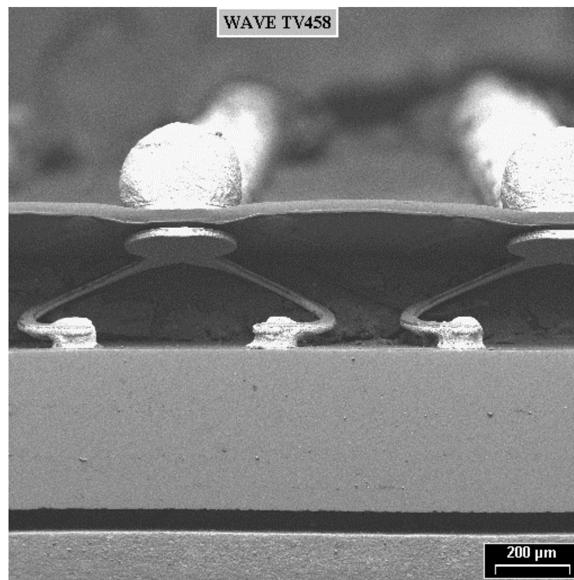


Figure 1-17 Wide Area Vertical Expansion (Source: [31])

1.2.4.2. <u>Sea of Leads</u>

The Sea of leads [32, 33] technology extends the BEOL process to fabricate the interconnects in high I/O density at the wafer level [32], which involves relatively less fabrication steps than the other types of compliant interconnects. A sacrificial layer, usually made of photoresist, Al thin-film or thermally decomposal polymer film, is first deposited and patterned, followed by the deposition of the Ti/Cu seed layer. Metal leads are then electroplated after a photoresist layer is patterned. A UBM layer and the solder bump are then electroplated. Lastly, the sacrificial layer is removed to release the leads.

The major drawbacks of this compliant interconnect are 1) the long elecric path affects the electrical performance; 2) the in-plane compliance value is orientation dependent so they must be properly oriented in order to achieve a better reliability under different applications.

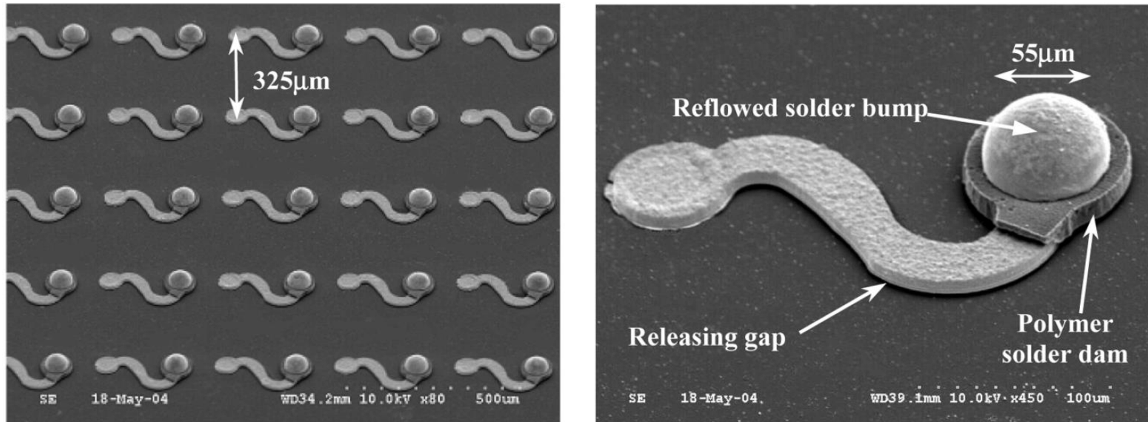


Figure 1-18 Sea of Leads (Source: [33])

1.2.4.3. <u>Serial Operation Interconnects</u>

The MicroSpring on silicon technology introduced by FormFactor [34] and the Microcoil Spring developed by NASA [35] are the two representative 3D compliant interconeccts fabricated via serial operation. The MicroSpring interconnects are fabricated directly on the silicon wafer using wire-bonding. This is very time-consuming if high I/O count is required, although they are less expansive to produce. The Microcoil Spring interconnects are fabricated using actual springs made from beryllium copper wire. The reported data shows that Microcoil Spring interconnect has very high characteristic life under the thermal cycling tests and vibration tests, owing to its long spring shape that provides very high in-plane and out-of plane compliance values. But it cannot scale in pitch and its extremely long electrical path leads to high electrical parasitcs. The serial fabrication also makes it time-consuming for the high volume manufacturing. In addition, it has relatively high self inductance due to the helix geometry.

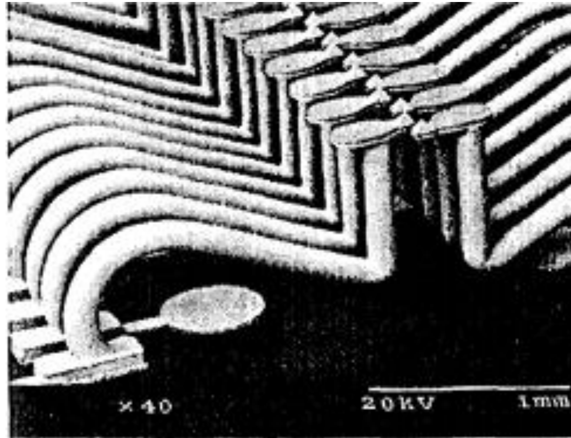


Figure 1-19 MicroSpring on silicon technology (Source: [34])

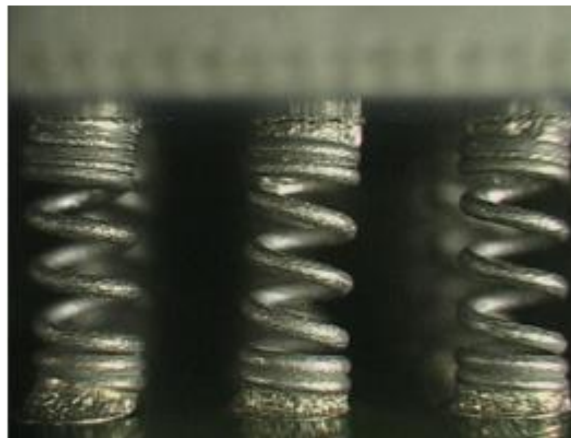


Figure 1-20 Microcoil Spring Interconnection (Source: [35])

1.2.4.4. G-Helix, β-Helix and Flexconnect

G-Helix interconnect [36], β-Helix interconnect [37] and Flexconnect [38] are compliant free-standing structures pursued at Georgia Tech with similar fabrication methods at the wafer level. A Ti/Cu seed layer is first deposited on the wafer, and a photoresist is applied and exposed to form the patterns for the first layer of the geometry – the post that provides the stand-off for the out-of-plane deformation. This is followed by the electroplating of the copper. Then, a second seed layer is deposited and a second photoresist layer is applied and patterned for the arcuate beam structure shown in Figure 1-21 to Figure 1-23. The copper is then electroplated to form the arcuate geometry. Depending on the number of layers of the compliant interconnect structure in ther vertical

direction, this seed layer-photolithography-electroplating process may be repeated multiple times. The solder balls are electroplated lastly for assembly, followed by the removing of the photoresist to release the interconnects.

It can be seen from Figure 1-21 to Figure 1-23 that the G-Helix interconnect and the Flexconnects have less layers than the β-Helix interconnect, and therefore less fabrication steps. However, the β-Helix interconnect, owing to its longer helix shape in the vertical direction, has higher compliance leading to better mechanical reliability. Among these three designs, the Flexconnects has the best electrical performance because its dual path design reduces the electrical resistance. The β-Helix interconnect which is inversely affected by its longer helix shape has the worst electrical performance. This group of compliant interconnects also have the same weakness as the other compliant interconnects introduced above – the in-plane compliance value is different in different directions.

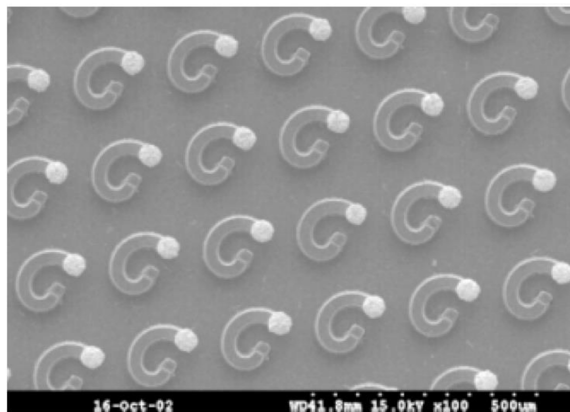


Figure 1-21 G-Helix (Source: [36])

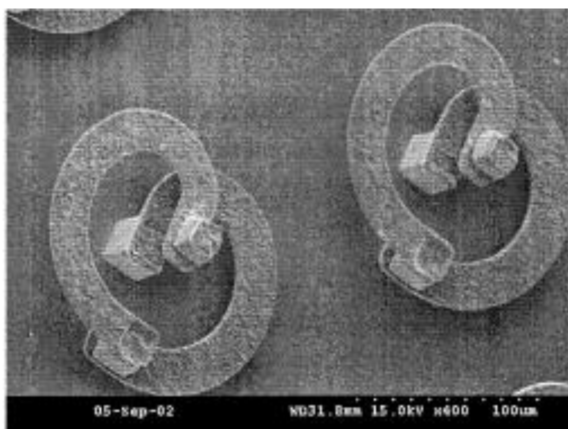


Figure 1-22 β-Helix (Source: [37])

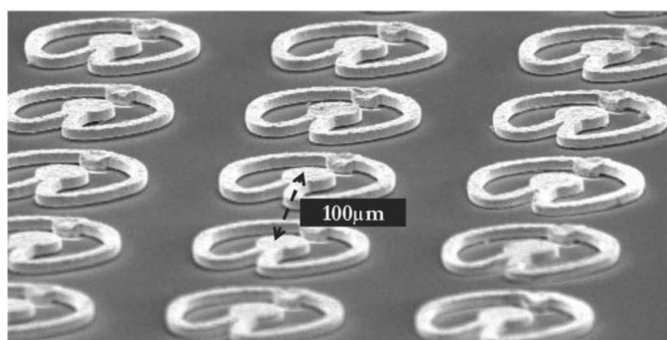


Figure 1-23 FlexConnects (Source: [39])

1.3. CONCLUSION

Compliant interconnects can decouple the die from the substrate or the substrate from the board, but their electrical performance is inferior to those of solder bumps. This is because the compliant interconnects have longer path and narrower cross-section than typical solder bumps used in microelectronic packaging. Any geometry improvement that enhances the mechanical compliance will also adversely affect the electrical performance. A number of different types of compliant interconnect have been pursued by several researchers. These interconnects have one or more of the following limitations: high electrical parasitics, low in-plane and out-of-plane compliance, inadequate thermo-mechanical reliability, extensive processing steps, non-standard processing steps, difficult assembly, non-uniformity, sequential processing, non-scalability, etc. The 3-Arc-Fan

compliant interconnects have been pursued in Georgia Tech. They have three electrical paths from the die pad to the solder ball to the substrate pad. Thus, these 3-Arc-Fan compliant interconnects can increase the mechanical compliance but also provide relatively good electrical characteristics.

CHAPTER 2 OBJECTIVES AND SCOPE OF THE RESEARCH

2.1. RESEARCH GAPS AND NEEDS

Based on the review of various kinds of compliant interconnects pursued by different researchers, there are several important gaps in the existing research on the second-level compliant interconnect technology:

- Compliant Interconnects, pursued in industry and academia, are primarily for first-level interconnections
    - There is a need to develop second-level compliant interconnects
- No systematic multi-physics design optimization and fabrication has been reported in literature
    - There is a need to perform systematic multi-physics optimization of compliant interconnects, and to fabricate such compliant interconnects
- Compliant interconnects, pursued so far, are typically fabricated in class 10 or 100 cleanroom, making them expensive
    - There is a need to explore less expensive fabrication of compliant interconnects in Class 1000 cleanroom
- Assembly of area-array compliant interconnects has not been adequately studied in open literature
    - There is a need to develop repeatable, easy-to-use assembly process steps for compliant interconnects
- Experimental assessment of thermal cycling reliability of compliant interconnect assemblies is rare in literature; even rarer for second-level area-array assemblies. And the compliant interconnects have not been demonstrated for multi-die stack 3D microelectronic packages

    - There is a need to study thermo-mechanical reliability of second-level compliant interconnect for 3D multi-die stack assemblies through experiments as well as simulations
- Although the compliant interconnects address thermo-mechanical reliability, there is not enough information on the response of compliant interconnects when subjected to impact and drop loads.
    - There is a compelling need to demonstrate that the area-array of compliant interconnects can be used as impact isolator as well as assess the reliability of compliant interconnects under drop-impact loads

2.2. OBJECTIVES AND SCOPES OF THE RESEARCH

The primary objectives of this research are to 1) develop second-level compliant interconnects by performing compliance analysis and multi-physics design optimization; 2) present the compliance values for the 3-Arc-Fan compliant interconnects using analytical formulations and finite-element simulations and validate these values against experimental data; 3) examine design variables to balance mechanical and electrical performance metrics of the 3-Arc-Fan compliant interconnects, and construct response surfaces for electrical resistance, inductance, as well as von Mises strain, and finally optimize the design variables using specified design and processing constraints as well as the ranges of the design variables; 4) fabricate the interconnects using cost-effective fabrication process; 5) assemble the substrate to the board and develop the guideline for the reliable assembly process, 6) study the thermo-mechanical reliability of the compliant interconnects in multi-layer substrates under thermal cycling tests; 7) perform drop-test experiments and simulations for both scaled-up prototypes of the 3-Arc-Fan compliant interconnects and the true scale interconnects to demonstrate that the developed interconnects can function as impact isolators, and compare with those of the assembly with BGA as the interconnection; 8) investigate the reliability of the 3-Arc-Fan compliant

interconnects subjected to the impact loads. Based on these objectives, the scopes of this research are organized as follows.

2.2.1. Development of Second-Level Compliant Interconnects

The second-level compliant interconnects are developed by performing compliance analysis and systematic multi-physics design optimization.

2.2.1.1. Analytical and Finite-Element Models for Compliance Analysis

The 3-Arc-Fan compliant interconnects are intended to mechanically decouple the substrate from the board, and the high mechanical compliance of the 3-Arc-Fan interconnects in the in-plane and out-of-plane directions (4-5 orders greater than the solder ball) is the essential reason that the compliant interconnects are the potential replacement for the solder balls in many fields. Therefore, it is important to determine the mechanical compliance of the structures in the three orthogonal directions. In this research, we present the compliance values for the 3-Arc-Fan interconnects using analytical formulations and finite-element simulations and compare these values against experimental data. The analytical solutions are based on Euler-Bernoulli beam assumptions and Castigliano's second theorem, and give an insight into how the geometry parameters affect the compliance values, which is critical to the structural optimization design in the next step. The finite-element models are built using both beam elements and 3D solid elements.

2.2.1.2. Multi-Physics Design Optimization

It is found that any geometry improvement that enhances the mechanical compliance will also adversely affect the electrical performance. Thus, the design of a compliant interconnect is a trade-off between the mechanical and electrical performance. In this research, we examine eight design variables to balance mechanical and electrical performance metrics of a 3-Arc-Fan compliant interconnect. These design variables are appropriately reduced to four and normalized. The response surfaces are constructed for

electrical resistance, inductance, and von Mises strains using the Central Composite Inscribed (CCI) design points. The Method of Global Criterion is used to scalarize this multi-objective optimization problem, and an optimization is done using specified design and processing constraints as well as the ranges of the design variables.

2.2.2. Fabrication and Assembly

An area-array of 3-Arc-Fan compliant interconnects are fabricated on a 6-inch silicon wafer using sequential processes in Class 1000 cleanroom which is less expensive. The design consists of about 2000 compliant interconnects at a 400-μm pitch on each 18mm×18mm silicon substrate, and there are 32 substrates on a 6-inch wafer. Dupont™ Riston® FX920 (thickness = 20μm) negative dry-film photoresist is used in our study and the arcuate beam thickness is uniform throughout the pattern. The 3-Arc-Fan compliant interconnects with arcuate beam width equal to 10μm, 15μm, and 20μm are fabricated simultaneously on the same silicon wafer, and their out-of-plane compliance values are measured and compared against the simulation results.

The silicon substrate with the fabricated compliant interconnects are assembled on an organic board using flip-chip bonding. The appropriate compression force or the spacer thickness is calculated and a proper flux type is selected. The assembled samples are inspected via non-destructive methods, visual examination under X-ray and electrical measurement using designed daisy chains to ensure the integrity of the assembly.

2.2.3. Assessment of Thermo-mechanical Reliability

The thermo-mechanical reliability of the 3-Arc-Fan compliant interconnects subjected to the JEDEC standard thermal cycling tests is investigated. The test condition G with T_{min} = -40°C and T_{max} = 125°C is applied. Relatively thicker silicon substrates are used to represent the multi-layer substrates or die stacks. The tests are run in a thermal cycle chamber and electrical resistance of daisy-chained interconnects of each package on the test board is monitored to detect the failure. The samples are examined using Dage

X-Ray XD7600NT® once the resistance change is detected in order to track the status of the arcuate beams.

The fatigue lives of the samples with the arcuate beam width of the compliant interconnects equal to 10μm, 15μm, and 20μm are recorded and compared. The finite-element simulations based on the strip models are carried out in ANSYS® to validate the experiments.

2.2.4. Impact Isolation

As a first step, the scaled-up polymer interconnects are examined through experiments and simulations. The simulations are based on Input-G method and performed using ANSYS® finite-element software. The samples are subjected to a simulated impact from varying drop heights. In parallel to the simulations, scaled-up polymer prototypes of the compliant interconnects are fabricated. 3D printing is used to fabricate an area-array of compliant interconnects, along with polymer die and polymer substrate which also serves as the board, as a quick low-cost alternative to cleanroom fabrication. The prototype of the assembly is subjected to drop tests from varying drop heights. The response of the assembly during drop testing is captured using strain gauges and mounted accelerometer. The data from the experiments are compared with the predictions from the simulations.

Then, the actual silicon substrates with copper compliant interconnects are assembled on organic boards. The assemblies are categorized according to the arcuate beam width of the 3-Arc-Fan compliant interconnects, equal to 10μm, 15μm, and 20μm. The overall design is based on the JEDEC standard for the board-level drop test. The assemblies are subjected to drop tests from varying drop heights and the response is captured using strain gauges and mounted accelerometer. The data from the experiments are compared with the simulations calculated using Input-G method. The finite-element models are simplified by replacing the 3-Arc-Fan compliant interconnects with equivalent orthotropic columns. The results obtained for the assemblies with different

arcuate beam width are compared against each other as well as those of the assembly with BGA as the interconnection.

2.2.5. Assessment of Drop Test Reliability

The samples assembled based on the JEDEC standard for the board-level drop test are subjected to drop tests at a particular drop height. The samples are daisy chained at the four corners which are the most critical locations. Each daisy chain at the corner connects 4×4 3-Arc-Fan compliant interconnects. The resistance of the daisy chains is measured and logged after one or more drop events. The samples are inspected in the X-ray to track the breakage of the compliant interconnects. The fatigue lives of the 3-Arc-Fan compliant interconnects with arcuate beam width equal to 10μm, 15μm, and 20μm under the drop test are recorded and compared. The simulations performed using ANSYS® based on Input-G method are carried out to validate the experiments.

CHAPTER 3 DEVELOPMENT OF ANALYTICAL AND FINITE-ELEMENT MODELS FOR COMPLIANCE ANALYSIS

3.1. INTRODUCTION

The interconnects with multiple paths have redundant electrical paths, increased compliance, and reduced electrical parasitics. This chapter presents evidence to support novel interconnect designs that make use of three parallel paths, where each path has an independent anchoring post. The results obtained from numerical simulations (both three dimensional solid models and one dimensional beam models), analytical solutions as well as scaled polymer prototype testing match perfectly and support the designs.

Decoupling the die from the substrate or the substrate from the board by means of mechanically compliant interconnects would reduce stresses created by the coefficient of thermal expansion mismatch. A decoupled die-substrate or substrate-board interface would allow the different components to expand or contract differently without inducing high stresses in the components [40]. Multi-path fan-shaped interconnect has several electrical paths from the die pad to the solder ball to the substrate pad. The scaled-up stereolithography-based prototypes shown in Figure 3-1 and Figure 3-2 are examples, and are only to illustrate the geometric features of the interconnects.

Figure 3-1 Scaled-up polymer version of the 2-Arc Fan Interconnect with second-order splines: 3-D rendering (left) and top view (right)

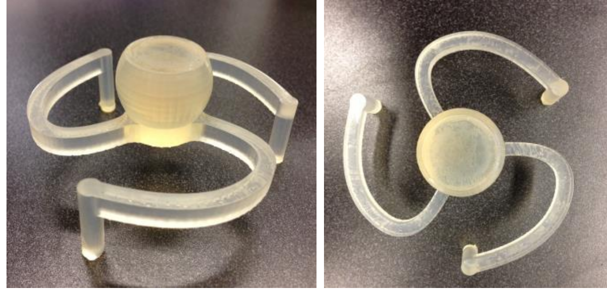


Figure 3-2 Scaled-up polymer version of the 3-Arc Fan Interconnect with second-order splines: 3-D rendering (left) and top view of the arc layout (right)

As seen in the images, the vertical posts are attached onto the surface, while the arcuate structures are parallel to the surface. The pad and solder ball are shown at the center of the compliant interconnect. This solder will be used to make permanent bonding to the substrate pad through reflow process. The interconnects, as shown in Figure 1, can be fabricated on a wafer through cleanroom LIGA-like process.

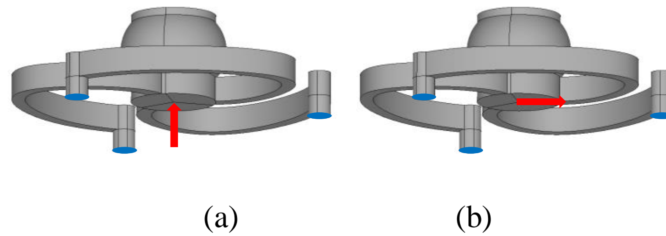
3.2. FINITE-ELEMENT ANALYSIS

The compliant interconnects are intended to mechanically decouple the die from the substrate, and therefore, it is essential to determine the mechanical compliance of the structures in the three orthogonal directions. As a first-step, the compliance in the three directions was determined using ANSYS® employing solid elements as well as beam elements.

3.2.1. Simulations using Solid Elements

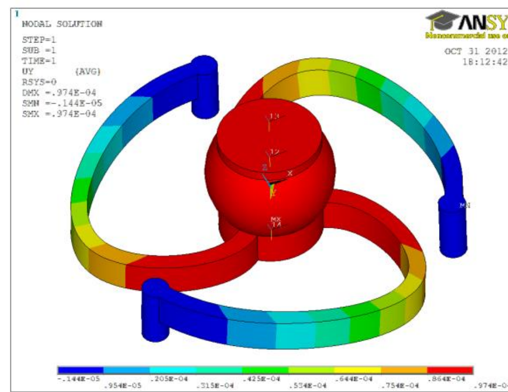
The bottom of the interconnect posts highlighted in blue (where the posts will touch the die pad) was fixed in all directions, and a unit force was applied at the pad center highlighted in red as illustrated in Figure 3-3. Figure 3-3 (a) shows the loading used for the out-of-plane compliance calculation. Figure 3-3 (b) shows the in-plane loading in one direction to determine the in-plane compliance. Similarly, load was applied in the other in-plane direction, orthogonal to the first in-plane direction, to

determine the compliance in the second in-plane direction. In any of these simulations, only one unit force was applied.

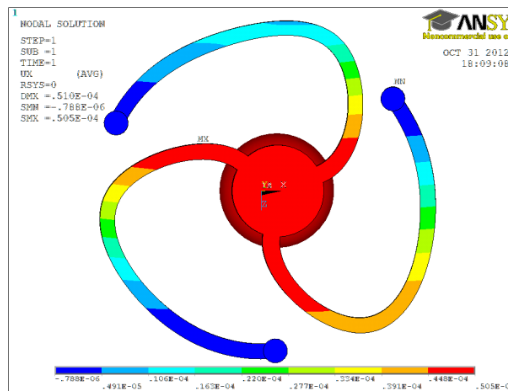


(a) (b)

Figure 3-3 The left image shows direction of application of out-of-plane load, while the in-plane is depicted in the right image.



(a)



(b)

Figure 3-4 Contour plot of the nodal displacement in *m* for the 3D solid models; (a). out-of-plane displacement (b). first in-plane displacement

The displacement in the direction of the applied force was determined through the simulations, and thus, the compliance in a particular direction could be computed by dividing the displacement by the force [36, 40]. Figure 3-4 a) shows the out-of-plane displacement contours in *m*, and Figure 3-4 b) shows the first in-plane displacement contours. As seen, the out-of-plane displacements are symmetric about the center of the solder pad, and thus, the out-of-plane simulations can be carried out using just one of the arcuate beams. Figure 3-5 shows the out-of-plane displacement contours for the model with only one of the arcuate beams. Note that the compliance value obtained in Figure 3-5 should be divided by three in order to take into account the effect of the other two arcuate beams.

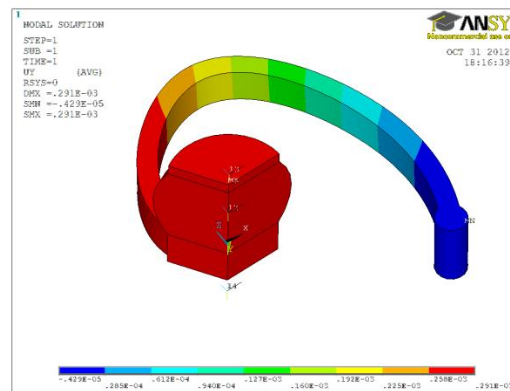


Figure 3-5 Contour plot of the nodal solution of the out-of-plane displacement in *m* for the 1/3rd symmetric 3D solid model. The pad and solder only have out-of-plane translation.

3.2.2. Simulations using Beam Elements

Compliance was determined in two orthogonal in-plane axes, and also in the out-of-plan axis. Although 3D solid models give very accurate results, they are computationally expensive, especially when we analyze a packaging assembly consisting of several compliant interconnects. Therefore, simplified beam models were developed. Figure 3-6 shows the simplified beam models corresponding to Figure 3-3, while Figure 3-7 is the simplified beam model for the out-of-plane simulation using just one of the

three arcuate beams. Those in green represent the pad and solder ball with the Young's Modulus set to be very large. The reason is that the bulk shape makes them much stiffer than other parts. Figure 3-8 a) shows the out-of-plane displacement contours, and Figure 3-8 b) shows the first in-plane displacement contours. Figure 3-9 shows the out-of-plane displacement contours for the model with only one of the arcuate beams.

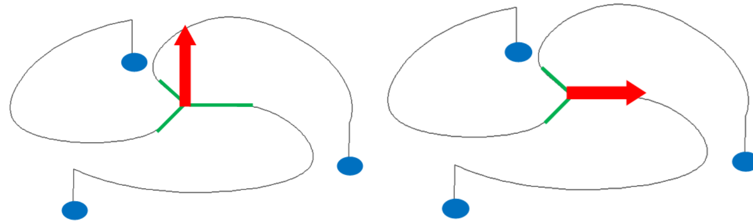


Figure 3-6 Beam models for the out-of-plane and in-plane compliance analyses.

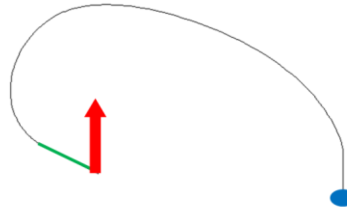
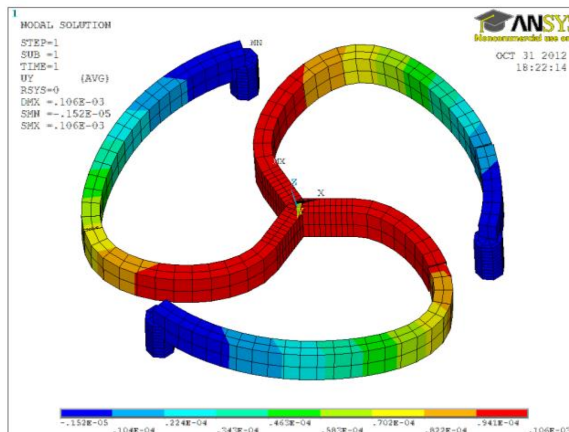
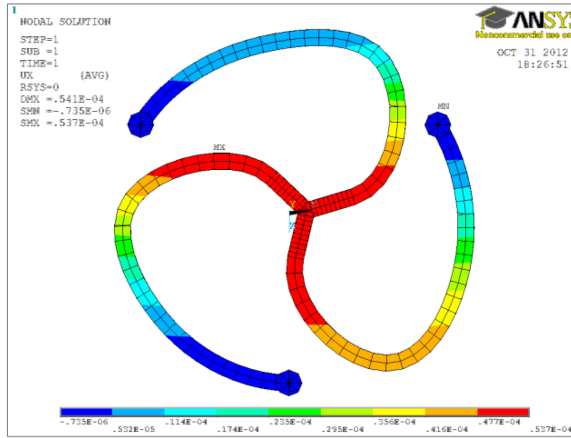


Figure 3-7 Simplified one dimensional beam model for the out-of-plane compliance analysis. The point where the load is applied and the green part only have out-of-plane translation.



(a)



(b)

Figure 3-8 Contour plot of the nodal displacement in *m* for the simplified beam models (a). out-of-plane displacement (b). first in-plane displacement

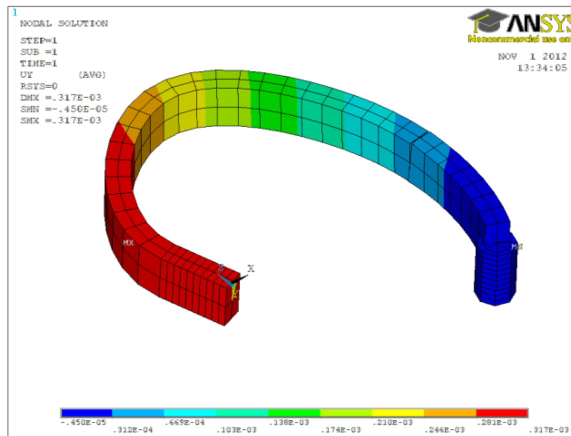


Figure 3-9 Contour plot of the nodal solution of the out-of-plane displacement in *m* for the Simplified beam model.

3.3. ANALYTICAL SOLUTIONS

To determine the compliance values of this hyperstatic interconnect system, the Castigliano's second theorem was applied, which states that for a linearly elastic structure, the prescribed deflection at a point is given by the partial derivative of the strain energy with respect to the driving force. Here are some notations used consistently in the following analysis: $\vec{a}$ represents a vector, while a is the scalar part; $\left(\vec{a},\vec{b}\right)$ is the dot

product of vector $\vec{a}$ and vector $\vec{b}$, and $\vec{a}\otimes\vec{b}$ is the cross product of $\vec{a}$ and $\vec{b}$; the superscripts of the bending moments and torsions indicate the forces by which those terms are induced; the subscript "*a*" represents "arcuate beam", while "*p*" represents "post".

3.3.1. Out-Of-Plane Compliance Analysis

For the analysis of the out-of-plane compliance value, only one third of the structure was modeled, and the end of the arcuate beam which is attached to the solder bump can only move vertically, without any rotation or in-plane translation, because of the symmetry. The free body diagram and the notations are shown in Figure 3-10. z is the out-of-plane axis, while x and y are in-plane axes. $\vec{i}$, $\vec{j}$ and $\vec{k}$ are unit vectors in x, y and z directions, respectively. $\vec{i}'$ is the unit vector along the tangential direction of the arcuate beam, and $\vec{j}'$ is the other in-plane unit vector normal to $\vec{i}'$. $\vec{r}=(k-x)\vec{i}+(l-y)\vec{j}=\left(\vec{r},\vec{i}'\right)\vec{i}'+\left(\vec{r},\vec{j}'\right)\vec{j}'$ is the vector pointing from P to D.

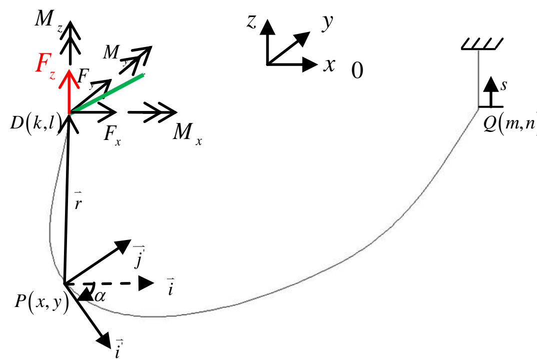


Figure 3-10 Free body diagram of 1/3rd of the interconnect subjected to out-of-plane force F_z. Since the green part is rigid and only has out-of-plane translation, it is reasonable to move F_z and the constraints to *D*, the end of the arcuate beam which is attached to the rigid part, without affecting the results. The arcuate beam is in the *x*-*y* plane while the post is along *z*-direction. *s* is the curvilinear coordinate along the post.

The structure is statically indeterminate. Remove the constraints at the end of the beam and replace them with F_x, F_y, M_x, M_y and M_z which constrain the translation in x and y axes, the rotation along x, y and z axes, respectively. This is a system of 5 degree of redundancy. 5 equations are required to solve for these 5 unknowns, and can be obtained from Castigliano's second theorem.

The bending moment applying at the arcuate beam due to F_x is:

$$\overrightarrow{M_a^{F_x}} = \vec{r} \otimes \overrightarrow{F_x} = (l-y)\vec{j} \otimes F_x\vec{i} = (y-l)F_x\vec{k} \tag{1}$$

The bending moment applying at the post due to F_x is

$$\overrightarrow{M_p^{F_x}} = \vec{s} \otimes \overrightarrow{F_x} = s\vec{k} \otimes F_x\vec{i} = sF_x\vec{j} \tag{2}$$

where s is the curvilinear coordinate along the post and $s = 0$ at point Q as shown in Figure 7. The torsion applying at the post due to F_x is

$$\overrightarrow{T_p^{F_x}} = (l-n)\vec{j} \otimes F_x\vec{i} = (n-l)F_x\vec{k} \tag{3}$$

The bending moment applied at the arcuate beam due to F_y is:

$$\overrightarrow{M_a^{F_y}} = \vec{r} \otimes \overrightarrow{F_y} = (k-x)\vec{i} \otimes F_y\vec{j} = (k-x)F_y\vec{k} \tag{4}$$

The bending moment applied at the post due to F_y is:

$$\overrightarrow{M_p^{F_y}} = \vec{s} \otimes \overrightarrow{F_y} = s\vec{k} \otimes F_y\vec{j} = -sF_y\vec{i} \tag{5}$$

The torsion applied at the post due to F_y is

$$\overrightarrow{T_p^{F_y}} = (k-m)\vec{i} \otimes F_y\vec{j} = (k-m)F_y\vec{k} \tag{6}$$

The bending moment applied at the arcuate beam due to the external force F_z is

$$\overrightarrow{M_a^{F_z}} = \left(\vec{r},\vec{i'}\right)\vec{i'} \otimes F_z\vec{k} = -\left(\vec{r},\vec{i'}\right)F_z\vec{j'} \tag{7}$$

And the torsion applied at the arcuate beam due to F_z is

$$\overrightarrow{T_a^{F_z}} = \left(\vec{r},\vec{j'}\right)\vec{j'} \otimes F_z\vec{k} = \left(\vec{r},\vec{j'}\right)F_z\vec{i'} \tag{8}$$

The bending moment applied at the post due to F_z is

$$\overrightarrow{M_p^{F_z}} = \left[(k-m)\vec{i} + (l-n)\vec{j} \right] \otimes F_z \vec{k} = (m-k) F_z \vec{j} + (l-n) F_z \vec{i} \tag{9}$$

The reaction moments resolved in the new coordinate system are

$$M_x^{'} = M_x \cos\alpha + M_y \sin\alpha \, ; M_y^{'} = -M_x \sin\alpha + M_y \cos\alpha \tag{10}$$

where $M_x^{'}$ and $M_y^{'}$ are the components in $\vec{i^{'}}$ and $\vec{j^{'}}$ respectively. Summing up all the moment components above leads to the vector forms of the moments applied at the different parts of the interconnect. For the post

$$\overrightarrow{M_p} = \left[M_p^{F_y} + (l-n)F_z + M_x \right]\vec{i} + \left[M_p^{F_x} + (m-k)F_z + M_y \right]\vec{j} + \left[T_p^{F_x} + T_p^{Fy} + M_z \right]\vec{k} \tag{11}$$

For the arcuate beam

$$\overrightarrow{M_a} = \left[T_a^{F_z} + M_x^{'} \right]\vec{i^{'}} + \left[M_a^{F_z} + M_y^{'} \right]\vec{j^{'}} + \left[M_a^{F_x} + M_a^{Fy} + M_z \right]\vec{k} \tag{12}$$

Then, the total potential energy due to the bending moments and torsions is

$$\begin{aligned} U = & \int \frac{\left[M_p^{F_y} + (l-n)F_z + M_x \right]^2}{2H_{11}^p} ds + \int \frac{\left[M_p^{F_x} + (m-k)F_z + M_y \right]^2}{2H_{22}^p} ds + \int \frac{\left[T_p^{F_x} + T_p^{Fy} + M_z \right]^2}{2H_{33}^p} ds \\ & + \int \frac{\left[T_a^{F_z} + M_x^{'} \right]^2}{2H_{11}^a} d\eta + \int \frac{\left[M_a^{F_z} + M_y^{'} \right]^2}{2H_{22}^a} d\eta + \int \frac{\left[M_a^{F_x} + M_a^{Fy} + M_z \right]^2}{2H_{33}^a} d\eta \end{aligned} \tag{13}$$

where *s* is the curvilinear coordinate along the post and $s = 0$ at point *Q*; η is the curvilinear along the arcuate beam and $d\eta = \sqrt{dx^2 + dy^2}$; the superscripts of the bending moments and torsions indicate the forces by which those terms are induced; H_{11}^p and H_{22}^p are the bending stiffness of the post about axes $\vec{i}$ and $\vec{j}$, while H_{33}^p is the torsional stiffness of the post; H_{22}^a and H_{33}^a are the bending stiffness of the arcuate beam about axes $\vec{j^{'}}$ and $\vec{k}$, while H_{11}^a is the torsional stiffness of the arcuate beam. The constraints that the end of the arcuate beam which attached to the solder bump can only move vertically, without any rotation or in-plane translation, imply that $\frac{\partial U}{\partial F_x} = \frac{\partial U}{\partial F_y} = \frac{\partial U}{\partial M_x} = \frac{\partial U}{\partial M_y} = \frac{\partial U}{\partial M_z} = 0$, according to the Castigliano's second theorem. So

the 5 unknowns can be solved in terms of F_z, by using these 5 equations. After that we can obtain $U = U(F_z)$, and the compliance value can be calculated from

$$C_z = \frac{\delta}{F_z} = \frac{\partial U}{\partial F_z} \Big/ F_z \tag{14}$$

3.3.2. In-Plane Compliance Analysis

The analyses of the in-plane compliance values of this 3-arc fan interconnect is more complicated than the out-of-plane case, because the symmetry is no longer valid and the whole structure must be analyzed, which makes it as a system of 12 degrees of redundancy (all of the three posts are clamped, introducing 18 unknown reaction forces/moments with only 6 equilibrium equations available). Release the constraints at posts A and B then replace them with the reaction forces/moments as shown in Figure 3-11.

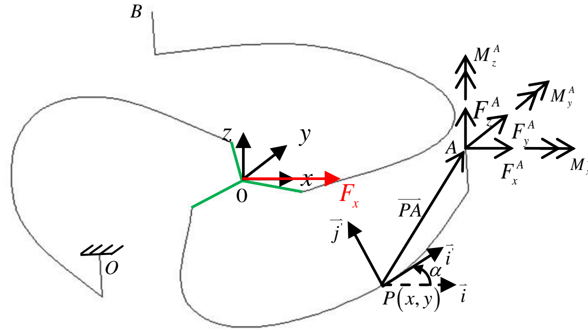


Figure 3-11 Free body diagram of the interconnect suffering in-plane force F_x. The constraints at points A and B are released and replaced with the reaction forces/moments. Only the reaction forces/moments at point A are drawn because those at point B are the same and following the same analysis procedure. These three paths are called O, A and B.

First, consider the effects of the reaction force F_x^A applied at point A. The moment applied at the post A is $s_A \vec{k} \otimes F_x^A \vec{i} = s_A F_x^A \vec{j}$ (s_A is the curvilinear coordinate along post A and $s_A = 0$ at point A); the moment applied at beams A and O is $\left(L\vec{k} + \overrightarrow{r_2^A}\right) \otimes F_x^A \vec{i} = LF_x^A \vec{j} - r_2^A F_x^A \vec{k}$ (L is the length of the posts and $r_2^A = y(A) - y$); the

moment and torsion applied at the post O are $s_O\vec{k}\otimes F_x^A\vec{i}=s_O F_x^A\vec{j}$ (s_o is the curvilinear coordinate along post O and s_o = 0 at point O) and $\left[y(A)-y(O)\right]\vec{j}\otimes F_x^A\vec{i}=\left[y(O)-y(A)\right]F_x^A\vec{k}$, respectively. F_x^A does not contribute any moments/torsions at post B or beam B.

Secondly, consider the effects of the reaction force F_y^A applied at point A. The moment applied at post A is $s_A\vec{k}\otimes F_y^A\vec{j}=-s_A F_y^A\vec{i}$; the moment applied at beams A and O is $\left(L\vec{k}+\overrightarrow{r_1^A}\right)\otimes F_y^A\vec{j}=-LF_x^A\vec{i}+r_1^A F_y^A\vec{k}$ ($r_1^A=x(A)-x$); the moment and torsion applied at the post O are $s_O\vec{k}\otimes F_y^A\vec{j}=-s_O F_y^A\vec{i}$ and $\left[x(A)-x(O)\right]\vec{i}\otimes F_y^A\vec{j}=\left[x(A)-x(O)\right]F_y^A\vec{k}$, respectively. F_y^A does not contribute any moments/torsions at post B or beam B.

Thirdly, consider the effects of the reaction force F_z^A applied at point A. The moment and torsion applied at beams A and O are $r_a^A\vec{i'}\otimes F_z^A\vec{k}=-r_a^A F_z^A\vec{j'}$ and $r_b^A\vec{j'}\otimes F_z^A\vec{k}=r_b^A F_z^A\vec{i'}$, respectively, where $r_a^A=\left(\overline{PA},\vec{i'}\right)$ and $r_b^A=\left(\overline{PA},\vec{j'}\right)$ are the projection of $\overrightarrow{PA}$ in $\vec{i'}$ and $\vec{j'}$; the moment applied at post O is

$$\left[\left(y(A)-y(O)\right)\vec{j}+\left(x(A)-x(O)\right)\vec{i}\right]\otimes F_z^A\vec{k}=\left[y(A)-y(O)\right]F_z^A\vec{i}-\left[x(A)-x(O)\right]F_z^A\vec{j}.$$

Then, consider the effects of reaction moments M_x^A, M_y^A and M_z^A applied at point *A*. The moment applied at posts O and A is $M_x^A\vec{i}+M_y^A\vec{j}+M_z^A\vec{k}$; the moment applied at beams *O* and *A* is $\left(M_x^A\cos\alpha+M_y^A\sin\alpha\right)\vec{i'}+\left(-M_x^A\sin\alpha+M_y^A\cos\alpha\right)\vec{j'}+M_z^A\vec{k}$, which are resolved in the new coordinate system. M_x^A, M_y^A and M_z^A do not contribute any moments/torsions at post *B* or beam *B*.

Following the same procedure gives us the contribution of the reaction forces/moments at point *B* to the interconnect, and all of the corresponding components

are denoted with the superscript B. Since both the posts A and B are released and the reaction forces/moments are applied, the external force F_x have only effects on the post O and beam O. The moment applied at the beam O due to F_x is $-y\vec{j}\otimes F_x\vec{i}=yF_x\vec{k}$, and that applied at the post O is $-y(O)\vec{j}\otimes F_x\vec{i}+(s_O-L)\vec{k}\otimes F_x\vec{i}=y(O)F_x\vec{k}+(s_O-L)F_x\vec{j}$

Then, we can obtain the total moments applied at the interconnect by summing up all of the components contributed by the 12 reaction forces/moments and external force F_x.

The moment applied at the post A is

$$\overrightarrow{M_p^A}=s_AF_x^A\vec{j}-s_AF_y^A\vec{i}+M_x^A\vec{i}+M_y^A\vec{j}+M_z^A\vec{k}=\left(M_x^A-s_AF_y^A\right)\vec{i}+\left(M_y^A+s_AF_x^A\right)\vec{j}+M_z^A\vec{k} \quad (15)$$

The moment applied at the post B is

$$\overrightarrow{M_p^B}=s_BF_x^B\vec{j}-s_BF_y^B\vec{i}+M_x^B\vec{i}+M_y^B\vec{j}+M_z^B\vec{k}=\left(M_x^B-s_BF_y^B\right)\vec{i}+\left(M_y^B+s_BF_x^B\right)\vec{j}+M_z^B\vec{k} \quad (16)$$

The moment applied at the post O is

$$\begin{aligned}\overrightarrow{M_p^O}&=\left[y(O)-y(A)\right]F_x^A\vec{k}+s_OF_x^A\vec{j}+\left[x(A)-x(O)\right]F_y^A\vec{k}-s_OF_y^A\vec{i}\\&+\left[y(A)-y(O)\right]F_z^A\vec{i}-\left[x(A)-x(O)\right]F_z^A\vec{j}+M_x^A\vec{i}+M_y^A\vec{j}+M_z^A\vec{k}\\&+\left[y(O)-y(B)\right]F_x^B\vec{k}+s_OF_x^B\vec{j}+\left[x(B)-x(O)\right]F_y^B\vec{k}-s_OF_y^B\vec{i}+\left[y(B)-y(O)\right]F_z^B\vec{i}\\&-\left[x(B)-x(O)\right]F_z^B\vec{j}+M_x^A\vec{i}+M_y^A\vec{j}+M_z^A\vec{k}+y(O)F_x\vec{k}+(s_o-L)F_x\vec{j}\end{aligned} \quad (17)$$

The moment applied at the arcuate beam A is

$$\begin{aligned}\overrightarrow{M_a^A}&=LF_x^A\vec{j}-r_2^AF_x^A\vec{k}-LF_y^A\vec{i}+r_1^AF_y^A\vec{k}-r_a^AF_z^A\vec{j}+r_b^AF_z^A\vec{i}\\&+\left(M_x^A\cos\alpha+M_y^A\sin\alpha\right)\vec{i}+\left(-M_x^A\sin\alpha+M_y^A\cos\alpha\right)\vec{j}+M_z^A\vec{k}\\&=\left[\left(-LF_y^A+M_x^A\right)\cos\alpha+\left(LF_x^A+M_y^A\right)\sin\alpha+r_b^AF_z^A\right]\vec{i}\\&+\left[-\left(-LF_y^A+M_x^A\right)\sin\alpha+\left(LF_x^A+M_y^A\right)\cos\alpha-r_a^AF_z^A\right]\vec{j}+\left[M_z^A-r_2^AF_x^A+r_1^AF_y^A\right]\vec{k}\end{aligned} \quad (18)$$

The moment applied at the arcuate beam B is

$$\begin{aligned}\overrightarrow{M_a^B}&=\left[\left(-LF_y^B+M_x^B\right)\cos\alpha+\left(LF_x^B+M_y^B\right)\sin\alpha+r_b^BF_z^B\right]\vec{i}\\&+\left[-\left(-LF_y^B+M_x^B\right)\sin\alpha+\left(LF_x^B+M_y^B\right)\cos\alpha-r_a^BF_z^B\right]\vec{j}+\left[M_z^B-r_2^BF_x^B+r_1^BF_y^B\right]\vec{k}\end{aligned} \quad (19)$$

The moment applied at the arcuate beam O is

$$\overrightarrow{M_a^O} = \overrightarrow{M_a^A} + \overrightarrow{M_a^B} + yF_x\vec{k} \tag{20}$$

Finally, the potential energy can be calculated from these bending and torsion terms. Solving $\frac{\partial U}{\partial F_x^A} = \frac{\partial U}{\partial F_y^A} = \frac{\partial U}{\partial F_z^A} = \frac{\partial U}{\partial M_x^A} = \frac{\partial U}{\partial M_y^A} = \frac{\partial U}{\partial M_z^A} = 0$ and $\frac{\partial U}{\partial F_x^B} = \frac{\partial U}{\partial F_y^B} = \frac{\partial U}{\partial F_z^B} = \frac{\partial U}{\partial M_x^B} = \frac{\partial U}{\partial M_y^B} = \frac{\partial U}{\partial M_z^B} = 0$ gives the value of the 12 unknowns in terms of F_x and thus $U = U(F_x)$. The compliance value in x-direction can be calculated from

$$C_x = \frac{\delta}{F_x} = \frac{\partial U}{\partial F_x} \Big/ F_x \tag{14}$$

The same procedure can be carried out for C_y, the compliance value in y-direction.

3.4. RESULTS AND DISCUSSION

The compliance values obtained through numerical simulations and analytical formulations were compared against one another to validate the approach developed in this research. Also, the compliance values obtained through the models were also compared against experimental data. Some tests have been conducted to experimentally measure the compliance of 2-Arc Fan interconnects. In [40], a scaled-up polymer version of the 2-Arc Fan design was produced. The polymer interconnect was made by stereo-lithography (STL) (using the Viper SLA System™ by 3D Systems®) at 1,000 times actual size. The measured Young's Modulus of the polymer is 2282MPa. Additional details on the test setup and results can be found in [40].

Table 3-1 presents the dimensions of the 2-Arc and 3-Arc Fan interconnects used in our work. Table 3-2 and Table 3-3 show the comparison of the compliance values obtained from different methods for the 2-Arc Fan Interconnect and the 3-Arc Fan Interconnect, respectively. Although it is not presented here in detail, the finite-element analysis and analytical solution for the 2-Arc Fan Interconnect follow the same procedure as outlined for the 3-Arc Fan Interconnects. As seen in Table 3-2, the simulated results

using 3D solid model match the experimental compliance values within 3% error for the 2-Arc Fan Interconnect. Thus, we can conclude that the fabricated interconnects are likely to perform mechanically, as designed and intended.

Also, it is seen that the compliance values obtained through beam elements and the analytical formulations are similar in magnitude as obtained through 3D solid elements and experimental data. The average discrepancy between the beam models and the 3D solid models is about 9.5%, while that between the analytical solutions and the beam models is about 11.3%. This confirms the validity of the analytical model developed in this work. Table 3-3 presents similar data for 3-Arc Fan interconnect. As seen, the compliance values obtained through 3D solid and beam elements as well as analytical models roughly agree with one another. However, the disparity among different models can be explained through these factors: 1) 3D models has the least assumption regarding the geometry and deformation of the interconnect, and therefore, are likely to produce the best results 2) the post is not slender enough to be modeled as a one dimensional beam; 3) the pad and solder ball are assumed to be rigid and modeled as beams with high Young's Modulus in the simplified beam model; 4) the analytical solutions are based on the Euler-Bernoulli beam assumptions.

In spite of these discrepancies, the beam model is a good substitution for the solid model in the application of a system with a large amount of interconnects, and such a model with several beam elements, instead of solid elements, will be computationally efficient. It can be seen that the analytical solutions are always higher than the others, because the analytical solutions are less constrained, i.e., when the force is applied in one direction, the displacements of the interconnect in the other two directions are not always constrained in order to reduce the calculation complexity. This will be improved in the future studies.

Table 3-1 Interconnect Geometry

	Beam Width [mm]	Beam Thickness [mm]	Beam Length [mm]	Post Height [mm]	Post Radius [mm]
2-Arc-Fan	4	8	77.5	27.5	3
3-Arc-Fan	6.6	13.2	178.7	23.7	5.3

Table 3-2 Comparison of the simulated compliance values among simulations, analytical solutions and experimental results for 2-Arc Fan Interconnect

	First In-Plane Axis [mm/N]	Second In-Plane Axis [mm/N]	Out-Of-Plane (full model) [mm/N]
3D Solid Model	0.133	0.0535	0.123
Beam Model	0.164	0.0526	0.142
Analytical Solution	0.164	0.0681	0.150
Experimental Results	0.129	0.0537	0.123

Table 3-3 Comparison of the simulated compliance values among simulations and analytical for 3-Arc Fan Interconnect

	First In-Plane Axis [mm/N]	Second In-Plane Axis [mm/N]	Out-Of-Plane (full model) [mm/N]	Out-Of-Plane (1/3 model) [mm/N]
3D Solid Model	0.0505	0.0509	0.0974	0.0974
Beam Model	0.0524	0.0537	0.106	0.106
Analytical Solution	0.0554	0.0597	--	0.121

Also, as seen from Table 3-2 and Table 3-3, with more arcs, an interconnect has more symmetry around the center pad. Thus, the in-plane compliance values in the two orthogonal planar directions for 3-Arc Fan interconnect are roughly the same, while they are significantly different for 2-Arc Fan Interconnect. It means that the radially periodic design addresses the directional problem, making the in-plane compliance values nearly planar isotropic.

3.5. CONCLUSION

The multi-path arc interconnects are potential solutions for mechanically decoupling the die from the substrate or the substrate from the board. The simplified beam model is a good substitute for the full 3D solid model in the case that there are a large number of interconnects in a structure. The analytical solutions based on Euler-Bernoulli beam assumptions and Castigliano's second theorem match the simulation and experimental results very well, and will give an insight into how the geometry parameters affect the compliance values, which is critical to the structural optimization design. The high compliance values of the interconnects can also improve the impact isolation of the die under dynamic mechanical loading conditions.

CHAPTER 4 RESPONSE SURFACE AND MULTI-OBJECTIVE DESIGN OPTIMIZATION

4.1. INTRODUCTION

The 3-Arc-Fan compliant interconnects have both in-plane and out-of-plane compliance and are able to accommodate the differential deflection between the die and the substrate or between the substrate and the board, and thus can enhance overall reliability and life of a microelectronic system. It is found that any geometry improvement that enhances the mechanical compliance will also adversely affect the electrical performance. Thus, the design of a compliant interconnect is a trade-off between the mechanical and electrical performance. The 3-Arc-Fan compliant interconnects have three electrical paths from the substrate pad to the solder ball to the board pad as shown in Figure 4-1. Thus, these interconnects can increase the mechanical compliance but also provide relatively good electrical characteristics. Since the design of interconnect is a trade-off between the mechanical compliance and electrical performance, this chapter developed a multi-objective optimization design method for the 3-Arc-Fan compliant interconnect to meet the desired mechanical and electrical performance targets, as well as the fabrication requirements.

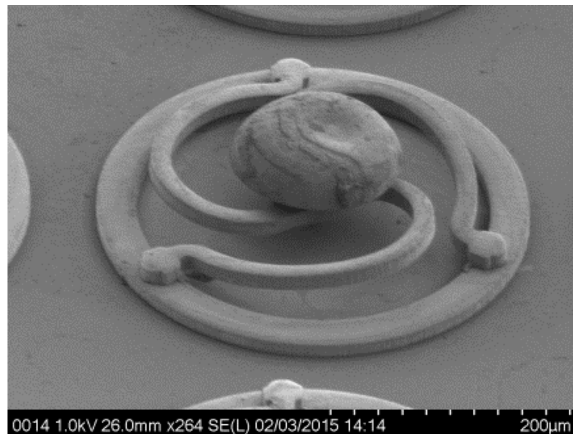


Figure 4-1 SEM image of the true scale copper version of the 3-Arc-Fan Compliant Interconnect with 2nd order splines, solder cap not reflowed

4.2. DESIGN VARIABLES

The 3-Arc-Fan compliant interconnect has three arcs, and the outer ends of the arcs will be connected to the substrate pad through columns, while the center of the arcs will be bonded to the board pad through solder. Figure 4-2 shows the 8 design variables that are considered in this work: *arcuate beam width*, *arcuate beam thickness*, *post diameter*, *post height*, *copper pad diameter*, *solder ball height*, *maximum solder diameter,* and *footprint* defining the size of the interconnect. Hundreds of cases must be run for each design objective (electrical resistance, inductance, etc.) in order to construct the response surface based on these eight design variables, which is very time consuming but not necessary. Reducing the number of design variables will significantly help to simplify the design process.

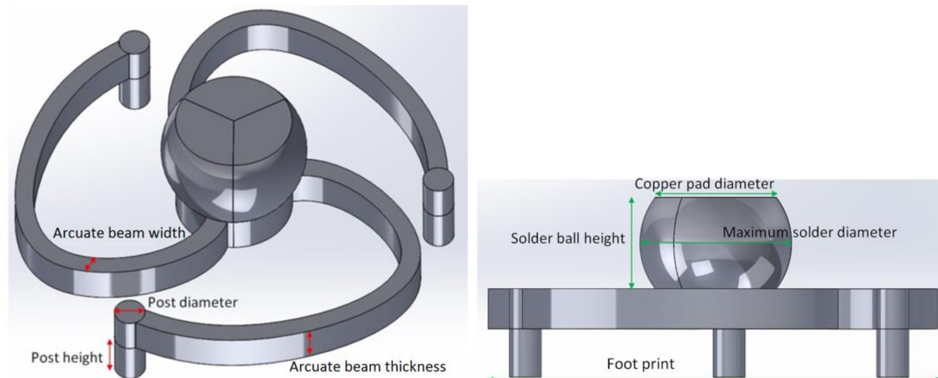


Figure 4-2 design variables of the 3-Arc-Fan compliant interconnect.

4.2.1. Solder Ball Variables

The variables defined for the solder ball in Figure 4-2 are *copper pad diameter*, *solder ball height,* and *maximum solder diameter*. However, these three variables are not independent. When the solder ball volume is given, the shape and dimensions of the solder ball in molten state during assembly can be determined using Surface Evolver [41, 42] taking into consideration the surface tension of solder liquid, the applied assembly force, and the copper pad diameter , as shown in Figure 4-3. Thus, the number of design variables for the solder ball can be reduced from three (*copper pad diameter, solder ball*

height, and maximum solder diameter) to two (*copper pad diameter and solder volume*). Thus, there are totally seven independent variables for the design of 3-Arc-Fan compliant interconnects. Surface Evolver is an interactive program for determining liquid shapes subjected to surface tension and other forces under various geometric constraints, Figure 4-4.

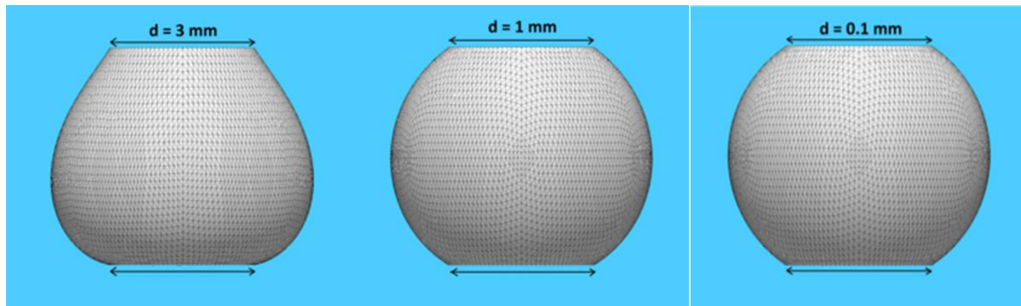


Figure 4-3 Shapes of different size of solder balls under the surface tension and the gravity. The left figure shows that the lower part of the solder ball is larger than the top part owing to the gravity force, and the middle and right figures show that the effect of the gravity force can be ignored if the solder ball is relatively small (pad diameter smaller than 1mm).

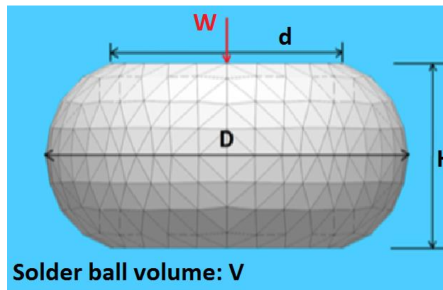


Figure 4-4 Surface Evolver can determine the maximum solder diameter *D* and solder ball height *H* based on the solder volume *V*, applied force *W* and pad diameter *d*.

4.2.2. Post Variables

There are two design variables, *post diameter* and *post height*, for the vertical posts, as shown in Figure 4-2. The three vertical posts are designed to provide the vertical stand-off height and thus the out-of-plane compliance. However, based on electrical capacitance considerations, the typical circular substrate pad has been replaced by an annular substrate pad, and the interconnect with the posts is placed on top of the annular

substrate pad, as shown in Figure 4-5. When simulations were run to determine the out-of-plane and in-plane compliance with and without posts, it is seen that the presence of posts will contribute to 9-15% of the compliance value, as outlined in Table 4-2. Also, our previous work [43] based on the analytical solutions has shown that the arcuate beam has the most contribution to the compliance values. In addition, the posts increase electrical parasitics and add additional processing steps. Because of these reasons, the posts are removed in the modified design, and the annular substrate pad is used to provide out-of-plane movement of the compliant interconnect. Thus, the rest of this research will not consider post variables, as these posts are not part of the modified compliant interconnect design.

In addition to the posts, the solder ball adds very little to the overall compliance of the interconnect. Simulations and analytical models show that an SnAg solder ball of 140μm diameter and 70μm standoff height will have an out-of-plane and in-plane compliance of about 7×10^{-5}mm/N and 3×10^{-4}mm/N, respectively. These compliance values are four to five orders of magnitude less than the compliant interconnect compliance values, as outlined in Table 4-2, and thus, Table 4-2 reports compliance values of the interconnects without considering the solder balls. Although the solder ball was not considered for mechanical compliance calculations, it was nevertheless included in electrical resistance and inductance analyses.

Figure 4-6 (a) shows the compliant interconnect directly placed on the annular substrate pad without posts and Figure 4-6 (b) is the same compliant interconnect with fillets added to the sharp corners to reduce the stress concentration. Thus, with the removal of posts, there are five design variables for the compliant interconnect, which are *copper pad diameter, arcuate beam width, arcuate beam thickness, solder ball volume* and *footprint (inner diameter of the annular substrate pad)*.

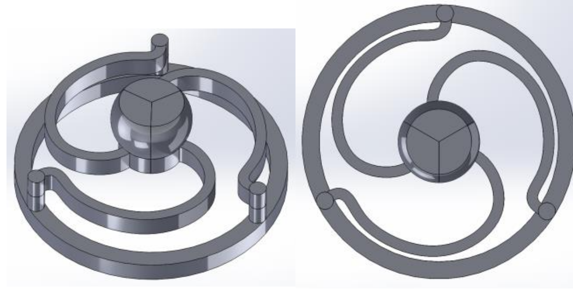


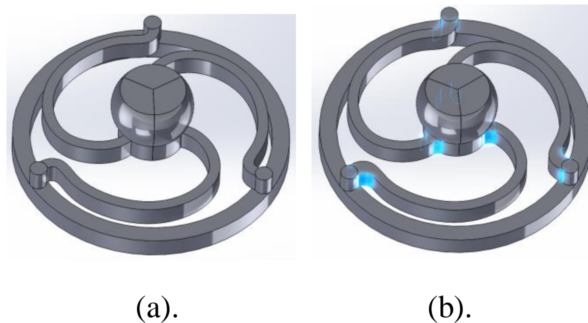
Figure 4-5 Compliant interconnect placed on the annular substrate pad via the posts

Table 4-1 3-Arc-Fan compliant interconnect geometry (Unit: µm; *footprint* = 140µm; Young's modulus = 117GPa)

Arcuate beam width	Arucuate beam thickness	Arcuate beam length	Post height	Post diameter	Cu pad diameter	Solder ball height	Max. solder ball diameter
6.6	13.2	178.7	23.7	10.6	40	30	50

Table 4-2 ANSYS® simulation results of compliance values of the 3-Arc-Fan compliant interconnect with/without posts

unit: *mm/N*	Out-of-plane	1st in-plane	2nd in-plane
With posts	4.97	2.56	2.59
Without posts	4.22	2.33	2.35
Contribution from the posts	15%	9.0%	9.3%



(a). (b).

Figure 4-6 (a). compliant interconnect placed on the annular substrate pad without posts; (b). the same compliant interconnect but with fillets, highlighted in light blue, added to the sharp corners to reduce the stress concentration

4.2.3. Normalized Design variables

The compliant interconnects are designed to be applicable as the First-Level interconnections between a die and a substrate, as well as the Second-Level

interconnections between a substrate and a board such that the footprint of the compliant interconnects is a variable. In order to make our design method applicable to different footprint size, the variables are normalized by footprint dimension. The simulation also reveals that for a compliant interconnect with compliant values $C_{\text{in-plane}}$ and $C_{\text{out-of-plane}}$, resistance R, inductance L, and the maximum Von Mises strain ε (under specific displacement), the corresponding values will be $C_{\text{in-plane}}/N$, $C_{\text{out-of-plane}}/N$, R/N, $L\times N$ and ε/N (under the same displacement) if the structure is scaled up by N. In this case, the footprint is the user selected/defined variable, and the other variables are to be calculated based on the defined footprint value and the optimization method developed in this work. Therefore, only one set of response surface data is needed to be constructed by selecting a particular footprint value. By normalizing using footprint size, there are only four design variables under consideration, as shown in Table 4-3.

Table 4-3 Dimensionless design variables after normalized by the footprint

D_0 = copper pad diameter/footprint
W_0 = arcuate beam width×10/footprint
T_0 = arcuate beam thickness×10/footprint
V_0 = Solder ball volume/(footprint/5)^3

4.3. RESPONSE SURFACE METHODOLOGY

Response surface methodology (RSM) consists of a group of statistical and mathematical techniques used to develop an adequate functional relationship between a response of interest, y, and a number of associated input variables denoted by x_1, x_2, . . . , x_k. In general, such a relationship is unknown but can be approximated by a low-degree polynomial model. The second-degree model which is one of the most commonly used in RSM is used in the work.

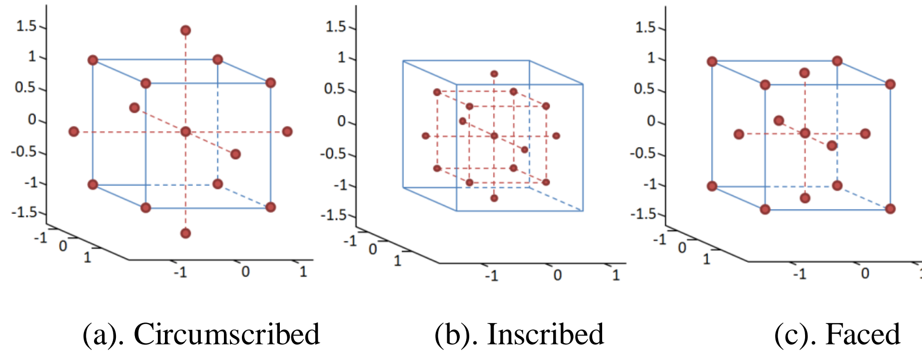
$$y = \beta_0 + \sum_{i=1}^{k} \beta_i x_i + \sum_{i<j}\sum \beta_{ij} x_i x_j + \sum_{i=1}^{k} \beta_{ii} x_i^2 + \zeta$$

where $\boldsymbol{\beta}$ is a vector of unknown constant coefficients, and ζ is a random experimental error assumed to have a zero mean, and $\boldsymbol{x} = [V_0, D_0, W_0, T_0]$ is the design variable vector.

As the design of interconnect is a trade-off between the mechanical compliance and electrical performance, this work will take the compliance values $C_{\text{in-plane}}$ and $C_{\text{out-of-plane}}$, resistance R (at low frequency), inductance L (at low frequency) and maximum Von Mises strains ε (under specific displacement) as the design objectives. The analytical solutions for both the in-plane and out-of-plane compliance values have been developed in our previous work [43] based on the Euler-Bernoulli beam theory and the energy method, and thus, response surfaces are only to be constructed for R, L and ε, respectively.

4.3.1. Design of Simulations

3^k factorial, central composite, the Box-Behnken designs are the most frequently used second-order designs [44]. The 3^k factorial design consists of all the combinations of the levels of k design variables with 3 levels each. As there are 4 design variables, there will be 81 simulations for each of the 3 design objectives, and thus, there will be 243 simulations for all 3 design objectives R, L and ε with 4 design variables. Box-Behnken designs are rotatable and require fewer runs than 3^k factorial designs and central composite designs, but they are only good for a small number of design variables (four or less). Although there are only 4 design variables in our current study, future work may involve more design variables. Central composite designs (CCDs), also known as Box-Wilson designs, are appropriate for calibrating full quadratic models. There are three types of CCDs— central composite circumscribed (CCC), central composite inscribed (CCI), and central composite faced (CCF), shown in Figure 4-7. CCF is fair over design space and poor for pure quadratic coefficients. CCC is good over entire design space, but it uses points beyond the predefined cube which might leads to non-physical meaning design variables (i.e. negative arcuate beam width value). CCI is good over central subset of design space and is selected to construct the response surfaces for our study.



(a). Circumscribed (b). Inscribed (c). Faced

Figure 4-7 Experimental space definition of the 3 central composite design models with three variables at 3 level

4.3.2. Determination of Data Points for Design Variables

The ranges of the design variables are determined based on Table 4-1, where the original design variables are calculated as D_0 = 0.2857, W_0 = 0.4714, T_0 = 0.9429 and V_0 = 2.3614. Table 4-4 shows the ranges of the 4 design variables, which is able to make sure that all of the CCI experiment points are reasonable. The arcuate structures of the interconnect are designed to act as slender beams with the width to length ratio as well as the thickness to length ratio ranging from 50 to 10. For example, for an interconnect with its footprint equal to 140μm, the arcuate structure width and thickness range from 3.5μm to 16.8μm if W_0, $T_0 \in [0.25, 1.2]$, while the arcuate beam length is 178.7μm as given in Table 4-1. Any further increase in the width or the thickness of the arcuate structure will make it much less compliant. Also, additional increase in width will make the arcuate structures to touch and interfere with each other upon loading. Similarly, further increase in the thickness of the arcuate structure will introduce fabrication difficulties as well as additional masking processes. Thus, the values provided in Table 4-4 are lower and upper limits of various design parameters and should not be exceeded for design optimization. The data points used to calculate the response surfaces are selected based on CCI and the determined ranges of the design variables. For a system with 4 design variables ranged within [-1, 1], CCI selects their values at -1, -0.5, 0, 0.5 and 1. And for a system with 3 design variables ranged within [-1, 1], CCI selects their values at -1, -0.5946, 0, 0.5946

and 1. Table 4-5 shows the corresponding values for V_0, D_0, W_0 and T_0 selected by CCI, if their maximum values correspond to 1 and minimum values correspond to -1. The footprint is chosen to be 140μm to construct the response surfaces.

Table 4-4 Ranges of the four design variables

D_0 = copper pad diameter/footprint	[0.24, 0.38]
W_0 = arcuate beam width×10/footprint	[0.25, 1.2]
T_0 = arcuate beam thickness×10/footprint	[0.25, 1.2]
V_0 = Solder ball volume/(footprint/5)^3	[2, 3]

Table 4-5 The corresponding values for V_0, D_0, W_0 and T_0 selected by CCI, if their maximum values correspond to 1 and minimum values correspond to -1.

[-1, 1]	-1	-0.5946	-0.5	0	0.5	0.5946	1
D_0 [0.24, 0.38]	0.24	0.2684	0.275	0.31	0.3450	0.3516	0.38
W_0 [0.25, 1.2]	0.25	0.4426	0.4875	0.725	0.9625	1.0074	1.2
T_0 [0.25, 1.2]	0.25	0.4426	0.4875	0.725	0.9625	1.0074	1.2
V_0 [2, 3]	2	2.2027	2.25	2.5	2.75	2.7973	3

4.3.3. Response Surfaces for *L* and *R*

The footprint is chosen to be 140μm to construct the response surfaces.

Table 4-6 shows the various combinations of design variables and the corresponding design objectives obtained from response surfaces, and the results are compared with the corresponding values calculated by ANSYS®. The response surfaces, on the average, have a 0.0735% relative error for inductance and 6.46% relative error for resistance. Both Figure 4-8 and

Table 4-6 show that the developed response surfaces predict the inductance and resistance very well. The inductance and resistance values for the interconnect whose footprint is 140μm can be calculated as,

$$L^* \text{ or } R^* = \beta_0 + \beta_1 V_0 + \beta_2 D_0 + \beta_3 W_0 + \beta_4 T_0 + \beta_{12} V_0 D_0 + \beta_{13} V_0 W_0 + \beta_{14} V_0 T_0 \\ + \beta_{23} D_0 W_0 + \beta_{24} D_0 T_0 + \beta_{34} W_0 T_0 + \beta_{11} V_0^2 + \beta_{22} D_0^2 + \beta_{33} W_0^2 + \beta_{44} T_0^2$$

where β's are constant coefficients obtained for the inductance and resistance response surfaces, respectively, shown in Table 4-7. And as discussed in the normalization section, the inductance and resistance for a compliant interconnect with arbitrary footprint size are,

$$L = L^{*} \times footprint/140\mu\text{m}$$

$$R = R^{*} \times 140\mu\text{m}/footprint$$

Table 4-6 Two response surfaces for the inductance *L* and resistance *R*, respectively. The first 4 columns are various combinations of V_0, D_0, W_0, and T_0. The 5th and 6th columns are the inductance and resistance values calculated by ANSYS®. The last 2 columns are the relative errors when the response surface values are compared against corresponding values calculated by ANSYS®.

V_0	D_0	W_0	T_0	L [nH]	$R[\Omega]$	L Relative Error (%)	R Relative Error (%)
2.25	0.275	0.4875	0.4875	3.87E-02	2.36E-02	0.0969	-5.8369
2.25	0.275	0.4875	0.9625	3.60E-02	1.34E-02	0.1389	-2.9384
2.25	0.275	0.9625	0.4875	3.23E-02	1.30E-02	0.0516	-2.4519
2.25	0.275	0.9625	0.9625	3.11E-02	7.97E-03	0.0134	8.1870
2.25	0.345	0.4875	0.4875	3.64E-02	2.21E-02	0.0458	-6.3367
2.25	0.345	0.4875	0.9625	3.35E-02	1.20E-02	0.0124	-3.6181
2.25	0.345	0.9625	0.4875	3.02E-02	1.16E-02	0.0690	-3.0963
2.25	0.345	0.9625	0.9625	2.88E-02	6.71E-03	-0.0579	9.4573
2.75	0.275	0.4875	0.4875	3.98E-02	2.38E-02	0.0419	-5.8141
2.75	0.275	0.4875	0.9625	3.71E-02	1.36E-02	0.0112	-2.8860
2.75	0.275	0.9625	0.4875	3.34E-02	1.32E-02	0.0624	-2.4053
2.75	0.275	0.9625	0.9625	3.22E-02	8.16E-03	-0.0518	7.9810
2.75	0.345	0.4875	0.4875	3.72E-02	2.23E-02	0.0560	-6.2967
2.75	0.345	0.4875	0.9625	3.43E-02	1.22E-02	-0.0486	-3.5280
2.75	0.345	0.9625	0.4875	3.09E-02	1.18E-02	-0.1618	-3.0120
2.75	0.345	0.9625	0.9625	2.96E-02	6.89E-03	-0.0422	9.0832
2	0.31	0.725	0.725	3.24E-02	1.12E-02	-0.1672	6.6778
3	0.31	0.725	0.725	3.44E-02	1.16E-02	0.0848	6.4907
2.5	0.24	0.725	0.725	3.62E-02	1.30E-02	-0.1496	5.3045
2.5	0.38	0.725	0.725	3.14E-02	1.04E-02	0.0929	7.8005
2.5	0.31	0.25	0.725	3.97E-02	2.98E-02	-0.1364	9.5903
2.5	0.31	1.2	0.725	2.87E-02	7.56E-03	0.1016	-17.9508
2.5	0.31	0.725	0.25	3.59E-02	2.88E-02	-0.1045	9.4025
2.5	0.31	0.725	1.2	3.19E-02	7.81E-03	0.0392	-15.4556
2.5	0.31	0.725	0.725	3.35E-02	1.14E-02	0	0
Average the Absolute Value of the Relative Errors						0.0735	6.46

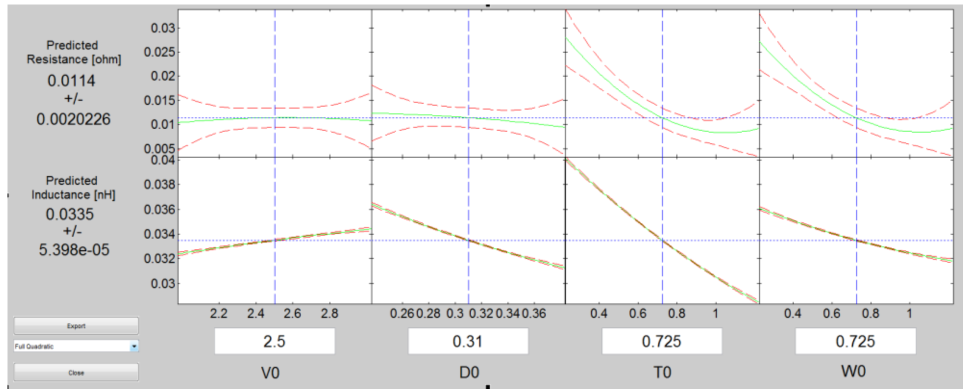


Figure 4-8 Prediction plots of full quadratic models for the inductance and resistance. The green lines are the predicted values with each of them bounded by two red lines representing 95% simultaneous confidence band for the fitted response. The predictor values in this figure are V_0 = 2.5, D_0 = 0.31, T_0 = 0.725 and W_0 = 0.725

Table 4-7 Coefficients of the second-degree response surfaces for the inductance and resistance

β	Inductance	Resistance
β_0	0.05399	0.05867
β_1	0.00655	0.01547
β_2	-0.05121	0.03261
β_3	-0.02251	-0.07861
β_4	-0.01045	-0.07520
β_{12}	-0.00929	-0.00007
β_{13}	-0.00011	-0.00003
β_{14}	0.00011	-0.00003
β_{23}	0.00526	0.00353
β_{24}	-0.00526	0.00353
β_{34}	0.00676	0.02297
β_{11}	-0.00035	-0.00300
β_{22}	0.06378	-0.09192
β_{33}	0.00316	0.02894
β_{44}	0.00183	0.02728

4.3.4. Response Surfaces for Maximum von Mises Strain

The solder ball contributes little to the compliance, so V_0 is not included in the two response surfaces for the maximum von Mises strain values ε, and both the number of the experimental points and the number of the coefficients are thus reduced. Table 4-8 shows the various combinations of design variables and the corresponding design

objectives obtained from response surfaces, and the results are compared with the corresponding values calculated by ANSYS®. The response surfaces, on the average, have a 2.93% and 4.89% relative error for von Mises strain when subjected to in-plane and out-of-plane displacement, respectively. Figure 4-9 and Table 4-8 show that the developed response surfaces predict the maximum von Mises strains very well. The von Mises strains for the interconnect whose footprint is 140μm are then calculated as,

$$\varepsilon^*_{\Delta x=1\mu m} \text{ or } \varepsilon^*_{\Delta y=1\mu m} = \beta_0 + \beta_1 D_0 + \beta_2 W_0 + \beta_3 T_0 + \beta_{12} D_0 W_0 + \beta_{13} D_0 T_0 + \beta_{23} W_0 T_0 + \beta_{11} D_0^2 + \beta_{22} W_0^2 + \beta_{33} T_0^2$$

where β's are constant coefficients obtained for the two maximum von Mises strain response surfaces, respectively, shown in Table 4-9. Von Mises strains for a compliant interconnect with an arbitrary footprint size under arbitrary amount of small in-plane displacement Δx or out-of-plane displacement Δy are,

$$\varepsilon_{\Delta x} = \varepsilon^*_{\Delta x=1\mu m} \times 140\mu\text{m}/footprint \times \Delta x/1\mu\text{m}$$

$$\varepsilon_{\Delta y} = \varepsilon^*_{\Delta y=1\mu m} \times 140\mu\text{m}/footprint \times \Delta y/1\mu\text{m}$$

Table 4-8 Response surfaces for the maximum von Mises strain value ε. As the solder ball contributes little to the compliance, the solder ball volume is not used for this response surface calculation. The first 3 columns are various combinations of D_0, W_0, and T_0. The 4th and 5th columns are von Mises strain values calculated by ANSYS® when the structure is under 1μm in-plane and out-of-plane displacement, respectively. The last 2 columns are the relative errors when the response surface values are compared against the corresponding values calculated by ANSYS®.

D_0	W_0	T_0	$\varepsilon_{\Delta x=1\mu m}$	$\varepsilon_{\Delta y=1\mu m}$	Δx Relative Error (%)	Δy Relative Error (%)
0.2684	0.4426	0.4426	0.0028	0.0008	2.2564	-4.6804
0.2684	0.4426	1.0074	0.0027	0.0014	-2.5931	-7.5118
0.2684	1.0074	0.4426	0.0062	0.0013	1.5809	-2.1780
0.2684	1.0074	1.0074	0.0059	0.0024	0.3550	-3.1393
0.3516	0.4426	0.4426	0.0031	0.0008	5.9502	-6.9899
0.3516	0.4426	1.0074	0.0031	0.0015	3.5159	-6.8462
0.3516	1.0074	0.4426	0.0072	0.0013	3.8210	-2.1871
0.3516	1.0074	1.0074	0.0069	0.0025	2.0826	-3.8884
0.24	0.725	0.725	0.0041	0.0017	0.7978	4.6531
0.38	0.725	0.725	0.0047	0.0019	-6.9589	5.5991
0.31	0.25	0.725	0.0017	0.0009	-4.2664	12.5620
0.31	1.2	0.725	0.0075	0.0021	-2.9312	3.4405
0.31	0.725	0.25	0.0044	0.0008	-6.1875	3.1416
0.31	0.725	1.2	0.0045	0.0026	-0.4729	6.3364
0.31	0.725	0.725	0.0044	0.0018	0.1137	-0.1794
Average the Absolute Value of the Relative Errors					2.9256	4.8889

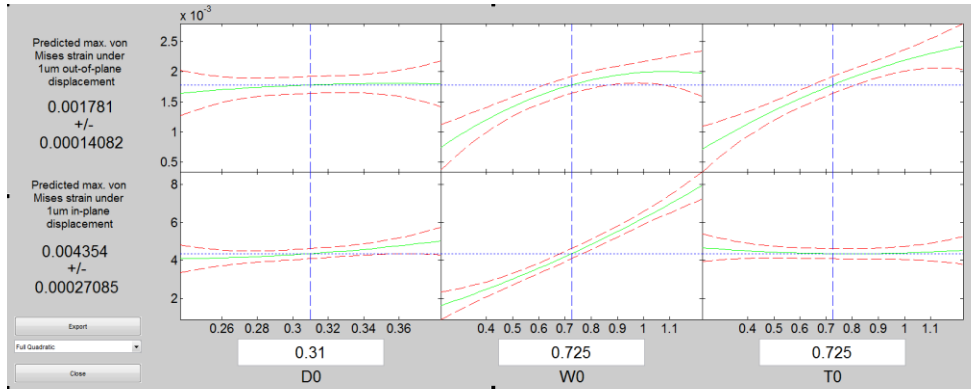


Figure 4-9 Prediction plots of full quadratic models for the maximum von Mises strains. The green lines are the predicted values with each of them bounded by two red lines representing 95% simultaneous confidence band for the fitted response. The predictor values in this figure are D_0 = 0.31, T_0 = 0.725 and W_0 = 0.725

Table 4-9 Coefficients of the second-degree response surface for von Mises strains

β	$\varepsilon_{\Delta x = 1\mu m}$	$\varepsilon_{\Delta y = 1\mu m}$
β_0	0.00555	-0.00206
β_1	-0.02680	0.00726
β_2	0.00021	0.00282
β_3	-0.00096	0.00129
β_{12}	0.01355	-0.00084
β_{13}	-0.00009	0.00171
β_{23}	-0.00076	0.00156
β_{11}	0.03770	-0.01106
β_{22}	0.00171	-0.00170
β_{33}	0.00097	-0.00085

4.4. MULTI-OBJECTIVE OPTIMIZATION DESIGN METHODOLOGY

The design of the compliant interconnect under study involves maximizing both the electrical and mechanical performance. Ideally, the objectives to be considered in this work are to minimize electrical resistance, inductance, and von Mises strain and simultaneously maximize the in-plane and out-of-plane compliance values. However, increasing the compliance values requires smaller beam dimensions, which adversely affect the electrical performance. The tradeoffs between the electrical and mechanical characteristics requires the use of multi-objective optimization, an area of multiple

criteria decision making that involves minimizing or maximizing more than one objective function subject to a set of constraints.

4.4.1. Design Constraints

The constraints are mostly dependent on the specific application of the compliant interconnect under study. For example, the lower limits of the compliance values are to be set for the case where the planarity is the main concern. Much stricter constraints will be applied for electrical resistance and inductance where the electrical performance is the most important part. Thus, the following discussion is just to give a general idea on how to set the constraints.

Considering a case where 400μm interconnect pitch is required, and the interconnect *footprint* is selected as 280μm. From mechanical point of view, it is desirable to have von Mises strain in the copper interconnect below its yield strain so that the interconnect will not plastically yield due to the differential displacement. However, it is not necessary to guarantee that the interconnect will always work within the elastic range. This is because plastic deformation under the thermal cycling is common, as the differential displacement under typical thermal cycling will exceed 2μm used in the calculations so far. $\varepsilon \times E_{cu} \leq \sigma_y/\eta$ is for enforced to make sure that the copper is working within the elastic range, where η is the safety factor. In addition, a compliance value of more than 1mm/N in both in-plane and out-of-plane directions is desirable. From an electrical standpoint, the parasitics should be as small as possible, and these values are determined based on the intended application. The electrical parasitics of the 3-Arc-Fan compliant interconnect are higher than the solder balls due to its geometry design, but they must be superior to the wire bond in the aspect of electrical performance. For a typical wire bond, the inductance is more than 0.5nH [45, 46] and the resistance is more than 20mΩ [46, 47]. So we will set 0.1nH as the limiting value for electrical inductance and 10mΩ as the limiting value for electrical resistance in this work. When considering

the fabrication process, the beam thickness is preferred to be less than twice of the beam width. Given these considerations, the constraints are:

$$C_{\text{in-plane}} \geq 1\text{mm/N}$$

$$C_{\text{out-of-plane}} \geq 1\text{mm/N}$$

$$R \leq 10\text{m}\Omega$$

$$L \leq 0.1\text{nH}$$

$$\varepsilon_{\Delta x} \times E_{\text{cu}} \leq \sigma_{\text{y}}/\eta$$

$$\varepsilon_{\Delta y} \times E_{\text{cu}} \leq \sigma_{\text{y}}/\eta$$

$$T_0 \leq 2W_0$$

4.4.2. Multi-Objective Optimization through the Method of Global Criterion

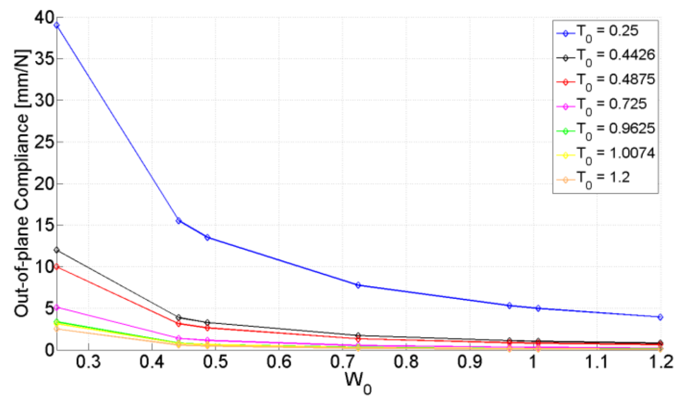


Figure 4-10 Out-of-plane compliance vs. arcuate beam width for various beam thickness (footprint = 300µm)

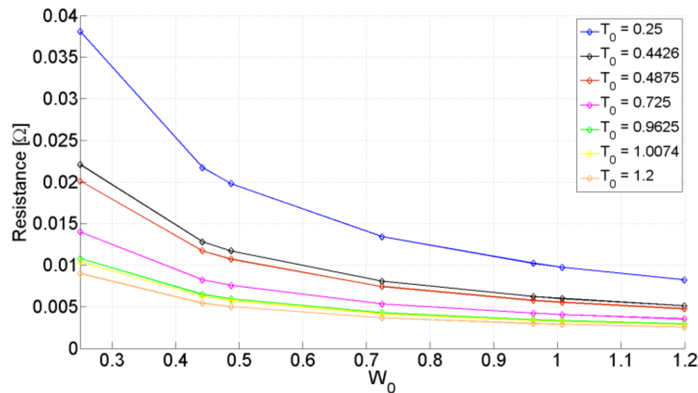


Figure 4-11 Electrical resistance vs. arcuate beam width for various beam thickness (footprint = 300µm)

The sensitivity plots of the out-of-plane compliance value and electrical resistance with respect to arcuate beam width and thickness for an interconnect with a footprint equal to 280μm are presented in Figure 4-10 and Figure 4-11, respectively. It can be seen that both the out-of-plane compliance and the electrical resistance decrease with the increase of the arcuate beam width and thickness. However, a good interconnect design requires lower electrical resistance but higher mechanical compliance. Therefore, there does not exist a single solution that simultaneously optimizes all objectives in our study. This study will convert the original problem with multiple objectives into a single-objective optimization problem. There are several methods to scalarize multi-objective optimization problem, including linear scalarization, a priori methods, a posteriori methods, etc. The method of global criterion [48] and weighted sums method [49] were used in our work.

The method of global criterion scalarizes the problem in the following form,

$$\min \left\| f(x) - z^{ideal} \right\|, s.t. x \in X$$

where $\|.\|$ can be any L_p norm, with common choices including L_1, L_2 and L_∞. To apply it into our study, the following objective function is constructed if the L_2 norm is used,

$$\min \sqrt{\left(R-R^{ideal}\right)^2+\left(L-L^{ideal}\right)^2+\left(\varepsilon_{\Delta x}-\varepsilon_{\Delta x}^{ideal}\right)^2+\left(\varepsilon_{\Delta y}-\varepsilon_{\Delta y}^{ideal}\right)^2+\left(C_{in-plane}-C_{in-plane}^{ideal}\right)^2+\left(C_{out-of-plane}-C_{out-of-plane}^{ideal}\right)^2},$$
$$s.t. D_0 \in [0.24, 0.38]; W_0, T_0 \in [0.25, 1.2]; V_0 \in [2,3];$$

where R^{ideal} is the minimum possible resistance value within the ranges of the four design values, L^{ideal} is the minimum possible inductance value, $\varepsilon_{\Delta x}^{ideal}$ *and* $\varepsilon_{\Delta y}^{ideal}$ are the minimum possible von Mises strain value under in-plane displacement Δx and out-of-plane displacement Δy, $C_{in-plane}^{ideal}$ *and* $C_{out-of-plane}^{ideal}$ the maximum possible in-plane and out-of-plane compliance value. This optimization method does not require any preference information to be explicitly articulated by a decision maker. However, if a decision maker wants to give some objectives more influence than the others on the result, the weighted sums method can be applied together with the method of global criterion,

$$\min \sqrt{w_1\left(R-R^{ideal}\right)^2+w_2\left(L-L^{ideal}\right)^2+w_3\left(\varepsilon_{\Delta x}-\varepsilon_{\Delta x}^{ideal}\right)^2+w_4\left(\varepsilon_{\Delta y}-\varepsilon_{\Delta y}^{ideal}\right)^2+w_5\left(C_{in-plane}-C_{in-plane}^{ideal}\right)^2+w_6\left(C_{out-of-plane}-C_{out-of-plane}^{ideal}\right)^2},$$
$$s.t. D_0 \in [0.24, 0.38]; W_0, T_0 \in [0.25, 1.2]; V_0 \in [2,3];$$

where w's are weight functions to be determined by a decision maker.

This scalarized objective function is sensitive to the scaling of the objective function, and thus, it is normalized into a uniform, dimensionless scale.

$$\min \sqrt{w_1\left(\frac{R-R^{ideal}}{R^{ideal}}\right)^2+w_2\left(\frac{L-L^{ideal}}{L^{ideal}}\right)^2+w_3\left(\frac{\varepsilon_{\Delta x}-\varepsilon_{\Delta x}^{ideal}}{\varepsilon_{\Delta x}^{ideal}}\right)^2+w_4\left(\frac{\varepsilon_{\Delta y}-\varepsilon_{\Delta y}^{ideal}}{\varepsilon_{\Delta y}^{ideal}}\right)^2+w_5\left(\frac{C_{in-plane}-C_{in-plane}^{ideal}}{C_{in-plane}^{ideal}}\right)^2+w_6\left(\frac{C_{out-of-plane}-C_{out-of-plane}^{ideal}}{C_{out-of-plane}^{ideal}}\right)^2},$$
$$s.t. D_0 \in [0.24, 0.38]; W_0, T_0 \in [0.25, 1.2]; V_0 \in [2,3].$$

In this work, w's were selected to be equal to "1" and the new objective function is reconstructed as

$$\min \sqrt{\left(\frac{R-R^{ideal}}{R^{ideal}}\right)^2+\left(\frac{L-L^{ideal}}{L^{ideal}}\right)^2+\left(\frac{\varepsilon_{\Delta x}-\varepsilon_{\Delta x}^{ideal}}{\varepsilon_{\Delta x}^{ideal}}\right)^2+\left(\frac{\varepsilon_{\Delta y}-\varepsilon_{\Delta y}^{ideal}}{\varepsilon_{\Delta y}^{ideal}}\right)^2+\left(\frac{C_{in-plane}-C_{in-plane}^{ideal}}{C_{in-plane}^{ideal}}\right)^2+\left(\frac{C_{out-of-plane}-C_{out-of-plane}^{ideal}}{C_{out-of-plane}^{ideal}}\right)^2},$$
$$s.t. D_0 \in [0.24, 0.38]; W_0, T_0 \in [0.25, 1.2]; V_0 \in [2,3].$$

4.4.3. Optimized Compliant Interconnect Geometry

Table 4-10 shows the starting design variables of the compliant interconnect, and the maximum von Mises strain under in-plane (x) and out-of-plane displacements, the self-inductance, the resistance, and the in-plane and out-of-plane compliance values for the starting design variables. As seen, the interconnect does not meet the constraints for compliance, and the compliance values are less than the minimum requirement of 1mm/N.

Table 4-10 Starting design

Starting Design Variables			
V_0	D_0	W_0	T_0
2.3614	0.2857	0.4714	0.9429
V [mm^3]	D [μm]	W [μm]	T [μm]
0.00051	85.7100	14.1420	28.2870
Maximum von Mises Strain [Δx = 2μm]			0.0027
Maximum von Mises Strain [Δy = 2μm]			0.0013
Self-Inductance [nH]			0.0772
Resistance [mΩ]			6.4492
In-Plane Compliance [mm/N]			0.3096
Out-Of-Plane Compliance [mm/N]			0.6547

Based on the upper and lower limits of various design variables, the analytical solution for the compliance values [43], response surfaces for von Mises strains, resistance and inductance, seven imposed constraints for design and processing conditions, and the dimensionless scalarized objective function, the optimized values for the design variables of the compliant interconnect geometry are obtained. The results are shown in Table 4-11. It should be noted that the solder ball volume is calculated to have the minimum value $V_0 = 2$, because the solder does not contribute to compliance value but will increase the electrical parasitics. According to the constraints set previously, $V_0 = 2$ is apparently the best choice. However, smaller solder ball size might lead to assembly issues, e.g. the non-wetting, and the constraints on the solder ball volume can be added dependent on the particular assembly requirement.

Table 4-11 Optimization results

<table>
<tr><td colspan="5">Optimized Design Variables</td></tr>
<tr><td>V_0</td><td>D_0</td><td>W_0</td><td colspan="2">T_0</td></tr>
<tr><td>2</td><td>0.37</td><td>0.34</td><td colspan="2">0.69</td></tr>
<tr><td>V [mm^3]</td><td>D [μm]</td><td>W [μm]</td><td colspan="2">T [μm]</td></tr>
<tr><td>0.000432</td><td>110.31</td><td>10.31</td><td colspan="2">20.62</td></tr>
<tr><td colspan="2">Objectives</td><td>Response Surfaces</td><td>ANSYS®</td><td>Relative Error [%]</td></tr>
<tr><td colspan="2">Maximum von Mises Strain [Δx = 2μm]</td><td>0.22%</td><td>0.23%</td><td>4.35</td></tr>
<tr><td colspan="2">Maximum von Mises Strain [Δy = 2μm]</td><td>0.099%</td><td>0.11%</td><td>10</td></tr>
<tr><td colspan="2">Self-Inductance [nH]</td><td>0.077</td><td>0.072</td><td>6.94</td></tr>
<tr><td colspan="2">Resistance [mΩ]</td><td>10</td><td>11</td><td>9.09</td></tr>
<tr><td colspan="2">In-Plane Compliance [mm/N]</td><td>1.21</td><td>1.14</td><td>6.14</td></tr>
<tr><td colspan="2">Out-Of-Plane Compliance [mm/N]</td><td>2.39</td><td>2.42</td><td>1.24</td></tr>
</table>

Table 4-11 presents the optimized design variables, and it is seen that all of the constraints are met. Furthermore, it is observed that when the mechanical compliance exceeds 1mm/N, the von Mises strain also decreases compared to the unoptimized interconnect design. Also, it can be observed that with better mechanical metrics, the electrical resistance and inductance have increased, as would be expected. However, the increase in electrical metrics is still within the constraints outlined earlier. Thus, through

the response surface methodology, an interconnect design is obtained that meets all of the constraints. In addition, separate simulations were carried out using the optimized design variables, and the results obtained from such simulations are compared against the values suggested by response surfaces, as shown in Table 4-11. It is seen that the relative error is only 1 – 10%.

4.5. CONCLUSION

A multi-objective design optimization of 3-Arc-Fan compliant interconnect is presented in this chapter. A discussion on reducing the number of design variables and selecting the most important design variables are first presented. This helps to reduce the total number of design variables from 8 to 5, which significantly reduces the number of simulations needed for developing the response surfaces. The design variables are normalized using interconnect footprint dimension, and thus, the process not only normalized the design variables but also reduced the number of design variables to 4. This method of normalization makes the response surfaces constructed for a particular footprint size applicable to interconnects with arbitrary footprint size. After identifying the limiting values of the design variables, response surfaces are constructed for inductance, resistance and the von Mises strains based on CCI simulation points. The response surface creates 0.074% average relative error for inductance, 6.46% average relative error for electrical resistance, and 2.93% and 4.89% average relative errors for von Mises strains when subjected to in-plane and out-of-plane displacement, respectively. Finally, the Method of Global Criterion is used to scalarize this multi-objective optimization problem. An optimization has been done under the specified constraints and the ranges of the design variables, and the results show that the interconnect geometry can be designed such as to meet the electrical and mechanical requirements, as well as the fabrication constraints.

This work has employed response surface methodology for optimization, rather than coupling the optimizer with the commercial finite-element software. Response

surface methodology is simple and can determine responses for a combination of input variables a priori. To construct the response surfaces, 25 simulations are done for the inductance and resistance and 15 simulations are done for determining von Mises strain under in-plane and out-of-plane loading conditions. Compliance values are computed analytically. Thus, no further simulations are needed and the optimization process involves polynomial evaluations whose evaluation times are negligible, once the response surfaces are constructed. During the optimization process using response-surface methodology, the total number of points where objective function evaluations take place is more than 200. This indicates that if one were not to use the response-surface methodology, there will be at least 200 simulations each for the inductance, resistance and the von Mises strain values under in-plane and out-of-plane loading conditions. Thus, more than 800 simulations will become tedious and time-consuming especially when multiple software packages are used for mechanical and electrical analyses, and when each simulation takes multiple load steps as in thermal cycling simulations. Furthermore, each new optimization process with different design constraints will request another hundreds of simulations. The number of simulations here is approximate and is intended to give an idea of the scope of the problem.

The methodology introduced in this work gives a framework for the design of compliant interconnects. Future work will include other design objectives such as thermal cycling fatigue life and drop impact performance to be able to further optimize the 3-Arc-Fan compliant interconnect geometry. The methodology, presented in this research, is not restricted to the 3-Arc-Fan compliant interconnect, but can also be applied for the design of other compliant interconnects.

CHAPTER 5 FABRICATION USING NEGATIVE DRY-FILM PHOTORESIST

The present work is to explore a new fabrication method which can significantly reduce the number of fabrication steps, increase the fabrication reliability, as well as reduce the cost.

Earlier work [50] has focused on fabricating the multi-path interconnects using liquid positive photoresist on a 4-inch silicon wafer. By using liquid photoresist, the wafer requires both soft bake step to drive-off the excess solvents in the photoresist after coating, as well as the hard bake step after development in order to increase the thermal, chemical, and physical stability of developed photoresist structures for subsequent processes. Additionally, the post exposure bake step might be also preferred if the liquid photoresist is used. These bake processes not only add extra steps but may lead to cracking of the photoresist due to the different thermal expansion coefficients of photoresist and substrate. As the 3-Arc-Fan compliant interconnect fabrication involves multiple photoresist layers, there are many times for the bake processes leading to much more fabrication steps as well as higher risk of photoresist cracking in the case of using liquid photoresist. In addition, this fabrication involving liquid positive photoresist should be finished in class 10 or 100 cleanroom.

So this work explores an alternate fabrication method by using negative dry-film photoresist, which significantly reduces the number of fabrication steps and increases the fabrication reliability by avoiding the bake processes. Since the fabrication can be done in the class 1000 cleanroom, the use of the dry-film photoresist makes the fabrication process cost effective compared to the use of liquid film photoresist [51].

5.1. PHOTORESIST SELECTION

A photoresist is a light-sensitive polymer used in several processes like photolithography and photoengraving to form a patterned coating on a surface. There are

two types of photoresists: positive photoresists and negative photoresists. A positive photoresist is the one in which the portion of the photoresist that is exposed to the light becomes trenches after develop, and a negative photoresist is the one in which the portion of the photoresist that is not exposed to the light becomes trenches after develop.

The photoresist used in our study is Dupont™ Riston® FX920. It is a negative working, aqueous processable dry-film photoresist, and compatible with acid copper, tin, tin/lead, nickel sulfamate and acid gold electrolytic plating baths. It is able to resolve 10 micron features in an optimized production environment. Table 5-1 summarizes some processing information for Dupont™ Riston® FX920.

Table 5-1 Processing information for Dupont™ Riston® FX920

Roll Temperature	105 – 120°C (220 – 250°F)
Roll Speed	0.6 – 1.5m/min (2 – 5 ft/min) (HRL Hot Roll Laminator Conditions)
Air Assist Pressure	0 – 2.8 bar (0 – 40 psig); for ≥1.7 bar (25psig) use heavy duty or crowned rolls (HRL Hot Roll Laminator Conditions)
Post-lamination Hold Time	About 15 minutes
Exposure Energy	35 – 105 mJ/cm^2
Stripping	Aqueous caustic (NaOH or KOH) conveyorized stripping

5.2. 3-ARC-FAN COMPLIANT INTERCONNECT FABRICATION

5.2.1. Substrate Layout

The fabrication of an area-array of 3-Arc-Fan compliant interconnects was carried out on a 6-inch silicon wafer using sequential processes. The design consists of about 2000 compliant interconnects at a 400-μm pitch on each 18mm×18mm silicon substrate, and there are 32 substrates on a 6-inch wafer, as shown in Figure 5-1. The three arcuate beams of the compliant interconnects are the main parts that provide both the in-plane and out-of-plane compliance, and thus the arcuate beam width and thickness are the most important factor to be considered. DupontTM Riston® FX920 negative dry-film

photoresist was used in our study and the arcuate beam thickness is uniform throughout the pattern. However, by designing the arcuate beam width to be 10µm, 15µm, and 20µm, as shown in Figure 5-2, different compliance values can be achieved in the same or different substrates.

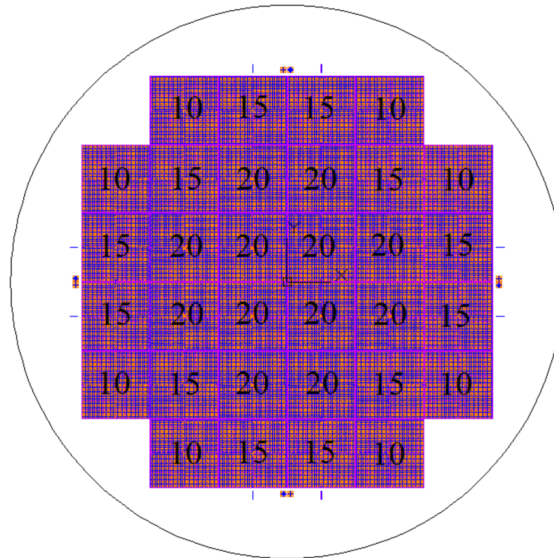


Figure 5-1 Substrate layout on a 6-inch wafer; 10, 15 and 20 represent the arcuate beam width (in µm) of the interconnects fabricated on that substrate

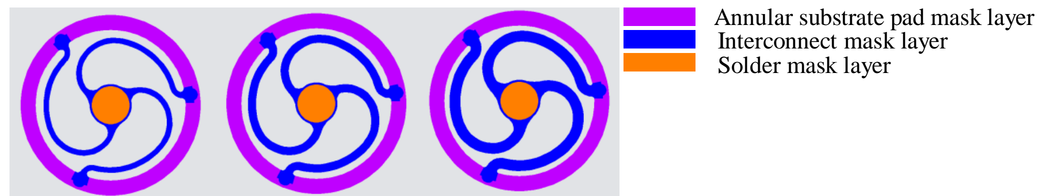


Figure 5-2 Mask design for compliant interconnects with arcuate beam width equal to 10µm, 15µm, and 20µm (from left to right)

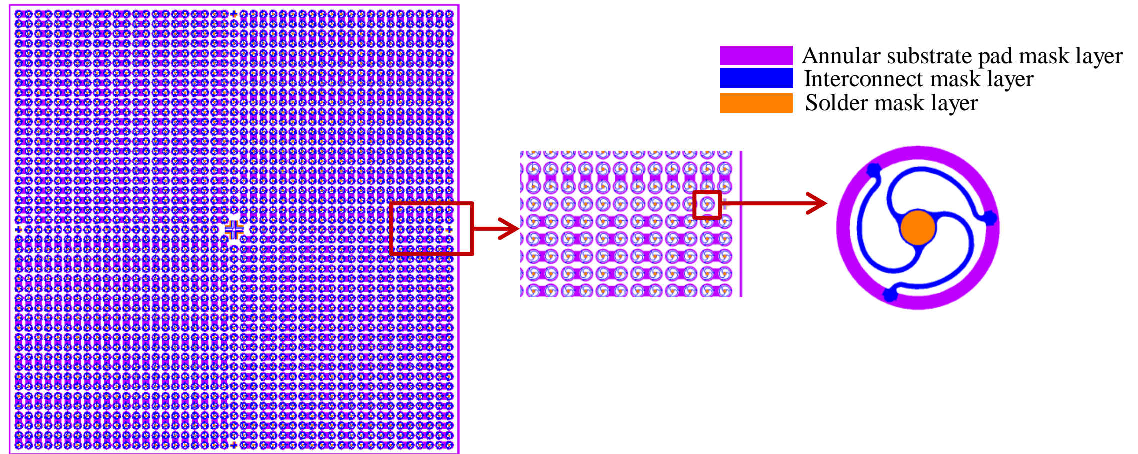


Figure 5-3 Mask design

Figure 5-3 shows the layout of one substrate. A total of three masks were needed for the fabrication. The first mask layer is the annular substrate pad layer, where the annular pads were daisy chained for the purposes of reliability assessment of the 3-Arc-Fan compliant interconnects under thermal cycling tests and drop tests. The second layer is the interconnect layer, and the third layer is the solder layer.

5.2.2. Fabrication Process Overview

The fabrication process of the second-level 3-Arc-Fan compliant interconnects is illustrated step by step in Figure 5-4. A titanium-copper seed layer was sputtered onto the clean wafer and a first layer dry-film photoresist was laminated. The photoresist was exposed to get the pattern for the annular substrate pad followed by the electroplating of the annular substrate pad. A second titanium-copper seed layer was then sputtered onto the wafer and a second-layer photoresist was laminated. The photoresist was then patterned for the interconnect. After electroplating the interconnect, a third-layer photoresist was laminated to define the trench for the solder. A short copper column and then solder were then electroplated which is used for the assembly. The presence of the copper column would ensure that the solder would not wet the arcuate beams during reflow assembly. The photoresist layers and the seed layers were sequentially removed resulting in free-standing interconnects. The last step which is optional is the reflow of

the electroplated solder to form the solder ball. More details will be discussed in the following sections.

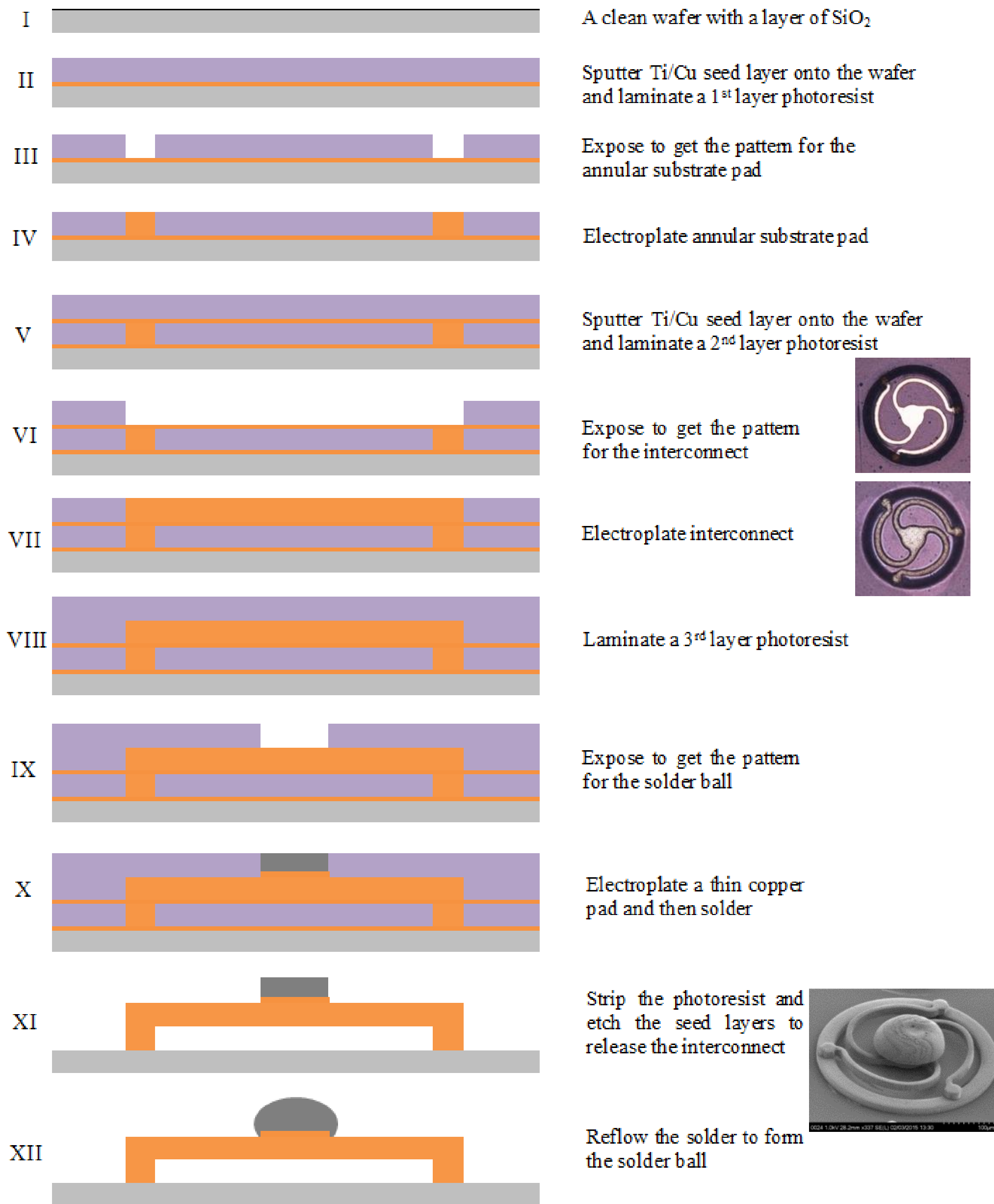


Figure 5-4 Fabrication process of the second-level 3-Arc-Fan compliant interconnects

5.2.3. Annular Substrate Pad Fabrication

The whole process starts from the fabrication of the annular pad because this fabrication was carried out on a blank wafer. A very thin insulating layer of SiO_2 was

first deposited using Oxford® Plasma Enhanced Chemical Vapor Deposition (PECVD) technique on a clean and dried silicon wafer. To ensure good adhesion between copper and silicon, titanium of thickness in the range of 100 - 200Å was then sputtered onto the wafer at a rate of 130Å/min. Copper was then sputtered at a rate of about 1000Å/min to a thickness in the range of 2000 - 2500Å. This relatively thicker copper seed layer is to make sure the uniformity of the electrodeposition under different plating currents for the 6-inch wafer. The sputtering tool used for this fabrication is a UNIFILM® magnetron sputterer capable of achieving uniform deposits with a variation of less than 1%.

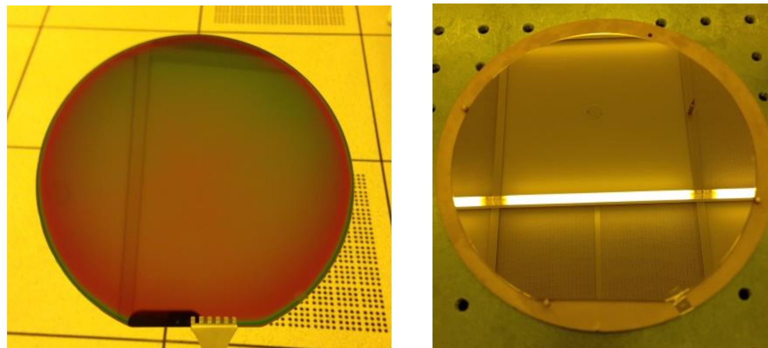


Figure 5-5 A 6-inch wafer with SiO_2 deposited (left) and seed layer sputtered (right)

After the deposition of the Ti/Cu seed layer, a first layer of the dry-film photoresist was laminated using a Hot Roll Laminator. This machine laminates the photoresist by using heat and pressure. The temperature was set at about 120°C for our fabrication. The wafer was then allowed to cool down to the room temperature before the exposure to ultra-violet (UV) radiation (about 15 minutes). Karl Suss® TSA MA6 Mask Aligner was used for the photolithographic exposure of the sample. The UV radiation with a wavelength of 365nm (exposure intensity equal to 25.5mW/cm^2) was performed using the vacuum contact mode which makes the wafer in very tight contact with the mask. The exposure time was determined to be 2.5s after preforming calibration runs.

Following the exposure step is the development of the exposed dry-film photoresist. A time interval more than 15mins between exposure and development is

needed to allow the photoresist to cross-link. After the development, the wafer was thoroughly rinsed using deionized (DI) water and dried using nitrogen gun. Figure 5-6 shows the optical image of the annular substrate pad openings with daisy chain links prior to electroplating.

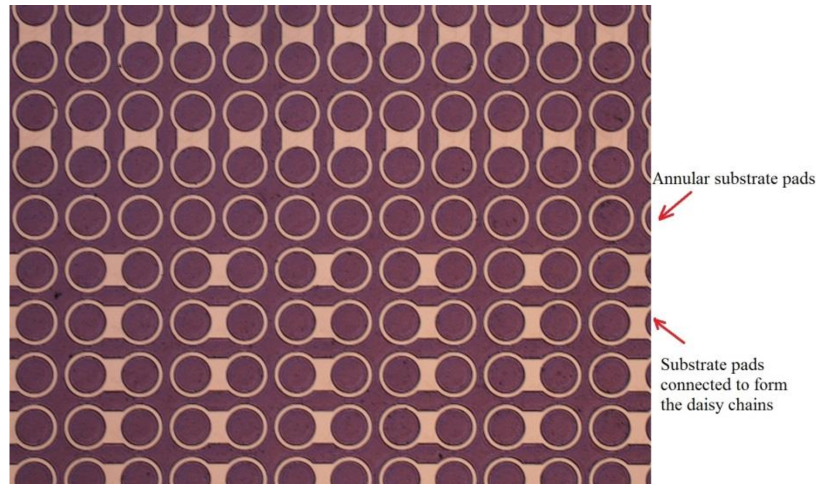
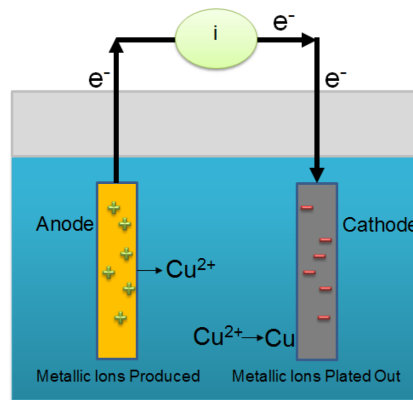


Figure 5-6 Image of the annular substrate pad openings with daisy chain links

Electroplating of copper was performed using a copper sulfate based plating bath, Technic CU 2800, as shown in Figure 5-7. The bath recipe, Table 5-2, was provided by Technic™ and is designed for standard aspect ratio structures, i.e., aspect ratios less than 10. The electroplating bath includes a 5 liter beaker, current source, a teflon coated magnetic stirring rod, a magnetic stirring hotplate, copper anode, and the sample to be plated. The current density used for this fabrication was chosen to be 5mA/cm^2. The current source provided had the capability to supply direct or pulsating direct current. Figure 5-8 and Figure 5-9 show the images of the plated annular substrate pad using constant direct current. However, the electroplating solution must be monitored and checked in order to get the best electroplating results. Figure 5-10 illustrates the electroplated annular pads using solutions with insufficient carrier or insufficient brightener.

Table 5-2 Solution make for standard aspect ratio electroplating

Chemicals Required	1 Liter
Deionized Water	644 ml
Purified Liquid Copper Sulfate [270g/l CuSO4·5H20]	222 ml
C.P. Grade Concentrated Sulfuric Acid (H2SO4)	120 ml
C.P. Grade Concentrated Hydrochloric Acid (HCL)	0.13 ml
TECHNIC CU 2800 Brightener	7.0 ml
TECHNIC CU 2800 Carrier	7.0 ml



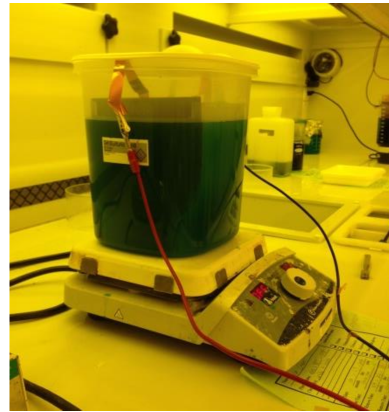


Figure 5-7 Copper sulfate based plating bath

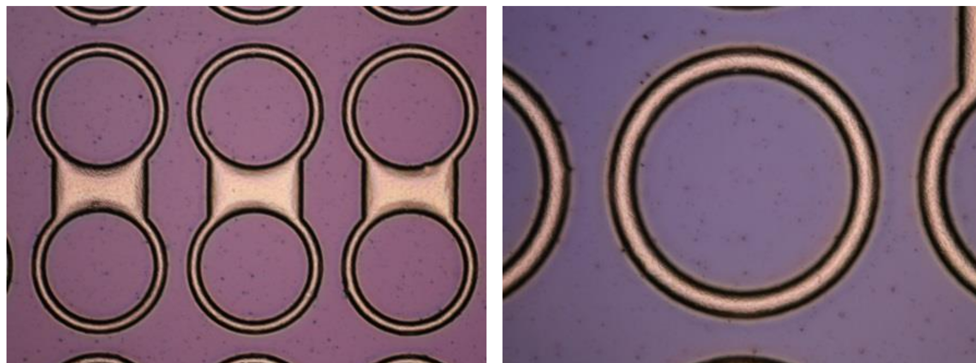


Figure 5-8 Optical images of plated annular substrate pads

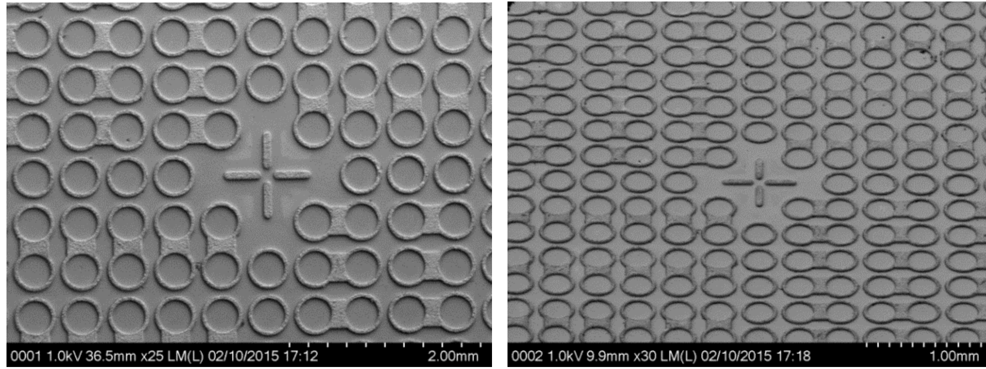


Figure 5-9 SEM images of plated annular substrate pads

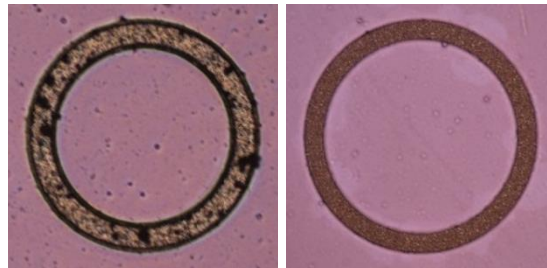
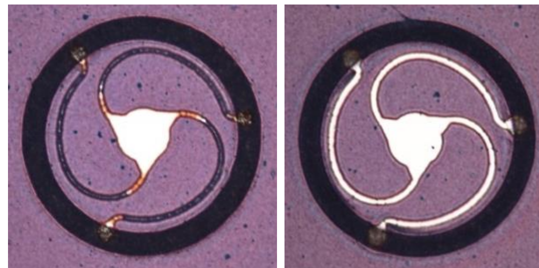


Figure 5-10 Optical images of plated annular substrate pads using electroplating solutions with insufficient carrier (left) or insufficient brightener (right)

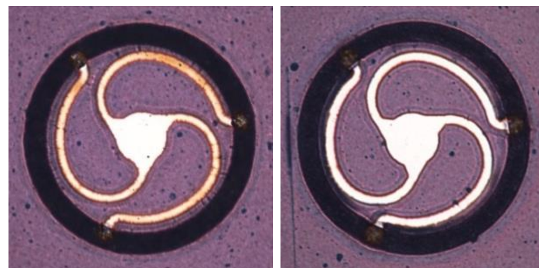
5.2.4. 3-Arc-Fan Compliant Interconnect Layer Fabrication

The wafer must be rinsed thoroughly using DI water and descummed in order to remove the residuals of the additives from the electroplating bath and to ensure good adhesion between the annular pad layer and the interconnect layer. Prior to the lamination of a second layer dry-film photoresist, another copper seed layer was sputtered at a rate of about 1000Å/min to a thickness in the range of 2000 - 2500Å onto the fabricated annular substrate pad layer. The laminated second layer photoresist was then exposed under the UV radiation with a wavelength of 405nm (exposure intensity equal to 50mW/cm^2) using the vacuum contact mode. The exposure time was determined to be 1.1s after the calibration. The high exposure intensity and the vacuum contact mode are preferred due to the fact that the 10μm arcuate beam width of the 3-Arc-Fan compliant interconnect requires for the aspect ratio of the pattern as high as about 2:1. Higher exposure intensity with shorter exposure time and the vacuum contact mode give better resolution for the high aspect ratio design in our work. However, the 365nm wavelength with lower

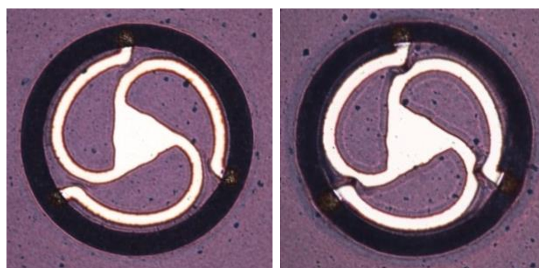
exposure intensity gives better openings for the 20μm beam width. The developed samples were then descummed for 30 minutes to remove the photoresist residuals. Figure 5-11 shows the 3-Arc-Fan compliant interconnect openings after exposure, development, and descum. It is seen that 365nm wavelength with 25.5mW/cm^2 exposure intensity is better for the 20μm arcuate beam width, but 405nm wavelength with 50mW/cm^2 exposure intensity is much better for the 10μm and 15μm arcuate beam widths.



(a). 10μm arcuate beam width



(b). 15μm arcuate beam width



(c). 20μm arcuate beam width

Figure 5-11 Images of the 3-Arc-Fan compliant interconnect openings after exposure, development and descum. The left figures represent the exposures performed by 365nm wavelength (exposure intensity equal to 25.5mW/cm^2) using the vacuum contact mode, while the right figures represent the exposures performed by 405nm wavelength (exposure intensity equal to 50mW/cm^2) using the vacuum contact mode

The 3-Arc-Fan compliant interconnects were plated next using direct current with density equal to 5mA/cm^2 and up to 15µm.The plated interconnects are shown in Figure 5-12.

Figure 5-12 Images of plated 3-Arc-Fan compliant interconnects (from left to right: 10µm, 15µm and 20µm arcuate beam width)

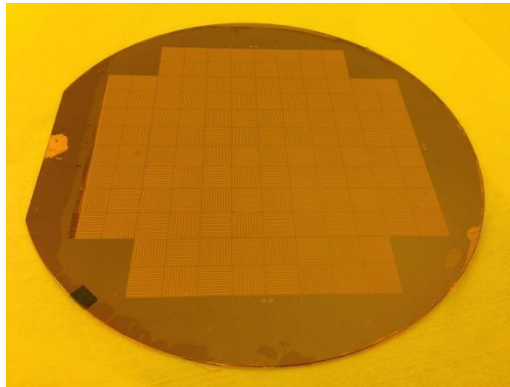


Figure 5-13 A 6-inch wafer with the annular pad and interconnect layers fabricated

5.2.5. Solder Layer Fabrication

A third layer dry-film photoresist was laminated onto the 3-Arc-Fan compliant interconnect layer and exposed using UV with wavelength of either 405nm or 365nm. Before plating the solder, a thin copper pad was first plated. The purpose of the copper pad is to provide a standoff height as well as to ensure that the solder would not wet arcuate beams during reflow. The solder plating solution used is a lead-free eutectic tin-silver solution (3.5% silver) manufactured by Technic©.

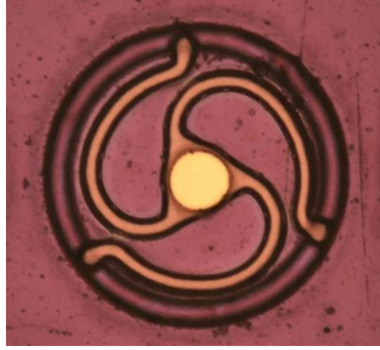


Figure 5-14 Image of the solder opening after exposure

5.2.6. Interconnect Release

The dry-film photoresist layers were stripped using the standard strip solution. Since there are 3 photoresist layers, with some of them covered by the interconnects, it is preferred to put the sample into the strip solution for a longer time at its desired temperature, 55°C. The second seed layer was also removed during stripping the photoresist because this ultra-thin seed layer was sputtered in between the second and third layers of the photoresist. The first copper seed layer was etched away using Copper Etch 49-1 made by Transene Company, Inc. Note that during etch of the 2000 - 2500Å thickness copper seed layer, the copper interconnect structures were also etched and the actual values of the beam widths become 9.5µm, 14.5µm, and 19.5µm after the etchings, respectively. The titanium layer was removed in the plasma system using selective etching gas. After all of the etchings were completed, there was still some photoresist trapped by the interconnects as shown in Figure 5-15. In order to remove such photoresist residuals, the sample was put into a container with acetone solution or DI water and was run in the ultrasonic for certain time. However, it is not uncommon that some of the interconnect might be destroyed during the release, which is illustrated in Figure 5-16. Figure 5-17 through Figure 5-20 show the images of the released interconnects with solder balls plated on the top.

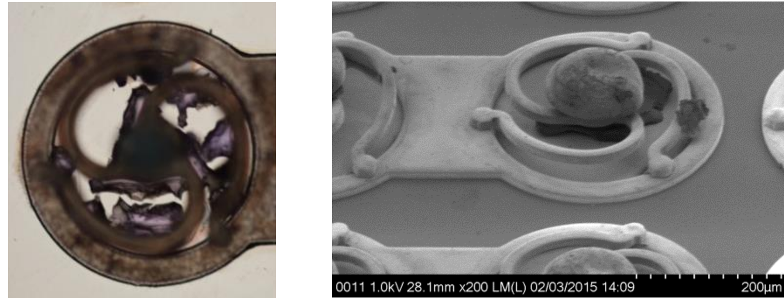


Figure 5-15 Optical and SEM images of dry-film photoresist residuals trapped by the interconnect

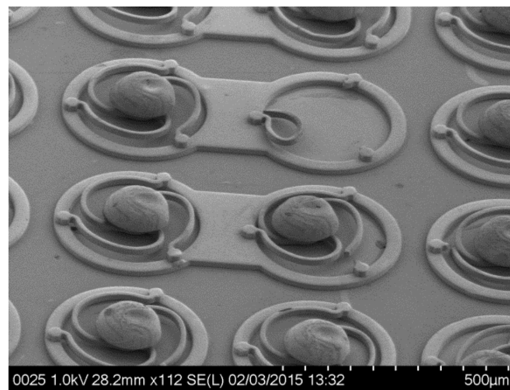


Figure 5-16 SEM image of missing interconnect and arcuate beam breakage

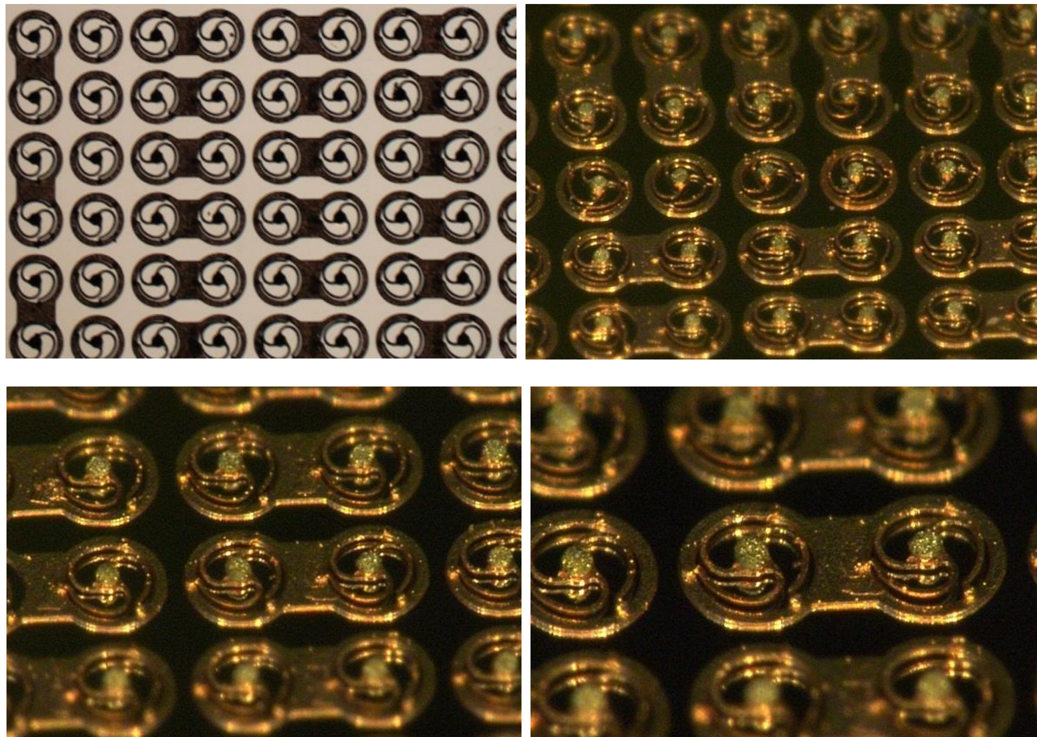


Figure 5-17 Optical images of the released interconnects

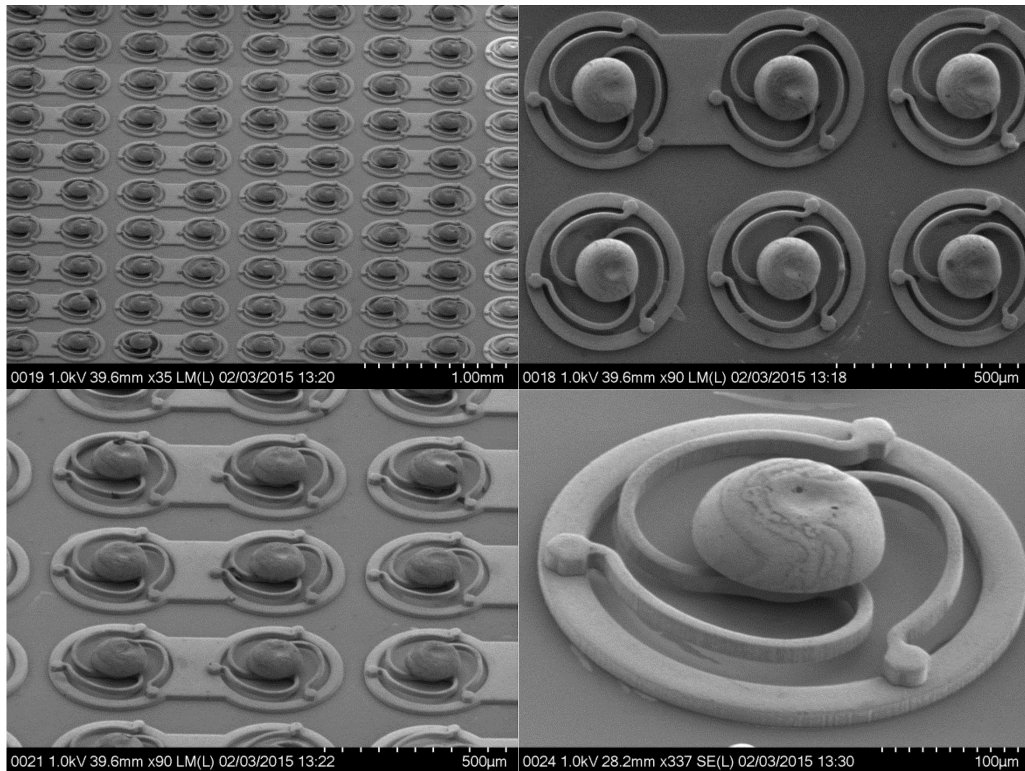


Figure 5-18 SEM of the released interconnects with 10µm arcuate beam width

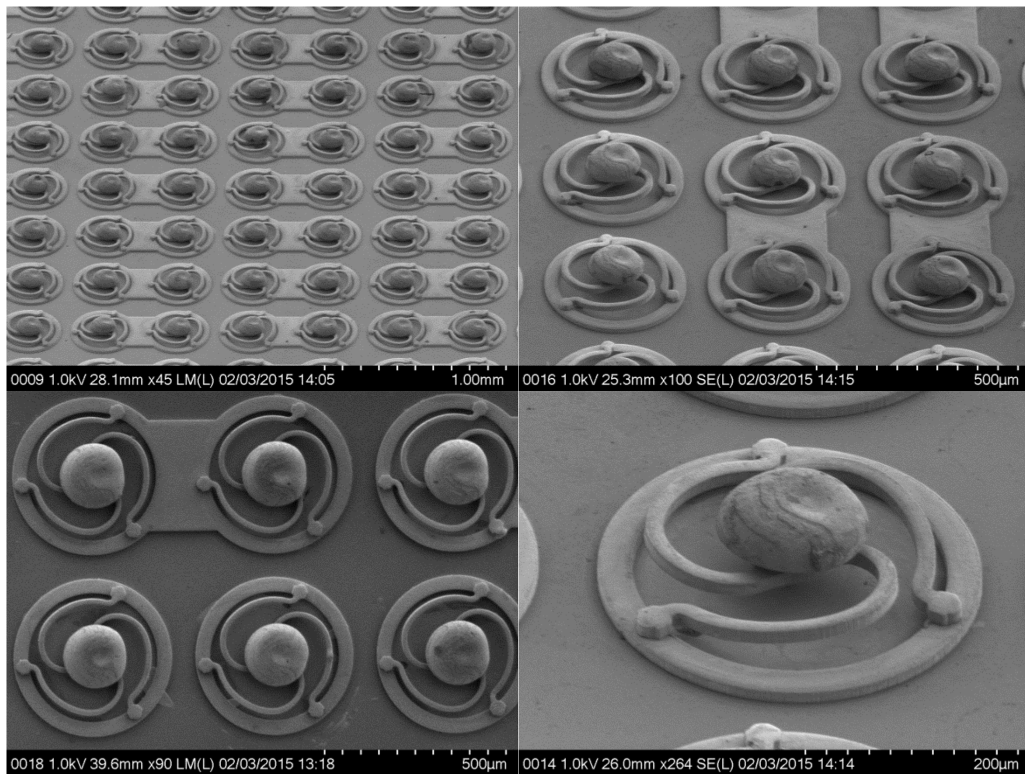


Figure 5-19 SEM of the released interconnects with 15µm arcuate beam width

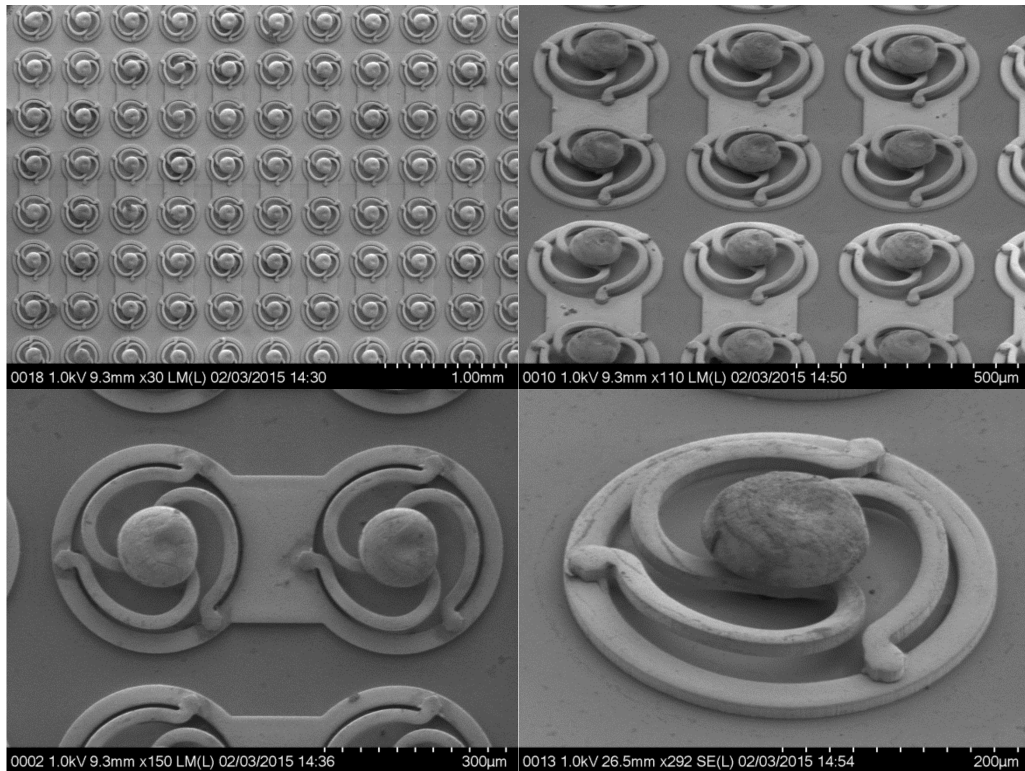


Figure 5-20 SEM of the released interconnects with 20µm arcuate beam width

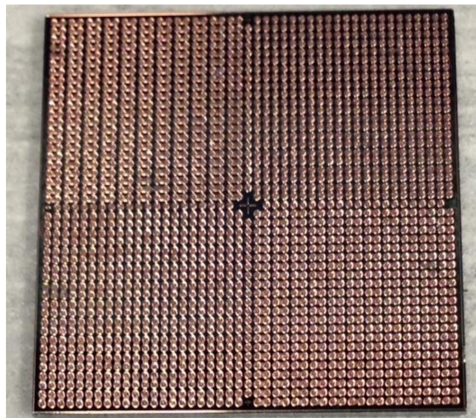


Figure 5-21 45×45 daisy-chained 3-Arc-Fan interconnects fabricated on a 18mm×18mm silicon substrate with 400µm pitch value

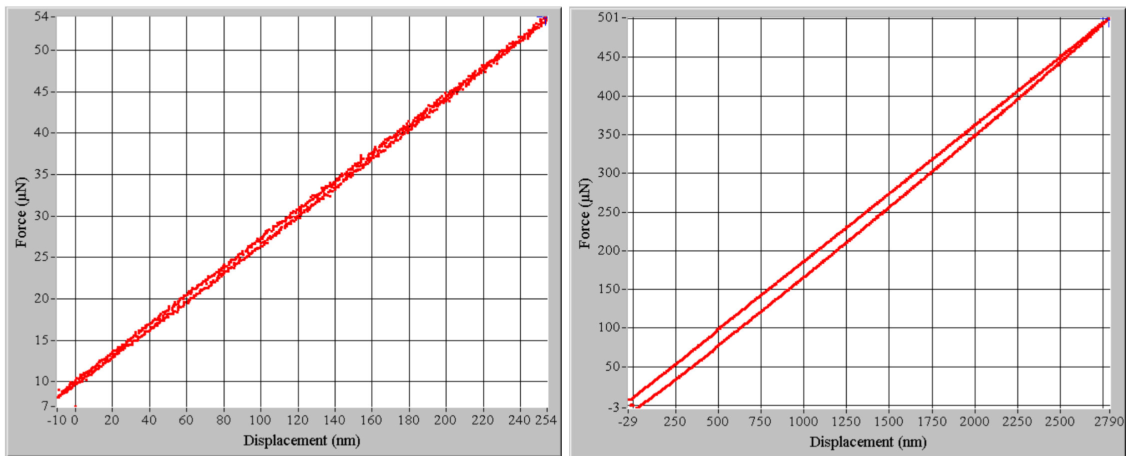
5.3. COMPLIANCE MEASUREMENTS

5.3.1. Experimental Measurements

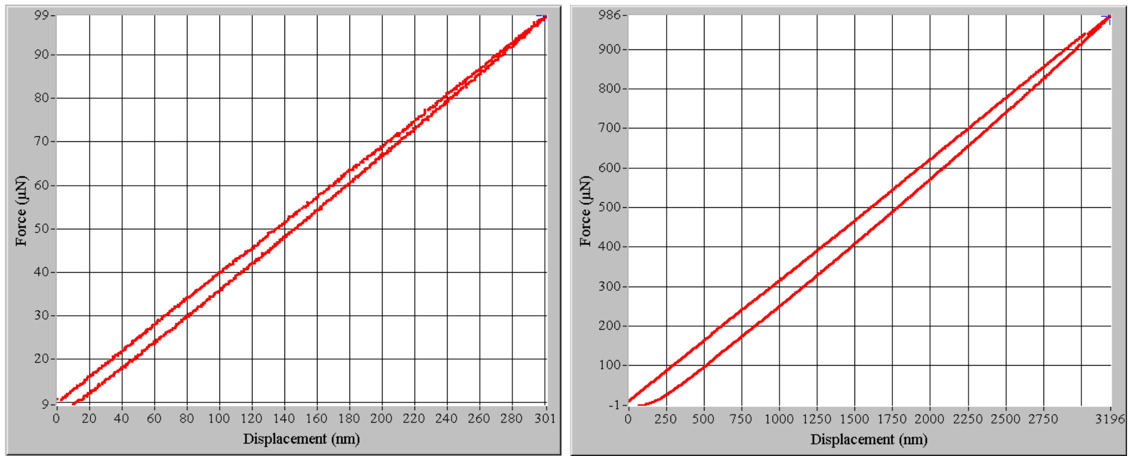
The out-of-plane compliance values of the fabricated 3-Arc-Fan compliant interconnects with different arcuate beam width were measured using Hysitron TriboIndenter®. The samples were mounted on the working plate of the machine, and the

Flat Punch tip applied the load onto the center of the 3-Arc-Fan interconnects (solder cap) in the out-of-plane direction according to the pre-defined load function. The compliance values can be calculated from the unloading force-displacement curves. The measured force-displacement curves of the interconnects with various arcuate beam widths are shown in Figure 5-22. It can be seen that all the measurements with either large displacement (≈ 3µm) or small displacement (≈ 0.3µm) exhibit almost linear force-displacement curves, so the compliance values of those 3-Arc-Fan interconnects are constant under the externally applied loads. This is because even though there are certain plastic deformation regions within the 3-Arc-Fan interconnects under large deformation, the overall compliance values depend on the whole structure of the interconnects and the portion of the plastic deformation regions is very limited.

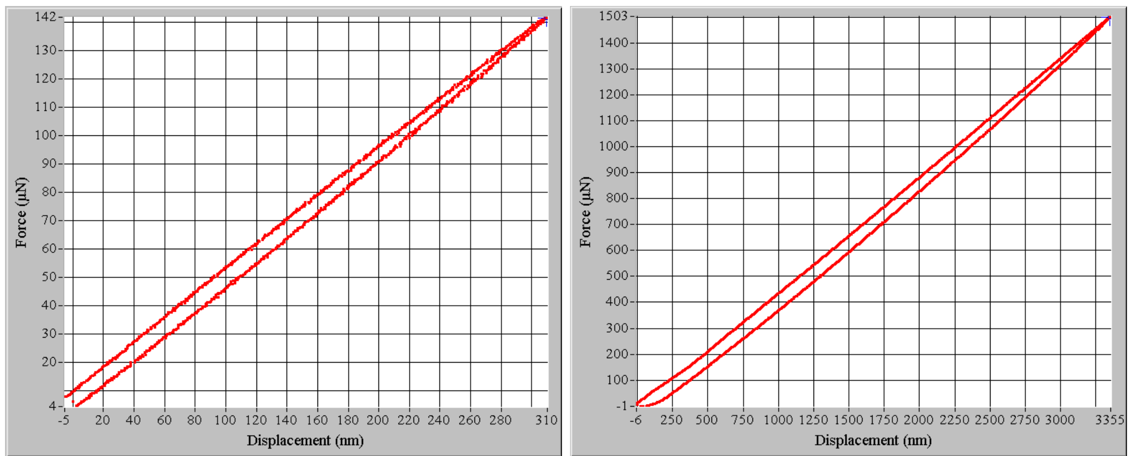
The out-of-plane compliance values were measured for different samples, and the compliance values calculated from the measured unloading curves are given in Table 5-3 through Table 5-5. It can be seen that the out-of-plane compliance values of the designed 3-Arc-Fan compliant interconnect are 4 - 5 orders of magnitude greater than that of the solder balls.



(a). arcuate beam width = 9.5µm



(b). arcuate beam width = 14.5µm



(c). arcuate beam width = 19.5µm

Figure 5-22 Force-displacement curves of the out-of-plane compliance values for the interconnects with beam width equal to 9.5µm, 14.5µm, and 19.5µm. The plots on the left represent the measurements with small displacement, while the plots on the right represent the measurements with large displacement. The compliance values are obtained from the unloading curves (the lower curve in each figure) and calculated as displacement over force. E.g., the compliance value measured on the left plot of Figure 5-22 (c) is calculated as C_m = 310nm/(142 - 4)µN = 2.25mm/N.

Table 5-3 Measured out-of-plane compliance values (mm/N) for the interconnects with beam width equal to 9.5μm

Sample	Displacement	Compliance
Sample 1	Large Displacement	5.59
	Small Displacement	5.74
Sample 2	Large Displacement	5.49
	Small Displacement	5.91
Sample 3	Large Displacement	5.25
	Small Displacement	5.14
Average: 5.52		

Table 5-4 Measured out-of-plane compliance values (mm/N) for the interconnects with beam width equal to 14.5μm

Sample	Displacement	Compliance
Sample 1	Large Displacement	2.87
	Small Displacement	3.02
Sample 2	Large Displacement	3.11
	Small Displacement	3.23
Sample 3	Large Displacement	2.76
	Small Displacement	2.85
Average: 2.97		

Table 5-5 Measured out-of-plane compliance values (mm/N) for the interconnects with beam width equal to 19.5μm

Sample	Displacement	Compliance
Sample 1	Large Displacement	2.23
	Small Displacement	2.25
Sample 2	Large Displacement	2.28
	Small Displacement	2.41
Sample 3	Large Displacement	2.19
	Small Displacement	2.49
Average: 2.31		

5.3.2. Numerical Simulation

The compliance values of the interconnects with different beam width values were also simulated in ANSYS® with the assumption that the Young's modulus of the copper is 117GPa.

5.3.2.1. Out-of-Plane Compliance

Figure 5-23 shows the applied force and the boundary conditions used to obtain the out-of-plane compliance values in ANSYS®. The contour plots of the nodal out-of-plane displacement are shown in Figure 5-24 where the out-of-plane compliance values can be readily obtained from.

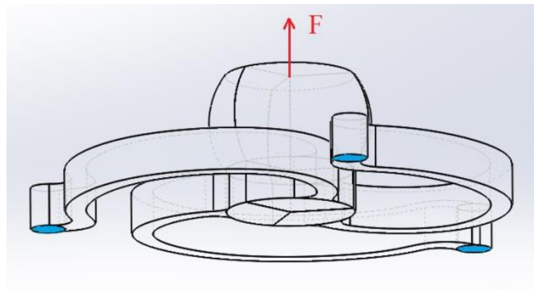
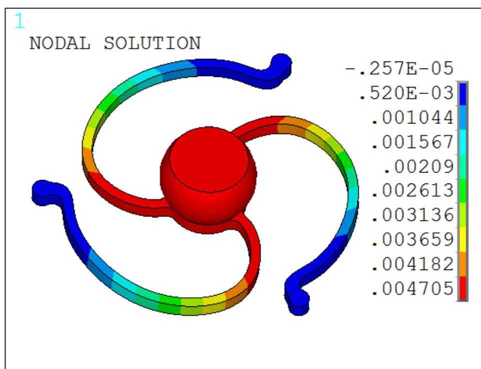
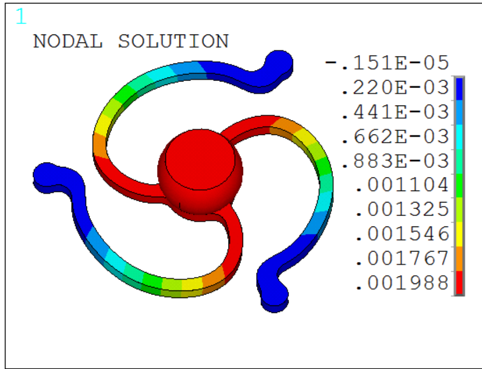


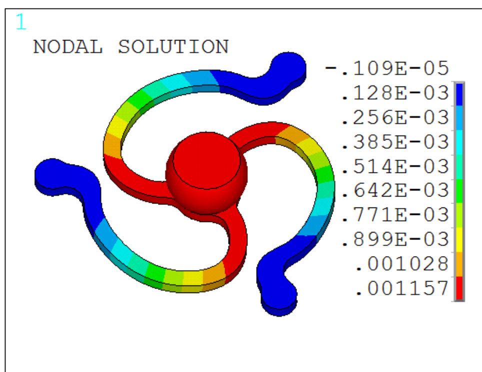
Figure 5-23 Simulation set up for the out-of-plane compliance analysis in ANSYS®. The places where the arcuate beams are connected to the annular substrate pad were fixed and the load was applied in the out-of-plane direction at the solder center.



(a). arcuate beam width = 9.5μm



(b). arcuate beam width = 14.5μm



(c). arcuate beam width = 19.5μm

Figure 5-24 Contour plots of the nodal out-of-plane displacement for the interconnects with beam width equal to 9.5μm, 14.5μm, and 19.5μm

Table 5-6 shows the comparison of the measured and simulated out-of-plane compliance values for the interconnects with beam width equal to 9.5μm, 14.5μm, and 19.5μm. It can be seen that the measured values are consistently larger than the simulated values. It is believed that one of the main reasons for the discrepancy is the Young's modulus of copper used in the ANSYS® model, because the Young's modulus of electroplated copper could vary between 30GPa and 200GPa depending on the plating parameters used as reported by [21]. The other main reason is the dimension used in the ANSYS® model, because the beam width may not be exactly 9.5μm, 14.5μm or 19.5μm, and the beam thickness may be slightly different from 14.5μm as well. Note that C_m/C_s increases from 1.17 to 1.99 with the increase of the arcuate beam width. This is mainly

because of different grain sizes or/and different porosity of the electroplated copper within different patterns.

Table 5-6 Comparison of the measured and simulated out-of-plane compliance values for the interconnects with beam width equal to 9.5μm, 14.5μm, and 19.5μm

Arcuate Beam Width [μm]	9.5	14.5	19.5
Measured Out-of-plane Compliance Values C_m[mm/N]	5.52	2.97	2.31
Simulated Out-of-plane Compliance Values C_s[mm/N]	4.71	1.99	1.16
C_m/C_s	1.17	1.49	1.99

5.3.2.2. In-Plane Compliance

The in-plane compliance values for all the three different beam widths were also simulated in ANSYS®. Figure 5-25 shows the applied force and the boundary conditions used to obtain the out-of-plane compliance values in ANSYS®. The contour plots of the nodal in-plane displacement are shown in Figure 5-26 where the in-plane compliance values can be readily obtained from.

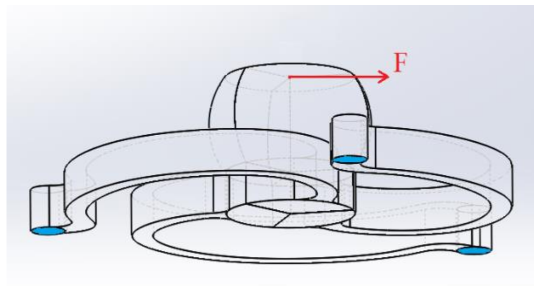
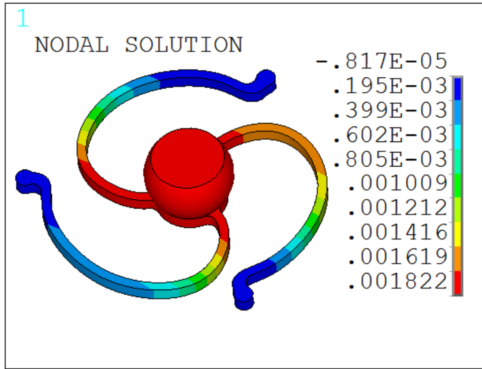
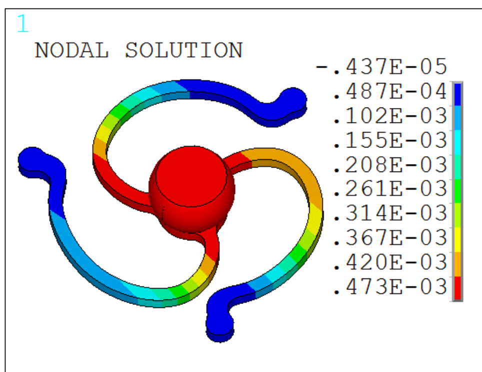


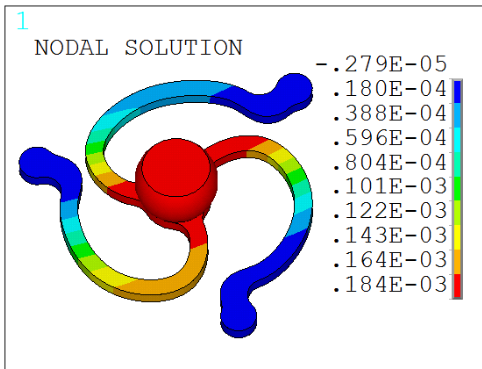
Figure 5-25 Simulation set up for the in-plane compliance analysis in ANSYS®. The places where the arcuate beams are connected to the annular substrate pad were fixed. The load was applied in the in-plane direction at the solder center and the nodes at the area where the load was applied were coupled.



(a). arcuate beam width = 9.5μm



(b). arcuate beam width = 14.5μm



(c). arcuate beam width = 19.5μm

Figure 5-26 Contour plots of the nodal in-plane displacement for the interconnects with beam width equal to 9.5μm, 14.5μm, and 19.5μm

Table 5-7 shows the simulated out-of-plane and in-plane compliance values for the interconnects with beam width equal to 9.5μm, 14.5μm and 19.5μm.

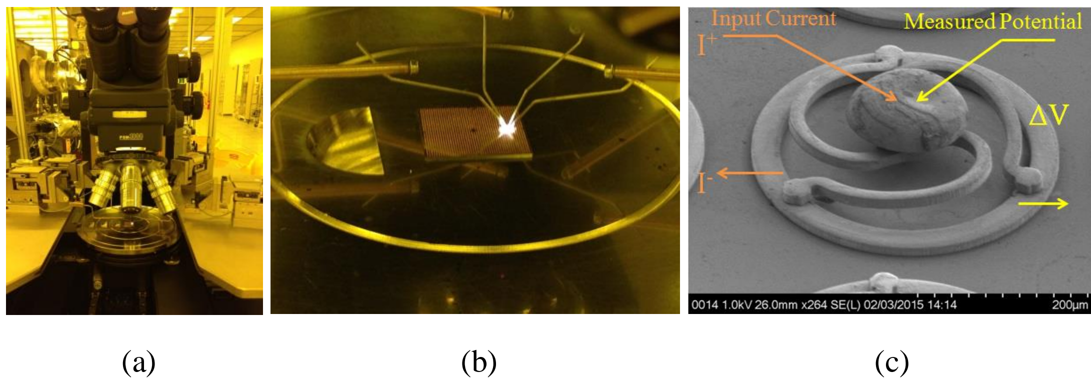
Table 5-7 Simulated out-of-plane and in-plane compliance values for the interconnects with beam width equal to 9.5μm, 14.5μm, and 19.5μm

Arcuate Beam Width [μm]	9.5	14.5	19.5
Simulated Out-of-Plane Compliance Values $C_{out\text{-}of\text{-}plane}$[mm/N]	4.71	1.99	1.16
Simulated in-Plane Compliance Values $C_{in\text{-}plane}$[mm/N]	1.82	0.47	0.18

5.4. ELECTRICAL RESISTANCE MEASUREMENTS

5.4.1. Experimental Measurements

The electrical resistance values of the fabricated 3-Arc-Fan compliant interconnects with different arcuate beam width were measured using Signatone® probe station. The sample was fixed on the working plate of the machine via vacuum, with four probe tips (two pairs) used to measure the resistance, as shown in Figure 5-27 (a) and (b). The first pair was used to provide the input current, one tip applied on the top of the solder ball and the other applied on the annular substrate pad, shown as orange arrows in Figure 5-27 (c). The other pair, shown as yellow arrows in Figure 5-27 (c), was used to measure the potential, with one tip applied on the top of the solder ball and the other applied on the annular substrate pad. The measured resistance values of the interconnects with various arcuate beam widths are shown in Table 5-8.



(a) (b) (c)

Figure 5-27 Resistance measurement setup using probe station

Table 5-8 Measured resistance values for the interconnects with beam width equal to 9.5µm, 14.5µm, and 19.5µm

Arcuate Beam Width [µm]	Resistance Measurements [mΩ]		Average Resistance [mΩ]
9.5	Interconnect 1	12.7	12.47
	Interconnect 2	12.5	
	Interconnect 3	12.2	
14.5	Interconnect 1	8.3	8.43
	Interconnect 2	8.6	
	Interconnect 3	8.4	
19.5	Interconnect 1	6.1	6.13
	Interconnect 2	6.1	
	Interconnect 3	6.2	

5.4.2. ANSYS® Simulation

The resistance values for the interconnects with three different beam widths were also simulated in ANSYS® with the assumption that the resistivity of the copper is $1.68\times10^{-8}\Omega\cdot m$ and resistivity of the solder $7.7\times10^{-8}\Omega\cdot m$ [52]. Figure 5-28 shows the applied boundary conditions used to obtain the resistance values in ANSYS®. The current value was then read as the "reaction forces" either on the top of the solder ball or the bottom of the annular pad in the post process, and the resistance was calculated using $R = U/I$.

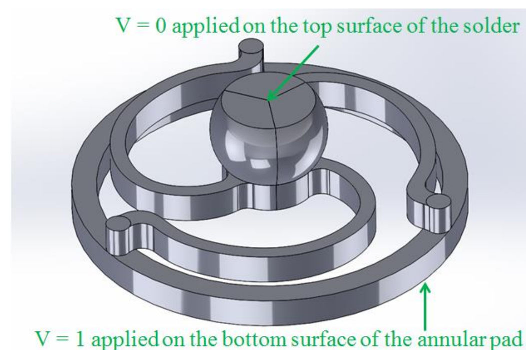


Figure 5-28 Applied boundary conditions used to obtain the resistance values in ANSYS®

Table 5-9 Comparison of the measured and simulated resistance values for the interconnects with beam width equal to 9.5μm, 14.5μm, and 19.5μm

Arcuate Beam Width [μm]	9.5	14.5	19.5
Measured Resistance Values R_m[mΩ]	12.47	8.43	6.13
Simulated Resistance Values R_s[mΩ]	16.10	10.67	8.01
R_s/R_m	1.29	1.27	1.31

Table 5-9 shows the comparison of the measured and simulated resistance values for the interconnects with beam width equal to 9.5μm, 14.5μm, and 19.5μm. It can be seen that the resistance values calculated from the simulation are 27% ~ 31% larger than those obtained from the experiments. The average difference is 29%. Since the contribution of the bulk solder ball to the resistance values is much smaller than the slender arcuate beams, the difference between the measured and simulated values can be attributed to the resistivity value of copper used in the simulation model. The electroplated copper usually has different resistivity from the bulk copper [53, 54]. Therefore, the resistivity of the copper in the fabricated 3-Arc-Fan compliant interconnect can be approximated as $1.68\times10^{-8}\Omega\cdot m/1.29 = 1.30\times10^{-8}\Omega\cdot m$.

CHAPTER 6 DEVELOPMENT OF ASSEMBLY PROCESS

6.1. INTRODUCTION

The assembly process is to attach the silicon substrate to the board in order to form the signal/power communication between the substrate and the board. Due to the mechanical compliance property, the 3-Arc-Fan compliant interconnects will be compressed together with the solder balls when the compression force is applied during the bonding. Due to the complexity of the geometry of the 3-Arc-Fan compliant interconnect, there are several challenges in the development of assembly process including determining the compression force so that the compliant interconnects do not permanently deform, creating a thermal profile to ensure solder melting, applying appropriate amount of flux to ensure solder bonding, etc. Under the compression load, the compliant interconnect will deform to accommodate the non-flatness of the substrate/board and the standoff discrepancy of the different compliant interconnects. These phenomena are different from the traditional BGA bonding where the solder balls are the only components that accommodate the compression force and the substrate/board warpages.

6.2. ASSEMBLY PROCESS

6.2.1. Assembly Process Overview

Shown in Figure 6-1 is the main assembly steps that includes surface finish of the copper pads, cleaning the substrate and the board, alignment, adjusting the compression force, applying the flux, applying the compression force, reflow and cleaning of the assembly.

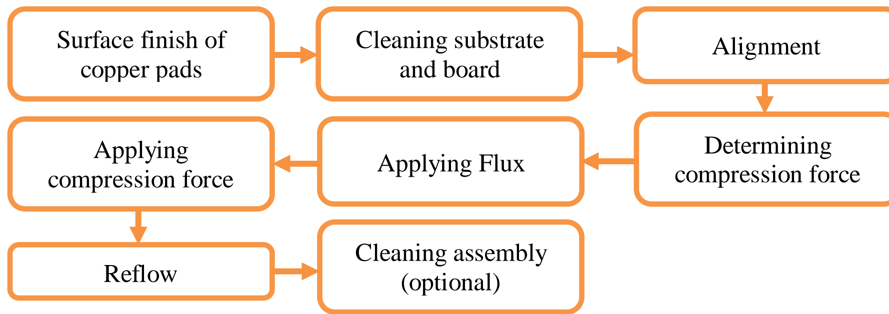


Figure 6-1 Assembly process overview

6.2.2. Preparation Steps

The preparation steps involve the surface finish of the copper pads and the cleaning of the silicon substrate and the organic board.

The surface finish is very crucial to providing reliable assemblies. There are several types of surface finish including organic solderability preservatives (OSP), immersion tin, immersion silver, direct immersion gold (DIG), electroless nickel immersion gold (ENIG), electroless nickel, electroless palladium, immersion Gold (ENEPIG), etc. However, in this work, only a small amount of samples were assembled and no surface finishes were applied for the boards. Instead, the copper pads on the boards were micro-etched in 5% H_2SO_4 solutions and then dried before the next step. This is to get rid of the oxides from the copper pads, because the oxidized copper pads can prevent the wetting of the pads reducing the reliability of the solder joints.

The silicon substrate and the board to be assembled must be thoroughly cleaned using acetone in order to remove the contaminant. The contaminant can affect the reflow process and form the voids inside the reflowed solder balls. The substrate and the board were then dried using nitrogen gun to get rid of the acetone.

6.2.3. Alignment

The Finetech® flip-chip bonder, shown in Figure 6-2, was used for the assembly process. It is a very high precision flip-chip bonder and is capable of submicron alignment accuracy which makes it relatively easy to align the components with 400um

pitch. The alignment was done at room temperature. Figure 6-3 shows very good alignment results obtained.

Figure 6-2 Finetech® flip-chip bonder

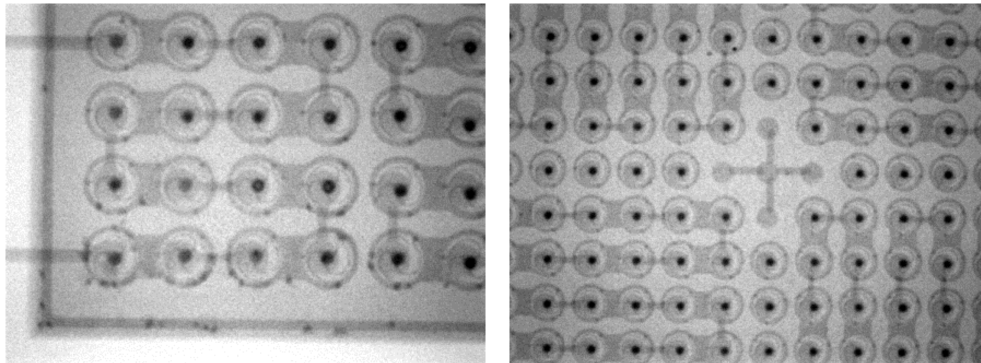


Figure 6-3 X-ray inspected sample alignment

6.2.4. Determining Compression Force

Properly selecting the compression force is very critical to the assembly process. During the reflow process, the substrate was placed over the board. The silicon substrates are usually flat, but the organic boards have notable warpage at the room temperature. Although the vacuum applied to fix the board on the heat plate of the flip-chip bonder can significantly reduce the warpage of the board, it cannot be completely eliminated. The 3-Arc-Fan compliant interconnects together with solder balls capped on the top were fabricated via electroplating, and there is usually about 10% standoff discrepancy. Therefore, due to the warpage of the organic board and the 10% standoff discrepancy of

the compliant interconnects, if the silicon substrate is placed over the board without any compression force, some of the interconnects will not form a good bond with the board.

However, due to the mechanical compliance property, the 3-Arc-Fan compliant interconnects will be compressed together with the solder balls when the compression force is applied during the bonding, and the compliant interconnect will deform as well to accommodate the non-flatness of the board and the standoff discrepancy of the compliant interconnects. These phenomena are different from the traditional BGA bonding where the solder balls are the only components that accommodate the compression force and the substrate/board warpages.

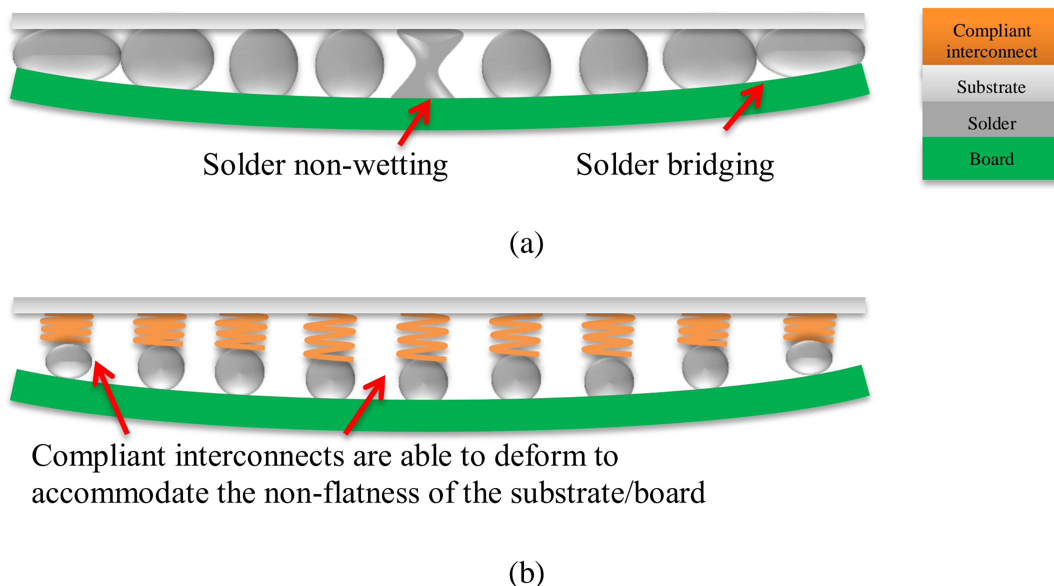


Figure 6-4 Comparison between solder ball interconnects and 3-Arc-Fan compliant interconnects (the 3-Arc-Fan structure is replaced by the spring shape to better demonstrate the deformation of the compliant interconnects) in the assembly process

Figure 6-4 (a) shows that when the solder balls are the only components that accommodate the compression force and the board warpage in the BGA bonding, the solder could have the non-wetting and/or the bridging issues. Figure 6-4 (b) shows that the non-wetting and the bridging issues can be completely avoided because (1) the compliant interconnects are able to deform to accommodate the non-flatness of the

substrate/board and the standoff discrepancy; (2) much less solder is needed for the assembly. Therefore, although there are several challenges in the assembly process when using compliant interconnects, the advantages are also significant.

The compression force helps to make sure that all of the compliant interconnects are properly connected to the board via the reflowed solder joints, and the amount of the compression force to be applied during the assembly depends on both the electroplated solder cap volume and the out-of-plane compliance value of the compliant interconnect. If a relatively small amount of the solder balls are electroplated and wetting of the arcuate beams of the 3-Arc-Fan compliant interconnect is not a concern, the applied compression force can be calculated according to the out-of-plane compliance value of the compliant interconnect. For example, for the compliant interconnect with the arcuate beam width equal to 10μm, the out-of-plane compliance value is 5.52mm/N, and the standoff of the compliant interconnect is the total height of the annular copper pad and the arcuate beam which is about 30μm. The 10% standoff discrepancy together with the warpage of the board require that the compression force should be able to compress the interconnects on the substrate by at least 3μm. There are about 2000 compliant interconnects fabricated on one substrate and the compression load can be calculated as $3\mu m/(5.52mm/N)\times 2000 \approx 1.1N$. The compression forces calculated for the compliant interconnects with the arcuate beam width equal to 15μm and 20μm are about 2.0N and 2.6N, respectively.

But if the solder cap volume is relatively large, the applied compression force calculated based on the out-of-plane compliance value of the compliant interconnect will not only compress the interconnects but also squash the solder balls resulting in wetting of the arcuate beams during the reflow, because the surface tension of the liquid state of the solder ball is much lower than the applied compression force distributed on each compliant interconnect. In this case, instead of applying the compression force, pre-define the distance between the tool head and the plate is preferred. The distance between the tool head and the plate will then determine the standoff of the compliant interconnect.

For example, if a relatively large amount of solder ball was electroplated on the top of the compliant interconnect, and the thickness of the solder ball is 30μm before reflow, the total height of the compliant interconnect is now about 60μm after adding the thickness of the annular copper pad and the thickness of the arcuate beam. Therefore, the 10% standoff discrepancy and the warpage of the board require that the standoff of the compliant interconnect should be about 54μm after reflow to ensure that all of the compliant interconnects are properly connected to the board via the reflowed solder joints. A spacer with the right thickness can be used in order to achieve this expected standoff.

6.2.5. Applying Flux

After adjusting the compression force or adding the spacer, a very thin layer of flux was then dispensed onto the copper pads on the organic board as shown in Figure 6-5.

The primary purpose of applying flux is to prevent oxidation of the solder and copper pads. The solder ball attaches very well to copper, but the copper is oxidized very quickly at the relatively high reflow temperature and the solder ball can barely attached to the oxidized copper pad. Applying flux during the reflow process can prevent the formation of metal oxides. In addition, the oxidation on the surface of the solder prevents it from reflowing and flux allows solder to flow easily instead of forming beads.

The reason why the flux should be dispensed after the alignment and the adjustment of the compression force is because 1) the copper pads on the board become hardly to be distinguished after applying the flux making the alignment more difficult; 2) it usually takes several minutes to finish the alignment process and the flux may evaporate during this process resulting in insufficient amount of flux for the reflow.

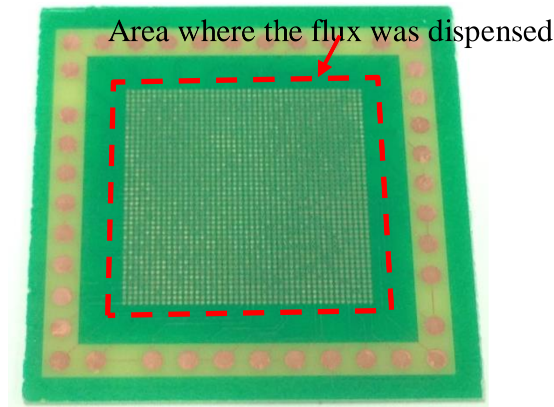


Figure 6-5 Flux dispensed onto the copper pads on the organic board

The flux used in this work was Alpha NR200. This is a low solids, halide-free, rosin/resin free and no-clean flux for soldering. It also provides high activity with virtually no visible residue with most solder masks [55].

6.2.6. Applying Compression Force

The compression load or the pre-defined distance was then applied while placing the substrate over the board. It is very important that the compression load is applied at the center of the substrate to avoid the incline of the substrate that will result in non-landing issue. Figure 6-6 is the cross-section view of the assembly from two opposite sides. It is shown that the compliant interconnects on one side are bonded well to the board but those on the other side present the non-landing problem.

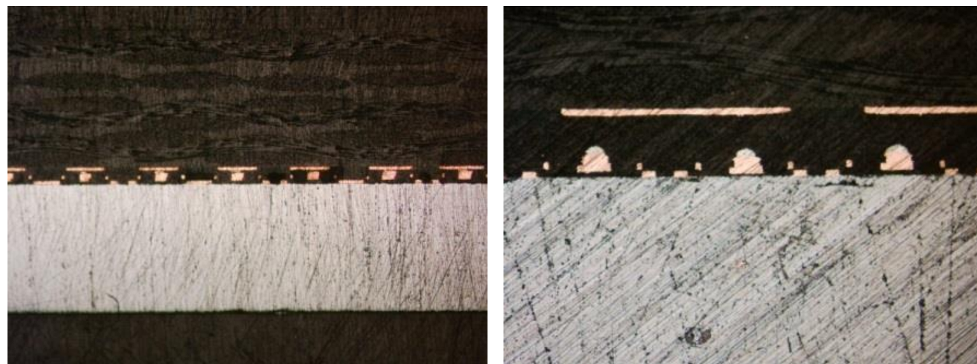


Figure 6-6 Cross-section showing landing on one side but non-landing on the other side

6.2.7. Reflow

The sample was then reflowed under certain temperature profile as shown in Figure 6-7 which is created based on the JEDEC J-STD-020D. The soak temperature for lead-free based assemblies was 150°C and the peak reflow temperature was less than 260°C. But these values were increased by 20ºC to 30ºC because of the relative larger substrate size (18mm × 18mm) and board size (3mm × 33mm for the samples used in the thermal cycling test and 132mm × 77mm for the samples used in the drop tests) in this work, which formed the temperature gradient inside the substrate and the board. Increasing the temperature by 20ºC to 30ºC ensures the reflow the solder balls, so does the 50s reflow time at the peak reflow temperature.

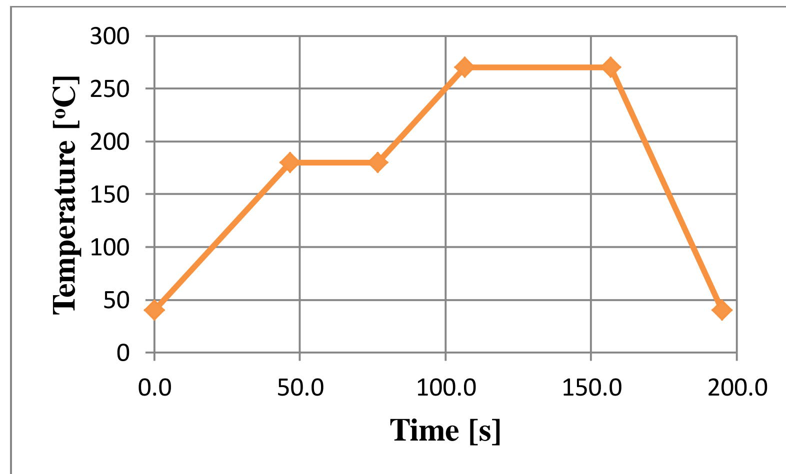


Figure 6-7 Reflow temperature profile

Both the plate heat and the chip heat were applied during the reflow to make sure that all of the solder balls were able to reach the reflow temperature. Shown in Figure 6-8 is a silicon substrate (18mm × 18mm × 0.675mm) assembled on an organic board (33mm × 33mm × 0.75mm) through solder reflow using Finetech® flip-chip bonder and this sample will be used for the thermal cycling test.

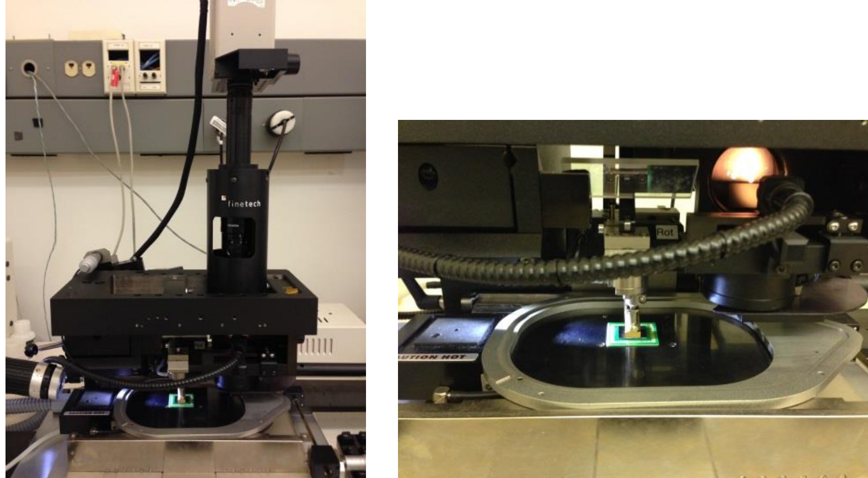


Figure 6-8 A silicon substrate (18mm × 18mm × 0.675mm) assembled on an organic board (33mm × 33mm × 0.75mm) through solder reflow using Finetech® flip-chip bonder

6.2.8. Assembly Checking

The assembled samples must be inspected via non-destructive methods, visual examination under X-ray and electrical measurement using designed daisy chains, to ensure that the silicon substrate was properly mounted on the organic board.

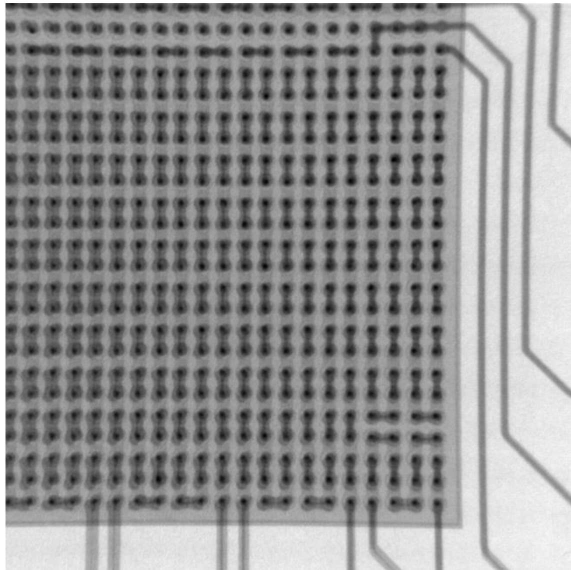


Figure 6-9 X-ray image of daisy chains designed to check the integrity of the assembly

Both the silicon substrate and the FR4 board have inbuilt daisy chain patterns specifically designed to assess the assembly as well as for the thermo-mechanical

reliability and drop tests. The daisy-chain resistance measurement at different locations of a sample is a good way to determine if there is a non-landing issue or not. Figure 6-9 shows some of the daisy chains designed to check the integrity of the assembly. Figure 6-10 shows close-up view of one well assembled sample.

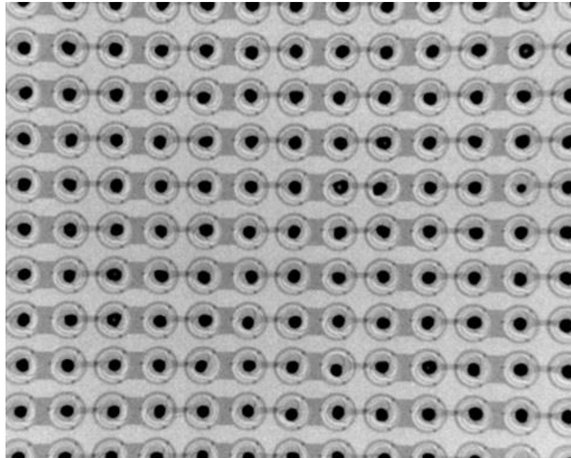


Figure 6-10 X-ray image of close-up view of one well assembled sample

However, some of the daisy chains may show the open loops because of missing compliant interconnect during the fabrication shown in Figure 6-11, which is not uncommon and does not mean that the sample was not properly assembled. The resistance values of the daisy chains measured after the assembly will be used as the time zero value for the thermal cycling test or the drop test in the future.

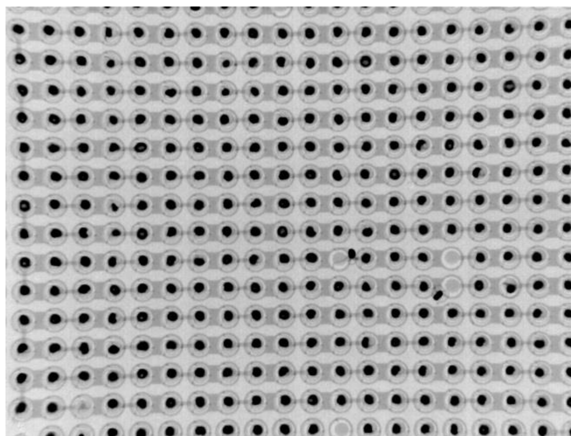


Figure 6-11 Missing compliant interconnects due to the fabrication

The X-ray inspection helps to check the status of the solder balls after reflow, e.g. wetting of the arcuate beams (Figure 6-12) and voids inside the solder balls (Figure 6-13). In addition, it is capable of showing the initial shapes of the compliant interconnects before the thermal cycling test or the drop test is conducted. It also helps to identify the compliant interconnects that are poorly deformed after the assembly and before any tests, shown in Figure 6-14, so that it can be determined whether a failure is present after the assembly process (indicates poor yield) or whether the failure occurs during subsequent reliability testing.

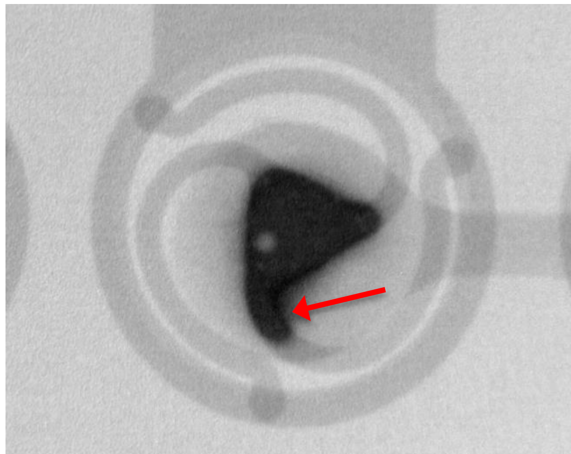


Figure 6-12 X-ray image showing wetting of the arcuate beams

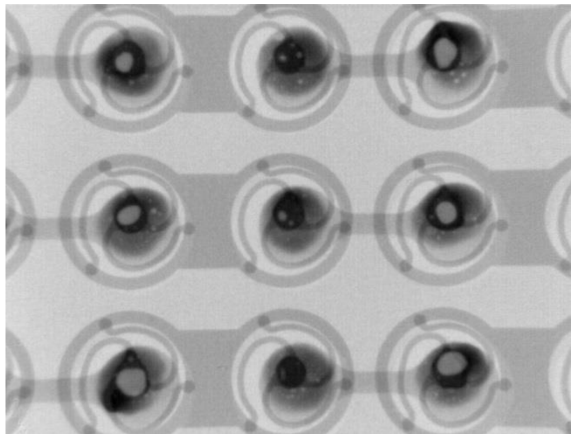


Figure 6-13 X-ray image showing the voids inside a solder ball

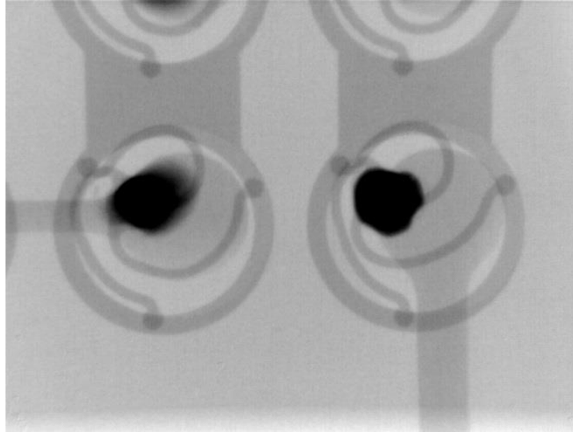


Figure 6-14 Poorly deformed compliant interconnect after assembly

CHAPTER 7 THERMAL CYCLING RELIABILITY ASSESSMENT

7.1. INTRODUCTION

One of the most important reliability tests of the interconnect is its thermal cycling reliability. The thermo-mechanical reliability assessment is to evaluate the fatigue life of the interconnect under thermal cycling. The objective of this chapter is to experimentally assess the thermo-mechanical reliability and compare against theoretical predictions.

7.2. EXPERIMENTAL THERMAL CYCLING TEST

7.2.1. Experimental Setup

Copper compliant interconnects were fabricated on silicon wafer at pitch value equal to 400μm, through sequential cleanroom fabrication processes. The silicon wafer was diced into 18mm×18mm×0.675mm silicon substrates and assembled on organic FR-4boards (33mm × 33mm × 0.75mm) through solder reflow, as shown in Figure 6-8.

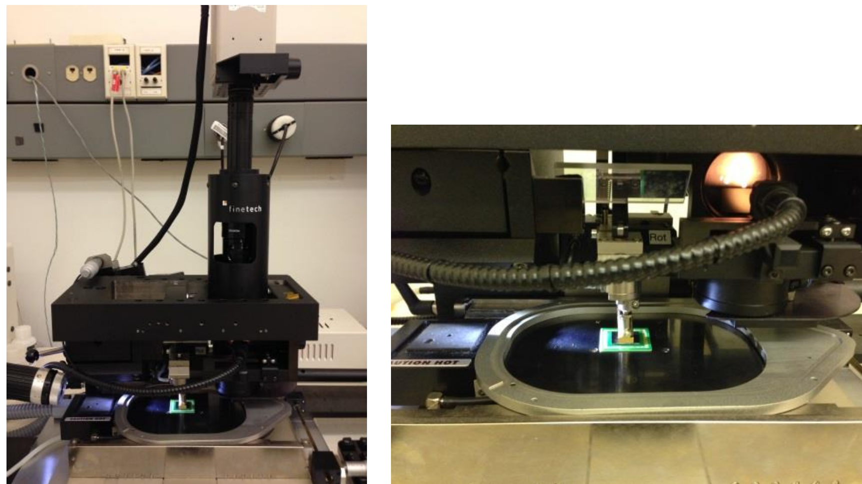


Figure 7-1 A silicon substrate (18mm × 18mm × 0.675mm) assembled on an organic board (33mm × 33mm × 0.75mm) through solder reflow using Finetech® flip-chip bonder

However, one more layer of silicon substrate was attached in order to mimic the situation where there is die stack on the top of the silicon substrate. Figure 7-2 shows the

test sample consists of an 18mm×18mm×1.35mm die stack and a 33mm×33mm×0.75mm organic board, bonded by the 3-Arc-Fan interconnects

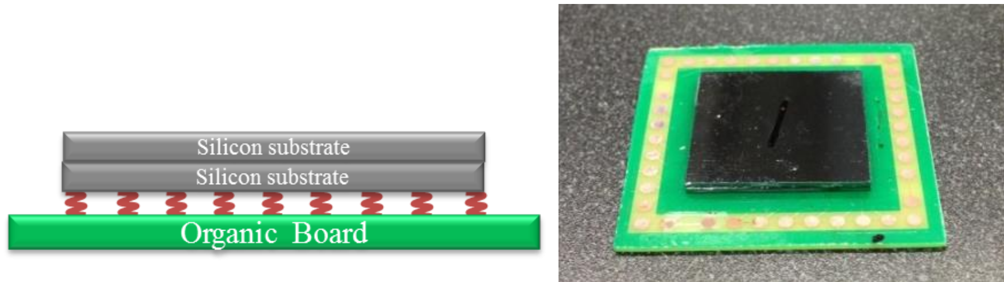


Figure 7-2 The test sample consists of an 18mm × 18mm × 1.35mm die stack and a 33mm × 33mm × 0.75mm organic board, bonded by the 3-Arc-Fan interconnects

The daisy chain patterns at the four corners were designed. Each daisy chain connects the 4 × 4 compliant interconnects at that corner, as shown in Figure 7-3. The compliant interconnects at the four corners of the assembly are believed to be the most critical due to the fact that they are the outermost interconnects and have the most deformation under thermal cycling load.

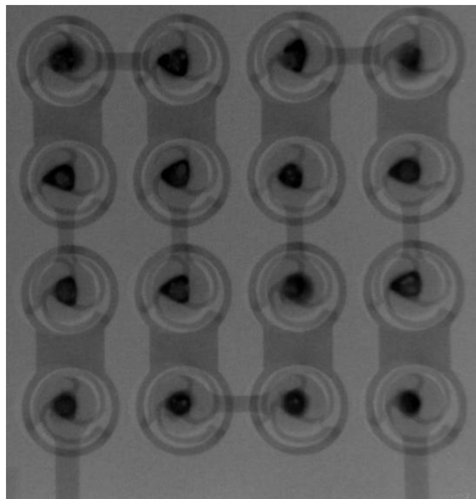


Figure 7-3 Layout of the daisy chain connecting 4 × 4 compliant interconnects at the corner

The thermal cycling chamber used to conduct the test is manufactured by ESPEC® as shown in Figure 7-4. This chamber can be programmed to run thermal cycling tests with different intended load profiles.

Figure 7-4 Thermal cycle chamber manufactured by ESPEC®

The JEDEC standard (JESD22-A104D) test condition G with $T_{\min}$ = -40°C and $T_{\max}$ = 125°C was used. The ramp time and dwell time are 15 minutes and it is 60 minutes for one complete cycle. Shown in Figure 7-5 is the thermal load profile used for the thermal cycling test.

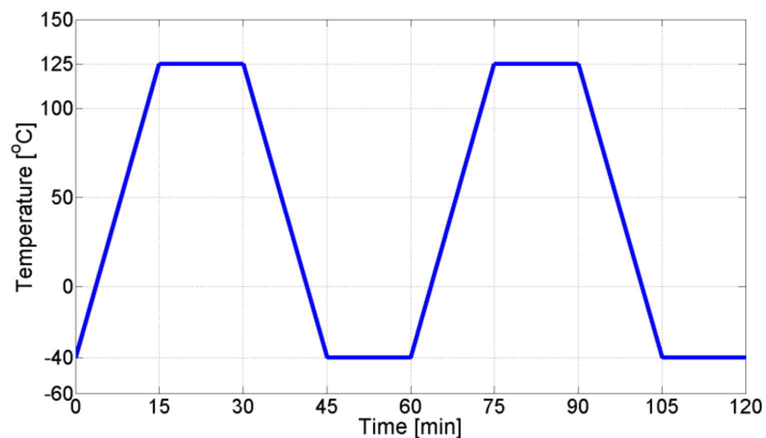
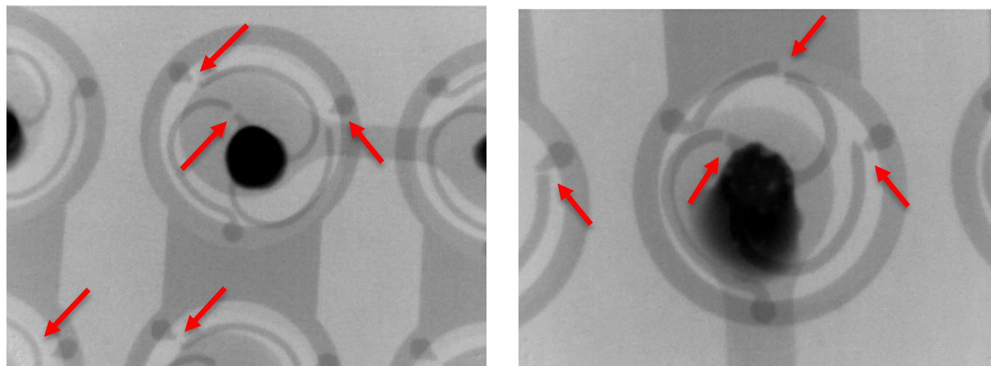


Figure 7-5 Thermal load profile showing two thermal cycles

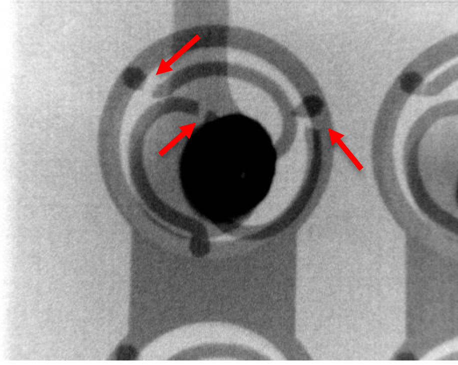
The electrical resistance of daisy-chained interconnects of each package on the test board was monitored and the samples were examined using Dage X-Ray XD7600NT® to detect the failure location after each 50 cycles. The Dage X-Ray XD7600NT® provides very high resolution and large X-ray images for failure analysis. The 3-Arc-Fan interconnect consists of three parallel arcuate beams, so it will not be considered as failure unless all three arcuate beams in the same interconnect are broken,

which can also be detected and confirmed under the X-ray. The breakage of one arcuate beam during the test increases the daisy-chain resistance by several milliohms. The resistance will increase by several orders if all three arcuate beams in at least one of the interconnects are broken (open circuit), and this type of resistance increase will be considered as package failure. Figure 7-7 shows the X-ray images of the typical failure locations for different arcuate beam width under thermal cycling loads. The fatigue failures are mostly at the locations where the arcuate beams connect to the annular substrate pads and the copper pad underneath the solder balls. Figure 7-7 (b) also shows that the failures sometimes happen at the center of the arcuate beams

Figure 7-6 Dage X-Ray XD7600NT®



(a) 10μm (b) 15μm



(c) 20µm

Figure 7-7 X-ray images of typical failure locations for different arcuate beam width; the fatigue failures are mostly at the locations where the arcuate beams connect to the annular substrate pads and the copper pad underneath the solder balls; (b) also shows that the failures sometimes happen at the center of the arcuate beams

7.2.2. Measured Daisy-Chain Resistance

The change of daisy-chain resistance values over thermal cycles for the samples with 3-Arc-Fan interconnects beam width equal to 10µm, 15µm and 20µm were measured and recorded in Figure 7-8, Figure 7-9 and Figure 7-10, respectively. The daisy-chain resistance values were measured at every 50 cycles.

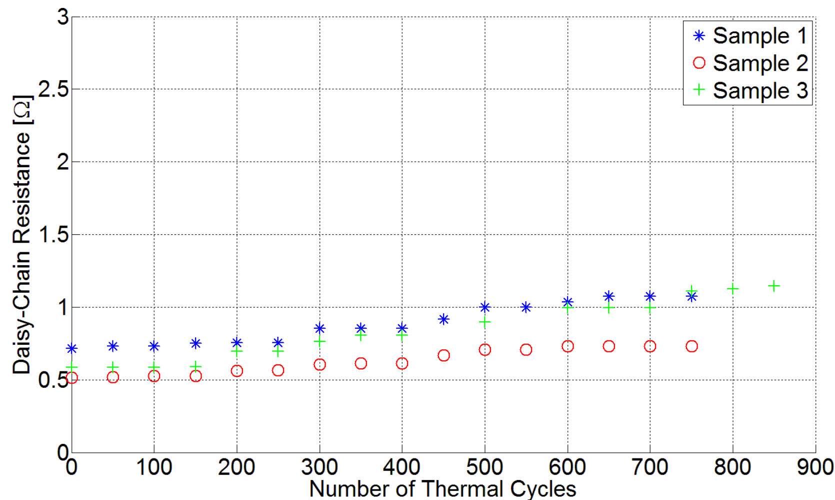


Figure 7-8 Change of daisy-chain resistance over thermal cycles for the samples with 3-Arc-Fan interconnects beam width equal to 10µm

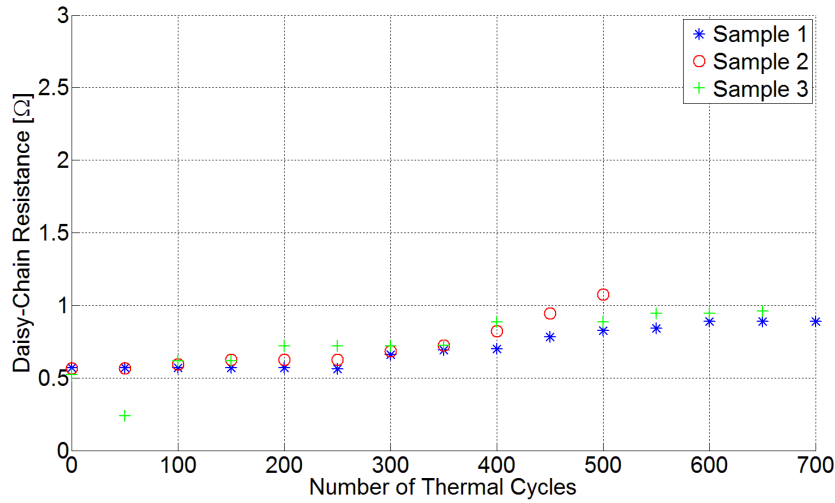


Figure 7-9 Change of daisy-chain resistance over thermal cycles for the samples with 3-Arc-Fan interconnects beam width equal to 15µm

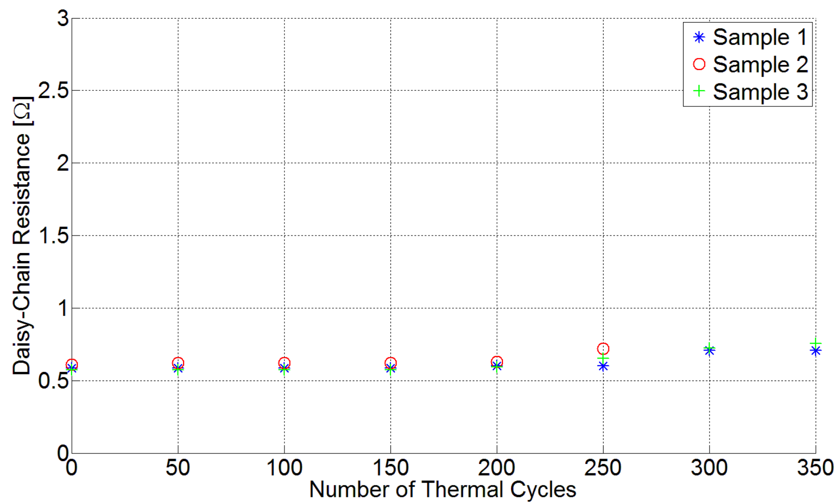


Figure 7-10 Change of daisy-chain resistance over thermal cycles for the samples with 3-Arc-Fan interconnects beam width equal to 20µm

For the 10µm beam width samples, two survived more than 750 cycles and one survived more than 850 cycles. For the 15µm beam width samples, Sample 1 survived more than 500 cycles, Sample 2 more than 650 cycles and Sample 3 more than 700 cycles. For the 20µm beam width samples, two survived more than 350 cycles and one survived more than 250 cycles. Those fatigue lives are summarized in Table 7-1. Since the measurement was taken at every 50 cycles, the exact fatigue life cannot be obtained.

As a best estimation, if the failure is found at the Nth cycle the fatigue life is determined to be N – 25. For instance, sample 1 in Figure 7-8 survived up to 750 cycles but failed at 800 cycles, so the its fatigue life was determined to be 800 – 25 = 775 cycles. Since only small amount of samples were tested, the average fatigue life was calculated and used instead of the characteristic fatigue life, shown in Table 7-2.

Table 7-1 Thermal cycling fatigue lives for the packages assembled using 3-Arc-Fan interconnects with different beam width

	Sample 1	Sample 2	Sample 3
10µm	$750 < N_f < 800$	$850 < N_f < 900$	$750 < N_f < 800$
15µm	$500 < N_f < 550$	$650 < N_f < 700$	$700 < N_f < 750$
20µm	$350 < N_f < 400$	$250 < N_f < 300$	$350 < N_f < 400$

Table 7-2 Average thermal cycling fatigue lives for the packages assembled using 3-Arc-Fan interconnects with different beam width

	Sample 1	Sample 2	Sample 3	Average
10µm	775	875	775	808
15µm	525	625	725	625
20µm	375	375	375	341

7.3. THERMAL CYCLING SIMULATION

7.3.1. Finite-Element Model

The assembly consists of 2020 compliant interconnects at a 400-µm pitch, sandwiched between the 18mm×18mm×1.35mm silicon substrate and 33mm×33mm×0.75mm organic substrate. The thermal cycling simulation includes multiple load steps and different nonlinear material properties. Such nonlinear simulation with multiple load steps could take several days to solve. To reduce the simulation time, a strip model that extracted from the full model was used.

The strip model only takes into account one row of the compliant interconnects as well as the silicon substrate and the organic board they are attached to. The width of the strip model is equal to the product of $\sqrt{2}$ and the pitch of the interconnect. The strip

model is a simplified 3D geometry that preserves the 3D nature of the structure but significantly reduced the number of elements and therefore the computational time compared to the full 3D model. It is capable to generate very accurate results if appropriate boundary conditions are applied. The strip model extracted from the full model for the thermal cycling simulation is shown in Figure 7-11. Only half of the strip was extracted because of the symmetry.

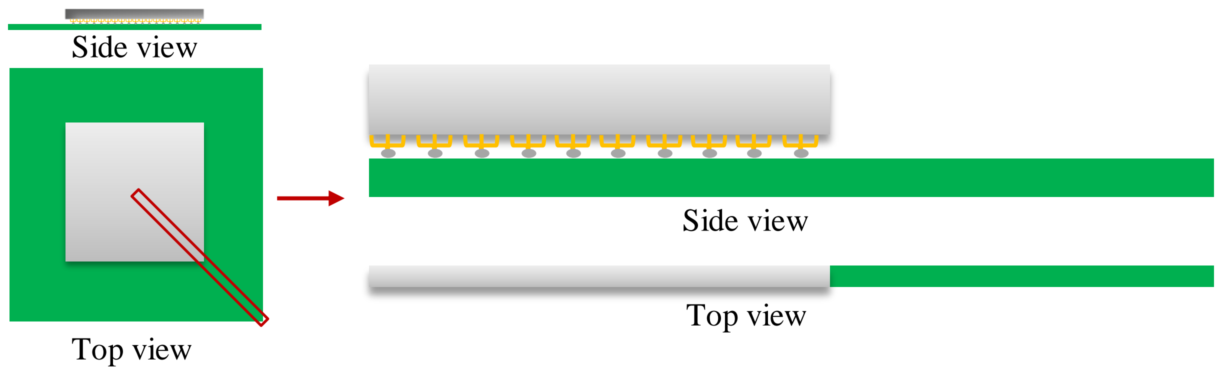


Figure 7-11 Strip model extracted from the full model

Illustrated in Figure 7-12 are the boundary conditions applied to the strip model. The displacement of the four lateral planes (two in the board and two in the substrate, normal to the *Y* coordinate) in the *Y*-direction is coupled, respectively, so the nodes on individual plane can only expand or contract by the same amount in the *Y*-direction. This is to ensure that the strip model is not a free stand model but a cut-out model from the full one. At the rear cut end of the strip, the displacement in the *X*-direction is constrained because of the symmetry. One of the nodes at the bottom of the FR-4 board is fixed in all directions to prevent rigid body motion.

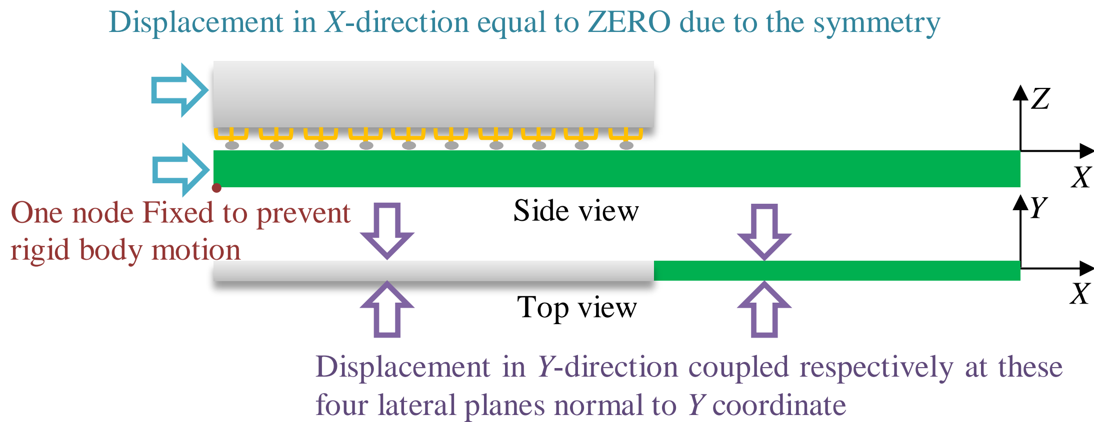
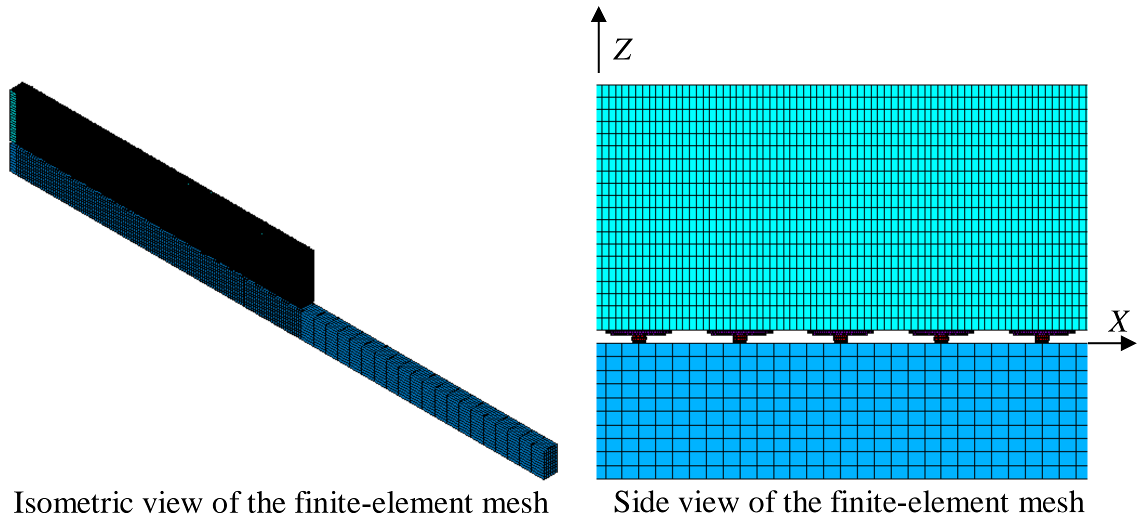


Figure 7-12 Boundary conditions for the strip model

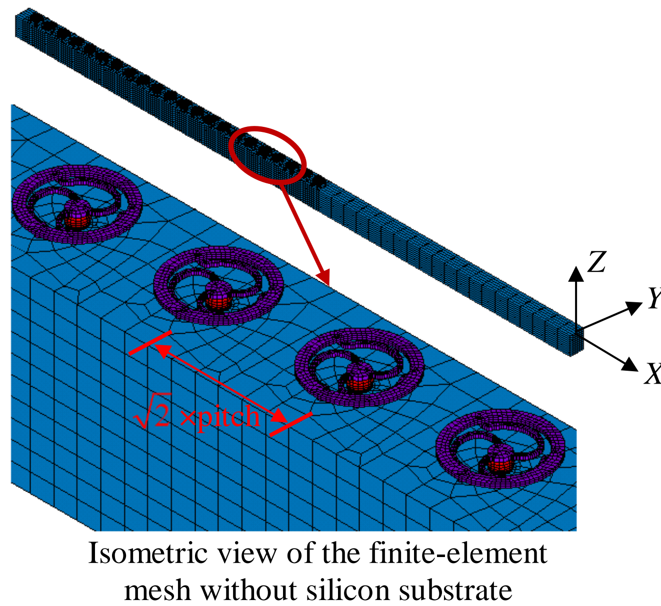
The model used for simulation was created using SOLID185 elements, defined by eight nodes having three degrees of freedom (displacements in the nodal *X*, *Y* and *Z* directions) at each node.

The total numbers of elements created for the assemblies with the interconnect beam width equal to 10µm, 15µm and 20µm were about 536,000, 359,000 and 242,000, respectively. The reason why the finite-element model with smaller interconnect beam width requires for larger number of elements is that, 1) the structure having smaller dimension needs smaller meshes near it in order to prevent the poorly shaped elements; 2) the dimension of the whole model ranges from the order of 10µm to the order of 10mm, and the change of the element size should be gradually in order not to form the poorly shaped elements. The mesh size control is shown in Figure 7-13. However, the results obtained from the simplified strip model should be interpreted and applied with caution.



Isometric view of the finite-element mesh

Side view of the finite-element mesh



Isometric view of the finite-element mesh without silicon substrate

Figure 7-13 Mesh size control for the strip model (green: silicon substrate; blue: FR-4 board; purple: copper; red: solder)

7.3.2. Material Properties

The mechanical material properties of silicon substrate, FR-4 board (orthotropic), copper and solder used in the finite-element simulations are listed as below. The same material properties were used in the impact isolation (Chapter 9) and drop test reliability simulations (Chapter 10).

Table 7-3 Material properties of silicon substrate

Property	Values				
Young's modulus as a function of temperature (GPa)	218K	273K	323K	373K	500K
	125.85	120.85	114.85	109.85	94.85
Coefficient of thermal expansion (ppm/K)	2.6				
Poisson's ratio	0.25				
Density (kg/m^3)	2320				

Table 7-4 Primary material properties of the orthotropic FR-4 board at room temperature

Property	Values	
	In-plane	Out-of-plane
Young's modulus (GPa)	22.4	1.6
Shear modulus (GPa)	0.199	0.630
Coefficient of thermal expansion (ppm/K)	16	25
Poisson's ratio	0.1425	0.1360
Density (kg/m^3)	1850	

Table 7-5 Material properties of solder

Property	Values					
Young's modulus as a function of temperature (GPa)	248K	298K	333K	373K	423K	500K
	58.88	49.22	42.47	34.75	25.10	10.23
Coefficient of thermal expansion (ppm/K)	24					
Poisson's ratio	0.4					
Density (kg/m^3)	7360					

Anand viscoplasticity model (source: [56])		
Property	**Meaning**	**Values**
Initial value of deformation resistance	s_o	39.09 MPa
Activation Energy/Universal gas const.	Q/R	8900 K^{-1}
Pre-exponential factor	A	22300 1/s
multiplier of stress	ξ	6
strain rate sensitivity of stress	m	0.182
hardening/softening constant	h_o	3321.2 MPa
coefficient for deformation resistance saturation	$\hat{s}$	73.81 MPa
strain rate sensitivity of saturation	n	0.018
strain rate sensitivity of hardening or softening	a	1.82

Table 7-6 Material properties of copper

Property	Values				
Young's modulus as a function of temperature (GPa)	300K	311K	366K	422K	533K
	121	120.48	117.88	115.24	112.64
Coefficient of thermal expansion (ppm/K)	17.3				
Poisson's ratio	0.3				
Density (kg/m^3)	8900				
Multilinear kinematic hardening model					
Strain	0.001	0.004	0.01	0.02	0.04
Stress (MPa) @ T = 300K	121	186	217	234	248
Stress (MPa) @ T = 533K	110	179	214	231	245

7.3.3. Loading Conditions and Simulation Results

The samples were assembled using the flip-chip bonder, as shown in Figure 6-8. In the assembly process, the eutectic tin-silver (Sn3.5Ag) solder was melt at its melting point 225°C during the reflow, and then cooled from this stress-free temperature to the room temperature so that the silicon substrate was mounted on the organic board. The internal stress was induced during this cooling down process due to the CTE mismatch between the silicon substrate and the organic board. Hence, this assembly process was included into the ANSYS® simulation in order to better capture the strain/stress distribution and then the fatigue life. After the simulation of the reflow process, the thermal cycling load using JEDEC standard (JESD22-A104D) test condition G was applied. The temperature profile used in the thermo-mechanical simulations is presented in Figure 7-14.

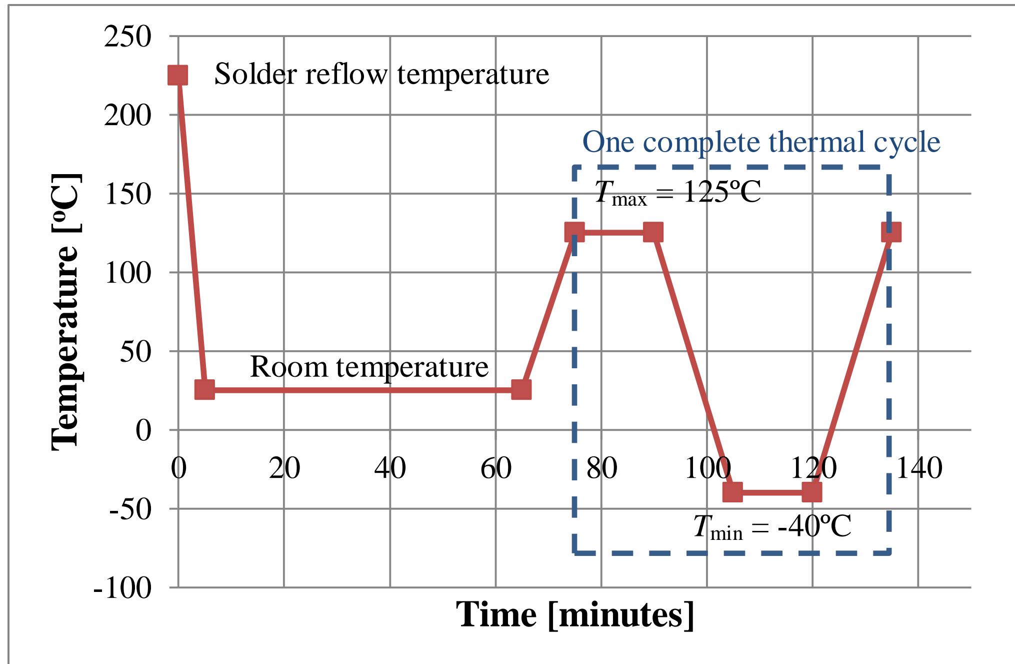


Figure 7-14 Temperature profile for the thermo-mechanical simulations in ANSYS®

The location of the maximum mechanical strain is shown in the left image of Figure 7-15. It is located at the root of one of the arcuate beams where is connected to the copper pad at the outermost interconnect. The reason is that the outermost interconnect has the largest displacement in *X*-direction due to the CTE mismatch between the silicon substrate and the organic board under the thermal cycling load, and the location where the maximum mechanical strain happens is bended the most because of the displacement in *X*-direction.

The right image of Figure 7-15 shows the critical locations the arcuate beams at the outermost compliant interconnect which is believed to fail first. The other compliant interconnects inside also have the same critical locations, because of similar deformation mechanism but with smaller amplitude. It can also be seen that those critical locations in the right image of Figure 7-15 are similar to the failure locations shown in Figure 7-7.

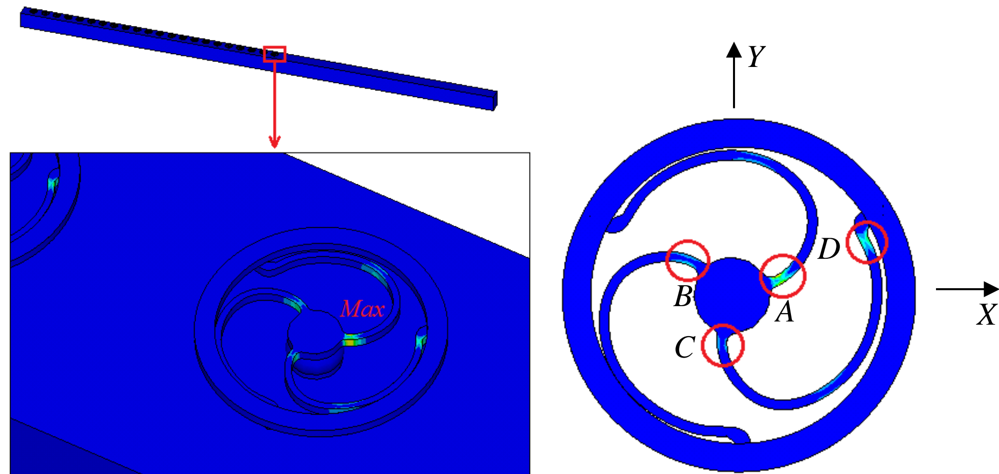


Figure 7-15 Left: location of the maximum mechanical strain; right: critical location of each arcuate beam at the outermost compliant interconnect

For the compliant interconnect with arcuate beam width equal to 10µm and 15µm, the most critical location is A, followed by D, B and C. For the compliant interconnect with arcuate beam width equal to 20µm, the most critical location is A, followed by B, D and C. Since location C and D are in the same arcuate beam and C always has less plastic strain than D, location C is not considered for the fatigue analysis. The 3-Arc-Fan interconnect consists of three parallel arcuate beams, and it is considered as failure only if all three arcuate beams in the same interconnect are broken. Therefore, the fatigue life of the compliant interconnect with arcuate beam width equal to 10µm is decided by its arcuate beam that includes location B who has less plastic strain than the other two arcuate beams that include location A and D. And the fatigue life can be calculated based on the volume-averaged accumulated equivalent plastic strain or plastic strain range after each thermal cycle at location B. For the same reason, the fatigue life of the compliant interconnect with arcuate beam width equal to 15µm is decided by location B as well, while location D should be used to calculate the fatigue life of the compliant interconnect with arcuate beam width equal to 20µm

Table 7-7 Volume-averaged accumulated equivalent plastic strain after each thermal cycle for the outermost interconnect in the strip models with different beam width

Arcuate beam width	Volume-averaged accumulated equivalent plastic strain
10μm (location B)	1.2075×10^{-2}
15μm (location B)	2.6449×10^{-2}
20μm (location D)	3.1341×10^{-2}

Table 7-7 shows the volume-averaged accumulated equivalent plastic strain per thermal cycle for the outermost interconnect in the strip models with different beam width. The compliant interconnect with smaller arcuate beam width value has the least volume-averaged accumulated equivalent plastic strain per cycle, which means that the samples assembled with the compliant interconnect with smaller arcuate beam width are the most reliable. This is also validated by the experimental test data presented in Table 7-1 and Table 7-2.

7.3.4. Thermal Cycling Fatigue Life Prediction

Some works have been done [57] showing that the failure of the solder joints will not precede the failure of the arcuate beams in the compliant interconnect. For this reason, only the failure modes for the arcuate beams will be discussed in this work and the fatigue life of the 3-Arc-Fan compliant interconnect is totally dependent on the fatigue life of the arcuate beams.

Coffin-Manson-type equation for the low-cycle fatigue life prediction, derived based on Engelmaier's work using experimental data for IPC copper foil [58], is applied to determine the fatigue life of the 3-Arc-Fan compliant interconnects and is given as:

$$\Delta\varepsilon_p = N_f^{-0.6} \times D_f^{0.75} \quad (1)$$

$\Delta\varepsilon_p$ = plastic strain range,

N_f = fatigue life, number of cycles to failure

D_f = fatigue ductility, ranges between 0.15 and 0.3 for copper [59]

Using Table 7-7 and equation (1), the fatigue life for the samples with different arcuate beam width can be estimated, as shown in Table 7-8.

Table 7-8 Fatigue life prediction for the samples with different arcuate beam width

Arcuate beam width	D_f = 0.15	D_f = 0.2	D_f = 0.25	D_f = 0.3
10μm	466	668	883	1109
15μm	126	181	239	300
20μm	95	136	180	226

By comparing Table 7-8 against Table 7-2, it can be seen that equation (1) is able to predict the fatigue life of the compliant interconnect with arcuate beam width equal to 10μm and 20μm if D_f is properly selected, but the fatigue life predicted for the compliant interconnect with arcuate beam width equal to 15μm is only half of the fatigue life obtained from the experiments. The primary reasons are 1) equation (1) is based on the experimental data for IPC copper foil whose geometry is different from the 3-Arc-Fan interconnect; 2) different process parameters affect the copper microstructure and the interconnect reliability. Therefore, a modified Coffin-Manson-type equation specifically for the 3-Arc-Fan compliant interconnect should be developed and validated. The modified Coffin-Manson-type equation can be assumed as

$$N_f = \left(\frac{\varepsilon_p^{acc}}{A} \right)^k \tag{2}$$

ε_p^{acc} = volume-averaged accumulated equivalent plastic strain per cycle

N_f = fatigue life, number of cycles to failure

A, k = numerical constants to be determined

7.4. DISCUSSION

7.4.1. Comparison among Different 3-Arc-Fan Compliant Interconnect Designs

The simulations carried out in the previous section are for the assemblies with the silicon substrate thickness equal to 1.35mm. The other simulations for the assemblies

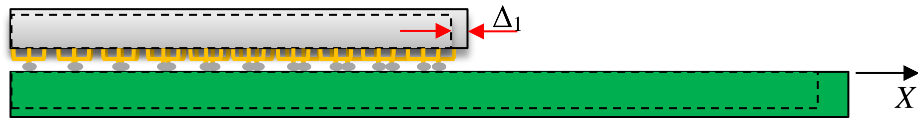
with the silicon substrate thickness equal to 0.675mm were also carried out and the results are compared against each other in Table 7-9.

Table 7-9 Comparison of the volume-averaged accumulated equivalent plastic strain after each thermal cycle between the assemblies with different silicon substrate thickness obtained from the strip models

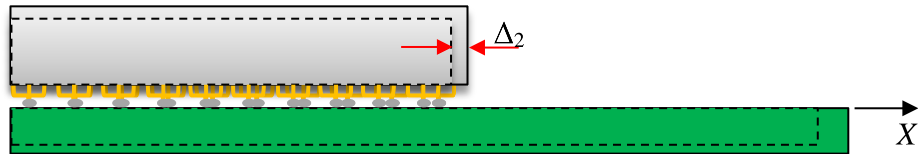
Arcuate beam width	Volume-averaged accumulated equivalent plastic strain		Difference
	0.675mm thickness substrate	1.35mm thickness substrate	
10μm	1.1909×10^{-2}	1.2075×10^{-2}	1.39%
15μm	2.5757×10^{-2}	2.6449×10^{-2}	2.69%
20μm	2.9934×10^{-2}	3.1341×10^{-2}	4.70%

It can be seen that the volume-averaged accumulated equivalent plastic strain is only increased by 1.39%, 2.69% and 4.70% for the assemblies with the arcuate beam width of the interconnects equal to 10μm, 15μm and 20μm, respectively, when the thickness of the silicon substrate is doubled from 0.675mm to 1.35mm.

Among these three arcuate beam width designs, the 10μm design has the least increment while the 20μm design has the most increment. This is because the compliant interconnect with smaller arcuate beam width is more compliant than that with larger arcuate beam width, and it can better mechanically decouple the silicon substrate from the organic board. For instance, if the interconnect is infinitely compliant and the silicon substrate is completely mechanically decoupled from the organic board, the strain in the interconnect is only determined by the displacement in the *X* and *Y* direction, because no warpage will exist in this case. And changing the thickness of either the silicon substrate or the organic board does not change the displacement in the *X* and *Y* direction, as shown in Figure 7-16 that $\Delta_1 = \Delta_2$. Therefore, the strain of the interconnect of infinite compliance values does not change. Based on this, changing the thickness of the silicon results in less change of deformation and thus less change of strain if the interconnect with higher compliance value is used.



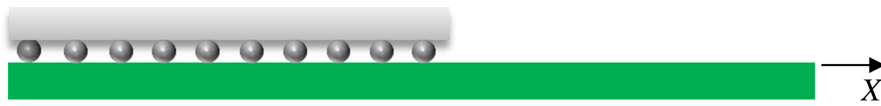
(a) Thin silicon substrate



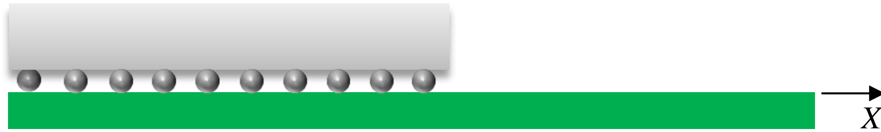
(b) Thick silicon substrate

Figure 7-16 Silicon substrate-infinitely compliant interconnect-organic board assembly under thermal expansion (dashed line: original state; solid line: final state); (a) and (b) have the same loading and boundary conditions, as well as the geometries except that the silicon substrate in (a) is thinner than the silicon substrate in (b)

This is different from the assembly using solder ball interconnects, presented in Figure 7-17, where the thickness values of the substrate and the board are very critical to the strain distribution and the fatigue life of the solder balls. For such an assembly, the solder balls tightly couple the substrate and the board. If a thin silicon substrate is mounted over the organic board, the whole structure is able to warp in order to relieve the strain/stress under the thermal loads. But if a thick silicon substrate or combined die stack is mounted over the organic board, the thick silicon structure becomes extremely rigid and difficult to warp, and the non-compliance of the thick silicon structure aggravates the strains/stresses in the solder balls as little relief in the form of warpage is available to the solder balls in such a scenario.



(a) Thin silicon substrate

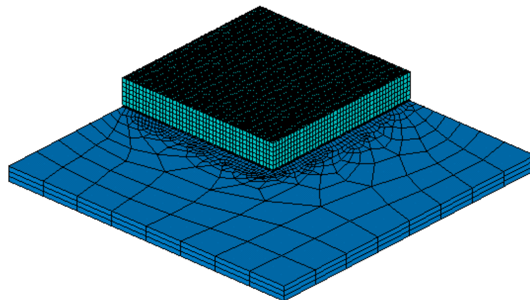


(b) Thick silicon substrate

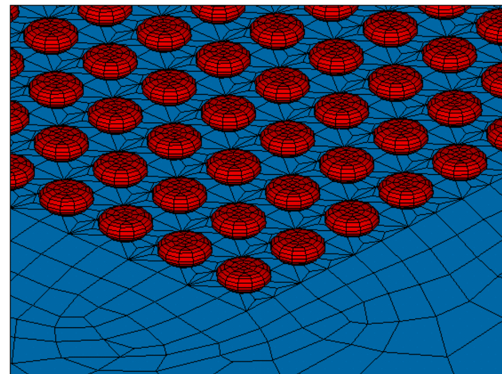
Figure 7-17 Silicon substrate-solder ball interconnect-organic board assembly; (a) and (b) have the same loading and boundary conditions, as well as the geometries except that the silicon substrate in (a) is thinner than the silicon substrate in (b)

7.4.2. Comparison between 3-Arc-Fan Interconnect and Solder Ball Interconnect

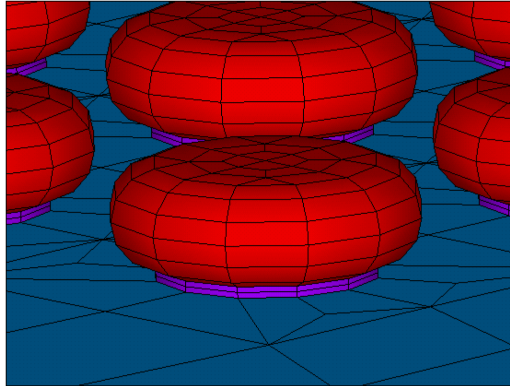
The finite-element model in the previous section was modified and the 3-Arc-Fan compliant interconnects were replaced by the solder ball interconnects with the same stand-off and with maximum solder ball diameter equal to the footprint of the 3-Arc-Fan compliant interconnect. One quarter of the model was built due to the symmetry of the structure and proper boundary conditions were imposed. The mesh size control is shown in Figure 7-18.



(a) Isometric view of the finite-element mesh



(b) Mesh size control for the solder balls



(c) Zoomed-in view of the mesh size control for the solder balls

Figure 7-18 Mesh size control for the finite-element model with solder ball interconnects (green: silicon substrate; blue: FR-4 board; purple: copper; red: solder)

Presented in Figure 7-19 is the contour plot of the nodal solution of the equivalent plastic strain in the solder balls. It can be seen that the solder ball with the maximum equivalent plastic strain is at the outmost corner and on the side that it is connected to the silicon substrate. Because the CTE mismatch between the solder and the silicon is much larger than the CTE mismatch between the solder and the FR-4 board. The volume-averaged equivalent plastic strain was calculated over the volume of a layer of elements with thickness of 25μm [60, 61] as shown in the zoomed-in view of Figure 7-19. This is because there is stress singularity happens at the edge or corner of the solder balls due to the material property jump, which cannot be eliminated by refining the FEM mesh.

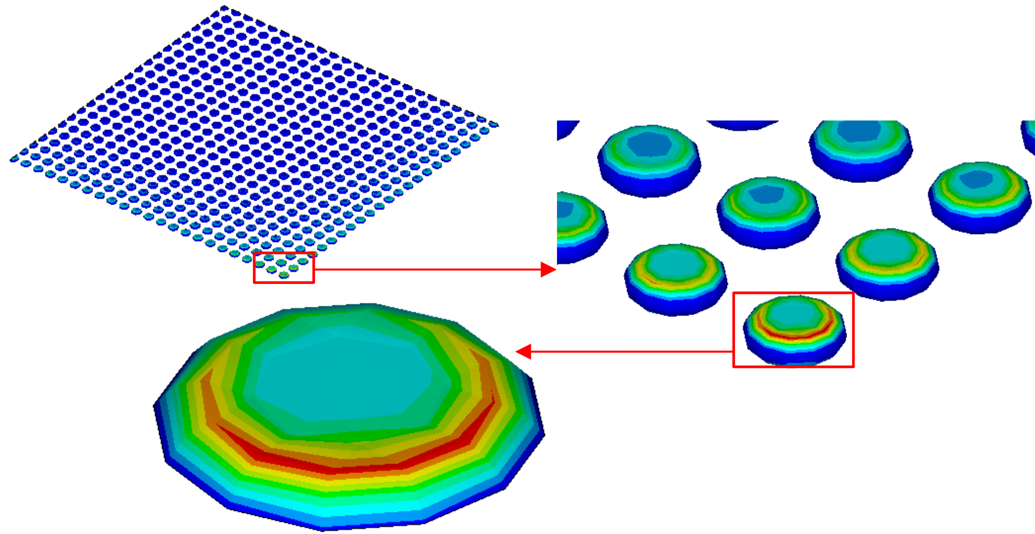


Figure 7-19 Contour plot of the nodal solution of the equivalent plastic strain in the solder balls

The comparison of the volume-averaged accumulated equivalent plastic strain after each thermal cycle between the assemblies with different silicon substrate thickness for the assemblies with solder ball interconnects is shown in Table 7-10. It can be seen that the volume-averaged accumulated equivalent plastic strain is increased by 41.18% when the thickness of the silicon substrate is doubled from 0.675mm to 1.35mm. This is much larger than the compliant interconnects that only have the increment of 1.39%, 2.69% and 4.70% with the arcuate beam width equal to 10μm, 15μm and 20μm, respectively.

Table 7-10 Comparison of the volume-averaged accumulated equivalent plastic strain after each thermal cycle between the assemblies with different silicon substrate thickness for the assemblies with solder ball interconnects

Volume-averaged accumulated equivalent plastic strain		**Difference**
0.675mm thickness substrate	1.35mm thickness substrate	
6.1102×10^{-2}	8.6267×10^{-2}	41.18%

7.5. CONCLUSION

The 3-Arc-Fan compliant interconnects are able to survive for more than 800, 600 and 300 thermal cycles for those designs with arcuate beam width equal to 10μm, 15μm and 20μm, respectively, when subjected to the JEDEC standard (JESD22-A104D) test

condition G with T_{min} = -40°C and T_{max} = 125°C. The 3-Arc-Fan compliant interconnect with smaller arcuate beam width and thus higher compliance is more reliable under the thermal cycling loads.

The volume-averaged accumulated equivalent plastic strains of the compliant interconnect and the solder ball interconnect after each thermal cycle are compared and summarized in Table 7-11. It can be seen that the 3-Arc-Fan compliant interconnect is much superior to the solder ball interconnect when a thick silicon substrate or combined die stack is mounted over the organic board. The thickness of the silicon substrate or the combined die stack has little effect on the strain and hence the fatigue life of the 3-Arc-Fan compliant interconnect, whereas it significantly affects the strain and further the fatigue life of the solder balls. The more compliant the interconnect is the smaller the effect of the substrate thickness will be. The 3-Arc-Fan interconnect with smaller beam width is more reliable than the 3-Arc-Fan interconnect with larger beam width when the assembly is under the thermal cycling loads. The 3-Arc-Fan interconnect with smaller beam width is less sensitive to the substrate thickness than the 3-Arc-Fan interconnect with larger beam width when the assembly is under the thermal cycling loads. Because the interconnect with larger compliant values can better mechanically decouple the substrate from the board. The interconnect with larger compliant values is also less sensitive to organic board thickness due to the same reasons discussed in this section.

Table 7-11 Comparison of the volume-averaged accumulated equivalent plastic strain after each thermal cycle between the assemblies with different silicon substrate thickness using 3-Arc-Fan interconnects with arcuate beam width equal to 10µm, 15µm, 20µm and solder ball interconnects

Different interconnects		**Volume-averaged accumulated equivalent plastic strain**		**Difference**
		0.675mm thickness substrate	1.35mm thickness substrate	
Compliant ↓ **Stiff**	10µm 3-Arc-Fan	1.1909×10^{-2}	1.2075×10^{-2}	1.39%
	15µm 3-Arc-Fan	2.5757×10^{-2}	2.6449×10^{-2}	2.69%
	20µm 3-Arc-Fan	2.9934×10^{-2}	3.1341×10^{-2}	4.70%
	Solder Ball	6.1102×10^{-2}	8.6267×10^{-2}	41.18%

CHAPTER 8 IMPACT ISOLATION EXPERIMENTS AND SIMULATIONS FOR THE SCALED-UP POLYMER INTERCONNECTS

8.1. INTRODUCTION

Compliant interconnects are an emerging technology which can potentially replace solder balls as first-level and second-level interconnects. Their inherent compliance allows them to decouple the die from the substrate or the substrate from the board. Decoupling leads to a reduction in stress accumulation in the die and/or the substrate, increasing the overall life of the die-interconnect-substrate or substrate-interconnect-board assembly. In order to effectively utilize these structures as interconnects, the performance of these structures when subjected to drop loads must be understood. This chapter presents experimental and simulation results of drop testing of scaled prototypes of compliant interconnects. Drop testing involves subjecting components to sudden drop loads and observing the strains and deflection of the components. Various drop testing methods have been utilized over the years. The most widely used methods are based on standards set by Joint Electron Devices Engineering Council (JEDEC) [62].

The testing method discussed in this chapter uses JEDEC standard JESD22-B111, which specifies the generalized drop test technique for board-level components and the simulation uses the Input-G method. The Input-G method uses displacement as input boundary condition for implicit simulations. The displacement is obtained by double integrating the measured acceleration. Luan and Tee [63], Tee et al. [64], Luan and Tee [65] have applied the Input-G method in the study of board level drop test and simulation of chip-scale packages (CSPs). The Input-G method is used to simulate drop testing of microelectronic packages using an implicit finite-element simulation solver. Published

papers by Pan et al. [66] and Chen et al. [67] have also used the Input-G method. Both of these papers have shown the efficacy of this method to perform drop test simulations.

Other publications have used different techniques and approaches to perform drop test simulations and experiments. These include the use of implicit solution for drop testing of IC packages [68, 69], as well as simulation using explicit submodeling techniques [70]. High-speed digital image correlation of experimental drop tests [70, 71] has also been reported. Chen et al. [72] have done the simulation of compliant interconnects under drop impact using explicit ANSYS/LS-DYNA® solver.

Drop testing of microelectronic components necessitates the use of experimental drop test samples. This chapter presents experimental data obtained by drop testing of scaled-up polymer prototypes of compliant interconnects, fabricated using 3D printing. The use of stereolithography prototype models for model validation has been explored by Tribe et al. [73]. Mahn and Bayly [74] have discussed the use of stereolithography models to determine natural frequencies of components. These findings allow the use of 3D print prototypes which have very similar properties as stereolithography prototypes for drop test validation. The primary purpose was to use a fabrication technique that would give experimental samples within a much shorter frame of time, with behavior similar to samples fabricated using cleanroom fabrication processes. Insight into the response behavior of the actual interconnects could be gained by first studying scaled-up prototypes. Therefore, 3D printing was used for fabricating compliant interconnect assemblies for the current work. The data obtained from experimental drop testing was used to validate finite-element simulation results obtained from simulations conducted for the same geometry using the ANSYS® Implicit solver. Thus, the important elements in this chapter are to conduct drop-test experiments with compliant interconnects, model the drop testing of compliant interconnects, and to show that the compliant interconnects can isolate the substrate from the board during impact loading.

8.2. EXPERIMENTAL DROP TESTING

8.2.1. Experimental Setup

One of the objectives of this work was to develop an alternative technique which could effectively and economically help ascertain drop test reliability of microelectronic packages. It was decided that the original compliant interconnect designs would be scaled for ease of fabrication and testability. 3D printing-based fabrication was selected for its versatility and ability to generate complex geometries in relatively short spans of time. The compliant interconnect design used for this experiment was based on the multi-path 3-Arc-Fan compliant interconnect design specified in the paper by Lee et al. [40].

It should be pointed out that one of the goals of this chapter is to demonstrate that an array of 3-Arc-Fan compliant interconnects can be used as an effective vibration isolator between a substrate and a board in an assembly. The polymer material used in this work is FullCure®720. The glass transition temperature of FullCure®720 is 47.8 ºC, which is about 25 ºC higher than the room temperature. As discussed later in this chapter, the impact time for drop tests was only about 20ms. Under such short impact time as well as at a temperature below the glass transition temperature, it is reasonable to neglect viscoelastic effects.

Copper compliant interconnects can be fabricated on silicon wafers at different pitches, 100, 200, or 400μm, through sequential cleanroom fabrication processes and assembled on organic or other boards through solder reflow. Such samples can then be subjected to drop testing. However, the fabrication, assembly, and data extraction from such samples are time-consuming. Work is ongoing in the fabrication and assembly of such micro-scale compliant interconnects, and once such samples are ready, they will be subjected to drop testing. The results from such a study will be reported in a future publication.

Objet Eden 250™ system was used for the fabrication of the polymer compliant interconnect structures. The 16 micron high resolution of this machine ensures smooth surfaces and fine details. To ensure all features of the compliant interconnects were created with accurate dimensions, the original 3-Arc-Fan compliant interconnect design was scaled up 75 times, using the interconnect pitch as the scaling metric. Shown in Figure 8-1 is the design geometry for the 3-Arc-Fan compliant interconnect and a rapid prototyped sample scaled up 75 times from its original size. FullCure®720 was selected as the 3D printing material, with its Young's modulus equal to 2.870GPa.

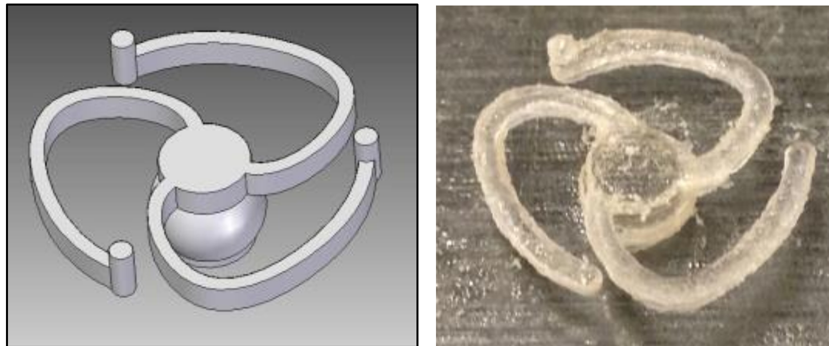


Figure 8-1 Image on left shows 3D model of 3-Arc-Fan compliant interconnect; image on right shows the compliant interconnect printed by Objet Eden 250™ system

Using a 3D printing procedure, a 3×3 area-array of polymer compliant interconnects was fabricated, sandwiched between a (45mm × 45mm × 1mm) polymer substrate and a (110mm × 64mm × 1mm) polymer board, imparting completely homogenous properties to the entire sample (Figure 8-2). The board was designed with built-in holes to allow for mounting of the sample on the drop table surface.

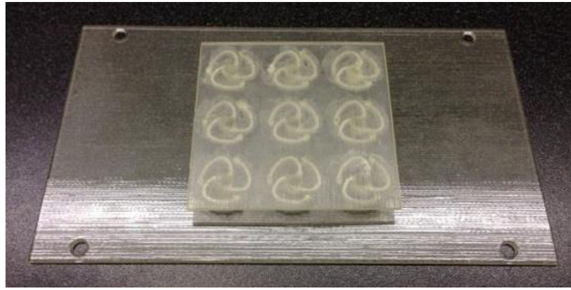


Figure 8-2 3-Arc-Fan compliant interconnect drop test sample; shows a 3x3 area-array of 3-Arc-Fan compliant interconnects between polymer substrate and polymer board

An Instron Dynatup® 8250 drop weight impact tester was used to conduct the drop tests. The Instron machine was suitably modified to accommodate the drop testing. A custom drop test fixture which mimics a drop table was designed and fabricated using impact-resistant steel. This fixture was designed to house the drop test sample inside it and would serve as the drop table needed for mounting the test sample. The fixture was bolted onto the crosshead of the Instron machine, as shown in Figure 8-3, and could be freely raised or lowered using the crosshead movement controls of the Instron drop weight tester.

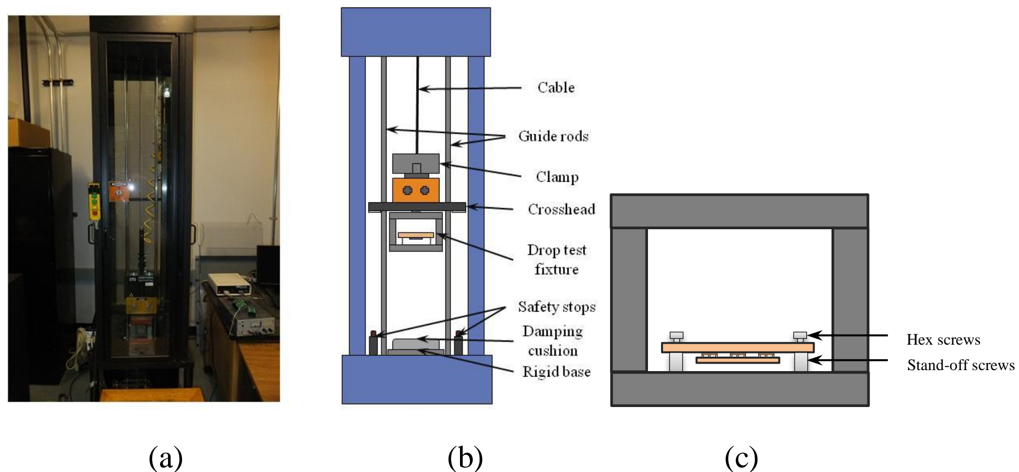


Figure 8-3 Custom drop test fixture bolted to crosshead of Instron Dynatup® 8250 drop weight impact tester

As shown in Figure 8-3(c), stand-off screws were used to raise the board above the drop test surface inside the fixture, and hex screws were used to bolt the board onto

the stand-off screws. The stand-off screws allowed the board to flex during the drop test, which is known to be the primary reason for interconnect failure during drop [75].

Strain was used as a metric for determining the effect of the drop test on the mounted sample. A linear 1-axis strain gauge (Gauge Factor 2.09) was attached directly on top of the free surface of the board. A bi-axial tee-rosette strain gauge (Gauge Factor 2.1) was attached on the polymer substrate, directly opposite the linear 1-axis strain gauge at the center of the substrate. In addition, a unidirectional piezoelectric accelerometer was mounted next to one of the holes, to measure the input acceleration as well as the impact pulse generated during the actual drop event.

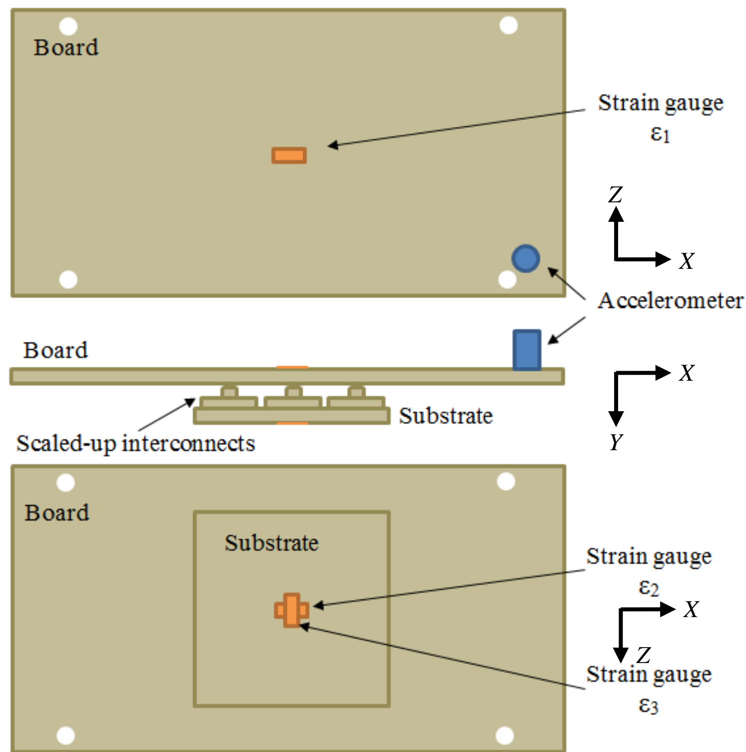


Figure 8-4 Accelerometer and strain gauge positions and orientations: (a) accelerometer and linear 1-axis strain gauge mounted on board (top view); (b) side view of mounted accelerometer and strain gauges; (c) bi-axial Tee-rosette strain gauge mounted on substrate (bottom view)

The information from the accelerometer was used to generate input boundary conditions necessary to conduct finite-element simulations using the Input-G method. The gauge and accelerometer positions and orientations are shown in Figure 8-4.

In Figure 8-4, ε_1 refers to the linear 1-axis strain gauge attached on the board parallel to the planar *X* direction, along the length of the board. ε_2 and ε_3 together refer to the bi-axial tee-rosette strain gauge attached at the center of the substrate. ε_2 is parallel to the planar *X* direction, while ε_3 is parallel to the planar *Z* direction. The accelerometer is mounted next to one of the holes. This layout of strain gauges and accelerometers was used for all experiments.

8.2.2. Input and Post-Test Calculation

An excitation voltage of 5V was used to power the strain gauges while an external power source with built-in signal conditioner was used to charge and power the accelerometer. The strain gauge output and accelerometer readings were fed into a National Instruments® Analog-to-Digital Convertor (ADC) voltage module. With a sampling rate of 100,000 readings/s and four simultaneous channels, the output from all the strain gauges and the accelerometer was obtained in real time. The voltage module was interfaced with a data-acquisition software, LabVIEW®, which allowed collection of output voltage data. This voltage data was subsequently converted to strain using an appropriate strain-gauge relation for the quarter-bridge type.

8.2.3. Drop Test Results

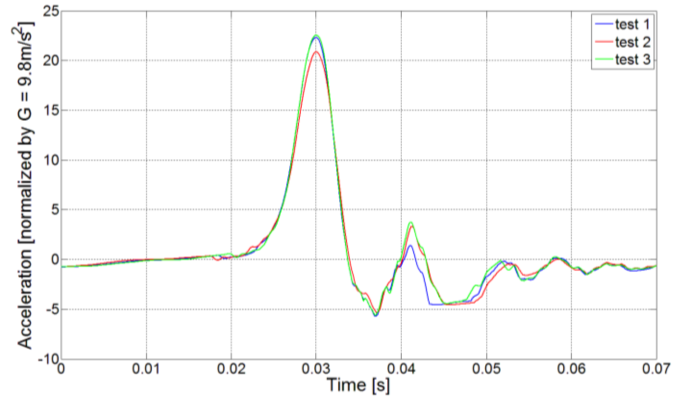
Drop tests were conducted from different drop heights, ranging from 50mm to 200mm in steps of 50mm. The drop height of the fixture was controlled and the impact acceleration was recorded. Additionally, a cushioning material was used to damp the impact of the drop test fixture with the underlying rigid surface.

Figure 8-5 shows the acceleration plots obtained from the accelerometer during the actual drop event for drop heights 50mm 100mm, 150mm and 200mm. These were

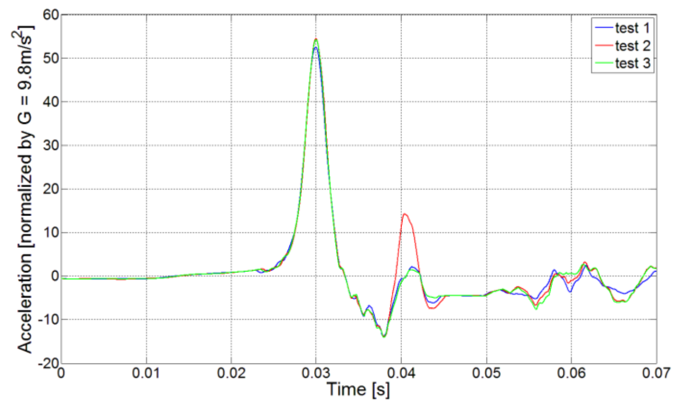
obtained by plotting the acceleration values measured by the mounted unidirectional piezoelectric accelerometer versus time and indicate the change in measured acceleration experienced by the test sample during the drop event. Shown in Table 8-1 are the different drop heights and impact accelerations recorded during the drop testing of the 3-Arc-Fan compliant interconnect samples. It can clearly be seen that the impact acceleration increases and the impact time decreases with increase in the drop height. Based on the acceleration plots, the peak acceleration was found to increase almost linearly from a low value of 21.9G (1G = standard acceleration due to gravity) for a drop height of 50mm to 89.7G for a drop height of 200mm. The increasing behavior of the acceleration recorded was attributed to the fact that the acceleration experienced was a function of the drop height (h), the velocity before impact (v) as well as the material used to obtain the required damping and output pulse shaping. These variables when put together give rise to increasing peak acceleration.

Table 8-1 Peak acceleration and impact times for 3-Arc-Fan compliant interconnect drop tests

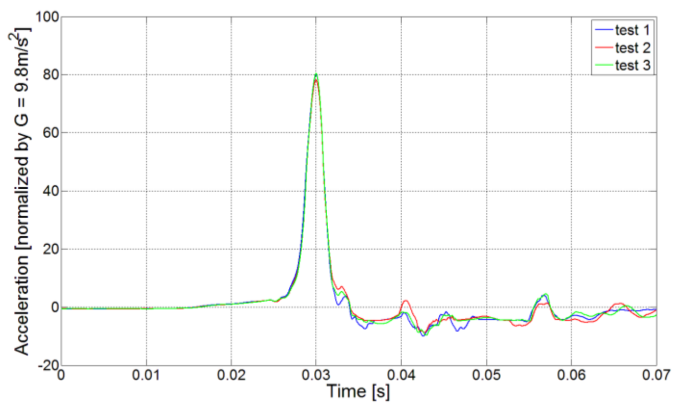
Drop Height (mm)	Measured Peak Acceleration (G)	Measured Impact Times (ms)
	Mean (Range)	Mean (Range)
50	21.9 (20.9 – 22.6)	20.8 (19.4 – 22.4)
100	53.7 (52.4 – 54.5)	19.6 (19.4 – 19.9)
150	79.8 (78.3 – 80.5)	17.9 (18.1 – 17.6)
200	89.7 (87.8 – 90.1)	16.3 (15.5 – 17.2)



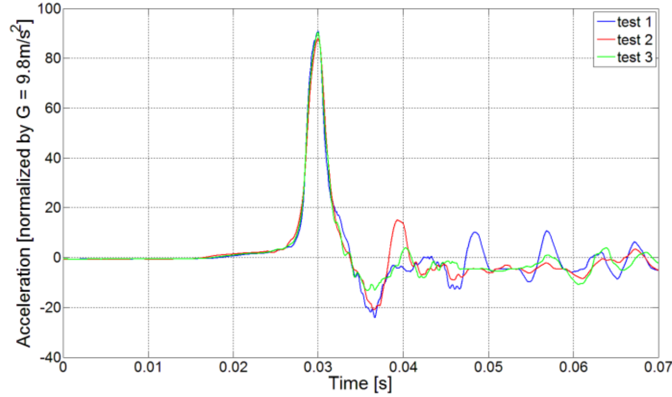
(a) 50mm drop height acceleration data



(b) 100mm drop height acceleration data



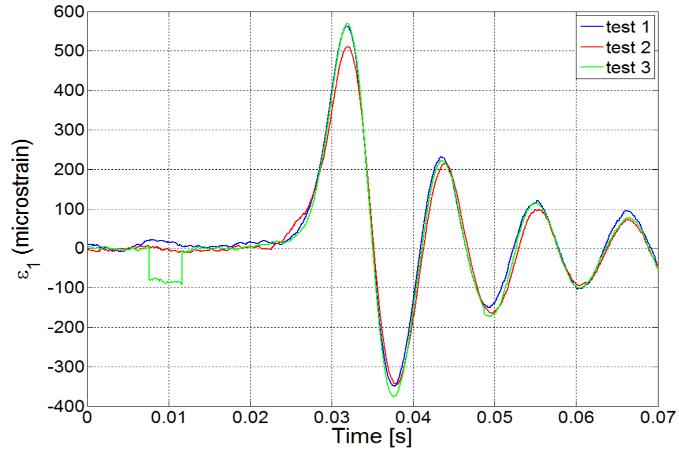
(c) 150mm drop height acceleration data



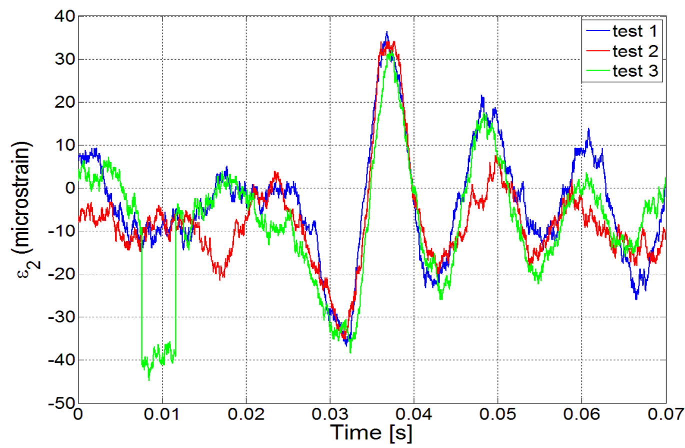
(d) 200mm drop height acceleration data

Figure 8-5 Measured acceleration for 3-Arc-Fan compliant interconnect assembly for drop heights equal to 50mm, 100mm, 150mm and 200mm

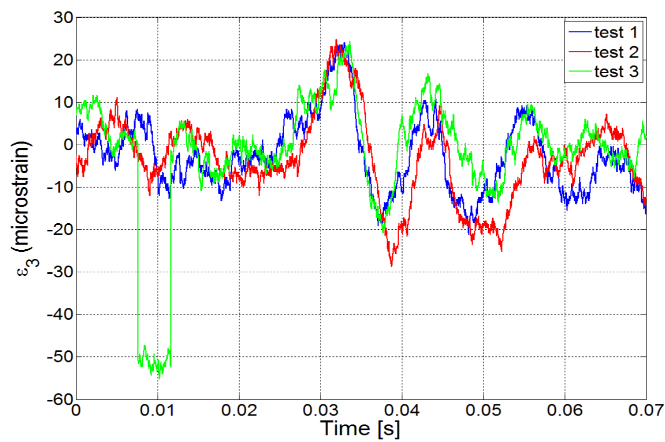
Figure 8-6 and Figure 8-7 show the strain data plots calculated from the strain output data recorded by the strain gauges for 3-Arc-Fan compliant interconnect with drop heights equal to 50mm and 150mm, which also reveal that ε_1 and ε_3 are in phase while ε_2 has 180º phase difference. There are two reasons for these observations. As shown in Figure 8-4, the sensor (ε_1) and the accelerometer were mounted on the board side that faces the ceiling, while the sensors (ε_2 and ε_3) were mounted on the substrate side that faces the floor. Thus, sensors ε_1 and ε_2 are on two opposite sides of the test sample. This would mean that during the drop test, when one side is under tension, the other side must be under compression. Therefore, ε_1 and ε_2 are out of phase during the test. On the other hand, both ε_2 and ε_3 measure the normal strain on the substrate but in two mutually perpendicular directions. The whole structure's longitudinal dimension is much greater than the whole structure's transverse dimension, and thus, upon impact and subsequent vibrations, the structure's deformation in the longitudinal direction is more dominant than its deformation in the transverse direction. Therefore, ε_3 strain is mainly determined by the Poisson's effect which results in the opposite sign of ε_2.



(a) ε_1

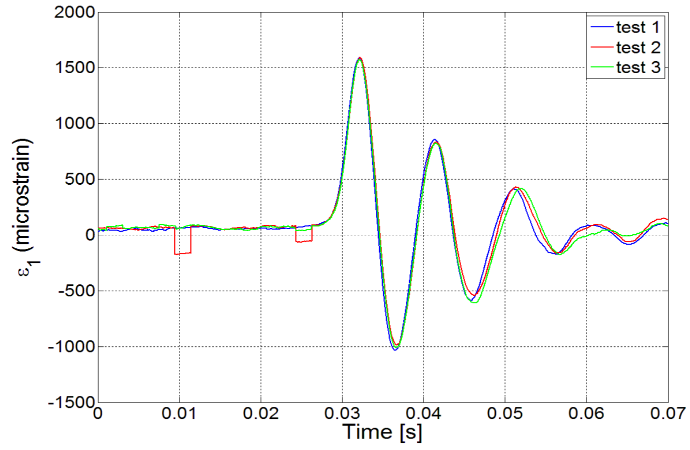


(b) ε_2

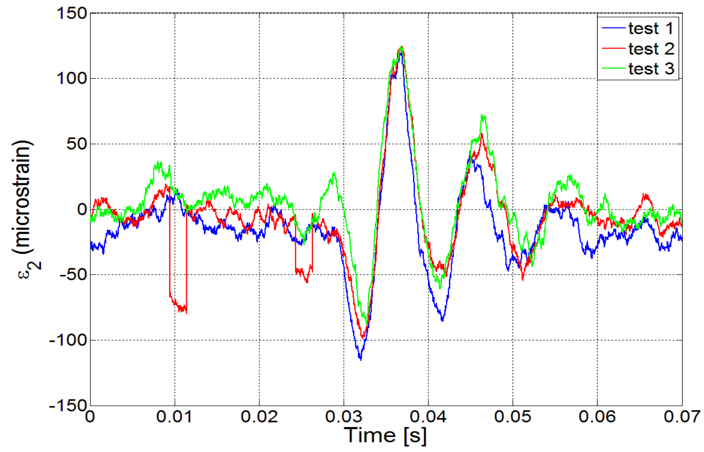


(c) ε_3

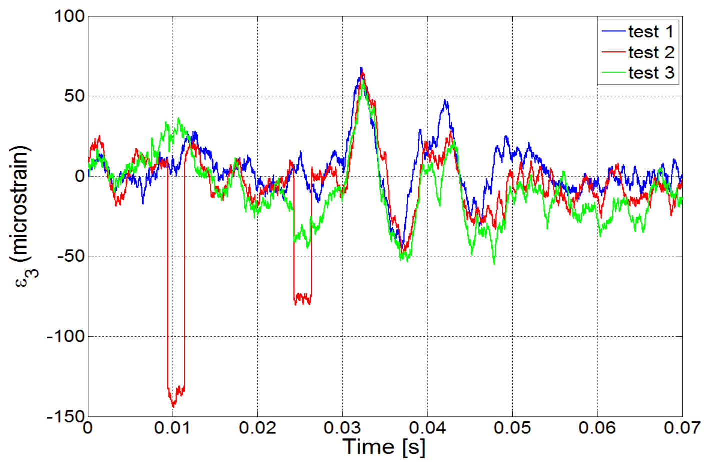
Figure 8-6 Experimental strain data for 3-Arc-Fan compliant interconnect drop tests with a drop height equal to 50mm



(a) ε_1



(b) ε_2



(c) ε_3

Figure 8-7 Experimental strain data for 3-Arc-Fan compliant interconnect drop tests with a drop height equal to 150mm

Table 8-2 shows the microstrain values for different drop heights for all the strain gauges mounted on the drop test samples. These values are the average peak microstrain values obtained from the three test cases for a given drop height.

Table 8-2 Peak microstrain values for 3-Arc-Fan compliant interconnect for different drop heights

Drop Height (mm)	ε_1	ε_2	ε_3
	Mean (Range)	Mean (Range)	Mean (Range)
50	548 (512 – 570)	34 (32 – 36)	24 (24 – 25)
100	1192 (1164 – 1222)	91 (82 – 99)	49 (47 – 52)
150	1587 (1574 – 1596)	123 (121 – 125)	64 (60 – 68)
200	1768 (1705 – 1835)	150 (140 – 158)	73 (73 – 74)

Based on the values given in Table 8-2, the strains in the board and substrate can be seen to monotonically increase as the drop height increases from 50mm to 200mm. The strain in the substrate along the transverse direction, recorded by ε_3 is nearly half that of ε_2. It is seen that the board strain increases with the drop height. The substrate strains (ε_2 and ε_3) also increase with the drop height, and are much smaller in magnitude compared to ε_1. This reduction in substrate strains can be attributed to the effect of the 3-Arc-Fan compliant interconnects, which are able to absorb and thus damp most of the strain from being transferred to the substrate from the board. The mean ratio of the board-to-substrate strain ratio along the longitudinal axis is calculated to be 13:1, and thus, the 3-Arc-Fan compliant interconnects are able to isolate the impact and reduce the strain in the substrate by a factor of approximately 13 compared to the strain in the board.

8.3. DROP TEST SIMULATION

For the purpose of conducting drop test simulations, the Input-G method was selected, which makes use of an implicit method to simulate a drop test. In this technique, the impact acceleration recorded from experimental drop tests was converted to

displacement boundary conditions. The calculated displacement was then applied at the supports, taking into account the impulse time of the drop [63].

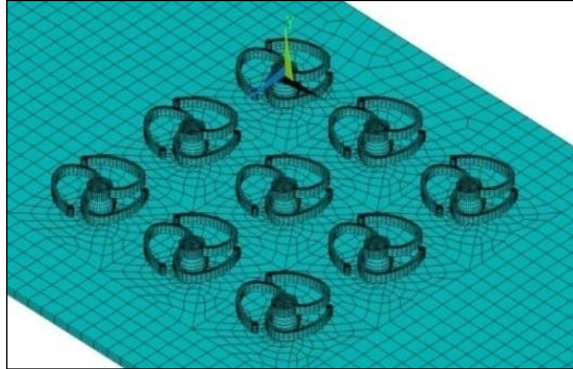


Figure 8-8 Close-up of 3-Arc-Fan compliant interconnect array model used in simulation

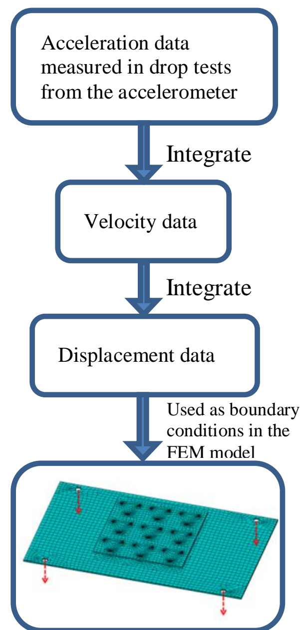


Figure 8-9 Flowchart describing the Input-G method and locations where the prescribed displacement boundary conditions are applied

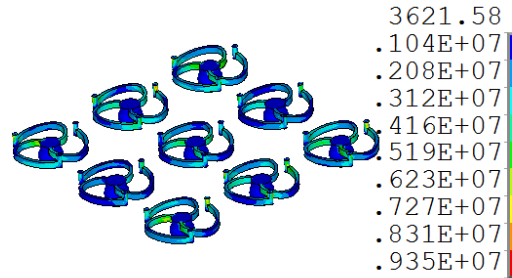


Figure 8-10 Contour plot of the nodal von Mises stress (Pa) in the interconnects for a drop height of 200mm during maximum deformation

The finite-element simulations were carried out using the ANSYS® Implicit solver. A 3×3 array of scaled up compliant interconnects was created with substrate and assembly as shown in Figure 8-8, which shows a close-up mesh of the exposed 3-Arc-Fan compliant interconnect array. Shown in Figure 8-9 is the flowchart describing the Input-G method and how the displacement data integrated from the acceleration data are applied as boundary conditions. The model geometry was designed to closely mimic the drop test samples used for experimental testing. The model used for simulation was created using SOLID185 elements. A total of 60906 elements were used to create the model. The polymer material used to fabricate the experimental drop test samples was modeled in the simulation as a linear elastic material with a modulus of elasticity of 2.870GPa, a yield strength of 60MPa [76], a Poisson's ratio of 0.3 and a density 1180 Kg/m3. It can be seen in Figure 8-10 that the maximum von Mises stress in the interconnects for a drop height of 200mm was 9.35MPa which is smaller than the yield strength, and thus remains in the elastic range throughout the drop response.

Luan and Tee [63] proposed two simplified pulse shapes to capture the impact pulse, rectangle acceleration pulse and half-sine acceleration pulse. The rectangle acceleration pulse is good for constant acceleration cases, and is not suitable to approximate our cases. Thus, only the half-sine acceleration pulse is discussed. Figure 8-11 compares the actual acceleration curve (in red) with two different simplified half-sine acceleration pulse curves (in blue) for one of the 50mm drop events. The solid blue

curve uses the true impact time, the time span when the acceleration crosses zero. However, because of the effect of the cushioning material, the acceleration increases very slowly at the beginning of the impact, and thus applying the true the impact time to the half-sine acceleration pulse is inappropriate. A modified impact time, which starts from the instant when the acceleration curve gradient becomes very large, can also be used to create the half-sine pulse. Even though the new half-sine pulse shows a significant improvement in approximating the acceleration, the velocity (Figure 8-12(a)) and the displacement (Figure 8-12(b)) are overestimated by at least 20% and 35% after the integration, respectively. This is because the measured acceleration curve is concave in the initial stage, while the half-sine pulse is convex, as shown in Figure 8-11.

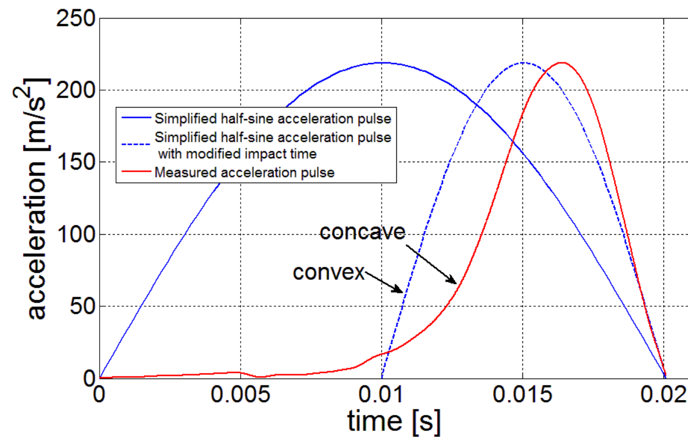
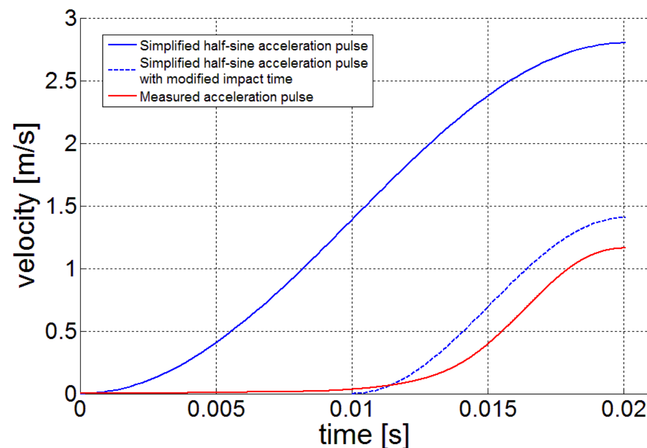
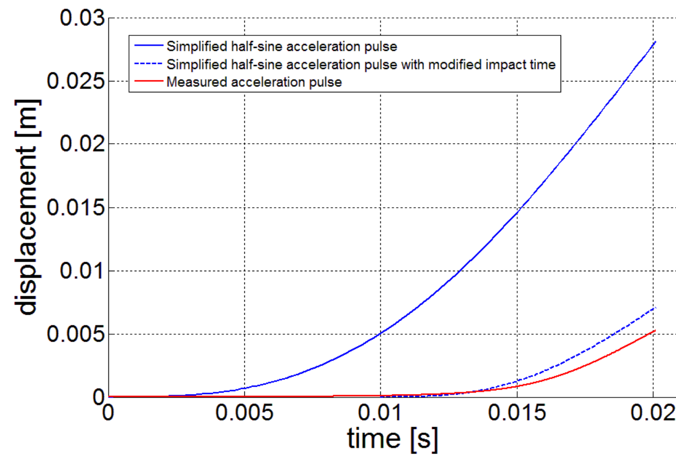


Figure 8-11 Measured acceleration curve and two half-sine acceleration pulse curves with different impact time for one of the 50mm drop events.



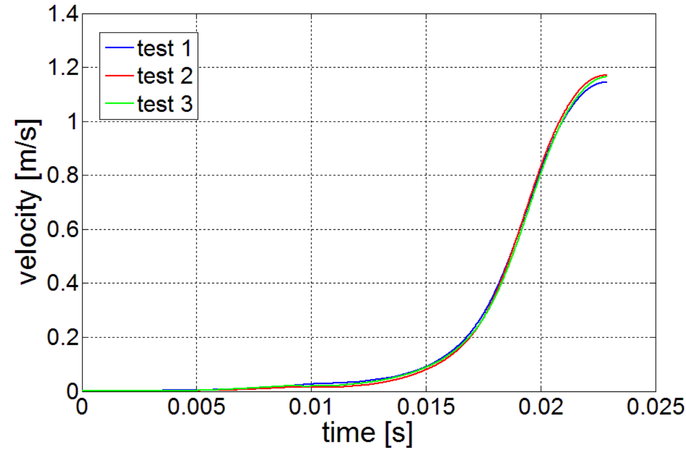
(a) Velocity curves



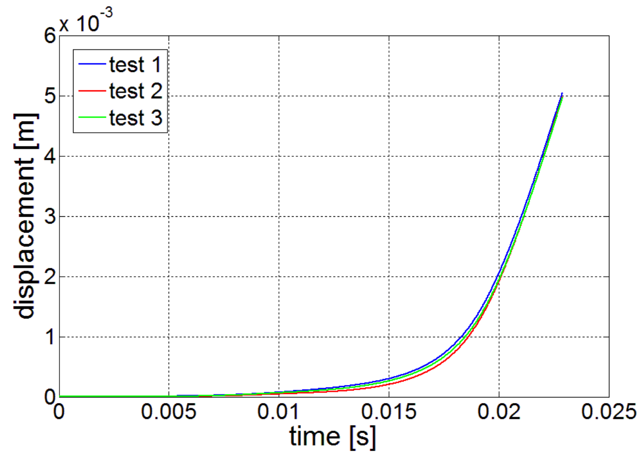
(b) Displacement curves

Figure 8-12 Velocity and displacement curves obtained from the measured acceleration pulse and two half-sine acceleration pulse curves with different impact time for one of the 50mm drop events.

Based on the above discussion, it is clear that both approximations of acceleration are not adequate to capture displacement, and thus, direct integration based on the measured acceleration was used to obtain the displacement boundary conditions in this work. Additionally, it should be pointed out that 1) the half-sine acceleration pulse is very sensitive to the chosen impact time; 2) although the modified half-sine pulse shows good approximation of the acceleration, it still overestimates the velocity and displacement; 3) the determination of impact time for the half-sine pulse based on the acceleration curve gradient is subjective. Figure 8-13 shows the velocity and displacement boundary condition curves, obtained from integrating the measured acceleration data, for three 50mm drop tests.



(a) Velocity curves for 50mm height drop test



(b) Displacement curves for 50mm height drop test

Figure 8-13 Velocity and displacement boundary condition curves for three 50mm drop test events

8.4. COMPARISON BETWEEN SIMULATION AND EXPERIMENT

Table 8-3 compares the microstrain values recorded from both experiment and simulation. Both experiments and simulation showed significantly lower strains in the substrate than that observed in the board. It can be seen that the experiments and simulation of ε_2 and ε_3 for the 50mm drop height have relatively bigger discrepancy, mainly because that the measured output voltages for ε_2 and ε_3 are much smaller due to the lower drop height which leads to lower signal to noise. But all other results show very

good match between the experiments and simulation with the average discrepancy less than 10%.

Table 8-3 Comparison between experimental and simulation microstrain values for 3-Arc-Fan compliant interconnect drop tests for different heights

Drop Height (mm)		50	100	150	200
ε_1	Experimental	548	1192	1587	1768
	Simulation	567	1193	1595	1989
ε_2	Experimental	34	91	123	150
	Simulation	62	107	115	178
ε_3	Experimental	24	49	64	73
	Simulation	31	47	58	70

On comparing the substrate strains, it was observed that the substrate strains (ε_2 and ε_3) were reported to be significantly lower than board strain (ε_1) in both experiments and simulations. A close relation was observed between experimental and simulation microstrain values. The board-to-substrate strain ratio (ε_1/ ε_2) averages about 13:1 for this scaled-up 3×3 area-array of 3-Arc-Fan compliant interconnects between a polymer substrate and a polymer board. The actual ratio in an assembly with the micro-scale compliant interconnect could be different.

To ensure that the strain transfer is influenced by the compliance of the interconnects, and not by damping or by other factors, additional simulations were conducted by changing the modulus of the interconnect material, but keeping the dimensions and the geometry the same. Accordingly, several simulations were done by changing the Young's modulus from 1.435GPa to 28.70GPa. As seen in Table 8-4, whenever the modulus is increased, the compliance of the interconnect decreases, and thus, the board-to-substrate strain ratio decreases, and vice versa.

Table 8-4 Effect of compliant interconnect Young's modulus on strain transfer ratio from the board to the substrate (for 50mm drop tests)

Young's modulus (GPa)	ε_1	ε_2	ε_3	$\varepsilon_1/\varepsilon_2$
1.435	662	34	11	19.5
2.870	567	62	31	9.1
5.740	554	107	52	5.2
28.70	387	224	127	1.7

These results give evidence of the strong decoupling effect of the compliant interconnects, while proving that the compliant nature of the interconnects reduces strain transfer from the board to the substrate.

8.5. CONCLUSION

Experimental drop testing of compliant interconnect prototypes was carried out in order to understand the reliability of these structures and to validate finite-element simulation data. In experiments, it was observed that the strain in the board was found to increase with increase in drop heights. A similar response was observed in the substrate strains. The board-to-substrate strain ratio was found to be about 13: 1 for this scaled-up 3×3 area-array of 3-Arc-Fan compliant interconnects between a polymer substrate and a polymer board, displaying the strain isolating nature of the 3-Arc-Fan compliant interconnects.

Simulations were conducted for the 3-Arc-Fan compliant interconnects using the Input-G method, and the direct integral method based on the measured acceleration curve was used to obtain the displacement boundary curve, instead of using a simplified half-sine pulse or a rectangle pulse. The results from simulation were validated using the conducted experimental drop tests and were found to be within reasonable error. The simulated results agree very well with the experimental for the strains observed in both the substrate and board. The reported results show that the 3-Arc-Fan compliant

interconnects could be used to obtain reduced strain transfer from the board to the substrate.

An actual silicon substrate with copper compliant interconnects assembled on an organic board and will be presented in the next chapter.

CHAPTER 9 IMPACT ISOLATION THROUGH THE USE OF 3-ARC FAN INTERCONNECTS

9.1. INTRODUCTION

As reported in the previous chapter that the board-to-substrate strain ratio was found to be about 13: 1 for the scaled-up 3×3 area-array of three-arc compliant interconnects between a polymer substrate and a polymer board, displaying the strain isolating nature of the three-arc compliant interconnects. This chapter presents experimental and simulation results of drop testing of actual silicon substrates with copper compliant interconnects assembled on organic boards, and shows that the compliant interconnects, when scaled down in size and fabricated through copper electroplating process, are able to isolate the strain transfer from an organic board to a silicon substrate.

9.2. EXPERIMENTAL DROP TESTING

9.2.1. Experimental Setup

Copper compliant interconnects were fabricated on silicon wafers at a pitch of 400µm, through sequential cleanroom fabrication processes. The silicon wafer was diced into 18mm × 18mm × 0.675mm substrates which were then assembled on organic FR-4boards (132mm × 77mm × 1mm) through solder reflow, as discussed in Chapter 9. The overall design was based on the JEDEC standard for the board-level drop test reliability. Such samples can then be subjected to drop testing.

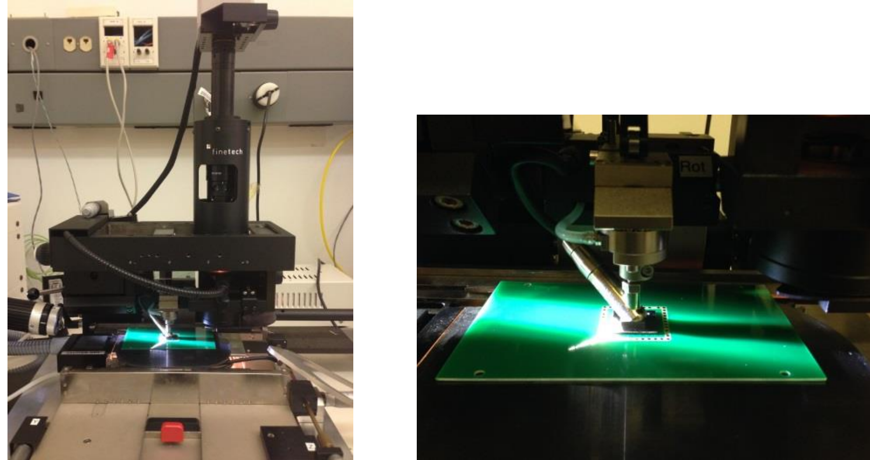


Figure 9-1 A silicon (18mm × 18mm × 0.625mm) substrate assembled on an organic board (132mm × 77mm × 1mm) through solder reflow using Finetech flip-chip bonder

The Instron Dynatup® 8250 drop weight impact tester was used to conduct the drop tests. A new drop test fixture was designed and fabricated according to the JEDEC standard. The fixture was bolted onto the crosshead of the Instron machine, as shown in Figure 9-2. The schematic plots of the drop weight impact tester, custom drop test fixture and drop test sample are shown in Figure 9-3.

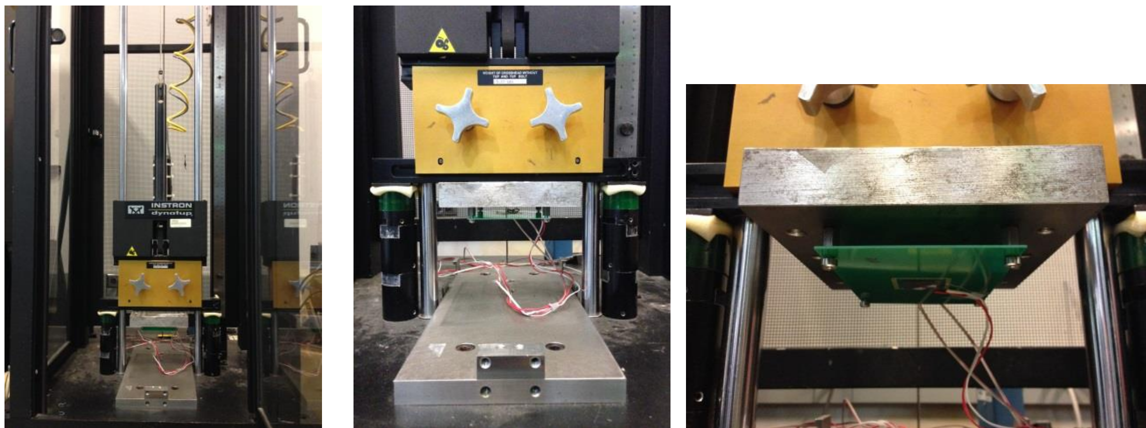


Figure 9-2 Instron Dynatup® 8250 drop weight impact tester, custom drop test fixture and drop test sample with strain gauges attached

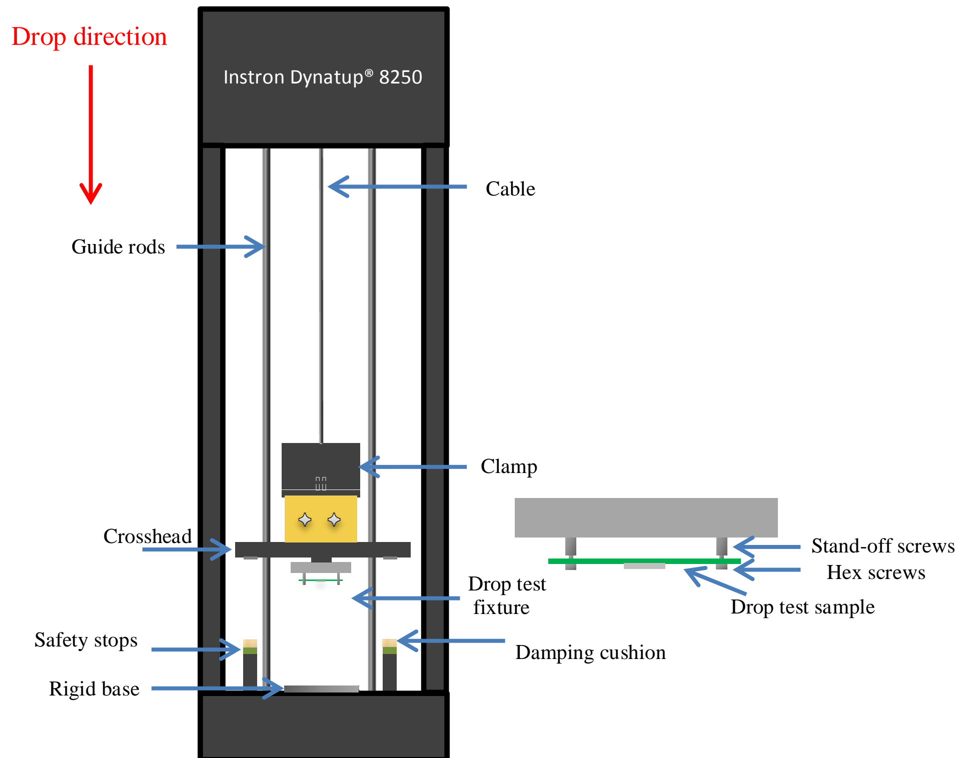
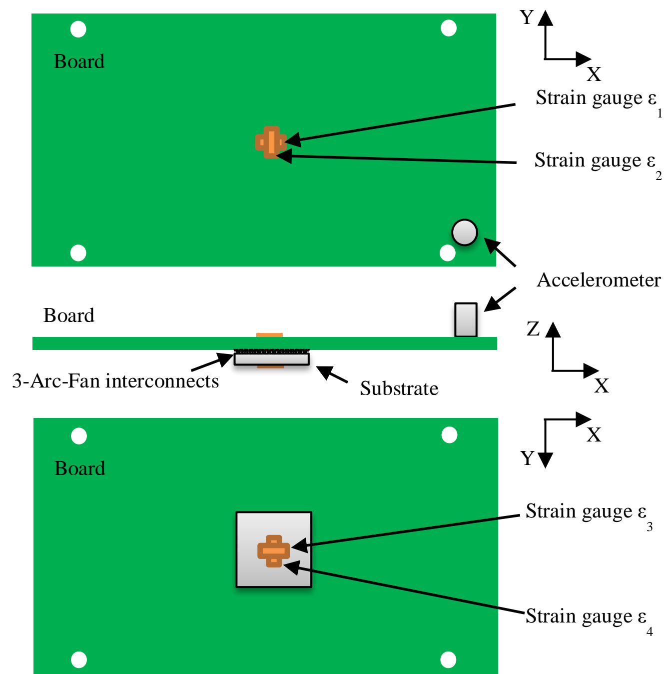


Figure 9-3 Schematic plots of the Instron Dynatup® 8250 drop weight impact tester, custom drop test fixture and drop test sample

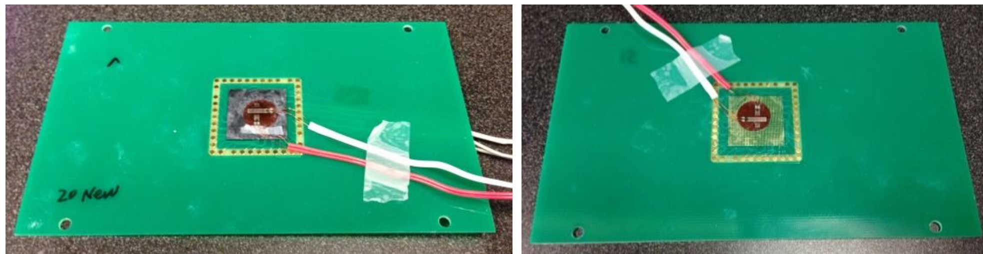
A bi-axial tee-rosette strain gauge (Gauge Factor 2.1) was attached on top of the free surface of the organic board. The other bi-axial tee-rosette strain gauge was attached on the silicon substrate. In addition, a unidirectional piezoelectric accelerometer was mounted next to one of the holes, to measure the input acceleration as well as the impact pulse generated during the actual drop event.

As described in the previous chapter, the information from the accelerometer was used to generate input boundary conditions necessary to conduct finite-element simulations using the Input-G method. In Figure 9-4, ε_1 and ε_2 together refer to the bi-axial tee-rosette strain gauge attached at the center of the board. ε_1 measures the normal strain in X direction, while ε_2 measures the normal strain in Y direction. ε_3 and ε_4 together refer to the bi-axial tee-rosette strain gauge attached at the center of the silicon substrate. ε_3 measures the normal strain in X direction, while ε_4 measures the normal strain in Y

direction. The accelerometer is mounted next to one of the holes. Shown in Figure 9-5 is the apparatus of the experimental setup.



(a)



(b) (c)

Figure 9-4 Drop test sample (an 18mm×18mm silicon substrate bonded on a 135mm × 72mm board by 2000 3-Arc-Fan interconnects); accelerometer and strain gauge positions and orientations.

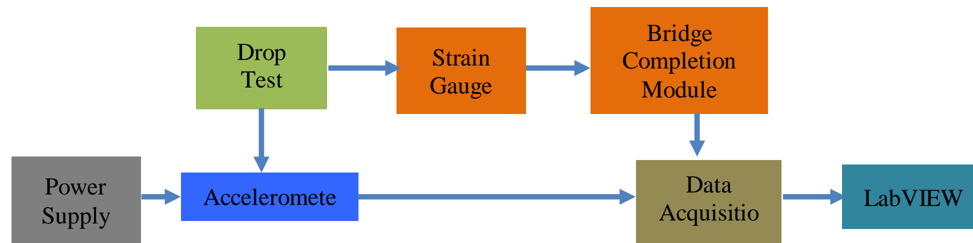


Figure 9-5 Apparatus of the experimental setup

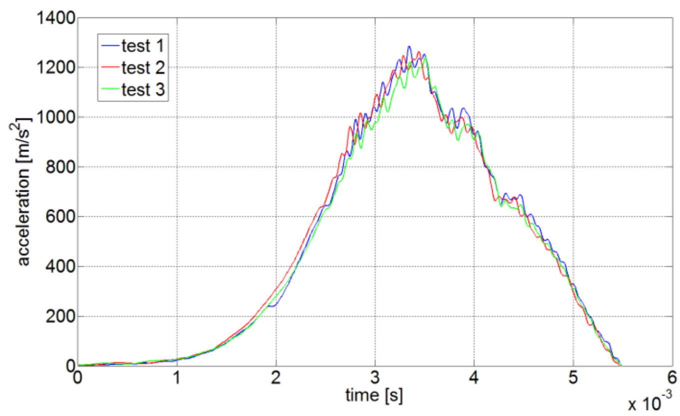
9.2.2. Input and Post-Test Calculation

The maximum allowable excitation voltage of 8V was used to power the strain gauges. This relatively higher excitation voltage was selected in order to obtain higher magnitude of signals and thus increase the signal to noise ratio. The four strain gauge outputs and the accelerometer readings were collected independently using National Instruments® Analog-to-Digital Convertor (ADC) voltage module with four simultaneous channels. Multiple drop tests were conducted at the same height for the same sample to ensure that the acceleration data and strain data collected are consistent at the specific drop height. As it was done in the drop tests for the scaled-up polymer samples, the voltage module was interfaced with LabVIEW®, which allowed collection of output voltage data. The voltage data was then converted to strain and acceleration values using appropriate relation for the strain gauges and accelerometer.

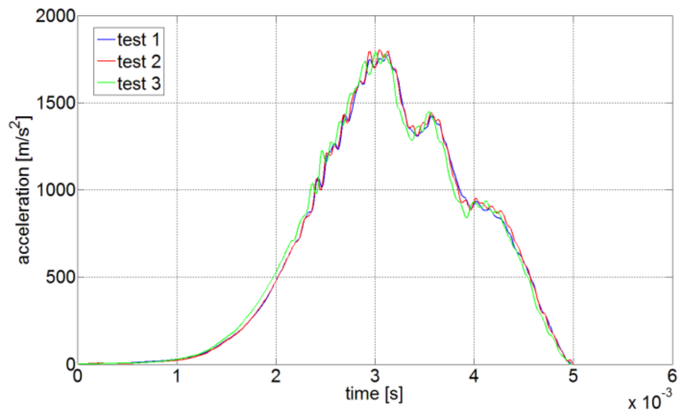
9.2.3. Measured Acceleration Data

Drop tests were conducted from different drop heights, ranging from 20cm to 50cm in steps of 10cm. The drop height of the fixture was controlled and the impact acceleration was recorded. Additionally, a cushioning material was used to damp the impact of the drop test fixture with the safety stops.

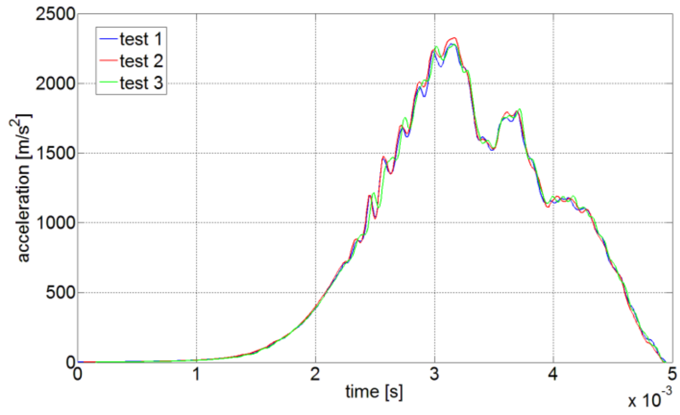
Figure 9-6 shows the acceleration plots obtained from the accelerometer during the actual drop events for drop heights from 20cm to 50cm.



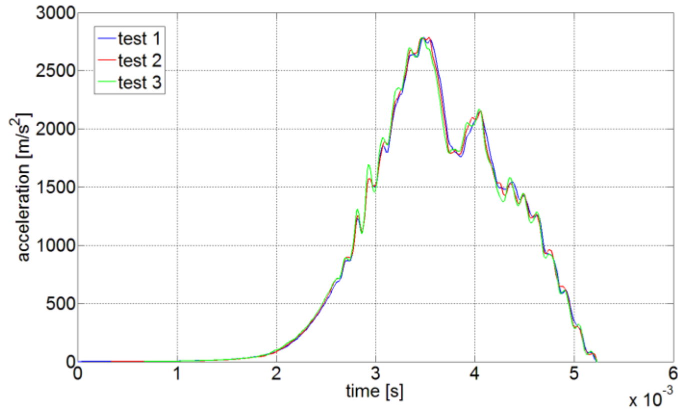
(a) 20cm drop height acceleration data



(b) 30cm drop height acceleration data



(c) 40cm drop height acceleration data



(d) 50cm drop height acceleration data

Figure 9-6 Acceleration magnitude plots for drop tests with drop height from 20cm to 50cm

Table 9-1 shows the averaged measured peak accelerations for different drop heights during the drop testing of the 3-Arc-Fan compliant interconnect samples. The peak acceleration was found to increase almost linearly from a low value of 1263m/s^2 for a drop height of 20cm to 2787m/s^2 for a drop height of 50cm, and was independent of the samples tested.

Table 9-1 Peak acceleration for different drop heights

Drop Height (cm)	Averaged Measured Peak Acceleration (m/s^2)
20	1263
30	1791
40	2296
50	2787

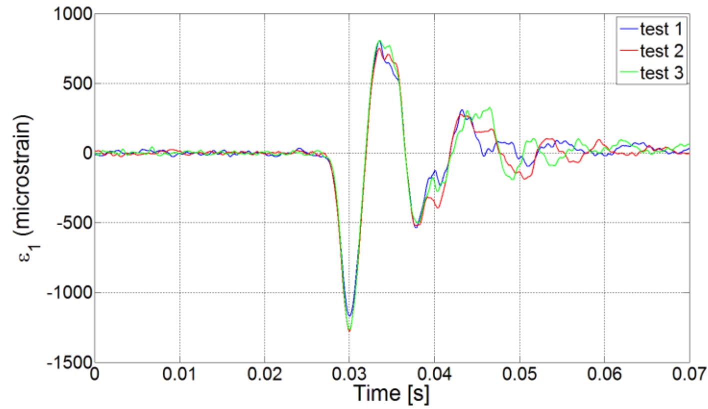
These acceleration data will be used to generate input boundary conditions necessary to conduct finite-element simulations using the Input-G method.

9.2.4. Measured Strain Data

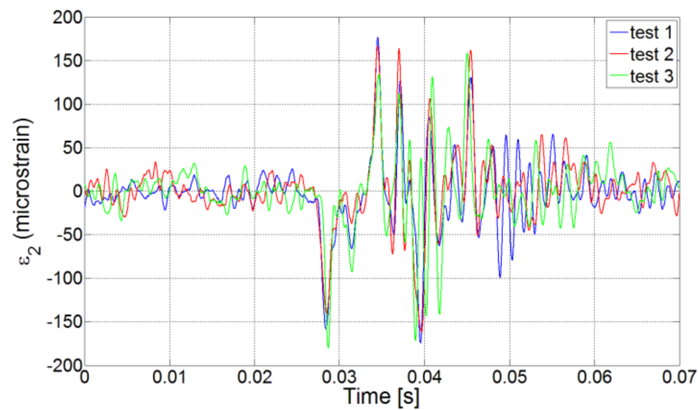
The drop tests were carried out for the samples assembled using the 3-Arc-Fan compliant interconnect with the arcuate beam width equal to 10µm, 15µm and 20µm, which were actually 9.5µm, 14.5µm and 19.5µm respectively after the etching process.

9.2.4.1. Arcuate Beam Width Equal to 10μm

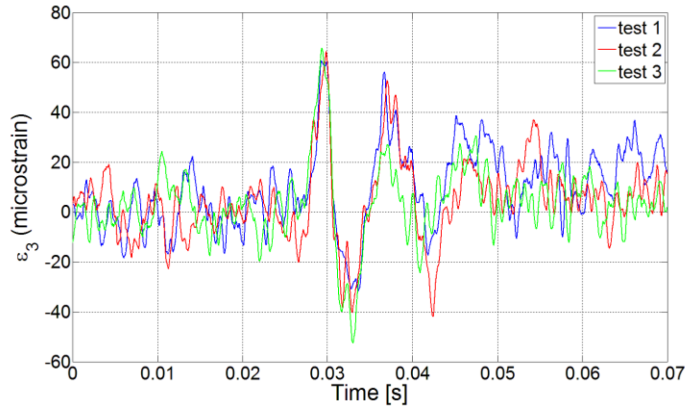
Figure 9-7 to Figure 9-10 show the strain data plots calculated from the strain output data recorded by the strain gauges with drop heights ranging from 20cm to 50cm for the 3-Arc-Fan compliant interconnect with the arcuate beam width equal to 10μm.



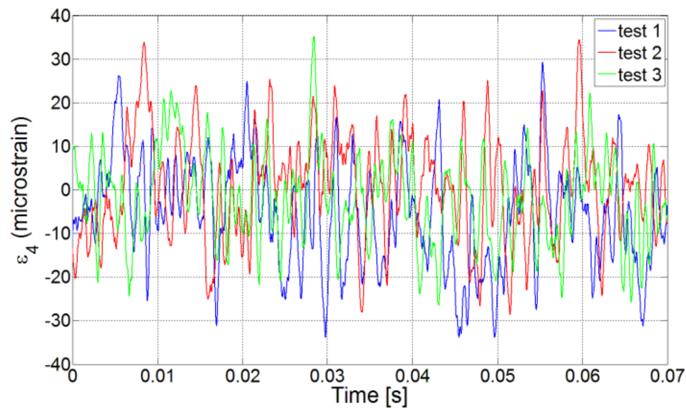
(a) ε_1



(b) ε_2

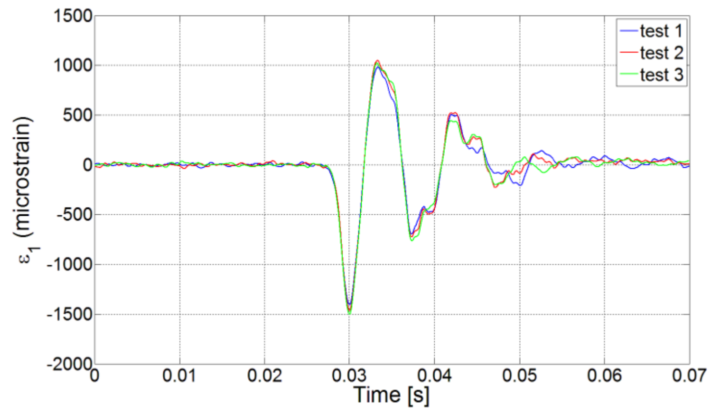


(c) ε_3

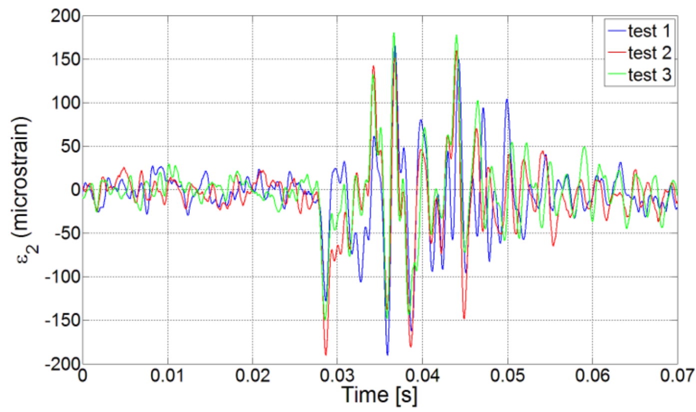


(d) ε_4

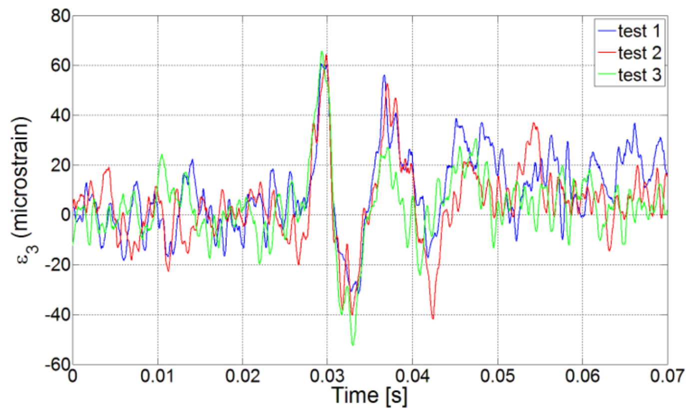
Figure 9-7 Strain data plots for drop tests of the sample with 10µm beam width 3-Arc-Fan compliant interconnect at drop height equal to 20cm



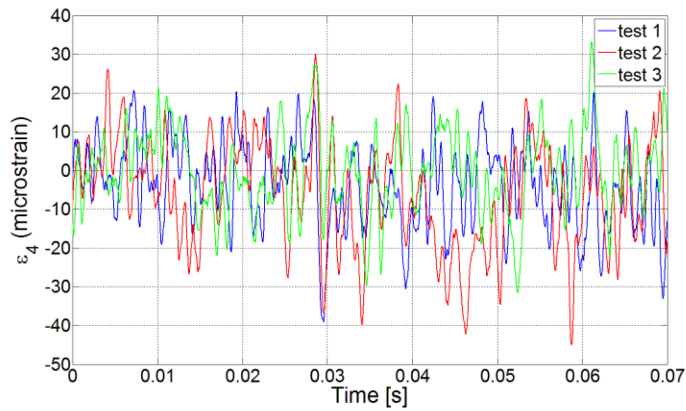
(a) ε_1



(b) ε_2

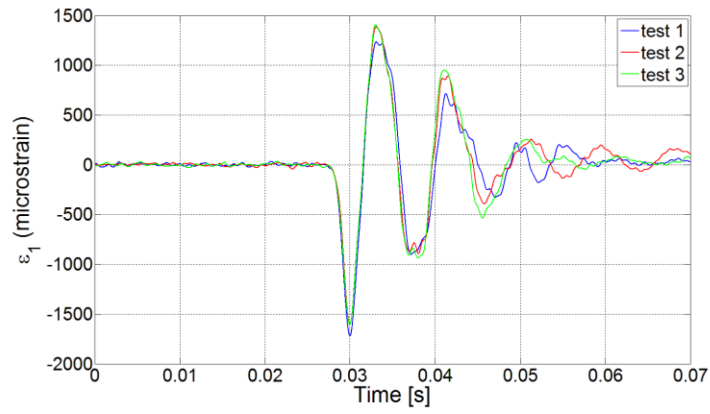


(c) ε_3

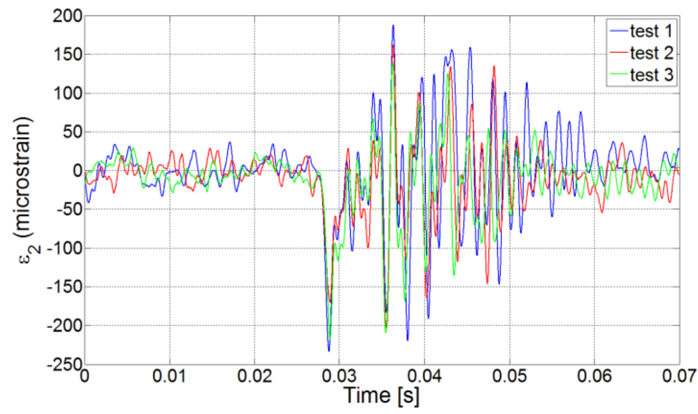


(d) ε_4

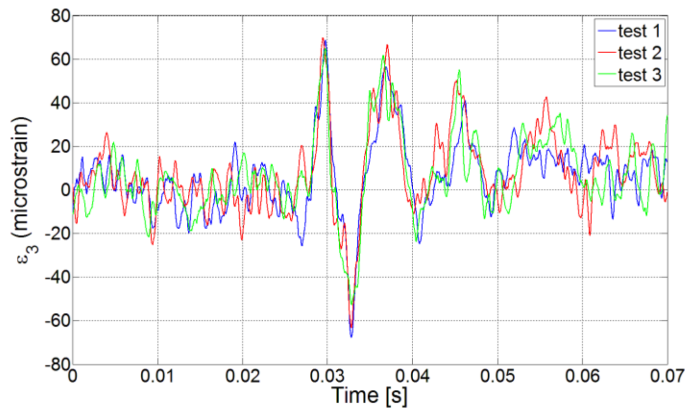
Figure 9-8 Strain data plots for drop tests of the sample with 10μm beam width 3-Arc-Fan compliant interconnect at drop height equal to 30cm



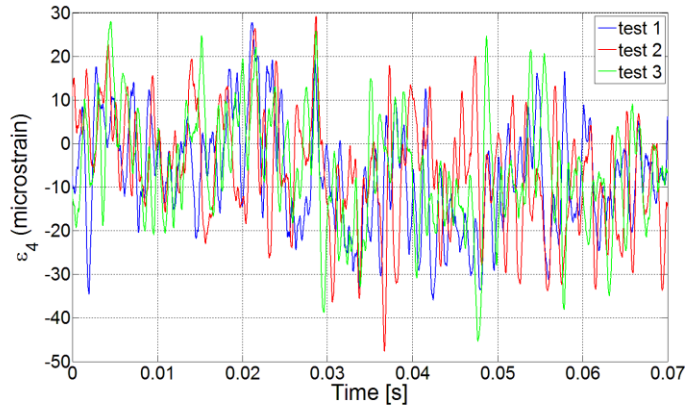
(a) ε_1



(b) ε_2

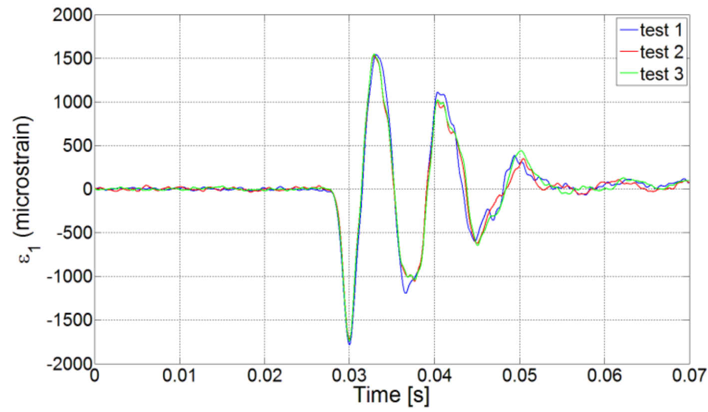


(c) ε_3

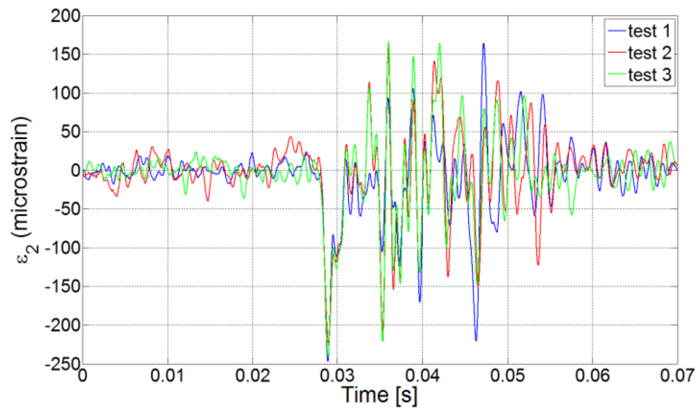


(d) ε_4

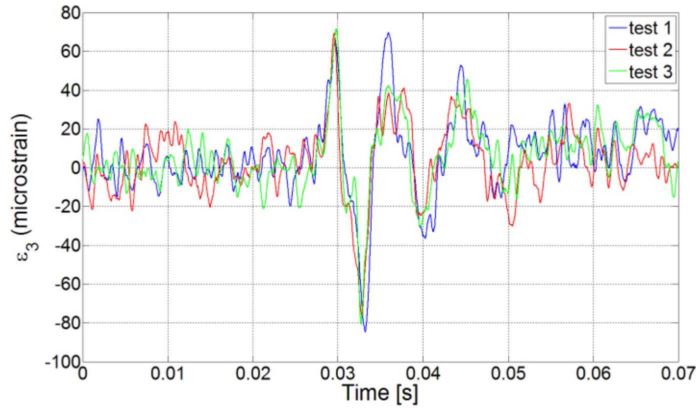
Figure 9-9 Strain data plots for drop tests of the sample with 10µm beam width 3-Arc-Fan compliant interconnect at drop height equal to 40cm



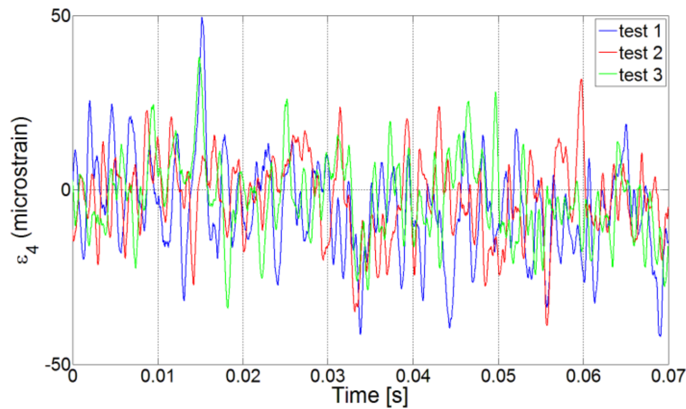
(a) ε_1



(b) ε_2



(c) ε_3



(d) ε_4

Figure 9-10 Strain data plots for drop tests of the sample with 10μm beam width 3-Arc-Fan compliant interconnect at drop height equal to 50cm

It can be seen from Figure 9-7 to Figure 9-10 that ε_1 and ε_3 are more distinct than ε_2 and ε_4, because 1) ε_1 and ε_3 measure the normal strain values in the longitudinal direction which are more dominant during the drop tests; 2) the organic board's longitudinal dimension is almost twice as much as its transverse dimension, and thus, upon impact and subsequent vibrations, the deformation of the board in the longitudinal direction is more dominant than its deformation in the transverse direction. Therefore, ε_2 is determined by the combination of the Poisson's effect which results in the opposite sign of ε_1 and the deformation in the transverse direction which results in the same sign of ε_1; 3) ε_4 which measures the normal strain in the transverse direction on the silicon

substrate is very small due to the vibration isolation characteristic of the compliant interconnects, and is indistinguishable from the noise. Therefore, ε_1 and ε_3 were selected for all the drop tests to demonstrate the vibration isolation characteristic of the 3-Arc-Fan compliant interconnect, and the board-to-substrate strain ratios at the first and second peaks were calculated to quantify the isolation factor.

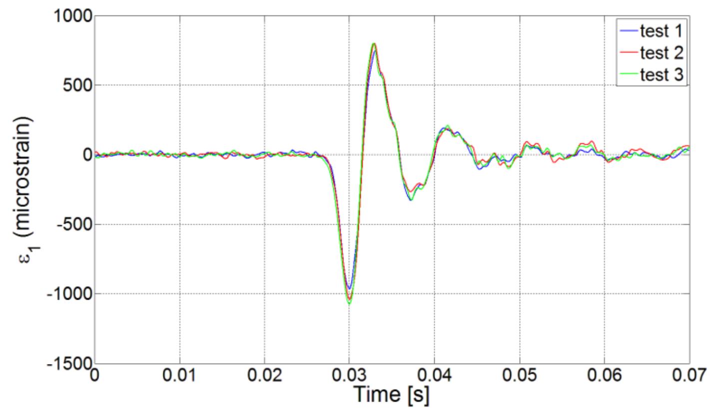
Table 9-2 shows the average peak microstrain values of ε_1 and ε_3 for drop tests of the sample with 10μm beam width 3-Arc-Fan compliant interconnect at different drop heights, and the ratios of the board to substrate strain at the 1st and 2nd peaks. The average board-to-substrate strain ratios were calculated as 23.13 and 21.55.

Table 9-2 Average peak microstrain values of ε_1 and ε_3 for drop tests of the sample with 10*μm* beam width 3-Arc-Fan compliant interconnect at different drop heights, and the board-to-substrate strain ratio at the 1st and 2nd peaks

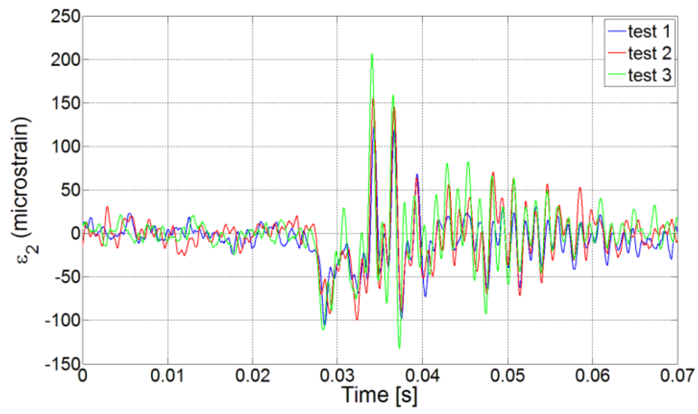
Drop Height [cm]	Average ε_1 [microstrain]		Average ε_3 [microstrain]		1st Peak Ratio	2nd Peak Ratio
	1st Peak	2nd Peak	1st Peak	2nd Peak		
20	-1238	787.7	61.81	-36.69	20.03	20.74
30	-1458	1017	63.58	-41.51	22.93	24.50
40	-1643	1343	67.77	-61.28	24.24	21.92
50	-1747	1536	68.99	-80.70	25.32	19.03
Average Board-to-Substrate Strain Ratio:					23.13	21.55

9.2.4.2. Arcuate Beam Width Equal to 15μm

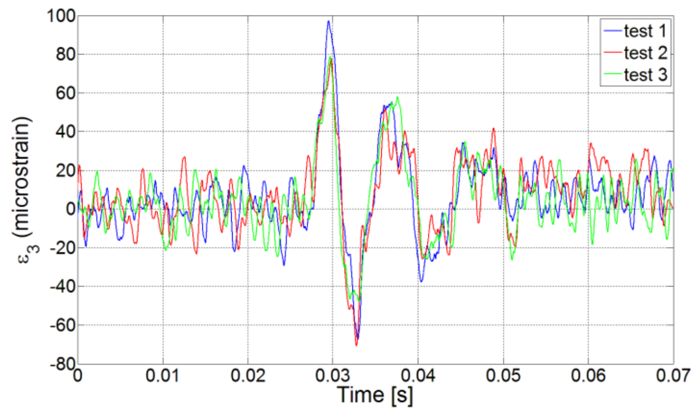
Figure 9-11 to Figure 9-14 show the strain data plots calculated from the strain output data recorded by the strain gauges with drop heights ranging from 20cm to 50cm for the 3-Arc-Fan compliant interconnect with the arcuate beam width equal to 15μm.



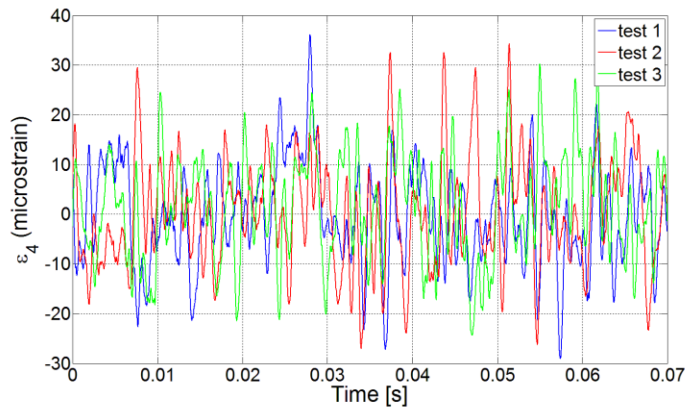
(a) ε_1



(b) ε_2

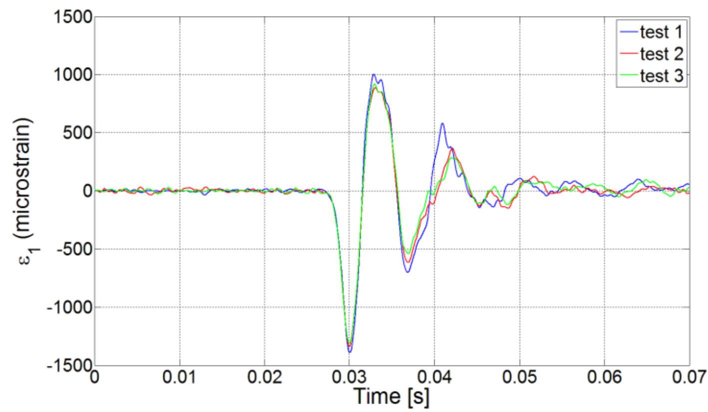


(c) ε_3

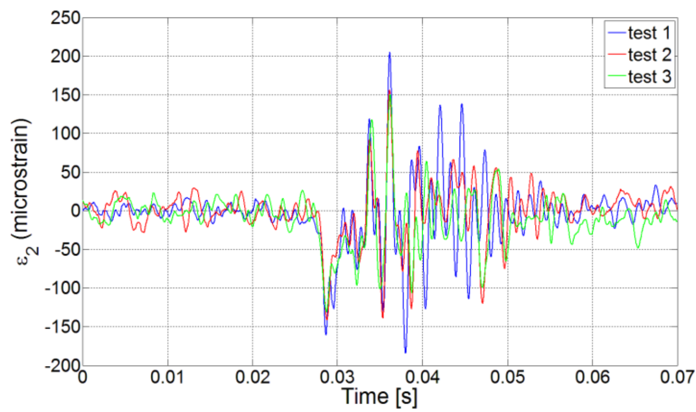


(d) ε_4

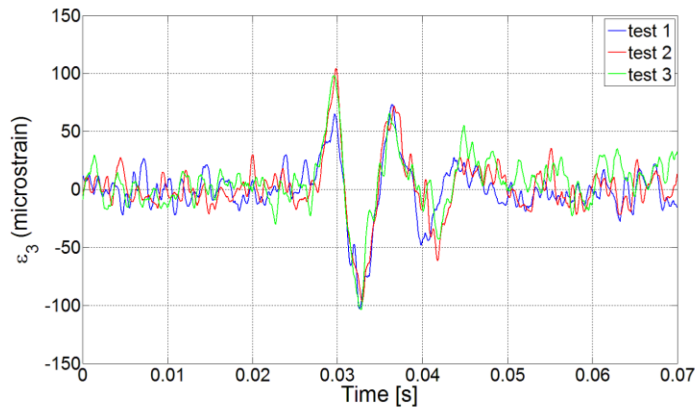
Figure 9-11 Strain data plots for drop tests of the sample with 15µm beam width 3-Arc-Fan compliant interconnect at drop height equal to 20cm



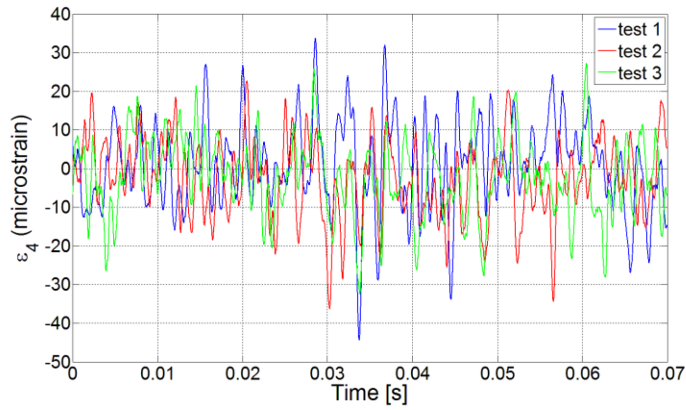
(a) ε_1



(b) ε_2

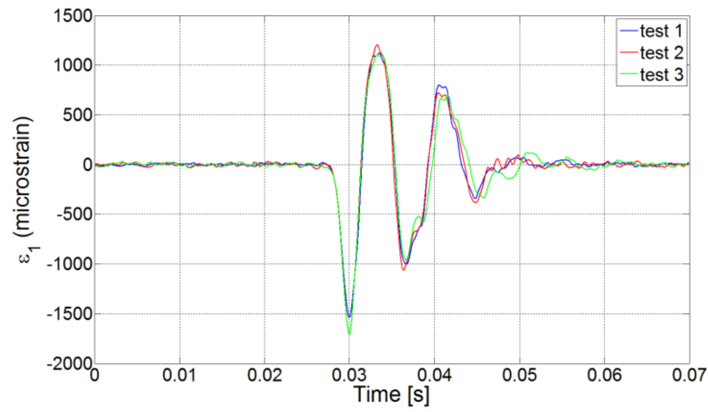


(c) ε_3

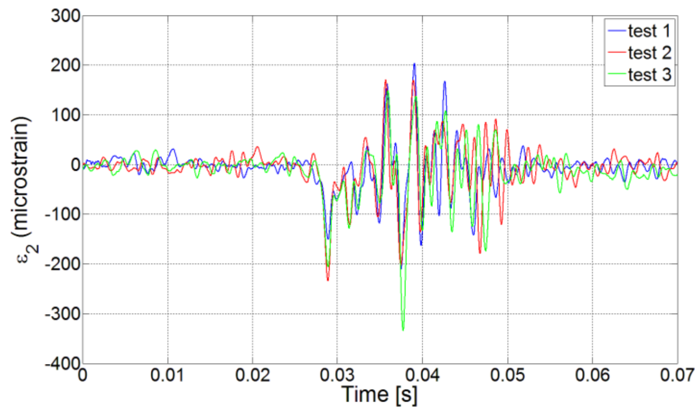


(d) ε_4

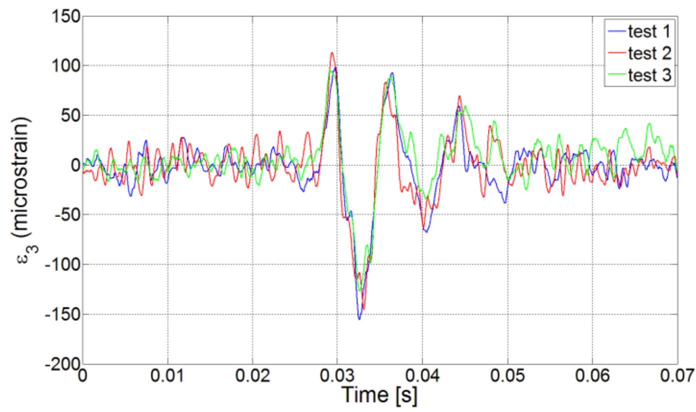
Figure 9-12 Strain data plots for drop tests of the sample with 15µm beam width 3-Arc-Fan compliant interconnect at drop height equal to 30cm



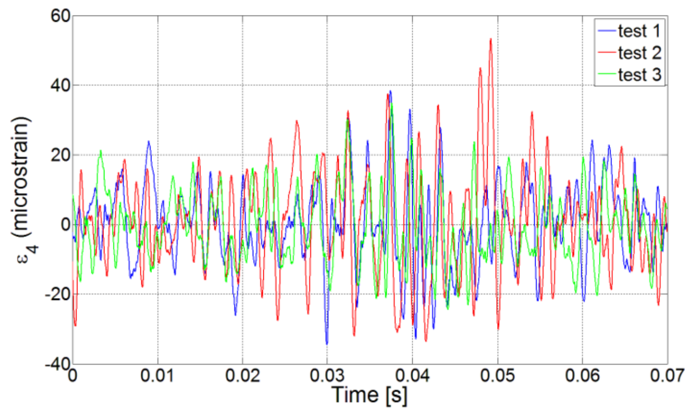
(a) ε_1



(b) ε_2

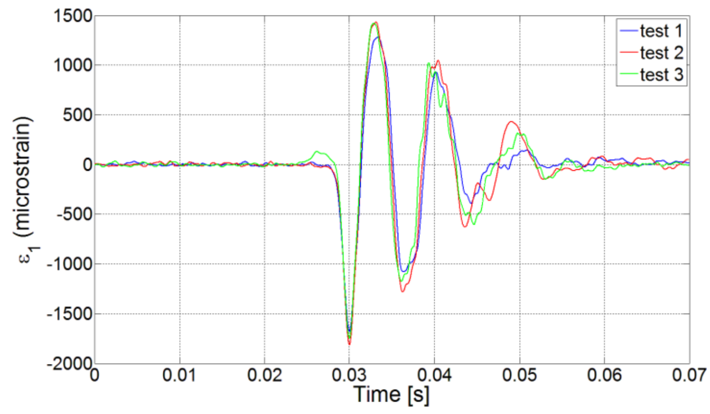


(c) ε_3

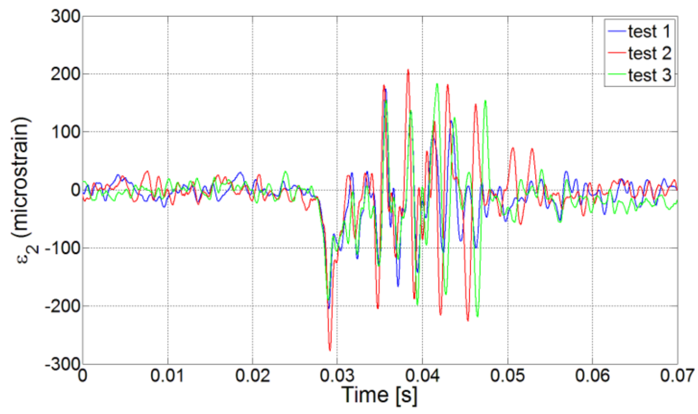


(d) ε_4

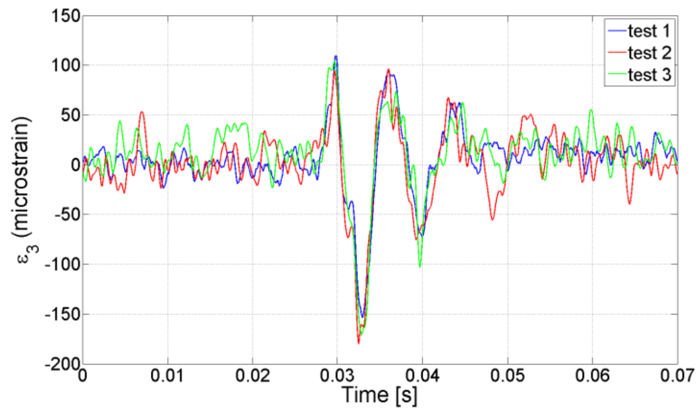
Figure 9-13 Strain data plots for drop tests of the sample with 15µm beam width 3-Arc-Fan compliant interconnect at drop height equal to 40cm



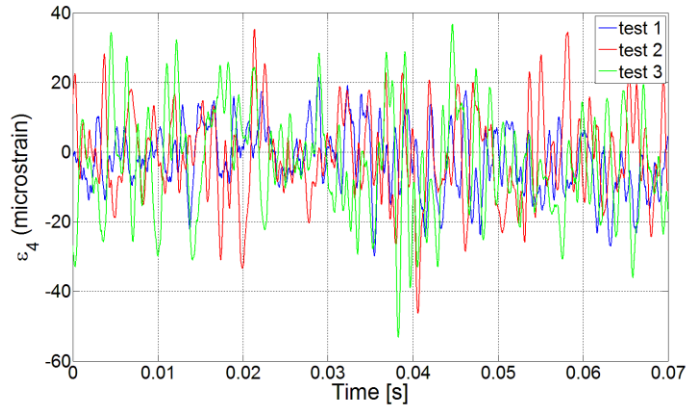
(a) ε_1



(b) ε_2



(c) ε_3



(d) ε_4

Figure 9-14 Strain data plots for drop tests of the sample with 15μm beam width 3-Arc-Fan compliant interconnect at drop height equal to 50cm

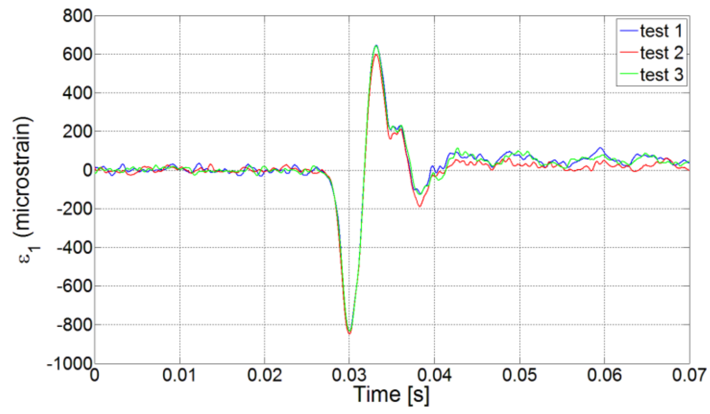
Table 9-3 shows the average peak microstrain values of ε_1 and ε_3 for drop tests of the sample with 15μm beam width 3-Arc-Fan compliant interconnect at different drop heights, and the ratios of the board to substrate strain at the 1st and 2nd peaks. The average board-to-substrate strain ratios were calculated as 15.10 and 9.53.

Table 9-3 Average peak microstrain values of ε_1 and ε_3 for drop tests of the sample with 15*μm* beam width 3-Arc-Fan compliant interconnect at different drop heights, and the board-to-substrate strain ratio at the 1st and 2nd peaks

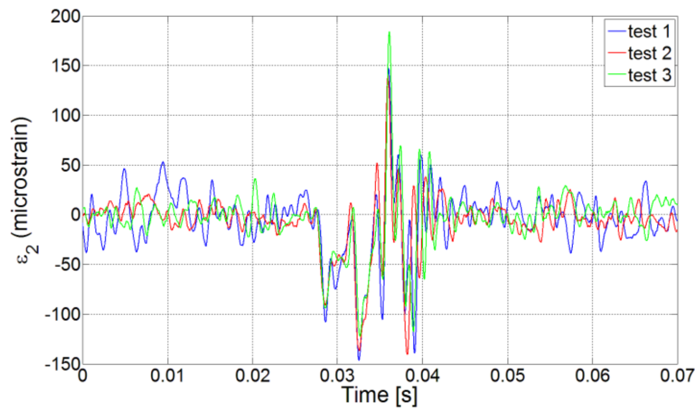
Drop Height [cm]	Average ε_1 [microstrain]		Average ε_3 [microstrain]		1st Peak Ratio	2nd Peak Ratio
	1st Peak	2nd Peak	1st Peak	2nd Peak		
20	-1027	782.8	84.56	-61.97	12.15	12.63
30	-1348	937.6	89.18	-101.1	15.12	9.27
40	-1651	1143	102.4	-142.6	16.12	8.02
50	-1749	1380	102.7	-168.3	17.03	8.20
Average Board-to-Substrate Strain Ratio					15.10	9.53

9.2.4.3. Arcuate Beam Width Equal to 20μm

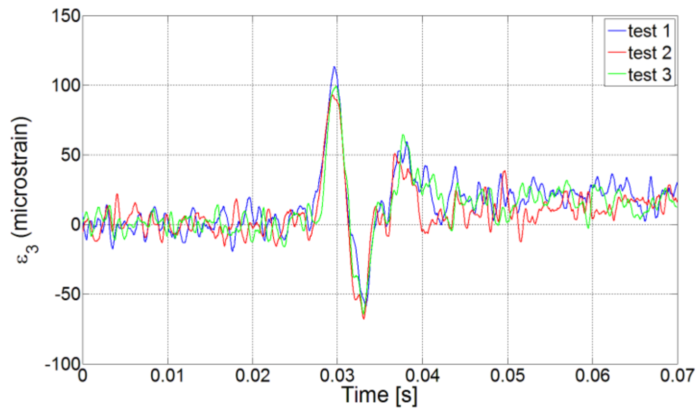
Figure 9-15 to Figure 9-18 show the strain data plots calculated from the strain output data recorded by the strain gauges with drop heights ranging from 20cm to 50cm for the 3-Arc-Fan compliant interconnect with the arcuate beam width equal to 20μm.



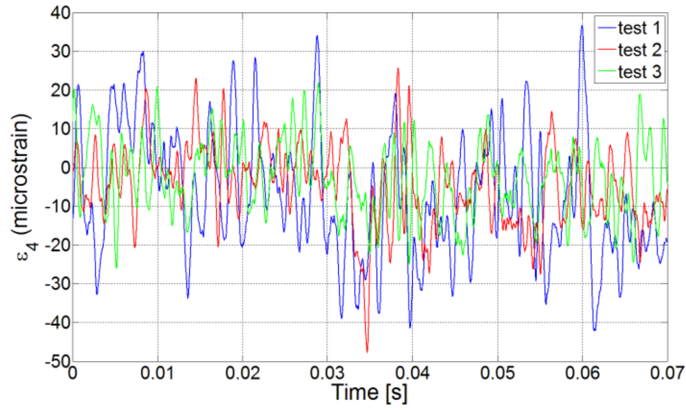
(a) ε_1



(b) ε_2

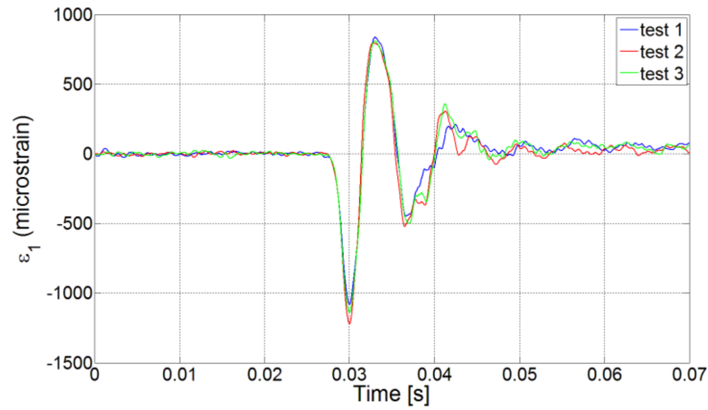


(c) ε_3

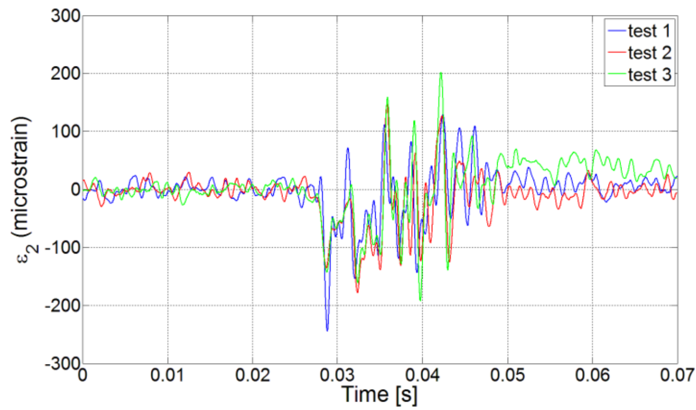


(d) ε_4

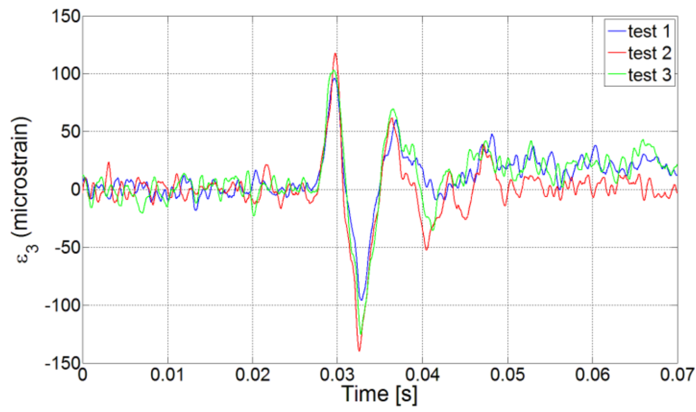
Figure 9-15 Strain data plots for drop tests of the sample with 20μm beam width 3-Arc-Fan compliant interconnect at drop height equal to 20cm



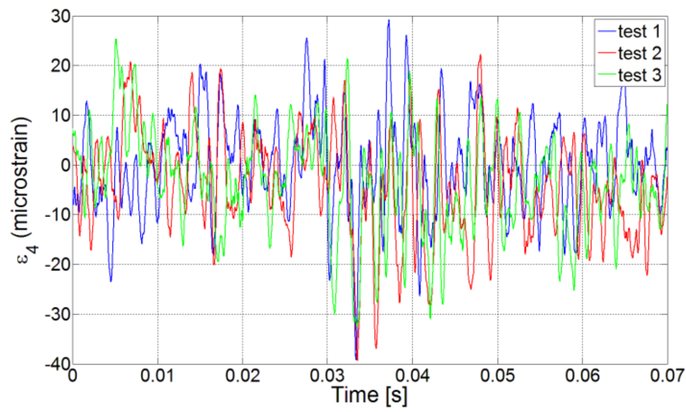
(a) ε_1



(b) ε_2

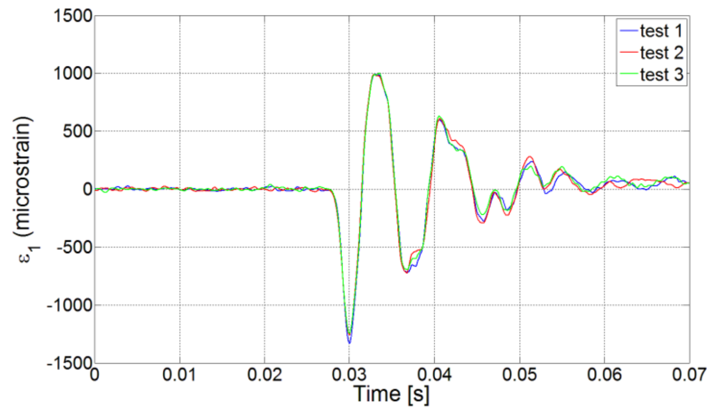


(c) ε_3

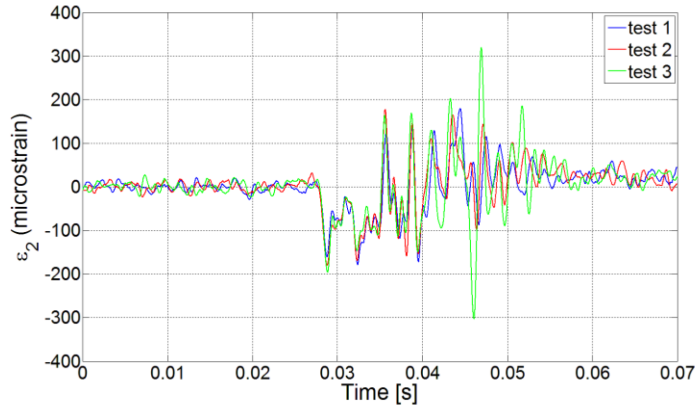


(d) ε_4

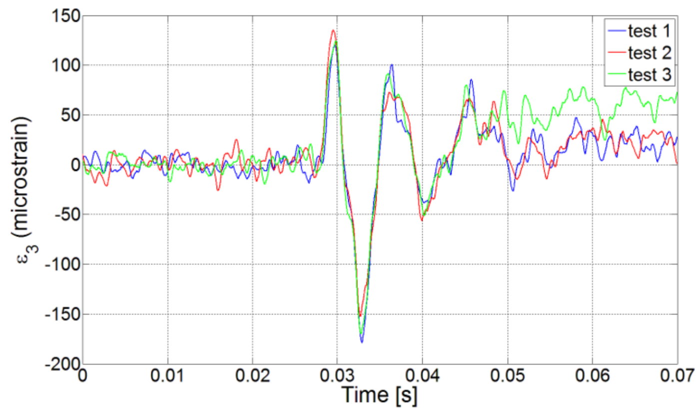
Figure 9-16 Strain data plots for drop tests of the sample with 20μm beam width 3-Arc-Fan compliant interconnect at drop height equal to 30cm



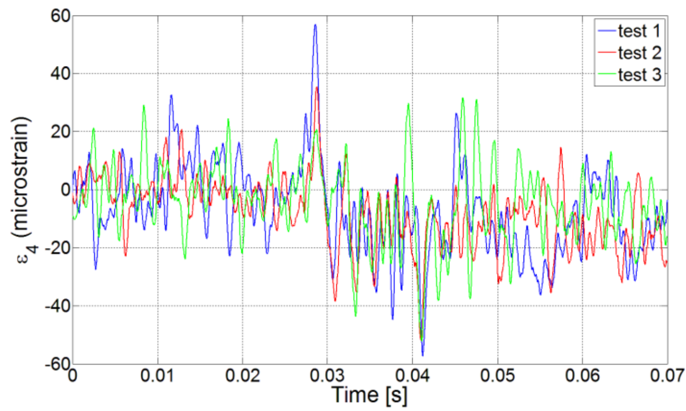
(a) ε_1



(b) ε_2

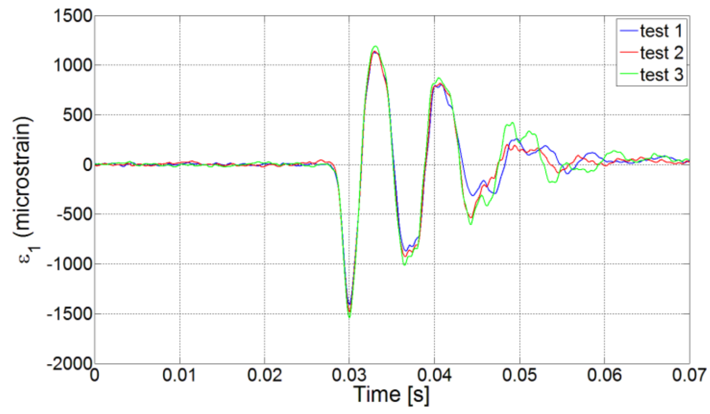


(c) ε_3

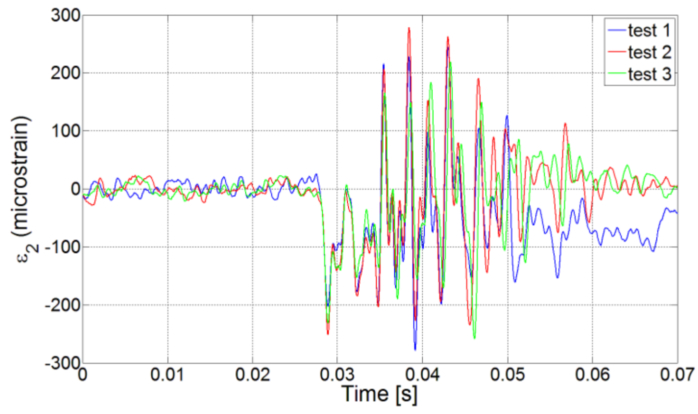


(d) ε_4

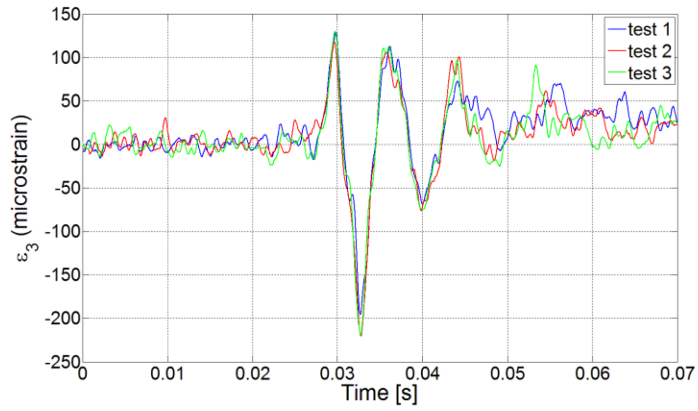
Figure 9-17 Strain data plots for drop tests of the sample with 20µm beam width 3-Arc-Fan compliant interconnect at drop height equal to 40cm



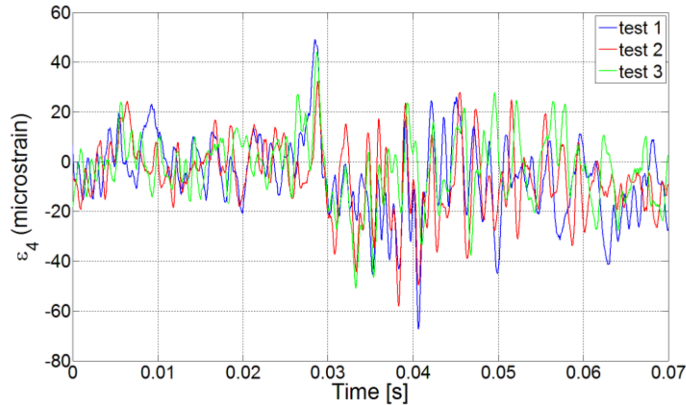
(a) ε_1



(b) ε_2



(c) ε_3



(d) ε_4

Figure 9-18 Strain data plots for drop tests of the sample with 20μm beam width 3-Arc-Fan compliant interconnect at drop height equal to 50cm

Table 9-4 shows the average peak microstrain values of ε_1 and ε_3 for drop tests of the sample with 20μm beam width 3-Arc-Fan compliant interconnect at different drop heights, and the ratios of the board to substrate strain at the 1st and 2nd peaks. The average board-to-substrate strain ratios were calculated as 10.23 and 7.01.

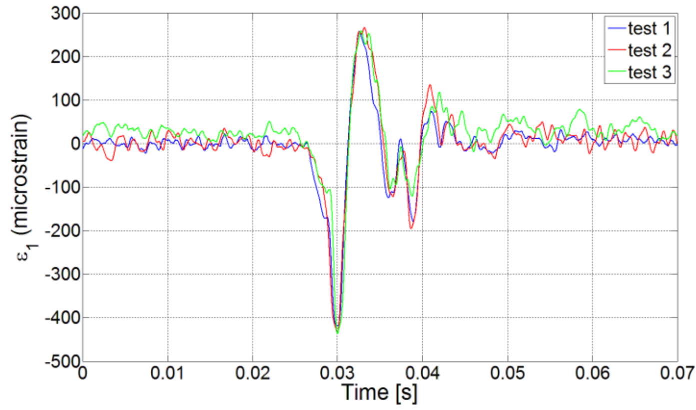
Table 9-4 Average peak microstrain values of ε_1 and ε_3 for drop tests of the sample with 20*μm* beam width 3-Arc-Fan compliant interconnect at different drop heights, and the board-to-substrate strain ratio at the 1st and 2nd peaks

Drop Height [cm]	Average ε_1 [microstrain]		Average ε_3 [microstrain]		1st Peak Ratio	2nd Peak Ratio
	1st Peak	2nd Peak	1st Peak	2nd Peak		
20	-838.3	629.0	101.9	-63.57	8.23	9.89
30	-1148	814.1	105.8	-120.4	10.85	6.76
40	-1278	994.6	126.7	-167.1	10.09	5.95
50	-1478	1153	125.7	-211.7	11.76	5.45
Average Board-to-Substrate Strain Ratio					10.23	7.01

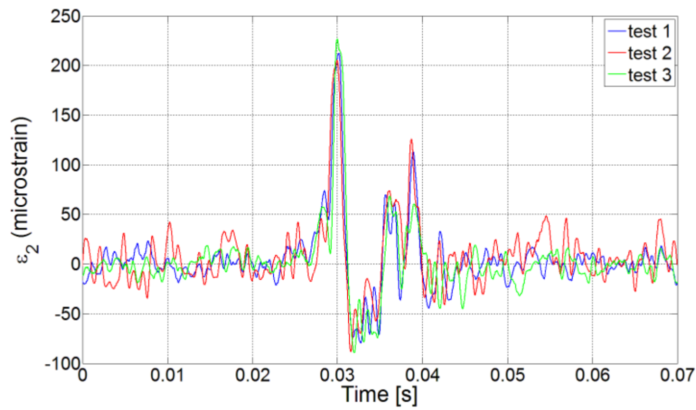
9.2.4.4. Solder Ball Interconnects

The drop tests for the sample using solder ball interconnects were also conducted at different drop heights. The height of the solder balls is equal to the standoff of the compliant interconnects and the maximum diameter of the solder balls is equal to the footprint of the compliant interconnects. The normal strain values on both the organic

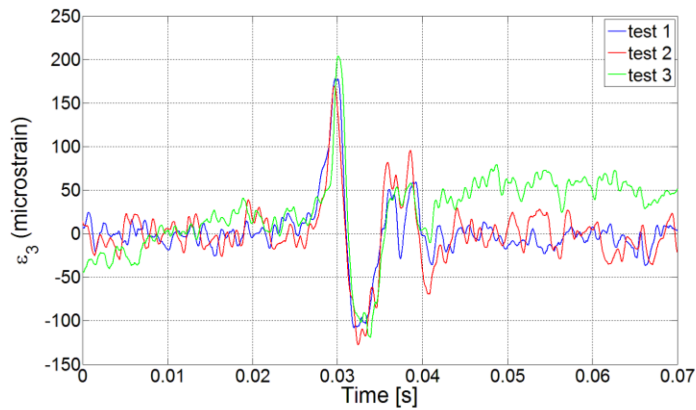
board and the silicon substrate at the same location were also recorded, in order to compare against the results obtained from the 3-Arc-Fan compliant interconnect samples.



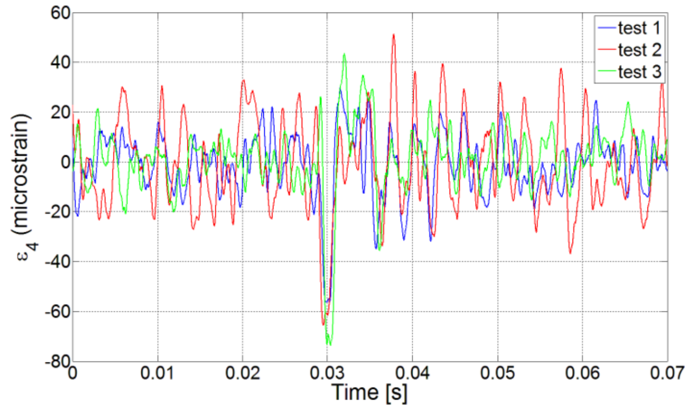
(a) ε_1



(b) ε_2

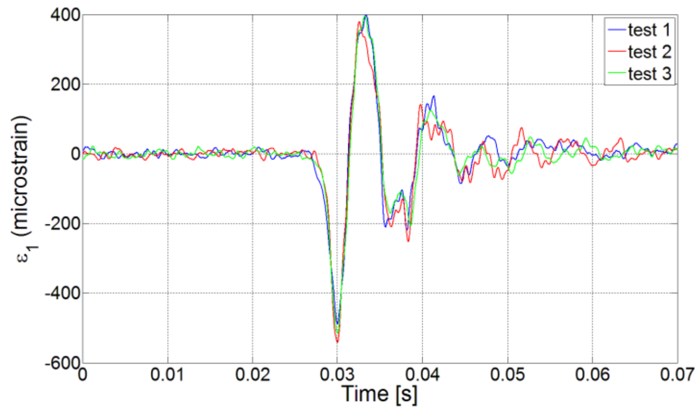


(c) ε_3

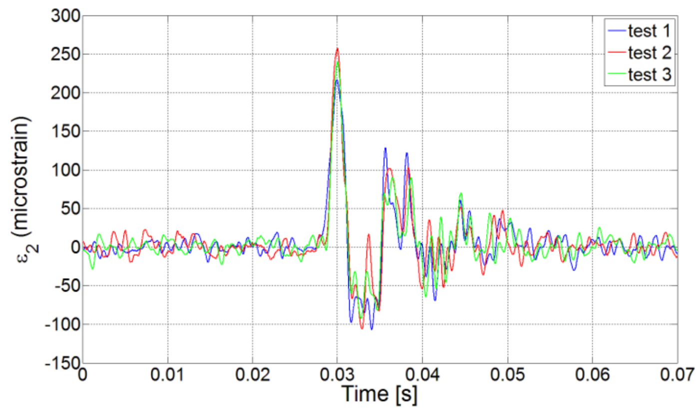


(d) ε_4

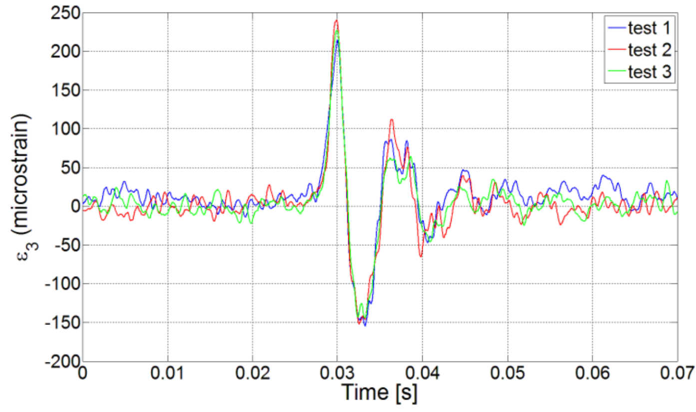
Figure 9-19 Strain data plots for drop tests of the sample using solder ball interconnects at drop height equal to 20cm



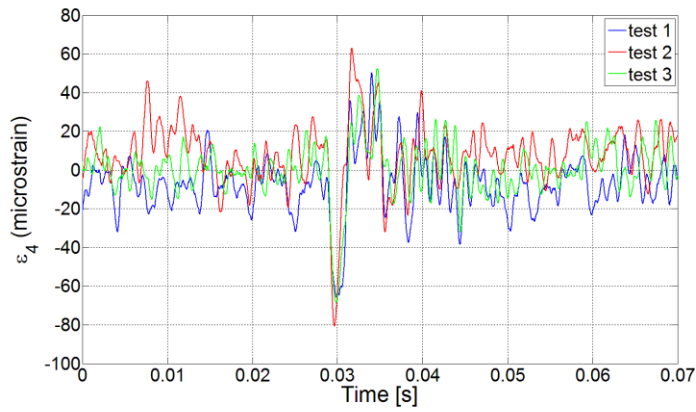
(a) ε_1



(b) ε_2

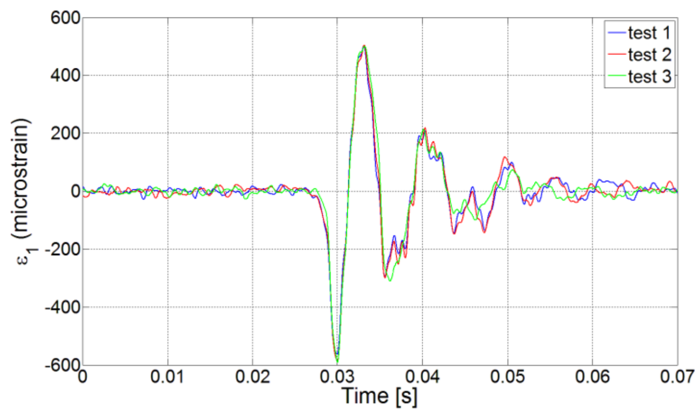


(c) ε_3

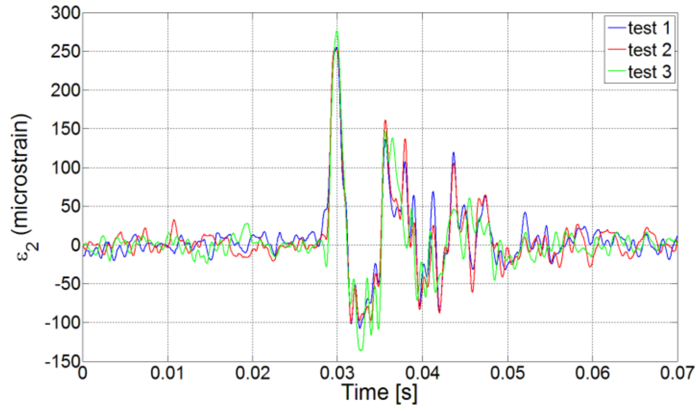


(d) ε_4

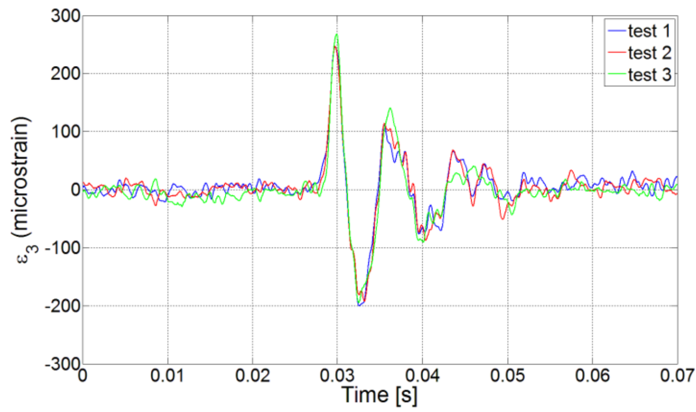
Figure 9-20 Strain data plots for drop tests of the sample using solder ball interconnects at drop height equal to 30cm



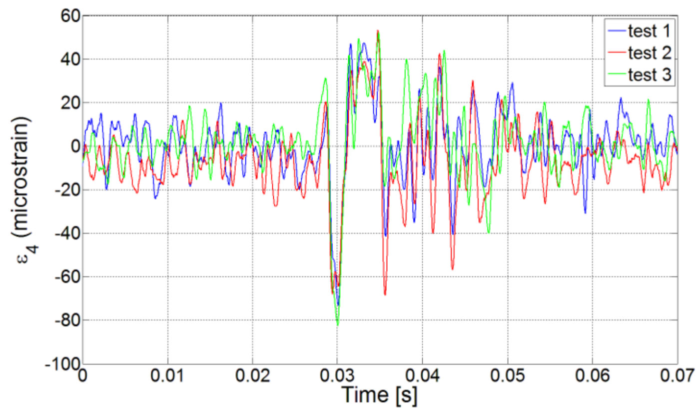
(a) ε_1



(b) ε_2

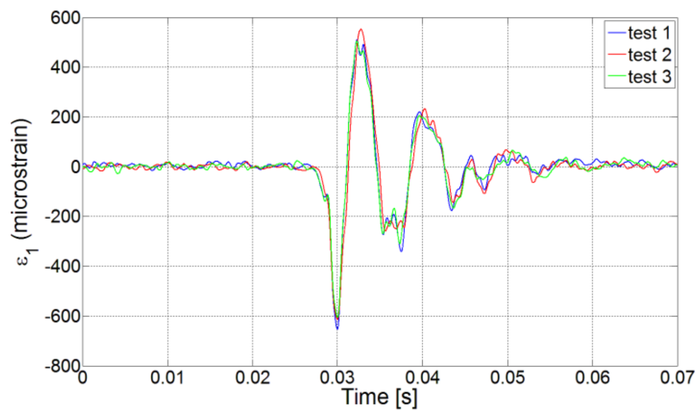


(c) ε_3

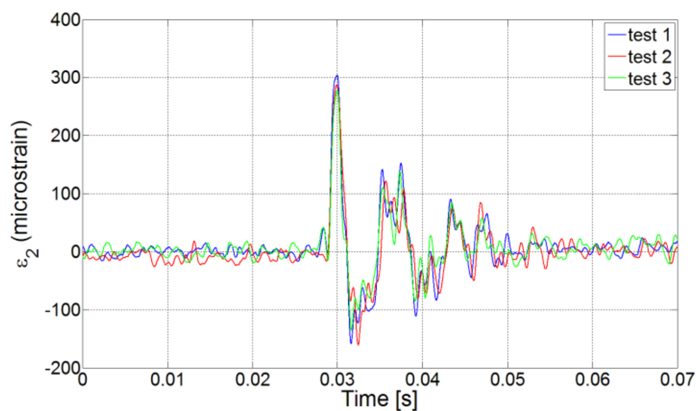


(d) ε_4

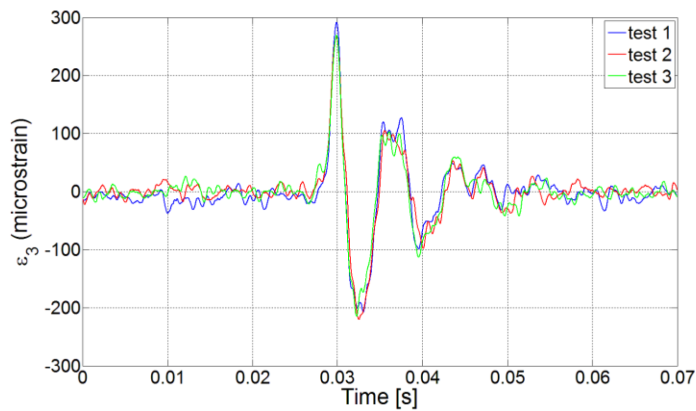
Figure 9-21 Strain data plots for drop tests of the sample using solder ball interconnects at drop height equal to 40cm



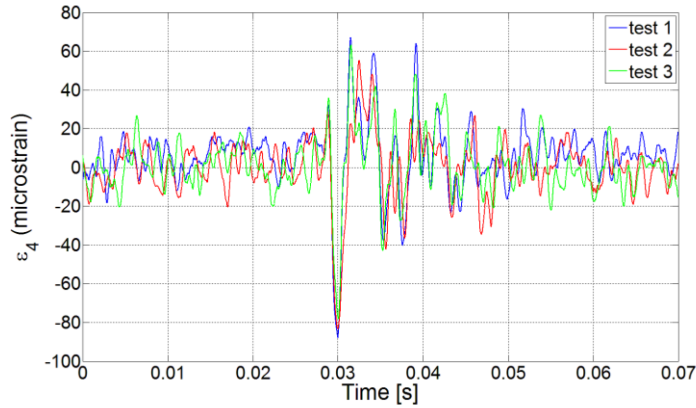
(a) ε_1



(b) ε_2



(c) ε_3



(d) ε_4

Figure 9-22 Strain data plots for drop tests of the sample using solder ball interconnects at drop height equal to 50cm

Table 9-5 shows the average peak microstrain values of ε_1 and ε_3 for drop tests of the sample using solder ball interconnects at different drop heights, and the ratios of the board to substrate strain at the 1st and 2nd peaks. The average board-to-substrate strain ratios were calculated as 2.29 and 2.46.

Table 9-5 Average peak microstrain values of ε_1 and ε_3 for drop tests of the sample using solder ball interconnects at different drop heights, and the ratio of the board to substrate strain at the 1st and 2nd peaks

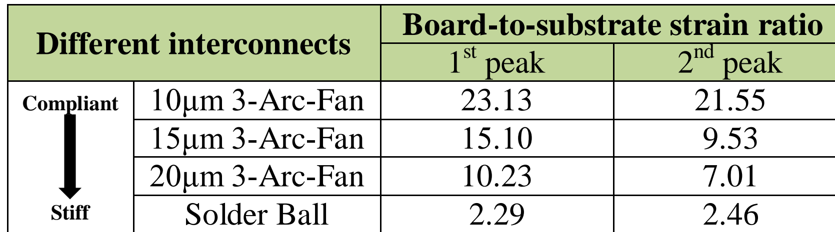
Drop Height [cm]	Average ε_1 [microstrain]		Average ε_3 [microstrain]		1st Peak Ratio	2nd Peak Ratio
	1st Peak	2nd Peak	1st Peak	2nd Peak		
20	-430.5	261.3	183.7	-118.3	2.34	2.21
30	-515.4	391.0	227.3	-150.4	2.27	2.60
40	-579.4	502.3	253.7	-195.8	2.28	2.57
50	-624.5	523.4	275.8	-214.4	2.26	2.44
Average Board-to-Substrate Strain Ratio					2.29	2.46

9.2.4.5. Comparison among Different Interconnects

The board-to-substrate strain ratios for compliant interconnects with different arcuate beam width values and solder ball interconnect are summarized and compared in Table 9-6. The board-to-substrate strain ratios at the 1st peak for the compliant interconnects with arcuate beam width equal to 10µm, 15µm and 20µm are 23.13, 15.10

and 10.23, respectively, which are significantly greater than the ratio when the solder balls are used as the interconnects which is 2.29. The board-to-substrate strain ratios at the 2nd peak for the compliant interconnects with arcuate beam width equal to 10μm, 15μm and 20μm are 21.55, 9.53 and 7.01, respectively, while the ratio is only 2.46 when the solder balls are used as the interconnects. It can also be seen that the more compliant the interconnect is the higher the board-to-substrate strain ratio will be, and hence can better isolate the strain transfer from the board to the substrate.

Table 9-6 Board-to-substrate strain ratios for compliant interconnects with different arcuate beam width values and solder ball interconnect

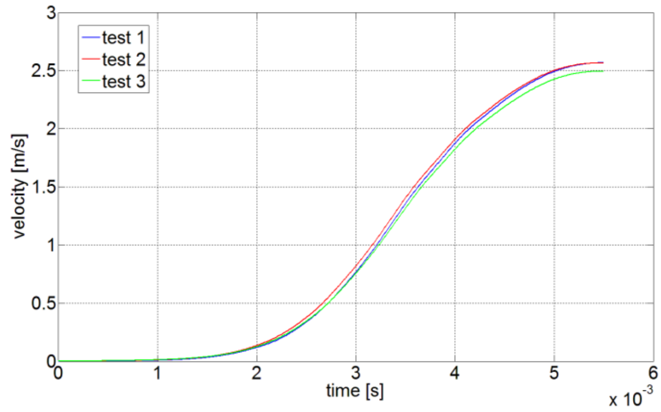


Different interconnects		Board-to-substrate strain ratio	
		1st peak	2nd peak
Compliant ↓ Stiff	10μm 3-Arc-Fan	23.13	21.55
	15μm 3-Arc-Fan	15.10	9.53
	20μm 3-Arc-Fan	10.23	7.01
	Solder Ball	2.29	2.46

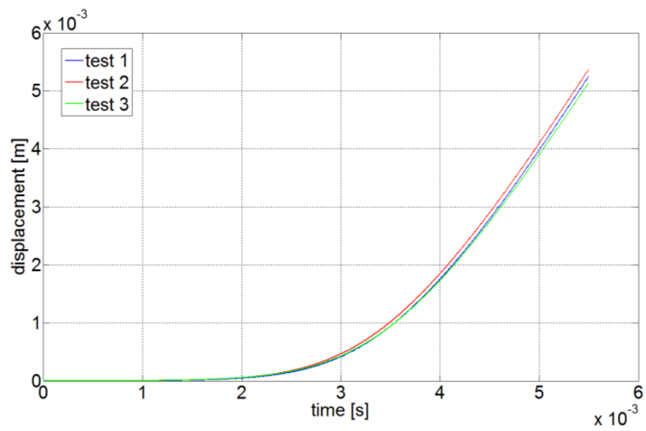
9.3. DROP TEST SIMULATION

9.3.1. Simulation Boundary Conditions

In addition to experiments, numerical simulations were carried out to determine the strain transfer ratio under drop conditions from different heights. According to the discussion in the previous chapter, direct integral based on the measured acceleration was used to obtain the displacement boundary conditions. Figure 9-23 to Figure 9-26 show the velocity and displacement boundary condition curves for the drop tests at different heights. And the displacement curves will be used as the input boundary conditions in the finite-element simulations using the Input-G method.

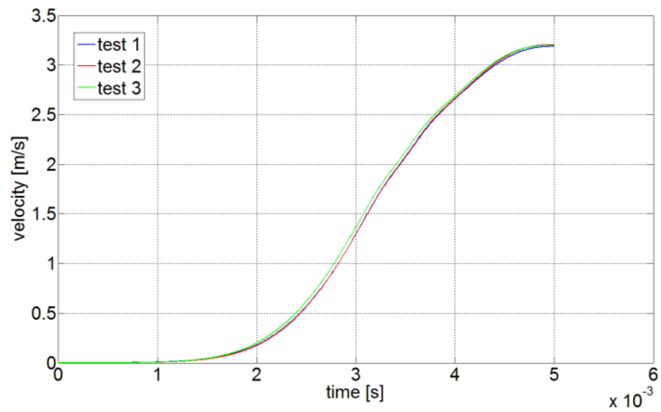


(a) Velocity curves for 20cm height drop test

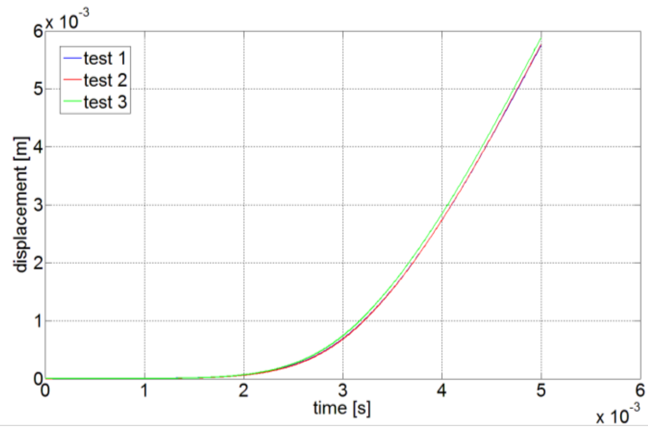


(b) Displacement curves for 20cm height drop test

Figure 9-23 Velocity and displacement boundary condition curves for three 20cm drop test events

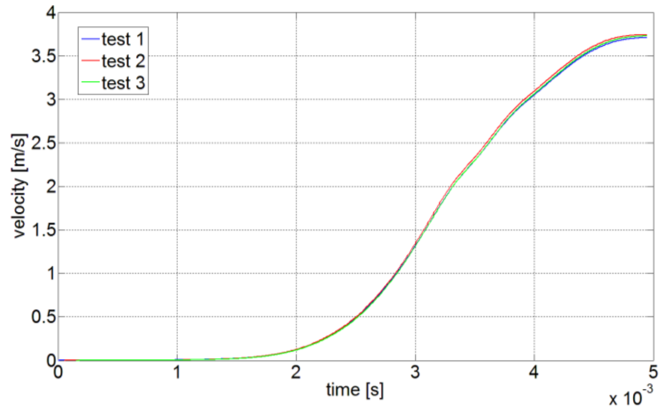


(a) Velocity curves for 30cm height drop test

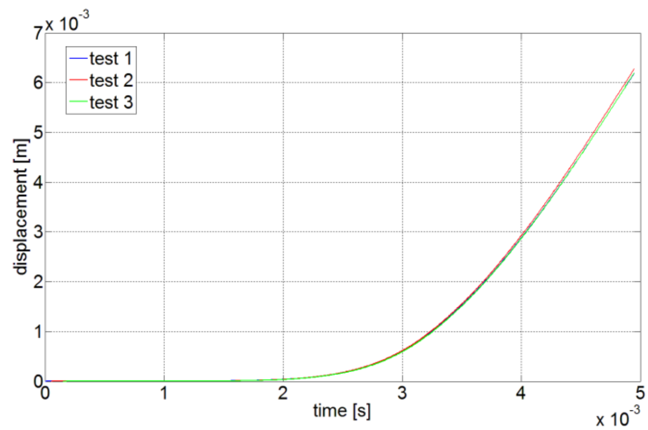


(b) Displacement curves for 30cm height drop test

Figure 9-24 Velocity and displacement boundary condition curves for three 30cm drop test events

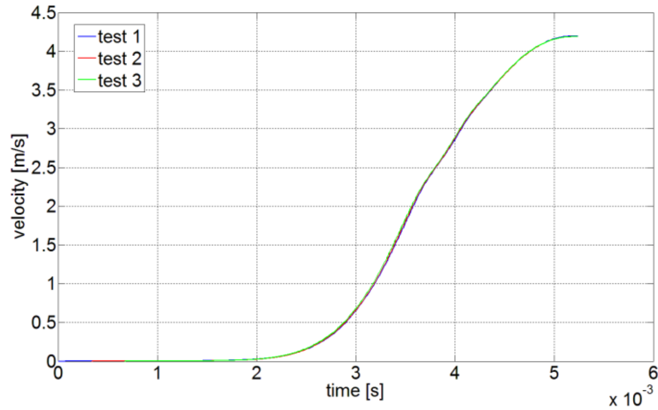


(a) Velocity curves for 40cm height drop test

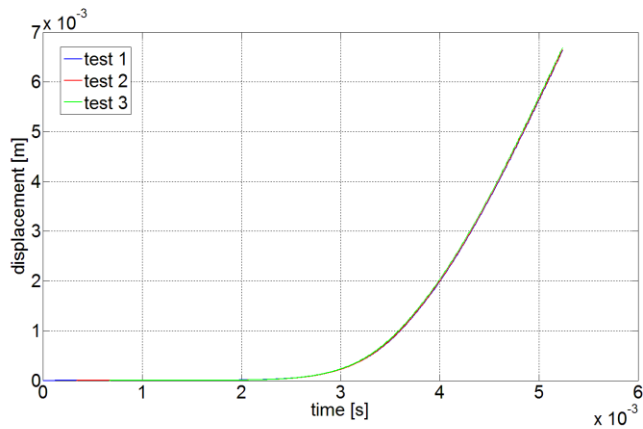


(b) Displacement curves for 40cm height drop test

Figure 9-25 Velocity and displacement boundary condition curves for three 40cm drop test events



(a) Velocity curves for 50cm height drop test



(b) Displacement curves for 50cm height drop test

Figure 9-26 Velocity and displacement boundary condition curves for three 50cm drop test events

9.3.2. Simplified Finite-Element Model

The geometry of this model consists of about 2000 compliant interconnects at a 400-μm pitch on the 18mm × 18mm silicon substrate, and of still about 500 compliant interconnects if the ¼ symmetry is used. The dimension of the ¼ model ranging from 10μm (arcuate beam width) to 66mm (half substrate width) makes the mesh size control relatively difficult for this 3D problem and more meshes will be needed in order to avoid badly shaped elements. Figure 9-27 shows the side and isometric views of the meshed pitch-size model with one 3-Arc-Fan interconnect. There are totally 4266 elements and 20% of them are badly shaped. To reduce the error/warning elements, finer mesh size are

needed which will lead to larger number of elements. Thus, more than 2 million elements are needed for a one quarter model. So a simplified model is necessary for this problem.

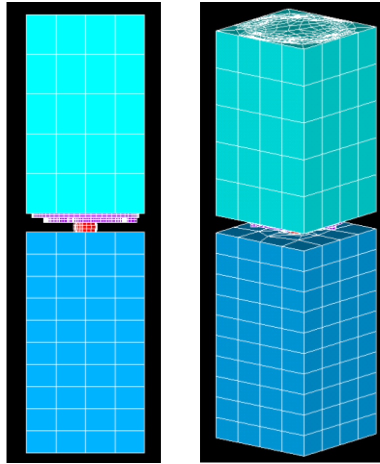


Figure 9-27 Mesh control for the pitch-size of the real model, including 4266 elements in total with 20% of them badly shaped. To reduce the error/warning elements, finer mesh size will be needed.

The mechanically compliant property of the 3-Arc-Fan interconnects is the reason that the substrate is mechanically decoupled from the board, so a much simpler model with the same in-plane and out-of-plane compliance values will be selected to replace the 3-Arc-Fan interconnect in the ANSYS® model. Thus, the complex 3-Arc-Fan interconnect is replaced with an orthotropic short column with its diameter ($D = 2\times R$) equal to the interconnect footprint and its height equal (h) to the interconnect stand-off, shown in Figure 9-28. The reason why short wide column is chosen instead of a long slender one is that the dimension of the model only varies within a much smaller range making the mesh size control easier and thus much fewer elements. A circular column is selected because the in-plane compliance of the 3-Arc-Fan interconnect is almost orientation independent. Since the compliance property of the 3-Arc-Fan interconnects is the fundamental reason why the substrate is mechanically decoupled from the board, the Young's modulus, Poisson's ratio and shear modulus of the equivalent column are to be derived according to the out-of-plane and in-plane compliance values of the original 3-Arc-Fan interconnect. In order to eliminate the Poisson's effect, it is reasonable to

assume that its Poisson's ratios in all directions are very small and equal to each other, $\nu = \nu_0 << 1$. Thus the out-of-plane (z-direction) compliance value of the column can be readily calculated as

$$C_{out-of-plane} = \frac{h}{E_z A} \quad (1)$$

where h is column height, A cross-sectional area and E_z the Young's modulus in z-direction. From equation (1), E_z can be obtained if $C_{out\text{-}of\text{-}plane}$ is given, and E_x, E_y are assumed to be equal to E_z for simplicity. As for the in-plane compliance, if y-direction is taken for example, the compliance value is only relevant to E_z and G_{yz} when $\nu << 1$. And the in-plane (y-direction) compliance value can be calculated as

$$C_{in-plane} = \frac{h^3}{3E_z \pi R^4} + \frac{37h}{32\pi G_{yz} R^2} \quad (2)$$

by using Energy Method, where G_{yz} is shear modulus in y-z plane and $\frac{32}{37}\pi G_{yz} R^2$ is shear stiffness for a circular column. From equation (2), G_{yz} can be obtained if $C_{in\text{-}plane}$ is given, and G_{xz} is equal to G_{yz}. G_{xy} is assumed to be equal to E_z for simplicity.

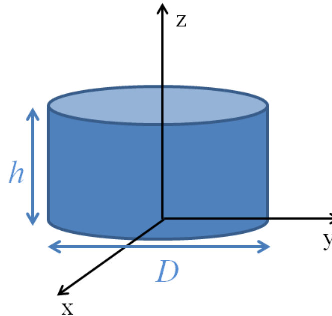


Figure 9-28 Equivalent orthotropic short column with its diameter equal to the interconnect footprint and its height equal to the interconnect stand-off

The out-of-plane and in-plane compliance values of the 3-Arc-Fan interconnects with different arcuate beam width values were shown in Table 9-7. By using equation (1) and (2), the Young's moduli and shear moduli of their corresponding equivalent columns were calculated and also shown in Table 9-7, if the stand-off is equal to 75μm and the diameter is equal to 280μm. However, choosing the stand-off or the column diameter is

not critical, because the Young's modulus and shear modulus will be calculated accordingly to make sure of the right compliance values in both directions. Therefore, an alternative method is to calculate *h* and *D* by pre-defining the Young's modulus and shear modulus.

Table 9-7 The out-of-plane and in-plane compliance values of 3-Arc-Fan interconnect with different arcuate beam width values, and the calculated Young's moduli and shear moduli of their corresponding equivalent columns

Arcuate Beam Width [μm]	$C_{out\text{-}of\text{-}plane}$ [mm/N]	$C_{in\text{-}plane}$ [mm/N]	Young's Modulus *E* [MPa]	Shear Modulus *G* [MPa]
10	5.52	2.13	0.221	0.879
15	2.97	0.70	0.410	3.386
20	2.31	0.36	0.527	10.131

By substituting these Young's modulus and shear modulus values into the simplified finite-element model, the compliance values are only off by 0.43% ~ 2.78%, as shown in Table 9-8. Figure 9-29 shows that the total element number of the pitch-size model reduced to 396 if the 3-Arc-Fan interconnect is replaced by this equivalent column. The number of elements is reduced by 1 order and none of them are badly shaped. Thus this equivalent column will be applied in the drop test simulation.

Table 9-8 Comparison of the compliance values between 3-Arc-Fan interconnects and corresponding equivalent columns

Arcuate Beam Width [μm]		$C_{out\text{-}of\text{-}plane}$ [mm/N]	$C_{in\text{-}plane}$ [mm/N]
10	3-Arc-Fan Interconnect	5.52	2.13
	Equivalent Column	5.56	2.10
	Relative Error	0.70%	1.41%
15	3-Arc-Fan Interconnect	2.97	0.70
	Equivalent Column	2.99	0.69
	Relative Error	0.67%	1.43%
20	3-Arc-Fan Interconnect	2.31	0.36
	Equivalent Column	2.32	0.35
	Relative Error	0.43%	2.78%

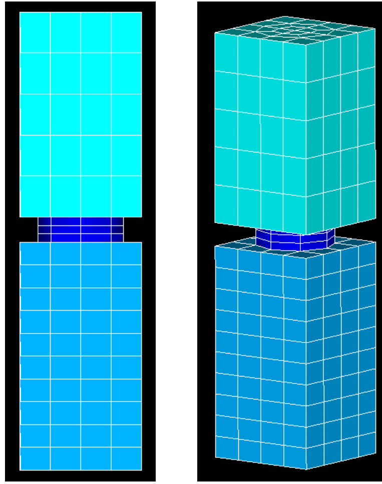


Figure 9-29 Mesh control for the pitch-size of the simplified model, including 396 elements in total with none of them badly shaped.

9.3.3. Simulation Results and Discussion

The Input-G method was selected to simulate the drop tests based on the simplified models discussed above. The finite-element simulations were carried out using the ANSYS® Implicit solver.

9.3.3.1. Natural Frequencies

The natural frequencies f_i (in Hz) were first calculated in ANSYS®, as shown in Table 9-9. It can be seen that the assembly with more compliant interconnection has lower natural frequencies. By comparing each natural frequency (each column in Table 9-9), the difference amongst is very small, this is because they use the same organic board which has much larger dimension than the rest of the assembly and contributes the most to the natural frequencies.

Table 9-9 First 12 natural frequencies (in Hz) having one quarter symmetry mode shapes for the assembly with different interconnection

	1	2	3	4	5	6
10µm	132.469	327.211	637.800	1034.62	1303.46	1571.21
15µm	132.752	327.521	642.574	1038.00	1307.10	1573.14
20µm	132.894	327.814	646.016	1040.03	1309.13	1574.28
Solder	136.326	333.545	711.810	1076.46	1345.67	1594.80
	7	**8**	**9**	**10**	**11**	**12**
10µm	2459.66	2904.91	3025.47	3482.25	3637.45	4212.60
15µm	2493.10	2935.02	3045.44	3508.89	3645.48	4318.95
20µm	2505.69	2943.85	3058.01	3517.30	3648.45	4343.35
Solder	2679.68	2998.00	3295.09	3616.39	3774.85	4526.12

9.3.3.2. Rayleigh Damping

Rayleigh damping was used in the ANSYS® finite-element models to capture the damping phenomenon in the drop tests. The modal damping factors ζ_i are related to the two Rayleigh damping coefficients, a and b, by

$$\varsigma_i = \frac{1}{2}\left(\frac{a}{\omega_i} + b\omega_i\right) \tag{3}$$

where ω_i is the circular natural frequency and $\omega_i = 2\pi f_i$. The modal damping factors are assumed to be the same for different modes, $\zeta_1 = \zeta_2 = \ldots = \zeta_N = \zeta$, and ζ can be calculated from the measured strain curves, Figure 9-7 to Figure 9-22, for different drop events. The modal damping factors are different among the ε_1, ε_2, ε_3 and ε_4 curves, because 1) the silicon substrate is mechanically decoupled from the organic board and they are of different material properties and dimensions; 2) the vibration characteristics in the longitudinal and transverse directions are different. However, the modal damping factors calculated from ε_1 curves were only used in the ANSYS® models, because ε_2, ε_3 and ε_4 curves exhibit a significant amount of noise.

The logarithmic decrement method was used to calculate the damping factors. The amplitude of motion u_P at the beginning of the first free vibration cycle and the amplitude u_Q at the end of the cycle were measured, shown in Figure 9-30. u_P and u_Q were

calculated from the average values of the three drop tests. The damping factor for small damping (ζ < 0.2) can be obtained from the following equation,

$$\varsigma = \frac{1}{2\pi} \ln \frac{u_P}{u_Q} \tag{4}$$

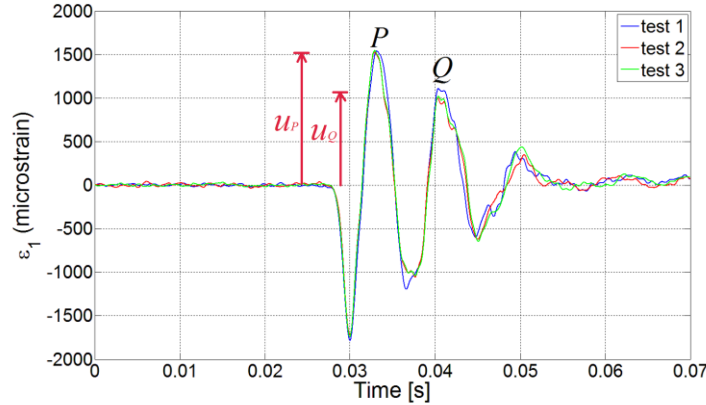


Figure 9-30 Decay record of ε_1 for drop tests of the sample with 10*μm* beam width 3-Arc-Fan compliant interconnect at drop height equal to 50*cm*

Then, the Rayleigh damping coefficients can be calculated by choosing two natural frequencies (1st and 2nd natural frequencies were used in this work) and using equation (3),

$$\varsigma = \frac{1}{2}\left(\frac{a}{\omega_1} + b\omega_1\right);\ \varsigma = \frac{1}{2}\left(\frac{a}{\omega_2} + b\omega_2\right) \tag{5}$$

where there are two equations solving for two unknowns *a* and *b*.

The damping factors and Rayleigh damping coefficients were calculated and shown in Table 9-10 through Table 9-13. And the Rayleigh damping coefficients will be used in the ANSYS® finite-element models.

Table 9-10 Damping factors and Rayleigh damping coefficients of the sample with 10μm beam width 3-Arc-Fan compliant interconnect at different drop height

Drop Height [cm]	20	30	40	50
ζ	0.15	0.12	0.07	0.06
a	179.18	137.90	85.60	73.00
b	1.05×10^{-4}	8.06×10^{-5}	5.00×10^{-5}	4.27×10^{-5}

Table 9-11 Damping factors and Rayleigh damping coefficients of the sample with 15μm beam width 3-Arc-Fan compliant interconnect at different drop height

Drop Height [cm]	20	30	40	50
ζ	0.22	0.17	0.07	0.05
a	261.14	199.12	82.29	60.28
b	1.52×10^{-4}	1.16×10^{-4}	4.79×10^{-5}	3.51×10^{-5}

Table 9-12 Damping factors and Rayleigh damping coefficients of the sample with 20μm beam width 3-Arc-Fan compliant interconnect at different drop height

Drop Height [cm]	20	30	40	50
ζ	0.27	0.09	0.08	0.07
a	314.97	111.19	98.89	82.51
b	1.83×10^{-4}	6.46×10^{-5}	5.75×10^{-5}	4.80×10^{-5}

Table 9-13 Damping factors and Rayleigh damping coefficients of the sample with solder ball interconnects at different drop height

Drop Height [cm]	20	30	40	50
ζ	0.14	0.16	0.14	0.14
a	169.05	193.51	165.85	167.73
b	9.42×10^{-5}	1.08×10^{-4}	9.24×10^{-5}	9.34×10^{-5}

9.3.3.3. Simulated Drop Response

Only one quarter of the structure was built in the ANSYS® models, due to the symmetry of the structure. The symmetric boundary conditions were applied as $u_x = 0$ along the edge $x = 0$ and $u_y = 0$ along the edge $y = 0$, shown in Figure 9-31. The displacement boundary conditions obtained from the double integral of the measured acceleration data were applied by using the Input-G method. The 3-Arc-Fan compliant interconnects were replaced by the equivalent short columns with the same in-plane and out-of-plane compliance values. The calculated Rayleigh coefficients were input in the ANSYS® model. The model used for simulation was created using SOLID185 elements and there were 179960 elements in total. The mesh size control for the finite-element model is shown in Figure 9-32.

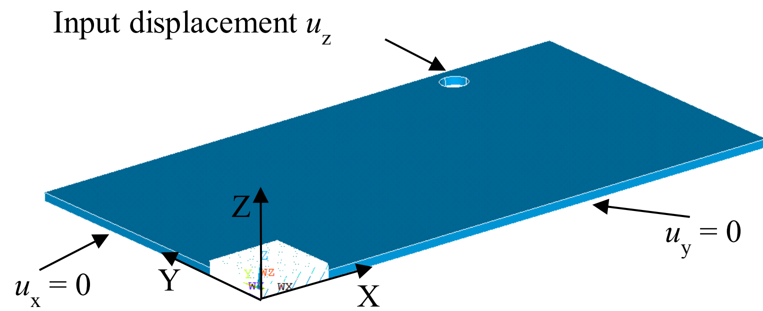


Figure 9-31 Applied boundary conditions in the ANSYS® finite-element model

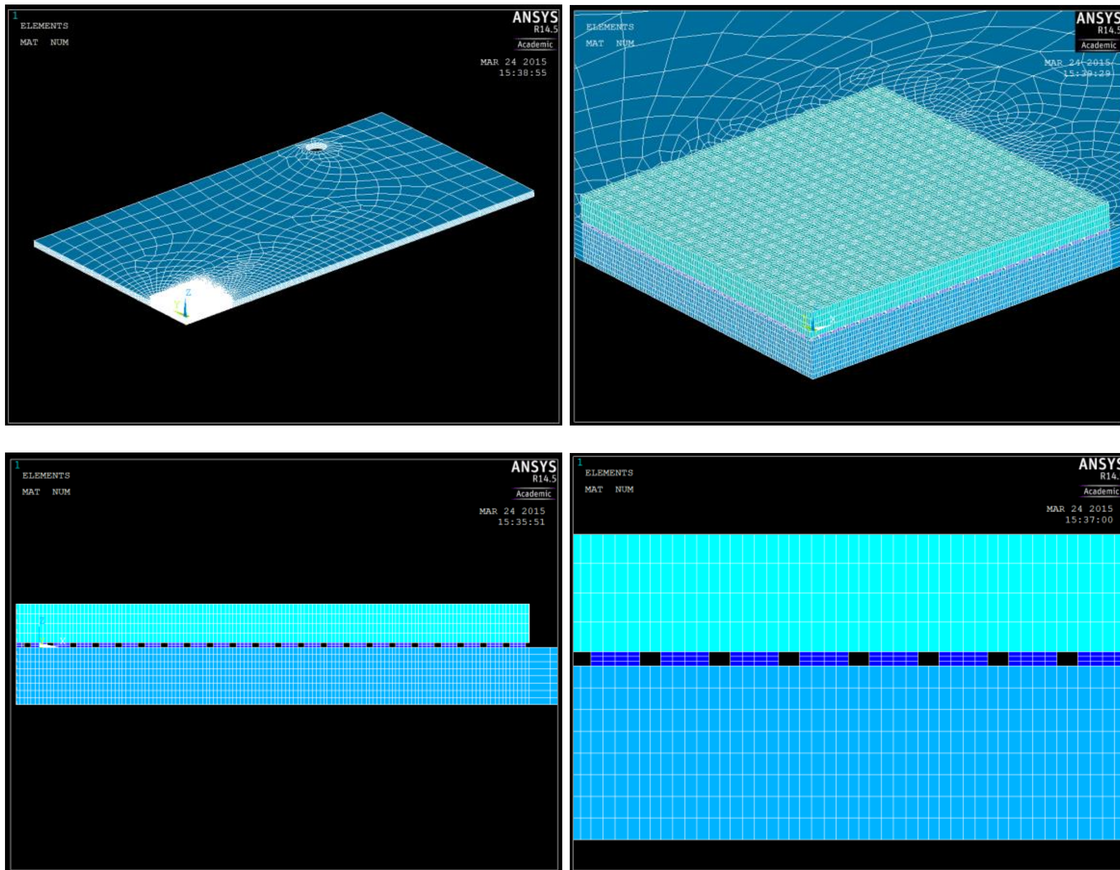


Figure 9-32 Mesh size control for the finite-element model (green: silicon substrate; dark blue: equivalent columns; light blue: organic FR-4 board)

The simulated peak microstrain values of ε_1 and ε_3 for drop tests of the samples with different interconnects at different drop heights, and the board-to-substrate strain ratios at the 1st and 2nd peaks are presented in Table 9-14 through Table 9-17. It can be seen that the simulations have similar strains on the substrate and the board as in

experiments, as well as similar strain ratios as in experiments. However, the simulations were not able to converge for the models using compliant interconnects with 10μm and 15μm arcuate beam width at 50cm drop height due to large deformation of interconnects.

Table 9-14 Simulated peak microstrain values of ε_1 and ε_3 for drop tests of the sample with 10μm beam width 3-Arc-Fan compliant interconnect at different drop heights, and the board-to-substrate strain ratio at the 1st and 2nd peaks

Drop Height [cm]	Average ε_1 [microstrain]		Average ε_3 [microstrain]		1st Peak Ratio	2nd Peak Ratio
	1st Peak	2nd Peak	1st Peak	2nd Peak		
20	-1090	720.0	50.90	-42.62	21.41	16.89
30	-1434	1026	64.85	-65.04	22.11	15.77
40	-1770	1289	77.49	-87.19	22.84	14.78
50	NA	NA	NA	NA	NA	NA
Average Board-to-Substrate Strain Ratio					22.12	15.81

Table 9-15 Simulated peak microstrain values of ε_1 and ε_3 for drop tests of the sample with 15μm beam width 3-Arc-Fan compliant interconnect at different drop heights, and the board-to-substrate strain ratio at the 1st and 2nd peaks

Drop Height [cm]	Average ε_1 [microstrain]		Average ε_3 [microstrain]		1st Peak Ratio	2nd Peak Ratio
	1st Peak	2nd Peak	1st Peak	2nd Peak		
20	-1018	482.5	80.31	-46.38	12.68	10.40
30	-1332	746.0	102.8	-76.83	12.96	9.71
40	-1664	1191	124.4	-139.5	13.38	8.54
50	NA	NA	NA	NA	NA	NA
Average Board-to-Substrate Strain Ratio					13.00	9.55

Table 9-16 Simulated peak microstrain values of ε_1 and ε_3 for drop tests of the sample with 20μm beam width 3-Arc-Fan compliant interconnect at different drop heights, and the board-to-substrate strain ratio at the 1st and 2nd peaks

Drop Height [cm]	Average ε_1 [microstrain]		Average ε_3 [microstrain]		1st Peak Ratio	2nd Peak Ratio
	1st Peak	2nd Peak	1st Peak	2nd Peak		
20	-974.7	434.2	84.50	-49.65	11.53	8.75
30	-1283	925.9	108.4	-131.1	11.84	7.06
40	-1588	1090	130.3	-169.2	12.19	6.44
50	-1874	1289	152.5	-218.2	12.29	5.91
Average Board-to-Substrate Strain Ratio					11.96	7.04

Table 9-17 Simulated peak microstrain values of ε_1 and ε_3 for drop tests of the sample with solder ball interconnects at different drop heights, and the board-to-substrate strain ratio at the 1st and 2nd peaks

Drop Height [cm]	Average ε_1 [microstrain]		Average ε_3 [microstrain]		1st Peak Ratio	2nd Peak Ratio
	1st Peak	2nd Peak	1st Peak	2nd Peak		
20	-497.5	349.0	210.0	-141.7	2.37	2.46
30	-652.0	425.1	275.4	-172.5	2.37	2.46
40	-795.9	536.3	332.4	-217.1	2.39	2.47
50	-929.5	614.9	387.3	-248.7	2.40	2.47
Average Board-to-Substrate Strain Ratio					2.38	2.47

Table 9-18 and Table 9-19 compare the board-to-substrate strain ratios obtained from both experiments and simulation. Both experiments and simulation show that the 3-Arc-Fan compliant interconnect have much greater board-to-substrate strain ratios than the solder ball interconnects, and that the more compliant the interconnect is, the higher the board-to-substrate strain ratio will be. The results obtained from the simulations based on the simplified model match the experimental data very well in terms both strain values and board-to-substrate strain ratios. The discrepancy is mainly due to the finite-element models that simplified the compliant interconnects as the equivalent orthotropic columns and the uncertainty of the drop tests.

Table 9-18 Board-to-substrate strain ratios at the 1st peak for compliant interconnects with different arcuate beam width values and solder ball interconnect

Different interconnects		Board-to-substrate strain ratio	
		Experiment	Simulation
Compliant	10µm 3-Arc-Fan	23.13	22.12
↓	15µm 3-Arc-Fan	15.10	13.00
↓	20µm 3-Arc-Fan	10.23	11.96
Stiff	Solder Ball	2.29	2.38

Table 9-19 Board-to-substrate strain ratios at the 2nd peak for compliant interconnects with different arcuate beam width values and solder ball interconnect

Different interconnects		Board-to-substrate strain ratio	
		Experiment	Simulation
Compliant	10µm 3-Arc-Fan	21.55	15.81
↓	15µm 3-Arc-Fan	9.53	9.55
↓	20µm 3-Arc-Fan	7.01	7.04
Stiff	Solder Ball	2.46	2.47

The reported results show that the area-array of 3-Arc-Fan compliant interconnects can be used as effective impact isolator.

9.4. CONCLUSION

In this chapter, 3-Arc-Fan compliant interconnects were drop-tested for heights ranging from 20cm to 50cm. Three different interconnect arcuate beam widths, namely 10 um, 15 um, and 20 um, were tested. In all tests and simulations, it is seen that the interconnects are able to isolate the strain transfer from the board to the substrate. The board-to-substrate strain ratio could be as high as 22.12. It is seen through this work that as the compliance increases, the isolation effect also increases, and thus the strain isolation also increases. In contrast, solder interconnects, used in common microsystem applications, are not able to isolate the substrate from the board, and the board-to-substrate strain ratio is less than 2.5 indicating the extremely low compliance of solder interconnects. Thus, an area-array of 3-arc fan compliant interconnects, in addition to serving as electrical interconnects, can also be effectively pursued as a mechanical drop-impact isolator for microelectronic and MEMS applications.

CHAPTER 10 RELIABILITY ASSESSMENT UNDER DROP TEST

10.1. INTRODUCTION

The handheld electronic products like mobile phones, wearable devices, cameras, calculators and other electronic products are getting more and more popular in the market. They can be easily stored in the pockets and carried with the users. These portable electronic products are usually small in size and light in weight, and are subjected to drops during normal use. The impact force from the drops will not only causes the mechanical failure of the components but also create failures of the interconnects between the substrate and the board. Therefore, the reliability assessment of the 3-Arc-Fan compliant interconnects under the board level drop test is very important for the application in the handheld electronic products.

The primary reason for the failure of the 3-Arc-Fan compliant interconnect and other types of interconnects under the drop tests is the flexure of the board causing the relative motion between the board and the substrate, which further results in the deformation of the interconnects sandwiched in-between. The other important reason for the failure of the interconnects is due to the inertial effects of the components/substrate mounted on the board. The inertial force upon the impact during the drop test will pull the interconnects and cause the permanent deformation or crack within the interconnects.

The failure of the 3-Arc-Fan compliant interconnect is a strong function of the structural design variables, e.g. *arcuate beam width*, *arcuate beam thickness*, *copper pad diameter* and *standoff height*, as well as interconnect material. In this chapter, the reliability of the 3-Arc-Fan compliant interconnects with different arcuate beam width values (10μm, 15μm and 20μm) under drop tests is evaluated and compared.

10.2. EXPERIMENTAL DROP TESTING

10.2.1. Experimental Setup

The experimental setup is the similar to the one in the previous chapter discussing the impact isolation. Copper compliant interconnects were fabricated on silicon wafers at pitch value equal to 400μm, through sequential cleanroom fabrication processes. The silicon wafer was diced into 18mm × 18mm × 0.675mm silicon substrates which were assembled on organic FR-4boards (132mm × 77mm × 1mm) through solder reflow, as discussed in Chapter 9. The overall design was based on the JEDEC standard for board-level drop test reliability. Such samples can then be subjected to drop testing. The Instron Dynatup® 8250 drop weight impact tester was used to conduct the drop tests as shown in Figure 9-2.

Instead of measuring the strain values and the acceleration, all the samples used for the drop testing were daisy-chained, as shown in Figure 10-1. The four daisy chains measuring the resistance at the four corners which are the most critical locations were labeled as A, B,C and D. Each daisy chain at the corner includes 4×4 compliant interconnects. The resistance of the four daisy chains measuring the compliant interconnects at the four corners was monitored and logged after certain (one or more) drop tests.

Figure 10-1 Left: daisy chain patterns on the organic board to be assembled; right: drop test sample with the four daisy chains measuring the resistance at the four corners which are the most critical locations (each corner includes 4×4 compliant interconnects)

However, several of the compliant interconnects might be broken or missed during the fabrication or assembly process, so sometimes the daisy chain might indicate an open loop. The other daisy chains measuring the resistance inside the sample were used to make sure that the sample was properly assembled.

All of the samples tested were dropped at the height equal to 30cm and the acceleration data is shown in Figure 10-2. The peak acceleration is 1791m/s and the impact time is 3 to 4ms.

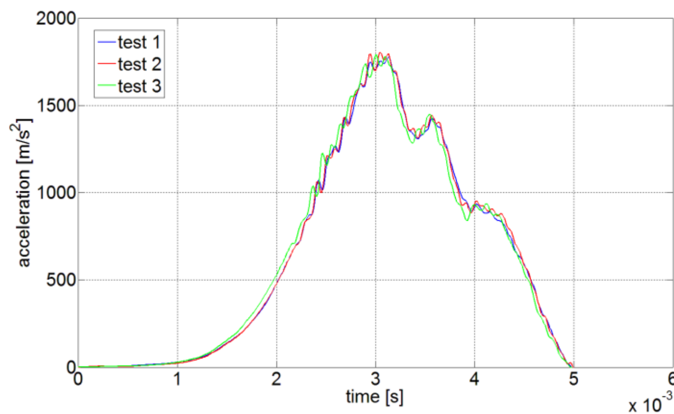


Figure 10-2 Acceleration magnitude plots for drop tests at drop height equal to 30cm

10.2.2. Measured Daisy-Chain Resistance

The drop tests were carried out for the samples assembled using the 3-Arc-Fan compliant interconnects with the arcuate beam width equal to 10µm, 15µm and 20µm, which were actually 9.5µm, 14.5µm and 19.5µm respectively after the etching process.

10.2.2.1. <u>Arcuate Beam Width Equal to 10µm</u>

The change of daisy-chain resistance values over the drop tests for the samples with 3-Arc-Fan interconnect beam width equal to 10µm were measured and recorded in Figure 10-3 and Figure 10-4. The daisy-chain resistance consists of the resistance of the compliant interconnects and the resistance of the copper traces in the daisy-chain pattern. As discussed before that it is not uncommon that several of the compliant interconnect might be missed or broken during the fabrication or assembly process and some of the

daisy chains may show open loops even before the drop tests, e.g., Daisy-Chain C in Sample 1 and Daisy-Chain B in Sample 2.

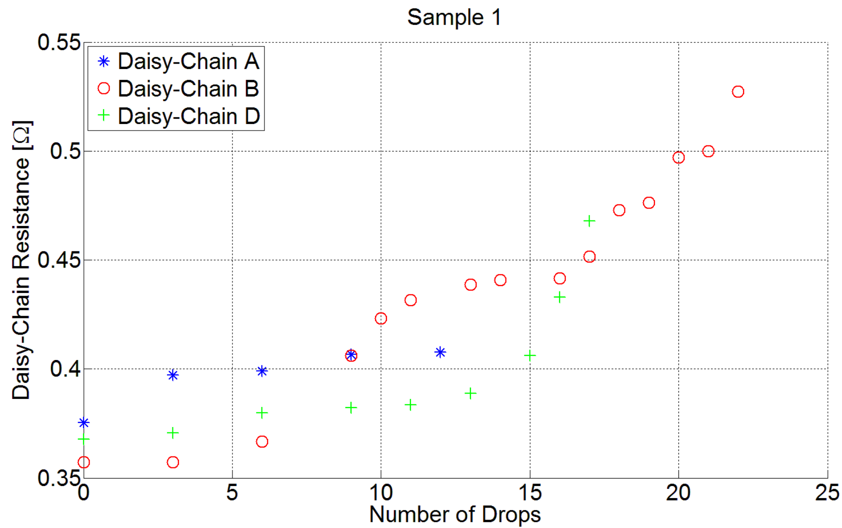


Figure 10-3 Change of daisy-chain resistance over the drop tests for sample 1 with 3-Arc-Fan interconnect beam width equal to 10μm

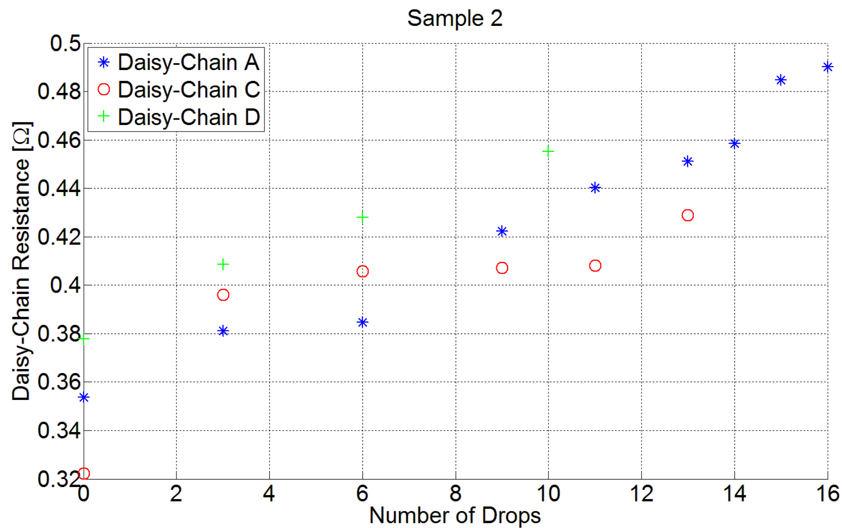


Figure 10-4 Change of daisy-chain resistance over the drop tests for sample 2 with 3-Arc-Fan interconnect beam width equal to 10μm

The gradually and monotonically increased daisy chain resistance represents the breakage of the arcuate beams of compliant interconnects during the drop tests. The resistance does not jump to a huge value unless all the three arcuate beams in the same 3-

Arc-Fan compliant interconnect break, which indicates the failure at that particular corner of the sample.

The average resistance of all the daisy chains before the drop tests was 0.359Ω and the average resistance of all the daisy chains right before the failure is 0.463Ω. The resistance increases about 29% after the samples failed. Table 10-1 shows the number of drops survived for the daisy chains measuring the 4×4 compliant interconnects at the corner of the samples with 3-Arc-Fan interconnect beam width equal to 10μm, and the average number of drops survived is about 15.

Table 10-1 Number of drops survived for the daisy chains measuring the 4×4 compliant interconnects at the corner of the samples with 3-Arc-Fan interconnect beam width equal to 10μm

	Sample 1			Sample 2		
Daisy-Chain	A	B	D	A	C	D
Resistance before Tests [mΩ]	375	357	368	354	322	378
Resistance before Failure [mΩ]	408	527	468	490	429	455
# of Drops Survived	12	22	17	16	13	10
Average # of Drops Survived = 15						

10.2.2.2. Arcuate Beam Width Equal to 15μm

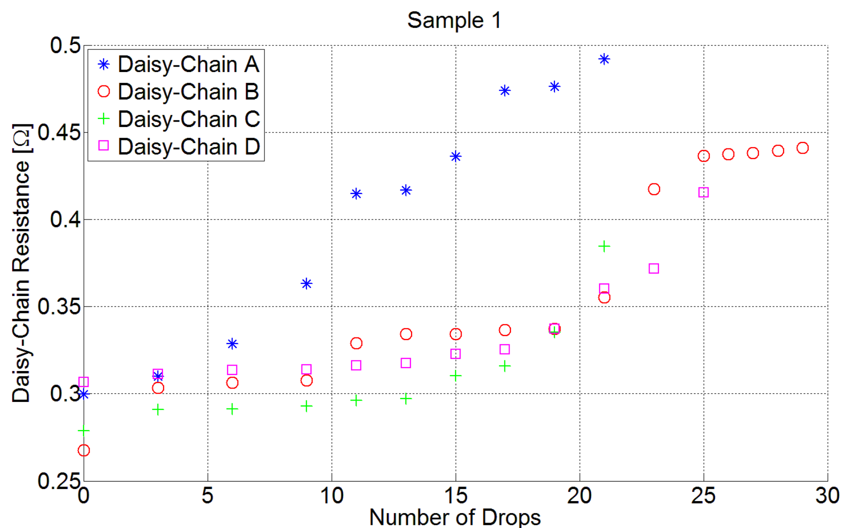


Figure 10-5 Change of daisy-chain resistance over the drop tests for sample 1 with 3-Arc-Fan interconnect beam width equal to 15μm

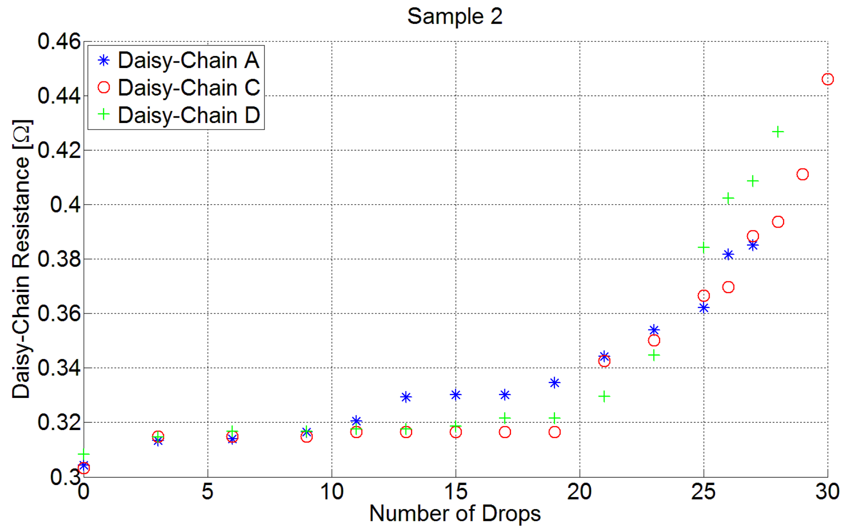


Figure 10-6 Change of daisy-chain resistance over the drop tests for sample 2 with 3-Arc-Fan interconnect beam width equal to 15μm (Daisy-chain B indicated an open loop due to one missing interconnect)

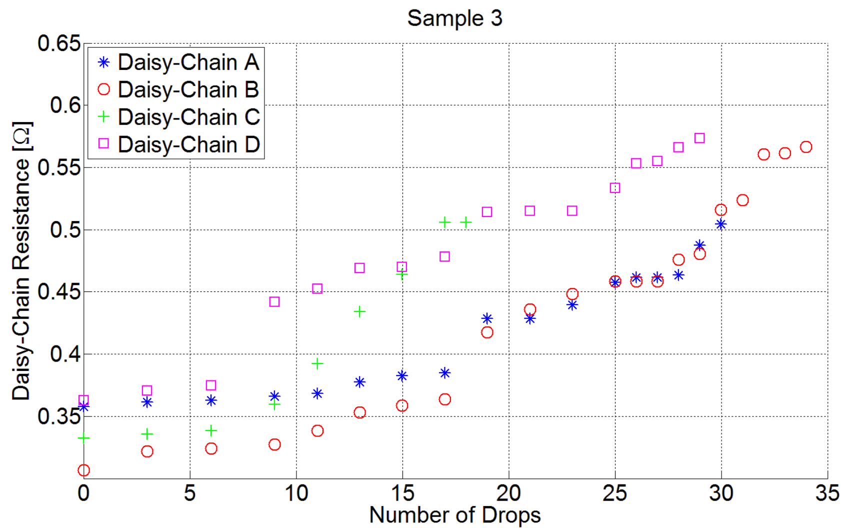


Figure 10-7 Change of daisy-chain resistance over the drop tests for sample 3 with 3-Arc-Fan interconnect beam width equal to 15μm (Daisy-Chain C failed in the early stage due to the assembly imperfection)

It is important to point out that Daisy-Chain C in Sample 3 failed after 18 drops is due to the assembly imperfection. One of the compliant interconnects detached from the board. The X-ray inspection also showed that none of the interconnects failed (breakage

of all three arcuate beams in the same compliant interconnect) after 18 drops. Therefore this data was not used as the reliability assessment.

The average resistance of all the daisy chains before the drop tests was 0.310Ω and the average resistance of all the daisy chains right before the failure is 0.463 Ω. The resistance increases about 50% after the samples failed. Table 10-2 shows the number of drops survived for the daisy chains measuring the 4×4 compliant interconnects at the corner of the samples with 3-Arc-Fan interconnect beam width equal to 15µm, and the average number of drops survived is about 27.

Table 10-2 Number of drops survived for the daisy chains measuring the 4×4 compliant interconnects at the corner of the samples with 3-Arc-Fan interconnect beam width equal to 15µm

	Sample 1				**Sample 2**			**Sample 3**			
Daisy-Chain	A	B	C	D	A	C	D	A	B	C	D
R before Tests [mΩ]	300	268	279	307	304	303	308	358	307	333	363
R before Failure [mΩ]	492	441	385	416	385	446	427	505	567	506	574
# of Drops Survived	21	29	21	25	27	30	28	30	34	NA	29
Average # of Drops Survived ≈ 27											

10.2.2.3. Arcuate Beam Width Equal to 20µm

The change of daisy-chain resistance values over the drop tests for the samples with 3-Arc-Fan interconnect beam width equal to 20µm were measured and recorded in Figure 10-8, Figure 10-9 and Figure 10-10, respectively. As discussed before that it is not uncommon that several of the compliant interconnect might be missed or broken during the fabrication or assembly process and some of the daisy chains may show open loops even before the drop tests.

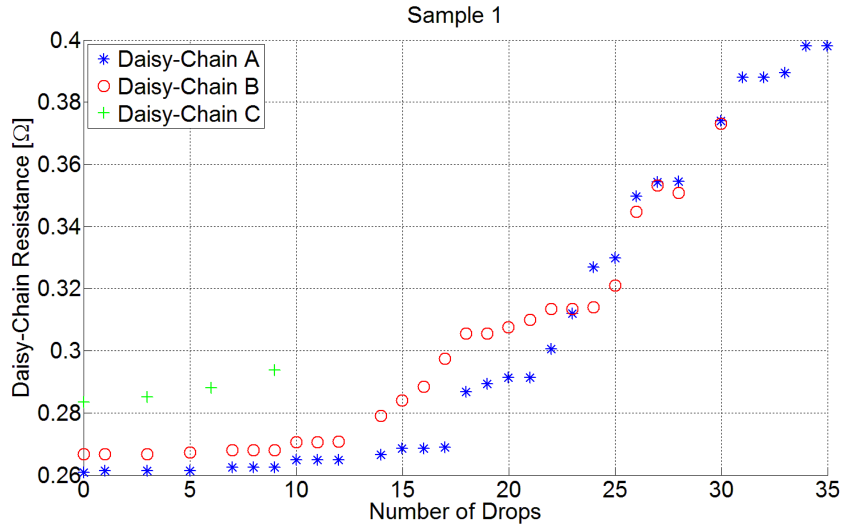


Figure 10-8 Change of daisy-chain resistance over the drop tests for sample 1 with 3-Arc-Fan interconnect beam width equal to 20μm (Daisy-chain D indicated an open loop due to one missing interconnect and Daisy-Chain C failed in the early stage due to the assembly imperfection)

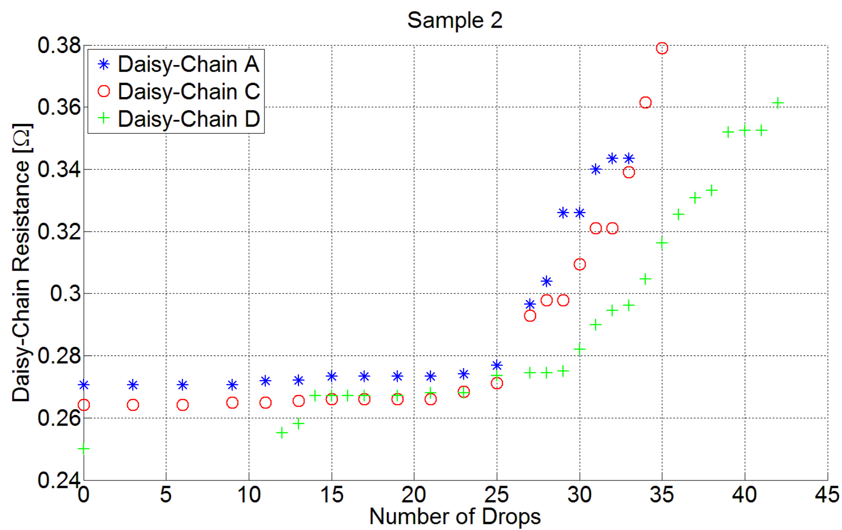


Figure 10-9 Change of daisy-chain resistance over the drop tests for sample 2 with 3-Arc-Fan interconnect beam width equal to 20μm (Daisy-chain B indicated an open loop due to one missing interconnect)

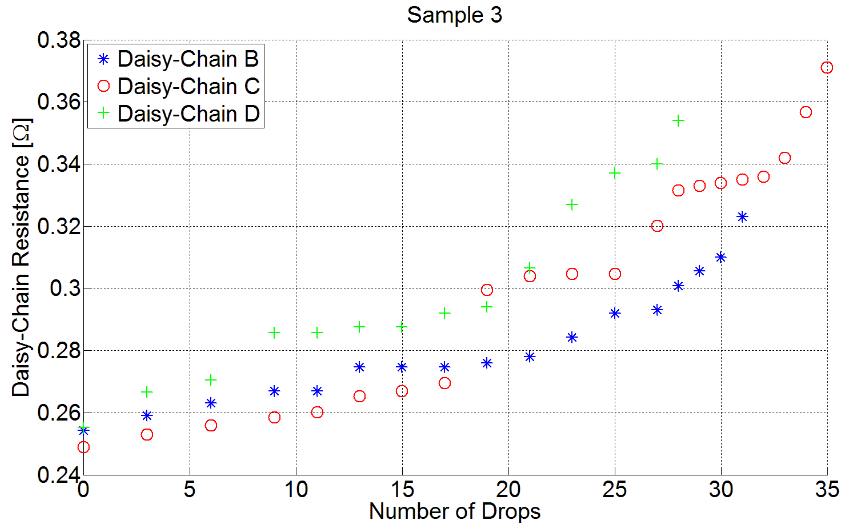


Figure 10-10 Change of daisy-chain resistance over the drop tests for sample 3 with 3-Arc-Fan interconnect beam width equal to 20μm (Daisy-chain A indicated an open loop due to one missing interconnect)

Daisy-Chain C in sample 3 failed after 9 drops which is due to the assembly imperfection and this data was not used as the reliability assessment.

The average resistance of all the daisy chains before the drop tests was 0.262Ω and the average resistance of all the daisy chains right before the failure is 0.355Ω. The resistance increases about 36% after the samples failed. Table 10-3 shows the number of drops survived for the daisy chains measuring the 4×4 compliant interconnects at the corner of the samples with 3-Arc-Fan interconnect beam width equal to 20μm, and the average number of drops survived is about 34.

Table 10-3 Number of drops survived for the daisy chains measuring the 4×4 compliant interconnects at the corner of the samples with 3-Arc-Fan interconnect beam width equal to 20μm

	Sample 1			Sample 2			Sample 3		
Daisy-Chain	A	B	C	A	C	D	B	C	D
R before Tests [mΩ]	261	267	284	271	264	250	254	249	255
R before Failure [mΩ]	398	373	294	344	379	361	323	371	354
# of Drops Survived	35	30	NA	33	35	42	31	35	28
Average # of Drops Survived ≈ 34									

10.3. CONCLUSION

As stated before that the primary reason for the failure of the 3-Arc-Fan compliant interconnect under the drop tests is the flexure of the board causing the relative motion between the board and the substrate, which further results in the deformation of the interconnects sandwiched in-between. So the outer compliant interconnects have larger deformation than the inner compliant interconnects, as shown in Figure 10-11. The compliant interconnects located at the four corners had the largest deformation during the drop test, and failed the earliest, as shown in Figure 10-12 and Figure 10-13.

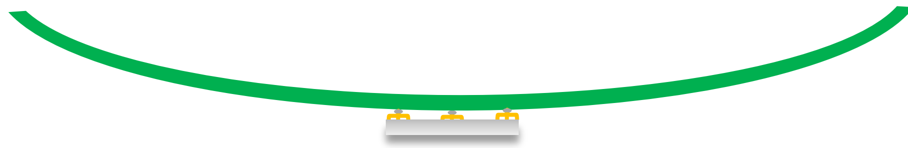


Figure 10-11 Flexure of the board causing the relative motion between the board and the substrate

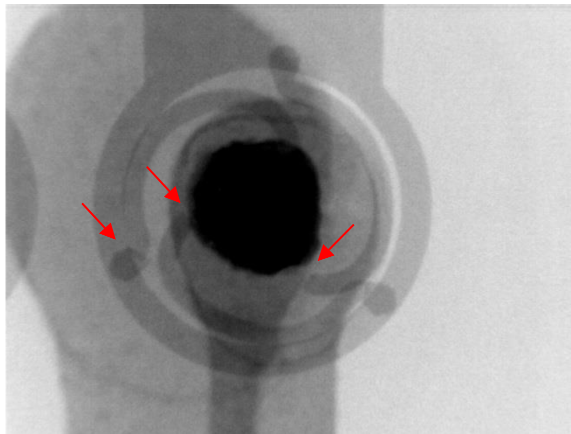


Figure 10-12 X-ray image of the failure of the compliant interconnect located at the corner

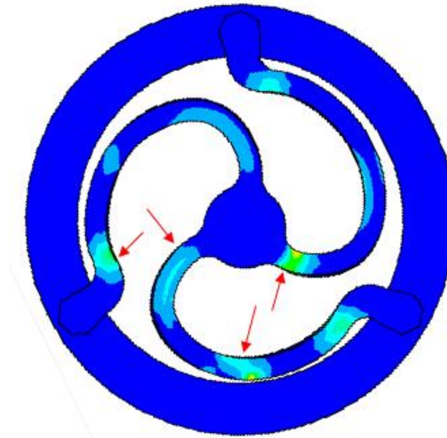


Figure 10-13 Critical locations predicted by finite-element simulation using ANSYS®

Table 10-4 compares the number of drops survived under the drop tests with prescribed input acceleration for the 3-Arc-Fan compliant interconnects with different arcuate beam width. It can be seen that the 3-Arc-Fan compliant interconnect with larger beam width is more reliable under the drop-impact loads. This is because the compliant interconnect with larger beam width is less compliant leading to less relative motion between the board and the substrate, and therefore less deformation of the compliant interconnect itself.

Table 10-4 Comparison of the number of drops survived under the drop tests for the 3-Arc-Fan compliant interconnects with different arcuate beam width

3-Arc-Fan compliant interconnect beam width	Average number of drops survived
10μm	15
15μm	27
20μm	34

CHAPTER 11 SUMMARY AND RESEARCH CONTRIBUTIONS

11.1. SUMMARY

Some of the main compliant interconnects that are being pursued in universities and industry were reviewed and the strengths and weaknesses associated with them were discussed. It can be seen that any geometry improvement that enhances the mechanical compliance will also adversely affect the electrical performance. The 3-Arc-Fan compliant interconnect with multiple electrical paths studied in this research can increase the mechanical compliance but also provide relatively good electrical characteristics.

The compliance values of the 3-Arc-Fan compliant interconnect were calculated using analytical solutions based on Euler-Bernoulli beam assumptions and Castigliano's second theorem, as well as finite-element simulations using both simplified beam model and full 3D solid model. The analytical solutions and the simulation results were compared against and validated by the experimental data. The analytical solutions match the simulation and experimental results very well, and give an insight into how the geometry parameters affect the compliance values.

A multi-objective design optimization of 3-Arc-Fan compliant interconnect was carried out. By eliminating the post from the original design, using Surface Evolver and normalizing the other design parameters by the footprint, the total number of design variables was reduced from 8 to 4. The response surfaces were constructed for inductance, resistance and the von Mises strains based on CCI simulation points. To construct the response surfaces, 25 simulations were done for the inductance and resistance and 15 simulations were done for determining von Mises strain under in-plane and out-of-plane loading conditions, and no further simulations are needed which significantly reduces the computational time for the optimization process. The method of global criterion was used to construct a single-objective. The methodology, presented in this research can be applied for the design of other compliant interconnects.

An area-array of 3-Arc-Fan compliant interconnects were fabricated on a 6-inch silicon wafer using sequential processes. The compliant interconnects with arcuate beam width equal to 10μm, 15μm, and 20μm were fabricated simultaneously in the same wafer. The use of the dry-film photoresist makes the fabrication process cost effective compared to the use of liquid film photoresist by involving less fabrication steps, having higher fabrication reliability and finishing in Class 1000 cleanroom. The out-of-plane mechanical compliance were measured to be 5.52mm/N, 2.97mm/N and 2.31mm/N, and the electrical resistance were measured to be 12.47mΩ, 8.43mΩ and 6.13mΩ, respectively for the compliant interconnects with arcuate beam width equal to 10μm, 15μm, and 20μm. A reliable easy-to-assemble method was introduced to assemble the silicon substrates with fabricated area-array of compliant interconnects onto the organic boards.

The assemblies were tested under the thermal cycling loads. The results show that the samples can survive several hundred cycles under the JEDEC standard (JESD22-A104D) test condition G and when a thick silicon substrate or combined die stack was presented. The compliant interconnect with arcuate beam width equal to 10μm has the best reliability, followed by the 15μm and then 20μm designs. It also shows that the more compliant the interconnect is the less it is sensitive to the substrate thickness and the board thickness when the assembly is under the thermal cycling loads.

Experimental drop testing and the finite-element simulations using Input-G method for the scaled-up polymer compliant interconnect prototype as well as the true samples with micro scale copper interconnects were carried out. It is shown that the strains in the board were found to be much lower than the corresponding strains transferred to the substrate strains. The simulated results agreed very well with the experiment for the strains observed in both the substrate and board. The reported results show that the area-array of 3-Arc-Fan compliant interconnects could be used as effective impact isolator.

The reliability of the 3-Arc-Fan compliant interconnects under the board level drop tests were studied. It can be seen that all the compliant interconnects with different arcuate beam width can survive after tens of drop events under certain input acceleration. And the compliant interconnect with arcuate beam width equal to 20μm has the best reliability, followed by the 15μm and then 10μm designs.

11.2. RESEARCH CONTRIBUTIONS

This work is the first published work to examine the design, fabrication, and reliability of a multi-path second-level interconnect under thermo-mechanical as well as drop-impact loading conditions, and to develop an optimized design through a systematic approach. In particular,

- This work has developed second-level compliant interconnects by performing compliance analysis and systematic multi-physics design optimization.
- This work has developed a general-purpose analytical solution to determine the compliance of the 3-Arc-Fan compliant interconnect and to validate the results from the analytical solution against numerical simulations and experimental data.
- This work has employed a multi-objective and multi-physics optimization design methodology for the 3-Arc-Fan compliant interconnect based on the Response Surfaces, Method of Global Criterion and footprint normalization, which is applicable to a wide range of other compliant interconnects.
- This work has developed a unique fabrication and assembly process of an area-array of 3-Arc-Fan compliant interconnects on a silicon wafer using dry-film photoresist. The use of the dry-film photoresist makes the fabrication process cost effective and more reliable compared to the use of liquid film photoresist.

- This work has studied the thermo-mechanical as well as drop-impact reliability of 3-Arc-Fan compliant interconnect prototypes through experiments and computer simulations.
- This work has demonstrated that the area-array of 3-Arc-Fan compliant interconnects can be used as effective impact isolator

11.3. FUTURE WORK

- Although a number of samples have been fabricated, assembled and tested to demonstrate the viability of 3-Arc-Fan compliant interconnects, more prototypes need to be fabricated, assembled and tested for the statistical analyses. Drop testing and thermal cycling testing at different conditions can be done.
- Although some electrical characterizations have been done, more need to be done at high frequency
- Copper oxidation affects the compliance and the reliability of the copper microstructure compliant interconnect, and elastomer that encapsulates and protects 3-Arc-Fan compliant interconnects may be pursued as an underfill material.
- This works has assessed the reliability of the compliant interconnects under thermal cycling and drop-impact conditions. The assessment of the long term reliability of the compliant interconnects in the realistic products is another important research topic.
- The plating current density, annealing temperature and interconnect dimensions will influence the copper microstructure and the interconnect reliability, such process parameters need to be systematically studied.

REFERENCES

[1] G. E. Moore, "Cramming more components onto integrated circuits," *Proceedings of the IEEE,* vol. 86, pp. 82-85, 1998.

[2] R. R. Tummala, "2.5D Interposers; Organics vs. Silicon vs. Glass," *ChipScaleReview,* vol. 13, pp. 18-19, July-August 2013.

[3] M. Hogan, "Silicon interposers: building blocks for 3 D-ICs," *Solid State Technology,* vol. 54, pp. 18-19, 2011.

[4] R. R. Tummala, "Fundamentals of microsystems packaging," ed: New York: McGraw-Hill, 2001.

[5] J. H. Lau, "Overview and outlook of through-silicon via (TSV) and 3D integrations," *Microelectronics International,* vol. 28, pp. 8-22, 2011.

[6] S. K. Lim, *Design for High Performance, Low Power, and Reliable 3D Integrated Circuits*: Springer Science & Business Media, 2012.

[7] J. U. Knickerbocker, P. S. Andry, B. Dang, R. R. Horton, M. J. Interrante, C. S. Patel*, et al.*, "Three-dimensional silicon integration," *IBM Journal of Research and Development,* vol. 52, pp. 553-569, 2008.

[8] D. C. Sekar and Z. Or-Bach, "Monolithic 3D-ICs with single crystal silicon layers," in *3DIC*, 2011, pp. 1-2.

[9] K. Saitoh and R. Shoji, "Bump structure, bump forming method and package connecting body," 2001.

[10] F. Tung, "Pillar connections for semiconductor chips and method of manufacture," 2003.

[11] T. Wang, F. Tung, L. Foo, and V. Dutta, "Studies on a novel flip-chip interconnect structure. Pillar bump," in *Electronic Components and Technology Conference, 2001. Proceedings., 51st*, 2001, pp. 945-949.

[12] V. M. Dubin, S. Balakrishnan, and M. Bohr, "Designs and methods for conductive bumps," 2007.

[13] W. Koh, B. Lin, and J. Tai, "Copper pillar bump technology progress overview," in *Electronic Packaging Technology and High Density Packaging (ICEPT-HDP), 2011 12th International Conference on*, 2011, pp. 1-5.

[14] J. B. Kwak and S. Chung, "Thermal fatigue reliability for Cu-Pillar bump interconnection in flip chip on module and underfill effects," *Soldering & Surface Mount Technology,* vol. 27, pp. 1-6, 2015.

[15] X. Qin, S. Gottschall, N. Kumbhat, P. M. Raj, S. Kim, V. Sundaram*, et al.*, "Large silicon, glass and low CTE organic interposers to printed wiring board SMT interconnections using copper microwire arrays," in *Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd*, 2013, pp. 867-871.

[16] J. Li, Q. Ye, A. Cassell, J. Koehne, H. Ng, J. Han*, et al.*, "Carbon nanotube interconnects: A process solution," in *Interconnect Technology Conference, 2003. Proceedings of the IEEE 2003 International*, 2003, pp. 271-272.

[17] A. Naeemi and J. D. Meindl, "Carbon nanotube interconnects," in *Proceedings of the 2007 international symposium on Physical design*, 2007, pp. 77-84.

[18] S. Lee, B.-J. Lee, and P.-K. Shin, "Carbon nanotube interconnection and its electrical properties for semiconductor applications," *Japanese Journal of Applied Physics,* vol. 48, p. 125006, 2009.

[19] N. J. Ginga, "On-chip dielectric cohesive fracture characterization and mitigation investigation through off-chip carbon nanotube interconnects," Georgia Institute of Technology, 2014.
[20] N. J. Ginga, W. Chen, and S. K. Sitaraman, "Waviness reduces effective modulus of carbon nanotube forests by several orders of magnitude," *Carbon,* vol. 66, pp. 57-66, 2014.
[21] A. Ibanez and E. Fatas, "Mechanical and structural properties of electrodeposited copper and their relation with the electrodeposition parameters," *Surface and Coatings Technology,* vol. 191, pp. 7-16, 2005.
[22] J. Xu, K. M. Razeeb, S. K. Sitaraman, and A. Mathewson, "The fabrication of ultra long metal nanowire bumps and their application as interconnects," in *Nanotechnology (IEEE-NANO), 2012 12th IEEE Conference on*, 2012, pp. 1-6.
[23] J. Chow and S. K. Sitaraman, "Overplated Electroplated Nanowires as Electrical Interconnections," in *Poster session presented at: International Mechanical Engineering Congress & Exposition*, Montreal, Canada, 2014.
[24] E. Liao, A. A. Tay, S. S. Ang, H. Feng, R. Nagarajan, and V. Kripesh, "Fatigue and bridging study of high-aspect-ratio multicopper-column flip-chip interconnects through solder joint shape modeling," *Components and Packaging Technologies, IEEE Transactions on,* vol. 29, pp. 560-569, 2006.
[25] B. Cheng, E. Chow, D. DeBruyker, C. Chua, K. Sahasrabuddhe, I. Shubin*, et al.*, "Microspring Characterization and Flip Chip Assembly Reliability," *42th International Microelectronics and Packaging Society (IMAPS),* 2009.
[26] L. Ma, Q. Zhu, T. Hantschel, D. K. Fork, and S. K. Sitaraman, "J-Springs-Innovative compliant interconnects for next-generation packaging," in *Electronic Components and Technology Conference, 2002. Proceedings. 52nd*, 2002, pp. 1359-1365.
[27] L. Ma, S. K. Sitaraman, Q. Zhu, K. Klein, and D. Fork, *Design and Development of Stress-Engineered Compliant Interconnect for Microelectronic Packaging*: Springer, 2008.
[28] P. Arunasalam, H. D. Ackler, and B. G. Sammakia, "Design, fabrication and implementation of smart three axis compliant interconnects for ultra-thin chip stacking technology," in *Electronic Components and Technology Conference, 2006. Proceedings. 56th*, p. 7 pp.
[29] V. Solberg, D. Light, and J. Fjelstad, "Reliable and low cost wafer level packaging. Process description and qualification testing results for wide area vertical expansion (WAVE TM) package technology," in *Electronics Manufacturing Technology Symposium, 2000. Twenty-Sixth IEEE/CPMT International*, 2000, pp. 108-114.
[30] Y. G. Kim, I. Mohammed, B. S. Seol, and T. G. Kang, "Wide area vertical expansion (WAVE^{TM}) package design for high speed application: reliability and performance," in *Electronic Components and Technology Conference, 2001. Proceedings., 51st*, 2001, pp. 54-62.
[31] D. Li, D. Light, D. Castillo, M. Beroz, M. Nguyen, and T. Wang, "A Wide Area Vertical Expansion (WAVE TM) packaging process development," in *Electronic Components and Technology Conference, 2001. Proceedings., 51st*, 2001, pp. 367-371.

[32] M. S. Bakir, H. A. Reed, P. A. Kohl, K. P. Martin, and J. D. Meindl, "Sea of leads ultra high-density compliant wafer-level packaging technology," in *Electronic Components and Technology Conference, 2002. Proceedings. 52nd*, 2002, pp. 1087-1094.

[33] B. Dang, M. S. Bakir, C. S. Patel, H. D. Thacker, and J. D. Meindl, "Sea-of-leads MEMS I/O interconnects for low-k IC packaging," *Microelectromechanical Systems, Journal of,* vol. 15, pp. 523-530, 2006.

[34] J. Novitsky and D. Pedersen, "FormFactor introduces an integrated process for wafer-level packaging, burn-in test, and module level assembly," in *Advanced Packaging Materials: Processes, Properties and Interfaces, 1999. Proceedings. International Symposium on*, 1999, pp. 226-231.

[35] S. Strickland, J. Hester, A. Gowan, R. Montgomery, D. Geist, J. Blanche*, et al.*, "Microcoil spring interconnects for ceramic grid array integrated circuits," 2011.

[36] Q. Zhu, L. Ma, and S. K. Sitaraman, "Development of G-Helix structure as off-chip interconnect," *TRANSACTIONS-AMERICAN SOCIETY OF MECHANICAL ENGINEERS JOURNAL OF ELECTRONIC PACKAGING,* vol. 126, pp. 237-246, 2004.

[37] Q. Zhu, L. Ma, and S. K. Sitaraman, "β-Helix: a lithography-based compliant off-chip interconnect," *Components and Packaging Technologies, IEEE Transactions on,* vol. 26, pp. 582-590, 2003.

[38] K. Kacker, T. Sokol, and S. K. Sitaraman, "FlexConnects: a cost-effective implementation of compliant chip-to-substrate interconnects," in *Electronic Components and Technology Conference, 2007. ECTC'07. Proceedings. 57th*, 2007, pp. 1678-1684.

[39] K. Kacker and S. K. Sitaraman, "Electrical/mechanical modeling, reliability assessment, and fabrication of flexconnects: A MEMS-based compliant chip-to-substrate interconnect," *Microelectromechanical Systems, Journal of,* vol. 18, pp. 322-331, 2009.

[40] R. E. Lee, R. Okereke, and S. K. Sitaraman, "Multi-path fan-shaped compliant off-chip interconnects," in *Electronic Components and Technology Conference (ECTC), 2011 IEEE 61st*, 2011, pp. 2141-2145.

[41] K. A. Brakke, "The surface evolver," *Experimental mathematics,* vol. 1, pp. 141-165, 1992.

[42] K. A. Brakke. The Surface Evolver Version 2.70 [Online]. Available: http://www.susqu.edu/brakke/evolver/evolver.html

[43] W. Chen, R. Okereke, and S. K. Sitaraman, "Compliance analysis of multi-path fan-shaped interconnects," *Microelectronics Reliability,* vol. 53, pp. 964-974, July 2013.

[44] A. I. Khuri and J. A. Cornell, *Response surfaces: designs and analyses* vol. 152: CRC press, 1996.

[45] R. K. Ulrich and W. D. Brown, *Advanced electronic packaging*: Wiley Hoboken, NJ, 2006.

[46] Amkor Technology, Inc. Copper Wire Bonding Data Sheet [Online]. Available: http://www.amkor.com/go/packaging/copper-cu-wire-bonding

[47] Amkor Technology, Inc. [Online]. Available: http://ece.wpi.edu/analog/resources/1mil_bwire_RLC.pdf

[48] M. Zeleny, "Compromise programming," *Multiple criteria decision making,* vol. 286, 1973.
[49] T. W. Athan and P. Y. Papalambros, "A note on weighted criteria methods for compromise solutions in multi-objective optimization," *Engineering Optimization,* vol. 27, pp. 155-176, 1996.
[50] R. Okereke and S. K. Sitaraman, "Three-path electroplated copper compliant interconnects—fabrication and modeling studies," in *Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd*, 2013, pp. 129-135.
[51] W. Chen, Y. Song, J. Liang, and S. K. Sitaraman, "Fabrication of Second-Level TriDelta Interconnects Using Negative Dry-Film Photoresist," in *ASME 2014 International Mechanical Engineering Congress and Exposition*, 2014, pp. V010T13A041-V010T13A041.
[52] S. Kang, J. Horkans, P. Andricacos, R. Carruthers, J. Cotte, M. Datta*, et al.*, "Pb-free solder alloys for flip chip applications," in *Electronic Components and Technology Conference, 1999. 1999 Proceedings. 49th*, 1999, pp. 283-288.
[53] B.-N. Park, S.-C. Bae, S.-H. Son, J.-H. Lee, S.-Y. Choi, C.-G. Suk*, et al.*, "Film properties of copper grown by the electroplating process," *JOURNAL-KOREAN PHYSICAL SOCIETY,* vol. 38, pp. 232-235, 2001.
[54] T. Hara, K. Namiki, and Y. Shimura, "Low resistivity copper interconnection layers," in *Solid-State and Integrated Circuits Technology, 2004. Proceedings. 7th International Conference on*, 2004, pp. 514-519.
[55] Available: http://www.murraypercival.com/files/pdf/NR200TDS.pdf
[56] G. Wang, Z. Cheng, K. Becker, and J. Wilde, "Applying Anand model to represent the viscoplastic deformation behavior of solder alloys," *Journal of electronic packaging,* vol. 123, pp. 247-253, 2001.
[57] R. I. Okereke, "Electroplated Multi-path Compliant Copper Interconnects for Flip-chip Packages," Georgia Institute of Technology, 2014.
[58] W. Engelmaier, "Results of the IPC copper foil ductility round-robin study," *Testing of Metallic and Inorganic Coatings (STP947), ASTM, Philadelphia, PA,* pp. 66-95, 1987.
[59] A. S. Prabhu, D. B. Barker, M. G. Pecht, J. Evans, and W. Grieg, "A thermo-mechanical fatigue analysis of high density interconnect vias," research directed by Dept. of Mechanical Engineering.University of Maryland at College Park, 1994.
[60] A. Syed, "Accumulated creep strain and energy density based thermal fatigue life prediction models for SnAgCu solder joints," in *Electronic Components and Technology Conference, 2004. Proceedings. 54th*, 2004, pp. 737-746.
[61] J.-H. Zhao, V. Gupta, A. Lohia, and D. Edwards, "Reliability modeling of lead-free solder joints in wafer-level chip scale packages," *Journal of Electronic Packaging,* vol. 132, p. 011005, 2010.
[62] J. S. JESD22-B111, "Board Level Drop Test Method of Components for Handheld Electronic Products," *JEDEC Solid State Technology Association,* September 2013.
[63] J.-e. Luan and T. Y. Tee, "Novel board level drop test simulation using implicit transient analysis with input-G method," in *Electronics Packaging Technology Conference, 2004. EPTC 2004. Proceedings of 6th*, 2004, pp. 671-677.

[64] T. Y. Tee, J.-e. Luan, E. Pek, C. T. Lim, and Z. Zhong, "Novel numerical and experimental analysis of dynamic responses under board level drop test," in *Thermal and Mechanical Simulation and Experiments in Microelectronics and Microsystems, 2004. EuroSimE 2004. Proceedings of the 5th International Conference on*, 2004, pp. 133-140.

[65] J.-e. Luan and T. Y. Tee, "Effect of impact pulse parameters on consistency of board level drop test and dynamic responses," in *Electronic Components and Technology Conference, 2005. Proceedings. 55th*, 2005, pp. 665-673.

[66] K. Pan, B. Zhou, and Y. Yan, "Simulating Analysis of Dynamic Responses for CSP under Board Level Drop Test," in *Electronic Packaging Technology, 2006. ICEPT'06. 7th International Conference on*, 2006, pp. 1-5.

[67] Z. Chen, X. Wang, Y. Liu, and S. Liu, "Drop test simulation of 3D stacked-die packaging with Input-G finite element method," in *2010 11th International Conference on Electronic Packaging Technology&High Density Packaging*, 2010, pp. 742-746.

[68] E. Wong, K. Lim, N. Lee, S. Seah, C. Hoe, and J. Wang, "Drop impact test-mechanics & physics of failure," in *Electronics Packaging Technology Conference, 2002. 4th*, 2002, pp. 327-333.

[69] S. Irving and Y. Liu, "Free drop test simulation for portable IC package by implicit transient dynamics FEM," in *Electronic Components and Technology Conference, 2004. Proceedings. 54th*, 2004, pp. 1062-1066.

[70] P. Lall, S. Shantaram, A. Angral, and M. Kulkarni, "Explicit submodeling and digital image correlation based life-prediction of leadfree electronics under shock-impact," in *Electronic Components and Technology Conference, 2009. ECTC 2009. 59th*, 2009, pp. 542-555.

[71] Y. Sun and J. H. Pang, "Digital image correlation for solder joint fatigue reliability in microelectronics packages," *Microelectronics Reliability,* vol. 48, pp. 310-318, 2008.

[72] W. Chen, A. Bhat, and S. K. Sitaraman, "Use of compliant interconnects for drop impact isolation," in *Electronic Components and Technology Conference (ECTC), 2013 IEEE 63rd*, 2013, pp. 835-839.

[73] A. Tribe, K. Garraway, P. M. Daborn, and K. Miles, "The Use of Rapid Prototypes for Model Validation," in *IMAC XXV*, Orlando,FL, 2007.

[74] J. Mahn and P. Bayly, "Impact testing of stereolithographic models to predict natural frequencies," *Journal of sound and vibration,* vol. 224, pp. 411-430, 1999.

[75] S. Seah, C. Lim, E. Wong, V. Tan, and V. Shim, "Mechanical response of PCBs in portable electronic products during drop impact," in *Electronics Packaging Technology Conference, 2002. 4th*, 2002, pp. 120-125.

[76] I. Gibson, G. Goenka, R. Narasimhan, and N. Bhat, "Design rules for additive manufacture," in *International Solid Free Form Fabrication Symposium*, 2010.