TRANSPORT CHARACTERISTICS OF PIN FIN ENHANCED MICROGAPS UNDER SINGLE AND TWO PHASE COOLING

A Dissertation
Presented to
The Academic Faculty

by

Zhimin Wan

In Partial Fulfillment
of the Requirements for the Degree
Doctoral of Philosophy in the
School of Mechanical Engineering

Georgia Institute of Technology
August 2016

TRANSPORT CHARACTERISTICS OF PIN FIN ENHANCED MICROGAPS UNDER SINGLE AND TWO PHASE COOLING

Approved by:

Dr. Yogendra K. Joshi, Advisor
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Saibal Mukhopadhyay
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Andrei Fedorov
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Sudhakar Yalamanchili
School of Electrical and Computer Engineering
Georgia Institute of Technology

Dr. Satish Kumar
School of Mechanical Engineering
Georgia Institute of Technology

Date Approved: [April 25, 2016]

To my grandmother
To my parents
To my brothers

ACKNOWLEDGEMENTS

I would like to deeply thank all the people who have helped me during my doctoral study at Georgia Tech.

First and foremost, I would like to thank my advisor, Dr. Yogendra Joshi, for his continuous guidance, support, encouragement. His passion and vision always inspire me to think more and differently about my research. I really enjoyed our discussions over the years and his valuable suggestions helped me a lot when I encountered difficulties in my research. I cannot thank him enough for his outstanding mentorship and kindness.

I am very grateful for my committee members, Dr. Andrei Fedorov, Dr. Satish Kumar, Dr. Saibal Mukhopadhyay, and Dr. Sudhakar Yalamanchili for their time and valuable feedback throughout my PhD proposal and defense process. Part of this work was performed in collaboration with Dr. Saibal Mukhopadhyay and Dr. Sudhakar Yalamanchili. I learned a lot about chip architectures and gained insight into the challenges of cooling-architecture co-design of microprocessor. I would like to acknowledge the financial support from Cisco Systems, Inc., Sandia National Laboratories, and National Science Fundation.

I extend my thanks to Dr. Muhannad Bakir, Dr. Yue Zhang, Dr. Li Zhen, and William Song from School of Electrical and Computer Engineering, for their valuable time, advice. I would specially like to thank Dr. Wen Yueh and He Xiao for their help and discussion on the modelling and experimental study of electrical performance of microprocessors.

I would also like to thank all the current and previous members in the Microelectronics and Emerging Technologies Thermal Laboratory (METTL) for their assistance, friendship. Especially, I want to thank Xuefei Han for her help on numerical modeling, Dr. Craig Green for his help on experiment test, Dennis Tung for his help on microfabrication, Dr. Aravind Sathyanarayana for his valuable discussion on the study of mixture.

I am very grateful to all the staff members at the Microelectronics Research Center (MiRC) for their help and guidance with the microfabrication tools and processes in the cleanroom. Especially, I would like to thank Tran-Vinh Nguyen, Charlie Suh, Hang Chen, Chris Yang, Thomas Johnson-Averett, and Mikkel A. Thomas. Without their help, I cannot finish my fabrication of test samples.

I am also grateful to all the staff members at the School of Mechanical Engineering. I would like to thank Ms. Glenda Johnson for her help on my graduate study, Ms. Regina Neequaye for help in timely ordering all the experiment stuff, Mr. Kyle French for his help on the printed circuit board (PCB) fabrication, Steven Sheffield for his help on the machining of the test package.

Last but not least, I express my deepest gratitude to my grandparents, parents and brothers for their unconditional love and support. Without their support and love, I would not have been in this position today.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

NOMENCLATURE

$\alpha_1, \alpha_2, \alpha_3, C, m$	Coefficients for friction factor and Colburn j factor
A_{pin}	Pin fin cross-section area [m^2]
A_h	Heater area [m^2]
A_{in}	Inlet cross-section area [m^2]
A_{min}	Total minimal cross-section area [m^2]
A_{eff}	Effective wetted area [m^2]
C_p	Specific heat [J/kg-K]
CHF	Critical heat flux [W/cm^2]
D_P	Diameter of the pin fin [m]
D_h	Hydraulic diameter [m]
f	Friction factor, $\frac{D_p \Delta P}{2L\rho v_{max}^2}$
f_{fan}	Fanning friction factor, $\frac{2\Delta P \rho_f}{N_L G^2}$
G	Maximum mass flux of the smallest cross section area [kg/m^2-s]
h	Heat transfer coefficient [W/m^2-K]
h_{fg}	Latent heat [kJ/kg]
$\bar{h}$	Average convective heat transfer coefficient [W/m^2-K]
H_c	Height of the channel [m]
H_P	Height of pin fin [m]
I_{leak}	Leakage current [A]
j	Colburn j factor, $StPr^{\frac{2}{3}}$
k_f	Thermal conductivity of fluid [W/m-K]

k_o	Thermal conductivity of Silicon oxide [W/m-K]
k_s	Thermal conductivity of Si [W/m-K]
L	Chip length [mm]
L_{pin}	Length of square pin [m]
$\dot{m}$	Mass flow rate [kg/s]
MAE	Mean absolute error
η	Fin efficiency
N_L	Number of pin rows in longitudinal direction
N_T	Number of pins in transversal direction
Nu	Nusselt number
P_{pin}	Pin fin perimeter [m]
Pr	Prandtl number
P_{leak}	Leakage power [W]
ΔP	Pressure drop [Pa]
PCB	Printed circuit board
Q	Total power applied on the chip [W]
q	Heat transfer rate [W]
q"	Heat flux [W/m^2]
R	Thermal resistance [k/W]
R_{cond}	Conduction thermal resistance [k/W]
R_{conv}	Convection thermal resistance [k/W]
R_{PR}	Electrical resistance of precision resistor [ohm]
Re	Reynolds number, $\frac{\rho v_{max} D_p}{\mu_f}$

St	Stanton number
S_T	Transversal pin separation in a column [m]
S_L	Longitudinal distance between pin rows [m]
t_s	Thickness of silicon [m]
t_c	Tip clearance [m]
t_o	Silicon oxide thickness [m]
T	Temperature [K]
T_b	Temperature of pin fin base [K]
ΔT	Temperature difference between fluid and silicon [K]
TS	Temperature sensor
v_{max}	Average velocity at minimal cross-section [m/s]
u	Fluid flow velocity [m/s]
v_{in}	Inlet velocity [m/s]
V	Voltage [V]
V_{dd}	Supply voltage [V]
$\dot{V}$	Volumetric flow rate [m^3/s]
W	Chip width [m]
W_{pin}	Width of square pin [m]

Greek Symbols

ρ	Density [kg/m^3]
μ	Dynamic viscosity [$Pa \cdot s$]
σ	Surface tension [N/m]

Subscripts

amb	Ambient
avg	Average
conv	Convection
cond	Conduction
f	Fluid
pr	Precision resistor
o	Oxide
s	Silicon
sat	Saturation
tot	Total

SUMMARY

Microfluidic convection cooling is a promising technique for future high power microprocessors, radio-frequency (RF) transceivers, solid-state lasers, and light emitting diodes (LED). Three-dimensional (3D) stacking of chips is a configuration that allows many performance benefits. A microgap with circulating fluid is a promising cooling arrangement that can be incorporated within a 3D chip stack. Although studies have examined the thermal characteristics of microgaps under both single-phase and two-phase convection, the characteristics and benefits of microgaps with surface enhancement features have not been fully explored. In this work, firstly, the single phase thermal/fluid characteristics of microgaps with staggered pin fin arrays are studied. The effects of the pin fin dimensions including diameter, transversal and longitudinal spacing, and height are investigated computationally and experimentally over a range of Reynolds number (Re) 22-357. Micropin fin arrays investigated have pin diameter of 100 μm, pitch/ diameter ratios of 1.5 ~ 2.25, and height/ diameter ratios of 1.5 ~ 2.25. Correlations of friction factor (f) and Colburn j factor for these dense arrays of micro pins have been developed. Subsequently, microfluidic cooling with staggered pin fin arrays is employed in functional 3D integrated circuit (ICs). Thermal and electrical performance of a CMOS chip in terms of temperature and leakage power under realistic operating conditions are studied. Both experimental and modeling results show that microfluidic cooling could significantly decrease the chip temperature and leakage power, thus increasing the chip performance. Lastly, two-phase cooling is studied with dielectric fluid HFE-7200 as a baseline with mass flux from 354.5 kg/m^2-s to 576.3 kg/m^2-s. Critical heat flux (CHF) increases with increasing mass flux but decreases with decreasing gap height. Nonuniform heating will

cause nonuniform flow with a decrease of mass flux in high power area, which decreases the thermal performance. The effects of fluid mixture (HFE-7200/Methanol) on thermal performance are studied with mass fraction of Methanol from 8.5% to 35.8%. A very small amount of addition of Methanol (8.5% mass fraction) can significantly increase the thermal performance due to the sharp decrease of saturation temperature, increase of effective thermal conductivity and latent heat. However, the Marangoni effect caused by the concentration gradient deteriorates the CHF.

CHAPTER 1

INTRODUCTION

1.1 Background

The pursuit of multi-functionality and low cost for either military or consumer electronics, such as radio-frequency (RF) transceivers, solid-state lasers, light emitting diodes (LED), and future high power microprocessor, continues pushing up the power consumption and power density of these devices. For example, Gallium-nitride (GaN) high electron-mobility transistors (HEMT) have power densities many times higher than other power transistor technologies. The output power density of a N-polar GaN HEMTs with a drawn gate length of 0.7 μm and a gate drain spacing of 0.8 μm can be 12.1 W/mm [1], resulting in a heat flux of 1.5×10^{6}W/cm^2. A pulse of sub-picosecond duration and petawatt (PW) power was first reached at the Lawrence Livermore National Laboratory in 1996, and the Jan USP laser developed there has a peak power intensity of 2×10^{20}W/cm^2 [2]. Another common example of a high heat flux device is the microprocessor for which the "Moore's law" [3] has been the driving force for development [4]. The feature size has become smaller and transistor count increased with each technology node to improve IC functionality and performance, while decreasing costs [5]. From 1971 to 2012, the feature size decreased from 10 μm to 22 nm, the transistors count increased from 2,300 to 1.4 billion, and the clock speed increased from 108 kHz to 2.9 GHz. At the same time, each transistor used about 5,000 times less energy and the price per transistor has dropped by a factor of about 50,000 [6]. The latest International Technology Roadmap for Semiconductors (ITRS) [7] shows that the transistor density on a logic chip was about

1,596 million/cm^2 in 2013 and is projected to increase to 32,179 million/cm^2 in 2026. While the transistor count is increasing, the packaging size continues to shrink due to the customer expectations for small form factor products and technology development [8]. Packaging technologies have evolved significantly from the early stage dual in-line package (DIP), and ball grid arrays (BGA), to more recent system-on-chip (SOC), system-in-package (SIP), package-on-package (PoP), and three-dimensional integrated circuits (3D ICs).

Although Moore's law has proved its success in predicting the technology trends until recently, such scaling has now slowed down [9]. The 2012 update to the ITRS [7] had growth slowing and predicted that the transistor density will double only every three years after 2013. Several factors are behind this trend. First, the size of transistor cannot be miniaturized indefinitely since it will eventually reach the fundamental physical barrier [10]. If the thickness of gate oxide layer is less than four layers of silicon atoms, the current will penetrate through the gate oxide, which leads to the failure of the transistor. Secondly, the scaling of the transistor and interconnect are not developed in the same step. While the transistor becomes faster and smaller, the global interconnect does not. Indeed the interconnects have become a major bottleneck for high performance computing systems, instead of transistors [11]. Continuing to extend Moore's law by increasing the transistor density in planar direction results in longer interconnects and increase in latency. It is reported that the interconnects latency will exceed that of transistor for interconnect length greater than 30 μm [11]. Also, the longer interconnects consume more power due to Joule heating. All of the above factors will cause degradation of the performance and reduce the expected benefits from scaling.

Compared to 2D IC in which all the chips are in the same plane, the bare chips are stacked directly for 3D ICs. 3D ICs could overcome the problems associated with 2D IC [9-11], and thus promise continuation of Moore's law in the out-of-plane direction. The vertical integration of chips could reduce the wire interconnection length by as much as 50% [12]. The global RC delay could thus be reduced and the wire-limited clock frequency increased by 3.9 X [13]. Also, the wire-limited power consumption in the interconnection could also be reduced [13]. Wide bandwidth buses between functional blocks in different chips could be achieved [14]. Lastly, 3D integration allows realization of various heterogeneous technologies including memory, logic, radio frequency (RF), and optoelectronics within a single block, increasing package functionality and reducing size.

1.1.1 Motivation for Microfluidic Cooling

Although the energy per transistor is decreasing because of the decreasing supply voltage, the total chip power is increasing due to the increase in transistor count. The power density is also increasing due to the decreasing packaging size. The power distribution on a die is usually non-uniform with some high power regions, hotspots with larger power density [15]. The power on a chip is continually increasing, and the maximum heat flux on an automotive electronics chip was about 240 W/cm^2 in 2013. It is projected that the hotspot power density could be greater than 300 W/cm^2 in 2015 [16]. If not effectively removed, it would result in high chip temperatures, which will increase the leakage power exponentially, degrade the computational performance, and possibly even accelerate failure of the device [17].

Thermal issues are extremely important for the 3D ICs development. As the number of chips in a 3D stack increases, the package heat flux based on the top surface

area increases. Also, as more components are put into the stack, the space available for cooling is reduced. Another problem is that insulation dielectric layers with low thermal conductivity exist between the chips, potentially leading to high temperature of the interior chips [18]. Heat dissipation non-uniformity on the chip can result in hotspot heat flux 10 times or larger than the average level, which is a problem in planar architectures as well [19]. The high power density in the stack, if not removed, would result in high chip temperature and thermal stress, thus limiting the performance and reliability of the chip stack [20]. For CMOS circuits, each 10 ℃ increase in operating temperature, increases delay by almost 5% [21]. Lastly, the leakage power which does not contribute to computation increases exponentially with temperature [22].

Thermal issues have been widely regarded as a key bottleneck for the continued development of microelectronics. Conventional backside air cooling cannot meet the thermal management requirements of planar and 3D devices. Microfluidic cooling with surface enhancement structures such as microchannels and micropin fin arrays have been developed for their superior heat removal capability [23].

1.1.2 Challenges

Although microfluidic cooling has superior thermal performance, there are numerous challenges associated with this new technology. The move from air cooling to microfluidic cooling requires a significant change in the design and manufacturing processes. A key challenge is to integrate the microfluidic cooling at low cost without adversely impacting reliability. A closed flow loop with heat exchanger, pump, and reservoir is needed for microfluidic cooling. These components need to be packaged compactly, or the benefits of microfluidic cooling cannot be fully realized. Possible fluid

leakage and lack of mechanical strength can cause failure of the whole system and need to be addressed in a successful design.

A promising configuration for implementing microfluidic cooling is a microgap. The thermal performance of such microgap with surface enhanced structures needs further study. The maximum heat removal capability, factors impacting heat transfer performance, and techniques for heat transfer enhancement require further study.

1.2 Research Objectives

The overall objectives of this work are to experimentally and computationally study pin fin enhanced microgaps in a systematic manner to gain fundamental understanding into its transport characteristics, and explore the benefits of microfluidic cooling on temperature and leakage power reduction. With this in mind, the following specific goals and objectives are proposed:

1. For single phase cooling, study the effects of Re, pin spacing, height, on the single phase pressure drop and heat transfer characteristics of micropin fin arrays. Develop correlations to predict the pressure drop and heat transfer coefficient.
2. Develop a coupled power-thermal model for 3D ICs with microfluidic cooling, with the ability to model both temperature and leakage power.
3. Experimentally demonstrate the benefits of microfluidic cooling on temperature and leakage power reduction.
4. Study the two-phase flow regime, and thermal characteristics of HFE 7200/ Methanol mixtures. Compare the mixture results with single fluid results.

1.3 Thesis Outline

The thesis is organized as follows:

Chapter 1 introduces the background and motivations for this work. The challenges associated with microfluidic cooling have been presented and the overall objectives and scope of this work are also discussed.

Chapter 2 reviews the existing state-of-art of both single phase, two phase cooling of pin fin enhanced microgaps, and their applications. Flow boiling with different fluids

and fluid mixtures are presented. Applications of microfluidic cooling in 3D ICs are also reviewed.

In Chapter 3, design and fabrication of the pin fin enhanced microgaps with integrated temperature sensors are presented. A fabrication procedure is proposed and the fabrication challenges are discussed. Accordingly, the PCB and package design are also presented. A closed flow loop is built to test the characteristics of the pin fin enhanced microgaps.

Chapter 4 presents the results of the computational fluid dynamics (CFD) modeling of staggered pin fin enhanced microgaps under single phase cooling with DI water as the coolant. The numerical model is validated against experiments. The effects of the pin fin dimensions including diameter, transversal and longitudinal spacing, and height are investigated computationally and experimentally over a range of Reynolds number (Re) 22-357. Micropin fin arrays investigated have pin diameter of 100 μm, pitch/ diameter ratios of 1.5 ~ 2.25, and height/ diameter ratios of 1.5 ~ 2.25. Performance of circular and square pin fin are compared. Correlations of friction factor (f) and Colburn j factor for these dense arrays of micro pins have been developed.

To demonstrate the benefits of microfluidic cooling, a compact thermal model of 3D stacked ICs with integrated microfluidic cooling is presented in Chapter 5. Model validation is performed and illustrative cases studies are conducted. It is demonstrated that microfluidic cooling can achieve significant temperature and leakage power reduction. Experiment with a functional CMOS chip are conducted to compare the performance of air cooing and microfluidic cooling, which further proves the benefits of microfluidic cooling.

Flow boiling experiments were performed with pure HFE 7200 and HFE 7200 – Methanol mixture and the results are discussed in Chapter 6. HFE 7200 has high electrical resistivity but low thermal properties. Addition of Methanol into HFE 7200 can decrease its saturation temperature significantly, increase the effective thermal conductivity and latent heat. However, the Marangoni effect has a negative effect on heat transfer.

Chapter 7 summarizes the entire work and provides recommendations for future work.

CHAPTER 2

LITERATURE REVIEW

Microfluidic cooling offers high surface area to volume ratio, large convective heat transfer coefficient (h), small mass and volume, and small coolant inventory. These attributes render the microfluidic heat sink very suitable for cooling such devices as high-performance microprocessors, laser diode arrays, radars, and high-energy-laser mirrors [24]. In this chapter, earlier work on single phase, two phase and the applications of microfluidic cooling are reviewed.

2.1 Single Phase Cooling

The microchannel heat sink cooling concept was first introduced by Tuckerman and Pease in the early 1980s [23]. They fabricated a rectangular micro-channel heat sink in a 1 x 1 cm^2 silicon wafer. The channels had a width of 50 μm and a depth of 302 μm, and were separated by a 50 μm thick walls. Using water as cooling fluid, the microchannel heat sink was capable of dissipating 790 W/cm^2 with a maximum substrate temperature of 71 ℃ above the water inlet temperature and a pressure drop (ΔP) of 214 kPa. Due to their inherent advantages, microchannel heat sinks have received considerable attention [25-29] since Tuckerman and Pease's pioneering study.

However, significant temperature variations across the chip persist for conventional single pass parallel flow microchannel heat sink, since the heat transfer performance deteriorates in the flow direction in microchannels as the coolant heats up. Recent advancement in micromachining techniques allows more complex 3D microsize geometries to be fabricated directly into the high thermal conductivity materials that can be used as the substrates for miniature heat sinks. This makes it possible to explore structures that may be more effective in heat transfer enhancement than the parallel

microchannels. One such enhanced structure is micropin fin arrays with pin characteristics dimension of tens to hundreds of micrometers and height (H_p) to diameter (D_p) ratio from 0.5 to 8. The flow disruptions provided by the separated pin fins increase the flow mixing and also can serve to break up the boundary layer [30].

Thermal design and performance assessment of a micropin fin heat sink require a fundamental understanding and accurate prediction of ΔP and heat transfer in microsize short pin fin arrays. The thermal-hydraulic performance of micropin fin arrays and microchannel was compared in terms of total thermal resistance (R_{tot}) by Peles et al. [31]. At a ΔP of two atmospheres, the minimum R_{tot} was 0.0389 K/W, which corresponded to 7.8 ℃ maximum wall temperature raise for 200 W/cm^2 heat dissipation power, and 30.7 ℃ at 790 W/cm^2 compared to 71 ℃ for microchannel cooling [23]. A recent study by Jasperson et al. [32] showed that the flow rate was a factor to determine whether microchannels or micropin fin arrays have better performance. In their study, microchannels and micropin fin arrays of same height and width (670 μm and 200 μm) were made on copper. Under a mass flow rate from 30 g/min to 90 g/min, the ΔP of micropin fin heat sink was always higher than that of microchannel heat sink and the difference increased with the flow rate. The convection thermal resistance (R_{conv}) of micropin fin heat sink was higher than that of microchannel heat sink at flow rate less than 60 g/min and lower above 60 g/min.

The micropin fin arrays can be arranged in in-line or staggered configurations. Kosar et al. [33] experimentally studied and compared the ΔP associated with the forced flow of de-ionized water over staggered and in-line circular micro pin fins. The D_p was 100 μm, H_p was 100 μm, longitudinal (S_L) and transverse (S_T) spacing were 150 μm. Under the same Re, the staggered configuration resulted in higher ΔP than the in-line

configuration. A more recent comparison study by Brunschwiler et al. [34] showed that under the same flow rate, in-line pin fin showed lower ΔP and higher thermal resistance than staggered pin fin. Another interesting finding was that in-line pin fin presented a flow regime transition, which manifested itself as an abrupt pressure gradient change and a local heat transfer maximum. The transition moved towards the inlet at increasing flow rate.

Due to the superior performance of staggered micropin fin arrays, considerable research has been done to study its thermal and hydraulic characteristics from different aspects, including the effects of Re, S_T, S_L, H_p, pin shape, tip clearance (t_c).

2.1.1 Effect of Re

Due to the small pin fin dimensions at the microscale, the flow regime is expected to be predominantly laminar. For a specific pin fin configuration, the heat transfer coefficient (h) and ΔP increase with Re. The non-dimensional friction factor (f), could be defined as [35]:

$$f_{fan} = \frac{2\Delta P \rho_f}{N_L G^2} \tag{2.1}$$

where ρ_f is the fluid density, N_L is the number of pins in the longitudinal direction, G is the maximum mass flux of the smallest cross section area.

The friction factor is comprised of two components, one accounting for the drag due to flow separation and the other stemming from shear stress [35]. As the fluid flows across the micropin fins, a thin boundary layer is formed at the pin surface. As Re increases, the boundary layer becomes thinner and flow separation is enhanced [35]. Kosar et al. [33] experimentally studied the pressure drop and f of circular micropin fin arrays and their results showed that f decreased with increasing Re, which was also observed by Prasher et al. [36], Short et al. [37] and Tullius et al. [38]. A change in the relationship of f to Re was

observed by both Kosar et al. [33] and Prasher et al. [36]. f was very sensitive to Re for Re <100 and was less sensitive to Re for Re >100. It was believed that some type of transition was happening around Re=100. Nusselt number (Nu) increased with Re, which is also observed by Prasher et al. [36], Tullius et al. [38] and Short et al. [39]. Similarly, two distinct regions of the Nu dependency on the Re separated by Re=100 had been identified [33, 35]. Kosar and Peles [40-41] attributed such dependency to two factors: endwall effects and a delay in flow separation. Flow separation was assumed to control the transition Re.

2.1.2 Effect of Spacing

The effect of longitudinal spacing was evident when comparing the friction factors of micropin fin array with S_L=150 μm and S_L=350 μm [35]. Device with S_L=150 μm had larger f than device with S_L=350 μm, which suggested that densely populated pin fins lead to higher f. This was because that wakes behind pin fins formed due to flow separation. For densely populated pin fins the wake generated downstream of a pin fin interacted more strongly with pin fins in the following row. As a result, f were higher for closely packed objects. This was also observed by Prasher et al. [36] and Short et al. [37]. However, Tullius et al. [38] showed an opposite trend. h of device S_L=150 μm were greater than for device S_L=350 μm over Re ranging from 30 to 112 [35]. This may be due to the pronounced wake-pin fin interaction in S_L=150 μm. Because of the dense spacing, the wake formed downstream a pin fin may interacted with the pin fins in the following row, so that mixing and heat transfer were enhanced. This was reflected as higher h in S_L=150 μm. Since at low Re, the wake-pin fin interaction moderated, deviations between Nu of the two devices

diminished. Results of Prasher et al [36] agreed with observation in [35]. However, Both Tullius et al. [38] and Short et al. [39] showed that sparse pins had larger h.

Very little work studied the effect of S_T on f and Nu. Prasher et al. [36] and Short et al. [37] reported an increasing f with decreasing S_T while an opposite trend was presented by Tullius et al. [38]. Both Tullius et al. [38] and Short et al. [39] found that Nu increased with increasing S_T.

2.1.3 Effect of Aspect Ratio (H_P/D_P)

Ratio of H_p to D_p has a significant effect on the f. It was reported that the micropin fin arrays with lower H_P/D_P ratio produced higher f at the same pin densities and Re [33]. However, The H_P/D_P ratio effect reduced with increasing Re [33]. This was attributed to the endwall effect. Small aspect ratio devices were more affected by the hydrodynamic boundary layer imposed by the endwalls (wall pin interaction), resulting in increased viscous shear forces and therefore larger f were obtained [42]. The effect of pin fin H_p to D_p aspect ratio was significant for low Re and diminished at larger Re because of a thinning hydrodynamic boundary layer. Therefore, with the increase in Re, the deviation between smaller and larger H_p to D_p pillars moderated. The observation in [33, 42] agreed with Prasher et al. [36] for Re <100 and Short et al. [37]. However, f was reported to be increased with aspect ratio for Re>100 [36, 38].

The dependence of the Nu on the Re was considerably more notable than for long pin fin as a result of endwall effects [33] since the end wall effects were significant at a low Re flow over short pin fins ($1/2<H_P/D_P<6$). Two intrinsically coupled physical factors adversely affected h at 10< Re<100 for flow over micropin fins: the thermal and hydrodynamic boundary layer established at the end wall and a delay in flow separation to

higher Re. The suppression of h was amplified with the reduction of H/D ratio and was more evident at low Re [40]. The results of Short et al. [39] showed that Nu decreased with increased aspect ratio. However, Koz et al. [43] did a parametric study on the effect of end walls on heat transfer and found that Nu increased with Re but not necessarily with H_P/D_P. Nu of various H_P/D_P ratios can show different trends when plotted against Re. Tullius et al. [38] found that Nu increased with aspect ratio.

2.1.4 Effect of Tip Clearance

The clearance (t_c) between the pin tip and wall was believed to affect the overall hydraulic and thermal performance of a given cooling system [44]. Introducing tip clearance resulted in a decrease in form drag and an increase in shear stresses at the walls [45]. The balance between the two determined the overall increase or decrease in f. A slightly increase in f with t_c/D_P =0.1 at high Re was observed [45]. As the t_c increased further to t_c/D_P=0.3 and 0.4, f was decreased. The reduction in f with increasing t_c was much more evident at higher Re. Moores et al. [46] also found that the overall pressure drop is initially increased with the introduction of tip clearances for t_c/D_P <0.1 and then decreased.

The pin fins tend to have relatively low height to diameter ratio due to the high h. So the pin tip area can represent a considerable portion of the total area of the array. Exposing the tips of the pin fins to the cooling fluid can increase the total heat transfer area. Also the tip clearance introduces a three dimensional behavior into the flow field around the pins and may change the local heat transfer rate. Moores and Joshi [47] reported an increase of heat transfer rate with the introduction of t_c and attributed the enhancement primarily to the additional surface area exposed to the cooling fluid. Rozati et al. [45]

believed that t_c affected h by eliminating viscosity dominated endwall effects on the pin, by eliminating the pin wake shadow on the end walls, by inducing accelerated flow in the vicinity of the top wall and the pin top, by reducing or impeding the development of the recirculating wakes, and by redistributing the flow along the height of the channel. For a tip gap of t_c/D_P =0.1, Nu decreased sharply. As t_c/D_P continued to increase, the Nu increased [45].

2.1.5 Effect of Pin Shape

Advanced microfabrication technologies enable researchers to explore the characteristics of micropin fins with different shape beside circular pins. The pins can be divided into two categories: streamlined pins like hydrofoil, and unstreamlined pins including circular, square, diamond, cone, triangle, hexagon, and ellipse. ΔP and heat transfer characteristics of square micropin fins were experimentally studied by Siu-Ho et al. [48] and Liu et al. [49]. Their results showed that both ΔP and h increased with increasing Re. A flow friction factor transition phenomenon appeared at Re~300 [49]. h had a higher value near heat sink inlet and decreased along the flow direction. This trend may be caused by entrance and streamwise heat conduction effects [48].

Micropin fins having sharp edges generated higher h than streamlined pin fins [35]. This was associated with separation effects mitigated by sharp edges as well as extended wake regions, which increased the mixing and heat transfer. However, sharp edge pins resulted in larger f. The sharp edges enhance wake-pin interaction and introduced more pressure drop. A comparison between circular, diamond, square micropin fins with same hydraulic diameter, spacing and height by Kosar et al. [33] and Mita et al. [50] showed that circular micropin fins had smallest f. Hydrofoil pin fins with zero angle of attack resulted

in considerably lower f compared to circular pins, especially at high Re [42]. f of the hydrofoil device at a Re of 1,000 was around 7.5 times lower than that for the circular pin fin device. The difference in f continued to amplify as the Re increased above 1,000, primarily because crossflow over circular shape fins transitioned to turbulent flow (where the friction factor is less dependent on Re), while flow over the hydrofoil fins was well within the laminar flow regime. Therefore, the merits of using micropin fin device are dependent on the performance evaluation criterion used, as well as on the hydrodynamic conditions. In general, for a fixed pressure drop and pumping power, utilizing streamlined pin fin heat sink is favored at moderate pressure drops and flow rate, while for very high and lower pressure drops and flow rates pin fins promoting flow separation should be favored. For fixed mass flow rate, streamlined pin fins provided inferior performance.

Table 2.1: Nu correlations-single phase.

Ref.	Phase	Fluid	Scale	Correlation
Prasher et al. [36]	Single	water	D_P= 55 μm, 155 μm; H_P/D_p=1.3,2.48,2.8; S_T/D_P=2.4, 3.6; S_L/D_P=2.4, 3.6;	Nu=0.132$(\frac{S_L-D_P}{D_P})^{-0.256}Re^{0.84}$ Re<100 $Nu = 0.281(\frac{S_L-D_P}{D_P})^{-0.63}Re^{0.73}$ Re>100

Table 2.1 (continued).

Ref.	Phase	Fluid	Scale	Correlation
Short et al. [39]	Single	air	D_P= 1.75mm~ 3.18mm; H_P/D_p=1.88~7.25; S_T/D_P=2.0~6.41; S_L/D_P=1.83~3.21;	$Nu = 0.76(\frac{H_P}{D_P})^{-0.11}(\frac{S_L}{D_P})^{0.16}(\frac{S_T}{D_P})^{0.2}Re^{0.33}Pr^{1/3}$ 100<Re<1000
Tullius et al. [38]	Single	water	D_H= 0.5mm~ 2.5mm; H_P/D_p=0.25~0.75; S_T/D_P=1~5; S_L/D_P=1.5~5;	$Nu = 0.08\left(\frac{H_P}{D_P}\right)^{0.25}(1 + \frac{t_c}{D_P})(\frac{S_L}{D_P})^{0.2}(\frac{S_T}{D_P})^{0.2}Re^{0.6}Pr^{0.36}(\frac{Pr}{Pr_s})^{0.25}$ 100<Re<1400
Kosar and Peles [41]	Single	R-123	D_P= 99.5 μm; H_P/D_p=2.44; S_T/D_P=1.5; S_L/D_P=1.5;	$Nu = 0.0423Re^{0.99}Pr^{0.21}(\frac{Pr}{Pr_s})^{0.25}$ 134<Re<314
Moores and Joshi. [47]	Single	water	D_H= 3.67mm~ 3.84mm; H_P/D_p=0.52~1.09; S_T/D_P=1.3~1.36; S_L/D_P=1.13~1.18; tc/D_P=0~0.25;	$Nu = 0.64\left(\frac{H_P}{D_P}\right)^{0.36}(\frac{t_c + H_P}{H_P})^{-0.57}Re^{0.64}Pr^{0.36}$ 100 < Re <1000

Table 2.1 (continued).

Ref.	Phase	Fluid	Scale	Correlation
Liu et al. [49]	Single	water	D_H= 445 μm, 559 μm H_P =3mm; S_T =0.5657mm; S_L =0.5657mm;	$Nu = 0.143Re^{0.615}Pr^{0.33}$ 0< Re <800 $Nu = 0.1245Re^{0.6106}Pr^{0.36}(\frac{Pr}{Pr_w})^{0.25}$ 0< Re <800
Konish et al. [51]	Single	water	D_H= 200 μm; H_P =670 μm; S_T =400 μm; S_L =400 μm;	Nu=10.485$Re^{-0.35}$
Qu and Siu-Ho [52]	Single	water	D_H= 200 μm; H_P =670 μm; S_T =400 μm; S_L =400 μm;	Nu=0.0285$Re^{0.932}Pr^{0.333}$ Re <100

Table 2.2: f correlations-single phase.

Ref.	Phase	Fluid	Scale	Correlation
Kosar et al. [33]	Single	water	D_P= 50 μm, 100 μm; H_P/D_p=1,2; S_T/D_P=1.5; S_L/D_P=1.5;	$f_{fan}=\pi_1+\pi_2$, 5 < Re < 128. $\pi_1=\frac{1739}{Re^{1.7}}(\frac{H_P/D_P}{\frac{H_P}{D_P}+1})^{1.1}(\frac{S_T S_L}{A_c})^{-0.3}$ $\pi_2=\frac{345}{Re^{1.0}}(\frac{1}{\frac{H_P}{D_P}+1})^{2.0}(\frac{S_T S_L}{A_c})^{-0.3}$
Prasher et al. [36]	Single	water	D_P= 55 μm, 155 μm; H_P/D_p=1.3,2.48,2.8; S_T/D_P=2.4, 3.6; S_L/D_P=2.4, 3.6;	$f_{fan}=679.2(\frac{H_P}{D_P})^{-0.640}(\frac{S_L-H_P}{D_P})^{-0.258}(\frac{S_T-H_P}{D_P})^{-0.258}Re^{-1.35}$ Re<100 $f_{fan}=1.18(\frac{H_P}{D_P})^{1.249}(\frac{S_L-H_P}{D_P})^{-0.7}(\frac{S_T-H_P}{D_P})^{-0.36}Re^{-0.1}$ Re>100
Short et al. [37]	Single	air	D_P= 1.75mm~3.18mm; H_P/D_p=1.88~7.25; S_T/D_P=2.0~6.41; S_L/D_P=1.83~3.21;	$f=140.4(\frac{H_P}{D_P})^{-0.55}(\frac{S_L}{D_P})^{-1.3}(\frac{S_T}{D_P})^{-0.78}Re^{-0.65}$ 100<Re<1000
Tullius et al. [38]	Single	water	D_H=0.5mm~2.5mm; H_P/D_p=0.25~0.75; S_T/D_P=1~5; S_L/D_P=1.5~5;	$f_{fan}=2.963\left(\frac{H_P}{D_P}\right)^{0.18}(1+\frac{t_c}{D_P})^{0.2}(\frac{S_L}{D_P})^{0.2}(\frac{S_T}{D_P})^{0.2}Re^{-0.435}$ 100<Re<1400

Table 2.2 (continued).

Ref.	Phase	Fluid	Scale	Correlation
Tullius et al. [38]	Single	water	D_H= 0.5mm~ 2.5mm; H_P/D_p=0.25~0.75; S_T/D_P=1~5; S_L/D_P=1.5~5;	$f_{fan} = 2.963\left(\frac{H_P}{D_P}\right)^{0.18}(1 + \frac{t_c}{D_P})^{0.2}(\frac{S_L}{D_P})^{0.2}(\frac{S_T}{D_P})^{0.2}Re^{-0.435}$ 100<Re<1400
Moores et al. [46]	Single	water	D_H= 3.6mm~ 3.8mm; H_P/D_p=0.52~1.09; S_T/D_P=1.3~1.36; S_L/D_P=1.13~1.18; tc/D_P=0~0.25;	$f_{fan} = 10.5k_1\left(\frac{H_P}{D_P}\right)^{0.28+(1-k_1)}Re^{-0.39+(1-k_2)}$ $k_1 = e^{4.3(\frac{t_c}{H_P})}$ $k_2 = e^{0.8(\frac{t_c}{H_P})}$ 200<Re<10000
Moores and Joshi. [47]	Single	water	D_H= 3.6mm~ 3.8mm; H_P/D_p=0.52~1.09; S_T/D_P=1.3~1.36; S_L/D_P=1.13~1.18; tc/D_P=0~0.25;	$f_{fan} = 19.04\left(\frac{H_P}{D_P}\right)^{-0.742}(\frac{t_c + H_P}{H_P})^{0.505}Re^{-0.502}$ 100 < Re <1000
Liu et al. [49]	Single	water	D_H= 445 μm, 559 μm H_P =3mm; S_T =0.5657mm; S_L =0.5657mm;	$f_{fan} = 43.322Re^{-0.9116}E^{0.9362}$ 0< Re <300 $f_{fan} = 1.6361Re^{0.01076}E^{-0.94496}$ 300< Re <550 $E = \frac{2S_T}{W_c/sin45^\circ}$

Table 2.2 (continued).

Ref.	Phase	Fluid	Scale	Correlation
Qu and Siu-Ho [53]	Single	water	D_H= 200 μm; H_P =670 μm; S_T =400 μm; S_L =400 μm;	f_{fan}=$20.09Re^{-0.547}$ Re<100
Konish et al. [54]	Single	water	D_H= 200 μm; H_P =670 μm; S_T =400 μm; S_L =400 μm;	$f_{fan} = \frac{55.631}{Re} + \frac{2.1114}{Re^{0.09597}}$ Re<700

2.2 Two Phase Cooling Using Flow Boiling

A key limitation of single-phase cooling is the bulk fluid temperature rise along the flow direction due to the sensible heating, which results in temperature non-uniformity on the chip. Flow boiling is an alternative approach for which the bulk fluid temperature depends on the saturation pressure. It has higher heat transfer coefficients, so reduced fluid flow rates are required [17]. The resulting smaller pressure drop can result in higher surface temperature uniformity. Two-phase micropin fin heat sinks that utilize arrays of micro size pin fins as internal heat transfer enhancement structures, and capitalize on latent heat exchange have recently emerged as a promising alternative to the popular two-phase microchannel heat sinks to meet the future high heat flux electronic cooling needs [55].

The mechanisms of nucleate boiling and two-phase forced convection govern saturated flow boiling heat transfer [55]. The regime dominated by nucleate boiling is

usually associated with bubbly and slug flow. In this regime, liquid near the heated surface is superheated to a sufficient degree to sustain nucleation. h is dependent upon heat flux, but fairly independent of mass velocity and vapor quality. The general trend is increasing h with increasing heat flux due to intensification of nucleation. The regime dominated by two-phase forced convection, on the other hand, is often associated with annular flow. In this regime, nucleation is suppressed along the heated surface, and heat is transferred mainly by conduction across the liquid film and evaporation at the liquid-vapor interface. As such, h is dependent upon mass velocity and vapor quality, but less sensitive to heat flux. The general trend is increasing h with increasing mass velocity and vapor quality due to reduction in liquid film thickness along the heated surface.

2.2.1 Flow Boiling with Pure Fluid

Qu and Siu-Ho [55] conducted experiments to measure coefficient for water saturated flow boiling in an array of staggered square micro pin fins. For a near saturated inlet, h was fairly constant in the high quality region, insensitive to both quality and mass velocity. Heat transfer in the low quality region was enhanced by inlet subcooling. The enhancement effect due to the inlet subcooling diminished with increasing quality. Two phase forced convection associated with annular flow was postulated to be the governing heat transfer mechanism.

Krishnamurthy and Peles [56] studied the flow boiling of water across a bank of circular staggered micropin fins, 250 μm long and 100 μm diameter with pitch-to-diameter ratio of 1.5. For mass flux G=364 kg/m^{2}s at heat fluxes slightly above the onset of boiling, vapor formed at nucleation sites in the vicinity of the channel exit. The hydraulic resistance imposed by the pin fins forced the bubbles to oscillate between the pin fins. The sliding

motion of the bubble caused the thin liquid film between the surface and the bubble to evaporate and to form vapor cavity. High surface tension forces acting along the vapor-liquid interface, low superficial liquid velocity, and hydraulic resistance of the pin fins caused these vapor cavities to remain stationary. With increasing heat flux, the vapor cavities grew, resulting in an increase in the local void fraction. This in turn increased the local superficial liquid velocity and, thus the drag force on the vapor cavity forcing the bubbles to propagate downstream. At higher heat fluxes, annular flow was established. The heat transfer coefficient moderately depended on the mass flux and was weakly dependent on the heat flux. This trend suggested that the dominant heat transfer mechanism was convective boiling, which was further supported by the presence of annular flow observed during flow visualization. This convective flow boiling was also observed by Isaacs et al. [57-58]. However, an experiment by Reeser et al. [59] found that the average heat transfer coefficient appeared almost independent of mass flux and increased with heat flux.

Due to the microscale flow passages and vapor production inside the heat sink, excessive pressure loss is always a concern, which can lead to elevated pumping power consumption and high operating cost. Konishi et al. [51] found that for a given mass flux, pressure drop increased rapidly with increasing exit vapor quality x_e. For a fixed x_e, pressure drop increased appreciably with increasing mass flux. Heat transfer coefficient was found to decrease sharply at low exit quality and low heat flux, and then plateaued at moderate to high exit qualities and heat fluxes [55]. However, Reeser et al. [59] showed that the average heat transfer coefficient increased monotonically as the x_e increased from 0% to 25%. It was also important to note that the inline and staggered data points nearly coincide over the entire range of qualities, implying that-contrary to conventional wisdom-

neither the inline nor staggered array was significantly better than the other in terms of cooling performance in this parametric range.

The selection criteria for coolant for two phase cooling are different from single phase coolant due to the different working conditions. For example, operating pressure is a major consideration for two-phase cooling. The saturation temperature of water is 100 ℃ at atmosphere pressure, which is too high for CMOS chips to effectively utilize the benefit of latent heat. Although water is the best coolants, their high electrical conductivities make them difficult to use for direct chip level cooling. Dielectric fluids are electrically non-conductive and therefore preferred over water for direct contact cooling. Fluorinerts are more inert, and over long usage durations may be a better choice from materials compatibility and reliability perspective for some applications with flow loops comprised of components such as metal tubing. R-123 was used as the fluid to study the boiling inception and pressure drop over a bank of micropin fin arrays 243 μm long with hydraulic diameter of 99.5 μm [41]. Boiling initiation was suppressed to high liquid superheat temperatures due to the hydrophilicity of the working fluid on silicon surfaces. R-123 has a near-zero contact angle on silicon, and as a result large nucleation cavities were flooded, which in turn gave rise to high liquid superheat at boiling inception. The delay in boiling to high superheats triggered a chain of periodic events. Once boiling is initiated, vapor burst instabilities are remarkable.

McNeil et al. [60] compared flow boiling heat transfer in in-line pin fin and plane channel using R113 at atmospheric pressure. The mass flux range was 50 – 250 kg/m^{2}s and the heat flux range was 5 – 140 kW/m^2. The measured heat transfer coefficients for the pin fin surface were slightly higher than those for the plate surface. Both were dependent on

heat flux and reasonably independent of mass flux and vapor quality. Thus the heat transfer was probably dominated by nucleate boiling. The pin fin pressure drops were typically 7 times larger than the plate values.

HFE-7200 has also been studied as a dielectric coolant [59]. Unlike the observed water behavior, the HFE-7200 data displayed an approximately 50% improvement in the average coefficient for the staggered array over the inline array, for much of the range of exit qualities. Most notable for both HFE-7200 array configurations, however, was the initial sharp decline in the average heat transfer coefficient from the lowest exit qualities to about 10%-15%, followed by a plateauing or mild increase up to exit qualities of 40%-50% where it reached a local maximum. Finally, the average heat transfer coefficient deteriorated as the exit quality approaches 100%, possibly reflecting localized dryout in the pin fin arrays.

Ma et al. [61] studied the flow boiling heat transfer performance of FC-72 on silicon chips with micro-pin finned surface. Channel liquid velocities of 0.5, 1 and 2m/s were tested at inlet subcoolings of 15, 25 and 35 K. The micro pin finned surface had considerable heat transfer enhancement compared to a smooth surface. The CHF values for all the surfaces increased with fluid velocity and subcooling. And the effect of fluid velocity was more notable, especially for fluid velocity larger than 1 m/s. The CHF of the micro pin fin surface was more sensitive to the fluid velocity and liquid subcooling than that of the smooth chip. For a lower ratio of pin fin height to fin pitch and/or higher fluid velocity, the forced flow and heat transfer on the chip had a great effect on the bubble nucleation, and the entire micro pin finned surface was not completely covered with bubbles, creating a dominant convective heat transfer effect in the nucleate boiling region.

2.2.2 Flow Boiling of Mixtures

Fluid mixtures have been a research topic for boiling enhancement and studied extensively. A large body of work has focused on pool boiling of mixtures, and the enhancement mechanisms have been studied. Van Wijk et al. [62] studied the mixtures of water with aceton, alcohols, ethylene glycol and methylethylketone. A CHF enhancement was achieved at an optimum concentration. They concluded that this enhancement in CHF was due to reduction in the bubble departure diameters. McGillis and Carey [63] investigated pool boiling of mixtures of water with ethylene glycol, methanol, and 2-propanol. Small addition of alcohol to water enhanced the CHF. The mixtures were classified into positive (more volatile component has lower surface tension), and negative (less volatile component has the lower surface tension) mixtures. Due to the differences in fluid volatility, preferential evaporation of one component occurred along the liquid-vapor interface of a binary mixture. The variation in concentration along the liquid – vapor interface resulted in a surface tension gradient (Marangoni effect). If the surface tension of the more volatile component was less than the surface tension of the less volatile component, the concentration gradient would generate a force that pulled the liquid toward the heated wall. If the surface tension of the more volatile component was greater than the surface tension of the less volatile component, a force that pulled the liquid away from the heated surface can be generated. The study by Hovestreijdt [64] and Fujita and Bai [65] attributed the CHF enhancement to the Marangoni effect. Kandlikar and Alves [66] did pool boiling experiments using mixtures of water with ethylene glycol at low concentrations (1 -10 wt. %). The effects of surface tension gradients were negligible at low mixture concentrations, and they attributed the improvement in heat transfer

coefficient to the changes in contact angle and wetting characteristics of the mixture. Arik and Bar-Cohen [67] observed significant CHF enhancement using mixture of FC-72 and FC-40. They attributed the enhancement to the improvement in thermal properties of the mixture.

There exist a few studies on flow boiling of mixtures. Peng et al. [68] and Lin et al. [69] studied the flow boiling of water-methanol mixtures in microchannels. The CHF increased at low concentration but decreased as the concentration of methanol in water increased. The enhancement was attributed to the Marangoni effect. However, heat transfer degradation was also observed by other studies. Benett and Chen [70] observed a significant reduction in heat transfer coefficient for mixtures of water and ethylene glycol and attributed it to mass transfer effects. Kandlikar and Bulut [71] studied the flow boiling of ethylene glycol and water. The heat transfer performance deteriorated as ethylene glycol concentration increased. They also attributed the degradation to the mass transfer. Sathyanarayana [72] conducted flow boiling experiment with 20 wt. % mixture of HFE 7200 – methanol in a microgap channel. The CHF enhancement was attributed to the smaller bubble departure diameter.

2.3 Applications of Microfluidic Cooling

A key area for potential use of microfluidic cooling is 3D stacked microelectronics. Due to the compatibility of pin fin arrays with TSVs, 3D ICs structures with integrated microgaps with pin fin arrays have been developed (Figure 2.1) [73]. The microgaps with pin fins were fabricated on high power processors, and low power memory chips were stacked on the microgaps. Signal vias for interlayer communication were embedded in the pin fins. This 3D system allowed high performance communication between processors

and memory stacks, with low parasitic and low energy interconnects. Experiments showed that the staggered pin fin heat sink was able to provide a thermal resistance as low as 0.27 Kcm^2/W at a flow rate 70 ml/min [74].

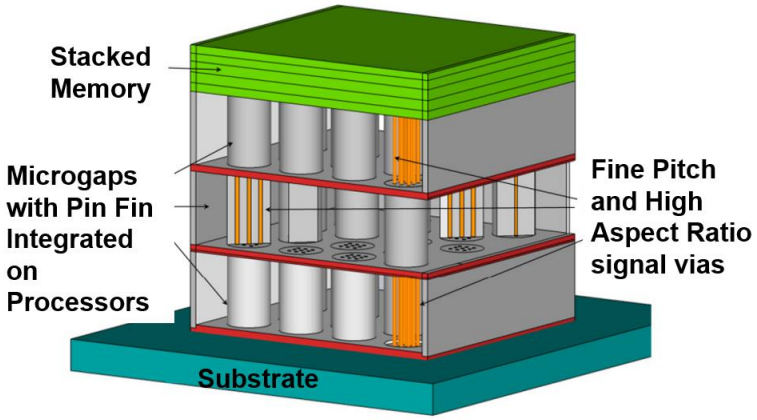


Figure 2.1: Schematic of micro pin fin heat sink with embedded signal vias [73].

The coupled fluid flow and heat transfer, and the interplay between different tiers pose challenges for the modeling of heat transfer in 3D stack. In order to design single phase microfluidic cooling, accurate thermal modeling is needed. However, computational fluid dynamics/heat transfer (CFD/HT) based detailed numerical analysis methods, such as finite element or finite volume, need very fine mesh, and are time-consuming, and thus not suitable for thermal management of very complex 3D architectures. Compact or reduced thermal modeling is typically used to improve computational efficiency. Fast and accurate thermal circuit model for 3D ICs with integrated microchannel heat sink was proposed based on thermal circuit [75]. This model achieved more than 3,300x speedup with less than 5% error, in comparison with a commercial numerical finite volume simulation tool. However, it was only applicable to steady state conditions and numerical

pre-simulations were needed for every simulation executed, which further increased the calculation time.

3D-ICE was a transient compact thermal model, which took into account the effects of the inter-tier cooling through microchannel heat sink [76]. The advantage of 3D-ICE was that it can predict the temporal evolution of chip temperatures. Only one node was used for each channel block, which reduced the problem size greatly. Empirical correlations for heat transfer coefficient were used, so no detailed convective heat transfer analysis was needed. However, the empirical correlations utilized were for fully developed flow and did not capture the developing flow regime.

Another technique to model the integrated microchannel cooling of 3D ICs was based on modeling the channel layer as a porous medium [77]. A porous medium model as in ref [77] was developed to analyze the thermal characteristics of 3D ICs with integrated microgaps. One limitation of the previous thermal resistance method [76] was that the grid size must be the same as the channel pitch. Using the porous medium model removed this limitation by homogenizing the channel layers. As such, it provided freedom to increase the grid size, resulting in faster simulations.

Currently, two-phase cooling modeling of 3D ICs has only been developed for microchannels [78-79]. A two-tier stack of logic and memory with integrated microchannel cooling under flow boiling condition was studied by numerical modeling [78]. The two-phase microchannel cooling had distinct characteristics of a nonuniform temperature distribution, even under a uniform heating condition. The temperature increased along the channel in the liquid phase region due to sensible heating, and decreased in the two phase region due to decrease of the fluid saturation pressure along the channel. The junction

temperature had its peak at the onset of boiling due to the dramatic change in convective heat transfer coefficient from a liquid-phase region to a two-phase region. A 4-tier stack with Intel Core 2 Duo processors under two-phase cooling was studied [79]. Single-pass channel and dual-pass channel configurations were compared. Under the same pressure drop between the inlet and outlet, the dual pass configuration with short flow path had lower flow resistance.

2.4 Summary

Compared to microchannels, thermal and hydraulic characteristics of pin fin enhanced microgaps remain relatively unexplored. When the pin diameter decreases to the range of interest in the proposed study (D_P~100 μm), flow separation, endwall effects, and wake interaction become increasingly important in determining the pressure drop and heat transfer coefficient. The clearance between the tip and wall significantly changes the pressure drop. It is still unknown whether the appearance of clearance will increase or decrease the thermal performance. The heat transfer coefficient and pressure drop correlations existing in the literature were developed either for a specific pin dimensions or mini pins. They do not extrapolate well to the pin dimensions of interest. Also, the effects of pin spacing, height on pressure drop and heat transfer are contradictory in literature. It is very important to comprehensively investigate the effects of Re, H_P, S_T, S_L and t_c, and develop new correlations for pressure drop and heat transfer coefficient.

The benefit of microfluidic cooling can be demonstrated by both modeling and experiments. The main problems of the existing thermal modeling of 3D ICs incorporating microfluidic cooling are: (1) the power map is either assumed uniform or not realistic. When a specific application runs on a chip, the power should be non-uniform; (2) the

coupling effect between power and thermal is not included. Increased temperature could lead to higher consumption of power, due to increased leakage power. The leakage power raises the temperature further. So it is important to include the temperature dependent leakage power in the thermal model. For the experiment, there is no experiment demonstrating the advantage of microfluidic cooling in terms of temperature and leakage power reduction.

For the two-phase convection cooling with micro pin arrays, several studies exist for single fluids using water, R-123, or HFE-7200. Flow boiling of binary mixtures in micro-scale geometries has received little research attention so far. Changes in mixture properties with concentration might play an important role in boiling heat transfer in mixtures. The addition of another liquid can change the contact angle and wetting characteristics of the mixture. In the boiling of binary mixtures, evaporation of the more volatile component from the liquid-vapor interface is more intensive near the heating surface, and hence, concentration of the more volatile component in the liquid phase adjacent to the interface decreases toward the heating surface. This yields a surface tension gradient according to the concentration distribution along the liquid-vapor interface. So more volatile component with lower surface tension may cause CHF enhancement.

CHAPTER 3

DESIGN AND FABRICATION OF PIN FIN ENHANCED MICROGAP AND EXPERIMENTAL TEST FLOW LOOP

To study the characteristics of pin fin enhanced microgaps, device, package and test flow loop are required. This chapter introduces the design and fabrication of pin fin enhanced microgap, package and experimental flow loop and discusses the challenges of the fabrication.

3.1 Mask Design

The pin fin enhanced microgaps includes staggered pin fin arrays, fluidic ports, heaters and temperature sensor, and electrical pads for wirebonding, each of which requires a mask. Figure 3.1 shows the layout of the gap with staggered pin fin array. Six devices are placed on a 4 inch wafer. The 1 cm × 1 cm staggered pin fin array is placed at the middle of the device. Six pins with diameter 200 um are used for structural support of the gap. Two pressure ports are designed to measure the pressure before and after the pin fin array. Also two fluidic ports serve as fluidic inlet and outlet. These ports are fabricated with a separate mask.

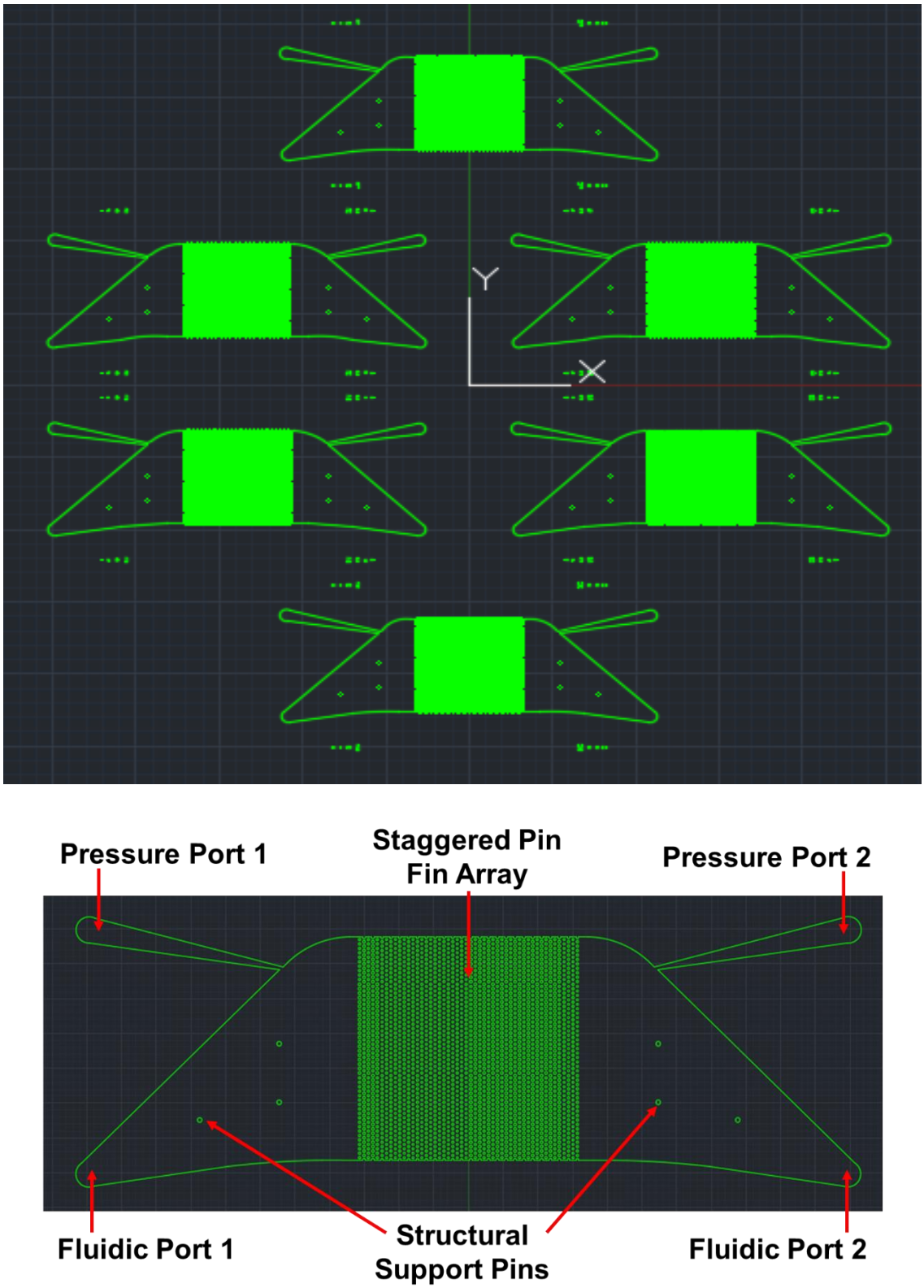


Figure 3.1: Mask design for the microgaps with staggered pin fin arrays on a 4” wafer.

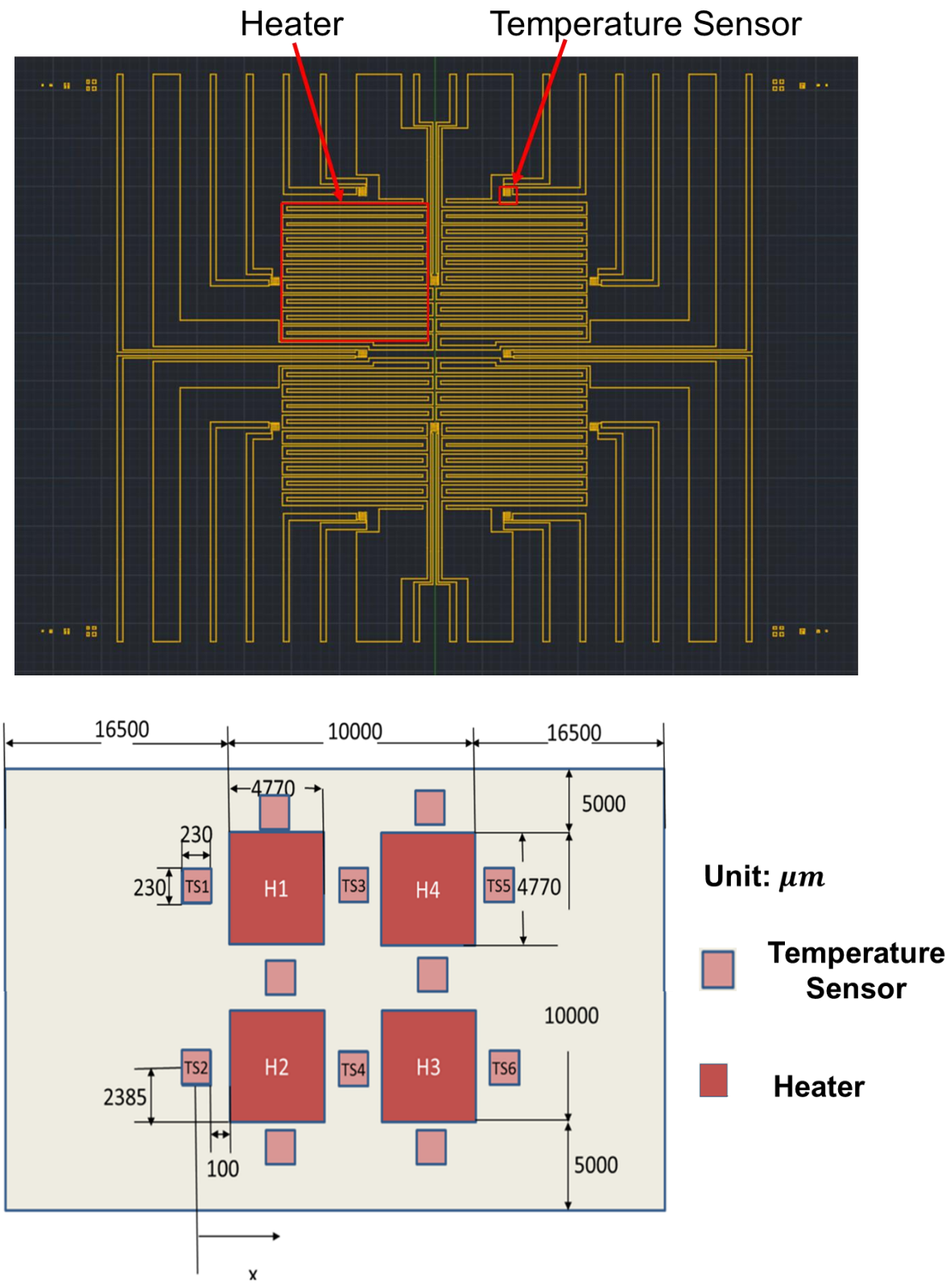


Figure 3.2: Mask design and schematic of the 4 heaters and 12 temperature sensors.

Figure 3.2 shows the schematic and design of the heaters and temperature sensors. There are 4 heaters and 12 temperature sensors around the heaters to measure the temperatures at different locations. Both are serpentine structures and are made of Pt or Ni, for which the resistance changes linearly with temperature. The heaters are aligned with the staggered pin fin array.

Figure 3.3 shows the mask design of the electrical pads for heaters and temperature sensors. The electrical pads mask overlaps pads on the heaters and temperature sensors in Figure 3.2 to make sure most of the resistance is due to the serpentine structure. Thus very little heat is generated in the electrical pads. They are wirebonded to PCB to provide electrical connection.

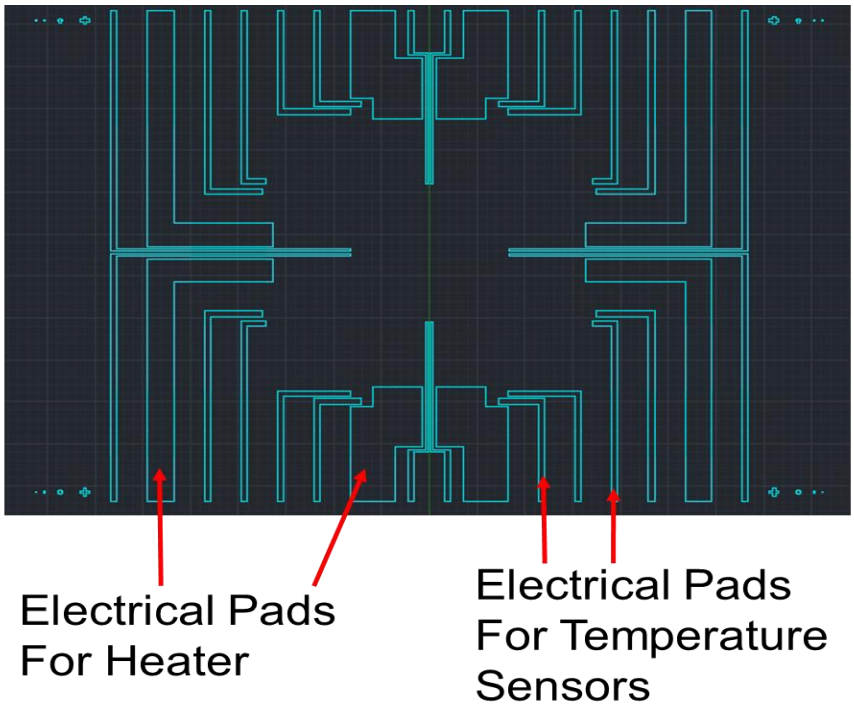


Figure 3.3: Electrical pads for heaters and temperature sensors.

3.2 Fabrication Procedure

The pin fin enhanced microgap fabrication process starts with a double-side polished 4" silicon wafer with a thickness 500 μm (Figure 3.4). In the first step, a 2 μm thickness silicon oxide layer is deposited by Plasma Enhanced Chemical Vapor Deposition (PECVD) using Oxford PECVD, as an insulation layer. Then 0.2 μm thick platinum serpentine structure is deposited using evaporator with 0.03 μm thick titannium as adhesion layer. There are two kinds of serpentine structures: 4 as heaters, and 12 as resistive temperature sensors. A 0.5 μm copper layer is deposited as electrical pads with 0.03 um thick titanium as adhesion layer. In the next step, the wafer is taken through a photolithography step and a Reactive Ion Etching (RIE) process to remove the oxide and expose the silicon, which is etched to form the inlet, outlet, and fluid vias using the standard Bosch process in STS ICP, which alternates between a plasma etching step and passivation step. Then the wafer is flipped over, positive photoresist SPR-220 is spun and exposed to form a mask for the microgap. Then the wafer is etched using the Bosch process, and the deep microgap cavity with staggered micropin fin arrays is etched. Tencor P15 profilometer is used to measure the depth of the microgap. Thereafter, the processed wafer is bonded with a 700 μm thick Pyrex (glass) wafer using SB6 anodic bonder, and the microgap samples are diced from the wafer using dicing saw. Figure 3.5 shows the top and bottom views of the fabricated device, and the SEM image of the staggered pin fin arrays. The dimensions of the fabricated device are 43 mm x 20 mm. The pin fin array is 1 cm by 1 cm. The microgap includes pressure ports and fluid inlet and outlet, where fluid temperature and pressure can be measured. The micropin fin array sample is placed into a package which provides protection, heat insulation and fluid interconnection.

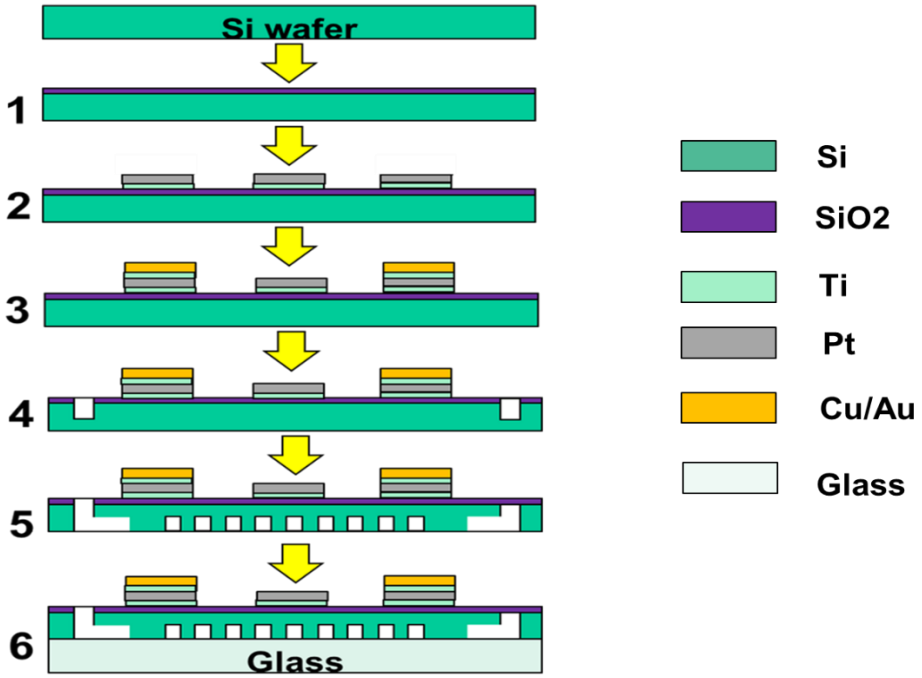
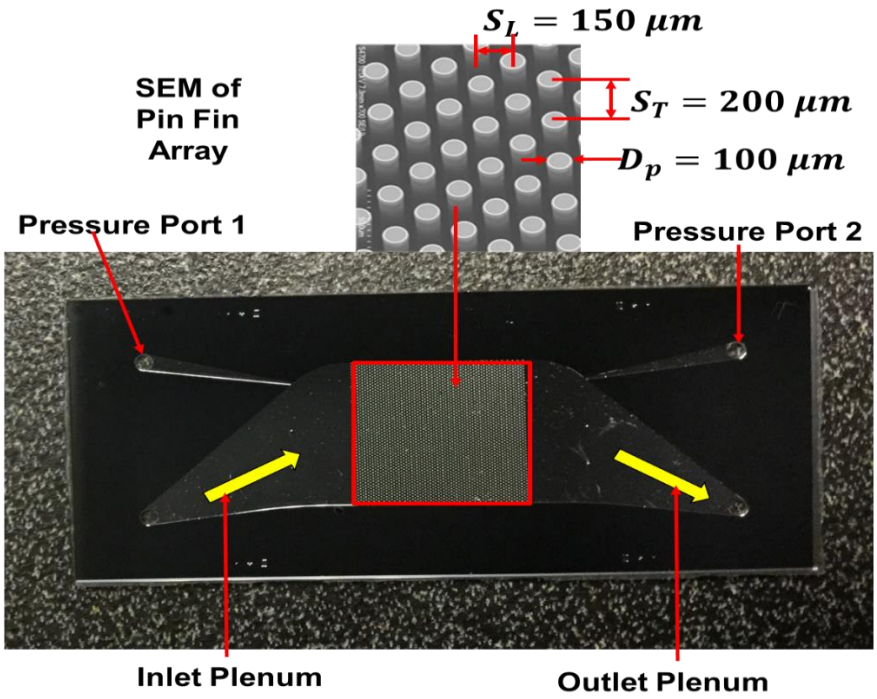
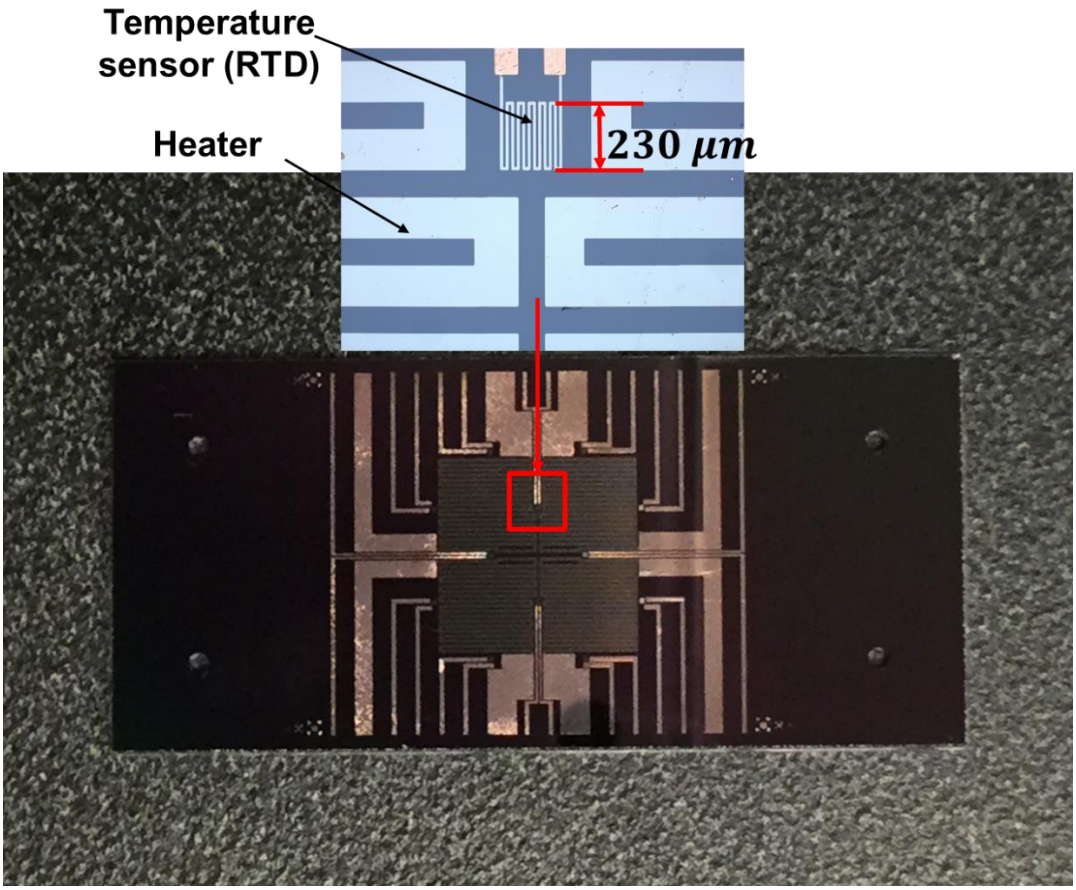


Figure 3.4: Fabrication process for pin fin enhanced microgaps.



(a)

Figure 3.5: (a) Top view of the pin fin enhanced microgaps and scanning electron microscope (SEM) image of pin fin arrays, (b) Bottom view of the fabricated device.



(b)

Figure 3.5 continued.

3.3 Fabrication Challenges

The fabrication of the pin fin enhanced microgaps presents multiple challenges. The first comes from the fabrication procedure. In the present study, the fabrication is conducted in the order of oxidation, metallization, etching, and bonding. An alternative way is to do etching of the microgap first, then anodic bonding, oxidation, metallization, and lastly etching of the through hole. However, the oxidation process is a high temperature process with temperature up to 300℃. The bond is easily cracked due to the high temperature and mismatch of coefficients of thermal expansion between silicon and glass. An alternative way is to do the fabrication in the order of oxidation, etching, anodic

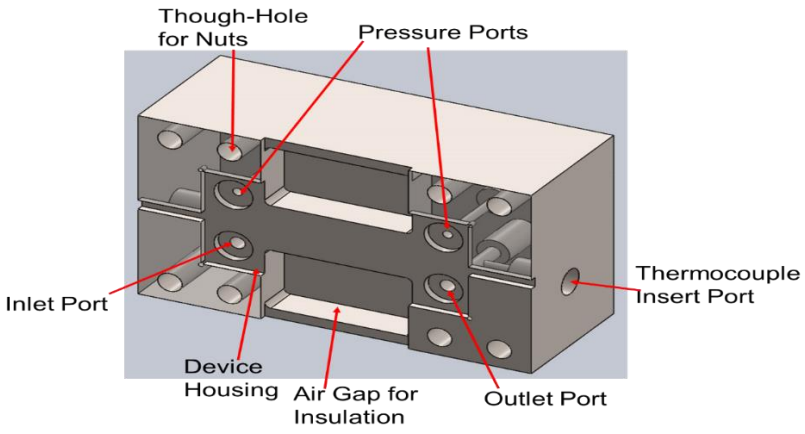
bonding, metallization, through-hole etching. This can avoid the high temperature process after the bonding. However, with the glass bonded with the Si wafer, the glass can block the heat transfer in the baking step of photolithography, which results in low quality of metallization.

To make sure the metal layer sticks to the device strongly, high qualities of the photolithography and exposure are required. So the baking time, baking temperature, exposure dose, and develop time need to be carefully monitored and controlled. Before the metallization using the e-beam evaporator, at least 2 min descum process is needed to make sure the residual of photoresist after the development is completely removed. Usually the photoresist pattern after the descum process needs to be examined under microscope. Similar procedures need to be followed when etching the pin fin array.

The reliability of the device depends on reliable bonding between the Si wafer and glass wafer. The surface must be carefully cleaned to remove particles contaminants before bonding. Usually, the wafer is cleaned by immersion into concentrated H_2SO_4 and H_2O_2. However, metal layers can be etched by the acid. So a 1 hour descum process is conducted by Oxford Endpoint RIE to clean the residual instead of using acid cleaning. An examination under microscope is followed to make sure that there are no visible particles on the wafer. In the current design, the bonding interface is smaller compared to the gap. So the tool pressure is set as high as 3 bar during the bonding process to make sure the bonding between the Si and glass is strong enough. The maximum pressure the device experiences can reach up to 4 bar absolute.

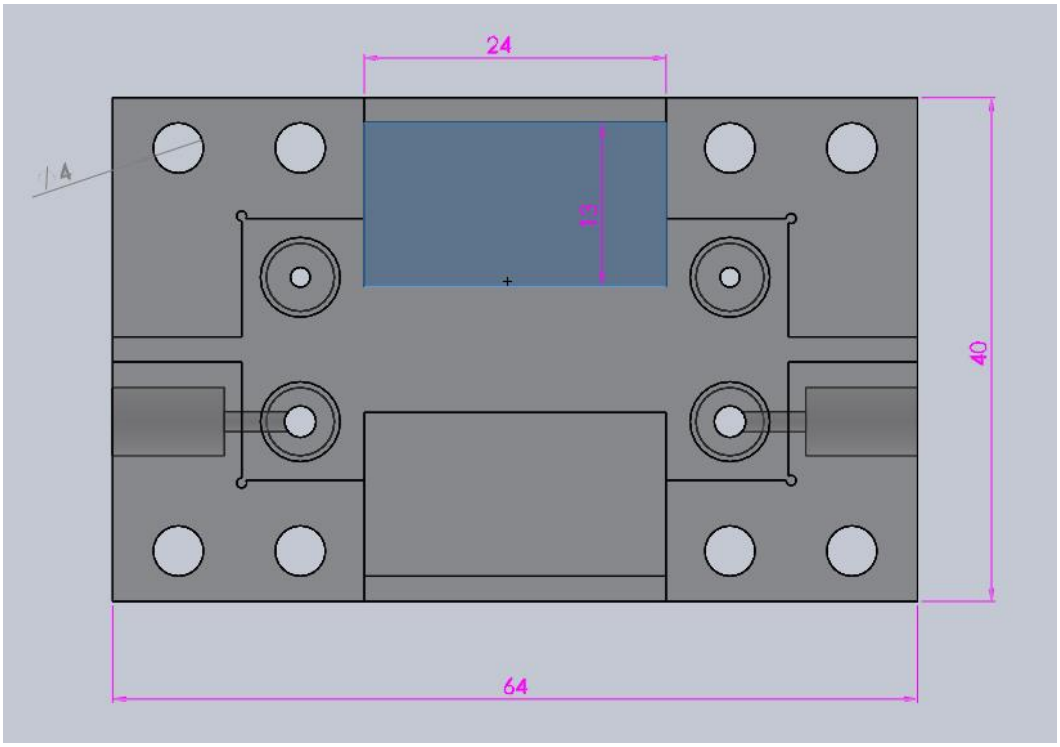
3.4 Microgap Package and PCB Design

A reliable package is needed to provide housing, insulation, sealing, and reliable fluidic interconnection. The package is made of Polyether ether ketone (PEEK). PEEK is chosen due to its excellent mechanical, chemical resistance properties, good insulation property (thermal conductivity 0.25 W/mK) and ability to withstand high temperature (melting point about 343℃). The length of the package is 6.4 cm, width 4 cm and height 2.5 cm. Figure 3.6 (a) shows the isometric view of the package. A 1.2 mm deep cavity is made to provide housing for the microgap device since the thickness of the Si wafer is 500 μm and glass wafer 700 μm. Four holes are drilled through the cavity to provide fluidic connections for inlet, outlet and pressure ports. O-rings are used for sealing. Copper tubes of 3.175mm diameter are used for fluidic connection of the package to the flow loop. Eight through-package holes are drilled for alignment with the PCB and connection with nuts. To measure the inlet and outlet fluid temperatures, 2 holes are drilled on the sides (Figure 3.6 (c)). T-type thermocouples are inserted into those holes to measure the fluid temperatures.

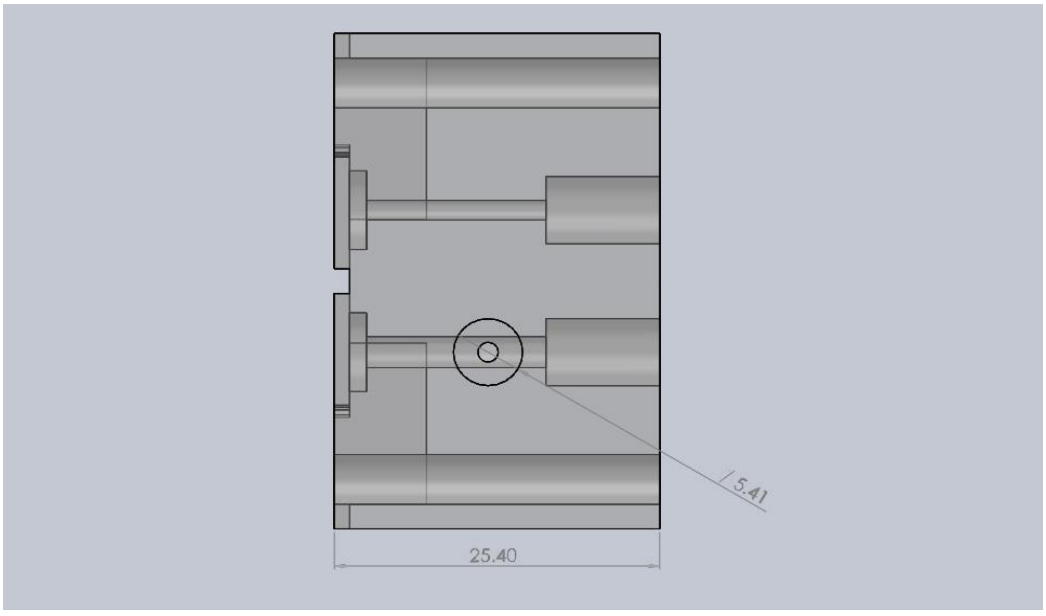


(a)

Figure 3.6: CAD drawing of package, unit: mm (a) Isometric view, (b) Top view, (c) Side view.



(b)



(c)

Figure 3.6 continued.

Figure 3.7 shows the design of PCB using CircuitCAM software. The dimension of the PCB is 8.3 cm × 7cm. The spacing of the pad is the same as that of the heaters. A 1.8 cm × 1.2 cm window is opened at the middle for visualization.

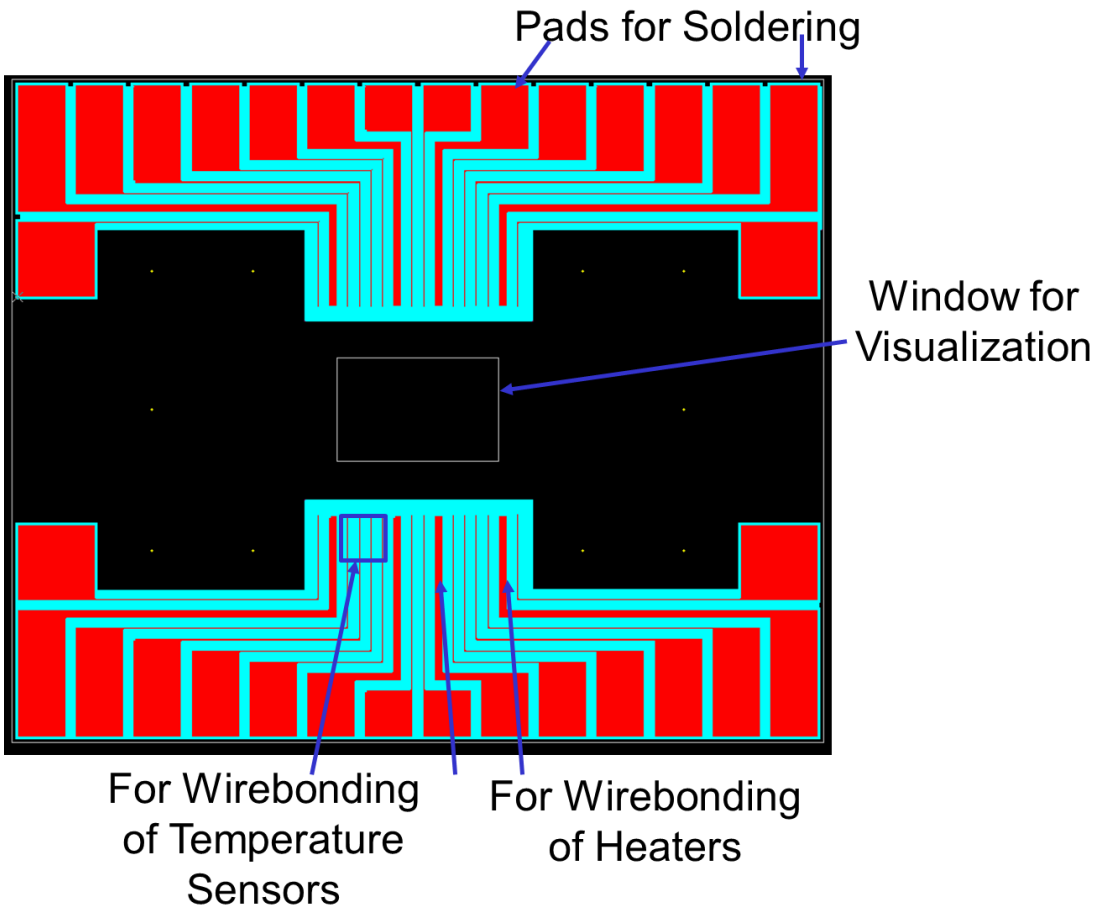
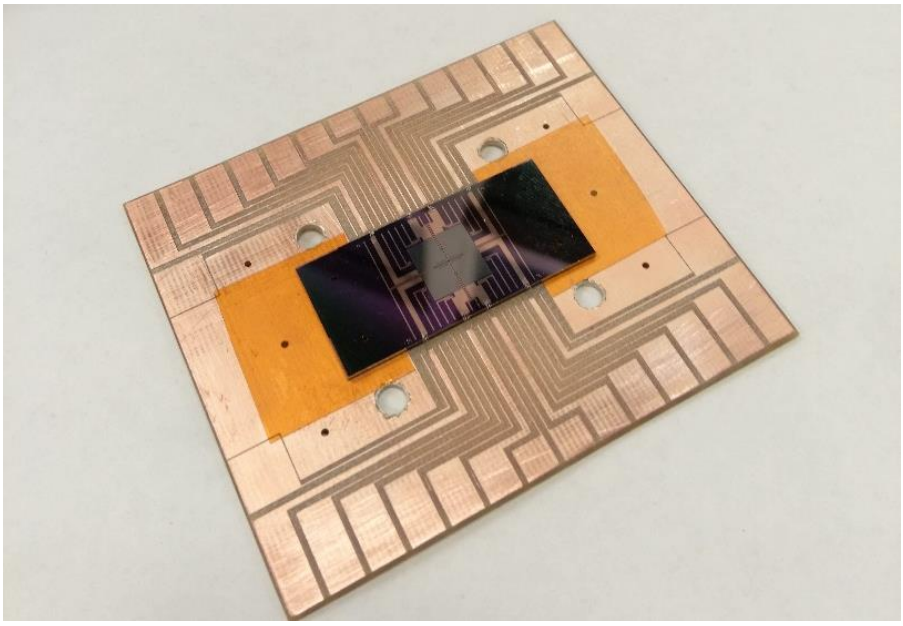


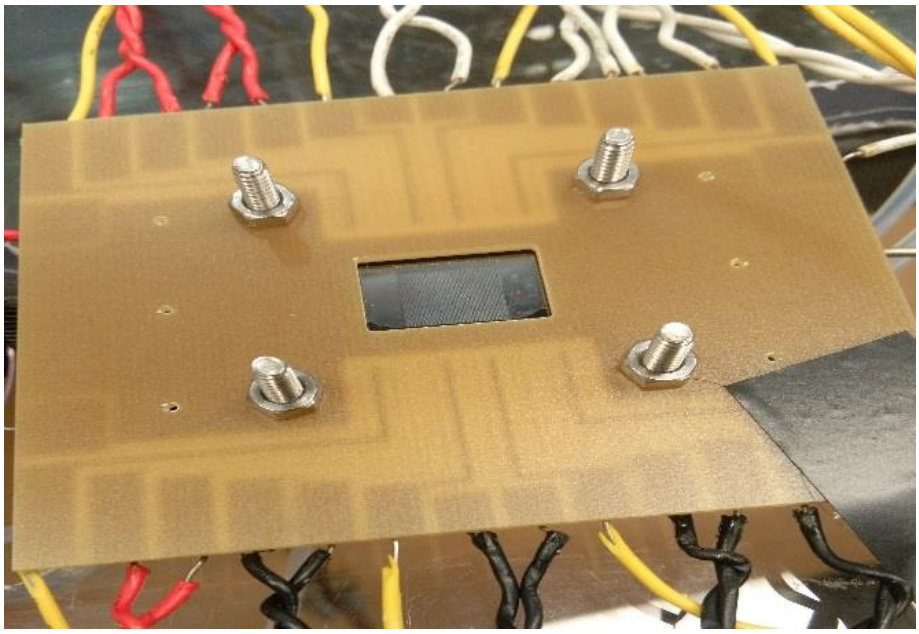
Figure 3.7: Design of PCB illustrating the pads for soldering and wirebonding.

The device is aligned and fixed on the PCB by double sided tape. Then wirebonding is done using a semi-automatic wire bonder from West Bond, Inc. There are 10 wirebonds for each interconnection from the device to PCB for heaters to make sure the wirebonds can stand high voltage and current. For temperature sensors, only 2 wirebonds are done. Before the experiment, the temperature sensors are calibrated in a controlled temperature

oven. The PCB is flipped, aligned and connected to the package by nuts (Figure 3.8) to form a tight sealing for the device.



(a)



(b)

Figure 3.8: Assembly of device, package, and PCB (a) Device attached on PCB by double side tape, (b) PCB flipped and locked with package by nuts.

3.5 Flow Loop Design

A flow loop was built to test the thermal performance of single phase cooling of pin fin enhanced microgap. Figure 3.9 shows the experimental setup. It consists of pump, controlled temperature bath, flow meter, filter, metering valve, solid state pressure transducer (Omega^{TM} PX219), fine gage thermocouple (Omega^{TM} TMQSS-062E-6), micropin fin arrays with the package, air cooled heatsink, and 1000 ml stainless steel reservoir. Cole-Parmer digital gear pump (Model No. 75211-30) provides flow rates from 5.52 ml/min to 331.2 ml/min through the microgap. A controlled temperature bath (LAUDA RM6) is used to control the fluid temperature at the inlet of the microgap. A calibrated McMillan S-114 flow meter is used to measure the volumetric flow rate. A Swagelok filter (pore size 15 μm) is used to keep the inlet water clean and prevent clogging of the microgap. A metering valve (SS-1RS4) is used to adjust the flow rate. An air-cooled heatsink is used to cool down the fluid from the exit of the microgap. The reservoir is open to atmosphere. All the tubing is 6.35 mm diameter stainless steel tube. Agilent N5752A DC power supply (600V/1.3A) is used to provide power to the heaters. Agilent E3620A dual output DC power supply (25V/1A) is used to provide power to the pressure transducer. Agilent 34970A data acquisition unit with 20 channel multiplex is used to record the data from pressure transducer, thermocouples, flowmeter, temperature sensors, and power supply.

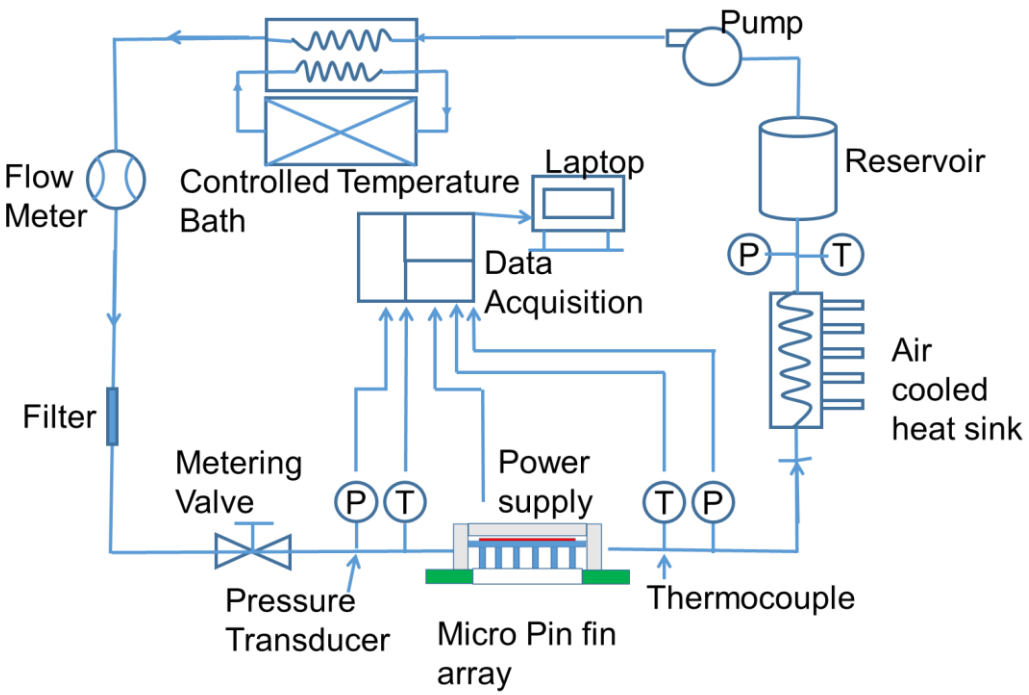


Figure 3.9: Flow loop for single phase cooling.

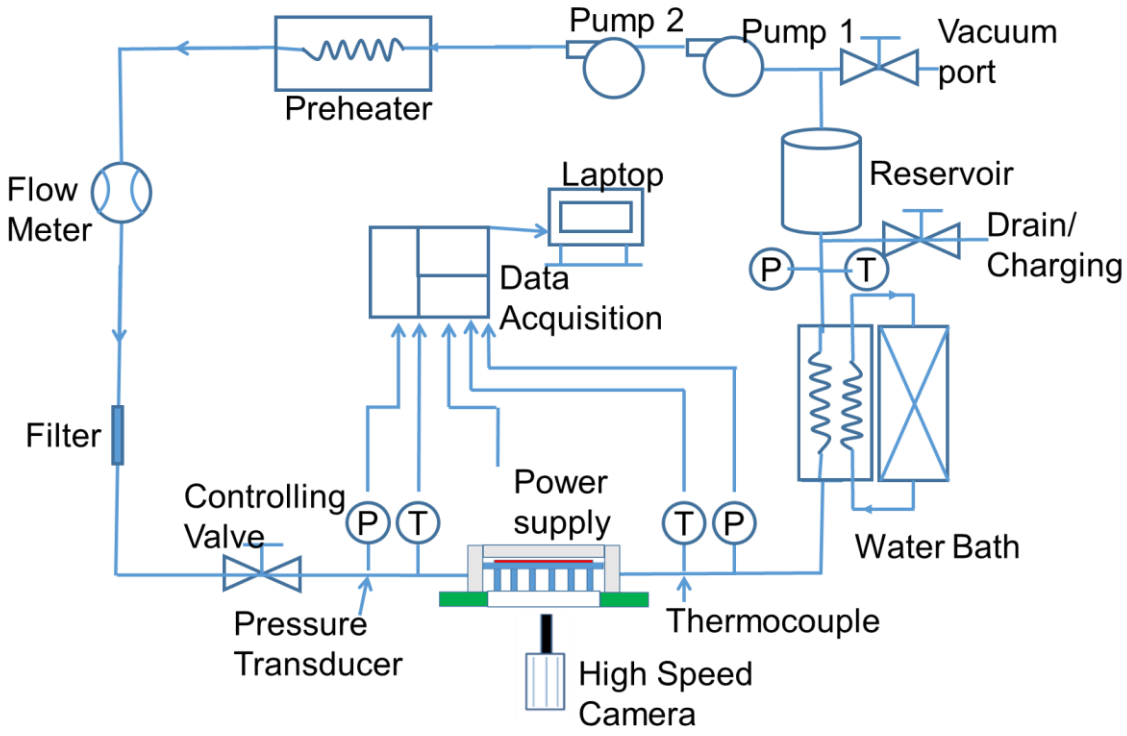


Figure 3.10: Flow loop for two phase cooling.

Due to the complexity of two phase cooling, the previous single phase flow loop is modified to meet the requirement of two phase cooling (Figure 3.10). A high speed camera (Phantom V211) is used to capture the boiling in the test section. To suppress the two phase flow instability, a high pressure drop right before the test section is needed. This is achieved by adding one more pump to elevate the pressure, while throttling the controlling valve [80] right before the test section. So a high pressure drop across the controlling valve is generated. The water bath is moved right after the test section and its temperature is set as 1 degC. The vapor inside the test section elevates the pressure inside the device significantly. The low temperature in the water bath is used to make sure the vapor is condensed back to liquid completely and quickly before it enters the reservoir. The two phase flow loop is a closed system. So a vacuum port and a drain port are added.

Figure 3.11 shows the electrical circuit for the heaters. Each heater is connected with precision resistor (1 ± 0.01 ohm) and the DC power supply. The precision resistors are connected into the circuit by solder. So about 0.05 ohm resistance is added to each resistor. This additional resistance is also checked by multimeter. When calculating the current through the heaters, these additional resistances need to be included. The power consumption of the precision resistors is negligible since the heater resistance is almost 500 times that of precision resistor. By measuring the total voltage across the power supply and the voltage across the precision resistor, the total power dissipation can be calculated as:

$$q_{tot} = V_{tot} * \left(\frac{V_{pr1}}{R_{pr1}} + \frac{V_{pr2}}{R_{pr2}} + \frac{V_{pr3}}{R_{pr3}} + \frac{V_{pr4}}{R_{pr4}}\right) \quad (3.1)$$

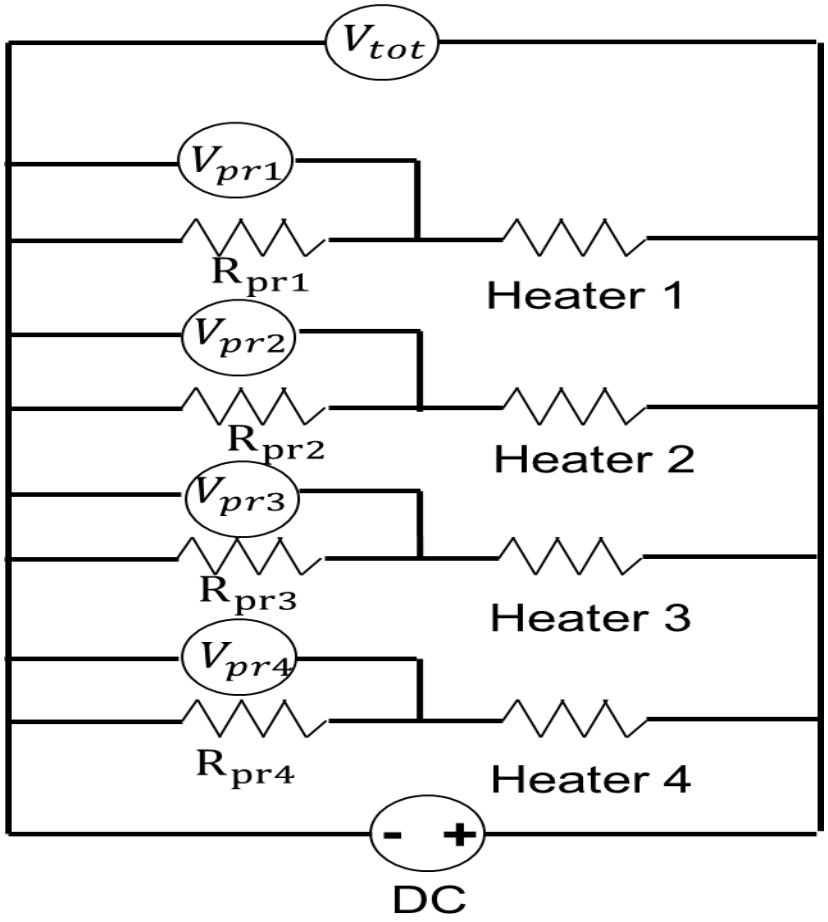


Figure 3.11: Circuit diagram illustrating the measurement of the power dissipation of the heaters.

3.6 Calibration and Measurement Uncertainty

The pressure transducers were calibrated using a pressure calibrator (Omega™ DPI620). The voltage and pressure reading were recorded and correlated. The uncertainty in the measurement of pressure is 0.25% of the full scale value (30 psi). The uncertainty of the T-type thermocouples is ± 0.5 ℃ [81]. The flowmeter was calibrated using standard bucket-stop watch method and the uncertainty is ± 0.2 ml/min. The microgap height measurement uncertainty is $\pm 6\%$.

To determine the temperature-resistance relationship, the temperature sensors were calibrated using an oven. A T-type thermocouple was attached to the device to measure the

surface temperature. The oven temperature was set to different values of temperature (20 ℃, 40 ℃, 60 ℃, 80 ℃, 100 ℃, 120 ℃, 135 ℃). All the chips during the experiment were calibrated by the above method. Figure 3.12 shows sample calibration curves. To make sure that the calibration curve does not change during the experiment, the temperature sensors were recalibrated after the experiments. For the devices used in the present study, the calibration curves were very stable. It was found that for some devices, the curves shifted for a few temperature sensors after experiments especially when the temperature was high (> 145 ℃). The mismatch of coefficients of thermal expansion between metal and silicon oxide layer at high temperature can lead to stress in the thin metal layer, which might cause irreversible structural changes. Before metallization, the silicon oxide surface must be cleaned to remove any particles of photoresist. The residual of photoresist between the metal and oxide layer can result in peel-off.

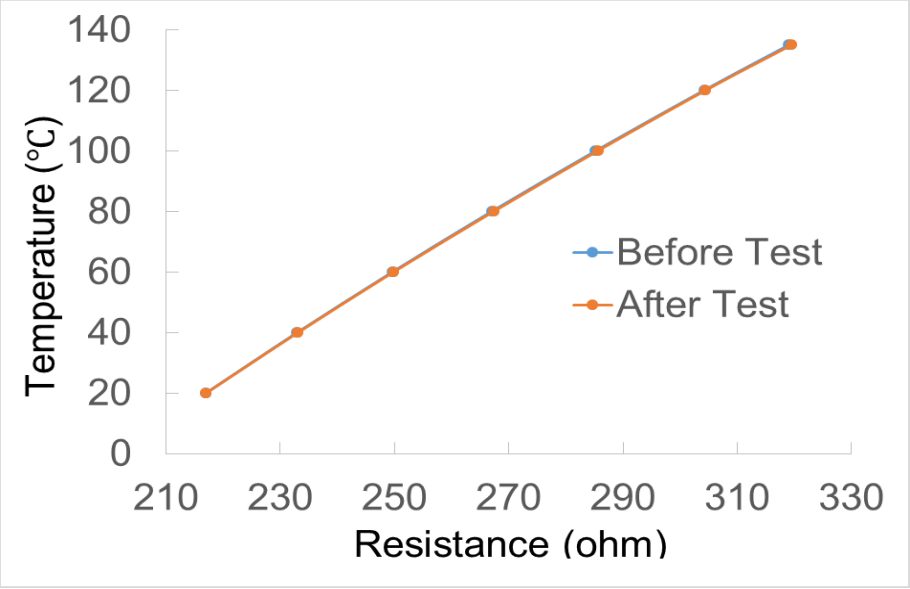


Figure 3.12: Temperature sensor calibration curve.

The uncertainty in the measurement of the total voltage and precision resistor voltage was 14.7 mV and 0.015 mV, the uncertainty of the resistance of precision resistor was 0.01

ohm. Following the uncertainty propagation procedure proposed by Kline and McClintock [82], the uncertainty of q_{tot} was 0.46%.

To estimate the heat loss to the ambient, the device was drained of fluid. Low power (0~5W) was applied to the heaters and the sensor resistance and power were recorded. The average temperature of the 12 temperature sensors was obtained for each power increment. A linear relationship between average temperature and heat loss was formed. The heat loss to the ambient was found to be less than 5.4% of the total power dissipation for all the experiments. So the effective power dissipation of the heaters was given by:

$$q_{eff} = q_{tot} - q_{loss} \tag{3.2}$$

3.7 Summary

In this chapter, the design and fabrication procedure of the pin fin enhanced microgaps, package, and PCB are presented. The challenges associated with the fabrication are discussed. The details of the experimental setup for both single phase and two phase cooling are described. The main observations of this chapter are as follows:

(1) The design and fabrication of pin fin enhanced microgaps is very challenging. Up to 4 masks are required in the present study. The tradeoff of different fabrication processes, and the recipe parameters need to be considered to produce a reliable device.

(2) The flow loop needs to be designed from by considering the entire system. The selections of the different components depend on parameters such as flow rate, and power.

(3) Compared to single phase flow, two phase flow loop is much more complicated. Flow instability is a significant concern in designing the two phase flow loop.

CHAPTER 4

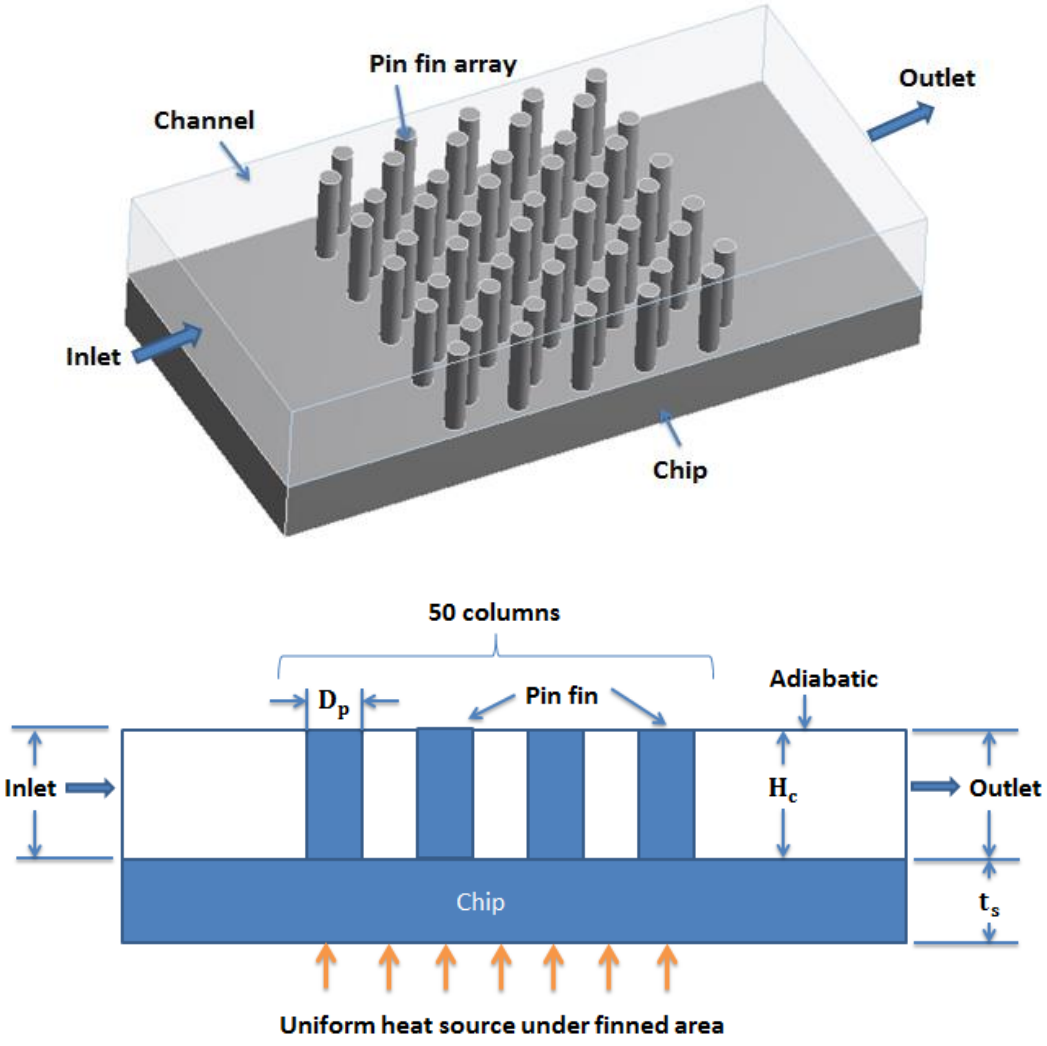
SINGLE PHASE CONVECTION IN PIN FIN ENHANCED MICROGAP

Microfluidic cooling with microgaps with surface area enhancements such as pin fins can potentially achieve superior thermal performance. As such, the hydraulic and thermal characteristics of this configuration over parametric ranges of practical interest are important. Numerical modeling is proved to be applicable for the study of this kind of structure [54]. In this chapter, the hydraulic and thermal characteristics of micro pin fin array with different dimensions in the range Re (22~357) were studied numerically. The numerical model was validated against experimental results. Then correlations for friction factor and Colburn j factor were proposed. Performance of circular and square pin fin arrays were compared.

4.1 Numerical Model

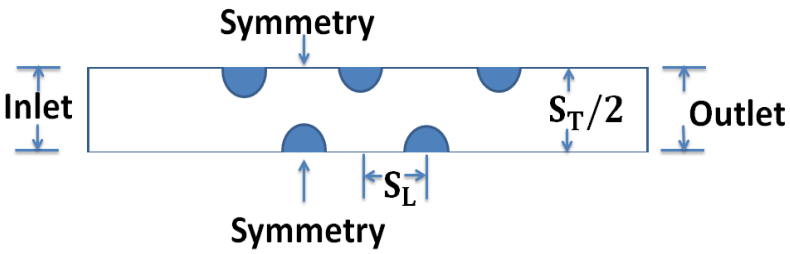
Figure 4.1(a) shows the schematic of the pin fin array. 50 columns of pin fins in the flow direction were modeled. The thickness of the chip base t_s was 100 μm in the model. In order to simplify the model and save calculation time, only part of the geometry (Figure 4.1(b)) were modeled using a symmetric boundary condition [83]. There was no gap between the pin tips and top wall. Number of pin fin columns in flow direction was still 50. The inlet boundary condition was constant normal velocity. The outlet boundary condition was specified ambient pressure. The pin surface, and the top and bottom walls of the channel used non-slip wall condition. A symmetry boundary condition was applied

between the pin fins. An inlet plenum was added to avoid the high pressure gradient at first pin fin, and outlet plenum was added to prevent back flow. For the thermal boundary conditions, a uniform heat source was applied under the finned area. The top wall of the channel was assumed adiabatic. The flow was assumed to be steady, incompressible and laminar [52]. Silicon was used as the chip material and DI water was used as the coolant. The inlet temperature was set as 25 ℃.



(a)

Figure 4.1: Schematic of staggered pin fin array model: (a) Full model, (b) Simplified model.



(b)

Figure 4.1 continued.

The flow was assumed steady state and laminar. Buoyancy force was assumed negligible. Material properties were constant. The basic governing equations were [84]:

Continuity equation:

$$\nabla \cdot (u) = 0 \tag{4.1}$$

Conservation of momentum:

$$\rho(u \cdot \nabla u) = -\nabla P + \mu \nabla^2 u \tag{4.2}$$

Conservation of energy:

$$\rho C_p (u \cdot \nabla T) = k \nabla^2 T \tag{4.3}$$

Table 4.1 shows the material properties used in the modeling. Water properties at 25 ℃ were used.

Table 4.1: Material properties of staggered pin fin array model.

Material	Density (kg/m^3)	Thermal conductivity (W/m-K)	Specific heat (J/kg-K)	Viscosity ($Pa \cdot s$)
Silicon	2330	149	707	
Water	997	0.5945	4183	0.0008936

Table 4.2 shows all the scope of the parametric study performed. The ratio of pin spacing to diameter, height to diameter varied from 2.25 to 1.5. The Re varied from 22 to 357.

Table 4.2: Summary of simulations performed**.**

$D_p(\mu m)$	$S_T(\mu m)$	$S_L(\mu m)$	$H_c(\mu m)$	Re
100	225	200	200	22~357
100	200	200	200	22~357
100	175	200	200	22~357
100	150	200	200	22~357
100	200	225	200	22~357
100	200	200	200	22~357
100	200	175	200	22~357
100	200	150	200	22~357
100	200	200	225	22~357
100	200	200	200	22~357
100	200	200	175	22~357
100	200	200	150	22~357

ANSYS Fluent was used for the modeling. An upwind scheme with SIMPLE algorithm [85] was applied to discretize and solve the governing equations. A sweep method was used to generate the structural mesh (Figure 4.2). Fine meshes were generated around the pin fins and near the top and bottom of the channel. The convergence criteria for the continuity, momentum and energy were residuals less than 10^{-6}.

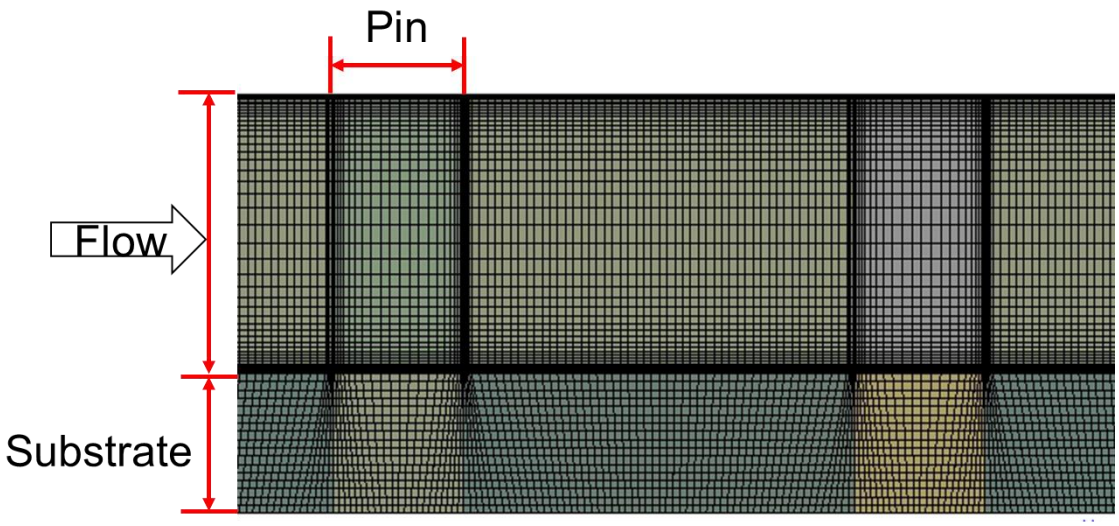


Figure 4.2: Front view of a section of the numerical mesh with a body size 6 μm.

For the mesh independence study, five different values were used. Table 4.3 shows that when number of elements increased from 2630k to 2900k, the pressure drop decreased only 0.33%. The bottom average temperature for the heat source area changed less than 0.01 K. So 2630k elements were used.

Table 4.3: Mesh independence study of the staggered pin fin array model**.**

Number of elements	Pressure drop (Pa)	Bottom average temp (K)
710k	25048	328.262
1080k	24471	328.397
1440k	24668	328.351
2630k	24361	328.353
2900k	24280	328.357

4.2 Data Reduction

Current literature uses either pin fin diameter (D_P) or hydraulic diameter (D_h) as the characteristic dimension in the definition of Re and f. In the present study the pin fin diameter was used. The Re was defined by:

$$\mathrm{Re} = \frac{\rho \cdot v_{max} \cdot D_p}{\mu} \tag{4.4}$$

For square pin fin array, D_p was defined as [52]:

$$D_p = \frac{4A_{pin}}{P_{pin}} \tag{4.5}$$

A_{pin} was the cross-sectional area of the pin,

$$A_{pin} = W_{pin} L_{pin} \tag{4.6}$$

where W_{pin} was the width of the pin and L_{pin} was the length of the pin. In this study $W_{pin} = L_{pin}$.

P_{pin} was the cross section perimeter of the pin,

$$P_{pin} = 2W_{pin} + 2L_{pin} \tag{4.7}$$

v_{max} was the maximum average velocity of the fluid between the pins [34]:

$$v_{max} = \frac{\dot{V}}{A_{min}} = \frac{\dot{V}}{H_c(W - D_P * N_T)} \tag{4.8}$$

where H_c was the height of channel. In this work, no clearance between the fin tip and top wall was considered. So the channel height H_c was equal to the pin fin height H_P. N_T was the number of pins in the transversal direction. And W was the chip width.

An equivalent fanning friction factor for pin fin structure was given by [37]

$$f = \frac{D_p \Delta P}{2L\rho v_{max}^2} \tag{4.9}$$

where ΔP was the pressure drop, and L was the chip length.

Nu was derived by a thermal resistance method [36]. An average heat transfer coefficient $\bar{h}$ was assumed to be the same for the finless area and finned area. Nu was then defined as:

$$Nu = \frac{\bar{h} \cdot D_p}{k_f} \tag{4.10}$$

where k_f was the thermal conductivity of the fluid.

Stanton number was defined by:

$$St = \frac{Nu}{RePr} = \frac{h}{\rho V_{max} C_p} \tag{4.11}$$

The Colburn j factor

$$j = StPr^{\frac{2}{3}} \tag{4.12}$$

The thermal resistance between the heating surface and the fluid was calculated as:

$$R = \frac{\Delta T}{Q} = \frac{T_{s,avg} - T_{f,avg}}{Q} \tag{4.13}$$

where Q was the total power applied on the heating surface, $T_{s,avg}$ was the average temperature of the heating surface, $T_{f,avg}$ was the average fluid temperature which was obtained by:

$$T_{f,avg} = \frac{T_{in} + T_{out}}{2} \tag{4.14}$$

T_{in} was the inlet fluid temperature and T_{out} was the outlet fluid temperature which could be calculated by:

$$Q = \dot{m} C_P (T_{out} - T_{in}) \tag{4.15}$$

where $\dot{m}$ was the mass flow rate and C_P was the specific heat of the fluid.

R consisted of two parts: R_{cond}, the conduction resistance through the silicon substrate, and R_{conv}, the convective thermal resistance.

$$R_{cond} = \frac{t_s}{k_s \cdot W \cdot L} \tag{4.16}$$

where t_s was the silicon substrate thickness, k_s was the thermal conductivity of silicon substrate, L was the longitudinal length of the chip. The convection resistance was defined by:

$$\text{Circular:} \quad R_{conv} = \frac{1}{\bar{h} \cdot A_{eff}} = \frac{1}{\bar{h} \cdot (W \cdot L - N_T N_L \frac{\pi D_P^2}{4} + \eta N_T N_L \pi D_P H_P)} \tag{4.17}$$

$$\text{Square:} \quad R_{conv} = \frac{1}{\bar{h} \cdot A_{eff}} = \frac{1}{\bar{h} \cdot (WL - N_L N_T W_{pin} L_{pin} + \eta N_L N_T * 2(W_{pin} + L_{pin}) H_P)} \tag{4.18}$$

where η was the fin efficiency which was given by [84]:

$$\eta = \frac{\tanh(mH_P)}{mH_P} \tag{4.19}$$

and m was [84]:

$$m = \sqrt{\frac{\bar{h} P_{pin}}{k_s A_{pin}}} \tag{4.20}$$

where P was the perimeter of the fin and A the cross-sectional area of the fin. In order to obtain $\bar{h}$, iterations were needed.

4.3 Model Validation with Experimental Results

The previous numerical model was validated against experimental results. The fabrication of microgaps and experimental setup are described in Chapter 3. The pump circulated the fluid through the controlled temperature bath which maintained the fluid temperature at the device inlet to be about 20 ℃. The loop was adjusted to get the desired inlet temperature and mass flowrate. The data was recorded at steady state. The inlet temperature was maintained at 20 ± 1℃. Re range was from 39 to 221. Two types of experiments were conducted: (1) pressure drop measurement without power, (2) pressure drop and temperature measurement with effective power input at $50\text{W} \pm 1$ W. A

symmetric model with the same inlet temperature, mass flowrate, power input, dimensions, materials were built at the same time.

For the experiments with power input, since the numerical model only considered half column of the pins, the average temperatures of $\frac{TS1+TS2}{2}, \frac{TS3+TS4}{2}, \frac{TS5+TS6}{2}$ from the experiment were compared with the predicted temperatures at the selected locations along the flow direction as shown in Figure 4.3.

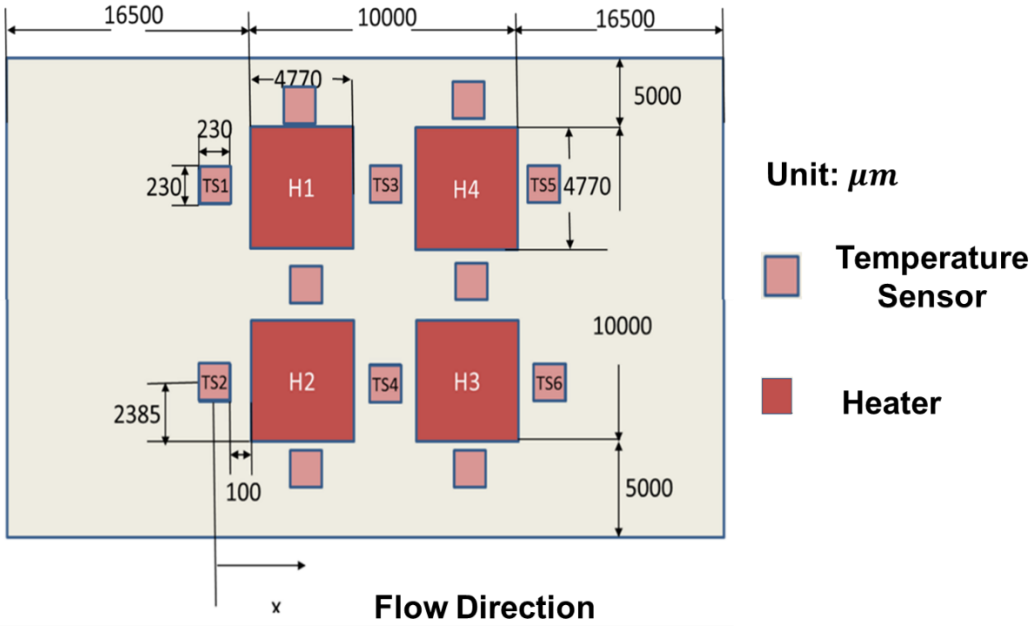


Figure 4.3: Schematic illustrating the location of temperature sensors.

The inlet velocity in the model was:

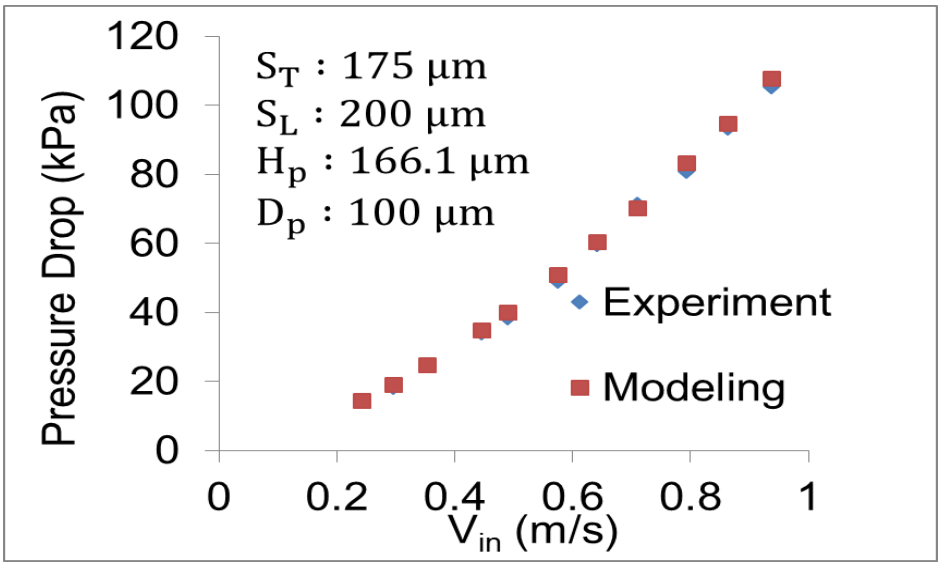
$$v_{in} = \frac{\dot{V}}{A_{in}} = \frac{\dot{V}}{0.01 * H_p} \tag{4.21}$$

where $\dot{V}$ was the volume flowrate measured from the flowmeter, and A_{in} the cross section area of the channel.

The mean absolute error (MAE) was defined as:

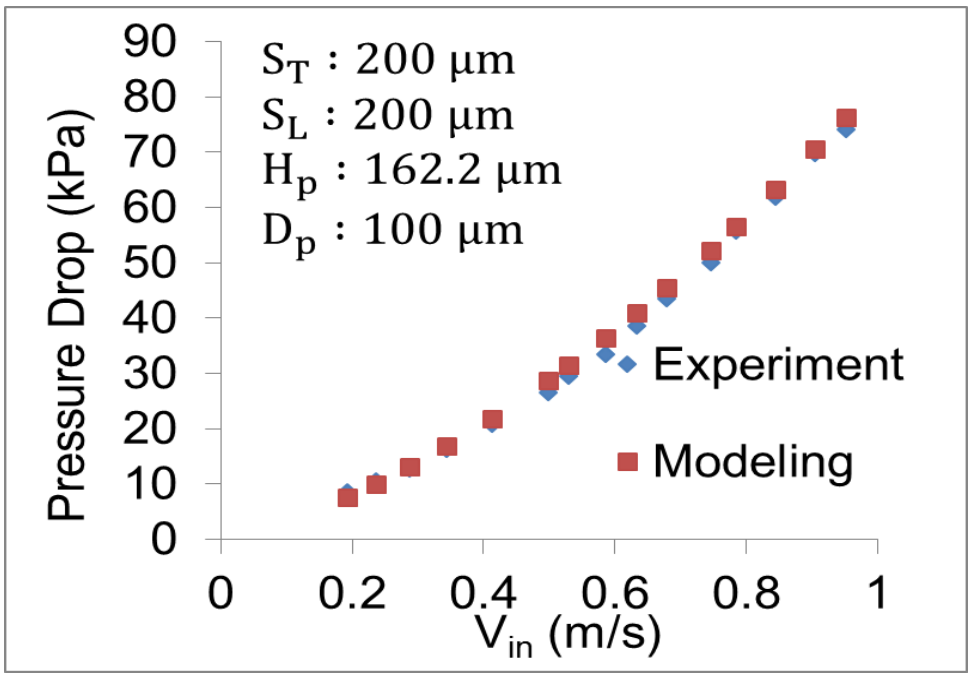
$$\text{MAE} = \frac{1}{N} \sum_1^N \left| \frac{\emptyset_{modeling} - \emptyset_{experiment}}{\emptyset_{experiment}} \right| \tag{4.22}$$

Figure 4.4 shows the pressure drop comparison between experiment and modeling at Re 39~221 with three different pin fin dimensions without power dissipation. Figure 4.5 and Figure 4.6 show the pressure drop and temperature at selected locations (beginning of pin arrays, middle of pin arrays, and end of pin arrays). In Figure 4.6 (a), there is a cross-over between modeling and experiment results, which might be due to the entrance geometry. The cross section of the inlet plenum expands along the flow direction, which cannot be captured by the simplified model. Overall, the comparison between the numerical and experimental data shows excellent agreement producing MAE of pressure 5%, and of temperature 2.9%. In the present study, the experiment was performed with Re lower than 221. As Re increases, the pressure inside the device also increases which can cause device failure. A good agreement between modeling and experiment was shown for Re<700 [54].

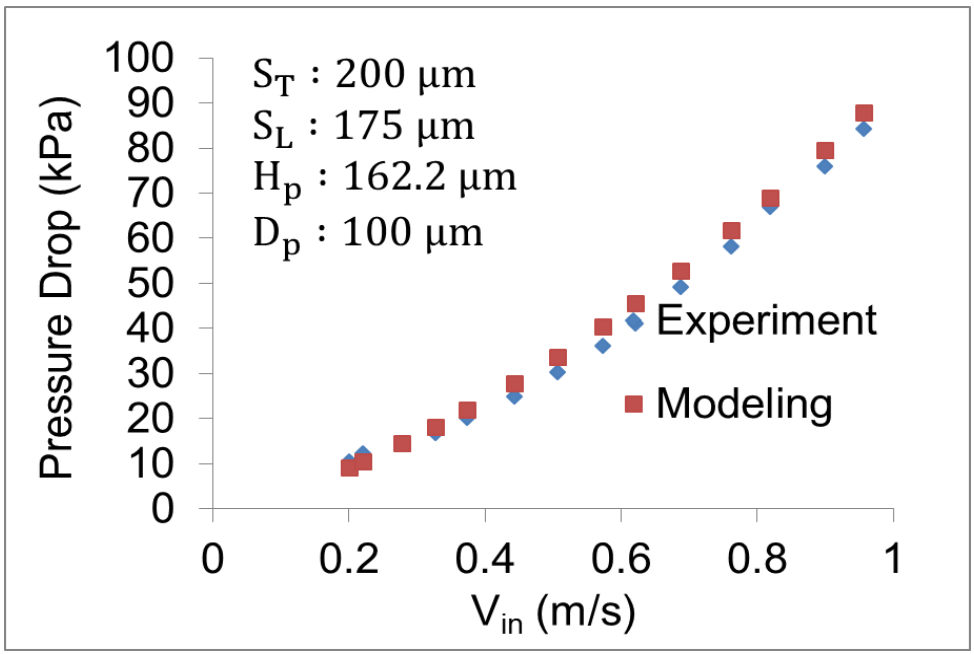


(a)

Figure 4.4: Pressure drop comparison between experiment and modeling without power input for three different pin dimensions.



(b)



(c)

Figure 4.4 continued.

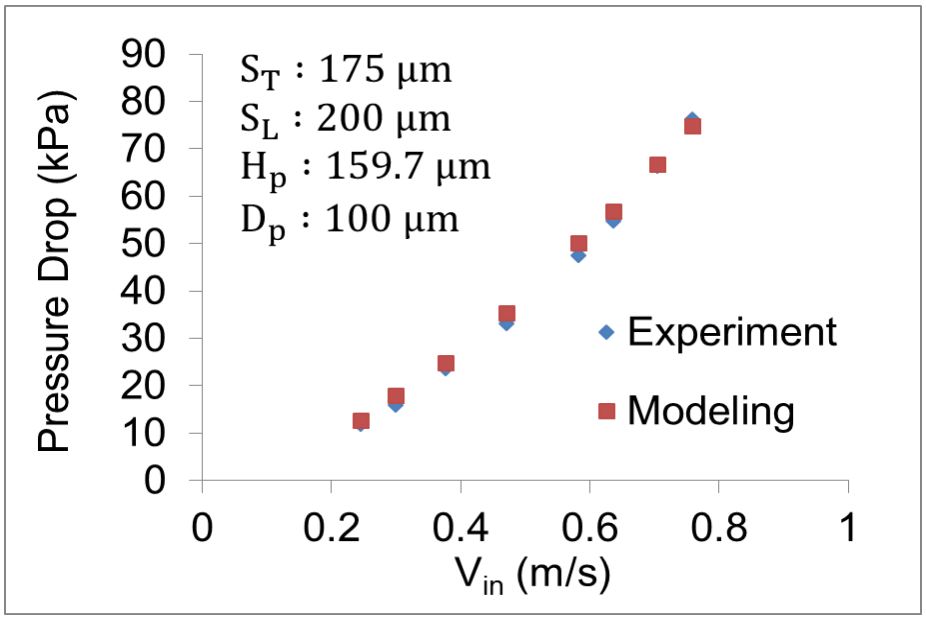
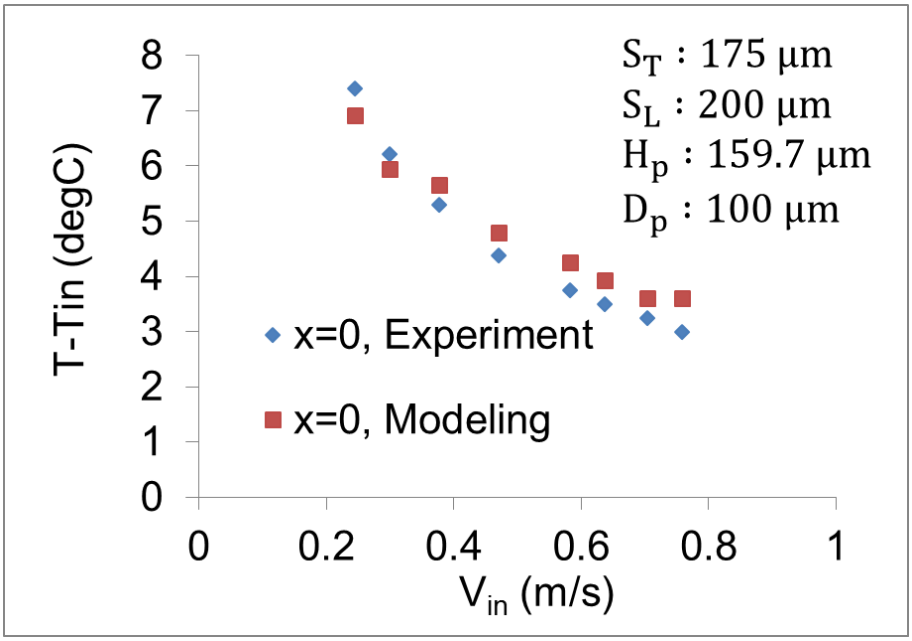
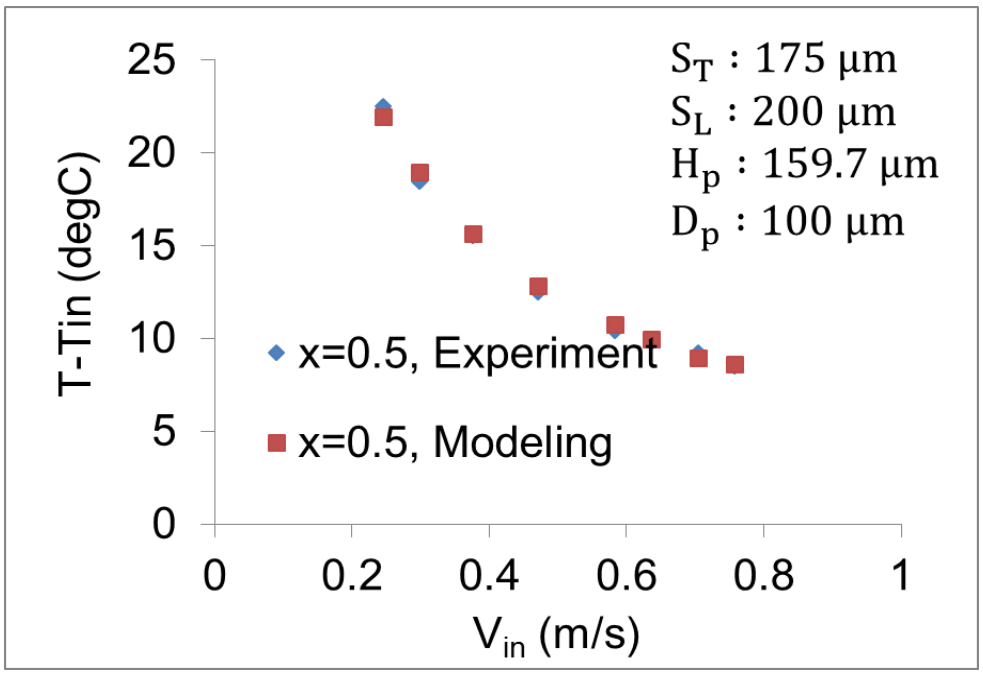


Figure 4.5: Pressure drop comparison between experiment and modeling at power input 50 W.

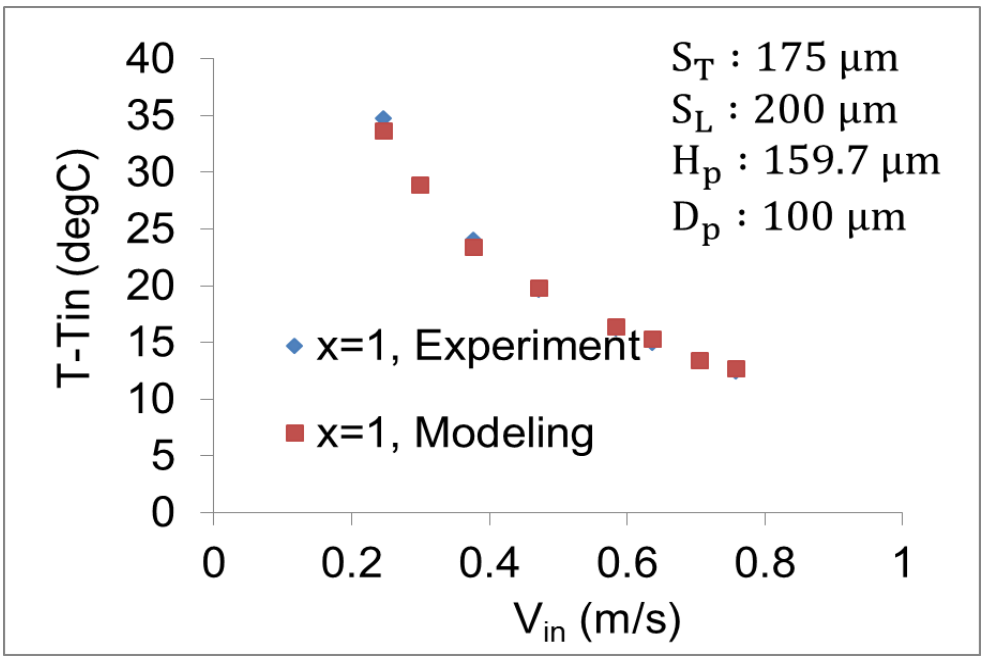


(a)

Figure 4.6: Temperature comparison between experiment and modeling at power input 50W for (a) $\frac{TS1+TS2}{2}$, (b) $\frac{TS3+TS4}{2}$, (c) $\frac{TS5+TS6}{2}$.



(b)



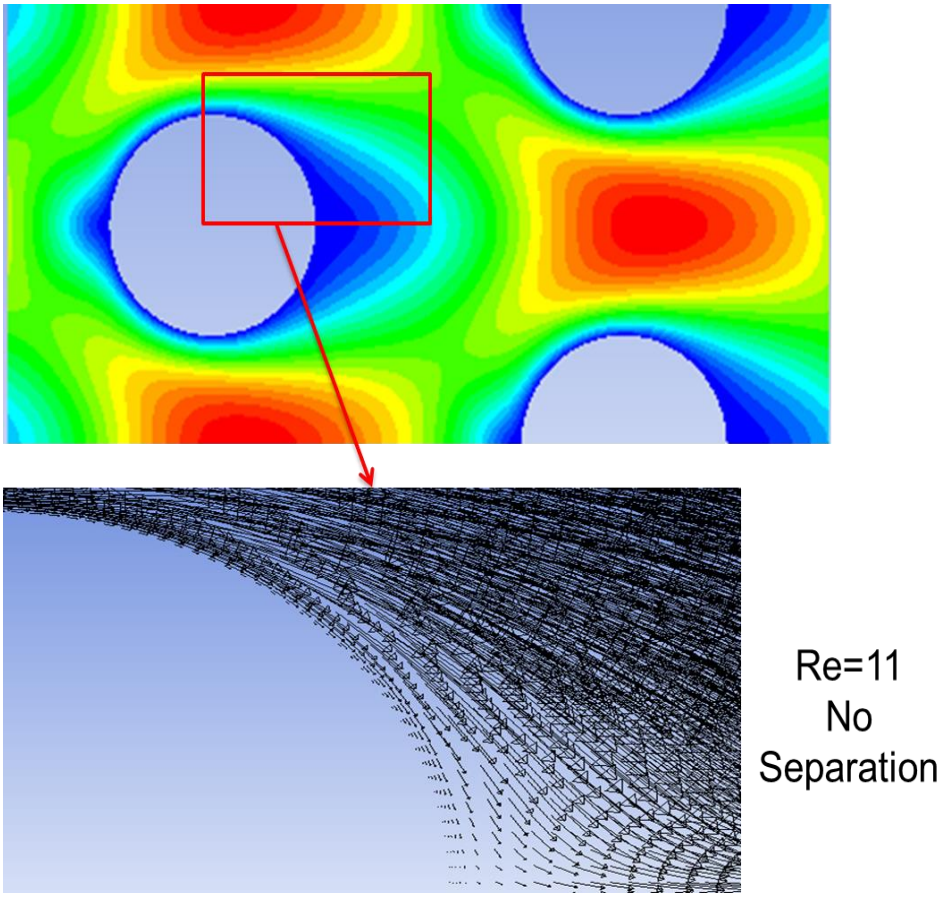
(c)

Figure 4.6 continued.

4.4 Parametric Study Results

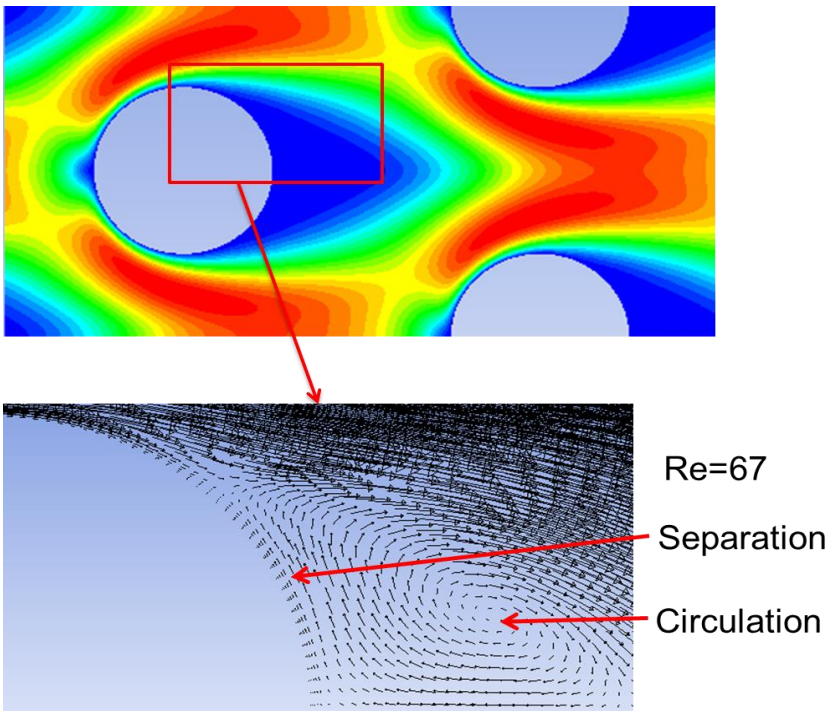
These existing correlations in Table 2.2 show different and even opposite trends of f with pin fin dimensions and Re. So the effect of pin fin dimensions and Re on f were studied by numerical modeling.

Figure 4.7 shows the velocity contour and vector plot around pins, as Re increased from 11 to 267.7. It can be seen that as the Re increased, the wake interaction increased and flow separation can be observed, which can affect both the pressure drop and heat transfer.

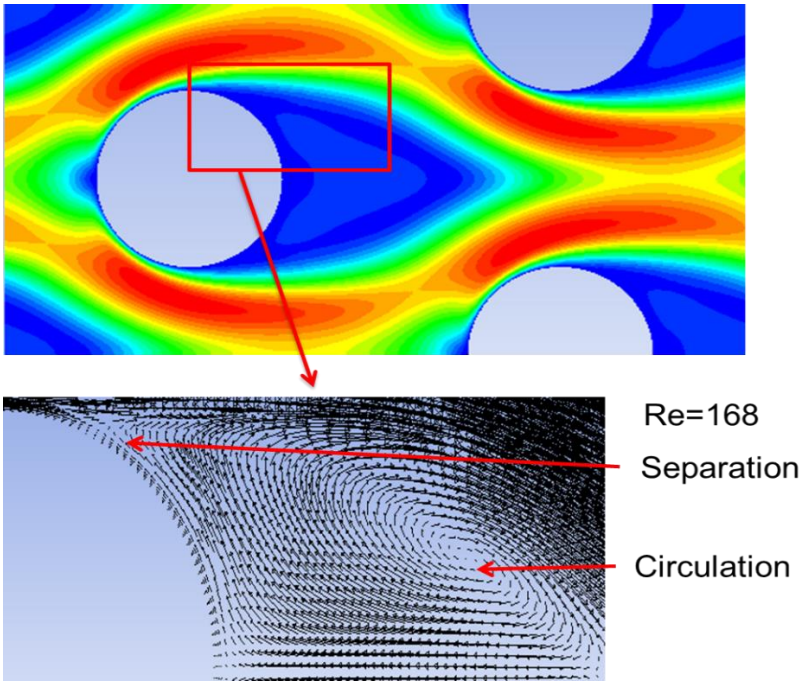


(a)

Figure 4.7: Velocity contours and vector showing the flow separation and circulation, (a) Re=11, (b) Re=67, (c) Re=168, (d) Re=267.7.

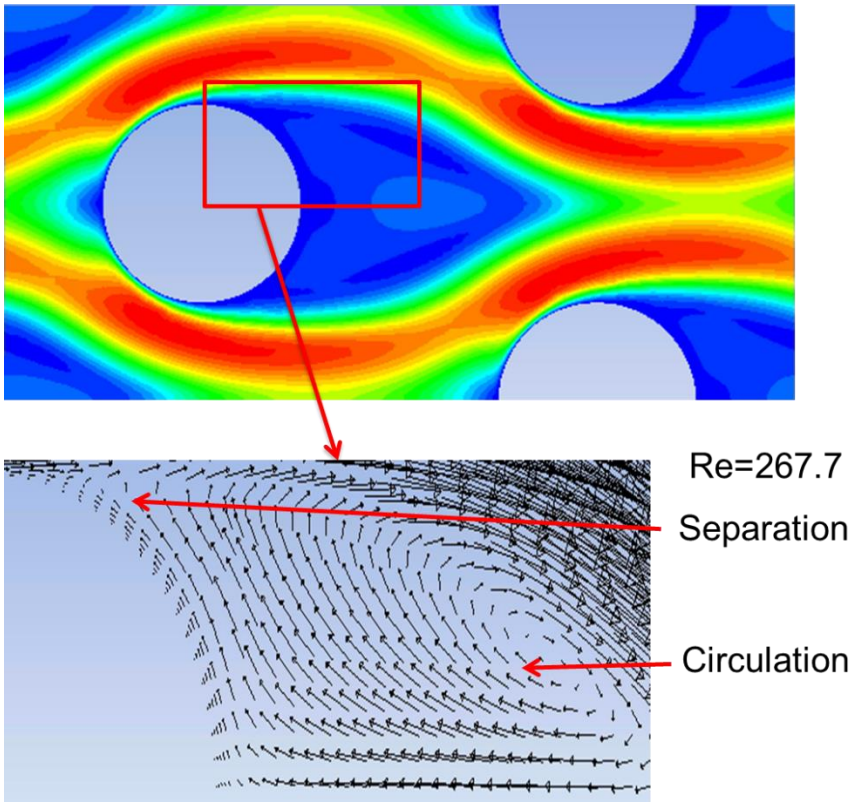


(b)



(c)

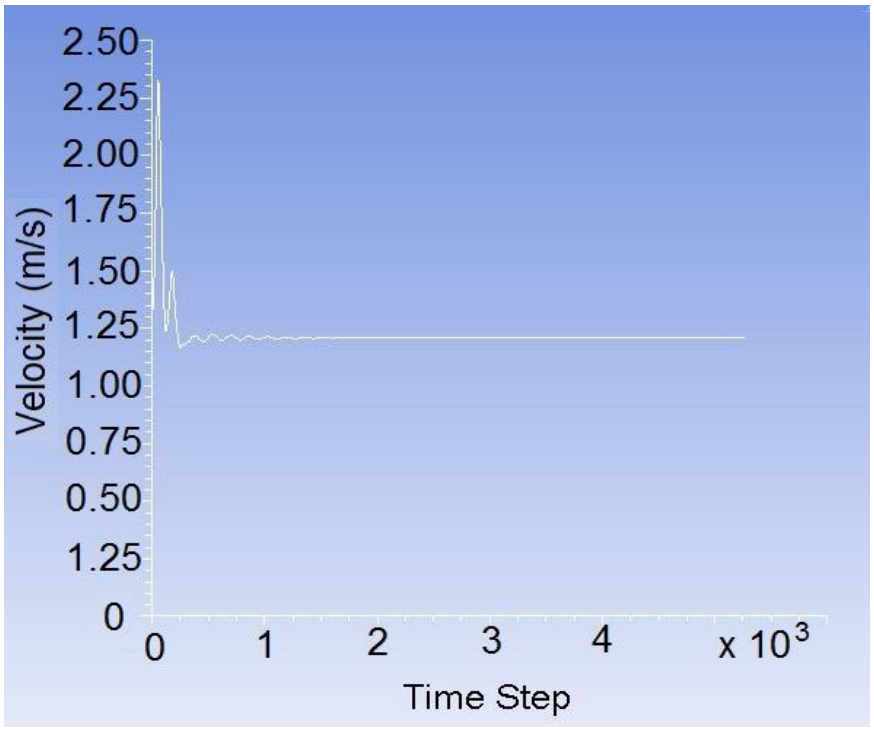
Figure 4.7 continued.



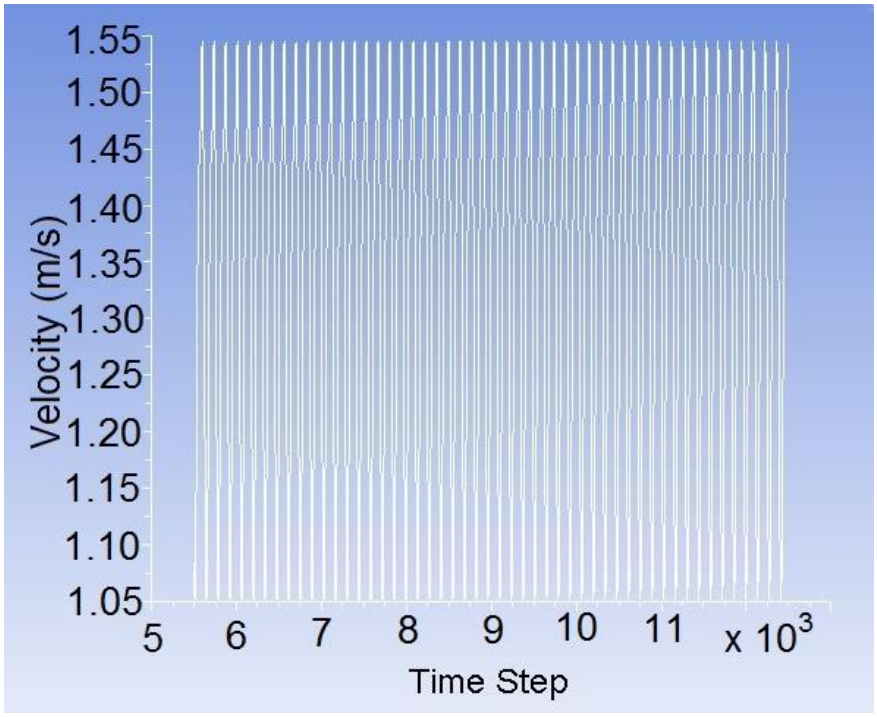
(d)

Figure 4.7 continued.

As Re continued to increase, the flow circulation became even stronger. Velocity fluctuations started to occur. Transient simulation was done to monitor the velocity at the center of the symmetric model with initial velocity as 0 and time step size 2 μs. Figure 4.8(a) shows that at Re 267.7 the velocity fluctuated initially and after certain time steps the fluctuation disappeared, which indicated that the flow became steady. However, at Re 312.4, the fluctuation continued and no steady state was reached as shown in Figure 4.8(b).



(a)



(b)

Figure 4.8: Velocity fluctuation at the center of the symmetric model, (a) Re=267.7, (b) Re=312.4.

Figure 4.9 shows the modeling results of f, which decreases as Re increases. At very low Re<30, f was very sensitive to Re. At high Re, it became less sensitive. The exponent relating f with Re decreased from -0.894 to -0.440. This could explain why the friction factor correlations in table 2.2 show different trend with Re. At low Re, the boundary layer was thick so increase of Re can cause a dramatic change of f. At high Re, the boundary layer was thinner. So further increase of Re did not affect f significantly. Prasher et al. [36] showed the trend change, however at much lower Re. Data in Moores and Joshi [47], Short et al. [37], and Tullius et al. [38] mostly fell in Re>100. Effects of Re with other dimensions were also studied.

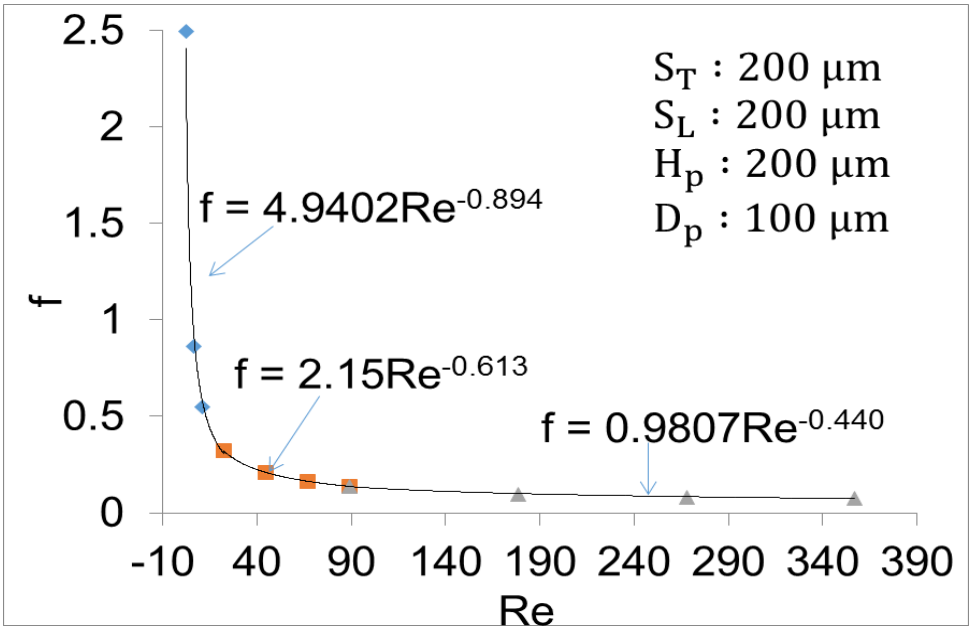


Figure 4.9: Friction factor versus Re.

In order to investigate the effect of ratio of pin fin height to diameter on the friction factor, the diameter, transversal and longitudinal spacing were kept fixed as seen in Table 4.2. Figure 4.10 shows that as the pin fin height decreased, f increased. This was because as the pin fin height decreased, the end wall effect became larger. This negative trend (f increases as pin fin height decreases) was also observed by Mita et al. [86] and Moores and

Joshi [47]. Prasher et al. [36] 's correlation at Re<100 showed a negative trend, but positive trend (f increases as pin height increases) at Re>100. In the present study, the trend was negative even at Re=357. Tullius et al. [38] showed a positive trend.

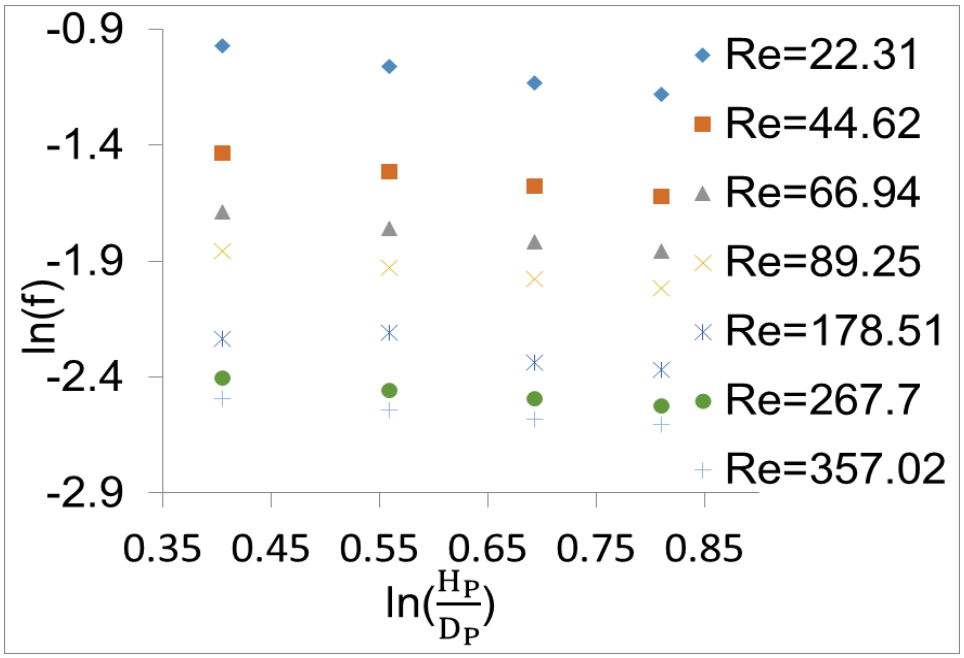


Figure 4.10: Friction factor versus ratio of pin fin height to pin diameter.

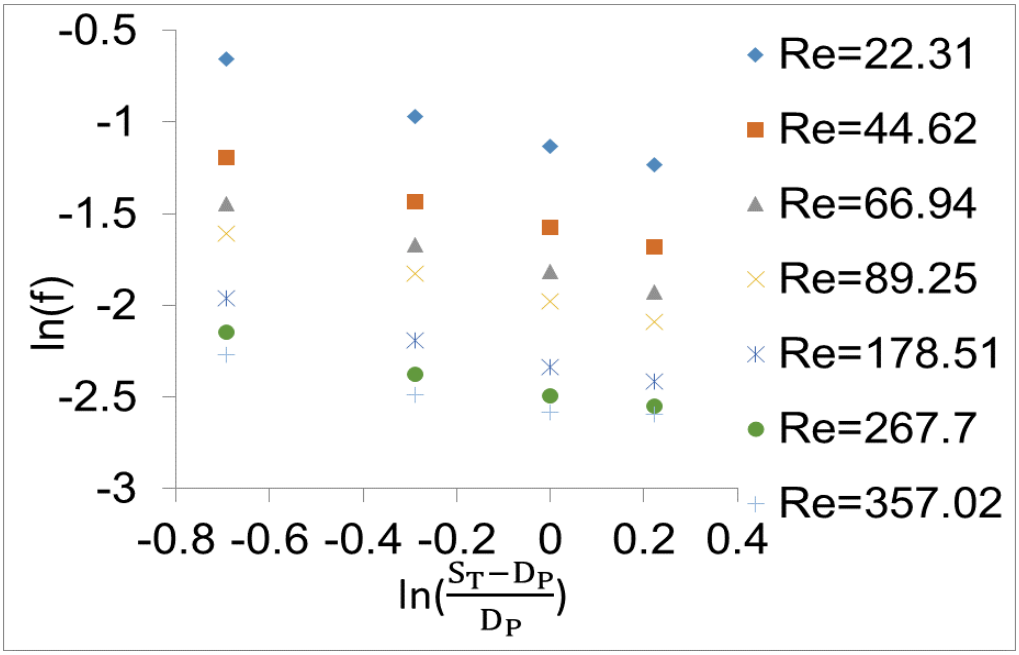


Figure 4.11: Friction factor versus ratio of transversal spacing to pin diameter.

Figure 4.11 shows that as the transversal spacing decreased, f increased. This was because as the transversal spacing decreased, it caused increased blockage to the fluid flow, which increased the pressure drop and thus the friction factor. Moores and Joshi [47] did not incorporate this into their correlation due to limited experimental data. Prasher et al. [36] only observed this negative trend at Re>100. Their correlations showed a positive trend at Re<100 which was not reflected by present modeling results. Short et al. [37] showed this negative trend, while Tullius et al. [38] showed a positive trend.

Figure 4.12 shows that as the longitudinal spacing decreased, friction factor increased. As the pins moved closer, the interaction between upstream and downstream pins became stronger. Both Short et al. [37] and Prasher et al. [36] also observed this trend. However, Tullius et al [38] showed a positive trend.

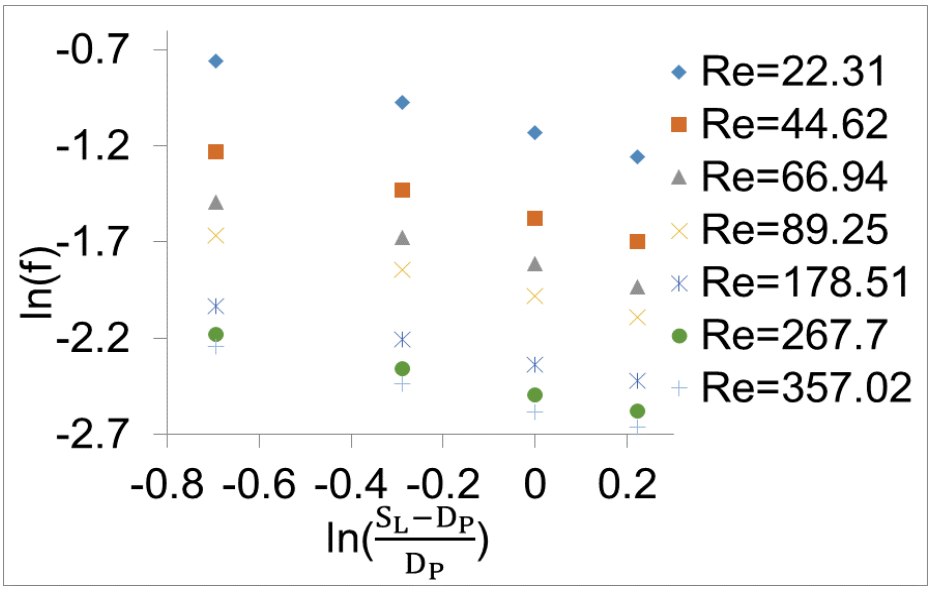


Figure 4.12: Friction factor versus ratio of longitudinal spacing to pin fin diameter.

Based on the simulations performed, a correlation for the friction factor for micro pin fin array was proposed. Table 4.4 shows the coefficients. In order to make the

correlations accurate, different coefficients were developed for Re<100 and Re>100. MAE between the correlation and CFD modeling was 2.2%.

$$f = C\left(\frac{H_p}{D_p}\right)^{\alpha_1}\left(\frac{S_L - D_p}{D_p}\right)^{\alpha_2}\left(\frac{S_T - D_p}{D_p}\right)^{\alpha_3} Re^m \quad (4.23)$$

Table 4.4: Coefficients for friction factor correlation for circular pin fin arrays**.**

	C	α_1	α_2	α_3	m
Re<100	3.1335	-0.4485	-0.4965	-0.5553	-0.6292
Re>100	1.246	-0.3362	-0.4478	-0.4615	-0.4393

In the present study, Colburn j factor was used to evaluate the thermal characteristics of pin fin array, while Kosar et al. [33], along with others used Nu.

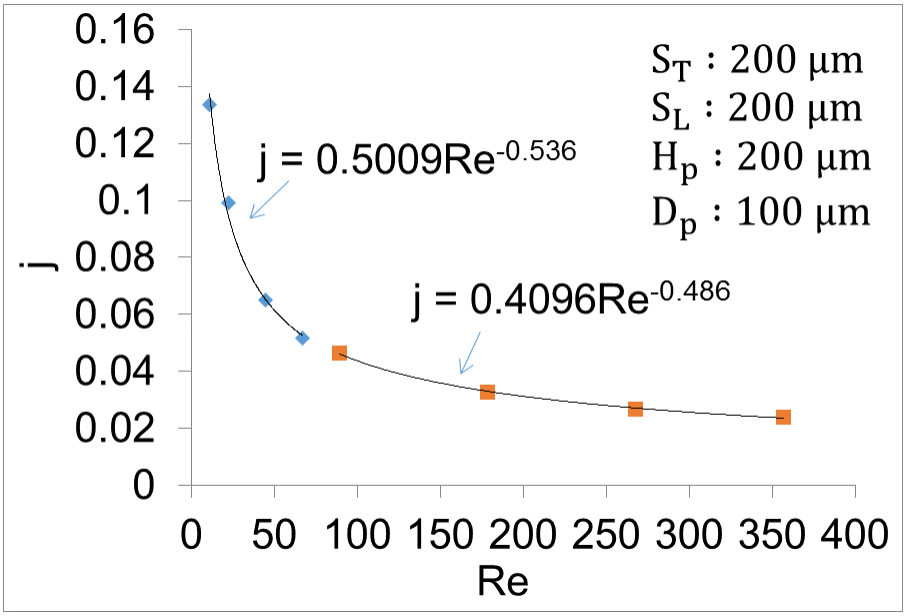


Figure 4.13: Colburn j factor versus Re.

Figure 4.13 shows the modeling result of j with Re. It was seen that j was not very sensitive to Re. The trend of j changed from -0.536 to -0.486, as Re increased from 22 to 357.

Figure 4.14 shows Colburn j factor was not sensitive to the ratio of pin fin height to diameter. It shows a positive trend at low Re and a negative trend at high Re. Moores and Joshi [47], and Tullius et al. [38] showed a positive trend, while Short et al. [39] observed a negative trend. Prasher et al. [36] and Kosar and Peles [41] did not include the effect of ratio of pin fin height to diameter in their correlations due to the limited number of samples.

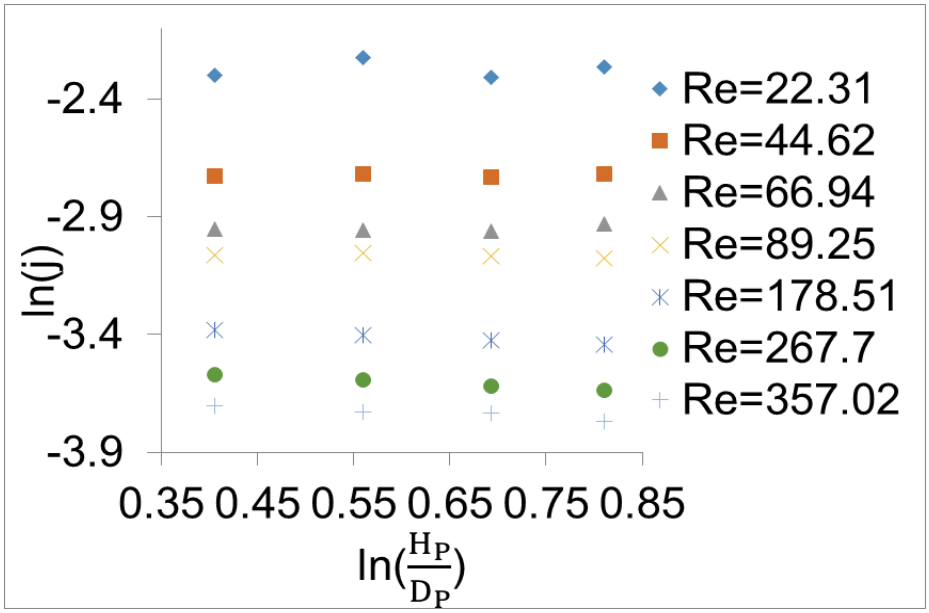


Figure 4.14: Colburn j factor versus ratio of pin fin height to diameter.

Figure 4.15 shows that the Colburn j factor decreased as the ratio of pin fin transversal spacing to diameter increased. However, at Re=357, a positive trend was observed. Kosar and Peles [41], Moores and Joshi [47] , Prasher et al. [36] did not include the effect of ratio of pin fin transversal spacing to pin fin diameter in their correlations. Short et al. [39] and Tullius et al. [38] showed a positive trend, which is because most of their data fell in Re>100.

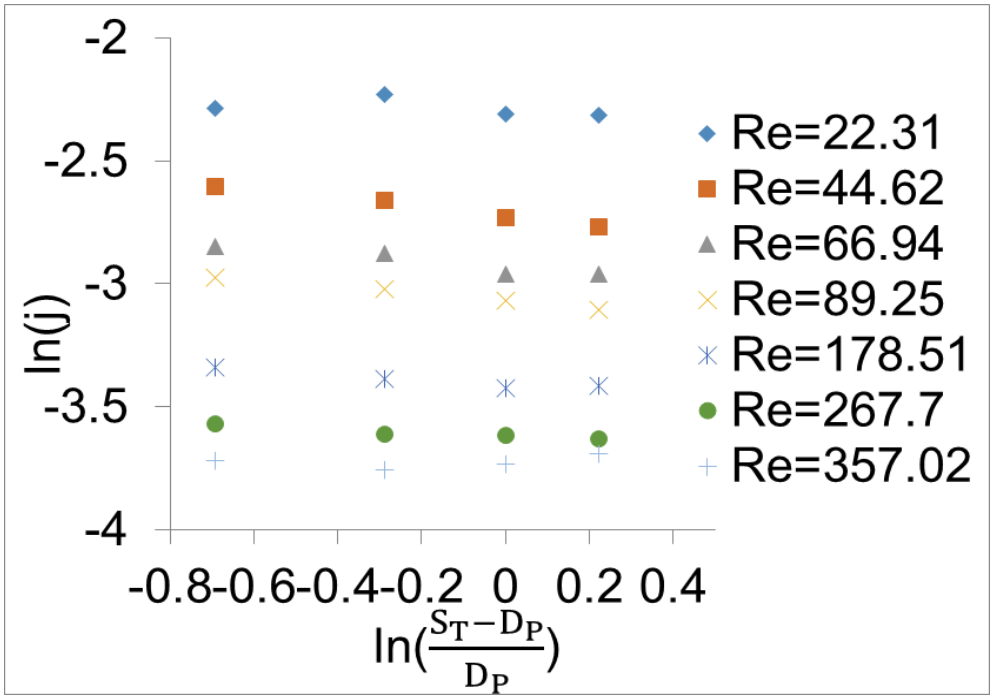


Figure 4.15: Colburn j factor versus ratio of pin fin transversal spacing to pin fin diameter.

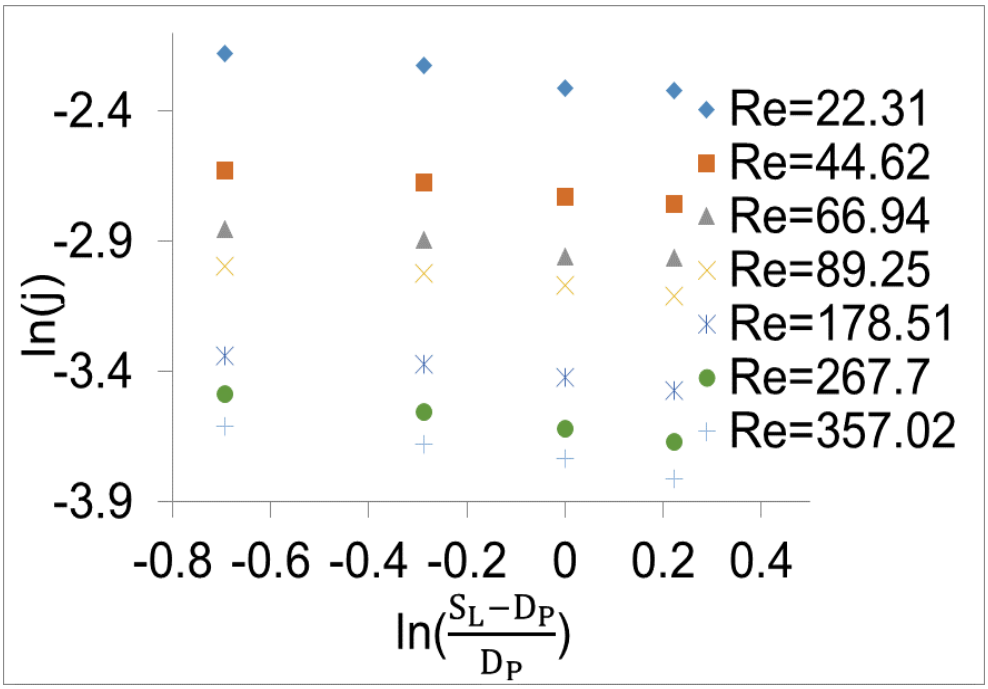


Figure 4.16: Colburn j factor versus ratio of longitudinal spacing to pin fin diameter.

Figure 4.16 shows that Colburn j factor decreased as ratio of longitudinal spacing to pin diameter increased. Kosar and Peles [41], and Moores and Joshi [47] did not include the effect of ratio of longitudinal spacing to pin fin diameter in their correlations. Prasher et al. [36] observed a negative trend. However, Short et al. [39] and Tullius et al. [38] showed a positive trend.

Based on the simulations performed, a new Colburn j factor correlation was developed. Table 4.5 shows the coefficients for the correlation. MAE between the correlation and CFD modeling was 2.5%.

$$j = C\left(\frac{H_p}{D_p}\right)^{\alpha_1}\left(\frac{S_L - D_p}{D_p}\right)^{\alpha_2}\left(\frac{S_T - D_p}{D_p}\right)^{\alpha_3} Re^m \quad (4.24)$$

Table 4.5: Coefficients for Colburn j factor correlation for circular pin fin arrays**.**

	C	α_1	α_2	α_3	m
Re<100	0.5885	0.0072	-0.1432	-0.1289	-0.5697
Re>100	0.4481	-0.1285	-0.1707	0.0804	-0.4864

The effect of pin shape was studied. Figure 4.17 shows the velocity plot across the square micro pin fin at different Re. It could be seen that the maximum velocity was between the pin fins. As Re increased, the influence of the upstream pin fin on the downstream pin fin became strong. At Re=100, re-circulation was observed. Around the corner of the square pin, there was a sharp change of the flow which increased the flow mixing, which can increase the heat transfer coefficient.

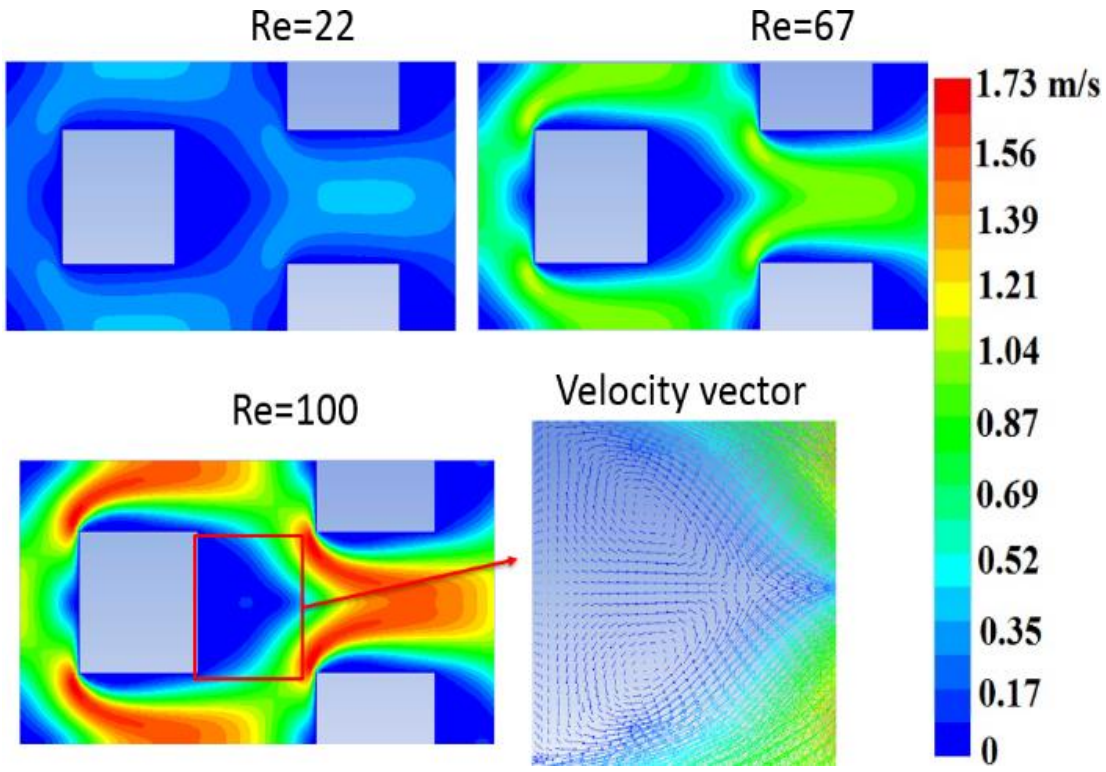


Figure 4.17: Velocity plot at different Re for square pin fin arrays.

Following the same procedure, the coefficients for friction factor and Colburn j factor were obtained as shown in Table 4.6 and Table 4.7. MAE between the correlation and CFD modeling were 3.4% and 2.3% respectively.

Table 4.6: Coefficients for friction factor correlation for square pin fin arrays.

	C	α_1	α_2	α_3	m
Re<100	3.3553	-0.356	-0.7906	-0.7453	-0.525

Table 4.7: Coefficients for Colburn j factor correlation for square pin fin arrays.

	C	α_1	α_2	α_3	m
Re<100	0.5862	-0.0514	-0.175	-0.2494	-0.5518

4.5 Comparison between Circular and Square Pin Fin Arrays

In the comparison of the ΔP between square and circular staggered micro pin fin arrays, the numbers of pins in the flow direction were the same; the pin fin dimensions including the S_L and S_T, H_p, D_h were the same; the Re was also the same. Figure 4.18 shows that ΔP of square micro pin fin arrays was much higher than that of circular pin fin array. That is because when fluid flew across the circular micro pin fin, it encountered less flow resistance than the square micro pin fin. The square shape produced larger flow separation regions. When Re increased, the pressure drop difference between circular and square pin fin was also increasing.

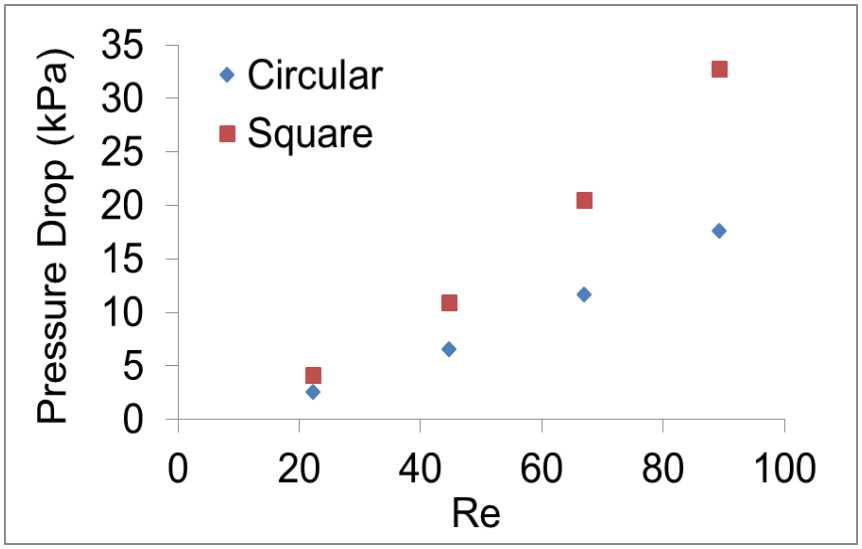


Figure 4.18: Pressure drop comparison between square and circular micro pin fin arrays.

Figure 4.19 shows that square micro pin fin array had larger heat transfer coefficients than circular micro pin fin array. However, when evaluated under the same pumping power which was more realistic, the square micro pin fin array had poor thermal performance due to its larger flow resistance (Figure 4.20). The benefit of circular micro pin fin became more evident as the pumping power increased.

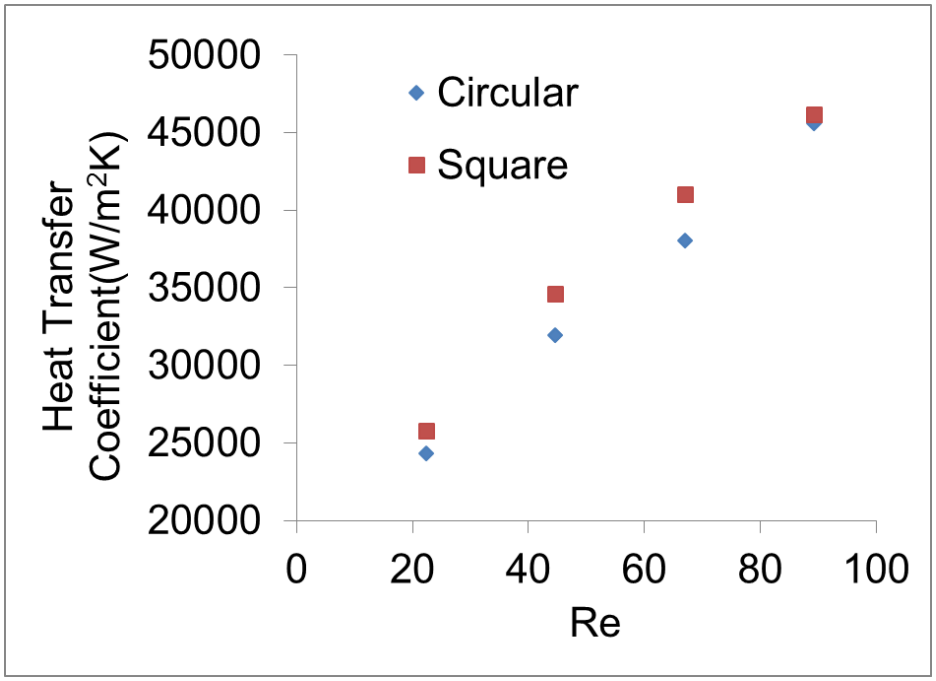


Figure 4.19: Heat transfer coefficients comparison between square and circular micro pin fin arrays for same Re.

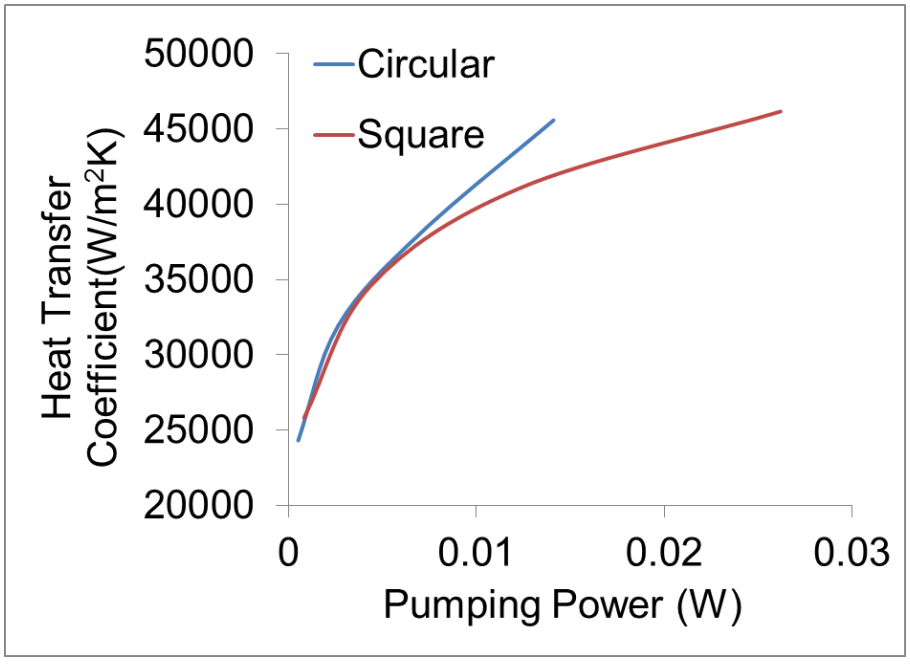


Figure 4.20: Heat transfer coefficients comparison between square and circular micro pin fin arrays under same pumping power with 1cm × 1cm chip.

4.6 Summary

In this chapter, a numerical model with symmetric boundary conditions was built to study the hydraulic and thermal characteristics of pin fin enhanced microgaps under single phase cooling. Predicted pressure drop and temperatures were compared with experimental results. A parametric study was conducted to study the effect of Re, pin spacing, and pin height. Both circular and square pin fin arrays were studied, and their performance was compared under same Re and pumping power. The main observations of this chapter were:

(1) At low Re, f was very sensitive to Re. As Re increased, f became less sensitive. f varied as $Re^{-0.894}$ to $Re^{-0.440}$, as Re increased from 22 to 357.

(2) Colburn j factor was not very sensitive to Re.

(3) As the spacing of the pins was reduced, the interaction between the pins became stronger.

(4) The pressure drop of the square pin fin array was much larger than circular pin fin array under same Re. Heat transfer coefficient of square pin fin array was higher than circular pin due to the increased fluid mixing. However, for the same pumping power, circular micro pin fin array showed better thermal performance than square micro pin fin array.

CHAPTER 5

CO-DESIGN OF MULTICORE ARCHITECTURES AND MICROFLUIDIC COOLING FOR 3D STACKED ICS

The characteristics of the pin fin enhanced microgap have been studied previously. As the power dissipation of microprocessor increases, and the chips are stacked, the air cooling cannot meet the requirement of thermal management. Microfluidic cooling was proposed as new cooling technique due to its high thermal performance. In this Chapter, the pin fin enhanced microgap was used for cooling of 3D stacked ICs. The benefits and advantage of single phase microfluidic cooling have been demonstrated by both modeling and experiments.

5.1 3D Stacked ICs Structure Model

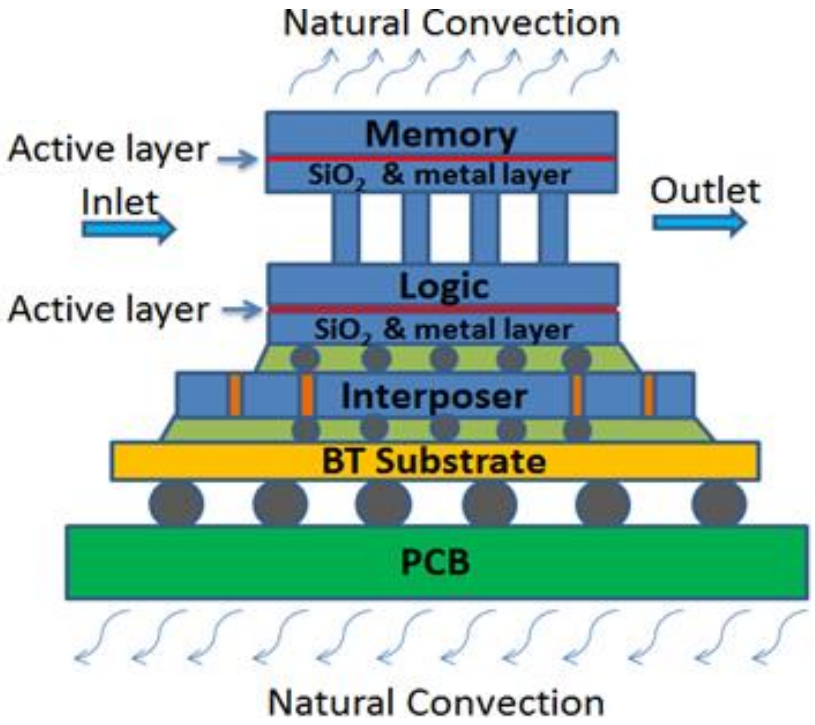


Figure 5.1: 3D stacked ICs structure.

Figure 5.1 shows the notional packaged 3D stacked IC structure [87] with microfluidic cooling considered in the present study. Two tiers, logic (processor) and memory, were enclosed in the system. The thin active layer in which most of the heat was generated was identified. Below the active layer were the SiO_2 & metal layer used for bonding and routing. Between the two tiers was the pin fin enhanced microgaps, incorporating fluid flow which was driven by an outside flow loop. The pin fin array was fabricated by Deep Reactive Ion Etching (DRIE) of the Si chip. Inside the pin fins were electrical vias filled with copper which connected the logic and memory layers. The vias were first etched and then the copper was filled by electroplating. For simplicity, the metal layer and electric vias were not included in the modelling. The two tiers were placed on a bismaleimide triazine (BT) substrate through a silicon interposer. The BT substrate was attached to the printed circuit board using solder ball array. The top and bottom of the system were assumed to be natural convection cooled, with heat transfer coefficient of 10 $W/(m^2K)$. Table 5.1 shows the dimensions and properties of materials.

Table 5.1: Material dimensions and properties of 3D stacked ICs.

	Thickness (μm)	Length (mm)	Width (mm)	Thermal Conductivity (W/(mK))	
				k_{xy}	k_z
PCB	1600	100	100	56.9	0.36
BT Substrate	950	20	20	13.4	0.21

Table 5.1 continued.

	Thickness (μm)	Length (mm)	Width (mm)	Thermal Conductivity (W/(mK))	
				k_{xy}	k_z
Interposer	1.69	2.06	2.81	2.31	1.63
Logic/Memory	100	8.4	8.4	149	149
SiO_2	10	8.4	8.4	1.4	1.4
Solder Ball	D=600 μm, pitch =1000 μm. Between PCB and BT substrate.			0.05	14.1
Micro Bump	D=12 μm, pitch =250 μm. Between interposer and BT substrate.			0.63	0.63
TSV	D=25 μm, pitch=150 μm.			401	401

5.1.1 Model Development

A simplified structure was proposed in Figure 5.2. An effective heat transfer coefficient was applied on the bottom of SiO_2 & metal layer.

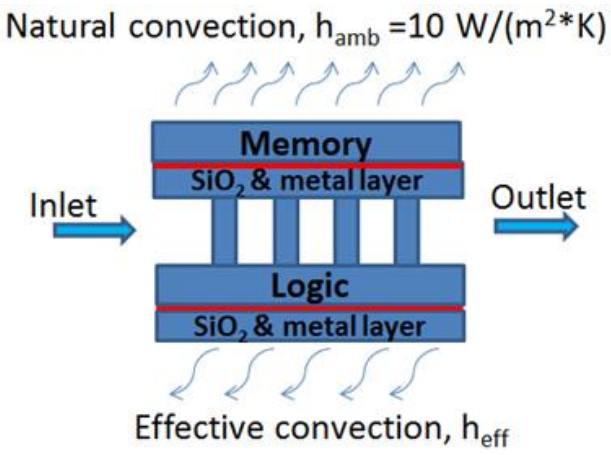


Figure 5.2: Simplified structure.

To obtain the effective heat transfer coefficient, a finite element (FE) heat conduction model, including the materials from the underfill below the SiO_2 & metal layer to PCB was built (Figure 5.3). The effective heat transfer coefficient was obtained by:

$$R = \frac{1}{h_{eff} A_o} = \frac{T_{o,avg} - T_{amb}}{Q} \tag{5.1}$$

where R is the thermal resistance between the heating surface and the ambient. It included the conduction resistance from the underfill to the PCB and the convection resistance to the ambient. Also, Q was the total power applied on the surface of underfill (2 W), A_o was the surface area of the oxide layer, $T_{o,avg}$ was the average temperature of the heating surface, and T_{amb} was the ambient temperature (20 ℃ in the present study).

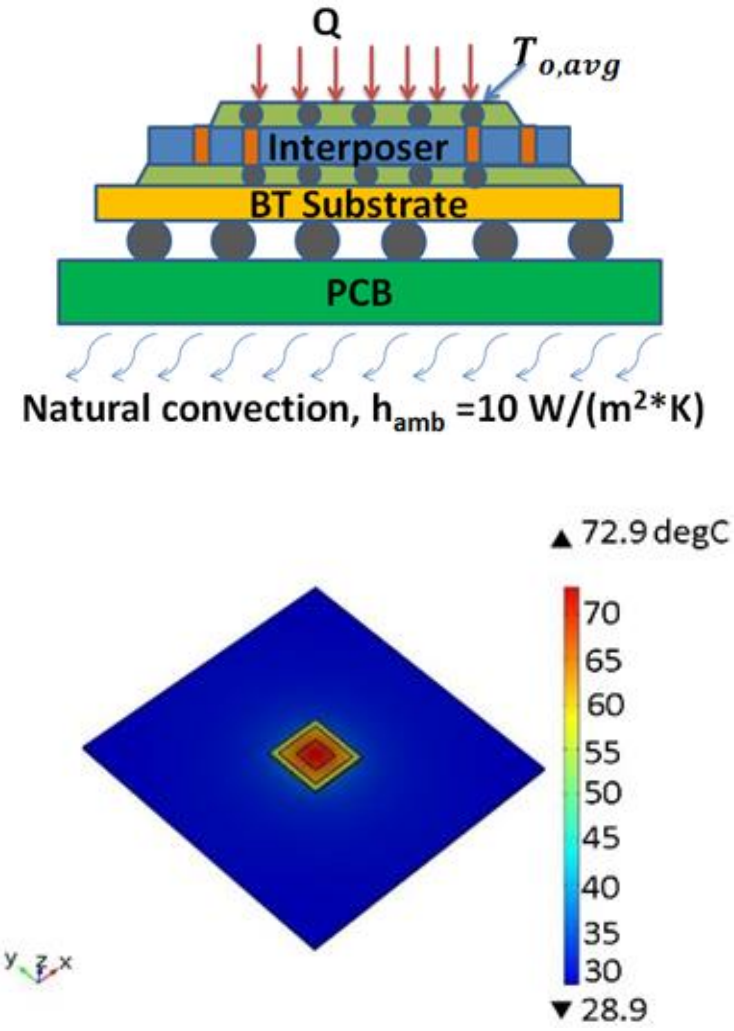
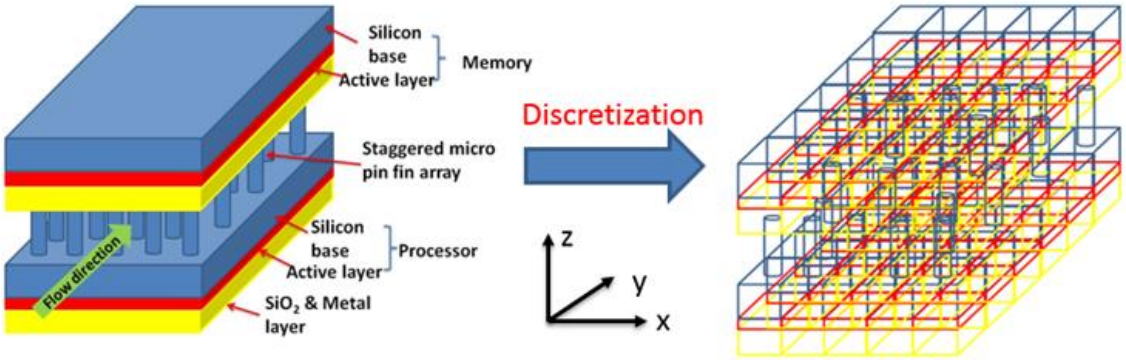


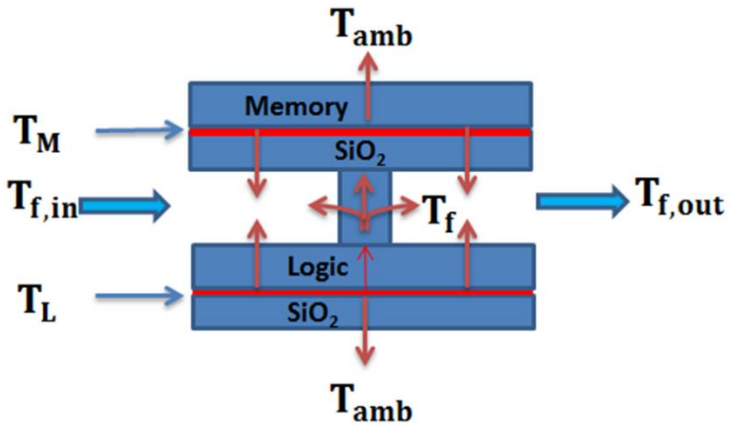
Figure 5.3: Conduction FE model and temperature result.

The average temperature of the heating surface was 70.4 ℃. So the effective heat transfer coefficient was 562.4 W/ (m^2K).

A compact thermal model was built, which discretized the 3D stacked ICs model into multiple control volumes (Figure 5.4(a)), each around one pin (Figure 5.4(b)). The metal layer and electrical vias were not included for simplicity. The arrows showed the energy flows in the vertical direction within one control volume.



(a)



(b)

Figure 5.4: Compact thermal model: (a) Model discretization; (b) Control volume around one pin.

After the control volumes were defined, energy balance analyses were conducted for each control volume. Within the control volume, there were solid and fluid parts. For the solid part, in-plane heat conduction from 4 directions was considered. Moreover, it had vertical heat conduction to the other tiers through the pin, convection to the fluid and the ambient. A uniform temperature for each active layer and fluid in one control volume was assumed for simplification. The energy equation for the solid domain was:

$$\text{Solid: } \dot{q}_{gen} + \dot{q}_{cond} + \dot{q}_{conv} = 0 \tag{5.2}$$

where $\dot{q}_{gen}$ was the energy generation rate obtained from the power map. Also $\dot{q}_{cond}$ was the heat conduction from neighbouring control volumes. $\dot{q}_{conv}$ was the heat transferred by convection between the solid and fluid. Since both processor and memory tiers were included, two energy equations are needed.

Unidirectional fluid flow was assumed and axial conduction inside the fluid was neglected. The energy balance equation for the fluid was:

$$\text{Fluid: } \dot{m}C_p(T_{f,in} - T_{f,out}) + \dot{q}_{conv} = 0 \tag{5.3}$$

A system of equations was obtained by applying energy analysis on every control volume. In order to obtain the temperature distribution, we need to solve these equations simultaneously. All the convection and conduction terms were expressed as functions of fluid, processor and memory temperatures first. The resulting system of equations only had the temperature of processor, memory and fluid as the variables. The temperature information for every control volume were stored in three 2D matrices. In the present study, Tridiagonal Matrix Algorithm (TDMA) [88] was used to solve these equations. Absolute convergence criteria was 10^{-6}. All the calculations of the compact thermal model were conducted in Matlab.

Heat transfer coefficient was obtained based on the numerical modelling in Chapter 4.

5.1.2 Model Validation

In order to validate the compact thermal model, a full computational fluid dynamics and heat transfer (CFD/HT) model was built in Fluent. D_p was 100 μm, S_L and S_T were 200 μm each, and H_P was 300 μm. The chip dimension was 8.4 mm x 8.4 mm. Figure 5.5

shows the model and boundary conditions used. A symmetric boundary condition was used to simplify the model. The uniform heat dissipation of the active layer of the logic tier was 160 W. The uniform dissipation of active layer of the memory tier was 80 W. The inlet boundary condition was water at 20 ℃ with inlet velocity 0.58 m/s. The outlet boundary condition was atmospheric pressure. The fluid properties were evaluated at mean fluid temperature. An upwind scheme with Semi-Implicit Method for Pressure-Linked Equations (SIMPLE) [85] algorithm was employed for the solution of fluid flow and heat transfer.

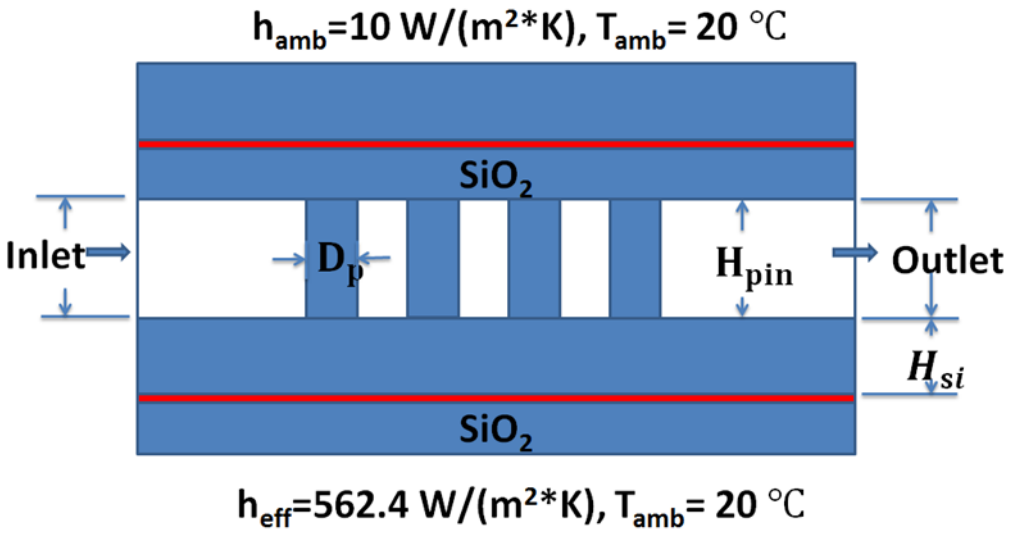


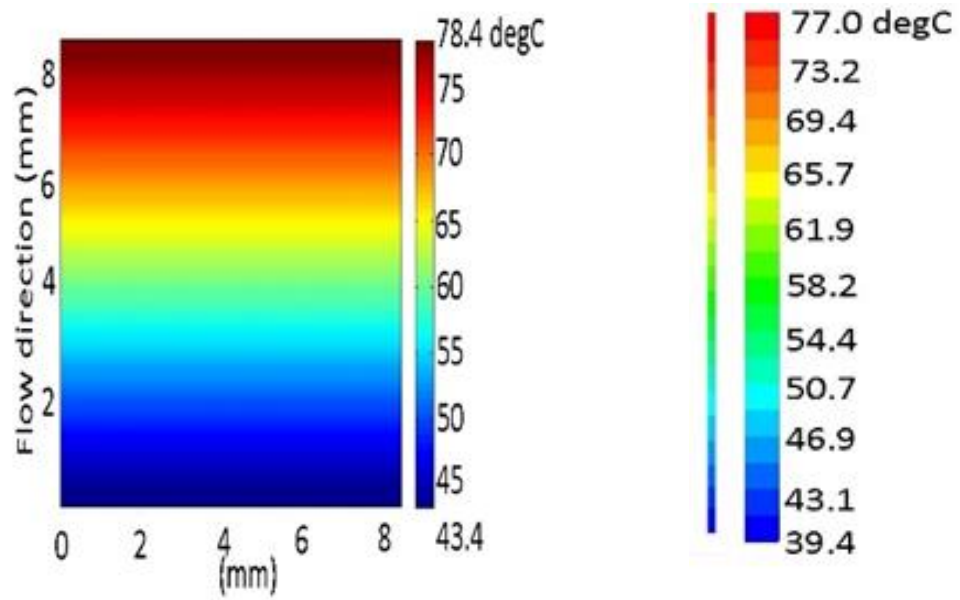
Figure 5.5: Full CFD/HT model.

In order to balance the accuracy and calculation time, a mesh independence study was did for the full CFD/HT model. Table 5.2 shows the results. When the number of elements increased from 3745k to 4133k, the pressure drop changed 0.09% and the maximum temperature changed less than 0.2%. So 3745k elements were used subsequently.

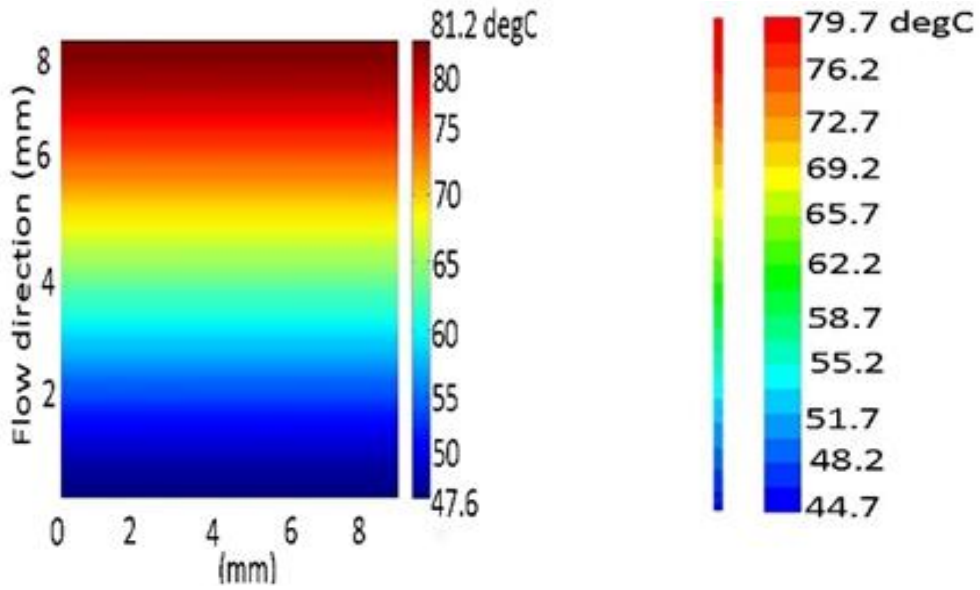
Table 5.2: Mesh independence study for 3D stacked ICs model.

Number of elements	ΔP (Pa)	$T_{max,processor}$ (℃)	$T_{max,memory}$ (℃)
2777k	20949	76.87	79.98
3745k	20934	76.96	79.74
4133k	20953	76.95	79.89

Figure 5.6(a) shows the comparison of the temperature distribution of logic tier between compact thermal model and detailed CFD/HT model. The temperature increased almost linearly along the flow direction due to the uniform heating. The difference in the maximum temperature between the two models was 1.8%, while that in minimum temperature was 9.2%. In the compact thermal model, an average heat transfer coefficient was used for every column of the pin fins. However, the heat transfer coefficient at the inlet of the full CFD/HT model was much higher than the average heat transfer coefficient. This resulted in the detailed CFD/HT model prediction being lower than that of compact model.



(a)



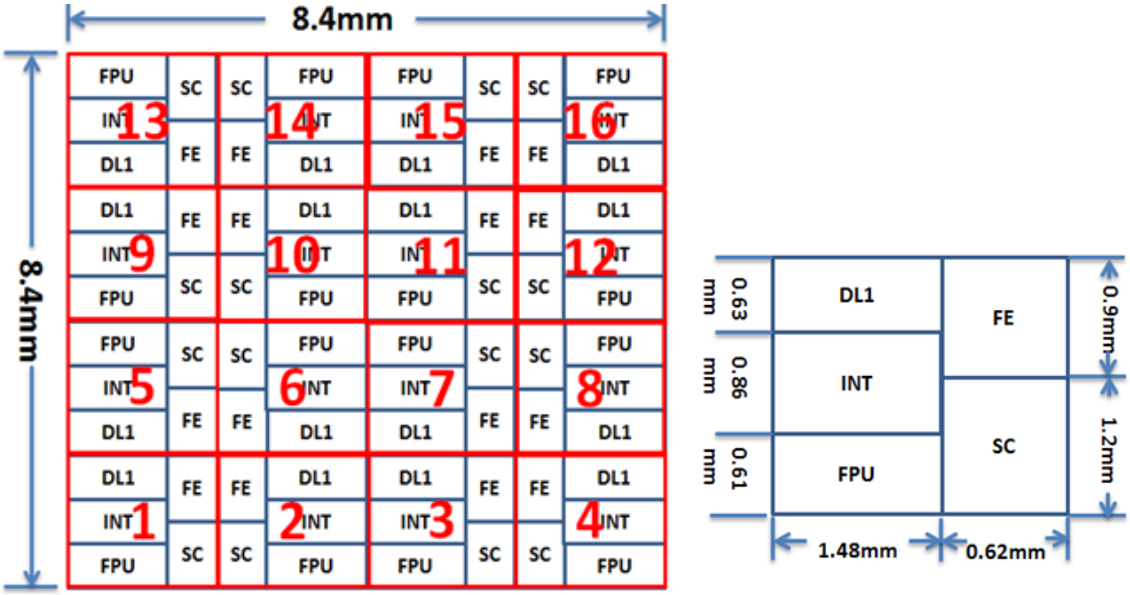
(b)

Figure 5.6: Comparison of temperature distribution of processor tier, memory tier between compact thermal model and detailed CFD/HT model; (a) processor tier, compact thermal model/ detailed CFD/HT model, (b) Memory tier, compact thermal model/ detailed CFD/HT.

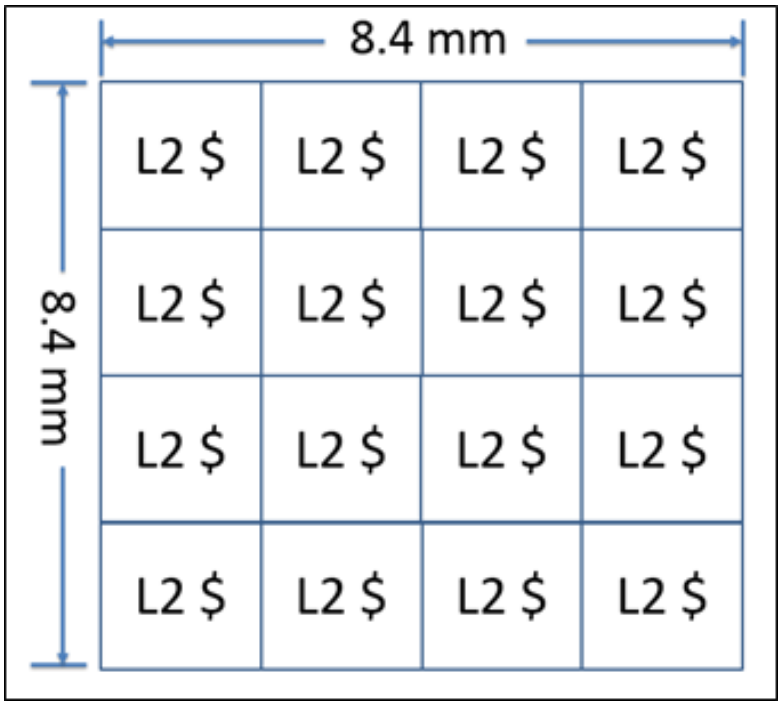
Figure 5.6(b) is the comparison of temperature distribution of memory tier between compact thermal model and detailed CFD/HT model. The difference in the maximum temperatures between the two models was 1.8%, while that in minimum temperature was 6.1%. This confirmed the validity of the compact thermal model. The compact thermal model took about 45 seconds to compute, while the detailed CFD/HT model took about 3 hours and 20 min on a Win 7 machine with 3.4 GHz CPU and 8.0 GB memory.

5.1.3 Realistic Nonuniform Power Map

We modeled a 16 core, x86 processor, each with its own L1 cache and all cores sharing a banked, coherent L2 cache interconnected by a 2D mesh interconnect. The simulation model was a cycle-level timing model that was driven by a multicore emulator front-end that booted a linux operating system and executed compiled 32-bit x86 binaries. The goal of this infrastructure was to generate timing, energy, and power behaviors that were as close as possible to commodity processors. The floor plan used in this study is shown in Figure 5.7. The 16 cores were placed on the 8.4mm x 8.4mm chip. Every core consisted of five modules: Frontend (FE), scheduler (SC), integer unit (INT), floating point unit (FPU) and memory (DL1). The L2 cache consisted of 16 equal sized L2 cache banks arrayed on a 8.4mm x 8.4 mm die. Each L2 bank had a 1 Mbyte capacity. This floor plan was generated using the McPAT [89] modeling library using publicly available information about commodity x86 processors.



(a)



(b)

Figure 5.7: Floor plan for (a) Processor tier, (b) Memory tier.

Simulations were run for 500M clock cycles to warm up the processor state and reach a "region of interest" in the benchmark program. This was a region wherein the computational characteristics were representative, since they primarily avoided operating system boot code and application startup and initialization code. Once execution had reached the region of interest, the power at each block in the processor floor plan was sampled every 10 microseconds to produce a power trace. Such traces were used to drive the thermal models. In general, we drew upon benchmark programs from the SPLASH and PARSEC benchmark suites. In the specific results reported here, the power traces were generated from the Canneal benchmark in the PARSEC benchmark suite.

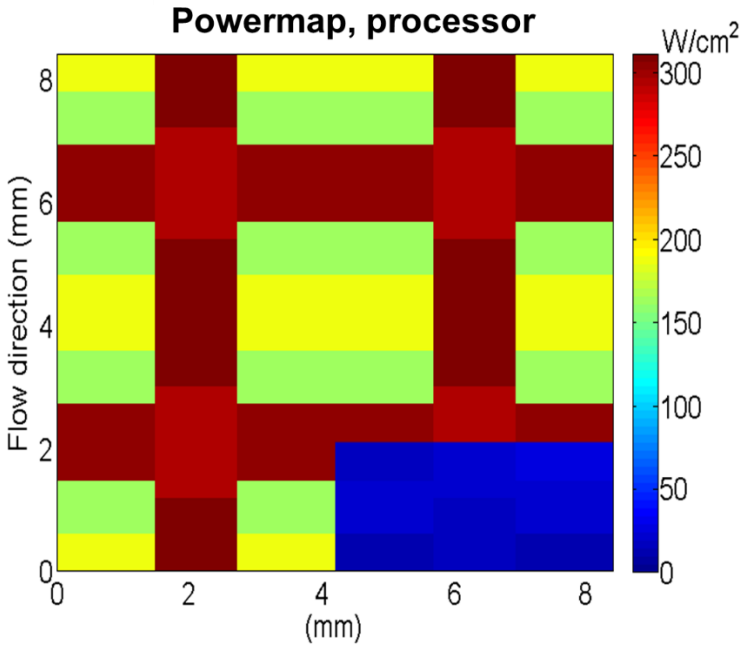


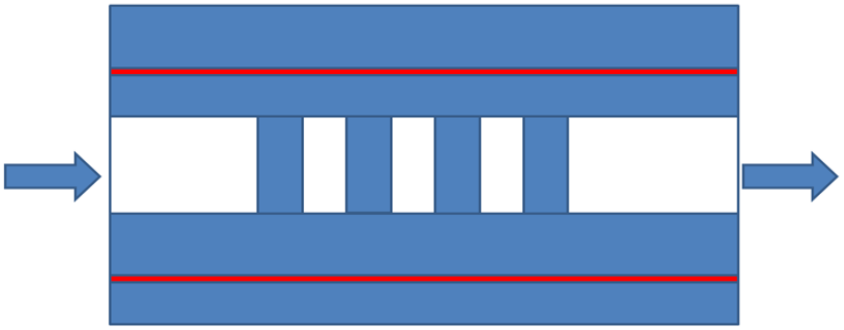
Figure 5.8: Non-uniform power map of processor: barnes.

The physical model employed various configurations of the processor tier and memory tier with microfluidic cooling. While there were many more configurations and packaging options that could have been explored, we emphasized two main points– i) the methodology for co-design, and ii) demonstration that co-design matters. Figure 5.8 shows

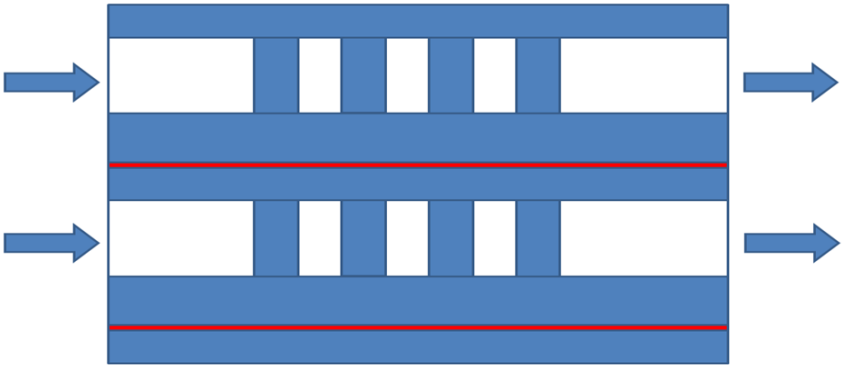
the dynamic power map of the processor for “barnes”. The total dynamic power of the processor was 132.9 W and the maximum heat flux was 310.1 W/cm^2. The total dynamic power of the memory was assumed to be 30% of that of processor and uniformly distributed.

5.1.4 Case Study with Different Microgap Configurations

The compact thermal model was used to analyze the thermal characteristics of 3D stacked ICs under realistic power map “barnes”. The total pumping power was 0.03 W, water inlet was at 20 ℃, and the outlet boundary condition was atmospheric pressure.



(a)

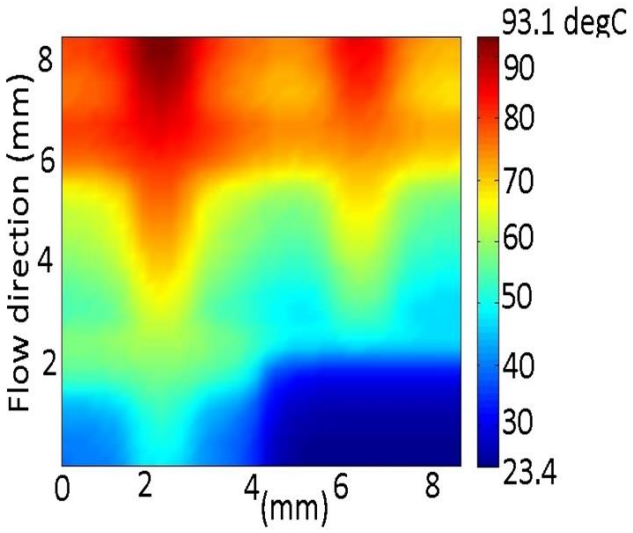


(b)

Figure 5.9: Two types of microgap configurations: (a) Two tiers with one microgap, (b) Two tiers with two microgaps.

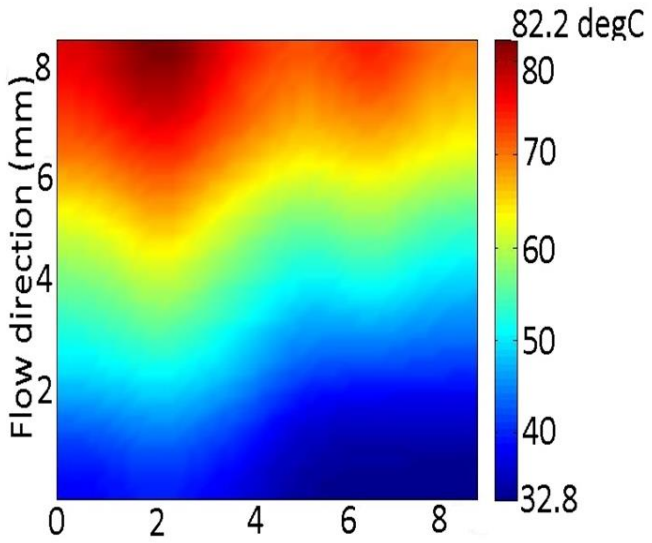
Two types of microgap configurations were studied as in Figure 5.9. The first configuration had only one microgap, while the other one had two. The D_p was 100 µm, S_L and S_T 200 µm, and H_P 200 µm.

The first case studied was one microgap with processor tier at bottom and memory tier on top. Figure 5.10 shows the temperature distribution of logic and memory tier for this case. The non-uniform temperature distribution was due to the non-uniform heat dissipation. The maximum temperature of the logic tier was 93.1 ℃ at the outlet. Every core had the same power distribution, except cores 3 and 4. Due to the bulk fluid temperature rise, the maximum temperature was at the outlet. Although the uniform heat dissipation of memory tier was only 30% of that of the logic tier, the temperature distribution was non-uniform and the maximum temperature of the memory tier reached 82.2 ℃ because of the cross-tier heat conduction. The pressure drop ΔP was 27.3 kPa and the mass flow rate ṁ was 1.1 g/s for this case.



(a)

Figure 5.10: Temperature distribution for case 1 (a) Processor, (b) Memory.



(b)

Figure 5.10 continued.

Table 5.3: Results for 4 cases.

	Configurations	$T_{max,processor}$ (°C)	$T_{max,memory}$ (°C)
Case 1	One microgap with processor tier at bottom and memory tier on the top	93.1	82.2
Case 2	One microgap with processor tier on the top and memory tier at the bottom	114.9	77.1
Case 3	Two microgaps with processor tier at bottom and memory tier on the top	87.7	54.8
Case 4	Two microgaps with processor tier on the top and memory tier at the bottom	72.7	58.3

Table 5.3 shows the maximum temperature of the processor and memory tier for 4 different cases. Compared with case 1, the temperature of processor tier in case 2 was 114.9 ℃, which was higher than that of case 1. The temperature of memory tier was 77.1 ℃, which was lower than that of case 1. This was because the thermal conductivity of silicon is higher than that of silicon oxide. So for two tiers with one microgap configuration, the processor tier with high heat dissipation should be placed at the bottom. For case 3, the maximum temperature of processor tier was reduced by about 5.4 ℃, and that of the memory tier was reduced by about 27.4 ℃ compared with case 1. The pumping power was determined as the product of the pressure drop and volume flow rate. When the pumping power of each microgap was reduced to half of case 1, both the pressure drop and volume flow rate were reduced. Thus, volume flow rate of each microgap should be larger than half of case 1. The total mass flow rate for case 3 was 1.6 g/s - higher than case 1. Therefore, the bulk fluid temperature rise was lower than case 1 and the maximum temperature of case 3 should be lower than case 1. Further, the pressure drop was reduced to 18.3 kPa. Thus the two tiers with two microgaps was superior, both in thermal and hydraulic performance. Compared with previous cases, the maximum temperature of the processor tier in case 4 was further reduced to 72.7 ℃, since the processor tier had microgaps below and above. The temperature of the memory tier was slightly increased, because it had only one sided microgap cooling, compared with case 3. The above four cases show that the two tiers with two microgaps, and high heat dissipation tier with double side microgap cooling has the best thermal performance.

5.1.5 Workload Driven Cooling Solution Optimization

In the above cases, the pin fin dimensions were fixed. In this section, the compact thermal model was linked to the Matlab optimization tool box. A genetic algorithm was used to find an optimized pin fin structure, which minimized the maximum temperature of the logic tier for the configuration of case 4. The heat dissipation for logic and memory tiers were the same as before, with pumping power fixed at 0.03 W. The optimization range of pin fin diameters was 100 μm ~ 200 μm; the range of ratio of longitudinal spacing to pin diameter was 1.5 ~ 2.25; the range of ratio of transversal spacing to pin diameter was 1.5 ~ 2.25; and the range of ratio of pin height to pin diameter was 1 ~ 3. DI-water was used as coolant, with inlet temperature at 20 ℃.

Table 5.4: Optimization results for non-uniform heat dissipation without hotspot.

	D_p (μm)	S_L (μm)	S_T (μm)	H_P (μm)	$\dot{m}$ (g/s)	ΔP (kPa)	$T_{max,logic}$ (℃)
1	100	200	200	200	1.6	18.3	72.7
2	100	150	150	243	1.2	25.5	81.6
3	100	200	200	100	1.0	29.7	92.3
$4_{(optimized)}$	194	290	420	400	3.4	8.9	57.6

Table 5.4 shows the optimization results. The pin fin dimensions 1, 2, 3 were selected from literature. Although there were more pin fins for the smaller pin fin dimensions, the mass flow rate was smaller and pressure drop higher due to the higher flow

resistance, which lead to a larger bulk fluid temperature rise. Therefore, the maximum temperature of logic tier was higher. The low flow resistance for larger pin fin dimensions increased the mass flow rate significantly, and the bulk fluid temperature rise was reduced. So the maximum temperature of processor tier was smaller.

The previous optimization was for non-uniform heat dissipation without hotspot. Next, the power of DL1 module in the 7th core was increased to 28.1 W, while other modules remained the same. So, the maximum temperature was now at this hotspot. The optimized pin fin dimensions in Table 5.5 show that for the non-uniform heat dissipation with hotspot, smaller pin fin dimensions achieved better thermal performance. Compared with large pin fin dimensions, which produced large mass flow rate and small bulk fluid temperature rise, smaller pin fin dimensions resulted in more convection surface area. While this overall result was expected, the present analysis provided a quantitative definition of the optimized design.

Table 5.5: Optimization results for non-uniform heat dissipation with hotspot.

	D_p (μm)	S_L (μm)	S_T (μm)	H_P (μm)	$\dot{m}$ (g/s)	ΔP (kPa)	$T_{max,logic}$ (°C)
1	100	200	200	200	1.6	18.2	149.5
2	100	150	150	243	1.2	25.2	136.1
3	100	200	200	100	1.0	29.4	158.5
4	194	290	420	400	3.4	8.8	151.9
5(optimized)	116	175	175	349	1.6	18.3	131.1

5.2 Coupled Power-Thermal Model

In addition to the dynamic power dissipated when the transistors are switching, another power could be dissipated even when the circuit is in idle state-static power, also called leakage power. One type of leakage-the subthreshold leakage, occurs when the gate voltage is below the threshold voltage. As semiconductor technology scales to smaller feature sizes, leakage power increases exponentially because transistor threshold voltages are reduced in concert with supply voltage to maintain transistor performance. The leakage power strongly depends on the supply voltage and leakage current:

$$P_{leak} \propto I_{leak}(T, V_{dd}) * V_{dd} \tag{5.4}$$

The significance of leakage power exacerbates the thermal problems since leakage power has an exponential dependence on temperature (Figure 5.11) [90]. The International Technology Roadmap for Semiconductors (ITRS) projects that the static power consumption will exceed the dynamic power consumption in 2016 unless effective measures are taken to reduce the leakage power [91].

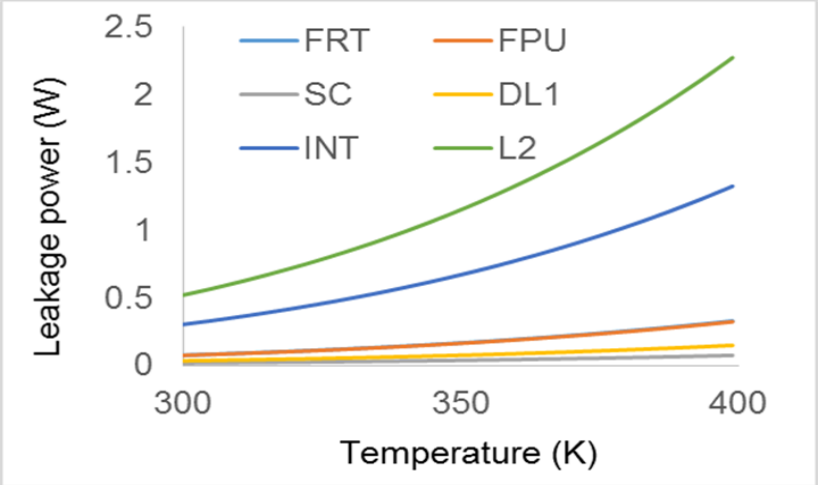


Figure 5.11: Leakage power characteristics for each module.

Figure 5.12 shows the power-thermal simulation framework. The same floorplan and application binary named “barnes” was used. The cycle-based simulator simulated a x86 16-core processor with real applications and the hardware activity was collected for regions of interest in the application and drove the power models. The power distribution for each core was determined which in turn drove the thermal model. The thermal model determined the thermal map under a certain pumping power. Since the leakage power depends on the temperature, the power model calculated the leakage power of each core based on the thermal map and updated the input power to the thermal model.

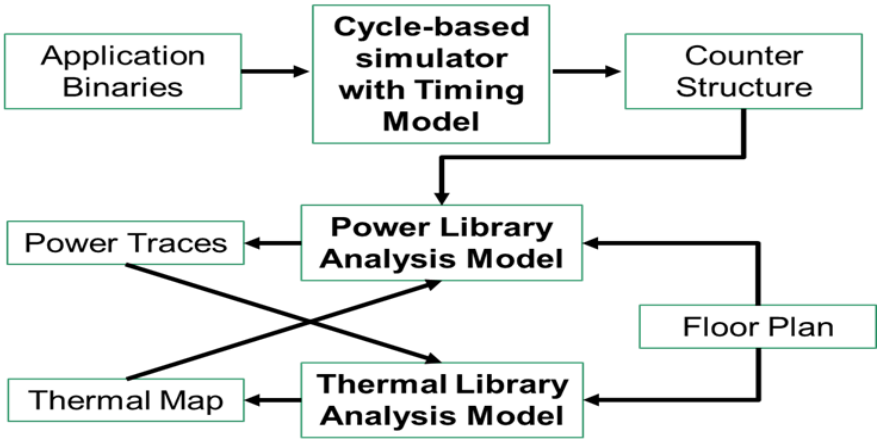
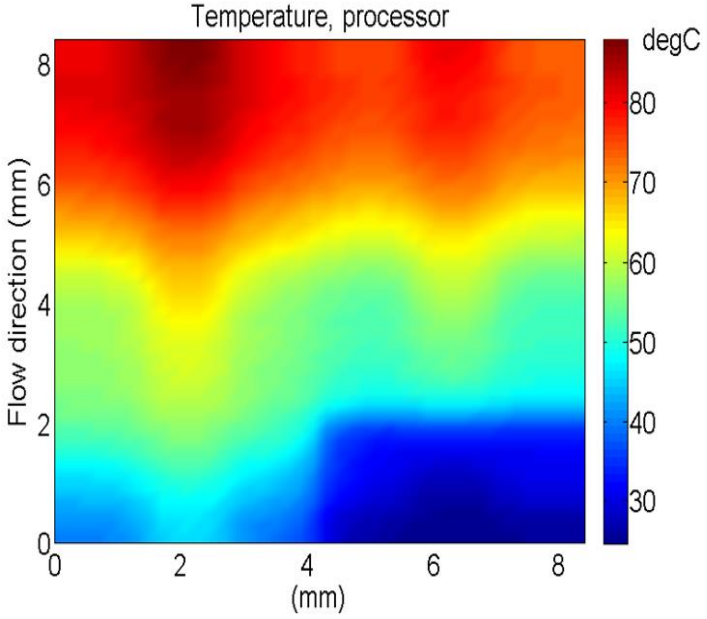


Figure 5.12: Coupled power-thermal model.

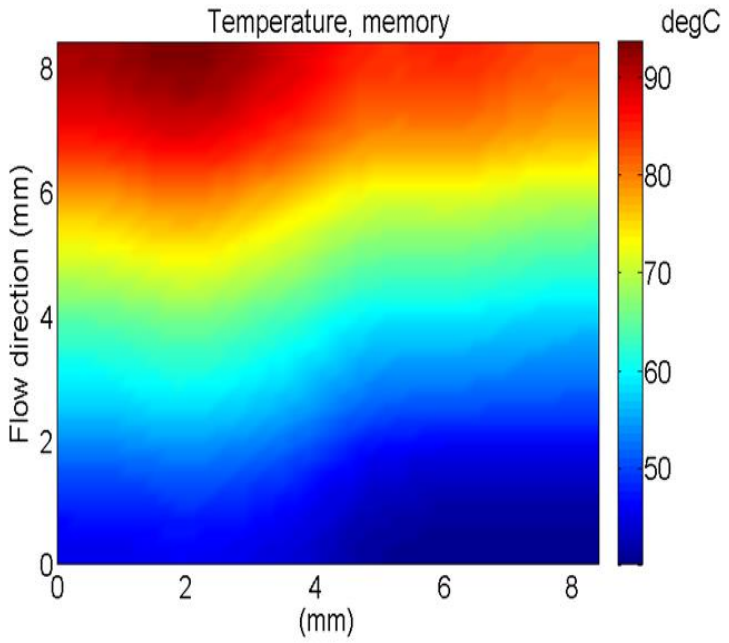
The effects of various parameters related to microfluidic cooling such as ambient heat transfer coefficient, ambient temperature, and pumping power on the electrical and thermal performance were evaluated. The initial pin fin dimensions were: diameter 100 µm, pitch 100 µm in both directions, and height 200 µm. Ambient heat transfer coefficient was assumed to be 10 W/m^{2}K and ambient temperature 20 $^{\circ}$C. The pumping power for the flow loop was 0.1 W.

Figure 5.13 shows the temperature distribution of the processor and memory. Although the dynamic power of the memory was only 30% of that of processor, the maximum temperature of the stack, 93.8 °C, was located on the memory tier. This was because the heat on the memory tier must transfer through the oxide layer with low thermal conductivity and then dissipated into the fluid. However, the heat on the processor was conducted through the silicon base layer with much higher thermal conductivity than that of oxide layer into the fluid. As can be seen from Figure 5.13, the chip temperature increased along the flow direction. This was because as the fluid flew through the channel it absorbed the heat and its temperature increased. The leakage power on the processor was 40.8 W while that of the memory was 56.1 W. The leakage power amounted to 55.8% of the dynamic power of processor and memory. This proves that it is necessary to consider the leakage power consumption for accurate results.



(a)

Figure 5.13: Temperature plot (a) Processor, (b) Memory.



(b)

Figure 5.13 continued.

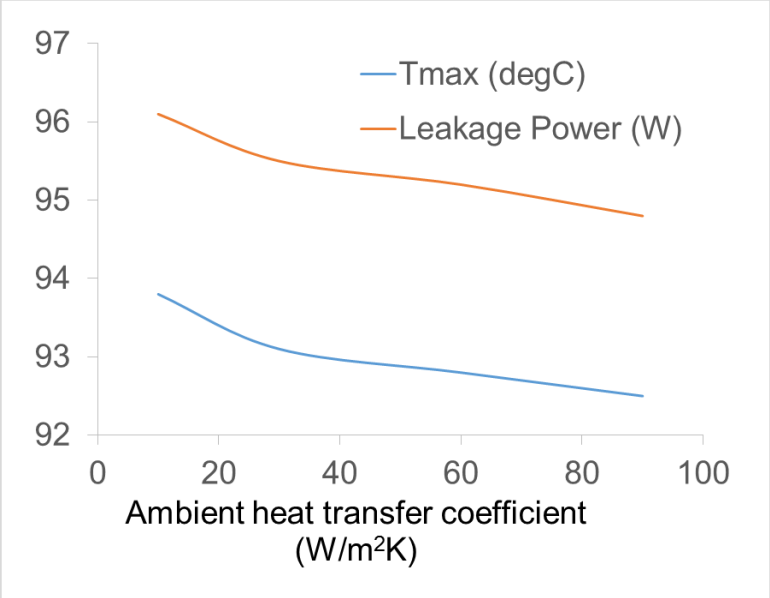


Figure 5.14: Effect of ambient heat transfer coefficient on the maximum temperature and leakage power.

Figure 5.14 shows that when the ambient heat transfer coefficient increased from 10 W/m^2K to 90 W/m^2K, the maximum temperature decreased by 1.3 °C, and the leakage

power decreased by 1.3 W. The ambient heat transfer coefficient was much smaller than that for microfluidic cooling, so most of the heat was removed by the fluid. With the microfluidic cooling, there would be no need to use air cooling.

In the present study, the inlet fluid temperature was assumed to be the ambient temperature. Figure 5.15 shows that when ambient temperature increased from 10 °C to 40 °C, the maximum temperature increased from 76.7 °C to 151.2 °C, and leakage power increased from 77.4 W to 167.6 W. The increase of temperature and leakage power was not linear because when the temperature increased, the resulting leakage power also increased, which further increased the temperature. The high temperature could cause device failure while leakage power wastes energy. Thus, for some extreme operation environments with high ambient temperature, a chiller may be needed to cool down the inlet fluid, and thus reduce the junction temperature and leakage power dissipation.

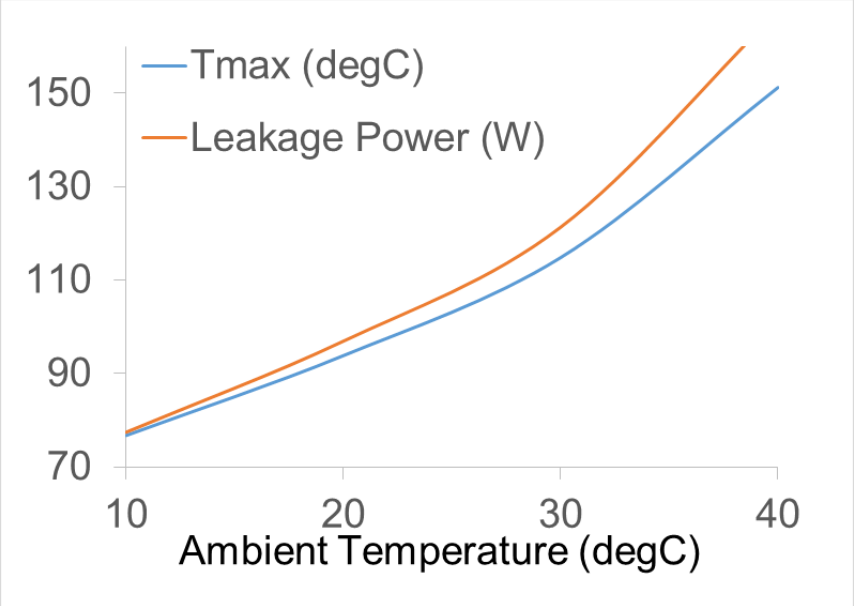


Figure 5.15: Effect of ambient temperature on the maximum temperature and leakage power.

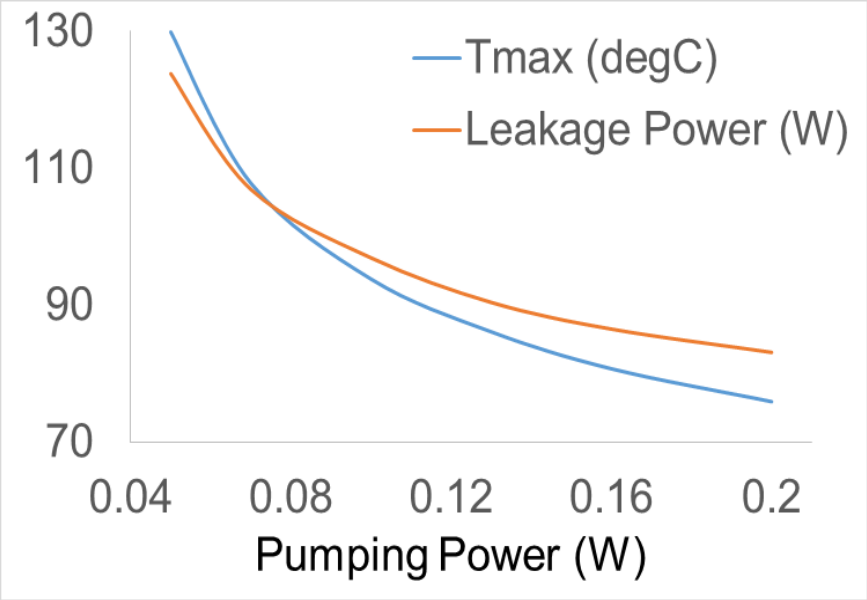


Figure 5.16: Effect of pumping power on the maximum temperature and leakage power.

Figure 5.16 shows the effect of pumping power on the maximum temperature and leakage power. As the pumping power increased from 0.05 W to 0.2 W, the maximum temperature decreased from 129.9 ˚C to 75.9 ˚C and the leakage power decreased from 123.8 W to 83.1 W. Compared to the power consumption of the chip, the pumping power was much smaller. This demonstrates the effectiveness of on-chip microfluidic cooling.

5.3 Experimental Study of CMOS Chip Performance Enhancement through Microfluidic Cooling

Although there are several modeling studies of microprocessor thermal management with microfluidic cooling, no experiment exists to demonstrate the benefits of microfluidic cooling on a real chip, in terms of temperature and leakage power reduction. In this section, a functional chip with on-chip temperature sensors was packaged with the

fabricated microgaps. Experiments were performed to study thermal performance of chip with microfluidic cooling.

Figure 5.17 shows the field programmable thermal emulation (FPTE) die with polysilicon based resistors as heaters [92]. The thermal sensors were bi-polar junction technology (BJT) based, for directly measuring substrate temperature. There were 5 digitally controllable structures composed of NMOS transistors and diffusion resistors. When all NMOS devices were turned off, measuring current flowing through the structure represented leakage current. External current sensors were used to measure this leakage current. The leakage sensor captured the effect of temperature on subthreshold current. The on-chip temperature sensors directly sensed the junction temperature and transient temperature pattern. The test-chip was fabricated in 130nm (Figure 5.17). After checking its functionality and ability to emulate various power patterns, temperature variations under actual conditions were recorded.

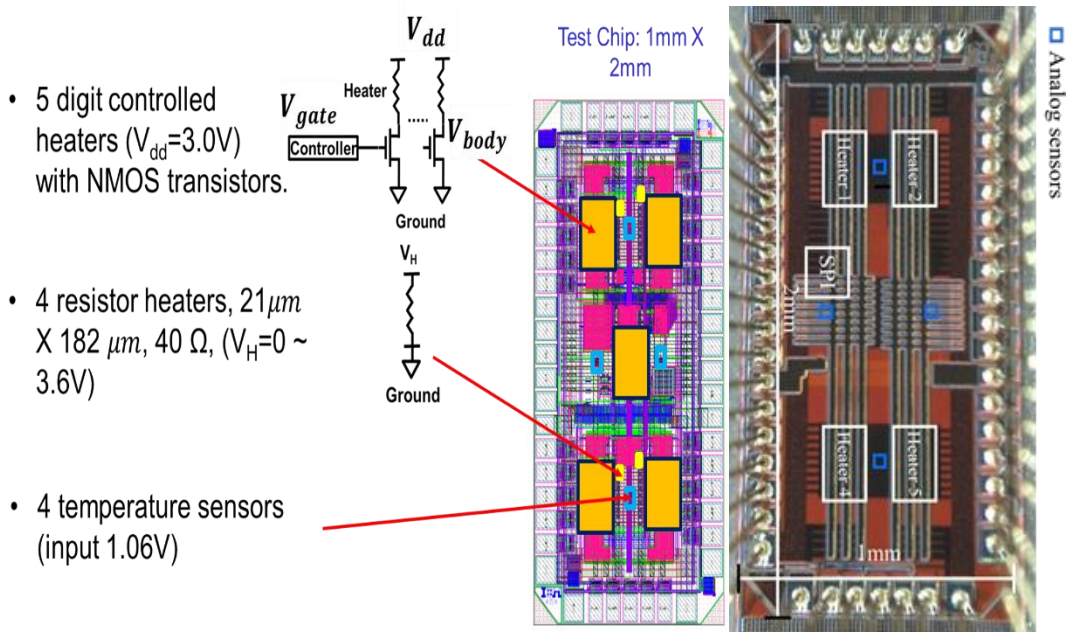


Figure 5.17: CMOS Chip layout and die-photo [92].

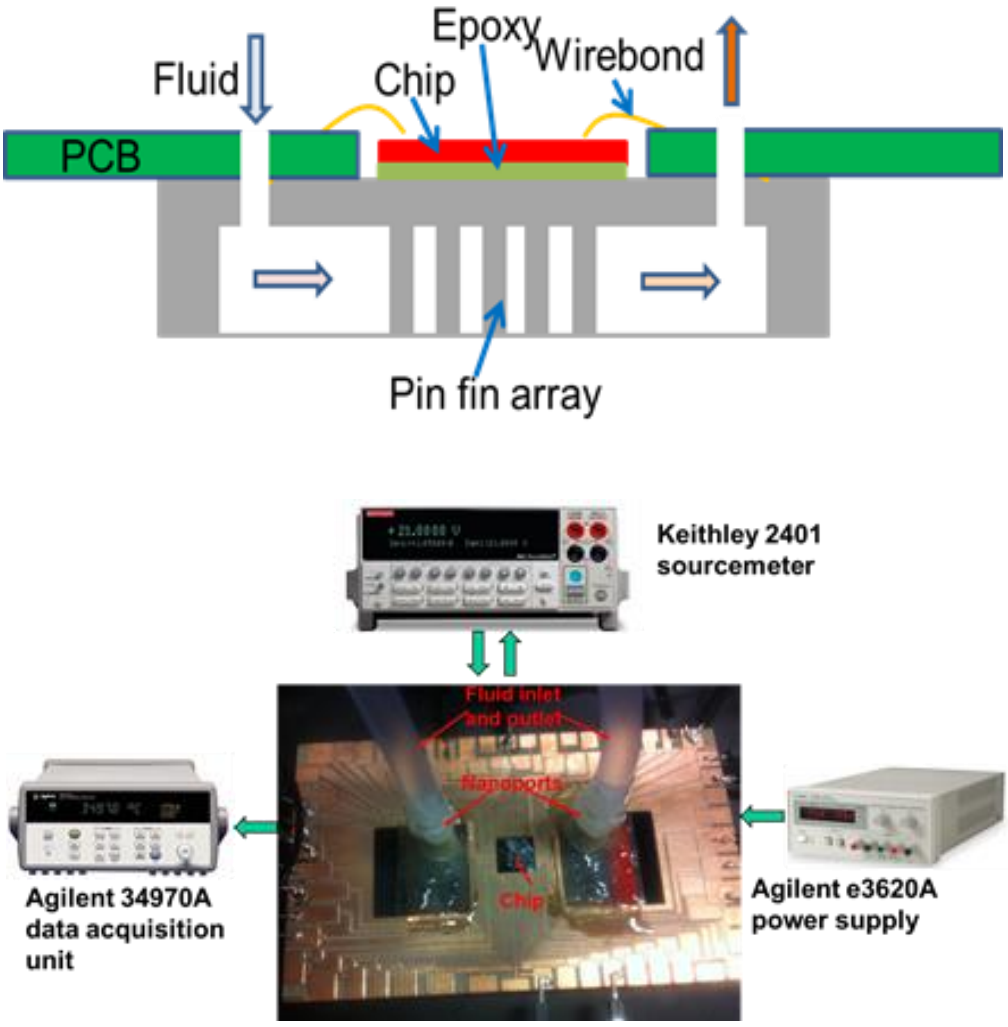


Figure 5.18: Schematic and experimental assembly of CMOS chip, microgap, PCB.

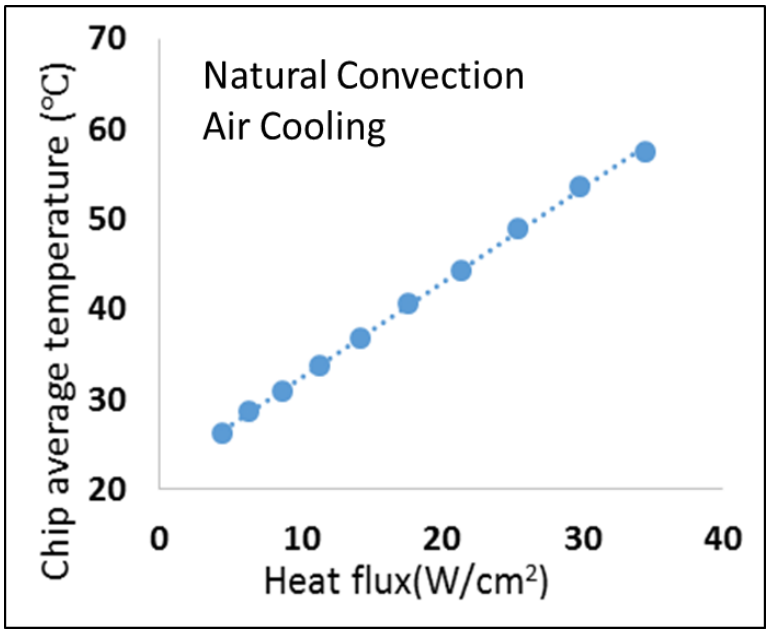
Figure 5.18 shows the schematic and experimental assembly of the CMOS chip, microgap, and PCB. The CMOS chip was attached to the center of the microgap by a thin layer of epoxy above the pin fin area. Then the microgap was attached to the back of PCB by tape. There was a small rectangular hole (8.3 mm x 8.3 mm) at the center of the PCB, which was used to expose the chip. The chip was then wirebonded to the PCB which was soldered and connected to the outside circuit. Agilent e3620A dual power supply was used to provide 1.06 V to the four temperature sensors, and variable power input to the resistor

heaters. Keithley 2401 sourcemeter was used to provide 3.0 V V_{dd} and measure the leakage current through the transistors. The sensor output voltages were collected by Agilent 34970A data acquisition unit and converted to temperatures. Two large rectangular holes (21.1 mm x 21.1 mm) were cut into the PCB to expose the fluid vias of the microgap. Then two nanoports were placed upon the fluid vias and attached to the microgap by epoxy. The nanoports were connected to quarter inch plastic tubes which were part of a flowloop described in Chapter 3.

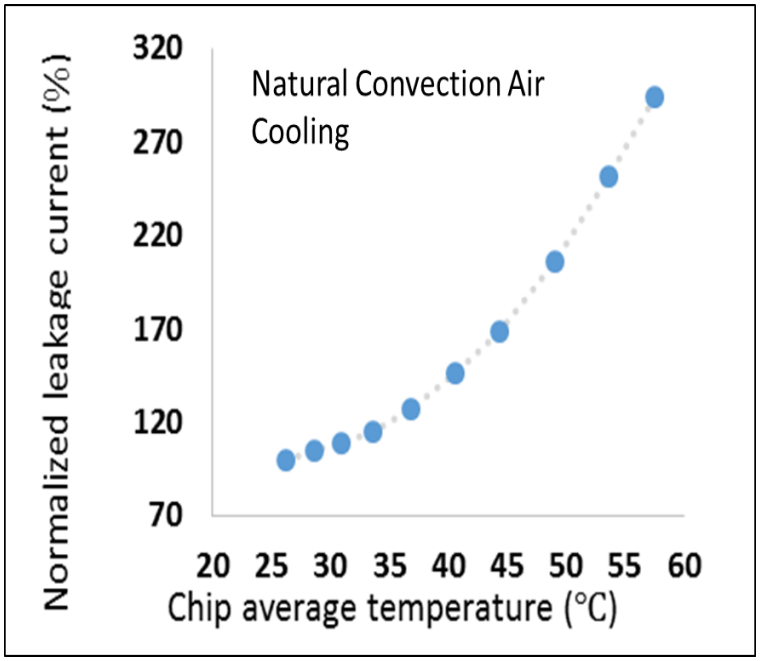
Figure 5.19(a) shows that the chip average temperature increased nearly linearly with the heat flux. The total thermal resistances included the conduction thermal resistance of the chip, epoxy, spreading resistance from the epoxy to the microgap with no fluid running, conduction thermal resistance of the silicon oxide layer, and convection resistance to the ambient. It can be calculated by [84]:

$$R = \frac{T_{chip} - T_{amb}}{Q} \tag{5.5}$$

where T_{chip} was the chip average temperature, T_{amb} was the ambient temperature, and Q was the total heater power. The total thermal resistance in Figure 5.19(a) was 52.6 K/W. Figure 5.19(b) shows that the leakage current increased exponentially with the chip average temperature, which agreed with the ref. 98. The leakage current increased by 1.9x as the temperature increased from 26.3 ℃ to 57.6 ℃. In the present study, high input power was avoided to protect the chip from damage and aging. But it is projected that the leakage current can increase significantly when the temperature increases.



(a)

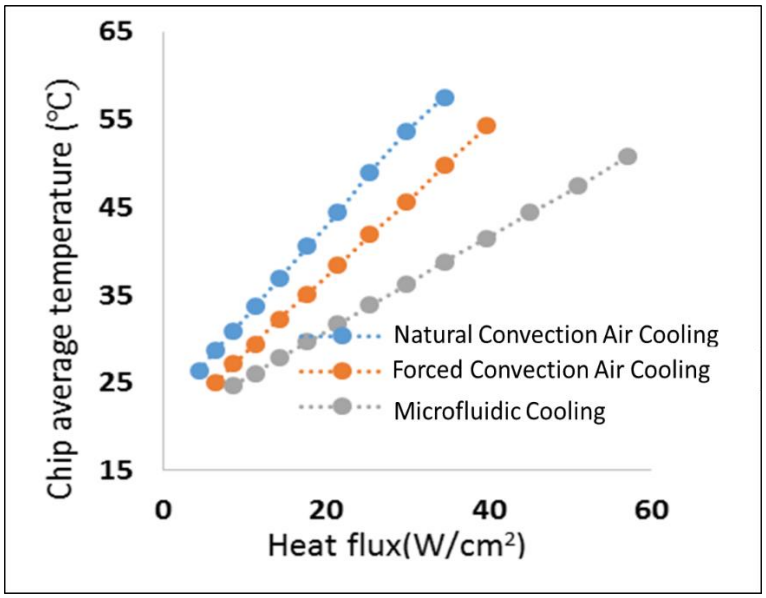


(b)

Figure 5.19: Natural convection air cooling. (a) Chip average temperature changes with heat flux, (b) Leakage current changes with chip average temperature.

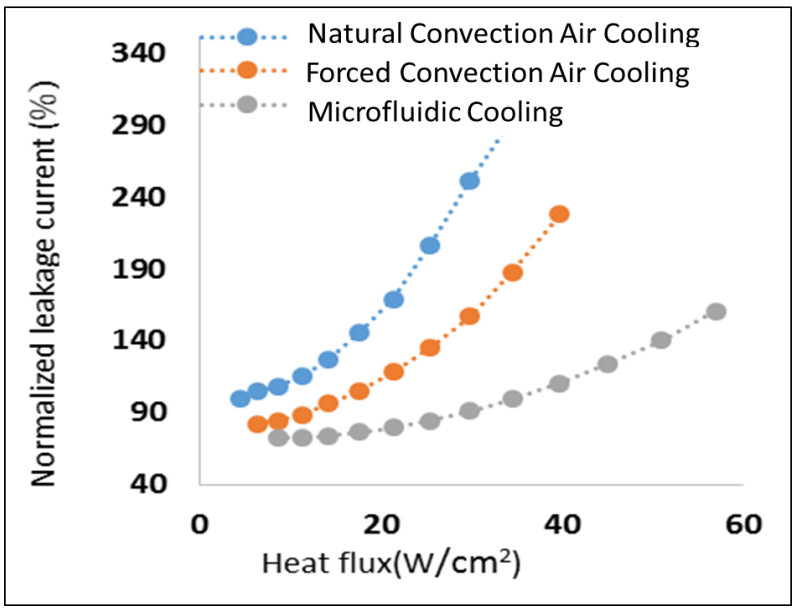
Next, three different cooling conditions were compared: natural convection air cooling, forced convection air cooling when there was no fluid running while a ROTRON

fan with 18 cfm (0.51 m^3/min) flow rate was in place above the chip, and microfluidic cooling with a flow rate 70.5 ml/min while the fan was turned off. Figure 5.20 shows the comparison. In Figure 5.20(a), the total thermal resistance of the forced air cooling was 43.6 K/W while that of the microfluidic cooling was 26.9 K/W. Compared to the natural convection air cooling, 45.1% thermal resistance reduction was achieved by the microfluidic cooling. Also, the chip average temperature was lowest under microfluidic cooling for the same power input. 18.8 ℃ temperature drop was obtained by microfluidic cooling compared to the natural air cooling when the heat flux was 34.5 W/cm^2. As the power continued to increase, the temperature difference was even larger. Figure 5.20(b) shows that microfluidic cooling gave slowest increase of the leakage current with the power increase. 66.2% leakage current saving was achieved by microfluidic cooling, compared to the natural air cooling at heat flux 34.5 W/cm^2.



(a)

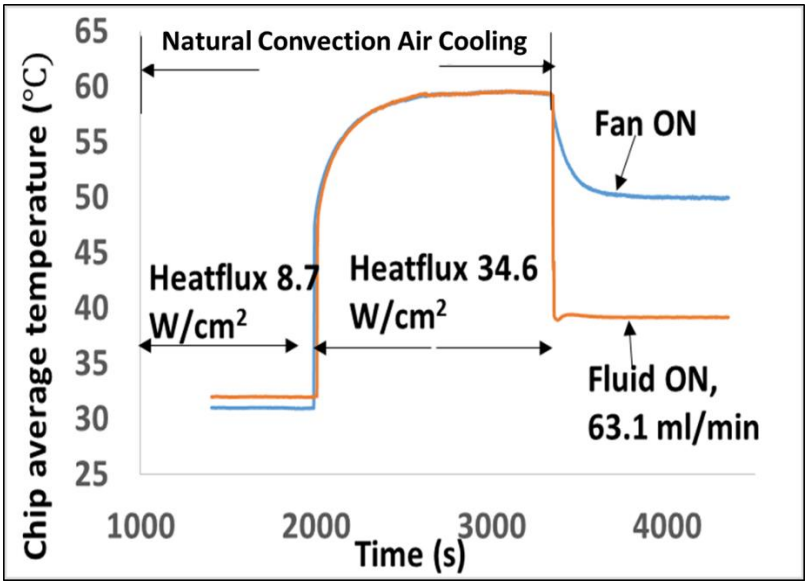
Figure 5.20: Comparison of natural convection air cooling, forced convection air cooling, and microfluidic cooling: (a) Chip average temperature changes with heat flux, (b) Leakage current changes with chip average temperature.



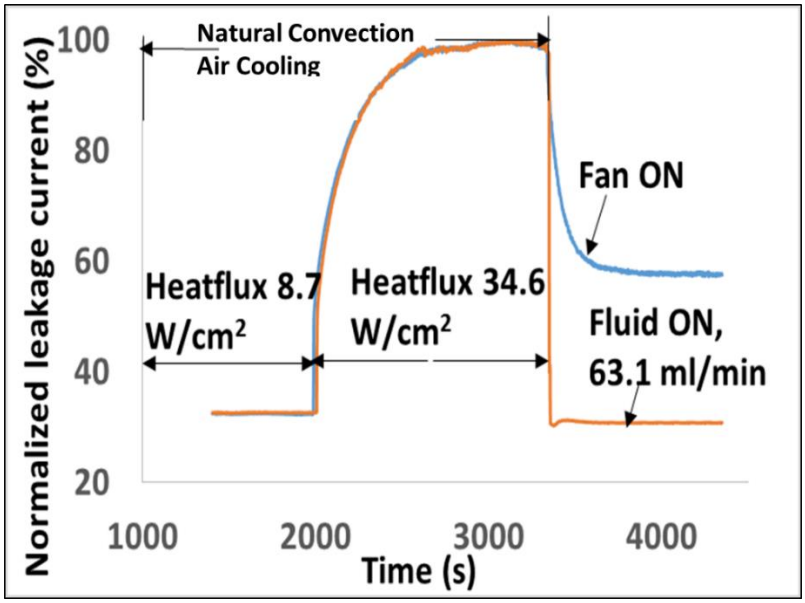
(b)

Figure 5.20 continued.

Figure 5.21 shows comparisons of the temperature and leakage response for forced air cooling and microfluidic cooling. From 0 s to 1983 s, the heat flux of the chip was 8.7 W/cm^2 with natural air cooling. At 1983 s, the heat flux jumped to 34.6 W/cm^2 suddenly and the temperature reached steady state at about 3,335 s. Two cooling conditions were tested after 3,335 s: the fan was turned on suddenly, or the fluid flow initiated suddenly at flow rate of 63.1 ml/min. It can be observed that the temperature and leakage current reached steady state at 3,881 s for the forced air cooling. However, the temperature and leakage current became steady at 3,600 s for microfluidic cooling, and the time to reach steady state was 48.5% of the forced air cooling. This means that microfluidic cooling enables rapid response to the power variation and can maintain system nearly steady.



(a)



(b)

Figure 5.21: Transient response measurement: (a) Temperature response, (b) Leakage current response.

Figure 5.22 shows the chip average temperature and leakage current at different flow rates. It can be seen that the temperature and leakage current decreased only about 7.2% and 9.9% as the flow rate increased from 5.9 ml/min to 77.9 ml/min. This was because the

dominant thermal resistance was conduction thermal resistance across the chip, epoxy, and silicon oxide, while the convection resistance of the microfluidic cooling was a much smaller fraction of the total thermal resistance.

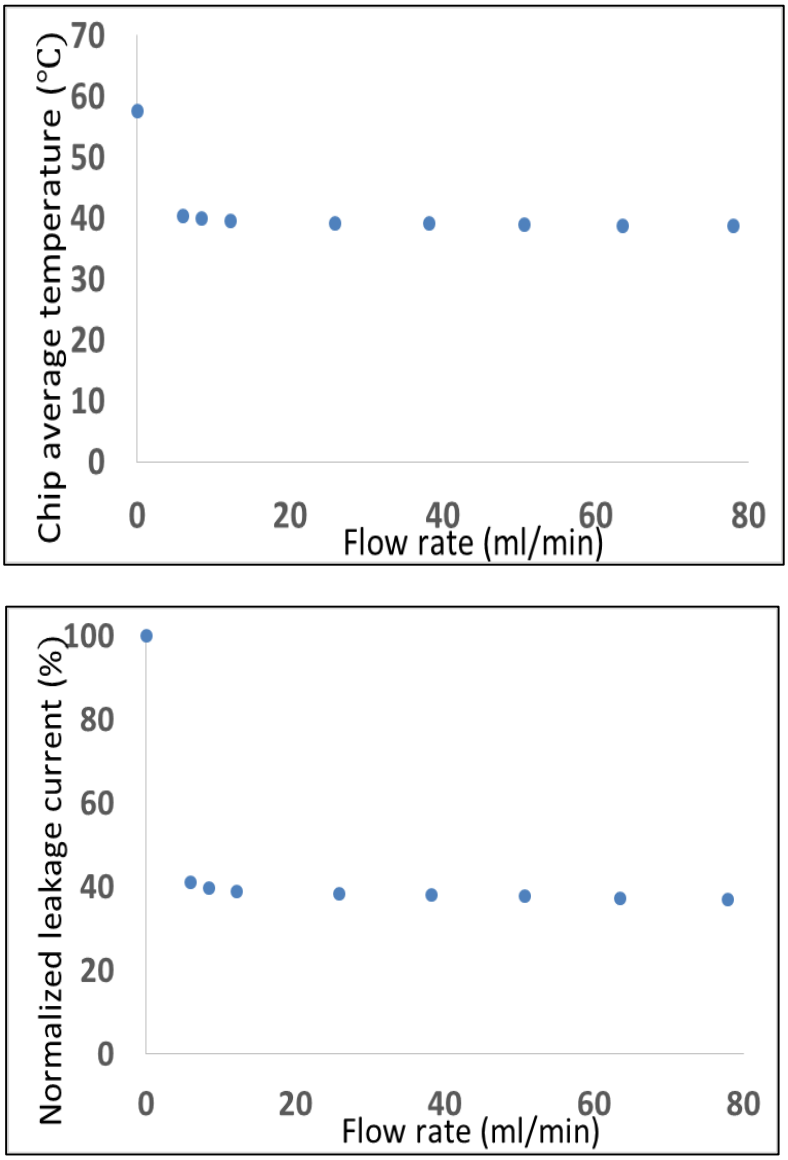


Figure 5.22: Chip average temperature and leakage current at different flow rates.

In the present study, the chip used was a 130 nm CMOS chip. For deep submicron process technology nodes (65 nm and below), the total power consumption expected to be much higher and the leakage power is also increased due to the decrease of threshold

voltage in accordance with the decreasing supply voltage. So microfluidic cooling is a solution for performance improvement and leakage reduction of future high performance electronics. In the experiment, the chip was externally attached to the microgap, which resulted in additional thermal resistances from conduction within epoxy, silicon oxide layer, and spreading resistance from epoxy to microgap. The conduction resistances of epoxy and silicon oxide were large due to their low thermal conductivities. So a more efficient cooling technique is embedded cooling-etching the microgap directly at the back of the chip. This could significantly reduce the thermal path and thus the resistance. A thermal resistance of 0.24 K/W has been reported for embedded cooling [93].

5.4 Summary

In this Chapter, the benefits of microfluidic cooling on 3D stacked ICs have been studied by both modelling and experiments. The main observations are:

(1) The leakage power amounted to 55.8% of the dynamic power and needed to be considered in the simulation.

(2) The temperature of the memory tier with low power consumption could be higher than that of processor tier due to the microfluidic layout.

(3) Ambient heat transfer coefficient had very weak effect on the maximum temperature and leakage power. Increasing the ambient temperature could increase the maximum temperature and leakage power significantly.

(4) The pumping power was much smaller than the power consumption of the chip. Increasing the pumping power could significantly reduce the maximum temperature and leakage power.

(5) Microfluidic cooling can achieve 45.1% thermal resistance reduction, and 18.8 ℃ temperature decrease compared to natural convection air cooling. For high power chips, the temperature drop between air cooling and microfluidic cooling will be even higher.

(6) The leakage current increased exponentially with the power, and thus the temperature. Under same power consumption, microfluidic cooling showed 66.2% leakage current saving.

(7) The time to reach steady state in response of sudden application of microfluidic cooling was only 48.5% of forced air cooling.

CHAPTER 6

FLOW BOILING OF HFE 7200 AND METHANOL MIXTURES IN PIN FIN ENHANCED MICROGAPS

Although single phase liquid cooling in surface enhanced microstructure has excellent thermal performance, the temperature nonuniformity due to the bulk fluid temperature rise is a concern. Flow boiling which takes advantage of the latent heat can achieve much higher heat transfer coefficients than single phase liquid cooling. The bulk fluid temperature in flow boiling depends on the saturation pressure which decreases along the flow path, and thus can reduce the temperature nonuniformity compared to single phase liquid cooling. Fluid properties affect the flow boiling performance. Earlier work on flow boiling uses liquids such as water, and alcohol. These fluid have good thermal properties. However, they have lower dielectric strength, and larger surface tension compared to dielectric fluids. For direct on-chip microfluidic cooling, dielectric fluids are preferred. But dielectric fluids usually have lower latent heat, and lower thermal conductivities. In this Chapter, flow boiling experiments using HFE 7200 were performed first as a baseline study. The effects of dissolved gas, mass flux, power map on the thermal performance were studied. Addition of methanol into HFE 7200 was next explored as a potential method to enhance the flow boiling thermal performance.

6.1 Leakage Test and Fluid Preparation

Different from water, both HFE 7200 and Methanol are very volatile. The liquid might leak to the ambient unnoticeably. So before the experiment, leakage test was required, which was performed at both high pressure and under vacuum conditions. First,

the flow loop was charged with compressed dry air after the device was connected. When the pressure transducer reading reached about 200 kPa absolute, the charging was stopped by closing the valve at the degassing port. The system was left at this state for 12 hours while maintaining the pressure inside the system. Next, the flow loop was evacuated by a vacuum pump until its absolute pressure reached about 4 kPa and maintained at this state for 5 hours. The flow loop was considered to be leak free if the pressure variations for both cases were less than 1.5 kPa. If there was a large change of the pressure, the flow loop was charged with high pressure air and soap was used to help identify the leak point.

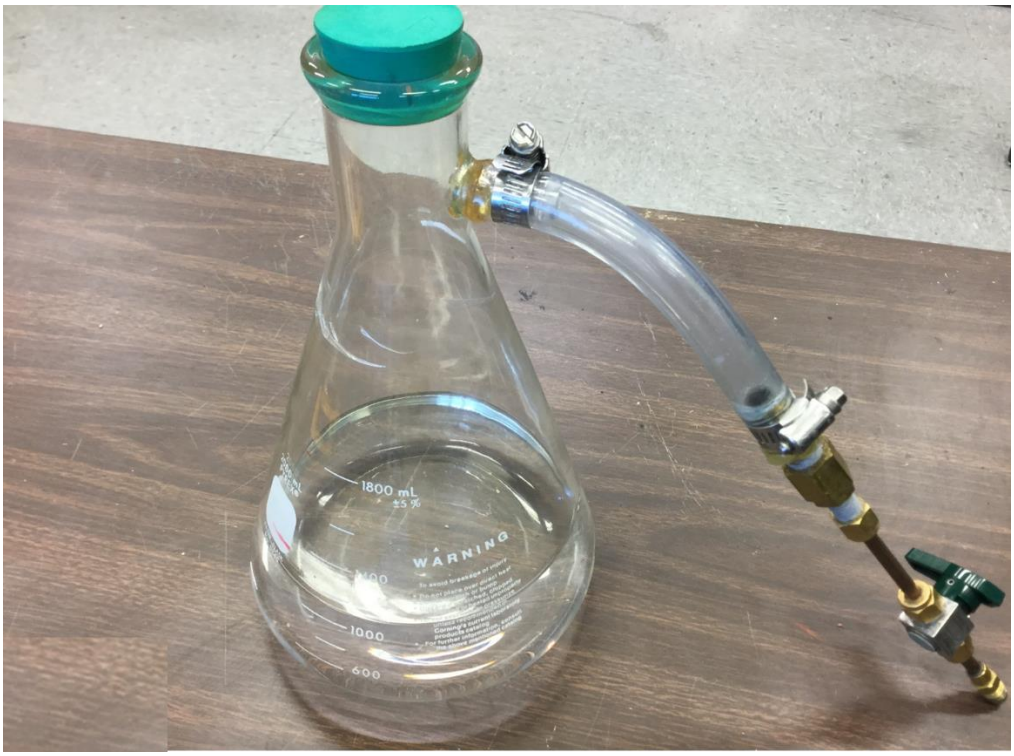


Figure 6.1: Filter flask for fluid storage and degassing.

To remove dissolved gases in the fluid, the test fluid was stored in a 1800 mL filter flask (Figure 6.1), which was connected to a vacuum pump. While the vacuum pump was running, the filter flask was stirred continuously. The valve was closed until no bubbling was observed in the fluid. Dow Corning high vacuum grease [94] was used to prevent

leakage around the tubing. The flask was left at this state for 2 hours. The above degassing process was repeated three times.

6.2 Experimental Procedure

Once the flow loop was determined to be leak-free, a vacuum pump was used to pull the system pressure down to < 4 kPa. A flexible tube was used to charge the reservoir. One end of this flexible tube was connected to the valve located at the drain/charging point. The other end was immersed into the fluid in the filter flask. While the valves before and after the reservoir were kept closed, the valve at the drain/charging point was open to allow the fluid to fill the reservoir up to the ambient pressure. Then the valve at the drain/charging point was closed, and all other valves along the flow path were kept open. All the tubing and components were covered with fiberglass insulation.

The gear pumps circulated the fluid in the flow loop. To suppress flow boiling instabilities, the controlling valve immediately before the test device was throttled while increasing the pumps speed. In this way the pressure before the controlling valve was elevated to 3 bar absolute, while the flowrate was set as wanted. With the chilled water running, the system reached steady state in usually about 2 hours. Then the power supply connected to the heaters was turned on and power incremented in steps of about 1W for low flow rate (<15 ml/min), and 2 W for high flow rate (> 15 ml/min). All temperature and pressure data were recorded once the system reached steady state.

Experiments were terminated when the system reached CHF, as determined by a sudden increase of the temperature at the end of the pin fin arrays ($\Delta T > 15$ ℃). A Phantom V211 high speed camera was used to capture the boiling in the pin fin arrays. The resolution was 1280 × 800, sampling rate was 2200 fps, and exposure time was 300 μs. It was found

that the light source also heated the device. So when not capturing video, the light intensity was kept at 5%, for which the heat from the light source was negligible. After the temperature and pressure data were recorded, light intensity was increased to 50% and the boiling was visualized. Then the light intensity was switched back to 5%.

After the experiment, the fluid in the flow loop was drained. Compressed dry air was used to flush the loop to remove any traces of the liquid. The loop was left at this state for a night before another test.

6.3 Data Reduction

The total power consumption (q_{tot}) measurement and heat loss (q_{loss}) estimation are described in Chapter 3. The effective power dissipation (q_{eff}) is the difference between q_{tot} and q_{loss}.

$$q_{eff}=q_{tot}-q_{loss} \tag{6.1}$$

So the effective heat flux is given by:

$$q''_{eff} = \frac{q_{eff}}{A_h} \tag{6.2}$$

Where A_h is the total heater area 1 cm^2.

The average heater temperature is obtained by averaging the temperatures of the 12 temperature sensors.

$$T_{ts,avg} = \frac{\sum_1^{12} T_{ts,i}}{12} \tag{6.3}$$

The base temperature of the pin fin arrays is calculated by a 1D thermal resistance method:

$$T_b = T_{ts,avg} - \frac{q_{eff}}{R_{cond}} \tag{6.4}$$

where R_{cond} includes the thermal resistance of the silicon oxide layer and si base and is given by:

$$R_{cond} = \frac{t_o}{k_o A} + \frac{t_s}{k_s A} \tag{6.5}$$

6.4 Experimental Results

Flow boiling experiment was performed to study the heat transfer performance of pure HFE 7200, and mixture of HFE 7200 and methanol at various concentration. The inlet temperature of the fluid was kept at 25 ℃. Three different volume flow rates were tested: 12.3 ml/min, 16.5 ml/min, and 20.0 ml/min. The corresponding maximum mass fluxes based on the minimum cross section area were 354.5 kg/m^2-s, 475.5 kg/m^2-s, and 576.3 kg/m^2-s, respectively. The pin fin dimensions of the microgap used were: D_P= 100 µm, S_T=200 µm, S_L=150 µm, H_P=164.7 µm.

6.4.1 Effect of Mass Flux

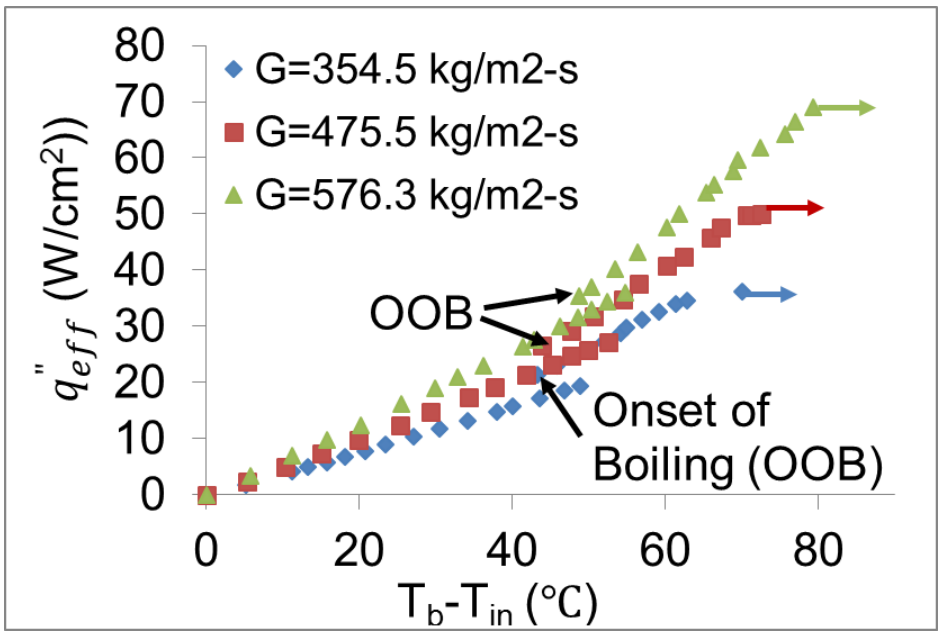
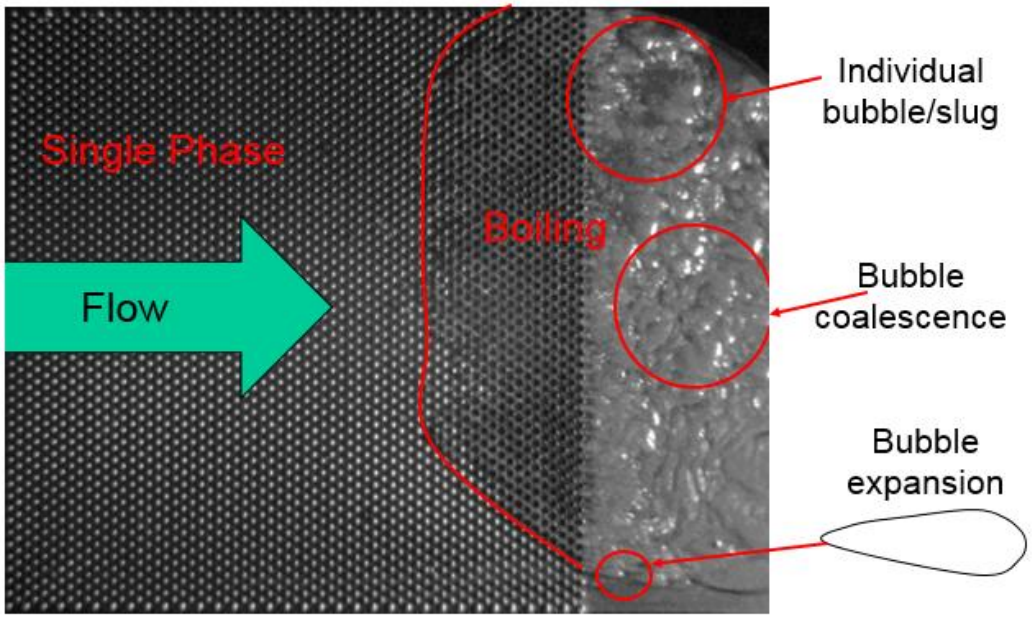


Figure 6.2: Flow boiling curves for HFE 7200 at different mass fluxes from 354.5 kg/m^2-s to 576.3 kg/m^2-s.

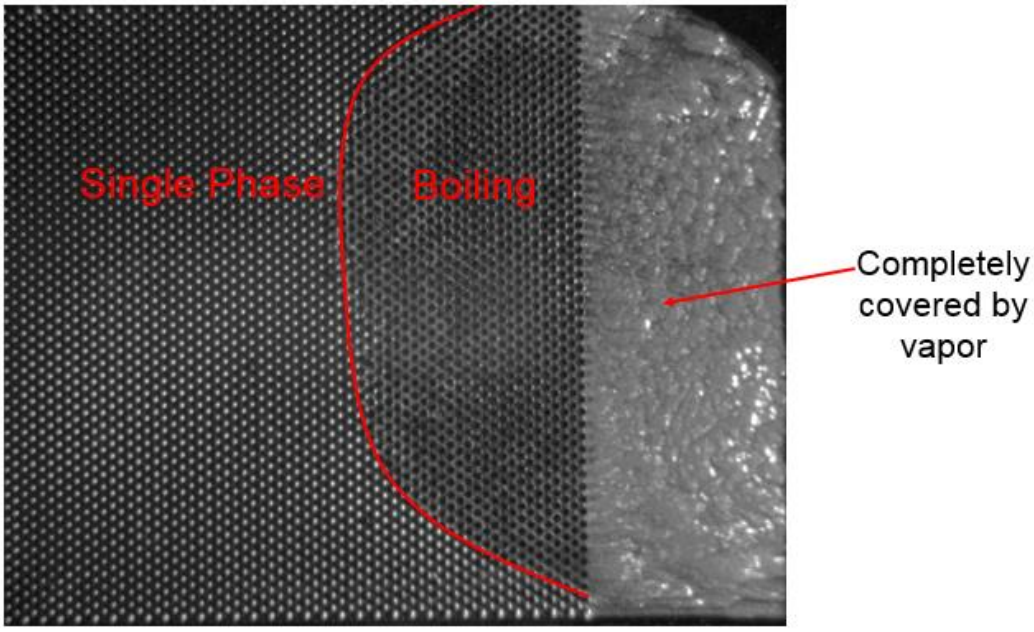
Figure 6.2 shows the flow boiling curve for pure HFE 7200 at different mass flux. The effective heat flux is plotted against the difference between average pin fin base temperature and fluid inlet temperature. Before the onset of boiling and at low heat flux, the flow was single phase flow. As the heat flux continued to increase, boiling started suddenly and the average temperature dropped significantly, as shown at the point of onset of boiling (OOB) in the figure. This was because the two phase heat transfer coefficient was much higher than single phase and the saturation temperature decreased along the flow path. In the two phase region, the slope of the boiling curve was higher than that of the single phase region. However, as the heat flux continued to increase, the slope decreased quickly. A small increase of effective heat flux resulted in significant increase of the average temperature, which indicated that the CHF had been reached. The effect of the mass fluxes on the heat transfer performance was also evident. In single phase region, higher mass fluxes had higher slopes, and thus higher heat transfer coefficients, as expected. Higher mass fluxes also showed higher heat flux and T_b-T_{in} at the onset of boiling. The critical heat flux was observed to increase with mass flux.

Figure 6.3 shows the flow pattern for mass flux at 576.3 kg/m^2-s at different heat flux. The flow direction was from left to right. At low heat flux q''_{eff}=35.4 W/cm^2, individual bubbles and slug can be observed downstream of the pin fin array, indicating bubbly/slug flow. The bubbles were generated and coalesced into larger bubbles. It can be also observed that the bubbles expanded in the flow direction. As the heat flux increased to q''_{eff}=47.5 W/cm^2, the area of two phase region increased. The bubble density and frequency increased significantly, as did bubble coalescence. Few individual bubbles can be observed, indicating an annular flow regime. As the heat flux increased to q''_{eff}=66.4

W/cm^2, dryout occurred at the end of the pin fin array and the temperatures in that part increased significantly.

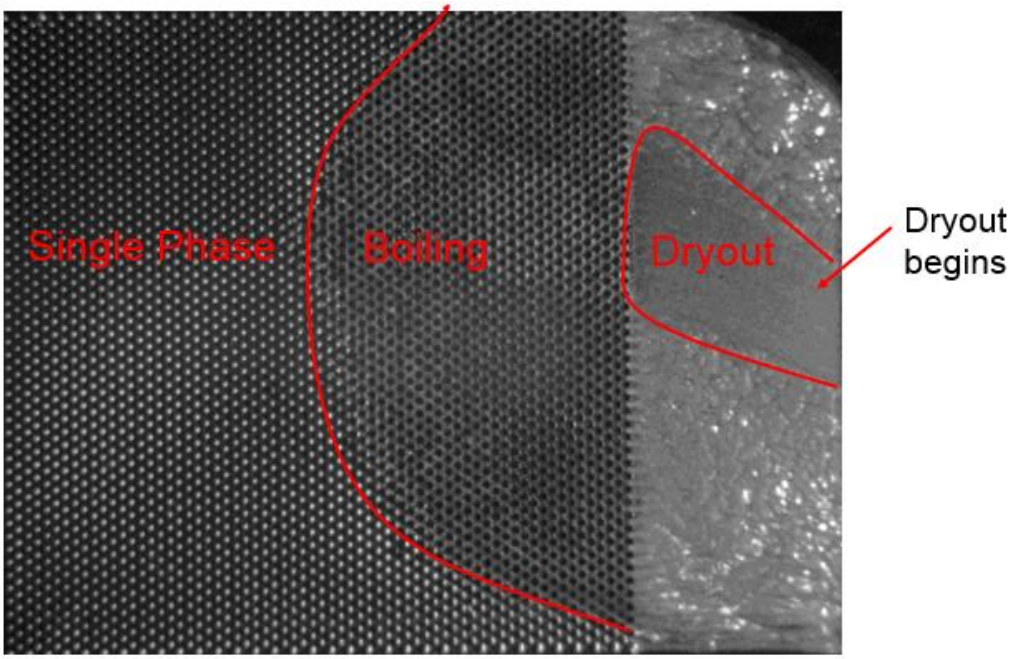


(a)

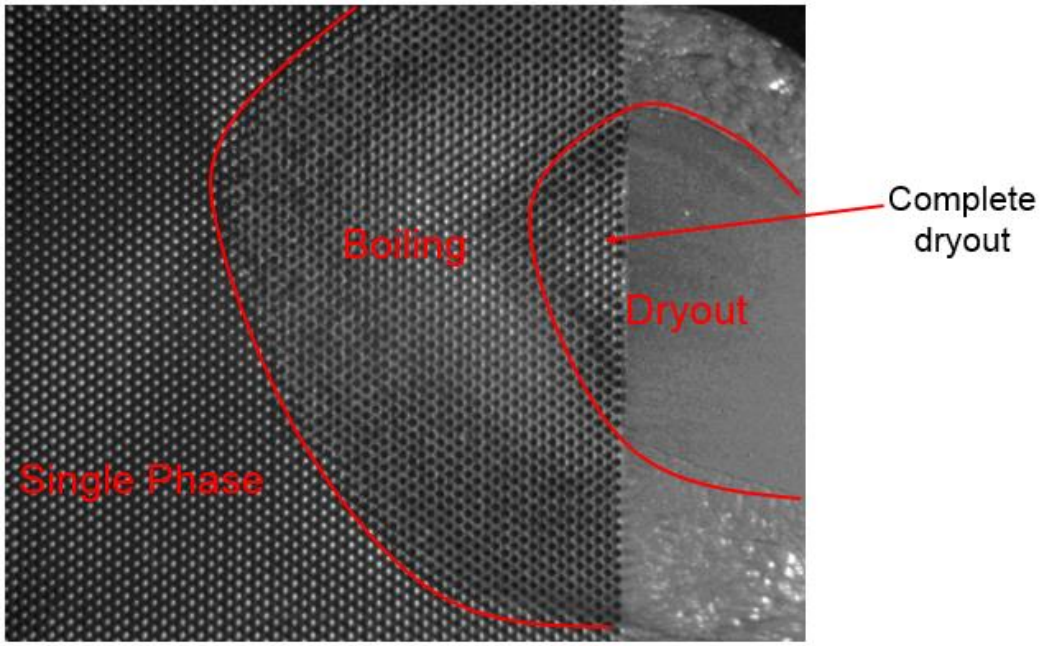


(b)

Figure 6.3: Flow patterns at different heat fluxes illustrating the flow boiling regime development until dryout occurs, G=576.3 kg/m^2-s, H_p=164.7 μm: (a) q''_{eff}=35.4 W/cm^2, (b) q''_{eff}=47.5 W/cm^2, (c) q''_{eff}=55.2 W/cm^2, (d) q''_{eff}=66.4 W/cm^2.



(c)

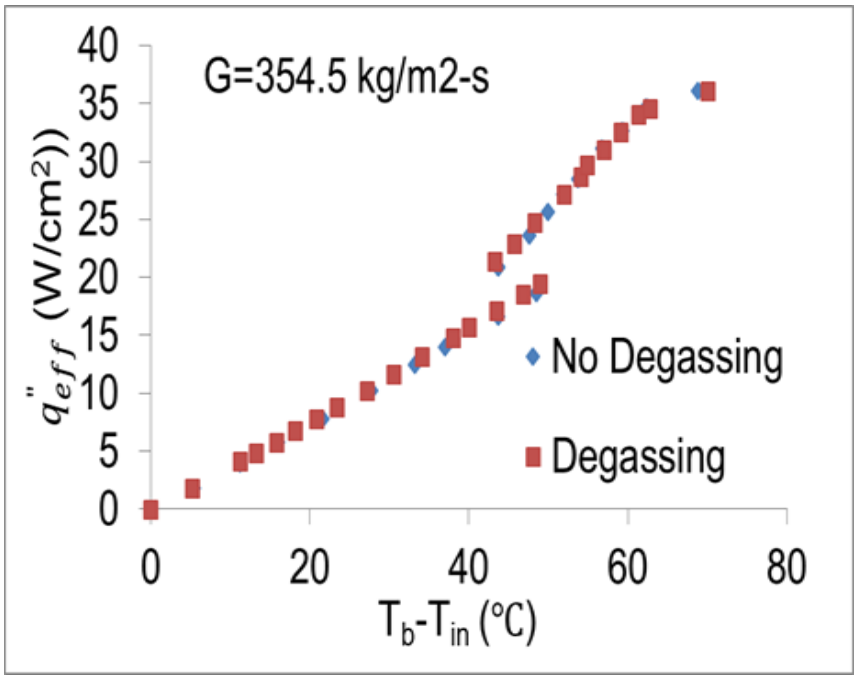


(d)

Figure 6.3 continued.

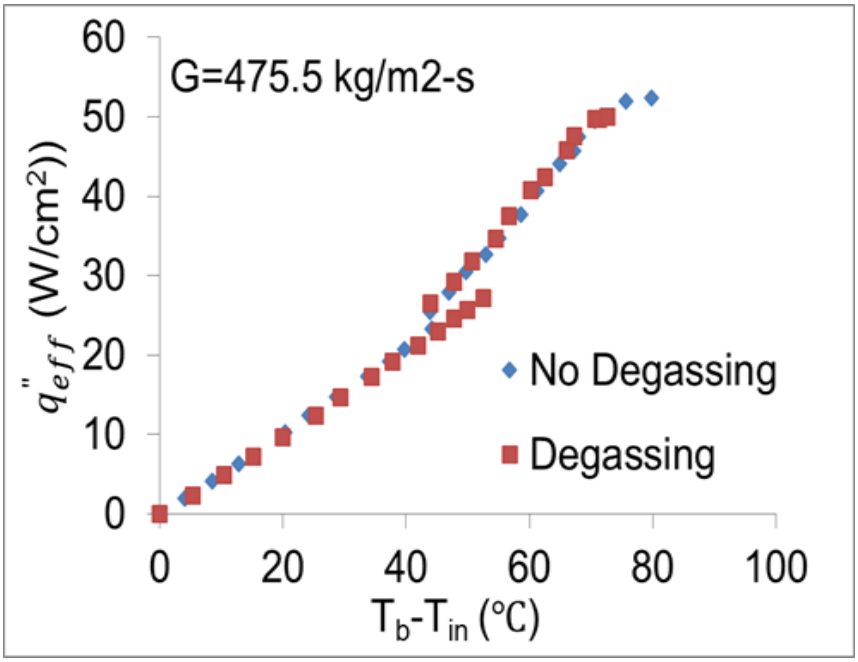
6.4.2 Effect of Dissolved Gas

In order to investigate the effects of the dissolved gas on flow boiling, experiments were performed with fluid after degassing and no degassing. Figure 6.4 shows the effect of dissolved gas in flow boiling curve. In single phase region, the dissolved gas had no effect on the flow boiling curve. However, the dissolved gas helped initiate the boiling (Figure 6.5), which meant an early start of the boiling, as can be seen in Figure 6.4. However, once boiling started, the boiling curves gradually converged. This was also demonstrated by Rohsenow et al. [95].

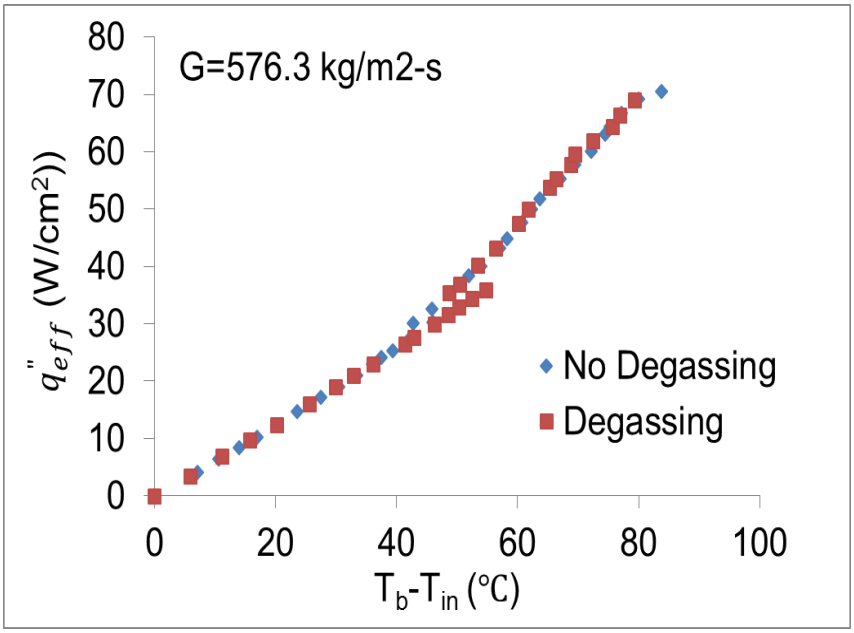


(a)

Figure 6.4: Effect of dissolved gas on flow boiling curve: (a) G= 354.5 kg/m^2-s, (b) G=475.5 kg/m^2-s, and (c) G=576.3 kg/m^2-s.



(b)



(c)

Figure 6.4 continued.

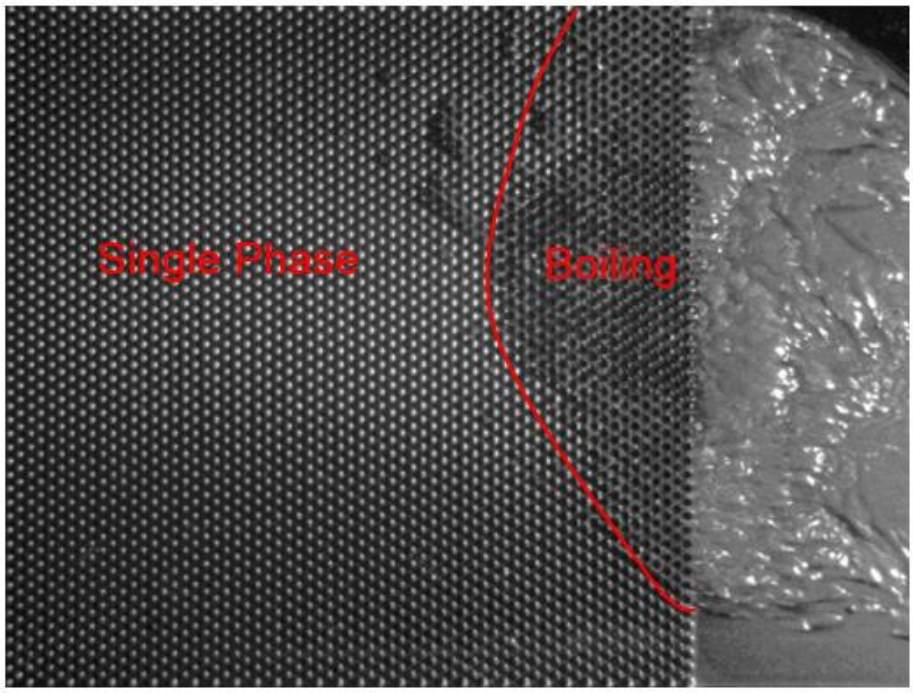
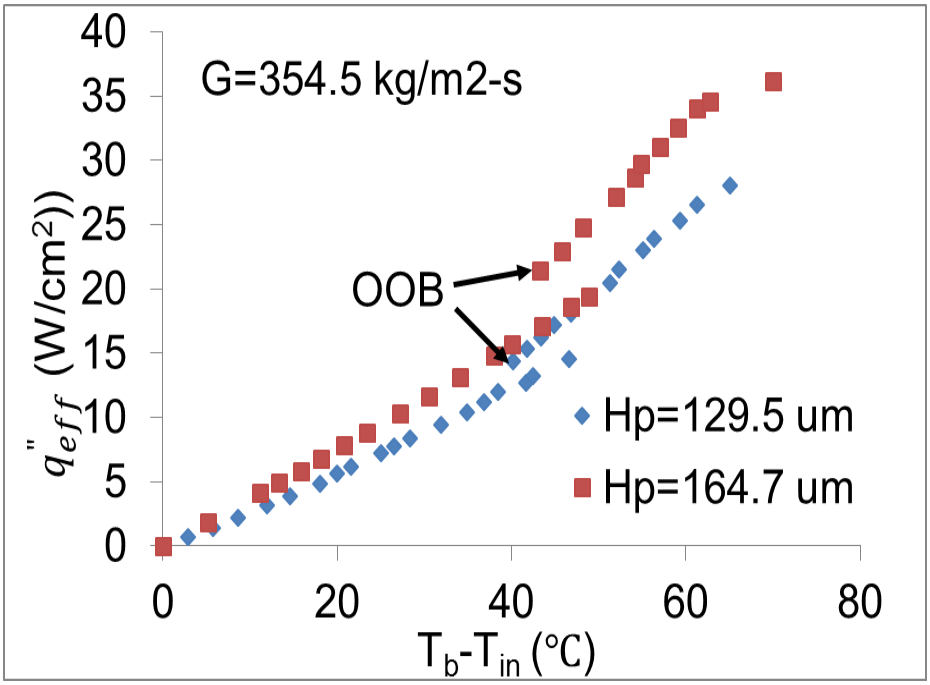


Figure 6.5: Dissolved gas induced bubbling.

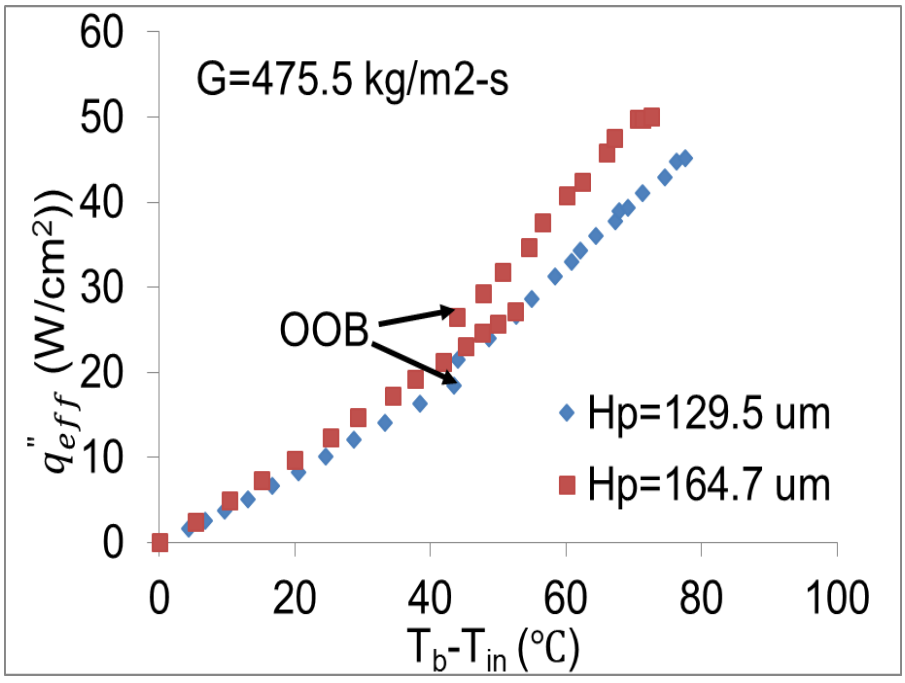
6.4.3 Effect of Gap Size

Due to the small gap size, the bubble can expand in the spanwise direction. However, the expansion in out-of-plane direction is constrained by the gap height. To investigate the effect of gap height on the heat transfer performance, experiments were performed with device dimensions: D_P= 100 μm, S_T=200 μm, S_L=150 μm, H_P=129.5 μm.

The mass fluxes were the same as for the larger gap size of 164.7 μm. Figure 6.6 shows the comparison of the boiling curves. Under the same heat flux, the larger gap size showed smaller temperatures at all mass fluxes. Also higher CHF was achieved for larger gap size. This was also demonstrated by Katto and Ohne [96]. Although the mass fluxes were the same for the two microgap sizes, larger microgap had higher mass flow rates and thus lower bulk fluid temperature rise.

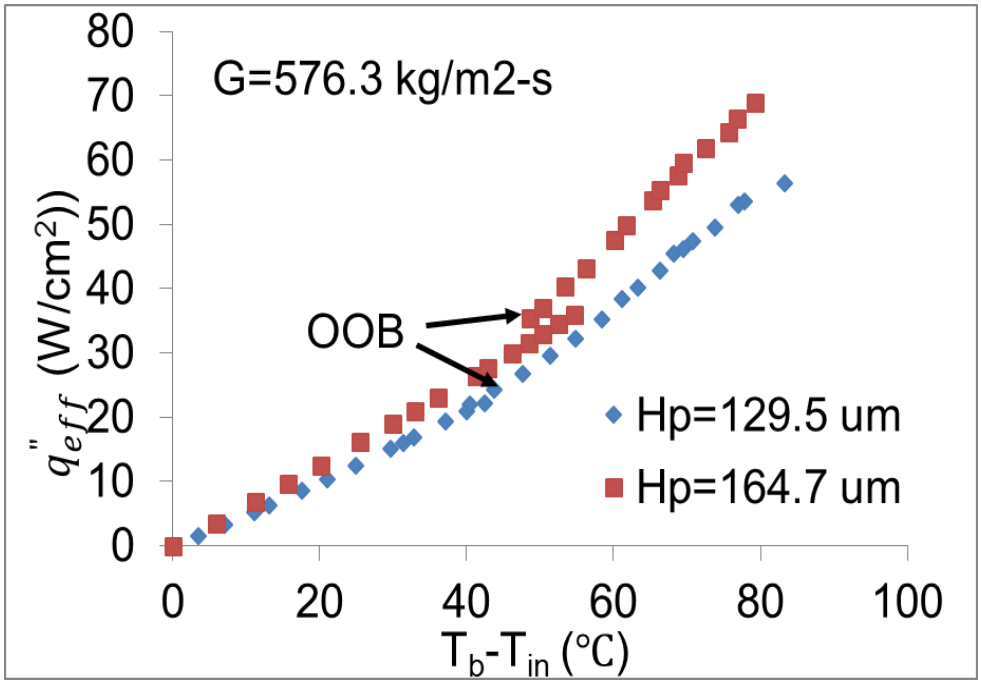


(a)



(b)

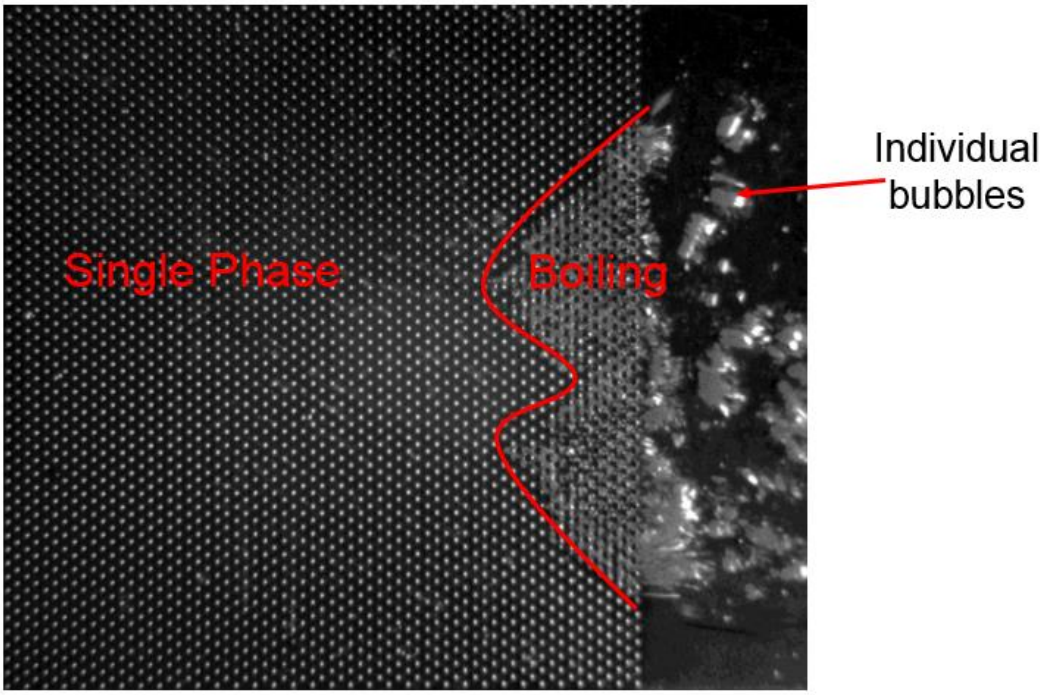
Figure 6.6: Effect of gap height on flow boiling curve: (a) G= 354.5 kg/m^2-s, (b) G=475.5 kg/m^2-s, and (c) G=576.3 kg/m^2-s.



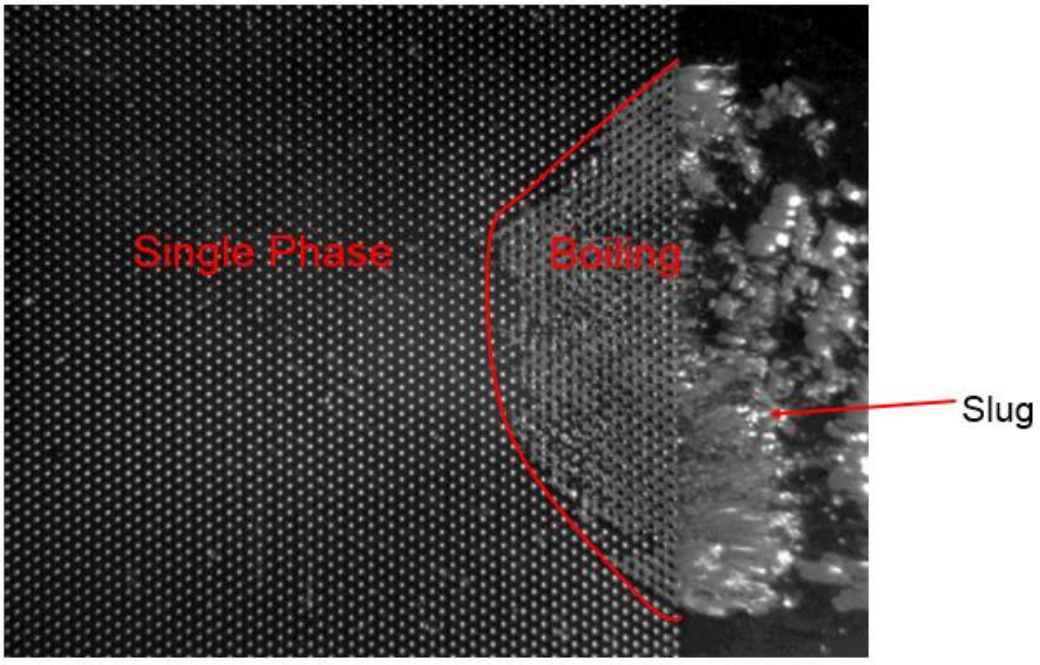
(c)

Figure 6.6 continued.

Figure 6.7 shows the flow regime transition as the heat flux increased for G=576.3 kg/m^2-s, H_p=129.5 μm. Similar to the larger gap size case, the boiling started as bubbly/slug flow and transitioned to annular flow. However, it was easy to see that the bubble size for the smaller gap size was smaller compared to the previous larger gap size.

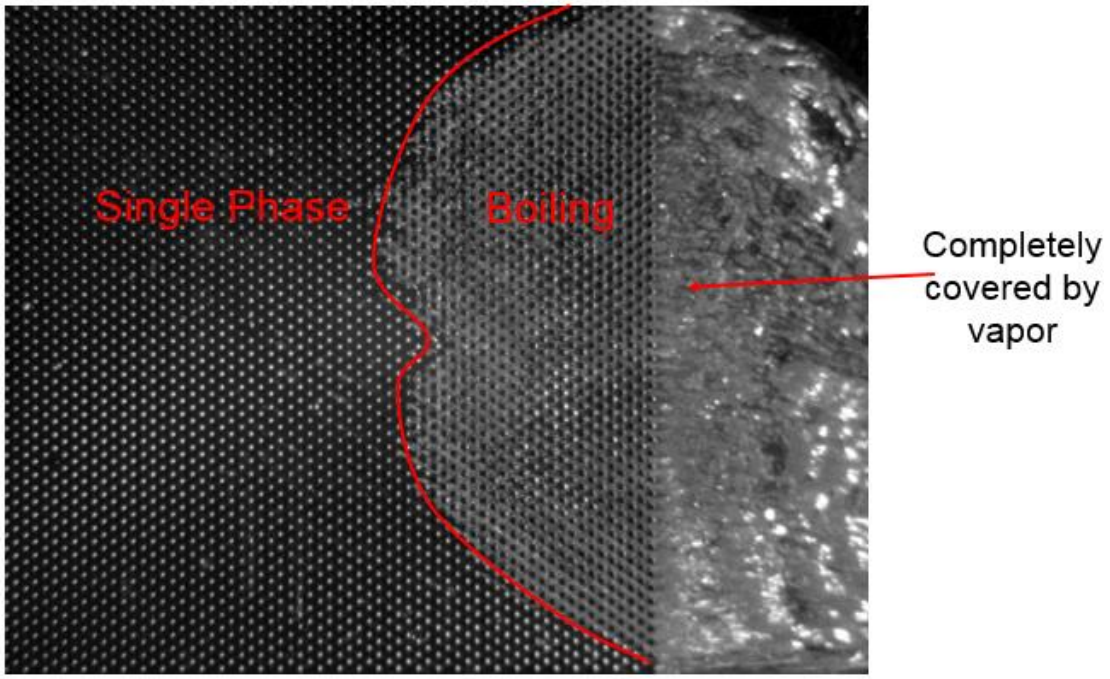


(a)

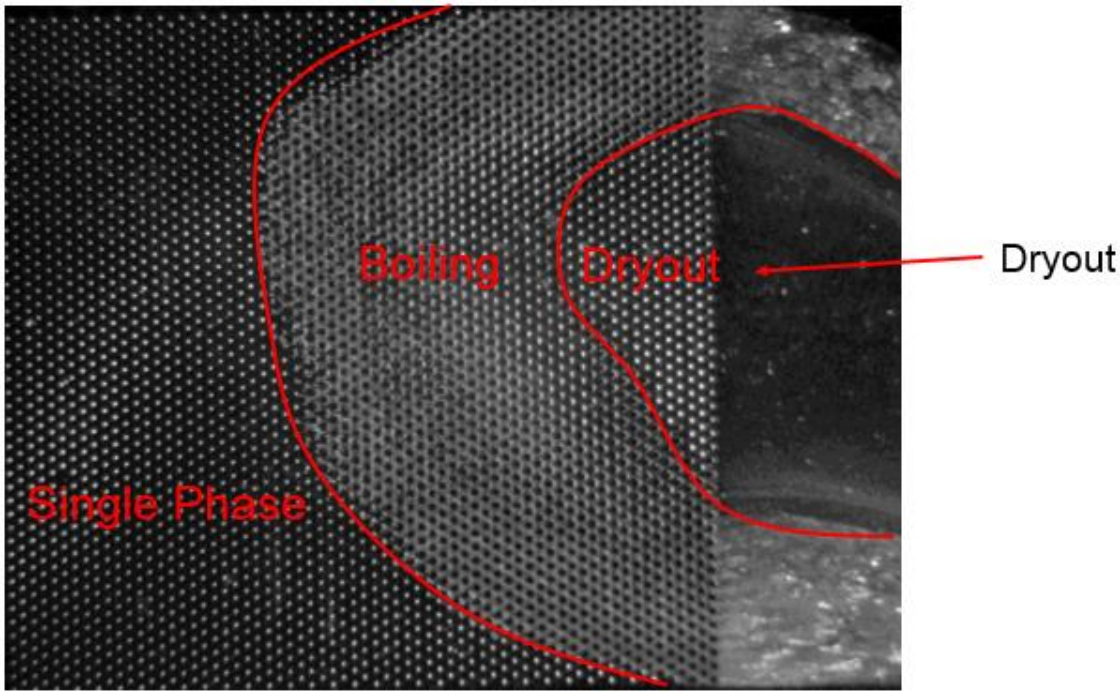


(b)

Figure 6.7: Flow patterns at different heat fluxes illustrating the flow regime transition from bubbly flow to annular flow until dry out occurs, G=576.3 kg/m^2-s, H_p=129.5 μm. (a) q''_{eff}=21.9 W/cm^2, (b) q''_{eff}=29.5 W/cm^2, (c) q''_{eff}=40.2 W/cm^2, (d) q''_{eff}=56.4 W/cm^2.



(c)



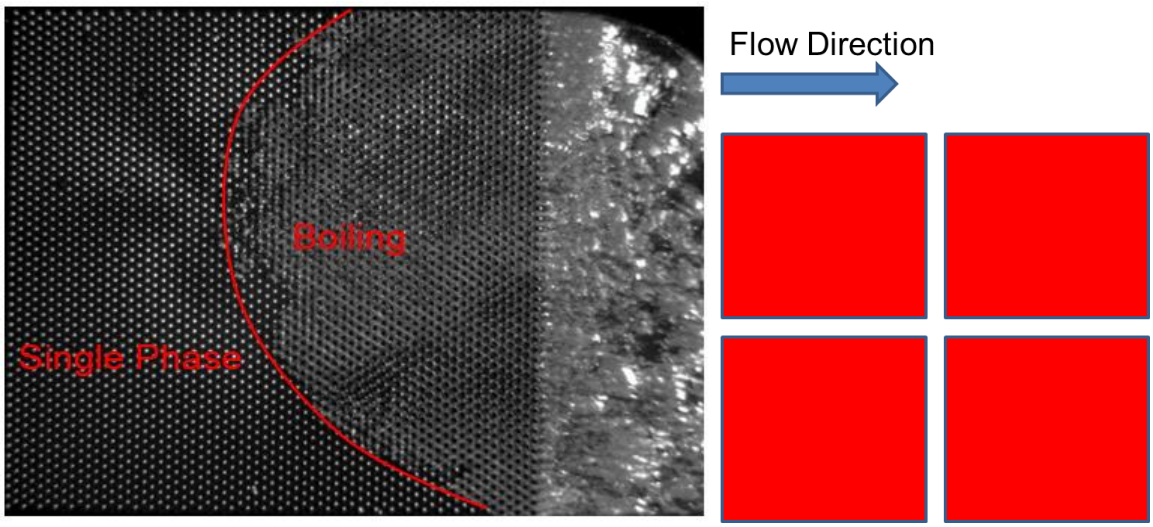
(d)

Figure 6.7 continued.

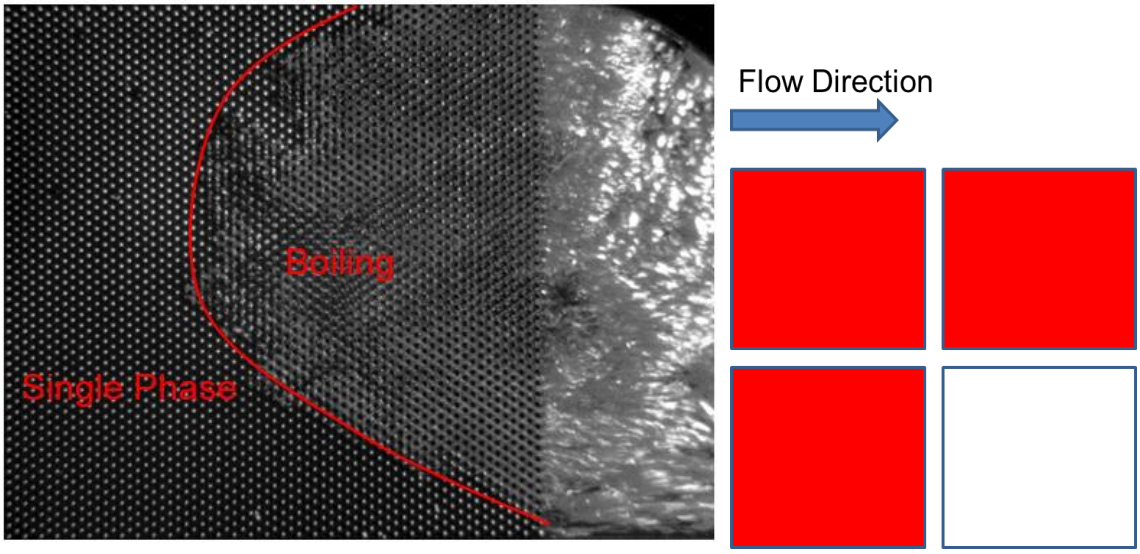
6.4.4 Effect of Non-Uniform Power Map

The power distribution on a realistic microprocessor is always nonuniform. For example, the power in logic region is much higher than in cache region. To study the effects of the power map nonuniformity on the flow pattern, experiments were performed with different power maps by switching on or off some of the heaters. Figure 6.8 shows the flow pattern for different power maps. The flow pattern was symmetric when the power map was symmetric along the flow path (Figure 6.8(a),(g),(h)). All other power maps were non-symmetric, resulting in non-symmetric boiling. The boiling always occurred above the high heat flux region. Since the flow resistance in the vapor region was much larger than in the liquid, the fluid bypassed the high heat flux region, which could be easily observed in Figure 6.8(e),(f),(i). The critical heat flux increased with mass flux. So a reduced mass flux resulted in a decrease of the CHF. However, in single phase liquid cooling, the non-uniform heating does not lead to a non-uniform flow. These flow patterns with different power maps also provided useful information about the configurations of the floorplan. For example, Figure 6.8(f)(g)(h) all had two active heaters and two inactive heaters. The symmetric power map in Figure 6.8(g) showed more uniform flow and thus better thermal performance. By placing the two active heaters upstream (Figure 6.8 (h)), boiling occurred across the entire pin fin area, even in the area with inactive heaters. That meant the boiling was heating up the inactive heaters, which was not desirable. Also the upstream pressure was higher, resulting in higher saturation temperature. If the two active heaters were placed downstream as shown in Figure 6.8(g), the incoming cool liquid won't heat up the two inactive heaters. Another problem with the non-uniform power map was the transient response of the system. When the power map changed from one pattern to another pattern,

the flow boiling pattern, pressure, and temperature also changed, which further increased the instability of flow boiling. The temperature fluctuations caused by two phase flow boiling instabilities under nonuniform heating for microchannel have been demonstrated by Bogojevic et al. [97].

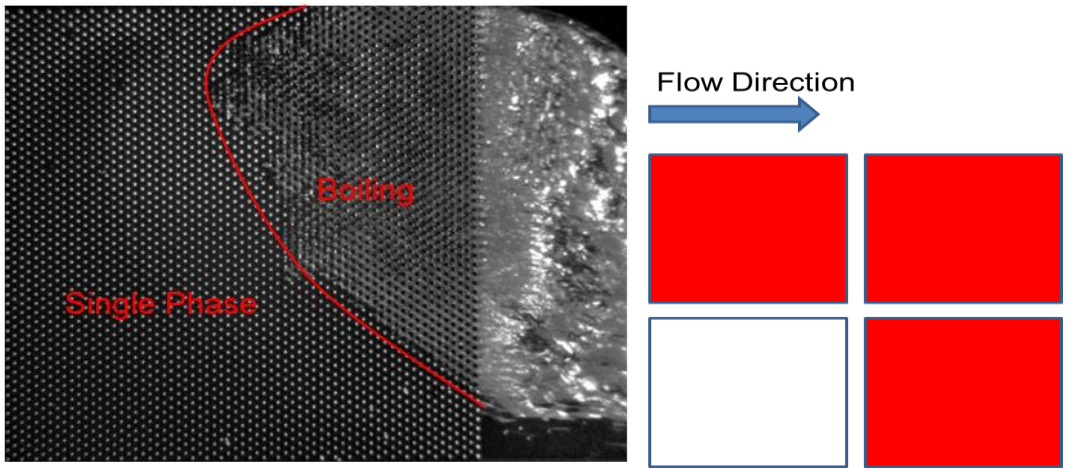


(a)

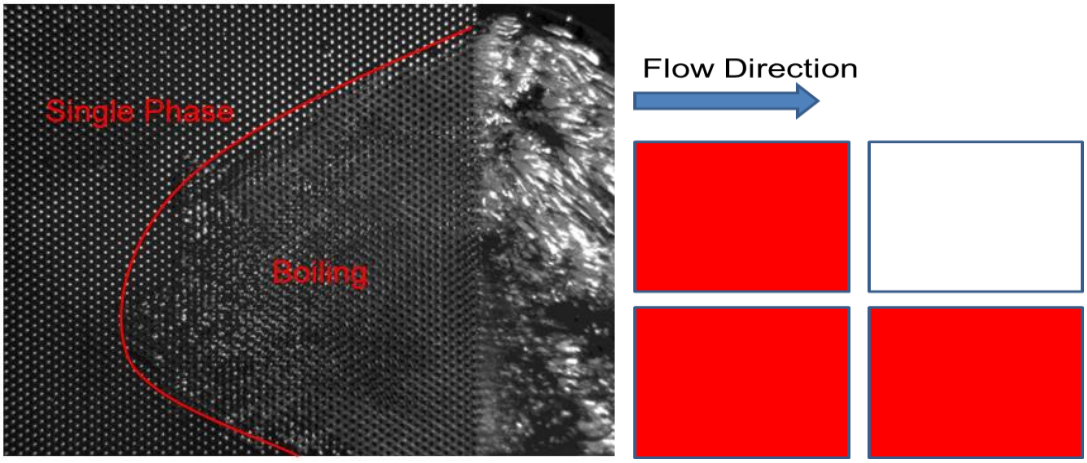


(b)

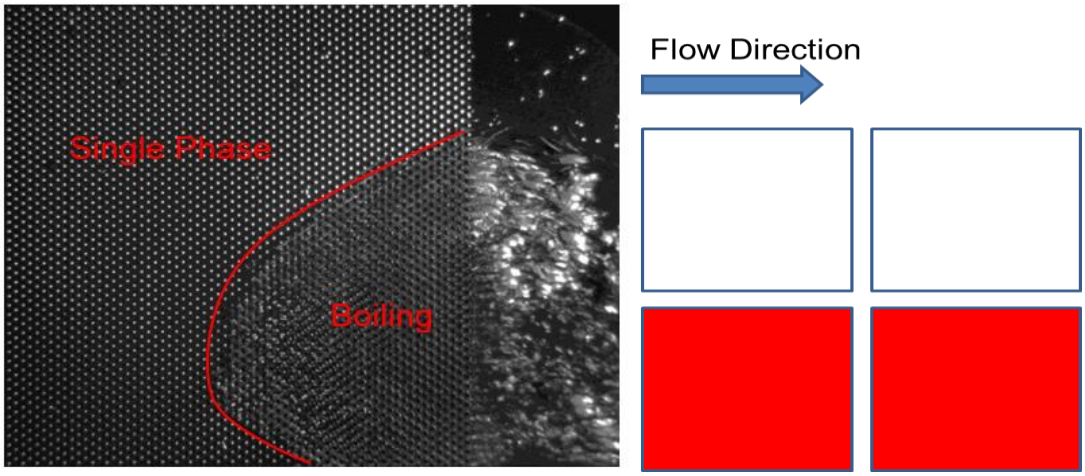
Figure 6.8: Flow patterns for different powermaps with nonuniform heating showing non-uniform heating results in non-uniform boiling, red block means heater on, white block means heater off.



(c)

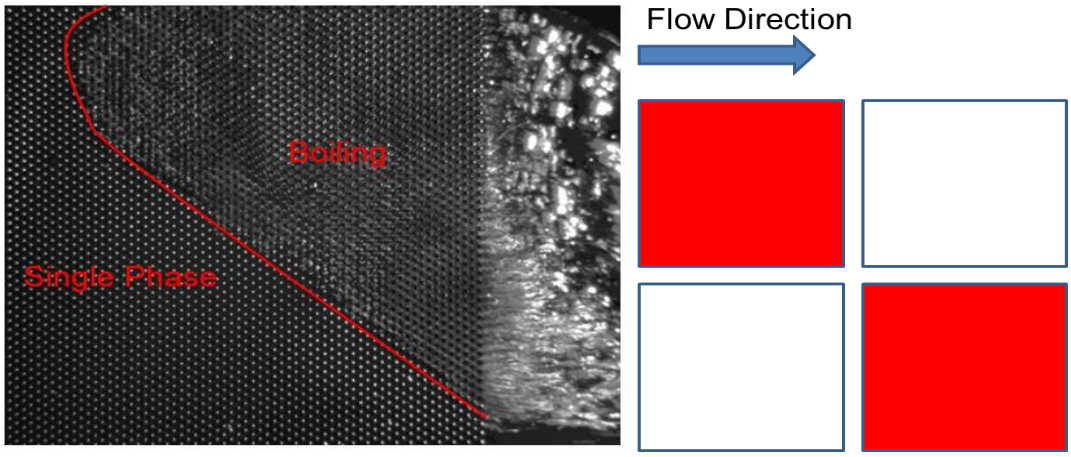


(d)

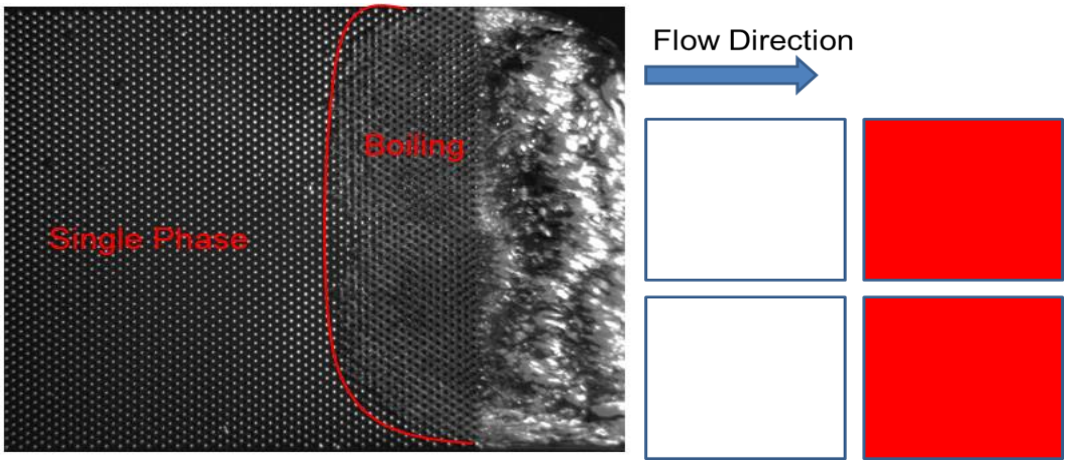


(e)

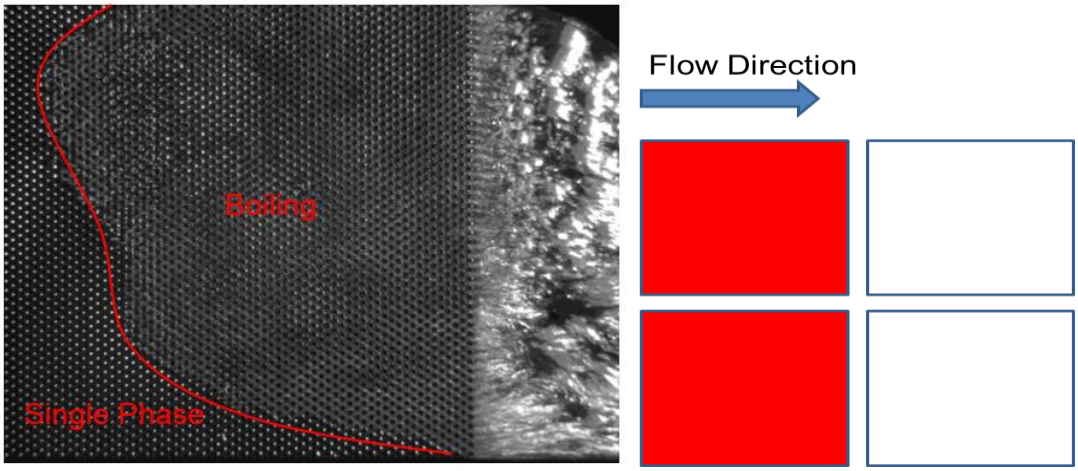
Figure 6.8 continued.



(f)

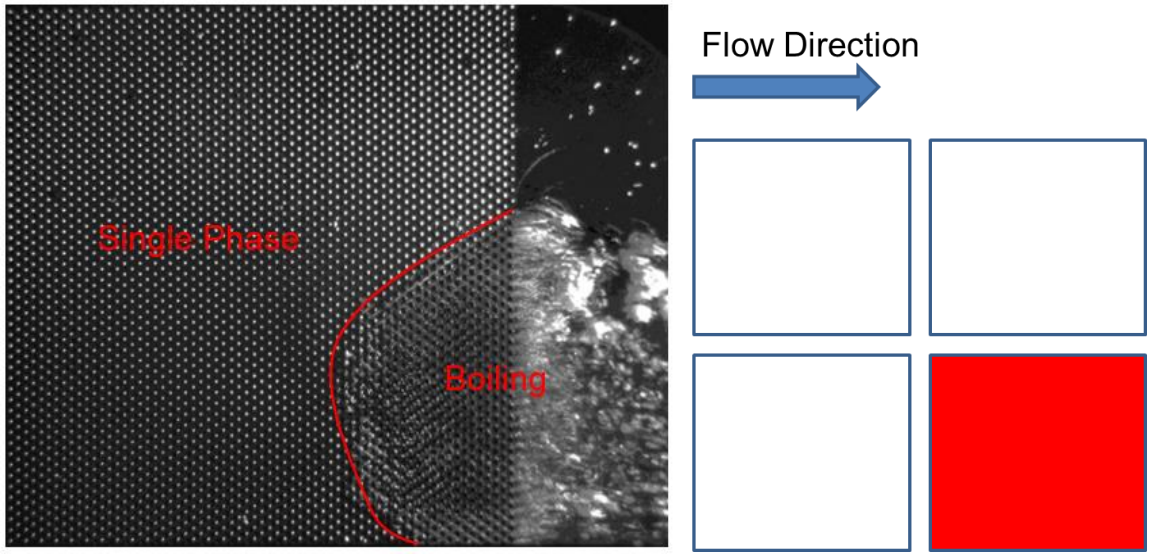


(g)

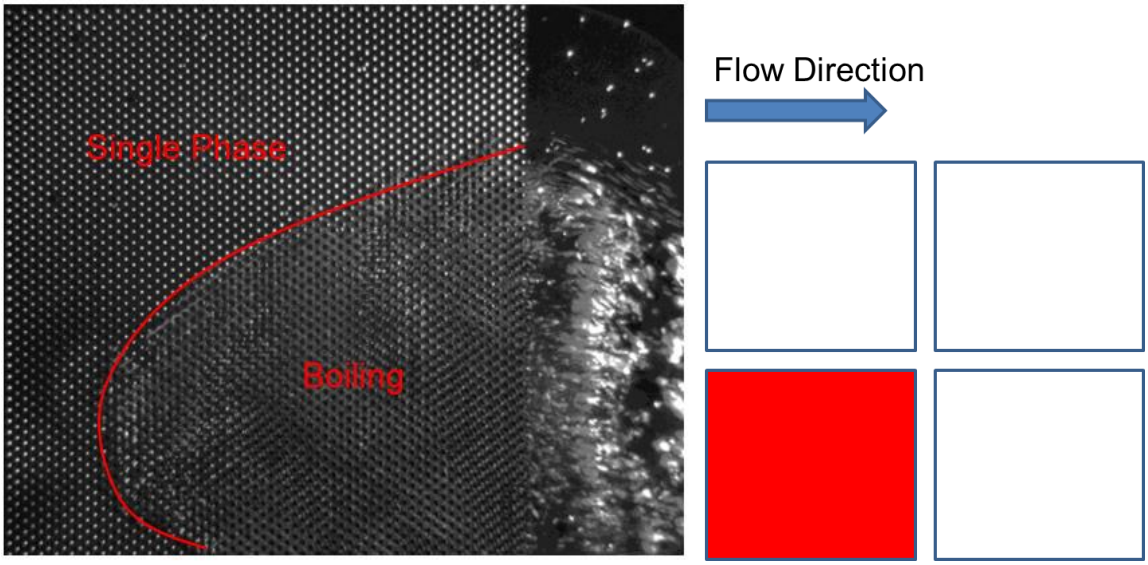


(h)

Figure 6.8 continued.



(i)



(j)

Figure 6.8 continued.

6.4.5 Effect of Mixture of HFE 7200 and Methanol

Although HFE 7200 has large dielectric strength, its thermal conductivity and latent heat are much lower than DI water. In order to enhance the flow boiling, addition of methanol into HFE 7200 was studied. Table 6.1 shows the thermal properties of HFE 7200

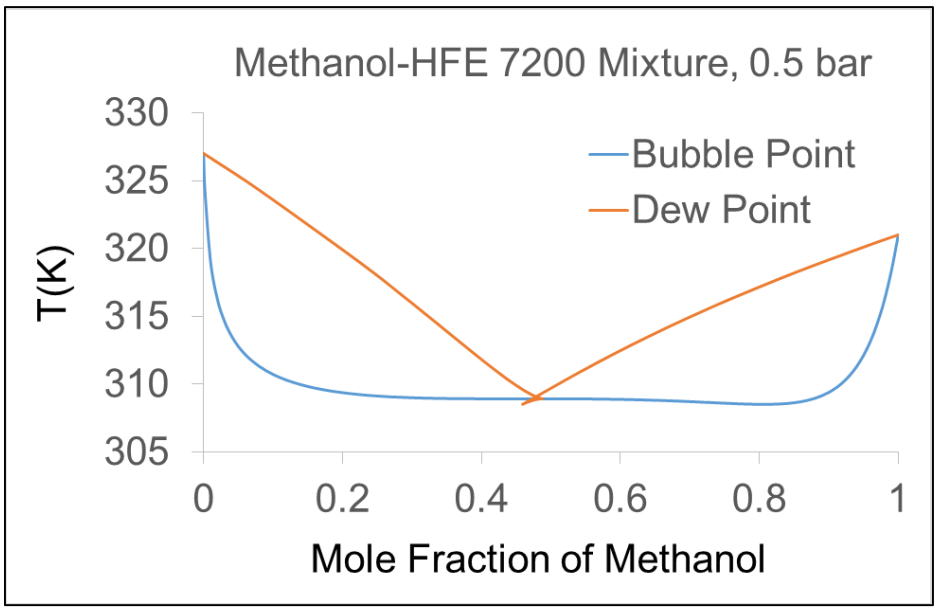
[72] and Methanol [98] at atmosphere pressure and room temperature. It can be seen that the thermal conductivity of Methanol is almost 3 times of that of HFE 7200 and the latent heat of Methanol is almost 10 times of that of HFE 7200.

Table 6.1: Thermal properties of HFE 7200 and Methanol.

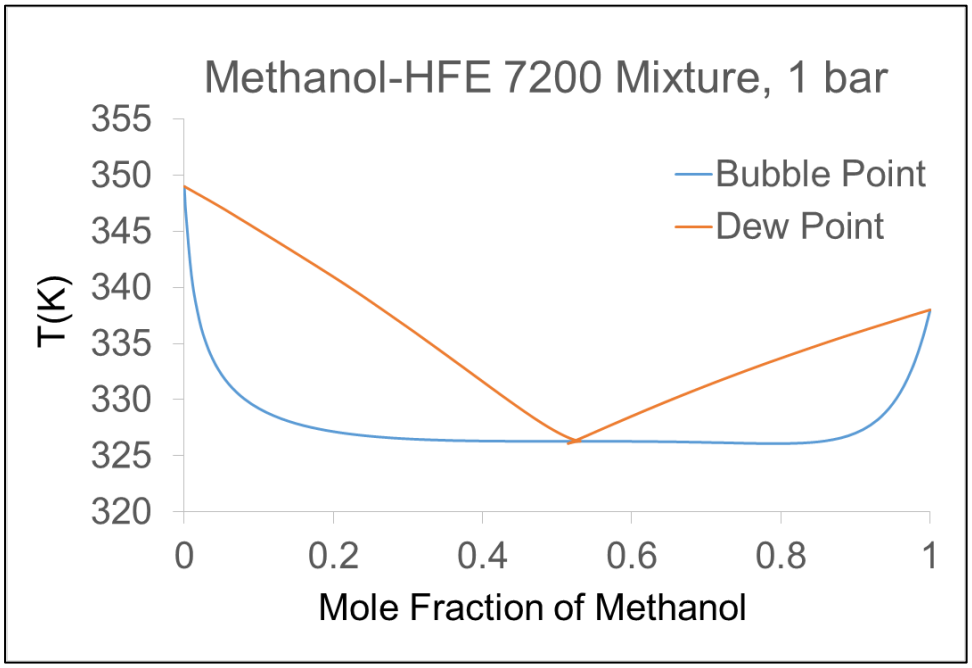
Fluid	T_{sat} (℃)	ρ_l (kg/m^3)	C_p (J/kg-K)	μ (kg/m-s)	k (W/m-K)	h_{fg} (kJ/kg)	σ (N/m)
HFE 7200	76	1420	1220	0.00063	0.069	119	0.0136
Methanol	65	792	2484	0.00055	0.2	1100	0.0218

In the present study, three different mass concentrations of Methanol were investigated: 8.5%, 18.2%, and 35.8%. The corresponding mole fractions of Methanol were 0.43, 0.65, and 0.82. Figure 6.9 shows the vapor-liquid equilibrium diagram of the binary mixture of HFE 7200 and Methanol calculated by COSMO-RS [99]. The dew point is the temperature at which the saturated vapor starts to condense. And the bubble point is the temperature at which the liquid begins to vaporize. It can be seen that the saturation temperature of the mixture is significantly reduced due to the addition of Methanol and is lower than both pure HFE 7200 and Methanol. This means an earlier initiation of boiling for the mixture. This can be explained as follows [100]: for a binary mixture, if the molecular attraction of component A and B in the mixture is much larger than both A-A and B-B, the boiling point of the mixture will be higher than both pure fluids. On the contrary, if the molecular attraction of component A and B in the mixture is much smaller

than both A-A and B-B, the boiling point of the mixture will be lower compared to pure component.

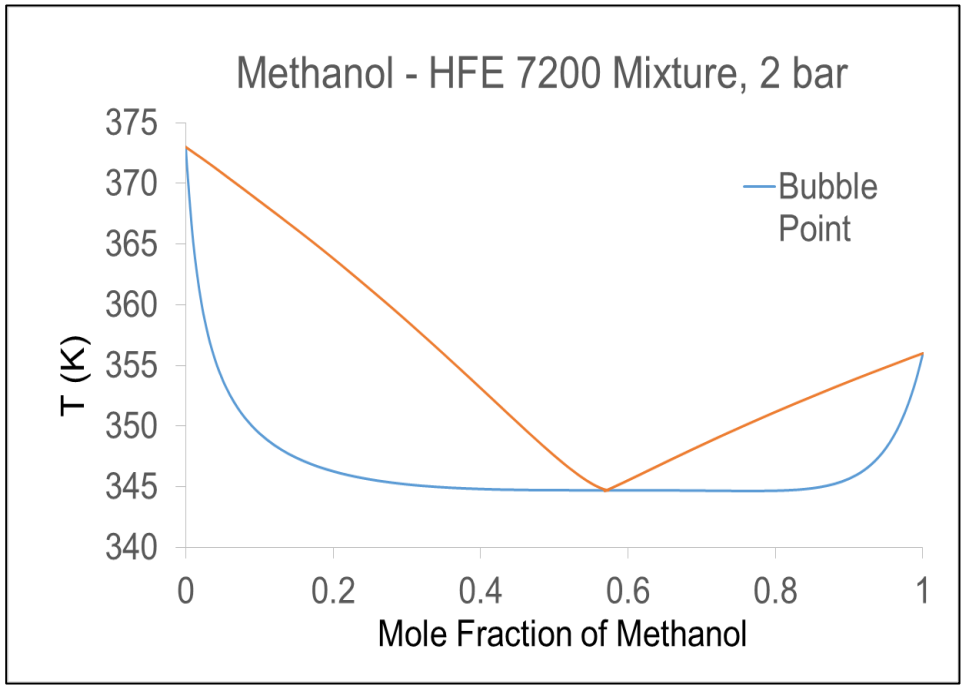


(a)



(b)

Figure 6.9: Vapor liquid equilibrium curves for mixture of HFE 7200 and Methanol at various pressure: (a) 0.5 bar, (b) 1 bar, (c) 2 bar.



(c)

Figure 6.9 continued.

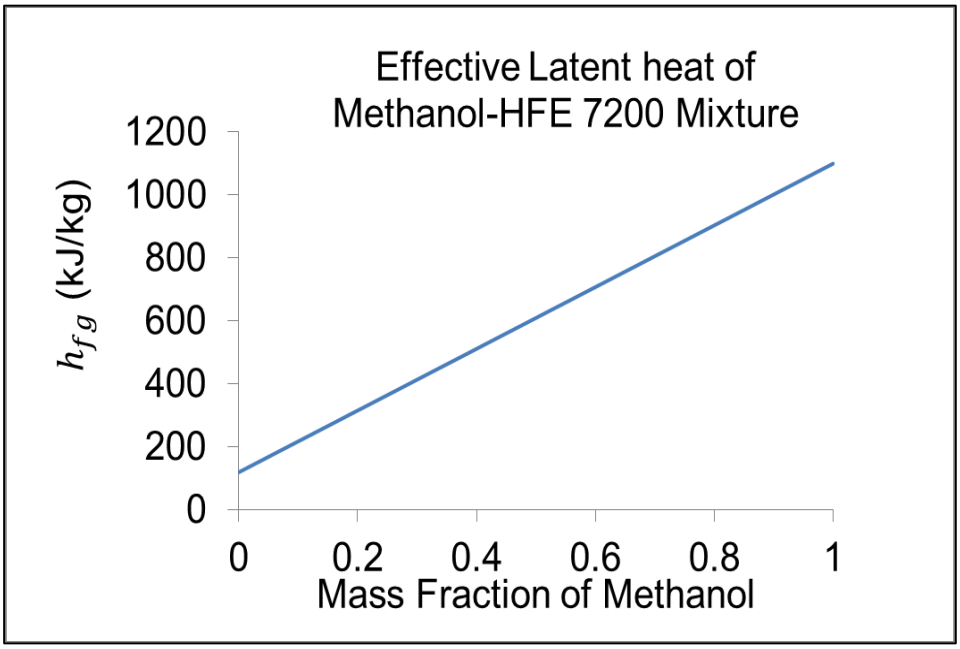


Figure 6.10: Effective latent heat of Methanol-HFE 7200 mixture.

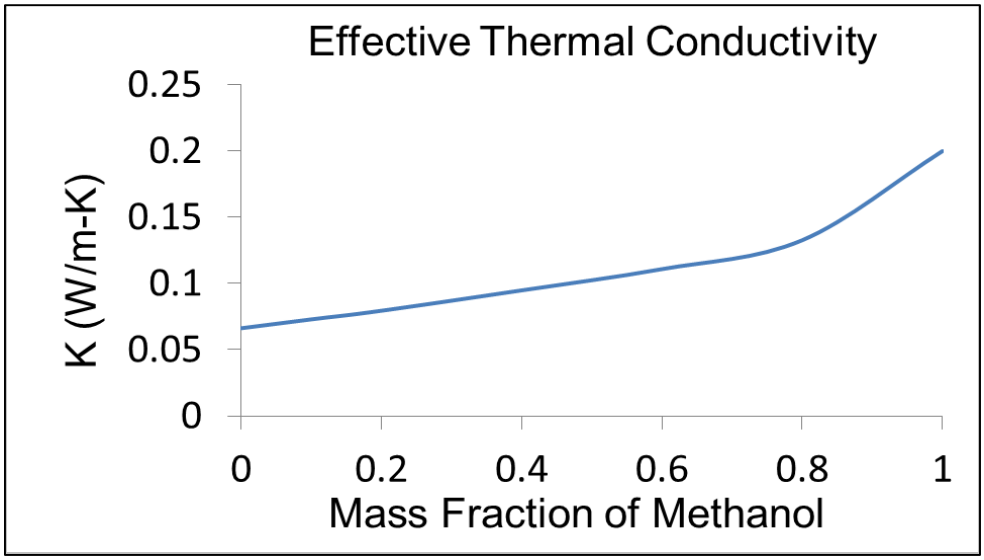


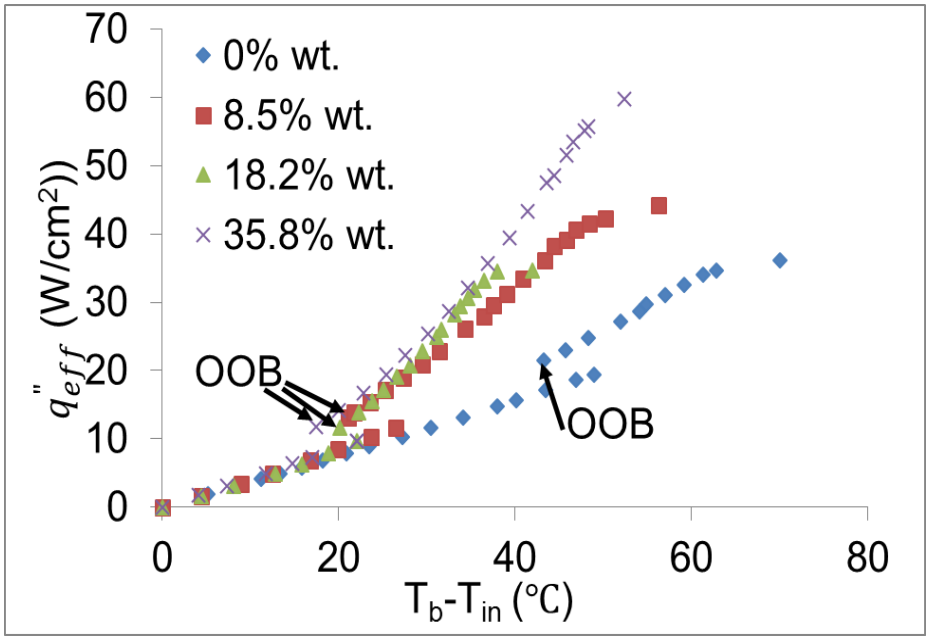
Figure 6.11: Effective thermal conductivity of Methanol-HFE 7200 mixture [101].

Figure 6.10 and Figure 6.11 show the effective latent heat and thermal conductivity of Methanol-HFE 7200 mixture under various mass fractions of Methanol. As the mass fraction of Methanol increases, both the latent heat and thermal conductivity of the mixture increase, indicating better thermal properties.

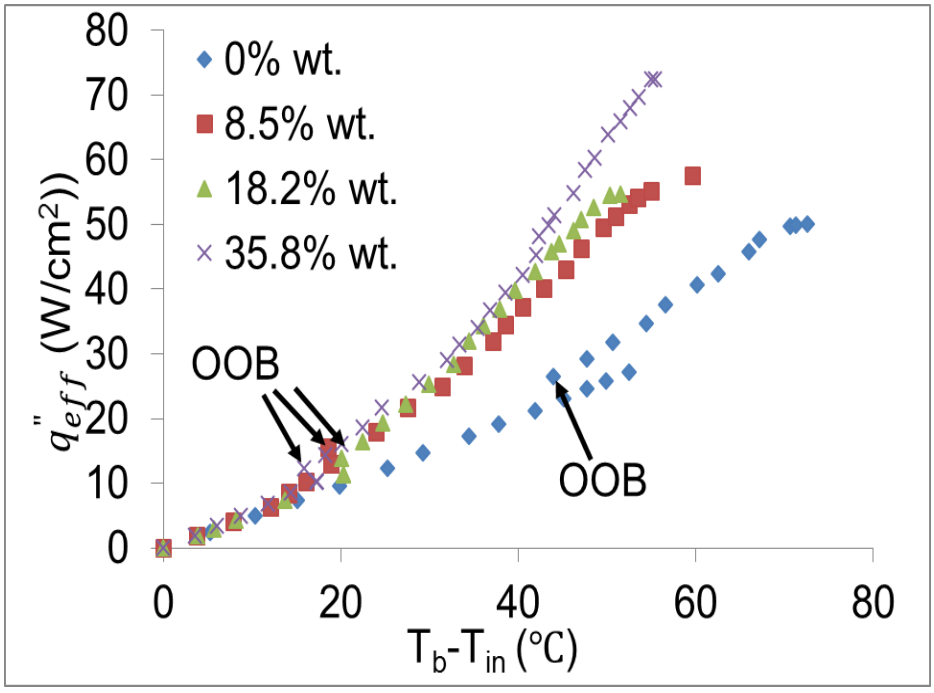
For the mixtures study, the density (ρ) and specific heat (C_p) of HFE 7200 and Methanol are different. To minimize the effect of fluid specific heat in the single phase region, the flow boiling experiments of the mixture were performed at the same volume flow rate as pure HFE 7200, instead of same mass flow rate. Figure 6.12 shows the comparison of flow boiling curves of pure HFE 7200 and Methanol-HFE 7200 mixture. In the single phase region, the boiling curves did not show large difference. However, the addition of Methanol into HFE 7200 significantly changed the boiling characteristics. The boiling curve in the two phase region shifted to the left. The boiling started at a lower temperature. At the same effective heat flux, the base temperature was about 15 ℃ lower for the mixture than that of pure HFE 7200. This was because the saturation temperature

of the mixture was much lower than pure HFE 7200. Also, the latent heat and thermal conductivity of the mixture was higher than pure HFE 7200. All of these factors enhanced the heat transfer performance. Comparison of boiling characteristics in Figure 6.13 shows that the boiling area of the mixture was much larger than the pure HFE 7200 at 8.5% wt. concentration of Methanol at flow rate 20.0 ml/min, q''_{eff} 61.8 W/cm^2. For pure HFE 7200, dryout started to occur downstream the pin fin arrays. The addition of Methanol increased the bubble density and frequency significantly. This was because the saturation temperature of the mixture is lower, and less energy is required for the boiling. It was much easier for the bubbles to departure from the surface. It can be observed in Figure 6.13 that no dryout occurred, and downstream of the pin fin area was completely covered by high density of bubbles. As the Methanol concentration increased from 8.5% wt. to 18.2% wt., the boiling curve continued to shift to the left due to the improved thermal properties of the mixture. However, the CHF was not necessarily increased. In the present study, the mixture of HFE 7200 and Methanol was a negative mixture: more volatile fluid (Methanol) had larger surface tension. As pointed by McGillis and Carey [63], preferential evaporation of one component occurs along the liquid-vapor interface of a binary mixture. The variation in concentration along the liquid – vapor interface resulted in a surface tension gradient (Marangoni effect). If the surface tension of the more volatile component is greater than the surface tension of the less volatile component, a force that breaks up the liquid film could be generated. This has been observed in Figure 6.14. At low methanol concentration (8.5% wt.), the Marangoni effect was not significant. Kandlikar and Alves [66] also showed that the surface tension effect was insignificant at low concentration. As the Methanol concentration increased from 8.5% wt. to 18.2% wt., the Marangoni effect became

important. But if the Methanol concentration continued to increase, the effects of the enhanced thermal properties became dominant, and the CHF was increased.

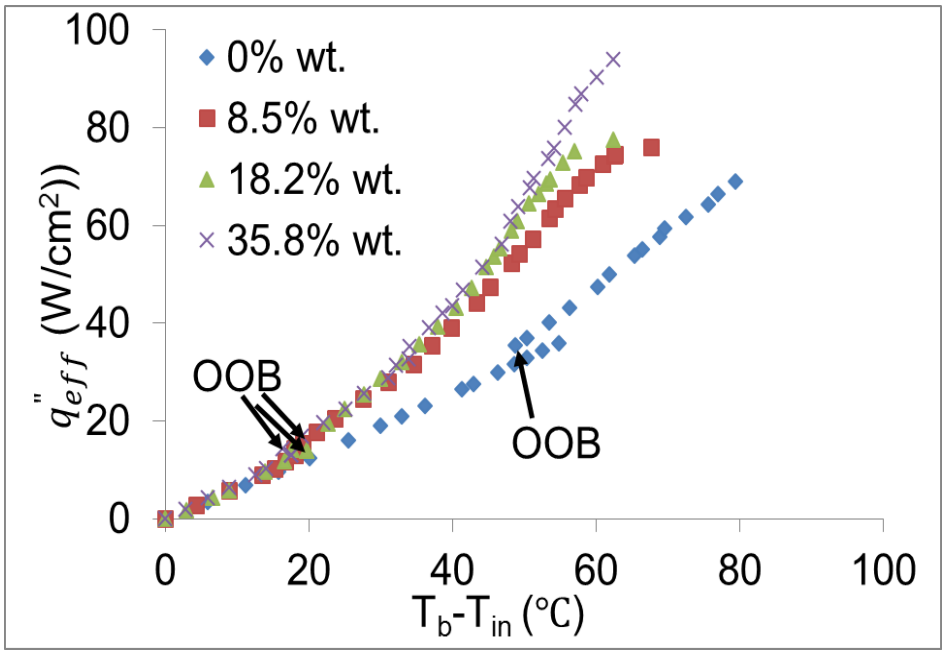


(a)



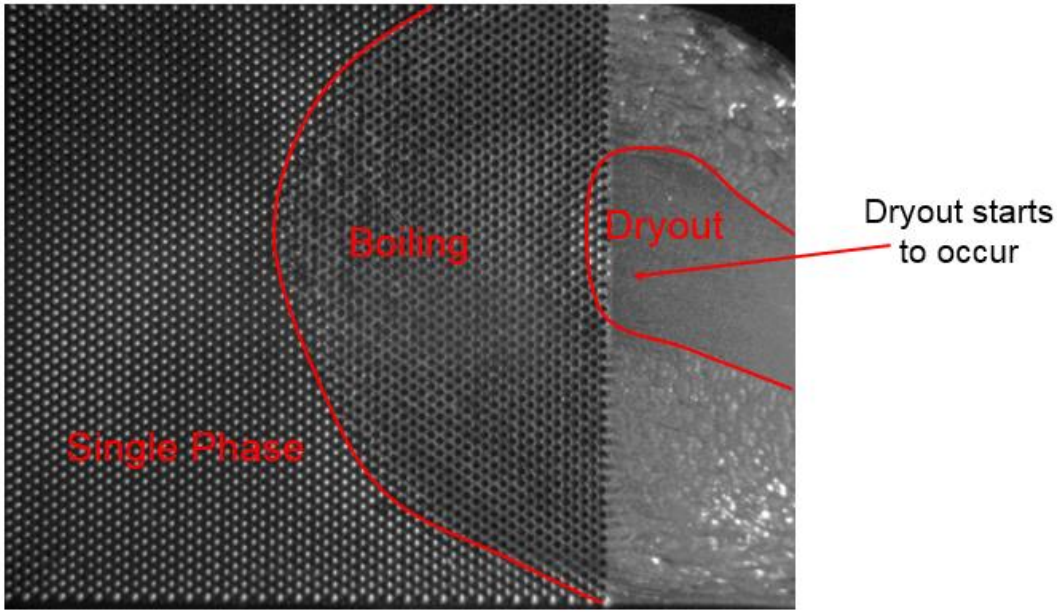
(b)

Figure 6.12: Comparison of flow boiling curves between pure HFE 7200 and Methanol-HFE 7200 mixture at flow rate: (a) 12.3 ml/min, (b) 16.5 ml/min, (c) 20.0 ml/min.



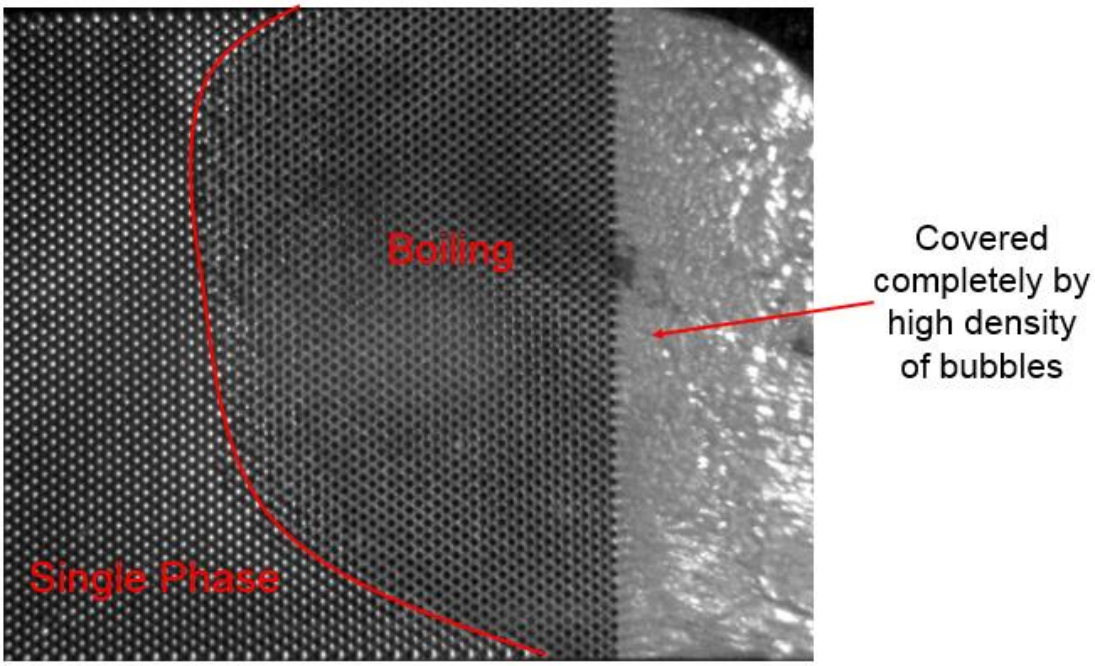
(c)

Figure 6.12 continued.



(a)

Figure 6.13: Comparison of boiling characteristics, flow rate=20.0 ml/min, q''_{eff}=61.8 W/cm^2 (a) Pure HFE 7200, (b) 8.5% wt. concentration of Methanol.



(b)

Figure 6.13 continued.

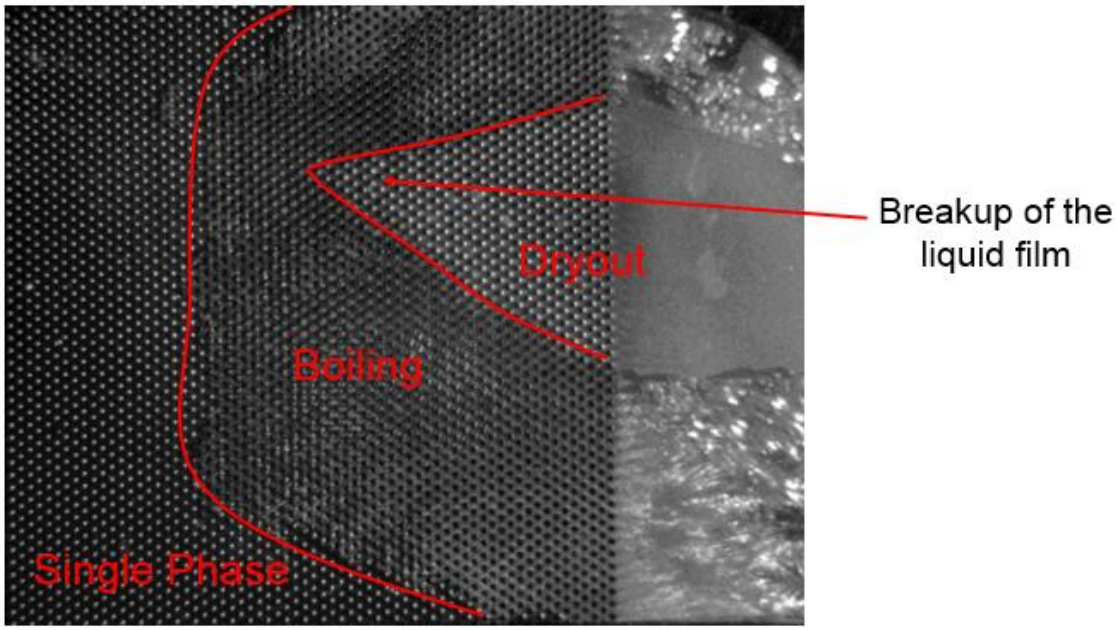


Figure 6.14: Boiling image showing the breakup of the liquid film, flow rate=20.0 ml/min, 18.2% wt. concentration of Methanol.

6.5 Summary

In this chapter, flow boiling experiments with HFE 7200 and mixture of HFE 7200 and Methanol are reported. The effects of mass flux, dissolved gas, gap size, and non uniform power pattern were studied. Heat transfer enhancement by addition of Methanol into HFE 7200 was investigated. Mechanisms of heat transfer enhancement were identified via high speed visualization of the flow boiling. The main observations are:

(1) The dissolved gas initiated the boiling earlier. However, once boiling started, the boiling curves converged.

(2) CHF increased as mass flux increased.

(3) CHF decreased as gap size decreased. Smaller gap constrained the expansion of bubble.

(4) Nonuniform power map presented new challenges to two phase cooling in terms of non-uniform boiling patterns. The mass flux was reduced at the high heat flux area.

(5) Addition of Methanol into HFE 7200 significantly increased the heat transfer performance by reducing the saturation temperature, increasing effective latent heat and thermal conductivity. However, Marangoni effect caused by the preferential boiling of Methanol had a negative effect on CHF.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

7.1 Conclusions

This dissertation explores the transport characteristics of pin fin enhanced microgap, which contributes to the design and applications of direct microfluidic cooling for future high power microelectronics.

Pin fin enhanced microgap, as a promising technology, can handle very high heat flux compared to air cooled heat sink. Understanding of its characteristics is essential for its successful applications. Both numerical and experimental methods are used for the characteristics study. For single phase flow, a numerical model is used to conduct parametric study. Pin spacing affects both the pressure drop and heat transfer coefficient. As the pins move closer to each other, the flow mixing is increased. However, the flow resistance is also increased. So under the same flowrate, the denser pin array has higher heat transfer coefficient and larger heat transfer area but also the higher pressure drop. The pumping power is usually low (<1 W) and will not be an issue to consider for pin array design. However, the absolute pressure needs to be considered from a practical view. The pressure drop increases non-linearly with mass flowrate. The high operating pressure presents challenges to the device reliability. The pin geometry affects the fluid flow around the pins and therefore affects its pressure drop and heat transfer performance. The pins with sharp edges, such as the square pin, diamond pin, and triangular pin, can enhance the flow separation and mixing, which can increase heat transfer coefficient. However, the increase of heat transfer is usually accompanied by increased pressure drop.

Pin fin enhanced microgap can be adapted to inter-tier microfluidic cooling of 3D stacked ICs. The pins can provide routing for embedded copper based TSVs, which serve as electrical interconnections between tiers. The results of the present study demonstrate that microfluidic cooling can handle heat flux as high as 300 W/cm^2, which is far beyond the capability of air cooling without exceeding the size. The benefits of microfluidic cooling are evident. With microfluidic cooling, the processor can be kept at lower temperature and runs at high frequency. For large data centers, significant amounts of energy can be saved due to the leakage power reduction. Due to the high efficiency and heat removal capability of microfluidic cooling, the cooling system can be more compact compared to air cooling. However, before microfluidic cooling can be used widely, cost and reliability issues need to be considered and addressed. Microfluidic cooling system is usually more complicated and requires a flow loop consisting of pump, heat exchanger, filter, and reservoir. Liquid leakage and clogging need to be addressed. Also it requires that the microgap can stand high pressure. Incorporating microgap cooling into processor can increase the cost of fabrication. It may require some modification of the existing fabrication procedures. This is another obstacle for the applications of on chip microfluidic cooling.

Compared to single phase cooling, flow boiling in pin fin enhanced microgap can achieve even higher heat transfer performance, which can be further enhanced using a fluid mixture. However, the new challenges come from flow instability with the flow boiling, and non-uniform flow due to the non-uniform heating. The vapor can increase the pressure significantly. To condense the vapor back into liquid, a chiller is required.

In general, the selection between air cooling and microfluidic cooling depends on the application, cost, and reliability. For low power devices, convection air cooling can be

used. For high power devices, especially some military devices where high performance is required, microfluidic cooling may be the only option.

7.2 Recommendations for Future Work

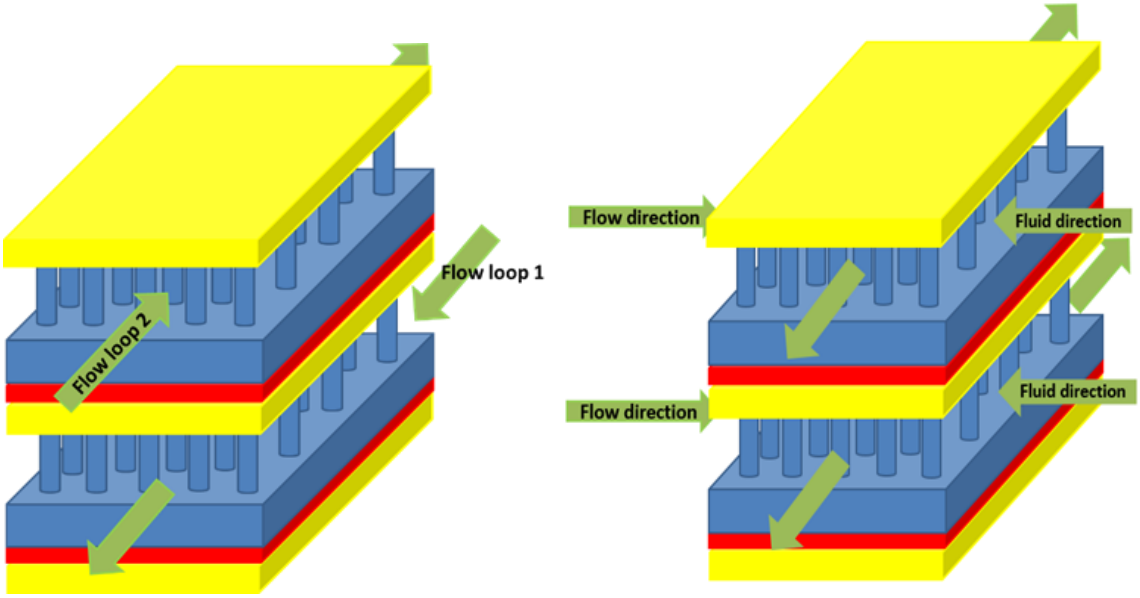
This work has demonstrated the superior thermal performance of microfluidic cooling with surface enhanced structure and its benefits for 3D ICs cooling. To further enhance the performance, the following are recommended:

(1) Explore more complicated structures to enhance the heat transfer coefficients. Numerical modelling will be a useful tool for this study. The problem of single phase cooling is the chip temperature nonuniformity due to the bulk fluid temperature rise. To mitigate this issue, nonuniform pin density can be explored with higher pin density at high heat flux area.

(2) Velocity fluctuations were observed by numerical modelling at high Re. MicroPIV system can be employed to visualize the fluctuations.

(3) In order to further explore the benefit of inter-tier microfluidic cooling, different fluid delivery methods can be studied. In the present work, the two microgaps of the two tiers share the same inlet and outlet. Only one flow loop is needed. We can also use two flow loops separately for each microgap. This allows us to individually control the fluid flow of each microgap (Figure 7.1 (a)). So more pumping power could be applied for the tier with high power dissipation and less power for the tier with low power dissipation. The flow directions for each tier could be different. So the hotspot in tier 1 is close to the inlet of the pin fin channel in tier 1. The bulk fluid temperature rise affects the temperature on the two

active layers. So another fluid delivery method is to inject the fluid into the middle of the microgaps and then spread to the two ends (Figure 7.1(b)). The flow paths could be reduced to half of the previous study. So the bulk fluid temperature is expected to be reduced.



(a) (b)

Figure 7.1: Schematic of fluid delivery methods: (a) Double flow loops (b) Middle injection flow.

(4) Flow boiling exhibits higher thermal performance than single phase cooling. However, it presents new challenge due to the instability caused by the nonuniform heating. Dynamic control of the system can be used to minimize the effect of the instability. In the present work, only mixture of Methanol and HFE 7200 has been explored. New fluid mixtures with combinations of different fluids can also be studied.

REFERENCES

[1] S. Kolluri, S. Keller, S. P. Denbaars, and U. K. Mishra, "N-Polar GaN MIS-HEMTs with a 12.1-W/mm continuous wave output power density at 4 GHz on sapphire substrate," *IEEE Electron Device Letters*, vol. 32(5), pp. 635-637, 2011.

[2] Y. I. Salamin, S. X. Hu, K. Z. Hatsagortsyan, and C. H. Keitel, "Relativistic high-power laser-matter interactions," *Physics Reports*, vol. 427(2-3), pp. 41-155, 2006.

[3] G. E. Moore, "Cramming more components onto integrated circuits," *Proceedings of the IEEE*, vol. 86(1), pp. 82-85, 1998.

[4] C. A. Mack, "Fifty years of Moore's Law," *IEEE Transactions on Semiconductor Manufacturing*, vol. 24(2), pp. 202-207, 2011.

[5] Moore's Law: Fun Facts. Available: http://www.intel.com/content/www/us/en/history/history-moores-law-fun-facts-factsheet.html.

[6] Intel Chips Timeline. Available: http://www.intel.com/content/www/us/en/history/history-intel-chips-timeline-poster.html.

[7] International Technology Roadmap for Semiconductors, 2012 update. Available: http://public.itrs.net/Links/2012ITRS/Home2012.html.

[8] R. R. Tummala, and M. Swaminathan, *Introduction to System-on-Package (SOP*), McGraw-Hill, pp. 3-34, 2008.

[9] A. A. Chien, V. Karamcheti, "Moore's Law: The first ending and a new beginning," *Computer*, vol. 46(12), pp. 48-53, 2013.

[10] M. Schulz, "The end of road for silicon," *Nature*, vol. 399, pp. 729-730, 1999.

[11] J. D. Meindl, "Beyond Moore's Law: the interconnect era," *Computing in Science & Engineering*, vol. 5(1), pp. 20-24, 2003.

[12] N. H. Khan, S. M. Alam, and S. Hassoun, "System-level comparison of power delivery design for 2D and 3D ICs," *IEEE International Conference on 3D System Integration*, pp. 1-7, 2009.

[13] M. Bamal, S. List, M. Stucchi, A. S. Verhulst, M. V. Hove, R. Cartuyvels, G. Beyer, and K. Maex, "Performance comparison of interconnect technology and architecture options for deep submicron technology nodes," *International Interconnect Technology Conference*, pp. 202-204, 2006.

[14] G. Kumar, T. Bandyopadhyay, V. Sukumaran, V. Sundaram, S. K. Lim, R. Rummala, "Ultra-high I/O density glass/silicon interposers for high bandwidth smart mobile applications," *IEEE 61st Electronic Components and Technology Conference*, pp. 217-223, 2011.

[15] S. M. Sri-Jayantha, G. McVicker, K. Bernstein, J. U. Knickerbocker, "Thermomechanical modeling of 3D electronic packages," *IBM Journal of Research and Development*, 52(6), pp. 623-634, 2008.

[16] 2006 International Electronics Manufacturing Initiative Roadmap. Available: http://www.inemi.org/.

[17] M. S. Bakir, J. D. Meindl, *Integrated Interconnect Technologies for 3D Nanoelectronic Systems*, Artech House, 2008.

[18] K. Banerjee, A. Amerasekera, G. Dixit, and C. Hu, "The effect of interconnect scaling and low-k dielectric on the thermal characteristics of the IC metal," *International Electron Devices Meeting*, pp. 65–68, 1996.

[19] H. C. Chien, J. H. Lau, Y. L. Chao, M. J. Dai, R. M. Tain, L. Li, P. Su, J. Xue, M. Brillhart, "Thermal evaluation and analyses of 3D IC integration SiP with TSVs for network system applications," *IEEE 62nd Electronic Components and Technology Conference*, pp. 1866-1873, 2012.

[20] F. Li, C. Nicopoulos, T. Richardson, Y. Xie, V. Narayanan, M. Kandemir, "Design and management of 3D chip multiprocessors using network-in-memory," *33rd International Symposium on Computer Architecture*, pp.130–141, 2006.

[21] W. R. Davis, J. Wilson, S. Mick, J. Xu, H. Hua, C. Mineo, A. M. Sule, M. Steer, and P. D., Franzon, "Demistifying 3D ICs: the pros and cons of going vertical," *IEEE Design & Test of Computers*, vol. 22(6), pp. 498-510, 2005.

[22] Z. Wan, W. Yueh, Y. Joshi, S. Mukhopadhyay, "Enhancement in CMOS chip performance through microfluidic cooling," *2014 20th International Workshop on Thermal Investigations of ICs and Systems (THERMINIC),* pp. 1-5. 2014.

[23] D. B. Tuckerman and R. F. W. Pease, "High performance heat sinking for VLSI," *IEEE Electron Device Letters*, vol. 2(5), pp. 126-129, 1981.

[24] W. Qu, I. Mudawar, "Experimental and numerical study of pressure drop and heat transfer in a single-phase micro-channel heat sink," *International Journal of Heat and Mass Transfer*," vol. 45, pp. 2549-2565.

[25] V. K. Samalam, "Convective heat transfer in microchannels," *Journal of Electronic Materials*, vol. 18(5), pp. 611-617, 1989.

[26] T. M. Harms, M. J. Kazmierczak, F. M. Gerner, "Developing convective heat transfer in deep rectangular microchannels," *International Journal of Heat and Fluid Flow*, vol. 20(2), pp. 149-157, 1999.

[27] M. M. Rahman, "Measurements of heat transfer in microchannel heat sinks," *International Communications in Heat and Mass Transfer*, vol. 27(4), pp. 495-506, 2000.

[28] T. B. Ochende, L. Liebenberg, J. P. Meyer, "Constructual cooling channels for micro-channel heat sinks," *International Journal of Heat and Mass Transfer*, vol. 50(21-22), pp. 4141-4150, 2007.

[29] P. Naphon, O. Khonseur, "Study on the convective heat transfer and pressure drop in the microchannel heat sink," *International Communications in Heat and Mass Transfer*, vol. 36(1), pp. 39-44, 2008.

[30] M. E. Steinke and S. G. Kandlikar, "Review of single-phase heat transfer enhancement techniques for application in microchannels, minichannels and microdevices," *Heat and Technology*, vol. 22(2), pp. 3-11, 2004.

[31] Y. Peles, A. Kosar, C. Mishra, C. J. Kuo, and B. Schneider, " Forced convective heat transfer across a pin fin micro heat sink," *International Journal of Heat and Mass Transfer*, vol. 48, pp. 3615-3627, 2005.

[32] B. A. Jasperson, Y. Jeon, K. T. Turner, F. E. Pfefferkorn, and W. Qu, "Comparison of micro-pin-fin and microchannel heat sinks considering thermal-hydraulic performance and manufacturability," *IEEE Transaction on Components and Packaging Technologies,* vol. 33(1), pp. 148-160, 2010.

[33] A. Kosar, C. Mishra, Y. Peles, "Laminar flow across a bank of low aspect ratio micro pin fins," *Journal of Fluid Engineering*, vol. 127, pp. 419-430, 2005.

[34] T. Brunschwiler, B. Michel, H. Rothuizen, U. Kloter, B. Wunderle, H. Oppermann, and H. Reichl, "Interlayer cooling potential in vertically integrated packages," *Microsystem Technologies*, vol. 15(1), pp. 57-74, 2009.

[35] A. Kosar, Y. Peles, "TCPT-2006-096.R2: micro scale pin fin heat sinks-parametric performance evaluation study," *IEEE Transaction on Components and Packaging Technologies*, vol. 30(4) pp. 855-865, 2007.

[36] R. S. Prasher, J. Dirner, J. Y. Chang, A. Myers, D. Chau, D. He, S. Prstic, "Nusselt number and friction factor of staggered arrays of low aspect ratio micropin-fins under cross flow for water as Fluid," *Journal of Heat Transfer*, vol. 129, pp. 141-153, 2007.

[37] B. E. Short Jr., P. E. Raad, D. C. Price, "Performance of pin fin cast aluminum coldwalls, part I: friction factor correlations," *Journal of Thermo-Physic Heat Transfer*, vol 16(3), pp. 389-396, 2002.

[38] J. F. Tullius, T. K. Tullius, Y. Bayazitoglu, "Optimization of short micro pin fins in minichannels," *International Journal of Heat and Mass Transfer*, vol. 55, pp. 3921-3932, 2012.

[39] B. E. Short Jr., P. E. Raad, D. C. Price, "Performance of pin fin cast aluminum coldwalls, part II: colburn j factor correlations," *Journal of Thermo-Physic Heat Transfer*, vol 16(3), pp. 397-403, 2002.

[40] A. Kosar, Y. Peles, "Thermal-hydraulic performance of MEMS-based pin fin heat sink," *Journal of Heat Transfer*, vol.128, pp. 121-131, 2006.

[41] A. Kosar, Y. Peles, "Convective flow of refrigerant (R-123) across a bank of micro pin fins," *International Journal of Heat and Mass Transfer*, vol. 49, pp. 3142-3155, 2006.

[42] A. Kosar, B. Schneider, Y. Peles, "Hydrodynamic characteristics of crossflow over MEMS-based pillars," *Journal of Fluids Engineering*, vol. 133, pp. 081201-1 – 081201-11, 2011.

[43] M. Koz, M. R. Ozdemir, A. Kosar, "Parametric study on the effect of end walls on heat transfer and fluid flow across a micro pin-fin," *International Journal of Thermal Science*, vol. 50(6), pp. 1073-1084, 2011.

[44] E. M. Sparrow, J. W. Ramsey, and C. A. Altemani, "Experiment on in-line pin fin arrays and performance comparisons with staggered arrays," *Journal of Heat Transfer*, vol. 102, pp. 44-50, 1980.

[45] A. Rozati, D. K. Tafti, N. E. Blackwell, "Effect of pin tip clearance on flow and heat transfer at low Reynolds numbers," *Journal of Heat Transfer*, vol. 130, pp. 071704, 2008.

[46] K. Moores, J. Kim, Y. Joshi, "Heat transfer and fluid flow in shrouded pin fin arrays with and without tip clearance," *International Journal of Heat and Mass Transfer*, vol. 52(25-26), pp. 5978-5989, 2009.

[47] K. A. Moores and Y. Joshi, "Effect of tip clearance on the thermal and hydrodynamic performance of a shrouded pin fin array," *Journal of Heat Transfer*, vol. 125, pp. 999-1006, 2003.

[48] A. Siu-Ho, W. Qu, F. Pfefferkorn, "Experimental study of pressure drop and heat transfer in a single-phase micropin-fin heat sink," *Journal of Electronic Packaging*, vol. 129, pp. 479-487, 2007.

[49] M. Liu, D. Liu, S. Xu, Y. Chen, "Experimental study on liquid flow and heat transfer in micro square pin fin heat sink," *International Journal of Heat and Mass Transfer*, vol. 54, pp. 5602-5611, 2011.

[50] J. R. Mita, W. Qu, M. H. Kobayashi, F. E. Pfefferkorn, "Experimental Study and Numerical Analysis of Water Single-Phase Pressure Drop Across an Array of Circular Micro-Pin-Fins," *ASME/JSME 2011 8th Thermal Engineering Joint Conference*, pp. T10131-T10131-9, 2011.

[51] C. A. Konishi, W. Qu, and F. E. Pfefferkorn, "Experimental study of water liquid-vapor two-phase pressure drop across an array of staggered micropin fins," *Journal of Electronic Packaging*, vol. 131, pp. 021010-1-021010-8, 2009.

[52] W. Qu and A. Siu-Ho, "Liquid single phase flow in an array of micro pin fins: part I: heat transfer characteristics," *Journal of Heat Transfer*, vol. 130, 122402-1-122402-11, 2008.

[53] W. Qu and A. Siu-Ho, "Liquid single phase flow in an array of micro pin fins part II: pressure drop characteristics," *Journal of Heat Transfer*, vol. 130, 124501-1124501-4, 2008.

[54] C. A. Konish, R. Hwu, W. Qu, F. E. Pfefferkorn, "Experimental study and numerical analysis of water single-phase pressure drop across a micro pin fin array," *Proceedings of the 14th International Heat Transfer Conference*, pp. 711-719, 2010.

[55] W. Qu, A. Siu-Ho, "Experimental study of saturated flow boiling heat transfer in an array of staggered micro-pin-fins," *International Journal of Heat and Mass Transfer*, vol. 52, pp. 1853-1863, 2009.

[56] S. Krishnamurthy and Y. Peles, "Flow boiling of water in a circular staggered micro-pin fin heat sink," *International Journal of Heat and Mass Transfer*, vol. 51, pp. 1349-1364, 2008.

[57] S. Isaacs, Y. Kim, A. Mcnamara, Y. Joshi, Y. Zhang, M. Bakir, "Two phase flow and heat transfer in pin fin enhanced micro gaps," *13th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronics Systems (ITherm*), pp. 1084-1089, 2012.

[58] S. Isaacs, Y. Joshi, Y. Zhang, M. Bakir, Y. Kim, "Two phase flow and heat transfer in pin fin enhanced micro gaps with non-uniform heating," *4th International Conference on Micro/Nanoscale Heat and Mass Transfer*, pp. V001T12A003, 2013.

[59] A. Reeser, A. Bar-Cohen, G. Hetsroni, "High vapor quality two phase heat transfer in staggered and inline micro pin fin arrays," *14th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronics Systems (ITherm)*, pp. 213-22, 2014.

[60] D. A. Mcneil, A. H. Raeisi, P. A. Kew and P. R. Bobbili, "A comparison of flow boiling heat transfer in in-line mini pin fin and plane channel flows," *Applied Thermal Engineering*, vol. 30(16), pp. 2412-2425, 2010.

[61] A. Ma, J. Wei, M. Yuan, and J. Fang, "Enhanced flow boiling heat transfer of FC-72 on micro-pin-finned surfaces," *International Journal of Heat and Mass Transfer*, vol. 52, pp. 2925-2931, 2009.

[62] W. R. Van Wijk, A. S. Vos, and S. J. D. Van Strallen, "Heat transfer to boiling binary liquid mixtures," *Chemical Engineering Science*, vol.5, pp. 68-80, 1956.

[63] W. R. McGillis and V. P. Carey, "On the role of Marangoni effects on the critical heat flux for pool boiling of binary mixtures," *Journal of heat transfer*, vol. 118, pp. 103-109, 1996.

[64] J. Hovestreijdt, "The influence of the surface tension difference on the boiling of mixtures," *Chemical Engineering Science*, vol.18, pp. 631-639, 1963.

[65] Y. Fujita and Q. Bai, "Critical heat flux of binary mixtures in pool boiling and its correlation in terms of Marangoni number," *International Journal of Refrigeration*, vol. 20, pp. 616-622, 1997.

[66] S. G. Kandlikar and L. Alves, "Effects of surface tension and binary diffusion on pool boiling of dilute solutions: An experimental assessment," *Journal of Heat Transfer*, vol. 121, pp. 488-493, 1999.

[67] M. Arik and A. Bar-Cohen, "Pool boiling of perfluorocarbon mixtures on silicon surfaces," *International Journal of Heat and Mass Transfer*, vol. 53, pp. 5596-5604, 2010.

[68] X. F. Peng, G. P. Peterson, and B. X. Wang, "Flow boiling of binary mixtures in microchannel plates," *International Journal of Heat and Mass Transfer*, vol. 39, pp. 1257 – 1264, 1996.

[69] P. H. Lin, B. R. Fu, and C. Pan, "Critical heat flux on flow boiling of methanol – water mixtures in a diverging microchannel with artificial cavities," *International Journal of Heat and Mass Transfer*, vol. 54, pp. 3156-3166, 2011.

[70] D. L. Bennett and J. C. Chen, "Forced convective boiling in vertical tubes for saturated pure components and binary mixtures," *AIChE Journal*, vol. 26, pp. 454-461, 1980.

[71] S. G. Kandlikar and M. Bulut, "An experimental Investigation on flow boiling of ethylene-glycol/water mixtures," *Journal of Heat Transfer*, vol. 125, pp. 317-325, 2003.

[72] A. Sathyanarayana, "Pool and flow boiling of novel heat transfer fluids from nanostructured surfaces," PhD Dissertation, Mechanical Engineering, Georgia Institute of Technology, Atlanta, 2013.

[73] A. Dembla, Y. Zhang, and M. S. Bakir, "Fine pitch TSV integration in silicon micropin-fin heat sinks for 3D ICs," *Proceedings of 2012 IEEE International Interconnect Technology Conference*, pp. 1-3, 2012.

[74] C. R. King, D. Sekar, M. S. Bakir, B. Dang, J. Pikarsky, J. D. Meindl, "3D Stacking of chips with electrical and microfluidic I/O interconnects," *Proceedings of 58th Electronic Components and Technology Conference*, pp. 1-7, 2008.

[75] H. Mizunuma, C. L. Yang, Y. C. Lu, "Thermal management of 3D-ICs with Integrated microchannel cooling," *Proceedings of the 2009 International Conference on Computer-Aided Design*, pp. 256-263, 2009.

[76] A. Sridhar, A. Vincenzi, M. Ruggiero, T. Brunschwiler, D. Atienza, "3D-ICE: fast compact transient thermal modeling for 3D ICs with inter-tier liquid cooling," *Proceedings of the 2010 International Conference on Computer-Aided Design*, pp. 463-470, 2010.

[77] A. Sridhar, A. Vincenzi, M. Ruggiero, T. Brunschwiler, D. Atienza, "Compact transient thermal model for 3D ICs with liquid cooling via enhanced heat transfer cavity," *Proceedings of 2010 16th International Workshop on Thermal Investigations of ICs and Systems*, pp. 1-6, 2010.

[78] J. M. Koo, S. J. Im, L. Jiang, K. E. Goodson, "Integrated microchannel cooling for three-dimensional electronic circuit architectures," *Journal of Heat Transfer*, 127(1), pp. 49-58, 2005.

[79] Y. J. Kim, Y. J. Lee, S. K. Lim, Y. K. Joshi, A. G. Fedorov, "Thermal characterization of interlayer microfluidic cooling of three-dimensional integrated circuits with nonuniform heat flux," *Journal of Heat Transfer*, 132(4), pp. 041009-1-041009-9, 2010.

[80] W. Qu, I. Mudawar, "Measurement and prediction of pressure drop in two-phase microchannel heat sinks," *International Journal of Heat and Mass Transfer*, vol. 46, pp. 2737-2753, 2003.

[81] www.omega.com.

[82] S. J. Kline and F. A. McClintock, "Describing uncertainties in single-sample experiments," *Mechanical Engineering*, p.3, 1953.

[83] H. R. Seyf, M. Layeghi, "Numerical analysis of convective heat transfer from an elliptic pin fin heat sink with and without metal foam insert," *Journal of Heat Transfer*, vol. 132, pp. 12-21, 2010.

[84] T. L. Bergman, F. P. Incropera, A. S. Lavine, D. P. Dewitt, *Fundamentals of Heat and Mass Transfer*, John Wiley & Sons, 2011.

[85] www.ansys.com.

[86] J. R. Mita, W. L. Qu, F. E. Pfefferkkorn, "Numerical study of the endwall effects on water single-phase pressure drop across a circular micro-pin-fin array," *ASME 2011 International Mechanical Engineering Congress and Exposition*, pp. 251-255, pp. 2011.

[87] Y. Zhang, A. Dembla, S. Bakir, "Silicon micropin-fin heat sink with integrated TSVs for 3-D ICs: Tradeoff analysis and experimental testing," *IEEE Transactions on Components, Packaging and Manufacturing*, vol. 3(11), pp. 1842-1850, 2013.

[88] S. V. Patankar, *Numerical heat transfer and fluid flow*, McGraw-Hill, New York, 1980.

[89] S. Li, H. H. Ahn, R. D. Strong, J. B. Brockman, D. M. Tullsen, N. P. Jouppi, "McPAT: an integrated power, area, and timing modeling framework for multicore and manycore architectures", *42nd Annual IEEE/ACM International Symposium on Microarchitecture, MICRO-42*, New York, NY, USA, pp. 469-480, 2009.

[90] A. Chandrakasan, W. J. Bowhill, and F. Fox, *Design of High-Performance Microprocessor Circuits*, Wiley-IEEE Press, 2011.

[91] International Technology Roadmap for Semiconductors. International SEMATECH, Austin, TX, 2011. [Online]. Available: http://public.itrs.net/.

[92] W. Yueh, Z. A. Khondker, S. Mukhopadhyay, "Field programmable thermal emulator (FPTE): an all-silicon test structure for thermal characterization of integrated circuits," *Proceedings of 30th Semiconductor Thermal Measurement and Management Symposium(SEMI-THERM*), pp. 66-71, 2014.

[93] D. Sekar, C. King, B. Dang, T. Spencer, H. Thacker, P. Joseph, M. Bakir, J. Meindl, "A 3D-IC technology with integrated microchannel cooling," *Proceedings of 2008 International Interconnect Technology Conference*, pp. 13-15, 2008.

[94] http://www.dowcorning.com.

[95] W. M., Rohsenow, J. P. Hartnett, and E. N. Ganic, *Boiling, handbook of heat transfer fundamentals*, McGraw-Hill, p.12, Chapter. 12, 1985.

[96] Y. Katto, H. Ohne, "An improved version of the generalized correlation of critical heat flux for convection boiling in uniformly heated vertical tubes," *International Journal of Heat Mass Transfer*, vol. 27(9), pp. 1641-1648, 1984.

[97] D. Bogojevic, K. Sefiane, A. J. Walton, H. Lin, G. Cummins, D. B . R. Kenning, T. G. Karayiannis, "Experimental investigation of non-uniform heating effect on flow boiling instabilities in a microchannel-based heat sink," *International Journal of Thermal Science*, vol. 50(3), pp. 309-324. 2011.

[98] http://www.methanol.org.

[99] A. Klamt, *COSMO-RS : from quantum chemistry to fluid phase thermodynamics and drug design*, 1st ed. Amsterdam: Boston, 2005.

[100] P. Warrier, "Design and evaluation of heat transfer fluids for direct immersion cooling of electronic systems," Ph.D. dissertation, Chemical Engineering, Georgia Institute of Technology, Atlanta, GA, 2012.

[101] P. Warrier, and A. S. Teja, "Density, viscosity, and thermal conductivity of mixtures of 1-ethoxy-1,1,2,2,3,3,4,4,4-nonafluorobutane (HFE 7200) with Methanol and 1-Ethoxybutane," *Journal of Chemical & Engineering Data*, vol. 56, pp. 4291-4294, 2011.