DIGITAL FRINGE PROJECTION SYSTEM FOR MEASURING WARPAGE OF PAINTED AND UNPAINTED PBGAS AND BOARDS AND FEA STUDIES OF PBGA WARPAGE

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DIGITAL FRINGE PROJECTION SYSTEM FOR MEASURING WARPAGE OF PAINTED AND UNPAINTED PBGAS AND BOARDS AND FEA STUDIES OF PBGA WARPAGE

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This dissertation is dedicated to my parents

for their unconditional love and supports.

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LIST OF SYMBOLS

α	Observation angle of the camera
β	Illumination (or projection) angle
ε	Percentage error
$\bar{\varepsilon}$	Mean percentage error
E	Elastic modulus
F1	Solder bump pitch
F2	Package size
F3	Molding compound thickness
F4	Substrate thickness
N	Number of measurements
P	Fringe pitch
R	Out-of-plane resolution
σ	Standard deviation
σ_p	Pooled standard deviation
W_{max}	Maximum warpage
K_{max}	Maximum curvature of warpage
y	True height
y_i	Measured height
$\bar{y}$	Average of measured heights

LIST OF ABBREVIATIONS

ANOVA	Analysis of variance
APDL	ANSYS parametric design language
BT	Bismaleimide triazine
CCD	Charge-coupled device
CMM	Coordinate measuring machine
CMOS	Complementary metal–oxide semiconductor
DCA	Direct chip attachment
CP	Contact profilometer
CSP	Chip scale package
CTE	Coefficient of Thermal Expansion
CTF	Coordinate transfer function
DNF	Dual flat no lead
DFP	Digital fringe projection
DDFP	Dynamic digital fringe projection
DIP	Dual inline package
DLP	Digital light processing
DOE	Design of experiment
FC	Flip chip
FE	Finite element
FEA	Finite element analysis
GIS	Gauge indicator shim
DIC	Digital image correlation
IC	Integrated circuit

IO	Input and output
ITF	Intensity transfer function
LCD	Liquid crystal display
LED	Light-emitting diode
LFP	Laser fringe projection
LPI	Lines per inch
MSE	Mean squared error
NCP	Non-contact profilometer
PBGA	Plastic ball grid array
POP	Package on package
PWB	Printed wiring board
PWBA	Printed wiring board assembly
PZT	Piezoelectric transducer
QFN	Quad flat no lead
QFP	Quad flat package
RDRP	Ramp to dwell, ramp to peak
RGM	Region growing method
SM	Shadow moiré
SMT	Surface mount technology
SO	Small outlined
TGI	Twyman-green interferometry
TQFP	Thin quad flat package
TSOP	Thin small outlined package

SUMMARY

Improvements in chip package technologies have led to smaller package sizes and higher density circuitry that require superior reliability of chip packages. One of the crucial factors affecting the reliability of chip packages is warpage which primarily occurs during the reflow process. Because warpage may cause serious reliability problems such as solder bump failure and die cracking, warpage control has become a crucial task. As the reliability requirements of chip packages become more stringent, warpage control becomes more crucial. Advancements in warpage measurement and prediction would provide important steps toward addressing this concern. In this research, a novel warpage measurement system for measuring painted and unpainted chip packages, printed wiring boards (PWBs), and PWB assemblies (PWBAs) was developed. Also, parametric studies were performed to predict the warpage of plastic ball grid array (PBGA) packages affected by four geometric factors.

Among the various warpage measurement techniques, fringe projection techniques (i.e., laser fringe projection (LFP) and digital fringe projection (DFP)) have emerged as recent trends due to their non-contact, full-field, and high-resolution (for small viewing area) capabilities for measuring the warpage of chip packages and boards (i.e., PWBs and PWBAs). The fringe projection techniques generate and project fringe patterns onto a sample surface and these patterns are analyzed to obtain the warpage of the sample surface. For projecting the fringe patterns, the LFP and DFP techniques use a laser interferometer and a digital projector, respectively.

The most important features of the LFP technique are measurement accuracy and repeatability, although these features may be adversely impacted by noisy fringe patterns caused by laser speckle from the laser interferometer. In order to minimize laser speckle noise, this study optimized its control parameters (i.e., laser power, camera exposure, and camera gain) through the use of the Taguchi's design of experiment method, the analysis of variance, and the regression method. Another important feature of the LFP system is measurement speed, and a necessary step to improve measurement speed is to reduce the post-processing time. In order to reduce the post-processing time, this study developed a fast automatic chip package segmentation method using the region-growing algorithm.

With recent advancements in digital projection technology, the DFP technique has become popular for measuring the warpage of small viewing areas on chip packages and boards. In comparison to the LFP technique, the DFP technique has no laser speckle because it uses a digital projector instead of the laser interferometer. However, the DFP technique introduces a different source of error, the gamma nonlinearity of the digital projector. This research developed a DFP system for measuring the warpage of chip packages and boards, and compared the measurement capabilities and experimental results obtained against those obtained with the LFP system.

When using the fringe projection techniques, reflective paint is generally sprayed on the sample surface to ensure uniform surface reflectance and to obtain better fringe image contrasts in the measurement process. However, painted samples may not be reused, and the spray-painting process is not suitable for the assembly line. To solve this problem, this study developed a novel dynamic digital fringe projection (DDFP) technique for measuring the warpage of unpainted chip packages and boards. The DDFP

technique generates a dynamic fringe pattern, in which a proper fringe intensity distribution is dynamically determined based on the surface reflectance of an unpainted sample in order to obtain better fringe image contrasts. The DDFP technique includes an automatic method to segment the chip package and PWB regions in an unpainted PWBA image. It also incorporates calibration methods to compensate for the mismatches in coordinates and intensities between the projected and captured images.

In addition to warpage measurement, accurate warpage prediction is an important factor in controlling the reliability of chip packages. The finite element analysis (FEA) has been widely used to investigate warpage behavior of chip packages and boards. One of the most commonly used chip packages is the PBGA package, which has widespread applications in various electronic devices, such as digital televisions, microcontrollers, laptops, and tablets. In order to assess the effects of solder bump pitch, package size, and molding compound and substrate thicknesses on PBGA warpage (i.e. the warpage of PBGA packages) after the reflow process, this research conducted parametric studies using the FEA.

As chip packages and boards continue to diversify, choosing the most suitable warpage measurement technique for a particular application becomes a daunting task for manufacturing engineers. To solve this problem, this study developed a selection guideline of warpage measurement techniques.

The results of this will help to improve the yields and reliability of chip packages and boards, reduce the manufacturing costs and time to market for chip packages and boards and ultimately reduce the prices of end-products.

CHAPTER 1

INTRODUCTION

An integrated circuit (also known as IC or chip) is a set of electronic circuits integrated on a small plate of semiconducting material such as silicon. Electronic packaging involves a series of processes toward the end of the microelectronics manufacturing process, in which ICs and discrete electronic components are electronically interconnected and mechanically assembled [1]. This study is motivated by concerns about thermomechanical reliability during the assembly process.

1.1 Electronic Packaging Technologies

In early 1960s, IC technology was developed to achieve high-functionality electronic products by integrating hundreds of transistors on a small plate of semiconductor material. Over the years, IC technologies consistently have improved, achieving smaller chip sizes and more circuitry on each chip as Moore predicted in 1965 [2]. Compared to the first microprocessor that had 2,300 transistors on a chip [3], current microprocessors can accommodate more than four billion transistors. These embedding technologies also have enabled low unit costs, low switching power consumption, and high speed for ICs. To use these ICs, however, they have to be packaged, tested, and assembled on a system board [4].

Electronic packaging involves a series of processes, in which ICs and discrete electronic components are electronically interconnected and mechanically assembled to form electronic products [1]. As shown in Figure 1.1, electronic packaging can be

divided into three levels [4]. In the first level, an IC (or chip) is interconnected on a substrate and packaged to form a chip package. The primary interconnection methods are wire bonding and flip chip [4]. In the second packaging level, the chip packages are ready to be assembled onto a PWB to form a PWBA [5]. An example of a PWBA is a computer memory board, consisting of several chip packages assembled onto a PWB. A single PWBA may not carry all the components necessary to form a complete system, such as a personal computer, because some systems require many components to provide high transactional throughput [4]. In order to form the complete system, several PWBAs are generally connected to one another with connectors and cables at the third level of packaging. This research will focus on the second level of the packaging hierarchy.

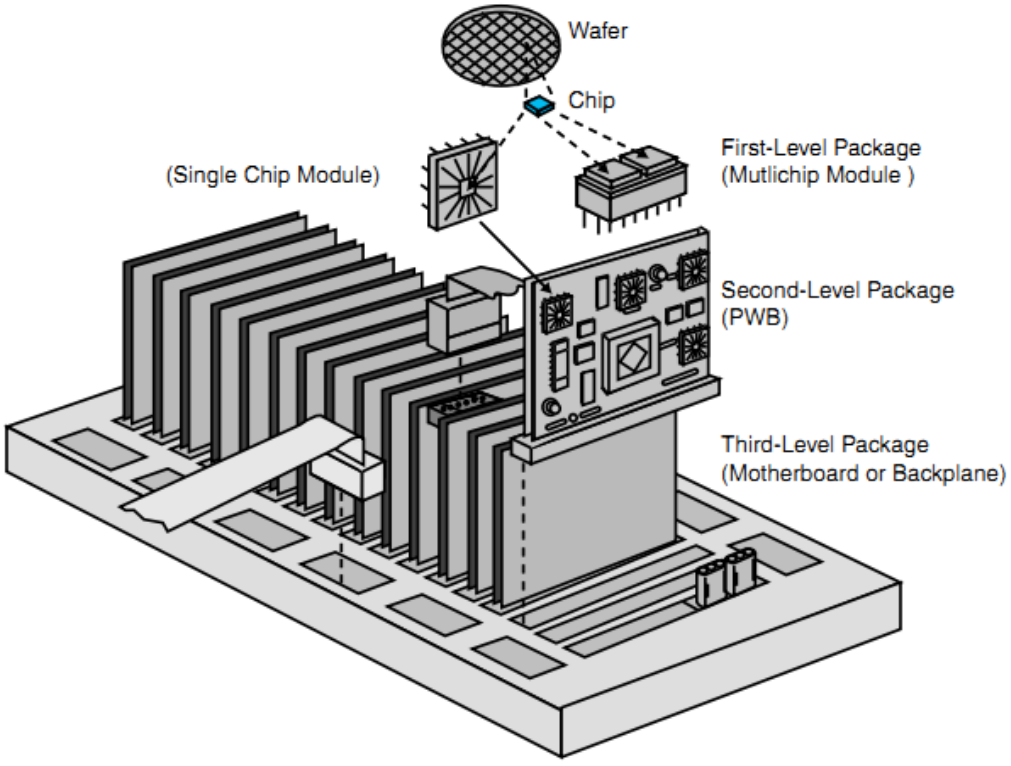


Figure 1.1. Electronic packaging hierarchy [4]

As noted above, the second level of the packaging involves interconnecting chip packages and a PWB. The two primary methods employed for second-level interconnections are the through-hole and surface mount technologies [4]. Using the through-hole technology, the leads of the chip packages are inserted into plated holes on the PWB. Examples of through-hole packages are the dual inline package (DIP) and the pin grid array (PGA) package, shown in Figure 1.2. In DIPs, the pins are distributed along the sides of the package. To achieve a higher input/output (I/O) count, PGAs are used when the pins are distributed in an area array underneath the package surface [4].

Dual Inline Package (DIP) Pin Grid Array (PGA) Package

Figure 1.2. Though-hole packages

On the other hand, in surface mount technology (SMT), the chip packages are directly mounted onto the surface of the PWB via leads, flat contacts, a ball grid array (BGA), etc. The use of SMT has grown rapidly in the past decade because it allows for the assembly of small chip packages with high density I/Os [1]. Examples of SMT packages are shown in Figure 1.3. Because of its extremely low cost, the small-outlined (SO) package, which is suitable for low I/O packages, is the most widely used. The quad flat package (QFP) is an extension of the SO package with a higher I/O count. Both the SO packages and QFPs use leads that can be attached to the PWB. However, BGA packages, developed in the late 1980s, use solder balls, which can be placed underneath the surface of the packages in an area-array manner. The BGA significantly increases the

I/O count of the packages. The increased demand for smaller and thinner packages for use in small electronic devices such as smartphones has led to the development of the chip scale package (CSP), which is no larger than 1.2 times the size of the chip. Three-dimensional (3-D) packages, in which ICs are stacked vertically, are a more recent development designed to produce higher integration and performance in chip packages [6].

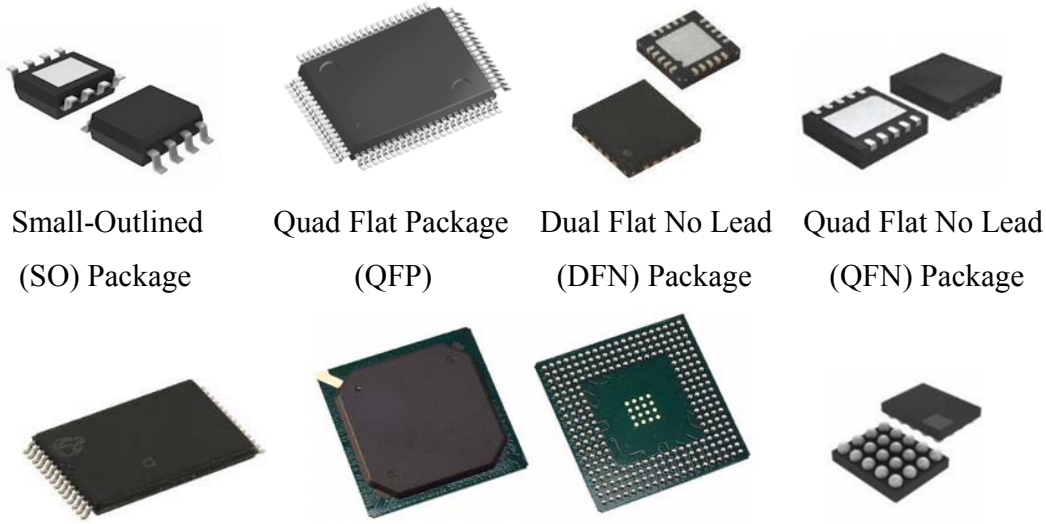


Figure 1.3. Various types of SMT packages

A forecast of the relative share of production of the various chip packages from 2015 to 2017 is summarized in Table 1.1. This forecast shows that SMT will be used in more than 80% of total chip packages. It also shows that BGA, SO, and QFN packages will make up the biggest portion of total chip packages units. Therefore, this research will focus on BGA packages that uses SMT assembly.

Table 1.1. Forecast of the relative share of production of the various chip packages [7]

Package Types	Assembly Method	The Relative Share of Production (%)		
		2015	**2016**	**2017**
DIP	Through-Hole	6.60	6.50	6.40
SO	SMT	19.30	19.00	18.80
QFP	SMT	7.20	7.20	7.10
DFN	SMT	7.00	7.20	7.50
QFN	SMT	12.40	12.90	13.40
TSOP	SMT	11.40	11.00	10.60
PGA	SMT	0.10	0.10	0.10
BGA[a]	SMT	18.80	18.90	19.00
CSP	SMT	5.30	5.50	5.60
Others	-	11.90	11.70	11.50

[a]Including fine-pitch BGA

1.2 SMT Assembly Process

The SMT assembly process involves screen printing, chip package placement, and reflow, as shown in Figure 1.4. In the screen printing process, a stencil, which has holes that line up exactly with the pads on the PWB, is placed over the PWB to be assembled. Solder paste is applied to the stencil in order to dispense solder paste onto the pads. After the screen printing process, a chip package placement machine distributes the chip packages onto their appropriate locations on the PWB. To place the chip packages in the correct locations, the chip package placement machine uses fiducial marks on the PWB as references. The solder paste dispensed on the PWB acts as a temporary glue to hold the chip packages onto the PWB. After the placement process, the chip packages are rigidly assembled on the PWB via a process called reflow soldering.

Figure 1.4. SMT assembly line [1]

In industry, many types of reflow processes are used, such as infrared reflow, vapor-phase reflow, in-line conduction reflow, hot-bar reflow, laser reflow and forced convection reflow [5], but forced convection reflow is the most widely used method [1]. Forced convection reflow ovens contain either five or seven temperature zones, as shown in Figure 1.5, where PWBAs are heated from both the top and bottom of the oven. The reflow temperature profile is determined by the zone temperatures and the speed of the conveyor carrying the PWBAs. Even though the forced convection reflow process is slow, its uniform heating and slow heat transfer rate minimize component cracking [1].

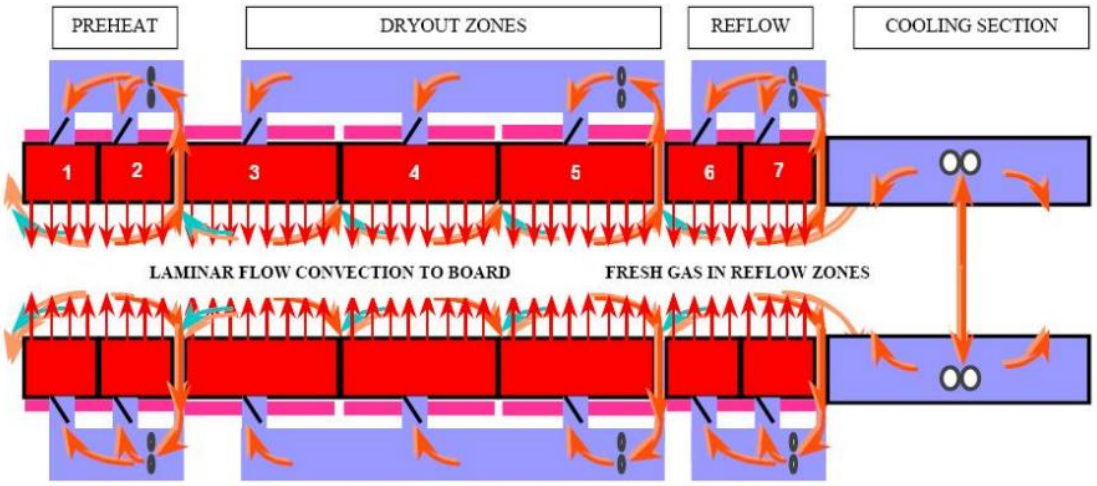


Figure 1.5. Schematic of seven chamber convective reflow oven [5]

1.3 Warpage and the Thermomechanical Reliability of Chip Packages

During the reflow process, the PWBs as well as the chip packages generally warp due to the coefficient of thermal expansion (CTE) mismatches within the PWBs and chip packages. This warpage can lead to a number of problems. If induced warpage in the chip packages or PWBs exceeds critical values, one of the resultant effects is component misregistration during the component placement and insertion processes. The presence of warpage can also cause reliability problems in chip packages such as die cracking, underfill delamination, creep and voids in solder bumps, and fatigue failure in solder bumps resulting from high residual stresses [8-11]. Several of these conditions are illustrated in Figure 1.6.

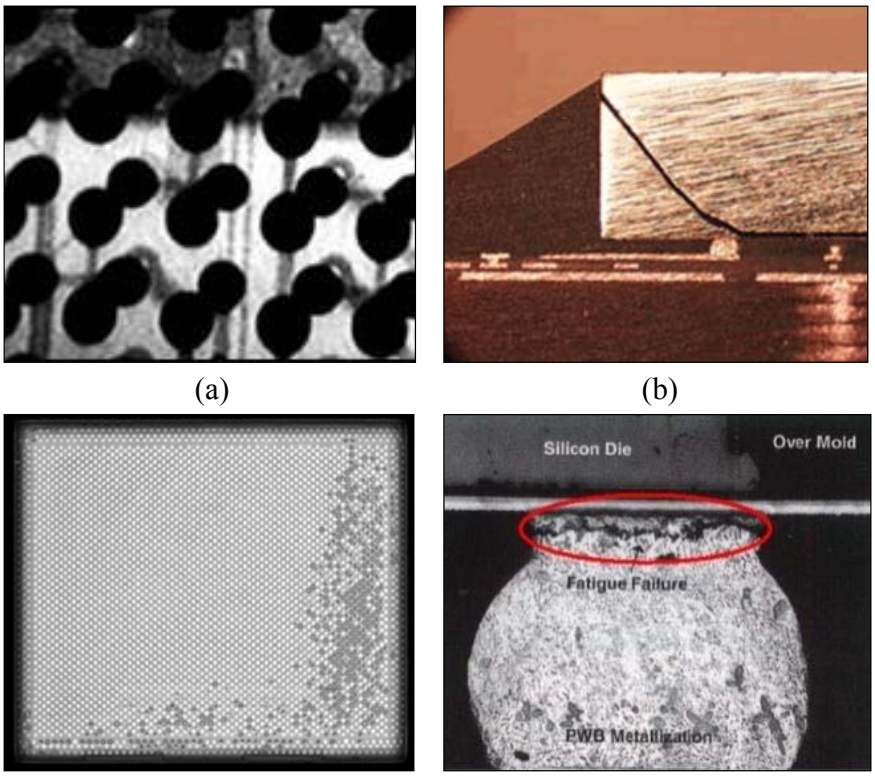


Figure 1.6. (a) Component misregistration, (b) die cracking, (c) underfill delamination, and (d) solder bump fatigue failure [1]

1.4 Warpage Measurement and Prediction

The effects of warpage on the failure of chip packages have rendered warpage control a crucial factor during the reflow process. To address this concern, the first step is to measure the warpage accurately and quickly. Several techniques for measuring the warpage of chip packages and boards (i.e., PWBs and PWBAs) have been developed. In the early days, contact measurement techniques, such as the contact profilometer, were used to measure warpage. As the requirement arose for higher measurement speed and in-line measurement capabilities, several non-contact warpage measurement techniques were developed.

For example, moiré techniques are widely used to measure the warpage of chip packages and boards due to their noncontact, full-field, fast, and high-resolution measurement capabilities. The moiré techniques use fringe patterns to obtain the out-of-plane displacement of a sample surface, and they can be classified into the following three types based on how they generate the fringe patterns: the shadow moiré, LFP, and DFP techniques. The shadow moiré uses glass grating, located very close to the sample, to generate the fringe patterns. This technique is the most commonly used for measuring warpage because it is easy to set up and to calibrate, and it facilitates image calculations [12]. However, it is not a suitable technique for simultaneously measuring the warpage of chip package(s) and PWB in a PWBA because the glass grating must be placed very close to the sample surface [12]. Such proximity can also affect the thermal behavior of the sample during the reflow process [12].

The fringe projection techniques (i.e. the LFP and DFP techniques) can be used to overcome these disadvantages of the shadow moiré technique because they do not require

glass grating. Instead, the LFP technique typically uses a laser interferometer to generate the fringe patterns. Its major disadvantage, however, is its noisy fringe patterns caused by laser speckle [13]. The DFP technique overcomes this drawback because it uses a digital projector to generate the fringe patterns. However, the DFP technique has its own disadvantage in the form of gamma nonlinearity [14], which represents the nonlinear relationship between the input and output intensities of the digital projector.

In addition to warpage measurements, accurate warpage prediction is an important task for controlling the reliability of the chip package. The FEA has been widely used to investigate the warpage behavior of chip packages and boards by developing and using their finite element (FE) models validated by the warpage measurement results. The plastic ball grid array (PBGA) package is one of the most commonly used chip packages and is employed in various electronic devices such as digital televisions, microcontrollers, laptops, and tablets. Because PBGA packages have various I/O densities, sizes, and thicknesses that affect warpage, their design requires accurate prediction of PBGA warpage resulting from solder bump pitch, package size, and molding compound and substrate thicknesses.

1.5 Research Objectives

The major goals of this research are to develop a novel warpage measurement system for measuring painted and unpainted chip packages and boards and to assess the effects of solder bump pitch, package size, and molding compound and substrate thicknesses on PBGA warpage after the reflow process. More specifically, the research objectives are:

1) To improve the measurement capabilities of the LFP system by reducing its laser speckle noise and post-processing time. Two of the key features of the LFP system are its measurement accuracy and repeatability. These features are adversely impacted by noisy fringe patterns caused by laser speckle from the laser interferometer of the LFP system. In order to minimize the laser speckle noise, three control parameters (i.e. laser power, camera exposure, and camera gain) will be optimized.

The current automatic chip package segmentation methods require high post-processing time when they are used to simultaneously measure the separate warpage of chip package(s) and PWB in a PWBA. In order to reduce the post-processing time, a fast automatic chip package segmentation method using the region-growing algorithm will be developed.

2) To develop a DFP system for measuring the warpage of painted and unpainted chip packages and boards. With advances in digital projection technology, the DFP technique has become popular for measuring the warpage of chip packages and boards. The DFP technique lacks the disadvantages of the laser speckle in the LFP system and is easier to control because it uses a digital projector instead of a laser interferometer. However, the DFP technique introduces a different source of error resulting from the gamma nonlinearity of the digital projector. In this study, a DFP system that includes a customized software for measuring the warpage of chip packages and boards will be developed. The measurement capabilities and experimental results obtained by using the LFP and DFP systems will be compared.

Similar to the shadow moiré and LFP systems, the DFP system requires reflective painting, which is generally sprayed on the sample surface to ensure uniform surface

reflectance and to obtain better fringe image contrasts in the measurement process. However, painted samples may not be reused, and the spray-painting process is not suitable for an assembly line. To solve this problem, a novel DDFP technique, for measuring the warpage of unpainted chip packages and boards will be developed. This includes development of an automatic method to segment the chip package and PWB regions in an unpainted PWBA image. It also includes development of calibration methods that compensate for mismatches in coordinates and intensities between the projected and captured images.

3) To assess the effects of solder bump pitch, package size, and molding compound and substrate thicknesses on PBGA warpage after the reflow process using the FEA. The PBGA package is one of the most widely used chip packages in electronic packaging devices. Accurate prediction of PBGA warpage resulting from solder bump density, package size, and package thickness is necessary during PBGA design. In this research, parametric FE studies to access the effects of solder bump pitch, package size, and molding compound and substrate thicknesses on PBGA warpage after the reflow process will be carried out. The full-factorial design of experiments (DOE) method will be used to design simulation runs while the simulation results incorporate all individual and two-factorial interacting effects of the factors. The analysis of variance (ANOVA) will be used to identify the effects of each factor on PBGA warpage. The correlation between PBGA warpage and the four factors will be studied using the regression method.

4) To develop a guideline for selecting the most suitable warpage measurement technique for a particular application. As the chip packages and boards diversify, choosing the most suitable warpage measurement technique for a particular application

becomes a challenging task for manufacturing engineers. In this study, a guideline will be developed that manufacturing engineers can use when selecting a warpage measurement technique.

After this introduction, literature relevant to the research objectives is reviewed in Chapter 2. Chapter 3 presents the improvement of the measurement capabilities of the LFP system, and Chapter 4 presents the development of the DFP system for measuring painted and unpainted chip packages and boards. Chapter 5 presents the parametric studies of the effects of solder bump pitch, package size, and molding compound and substrate thicknesses on PBGA warpage using the FEA. Chapter 6 discusses the guideline for selecting warpage measurement technique. Finally, conclusions, technical contributions, and recommendations for future work are given in Chapter 7.

CHAPTER 2

LITERATURE REVIEW

Many researchers have studied the warpage of chip packages and boards. The literature related to the warpage measurement techniques is reviewed and an overview of the DFP technique is presented with related literature reviews. In addition, the literature related to the parametric study used to investigate the warpage behavior of chip packages and boards is reviewed.

2.1 Warpage Measurement Techniques

Warpage measurement techniques can be classified into two major categories: contact type and non-contact type. In the early days, contact measurement techniques such as the gauge indicator shim method and the contact profilometry were used to measure warpage. As higher measurement accuracy and in-line measurement capabilities became necessary, several non-contact measurement techniques were developed for measuring warpage.

2.1.1 Contact Type

Traditionally, industry has used contact measurement techniques. The two most common techniques for measuring the warpage of chip packages and PWBs are the gauge indicator shim method and the contact profilometry.

Gauge Indicator Shim Method

The oldest techniques for measuring the warpage of PWBs are mechanical methods [15] such as the gauge indicator shim method. In this method, feeler gauges are placed under a PWB so that the level of its warpage can be determined. The feeler gauges are thin metal blocks with various known thicknesses, shown in Figure 2.1.

Figure 2.1. A feeler gauge set

Contact Profilometry

The contact profilometry uses a vertical stylus or probe for measuring surface variation as a function of position. The stylus or probe moves laterally in contact with the surface across a specified distance and is controlled by stepper (or step) motors or servo motors. While the stylus moves, the transducer connected to the stylus generates an analog signal, generally voltage difference, corresponding to the vertical displacement of the stylus. This analog signal can be directly converted to the surface profile (or surface height variation) of a sample. Some applications of the contact profilometry are stylus scratch and atomic force microscopy.

Yang et al. [16] used a contact probe to measure process-induced warpage during the array-molding process of quad flat non-lead packages. Miyake et al. [17], who

investigated the relationship between the magnitude of the warpage of a TSOP and its compound properties, used stylus profilometry to measure the warpage of the TSOP. Yeung and Yeun [18, 19], who examined the variation in processing conditions on predicting the warpage of a QFP, used a touch probe to measure the warpage of the QFP ranging from 5.0 μm to 74 μm. Figure 2.2 shows the warpage profile generated from the 25-point measurements using the touch probe in [18].

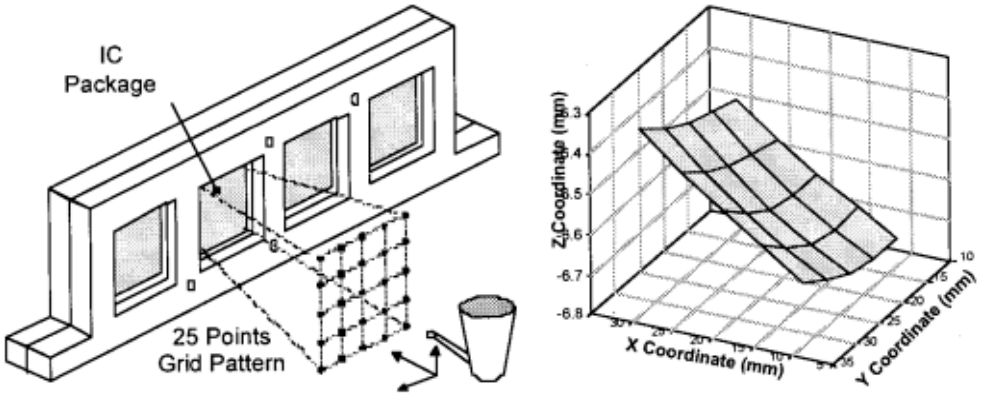


Figure 2.2. Warpage measurement of QFP using a touch probe [18]

2.1.2 Non-Contact Type

Since the 1980s, with the development of non-contact measurement technologies, industry has shifted away from the contact techniques because of the relative advantages offered by the new technologies. By eliminating the need for contact with the sample surface – these technologies provide much faster options for measuring large numbers of points as the majority of these methods are full-field measurement techniques. In non-contact measurement techniques, light is projected onto a physical part, reflected back from the surface of the part, and sensed by an electronic detection device that is typically a camera or sensor. Then surface shape is determined by analyzing the sensed light signal.

Non-Contact Profilometry

The non-contact profilometry is a non-destructive surface measurement technique for measuring the height of a sample or its surface profile. A laser sensor is usually used, and the laser sensor is moved laterally by a stage equipped with step or servo motors while sensing the reflected light from the surface.

The common methods used to get the surface profile using reflected light from the surface are the time-of-flight and triangulation principles. Between these two principles, the triangulation principle is generally used for the warpage measurement because it is capable of high-resolution measurement. The triangulation principle uses the incident and reflected angles of the laser beam relative to a baseline to determine surface coordinates (Figure 2.3).

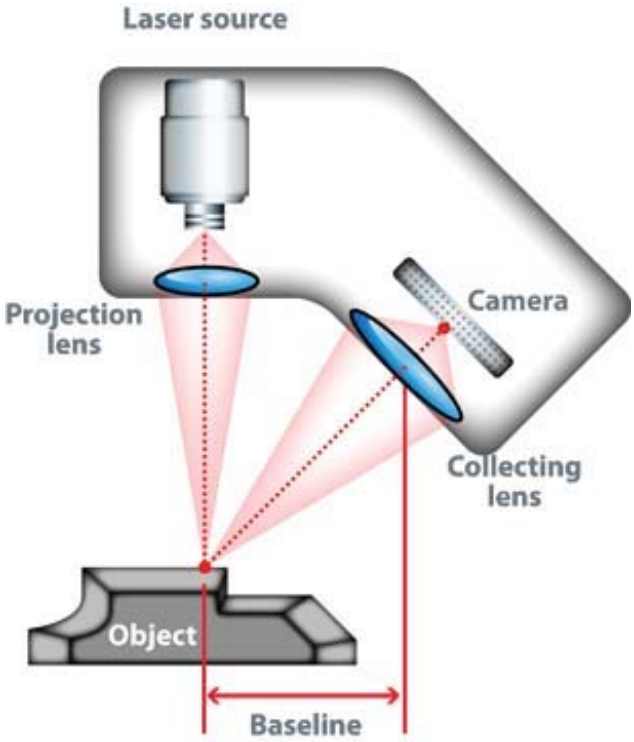


Figure 2.3. Schematic diagram of a non-contact laser profilometer using triangulation principle

Yean et al. [20] used a laser profilometer working in triangulation mode to measure the warpage of BGA packages. The diagonal length of the BGA package was scanned using a laser beam with a diameter of approximately 2 μm, and detailed topology maps of the surface were then generated. Sawada et al. [21] measured the warpage of flip-chip BGA packages at the temperature ranging from -55°C to 230°C using the flatness measurement system with a laser scanning microscope. Fayolle and Lecomte [22] developed a 3D surface measurement system using the laser triangulation method to measure the warpage of chip packages during the fast temperature profiles. Du et al. [23] developed an optical method to measure the surface curvatures of flip-chip packages during the thermal cycle by using four laser beams with 10 μm resolution of the detector.

Optical Interferometry

Optical interferometry relies on interference of two or more light waves. There are many different kinds of optical configurations of optical interferometry. Among these configurations, the most widely used methods for measuring warpage of electronic packages are Twyman-Green interferometry, Fizeau interferometry, and Speckle interferometry. The basic principles behind each method are similar but the differences among the devices depend on the optical setups.

Twyman-Green Interferometry

Twyman-Green interferometry is a classical and commonly used form of interferometry that uses the interference of coherent light, usually laser light. Conceptually, a laser beam is collimated and split into two paths after passing a beam splitter. One is the active pass, which is reflected by the specimen, and the other is the

reference pass, which is reflected by the reference, as shown in Figure 2.4. The interference of these two reflected beams creates a fringe pattern.

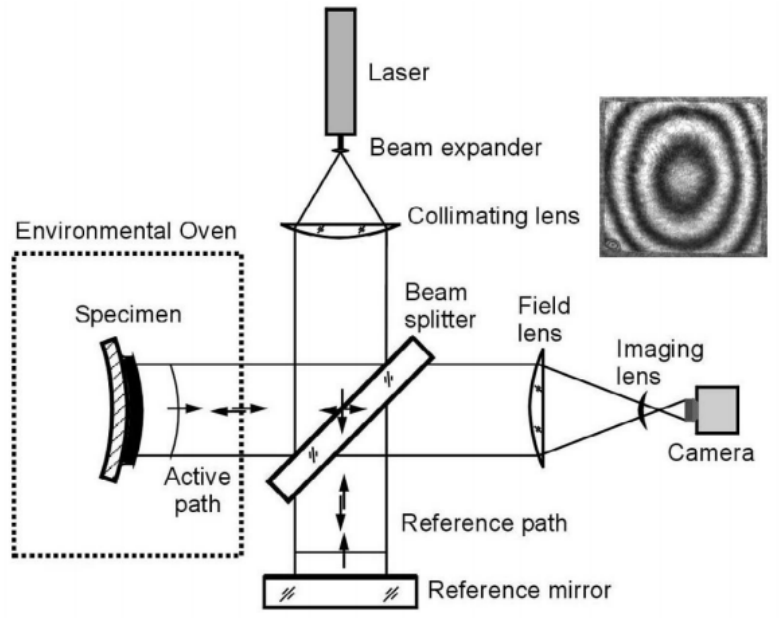


Figure 2.4. Schematic diagram of a Twyman-Green interferometer [24]

Hartsough, et al. [24] used the Twyman-Green interferometry system (Figure 2.4) with sub-micrometer scale resolution to measure the real time warpage of PWBAs subjected to thermal loading. Tsai et al. [25] used the Twyman-Green interferometry to measure the warpage of flip-chip BGA packages during the reflow process with a resolution of 0.32 μm. Xinlin et al. [26] used real-time Twyman-Green interferometry to measure the deformation of the silicon surface of direct chip attachment (DCA) assemblies under thermal loading.

Fizeau Interferometry

Along with Twyman-Green interferometry, Fizeau interferometry is a classical form of interferometry that uses the interference of coherent light, usually light from a laser. A practical optical setup of Fizeau interferometry is shown in Figure 2.5. In this

setup, a beam from the light source is expanded by the beam expander and collimated by the collimating lens. The beam then meets the optical flat that is the heart of Fizeau interferometry, where a portion of the beam is reflected from the back surface of the optical flat and the reflected light works as the reference light. The other portion is transmitted through the optical flat and reflected from the specimen surface. These two light waves recombine inside the interferometer, and are collected by an imaging system.

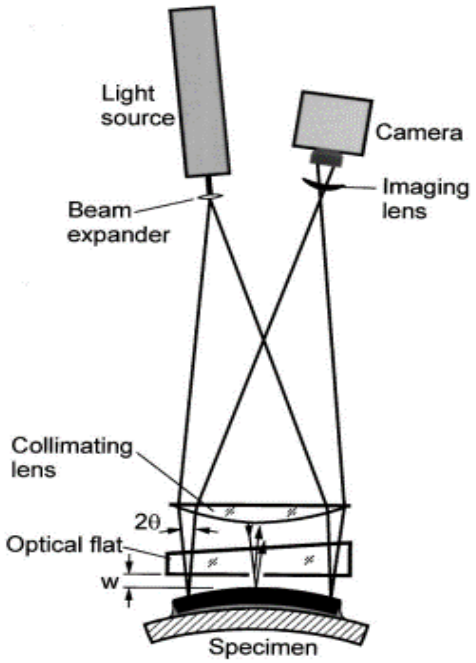


Figure 2.5. Schematic diagram of a Fizeau interferometer [27]

Verma, et al. [27-30] developed Far infrared Fizeau interferometry to measure the warpage of flip chip PBGA packages with a resolution of 5.3 μm. Verma, et al. [31] also developed an apparatus that combines Far infrared Fizeau interferometry and the shadow moiré technique to measure the warpage of flip chip PBGA packages with various resolutions, ranging from 5.3 μm to 100 μm.

Electronic Speckle Pattern Interferometry

The principle of electronic speckle pattern interferometry (ESPI) is depicted in Figure 2.6. When a coherent light or laser beam is incident on a rough surface, a speckle pattern is formed. The reference coherent light from the light source is superimposed using a charge-coupled device (CCD) camera, and this results in an interference pattern, which is also a speckle pattern. If the surface is deformed, the phase of the speckle pattern will change. A series of phase-shifted speckle patterns are used to generate a phase map that provides quantitative and directional information of the surface displacement. This method theoretically allows for the measurement of surface deformation with a 10 nm resolution [32].

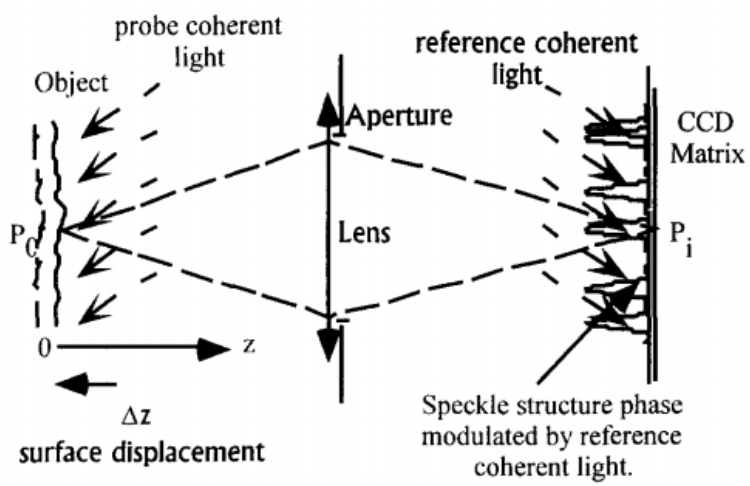


Figure 2.6. Schematic diagram of an electronic speckle pattern interferometer [32]

Toh et al. [33] used laser-based speckle interferometry to analyze the real-time warpage of thin quad packages with varied moisture exposure time during the surface mount process. Dilhaire et al. [32] studied the warpage and the thermo-mechanical behavior of chips. He used the ESPI to measure the warpage of 2×3 mm chips in the sub-micrometer range.

Digital Image Correlation

Digital image correlation (DIC) is a non-contact and full-field technique that can be used to measure both in-plane and out-of-plane displacements of a sample surface [34]. A random pattern with good contrast is applied to the surface of the sample. As the pattern deforms along the sample, the deformation is then recorded with two CCD cameras and later analyzed using digital image processing for measuring the deformation [35].

Pan et al. [34] used a DIC system as shown in Figure 2.7 to measure the temperature dependent warpage of BGAs with a resolution of 1 μm. Sato and Yu [36] developed a new method to measure the real time warpage of a CSP using the DIC technique. Shishido et al. [37] developed a DIC system in conjunction with an optical microscope for measuring the thermal strain in the micron region of PCBs.

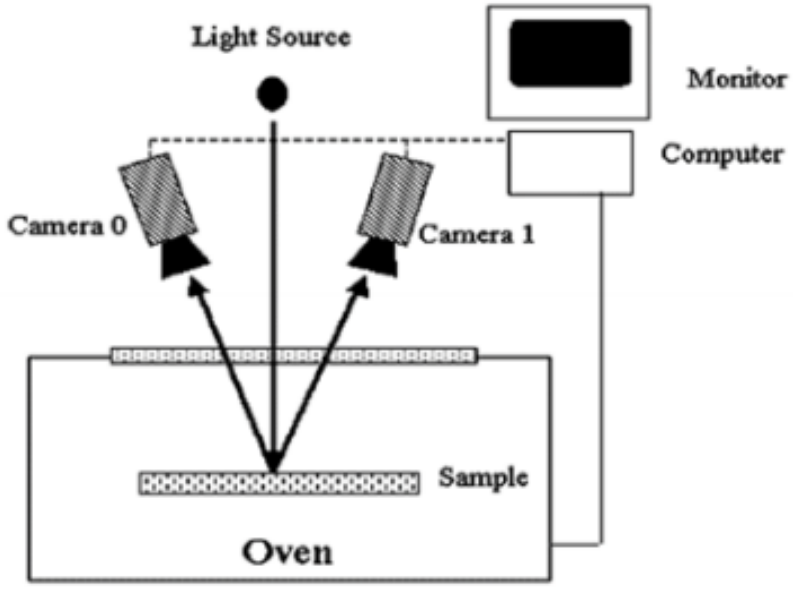


Figure 2.7. Schematic diagram of a DIC system [34]

Moiré Techniques

The term "moiré" is a French word meaning "an irregular wavy finish on a fabric" that was first introduced in 1818 (Webster's 1981). Moiré interferometry uses moiré fringes generated by overlapping two fringe patterns for measuring the surface height variation of a specimen. One fringe pattern (or grating) is called a reference grating and the other fringe pattern is called a specimen grating. The specimen grating is distorted in accordance with the surface height variation of the specimen.

Because the moiré techniques have non-contact, full-field, fast, and high-resolution measurement capabilities, they have frequently been used to measure the warpage of chip packages and boards [38, 39]. To increase the measurement resolution of the moiré techniques, the phase-shifting method [40] is widely used. The moiré techniques can be classified into three types based on how they generate the fringe patterns: shadow moiré; LFP, or projection moiré; and DFP.

Shadow Moiré

In the shadow moiré technique, the fringe pattern (or grating) is generated using a master grating (reference grating), usually made of glass, as shown in Figure 2.8. A white light source at approximately 45 degrees to the master grating produces a shadow of the grating on the sample surface, which is referred to as the specimen grating. The overlapping of the specimen grating and the reference grating creates moiré fringes, which is then used to calculate the warpage of the sample. For phase shifting, precision motors (step or servo motors) connected to the sample holder move the sample surface up and down [1]. The resolution of the shadow moiré technique depends on the pitch of the glass grating. As the grating pitch increases, the resolution will decrease correspondingly.

On the other hand, the field of view (FOV) is independent from the resolution or the grating pitch but dependent on the size of the glass grating.

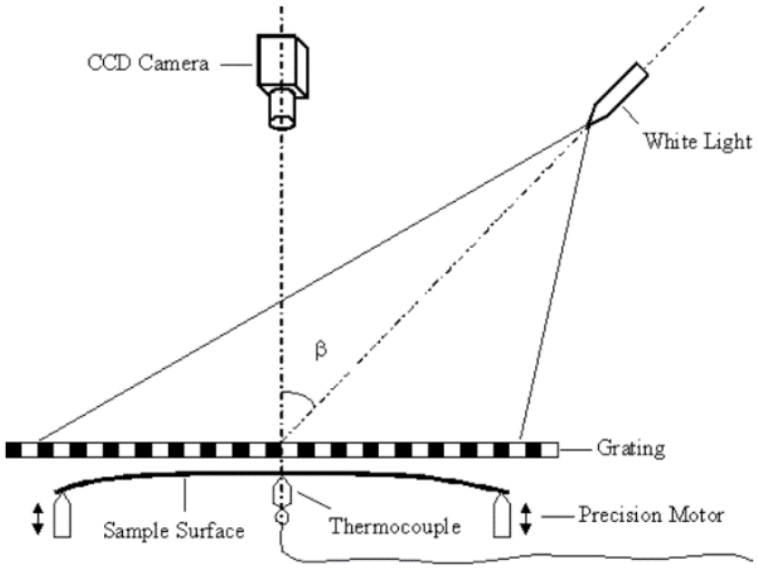


Figure 2.8. Setup of a shadow moiré system [1]

Shadow moiré was first used by Ume et al. [12, 41-45] at the Georgia Institute of Technology (Georgia Tech) for measuring thermally induced warpage of the PWB or BGA during a simulated reflow process with a resolution of 1.25 μm. Following this discovery, many other researchers also have used the shadow moiré technique to measure the warpage of electronic components or PWBs. For example, the method has been used to measure thermally induced warpage of BGA packages [8, 24, 30, 34, 46-64], PWBs [65-67], flexible circuit boards [68], and 3D packages such as package on package (POP) [69-78] with resolution (or sensitivity) ranging from 1.25μm [12] to 30μm [62]. A commercially available shadow moiré system can achieve a practical resolution of 0.83 μm using a phase-shifting method and 300 lines-per-inch (LPI) grating (grating pitch is

1/300 inch). Its data acquisition and computation times are one to two seconds and three seconds, respectively, for a FOV up to 600×600 mm.

Laser Fringe Projection

In the LFP (or projection moiré) technique, a laser interferometer generates and projects the fringe pattern onto the sample surface as shown in Figure 2.9. A camera above the sample acquires fringe images that are phase modulated. The phase modulation can be calculated by obtaining a wrapped phase image from the fringe images with one of the fringe analysis methods. Among the fringe analysis methods, phase shifting method is widely used in the moiré techniques to increase measurement resolution. By applying an appropriate phase unwrapping algorithm to the wrapped phase image, a continuous phase distribution can be obtained and used to determine the surface profile of the sample. To increase the measurement accuracy, the surface profile of a flat reference is usually subtracted from the surface profile of the sample [14]. A piezoelectric transducer (PZT) is usually used to move the reference mirror of the laser interferometer for phase shifting, as does the precision motor in the shadow moiré technique. The theoretical out-of-plane resolution of the LFP can be calculated using the following equation 2.1 [46, 79]:

$$R = \frac{P}{C(tan\alpha + tan\beta)} \tag{2.1}$$

where R = the out-of-plane resolution, P = the fringe pitch, α = the observation angle of the camera, β = the illumination (or projection), and C = a coefficient of resolving power for the gray level of light intensity.

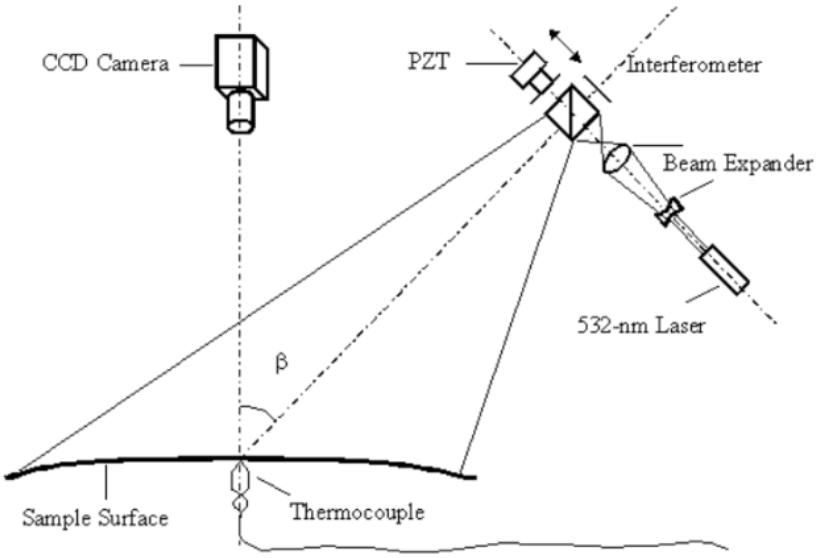


Figure 2.9. Setup of an LFP system [41]

Along with the shadow moiré technique, Ume et al. [12, 39, 80-85] used LFP for measuring warpage of the PWB or PWBA during the reflow process. Many other researchers have also used the LFP technique to measure BGA packages [84] and flexible boards [86, 87]. In some cases, a micro LFP technique that uses microscopic optics has been used to measure warpage of small chip packages with higher resolution [61, 79, 88, 89].

Digital Fringe Projection

The DFP technique is very similar to the LFP technique except that it generates the grating patterns digitally. In this approach, the fringe pattern is generated digitally by a computer and then projected by a computer-controlled digital projector onto the sample surface. Among the various techniques of digital projection such as liquid crystal display (LCD) and digital light processing (DLP), the DLP is widely used in DFP because it provides a higher contrast fringe pattern at a faster rate [90]. The DFP technique uses

projection lenses for obtaining the desired FOV. The theoretical out-of-plane resolution of the DFP can be calculated using equation 2.1, above.

Chang et al. [91] applied a DLP projector and a set of optical lenses (as shown in Figure 2.10) to a DFP system for measuring the warpage of a flip-chip BGA package and the profile of a solder ball of a flip chip package. They reduced the fringe pitch by directing the fringe pattern into a stereo zoom microscope. Yen et al [92, 93] also used a DFP system with a DLP projector for measuring the coplanarity of solder balls of BGA packages. Joo and Kim [94] enhanced the sensitivity of a DFP system by using immersion interferometry and the optical/digital fringe multiplication method that enables a 52 nm fringe pitch. Pan et al. [79] measured the warpage of PBGA packages using a DFP system with a resolution of 3 μm. Pan et al. [79] also developed a microscopic DFP system to measure the warpage of chip packages with size below 10×10 mm. The system enables fringe pitch of 80 μm. Shien et al. [95] developed a novel measurement system utilizing the DFP technique and measured the warpage of BGA packages. The results showed that the accuracy is 2.6 μm [95]. Michael et al. [96] used a fringe projection system to measure a PWBA during the reflow process with resolution of 2.5 μm. The range of practical resolution of a commercially available DFP system is from 2.5 μm to 20.0 μm using a phase-shifting method. The minimum and maximum resolutions correspond to FOVs of 25×25 mm and 200×200 mm respectively.

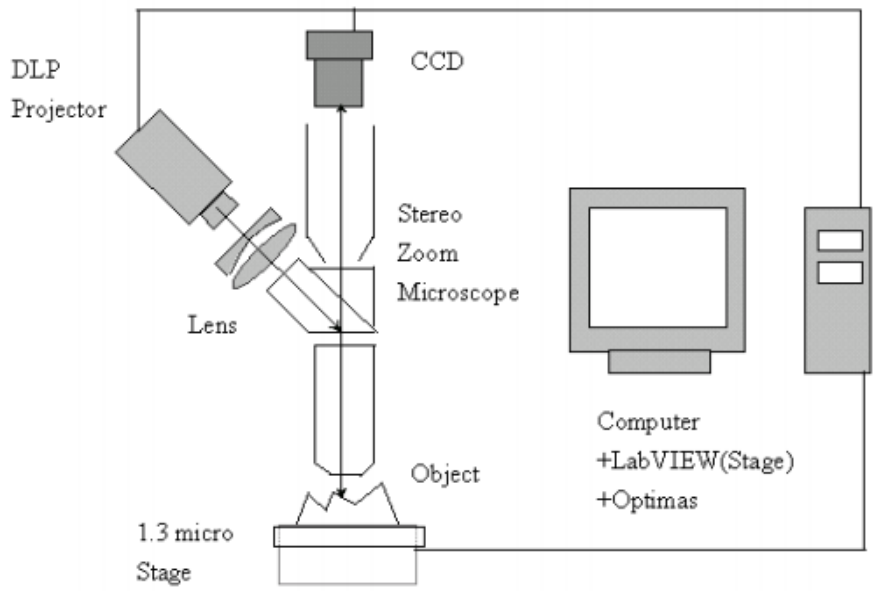


Figure 2.10. Setup of a DFP system [92]

An extensive review of the literature shows that the moiré techniques have been widely used for measuring the warpage of chip packages and boards because of their noncontact, full-field, fast, and high-resolution measurement capabilities. Among the moiré techniques, the LFP and DFP techniques can simultaneously measure the separate warpage of the chip packages and PWBs in PWBAs. Therefore, this study focuses on the LFP and DFP techniques for improving the measurement capabilities of the LFP system and developing a DFP system. Using the information obtained from the referenced literature, a selection guideline of warpage measurement techniques is also developed.

2.2 Digital Fringe Projection Technique

The measurement process using the DFP technique involves (1) generating and projecting a sinusoidal fringe pattern onto a sample surface, (2) capturing the fringe image(s) reflected from the sample surface, which is phase modulated by the surface

height distribution, (3) applying a fringe analysis method such as the phase-shifting methods to the captured fringe image(s) to obtain a wrapped phase image, (4) applying a phase unwrapping algorithm to the wrapped phase image to obtain an unwrapped phase image that contains a continuous phase distribution, and (5) converting the unwrapped phase image to a displacement image that contains the surface height distribution [14].

In the DFP technique, fringe analysis is the most important task because it significantly affects the overall performance of a DFP system in terms of measurement resolution and accuracy and computational complexity [14]. Among the several fringe analysis methods, such as Fourier transform, discrete-cosine transform, Hilbert transform, spatial phase detection, and the phase-shifting methods, the latter, in which the captured fringe patterns are incrementally spatially shifted, is typically applied as part of the DFP technique to enhance the measurement resolution [97, 98]. Based on the number of shifting steps, various phase-shifting methods such as the four-step [99], five-step, six-step [100], seven-step [101], and eight-step [102] phase-shifting methods have been developed. According to a comparative study provided by Proll et al. [103], measurement resolutions are not significantly different for the phase-shifting methods that use equal or more than four steps. Consequently, the four-step phase-shifting method is applied in this study. In order to use the four-step phase-shifting method, four fringe patterns are captured consecutively with a $\pi/2$ phase shift. Those fringe patterns are used to generate a wrapped phase image by using equation 2.2, as follows:

$$\varphi(x,y) = \arctan\left(\frac{I_3(x,y) - I_1(x,y)}{I_0(x,y) - I_2(x,y)}\right) \tag{2.2}$$

where $\varphi(x, y)$ = the wrapped phase at pixel (x, y), $I_i(x, y)$ = the intensity at pixel (x, y) of ith fringe image.

Because fringe analysis methods use an arctangent function, as shown in equation 2.2, to generate the wrapped phase, the interval of the wrapped phase is limited to $[-\pi, \pi]$. However, the actual phase can have an interval greater than 2π, whereby the wrapped phase can contain artificial discontinuities, called 2π discontinuities, as shown in Figure 2.11. Various phase unwrapping algorithms that remove 2π discontinuities have been developed. The commonly used phase unwrapping algorithms are the Goldstein, quality guided path following, mask-cut, Flynn's minimum discontinuity, unweighted least-squares, preconditioned conjugate gradient, multi-grid, and minimum L^p-norm algorithms [104]. Among these, the Goldstein algorithm [105] is the most widely used because it has simple input requirements and is very fast [104, 106]. However, Ding found that the Goldstein algorithm has a limitation for measuring PWBA warpage because the steep edges of assembled chip packages can produce unwrapping error when using the algorithm [107]. Because of this problem, Ding used the mask-cut phase unwrapping algorithm [108] and experimentally verified that it works well for measuring PWBA warpage [107]. Therefore, the mask-cut phase unwrapping algorithm is applied in this study to measure the warpage of chip packages and boards.

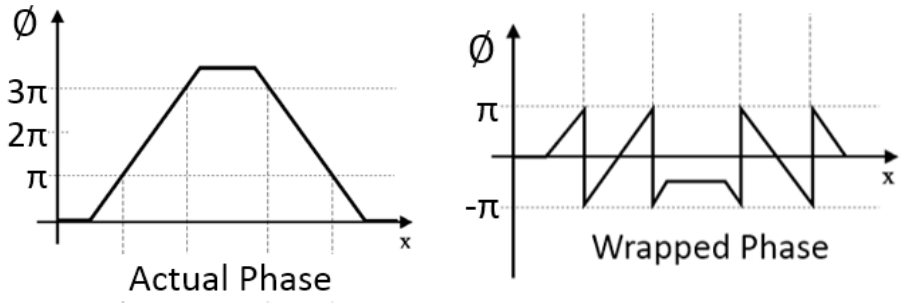


Figure 2.11. Actual phase and wrapped phase

Figure 2.12 shows the intensity flow in the DFP system. The intensity transfer function (ITF) represents the relationship between computer input intensity (I_I) and captured intensity (I_C). This relationship is generally nonlinear due primarily to the gamma nonlinearity of the digital projector [106]. The nonlinearity between I_I and I_C causes the presence of non-ideal sinusoidal waveforms in the captured fringe images, which decreases the measurement accuracy and repeatability of the DFP system [14].

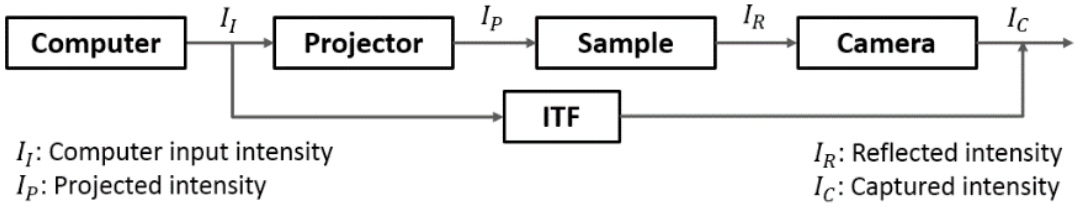


Figure 2.12. Intensity flow in the DFP system

The simplest and most accurate method of compensating for the nonlinearity is the lookup table method [109], which stores experimentally measured I_C values and corresponding I_I values in a lookup table, allowing input intensity to be modified using the lookup table to compensate for nonlinearity. However, because a lookup table is dependent on the reflectance of a sample surface, the lookup table method is very time-consuming when measuring unpainted samples. The polynomial regression method [106, 109] can be used to overcome this disadvantage by obtaining regression equations representing the relationship between I_I and Ic for each sample. The regression equations can be used to build lookup tables for each sample. In this study, the lookup table method is used to calibrate the nonlinearity when measuring the warpage of painted samples, which have uniform surface reflectance. When measuring the warpage of unpainted samples that have various reflectances, the polynomial regression method is applied together with the lookup table method to save calibration time.

2.3 Application of the FEA to Investigate the Warpage Behavior in Chip Packages and Boards

The parametric FEA has been used extensively to investigate the warpage behavior in chip packages and boards. Chong et al. [110] assessed the effects of die thickness on the warpage of fine-pitch BGA packages and found that package warpage increases with die thickness and the package size to die size ratio. Tsai et al. [54] conducted a parametric study to reduce the warpage of PBGA packages in terms of material properties of substrates and underfills. Li [111] studied the effects of the materials and structures of heat spreader and die sizes on the warpage of BGA packages. He found that a higher CTE of heat spreader, larger contacting area between heat spreader and substrate, and a larger and thicker die sizes reduce the warpage of BGA packages. Lee et al. [56] showed that die and package sizes have more effects on the warpage of BGA packages than the different material sets. Yi et al. [112] analyzed the effects of various material properties of die attach adhesive on the warpage of the die and the substrate of PBGA packages and found that the warpage increases significantly as modulus of the die attach increases. Ding and Ume [113] investigated the warpage of PWBA containing PBGA packages affected by PWB thickness, temperature loading, package location, and the CTE and elastic modulus of the solder bumps. The results showed that the elastic modulus of FR-4, temperature loading, and PWB thickness were the most influential parameters. Chen et al. [47] evaluated the effect of the CTE and elastic modulus of underfill on the warpage of flip-chip BGA packages and concluded that a low elastic modulus and a high CTE of the underfill decrease the warpage of flip-chip BGA packages. Verma et al. [30] studied the effect of the warpage of PBGA

packages on solder ball strains and identified critical design parameters to improve solder ball reliability. They found that the CTE of the substrate was most critical to solder ball reliability. Yeh and Ume et al. [114] investigated the effects of PWB material properties on thermally induced PWB warpage. The results showed that CTE was the most influential material property followed by elastic modulus and layer thickness. Dunne and Sitaraman [115] developed a process modeling methodology that enables monitoring of warpage and stresses during sequential multilayered substrate fabrication. The results demonstrated the importance of incorporating viscoelasticity into the model in order to accurately predict the warpage of the substrate. Moore et al. [116] studied the warpage of PBGA packages and found that the orientation and density of copper traces on bismaleimide triazine (BT) substrate have a significant effect on the warpage of BT substrate. Yeung et al. [19] used 3-D FE elastic and viscoelastic models to predict the warpage of QFPs and found that the viscoelastic model was more accurate than the elastic model. Tee et al. [117] studied the warpage of BGA packages and found that lower CTE and elastic modulus of molding compound are preferred for lower warpage. Also, a molding compound with high T_g and lower chemical shrinkage also helps to reduce warpage.

Thus, the literature shows that significant warpage studies have been conducted using the FEA and that various parameters affect the warpage of chip packages and boards. However, because the effects of solder bump pitch, package size, and molding compound and substrate thicknesses on the warpage of PBGA after the reflow process have not been studied, those effects are studied in this research using the FEA.

CHAPTER 3

IMPROVEMENT OF THE MEASUREMENT CAPABILITIES OF THE LFP SYSTEM BY REDUCING LASER SPECKLE NOISE AND POST-PROCESSING TIME

Measurement accuracy, repeatability, and speed are the most important features of a warpage measurement system. These features were improved in the LFP system by reducing its laser speckle noise and post-processing time. To minimize the laser speckle noise of the LFP system, its control parameters (laser power, camera exposure, and camera gain) were optimized by using the Taguchi's DOE method, the ANOVA, and the regression method. To reduce the post-processing time of the LFP system, a noble and fast chip package segmentation method, the region growing method (RGM), which can be used for simultaneous measurement of the separate warpage of the chip package(s) and the PWB in a PWBA, was developed.

3.1 LFP System Configuration

In previous warpage measurement research performed in the Advanced Electronic Packaging Laboratory (AEPL) at Georgia Tech, an LFP system was developed and used to measure the warpage of chip packages and boards [1, 5, 107]. The setup of this LFP system is shown in Figure 3.1. A coherent laser with a wavelength of 532 nm is used as the light source. The laser light is expanded through the beam expander and then enters a Michelson interferometer that generates a fringe pattern and projects it onto the sample surface. The reference mirror of the interferometer is mounted on a PZT for phase

shifting of the fringe pattern. A CCD camera is used to capture the image of the projected fringe pattern in its 60×45 mm FOV. The four-step phase-shifting method [40] is used to increase the measurement resolution and the mask-cut algorithm [104, 107] is used for phase unwrapping. The reference-subtraction and the linear conversion methods [14, 118] are used to convert the unwrapped phase image to a displacement image that contains the height distribution of the sample surface. The theoretical out-of-plane resolution of the LFP system for measuring warpage can be calculated using equation 2.1, above. For the calculation, the values of P, α, and β of the LFP system used in this study are 0.6 mm, 0º, and 45º, respectively. The value of C is 256 because 8-bit data are used to represent one pixel. The theoretical resolution of the LFP system is 2.34 μm.

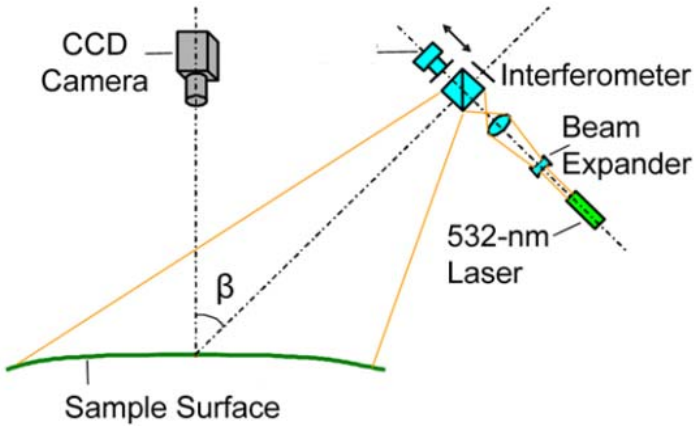
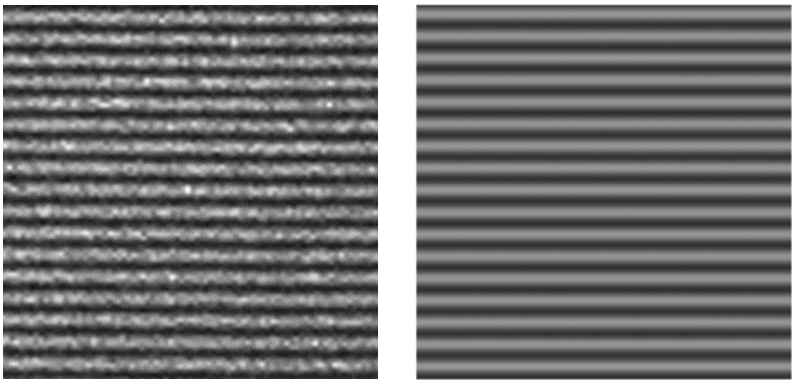


Figure 3.1. Setup of the LFP system [5]

3.2 Reduction of the Laser Speckle Noise of the LFP System by Optimizing Its Laser Power, Camera Exposure, and Camera Gain

The major advantage of the LFP technique compared to the shadow moiré technique is that the LFP can be used to simultaneously measure the warpage of chip packages and PWBs in PWBAs. On the other hand, the LFP is error-prone because of its

noisy fringe image caused by laser speckle [119]. The noise in the fringe image decreases measurement accuracy and repeatability [120]. A comparison of two fringe images, one with and one without laser speckle noise, is shown in Figure 3.2. As the size of the chip packages becomes smaller, the fringe pitch also becomes smaller, and as a result, the laser speckle has an increasing effect on the measurement result.



(a) (b)

Figure 3.2**.** Comparison of fringe images (a) with and (b) without laser speckle noise

The simplest way to decrease the laser speckle is by lowering the laser power, but this method also causes a lower contrast fringe pattern in the images, which affects the quality of measurement. The low contrast in the images can be adjusted by changing the camera exposure and camera gain, but these two parameters not only make the image brighter with more contrast but also add noise. Therefore, it is important to find the optimum balance among the three control parameters to improve the quality characteristic of the LFP system.

The optimum values of the three control parameters were determined by using the Taguchi's DOE method, the ANOVA, and the regression method. The Taguchi's DOE method was used to design the experiments efficiently, and the ANOVA was used to identify the effects of each control parameter on the quality characteristic of the LFP

system. The regression method was used to precisely estimate the optimum values of the control parameters. The steps applied in this study were (1) designing experiments using the Taguchi's DOE method and conducting the experiments, (2) analyzing the experimental results using the ANOVA, (3) obtaining regression equations and determining the optimum values of each parameter from the regression equations, and (4) validating the optimum values with experiments

3.2.1 Measurement Accuracy and Repeatability of the LFP System

Measurement accuracy and repeatability are commonly used to evaluate the quality characteristics of measurement systems [121]. After measuring the relative height between 14 μm and 39 μm step heights of a calibration block (Figure 3.3) ten times, the measurement accuracy and repeatability of the LFP system were quantified by calculating the percentage error (Ɛ) and the standard deviation (σ) of the measurements using the following equations (3.1 and 3.2):

$$\varepsilon = \frac{1}{N}\sum_{i=1}^{N}\frac{|y_i - y|}{|y|} \times 100 \tag{3.1}$$

$$\sigma = \sqrt{\frac{1}{N-1}\sum_{i=1}^{N}(y_i - \bar{y})^2} \tag{3.2}$$

where y = the true height, N = the number of measurements, y_i = the ith measured height, $\bar{y}$ = the average of y_i's, Ɛ = the percentage measurement error of $\bar{y}$, and σ = the standard deviation of y_i's.

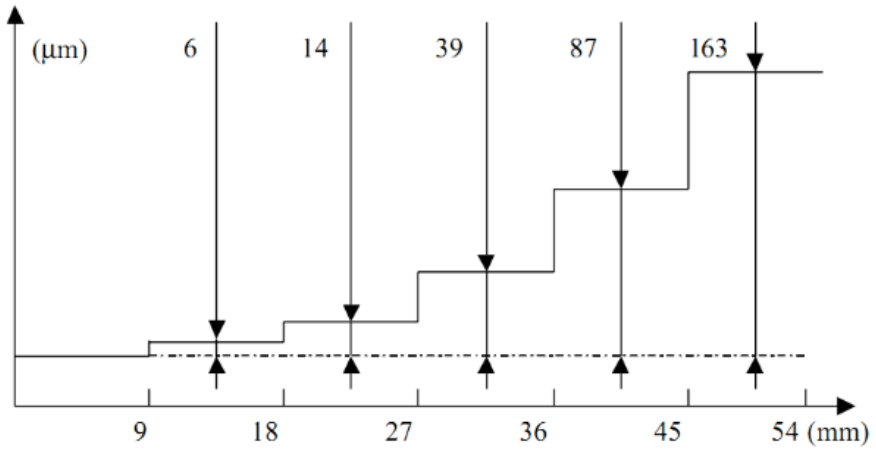


Figure 3.3. The cross section of the calibration block

3.2.2 Design of Experiments and Experimental Results

As the conventional full-factorial way of designing experiments requires many simulation runs, the process is time consuming [122]. For example, four factors, each with three levels, require 3^4 (= 81) experiments. As the number of factors or the number of levels increases, the number of experiments increases dramatically in a full-factorial design. This problem can be solved by the Taguchi's DOE method. It uses an orthogonal array testing strategy to investigate the entire factor space with a minimum number of experimental runs [123]. Because experimenters can save time, effort, and costs efficiently with the Taguchi's DOE method, it is widely used in many engineering optimization problems [124-127].

In order to design experiments to investigate the effects of the control parameters, laser power, camera exposure, and camera gain, the Taguchi's DOE method was used. Three levels of the three control parameters were established as the minimum required for determining the optimum values of each parameter. The range of the laser power is determined based on the results of the pre-trial experiments summarized in Table 3.1. In

this table P, E, and G indicate the laser power, camera exposure, and camera gain, respectively. To estimate the appropriate range of the laser power, the camera exposure is fixed as its maximum value, 30 ms, and the camera gain is fixed as its minimum value, 0 db, as the manufacturer's recommendation. The results show that the percentage error (Ɛ) and the standard deviation (σ) are relatively low when P is between 50 mw and 75 mw.

Table 3.1. The results of the pre-trial experiments

Experiment #	**Control Parameters**			**Measurement Results**	
	P (mw)	**E (ms)**	**G (dB)**	**Ɛ (%)**	**σ (μm)**
1	100.00	30.00	0	11.37	2.23
2	87.50	30.00	0	9.96	1.54
3	75.00	30.00	0	6.47	1.13
4	62.50	30.00	0	6.34	0.82
5	50.00	30.00	0	8.84	1.24
6	37.50	30.00	0	17.70	1.84
7	25.00	30.00	0	16.56	2.34
8	12.50	30.00	0	54.74	3.34

Because higher camera exposure and lower camera gain are recommended to reduce the image noise, the high level of the camera exposure was determined as its maximum value, 30 ms, and the low level of the camera gain was determined as its minimum value, 0 db. Then the low level of the camera exposure and the high level of the camera gain were determined as 18 ms and 2.9 db, respectively, using the calibration function of the control software, HoloFringe-300K. The three levels of each control parameter are summarized in Table 3.2.

Table 3.2. The three levels of each control parameter (P, E, and G)

Level #	P (mw)	E (ms)	G (db)
1 (Low)	50	18	0
2 (Middle)[a]	62.5	24	1.5
3 (High)	75	30	2.9

[a]The average of the low and high levels

To conduct experiments, nine combinations of the three control parameters (P, E, and G) were designed using the Taguchi's DOE method [128], as shown in Table 3.3. For each experiment run, the percentage error (Ɛ) and standard deviation (σ) were obtained as summarized in Table 3.3. For example, Ɛ is 7.74 % when P, E, and G are 50, 18, and 0, respectively.

Table 3.3. The design of experiments and experimental results

Experiment #	Control Parameters			Measurement Results	
	P (mw)	E (ms)	G (dB)	Ɛ (%)	σ (μm)
1	50.00	18.00	0.00	7.74	0.97
2	50.00	24.00	1.50	6.97	0.79
3	50.00	30.00	2.90	9.29	1.13
4	62.50	18.00	1.50	7.33	0.81
5	62.50	24.00	2.90	5.89	0.97
6	62.50	30.00	0.00	7.40	0.85
7	75.00	18.00	2.90	10.17	1.39
8	75.00	24.00	0.00	7.49	1.02
9	75.00	30.00	1.50	10.67	1.31

3.2.3 Analysis of Experimental Results

The ANOVA is a widely used collection of statistical models by which the effect of a specific factor on a system response can be estimated. P-values obtained by ANOVA quantify the significance of the effects of the factors, in which a smaller p-value indicates a more significant effect [122]. Main effect plots can be used to visualize the effects of the factors [122]. The ANOVA was applied to the experimental results (Table 3.3) to estimate the effects of each control parameter on Ɛ and σ. The calculated p-values of each control parameter are shown in Table 3.4. The results show that the order of significance of the control parameters are P, E, and G for Ɛ and P, G, and E for σ.

Table 3.4. The p-values of each control parameter

Control Parameter	**p-values for Ɛ**	**p-values for σ**
Laser Power (P)	0.003	0.066
Camera Exposure (E)	0.004	0.244
Camera Gain (G)	0.021	0.152

Figure 3.4 depicts the main effect plots of each control parameter on Ɛ and σ, respectively. The plots show that the optimum G value is 0 db because Ɛ and σ increase when G value increases. The plots also show that the optimum P and E are located between their first and third levels, respectively.

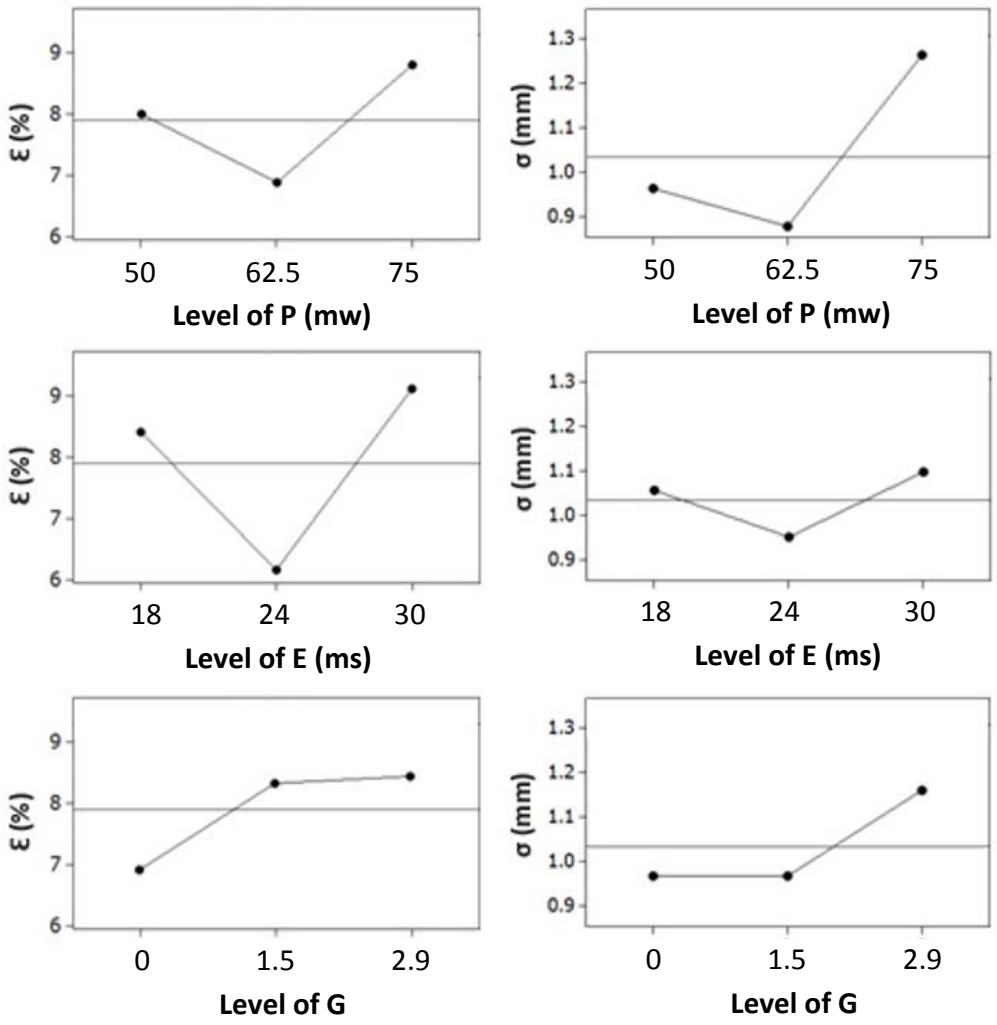


Figure 3.4**.** Main effect plots of each control parameter (P, E, and G) on Ɛ and σ

3.2.4 Determination of the Optimum Values of the Control Parameters

The regression method can be used to find the best-fitting equation with known experimental data [129]. To determine the optimum P and E values, second-order regression equations of Ɛ and σ about P and E were obtained using the regression method. Nine sets of experimental results, summarized in Table 3.5, were used to obtain the regression equations. In these experiments, the G value was fixed at the already determined optimum value, 0 db.

Table 3.5. The experimental results used to obtain the regression equations

Experiment #	Control Parameters			Measurement Results	
	P (mw)	**E (ms)**	**G (db)**	**Ɛ (%)**	**σ (µm)**
1	50	18	0	7.74	0.97
2	50	24	0	6.32	0.84
3	50	30	0	5.46	0.87
4	62.5	18	0	6.76	0.95
5	62.5	24	0	5.48	0.82
6	62.5	30	0	7.40	0.85
7	75	18	0	10.73	1.32
8	75	24	0	7.49	1.02
9	75	30	0	10.67	1.01

Equations 3.3 and 3.4 are the regression equations used to determine the optimum P and E values that minimize Ɛ and σ. Ɛ was minimized when the P and E values were 56 mw and 24 ms, respectively, and σ was minimized when P and E values were 58 mw and 26 ms, respectively. By averaging the P and E values, the optimum P and E values were determined as 57 mw and 25 ms, respectively. The minimized Ɛ and σ calculated by equations 3.3 and 3.4 were 4.98 % and 0.77 µm, respectively.

$$\varepsilon(\mathrm{P},\mathrm{E}) = 75.02888 - 1.270000\mathrm{P} - 2.771944\mathrm{E} + 0.007400\mathrm{PE} + 0.009726\mathrm{P}^2 + 0.047130E^2 \quad (3.3)$$

$$\sigma(\mathrm{P},\mathrm{E}) = 4.455555 - 0.079599\mathrm{P} - 0.105972\mathrm{E} - 0.000700\mathrm{PE} + 0.000843\mathrm{P}^2 + 0.002824E^2. \quad (3.4)$$

3.2.5 Validation of the Optimum Values of the Control Parameters

To validate the minimum Ɛ and σ (4.98 % and 0.77 μm) calculated from the regression equations, the calculations were compared with experimental results, as summarized in Table 3.6. The results show that the errors of the calculated Ɛ and σ are 2.73% and 8.45%, respectively, compared to the experimental results.

Table 3.6. Comparison of Ɛ and σ obtained from the experiments and the regression equations

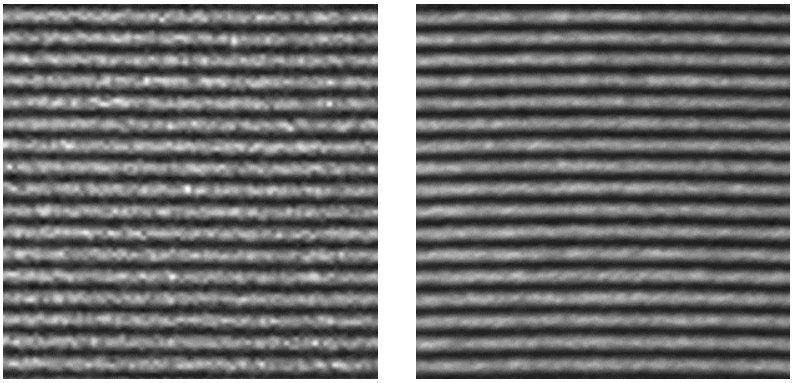
	Measured	**Calculated**	**Error (%)**
Ɛ (%)	5.12	4.98	2.73
σ (μm)	0.71	0.77	8.45

Finally, Ɛs and σs before and after the optimization were compared, as summarized in Table 3.7. The results show that the Ɛ and σ are improved by 26.54 % and 10.13 %, respectively, by the optimization. Figure 3.5 shows the comparison of the fringe images before and after the optimization and indicates that laser speckle noise is significantly reduced by the optimization.

Table 3.7. Comparison of Ɛ and σ before and after optimization

	Before[b]	**After**[c]	**Improvement (%)**
Ɛ[a] **(%)**	6.97	5.12	**26.54**
σ[a] **(μm)**	0.79	0.71	**10.13**

[a]Lower Ɛ and σ mean better accuracy and repeatability, respectively. [b]When P, E, and G were 60 mw, 30 ms, and 1 db, respectively. [c]When P, E, and G were 57 mw, 25 ms, and 0 db, respectively.



(a) (b)

Figure 3.5. The fringe images (a) before and (b) after the optimization

3.3 Region Growing Method for Chip Package Segmentation

When measuring a PWBA, the LFP system generates a PWBA displacement image. To simultaneously measure the separate warpage of chip package(s) and the PWB in the PWBA, the chip package and PWB regions in the PWBA displacement image needs to be segmented. To do this automatically, Powell and Ume developed the mask image and active contour models [81]. Table 3.8 summarizes the features of these models. With regard to practical processing time, even though the mask image model is faster than the active contour model, the mask image model still requires a high

processing time. Because of the limitations presented by the current segmentation methods, a faster segmentation method, the RGM, was developed in this study.

Table 3.8. Comparison of two automated segmentation methods [81]

Segmentation Method	**Active Contour Model**	**Mask Image Model**
Resolution	High	High
Multiple Package Measurement	Suitable	Suitable
Package Location	Not Needed	Not Needed
Variability	Good	Good
Digital Image Processing	Complex	Complex
Calculation	Complex	Moderate
Practical Processing Time[a]	8.59 (1 package) 9.84 (2 packages)	4.72 (1 package) 5.01 (2 packages)

[a]Practical processing time for segmenting one or two chip package. The test conditions: 1.8 GHz CPU, 640 MB memory, and single core processor.

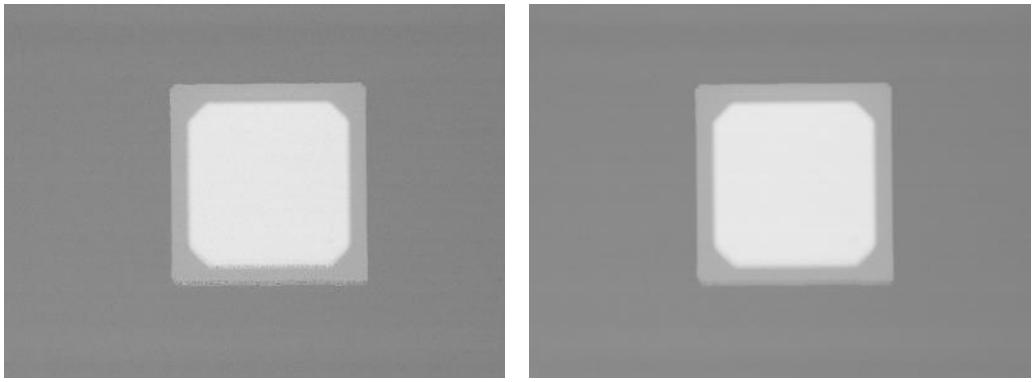
In the RGM, the chip package and PWB regions in the PWBA displacement image are segmented by the following steps: (1) smoothen the PWBA displacement image using the Gaussian filter, (2) segment the regions in the smoothened displacement image using the region-growing algorithm, and (3) detect the chip package and PWB regions in the segmented region image using geometric analysis. The details of each step are provided below.

Step 1: Smoothen the PWBA image using the Gaussian filter.

The PWBA displacement image is smoothened by calculating the weighted average intensity using a two-dimensional (2-D) Gaussian function [130]. Since the image is stored as a collection of discrete pixels, a Gaussian kernel, which is a discrete approximation of the Gaussian function, is convolved onto the image to smoothen it [130]. In this study, the 5×5 Gaussian kernel shown in Figure 3.6 was used, and sample images before and after convolving the Gaussian kernel on an unpainted PWBA image are shown in Figure 3.7.

$$G_{5\times5} = \frac{1}{159}\begin{bmatrix} 2 & 4 & 5 & 4 & 2 \\ 4 & 9 & 12 & 9 & 4 \\ 5 & 12 & 15 & 12 & 5 \\ 4 & 9 & 12 & 9 & 4 \\ 2 & 4 & 5 & 4 & 2 \end{bmatrix}$$

Figure 3.6. The 5×5 Gaussian kernel



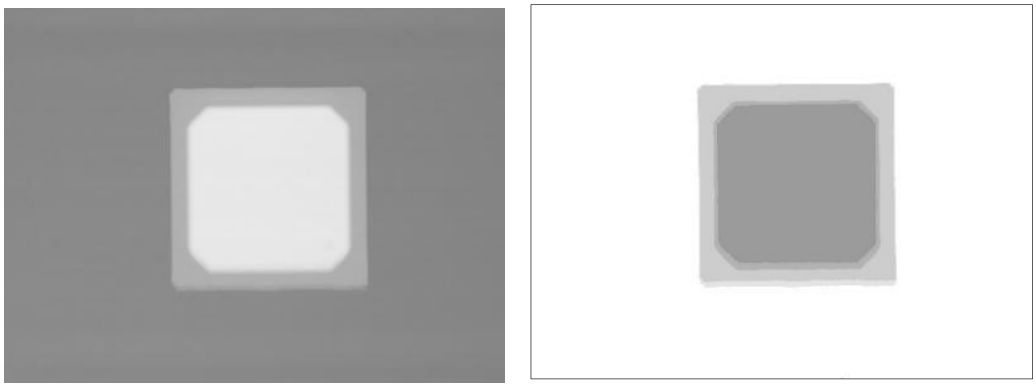
(a) (b)

Figure 3.7**.** PWBA displacement images (a) before and (b) after the Gaussian filtering

Step 2: Segment the regions in the smoothened displacement image using the region-growing algorithm.

The region-growing algorithm [131] is a process of joining adjacent pixels of similar intensities in regions, a widely used process for region-based image segmentation

[132]. The region-growing algorithm is applied to the smoothened PWBA displacement image in order to label each region in the displacement image. Figure 3.8 shows the displacement image and the label image of the PWBA obtained after the region-growing algorithm was applied to the displacement image. In the label image, different gray levels are assigned for each region, as depicted on the figure.

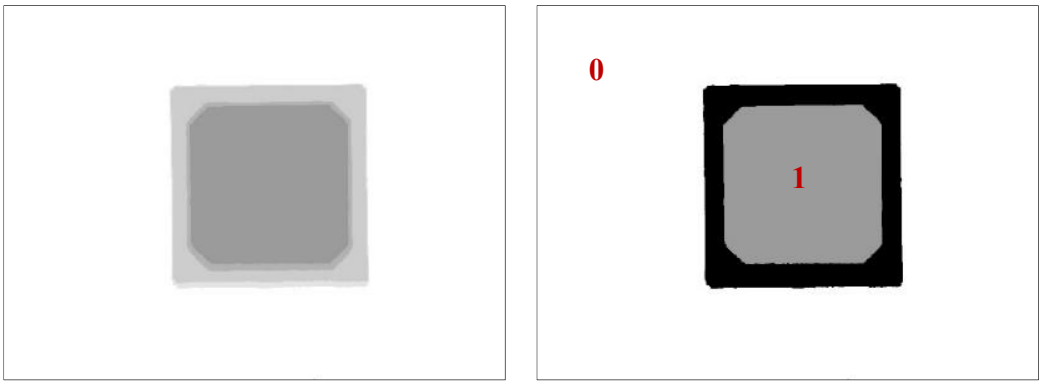


(a) (b)

Figure 3.8**.** (a) Smoothened PWBA displacement image and (b) label image obtained after the region-growing algorithm is applied to (a)

Step 3: Detect the chip package and PWB regions in the segmented region image using geometric analysis.

To detect the chip package and PWB regions among the regions segmented in step 2, a geometric analysis is performed. By the geometric analysis, the largest region is recognized as the PWB region. Any region that does not encompass another region is recognized as the chip package region. Figure 3.9 depicts the results of detecting the chip package and PWB regions from the label image using the geometric analysis. The PWB region is marked with "0," the chip package regions are marked with "1," and the substrate region is masked-out (in black).

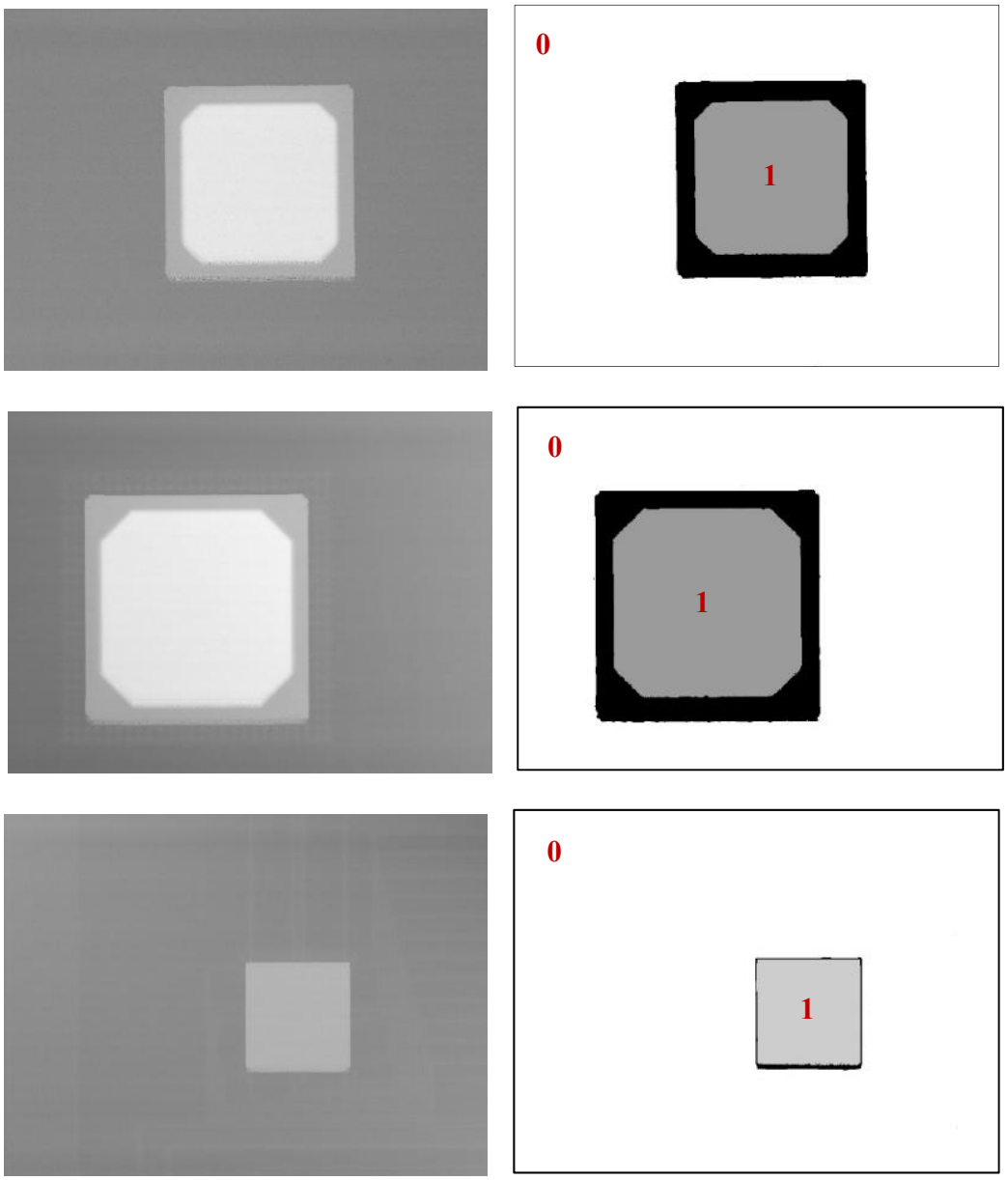


(a) (b)

Figure 3.9. (a) Label image of the PWBA and (b) detected chip package and PWB regions after the geometric analysis is applied to (a)

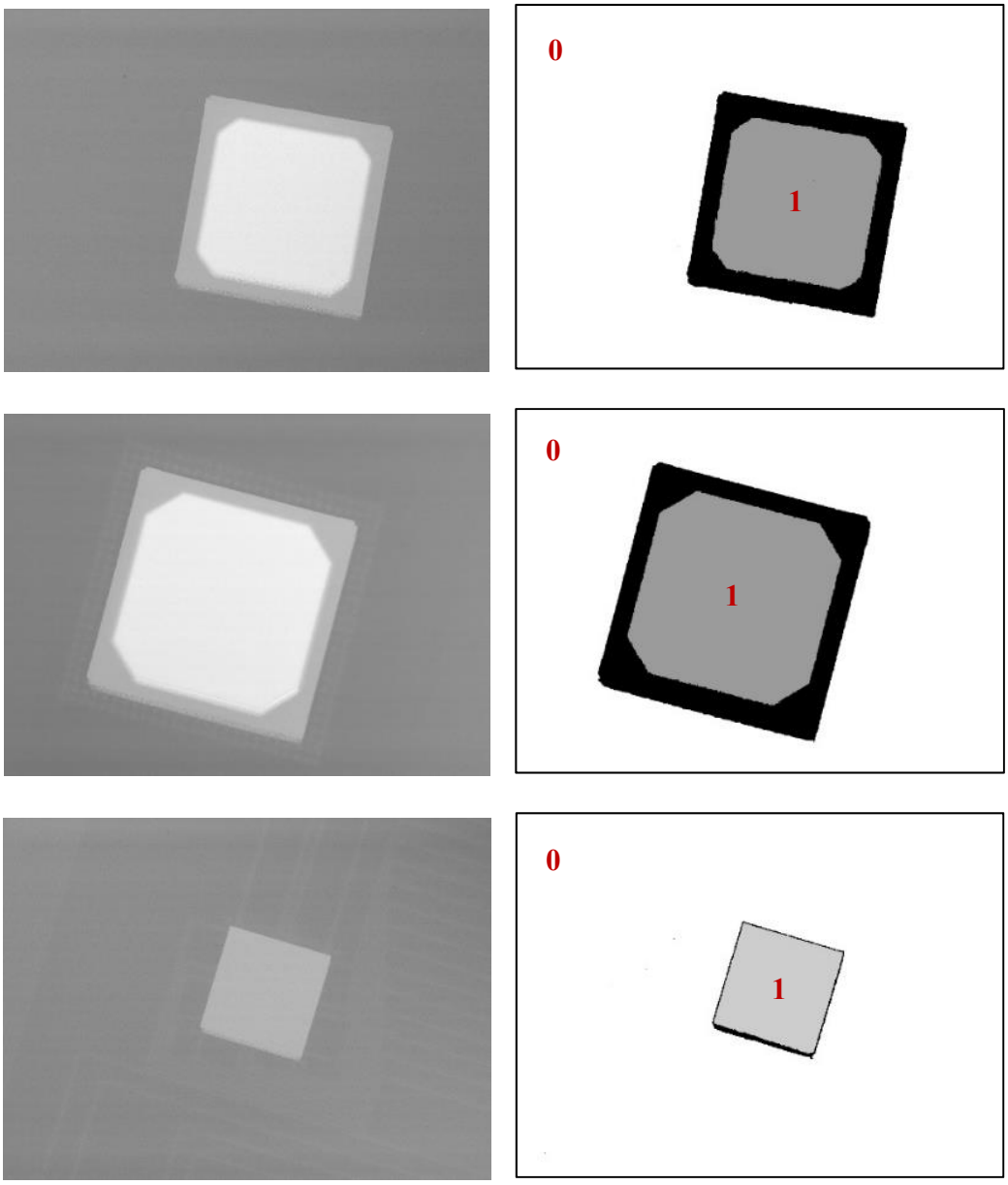
Validation of the RGM

Using the RGM to test the segmentation of the chip package and PWB regions in PWBA displacement images, three different PWBAs were used. Figure 3.10 and 3.11 show their PWBA displacement images and the resulting segmentation images produced by the RGM. The detected PWB and chip package regions are marked with "0" and "1," respectively. The sizes of the chip packages shown in the unpainted PWBA images are 23×23 mm, 27×27 mm, and 10×10 mm, respectively.



(a) (b)

Figure 3.10**.** (a) PWBA displacement images and (b) resulting segmentation images



(a) (b)

Figure 3.11. (a) PWBA displacement images (rotated) and (b) resulting segmentation images

The processing times of the RGM and the mask image model are compared in Table 3.9, which show that the RGM is 43.6 % or 40.2 % faster than the mask image model for segmenting one or two package, respectively.

Table 3.9. Comparison of the processing times of the mask image model and the RGM

Number of Packages	Processing Time (s)		Difference (%)
	Mask Image Model	RGM	
1	0.94	0.53	43.61%
2	1.02	0.61	40.20%

Test conditions: 3.3 GHz CPU, 8GB memory, and single core processor

3.4 Chapter Summary

The measurement accuracy, repeatability, and speed of the LFP system were improved by reducing its laser speckle noise and post-processing time. In order to reduce the laser speckle noise of the LFP system, the noise control parameters were optimized by using the full-factorial DOE method, the ANOVA, and the regression method. The optimum values of the laser power, camera exposure, and camera gain were determined to be 57 mw, 25 ms, and 0 db, respectively. The optimization improved the measurement accuracy and repeatability of the LFP system by 26.5 % and 10.1 %, respectively. In order to reduce the post-processing time of the LFP system, a fast package segmentation method, the RGM, was developed. The RGM segmented the chip package and PWB regions in PWBA displacement images. Experimental results showed that the RGM is 43.6 % or 40.2 % faster than the current automatic segmentation method, the mask image model, for segmenting one or two packages, respectively.

CHAPTER 4

DEVELOPMENT OF A DFP SYSTEM FOR MEASURING THE WARPAGE OF PAINTED AND UNPAINTED CHIP PACKAGES AND BOARDS

Compared to the LFP technique, the DFP technique has the major advantage of not producing laser speckle because it uses a digital projector instead of a laser interferometer. However, the DFP technique injects a different source of error, the gamma nonlinearity of the digital projector. A DFP system for measuring the warpage of chip packages and boards was developed. The measurement capabilities and experimental results obtained by using the LFP and DFP systems were compared.

Similar to the shadow moiré and LFP techniques, the DFP technique requires reflective painting, which is generally sprayed on the sample surface to ensure uniform surface reflectance and to obtain better fringe image contrasts in the measurement process. However, painted samples may not be reused, and the spray-painting process is not suitable for the assembly line. To solve this problem, this study developed a new DDFP technique for measuring the warpage of unpainted chip packages and boards.

4.1 Development of a Digital Fringe Projection System

The major disadvantage of the LFP is its noisy fringe pattern caused by laser speckle [13]. Even though the laser speckle noise inherent in the LFP system was reduced by optimizing the control parameters discussed in the previous chapter, the remaining laser speckle noise still affected the measurement accuracy and repeatability. The DFP

can overcome this disadvantage by using a digital projector to generate the fringe patterns instead of a laser interferometer. However, the DFP has different source of error in the form of gamma nonlinearity [14], which represents the nonlinear relationship between the input and output grayscale levels of the digital projector. Table 4.1 compares the features of the three moiré techniques. In this study, a DFP system was developed for measuring the warpage of chip packages and boards more accurately than the LFP system.

Table 4.1. Comparison of the features of the LFP and DFP techniques

Feature	**LFP**	**DFP**
Fringe Generating Method	Laser Interferometer	Digital Projector
Light Source	Coherent Light (Laser)	White Light (Light-Emitting Diode)
Phase-Shifting Method	Mechanical Shift Using Piezoelectric Transducer	Digital Shift
Image Processing	Complex	Very Complex
Major Image Error Source	Laser Speckle	Gamma Nonlinearity of Digital Projector
Ability to Measure PWBA	High	High

4.1.1 DFP System Configuration

The setup of the DFP system developed in this study is illustrated in Figure 4.1. A fringe pattern is generated by a computer and projected through a digital projector onto the sample surface. The image of the projected fringe pattern in its 60×45 mm FOV is

captured by a CCD camera. The same processing algorithms used for the LFP system are used for the DFP system. The four-step phase-shifting method [40] is used for phase wrapping to increase the measurement resolution [133], and the mask-cut algorithm [104, 107] is used for phase unwrapping. The reference-subtraction and the linear conversion methods [14, 118] are used to convert the unwrapped phase to a displacement image that contains the height distribution of the sample surface. The theoretical out-of-plane resolution of the DFP system can be calculated using equation 2.1, above. For the calculation, the values of P, α, β, and C of the DFP system are 0.6 mm, 0º, 45º, and 256, respectively. The theoretical resolution of the DFP system is 2.34 μm.

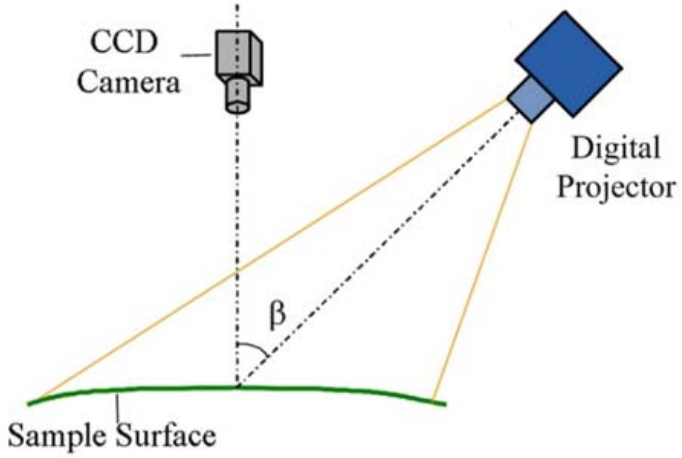


Figure 4.1 Setup of the DFP System

4.1.2 Customized Software of the DFP System

The DFP system includes customized software written in the C++ programming language. All the processing algorithms, such as the phase wrapping and unwrapping algorithms are implemented in the software, which controls the camera to capture images and the projector to project and shift fringe patterns. The user interface of the software is

shown in Figure 4.2. Camera-captured or processed images are displayed on the display panel and the user buttons are located on the control panel.

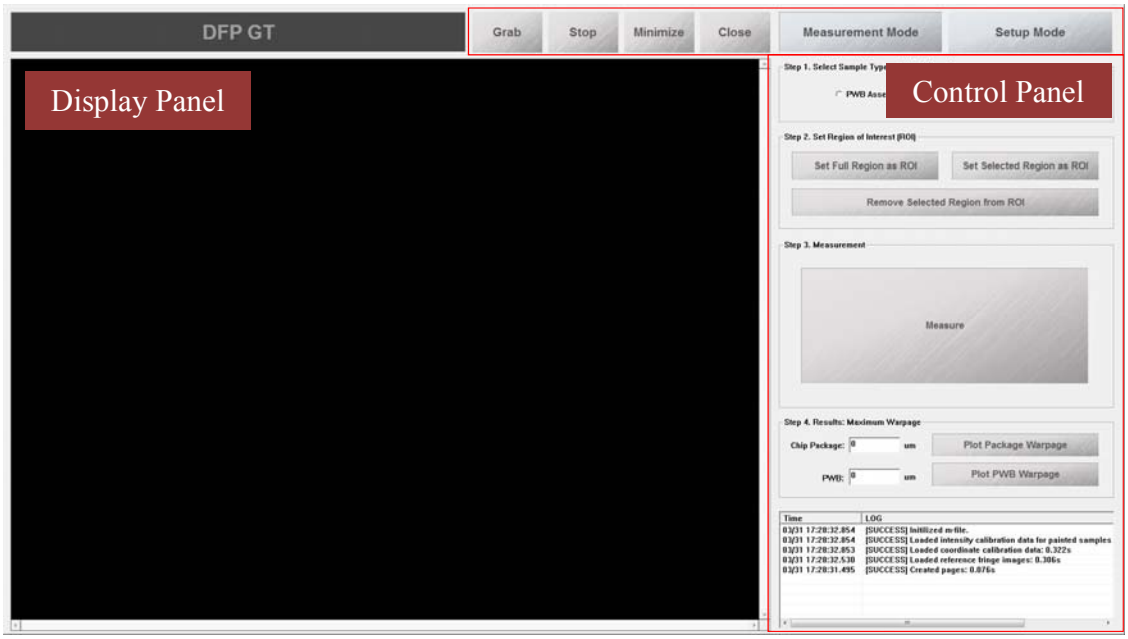


Figure 4.2. The user interface of the customized software

4.1.3 Intensity Calibration of the DFP System

As described in Chapter 2.2, the relationship between computer input intensity (I_I) and capture intensity (I_C) is generally nonlinear due primarily to the gamma nonlinearity of the digital projector, which decreases the measurement accuracy and repeatability of the DFP system [14]. Figure 4.3 illustrates this nonlinearity when the sample is a painted chip package or board. In this case, the average absolute error between I_I and I_C is 19.95.

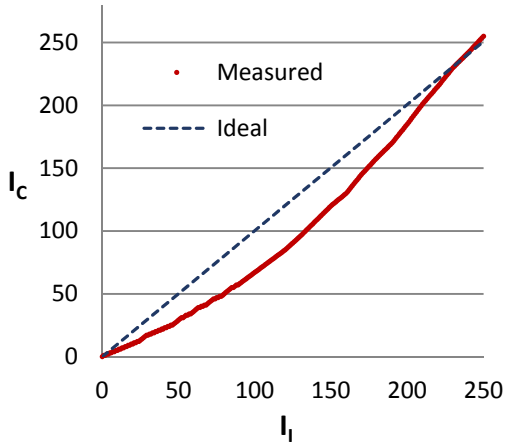


Figure 4.3. Relationship between I_I and I_C when the sample is a painted chip package or board

To calibrate the nonlinearity, the lookup table method [109] was used, which involves storing experimentally measured 255 I_C values and corresponding I_I values that can be used to modify input intensity in order to compensate for the nonlinearity. As shown in Figure 4.4, after the calibration of intensity, the nonlinearity significantly declined. In this case, the average absolute error between I_I and I_C is 3.93.

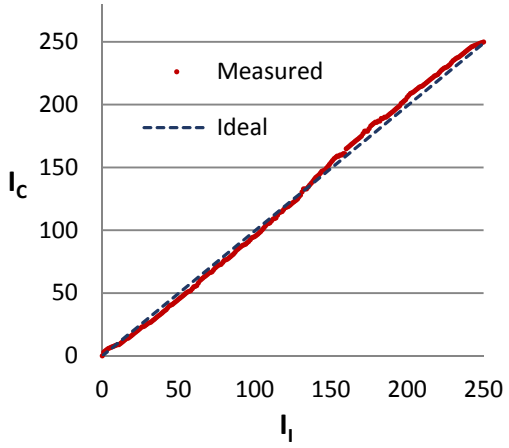


Figure 4.4. Relationship between I_I and I_C after the intensity calibration when the sample is a painted chip package or board

4.1.4 Validation of the DFP System

A calibration block with five steps (6, 14, 39, 87, and 163 μm) was used to validate the DFP system developed in this study. Using the DFP system, each step of the calibration block was measured ten times. The averages ($\bar{y}$), the percentage errors (Ɛ), and the standard deviations (σ) of the ten measurements are summarized in Table 4.2.

Table 4.2. The measurement results obtained using the calibration block

Step Height (μm)	**6**	**14**	**39**	**87**	**163**
$\bar{y}$ **(μm)**	6.45	14.84	37.65	85.18	162.12
Ɛ[a] (%)	7.57	6.02	3.46	2.09	0.54
σ[b] (μm)	0.37	0.40	0.59	0.69	0.50

[a]Calculated using equation 3.1, [b]Calculated using equation 3.2

From the results provided in Table 4.2, the measurement accuracy and repeatability were quantified as 3.94 % and 0.52 μm, respectively, by the mean percentage error ($\bar{\varepsilon}$) [134] and the pooled standard deviation (σ_p) [135] as provided in the following equations (4.1 and 4.2):

$$\bar{\varepsilon} = \frac{1}{M}\sum_{j=1}^{M} \varepsilon_j \tag{4.1}$$

$$\sigma_p = \sqrt{\frac{\sum_{j=1}^{M}(N_j - 1)\sigma_j^2}{\sum_{j=1}^{M}(N_j - 1)}} \tag{4.2}$$

where M = the number of steps of the calibration block, N_j = the number of measurements for the jth step of the calibration block, ε_j = the percentage error for measuring the jth step, σ_j = the standard deviation for measuring the jth step.

4.2 Experimental Comparison of the LFP and DFP Systems

The advantages and disadvantages of the LFP and the DFP systems were compared using experimental results. The qualities of the fringe images, practical measurement resolutions, accuracy, repeatability, and speeds of the LFP and DFP systems were compared. The results of warpage measurements using a PWBA were also compared.

4.2.1 Quality of the Fringe Images

Noise and the presence of non-ideal sinusoidal waveforms in the recorded fringe images cause measurement errors [14] and thus degrade the measurement resolution and accuracy. The noise and the non-ideal sinusoidal waveforms of a fringe image are quantified by calculating the mean square error (MSE) [136] between the recorded fringe image and an ideal sinusoidal fringe image. The lower MSE value indicates that fewer non-ideal sinusoidal waveforms are present in the recorded fringe images. To reduce noise in the recorded fringe images, median, blur, or despeckle filter [137] was applied to the recorded fringe image. The MSEs of each of the recorded fringe image including the filtered fringe images were calculated as shown in Figure 4.5. The minimum MSE yielded by the LFP is 936 when a median filter is applied and the minimum MSE yielded by the DFP is 512 when none of the filters is applied. The results show that the fringe images of the LFP contain more noise and non-ideal sinusoidal waveforms than those of the DFP.

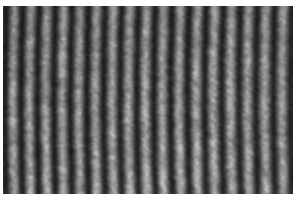
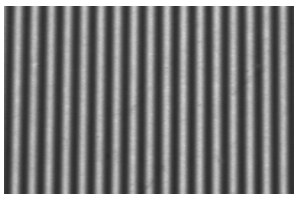
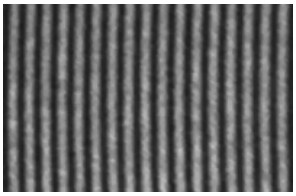
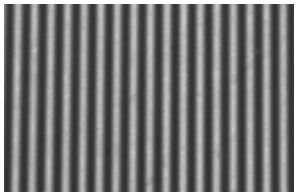
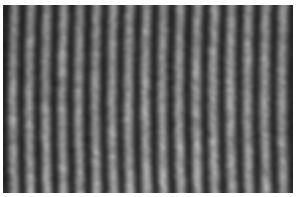
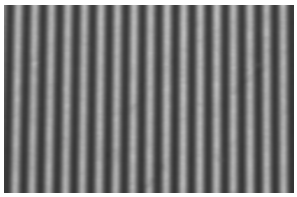
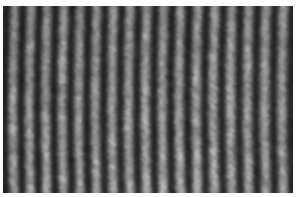
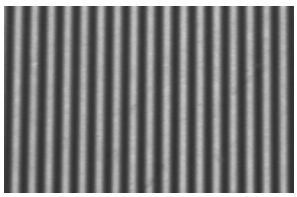
Filter	LFP	DFP
Unfiltered	 (MSE=1231)	 (MSE=512)
Filtered by Median	 (MSE=936)	 (MSE=624)
Filtered by Blur	 (MSE=1058)	 (MSE=775)
Filtered by Despeckle	 (MSE=1128)	 (MSE=572)

Figure 4.5. Recorded fringe images (unfiltered and filtered) and their MSEs

4.2.2 Practical Measurement Resolution, Accuracy, and Repeatability

A calibration block with five steps (6, 14, 39, 87, and 163 μm) was used to evaluate and compare the practical measurement resolution, accuracy, and repeatability of the LFP and DFP systems. Each step of the calibration block was measured ten times using the LFP and DFP systems. The averages ($\bar{y}$), the percentage errors (Ɛ), and the standard deviations (σ) of the ten measurements are summarized in Table 4.3. From these

results, the measurement accuracy and repeatability of the LFP and DFP systems were quantified by the mean percentage error ($\bar{\varepsilon}$) (equation 4.1) and the pooled standard deviation (σ) (equation 4.2), as summarized in Table 4.4. The results provided in Table 4.3 and 4.4 show that the DFP system has better practical resolution, accuracy, and repeatability than the LFP system.

Table 4.3. Comparison of the measurement results obtained using the calibration block

Step Height (µm)		**6**	**14**	**39**	**87**	**163**
LFP	$\bar{y}$ **(µm)**	5.31	15.42	35.71	79.19	175.24
	Ɛ[a] (%)	11.45	10.14	8.44	8.98	7.51
	σ[b] (µm)	0.86	1.79	2.12	2.31	5.22
DFP	$\bar{y}$ **(µm)**	6.45	14.84	37.65	85.18	162.12
	Ɛ[a] (%)	7.57	6.02	3.46	2.09	0.54
	σ[b] (µm)	0.37	0.40	0.59	0.69	0.50

[a]Calculated using equation 3.1, [b]Calculated using equation 3.2

Table 4.4. Comparison of the accuracy and repeatability

System	$\bar{\varepsilon}$**[a] (%)**	σ_p**[b] (µm)**
LFP	9.30	2.46
DFP	3.94	0.52

[a]Lower value indicates better accuracy, [b]Lower value indicates better repeatability

4.2.3 Measurement Speed

Another important factor in the comparison of the LFP and DFP systems is measurement speed. The sums of the data acquisition and processing times used to obtain the warpage of a sample using the LFP and DFP systems, respectively, represent their

measurement speeds. The definitions of the data acquisition and processing times of the LFP and DFP systems are summarized in Table 4.5.

Table 4.5. Definition of the data acquisition and processing times of the LFP and DFP systems

Item	**Definition**
Data acquisition time of the LFP and DFP systems	Time to capture and save four fringe images from the sample (including phase-shifting time)
Data processing time of the LFP system	Time to generate surface profile data from the fringe images (including phase wrapping, phase unwrapping, and filtering)
Data processing time of the DFP system	Time to generate the sinusoidal fringe pattern + time to generate surface profile data from the fringe images (including phase wrapping, phase unwrapping, and filtering)

Table 4.6 shows the actual data acquisition times of the LFP and DFP systems for measuring the warpage of a sample. The results show that both systems require similar times for data acquisition. Even though the LFP system employs mechanical shifting using a PZT, it only slightly affects the measurement speed because the PZT is very fast. The DFP system, however, requires more data processing time mainly because of the additional processing time required by the system to generate the fringe pattern.

Table 4.6. Comparison of the practical data acquisition and processing times of the LFP and DFP systems

System	**Data Acquisition Time (s)**	**Data Processing Time (s)**
LFP	1.8	1.9
DFP	1.7	2.8

Test conditions: 3.3 GHz CPU, 8GB memory, single core processor

4.2.4 Measurement of PWBA Warpage

To compare the warpage measurement capabilities of the LFP and DFP systems, a PWB and a PBGA package, shown in Figure 4.6, were used. The size and thickness of the three-layer PWB were 200×140 mm and 1.5 mm, respectively and the size of the PBGA package was 23×23 mm. The warpage of the PBGA package and the PWB region (60×45 mm) were separately measured using as the reference a contact profilometer with a resolution of less than 0.1 μm. Red masking tape was placed on the PWB to ensure consistency of the FOVs in all measurements and adhesive was used to attach the PBGA package to the PWB to simulate a PWBA. Then, using the LFP and DFP systems, the warpage of the PBGA package and the PWB in the PWBA region (60×45 mm) were simultaneously measured, as shown in Figure 4.7 and 4.8. The results of the warpage measurements are compared in Table 4.7, which shows that the results of DFP are closer to those of the contact profilometer (used here as the "gold standard") than those of LFP.

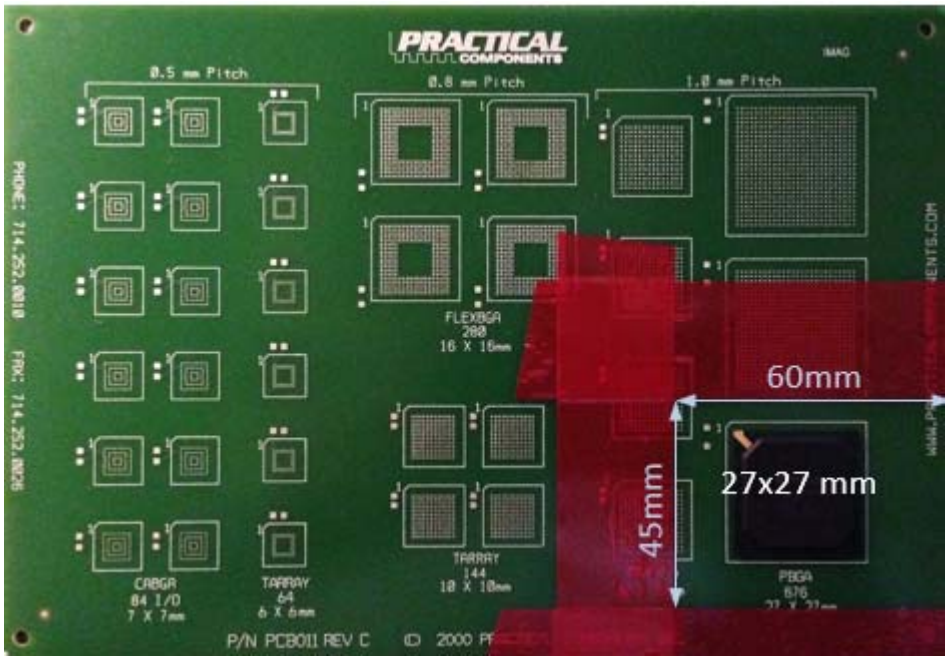
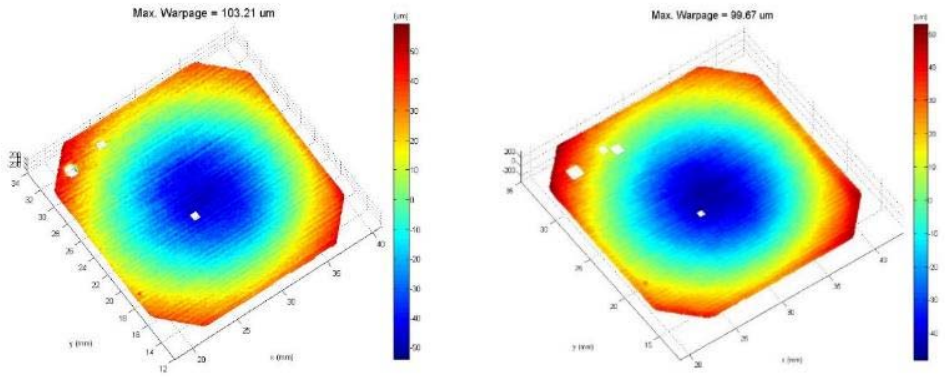
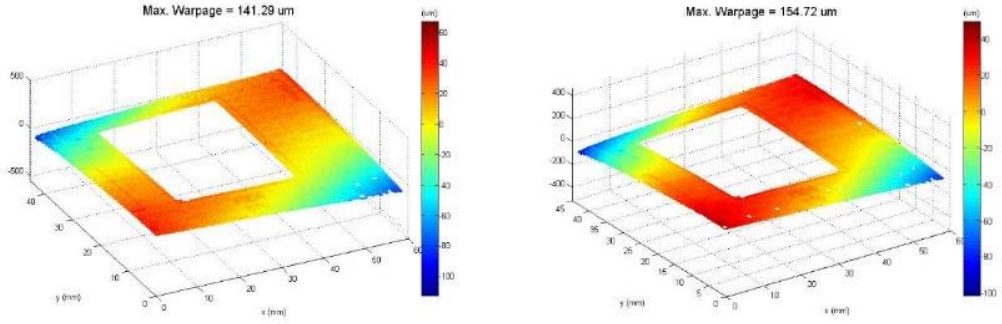


Figure 4.6. A PWBA with one PBGA package



(a) (b)

Figure 4.7. Warpage of the PBGA package obtained with (a) LFP and (b) DFP systems



(a) (b)

Figure 4.8. Warpage of the PWB obtained with (a) LFP and (b) DFP systems

Table 4.7. Comparison of the warpage measurement results

System	PBGA		PWB	
	W_{max} (µm)	Ɛ (%)	W_{max} (µm)	Ɛ (%)
CP	94.51	-	150.18	-
LFP[a]	105.93	11.36	138.70	8.29
DFP[a]	100.05	5.87	153.78	2.40

CP: contact profilometer, W_{max}: maximum warpage, Ɛ: percentage error compared to the CP results. [a]A W_{max} value is the average of three measurements.

4.3 Dynamic Digital Fringe Projection Technique for Measuring the Warpage of Unpainted Chip Packages and Boards

The use of the moiré techniques in the measurement process generally requires spraying the sample surface with reflective paint in order to ensure uniform surface reflectance and better fringe image contrast. Painted samples, however, may not be reused, and the spray-painting process is not suitable for use in the assembly line. When an unpainted PWBA containing a PBGA package is measured using the DFP technique, variances in surface reflectance between the PBGA package and the PWB generally result in either too dark or too bright regions in the PWBA fringe image. For example, when a dark fringe pattern (Figure 4.9 (a)) is projected onto the PWBA, the PWB region of the PWBA fringe image (Figure 4.9 (b)) is too dark for processing. In contrast, when a bright and uniform fringe pattern (Figure 4.9 (c)) is projected onto the PWBA, the package region of the PWBA fringe image (Figure 4.9 (d)) is too bright for processing. This problem can be solved by projecting a fringe pattern containing varying intensities, shown in Figure 4.9 (e), in order to obtain a fringe image with improved fringe image contrast as shown in Figure 4.9 (f).

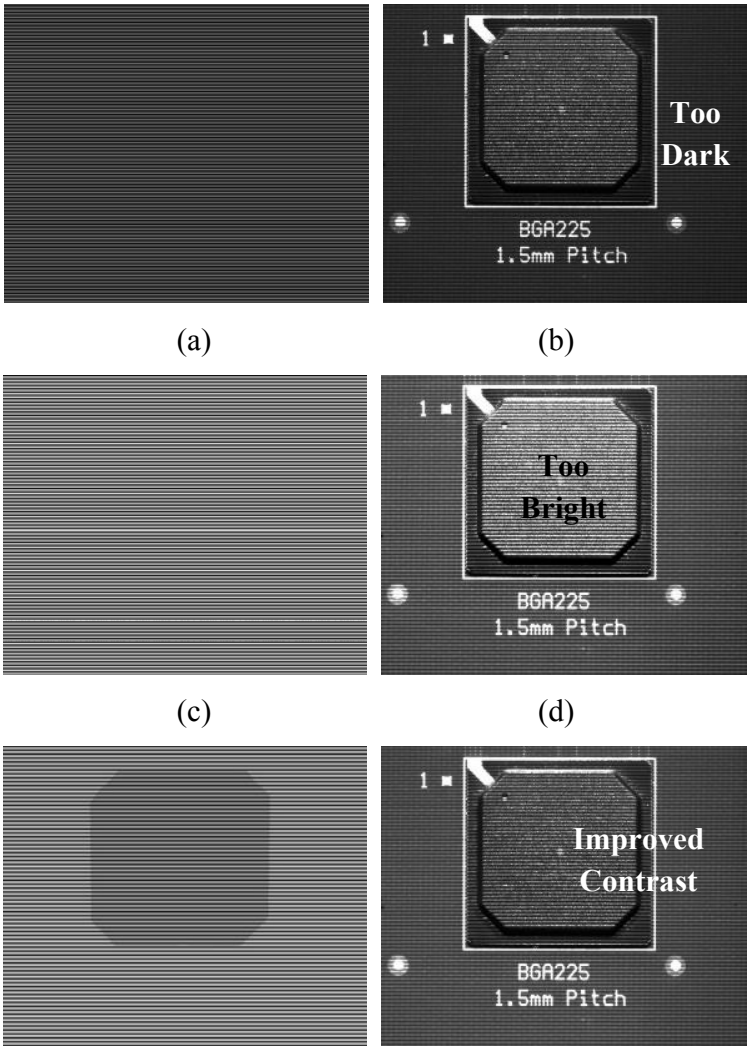


Figure 4.9. (a) A dark fringe pattern, (b) a PWBA fringe image illuminated by (a), (c) a bright fringe pattern, (d) a PWBA fringe image illuminated by (c), (e) a dynamic fringe pattern, and (f) a PWBA fringe image illuminated by (e)

To measure the warpage of unpainted PBGA packages and boards, a DDFP technique was developed. The DDFP technique generates and projects a dynamic fringe pattern, in which proper fringe intensity distributions are dynamically determined based on the coordinates and the surface reflectance of PBGA packages and PWBs.

DDFP incorporates the DFP technique's process [138] for measuring the warpage of painted chip packages and boards. The steps of the process are (1) to generate and project a sinusoidal fringe pattern onto a sample surface [97], (2) to obtain four-step phase-shifted fringe images reflected from the sample surface [40], (3) to apply the four-step phase-shifting method to the captured fringe images to obtain a wrapped phase image [40], (4) to apply the mask-cut phase unwrapping algorithm to the wrapped phase image to obtain an unwrapped phase image [104, 107], (5) to convert the unwrapped phase image to a displacement image that contains the surface height distribution using the reference-subtraction and the linear conversion methods [14, 118], and (6) to obtain the warpage of the sample from the displacement image [138].

In addition to incorporating the process of the DFP technique, the DDFP technique includes an automatic method for segmenting the PBGA package and PWB regions in an unpainted PWBA image, together with calibration methods that compensate for the mismatches in coordinates and intensities between the projected and captured images. Because coordinate calibration is independent of sample changes, it needs to be performed only once after the system is set up. After the segmentation and the calibrations are performed, the DDFP technique generates a dynamic fringe pattern and projects it onto the unpainted PWBA. Figure 4.10 presents the flowchart depicting the process of the DDFP technique, and the remainder of this chapter details the first four steps of the process, which differ from those of the DFP technique. The DDFP technique was implemented in the customized software of the DFP system and its operation guide is provided at http://dfp.comli.com.

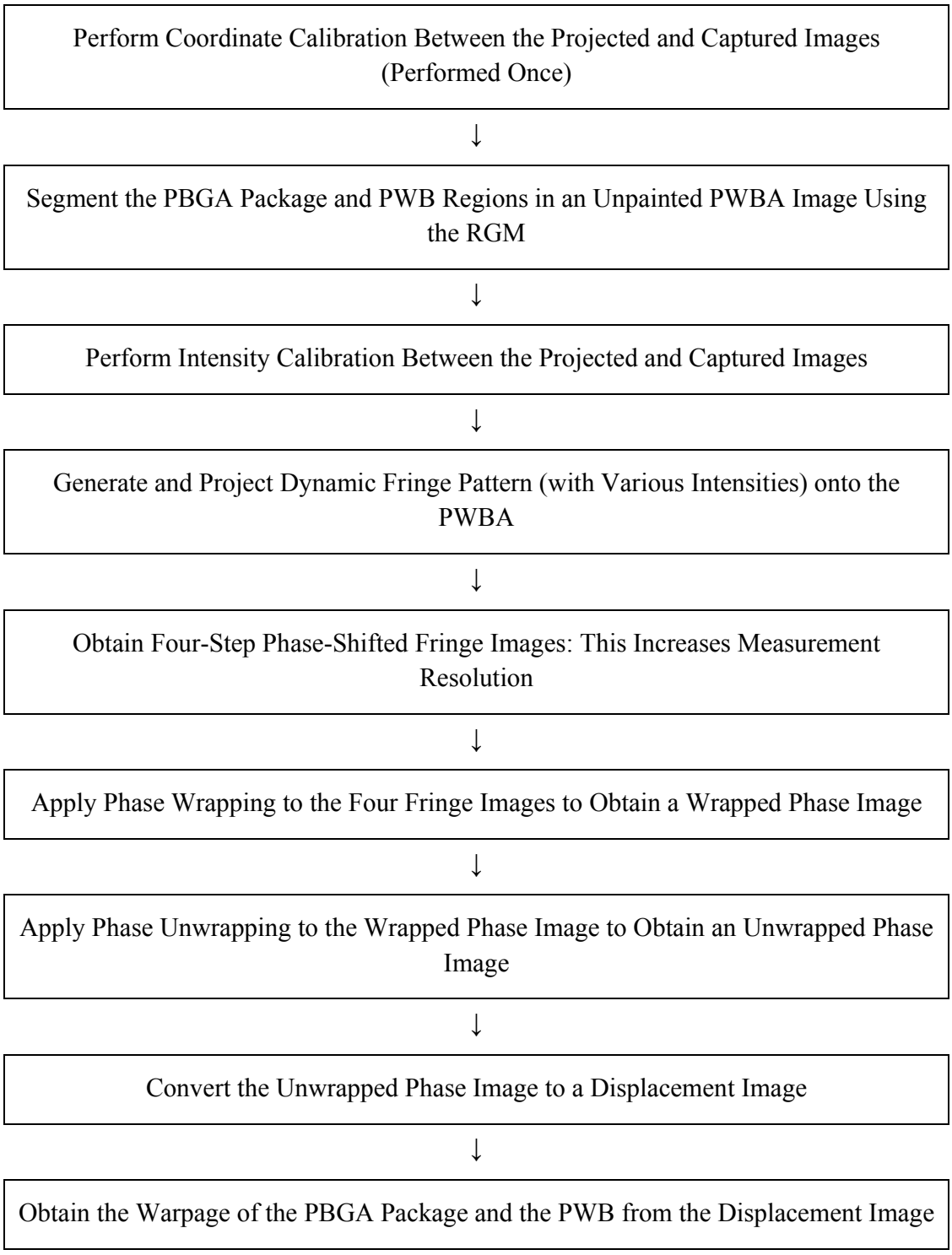
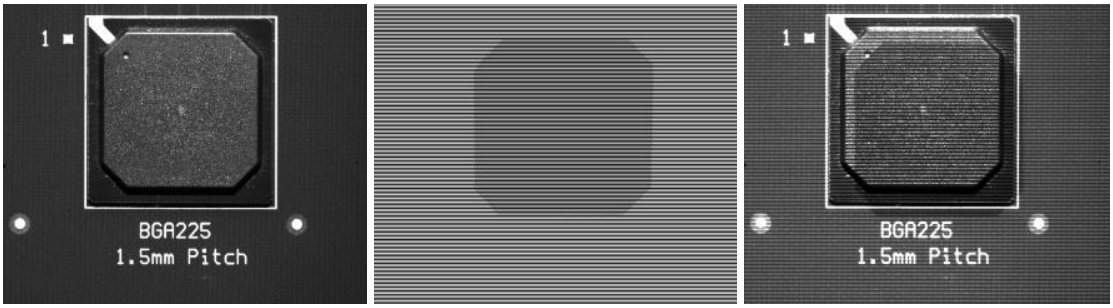


Figure 4.10. Flowchart of the implementation process of the DDFP technique

4.3.1 Coordinate Calibration Between Projected and Captured Images

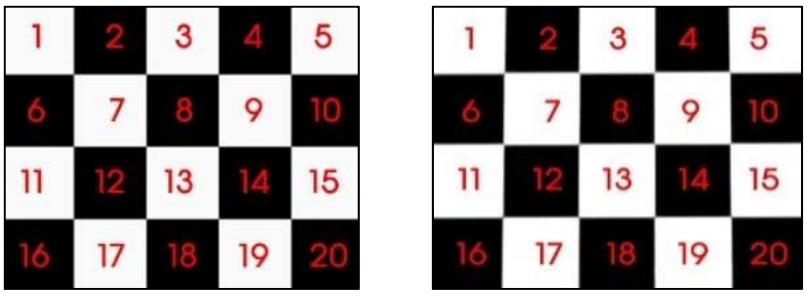
The coordinates of projected and captured images differ; that is, the FOVs of the projector and the camera do not perfectly match, causing misalignment of the projected dynamic fringe pattern, as shown in Figure 4.11 (c).



(a) (b) (c)

Figure 4.11. (a) A PWBA image, (b) a dynamic fringe pattern generated based on the chip package coordinates in (a), and (c) a PWBA fringe image illuminated by (b)

To calibrate the coordinate mismatches, coordinate transfer functions (CTFs) were obtained using a checkered pattern [139] and projector-camera homography [140]. A checkered pattern with n×m squares was generated, projected, and captured, which, in turn, divided the projected and captured images into n×m divisions, shown in Figure 4.12.



(a) (b)

Figure 4.12. Square divisions in the (a) projected and (b) captured images when a 5×4 checkered pattern is used

The CTF for the ith division is provided in equation 4.3 [140], in which $T_{i,j}$ is calculated by the eigenvector corresponding to the smallest eigenvalue of A^TA and A is given in equation 4.4 [140], as shown by

$$X_i(x_i, y_i) = \frac{T_{i1}x_i + T_{i2}y_i + T_{i3}}{T_{i7}x_i + T_{i8}y_i + T_{i9}} \qquad Y_i(x_i, y_i) = \frac{T_{i4}x_i + T_{i5}y_i + T_{i6}}{T_{i7}x_i + T_{i8}y_i + T_{i9}} \tag{4.3}$$

where (X_i,Y_i) = coordinates in the ith division of the projected image, (x_i,y_i) = coordinates in the ith division of the captured image, and $T_{i,j}$ = transformation coefficients for the ith division. Equation 4.4 is as follows:

$$A = \begin{pmatrix} x_{i1} & y_{i1} & 1 & 0 & 0 & 0 & -X_{i1}x_{i1} & -Y_{i1}x_{i1} & -X_{i1} \\ 0 & 0 & 0 & x_{i1} & y_{i1} & 1 & -X_{i1}y_{i1} & -Y_{i1}y_{i1} & -Y_{i1} \\ \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots & \vdots \\ x_{i4} & y_{i4} & 1 & 0 & 0 & 0 & -X_{i4}x_{i4} & -Y_{i4}y_{i4} & -X_{i4} \\ 0 & 0 & 0 & x_4 & y_4 & 1 & -X_{i4}y_{i4} & -Y_{i4}y_{i4} & -Y_{i4} \end{pmatrix} \tag{4.4}$$

where (X_{i1}, Y_{i1})~(X_{i4}, Y_{i4}) = the four corner coordinates of the ith division in the projected image and (x_{i1}, y_{i1})~(x_{i4}, y_{i4}) = the four corner coordinates of the ith division in the captured image.

The CTFs are used to modify the coordinates in the projected image in order to compensate for the coordinate mismatches between the projected and captured images. To validate the coordinate calibration, the coordinates of 35 equally-distributed cross marks between the projected and captured images were compared before and after the coordinate calibration. Coordinate transfer errors were quantified by the average differences between the mark coordinates for the projected and captured images. Because the number of the squares (n×m) in the checkered pattern affects the quantity of coordinate transfer errors [141], the coordinate transfer errors were obtained with various

numbers of squares, as shown in Figure 4.13. Here, the errors before the calibration are reflected when n is zero. As the figure shows, the coordinate transfer error decreases when n increases up to 25. Therefore, a 25×18 checkered pattern was used to calibrate the coordinates (m is 18 when n is 25).

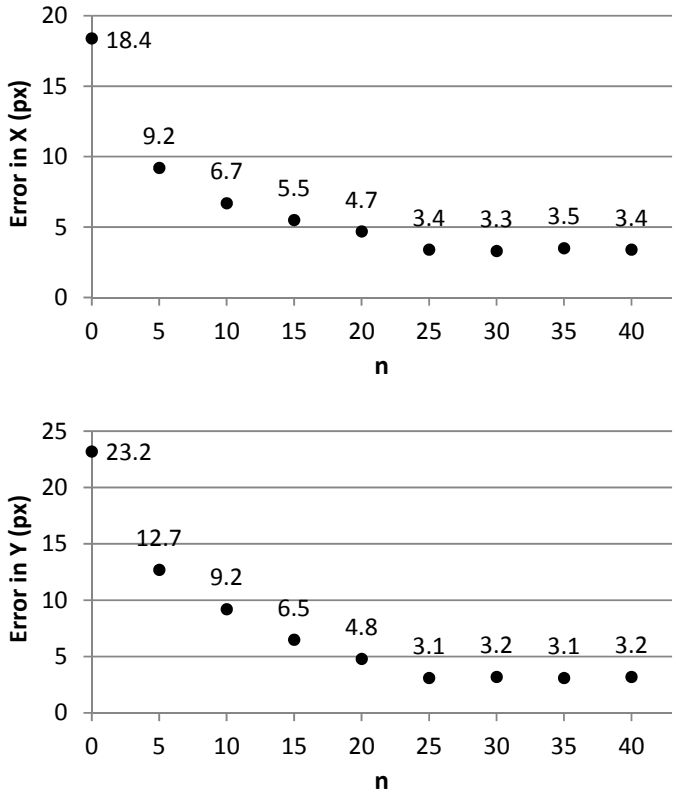


Figure 4.13. Coordinate transfer errors when n of the checker pattern increases

4.3.2 Segmentation of the PBGA Package and PWB Regions in Unpainted PWBA Images

To generate dynamic digital fringes and measure the warpage of PBGA package(s) and PWB in an unpainted PWBA, the PBGA package and PWB regions in an unpainted PWBA image need to be segmented. However, the mask image model, the active contour model, and the RGM cannot be applied for unpainted PWBA images

because they contain various surface patterns such as copper patterns and inscriptions, as shown in Figure 4.14. To solve this problem, the RGM was modified to segment the PBGA package and PWB regions in an unpainted PWBA image.

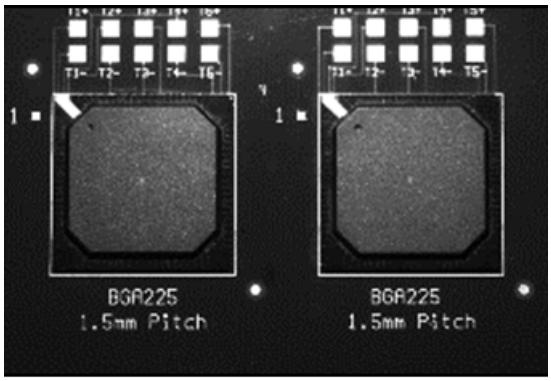


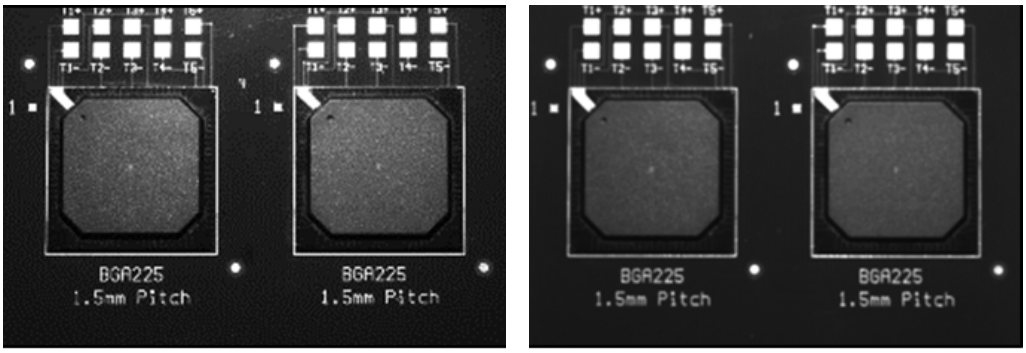
Figure 4.14. An unpainted PWBA image

The modified RGM process consists of the following steps: (1) capturing an unpainted PWBA image, (2) smoothening the PWBA image using the Gaussian filter [130], (3) generating the edges around each smoothened feature using the Canny algorithm [142], (4) segmenting the regions in the edged image with labels using the region-growing algorithm [143], and (5) detecting the PBGA package and PWB regions in the label image using geometric analysis [144]. The details of each step are provided below.

Step 1: Smoothening the PWBA image using the Gaussian filter.

Before applying the Canny algorithm, which is susceptible to noise present in raw image data, the unpainted PWBA image is smoothened by calculating the weighted average intensity using a 2D Gaussian function [130]. Since the image is stored as a collection of discrete pixels, a Gaussian kernel is convolved onto the image to smoothen it [130]. In this study, a 5×5 Gaussian kernel [130] was used, and sample images before

and after convolving the Gaussian kernel onto an unpainted PWBA image are shown in Figure 4.15.

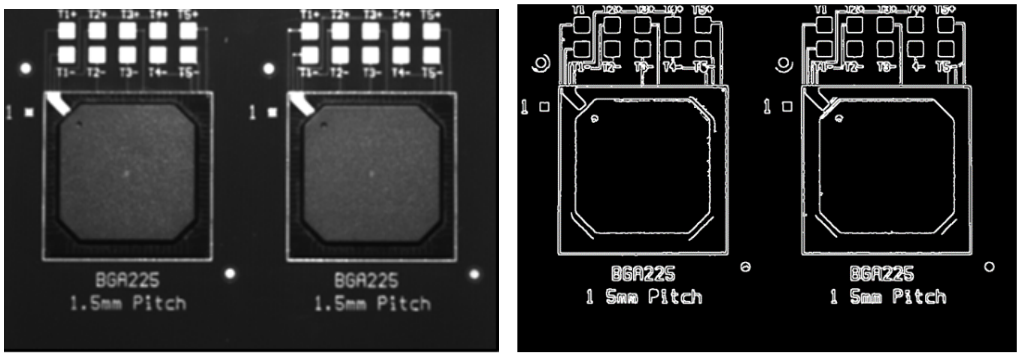


(a) (b)

Figure 4.15**.** Unpainted PWBA images (a) before and (b) after the Gaussian filtering

Step 2: Generating the edges around each smoothened feature using the Canny algorithm.

The Canny algorithm is the most frequently used algorithm for detecting edges in an image [142, 145]. To generate the edges around each smoothened feature, the Canny algorithm is applied to the smoothened PWBA image. Figure 4.16 shows the smoothened PWBA image and the edged PWBA image obtained after the Canny algorithm was applied.

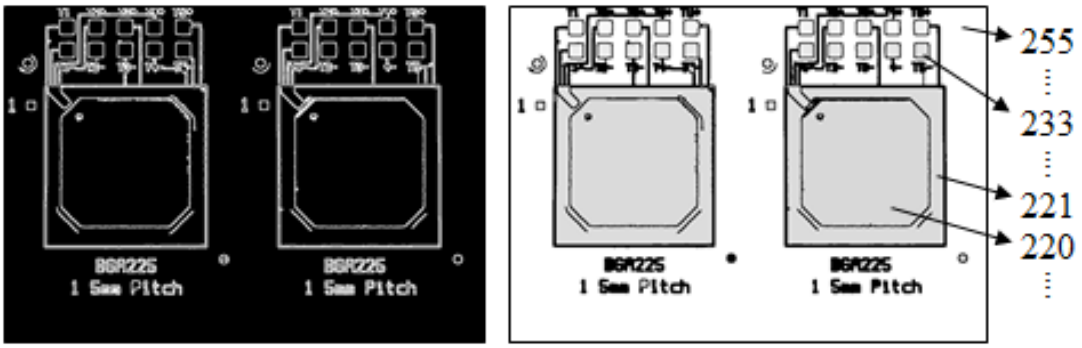


(a) (b)

Figure 4.16. (a) Smoothened PWBA image and (b) edged PWBA image obtained after the Canny algorithm is applied to (a)

Step 3: Segmenting the regions in the edged image with labels using the region-growing algorithm.

The region-growing algorithm [131] is a process of joining adjacent pixels of similar intensities into regions, a widely used process for region-based image segmentation [132]. The region-growing algorithm is applied to the edged PWBA image in order to label each region in the edged PWBA image. Figure 4.17 shows the edged PWBA image and the label image of the PWBA obtained after the region-growing algorithm was applied. In the label image, different gray values are assigned for each region, as depicted on the figure.



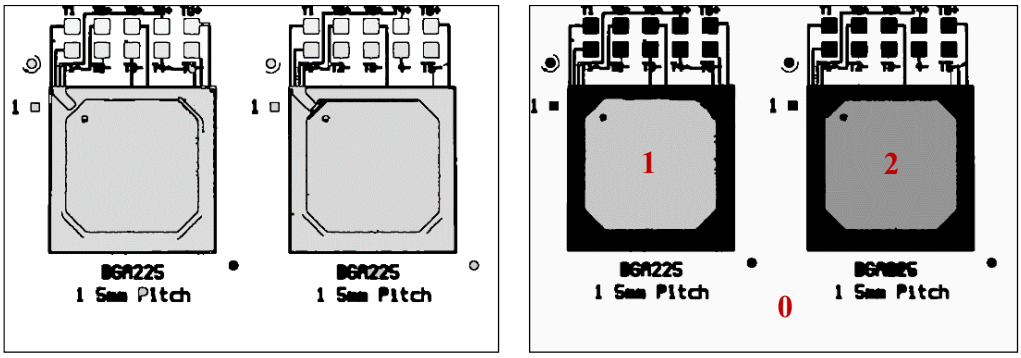
(a) (b)

Figure 4.17. (a) Edged PWBA image and (b) label image obtained after the region-growing algorithm is applied to (a)

Step 4: Detecting the PBGA package and PWB regions in the label image using geometric analysis.

To detect the PBGA package and PWB regions among the regions segmented in step 3, a geometric analysis was performed. After applying the geometric analysis, the largest region was recognized as the PWB region. Any region larger than 14×14 mm that does not encompass another region larger than 14×14 mm was recognized as the PBGA

package region. Here, the modified RGM was designed for PWBAs that contain PBGA package(s) larger than 14×14 mm because the minimum size of commercially available PBGA packages provided by Amkor, Samsung, ASE, and SPIL is 15×15 mm. Figure 4.18 depicts the results of detecting the PBGA package and PWB regions from the label image using the geometric analysis. The PWB region is marked with "0," the PBGA package regions are marked with "1" and "2," and the surface patterns and substrate regions are masked-out (in black).

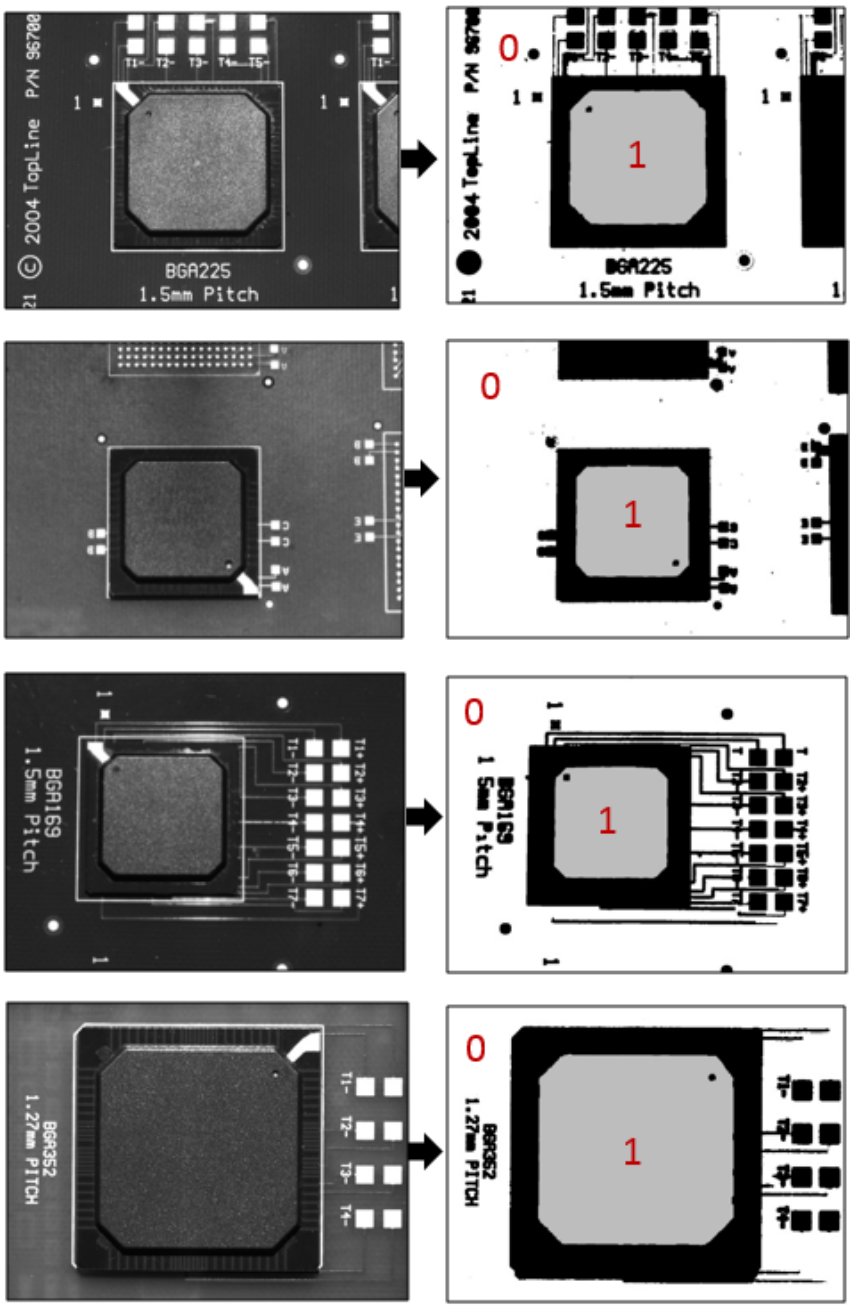


(a) (b)

Figure 4.18. (a) Label image of the PWBA and (b) detected PBGA package and PWB regions after the geometric analysis is applied to (a)

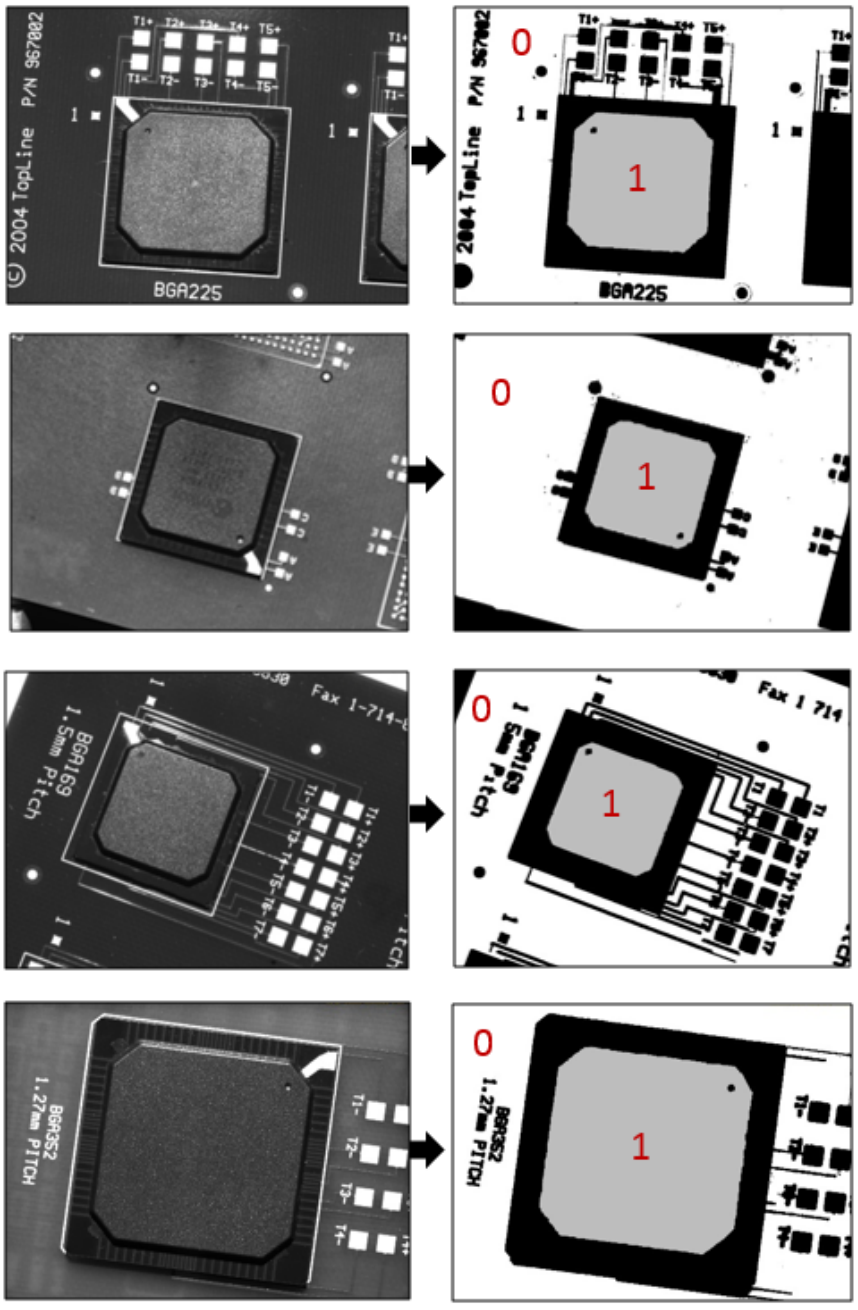
Validation of the modified RGM

Using the modified RGM to test the segmentation of the PBGA package and PWB regions in unpainted PWBA images, four different PWBAs were used. Figure 4.19 and 4.20 show their unpainted PWBA images and the resulting segmentation images produced by the modified RGM. The detected PWB and PBGA regions are marked with "0" and "1," respectively. The sizes of the PBGA packages shown in the unpainted PWBA images are 27×27 mm, 23×23 mm, 23×23 mm, and 35×35 mm, respectively.



(a) (b)

Figure 4.19. (a) Unpainted PWBA images and (b) resulting segmentation images



(a) (b)

Figure 4.20. (a) Unpainted PWBA images (rotated) and (b) resulting segmentation images

4.3.3 Intensity Calibration Between Projected and Captured Images

As described in Chapter 2.2, the ITF represents the relationship between computer intensity (I_I) and captured intensity (I_C), which is generally nonlinear. Figure 4.21 illustrates this nonlinearity when the sample is an unpainted PBGA package. In this case, the average absolute error between I_I and I_C is 19.1.

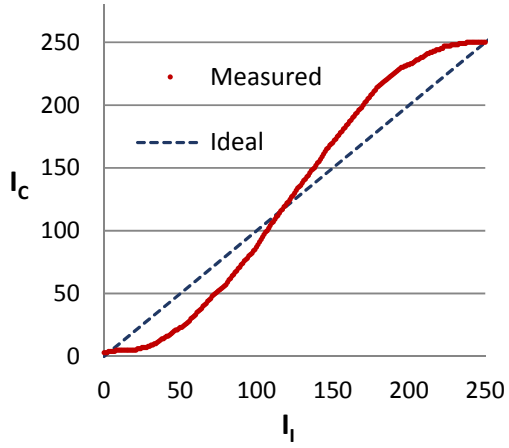


Figure 4.21. Relationship between I_I and I_C when the sample is an unpainted PBGA package

To calibrate the nonlinearity for unpainted samples, the polynomial regression method [106, 109] is applied together with the lookup table method [109]. A third-order polynomial regression equation (or ITF) between I_I and I_C for a sample surface is obtained by regressing six measured intensities. Figure 4.22 shows the ITF obtained using the polynomial regression method when the sample is the unpainted PBGA package.

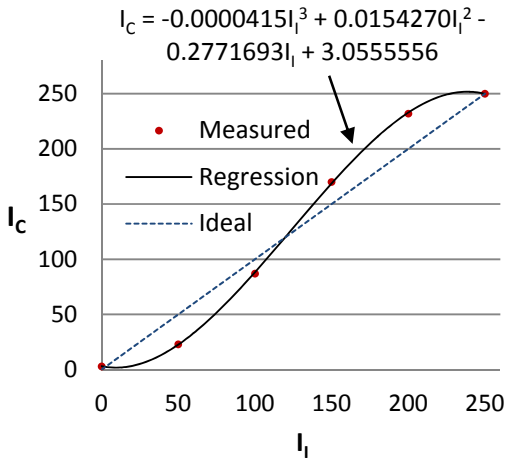


Figure 4.22. An ITF obtained by regressing six measured intensities

Using the ITF, a lookup table of the sample surface is created, which stores 256 I_C values and corresponding I_I values. Ultimately, the lookup table is used to calibrate input intensity in order to compensate for the nonlinearity [109]. As shown in Figure 4.23, the nonlinearity significantly declines after the calibration. In this case, the average absolute error between I_I and I_C is 4.1. When measuring a PWBA, intensities are simultaneously calibrated for each of the chip package and PWB surfaces.

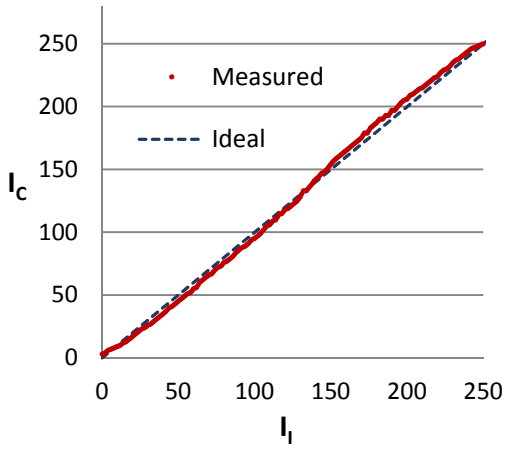
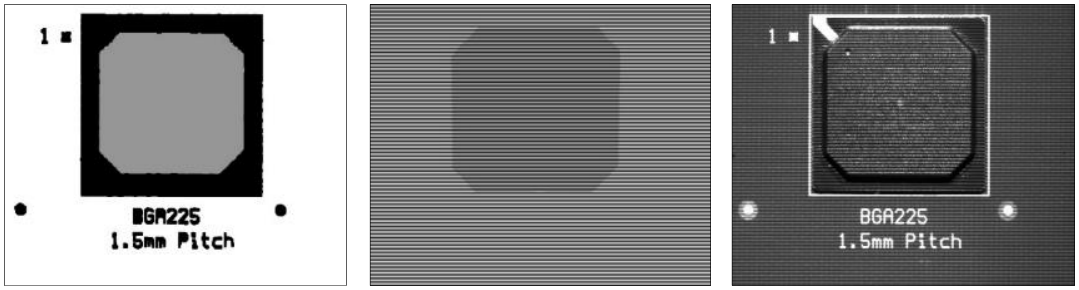


Figure 4.23. Relationship between I_I and I_C after the intensity calibration when the sample is the unpainted PBGA

4.3.4 Generation and Projection of a Dynamic Fringe Pattern

After the coordinate and intensity calibrations, a dynamic fringe pattern is generated. The coordinates of the PBGA package region in the segmented label image (Figure 4.24 (a)) are converted to those coordinates in the dynamic fringe pattern (Figure 4.24 (b)). For each region in the segmented label image, a proper fringe intensity distribution is determined, as depicted in Figure 4.24 (b). After the dynamic fringe pattern is generated, it is projected onto the PWBA, as shown in Figure 4.24 (c).



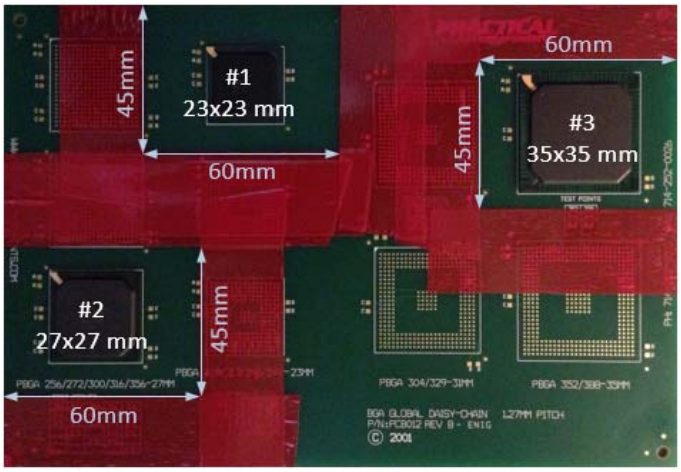
(a) (b) (c)

Figure 4.24. (a) The segmented label image, (b) the dynamic fringe pattern, and (c) the PWBA fringe image illuminated by (b)

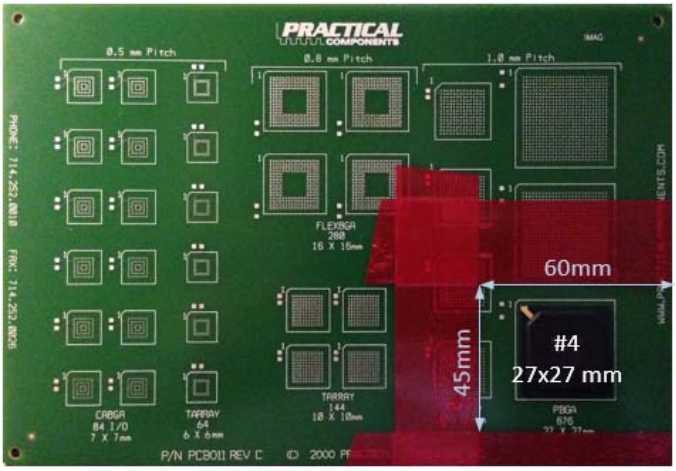
4.3.5 Validation of the DDFP Technique

To validate the DDFP technique, four PBGA packages and two PWBs, shown in Figure 4.25, were used. The sizes of the three-layer PWBs are 200×140 mm and the thicknesses are 1.5 mm. The sizes of the PBGA packages are 23×23 mm, 27×27 mm, 35×35 mm, and 27×27 mm, and the substrate materials of the PBGA packages are BT. The warpage of the four PBGA packages and four PWB regions (60×45 mm) were separately measured using as the reference a contact profilometer with a resolution of less than 0.1 μm. Red masking tape was placed on the PWBs to ensure consistency of the FOVs in all measurements and adhesive was used to temporarily attach the PBGA

packages to the PWBs in order to simulate PWBAs. Then, using the DFP system integrated with the DDFP technique, the warpage of the PBGA package and the PWB in each of the four PWBA region (60×45 mm) were simultaneously measured. Next, the PBGA packages were detached from the PWBs, and the warpage of the PBGA packages and the PWBs (60×45 mm) were separately measured using the shadow moiré system as a comparison after painting the sample surfaces. Figures from 4.26 to 4.29 contain warpage images obtained by the DFP and shadow moiré systems.



(a)



(b)

Figure 4.25. (a) PWBA1 with three PBGA packages and (b) PWBA2 with one PBGA package

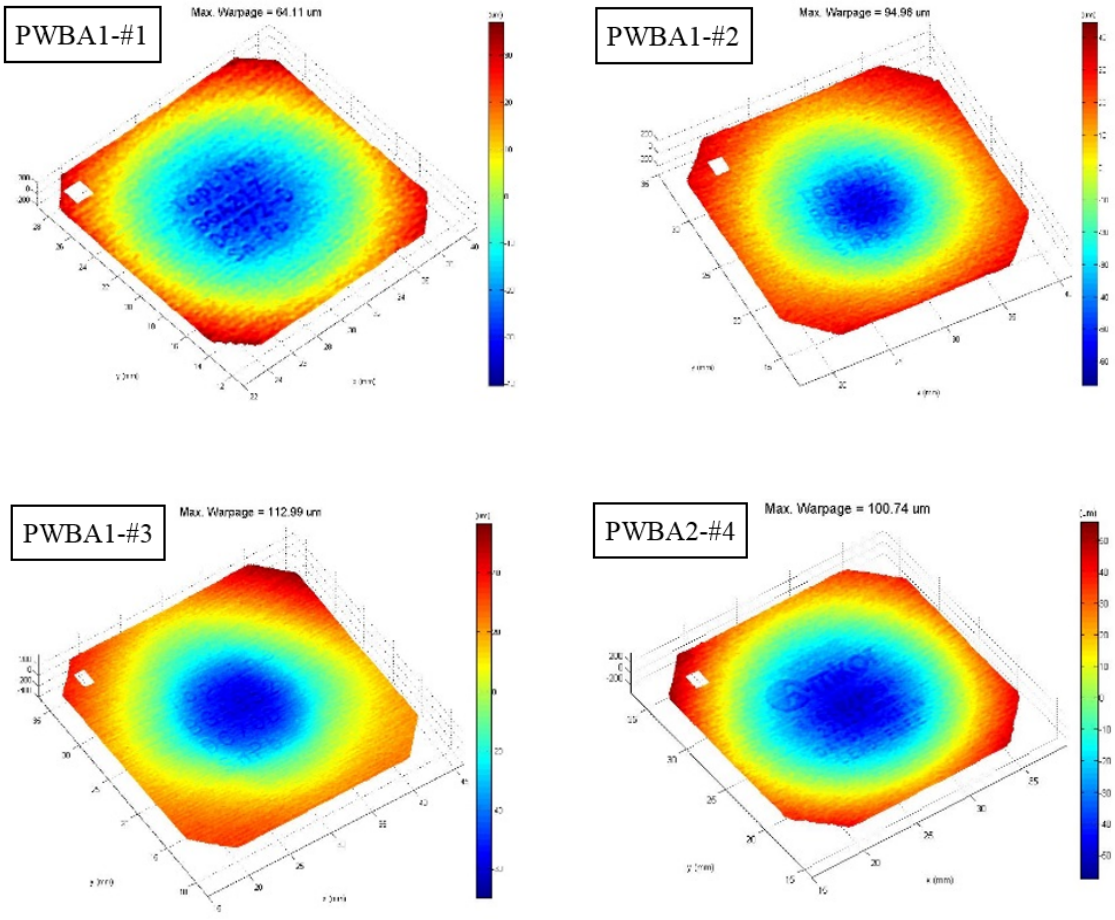


Figure 4.26. Warpage of the PBGA packages obtained with the DDFP

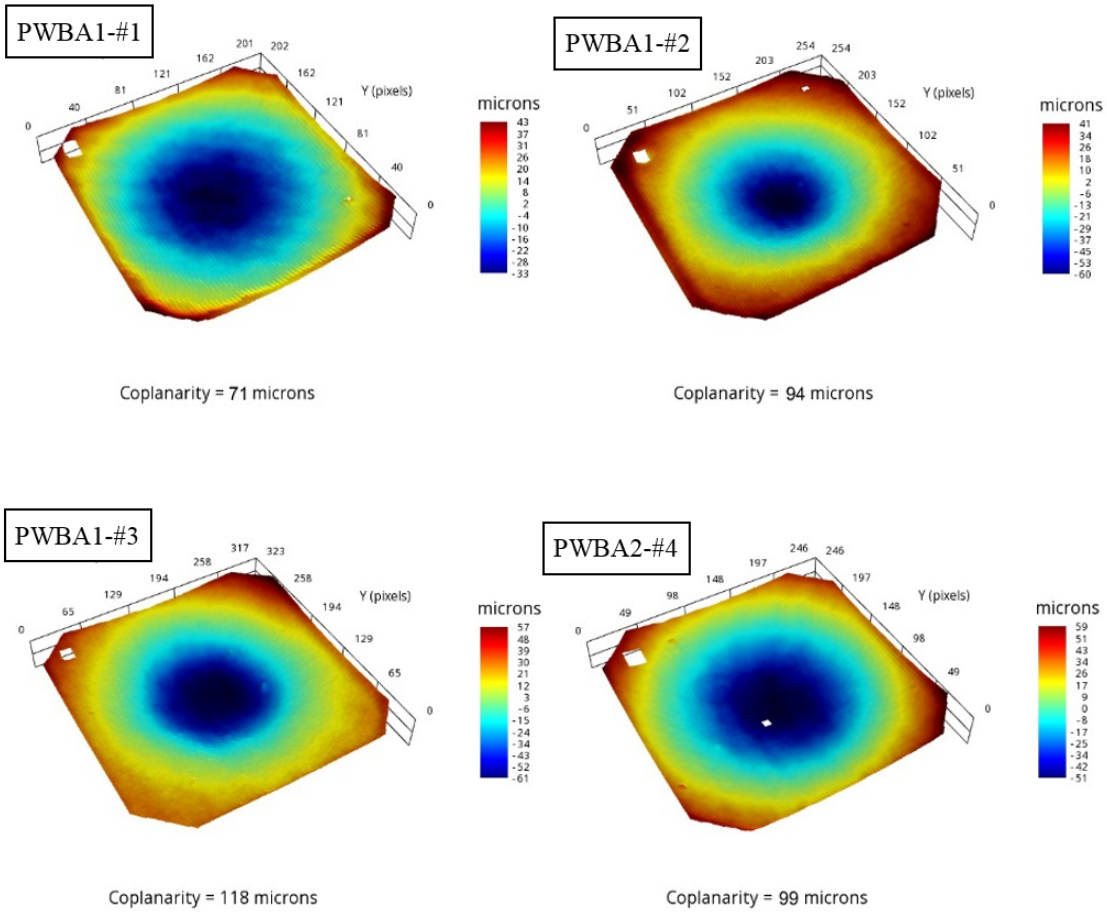


Figure 4.27. Warpage of the PBGA packages obtained with the shadow moiré

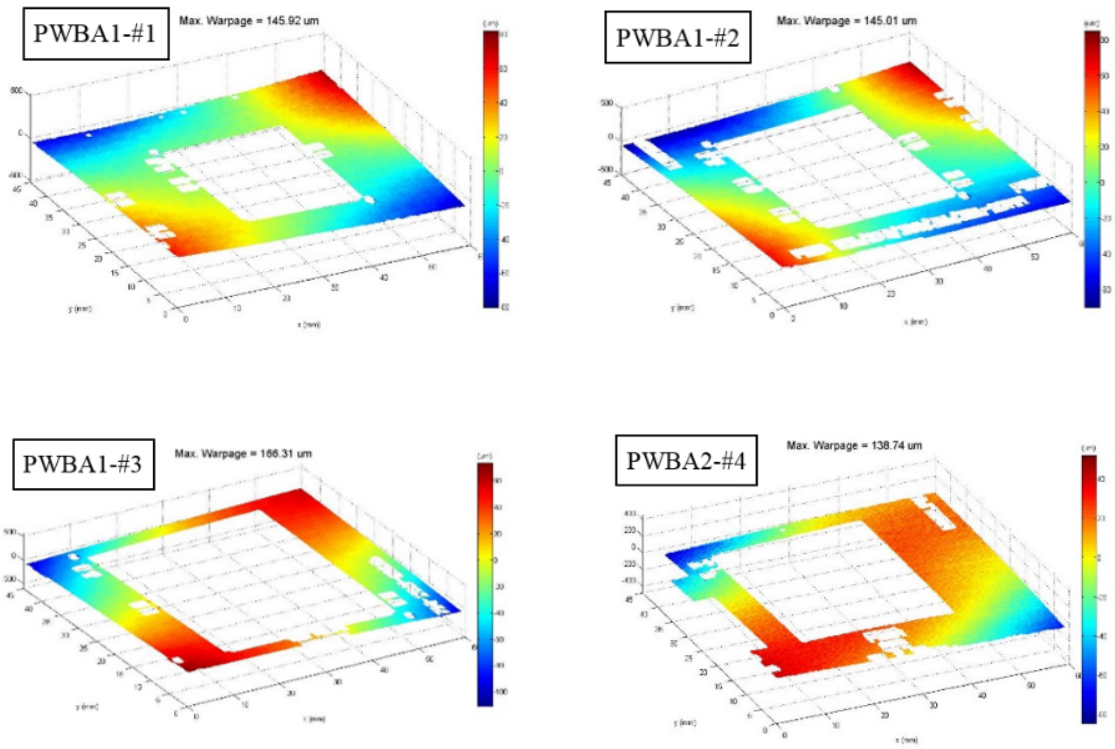


Figure 4.28. Warpage of PWBs obtained with the DDFP

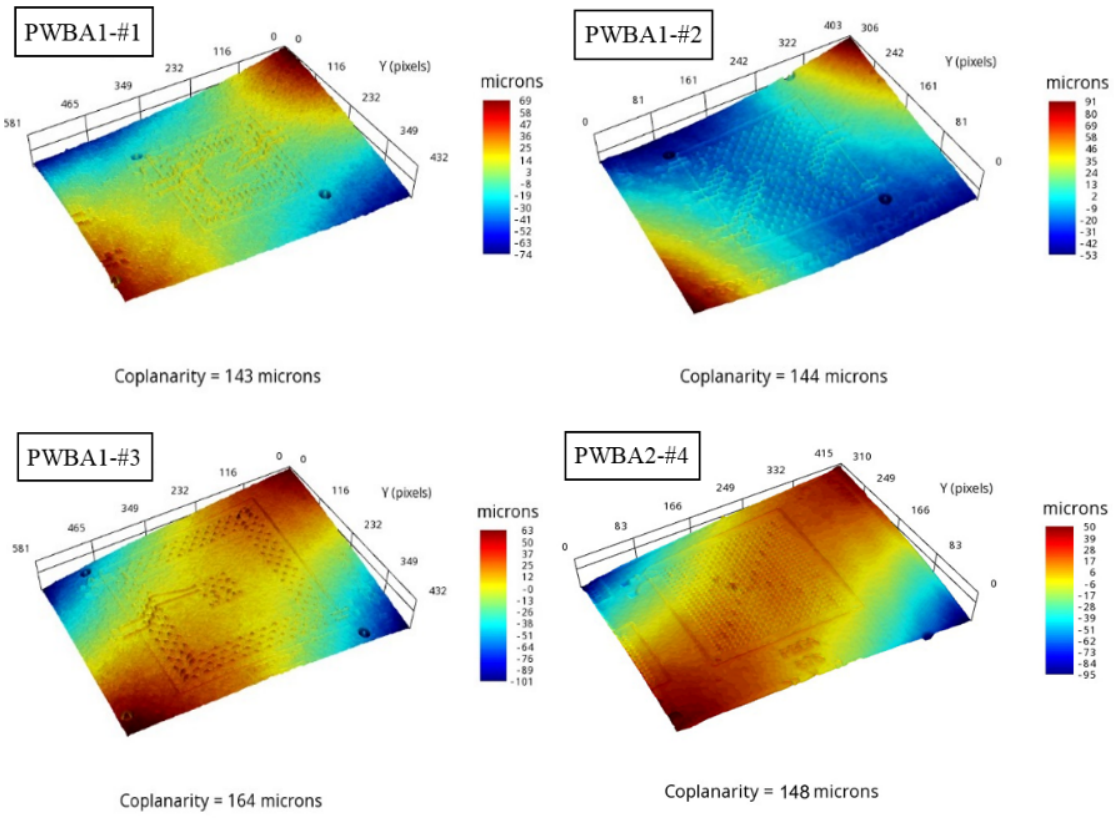


Figure 4.29. Warpage of PWBs obtained with the shadow moiré

The measurement results are summarized in Tables 4.8 and 4.9. The results show that the absolute measurement errors of the DDFP results were less than 8% compared to those of the contact profilometer results, while the errors of the shadow moiré results were less than 5%. The results also show that the major advantage of the DDFP technique is that it can simultaneously measure the warpage of PBGA package(s) and PWBs in PWBAs without surface painting, enabling the warpage measurement during the assembly process. On the other hand, if a sample surface has too many surface patterns such as copper patterns and inscriptions, the DDFP technique causes greater error, for it obscures these patterns during measurements as shown in Figure 4.28.

Table 4.8. Comparison of the warpage of PBGA packages measured using the contact profilometer (CP), shadow moiré (SM) system, and DDFP

Sample	Max. Warpage (μm)			Error (%)	
	CP[a]	SM[b]	DDFP[c]	SM	DDFP
PWBA1-#1	67.80	70.33	64.40	3.74%	5.01%
PWBA1-#2	90.33	93.67	95.02	3.69%	5.19%
PWBA1-#3	120.21	118.33	113.48	1.56%	5.60%
PWBA2-#4	94.51	98.67	100.53	4.40%	6.36%

[a]Used as reference (CP resolution < 0.1 μm), [b]Average of three measurements (SM resolution = 0.83 μm when using 300 LPI grating), [c]Average of ten measurements

Table 4.9. Comparison of the warpage of PWBs measured using the contact profilometer (CP), shadow moiré (SM) system, and DDFP

Sample	Max. Warpage (μm)			Error (%)	
	CP[a]	SM[b]	DDFP[c]	SM	DDFP
PWBA1-#1	138.82	143.33	145.47	3.25%	4.79%
PWBA1-#2	136.48	142.67	146.87	4.53%	7.61%
PWBA1-#3	160.32	164.00	167.01	2.30%	4.17%
PWBA2-#4	150.18	147.67	138.45	1.67%	7.81%

[a]Used as reference (CP resolution < 0.1 μm), [b]Average of three measurements (SM resolution = 0.83 μm when using 300 LPI grating), [c]Average of ten measurements

4.4 Chapter Summary

This work introduced an unique DDFP technique, the first of its kind, for measuring the warpage of unpainted PBGA packages and boards. The DDFP technique

includes a method for segmenting the PBGA package and PWB regions in an unpainted PWBA image and calibration methods to compensating for coordinate and intensity mismatches between projected and captured images. Experimental results showed that the DDFP technique successfully measured the warpage of PBGA packages and PWBs in unpainted PWBAs and that, compared to the contact profilometer, DDFP produced a measurement error of less than 8%. Because of rapid advances in digital technologies, this new technique presents great potential for generating accurate measurements of the warpage of unpainted PBGA packages and boards in an assembly line.

CHAPTER 5

PARAMETRIC STUDIES OF THE EFFECTS OF SOLDER BUMP PITCH, PACKAGE SIZE, AND MOLDING COMPOUND AND SUBSTRATE THICKNESSES ON WARPAGE OF PBGA PACKAGES USING THE FEA

Along with warpage measurement; accurate warpage prediction for a particular chip package is crucial for ensuring the reliability of the chip package. Among the various chip packages, PBGA, one of the most widely used, has widespread application in various electronic devices such as digital televisions, microcontrollers, laptops, and tablets. The commercially available PBGA packages have various dimensions as shown in Table 5.1.

Table 5.1. The dimensions of commercially available PBGA packages

Company	Amkor	Samsung	ASE	SPIL
Solder Bump Count	144-1521	208-1156	119-1520	up to 1156
Solder Bump Pitch (mm)	1.0-1.5	0.65-1.27	1.0-1.5	1.0-1.27
Package Size (mm)	17×17-40×40	17×17-35×35	15×15-45×45	15×22-40×40
Molding Compound Thickness (mm)	0.85-1.17	0.68-1.28	N/A	N/A
Substrate Thickness (mm)	0.36-0.56	0.26-0.56	0.36-0.56	N/A
Overall Thickness (mm)	1.8-2.5	1.4-2.6	1.61-2.33	N/A

Because the PBGA packages have various I/O densities, sizes, and thickness, accurate prediction of PBGA warpage resulting from those parameters is required during PBGA design. Therefore, parametric FE studies were conducted to assess the effects of solder bump pitch, package size, and molding compound and substrate thicknesses on PBGA warpage after the reflow process.

5.1 FE Model

The FE model of a PWBA containing a PBGA package developed by Powell [5] was used in the parametric studies. The cross section of the PWBA is depicted in Figure 5.1. In this work, the FE model was slightly modified. The PWB size was reduced from 203.2×139.7mm to 46×46 mm to minimize the effect of PWB warpage. In addition, instead of the full model used by Powell, this work used a quarter-symmetric model to save simulation time.

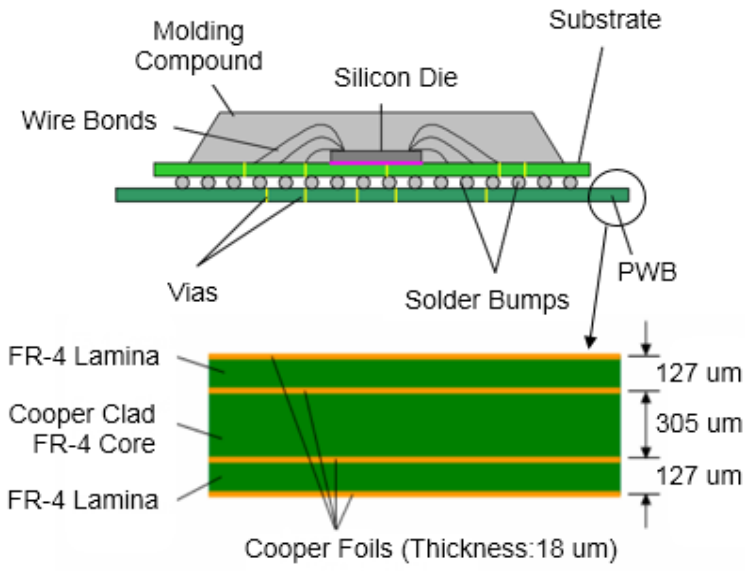


Figure 5.1. Cross section of the PWBA used for the FEA [1, 5]

The material properties used for the FE model are summarized in Table 5.2 and 5.3. The PBGA was modeled using SOLID95, a 3D 20-node structural solid element [5]. The PWB was modeled using SHELL91, a nonlinear layered structural shell element, known for its advantages in modeling layered shell structures [5].

Table 5.2. Room temperature material properties used for the FE model [1, 5]

Part	Material	CTE (ppm/K)	E (GPa)	ν
PWB	**FR-4**	20.00	22.40	0.14
	Copper Foil	18.94	79.51	0.32
Solder Bumps	**Sn-Pb**	21.00	19.78	0.40
Substrate	**BT**	15.00	14.00	0.15
Molding Compound	**Plastic Molding**	17.50	15.00	0.15
Die	**Silicon**	2.60	160.00	0.23

(CTE: Coefficient of Thermal Expansion, E: Elastic Modulus, ν: Poisson's Ratio)

Table 5.3. Temperature-dependent material properties used for the FE model [1, 5]

Material	Temperature (K)	CTE (ppm/K)	E (GPa)	ν
FR-4	303	20.00	22.40	0.14
	368	20.00	20.68	0.14
	423	20.00	17.92	0.14
	543	20.00	16.00	0.14
Sn-Pb	248	21.00	27.39	0.40
	298	21.00	19.65	0.40
	358	21.00	15.27	0.40
	398	21.00	11.68	0.40

5.2 Reflow Profile

Figure 5.2 shows a typical ramp to dwell, ramp to peak (RDRP) profile, which was used in this study. The RDRP profile consists of the following four zones: the ramp to dwell, dwell, ramp to peak, and cooling zones [5]. An assembly enters a reflow oven and passes the ramp to dwell zone, in which the assembly is heated at the rate of 2ºC/second [5]. Component manufacturers typically specify a maximum rate of temperature rise of 2 to 4 ºC/second in the ramp to dwell zone [5]. In the dwell zone, the solvents evaporate, the flux in the solder paste activates, and the temperature of the assembly becomes uniform before entering the ramp to peak zone [5]. In the ramp to peak zone, the assembly is heated above the solder liquidus temperature so that the solder melts completely. A minimum dwell time above liquidus is usually specified [5]. Finally, the assembly is cooled to room temperature in the cooling zone.

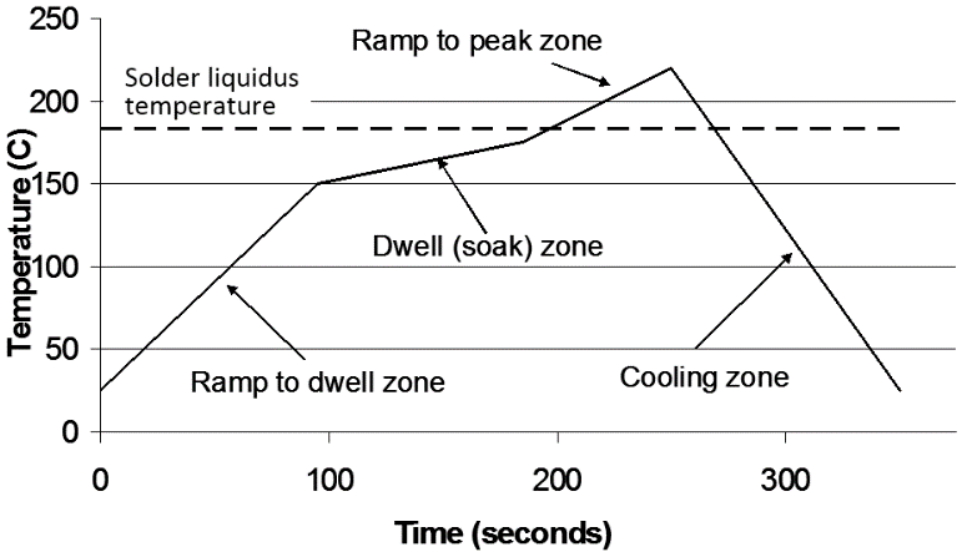
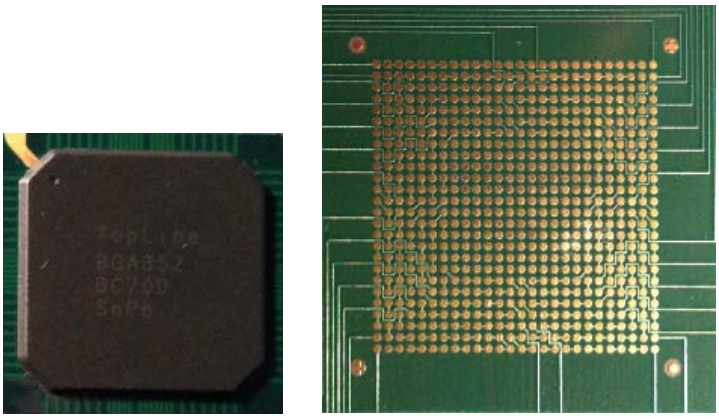


Figure 5.2**.** Typical ramp to dwell, ramp to peak reflow profile [5]

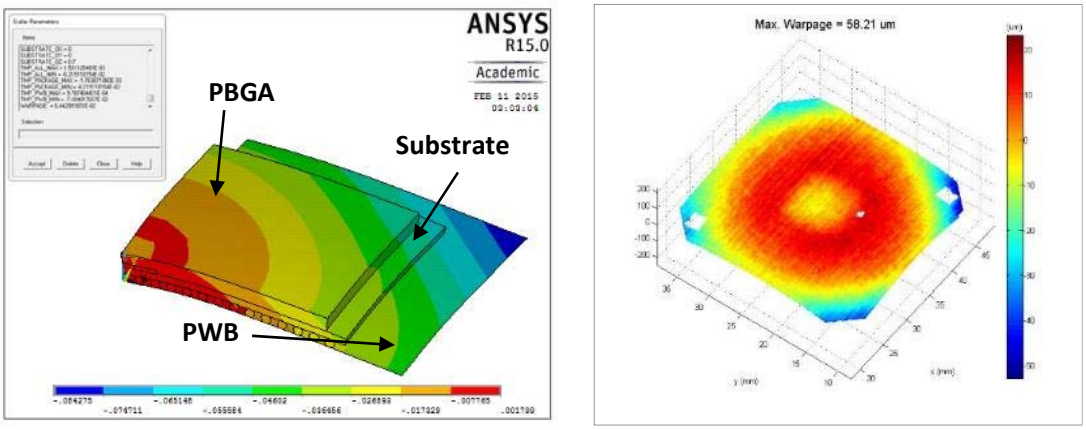
5.3 Validation of the FE Model

To validate the FE model, a 45×45 mm region was cut from a 203.2×139.7 mm PWB, and a 35×35 mm PBGA package was assembled on the 45×45 mm region in a reflow oven using the RDRP profile. The PBGA package and the 45×45 mm PWBA region are shown in Figure 5.3. The solder bump pitch and the molding compound and substrate thicknesses of the PBGA package are 1.27 mm, 1.17 mm, and 0.56 mm, respectively. The warpage of the PBGA package in the PWBA was measured using the DFP system and compared with the simulation results obtained using the FE model. Figure 5.4 shows the wapage contour plots generated by the FEA and the DFP system.



(a) (b)

Figure 5.3. (a) A 35×35 mm PBGA package and (b) a 45×45 mm PWB region used to validate the FE model



(a) (b)

Figure 5.4. The warpage contour plots generated by (a) the FEA and (b) the DFP system

The maximum PBGA warpage obtained from the FE model and the experiment were 64.42 µm and 58.21 µm, respectively. The FE results produced a percentage error of 9.64% when compared to the experimental results. The difference between the simulation and experimental results can be attributed to a number of factors. First, the initial warpage of the PWB produced during its lamination process [6] and when cutting it from the large PWB could have affected the PBGA warpage after the assembly. Second, some of the material properties used in the FEA were the room temperature material properties which are different from temperature dependent properties. Even though the simulation and experimental results did not match exactly, the FE model can still be used to perform the parametric studies.

5.4 Design of Simulations and Simulation Results

The DOE is a systematic approach to get the maximum amount of information out of various types of experiments. One of the most simple and widely used DOE methods is the full-factorial DOE method [146]. The full-factorial DOE method provides complete

information on the effects of factors on the system [147]. On the other hand, the number of runs in the full-factorial design increases exponentially with the number of factors and the number of factor levels [147].

To determine the effects of the four factors (F1: solder bump pitch, F2: package size, F3: molding compound thickness, and F4: substrate thicknesses) on PBGA warpage, the full-factorial DOE was used to design the simulation runs. As summarized in Table 5.4, two levels of each factor were determined from the possible geometric variation of the PBGA packages that are commercially available.

Table 5.4. The two levels of the factors

Level #	**F1 (mm)**	**F2 (mm)**	**F3 (mm)**	**F4 (mm)**
1	0.65	15	0.68	0.26
2	1.5	45	1.28	0.56

(Full array solder bumps are used)

To conduct simulations, sixteen combinations of the four factors (F1-F4) were designed using the full-factorial DOE method, as shown in Table 5.5. For each simulation run, the maximum PBGA warpage (W_{max}) after the RDRP reflow process was obtained by the FEA, and the maximum curvature of PBGA warpage (K_{max}) was calculated based on the accumpsion of small deformation [62], as summarized in Table 5.5. For example, W_{max} and K_{max} are 60.21 μm and 0.54 μm, respectively, when F1, F2, F3, and F4 are 0.65 mm, 15 mm, 0.68 mm, and 0.56 mm, respectively. A warpage contour plot generated by the FEA is shown in Figure 5.5 that depicts the amount of the warpage used in this study.

Table 5.5. The design of simulations and simulation results

Run #	F1 (mm)	F2 (mm)	F3 (mm)	F4 (mm)	W_{max} (μm)	K_{max}[a] (μm)
1	0.65	15.00	0.68	0.56	60.21	0.54
2	0.65	45.00	1.28	0.56	121.01	0.12
3	1.50	15.00	1.28	0.26	28.39	0.25
4	0.65	15.00	1.28	0.26	25.30	0.22
5	0.65	45.00	0.68	0.26	255.00	0.25
6	1.50	45.00	1.28	0.26	80.62	0.08
7	1.50	45.00	0.68	0.56	175.59	0.17
8	1.50	15.00	0.68	0.56	31.74	0.28
9	0.65	15.00	1.28	0.56	27.20	0.24
10	1.50	15.00	0.68	0.26	25.03	0.22
11	1.50	45.00	0.68	0.26	186.90	0.18
12	0.65	45.00	0.68	0.56	226.82	0.22
13	1.50	15.00	1.28	0.56	26.91	0.24
14	1.50	45.00	1.28	0.56	69.41	0.07
15	0.65	45.00	1.28	0.26	128.80	0.13
16	0.65	15.00	0.68	0.26	57.41	0.51

[a] $K_{max}=2W_{max}/F2^2$ [62]

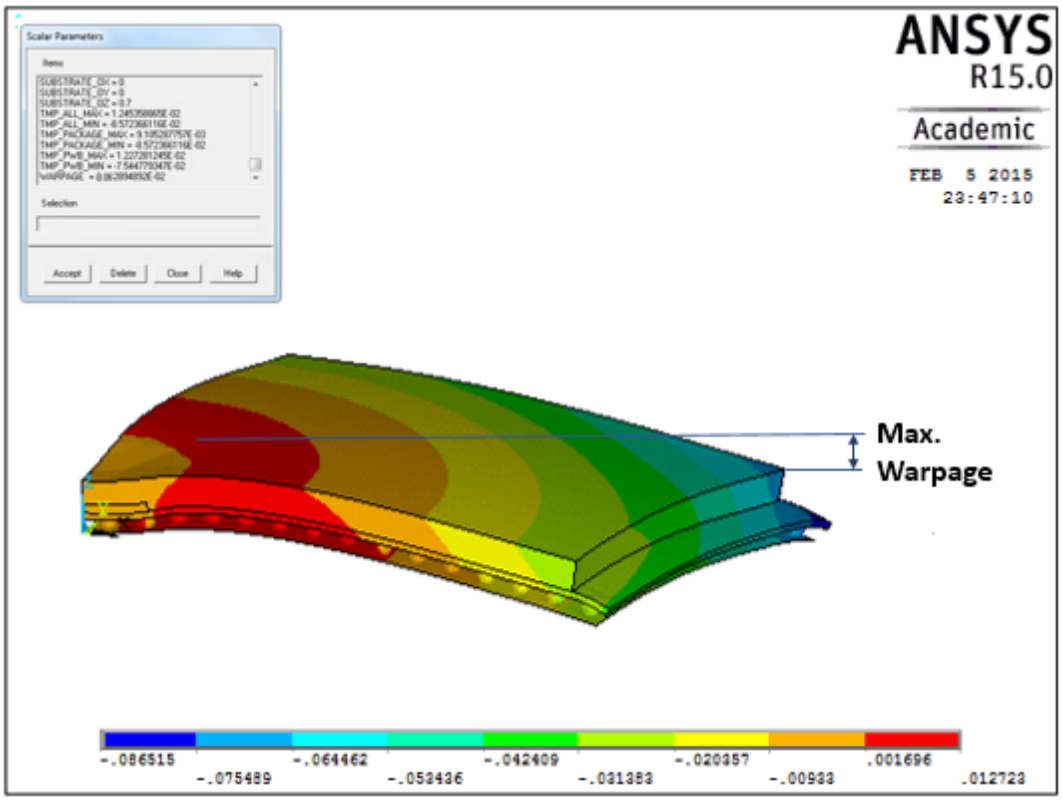


Figure 5.5. A warpage contour plot generated by the FEA (when F1 = 1.5 mm, F2 = 45 mm, F3 = 1.28 mm, F4 = 0.26 mm)

5.5 Analysis of Simulation Results

The ANOVA is a widely used collection of statistical models by which the effects of a specific factor on a response of interest can be evaluated [148, 149]. P-values obtained by the ANOVA quantify the significance of the effects of the factors, in which a smaller p-value indicates a more significant effect [122]. Main effect plots can be used to visualize the effects of the factors [122].

The ANOVA was applied to simulation results to identify the effects of each factor on W_{max} and K_{max}. Table 5.6 shows the p-values of each factor obtained by the ANOVA. According to the table, the orders of significance of the factors on W_{max} and

K_{max} are F2, F3, F1, and F4. Figures 5.6 and 5.7 depict the main effect plots of each factor on W_{max} and K_{max}.

Table 5.6. p-values of each factor (F1-F4) when the response is W_{max} or K_{max}

Response	Factor	p-value
$\mathbf{W_{max}}$	**F1**	0.0562
	F2	0.0004
	F3	0.0023
	F4	0.7153
$\mathbf{K_{max}}$	**F1**	0.0202
	F2	0.0012
	F3	0.0031
	F4	0.9123

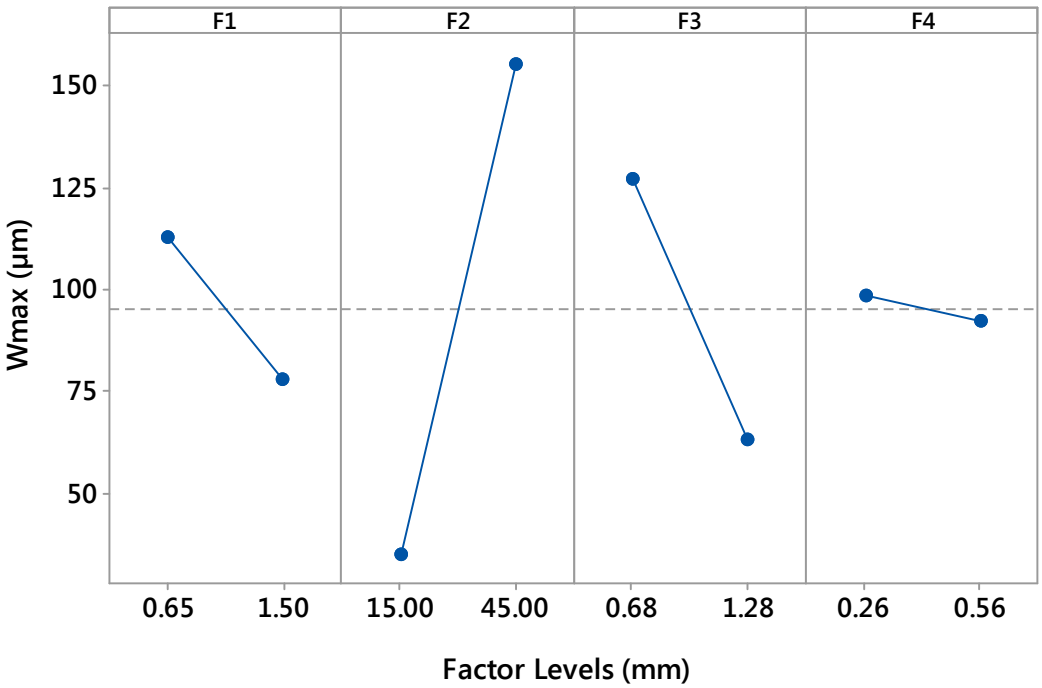


Figure 5.6. The main effect plots of each factor (F1-F4) on W_{max}

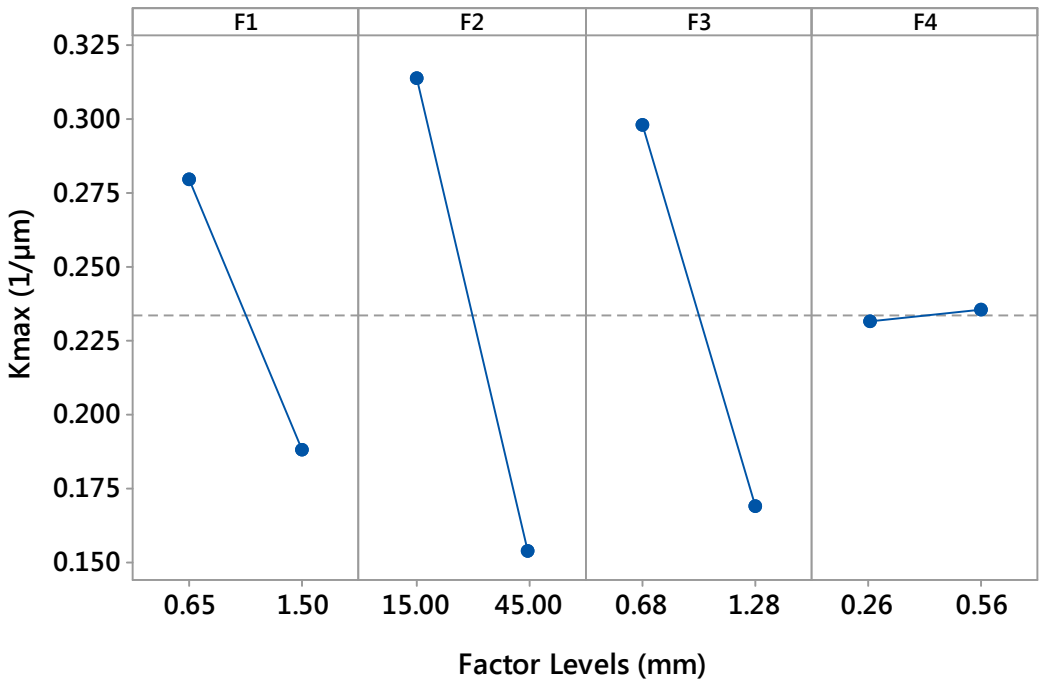


Figure 5.7. The main effect plots of each factor (F1-F4) on K_{max}

Solder bump pitch determines solder bump density and the corresponding contact conditions between the substrate and board. Solder bump pitch also determines solder bump diameter, which is closely related to the amount of deformation of the solder balls during the reflow process. These factors could explain why solder bump pitch significantly affects the warpage, as the results show. The reason the variance in substrate thickness does not significantly affect warpage could be because the substrate is between the molding compound and the board, and they are thicker than the substrate. The results also show that package size and molding compound thickness significantly affect the warpage, as is to be expected. In sum, a proper combination of solder bump pitch, package size, and molding compound is important to reduce the warpage of PBGA packages in PWBAs in order to increase the reliability of the PWBAs.

5.6 Regression Equations of PBGA Warpage

The regression method is one of the standard ways for determining the best-fitting mathematical equation with known experimental or simulation data [129]. This method is useful for understanding how a dependent variable changes when any one of the independent variables varies using a mathematical equation. Therefore, regression method is widely used for prediction and forecasting [129].

To study the correlation between PBGA warpage and the four factors, bilinear equations were developed using the regression method. Equations 5.1 and 5.2 show bilinear equations expressing W_{max} and K_{max} as functions of the four factors (F1-F4) and their two-factorial interactions. Notably, the three-factorial interactions are omitted based

on the hierarchical ordering principle, which states that lower-order effects are more likely to be important than higher-order effects [122].

$$\begin{aligned} W_{max} = & -41.6 - 39.0\,F1 + 11.628\,F2 + 0.6\,F3 + 6.5\,F4 \\ & - 1.579\,F1F2 + 40.8\,F1F3 + 13.7\,F1F4 \\ & - 5.248\,F2F3 - 1.901\,F2F4 + 15.8\,F3F4 \end{aligned} \tag{5.1}$$

$$\begin{aligned} K_{max} = & \ 1.098 - 0.484\,F1 - 0.00891\,F2 - 0.552\,F3 + 0.198\,F4 \\ & + 0.00294\,F1F2 + 0.287\,F1F3 + 0.018\,F1F4 \\ & + 0.00212\,F2F3 - 0.00406\,F2F4 - 0.084\,F3F4 \end{aligned} \tag{5.2}$$

The resulting bilinear equations were evaluated by R^2 [107], which indicates how well regression equations approximate actual data. The R^2 values of the bilinear equations were 99.73 % and 92.12 %, respectively.

5.7 Chapter Summary

This work used the FEA to carry out parametric studies to access the effects of solder bump pitch (F1), package size (F2), molding compound thickness (F3), and substrate thickness (F4) on PBGA warpage after the reflow process. The study employed the full-factorial DOE method to design simulations and the ANOVA to identify the effects of each factor on the maximum PBGA warpage (W_{max}) and the maximum curvature of PBGA warpage (K_{max}). For the particular PWBA model used in this study, the orders of significance of the factors on W_{max} and K_{max} were found to be F2, F3, F1, and F4. The regression method was used to obtain the bilinear equations of W_{max} and K_{max} as functions of the four factors (F1-F4). The R^2 values of the bilinear equations were 99.73 % and 92.12 %, respectively. Even though this study used a particular PWBA

model, the results from this study will provide guidelines that PBGA designers can use to minimize the warpage of PBGA packages.

CHAPTER 6

DEVELOPMENT OF A SELECTION GUIDELINE OF WARPAGE MEASUREMENT TECHNIQUES

With the development of new warpage measurement techniques and diversified chip packages, choosing the appropriate measurement technique for a particular application can be daunting for manufacturing engineers. To address this problem, a selection guideline for warpage measurement techniques was developed. Eight measurement features important for warpage measurement were determined and used to develop the guideline.

6.1 Features of Warpage Measurement Techniques

In order to choose an appropriate warpage measurement technique, a manufacturing engineer should first assess the major features of each technique. The following eight measurement features were determined to be important for measuring the warpage of chip packages and boards: resolution, coverage area, speed, cost, accuracy, flexibility, robustness, and in-line capability. The definitions of these features are summarized in Table 6.1.

Table 6.1. Definitions of the measurement features

Feature	**Definition**
Resolution	The smallest displacement that a system can measure in the out-of-plane direction (or z-direction)
Coverage Area	The maximum sample size that a system can measure
Speed	The time it takes to measure the warpage of each chip package, PWB, or PWBA
Cost	The price of a measurement system including necessary positioning stages
Accuracy	The measurement accuracy in the out-of-plane direction
Flexibility	The ability to measure samples of different sizes and surface reflectance
Robustness	Insensitivity to noise and error sources such as surface contamination, vibration, and manual operation
In-Line Capability	The ability of a system to be used in a production line for warpage measurement

Each measurement feature defined in Table 6.1 is affected and controlled by its primary factors. For example, the primary factors affecting accuracy are practical resolution and calibration accuracy [98]. The primary factors that affect and control each of the eight features are summarized in Table 6.2.

Table 6.2. Measurement features and their primary factors

Feature	**Primary Factor**
Resolution	Practical Resolution
Coverage Area	Full-field Coverage Area or Scan Range
Speed	Full-field Coverage Area
	Data Acquisition Speed
	Computation Speed
Costs	Cost of Positioning Stage and Actuator
	Cost of Sensor Components
	Cost of Software
Accuracy	Practical Resolution
	Calibration Accuracy
Flexibility	Insensitivity to Surface Reflectance
	Ability to Measure Various Sample Sizes
Robustness	Insensitivity to Surface Contamination
	Insensitivity to Vibration
	Insensitivity to Manual Operation
In-Line Capability	Contact (C) or Non-Contact (N)
	Full-field Coverage Area
	Data Acquisition Speed
	Computation Speed
	Insensitivity to Surface Contamination
	Insensitivity to Vibration
	Ability to Measure Unpainted Sample

6.2 Comparison of Features of Various Warpage Measurement Techniques

Chapter 2 outlines the basic principles of the various warpage measurement techniques and reviews the literature addressing these techniques. This chapter compares the features of ten warpage measurement techniques by studying their relative advantages and disadvantages.

6.2.1 Contact-Type

Gauge Indicator Shim Method

The gauge indicator shim method, which uses feeler gauges, is the oldest technique for measuring the warpage of PWBs. The application of this method is very simple, inexpensive, and easy. Because the measurement is performed by human operation, various samples with different sizes and surface reflectances are measurable, and the results are insensitive to ambient vibration and surface contamination. However, the method measures rough warpage only along the edges and corners of the sample with low resolution and accuracy. The method's resolution is determined by the minimum thickness of commercially available feeler gauges. Currently, the minimum thickness available is 0.0015 in (38.1 μm). Additionally, because this method requires manual operation, automating the measurement function is difficult. The method generally requires at least several minutes to quantify the level of warpage, making it unsuitable for in-line measurement. The method is also very error-prone because measurement results are dependent on the judgment of the human operator.

Contact Profilometry

The contact profilometry uses a vertical stylus or probe, which is moved laterally by an accurate moving stage, for measuring the warpage of chip packages and boards. The major advantages of contact profilometry are high-resolution, accuracy, and robustness. The radius of the stylus tip that determines the measurement resolution can be as small as 20 nm, making this method capable of very high-resolution [150]. For example, the contact profilometer used in this study provides a resolution of less than 0.1 μm and a scan range up to 150×150 mm. Because the stylus tip is in contact with the surface of a sample, contact profilometry is not sensitive to environmental noise and surface conditions such as vibration, surface reflectance, and surface contamination, making it suitable for measuring highly reflective or transparent surfaces that are hard to measure with non-contact measurement techniques. Also, this method allows for the measurement of various sample sizes within the scan range of the moving stage.

The major disadvantages of contact profilometry are that it requires too much time (tens of seconds in general) to get the full-field topology because extensive scanning is required to get the surface profile of the designated area, although the computation is simple [117]. Because it is too time-consuming and the stylus or probe must contact the surface of a sample, contact profilometry cannot be used for in-line measurements. In addition, because a contact profilometry system generally includes an accurate moving stage equipped with motors and encoders, the costs of the system increases.

6.2.2 Non-Contact Type

Non-Contact Profilometer

The non-contact profilometry usually uses a laser sensor, which is moved laterally by an accurate moving stage, for measuring the warpage of chip packages and boards. Non-contact profilometry provides high-resolution warpage results that can achieve micrometer scale resolution by applying the triangulation principle with simple computation. The optical setup of the system is relatively simple and inexpensive compared to the other non-contact measurement systems. The laser triangulation principle is insensitive to surface reflectance, enabling the measurements of multiple samples with different reflectance [151]. This method also allows for the measurement of various sample sizes within the range of motion of the moving stage. However, non-contact profilometry also has several disadvantages. First, extensive scanning, generally taking tens of seconds, is required to get the full-field topology, although this process is faster than contact profilometry. Even though this technique involves no contact, its correspondingly low measurement speed renders it unsuitable for in-line measurement. Second, the moving stage increases the costs of a system, and the mechanical movements reduce the calibration accuracy when using the laser triangulation principle. Third, if a coherent laser source is used, the laser speckle effect limits resolution when measuring rough surfaces.

Optical Interferometry

Optical interferometry measures the warapge of chip packages and PWBs using interference of two or more light waves. Twyman-Green and Fizeau interferometry are classical forms of interferometry that use the interference of coherent light, usually a laser.

Twyman-Green Interferometry

The advantages of Twyman–Green interferometry are that it is a non-contact and full-field technique and it produces high-resolution measurement capability comparable to the wavelength of a laser. This method's signal processing is relatively simple compared to other non-contact measurement techniques. On the other hand, the disadvantages of Twyman-Green interferometry are that the optical setup is very complex and expensive and the sample must be small (e.g., a flip chip) and have a mirror-like surface finish. The complex optical setup increases the calibration complexity and the sensitivity to vibration. Also, it is not suitable for in-line measurement due to its small full-field coverage area and limited sample application, constrained by the measurable size and reflectance of the sample surface [1, 70].

Fizeau Interferometry

Fizeau interferometry can be used to measure optically rough surfaces, such as the ground surface of silicon organic substrate, because it employs light with a long wavelength, which decreases the effects of the roughness and contamination of a sample surface [28]. Also, the Fizeau interferometer is much easier to tune and more robust to vibration and surface reflectance compared to the Twyman-Green interferometer because it has nearly identical reference and active light paths that permit a small gap to exist between the optical flat and the sample surface [27]. This method also requires relatively simple computation compared to other non-contact measurement techniques. The disadvantages of Fizeau interferometry are that it can only measure small samples, such as flip chips, and the optical setup is complex and expensive. In addition, it is unsuitable for in-line use due to its small full-field coverage area and limited sample applications [1].

Electronic Speckle Pattern Interferometry

To measure the warpage of chip packages and PWBs, ESPI uses a speckle pattern generated when a coherent light or laser beam is incident on a rough surface. The advantages of ESPI are that it has high-resolution and is a full-field and non-contact measurement technique. On the other hand, its primary disadvantage is that it requires a rather complex and computationally intensive algorithm, which decreases the measurement speed and increases the software cost. The speckle pattern images also have poor contrast and high levels of noise, which decrease the measurement accuracy. This method is sensitive to surface contamination and reflectance, as well as ambient noise due to vibration [152].

Digital Image Correlation

The digital image correlation is a full-field measurement technique that has the capability of measuring both the out-of-plane and in-plane deformations of a sample surface [34]. This method provides 1 μm scale resolution based on the triangulation principle. Its hardware is simple and inexpensive, and the measurement speed is relatively high because of its high data acquisition speed and moderate computational complexity without any mechanical movement [34]. Also, this method can measure various sample sizes. However, the digital image correlation method has several disadvantages. The optical system and the nonlinearity of the complementary metal-oxide semiconductor (CMOS) image sensor cause image distortion that affects calibration accuracy [37]. Because the surface profile is generated from the images captured by the two cameras, the measurement results are sensitive to surface reflectance and contamination. This method also is sensitive to initial calibration and mechanical

vibration during measurements because small changes in the relative camera positions can cause great measurement inaccuracy [48, 153].

Moiré Techniques

The moiré techniques use fringe patterns for measuring the warpage of chip packages and boards. The moiré techniques can be classified into three types based on how they generate the fringe patterns: shadow moiré, LFP, and DFP techniques.

Shadow Moiré

In comparison to other contact and non-contact measurement techniques, the shadow moiré technique has many strong advantages. First, it is a non-contact and full-field measurement method that is very suitable for in-line use. The shadow moiré technique also provides high-resolution for measuring warpage in both small and large samples. The master grating is fairly cheap when compared to the sub-system that produces fringe patterns in the LFP system. The specimen grating, the grating (or fringe pattern) produced on a specimen surface, is relatively insensitive to ambient vibration because the master grating is placed very close to the specimen surface.

However, the shadow moiré technique has a few disadvantages. First, it requires a master glass grating that must be placed very close to the surface of the sample whose warpage is to be measured, and this can affect the thermal behavior of the sample. The close proximity between the surfaces of the glass grating and the test sample makes it difficult to simultaneously measure the warpage of chip package(s) and PWB in a PWBA. Second, the mechanical moving parts for the phase shifting can easily introduce a phase-shifting error that decreases the calibration accuracy. Third, this method has limited sample application for in-line measurement because sample surfaces with shiny

or variable reflectance usually have to be painted white in order to produce fringe pattern with a sufficiently high contrast.

Laser fringe projection

The LFP (or projection moiré) technique has several advantages compared to the shadow moiré technique. First, because the LFP technique projects a fringe pattern onto a sample surface without a glass grating, it interferes less with the sample's thermal behavior and is suitable for simultaneously measuring the warpage of chip package(s) and PWB in a PWBA. Second, although the PZT's mechanical movements introduce a phase-shifting error, this error is less than that of the shadow moiré system because the PZT actuator is more accurate than the step or servo motors used in that method.

On the other hand, the LFP technique has several disadvantages compared to the shadow moiré technique. First, it requires a more complex optical setup necessitating a more complex calibration procedure. Second, it is not suitable for measuring the warpage of large samples accurately because its resolution decrease when its FOV increases. Third, LFP technique is more error-prone because of its non-uniform and noisy fringe patterns. Major source of noise in the fringe pattern is laser speckle produced by the laser interferometer.

Digital Fringe Projection

The DFP technique has many strong advantages compared to the shadow moiré and LFP techniques. First, it does not interfere with the sample's thermal behavior and is suitable for simultaneously measuring the warpage of chip package(s) and PWB in a PWBA because it does not require a master grating, as does the shadow moiré technique. Second, because it shifts the fringe pattern digitally, not mechanically, no phase shifting

error occurs as in the other moiré techniques. Third, the fringe image produced by DFP does not have the laser speckle noise that is produced by the laser in the LFP technique. Fourth, a DFP system is cheaper than an LFP system because DFP only requires a camera and a digital projector with simple optical elements.

The major disadvantage of the DFP technique, compared to the shadow moiré and LFP techniques, arises because the digitally projected fringes produce non-ideal sinusoidal waveforms in the fringe image, which potentially cause measurement uncertainties. Also, as with the LFP technique, the DFP technique is not suitable for measuring the warpage of large samples accurately because its resolution decrease when its FOV increases.

6.3 Selection Guideline of Warpage Measurement Techniques

The levels of the primary factors of each feature are listed in Table 6.3. The level assigned to each primary factor was determined by a relative comparison of the real primary factor (e.g. practical resolution) or qualitative information provided in the previous section.

The levels of the features of ten measurement techniques are listed in Table 6.4. The level assigned to each feature was determined by averaging the levels of the primary factors of each feature listed in Table 6.3. Among the eight features, resolution, coverage area, speed, costs, and accuracy have practical values. The practical ranges of each level (0, 1, 2, 3, or 4) of those features are provided in Table 6.5.

Table 6.3. The levels of the primary factors that determine each measurement feature

Feature	Primary Factor	Contact		Non-Contact Type							
		GIS	CP	NCP	Optical Interferometry			DIC	Moiré Techniques		
					TGI	FI	ESPI		SM	LFP	DFP
Resolution[a]	Practical Resolution	0	4	3	4	2	4	3	4	2	3
Coverage Area	Full-field Coverage Area or Maximum Scan Range	4[b]	3	3	1	1	0	3	4	3	3
Speed	Full-field Coverage Area	0	0	0	1	1	0	4	4	3	3
	Data Acquisition Speed	1	0	0	3	3	3	4	3	3	3
	Computation Speed	1	3	3	3	3	1	2	3	2	1
Costs[a]	Cost of Positioning Stage and Actuator	4	1	1	4	4	4	4	2	3	4
	Cost of Sensor Components	4	3	3	1	1	1	3	3	2	3
	Cost of Software	4	3	3	3	3	2	1	2	2	1
Accuracy[a]	Practical Resolution	0	4	3	4	2	4	3	4	2	3
	Calibration Accuracy	0	3	2	2	3	1	1	2	2	2
Flexibility	Insensitivity to Surface Reflectance	4	3	3	1	3	1	1	2	2	3
	Ability to Measure Various Sample Sizes	3	3	3	1	1	0	3	4	3	3
	Ability to Measure PWBA	0	0	1	0	0	0	3	1	4	4
Robustness	Insensitivity to Surface Contamination	4	3	2	1	3	1	1	2	2	2
	Insensitivity to Vibration	4	3	2	2	3	1	1	2	2	2
	Insensitivity to Manual Operation	0	1	1	4	4	4	4	4	4	4
In-Line Capability	Contact (C) or Non-Contact (N)	C	C	N	N	N	N	N	N	N	N
	Full-field Coverage Area[c]	0	0	0	1	1	2	4	4	4	4
	Data Acquisition Speed[c]	1	0	0	3	3	3	4	3	3	3
	Computation Speed[c]	1	3	3	3	3	1	2	3	2	1
	Insensitivity to Surface Contamination	4	3	2	1	3	1	1	2	2	2
	Insensitivity to Vibration	4	3	2	2	3	1	1	2	2	2
	Ability to Measure Unpainted Sample	4	3	3	1	3	1	1	2	2	3

0: Very Low, 1: Low, 2: Moderate, 3: High, 4: Very High, GIS: gauge indicator shim method, CP: contact profilometer, NCP: non-contact profilometer, TGI: twyman-green interferometry, FI: fizeau interferometry, ESPI: electronic speckle pattern interferometry, DIC: digital image correlation, SM: shadow moiré, LFP: laser fringe projection, DFP: digital fringe projection. [a]A higher level indicates lower actual value, [b]The level of the maximum measurable sample size, [c]Primary factors of speed.

Table 6.4. The features levels of ten measurement techniques

Feature	Contact Type		Non-Contact Type							
	GIS	CP	NCP	Optical Interferometry			DIC	Moiré Techniques		
				TGI	FI	ESPI		SM	LFP	DFP
Resolution[a]	0.0	4.0	3.0	4.0	2.0	4.0	3.0	4.0	2.0	3.0
Coverage Area[a]	4.0	3.0	3.0	1.0	1.0	0.0	3.0	4.0	3.0	3.0
Speed[a]	0.7	1.0	1.0	2.3	2.3	1.3	3.3	3.3	2.7	2.3
Costs[a]	4.0	2.3	2.3	2.7	2.7	2.3	2.7	2.3	2.3	2.7
Accuracy[a]	0.0	3.5	2.5	3.0	2.5	2.5	2.0	3.0	2.0	2.5
Flexibility[a]	2.3	2.0	2.3	0.7	1.3	0.3	2.3	2.3	3.0	3.3
Robustness[a]	2.7	2.3	1.7	2.3	3.3	2.0	2.0	2.7	2.7	2.7
In-Line Capability[a,b]	0.0	0.0	1.7	1.8	2.7	1.5	2.2	2.7	2.5	2.5
Practical Resolution (μm)	38.1	< 0.1	2	0.32	5.3	< 1	1	0.83[c]	6[d]	2.5[d]
Corresponding FOV (mm)	N/A	Up to 150× 150	63× 63	5.6× 5.6	6×4	2×3	45× 34	Up to 600× 600	60× 45	25× 25

[a]4.0 Scale, [b]The in-line capability of a contact type technique is zero, [c]For 300 lines/inch grating, [d]The practical resolution depends on the corresponding FOV.

Table 6.5. The practical ranges of resolution, coverage area, speed, costs, and accuracy

Feature	Practical Ranges of Each Level (0-4)[a]				
	0	1	2	3	4
Resolution (μm)	> 20	10-20	5-10	1-5	< 1
Coverage Area (mm)	< 5×5	5×5- 10×10	10×10-25×25	25×25- 200×200	> 200×200
Speed (seconds)	> 60	8-60	5-8	2-5	< 2
Costs[b] ($)	> 400k	300k-400k	200k-300k	100k-200k	< 100k
Accuracy (%)	> 15	9-15	3-9	1-3	< 1

[a]4: Very High, 3: High, 2: Moderate, 1: Low, 0: Very Low, [b]Estimated ranges of costs including reflow oven.

The following steps can be used as a guideline for selecting the most suitable warpage measurement technique for a particular application:

1) Using Table 6.5, determine the required levels of resolution, coverage area, speed, costs, and accuracy for the particular application. For example, if the application requires resolution of 2 μm, the required level of the resolution is 3.

2) Assign the required levels of the primary factors of flexibility, robustness, and in-line capability. For example, if the sample surface is painted and has uniform reflectance, the required level of the insensitivity to surface reflectance can be 0 (very low).

3) Determine the required levels of flexibility, robustness, and in-line capability by averaging the required levels of their primary factors assigned in step 2.

4) Select the most suitable technique by comparing the required feature levels determined in the previous steps and the feature levels of ten warpage measurement techniques provided in Table 6.4.

For example, assuming a need to purchase a system to measure the warpage of chip packages during the reflow process with the following requirements and conditions:

- Required resolution: less than 1 μm
- Budget: $250k
- Required accuracy: less than 5 %
- Required time for measuring one sample: less than 4 seconds
- Sample sizes: 20×20 mm, 30×30 mm, and 40×40 mm
- Spray painting on sample surface can be used

- Non-contact technique is required
- Will be measured in a clean room
- Will be operated with an unskilled operator,

the most suitable measurement technique can be selected by following the steps of the selection guideline listed below:

1) Using Table 6.5, the required levels of resolution, coverage area, speed, costs, and accuracy are determined as 4, 3, 3, 2, and 2, respectively.

2) The required levels of the primary factors of flexibility, robustness, and in-line capability are assigned, as listed in the Table 6.6.

3) The required levels of flexibility, robustness, and in-line capability are determined by averaging the levels of their primary factors assigned in step 2. The determined levels of flexibility, robustness, and in-line capability are 1, 1.3, and 2, respectively, as listed in Table 6.6.

4) By comparing the required feature levels determined in the previous steps and the feature levels of ten warpage measurement techniques provided in Table 6.4, shadow moiré is selected as the most suitable technique for the application, because only it covers the required feature levels. Table 6.7 is used for the comparison. (If more than one technique covers the required feature levels, select one of them considering more important features for the application. If no technique covers the required feature levels, adjust the requirements of the application and repeat the steps of the selection guideline.)

Table 6.6. Table for assigning the levels of flexibility, robustness, and in-line capability

Feature	Primary Factor	Required Level[a]	Average[b]
Flexibility	Insensitivity to Surface Reflectance	0	1
	Ability to Measure Various Sample Sizes	3	
	Ability to Measure PWBA	0	
Robustness	Insensitivity to Surface Contamination	0	1.3
	Insensitivity to Vibration	0	
	Insensitivity to Manual Operation	4	
In-Line Capability	Contact (C) or Non-Contact (N)	N	0.8
	Speed[c]	3	
	Insensitivity to Surface Contamination	0	
	Insensitivity to Vibration	0	
	Ability to Measure Unpainted Sample	0	

[a]4: Very High, 3: High, 2: Middle, 1: Low, and 0: Very Low; [b]Feature level, [c]4: <2 sec, 3: 2-5 sec, 2: 5-8 sec, 1: 8-60 sec, and 0: >60 sec.

Table 6.7. The required feature levels for the particular application and the feature levels of ten warpage measurement techniques

Feature	Required Feature Level	Contact Type		Non-Contact Type							
		GIS	CP	NCP	Optical Interferometry			DIC	Moiré Techniques		
					TGI	FI	ESPI		SM	LFP	DFP
Resolution	**4.0**	0.0	4.0	3.0	4.0	2.0	4.0	3.0	4.0	2.0	3.0
Coverage Area	**3.0**	4.0	3.0	3.0	1.0	1.0	0.0	4.0	4.0	3.0	3.0
Speed	**3.0**	0.7	1.0	1.0	2.3	2.3	1.3	3.3	3.3	2.7	2.3
Costs	**2.0**	4.0	2.3	2.3	2.7	2.7	2.3	2.7	2.3	2.3	2.7
Accuracy	**2.0**	0.0	3.5	2.5	3.0	2.5	2.5	2.0	3.0	2.0	2.5
Flexibility	**1.0**	2.3	2.0	2.3	0.7	1.3	0.7	2.3	2.3	3.0	3.3
Robustness	**1.3**	2.7	2.3	1.7	2.3	3.3	2.0	2.0	2.7	2.7	2.7
In-Line Capability	**0.8**	0.0	0.0	1.7	1.8	2.7	1.5	2.2	2.7	2.5	2.5

A higher level indicate better feature.

6.4 Chapter Summary

As chip packages and boards diversify, choosing the most suitable warpage measurement technique for a particular application presents a challenge for manufacturing engineers. The purpose of this study was to develop a guideline for engineers to use in selecting the most appropriate warpage measurement technique for a designated application. To create the guideline, eight features important for warpage measurement were defined and the feature levels of ten warpage measurement techniques were determined. Using this information, a selection guideline for warpage measurement techniques was developed, and an example of how to use the guideline was provided. The guideline will help manufacturing engineers select the most suitable warpage measurement technique for a particular application.

CHAPTER 7

CONCLUSIONS

The research objectives, approaches, and results of each research area are summarized in this chapter. Also, the major contributions of the research are presented. Finally, recommendations for future work are provided.

7.1 Conclusions

The warpage of chip packages and PWBs is a common thermomechanical reliability concern in electronic packaging. The overall goals of this research were to develop a warpage measurement system capable of measuring the warpage of painted and unpainted chip packages and boards and to study the effects of solder bump pitch, package size, and molding compound and substrate thicknesses on PBGA warpage using the FEA.

The first objective was to improve the measurement capabilities of the LFP system by reducing its laser speckle noise and post-processing time. In previous warpage measurement research performed at the AEPL, an LFP system was developed and used to measure the warpage of chip packages and PWBs in PWBAs. The major disadvantage of the LFP system is its laser speckle noise, which decreases measurement accuracy and repeatability. In order to reduce the laser speckle noise, the Taguchi's DOE method, the ANOVA, and the regression method were used to optimize the control parameters (laser power, camera exposure, and camera gain). The optimum values of the laser power, camera exposure, and camera gain were determined to be 57 mw, 25 ms and 0 db,

respectively. This optimization improved the measurement accuracy and repeatability of the LFP system by 26.5 % and 10.1 %, respectively.

When measuring a PWBA, the LFP system generates a PWBA displacement image that contains the surface height variation of the sample. During the post-processing of the LFP system, the chip package and PWB regions in the PWBA displacement image need to be automatically segmented for measuring the separate warpage of the chip package(s) and PWB. In order to reduce the post-processing time of the LFP system, a fast automatic segmentation method, the RGM, was developed. Comparison results showed that the RGM is 43.6 % or 40.2 % faster than the current automatic segmentation method for segmenting one or two packages, respectively.

The second objective was to develop a DFP system for measuring the warpage of painted and unpainted chip packages and boards. With advances in digital projection technology, the DFP technique has become popular for measuring such warpage. In comparison to the LFP technique, the DFP technique does not have laser speckle, and it is easier to control because it uses a digital projector instead of a laser interferometer. However, the gamma nonlinearity of the digital projector in the DFP technique introduces a different source of error. A DFP system that includes customized software for measuring the warpage of painted chip packages and boards was developed. To compare the measurement capabilities of the LFP and DFP systems, the experimental results obtained with the DFP and LFP systems were compared. The results showed that the DFP system has several advantages over the LFP system. For example, the fringe images obtained with the LFP system contained more non-ideal sinusoidal waveforms, resulting in more measurement errors than those obtained with fringe images from the

DFP system. In addition, the measurement results obtained from the calibration block showed that the DFP system has higher practical resolution, better accuracy, and better repeatability than the LFP system. Further, the results obtained by using the DFP system to measure the warpage of the PWBA were closer to those obtained with the contact profilometer than were the LFP results. On the other hand, the DFP system involved more processing time than the LFP system because the DFP system requires additional time to generate the sinusoidal fringe pattern. Nevertheless, based on our comparative analysis, the DFP system appears to have more desirable features for measuring warpage than the LFP system.

This work also developed the novel DDFP technique for measuring the warpage of unpainted PBGA packages and boards. The DDFP technique generates and projects a dynamic fringe pattern, in which proper fringe intensity distributions are dynamically determined based on the coordinates and the surface reflectance of PBGA packages and PWBs. This technique includes a method to segment the PBGA package and PWB regions in an unpainted PWBA image, as well as calibration methods to compensate for coordinate and intensity mismatches between projected and captured images. Experimental results showed that the DFP system successfully measured the warpage of the PBGA packages and PWBs in unpainted PWBAs and that, compared to the contact profilometer, DDFP produced a measurement error of less than 8 %.

The third objective was to assess the effects of solder bump pitch, package size, and molding compound and substrate thicknesses on PBGA warpage after the reflow process using the FEA. The PBGA package is one of the most widely used chip packages in common electronic packaging devices, which has various I/O densities, sizes, and

thicknesses. Therefore, accurate prediction of PBGA warpage resulting from those parameters is required during PBGA design. This work used the FEA to carry out parametric studies to access the effects of solder bump pitch (F1), package size (F2), molding compound thickness (F3), and substrate thickness (F4) on PBGA warpage after the reflow process. The study employed the full-factorial DOE method to design simulations and the ANOVA to identify the effects of each factor on the maximum PBGA warpage (W_{max}) and the maximum curvature of PBGA warpage (K_{max}). This approach demonstrated that, for the particular PWBA model used, the orders of significance of the factors on W_{max} and K_{max} are F2, F3, F1, and F4. The regression method was used to obtain bilinear equations of W_{max} and K_{max} as functions of the four factors. The R^2 values of the bilinear equations were 99.73 % and 92.12 %, respectively.

The last objective was to develop a guideline for selecting the most suitable warpage measurement technique for a particular application. As the diversity of chip packages and boards increases, manufacturing engineers face more challenges in selecting the most appropriate warpage measurement technique for a particular application. In this study, a guideline was developed for manufacturing engineers to use in selecting a warpage measurement technique. Eight measurement features important for measuring the warpage were defined and the features of ten warpage measurement techniques were compared. The comparison results were used in the selection guideline.

7.2 Summary of Contributions

The details of the contributions and impacts of this research are as follow:

1) The measurement accuracy and repeatability of the LFP system were improved by optimizing the control parameters to minimize laser speckle noise. The optimization procedure used in this research can be adapted for any LFP system. In addition, the measurement speed of the LFP system was improved by developing a fast segmentation method, the RGM, to reduce the post-processing time. The RGM can be used for any shadow moiré, LFP, or DFP system.

2) The DFP system with a novel DDFP technique and customized software were developed for measuring the warpage of painted and unpainted chip packages and boards. The DDFP was the first technique of its kind for measuring the warpage of unpainted chip packages and boards. Because digital technologies advance rapidly, this new technique has great potential for measuring the warpage of unpainted chip packages and boards accurately and quickly in the assembly line, resulting in improved yields and quality for chip packages and boards.

3) Parametric studies were conducted to access the effects of solder bump pitch, package size, and molding compound and substrate thicknesses on the warpage of PBGA packages after the reflow process. The results of the study are expected to be used as guidelines that in-house PBGA designers can use to meet the warpage requirements for PBGA packages.

4) The selection guideline of warpage measurement techniques was developed by comparing the features of the various warpage measurement techniques. The guideline is

expected to help manufacturing engineers select the most appropriate warpage measurement technique for a particular application.

Overall, the research is expected to improve the yield and reliability of chip packages and boards, which will reduce manufacturing costs and time to market for chip packages and boards, and ultimately reduce the price of the end products.

7.3 Recommendations for Future Work

After the completion of this research, many challenging research topics remain to be explored, including the improvement of the DDFP technique and the DFP system for measuring the warpage of various chip packages and boards and further parametric studies for different types of chip packages. Some recommendations for future research work are listed below:

1) This study developed an automatic method to segment the PBGA package and PWB regions in an unpainted PWBA image. The segmentation method was designed for PWBAs that contain PBGA package(s) larger than 14×14 mm. However, there are various types and sizes of chip packages, and some are equal or less than 14×14 mm. In order to measure various types and sizes of chip packages, the segmentation method could be improved or a new segmentation method should be developed.

2) Higher resolution of the DFP system is needed to measure warpage more accurately. The simplest way to increase the resolution of the DFP system is to use higher resolution projector and camera. This change will also require modification of the software to control the higher resolution projector and camera and to process higher resolution images.

3) The DFP system needs an increased FOV to measure warpage of samples larger than 60×45 mm. Higher resolution projector and camera could be used to increase the FOV while maintaining the resolution of the DFP system. Alternatively an image stitching method could be used for the same purpose. In this case, the surface of a large sample is divided into multiple regions smaller than the FOV, displacement images of each region are obtained using the DFP system, and the displacement images are combined to produce one large displacement image containing the surface height variation of the entire sample. The disadvantages of this process are that it increases the measurement time and generally requires a moving stage to measure multiple regions of the sample surface.

4) The speed of the DFP system could be increased by further optimizing the software and using a higher performance computer. Also, because the four-step phase-shifting method requires the capture of four fringe images, which reduces the measurement speed, a faster method providing similar resolution with the four-step phase-shifting method could be developed. In addition, for faster data acquisition, the projector and the camera of the DFP system could be exactly synchronized using additional hardware directly connected between the projector and the camera.

5) Parametric studies to investigate the effects of four geometric factors (solder bump pitch, package size, and molding compound and substrate thicknesses) on PBGA warpage were performed. The effects of those factors on various chip packages such as chip scale packages could be investigated. Material properties such as CTE and elastic modulus also could be explored to study the combined effects of the materials' properties on the warpage of chip packages.

6) 3-D packages are a recent development for obtaining higher integration and performance of chip packages. Detailed investigation into the warpage behavior of 3-D packages needs to be conducted to ensure the manufacture of high-reliability and low-cost 3-D packages.

APPENDIX A

C PROGRAM CODE FOR THE RGM

```
bool RGM(CBuffer *DispImg, CBuffer *RegionImg)
{
	int i,j;
	BYTE *DispData = DispImg->GetData();
	BYTE *RegionData = RegionImg->GetData();
	int Width = DispImg->GetWidth();
	int Height = DispImg->GetHeight();
	int RegionCount = 0;
	BYTE *RegionLabel = new BYTE[5];
	for(i=0; i<5; i++) RegionLabel[i] = 250-i*50;
	for(i=0; i<Width*Height; i++) RegionData[i] = 0;
	GaussianFilter(DispData, Width, Height);

	for(i=0; i<Height; i++)
	{
		for(j=0; j<Width; j++)
		{
			if(RegionData[i*Width+j] == 0)
			{
				if(RegionGrowing(DispData, Width, Height, RegionData,
				RegionLabel[RegionCount], CPoint(j,i))) RegionCount++;
				if(RegionCount >= 4) goto END;
			}
		}
	}
	for(i=0; i<Width*Height; i++) if(RegionData[i] == 1) RegionData[i] = 0;
	END:
	return true;
}

bool RegionGrowing(unsigned char *SrcData, int Width, int Height, unsigned char *RegionData, unsigned
char LabelValue, CPoint Seed)
{
	short *RegionPixel_X;
	short *RegionPixel_Y;
	RegionPixel_X = new short[1280*960*10];
	RegionPixel_Y = new short[1280*960*10];
	int NumRegionPixel=0;
	int IndexRegionPixel=0;
	int CurrentIndex, NeighborIndex, i;

	RegionPixel_X[NumRegionPixel] = (short)Seed.x;
	RegionPixel_Y[NumRegionPixel] = (short)Seed.y;
```

```
NumRegionPixel++;
RegionData[RegionPixel_Y[0] * Width + RegionPixel_X[0]] = LabelValue;

while(IndexRegionPixel < NumRegionPixel)
{
	CurrentIndex = RegionPixel_Y[IndexRegionPixel] * Width +
			RegionPixel_X[IndexRegionPixel];

	// Left
	if(RegionPixel_X[IndexRegionPixel] - 1 >= 0)
	{
		NeighborIndex = CurrentIndex - 1;
		if(RegionData[NeighborIndex] == 0)
		{
			if(abs(SrcData[NeighborIndex] - SrcData[CurrentIndex]) < 2)
			{
				RegionData[NeighborIndex] = LabelValue;
				RegionPixel_X[NumRegionPixel] =
					RegionPixel_X[IndexRegionPixel] - 1;
				RegionPixel_Y[NumRegionPixel] =
					RegionPixel_Y[IndexRegionPixel];
				NumRegionPixel++;
			}
		}
	}

	// Right
	if(RegionPixel_X[IndexRegionPixel] + 1 < IMGX)
	{
		NeighborIndex = CurrentIndex + 1;
		if(RegionData[NeighborIndex] == 0)
		{
			if(abs(SrcData[NeighborIndex] - SrcData[CurrentIndex]) < 2)
			{
				RegionData[NeighborIndex] = LabelValue;
				RegionPixel_X[NumRegionPixel] =
					RegionPixel_X[IndexRegionPixel] + 1;
				RegionPixel_Y[NumRegionPixel] =
					RegionPixel_Y[IndexRegionPixel];
				NumRegionPixel++;
			}
		}
	}

	// Upper
	if(RegionPixel_Y[IndexRegionPixel] - 1 >= 0)
	{
		NeighborIndex = CurrentIndex - Width;
		if(RegionData[NeighborIndex] == 0)
```

```
		{
			if(abs(SrcData[NeighborIndex] - SrcData[CurrentIndex]) < 2)
			{
				RegionData[NeighborIndex] = LabelValue;
				RegionPixel_X[NumRegionPixel] =
					RegionPixel_X[IndexRegionPixel];
				RegionPixel_Y[NumRegionPixel] =
					RegionPixel_Y[IndexRegionPixel] - 1;
				NumRegionPixel++;
			}
		}
	}

	// Lower
	if(RegionPixel_Y[IndexRegionPixel] + 1 < IMGY)
	{
		NeighborIndex = CurrentIndex + Width;
		if(RegionData[NeighborIndex] == 0)
		{
			if(abs(SrcData[NeighborIndex] - SrcData[CurrentIndex]) < 2)
			{
				RegionData[NeighborIndex] = LabelValue;
				RegionPixel_X[NumRegionPixel] =
					RegionPixel_X[IndexRegionPixel];
				RegionPixel_Y[NumRegionPixel] =
					RegionPixel_Y[IndexRegionPixel] + 1;
				NumRegionPixel++;
			}
		}
	}

	IndexRegionPixel++;
}

int Skip = 0;
CRect Rect = CRect(2000,2000,0,0);

for(i=0; i<NumRegionPixel; i++)
{
	if(RegionPixel_X[i] < Rect.left) Rect.left = RegionPixel_X[i];
	if(RegionPixel_X[i] > Rect.right) Rect.right = RegionPixel_X[i];
	if(RegionPixel_Y[i] < Rect.top) Rect.top = RegionPixel_Y[i];
	if(RegionPixel_Y[i] > Rect.bottom) Rect.bottom = RegionPixel_Y[i];
}

int Area = Rect.Width() * Rect.Height();
if(NumRegionPixel < 50000) Skip = 1;
else if(Area < 50000) Skip = 1;
else if(LabelValue != 250 && NumRegionPixel < Area * 0.7) Skip = 1;
```

```
	if(Skip == 1)
	{
		for(i=0; i<NumRegionPixel; i++)
			RegionData[RegionPixel_Y[i] * Width + RegionPixel_X[i]] = 1;
		delete [] RegionPixel_X;
		delete [] RegionPixel_Y;
		return false;
	}
	delete [] RegionPixel_X;
	delete [] RegionPixel_Y;
	return true;
}

bool GaussianFilter(unsigned char *SrcData, int Width, int Height)
{
	int i, j, m, n, q;
	double GaussianMask[25] =
		{2./159, 4./159, 5./159, 4./159, 2./159,
		4./159, 9./159, 12./159, 9./159, 4./159,
		5./159, 12./159, 15./159, 12./159, 5./159,
		4./159, 9./159, 12./159, 9./159, 4./159,
		2./159, 4./159, 5./159, 4./159, 2./159};

	double FilteredValue = 0;
	int Offset = 5/2;
	unsigned char *DataWindow;
	int KernelSize = 5;
	unsigned char *DestData = new unsigned char[Width*Height];

	for(i=Offset; i<Height-Offset; i++)
	{
		for(j=Offset; j<Width-Offset; j++)
		{
			DataWindow = SrcData + (i-Offset) * Width + (j-Offset);
			FilteredValue = 0;

			for(m=0; m<KernelSize; m++)
			{
				for(n=0; n<KernelSize; n++)
				{
					FilteredValue +=
					GaussianMask[m*KernelSize+n] *
					DataWindow[m*Width+n];
				}
			}
			DestData[i*Width+j] = (BYTE)FilteredValue;
		}
	}
```

```
        for(q=0; q<Height*Width; q++) SrcData[q] = DestData[q];
        delete[] DestData;
        return true;
}
```

APPENDIX B

APDL CODE FOR THE PARAMETRIC STUDY

```
/PREP7

!*************************************************************************
!******* PARAMETERS
!*************************************************************************

incc = 1e-12
solder_mesh_fine_num = 4
solder_mesh_rough_num = 2

solder_pit = 1.5
substrate_dx = 45/2
substrate_dy = 45/2
molding_dz = 0.68
substrate_dz = 0.26

chip_dx = 5/2
chip_dy = 5/2
chip_dz = 0.3

solder_dia = 0.75
solder_hgt = 0.7

molding_dx = 42/2
molding_dy = 42/2

solder_num = 15

solder_offx = substrate_dx-(solder_num-0.5)*solder_pit
solder_offy = substrate_dy-(solder_num-0.5)*solder_pit

pwb_dx = 45/2
pwb_dy = 45/2
pwb_dz = 0

pwb_ox = 0
pwb_oy = 0
pwb_oz = 0

solder_ox = solder_pit/2
solder_oy = substrate_dy-solder_offy
solder_oz = pwb_oz+pwb_dz+solder_hgt/2
```

```
substrate_ox = 0
substrate_oy = 0
substrate_oz = solder_oz+solder_hgt/2

chip_ox = 0
chip_oy = 0
chip_oz = substrate_oz+substrate_dz

molding_ox = 0
molding_oy = 0
molding_oz = substrate_oz+substrate_dz

!*********************************************************************************
!******** GEOMETRIC MODELING
!*********************************************************************************

!******** PWB

BLC4,0,0,pwb_dx,pwb_dy

!******** Substrate

BLOCK,substrate_ox,substrate_ox+substrate_dx,substrate_oy,substrate_oy+substrate_dy,substrate_oz,subs
trate_oz+substrate_dz
NUMCMP,volu

!******** Molding

BLOCK,molding_ox,molding_ox+molding_dx,molding_oy,molding_oy+molding_dy,molding_oz,molding
_oz+molding_dz
BLOCK,chip_ox,chip_ox+chip_dx,chip_oy,chip_oy+chip_dy,chip_oz,chip_oz+chip_dz
VSBV,2,3,,delete,delete silicon die space
NUMCMP,volu

!******** Chip

BLOCK,chip_ox,chip_ox+chip_dx,chip_oy,chip_oy+chip_dy,chip_oz,chip_oz+chip_dz
NUMCMP,volu

!******** Solder Ball

BLOCK,substrate_ox,substrate_ox+substrate_dx,substrate_oy,substrate_oy+substrate_dy,pwb_oz,pwb_oz-
solder_hgt
NUMCMP,volu
SPH4,solder_ox,solder_oy,solder_dia/2

VSEL,s,volu,,5
VGEN, ,all, , ,0,0,solder_oz, , ,1
```

```
VSEL,s,volu,,5
VSEL,a,volu,,4
VSBV,5,4,,DELETE,DELETE
NUMCMP,volu

VSEL,s,volu,,4
VSEL,a,volu,,1
VSBV,4,1,,DELETE,KEEP
NUMCMP,volu

VSEL,s,volu,,4
VGEN,solder_num,all,,,solder_pit
VSEL,s,loc,z,pwb_oz,pwb_oz+solder_hgt
VGEN,solder_num,all,,,,-solder_pit
NUMCMP,volu

VSEL,all
VGLUE,all

ASEL,S,LOC,X,pwb_ox,pwb_ox+pwb_dx
ASEL,R,LOC,Y,pwb_oy,pwb_oy+pwb_dy
ASEL,R,LOC,Z,pwb_oz-0.01,pwb_oz+0.01
CM,solder_area,AREA
AOVLAP,solder_area

NUMCMP,volu
NUMCMP,area

!*********************************************************************************
!******** MATERIAL / ELEMENT MODELING
!*********************************************************************************

mat_solder = 1
mat_si = 2
mat_molding = 3
mat_fr4 = 4
mat_cu = 5
mat_bt = 6

!******** FR-4

MPTEMP
MPTEMP,1,303,368,383,398,423,543
MPDATA,EX,mat_fr4,1,22400,20680,19970,19300,17920,16000
MPDATA,EY,mat_fr4,1,22400,20680,19970,19300,17920,16000
MPDATA,EZ,mat_fr4,1,22400,20680,19970,19300,17920,16000
MPDATA,NUXY,mat_fr4,1,0.1360,0.1360,0.1360,0.1360,0.1360,0.1360
MPDATA,NUXZ,mat_fr4,1,0.1425,0.1425,0.1425,0.1425,0.1425,0.1425
MPDATA,NUYZ,mat_fr4,1,0.1425,0.1425,0.1425,0.1425,0.1425,0.1425
```

```
MPDATA,ALPX,mat_fr4,1,20e-6,20e-6,20e-6,20e-6,20e-6,20e-6
MPDATA,ALPY,mat_fr4,1,20e-6,20e-6,20e-6,20e-6,20e-6,20e-6
MPDATA,ALPZ,mat_fr4,1,86.5e-6,86.5e-6,243e-6,400.e-6,400.e-6,400.e-6
MPDATA,GXY,mat_fr4,1,630,600,550,500,450,441
MPDATA,GXZ,mat_fr4,1,199,189,173,157,142,139.3
MPDATA,GYZ,mat_fr4,1,199,189,173,157,142,139.3

!******** Silicon

MP,EX,mat_si,160000
MP,NUXY,mat_si,0.23
MP,ALPX,mat_si,2.6e-6
MP,GXY,mat_si,65000
MP,DENS,mat_si,2.330e-6

!******** Solder Ball

MP, ALPX, mat_solder, 21.0E-6

MPTEMP
MPTEMP, 1, 248, 298, 358, 398

MPDATA, EX, mat_solder, 1, 27390, 19650, 15270, 11680
MPDATA, EY, mat_solder, 1, 27390, 19650, 15270, 11680
MPDATA, EZ, mat_solder, 1, 27390, 19650, 15270, 11680

MPDATA, GXY,mat_solder,1,9782,7018,5454,4171
MPDATA, GYZ,mat_solder,1,9782,7018,5454,4171
MPDATA, GXZ,mat_solder,1,9782,7018,5454,4171

MP, NUXY, mat_solder, 0.4
MP, NUYZ, mat_solder, 0.4
MP, NUXZ, mat_solder, 0.4

!******** Copper

MP,EX,mat_cu,79510
MP,PRXY,mat_cu,0.32
MP,ALPX,mat_cu,18.94e-6
MP,DENS,mat_cu,8.94e-6

!******** Molding

MP,EX,mat_molding,15000
MP,PRXY,mat_molding,0.15
MP,ALPX,mat_molding,17.5e-6
MP,DENS,mat_molding,3.0e-6

!******** BT
```

```
MP,EX,mat_bt,14000
MP,PRXY,mat_bt,0.15
MP,ALPX,mat_bt,15e-6
MP,DENS,mat_bt,3.0e-6

!******** Element Type

element_shell91 = 1
element_solid95 = 2

ET,element_shell91,SHELL91,,1
ET,element_solid95,SOLID95

!******** Element/Material Assignment

pwb_nls = 7
pwb_hgt = 0.631
*DIM,pwb_hls,ARRAY,pwb_nls
pwb_hls(1) = 0.018,0.127,0.018,0.305,0.018,0.127,0.018

R,element_shell91
RMODIF,element_shell91,1,pwb_nls                    ! 7 layers
RMODIF,element_shell91,19,mat_fr4,0,pwb_hls(2)      ! 2nd layer: FR-4
RMODIF,element_shell91,25,mat_fr4,0,pwb_hls(3)      ! 3rd later: copper
RMODIF,element_shell91,31,mat_fr4,0,pwb_hls(4)      ! 4th layer: FR-4
RMODIF,element_shell91,37,mat_fr4,0,pwb_hls(5)      ! 5th later: copper
RMODIF,element_shell91,43,mat_fr4,0,pwb_hls(6)      ! 6th layer: FR-4
RMODIF,element_shell91,13,mat_fr4,0,pwb_hls(1)      ! 1st later: copper trace
RMODIF,element_shell91,49,mat_fr4,0,pwb_hls(7)      ! 7th later: copper trace

ALLSEL
ASEL,S,LOC,Z,pwb_oz-incc,pwb_oz+incc
AATT,-1,element_shell91,element_shell91

ALLSEL
VSEL,S,LOC,Z,pwb_oz,pwb_oz+solder_hgt
VATT,mat_solder,-1,element_solid95

ALLSEL
VSEL,S,LOC,Z,substrate_oz,substrate_oz+substrate_dz
VATT,mat_bt,-1,element_solid95

ALLSEL
VSEL,S,LOC,Z,chip_oz,chip_oz+chip_dz
VSEL,U,LOC,Z,chip_oz+chip_dz-0.1,molding_oz+molding_dz+0.1
VATT,mat_si,-1,element_solid95

ALLSEL
```

```
VSEL,S,LOC,Z,chip_oz+chip_dz-0.1,molding_oz+molding_dz+0.1
VATT,mat_molding,-1,element_solid95

!*****************************************************************************
!******** MESHING / BOUNDARY CONDITIONS
!*****************************************************************************

SMRT,7
ASEL,S,LOC,Z,pwb_oz-incc,pwb_oz+incc
MSHKEY,0
MSHAPE,1,2D
AMESH,all

SMRT,7
VSEL,all
MSHKEY,0
MSHAPE,1,3D
VMESH,all

/SOLU
/NERR,,50000

allsel
nsel,s,loc,x,0
D,all,Ux,0
D,all,ROTY,0

allsel
nsel,s,loc,y,0
D,all,Uy,0
D,all,ROTX,0

allsel
nsel,s,loc,x,pwb_oz
nsel,r,loc,y,pwb_oy
nsel,r,loc,Z,pwb_oz
D,all,all,0

!*****************************************************************************
!******** SOLUTIONS
!*****************************************************************************

/SOLU
/UIS,MSGPOP,4
nlgeom,on
autots,on

TREF,298
TUNIF,423
```

```
allsel,all
TIME,100
SOLVE

/SOLU
TREF,423
TUNIF,456
allsel,all
TIME,80
SOLVE

/SOLU
TREF,456
TUNIF,488
allsel,all
TIME,70
SOLVE

/SOLU
TREF,488
TUNIF,298
allsel,all
TIME,100
SOLVE

!******** Warpage Calculation

/POST1
ALLSEL
VSEL,S,LOC,Z,substrate_oz,substrate_oz+substrate_dz
VSEL,A,LOC,Z,chip_oz,chip_oz+chip_dz
VSEL,A,volu,,1
ESLV,S
AVPRIN,0,0
ETABLE,tbl2,U,Z
ESORT,ETAB,tbl2,0,0
*GET,tmp_package_max,SORT,,MAX
*GET,tmp_package_min,SORT,,MIN
WARPAGE = tmp_package_max-tmp_package_min

/POST1
/DSCALE,ALL,30
allsel,all
/EFACET,1
PLNSOL, U,Z, 0,1.0
```

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