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Stabilizing Controller Design for a DC Power Distribution System Using A Passivity-Based Stability Criterion

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STABILIZING CONTROLLER DESIGN FOR A DC POWER DISTRIBUTION SYSTEM USING A PASSIVITY-BASED STABILITY CRITERION

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DEDICATION

To Rosalia, my dear wife for her warm support

and

To Samuele, my lovely son

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ABSTRACT

In modern times there has been an increased penetration of power electronic converters into Power Distribution Systems. In particular, there has been a strong interest in DC Power Distribution Systems as opposed to conventional AC Power Distribution Systems. These DC Power Distribution Systems are enabled by power electronics converters. The strong interest is motivated by improvements in power electronic converter technology, like advances in power semiconductor devices, magnetics, control, and converter topologies which have made possible to build high-performance converters at low cost. In many systems, such as cars, ships and airplanes, there has also been a trend towards the replacement of a number of older mechanical and hydraulic systems with electrical power-electronic-based systems, since these systems provide a number of advantages such as increased system flexibility, reliability, long life expectancy and decreased weight, size, and cost.

Together with these advantages, DC Power Distribution Systems offer system-level challenges related to system stability issues and design of individual converter controllers to guarantee proper operation of the interconnected system. System-level stability issues may arise due to interactions among feedback-controlled power converters, which are part of such a large interconnected system. These feedback-controlled power converters exhibit negative incremental input impedance within their control bandwidth. As a result, a power converter that was satisfactorily performing when

tested as a standalone unit may experience degradation in performance when connected as part of a system.

While the analysis and design of a single power converter and its controls is well understood, in a DC Power Distribution System the situation is different. Analyzing and designing a complex multi-converter system in such a way as to guarantee both system stability and performance is a complex problem that was not fully solved in the past. Difficulties stem from a lack of adequate analysis and design tools, limited understanding of the problem, difficulties in applying the existing stability criteria, and the need for stabilizing converter controllers. To tackle all these difficulties, the present work proposes two tools to address system level stability issues in DC Power Distribution Systems: the Passivity-Based Stability Criterion (PBSC) and the Positive Feed-Forward (PFF) control.

The PBSC is proposed as a tool for stability analysis in a DC Power Distribution System. The criterion is based on imposing passivity of the overall DC bus impedance. If passivity of the bus impedance is ensured, stability is guaranteed as well. The PBSC, which imposes conditions on the overall bus impedance, offers several advantages with respect to existing stability criteria, such as the Middlebrook criterion and its extensions, which are based on the minor loop gain concept, i.e. an impedance ratio at a given interface: reduction of artificial design conservativeness, insensitivity to component grouping, applicability to multi-converter systems and to systems in which the power flow direction changes, for example as a result of system reconfiguration. Moreover, the criterion is very designed-oriented because it can be used in conjunction with the second tool proposed in this dissertation, the PFF control, for the design of stabilizing virtual

damping networks. The PFF controller design formulation guarantees both stability and performance (a challenge not fully solved in the past, as previously stated). By designing the stabilizing virtual impedance so that the bus impedance passivity condition is met, the approach results in greatly improved stability and damping of transients on the DC bus voltage. Simulation validation is performed using a switching-level-model of the DC power distribution system. Experimental validation is carried out on a DC power distribution system built in the laboratory.

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CHAPTER 1

INTRODUCTION

First, this introductory chapter motivates this work by describing how stability is a significant design consideration in DC Power Distribution Systems. Second, a literature review of the state of the art in the stability analysis and improvement is provided. Third, the research objectives are stated, identifying the original contributions of the present work.

1.1. STABILITY ISSUES IN DC POWER DISTRIBUTION SYSTEMS

Although most power distribution systems over the terrestrial power grid use AC power, DC systems offer a number of advantages in a growing group of applications. In fact, in recent times DC Power Distribution Systems consisting of a network interconnection of feedback-controlled switching power converters are becoming increasingly common in industrial applications [1, 2], such as telecommunication systems, aircraft, electric cars, and in military applications, such as the power distribution system for the all-electric ship proposed by the US Navy [3-5]. The increased popularity of power electronics solutions is due to advances in power electronics technology, such as power semiconductor devices, magnetics, control, and converter topologies. Advantages of DC Power Distribution Systems are power interface flexibility due to feedback control, reduced weight and size, highly efficient energy conversion, possibility of high-frequency isolation, simpler implementation of power source paralleling (no

synchronization required), easy incorporation of DC-type renewable resources, and the ability to satisfy a variety of control objectives [5-7].

An example of DC Power Distribution System is the Medium Voltage DC (MVDC) Power Distribution for the US Navy All-Electric Ship, for which a new IEEE Standard has been recently released [8]. The single-bus MVDC Power Distribution System depicted in Fig. 1.1 is an example of a possible MVDC system topology described in the IEEE Standard. This system has a DC bus, shown in the center, powered by several power sources and power storage devices, such as turbine generators, fuel cells, batteries and flywheels, shown on the left hand side of the figure. The system supplies several loads, such as propulsion motors, actuators, sensors and power weapons, shown on the right hand side of the figure. These power sources, energy storage systems, and loads are all connected to the DC bus through feedback-controlled switching converters.

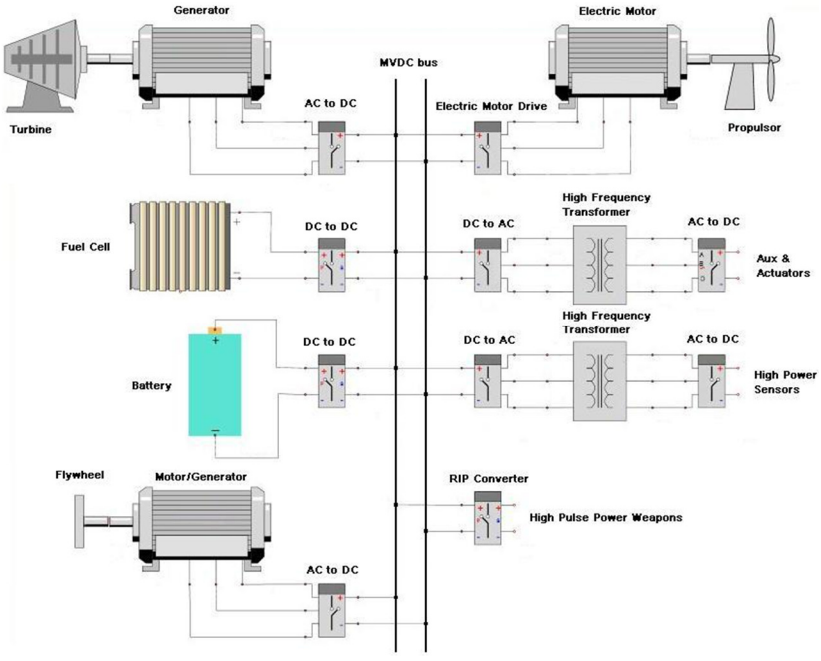


Figure 1.1. A simplified MVDC system diagram for an all-electric ship.

As a well-known challenge, DC Power Distribution Systems suffer from stability degradation caused by interactions among converters due to the constant power load (CPL) effect. Typically, feedback-controlled converters, such as feedback-controlled converters and inverters [6, 9-10], behave as CPLs at their input terminals within their control loop bandwidth [6, 10]. The CPLs exhibit negative incremental input impedance, which is cause of the subsystem interaction problem and origin of the undesired destabilizing effect [9]. Although each subsystem is independently designed to be standalone stable, a system consisting of many power-electronics-based subsystems, like that in Fig. 1.1, may exhibit degraded stability due to subsystem interactions caused by CPLs. This is because the subsystem interaction affects the bandwidth, the phase and the gain margin of each individual converter subsystem [11]. In the past, the subsystem interaction problem was not significant because an individual subsystem such as a tightly regulated converter operated under quasi-ideal conditions: low source impedance at its input and mainly passive loads at its output [12]. In DC Power Distribution Systems, the subsystem interaction is a serious issue, due to rapid increase in the use of interconnected power electronic converters and motor drives forming a large power distribution system.

1.2. STATE OF THE ART

To address system-level stability issues, several authors have studied the linearized system under steady state conditions by breaking it down into two subsystems: a source subsystem and a load subsystem defined at an arbitrary interface within the overall system. Fig. 1.2 shows the equivalent system broken down into two subsystems assumed to be individually stable. The total input-to-output transfer function is

$$G_{SL} = \frac{V_{out\_L}}{V_{in\_S}} = G_S G_L \cdot \frac{Z_{in\_L}}{Z_{in\_L} + Z_{out\_S}} = G_S G_L \cdot \frac{1}{1 + T_{MLG}} \tag{1.1}$$

where the minor loop gain T_{MLG} is defined as

$$T_{MLG} = \frac{Z_{out\_S}}{Z_{in\_L}} \tag{1.2}$$

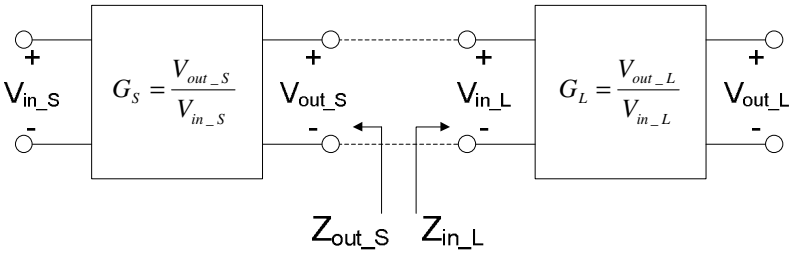


Figure 1.2. Equivalent source subsystem interaction with the equivalent load subsystem.

Since G_S and G_L are stable transfer functions, the minor loop gain term is the one responsible for stability. Therefore, a necessary and sufficient condition for stability of the system can be obtained by applying the Nyquist Criterion to T_{MLG}, i.e. the interconnected system is stable if and only if the Nyquist contour of T_{MLG} does not encircle the *(-1, 0)* point. Based on this concept many stability criteria for the interconnected system of Fig. 1.2 were proposed. These stability criteria define various forbidden regions for the polar plot of T_{MLG}. Fig. 1.3 shows the boundaries between forbidden and allowable regions. The forbidden regions are the ones that include the *(-1, 0)* point. System stability can be ensured by keeping the contour of T_{MLG} outside the forbidden regions. Based on the definition of the forbidden regions, design formulations can be specified. Note that these criteria give only sufficient, but not necessary stability conditions.

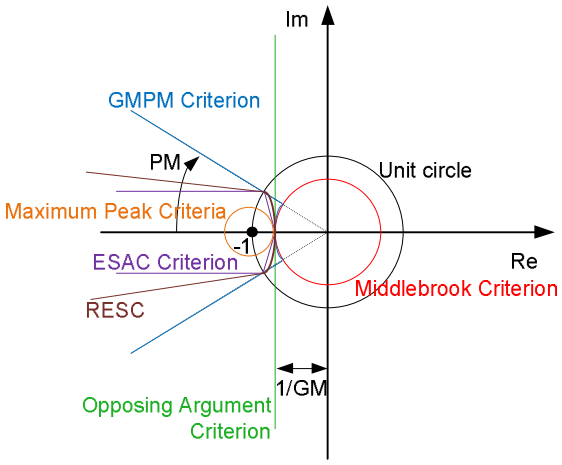


Figure 1.3. Stability Criteria boundaries.

1.2.1. Stability Analysis in DC Power Distribution Systems

To assess overall system stability, several stability criteria for DC systems based on forbidden regions for the minor loop gain have been proposed in the literature, such as the Middlebrook Criterion [13], and its various extensions, such as the Gain and Phase Margin (GMPM) Criterion [14], the Opposing Argument Criterion [15-17], the Energy Source Analysis Consortium (ESAC) Criterion [18, 19] and its extension, the Root Exponential Stability Criterion (RESC) [20]. All these criteria have been reviewed by the author in [21], which presents a discussion, for each criterion, of the artificial conservativeness of the criterion in the design of DC systems, and the design specifications that ensure system stability. Shortcomings of all these criteria (also discussed in [21]) are that they lead to artificially conservative designs, encounter difficulties when applied to multi-converter systems (more than two interconnected subsystems) especially in the case when power flow direction changes, and are sensitive to component grouping. Moreover, all these criteria, with the exception of the

Middlebrook Criterion, are not conducive to an easy design formulation. Another significant practical difficulty present with all the prior stability criteria is the minor loop gain online measurement [22]. It requires two separate measurements, source subsystem output impedance and load subsystem input impedance, and then some post-processing. Due to the complexity in the calculation, this approach is not suitable for online stability monitoring. (Only in the work [23], a practical approach to measure the stability margins of the minor loop gain was proposed. However, such an approach, based on the Opposing Argument Criterion, fails when used with other less conservative criteria.)

More recent stability criteria include the Three-Step Impedance Criterion (T-SIC) [24], the Unified Impedance Criterion (UIC) [25], and the Maximum Peak Criteria (MPC) [26, 27]. The T-SIC [24] relaxes the conservativeness of previous criteria because it does not assume that G_S in (1.1) is necessarily a stable transfer function, which is typical of regulated source subsystem. For this reason, the impedance criterion should not be applied on the minor loop gain defined in (1.2), but rather on an extended minor loop gain defined in [24]. All previous stability criteria were developed for source subsystem interaction alone or load subsystem interaction alone by using the Middlebrook's Extra Element Theorem (EET) [28]. Derived by using the two Extra Element Theorem (2EET) [29], the UIC [25], particularly suitable for cascade connected subsystems, constructs the minor loop gain considering the simultaneous interaction of both source and load subsystems. The last proposed stability criterion in order of time is the MPC [26, 27] which defines the minimum forbidden region for the minor loop gain among all prior stability criteria (Fig. 1.3). Such a forbidden region is determined by the maximum allowable peak of the sensitivity function, providing a direct measure of the stability

robustness. However, as also demonstrated in [26, 27], the state of the stability robustness strongly suffers from the interface where the minor loop gain is measured.

1.2.2. Stability Improvement in DC Power Distribution Systems

As an attempt to solve the stability degradation due to subsystem interaction problem in DC Power Distribution Systems, many approaches were proposed in the past. These approaches can be classified as either passive or active. Passive approaches, like the use of passive damping circuits and DC link capacitor banks [30], have disadvantages in term of cost, size, and weight, due to the addition of bulky passive components. Also, the increase of the bus capacitance may result in inrush current problems and poor dynamic output performance [30, 31]. An alternative to overcome all the disadvantages of passive approaches, active approaches, such as intermediate line filter [32], buck derived line conditioner [33], and active bus conditioner [34], and power buffering [35, 36], were proposed. However, all these techniques require additional power electronics, and have the drawback of a very complicated control scheme which is not practical for large multi-converter system.

Recently, active damping techniques which rely on the introduction of a virtual inductor ESR [37] and the introduction of a virtual DC-link capacitor [38, 39] have been proposed. These techniques provide solution for the load subsystem interaction only and the modification of the output (for [37]) and input (for [38, 39]) impedances, crucial for the system-level stability assessment, was not discussed. As an attempt to solve system-level stability issues in DC Power Distribution Systems, a State Feedback Linearization Technique [40, 41] has been presented. The method consists of linearizing the system (which is nonlinear due to the presence of CPLs) by the feedback of the nonlinear term

given by the CPLs themselves at the generating side of the system. However, an effective feedback linearization can be achieved only by oversimplifying the system model.

1.3. RESEARCH OBJECTIVES

The exigency to overcome all problems present with prior stability criteria and prior techniques for stability improvement motivates this work. In particular, the need for a less conservative and at the same time highly design-oriented stability criterion is crucial for DC Power Distribution Systems. Also, an effective active damping technique with simple implementation for system stability improvement is important. The present work presents two unique contributions: a novel Passivity-Based Stability Criterion (PBSC) for the system stability analysis, and a Positive Feed-Forward (PFF) control for the system stability improvement. Furthermore, the two contributions can be used together to form a unique framework which allows the engineer to have a system-level tool for on-line stability monitoring and a system-level tool for stability improvement.

1.3.1. THE PASSIVITY-BASED STABILITY CRITERION

To tackle all the difficulties typical of prior stability criteria, a novel PBSC is proposed and presented for the first time in [42]. The criterion is based on the passivity of the overall bus impedance rather than on the Nyquist Criterion applied to the minor loop gain. Like all prior stability criteria, the proposed criterion gives a sufficient condition [21] for the stability of two (or more) interacting subsystems being part of a larger DC Power Distribution System. The PBSC offers several advantages: reduction of artificial design conservativeness, insensitivity to component grouping, applicability to multi-converter systems and to systems in which the power flow direction changes, for example as a result of system reconfiguration. Moreover, it will be shown that the PBSC lends

itself to the design of stabilizing active impedances for DC Power Distribution Systems. In particular, the proposed criterion can be coupled with the PFF control [43, 44], to provide a control design method that ensures overall system stability and performance.

1.3.2. THE POSITIVE FEED-FORWARD CONTROL

To solve the stability degradation due to subsystem interactions, and in particular source subsystem interaction, the PFF control is proposed and presented in [43-48] as an active approach. The proposed approach combines an input voltage PFF control to the conventional negative FB control. The effect is the modification of the converter input impedance so that it now has two parallel components: one given by the FB control, and another actively introduced by the PFF control, both in parallel at the input port of the converter. While the PFF control stabilizes the input port, the Negative Feedback (NFB) control maintains the desired output regulation within its bandwidth. This approach is conceptually different from conventional Negative Feed-Forward (NFF) control [49-58], which is commonly introduced to compensate for input voltage variations, so that the output voltage is not affected. As a result, NFF control actually has a destabilizing effect at the input port of a converter by extending negative input impedance up to higher frequencies.

Compared with well-known passive approaches to this problem, such as damping circuits and large dc-link capacitors [30], the PFF control not only yields DC bus system stability improvement, but also guarantees good performance of the system. Compared with other active approaches, such as intermediate line filter [32], buck-derived line conditioner [33], and bus conditioner [34], which require additional power electronics with complicated control schemes, the PFF control has a much simpler implementation.

The PFF control method has so far been successfully applied to DC/DC converters [45, 46] and three-phase DC/AC inverters [47, 48]. In [45, 46] only an oversimplified PFF controller design procedure based on feedback (FB) and feed-forward (FF) control loop gains at low and high frequencies was presented. In the present work and also in [43, 44], the PFF control is designed using the proposed PBSC. In particular, by designing the virtual impedance introduced by the PFF control so that the bus impedance passivity condition is met, the approach results in greatly improved stability and damping of transients on the DC bus voltage.

CHAPTER 2

STABILITY ANALYSIS IN DC POWER DISTRIBUTION SYSTEMS

This chapter formalizes the PBSC, pointing out its main advantages. Since the PBSC offers only a sufficient condition for system stability, some investigation on the relationship between PBSC and Nyquist Criterion (which, instead, offers a necessary and sufficient condition for stability) is carried out. To overcome such a limitation, the concept of practical PBSC or Frequency-Bounded PBSC is proposed.

2.1. THE PASSIVITY-BASED STABILITY CRITERION

To better understand the main difference between the PBSC and all previous criteria, one can examine Fig. 2.1. The single-bus DC power distribution system in Fig. 2.1 (a) consists of n source converters and m load converters connected to the bus, a generalization of a system like the MVDC power distribution system for All-Electric Ships depicted in Fig. 1.1. By looking at the bus port, the given system can be reduced to an equivalent interacting source subsystem and load subsystem network (Fig. 2.1 (b)) and then to an equivalent 1-port network (Fig. 2.1 (c)). In Fig. 2.1(b) the source subsystem impedance is $Z_S=Z_1//...//Z_n$ and the load subsystem impedance is $Z_L= Z_{n+1}//…//Z_{n+m}$.

While all previous criteria have stopped at the step shown in Fig. 2.1 (b) defining the minor loop gain as $T_{MLG}=Z_S/Z_L$, the proposed PBSC combines together the two subsystems. The resulting 1-port network shown in Fig. 2.1 (c) seen from the DC bus port has an impedance $Z_{bus}(s)=V_{bus}(s)/I_{inj}(s)$, where $I_{inj}(s)$ is an injection current from an

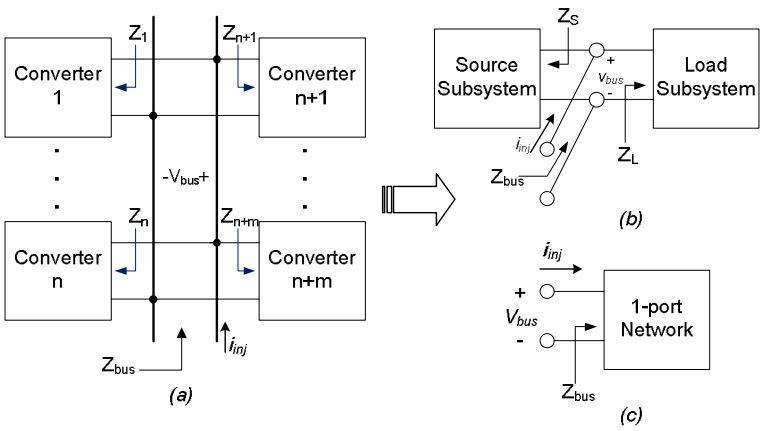


Figure 2.1. (a) Typical DC Power Distribution System with *n+m* converters, (b) equivalent interacting source subsystem and load subsystem network, and (c) equivalent 1-port network.

external bus-connected device used to perturb the bus. This impedance is clearly the parallel combination of all the converters' input/output impedances, i.e. $Z_{bus}=Z_S//Z_L=Z_1//.../Z_n//Z_{n+1}//.../Z_{n+m}$. The resulting network is passive if and only if:

1) $Z_{bus}(s)$ has no right half plane (RHP) poles, and

2) $Re\{Z_{bus}(j\omega)\}\geq 0, \forall \omega$.

Condition 2) is equivalent to $-90° \leq arg[Z_{bus}(j\omega)] \leq 90°, \forall \omega$, and corresponds to an impedance having positive real part at all frequencies. This also implies that the Nyquist contour of $Z_{bus}(j\omega)$ must lie wholly in the RHP. The phase of $Z_{bus}(j\omega)$ is the difference between the phase of the voltage $V_{bus}(j\omega)$ at the bus port and the phase of the current $I_{inj}(j\omega)$ injected into the port. If the phase of $Z_{bus}(j\omega)$ is between $-90°$ and $+90°$, the average power into the port is positive at all frequencies and therefore the system consumes energy (it is a passive system). If the phase is equal to $+90°$ or to $-90°$, the average power is zero, and the system is lossless. If the phase is less than $-90°$ or greater than $+90°$, the average power is negative and the system may produce energy (it is an active system).

A passive network consisting of an interconnection of passive elements has the property of being stable [59]. Therefore, the proposed Passivity-Based Stability Criterion (PBSC) for switching converter DC power distribution systems (Fig. 2.1 (a)) states that:

If the passivity condition (and therefore the phase constraint) is satisfied for $Z_{bus}(s)$, then the overall system consisting of the parallel combination of all the converters' input/output impedances (or equivalently of the two interacting subsystems) is stable.

The PBSC has several advantages over the minor-loop-gain-based stability criteria:

- It can easily handle multiple interconnected converters and inversion of power flow direction because what matters is only the parallel combination of all input/output impedances. Notice that for this reason, the PBSC is also insensitive to component grouping – typically a problem for the more conservative prior criteria.
- It reduces artificial design conservativeness typical of all prior stability criteria because the LHP of the Nyquist plot of $Z_{bus}(j\omega)$ is the "forbidden region". One does not need to consider encirclements of the *(-1, 0)* point.
- Unlike the minor loop gain online measurement, the bus impedance online measurement is easy to implement, does not require complex post-processing, and is suitable for system stability monitoring.
- The criterion lends itself to the design of virtual damping impedances which can be actively introduced in parallel at the bus load-side by the PFF control. The PFF controller is designed based on imposing passivity of the overall DC

bus impedance to provide a control design method that ensures system stability and performance.

2.2. CLASSICAL STUDY ON THE STABILITY OF INTERACTING SYSTEMS

The PBSC in its raw form gives only a sufficient condition for system stability. This means that if the Nyquist plot of the system bus impedance wholly lies on the RHP then the resulting system formed by a source interacting with a load subsystem is passive and therefore surely stable. However, if for some frequency the Nyquist plot of the system bus impedance goes to the LHP the resulting system can be not-strictly-passive or active, and therefore nothing can be stated about the stability of the system. This will be shown in the next section by an illustrative example. In this section, classical results on the passivity conditions for the stability of an interacting system like the one shown in Fig. 2.1 (b) are presented. The goal is to understand the limits of such classical results in the application of the PBSC for DC power distribution systems.

Impedance-based stability in a single bus DC power distribution system can be explained by using Fig. 2.2. The simplified circuital model is shown in Fig. 2.2 (a), while the equivalent block diagram is in Fig. 2.2 (b). Notice that the block diagram captures the concept of minor loop gain. The system consists of a source subsystem with Thévenin equivalent output impedance $Z_S(s)$ interacting at the bus port with a load subsystem with Thévenin equivalent input impedance $Z_L(s)$. An external device provides $\hat{i}_{inj}(s)$ as an injection current to perturb the bus for $Z_{bus}(s)$ measurement.

In the following, the stability of the system depicted in Fig. 2.2, and modeled according to (2.1), is addressed according to the classical analysis in [60]. The source subsystem output impedance $Z_S(s)$ is assumed to be passive.

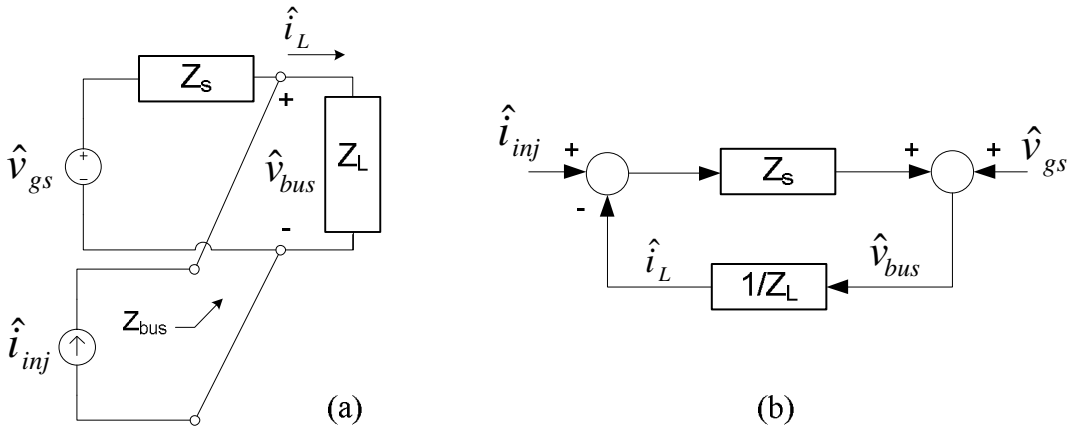


Figure 2.2. Thévenin equivant source and load subsystems: (a) circuital model, and (b) block diagram.

Moreover, the voltage source $\hat{v}_{gs}$ is assumed to be bounded. The interacting system of Fig. 2.2 is defined to be internally stable if each element of the following matrix is exponentially stable [61].

$$\begin{bmatrix} \hat{i}_L(s) \\ \hat{v}_{bus}(s) \end{bmatrix} = \begin{bmatrix} \dfrac{1}{Z_L(s)} \dfrac{Z_S(s)}{1+\dfrac{Z_S(s)}{Z_L(s)}} & \dfrac{1}{Z_L(s)} \dfrac{1}{1+\dfrac{Z_S(s)}{Z_L(s)}} \\ \dfrac{Z_S(s)}{1+\dfrac{Z_S(s)}{Z_L(s)}} & \dfrac{1}{1+\dfrac{Z_S(s)}{Z_L(s)}} \end{bmatrix} \begin{bmatrix} \hat{i}_{inj}(s) \\ \hat{v}_{gs}(s) \end{bmatrix} \tag{2.1}$$

For the given passive $Z_S(s)$, conditions on $Z_L(s)$ under which the coupled system in Fig. 2.2 is internally stable are given first. The input impedance of the load subsystem $Z_L(s)$ is assumed to be exponentially stable (coupled stability also assumes that isolated stability holds), which means that the load subsystem is stable when fed by an ideal voltage source (zero Thévenin equivalent source impedance). Assuming this condition is true, the interacting system is internally stable if and only if the term $Z_{bus}(s)=Z_S(s)/(1+Z_S(s)/Z_L(s))$ in (2.1) is exponentially stable [61]. Therefore, the

exponential stability of $Z_{bus}(s)$ implies the exponential stability of the other three terms in the matrix in (2.1).

Therefore, given a passive source subsystem output impedance $Z_S(s)$, the problem is now to find conditions for the load subsystem input impedance $Z_L(s)$ under which the port flow $\hat{i}_L(s)$ is exponentially stable. This is also sufficient to find conditions under which the transfer function $1/(1+Z_S(s)/Z_L(s))$ is exponentially stable. Reference [60] provides solution to such a problem by stating the following theorem.

For the system in Fig. 2.2, the source subsystem output impedance $Z_S(s)$ is assumed to be passive and the source voltage $\hat{v}_{gs}$ is bounded. Necessary and sufficient conditions for the port flow $\hat{i}_L(s)$ to be exponentially stable are:

1. *The load subsystem input impedance $Z_L(s)$ is exponentially stable, and*
2. *The load subsystem input impedance $Z_L(s)$ is strictly passive, i.e. $Re\{Z_L(j\omega)\}>0, \forall \omega$.*

As a consequence, if $Z_L(s)$ is strictly passive and $Z_S(s)$ is passive, then the parallel combination of $Z_L(s)$ and $Z_S(s)$ is passive and the Nyquist contour of the minor loop gain $T_{MLG}(j\omega)=Z_S(s)/Z_L(s)$ can never encircle the $(-1, 0)$ point. In fact, those conditions guarantee that $|arg[Z_S(j\omega)]|\leq 90^\circ \ \forall \omega$ and $|arg[Z_L(j\omega)]|<90^\circ \ \forall \omega$, and therefore $|arg[T_{MLG}(j\omega)]|<180^\circ \ \forall \omega$. Therefore, the Nyquist Criterion ensures that the poles of $1/(1+Z_S(s)/Z_L(s))$ lie on the LHP. As a consequence, $\hat{i}_L(s)$ is exponentially stable.

The bus impedance $Z_{bus}(s)$ is also passive, since

$$\begin{aligned}\mathrm{Re}\left[Z_{bus}(j\omega)\right] &= \mathrm{Re}\left[\frac{Z_S(j\omega)}{1+Z_S(j\omega)/Z_L(j\omega)}\right] \\ &= \mathrm{Re}\left[\frac{Z_S(j\omega)\cdot\left(1+Z_S^{\ *}(j\omega)/Z_L^{\ *}(j\omega)\right)}{\left|1+Z_S(j\omega)/Z_L(j\omega)\right|^2}\right] \\ &= \frac{\mathrm{Re}\left[Z_S(j\omega)\right]+\left|Z_S(j\omega)\right|^2\cdot\mathrm{Re}\left[1/Z_L(j\omega)\right]}{\left|1+Z_S(j\omega)/Z_L(j\omega)\right|^2} \geq 0, \forall\omega\end{aligned} \tag{2.2}$$

In practice, it often occurs that neither $Z_S(s)$ nor $Z_L(s)$ are passive at all frequencies. In particular, $Z_L(s)$ is usually the input impedance of a feedback-controlled switching converter and exhibits CPL characteristics within its bandwidth. This translates into a transfer function $Z_L(s)$ that is not passive within the feedback bandwidth because its phase is equal to -180° at low frequencies. On the other hand, the status of passivity of the output impedance of the source subsystem, $Z_S(s)$, highly depends on the type of control implemented. The phase of the source impedance output impedance may exceed the range $-90^\circ \div +90^\circ$ within the feedback bandwidth depending on the type of control adopted. Therefore, since the bus impedance $Z_{bus}(s)$ is dominated by the source impedance $Z_s(s)$, i.e. $Z_{bus}(s)=Z_S(s)/(1+Z_S(s)/Z_L(s))\approx Z_S(s)$, except in a narrow range of frequencies around the resonant frequency of the source subsystem where the inequality $\|T_{MLG}(s)\|=\|Z_S(s)/Z_L(s)\|<<1$ does not hold, the passivity condition of $Z_{bus}(s)$ is violated even for a stable system if the source subsystem is not passive at low frequencies. The next section will show this with an example in simulation.

2.3. An Illustrative Example and Simulation

As an illustrative example, an averaged model simulation of a cascade of a buck converter with a Voltage Source Inverter (VSI) in Fig. 2.3 is considered to test the

validity and limitations of the PBSC. The values of voltages and components for both buck converter and VSI are also reported in Fig. 2.3.

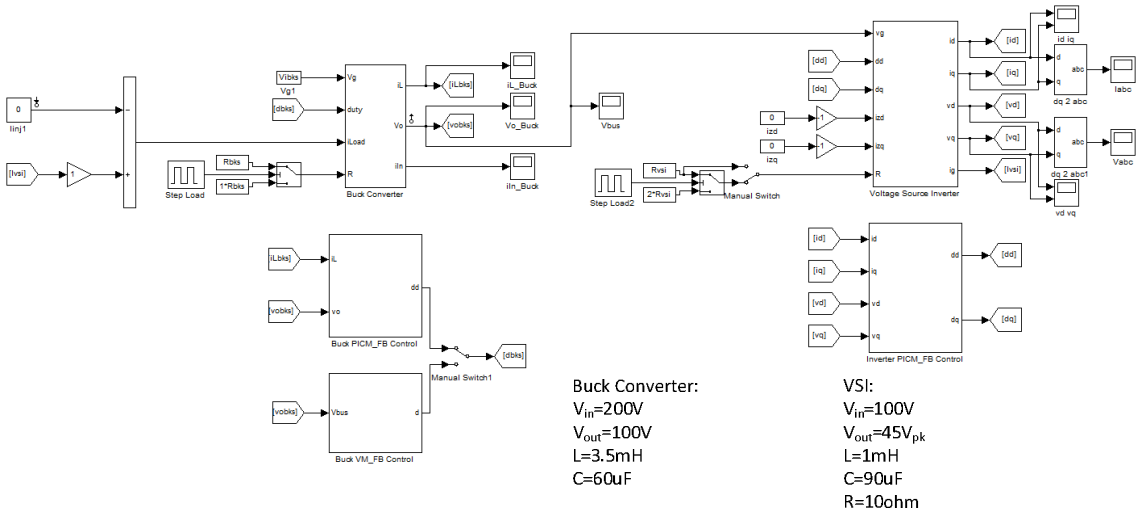


Figure 2.3. Averaged model simulation in Simulink of the cascade of a buck Converter and a VSI.

The VSI, modeled in synchronous *dq* coordinates [47, 48], is controlled by an inner PI current mode (PICM subscript) loop with crossover frequency $f_{c\_PICM}=1\ kHz$ and phase margin $PM\_{PICM}=80^{\circ}$, and an outer PI voltage (PICM_FB subscript) loop with crossover frequency $f_{c\_PICM\_FB}=0.1\ kHz$ and phase margin $PM\_{PICM\_FB}=80^{\circ}$. Due to its importance in the evaluation of the system bus impedance, Fig. 2.4 depicts how the input impedance of the VSI is modified by effect of the control action with respect to the open-loop (OL subscript) case. The addition of the PI current loop and then of the outer PI voltage loop has the effect of making such an impedance not passive at low frequencies since its phase clearly goes beyond the range $-90^{\circ} \div +90^{\circ}$. In other words, the PICM-controlled VSI and the PICM_FB-controlled VSI behave as a CPL within the control bandwidth.

Two different types of control are implemented on the buck converter to show their effect on the output impedance. Notice that the buck converter control was designed

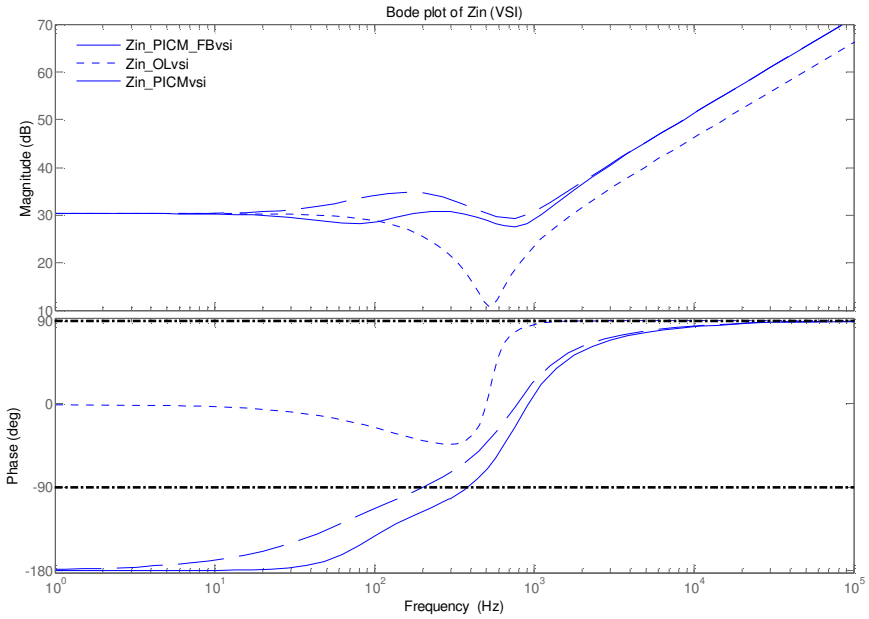


Figure 2.4. Bode plot of the OL, PICM, and PICM_FB input impedances of the VSI.

to take into account a load resistance that sinks the same amount of power that the VSI would do on its place. After the controller design is complete, the buck converter resistive load is removed and the VSI is connected. The first type of control that will be analyzed is a current mode, i.e. an inner PI current loop with crossover frequency $f_{c\_PICM}=1\ kHz$ and phase margin $PM\_{PICM}=80^{\circ}$, and an outer PI voltage loop with crossover frequency $f_{c\_PICM\_FB}=0.1\ kHz$ and phase margin $PM\_{PICM\_FB}=70^{\circ}$. The second type of control is a PID voltage mode (VM_FB subscript), i.e. a single voltage loop with crossover frequency $f_{c\_VM\_FB}=0.5\ kHz$ and phase margin $PM\_{VM\_FB}=52^{\circ}$.

The current mode control case is analyzed first. Figs. 2.5 and 2.6 depict how the output impedance of the buck converter with and without resistive load, respectively, is modified by effect of the control action with respect to the open-loop (OL subscript) case. The addition of the PI current loop and then of the outer PI voltage loop still keeps the

phase of the output impedance within the range $-90^{\circ} \div +90^{\circ}$. Therefore, both the PICM-controlled and the PICM_FB-controlled buck converter output impedances are passive transfer functions.

The case of VM_FB-controlled buck converter produces a different result. Figs. 2.7 and 2.8 depict how the output impedance of the buck converter with and without resistive load, respectively, is modified by effect of the control action with respect to the open-loop (OL subscript) case. The addition of the PID voltage loop has the effect of making such an impedance not passive at low frequencies since its phase clearly goes beyond the range $-90^{\circ} \div +90^{\circ}$.

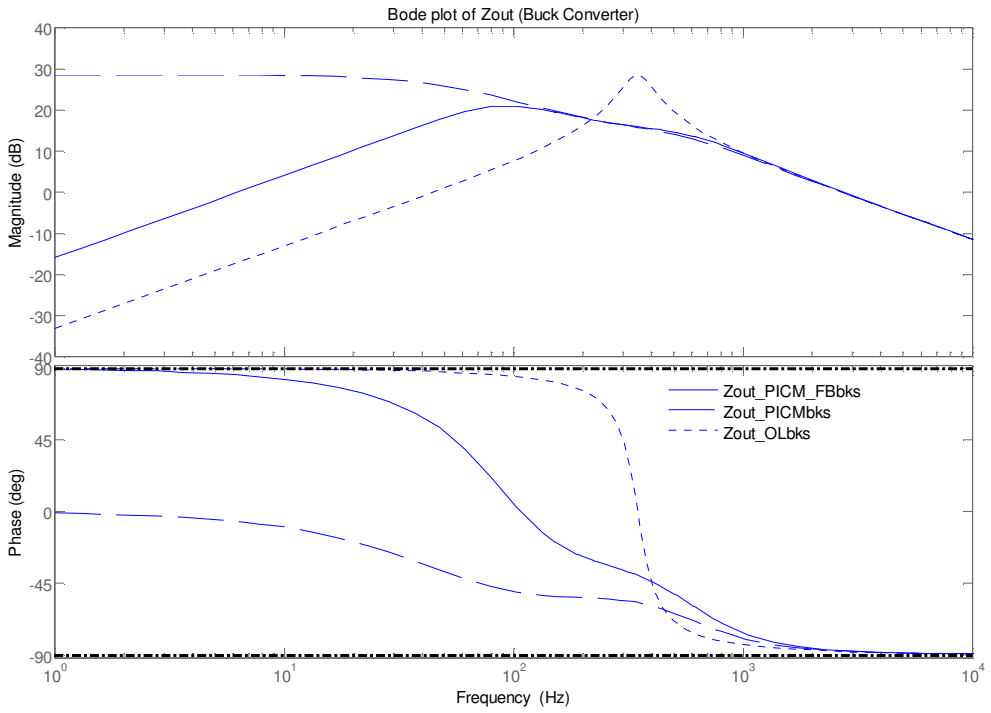


Figure 2.5. Bode plot of the OL, PICM, and PICM_FB output impedance of the buck converter with resistive load.

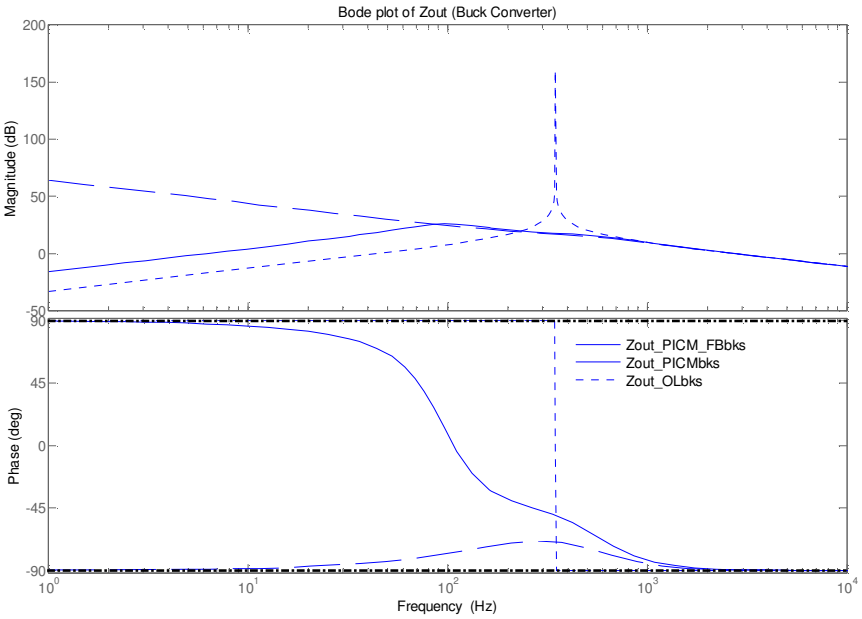


Figure 2.6. Bode plot of the OL, PICM, and PICM_FB output impedance of the buck converter with resistive load removed.

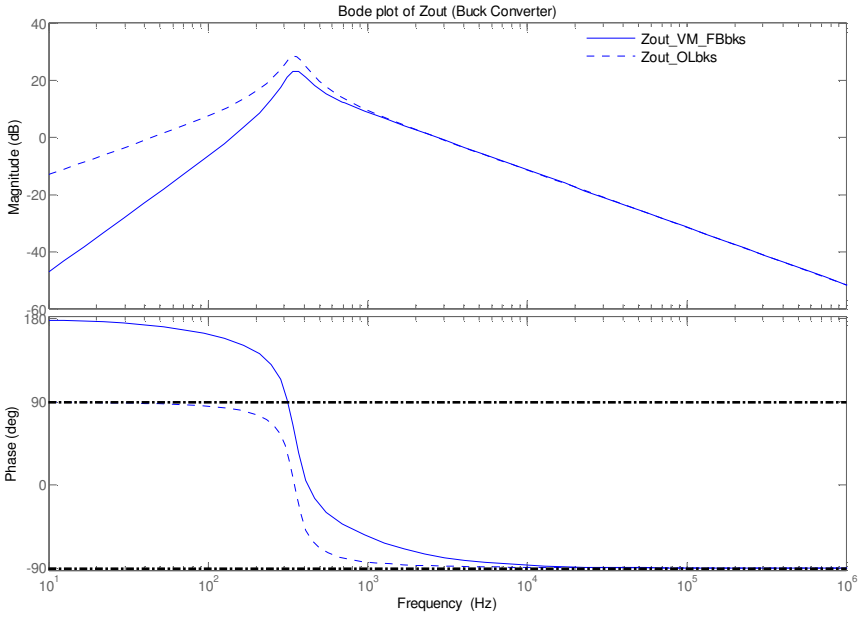


Figure 2.7. Bode plot of the OL and VM_FB output impedance of the buck converter with resistive load.

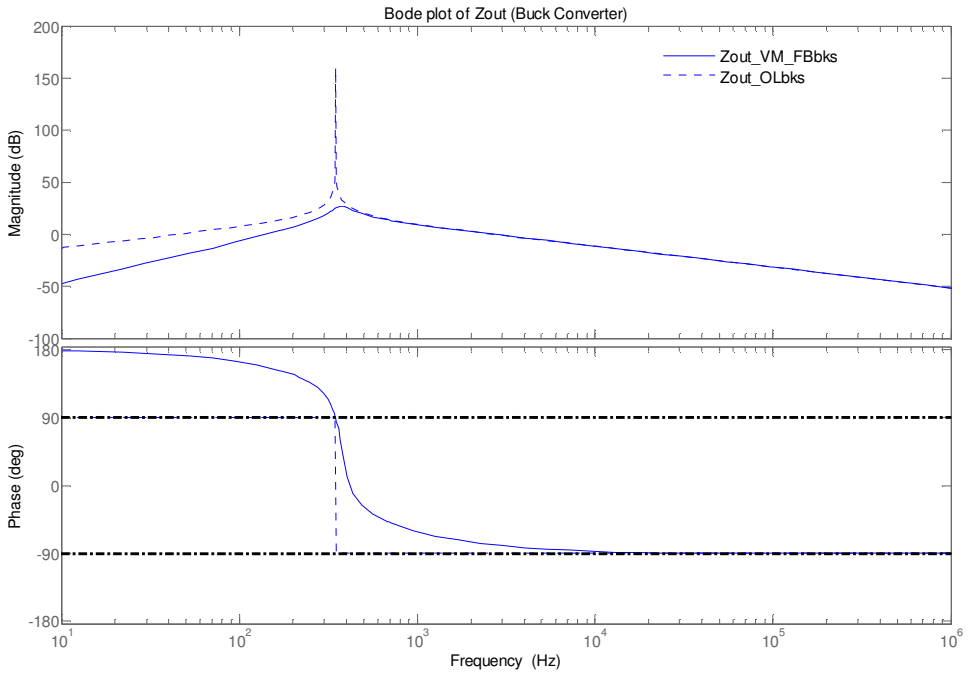


Figure 2.8. Bode plot of the OL and VM_FB output impedance of the buck converter with resistive load removed.

In the next two subsections, the bus impedance is built as the parallel combination of the buck converter output impedance and the VSI input impedance. The stability of the system is assessed by using the PBSC applied to the bus impedance and the Nyquist Criterion applied to the minor loop gain in frequency-domain simulations as well as time-domain simulations to verify the limitations of the PBSC. Two cases are analyzed: a stable one and an unstable one, depending on the types of the controllers implemented for the buck converter and the VSI. Table 2.1 summarizes the results that are presented in the next two subsections.

Table 2.1 Summary of results for stable and unstable cases.

CASE	TYPE OF CONTROL	Z_{bus} PASSIVE?	STABLE?	FIGURES
STABLE	PICM_FB Buck PICM_FB VSI	Yes	Yes	2.9-2.13
	VM_FB Buck PICM VSI	No	Yes	2.14-2.18
UNSTABLE	PICM_FB Buck PICM_FB VSI	No	No	2.19-2.23
	VM_FB Buck PICM VSI	No	No	2.24-2.28

2.3.1. STABLE CASES

The frequency-domain simulation results for the cascade of a PICM_FB-controlled buck converter and a PICM_FB-controlled VSI are shown in Figs. 2.9-2.11. The Bode plot of Fig. 2.9 reveals that the bus impedance $Z_{bus}(s)$ follows the source subsystem output impedance $Z_{out\_PICM\_FB}(s)$ everywhere except around the range where it exhibits resonance (in the parallel combination the smaller impedance dominates). The bus impedance resonant peak is near the resonance of the source subsystem (at ~*100Hz*) and its phase stays within the range $-90^{\circ} \div +90^{\circ}$ at all frequencies. This means that the bus impedance has a Nyquist plot that wholly lies on the RHP as depicted in Fig. 2.10, implying that the PBSC is satisfied resulting in a stable system. This is also confirmed by using the Nyquist Criterion on the minor loop gain $T_{MLG}(s)=Z_{out\_PICM\_FB}(s)/Z_{in\_PICM\_FB}(s)$ since the contour does not encircle the *(-1, 0)* point, as shown in Fig. 2.11. The time-

domain simulations are reported in Figs. 2.12-2.13 which show the transient of the bus voltage and VSI three-phase output voltage in correspondence of a VSI symmetric three-phase load step from 20Ω to 10Ω and VSI voltage step from $22.5V_{pk}$ to $45V_{pk}$, respectively. A stable performance is evident.

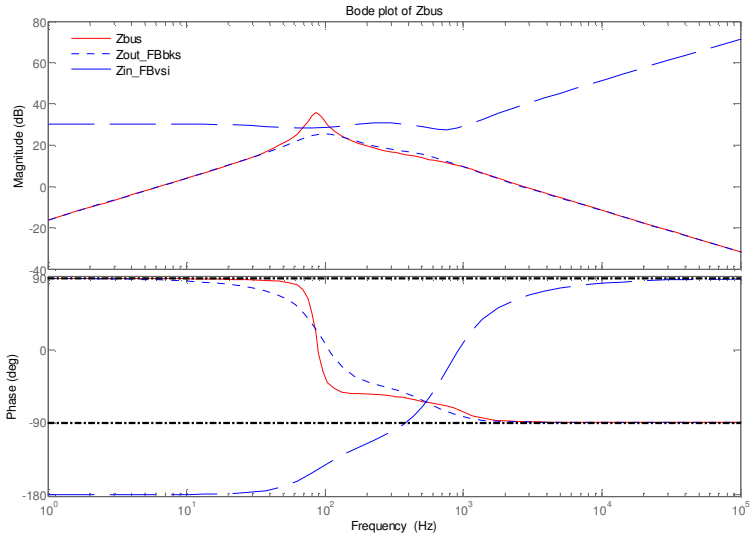


Figure 2.9. Bode plot of the bus impedance for the cascade of PICM_FB-controlled buck converter and PICM_FB-controlled VSI (stable case).

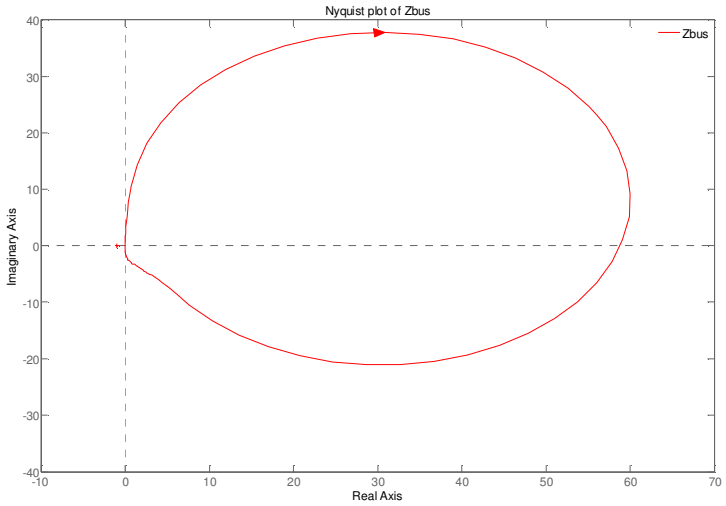


Figure 2.10. Nyquist plot of the bus impedance for the cascade of PICM_FB-controlled buck converter and PICM_FB-controlled VSI (stable case).

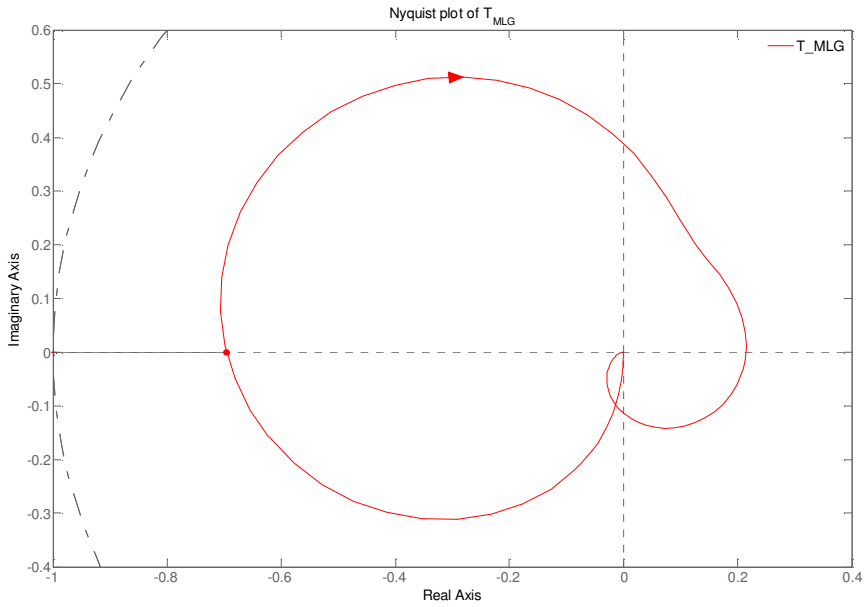


Figure 2.11. Nyquist plot of the minor loop gain for the cascade of PICM_FB-controlled buck converter and PICM_FB-controlled VSI (stable case).

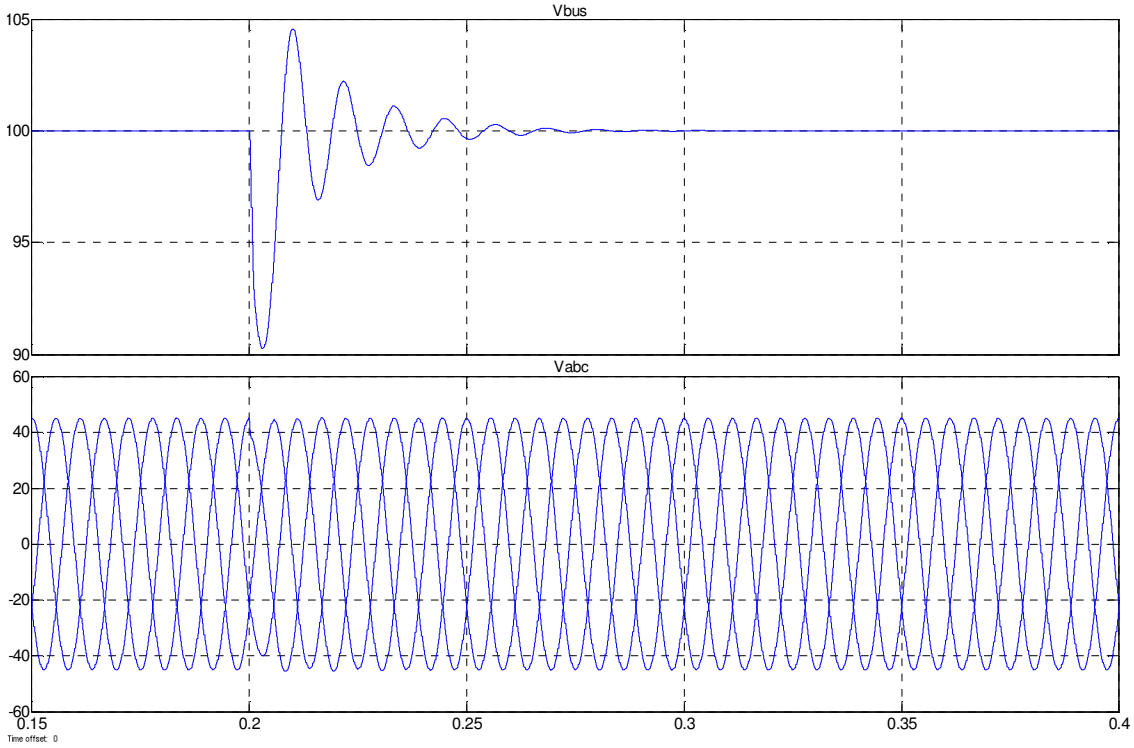


Figure 2.12. Bus voltage and VSI trhee-phase output voltage transient in corrispondence of a symmetric VSI load step from *20*Ω to *10*Ω for the cascade of PICM_FB-controlled buck converter and PICM_FB-controlled VSI (stable case).

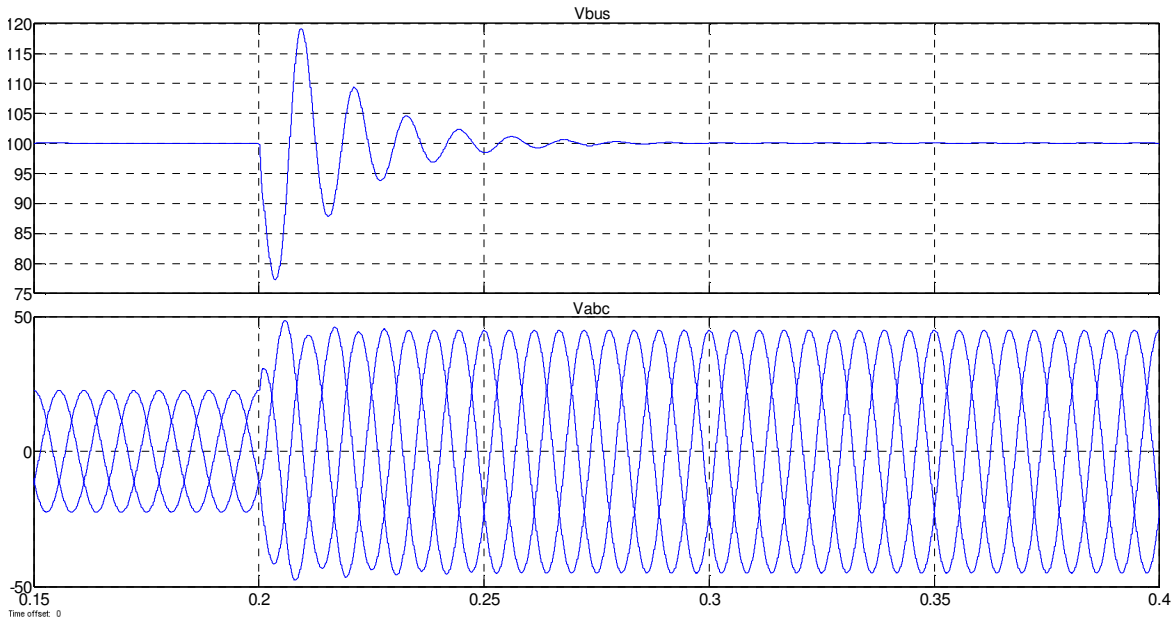


Figure 2.13. Bus voltage and VSI trhee-phase output voltage transient in corrispondence of a VSI voltage step from $22.5V_{pk}$ to $45V_{pk}$ for the cascade of PICM_FB-controlled buck converter and PICM_FB-controlled VSI (stable case).

The frequency-domain simulation results for the cascade of a VM_FB-controlled buck converter and a PICM_FB-controlled VSI are shown in Figs. 2.14-2.16. The Bode plot of Fig. 2.14 reveals that the bus impedance $Z_{bus}(s)$ follows the source subsystem output impedance $Z_{out\_VM\_FB}(s)$ everywhere except around the range where it exhibits resonance (again, in the parallel combination the smaller impedance dominates). The bus impedance resonant peak is near the resonance of the source subsystem (at ~$500Hz$), but its phase, this time, does not stay within the range $-90^{\circ} \div +90^{\circ}$ at all frequencies. In particular, the phase of the bus impedance is equal to 180° at low frequencies. This means that the bus impedance has a Nyquist plot that does not wholly lie on the RHP as depicted in Fig. 2.15, implying that the PBSC is not satisfied resulting in a not-passive system. From this result, by using the PBSC in its raw form, one cannot reach a conclusion on system stability, because passivity is a sufficient, but not necessary condition for stability.

In this case, the system is stable, as confirmed by using the Nyquist Criterion (which provides a necessary and sufficient condition for the system stability) on the minor loop gain $T_{MLG}(s)=Z_{out\_VM\_FB}(s)/Z_{in\_PICM\_FB}(s)$ since the contour stays does not encircle the *(-1, 0)* point, as shown in Fig. 2.16. The time-domain simulations are reported in Figs. 2.17-2.18 which show the transient of the bus voltage and VSI three-phase output voltage in correspondence of a VSI symmetric three-phase load step from *20*Ω to *10*Ω and VSI voltage step from $22.5V_{pk}$ to $45V_{pk}$, respectively. A stable performance is evident.

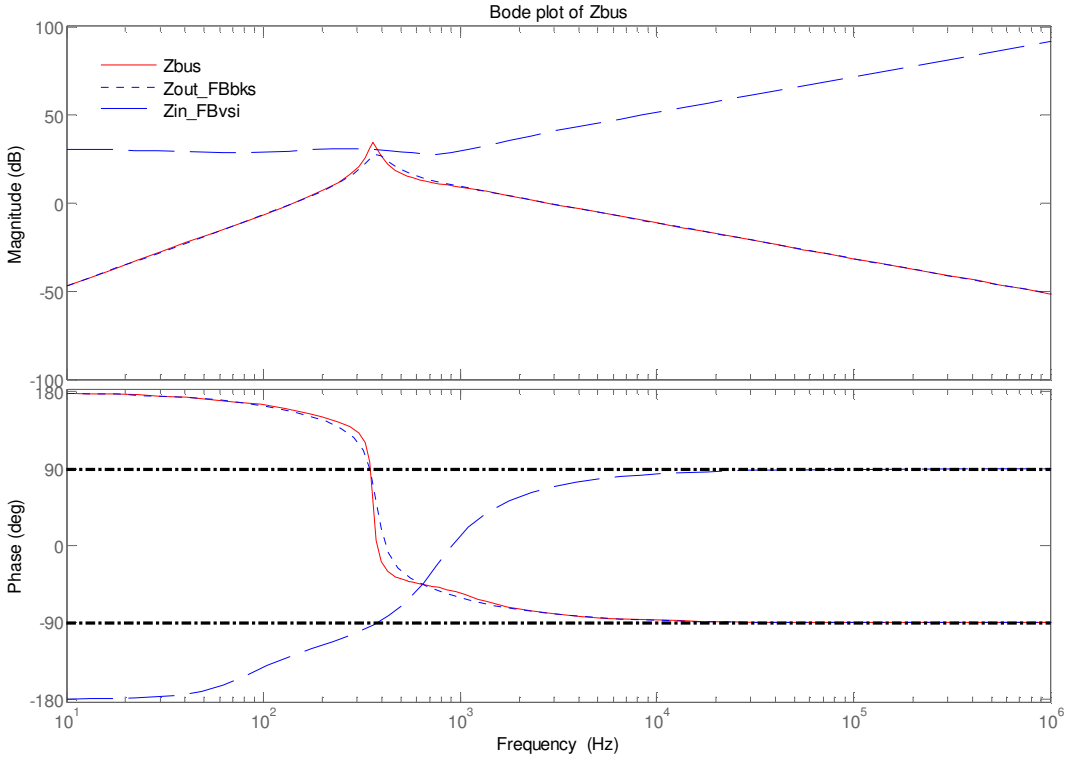


Figure 2.14. Bode plot of the bus impedance for the cascade of VM_FB-controlled buck converter and PICM_FB-controlled VSI (stable case).

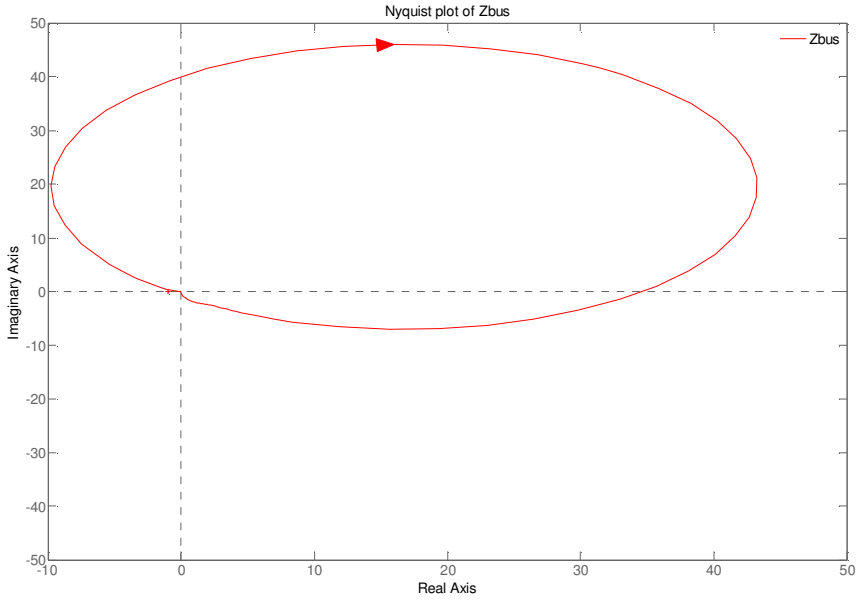


Figure 2.15. Nyquist plot of the bus impedance for the cascade of VM_FB-controlled buck converter and PICM_FB-controlled VSI (stable case).

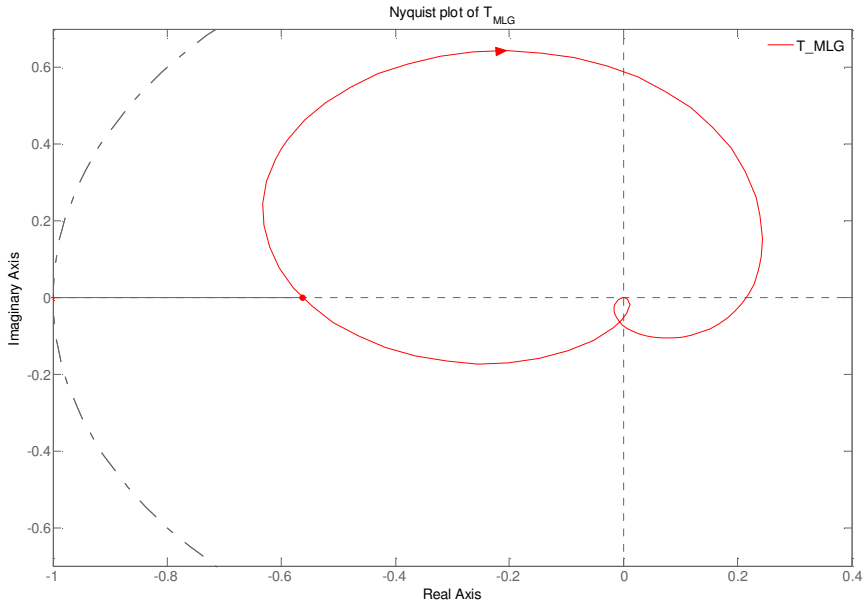


Figure 2.16. Nyquist plot of the minor loop gain for the cascade of VM_FB-controlled buck converter and PICM_FB-controlled VSI (stable case).

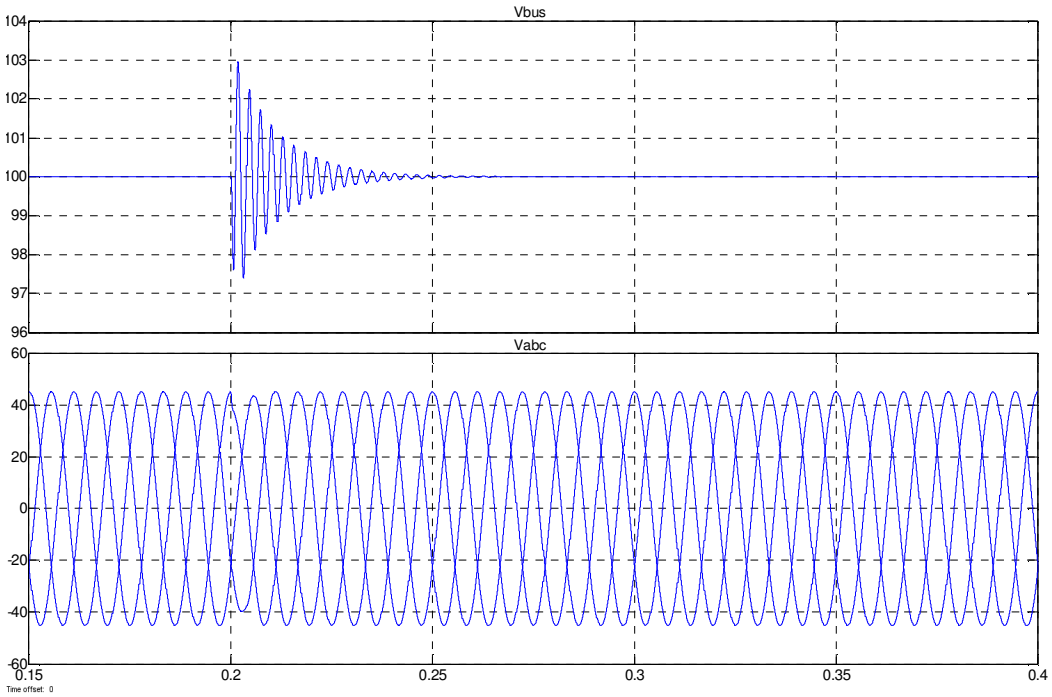


Figure 2.17. Bus voltage and VSI trhee-phase output voltage transient in corrispondence of a symmetric VSI load step from *20*Ω to *10*Ω for the cascade of VM_FB-controlled buck converter and PICM_FB-controlled VSI (stable case).

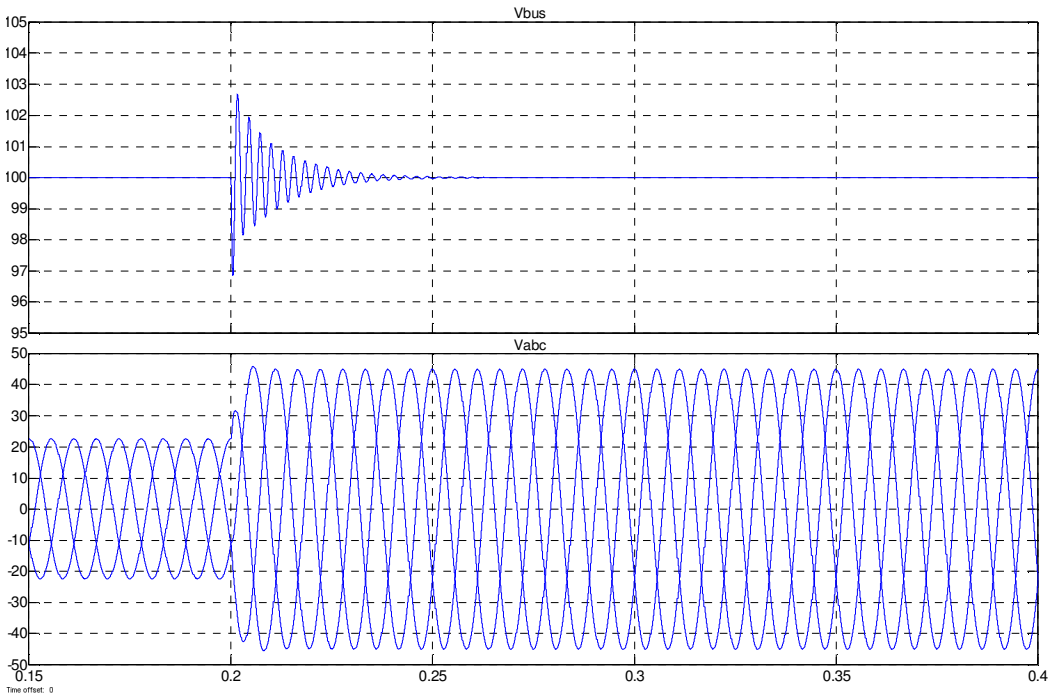


Figure 2.18. Bus voltage and VSI trhee-phase output voltage transient in corrispondence of a VSI voltage step from $22.5V_{pk}$ to $45V_{pk}$ for the cascade of VM_FB-controlled buck converter and PICM_FB-controlled VSI (stable case).

2.3.2. UNSTABLE CASES

To make the system consisting of the cascade of a PICM_FB-controlled buck converter and a PICM_FB-controlled VSI unstable, the buck converter outer voltage loop phase margin is reduced to $PM\_{PICM\_FB}=50^{\circ}$. The frequency-domain simulation results for the cascade of a PICM_FB-controlled buck converter and a PICM_FB-controlled VSI are shown in Figs. 2.19-2.21. The Bode plot of Fig. 2.19 reveals that the bus impedance $Z_{bus}(s)$ follows the source subsystem output impedance $Z_{out\_PICM\_FB}(s)$ everywhere except around the range where it exhibits resonance. The bus impedance resonant peak is near the resonance of the source subsystem (at ~*100Hz*) and its phase stays within the range $-90^{\circ} \div +90^{\circ}$ at all frequencies except in a frequency range around the resonant frequency. This means that the bus impedance has a Nyquist plot that goes to the LHP as depicted in Fig. 2.20, intersecting the negative axis at about *-200*. For this case, nothing can be stated about the stability of the system by using the PBSC in its raw form. However, the resulting system is unstable, as confirmed by using the Nyquist Criterion on the minor loop gain $T_{MLG}(s)=Z_{out\_PICM\_FB}(s)/Z_{in\_PICM\_FB}(s)$ since the contour encircles the *(-1, 0)* point, as shown in Fig. 2.21. The time-domain simulations are reported in Figs. 2.22-2.23 which show the transient of the bus voltage and VSI three-phase output voltage in correspondence of a VSI symmetric three-phase load step from *20*Ω to *10*Ω and VSI voltage step from $22.5V_{pk}$ to $45V_{pk}$, respectively. An unstable performance is evident.

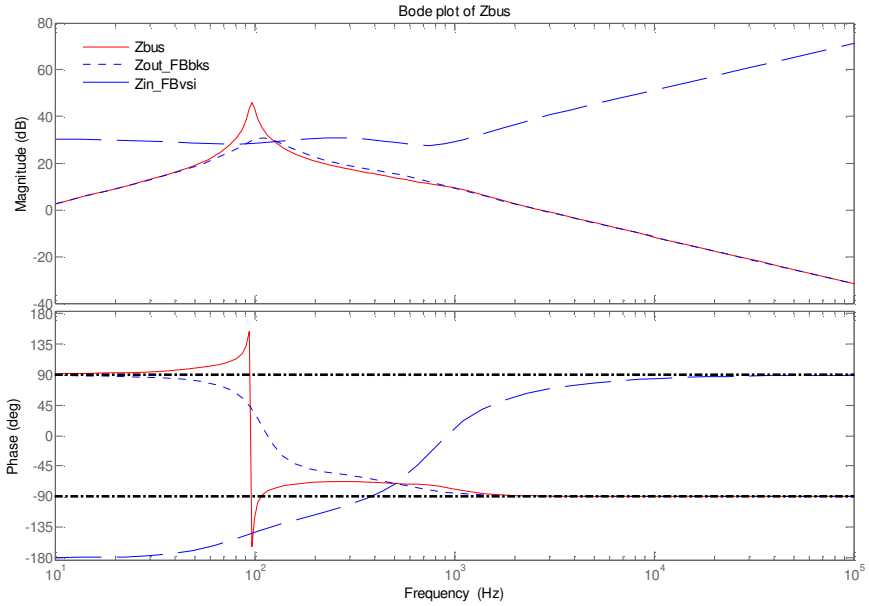


Figure 2.19. Bode plot of the bus impedance for the cascade of PICM_FB-controlled buck converter and PICM_FB-controlled VSI (unstable case).

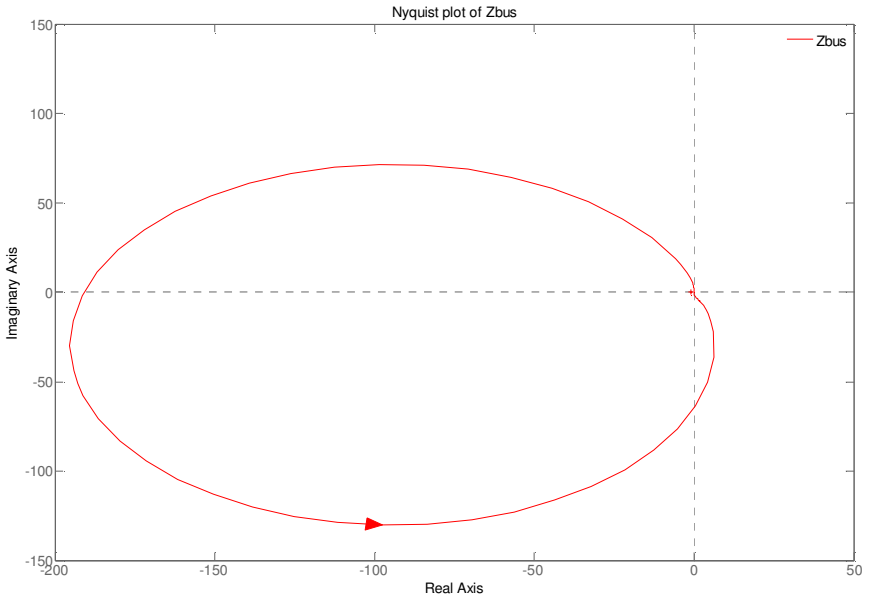


Figure 2.20. Nyquist plot of the bus impedance for the cascade of PICM_FB-controlled buck converter and PICM_FB-controlled VSI (unstable case).

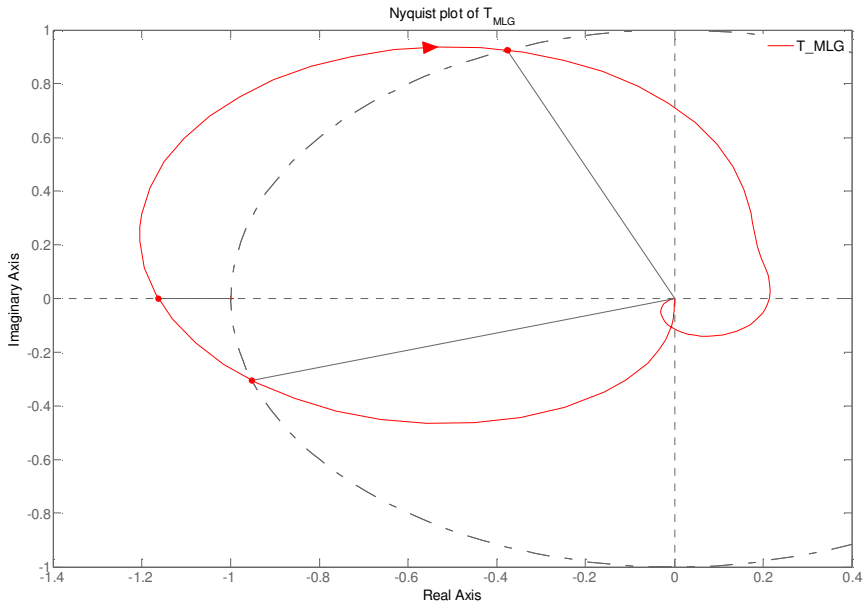


Figure 2.21. Nyquist plot of the minor loop gain for the cascade of PICM_FB-controlled buck converter and PICM_FB-controlled VSI (unstable case).

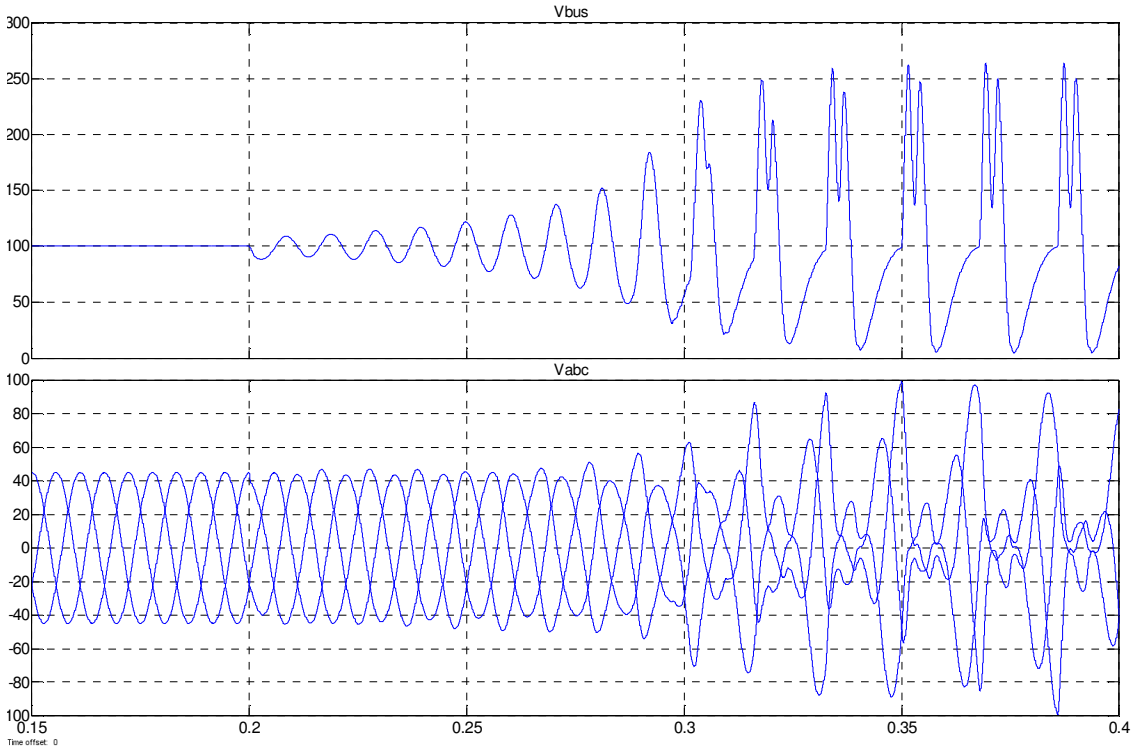


Figure 2.22. Bus voltage and VSI trhee-phase output voltage transient in corrispondence of a symmetric VSI load step from *20*Ω to *10*Ω for the cascade of PICM_FB-controlled buck converter and PICM_FB-controlled VSI (unstable case).

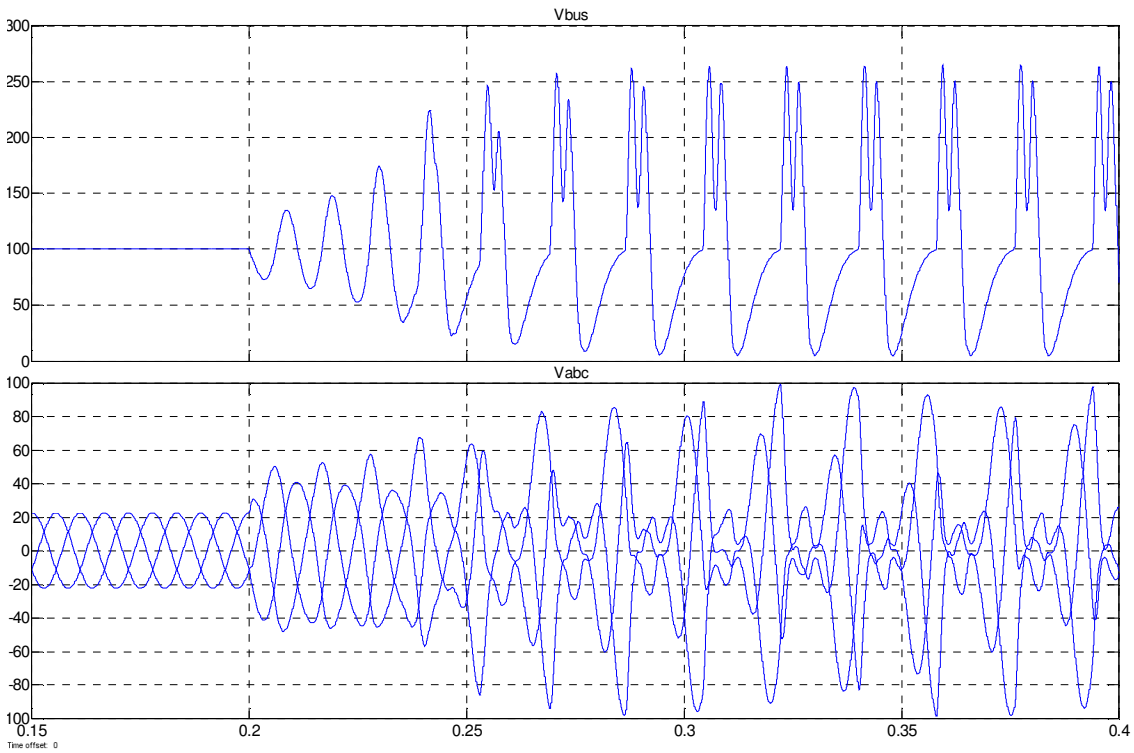


Figure 2.23. Bus voltage and VSI trhee-phase output voltage transient in corrispondence of a VSI voltage step from $22.5V_{pk}$ to $45V_{pk}$ for the cascade of PICM_FB-controlled buck converter and PICM_FB-controlled VSI (unstable case).

To make the system consisting of the cascade of a VM_FB-controlled buck converter and a PICM_FB-controlled VSI unstable, the buck converter outer voltage loop cross-over frequency is reduced to $f_{c\_VM\_FB}=0.2KHz$. The frequency-domain simulation results for the cascade of a VM_FB-controlled buck converter and a PICM_FB-controlled VSI are shown in Figs. 2.24-2.26. The Bode plot of Fig. 2.24 reveals that the bus impedance $Z_{bus}(s)$ follows the source subsystem output impedance $Z_{out\_VM\_FB}(s)$ everywhere except around the range where it exhibits resonance. The bus impedance resonant peak is near the resonance of the source subsystem (at ~$500Hz$), and its phase does not stay within the range $-90^{\circ} \div +90^{\circ}$ at all frequencies. In particular, the phase of the bus impedance is equal to 180° at low frequencies and, more important, in the frequency range around the resonant frequency. This means that the bus impedance has a

Nyquist plot that goes to the LHP as depicted in Fig. 2.25, intersecting the negative axis at about *-150*. Even in this case, nothing can be stated about the stability of the system by using the PBSC in its raw form. However, the resulting system is unstable, as confirmed by the Nyquist Criterion on the minor loop gain $T_{MLG}(s)=Z_{out\_VM\_FB}(s)/Z_{in\_PICM\_FB}(s)$ since the contour encircles the *(-1, 0)* point, as shown in Fig. 2.26. The time-domain simulations are reported in Figs. 2.27-2.28 which show the transient of the bus voltage and VSI three-phase output voltage in correspondence of a VSI symmetric three-phase load step from *20*Ω to *10*Ω and VSI voltage step from $22.5V_{pk}$ to $45V_{pk}$, respectively. An unstable performance is evident.

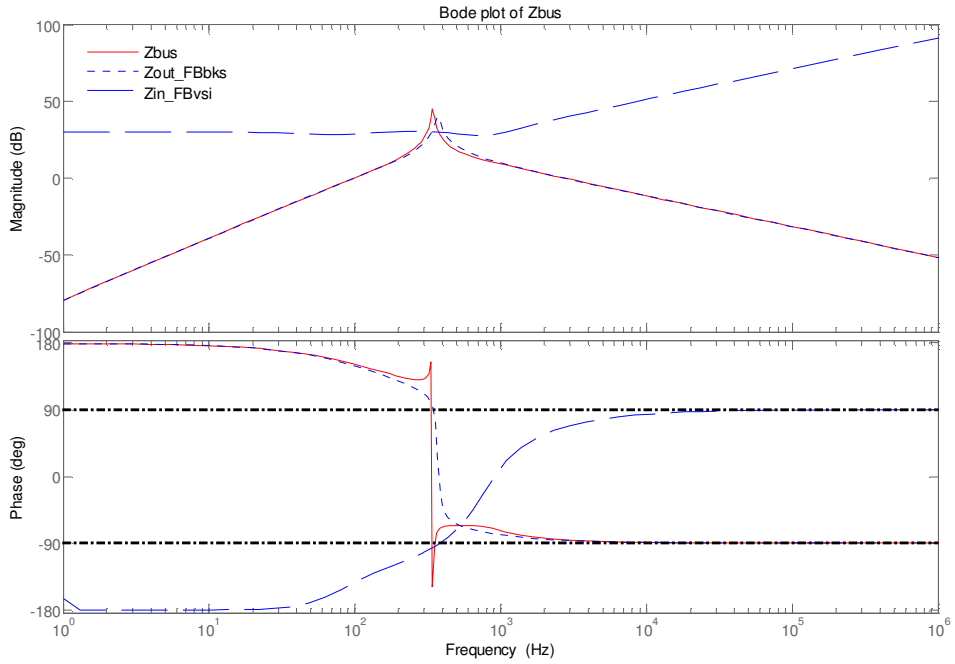


Figure 2.24. Bode plot of the bus impedance for the cascade of VM_FB-controlled buck converter and PICM_FB-controlled VSI (unstable case).

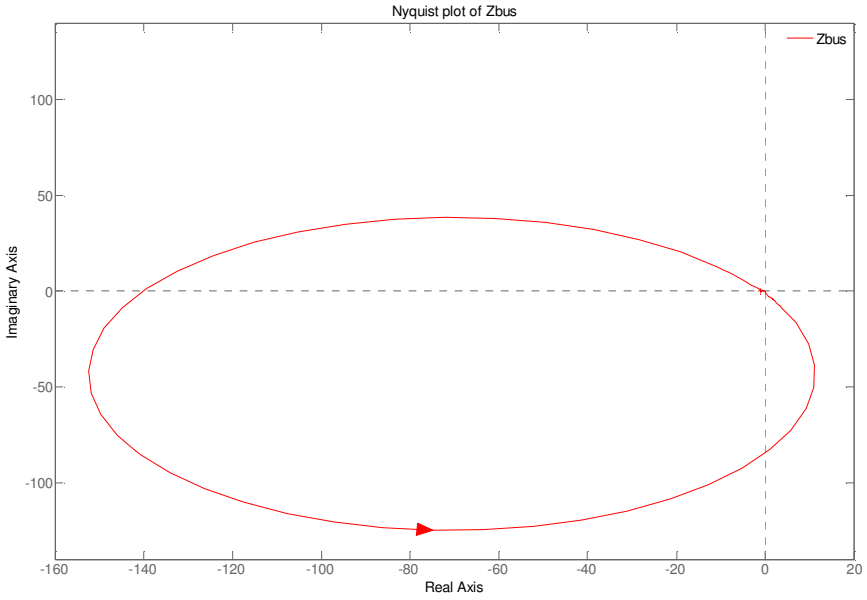


Figure 2.25. Nyquist plot of the bus impedance for the cascade of VM_FB-controlled buck converter and PICM_FB-controlled VSI (unstable case).

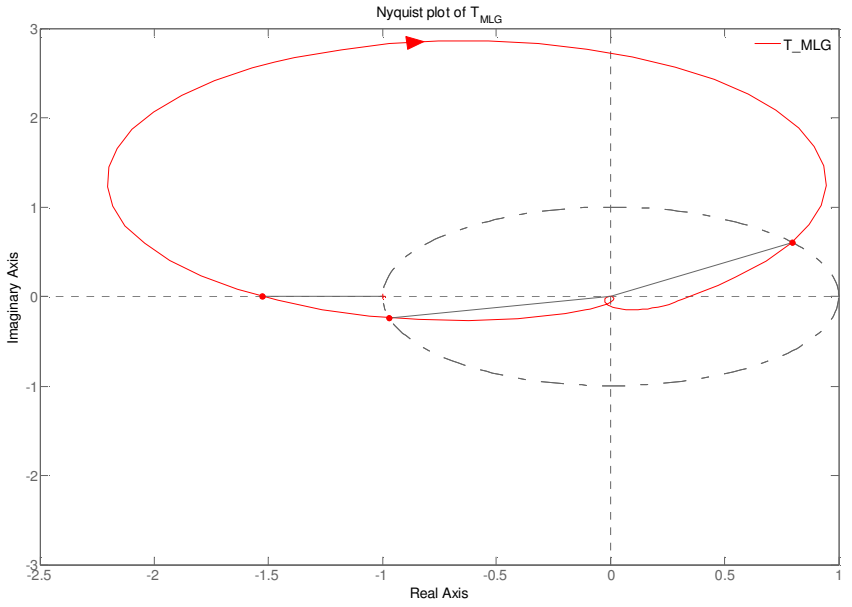


Figure 2.26. Nyquist plot of the minor loop gain for the cascade of VM_FB-controlled buck converter and PICM_FB-controlled VSI (unstable case).

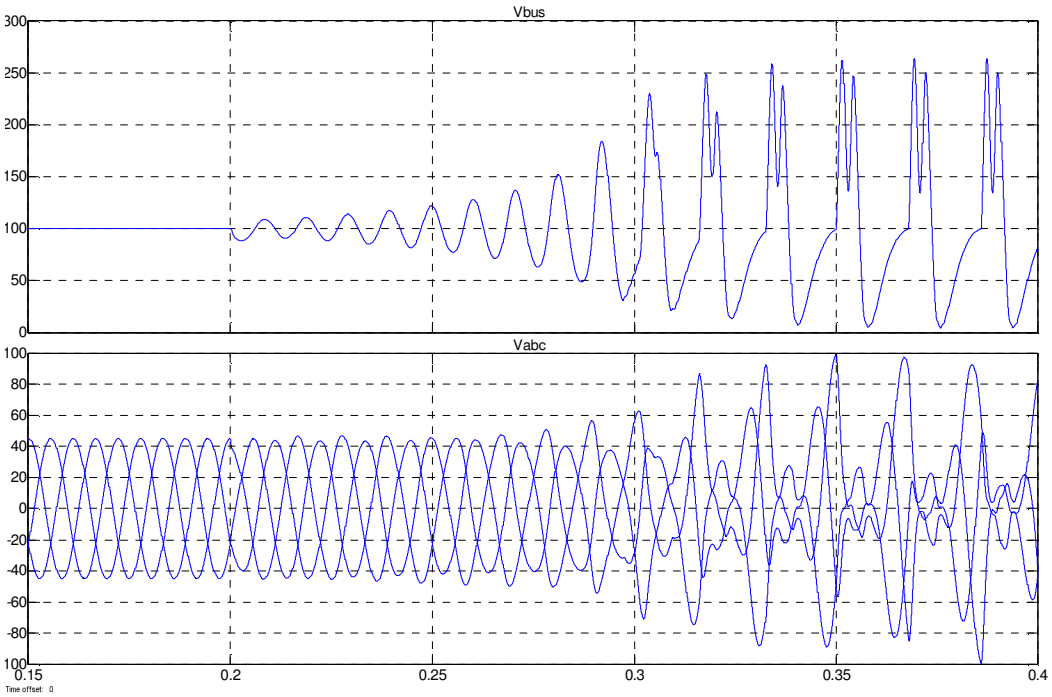


Figure 2.27. Bus voltage and VSI trhee-phase output voltage transient in corrispondence of a symmetric VSI load step from *20*Ω to *10*Ω for the cascade of VM_FB-controlled buck converter and PICM_FB-controlled VSI (unstable case).

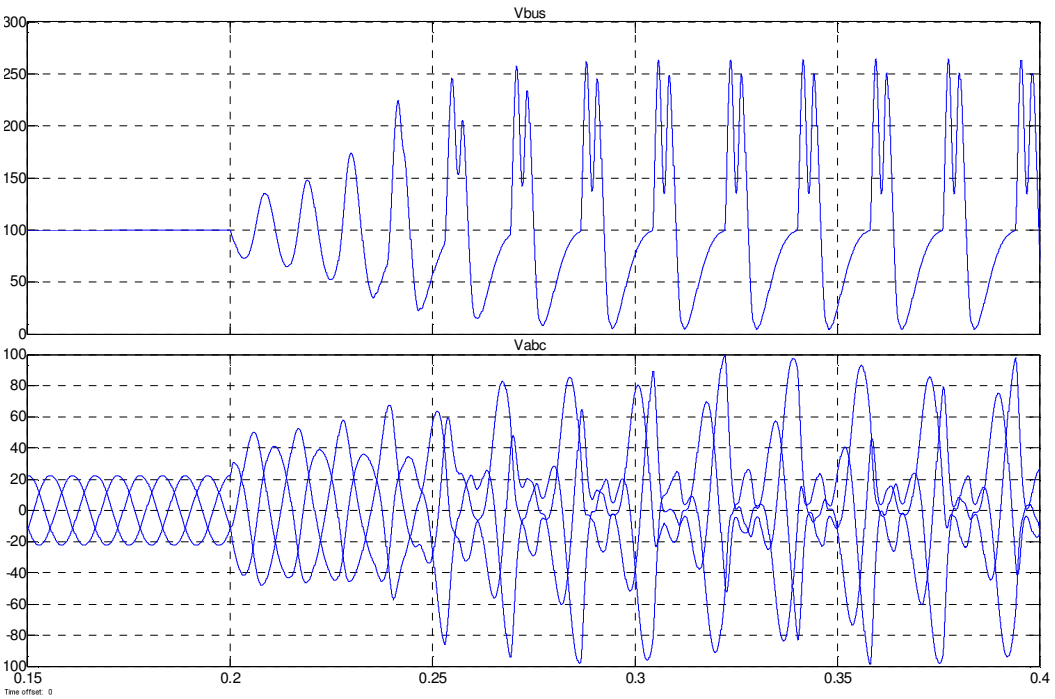


Figure 2.28. Bus voltage and VSI trhee-phase output voltage transient in corrispondence of a VSI voltage step from $22.5V_{pk}$ to $45V_{pk}$ for the cascade of VM_FB-controlled buck converter and PICM_FB-controlled VSI (unstable case).

2.4. THE RELATIONSHIP BETWEEN PBSC AND NYQUIST CRITERION

The PBSC in its raw form gives only a sufficient condition for system stability. This is confirmed by the simulation results summarized in Table 2.1. If the bus impedance is passive, the system is stable. However, if the bus impedance is not passive, the system may be stable or unstable, and both cases occur in the results reported in Table 2.1.

Since the PBSC in its raw form gives only a sufficient condition for system stability, while the Nyquist Criterion provides a necessary and sufficient condition, an analysis that makes the relationship between PBSC and Nyquist Criterion is needed. The following analysis is based more on practical observations of results rather than on a formal definition, which is left as a future work. The goal is to show that the low-frequency passivity information of the system bus impedance does not really contribute in the assessment of the system stability. Instead, the passivity information of the system bus impedance around the resonant frequency plays a key role in the system stability assessment.

The interacting system of Fig. 2.2 is taken into consideration for which the minor loop gain is defined as $T_{MLG}(j\omega)=Z_S(j\omega)/Z_L(j\omega)$. According to the Nyquist Criterion, the system of Fig. 2.2 is stable if and only if the Nyquist contour of $T_{MLG}(j\omega)$ does not encircle the $(-1, 0)$ point. Encirclement of the critical point is avoided if either one of the two conditions is met:

1) $|T_{MLG}(j\omega)|<1 \ \forall \omega$ (infinite phase margin condition), or

2) $|arg[T_{MLG}(j\omega)]|<180^{\circ} \ \forall \omega$ (infinite gain margin condition).

Considering the illustrative example shown in the previous section, condition 1) was met for the case of a passive bus impedance at all frequencies (PBSC satisfied) shown in Fig. 2.11 and for the case of a not-passive bus impedance at low frequencies (PBSC not satisfied) shown in Fig. 2.16, resulting in a stable system.

In DC power distribution systems, in normal operation, condition 1) may not be met at the source subsystem resonant frequency, where its output impedance exhibits a resonant peak and may exceed the amplitude of the load subsystem input impedance. Instead, at low frequencies and at high frequencies condition 1) is met. Condition 1) is met at low frequencies because the source subsystem has the control of the bus voltage within its control bandwidth. Condition 1) is met at high frequencies because the source subsystem output impedance exhibits capacitive impedance. As a result, the bus impedance is dominated by the source subsystem output impedance at low and high frequencies, while neither $Z_S(j\omega)$ nor $Z_L(j\omega)$ dominate at frequencies around the resonant frequency. Therefore, even though the PBSC (and condition 2)) was not respected at low frequency for the cascade of a VM_FB-controlled buck converter with a PICM_FB-controlled VSI (Figs. 2.14 to 2.18), the corresponding minor loop gain magnitude is less than one at those frequencies.

As a result of this discussion, *the following hypothesis is made*. Assuming that the source subsystem and load subsystem were designed to be standalone stable, and assuming that the source and load impedance are comparable in magnitude only in a certain frequency range called interaction frequency range (around one or more resonant frequencies), in order to establish stability it is sufficient to verify overall bus impedance passivity only in the interaction frequency range.

Let us now examine the results of the simulation study presented earlier in light of this hypothesis. Looking at Table 2.1, four cases were analyzed. In the first case (Case 1) the PBSC is met and consequently the system is stable. We will now focus on the other three cases (Cases 2-4), where the PBSC is not met. In all four cases source impedance $Z_S(j\omega)$ dominates both at low and high frequencies, as shown in Figs. 2.9, 2.14, 2.19 and 2.24. Considering stable Case 2, we can see from Fig. 2.15 that passivity is violated only at low frequencies, but it is met around the resonant frequency. For the unstable Cases 3-4 passivity condition is violated around the resonant frequency, as can be seen in Figs. 2.20 and 2.25.

2.5. THE PRACTICAL PBSC

Directly following from the analysis and the hypothesis made in the previous section, under the practical standpoint, it is not necessary that the PBSC be satisfied at all frequencies. A practical concept of passivity is the passivity condition within a finite frequency interval [63]. The term "practical passivity" is here adopted in order to highlight the convenience of this concept in practice. Again referring to the 1-port network depicted in Fig. 2.1 (c), the resulting network is practical passive if and only if:

1) $Z_{bus}(s)$ has no RHP poles, and

2) $Re\{Z_{bus}(j\omega)\} \geq 0, \ \forall \Omega := \{\omega \in \Re : \omega_{\min} \leq \omega \leq \omega_{\max}\}$.

The bandwidth Ω can be identified as the frequency range in which the phase of the minor loop gain is equal to 180° or greater which corresponds to an undamped system with null or negative damping factor $\varsigma \leq 0$ or in the range $180^{\circ} \div 90^{\circ}$ which corresponds to an under-damped system with less than unity damping factor $0 \leq \varsigma \leq 1$. An over-damped system corresponds to a system with $\varsigma > 1$. However, this is not a practical approach since

most of the times the minor loop gain measurements in real system is not easy to have. The definition of Ω has to be made in a different way by using the easily obtainable bus impedance measurement. The first problem in a real system is to identify the resonant frequency. After measurement and model fitting [64], the expression of the bus impedance can be very complex. In general, the expression of the bus impedance is

$$Z_{bus}(s) = K \frac{(s+a_0)(s+a_1)...(s+a_n)\cdot\left(\frac{s^2}{\omega_{res\_N_0}{}^2}+2\zeta_{N_0}\frac{s}{\omega_{res\_N_0}}+1\right)\left(\frac{s^2}{\omega_{res\_N_1}{}^2}+2\zeta_{N_1}\frac{s}{\omega_{res\_N_1}}+1\right)...\left(\frac{s^2}{\omega_{res\_N_m}{}^2}+2\zeta_{N_m}\frac{s}{\omega_{res\_N_m}}+1\right)}{(s+b_0)(s+b_1)...(s+b_p)\cdot\left(\frac{s^2}{\omega_{res\_D_0}{}^2}+2\zeta_{D_0}\frac{s}{\omega_{res\_D_0}}+1\right)\left(\frac{s^2}{\omega_{res\_D_1}{}^2}+2\zeta_{D_1}\frac{s}{\omega_{res\_D_1}}+1\right)...\left(\frac{s^2}{\omega_{res\_D_q}{}^2}+2\zeta_{D_q}\frac{s}{\omega_{res\_D_q}}+1\right)} \tag{2.16}$$

where the damping factor vector and the corresponding resonant frequency vector are given by

$$\varsigma = \left[\zeta_{N_0}, \zeta_{N_1}, ..., \zeta_{N_m}, \zeta_{D_0}, \zeta_{D_1}, ..., \zeta_{D_q}\right] \tag{2.17}$$

$$\omega_{res} = \left[\omega_{res\_N_0}, \omega_{res\_N_1}, ..., \omega_{res\_N_m}, \omega_{res\_D_0}, \omega_{res\_D_1}, ..., \omega_{res\_D_q}\right] \tag{2.18}$$

MATLAB software implements a function "damp" which returns the natural frequency and corresponding damping frequency vectors of a linear system similar to that in (2.16). At this point, identified the resonant frequency (or frequencies) with low or negative damping factor (or factors), the bandwidth Ω can be calculated [65] as follows

$$\omega_{\min} = \left(e^{\pi/2}\right)^{-\zeta}\omega_{res} \qquad \textit{and} \qquad \omega_{\max} = \left(e^{\pi/2}\right)^{\zeta}\omega_{res} \tag{2.19}$$

Since the stability problem is only in the narrow range of frequencies around the resonant frequency, as shown in the previous section, the PBSC has to be defined within Ω. The practical PBSC is then defined as follows.

If the Nyquist contour of the system bus impedance $Z_{bus}(s)$ intersects the positive real axis in Ω, then the overall system consisting of the parallel combination of all the converters' input/output impedances (or equivalently of the two interacting subsystems)

is stable. Conversely, if such an intersection occurs in the negative real axis, then the system is unstable.

To further validate the practical PBSC the example of the cascade of a VM_FB-controlled buck converter and a PICM_FB-controlled VSI is taken again into consideration. In the stable case, the bus impedance has the following expression

$$Z_{bus}(s) = \frac{16666.6667\,s^2\,(s+1.257e06)\,(s+1.257e05)\,(s^2+791.1s+2.903e05)}{(s+1.257e06)\,(s+1.221e05)\,(s+2470)\,(s^2+789.9s+2.872e05)\,(s^2+178s+5.146e06)} \cdot \frac{(s^2+4766s+2.431e07)\,(s^2+4766s+2.431e07)}{(s^2+4766s+2.431e07)\,(s^2+5349s+2.976e07)} \tag{2.20}$$

The vector of the system damping factors and the system natural frequencies are reported in (2.21).

$$\varsigma = \begin{bmatrix} 0.736988588359644 \\ 0.736988588359644 \\ 0.039227205867031 \\ 0.039227205867031 \\ 1.000000000000000 \\ 0.483387259354916 \\ 0.483387259354916 \\ 0.490192885127426 \\ 0.490192885127426 \\ 1.000000000000000 \\ 1.000000000000000 \end{bmatrix} \quad and \quad f_{res} = \begin{bmatrix} 0.000852884429228 \\ 0.000852884429228 \\ 0.003610284227573 \\ 0.003610284227573 \\ 0.003931116640854 \\ 0.007846541349854 \\ 0.007846541349854 \\ 0.008682770174527 \\ 0.008682770174527 \\ 0.194303338047038 \\ 2.000557696322256 \end{bmatrix} \cdot 1.0e5Hz \tag{2.21}$$

The lowest damping factor is $\varsigma=0.039$ which corresponds to an under-damped system at the resonant frequency $f_{res}=361Hz$. By using (2.19), the range of frequencies Ω is then calculated:

$$f_{\min} = \left(e^{\pi/2}\right)^{-\zeta} f_{res} = 340Hz \quad and \quad f_{\max} = \left(e^{\pi/2}\right)^{\zeta} f_{res} = 383Hz \tag{2.22}$$

Figure 2.31 shows that the bus impedance Nyquist contour has an intersection with the positive real axis within Ω, resulting in a stable system.

In the unstable case, the bus impedance has the following expression

$$Z_{bus}(s) = \frac{16666.6667\,s^2\,(s+1.257e06)\,(s+1.257e05)\,(s^2+791.1s+2.903e05)}{(s^2+4766s+2.431e07)\,(s^2+4766s+2.431e07)} \qquad (2.23)$$
$$\frac{}{(s+1.257e06)\,(s+1.243e05)\,(s+1118)\,(s^2+793.1s+2.835e05)\,(s^2-75.46s+4.638e06)}$$
$$(s^2+4766s+2.431e07)\,(s^2+4991s+2.904e07)$$

The vector of the system damping factors and the system natural frequencies are reported in (2.23).

$$\varsigma = \begin{bmatrix} 0.744755665469081 \\ 0.744755665469081 \\ 1.000000000000000 \\ -0.017520674280632 \\ -0.017520674280632 \\ 0.483387259555926 \\ 0.483387259555926 \\ 0.463045477700980 \\ 0.463045477700980 \\ 1.000000000000000 \\ 1.000000000000000 \end{bmatrix} \quad and \quad f_{res} = \begin{bmatrix} 0.000847419681418 \\ 0.000847419681418 \\ 0.001779704113860 \\ 0.003427398427052 \\ 0.003427398427052 \\ 0.007846541348765 \\ 0.007846541348765 \\ 0.008577322691490 \\ 0.008577322691490 \\ 0.197756607325960 \\ 2.000223157281303 \end{bmatrix} \cdot 1.0e5Hz \qquad (2.24)$$

The negative damping factor is ς=*-0.017* which corresponds to an under-damped (actually unstable) system at the resonant frequency ω_{res}=*342Hz*. By using (2.19), but swapping f_{max} and f_{min} since the damping factor is negative, the range of frequencies Ω is then calculated:

$$f_{\max} = \left(e^{\pi/2}\right)^{-\zeta} f_{res} = 352Hz \qquad and \qquad f_{\min} = \left(e^{\pi/2}\right)^{\zeta} f_{res} = 333Hz \qquad (2.25)$$

Figure 2.32 shows that the bus impedance Nyquist contour has an intersection with the negative real axis within Ω, resulting in an unstable system.

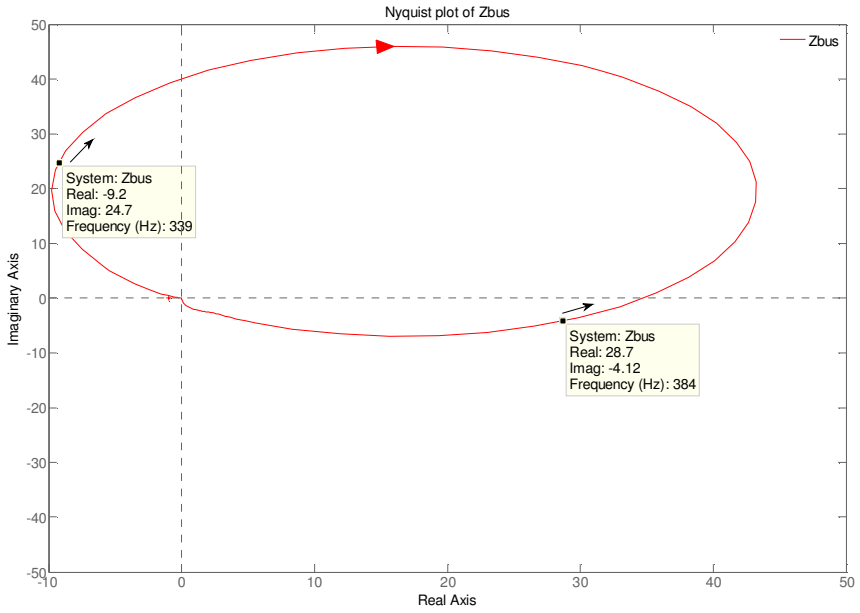


Figure 2.29. Practical PBSC applied to the bus impedance of the cascade of a VM_FB-controlled buck converter and a PICM_FB-controlled VSI (stable case).

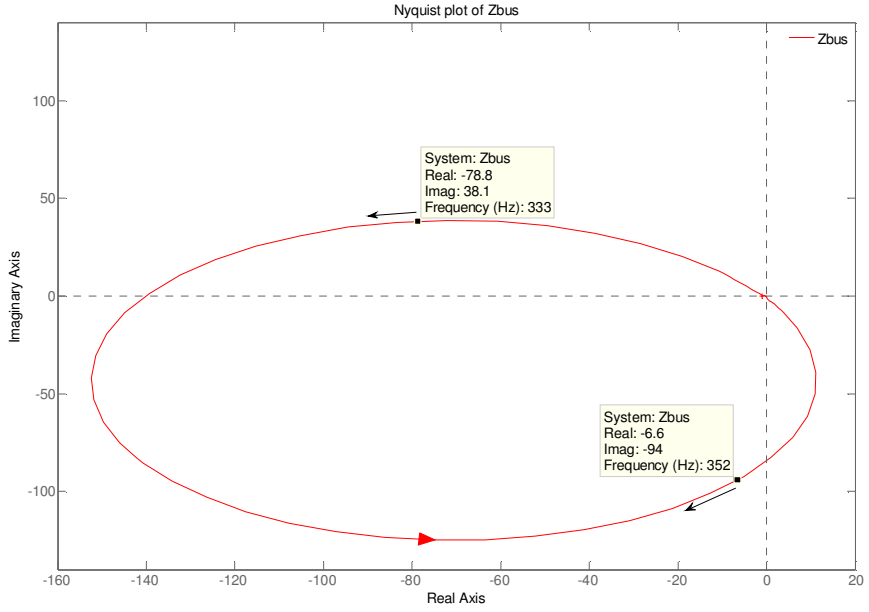


Figure 2.30. Practical PBSC applied to the bus impedance of the cascade of a VM_FB-controlled buck converter and a PICM_FB-controlled VSI (stable case).

The next chapter will show that the PFF control is designed so that system bus impedance passivity is met in Ω. In particular, the PFF control is designed to provide a critically damped system with damping factor equal to 1 at the previously undamped resonant frequency for the system without PFF control.

CHAPTER 3

STABILITY IMPROVEMENT IN DC POWER DISTRIBUTION SYSTEMS

In this chapter the concept of PFF control is given. To understand its effect on system bus stability improvement, the averaged model of a PFF-and-FB-controlled switching converter is provided first. The design formulation for the PFF controller using the practical PBSC, so that both stability and performance are guaranteed, is discussed in detail.

3.1. MODELING OF A CONVERTER IN A DC POWER DISTRIBUTION SYSTEM

A standalone converter is typically fed by an ideal voltage source and feeds a pure resistive load. This is not the case for a switching converter which is part of a DC Power Distribution System. As it is evident from Fig. 3.1, in a DC Power Distribution System a switching converter with both the PFF control and NFB control may be connected to non-ideal source subsystem with complex impedance Z_S and to a non-pure resistive load with another complex impedance Z_L. In such a system both source and load subsystem interactions may bring the system to instability. Even though the switching converter is designed to be standalone stable, when connected to a system like the one in Fig. 3.1, it may exhibits instability due to the effect of subsystem interactions.

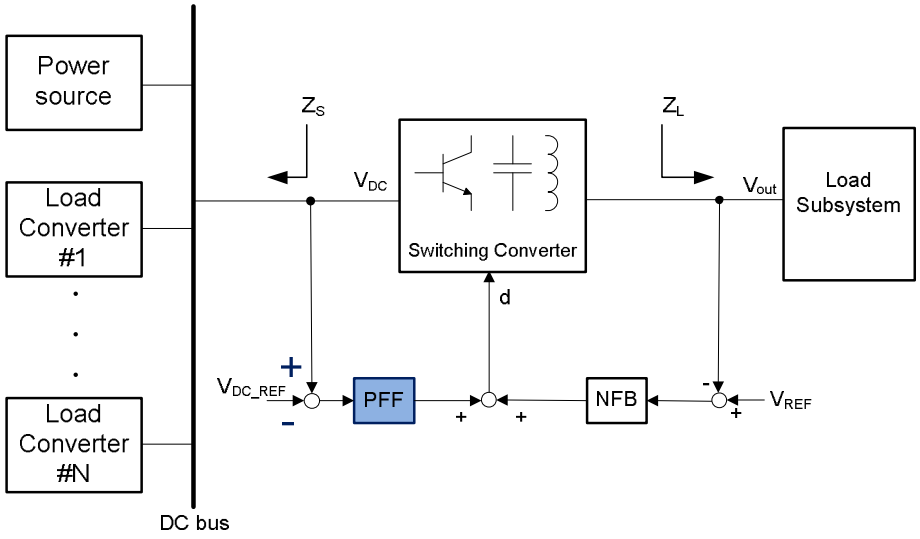


Figure 3.1. Switching converter with both PFF and NFB controllers merged in a DC Power Distribution System.

For the purpose of system stability analysis and controller design, the source and load subsystems are represented as lumped impedances at the input and output ports of the converter, respectively. The converter in Fig. 3.1 can be represented as in Fig. 3.2. The complete small-signal model of the converter with both source and load lumped impedances was given in [45], where the source and load impedances were considered as extra elements in the sense of the Middlebrook's 2EET [29]. Their combined effect on system stability was also studied in [45].

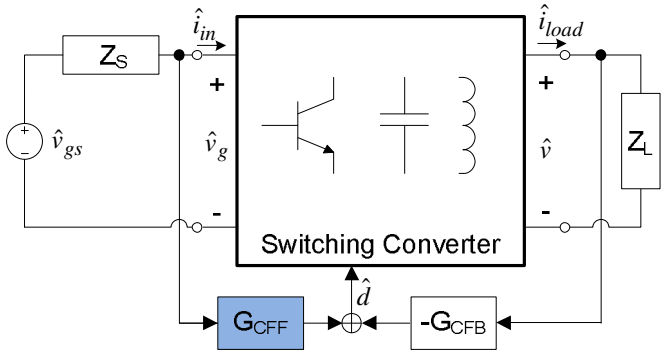


Figure 3.2. Representation of a switching converter with both PFF and NFB controllers with lumped source and load impedances.

Clearly, the dynamics of a switching converter in a DC Power Distribution System can be affected by the subsystems it is connected to. Therefore, as earlier discussed, two types of interactions can be identified: the source subsystem interaction, and the load subsystem interaction. In this work, the focus is on the source subsystem interaction problem, and the proposed PFF control aims to solve such a problem. The single bus system in Fig. 1.1 or its generalization in Fig. 2.1 (a) is taken into consideration. The PFF control is applied to one (or more) load-side converter which is supposed to drive mainly a resistive load, so that load subsystem interaction does not occur.

3.2. SMALL-SIGNAL MODEL OF A CLOSED-LOOP SWITCHING CONVERTER

To understand the concept of PFF control, a complete small-signal model of a PFF-and-FB-controlled (FFFB subscript) switching converter using g-parameter representation [66] is given in this section. First, the standalone modeling is carried out for the two types of control taken into consideration: a Current Mode (CM), and a Voltage Mode (VM) control. After the model is derived for both CM and VM control, the role of PFF control in the passivation of system bus impedance, and, therefore, in the converter input port stabilization, is described. Then, the model including source impedance Z_S is discussed, pointing out that the beneficial input port stability improvement comes at the cost of output performance degradation of the converter.

The small-signal model of the open-loop converter under duty cycle control (OL subscript) based on g-parameter representation can be found in [25, 45, 68] for the case of DC-DC converters and in [47, 48] for the case of a three-phase DC-AC converter. However, for the sake of completeness of the present dissertation, the complete OL

model for the case of DC-DC converters and for the case of a three-phase DC-AC converter is reported in Appendix A.

3.2.1. STANDALONE MODEL OF A SWITCHING CONVERTER IN CM

In CM control, the converter has an inner PI current loop and two outer loops represented by a PI output voltage feedback control and a PFF control as shown in Figs. 3.3 and 3.4. First, the standalone ($Z_S=0$) open-loop PI current mode (PICM) model is given, and then the standalone closed-loop model, including both feed-forward and PICM feedback (PICM_FFFB), is derived.

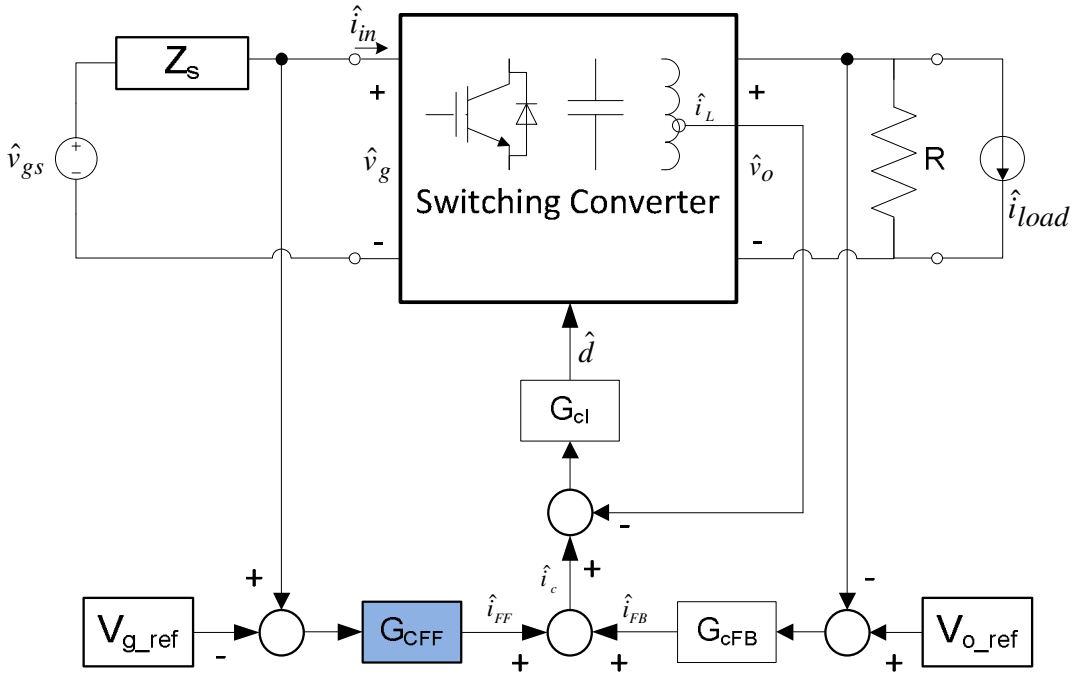


Figure 3.3. Circuital representation of a switching converter with inner PI current loop, outer PI voltage loop, and PFF control.

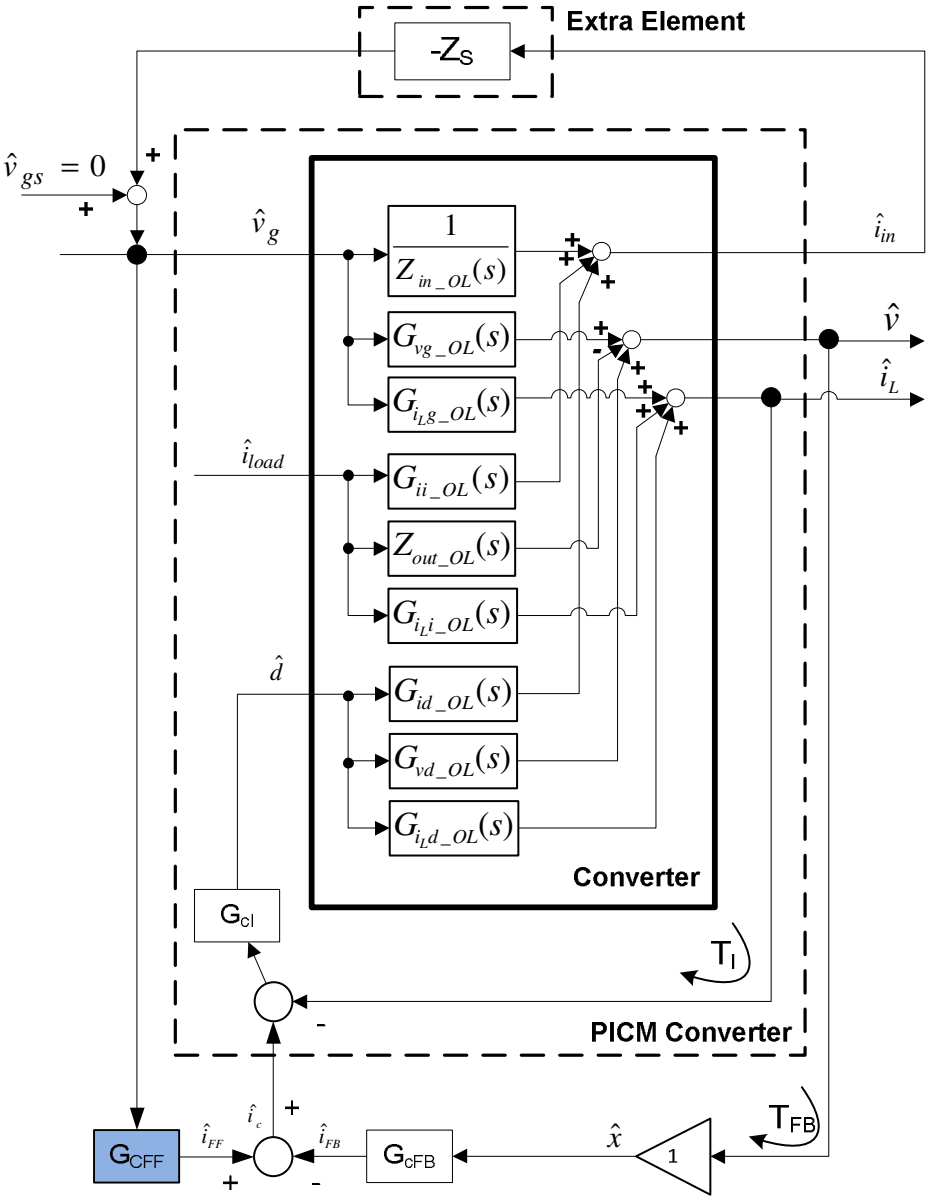


Figure 3.4. Small-signal block diagram representation of a switching converter with inner PI current loop, outer PI voltage loop, and PFF control.

A. Open-loop PICM model

The small-signal linearized open-loop ($G_{cFB}(s)$=0 and $G_{cFF}(s)$=0) PICM converter model has three inputs and three outputs, as shown in Fig. 3.5. The inputs are supply voltage perturbation $\hat{v}_g$, load current perturbation $\hat{i}_{load}$ and control current $\hat{i}_c$. The first

two inputs are disturbances and the third input is the control input. The three outputs are input current perturbation $\hat{i}_{in}$, output voltage perturbation $\hat{v}$ and inductor current perturbation $\hat{i}_L$. The model is

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{v} \\ \hat{i}_L \end{bmatrix} = \begin{bmatrix} \dfrac{1}{Z_{in\_PICM}} & G_{ii\_PICM} & G_{ic\_PICM} \\ G_{vg\_PICM} & -Z_{out\_PICM} & G_{vc\_PICM} \\ G_{i_Lg\_PICM} & G_{i_Li\_PICM} & G_{i_Lc\_PICM} \end{bmatrix} \begin{bmatrix} \hat{v}_g \\ \hat{i}_{load} \\ \hat{i}_c \end{bmatrix} \tag{3.1}$$

The transfer functions for (3.1) are given in (3.2)-(3.10)

$$\frac{1}{Z_{in\_PICM}} = \frac{1}{Z_{in\_OL}} - \frac{G_{id\_OL}G_{i_Lg\_OL}}{G_{i_Ld\_OL}} \frac{T_I}{1+T_I} \tag{3.2}$$

$$G_{ii\_PICM} = G_{ii\_OL} - \frac{G_{id\_OL}G_{i_Li\_OL}}{G_{i_Ld\_OL}} \frac{T_I}{1+T_I} \tag{3.3}$$

$$G_{ic\_PICM} = \frac{G_{id\_OL}}{G_{i_Ld\_OL}} - \frac{G_{id\_OL}G_{i_Lg\_OL}}{G_{i_Ld\_OL}} \frac{T_I}{1+T_I} \tag{3.4}$$

$$G_{vg\_PICM} = G_{vg\_OL} - \frac{G_{vd\_OL}G_{i_Lg\_OL}}{G_{i_Ld\_OL}} \frac{T_I}{1+T_I} \tag{3.5}$$

$$Z_{out\_PICM} = \frac{1}{Z_{in\_OL}} + \frac{G_{vd\_OL}G_{i_Li\_OL}}{G_{i_Ld\_OL}} \frac{T_I}{1+T_I} \tag{3.6}$$

$$G_{vc\_PICM} = \frac{G_{vd\_OL}}{G_{i_Ld\_OL}} \frac{T_I}{1+T_I} \tag{3.7}$$

$$G_{i_Lg\_PICM} = \frac{G_{i_Lg\_OL}}{1+T_I} \tag{3.8}$$

$$G_{i_Li\_PICM} = \frac{G_{i_Li\_OL}}{1+T_I} \tag{3.9}$$

$$G_{i_Lc\_PICM} = \frac{T_I}{1+T_I} \tag{3.10}$$

where $T_I = G_{cI} \cdot G_{iLd\_OL}$.

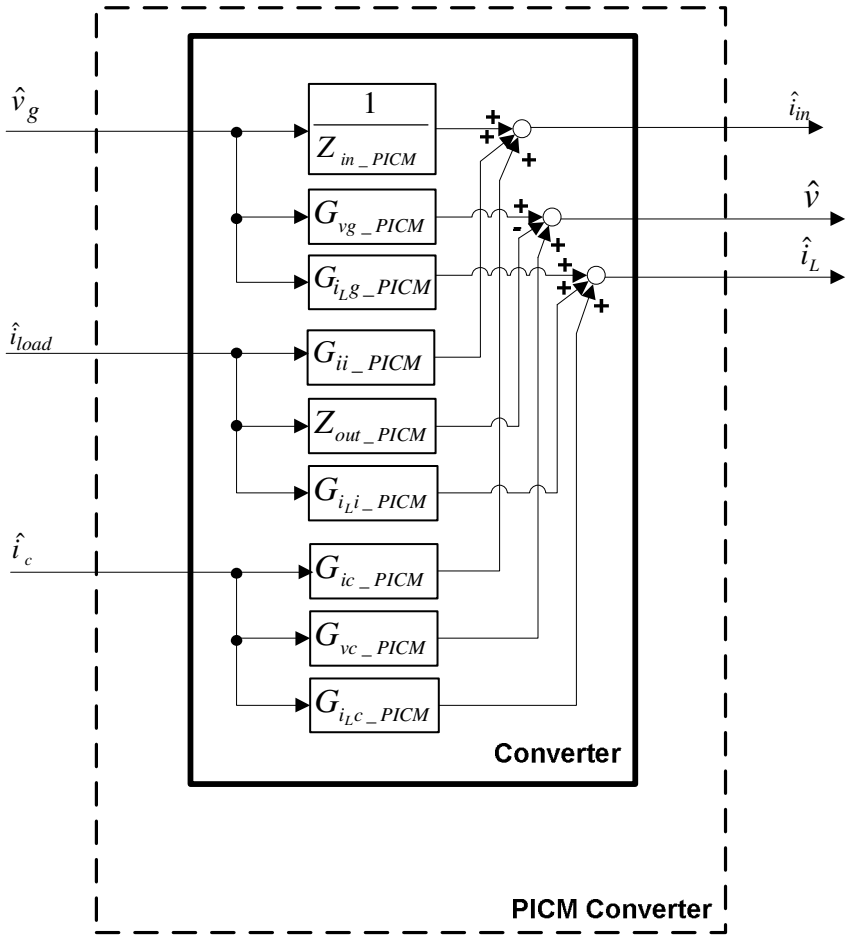


Figure 3.5. Small-signal block diagram representation of a switching converter in CM control.

B. Closed-loop FFFB model

The closed-loop PICM_FFFB converter model (3.11) is obtained from the open-loop PICM converter model (3.1) by imposing a control current $\hat{i}_c = \hat{i}_{FF} - \hat{i}_{FB} = G_{cFF} \cdot \hat{v}_g - G_{cFB} \cdot \hat{v}$

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{v} \end{bmatrix} = \begin{bmatrix} \frac{1}{Z_{in\_PICM\_FFFB}} & G_{ii\_PICM\_FFFB} \\ G_{vg\_PICM\_FFFB} & -Z_{out\_PICM\_FFFB} \end{bmatrix} \begin{bmatrix} \hat{v}_g \\ \hat{i}_{load} \end{bmatrix} \tag{3.11}$$

The transfer functions of model (3.11) are given in (3.12)-(3.15). Notice that for the case of a three-phase DC-AC converter, the model is developed in the *dq*

synchronous reference frame and therefore the elements $G_{ii\_PICM\_FFFB}$, $G_{vg\_PICM\_FFFB}$, and $Z_{out\_PICM\_FFFB}$ of the matrix in (3.11) are 2x2 sub-matrices.

$$\frac{1}{Z_{in\_PICM\_FFFB}} = \left\{\frac{1}{Z_{in\_PICM}}\frac{1}{1+T_{PICM\_FB}} + \frac{1}{Z_{N\_vc\_PICM}}\frac{T_{PICM\_FB}}{1+T_{PICM\_FB}}\right\} + \left\{\frac{T_{PICM\_FF}}{1+T_{PICM\_FB}}\right\} \tag{3.12}$$
$$= \left\{\frac{1}{Z_{in\_PICM\_FB}}\right\} + \left\{\frac{1}{Z_{damp}}\right\}$$

$$G_{ii\_PICM\_FFFB} = G_{ii\_PICM} + \frac{G_{ic\_PICM}Z_{out\_PICM}}{G_{vc\_PICM}} \cdot \frac{T_{PICM\_FB}}{1+T_{PICM\_FB}} = G_{ii\_PICM\_FB} \tag{3.13}$$

$$G_{vg\_PICM\_FFFB} = \left\{\frac{G_{vg\_PICM}}{1+T_{PICM\_FB}}\right\} + \frac{G_{vc\_PICM}}{G_{ic\_PICM}} \cdot \left\{\frac{T_{PICM\_FF}}{1+T_{PICM\_FB}}\right\} \tag{3.14}$$
$$= \left\{G_{vg\_PICM\_FB}\right\} + \frac{G_{vc\_PICM}}{G_{ic\_PICM}} \cdot \left\{\frac{1}{Z_{damp}}\right\}$$

$$Z_{out\_PICM\_FFFB} = \frac{Z_{out\_PICM}}{1+T_{PICM\_FB}} = Z_{out\_PICM\_FB} \tag{3.15}$$

where

$$\frac{1}{Z_{N\_vc\_PICM}} = \frac{1}{Z_{in\_PICM}} - \frac{G_{ic\_PICM}G_{vg\_PICM}}{G_{vc\_PICM}} \tag{3.16}$$

$T_{PICM\_FB}=G_{cFB}\cdot G_{vc\_PICM}$ is the FB loop gain and $T_{PICM\_FF}=G_{cFF}\cdot G_{ic\_PICM}$ is the FF gain, respectively. Notice that FF gain has dimensions of admittance [45-48]. Also, the special cases of PICM_FB control only and PICM_FF control only can be found from the more general PICM_FFFB model (3.11) and (3.12)-(3.15) by imposing $G_{cFF}=0$ ($T_{PICM\_FF}=0$) and $G_{cFB}=0$ ($T_{PICM\_FB}=0$), respectively.

3.2.2. STANDALONE MODEL OF A SWITCHING CONVERTER IN VM

In VM control, the converter has two loops represented by a PID voltage control and a PFF control as shown in Figs. 3.6 and 3.7. The standalone ($Z_S=0$) small-signal model of the OL converter under duty cycle control is given in Appendix A. The

standalone closed-loop model, including both feed-forward and VM feedback (VM_FFFB), is derived.

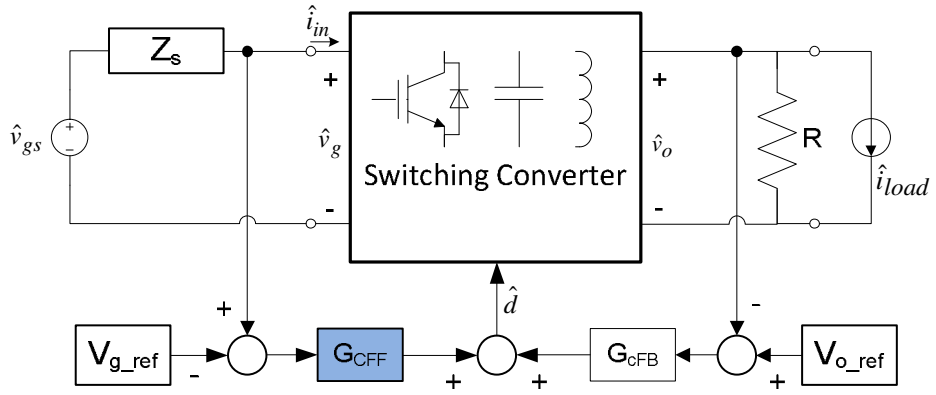


Figure 3.6. Circuital representation of a switching converter with PID voltage loop, and PFF control.

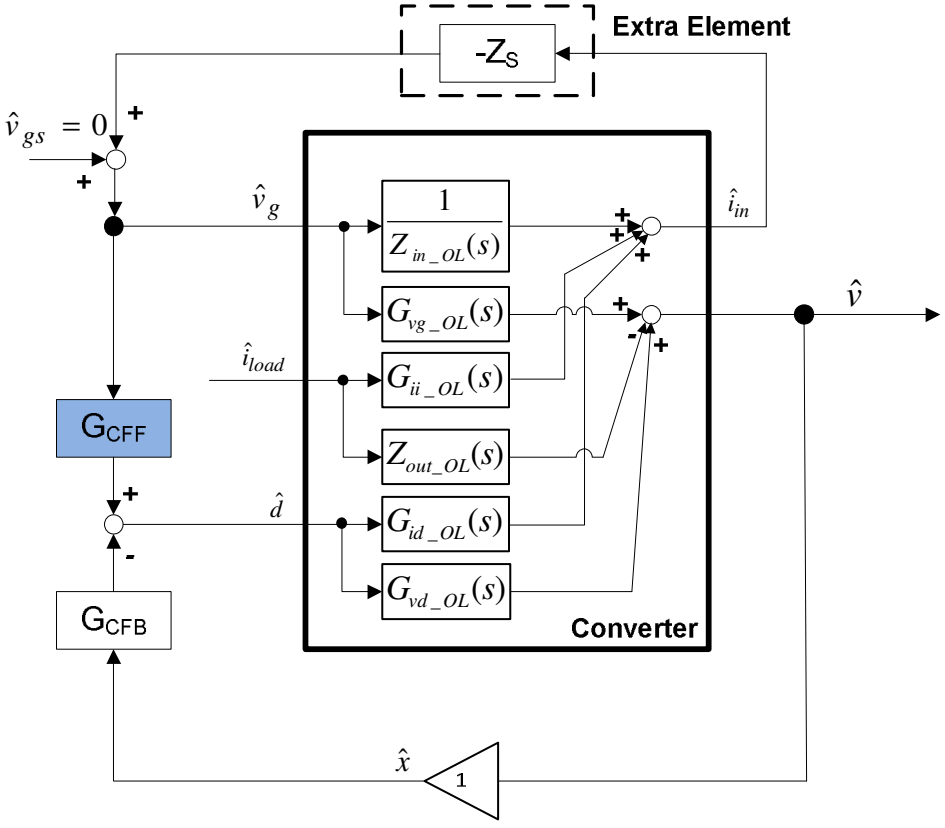


Figure 3.7. Small-signal block diagram representation of a switching converter with PID voltage loop, and PFF control.

A. Closed-loop FFFB model

The closed-loop VM_FFFB converter model (3.17) is obtained from the OL converter model (A.1) given in Appendix A by imposing a control signal $\hat{d} = -G_{cFB}\hat{v} + G_{cFF}\hat{v}_g$

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{v} \end{bmatrix} = \begin{bmatrix} \dfrac{1}{Z_{in\_VM\_FFFB}} & G_{ii\_VM\_FFFB} \\ G_{vg\_VM\_FFFB} & -Z_{out\_VM\_FFFB} \end{bmatrix} \begin{bmatrix} \hat{v}_g \\ \hat{i}_{load} \end{bmatrix} \tag{3.17}$$

The transfer functions of model (3.17) are given in (3.18)-(3.21). Notice that for the case of a three-phase DC-AC converter, the model is developed in the *dq* synchronous reference frame and therefore the elements G_{ii_FFFB}, G_{vg_FFFB}, and Z_{out_FFFB} of the matrix in (3.11) are 2x2 sub-matrices.

$$\begin{aligned} \frac{1}{Z_{in\_VM\_FFFB}} &= \left\{ \frac{1}{Z_{in\_OL}} \frac{1}{1+T_{VM\_FB}} + \frac{1}{Z_{N\_vd\_OL}} \frac{T_{VM\_FB}}{1+T_{VM\_FB}} \right\} + \left\{ \frac{T_{VM\_FF}}{1+T_{VM\_FB}} \right\} \\ &= \left\{ \frac{1}{Z_{in\_FB}} \right\} + \left\{ \frac{1}{Z_{damp}} \right\} \end{aligned} \tag{3.18}$$

$$G_{ii\_VM\_FFFB} = G_{ii\_OL} + \frac{G_{id\_OL} Z_{out\_OL}}{G_{vd\_OL}} \cdot \frac{T_{VM\_FB}}{1+T_{VM\_FB}} = G_{ii\_FB} \tag{3.19}$$

$$\begin{aligned} G_{vg\_VM\_FFFB} &= \left\{ \frac{G_{vg\_OL}}{1+T_{FB}} \right\} + \frac{G_{vd\_OL}}{G_{id\_OL}} \cdot \left\{ \frac{T_{VM\_FF}}{1+T_{VM\_FB}} \right\} \\ &= \left\{ G_{vg\_VM\_FB} \right\} + \frac{G_{vd\_OL}}{G_{id\_OL}} \cdot \left\{ \frac{1}{Z_{damp}} \right\} \end{aligned} \tag{3.20}$$

$$Z_{out\_VM\_FFFB} = \frac{Z_{out\_OL}}{1+T_{VM\_FB}} = Z_{out\_VM\_FB} \tag{3.21}$$

where

$$\frac{1}{Z_{N\_vd\_OL}} = \frac{1}{Z_{in\_OL}} - \frac{G_{id\_OL} G_{vg\_OL}}{G_{vd\_OL}} \tag{3.22}$$

$T_{VM\_FB}=G_{cFB}\cdot G_{vd\_OL}$ is the FB loop gain and $T_{VM\_FF}=G_{cFF}\cdot G_{id\_OL}$ is the FF gain. Again, the special cases of FB control only and PFF control only can be found from the more general VM_FFFB model (3.17) and (3.18)-(3.21) by imposing $G_{cFF}=0$ ($T_{VM\_FF}=0$) and $G_{cFB}=0$ ($T_{VM\_FB}=0$), respectively.

3.2.3. EFFECT OF PFF CONTROL

The expressions for the input impedance in CM (3.12) and in VM (3.18) show that the PFF control provides a way to control the converter input impedance through the last term on the right hand side of (3.12) and (3.18). In particular, the PFF control has the effect of actively introducing damping impedance Z_{damp} in parallel to the already existing Z_{in_FB} with the goal of stabilizing the system. Given a desired stabilizing impedance Z_{damp}, designed so that the bus impedance satisfies the practical PBSC (details in the next section), the transfer function of the PFF controller is easily found from the last term on the right hand side of (3.12) for CM of (3.18) for VM and from the expression of the FF gains:

$$G_{cFF}=\begin{cases}\dfrac{T_{PICM\_FF}}{G_{ic\_PICM}}=\dfrac{1+T_{PICM\_FB}}{G_{ic\_PICM}\cdot Z_{damp}} & for\ PICM\_FFFB\\ G_{cFF}=\dfrac{T_{VM\_FF}}{G_{id\_OL}}=\dfrac{1+T_{VM\_FB}}{G_{id\_OL}\cdot Z_{damp}} & for\ VM\_FFFB\end{cases} \tag{3.23}$$

Fig. 3.8 shows the equivalent two-port network terminal model [68, 69] connected to a non-ideal source impedance Z_S, directly drawn from model (3.11) or (3.17), for the case of the addition of PFF control to FB control. The feed-forward action introduces two additional elements, impedance Z_{damp} on the input side and a controlled voltage source on the output side. The impedance Z_{damp} stabilizes the bus, but at a cost: the output side voltage source has a negative effect on the audio susceptibility transfer functions defined

in (3.14) and (3.20). This represents a tradeoff between stability improvement and output performance degradation. In fact, as it will be shown in the next section, on the one hand the addition of Z_{damp} small in magnitude at the source subsystem resonant frequency ω_{res} (so that it dominates to solve the passivity violation problem) is desired for stability improvement purposes, on the other hand it negatively affects the audio-susceptibility transfer functions (3.14) and (3.20). This is contrasted with the conventional NFF control [50-58], which instead suppresses the audio susceptibility, but at the cost of input port destabilization.

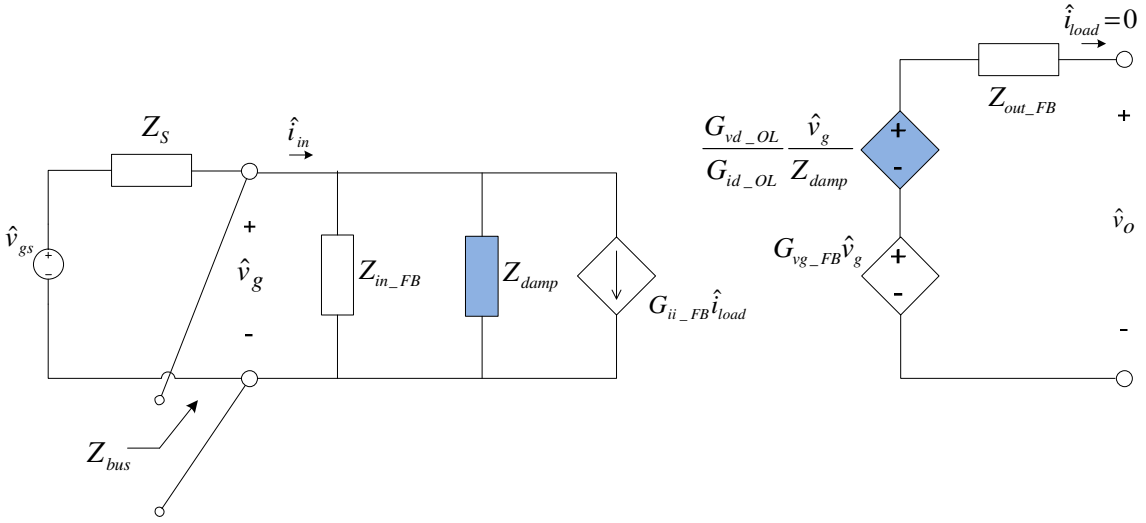


Figure 3.8. Source impedance Z_S connected to the input port of the equivalent circuital model of a switching converter.

It is evident that the output performance of a switching converter is degraded not only by source subsystem interaction (the presence of Z_S in the source subsystem), but also by the addition of the PFF control to the FB control. In particular, the FB loop gain will be modified by the presence of Z_S and the addition of PFF control to the FB control. For source subsystem interaction with no PFF control ($G_{cFF}=0$), the output impedance of the source subsystem can be regarded as an extra element as shown in Figs. 3.4 and 3.7.

The transfer functions modified by the source subsystem interaction are obtained in the form of the original transfer function multiplied by the correction factor according to the EET [28] (see Appendix B). The FB loop gain affected by the source impedance only is

$$T_{FB\_ZS} = \begin{cases} T_{PICM\_FB} \dfrac{1+\dfrac{Z_S}{Z_{N\_vc\_OL}}}{1+\dfrac{Z_S}{Z_{in\_PICM}}} & for\ PICM\_FFFB \\ T_{VM\_FB} \dfrac{1+\dfrac{Z_S}{Z_{N\_vd\_OL}}}{1+\dfrac{Z_S}{Z_{in\_OL}}} & for\ VM\_FFFB \end{cases} \tag{3.24}$$

The inclusion of the PFF control as well alters the expression of correction factor in (3.24). The expression of the FB loop gain affected by the presence of both the non-ideal source impedance Z_S and the PFF control, which actively introduces Z_{damp} at the input port, can be easily found from Figs. 3.4 and 3.6 as

$$T_{FB\_Z_S\_FF} = \frac{\hat{v}}{-\hat{x}} = \begin{cases} T_{PICM\_FB} \dfrac{1+\dfrac{Z_S}{Z_{N\_vc\_OL}}}{1+Z_S \cdot \left(\dfrac{1}{Z_{in\_PICM}} + \dfrac{1+T_{PICM\_FB}}{Z_{damp}} \right)} & for\ PICM\_FFFB \\ T_{VM\_FB} \dfrac{1+\dfrac{Z_S}{Z_{N\_vd\_OL}}}{1+Z_S \cdot \left(\dfrac{1}{Z_{in\_OL}} + \dfrac{1+T_{VM\_FB}}{Z_{damp}} \right)} & for\ VM\_FFFB \end{cases} \tag{3.25}$$

Even though the PFF control provides an active way to stabilize the DC bus, the price to be paid is that it negatively affects the FB bandwidth of the converter it is applied to. Special cases of no-interactions and no-PFF control can be found by imposing $Z_S=0$ and $Z_{damp}=\infty$, respectively. Notice that without interactions ($Z_S=0$), the presence of the PFF control has no effect on the FB loop gain.

Therefore, since the addition of the PFF control alters the FB loop gain, Z_{damp} should be carefully chosen. Next section will provide the design formulation for Z_{damp}, so that both input stability improvement and the desired output performance are guaranteed.

3.3. PFF CONTROL DESIGN USING THE PRACTICAL PBSC

As discussed earlier, the PFF control has the effect of introducing damping impedance Z_{damp} in parallel to the already existing Z_{in_FB}. The goal of the introduction of damping impedance Z_{damp} is to stabilize the DC bus voltage by *modifying the bus impedance only in the frequency range where the original impedance* Z_{bus_FB} *violates the passivity criterion*. Z_{bus_FFFB} is the bus impedance resulting from the addition of the PFF control. Fig. 3.9 graphically summarizes the action of Z_{damp} on bus voltage stabilization.

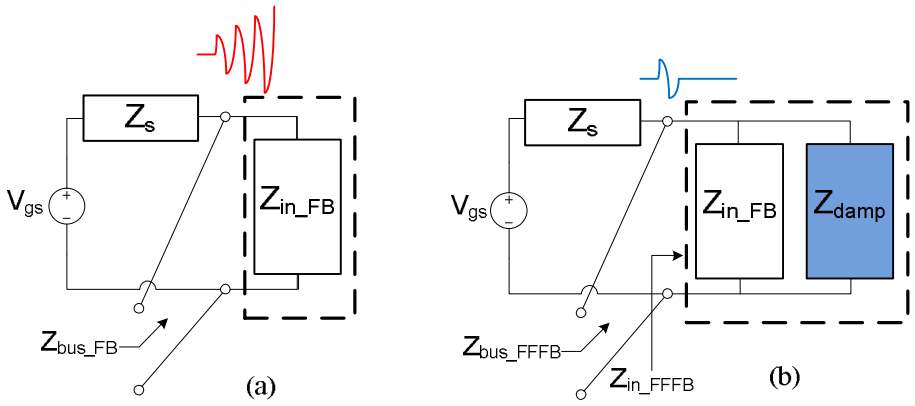
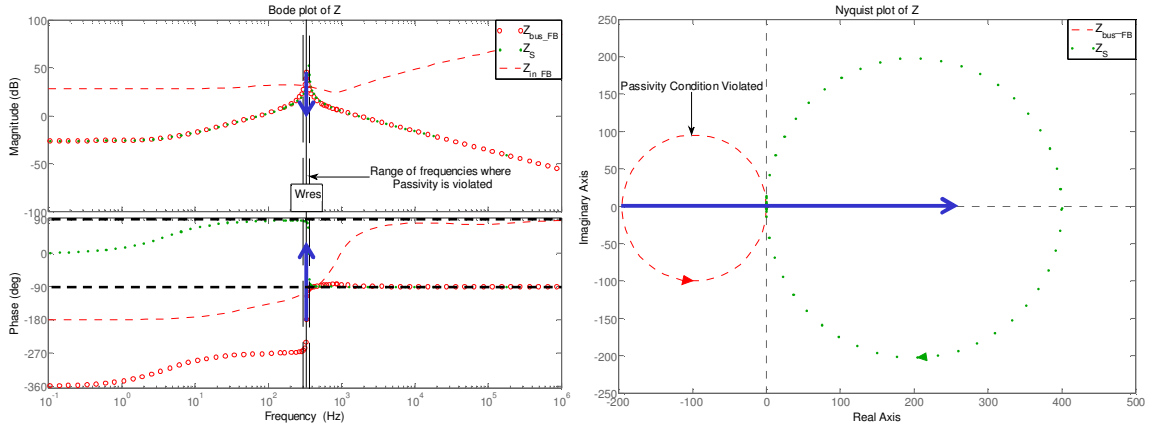


Figure 3.9. Source impedance Z_S connected to the equivalent input port of the switching converter: (a) unstable, (b) stable cases.

As proved in Chapter II, passivity condition for Z_{bus_FB} is usually violated at ω_{res}, i.e. the frequency where Z_{bus_FB} exhibits resonance, as shown in Fig. 3.10. Impedance Z_{bus_FB} follows the output impedance of the source subsystem Z_S everywhere except around the range of frequencies where it exhibits resonance (in the parallel combination the smaller impedance dominates). Fig. 3.10 (a) shows the Bode plot of the relevant

impedances highlighting that the passivity condition violation means that the phase of the bus impedance is outside the range $-90^{\circ} \div +90^{\circ}$ at frequencies around the resonant frequency ω_{res}. Fig. 3.10 (b) shows the Nyquist plot of the same relevant impedances highlighting that the passivity condition violation means that Z_{bus_FB} exhibits negative real part at frequencies around ω_{res}.



(a) **(b)**

Figure 3.10. Bode plot (a) and Nyquist plot (b) of the impedances Z_{bus_FB}. The blue arrows represent the desired passivation of the bus impedance.

To solve the passivity condition violation, i.e. to bring Z_{bus} to the RHP so that it exhibits positive real part at frequencies around ω_{res}, the PFF control is added to the conventional FB control. The addition of PFF control has the effect of adding the damping impedance Z_{damp} in parallel to existing Z_S and Z_{in_FB} (Fig. 3.9 (b)). If Z_{damp} is designed so that

$$\frac{1}{Z_{bus\_FFFB}} = \frac{1}{Z_S} + \frac{1}{Z_{in\_FB}} + \frac{1}{Z_{damp}}$$
$$\approx \begin{cases} \frac{1}{Z_S} & at\ low\ frequencies \\ \frac{1}{Z_{damp}} & at\ \omega = \omega_{res} \\ \frac{1}{Z_S} & at\ high\ frequencies \end{cases} \tag{3.26}$$

the passivity violation can be solved. In other words, (3.26) shows that if Z_{damp} is designed so that it dominates at ω_{res} (note, again, that in the parallel combination the smallest impedance dominates), it can provide the desired passivation effect (see blue arrows in Fig. 3.10 (a)), i.e. $-90° \leq arg[Z_{bus\_FFFB}(j\omega_{res})] \leq 90°$ while leaving the bus impedance unchanged everywhere else. This is also equivalent to moving the Nyquist plot of the bus impedance from the LHP to the RHP, as the blue arrow in Fig. 3.10 (b) indicates.

Now, mathematical formulations for the design of the PFF controller are provided. Three cases are described:

$$Z_{damp} = \begin{cases} \frac{1}{sC_b} & (A): C_b\ parallel\ damping \\ R_b + \frac{1}{sC_b} & (B): R_b - C_b\ parallel\ damping \\ sL_b + R_b + \frac{1}{sC_b} & (C): L_b - R_b - C_b\ parallel\ damping \end{cases} \tag{3.27}$$

where C_b, L_b, and R_b are virtual capacitor, inductor and resistor that can be added through PFF control to provide the desired stabilizing effect.

The design procedure, graphically depicted in Fig. 3.11, is as follows. The design starts from the choice of a desired crossover frequency for the load subsystem, which means desired output performance, in the presence of source impedance Z_S and PFF

control. This crossover frequency, which is called $\omega_{c\_Zs\_FF}$, should be smaller than resonant frequency ω_{res} of the bus impedance Z_{bus_FB}, so $\omega_{c\_Zs\_FF}<\omega_{res}$. If $\omega_{c\_Zs\_FF}$ is chosen too low, output performance is affected (low FB bandwidth, sluggish response), but, if it chosen too close to ω_{res}, it may be difficult to achieve good passivation action. The second step is to impose the passivity condition on bus impedance Z_{bus_FFFB} by proper design of virtual damping impedance Z_{damp} according to (3.26). In particular the phase constraint for passivity must be satisfied at the resonant frequency ω_{res}: $-90° \leq arg[Z_{bus\_FFFB}(j\omega_{res})] \leq 90°$. At this point, the designer has to choose the type of damping impedance. Notice that Z_{damp} can be chosen to be either passive or active impedance. For the purposes of this work, only passive impedances are considered. Three types of passive parallel damping are considered: C_b, R_b-C_b, and L_b-R_b-C_b parallel damping. Three slightly different design procedures are used to find relationships among the parameters to be determined. In order to force $\omega_{c\_Zs\_FF}$ to be the FB crossover frequency, the condition $||T_{FB\_ZS\_FF}(j\omega_{c\_Zs\_FF})||=1$ is imposed using (3.25). From this condition $||Z_{damp}(j\omega_{c\_Zs\_FF})||$ can be found as a function of OL and FB quantities only. Then, according to the chosen parallel damping impedance, (3.27) can be used to determine all other parameters that need to be designed. Once Z_{damp} is determined, the PFF controller transfer function is calculated using (3.23). At the end of this process, if a good tradeoff between stability improvement and output performance is obtained, the procedures stops, otherwise it has to be iterated starting from the choice of a different desired crossover frequency $\omega_{c\_Zs\_FF}$.

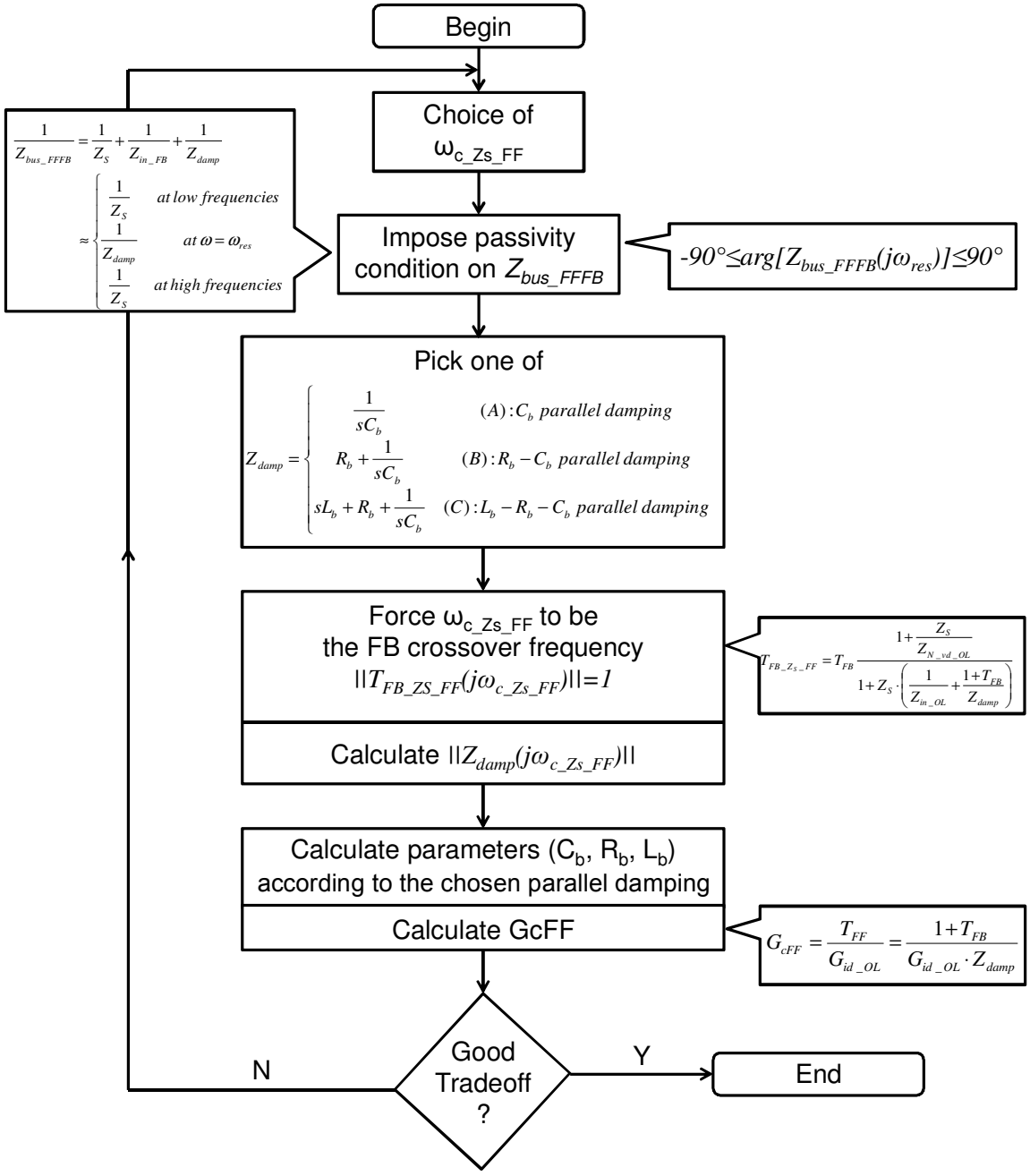


Figure 3.11. Flow chart of the PFF control design procedure using the practical PBSC.

A. C_b parallel damping

Even though not good as a practical approach, the use of a pure capacitor as damping impedance gives a simplified case, which is useful to gain understanding of the

method. With a pure capacitor as damping impedance, from (6) and (7) the phase of the bus impedance at the resonant frequency is

$$\begin{aligned}\arg\left[Z_{bus\_FFFB}(j\omega_{res})\right] &\approx \arg\left[Z_{damp}(j\omega_{res})\right] \\ &= \arg\left[\frac{1}{j\omega_{res}C_b}\right] = -90^\circ\end{aligned} \tag{3.28}$$

Only a marginally passive (and stable) system can be obtained, which explains why this choice of damping impedance is not practical. Another problem with this solution, which will be better explained in the next section, is the need of choosing a significantly low FB bandwidth to guarantee bus impedance passivity. At the crossover frequency $\omega_{c\_Zs\_FF}$ the magnitude of (3.25) is equal to 1.

$$\begin{aligned}&\left\|T_{FB\_Z_S\_FF}(j\omega_{c\_Zs\_FF})\right\| = 1 \\ &\left\|T_{FB}(j\omega_{c\_Zs\_FF})\right\| \cdot \frac{\left\|1+\frac{Z_S(j\omega_{c\_Zs\_FF})}{Z_{N\_vd\_OL}(j\omega_{c\_Zs\_FF})}\right\|}{\left\|1+\frac{Z_S(j\omega_{c\_Zs\_FF})}{Z_{in\_OL}(j\omega_{c\_Zs\_FF})}\cdot\left(1+Z_{in\_OL}(j\omega_{c\_Zs\_FF})\cdot\frac{1+T_{FB}(j\omega_{c\_Zs\_FF})}{Z_{damp}(j\omega_{c\_Zs\_FF})}\right)\right\|} = 1\end{aligned} \tag{3.29}$$

Bringing $||Z_{damp}(j\omega_{c\_Zs\_FF})||$ on the left hand side of (3.29) and all the other terms to the right hand side, it yields an inequality (refer to Appendix C for calculations)

$$\left\|Z_{damp}(j\omega_{c\_Zs\_FF})\right\| \le M \tag{3.30}$$

where the expression for M is given by

$$M \triangleq \frac{\left\|Z_S(j\omega_{c\_Zs\_FF})\cdot Z_{in\_OL}(j\omega_{c\_Zs\_FF})\cdot\left(1+T_{FB}(j\omega_{c\_Zs\_FF})\right)\right\|}{\left\|T_{FB}(j\omega_{c\_Zs\_FF})\right\|\cdot\left\|1+\frac{Z_S(j\omega_{c\_Zs\_FF})}{Z_{N\_vd\_OL}(j\omega_{c\_Zs\_FF})}\right\|\cdot\left\|Z_{in\_OL}(j\omega_{c\_Zs\_FF})\right\| - \left\|Z_{in\_OL}(j\omega_{c\_Zs\_FF})+Z_S(j\omega_{c\_Zs\_FF})\right\|} \tag{3.31}$$

In other words, $||Z_{damp}(j\omega_{c\_Zs\_FF})||$ is the term that, if correctly designed, guarantees not only bus impedance passivity and therefore stability, but also the desired crossover frequency and therefore desired output performance. However, since solving (3.29) algebraically brings to the inequality (3.30), to get the desired crossover frequency,

some iteration is needed. The term M depends only on open-loop (OL) and feedback (FB) quantities, and does not depends on FF control. The only term that depends on FF control is, of course, Z_{damp}.

Being Z_{damp} a pure capacitor, for a desired FB crossover frequency $\omega_{c\_Zs\_FF}$, capacitor C_b, is the only parameter that needs to be designed for this case

$$\begin{aligned} &\left\| Z_{damp}(j\omega_{c\_Zs\_FF}) \right\| = \left\| \frac{1}{j\omega_{c\_Zs\_FF} C_b} \right\| \le M \\ &\xrightarrow{\text{solving for } C_b} \qquad C_b \ge \frac{1}{M \cdot \omega_{c\_Zs\_FF}} \end{aligned} \tag{3.32}$$

Notice that if the desired crossover frequency is chosen at a reasonably low frequency for stable operation, some simplifications on M can be made as described in the Appendix C, yielding the following relationship

$$\left\| Z_{damp}(j\omega_{c\_Zs\_FF}) \right\| \le M \approx \left\| Z_S(j\omega_{c\_Zs\_FF}) \right\| \tag{3.33}$$

B. R_b-C_b parallel damping

The addition of a resistor to the capacitor improves the design. For this case, from (3.26) and (3.27) the phase of the bus impedance at the resonant frequency is

$$\begin{aligned} &\arg\left[Z_{bus\_FFFB}(j\omega_{res}) \right] \approx \arg\left[Z_{damp}(j\omega_{res}) \right] \\ &= \arg\left[R_b + \frac{1}{j\omega_{res} C_b} \right] = \arg\left[\frac{1 + j\omega_{res} R_b C_b}{j\omega_{res} C_b} \right] \\ &= -90^\circ + \tan^{-1}\left(\omega_{res} R_b C_b \right) \end{aligned} \tag{3.34}$$

Equation (3.34) can be rewritten as

$$\begin{aligned} &\tan^{-1}\left(\omega_{res} R_b C_b \right) = 90^\circ + \arg\left[Z_{bus\_FFFB}(j\omega_{res}) \right] \\ &\tau_b \triangleq R_b C_b = \frac{\tan\left(90^\circ + \arg\left[Z_{bus\_FFFB}(j\omega_{res}) \right] \right)}{\omega_{res}} \end{aligned} \tag{3.35}$$

This time, we have another parameter that must be designed, i.e. R_b. For this reason, at this point we can find the product $\tau_b=C_bR_b$ for a desired phase of the bus impedance at the resonant frequency. Note that the phase of the bus impedance cannot be chosen to be equal to $0°$. However, it is desired that $arg[Z_{bus\_FFFB}(j\omega_{res})]$ be as close as possible to $0°$ to offer the best passivation action. A reasonable choice is

$$\arg\left[Z_{bus\_FFFB}(j\omega_{res})\right]=-5^{\circ} \tag{3.36}$$

Once again, $||Z_{damp}(j\omega_{c\_Zs\_FF})||$ is the term extracted by taking the magnitude of (3.25) and making it equal to 1 that, if correctly designed, guarantees not only bus impedance passivity and therefore stability, but also the desired crossover frequency. As before, imposing (3.29), one obtains (3.30). Being Z_{damp} the series of a capacitor and a resistor, for a desired FB crossover frequency $\omega_{c\_Zs\_FF}$, C_b is calculated as

$$\begin{aligned}
&\left\|Z_{damp}(j\omega_{c_Zs_FF})\right\|=\left\|R_b+\frac{1}{j\omega_{c_Zs_FF}C_b}\right\| \\
&=\frac{\sqrt{1+\left(\omega_{c_Zs_FF}R_bC_b\right)^2}}{\omega_{c_Zs_FF}C_b}=\frac{\sqrt{1+\left(\omega_{c_Zs_FF}\tau_b\right)^2}}{\omega_{c_Zs_FF}C_b}\le M \\
&\xrightarrow{\text{solving for } C_b} \qquad C_b\ge\frac{\sqrt{1+\left(\omega_{c_Zs_FF}\tau_b\right)^2}}{\omega_{c_Zs_FF}M}
\end{aligned} \tag{3.37}$$

Once τ_b and C_b are found from (3.35) and (3.37) respectively, R_b is directly calculated as

$$R_b=\frac{\tau_b}{C_b} \tag{3.38}$$

C. L_b-R_b-C_b parallel damping

The addition of an inductor further improves the design. For this case, from (3.26) and (3.27) the phase of the bus impedance at the resonant frequency is

$$\begin{aligned}
&\arg\left[Z_{bus_FFFB}(j\omega_{res})\right] \approx \arg\left[Z_{damp}(j\omega_{res})\right] \\
&= \arg\left[j\omega_{res}L_b + R_b + \frac{1}{j\omega_{res}C_b} \right] \\
&= \arg\left[\frac{1 + j\omega_{res}R_bC_b - \omega_{res}^{\ 2}L_bC_b}{j\omega_{res}C_b} \right]
\end{aligned} \tag{3.39}$$

To get the best bus impedance passivity condition, i.e. $arg[Z_{bus\_FFFB}(j\omega_{res})]=0°$, the following equality should be satisfied

$$1 - \omega_{res}^{\ 2}L_bC_b = 0 \qquad \rightarrow \qquad \omega_{res} = \frac{1}{\sqrt{L_bC_b}} \tag{3.40}$$

The numerator of Z_{damp} given in (3.27) can be written as

$$1 + sR_bC_b + s^2L_bC_b \triangleq 1 + \frac{s}{\omega_{res} \cdot Q} + \frac{s^2}{\omega_{res}^{\ 2}} \tag{3.41}$$

With the choice of $Q=0.5$ (damping factor $\zeta=1/(2Q)=1$) equation (3.41) gives other two design relationships

$$\tau_b = R_bC_b = \frac{2}{\omega_{res}} \qquad and \qquad \omega_{res} = \frac{1}{\sqrt{L_bC_b}} \tag{3.42}$$

Actually, the second relationship of (3.42) was already found in (3.40), which gives the condition for the best achievable passivity condition, i.e. $arg[Z_{bus\_FFFB}(j\omega_{res})]=0°$. Once again, $||Z_{damp}(j\omega_{c\_Zs\_FF})||$ is the term extracted by taking the magnitude of (3.25) and making it equal to 1 that, if correctly designed, guarantees not only bus impedance passivity and therefore stability, but also the desired crossover frequency. As previously done in (3.29), the result is identical to (3.30). Being Z_{damp} the series of an inductor, a capacitor, and a resistor, for a desired FB crossover frequency $\omega_{c\_Zs\_FF}$, C_b is calculated as

$$\left\| Z_{damp}(j\omega_{c\_Zs\_FF}) \right\| = \left\| sL_b + R_b + \frac{1}{j\omega_{c\_Zs\_FF} C_b} \right\|$$

$$= \frac{\sqrt{\left(1 - \omega_{c\_Zs\_FF}{}^2 / \omega_{res}{}^2\right)^2 + \left(\omega_{c\_Zs\_FF}\tau_b\right)^2}}{\omega_{c\_Zs\_FF} C_b} \le M \tag{3.43}$$

$$\xrightarrow{\text{solving for } C_b} \; C_b \ge \frac{\sqrt{\left(1 - \omega_{c\_Zs\_FF}{}^2 / \omega_{res}{}^2\right)^2 + \left(\omega_{c\_Zs\_FF}\tau_b\right)^2}}{\omega_{c\_Zs\_FF} M}$$

Once τ_b and C_b are found from (3.42) and (3.43) respectively, R_b and L_b are directly calculated as

$$R_b = \frac{\tau_b}{C_b} \quad and \quad L_b = \frac{1}{\omega_{res}{}^2 C_b} \tag{3.44}$$

CHAPTER 4

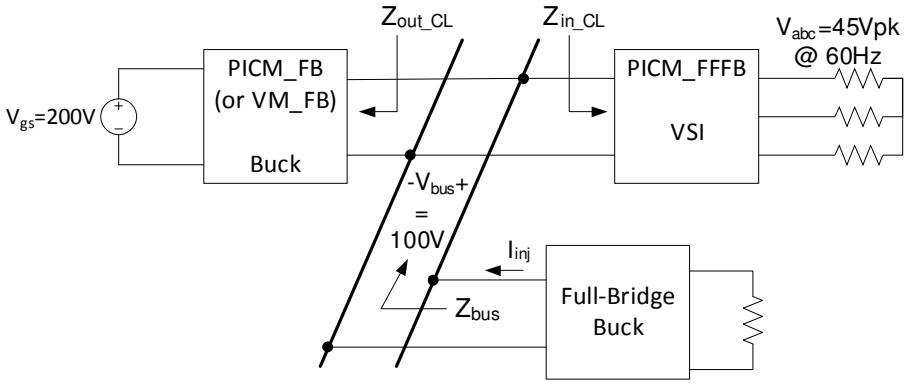
SIMULATION AND EXPERIMENTAL VALIDATION

This chapter provides simulation and experimental verification of the tools presented in Chapter 2 and 3, e.g. the practical PBSC and the PFF control. A DC power distribution system, which is chosen to be the same as the one presented in Chapter 2, is simulated in Simulink by using converter switching models. This provides improved accuracy as compared to averaged models. On the other hand, average models are more convenient for analysis and controller design. A system with the same specifications is also built in the laboratory by using custom converters and two different digital control platforms. Frequency domain simulation and experimental results, obtained by using a wideband system identification technique, are compared to the analytic model to verify the accuracy of the practical PBSC in assessing system stability and the effectiveness of PFF control in improving system bus voltage stability. Good matching of both simulation and experimental frequency domain results is obtained.

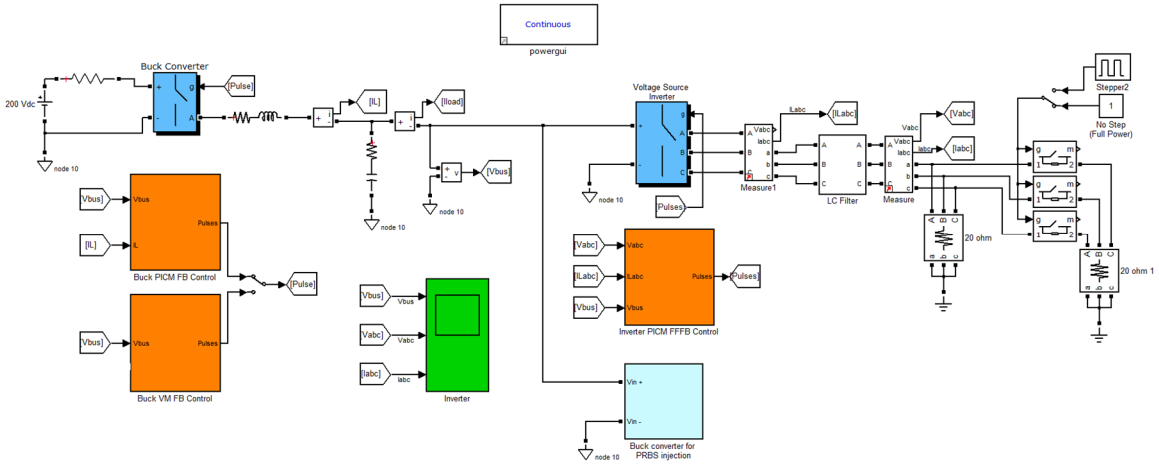
4.1. SIMULATION RESULTS

Fig. 4.1 shows the functional schematic (a) and switching model built in Simulink (b) of the DC power distribution system taken into consideration for stability analysis as well as stability improvement. The system has the same specifications as the averaged model example in Chapter 2, and consists of a cascade of a PICM-FB-controlled or VM_FB-controlled buck converter and a PICM-FFFB-controlled three-phase VSI. The

switching frequency for both the buck converter and the VSI is *20 kHz*. The controller of the VSI has a PFF controller in addition to the conventional FB controller as shown in Fig. 4.2. Figs. 4.3 and 4.4 show the control implementation of the buck converter in CM and VM, respectively. The third converter called "Full-Bridge Buck" in Fig. 4.1(a) is used to measure bus impedance Z_{bus}.



(a)



(b)

Figure 4.1. Functional schematic (a) and switching mode in Simulink (b) of the DC power distribution system under consideration.

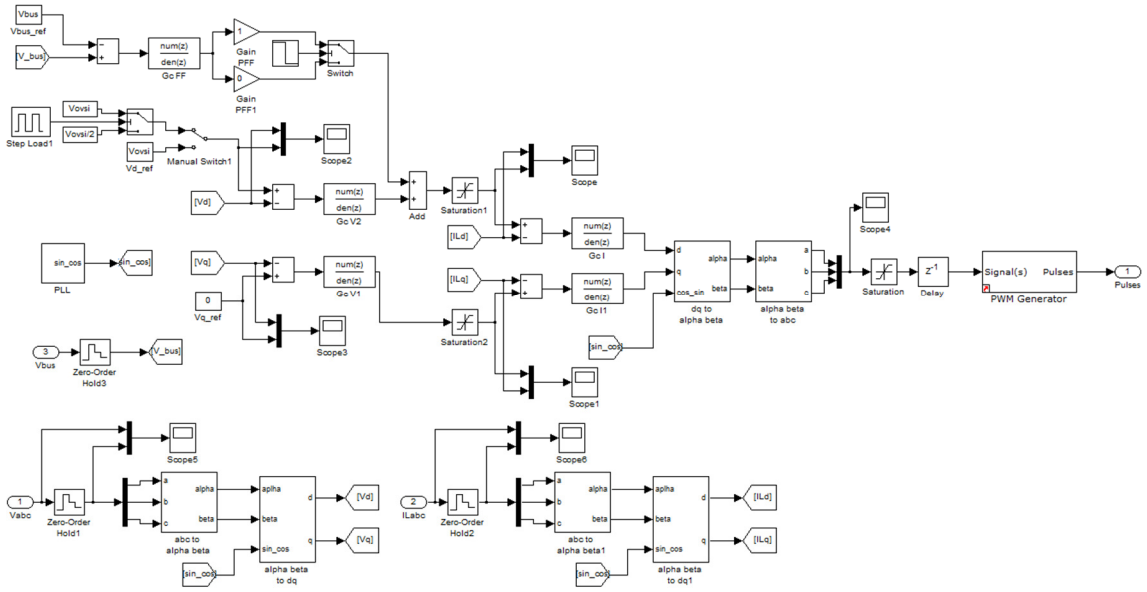


Figure 4.2. Control of the VSI. PICM-FB loop in the middle and FF loop at the top.

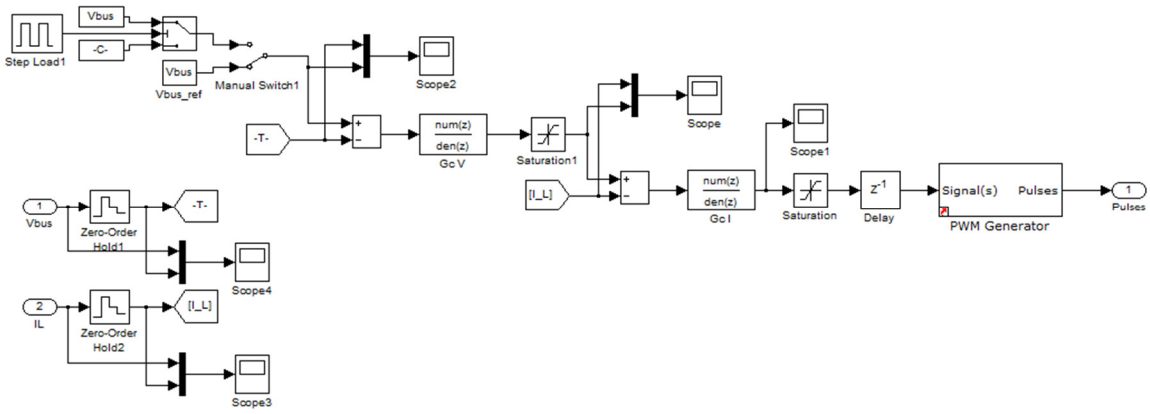


Figure 4.3. Control of the buck converter in CM.

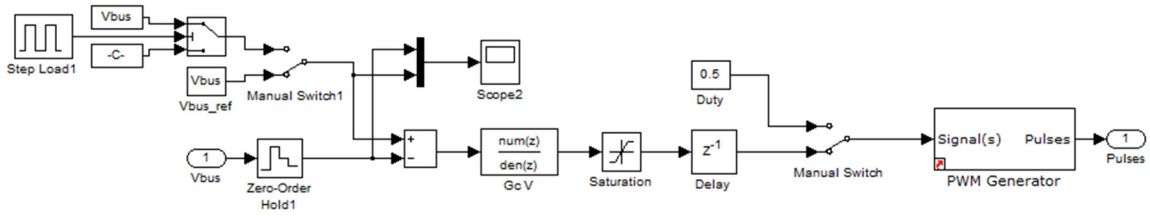


Figure 4.4. Control of the buck converter in VM.

Viewed from the bus port, the entire system in Fig. 4.1 (a) can be lumped into a 1-port network, as Fig. 4.5 shows and as previously described in Chapter 2. The wideband system identification, a particular digital network analyzer technique [70-72], is the tool used to measure the bus impedance and address system level stability issues in the DC power distribution system. This technique uses a switching converter – converter "Full-Bridge Buck" in Fig. 4.1(a) – as a perturbation source and its controller as a signal analyzer to measure small-signal transfer functions and impedances of interest. Referring to Fig. 4.5, a pseudo-random binary sequence (PRBS) test signal – a digital approximation of white noise – is added to the duty cycle signal from the feedback controller. The injected white noise is wideband in nature (it excites a wide range of frequencies at once), and applying the cross-correlation technique to the appropriate measured quantities, it allows online monitoring of the bus impedance $Z_{bus}(s)=V_{bus}(s)/I_{inj}(s)$.

A Full-Bridge buck converter, shown in Fig. 4.6, with $R=10\Omega$, $C=90\mu F$, and $L=1.5mH$ switching at $12\ kHz$ is connected from its input port to the bus of the system. A unipolar modulator is used to effectively double the switching ripple frequency. Initially the PRBS signal is disabled and the system operates under steady-state condition. The identification procedure starts at simulation time $t=0.2s$, when a 10% 14-bit PRBS injection is enabled, and is added to a 50% duty cycle (Fig. 4.6), providing wideband excitation to the system under test (Fig. 4.1). Looking at the bus voltage and the injected current in Fig. 4.7, clearly the additional PRBS does not add a significant amount of noise to the system, since the bus voltage is perturbed by less than 10% from its steady-state value. The Full-Bridge buck converter input current in Fig. 4.7 is negative because the

chosen direction of the sensor named "Current1" allows measuring positive bus impedance. The maximum identifiable frequency is limited to half of the converter sampling rate (Nyquist frequency), i.e. *6 kHz*. Instead, the minimum identifiable frequency is the inverse of the time duration of the PRBS injection [70-72].

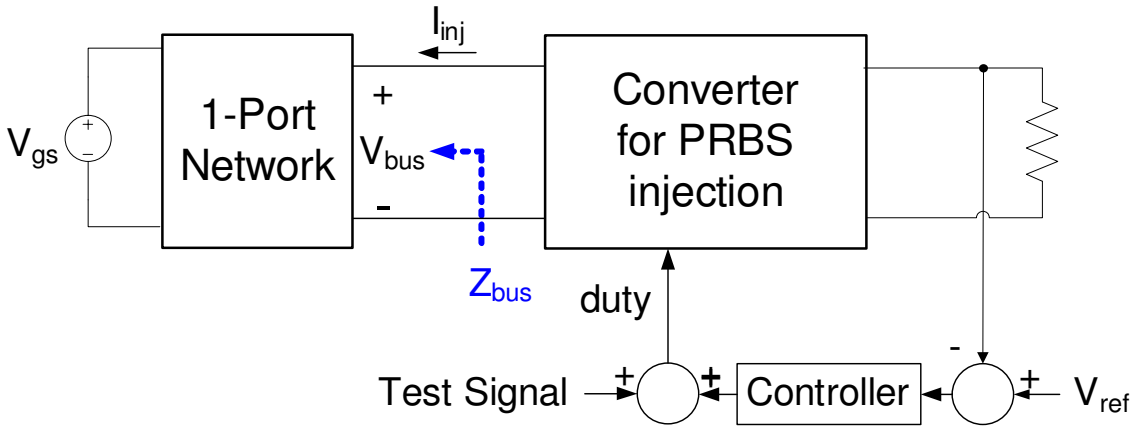


Figure 4.5. Conceptual block diagram showing injection of a test signal for system bus impedance measurements.

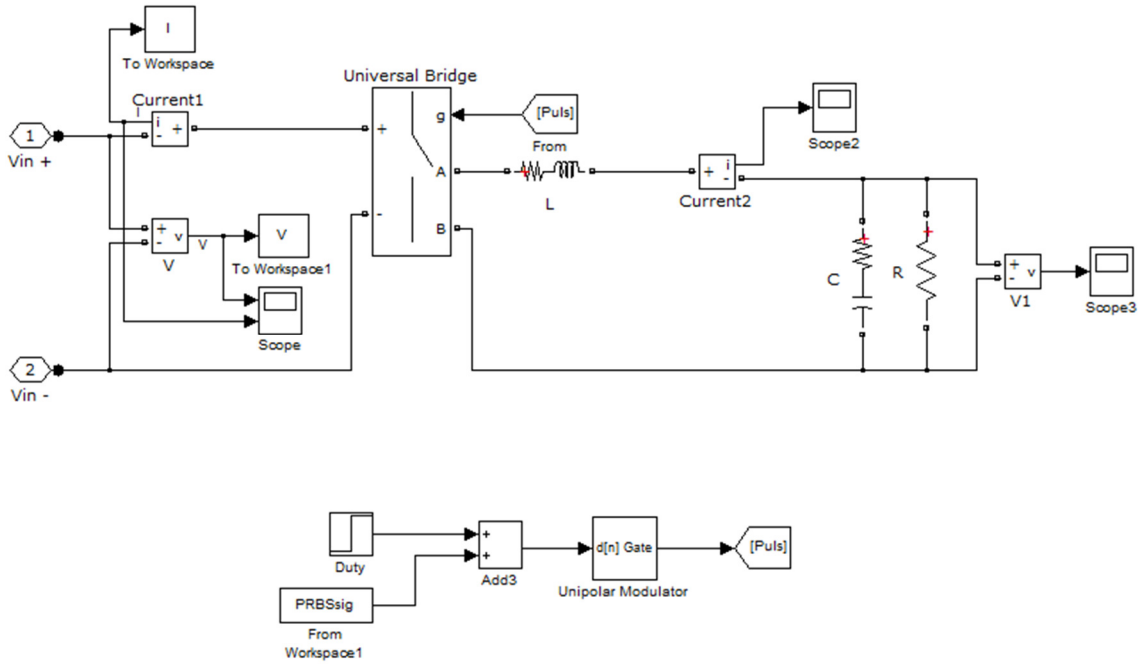


Figure 4.6. Full-Bridge buck converter used for PRBS injection.

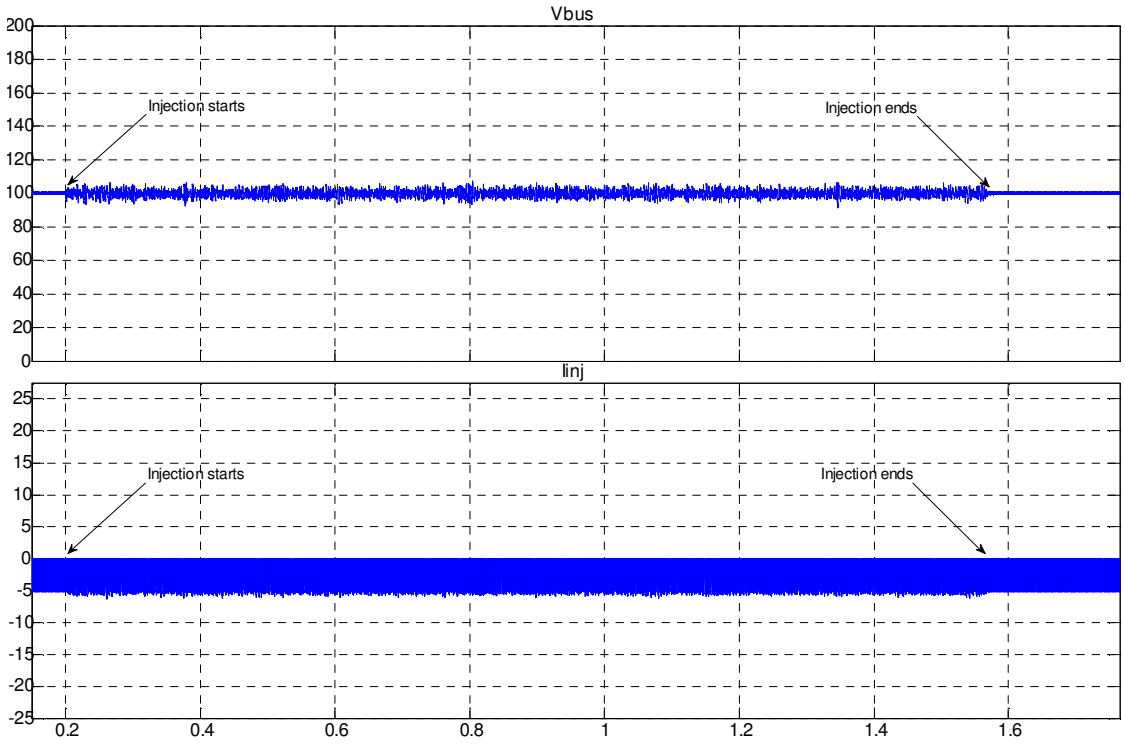


Figure 4.7. Bus voltage and injected current waveforms in correspondence of a PRBS injection.

4.1.1. CASE 1: SIMULATION OF PICM_FB-CONTROLLED BUCK CONVERTER

For the case of a PICM_FB-controlled buck converter in cascade with a PICM_FFFB-controlled VSI, the system with only FB control exhibits some oscillations, while the same system with FFFB control is highly stabilized. The PFF control was designed following the procedure introduced in Chapter 3 to guarantee a desired VSI FB crossover frequency $f_{c\_Zs\_FF}$=*50Hz* (the desired output performance), and to actively introduce the following damping impedance at the VSI input port with the goal of passivating the bus impedance, and therefore stabilizing the system

$$Z_{damp} = R_b + sL_b + \frac{1}{sC_b} \tag{4.1}$$

where $R_b=13.42\Omega$, $L_b=12.40mH$, and $C_b=275.66\mu F$. The PFF controller transfer function is then calculated from (3.23). The obtained VSI FB loop gain $T_{PICM\_FB\_Zs\_FF}$ is shown in Fig. 4.8 which compares the VSI FB loop gains for standalone, addition of source impedance, and addition of PFF control. Fig. 4.9 shows the Bode plot of the bus impedance, which is the parallel combination of the output impedance of the buck converter and the input impedance of the VSI. The analytic transfer functions, given in (4.2), are compared with the nonparametric results given by the digital network analyzer in simulation.

$$Z_{bus\_CL} = \left(\frac{1}{Z_{out\_FB(Buck)}} + \frac{1}{Z_{in\_CL(VSI)}} \right)^{-1} \tag{4.2}$$

CL denotes either FB or FFFB.

As shown in Fig. 4.9, in the FFFB case the bus impedance well satisfies the passivity condition at the resonant frequency, because $arg[Z_{bus\_FFFB}(j\omega_{res})]\approx 0°$, while in the FB only case the passivity condition is only weakly met, because $arg[Z_{bus\_FB}(j\omega_{res})]\approx \pm 90°$ due to the abrupt phase change at the resonant frequency. At the same time the resonant peak is reduced in magnitude because at the resonant frequency Z_{damp} is designed to dominate the bus impedance. Notice that for both FB only and FFFB cases the bus impedance satisfies the passivity condition, i.e. $-90° \le arg[Z_{bus}(j\omega)] \le 90°$, $\forall \omega$. Figs. 4.10 and 4.11 depict the transient responses of the bus voltage and three-phase output voltage in correspondence of VSI voltage reference step, starting from a steady-state condition. Notice the presence of lightly damped oscillations for the FB case only, and the stabilization of the bus voltage for the FFFB case.

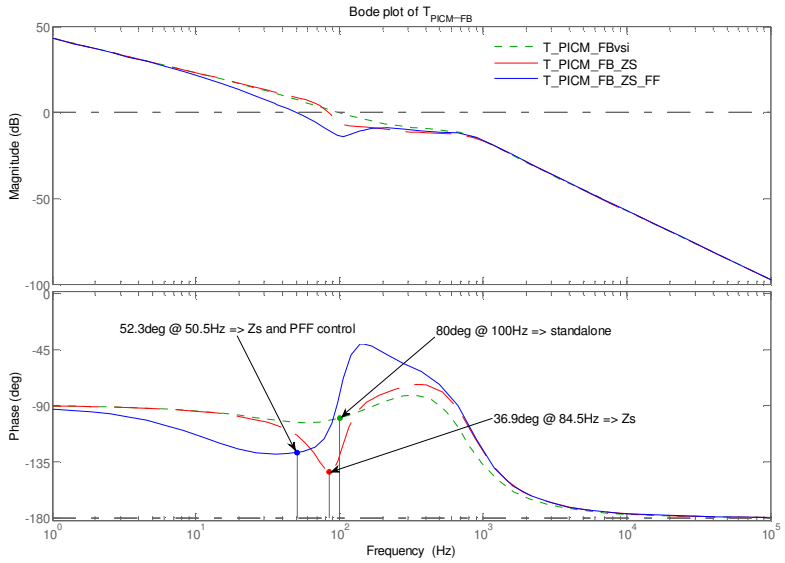


Figure 4.8. Bode plot of the VSI FB loop gain for standalone, addition of source impedance, and addition of PFF control for the cascade of PICM_FB-controlled buck converter and PICM_FB-controlled VSI.

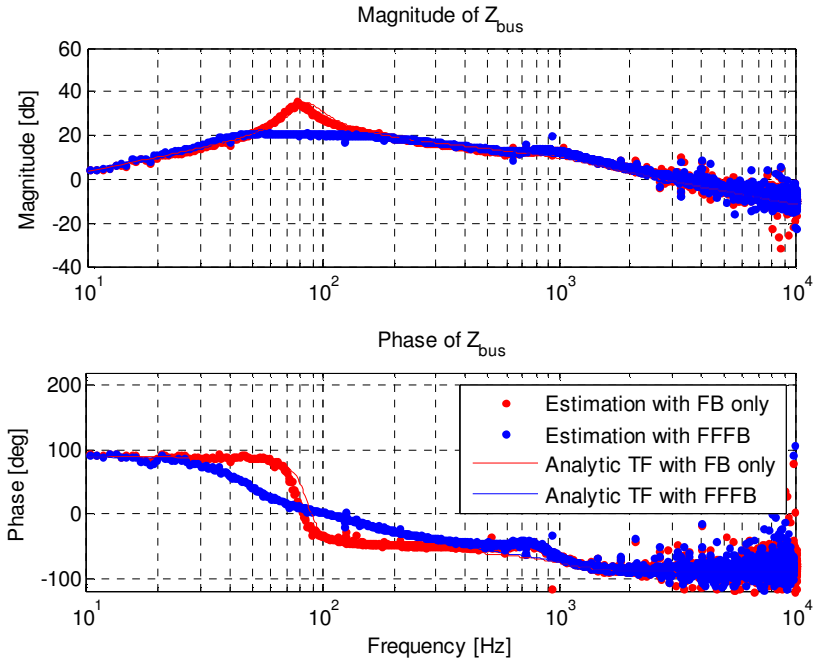


Figure 4.9. Z_{bus} estimation through PRBS injection and comparison with analytic transfer functions for the cascade of PICM_FB-controlled buck converter and PICM_FB-controlled VSI.

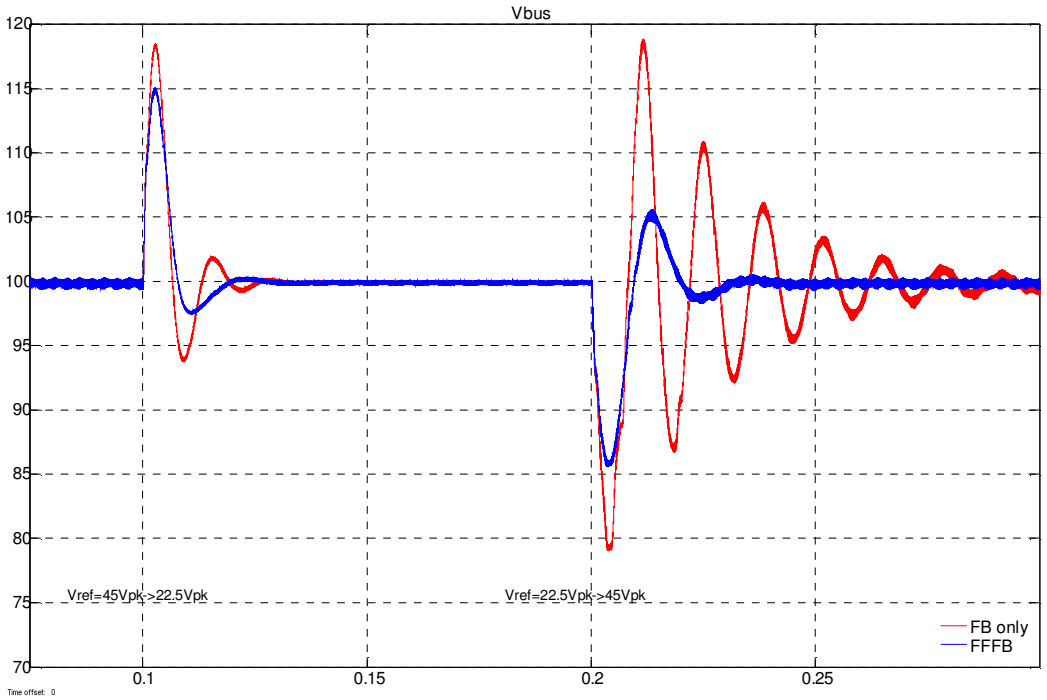


Figure 4.10. Time-domain V_{bus} transient for the cascade of PICM_FB-controlled buck converter and PICM_FB-controlled VSI. Comparison of FB only and FFFB in correspondence to voltage reference step applied to the VSI.

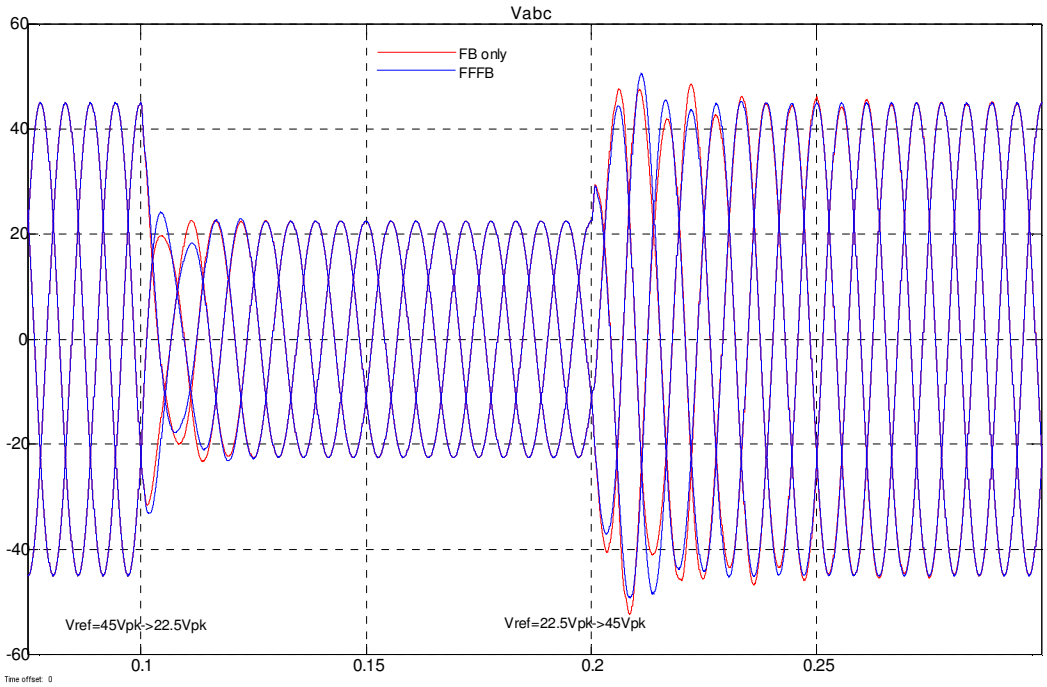


Figure 4.11. Time-domain V_{abc} transient for the cascade of PICM_FB-controlled buck converter and PICM_FB-controlled VSI. Comparison of FB only and FFFB in correspondence to voltage reference step applied to the VSI.

4.1.2. CASE 2: SIMULATION OF VM_FB-CONTROLLED BUCK CONVERTER

Also for the case of a VM_FB-controlled buck converter in cascade with a PICM_FFFB-controlled VSI, the system with FFFB control is highly stabilized with respect to the FB only control. As in the prior case, the PFF control was designed following the procedure introduced in Chapter 3 to guarantee a desired VSI FB crossover frequency $f_{c\_Zs\_FF}=100Hz$ (the desired output performance), and to actively introduce the same R_b-L_b-C_b damping impedance as in (4.1) at the VSI input port with the goal of passivating the bus impedance, and therefore stabilizing the system. The parameters of the damping impedance are calculated to be $R_b=23.56\Omega$, $L_b=5.23mH$, and $C_b=37.71\mu F$. The resulting PFF controller transfer function is then calculated from (3.23). The obtained VSI FB loop gain $T_{PICM\_FB\_Zs\_FF}$ is shown in Fig. 4.12 which compares the VSI FB loop gains for standalone, addition of source impedance, and addition of PFF control. It can be noticed that for this case the additions of Z_S and then the PFF control do not significantly change the shape of $T_{PICM\_FB\_Zs\_FF}$. Fig. 4.13 shows the Bode plot of the nonparametric bus impedance compared with the counterpart analytic transfer functions. As shown in Fig. 4.13, in the FFFB case the bus impedance well satisfies the passivity condition at the resonant frequency, because $arg[Z_{bus\_FFFB}(j\omega_{res})]\approx 0°$, while in the FB only case the passivity condition is only weakly met, because $arg[Z_{bus\_FB}(j\omega_{res})]\approx \pm 90°$ due to the abrupt phase change at the resonant frequency. At the same time the resonant peak is reduced in magnitude because at the resonant frequency Z_{damp} is designed to dominate the bus impedance. Notice that for both cases the bus impedance does not satisfy the passivity condition at low frequencies, which is not important for stability assessment as proved in Chapter 2. Figs. 4.14 and 4.15 depict the transient responses of

the bus voltage and three-phase output voltage in correspondence of VSI voltage reference step, starting from a steady-state condition. Notice the presence of sustained oscillations for the FB case only, and the stabilization of the bus voltage for the FFFB case. Moreover, the three-phase output voltage transient is almost the same for both the FB only case and the FFFB case. This is due to the fact that the addition of Z_S and the PFF control does not significantly alter the VSI loop gain $T_{PICM\_FB\_Zs\_FF}$.

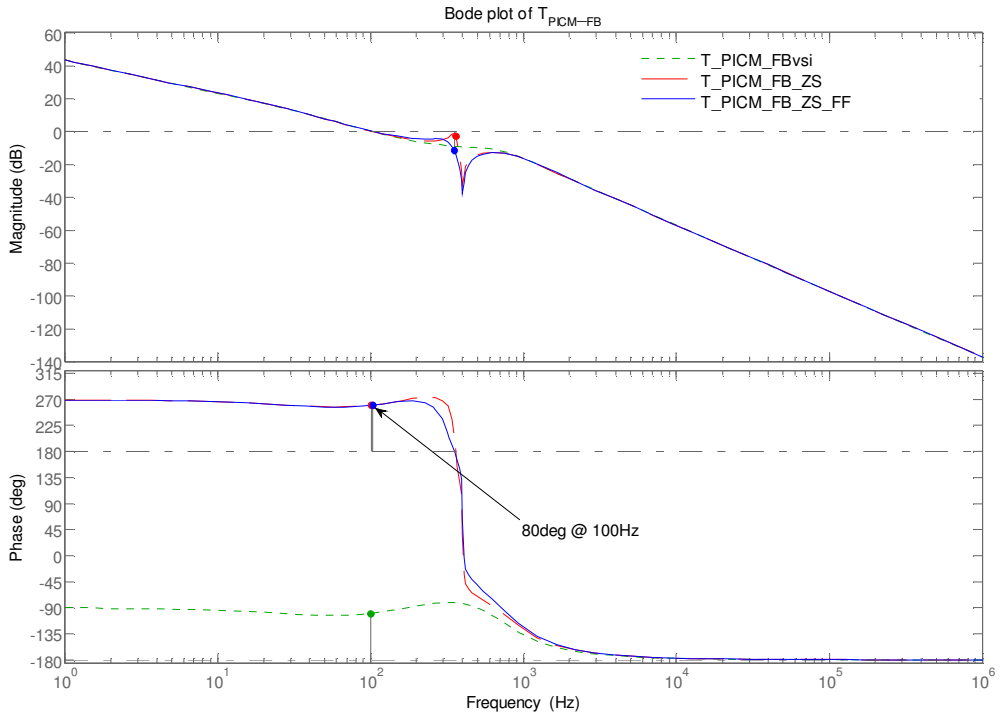


Figure 4.12. Bode plot of the VSI FB loop gain for standalone, addition of source impedance, and addition of PFF control for the cascade of VM_FB-controlled buck converter and PICM_FB-controlled VSI.

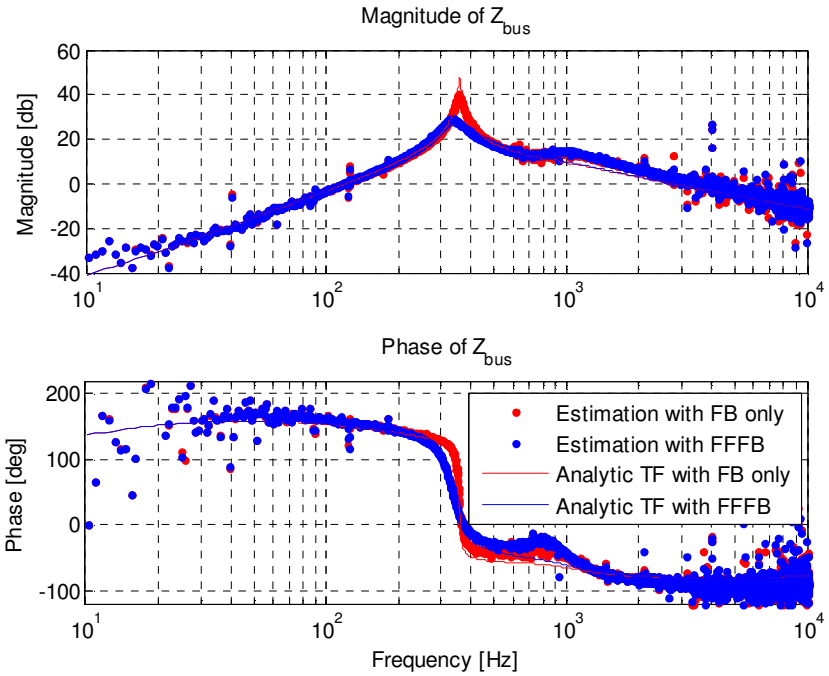


Figure 4.13. Z_{bus} estimation through PRBS injection and comparison with analytic transfer functions for the cascade of VM_FB-controlled buck converter and PICM_FB-controlled VSI.

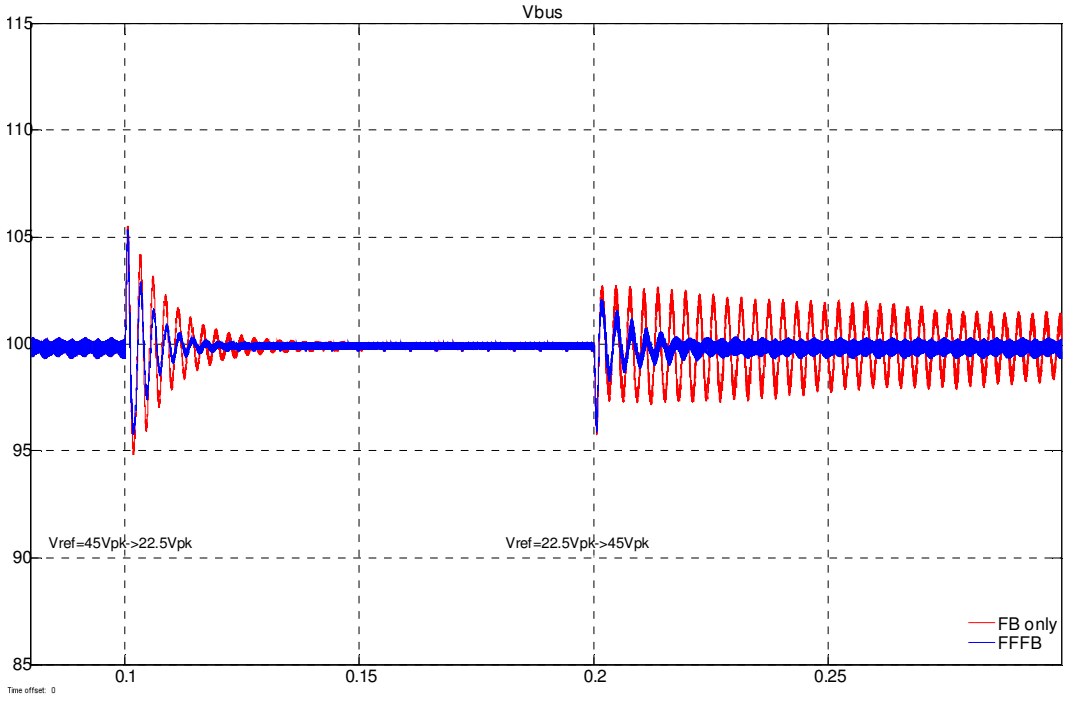


Figure 4.14. Time-domain V_{bus} transient for the cascade of VM_FB-controlled buck converter and PICM_FB-controlled VSI. Comparison of FB only and FFFB in correspondence to voltage reference step applied to the VSI.

Figure 4.14.

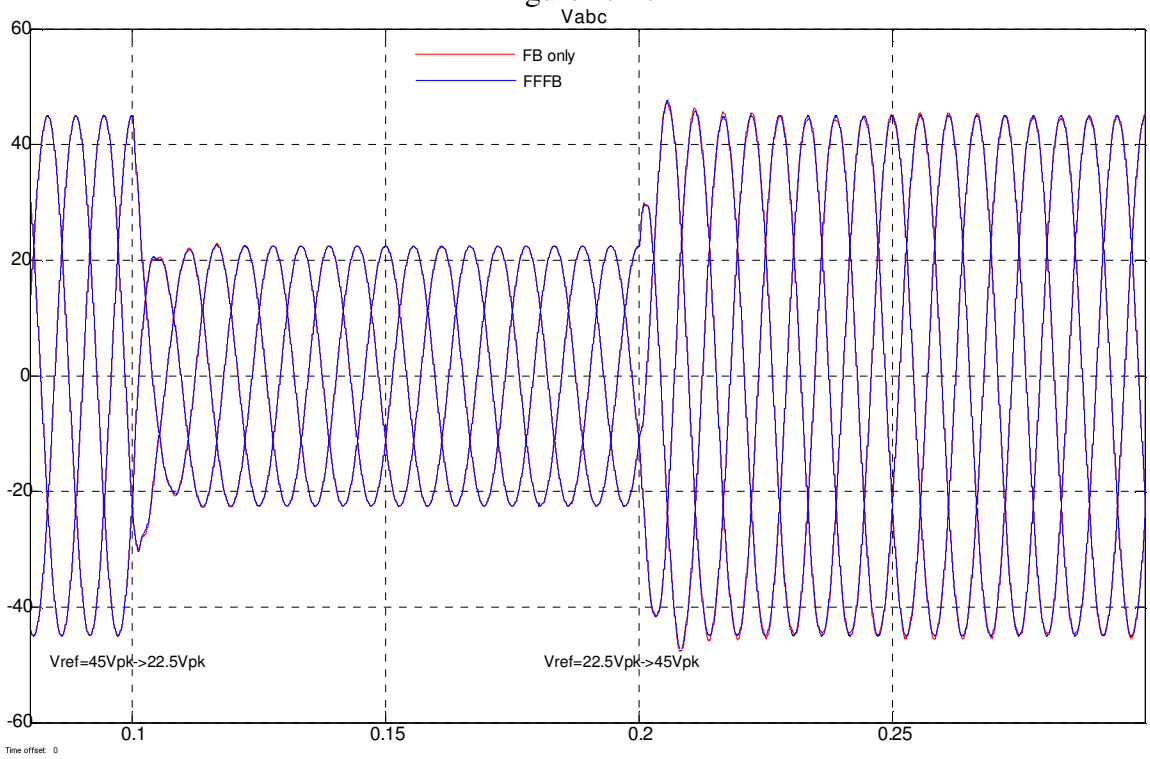


Figure 4.15. Time-domain V_{abc} transient for the cascade of VM_FB-controlled buck converter and PICM_FB-controlled VSI. Comparison of FB only and FFFB in correspondence to voltage reference step applied to the VSI.

4.2. EXPERIMENTAL RESULTS

For the experimental validation, the same DC power distribution system in Fig. 4.1 is used. A picture of the laboratory setup is shown in Fig. 4.16. Appendix D provides schematics and more technical details concerning the DC power distribution system hardware setup built in the laboratory.

The digital control of the buck converter and that of the VSI are implemented using dSPACE DS1104 system [73], i.e. a DSP based control platform especially designed for rapid control prototyping of high-speed multivariable systems. The DS1104 processor board contains a 64-bit PowerPC 603e floating-point processor running at

250MHz and a slave-DSP system based on a TMS320F240 DSP microcontroller, providing a complete real-time control package.

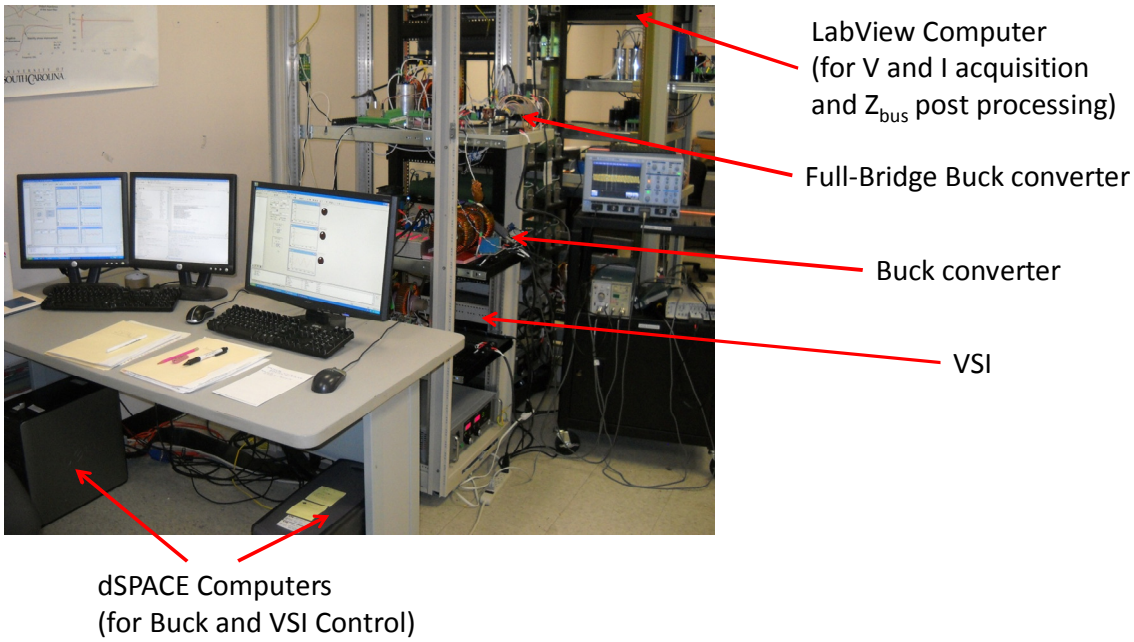


Figure 4.16. A picture of the DC power distribution system built in the laboratory.

The Real-Time Interface [74] (RTI) for dSPACE systems links Simulink models to the DS1104 hardware. RTI generates and compiles real-time code that runs on the dSPACE hardware. The RTI augments the standard Simulink library with a custom blockset that gives the user access to I/O ports, slave-PWM support, and various other event handling and timing systems on the DS1104 controller. The digital controller for the VSI is implemented as reported in Fig. 4.17. It is easy to recognize both the PICM_FB (in the middle) and the PFF (at the top) loops. The digital controller for the buck converter in CM and VM are implemented as shown in Figs. 4.18 and 4.19, respectively. With respect to the Simulink simulations in Figs. 4.2 to 4.4, the Simulink implementation of controllers in Figs. 4.17 to 4.19 uses dSPACE ADC blocks and PWM

block at the controller interfaces to connect the digital controller to the real plant. Moreover, a PWM-Interrupt block connected to a Timer Task Assignment block has to be present so that an interrupt from the slave-DSP PWM triggers the ADC sampling. By doing so, the ADC sampling can be synchronized to occur at in the middle of the PWM low pulse to reduce significant acquisition errors due to the switching. The block at the right bottom of Figs. 4.17 to 4.19 implements overvoltage and over current protections (Fig. 4.20) that turns both the buck converter and the VSI off during unstable operations. The digital PICM_FB and VM_FB controller for the buck converter and the digital PICM_FFFB controller for the VSI are designed as explained in the previous section. The dSPACE hardware is user configurable via the dSPACE ControlDesk environment [75], shown in Fig. 4.21 for the PICM_FFFB control of the VSI and in Fig. 4.22 for the PICM_FB control of the buck converter.

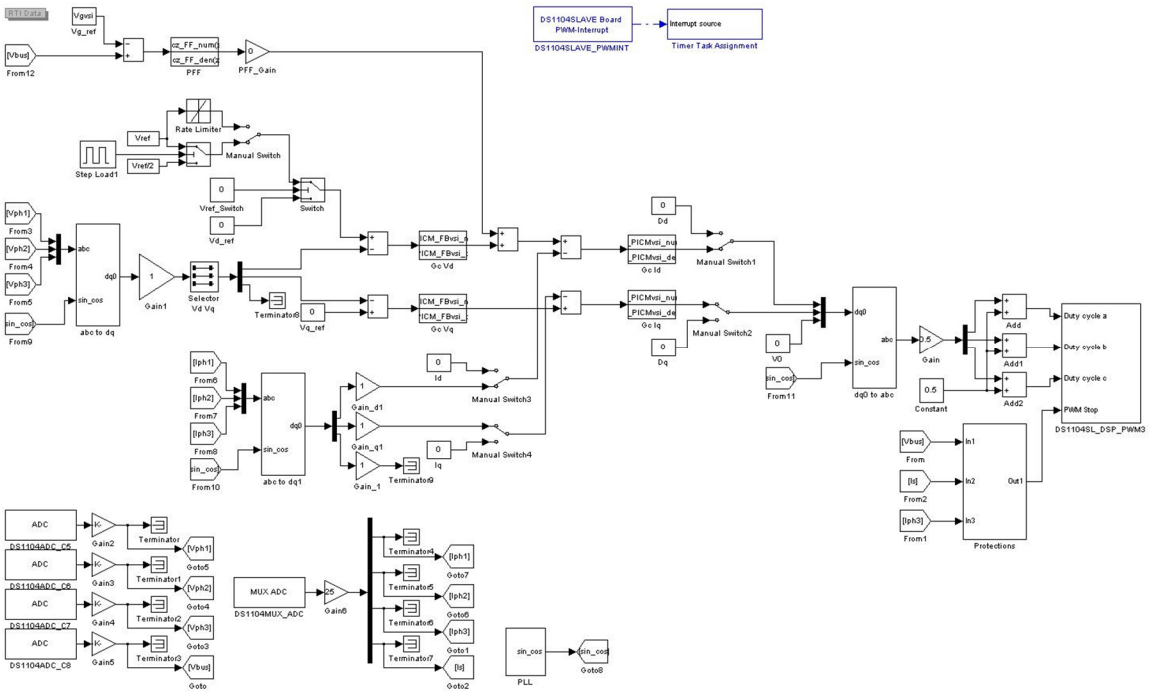


Figure 4.17. Simulink implementation of the VSI PICM_FFFB control by using dSPACE blockset.

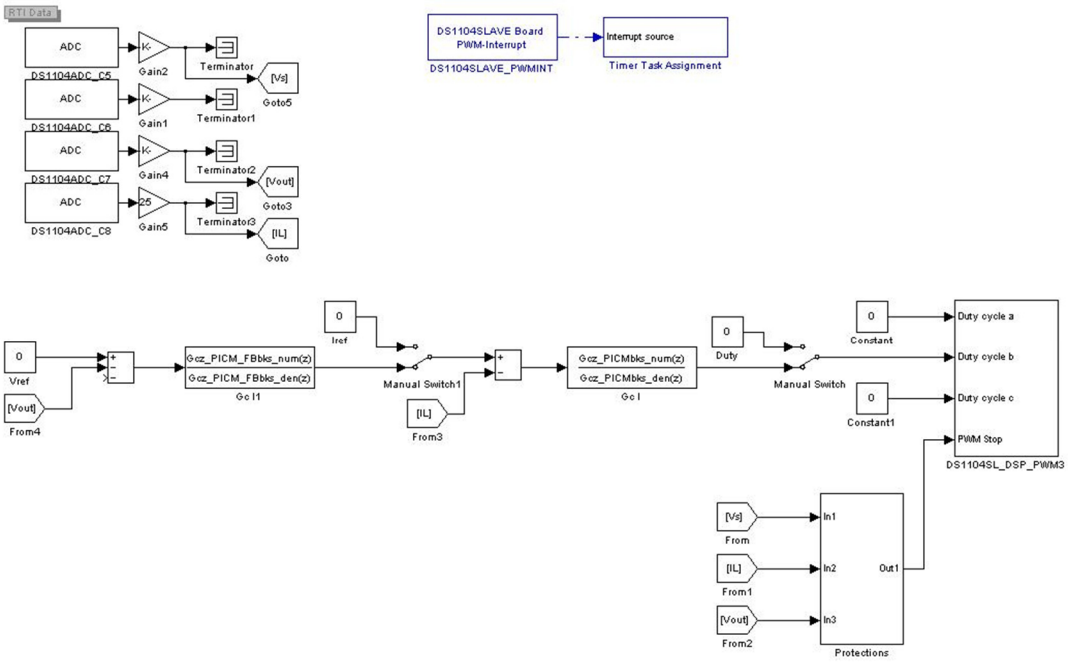


Figure 4.18. Simulink implementation of the buck converter PICM_FB control by using dSPACE blockset.

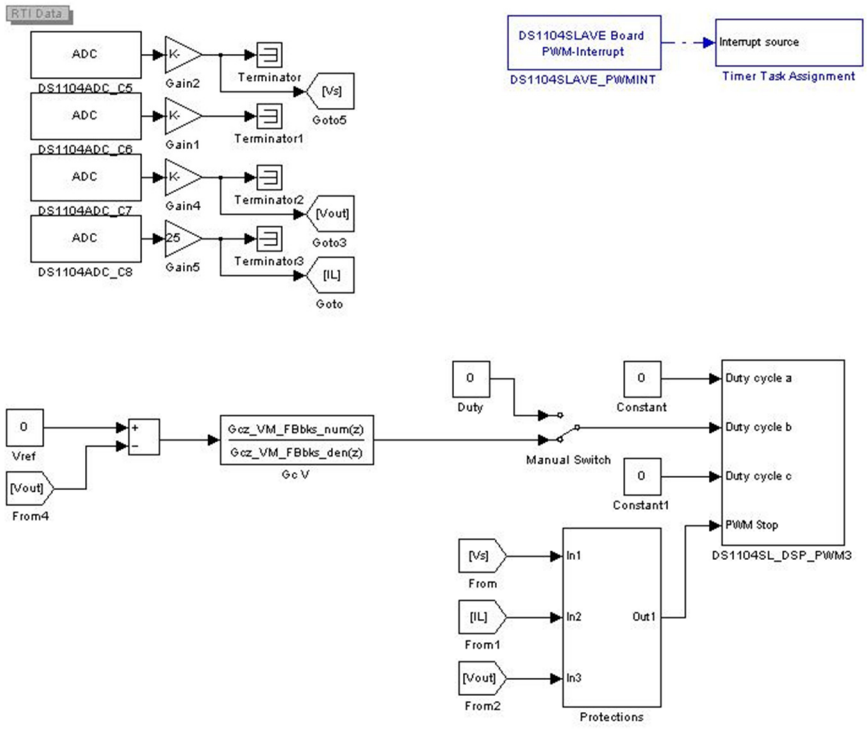


Figure 4.19. Simulink implementation of the buck converter VM_FB control by using dSPACE blockset.

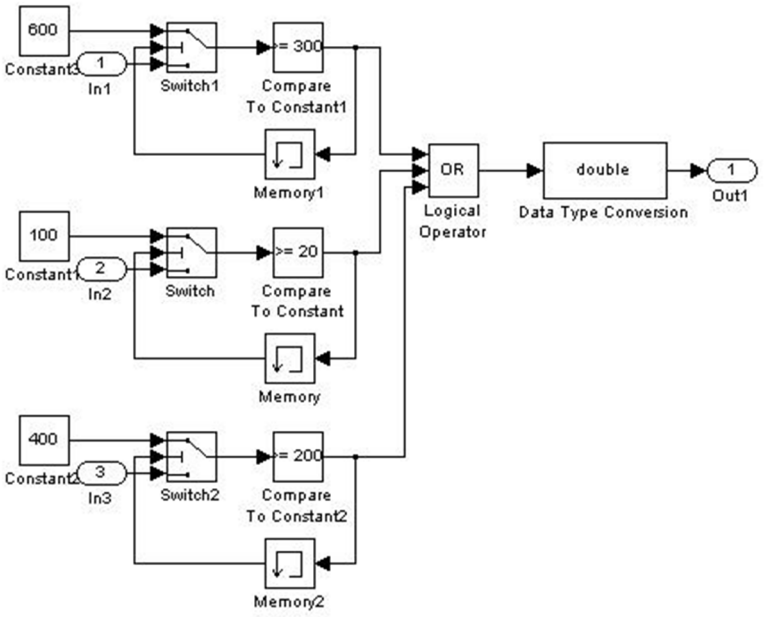


Figure 4.20. Simulink implementation of the over-current and over-voltage protections.

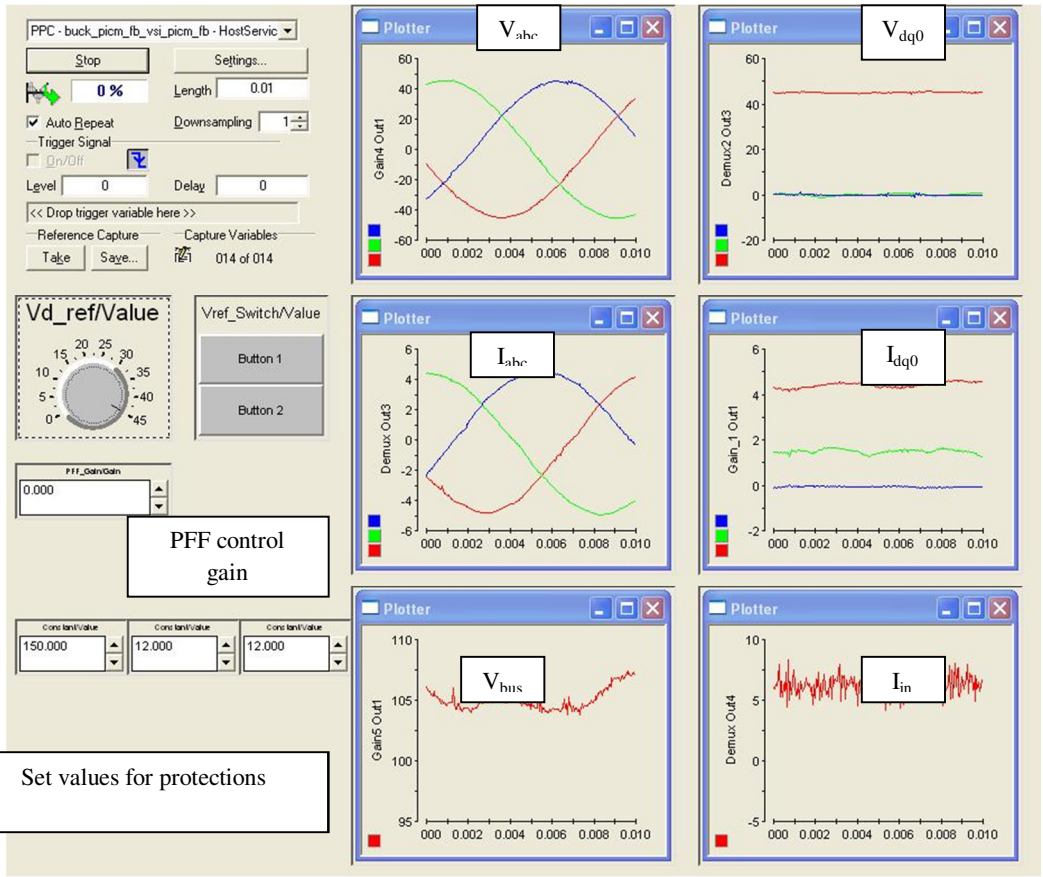


Figure 4.21. ControlDesk interface screenshot for the VSI controller.

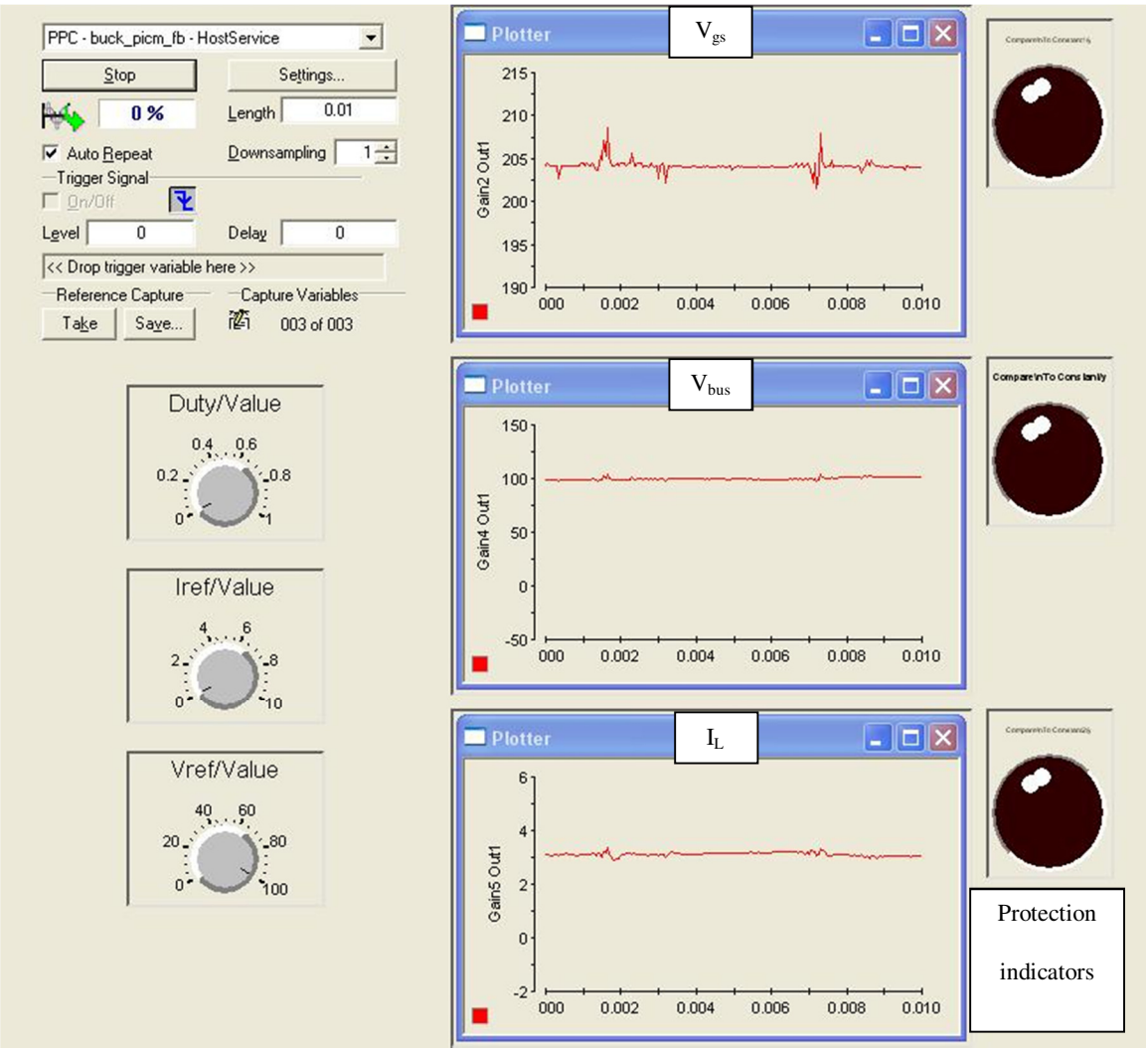


Figure 4.22. ControlDesk interface screenshot for the buck converter controller.

The microcontroller used for the full-bridge buck converter control is a Texas Instruments TMS320F28335 floating point DSP control card, which is inserted into a custom built sensing board (see Appendix D for details). The full-bridge buck converter is used to create a perturbation for bus impedance estimation. A 14-Bit PRBS (16,383 terms) is generated, and fed into the duty cycle reference as a 10% perturbation. Since the microcontroller control card doesn't have space for external memory, a separate National Instruments data acquisition unit (NI-6259 DAQ) with 16-Bit ADCs is used for data

acquisition and calculation of system impedance. In particular, the system bus impedance identification is carried out by capturing the output current of the full-bridge buck converter and bus voltage, and post processing was carried out in LabView. Figs. 4.23 and 4.24 show the NI VI block diagram and front panel for voltage and current acquisition as well as for nonparametric bus impedance post processing. As last step of the description of the experiment, least squares fitting [64, 71-72] is applied to the nonparametric model, and the parametric transfer function is extracted and compared to the analytic transfer function.

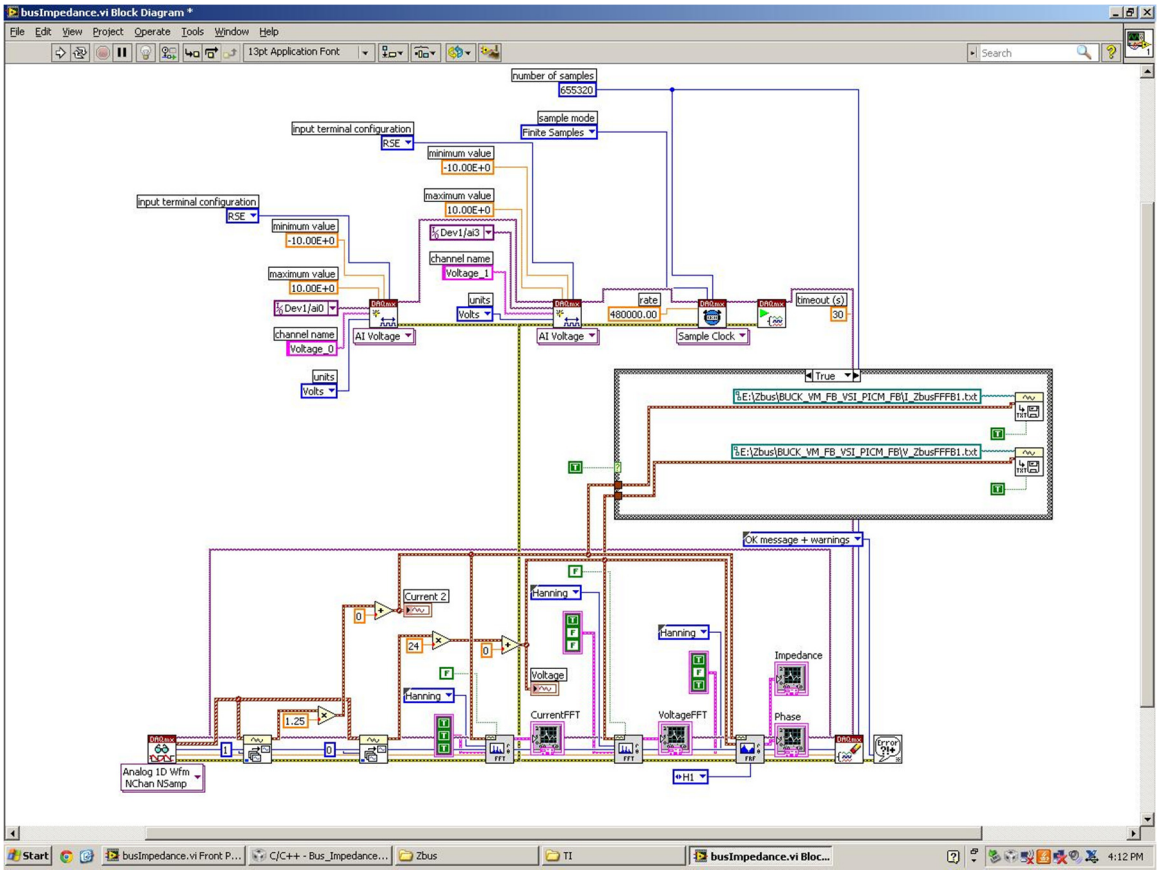


Figure 4.23. NI VI block diagram for voltage and current acquisition as well as bus impedance post processing.

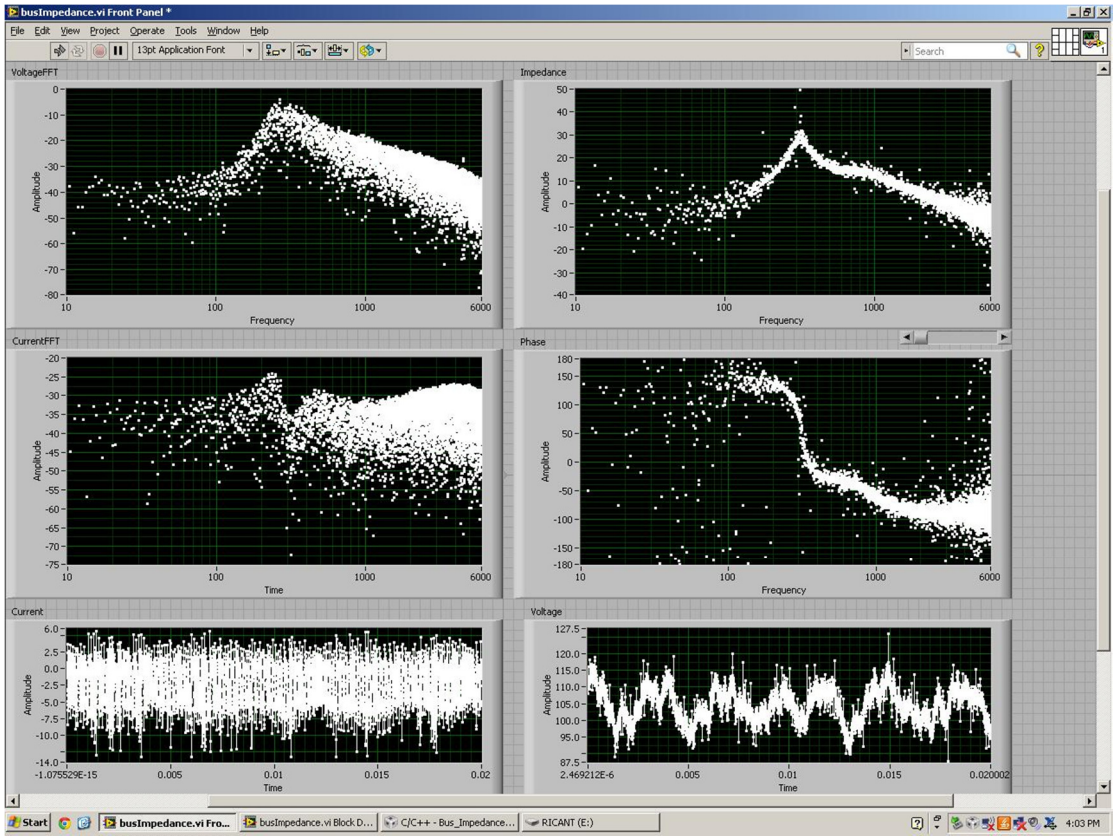


Figure 4.24. NI VI front panel for voltage and current acquisition as well as bus impedance post processing.

For the frequency domain experimental results, four sets of controller configurations are used:

- Set 1 (Figs. 4.25-4.29): cascade of
  - PICM_FB-controlled (f_{c_PICM}=*1 kHz*, $PM_{\_PICM}$=80°; $f_{c\_PICM\_FB}$=*100 Hz*, $PM_{\_PICM\_FB}$=70°) buck converter, and
  - PICM_FB-controlled (f_{c_PICM}=*1 kHz*, $PM_{\_PICM}$=80°; $f_{c\_PICM\_FB}$=*1 kHz*, $PM_{\_PICM\_FB}$=80°) VSI.
- Set 2 (Figs. 4.30-4.34): cascade of
  - PICM_FB-controlled (f_{c_PICM}=*1 kHz*, $PM_{\_PICM}$=80°; $f_{c\_PICM\_FB}$=*100 Hz*, $PM_{\_PICM\_FB}$=70°) buck converter, and

- PICM_FFFB-controlled (f_{c_PICM}=*1 kHz*, $PM_{\_PICM}$=80°*; PFF control designed so that* L_b-R_b-C_b *active damping is introduced and* $f_{c\_PICM\_FB\_Zs\_FF}$=*50 Hz*) VSI.

- Set 3 (Figs. 4.35-4.39): cascade of
  - VM_FB-controlled ($f_{c\_VM\_FB}$=*300 Hz*, $PM_{\_VM\_FB}$=52°) buck converter, and
  - PICM_FB-controlled (f_{c_PICM}=*1 kHz*, $PM_{\_PICM}$=80°*;* $f_{c\_PICM\_FB}$=*1 kHz*, $PM_{\_PICM\_FB}$=80°) VSI.
- Set 4 (Figs. 4.40-4.44): cascade of
  - VM_FB-controlled ($f_{c\_VM\_FB}$=*300 Hz*, $PM_{\_VM\_FB}$=52°) buck converter, and
  - PICM_FFFB-controlled (f_{c_PICM}=*1 kHz*, $PM_{\_PICM}$=80°*; PFF control designed so that* L_b-R_b-C_b *active damping is introduced and* $f_{c\_PICM\_FB\_Zs\_FF}$=*100 Hz*) VSI.

In these sets of measurements, first the nonparametric bus impedance (raw data from bus voltage and injection current acquisition and post processing via NI DAQ) is compared with the analytic transfer function. As shown in Figs. 4.25, 4.30, 4.35, and 4.40 a good matching is obtained. Then, to enforce equal fitting priority across the Bode plots of the nonparametric data, a thinning technique is used to obtain a logarithmically spaced subset of the data points as seen in the red crosses of Figs. 4.26, 4.31, 4.36, and 4.41. This method dramatically reduces the computational time of the numerical fitting algorithm, since the number of data points is reduced. However, care must be taken in choosing a large enough number of data points to capture the sharpest features (highest Q) for the expected worst case scenario (FB control only). The fit from the thinned data points is shown in Figs. 4.27, 4.32, 4.37, and 4.42, where, again, good matching is obtained. Figs.

4.28, 4.33, 4.38, and 4.43 also show a good matching of the fitted transfer functions, given in (4.3)-(4.6), and the corresponding analytic transfer functions. Finally, Figs. 4.29, 4.34, 4.39, and 4.44 depict the Nyquist plots of the fitted transfer functions, demonstrating the validity of the practical PBSC.

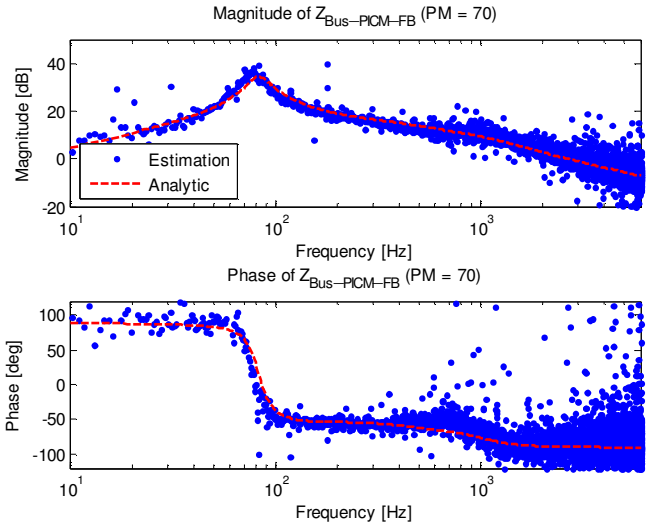


Figure 4.25. Bode plot of the bus impedance nonparametric estimation and analytic transfer function for set 1.

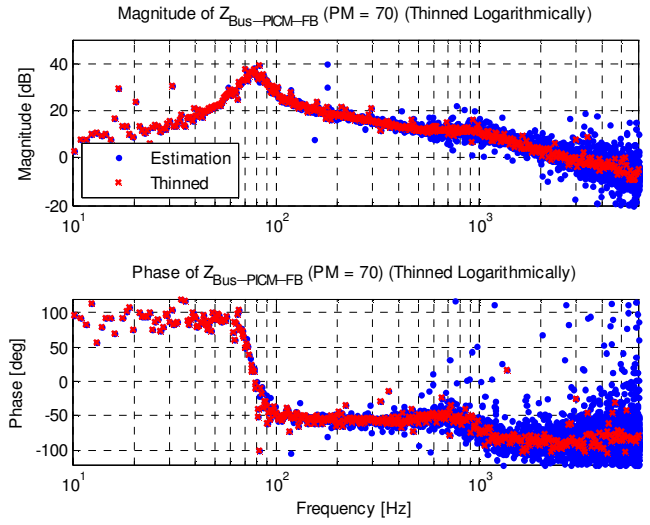


Figure 4.26. Bode plot of the bus impedance nonparametric estimation data (blue dots) and logarithmically thinned subset (red crosses) for set 1.

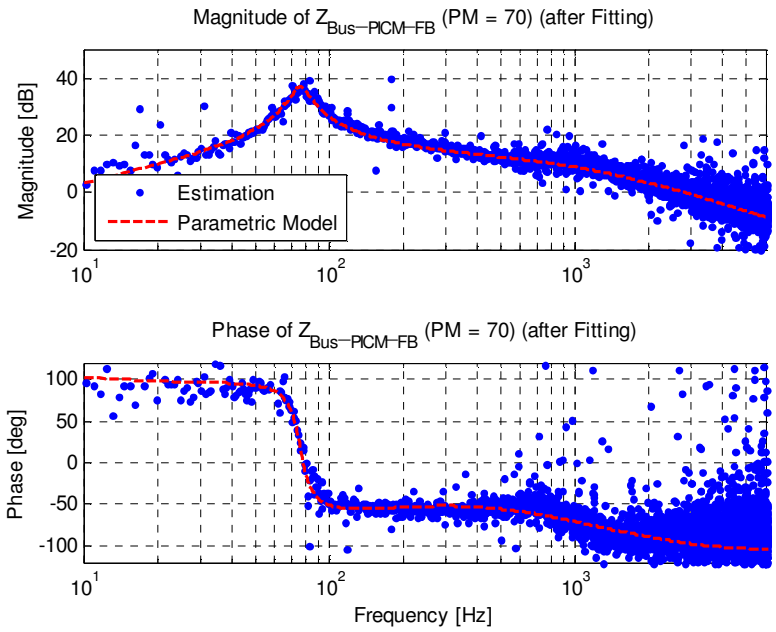


Figure 4.27. Bode plot of the bus impedance nonparametric estimation data (blue dots) and fitted parametric model via logarithmic thinning (red dashed line) for set 1.

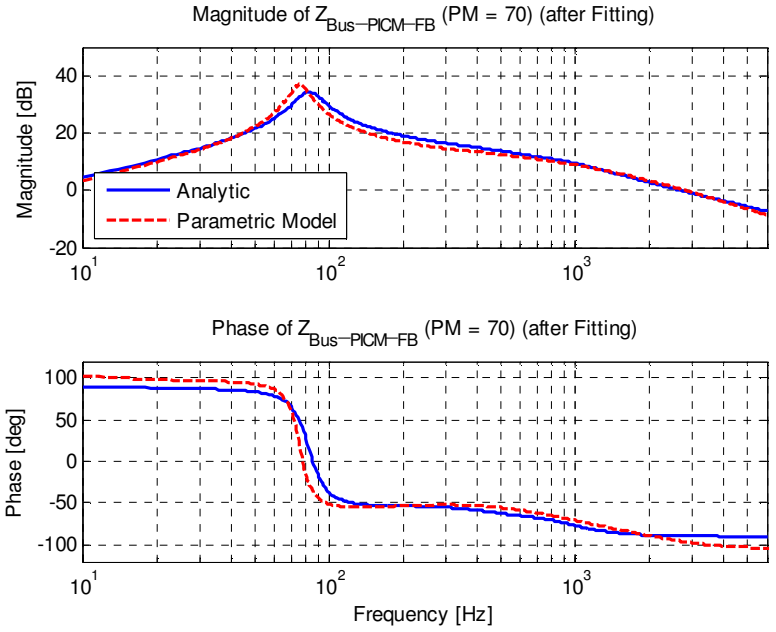


Figure 4.28. Bode plot of the bus impedance analytic transfer function (blue line) and fitted parametric model via logarithmic thinning (red dashed line) for set 1.

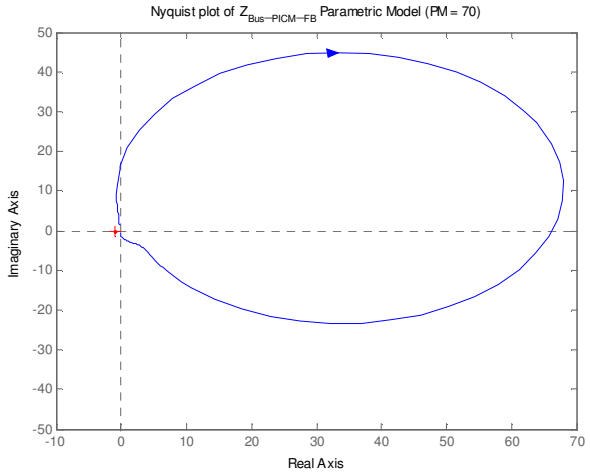


Figure 4.29. Nyquist plot of the bus impedance fitted parametric model via logarithmic thinning for set 1.

The fitted bus impedance for set 1 is:

$$Set\,1:$$

$$Z_{bus\_FB} = \frac{2.134e023\,s^3 + 8.6e027\,s^2 + 9.285e030\,s - 1.218e032}{s^5 + 1.939e019\,s^4 + 4.688e023\,s^3 + 1.852e027\,s^2 + 2.529e029\,s + 4.146e032} \tag{4.3}$$

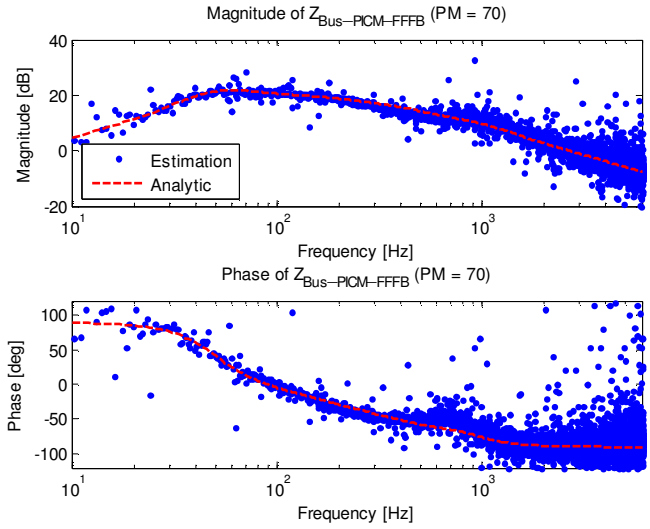


Figure 4.30. Bode plot of the bus impedance nonparametric estimation and analytic transfer function for set 2.

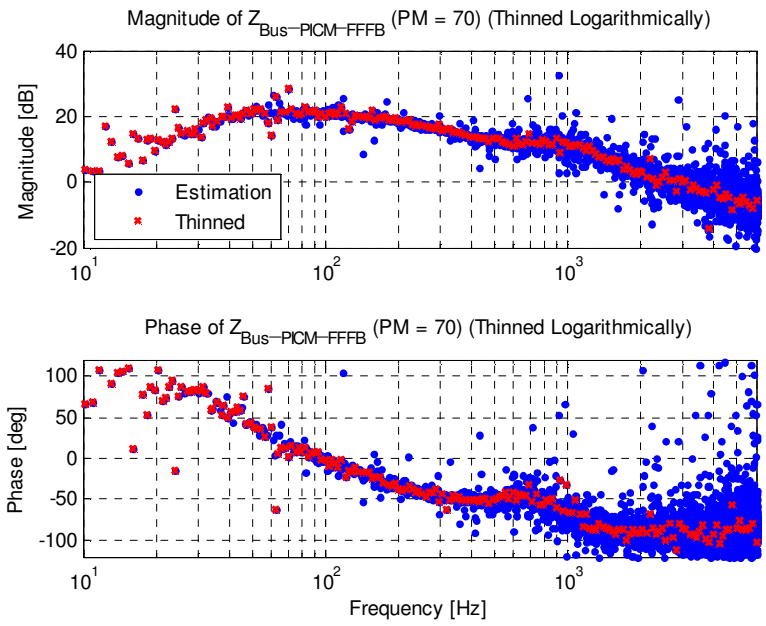


Figure 4.31. Bode plot of the bus impedance nonparametric estimation data (blue dots) and logarithmically thinned subset (red crosses) for set 2.

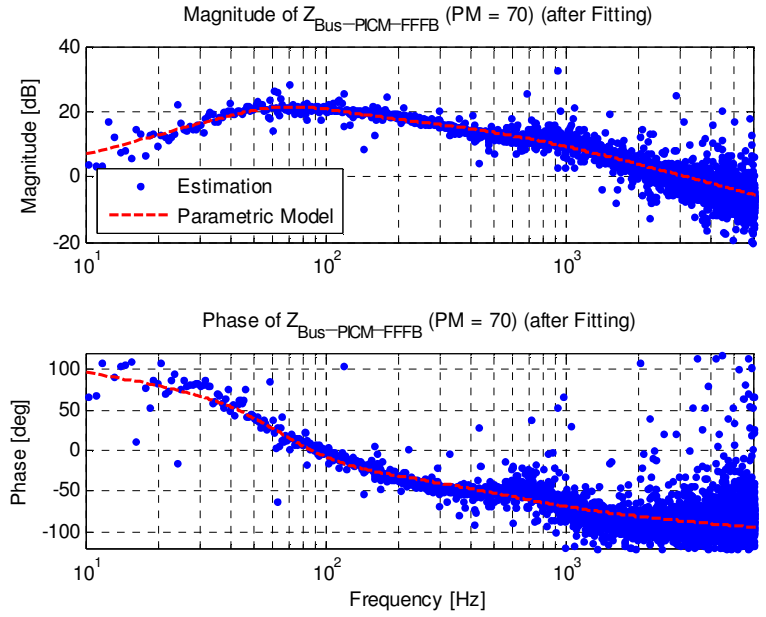


Figure 4.32. Bode plot of the bus impedance nonparametric estimation data (blue dots) and fitted parametric model via logarithmic thinning (red dashed line) for set 2.

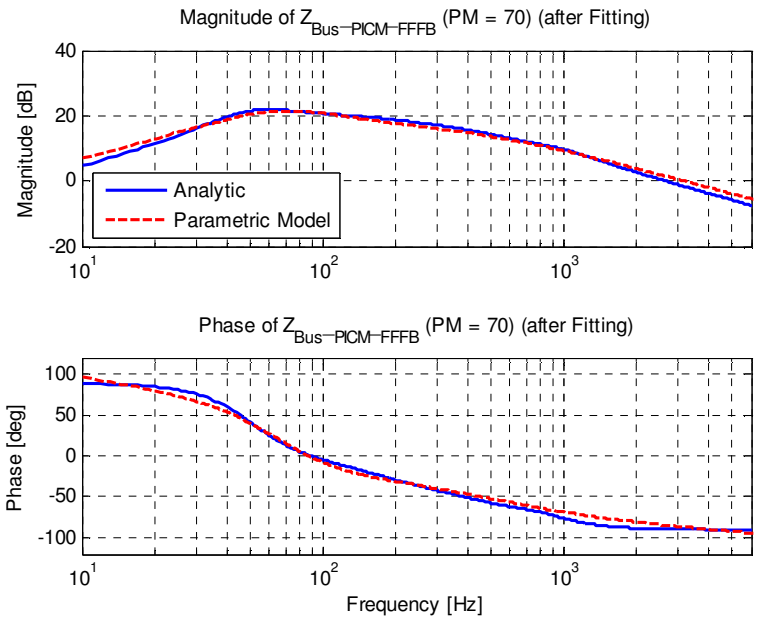


Figure 4.33. Bode plot of the bus impedance analytic transfer function (blue line) and fitted parametric model via logarithmic thinning (red dashed line) for set 2.

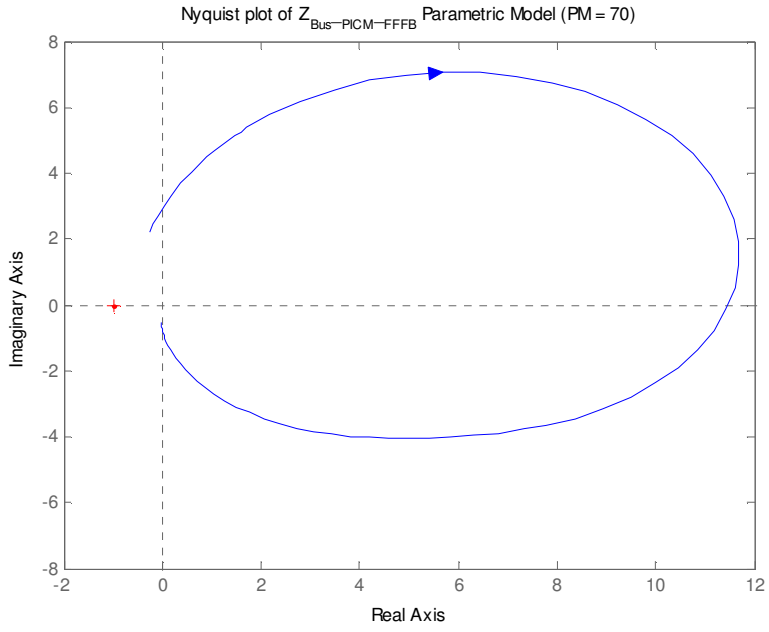


Figure 4.34. Nyquist plot of the bus impedance fitted parametric model via logarithmic thinning for set 2.

The fitted impedance for set 2 is:

$$Set\ 2:$$

$$Z_{bus\_FFFB} = \frac{-4.552e026\,s^3 + 1.141e032\,s^2 + 9.981e034\,s - 1.733e036}{s^5 + 1.794e020\,s^4 + 5.67e027\,s^3 + 2.029e031\,s^2 + 1.043e034\,s + 2.998e036} \tag{4.4}$$

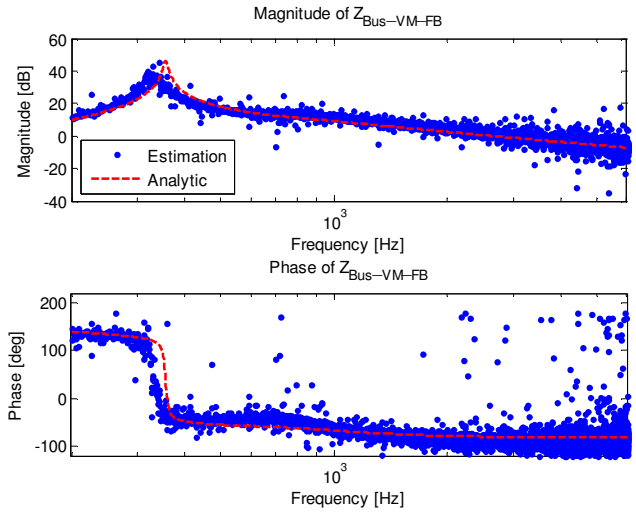


Figure 4.35. Bode plot of the bus impedance nonparametric estimation and analytic transfer function for set 3.

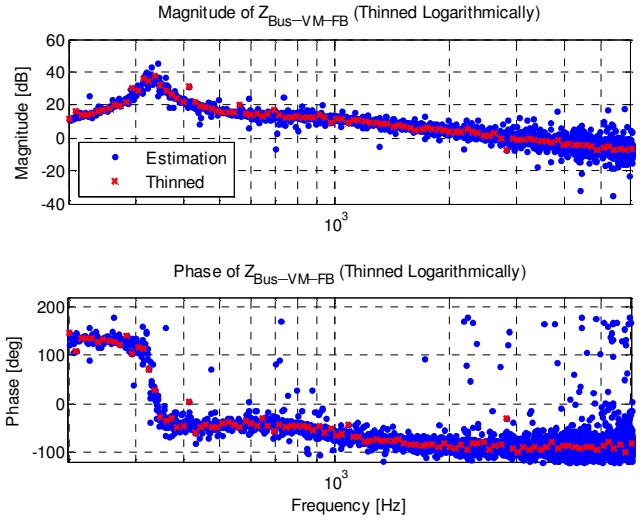


Figure 4.36. Bode plot of the bus impedance nonparametric estimation data (blue dots) and logarithmically thinned subset (red crosses) for set 3.

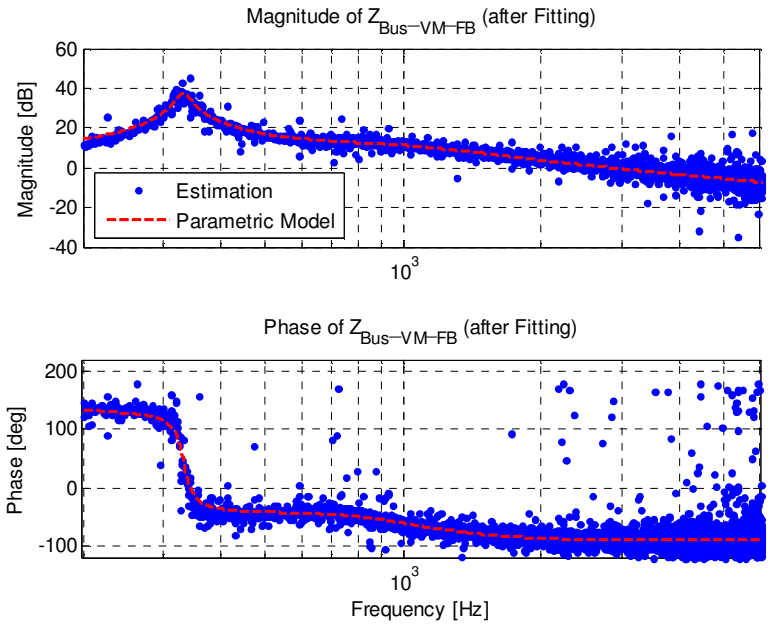


Figure 4.37. Bode plot of the bus impedance nonparametric estimation data (blue dots) and fitted parametric model via logarithmic thinning (red dashed line) for set 3.

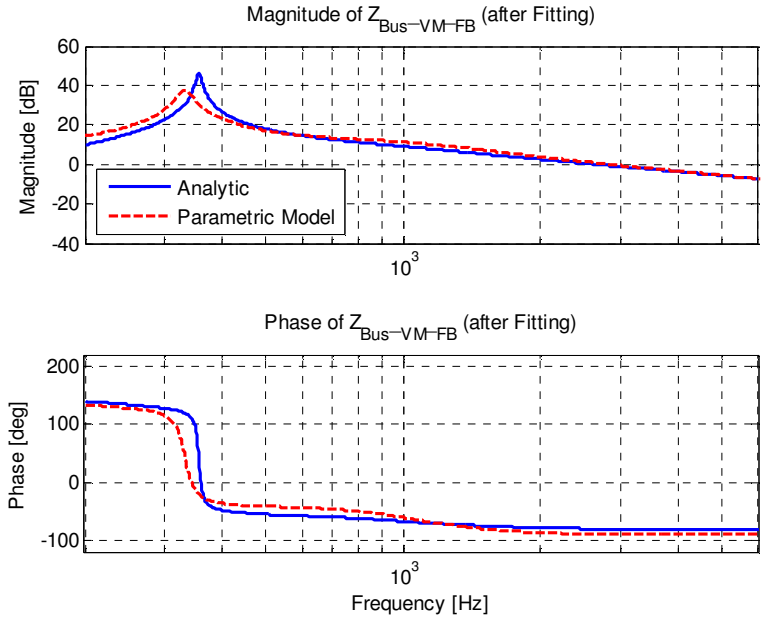


Figure 4.38. Bode plot of the bus impedance analytic transfer function (blue line) and fitted parametric model via logarithmic thinning (red dashed line) for set 3.

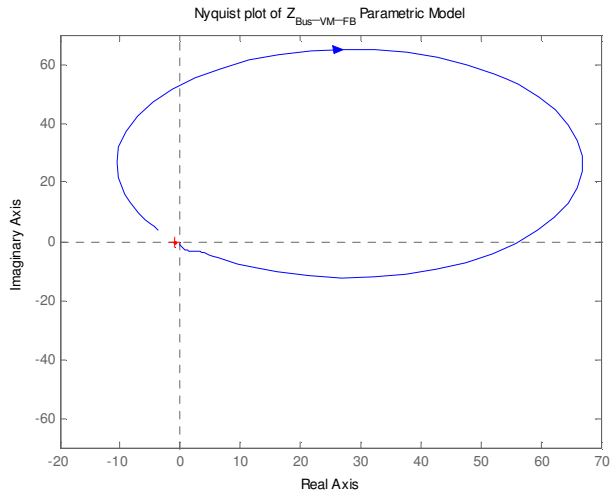


Figure 4.39. Nyquist plot of the bus impedance fitted parametric model via logarithmic thinning for set 3.

The fitted impedance for set 3 is:

$$Set\,3:$$

$$Z_{bus\_FB} = \frac{1.618e004\,s^3 + 1.174e008\,s^2 + 2.608e011\,s - 3.172e014}{s^4 + 6871\,s\text{^}3 + 4.635e007\,s^2 + 3.521e010\,s + 1.785e014} \tag{4.5}$$

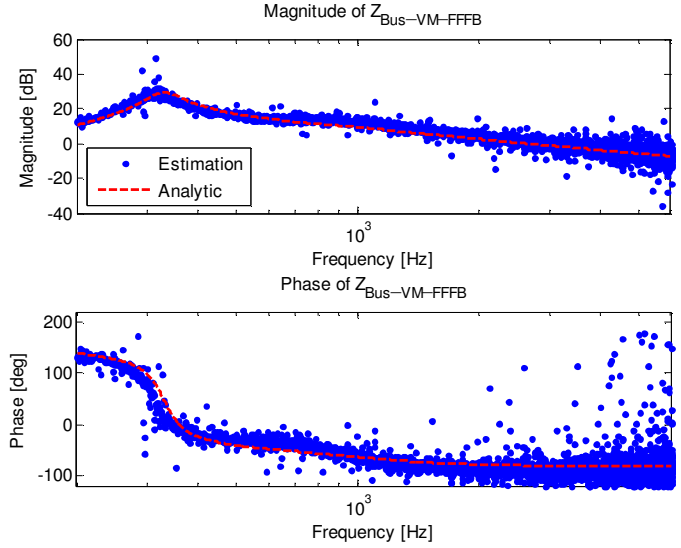


Figure 4.40. Bode plot of the bus impedance nonparametric estimation and analytic transfer function for set 4.

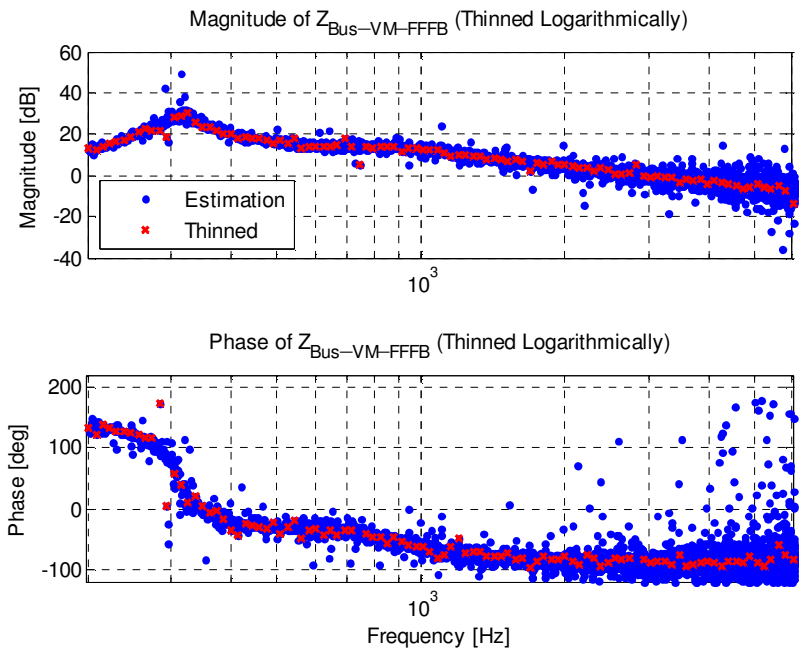


Figure 4.41. Bode plot of the bus impedance nonparametric estimation data (blue dots) and logarithmically thinned subset (red crosses) for set 4.

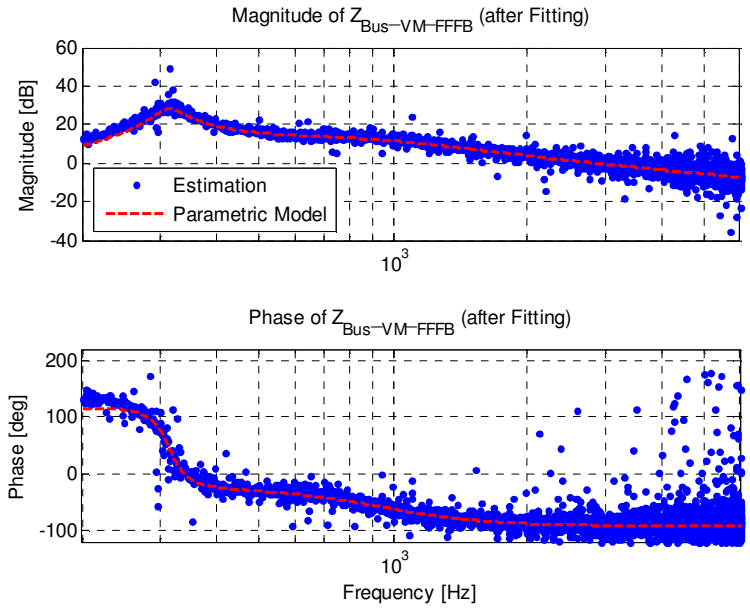


Figure 4.42. Bode plot of the bus impedance nonparametric estimation data (blue dots) and fitted parametric model via logarithmic thinning (red dashed line) for set 4.

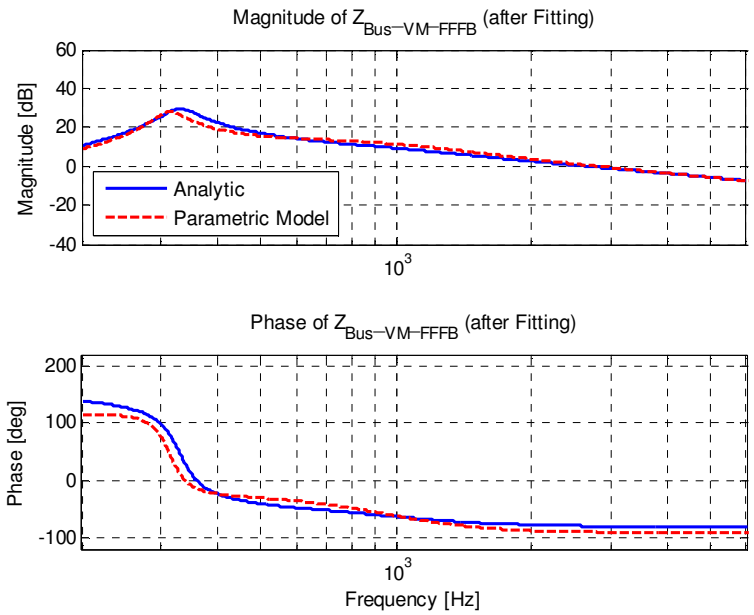


Figure 4.43. Bode plot of the bus impedance analytic transfer function (blue line) and fitted parametric model via logarithmic thinning (red dashed line) for set 4.

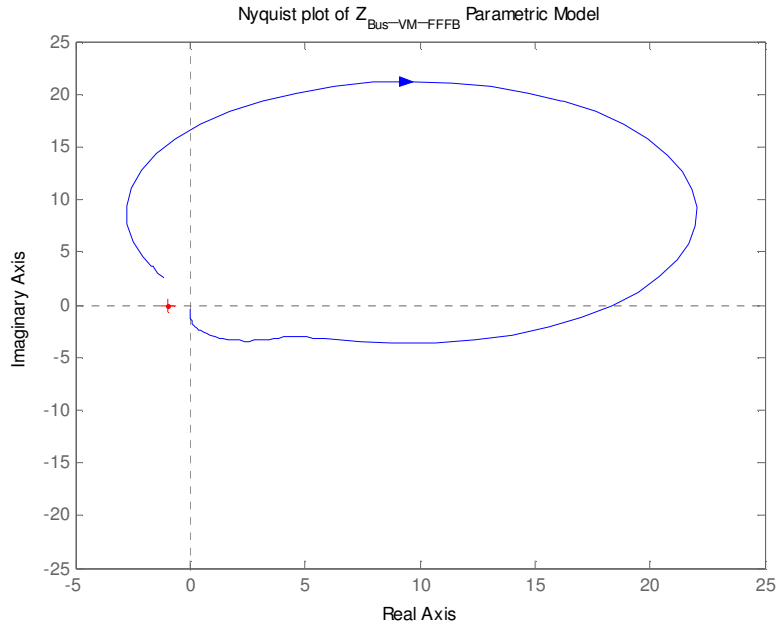


Figure 4.44. Nyquist plot of the bus impedance fitted parametric model via logarithmic thinning for set 4.

The fitted impedance for set 4 is:

$$Set\,4:$$
$$Z_{bus\_FFFB} = \frac{1.585e004\,s^3 + 1.263e008\,s^2 + 1.473e011\,s + 3.548e013}{s^4 + 7081\,s^3 + 4.052e007\,s^2 + 3.635e010\,s + 1.345e014} \tag{4.6}$$

To verify the stability improvement introduced by the PFF control, time domain experimental results of the FB case and the FFFB case are compared. Figs. 4.45-4.48 show transient responses of the bus voltage and three-phase output voltage for a VSI voltage reference step from $22.5V_{pk}$ to $45V_{pk}$. For FB control only (Figs. 4.45, 4.47), the interaction between source and the load subsystems causes sustained DC input voltage oscillation due to the passivity condition marginally met at the resonant frequency. Let us examine the PFF case now. Due to the active damping around the resonant frequency of the input filter introduced by the PFF control, the DC input voltage of the inverter is highly stabilized as shown in Figs. 4.46, 4.48. These time domain results are in excellent agreement with the frequency domain results as far as system stability using the practical PBSC.

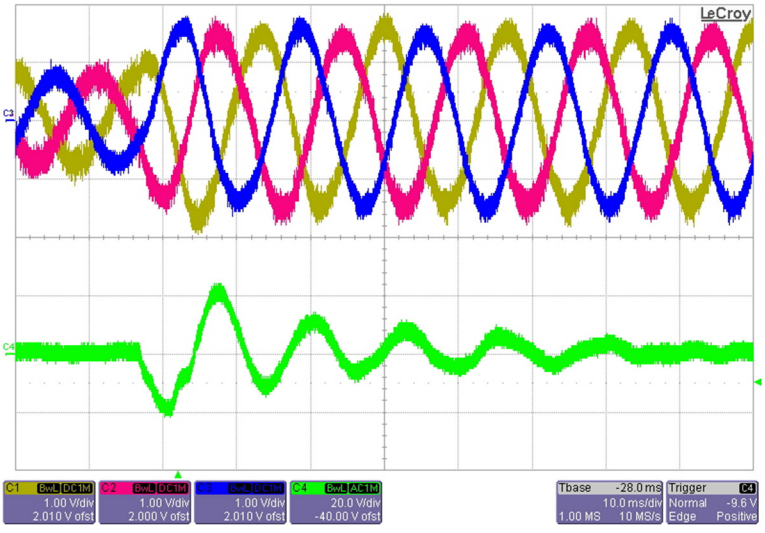


Figure 4.45. The AC coupled bus voltage and sensed three-phase output voltage of the VSI under FB control for a voltage reference step of $22.5V_{pk} \rightarrow 45V_{pk}$ for set 1.

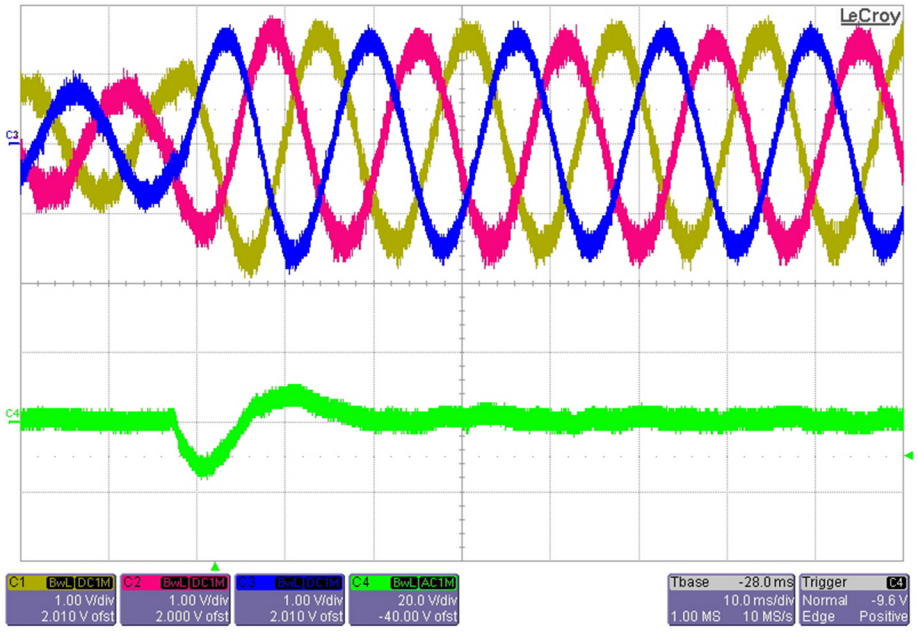


Figure 4.46. The AC coupled bus voltage and sensed three-phase output voltage of the VSI under FFFB control for a voltage reference step of $22.5V_{pk} \rightarrow 45V_{pk}$ for set 2.

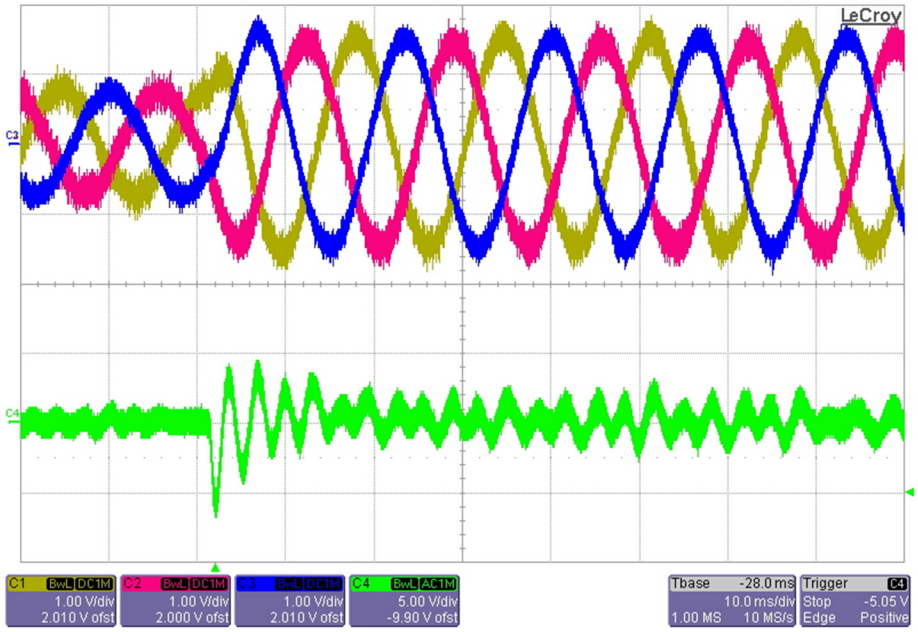


Figure 4.47. The AC coupled bus voltage and sensed three-phase output voltage of the VSI under FB control for a voltage reference step of $22.5V_{pk} \rightarrow 45V_{pk}$ for set 3.

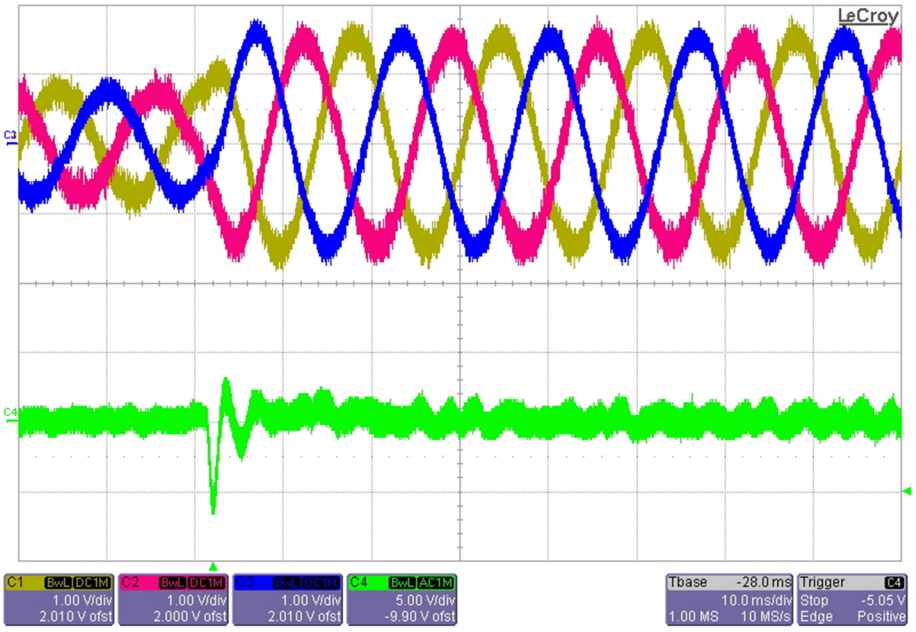


Figure 4.48. The AC coupled bus voltage and sensed three-phase output voltage of the VSI under FFFB control for a voltage reference step of $22.5V_{pk} \rightarrow 45V_{pk}$ for set 4.

4.3. DISCUSSION

In this concluding section, a discussion of simulation and experimental results is provided first and then the fitting process is discussed.

Regarding the results, it is noteworthy that all the frequency-domain bus impedance measurement results in Figs. 4.25 to 4.44 correctly predict stable operation of the system according to the hypothesized practical PBSC criterion. All the Nyquist plots of the fitted bus impedance transfer functions in Figs. 4.29, 4.34, 4.39, and 4.44 show a contour that has a unique intersection with the positive real axis. The fact that the system is stable under all the investigated control configurations is also confirmed by the time-domain results in Figs. 4.45 to 4.48. However, for the cases of FB control only (Figs. 4.45 and 4.47) the transient response is more oscillatory than for the cases of FFFB control (Figs. 4.46 and 4.48). For the FB control only cases the oscillations last about *70*

ms, while for the FFFB control they are reduced to about *15 ms*. This is in agreement with the bus impedance Nyquist plots; notice the reduction of the equivalent radius of the contour from about *70* to about *12* in Figs. 4.29 and 4.34 for the case of the cascade of a PICM_FB-controlled buck converter and PICM_FFFB-controlled VSI, and the reduction of the equivalent radius of the contour from about *70* to about *23* in Figs. 4.39 and 4.44 for the case of the cascade of a VM_FB-controlled buck converter and PICM_FFFB-controlled VSI. A bus impedance with a large Nyquist contour means that the system has a lightly damped resonance and is therefore close to the instability (it is closer to the passivity boundary), while a bus impedance with a small Nyquist contour is far away from instability. Moreover, notice the resonant peak reduction of about *15dB* for the case of the cascade of a PICM_FB-controlled buck converter and PICM_FFFB-controlled VSI (Figs. 4.25 and 4.30), and the resonant peak reduction of about *10dB* for the case of the cascade of a VM_FB-controlled buck converter and PICM_FFFB-controlled VSI (Figs. 4.35 and 4.40). This shows that the proposed PFF design procedure based on the PBSC criterion is effective in improving system stability.

Last, the fitting process is discussed. The fitting process from the thinned data points provides good matching of the obtained parametric transfer functions (4.3)-(4.6) with the corresponding analytic transfer functions, as shown in Figs. 4.28, 4.33, 4.38, and 4.43. However, some little discrepancies are present around the resonant frequency and at low frequency. To understand this, the fitting process is described in more detail. First, thinning is applied to the nonparametric data by creating an equally logarithmically spaced frequency index from a starting frequency to an ending frequency. Within the chosen range of frequency the engineer has to choose the number of points. Then, the

fitting is carried out on the thinned data points by using the MATLAB function "invfreqs" which converts magnitude and phase data into a least-squares-fitted transfer function. As an example, the command [b,a]=invfreqs(h,w,n,m) (complex frequency response is given in vector h at the frequency points specified in vector w) returns the real numerator and denominator coefficient vectors b and a of the following transfer function

$$H(s) = \frac{B(s)}{A(s)} = \frac{b_1 s^n + b_2 s^{n-1} + \ldots + b_{n+1}}{a_1 s^m + a_2 s^{m-1} + \ldots + a_{m+1}} \tag{4.7}$$

where n and m specify the desired orders of the numerator and denominator polynomials. The orders of numerator and denominator are chosen to be quite low, 3 and 5 for the case, for example, of the fitted bus impedance in (4.3). The order of the system is actually 9. It is interesting to note that, even if the system order is 9, a fifth order fitting provides a fairly good approximation. This indicates that reduced order models can be successfully used for modeling this type of multi-converter systems. The main source of discrepancy between fitted model and analytic transfer functions may be attributed to the significant amount of noise present in the measurement. This is typical of switching converter systems. Another source of discrepancy may be attributed to the choice of a large enough number of points for the thinning to capture the sharpest feature of the transfer function around the resonant frequency, as explained before in the previous section. Another source of discrepancy is due to parameter tolerances of the reactive elements in the system. In particular, it was shown in [81] that the inductance values of the powdered iron inductors used in the experimental setup is a function of bias current.

CHAPTER 5

CONCLUSIONS AND FUTURE WORK

5.1. CONCLUSIONS

The present work was motivated by the penetration of power electronics converters in DC Power Distribution Systems. This introduces several advantages in term of system reliability, interface flexibility, high power density, and power flow controllability. However, power-electronics-based DC Power Distribution Systems face the problem of system stability degradation when the interactions among converters due to CPLs become significant. This is not a trivial problem, especially when the system becomes quite big due to the large number of interconnected power converters. This work presents two original contributions to solve stability issues in DC Power Distribution Systems: the practical Passivity-Based Stability Criterion (PBSC) for system stability analysis, and the Positive Feed-Forward (PFF) control for system stability improvement.

In Chapter 2, the PBSC was proposed as a new stability criterion based on the passivity of the bus impedance. If that impedance is passive then the entire system is stable. Advantages of the PBSC over prior stability criteria, based on the minor loop gain concept, were discussed. It was shown that the PBSC in its raw form provides only a sufficient condition for system stability, like prior stability criteria based on the minor loop gain. For this reason, by linking the passivity concept to the Nyquist Criterion, which instead provides necessary and sufficient conditions for system stability, the

practical PBSC was proposed. The practical PBSC is based on the passivity condition of the system bus impedance in a limited range of frequency around the resonant frequency. This makes the practical PBSC very design oriented.

Chapter 3 presented the PFF control as an active method to improve system stability. With the PFF control, it is possible to design stabilizing virtual damping impedances so that the practical PBSC is satisfied. In particular, it was shown that the PFF control actively introduces the stabilizing virtual impedance Z_{damp} in parallel to the already existing load subsystem input impedance Z_{in_FB} and source subsystem output impedance Z_S. Design rules for Z_{damp} based on the practical PBSC were given in all their mathematical details. Since PFF control is an active technique, problems related to purely passive techniques, such as increased cost, weight, power dissipation, and large inrush currents are overcome. Compared with other active approaches, the PFF control has a much simpler implementation.

Finally, in Chapter 4, the usefulness of the practical PBSC in system stability online monitoring and design of the PFF control so that the entire system is stable and well-behaved was proved in a DC power distribution system example. The wideband system identification was the tool used to measure the bus impedance and address system level stability issues in a DC power distribution system. Frequency domain and time domain results were presented by using system switching model simulations and experimentally in a system built in the laboratory.

5.2. FUTURE WORK

Future work consists of the following tasks:

5.2.1. GENERALIZATION OF THE PBSC

Generalization of the practical PBSC to the case of a multi bus DC Power Distribution System has to be considered. This is motivated by multi bus systems that nowadays find several applications, like Advanced Automotive Power Systems, Electric and Hybrid Electric Vehicles, More Electric Aircraft Power Systems, and Space Power Systems, as described in [76]. In these systems the application of all prior stability criteria seems to be very tedious and for some aspects not feasible.

A multi bus system is represented in Fig. 5.1. It has *n* buses and could also have a large number of converters connected to the various buses. By looking at each bus port, it is possible to reduce the given multi bus system to an equivalent n-port network. The main difference with respect to the single bus case is that now the bus impedance is a matrix. The system bus impedance can be calculated (measured) as follows

$$\vec{V}_{bus} = \vec{Z}_{bus}\vec{I}$$

$$\begin{bmatrix} V_{bus1} \\ V_{bus2} \\ \vdots \\ V_{busn} \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} & \cdots & Z_{1n} \\ Z_{21} & Z_{22} & \cdots & Z_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ Z_{n1} & Z_{n2} & \cdots & Z_{nn} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ \vdots \\ I_n \end{bmatrix} \tag{5.1}$$

where V_{bus1}, V_{bus2}, …, V_{busn} are the bus voltages and I_1, I_2, …, I_n are the injection currents. Clearly, Z_{ij} for $i=j$ is the self-impedance of the i^{th} bus, while Z_{ij} for $i\neq j$ is the cross-impedance between the i^{th} bus and the j^{th} bus. The self impedance is the parallel combination of all the converters' input impedances connected to the i^{th} bus under the condition of no injection current in any of the remaining n-1 buses. The cross impedance represents the effect of a current injected on the j^{th} bus on the voltage on the i^{th} bus. Mathematically we can write (5.2) and (5.3) for self and cross impedances, respectively.

$$Z_{ii} = \left.\frac{Vi}{Ii}\right|_{I_k=0} \qquad \forall k \neq i \tag{5.2}$$

$$Z_{ij} = \left.\frac{Vi}{Ij}\right|_{I_k=0} \qquad \forall k \neq j \tag{5.3}$$

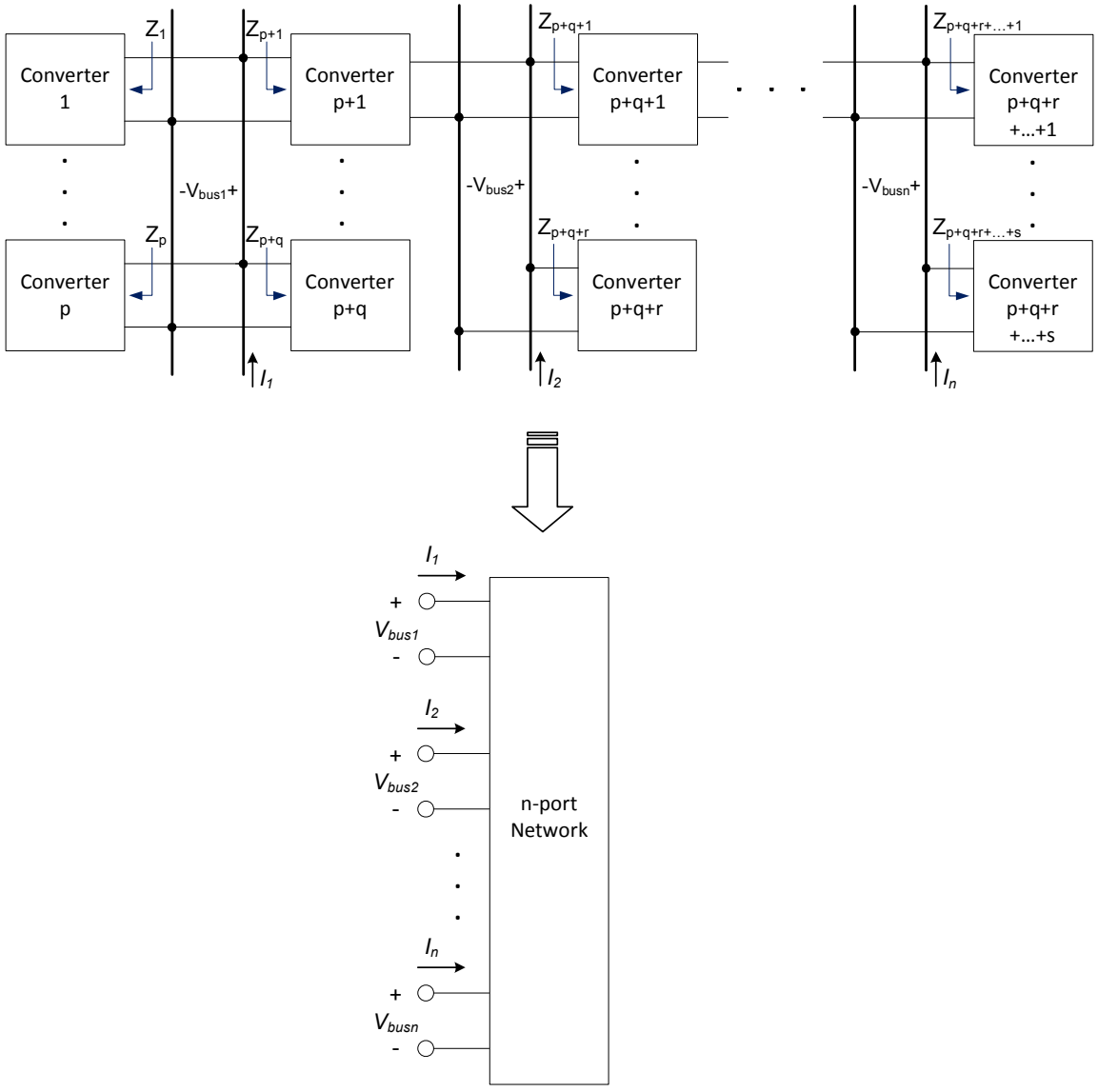


Figure 5.1. Multi-bus system and its reduction to an equivalent n-port network.

Clearly, the passivity of the i^{th} bus can affect the passivity of the j^{th} bus and vice versa. For this reason, more general passivity criteria must be found for the case of a multi bus system. This passivity criterion should be developed in the frequency domain as done for the single bus case. Appendix E shows the passivity concept for a n-port electrical network. Moreover, the PBSC for a multi bus system must be much better understood and verified in simulation and experimentally with a reasonable complex system.

5.2.2. ADAPTIVE PFF CONTROL

One possible adaptive PFF control structure is shown in Fig. 5.2. The bus is perturbed by a test signal of user-specified amplitude so that all frequencies are excited. The bus impedance transfer function is therefore obtained via identification. This transfer function can be seen as the most up-to-date estimate of the status of the passivity of the bus. This information is used to synthesize an appropriate PFF control to provide the desired stabilizing active damping at each instant of time. The identification technique as well as the control adaptation algorithm may be implemented into an embedded controller. Due to the simultaneous need of speed in calculation and large amount of memory, a Field Programmable Gate Array (FPGA) is recommended to be used as embedded controller. The idea is to come up with an intelligent PFF control that varies its parameters according to an algorithm based on bus passivity assessments. A study for developing an appropriate adaptation algorithm is needed.

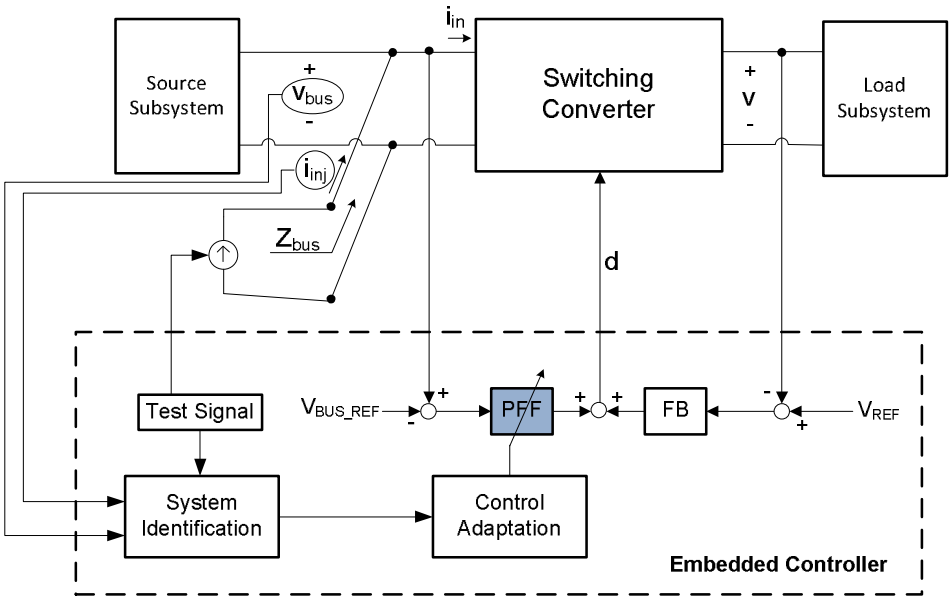


Figure 5.2. Proposed control architecture for adaptive PFF control.

5.2.3. GLOBAL CONTROL

In DC Power Distribution Systems, like the proposed MVDC Systems for the US Navy All Electric Ship in Fig. 1.1, to address system-level stability issues, a high-level coordinating global control is required, but there is generally a need for a low-level, local intelligent control which can act in a way to stabilize the system under dynamic operating conditions imposed by load requirements and global control actions. The problem is to develop such a local-global control method to increase system stability robustness using online monitoring and adaptive control. In fact, to properly design a stabilizing control, the designer must have knowledge of the bus impedance. On-line monitoring of the bus impedance enables a possible adaptation of stabilizing controller parameters in an intelligent manner as the system changes for a different power demand or reconfiguration. The information collected from the on-line monitoring could be communicated between converters or to a higher-level central controller. A supervisory

or agent-based control architecture could use this on-line measurement data to make an appropriate decision about converter coordination to ensure overall stability.

Other issues on a DC Power Distribution System must be addressed for which global control may help. In DC distribution power systems, the supply must match with the demand of power at the load side to ensure stable and reliable operation. This is not a trivial control task. The task becomes even more complicated in case of an insufficient supply or insufficient distribution to deliver power to the load. Many DC distribution systems, such as shipboard systems, are finite energy systems. Without the ability to connect to an auxiliary source of energy, these systems may operate near the threshold of being energy constrained [77, 78].

System stability requires a control system that is fault-tolerant and self-healing. Fault-tolerant control should guarantee the survival of the system with partial loss or malfunction of system components [79, 80]. Self-healing controls take actions to reduce further disruptions of the system to ensure that the remaining components operate as best as possible. These two qualities are crucial in Naval applications, since the power system may be required to continue to operate under external attacks.

Another scenario that needs to be investigated is the turning on and off of converters. For example, if the converter that was responsible for introducing the active damping in the system is turned off for some reason, a decision among agents must be taken in order to determine which other converter will be entrusted of introducing the same damping.

The last issue that needs to be addressed in DC Power Distribution Systems is the impact of storage elements on the system and their impact on system stability.

REFERENCES

[1] M. E. Baran and N. R. Mahajan, "DC distribution for industrial systems: opportunities and challenges," IEEE Trans. Industry Applications, vol. 39, no. 6, pp. 1596-1601, Nov. 2003.

[2] Qianzhi Zhou; Defang Yuan, "Prediction on future DC power system," Power Electronics and Motion Control Conference, 2009. IPEMC '09. IEEE 6th International , vol., no., pp.1192-1195, 17-20 May 2009.

[3] Parker, D.S.; Hodge, C.G., "The electric warship [electric propulsion]," Power Engineering Journal, Volume: 12 Issue: 1 , Feb. 1998, Page(s): 5 -13.

[4] Clayton, D.A.; Sudhoff, S.D.; Grater, G.F., "Electric ship drive and power system," Power Modulator Symposium, 2000. Conference Record of the 2000 Twenty-Fourth International, 2000, Page(s): 85 -88.

[5] N. Doerry, Next Generation Integrated Power Systems, NGIPS Master Plan, Whashington, DC: Naval Sea Systems Command, 2007.

[6] A. Emadi, A. Khaligh, C. H. Rivetta, and G. A. Williamson, "Constant power loads and negative impedance instability in automotive systems: definition, modeling, stability, and control of power electronic converters and motor drives," *IEEE Trans. Vehicular Technology*, vol. 55, pp. 1112-1125, Jul. 2006.

[7] A. Khaligh, A. M. Rahimi, and A. Emadi, "Modified Pulse-Adjustment Technique to Control DC/DC Converters Driving Variable Constant-Power Loads," *IEEE Trans. Industrial Electronics*, vol. 55, no. 3, pp. 1133-1146, Mar. 2008.

[8] IEEE Std 1709-2010, "IEEE Recommended Practice for 1 kV to 35 kV Medium-Voltage DC Power Systems on Ships," IEEE Std 1709-2010, vol., no., pp.1-54, Nov. 2 2010.

[9] Y. Jang and R. W. Erickson, "Physical origins of input filter oscillations in current programmed converters," *IEEE Trans. Power Electronics*, vol. 7, no. 4, pp. 725-733, Jul. 1992.

[10] Emadi, A.; Ehsani, A.; , "Dynamics and control of multi-converter DC power electronic systems ," *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual* , vol.1, no., pp.248-253 vol. 1, 2001.

[11] A. Emadi, B. Fahimi, and M. Ehsani, "On the concept of negative impedance instability in advanced aircraft power systems with constant power loads," *Society of Automotive Engineers (SAE) Journal, Paper No. 1999-01-2545*, 1999.

[12] A. B. Jusoh, "The instability effect of constant power loads," in *Proc. IEEE National Power and Energy Conference*, 2004, pp. 175-179.

[13] Middlebrook, R.D., "Input Filter Considerations in Design and Application of Switching Regulators," IEEE IAS Annual Meeting, 1976.

[14] Wildrick, C.M.; Lee, F.C.; Cho, B.H.; Choi, B.; , "A method of defining the load impedance specification for a stable distributed power system," Power Electronics, IEEE Transactions on , vol.10, no.3, pp.280-285, May 1995.

[15] Xiaogang Feng; Zhihong Ye; Kun Xing; Lee, F.C.; Borojevic, D.; , "Impedance specification and impedance improvement for DC distributed power system," Power Electronics Specialists Conference, 1999. PESC 99. 30th Annual IEEE , vol.2, no., pp.889-894 vol.2, 1999.

[16] Xiaogang Feng; Zhihong Ye; Kun Xing; Lee, F.C.; Borojevic, D.; , "Individual load impedance specification for a stable DC distributed power system," Applied Power Electronics Conference and Exposition, 1999. APEC '99. Fourteenth Annual , vol.2, no., pp.923-929 vol.2, 14-18 Mar 1999.

[17] Xiaogang Feng; Jinjun Liu; Lee, F.C.; , "Impedance specifications for stable DC distributed power systems ," Power Electronics, IEEE Transactions on , vol.17, no.2, pp.157-162, Mar 2002.

[18] Sudhoff, S.D.; Glover, S.F.; Lamm, P.T.; Schmucker, D.H.; Delisle, D.E.; , "Admittance space stability analysis of power electronic systems," Aerospace and Electronic Systems, IEEE Transactions on , vol.36, no.3, pp. 965- 973, Jul 2000.

[19] Sudhoff, S.D.; Glover, S.F.; , "Three-dimensional stability analysis of DC power electronics based systems," Power Electronics Specialists Conference, 2000. PESC 00. 2000 IEEE 31st Annual , vol.1, no., pp.101-106 vol.1, 2000.

[20] Sudhoff, S.D.; Crider, J.M.; , "Advancements in generalized immittance based stability analysis of DC power electronics based distribution systems," Electric Ship Technologies Symposium (ESTS), 2011 IEEE , vol., no., pp.207-212, 10-13 April 2011.

[21] Riccobono, A.; Santi, E.; , "Comprehensive review of stability criteria for DC distribution systems," *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE* , vol., no., pp.3917-3925, 15-20 Sept. 2012.

[22] Panov, Y.; Jovanovic, M.; , "Practical issues of input/output impedance measurements in switching power supplies and application of measured data to

stability analysis," *Applied Power Electronics Conference and Exposition, 2005. APEC 2005. Twentieth Annual IEEE* , vol.2, no., pp.1339-1345 Vol. 2, 6-10 March 2005.

[23] Xiaogang Feng; Lee, F.C.; , "On-line measurement on stability margin of DC distributed power system," *Applied Power Electronics Conference and Exposition, 2000. APEC 2000. Fifteenth Annual IEEE* , vol.2, no., pp.1190-1196 vol.2, 2000.

[24] X. Wang, R. Yao, and F. Rao, "Three-step impedance criterion for small-signal stability analysis in two-stage DC distributed power systems," *IEEE Power Electronics Letters*, vol. 1, pp. 83-87, Sept. 2003.

[25] H. Y. Cho and E. Santi, "Modeling and stability analysis in multi-converter systems including positive feedforward control," in *Proc. IEEE 34th Annual Conference IECON08*, Nov. 2008, pp. 839-844.

[26] Vesti, S.; Oliver, J.A.; Prieto, R.; Cobos, J.A.; Suntio, T., "Simplified small-signal stability analysis for optimized power system architecture," *Applied Power Electronics Conference and Exposition (APEC), 2013 Twenty-Eighth Annual IEEE* , vol., no., pp.1702,1708, 17-21 March 2013.

[27] Vesti, S.; Suntio, T.; Oliver, J.A.; Prieto, R.; Cobos, J.A., "Impedance-Based Stability and Transient-Performance Assessment Applying Maximum Peak Criteria," *Power Electronics, IEEE Transactions on* , vol.28, no.5, pp.2099,2104, May 2013.

[28] R. D. Middlebrook, "Null double injection and the extra element theorem," *IEEE Trans. Education*, vol. 32, pp. 167-180, Aug. 1989.

[29] R. D. Middlebrook, "The two extra element theorem," *in Proc. IEEE 21st Annu. Frontiers in Education Conference*, pp. 702-708, 1991.

[30] G. S. Thandi, R. Zhang, K. Xing, F. C. Lee, and D. Boroyevich, "Modeling, control and stability analysis of a PEBB based DC DPS," *IEEE Trans. Power Delivery*, vol. 14, pp. 497-505, Apr. 1999.

[31] Tucker, J.; Martin, D.; Mersenski, R.; Barkley, A.; Cairoli, P.; Ghisla, U.; Riccobono, A.; Dougal, R.; Santi, E.; , "Fault protection and ride-through scheme for MVDC power distribution systems utilizing a supervisory controller," *Electric Ship Technologies Symposium (ESTS), 2011 IEEE* , vol., no., pp.319-325, 10-13 April 2011.

[32] B. Choi and B. H. Cho, "Intermediate line filter design to meet both impedance compatibility and EMI specifications," *IEEE Trans. Power Electronics*, vol. 10, no. 5, pp. 583-588, Sept. 1995.

[33] B. Choi, B. H. Cho, and S.-S. Hong, "Dynamics and control of DC-to-DC converters driving other converters downstream," *IEEE Trans. Circuits and Systems I, Fundam. Theory Appl.*, vol. 46, no. 10, pp. 1240-1248, Oct. 1999.

[34] K. Xing, J. Guo, W. Huang, D. Peng, F. C. Lee, and D. Borojevic, "An active bus conditioner for a distributed power system," in *Proc. IEEE 30th Annu. Power Electronics Specialists Conference*, vol. 2, 1999, pp. 895-900.

[35] D. Logue and P. T. Krein, "The power buffer concept for utility load decoupling," in *Proc. IEEE 31st Annu. Power Electronics Specialists Conference*, vol. 2, Jun. 2000, pp. 973-978.

[36] D. L. Logue and P. T. Krein, "Preventing instability in DC distribution systems by using power buffering," in *Proc. IEEE 32nd Annual Power Electronics Specialists Conference*, vol. 1, Jun. 2001, pp. 33-37.

[37] Rahimi, A.M.; Emadi, A., "Active Damping in DC/DC Power Electronic Converters: A Novel Method to Overcome the Problems of Constant Power Loads," *Industrial Electronics, IEEE Transactions on* , vol.56, no.5, pp.1428,1439, May 2009.

[38] Magne, P.; Marx, D.; Nahid-Mobarakeh, B.; Pierfederici, S., "Large-Signal Stabilization of a DC-Link Supplying a Constant Power Load Using a Virtual Capacitor: Impact on the Domain of Attraction," *Industry Applications, IEEE Transactions on* , vol.48, no.3, pp.878,887, May-June 2012.

[39] Maheshwari, R.; Munk-Nielsen, S.; Kaiyuan Lu, "An Active Damping Technique for Small DC-Link Capacitor Based Drive System," *Industrial Informatics, IEEE Transactions on* , vol.9, no.2, pp.848,858, May 2013.

[40] Sulligoi, G.; Bosich, D.; Lin Zhu; Cupelli, M.; Monti, A., "Linearizing control of shipboard multi-machine MVDC power systems feeding Constant Power Loads," *Energy Conversion Congress and Exposition (ECCE), 2012 IEEE* , vol., no., pp.691,697, 15-20 Sept. 2012.

[41] Sulligoi, G.; Bosich, D.; Arcidiacono, V.; Giadrossi, G., "Considerations on the Design of Voltage Control for Multi-Machine MVDC Power Systems on Large Ships," *Electric Ship Technologies Symposium (ESTS), 2013 IEEE* , vol., no., pp.314-319, 22-24 April 2013.

[42] Riccobono, A.; Santi, E.; , "A novel Passivity-Based Stability Criterion (PBSC) for switching converter DC distribution systems," *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE* , vol., no., pp.2560-2567, 5-9 Feb. 2012.

[43] Riccobono, Antonino; Santi, Enrico, "Stability analysis and design of stable DC distribution systems through positive feed-forward control using a novel passivity-based stability criterion," *Applied Power Electronics Conference and*

Exposition (APEC), 2013 Twenty-Eighth Annual IEEE , vol., no., pp.1693,1701, 17-21 March 2013.

[44] Riccobono, A.; Santi, E.; , " Stability Analysis of an All-Electric Ship MVDC Power Distribution System Using a Novel Passivity-Based Stability Criterion," *Electric Ship Technologies Symposium (ESTS), 2013 IEEE* , vol., no., pp.411-419, 22-24 April 2013.

[45] Cho, H.Y.; Santi, E.; , "Modeling and Stability Analysis of Cascaded Multi-Converter Systems Including Feedforward and Feedback Control," Industry Applications Society Annual Meeting, 2008. IAS '08. IEEE , vol., no., pp.1-8, 5-9 Oct. 2008.

[46] H. Y. Cho and E. Santi, "Peak-current-mode-controlled buck converter with positive feedforward control," in Proc. IEEE Energy Conversion Congress and Exposition, Sept. 2009, pp. 2928-2935.

[47] Riccobono, A.; Santi, E.; , "Positive Feed-Forward control of three-phase voltage source inverter for DC input bus stabilization," Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE , vol., no., pp.741-748, 6-11 March 2011.

[48] Riccobono, A.; Santi, E.; , "Positive Feed-Forward control of three-phase voltage source inverter for DC input bus stabilization with experimental validation," in press for publication in the IEEE Transactions on Industry Applications on April, 16th 2012.

[49] Kelkar, S.S.; Lee, F.C.; , "A Novel Feedforward Compensation Canceling Input Filter-Regulator I nteraction," Aerospace and Electronic Systems, IEEE Transactions on, vol.AES-19, no.2, pp.258-268, March 1983.

[50] Kelkar, S.S.; Lee, F.C.; , "Comments on "A Novel Feedforward Compensation Canceling Input Filter-Regulator Interaction"," Aerospace and Electronic Systems, IEEE Transactions on , vol.AES-21, no.4, pp.584-587, July 1985.

[51] King, R.J.; , "Feedforward control laws for the buck converter," Computers in Power Electronics, 1994., IEEE 4th Workshop on , vol., no., pp.192-197, 7-10 Aug 1994.

[52] Kazimierczuk, M.K.; Massarini, A.; , "Feedforward control of DC-DC PWM boost converter," Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on , vol.44, no.2, pp.143-148, Feb 1997.

[53] Arbetter, B.; Maksimovic, D.; , "Feedforward pulse width modulators for switching power converters ," Power Electronics, IEEE Transactions on , vol.12, no.2, pp.361-368, Mar 1997.

[54] Kazimierczuk, M.K.; Starman, L.A.; , "Dynamic performance of PWM DC-DC boost converter with input voltage feedforward control," Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on , vol.46, no.12, pp.1473-1481, Dec 1999.

[55] Kazimierczuk, M.K.; Edstrom, A.J.; , "Open-loop peak voltage feedforward control of PWM buck converter ," Circuits and Systems I: Fundamental Theory and Applications, IEEE Transactions on , vol.47, no.5, pp.740-746, May 2000.

[56] Sjoroos, J.-P.; Suntio, T.; Kyyra, J.; Kostov, K.; , "Dynamic performance of buck converter with input voltage feedforward control," Power Electronics and Applications, 2005 European Conference on , vol., no., pp.9 pp.-P.9, 0-0 0.

[57] Peng Zhang; Xuhui Wen; Jun Liu; , "Feed-Forward Control for Stability Improvement in Cascaded System," Electrical and Control Engineering (ICECE), 2010 International Conference on , vol., no., pp.3746-3749, 25-27 June 2010.

[58] Peng Zhang; Xuhui Wen; Jun Liu; , "Feed-Forward Control for Stability Improvement in Cascaded System," Electrical and Control Engineering (ICECE), 2010 International Conference on , vol., no., pp.3746-3749, 25-27 June 2010.

[59] Colgate, J. E.; *The control of dynamically interacting systems*, Ph.D., M.I.T. 1998.

[60] Colgate, J. E.; "Stricly Positive Real Admittances for Coupled Stability, " Journal of the Franklin Institute, 329(3):429-444, 1992.

[61] Maciejowski, JM (1989) *Multivariable feedback design.* Addison-Wesley, Wokingham, UK, -. ISBN 0201182432.

[62] Pal, D.; Belur, M.N., "Finite gain and phase margins as dissipativity conditions," *American Control Conference (ACC), 2010* , vol., no., pp.337,342, June 30 2010-July 2 2010.

[63] Iwasaki, T.; Hara, S.; Yamauchi, H., "Dynamical system design from a control perspective: finite frequency positive-realness approach," *Automatic Control, IEEE Transactions on* , vol.48, no.8, pp.1337,1354, Aug. 2003.

[64] Barkley, A.; Dougal, R.; Santi, E., "Adaptive control of power converters using Digital Network Analyzer Techniques," *Applied Power Electronics Conference and Exposition (APEC), 2011 Twenty-Sixth Annual IEEE* , vol., no., pp.1824,1832, 6-11 March 2011.

[65] R. W. Erickson and D. Maksimovic, *Fundamentals of power electronics*, 2nd ed. Norwell, MA: Kluwer Academic, 2001.

[66] S. Hiti, D. Boroyevich, and C. Cuadros, "Small-signal modeling and control of three-phase PWM converters," in Proc. IEEE Industry Applications Society Annual Meeting, vol. 2, Oct. 1994, pp. 1143-1150.

[67] Ahmadi, R.; Paschedag, D.; Ferdowsi, M.; , "Closed-loop input and output impedances of DC-DC switching converters operating in voltage and current mode control," *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society* , vol., no., pp.2311-2316, 7-10 Nov. 2010.

[68] Cvetkovic, I.; Boroyevich, D.; Mattavelli, P.; Lee, F. C.; Dong, D.; , "Unterminated Small-Signal Behavioral Model of DC–DC Converters," *Power Electronics, IEEE Transactions on* , vol.28, no.4, pp.1870-1879, April 2013.

[69] Arnedo, L.; Burgos, R.; Boroyevich, D.; Wang, F.; , "System-Level Black-Box Dc-to-Dc Converter Models," *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE* , vol., no., pp.1476-1481, 15-19 Feb. 2009.

[70] B. Miao, R. Zane, D. Maksimovic, "System identification of power converters with digital control through cross-correlation methods," *Power Electronics, IEEE Transactions on* , vol.20, no.5, pp. 1093-1099, Sept. 2005.

[71] A. Barkley, E. Santi, "Improved Online Identification of Switching Converters Using Digital Network Analyzer Techniques" Power *Electronics Specialists Conference, 2008*. pp. 891-896, June 2008.

[72] Martin, D.; Santi, E.; Barkley, A.; , "Wide bandwidth system identification of AC system impedances by applying pertubations to an existing converter," Energy Conversion Congress and Exposition (ECCE), 2011 IEEE , vol., no., pp.2549-2556, 17-22 Sept. 2011.

[73] *DS1104 R&D Controller Board*. dSPACE GmbH, 2011. Print.

[74] "Real-Time Interface (RTI and RTI-MP)." *dSPACE Implementation Guide*. 5.3. dSPACE GmbH, 2007. Print.

[75] "ControlDesk Experiment Guide." *dSPACE Implementation Guide*. 5.3. dSPACE GmbH, 2007. Print.

[76] Emadi, A.; Ehsani, M., "Multi-converter power electronic systems: definition and applications," *Power Electronics Specialists Conference, 2001. PESC. 2001 IEEE 32nd Annual* , vol.2, no., pp.1230,1236 vol.2, 2001.

[77] F. Casamatta et al., "Management of interruptible loads for power systems security and operation," in *2002 IEEE Power Engineering Society Summer Meeting,* vol. 2, 2002, pp. 880-885.

[78] J. Eto et al., "Innovative development in load as a reliability resource," in *Proceeding, IEEE Power Engineering Society Winter Meeting,* vol. 2, 2002, pp. 1002-1004.

[79] K. Moslehi et al., “Framework for a self-healing power grid,” in *Proceeding, IEEE Power Engineering Society General Meeting,* vol. 3, 2005, pp. 3027-3034.

[80] M. Amin, “Toward self-healing energy infrastructure systems,” *IEEE Computer Applications in Power,* vol. 14, no. 1, pp. 20-28, Jan 2001.

[81] Martin, D.; Santi, E., "Auto tuning of digital deadbeat current controller for grid tied inverters using wide bandwidth impedance identification," *Applied Power Electronics Conference and Exposition (APEC), 2012 Twenty-Seventh Annual IEEE* , vol., no., pp.277,284, 5-9 Feb. 2012.

APPENDIX A – OL MODELING

The small-signal model of the open-loop converter under duty cycle control (OL subscript) based on g-parameter representation is given in this Appendix. First the model is obtained for the case of DC-DC converters and then for the case of a three-phase VSI. A block diagram for the small-signal model of an OL standalone converter is shown in Fig. A.1. The hatted quantities represent small-signal perturbations around the converter steady-state operating point.

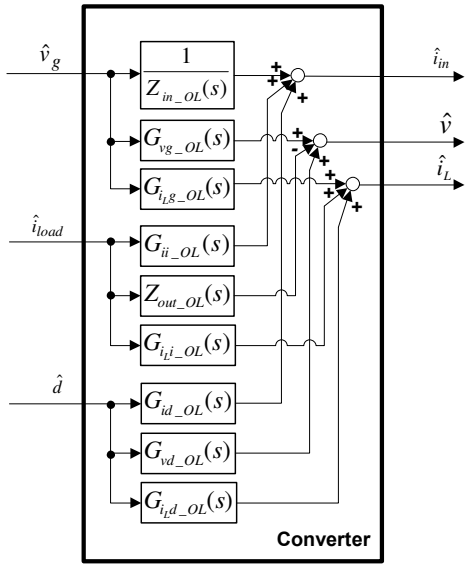


Figure A.1. Model of a standalone switching converter.

The small-signal OL converter model is the following

$$\begin{bmatrix} \hat{i}_{in} \\ \hat{v} \\ \hat{i}_L \end{bmatrix} = \begin{bmatrix} \frac{1}{Z_{in\_OL}} & G_{ii\_OL} & G_{ic\_OL} \\ G_{vg\_OL} & -Z_{out\_OL} & G_{vc\_OL} \\ G_{i_Lg\_OL} & G_{i_Li\_OL} & G_{i_Lc\_OL} \end{bmatrix} \begin{bmatrix} \hat{v}_g \\ \hat{i}_{load} \\ \hat{d} \end{bmatrix} \tag{A.1}$$

A.1. MODEL FOR A DC/DC CONVERTER

The OL transfer functions of (A.1) for buck, boost, and buck-boost converters are given in Table A.1.

Table A.1 OL transfer functions for buck, boost, and buck-boost converters.

	Buck	Boost	Buck-boost
$Y_{in\_OL}(s)$	$\frac{D^2}{R}\frac{(1+sRC)}{\left(1+s\frac{L}{R}+s^2LC\right)}$	$\frac{1}{D'^2R}\frac{(1+sRC)}{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}$	$\frac{D^2}{D'^2R}\frac{(1+sRC)}{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}$
$G_{id\_OL}(s)$	$\frac{V}{R}\left(1+\frac{(1+sRC)}{\left(1+s\frac{L}{R}+s^2LC\right)}\right)$	$\frac{V}{D'^2R}\frac{(1+(1+sRC))}{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}$	$-\frac{V}{D'^2R}\left(D'+\frac{(D+(1+sRC))}{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}\right)$
$G_{ii\_OL}(s)$	$\frac{D}{\left(1+s\frac{L}{R}+s^2LC\right)}$	$\frac{1}{D'}\frac{1}{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}$	$-\frac{D}{D'}\frac{1}{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}$
$G_{vg\_OL}(s)$	$\frac{D}{\left(1+s\frac{L}{R}+s^2LC\right)}$	$\frac{1}{D'}\frac{1}{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}$	$-\frac{D}{D'}\frac{1}{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}$
$G_{vd\_OL}(s)$	$\frac{V}{D}\frac{1}{\left(1+s\frac{L}{R}+s^2LC\right)}$	$\frac{V}{D'}\frac{\left(1-\frac{sL}{D'^2R}\right)}{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}$	$\frac{V}{D'D}\frac{\left(1-\frac{sLD}{D'^2R}\right)}{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}$
$Z_{out\_OL}(s)$	$\frac{sL}{\left(1+s\frac{L}{R}+s^2LC\right)}$	$\frac{1}{D'^2}\frac{sL}{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}$	$\frac{1}{D'^2}\frac{sL}{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}$
$G_{i_Li\_OL}(s)$	$\frac{V}{DR}\frac{(1+sRC)}{\left(1+s\frac{L}{R}+s^2LC\right)}$	$\frac{V}{D'R}\frac{\left(1-\frac{sL}{D'^2R}\right)(1+sRC)}{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}$	$\frac{V}{D'DR}\frac{\left(1-\frac{sLD}{D'^2R}\right)(1+sRC)}{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}$
$G_{i_Li\_OL}(s)$	$\frac{1}{\left(1+s\frac{L}{R}+s^2LC\right)}$	$\frac{1}{D'^2}\frac{1}{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}$	$\frac{1}{D'^2}\frac{1}{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}$
$G_{i_Lg\_OL}(s)$	$\frac{D}{R}\frac{(1+sRC)}{\left(1+s\frac{L}{R}+s^2LC\right)}$	$\frac{1}{D'R}\frac{(1+sRC)}{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}$	$\frac{D}{D'R}\frac{(1+sRC)}{\left(1+s\frac{L}{D'^2R}+s^2\frac{LC}{D'^2}\right)}$

A.2. MODEL FOR A VSI

A complete small-signal model for the three-phase VSI in Fig. A.2 is presented in this section based on *dq* rotating reference frame. The model of the stand-alone inverter, i.e., the inverter supplied by an ideal DC voltage source, is obtained by applying the *dq* transformation to all averaged state variables.

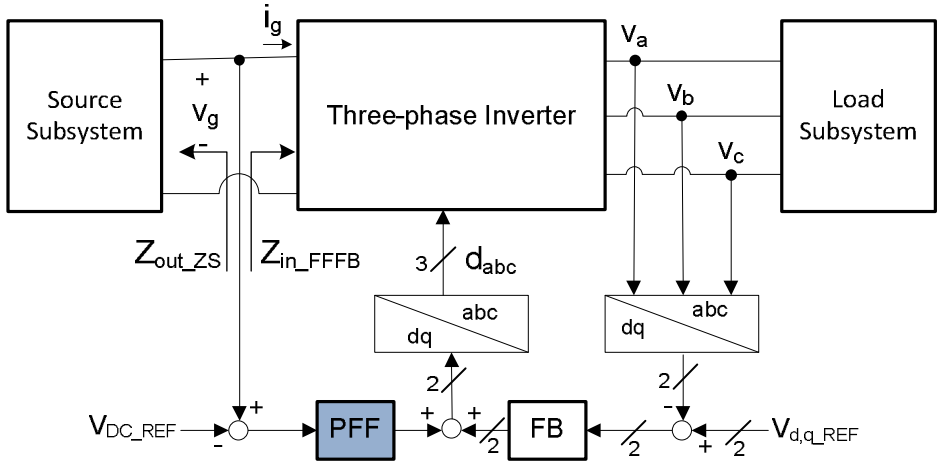


Figure A.2. Block diagram of a VSI.

The small-signal OL converter model (A.1) can still be used, but the elements of the matrix, except the input admittance, are matrices themselves. The OL transfer functions in model (A.1) are given by Equations (A.2)-(A.11). Notice also that, due to the decoupling technique implemented as in [48, 49] (commonly done to model such a type of converters), the whole system is equivalent to two independent DC/DC buck converters.

$$\frac{1}{Z_{in\_OL}} = \frac{3}{2}\frac{D_d^{\,2}}{R}\frac{(1+sRC)}{\left(1+s\frac{L}{R}+s^2LC\right)} \tag{A.2}$$

$$G_{igdd\_OL} = \frac{3}{2}\frac{V_g}{R}\left(\frac{I_d R}{V_g} + \frac{D_d(1+sRC)}{\left(1+s\frac{L}{R}+s^2LC\right)}\right) \tag{A.3}$$

$$G_{igdq\_OL} = \frac{3}{2}\frac{V_g}{R}\left(\frac{I_q R}{V_g}\right) \tag{A.4}$$

$$G_{igid\_OL} = \frac{3}{2}D_d\frac{1}{\left(1+s\frac{L}{R}+s^2LC\right)} \tag{A.5}$$

$$G_{vdvg\_OL} = \frac{D_d}{\left(1+s\frac{L}{R}+s^2LC\right)} \tag{A.6}$$

$$G_{vddd\_OL} = G_{vqdq\_OL} = \frac{V_g}{\left(1+s\frac{L}{R}+s^2LC\right)} \tag{A.7}$$

$$Z_{out\_dd\_OL} = Z_{out\_qq\_OL} = \frac{sL}{\left(1+s\frac{L}{R}+s^2LC\right)} \tag{A.8}$$

$$G_{iLddd} = G_{iLqdq} = \frac{V_g}{R}\frac{(1+sRC)}{\left(1+s\frac{L}{R}+s^2LC\right)} \tag{A.9}$$

$$G_{iLdid} = G_{iLqiq} = \frac{1}{\left(1+s\frac{L}{R}+s^2LC\right)} \tag{A.10}$$

$$G_{iLdvg} = G_{iLqvg} = \frac{D}{R}\frac{(1+sRC)}{\left(1+s\frac{L}{R}+s^2LC\right)} \tag{A.11}$$

APPENDIX B – THE EXTRA ELEMENT THEOREM

The Extra Element Theorem (EET) by R. D. Middlebrook [28] shows how any transfer function of interest is changed by the addition of an external impedance (the extra element) to a port of an electrical network, without solving the system all over again.

The linear network with an input u, an output y, and a port to be connected to an extra element is shown in Fig. B.1.

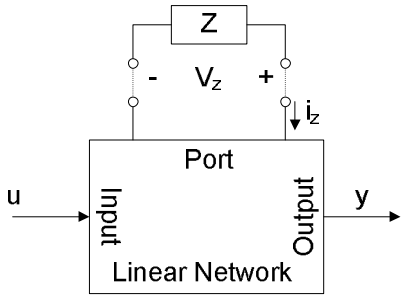


Figure B.1. Linear network with an input *u*, an output *y*, and a port to be connected to an extra element.

The current i_z is first considered as an input for the port. Using two-port network techniques, the linear network can be modeled as

$$\begin{cases} y = A_1 u + A_2 i_z \\ v_z = B_1 u + B_2 i_z \end{cases} \tag{B.1}$$

In (B.1), A_1 represents the original transfer function before the connection of the extra element *Z*. By connecting the impedance *Z* as an extra element to the original linear network, the input current of the port is

$$i_z = -\frac{v_z}{Z} \tag{B.2}$$

Substituting (B.2) into (B.1), the linear network model now is

$$\begin{cases} y = A_1 u - A_2 \dfrac{v_z}{Z} \\ v_z = B_1 u - B_2 \dfrac{v_z}{Z} \end{cases} \tag{B.3}$$

By eliminating v_z in (B.3) the equation is described as (B.4) where Z_n is the null double injection driving point impedance and Z_d is the single injection driving point impedance.

$$\frac{y}{u} = A_1 \frac{1 + \dfrac{1}{Z}\left(\dfrac{A_1 B_2 - A_2 B_1}{A_1}\right)}{1 + \dfrac{1}{Z} B_2} = A_1 \frac{1 + \dfrac{Z_n}{Z}}{1 + \dfrac{Z_d}{Z}} \tag{B.4}$$

To derive a dual form, the linear network model (B.1) is equivalently represented by setting v_z as input.

$$\begin{cases} y = A_1 u + A_2 v_z \\ i_z = B_1 u + B_2 v_z \end{cases} \tag{B.5}$$

Similarly by defining $v_z = -i_z Z$ and eliminating i_z, the linear network model in (B.4) is described in a dual form as (B.6), where Z_n and Z_d are reciprocal respectively to the Z_n and Z_d derived in (B.4).

$$\frac{y}{u} = A_1 \frac{1 + Z\left(\frac{A_1 B_2 - A_2 B_1}{A_1}\right)}{1 + ZB_2} = A_1 \frac{1 + \frac{Z}{Z_n}}{1 + \frac{Z}{Z_d}} \tag{B.6}$$

Considering the source subsystem as an extra element with output impedance Z_S, as an example, it is possible to find how the feedback loop gain is modified by the addition of Z_S. The feedback loop gain transfer function has $\hat{x}$ as input and $\hat{v}$ as output, as shown in Fig. 3.7. The linear network is modeled using the dual form, as follows

$$\begin{cases} \hat{v} = T_{VM\_FB}\hat{x} + A_2\hat{v}_z \\ \hat{i}_z = B_1\hat{x} + B_2\hat{v}_z \end{cases} \tag{B.7}$$

Since $\hat{i}_z$ and $\hat{v}_z$ can be identified as $\hat{i}_{in}$ and $\hat{v}_g$ in the g-parameter representation of the open-loop transfer function of the converter in (A.1), the unknown transfer functions in (B.7) are defined as follows

$$\begin{aligned} A_2 &= G_{vg\_OL} \\ B_1 &= G_{id\_OL} \\ B_2 &= \frac{1}{Z_{in\_OL}} \end{aligned} \tag{B.8}$$

The transfer functions Z_n and Z_d are calculated as

$$\begin{aligned} \frac{1}{Z_n} &= \frac{A_1 B_2 - A_2 B_1}{A_1} = \frac{1}{Z_{in\_OL}} - \frac{G_{id\_OL} G_{vg\_OL}}{G_{vd\_OL}} = \frac{1}{Z_{N\_vd\_OL}} \\ \frac{1}{Z_d} &= B_2 = \frac{1}{Z_{in\_OL}} \end{aligned} \tag{B.9}$$

Thus the modified transfer function by the correction factor in EET is obtained as

$$T_{VM\_FB\_ZS} = T_{VM\_FB} \frac{\left(1 + \frac{Z_S}{Z_{N\_vd\_OL}}\right)}{\left(1 + \frac{Z_S}{Z_{in\_OL}}\right)} \tag{B.10}$$

APPENDIX C – PFF CONTROL USING PBSC

This appendix shows the algebra to find M and $|Z_{damp}(j\omega_{c\_Zs\_FF})|$ from the expression $|T_{FB\_Zs\_FF}(j\omega_{c\_Zs\_FF})|=1$.

$$\left\|T_{FB\_Z_S\_FF}(j\omega_{c\_Zs\_FF})\right\|=1 \tag{C.1}$$

$$=\left\|T_{FB}(j\omega_{c\_Zs\_FF})\right\|\cdot\frac{\left\|1+\dfrac{Z_S(j\omega_{c\_Zs\_FF})}{Z_{N\_vd\_OL}(j\omega_{c\_Zs\_FF})}\right\|}{\left\|1+\dfrac{Z_S(j\omega_{c\_Zs\_FF})}{Z_{in\_OL}(j\omega_{c\_Zs\_FF})}\cdot\left(1+Z_{in\_OL}(j\omega_{c\_Zs\_FF})\cdot T_{FF}(j\omega_{c\_Zs\_FF})\right)\right\|} \tag{C.2}$$

$$=\left\|T_{FB}(j\omega_{c\_Zs\_FF})\right\|\cdot\frac{\left\|1+\dfrac{Z_S(j\omega_{c\_Zs\_FF})}{Z_{N\_vd\_OL}(j\omega_{c\_Zs\_FF})}\right\|}{\left\|1+\dfrac{Z_S(j\omega_{c\_Zs\_FF})}{Z_{in\_OL}(j\omega_{c\_Zs\_FF})}\cdot\left(1+Z_{in\_OL}(j\omega_{c\_Zs\_FF})\cdot\dfrac{1+T_{FB}(j\omega_{c\_Zs\_FF})}{Z_{damp}(j\omega_{c\_Zs\_FF})}\right)\right\|} \tag{C.3}$$

$$=\left\|T_{FB}(j\omega_{c\_Zs\_FF})\right\|\cdot\frac{\left\|1+\dfrac{Z_S(j\omega_{c\_Zs\_FF})}{Z_{N\_vd\_OL}(j\omega_{c\_Zs\_FF})}\right\|}{\left\|1+\dfrac{Z_S(j\omega_{c\_Zs\_FF})}{Z_{in\_OL}(j\omega_{c\_Zs\_FF})}+\dfrac{Z_S(j\omega_{c\_Zs\_FF})}{Z_{damp}(j\omega_{c\_Zs\_FF})}+\dfrac{Z_S(j\omega_{c\_Zs\_FF})}{Z_{damp}(j\omega_{c\_Zs\_FF})}\cdot T_{FB}(j\omega_{c\_Zs\_FF})\right\|} \tag{C.4}$$

Bringing $||Z_{damp}(j\omega_{c\_Zs\_FF})||$ on the left hand side of (C.4) and all the other terms to the right hand side, after some algebra, the inequality (C.8) is found.

$$\left\|T_{FB}(j\omega_{c\_Zs\_FF})\right\|\cdot\left\|1+\frac{Z_S(j\omega_{c\_Zs\_FF})}{Z_{N\_vd\_OL}(j\omega_{c\_Zs\_FF})}\right\|=\left\|1+\frac{Z_S(j\omega_{c\_Zs\_FF})}{Z_{in\_OL}(j\omega_{c\_Zs\_FF})}+\frac{Z_S(j\omega_{c\_Zs\_FF})}{Z_{damp}(j\omega_{c\_Zs\_FF})}+\frac{Z_S(j\omega_{c\_Zs\_FF})}{Z_{damp}(j\omega_{c\_Zs\_FF})}\cdot T_{FB}(j\omega_{c\_Zs\_FF})\right\| \tag{C.5}$$

$$\begin{aligned}&\left\|T_{FB}(j\omega_{c\_Zs\_FF})\right\|\cdot\left\|1+\frac{Z_S(j\omega_{c\_Zs\_FF})}{Z_{N\_vd\_OL}(j\omega_{c\_Zs\_FF})}\right\|\cdot\left\|Z_{in\_OL}(j\omega_{c\_Zs\_FF})\right\|\cdot\left\|Z_{damp}(j\omega_{c\_Zs\_FF})\right\|\\&=\left\|\begin{aligned}&Z_{in\_OL}(j\omega_{c\_Zs\_FF})\cdot Z_{damp}(j\omega_{c\_Zs\_FF})+Z_S(j\omega_{c\_Zs\_FF})\cdot Z_{damp}(j\omega_{c\_Zs\_FF})\\&+Z_S(j\omega_{c\_Zs\_FF})\cdot Z_{in\_OL}(j\omega_{c\_Zs\_FF})+Z_S(j\omega_{c\_Zs\_FF})\cdot Z_{in\_OL}(j\omega_{c\_Zs\_FF})\cdot T_{FB}(j\omega_{c\_Zs\_FF})\end{aligned}\right\|\\&\le\left\|Z_{damp}(j\omega_{c\_Zs\_FF})\cdot\left(Z_{in\_OL}(j\omega_{c\_Zs\_FF})+Z_S(j\omega_{c\_Zs\_FF})\right)\right\|+\left\|Z_S(j\omega_{c\_Zs\_FF})\cdot Z_{in\_OL}(j\omega_{c\_Zs\_FF})\cdot\left(1+T_{FB}(j\omega_{c\_Zs\_FF})\right)\right\|\end{aligned} \tag{C.6}$$

$$\left(\left\|T_{FB}(j\omega_{c\_Zs\_FF})\right\|\cdot\left\|1+\frac{Z_S(j\omega_{c\_Zs\_FF})}{Z_{N\_vd\_OL}(j\omega_{c\_Zs\_FF})}\right\|\cdot\left\|Z_{in\_OL}(j\omega_{c\_Zs\_FF})\right\|-\left\|Z_{in\_OL}(j\omega_{c\_Zs\_FF})+Z_S(j\omega_{c\_Zs\_FF})\right\|\right)\cdot\left\|Z_{damp}(j\omega_{c\_Zs\_FF})\right\| \quad \text{(C.7)}$$
$$\le\left\|Z_S(j\omega_{c\_Zs\_FF})\cdot Z_{in\_OL}(j\omega_{c\_Zs\_FF})\cdot\left(1+T_{FB}(j\omega_{c\_Zs\_FF})\right)\right\|$$

$$\left\|Z_{damp}(j\omega_{c\_Zs\_FF})\right\|\le \frac{\left\|Z_S(j\omega_{c\_Zs\_FF})\cdot Z_{in\_OL}(j\omega_{c\_Zs\_FF})\cdot\left(1+T_{FB}(j\omega_{c\_Zs\_FF})\right)\right\|}{\left\|T_{FB}(j\omega_{c\_Zs\_FF})\right\|\cdot\left\|1+\frac{Z_S(j\omega_{c\_Zs\_FF})}{Z_{N\_vd\_OL}(j\omega_{c\_Zs\_FF})}\right\|\cdot\left\|Z_{in\_OL}(j\omega_{c\_Zs\_FF})\right\|-\left\|Z_{in\_OL}(j\omega_{c\_Zs\_FF})+Z_S(j\omega_{c\_Zs\_FF})\right\|}\triangleq M \quad \text{(C.8)}$$

Two simplifications can be applied to the coefficient M if the following constraints hold:

$$\begin{aligned} &Approx.(1)\ \left\|Z_S(j\omega_{c\_Zs\_FF})\right\| << \left\|Z_{N\_vd\_OL}(j\omega_{c\_Zs\_FF})\right\| \\ &for\quad \left\|Z_{N\_vd\_OL}(j\omega_{c\_Zs\_FF})\right\| \ge \left\|Z_S(j\omega_{c\_Zs\_FF})\right\| + 20dB \end{aligned} \quad \text{(C.2)}$$

and

$$\begin{aligned} &Approx.(2)\ \left\|Z_S(j\omega_{c\_Zs\_FF})\right\| << \left\|Z_{in\_OL}(j\omega_{c\_Zs\_FF})\right\| \\ &for\quad \left\|Z_{in\_OL}(j\omega_{c\_Zs\_FF})\right\| \ge \left\|Z_S(j\omega_{c\_Zs\_FF})\right\| + 20dB \end{aligned} \quad \text{(C.3)}$$

The two approximations are valid only if $\omega_{c\_Zs\_FF}$ is chosen to be less than the frequency limits shown in Fig. C.1.

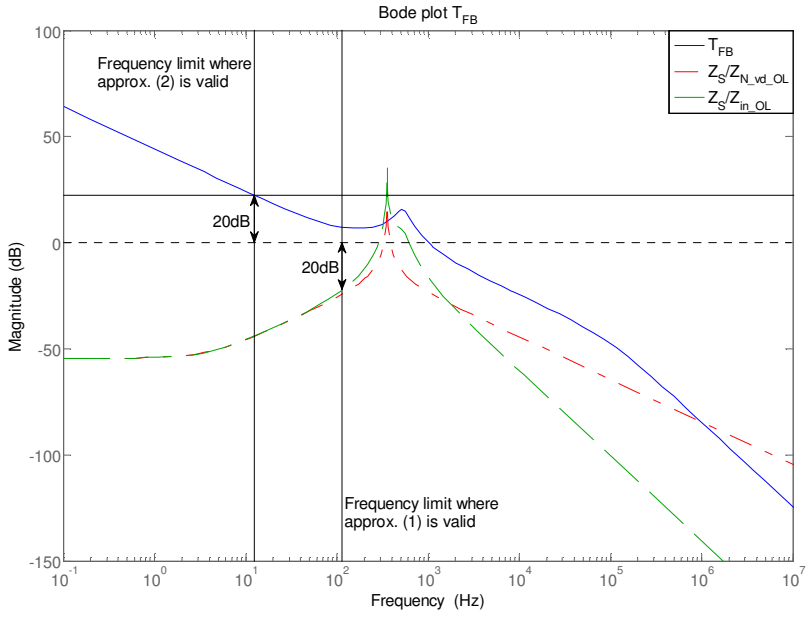


Figure C.1. Bode plot of T_{FB}, $Z_S/Z_{N\_vd\_OL}$ and Z_S/Z_{in_OL}.

APPENDIX D – THE LABORATORY DC POWER DISTRIBUTION SYSTEM

This appendix provides schematics and other technical details of the DC power distribution system built in the laboratory. A front picture of the rack which contains the system is shown in Fig. D.1.

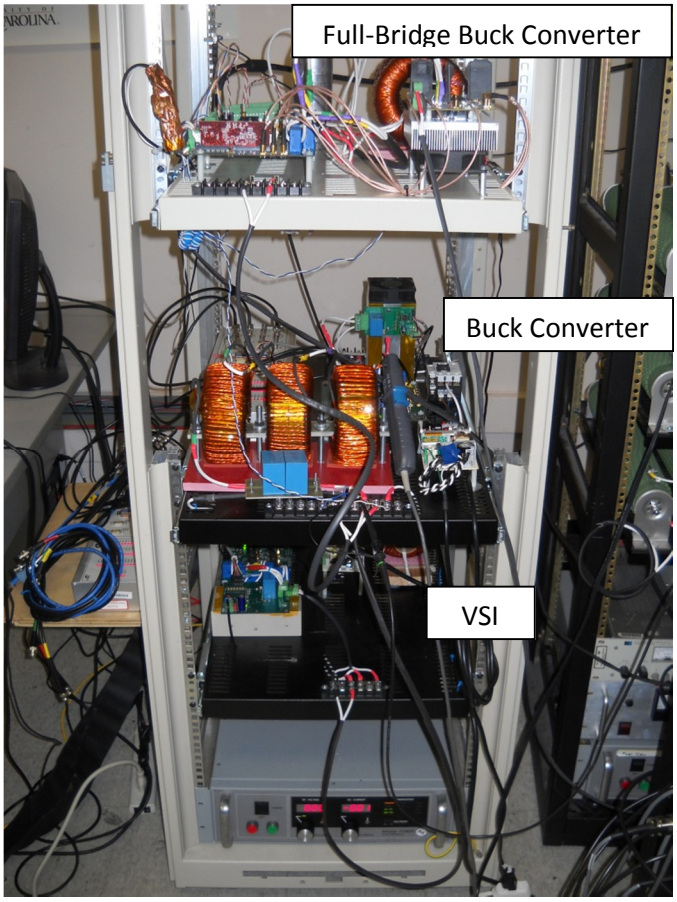


Figure D.1. Front picture of the laboratory DC power distribution system.

The buck converter and the VSI use a three-phase bridge 600V/20A Control Integrated Power System (CIPOS) IGCM30F60GA powered by Infineon with built-in gate

drive circuitry which enables a simple and flexible test setup. The output filter for the buck converter consists of the series of three inductors for a total inductance of *3.3mH* and a *50μF* capacitor in parallel with the VSI input capacitance of *12μF*. The buck converter is fed by *200V* DC source (a Magna Power supply) and VSI is fed from the buck converter at *100V* DC. The VSI feeds a balanced three-phase passive load *R=10*Ω through a balanced three-phase LC filter with *L=1mH* and *C=90 μF*. The schematics of the buck converter and the VSI are shown in Figs. D.2 and D.3. Printed circuit boards (PCBs) for the Infineon IGBT power module were developed, for which two versions are shown in Fig. D.4.

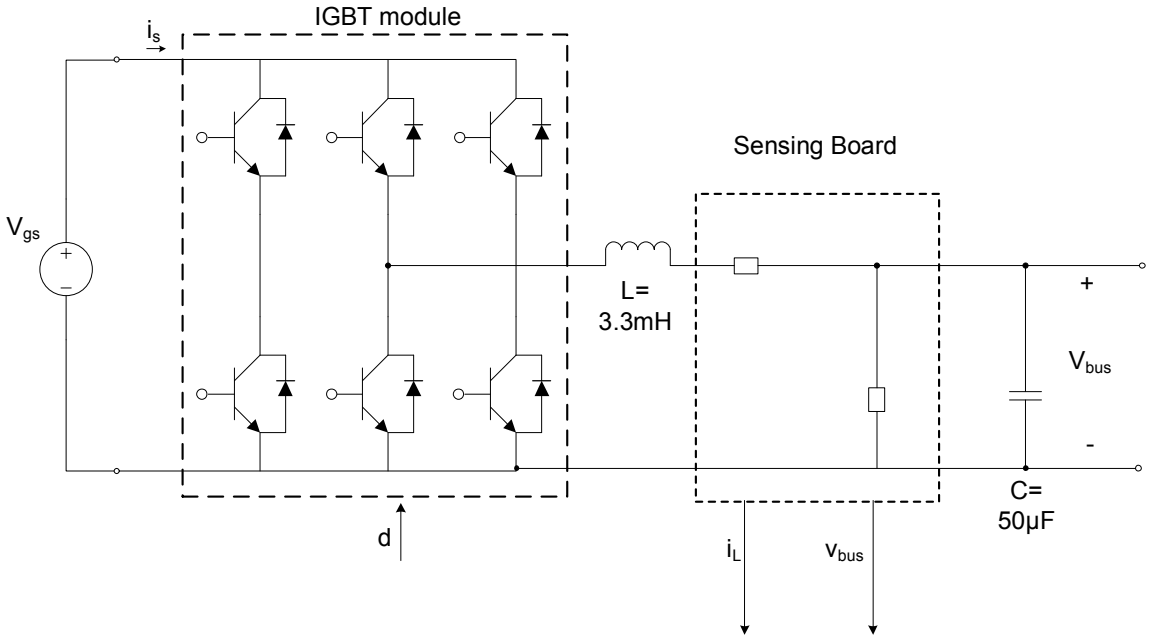


Figure D.2. Schematic of the buck converter.

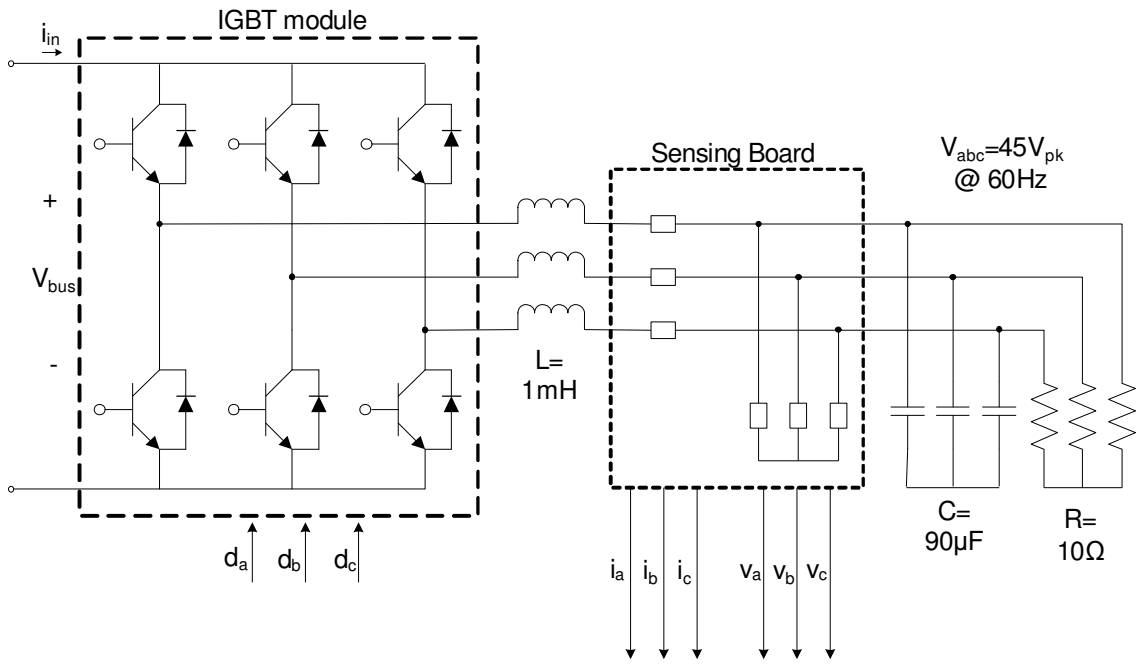


Figure D.3. Schematic of the VSI.

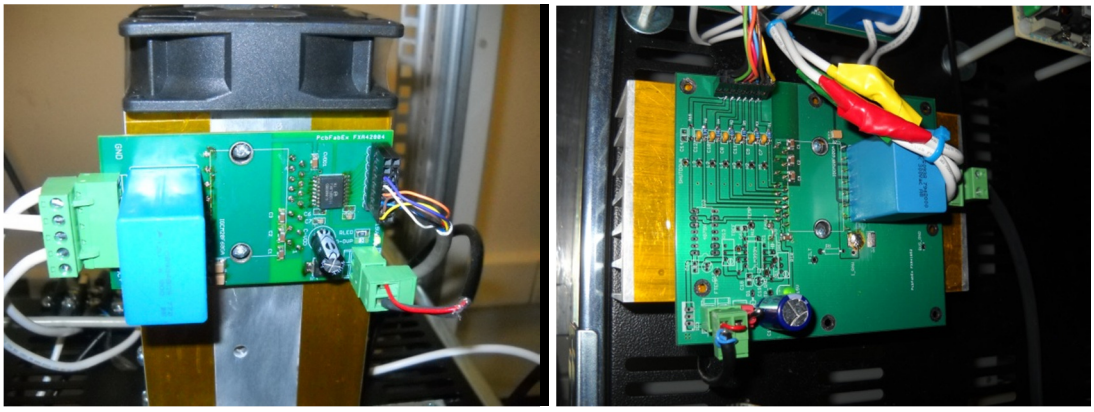


Figure D.4. Pictures of the PCBs with the Infineon IGBT power module: on the left the new version, and on the right the old version.

The full-bridge buck converter, used for PRBS injection, utilizes a Microsemi APTGT50X60T3G 600V 50A IGBT 6-Pack. Modular isolated gate drivers were also used to decrease any common mode noise that would otherwise be fed back into the controller. The chosen switching frequency is 12 kHz under unipolar modulation which yields an inductor current ripple at 24 kHz. The schematic of the full-bridge buck

converter is shown in Figs. D.5. The PCB which contains the Microsemi IGBT 6-pack was developed, shown in Fig. D.6.

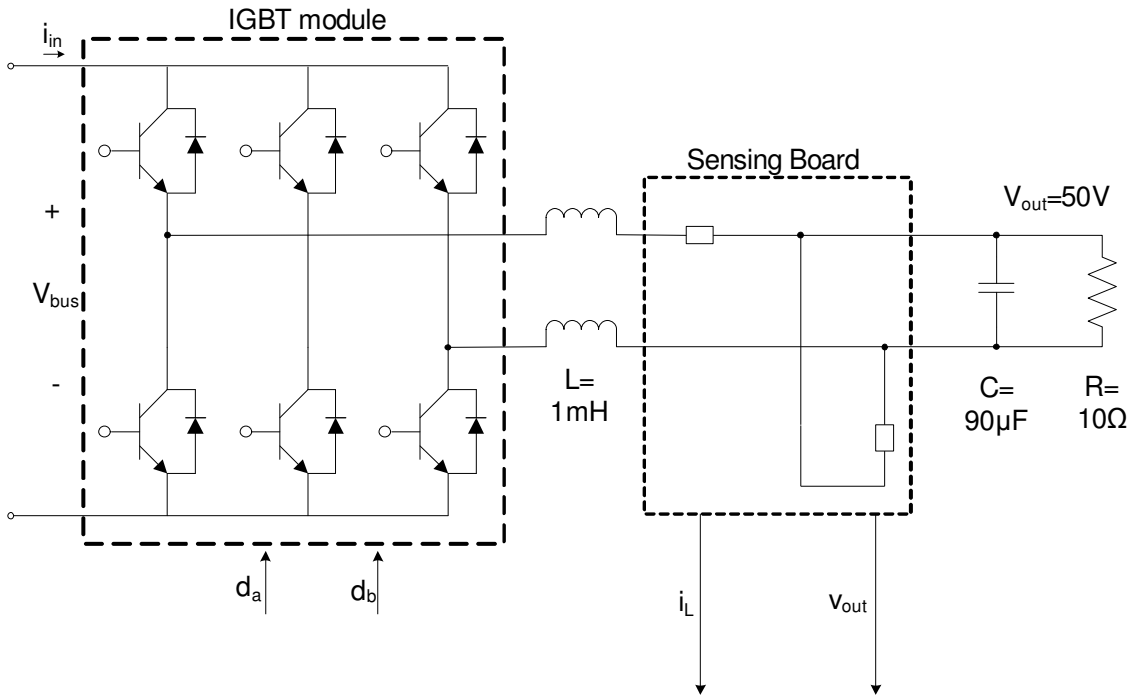


Figure D.5. Schematic of the full-bridge buck converter.

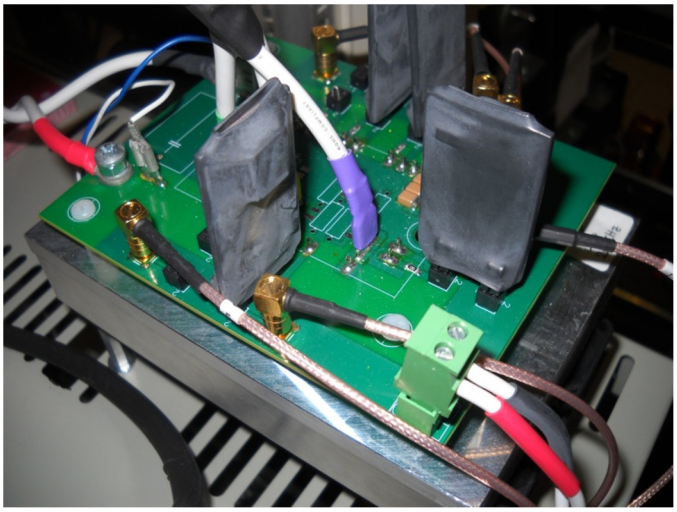


Figure D.6. Pictures of the PCBs with the Microsemi IGBT 6-pack.

The last PCB implemented for the laboratory DC power distribution system is the sensing board. The sensing board is capable of sensing 4 currents (max 25 A) and 4 differential voltages (max 600 V), analog signal processing with high SNR, and possibility of using dSPACE DS1104 or TI TMS320F28335 as control system. Two versions of the sensing board, shown in Fig. D.7, have developed so far.

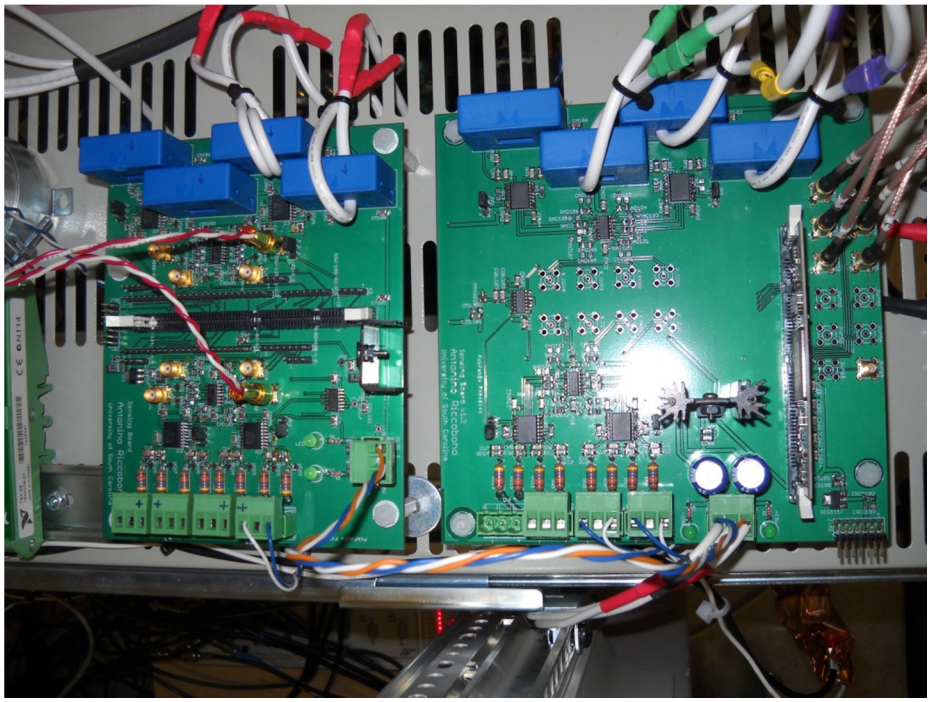


Figure D.7. Pictures of the sensing boards: on the left the old version, and on the right the new version.

APPENDIX E – PASSIVITY FOR N-PORT NETWORK

This appendix provides mathematical definitions for the passivity of a n-port electrical network. This analysis is based on [59]. In the time domain, an n-port network is passive if and only if $\int_{-\infty}^{T} \boldsymbol{i}'(t)\boldsymbol{v_{bus}}(t)dt \geq 0$ for all T. For the following analysis, since the time-domain condition is hard to check, a passivity concept will be developed in the frequency domain. The bus voltages and injected currents can be expressed as the real part of complex quantities in the following form

$$\boldsymbol{i}(t) = \boldsymbol{I}e^{\sigma t}\cos(\omega t) = Re[\boldsymbol{I}e^{st}] \tag{E.1}$$

$$\boldsymbol{v_{bus}}(t) = \boldsymbol{V_{bus}}e^{\sigma t}\cos(\omega t + \varphi) = Re\left[\boldsymbol{V_{bus}}e^{st+j\varphi}\right] \tag{E.2}$$

where $s = \sigma + j\omega$ and both $\boldsymbol{I}$ and $\boldsymbol{V_{bus}}$ are real quantities. According to the passivity definition, the energy delivered to the n-port network must be non-negative at any time T, as follows

$$\int_{-\infty}^{T} \boldsymbol{i}'(t)\boldsymbol{v_{bus}}(t)dt = \tag{E.3}$$

$$= \int_{-\infty}^{T} \boldsymbol{I}'\boldsymbol{V_{bus}}e^{2\sigma t}\cos(\omega t)\cos(\omega t + \varphi)dt \tag{E.4}$$

$$= \frac{1}{4\sigma}\boldsymbol{I}'\boldsymbol{V_{bus}}e^{2\sigma t}\cos(\varphi) \geq 0 \tag{E.5}$$

For the more general case of $\boldsymbol{i}(t)$ and $\boldsymbol{v_{bus}}(t)$ complex quantities, from the definition of passivity we can write

$$Re\left[\int_{-\infty}^{T} \boldsymbol{i}^{H}(t)\boldsymbol{v_{bus}}(t)dt\right] = \tag{E.6}$$

$$= Re\left[\int_{-\infty}^{T} \boldsymbol{I}'e^{s^{*}t}\boldsymbol{V_{bus}}e^{st+j\varphi}dt\right] = \tag{E.7}$$

$$= \frac{1}{2\sigma}\boldsymbol{I}'\boldsymbol{V_{bus}}e^{2\sigma t}\cos(\varphi) \geq 0 \tag{E.8}$$

where the symbols * and ^{H} indicate complex conjugate and Hermitian (complex conjugate transpose) operators, respectively. Comparing (E.8) with (E.5) reveals that, besides a factor of 2, the two equations provide identical passivity results.

The powerfulness of the complex variable analysis is that it allows to assess passivity of an n-port electrical network in terms of properties of the driving point impedance matrix $\boldsymbol{Z_{bus}}$, as previously defined (5.1). Thus, passivity can be investigated for injected currents and bus voltages of the following form

$$\boldsymbol{i}(t) = \boldsymbol{I}e^{st} \tag{E.9}$$

$$\boldsymbol{v_{bus}}(t) = \boldsymbol{Z_{bus}}(s)\boldsymbol{I}e^{st} \tag{E.10}$$

Using the passivity definition in (E.6) and its result in (E.8), it is possible to write

$$Re\left[\int_{-\infty}^{T} \boldsymbol{I}^{H}\boldsymbol{Z_{bus}}(s)\boldsymbol{I}e^{2\sigma t}dt\right] = \tag{E.11}$$

$$= \frac{1}{2\sigma}Re[\boldsymbol{I}^{H}\boldsymbol{Z_{bus}}(s)\boldsymbol{I}]e^{2\sigma t} \geq 0 \tag{E.12}$$

For all $\boldsymbol{I}$, and $\sigma \geq 0$, (E.12) leads to

$$Re[\boldsymbol{I}^{H}\boldsymbol{Z_{bus}}(s)\boldsymbol{I}] \geq 0 \tag{E.13}$$

which can be written as follows:

$$\frac{1}{2}\{[\boldsymbol{I}^H \boldsymbol{Z_{bus}}(s)\boldsymbol{I}] + [\boldsymbol{I}^H \boldsymbol{Z_{bus}}(s)\boldsymbol{I}]^H\} \geq 0 \tag{E.14}$$

$$\boldsymbol{I}^H[\boldsymbol{Z_{bus}}(s) + \boldsymbol{Z_{bus}}(s)^H]\boldsymbol{I} \geq 0 \tag{E.15}$$

The condition in (E.15) is satisfied if the matrix $\boldsymbol{Z_{bus}}(s) + \boldsymbol{Z_{bus}}(s)^H$ is not negative definite for $\sigma > 0$. Thus, similarly for the 1-port case, an equivalent passivity condition for an n-port network can be stated [56]. An n-port electrical network is passive if and only if

1. $\boldsymbol{Z_{bus}}(s)$ has no poles in the RHP,
2. The Nyquist plot of the *n* upper left determinants of $\boldsymbol{Z_{bus}}(j\omega) + \boldsymbol{Z_{bus}}(j\omega)^H$ lie in the RHP.