EXPERIMENTAL AND THEORETICAL STUDY OF ON-CHIP BACK-END-OF-LINE (BEOL) STACK FRACTURE DURING FLIP-CHIP REFLOW ASSEMBLY

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EXPERIMENTAL AND THEORETICAL STUDY OF ON-CHIP BACK-END-OF-LINE (BEOL) STACK FRACTURE DURING FLIP-CHIP REFLOW ASSEMBLY

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To my wife

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SUMMARY

With continued feature size reduction in microelectronics and with more than a billion transistors on a single integrated circuit (IC), on-chip interconnection has become a challenge in terms of processing-, electrical-, thermal-, and mechanical perspective. Today's high-performance ICs have on-chip back-end-of-line (BEOL) layers that consist of copper traces and vias interspersed with low-*k* dielectric materials. These layers have thicknesses in the range of 100 nm near the transistors and 1000 nm away from the transistors and near the solder bumps. In such BEOL layered stacks, cracking and/or delamination is a common failure mode due to the low mechanical and adhesive strength of the dielectric materials as well as due to high thermally-induced stresses.

This work focuses on developing a framework based on cohesive zone modeling approach to study interfacial delamination in sub-micron thick BEOL stack layers. Such a framework is then successfully applied to predict microelectronic device reliability. As intentionally creating pre-fabricated cracks in such interfaces is difficult, this work examines a combination of four-point bend and double-cantilever beam tests to create initial cracks and to develop cohesive zone parameters over a range of mode-mixity. Similarly, a combination of four-point bend and end-notch flexure tests is used to cover additional range of mode-mixity. In these tests, silicon wafers obtained from a wafer foundry are used for experimental characterization. The developed parameters are then used in actual microelectronic device FE simulations to predict the initiation and propagation of a crack, and the results from such predictions are successfully validated with experimental data. In addition, a nanoindenter-based shear test technique designed specifically for this study is demonstrated. The new test technique can address different mode-mixities compared to other interfacial fracture characterization tests. The nano-indenter based bump shear test technique is sensitive to capture the change in fracture parameter due to changes in local trace pattern variations around the vicinity of a solder bump and the test mimics the forces experienced by the bump during flip-chip assembly reflow process. Through this experimental and theoretical modeling research, guidelines are also developed to improve the reliability of current and future-generation microelectronic devices.

CHAPTER 1

INTRODUCTION

The microelectronic revolution started with the invention of transistors in 1949. It took 10 years to develop the first electronic circuit integrating two transistors and a resistor by Jack Kilby [1]. Thus the term integrated circuit (IC) is defined as a micro-device that integrates active (transistors) and passive (resistors, capacitors, inductors) components into an electronic circuit to perform a specific task. In 1965 Gordon Moore predicted that the number of circuits on a silicon chip would keep doubling every 18-24 months [2]. Advances in nano-fabrication and lithography techniques have enabled the IC fabrication industry to hold-on to the trend predicted by Moore till date, as shown in Figure 1-1. Figure 1-1 presents data obtained from Intel, similar trends can be found for most of the IC manufacturers.

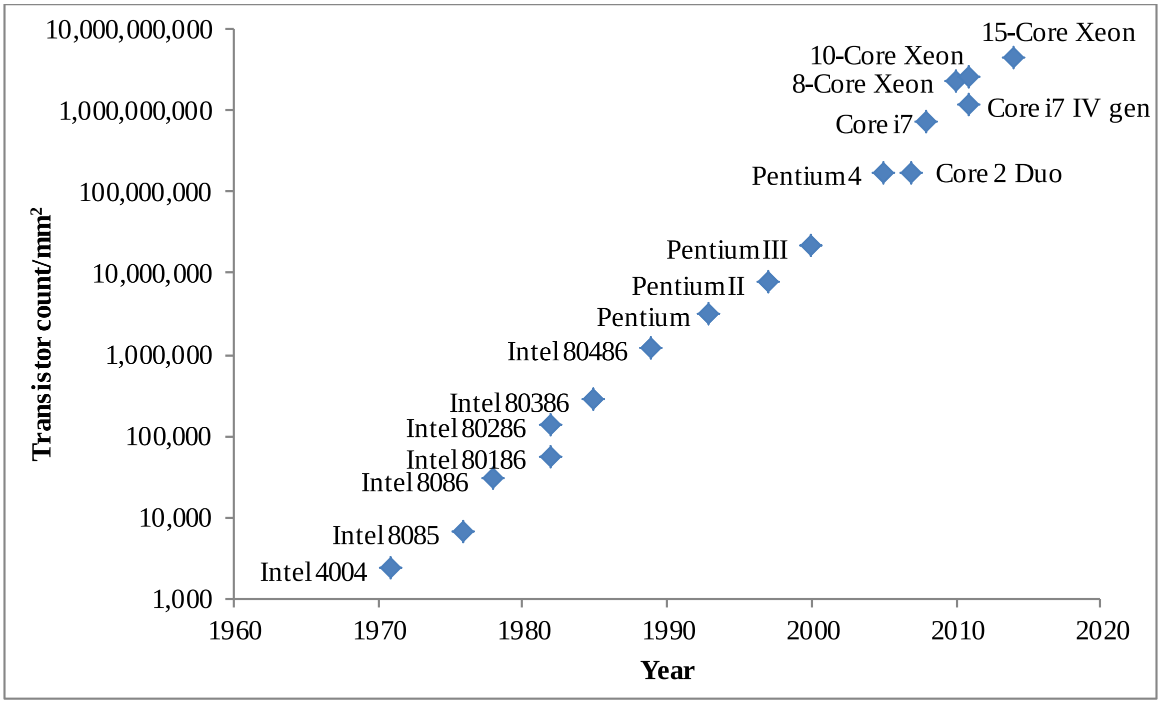


Figure 1-1. Moore's Law (Data Source: Intel Corp.)

Microelectronics industry is rapidly moving towards consistently building more than four billion transistors on 512 mm^2 silicon die. To transmit signals and to build logic circuits multiple layers of wiring are fabricated on top of the transistors. The metallization layers are insulated using interlayer dielectric (ILD) layers and the metallization layers along with the insulation is called back end of line stack (BEOL). A focused ion beam (FIB) cross-section of BEOL stack imaged using scanning electron microscope (SEM) is shown in Figure 1-2. It can be seen that the layers close to the Silicon die/chip are thinner than the layers away from the die. The terms die and chip are interchangeably used in this document. In other words, layers close to the die are tightly packed than the layers away from the die. The BEOL stack acts as a means for establishing communication between transistors, supply power to transistors and transmit signals from transistors to external circuitry. Thus, the electrical performance of these chips is directly impacted by the RC delay or time constants (R – resistance; C – capacitance) of the signal transmission lines in the BEOL stack.

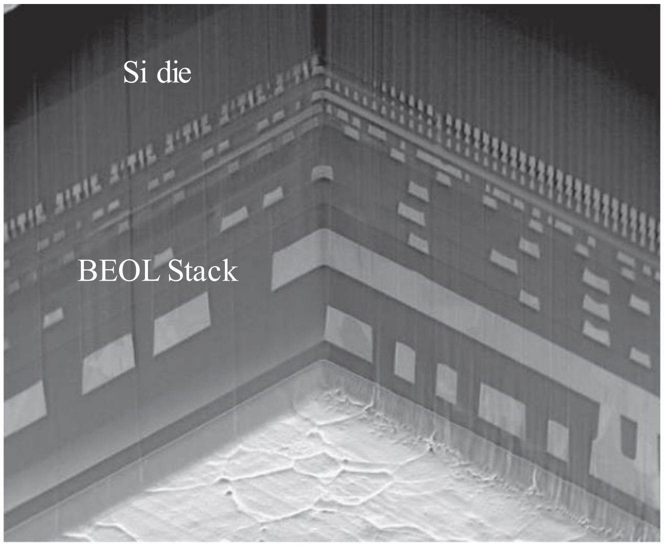


Figure 1-2: BEOL stack - thickness of the ILD layers are typically range from few 100s of nm near transistors and few µm close to the bump

Traditionally, aluminum (Al) is used for patterning the metal traces present in the BEOL stack insulated by silicon dioxide (SiO_2) ILD layers. Al has a resistivity of 3.3 μΩ-cm, and the dielectric constant (κ) of SiO_2 is 4.0 [3]. On the other hand, copper (Cu) has a resistivity of 1.6 μΩ-cm. In order to reduce the RC time constants and thus enhance the electrical performance Cu/low-κ dielectrics replaced Al/SiO_2 dielectrics in BEOL stack in late ‘90s [4]. The international technology roadmap for semiconductors (ITRS) predicts that the trend in lowering the effective dielectric constant (κ) of the ILD layers would scale down linearly in coming years. Proposed fabrication solutions to further reduce κ include introduction of air gaps in the dielectric layers by non-conformal deposition e.g.,[5] or removal of sacrificial materials after multi-level interconnects [6, 7]. Currently, materials that have dielectric constants as low as 2.55 are used as ILD layers. Although, the reduction in κ by introduction of pores improves the electrical performance, it also results in reduction of the of the modulus of these layers [8, 9]. The low-κ films have a modulus of less than 10 GPa compared to SiO_2 modulus of 70 GPa. Furthermore, the nano-sized pores not only lower the modulus of the dielectric material but also act as stress raisers resulting in lower fracture toughness. Therefore, when such a die is packaged in an electronic device several reliability challenges arise. This work focuses on thermo-mechanical reliability of microelectronic packages.

1.1 MICROELECTRONIC PACKAGING

The role of microelectronic packaging is to act as a bridge that interconnects several individual active devices and other system level passive devices to create functional electronic device. Therefore, a package needs to provide electrical connectivity, mechanical support, efficient thermal management and environmental protection for the components present in it. Furthermore, packages also facilitate I/O redistribution to establish communication between nano-scale transistors and macro-scale human-interaction systems like keypad, mouse, touch-screens. Such large scale redistribution is done in three levels as illustrated in Figure 1-3. First-level packaging acts as an IC carrier. The first-level packaging facilitates powering, cooling and protecting the ICs. Also, first-level packaging should enable interconnection to the second-level. The packaged ICs and the system level passive components are assembled on a printed wiring board in the second-level packaging. Several such individual system level modules are assembled on a motherboard or a backplane with the ability to communicate with the human interaction devices contribute to the third-level of packaging. Complex systems may involve more than three levels.

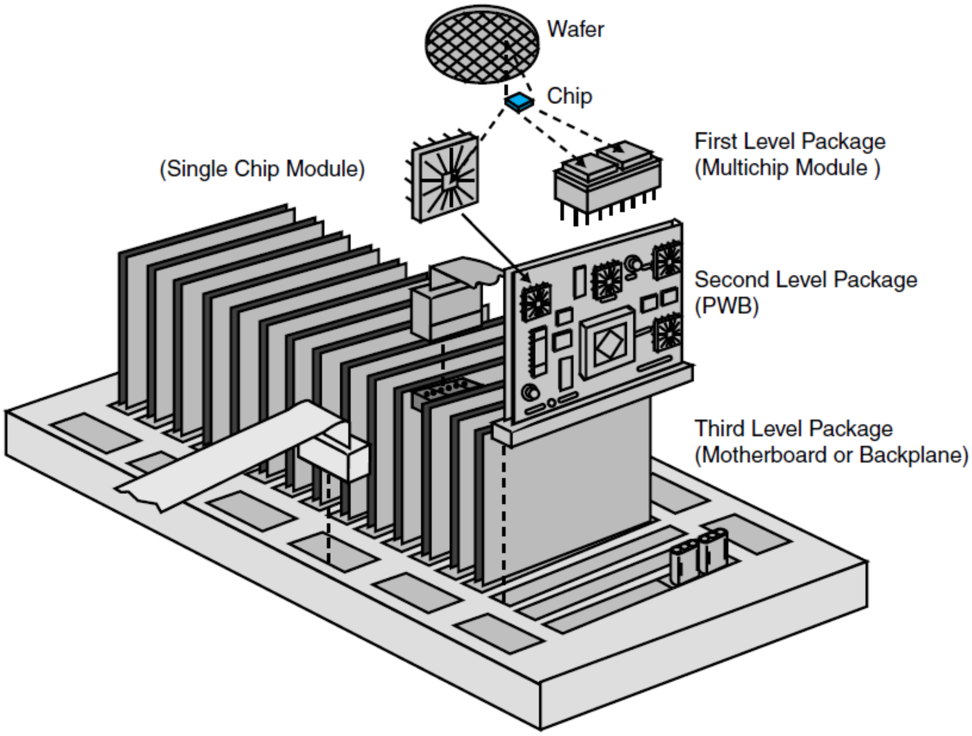


Figure 1-3. Levels of packaging [10]

The objective of this work is to improve the thermo-mechanical reliability of the first-level package (single chip module) shown in Figure 1-3. The fundamental components of a first-level package are the IC (die), substrate, and interconnect that connects the I/O pads on the IC to first-level package. The major first-level packaging technologies are wire-bonding, tape automated bonding (TAB) and flip-chip bonding. Although, there are specific advantages and disadvantages of each technology, advanced ICs adopt flip-chip technology as it facilitates area-array interconnection to the substrate. In wire-bonding and TAB, interconnects are present only along the periphery. Some of the advantages offered by flip-chip technology compared to other packaging technologies are high I/O density, better electrical performance, self-alignment, smaller footprint, and better heat dissipation through the back of the die. These merits have rendered the flip-chip technology as an enabling technology for future package development that includes multi-chip module (MCM), high-frequency communications, high-performance computers, portable electronics and fiber-optic assemblies.

1.2 FLIP-CHIP TECHNOLOGY

The rapid progress in miniaturization and large scale functional integration led to innovative high density area array interconnection technologies. In the flip-chip technology, the active device side of the silicon faces down and is interconnected to multilayered substrate using solder bumps. Various stages involved in flip-chip interconnection are graphically described in Figure 1-4. At the wafer level, solder bumps are electro-plated on copper or aluminum I/O pads present on the die. Next, the solder is reflown by heating the wafer above the solder melting temperature. The individual dies are diced from the wafer after it is cooled-down to room temperature. At the assembly house, each die is picked and aligned on top of substrate pads. The substrate is fluxed to create an inert atmosphere at high temperature preventing the oxidation of I/O pads and to improve the wettability of solder bumps on the pads. In some cases, force is applied to the backside of the die to ensure bump connectivity. However, high bonding forces may squish the solder and result in solder-bridging or crack the die passivation. The assembly is then taken through a multi-zone solder reflow oven on a conveyor to form the interconnection. The conveyor speed is precisely controlled so that the assembly is heated and cooled gradually to avoid thermal shock induced stresses and control the metallurgy of the solder bumps. Finally, underfill is dispensed between the die and substrate. Underfill is an epoxy based polymer with fillers to engineer the properties and thus improve the solder bump reliability. After dispensing the underfill, it is cured at high temperature. Such an assembly is often referred to as organic lead-free flip-chip package or simply flip-chip package.

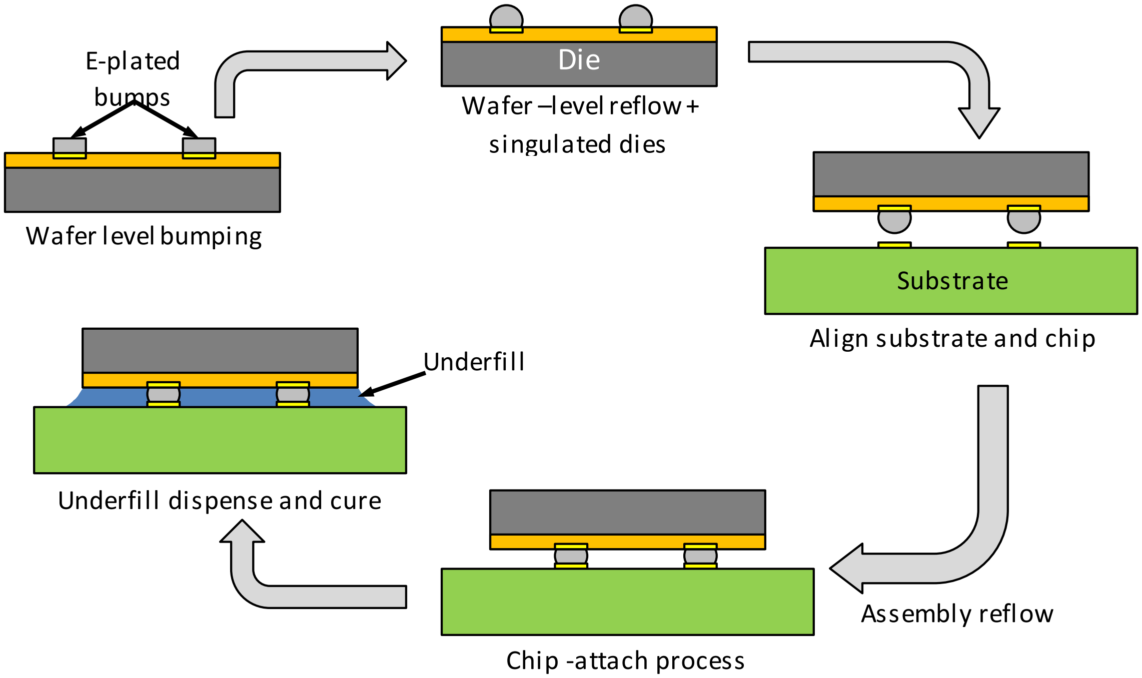


Figure 1-4. Flip-chip process flow for lead-free solder interconnects

1.2.1 Flip-Chip Reliability

Microelectronic device technology is specified by the length of the gate-oxide channel in the transistor. For example, Intel Core i- series of processors belong to 22 nm technology. As the technology progresses, the size of the gate-oxide channel in transistor are being reduced, meaning more transistors are packed on same surface area of silicon. Consequently, more number of layers are built on the BEOL stack. An ILD material present in the BEOL stack passes through several processes during fabrication of IC devices like dual-damascene lithography, etching, stripping, plasma-based cleaning processes, chemical mechanical polishing (CMP), etc. When such a die is assembled on a substrate, it is not unreasonable to expect every known-good-die (KGD) to pass assembly and qualification. Thus, assembly or packaging becomes a critical stage in microelectronic device life cycle. Some of the common assembly related failures are die cracking, low-κ dielectric cracking, and bump cracking.

1.2.2 Flip-Chip Thermo-Mechanical Reliability Challenges

Higher performance to cost ratio offered by the organic substrates compared to the ceramic or silicon substrates has led to the increased usage of organic substrates in flip-chip packages. Current day organic substrates include multiple layers of metallization insulated using build-up dielectric built symmetrically around a thick core material like BT (bismaleimide-triazine) or FR4, as shown in Figure 1-5. When the substrate is assembled with a silicon die and cooled-down from solder reflow temperature to room temperature, the assembly warps as shown schematically in Figure 1-5. The flip-chip assembly warps due to the difference in coefficient of thermal expansion (CTE) between the silicon die and the organic substrate. This introduces large peeling stresses on the corner solder balls of the flip-chip assembly, shown schematically in Figure 1-6.

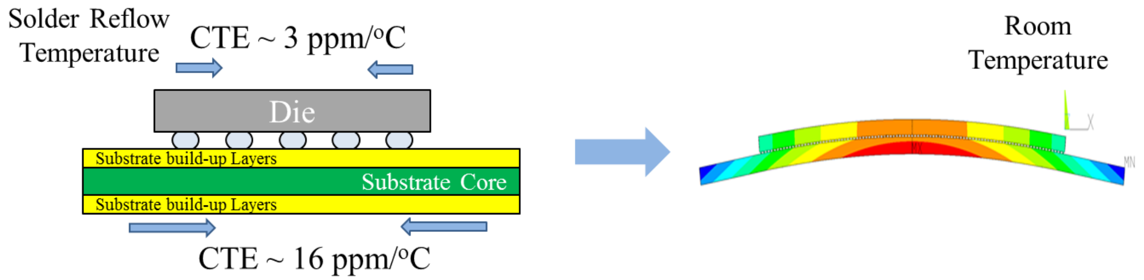


Figure 1-5. Assembly warpage at the end of chip-attach process

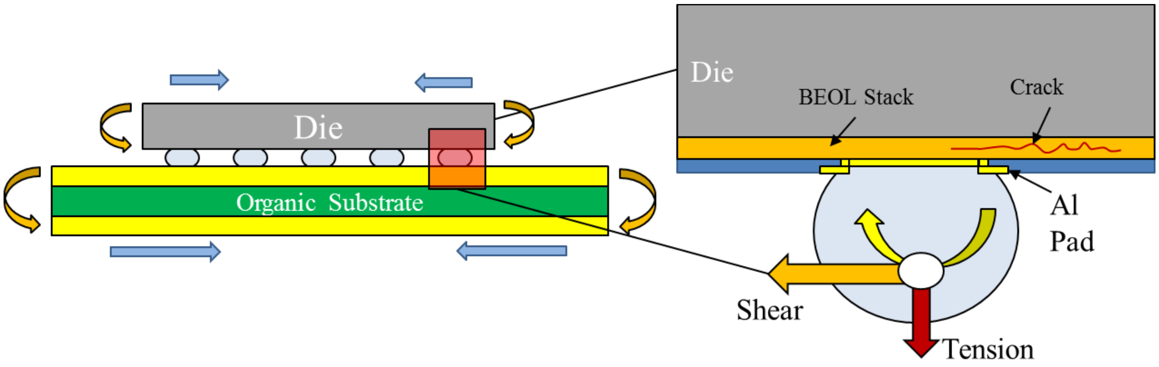


Figure 1-6. Schematic of stresses experienced by solder bump during chip-attach

Environmental regulations led to the introduction of lead-free solders in flip-chip packages. Lead-free solders, apart from being environmentally friendly, have higher current carrying capability [11]. However, they pose significant challenges from mechanical reliability standpoint due to higher stiffness and higher melting point than their leaded counterparts [11].

Introduction of low-κ ILD layers, increased die sizes, reduced die pad pitch, CTE mismatch between die and substrate, and the use of lead-free solder as interconnects would directly translate to reduction in reliability of IC assemblies due to low-κ ILD layer cracking. These cracks are predominantly observed above the solder bumps along the edge because bumps along the edge experience higher stress due to CTE mismatch compared to bumps near the center [12, 13]. Typical ILD crack above a solder bump is shown in Figure 1-7. These cracks appear as a white spot in C-mode scanning acoustic microscopic (CSAM) images as seen in Figure 1-8, thus they are often referred to as white-bumps or ghost-bumps. There is a need for better experimental methodologies and numerical modeling capabilities to successfully characterize the observed fracture and thus to improve future yield.

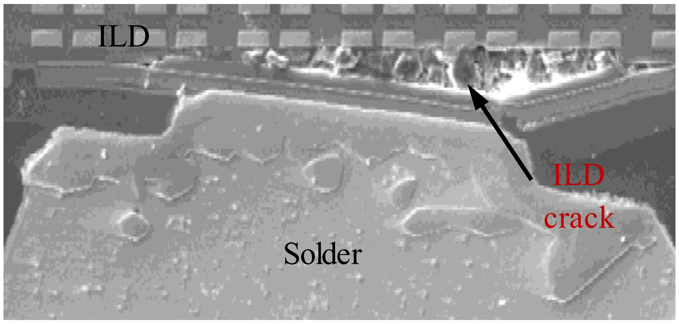


Figure 1-7. ILD crack above solder bump [12]

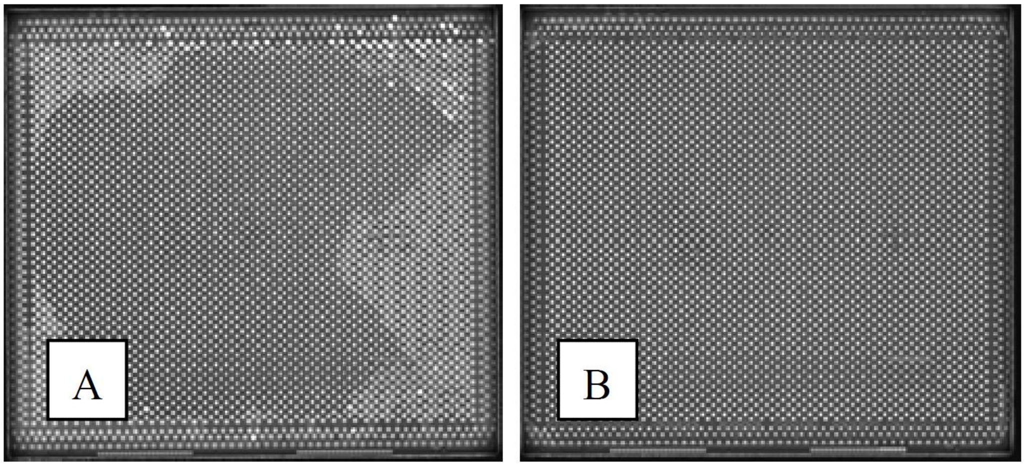


Figure 1-8. CSAM image showing white-bumps. A) white-bumps are observed around the corner. B) No white-bumps observed [13]

1.3 BACKGROUND

This research presents a systematic approach to predict white-bump failures observed at the end of flip-chip chip-attach process using cohesive zone modeling (CZM) technique. CZM is phenomenological approach therefore mixed-mode fracture strength of the critical layer present in BEOL stack needs to be determined. It has to be pointed out that the developed methodology can be extended to study any fracture process and is not restricted to microelectronic device failure alone.

Four-point bend (FPB) test e.g.[14, 15], double cantilever bend (DCB) test e.g.[16, 17] and nano-indentation e.g.[18, 19] have been used extensively to characterize the adhesive fracture toughness of Cu/low-κ structures. Apart from these methods novel non-contact type techniques like the magnetic actuation test for interfacial strength measurement [20] and the stress engineered “superlayer” technique [21] for cohesive strength measurement can be employed. The FPB test technique has been used to investigate the adhesive energies of Cu and various low-κ materials deposited using different processes extensively in [22].

The FPB, DCB, and end notch flexure (ENF) tests are typically used to determine critical energy release rate or interfacial fracture toughness (G_c) at different mode-mixities (Ψ). For such tests, it is possible to create starter cracks for layers that are few microns thick or for samples which are fabricated in-house. However, it is not readily possible to create starter cracks in layers that are sub-micron thick or where the samples are created through industry-based wafer fab cleanrooms. Also, in larger samples, optical and other techniques can be used to measure in-situ crack length as the interfacial delamination propagates. Such an in-situ measurement is often difficult when the layers are sub-micron in thickness. Also, CZM needs other parameters beyond such fracture parameters, including maximum traction, separation, and shape of traction-separation curve for different mode-mixities. Therefore in this work, the objectives of FPB, DCB, and ENF go beyond obtaining G_c and Ψ. Thus, this research presents an approach to identify the weakest layer present in sub-micron scale thin-film stack, create starter cracks along the critical layer, determine crack length through compliance calculations, and extract mixed-mode traction-separation curves from load-displacement curves of interfacial fracture characterization experiments.

Although the current interfacial fracture experiments are reliable, extensive sample preparation steps and care during sample preparation are imperative to get repeatable results. Also, sample size and the crack lengths are much larger than the failures in real devices. For example, largest white-bumps span a length of approximately 90 µm whereas the samples used for the bend test experiments and the crack lengths measured are at the order of tens of mm. Such a test is insensitive to vias/trace pattern changes around a solder bump. Therefore, a new test technique to determine the fracture strength of thin-film stack is developed. Such a technique is sensitive to variation in fracture parameter across an interface. Since, the test damages only one bump, a single sample can yield hundreds of samples and very minimal processing is required. Also, the results from the test can be directly compared with finite-element results without the need for complicated post-processing.

CHAPTER 2

LITERATURE REVIEW

2.1 INTRODUCTION

Modern microelectronic flip-chip packages are an assembly of multilayered die and multilayered substrate interconnected using viscoplastic solder material. One of the common critical failure modes experienced by such a complex assembly is delamination. Delamination occurs due to structural material properties of individual components assembled together and loading conditions that it is subjected during assembly. As mentioned in Chapter 1, the thermo-mechanical stresses that arise during flip-chip assembly due to CTE mismatch between the die and substrate. The stresses can be high enough to cause delamination in the ILD layers present in the die. Predicting such a failure calls for systematic study using various available techniques.

2.2 STRESS BASED APPROACHES

Over the past several decades extensive analytical and numerical approaches have been developed to study stresses along an interface. Classical laminate theory is applicable for predicting nominal stresses in thin laminates. Stress singularities can be considered by methods described by Suhir [23, 24]. Although analytical models offer quick results for simple problems, it is complicated to derive analytical expressions considering material nonlinearities, geometric nonlinearities over a wide range of sequential loading conditions. It also goes without saying that a general solution covering a large solution space is difficult or nearly impossible to obtain using analytical methods. On the other hand, numerical models handle all the above said difficulties without the need for rethinking the solution process from scratch. Finite-element approach is one of the well-established numerical techniques to study interfacial crack.

Morgan (1991) [25] demonstrated the use of finite-element models to study to thermal stresses in layered assemblies bonded with solder. Validity of 2D modeling assumptions to determine interfacial stresses in the layers at the end of monotonic thermal cool-down from 280 °C to 27 °C for linear-elastic and non-linear analyses. Morgan showed that more than three linear elements are required in each layer to capture bending accurately in 3D as well as 2D models. He also showed that linear-elastic 2D plane-strain models could capture stresses along the length of the assembly but could not capture the corner stresses and out-of-plane edge effects. He further argued that 2D plane-strain or plane-stress assumptions cannot capture the stresses acting along a layer when viscoplastic effects of solder are considered in modeling. This is because all stress components contribute towards calculating von Mises stress required for determining the flow potentials. In order to overcome the difficulty, Morgan used generalized plane-strain assumption, wherein the out-of-plane strain is assumed to be non-zero constant computed as a solution variable. He found that using such an assumption, the in-plane stresses could be captured accurately and the variation in corner stresses is within 5% compared to 3D models even when material nonlinearities are considered. Very good correlation between finite-element approach and exact solutions has been demonstrated by various authors for stress contours under single step and simple multilayered configurations without complex features e.g., [26-28] [29, 30].

Traditionally, researchers have studied delamination problems in multilayered structures using stress based approach by comparing the interfacial stress with adhesive bond strength [31, 32]. Typical failure criterion for this approach is,

$$\left(\frac{\sigma_{yy}}{\sigma_{yy,u}}\right)^2 + \left(\frac{\sigma_{xy}}{\sigma_{xy,u}}\right)^2 \geq 1 \tag{2-1}$$

where σ_{yy}, σ_{xy} are the calculated maximum peeling and shear stresses at the interface and $\sigma_{yy,u}$, $\sigma_{xy,u}$ are peeling and shear bonding strengths. Well-known disadvantage of this technique is the complexity involved in handling singularities that arise at the multi-material wedges, stress concentration features in bulk material, or defects along the interface.

2.3 FRACTURE MECHANICS APPROACH

In order to overcome the difficulties of stress based approaches, fracture mechanics based approach or damage tolerant design approach [33] is pursued. Fracture mechanics views crack growth as a thermodynamic process. The resistance to crack growth is equated to energy required to create new surfaces, and generate dislocations/defects near the crack tip. It assumes a void, flaw or crack of known size and geometry in the bulk material or along an interface. Characterization of initiation and propagation of these material discontinuities is the focus of fracture mechanics. The remote loading applied to the material systems is resolved into inter-laminar tension and shearing loads at the discontinuities to create a mixed-mode (mode I, II and III) loading scenario. Various fracture parameters like strain energy release rate (energy based), stress intensity factors (stress based) at the tip of the crack can be calculated based on the applied loading. Typical failure criteria is established by comparing the fracture parameter values against experimentally determined critical parameter values, thus, this technique calls for material characterization techniques to determine the critical fracture parameters. Two fracture parameters have been commonly used in linear-elastic fracture mechanics (LEFM) to study crack propagation, namely stress intensity factor (SIF) and strain energy release rate (*G*).

2.3.1 Crack Modes

Linear elastic fracture mechanics defines three independent cracking modes based on the direction in which the load is applied.

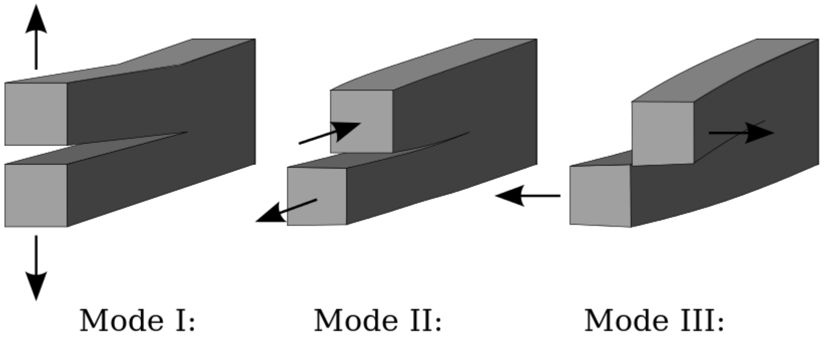


Figure 2-1. Modes of crack propagation [43]

- Mode I: shown in Figure 2-1, opening (tensile) mode. Crack surfaces move away from each other under tensile stresses acting normal to the plane of crack.
- Mode II: shown in Figure 2-1, in-plane shearing mode. Crack surfaces slide over each other under shear stresses acting parallel to the plane of crack and perpendicular to the crack front.
- Mode III: shown in Figure 2-1, tearing (out-of-plane shear) mode. Crack surfaces slide over each other under shear stresses acting parallel to plane of crack and parallel to the crack front.

In homogeneous brittle materials crack predominantly travels in mode I [34]. However, cracks in orthotropic materials or cracks present along material interfaces may propagate under mixed-mode loading conditions [34].

2.3.2 Stress Intensity Factor

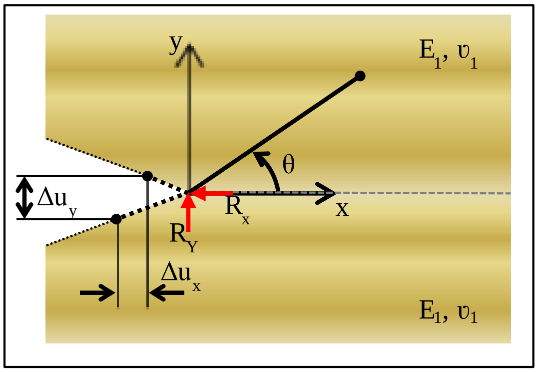


Figure 2-2. Generic representation of crack in a homogeneous isotropic body

The stresses around the crack tip due to remote load are dominated by the crack. Closed form solutions have been developed to calculate stresses acting ahead of the crack as early as 1948 by Irwin and Orowan [35, 36]. The stress fields at a crack tip for a crack present in homogeneous isotropic elastic solid is given by Williams asymptotic solution [37]. Stress at crack tip under tensile loading (mode I) is given by equation (2-2) and under shear loading (mode II) is given by equation (2-3). For the sake of convenience, the equations are usually written in polar co-ordinates where r is the radial distance from the crack tip to the element and θ is the angle measured from the crack surface, as indicated in Figure 2-2.

$$\sigma_{xx} = \frac{K_I}{\sqrt{2\pi r}} \cos\left(\frac{\theta}{2}\right)\left[1 - \sin\left(\frac{\theta}{2}\right)\sin\left(\frac{3\theta}{2}\right)\right]$$

$$\sigma_{yy} = \frac{K_I}{\sqrt{2\pi r}} \cos\left(\frac{\theta}{2}\right)\left[1 + \sin\left(\frac{\theta}{2}\right)\sin\left(\frac{3\theta}{2}\right)\right] \tag{2-2}$$

$$\tau_{xy} = \frac{K_I}{\sqrt{2\pi r}} \cos\left(\frac{\theta}{2}\right)\sin\left(\frac{\theta}{2}\right)\cos\left(\frac{3\theta}{2}\right)$$

$$\sigma_{xx} = -\frac{K_{II}}{\sqrt{2\pi r}} \sin\left(\frac{\theta}{2}\right)\left[2 + \cos\left(\frac{\theta}{2}\right)\cos\left(\frac{3\theta}{2}\right)\right]$$

$$\sigma_{yy} = \frac{K_{II}}{\sqrt{2\pi r}} \sin\left(\frac{\theta}{2}\right)\cos\left(\frac{\theta}{2}\right)\cos\left(\frac{3\theta}{2}\right) \tag{2-3}$$

$$\tau_{xy} = \frac{K_{II}}{\sqrt{2\pi r}} \cos\left(\frac{\theta}{2}\right)\left[1 - \sin\left(\frac{\theta}{2}\right)\sin\left(\frac{3\theta}{2}\right)\right]$$

where, K is the amplitude of singular stress fields acting ahead of the crack tip along the crack surface ($\theta = 0$). K_I and K_{II} are mode I and mode II stress intensity factors. It can be seen from the equation that, σ_{ij} goes to infinity when r goes to zero. In other words, the equation predicts that stress acting at the crack tip is infinity. When such high stresses act around the crack tip, material deforms plastically and the equation no longer holds true. However, if the plastic zone is small enough then the stress distribution around the crack tip can be still predicted using the above equations (2-2) and (2-3). Since, the magnitude of the crack tip stress fields is given by K, it can be compared against critical stress intensity factor (K_c) to predict failure. K_c is a material property that characterizes the stress field at the point of failure. If the magnitude of K is greater than K_c then it will result in crack propagation or failure of the component.

2.3.3 Strain Energy Release Rate

Strain energy release rate (G) is defined as energy dissipated during fracture per unit of newly created fracture surface area. . G can also be interpreted as rate of change in strain energy of the system with respect to crack area. Stress intensity factor is a local parameter at the crack tip calculated based on singular stresses acting at the crack tip. Whereas, G is a global parameter calculated based on global energy change, and is more commonly used as fracture parameter. To determine the total strain energy release rate, the mode I, mode II and mode III G need to be determined. There are several available techniques to calculate G like finite crack extension method [38], domain integral technique [39, 40], virtual crack extension technique [41, 42] and in this work virtual crack closure technique (VCCT) is used. VCCT is based on Irwin's crack closure integral [43, 44], it assumes that energy required to propagate a crack by an infinitesimal amount is equal to energy required to close the crack. Mode I (G_I) and Mode II (G_{II}) strain energy release rates can be calculated using VCCT by the following equations [44],

$$G_I = -\frac{1}{2\,\Delta A} R_y \Delta u_y \tag{2-4}$$

$$G_{II} = -\frac{1}{2\,\Delta A} R_x \Delta u_x \tag{2-5}$$

where, ΔA is crack surface area, R_y, and R_x are the reaction forces at the crack tip in y and x directions, respectively; Δu_y and Δu_x are relative displacements in y and x directions, respectively of a pair of nodes that are initially coincident behind the crack tip, as shown in Figure 2-2. Total energy release rate, G is given by,

$$G = G_I + G_{II} \tag{2-6}$$

2.3.4 Interfacial Fracture Mechanics

First published works on interfacial fracture mechanics appeared in the late 1950s and early 1960s by Williams (1959) [37], Cherepanov (1962) [45], England (1965) [46], Erodogan (1965) [47], Rice and Shih (1965) [48]. However, it lost traction due to lack of application. Recent advances in utilizing multilayered and composite materials in microelectronics, photo-voltaic cells, aerospace and other commercial applications have rekindled the field of interfacial fracture mechanics. The primary difference between interfacial crack and crack propagation through isotropic homogeneous material is, many interfacial crack propagation are mixed-mode in nature [49]. Such a mixed-mode crack propagation scenario arises due to asymmetry in loading and/or mismatch in elastic properties across the interface [34]. Therefore, the stresses acting ahead of the crack tip and displacements behind the crack tip are complex functions of opening and shearing modes for two-dimensional geometries.

Interfacial fracture mechanics has been well studied and documented, if interested the readers are requested to refer the review articles by [34, 49] for detailed explanations. Here only few concepts that will be used in our models are outlined. Generic representation of a crack along an interface is shown in Figure 2-3. Both the materials are assumed to be linear, elastic and isotropic throughout this work. E and v correspond to elastic modulus and Poisson's ratio respectively and the subscripts 1, 2 refer to different materials. The complex stress field ahead around the crack tip is given by,

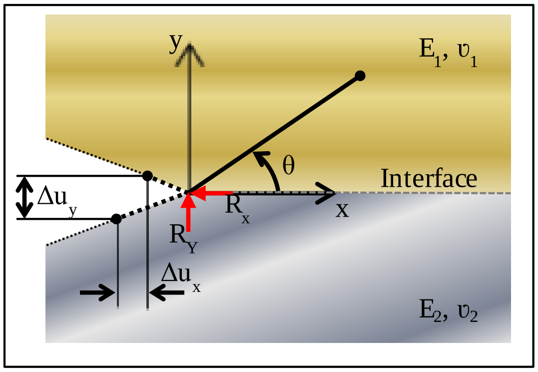


Figure 2-3. Generic representation of crack along a bi-material interface

$$\sigma_{lm}(r,\theta) = \frac{Re\left(Kr^{-i\varepsilon}\right)}{\sqrt{2\pi r}}\tilde{\sigma}^{I}(\theta) + \frac{Im\left(Kr^{-i\varepsilon}\right)}{\sqrt{2\pi r}}\tilde{\sigma}^{II}(\theta) \tag{2-7}$$

where, σ_{lm} is the stress ahead of the crack tip, its subscripts *l*, *m* stand for the components of stress. *‘i’* is the imaginary unit which satisfies the equation $i^2 = -1$ and r, θ are defined in the Figure 2-3. The complex quantity $K = K_I + iK_{II}$ is the stress intensity factor and ε is the bi-material constant or sometimes referred to as oscillation index and is given by,

$$\varepsilon = \frac{1}{2\pi}\log_e\frac{1-\beta}{1+\beta} \tag{2-8}$$

As it can be seen from the above equation that ε depends on Dundurs elastic mismatch parameter β given by [50],

$$\beta = \frac{\mu_1(\kappa_2 - 1) - \mu_2(\kappa_1 - 1)}{\mu_1(\kappa_2 + 1) + \mu_2(\kappa_1 + 1)} \tag{2-9}$$

where, $\kappa_n = (3 - 4\,v_n)$ for plane-strain and μ_n are shear modulus of the materials given by $E_n/(2(1+v_n))$. The dimensionless angular functions $\sigma^{\sim I}_{ij}$, $\sigma^{\sim II}_{ij}$ in (1) is given by [49] and it’s normalized so that at the interface traction (at $\theta = 0°$) is given by,

$$\sigma_{yy} + i\sigma_{yx} = \frac{Kr^{i\varepsilon}}{\sqrt{2\pi r}} \tag{2-10}$$

Mode-mixity is calculated from the ratio of shear stresses to normal stresses. Mode-mixity is measured by the phase angle, Ψ in degrees. It could be understood from the definition of mode-mixity that when $\Psi = 0°$ at a crack tip, stresses ahead of crack tip are only tensile (mode I) and, when $\Psi = 90°$ stresses ahead of crack tip are only shear (mode II). It is important to calculate this parameter because materials have different critical energy release rate (G_c) in different modes. Usually, materials exhibit higher strength in mode II compared to mode I e.g.[51, 52]. From equation (2-10) it can be seen that this ratio can be determined by calculating the real and imaginary parts of K. Also, it can be noticed from equation (2-10) that K has material dependent dimensions when $\varepsilon \neq 0$. This suggests that shear and the tensile modes ahead of the crack tip are inseparably coupled. In other words, the mode-mixity given by the argument of K keeps changing as we approach near the crack tip. As a remedy the mode-mixity for interfacial cracks is measured at a fixed distance L ahead of the crack tip given by, [49]

$$\tan \Psi_L = \frac{Im\left(KL^{i\varepsilon}\right)}{Re\left(KL^{i\varepsilon}\right)} \tag{2-11}$$

Also, phase angle $\Psi_{L'}$ at a distance L' ahead of the tip is given by,

$$\Psi_{L'} - \Psi_L = \varepsilon \log_e \frac{L'}{L} \tag{2-12}$$

This shows that, $\Psi = 0°$ is associated with opening mode at a distance L from the crack tip and at $r \neq L$ mixed-mode fracture can be observed.

Various numerical [29, 30] and exact solution [53] methods have been proposed to determine the real and imaginary parts of K so that the mode-mixity can be calculated. The technique illustrated by [30] using crack surface displacements in order to estimate

K_I and K_{II} is presented here. The analytical solution for oscillatory crack surface displacements can be expressed in complex form as,

$$\Delta u_y + i\Delta u_x = \frac{2\left[\left(\frac{1-\nu_1}{\mu_1}\right)+\left(\frac{1-\nu_2}{\mu_2}\right)\right]}{(1+i2\varepsilon)\,\cosh(\pi\varepsilon)}\,(K_I^* + iK_{II}^*)\sqrt{\frac{r}{2\pi}}\,r^{i\varepsilon} \tag{2-13}$$

Where, Δu_y and Δu_x are the crack surface displacements of initially coincident nodes as defined in Figure 2-3. The distance at which the Ψ_L is evaluated can be obtained by comparing modulus of complex quantity K calculated from the equation (2-13) against the exact linear elastic solution given by [54],

$$|K| = \left[\frac{G}{2\left[\left(\frac{1-\nu_1}{\mu_1}\right)+\left(\frac{1-\nu_2}{\mu_2}\right)\right]}\right]^{1/2} 2\cosh(\pi\varepsilon) \tag{2-14}$$

where G is calculated using virtual crack closure technique given by equation (2-6).

As per equation (2-14) $|K|$ is a constant, however as per equation (2-13) $|K|$ varies with respect to 'r'. However, at a distance $r = L$ the two estimates coincide. In other words, the nodal displacements at a characteristic distance L provide an estimate for $|K|$ close to linear elastic solution. Therefore, phase angle Ψ_L can be determined at L.

As seen from equation (2-10), when $\varepsilon \neq 0$ the variation in normal and shear stresses along the interface (at $\theta = 0°$) is governed by,

$$r^{i\varepsilon} = \cos(\varepsilon \ln r) + i\sin(\varepsilon \ln r) \tag{2-15}$$

This variation of stresses and displacements that depends on ε complicates the implementation of interfacial fracture mechanics. The crack surface displacements given by equation (2-13) predict that the surfaces interpenetrate over a small region, when $\varepsilon \neq$

0. Although researchers have proposed modifications to the solution to negate the interpenetration e.g. [55], others argue that the region of interpenetration is few hundredths even when the ratio of elastic modulus of materials on either side of the interface is 4 or 5. Therefore, this effect can be neglected and the stresses predicted by the above equations away from the zone can be used for failure prediction [56, 57].

As a special case, when $\varepsilon = 0$, $r^{i\varepsilon} = 1$ and then the stress intensity factors is no longer complex function, they fall back to the conventional definitions as mode I and mode II stress intensity factors. In such a case, mode-mixity is given by,

$$\tan\Psi = \frac{K_{II}}{K_I} = \sqrt{\frac{G_{II}}{G_I}} \tag{2-16}$$

G_{II} and G_I are given by equation (2-4) and equation (2-5) respectively.

2.3.5 Critical Strain Energy Release Rate

Critical strain energy release rate (G_c) is considered to be a material property. As mentioned before, material interfaces exhibit higher strength in mode II compared to mode I. Therefore for an interfacial crack, G_c depends on the mode of the loading or mode-mixity. A widely accepted description of the functional dependence of mode-mixity on critical energy release rate is proposed by Hutchinson and Suo [34] and is given by,

$$G_c(\Psi) = G_{Ic}[1 + tan^2(\Psi(1-\gamma))] \tag{2-17}$$

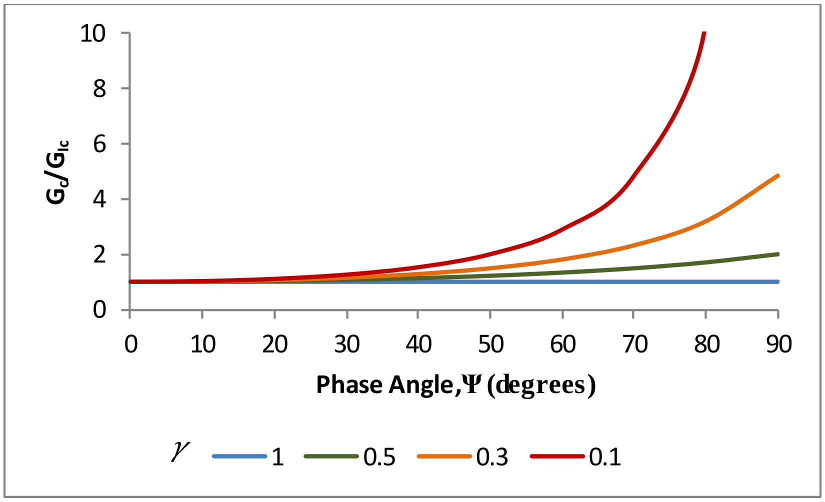


Figure 2-4. G_c vs Ψ variation with respect to change in γ

where, G_{Ic} is the mode I critical energy release rate when phase angle $\Psi = 0$ and γ is a variable that adjusts the influence of the mode II contribution. Figure 2-4 plots the variation in Gc with respect to Ψ for different values of γ, predicted by equation (2-17). For ideally brittle materials $\gamma = 1$ and the crack propagation depends only on mode I. For most material interfaces, as suggested by the above model, G_{IIc} (G_c(90°)) is higher than G_{Ic} (G_c(0°)). It should be noted that, although $G_c(\Psi)$ is symmetric with respect Ψ as per equation (2-17), in most cases this is not true [34]. Once we obtain G_c values at several mode-mixities through appropriate experiments then model given by equation (2-17) can be fit by varying γ.

2.4 COHESIVE ZONE MODELING

Fracture mechanics will provide valuable insights in predicting critical regions, and trends when design changes are carried out. However, it is based on the assumption that a finite size initial crack is present and the assumed size/geometry of the crack may affect the result significantly. Therefore, simulation of crack nucleation and propagation is not straight-forward. Also, multiple simulations are required to predict the full fractured region, given that assumed initial flaw size is reasonably accurate. It is also complicated to consider various fracture mechanisms (e.g. fiber toughening observed in polymeric adhesives [58]). Furthermore 3D fracture mechanics based modeling requires keeping track of energy available for crack propagation at all the nodes along the crack front. Three-dimensional crack propagation simulation involves building a model capable of propagating crack along certain specific paths, which may call for re-modeling and re-meshing the 3D model at each step. Thus, conventional approach is time consuming and calls for assumptions which may have a significant impact on the final results and difficult to include complex material behavior. Also, there are few uncertainties involved in the application of interfacial fracture mechanics as mentioned in the previous section.

Several alternative approaches like cohesive zone modeling (CZM) and extended finite-element method (XFEM) can effectively tackle the above-mentioned disadvantages of fracture mechanics [59, 60]. XFEM is a mesh-free modeling methodology and uses heavyside enrichment function to capture displacement jumps across a crack surface. However, XFEM requires a method to quantify crack initiation and propagation [61]. Remmers et al. [62] formulated cohesive segment method wherein CZM is introduced in an XFEM framework to predict crack initiation and to overcome the mesh dependency of CZM. Although, XFEM sounds promising, there are several numerical challenges [63] and implementation of XFEM in commercial programs is limited in capability at present [61]. Therefore, CZM is used to predict fracture in this work.

Some of the advantages of CZM are,

- CZM eliminates singularity of stress at the crack tip and limits it to adhesive strength of the interface.

- CZM is a single step simulation process, no re-meshing is necessary.
- CZM maintains continuity conditions, despite the physical separation
- CZM effectively integrates strength, stiffness and failure of interfaces
- The size of the non-linear zone (K-dominated zone) need not be negligible in comparison with other dimensions of the cracked geometry [64]
- Since CZM is a phenomenological modeling approach and uses adhesive strength as a failure parameter determined from interface characterization experiments. Therefore, it does not require any ad-hoc criteria for simulating fracture initiation and propagation. In other words, CZM does not require an initial crack.

Over the last few decades, CZM has been successfully implemented to study fracture in metals [65], welded joints [66], concrete [67, 68], polymers, functionally graded materials [69, 70], adhesively bonded joints in [71, 72]. Multimaterial stack numerical analysis using custom material models or in-house programs based on interfacial fracture mechanics and damage evolution laws has also been demonstrated in [73-75].

CZM is an evolution of Dugdale-Barenblatt non-linear process zone [76] that replaces singular stress field ahead of crack tip described by LEFM. CZM views fracture as a gradual phenomenon in which separation takes place across an extended crack tip or cohesive zone and is resisted by cohesive tractions [77]. Usually, in CZM the entire body is treated to be elastic and non-linear behavior fracture behavior is lumped in the cohesive elements described by the cohesive law [78]. Cohesive zone material behavior explained above is illustrated in Figure 2-5. Figure 2-5 shows a crack on the left of the figure and various zones are indicated in it. At point (1) the material behaves in a linear elastic manner with undamaged interface (indicated in green), between points (2) and (4) the interaction between the surfaces is controlled by the traction-separation law, at point (3) damage initiates when the separation exceeds the δ^*, and at point (4) complete debonding occurs when separation exceeds the critical separation, δ_c. Beyond point (4) there is no active interaction between the crack surfaces. As shown in Figure 2-5, δ_c is the point at which traction goes to zero. Since cohesive zone spans the region between undamaged and fully damaged, the area under the *T*-δ law is the energy required to separate the interface G_c.

$$G_c = \int_0^{\delta_c} \sigma(\delta) d\delta \tag{2-18}$$

where $\sigma(\delta)$ is the functional form of *T*-δ law.

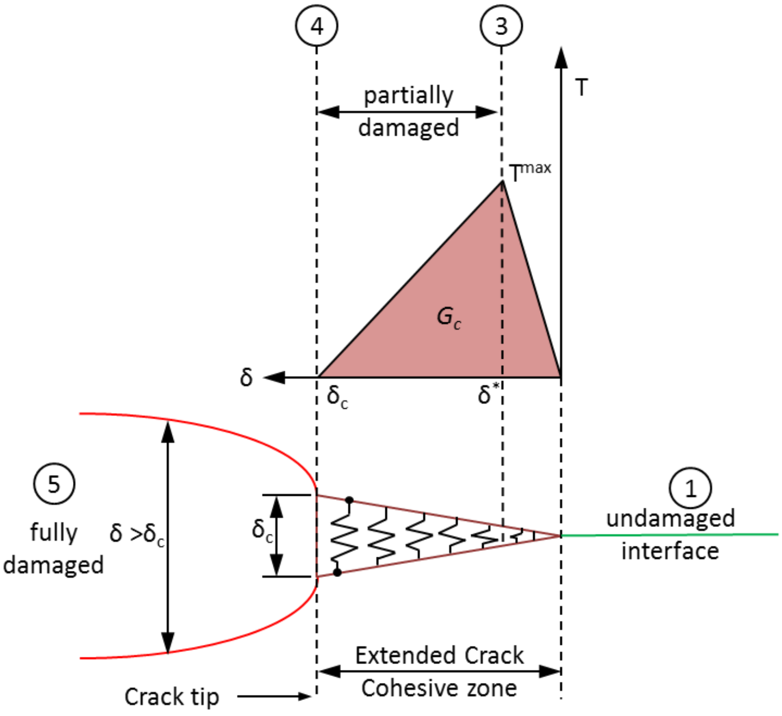


Figure 2-5. Cohesive zone modeling

2.4.1 Traction Separation Law

Nonlinear fracture process or the interactions between the fracture surfaces in the cohesive zone is governed by the chosen traction-separation law. In other words, stresses in the cohesive zone are governed by the T-δ law. Two key parameters required to describe any law are the maximum traction (T^{max}) and the critical separation (δ_c), as seen in Figure 2-5.

Several traction-separation constitutive relations have been developed based on specific application like cubic polynomial [79], trapezoidal [80], exponential [77], bilinear law [81, 82]. Each of them has their own advantages and limitations, and most of them have a positive slope, followed by a negative slope indicating decreasing resistance during separation. When the separation exceeds a critical value it results in complete failure, in other words, no loads are transferred across the fracture surfaces. Detailed reviews about different cohesive laws and their limitations can be found in [83].

Selection of appropriate material constitutive behavior (linear elastic, plastic, or viscoplastic) and the type of cohesive law will influence the simulation results [84, 85]. Rose and Ferrante [86] have provided the relationship between binding energy and atomic separation. Based on this work, Needleman [87] is one of the first to apply the exponential traction-separation type cohesive model to study fracture in ductile materials. For analytical convenience and to better model material behavior various traction-separation relationships have been proposed and are reviewed in literature [60, 88]. Researchers have used bilinear CZ model to study brittle and quasi-brittle fracture [89, 90]. Since the material system of interest in this work undergoes brittle failure, a bilinear cohesive law is used [91], as shown in Figure 3. Although CZM can predict crack initiation and propagation, embedding CZ elements all over the model will change its stiffness and will be computationally expensive. Also, this requires characterization of CZ parameters for various materials and interfaces in the structure. Therefore, in this work, the CZ elements are introduced along the anticipated crack paths, as guided from focused ion beam (FIB) cross-sections.

The bilinear law was introduced by Hillerborg et al. [92] and implemented by Espinosa, and Zavattieri [93] to study failures observed in brittle, polycrystalline materials. Over the years several modifications have been suggested, and here we will use the framework developed by Alfano and Crisfield [78].

2.4.2 Bilinear CZ Model

A schematic of Mode I and Mode II dominated bilinear model is shown in Figure 2-6. Mode I dominated law is applicable when cohesive separation is dominated by displacement jump normal to the interface, e.g. DCB test. Mode II dominated law is applicable when cohesive separation is dominated by shear displacement, e.g. three-point end notch flexure test (3ENF) or four-point end notch flexure test (4ENF). In reality most systems operate under mixed-mode loading conditions and the critical energy release rate is in between Mode I and Mode II as shown in Figure 2-6. Therefore, it is essential to determine both the limiting cases of Mode I and Mode II to predict real-time fracture process.

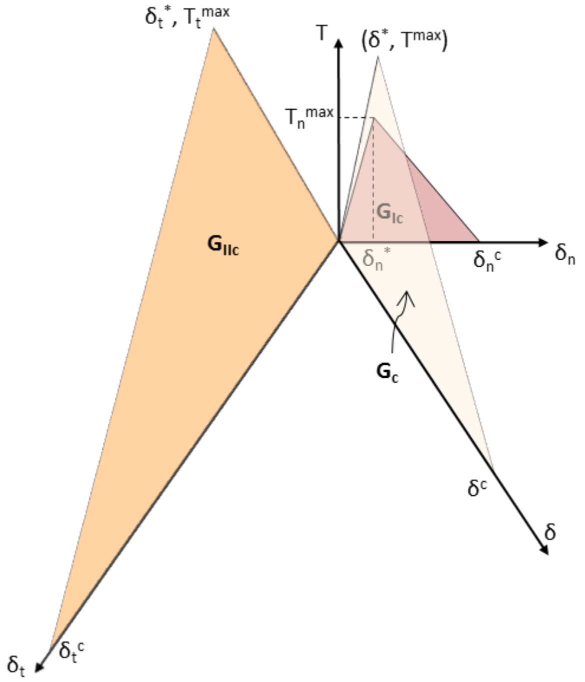


Figure 2-6. Mixed-mode bilinear traction-separation law

2.4.3 Mode I and Mode II Damage Models

The relation between normal traction T_n and normal displacement δ_n is expressed as, [78]

$$T_n = K_n \delta_n (1 - D_n) \tag{2-19}$$

where, K_n is normal cohesive zone element stiffness (T_n^{max}/δ_n^{*}), T_n^{max} is the maximum normal traction, δ_n^{*} is the normal displacement jump at T_n^{max} and δ_n^{c} is the normal displacement jump at completion of debonding.

δ_n is the normal displacement jump attained in deformation history and the damage D_n (ranges between 0 and 1) is given by equation (2-20).

$$D_n = \begin{cases} 0 \quad , & \delta_n \leq \delta_n^* \\ \left(\frac{\delta_n - \delta_n^*}{\delta_n}\right)\left(\frac{\delta_n^c}{\delta_n^c - \delta_n^*}\right), & \delta_n^* \leq \delta_n \leq \delta_n^c \\ 1 \quad , & \delta_n \geq \delta_n^c \end{cases} \tag{2-20}$$

In a series of loading and unloading processes, δ_n at a given instant may be less than the δ_n attained in one of the prior loadings. This does not mean that D_n will become less than the D_n achieved for the prior loading. In other words, regardless of the current value of δ_n, at no particular instant, D_n can be less than previously attained D_n.

Mode II dominated damage model is obtained by replacing subscripts 'n' with 't' in the above equations to indicate that the fracture process is shear dominated. T_n^{max}, δ_n^*, δ_n^c, T_t^{max}, δ_t^*, and δ_t^c are schematically shown in Figure 2-6. Typically, the mode II (shear mode) critical strain energy release rate G_{IIc} is greater than mode I (normal) critical strain energy release rate G_{Ic} [51], as shown schematically in Figure 2-6.

2.4.4 Mixed-mode Damage Model

The separation behavior under mixed-mode loading conditions depends on both Mode I and Mode II components of displacement jumps. A non-dimensional effective displacement jump λ for mixed-mode fracture is defined as,

$$\lambda = \sqrt{\left(\frac{\delta_n}{\delta_n^c}\right)^2 + \beta^2\left(\frac{\delta_t}{\delta_t^c}\right)^2} \tag{2-21}$$

where β is the weighting parameter defined by,

$$\lambda_{cr} = \frac{\delta_n^*}{\delta_n^c} = \beta\left(\frac{\delta_t^*}{\delta_t^c}\right) \tag{2-22}$$

The normal and tangential components of the traction is given by,

$$T_n = K_n\delta_n(1 - D_m) \tag{2-23}$$

$$T_t = K_t\delta_t(1 - D_m) \tag{2-24}$$

Mixed-mode bilinear cohesive law damage parameter D_m is given by,

$$D_m = \begin{cases} 0, & \lambda \leq \lambda_{cr} \\ \min(1, \quad d_m), & \lambda > \lambda_{cr} \end{cases} \tag{2-25}$$

where, λ is the effective normalized displacement jump attained during deformation history, and λ_{cr} is the value of λ at which effective traction is maximum given by equation (2-22). Damage starts to accumulate once λ exceeds λ_{cr} given by equation (2-25) and damage variable d_m is given by equation (2-26).

$$d_m = \eta \left(\frac{\lambda - \lambda_{cr}}{\lambda} \right) \tag{2-26}$$

where,

$$\eta = \sqrt{\left(\frac{\delta_n^c}{\delta_n^c - \delta_n^*} \right)^2 + \beta^2 \left(\frac{\delta_t^c}{\delta_t^c - \delta_t^*} \right)^2} \tag{2-27}$$

To fully characterize a delamination process using mixed-mode cohesive law, six independent parameters schematically shown in Figure 2-6 (G_{Ic}, T_n^{max}, α_n the ratio of δ_n^* to δ_n^c, G_{IIc}, T_t^{max}, α_t the ratio of δ_t^* to δ_t^c) are to be determined. In this work, mode I CZ parameters (G_{Ic}, T_n^{max}, α_n) are determined from DCB test results, as the crack propagates close to mode I during DCB test. Mode II energy release rate (G_{IIc}) is determined from 3ENF tests as the crack propagates close to mode II during 3ENF test. The remaining mode II parameters (T_t^{max}, α_t) are obtained from results of mixed-mode FPB test experiments.

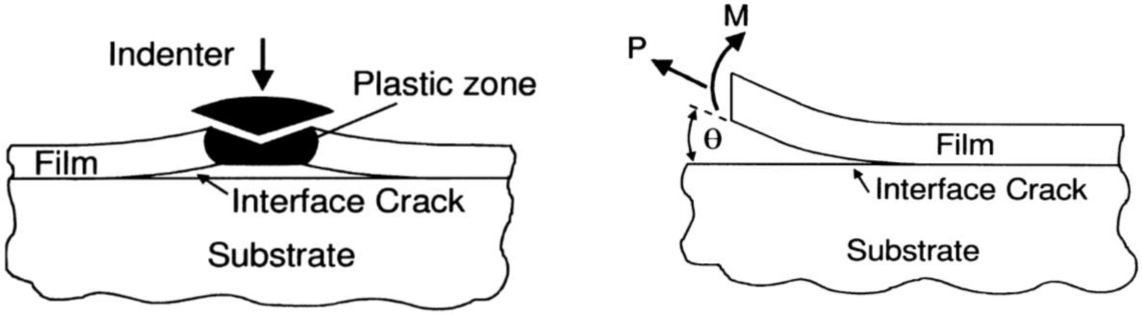
2.5 EXPERIMENTAL TECHNIQUES

Determination of critical energy release rate (G_c) for different modes of failure is a key component in reliability assessment of microelectronic devices involved in this study. Many different measurement techniques are available to obtain G_c for thin-films and they can be broadly classified as sandwich specimen bend tests (four-point bendFPB, DCB), indentation tests, peel tests, and blister test. The tests are reviewed in this work [94].

Indentation methods using nano-indenter to measure the adhesion strength of thin-films have been successfully demonstrated [19]. Schematic of the indentation test is shown in Figure 2-7a. The value of the fracture parameter is related to plastic zone size and extent of debonding [95]. However, there are several assumptions involved in such a technique with regards to the complex plastic strain fields and the effect of underlying layers. Typically, indentation and derivatives of indentation (scratch test) yield qualitative results.

In peel tests, thin-films are peeled from a substrate using mechanical forces [96] or magnetic forces [20] or electrostatic forces [97] or even by depositing highly stressed layer on the thin-films [98-100]. Schematic of peel test is shown in Figure 2-7b. Since, the displacements and forces are large enough for existing metrology, accurate prediction of G_c is possible. Consequently, large displacements result in plastically straining the thin-films during delamination. In most cases, separating plastic strains in calculation of G_c is complicated [101].

Finally, blister test is performed by etching a cavity in the substrate and pressurizing the thin-films [102]. Schematic of blister test is shown in Figure 2-7c. The challenge in employing such a test is to avoid the chemical interaction between the pressurizing environment and interface as well as the etchants or other procedures used for creating the cavity should avoid damaging the interface.



a) Indentation

b) Peel test

c) Blister test

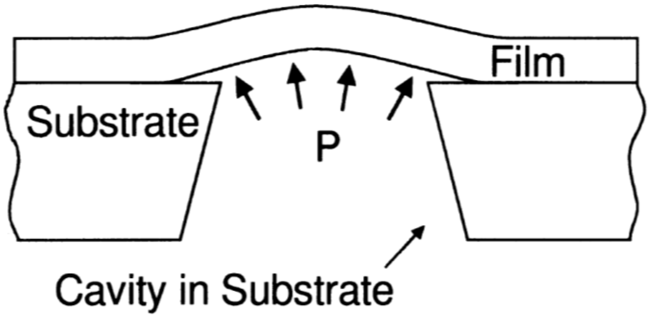


Figure 2-7. Thin-film delamination tests [103]

The biggest limitation of the techniques mentioned above is the relaxation of residual stresses in the thin-films during delamination. Such relaxation effects contribute significantly towards the driving force required for delamination [103, 104]. Although residual stress effects on G_c can be considered for few cases [104], it is often difficult to accurately characterize the residual stress effects. Particularly for thin-film stacks subjected several thermal excursions during processing, it is very complicated to include such effects. Also, most of these tests have been demonstrated for blanket layer of film deposited on substrate. However, in the sample used for the study there are several layers of thin-films ranging from tens of nm to hundreds of microns in thickness deposited on silicon substrate. The challenge is to first identify the weakest layer/interface and propagate the crack along that layer by applying mixed-mode loads. Also, the layers are expected to be brittle in nature characterized by their low G_c [34, 51]. Furthermore, the samples used for the study are obtained from 45 nm wafer-fab and introducing a crack or flaw at the desired location during processing is not readily possible.

2.6 BEND TESTS

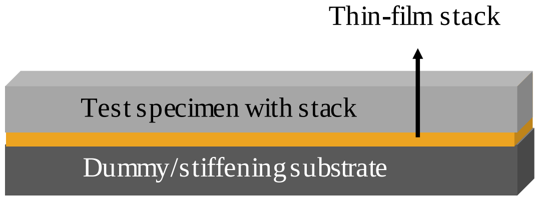


Figure 2-8. Schematic of sandwich specimen

In the quest for tests that can create a crack in the weakest layer, provide mixed-mode G_c data and yield reliable and repeatable results, we chose bend tests performed using sandwich specimen. Schematic of a symmetric sandwich test specimen is shown in Figure 2-8. As shown, the test substrate is the substrate on which the thin-films are deposited is glued on to a dummy or stiffening substrate. A symmetric sandwich specimen is one in which the test and dummy substrates are of same dimensions and material properties. Since the test substrate on which thin-films are deposited and the dummy substrate are at least couple of orders of magnitude thicker than the thin-film stack thickness, the fracture parameter does not depend on the properties of the of thin-films.

2.6.1 Double Cantilever Beam Test

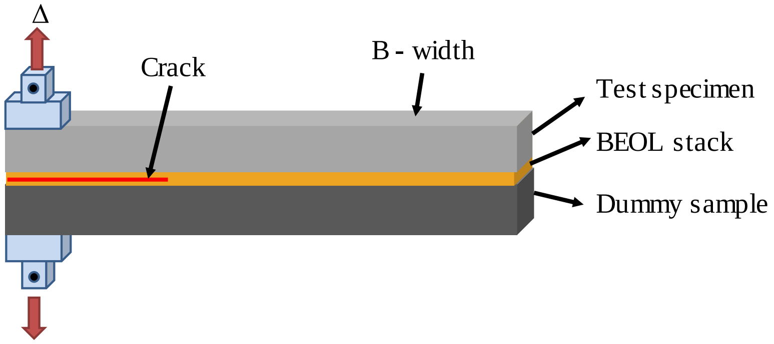


Figure 2-9. Schematic of DCB sample

One of the most popular thin-films fracture characterization experiments is double cantilever beam (DCB) test. The schematic of DCB test is shown in Figure 2-9. Crack in DCB, predominantly propagates close to mode I in symmetric sandwich specimen.

2.6.2 Four-Point Bend (FPB) Test

Charalambides (1989) [105] proposed four-point bend test geometry for finding the G_c of bi-material interfaces. Later it is modified by Dauskardt et al. [103] to use FPB test to determine the G_c of thin-film stack. Schematic of the FPB test sample proposed by Dauskardt et al. is shown in Figure 2-10. He noticed that the crack starts from the notch propagates through the stack of thin-films and once it hits the weakest layer, the crack propagates parallel to the length of the sample.

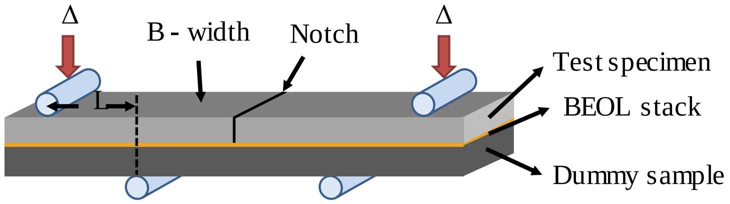


Figure 2-10. Schematic of FPB test sample

2.6.3 Three-Point End Notch Flexure (3ENF) Test

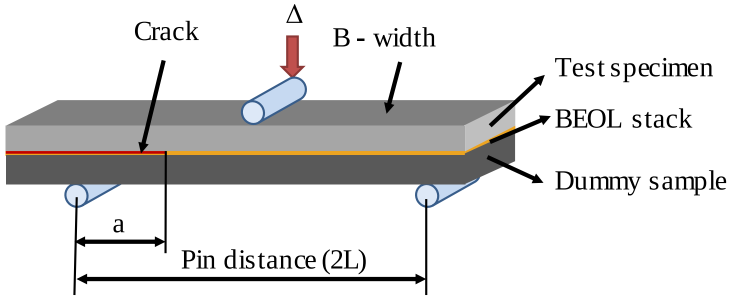


Figure 2-11. Schematic 3ENF test sample

The schematic of the 3ENF test is shown in Figure 2-11. Crack in 3ENF, predominantly propagates close to mode II in symmetric sandwich specimen.

Thus three separate experiments with different sample preparation methods are required to determine the mixed-mode G_c. In order to overcome such difficulties there are setups available in literature where a single test setup can yield G_c values in different mode-mixities.

2.6.4 Modified DCB Test Technique

Fernlund and Spelt [106] developed a test setup to determine mixed-mode G_c for sandwich test specimen. The loading fixture is illustrated in Figure 2-12. The forces F_1 and F_2, applied on upper and lower beams can be varied to obtain different mode-mixities. Such a configuration is a modification of standard double cantilever beam (DCB) test. G_c is given by equation (2-28), can be calculated from the applied forces and crack lengths. Similarly, Ψ can also be determined from the forces given by equation (2-29).

$$G = \frac{6(1-\nu^2)F_1^2a^2}{EB^2H^3}\left[1+\left(\frac{F_2}{F_1}\right)^2-\frac{1}{8}\left(1-\frac{F_2}{F_1}\right)^2\right] \tag{2-28}$$

$$\Psi = arctan\left(\frac{\sqrt{3}}{2}\frac{\left(\frac{F_1}{F_2}-1\right)}{\left(\frac{F_1}{F_2}+1\right)}\right) \tag{2-29}$$

However, the test technique requires a known crack length to be embedded in the sample and the next challenge is measurement of crack length as the test progresses. The differential separation between the upper and lower beams is at the order of few microns and measuring such low deflections reliably is tedious. As seen from equation (2-28), the measurement of crack length as the test progresses is critical because the fracture parameter depends on critical load as well as the crack length. Therefore, the test technique can be used for standard lab specimen with a crack of known length embedded along the critical interface and when a reliable method for determining the crack length as the test progresses is not available.

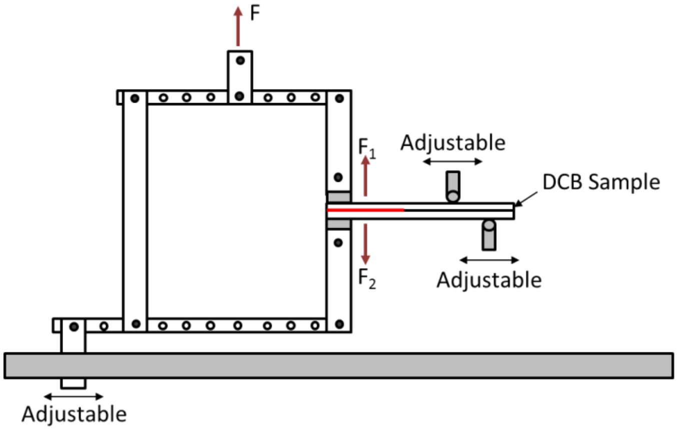


Figure 2-12. Schematic of modified DCB test setup [51]

Since the samples in this work does not fall under the standard lab sample category. Here, DCB, FPB and 3ENF are used for determining mixed-mode G_c. Furthermore, the results from the experiments can be used to calibrate CZ parameters required for white-bump risk prediction.

CHAPTER 3

OBJECTIVES AND SCOPE

3.1 GAPS IN EXISTING RESEARCH

Cracking in multilayer sub-micron scale thin-film stacks has been a reliability concern, particularly in microelectronic packages. However, the existing literature based-on stress based approaches or fracture-mechanics based approaches are not able to effectively address the concerns due to:

1. lack of experimental characterization of sub-micron scale BEOL stacks over a wide range of mode-mixity
2. lack of existing methodology to obtain mixed-mode cohesive zone parameters
3. lack of integrated simulation techniques that cover the wide range of length scales from nm to mm in combination with appropriate experimental characterization
4. lack of reliable framework to simulate crack initiation and propagation through sub-micron scale multimaterial stacks using commercially available FE modeling package
5. lack of fracture characterization experiments that are sensitive to microscale variations in trace pattern layout around the vicinity of a solder bump.

3.2 OBJECTIVES AND SCOPE

Given the above gaps in the literature, the objectives of this work are to:

1. Develop appropriate experimental characterization techniques to study interfacial crack propagation in sub-micron layers. In particular,
    a. Use a FPB test to create a starter delamination in sub-micron layer BEOL stack
    b. Use the sample with starter delamination to perform DCB tests and 3ENF tests to determine the critical energy release rate at different mode-mixities.
2. Characterize the mixed-mode CZ parameters using experiment results through inverse analysis technique. In particular,
    a. Crack propagates close to mode I in DCB test and close to mode II in 3ENF test. Therefore, area under the mode I and mode II T-δ law is assumed as critical energy release rate determined from DCB and 3ENF tests, respectively.
    b. The remaining mode I CZ parameters are determined through inverse analysis of the load-displacement curve of DCB test.
    c. The remaining mode II CZ parameters are determined through inverse analysis of the load-displacement curve of FPB test.
3. Employ the developed cohesive zone model to determine the onset and propagation of interfacial crack in a flip-chip assembly. In particular,
    a. Develop a numerical model that can mimic the flip-chip assembly process taking into consideration the time-, temperature-, and

    direction-dependent material properties with the appropriate time-temperature history

    b. Implement the developed cohesive zone elements at critical interfaces and study delamination initiation and propagation under assembly loading conditions
    c. Determine the bumps where such delamination will occur and at what temperature conditions, and validate such predictions with experimental data

4. Develop appropriate material and geometry based design guidelines to mitigate interfacial delamination and thus white-bump formation
5. Demonstrate a new micro-scale nanoindentor-based bump shear test technique, specifically designed and developed as part of this research. The test technique is sensitive to variations in fracture parameter owing to micro-scale variations in trace patterns in the vicinity of a bump.

3.3 THESIS LAYOUT

The rest of the chapters in this thesis are organized as shown below,

3.3.1 Chapter 4

As a first step, 2D fracture mechanics based finite-element models are developed to study the white-bump (ILD) failures observed at the end of flip-chip chip-attach process. Such models provide valuable insights on potential failure locations and predict favorable design changes to reduce white-bump risk.

3.3.2 Chapter 5 and Chapter 6

Next, a CZM based approach is developed to study the white-bump failures in order to overcome the limitations of fracture mechanics models. CZM is a phenomenological approach; therefore this necessitates interface fracture strength characterization of BEOL stack. In flip-chip assembly conditions, a crack present in critical layer of the BEOL stack propagates in mixed-mode conditions. Therefore, mixed-mode fracture characterization experiments are performed to obtain the fracture strength at different mode-mixities.

3.3.2.1 Chapter 5

The samples obtained for the study are diced from C45 (45 nm technology node) wafers. The advantage in performing experiments using such a sample is that the internal stresses of thin-films that develop during fabrication are considered in-situ. However, the biggest challenge is that pre-fabricated cracks cannot be introduced in the stack.

In order to overcome the challenge, a symmetric sandwich specimen is prepared by gluing the test specimen on a dummy silicon substrate. Then, the specimen is subjected to FPB test. FPB test is capable of identifying the weakest layer present in the stack. Another advantage of FPB test is that the steady-state G_c value obtained from FPB test does not depend on crack length.

Using the crack generated by FPB test as the starter crack, DCB and 3ENF tests are performed to characterize the critical interface in various mode-mixities.

3.3.2.2 Chapter 6

FPB, DCB, and ENF tests are used to determine G_c as a function of Ψ. However, CZM needs other parameters beyond such fracture parameters, including maximum traction, separation, and shape of traction-separation curve for different mode mixities. Therefore, simulations to mimic load versus displacement curves of DCB and FPB tests are used to determine the mixed-mode CZ parameters.

3.3.3 Chapter 7 and Chapter 8

The developed cohesive zone parameters are then placed in the BEOL stack to determine the fractured region using 2D and 3D numerical models. The results obtained through cohesive zone model are compared against fracture mechanics based models as well as experimental failure-analysis data. Such models are used to develop design guidelines to reduce white-bump failures in flip-chip assemblies.

3.3.4 Chapter 9

Finally, nanoindenter-based bump shear test technique is presented that can address different mode-mixities compared to DCB, FPB and 3ENF tests. The test technique is sensitive to local BEOL fracture characteristics (example change in trace pattern layout) and mimics flip-chip assembly reflow process.

Through this experimental and theoretical modeling research, this thesis aims to develop guidelines for the reliable design of BEOL stacks for current and next-generation microelectronic devices.

CHAPTER 4

BEOL RELIABILITY STUDY USING FRACTURE MECHANICS

4.1 INTRODUCTION

This chapter presents a fracture mechanics based numerical models to study the effect of package induced stresses on BEOL stack. Two-dimensional plane-strain flip-chip finite-element (FE) models are created to study the energy available for a crack present in ULK layer. In fracture mechanics a crack/flaw of known geometry and location is assumed to be present and G is calculated based on the loading conditions. If G is greater than G_c for the interface then the crack is allowed to propagate. In the numerical models presented in this chapter, a crack of 2 µm length is assumed to be present along the critical ULK layer. The critical layer is determined from FIB cross-sections of white-bumps observed in real devices. A crack length of 2 µm is chosen because it can be reliably detected using available non-destructive techniques like C-mode scanning acoustic microscopy (CSAM). Next, the flip-chip assembly is simulated to go through the reflow process and the energy available for the crack at the end of chip-attach process is determined. The objectives of this chapter are to:

- develop a modeling methodology to simulate the flip-chip assembly chip-attach process
- determine G for a crack along the critical ULK interface
- determine the critical region above the solder bump where the crack has maximum energy to propagate
- propagate the crack present in the critical region if it satisfies the failure criterion ($G \geq G_c$) and compare the predicted final crack length with failure analysis results.

Such a model is then used to develop design guidelines to prevent ULK cracking in flip-chip assemblies.

4.2 MODELING METHODOLOGY

The chip used in this study is based on the 45 nm technology node (C45) with ten metal layers in the BEOL stack. The stack built on top of the die comprises of four 1x, four 2x and two 10x layers, where ‘x’ refers to a normalized trace thickness. The 1x and 10x metal layers are insulated by low-κ ILD layers, while 2x metal layers are insulated using ULK ILD layers. Figure 4-1a shows the schematic of the BEOL stack with a crack above the Al pad edge. Figure 4-1b shows the detailed schematic of the C45 BEOL stack. As shown, 1x layers are near the transistors and are 100 nm thick, 2x ULK layers are 250nm thick, and 10x layers are near the solder bumps and are 1.2 µm thick. A focused ion beam (FIB) cross-section of the C45 die with BEOL stack is shown in Figure 4-1c, and the various components are also indicated in the figure. Interlayer cracking in one of the ULK layers can be clearly seen in Figure 4-1c and it is schematically shown in Figure 4-1b. As indicated in Figure 4-1b, the interlayer crack propagates primarily along the interface of two sequentially deposited ULK layers.

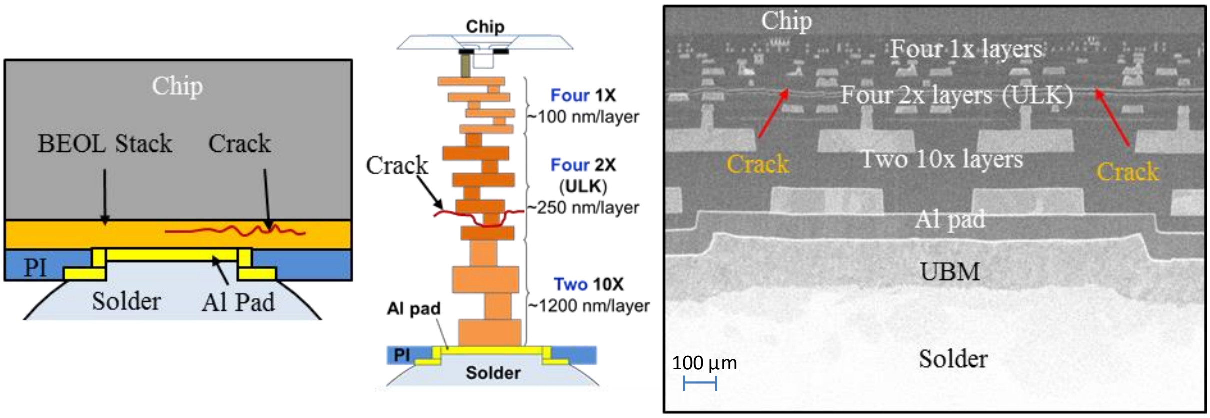


Figure 4-1. a) Schematic of white bump b) Schematic of BEOL stack with dimensions and c) FIB cross-section of 45 nm BEOL stack showing crack propagating along ULK layer.

Two-dimensional (2D) plane-strain half-symmetric parametric FE model of the organic flip-chip assembly is created using ANSYS®. Schematic of the cross-section is shown in Figure 4-2 and the dimensions of various components are given in Table 4-6. Die thickness is 780 µm, solder diameter is 88 µm, solder height is approximately 64 µm, polyimide thickness is 6.4 µm, the die pad is a 75 µm square Al pad and the pad opening is 47 µm. The multi-layer organic substrate consists of 400 µm thick core and four buildup layers on either side of the core. Each buildup layer consists of 33 µm thick buildup dielectric and 15 µm thick metallization layer. The size of the die is 15 x 12 mm and the size of the substrate is 37.5 x 37.5 mm. The thickness of the layers present in the BEOL stack is in nanometer scale. In order to build an "all in one" assembly model which includes the substrate, solder, passivation layer, die with BEOL stack and finally include a crack in the BEOL stack would prove costly in terms of modeling time, solution time, scratch space and memory required. Therefore, a global-local model or submodeling approach is adopted here.

In the global model, the components that do not affect the overall stiffness of the assembly significantly are ignored, and the model is simulated to go through the chip-attach process. Then a separate local model around a specific region of interest is created which includes the fine features. The model is solved by applying the displacement boundary conditions obtained from the global model. Local model focuses on a small critical area, and therefore, determining the location and size of the local model plays an important role in getting reliable results from this approach. The sub-modeling approach yields reasonably accurate solutions, provided that the boundary conditions are applied far away from the regions of interest. The results from the simulation are compared against hammer test failure analysis results. The hammer test is performed by cooling the package from reflow temperature to room temperature at a much higher rate than reflow process in order to ensure robustness of the package. Typical reflow process cooling rate is 25 °C/minute and hammer test cooling rate is 60 °C/minute from reflow temperature to room temperature.

4.2.1 Material Properties

Isotropic material properties are used for silicon die and BEOL stack materials as shown in Table 4-1. Table 4-2 shows the temperature dependent isotropic material properties used for buildup dielectric layer present in the substrate; orthotropic material properties are applied to the core and it is shown in Table 4-3. Isotropic temperature dependent properties are used for lead-free solder (96.5% Sn; 3.5% Ag) is shown in Table 4-4 and Anand viscoplastic material properties for the lead-free solder is shown in Table 4-5.

Table 4-1. Elastic Material Properties [*Freescale Semiconductor vendor data]

Material Property	Cu [107, 108]	Si [109, 110]	Al*	TEOS*	PI*	ULK*	SICOH*
E (GPa)	103.42	130	68.9	66	3.2	4.5	7.4
ν	0.34	0.28	0.33	0.18	0.28	0.28	0.15
CTE, α (ppm/°C)	17	2.66	24	0.54	55	14	15

Table 4-2. Substrate Build-up Properties [Freescale Semiconductor vendor data]

Temperature (°C)	25	50	100	125	130	150	200	260
E (GPa)	4.05	4.00	3.10	2.40	2.00	1.70	0.10	0.10
ν	0.26	0.26	0.26	0.26	0.26	0.26	0.26	0.26
CTE, α (ppm/°C)	46	46	46	46	46	46	120	120

Table 4-3. Substrate Core Properties [Freescale Semiconductor vendor data]

Temperature (°C)	30	95	125	150	270
E_x (GPa)	22.4	20.7	19.3	17.9	16.0
E_z (GPa)	22.4	20.7	19.3	17.9	16.0
E_y (GPa)	1.6	1.2	1.0	0.6	0.5
ν_{xy}	0.02	0.02	0.02	0.02	0.02
ν_{yz}	0.143	0.143	0.143	0.143	0.143
ν_{xz}	0.143	0.143	0.143	0.143	0.143
G_{xy} (GPa)	4.99	4.78	4.51	4.40	4.30
G_{yz} (GPa)	4.99	4.78	4.51	4.40	4.30
G_{xz} (GPa)	4.99	4.78	4.51	4.40	4.30
α_x (ppm/°C)	16	16	16	12	12
α_z (ppm/°C)	16	16	16	12	12
α_y (ppm/°C)	23	23	23	150	150

Table 4-4. Solder Material Properties [111]

Temperature (°C)	-25	25	60	100	150	227
E (GPa)	58.881	49.229	42.472	34.750	25.097	10.232
ν	0.4	0.4	0.4	0.4	0.4	0.4
α (ppm/°C)	24	24	24	24	24	24

Table 4-5. Anand viscoplastic solder material properties [111].

Parameter	S_o (MPa)	Q/R (K)	A	X_i	H_o (MPa)	M	S_h (MPa)	n	a
Value	39.09	8900	22300	6	3321.15	0.13	73.81	0.018	1.82

4.2.2 Global Model

A schematic of the global model is shown in Figure 4-2. The global model includes the die, solder bump, bump pads, polyimide layer as a mask on top of die and various layers in the substrate with appropriate material properties, as shown in Figure 4-2. Figure 4-2 also shows that symmetric boundary conditions are applied to the left edge of the model and one node is additionally constrained in all degrees of freedom to prevent rigid body motion. The substrate is assumed to be stress free at 150 °C because build-up layers and solder mask cure temperatures varies between 150 to 180 °C based on the manufacturer. The stress-free temperature for the solder and die is assumed to be the lead-free solder melting temperature (220 °C). It can be seen from Figure 4-2 and Figure 4-6 that the metallization and the buildup dielectric layers present in the substrate are also modeled in the global and local models. Since the substrate metallization layers consist of copper traces interspersed with buildup dielectric, effective orthotropic material properties determined using the micromechanics approach are used. The volume percentage of copper required to calculate the effective material properties is determined from the trace pattern images of each metallization layer in the substrate. Trace pattern image for each metallization layer is extracted from .mcm (multichip module) file and converted to high resolution bitmap image using Cadence Allegro PCB™ designer software. Then, the image is further subdivided into several small areas and the volume percentage of copper in each area is calculated by counting the number of colored and uncolored pixels in each area [112, 113]. The above mentioned image-processing methodology to extract volume percentage of copper is implemented using in-house developed MATLAB® code. Calculated orthotropic material properties are applied to metallization layers present in the substrate. The global model is simulated to cool down from the solder reflow temperature (220 °C) to room temperature (25 °C) at 60°C/minute. Since the actual samples are cooled in a reflow oven, the temperature is assumed to be uniform across the entire model during the simulation.

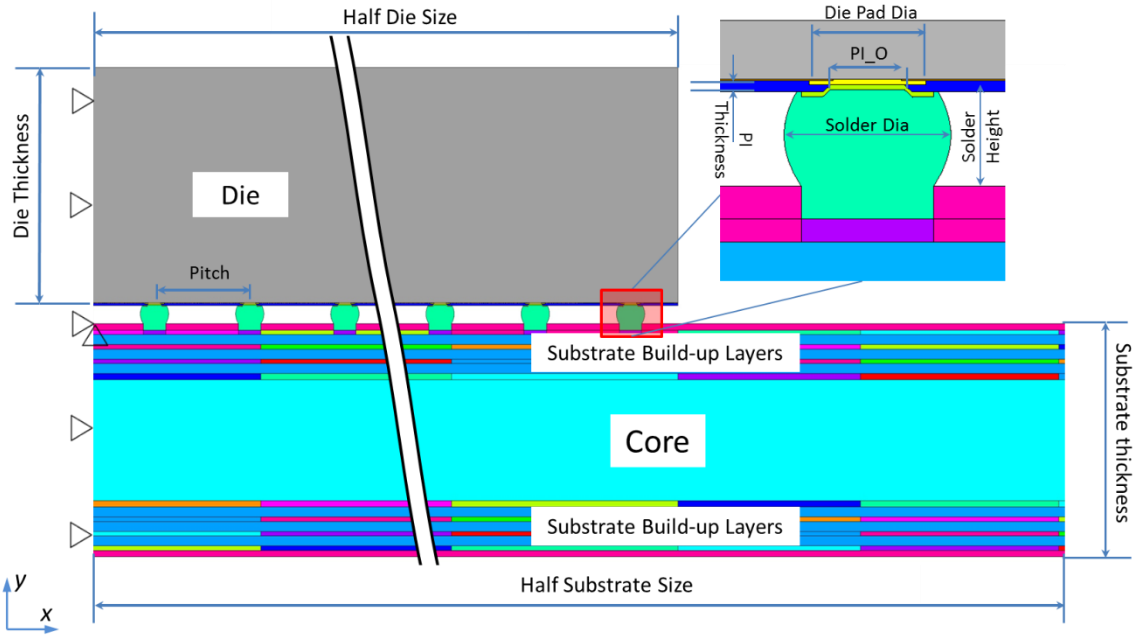


Figure 4-2. 2D flip-chip global assembly model with boundary conditions

Table 4-6. Global model dimensions

Parameter	Value (µm)
Full Die Size	15000
Die Thickness	780
Die Pad Dia	90
Pitch	360
PI Thickness	6.4
PI_O	30
Solder Dia	88
Solder Height	~64
Full Substrate Size	37500
Core Thickness	400
Substrate Thickness	730

Warpage of the die at room temperature obtained from the global model is shown in Figure 4-3. Since the model is half-symmetric, span of the *x*-axis in Figure 4-3 is half the length of the long edge of the die (7500 µm). As expected, the die warps down as the effective CTE of the substrate is greater than the die. Figure 4-3 also compares the warpage of the die with elastic temperature dependent solder material properties and viscoplastic solder material properties. It should be noted that, the rate at which the temperature-dependent elastic model is cooled down does not affect the results. However, care is taken to ensure that, enough number of sub-steps are provided to capture the temperature dependency of different material properties during cool-down simulation.

The model with viscoplastic solder is cooled down at the prescribed hammer test cool-down rate of 60 °C/minute. It can be seen from Figure 4-3 that the maximum difference in warpage is less than 1%. Such a behavior is expected because cool-down time of three minutes is not enough time to cause viscoplastic relaxation of solder. Therefore, all materials are assumed to be temperature-dependent elastic/orthotropic and rate independent, as appropriate.

Figure 4-4 shows the peel stress variation (*y* direction) between center and corner solder bumps having same finite-element mesh density, at room temperature. It can be seen from the contour plots shown in Figure 4-4 that the magnitude of stress increases as we move away from the center of the die. In other words, the stresses near the corner solder bumps are significantly greater than the stresses experienced by the bumps, located near the center of the die. This indicates that the corner solder bumps are more prone to white-bump failure compared to the bumps present near the center of the die. Therefore, the corner solder bump is further studied using the local model. It can be seen from Figure 4-5, that the corner solder bump is subjected to a moment (clockwise in this case) resulting in tensile stresses on the right side and compressive stresses on the left side of the bump.

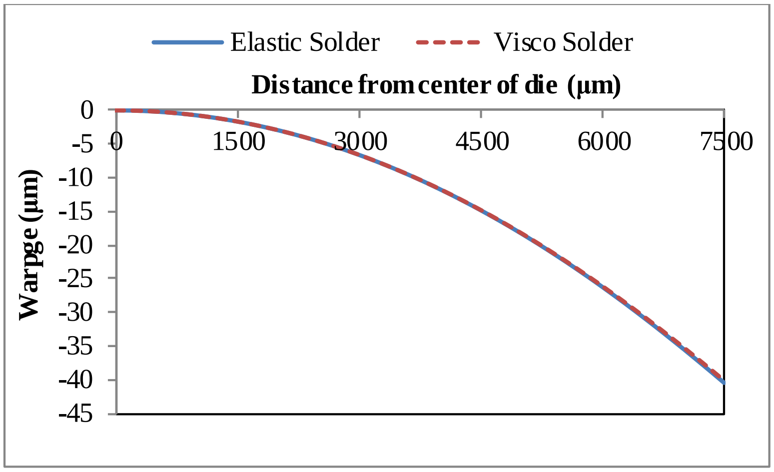


Figure 4-3. Global model warpage comparison between viscoplastic and elastic solder material

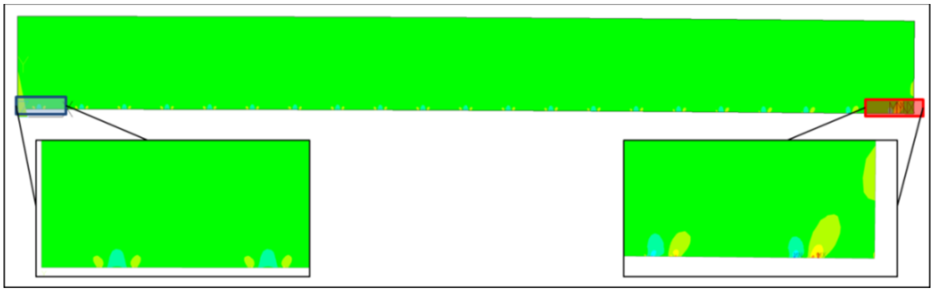


Figure 4-4. Peel stress (*y* direction) contour reveals variation from the center to the edge of the die at room temperature.

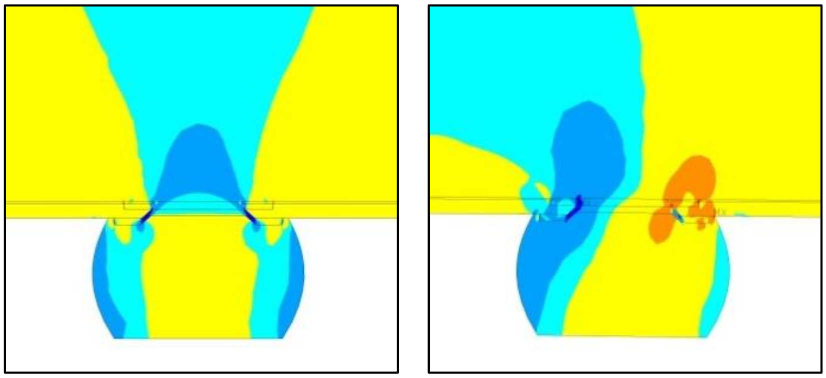


Figure 4-5. Peel stress (*y* direction) contour a) above center solder bump b) above corner solder bump. Shades of red/yellow indicates tensile stresses and shades of blue indicate compressive stresses

4.2.3 Local Model

Figure 4-6 shows the detailed schematic of the local model and the focused ion beam (FIB) cross-section of a solder bump from C45 device. As seen, the local model consists of the substrate and the die with all dielectric and metallization layers as well as the solder bump with the passivation layer. Figure 4-6 also shows a cohesive crack along ULK layer. The BEOL stack layer thickness is shown in Figure 4-1.

4.2.4 Global and Local Model Finite-Element Mesh

A mesh convergence study is first conducted on the global model by changing the mesh density and determining the displacements at regions of interest. Subsequently, a similar mesh convergence study is performed on the local model using the displacements, obtained from the global model, as boundary conditions for the local model. *G* is used as the convergence parameter for different mesh densities. Care is taken to ensure that all dielectric material layers in the local model have at least three rows of finite elements to capture bending effects. As the etch stop layers are extremely thin (8 nm), only one layer of elements is used to model the etch stop layers. The elements are designed such that their aspect ratio is within acceptable limits.

In addition to mesh density variations, different width and height of the local model are also employed to determine *G*, and thus, an appropriate size for the local model is determined such that the boundaries are at least one order of magnitude away from critical locations/dimensions in the model.

Quarter-point crack tip elements as well as highly-dense linear elements are used to model crack tip, and it is found that both types of elements yield similar values for *G* determined using virtual crack closure technique (VCCT). Thus, further studies are conducted using highly-dense linear elements, as the focus of this work is on *G*, and not on crack tip stresses. The local model mesh used for BEOL stack and various other materials along with the crack is shown in Figure 4-6.

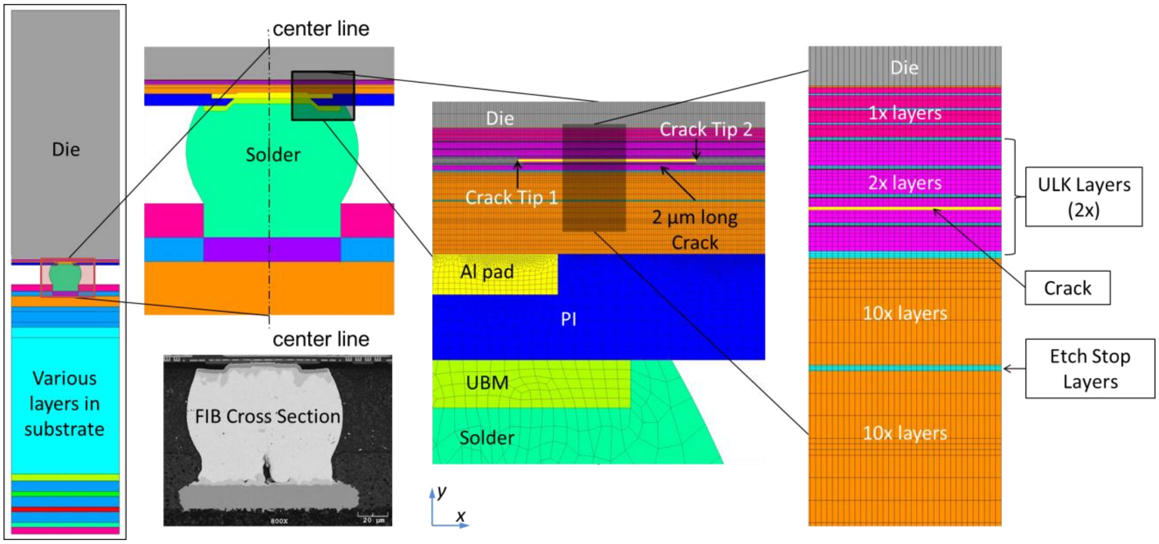


Figure 4-6. Detailed schematic of local model along with mesh and pre-existing crack above the critical location.

4.3 CRITICAL REGION PREDICTION

A 2 µm long crack is placed at various locations at the interface of two ULK dielectric layers processed sequentially, and the energy available for the crack to propagate (*G*) is calculated at both crack tips, shown in Figure 4-6. Crack Tip 1 will propagate toward the die center, while Crack Tip 2 will propagate toward the die edge. Also, as shown in the Figure 4-6, copper traces and vias present in the ULK layers are not modeled in this simulation. *G* is calculated using equation (2-6) for both the crack tips and is plotted as shown in Figure 4-6. The cross marks shown in Figure 4-7 indicate the locations at which the *G* at Crack Tip 1 and Crack Tip 2 is computed. The locations are chosen based on the peel stress profile under the corner solder bump. The embedded schematic in Figure 4-7 provides the distance of various points of significance from the die edge, and helps in visualizing the Crack Tip 1 position plotted along the *x*-axis. *G* calculated at Crack Tip 1 provides the energy available for the crack to propagate towards the center of the solder bump, while *G* calculated at Crack Tip 2 provides the energy available for the crack to propagate towards the edge of the die. It can be seen from Figure 4-7 that, *G* increases first and then decreases as we approach the solder bump center. The maximum *G* occurs above the Al pad edge (nearly 142.5 μm from the die edge). This shows that any flaw or a crack above the Al pad edge or the neighboring region have a higher energy for crack propagation, compared to the flaws present at other locations in the vicinity of a solder bump. As mentioned earlier, each bump is subjected to a moment therefore, the cracks present in tensile side of the bump have higher energy to propagate compared to the cracks present in the compressive side.

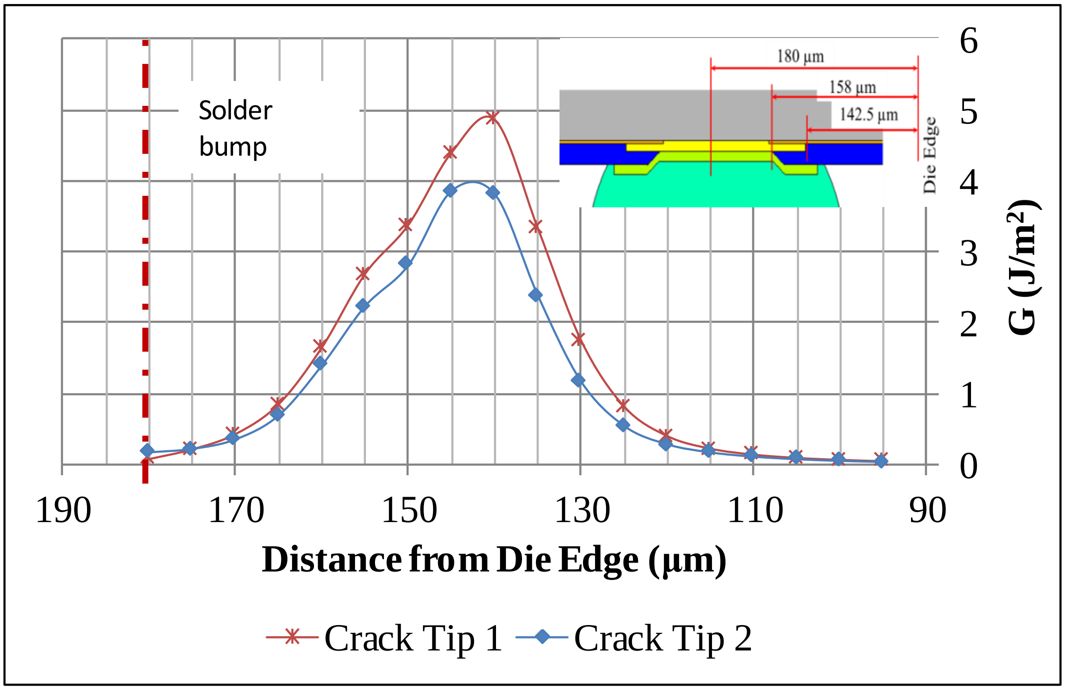


Figure 4-7. Energy release rate for a crack placed at various locations.

4.4 CRACK PROPAGATION SIMULATION

A cohesive crack is embedded in the ULK dielectric layer at the determined critical location (i.e.) above the Al pad and is simulated to propagate in either direction using nodal release technique. The criterion for crack propagation is set as $G \geq G_c$. The G_c of low-κ materials has been extensively researched. The G_c of 5 J/m^2 is estimated at room temperature for chemical mechanical polishing [22], cohesive fracture toughness is found to be 3.5 – 6 J/m^2 [114], G_c is found to vary between 0.5 – 3 J/m^2 based on loading angle [115] and between 1.8 – 2.4 J/m^2 [116] based on loading rates. In this chapter, critical energy release rate of 5 J/m^2 (G_c) is used, and this value is conservative and consistent with the lowest G_c value near Mode I, as measured and discussed in later chapters. It can be seen from Figure 4-8 that the energy available for the propagation of Crack Tip 1 has a similar profile as the one seen in Figure 4-7. The magnitude of G, however, is higher. This is because Figure 4-7 uses a crack of same length 2 μm for various locations, while results shown in Figure 4-8 is for a crack that is allowed to propagate using a failure criterion. It can be seen from Figure 4-8 that Crack Tip 1 propagated 45 μm and Crack Tip 2 propagated 40 μm. Figure 4-9 shows the mode-mixity during crack propagation. It can be seen that Crack Tip 1 propagates closer to mode I compared to Crack Tip 2. From Figure 4-7 and Figure 4-8, it is seen that the region spanning about 22 μm above the outer edge of Al pad is the critical region for crack initiation and propagation. However, once the crack propagates, the crack can grow to as much as 85 μm, as the G value is greater than G_c in this region.

4.4.1 Validation of Simulation Results

As mentioned earlier, the results from the simulation are compared against failure analysis (FA) results obtained from five C45 flip-chip devices. The die and substrate dimensions, the bump pitch and dimensions, and the BEOL stack layout and dimensions are identical to the flip-chip assembly modeled in Section 4.2, and therefore, the data from the experiments can be compared against simulation results. A typical focused ion beam (FIB) cross-section of a white-bump seen in a C45 device subjected to hammer test is shown in Figure 4-10. Figure 4-10a and Figure 4-10c reveal the location where Crack Tip 2 and Crack Tip 1 stop, respectively. Figure 4-10b shows the region above the Al pad and it can be seen that the crack is passing through the entire region. The crack is seen to propagate between 3rd and 4th ULK layer. FA results from various other tests like interfacial fracture test and nano-indenter based shear test reported in CHAPTER 5 and CHAPTER 9 respectively, also indicate that the crack travels in between 3rd and 4th ULK layer. Table 4-7 compares the results obtained from simulation with FA results from five units. As seen from Table 4-7, the simulations predict a crack length of 87 µm, while the five samples show an average crack length of 90 µm. Also, the simulations show that the Crack Tip 1 stops at a distance 185 µm from the die edge, while the samples show the Crack Tip 1 stops at an average distance of 199 µm from the die edge. Given the uncertainties in material and geometry modeling, the obtained results show reasonably good agreement. However, the starting and the ending location of the crack and thus the length of the crack are dependent on the value of G_c. For higher G_c value, the crack length will be smaller, and vice versa. Similarly, the energy available for crack propagation and thus the crack length are dependent on the modeling, geometry, and material assumptions. Although both the critical energy release rate (G_c) and the energy available for crack propagation (G) are dependent on such factors, in this study, it happens that for the chosen G_c values and modeling assumptions, the crack length is predicted with reasonable accuracy. However, regardless of the underlying assumptions, one can say that the trends presented in this work will still hold true.

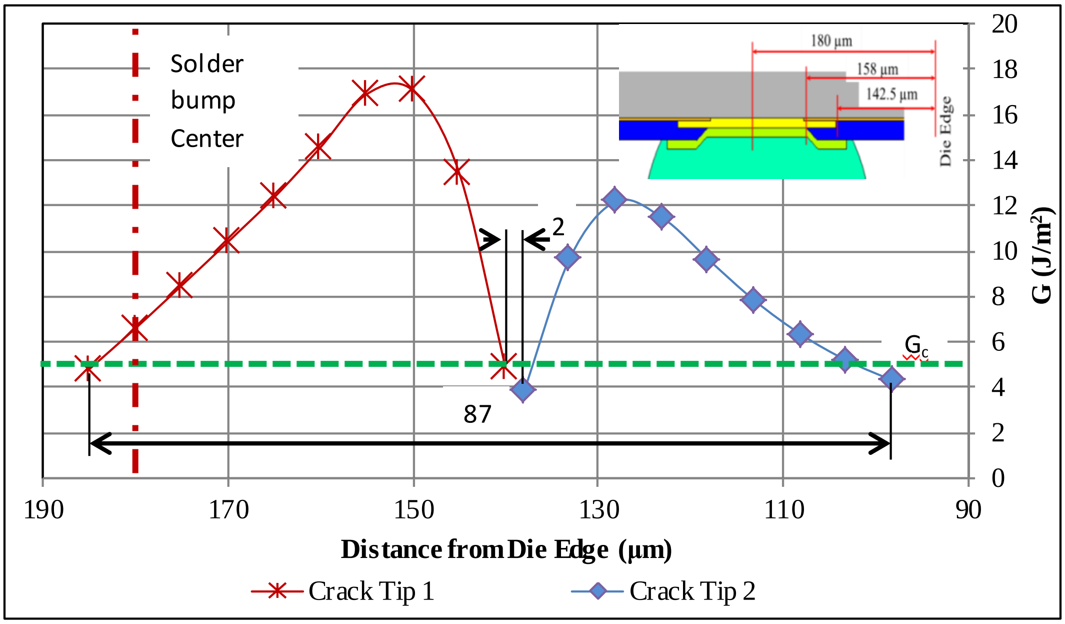


Figure 4-8. Energy release rate as the crack initiates from the critical location and propagates in either direction.

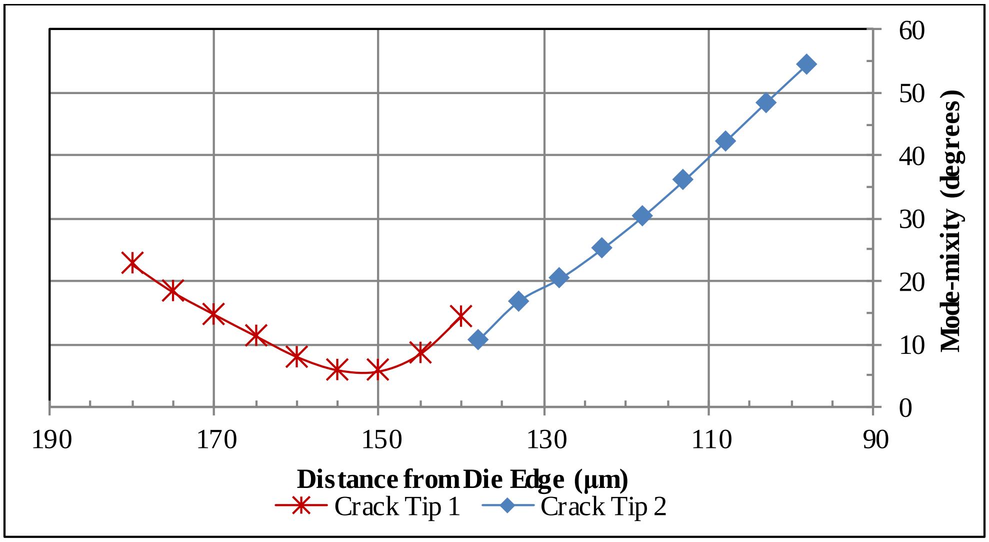


Figure 4-9. Mode-mixity during crack propagation

Table 4-7. Comparison of crack propagation simulation results with failure analysis (FA) results

		Crack Length (µm)	Distance from Die Edge (µm)	
			Crack Tip 1	Crack Tip 2
Simulation	**FEM**	87	185	98
FIB Cross-section of white bump	**Sample 1**	84	203	119
	Sample 2	62	186	124
	Sample 3	102	208	106
	Sample 4	103	217	114
	Sample 5	105	193	88
Experiment Average		90 ± 14	199 ± 13	108 ± 10

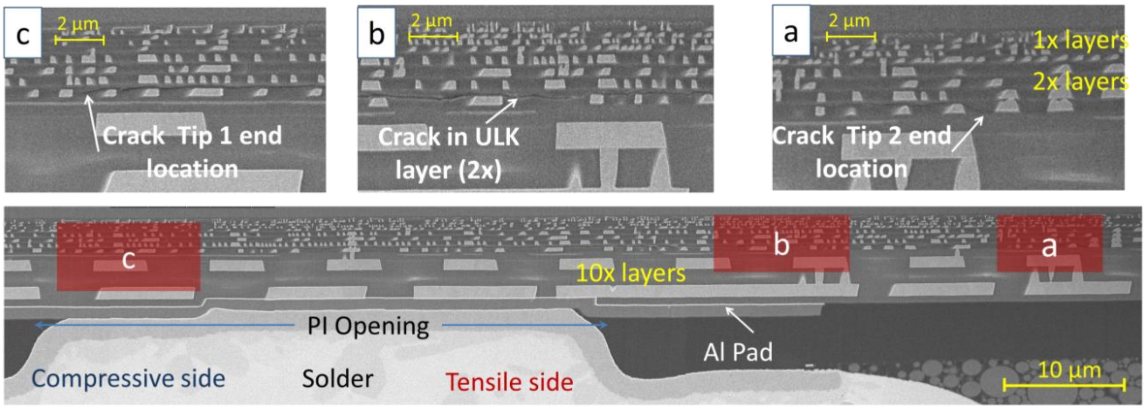


Figure 4-10. Focused ion beam (FIB) cross-section of a white bump (die edge is to the right of the picture and it is not shown). a) FIB cross-section of location where Crack Tip 1 ends, b) FIB cross-section of location above the Al pad showing the crack through the entire area, c) FIB cross-section of location where Crack Tip 2 ends.

4.5 DESIGN AGAINST CRACK GROWTH

In the following sections, the effect of "global" or "macro" parameters such as die thickness and substrate core material properties as well as the effect of "local" or "micro" parameters such as aluminum (Al) pad size and polyimide opening on the energy available for crack propagation is presented. The studies are conducted using 2 µm crack placed at various locations above the Al pad, as done in Figure 4-7. Based on the simulations, design guidelines for reducing the crack propagation are developed. As Crack Tip 1 has more energy available for crack propagation compared to Crack Tip 2, the following sections focus on energy available for Crack Tip 1.

4.5.1 Effect of Die Thickness

The global and subsequently the local model simulations are performed by varying the die thickness. The energy available for crack growth is calculated and plotted with respect to the distance of Crack Tip 1 from die edge as shown in Figure 4-11. In Figure 4-11, the x-axis shows the distance of the Crack Tip 1 from die edge and the y-axis shows the energy available for crack propagation G. Three die thickness values, namely 780 µm, 500 µm, and 300 µm, are considered as shown in Figure 4-11. The results reveal that G decreases by more than 60% as the die thickness is reduced from 780 µm to 300 µm. This is because as the die thickness is reduced, the overall compliance of the structure increases resulting in increased assembly warpage and thus reduces the energy available for crack propagation.

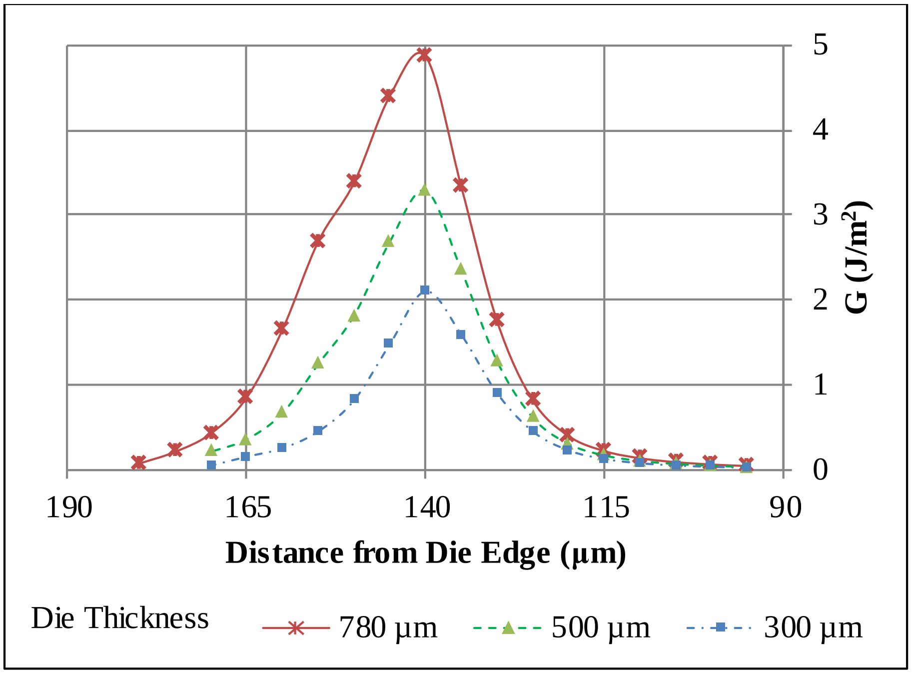


Figure 4-11. Effect of die thickness.

4.5.2 Effect of Substrate Core Properties

Table 4-8 presents the properties of a low-CTE core substrate, and the effect of this substrate on the energy available for crack propagation is studied. As shown in Figure 4-12, the results obtained are compared against standard core substrate having an in-plane CTE of 16 ppm/°C below T_g and 12 ppm/°C above T_g. Detailed orthotropic properties of the standard core substrate are provided in Table 4-3. As expected, the model predicts that a low CTE core substrate results in lower risk of crack propagation. It can be seen from Figure 4-12 that reduction in in-plane CTE by 37.5% results in more than 40% reduction in *G*.

Table 4-8. Low CTE core substrate material properties [Freescale Semiconductor]

Temperature (°C)	30	95	125	150	270
E (GPa)	32.8	31.2	28.8	27	20.6
ν	0.143	0.143	0.143	0.143	0.143
α_x, α_z (ppm/°C)	10	10	10	10	6
α_y (ppm/°C)	22	22	22	22	97

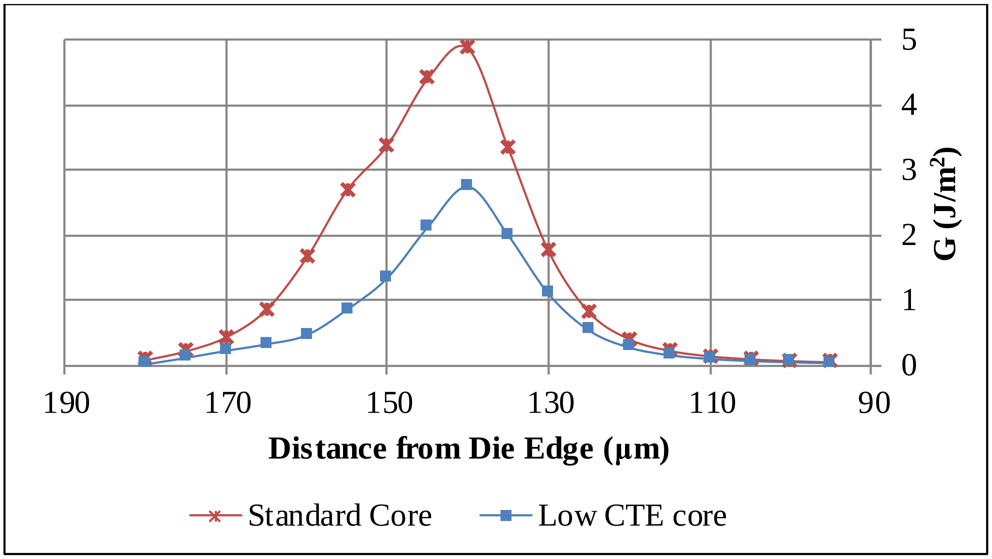


Figure 4-12. Effect of substrate core material properties.

4.5.3 Influence of Local Parameters on Cohesive Crack Propagation

Figure 4-13 and Figure 4-14 show the aluminum pad size and the PI opening size, respectively, along with the distance from the die edge. Figure 4-15 shows that as the Al pad size approaches the PI opening, *G* value above the Al pad edge increases because of super-position of peel stresses above the Al pad and PI opening. On the other hand, if the Al pad is much larger than the PI opening, the risk of failure reduces. Thus, increase in Al pad size from 75 μm to 100 μm results in approximately 34% reduction in *G*. Figure 4-15 also shows that the magnitude of *G* above PI edge remains constant regardless of Al pad size.

Keeping the Al pad size to be 100 µm, it is seen from Figure 4-16 that G above PI edge reduces by 50% when the PI opening is reduced from 47 µm to 30 µm. Also it can be seen from Figure 4-16 that, the peak value of G shifts from above PI edge to above the Al pad edge. In addition, the reduction in PI opening also reduces G above the Al pad edge by 12%.

Based on the above two simulations, it is seen that it is beneficial to design the Al pad and the PI opening such that their edges do not vertically align, and the edges be separated from each other as much as possible.

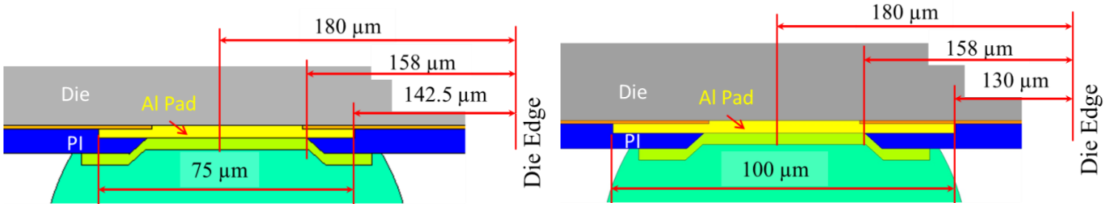


Figure 4-13. Distance from die edge. Al pad size increased. PI opening = 47 µm.

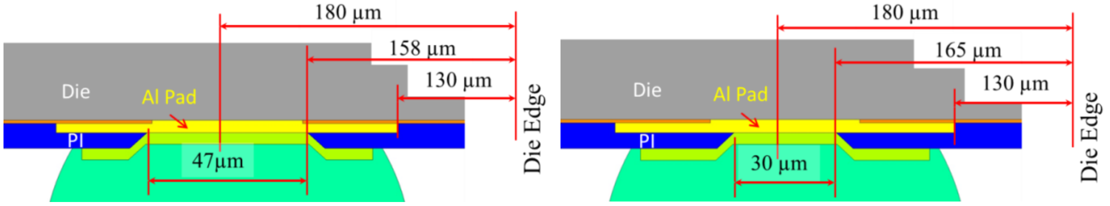


Figure 4-14. Distance from die edge. PI opening increased. Al pad size = 100 µm.

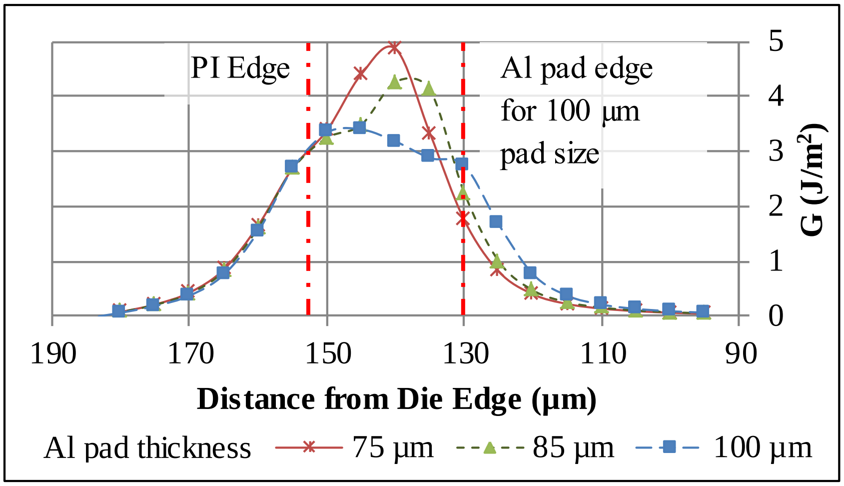


Figure 4-15. Effect of increase in Al pad size

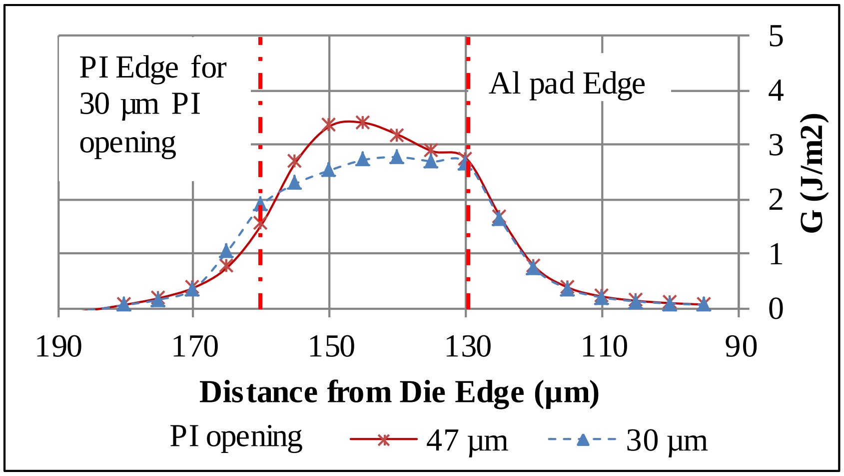


Figure 4-16. Effect of reduction in PI opening

4.5.4 Parameter Interaction

Furthermore, interactions between the chosen global and local parameters are studied by performing simulations. Full factorial simulations considering two levels of die thickness, CTE of core material, Al pad size and PI opening are performed. The maximum *G* (above the Al pad edge) is determined and is shown in Table 4-9. The percentage reduction in *G* compared to the base case (Case No. 6) is also shown in Table

4-9. It can be seen from Case No. 11 that, when lower CTE substrate core, lower die thickness, larger Al pad size and smaller PI opening are used, *G* reduces by 90%. Also, the result from Case No. 12 reveals that more than 75% reduction in *G* can be achieved if lower die thickness along with lower CTE substrate core material is employed in flip-chip assembly. This shows that the global parameters have a greater role in reducing the fracture parameter.

Table 4-9. Parameter interaction, showing effect of various global and local parameters on *G*

Case No.	Core Type	Die Thick (μm)	Al Pad Size (μm)	PI Open (μm)	*G* (J/m^2)	%Reduction in *G* compared to case 6
1	Standard	300	75	30	1.8	64%
2	Standard	300	75	47	2.1	57%
3	Standard	300	100	30	0.9	82%
4	Standard	300	100	47	1.1	77%
5	Standard	780	75	30	4.4	10%
6	Standard	780	75	47	4.9	0%
7	Standard	780	100	30	2.8	43%
8	Standard	780	100	47	3.2	35%
9	Low CTE	300	75	30	0.8	84%
10	Low CTE	300	75	47	1.0	79%
11	Low CTE	300	100	30	0.3	94%
12	Low CTE	300	100	47	0.4	91%
13	Low CTE	780	75	30	2.3	52%
14	Low CTE	780	75	47	2.7	44%
15	Low CTE	780	100	30	1.3	74%
16	Low CTE	780	100	47	1.6	68%

4.6 SUMMARY

A finite-element simulation study focusing on underbump delamination during flip-chip assembly is presented in this chapter. A small crack was placed at various locations above the solder bump to determine the critical locations. It is found that a crack present in the region above the die pad edge (tensile side of the bump) has the maximum energy to propagate. Assuming the critical energy release rate of ULK material to be 5 J/m^2, the calculated energy release rates are in the expected range to explain the interlayer dielectric cracks commonly found in BEOL stacks. Energy release rate curves obtained from local model simulations are consistent with peel stress profiles observed in global model. Crack propagation simulations are performed by initiating a crack from the critical location and results are also compared against failure analysis performed on 45nm devices with reasonable accuracy. Furthermore, the results reveal a decreased risk for thinner die, lower CTE core substrate material, larger Al pad size and lower PI opening. Also, studies performed on parameter interaction revealed that global parameters have the maximum impact on the energy available for crack propagation, and thus, the risk of ultra-low-κ cracking.

4.7 LIMITATIONS OF FRACTURE MECHANICS APPROACH

Fracture mechanics based simulations presented in this chapter predict the critical region above the solder bump during reflow simulation and provide insights on favorable design changes to reduce white-bump risk. However, such an approach has several limitations. The initial crack length assumed to determine the critical region and G_c of 5 J/m^2 used in crack propagation criteria can affect the results significantly. The simulations are time consuming, for example each data-point presented in Figure 4-7 and

Figure 4-8 is a separate simulation iteration. Furthermore, if cracking through multiple layers needs to be simulated then the FE model needs to be re-meshed after each iteration. This significantly increases the time to obtain the final solution and complexity in modeling. In this study, traces and vias are not modeled. To repeat this study by considering trace metal pattern and metal density with plastic material behavior for copper present in the traces, can be computationally and memory wise be much more expensive. As well as, since LEFM does not hold true in such situations, equations have to be modified considering the effect of plastic deformation of copper at the crack tip. Also, to implement a methodology described in this chapter to study 3D crack propagation can be even more complex.

CHAPTER 5

COHESIVE LAW EXTRACTION: EXPERIMENTAL METHODS

5.1 INTRODUCTION

Cohesive zone modeling is a popular alternative to the fracture-mechanics based approach. Cohesive zone modeling (CZM) is a phenomenological approach wherein the singular stresses ahead of the crack are replaced by a cohesive zone, a fictitious extension of the crack tip. The stresses within the zone are characterized as a function of crack tip opening displacements using traction-separation (T-δ) law. As mentioned in CHAPTER 2, bilinear T-δ law is used in this work and six independent parameters are required to fully characterize the mixed-mode bilinear law. The parameters that define the T-δ law are often referred as cohesive zone parameters.

Cohesive zone parameters can be determined directly from tensile test experiments or through indirect method, known as the inverse method. The major challenges that render direct experimental measurements of CZM parameters nearly impossible are: crack initiation location is unknown, multiple crack initiation due to material inhomogeneity, ductile materials/interfaces undergo extensive plastic deformation before crack propagation, even a controlled sample preparation and testing conditions can result in unstable crack propagation [60]. Also, in this work, crack propagates through sub-micron thick layers and creating macroscopic tensile test specimen is impossible. Therefore, the inverse analysis to fit simulation results to experimental load-displacement or load-COD (crack opening displacement) is the preferred method to determine CZM parameters [117-119].

The objectives of this chapter are to

- Develop appropriately modified experimental characterization techniques to study interfacial crack propagation in sub-micron layers.
- Use FPB test to create a starter delamination in sub-micron layer BEOL stack
- Use the sample with starter delamination created by FPB test to perform DCB tests and 3ENF tests to determine the critical energy release rate at different mode-mixities.

5.2 EXPERIMENT SAMPLE PREPARATION

In this thesis, DCB, FPB, 3ENF tests are performed using a sandwich test specimen because the experiments are reliable, simple to perform, require minimal post-processing and yield repeatable results. Also, the advantage of bend tests performed using sandwich specimen is that the fracture parameter does not depend on the property of the thin-films through which the crack propagates. As seen from equations (5-1) through (5-4), the fracture parameter (G_c) depends only on the properties of the substrate.

The samples obtained for the study are diced from 300 mm (12") wafer with 45nm (C45) technology node devices and BEOL stack fabricated on the wafer. First, the wafer is diced such that each sample is of one die width and has four dies along its length, as shown in the inset in Figure 5-1. Each singulated piece is 65 mm long, 12 mm width, and 0.78 mm thick, as shown in Figure 5-2. Dicing is done along the sawing streets that have crack-stop structures on both sides, as indicated in Figure 5-1 and Figure 5-2. These crack-stop structures ensure that cracks do not propagate into the dies when individual dies are diced or singulated from a larger silicon wafer. As shown in the schematic in Figure 5-1, all dies have crack-stop structures around them and no starter crack is pre-fabricated. As shown in Figure 5-2, solder bumps are present in all samples. Therefore, a process flow shown in Figure 5-3 is employed for sample preparation and testing. As illustrated in Figure 5-3, solder bumps on the sample are removed by fine polishing. The surface of the test sample with the bumps and after removing the bumps is shown in Figure 5-4. Then, the test sample is glued onto a dummy sample using epoxy (EPOTEK-301™) to obtain a sandwich specimen. Fine polishing the sides of the sandwich specimen is a critical step to get rid of the micro-cracks generated during dicing. Unpolished samples resulted in premature breakage of the sample before the crack propagated along one of the layers when bending tests are performed. A notch of 700-750 µm depth is made on the polished test sample as shown in Figure 5-5 to create a four-point bend notched specimen, with the notch depth covering nearly 95% of the die thickness. The notch is made using *DISCO DAD 321* automatic dicing saw. As shown in the inset in Figure 5-1, the notch is centered between two crack-stop structures. The reason for centering the notch between two crack-stop structures is explained in the next section.

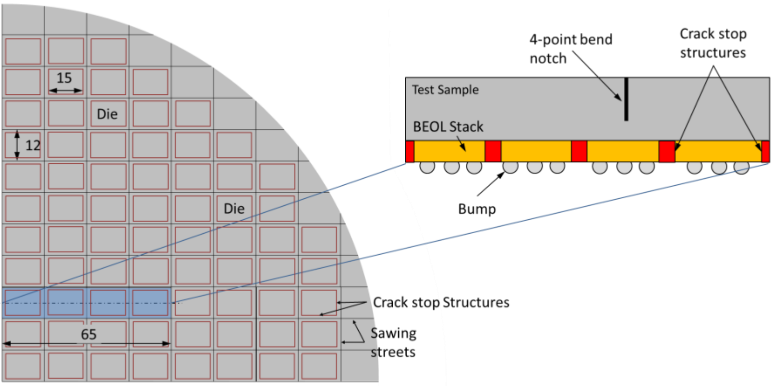


Figure 5-1. Schematic of quarter wafer with dicing streaks. Inset: Typical sample containing 4 dies with crack strop structures in-between.

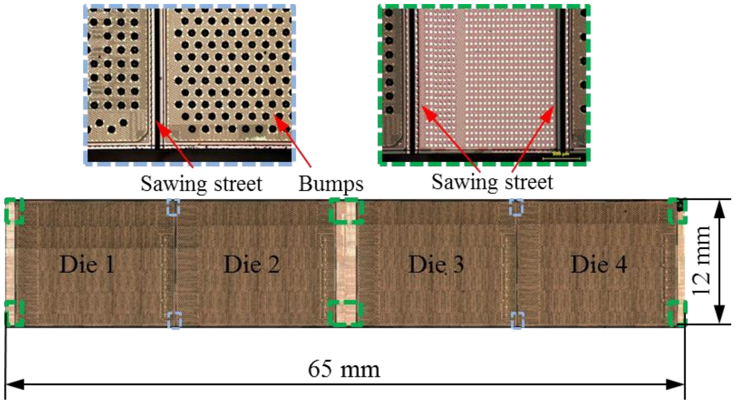


Figure 5-2. Test sample

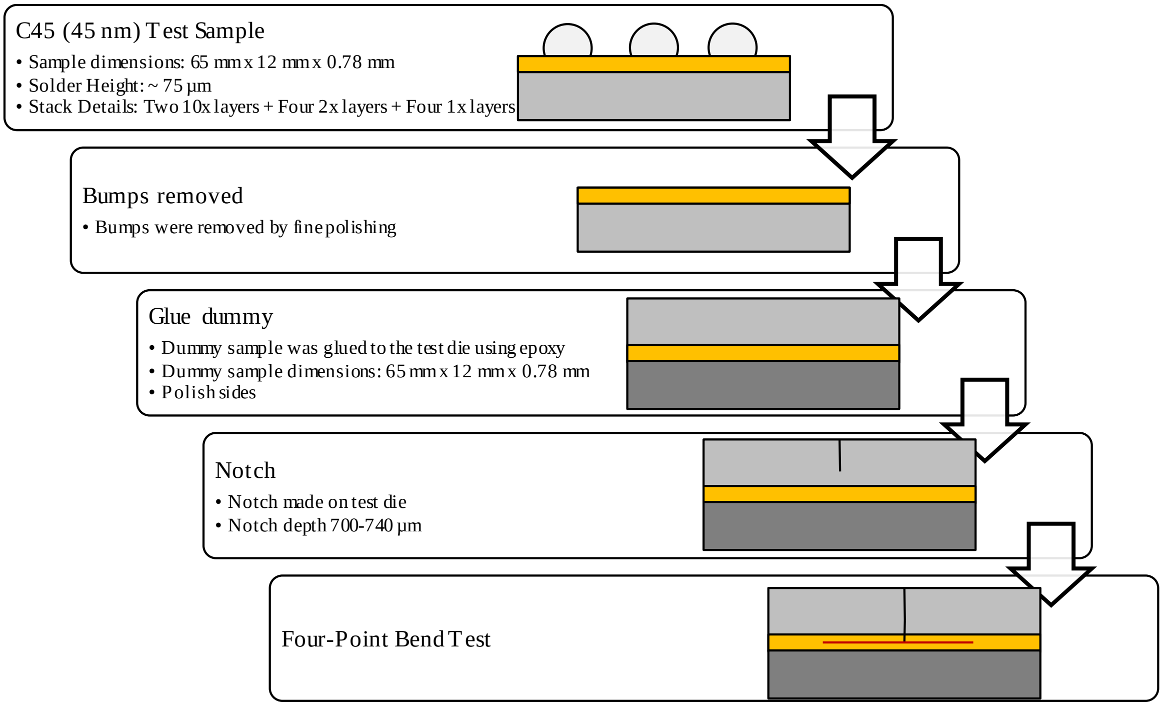


Figure 5-3. Steps involved in sample preparation for DCB and FPBT

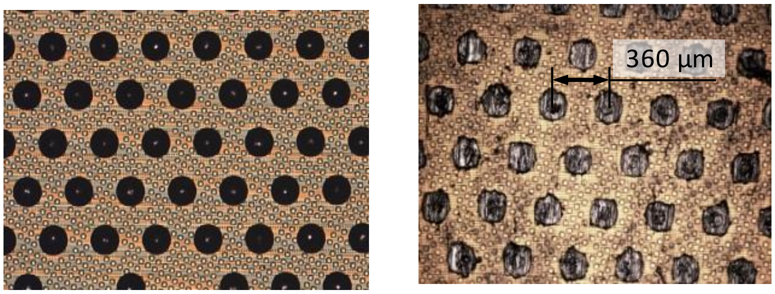


Figure 5-4. Sample surface with bumps and after fine polishing of bumps

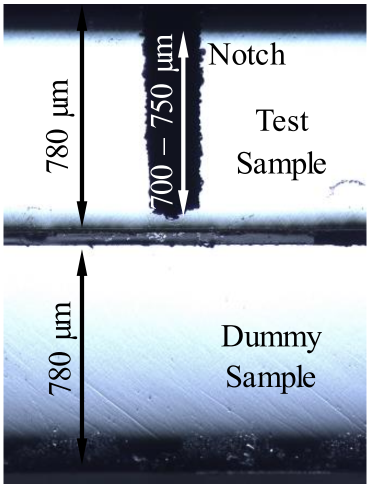


Figure 5-5. Sides of the sample polished then notched

5.3 FOUR-POINT BEND TEST EXPERIMENT

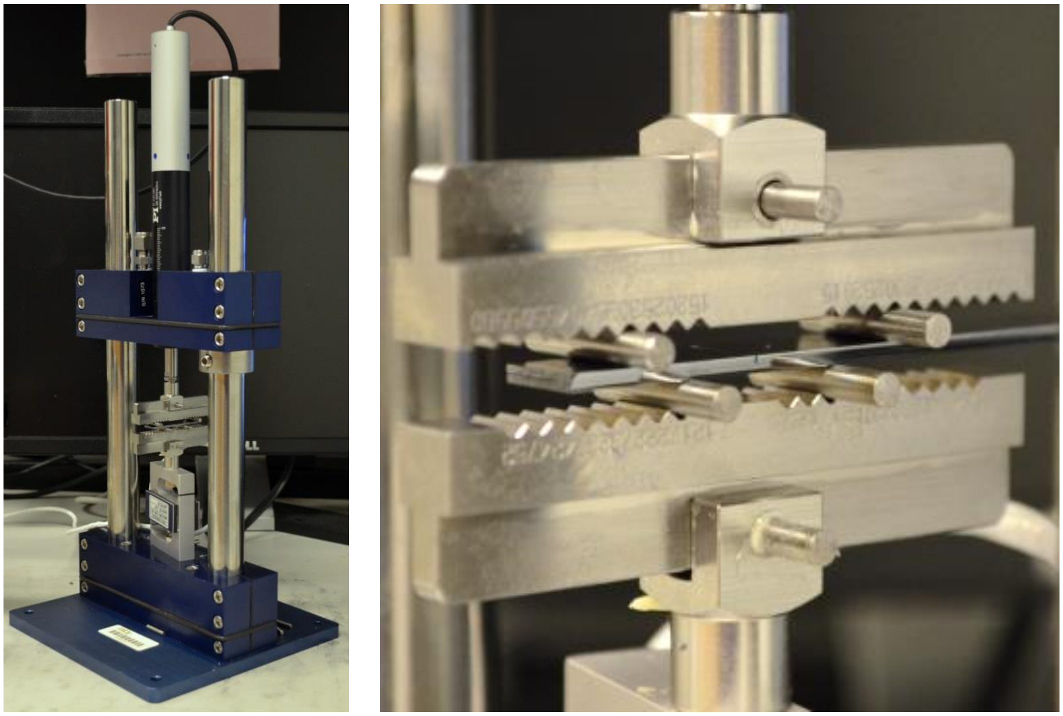


Figure 5-6. Four-point bend test experiment setup

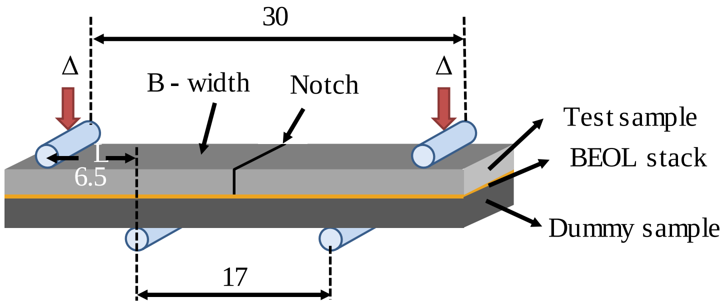


Figure 5-7. Four-point bend test schematic.

Figure 5-6 shows the experimental four-point bend test setup. Figure 5-7 shows the schematic of the FPB test setup with dimensions. As shown in Figure 5-7, displacement is applied on the two outer pins. A typical load-displacement curve, obtained from FPB test is shown in Figure 5-8. During the test, a crack initiates from the root of the notch and travels into the BEOL stack, indicated by the kink in the initial loading curve, marked by a red circle in Figure 5-8. Once the crack finds the weakest layer [103], it starts propagating along the layer parallel to the length of the specimen. Figure 5-9 shows the SEM image of a crack initiating from the notch and traveling through the interface of interest. Therefore, it is critical to create the notch between two crack-stop structures, so that crack can travel a sufficient distance before being stopped by these structures. Since crack of known size and geometry cannot be introduced during wafer fabrication, the crack generated by FPB test is used as the starter crack for DCB and 3ENF tests.

The load remains constant as the crack propagates with respect to the applied displacement as long as the crack stays within the two inner pins, since the moment remains constant between the two inner pins, as seen in Figure 5-8. Therefore, the energy release rate attains a steady state value as long as the crack stays within the two inner pins. As seen from the experimental setup shown in Figure 5-6, a rotational degree of freedom is provided to the loading fixture. This ensures that the pins adjust themselves during asymmetric crack propagation about the notch to keep the load balanced [120]. Therefore, as long as the crack stays within the two inner pins, the energy release rate remains constant irrespective of symmetric or asymmetric crack propagation about the notch. The steady state energy release rate for FPB test (G_{FPB}) is given by [103],

$$G_{FPB} = \frac{21(1-\nu^2)P^2L^2}{16EB^2H^3} \tag{5-1}$$

where, P is the load at which steady state crack propagation is achieved indicated by plateau in P-δ curve and L is the distance between inner and outer loading pins. Also, since steady state crack propagation with constant load is achieved between the two inner pins, G_{FPB} does not depend on the crack length 'a' as seen from equation (5-1).

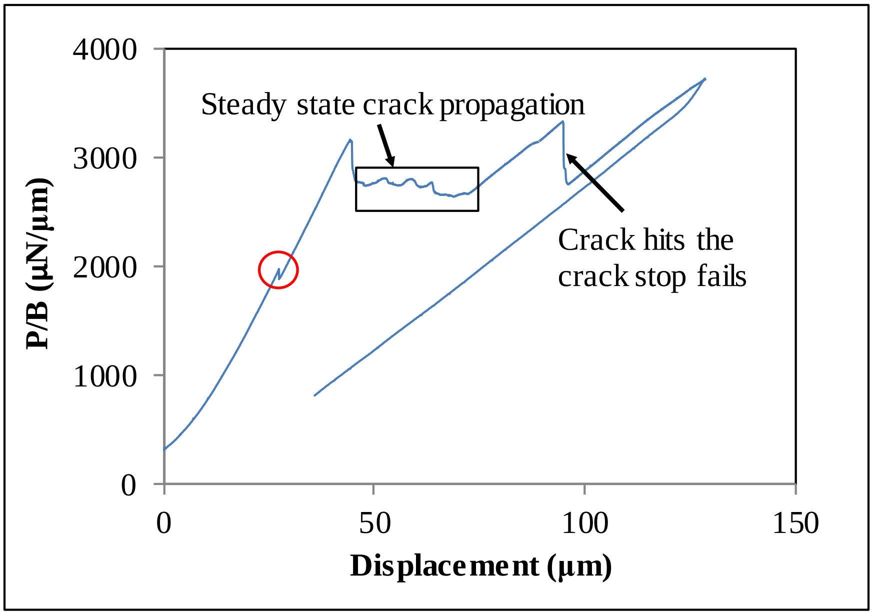


Figure 5-8. Typical four-point bend test load-displacement curve.

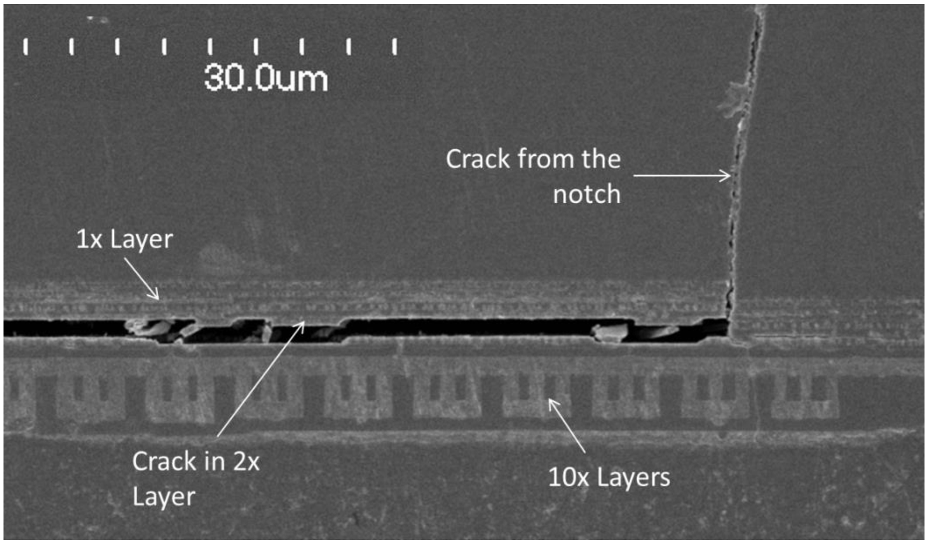


Figure 5-9. SEM image showing crack propagating in 2x layer at the end of FPB test.

Figure 5-10 shows the load-displacement curves obtained from five samples and the Table 5-1 summarizes the results obtained from ten samples. The average G_{FPB}, obtained from ten samples is 7.15 ± 1 J/m^2.

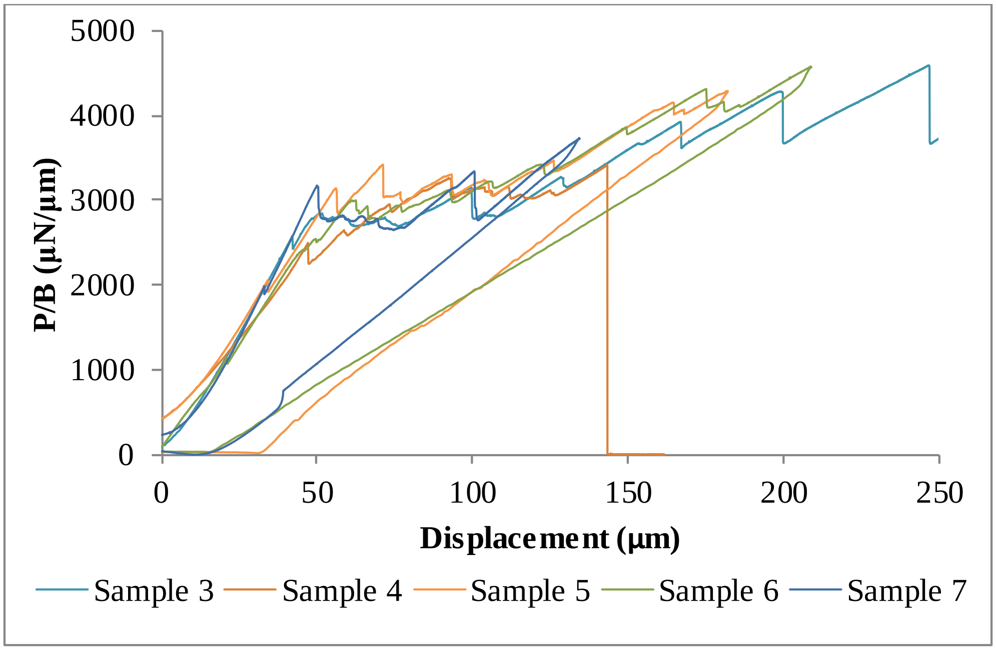


Figure 5-10. FPB test load-displacement results

Table 5-1. FPB test results summary

Name	L (dist b/w pins) (µm)	B (µm)	P_c (N)	P_c/B (µN/µm)	G_{FPB} (J/m^2)
Sample 1	10000	10400	21	2004	7.97
Sample 2	10000	8990	16	1725	5.90
Sample 3	6500	9950	28	2814	6.64
Sample 4	6500	8050	25	3106	8.08
Sample 5	6500	9560	29	3033	7.71
Sample 6	6500	8980	25	2784	6.50
Sample 7	6500	9400	26	2766	6.41
Sample 8	4000	8300	39	4699	7.01
Sample 9	6500	9550	28	2932	7.20
Sample 10	6500	8350	26	3114	8.13
				Average	7.15

It can be seen from Table 5-1 that G_{FPB} values are fairly consistent across multiple samples. This indicates that the mechanical polishing step to remove the solder bumps during sample preparation does not affect G_{FPB} significantly. Load-displacement curve across several samples does not indicate any evidence of environmentally-assisted cracking/corrosion. Although not directly of interest in this study, it can be seen from Figure 5-8 that once the crack hits the crack-stop structures, the load begins to rise and the failure of crack-stop structures is indicated by a sudden drop in the load. The sample is then carefully unloaded and it can be seen from Figure 5-8 that the loading curve is stiffer than the unloading curve indicating that the crack has propagated and the specimen is more compliant.

5.4 DOUBLE CANTILEVER BEAM TEST EXPERIMENT

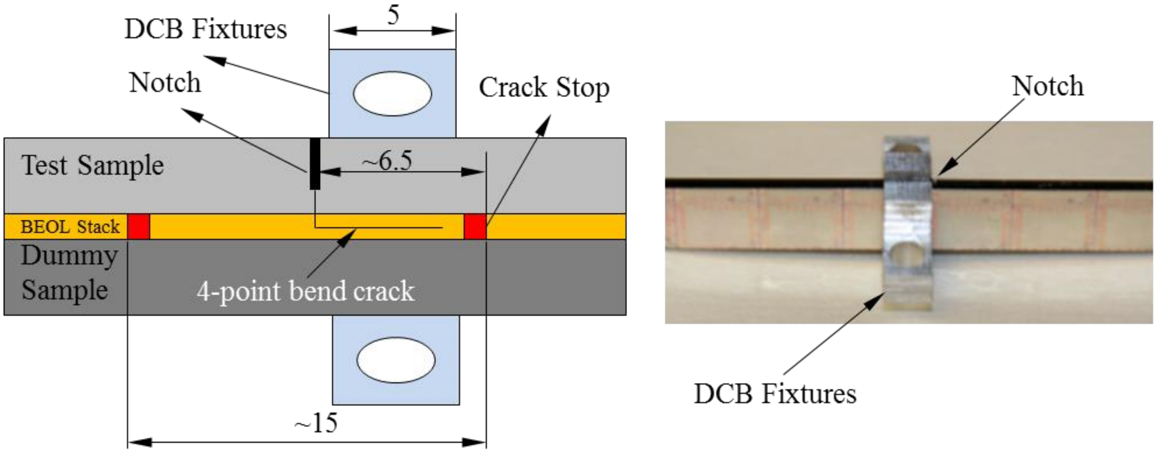


Figure 5-11. a) Schematic of DCB sample (all dimensions in mm – not to scale)

b) DCB sample

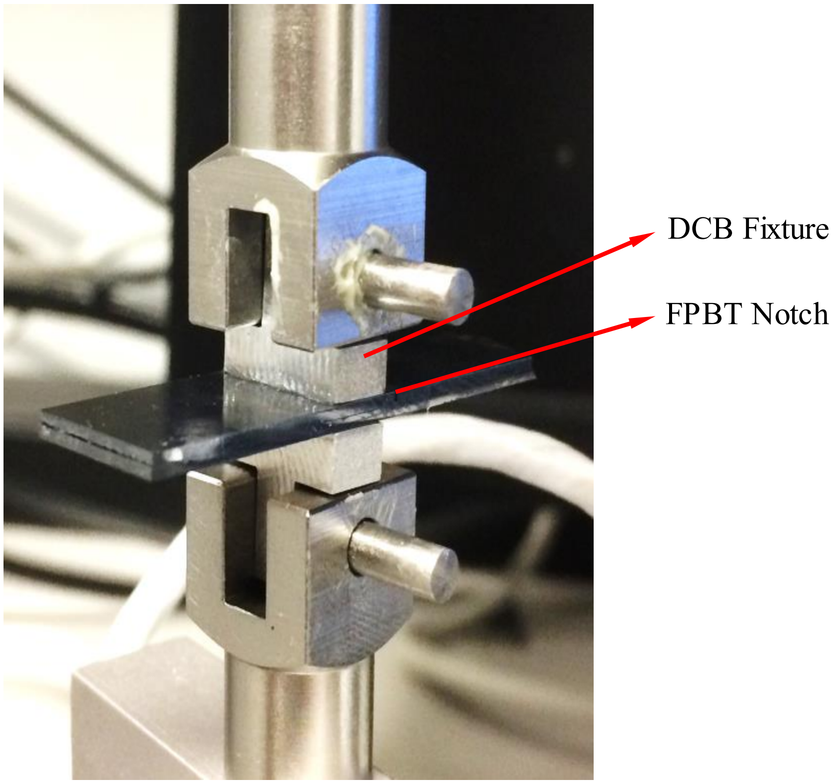


Figure 5-12. DCB experiment setup

The crack created by four-point bend test is used as the starter crack for the DCB test, since there is no pre-fabricated starter crack. Therefore, fixtures are attached on either side of the sample as shown in Figure 5-11. The sample is loaded on the test setup as shown in Figure 5-12. The sample is then subjected to DCB testing. The energy release rate (G_{DCB}) under symmetric loading for DCB test (N/µm) derived from beam bending theory is given by [121],

$$G_{DCB} = \frac{12(1-\nu^2)P^2a^2}{EB^2H^3} \tag{5-2}$$

where, ν is the Poisson's ratio, a is the crack length in µm, E is the Young's modulus of the substrate (N/µm^2), B and H is the width and thickness of the substrate respectively (µm), and P is the critical load at which load-displacement curve becomes nonlinear (N).

The test requires pre-crack of known length, as seen in equation (5-2). Since the BEOL stack layers are hundreds of nm thick, the displacement of the fixtures is expected to be in hundreds of µm, optical measurement of crack length as the testing progresses is very difficult. Therefore, compliance calibration method is used for finding the crack length [43, 121]. In this approach, once the crack begins to propagate the sample is unloaded and re-loaded. The crack propagation is indicated by drop in load in the load-displacement curve. The compliance of the unloading curve given by equation (5-3) can then be used to find crack length [122], as explained below.

Figure 5-13 shows the load-displacement curve from one of the three DCB samples. As seen, the load increases with the applied displacement and suddenly drops when the crack begins to propagate. The sample is unloaded at this juncture and the stiffness is calculated using the unloading curve as indicated in Figure 5-13. The sample is then reloaded, and the loading-unloading cycle is repeated until the sample fails. It can be seen that after each unloading cycle the stiffness decreases. In other words, the compliance increases and the crack length can then be determined from the measured compliance using equation (5-3).

$$C = \frac{\delta}{P} = \frac{8\,a^3}{EBH^3} + \frac{12a}{5BH\mu} \tag{5-3}$$

where, C is the compliance obtained from the load (P) – displacement (δ) curve, a is the crack length, E is the Young's modulus of silicon substrate, B is the width, H is the thickness of the dummy specimen, respectively, and μ is the shear modulus of the dummy specimen given by, $E/(2(1+v))$. It can be seen that the Timoshenko shear component is considered in crack length measurements. The only unknown parameter is the crack length 'a' which can be determined from the measured compliance, material properties and dimensions. It should be pointed out that since $a > H$ the error in not considering the shear component to measure crack length is not significant.

As shown in Figure 5-13, one sample is loaded and unloaded several times, and thus crack lengths are determined using increasing compliance of the sample. Thus, one sample can give multiple G_{DCB} data points for various crack lengths.

Table 5-2 summarizes the results obtained from three samples and the average G_{DCB} of 4.62 J/m^2 will be used for determining cohesive zone parameters. It should be pointed out that G_{DCB} values determined using cracks less than 6.5 mm long are not appropriate to use, as they would include crack-stop structures fracture as shown in Figure 5-11. Therefore, Table 1 shows G_{DCB} values for cracks longer than 6.5 mm.

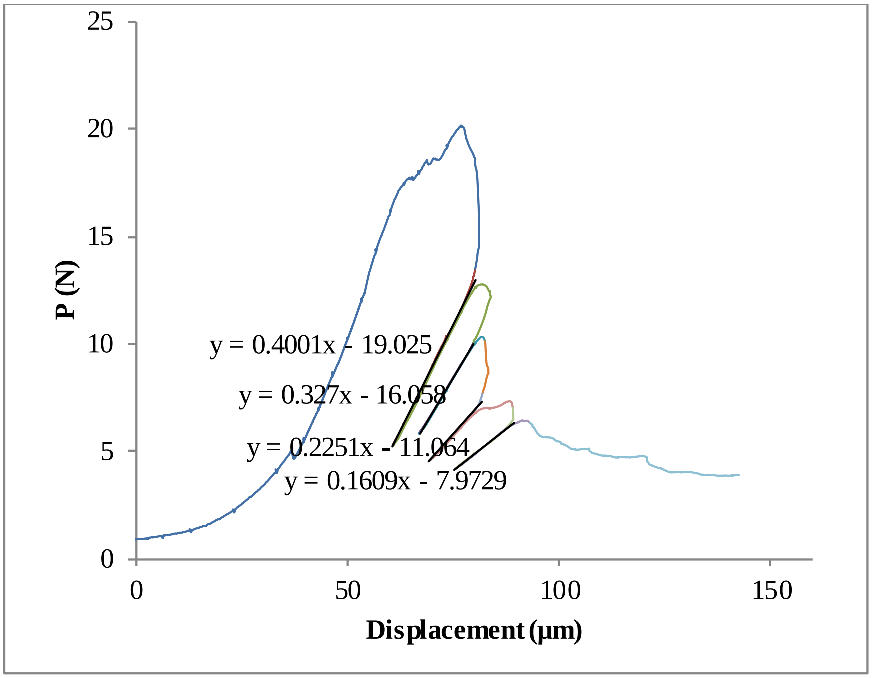


Figure 5-13. DCB P-δ Curve Sample 3

Table 5-2. DCB Results summary

Sample	**B (µm)**	**Compliance (µm/N)**	**Crack Length (a) (µm)**	**P_c (N)**	**G_{DCB} (J/m^2)**
1	10400	4.47	7081.33	5.93	3.18
1	10400	11.78	9796.3	5.42	5.09
2	8990	9.14	8571.49	4.97	4.37
3	8800	4.44	6682.38	6.76	5.14
3	8800	6.22	7478.87	6.14	5.31
			Average		4.6

5.5 THREE-POINT END NOTCH FLEXURE TEST EXPERIMENT

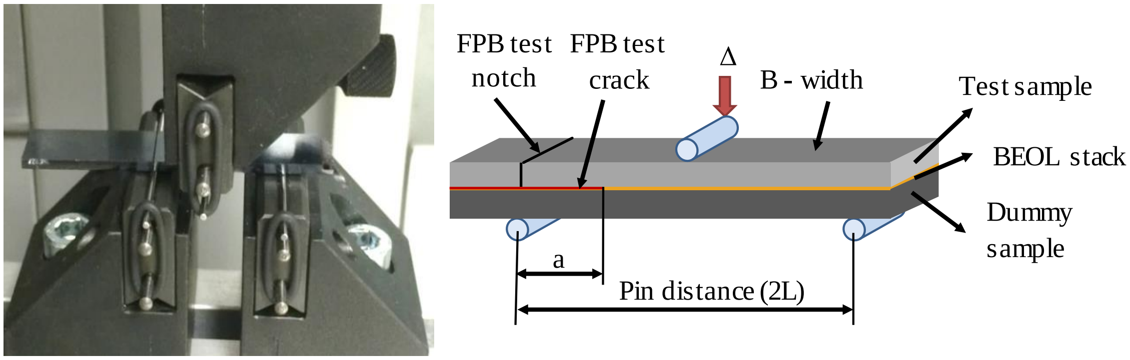


Figure 5-14. a) 3ENF test setup. b) 3ENF test schematic

Similar to the DCB test, crack generated by FPB test is used as the starter crack for three-point end notch flexure (3ENF) test, as shown in Figure 5-14b. Initial length of the crack is calculated from the compliance of unloading segment of P-δ curve obtained from FPB test, as shown in Figure 5-15a. A 2D fracture mechanics based finite-element model of the FPB test is created and a crack of known length is placed along the weakest layer determined from experiments. The compliance of the structure is determined, then the procedure is repeated for different crack lengths and the results are plotted. As expected, a linear relationship between crack length and compliance is obtained as shown in Figure 5-15b. The compliance versus crack length relationship can then be used to find the initial crack length using the experimental compliance value.

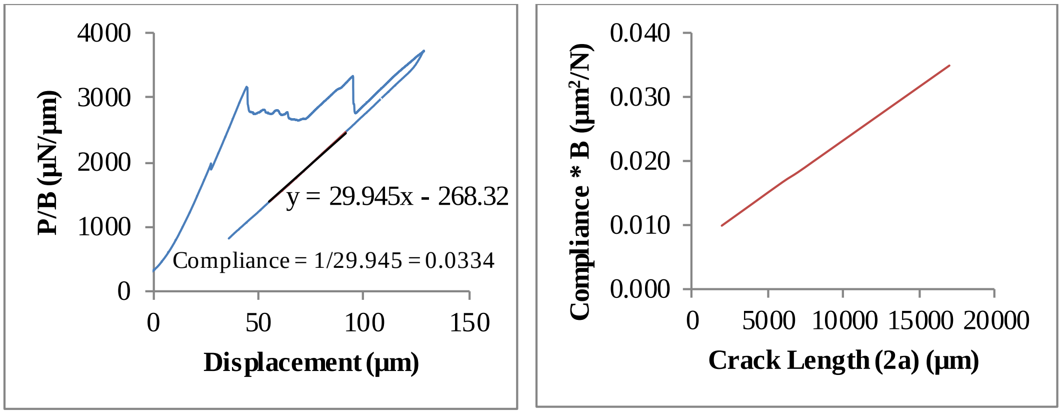


Figure 5-15. a) FPB test load-displacement curve with unloading compliance. b) Compliance as a function of crack length obtained from FPB test FE simulations.

As shown in Figure 5-14a, the 3ENF test is performed by resting one of the pins along the notch. The P-δ curve obtained from 3ENF test is shown in Figure 5-16. Since the initial crack length is close to an order higher than the thickness of the sample (0.78 mm), elementary beam theory is assumed to be valid. The critical load (P) where the unstable crack propagation begins is indicated by a sudden drop in the load and P is used for the G_{ENF} computation using equation (5-4).

The schematic of the 3ENF test is shown in Figure 5-14b. G_{ENF} for an ENF specimen with a span of $2L$, a known crack length a and loaded at the center based on beam theory is given by [123],

$$G_{ENF} = \frac{9(1-\nu^2)P^2a^2}{16EB^2H^3} \tag{5-4}$$

where, P is the critical load at which unsteady crack propagation begins, E is the Young's modulus of silicon, H is the thickness and B is the width of the dummy specimen. Initial crack length from FPB test experiment, the distance between the outer pins, the critical load obtained from 3ENF test and G_{ENF} value are shown in Table 5-3. An average value of 22.1 J/m^2 will be used for cohesive zone element characterization.

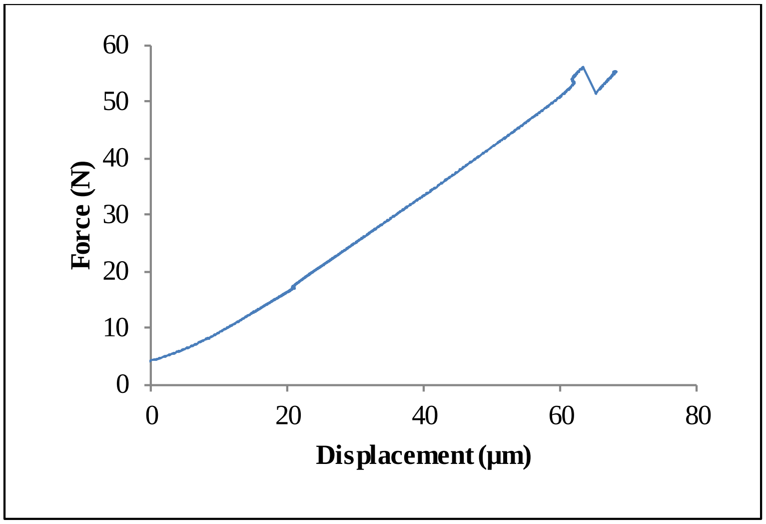


Figure 5-16. 3ENF P-δ Curve Sample 1

Table 5-3. Three-point end notch flexure (3ENF) test results

Sample	**Pin distance (mm)**	**B (mm)**	**a (mm)**	**P (N)**	G_{ENF} **(J/m^2)**
1	20	9.55	8.03	56	20.3
2	16	9.55	6.36	77	24

5.6 FAILURE ANALYSIS

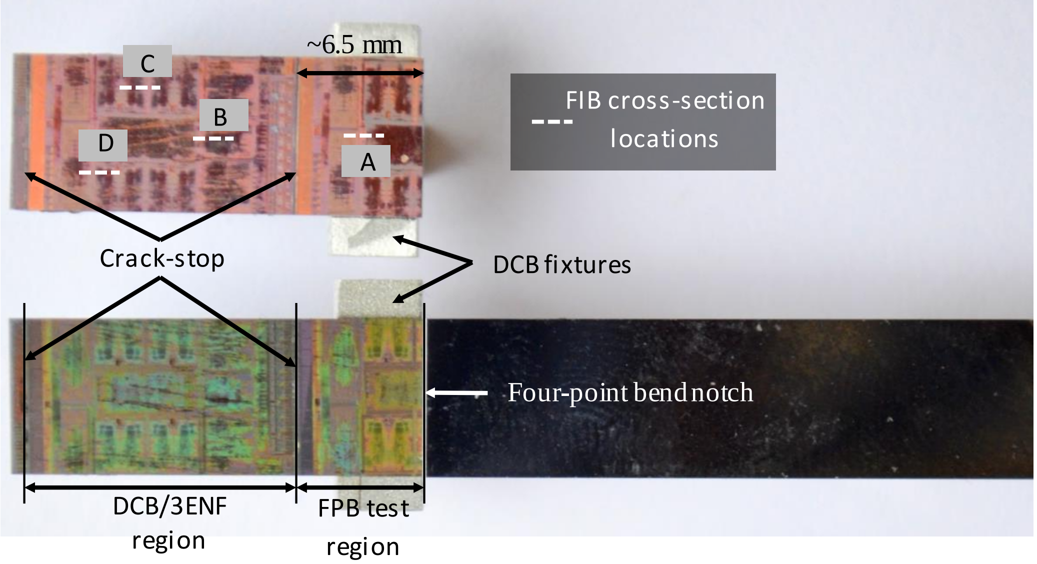


Figure 5-17. Sample after DCB test and FIB cross-section locations.

Figure 5-17 shows the fractured specimen after DCB test. The FPB test, DCB test regions and the crack-stop structures are indicated in Figure 5-17. In order to ensure that the crack is traveling along the same interface that fail at the end of chip-attach process, FIB cross-sections are made at various locations as indicated in Figure 5-17. The locations are carefully chosen to study the crack propagation along the width and length as well as different test areas. Each cross-section is 100 µm in length. Platinum (Pt) is deposited on top of BEOL stack prior to cutting through the sample to protect the brittle BEOL layers. It can be seen from the FIB cross-section images shown in Figure 5-18 and Figure 5-19 that the delamination stays in the 2x ULK layers and is located predominantly between the interface of B3 and B4 layers. The images also show that the delamination jumps to other ULK layers at some locations but finds its way back to the B3-B4 interface. This is consistent with the white-bump cross-sections shown in Figure 4-10.

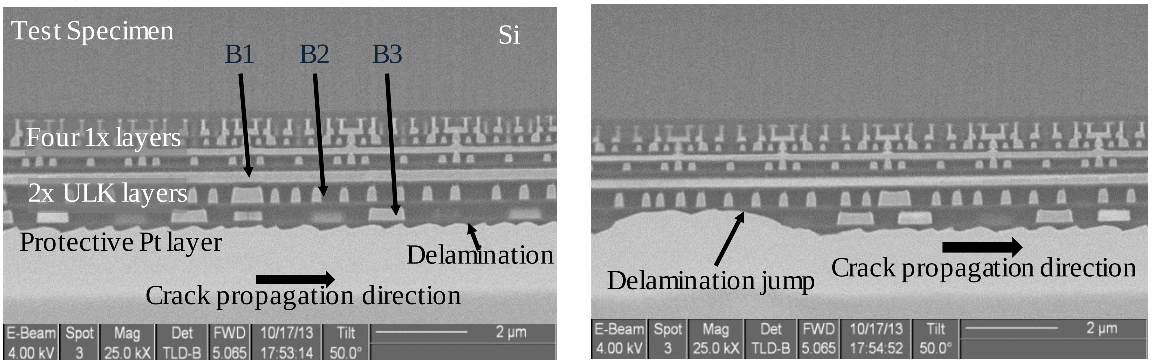


Figure 5-18. FIB cross-sections at location A – FPBT area.

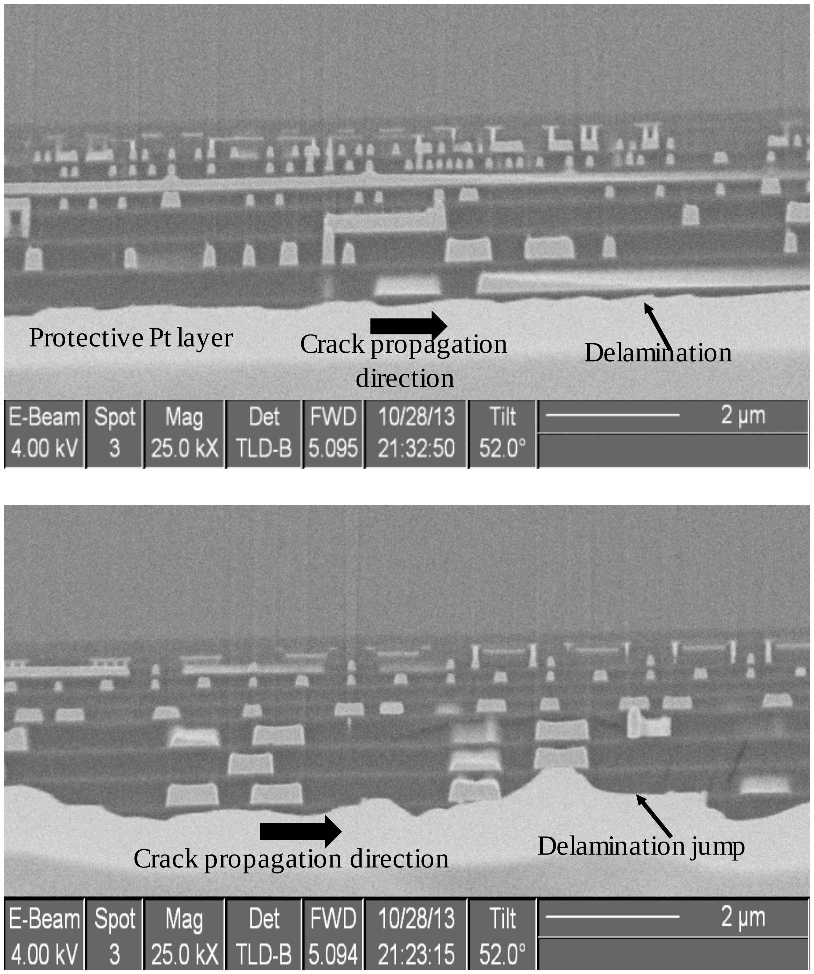


Figure 5-19. FIB cross-sections at location B, C and D – DCB area

5.7 MODE-MIXITY CALCULATION

Two-dimensional (2D) plane-strain fracture mechanics based models are developed to determine the mode-mixity of the experiments performed. For all the simulations, G_I, and G_{II} values are calculated using equations (2-4) and (2-5). Mode-mixity is determined using equation (2-16) as the crack travels at the interface of two sequentially deposited ULK layers. The results obtained from various simulations are summarized in Table 5-4.

5.7.1 DCB Mode-Mixity

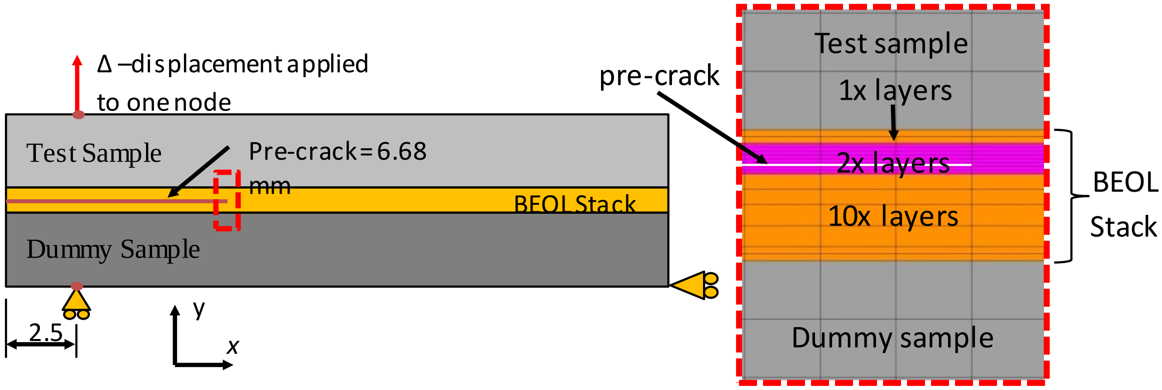


Figure 5-20. Schematic of DCB FE model. Inset: BEOL stack with FE mesh.

All model dimensions and loads are obtained from the DCB experiment setup described in section 5.4. Figure 5-20 shows the schematic of the 2D plane-strain finite-element model of the DCB test with boundary conditions and the inset shows the mesh along with various layers modeled in the BEOL stack. As shown, a pre-crack of 6.68 mm in length is modeled. The critical force per unit width corresponding to the pre-crack length obtained from Table 5-2 is applied to one node at a distance of 2.5 mm from the left edge on the top face. One node at 2.5 mm from the left edge is constrained in *'y'* direction (vertical direction) along the bottom face. The critical force and vertical constraints are applied at a distance of 2.5 mm from the left edge because the width of the

DCB fixtures is 5 mm, as shown in Figure 5-11. Also, as shown in Figure 5-20, one node is constrained in ‘*x*’ direction (horizontal direction) along the right edge of the model to prevent rigid body motion. The resulting displacement profile is shown in Figure 5-21. Figure 5-22 shows the σ_y profile around the crack tip. The ratio of G_{II} to G_I and the mode-mixity is shown in Table 5-4. As expected, mode-mixity for DCB test is close to 0°.

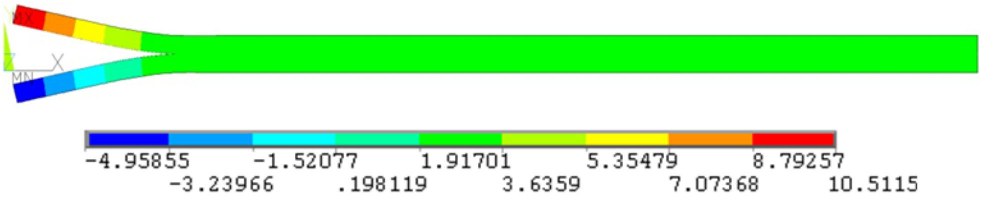


Figure 5-21. DCB FE model displacement contours in μm

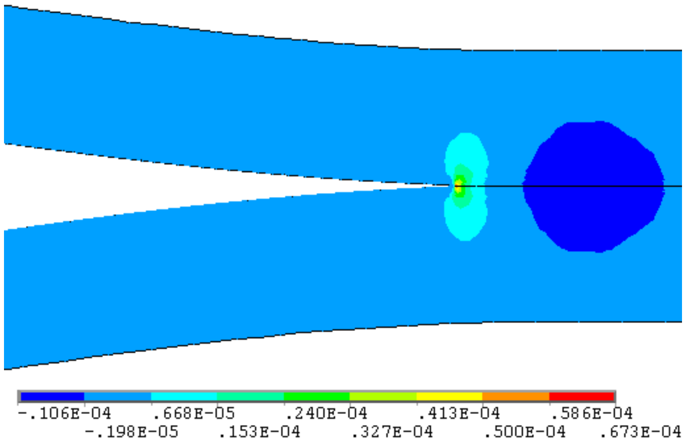


Figure 5-22. DCB stress (σ_y) contours around crack tip in N/μm^2

5.7.2 FPB Simulations

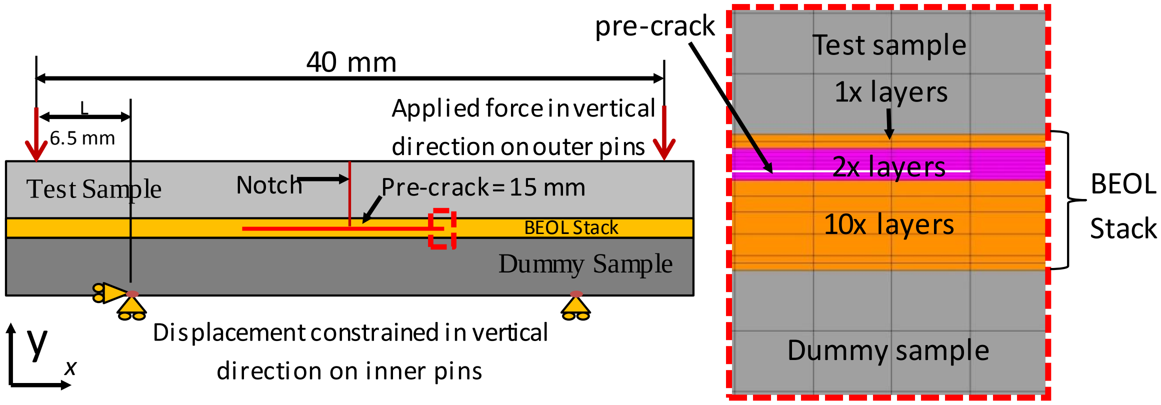


Figure 5-23. Schematic of FPB FE model. Inset: BEOL stack with FE mesh.

Schematic of 2D plane-strain finite-element model of the FPB test along with the boundary conditions and model dimensions are shown in Figure 5-24. As shown, critical force per unit width obtained from Table 5-1 is applied to the outer pins and displacement boundary conditions in vertical direction is applied to the inner pins. One of the inner pins is constrained in all directions to prevent rigid body motion. All model dimensions indicated in Figure 5-23 and loads are obtained from experiments described in Section 5.3. The resulting displacement profile is shown in Figure 5-25. Figure 5-29 shows the σ_y profile around the crack tip. The ratio of G_{II} to G_I and the mode-mixity is shown in Table 5-4. The mode-mixity for FPB test is 39.9°.

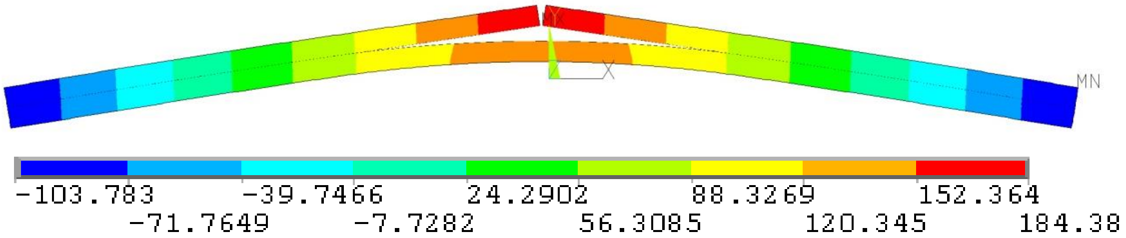


Figure 5-24. FPB FE model displacement contours in μm

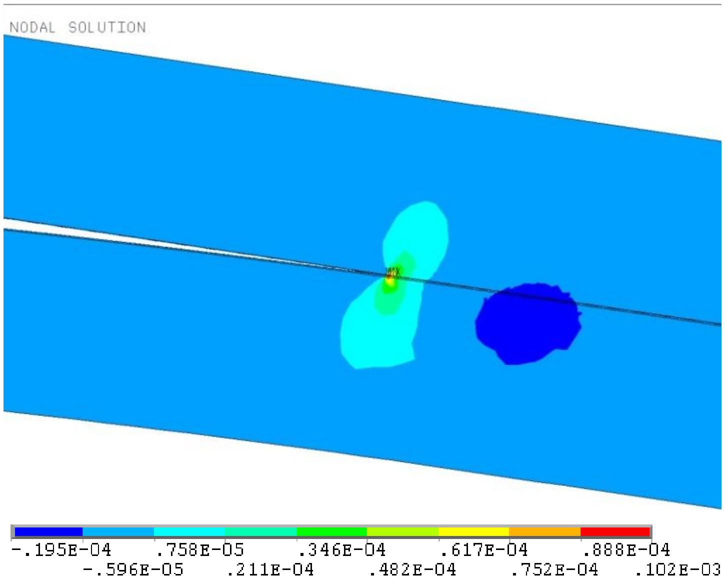


Figure 5-25. FPB stress (σ_y) contours around crack tip in N/μm^2

5.7.3 3ENF Simulations

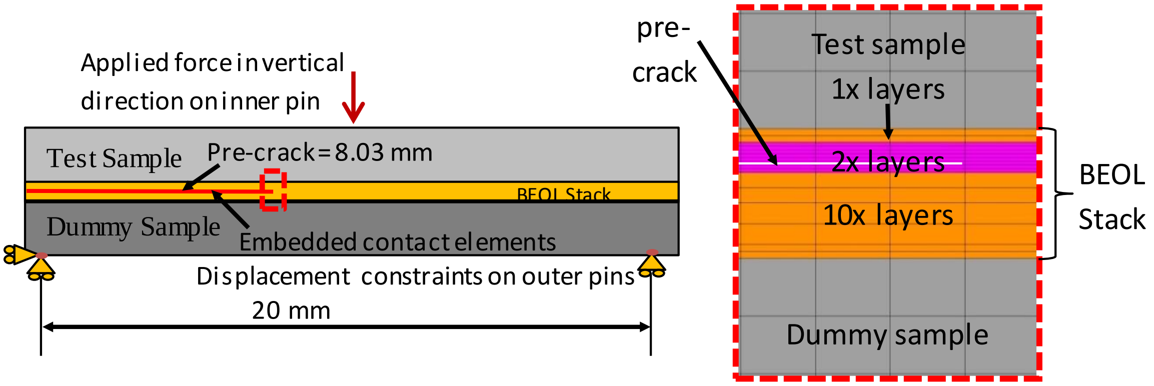


Figure 5-26. Schematic of 3ENF FE model. Inset: BEOL stack with FE mesh.

Schematic of 2D plane-strain finite-element model of the 3ENF test along with the boundary conditions and model dimensions are shown in Figure 5-26. As shown, pre-crack 8.03 mm is embedded with contact elements to prevent interpenetration of crack surfaces. Outer pins are constrained in vertical direction and one of the outer pins is constrained in horizontal direction as well, to prevent rigid body motion. The critical force corresponding to the pre-crack length obtained from Table 5-3 is applied to the middle pin. All model dimensions and loads are obtained from experiments described in Section 5.5. The resulting displacement profile is shown in Figure 5-27. As seen, the crack faces slide against each other indicating mode II dominant crack propagation. Figure 5-28 shows the σ_{xy} profile around the crack tip and the shape and the resulting profile indicates that crack propagates close to mode II in 3ENF test. The ratio of G_{II} to G_I and the mode-mixity is shown in Table 5-4. The mode-mixity for 3ENF test is 89.97°.

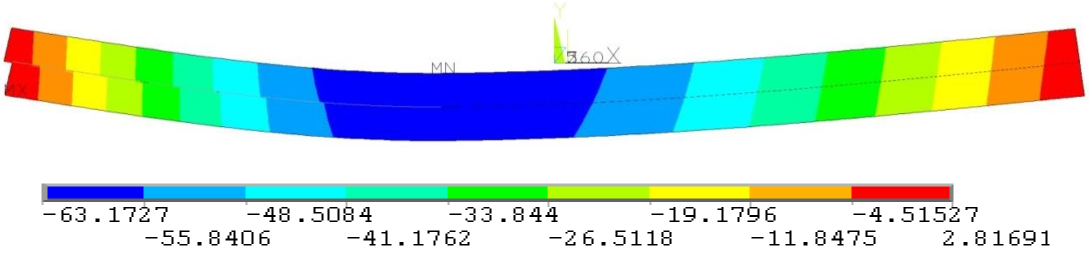


Figure 5-27. 3ENF FE model displacement contours in μm

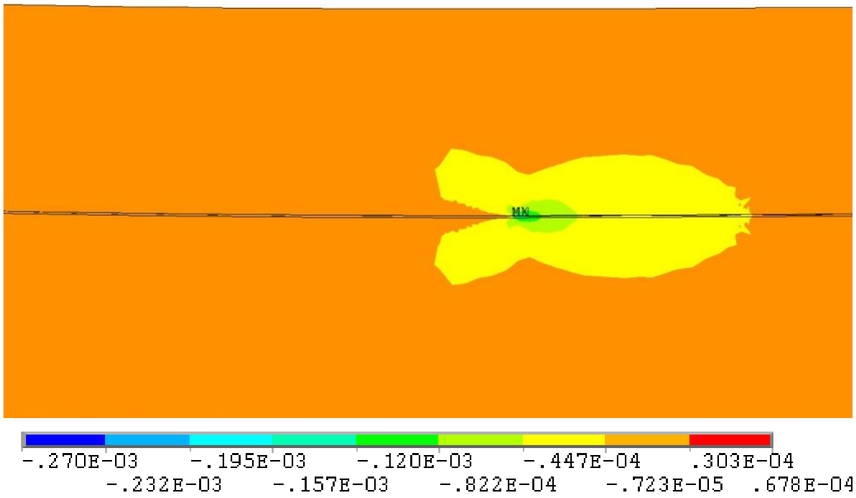


Figure 5-28. 3ENF stress (σ_{xy}) contours around crack tip in N/μm^2

Table 5-4. Mode-mixity and G_c for different experiments

Experiment	G_c (J/m^2)	G_{II}/G_I	Mode-mixity (degrees)
DCB	4.62	0.0014	0.0811
FPB	7.15	0.8391	39.9985
3ENF	22.1	2545.7650	89.9775

The G_c obtained from various experiments and the corresponding mode-mixities obtained from simulations are summarized in Table 5-4 and Figure 5-29. Several relationships have been proposed to characterize the critical energy release rate as a function of phase angle (mode-mixity) [34]. A widely accepted description of the functional dependence of mode-mixity on critical energy release rate is proposed by Hutchinson and Suo [34] and is given by equation (2-17),

In equation (2-17) γ is a variable that adjusts the influence of the mode II contribution. Figure 5-29 shows that when $\gamma = 0.28$, the curve fits the experiment results.

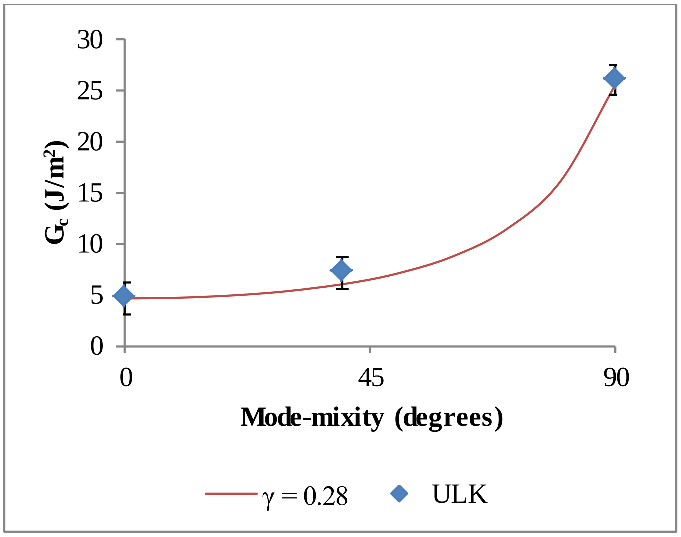


Figure 5-29. Experiment results summary, G_c as a function of mode-mixity.

The three tests described above will be used to characterize the CZ parameters described earlier in this study by performing appropriate finite-element simulations. Since the mode mixities of DCB and 3ENF tests are very close to mode I and mode II crack propagation, average values of G_{DCB} and G_{ENF} shown in Table 5-4 will be used as G_{Ic} and G_{IIc} respectively.

CHAPTER 6

COHESIVE LAW EXTRACTION: FINITE-ELEMENT SIMULATION

6.1 INTRODUCTION

The previous chapter outlined the interfacial fracture characterization experiments. Using the experiments, the critical layer present in the BEOL stack is identified and the critical fracture strength for various mode-mixities is characterized. In this chapter, a methodology used for extracting the cohesive zone parameters from the interface fracture characterization experiments is presented. As mentioned in CHAPTER 2, a bilinear T-δ law is used for characterizing the CZ elements. The CZ parameters required to fully define the bilinear law are the maximum traction (apex), critical separation (span) and the area under the curve for mode I and mode II respectively. Therefore, six independent parameters are required to fully define the mixed-mode T-δ law. Area under the curve given by the critical fracture strength is directly obtained from the experiments. G_{Ic} is determined from DCB test and G_{IIc} is determined from 3ENF test. Mimicking simulations of the interfacial fracture characterization tests are performed to obtain the remaining parameters. All of the tests can be approximated using 2D plane-strain finite-element (FE) models with cohesive zone elements placed along critical ULK layer interface (between B3 and B4) determined from FIB cross-sections shown in Figure 4-10, Figure 5-18 and Figure 5-19. Since the ULK material is doped silicon di-oxide, fracture occurs with negligible plasticity [124]. Also, low G_{Ic} indicates that the material is brittle [34]. Therefore, linear elastic fracture mechanics (LEFM) is assumed to be valid in this wok. Detailed discussion on CZM is presented in Chapter 2, here a brief summary is provided for the sake of continuity.

6.2 CZM –FINTE ELEMENT IMPLEMENTATION

Figure 6-1. CZ elements placed at the interface of two layers

Cohesive zone elements are implemented in the FE package using interface elements. Interface elements or CZ elements are zero thickness elements. As shown in Figure 6-1, CZ elements are placed along the interface of two sequentially deposited ULK layers in all the simulations. Since the material undergoes brittle fracture, the cohesive elements are characterized by bilinear cohesive law. Schematic of the bilinear law is shown in Figure 6-2. The cohesive law governs the traction-separation response of the cohesive elements and the area under the cohesive law is G_c. Figure 6-3 shows the deformation of the cohesive elements under mixed-mode loading conditions. As shown, if the resulting displacement of the cohesive elements due to the applied loads is less than δ^* then the elements are considered to be undamaged. If the resulting displacement is greater than δ^* and less than δ_c then the elements are considered to be partially damaged. The damage parameter, D_m within the partially damaged region ranges from 0 to 1 and can be determined using equation (2-25). If the resulting displacement is greater than δ_c then the elements are considered to be fully damaged and there is no interaction between the two surfaces ($T = 0$). As seen from equation (2-25) and schematically shown in Figure 6-3, D_m is 0 in the undamaged region and can take up a maximum value of 1 in the fully damaged region.

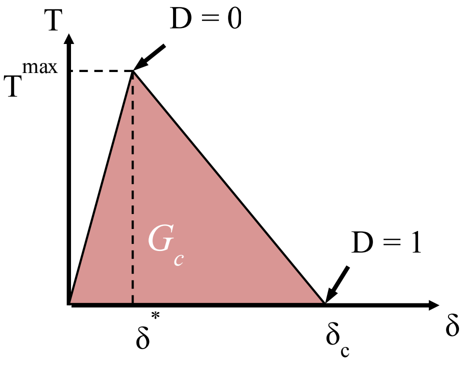


Figure 6-2. Bilinear cohesive law

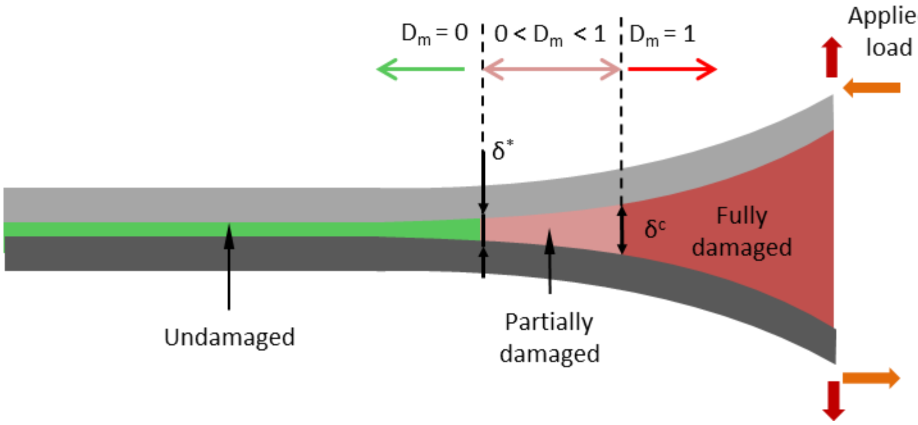


Figure 6-3. Deformation of CZ elements under mixed-mode loads

Six independent parameters namely G_{Ic}, T_n^{max}, $\delta_n^{\ c}$, G_{IIc}, T_t^{max} and $\delta_t^{\ c}$ are required to fully characterize the mixed-mode T-δ law. As seen from Table 5-4, crack propagates close to mode I in DCB test. Therefore, G_{Ic} is directly obtained from the DCB tests and the remaining mode I CZ parameters T_n^{max} and $\delta_n^{\ c}$ are determined from simulations mimicking the load versus displacement curve of the DCB test. G_{IIc} is obtained from 3ENF test as the crack propagates close to mode II in 3ENF test. The remaining mode II CZ parameters T_t^{max} and $\delta_t^{\ c}$ are obtained from simulations mimicking FPB test.

6.3 MODE I CZ PARAMETERS – SIMULATION OF DCB TEST

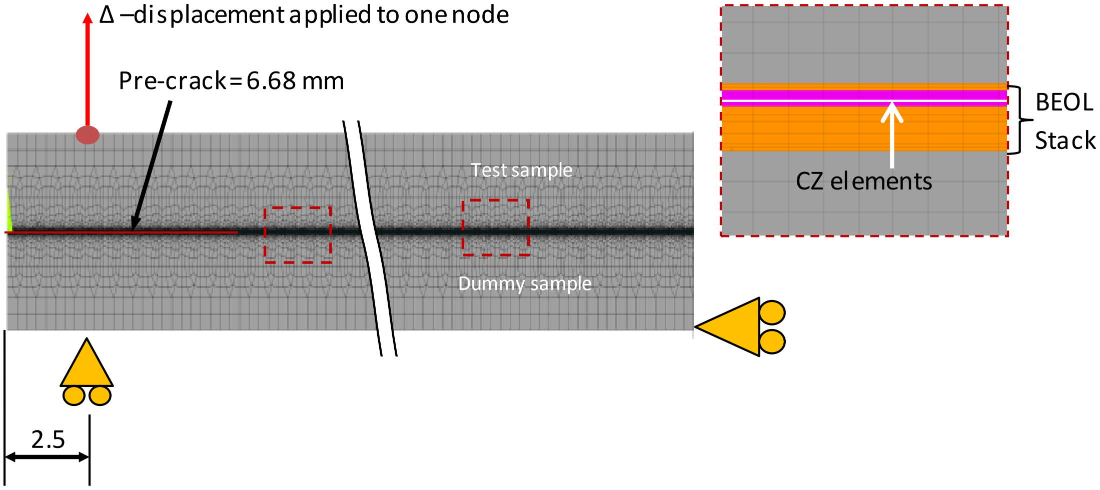


Figure 6-4. DCB CZ based FE model showing mesh and boundary conditions

Figure 6-4 shows the schematic of the 2D plane-strain FE model of the DCB test. A pre-crack of length 6.68 mm determined from compliance calculations is placed in the FE model as indicated in Figure 6-4, along the critical ULK layer. Mode I dominated CZ elements are placed along the crack path. Contact elements are overlaid on top of CZ elements to prevent interpenetration of crack surfaces. The bottom clamp is represented with vertical displacement constraint, and the top clamp is simulated with the applied displacement. One node away from the interface is constrained in the horizontal direction to prevent rigid body motion. The geometry is finely meshed to account for various thin layers of the BEOL stack. Mesh convergence studies are done to determine appropriate mesh densities.

As mentioned before, the area under the mode I T-δ curve is given by G_{Ic} determined from DCB tests. In order to determine the remaining parameters, a systematic analysis is performed by varying the T_n^{max} and α_n, the ratio of δ_n^* to δ_n^c to mimic the experiment DCB test. It can be seen that, change in T_n^{max} changes the maximum force and change in α_n changes the initial slope. As seen from Figure 6-5b, T_n^{max} is varied until the maximum force value obtained from simulations matches the experiment results. Once the maximum force values are matched with experiments, α_n is varied until the initial slope of simulations matches experiments. It can be seen from Figure 6-5 that, when T_n^{max} is equal to 1.8 MPa and α_n is equal to 0.035, simulation results agree well with experiments.

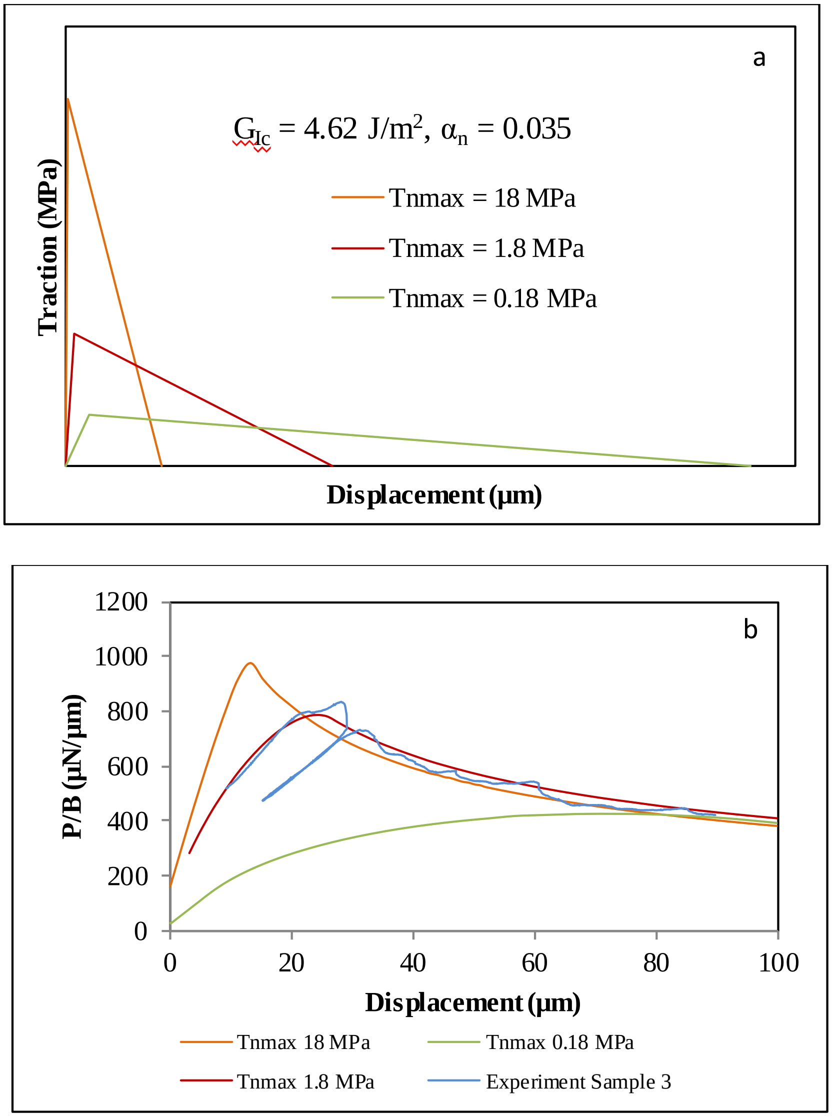


Figure 6-5 a) *T-δ* curves used for sensitivity analysis b) DCB Simulation results comparison with experiments

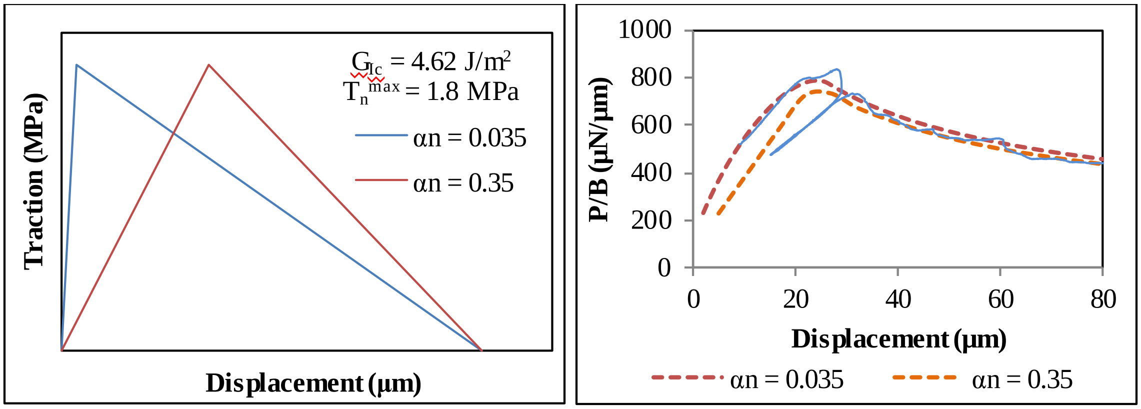


Figure 6-6. a) *T-δ* curves used for sensitivity analysis b) DCB Simulation results - variation of α_n

The mode I CZ parameters determined from the inverse analysis are shown in Table 6-1. Once the mode I CZ parameters are determined, it is necessary to validate it for different pre-crack lengths obtained from experiments shown in Table 5-2. Figure 6-7 shows load vs. displacement curve obtained for pre-crack lengths of 6.68 mm and 7.75mm. It can be seen that the simulation is able to capture the loading stiffness as well as the load vs. displacement history after crack propagation for both the cases.

Critical load obtained from three DCB test samples is plotted against the corresponding crack length in Figure 6-8. The reaction forces and crack length are then calculated at several sub-steps during the DCB test simulation and plotted in Figure 6-8. In the DCB test simulation, the crack length is calculated from the mode I dominated damage equations. It can be seen that the simulation parameters are able to exactly mimic critical load vs crack length curve obtained from DCB experiments. Thus, the simulation parameters capture both load vs displacement and critical load vs crack length curves obtained from different samples.

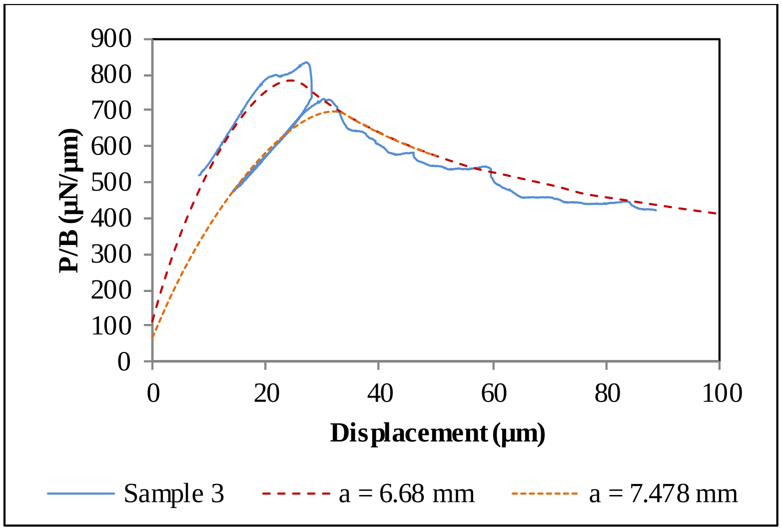


Figure 6-7. DCB simulation results comparison with experiments. Load vs displacement.

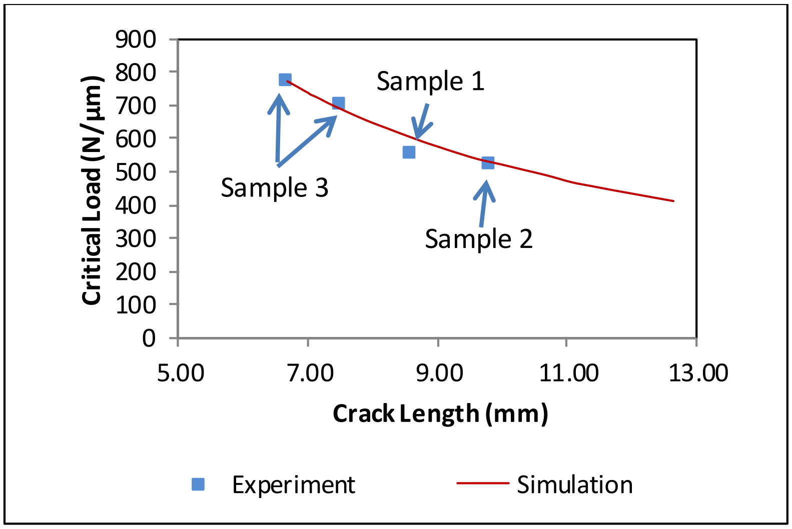


Figure 6-8. DCB results comparison with experiments. Critical load vs crack length

6.4 MIXED-MODE SIMULATION OF FOUR-POINT BEND TEST

Area under the tangential bilinear traction-separation law is given by G_{IIc} obtained from 3ENF test. The two remaining parameters: maximum tangential traction (T_t^{max}) and critical tangential separation (δ_t^c) are obtained from finite-element simulation of FPB test using CZ elements. Figure 6-9 shows the schematic of the FPB test FE model along with boundary conditions. As seen, no pre-crack is modeled to mimic the test. The CZ elements placed along the interface of critical ULK layer. Since the crack propagates in mixed-mode condition during FPB test, mixed-mode CZ elements characterized by six independent parameters are used in the simulation. Using the mode I CZ parameters obtained earlier from DCB test, T_t^{max} and ratio of δ_t^* to δ_t^c are varied until the simulation matches the experiment results. The final results are shown in Figure 6-10 and it can be seen that the FE model can capture both the loading slope and steady state critical load. The mode II CZ parameters thus obtained are shown in Table 6-1.

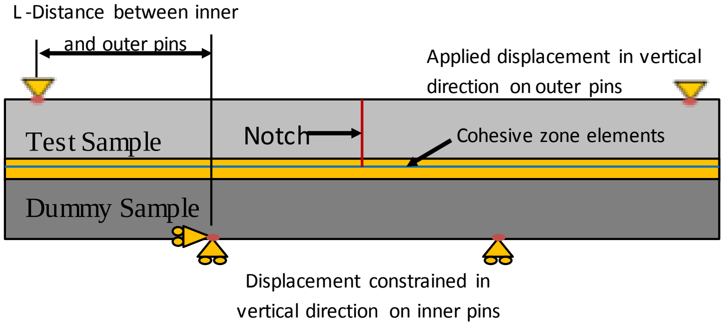


Figure 6-9 Schematic of four-point bend test FE model with boundary conditions

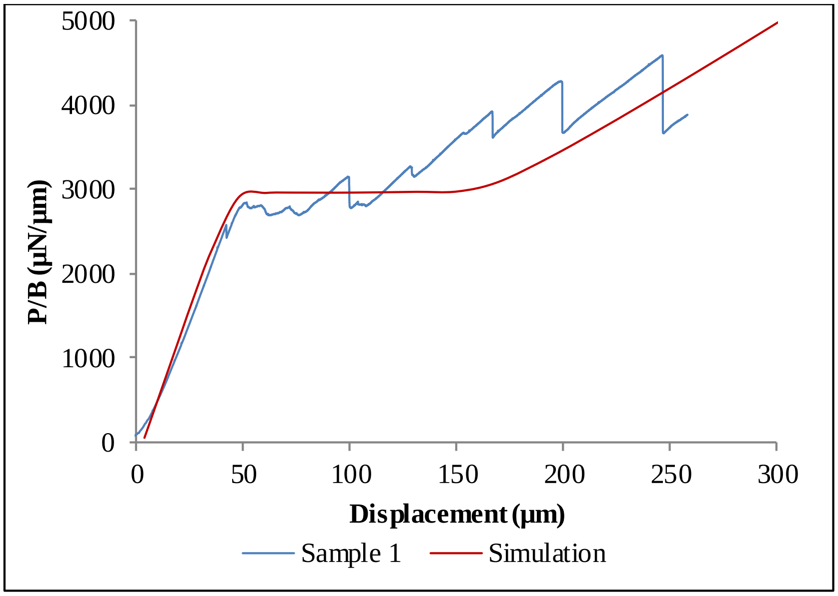


Figure 6-10 FPBT simulation results compared against experiments

Figure 6-11 shows the experimentally determined *T-δ* curves for mode I and mode II, and the mixed-mode traction-separation law parameters are also tabulated in Table 6-1.

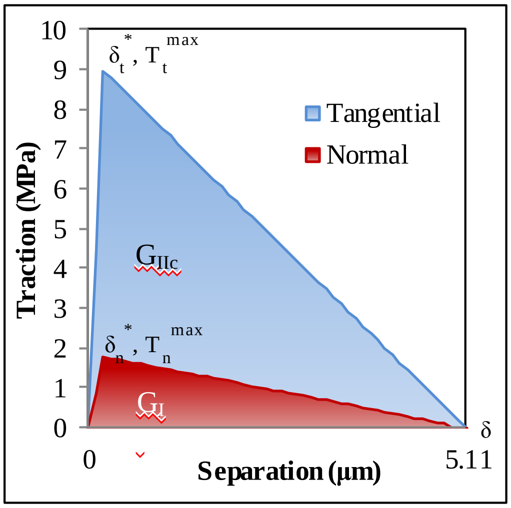


Figure 6-11. Mixed-mode cohesive zone parameters

Table 6-1. Mixed-mode CZ parameters

	Normal	**Tangential**
G (J/m^2)	4.62	22.10
T^{max} (MPa)	1.80	9.00
δ*(µm)	0.18	0.09
δ$_c$ (µm)	5.13	4.91

The primary challenge in using inverse analysis for obtaining CZ parameters is that, the CZ parameters may not be unique. In order to overcome that, the results are validated across multiple samples, mode-mixities and a real-life microelectronic device failure presented in the next chapters.

CHAPTER 7

DELAMINATION PREDICTION USING COHESIVE ZONE MODELING: 2D MODEL

7.1 INTRODUCTION

Now that the mixed-mode CZ parameters have been characterized for critical layer present in BEOL stack, the next step is to develop CZ based FE models to predict failure. The developed CZ parameters can be applied to predict failure of flip-chip packages under various loading conditions. For example, failure of BEOL stack can be predicted after underfill curing or during qualification tests like thermal cycling, thermal shock testing, highly accelerated stress tests (HAST), etc. that a flip-chip assembly may experience. CZM approach enables quick as well as reliable prediction of the failure region. In this chapter, the application of CZM based FE models to predict white-bump failures observed at the end of chip-attach process is demonstrated. Therefore, the objectives of this chapter are

1. apply the developed CZ models in a flip-chip reflow assembly simulation
2. predict multiple white-bump failures using the CZ based FE model

7.2 TWO DIMENSIONAL FLIP-CHIP RELIABILITY MODELING

A schematic of the flip-chip assembly is shown in Figure 7-1. CHAPTER 4 outlined fracture-mechanics based approach to predict the white-bump failures at the end of flip-chip chip-attach process. Unlike the fracture-mechanics based model wherein submodeling modeling approach is pursued, here all the components including the stack are modeled in one model. Although computationally expensive compared to sub-modeling approach, this is adopted because it is a one-time simulation. In other words, re-meshing or re-iteration is not required to capture the fully fractured area. Also, in CZM approach the concept of crack (a discontinuity) is replaced by damage (numerical continuity is maintained but there is no interaction in the fully damaged region). Damage initiation and propagation criteria are governed by the T-δ law. The CZ elements are placed along the critical B3/B4 ULK interface across the entire model. The model is then simulated to go through the flip-chip chip-attach process using element birth/death approach. As the model is simulated to cool-down from reflow temperature to room temperature during the final step, damage gets accumulated across multiple bumps and such a model can simulate multiple bump cracking using a single model as observed in reality.

7.2.1 C45 Flip-Chip Model

A two-dimensional (2D) plane-strain half symmetric FE model of the organic flip-chip assembly is created. As shown in the schematic Figure 7-1, the model accounts for the die, passivation layer, die pad, solder bump, substrate pad, various layers in the substrate, BEOL stack consisting of metallization layers, low-κ dielectric layers, and ULK dielectric layers. Isotropic material properties are used for silicon and BEOL stack materials. The flip-chip has a planar size of 15 mm and 12 mm, thickness of 0.78 mm, having lead-free solder bumps with a pitch of 360 μm. The bumps are 65 μm in height, and have a diameter of 105 μm, while being attached to a 75 μm square Al pad. Isotropic, temperature-dependent properties along with Anand's viscoplastic model are used for lead-free solder (96.5% Sn; 3.5% Ag). Temperature-dependent isotropic material properties are used for buildup dielectric layer present in the substrate and orthotropic properties for the substrate core. It can be seen from Figure 7-1 that the metallization and buildup dielectric layers present in the substrate are also included in the models. Since the substrate metallization layers consist of copper traces interspersed with buildup dielectric, effective orthotropic material properties determined using the micromechanics approach are used. The traces and vias present in the BEOL stack are not modeled to reduce the complexity. Additional details on material properties, geometry of such flip-chip assembly, model dimensions and stress distribution in such configurations can be found in CHAPTER 4.

The CZ elements are placed along the critical ULK layer. Contact elements are overlaid on the CZ elements to prevent interpenetration of interface CZ elements. The model is then simulated to go through the flip-chip chip-attach process. Damage initiation and propagation criteria of the CZ elements are governed by the *T*-*δ* law. The mixed-mode CZ parameters that define the *T*-*δ* law determined from fracture characterization experiments is shown in Table 6-1.

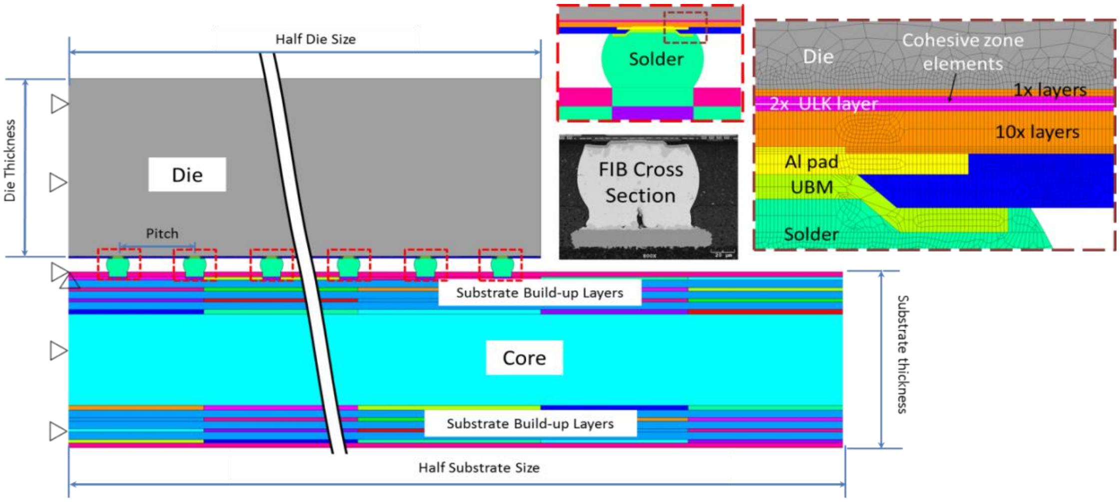


Figure 7-1. 2D flip-chip model with BEOL stack and cohesive zone elements placed along critical ULK layer

The boundary conditions are shown in Figure 7-1, symmetric boundary conditions are applied to the left edge of the model and one node at substrate is constrained in all degrees of freedom to prevent rigid body motion. The reference temperature of the substrate is assumed to be 150 °C and all other components of the model are assumed to be stress free at solder reflow temperature (220 °C). To reflect the process history, the simulation is performed by killing the solder during the first load-step and the model is simulated to heat up to solder reflow temperature. During the next load-step, solder is activated/birthed at reflow temperature and the assembly is then simulated to cool-down from solder reflow temperature to room temperature (25 °C) at a rate of 60 °C/minute.

7.3 PREDICTION OF MULTIPLE CRACKS

As mentioned before, cohesive zone elements are zero thickness interface elements with coincident nodes. When the model is simulated to cool down from solder reflow to room temperature, the entire model warps down because the CTE of the substrate is higher than silicon die. From the normal and shear displacements of the nodes attached to cohesive elements the mixed-mode damage parameter is calculated across the entire die length at room temperature. The mixed-mode damage parameter is calculated based on equations presented in Section 2.4.4. Figure 7-2 shows the calculated damage value plotted against the distance from the center of the chip. As shown in Figure 1, the chip size is approximately 15 mm x 12 mm, and the solder pitch is 360 µm. Since the model is a half-symmetric model, the span of the plot shown in Figure 7-2 is ~7.5 mm. Damage value of more than 1 indicates fully damaged region or crack. As seen from Figure 7-2, the model predicts that the last five bumps from the edge solder bump are likely to fail. The displacement contours in vertical direction for last three solder bumps from the die edge at room temperature is shown in Figure 7-3. CZ elements are removed in order to visualize the failure region or cracks seen in Figure 7-3. Thus, the model is able to capture the simultaneous failure of multiple bumps and can also predict the failure region over several bumps in a single step simulation process.

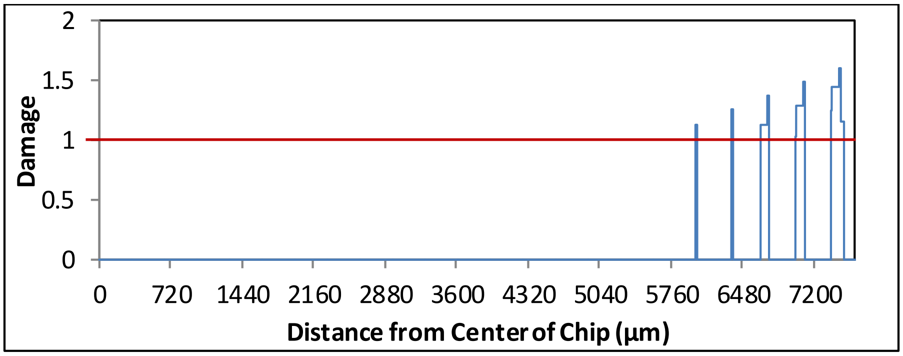


Figure 7-2. Damage across the entire model at room temperature

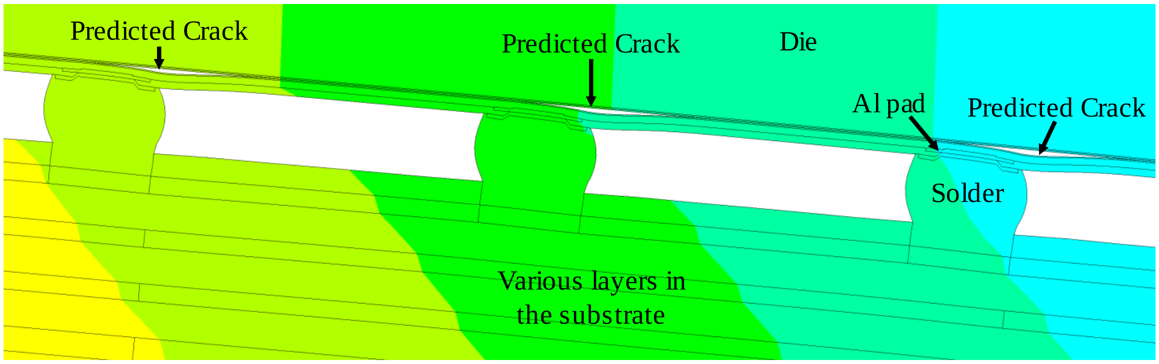


Figure 7-3. Displacement profile of the edge solder bumps at room temperature

The damage is calculated at several intermediate temperatures as the model is simulated to cool down from reflow to room temperature. The crack length is calculated from the mixed-mode damage model for each intermediate temperature. Figure 7-4 shows the displacement contour around the outermost solder bump at 64 °C and 25 °C along with the calculated crack length. It can be seen from Figure 7-4 that as the model is cooled down, the crack initiates around Al pad edge and crack size increases, as expected. Figure 7-5 shows the damage above the solder bumps that failed during the cool down simulation, at different temperatures. The orange lines in Figure 7-5 show the center of the solder bumps. It can be seen that the damage is confined to one side around all bumps, the side closer to die edge for all bumps. It is noticed that till 64 ^{0}C there is no damage and at that temperature cracking is observed above the last two solder bumps from the die edge. As the model is cooled down cracking is observed above more bumps. Figure 7-5 also shows length of the damaged region or crack length at room temperature, as expected crack length reduces as we move close to the center of the die. Although damage value of more than 1 indicates fully damaged region, higher values are also plotted to understand the region that suffered maximum damage. It can be seen that the region that suffered the maximum damage is the region at which the crack begins to initiate at 64 ^{0}C. Also, the region that suffers maximum damage is above the Al pad edge. These results correlate well with fracture mechanics based simulation model predictions presented in CHAPTER 4.

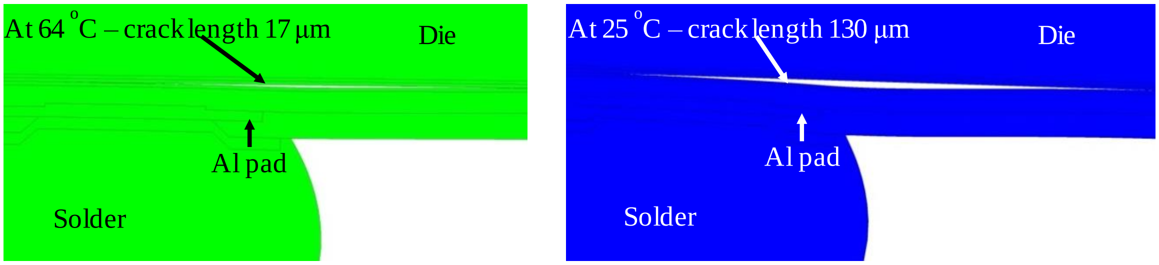


Figure 7-4. Schematic of crack above the edge solder bump

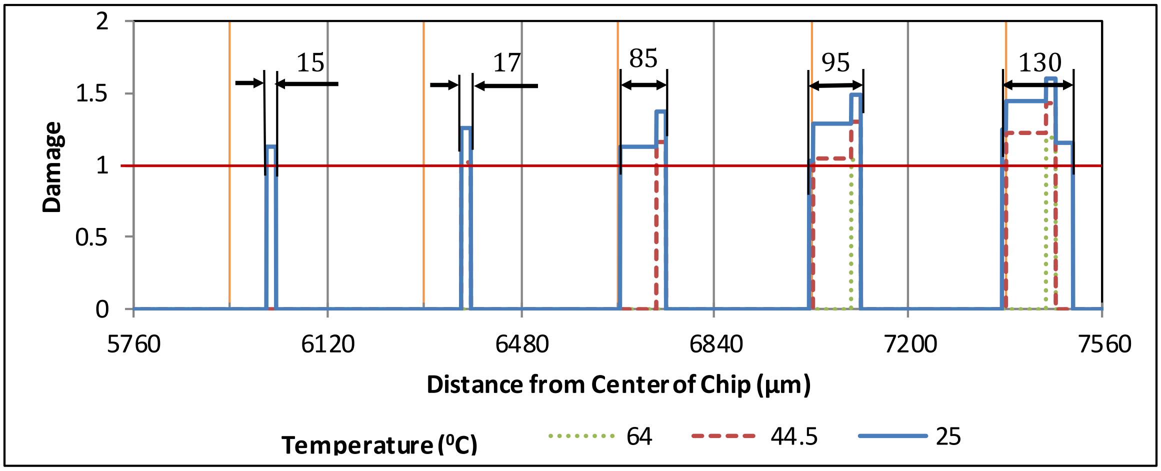


Figure 7-5. Damage above the outermost solder bumps at room temperature

7.4 SUMMARY

Cohesive zone modeling approach is presented in this chapter to predict white-bump failures observed in lead-free organic flip-chip assemblies at the end of chip attach process. A 2D plane-strain finite-element model of flip-chip assembly with BEOL stack and cohesive elements placed along the critical ULK layer is created. Cohesive elements are characterized by mixed-mode T-δ parameters determined from inverse analysis of load-displacement curves of interfacial fracture characterization experiments. The flip-chip assembly model is then simulated to go through the solder reflow process considering the process history using element birth/death approach. The damage suffered by the cohesive elements is studied and plotted across the entire die at various temperatures during the cool-down process. It is noticed that the damage or crack initiates at 64 ^{0}C and grows as the assembly is cooled down further. The model predicts that outermost five solder bumps from the longer edge of the die are likely to fail at room temperature. It is seen that the crack length reduces as we move towards the center of the die. Also, the damage is confined to one side of the bump. It is also noticed that the region that suffers maximum damage is the region where the crack initiated, and this region is located above the Al pad. These findings are consistent with fracture mechanics based results as well as experimental data presented in CHAPTER 4.

CHAPTER 8

DELAMINATION PREDICTION USING COHESIVE ZONE MODELING: 3D MODEL

In the previous chapter, CZ elements were used in a 2D model to predict the location and length of delamination during flip-chip assembly. In this chapter, the same set of CZ parameters is used to predict location, span and shape of delamination in a 3D model. The results from 3D models can be compared against failure analysis results of flip-chip devices. Such models can then be used to develop design guidelines to reduce white-bump failures.

8.1 THREE DIMENSIONAL GLOBAL-LOCAL MODEL

Figure 8-1 shows the 3D schematic of flip-chip assembly. To build a 3D model comprising of components with dimensions ranging from tens of mm to hundreds of nm can be expensive in terms of computation memory and solution time required. Same limitations are applicable for quarter model or 1/8th model of the assembly. Therefore, global plane deformation model (GPD) or 3D strip model is pursued in this study. 3D strip models have been used in literature extensively to study solder joint fatigue [125], evolution of stresses in flip-chip packages [126]. Strip models are a good compromise between 2D and 3D FE models. Since corner solder bumps are subjected to highest thermo-mechanical stresses, a strip model of length equal to the diagonal is modeled, as indicated in Figure 8-1.

Global-local (submodeling) approach is pursued for the reasons mentioned above. Schematic of the 3D strip model along with GPD boundary conditions is shown in Figure 8-2. As seen, strip model is half-pitch wide with coupled boundary conditions applied to all nodes in the plane $x = 0$, symmetric boundary conditions are applied to all nodes in the plane x = pitch/2 and $z = 0$. One node along $z = 0$ is constrained in all direction to prevent rigid body motion. Different colors in Figure 8-2 attribute to different material properties associated with each section. Similar to the global models described in CHAPTER 4, the BEOL stack is not modeled in the global model. All other features including the layers present in the substrate are modeled in the global model. The approach, material properties and the model features are same as 2D global models described in CHAPTER 4. The global model is simulated to cool down from reflow temperature to room temperature at the rate of 60 ^{o}C/minute.

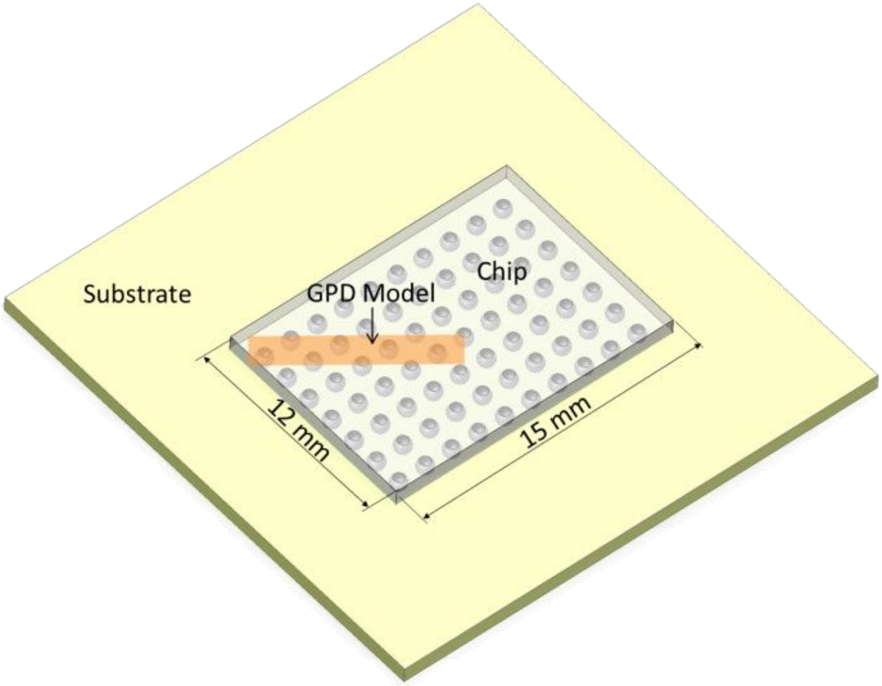
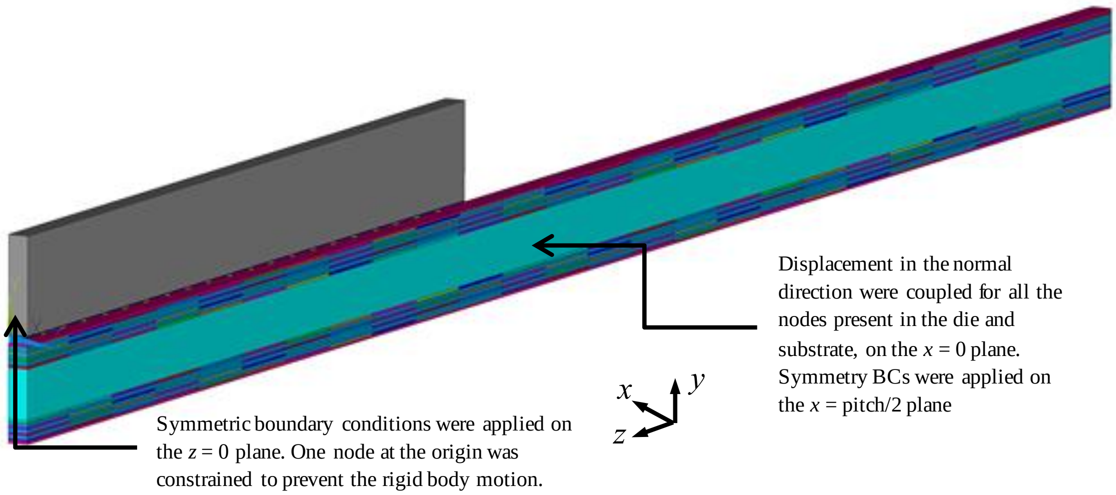


Figure 8-1. Schematic of a flip-chip assembly



Displacement in the normal direction were coupled for all the nodes present in the die and substrate, on the $x = 0$ plane. Symmetry BCs were applied on the x = pitch/2 plane

Symmetric boundary conditions were applied on the $z = 0$ plane. One node at the origin was constrained to prevent the rigid body motion.

Figure 8-2. Global plane displacement model (3D strip model)

In Figure 8-3 schematic of 3D local model of the critical corner solder bump is shown. As seen, a quarter of the chip along with BEOL stack, Al pad, UBM, polyimide (PI) layer, solder bump and the top four layers of the substrate are modeled in the local model. The characterized CZ elements are placed along the critical ULK layer. Contact elements are overlaid on top of CZ elements to prevent inter-penetration of interface CZ elements. The displacement constraints at room temperature obtained from the global model are applied as boundary conditions to the 3D local model. The constraints are imported for the nodes on the outer faces of the local model far away from the region where damage is expected. The displacement contour results obtained from the local model is shown in Figure 8-4. It can be seen from Figure 8-4 that the cracked region above the solder bump is confined to one side of the bump, as predicted by 2D fracture mechanics based models in CHAPTER 4.

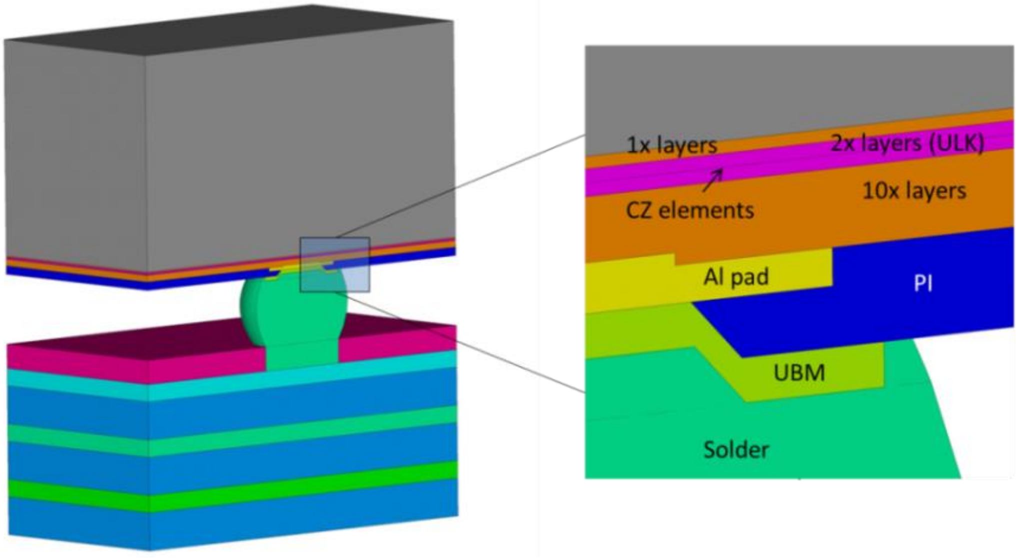


Figure 8-3. Schematic of 3D local model

8.2 WHITE-BUMP PREDICTION

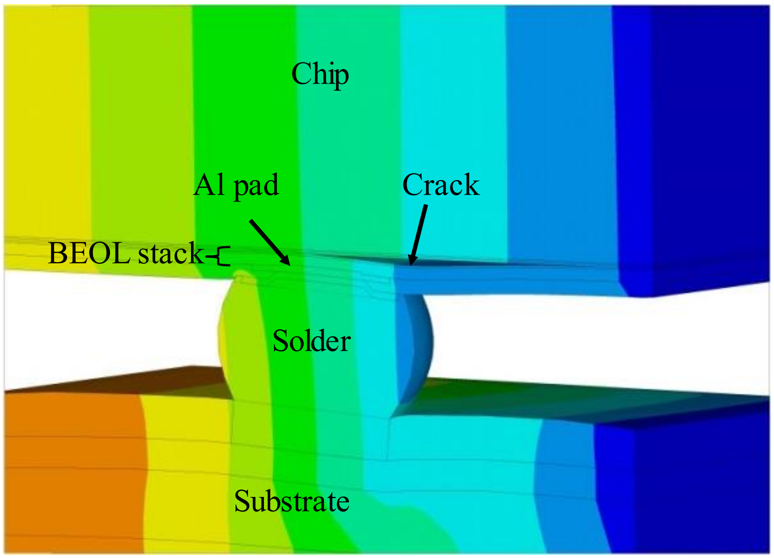


Figure 8-4. Displacement contours with failed CZ elements.

Since the crack propagates in mixed-mode conditions, the damage is calculated using equations in Section 2.4.4. In Figure 8-5a opacity of components are decreased in order to visualize the different components of local model such as the die, different layers in the BEOL stack, solder bump and different layers in the substrate. Figure 8-5b shows the top view of the critical ULK interface over which CZ elements are overlaid. Figure 8-5b also shows the location of Al pad and solder bump. Damage is calculated at each node on the area shown in Figure 8-5b. Figure 8-6 shows the resulting damage contours in the ULK layer around the corner solder bump. Figure 8-6 shows an area of one square pitch, with the inset showing the solder bump and Aluminum pad to indicate the viewing angle. The Aluminum (Al) pad area is also included to visualize the damage area. In Figure 8-6, the resulting damage value is plotted against distance from the edge of the die. The fully-damaged region ($d_m > 1$) is plotted in different colors, whereas partially-damaged and the undamaged region ($d_m < 1$) is plotted in dark blue. It can be seen from Figure 8-6 also that the fully damaged area ($d_m>1$) is confined to one side of the bump, similar to 2D model prediction, presented in CHAPTER 4 and CHAPTER 7. It is seen from Figure 8-6 that under reflow assembly and cool-down, the outermost solder bump is likely to have a fully damaged region that spans from 75 µm from the die edge to about 170 µm from the die edge. Thus, the fully damaged region is predicted to be 95 µm, and is likely to be positioned above the aluminum pad of the outermost solder bump. One representative FIB cross-section of an actual flip-chip assembly is shown in Figure 8-7 and Figure 4-10 with the crack seen along the 2x ULK layer. The average crack length is found to be 90 µm for five samples that were cross-sectioned and imaged through FIB, as shown in Table 4-7.

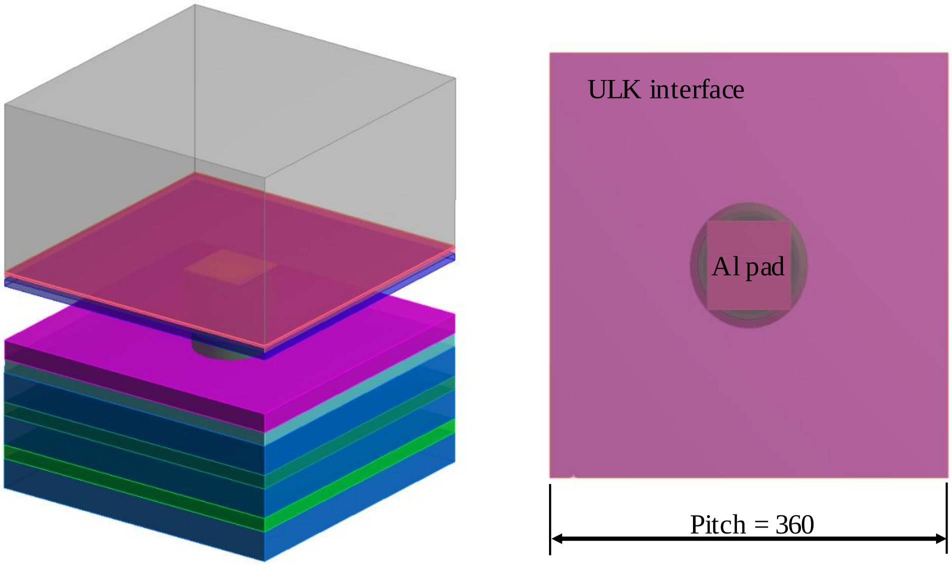


Figure 8-5. a) Local Model. b) Top view showing the ULK interface, Al pad and solder bump. All other components are hidden

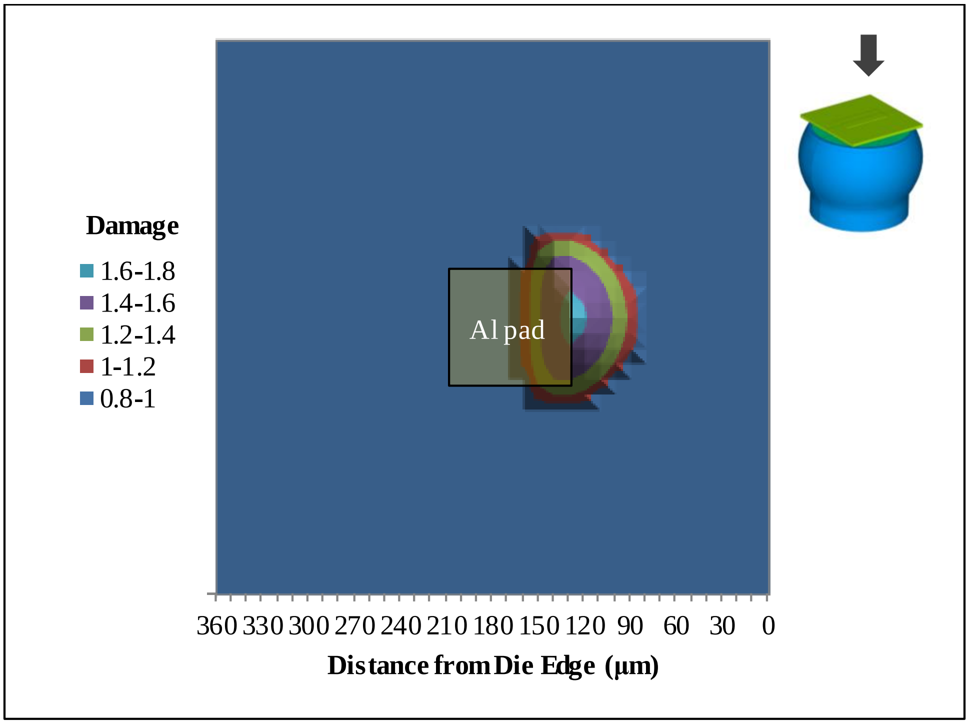


Figure 8-6. Damage profile predicted by 3D FE model

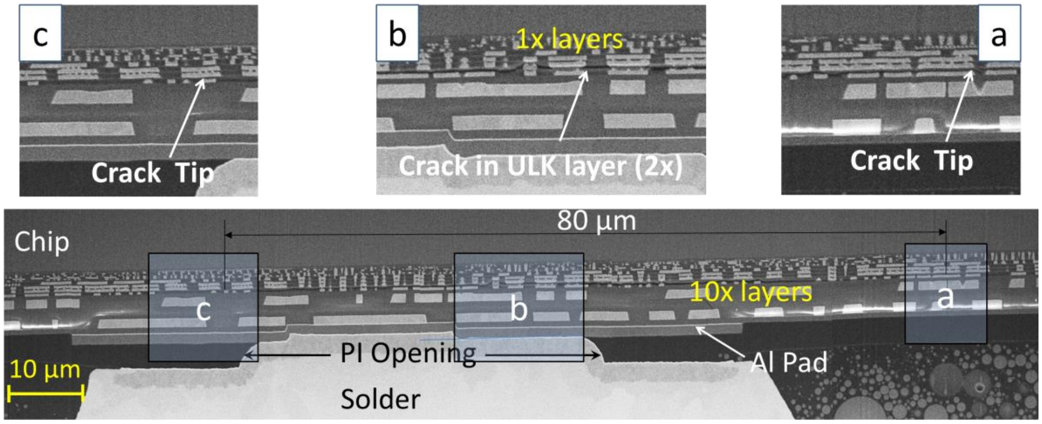


Figure 8-7. FIB cross-section of white-bump with crack tip locations

8.3 ROLE OF ASSEMBLY REFLOW TEMPERATURE IN BEOL CRACKING

The damage is calculated at each intermediate temperature during the cool-down simulation. Damage accrued by all the CZ elements present along the ULK interface is plotted in Figure 8-8 at different temperatures. Damage value ranges between 0 and 1, and a value greater than 1 indicates fully damaged element or a crack. In Figure 8-8, the calculated damage value is plotted against the distance of the element from the edge of the die. Damage values less than 1 are plotted in blue and values greater than 1 are plotted in different colors, as shown in the legend. It can be seen from Figure 8-8 that the damage /crack initiates above the Al pad edge around 85 °C and gradually grows in size as the model is cooled down. It can also be seen from the damage profile at 25 °C that the failure region is confined to one side of the bump during the cool down and the region that suffered maximum damage is the crack initiation region. Such a model is then used to study the impact of design variations and chip-package interaction parameters on flip-chip assembly reliability.

Furthermore, local model of bumps away from the corner solder bump is modeled and the appropriate displacement constraints are obtained from global model at room temperature. As shown in Figure 8-9, the model predicts that the last two bumps would fail and as expected the corner solder bumps suffer more damage than the bumps located further away from the die edge.

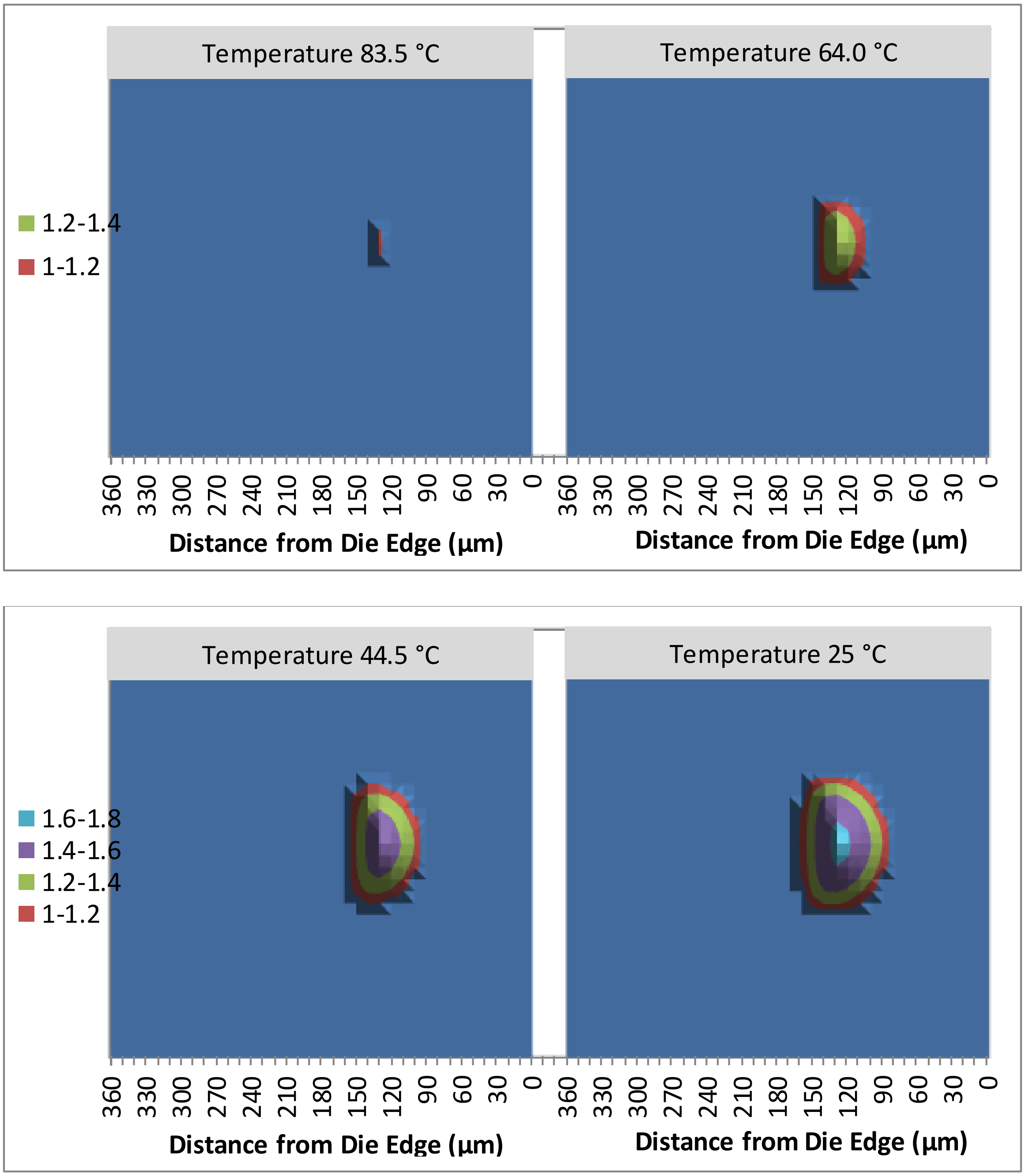


Figure 8-8. Damage profile predicted by the 3D FE model at various intermediate temperatures during the cool-down simulation

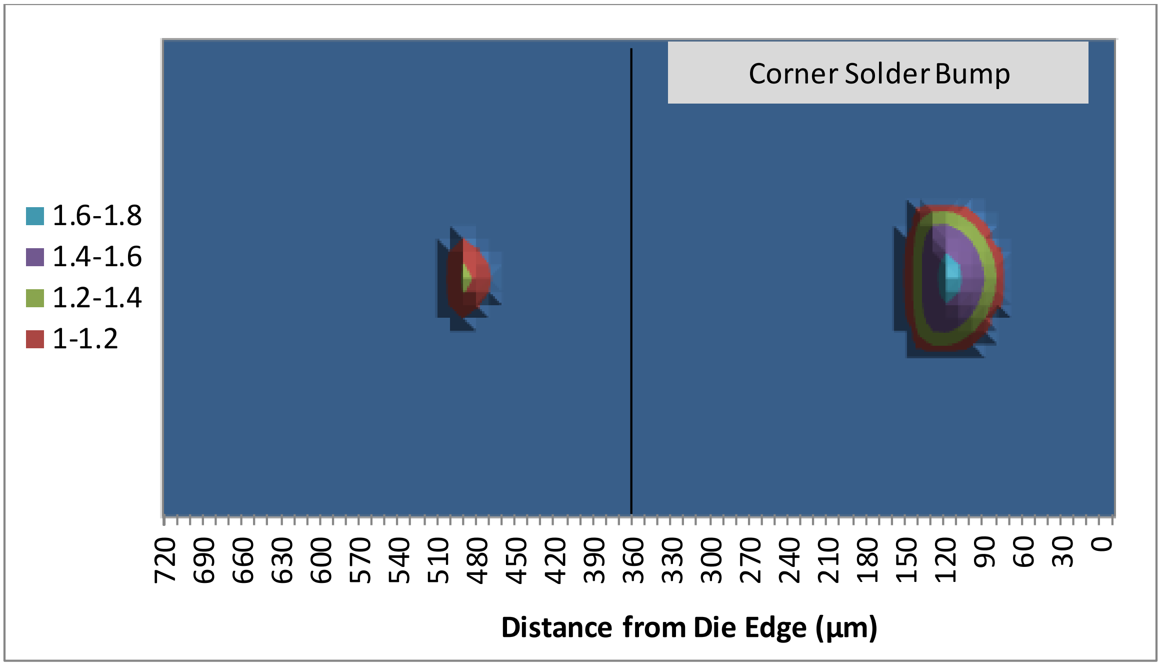


Figure 8-9. Damage profile of corner solder bump compared and the bump next to it at room temperature

8.4 CHIP-PACKAGE INTERACTION

8.4.1 Effect of Die Thickness

Global model and local model simulations varying the die thickness are performed. Similar to previous cases, the displacement constraints from the corner solder bump at room temperature is applied to the local model. The damage accrued by the cohesive elements is plotted for each case against the distance of the cohesive element from the edge of the die in Figure 8-10. The failure region for standard 780 µm thick die at room temperature is shown in Figure 8-8. It can be seen from Figure 8-8 and Figure 8-10, that the failure region reduces in size as the die thickness is reduced, and for a die thickness of 300 µm, none of the CZ elements failed. In other words, the model predicts that there will not be any white-bump failures when a 300 μm thick die is used for the flip-chip assembly instead of the standard full thickness die.

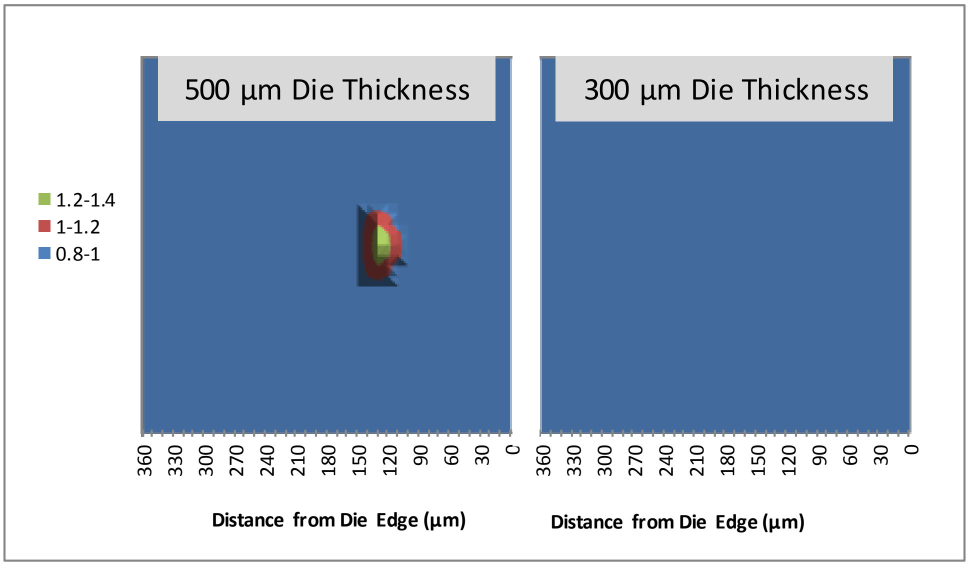


Figure 8-10. Damage profile at room temperature for different die thickness

8.4.2 Effect of Substrate Core Material Properties

Global model and corresponding local model simulations are performed considering a commercially available substrate with approximately 40% less CTE compared to the standard substrate used in the assembly. The properties of low CTE are given in Table 4-8 and the properties of the standard core substrate are given in Table 4-3. The thickness of the core is 400 μm and total thickness of the substrate is 730 μm. The CTE of standard core is 16ppm/°C in-plane and 23 ppm/°C out-of-plane. The low CTE substrate with the same thickness has 10 ppm/°C in-plane and 22 ppm/°C out-of-plane. Similarly, the damage is calculated for all CZ elements placed along the critical ULK layer. It is seen that, with reduction in CTE by 40% there is no damage predicted by the model. In other words, if the substrate core CTE is reduced by 40%, the model predicts that there will not be any white-bump failures at the end of flip-chip assembly reflow process.

8.5 SUMMARY

Cohesive zone model based 3D finite-element models are developed to predict white-bump failures at the end of flip-chip chip-attach process. Mixed-mode CZ parameters are extracted from fracture characterization experiments. Global-local 3D FE models are developed with CZ elements placed along the critical ULK layer in the local model. Global model is simulated to go through the reflow process and the displacements from the corner solder bump are applied as constraints to the local model at various intermediate temperatures. Failure region or crack is predicted using mixed-mode damage equations and the calculated damage across the entire layer is plotted against the distance of the element from the edge of the die. Such a model is then used to predict the crack initiation temperature during the cool-down from reflow temperature to room temperature. It is seen that the crack initializes at 85 °C above the Al pad edge. It is shown that the crack gradually increases in size as the assembly is cooled down to room temperature and it is confined to one side of the bump. Also, a local model of bumps away from the die edge is created, and it can be seen that the last two bumps near the die edge will fail during flip-chip assembly at room temperature. Furthermore, the effect of chip interaction parameters on flip-chip assembly reliability is studied using the developed models. The models predict that a die thickness of less than 300 µm on a substrate of thickness 730 µm, or a substrate CTE reduction by 40%, can effectively mitigate the white-bump risk.

CHAPTER 9

BUMP SHEAR TEST

White-bumps occur due to thermo-mechanical stresses experienced by the bumps at the end of flip-chip assembly process. As predicted by CZ based and fracture-mechanics based FE models, corner solder bumps are subjected to highest thermo-mechanical stresses. Therefore, corner solder bump suffer highest white-bump risk. White-bump failure locations observed at the end of reflow for C45 flip-chip assembly used in this study are shown in Figure 9-1. It can be seen that white-bumps are predominantly located along the long edge of the die. However, bumps along the long edge of the die suffer lower thermo-mechanical stress compared to the bumps along the short edge, owing to lesser distance from the center of the die (neutral point). Furthermore, as indicated by red squares in Figure 9-1, two bumps at same distance from the neutral point, may exhibit totally different white-bump signatures. In other words, two bumps subjected to apparently same amount of thermo-mechanical stresses and same process history can exhibit difference in failure pattern. Current numerical models nor interfacial fracture characterization experiments, including the models and experiments discussed in this work so far are not capable of predicting such a failure. Such a behavior is possible only if the adhesion strength of the ILD layers are not constant but varies spatially from bump to bump. The difference in adhesion strength between adjacent bumps can be attributed to the difference in trace pattern layout or via distribution. Also, with each new technology introduction, the thickness of layers present in BEOL stack are continuously shrinking and this makes it difficult to reliably characterize the fracture strength with existing techniques. In order to understand the failure at the bump level that is sensitive to capture differences in local trace patterns, microscale test techniques need to be developed.

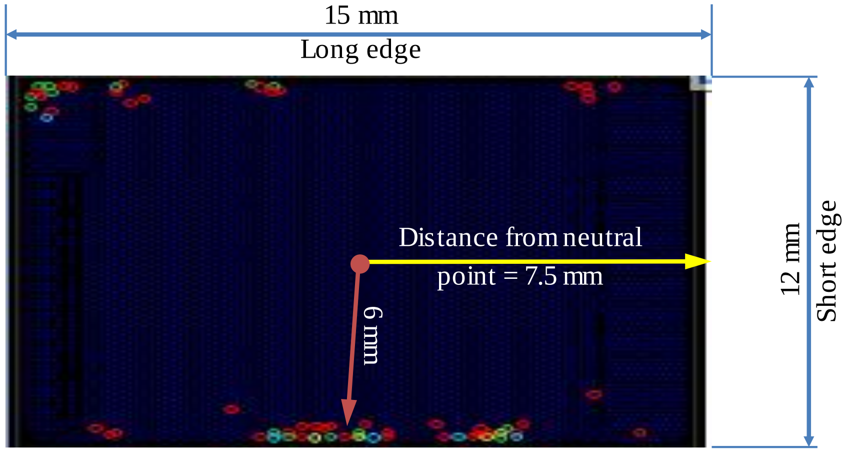


Figure 9-1. White-bump locations (red circles)

9.1 EXISTING MICROSCALE TEST TECHNIQUES

Indentation techniques using nano-indenter have been used in literature to study the variation in mechanical properties across a sample. However, the primary challenge in using indentation technique to measure adhesion strength is plastic deformation of thin-films. Plastic deformation results in pile up around the indentation rather than crack propagation. Such a deformation can be avoided by depositing a hard super-layer capable for storing large amounts of elastic energy [127, 128]. Upon indentation a blister is formed around the indent and the adhesion strength can be determined from the area of the blister, super layer material properties, and contact radius of the indenter. However, the measured values show a large variation in results (20 to 30%) and involve complicated post-processing. Thus, nano-indentation techniques have been successfully demonstrated to provide qualitative estimates of adhesion strength of blanket thin-film deposited on a substrate. However, application of nano-indentation to study multilayer stack failure is limited in application as well as capability. Two techniques available in literature that use nano-indenter to study crack propagation through multimaterial stack are cross-sectional nano-indentation (CSN) and bump assisted BEOL stability indentation (BABSI) tests.

9.1.1 Cross-Sectional Nano-Indentation

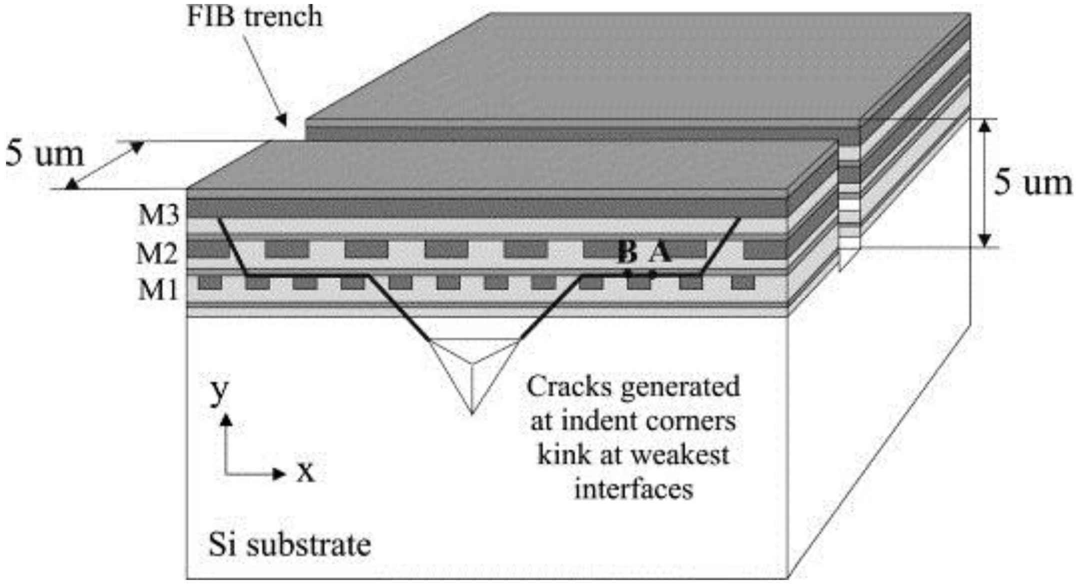


Figure 9-2. Schematic of CSN test [129]

Schematic of the CSN test is shown in Figure 9-2 [129]. As shown, the test involves indenting the sample below the thin-film stack using a three-sided pyramidal (Berkovich) type indenter. During indentation, cracks are generated from the indent corners and proceed towards the stack. Further loading propagates the crack through the BEOL stack as shown. The authors note that the indentation load at which fracture through the BEOL stack occurs is a function of distance of the indentation from the bottom of the stack and is insensitive to change in material configuration. However, the length of crack propagation through the stack can provide a qualitative estimate of the adhesion strength of the film. Furthermore, the test technique requires sophisticated sample preparation steps which involve mechanical polishing of the indentation surface and milling a trench at the backside to get reliable results. Such a technique is complicated to setup, requires sophisticated tools and finally does not provide a quantitative estimate of the adhesion strength.

9.1.2 Bump Assisted BEOL Stability Indentation

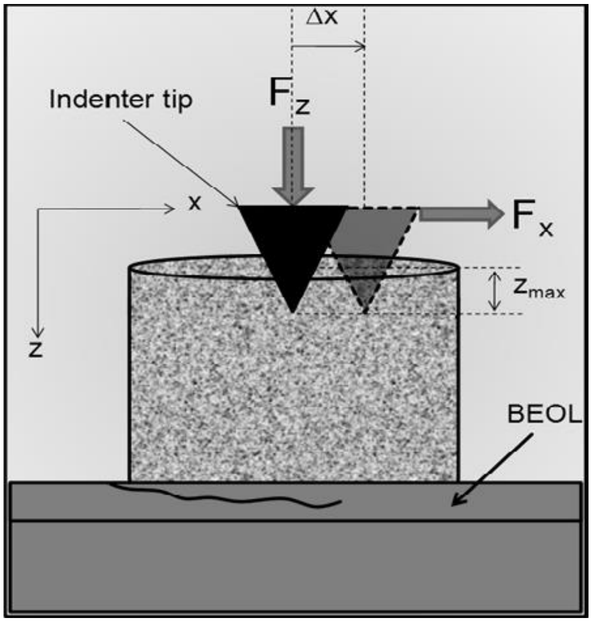


Figure 9-3. Schematic of BABSI Test [130]

BABSI test is performed using a nano-indenter with high load head and scratch test option. As shown in the schematic Figure 9-3, wedge type indenter is first latched on the individual copper pillar by applying a force in the vertical direction then a lateral force is applied. As shown in the schematic, a crack emanates from the root of the copper pillar and proceeds into the stack. As seen in Figure 9-4, a drop in measured lateral force in the lateral force vs displacement curve is attributed to the crack generated at the root of copper pillar. The critical lateral force is used as a measure for the adhesion strength.

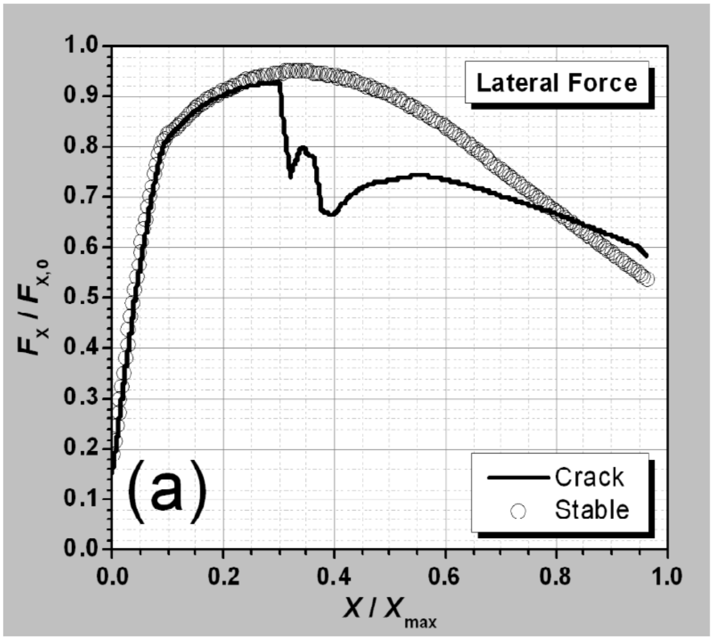


Figure 9-4. Lateral force vs displacement – BABSI test [130]

However, the test technique first involves indenting the copper pillar and the compressive force may crack the porous layers underneath. Also, such a test technique does not yield a critical force value for all the pillars tested. As shown in Figure 9-5, in some cases the indenter scratches the surface without latching on-to the copper pillar when the lateral force is applied. If such a behavior is observed, the authors conclude that the stack has higher adhesion strength. Also, complicated post-processing considering the plastic deformation of the copper pillar, height of the copper pillar, maximum compressive force required to indent the copper pillar surface and fine-tuning of the process parameters are required to yield reliable lateral force values. However, the test does provide a qualitative estimate of the adhesion strength via the measured lateral force value.

Figure 9-5. BABSI test scratching the surface of Cu pillar [131]

9.2 TEST DESCRIPTION

The focus of this chapter is to demonstrate a new reliable microscale test technique for thin-film fracture characteriztion. In the proposed technique, forces are directly exerted on bumps electroplated on pads present on top of the multimaterial thin-film stack, as shown in Figure 9-6. The thin-film stack underneath the bumps is subjected to both tensile and shearing reaction forces due to the applied load, as shown schematically in Figure 9-6. As seen, the reaction forces closely match the reaction forces experienced by the bump during flip-chip chip-attach process. Once the applied force exceeds the critical force required for crack propagation the weakest layer present in the stack delaminates. Since, the entire stack is subjected to same amount of force and there is no change in temperature during the test, the critical force requried to crack the ILD layers can be directly used as a fracture parameter without the need for any post-processing.

A nano-indenter with high-load head attachment and 20 μm spherical indenter is used to apply the point force indicated in Figure 9-6. The height of each bump is measured using the optical microscope present in the nanoindenter and the head is positioned such that the force is applied close to the center of each tested bump. The high load head can measure up to 1000 mN and 20 μm spherical indenter is chosen because the diameter of the bump is approximately 100 μm.

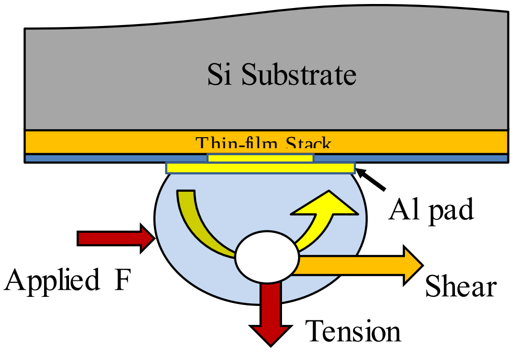


Figure 9-6. Schematic of the proposed test technique

It should be pointed out that there is no pre-crack fabricated as the samples are directly obtained from wafer-fab. Once the applied force reaches a critical value, the weakest layer in the stack delaminates. Therefore, the test technique can identify the weakest layer in the thin-film stack. Also, the test technique does not call for sophisticated sample preparation steps like notching or mechanical polishing, as required by interfacial fracture tests presented in CHAPTER 5. The critical force is a direct measure of the adhesion strength of the weakest layer in the thin-film stack. Some of the advantages of this techique are,

- The test is sensitive to variations in adhesion strength due to local variations in metal pattern density or via layout or specialized treaments such as UV cure subjected to certain parts of the wafer.
- The test requires a simple setup and does not require any complicated sample preparation steps

- Since the test technique indents the bump along the periphery, a single die yields as many samples as the number of bumps along the periphery. Inner bumps can also be tested after hand-polishing of outer rows of bumps.
- The test technique does not call for complicated post-processing or finite-element techniques to evaluate the fracture parameter.
- Finally, fatigue characterization is also possible by repeated application of the force at the same bump till a fracture is observed. Such a characterization is possible because the bump is not deformed plastically during the test, as explained in the following sections.

9.3 EXPERIMENT SETUP

The sample obtained for the study is an individual C45 die with first-level solder bump interconnects. The sample is diced from the wafer using *DISCO DAD 321* dicing saw along the dicing streaks. As mentioned before, crack-stop structures around each die prevent the micro-cracks generated during dicing from propagating into the sample. Therefore, the sample with no pre-crack is mounted on the fixture using epoxy glue or a double-sided sticky tape as shown in Figure 9-7. The fixture is then glued on to the nano-indenter table. An optical microscope present in the nano-indenter is used to measure the height of each bump and to ensure that load is applied close to the center of the bump. A 20 µm radius spherical nano-indenter tip is used for applying the load, as shown in Figure 9-8.

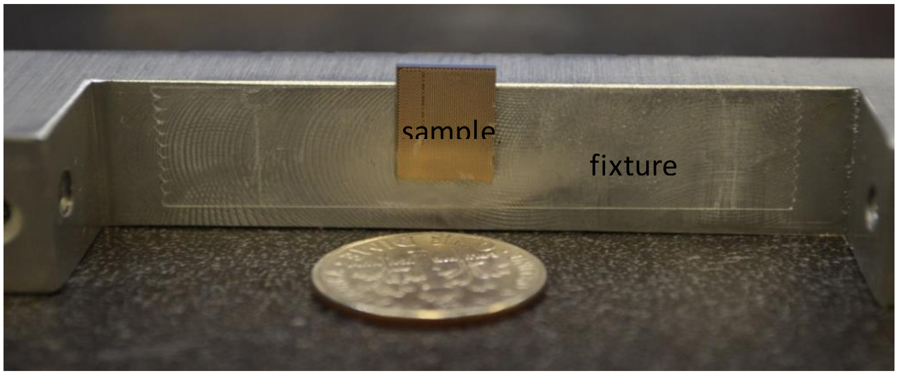


Figure 9-7. Sample attached to fixture

The diamond indenter tip has a modulus of ~1220 GPa, while the modulus of lead-free solder at room temperature is 50 GPa. Since the modulus of the indenter is two orders higher than the bump, the bump can deform plastically when loaded. Figure 9-9 shows two adjacent bumps, and it can be seen that the bump loaded with nano-indenter has deformed plastically. Due to the plastic deformation of bumps, forces large enough to fracture the BEOL stack layers underneath the bump are not achieved. In energy perspective, most of the energy is dissipitated due to plastic deformation of the bump and the energy available for delaminating the ILD layers is not large enough to effect the delamination.

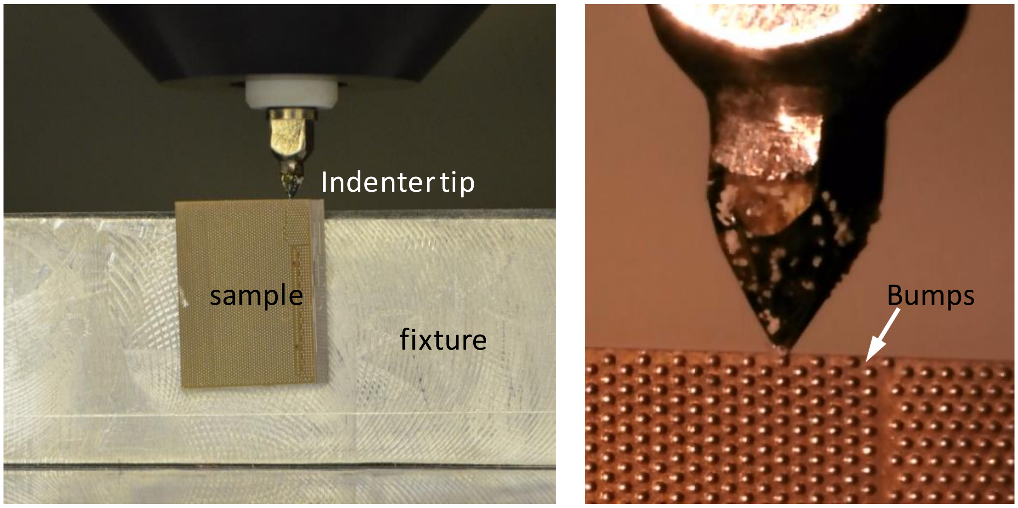


Figure 9-8. Bump shear test experiment setup

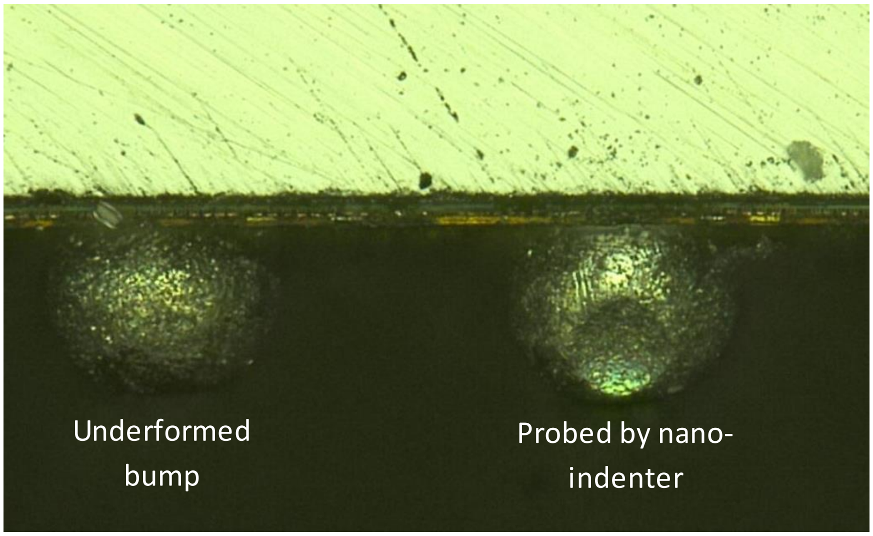


Figure 9-9. Plastic deformation of uncoated bump

In order to prevent plastic deformation of the solder bump, hard silicon nitride film is coated on the bump. The purpose of the coating is to prevent the nano-indenter tip from reaching the solder bump during indentation. The most common method for dielectric deposition on substrate is PECVD (plasma enhanced chemical vapor deposition). Standard PECVD recipes call for depositon temperatures in the range of 250-400 °C depending on the quality of the deposited film. However, the melting temperature of lead-free solder bump is around 220 °C, therefore Oxford ICP PECVD tool (inductively coupled plasma, plasma enhanced chemical vapor deposition) is chosen for deposition of silicon nitride. ICP enables low temperature deposition of dielectrics using PECVD technique. The deposition temperature is set to 20 °C and the deposition is done for two hours using the standard recipe.

Figure 9-10 shows the plane along which the bump is cross-sectioned to check the coated profile. Cross-sectioning is done by vacuum molding the sample and fine polishing. The epoxy mold protects the thin-films from cracking during polishing and vacuum ensures that there are no air bubbles get entrapped during curing. As shown in

Figure 9-10, a conformal Silicon nitride is coated on the bump. The thickness of the coating is around 4 µm near the top of the bump, 3 µm near the center of the bump and 1 µm around the base of the bump. Although the thickness of the silicon nitride film is not uniform around the bump, the thickness is large enough to prevent the nano-indenter from reaching the solder bump. It should also be noted that indenter applies the force on the bump and does not indent the coating.

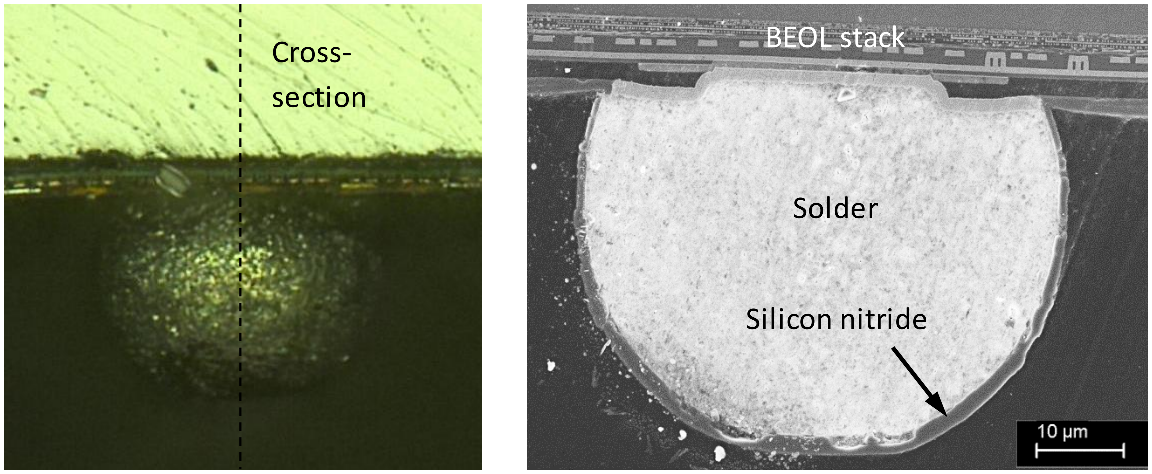


Figure 9-10. Silicon nitride coated bump cross-section

A displacement controlled test is performed, and a typical load vs displacement curve obtained from the test is shown in Figure 9-12. As seen, the force increases with applied displacement and once the force reaches a critical value it drops suddenly indicating fracture of the stack. As mentioned before, no pre-existing crack is introduced in the BEOL stack and the measured critical force is a direct measure of the adhesion strength of the weakest layer present in the thin-film stack.

Figure 9-11 shows the optical image and SEM cross-section of the bumps tested after silicon nitride coating. The arrow in the SEM cross-section image indicates the load application direction. It can be seen from the optical image that the bumps are not plastically deformed and from the cross-section that the silicon nitride layer did not crack during the test.

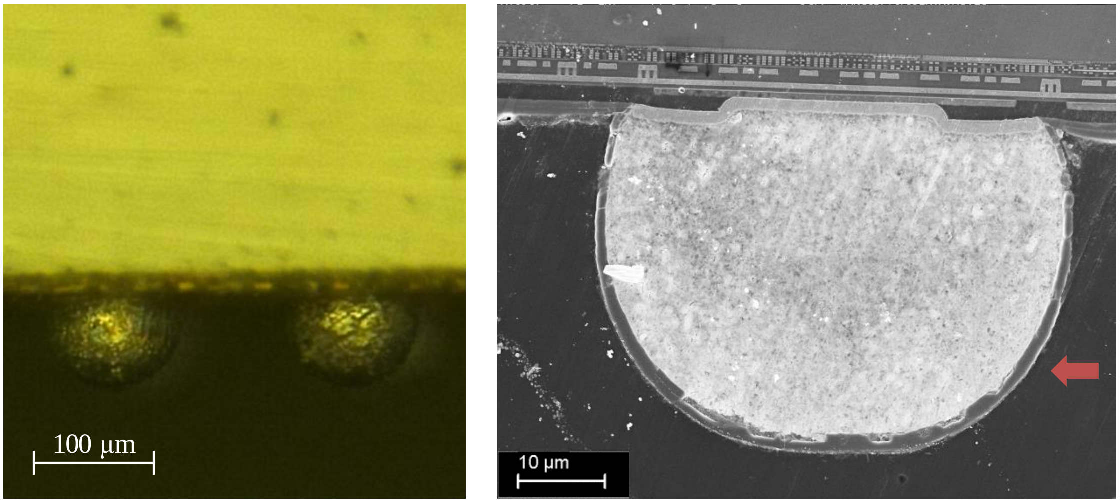


Figure 9-11. Optical image and SEM cross-section of bumps tested after silicon nitride coating

9.4 EXPERIMENT RESULTS

The load-displacement curve obtained for six samples is shown in Figure 9-13 and as seen, the critical force value ranges between 210 to 315 mN. Three sample dies are diced from a wafer. Several bumps present in three dies are tested and the critical force obtained from all the twenty seven bumps is shown in Figure 9-14. Bump 1 through 8 are obtained from Sample 1, Bumps 9 through 18 are obtained from Sample 2 and the remaining bumps are obtained from Sample 3. The critical froce value varies between 80 mN to 350 mN across three different samples and twenty-seven bumps tested. It is evident that critical fracture parameter is not constant and it varies spatially across a sample as well as between samples. Such differences across samples are expected because the bump locations are not consistent across samples. It should be pointed out that the BEOL trace pattern distribution and via densities vary from one bump to adjacent bump in the same sample. For example, bump delivering power to the transistor can have a totally different trace pattern distribution compared to a bump transferring signal from transistor to the package. Such variations contribute to the difference in critical force between bumps present in the same sample. The average critical force is 234 mN, and it can be seen that the majority of the bumps fail around this load.

The effect of residual stresses in silicon nitride on the critical force can also be studied. First, the residual stresses in silicon nitride layer can be characterized by depositing blanket layers of silicon nitride of known thickness on bare silicon wafers. The stresses can then be determined from the curvature measurement. It can be seen from Figure 9-10 and Figure 9-11 that thickness of the silicon nitride layer deposited is around 1 – 2 µm. Since the thickness of silicon nitride layer is an order lower than the diameter of the solder bump, the effect of residual stresses on critical force is assumed to be negligible in this work.

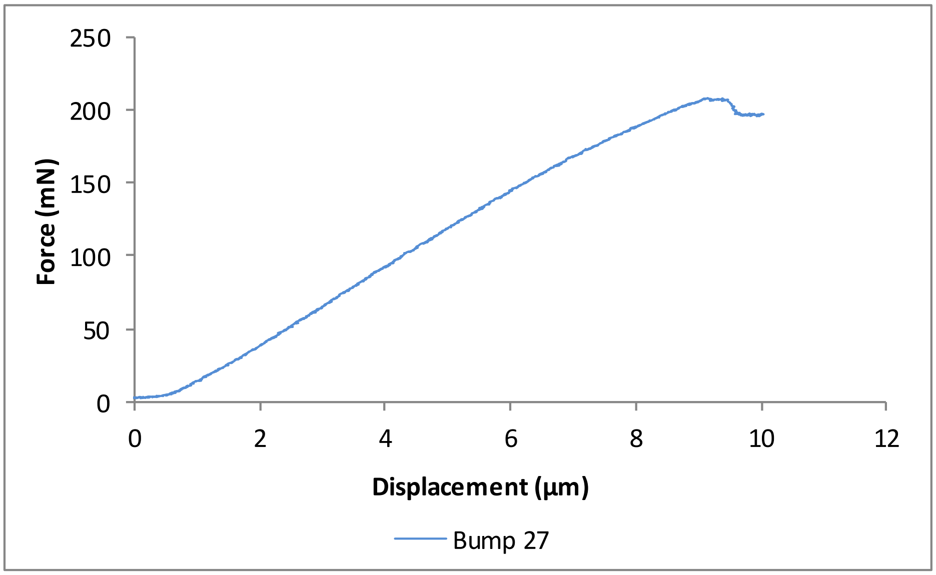


Figure 9-12. Typical load vs displacement

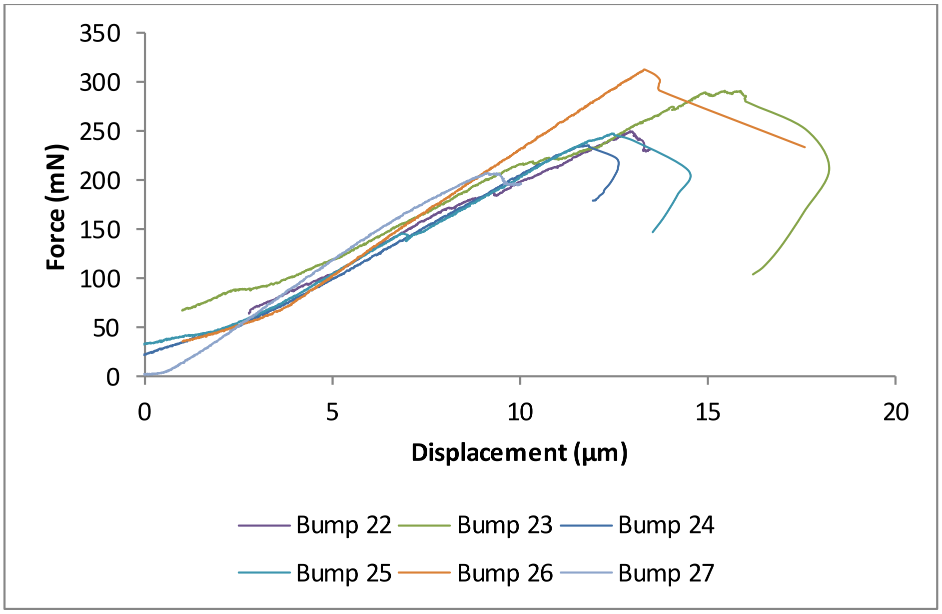


Figure 9-13. Load vs displacement curve obtained for several samples

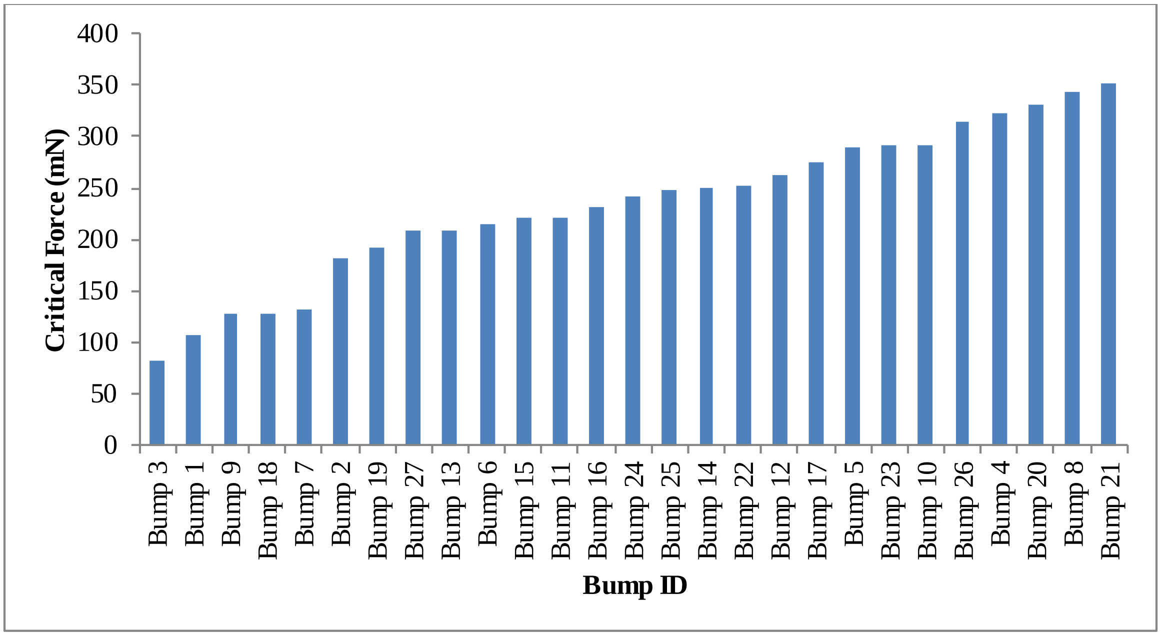


Figure 9-14. Critical force obtained from all bumps

9.5 FAILURE ANALYSIS

In order to determine the crack path, the sample is molded in vaccum and then the tested bumps are cross-sectioned by hand-polishing. Polishing is done at low speeds (100 rpm) starting with 400 grit to reach close to the center of the failed bump, followed by fine-polishing so that the sample can be imaged using SEM. Low speeds also ensure that the polishing process does not induce any damage to the thin-films. The cross-section is shown in Figure 9-15. As seen, a crack can be clearly seen to have initated in one of the ULK layers around the Al pad edge. Figure 9-16 shows that crack propagates in-between B3 and B4 layers. It should be pointed out that, crack is confined to one side of the bump and the propagation in-between B3 and B4 layers compares well with white-bump failure observed at the end of flip-chip chip-attach process presented in CHAPTER 4 and CHAPTER 8.

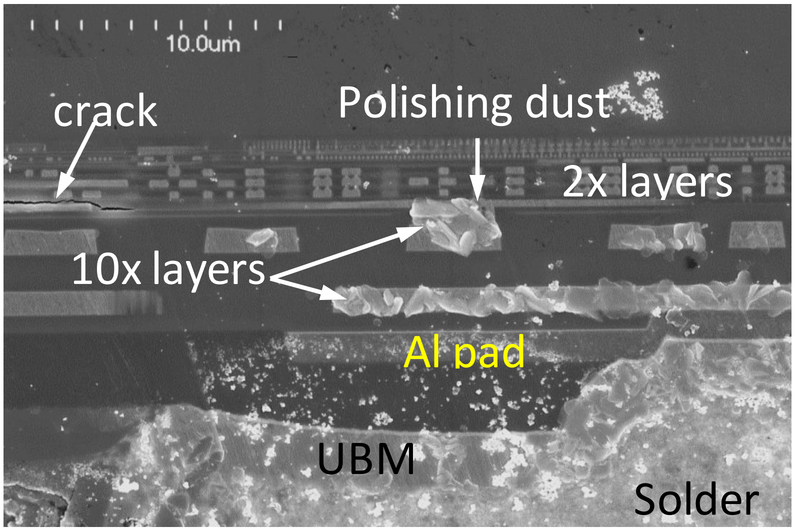


Figure 9-15. Cross-section of the bump showing crack initiation location

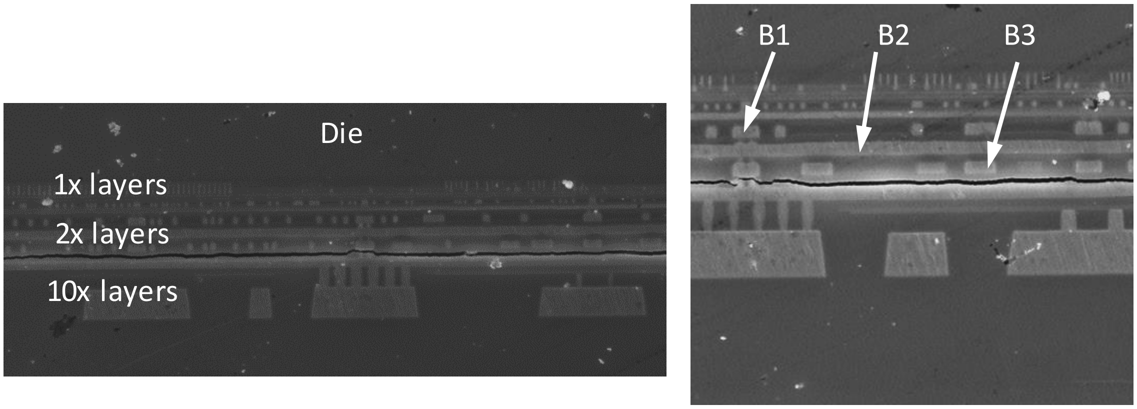


Figure 9-16. Crack propagation along the ULK layer

9.6 NUMERICAL MODELING

Schematic of the FE model of the test along with boundary conditions is shown in Figure 9-17. As seen, top of the silicon die is constrained in all degrees of freedom and displacement is applied to one node in the solder bump. Figure 9-18 shows the 3D FE model of the test setup built using ANSYS. Since, the fracture is confined to one bump during testing, the planar dimensions of the model are chosen to be equal to one-and-half pitch (540 μm). It can be seen from the cross-section shown in the inset of Figure 9-18 that, all the layers present in the BEOL stack are modeled along with solder, Al pad, UBM, PI, and a one-tenth the thickness of the silicon die. The silicon nitride coating is not modeled, instead solder is considered to be linear-elastic material. As shown,CZ elements are embedded across the entire layer along the critical B3/B4 ULK interface present in the BEOL stack. The CZ elements are characterized by mixed-mode CZ parameters extracted from interface fracture characterization experiments outlined in previous chapters. Contact elements are overlaid on CZ elements to prevent inter-penetration of cohesive surfaces. The displacement is applied gradually on the bump at one node and the reaction forces are calculated at several sub-steps during the simulation.

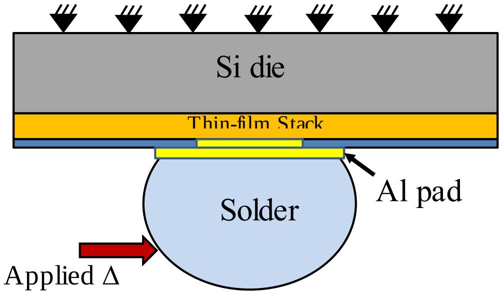


Figure 9-17. Schematic of FE model with boundary conditions

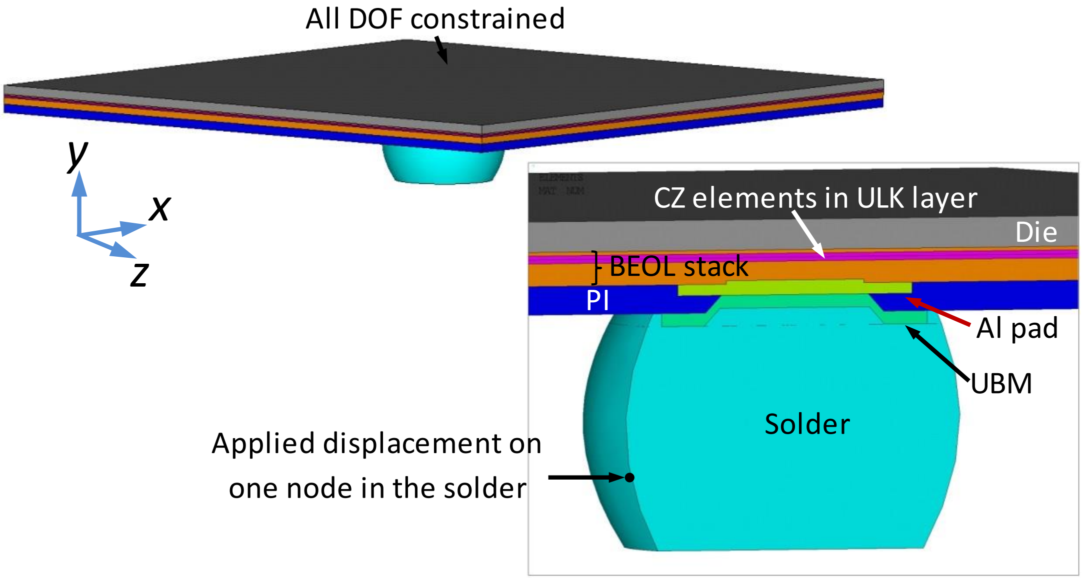


Figure 9-18. 3D FE model

Although, optical microscope is used to position the load-head in experiments to be close to the center of the bump, the exact location at which load is applied is unknown. Therefore, numerical models with different load application locations are simulated. Displacements are applied at the center of the bump, top of the bump and at a location in-between the two previous locations. The locations of applied displacement from the critical ULK layer are schematically shown in Figure 9-19. Separate simulations are performed for each case and the load vs displacement plot for each case is shown in Figure 9-20. It can be seen from Figure 9-20 that the slope of the load-dispalcement curve is stiffer when the load is applied at the center of the bump and the stiffness reduces as the loading location is moved towards to the top of the bump. Such a behavior is expected because the test is analogous to a cantilever beam. It can be seen that, all three locations follow the typical trend from the experiments. When simulation results are overlaid on experiments as shown in Figure 9-20, it appears that the initial slope as well as the critical force predicted by model when load application location is 64 µm seems appropriate.

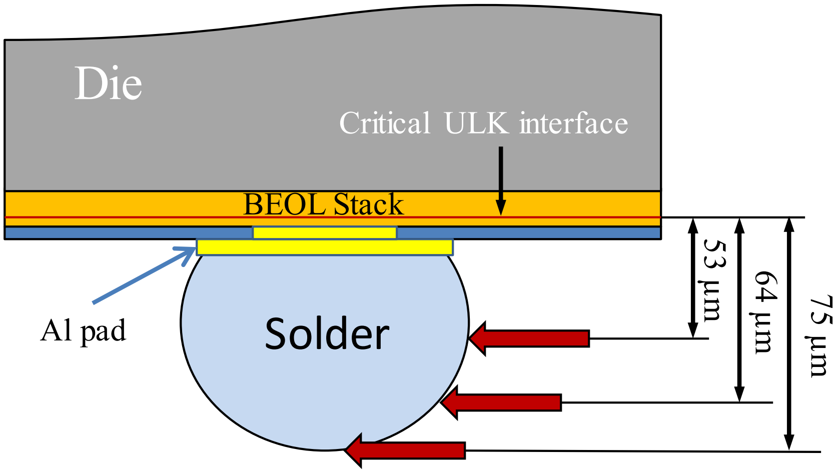


Figure 9-19. Applied displacement locations during simulation

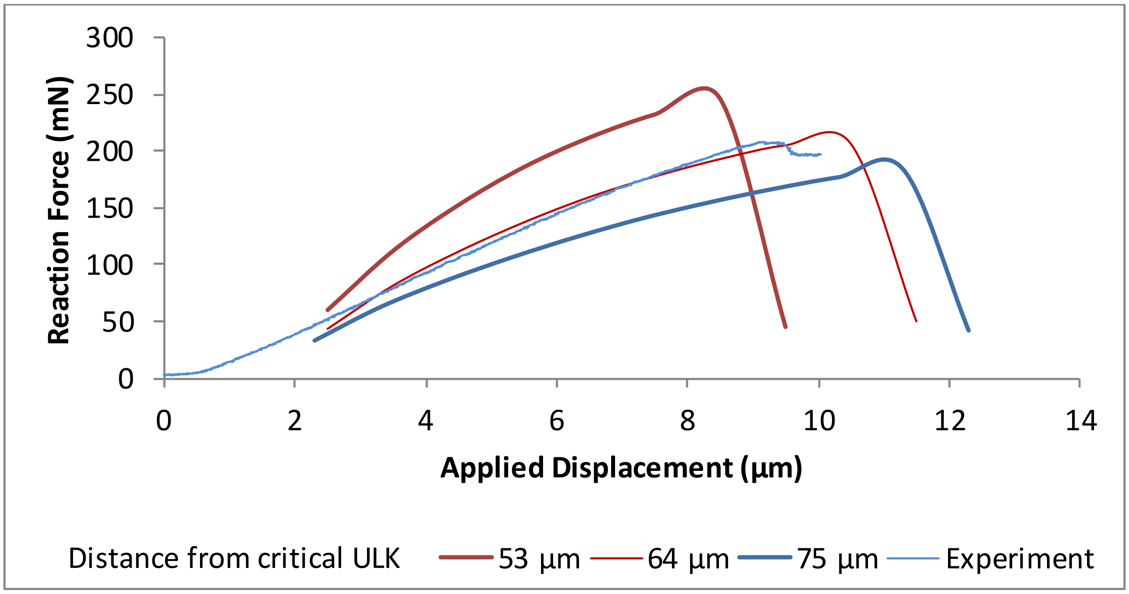


Figure 9-20. P-δ curve for displacement applied at several locations

Figure 9-21 shows the resulting resulting reaction forces obtained from the simulation plotted against the applied displacement, for load application location of 64μm from the critical ULK layer. Figure 9-21 also shows the experiment results obtained from Bump 22 through Bump 27. As seen from Figure 9-21, the model is able to capture the average critical force as well as the loading slope.

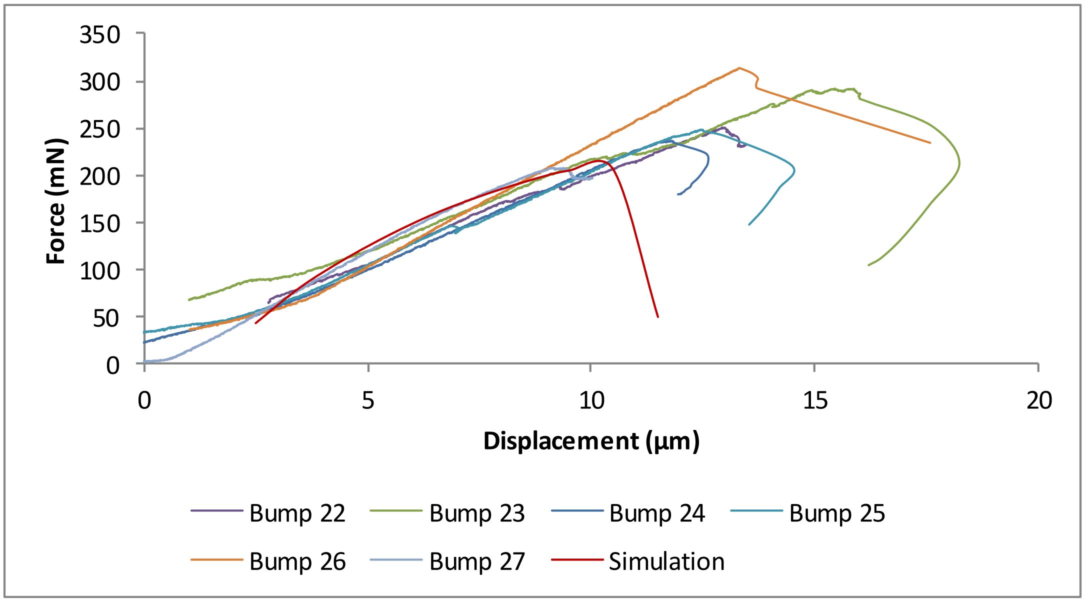


Figure 9-21. P-δ obtained from simulations compared against experiments

The resulting displacement profile in *y*-direction is shown in Figure 9-22. The CZ elements are removed in order to visualize the fully-damaged area. It can be seen that, the damage is confined to one side of the bump. Figure 9-23 shows the damage calculated at all nodes present in the critical ULK layer when the load is applied at 64 μm from the critical ULK layer, similar to the plots shown in Section 8.2. Since the planar dimensions are 1.5 times the pitch, the *x*-axis spans a width of 540 μm. The fully-damaged region (d_m > 1) is plotted in different colors, whereas partially-damaged and the undamaged region (d_m < 1) is plotted in dark blue. As seen from Figure 9-23, the model predicts that the elements around the Al pad edge region suffer the maximum damage. This corresponds well with the maximum damaged region predicted by CZ based FE models during flip-chip reflow prcess presented in CHAPTER 7 and CHAPTER 8. With further application of load, the damaged region increases in size as shown in Figure 9-23. The Figure 9-23a shows the damage calculated for an applied displacement of 7 μm. The profile compares well with white-bump damage profile predicted at room temperature, presented in CHAPTER 8. These validations also show that the developed CZ parameters are applicable to other tests beyond DCB, FPB tests. Damage profile at the critical load, when the applied displacement is around 10 μm is shown in Figure 9-23b. It can be seen that the fully damaged region is no longer confined to only one side of the bump and the damage can reach the edge of the die during bump shear test technique.

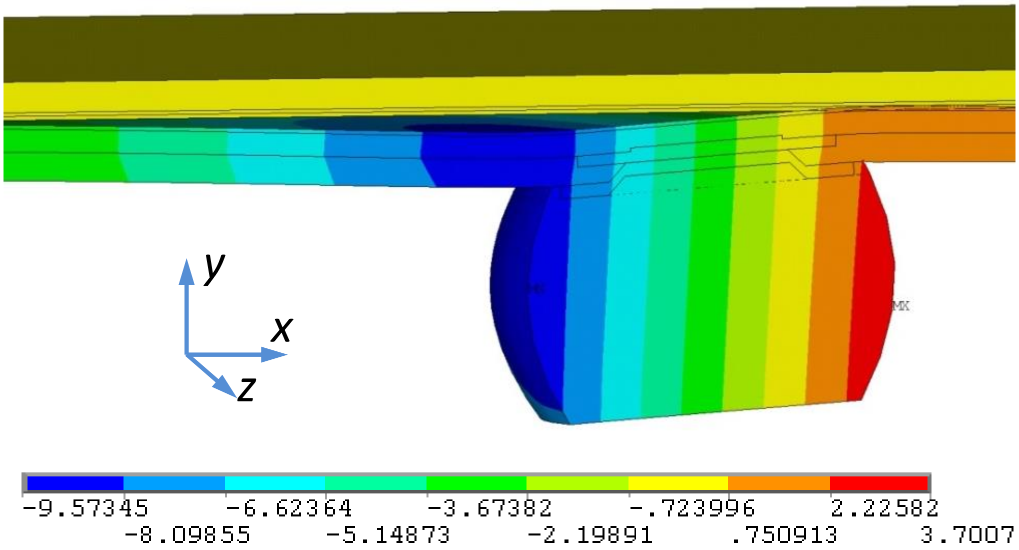


Figure 9-22. Resulting displacement contours in *y*-direction. CZ elements are removed to visualize the damaged region.

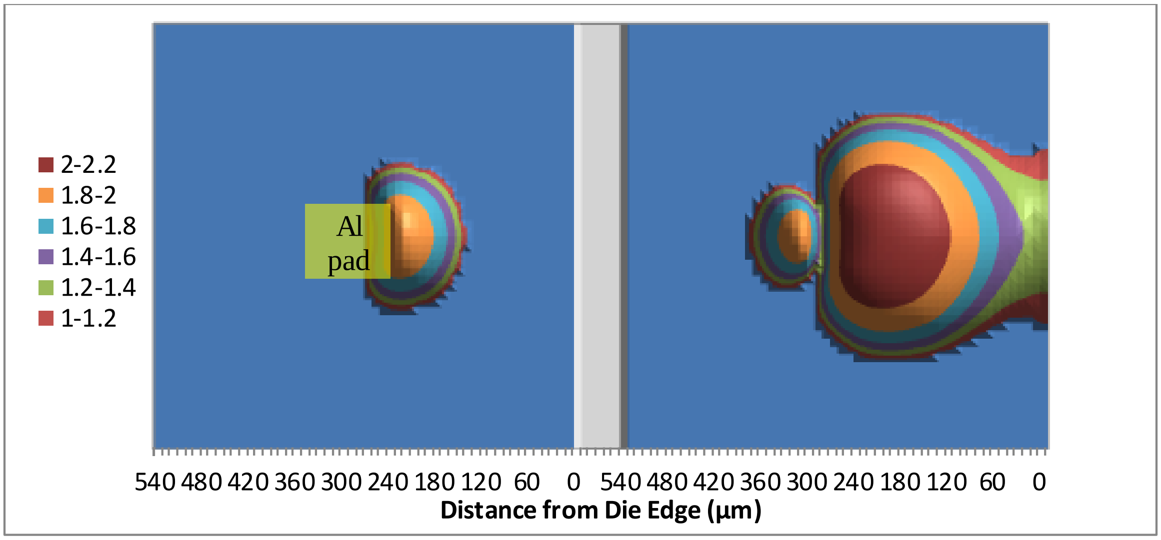


Figure 9-23. Damage propagation. a) damage calculated for an applied displacement of 7 µm b) damage calculated at critical load (applied displacement of 10 µm)

The test technique presented in this chapter provides another important insight. Unlike the DCB, FPB and 3ENF tests, it can be seen from the damage profiles that the bump shear test mimics the actual reflow process. Figure 9-24 shows the variation of critical force with respect to the location at which the load is applied. As seen, critical force required to crack the BEOL stack reduces as the loading location is moved closer to the top of the bump. The force induced by the package at the end of flip-chip assembly process is primarily due to the CTE mismatch between the die and substrate. Therefore, the force at the end of flip-chip assembly are exerted at the top of the bump rather than the center of the bump. It can be seen from Figure 9-24 that as the applied load position is moved towards the top of the bump, the force required to crack the stack reduces. Thus, the critical force measured from the test has to the multipled by a reduction factor. The reduced critical force can then be compared with forces acting at the end of flip-chip chip-attach process determined from FE models. As seen from Figure 9-24, the force varies linearly with respect to the position at which the load is applied. The reduced critical force F_c is given by,

$$F_c = \mathrm{F} - 3\ (\mathrm{d}_1 - \mathrm{d}_2) \qquad (9\text{-}1)$$

where, F is the critical force determined from the nanoindeter based bump shear test, d_1 is the height of the solder bump and d_2 is the position at which the load is applied during the test.

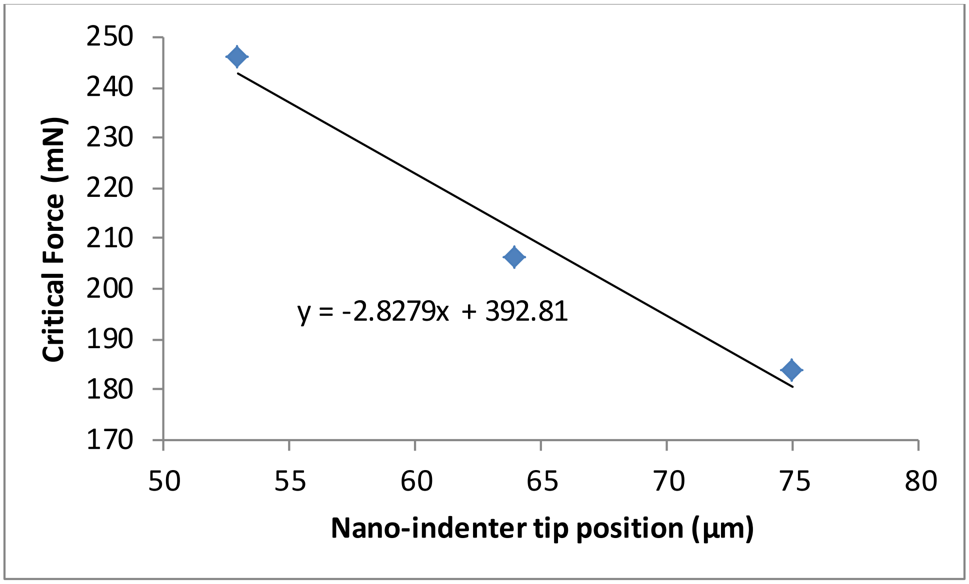


Figure 9-24. Critical force vs load application position

9.7 SUMMARY

A new nano-indenter based test technique to determine fracture parameter of thin-films is presented in this chapter. Load is applied directly on the bump using spherical nano-indenter around the center of the bump. A drop in load in the load-displacement curve indicated the critical force required for cracking the BEOL stack. The failed bump is cross-sectioned to determine the layer that delaminated in the BEOL stack. It is found that the delamination propages through the same layer that failed duirng flip-chip chip-attach process presented in previous chapter. The critical force at which the bump fails, can be used as a fracture parameter. It is seen that different bumps fail at different critical loads. Thus, the test technique is sensitive to microscale variations in adhesion strength. Such variations in adhesion strength can be attributed to the variation in trace pattern and via locations around the vicinity of the bump. It is seen that the majority of the bumps fail around 250 mN. Since, the thickness of the silicon nitride layer deposited is an order lower than the diameter of the solder bump, the effect of residual stresses in silicon nitride on critical force is assumed to be negligible. The effect of residual stresses in silicon nitride layer on the measured critical force can be studied as a future work.

The CZ based FE models of the bump shear test is created. CZ parameters characterized from interfacial fracture characterization experiments are used to simulate the test. It is shown that the simulation can mimick the load-displacement curve of the test and the critical load predicted by the simulation compares well with the average failure load obtained from experiments. Furthermore, simulations indicated that as the load application location is moved towards the top of the bump, the critical force required to crack the BEOL stack reduces linearly.

Such a test technique has several advantages compared to the existing approaches present in literature as well as approaches presented in earlier chapters. The nano-indenter based bump shear test technique can be automated to indent the bumps along the periphery to create a map of critical force required to fracture the BEOL stacks. Such an effort will be able to pin-point the weaker bumps. Furthermore, the trace patterns above the strong and weak bumps can be compared to design robust trace pattern designs and the variation in fracture parameter with respect to the orientation of applied force can also be studied with such a technique. Also, the force applied by a package on the BEOL stack can be determined using global finite-element mdoels of flip-chip packages. The force can be directly compared against the critical force. Thus, the test technique does not call for complicated post-processing or development of CZ based models to predict failure. To be conservative, the lowest measured critical force measured from the test can also be used for design calculations. Such an experiment performed on pilot batch of wafers can provide a safe die length estimate for a given die thickness and substrate material properties. The test can also be applied during process development to study variation in adhesion strength across a wafer. The test technique is not limited to microelectronic applications, it can be applied to study thin-film stacks or a blanket layer of thin-film on a substrate by electroplating bumps or copper pillars at critical locations on the substrate.

CHAPTER 10

SUMMARY, CONTRIBUTIONS AND FUTURE WORK

10.1 SUMMARY AND FINDINGS

This work has developed a combined experimental and numerical framework to study thin-film fracture. The developed framework was successfully implemented to predict ILD cracking observed in microelectronic devices during chip-attach process.

Fracture mechanics simulations were performed to predict potential failure locations around the vicinity of solder bump during flip-chip chip-attach process. The simulations indicated that a crack present above the Al pad edge has the maximum energy to propagate. Furthermore, crack propagation simulations were performed by placing a pre-crack at the critical location identified through simulations and allowing it to propagate using a failure criterion ($G > G_c$). The final crack length of 87 μm predicted by such a model compared well against the crack length determined from FIB cross-section of white-bumps failures observed in real deveices.

Such a model was then used to study impact of chip-pacakge interaction parameters on energy available for crack propagation. The models indicated that thinner die, lower CTE core substrate material, larger Al pad size and lower PI opening resulted in reduced energy available for crack propagation. Also, studies performed on parameter interaction revealed that global parameters (die thickness and substrate core CTE) have the maximum impact on the energy available for crack propagation compared to local parameters (Al pad size and PI opening). However, the models were limited in scope and application due to the inherent assumptions involved in fracture-mechanics based approaches. In order to overcome the limitations, CZ based FE models were purused to study the thin-film fracture.

The CZ interface elements were characterized by bilinear traction-separation law. In order to determine the CZ parameters that define the traction-separation law, interface fracture characterization experiments were performed. Appropriately modified interface fracture characterization bend tests were carried out using sandiwch specimens. The test specimens were diced from C45 wafers obtained from wafer-fabs with no pre-facbricated crack. Modified FPB test was leveraged to identify the weakest layer present in the thin-film stack and to create a pre-crack required for DCB and 3ENF tests. These tests characterized the critical interface over a wide-range of mode-mixities.

The average G_{Ic} determined from DCB tests was 4.61 J/m^2. The average G_{IIc} determined from 3ENF test was found to be 22.1 J/m^2. The average mixed-mode G_c determined from FPB test was 7.14 J/m^2. FIB cross-sections of failed samples revealed that the crack propagated majorly along the same interface that failed during flip-chip chip-attach process.

The experimental data – critical energy release rate and load vs. displacement – were used to develop the mixed-mode traction-separation law. The mixed-mode bilinear T-δ law required six independent parameters to be determined. Two parameters were directly obtained from bend test experiments (G_{Ic} and G_{IIc}). The remaining mode I T-δ parameters (T_n^{max} and δ_n^c) were obtained by performing simulations mimicking load-displacement curve of DCB test. The remaining mode II T-δ parameters (T_t^{max} and δ_t^c) were obtained by performing simulations mimicking load-displacement curve of FPB test.

As a next step, CZ based FE models were developed to predict microelectronic device failure at the end of chip-attach process. Two-dimensional and three-dimensional FE models of flip-chip assembly were simulated to go through the chip-attach process. The CZ elements were placed along the critical layer present in the BEOL stack. The critical layer was identified from FIB cross-sections of white-bumps observed in real devices and bend-test experiment samples.

The 3D CZ based FE simulations predicted that damage initiated above the Al pad edge at around 84 °C. The damage region increases in size as the model was simulated to cool-down and was confined to one side of the solder bump. The fully-damaged region at room temperature spanned a length of 80 µm. The span of fully-damaged region was successfully compared against crack lengths measured from FIB cross-sections of white-bump failures observed in real devices. The 2D CZ based models were able to predict simultaneous failure of multiple bumps during the cool-down process using a single model. It should be pointed out that, there was no pre-crack introduced in the 2D and 3D CZ based FE models. The CZ model can identify the damage initation location, propagation front and the fully-damaged region region, all in a single load-step simulation process without any need for re-meshing. Such models were then used to study the impact of chip-pacakge interaction parameters on white-bump failure risk. The models indicated that, if the die thickness was reduced to 300 µm from 780 µm or if the CTE of the core was reduced by 40%, package induced white-bump failures can be avoided.

The three-dimensional CZ based FE models predicted the failure region around the corner solder bumps, however white-bumps observed at thermo-mechanically “weaker” locations cannot be captured using the numerical models. Therefore, a new nanoindenter based microscale test technique to determine the critical fracture parameter of blanket layer of thin-film or thin-film stacks was developed. The test technique is sensitive to capture the variations in fracture parameter across an interface. In the proposed technique, point force was directly applied on a solder bump using a nano-indenter. In order to prevent plastic deformation of the bump, the bump was conformally coated with silicon nitride. The critical force required to create a delamination in the stack was a direct measure of fracture strength of the material. The critical force varied between 80 mN to 350 mN and majority of bumps failed at an average critical force of around 230 mN. The variation in critical force can be attributed to the variations in trace pattern layout or via locations. Such a variation also explains the reason for white-bump failures observed around thermo-mechanically “weaker” locations. Cross-sections of bump tested reveal that the failed interface during the test was consistent with FIB cross-sections of white-bump failures observed in real devices and interfacial fracture test specimens.

Three-dimensional CZ based FE simulations of the test were performed. The CZ elements were characterized by the parameters determined from interfacial fracture test experiments. The simulations were able to capture the load-dispalcement curve obtained from the test. The critical load predicted by the simulation was 210 mN when the load was applied at the center of the bump. Thus, the simulation was able to capture the average critical load required to crack the interface and the load-displacement profile. Such an FE model was then used to predict variation in critical force with respect to the load application location. It was shown that, as the point of load application increases from the failure interface, the critical force required to crack reduces. Thus, the methodology developed in this work will contribute to understanding and reducing on-chip delamination through the use of experimentally-characterized cohesive zone models.

10.2 RESEARCH CONTRIBUTIONS

This work has made important research contributions in the area of sub-micron thin film cracking. In particular,

- This work has developed appropriately-modified experimental characterization techniques to study interfacial crack propagation in sub-micron layers. In particular, this work has used a FPB test to create a starter delamination in sub-micron layer BEOL stack, and used such delaminations to experimentally study two extreme mode mixities, ranging from 0.08 degrees to 89.98 degrees.
- This work has characterized the mixed-mode CZ parameters using experiment results through inverse analysis technique. In particular, this work has used the combination of critical energy release rate as well as load vs. displacement curve for three independent tests to be able to characterize all of the parameters of mixed-mode traction-separation laws. Such a characterization over a range of mode mixity is probably first of its kind available in open literature.
- This work has employed the developed cohesive zone model to determine the onset and propagation of interfacial crack in a flip-chip assembly. In particular, this work has developed a numerical model that can mimic the flip-chip assembly process taking into consideration the time-,

temperature-, and direction-dependent material properties with the appropriate time-temperature history, and implemented the developed cohesive zone elements at critical interfaces to study delamination initiation and propagation under assembly loading conditions. Thus, this work has successfully demonstrated that CZM technique can be used to predict delamination locations and lengths.

- This work has developed appropriate material and geometry based design guidelines to mitigate interfacial delamination and thus white-bump formation
- This work has demonstrated a new micro-scale nanoindentor-based bump shear test technique, specifically designed and developed as part of this research. The test technique is sensitive to variations in fracture parameter owing to micro-scale variations in trace patterns in the vicinity of a bump.

10.3 FUTURE WORK

- This work applied fracture-mechanics based approach to study delamination observed in ILD layers present in the BEOL stack. However, copper trace patterns and vias present in real devices were not modeled. Models considering such micro/nano scale trace pattern details may provide more insights on crack initiation and propagation.
- This work has performed interfacial fracture tests at room temperature. Such tests can be performed at other temperatures and thus, the thermo-mechanically-induced stresses as well as any potential changes of interfacial fracture toughness at different temperatures can be determined.

- This work has demonstrated the use of cohesive zone elements for one interface. It is necessary to apply and demonstrate the developed technique to sub-micron interfaces in other microelectronic, photo-voltaic, and other applications.
- Experiments at different temperatures and other loading conditions will yield to modified cohesive zone models which can be used to assess long-term reliability of intended interfaces.
- The new bump shear test technique provides information about variation in critical force due to variations in trace pattern layout or via density in the vicinity of a bump. The trace layout and via patterns of bumps that require higher critical force to fracture can be analyzed to design a more robust BEOL stack structure. This leads to larger die sizes facilitating 3D flip-chip integration as well as more functions integrated on system on chip (SOC) microelectronic packages.
- In addition to monotonic loading and interface characterization, the bump shear test technique can be implemented to study fatigue failure of BEOL stacks by performing a force-controlled test.

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