MATERIAL AND ARRAY DESIGN FOR CMUT BASED VOLUMETRIC INTRAVASCULAR AND INTRACARDIAC ULTRASOUND IMAGING

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MATERIAL AND ARRAY DESIGN FOR CMUT BASED VOLUMETRIC INTRAVASCULAR AND INTRACARDIAC ULTRASOUND IMAGING

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LIST OF SYMBOLS AND ABBREVIATIONS

List of Abbreviations:

ALD – Atomic Layer Deposition

CMUT – Capacitive Micromachined Ultrasonic Transducer

CTOs – Chronic Total Occlusions

CVD – Chemical Vapor Deposition

DES – Drug Eluting Stent

FL-IVUS – Forward Looking IVUS

IC – Integrated Circuit

ICE – Intracardio-echocardiography

LAA - left atrial appendage closure

LPCVD – Low Pressure Chemical Vapor Deposition

IVUS – Intravascular Ultrasound

PECVD – Plasma Enhanced Chemical Vapor Deposition

PMUT – Piezoelectric Micromachined Ultrasonic Transducer

PMVR - percutaneous mitral valve replacement

PZT – Lead Zirconium Titanate

Rx – Receive or Receiver

SL-IVUS – Side Looking IVUS

SNR – Signal-to-Noise Ratio

TAVI – Trans-aortic Valve Implants

TDMAHf – Tetrakis[DiMethylAmino]Hafnium

TIA – Transimpedance Amplifier

TSV – Through Silicon Via

Tx – Transmit or transmitter

List of Symbols:

$V_{COLLAPSE}$ – Collapse Voltage (Pull-in Voltage)

V_{BD} – Break down voltage

g_{eff} – Effective gap

g – Vacuum gap

t_d – Dielectric layer thickness

F_{es} – Electrostatic force

V_{PULSE} – Pulsing voltage

n – Small signal transformer ratio

V_{DC} – Direct current voltage

α – Attenuation coefficient

$I^2_{CMUT_NOISE}$ – Thermal mechanical noise current squared

$I^2_{SIGNAL_RMS}$ – Root mean square of the current from the receiver output squared

Si_xN_y – Silicon nitride

HfO_2 – Hafnium oxide

AlSi – Aluminum silica

SiN – PECVD Silicon Nitride

HfO – ALD Hafnium Oxide

SUMMARY

Recent advances in medical imaging have greatly improved the success of cardiovascular and intracardiac interventions. This research aims to improve capacitive micromachined ultrasonic transducers (CMUT) based imaging catheters for intravascular ultrasound (IVUS) and intra-cardiac echocardiography (ICE) for 3-D volumetric imaging through integration of high-k thin film material into the CMUT fabrication and array design.

CMUT-on-CMOS integration has been recently achieved and initial imaging of ex-vivo samples with adequate dynamic range for IVUS at 20MHz has been demonstrated; however, for imaging in the heart, higher sensitivities are needed for imaging up to 4-5 cm depth at 20MHz and deeper at 10MHz. Consequently, one research goal is to design 10-20MHz CMUT arrays using integrated circuit (IC) compatible micro fabrication techniques and optimizing transducer performance through high-k dielectrics such as hafnium oxide (HfO2). This thin film material is electrically characterized for its dielectric properties and thermal mechanical stress is measured. Experiments on test CMUTs show a +6dB improvement in receive (Rx) sensitivity, and +6dB improvement in transmit sensitivity in (Pa/V) as compared to a CMUT using silicon nitride isolation (Si_xN_y) layer. CMUT-on-CMOS with HfO_2 insulation is successfully integrated and images of a pig-artery was successfully obtained with a 40dB dynamic range for 1x1cm^2 planes.

Experimental demonstration of side looking capability of single chip CMUT on CMOS system based FL dual ring arrays supported by large signal and FEA simulations was presented. The experimental results which are in agreement with simulations show promising results for the viability of using FL-IVUS CMUT-on-CMOS device with dual

mode side-forward looking imaging. Three dimensional images were obtained by the CMUT-on-CMOS array for both a front facing wire and 4 wires that are placed perpendicular to the array surface and ~4 mm away laterally.

For a novel array design, a dual gap, dual frequency 2D array was designed, fabricated and verified against the large signal model for CMUTs. Three different CMUT element geometries (2 receive, 1 transmit) were designed to achieve ~20MHz and ~40MHz bands respectively in pulse-echo mode. A system level framework for designing CMUT arrays was described that include effects from imaging design requirements, acoustical cross-talk, bandwidths, signal-to-noise (SNR) optimization and considerations from IC limitations for pulse voltage. Electrical impedance measurements and hydrophone measurements comparisons between design and experiment show differences due to inaccuracies in using Si_xN_y homogenous material in simulation compared to fabricated thin-film stacks (HfO_2-AlSi-Si_xN_y). It is concluded that for “thin” membranes the effect of stiffness and mass of HfO_2 and AlSi (top electrode) cannot be ignored in the simulation. Also, it is understood that aspect ratio (width to height) <10 will have up to 15% error for center frequency predicted in air when the thin-plate approximation is used for modelling the bending stiffness of the CMUT membrane.

CHAPTER 1. INTRODUCTION AND BACKGROUND

1.1. Cardiac Medical Ultrasound Imaging

1.1.1. Brief History of Medical Ultrasound

Before the application of ultrasound in medicine, sound wave technology was first utilized during World War I as sonar to locate submarines and mines, where distance to objects was measured using transmission and reception of low frequency sound waves [1], [2]. By the beginning of WWII, the first radar systems were developed by the U.S. Navy and used electromagnetic waves in a pulse-echo mode to detect enemy aircrafts [3].

Since WWII, medical ultrasound has been a key enabler technology for many common medical diagnostic procedures such as mammography, laparoscopy, endoscopy, endorectal ultrasonography and vascular ultrasonography [4], [5]. Where each of these procedures will be briefly summarized as follows: (1) Mammography is the use of ultrasound to image the breast tissue for non-palpable breast lesions and malignancy; (2) Laparoscopy ultrasound is used to image pancreatic surgical procedures and to detect previously undiagnosed lesions or bile duct stones and stenosis; (3) Endoscopic ultrasound involves the visualization of the gastrointestinal tract by relatively high frequency (10-20MHz) transducers placed through an endoscope [6], [7]; (4) Endorectal ultrasound is useful in evaluating patients with benign and malignant rectal conditions as well as the prostate gland. Typical frequency ranges from 7-10 MHz with a rotating transducer fitted at the tip of the endo-catheter; (5) Vascular ultrasound is a diagnostic imaging technique commonly used to diagnose patients with arterial stenosis and thrombosis and is commonly referred to as intravascular ultrasound (IVUS). Another vascular related ultrasonic diagnostic is known as intra-cardio echocardiography (ICE) and is used to image the structural heart through the access of a catheter into the right atrium. These two vascular

related ultrasound methods will be the focus for the rest of the thesis in terms of ultrasound application and will be introduced with more detail in the upcoming sections.

In medical ultrasound, there are different modes of imaging: (a) A-mode (b) B-mode (c) C-mode and (d) M-mode. A-mode is a single transducer scan line through the body with echo amplitude plotted as a function of time or depth. B-mode, also known as 2D mode, is when a linear array of transducers simultaneously scans a plane and post image processed as a 2D sectional image. C-mode is a 2D image formed in a plane normal to B-mode. Finally, M-mode is when quick pulses are emitted in succession and A-mode or A-scan data are collected and beamformed into frames of images. Over time, these frames of images are compiled into a video or as hardware allows, real-time imaging. In 1949, Dr.

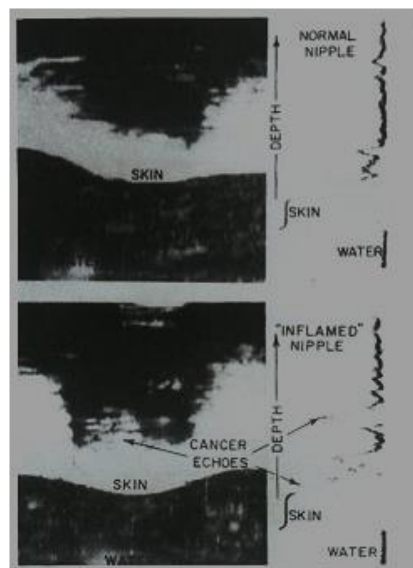


Figure 1.1 Diagnosis of a breast malignancy by B scan in 1953 by Dr. Wild and Reid [9].

John Wild performed the first medical ultrasound diagnostic of assessing the thickness of bowel tissue using amplitude (A) mode imaging [8]. In 1953, Dr. Wild and Reid captured

the first real-time image of a 7 mm cancer of the breast with brightness (B) mode imaging [9], shown in Figure 1.1.

The beginning of vascular and intravascular ultrasound started with I. Edler and C. H. Hertz [10] in 1953, who recorded the first M-mode echocardiograms of the heart using an industrial reflectoscope for flow detection seen in Figure 1.2.

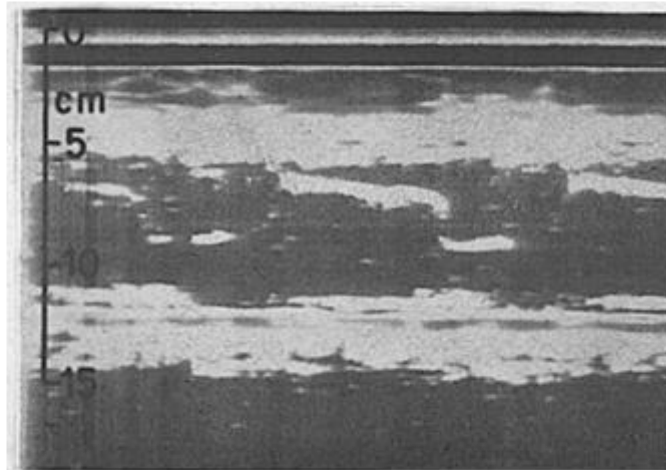


Figure 1.2 One of the earliest M-mode echocardiograms of the mitral valve, recorded by I. Edler and C. H. Hertz in December 1953. The sensitivity of the transducers used at that time allowed the recording of echoes from diseased valves only, and not from normal valves [134].

Later in 1956, T. Ciezynski developed the first single element transducer catheter to measure the canine heart chamber [11]. Just a decade later in 1962, N. Bom *et al.* [12] described a real-time intracardiac scanner using an electronically phased circular array of 32 elements at the tip of a 9 French (Fr) (Φ = 3 mm) catheter. These developments were discontinued at the time because of limitations of miniaturization of the transducer and prominent results from precordial image quality. Since the 1970s and 80s, ultrasound has become more popular in the field of cardiology, and surgeons in the US have embraced it

as a key diagnostic tool due to its minimally invasive capability, non-ionizing modality, portability and relative low costs compared to other diagnostic imaging tools such as computed tomography (CT) and magnetic resonance imaging (MRI) [4], [13], [14]. After the development of the first miniaturized single-transducer system in the late 1980s by Yock et al. [14] which enabled transducer placement within the coronary arteries, intravascular ultrasound has become a pivotal catheter-based imaging technology to provide guidance for percutaneous interventions and scientific insights into vascular biology in clinical settings.

1.1.2. Atherosclerosis and X-ray Angiography

Currently, heart diseases and vascular-related health problems are the number one killer in the US (1 in every 4 deaths), causing more deaths per year than cancer and car accidents [15]. In America, around 80 million people suffer from heart disease and there are around 5.7 million total heart failures every year, 385,000 of which lead to death [16], [17]. The American Heart Association (AHA) and the Center for Disease Control (CDC) have pronounced atherosclerosis, the buildup of plaque in arteries over time, the single largest contributor to modern society's heart diseases. Plaque is typically made up of fat, cholesterol, and calcium found in blood. This buildup slowly constricts the lumen (opening) of the artery and limits the flow of oxygen carrying red blood cells to the heart and other parts of the body depicted in Figure 1.3. This disease can occur in both peripheral

arteries that supply blood to parts of the body including the legs, arms, pelvis and kidneys for example. It can also occur at the coronary artery and have much more fatal effects.

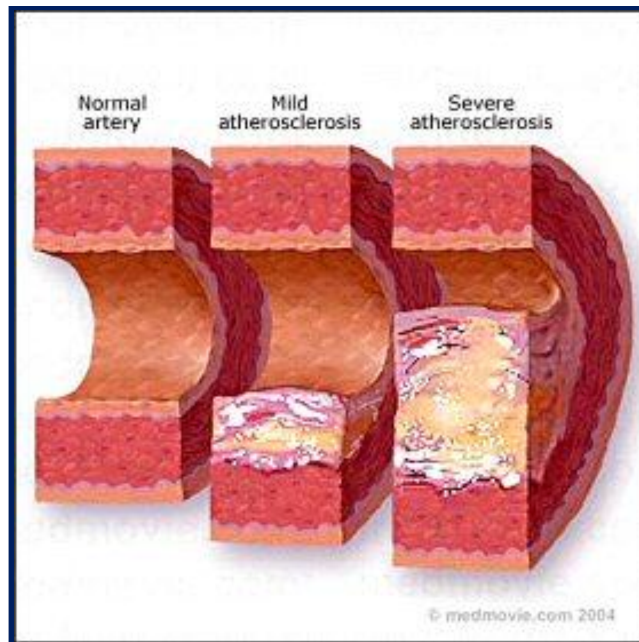


Figure 1.3 Cross section of a healthy artery, mild plaque buildup and severe plaque buildup from left to right. www.http://medmovie.com

Although intravascular ultrasound techniques has been identified as a minimally invasive procedure to diagnose plaque buildup and possible lesions inside the arteries, it is still today not the first diagnosis to be performed on a cardio-patient. A cardiologist will first examine the patient by X-ray angiography, utilizing radio-active tracers to identify the main locations of blockage and blood constriction shown in Figure 1.4. It is important to identify such regions of the artery in a patient because the plaque can harden and rupture causing potential blood clots and heart attacks to occur. Even without rupture, the patient will suffer from depleted oxygen levels to the heart, and as a result have high blood pressure, and chest pains (angina) with the prolonging blockages in the artery.

X-ray angiography is advantageous because it is quick, real-time imaging, simple to perform, non-invasive and shows blood flow information; however, it can have adverse health effects for the patients due to highly ionizing energy produced by X-ray exposure. Additionally, the 2D projected image of the artery lacks resolution in the image and cannot give information about the different layers of tissue and how much plaque exists in a particular section of the artery. It is often unclear by looking at an angiogram whether the blocked artery in question has what percentage of the lumen (arterial opening) blocked and the state of the plaque (its hardness and composition). Only in severe cases such as chronic total occlusions (CTOs), one will see complete blockage and stop of blood flow on the

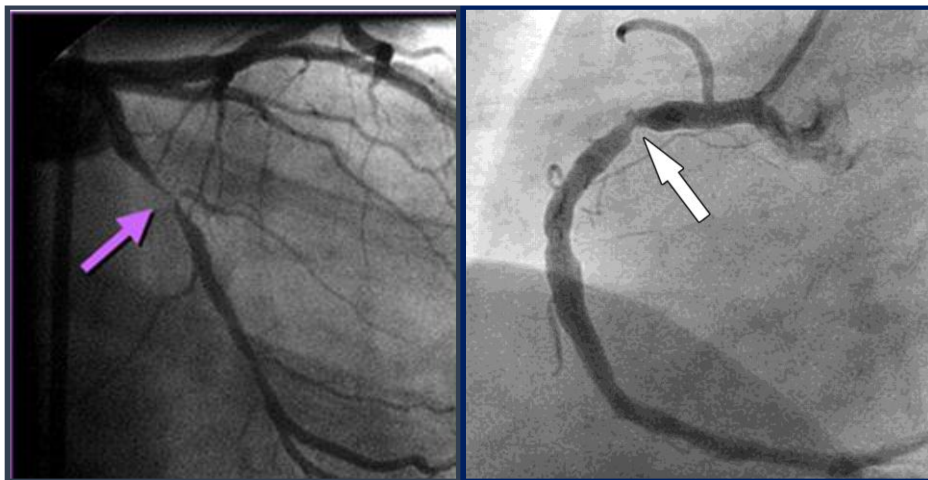


Figure 1.4 Two typical x-ray angiography 2D projections, showing sites of possible plaque buildup (atherosclerosis) due to relative narrowing of the artery and limited blood flow [135].

other side of the blockage. Thus, to aid cardiologists in better understanding and diagnosing the artery and plaque formation as well as the state of health of the arterial wall tissue, IVUS is needed.

1.1.3. Intravascular Ultrasound (IVUS)

To address the shortcomings of angiograms, IVUS is implemented as a minimally invasive procedure to further investigate the region of blockage inside arteries. Intravascular ultrasound typically involves insertion of a 3 French (Φ = 1 mm) catheter over a guidewire through the femoral artery to the place of blockage while guided by x-ray angiography. At the tip of the catheter is a piezoelectric transducer or an array of transducers that can produce a 2D cross section of the arterial walls and plaque if present. IVUS uses sound waves in the range of 20-40MHz center frequency (fc), to create 2D sectional images of the artery wall surface and penetrate up to 0.5-1cm into tissue [18], [19]. High-resolution lesion evaluation and precise stent placement guidance, of increasing importance for intervention cardiology over the past two decades [20]–[22], are also key advantages IVUS possesses over angiography. Currently, many studies and clinical trials have shown the successful use of IVUS and drug-eluting stents (DES) as a key intervention procedure for vascularization and active treatment of low to medium severity atherosclerosis with reduced stent-induced thrombosis and diminished need to re-vascularize due to repeat plaque buildup [13]. Balloon angioplasty is the inflation of a balloon like device at the tip of the IVUS catheter to expand the constricted lumen and push the plaque outwards. A stent or metal/polymer mesh is typically on the outside of the inflating balloon and situates inside the collapsing artery to permanently hold the lumen open, shown in Figure 1.5. To successfully perform these procedures, it is critical for IVUS technology to exhibit strength in image accuracy, real-time imaging capability, and high resolution imaging. Miniaturization of transducer design is key to delivering small and

compact profile catheters, around 3-Fr (Φ = 1 mm) in size, to access the tight confines of vital coronary arteries.

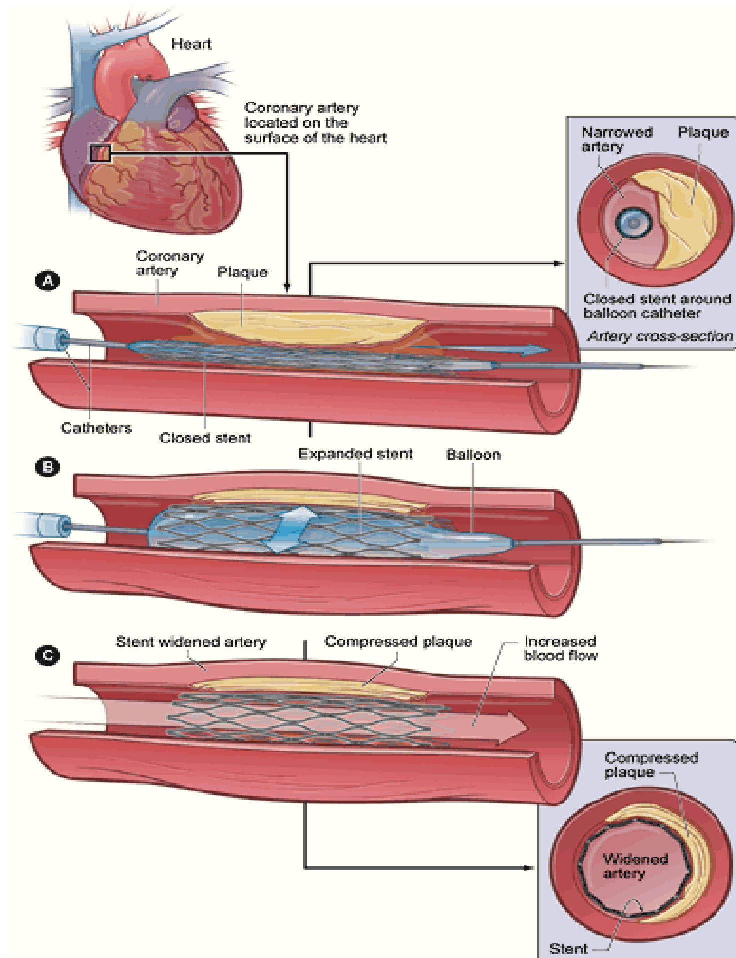


Figure 1.5 (a) Balloon and stent guided over the plaque region, (b) balloon inflates and expands the stent, (c) balloon deflates and catheter is retracted while the stent is permanently holding up the collapsing artery pushing the plaque outwards [136].

For more severe cases of atherosclerosis known as chronic total occlusions (CTOs) where 99-100% of the artery in question is blocked with plaque and has no blood flow, traditional 2D side-looking IVUS imaging catheters are not suitable for imaging the plaque-filled volume (Figure 1.6). CTOs represent the most difficult cases for interventional cardiologist and they are frequently encountered during endovascular interventions, with a reported presence in 40% of patients with symptomatic peripheral

arterial disease [23]. Revascularization of CTOs is usually hindered by failure to cross the lesion due to a variety of factors, such as the inability to position a guidewire in the true lumen. Attempts to revascularize heavily calcified CTOs with tradition catheters, guidewires and balloon technologies fail in at least 20% of cases [24], [25].

The goal of this research is to provide the interventional cardiologists with an emerging technology: forward- looking intravascular ultrasound (FL-IVUS) catheters

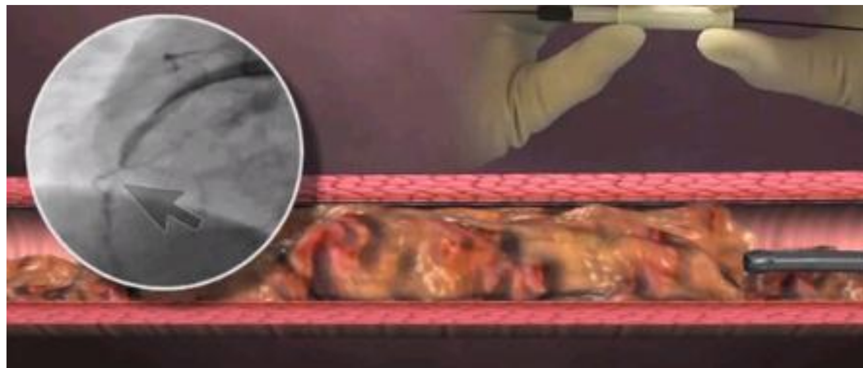


Figure 1.6 Chronic total occlusion, where > 99% of the lumen is blocked by plaque that is over 30 days [137].

utilizing a micro-electrical mechanical systems (MEMS) based transducer design known as the capacitive micro-machined ultrasonic transducer (CMUT). Such a catheter can enable the use of real-time 3D forward imaging of CTOs during diagnostics, as well as aid guidewire placement during crossings of high stenosis (blockage). The FL-IVUS transducer can also help in stent positioning after successful crossing of the stenosis and before balloon inflation. The 3D volumetric imaging is achieved by a 2D array of CMUT elements on the surface of a silicon substrate.

1.1.4. Intracardio-echocardiography (ICE)

Another application for such a 2D CMUT array on a catheter based delivery system is intracardiac-echocardiography (ICE), where diagnostic imaging is required for a variety of procedures, including: transaortic valve implant (TAVI) (Figure 1.7), left atrial appendage closure (LAA), percutaneous mitral valve replacement (PMVR) and atrial fibrillation ablation. Typically, ICE transducer design requirements call for a 5-15MHz center frequency for better depth penetration inside the structural heart (up to ~ 15cm) compared to IVUS (~1-2 cm) [26], [27]. Typical ICE catheters are 9-Fr (Φ = 3 mm) in size and can enter the heart through the right atrium or right ventricle via a femoral approach. A typical ICE image is shown in Figure 1.8.

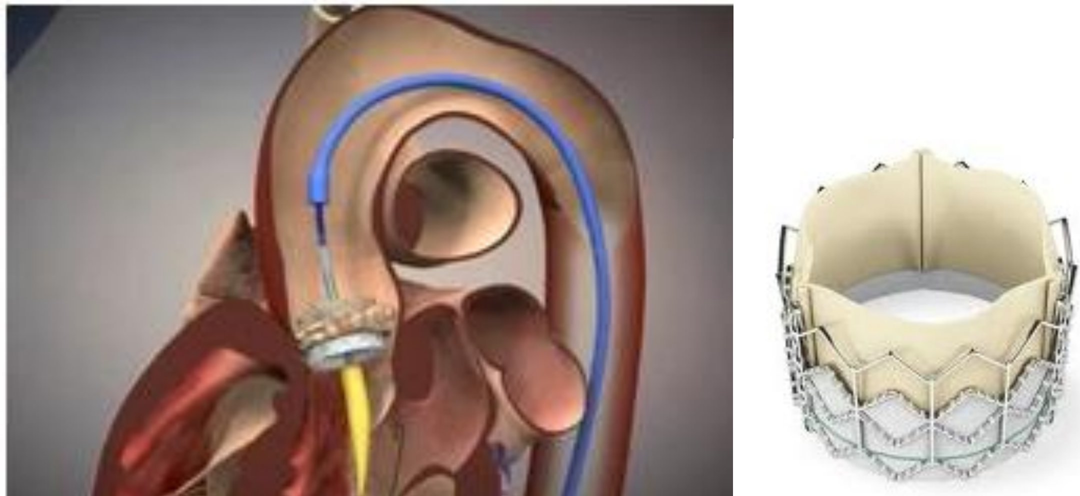


Figure 1.7 TAVI procedure shown placing an artificial aortic valve through the insertion of a catheter inserted near the groin area (left) and an artificial heart valve based on an expandable stent mesh (right) [138].

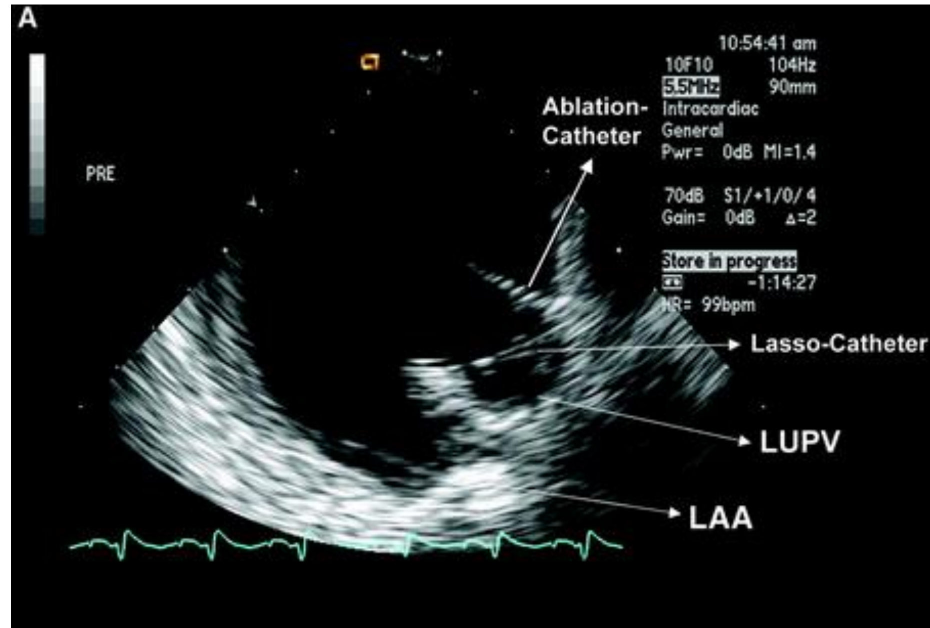


Figure 1.8 An example of a 2D ICE image showing circular mapping catheter positioned at the ostium of the left upper pulmonary vein (LUPV). LAA indicates left atrial appendage [139].

Positions of the veins, ridges, and septa in the heart are examples of information of critical use to a cardiologist that can be obtained easily by ICE imaging. The ICE procedure is minimally invasive and minimally discomforting to the patient. General anesthesia is not needed for the patient as it would be in fluoroscopy imaging, allowing for the doctor to communicate with the patient during the procedure [28], [29]. Although many advantages have been addressed by ICE, there are still several limitations of ICE that exist. First, the current 9-Fr catheter shaft size is mostly occupied by the transducer technology, leaving little to no space for additional catheter features such as guidewires and therapeutic devices. Second, the current 2D phased array catheters are expensive due to the complexity of integrating the transducer with front-end integrated circuits (IC). Third, the phased ICE arrays can only provide monoplane image sections which can be partly overcome by the steerability of the catheter. This can cause the operator to see nonconventional anatomical

views and disorient the surgeon during surgery, possibly causing prolonged diagnosis or misdiagnosis. The underlying CMUT technology described in this thesis hopes to address and improve future ICE imaging as well.

1.1.5. Current Commercially Available IVUS and ICE Transducer and Catheter Technology

Currently, all commercial IVUS and ICE catheters use piezoelectric transducers for their image sensors. There are essentially 2 types of piezoelectric imaging catheters: (1) single element rotating shaft (1900 rpm) and (2) multi-element phased/solid state arrays. Both of these types of transducers are side-looking only and can only produce a 2D sectional image of the arterial wall. The single element transducer creates the 2D sectional image by pulse-echoing and rotating 360^0 around the central shaft of the catheter (Figure 1.9). Its advantages are (a) little to no "dead zones" (Figure 1.10) in the image, (b) the ability to achieve high resolution with >45MHz single element transducer and (c) relatively simple electronic integration and post processing. Its disadvantages include (a) motion artifacts due to non-uniform transducer spin (blurring in the image) and (b) difficulty in mechanical incorporation of the guidewire and other intervention technologies due to the

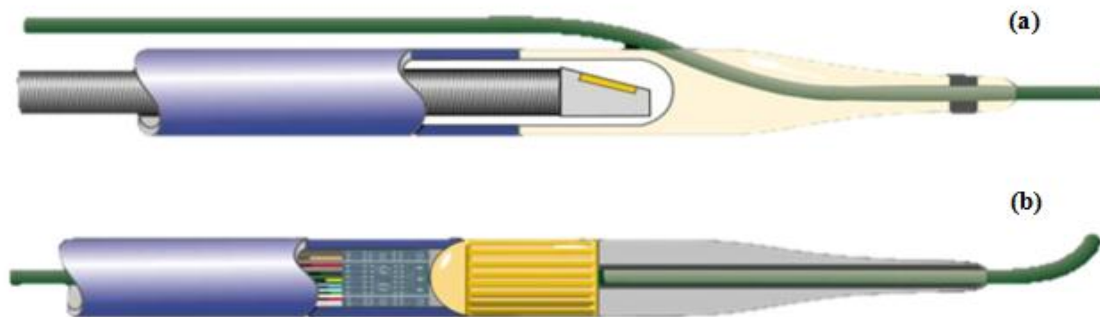


Figure 1.9 (a) Mechanical single element catheter e.g. 40 MHz Atlantis® SR Pro Catheter(Boston Scientific Corp.), (b) Phased/Solid State Array e.g. 20 MHz Eagle Eye Gold® (Volcano Corp.) [137].

centrally located spinning shaft. For phased array catheters such as Volcano Corp.'s Eagle Eye Gold® , 64 piezoelectric elements surrounds the circumference of the catheter and 2D sectional images are captured by electronically rotating 13 of the elements that make up the aperture. Its advantages are (a) no mechanical moving parts in the catheter (b) better image resolution due to a larger aperture size (c) ability to do dynamic focusing, and (d) more real-estate for the guidewire and other intervention tools in the center of the catheter. Primary disadvantages of phased arrays include (a) the complexity in transducer array fabrication and integration with front-end IC due to multiplexing and dynamic focusing and (b) the increased complexity in post processing.

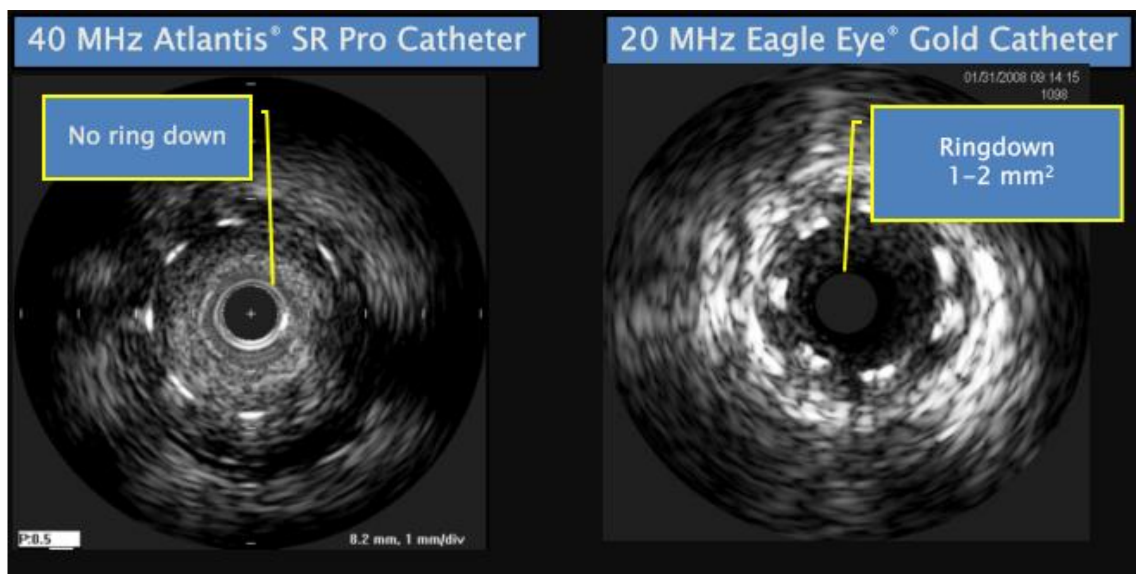


Figure 1.10 Image difference between the 2 catheters of stent apposition. With the no ring down single element transducer (left) and 1-2 mm ring down phased array (right) [137].

Future directions in IVUS include increasing resolution, forward-looking IVUS (FL-IVUS) and IVUS on a guidewire (Φ = 0.4 mm). Other emerging technology, such as optical coherence tomography (OCT), are also competing with traditional IVUS technologies. While OCT can produce very high resolution images, it operates on optical

principles instead of ultrasound and cannot penetrate deep past vessel walls and the blood needs to be flushed with saline solution [30].

As mentioned previously, no 3D FL-IVUS catheter currently exists on the commercial market, and such a catheter would provide great advantages in diagnosing CTOs, guiding CTO crossings, and preventing re-stenosis in highly clogged arteries through guiding drug-eluting stent (DES) placements. Volcano Corp. is currently developing a 2D FL-IVUS catheter based on a single piezoelectric transducer mounted at an angle on the tip of a rotating shaft. This allows the imaging unit to sweep a forward looking 2D-conical slice [31]–[33]. The design is complex, bulky and inflexible and it is not suitable for coronary and cerebral arteries and stent placements (Volcano Corp. 2013). Figure 1.11 shows the 2D FL-IVUS concept.

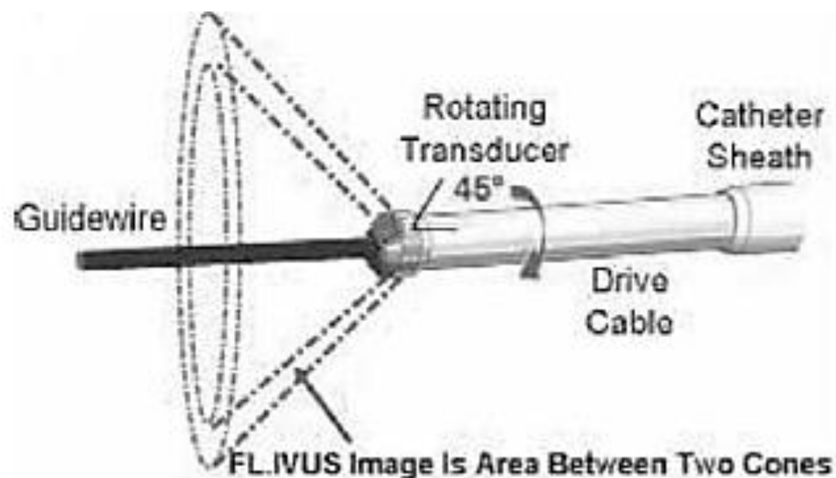


Figure 1.11 2D FL-IVUS catheter under development from Volcano Corporation [32].

An example of a commercialized ICE catheter and imaging system is AcuNav™ produced by Acuson Inc. (now part of Siemen's Medical Engineering Group after acquisition in year 2000). This particular ICE catheter is 10-Fr with 64 element used in a phased-array configuration. It is introduced into the femoral vein via an 11-Fr sheath with an additional decapolar Lasso catheter (Biosense) [34]. Both the AcuNav catheter and the imaging system from Acuson are shown in Figure 1.12.

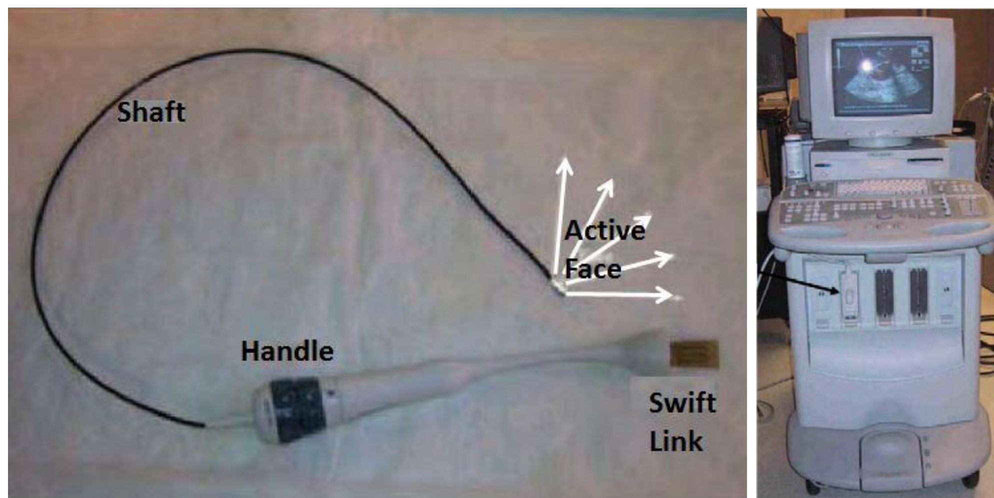


Figure 1.12 (left) AcuNav diagnostic ultrasound catheter with its steerable tip, (right) Acuson (Sequoia) echocardiograph with Swiftlink catheter connector (arrow) [34].

Just like the current state of IVUS technology, there are currently no 3D volumetric FL-ICE arrays available on the commercial market. However; this has been a hot research topic in the past decade and pursued by many research groups. For example, Nikoozadeh *et al.* [35], [36] have developed a 12-Fr (Φ = 4 mm) ICE catheter based on CMUT technology, with 64 CMUT elements configured into a ring shape and facing in the forward (perpendicular to circumferential) direction of the catheter. This overall packaged design integrates the CMUT based transducer silicon chip with its corresponding integrated circuitry chips (IC) via a flexible interconnect (Figure 1.13). This design has 8 separate IC

chips responsible for amplification and multiplexing the different channels, 244 solder interconnects and a total of 100 cables were necessary for all input/output connections. The choice of having separate chips for their CMUT sensors and IC is due to limitations in fabrication compatibility of their CMUT process with the IC. It will be described later in Chapter 3 the different strategies one may take in terms of CMUT and IC integration which can affect the overall design of the front-end sensor system for both IVUS and ICE. The main focus of the thesis is for the IVUS system; however, optimized material selection and design approaches that will be described in the subsequent chapters can also be translated to when designing for an ICE catheter system.

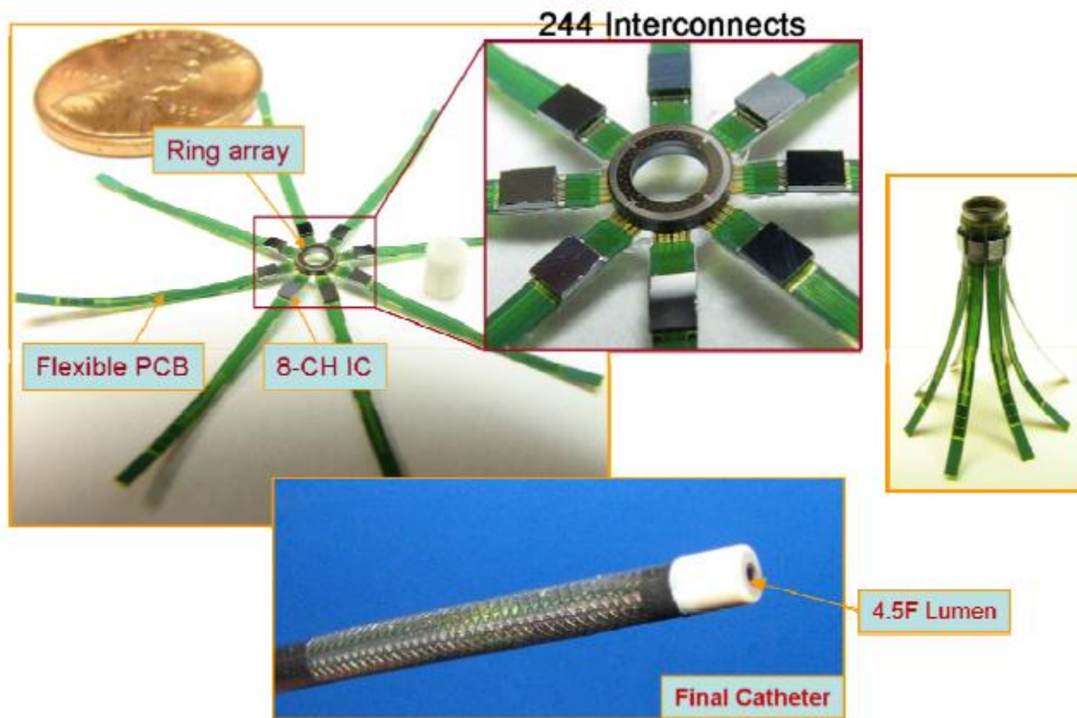


Figure 1.13 Ring shaped 2D array with 64 CMUT elements for a 12-Fr FL-ICE catheter with 3D volumetric imaging capabilities [36], [84].

1.1.6. Proposed Solution: CMUT-on-CMOS integration with 3D Forward-Looking and Side-Looking capability

The research described in this thesis differentiates from previous approaches by utilizing CMUT-on-CMOS transducer and IC integration technology to enable 3D volumetric FL-IVUS. This imaging unit is completely solid state and can generate 3D images by utilizing 2D arrays of CMUT transducers fabricated in a ring shaped aperture with separate rings for transmit (Tx) and receive (Rx) capabilities, shown in Figure 1.14. Having the ability to view forward and sideward at the same time is a highly useful feature to have for IVUS imaging. It can enable the cardiologist to have the possibility of switching between a volumetric forward looking view and a 2D sectional view of the arterial walls perpendicular to the transducer surface without the need to change positions or perform the pull-back method which can be timely and inconvenient. Such ideas have been previously been proposed [37]; however, at the cost of extra complexity in the catheter by adding additional annular CMUT arrays on each of the 4 sides of the catheter tube and additional

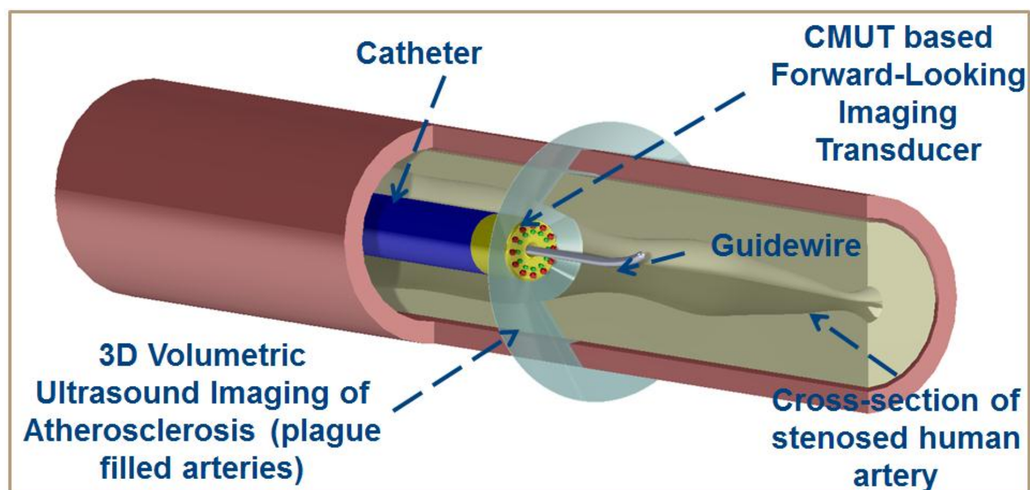


Figure 1.14 3D volumetric FL-IVUS catheter with CMUT-on-CMOS dual ring array technology (proposed research design)

cables and interconnects for power and outputs from the 4 separate side-looking annular CMUT-on-CMOS arrays. In theory these additional side-looking annular arrays can provide high resolution sidewall imaging, but the complexity of additional transducers, cables and interconnect can outweigh that benefit. Extra cables means the catheter will be ultimately stiffer and thicker in diameter and more interconnects can diminish manufacturing reliability. The ability to view close to 90^0 of the azimuth angle will be investigated in Chapters 4 & 5.

1.2. Ultrasound Principle and Transducer Technology

1.2.1. Principles of Ultrasound Imaging

Ultrasound is typically defined as acoustic waves with center frequencies above 20 kHz, which is above the human audible range. A sound/pressure source such as a transducer vibrates back and forth when actuated and will couple to the surrounding medium. Transverse waves or perpendicular waves can be carried by a solid medium while only longitudinal waves exists in liquid mediums such as blood, water or oil. When the ultrasonic waves radiate away from the transducer surface, a pressure front is developed and will travel at the speed of sound in that medium until it reaches the boundary of another medium with different physical properties such as density and speed of sound. A reflection of the wave will be generated at boundaries of mediums due to the difference in acoustical impedance $Z = \rho_0 \cdot C$ (MRayls) and generally the larger the impedance mismatch between two mediums the larger the reflected wave amplitude. Medical ultrasound depends on this physical phenomenon to differentiate the different layers of anatomical features such as blood to arterial tissue wall and tissue wall to the under laying plaque buildup in IVUS. Anatomically significant and different tissue boundaries may be hard to distinguish if their impedance properties are very similar.

As pressure waves travel through the medium, attenuation causes the wave amplitude to decrease due to physical losses and absorption of energy from the medium. Attenuation is described most commonly by a constant α (dB/cm) and is frequency-dependent (exponential law). High frequencies correspond to larger values of the attenuation constant which means IVUS (20-40MHz) will suffer in penetration depth compared to ICE (5-15MHz). Poor reflection off similar impedance mediums and attenuation in the bulk fluid accounts for the biggest losses in reflected pressure signal amplitude. A schematic of the main sources that contribute to the loss of acoustical wave amplitude in a pulse-echo mode of any transducer is described in Figure 1.15.

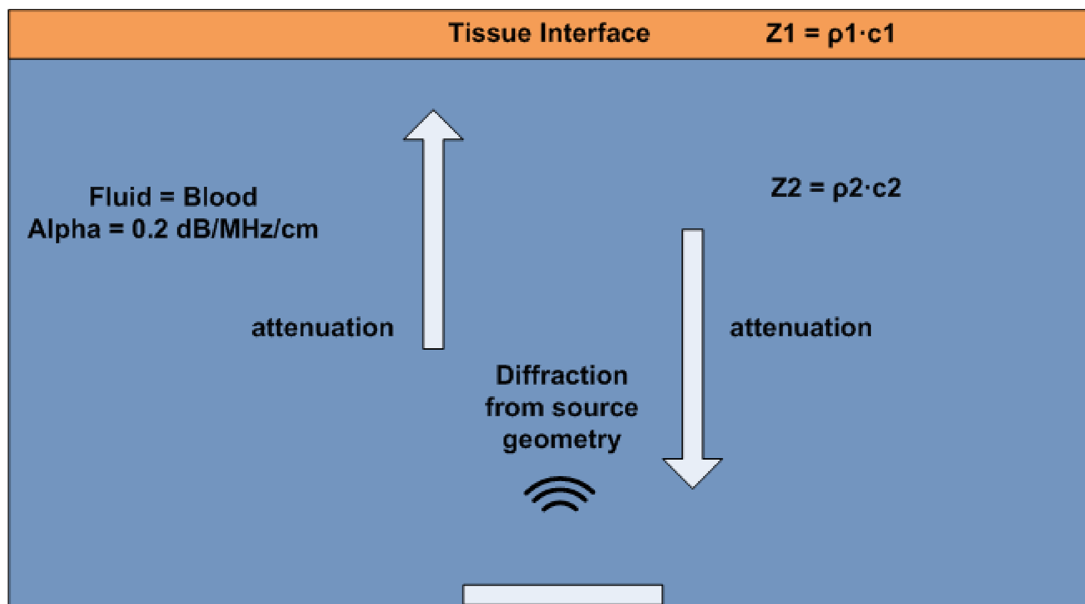


Figure 1.15 Schematic of wave travelling from the emitting transducer source and the main physical contributors to decreased acoustical amplitude on the receive side.

Typical attenuation constant values (α) for materials inside the human body are tabulated in Table 1.1[38] below.

Table 1.1 A Table of Attenuation Constants for Various Bio-materials Inside the Human Body

Material	$\alpha(\mathrm{dB}/(\mathrm{MHz}\cdot\mathrm{cm}))$
Air	1.64 (20°C)[6]
Blood	0.2
Bone, cortical	6.9
Bone, trabecular	9.94
Brain	0.6
Breast	0.75
Cardiac	0.52
Connective tissue	1.57
Dentin	80
Enamel	120
Fat	0.48
Liver	0.5
Marrow	0.5
Muscle	1.09
Tendon	4.7
Soft tissue (average)	0.54
Water	0.0022

As an example of attenuation in ultrasound imaging: if a wave with $f_c = 20$ MHz traveled to image at a distance of Z = 1 cm from the center of the transducer surface, and assuming that a perfect reflector (reflection coefficient R = 1) exists at that location, then for a pulse-echo two way travel (Z = 2 cm), one would expect a -8 dB change in the acoustical amplitude by the time the transducer receives this signal. This corresponds to ~2.5 times decrease in amplitude. At $f_c = 40$ MHz this effect is doubled. Also, since most transducers produce relatively broadband pressure signals, this means that the higher end of the frequency bands will attenuate more as a function of distance travelled in a medium thus affecting the overall bandwidth as a function of travelling or imaging distance. The

attenuation as a function of frequency and a total travel distance of Z = 2 cm is shown for 3 example materials in Figure 1.16. As mentioned previously, it is usually desirable to image as deep as possible into the tissue or muscle walls of the underlying anatomical feature. For IVUS and imaging of the arterial walls, 1-2 cm depth is the desirable range at f_c = 20 MHz and for ICE imaging 10-15 cm is desirable at f_c = 10 MHz.

Although it can be seen from the attenuation constant that lower frequencies give

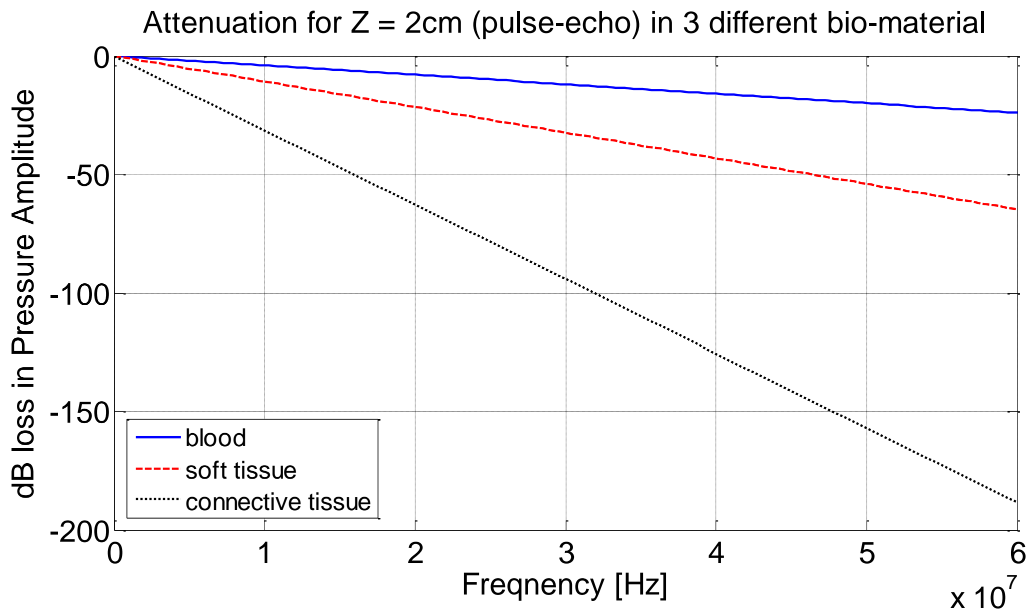


Figure 1.16 Attenuation as a function of frequency in 3 different bio-materials

better penetration and less prone to attenuation related loss in amplitude; however, one needs to also consider another important design parameter in medical ultrasound: resolution. The higher the spatial resolution, the easier it is to distinguish between two close objects. In IVUS imaging, resolution is typically defined in two directions: (1) axial and (2) lateral (Figure 1.17). Both resolutions are defined by Eqn. 1.1 and Eqn. 1.2 where λ is the wavelength, BW is the -6dB bandwidth, fc is the center frequency and F# is defined by the focal depth from the center of aperture and D is the diameter or length of the aperture.

In both the axial and lateral resolution equations, smaller the wavelength (or higher center frequency) the better the resolution in terms of smallest resolvable distance. Naturally, penetration depth of the ultrasound image and the resolution of the ultrasound is a trade-off when it comes to transducer design, and one must carefully design a transducer system to meet minimum expected clinical requirements based on the application at hand.

$$R_{axial} = \frac{c}{2 \cdot BW} = \frac{\lambda \cdot f_c}{2 \cdot BW} \qquad \text{Eqn. 1.1}$$

$$R_{lateral} = \lambda \cdot F\# = \frac{F \cdot \lambda}{D} \qquad \text{Eqn. 1.2}$$

In terms of the current commercially available IVUS technology, we can compare briefly each of their capabilities in-terms of resolution. Optical coherence tomography (OCT) is an emerging optical imaging method that uses light in the infra-red regime and it is also shown in Figure 1.17 for relative comparison in terms of its resolution performance for IVUS needs.

Resolution	Phased Array IVUS	Rotational IVUS	OCT
Axial (depth)	150 µm	75 µm	15-20 µm
Lateral	200 - 500 µm	100 - 200 µm	20 - 40 µm

Figure 1.17 Comparison of current IVUS technology (passed and rotational) and OCT systems for their axial and lateral resolution [140].

It can be seen that rotational IVUS or single element piezoelectric based transducers have better axial and lateral resolutions than the multi phased arrays. This is mainly due to two reasons: (1) the single element transducer does not suffer from acoustical cross-talk effects that can lower the bandwidth (BW) of the propagating waves, (2) the aperture size (D) of the single element transducer is larger than the effective moving aperture in the phased array. Although superior in resolution, the single element rotational transducers are complicated mechanically to manufacture with prone image distortions due to off-centering of rotation of the drive shaft during operation (also known as Non-Uniform Rotation Distortion (NURD), Figure 1.18). This type of imaging defect severely limits the user's ability to make any type of conclusive diagnoses. Lastly, guidewires are hard to incorporate into the rotational IVUS catheter and usually leaves "blind spots" where the guidewire is partially blocking the imaging space [39]. It can also be clearly seen from Figure 1.17 that OCT has the best resolution out of the three comparisons; however, due to absorption of light in matter, the penetration depth of OCT is poor.

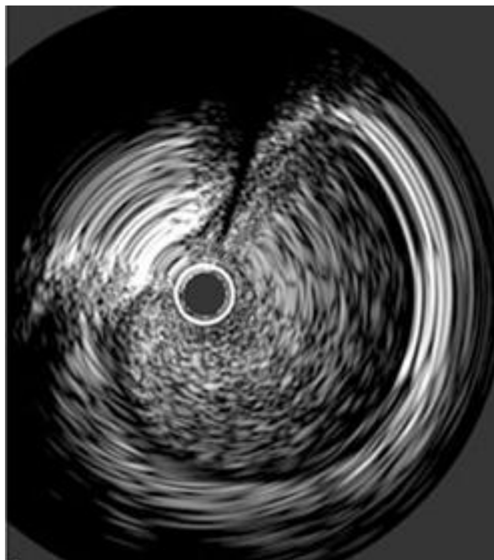


Figure 1.18 An example of NURD image distortion from a single element rotating IVUS catheter [39].

Lastly, the form of the transducer array also dictates the type of image one can obtain. A single transducer if pulse-echoed and rotated on a shaft can produce B mode imaging. A linear array of transducers can perform B mode imaging by beamforming and delaying the transmit pulses. This 1D array can only produce 2D images due to the ability to only acoustically steer in one plane, whereas the proposed CMUT array is arranged in a 2D circular aperture pattern to allow the capture of a 3D volumetric image. A 2D array can be in any form as long as separate elements of transducers are positioned in different X-Y Cartesian coordinates. A circular aperture is chosen for the CMUT arrays for IVUS and ICE due to the shape of catheters being cylindrical, and pushing the diameter to the outer edge of the design space to maximize the aperture size.

1.2.2. Piezoelectric Transducer Vs. CMUT Vs. PMUT

Currently, the most commonly used transducer technology in commercial IVUS and ICE catheters are bulk piezo-electric transducers. However, due to many limitations in terms of acoustical performance, miniaturization and IC integration, two MEMS based emerging technology are explored as the future alternative in these applications. Both capacitive and piezoelectric micro-machined ultrasonic transducers (CMUTs and PMUTs) are fabricated based on micro-machining techniques such as photolithographic patterning which enables manufacturing of mechanical structures of micron to sub-micron sizes in a batch manner on silicon substrates. The three competing technologies are shown in Figure 1.19.

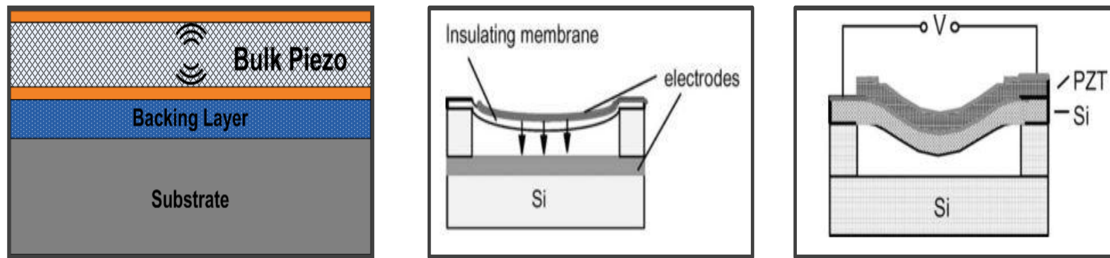


Figure 1.19 From left to right structures of each type of transducer that maybe suitable for IVUS applications: (left) Bulk Piezo-electric transducer, (middle) CMUT, (right) PMUT [42].

Piezoelectrics have many advantages including, ease of manufacturing in mm sizes, ability to stack for higher pressure output, withstand 500-1000V/mm before depolarization, and uniformity in acoustical behavior in terms of pressure output, center frequency and bandwidth [40]. Piezoelectric elements are generally diced into half wavelength (λ) size to avoid grating lobes which causes image artifacts [3]. With IVUS applications pushing towards 40MHz, it is difficult and expensive to mechanically dice below 20 μm pitch and thin the piezo ceramic past <10 μm thick (f_c dependent). Pitch reduction can be reduced further using dry etching techniques such as reactive ion etching (RIE) [40]. Recent thickness improvements have been shown through development of thin film piezoelectric materials via spin coating sol-gel method, aerosol deposition, hydrothermal, and RF sputtering [41]. These novel fabrication techniques have allowed the continual scale down of piezoelectric elements and the development of PMUTs (piezoelectric micromachined ultrasonic transducers) for up to 100MHz applications [42], [43].

However, traditional bulk piezoeletrics suffer from impedance mismatch [40] and requires front and back matching layers for better transmission of acoustic waves into the surrounding medium. Obtaining the ideal mechanical matching parameters can be difficult

in practice, as transmission line theory predicts 100% transmission occurs with a thickness of $\lambda_m/4$ and a matching layer impedance (Z_m) as the geometric mean of the transducer (Z_p) and medium impedance (Z_m) ($Z_m = \sqrt{Z_p \cdot Z_l}$) [44]. As one can see that as frequencies surpass 10-20MHz, it gets incredibly difficult to manufacture uniform matching layers below 20µm with the ideal matching acoustical impedance (Z_m). This impedance mismatch is not an issue in CMUT devices because acoustical waves are not generated inside a bulk material but rather via a continuity of motion of the micro membrane on the fluid, thus eliminating the need for matching layers. Piezoelectric transducers are often narrow band through transducer geometries and poor matching layer performance while CMUTs are easily designed for broadband pulses by simply modifying geometry parameters and usage of mass loading [45], [46].

Lastly, the coupling coefficient (K_T) of a CMUT transducer can easily be maximized as it is operated closer to collapse voltage [47]. But for bulk piezoelectric transducer, the coupling coefficient or efficiency of the transducer is limited to fundamental constants of the material [48], [49]. Typically k_T^2 constant is less than 50% in most bulk piezoelectric materials. PMUTs with a piezoelectric heteromorphous membrane have been quoted to have a K_T^2 of 18% [42], [43] if it is assumed that $k^2 = k_P^2/2$ with k_p = 60% (transverse coupling coefficient) typically for bulk PZT. With phase changes in PZT and as a function of the dielectric constant (ε_r), k_p can potentially increase to 70% at very high dielectric constant end of the spectrum [50]. In contrast, CMUTs can reach close to K_T^2 = 100% near collapse and can be calculated via either a capacitance based definition or mechanical vs. electrical stored energy based definition [47], [51].

In summary, the key comparisons made between the 3 transducer technologies are shown in Table 1.2. CMUTs are a good candidate for IVUS and ICE applications where physical design space is very limited, signal-to-noise ratio matters and easy front-end IC integration can enable fully populated, fine pitched 2D arrays at fc = 20-40 MHz. Fabrication techniques of CMUTs and front-end IC integration methods will be furthered discussed in Chapter 2, and the approach that this thesis describes will be discussed and compared to over previous methods in literature. Chapter 3 will describe the improved efficiency in both transmit and receive to further improve SNR in IVUS and ICE imaging through the use of high-k dielectrics as well as improvements in terms of dielectric reliability. Chapter 4 describes the integration of CMUT and CMOS technology for monolithic single chip implementation with the added performance increase with high-k dielectric insulation. Chapters 5 will address the possible ability in performing side-imaging with evanescent surface acoustic waves in conjuncture with 3D forward looking capability. This dual frequency/modality imaging on a single chip will have ~20MHz

Table 1.2 Table Summarizing the Main Difference Between the Three Transducer Technologies

Comparison Parameters	Bulk Piezoelectric	CMUT	PMUT
Impedance mismatch with fluid	Yes	No	No
Front-side matching layer required	Yes	No	No
Bandwidth	Low	High	Low
Coupling Coefficient (K_T^2)	Material limited, k^2 ~50%	DC Voltage limited, k^2 ~ 60-100% near collapse voltage	Material & bimorph/passive membrane limited, k^2 ~ 20%
Fabrication Techniques	Mechanical dicing or RIE	Micro-machined, Wafer bonding	Micro-machined (surface and bulk)
Front End IC Integration	Difficult	Easy	Difficult

forward looking and ~40MHz side looking capability. Chapter 6 will describe the methodology in designing, fabricating and testing a dual frequency IVUS array capable of volumetric imaging at f_c ~20MHz and ~40MHz simultaneously.

CHAPTER 2. CAPACITIVE MICRO-MACHINED ULTRASONIC TRANSDUCERS

Before discussion begins on how to improve the current CMUT technology, I will first begin by describing the basic operating principals as well as the classic equivalent circuit modelling. It is important for one to understand the lumped model or equivalent circuit analysis of a CMUT as it can tell us how various key physical CMUT parameters such as the geometry and size of a membrane can change the figures of merit of interest such as collapse voltage ($V_{collapse}$) and coupling coefficient (K_T).

2.1. Basic Operation Principles

CMUTs are flexible membrane structures made on the micro scale via micromachining techniques on silicon substrates. Typically a DC+AC voltage source is applied to top and bottom electrodes to generate electrostatic forces and actuate the membrane during transmit mode. In receive mode, only a DC voltage is applied to the electrodes pulling the membrane close for higher sensitivity and detect smaller changes in capacitance. When the membrane is actuated, it will couple to the surrounding fluid sending out a pressure wave. When the pressure wave reflects from a nearby object and travel back to the receive elements of the CMUT, a change in capacitance is recorded via a current amplifier. The general structure of a CMUT consists of a bottom electrode, a vacuum gap, a dielectric isolation, a top electrode and finally the membrane structural material (Figure 2.1). The first capacitive based ultrasonic transducers were theorized in the early 1900s by Langevin [52] with large air gaps and a desired application for the condenser microphone. Early micro-machined transducers were used as pressure sensors [53] and small condenser microphones [54]. Some of the first surface micro-machined

CMUTs were from Stanford University with first applications as air coupled transducers [55], [56]. Other groups followed in the research and development of CMUTs in the following 2 decades with applications ranging from medical ultrasound, air and liquid immersion pressure transducers, microphones and non-destructive testing (NDT) and most recent work on tunable acoustic meta-material using linear CMUT arrays [57].

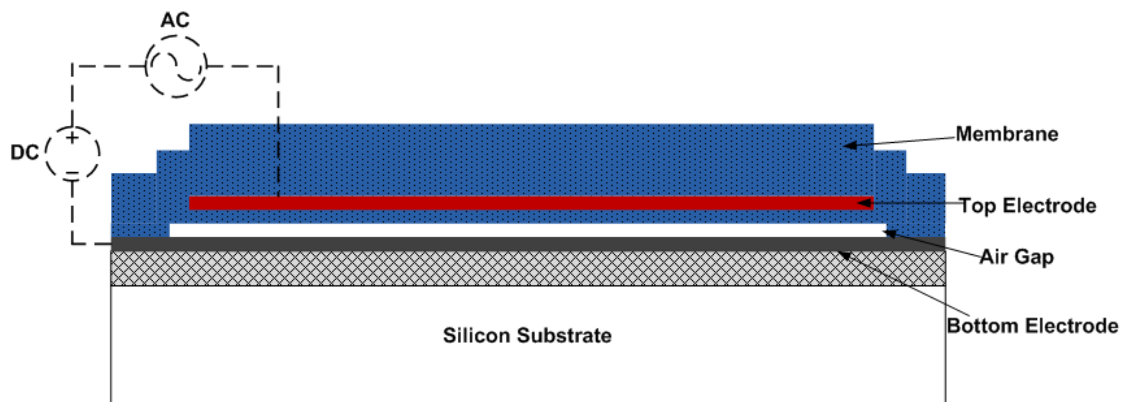


Figure 2.1 Schematic of generic CMUT structure

2.2. Parallel Plate Modelling and Device Physics

2.2.1 Static Operation

In order to understand the more complicated CMUT operation, it is useful to first implement a simplified analytical model. The simplest representation of a CMUT membrane is to think of it as a 1D mass-spring-dashpot system, with a parallel plate actuator attached to the spring and dashpot (Figure 2.2). This model is accurate to the first order. The CMUT is a complaint membrane and has mass and stiffness that can be in static equilibrium after deflection when an electrostatic force is generated between the parallel plates due to an electrical potential difference across the parallel plates.

If we consider the membrane under a quasi-static state, we can neglect the dashpot term since the membrane velocity is zero. Then a force balance between the mechanical (F_s) and electrical force (F_{es}) can be written as:

$$F_{es} = F_s \qquad \text{Eqn. 2.1}$$

For initial ideal discussion of the parallel plate model, the functional dielectric isolation layer thickness 't_d' is assumed to be zero at first. The electrostatic force can be derived from taking the derivative of the energy equation with respect to "x" the distance between 2 electrodes:

$$W = \frac{1}{2}CV^2 = \frac{1}{2}\frac{\varepsilon_0 A}{(x)}V^2 \qquad \text{Eqn. 2.2}$$

$$F_{es} = -\frac{\varepsilon_0 A V^2}{2x^2} \qquad \text{Eqn. 2.3}$$

Without any dielectric isolation and displacement of the top electrode, "x" is the vacuum gap "g" between the top and bottom electrodes of the parallel plate initially when the membrane has not yet displaced.

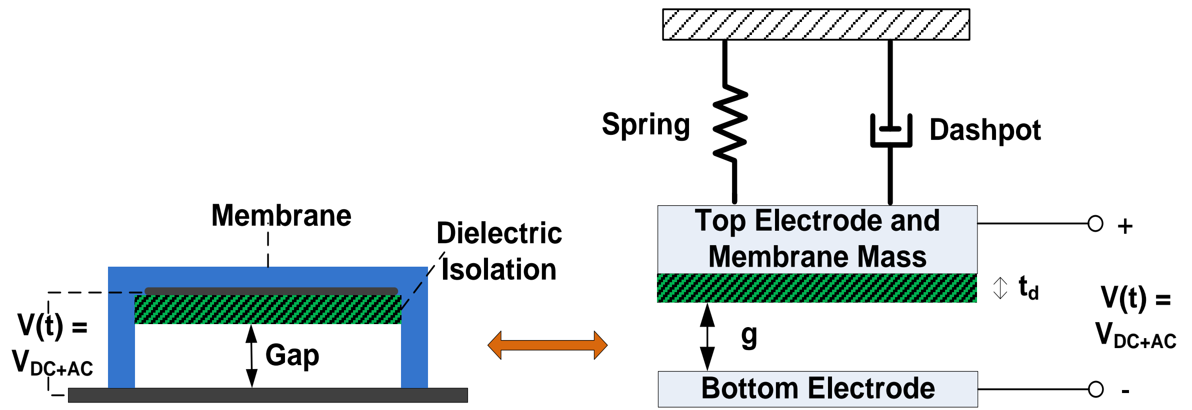


Figure 2.2 Schematic of CMUT structure (left) with mass-spring-damper representation (right)

In Eqn. 2.3: $\varepsilon_0 = 8.854 \times 10^{-12}$ F/m is the permittivity of free space, "V" is the applied DC voltage and "x" is the instantaneous vacuum gap in consideration (no dielectric isolation). From this relationship, one can see that the electrostatic force is proportional to the voltage applied squared and inversely proportional to the distance between the two electrode squared. The negative sign in front of Eqn. 2.3 is because as the DC voltage is applied to the electrodes, the electrostatic force is increased and pulling the membrane down or acting in the opposite direction of the mechanical spring restoring force given by:

$$F_s = Kz$$

Eqn. 2.4

In Eqn. 2.4: K is the effective spring stiffness of the membrane (not to be confused with "k", the relative dielectric constant) and "z" is the displacement in the vertical direction. If we take "g+z" ("z" would be negative when the top electrode moves towards the bottom electrode), we would obtain what the remaining gap is after a certain displacement.

It is obvious through observation that as the voltage is increased the electrostatic force grows exponentially while the mechanical restoring force only grows linearly. It can be shown that for relatively low DC voltages that the system has two equilibrium points at which the electrostatic force equates the mechanical restoring force of the membrane (Figure 2.3). As it turns out, only the lower crossing in the figure is a stable equilibrium point. The upper crossing is not stable because any small displacement in either direction would cause one force to become dominant and the membrane would shift away from equilibrium conditions.

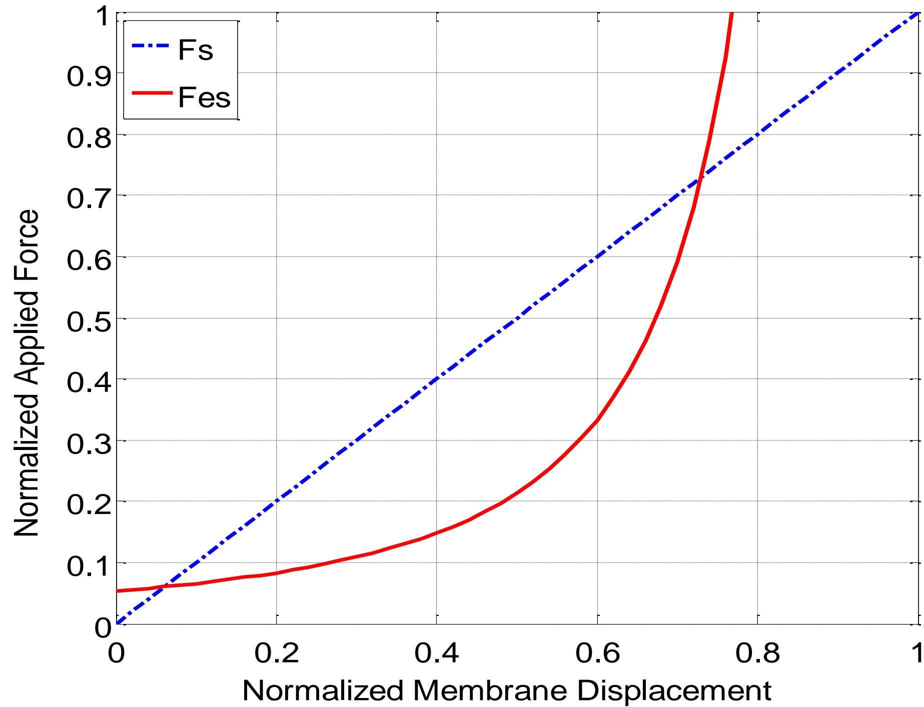


Figure 2.3 Mechanical vs. electrical forces on a parallel plate membrane for low DC Voltage

As the DC voltage is increased further the quadratic electrostatic curve will shift upwards and leftwards while the mechanical force remains the same. This means that after a certain voltage, there will not be a point where the mechanical force can restore or balance out the electrostatic force. This occurs at exactly when the displacement of the parallel plate membrane travels 1/3 of the original gap and can be seen in Figure 2.4:

This means that at the moment just before collapse occurs, the remaining vacuum gap has reduced to 2/3 of the original gap size "g":

$$Z_{collapse} = \frac{g}{3} \qquad \text{Eqn. 2.5}$$

$$g_{col} = \frac{2g}{3} \qquad \text{Eqn. 2.6}$$

The voltage at which this phenomenon occurs is known as the collapse voltage ($V_{collapse}$) and if we combine equations 2.1, 2.3, and 2.4 with "z" in Eqn. 2.4 as "$Z_{collapse}$" and "x" in Eqn. 2.3 as "g_{col}" then $V_{collapse}$ is expressed as:

$$V_{collapse} = \sqrt{\frac{8Kg^3}{27\varepsilon_0 A}} \qquad \text{Eqn. 2.7}$$

This is the limiting voltage for non-collapsed mode CMUT operation and need to be evaluated and considered during a particular design. Beyond this voltage, the CMUT membrane simply collapses towards the bottom electrode and unable to snap back to its original equilibrium position unless the DC voltage is removed (assuming the shorting of the electrodes did not damage the powering electronics).

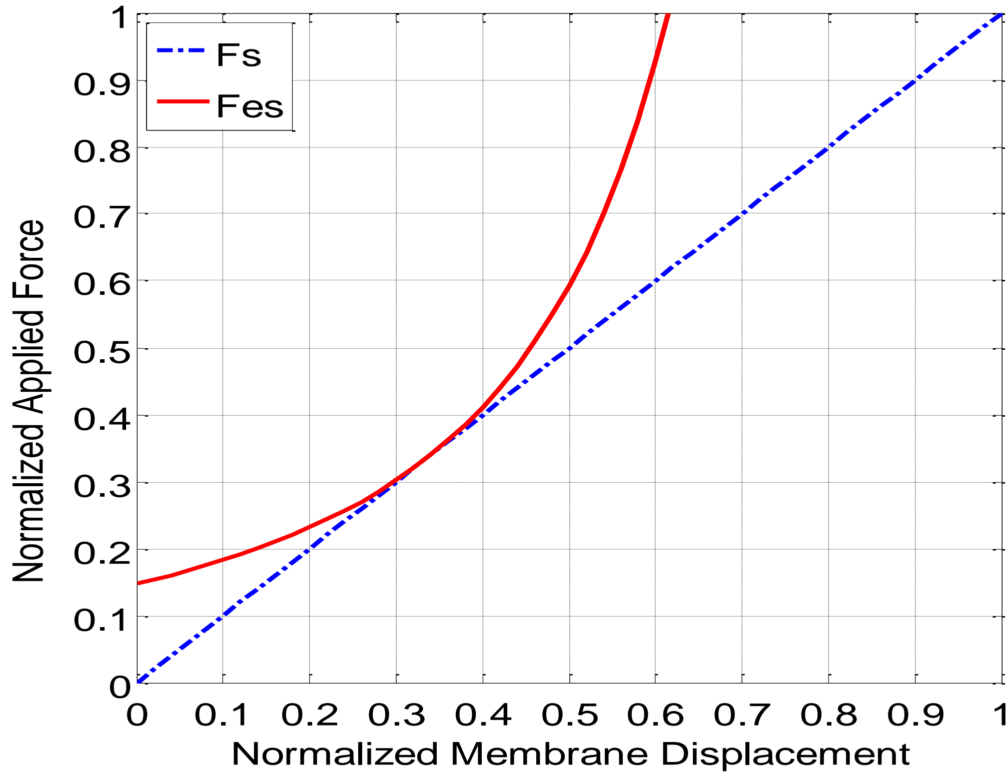


Figure 2.4 Analytical electrostatic and spring forces as a function of the normalized gap at collapse voltage and displacement of 1/3 gap.

Although this result is elegant, we will not analyze the ideal parallel plate any further because it is not representative of the realistically micro-fabricated structure. Typically at least one dielectric isolation layer exists between the top and bottom electrode with some known thickness "t_d" and dielectric constant "k" so that in the event when the top and bottom electrode touch during either collapse or large transient operations, the electrodes will not short to each other and damage the powering electronic circuits as well as stop normal operation. This introduction of the thin dielectric layer essentially adds another capacitance in series with the vacuum such that:

$$C_{tot} = \frac{C1 * C2}{C1 + C2} = \frac{\varepsilon_0 A}{(g + \frac{t_d}{k})} \qquad \text{Eqn. 2.8}$$

This is illustrated through the schematic drawing in Figure 2.5.

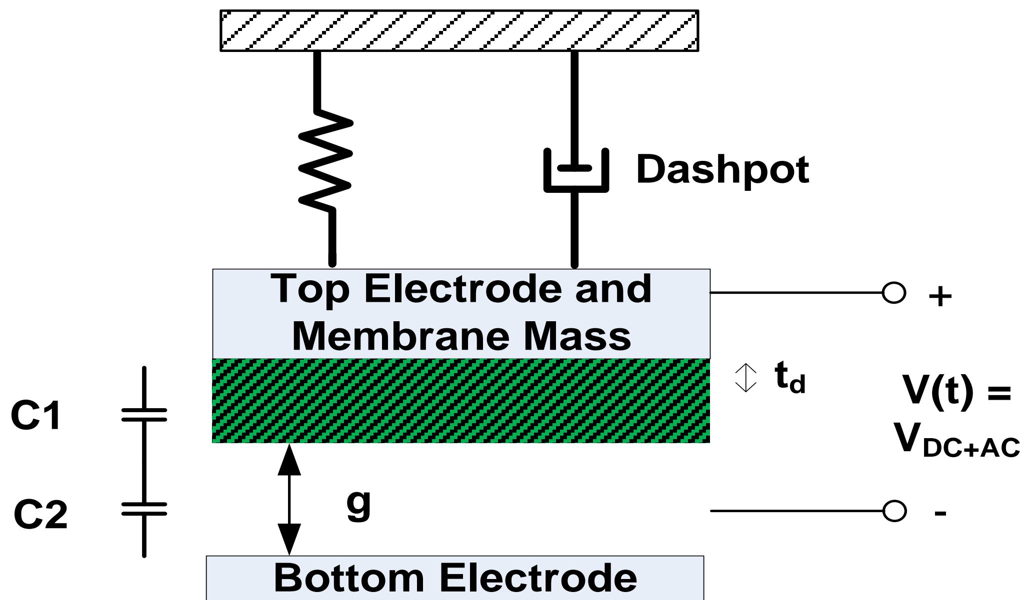


Figure 2.5 Plot showing a dielectric layer between the vacuum gap and the electrodes, which is analogous to 2 series capacitances

The denominator of Eqn. 2.8 is known as the effective gap and is defined below:

$$g_{eff} = g + \frac{t_d}{k} \qquad \text{Eqn. 2.9}$$

With this addition of a thin dielectric isolation layer, the electrostatic force equation is modified through the change in the capacitance term in the energy Eqn. 2.2:

$$F_{el_iso} = \frac{\varepsilon_0 \, AV^2}{2\left(g + \frac{t_d}{\kappa}\right)^2} \qquad \text{Eqn. 2.10}$$

The collapse voltage also modifies to the following:

$$V_{Collapse_iso} = \sqrt{\frac{8K{g_{eff}}^3}{27\varepsilon_0 A}} \qquad \text{Eqn. 2.11}$$

With the dielectric layer, the membrane will have moved by $1/3*g_{eff}$ before collapse, resulting in a physical remaining gap of $g-1/3*g_{eff}$ and is expressed as follows:

$$g_{col_iso} = \frac{2}{3}g - \frac{t_d}{3\kappa} \qquad \text{Eqn. 2.12}$$

It can be seen from Eqn. 2.10 that if $t_d = 0$, then $g_{col_iso} = g_{col} = 2/3*g$. If $t_d > 0$ then $g_{col_iso} < 2/3*g$ up until $g_{col_iso} = 0$. It is theoretically possible to have the isolation layer so thick that the membrane will never collapse or have a negative g_{col_iso}. The mathematical condition at which this occurs is: $t_d/\kappa > 2*g$. However this is not a desirable thing to design for as the CMUT sensitivity will suffer greatly with thick dielectric isolation layer.

Both the electrostatic force and collapse voltage will be discussed in greater detail in terms of CMUT design in Chapter 3, when the optimum dielectric material choice and design parameters are selected for realistic CMUT fabrication.

2.2.2 Small Signal Dynamic Analysis

In transmit mode of operation, an AC voltage, "V_{AC}" is applied in addition to a DC voltage, "V_{DC}". The total voltage applied to a transmit membrane is thus:

$$V = V_{DC} + V_{AC} \qquad \text{Eqn. 2.13}$$

Small signal analysis for electrostatic force is often useful for cases when $V_{DC} >> V_{AC}$ with V_{AC} written as a harmonic function with frequency "f":

$$V_{AC} = V_0 cos(2\pi f t) \qquad \text{Eqn. 2.14}$$

The square of the total voltage becomes:

$$V^2 = V_{DC}{}^2 + 2V_{DC}V_0 \, cos(2\pi f t) + (V_0 cos(2\pi f t))^2 \qquad \text{Eqn. 2.15}$$

If we substitute Eqn. 2.15 into Eqn. 2.10, then the electrostatic force on the CMUT membrane becomes:

$$F_{el_iso} = \frac{\varepsilon_0 A}{2\left(g + \frac{t_d}{\kappa}\right)^2}\left[\frac{V_0}{2} + V_{DC}{}^2 + 2V_{DC}V_0 \, cos(2\pi f t) + V_0 cos(4\pi f t)\right] \qquad \text{Eqn. 2.16}$$

From Eqn. 2.16 one can see that there are 3 distinct voltage components that generate the electrostatic force: DC bias (V_{DC}), an AC component with frequency "f" and another AC component with "2f" (second harmonic). If we assume that the CMUT is operating with $V_{DC} >> V_{AC}$ then the second harmonic term can be neglected and the transmitting CMUT only sees the linearized input voltage with just the first harmonic AC term. Note that the maximum DC voltage that can be applied is $V_{COLLAPSE_iso}$ if we were

to operate the CMUT in non-collapsed mode. Although small signal analysis gives a nice analytical solution to the dynamic forces on the membrane, it does not allow us to predict large signal AC actuation which can give the maximum full gap swing displacement needed for maximum pressure output from a given membrane with a fixed gap. A more complex modelling method is described by Satir *et al.* [58] that is able to accurately model large transmit signal (large V_0) with fluid loading. Later chapters will make use of this model to better predict the out-comes of large signal transmit pressure output. The details of this complex model is currently neglected to bring focus to the transducer design, fabrication and experimental verification explained in later chapters.

2.2.3 Equivalent Circuit Model

The Mason equivalent circuit model is a lumped element circuit model that can be useful in evaluating some key performance parameters of CMUTs. It is assuming again that the conditions are based on small signal analysis for parallel plate actuation [59]. This model neglects the deformed shape of the membrane and assumes uniform displacement across the membrane geometry. The model is depicted in Figure 2.6 and shows the electro-acoustical conversion circuit in immersion fluid.

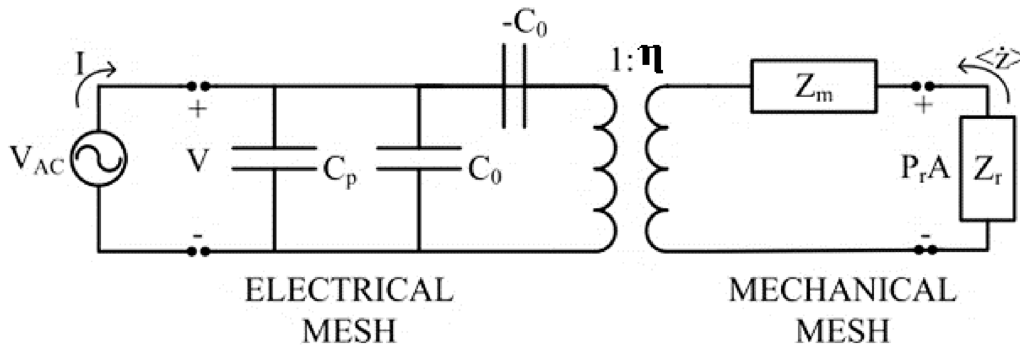


Figure 2.6 Mason’s equivalent circuit for parallel plate transducers.

Although this model is not good for modeling transmit behavior of a transducer (due to large V_{AC} in reality for maximum pressure output); however, it is sufficient in estimating the performance of a parallel plate transducer in receive mode, since the CMUT is typically operated with a larger V_{DC} that is close to collapse to obtain maximum efficiency. When $V_{DC} >> V_{AC}$, the AC part of the electrostatic force becomes:

$$F_{el_AC} \cong \frac{\varepsilon_0 \, A V_{DC} V_0 \, cos(2\pi f t)}{\left(g + \frac{t_d}{\kappa}\right)^2} \qquad \text{Eqn. 2.17}$$

This estimate of the AC part of the electrostatic force is reasonably accurate for receive mode operation because the incoming pressure waves from reflections typically generate very small deflections and changes in capacitance compared to the static bias levels. The left side of the circuit represents the electrical mesh, with all of the parameters of the CMUT represented as lumped circuit elements. The $-C_0$ term is included in the circuit to account for a physical phenomenon known as the "spring softening" effect. This spring softening occurs as a result of the electromechanical interaction and can be seen as the softening in the small-signal spring constant of the membrane [56]. This means that as the CMUT is pulled closer to collapse with increasing V_{DC} the same applied force to the membrane will results in a larger "z" displacement, which means that the effective stiffness of the membrane has "softened" (observed from the electrical side). This is typically seen during impedance measurements of a CMUT device through the use of a network analyzer

measuring the S11 input impedance as shown in Figure 2.7. The shift in the resonant peaks towards lower frequencies can be understood as the “spring softening” effect. The C_p term is accounting for any parasitic capacitances in the system that can originate from: (1) top and bottom electrode traces over lapping each other in places where there are no CMUT gap and (2) wire bonding of electrical input/output contacts.

The right hand side of the circuit represents the mechanical mesh and contains all the parameters for the physical properties of the membrane as well as fluid loading. The mechanical lumped parameters “Z_m” can be represented by an inductor, capacitor and a resistor analogous to mass, spring and damping (membrane). In the mechanical mesh, force and velocity is analogous to voltage and current in the electrical mesh. The radiation impedance, “Z_r”, is defined to be as the ratio between the force acting on the membrane (P_r*A) and the average velocity ($\dot{z}$) of the membrane surface:

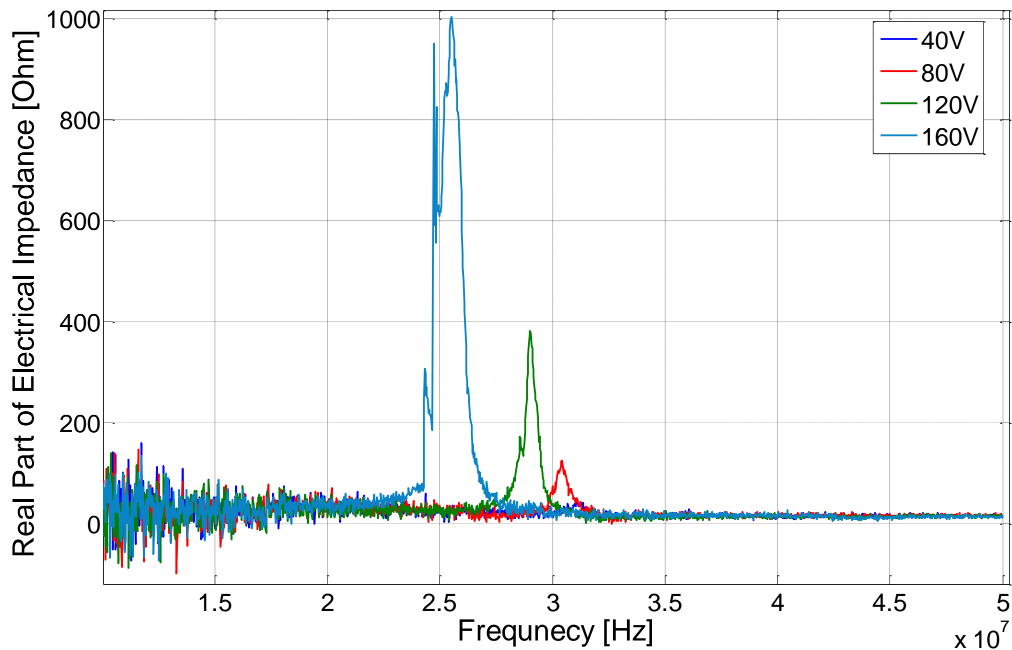


Figure 2.7 Real part of measured electrical impedance of an example CMUT at different V_{DC} bias conditions in air.

This radiation impedance can be complex in the frequency domain as the pressure and velocity on the membrane surface is complex as well. To clarify, the equivalent circuit shown in Figure 2.6 is strictly for transmit mode, as the electrical mesh has an AC voltage source as the actuation signal across the top and bottom electrodes. A receive mode equivalent circuit will look similar except instead of an AC voltage source, there will be in its place a receive amplifier circuitry [60] and a pressure forcing on the mechanical side acting across the radiation impedance. This pressure forcing is the incoming reflected pressure wave from surrounding objects.

2.2.3.1. Transformer Ratio

A useful parameter to evaluate the performance in the receive mode of a CMUT transducer is the transformer ratio (η). It describes the ratio of the force at the mechanical mesh to the voltage at the electrical mesh with units of (Newton/Volt) and is defined as:

$$\eta = \frac{F_{AC}}{V_{AC}} = \frac{\varepsilon_0 A V_{DC}}{\left(g_0 - x + \frac{t_d}{\kappa}\right)^2} \qquad \text{Eqn. 2.19}$$

From Eqn. 2.17, the transformer ratio can be interpreted as the product between the effective electric field across the effective gap, "g_{eff}", and the total capacitance between the top and bottom electrodes. It can be noted that the transformer ratio is proportional to the DC bias (V_{DC}) and inversely proportional to the square of effective gap, "g_{eff}". It can be observed that, in the receive mode, one wants to operate as close to collapse voltage as possible as the transformer ratio will be higher with increasing DC bias. The highest transformer ratio therefore occurs when the CMUT is at $V_{DC} = V_{COLLAPSE_iso}$ and $\eta = \eta_{col}$ and calculated as:

$$\eta_{col} = \sqrt{\frac{3k\varepsilon_0 A}{2g_{eff}}} \qquad \text{Eqn. 2.20}$$

Note that the transformer ratio is now not a function of the DC bias voltage anymore and only dependent on the dielectric constant, the area, and the initial gap, "g" of the CMUT. It can be deduced from observing Eqn. 2.20 that the smaller the initial gap and the larger the dielectric constant, the larger the transformer ratio, thus the more efficient in transduction the transducer will be. This will be discussed in more details in Chapter 3.

2.2.3.2. Coupling Coefficient

The coupling coefficient is another important measure of the efficiency of CMUT transduction and it is defined as a unit-less ratio of the mechanical energy in the transmit mode of operation delivered to the surrounding fluid to the total electrical energy in the receive mode of operation:

$$k_T^2 = \frac{E_{mech}}{E_{elec} + E_{mech}} \qquad \text{Eqn. 2.21}$$

This is a useful parameter to calculate and often used as a comparison with piezoelectric transducers to quantify and compare the efficiency of CMUTs vs. piezoelectric materials in which this term is a function of many material constants [61]. As already alluded to in Chapter 1, the limiting factor for high coupling coefficients in bulk piezoelectric materials is inherently in its material properties and piezoelectric material constants. It is often quoted that k_T^2 is hard to achieve over 50% in bulk piezoelectric which also reduces the bandwidth of the piezoelectric transducer [49].

For parallel plate actuators, the coupling coefficient can be derived through the definition of fixed and free capacitances and is given by [47]:

$$k_T^2 = 1 - \frac{C^S}{C^T} \qquad \text{Eqn. 2.22}$$

This definition uses "C^S" the fixed capacitance of the CMUT at a given DC Bias voltage and "C^T" the free capacitance of the CMUT.

The fixed capacitance, "C^S", and is defined by:

$$C^S = \frac{\varepsilon_0 A}{g_{eff} + z} \qquad \text{Eqn. 2.23}$$

The free capacitance, "C^T", and is defined by:

$$C^T = \frac{\varepsilon_0 A}{g_{eff} + z} + V\,\frac{\varepsilon_0 A}{(g_{eff} + z)^2}\frac{dz}{dV} \qquad \text{Eqn. 2.24}$$

The derivative in Eqn. 2.24 can be calculated through obtaining the displacement to voltage relationship through equating the electrostatic force (Eqn. 2.3) to the mechanical restoring force of the membrane (Eqn. 2.4). Further simplification of Eqn. 2.24 yields:

$$C^T = \frac{\varepsilon_0 A}{g_{eff} + 3z} \qquad \text{Eqn. 2.25}$$

By using the definitions of fixed and free capacitance, the coupling coefficient can be expressed as:

$$k_T^2 = \frac{-2z}{g_{eff} + z} \qquad \text{Eqn. 2.26}$$

Another way of obtaining the coupling coefficient can be derived based on the equivalent circuit definitions [59]:

$$k_T^2 = \frac{Q^2}{\varepsilon_0 AK(g_{eff} + z)} \qquad \text{Eqn. 2.27}$$

Where Q is the charge and can be defined by:

$$Q = CV = \frac{\varepsilon_0 AV}{g_{eff} + z} \qquad \text{Eqn. 2.28}$$

If we substitute Q from Eqn. 2.28 into Eqn. 2.27, then the coupling coefficient expression becomes:

$$k_T^2 = \frac{\varepsilon_0 AV^2}{K(g_{eff} + z)^3} \qquad \text{Eqn. 2.29}$$

If we then re-arranged Eqn. 2.1 to be solved for V:

$$V = \sqrt{\frac{-2Kz(g_{eff} + z)^2}{\varepsilon_0 A}} \qquad \text{Eqn. 2.30}$$

We can finally substitute Eqn. 2.30 into Eqn. 2.29 such that the result will be the same as originally expressed in Eqn. 2.26.This is an important result as it suggests that when the displacement of the top electrode is zero, the coupling coefficient is also zero. As the displacement "z" approaches $z_{collapse} = g/3$, the coupling coefficient can approach to unity. This means that at the moment of collapse, all the mechanical energy has converted to electrical energy. This is shown in Figure 2.8 with coupling coefficient plotted as a function of applied voltage that's normalized to the collapse voltage. We can see that this graph is highly non-linear and that it is extremely inefficient to operate at 50% of $V_{collapse}$ as the coupling coefficient is only ~10%. But at 95% $V_{collapse}$ the coupling coefficient is increased to ~57% and sharply rises to 100% as the DC bias is increased even more closer towards collapse voltage. Therefore, in receive the CMUT should never

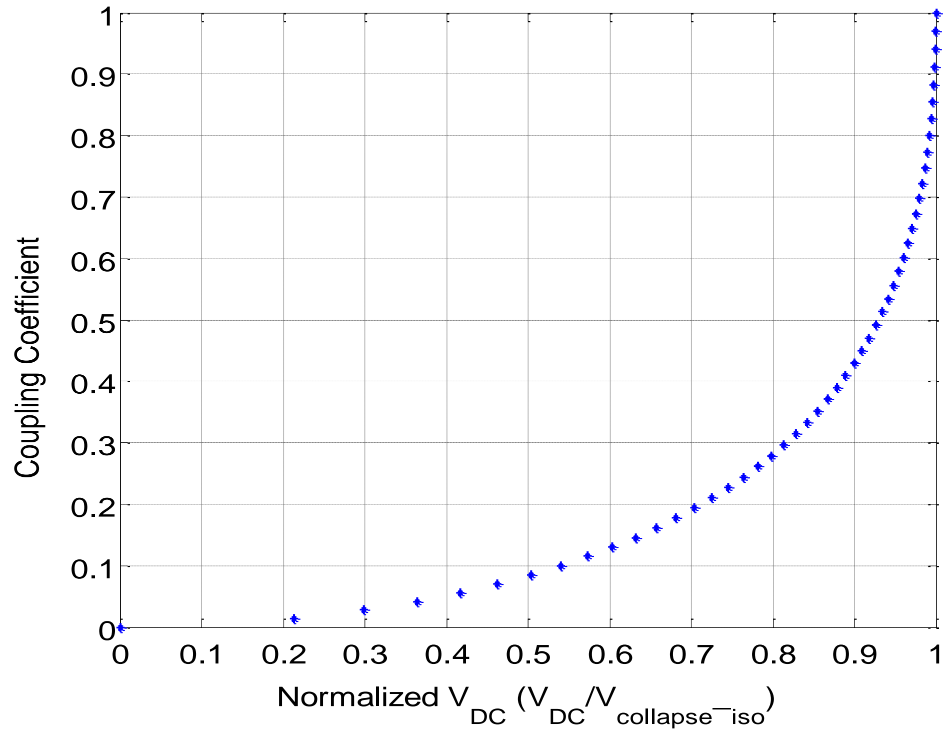


Figure 2.8 Coupling coefficient as a function of DC voltage normalized to collapse voltage for a parallel plate model of the CMUT. At V/Vcol of 1 means that the top electrode has travelled a distance of $g_{eff}/3$.

be biased at a DC level less than 90% of $V_{collapse}$ because the sensitivity will suffer and energy transfer will be less than 50% between the electrical and mechanical domain. These calculations have been previously shown in publications [45], [47], [56], [62] and text books [63] on the subject matter and are only iterated to complete later discussion on CMUT performance and in aid with CMUT design.

2.3. CMUT Fabrication Techniques and Integration Methods with IC

2.3.1 CMUT Fabrication Techniques

2.3.1.1. Wafer Bonding Technique

Over the past decade, two major fabrication methods for CMUTs became predominately popular and cited in literature. The first method is a wafer bonding technique, using silicon on insulator (SOI) wafers with thin low resistive silicon as the structural membrane [64]–[66]. Gaps can be controlled reasonably well to within ~100 nm as shown in Figure 2.9.

Variations of the wafer bonding method have been shown in literature including a 2D row-column CMUT array from Christiansen *et al.* [67] and can be seen in Figure 2.10. This particular wafer bonding processes uses 5 masks and also uses SOI wafer with a layer of high electrical insulating buried oxide layer (BOX) to act as the insulation layer between top and bottom electrodes [68]. Advantages of the wafer bonding include: (1) avoiding wet sacrificial layer etches and issues with chemical selectivity as well as stiction or collapsing of the membrane when performing wet release of sacrificial layer, (2) flexibility in membranes of different sizes and shapes since the membranes and cavities are fabricated

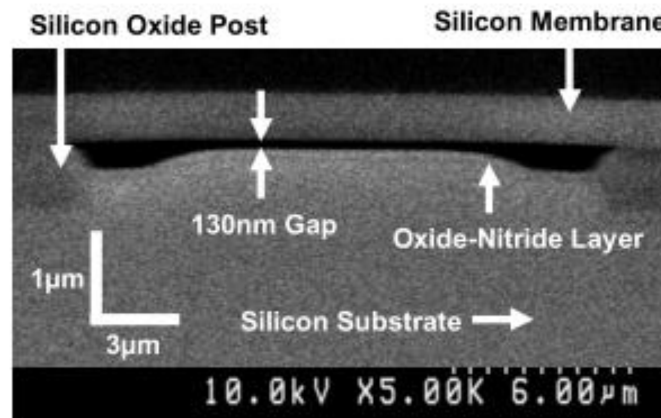


Figure 2.9 SEM image of the cross section of a single CMUT cell fabricated using the wafer bonding technique [64].

on different wafers, (3) good membrane thickness uniformity can be achieved if SOI wafers with single crystal silicon layer is used as the membrane material.

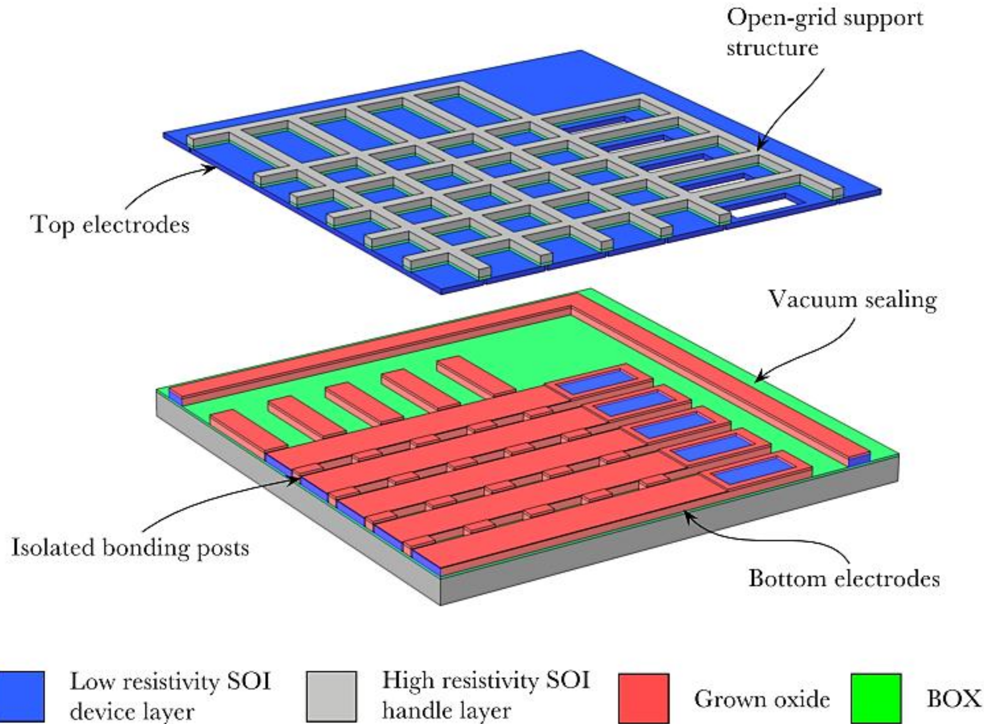


Figure 2.10 2-D row-column array design using SOI with BOX layer [67].

2.3.1.2. Sacrificial Release Technique

In the second method of fabricating a CMUT is a surface micromachined or top-down approach where the electrodes are defined by thin metal layers and the vacuum gap is defined by a sacrificial wet release and sealed by the membrane material under vacuum [69], [70]. The wet release is done by first etching the membrane material open on the sides to access the sacrificial material layer before submerging it under an wet etchant to release. After the etching of the sacrificial layer is complete, the etchant is evacuated and the sacrificial release holes are sealed again with typically some dielectric or membrane

material under vacuum, as shown in Figure 2.11.

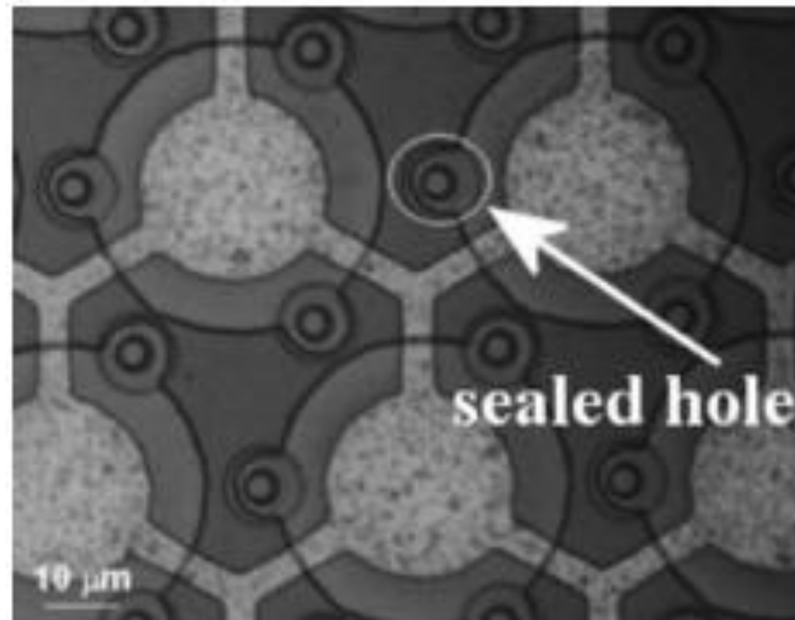


Figure 2.11 Micrograph of sacrificial release CMUTs with circular membrane geometry showing sealed holes that were etched to the sacrificial layer [141].

In both fabrication methods, a layer of dielectric exits between the top and bottom electrode structures to ensure that the electrodes do not electrically short during full gap swings in transmit and near membrane collapse operations during receive. This layer of dielectric material must by design be able to withstand the maximum electric fields generated within the material during CMUT operations, especially if the CMUT has already collapsed and the electrodes are separated only by the thin dielectric layer. Materials such as stoichiometric LPCVD silicon nitride (Si_3N_4), PECVD Si_xN_y, thermal silicon oxide (SiO_2) and PECVD SiO_2 are traditional materials used in either fabrication process as the isolation dielectric material. Advantages of the sacrificial release method include: (1) lower process temperatures as compared to bonding processes, (2) no need for precise and extremely clean surface conditions that is often required during wafer bonding

that determines the gap geometry, (3) does not require more expensive SOI wafers for processing. Common fabrication issues with this method include: (1) stress in the silicon nitride causes the membrane to bow down, thus reducing the physical vacuum gap, (2) while wet releasing the sacrificial layer, stiction of the membrane to the bottom electrode can occur due to capillary forces as the liquid inside the cavity is dried or evacuated. This means that if the stress in the membrane material is relatively significant due to thermal mismatch and intrinsic stress from deposition conditions, then larger surface area membrane geometry will be difficult to fabricate with high uniformity.

It is not clear other than some of the fabrication advantages and limitations mentioned that one method is necessarily "better" than the other; however, when choosing a method one must take into account important factors such as IC integration strategy, complexity of process flow, availability and quality of processing equipment. The following section will discuss the various strategies for front-end IC integration to allow the MEMS membrane to be successfully integrated with front end amplifiers, buffers and multiplexing circuitry.

2.3.2 CMUT and IC Integration Techniques

The main motivation for front-end CMUT-on-CMOS integration is to (1) reduce the number of output channels through utilizing multiplexing circuitry thus reducing overall cable count and (2) reducing parasitic capacitances such that small CMUT transient pressure signals in receive mode can be above parasitic capacitance level in the cables and interconnects.

There are four main integration methods for CMUT and ICs: (1) CMUT-in-CMOS, (2) Interleaved CMUT-CMOS, (3) Flip Chip Integration and (4) CMUT-on-CMOS. Each of these approaches have their own advantages and disadvantages and will

be discussed below. The last method of CMUT-on-CMOS is the approach that was selected for this thesis work.

2.3.2.1. CMUT-in-CMOS

Processing of the CMUTs can be simultaneously accomplished with the fabrication of electronics utilizing reliable and well-established CMOS processing techniques [71]. Because of the parallel processing, the overall fabrication time and processing costs are reduced. However, the design space for the CMUTs suffers from the limited CMOS fabrication options in terms of material types, material properties, and layer thicknesses. For example, the process described in Cheng *et al.* [71] are limited to standard n-well process materials such as poly-silicon layers, thick silicon dioxides and aluminum layers and their thicknesses are limited to the CMOS design rules. Total device area also increases because the electronics and CMUTs must be positioned side-by- side. Therefore, this is not an ideal scheme for FL-IVUS applications, in which available space is limited.

2.3.2.2. Interleaved CMUT-CMOS

To improve upon the CMUT design space, it is possible to interrupt the electronics fabrication for outside processing [72], [73]. This method has been utilized to generate smaller gap heights compared with the aforementioned CMUT-in-CMOS processing. Effective gap was also reduced by utilizing higher relative permittivity insulator material such as borophosphosilicate glass (BPSG) as opposed to standard silicon dioxide. This technique increases cost and fabrication complexity and may experience resistance from commercial CMOS foundries because of contamination concerns. In addition, even though CMUT performance can be improved, this process is still similar to the standard CMUT-in-CMOS technique, in which available area is not optimally utilized. The side-by-side

positioning of the CMUT and CMOS takes up approximately two times as much space as compared to if one stacked the CMUT and CMOS on top of each other.

2.3.2.3. Flip Chip Integration

To improve utilization of available device area, and to allow better optimization of CMUT material properties, separately fabricated CMOS and CMUT chips can be electrically connected through flip-chip bonding [74], [75]. In this case, the CMUTs are not limited to low-temperature, CMOS-compatible fabrication processes, nor are they limited to the materials and layer thicknesses designated by standardized foundry processes. However, this interconnect method requires several additional fabrication steps that include deep reactive ion etching (RIE), conformal metal and dielectric depositions, backside patterning, and the final wafer bonding step [76]. Furthermore, the packaging techniques associated with this technology are complex in nature, adding to the overall cost. This technique is attractive for larger CMUT arrays [36], but may not be ideal for FL-IVUS applications because the minimum solder bump pitch approaches the CMUT element pitch. For example, membrane lateral geometry can be in the range of 20-50μm.

2.3.2.4. CMUT-on-CMOS

The work described in this thesis uses the CMUT-on-CMOS process in which CMUTs are fabricated directly on top of pre-processed CMOS wafers, similar to those described by Noble *et al.* in [77], [78] and Daft *et al.* in [79]. This interconnect approach minimizes parasitic capacitances associated with connection lines and introduces only one additional masking step. The total occupied area is minimized because the CMUTs can be located over CMOS metal layers, similar to the flip chip bonding method, but without the complexity and spacing requirements associated with solder bump technology. In addition,

the CMUTs are not constrained by the CMOS processing steps, so it is possible to optimize material properties and produce thinner vacuum gaps for low-voltage operation and increased electromechanical coupling efficiency. A drawback to this method is that fabrication is limited to processes under 250°C, so as not to damage the CMOS. However, it is shown in Chapter 4 that the performance of CMUTs fabricated with such low-temperature plasma-enhanced chemical vapor deposited (PECVD) silicon nitride and oxide are not significantly affected. The main design trade-offs associated with different CMOS integration approaches are summarized in Table 2.1, with plus signs meaning advantages or favorable and minus signs for disadvantages and dis-favorable. For the design constraints associated with FL-IVUS, CMUT-on-CMOS fabrication was pursued as a good compromise, with advantages in optimal space utilization, minimal parasitic capacitances, and relative ease of fabrication and final assembly. The full process flow and fabrication of the CMUT-on-CMOS will be shown in Chapter 4.

Table 2.1 CMUT to CMOS Integration Technique Comparison

	Type of MEMS to CMOS Integration Approach for CMUTS			
Comparison Criterion	**CMUT-in-CMOS**	**Interleaved**	**Flip Chip Bonding**	**CMUT-on-CMOS**
Number of Processing Steps	+	+	-	-
Active CMUT area optimization	-	-	+	+
Processing Temperature	n/a	-	+	-
Gap height control	-	+	+	+
CMUT-on-CMOS interconnect assembly	+	+	-	+
Foundry compatibility	+	-	n/a	n/a

CHAPTER 3. IMPROVED TRANSMIT AND RECEIVE SENSITIVITY OF CMUT AND CMUT-on-CMOS ARRAYS USING HIGH-K INSULATION LAYER

As for mentioned in Chapter 1, one of the key figure of merits in terms of imaging criterion and goal is to have better penetration depth in the ultrasound image. This desired imaging requirement translates into a need for either (1) greater pressure output and (2) higher receive sensitivity from the CMUT. As explained in Chapter 2, the maximum pressure output of a single membrane is dependent on the maximum gap swing the membrane can produce which in turn is determined by the height of the vacuum gap. The larger the vacuum gap the more a membrane can displace and in turn achieve a higher output pressure. However, if the gap is too large, the trade-off is that a large voltage pulse is needed to achieve the full-gap swing. On the receive side, one wants to usually provide DC bias so that the membrane is pulled as close to $V_{COLLAPASE}$ as possible so that the coupling coefficient can be maximized. In both transmit and receive mode, it can be seen from the equivalent circuit analysis that a theoretically infinite high-k value and thin material with high break-down strength would be the ideal insulation layer to use to increase the electrostatic force and coupling coefficient. Since this type of material does not exist, this chapter explores how one can choose the most suitable high-κ insulation layer and compare the performance to that of PECVD silicon nitride (Si_xN_y) insulation layer typically used for fabricating low-temperature and low-stress membranes.

3.1. Motivation and Introduction for High-κ Insulation

As suggested by the simple linear parallel plate CMUT equivalent circuit, which is suitable for modeling small signal receive mode operation, the electromechanical transformer ratio of a CMUT is determined as the product of the DC electric field and the

device capacitance [80]. In the transmit mode, where large voltage signals are applied to obtain large membrane displacement swings, the electrostatic force applied to the CMUT membrane is a quadratic function of the ratio between the applied voltage to the instantaneous gap [58]. Therefore, one should reduce the gap between the top and bottom electrodes of the CMUT for efficient operation with reduced voltage levels. Limitations to the gap thickness will be the minimum gap thickness required for the desired transmit pressure at the operation frequency and the fabrication process limitations. Ideally the gap between the electrodes is filled with vacuum and can be completely traversed during the CMUT operation, but most realistic CMUT structures are as shown in Figure 2.2. A layer of dielectric material exists between the top and bottom electrodes to ensure that the electrodes do not electrically short during full gap swings in transmit and near collapse operation during receive. This layer of dielectric material must by design be able to withstand the maximum electric fields generated within the material during CMUT operation, especially if the CMUT has already collapsed and the electrodes are separated only by the thin dielectric layer [51], [81]–[83]. If one keeps the movable vacuum gap thickness the same to retain the same membrane displacement range, for a given applied voltage, this dielectric layer reduces the electric field and the device capacitance since it effectively increases the vacuum gap thickness. As further discussed below, the choice of the dielectric layer becomes a significant factor in determining the electromechanical performance of the CMUT, especially when the vacuum gap thickness is small (<100nm).

Materials such as low pressure chemical vapor deposition (LPCVD) silicon nitride (Si_xN_y), plasma enhanced chemical vapor deposition (PECVD) Si_xN_y, thermal silicon oxide (SiO_2) and PECVD SiO_2 are traditional dielectric materials in semiconductor

processing and they are commonly used as the insulation dielectric material in different CMUT fabrication processes [64], [69], [70], [84]. Here I focus on a low temperature surface micromachining based CMUT fabrication process, which allows monolithic integration of CMOS electronics and CMUT imaging arrays [79], [87], [86]. This approach is particularly suitable for catheter based ultrasound imaging applications where small size and flexibility is important [83], [87], [88].

In low temperature surface micromachining processes for CMUTs it is convenient to use the same PECVD Si_xN_y (abbreviated as SiN) as the dielectric insulation material [70], [86], [89], [90] and membrane structure material. However, as demonstrated below, higher performance CMUTs can be realized by choosing a high-κ dielectric material (high dielectric constant κ as compared to silicon dioxide) with minimal adverse effects in terms of achievable device capacitance and electric field.

There are many high-κ materials cited in literature with dielectric constants ranging from 9-200 [91], [92], seen in Figure 3.1. However, there is a tradeoff between dielectric breakdown strength (E_{BD}) and the dielectric constant κ. This is a non-linear relationship shown both in theory and in experiments [91], [93] shown in Figure 3.1, meaning that a decrease in dielectric strength corresponds to an increase in κ value. In Figure 3.2, the band gap energy is plotted instead of dielectric breakdown strength, but it is directly proportional to the dielectric's ability to stay as an insulator. In selection of a suitable high-κ dielectric material to improve capacitance while designing for maximum voltage requirements of CMUTs, I took a balanced approach in material selection of these two parameters. According to Robertson [93], dielectric materials with a good balance between κ and E_{BD} are ZrO_2, HfO_2, La_2O_3, Y_2O_3 and SrO. I chose hafnium oxide (HfO_2) for the study in this

thesis work due to its promising material performances in terms of κ and E_{BD} and its wide use in the scale down of complementary metal oxide semiconductor transistors (CMOS) [94]. Although there are many methods to deposit high-κ dielectric materials such as sputtering and chemical vapor deposition (CVD), here the method of atomic layer deposition (ALD) is selected. This method is attractive for CMUT application because of its low temperature processing, conformal deposition over large areas, intrinsically stress free film and ability to have nanometer precision control over the thickness of the film [95], [96].

In this work, ALD HfO_2 (abbreviated HfO) film is deposited at 250^0C and both κ and E_B are characterized in Section 3.3.3. It is noted that previous work with ALD materials for CMUTs focused on advantages of aluminum oxide (Al_2O_3) as a thin conformal

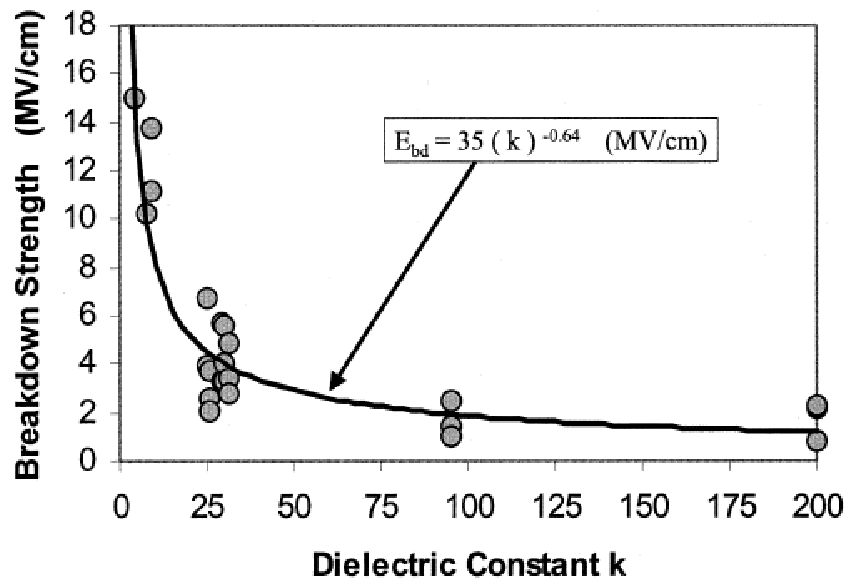


Figure 3.1 Relationship between dielectric breakdown strength and dielectric constant for a variety of dielectric materials [91].

structural film as a membrane material [97], [98]. The advantages of using ALD materials for collapsed mode CMUT operation due to its high dielectric constant has also been proposed in the past, but no optimization study or experimental data has been provided [99].

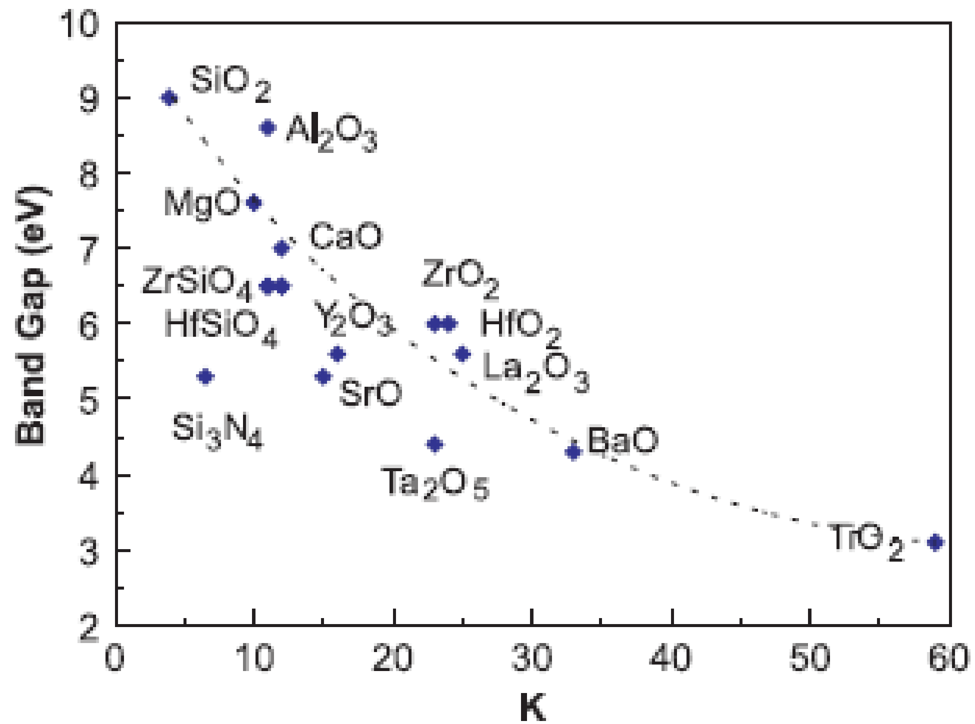


Figure 3.2 Relationship between band gap energy and dielectric constant for a variety of dielectric materials [93].

3.2. Design of High-K Dielectric Insulation CMUTs

3.2.1 Criteria for Choosing the Isolation Layer Material

In order to compare dielectric materials for CMUT applications, I follow a step by step approach. I first focus on the electrostatic force and transformer ratio, limited by the breakdown strength and at the limit of vanishing vacuum gap. I then calculate these parameters specifically for HfO and SiN materials for practical vacuum gap and insulation layer thickness. Finally, I impose the collapse voltage limitations on these curves for a particular CMUT geometry used in experimental comparisons. Using a simple parallel plate model as shown in Figure 2.2, the electrostatic force applied to the electrodes, F_{el_iso}, can be written as Eqn. 2.10 where "ε_0" is the permittivity of free space ($F \cdot m^{-1}$); "κ" is the dielectric constant or relative permittivity of the material (unitless); "g" is the vacuum gap (m); "$V(t) = V_{DC}+V_{AC}$" is the total input voltage (V). The term in the denominator of Eqn. 2.10 is also known as the "effective" gap (g_{eff}) of the CMUT which the vacuum and dielectric layer thicknesses can be lumped into a single term. This is simply an equivalent gap value that represents the same capacitance between the top and bottom electrodes of a capacitor. To evaluate the effect of the dielectric material on the electrostatic force, one can consider the limiting case that the vacuum gap "g" is close to zero, and the voltage on the dielectric layer is at maximum value, i.e. $V = E_{BD} \cdot t_d$. In this case, the electrostatic force approaches to the value

$$F_{el_iso} \rightarrow \frac{\varepsilon_0 A (E_{BD} t_d)^2}{2\left(\frac{t_d}{\kappa}\right)^2} = \frac{\varepsilon_0 A (E_{BD} \kappa)^2}{2} \qquad \text{Eqn. 3.1}$$

This result shows that for larger electrostatic force generation in the transmit mode, one should choose the dielectric material with the larger $E_{BD}\kappa$ product. For example, SiN has E_{BD} in 4-9 MV/cm and κ in the 6-7 range [100], which depends on the plasma power, gas ratios, temperature and processing pressure of deposition. The particular nitride layer we use and for CMUT-on-CMOS processing has E_{BD} = 6.5 MV/cm and κ = 6.3 [37]. In comparison, HfO has E_{BD} in 4-6.7 MV/cm range [91] depending on the molecular structure it takes during various deposition conditions. Low temperature HfO typically has breakdown strength of 4MV/cm and κ in 14-16 range as deposited below 300^{0}C. However, higher κ values, in 20-25 range, can be achieved with either higher deposition temperatures as high as 370^{0}C [101]–[103] or post deposition high temperature annealing in the 300-500^{0}C range [91], [93]. Leakage current improvements were also previously observed and reported after annealing, reducing the physical defects that may exist inside the thin film after deposition. Since most of the quoted annealing recipes are within the thermal budget of a CMOS compatible process, these methods can be used to enhance HfO properties for CMUT-on-CMOS implementation. As described in Section 3.3.3, the particular HfO layer deposited for this work has E_{BD} ~ 4 MV/cm and κ ~ 16. Therefore, one can expect a theoretical ~2.5 times improvement in electrostatic force generated when SiN is replaced with HfO and each film used close to their breakdown limit.

For the receive mode, one can use the small signal equivalent circuit turns ratio, "η" [63] as a comparison metric, especially when a low impedance transimpedance amplifier (TIA) is used to convert the current at the output of electromechanical transformer to voltage. A TIA with negligible input impedance will effectively short circuit both the CMUT and parasitic capacitances. As compared to high input impedance voltage

amplifiers, this approach significantly reduces the negative effects of parasitic capacitance and ensures constant voltage operation. Consequently TIA based receiver has been popular for integrated circuit (IC) design for CMUTs, and in this context provides us with a metric independent of the parasitic capacitance [76], [104]. In this case, the output current per membrane velocity (A/(m/s)) will be roughly proportional to η. which is given by Eqn. 2.19, if the spring softening effect is neglected.

If again one considers the limit where the vacuum gap vanishes and maximum field sustainable on the dielectric layer is used, i.e. $V_{DC} = E_{BD} \cdot t_d$, the transformer ratio takes the form

$$\eta \rightarrow \frac{\varepsilon_0 A E_{BD} t_d}{\left(\frac{t_d}{\kappa}\right)^2} = \frac{\varepsilon_0 A E_{BD} \kappa^2}{t_d} \qquad \text{Eqn. 3.2}$$

Therefore, for higher receive sensitivity, one should use the dielectric with a high E_{BD}, but especially high κ due to the quadratic dependence. In addition, the dielectric material which can be deposited as a thinner high quality film should be selected to minimize "t_d" without compromising the dielectric properties. For example, when used at the limiting field strength, HfO should provide up to 3.8 times larger η as compared to SiN of the same thickness. However, as discussed below, reliable deposition of SiN is limited to about 200nm, whereas thinner layers of HfO can be deposited with good dielectric properties, leading to a more significant advantage.

To analyze the effect of the insulation layer on coupling coefficient of a parallel plate CMUT model, one can modify the expression in A16 from [47] such that:

$$k_T^2 = \frac{1}{1+\left(\frac{g_{eff}-3x}{2x}\right)\left(1+\frac{C_p}{C_a}\right)} \qquad \text{Eqn. 3.3}$$

Here, C_p is the parasitic capacitance and $C_a = \frac{\varepsilon_0 A}{(g_{eff}-x)}$ is the active device capacitance under applied bias voltage. Note that if one uses a high-κ dielectric material, then g_{eff} is reduced while keeping the same vacuum gap. This implies that although all CMUTs would theoretically achieve $k_T^2 = 1$ at collapse ($x = \frac{g_{eff}}{3}$), this limit will be approached with a smaller DC bias with reduced g_{eff}. In addition, for any given stable DC bias and non-zero C_p, k_T^2 will be larger since C_a is larger (i.e. the ratio C_p/C_a is smaller). The relevant graphs for the effect of parasitic capacitance on coupling coefficient can be found in [47]. Given the same mechanical properties for the CMUT (same mechanical Q), the noise figure will also improve with larger coupling coefficient as described in [105].

3.2.2 Comparison of HfO_2 and PECVD Si_xN_y Insulation Layers in Transmit Mode CMUT Operation

The maximum output pressure of a transmitting CMUT is determined by the ability to reach full gap swing when actuated. It is important to achieve the same full gap swing with a smaller voltage input, i.e. higher transmit sensitivity. This is especially significant in case of CMUT-on-CMOS integration applications when pulse amplitudes generated by IC pulsers are limited by the CMOS fabrication process [86]. For a fair comparison between HfO and SiN insulation materials I compare the electrostatic force, F_{el_iso}, generated for the same input voltage using Eqn. 2.10 for the same vacuum gap. I then normalize F_{el_iso} with the maximum electrostatic force generated for the same vacuum gap, i.e. *without* the dielectric insulation layer ($t_d = 0$), $F_{el_no_iso}$, to arrive at a force ratio, R_F:

$$R_F = \frac{F_{el_iso}}{F_{el_no_iso}} = \frac{g^2}{(g + \frac{t_d}{\kappa})^2}$$ Eqn. 3.4

Figure 3.3, plots R_F as a function of the vacuum gap thickness for different practical HfO and SiN insulation layer thicknesses. The thickness of SiN is fixed to 200 nm due to the practical minimal thickness achievable during fabrication, and is further explained in Section 3.3. The breakdown field is not considered as a limitation in this graph. The thinnest insulation layer shows the closer behavior to the ideal case (R_F=1), as expected. For gap thickness larger than 200 nm, all insulation layers considered achieve R_F>0.75, i.e. the insulation layer material does not make a significant difference for large gaps. However, for small gap thicknesses, 50 nm and below, which are important for high frequency ultrasound applications, the difference is significant. For example, R_F = 0.64 and 0.37 for 200 nm thick HfO and SiN, respectively, at a gap of 50 nm. This shows that the CMUT with HfO layer will generate 4.75 dB larger electrostatic force generated when compared to a device with SiN. It should be noted that 200 nm thick HfO is not an optimized thickness and can be further reduced depending on the specific CMUT geometry design without surpassing the breakdown voltage limit (V_{BD}). Since a thinner dielectric material corresponds to a larger electrostatic force, one should choose the thinnest possible dielectric layer that can withstand the maximum operating voltage without exceeding the breakdown field of the dielectric. Hence, the thickness of the HfO dielectric (t_d), V_{BD} and

$V_{COLLAPSE}$ are considered as optimization parameters in designing CMUTs for maximum electrostatic force for given input voltage during non-collapse transmit mode operation.

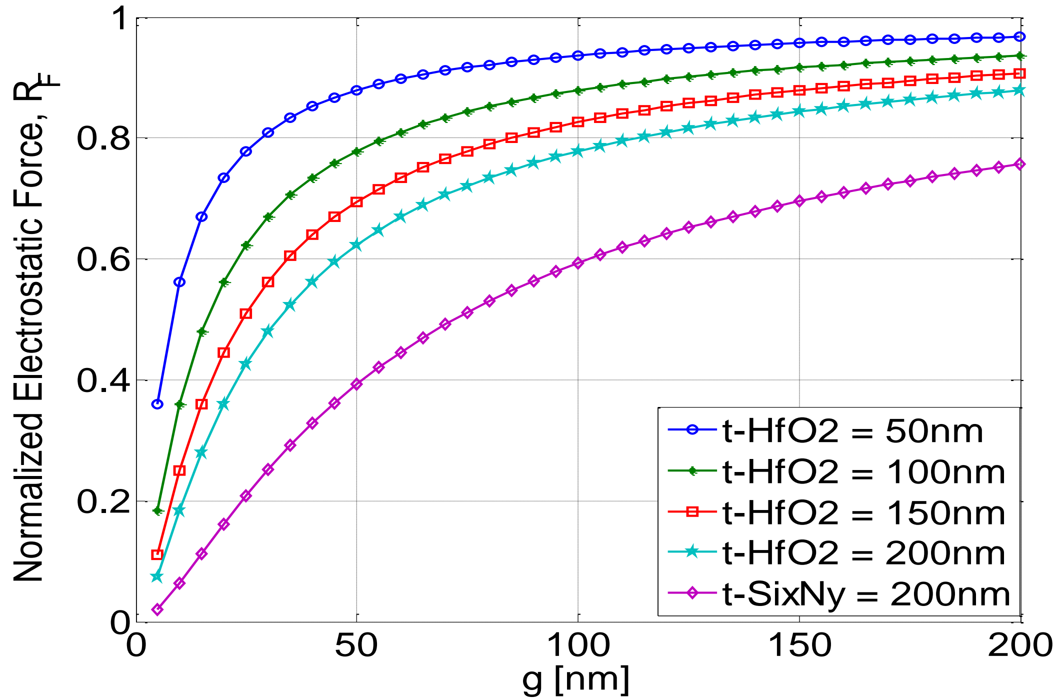


Figure 3.3 A plot of normalized electrostatic force (R_F) for the same input pulse between HfO Vs. SiN isolation device as a function of vacuum gap. $F_{el_no_iso}$ is when $t_d = 0$. SiN thickness is assumed constant at 200nm. $\kappa = 16$ and 6.3 for HfO and SiN respectively used. Top 4 curves are different thicknesses of HfO.

3.2.3 Comparison of HfO_2 and PECVD Si_xN_y Insulation Layers in Receive Mode CMUT Operation

To increase the sensitivity of a CMUT during receive mode operation, the CMUT should be biased close to collapse [45]. Therefore the maximum operating V_{DC} is $V_{COLLAPSE}$ for non-collapsed mode operation, which can be expressed as Eqn. 2.11, where "*K*" is the stiffness of the membrane [106].

The collapse voltage will increase for any fixed vacuum gap if either the thickness of the dielectric increases or the dielectric constant decreases. Thus the advantage of HfO

over SiN insulation is a lower collapse voltage for the same insulation thickness due to higher κ values and can be observed from Eqn. 2.9 and Eqn. 2.11. Additionally, if the thickness of HfO can be physically reduced further than SiN during fabrication, then the collapse voltage of a device with HfO layer can be even lower than that of a SiN insulation device given the same vacuum gap, stiffness, and electrode area. A lower collapse voltage is advantageous in reducing the maximum DC operating requirements while still able to achieve maximum sensitivity. This is especially advantageous in voltage limited situations such as CMUT-on-CMOS integration [107].

Given that η at collapse is expressed in Eqn. 2.20, one can improve the receive sensitivity by using a dielectric layer with a higher κ. However to capture both factors, reduction of collapse voltage and increase in the transformer ratio for a given vacuum gap thickness, one can use the transformer ratio evaluated at collapse and then normalize it to the corresponding collapse voltage itself.

Using a normalization similar to (R_f) in Eqn. 3.4, the ratio of the transformer ratio at collapse to the collapse voltage for a given gap and dielectric layer thickness (η_{col_d}) can be normalized to the case without the dielectric layer (η_{col_nd}). Hence, one can obtain R_η as

$$R_\eta = \frac{\eta_{col_d}}{\eta_{col_nd}} \qquad \text{Eqn. 3.5}$$

In Figure 3.4, it is observed that the calculated R_η has the same variation as R_f calculated for the electrostatic force ratio since both R_f and R_η simplify to the same fractional expression:

$$R_F = R_\eta = \frac{{g_0}^2}{(g_0 + \frac{t_d}{\kappa})^2} = \frac{{g_0}^2}{(g_{eff})^2} \quad \text{Eqn. 3.6}$$

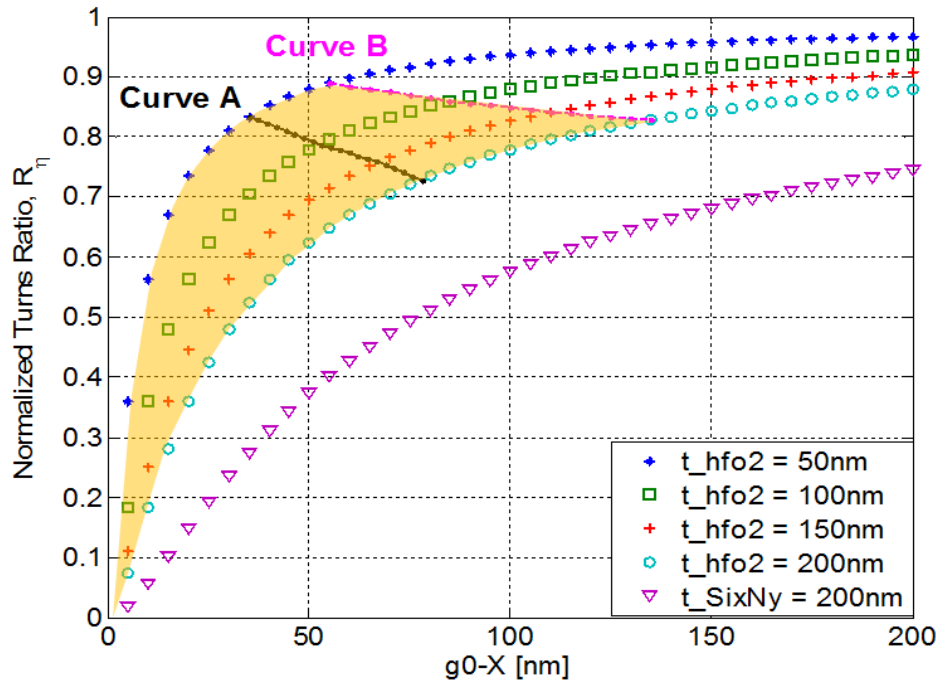


Figure 3.4 A plot of the ratio of transformer ratios normalized to the collapse voltage R_η for HfO and SiN isolation CMUTs compared to the ideal case of parallel plate with no isolation. Design Curve A is based on $V_{collapse_iso}$ calculated from Eqn. 2.11 and Design Curve B is based on $V_{COLLAPSE}$ calculated from a large signal model. E_{BD} of HfO used in calculation is 4 MV/cm. Shaded area is acceptable design space.

Similar to Figure 3.3, using HfO instead of SiN one can achieve the same maximum receive sensitivity with smaller DC bias, or conversely one can achieve higher maximum receive sensitivity with the same available DC bias. For a typical case of 50nm gap and 200nm dielectric layer thickness, the gain will be 4.45dB.

3.2.4 Insulation Design for a Practical CMUT

Although small gaps, very thin insulation, and high κ values are desirable to obtain large transformer ratio near collapse, there are practical limitations such as the breakdown field strength (E_{BD}) of the insulation layer which can withstand at $V_{COLLAPSE}$. Thus, the nature of optimizing t_d becomes an inequality problem since $V_{COLLAPSE}$ is a function of t_d and cannot be greater than $V_{BD} = E_{BD}\, t_d$ for non-collapse mode CMUT operation.

Then, for any CMUT design we need to choose the smallest t_d that can satisfy the following inequality:

$$V_{COLLAPSE}(t_d) < V_{BD}(t_d) \qquad \text{Eqn. 3.7}$$

To determine the range of gaps that are feasible for a particular design thickness of HfO, the collapse voltage is calculated either with Eqn. 2.11 or with the large-signal model used in [58] for higher accuracy to match the breakdown voltage at a particular HfO thickness. As an example, this calculation is performed for a 35 μm ×35 μm square, 2.2μm thick SiN membrane with Young's modulus of 110 GPa and Poisson's ratio of 0.22. The overall membrane stiffness is estimated using static Finite Element Analysis (FEA). The stiffness (K) used in Eqn. 2.11 to calculate $V_{COLLAPSE}$ is re-calculated for each data point (different HfO and SiN thicknesses) based on average membrane displacement to a

uniform pressure on the electrode area of 25×25 μm^2. The displacement result simulated by COMSOL^{TM} Multiphysics (Burlington, MA) is shown in Figure 3.5 for one particular case (100nm HfO) as an example.

By equating the collapse voltages at various gaps to the breakdown voltage of different thicknesses of HfO films, 2 design curves are shown in Figure 3.3. Note that an E_{BD} of 4MV/cm for HfO is used to calculate the breakdown voltage at a particular thin film thickness, which is experimentally determined and described in Section 3.3.1.4. The difference between the design curves is the method used to calculate $V_{COLLAPSE}$ which is based on: (1) the parallel plate model (curve A in Figure 3.4) in Eqn. 2.11, and (2) the large-signal model (curve B in Figure 3.4) being more accurate in modeling the stiffness of the square membrane which results in higher collapse voltages than the simple parallel-plate equation. This design curve helps one to choose the minimum HfO thickness for a given gap design such that the condition in Eqn. 3.7 is satisfied. Note that the CMUT

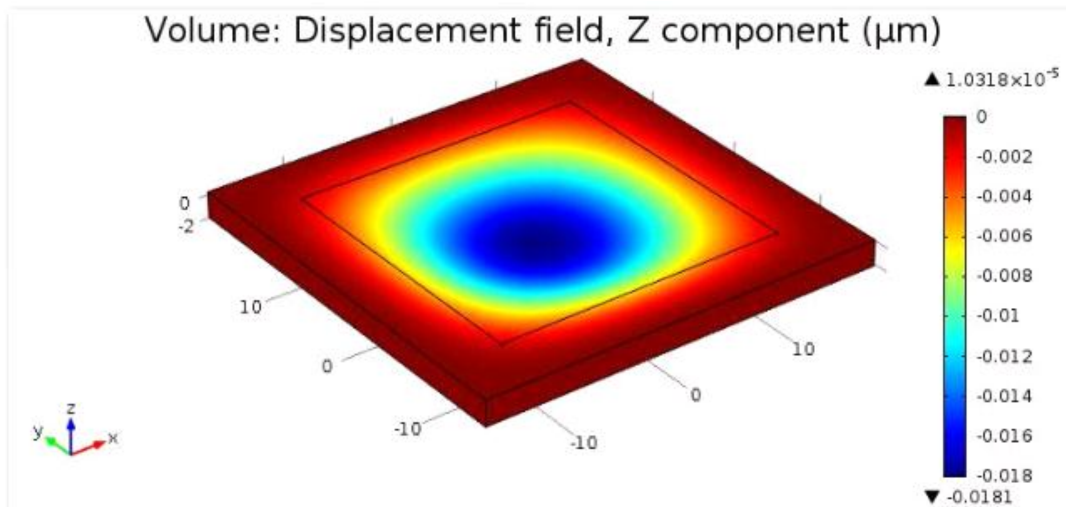


Figure 3.5 COMSOL Structural analysis of 35x35x2.2 μm membrane with 25x25 μm^2 top electrode size. 1 MPa of pressure applied to the electrode with zero displacement boundary condition on all four side walls (thickness plane).

device should be designed to operate more reliably by accounting the fabrication inaccuracies which may result in thinner dielectric thickness than expected. This can lead to lower dielectric breakdown voltages than predicted, and can be handled by choosing a design point which is shown as the shaded region shown in Figure 3.4. For example, for a 50-nm gap of 35 μm ×35 μm square 2.5 μm thick device, choosing a 100-nm-thick HfO satisfies design Curve A, whereas choosing a 120-nm HfO may be a more reliable design point such that the condition (Eqn. 3.7) is safely kept within bounds even if the fabricated device had a lower quality deposited HfO.

The true optimum point for R_η performance for g_0-x = 50-nm is when HfO t_d = 42 nm and can be seen when curve B crosses with 50-nm as the x-axis value. The true optimum point gives a marginally better R_η = 0.9 (~10% increase); however, we decided to fabricate at t_d=100-nm for a better balance between performance and stability of the HfO layer.

3.3. Fabrication of High-K Dielectric Isolation CMUTs

3.3.1 Material Characterization of ALD HfO_2

As mentioned previously, atomic layer deposition is chosen as the method for depositing hafnium oxide because: (1) low temperature processing (< 250^0C) and CMOS compatible, (2) the ability to obtain accurate thin films (controllable to ~1-2nm range), (3) the ability to batch process many wafers up to 6" (depending on the particular ALD system) with conformity in side profile coverage (up to 2000:1 aspect ratio) and uniformity in thickness and (4) low intrinsic stress of thin films from the deposition process [108]. Since atomic layer deposition is not currently considered an industrial standard processing technique, I will explain the basic concept and the specifics of the ALD system and

characterization for this thesis work. Then I present the characterization of the electrical and mechanical material properties that is relevant for the design of CMUTs.

3.3.1.1. Atomic Layer Deposition Overview

Atomic layer deposition (ALD) is usually described as similar but a subset of chemical vapor deposition (CVD), in that the final product formed is through chemical reaction of reactive species in a reaction chamber. ALD is different from CVD in the sense that it has a self-limiting chemistry when 2 pre-cursor chemical species react in an "AB-AB-AB--" reaction sequence. After the two precursors react and form a uniform layer of material, it can no-longer react until another cycle of AB precursors are introduced. The mechanism of ALD is dominated by surface reactions, and since it is performed sequentially, the two gas phase reactants are not in contact in the gas phase which limits the productions of granular films such as seen in typical CVD processes. This is what enables the ALD process to produce smooth and conformal films, one of its major advantages for deposition of thin films. A schematic of the "AB-AB" cycle is shown in Figure 3.6.

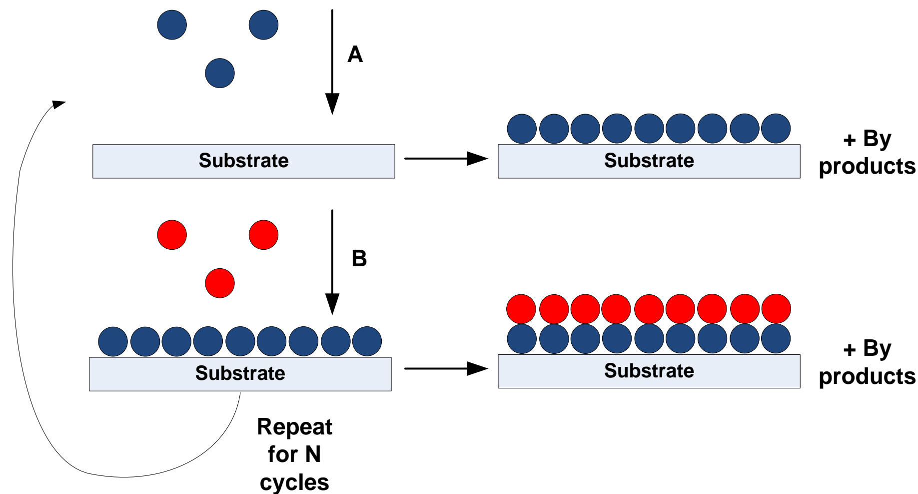


Figure 3.6 Schematic diagram showing the process of thermal ALD.

There are two common types of ALD processes: (1) Thermal ALD and (2) Plasma or Radical-enhanced ALD. Thermal ALD works very similar to the description of CVD and is based on a binary reactions such as A+B→Product+by-products. Unlike CVD, each gas phased chemical is introduced sequentially to react at the surface instead of a continuous reaction of 2 gases in CVD. Most common thermal ALD systems are binary metal oxides such as Al_2O_3, TiO_2, ZnO, ZrO, HfO_2 and Ta_2O_5. However, for some metals and semiconductor materials, it has been found difficult to deposit using a binary reaction sequence. Fortunately, Plasma ALD or Radical-enhanced ALD is used to deposit such materials and radicals or other energetic species in the plasma can help to induce reactions that are not possible with only thermal energy. Plasma ALD only require a single type of chemical to be introduced into the chamber, as the plasma source generates hydrogen radicals to reduce the metal or semi-conductor out of the pre-cursors. For this work, thermal ALD process is the focus for depositing HfO_2 as previously suggested.

The ALD deposition system used in this work is the Cambridge Nanotech Fiji F202 system. Thermal ALD process is used to deposit HfO_2 using water vapor (H_2O) as the A cycle reactant and Tetrakis[DiMethylAmino]Hafnium (TDMAHf) as B cycle reactant . The processing temperature is set to 250^0C. A schematic of the chamber and ALD system is shown in Figure 3.7. The system consists of a reaction chamber capable of handling an 8-inch plate from the load lock area. A flat and uniform heater chuck is set to 250^0C. Pre-cursor jackets are uniformly heated to 75^0C to increase volatility for TDMAHf precursor and consistent head vapor pressure inside the packaged canister. The vapor pressure of TDMAHf is ~1 torr at 65^0C, with a melting point of ~30^0C, flash point ~43^0C and boiling point ~85^0C. It is important not to heat the precursor bottle above 80^0C as it will degrade

the precursor chemical and breakdown it's chemical composition. Precursor lines are heated to 150^0C to energize the gaseous precursor and increase volatility. Argon carrier gas is mixed with the volatile precursor and injected into the reaction chamber via laminar flow control towards the substrate which is on top of the heated chuck. Waste and by-product from the reaction is purged through the cone filters where it will condense on a gridded shield vapor trap downstream from the cone.

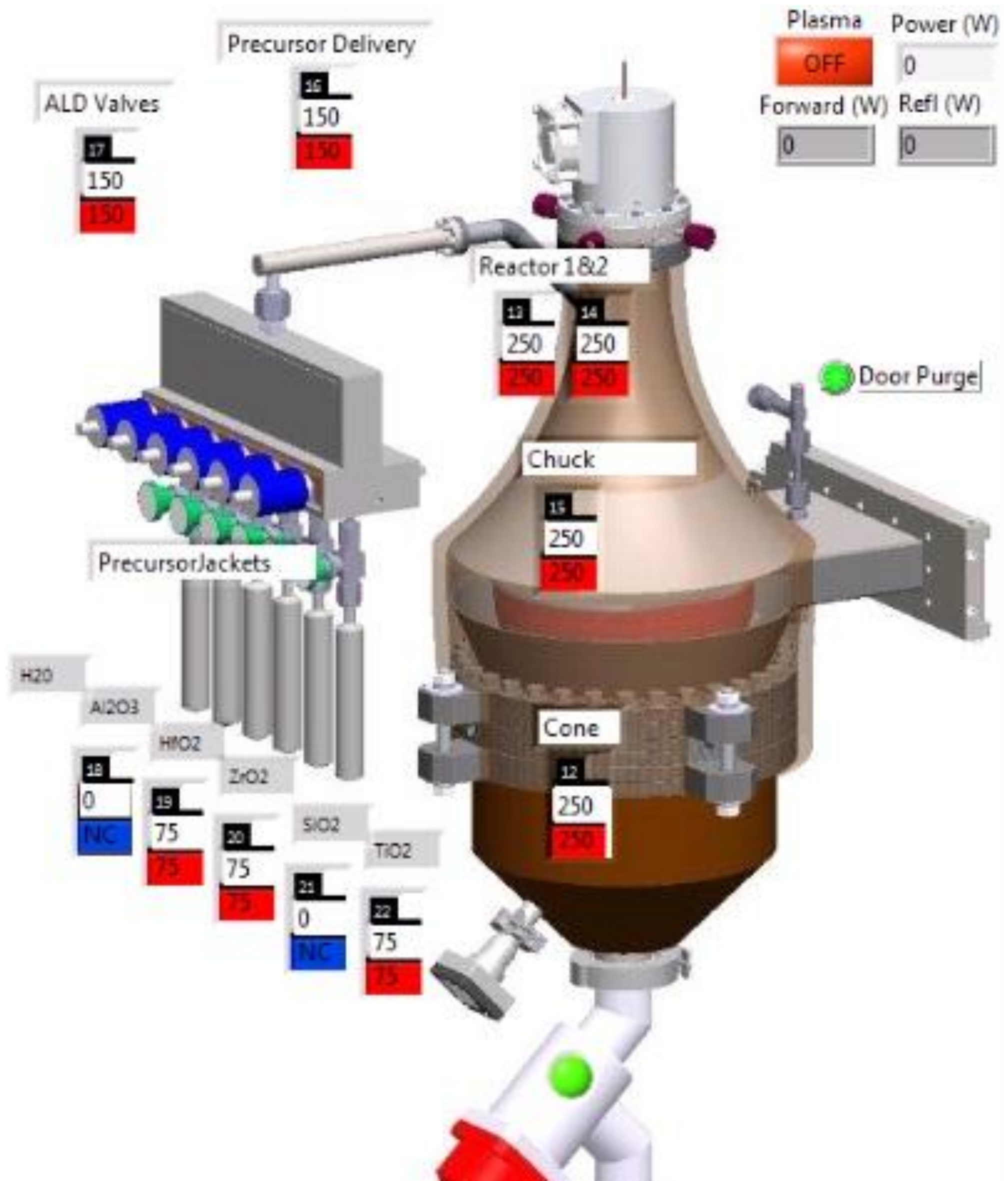


Figure 3.7 Schematic diagram showing the Cambridge Nanotech Fiji F202 system.

Another important design to this system are the ultrahigh cycle life (>20M cycles) and high-speed actuation valves that can control open-close duration to as low as 20 ms (www.swagelok.com). Typically these valves have a thermal isolation coupling housing to separate the heat transfer between pneumatic actuator assembly to the body which gives a more uniform temperature distribution and minimizes cold or hot spots in the fluid flow path.

The parameters optimized for this work is summarized in Table 3.1

Table 3.1 ALD HfO_2 Recipe Parameters

Parameter	**Value**
H_2O Pulse Time	0.6s
H_2O Pulse Pressure Peaks	100mTorr
Purge Time	10s
TDMAHf Pulse Time	0.25s
TDMAHf Pulse Pressure Peaks	20mTorr
Purge Time	10s
Substrate Temperature	250^oC
Pre-cursor Jacket Temperature	75 ^oC

For long deposition cycles or thicknesses (>30nm), it is typically separated into multiple deposition cycles of no more than 300 cycles. It is observed experimentally that the pulse heights of the HfO_2 starts to decrease after a long period of deposition. This means that not enough precursor is being introduced into the chamber and can be depleted quickly before all of the substrate surface has a chance to react and form HfO_2 layers. This means

the uniformity of the thickness of the growth will be affected. This is hypothesized to be due to a non-constant head pressure in the TDMAHf canister and letting pausing the process will allow the head pressure to thermal dynamically stabilize again. Although this method alleviates the pulse height issue, it is not ideal since the substrate will have to be taken out of the chamber and can face potential contamination and oxidation when in contact with the atmosphere. A sample of the pressure spikes can be seen from Figure 3.8.

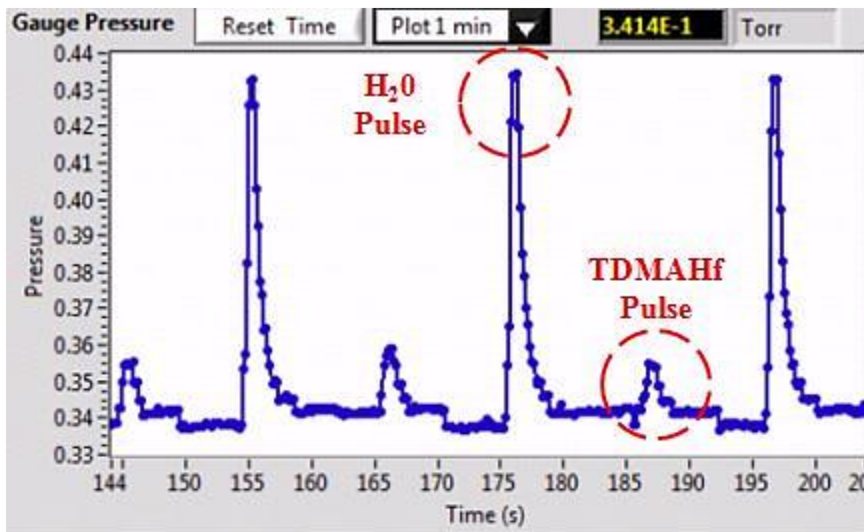


Figure 3.8 Time vs. pressure of ALD precursor pulses detected from the Cambridge Nanotech Fiji F202 system valves.

3.3.1.2. Atomic Layer Deposition Rate Characterization

Before utilizing ALD HfO_2 for fabrication of CMUT devices, the deposition rate must be first characterized to ensure an accurate amount of the film is deposited for the dielectric insulation layer. As previously mentioned, the correct thickness of the HfO_2 means that a high sensitivity can be achieved while withstanding the dielectric breakdown strength when the DC voltage approaches $V_{COLLAPSE}$.

A wafer is broken into 4 quarter pieces and each piece has 1200Å of thin metal deposited using the Unifilm© DC sputterer. The last piece is the control piece and left as bare Si with just the 1-2 nm of native SiO_2. Then each of these piece are put through the deposition process and subsequently measured the thickness of the films using Woollam M-2000 ellipsometer. The optical recipes built for the samples with the metal layer took into account the base reflectivity and refraction of light on those metal surfaces as deposited. Figure 3.9 shows the cycles deposited vs. the actual thickness measured for the various metals and silicon surface. The deposition calculated from a cumulative 500 cycles are tabulated in Table 3.2.

Table 3.2 Deposition Rates of HfO_2 on Various Surfaces

Surface Material	**Deposition Rate (Å/cycle)**
Copper (Cu)	1.27
Chromium (Cr)	1.31
Aluminum (AlSi 2%)	1.27
Silicon (Si <100>)	1.13

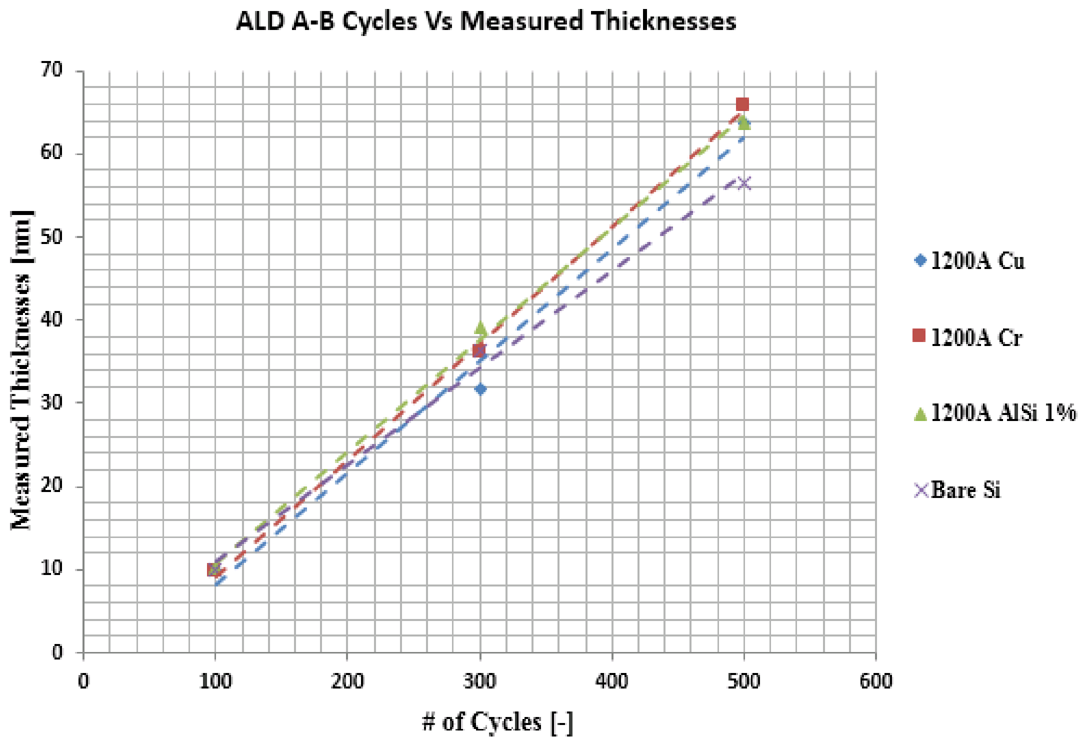


Figure 3.9 Deposited thickness of thermal ALD HfO_2 on a variety of metals and silicon surface

Since the proposed fabrication of CMUT devices described later in this work have copper sacrificial material. The reminder of the material characterization will be based on HfO_2 growing on copper surfaces. The deposition rate of 1.13Å/cycle on silicon is comparable to literature value of 1.15Å/cycle deposited at 250^0C [109]. The slightly higher values for deposition rate observed on the metal surfaces maybe due to surface roughness increased when introduced to the higher temperature and subsequently affecting the reflectivity of the surface. Thus it is further advised that all substrates with metal surfaces should be placed onto the substrate holder as close to room temperature as possible to minimize the oxidation of the metal surfaces.

Further investigation of HfO_2 deposition on copper reveals that there is a clear nucleation delay effect. It can be seen from Figure 3.10 that it can take up to 40 cycles before nucleation begins on a bare copper sample. However, with a short 25s, 250W, O_2 plasma treatment from a standard RIE system, the nucleation begins almost immediately. It is theorized that the plasma helped to activate the surface sites on the copper and become more attractive for hydroxyl groups (OH) to bond to when H_2O is pulsed into the chamber. Similar nucleation delay behavior is observed by Tao *et al.* [110] on copper and can be used as selective ALD deposition up to ~3-5 nm in this particular case. For films with a target thickness of 100nm, the nucleation delay if not factored into the estimation can lead up to a -5% error in the final thickness deposited. To better control the deposition rate and

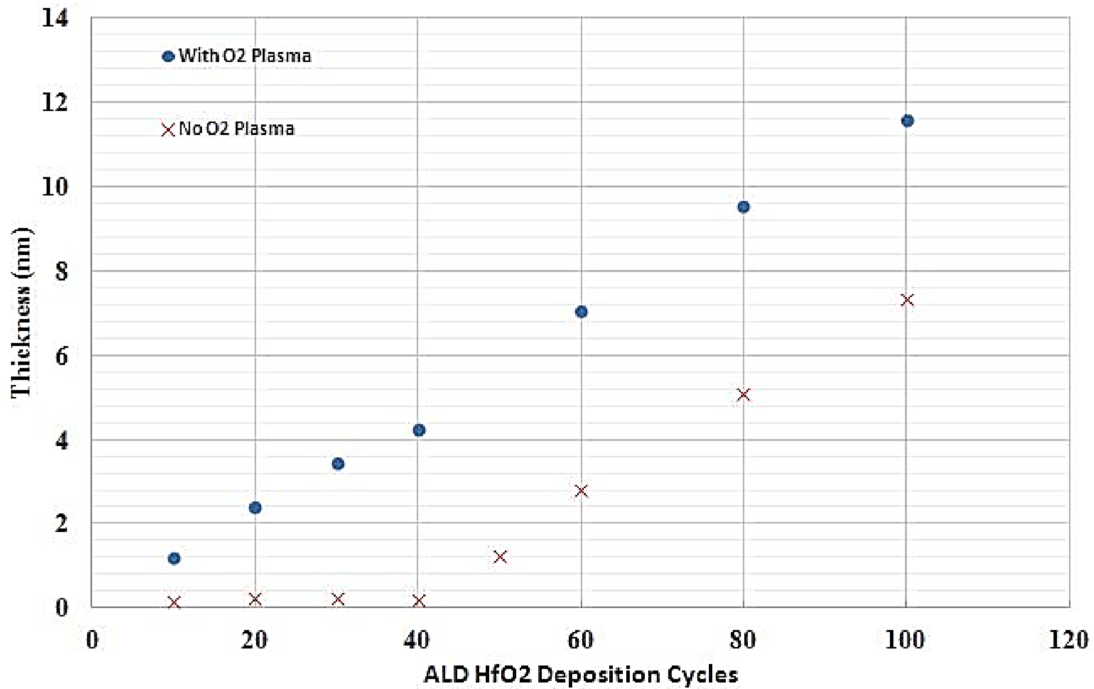


Figure 3.10 Deposited thickness of thermal ALD HfO_2 on copper with and without plasma pre-treatment

accuracy of the thickness of the thin film, a plasma treatment to activate the metal surface is always suggested. It may be possible that in plasma ALD, this activation can be done in-situ and do not need the use of a RIE to complete this step. However, one must take care to not create extra roughness through oxidation during the plasma treatment and keep the RF power low. Similarly, remote plasma ALD system such as the Cambridge Nanotech Fiji 202 is preferred over direct plasma systems in that the plasma damage to the substrate surface is kept to a minimum.

3.3.1.3. HfO_2 Insulation Layer Uniformity and Stress Characterization

The uniformity of the ALD is generally considered very good for thin films (10-100 nm) compared to other deposition methods such as RF sputtering or DC sputtering. This is heavily dependent on tooling parameters and how tightly the pressure and temperature of the chuck, precursor jackets, delivery lines and chamber walls are controlled.

In Figure 3.11, the uniformity of HfO_2 is measured over an Φ=100 mm wafer with 29 points for 900 cycles of deposition using the Woollam M200 Ellipsometer. The range is 8.11 nm across the wafer and it can be seen that the right side of the wafer has thickness values closer to the ideal deposition rate measured earlier. The average thickness across the wafer is 104 nm with a 2.4 nm standard deviation (2.3% variation). The reason for the thicker region on the left hand side turns out to be a defective design in the Cambridge Nanotech Fiji F202 tool where the thermal insulation in the dome section is not ideal. A lower temperature on the left hand side of the dome caused a higher rate of condensed material on the side walls of the chamber which can outgas back into the reaction or and deposit on to the left hand side of the wafer.

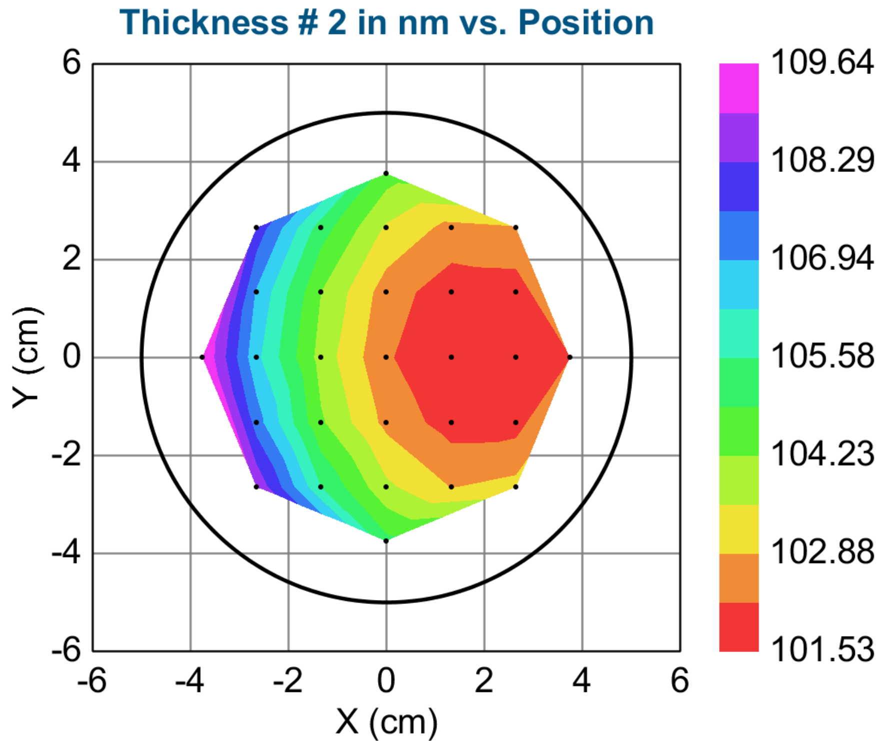


Figure 3.11 Uniformity measurement of HfO_2 on Si with ellipsometry.

Intrinsically, the deposition process of ALD does not introduce any stress in the HfO_2 layer [95], [96]; however, due to thermal mismatch (CTE) between the HfO_2 and the bulk silicon substrate stress is present. BowOptic 208 tool was used to measure the curvature of the wafer before and after 100nm deposition of ALD HfO_2 and Stoney's equation was used in the built-in software to calculate the stress based on the material properties of the thin-film and silicon substrate and the change in measured radius of curvature. An average tensile stress of +700MPa was measured for a 100nm film HfO_2 deposited at 250^0C on bulk silicon. Depending on the design of the CMUT this stress may or may not affect the overall curvature of the membrane after fabrication. The stress in the PECVD Si_xN_y is +90MPa; however, if the thickness of the SiN layer is dominant compared to HfO, then the bending effect due to thin-film stress is still mainly controlled by the SiN

layer. For the geometry that is later described in Table 3.4, that is exactly the case where the thickness of SiN is ~20 times larger than that of the HfO layer. For a first order approximation, the stiffness of the square membrane is proportional to the thickness (h) to the third power, which again supports the argument that HfO stress will minimally affect the curvature of the membrane if SiN thickness is dominant in the design. For the work described in this chapter, the fabricated device with HfO and its final membrane topography is scanned with a Veeco Dimension 3100 AFM.

Figure 3.12 shows a maximum dip of <5 nm in the middle of the membrane which is also verified in COMSOL simulation by applying pre-stress conditions to the membrane materials (HfO + SiN). COMSOL modeling showed a maximum of 6 nm dip in the center of the membrane based on the stress values reported.

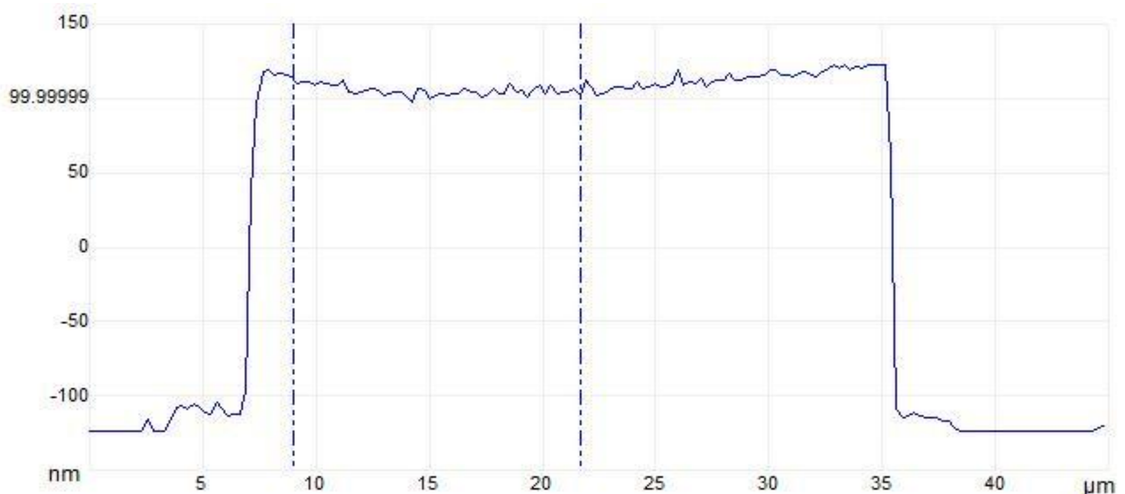


Figure 3.12 Membrane profile scanned with AFM after the complete fabrication of the CMUT device (after gap is formed and the membrane is at the final thickness with the sealed vacuum).

3.3.1.4. Material Properties Characterization

For accurate prediction and simulation of the CMUTs using high-κ material such as HfO_2, κ and E_{BD} should be experimentally characterized. A good prediction of E_{BD} is critical to achieve electrical reliability and the thinnest possible thickness for the dielectric layer. To calculate κ and measure E_{BD} of the HfO thin film, test capacitors with copper bottom and aluminum top electrodes were fabricated. Copper was chosen for the bottom electrode due to the material's low resistivity and the process similarity to the growth of HfO on copper sacrificial layer during the CMUT fabrication process [111]. Since the nucleation rate of HfO may differ on various material surfaces, affecting its thickness per cycle of deposition [110], the HfO film on top of a copper bottom electrode was characterized to best replicate the surface conditions used in the CMUT fabrication process. Both top and bottom electrodes are 1300 Å and a 50-nm HfO dielectric layer was deposited using Cambridge Nanotech Fiji F202 system at 250°C. The thickness of the ALD film was measured with a Woollam M-2000 ellipsometer, with a recipe that was calibrated for the specific copper layer that the HfO was deposited on. A mean squared error (MSE) of 27.5 Å and an average refractive index of 2.06 was measured for the HfO thin film on top of sputtered copper which is close to literature values [112]. Fluorine based Reactive Ion Etching (RIE) recipe (discussed in 3.3.2) is used to etch open the area over the bottom electrode copper bond pads used for external electrical characterization.

The capacitance of the test capacitor, measured using a standard probe station and Agilent B1500 Semiconductor Analyzer, is shown in Table 3.3 where other capacitor parameters are also summarized. The average capacitance value over 10 capacitor measurements were used to calculate the average dielectric constant of the HfO based on 50-nm thickness and designed capacitor electrode surface area. The variation in

capacitance measured in Figure 3.13 can be due to the non-uniformity of the actual HfO thickness deposited. A typical C-V measurement was obtained by sweeping between -15 V to +15 V with a 0.3 V step. The AC voltage level applied was at 0.25 V while the frequency of the AC signal was held at 100 kHz. All measurements were carried out at room temperature.

Table 3.3 Test Capacitor Parameters and Average κ value

Parameter	**Value**
Electrode Area	3.469e-7 m^2
HfO_2 film thickness	50 nm
Measured Capacitance	0.86 - 1.1 nF
κ	16 (+/-2)
3σ *(for* κ*)*	2

Subsequently the dielectric breakdown of the HfO deposited at 250°C was also measured and the corresponding I-V curve is shown in Figure 3.14. The measured E_{BD} is ~3.9 +/- 0.1 MV/cm (3 sigma variation) as shown in Figure 3.14 for one example measurement where the measured V_{BD} is 20.5 V for a 50-nm film. The retrace shows that breakdown phenomenon has occurred on the thin dielectric film and it behaves like a resistor instead of a capacitor.

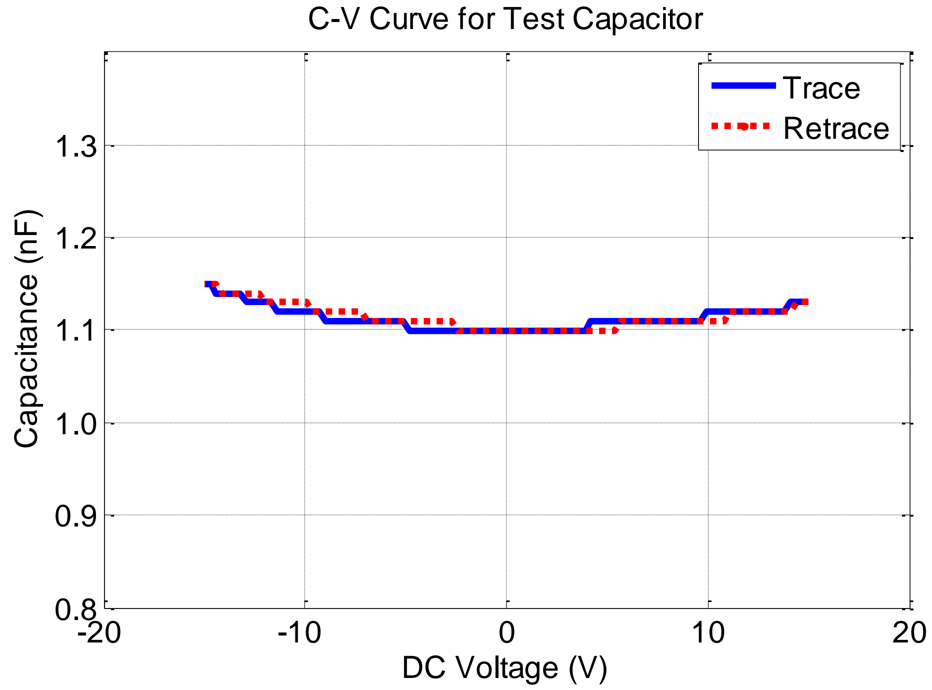


Figure 3.13 C-V curve for test capacitor with 50 nm of ALD HfO_2 as dielectric layer.

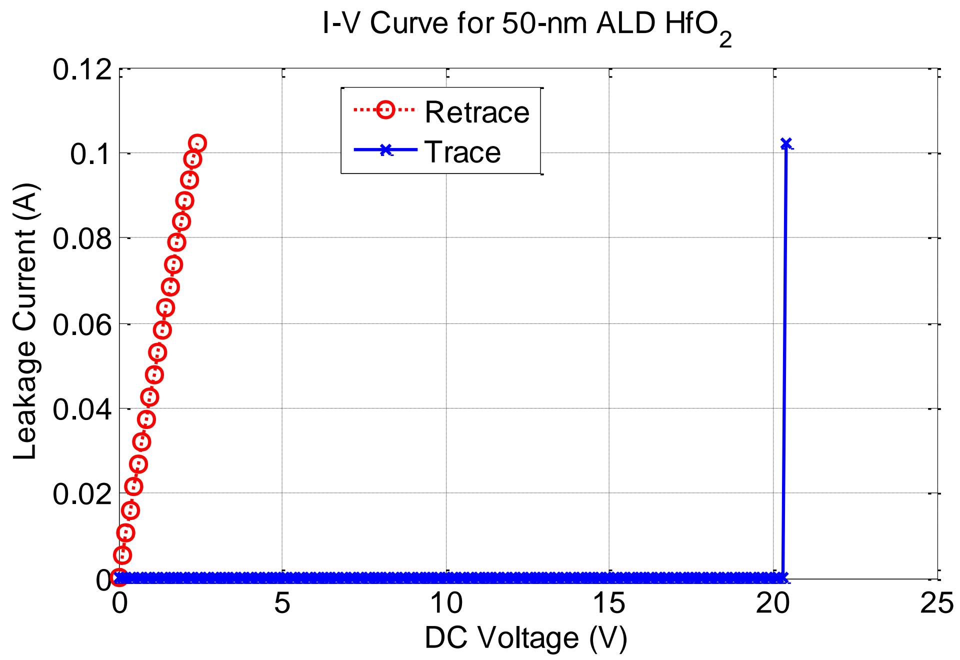


Figure 3.14 I-V curve for test capacitor with 50 nm of HfO as dielectric layer.

3.3.2 Fabrication of ALD HfO_2 Insulation CMUTs on Silicon Substrate

In this section, I will first describe the general steps for fabricating ALD HfO_2 insulation CMUTs on silicon. Then I will give details on the fabrication of CMUT-on-CMOS monolithic integration with the newly developed high-κ insulation process as well as the reliability design considerations.

The fabrication method used in this investigation is similar to that of the low temperature silicon nitride process previously described in Knight *et al* [71] and will be summarized in this this thesis along with the new steps. The novel steps including the ALD HfO_2 insulation layer and using a copper sacrificial layer, will be discussed in greater details, are schematically described in the CMUT fabrication process flow shown in Figure 3.15.

Starting with a 4” <100> silicon wafer, a 3 μm thermal oxide is grown for passivation from the substrate. A 120 nm of chromium is then sputtered and patterned to form the bottom electrode of the CMUT. After this step, 50 nm of copper is sputtered and patterned for the sacrificial layer (for the vacuum gap layer). Both electrodes are sputtered with the Unifilm DC Sputterer and achieved high thickness conformity over the entire wafer. The gap thickness and its uniformity are critical since it affects the CMUT device performance, such as collapse voltage and pressure output for the given input voltage. Both layers of patterning were achieved by using Shipley SPR 1813 photoresist. The chromium is wet etched via CR-7S Chromium etchant and the copper by Copper APS 100 diluted at 1:60 with deionized (DI) water. Both etchants etched in the range of 4-8 Å/s at room temperature. Chromium was chosen as the bottom electrode because the copper etchant

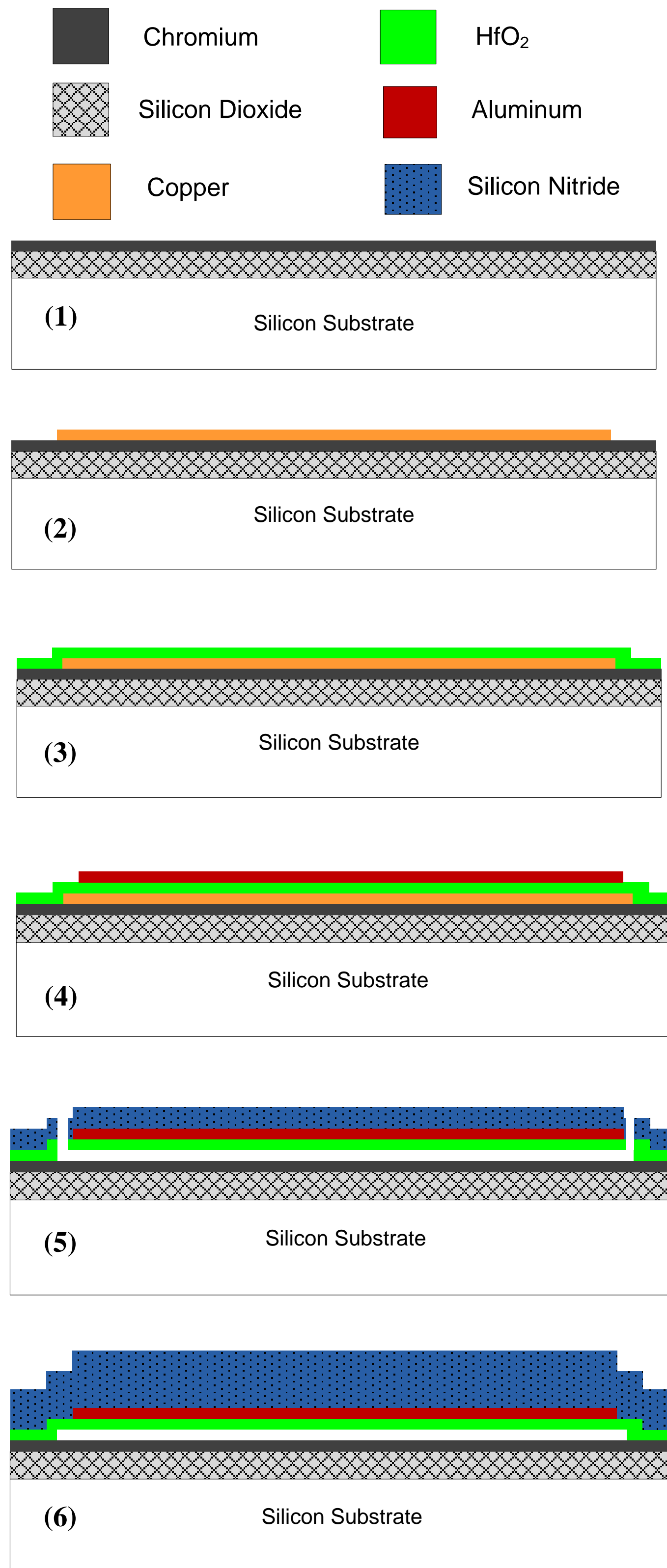


Figure 3.15 Fabrication process s flow with hafnium oxide insulation layer.

does not etch chromium, and thus is suitable for selectivity when patterning the sacrificial layer without the need to introduce an extra dielectric passivation layer in between. Then, a 100-nm layer of thermal HfO is grown uniformly across the surface of the substrate at 250 °C to form the top dielectric insulation. The thickness of this insulation is designed to operate near $V_{COLLAPSE}$ without exceeding the threshold of V_{BD} as discussed in Section 3.2.4. For the HfO CMUT device, operating at ~15 MHz center frequency, the thickness of the insulation is designed as 100 nm. This is not the optimum thickness for this particular device configuration, however it is also a safe thickness for other devices that work higher frequencies fabricated on the same wafer. The ALD recipe parameters used in HfO deposition are summarized in Table 3.1. The precursor used in this study is Tetrakis (Dimethylamido) hafnium (IV) (TDMAHf) along with Cambridge Nanotech's Fiji F202 ALD system.

In order to minimize the oxidation of the copper sacrificial layer which can introduce additional surface roughness, the substrate is loaded onto the ALD chuck at 25-35°C in the load lock area and subsequently reduced to a vacuum pressure of 0.5 Torr range before entering the main ALD deposition chamber. Due to the vacuum environment inside the ALD chamber, oxidation rate is very slow and negligible even at 250 °C. If a significant amount of oxidation occurred, then it would mean there is a large enough of a leak in the vacuum chamber to allow a significant amount of oxygen level to exist in the chamber. The average growth rate observed is 1.15 Å/cycle and an average of 20-40 cycles is needed before nucleation of the first layer of hydroxyl group forms to create the first molecular layer of HfO on top of the copper sacrificial layer. To control this slight delay in nucleation, a low powered plasma pre-treatment can be used to activate the copper surface for giving

more energy to form a bond to the hydroxyl group from the water vapor during A-cycle of the ALD process. If the nucleation delay or thickness is an acceptable error in the overall thickness of the design, then it is acceptable to overestimate by 20-40 cycles from the calculated required cycles from the average deposition rate. For example, if 100 nm HfO thickness was the target thickness, then ~870 cycles is required based on 1.15 Å/cycle deposition rate. Accounting for the worst case scenario of nucleation delay of 40 cycles, one would actually set the ALD tool to deposit at 910 cycles to achieve 100nm thickness.

To form the top electrode, a 300 nm of AlSi 1% is evaporated and patterned through lift-off. AlSi is chosen due to its good adhesion, relatively high electrical conductivity and linear thermal coefficient similar to that of copper ($22x10^{-6}$/°C for AlSi versus $16.7x10^{-6}$/°C for copper). The similarity in coefficient of thermal expansion (CTE) between the aluminum and copper helps with reducing thin film stress and peeling of the top electrode. After depositing 1 μm of SiN for the membrane formation, small release holes are drilled via RIE to the copper sacrificial layer to allow copper etchant APS 100 to come in for a wet release. A separate sulfur hexafluoride (SF_6) chemistry was also used to etch the HfO layer compared to the standard CHF_3 chemistry used to etch SiN. Etching rates of 5 nm/min and 58 nm/min are observed for the release hole etching in HfO and SiN, respectively. After the release, the wafer is placed back into the PECVD for sealing at 900 mTorr and further thickening to a desired 2.2 μm total thickness. A final step of opening the electrical bond pad connections for testing is needed via RIE. The test array geometry parameters used to compare the sensitivity performance of SiN and HfO insulation layers are summarized in Table 3.4.

Table 3.4 Test Array Geometry Parameters

Parameter	Value
Membrane Size	35x35 μm
Top Electrode Size	25x25 μm
Vacuum Gap	50 nm
Si_xN_y Membrane Thickness	2.0-2.1 μm
HfO_2 Isolation Thickness	100 nm
Si_xN_y Isolation Thickness	200 nm
No. of Membranes per element	4
No. of Elements per device	4
Total No. of Membrane per device	16

The fabrication method described above is used to fabricate the test arrays used in the next section for performance comparison. The silicon nitride insulation layer test device wafer was fabricated in the same way, except changing the ALD HfO_2 process to PECVD Si_xN_y. Note that the thickness of the SiN is chosen for 200 nm due to possible pin-hole defects from the PECVD deposition process being problematic if the thickness is reduced any further. Pin-hole defects not only decreases the physical density but also changes the dielectric properties of the thin-film. This is yet another advantage of using the ALD deposition process, since it can give conformal, high quality and "pin-hole free" deposition of thin film dielectrics.

3.3.3 CMUT Characterization and Performance Comparison

To compare the performance of CMUTs with HfO and SiN, insulation layers, CMUT elements with identical geometry and 50-nm vacuum gap were fabricated by the method described in Section 3.3. The only difference between these wafers is the method followed for the formation of dielectric insulation. The HfO and SiN thicknesses are 100 nm and 200 nm, respectively. The device geometry for the comparing test arrays are summarized in Table 3.4 and the fabricated CMUT devices are shown in Figure 3.16.

Both devices are diced from the main substrates and secured side by side to the same PCB testing board for wirebonding of the bond pad connections. A 3-µm layer of parylene-C is coated over the devices, exposed wirebonds and PCB traces and submerged for acoustical characterization in water. With the 2 devices side by side on the same PCB, physical setup variations such as alignment changes to the hydrophone are minimized to achieve a reliable comparison study.

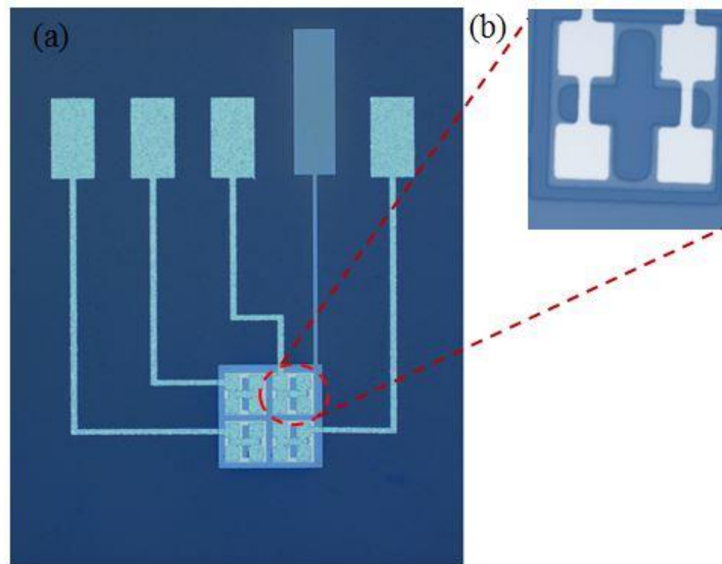


Figure 3.16 (a) A Micrograph of the test CMUT device. Both test cases are identical in lateral geometry size, only one test device is shown above. There are 4 elements per device (b) Close-up view of 1 element with 4 membranes

3.3.3.1. Transmit Performance Characterization and Comparison

Both devices were measured in the same setup using the same pulser. A 28-ns unipolar pulse generated by custom design pulser excited the transducers and the transmitted pressure was measured with a hydrophone (HGL0085, ONDA™). The experimental setup can be seen in Figure 3.17.

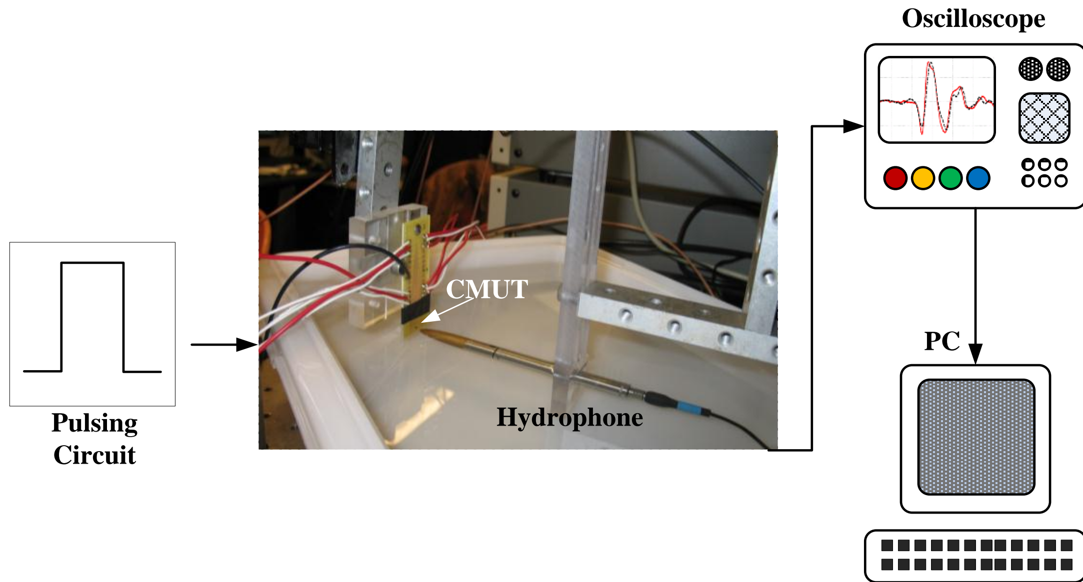


Figure 3.17 Schematic of experimental setup for CMUT transmit and hydrophone receive (pitch-catch mode).

The pulse amplitudes were increased to a point which maximizes the output peak-to-peak pressure observed by the hydrophone, meaning the full gap swing of the membrane. The spectra of the received signals were also monitored to make sure that the devices operated in the non-collapsed mode. No DC bias was applied with this short pulse to achieve maximum output pressure with full-gap swing [58]. Pulse amplitudes of 32 V and 60 V were found to reach maximum output pressure for HfO and SiN isolation devices respectively. Note that the collapse voltages of the devices were 21V and 42V for HfO and SiN isolation devices respectively. Therefore, the devices needed to be driven ~50% higher

than their collapse voltages for full swing operation with this particular pulse width. The hydrophone outputs from the devices at the maximum pressure points are shown in Figure 3.18. The pressure output signals are very similar in shape as well as amplitude meaning that both devices are fabricated with good uniformity and could be used for a fair performance comparison. The same peak output pressure measured on the hydrophone

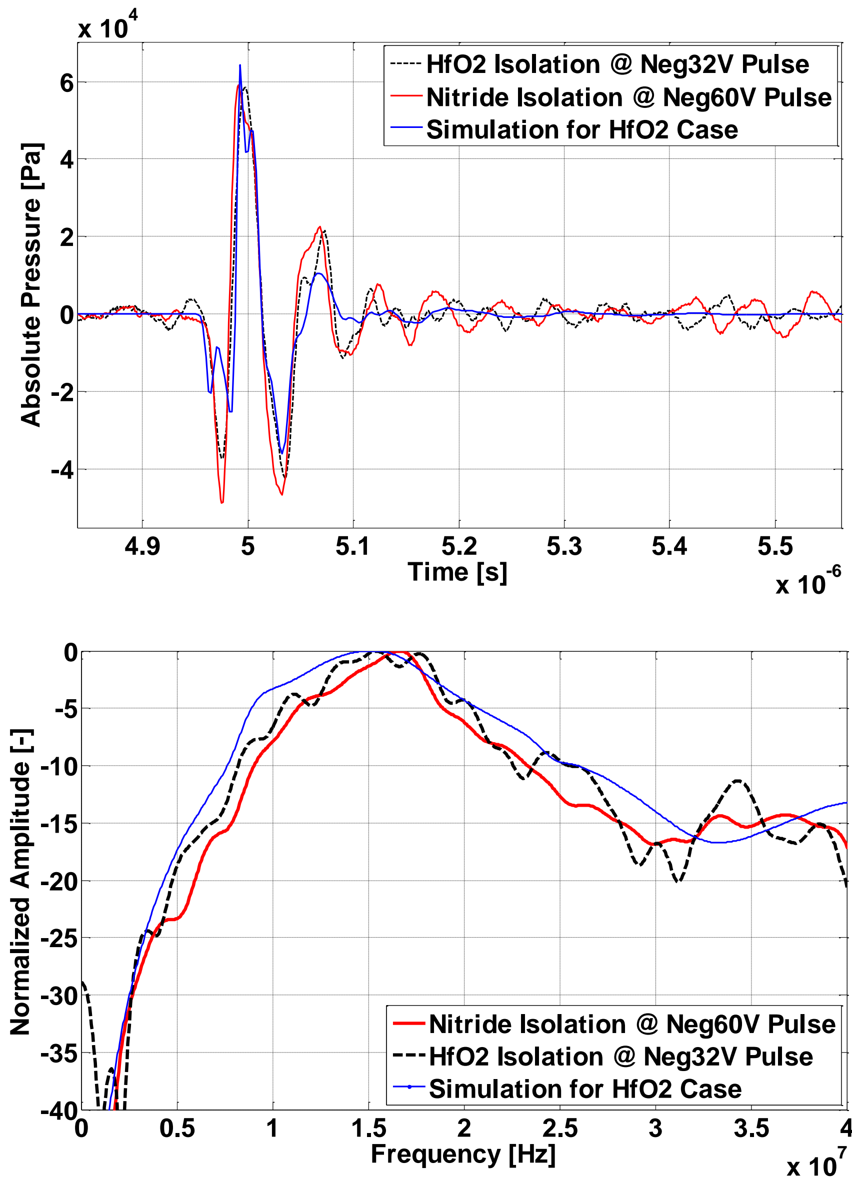


Figure 3.18 (top) Transient pressure waveforms from test devices, (bottom) Frequency response comparison of test devices showing fabrication uniformity that is suitable for a fair performance comparison.

shows that both devices achieved full gap swing. The frequency responses are similar with a center frequency of 16.5 MHz.

The detailed comparison of the transmit mode performance is depicted in Figure 3.19, which plots the hydrophone output voltage as a function of the pulse amplitude. The nonlinear dependence of the output pressure to input pulse amplitude is observed. As expected, both devices reach the same maximum pressure which is limited by the vacuum gap thickness. However, the CMUT with 100 nm HfO layer reaches maximum pressure with 32V pulse whereas a 60V pulse is required for the CMUT with 200-nm SiN layer. Therefore, there is ~2 times improvement in transmit sensitivity with no DC bias case. This is in reasonable agreement with the simple parallel plate model prediction in Figure 3.3.

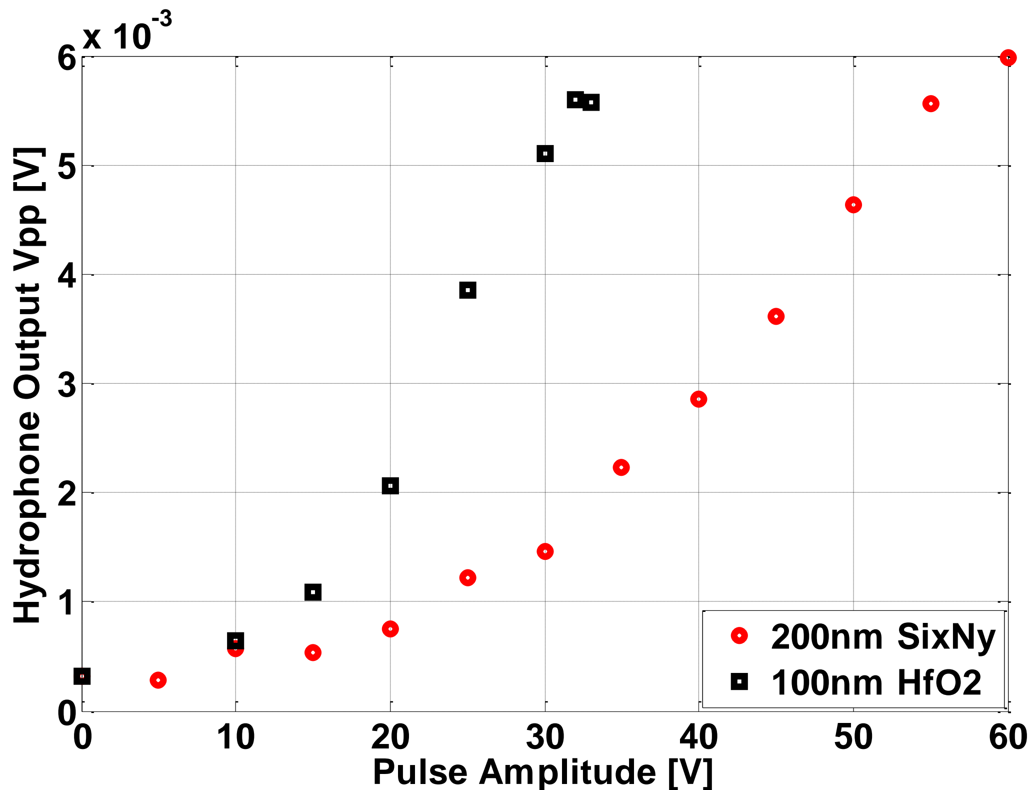


Figure 3.19 Experimental hydrophone data comparing the Tx between the two types CMUTs. HfO_2 device can achieve the same maximum pressure output with half the input voltage compared to Si_xN_y.

For validation of the experiment, a large signal model for CMUT was used. Quarter symmetry was implemented in the simulation and the geometry parameters listed in Table 3.4 for the HfO_2 insulation layer case was used. The input signal of $V_{PULSE} = 32V$ with a 28ns square pulse was applied to all membrane electrodes. In Figure 3.18, the simulation shows good match in both time and frequency response. It can be noted that the hydrophone output was converted to absolute pressure through a calibration constant. The peak to peak pressure amplitudes match to within 5%. It can also be noted that the simulated bandwidth is on average wider than the experimental results.

3.3.3.2. Receive Performance Characterization and Comparison

To compare receive performance of CMUT elements, a 15-MHz piezoelectric transducer was used as a transmitter, seen in Figure 3.20. The CMUT elements were connected to a Panametrics Pulser/Receive (Model 5072R, 500 Ω input impedance) using a coaxial cable with 60 pF capacitance (180 Ω impedance magnitude at 15 MHz). We note that the impedance magnitude of both SiN and HfO CMUTs due to its active capacitance and parasitic capacitances from wirebonding are greater than 5 kΩ. The effective receiver impedance magnitude resulting from the receiver input, and parasitics due to the cable and wirebonding is ~130 Ω. This is a low impedance termination for the CMUT, as considered in the simplistic calculations shown here, compared to an open circuit termination.

Both CMUT elements were centered with respect to the piezoelectric transducer before the data is collected for each CMUT element and absolute transmitter-receiver distances were kept the same between measurements. Figure 3.21 shows the received signal amplitude while the DC bias voltage is varied from 0 V up to each CMUT's collapse voltage.

Two important conclusions can be made about the receive performance. First, the 100-nm HfO isolation device has half the collapse voltage of the 200-nm SiN device. This is desirable since this will allow operation of the CMUT close to collapse at lower voltages. Second, the maximum receive signal from the HfO device is ~2.2 times that of the SiN device at collapse, indicating an absolute gain in receive sensitivity. When normalized to the collapse voltage of each CMUT, there is about 4 times improvement in the receiver performance. This is in reasonable agreement with Figure 3.4, considering that the gap is

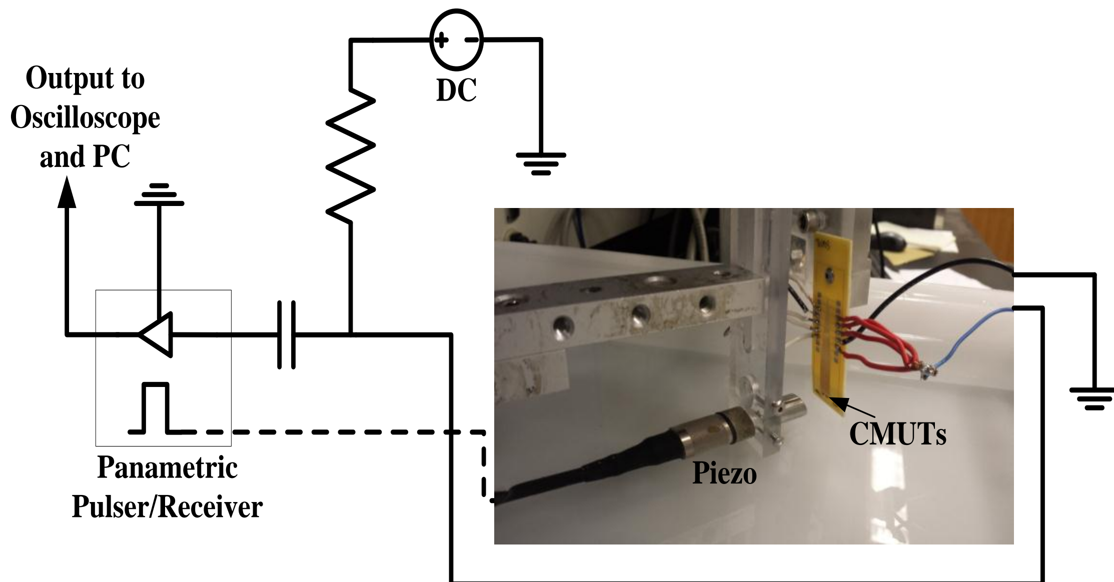


Figure 3.20 Schematic of experimental setup for Piezo transmit and CMUT receive (pitch-catch mode).

reduced and there is significant membrane curvature profile very close to membrane collapse.

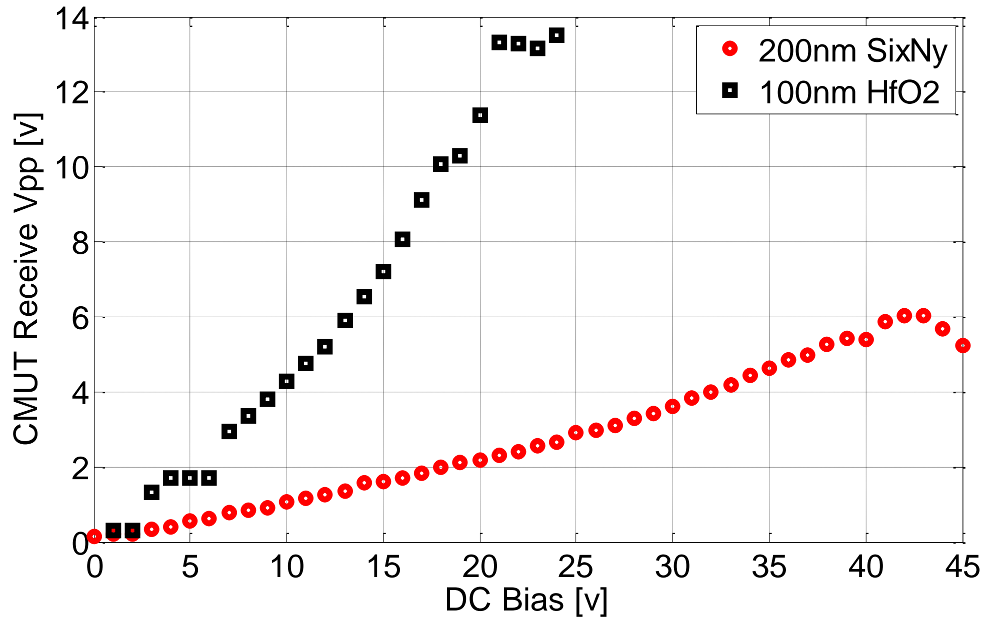


Figure 3.21 Experimental CMUT receive data comparing the Rx sensitivity of the 2 CMUTs. HfO device can achieve ~2.2 times the receive voltage using half the DC voltage compared to SiN.

CHAPTER 4. CMUT-on-CMOS WITH HIGH-K INSULATION LAYER INTEGRATION

4.1. Fabrication of High-K Dielectric Isolation CMUT-on-CMOS

As motivated in Chapter 1, the advantage of CMUT technology is in its ability to easily integrate with CMOS or IC so that the front-end receiver circuitry can be as close to the tip of the catheter and to the output of the CMUT as possible to reduce parasitic capacitances (C_p). This is especially important for catheter based volumetric imaging arrays when element sizes and capacitances are very small (on the order of 1 pF or less). In order to have the largest signal-to-noise (SNR), it is important to have (1) the largest signal possible from the receiving CMUT for a reflected pressure wave or (2) a small noise level.

It has already been shown in the IC design by Gurun *et al.* [60] that the TIA noise is actually below the noise floor of the thermal mechanical noise or Brownian noise of the CMUT element itself. Thus the remaining goal is to increase the signal (current) to the TIA amplifier input. By directly fabricating CMUTs on top of the CMOS instead of flip-chip bonding two separate chips (as already mentioned in Chapter 2's comparison on integration techniques) enables the further reduction of parasitic capacitance which for the case of a low input impedance amplifier or a TIA is highly desirable. This is because the bigger the parasitic capacitance, the more the output current from the receiving CMUT will flow into C_p which has sources that include the connection pads, wirebonds, TSVs or micro-solder joints. Thus with high C_p, not all of the output current of the receiving CMUT will flow into the input of the TIA, reducing the overall SNR of the CMUT receive RF signal. A direct comparison for parasitic capacitances is made between wirebonding case Vs. direct CMOS integration and show in Table 4.1.

Table 4.1 Array Element Connection Capacitance Comparison

Parameter	DRA Wirebond Connections	DRA CMOS Connections
Receiver Element (CMUT)	114 fF	114 fF
Connection Line	42 fF	42 fF
Bond Pad	239 fF	N/A
Wirebond	2pF	N/A
Total C_p	2.281 pF	11fF
Parasitic to CMUT Capacitance Ratio	20:1	1:11

The CMUT-on-CMOS integration proposed in this work strikes a good balance between optimizing the ~1.3 mm diameter real estate space for IVUS, minimizing the parasitic capacitance and relative ease of fabrication and final packaging considerations. It will be noted that the biggest fabrication constraint for directly processing on top of the CMOS substrate is temperature. Temperatures above 400^0C for more than one hour can cause additional diffusion of dopants inside of the transistors and temperatures above 600^0C is dangerously close to melting aluminum IC traces. For the reliability of our devices we set the maximum operating temperature for any process to not exceed 250^0C.

4.1.1. CMOS Wafer Substrate

Our CMUT-on-CMOS integration first begins with custom made 200 mm (8 inch) diameter CMOS electronics fabricated through Taiwan Semiconductor Manufacturing Company's (TSMC) 0.35 μm process. This wafer has 48 repeated square blocks with repeating IC patterns per die. Each individual square block has a variety of designs with

multiplexers, TIAS and buffers for different CMUT designs (low and high frequency). On chip NMOS pulsar electronics are capable of +25V unipolar pulse amplitude are also designed and fabricated at the IC level.

These wafer are subsequently grinded to 300-400 µm thickness with mirror polished surface finish on the back side and diced into 6 useable rectangular blocks by Corwil Technologies Ltd. shown in Figure 4.1. These blocks are roughly 4 cm x 7 cm (3 x

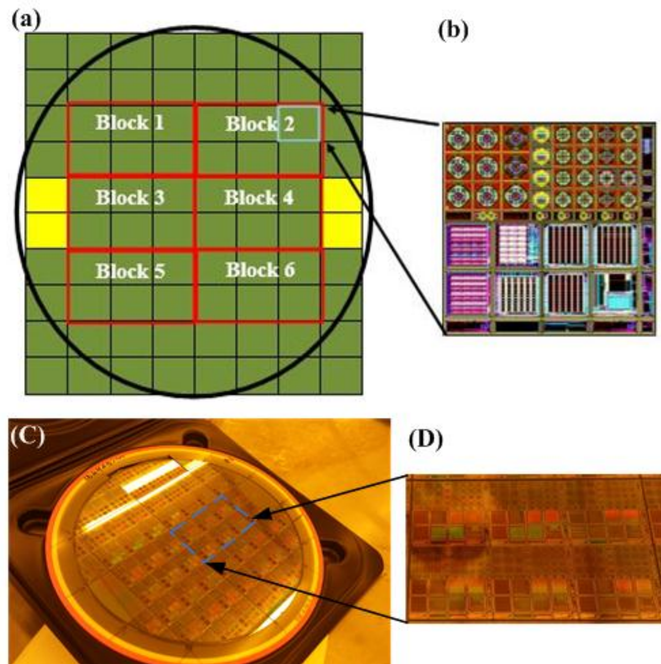


Figure 4.1 (a) Schematic of 6 functional blocks on the 200 mm CMOS wafer, (b) 1 out of the 6 dies per block, (c) The full 200 mm CMOS wafer post dicing into process-able blocks, (d) close up of the ~4 x 7 cm block

2 die) to allow for CMUT fabrication using standard micromachining tools designed for a 100 mm (4 inch) wafer in our in-house cleanroom facilities.

No wafer carrier is necessary for the photoresist spinning of these rectangular pieces as the SCS G3P8 spinners used in this work have specialized vacuum chucks that can handle the non-standard circular substrates; however, tools such as the Plasma-Therm ICP and STS-ICP that will be used to define the "donut" shape of the device requires the

mounting of the rectangular CMOS substrate to a 4 inch carrier wafer prior to processing. Although it is convenient to dice into rectangular pieces, it adversely affects the uniformity of the photoresist thickness during the spinning stage. Edge effects becomes very apparent especially for thicker and more viscous photoresist visible at the corners of the rectangular substrate and should be manually cleaned with a swap soaked with acetone before proceeding with mask alignment. Thick photoresist along the edges and corners will cause alignment issues and contact with the photo mask

4.1.2. Chemical Mechanical Polishing of CMOS Substrate

Before CMUTs can be fabricated directly on top of the CMOS substrate, the top surface of the CMOS must be (1) passivated with a thick layer of dielectric and (2) topographically “flat”. The passivation of the exposed CMOS connections from the IC foundry is performed via depositing 4 μm of PECVD silicon dioxide (SiO_2) at 250^0C. However, this passivation is not enough to smooth out the topography generated from the IC layers below. It is important to have a flat surface especially in the areas where CMUTs will be fabricated due to the small vacuum gaps of 30-100 nm. If the topography or surface roughness exceeds that of the gap or is or the order of the gap size, then the CMUT either not function or behave unpredictably due to a non-uniform in gap thickness. Initial efforts for planarizing the oxide layer is performed by Logitech PM5 semi-automatic polisher. The polishing slurry used is a mixture of Leeco 1 μm aluminum oxide and 0.06 μm colloidal silica. The finer particle size for colloidal silica helps to improve surface roughness of the SiO2. Figure 4.2 shows the profilometer scan of the CMOS surface at 3 different stages of the processing. Although not all of the topography can be removed via our polishing efforts, however, the observed slope is acceptable. Instead of sharp 1 μm posts, the

topography is now a gentle slope of 0.5 degrees from the horizontal shown in Figure 4.2. Over the lateral sizes of the CMUTs (20-50 μm) this will be considered insignificant topology. Removal of the residual slurry is best done by ultrasonic agitation soaked in acetone. If necessary, a brief dip in Aluminum Etch Type A can etch away the alumina particles and is selective over SiO_2 passivation layer.

With the decreasing in CMUT gap requirements for higher efficiency, current chemical mechanical polishing (CMP) efforts are outsourced to Axus Technologies Inc. where nanometer surface roughness can be controlled for. An average of 100 Å roughness may still exist even after industry quality polishing and could be due to contamination from piggy-back runs after other customer's polishing jobs. This can be easily treated by performing quick 10-20 second dip in buffered oxide etch (BOE) to remove the last part of the surface roughness.

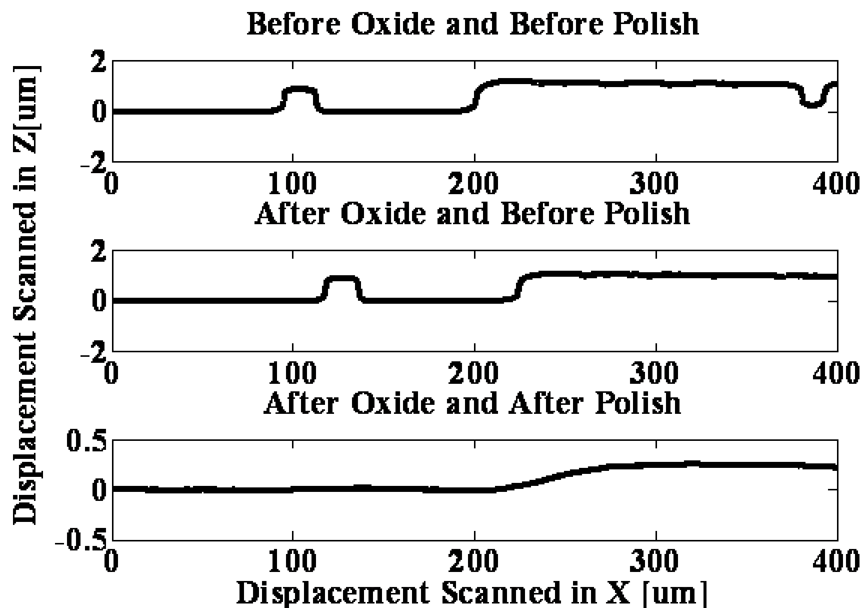


Figure 4.2 Profilometer scans of the CMOS surface at various processing steps before CMUT fabrication.

4.1.3. CMUT-on-CMOS Monolithic Integration with HfO_2 Insulation Layer

To avoid repeating the description of CMUT fabrication, only the details for CMUT-on-CMOS integration will be described in full. A summary of the entire process is necessary to keep the fluidity and clarity of the added steps necessary for MEMS to CMOS integration. The new process flow is described in Figure 4.3 to show the changes one has to make between processing on a silicon substrate versus on a CMOS substrate that already has the IC fabricated from TSMC foundry.

CMUT fabrication summary: (1) We begin with a 3 µm SiO_2 passivation layer. (2) Then a conformal chromium (Cr) bottom electrode (BE) is deposited and patterned. (3) A 50 nm layer of copper is uniformly deposited by the Unifilm DC sputter and patterned by wet Cu etchant (APS 100) as the sacrificial layer (SAC) for the vacuum gap. This etchant is highly selective and does not attack Cr. (4) Then a conformal layer of either SiN or HfO is deposited for the insulation layers. A Cambridge Nanotech Fiji F202 system was used to deposit thermal HfO at 250^0C from Tetrakis (Dimethylamido) hafnium (IV) (TDMAHf) precursor. It is noted that the substrate must be placed into the load-lock at near room temperature to prevent excessive oxidation of copper surface which increases surface roughness. (5) AlSi 2% is sputtered and patterned for the top electrode (TE). (6) 1 µm of SiN is deposited to thicken the membrane structure. (7) Reactive ion etching (RIE) is used to open the dielectric layers to the Cu layer. A separate SF_6 based chemistry is used to etch across the HfO layer instead of CHF_3 used for SiN. (8) Cu SAC layer is released via wet etchant and super critical dryer to avoid stiction of the membrane. (9) More SiN is deposited to the desired thickness of design and bond pads are opened via RIE for wirebonding.

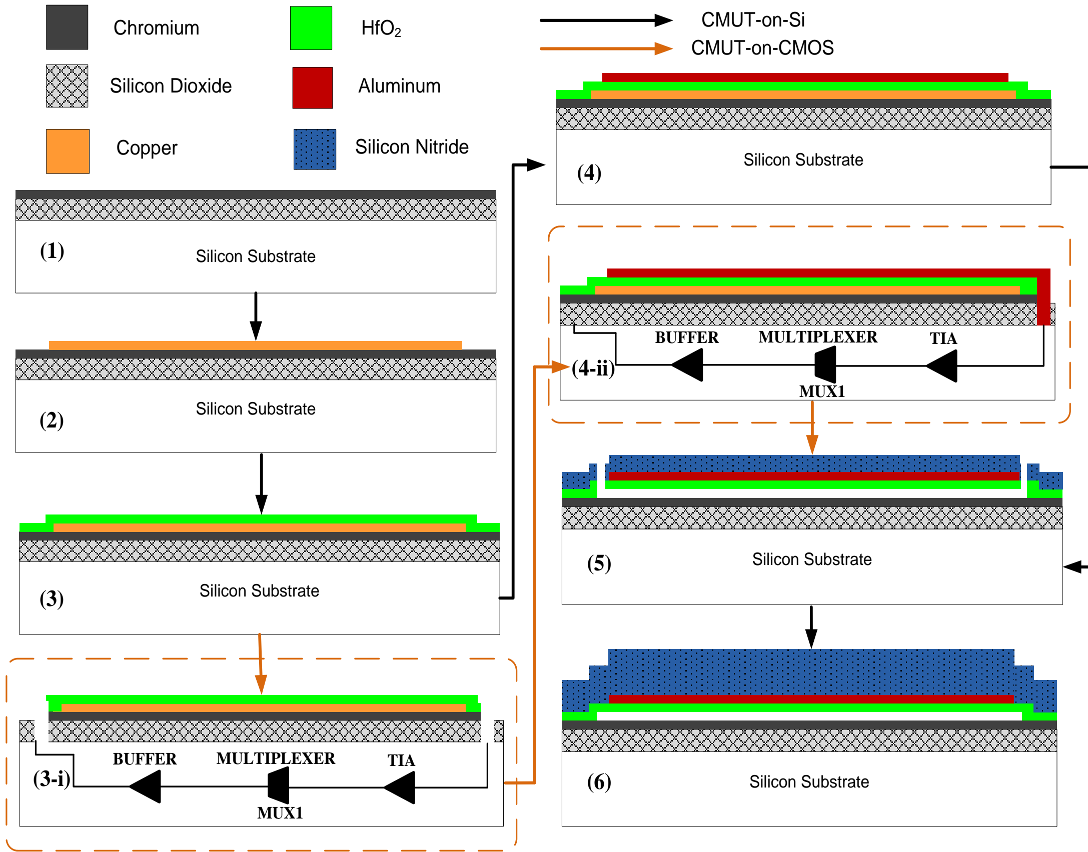


Figure 4.3 CMUT-on-CMOS monolithic integration fabrication process with low temperature ALD hafnium oxide insulation.

For CMUT-on-CMOS integration, we use the same IC electronics as in [86], with planarization of the CMOS substrate surface roughness to <100 Å. Before step (5), RIE is used to make vias from the HfO level through different layers of dielectrics (HfO and SiO_2 from the foundry layers) to the CMOS connection posts, where the positions are illustrated in Figure 4.4. The etch rate of HfO is significantly slower than bulk etching due to the size of via openings (Φ = ~15 μm) and is approximately ~3-4 nm/min. The larger CMOS connection pads (85 x 85 μm) which is later used for wirebonding, will be etched open first before the smaller connection etch holes. Since the under layers are all thick aluminum metal layers coming from TSMC (~1 μm), this acts as a good etch stop and can be used to

guarantee successful and complete etching of the dielectric layers by over etching with RIE.

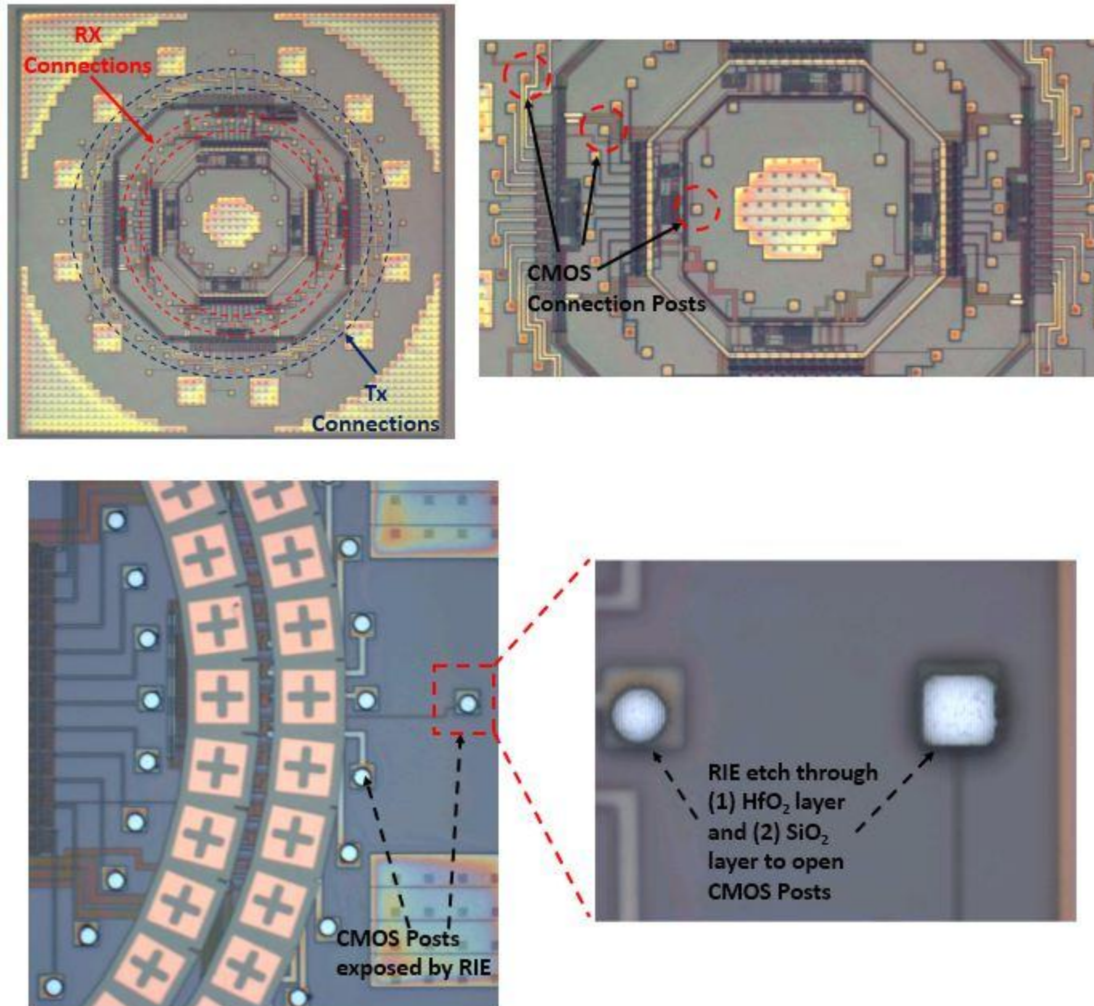


Figure 4.4 (Top) CMUT-on-CMOS die showing the location of TX and RX vias where the TE will connect to the CMOS IC underneath. (Bottom) RIE opening of these vias after the bottom and and sacrificial copper has been deposited and patterned. Also the HfO has been deposited and passivates the surface.

After which the TE is formed like previously mentioned so that the input of TIAs are connected to receive (Rx) TE and the output of NMOS pulsers are connected to transmit (Tx) TE. It has been observed that by adding another layer of AlSi 2% metal (~200-250 nm) around the region of the CMOS connection holes can increase the yield and decrease

the connectivity issues from the top electrode layer. The reason is that more metal thickness (TE + CMOS connection metal) will be available to uniformly coat the side-walls of the connection vias (~3 µm). The advantage to this technique is that it allows for larger margin of error for developing smooth and angled sidewalls on the via through tweaking the RIE etch recipe (plasma power, gas ratios and pressure). The disadvantage is that another mask is needed for the process and additional sputtering and lithography of the AlSi reliability layer. However, based on testing results, this has a higher yield/reliability for connections to make contact to the IC level and it also reduces the overall resistance at the contact vias due to thicker metal layers. Lastly, this method does not increase the thickness of the top electrode which can potentially affect the mass and stiffness of the membrane (which will affect the frequency design) if it were changed. This extra step can be seen in Figure 4.5.

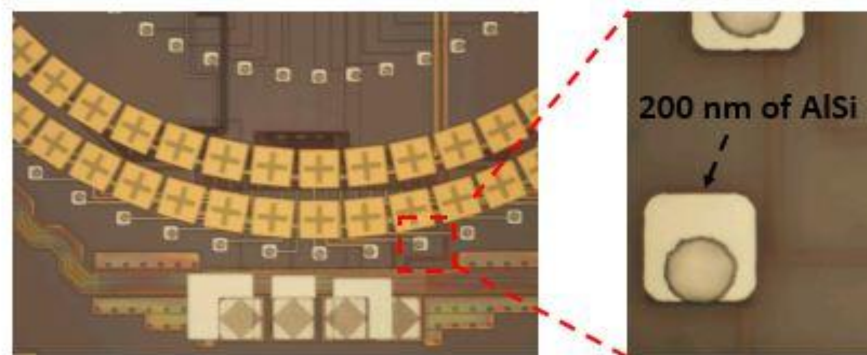


Figure 4.5 Extra layer of AlSi for connection reliability of the top electrode to the CMOS IC through the RIE vias. This micrograph shows the metal patterned and just before the formation of the top electrode.

Other steps continue the same as fabrication on silicon substrate. The fabrication of test devices on both Si and CMOS follow the process shown in Figure 4.3.

4.2. Characterization and Imaging of CMUT-on-CMOS with HfO_2 Insulation

Before the characterization and imaging results are presented from CMUT-on-CMOS integration, a brief system level description will be given. Detailed electronic design and characterization will be omitted for focus on the system level performance and can be found in [60]. This particular CMUT-on-CMOS array has 56 Tx elements and 48 Rx elements with an overall diameter of 1.4 mm aperture size. The CMOS electronics contain a separate TIA for each receiver element. Each receiver element is made of 4 membranes with 25x25μm^2 area (defined by the vacuum gap). All other geometric parameters are summarized in Table 4.2. There are four 16x1 multiplexers that routes to a total of 4 output receive channels with 4 buffers each connected to a separate output as shown in Figure 4.6.

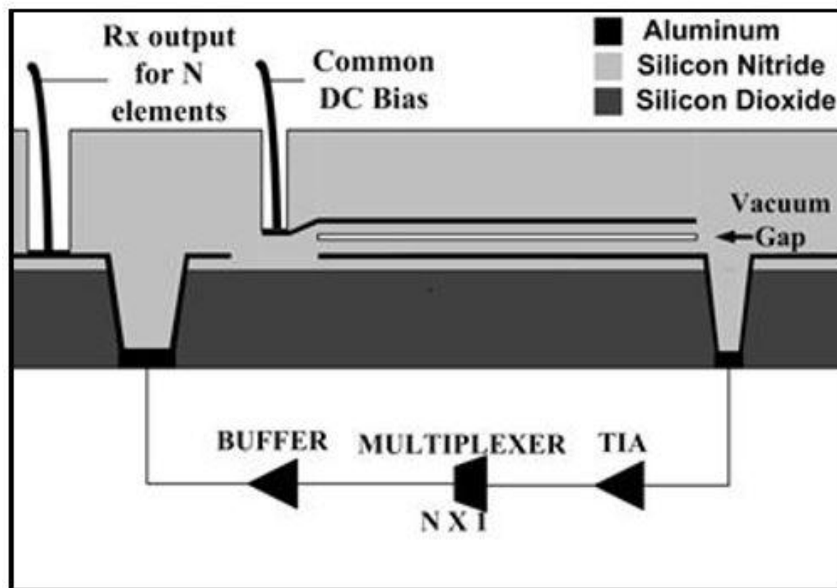


Figure 4.6 CMUT-on-CMOS cross section schematic showing the connection scheme of CMUT to CMOS circuitry.

Table 4.2 CMUT-on-CMOS High Frequency FL-IVUS Test Array Geometry

Parameter	**Value**
Membrane Size	25x25 μm
Top Electrode Size	20x20 μm
Vacuum Gap	50 nm
Si_xN_y Membrane Thickness	2.1 μm
HfO_2 Isolation Thickness	100 nm
No. of Membranes per element	4
No. of Tx Elements per device	56
No. of Rx Elements per device	48
Diameter of Array	1.4 mm
External Connections	13

Each of the 4 groups of TIA/multiplexer/buffers are routed in each of the four quadrants as shown in Figure 4.7.

The electronics on chip also include the digital decoder and control lines to aid in collecting data in a sequential manner from all of the Tx-Rx combinations. This clock input (CLK) requires a timed voltage input that is triggered by an external function generator. In this particular CMOS version, the N-type metal-oxide-semiconductor (NMOS) pulsing circuitry is included and is capable of generating up to +25V unipolar pulse. The IC in this version was directly positioned underneath the CMUT locations so that the 1.4 mm real-estate space was used optimally and the entire chip can theoretically be placed at the tip of a ~3F catheter. There are 13 output connections to the chip which can be either wirebonded at the initial testing phase or eventually be routed by through silicon vias (TSVs) to the

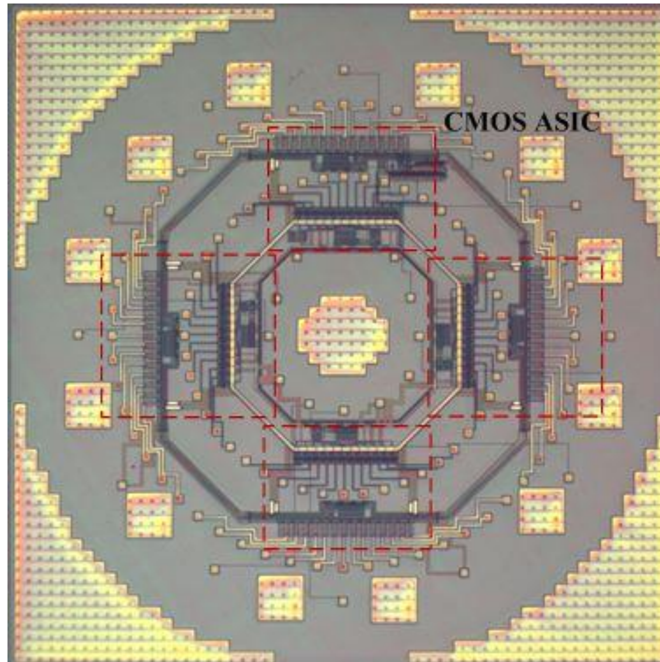


Figure 4.7 Micrograph of CMOS chip highlighting the position of receiver electronics (TIA/multiplexer/buffer) for each of the four output channels.

backside for integration with flexible interconnect and micro-cables. This will be described in more detail in Chapter 7. These 11 connections are shown in Figure 4.8. Additionally, 2 more connections/cables will be required to supply V_{DC} to Tx and Rx bottom electrodes. Each input/output (I/O) connection's function is described in brief for completeness of the system. There are four RF outputs (out1-out4) that carry the amplified RF analogue signals out of the chip. The clock (CLK) input is for supplier voltage signals to control the timing and switching of the Tx and Rx combinations. Clear_n pin is used to reset the chip to the ground state. Ground (GND) terminal is to supply the chip with a grounding reference from an external power supply. V_{CTRL} is the control voltage to tune the closed-loop gain of the TIA which also affects the bandwidth of the output. V_{dd} is typically 3.3V supplied to power the TIA and all the other circuitry included on chip. V_{BIAS} is supplied to the gate of the transistors and adjusting it actively controls the bias current and bandwidth of the output

of the TIA. V_{dd_pulser} is the externally supplied high voltage (up to +25V) to the input of the NMOS pulser IC for pulse voltage.

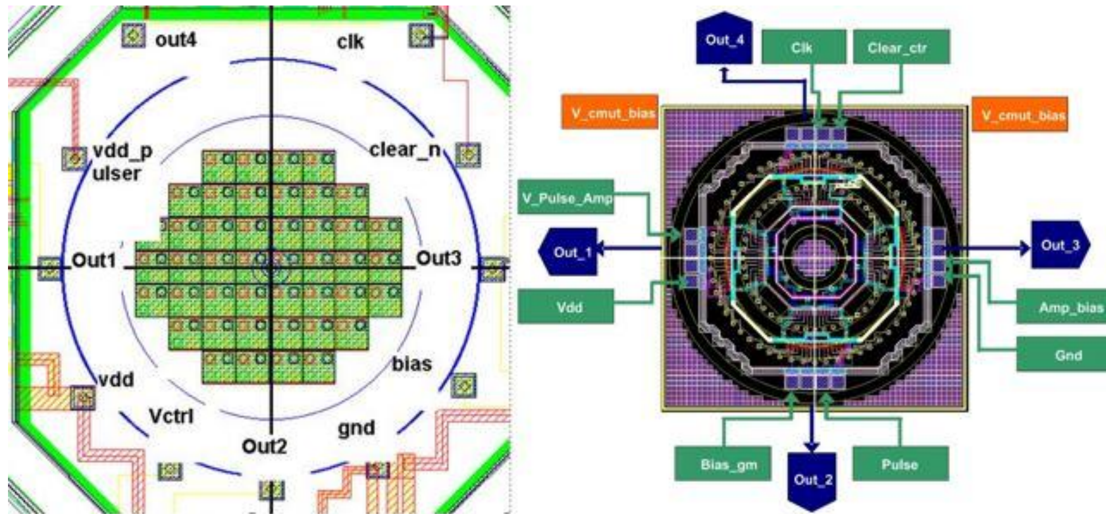


Figure 4.8 Schematic of IC I/O connections. 11 connections total for outside packaging/cabling (left). Micrograph of the IC with receive and transmit electronics and the digital control circuitry (right).

4.2.1. Experimental Setup: Imaging of Pig Artery Phantom

After dicing the fabricated CMUT-on-CMOS FL-IVUS chips with high-K HfO_2 insulation layer, it is packaged onto a custom PCB board via UV curable epoxy. The 13 external connections are wirebonded from the chip to the chip holder. It is then parylene coated to passivate the setup from water during testing. A petri dish is then used as a small water tank and encases the opening of the PCB package. This setup is shown in Figure 4.9.

The outputs of the channels are connected to high-end digitizer cards that are installed in PCIe slots inside a high performance PC built for this imaging setup. Each card can take up to 2 output analogue channels, which are subsequently digitized simultaneously at 4-bit and 250-MS/s. The pulse repetition rate is 40 KHz. The digitizer cards can record up to 2.5 seconds of image data with a 100-MHz sampling rate. A total of 6 power supplies is required for V_{dd}, V_{CTRL}, V_{bias}, V_{DC_TX}, V_{DC_RX}, V_{pulser} and a small ADC board to provide the logic 3V signal to clear_n to reset the chip.

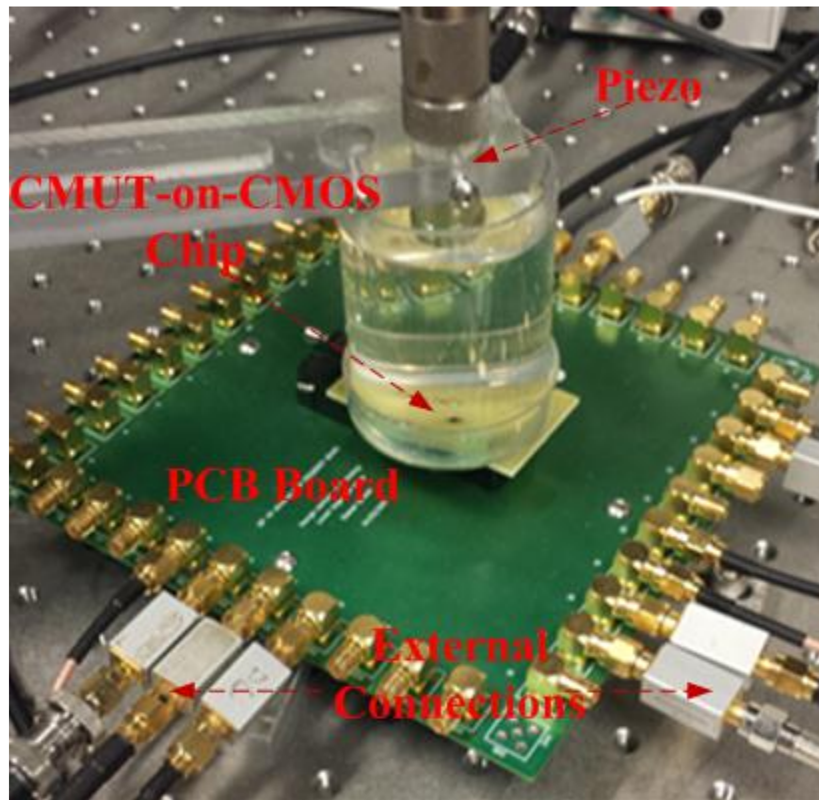


Figure 4.9 CMUT-on-CMOS characterization and imaging setup.

4.2.2. CMUT-on-CMOS Bias Scheme for Transmit and Receive Operation

Before presenting the results of CMUT-on-CMOS characterization, the biasing scheme of CMUT-on-CMOS must be explained and is different from a CMUT fabricated on a silicon substrate. The differences arise from the fact that the top electrode in the CMUT-on-CMOS chip is connected to the input of the NMOS pulser electronics for the transmit case and during the "off" state has a voltage of $V_{pulser.}$ The bottom electrode is supplied by a separate power supply with a voltage of V_{DC_TX}. This means that the potential difference between the top and bottom electrode of the Tx element is actually $\Delta V_1 = |V_{DC_TX} - V_{pulser}|$. For the "on" state of the pulser, $V_{pulser} = 0$ during the time of the short pulse and $\Delta V_2 = |V_{DC_TX}|$. The difference between the on and off state as well as the specific voltages that are applied to the top and bottom electrodes are shown in Figure 4.10.

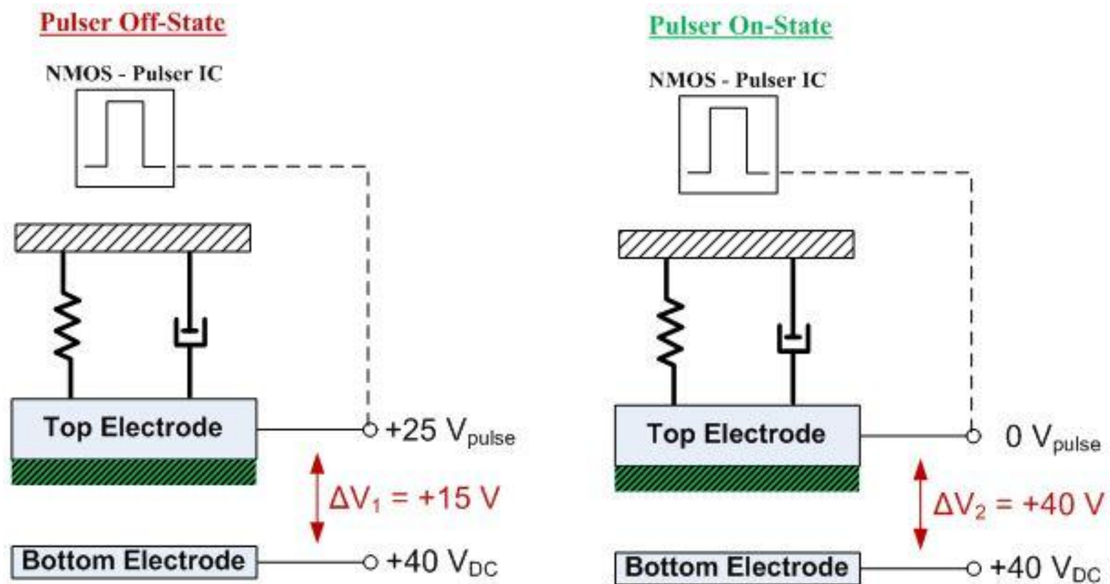


Figure 4.10 CMUT-on-CMOS biasing scheme for "on" and "off" state of the NMOS pulser.

The transient representation of the input voltage to the transmitter elements is shown in Figure 4.11. With this particular biasing scheme for CMUT-on-CMOS, a DC+AC 2D scan map was created to evaluate the Tx pressure output under different biasing conditions. It is known from simulation that the maximum pressure output is achieved by full swing of the vacuum gap and can be achieved by a large enough V_{pulser} voltage. In this particular design case, a V_{pulser} = 48V and V_{DC} = 0V for a pulse width of 24ns (square pulse) is necessary to achieve full gap swing. Unfortunately, the onboard pulser electronics is limited to +25V maximum. This means V_{DC} is needed as well in addition to the +25V to achieve similar maximum pressure output as compared to the case of full gap swing with only V_{pulser} voltage. Different $V_{DC} + V_{pulser}$ combinations are supplied to the Tx elements of the CMUT-on-CMOS chip and a hydrophone (ONDA HGL-0085) was used as the receiving transducer to measure the output pressure.

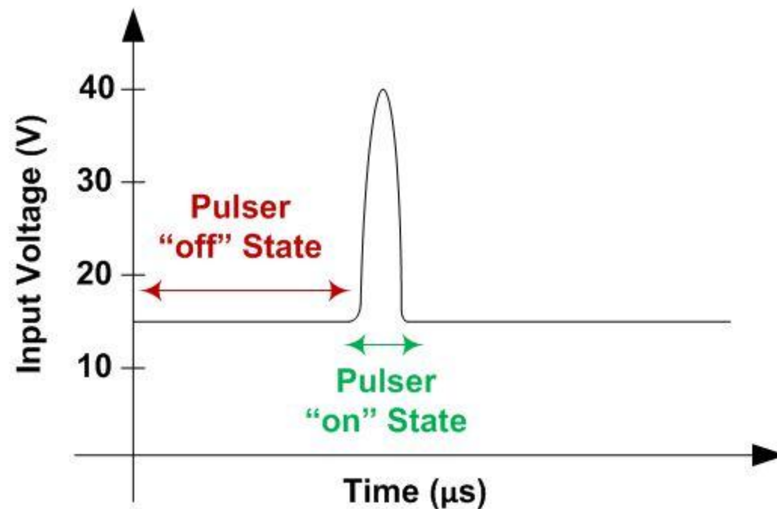


Figure 4.11 CMUT-on-CMOS transient input voltage schematic.

4.2.3. CMUT-on-CMOS Transmit optimization Results

The resulting peak-to-peak pressure map with different V_{DC} + V_{pulser} is shown in Figure 4.12. The missing data points in the region between V_{DC} = -10 to +10V was not collected because it is obvious that the pressure level from those conditions are very low. This reduces the number of total data points needed for data collection and decreases the experimental data collection time. Data between those points can be viewed as “Null” or “N/A”. The bottom left corner was also “Null” data since we tried to keep the total voltage below 40V which is close to the breakdown voltage of the HfO_2 insulation layer. It is worth pointing out that it is especially more “dangerous” to approach a total of 40V with the negative V_{DC} bias because it is at the higher voltage level during the “off” state. Since the device is at the “off” state the majority of the time, this can cause undesirable charging with higher probability over a long duration of device operation.

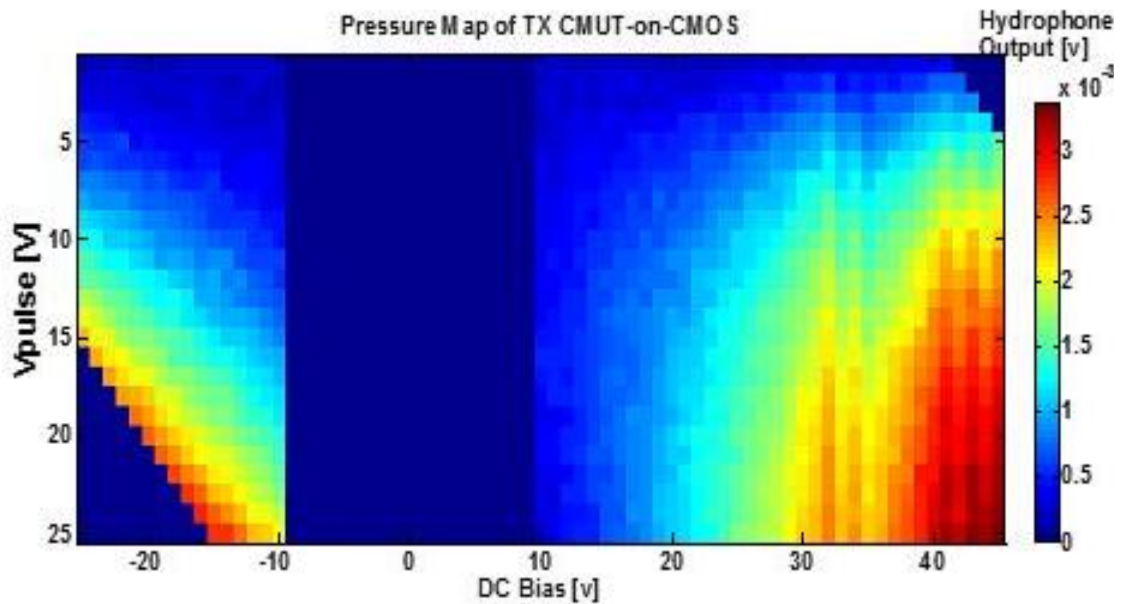


Figure 4.12 Pressure map: Tx optimization with different V_{DC} + V_{pulser} combination.

The main results from Figure 4.12 are that the largest pressure output can be achieved with this CMUT-on-CMOS system when we choose a high V_{DC} such as +40V and maximize V_{pulse} to +25V. This combination actually comes very close to the theoretical breakdown voltage of the HfO_2 during the "on" state when $\Delta V_2 = |V_{DC_TX} = +40V|$. However, unlike the negative V_{DC} bias situation, the "on" state is very short (in the 10-30 ns range) and thus minimizes the probability of long term charge trapping inside the HfO_2 insulation layer. Similar results and trends for optimizing Tx pressure were also reported in [37] with simulation validation from a large signal model [58].

4.2.4. CMUT-on-CMOS Stability Testing

A reliability test was performed to observe the transient stability of the HfO_2 insulation layer in terms charging during operation. Signals were transmitted from the CMUT and received with a piezoelectric transducer for 4 hours with data collection every minute. Then the experiment was repeated with a pulse transmitted by the piezoelectric transducer and received with the CMUT elements. In transmit mode of the CMUT, the peak-to-peak received signal from the piezoelectric transducer had a standard deviation of 7.9% from the mean, at near maximum output pressure actuation condition. In receive mode, the CMUT elements are DC biased at 88% of $V_{COLLAPSE}$ and V_{BD} voltage. The peak-to-peak received signal from the CMUT had a standard deviation of 3.7% from the mean. Since the variation in both transmit and receive mode are small, we conclude that the

reliability of the HfO_2 insulation is reasonable over the 4 hour testing period and little to no charging is observed, seen in Figure 4.13.

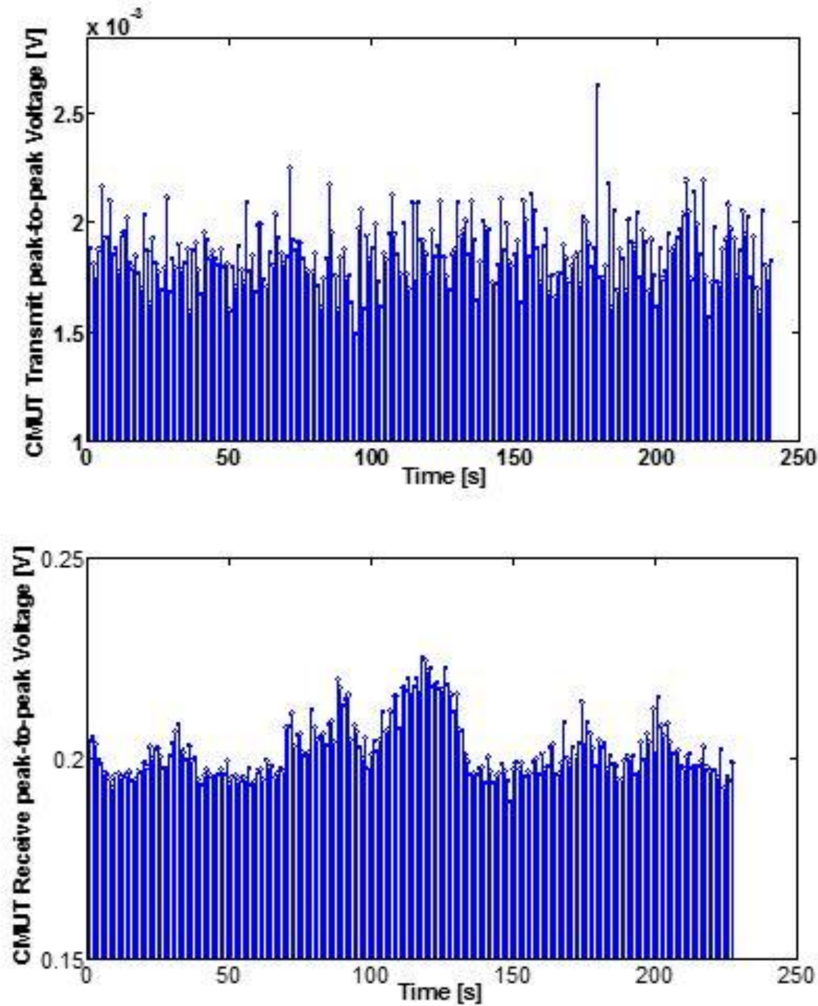


Figure 4.13 Reliability test over 4 hours; CMUT transmit pressure with piezo receiving (top), Piezo transmitting with CMUT receiving (bottom).

4.2.5. CMUT-on-CMOS Imaging Results

A full synthetic aperture data acquisition scheme is used for the CMUT-on-CMOS system described in this work. This means that one transmitter pulses while the first 4 receivers will receive. This is then repeated while switching to the next set of 4 Rx until all of the receiver combinations are cycles through for the one transmitter. This is then repeats

for the next Tx element. This means there is a total of 56x48 = 2688 Tx-Rx combinations. Every Tx-Rx element pair's pulse-echo data for was acquired for 25 μs (~1.9 cm imaging depth) without any time gain compensation or averaging. This gives a real time data acquisition rate of ~60 frames/s considering 2688 Tx-Rx combinations and 4 parallel receive channels. Lastly, a delay and sum algorithm was then used to create a volumetric image from the combination of all pulse echo data sets. Distances from each of the transducer element was calculated to every point in the image space (volume). If the echoes signals coherent added to a point in space after the artificial time delays then that means the echo actually came from that position and a bright spot will be created for that particular voxel (pixel if in 2D plane). If the signal did not come from that particular location then the noise will incoherently cancel each other out due to phase differences.

Figure 4.14 shows the experimental setup for imaging of a pig artery section. The biasing scheme used for this experiment was near optimum for Tx (V_{DC} = +40V with V_{pulser} = +25) and at 88% $V_{COLLAPSE}$ for Rx. In this particular experiment, coded excitation [113] was used to also improve SNR. we used a small pig artery phantom. The phantom was immersed in water inside the Petri dish and placed approximately 2.5 mm above the array surface as shown in Figure 4.14. The diameter of the artery is around 4 mm. We first collected and recorded all A-scans obtained from 56×48 Tx-Rx combinations to further perform offline processing and beamforming. Since the effective imaging depth is 10 mm, we collected 25-μs data for each A-scan with a sampling rate of 250 MS/s and pulse

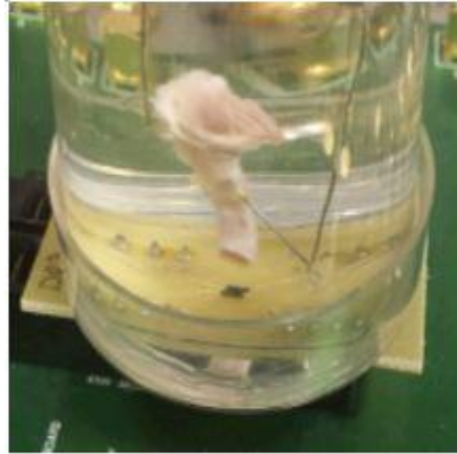


Figure 4.14 Experimental setup of wire-bonded CMUT array on a pcb chip holder combined with a modified Petri dish for pig artery imaging phantom.

repetition of 40 kHz. A custom RF beamforming software was used to process A-scan data. We reconstructed cross-sectional B-scan images in yz plane and xy plane. The xy cross-section was reconstructed at a depth of 6 mm. The images with 40 dB dynamic range are presented in Figure 4.15. This imaging result is comparable to previously presented results

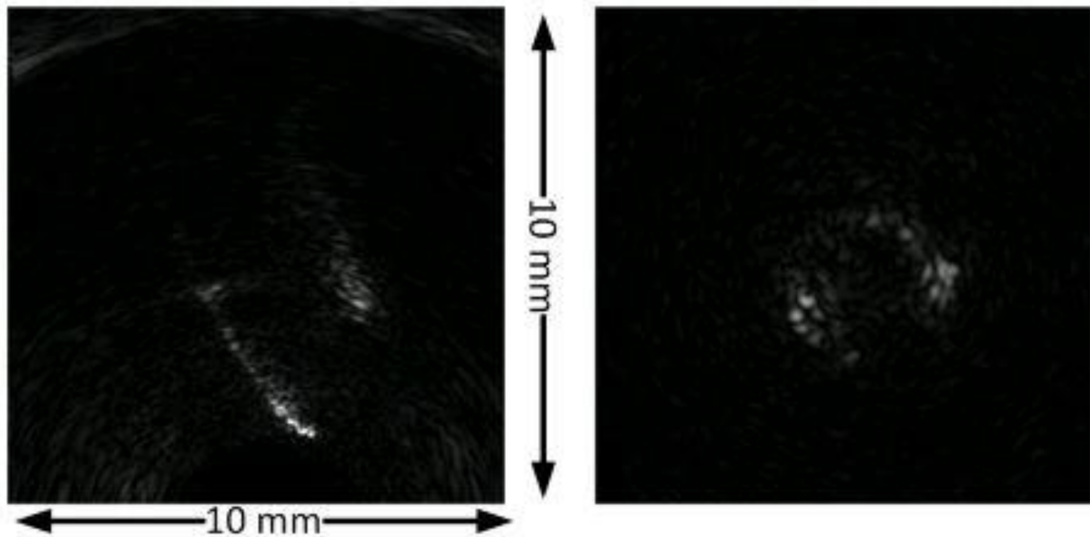


Figure 4.15 2D Cross-sectional image of the pig artery phantom on yz plane (left) and xy plane (right).

with larger gap CMUTs and SiN insulation layer in [83]. The reconstructed 2D cross-sectional images using coded excitation produces +9 dB improvement in image SNR compared to single pulse excitation without any frame rate degradation. The side walls of the pig artery can be easily seen up to 8 mm depth. In these cases, it is hard to make absolute comparisons as biasing conditions may not be exactly the same.

4.3. CMUT-on-CMOS Packaging for Catheter Prototype

4.3.1. Donut Fabrication Process for CMUT-on-CMOS

As suggested at the end of Chapter 1, the end goal is to produce a catheter prototype for initial efforts towards animal testing. In order to prototype a catheter, there are many requirements and packaging challenges that needs to be addressed from the silicon chip end. First the final die shape of the chip must be round and "donut" shaped to allow a center opening in the middle of the chip for standard guidewires (~Φ=350 µm or 0.014") to go through. Traditionally, devices are diced into square or rectangular dies before packaging and testing using semiconductor compatible dicing saws. However, round shapes are impossible to make with such methods. We used a combination of deep reactive ions etching (DRIE) and the Bosch process to "stamp out" or "etch release" the donut shape. Since this step is after the entire fabrication process of CMUT-on-CMOS, only soft masks such as photoresist is acceptable and compatible. In order to etch through to the bulk silicon surface, ~12-14 µm of dielectric stack is needed to be etched through including ~10 µm of SiO_2 from the IC level, ~100 nm HfO_2, and ~2.2 µm of SiN. After which the Bosch process is used to etch through the remaining bulk silicon thickness (300-400 µm). Thick photoresist such as AZ-4620 was used in this work with a double patterning process to obtain ~30 µm thickness. A long (~2 hour) low temperature pre-bake at 75^0C was needed

to cure the photoresist. One hour hydration rest between each spin layer is necessary in standard humidity levels. AZ 400K developing solution at a 1:3 dilute level with DI water is used to develop the resist. No post bake was performed so that resist reflow does not occur and change the dimensions of the feature. Changes to the feature can slow down the etch rate of each of the steps described. This process flow is shown in Figure 4.16.

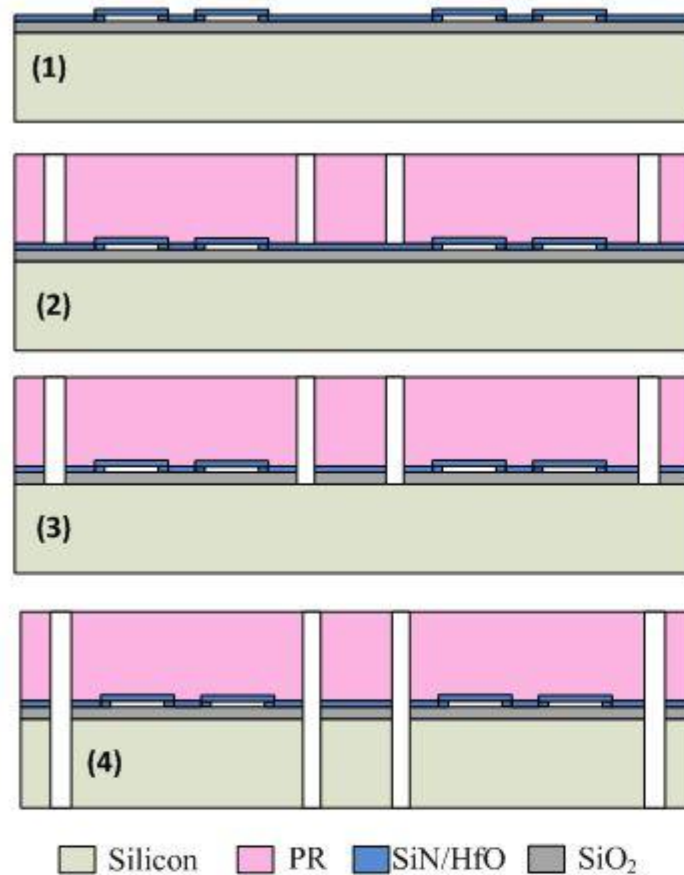


Figure 4.16 Donut fabrication process schematic.

Figure 4.17 shows the successfully released donut shapes from the CMOS substrate. Process yield for this particular method is poor (~70%) especially on the substrate edges due to significant edge bead effect during spinning of the rectangular shape substrate.

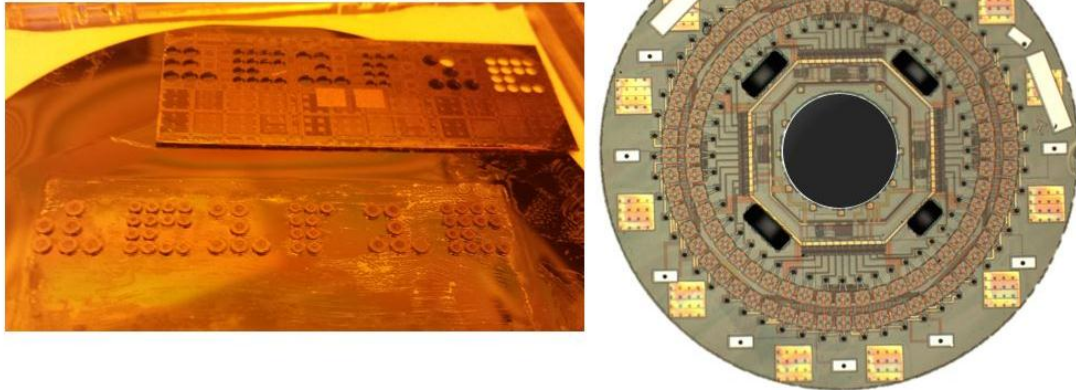


Figure 4.17 CMUT-on-CMOS devices released from the IC substrate through DRIE and Bosch process (left). Micrograph of the final released donut shaped DIE with CMUT-on-CMOS technology (right). The die has Φ = 1.5 mm OD and an inner hole diameter of Φ = 500 µm.

4.3.2. Polyimide Flexible Interconnect for CMUT-on-CMOS

Our approach for connecting micro-cables to the I/O connections and various power lines to the CMUT-on-CMOS chip is through the implementation of flexible interconnect. The beginning strategy is to attach flexible polyimide interconnect with gold electrical traces to the front side and outer edge of the chip. This work was performed by Dipl.-Ing. Jutta Müntjes and Dipl.-Phys. Sebastian Bette at Institut für Werkstoffe der Elektrotechnik, Aachen, Germany. After the successful fabrication of CMUT-on-CMOS chips, a selected batch of devices were first tested in house at Georgia Tech. to ensure that the IC electronics were functional and giving reasonable current readings. Connections such as GND, V_{CTRL}, V_{BIAS}, and V_{dd} are tested through the use of a probe station.

The cross-section of the polyimide flexible interconnect is shown in Figure 4.18. There are 2 layers of polyimide both shown in red in the diagram (5 µm and 7 µm respectively), and 2 layers of gold traces (5 µm and 5 µm respectively). On the top side where the polyimide is opened, an extra 3 µm of gold was electroplated so it can be easily attached to the matching gold pads on the CMUT-on-CMOS chip. The attachment is made between the Au/Au interface through the help of anisotropic conductive epoxy (Ecolite® 3061). Alignment is performed by a flip chip bonder between the flex interconnect and the CMUT-on-CMOS chip and bonded in the appropriate temperature range of ~140-170^{0}C.

Figure 4.18 Cross-section schematic of the polyimide interconnect. The two red layers are polyimide and the yellow color represents gold metal layers.

The anisotropic conductive epoxy has 1 µm metal conductive particles inside and is responsible for making electrical conduction between the flexible interconnect and the gold pads on the CMUT-on-CMOS chip. Figure 4.19 shows a close up microscopy image of the flexible interconnect successfully connected to the Au pads on the CMUT-on-CMOS chip. The alignment is critical as the outer ring of CMUTs (TX) are only ~100 µm away from the edge of the polyimide interconnect. Extra non-conductive epoxy were placed in other areas to ensure mechanical stability and robustness for later processing such as wire attachment and the catheter building stage.

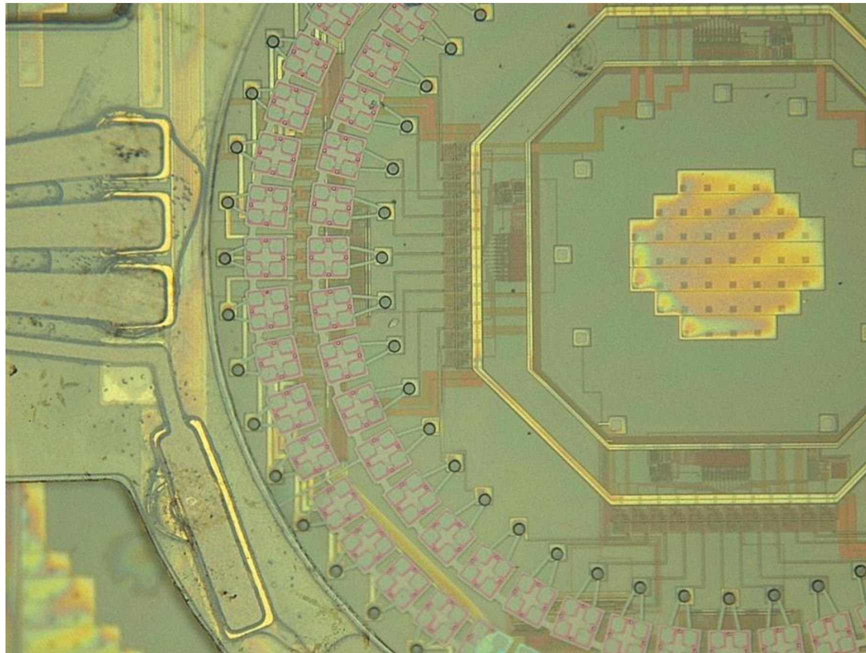


Figure 4.19 Flexible interconnect attached succesfully with a flipchip bonder to CMUT-on-CMOS connection pads. Alignment is very good in this case as no CMUTs were obstructed by the polyimide material.

To test the CMUT-on-CMOS device after flexible interconnect packaging, it is lightly epoxied onto a custom PCB board and inserted into a chip hold PCB like the one shown in Figure 4.14. The epoxy underneath the chip is very thin (~100-200 µm) and also underneath the flexible interconnect as shown in Figure 4.20. A hard epoxy must be used as too much elasticity or spring like behavior after curing will cause issues at the wirebonding stage. Next, 25 µm AlSi wirebonds are attached from the gold connection pads on the flexible interconnect side to the PCB pads. The PCB circuit material is 1oz copper with a silver coating (RoHS compliant) which is a compatible metal for wirebonding.

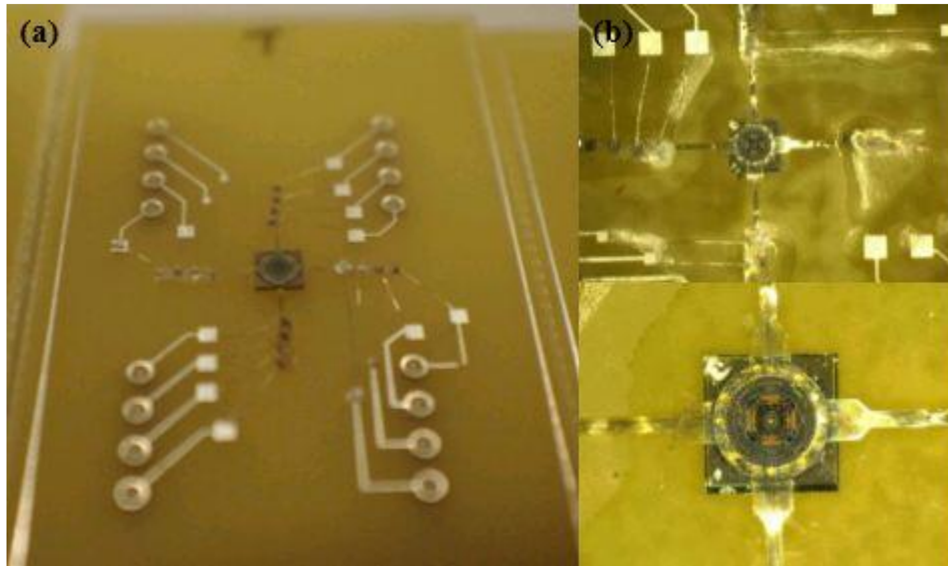


Figure 4.20 (a) Micrograph of flex interconnect packaged CMUT-on-CMOS chip on a custom PCB and wirebonded. (b) Zoomed in view of the packaged device.

Electrical I/Os are the same as the one described in Figure 4.8 and connected to the appropriate power supplies, function generators and the 4 outputs to the digitizer cards in the PC. Tx and Rx-Bias are at 120V since this was close to the $V_{COLLAPSE}$ for a vacuum gap of 120nm. These devices also have silicon nitride as the insulation layer. V_{pulse} was maximized to 25V with a pulse width of 24ns. After RF-data collection, image reconstruction was performed using full synthetic aperture approach. Figure 4.21 shows that the flexible interconnect packaged CMUT-on-CMOS device is capable of generation 3D images with good quality. The 0.5 mm diameter wire target was suspended 3.5 mm above the array surface and the image shown in Figure 4.21 has a dynamic range of 40-dB.

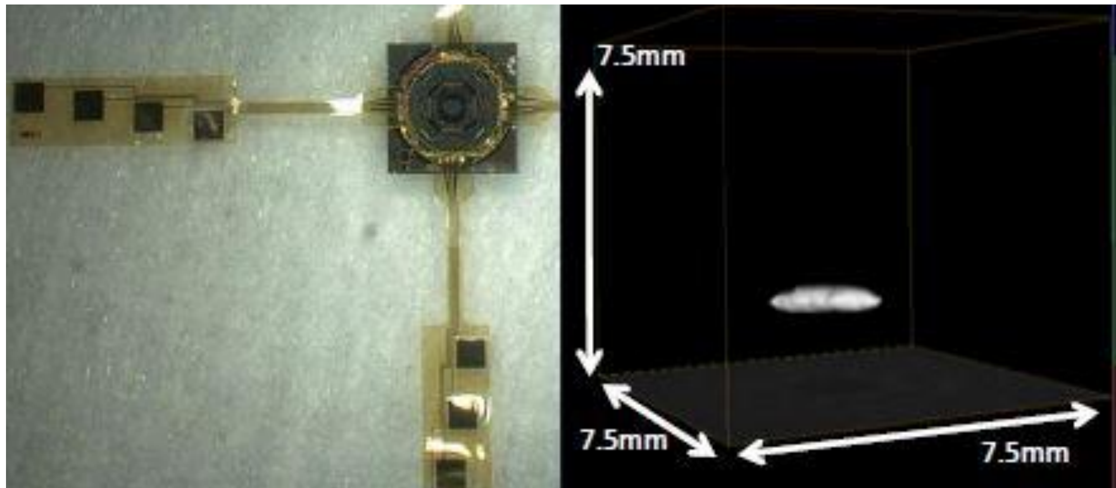


Figure 4.21 Flexible interconnect packaged CMUT-on-CMOS sensor chip (left). 3D image reconstruction of a single wire target. (Right).

The attachment of micro cables and first attempts of catheter prototyping with functional CMUT-on-CMOS devices will be described in Chapter 7 in the future work section.

CHAPTER 5. DUAL MODE SIDE AND FORWAD LOOKING IVUS USING A DUAL RING CMUT-on-CMOS ARRAY

5.1. Introduction

Currently available intravascular ultrasound (IVUS) imaging catheters have only side looking (SL) feature which enable to see the cross-sectional view of the coronary arteries [114]. A forward looking (FL) imaging system is highly desirable in IVUS for guiding interventions and potential to enable real time 3-D volumetric visualization of arteries. In particular chronic total occlusion interventions would benefit from this type of arrays. The addition of SL capability in the same catheter would be invaluable to locate the device with respect to vessel walls and provide a conventional image to the clinicians.

In FL-IVUS imaging, previous studies have focused on ring shaped transducer array configurations that fits onto the catheter's front-tip with a central opening which enables over the guide wire operation [115], [116]. Main drawback of these systems is the large number of interconnects and inflexibility due to multiple silicon chips on the side of the catheter tip. We have recently fabricated a single-chip FL-IVUS system design using the monolithic CMUT-on-CMOS integration where dual ring CMUT arrays are fabricated directly on top of pre-processed CMOS wafers [86]. We demonstrated the volumetric imaging capability of the FL-IVUS system with various phantoms [87], [117].

Although FL imaging system enables one to see 3-D volume in forward direction, a SL capability in the same FL catheter would provide a considerably functional device for the clinicians. Previous research attempted to combine these two functions in a single device using piezoelectric transducers [118]. However, this approach was not successful due to fabrication complexity and high level of crosstalk. More recently, a 3-D monolithic array was proposed to visualize both side and forward direction using 7 CMUT arrays

integrated on a flexible silicon substrate [119]. Although this system has the potential to image the whole 3-D volume (both in side and forward direction), front-end electronics integration and imaging demonstrations have not been presented. In addition, this approach suffers from stiffness of the catheter tip. A single chip CMUT-on-CMOS array may provide both capabilities while enabling an extremely flexible catheter tip implementation. Thus, it is unnecessary to have transducers located on the side of the catheter which increases catheter stiffness. For this purpose, we have investigated the combined side and forward viewing ability of the CMUT-on-CMOS IVUS array.

5.2. Experimental Work

In the CMUT-on-CMOS FL-IVUS array, individual elements radiates acoustic energy predominantly in the forward direction from the array plane. However, these small array elements have a wide radiation angle due to both bulk and evanescent waves traveling near the array surface. Initial fully coupled transient 2D-axisymmetric FEM simulation results showed that when excited with a broad-band excitation pulse, considerable amount of acoustic pressure can be achieved on z=0 plane (θ=90°) with a center frequency nearly half the operating frequency.

5.2.1 Dual Ring CMUT Arrays

The dual ring CMUT arrays used for the imaging experiments have 56 Tx (outer ring) and 48 Rx (inner ring) elements and fabricated on a 1.5-mm diameter 0.3-mm thick silicon donut. The array elements are approximately 70 μm × 70 μm and contain 4 individual membranes. Figure 5.1 shows a micrograph of the dual ring CMUT arrays that are monolithically fabricated on top of the CMOS IC. This single chip system includes all transmit and receive front-end electronics and has only 13 external connections including

the DC biases to the CMUT membranes. The center frequency of these devices was designed and measured to be around 20 MHz. Detailed information about the fabricated CMUT-on-CMOS device used in this study can be found in [86], [87], [117].

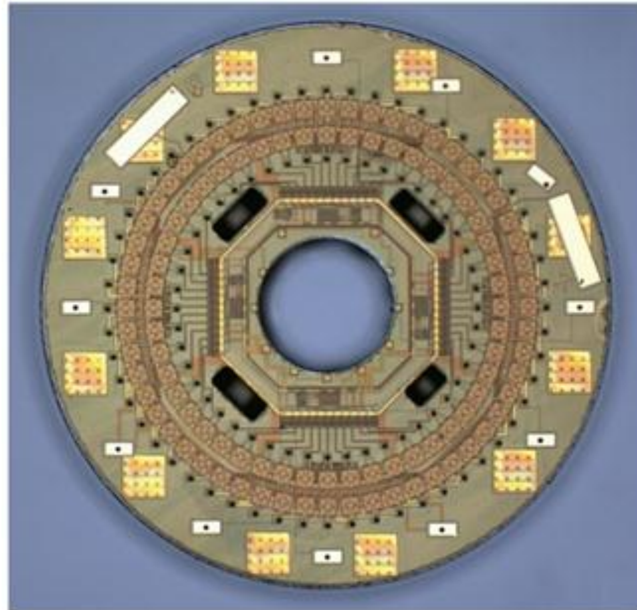


Figure 5.1 Micrograph of monolithically integrated dual ring CMUT-on-CMOS system.

5.2.2 Experimental Setup

For imaging experiments to demonstrate the side looking imaging capability of FL dual ring CMUT arrays, a custom data collection setup was constructed. We first wirebonded the fabricated dual ring CMUT arrays to a ceramic dual inline package (DIP) chip holder and secured a small petri dish on the top of the chip holder which was filled with water. Then, four metal wires attached to a holder was placed vertically in water close to the array plane (z=0) and approximately 3.8 mm away from the array center. **Figure 5.2** shows the picture of the experimental setup. A custom board was used to make the external

connections to the system. We also used a single wire phantom placed 5.5 mm above and parallel to the array plane to demonstrate dual mode imaging capability of the system.

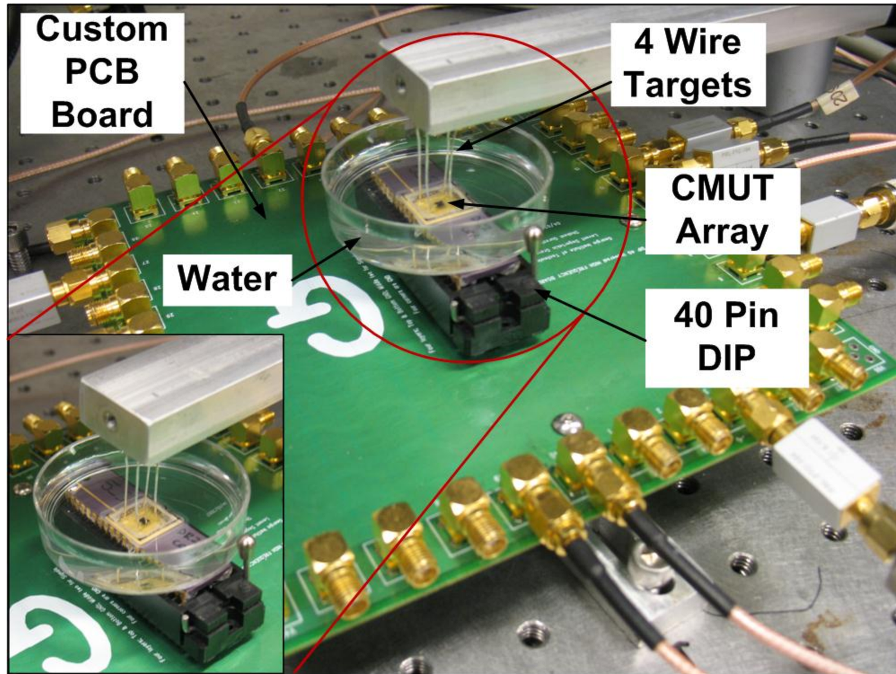


Figure 5.2 Experimental setup of wirebonded CMUT array in a chip holder for imaging four wires located vertically close to the array plane.

5.2.3 Imaging Results

Using the experimental setup, we have collected all Tx-Rx pulse-echo signals from vertically placed four wires and horizontally suspended front wire each 0.5 mm in diameter. The recorded data is used to reconstruct the images by offline synthetic phased array technique. 3-D rendered and 2-D cross-sectional images from the experiment are shown in Figure 5.3. In side looking mode all four wires can be clearly seen in the images with a dynamic range of 40 dB. The pulse-echo data from front wire and beamformed A-scan data from a single side wire are plotted in Figure 5.4. Figure 5.5 shows the frequency spectrum of the side and front targets which have a center frequency of 11 MHz and 20 MHz, respectively. This indicates that the effective frequency band of the side looking mode is

significantly lower than the operating frequency of the device. Therefore, in side looking image reconstruction we filtered the pulse-echo data around 11 MHz to obtain a better SNR image. The cross-sectional image in side looking mode is similar with the conventional IVUS images. The brightness of one of the side wires in cross-sectional image is less than the other three wires due to non-uniformity in the dual ring array.

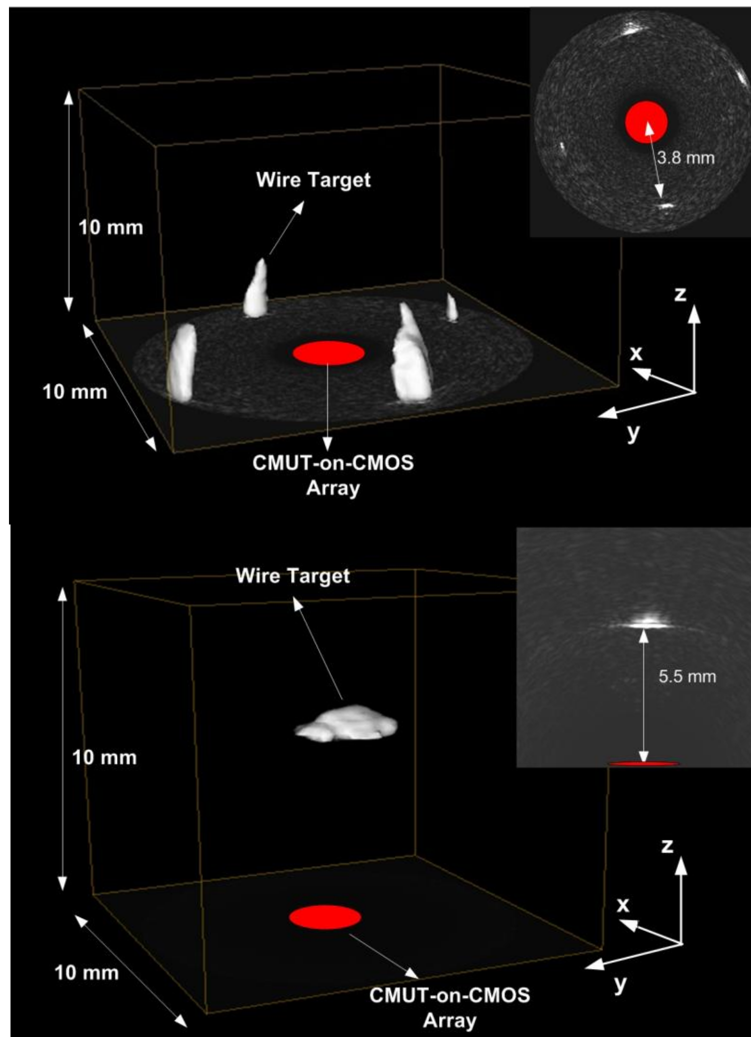


Figure 5.3 3D rendered and xy cross-section images of side wires (left) and front wire targets (right).

We also measured axial and lateral resolution on the side wire targets. The 6-dB axial and resolutions for the wire at 3.8 mm away from the array center are measured as 100 μm and 282 μm, respectively. These results are consistent with theoretical calculations when effective frequency spectrum for the side looking mode is considered. We have also computed image SNR of 31 dB corresponding to the brightest wire target of the four side wire phantom. This corresponds to an approximately 20 dB decrease when compared to the image SNR of the front wire.

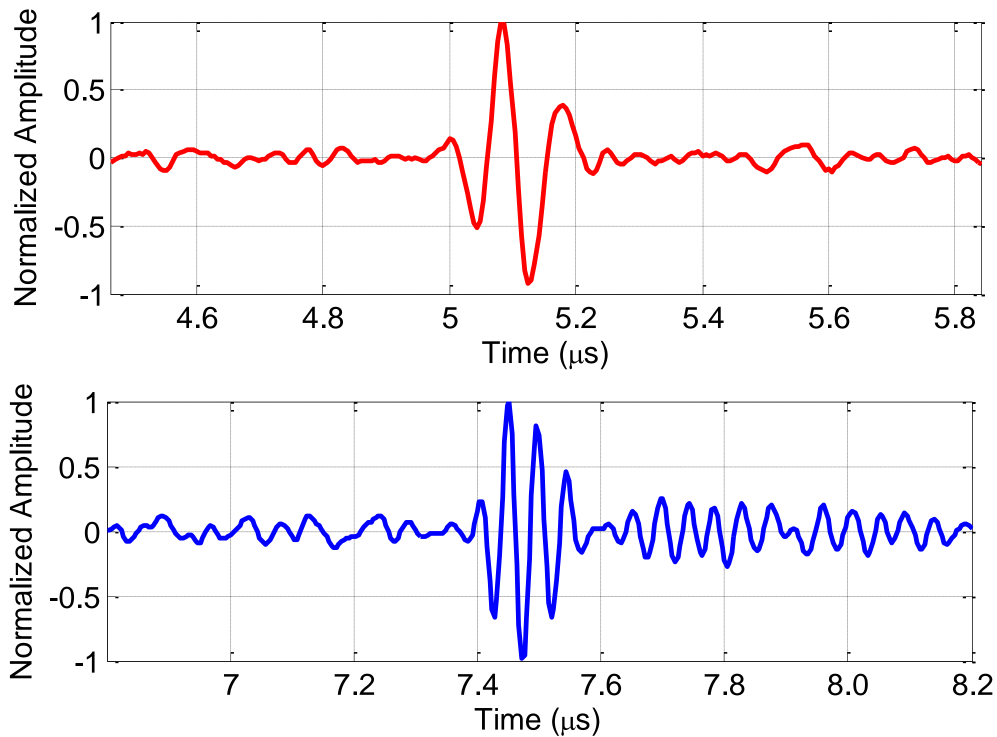


Figure 5.4 Beamformed Ascan data from side wire target 3.8 mm transverse to the array (top) and pulse-echo data from front wire target 5.5 mm directly above the array (bottom).

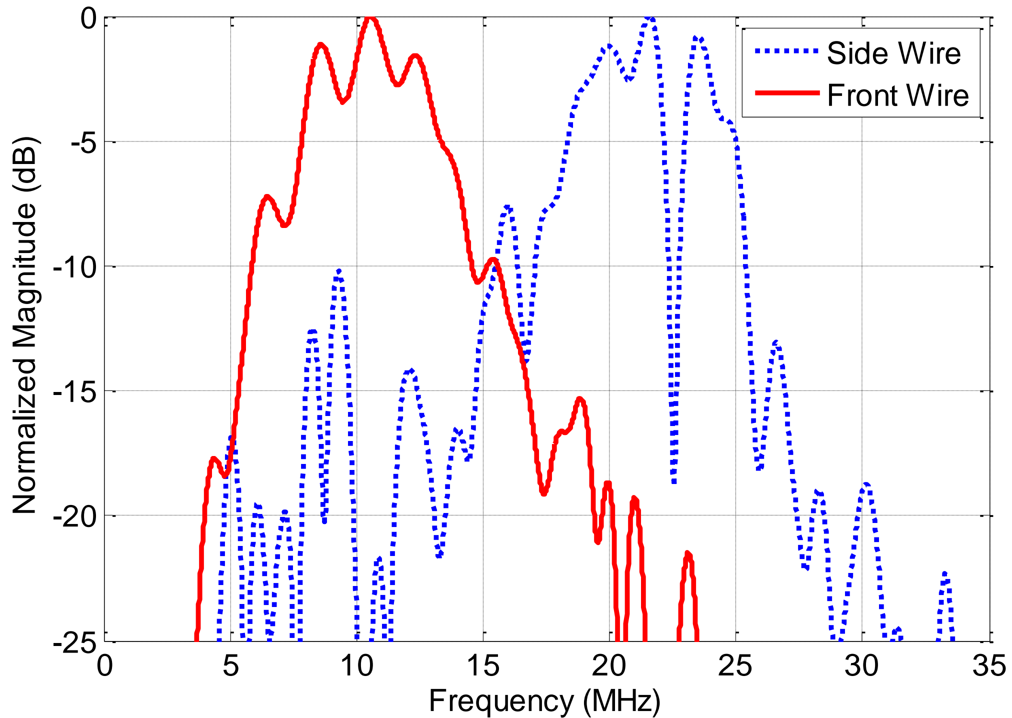


Figure 5.5 Pulse-echo frequency spectra from side and front wire targets.

Additionally, a larger X-Y image plane at Z=0 is taken from the data collected from the 4 wire experiment shown in Figure 5.6. This image has an 18x18 mm^2 area size and in this image one can observe the 4 wires as well as the border edges of the chip holder. Finally, the bright ring in the image is due to the grating lobe effect from the water air interface shown in the top image of Figure 5.6. The grating lobe effect is close to 90 degrees due to lambda sized pitch of the elements. This confirms that even with a bright reflector from the water/air interface it is still possible to simultaneously image the 4 wire targets on the side with sufficient dynamic range of 30 dB in the lower Figure 5.6. Separate filtering of the forward direction (f_c = 20MHz) and side direction (f_c = 10MHz) can used to better differentiate between the forward and side imaging as well as remove the grating lobe artifact (which has frequency content mainly in the f_c = 20MHz band).

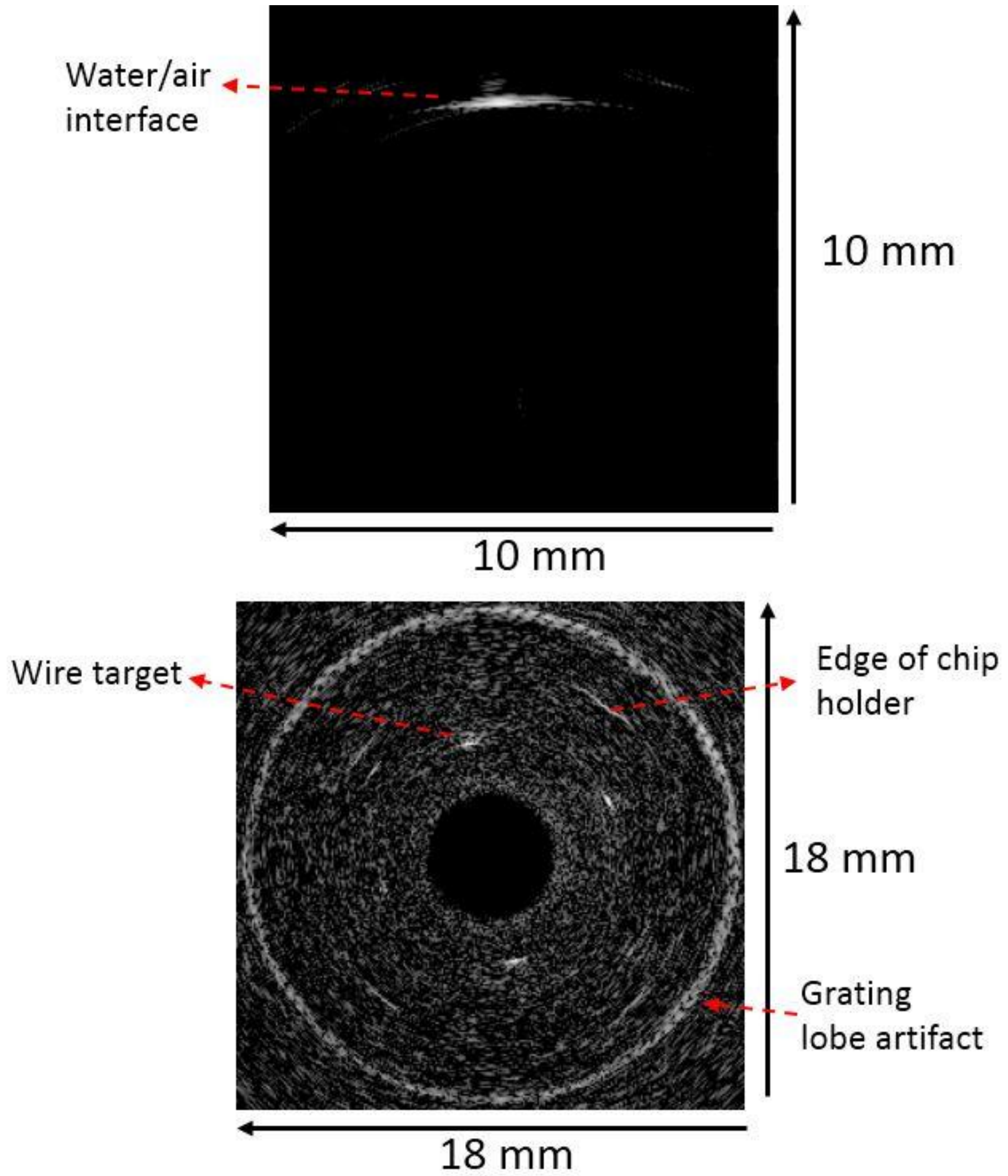


Figure 5.6 X-Z image plane of the water air interface (top), X-Y image plane at Z=0 mm showing the location of 4 wire targets as well as the 4 corners of the chip holder. The grating lobe artifact from the forward direction can be seen here as a bright ring.

5.3. Simulations

5.3.1 Finite Element Simulations

In verification of experimental results, a transient 2D-axisymmetric FEM simulation model was created using COMSOL multiphysics. The physics that the model describes are electrostatic actuation, fluid structure interface and acoustic propagation of ultrasound. Only the structural mechanics and acoustic module are used to create the model since the electrostatic force is introduced into the structural mechanics domain as a forced boundary condition similar to a 1D electrostatic effect in the Z-direction. Reasons for this method, its limitations and accuracy will be discussed.

The CMUT geometry is described as 4 rings of membranes in the 2D-axisymmetric model as shown in Figure 5.7. It closely represents the ring like geometry fabricated in reality; however, it is missing the behavior of individual CMUT elements when modeled this way. This means that the accuracy in modeling behavior is theoretical limited because of non-axisymmetric acoustic crosstalk behavior in reality compared to the FEM model. This is reasonable as an initial study since more accurate 3D geometry of individual CMUT elements require large amounts of fluid and solid elements as well as total degrees of freedom (DOF) count which makes the model size increase exponentially and non-solvable with conventional computer hardware.

In the structural mechanics module, both side walls of the ringed membranes are fixed in displacement in all directions (X-Y-Z). This is quite realistic since the membranes are virtually pinned on the edges during fabrication and the membranes are reasonably thin compared to their widths and lengths (> 1:10). The fluid structure interface of the membrane is managed by adding a boundary force calculated from the acoustics module onto the membrane structure and imposing a matching normal acceleration condition

between the membrane structural surface and the fluid elements. With these two compatibility conditions, the fluid and the structure are coupled together. Finally, a boundary force is applied to the top electrode line of the membranes through the electrostatic force equation.

The CMUT elements are meshed with quadratic quadrilateral elements while the surrounding fluids are meshed with quadratic triangular elements. The quadrilateral elements for the structural membrane will allow more efficient aspect ratios, higher compactness and more accurate results. Unfortunately, due to geometry constraints, only triangular elements can be used to mesh the fluid regions. Quad elements are controlled to a maximum of 3:1 aspect ratio to reach convergence and fluid element size are controlled to be less than at least half the size of the shortest wavelength that needs to be resolved. In this case, max element size was set to 18.75 μm to resolve up to 40MHz accurately.

The generalized-alpha solver was selected in COMSOL with the amplification for high frequency set to 0.1 to damp out numerical oscillation during integration of time steps. A direct solver (MUMPS) method was chosen to solve this particular model, since the model size was at a reasonable size. Total time of 2us is chosen so that no reflection is seen at the outer bounds of the fluid domain. A time step of 1.3ns was chosen for time resolution of the data output so that frequencies of interest can be accurately resolved. Even smaller time steps were internally generated by COMSOL during the time stepping of the numerical solver to provide stability. The simulated geometry and fluid space with a snap shot of the membrane movement and radiated pressure at t = 5.7e-7s is shown in Figure 5.7.

Time pressure data were taken at both on-axis (0 degrees) and transverse (90 degrees) to the transducer source plane. It is clear from visually inspecting the time response of pressure that the on-axis pressure contains higher frequency content than that of the transverse response. A Fast Fourier transform (FFT) of the transient pressure shows this observed behavior is similar to the experiments shown in Figure 5.5, as the center frequency of the on-axis pressure is near 20 MHz and the pressure in the transverse direction is 12.5 MHz as shown in Figure 5.8.

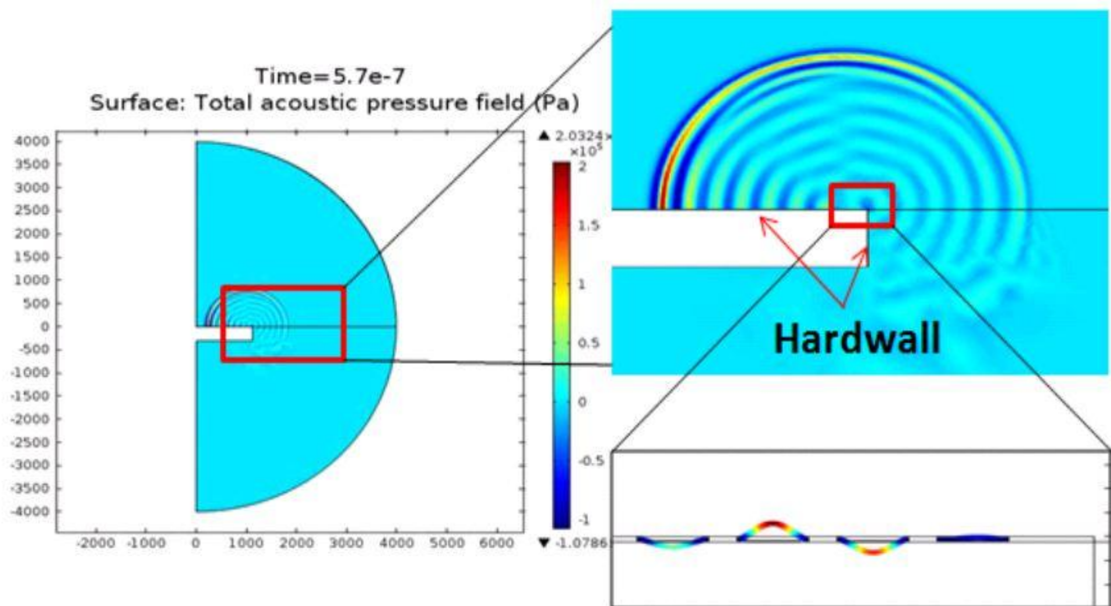


Figure 5.7 FEM result showing radiated pressure at t = 5.7e-7s

To further understand the spatially different frequency behavior, the average membrane velocity for membrane 2 as a function of time is plotted with the corresponding frequency response in Figure 5.9. It can be seen that the membrane has 2 distinct resonances that matches in frequencies of the propagated waves in the forward and side directions. The sharper and lower center frequency peak represents an evanescent wave in the R-direction generated due to the cross-talk behavior of multiple ring shaped

membranes; thus the wave does not propagate in the forward Z direction but rather only transversely to the primary acoustic beam. This behavior can be viewed as a wave having its energy trapped in the very near field of the transducer and propagating only along the surface of the substrate. This is also evident from the volume rendered images of the side wire in Figure 5.3, where the wire images extend a finite distance above the Z=0 plane.

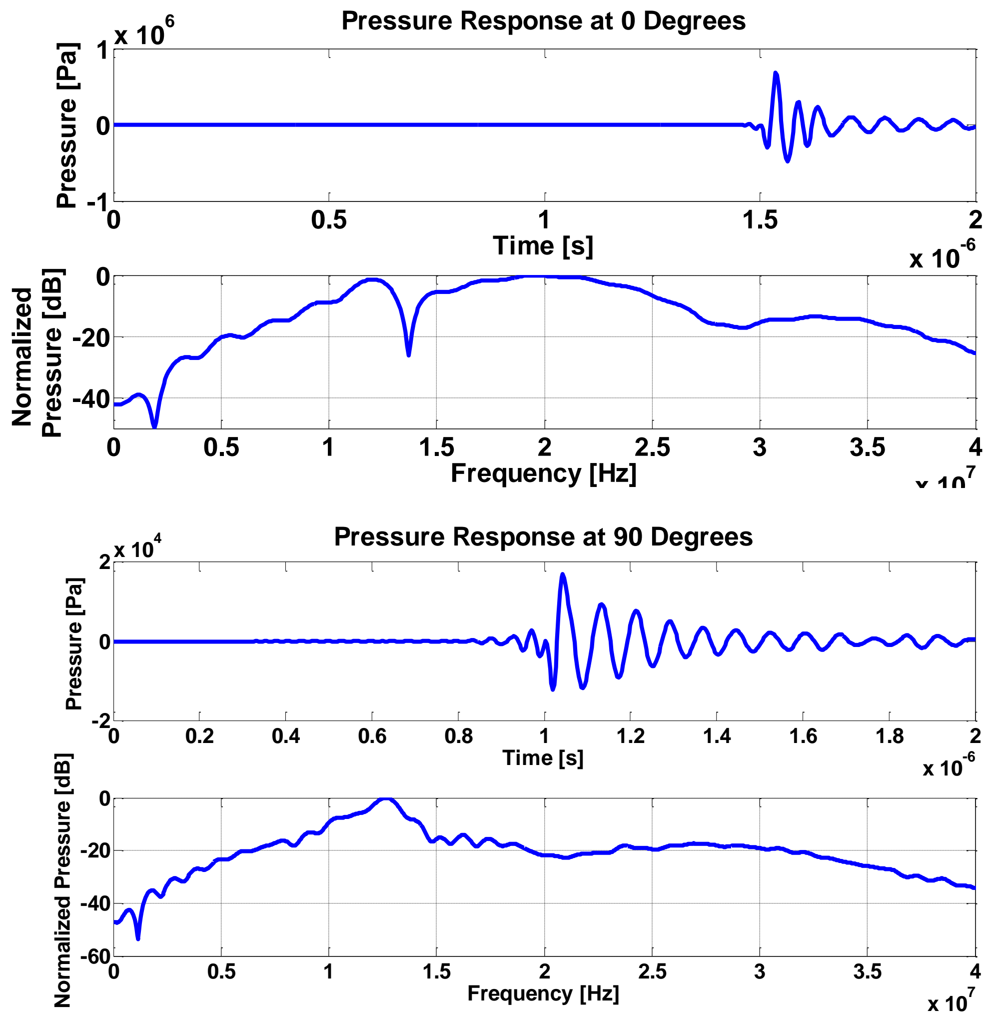


Figure 5.8 Time and frequency response of pressure at 0 Deg. (top). Time and frequency response of pressure at 90 Deg. (bottom).

The second and broader peak represents the higher center frequency that propagates mainly in the forward direction.

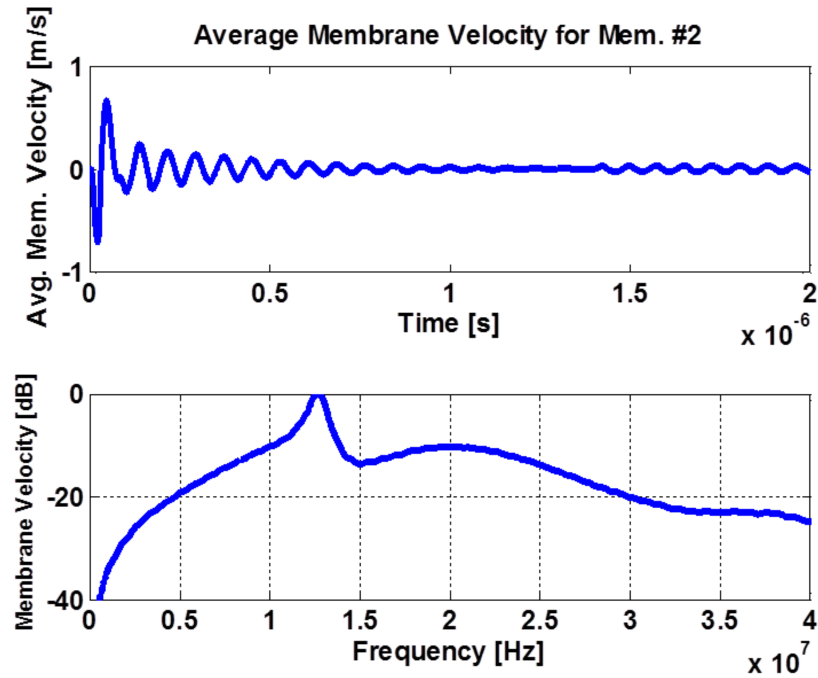


Figure 5.9 Time and frequency response of the average velocity of the actuated membrane surface.

5.3.2 Large Signal Model Simulations

In verification of experimental results, a large signal model for CMUT arrays [58] was used to simulate the pressure output accounting for (1) the dynamic behavior of the transmit element in presence of the mutual acoustical cross-talk coupling and (2) a perfect planar reflector in the forward looking direction. This model is complex and will be discussed in brief in-terms of its main functional blocks and input parameters to match and explain experimental results. Detailed implementation of the method can be found in [58].

The large signal model is divided into three main sections: (1) a non-linear electrostatic force calculation, (2) linear vibroacoustic problem and (3) CMUT force to propagation pressure calculation. The non-linear electrostatic block takes a drive signal

vector, V(t) which contains the applied voltage signal for each membrane's electrodes. The average displacements are used to iteratively calculate the total electrostatic force on each membrane. Nonlinearity comes from the fact that force is proportional to voltage squared and inversely proportional to gap squared. In this model the electrodes are divided into two patches to capture up to the 2nd symmetric mode (5th natural mode) of the membrane accurately in the frequency domain. This has been shown to be accurate in predicting the nonlinear behavior with full gap swing which is close to the conditions used in the experiment where the pulse voltage applied is significantly large causing the membrane to displace a reasonable amount.

The linear vibroacoustic problem describes the relationship between total electrostatic forces acting on each electrode patch and their respective average displacement. This analysis is derived from the linear acoustic analysis of CMUT arrays and uses boundary element method (BEM) where nodal displacements are calculated over a range of frequencies and summed due to superposition validity as the dynamic behavior of the membranes is linear. The BEM problem includes the effect of both self and mutual impedance, which the latter is the source of cross-talk between different membranes even if some membranes are not being directly excited by a voltage source. This part covers the effect of acoustic coupling between membranes without the need to mesh a fluid space as one would normally do in finite element analysis (FEA) analysis, thus reducing computational resource requirements for analysis of large arrays with many membranes.

Lastly, once the total electrostatic force and average membrane displacements are calculated, the solution of the transient model is used to calculate time-domain pressure signals at some point in the fluid. It is important to note that the pressure is not calculated

from average electrode patch displacements but rather all of the nodes in each membrane solving via the Raleigh integral for a baffled point-radiator.

A partial dual ring array was simulated, with 11 TX and 11 RX elements and each element consisting of 4 membranes, shown in Figure 5.10 Each of the membranes was individually designed to f_c=20MHz without accounting for acoustical cross-talk effects. The biasing schemes were similar as the experiment in terms of DC and pulse voltage amplitudes of 120V and 25V respectively. The frequency responses of both the echo wave from 1 cm above the array and the immediate wave travelled to the RX element are plotted in Figure 5.11. These normalized frequency responses were calculated from the temporal current output derived via changes in capacitance due to changes in the displacement of the membrane. Similar to the experimental data, the pulse-echo from the direction normal to the array surface (elevation angle 0 degrees) has an f_c =23.3MHz at -6dB. The center frequency of the side propagating wave (elevation angle 90 degrees) has an f_c=14.7MHz at -3dB first received by the RX element. The center frequency shifted above 20MHz due to the acoustical cross-talk contribution from the surrounding membranes. The center frequency of the side travelling was observed to be much lower than that of the forward direction due to evanescent waves trapped in the near-field of the array surface and propagating in the sideward direction. This wave will shift even lower in frequency (~11MHz) due to attenuation as it propagates further into the fluid medium and with more

influences from extra membranes not simulated in this partial dual-ring configuration as it reaches a side target reflector.

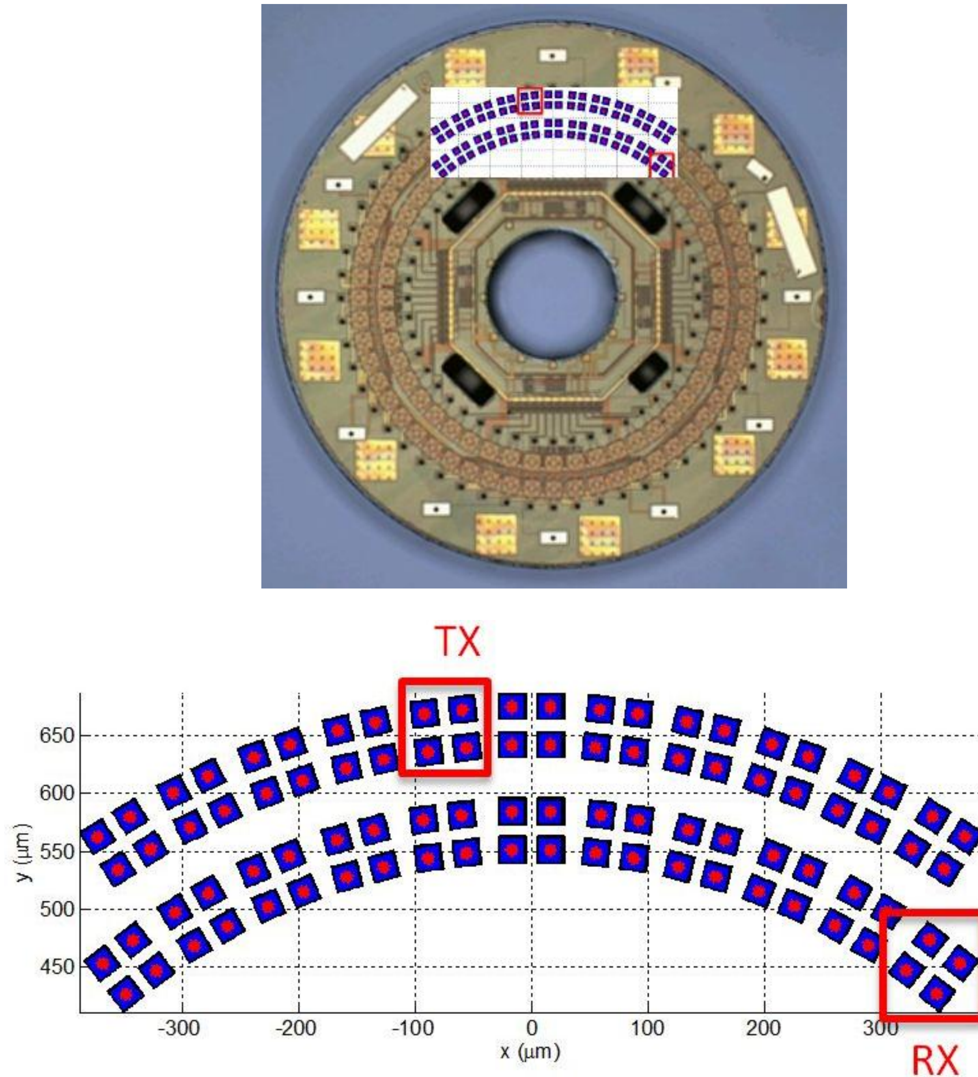


Figure 5.10 Overlay of the partial dual-ring array simulation on full DRA CMUT-on-CMOS chip (top). Schematic of partial dual-ring array with relative locations of simulated transmitter (TX) and the receiving element (RX) (bottom).

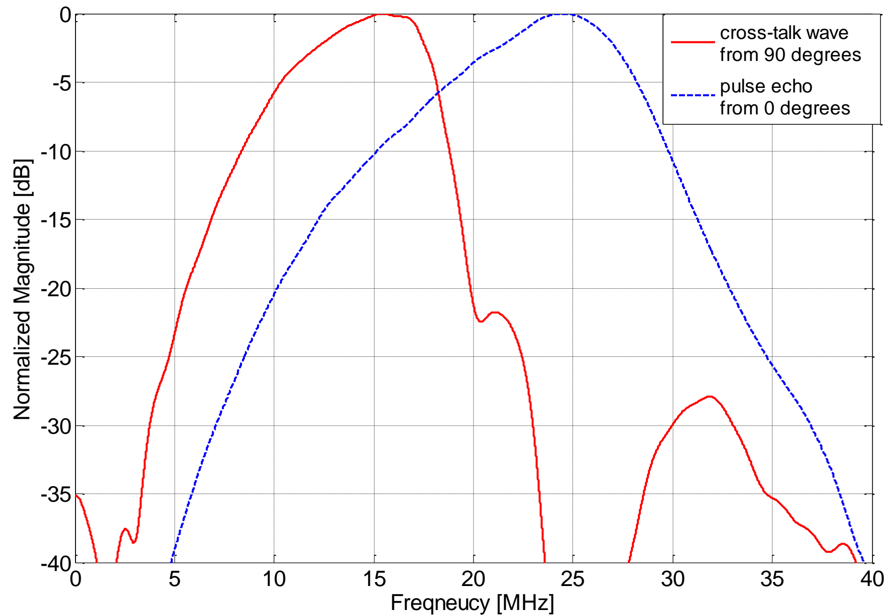


Figure 5.11 Frequency response of cross-talk wave from the RX element (solid) and of the echo from a simulated perfect reflector at 0 degrees (dashed).

In this chapter, experimental demonstration of side looking capability of single chip CMUT on CMOS system based FL dual ring arrays supported by large signal and FEA simulations was presented. The experimental results which are in agreement with simulations show promising results for the viability of using FL-IVUS CMUT-on-CMOS device with dual mode side-forward looking imaging. Imaging experiments with tissue like phantoms and 3D simulations to precisely capture the acoustic effects from individual membranes can be performed for further investigation and optimization of this particular mode of operation.

CHAPTER 6. DUAL FREQUENCY AND DUAL GAP 2D CMUT ARRAYS FOR IVUS

6.1. Background and Motivation for Dual Frequency Design

Dual frequency CMUTs can be an enabler technology in many intravascular ultrasound applications and a good approach for creating a marriage in the design trade-off between high image penetration vs. high image resolution. The goal is to design and fabricate a 2D CMUT array that can allow dual frequency band imaging on a single chip in the range of ~20MHz and ~40MHz. This is a useful feature for IVUS as it allows the lower frequency band to penetrate deeper into the tissue to observe early plaque growth and tissue infarction [120], [121]. Dual frequency capabilities are also useful in intervention procedures such as stent placements [122] where high resolution imaging can be used to look at the thin stent structure, while the lower frequency resolution can be used to penetrate up to 5 mm behind the initial tissue walls. Another related and useful application is during the positioning of RF ablation catheters and post ablation surgery evaluation of the heart tissue can be of benefit by using a dual frequency IVUS array [123]. Lastly, the dual frequency array can be useful in improving harmonic imaging, where acoustical tissue interaction and micro-bubble resonances for contrast agents can generate higher harmonics ($2f_0$, $3f_0$…etc.) than the excited fundamental frequency to perform imaging and differentiation of physiological changes [124].

Previous literature work in design, fabrication and characterization of dual frequency CMUTs have been mainly in the area of creating a marriage between therapeutic ultrasound (<2 MHz) and imaging ultrasound (~10-20MHz) [125]–[127]. The dual mode CMUT device described in those work have very different frequency ranges such that even at 100% fractional bandwidth (FBW) designs (from BW=1-3MHz for fc = 2MHz and

BW=5-15MHz for fc = 10MHz respectively), the two bands will still be sufficiently separate from each other. This becomes easier to design for in terms of less acoustical crosstalk interaction effects as the two types of transducers are outside of each other's main frequency band of interest. This will not be the case for the frequency ranges aimed for in this work due to the wide bands for high center frequencies (20, 30, 40MHz) if a large FBW can be achieved. Large FBW are desirable so that there can be more overlap between each of the 3 frequency bands, as well as increasing axial resolution.

The design of a dual frequency array comes with all of the typical design challenges of a single frequency transducer system plus the added challenges of (1) optimizing each frequency band, (2) optimizing the operational voltages for each type of membrane and (3) additional cross-talk effects from different frequency CMUTs. All of these challenges becomes more difficult to solve as the transducer design parameters that affect each of them such as membrane size, gap, thickness and pitch are all coupled effects to each other. Additional challenges comes from satisfying imaging requirements and pitch size as well as fabrication limitations with the process that has been previously developed for this work.

The design concept for this work follows that of the dual ring array previously described in Chapter 3-5 with the addition of 3 rings of transducers instead of 2. The chip is designed to have 2 receive apertures or rings of CMUT elements and 1 ring of transmitter elements. The goal is to design a transducer system such that the transmitter band (TX30) can overlap as much as possible both the lower frequency receiver band (RX20) and the higher frequency receiver band (RX40) to get the highest pulse echo overall sensitivity. During imaging, the TX30 elements will be actuated one by one and each of the RX20 and RX40 will receive simultaneously with parallel output channels. This is a full synthetic

aperture approach just like the dual ring array described earlier in this thesis except with an extra aperture of receivers. This will be covered in more detail in the system design section. Figure 6.1 shows an example of the desired band shapes to give the desired dual frequency.

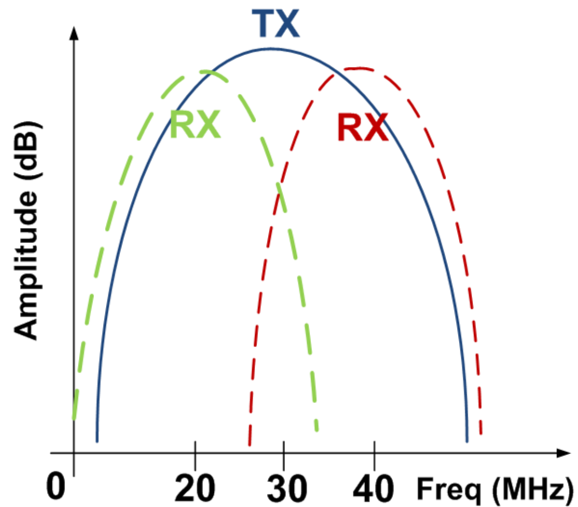


Figure 6.1 Schematic of the desired dual ring frequency device bands.

6.2. CMUT Design Methodology

6.2.1 CMUT Design Process and System Level Requirements

In general, many physical design parameters for a CMUT are closely linked to a variety of desired performance parameters such as collapse voltage ($V_{COLLAPSE}$), receive sensitivity, transmit pressure output and device bandwidth. These physical design parameters such as vacuum gap (g_0), insulation material, insulation thickness (t_d), membrane width (w) and membrane thickness (mem_t) have multiple effects in many of the design parameters. Device performance and device reliability are also two competing design considerations as described in Chapter 4 with the discussion of HfO_2 insulation. From a holistic CMUT system level requirement, there are 4 main areas of focus for design considerations: (1) Ultrasound imaging requirements, (2) Tx and Rx performance, (3) Tx

and Rx operational reliability and (4) CMOS design and are related to each other as shown in a system level diagram in Figure 6.2.

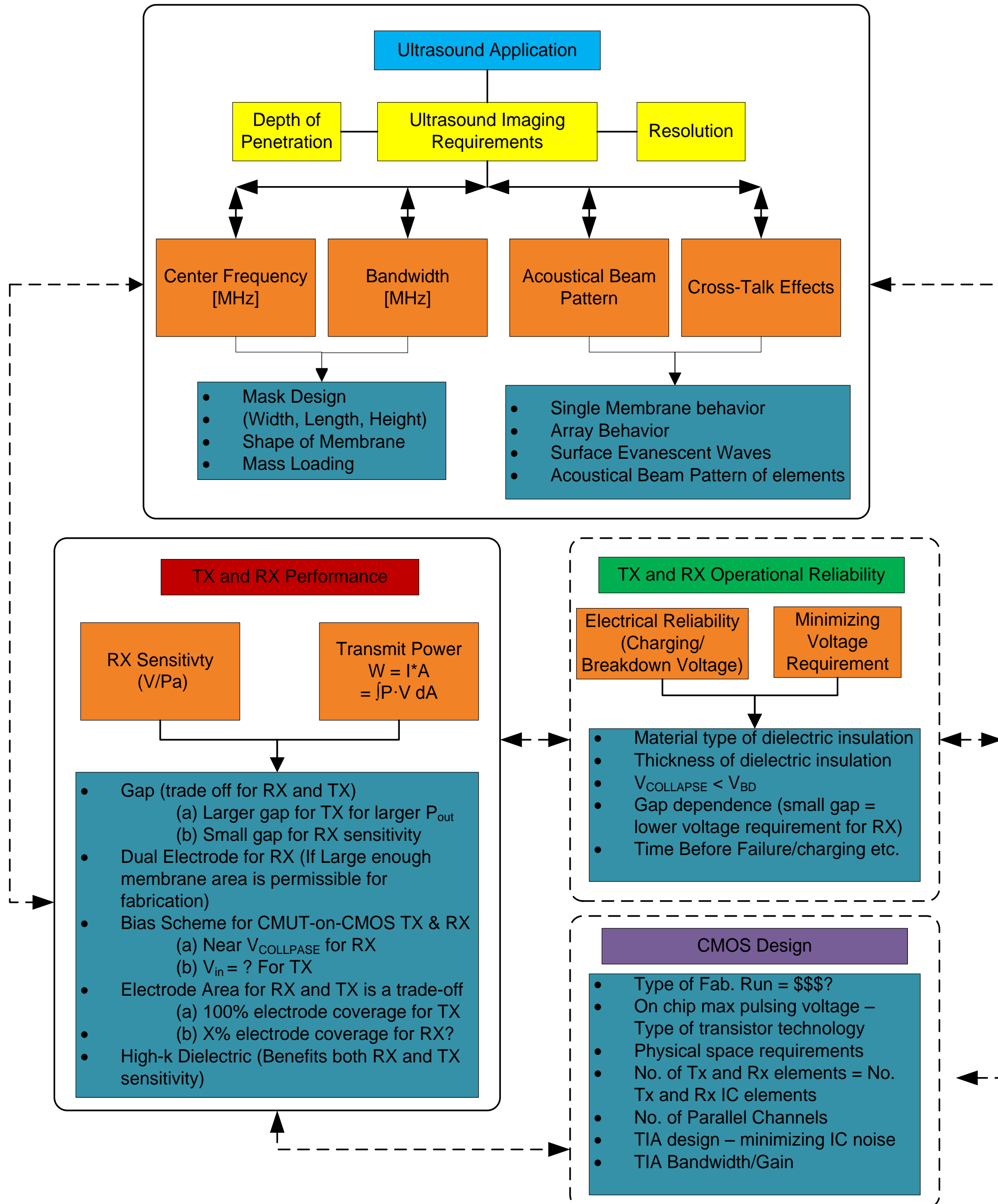


Figure 6.2 System level block diagram description of the 4 main areas of CMUT design focus for medical ultrasound application.

Starting with the ultrasound application, the purpose of the dual frequency device described in this work is for dual mode IVUS imaging. One higher frequency band (~40MHz) and one lower frequency band (~20MHz) will be simultaneously available in one frame by utilizing a synthetic aperture approach with parallel channels. Three different frequency bands will be designed for, which translates to 3 uniquely different geometry sizes and pitch for the CMUT. This also implies that the collapse voltages will vary amongst all 3 types of CMUTs. Since, the 3 frequency bands will have significant overlap, acoustical cross-talk effects will be large from one type of CMUT membrane to the next and cannot be ignored during design and modeling of the array behavior. To minimize grating lobe effects in the image, the pitch for each type of CMUT will be made close to $\lambda/2$. At half wavelength of the desired center frequency grating lobes will be suppressed up to 90^0 degrees in the elevation angle thus beyond the useful range of imaging for a forward looking IVUS device. For a wide band device not all grating lobes can be suppressed purely by this design requirement, but it does help to lower the grating lobe artifact significantly in the desired imaging space if the design follows the $\lambda/2$ element pitch.

With this imaging requirement, the relative pitches for elements are set to ~37.5µm, ~25µm, ~18.75µm for RX20, TX30 and RX40 designs respectively. A table of the desired system design requirements are summarized in Table 6.1 and provides a framework of the boundaries to design within. The rings of CMUT elements should be positioned close to each other in order to maximize their effective TX-RX aperture size. Larger aperture size will increase the axial resolution of the imaging system. A diameter of no more than 1.3mm was chosen so that the catheter can fit close to a 3-F size commonly used in IVUS

procedures. A higher number of parallel RF channels is good for faster data collection; however, it comes at the cost of more cabling and thicker catheters.

Table 6.1 Desired System Requirements for Dual Frequency, Dual Ring 2D IVUS Array Devices.

	Element Type		
Parameter	RX20	TX30	RX40
Desired Element Pitch	~37.5μm	~25μm	~18.75μm
Aperture Diameter	1.1-1.3mm	1-1.1mm	0.9-1mm
Desired Number of Channels	8-10	N/A	8-10
Desired Number of Elements	<100	<100	<120
Frame Rate	> 20	> 20	> 20

Two approaches can be taken from the IC design: (1) have an on-chip switch to switch between collecting RF data from either RX20 and RX40, (2) have separate channels for RX20 and RX40 outputs. Method (1) will require difficult designs on the IC chip (which is outside the scope of this work) and double the number of TX firings to obtain 2 separate frames for the two modes which decreases the frame rate by a half; however, this will result in ~8-12 cables for RF outputs and a smaller catheter. Method (2) mitigates the design and implementation issues with the IC switch, and allows both frames of imaging to be completed in one single set of TX firing; however, this will increase to ~16-24 RF output cables (double from method (1)) and make for a thicker catheter. These system level design considerations are presented to complete the picture of the transducer array design but these requirement are not necessarily needed to determine the transducer element

design. A 100x100 TX-RX combination, 25μs of time (3 cm of distance in water), and with 8 channel output will achieve a frame rate of 32 frames/sec (fps) for 3D volumetric imaging. This is a reasonable frame rate as most modern televisions project video in the ranges of 24-30 fps.

6.2.2 Design of Dual Frequency CMUTs

With imaging requirements in consideration, the approximate element pitches shown in Table 6.1 determine the range and approximate values of membrane widths that are suitable for each design. Due to fabrication considerations, a ~5μm space is designed between each membrane. This gap is used to create the sacrificial etch hole needed to release the sacrificial material. For the size of each element, one can either have a single membrane or multiple membranes to fit the same element pitch space. The trade-offs for 1 membrane versus many membranes are (1) area and (2) acoustical-cross talk behavior. Using one membrane will have a larger area given the 5μm spacing required between each element which translates to either a larger pressure output per given input voltage or a larger output current per Pascal of pressure received on the surface of the membrane. However, using one single membrane will not have the same acoustical-cross talk behavior as the case with many membranes fill the same element area and may have lower acoustical bandwidth compared to many membranes per element. Essentially the trade-offs are pressure output and receive sensitivity versus bandwidth of the acoustical waves.

Single element frequency response compared to simulating the full array cross-talk behavior will have differences; however, it is a good place to start for obtaining the estimated bands of interest. Figure 6.3 shows the frequency bands of each of the RX20, TX30 and RX40 elements individually. This is simulated using the large signal model for CMUTs [58] assuming thin plate model. The pressure was allowed to radiate into water fluid and at z = 1mm distance, the transient pressure response was collected and converted and normalized in the frequency spectrum. The input pulse to the CMUT in each case was a short (broad band) 10ns square wave. Individually, the elements have center frequencies, fc= 22.2, 38.0 and 36.8 MHz for RX20, TX30 and RX40 respectively. The -3dB acoustical

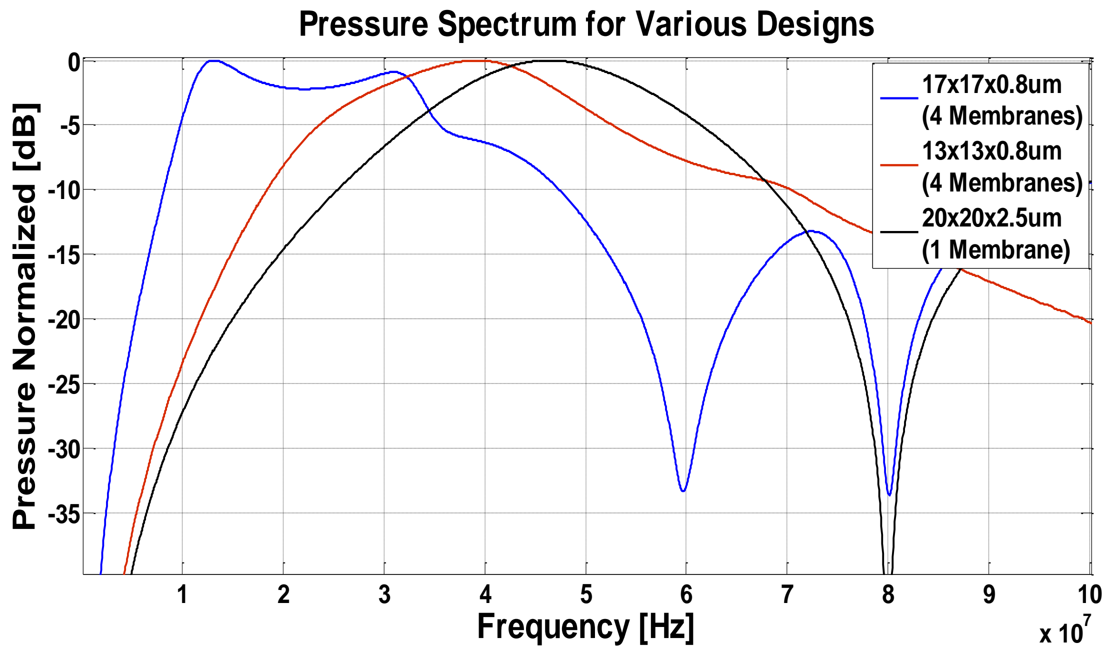


Figure 6.3 Pressure spectrum of each (single) element design and its respective dimensions: RX20 – Blue, TX30 – Red, and RX40- Black.

bandwidths are 23.3, 21.3, and 21.5MHz respectively. The low (f_1) and high (f_2) -3dB frequency ranges are also shown in Table 6.2.

Table 6.2 Single Element Frequency Design

	Element Type		
	RX20	**TX30**	**RX40**
f_c (MHz)	22.2	38.0	46.8
BW (-3dB) (MHz)	23.3	21.3	21.5
f_1 (MHz)	10.6	27.3	36.1
f_2 (MHz)	33.8	48.6	57.6
$V_{COLLAPSE}$ (V)	11	29	43

To investigate the frequency response with more membranes, a partial full ring array was created. Y-axis symmetry was used to reduce computation time and resources. The simulated array geometry is shown in Figure 6.4 with 7x RX20 elements, 8x TX30 elements and 10x RX40 elements. The 3 rings lay at diameters of 1.1mm, 1mm and 0.9mm respectively. The high frequency RX40 elements are located on the inner ring to reduce the number of total elements. Larger area or lower frequency elements (RX20) occupy the outer ring and the TX30 transmitter elements in the middle ring. The rings contains 90, 93 and 113 elements respectively for RX20, TX30 and RX40. A summary of all of the geometric parameters and designed array parameters are shown in Table 6.3.

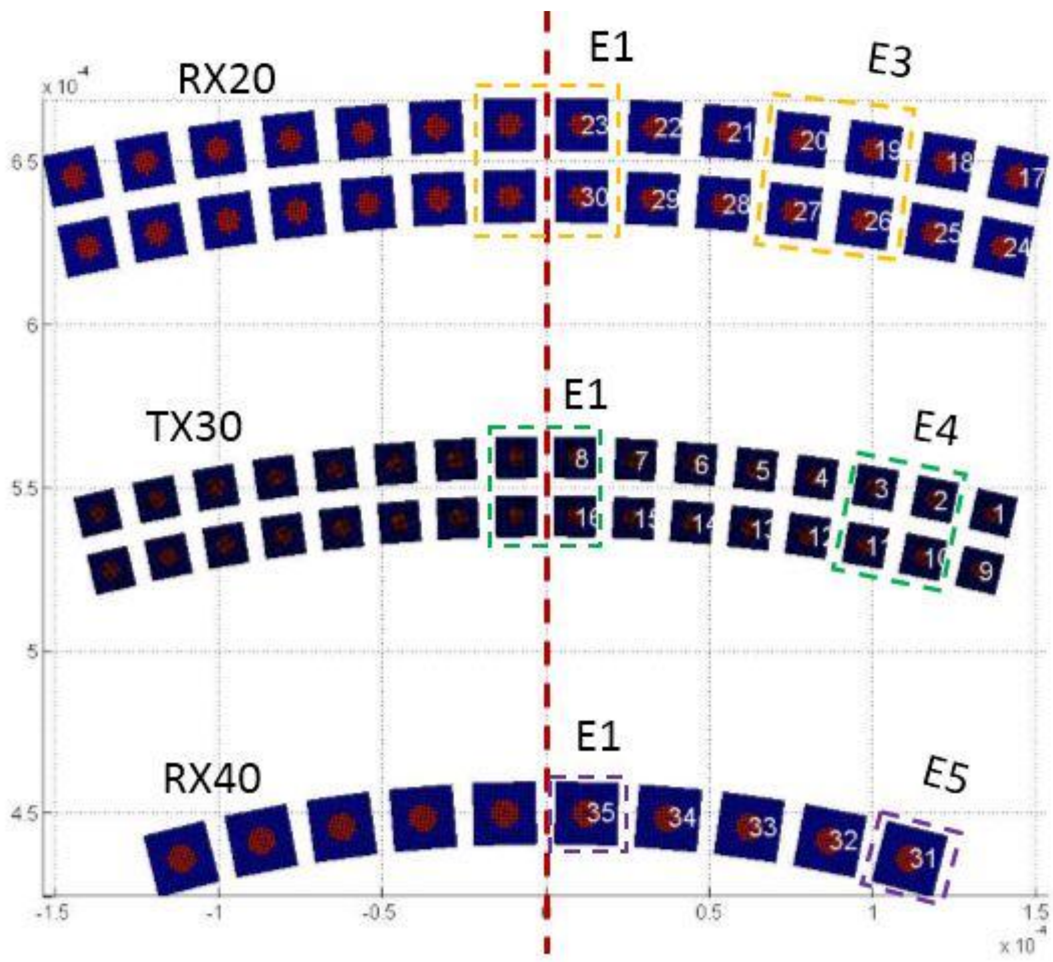


Figure 6.4 Simulated geometry for RX20, TX30 and RX40 elements. Top, middle and bottom rows are RX20, TX30 and RX40 type elements respectively. Dotted line resembles where the symmetry occurs.

Table 6.3 Geometry Parameters for the Simulated Array/Elements

	Element Type		
	RX20	**RX30**	**RX40**
Element Pitch (%λ)	58	72	67
Aperture Diameter (mm)	0.9	1	1.1
Number of Elements Designed for full device (-)	90	93	113
Number of Elements Modeled (-)	8	10	10
Membrane Width (μm)	17	13	20
HfO_2 Insulation Thickness (nm)	100	100	100
Top Electrode Thickness (nm)	0	0	0
Element Area (μm^2)	1156	676	400
Si_xN_y Membrane Thickness (μm)	0.8	0.8	2.5
Vacuum gap (nm)	35	50	35

6.2.3 Acoustical Cross-talk Analysis for Dual Frequency Design

To understand the cross-talk behavior of different frequency designs, the first element (E1) of TX30 CMUT was actuated with a bipolar pulse of 10ns pulse width per pulse and a $20V_{DC}$. Both RX20 and RX40 elements were biased to 90% of its own $V_{COLLPASE}$ as this would be close to the most ideal bias conditions for maximum sensitivity during imaging. The average velocities from each element are calculated in the frequency domain via the following equation:

$$\hat{V} = j\omega\hat{d} \qquad \text{Eqn. 6.1}$$

The average membrane velocities are calculated as a function of frequency and plotted for each type of element as well as the element number that matches with the geometry shown

in Figure 6.4 and Figure 6.5. From observation, TX30 E1 has the largest velocity output with its immediate neighboring TX30 element's velocity at -15dB center frequency level. It is also interesting to note that as the passive elements get further from the active element, the bandwidth also decreases in the TX30 ring. It can be also observed that the immediate neighbors of the active TX30 element contribute the most to the overall cross-talk and RX20 elements as well in the lower frequency range of 10-20MHz due to its wider band shape. RX40 elements do not contribute much to the overall cross talk as its average element surface velocity is on the order of -30 to -40dB below that of the active TX30 element in the main frequency band of interest.

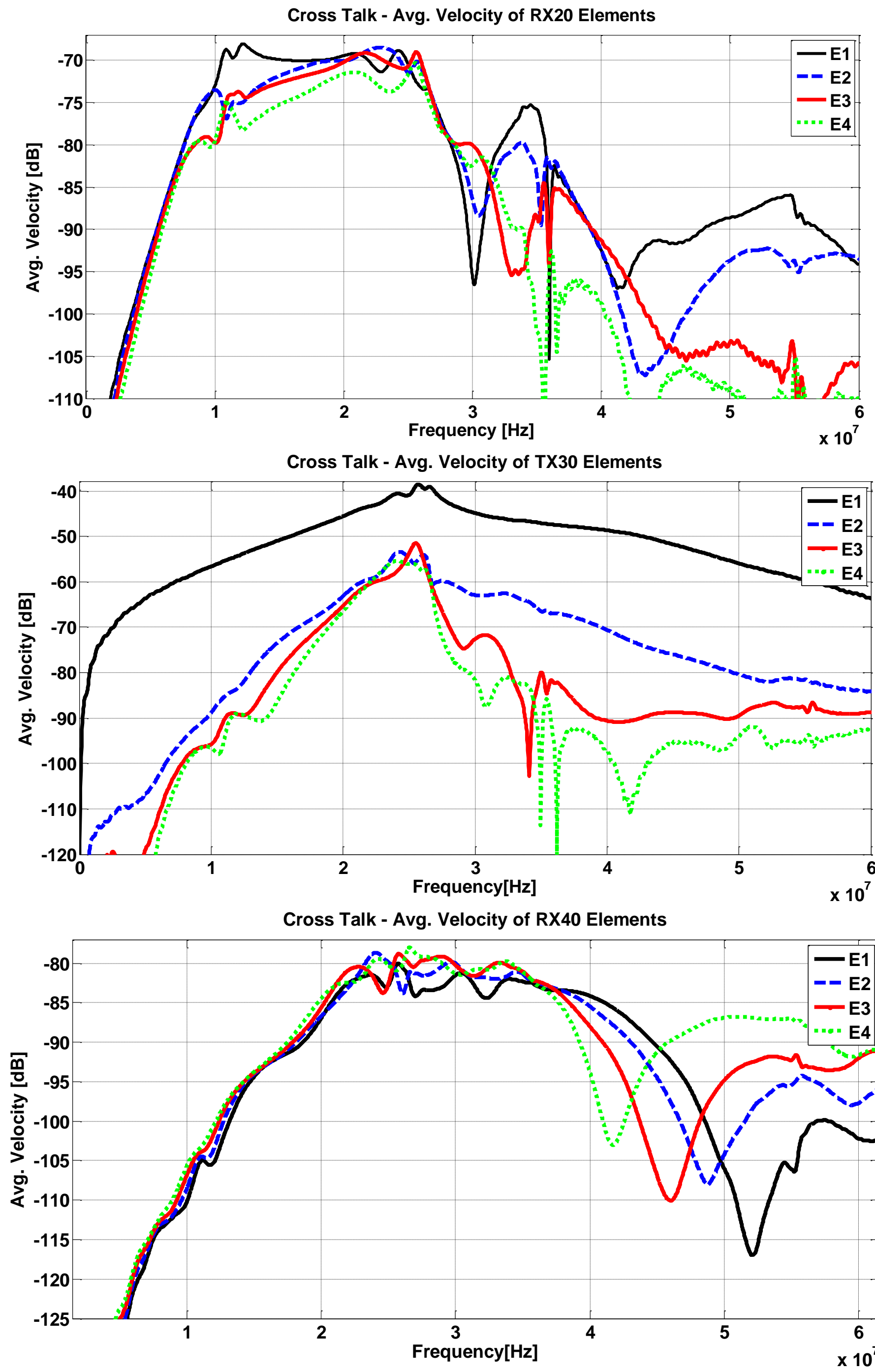


Figure 6.5 Simulated acoustical cross-talk behavior for different elements within each type of element after pulsing from E1-TX30.

6.2.4 Signal to Noise Ratio Calculation

An important transducer design parameter is the signal-to-noise (SNR) ratio of the system. High SNR translates to more contrast and dynamic range for the final ultrasound image and makes it easier for the cardiologist to distinguish between healthy and unhealthy parts of the tissue. To calculate the signal to noise, two parts are required: (1) signal strength and (2) noise level. The signal strength will be calculated via the large signal model [58] during a pulse echo operation, assuming a hard wall condition at z = 5mm. The noise level is calculated assuming that this will be a thermal mechanical (TM) noise limited system. This noise source is caused by the Brownian motion, which is the random vibration of microscopic particles caused by collisions of molecules and atoms in the surrounding space. This assumption implies that the TM-noise floor is higher than that of the TIA noise floor of the designed receive amplifier. This is a reasonable assumption following that previously designed CMUT-on-CMOS TIA can achieve this specification based on similar sized membrane and static capacitance values [60]. Based on this critical assumption, the noise performance of the system will be limited by the TM-noise and thus a best case scenario for estimating the SNR.

The TM-noise is calculated as follows:

$$I_{CMUT_NOISE}{}^{2} = n^{2}4kTRe(Y_{CMUT,MEC}) \qquad \text{Eqn. 6.2}$$

In Eqn. 6.2, “k” is the Boltzman’s constant (1.38×10^{-23} J/K), T is the temperature of the surrounding environment in Kelvin and $Y_{CMUT,MEC}$, is the admittance of the CMUT as seen from the left hand side of the equivalent circuit shown in Figure 6.6. The transformer ratio “n” is equivalent to $V_{DC}C_0/g_{eff}$ where “V_{DC}” is the applied DC bias

voltage, "C_0" is the capacitance of the CMUT and "g_{eff}" is the effective gap of the membrane.

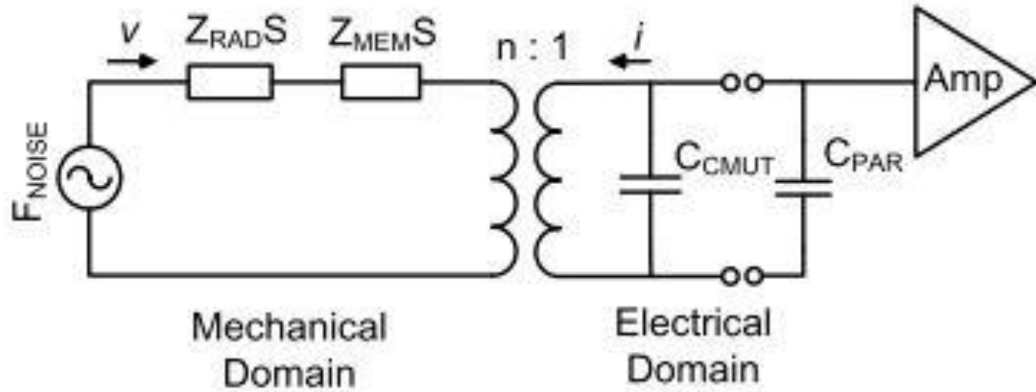


Figure 6.6 Equivalent circuit model for a CMUT element in receive mode. The units of Z_{RAD} and Z_{MEM} are in Rayls and S is the area of the transducer element. The spring softening term on the electrical domain is omitted for this analysis.

Making one more simplification, we notice that the equivalent impedance of the CMUT on the electrical side ($Z_{CMUT,MEC}/n^2$) can be referred to as $Z_{CMUT,ELEC}$. Thus, the CMUT current noise in Eqn. 6.1 can be rewritten as:

$$I^2{}_{CMUT_NOISE} = 4kTRe(Y_{CMUT,ELEC}) \quad \text{Eqn. 6.3}$$

For the dual frequency design proposed, it can be seen that each of the 3 types of membranes will have a different TM-noise source based on their differences in their lateral geometry, gap, membranes thicknesses and different V_{DC} bias levels. Note that $Y_{CMUT,ELEC}$ should also include the effect of radiation impedance seen from all of the membranes in the simulated system which is already included when using the large signal model for CMUTs through boundary element method (BEM) calculations of mutual impedances [128].

To calculate $Y_{CMUT,ELEC}$, the impedance ($Z_{CMUT,ELECT}$) of the CMUT element is determined through applying a very small V_{DC} (1% of $V_{COLLAPSE}$) and a small V_{AC} (1% of V_{DC}) to a particular element type using the large signal model and then subsequently calculate the current as seen from the output of the transducer. A small V_{DC} is used for verification of the model to better match the case when the impedance is strictly imaginary for a static capacitor of constant gap. Both voltage and current are transformed into the frequency domain via the fast Fourier transform. The impedance is calculated as follows:

$$\hat{Z}_{CMUT,ELEC} = \frac{\hat{V}}{\hat{I}} \quad \text{Eqn. 6.4}$$

The current of an element is calculated by taking the time derivative of the charge ("Q") which is a function of the instantaneous capacitance and voltage given by:

$$I(t) = \frac{d}{dt}\big(C(t)V(t)\big) \quad \text{Eqn. 6.5}$$

To verify the validity of the impedance calculation using this model, a RX20 element was used and the real, imaginary and magnitude compared to a static capacitance of the same gap is shown in Figure 6.7. It is noted that for high frequency ranges (>25MHz) the imaginary part of the impedance for the RX20 E1 with surrounding elements matches well with the static capacitance case with a constant gap. The admittance ($Y_{CMUT,ELEC}$) for RX20 element is shown in Figure 6.8.

Utilizing the real part of the calculated admittances for a particular V_{DC} bias point, the current noise power spectrum can be calculated as a function of frequency and various V_{DC} for RX20 and RX40 type receivers. The change in the noise power spectrum as a function of V_{DC} is shown in

Figure **6.9**. Typically, we observe that the noise spectrum shifts

to lower frequency bands as V_{DC} is increased due to the well-known spring softening effect and with increasing amplitude due to higher coupling coefficient and conversion between mechanical to electrical mesh.

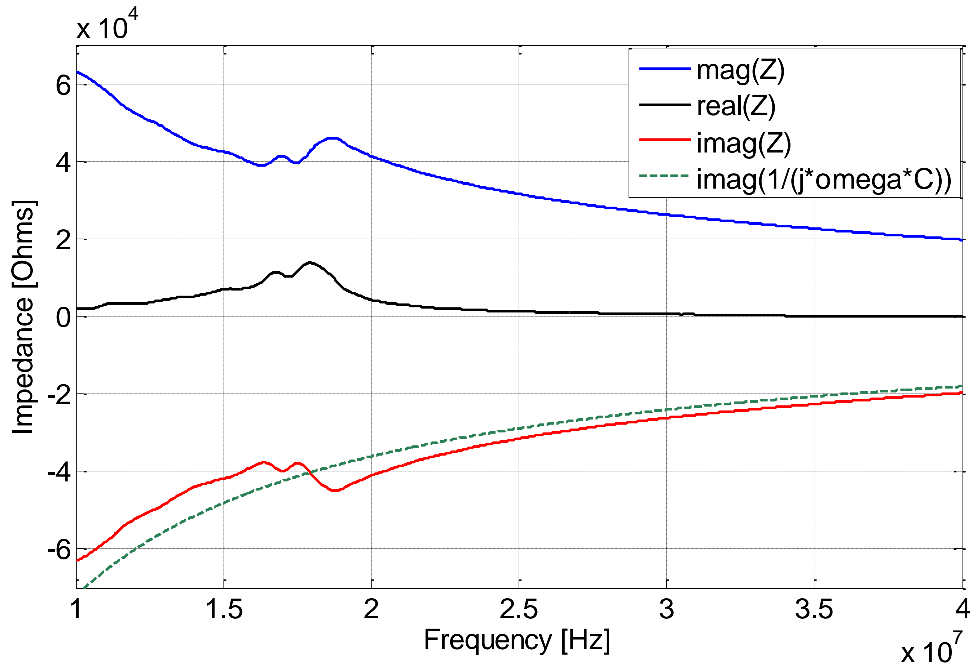


Figure 6.7 Impedance calculation (in water) for RX20 element with acoustical cross-talk effect and verification compared to a constant gap CMUT capacitor.

To calculate total SNR for a single Tx-Rx pair, the following equation was used:

Eqn. 6.6

$$SNR\ (dB) = 10 * log_{10}\left(\frac{I^2{}_{SIGNAL_RMS}}{\sum_f I^2{}_{CMUT_NOISE}}\right)$$

For a realistic estimate of the array performance for IVUS, the SNR is calculated assuming blood attenuation (α) with the units of dB/m/MHz, based on Treeby *et al.*'s power law model [129]:

$$\alpha = 5.46 * \left(\frac{f}{1e6}\right)^2 \qquad \text{Eqn. 6.7}$$

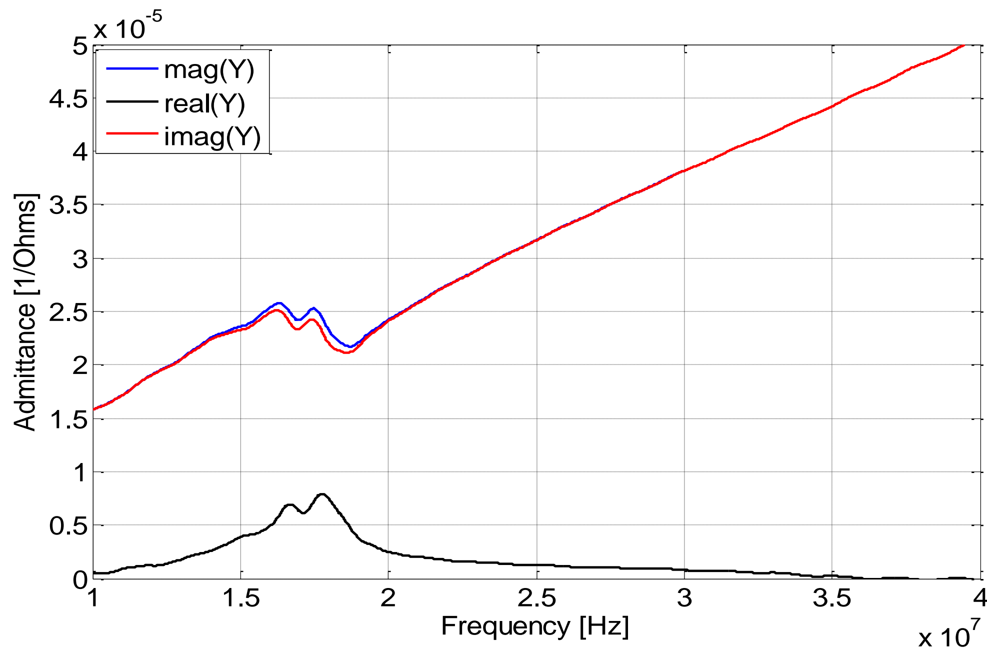


Figure 6.8 Admittance (in water) of RX20 element with acoustical cross-talk effect.

Two parameters that can have large effects on receive sensitivity and the TM-noise are (1) vacuum gap and (2) V_{DC} applied (or $V_{DC}/V_{COLLAPSE}$) for receiver elements. A parametric study is performed to understand how each of the parameters above affect the overall SNR performance of a single Tx-Rx pair in the simulated array (with acoustical cross-talk from neighbors).

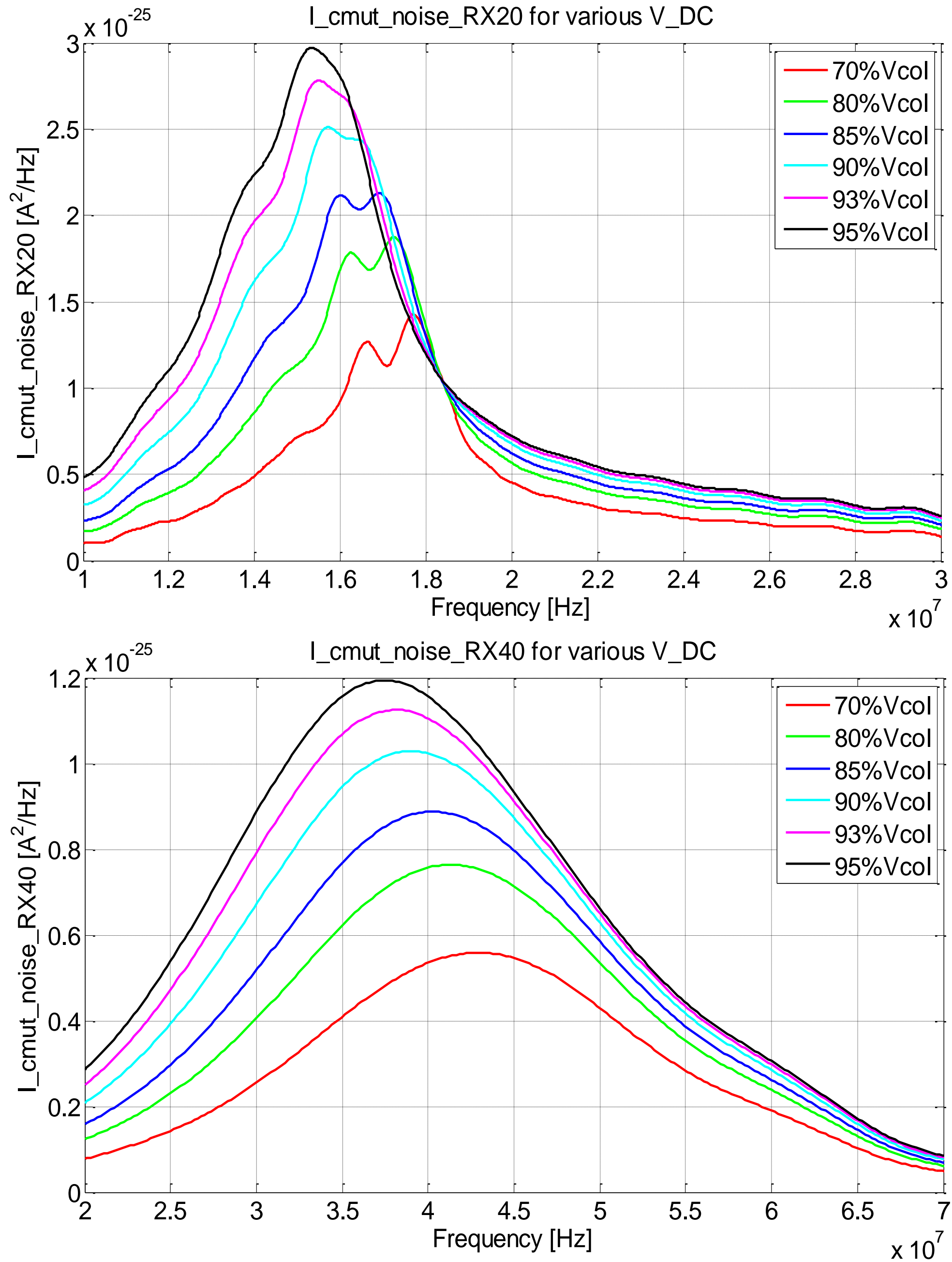


Figure 6.9 $I^2_{CMUT_NOISE}$ (TM-noise current) power spectrum for various V_{DC} bias points for RX20 element (top), $I^2_{CMUT_NOISE}$ (TM-noise current) power spectrum for various V_{DC} bias points for RX40 element (bottom).

6.2.4.1 SNR Vs. Vacuum Gap Height for Receive Elements

The SNR is calculated by placing a hard wall reflector at z = 5 mm in the model and pulsing the transmitter (TX30 E1) with a 10ns bi-polar pulse of +34V and -20V amplitude with a V_{DC} of 20V. This pulse allowed for the maximum pressure output and full displacement of the membrane without collapsing the membrane during dynamic operation. All receiver type elements were biased to 90% of its own $V_{COLLAPSE}$ for good sensitivity performance. Adjusting to the higher attenuation in blood (especially for high frequencies), both RX20 and TX30 membrane thicknesses were adjusted to 1µm instead of 0.8µm originally calculated for water attenuation. From Figure 6.10,One can see that the

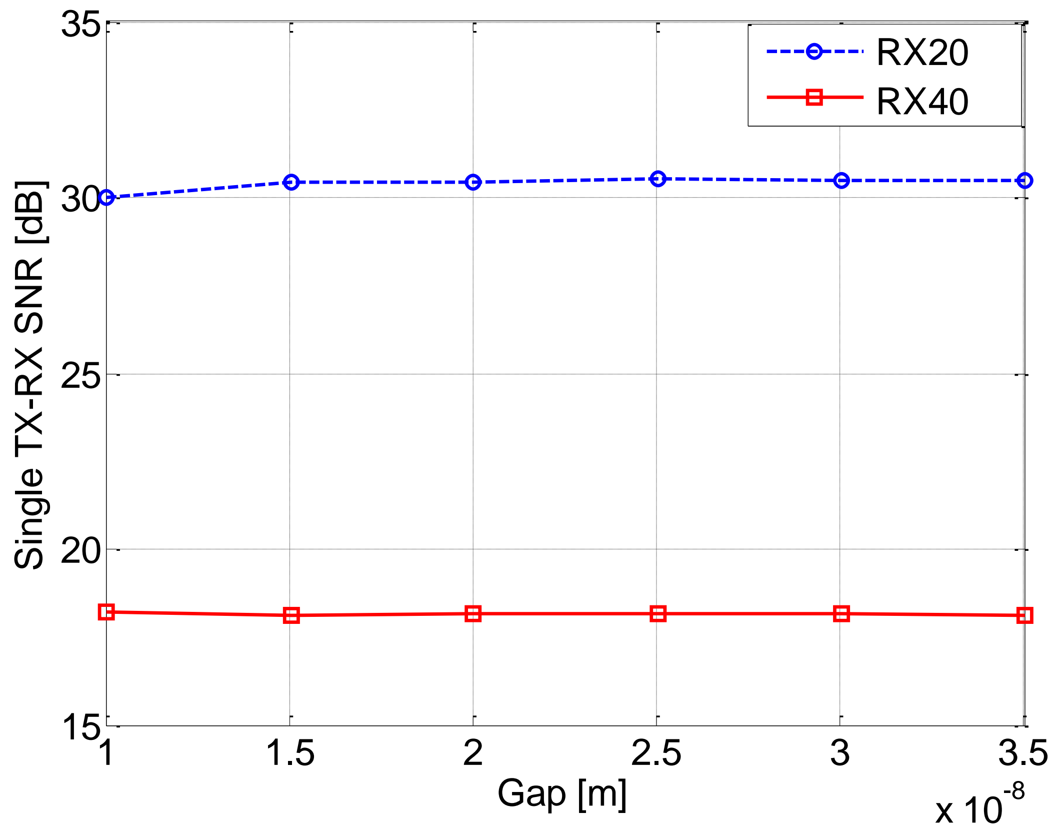


Figure 6.10 SNR calculated for different vacuum gaps for RX20 and RX40 receiver element. Acoustical cross-talk is taken into account with neighboring elements.

SNR does not change very much when the gap is decreased which is unexpected based on the assumption that the Rx element is more sensitive at 90% of $V_{COLLAPSE}$ with smaller gaps due to higher Pa/V conversion at lower gaps. This is true and shown in Figure 6.11 (top) that more Rx current is produced for each type of receiver as the gap is reduced; However, the TM-noise level also increases proportionally when gap decreases as shown in Figure 6.11 (bottom), thus causing the overall SNR to remain relatively constant. One can conclude for this particular array designed, the further reduction in gap does not give higher SNR assuming a TM-noise limited system. The only gain in reducing the gap will be to reduce the absolute $V_{COLLAPSE}$ in consideration for system design and voltage level designs on the IC chip as well as catheter shielding and packaging considerations. Another advantage for lower vacuum gaps is that a higher TM-noise can reduce the design requirements to minimize IC-noise below the TM-noise for the system to be TM-noise limited. If the system is IC-noise limited and the noise level is constant, then lowering the gap will increase the SNR.

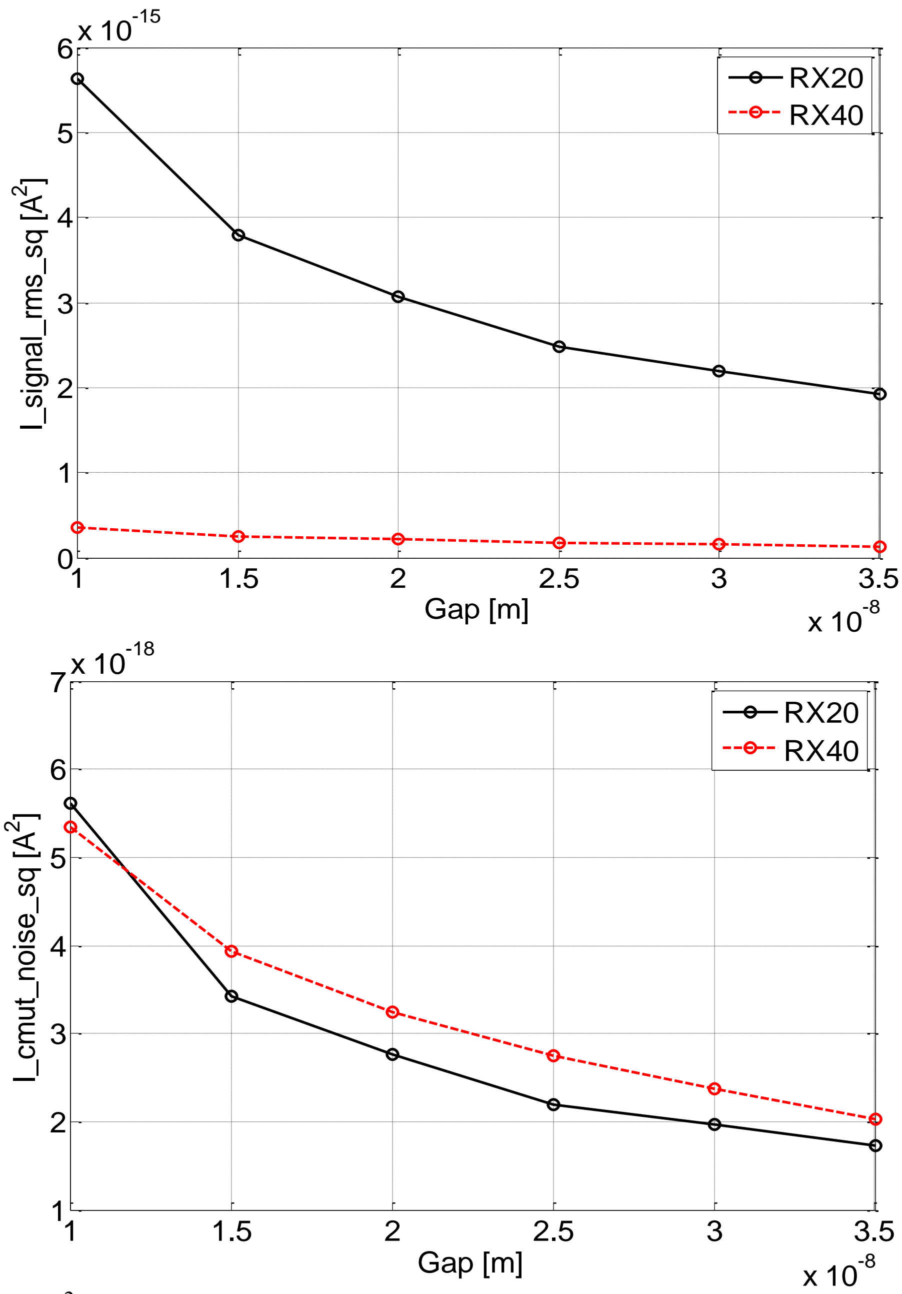


Figure 6.11 $I^2_{SIGNAL_RMS}$ as a function of different gaps for RX20 and RX40 receivers as calculated via pulse-echo at z=5mm in blood (top), $\Sigma_f I^2_{CMUT_NOISE}$ (TM-noise current) as a function of different gaps for RX20 and RX40 receivers as calculated via pulse-echo at z=5mm in blood (bottom).

6.2.4.2 SNR Vs. V_{DC} Applied to Receive Elements

A parametric study similar to SNR Vs. vacuum gap is now repeated for SNR Vs. applied V_{DC} to the receiver elements. The gap is fixed at 35 nm for both receivers in this case and all other geometric and modelling parameters unchanged. The independent parameter shown in Figure 6.12 is the fraction $V_{DC}/V_{COLLPASE}$ with 1 for the case V_{DC}= $V_{COLLAPSE}$.

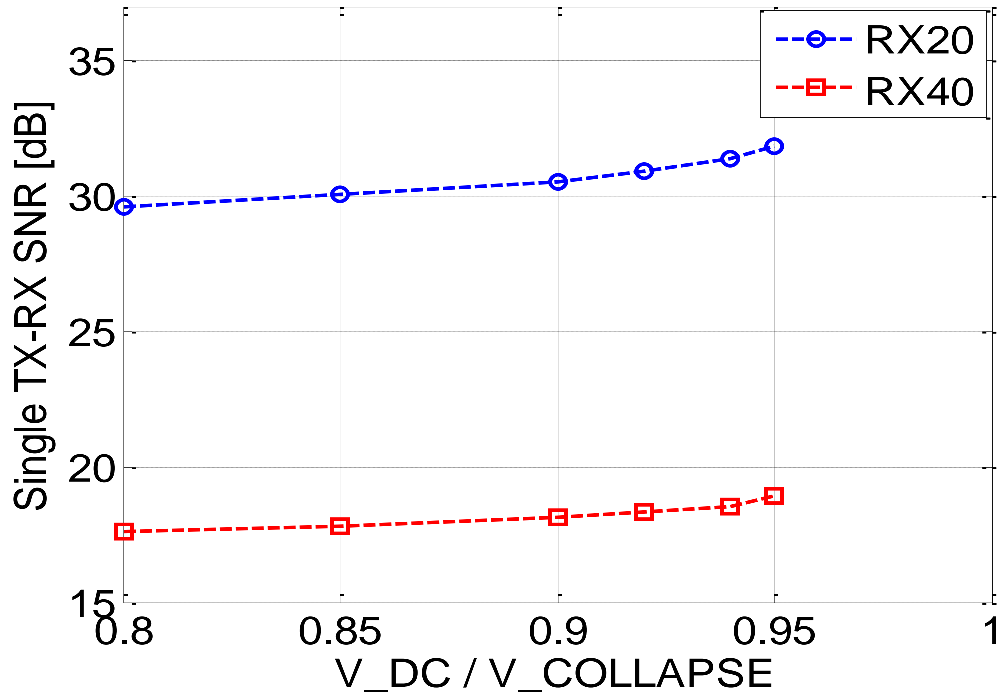


Figure 6.12 SNR calculated for different V_{DC} bias conditions for RX20 and RX40 receiver element with a constant gap of 35nm.

One can observe that there is an increase in SNR as V_{DC} approaches to $V_{COLLAPSE}$; however, from 80% to 95% $V_{COLLAPSE}$ there is only an increase of 7.4% for single Tx-Rx SNR for the 2 types of Rx elements. With reliable CMUT operation in consideration, it is not necessary to operate the receive mode beyond 90% $V_{COLLAPSE}$ as the marginal gain in SNR will be small. The gains in SNR are not large, again due to the fact that TM-noise increases (I_{CMUT_NOISE}) proportionally as V_{DC} is increased shown in Figure 6.9. Thus this

cancels out some of the effect of having higher signal current (I_{SIGNAL_RMS}) from the pulse echo as V_{DC} is increased.

In summary, the SNR is calculated for (1) Single Tx-Rx pulse echo, (2) Single Tx and All Rx and (3) All Tx-Rx combination assuming full synthetic aperture imaging for the geometry described in Table 6.3. Attenuation in blood and a perfect reflector at z = 5mm is assumed in this calculation. SNR calculated for TX30 assumed TX30 elements where hypothetically used as receivers to compare to the dual frequency array performance of RX20 and RX40 case.

$$(2)\ SNR_{single\ Tx\ \&\ All\ Rx} = SNR_{single\ TxRx} + 20 * log10(\sqrt{\#Rx}) \quad \text{Eqn. 6.8}$$

$$(3)\ SNR_{All\ Tx\ \&\ Rx} = SNR_{single\ TxRx} + 20 * log10\left(\sqrt{\#Rx}\right) + 20 * log10(\#Tx) \quad \text{Eqn. 6.9}$$

Table 6.4 SNR Values Calculated via Large Signal CMUT Model

	Designed/Modeled		
SNR (dB) @ z = 5mm (blood)	**RX20**	**TX30**	**RX40**
Single Element Tx & Rx	30	14	18
Single Tx, All Rx	49.5	33.7	38.5
All Tx, All Rx	88.9	74.7	77.6
Image SNR (with -30dB reflector)	58.9	44.7	47.6

6.2.5 Pulse-Echo Frequency Response

As mentioned at the beginning of this chapter, it is important in CMUT design to have a good fractional bandwidth in the pulse-echo frequency response so that axial

resolution does not suffer. Typically, it is easier to achieve high fractional bandwidth (FBW) in lower center frequency (f_c) CMUTs compared to high f_c CMUTs. The simulated pulse-echo frequency responses for each element of both RX20 and RX40 elements with TX30 E1 pulsed with an input pulse shown in Figure 6.13. A perfect reflector is located at a plane of z = 5mm and the attenuation in blood was used.

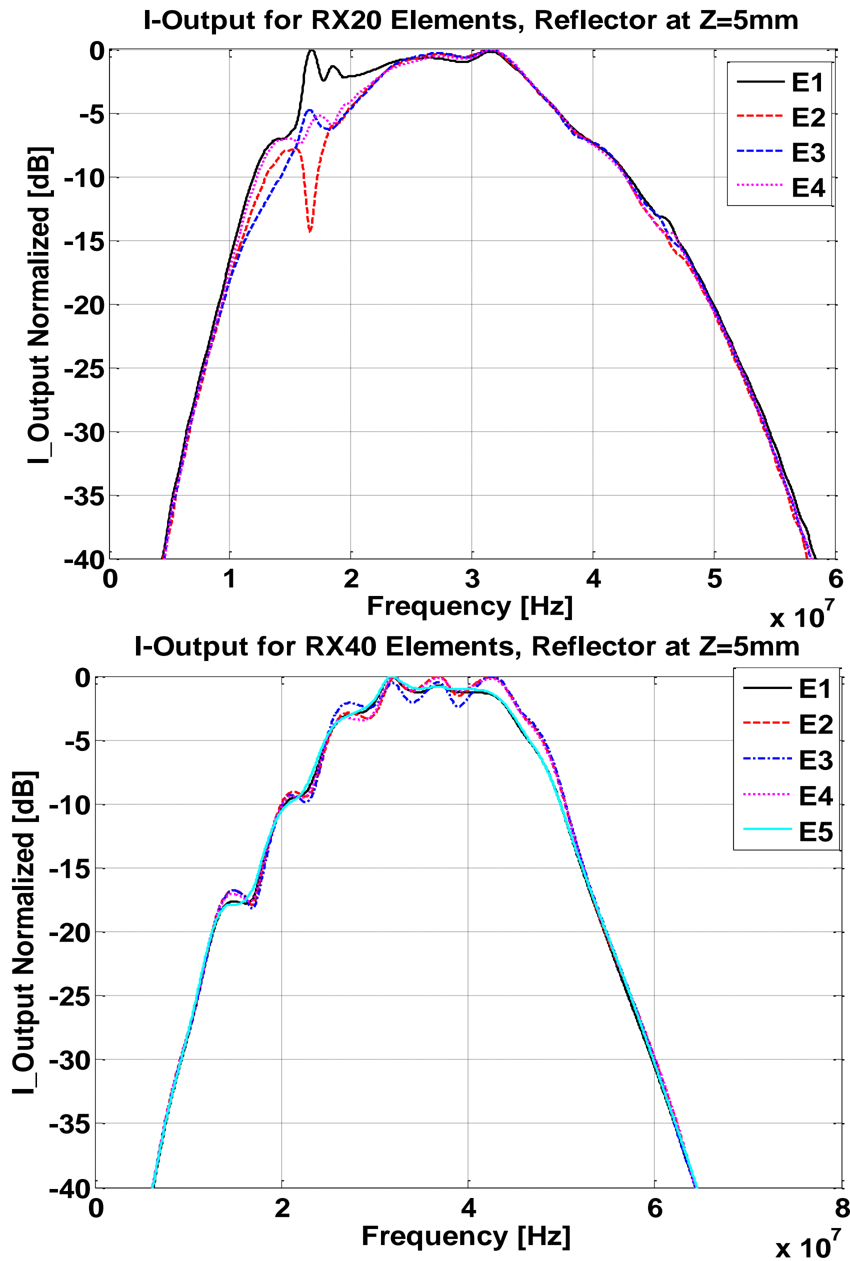


Figure 6.13 Frequency spectrum of I_{OUTPUT} for RX20 elements (top), Frequency spectrum of I_{OUTPUT} for RX40 elements (bottom).

The frequency response is calculated by converting the displacement of the membrane from the echo to a change in capacitance and then to a change in current output (I_{OUTPUT}) via Eqn. 6.5. In this calculation, it is assumed that no extra electrical loading was introduced by TIAs and thus a simplification of the actual current output. It should be noted that if a TIA with a certain characteristic impedance is placed at the output of the CMUT receiver, the I_{OUTPUT} spectrum shown in Figure 6.13 will change. Thus, the spectrum shown in Figure 6.13 is an ideal case. The average -6 dB bandwidth for RX20 element is 22.6 MHz and the average -6 dB bandwidth for RX40 is 24.6 MHz.

6.3. Dual Frequency CMUT Fabrication

As discussed earlier in the chapter, the design of a dual frequency dual ring array requires separate geometric design to satisfy different image requirements (resolution and depth of penetration), optimized transmit and receive operation conditions and optimum voltage conditions. One of those requirements is that the transmitter will need a larger gap than the two receiver type elements in order to achieve large pressure output while not sacrificing high sensitivity and low collapse voltage on receive mode. It was shown that a 50nm gap for Tx and 30nm gap for Rx is a good combination for the overall design, allowing good SNR and low voltage operations.

6.3.1 Fabrication Process Overview

The basis of the dual frequency fabrication process is similar to the standard fabrication process covered in Chapter 4 and 5. The novel steps are to define the dual gaps and dual thicknesses of the membranes. These two novel processes require a total of 3 additional masks, 1 for defining the second gap height and 2 for defining the dual thicknesses. The dual frequency fabrication process requires a total of 8 photo masks compared to 5 previously for CMUTs.

The overall fabrication process is shown in Figure 6.14: (1) We begin with a 4" <100> Silicon wafer and thermally grow 3μm of silicon dioxide for electrical passivation and reducing parasitic capacitance. Then 120-150nm of chromium is uniformly sputtered and patterned via wet etch using Cr-7s etchant. (2) Then a 50nm layer of copper is sputtered and patterned via wet etch using APS-100 1:60 dilute with deionized (DI) water. (3) Next, a methane (CH_4) based plasma etching chemistry is used to etch the RX20 and TX30 copper sacrificial layers from 50nm to 30nm as designed. This is described in detail in the next section. A ~100nm of HfO_2 is deposited via ALD at 250^0C. (5) The top electrode is formed by sputtering 150nm of AlSi 2% and wet etching via Al-type-A etchant. (6) A 0.7μm layer of Si_xN_y is deposited via PECVD at 250^0C. This is the desired thickness for RX20 and TX30 designs. (7) Then another layer of 60nm AlSi 2% is sputtered and patterned on top of the RX20 and TX30 layer to act as an etch stop for later steps. This is described in more details in the subsequent sections. Additional 0.5μm of Si_xN_y is deposited for structural integrity before the release process. (8) Next the sacrificial etch hole is patterned and carefully timed to etch through the Si_xN_y to the etch stop. Wet etch is used to etch open this layer before continuing to etch through the rest of the Si_xN_y until HfO_2 is reached, shown in Figure 6.15. RIE chemistry must then be switched from CHF_3

to SF_6 to finish etching to the copper sacrificial layer. Each of this multiple material stack etching must be well timed to ensure enough photoresist mask can remain for the whole etching process. Once the RIE has reached the copper layer, APS 100 is used to release the membranes. Test structures without top electrodes enables one to understand visually when the release etching has completed, shown in Figure 6.16. A 12 hour soak in isopropanol alcohol (IPA) and release in a super critical drying system will reduce the chances of stiction of the membrane from collapsing during the release stage. (9) An additional 1.2μm of Si_xN_y is deposited to both (a) seal the etch holes in a vacuum environment and (b) increase the thickness of the membrane to 2.4μm of Si_xN_y for the RX40 design. (10) The third new mask is used to etch down the extra Si_xN_y on top of the RX20 and TX30 area till the etch stop is reached. This is also discussed in greater detail in the subsequent sections. (11) Wet etch is then used to subsequently remove the etch stop. (12) Finally, the bond

pads are opened and more Ti/Au are deposited and patterned through lift-off method onto the bond pads for reliability and robust wire bonding during the packaging stage.

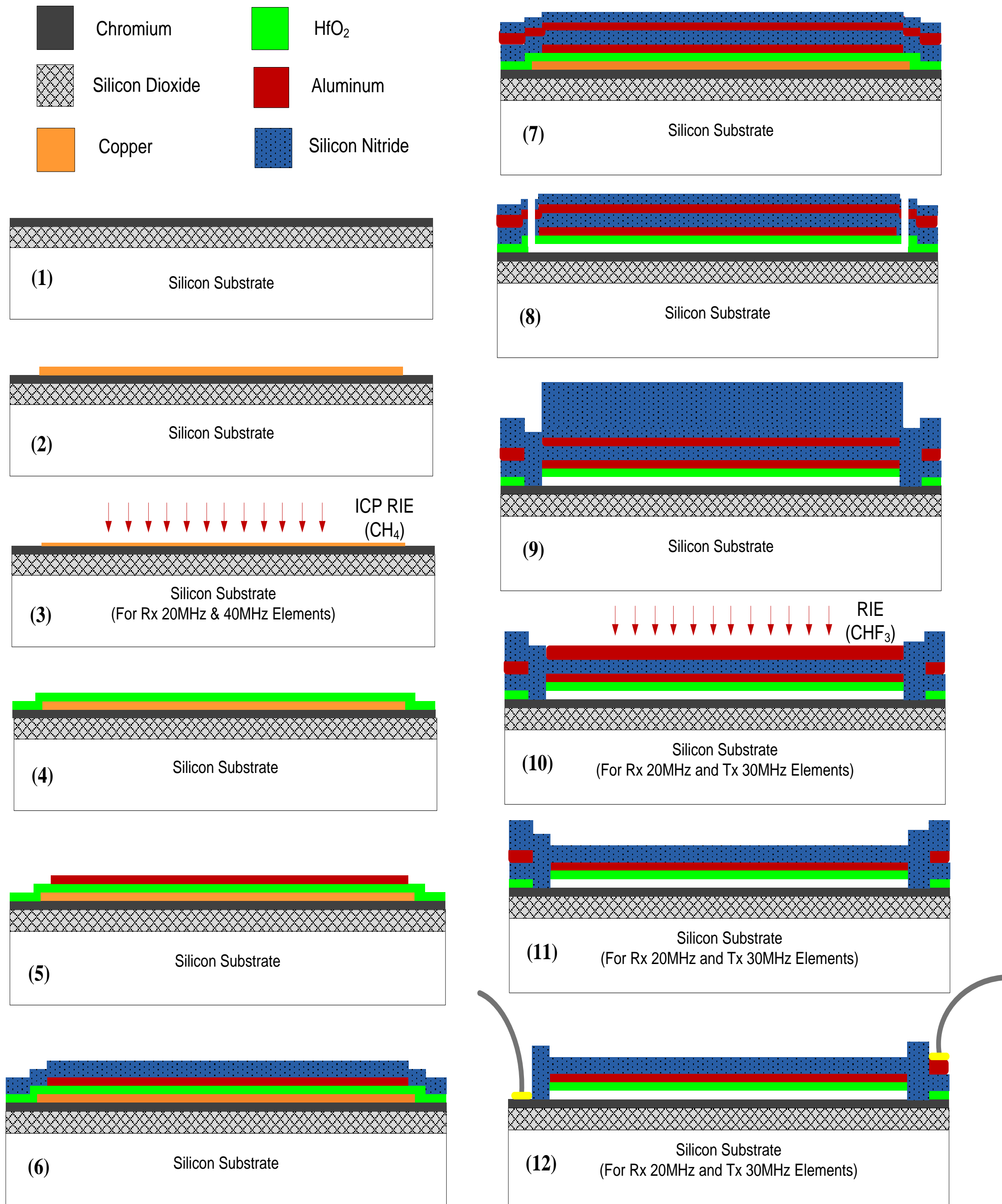


Figure 6.14 Schematic of dual frequency fabrication process for dual ring IVUS.

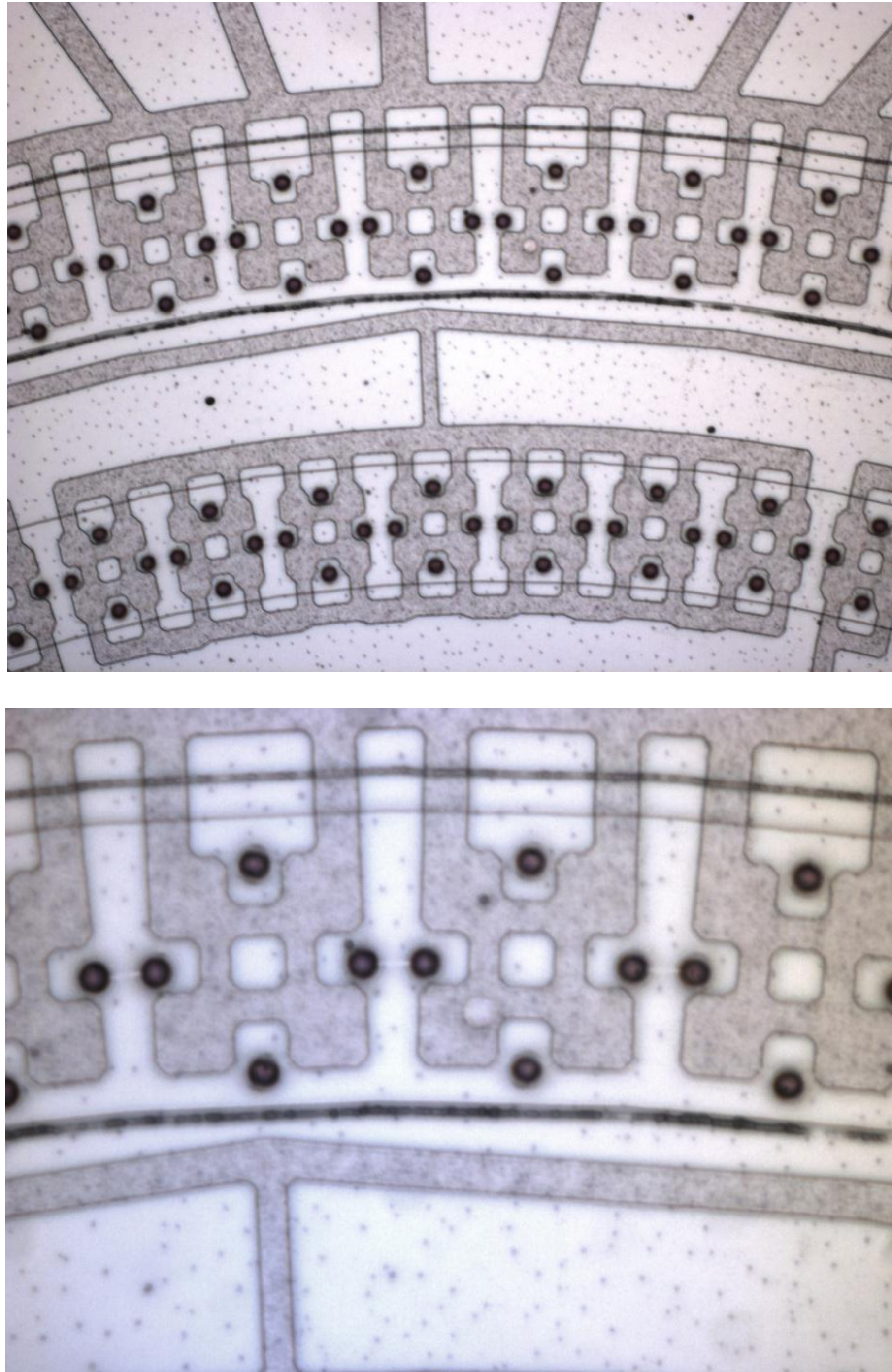


Figure 6.15 Micrograph of the CMUT during step (8) (top). Zoomed in image of the top figure (bottom). It can be seen that the copper is visible in the etch hole region.

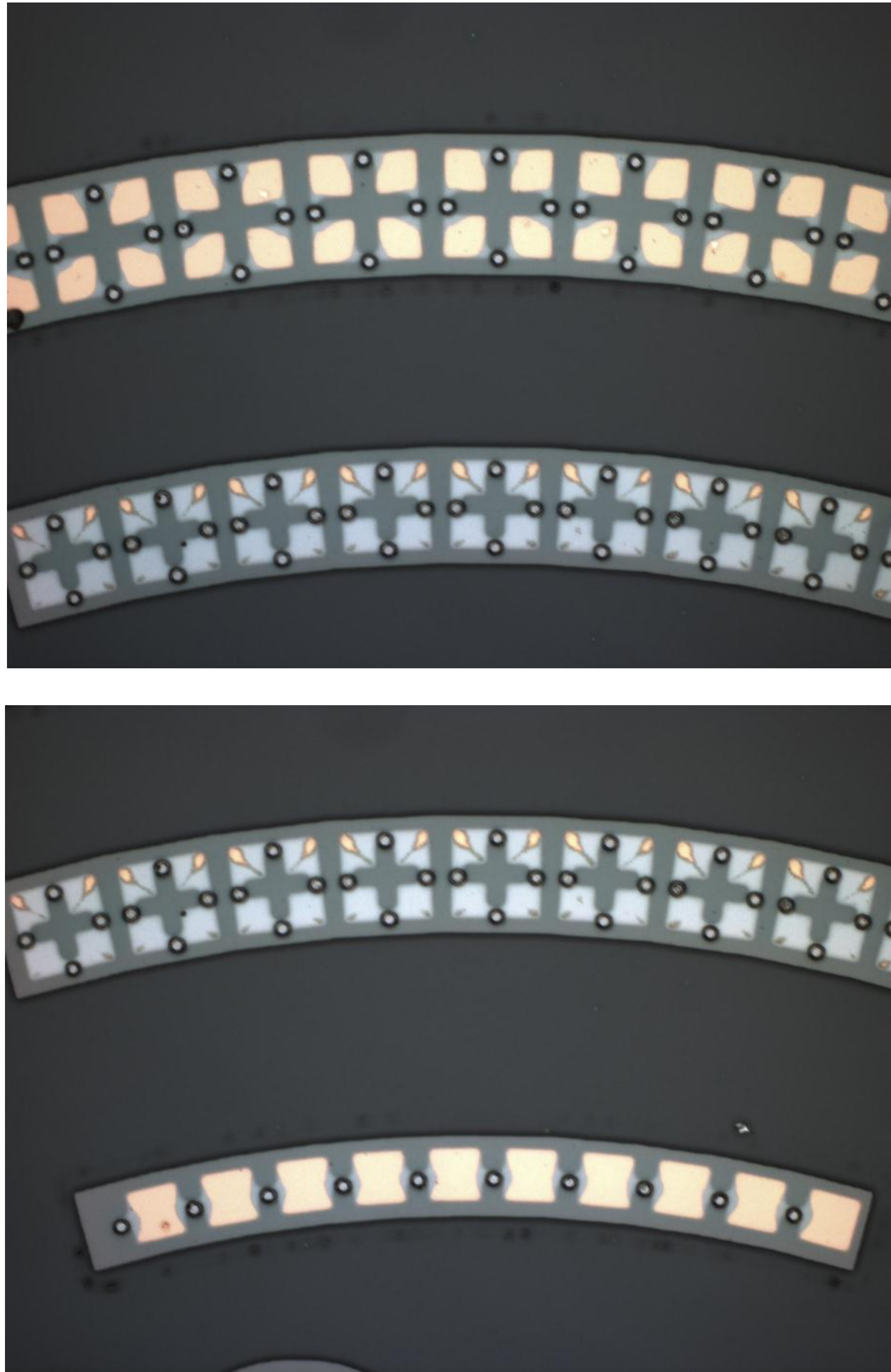


Figure 6.16 Micrograph of CMUT test structures during step (8) release step with RX20 and TX30 rings respectively (top). Micrograph of CMUT test structures during step (8) release step with TX30 and RX40 rings respectively (bottom). Different thicknesses of copper can be seen etching at different rates. These images are taken after 4 mins of etching in APS 100.

6.3.2 Dual Gap Process

There are many challenges and parameters to satisfy in a dual gap fabrication process. First, the process must require no more than one extra patterning step or mask. Second, the surface of the sacrificial layer (copper) must still remain smooth and flat after the second patterning step. Third, it is preferable to not change the sacrificial material as it will cause the re-design of all subsequent processing (although this is not a hard requirement). Two probable solutions have been identified: (1) deposit sacrificial and perform lift-off patterning sequentially to achieve two different sacrificial material thicknesses that will define the gap heights; (2) deposit the larger thickness of copper (50nm) and use another photoresist mask layer to mask the Tx elements and etch the Rx element's sacrificial material down to 30nm.

The advantage of method (1) is that no etching is involved with the patterning and thus technically easier than selecting an etching method to meet the process parameter requirements. However, the largest drawback with method (1) is the sharp edges or "horn like" features as a result of the lifting of the photoresist. These sharp edges are a weak point in the reliability of the device as thin dielectric insulation layers such as HfO_2 cannot guarantee uniform coating at sharp peaks. Also, the local electric field in that region will be very high thus causing a weak spot for high probability of shorting and charging effects to occur during operation. Thus choice (2) must be implemented for dual gap fabrication process.

The advantage of method (2) is patterning of the dual gaps or dual thickness copper without the sharp edges. The disadvantage in this method is that it is difficult selecting the right chemistry and etching process to achieve the aforementioned desired process

requirements. The rest of this section will describe the chemistry and process used for this process and its characterization post etching.

A dry etching method was used to pattern the copper due to its high repeatability and controllable etch rates in the ~10-20nm/min range. Since the goal is to etch ~20nm, this is a reasonably controllable etch rate range. The details of the recipe and chemical technical know-how is developed by Dr. Dennis Hess (Georgia Institute of Technology, Department of Chemical Engineering) and his Ph.D. student Tae-Seop Choi and can be found in [130]. This is a highly non-standard process, as copper is not typically dry etched. This is due to the fact that it has been historically difficult to find the “right” chemistry to achieve highly volatile by-products during the reactive ion etching process. Methods such as the damascene process are used instead in the IC industry to form the current generation of IC interconnects found in modern CPU chip manufacturing processes. The damascene process does not require etching of copper but rather pattern it by forming shallow dielectric trenches and filling it with thin layers of ALD copper and using CMP planarization to achieve the desired IC layering [131], [132]. For this dual frequency CMUT work, a methane (CH_4) based plasma chemistry was used to etch the copper layer controllably while satisfying the uniformity and surface roughness requirements. A custom configured Plasma-Therm ICP RIE (Saint Petersburg, FL) was used to perform the etching. The etch rate of the particular recipe was determined to be 10nm/min. Several pieces of patterned copper on top of chromium were mounted onto a 100mm wafer and etched for an additional minute each to observe the etch rate, shown in Figure 6.17.

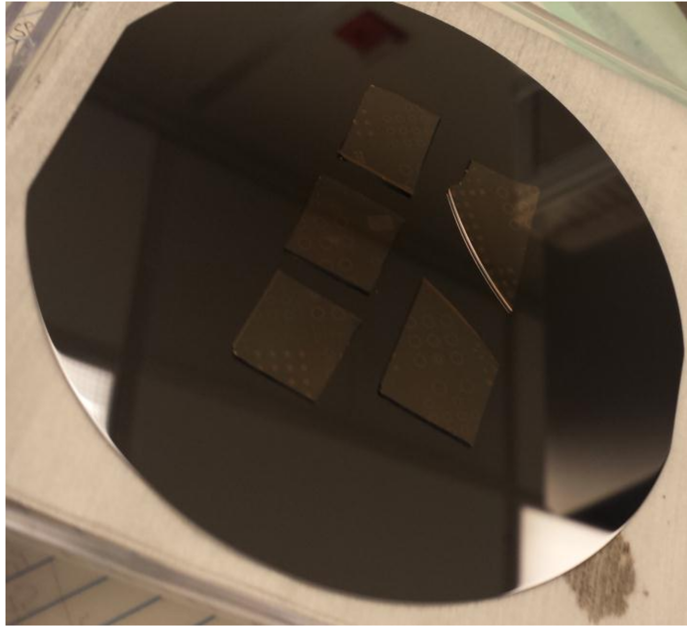
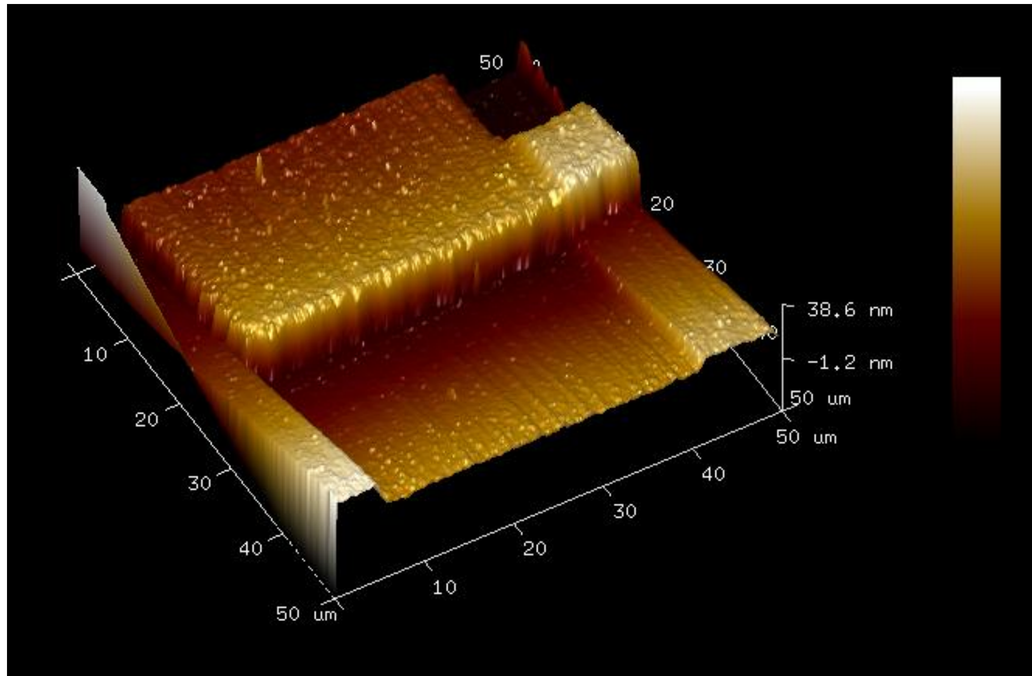


Figure 6.17 Test pieces for measuring etch rate of copper with CH_4 based plasma chemistry.

The sample that was etched for 2 minutes was subsequently scanned using a Veeco Dimension 3100 Atomic Force Microscope (AFM) for step height and surface roughness. Tapping mode measurement was used. Figure 6.18 shows the average Cu step height of 30nm (beginning thickness 50nm) and an average root-mean-squared (RMS) surface roughness of 1.7nm over a 10x10um^2 area.

A cross section SEM image was taken with Zeiss Ultra60 FE-SEM shown in Figure 6.19 to show that no additional non-volatile by products remain on the surface of the copper after etching. It has been shown in [130] that other surfaces in contact with the plasma chemistry including titanium, Si, SiO_2 all have small amounts of C_xH_y deposited on those surfaces. If the chamber is dirty with contaminants some non-volatile C_xH_y may redeposit onto the copper surface.



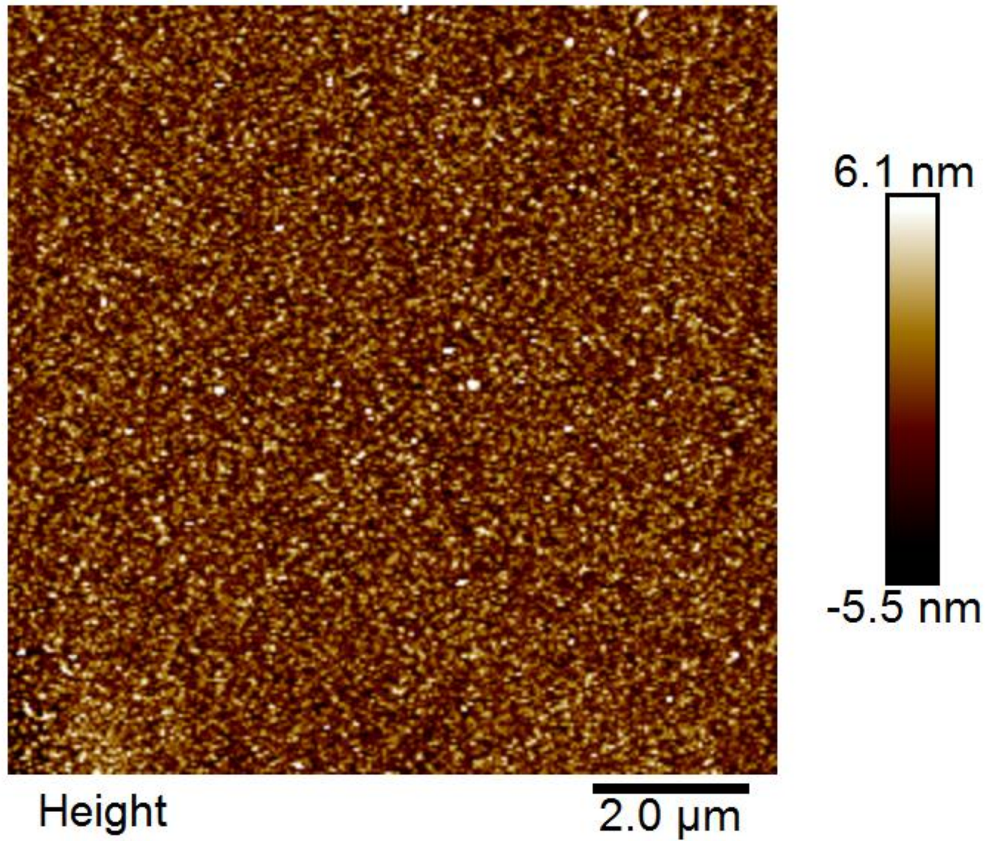


Figure 6.18 AFM step height measurement of copper on chromium after 2 minutes of etching (top), AFM surface roughness measurement after 2 minutes of etching (bottom).

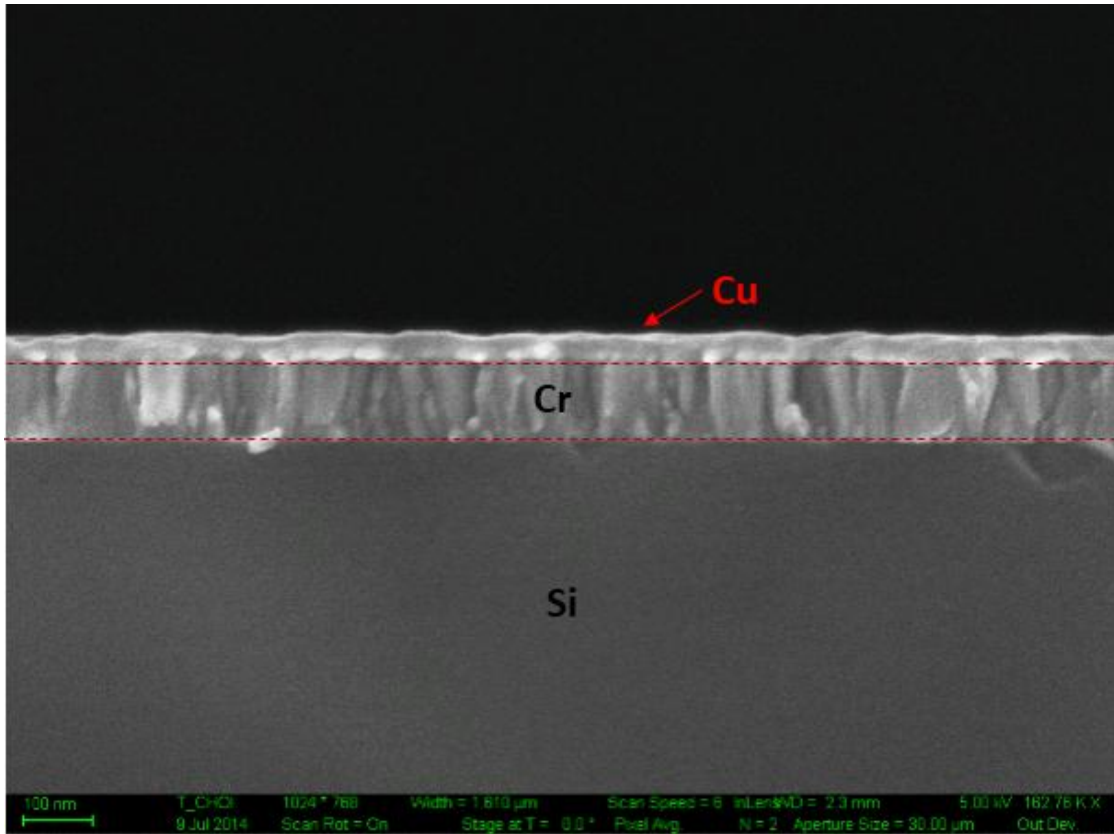


Figure 6.19 Zeiss Ultra60 FE-SEM image of Cr-Cu interface and the lack of any C_xH_y by-products on top of the copper surface after 2 minutes etch.

6.3.3 Dual Membrane Thickness

The dual frequency design have many restrictions for element sizes and pitch to satisfy the half lambda requirement to minimize grating lobe effects up to 90 degrees for the elevation angle in the final ultrasound image. As the design parameters have previously shown, the RX20 and TX30 elements will have a membrane thickness of 0.8µm to satisfy their simulated and desired frequency responses. The RX40 elements require a 2.5µm thick membrane to reach the ~40MHz range. This requires the fabrication process to produce two different final thicknesses for the 3 types of membranes. The strategy to achieve this was to use an extra mask to (1) pattern a metallic etch stop above the 0.8µm of structural

layer and (2) later used to define a photoresist etch mask and etch down the 2.5μm thick Si_xN_y to the etch stop for RX20 and TX30 to give the desired thicknesses for each element design. The RX40 elements are untouched during this process as photoresist will be protecting those areas of the mask. Figure 6.20 shows the region that has the etch mask and also the thinned area of Si_xN_y for RX20 and RX30 elements. Region for thicker membrane for RX40 is also shown.

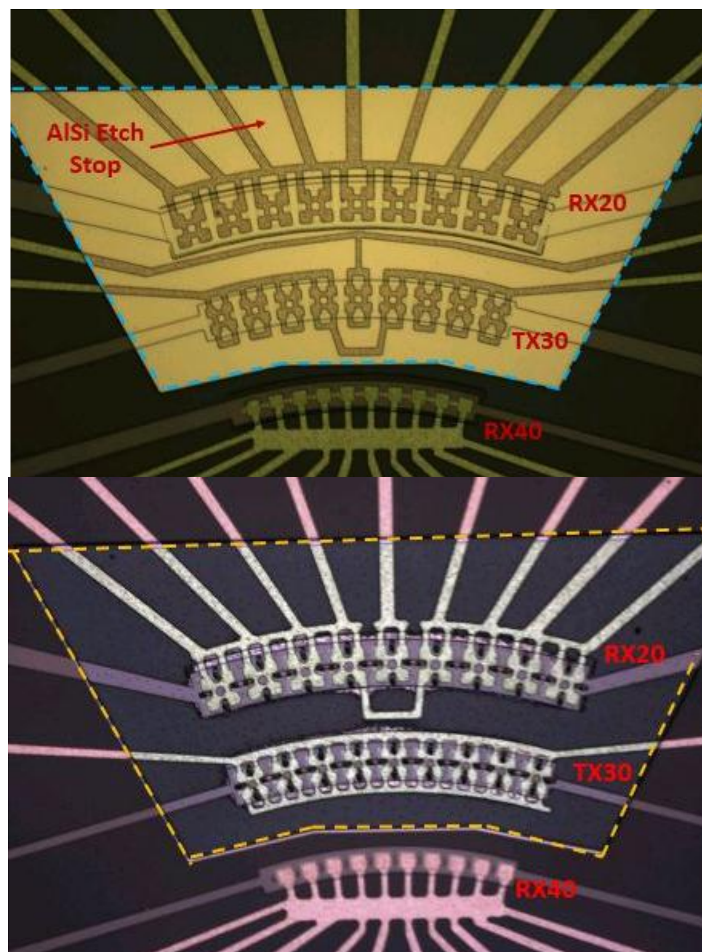


Figure 6.20 Micrograph of dual frequency CMUT array after the patterning of the AlSi 2% etch stop layer. The blue dotted lines outlines the region of etch stop (top). Micrograph showing post membrane thinning (etching) of Si_xN_y from 2.5μm to 0.8μm and after removal of etch stop (bottom).

To prevent the already Si_xN_y sealed sacrificial etch holes from being etched open during the membrane thinning step, photoresist features must be patterned on top of those areas to protect the etch holes. Failure to protect the etch hole features could mean that the vacuum seal will break and the gap of the device will no longer be evacuated to a reasonable pressure to prevent squeeze film damping effects. These are relatively small 5x10µm features as shown in Figure 6.21 and designed as rectangles not squares so that surface area can be larger to promote better adhesion onto the Si_xN_y surface. Since the edge of these feature come close to the membrane due to the tight tolerance of etch holes with respect to membranes and with a limit of ~1-2µm during alignment, it can be expected that these rectangular protection features protrude into the membrane by the limit of alignment accuracy. This can also be observed in Figure 6.21. The area where this protection photoresist covers the Si_xN_y will not etch which means there can be non-uniformity of the membranes in the RX20 and TX30 due to slight misalignment and can affect the overall frequency behavior of the device.

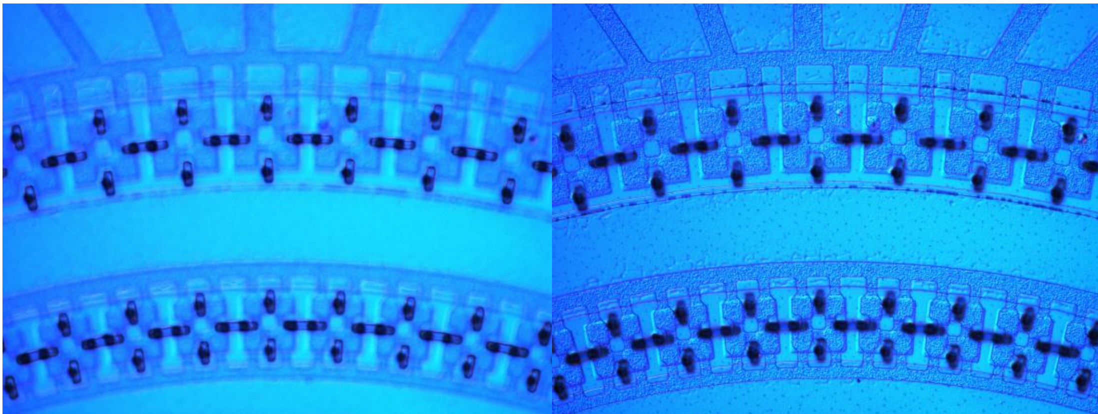


Figure 6.21 Micrograph of patterned photoresist to protect the Si_xN_y in the sacrificial etch-hole region with the objective focus on the patterned features (left). Same image as the one shown on the left except with objective focus on the already formed patterned features (right). Slight misalignment can be observed.

6.4. Experimental Results

6.4.1 Electrical Impedance Measurements in Air

To verify the accuracy of fabrication and the modelling, electrical impedance measurements were made with an Agilent Network Analyzer 8753ES. The experimental setup is shown in

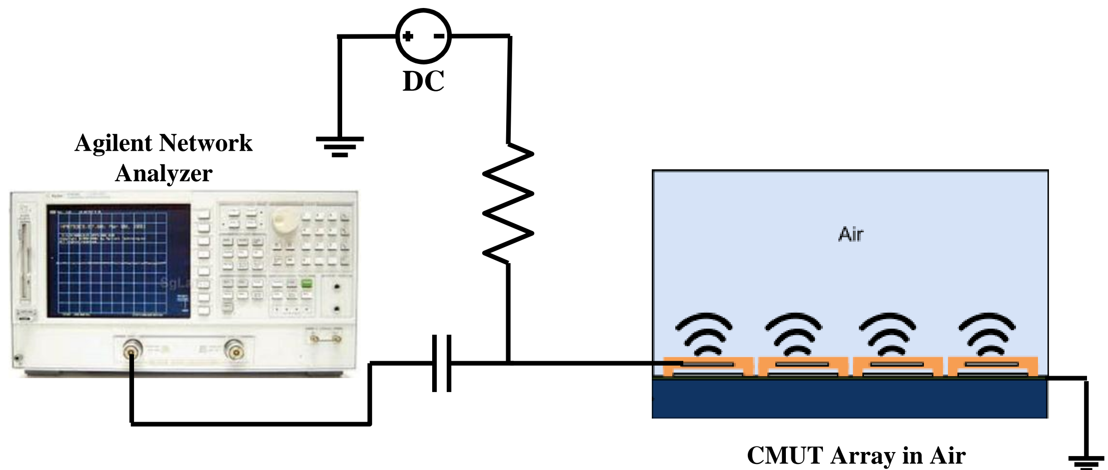


Figure 6.22 Diagram of electrical impedance measurement setup.

Figure **6.22**.

Resonance peaks are seen at different V_{DC} bias values for different element types. The spring softening effect is also visible with the peaks shifting to lower frequencies as high V_{DC} is applied. Figure 6.23 shows the real parts of the impedance measured for the different types of elements. Each type of elements have all of the top electrodes connected in series with each other, or each of the element capacitances are in parallel with each other. The individual elements in each type are connect in this way to give a reasonable overall capacitance for measurement. One can observe from each impedance measurement that there are sometimes multiple peaks due to slight fabrication differences and variations from

membrane to membrane. These peaks are smoother after Parylene-C coating which in effect gives some mass and stiffness coupling over the surface of the transducer.

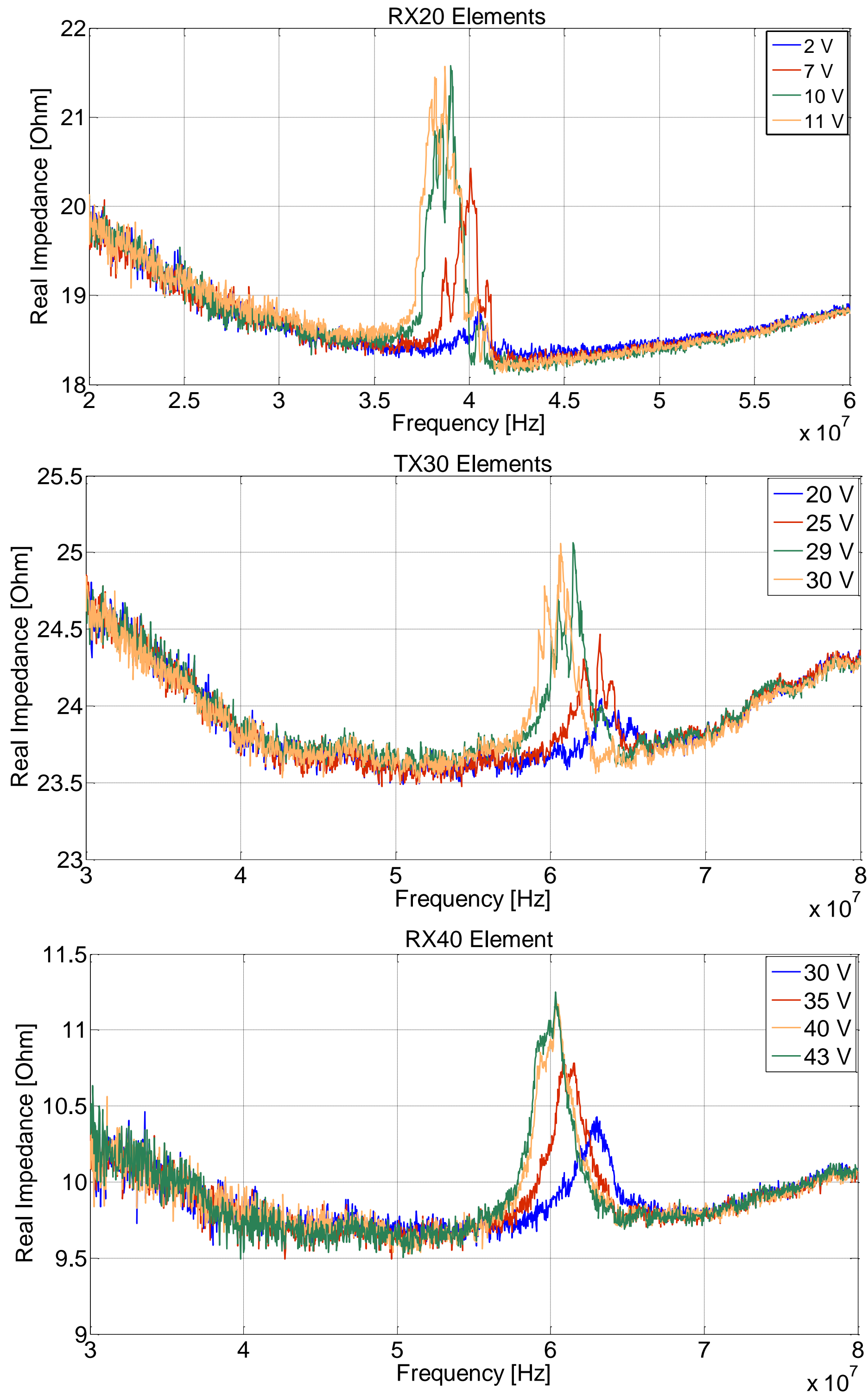


Figure 6.23 Real part of the electrical impedance measurement for each type of the dual frequency CMUT array: RX20 (top), TX30 (middle) and RX40 (bottom).

Next we compare the measured resonances in air to the simulated resonance frequencies in air for different thickness values of the membrane in Figure 6.24. The different thicknesses (h) are calculated for comparison because membrane thickness variation during fabrication is the largest contributing factor towards frequency response deviation from the original simulated design in Table 6.3. The bending stiffness coefficient (D) scales with h^3 for a square thin plate membrane.

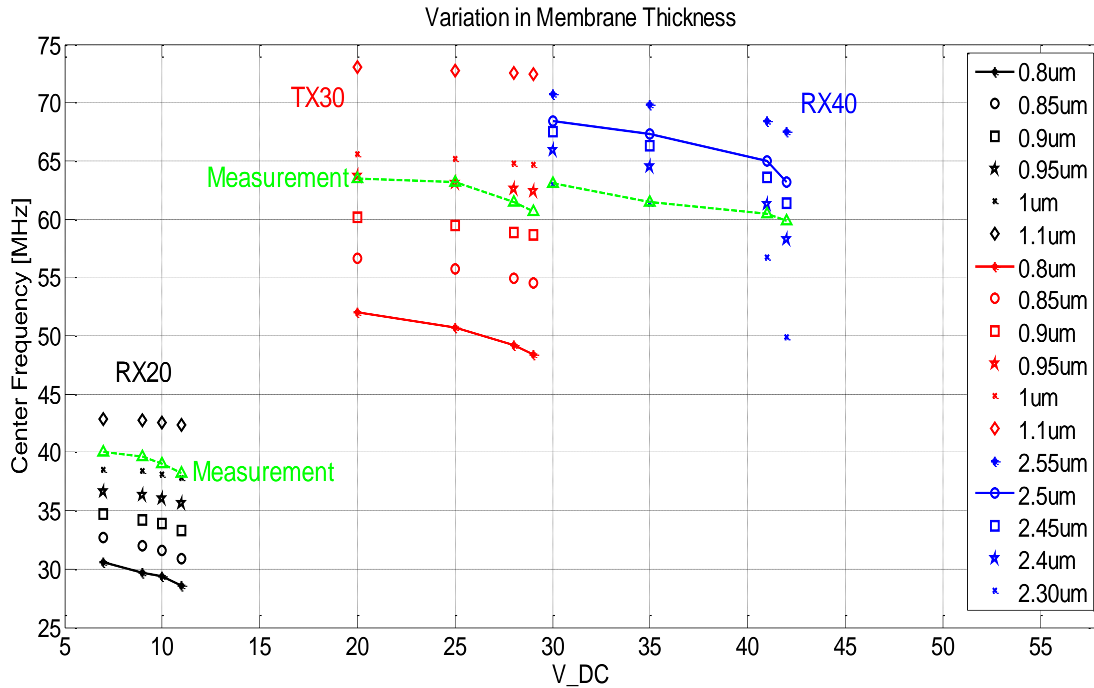


Figure 6.24 Center frequencies measured in air for various membrane thicknesses simulated compared to measurement (green). The solid connected lines are the simulated design parameters originally designed for the dual frequency array (Table 6.3). The spring softening effect for each type of element can be observed as V_{DC} is increased.

One can initially observe that the measured resonance frequencies in air for RX20 and TX30 are higher than the modelled and designed thicknesses. This is due to the fact that the model did not account for the mass and stiffness of the HfO_2 and AlSi 2% (top electrode) layers that are also physically part of the moving membrane. This was previously negligible in the design shown in Chapter 3 due to the large thickness ratio difference

between Si_xN_y:HfO_2 or Si_xN_y:AlSi (>20 times). For this dual frequency design the thickness ratio difference between Si_xN_y:HfO_2 and Si_xN_y:AlSi is on the order of 7 times and 5.3 times respectively (for both RX20 and TX30), which means the mass and stiffness of the "thin" 100nm HfO_2 insulation layer and 135nm AlSi top electrode cannot be ignored for a more accurate modelling of the membrane structure and its resonance frequency. An equivalent thickness for Si_xN_y can be approximated by matching the first eigen-frequency for the HfO_2-AlSi-Si_xN_y fabricated stack in COMSOL® Multiphysics. Table 6.5 shows the equivalent Si_xN_y thickness compared to the multi-stack of materials for a fabricated membrane. With the equivalent Si_xN_y thicknesses, the modelled resonance frequencies in air for RX20 and TX30 are within ~10% and ~5% error from the experimental values.

Table 6.5 Equivalent Si_xN_y Thickness Compared to HfO_2-AlSi-Si_xN_y Membrane Stack

	Element Type	
Parameter	**RX20**	**TX30**
Equivalent Thickness (μm)	0.95	0.95

RX40 element is over predicted by the model due to its low aspect ratio of width to thickness shown in Figure 6.25. When the aspect ratio (width/thickness) for the geometry falls below 10, the accuracy of the thin-plate approximation decreases as already studied and compared to FEM results in [62]. In cases for aspect ratios that are in the range of 6-8, the thin-plate model approximates the resonance frequencies ~15% higher than FEM simulated results. This is also consistent with the observations and comparisons made in [58].

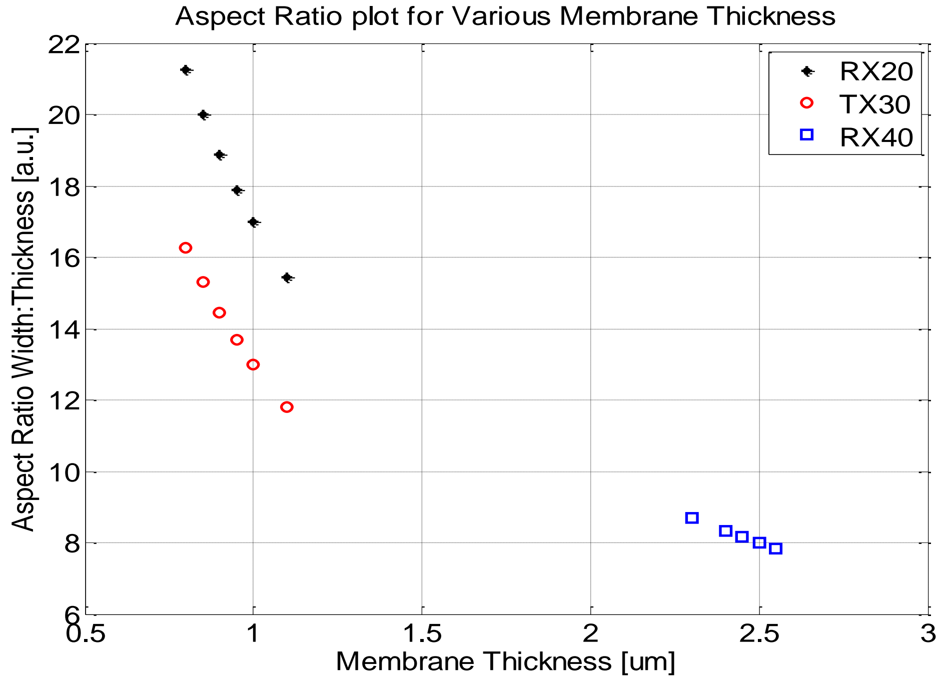


Figure 6.25 Aspect ratio of the membranes for various element/membrane types for various variations in the membrane thickness. The membrane widths are assumed to be constant and the same as the design in Table 6.3.

A similar study was performed by varying the width (w) of the membranes compared to the ideal design case and with the experimental results of resonance frequencies measured in air. The thicknesses are constant and the same as the original design in Table 6.3. It can be seen from Figure 6.26 that a change in width has a smaller change in the resonance frequency on average compared to a change in membrane thickness. The main contributing factor for smaller widths than designed are due to (1) over exposure/development during lithography and (2) over etch from isotropic wet etching process during the definition of copper sacrificial layer. There is also a +/- 0.25μm tolerance on the lateral features during the fabrication of the mask. It is noted for future designs that masks should be made on average 0.4-0.6μm larger laterally compared to the ideal design parameters to adjust for the loss of lateral dimensions during lithography and

etching. This of course changes as a function of lateral size of the membranes (sacrificial layer) and is less affected by larger membranes compared to smaller membranes (e.g. <20μm).

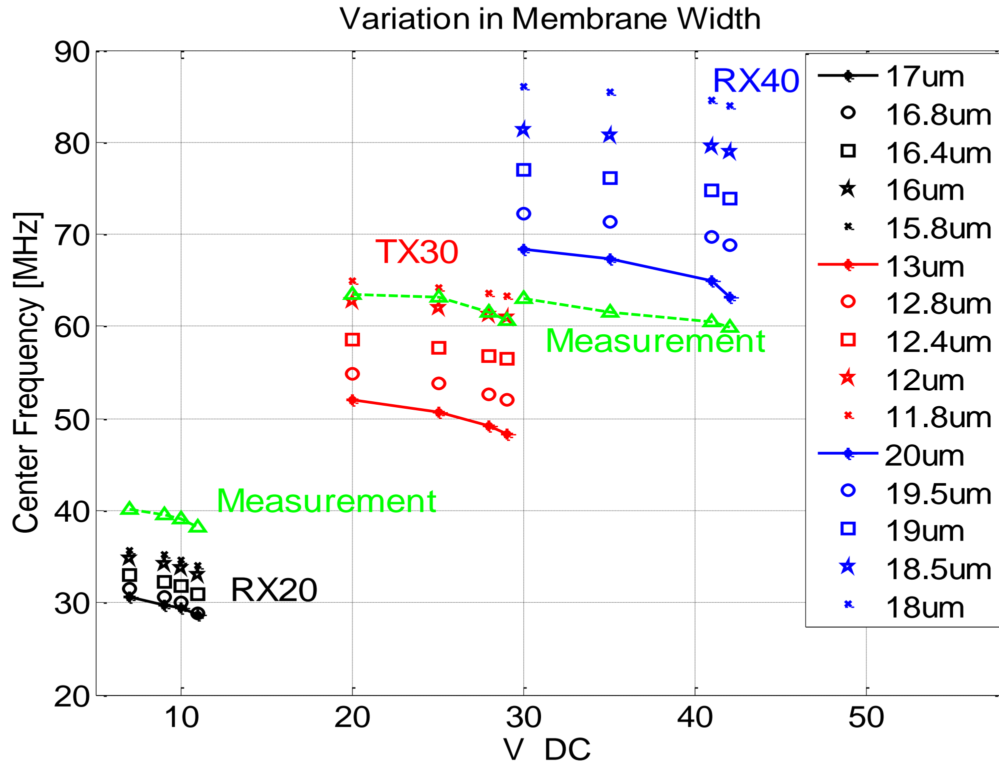


Figure 6.26 Center frequencies measured in air for various membrane thicknesses simulated compared to measurement (green). The solid connected lines are the simulated design parameters originally designed for the dual frequency array (Table 6.3).

6.4.2 Hydrophone Measurements in Water

Hydrophone measurements of the pressure spectrum from each type of elements are collected and compared with the simulated response. In each case, all of the elements in each ring are connected together in parallel. This is so that enough pressure output can be generated to meet the sensitivity level of the ONDA (Sunnyvale, CA) HGL-0200 hydrophone. At 20MHz, the sensitivity of the hydrophone is ~550 nV/Pa. The input pulse to the CMUT was generated by Agilent (Santa Clara, CA) 81150A function generator and

amplified through an EIN (Rochester, NY) Model 310L RF amplifier. The experimental setup is shown in Figure 6.27. The input pulse to the CMUT was measured via a 10x probe with the CMUT loaded and used for the same V_{INPUT} in the simulation.

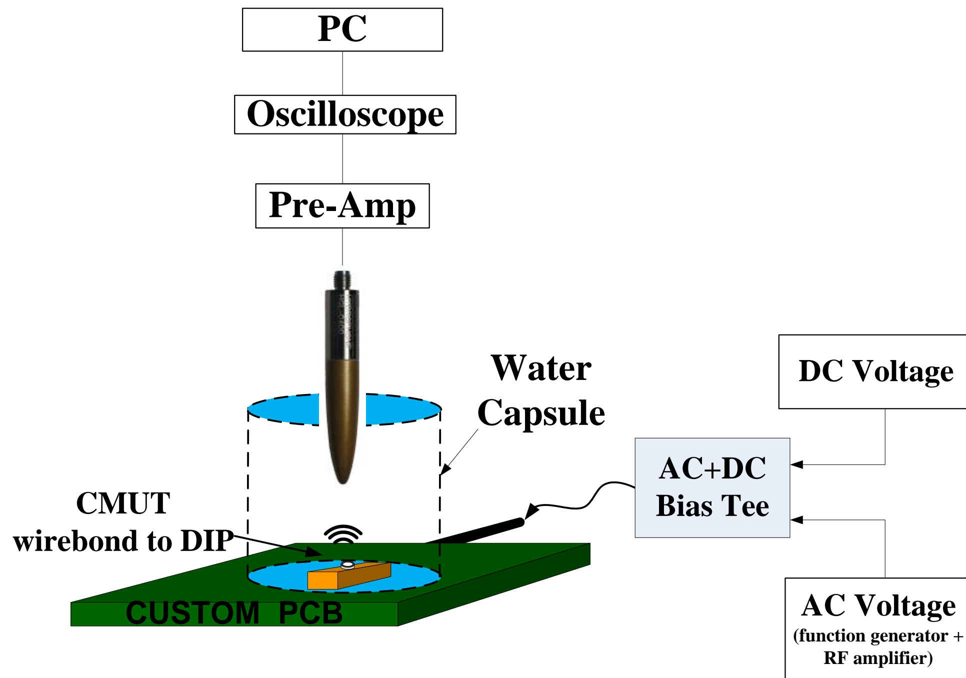


Figure 6.27 Diagram of hydrophone measurement setup.

The hydrophone was placed at a distance of Z = 2 mm away from the array and centered with respect to the CMUT. The frequency response was obtained by taking the Fast Fourier Transform (FFT) of the time domain hydrophone outputs and compared to the simulated cases for each transmit ring, shown in Figure 6.28. In the simulation shown, the thickness of RX20 and RX40 are adjusted to 0.95µm instead of 0.8µm to account for the combined mass and stiffness of the HfO_2-AlSi-Si_xN_y membrane stack. Overall, the main band shape in each of the designs matches quite well. The center frequency for RX20, TX30 and RX40 as measured are 27.7MHz, 40.5MHz and 41.5MHz. The center frequency for RX20, TX30 and RX40 as simulated are 25.8MHz, 40.9MHz and 41.4MHz. It is generally observed that the bandwidths simulated is larger than the bandwidths measured.

This could be due to a variety of reasons including (1) mass, stiffness and damping from the parylene layer not accounted for in the simulation (these are coupled to all of the

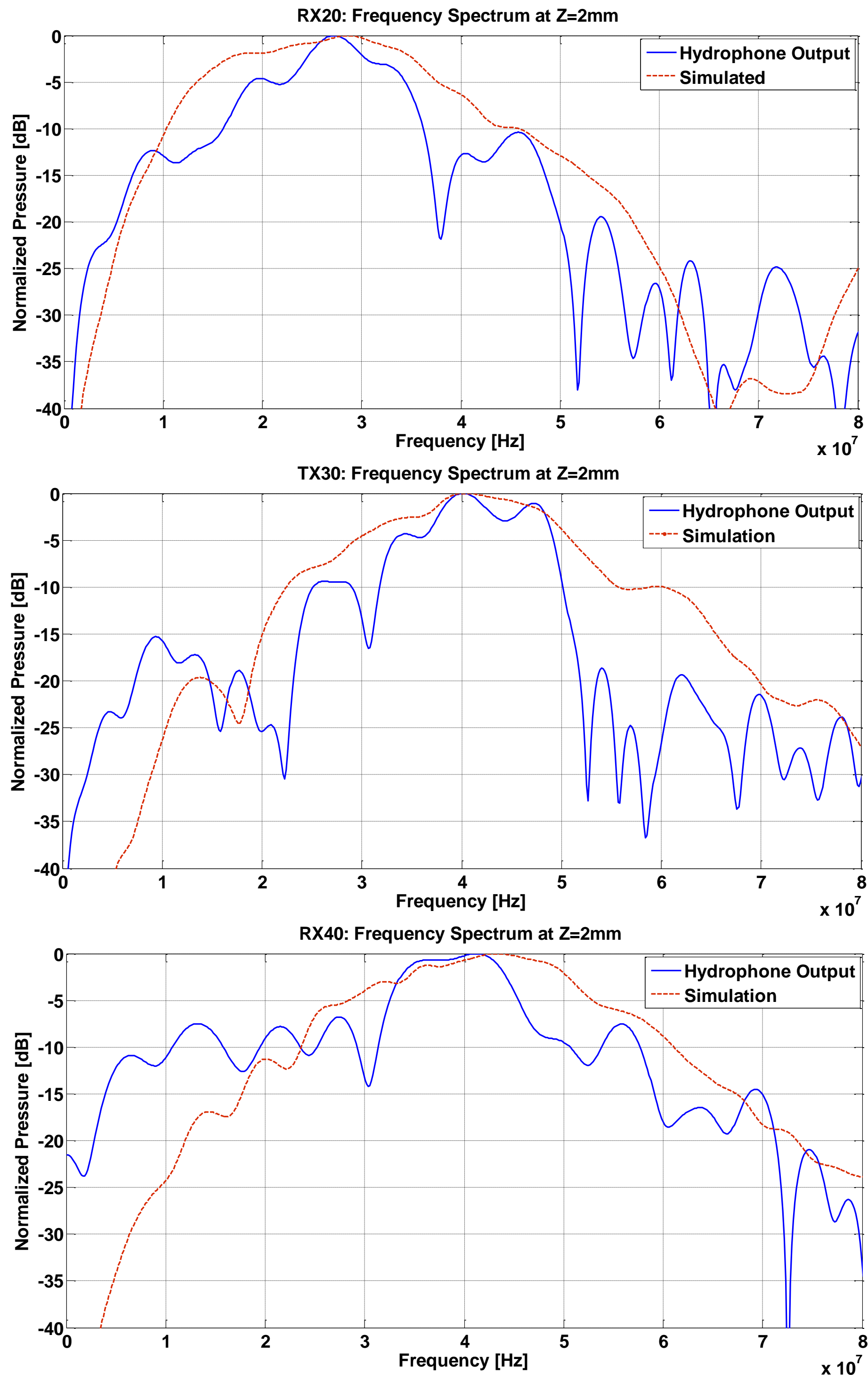


Figure 6.28 Frequency spectrum for the fabricated device measured with a hydrophone compared to simulated results.

membranes), (2) mis-alignment and fabrication non-uniformities that can cause un-predicted mode shapes to occur, (3) the cut-off response of the hydrophone (hydrophone's response is flat up to 20MHz with calibration data. Calibration beyond 20MHz is unknown).

It is interesting to point out that the measured center frequency in both TX30 and RX40 is close to 40MHz. However, the TX30 design has a higher -6dB bandwidth compared to the RX40 design. This means that for the same center frequency design, it is more advantages to design with thinner membranes as compared to thick membranes. Also, TX30 elements are composed of 4 membranes while RX40 elements are single membranes, which is another reason why acoustical cross-talk can sometimes enhance the performance in bandwidth.

In conclusion, a dual frequency and dual gap device have been designed, fabricated and characterized. A framework for designing CMUTs for any particular system have been described and the other subsystems and parameters CMUT design will be affected by. It can be seen that many parameters in CMUT design have coupled effects and it takes an iterative process and intuition about how different parameters in geometry can affect the f_c, BW and SNR of the CMUT device. In this work, simulated results have shown promising SNR values in both frequency bands assuming TM-noise limited system. An eight mask fabrication process was developed for the dual gap, dual thickness membrane process to satisfy multiple different design criterions for batch fabrication. Main limitations in fabrication processing are (1) accuracy of lithography, (2) etching definitions of the lateral geometry, (3) thickness accuracy of the multi-layered thin films and (4) X-Y and theta alignment accuracy. It is shown that for thin membranes, it is not acceptable to model

the membrane stack of material with just Si_xN_y as the membrane material and that the stiffness and mass from entire HfO_2-AlSi-Si_xN_y stack must be accounted for to make more accurate predictions for the center frequency of the CMUT device. Thin plate approximation for the stiffness of the membrane is also not accurate (upto 15-20% error) when aspect ratio of the square CMUT is below 10. Lastly, the general band shapes from hydrophone measurements were well predicted by the refined model (thicker membrane thickness to include for HfO_2-AlSi-Si_xN_y stack).

CHAPTER 7. CONCLUSIONS AND FUTURE WORK

7.1. Conclusions and Statement of Contribution

For the next generation intravascular ultrasound (IVUS) catheter systems, real time 3D volumetric imaging with high resolution (< 150μm), high dynamic range (> 40dB) is desired. This can be achieved by using the CMUT-on-CMOS integration technology with 2D CMUT arrays described in this thesis. It is desirable to keep the overall physical chip dimension to less than Φ=1.5mm with an opening in the middle of Φ=0.34mm for guidewire compatibility. It is also desirable to simultaneously produce forward and side looking images in chronic total occlusion (CTOs) patient cases where the frontal plaque blockage and arterial sidewalls imaged simultaneously, which can improve the accuracy and speed of the diagnosis or intervention procedure.

To increase the efficiency and sensitivity of micro-machined CMUTs, the effects of utilizing high-κ dielectrics was investigated. From this research, an analytical frame work for understanding the relationship between electrostatic force (F_{ELEC}) to dielectric constant ("κ") and dielectric insulation layer thickness ("t_d") was found. A relationship between the transformer ratio ("η") to κ and t_d was also derived and analyzed for Si_xN_y and HfO_2. It was shown that for lower vacuum gaps (<50nm), the gain in F_{ELEC} and η were significantly larger (~2 times or more) for high- κ dielectric materials such as HfO_2 compared to traditional semiconductor dielectric materials such as Si_xN_y. It was also shown that in receive mode operation, the collapse voltage can be minimized significantly (reduction by ½) by using small gaps and high-κ insulation layer (HfO_2) while also obtaining +6dB gain in sensitivity over the Si_xN_y insulation.

Using atomic layer deposition (ALD), a reliable and controllable method of fabricating thin high-κ insulation layers, monolithically integrated CMUT-on-CMOS chips

were fabricated with $V_{COLLAPSE}$ of 40V and close to 40dB dynamic range images of a pig artery were successfully produced with a V_{pulse} of +25V. High reliability of the HfO_2 insulation was also validated for 88% $V_{COLLAPSE}$ DC bias condition over a time period of ~4 hours, which is more than the standard time required for most IVUS surgeries without any patient complications (~2 hours) [133].

To address the functionality of simultaneously forward and side looking single 2D CMUT-on-CMOS array, the research has shown that this was possible due to acoustical cross-talk waves produced on the surface of the transducer array. Center frequencies of 11 and 22 MHz were measured from the pulse-echo of wire targets from the side (elevation angle 90 degrees) and the front (elevation angle 0 degree). This result was also supported by simulations from the large signal model for CMUTs showing a lower frequency band (fc = 14.7 MHz) traveling along the surface (elevation angle 90 degrees) of the transducer array and a propagated center frequency of (fc = 23.3 MHz) in the front direction. Finite element analysis (FEA) also supported this behavior by showing 2 distinct resonance peaks in the average velocity of the excited CMUT element. From the FEA simulation, a lower frequency but high quality factor ("Q"), which implies non propagating bulk acoustical energy (or evanescent waves in the z-direction) and higher frequency but low Q propagating, which implies bulk acoustic waves (into the far-field) were observed. Lastly, successful 3D images were reconstructed showing the capability of imaging wires located on the plane of the transducer as seen in Chapter 5.

Leveraging the system level understanding and CMUT-on-CMOS integration technology developed in Chapters 2-5, an initial design and prototype was developed for a 2D dual frequency CMUT array for IVUS. The system level design considered imaging

requirements driven by IVUS application, CMUT fabrication requirements and IC-design and fabrication requirements. A 3 ring design with 2 receive type elements (RX20 and RX40) and one transmit (TX30) ring was fabricated and validated against design through the large signal model for CMUTs. Maximum V_{DC} required for this array is 40V ($V_{COLLAPSE}$) for RX40 elements with the minimum V_{DC} of 11V for RX20 elements. A 100nm HfO_2 insulation layer was needed to avoid electrical break down when operating near 40V. To achieve the desired design specifications such as low collapse voltage, $\lambda/2$ element pitch size, and high sensitivity in each of the receiving bands (~20MHz and ~40MHz), each type of element design was optimized separately for its geometry parameters (width, thickness and vacuum gap height). It was determined that RX20 and RX40 will have g = 35nm while TX30 elements have g = 50nm to reach a high SNR design. The limitation on the gap for TX30 was determined by full gap swing criterion assuming maximum V_{pulse} of +50V (possible with a TSMC 0.18μm fabrication process).

Signal-to-noise ratio (SNR) calculations and parametric studies of gap heights and V_{DC} applied were simulated for optimum designs. For a thermal-mechanical noise limited system, reducing the receive element gap has no advantage in gain for SNR; however, it does reduce the $V_{COLLAPSE}$ and IC-noise design requirements.

A dual gap and dual membrane thickness fabrication process was developed for the dual frequency CMUT devices. A methane (CH_4) based DRIE process was used to define the dual height sacrificial copper features. An etch stop was designed into the fabrication process to achieve high thickness accuracy when etching down the membrane thickness for RX20 and TX30 elements.

Experimental impedance measurements in air showed some deviations from original design especially in the thinner membranes (RX20 & TX30) due to the simulation not accounting for the mass and stiffness of HfO_2 and AlSi2% (top electrode) layers. By adjusting the simulated thicknesses to an equivalent Si_xN_y thickness, the resonance frequencies between simulation and experiment came to within 5% deviation. Other effects such as width change and non-uniformity in fabrication and alignment error can also affect the resonance behavior of the device. For low aspect ratio elements such as the designed RX40 (aspect ratio < 10), it is observed that the thin plate approximation is not accurate with up to ~15% error for f_c in air between measured and simulated cases.

Hydrophone measurements in water showed similar center frequency and bandshapes as compared to the simulated results. Center frequency for RX20, TX30 and RX40 as measured by the hydrophone are 27.7MHz, 40.5MHz and 41.5MHz. The center frequency for RX20, TX30 and RX40 as simulated are 25.8MHz, 40.9MHz and 41.4MHz. The bandwidths from measurements are typically lower than that of the simulated results.

7.2. Future Work

7.2.1 Further Characterization of High-κ Dielectric Material

CMUT operational stability in receive mode have been characterized and shown to be stable at V_{DC} = 88% $V_{COLLAPSE}$. Additional characterization of the quality of the ALD HfO_2 can be made through C-V measurements of test CMUT structures under constant high V_{DC} bias to observe and quantify for any charging effects. High temperature rapid thermal annealing (~350-370^{0}C) can also be used to improve the dielectric characteristics of the insulation layer [101]–[103]. The dielectric constant of HfO_2 can potentially increase from 16 to as high as 20-25 through this technique and reduce the number of thin film defects that can cause premature breakdown before theoretical breakdown voltage (V_{BD}) is reached. The increase of κ from 16 to 20 will increase the CMUT receive sensitivity by ~1.5 times at the limit condition of g = 0 assuming all other parameters remain the same.

7.2.2 Catheter Packaging and Testing

Continued collaboration with RWTH for flexible interconnect and NIH for catheter packaging/integration is still underway. Initial catheter prototypes shown in Figure 7.1. have been shown to be partially functional and able to receive transmitted signals from a 20MHz piezo in water. The flexible interconnect are attached to 1 meter length single copper core braided microcables (~Φ = 100μm) as shown in Figure 7.2. Resistive welding technique were used to bond the copper wire to the gold pads on the flexible interconnect.

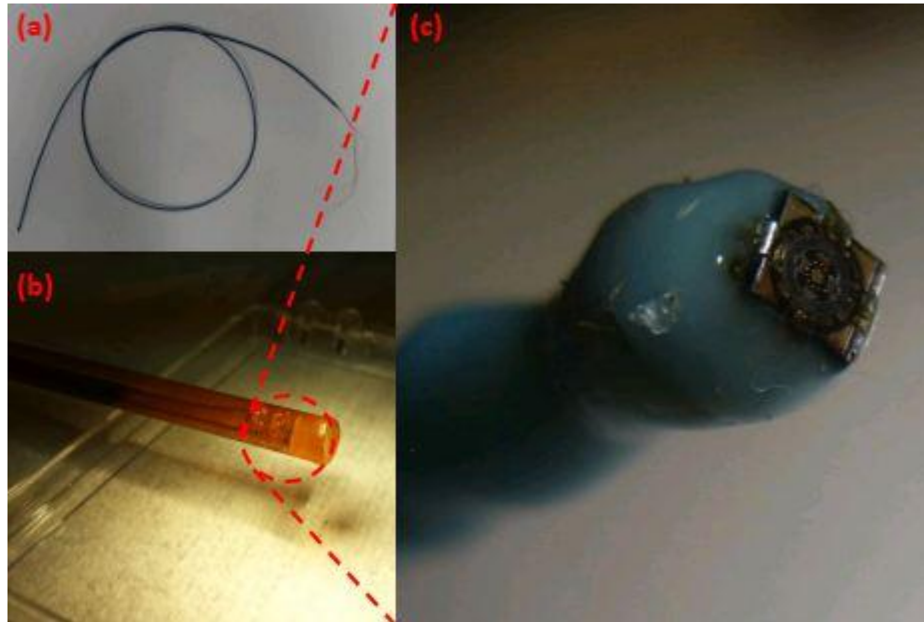


Figure 7.1 (a) Catheter prototype (b) Close-up view of the tip of the catheter (c) Tip view of the catheter with silicon casted around the CMUT-on-CMOS chip, flex interconnect and cabling.

Resistance, inductance and capacitance of the cable must be carefully characterized as these additional values can change the frequency response of the RF signal. Further design considerations on the IC side will need to take into consideration the types of driving circuitry needed for the cables. Shielding, electrical and magnetic cross-talk between the cables should also be tested with the CMUT-on-CMOS system and compared to RF signals before the cables were added. Once a fully functioning catheter prototype is obtained with full a functioning CMUT-on-CMOS chip, imaging can be performed inside of a pig artery or tissue like phantom and performance can be evaluated.

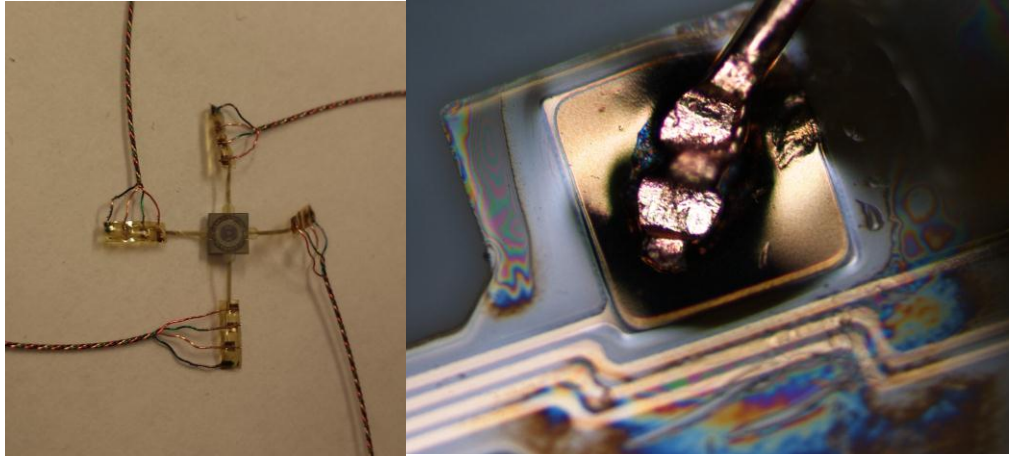


Figure 7.2 Single copper core braided micro-cable attached to the flexible interconnect (left) Close up view of the resistive welded copper wire to the gold bond pad on the flexible interconnect (right).

To make the flexible circuit attachment to the sensor chip easier and more robust, through silicon vias (TSV) technology can be utilized to bring front-side electrical connections to the backside of the chip. This will ease the restriction of epoxy over flowing onto the CMUT membranes from the front side as well as removing additional thickness of the flexible interconnect from the sides of the sensor chip. The TSV will however increase the overall cost and complexity of the manufacturing process and will need to be processed on the CMOS chip before the CMUT integration begins. The TSV process used must be CMOS compatible. Initial efforts were made in this area in [37]. A concept diagram is shown in Figure 7.3.

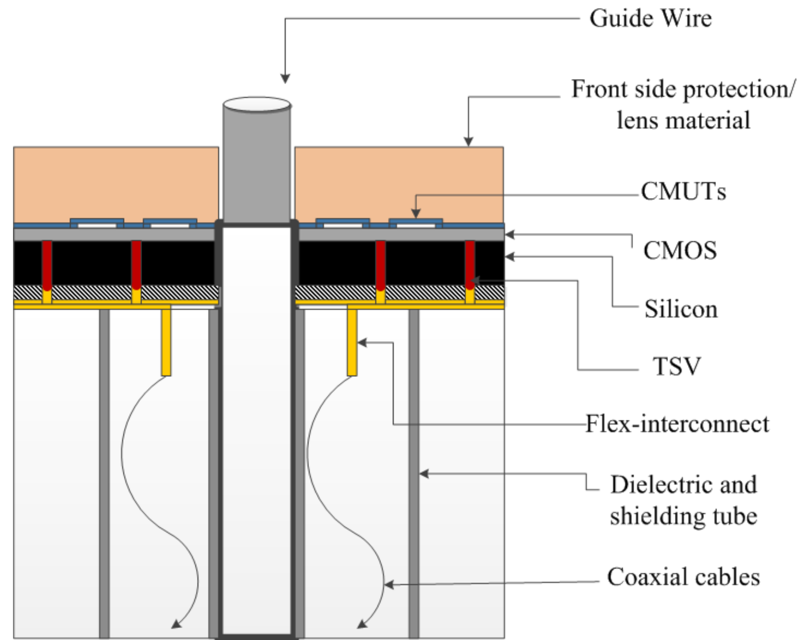


Figure 7.3 Schematic of TSV integration with CMUT-on-CMOS, and the attachment of flex interconnect from the backside of the die for catheter prototype.

7.2.3 Functional Catheter Prototype

After the successful development and attachment of the polyimide flexible interconnect and micro cabling, a catheter prototype development was attempted in collaboration with National Institute of Health (NIH) laboratory in Bethesda, Maryland. Before building the custom tubing, molds and jigs needed to achieve this, the partial assembly of CMUT-on-CMOS + polyimide flexible interconnect + micro-cabling (shown in Figure 7.2) is coated in a 5 µm thick Parylene-C layer for moisture and environmental protection.

For testing of the catheter prototype, the end of the micro cables are soldered to a custom PCB board connector shown in Figure 7.4 and the rest of the catheter submerged into a water bath. First, the electronics are tested by applying 3.3 V to Vdd and 1.3V to IC

Bias and GND to make sure the current draw from Vdd is the same as pre-packaged device. Vdd current was in the range of 12-16 mA and similar to measured values before catheter packaging. Receiver outputs were also checked for DC voltage level and were at a normal 0.9-1V. A 12MHz center frequency CMUT-on-CMOS is at the tip of this particular prototype originally designed for ICE application. The aperture size for this array is Φ = 2mm. By using a 100nm HfO_2 insulation layer and a 50nm gap, the $V_{COLLAPSE}$ of this device is only 20V. The V_{DC} on both Tx and Rx were at17V (85% of $V_{COLLAPSE}$) and a 36ns

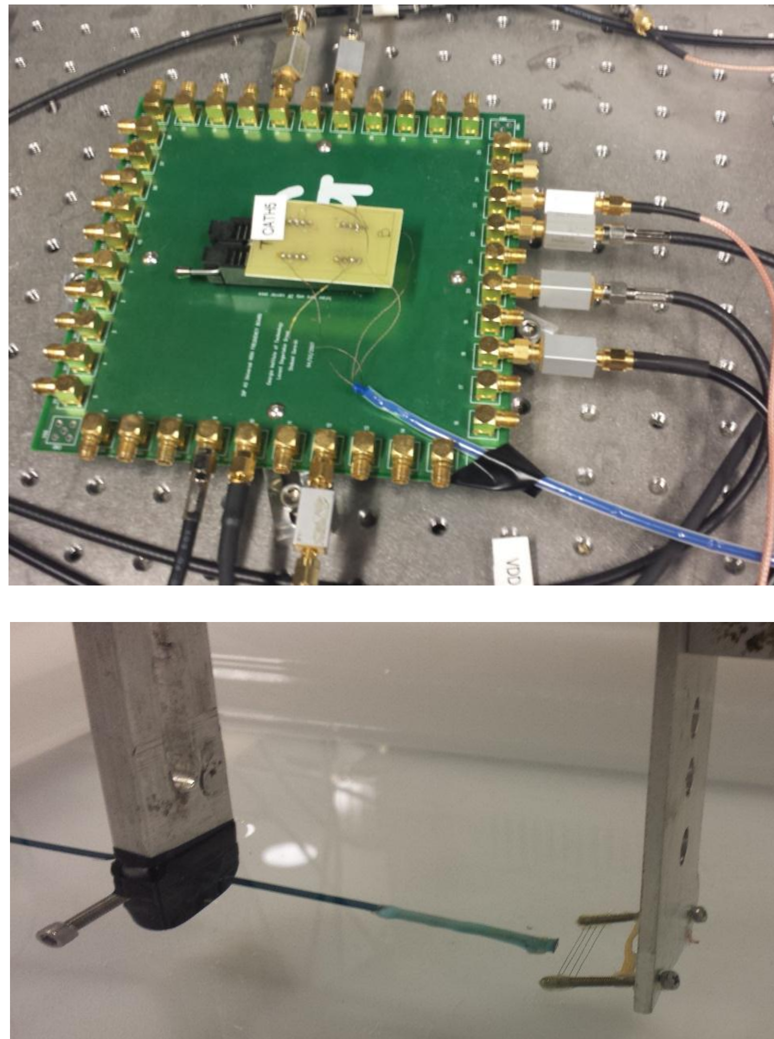


Figure 7.4 Custom PCB and 40 pin holder setup for catheter testing with the end of catheter cable is attached (top), catheter prototype in water with wire target phantom

unipolar 12.5V V_{PULSE} was applied to the top electrode of Tx. The voltage used for V_{PULSE} is the maximum based on this particular pulser design [60].

A cross-sectional image of the wire targets is shown in Figure 7.5 after image reconstruction using a delay and sum algorithm for full synthetic aperture [83]. The reconstructed image space is 10x10 mm^2 area. The first 1 mm is not shown due to near field effects and image artifacts that saturates the rest of the image at 30dB dynamic range. Three out of the 4 wires are clearly seen in this image. The 4th wire is not seen in this section most likely due to the acoustics did not reflect back from the wire due to the positioning of both the catheter and target.

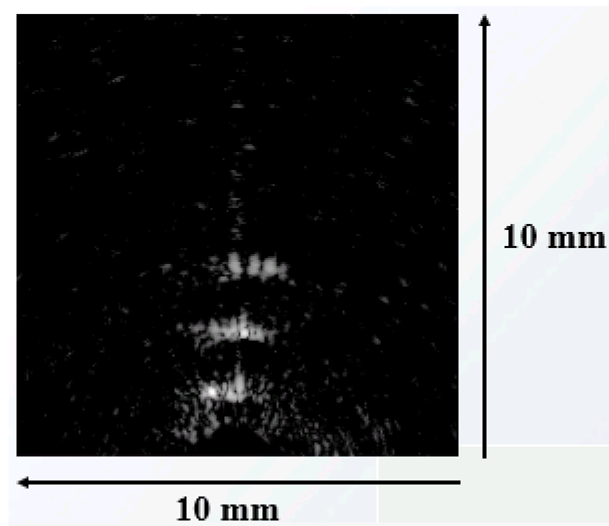


Figure 7.5 Image reconstruction of wire targets in a 10x10mm image slice. The image dynamic range is 30dB.

7.2.4 Dual Frequency Design and Integration with IC Chip

Initial simulation and optimization of Tx and Rx element design for the dual frequency 2D CMUT array has been shown in this thesis. The design considered imaging criterion to minimize grating lobes, maximizing the bandwidth of the pulse-echo signal and SNR. The design also considered the limitation of pulsing voltage with the chosen TSMC 0.18µm process and a maximum V_{PUSLSE} of +50V. Future work, first includes the design and implementation of the IC circuitry in both Tx and Rx. A two chip approach can be first implemented via wirebonding before extending to full CMUT-on-CMOS integration. For simulating "thin" membranes, the mass and stiffness of the HfO_2 and top electrode layers must also be accounted unlike the design originally made for this array. For more accurate incorporation of the mass and stiffness of the multi-layer membrane, a hybrid FEM + BEM approach can be used [58]. First, FEM is used to produce the stiffness matrix that incorporates the multi-layer stiffness. The mass can also be lumped and approximated into a homogenous material for simplification. Then these stiffness and mass matrices can be used in the BEM approach for solving the mutual impedance between each node of the membrane in a half baffle boundary condition. This approach will aid in achieving more accurate simulated results for center frequency and bandwidth without the need to iterate in FEM to find the "equivalent" silicon nitride thickness compared to the multi-layered membrane.

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