NUMERICAL INVESTIGATION OF CARBON NANOTUBE THIN-FILM COMPOSITES AND DEVICES

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NUMERICAL INVESTIGATION OF CARBON NANOTUBE THIN-FILM COMPOSITES AND DEVICES

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LIST OF SYMBOLS AND ABBREVIATIONS

CNT	Carbon nanotube
FET	Field-effect transistor
TFT	Thin-film field-effect transistor
CN-TFT	Carbon nanotube network thin-film transistor
LC	Liquid crystal
CVD	Chemical vapor deposition
CMOS	Complementary metal–oxide–semiconductor
DPD	Dissipative particle dynamics
L_C	Channel length
W_C	Channel width
H	Channel width
t_{ox}	Oxide thickness
t_{Si}	Si substrate thickness
T	Temperature
T_∞	Ambient temperature
$Q^{'}$	Reference Power

d	CNT diameter
k_t	Thermal conductivity
ξ_i	Non-dimensional temperature at i^{th} node of CNT
ξ_{OX}	Non-dimensional temperature of oxide layer
ξ_{Si}	Non-dimensional temperature of Si substrate layer
$q_i^{'}$	Power dissipation per unit volume in i^{th} node of CNT
Bi_C	Non-dimensional CNT junction thermal conductance
Bi_S	Non-dimensional CNT-substrate thermal conductance
h_C	Heat transfer coefficients at CNT junctions
h_S	Heat transfer coefficients at CNT-substrate contacts
h	Heat transfer coefficient
P_C	Perimeter of CNT
P_S	Length of the perimeter directly in contact with substrate
k_t	Thermal conductivity of CNT
k_S	Thermal conductivity of Substrate
A	Cross sectional area of CNT
ψ	Electrostatic potential

V_G	Gate Voltage
V_{SD}	Source-to-drain voltage
ρ	CNT network density
ε	Dielectric permittivity
λ	Screening length
ε_{CNT}	Dielectric constant of CNT
ε_{OX}	Dielectric constant of oxide layer
t_{OX}	Oxide thickness
J	Current density
p	Hole concentration
n	Electron concentration
$C_{ij}^{n,p}$	Charge transfer coefficient
M-CNT	Metallic CNTs
S-CNT	Semiconducting CNTs
Φ_D	Column vector for electrostatic potential in CNT nodes
Φ_B	Column vector for electrostatic potential in boundary nodes
E	Electric field

$D_{\mathrm{n/p}}$	Diffusion coefficient
N_{T}	Trap charge concentration
F_{T}	Trap charge filling probability
v_{th}	Thermal velocity
n_{H}	Hole concentration
n_{E}	Electron concentration
5-CB	4-cyano-4'-pentylbiphenyl
$\mathbf{r}_i$,	Position vector of a DPD bead
$\mathbf{v}_i$	Velocity vector of a DPD bead
m_i	Mass of a DPD bead
$\mathbf{f}_i$	Total force on a dead bead
$\mathbf{F}_{ij}^{C}$	Conservative force
$\mathbf{F}_{ij}^{D}$	Dissipative force
$\mathbf{F}_{ij}^{R}$	Random force
$\mathbf{F}_{ij}^{M}$	Morse potential force
$\mathbf{F}_{ij}^{S}$	Harmonic potential force

$\mathbf{F}_{ij}^{SC}$	Columbic interaction force
r_c	Cut-off radius
r_{ij}	Interbead distance in DPD
r_s	Interaction range parameter
D_e	Well depth in Morse potential
ω	Interaction range parameter in Morse potential
V_{BD}	Breakdown voltage
P_{BD}	Breakdown power
PP	Peak Power
L_t	CNT length
θ_{avg}	Average CNT network orientation

SUMMARY

Carbon Nanotube (CNT) based thin-film transistors (TFTs) are considered to play critical role as the building blocks of future electronics with applications in flexible, transparent and energy-efficient circuits, e-displays, solar cells, conformable radar and RFID tags, e-paper, touch screens, implantable medical devices and chemical/bio/optical sensors. Significant progress in recent years on synthesis, purification and integration challenges has reinforced the promise for technological and commercial success of CNT-TFTs. However, there are some issues related to their operational reliability which need to be addressed. CNTs in CNT-TFTs are deposited on low thermal conductivity substrates and therefore the excessive self-heating in CNT-TFTs is likely to degrade the electrical and thermal performance and could potentially lead to failure of the devices. Therefore, the high-field behavior of CNT-TFTs needs to be investigated and analyzed to improve their operational reliability.

A computational approach is developed and employed to study the electrical and thermal transport in CNT-TFTs. A numerical model based on the Poisson's equation, the drift-diffusion equations and the Fourier-conduction equations is developed to predict the transport properties and high-field behavior of CNT-TFTs. The validity of the model is established by comparing the numerical results with experiments. The CNT network based TFTs are studied to find how the channel geometry (length and width) and network morphology (network density, CNT length and alignment distribution, CNT junction topology) affect the heat dissipation and high-field breakdown of CN-TFTs. The impact

of thermal boundary conductance (TBC) at carbon nanotube CNT-substrate interfaces and CNT junctions on power dissipation and breakdown in the device is investigated. Comparison of the results from an electro-thermal transport model to experimental measurements of power dissipation and temperature profiles allows us to estimate thermal conductance values at CNT-substrate and CNT-CNT interfaces.

The electrical and thermal transport in aligned CNT-TFTs for moderate to high density arrays and varied oxide thickness is studied to explore the implications of electrostatic and thermal cross-talk among the CNTs on electrical and thermal performance. Performance metrics such as On-current, On/Off ratio and peak temperature of the devices are correlated with the array density and oxide thickness to obtain the optimum range of device parameters. Hysteresis in aligned CNT-TFTs is also studied with the aim to understand and quantify the effect of trap charges. Parameters such as trap sites concentration and location, oxide thickness, and CNT array density are varied to analyze how they change the hysteresis behavior. The current work offers new insights into thermal reliability of CNT-TFTs. Results presented here provide useful design guidelines on device parameters which can be engineered to enhance performance of CNT-TFTs for macro and flexible electronics applications. Lastly, CNT-liquid crystal composites are also studied using dissipative particle dynamics (DPD) technique with the aim to understand how the CNT concentration in composite affects the alignment of liquid crystals and to explore the method of CNT alignment using liquid crystals.

CHAPTER 1: INTRODUCTION

Carbon Nanotubes (CNTs) are seamless cylinders made of carbon atoms arranged in hexagonal/ honeycomb structure with open or close ends [1]. Depending upon the number of layers, CNTs are classified as either single-walled (SWCNT) or multi-walled (MWCNTs) (Figure 1.1). Diameters of SWNTs and MWNTs typically range between 0.8 nm to 2 nm and 5 nm to 20 nm respectively. CNT lengths can vary from a few nanometers to several centimeters. Owing to their unique one-dimensional structure, individual CNTs exhibit exceptional mechanical, electrical, thermal, optical and chemical properties [2, 3]. Individual CNT walls can be metallic or semiconducting based on the orientation of honeycomb structure with respect to tube axis, a property known as chirality. The MWCNTs are typically metallic but the SWCNTs can be metallic or semiconducting based on their chirality.

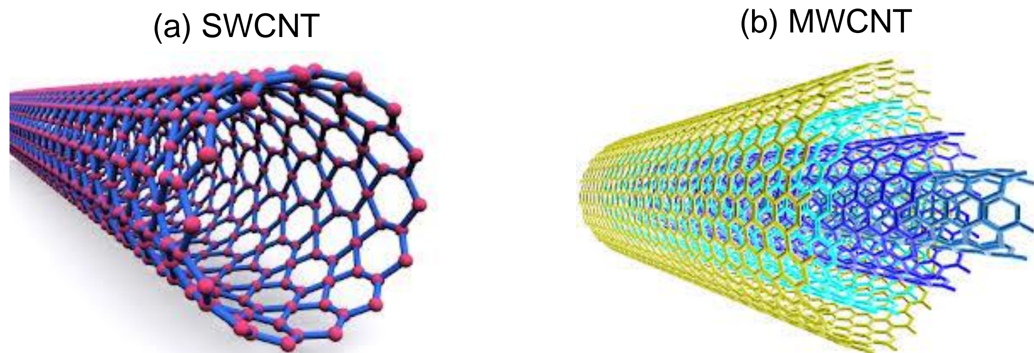

Figure 1.1. Schematic demonstration of the structure of (a) single-walled carbon nanotube (SWCNT), (b) multi-walled carbon nanotube (MWCNT).

Currently, the commercial usage of CNTs are limited to applications such as rechargeable batteries, automotive parts, sporting goods and rust-preventive coatings where CNTs are used in the form of bulk composite materials [2]. However, the recent advances in synthesis, purification and large scale controlled integration of ultra-thin films of networks and aligned arrays have paved the way for their applications in logic circuits, e-displays, sensors, antennae etc. with unique combination of properties such as mechanical flexibility, optical transparency, energy efficiency, and superior device performance [3-21].

1.1 Carbon Nanotube Thin Film Transistors (CNT-TFTs)

Transistors, used as amplifiers and switches, are the basic building blocks of all modern day electronics. Field-effect transistors (FETs) are the most common type of transistors employed in several applications such as logic, memory and sensors. FET is typically controlled using three electrodes known as source, drain and gate (Figure 1.2). These electrodes control the charge concentration and the electric field (and hence the current) within the active part of the device known as channel. Semiconducting SWCNTs (hereafter simply referred to as CNTs) are a very promising candidate for the channel material as they have been shown to exhibit excellent performance in both short and long channel transistors surpassing the performance of currently dominant silicon-based transistors [3-6]. They can enable a wide variety of novel applications such as flexible circuits, e-displays, solar cells, conformable radar and RFID tags, e-paper, touch screens, implantable medical devices and chemical/bio/optical sensors [3-21].

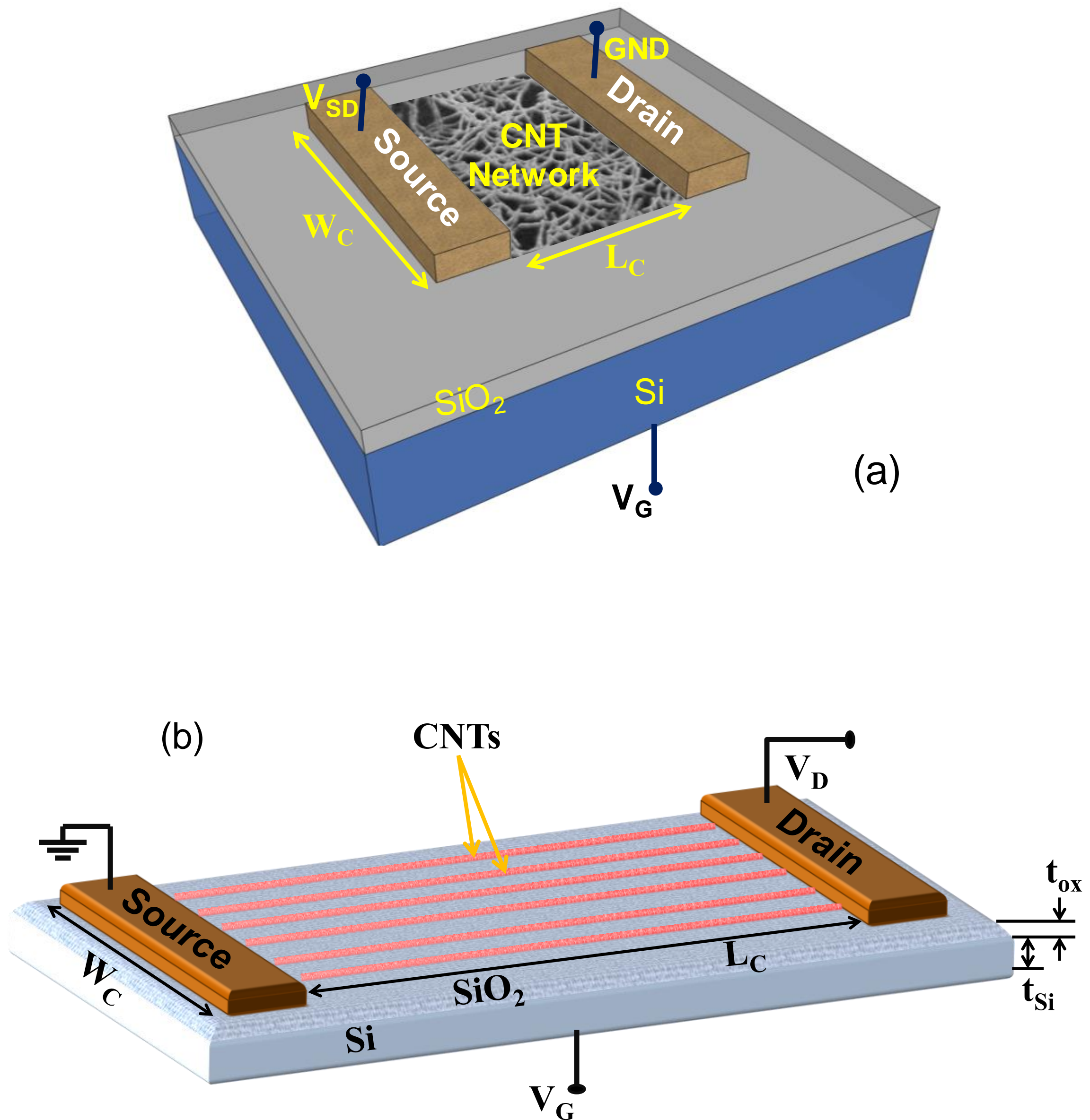

Figure 1.2. Schematic diagram of thin-film field effect transistor with (a) random CNT network, (b) aligned CNT array used as channel material.

To minimize performance variability and due to the ease of fabrication, thin-film of network or arrays of CNTs are preferred over individual CNTs as the channel material. Also, the thin-film of CNTs can withstand higher degree of strain which is needed for flexible electronics. These devices can be transferred onto both planar and non-planar

substrates, including clothes, papers and even the skin. The sensors can be interfaced with live plants or insects for real-time monitoring of environment and detection of toxicity in the air. The e-skin may be useful in applications such as interactive devices, robotics and medical/health monitoring devices [2, 4].

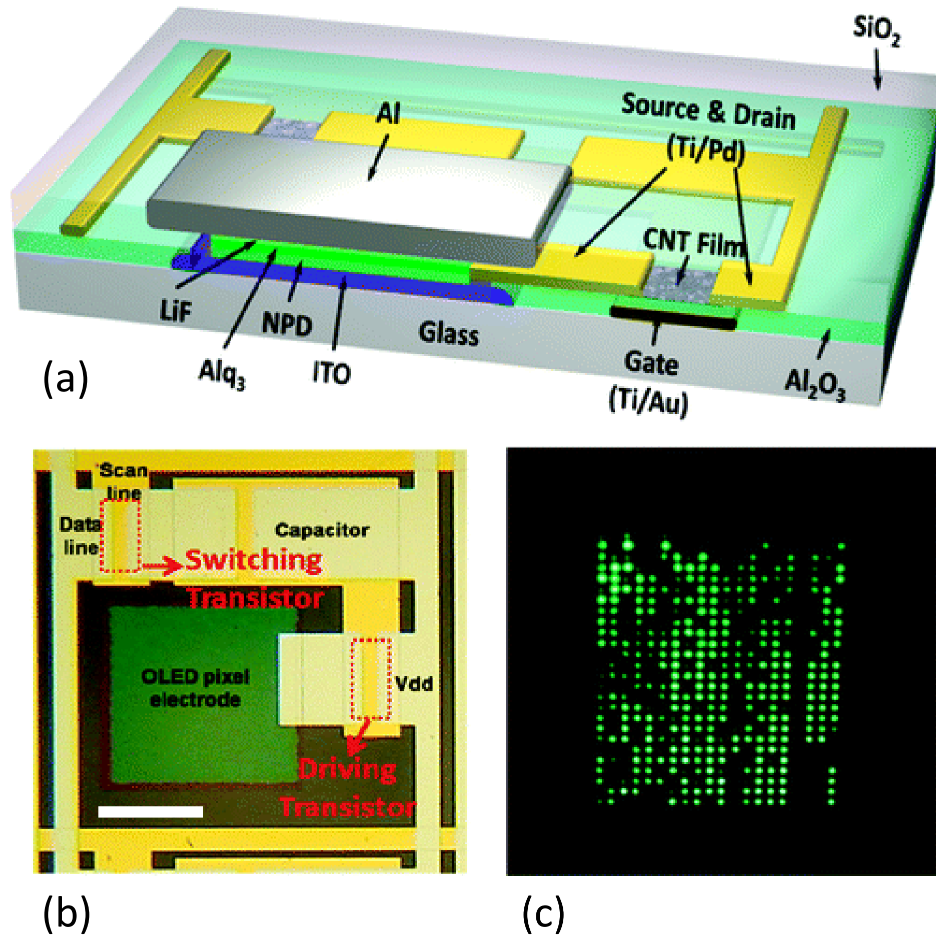

Figure 1.3 (a) Schematic of the structure of the active matrix organic light emitting diode (AMOLED) pixel consisting of a glass substrate, patterned Ti/Au gate electrode, Al_2O_3 gate dielectric, CNT thin film as the active channel, Ti/Pd source and drain contacts, integrated OLED (ITO/NPD/Alq_3/LiF/Al), and a SiO_2 passivation layer. (b) Optical microscope image (scale bar 100 μm) of the single pixel circuit with two CN-TFTs, one capacitor, and the ITO electrode for OLED integration. (c) Image showing the pixels on an integrated AMOLED. Reprinted with permission from [22]. Copyright (2011) American Chemical Society.

Thin-film transistors (TFTs), an important components of macro-electronic circuits for applications such as active matrix display drivers and X-ray image sensors [11], have the channel region typically made of amorphous *Si* which has low carrier mobility (< 1 $cm^2V^{-1}s^{-1}$) and involves high fabrication costs. There has been a large research thrust towards replacing Si in these devices with new materials which offer greater mobility, improved flexibility, and high transparency along with simple, low cost, and high throughput fabrication [5, 9, 11, 19, 23-27]. CNT network based TFTs (CN-TFTs) (Figure 1.3) have been considered strong candidates in this regard having the potential to pave the way towards broader next generation macro-electronic devices and systems due to the exceptional electrical, mechanical, thermal and optical properties of CNTs [8, 9, 11, 24, 25, 28].

1.2 Motivation and Scope of Current Work

1.2.1 Heat Dissipation and Thermal Reliability of CN-TFTs

Significant efforts have been made in recent years aimed at overcoming fabrication and integration challenges of CN-TFTs [19, 25, 29-33]. However, fewer studies have been focused on the heat dissipation and thermal reliability of these devices which is an important aspect of CN-TFT operation [34, 35]. CNTs in CN-TFTs are deposited on low-thermal conductivity substrates (plastic, glass) which may impede heat removal to ambient. As a result, self-heating during operation may lead to early breakdown of CN-TFTs and therefore presents a serious challenge to the device reliability particularly under high frequency and high bias operation [34, 36, 37]. Also, the structure of CNT junctions on substrate can become crucial in CN-TFTs as low

thermal boundary conductances (TBCs) and high electrical resistances at these junctions can lead to junction temperatures hundreds of degrees higher than the rest of the device, which will severely deteriorate the performance of CN-TFTs [16, 38-45]. Previous studies on electrical breakdown of single CNT transistors suggest that the TBCs at CNT interfaces may play a major role in the power dissipation of CNTs [46-51]. However, the effect of TBCs on operating voltages, power dissipation, and reliability of CN-TFTs is not well understood.

The variations in the channel geometry and network morphology may also influence the breakdown behavior and the thermal reliability of CN-TFTs as well. CNT network TFTs with a large aspect ratio [(channel length / channel width) ≫ 1] have been investigated previously to achieve higher ON/OFF current ratio. Narrow width and large channel length in CNT network TFTs (Figure 1) help in reducing the number of metallic percolating paths in unsorted CNT networks which typically have a 1:2 metallic–semiconducting CNT ratio [19, 52]. However, such high aspect ratios can also lead to substantial variability and non-uniformity in the ON current [53]. The variation in the breakdown behavior for a given TFT geometry can lead to instability and/or unreliability during the operation of CN-TFTs. Thus, it is very important to understand how the geometrical parameters affect the high-field operation of the CNT network TFT in order to optimize the device design for reliable and uniform behavior. In addition, a CNT network is comprised of CNTs of varying lengths (L_t) and alignment (θ) with respect to the source and drain electrodes. Previous studies have shown that the variability in the CNT network morphology in terms of CNT length and alignment distribution can significantly affect the channel resistance and device performance [54, 55]. Therefore

these variations in the channel geometry and network morphology are likely to influence the reliability and breakdown behavior of CN-TFTs as well. While some studies [56] have correlated the electronic properties of CNTs within a CN-TFT channel to the device thermal reliability, the effects of channel geometry and network morphology on CN-TFT power and reliability have not been studied in detail.

1.2.2 Electro-Thermal Cross-talk in Aligned CNT TFTs

Both CNT networks and arrays, used as the channel material in TFTs, have their own set of limitations and advantages. Aligned CNT TFTs are known to have high electrical performance in terms of high On current and mobility. Despite the integration challenges, they are strong candidate for the next generation logic devices [6, 57-59]. Highly dense arrays are recommended for better electrical performance of CNT array transistors [6, 60-62]. However, the electrostatic screening among the CNTs in dense arrays may lead to lower current per tube. The effect of this screening on the transistor performance needs to be systematically investigated [63]. The impact of dense CNT arrays on thermal profile of the device has also not been studied. Since the CNTs in these devices are deposited on thermally insulated substrates (such as glass or polymer), high On-current in dense array TFTs may lead to excessive Joule heating. The self-heating in these CNT TFTs may lead to substantially high temperature affecting the thermal reliability (breakdown temperature of CNTs in air ~600 ºC) [34]. It is also noteworthy that this self-heating effect is utilized for removal of metallic CNTs from the CNT arrays in CNT TFTs [57]. However, in case of dense arrays this method may also lead to damage of neighboring semiconducting CNTs due to the thermal coupling through the

substrate. Thus, understanding the nature of this thermal coupling among the neighboring CNTs in dense CNT arrays becomes very important.

1.2.3 Hysteresis and the Role of Trap Charges in Aligned CNT TFTs

Hysteresis is typically observed in current-voltage characteristics (transfer curves) of transistors (Figure 1.4). This causes temporal instabilities in the performance of transistors (and hence the circuits) and therefore it is a significant challenge. Methods such as chemical treatment of surfaces, heating under vaccum conditions and pulsed-mode operation are typically employed to overcome this limitation. Specifically in case of CNT TFTs, some studies have been performed to understand the details of underlying mechanisms of hysteresis. These studies provide useful insights which have been utilized to reduce hysteresis specifically in CNT-TFTs. It has been reported that trap charges (hydroxyl groups, ionic impurities etc.) present at CNT-oxide interface and within the oxide layer are responsible for the hysteresis. Due to the gate-induced dynamics of trapping/detrapping of holes or electrons by these trap sites, the hysteresis is dependent on the sweep rate of gate voltage. For aligned array CNT-TFTs, the electrostatic screening among the CNTs, can also have some effects on the hysteresis which has not be studied earlier. In the present work, objective is to analyze the effects of relevant parameters such as gate voltage sweep rate, trap charge concentrations, oxide thickness and array density on the hysteresis in aligned CNT-TFTs.

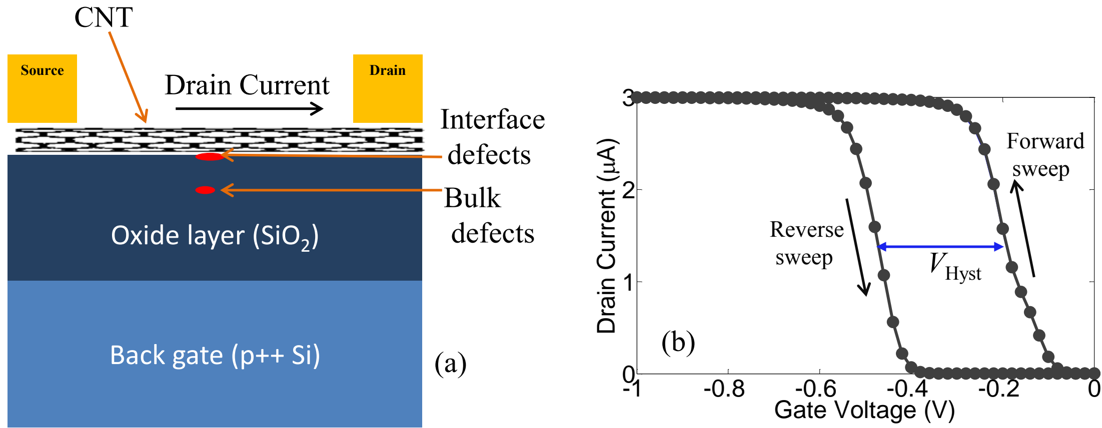

Figure 1.4 (a) Schematic side view of aligned CNT TFT with illustration of the presence of trap charges which cause hysteresis in device characteristics, (b) drain current –gate voltage characteristics with hysteresis.

1.2.4 Alignment Control in CNT-Liquid Crystal Composites

Liquid Crystals (LCs) typically consist of rod-shaped molecules with rigid backbone (mesogens) which are attached to the flexible alkyl chains. Dynamics of LCs under the application of external stimuli such as electric field has been studied extensively in the past due to their importance in LC display applications [64]. Recently, composite materials of LCs with colloidal particles such as carbon nanotubes (CNTs) have received significant interest for improving the performance of LC based devices, e.g., reducing driving voltage, parasitic ion effect, hysteresis of capacitance, back flow etc. [65-70]. In addition, the LC medium has been also used to assist the alignment control of the CNTs [65]. Since aligning the CNTs along a preferred direction is still a considerable challenge, exploring the usage of LCs in CNT alignment can be very useful. A detailed study of the dynamics of these CNT - LC systems under external electric field using appropriate modeling techniques has not been performed. Many studies have been conducted previously to describe the dynamic behavior of LCs. Computational

techniques such as Monte Carlo methods, continuum field theory, density functional theory, lattice Boltzmann technique, etc. have been applied successfully in this regard [71]. However, for systems such as soft matter and complex fluids with mixed constituents which are neither completely solid nor completely liquid, a different approach is required to capture the appropriate length and time scales. Dissipative particle dynamics (DPD) technique is a method which can be more useful for these types of systems as it facilitates the simulation of both equilibrium and transient behavior at physically relevant length and time scales. This mesoscopic simulation technique was first proposed and developed by Hoogerbruggue and Koelman in 1992 [72]. It involves coarse-graining of the system by clustering number of atoms or molecules into single beads. These beads interact with each other according to a soft quadratic potential which imparts the computational efficiency to this technique. As opposed to other equilibrium conditions based simulation techniques, a transient behavior analysis can be performed using DPD under the application of time dependent perturbations. The study of LC–CNT composites, using DPD, under external perturbations such as electric field has not been performed earlier [71]. The work presented here will explore the applicability of DPD method and investigate how CNT and LCs affect the alignment dynamics of each other under external electric field.

The thesis is organized in following sequence. Chapter 2 includes literature survey for CNT–TFT's synthesis, modeling, performance assessment and applications. It also lists the important contributions of the present work. Chapter 3 discusses the modeling approach utilized to study CNT-TFT devices and CNT-LC composite systems. Chapter 4 includes results and discussion of power dissipation in CNT network TFTs with focus on

the role of interfacial thermal conductance. Chapter 5 includes results and discussion on breakdown behavior of CNT network TFTs and how it is affected by channel dimensions and network morphology. Chapter 6 presents analysis on electro-thermal cross-talk among the CNT in aligned CNT-TFTs. Chapter 7 contains the results and analysis on hysteresis behavior of aligned CNT-TFTs. Chapter 8 presents dissipative particle dynamics study of liquid crystal-CNT composites. Chapter 9 summarizes the current work and includes discussion on the scope of future work.

CHAPTER 2: BACKGROUND AND OVERVIEW OF CURRENT WORK

Although MWCNTs were already discovered more than half a century ago, it is only two decades ago that CNTs started gaining significant attention due to their unique one-dimensional structure. Since then constant efforts were made to understand the properties of individual CNTs, and to utilize individual CNTs for electronics applications such as transistors. However, very soon it was realized that the lack of control over the synthesis of CNTs with precise chirality and related variation in electronic properties contributes to a large variation in the device performance. Moreover scalable integration of the CNTs was also a considerable challenge to incorporate CNTs in large scale integrated circuits. Subsequently, large amount of efforts were directed towards solving these critical challenges. In this chapter, a literature survey is presented to summarize the recent progress made and milestones achieved in the area of synthesis, purification, defects removal/reduction, performance improvement and integration of CNTs for nano/micro/macro-electronic applications and devices.

2.1 Synthesis of CNT Networks and Aligned Arrays

Chemical vapor deposition (CVD) is one of the most widely used methods of synthesizing CNTs for electronic applications [73, 74]. In CVD growth, a substrate with catalyst particles (*e.g.,* metal oxide, ferritin, iron, etc.) is placed in a furnace at high temperature (>800 ºC) with a supply of carbon feedstock gas and hydrogen gas; the CNTs are consequently grown directly on the surface of the substrate (Figure 2.1a). If catalyst is spin-cast onto the substrate, CNTs are produced in the form of a random

network. Density and thickness of the CNT network can be controlled using the concentration of catalyst solution, the type of catalyst, and the duration of growth. In order to grow the CNTs in aligned arrays, surface-oriented growth is used where the catalyst is deposited on sapphire or quartz substrate in small stripes perpendicular to the growth direction of the CNTs [12, 62]. The SWNTs preferentially grow towards the areas free of catalysts and along a specific direction on the surface, resulting in densely aligned CNTs between the patterned strips of catalyst (Figure 2.1c).

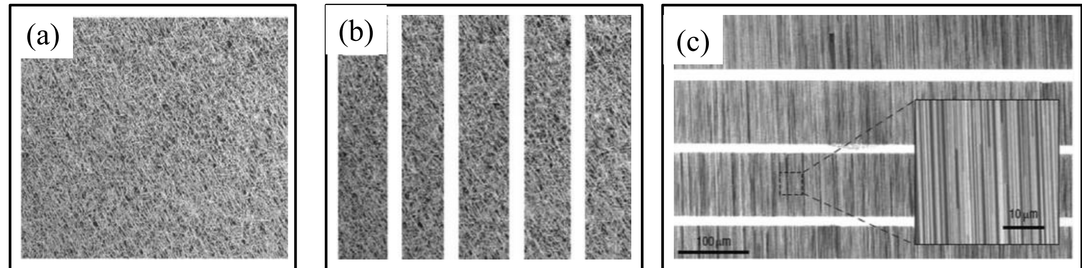

Figure 2.1. (a) A random CNT network grown using CVD grown on quartz substrate. (b) Striped CNT network used to suppress the effects of metallic CNT. (c) Aligned CNT arrays with surface-oriented growth. Adapted with permission from [23, 62]. Copyright (2009) American Chemical Society and (2007) Nature Publishing Group.

It should be noted here that as-grown network or arrays contain both metallic and semiconducting CNTs (in 1:2 ratio statistically). And therefore removal of metallic CNTs or separation of metallic and semiconducting CNTs still remains the most critical challenge. Some promising methods have been proposed and demonstrated. Striping [23, 53] (Figure 2.1b) and electrical burning [57] are arguably the most effective methods (for as-grown random network and aligned arrays of CNTs, respectively) for improving the

performance of CNT-TFTs. For the fabrication of flexible electronics, CNT thin-films need to be transferred to flexible substrates such as poly-ethylene terephthalate (PET), polycarbonate, polyimide etc. CVD grown thin-films have superior electrical performance but also involved multiple processing steps which create difficulty for scalability for large area applications.

To overcome the difficulty faced by CVD grown thin-films, solution-based processing of CNTs have been proposed. Here, CNTs are fabricated in powder form using arc-discharge, laser ablation and high pressure carbon mono-oxide. These CNTs are subsequently purified and dispersed in solution before deposition on the substrate. Solution-based approach allows the CNTs to be sorted based on chirality during or before the deposition. Some of the sorting techniques include DNA-assisted sorting, polymer-assisted sorting, gel chromatography, and density gradient ultracentrifugation (DGU) [75-80]. CNTs obtained through DGU have been widely used for TFT applications due to high fraction of sorted CNTs (up to 99% semiconducting) and ease of availability commercially [79]. The other great advantage of solution-processed CNTs lies in the fact that the deposition can be carried out using ink-jet/aerosol printing which are well-established solution deposition techniques [81, 82]. These processing steps provide a promising way for cost-effective large-area fabrication on the flexible substrates.

2.2 Performance Assessment of CNT-TFTs

Significant progress has been made in recent years towards improving the performance of CN-TFTs. For electrical performance, the important metrics are On-

current, On/Off current ratio, mobility, threshold voltage and subthreshold swing (Figure 2.2). Improvement over all these parameters simultaneously is a challenge which has attracted substantial research efforts.

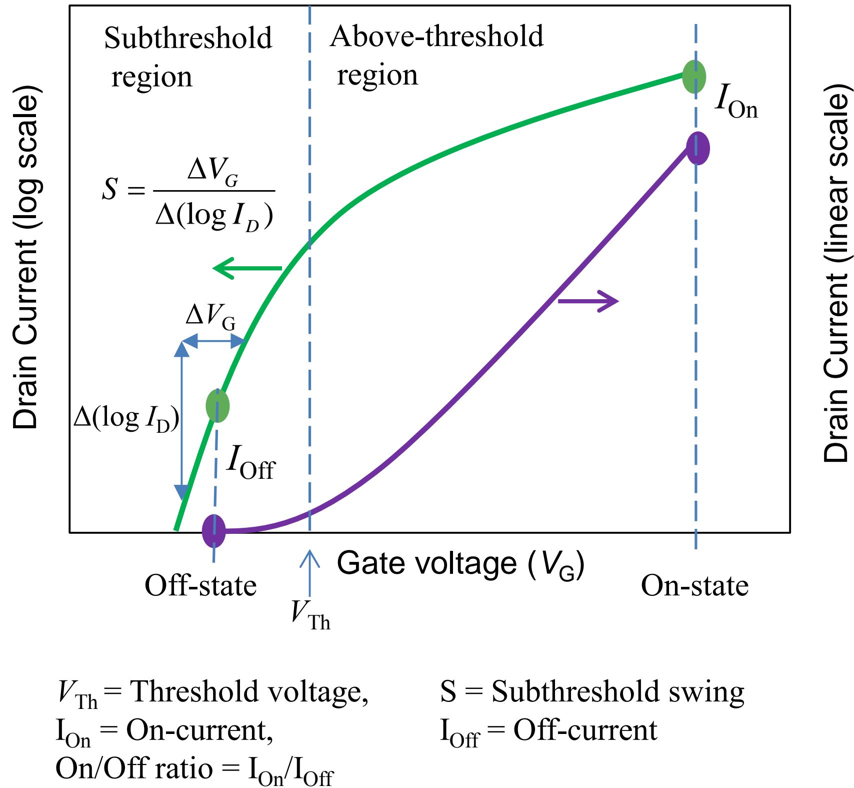

Figure 2.2. Typical current-voltage characteristics (transfer curves) and performance metrics of a field effect transistor.

In an effort to demonstrate improved device performance, Brady *et al.* used polyfluorene as selective agents to obtain highly sorted/purified single-wall CNTs. They fabricated both aligned CNT array-based and percolated CNT network based field effect transistors. For CNT network TFTs of channel length 9 μm, they report On/Off ratio of 2.2×10^7 and mobility as 46 cm^2/Vs. These results are reportedly better than other

solution processed CN-TFTs. For aligned array CNT-TFTs of channel length 400 nm, they reported On/Off ratio and On-conductance as 4 x 10^5 and 61 μS/μm respectively. They used floating evaporative self-assembly technique to obtain aligned arrays of CNTs with density of 50 CNTs/μm [83]. Kane *et al.* compared the device performance with and without the residual surfactant on CNTs obtained from the solution processed purification technique. They removed the surfactant by air oxidation followed by mild annealing. They reported no significant performance change of CN-TFTs [84].

Brady *et al.* fabricated solution processed 99.9% pure semiconducting CNTs based TFTs to show that On/Off ratio more than 10^5 can be obtained. They used ultracentrifugation to remove the metallic CNTs, however CNT lengths become smaller in this process [85]. Derenskyi *et al.* fabricated semi-aligned CNT network TFTs using polymer-wrapped CNTs and report a very high On/Off ratio of 10^8 with mobility of approximately 1cm^2/Vs. They find ambipolar behavior when PF12 is used as the polymer [86]. Kim *et al.* reported CNT network TFTs capable of operating at low voltages. They achieved this by using very thin oxide layer (EOT ~ 3 nm) and solution-processed sorted (99% semiconducting) CNTs. They reported the On/Off ratio of 10^5 and subthreshold swing of 200 mV/decade on average [87]. Wu *et al.*, reported an approach to fabricate densely packed aligned CNT arrays for high On-current density and high On/Off ratio with great degree of reproducibility. They used solution processed sorted CNTs and allowed them to align in bundles in the channel of TFTs with the help of predefined nanostructures called rafts. It is suggested that density of up to 80 CNTs/μm can be obtained using this technique [61].

2.3 Applications and Devices

2.3.1 Flexible circuits

Several key studies report the fabrication of integrated circuits using CN-TFTs with high performance and unique flexible properties to demonstrate their technological and commercial viability.

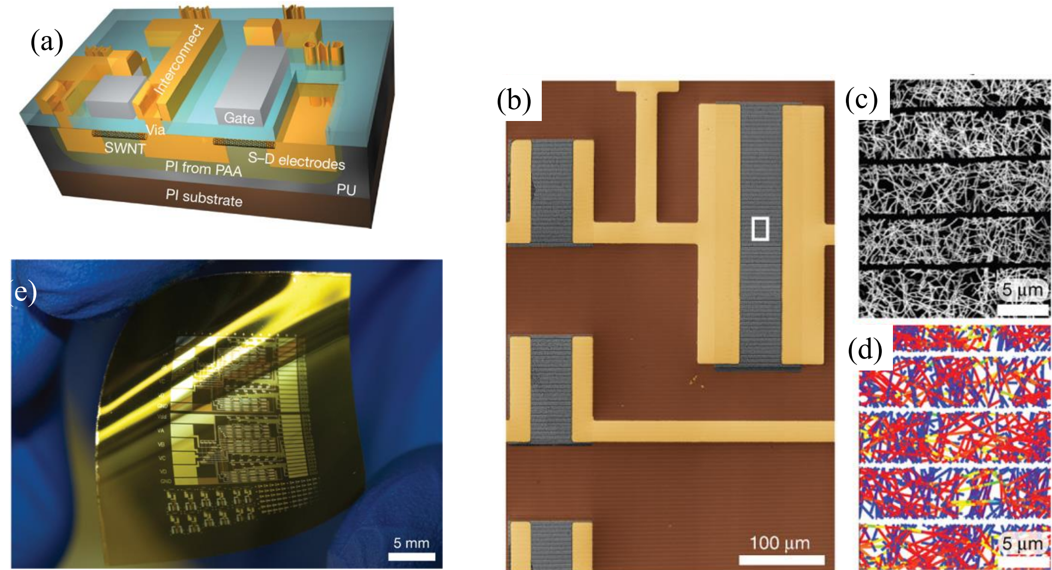

Figure 2.3. (a) Schematic diagram of a CNT network based PMOS inverter on a PI substrate. (PI = polyimide, PU = polyurethane, PAA = polyamic acid). (b) Scanning electron microscope image of part of the CNT circuit, made before deposition of the gate dielectric, gate or gate-level interconnects. Source/drain electrodes are shown in gold, substrate in brown color and CNT network strips in grey color. (c) Zoomed in view of the network strips corresponding to a region of the device channel highlighted with the white box in (b). (d) Theoretical modeling results for the normalized current distribution in CNT network stripes in the on-state of the device, where color indicates current density (yellow for high; red for medium and blue for low). (e) Photograph of the circuits on a thin sheet of plastic. Adapted with permission from [25]. Copyright (2008) Nature Publishing Group.

Cao et al. fabricated integrated circuits on a polyimide flexible substrate (Figure 2.4) based on CVD grown CNT random network-transistors [25]. The largest circuit

being a four-bit decoder consisting of 88 transistors, operated at 1 kHz. The CNT FETs used in the integrated circuits exhibited a mobility of ∼70 $cm^2\ V^{-1}\ s^{-1}$ with On/Off current ratio of 10^3. They fabricated inverters based on the CNT networks with minimal performance variation during bending test on the flexible circuits which underlines the advantage of flexibility of CNT random network-based FETs.

Geier *et al*. built CMOS circuits such as inverter, NAND and NOR logic gates using CNT network TFTs with subnanowatt static power consumption. They made use of enhancement mode p-type and n-type CN-TFTs with distinct and symmetric threshold voltages. They used supply voltage of 0.8 V with rail-to-rail operation, very low power and high gain [88]. Yoon *et al*. reported the fabrication of thin-film CNT based CMOS inverter arrays and ring oscillators on stretchable substrate to demonstrate their potential application in future wearable electronics. They found stable electrical performance of these devices under strain of up to 30%. They showed that the 3-stage ring oscillator have a stable frequency of ∼3.5 kHz at 10 V with uniform waveforms under cycles of strain [59].

Xu *et al*. fabricated highly stretchable CN-TFTs using polyfluorene-wrapped semiconducting single-walled CNTs and a flexible ion gel as the dielectric. These TFTs were able to operate at On /Off ratio 10^4 of and mobility 10 cm^2/Vs under <2 V operating voltage. They found that strain up to 50% can be handled by these TFTs without much degradation in performance [89]. Chen *et al*. fabricated large-scale complementary macroelectronic circuits (logic gates, ring oscillators and logic circuits) on both rigid and flexible substrate using p-type carbon nanotube and n-type indium-gallium-zinc-oxide

thin-film transistors. Thus they overcame the issue of making n-type CNT transistors and p-type metal oxide transistors [90].

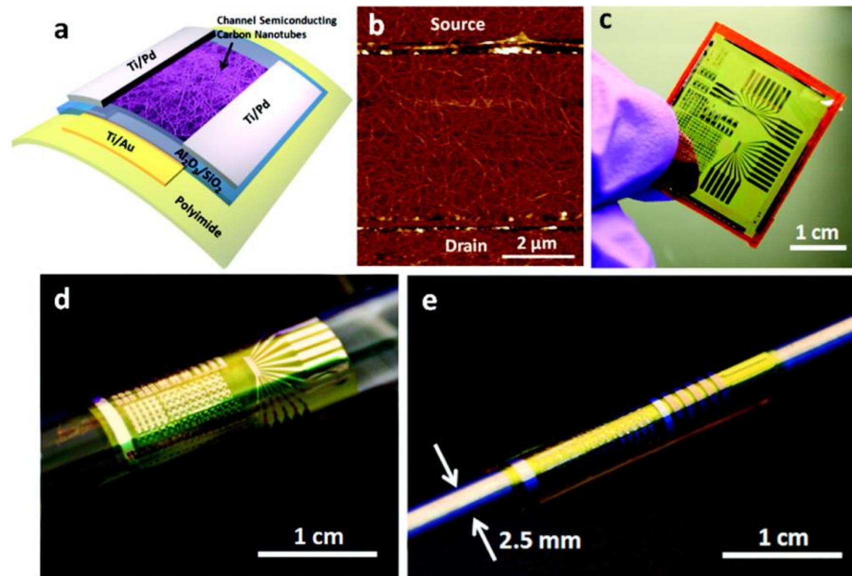

Figure 2.4. Flexible thin-film transistors and integrated circuits using semiconducting CNT networks. (a) Schematic diagram of a local-gated nanotube TFT on a flexible substrate. (b) AFM image showing the channel of the flexible nanotube TFT, which consists of CNT network. (c) Photograph of a flexible nanotube circuit. (d,e) Photographs showing the extreme bendability of the flexible nanotube circuits, where the samples are being rolled onto a test tube with a diameter of 10 mm (d), and a metal rod with a diameter of 2.5 mm (e). Reprinted with permission from [91]. Copyright (2012) American Chemical Society.

Wang *et al*. investigated the application of solution-processed semiconducting carbon nanotube networks for low-cost fabrication of TFTs on flexible substrates. They demonstrated various macro-scale system-level electronics such as flexible integrated circuits, flexible full-color active-matrix organic light-emitting diode display, and interactive skin sensor to simultaneously map and respond to the outside stimulus [92]. Sun *et al*. reported flexible and transparent integrated circuits using all-carbon elements in channel and electrode regions of transistors. They showed very high mobility of nearly

1000 cm^2/Vs and On/Off ratio of 10^5. They also showed extreme biaxial mechanical flexibility of up to 18%. For demonstration, they fabricated an XOR gate and a 1-bit SRAM cell [93].

Lau *et al*. fabricated fully printed CN-TFTs on flexible substrate using inverse gravure printing technique and solutions processed CNTs. They incorporated silver metal for source/drain electrodes and inorganic/organic high *k* dielectric. They reported the mobility of CN-TFTs to be 9 cm^2/Vs and On/Off ratio of 10^5. They also reported that these devices can sustain bending strain of up to the curvature of 1 mm without any significant degradation in electrical performance [94]. Takahashi *et al*. fabricated visible light and X-ray imaging devices on lightweight and flexible plastic substrate by using organic photodetectors on top of active matrix backplane consisting of CNT network TFTs; these TFTs control the pixels. They utilized the high mobility of CN-TFTs and efficient light absorption of organic hetero-junctions. The absorption peak of these devices occurs for green band of visible spectrum while scintillator film on top of the flexible imagers is used for an X-ray imaging [95].

Takei *et al*. fabricated pressure sensors (fondly called whiskers, due to their shape of high-aspect ratio fibers) using composite of carbon nanotube network films and silver nanoparticles. CNTs provide mechanical flexibility/bendability and silver particles improve electrical conductivity and strain-sensitivity. They reported the pressure sensitivity of these sensors to be 10 times higher than earlier reported capacitive or resistive pressure sensors [96]. Wang *et al*. built flexible pressure sensors using CNT network TFTs. They combine TFTs, pressure sensor and OLED arrays on plastic

substrate to directly visualize the pressure applied on the surface with the help of color and intensity of light [97].

2.3.2 Frequency Range

Shulaker *et al*. demonstrated a VLSI compatible approach toward fabrication of aligned array based CN-TFTs with channel length varying from 90 nm to less than 20 nm. They fabricated inverters operating at 1 MHz and an infrared sensor with interface circuit using these CN-TFTs [98]. Lee *et al*. reported single-step synthesis of integrated arrays of field-effect transistors and sensors which were made of carbon nanotube channels and graphitic electrodes and interconnects. These devices were fabricated on flexible substrate capable of being implanted on curves surfaces and as wearable electronics [85]. Shulaker *et al*. also built a working prototype computer using 178 CNT array transistors to demonstrate the feasibility of CNT based computer chips which could compete with Si and could prove to be the candidate for post-Si era to continue the path of chip scaling in terms of size, power and capability as suggested by Moore's law. Their device runs an operating system that is capable of multitasking. They also demonstrated the generality of their device by implementing 20 different instructions from commercial MIPS instruction set. This work may prove to be an important milestone in the roadmap of future electronics in post-silicon era [57]. Pei *et al.*, demonstrated an approach for building complex integrated circuits using individual CNTs with the help of modular components in the form of pass-transistor-logic style 8-transistor (8-T) units. They suggested that their approach can be used to fabricate ICs which are tolerant to CNT

inhomogeneity. They built an 8-BUS system which consisted 46 field effect transistors using 6 individual CNTs [58].

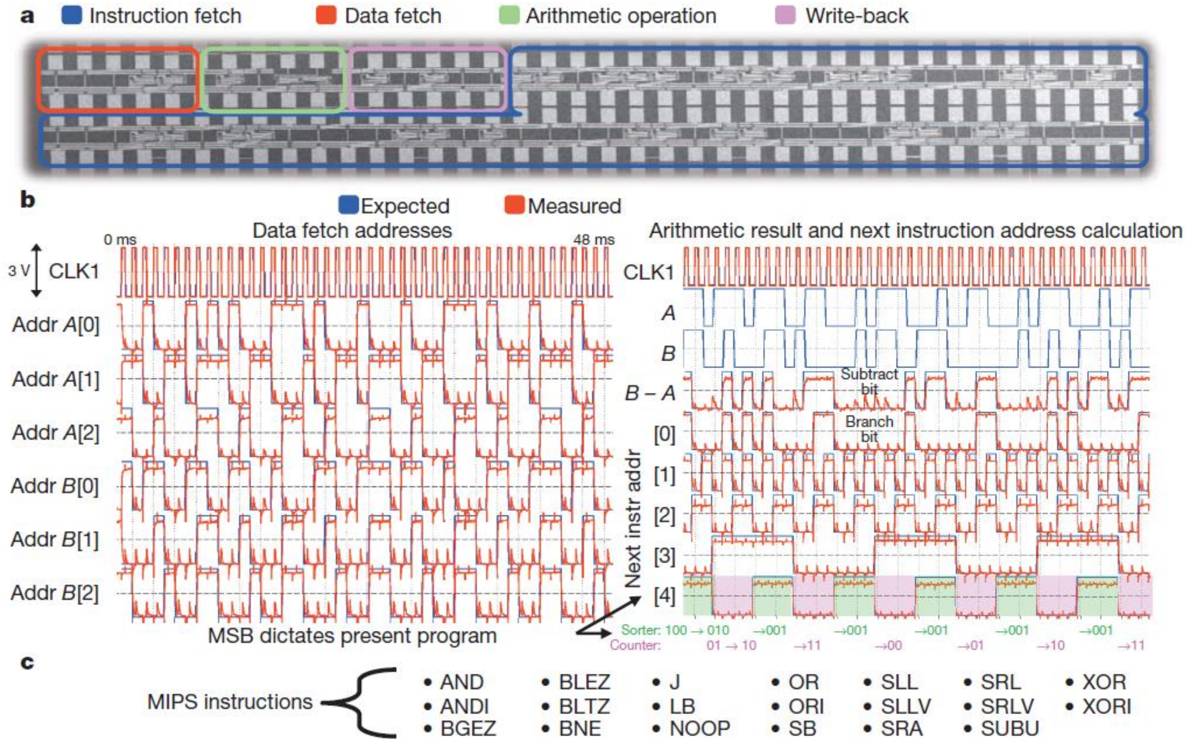

Figure 2.5. (a) SEM of an entire CNT computer. (b) Measured and expected output waveforms for a CNT computer, running the program of arithmetic unit. The exact match in logic value of the measured and expected output verifies correct operation. As shown by the most significant bit (MSB) (denoted [4]) of the next instruction address, the computer is switching between performing counting and sorting (bubble-sort algorithm). The running results of the counting and sorting are shown in the rows beneath the MSB of the next instruction address. (c), A list of the 20 MIPS instructions tested on the CNT computer. Reprinted with permission from [57]. Copyright (2013) Nature Publishing Group.

Wang *et al*. explored the possibility of using as grown CNTs on quartz which included both metallic and semiconducting CNTs for RF application by exploiting the ambipolar nature of CNTs. Ambipolar RF circuits such as frequency multiplier and mixer

fabricated using aligned array TFTs with CNTs grown on quartz. They reported that large diameter CNTs which have low band gaps and more metallic in nature are better suited to ambipolar electronics. They showed that these RF circuits can work up to and beyond 40 GHz frequency [99]. Landauer *et al*. discussed the RF performance potential of CN-TFTs including the impact of noise. They mentioned that the advantage of CN-TFT circuits lies in hundreds of gigahertz frequency operation which are difficult to obtain using Si-based TFTs at similar node technology [100]. Ha *et al*. fabricated five-stage ring oscillators with CNT network TFTs using jet printing technique. They reported the mobility of 20 cm^2/Vs and On/Off ratio of 10^5 for CN-TFTs. They showed that these ring oscillators can be operated at > 20 kHz with stage delay of < 5 μs at supply voltage below 3 V. They employed ion gel electrolyte as the gate dielectric [101].

Gao *et al*. fabricated n-type and p-type CNT network TFTs using passivation layers of silicon nitride and aluminum oxide respectively. They used these complementary transistors in building inverters, NOR, NAND, OR, AND logic gates and ring oscillators. They reported the switching frequencies in the kilohertz range for these devices [102]. Hills *et al.* proposed and demonstrated a systematic approach to deal with the variations in CNT performance due to involved fabrication steps. They studied the impact of CNT variations on circuit delay and noise margin which helped identifying optimized CNT processing and CN-TFT circuit design guidelines [103].

2.3.3 Optoelectronics

Barkelid *et al*. studied the photocurrent generation in CNTs and proposed separate mechanisms for metallic and semiconducting CNTs. They suggested that electrons in

metallic CNTs get thermally excited due to absorption of photons leading to increase in current. For semiconducting CNTs, they attributed photovoltaic mechanism where built-in electric field leads to electron-hole pair generation [104]. Xie *et al*. presented the mechanism for electroluminescence in aligned arrays of individual SWNTs. They suggested that exciton mediated electron/hole recombination near the lower work-function contact was mainly responsible for photon emission. They also reported high current thresholds for electroluminescence in these devices due to diffusion and quenching of excitons in the vicinity of metal contact [105]. Sczygelski *et al*. studied photocurrent responses of CN-TFTs fabricated using 99% sorted CNTs and hybrid organic/inorganic substrate. They performed temporal, spatial and spectral photocurrent microscopy for their study. They found that photocurrent in the depletion region was caused by extrinsic transient displacement current while the photocurrent in the accumulation region arises from intrinsic inter-band excitation in CNTs [106]. Zaumseil *et al*. carried out mapping of charge carrier distribution (spatial resolution 300 nm) in CN-TFTs using G' peak shift in Raman spectroscopy. Using this approach, they studied channel pinch off and saturation behavior in CN-TFTs [107].

2.4 Tuning of Properties of CNT-TFTs

2.4.1 Chirality

Darchy *et al*. presented an approach for improving the semiconducting properties of CNT networks which typically contain both metallic and semiconducting CNTs. They chemically treat CNTs using diazoether which inactivates metallic CNTs. These treated CNTs provide much better performance in terms of high On/Off ratio in CN-TFTs. It

could be inexpensive sorting method for semiconducting methods [108]. Li *et al*. proposed a technique to convert metallic CNTs into semiconducting ones. They immersed as grown metallic CNTs into acid yellow (an electron acceptor organic compound) and found that originally metallic CNTs behave as semiconducting CNTs. It improved the On/Off ratio of CNT TFT by three orders of magnitude [109]. Ford *et al*. demonstrated a method of selectively removing metallic CNTs from the CNT network. They performed alkylation and annealing followed by chloroform treatment to physically remove the metallic CNTs from the network deposited on SiO_2/Si substrate [110]. Jin *et al*. presented a method of obtaining aligned semiconducting CNTs for high performance logic devices. They used the principle of thermocapillary combined with reactive ion etching to expose and remove metallic CNTs from the arrays of aligned CNTs grown on quartz. Once metallic CNTs were removed, the remaining (semiconducting) CNTs were transfer printed on to the substrates for fabrication of field effect transistors. They reported the mobility of these TFTs to be 1000 cm^2/Vs and On/Off ratio of 10^4 [111].

Sanchez-Valencia *et al.* presented a unique method for synthesizing CNTs of pre-defined single chirality. They used template molecules deposited on substrate as the seeds for growing CNTs. This demonstrated the potential of this technique by growing (6,6) armchair CNT by using surface-catalyzed cyclo-dehydrogenation as seed molecule on a platinum (111) surface. They fabricated single-chirality and defect-free SWCNTs with lengths up to a few hundred nanometers [112]. Tian *et al*. explored the change in the conductivity of metallic and semiconducting thin film network with the help of metal deposition. They reported that covalent bond formation at the CNT junctions helped improve the conductivity of these percolating network [113]. Wang *et al.* proposed a

method of tuning the threshold voltage of CN-TFTs using 1H-benzoimidazole derivatives processed via either solution coating or vacuum deposition. Using this approach they fabricated CMOS inverter and logic gates on flexible substrate with rail-to-rail output voltage swing and sub-nanowatt power consumption [114]. Lobez *et al*. proposed a method for selective deposition/assembly of high density thin film of CNTs on HfO_2 over SiO_2. They accomplished this by covalent functionalization of CNTs using organic moieties bearing hydroxamic acids [6].

2.4.2 Electrical Contacts/Junctions

Sarker *et al*. experimented with metallic CNTs employed as source/drain electrodes for aligned array CNT TFTs. Here, aligned metallic CNTs were used as electrodes and aligned semiconducting CNTs were used as channel. They reported one order of magnitude improvement in On/Off ratio compared to Pd contacts with the same channel length and CNT density in channel. They attributed this improvement in performance with metal CNT electrodes to low Schottky barrier at contacts [115]. Franklin *et al.* studied contact resistance of CNT-metal interfaces at source and drain electrodes by employing different metals. They found that at short contact lengths (<20 nm), Rh can give lower contact resistance compared to other commonly used metals such as Pd [116]. In another study, Franklin *et al*. fabricated an all-around gate CNT transistor. They showed that both p-type and n-type transistors can be made by using suitable oxide, i.e., HfO_2 for n-type and Al_2O_3 for p-type [117]. Do *et al*. proposed an approach to reduce electrical resistance at the CNT junction in CN-TFTs. They utilized the excessive Joule heating at the junction by passing the gaseous particles of metals which get deposited at

the junctions due to high local temperature. This approach is self-limiting due to immediate decrease in the junction temperature due to metal deposition prevent further metal deposition. The effectiveness of the method depends on the metal being used for deposition. It is reported that an order of magnitude improvement can be achieved using this method with Pd deposition [118]. Choi *et al*. made short channel (15 nm) CNT transistors using solution processed CNTs with top gate geometry and dielectric ZrO_2 as gate insulator. They suggested that although the intrinsic field-effect mobility of these CNTs is lowered compared to as grown CNTs from chemical vapor deposition technique, the contact resistance between metal source/drain electrodes and CNTs is not degraded which helped obtain high performance from solution processed CN-TFTs [119].

2.4.3 Hysteresis

Ha *et al*. showed that fluorocarbon polymer encapsulated CNTs in CN-TFTs can help reduce hysteresis and produce operational stability in air and water. They claimed that the hydrophobicity of fluoropolymers removed water molecules from the vicinity of CNTs to avoid water-assisted charge trapping. In addition the dipole associated with carbon fluorine bonds also provides screening from trap charges in the oxide layer. Thus, fluorocarbon encapsulation technique was proposed to be a promising approach to enhance device reliability and stability [120]. Tunnel *et al*. presented a measurement approach of obtaining hysteresis free transfer characteristics of CN-TFTs which suffered from oxide trap charges and interface charges caused by fabrication methods. They employed series of positive and negative gate voltages with progressively smaller amplitudes to achieve neutral charge distribution in the device. Approximately 200

aligned SWNTs were grown using CVD on quartz. CNTs were encapsulated by 65 nm of an Al_2O_3 dielectric layer, on top of which a gold top-gate electrode is deposited. The channel width and length were 100 μm and 10 μm, respectively, and gate width was 8 μm. The source, drain, and gate electrodes were composed of 50 nm of gold, with a 5 nm titanium adhesion layer [121]. Lee *et al.* investigated the effect of different passivation layers (Al_2O_3, HfO_2, polymer) for CN-TFT on SiO_2/Si. They found Al_2O_3 to be the best passivation layer during gate bias stress stability tests [122]. Wang *et al*. fabricated double gated CNT network transistors using fluorinated top gate dielectrics to get rid of hysteresis and obtain transistors with high electrical stability under bias stress tests. They were able to control the threshold voltage using the bottom gate bias. They also observed both unipolar and ambipolar behavior when specific top gate dielectrics were used [123]. Qian *et al*. explored the reasons for p-type conduction in CNTs in CN-TFTs. They conducted experiments to test two major and commonly attributed hypotheses which are electrostatic doping at the contacts and doping effects of oxygen adsorption. Based on experiments they ruled out contact doping as the reason for p-type behavior. They suggested that trap charges induced by oxygen-water redox at CNT-substrate interfaces created trap density states near the edge of conduction edge causing poor gate modulation for electron conduction leading to only p-type behavior of CN-TFTs [124].

2.4.4 Thin-film Fabrication

King *et al.* fabricated liquid crystal films of semiconducting CNTs using vacuum filtration method. Thin-films of varied degrees of alignment of CNTs were used for CN-TFTs. They reported significant variation in the CN-TFTs performance in terms of

On/Off ratio, mobility etc. They also reported optical and electrical conductivity values to underline the transparent nature of CNT films [125]. Kim *et al.* combined CNTs and graphene to fabricate transparent electrodes and TFTs. They controlled the density and alignment of CNTs using the speed of spin-coating process. They reported an improvement of On-current and On/Off ratio of fabricated TFTs comparable to pristine graphene TFTs[126]. Wang *et al*. studied polymer-CNT hybrids as semiconducting material in field effect transistors. They reported that CNT dispersion of CNTs below percolation threshold in polymer improved the charge injection for electrons and holes in top-gate TFTs causing lower contact resistance and reduced threshold voltages [127]. Kim *et al*. fabricated CN-TFTs on ZrO_2 using inkjet printing method. They reported the mobility of the device to be 30 cm^2/Vs and On/Off ratio 10^5 at low operating voltages. They found that ultraviolet ozone treatment of the oxide substrate is important for achieving high performance by uniform dispersion of sorted CNTs. They suggested that single-pass inkjet printing process is both reliable and scalable [81]. Niu *et al*. demonstrated a method for obtaining ultrathin CNT thin films using electrostatic adsorption technique. They used these ultrathin CNT films to fabricate flexible and transparent supercapacitors with high electrochemical performance to showcase the capability of the method involved [128].

2.4.5 Miscellaneous

Simoneau *et al*. studied the effect of statistical distribution of different parameters used to describe the structure and electrical characteristics of CN-TFTs. They report that structural parameters such as length, diameter and angle can have significant impact on

physical properties but statistical distribution of CNT junction resistance does not cause significant effect beyond percolation threshold. Therefore, for high density network, an average value of CNT-CNT junction resistance can be used to describe the transport in the percolating network [129]. Kim *et al*. investigated the effect of strain on the performance of CN-TFTs. They found that the strain applied on the CN-TFTs caused the On-current and mobility to be lowered by nearly 15 % and 5 % respectively probably due to fracture/cracks in the CNT network which are irreversible damage to CN-TFTs [130]. Blancon *et al*. investigated the effects of pressure induced strain on individual CNT field effect transistor. They varied the pressure in the range of 10 kPa to 900 MPa. They proposed that at ambient temperature and high pressure intrinsic properties of CNTs and at CNT-metal interface affected the performance of CNT TFTs. They observed coulomb blockade at low temperature (<10 K) and high pressure (4.5 kbar). They also reported that ballistic nature of the electron transport remained intact even at high pressure [131]. Yano *et al*. demonstrated a nanoscale imaging technique using tip-enhanced Raman spectroscopy. They performed color-coded imaging of highly strained CNTs to visualize the distribution of strain also the CNT. They showed that structural properties of nanomaterials could change under strain and be manipulated using this technique [132].

2.5 Modeling and Simulation

2.5.1 CNT Network and Aligned Array TFTs

Wahab *et al*. studied partial gate CNT transistor operation by simulating 3D geometry and periodic boundary condition in width direction for aligned array CNT transistor. They reported that 3D electric fields terminating into 1D CNTs can affect both

On- and Off- currents irrespective of gate oxide thickness, dielectric constant or CNT diameter. They performed the simulations by solving Poisson's equation and drift-diffusion model self consistently. They consider recombination-generation, band-to-band tunneling, impact ionization and Schottky barrier tunneling in the current continuity equations [63].

Behnam and Ural employed Monte Carlo Simulations to study the electrical resistivity dependence of carbon nanotube network on geometrical parameters such as nanotube length, network density, CNT alignment and ratio of junction resistance to CNT resistance [133, 134]. They found that resistivity of the network increases with the increased density and decreases with the CNT length. They found that partially aligned CNTs show the least resistivity. They also reported that stronger scaling is observed when the transport is dominated by junction electrical resistance. They found that longer CNTs, denser networks, and shorter devices decreases the the alignment angle at which minimum resistivity occurs.

Sano and Tanaka proposed a simplified drain current model for CNT network TFTs and compared the results with experiments. They used a tunneling current model based on WKB assumption across a CNT junction and solved it self-consistently with resistive network current equations to obtain drain current [135]. Li *et al*. fabricated a short channel CNT TFT using Si substrate as source and Cr/Au as drain electrode. The geometrical location of source/drain and gate electrodes with respect to CNTs is referred to as vertical CNT-TFT by the authors. They explain experimental transfer characteristics of TFTs by modeling the device in the ballistic transport regime for electrical transport [136]. Joo *et al*. performed static and low noise characterization of n-type CN-TFTs.

They studied output and transfer characteristics for different gate lengths and evaluated gate-coupling capacitances. They also developed 2D percolation model of CN-TFTs. They used 1D capacitance model to explain the experimental and simulation results [137].

Pimparkar and Alam studied the CNT network TFTs using resistive network model based on stick-percolation theory. They defined the mobility of CN-TFT using a bottom-up approach to capture the effect of percolation transport in CNT network. By this approach the mobility includes the effect of CNT network density, CNT length, channel length and CNT junction resistance. This redefined mobility and compared it with amorphous silicon or p-silicon based TFTs to assess the performance improvement of CN-TFT over Si-based TFTs [138]. In another study [53], Pimparkar *et al*. investigate the technique called "striping" to reduce the effect of metallic CNTs present in the network. In this technique, CNT network is divided into multiple stripes in the width direction of the channel. This reduces the probability of forming percolating pathways across the channel by metallic CNTs. They conducted both experiment and simulations to explore the efficacy of this technique. They utilized drift-diffusion and Poisson's equation for CNT network to model the electrical transport. Pimparkar *et al*. [139] also compared the performance of aligned CNTs with random network based transistors. They varied the CNT length and alignment of CNTs to analyze their effect on device performance.

Kumar *et al*. [16] computed the conductivity of finite size percolating network using drift-diffusion theory. They studied the scaling of electrical conductivity of percolating network with channel length for various densities. Experimental validation of their results suggested that electrical transport in CNT network transistors can be

understood using finite size stick percolating network. Kumar *et al*. [140] also studied the electrical transport properties of CNT-organic matrix composites based TFTs. They applied drift diffusion theory for linear regime of transistor operation. They found that the effective channel length scales with CNT concentration in the organic semiconducting host material where CNT concentration even below percolation threshold is found to significantly affect the transistor characteristics. Here organic material is Kumar *et al*. [41] also calculated the effective thermal conductivity of 2-dimensional CNT composites. They employed Fourier's law for conduction coupled with stick percolation network model for calculating the temperature profile and thermal conductivity of the composite. Their study underlined the effect of percolation in calculation of CNT-CNT and CNT-substrate thermal resistance in CNT composites. Kumar *et al*. [141] further coupled the electrical and thermal transport models which were developed in earlier studies to describe current and temperature distribution in CNT network based TFTs for electronic display application. They studied the correlation between device performance (On current, temperature rise) and device parameters such as channel length, network density, CNT-substrate thermal conductance and CNT-substrate thermal conductivity ratio.

It should be pointed out at this point that governing equation and model for electrical and thermal transport can vary depending on the length scales of electrical and thermal transport. If average mean free path of carriers (electrons/holes in electrical transport; phonons in thermal transport) is much smaller than the CNT length, diffusive transport models are applicable (as used in the present work). However, if the average mean free path of carriers is comparable to or greater than CNT length, ballistic transport equations have to be applied for the modeling and simulation.

For example, Ouyang and Guo [142] performed atomistic quantum transport simulation using non-equilibrium Green's function (NEGF) to analyze the performance of quasi-ballistic CNT array transistors with channel length of 100 nm. They solved quantum transport equations along with Poisson's equation self-consistently using method of moments. They studied the effect of CNT diameter variation and CNT mis-alignment on transistor performance.

2.5.2 Liquid Crystal - CNT Composites

Hoogerbruggue and Koelman (1992) developed a mesoscopic method called Dissipative Particle Dynamics (DPD) for simulating complex hydrodynamic phenomena. They showed that the quantitative description of isothermal Navier-Stokes flow can be obtained with relatively few particles. This method was conceived as an improvement over conventional molecular dynamics (MD) simulations, computationally [143]. The particles (termed as beads) in DPD represent cluster of atoms or molecules and follow Newton's law of motion such that the momentum is conserved of the system while the energy is not conserved. Thus by introducing dissipation in molecular dynamics simulation with suitable coarse-graining, the hydrodynamic behavior (which requires considerably larger length and time scales compared to size and collision times of the individual molecules, respectively) is observed. For systems such as polymer-mixtures, colloids, micelles and networks DPD simulations can be faster than MD by many orders of magnitude, depending on the scaling factor chosen for the simulation. This brings phenomena of microseconds in reach of routine simulation, while maintaining a fairly accurate representation of the structure of the molecules.

Hoogerbruggue and Koelman further studied the flow of suspensions of solid spheres under steady shear using the DPD method. They were able to perform extensive 3D simulation to study the complicated interplay between hydrodynamic interactions and solids' variable configuration under flow conditions in which large departures from equilibrium configurations can exist. [144].

Groot and Warren presented the critical review of DPD as a mesoscopic simulation method. They suggested useful parameter ranges for simulations, and established a link between these parameters and chi-parameters in Flory-Huggins-type models. This link opened the way to do large scale simulations, effectively describing millions of atoms, by firstly performing simulations of molecular fragments retaining all atomistic details to derive chi-parameters, then secondly using these results as input to a DPD simulation to study the formation of micelles, networks, mesophases and similar systems. As an illustration they calculated the interfacial tension between homopolymer melts. They also analyzed and discussed the use of DPD to simulate the dynamics of mesoscopic systems, and indicate a possible problem with the timescale separation between particle diffusion and momentum diffusion (viscosity). [145].

For the direct simulation of mixed surfactants near oil-water interfaces, or for the simulation of Coulombic polymer-surfactant interactions, DPD is considered to have many advantages over full atomistic MD simulations. Groot first incorporated the electrostatic interactions in DPD simulations where the electrostatic field was solved locally on a grid which allows local inhomogeneities in the electrostatic permittivity. Key issues like the screening of the potential near a charged surface and the Stillinger-Lovett moment conditions were satisfied in such a way that the method captured the essential

features of electrostatic interaction. He studied the interaction between a cationic polyelectrolyte and anionic surfactant. The behavior of these systems as observed through the DPD simulations was in close agreement with theoretical predictions and experimental observations [146].

Gonzalez-Melchor *et al*. proposed an alternative way to calculate the electrostatic interactions in DPD simulations. They applied standard Ewald sum method to study bulk electrolyte and polyelectrolyte-surfactant solutions. They included charge distributions on DPD particles to prevent artificial ionic pair formation. They studied the structure of the fluid through the radial distribution function between charged particles. They found that their results were in good agreement with those reported by Groot for the same systems [147].

Li *et al*. studied the process of polymer translocation through a narrow pore using a DPD method. They included a rigid core in each particle to avoid particle interpenetration problems based on the original DPD method. Electrostatic interactions of charged particles were represented through screened Coulombic interactions. They correlated the average translocation time with polymer length and found a scaling law where the scaling exponent depended on the solvent quality. They suggested that the dynamic behaviors of various polymer and DNA molecules during translocation processes can be explored and understood using DPD method [148].

Zhao *et al*. studied the phase behavior of lyotropic rigid-chain liquid crystal polymer using DPD for varied solution concentration and temperature. They used a chain of fused DPD particles to represent each mesogenic polymer backbone surrounded by solvent molecules. The free solvent molecules were modeled as independent DPD

particles. They found that different combinations of anisotropic and isotropic phases existed corresponding to different range of values of the temperature and solutions concentration. The temperature-dependent phase transitions were found to occur in the high concentration range. Co-existence of the anisotropic phases and isotropic phase was observed in the intermediate concentration range. By calculating the mole fraction and compositions of the co-existed phases, they found that the concentration of rigid rods in isotropic phase increased for higher temperature. They also obtained the phase diagrams of the lyotropic rigid-chain polymer liquid crystal from DPD simulations. They found that presence of solvent particles in the DPD simulation was critical to predict the phase co-existence and obtain the phase diagrams [149].

2.6 Research Contributions of the Current Work

Following points outline the important findings and the major contributions of the current work:

(1) An extensive computational model is developed to describe the coupled electrical and thermal transport in carbon nanotube network/array based thin-film field effect transistors.

(2) The developed electro-thermal model for CNT network thin-film transistor (CN-TFTs) is employed to investigate the heat dissipation and network breakdown in CN-TFTs with the additional help of molecular dynamics simulations of the junctions, and experimental data on power dissipation (obtained by collaborators, Prof. Eric Pop's group, UIUC). Comparison of the measured CN-TFT power vs. source-to-drain voltage and temperature profiles with the corresponding

numerical results allows us to extract thermal boundary conductances (TBCs) at both CNT junctions (~2.4 pWK^{-1}) and CNT-substrate (~0.16 $Wm^{-1}K^{-1}$) interface simultaneously. The method followed here can be a valuable tool to extract interfacial thermal contact resistances for CNT networks on different substrates.

(3) The temperature profile of the CNT network which may be very difficult to gather directly from the experiments are obtained using the computational approach. The model provides useful insights about the role of the two aforementioned TBCs in power dissipation and electrical breakdown of CN-TFT devices. It is found that the key to enhance the power density capability and device reliability lies in the improvement of CNT-substrate TBC. The effects of network morphology parameters such as network density and junction topology on network breakdown have been investigated. It is noted that that the CNT junctions are the likely locations of the hot spots not because of poor CNT-CNT thermal conductance but rather due to the absence of direct contact of buckled part of CNTs with the substrate at crossed CNT junctions. The denser network may adversely affect the device reliability as the higher percentage of CNTs may not be in direct contact with the substrate. The results indicate that higher network density leads to higher power density in the network and consequently the breakdown occurs at lower source-to-drain voltage. The analysis suggests that the CN-TFT performance and reliability can be significantly enhanced by improving the CNT-substrate interactions and optimizing the network morphology.

(4) The breakdown characteristics such as peak power (or breakdown power, P_{BD}) and the corresponding source-to-drain voltage referred to as the breakdown

voltage (V_{BD}) of CN-TFTs in order to find their relation with the channel geometry (length L_C, width W_C) and network morphology (CNT length and alignment distribution) parameters. The analysis presented here, provides new insight into optimizing the device parameters in order to enhance thermal reliability and performance uniformity of CN-TFTs.

(5) The coupled electro-thermal model for aligned CNT array TFTs is used to study how electrostatic screening among CNTs affects the overall electrical and thermal performance of these devices as a function of CNT array density and dielectric oxide thickness. The results indicate that the current per CNT decreases due to charge screening as the CNT density increases but the device On-current and the On/Off ratio can increase substantially for denser arrays and therefore the denser arrays of CNTs in TFTs can benefit device electrical performance significantly particularly for logic devices. However gate oxide thickness needs to be optimized with array density for better electrical and thermal performance. Results indicate that the targeted array density (>100 CNTs/μm) for high performance CNT array based TFTs can present thermal reliability issues emphasizing the importance of design optimization of TFTs for efficient thermal management of the large scale integrated circuits.

(6) Hysteresis in aligned CNT TFTs due to the presence of interface and bulk trap charges has been studied using a computational model. The approach presented here is useful for obtaining precise quantitative information about the role of several parameters such as defect concentration and location, oxide thickness, gate voltage sweep rate and CNT array density in hysteresis. The results and

insights presented here can be utilized for optimizing fabrication strategies to minimize hysteresis in CNT TFTs.

(7) A mesoscopic simulation technique called dissipative particle dynamics (DPD) is applied to study the behavior of liquid crystals (LC) –CNT composites under the application of DC and AC electric fields. DPD being a relatively new technique has not been well explored particularly for studying the dynamic behavior of LC systems and their colloids under an electric field. Our analysis suggests that the coarse-grained model of the LC (~4-cyano-4'-pentylbiphenyl in present study) can retain most essential features of this LC molecule with rigid backbone and flexible tail. DPD is able to describe relevant physical behavior of LC system both in equilibrium and under an electric field. Results are consistent with the experimental observations of rotational viscosity and also for the presence of anisotropic nematic phase at room temperature. This technique is found to be very promising to examine the properties of CNT-liquid crystals composites for various practical applications. The modeling framework established here may be very useful for the future work in this direction.

CHAPTER 3: METHODOLOGY

3.1 Modeling of CNT network TFTs

In order to investigate the electrical and thermal transport in CNT TFTs, a coupled electro-thermal computational model is developed. The model is based on the semi-classical drift-diffusion equations for charge transport in the CNTs and diffusive thermal transport equations for the CNTs, Si, and SiO_2 layers considering all interfacial contact resistances. It provides the basic framework to obtain and analyze the current, power, and temperature distribution in the device as a function of various device parameters [35, 52, 150-152] and simulate the network breakdown process to study the thermal reliability aspects. A description about the governing equations is provided below.

3.1.1 Thermal Transport

The thermal transport in the device consisting of CNT-network, oxide layer and Si substrate is simulated using the diffusive energy transport equations, which can be written in the following non-dimensional form [151]:

$$\frac{d^2\xi_i}{ds^{*2}} + Bi_S\left(\xi_{\mathrm{OX}} - \xi_i\right) + \sum_{\substack{\text{intersecting} \\ \text{tubes j}}} Bi_C\left(\xi_j - \xi_i\right) + \frac{d}{L_t}\frac{q_i^{'}}{Q^{'}} = 0 \tag{3.1}$$

$$\nabla^{*2}\xi_{\mathrm{OX}} + \sum_{i=1}^{N_{tubes}} Bi_S\gamma\left(\xi_i - \xi_{\mathrm{OX}}\right) = 0 \tag{3.2}$$

$$\nabla^{*2}\xi_{\mathrm{Si}} = 0 \tag{3.3}$$

Here, $\xi = (T-T_\infty)/(Q^{'}dL_t/k_t)$ is the non-dimensional form of temperature (T). T_∞ denotes the ambient temperature, $Q^{'}$ is a reference power per unit volume, d is the diameter of CNT, and k_t is the axial thermal conductivity of CNT. ξ_i, ξ_{OX} and ξ_{Si} are the non-dimensionalized temperatures of a node on the ith CNT, oxide, and Si, respectively. Asterisk symbol is used to refer to length variables which are non-dimensionalized by d. Equation (3.1) governs the temperature of any i^{th} CNT along its axial direction (length variable s); the second and third terms in this equation represent thermal interactions at CNT-oxide interface and at CNT-CNT junctions, respectively. $q_i^{'}$ is the volumetric Joule heating term within the CNT which is obtained from the solution of electrical transport equations (discussed below). Bi_C and Bi_S represent the non-dimensional thermal contact conductance at CNT-CNT junctions and CNT-oxide interface respectively. Their values (Bi_C = 10^{-7} and Bi_S = 200) are obtained by comparing the power-voltage curves obtained from the experiments against the simulations [35]. Equation (3.2) describes the temperature in the oxide layer and the second term in this equation represents CNT-oxide thermal interaction, which is summed over all the CNTs. The parameter γ in this term characterizes the contact geometry. Equation (3.3) describes the temperature of the Si layer. The dimensionless parameters in these equations are defined as [41, 151]:

$$Bi_C = \frac{h_C P_C d^2}{k_t A}; \quad Bi_S = \frac{h_S P_S d^2}{k_t A}; \quad \gamma = \alpha_v \left(\frac{A}{P_S} \right) \frac{k_t}{k_S}$$

Here, h_C and h_S represent heat transfer coefficients at CNT-to-CNT and CNT-to-substrate contacts respectively, P_C and P_S are the corresponding contact perimeters, k_t is the thermal conductivity of the CNT, k_S is the thermal conductivity of the substrate and A is its cross-sectional area. The parameter γ characterizes the contact geometry and α_v is the

contact area per unit volume of substrate. A constant temperature boundary condition, $T = 300$ K, is applied at the bottom surface of Si substrate, while at the top surface of the oxide layer, a convective boundary condition is applied. The convective boundary condition can be expressed as $-k_S dT/dz = h(T - T_\infty)$, where T_∞ = 300 K is the ambient temperature and h is the heat transfer coefficient at the top of the oxide substrate. The lateral boundaries of the computational domain have been assumed to be thermally insulated.

3.1.2 Electrical Transport

The electrical transport in the carbon nanotubes has been described by Poisson's equations and current continuity equations as follows [17, 52, 151]:

$$\frac{d^2\psi_i}{ds^2} + \frac{\rho_i}{\varepsilon} - \frac{(\psi_i - V_G)}{\lambda^2} + \sum_{j \neq i} \frac{(\psi_j - \psi_i)}{\lambda_{ij}^2} = 0 \qquad (3.4)$$

$$\nabla . J_{pi} + \sum_{j \neq i} C_{ij}^p (p_j - p_i) = 0 \qquad (3.5)$$

$$\nabla . J_{ni} + \sum_{j \neq i} C_{ij}^n (n_j - n_i) = 0 \qquad (3.6)$$

Here, ψ is the electrostatic potential, V_G is the gate voltage, ρ is the net charge density, ε is the permittivity of CNT. The third term in Poisson's equation represents the gating effect [151] with screening length, $\lambda = (\varepsilon_{CNT}\, t_{OX}\, d/\varepsilon_{OX})^{0.5}$. Here, ε_{CNT} and ε_{OX} are the dielectric constants for the CNT and gate oxide respectively and t_{OX} is the oxide thickness. The fourth term in Equation (3.4) describes the inter-tube electrostatic interaction at CNT-CNT junctions with screening length, $\lambda \sim d$. Equations (3.5) and (3.6) are current continuity equations for holes and electrons respectively, where J is current

density given by drift-diffusion equations. Hole and electron charge density are represented by p and n, respectively. The second term, $C_{ij}^{n}(n_j - n_i)$ or $C_{ij}^{p}(p_j - p_i)$, in the continuity equations represents charge (electrons or holes) transfer across the CNT-CNT junctions.

Heterogeneous networks of metal (*M)* and semiconducting (*S)* type CNTs (1:2 ratio) are considered in all simulations unless specified otherwise. The charge transfer coefficient ($C_{ij}^{n,p}$) is considered zero for *M-S* junctions to account for very low contact conductance compared to the *M-M* and *S*-S junctions [45]. These assumptions have been employed in the previous study, where the developed model has successfully explained the experimental observations [20, 35, 53]. Experimental studies have also shown that the electrical resistance at heterogeneous junctions (*M-S*) is 2 orders of magnitude larger than at homogenous junctions (*M-M* or *S-S*) [45]. The electrical conductivity of *M*-CNTs is considered to be five times larger than that of *S*-CNTs according to the experimental measurements [56].

The numerical values of major parameters in Equations (3.1-3.6) are provided in Table 3.1. These electro-thermal equations are solved self-consistently to obtain the current, potential and temperature distribution in the CN-TFTs.

Drift-diffusion and Poisson's equations are solved self-consistently to obtain the current-voltage distribution and the power dissipation in the CNT network. The power distribution is taken as input for the thermal simulations to obtain the thermal profile in the device.

Table 3.1 Table of Parameters used in Electro-Thermal Model

Variable	Name	Nominal Value
$\xi = (T-T_\infty)/(Q' dL_t/k_t)$	Non-dimensional Temperature	-
T	Temperature	(Kelvin)
T_∞	Ambient Temperature	300 K
Q'	Reference Power	1 W
d	Diameter	1 nm
L_t	CNT length	1 µm
k_t	Thermal conductivity of CNT	1000 W/mK
t_{OX}	Oxide thickness	300 nm
t_{Si}	Si thickness	500 µm
Bi_S	Non-dimensional thermal conductance at CNT-oxide interface	2×10^{-4}
Bi_C	Non-dimensional thermal conductance at CNT-CNT junction	10^{-7}
k_{OX}	Thermal conductivity of oxide	1 W/mK
C_{ij}	Charge transfer coefficient	50

The model provides comprehensive details of the temperature and power distribution within the CNT network and thermal transport across substrate (Si) and insulator (SiO_2). Since these details are very difficult to obtain directly from the experiments, the model serves as an essential tool in analyzing the high-field transport and breakdown of CN-TFTs.

3.2 Modeling of Aligned CNT TFTs

The governing equations used to obtain current and potential distributions in the aligned CNT array TFTs are presented below. The schematic of aligned CNT -TFT is shown in Figure 1.2. Method of moments (MoM) approach is used to solve 3D Poisson's equation (Eq. 3.7, 3.8) self-consistently with current-continuity equations (Eq. 3.9) to obtain electrostatic potential and current in CNTs arrays [142]. Here, J is the current density, μ is the electron/hole mobility [63], n/p is the electron/hole concentration, E is the electric field and $D_{n/p}$ is the diffusion coefficient. Φ_D are Φ_B are electrostatic potential, n_D and n_B are charge concentration where subscript 'D' and 'B' represent device and boundary. The computational domain is divided into two regions: device (channel) and boundary (source, drain and gate electrodes). K is the kernel matrix (green's function for Poisson's equation) and A, B, C and D are sub-matrices of the kernel matrix representing electrostatic interaction between grid points on channel and boundaries (within channel, channel to boundary, boundary to channel and within boundary, respectively).

$$\begin{Bmatrix} \Phi_D \\ \Phi_B \end{Bmatrix} = K(r;r')\begin{Bmatrix} n_D \\ n_B \end{Bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix}\begin{Bmatrix} n_D \\ n_B \end{Bmatrix} \tag{3.7}$$

$$\Phi_D = (A - BD^{-1}C)n_D + BD^{-1}\Phi_B \tag{3.8}$$

$$\nabla . J_{n\,(p)} = 0 \tag{3.9}$$

$$J_n = -qn\mu_n E + qD_n \frac{dn}{dx} \tag{3.10}$$

$$J_p = -qp\mu_p E - qD_p \frac{dp}{dx} \tag{3.11}$$

This approach is computationally inexpensive and obviates the need for proper boundary treatment of electrostatic potential and electric field. It requires specification of grid points only on the surfaces where charges can reside and therefore, the computation domain for electrostatics and charge transport are only the surfaces of source/drain contacts, CNTs array channel and the gate. As the boundary elements are taken as point charges, the electrostatic potential of the system diminishes as the distance increases leading to zero potential and electric field at infinity. Thus, the MoM is very useful in dealing with electrostatically open boundaries in CNT-TFTs.

The charge transport in aligned CNT-TFT here is described by current continuity and drift-diffusion equations and these equations are solved self-consistently with Poisson's equation and coupled with the thermal transport equations described in earlier section [141]. This approach allows us to study the electrostatic screening also referred to as 'cross-talk' among the CNTs in the channel region.

3.3 Modeling of Hysteresis in Aligned CNT TFTs

The governing equations for modeling of hysteresis in aligned CNT TFTs is similar to described in earlier section with the addition of specification of trap charges present either at CNT-oxide interface or within the oxide layer. The trap charge concentration is given by following equations:

$$\rho(z,x) = -qN_T(z,x)[1 - F_T(z,x)] \tag{3.12}$$

$$\rho(z,x) = qN_T(z,x)F_T(z,x) \tag{3.13}$$

$$\frac{dF_T(z,x)}{dt} = \sigma v_{th} n_H(0,x)[1 - F_T(z,x)] - \sigma v_{th} n_E(0,x)F_T(z,x) \tag{3.14}$$

Equation 3.12 and 3.13 provide the charge density at the trap sites for electrons and holes respectively. Here, N_T is defect concentration in cm^{-3} and F_T is trap filling probability. The time rate of change of F_T is given by equation 3.14, here σ is capture coefficient, v_{th} is thermal velocity of charge carriers, n_H and n_E are hole and electron concentration along the CNT [153].

3.4 Modeling of Carbon Nanotube –Liquid Crystal Composites

3.4.1 Dissipative Particle Dynamics (DPD) Method

DPD is a relatively new mesoscopic Lagrangian technique to simulate the motion of molecules which are typically represented by a set of beads. Each of these beads represents a cluster of atoms or functional groups of the molecule. Their movement is governed by Newton's law of motion. In the present study a liquid crystal ensemble,

specifically 4-cyano-4'-pentylbiphenyl, commonly known as 5-CB is simulated. The 5-CB molecule comprises of two adjacent aromatic rings with alkyl ($–C_5H_{11}$) group at one end and –CN group attached at the other end (Figure 3.1a). The aromatic rings and –CN group form the mesogen (rigid backbone of the molecule) whereas alkyl group remains flexible. In the simulations, 5-CB molecule is represented using six beads; four of which are used to mimic the rigid part of 5-CB and the alkyl group is modeled by the remaining two beads (Figure 3.1b). The numbers of beads for rigid and flexible parts have been carefully selected to produce experimentally observed values of rotational viscosity and to obtain nematic phase at room temperature. CNTs are modeled as rigid chains of beads. More details about the interaction forces and the mechanism to provide the flexibility of alkyl group and the rigidity of the mesogen are described below.

The kinetics of the DPD particles is governed by Newton's law of motion:

$$\frac{d\mathbf{r}_i}{dt} = \mathbf{v}_i, \qquad \mathrm{m}_i \frac{d\mathbf{v}_i}{dt} = \mathbf{f}_i \tag{3.15}$$

Here, $\mathbf{r}_i$, $\mathbf{v}_i$ and m_i, are the position, velocity and mass of the ith particle. The net force ($\mathbf{f}_i$) on any i^{th} particle is given as the summation of pair-wise forces namely, conservative $(\mathbf{F}_{ij}^{C})$, dissipative ($\mathbf{F}_{ij}^{D}$), random ($\mathbf{F}_{ij}^{R}$) and few additional customized terms [72]:

$$\mathbf{f}_i = \sum_{j \neq i} (\mathbf{F}_{ij}^{C} + \mathbf{F}_{ij}^{D} + \mathbf{F}_{ij}^{R} + \mathbf{F}_{ij}^{M} + \mathbf{F}_{ij}^{S} + \mathbf{F}_{ij}^{SC}) + \mathbf{F}_{i}^{ext} \tag{3.16}$$

$$\mathbf{F}_{ij}^{C} = a_{ij} w(r_{ij}) \hat{\mathbf{r}}_{ij} \tag{3.17}$$

$$\mathbf{F}_{ij}^{D} = -\gamma w^{D}(r_{ij})(\hat{\mathbf{r}}_{ij} \bullet \mathbf{v}_{ij}) \hat{\mathbf{r}}_{ij} \tag{3.18}$$

$$\mathbf{F}_{ij}^{R} = \sigma w^{R}(r_{ij})\theta_{ij}(\Delta t)^{-1/2}\hat{\mathbf{r}}_{ij} \tag{3.19}$$

where $\mathbf{r}_{ij} = \mathbf{r}_i - \mathbf{r}_j$, $\hat{\mathbf{r}}_{ij} = \mathbf{r}_{ij} / |\mathbf{r}_{ij}|$, $\mathbf{v}_{ij} = \mathbf{v}_i - \mathbf{v}_j$, t is the time step, a_{ij} is the repulsion parameter, γ is the friction coefficient, σ is noise amplitude, $w^D(r)$ and $w^R(r)$ are dimensionless weight functions for the dissipative and random processes, θ_{ij} is a delta-correlated Gaussian random variable ($\langle\theta_{ij}(t)\rangle = 0$ and $\langle\theta_{ij}(t)\theta_{kl}(t')\rangle = (\delta_{ik}\delta_{jl} + \delta_{il}\delta_{jk})\delta(t-t')$). According to the fluctuation dissipation theorem [72] $w^D(r)$, $w^R(r)$, γ, and σ follow the relation, $w^D(r) = [w^R(r)]^2$ and $\sigma^2 = 2\gamma\, k_B T$ (k_B is Boltzmann constant, T is temperature).

These conditions allow the simulation to obtain equilibrium Gibbs–Boltzmann distribution when the dissipative and noise terms are included. The weight function of the conservative force is given by,

$$w(r) = \begin{cases} 1 - r/r_c & (r \le r_c) \\ 0 & (r > r_c) \end{cases} \tag{3.20}$$

where r_c is the maximum interaction radius. The weight function for the random force $w^R(r)$ is the same function as $w(r)$.

In the DPD method, the dissipative and random forces act as heat sink and source respectively. The combined effect of these two forces acts as a thermostat. Also, the symmetric interaction between the particles ensures the conservation of momentum which leads to correct hydrodynamic behavior of the system.

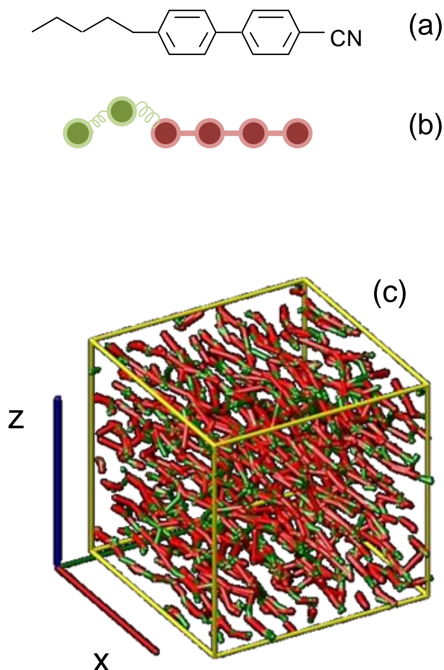

Figure 3.1(a) Schematic representation of 5-CB molecule, (b) Bead representation of 5-CB where rigid part is modeled as four locked DPD beads which move together in rigid manner and the flexible alkyl groups are modeled as two additional beads connected to one end of the rigid beads which are free to move according to a harmonic potential. (c) Simulation box for ensemble of semi-rigid chain liquid crystal molecules.

For ensemble of LCs, the DPD simulation is carried out in a cubic box ($42r_c \times 42r_c \times 42r_c$) with periodical boundaries. Particle density is chosen to be approximately $0.45r_c^{-3}$ (Figure 3.1c). The particle mass m, maximum interaction radius r_c, and k_BT were all kept unity, *i.e.*, $m = r_c = k_B\mathrm{T} = 1$. The time unit is chosen as $(mr_c^2/k_B\mathrm{T})^{1/2} = 1$ and time-step for integration is taken as $\Delta t = 0.006$. $\sigma = 3$ is chosen for the noise amplitude, and $\gamma = \sigma^2/2k_B\mathrm{T} = 4.5$ for the friction coefficient. The values of these parameters have been taken from previous studies [145, 149, 154]. The net force/torque on the rigid part of the

molecule is computed as the sum of the forces on its constituent particles. At each time-step, the coordinates and velocities of the six particles in each 5-CB molecule are updated such that the rigid part of the molecule moves and rotates as a single entity. The distance between the successive particles in the molecule is kept fixed at $1.0r_c$.

The soft potential of DPD does not prevent overlapping of beads. In order to avoid this overlap, an additional force known as Morse force is specified which is given as:

$$\mathbf{F}_{ij}^{M} = 2D_e\omega[e^{2\omega(2r_s-r_{ij})} - e^{\omega(2r_s-r_{ij})}]\hat{\mathbf{r}}_{ij} \tag{3.21}$$

This force acts between each pair of DPD beads when the distance between them r_{ij} is less than $2.0r_s$ [155]. For 5CB beads, $r_s = 0.2$, $D_e = 200$, $\omega = 0.5$ and cut off radius = 3 where for interaction between CNT and 5-CB, $r_s = 1$, $D_e = 400$, $\omega = 0.5$ and cut off radius = 3.

In order to specify the bond stretching and the flexibility of alkyl part of the molecule the following harmonic force is specified between the consecutive beads of non-rigid part of the 5-CB DPD chain:

$$\mathbf{F}_{ij}^{S} = k_{bond}(1-\frac{r_{ij}}{r_0})\hat{\mathbf{r}}_{ij} \tag{3.22}$$

Here $r_o = 0.6$ and $k_{bond} = 100$. [155]

The dipole moment plays an important role for the molecular reorientation of LC molecule when external electric field is applied. In the simulations, two equal and opposite charges at the two ends of the DPD chain are specified such that product of

charge and distance between them matches with the experimental value of dipole moment of 5-CB (6.3 Debye). The charges calculated in DPD units are +/- 0.6 based on the actual length of the 5-CB molecule (~20 Angstrom). In CNT-LC ensemble simulations, CNT length is considered to be 5 times the length of 5-CB molecule and dipole moment 50 times greater than 5-CB molecules.

The electrostatic interactions due to the charges are specified by the following screened Coulombic relation:

$$\mathbf{F}_{ij}^{SC} = \frac{q_i q_j \exp(-k r_{ij})}{r_{ij}} \left(\frac{1}{r_{ij}} + k\right) \hat{\mathbf{r}}_{ij} \tag{3.23}$$

Here, q_i and q_j are the charges on any two charged particles i and j. The inverse Debye length (k) to this interaction is 0.24 [155].

Finally, the force due to the external electric field is given by following expression:

$$\mathbf{F}_{i}^{ext} = q_i E_{ext} \tag{3.24}$$

Here q_i is charge on i^{th} charged particle and E_{ext} is the electric field.

The DPD simulations have been carried out using open source molecular dynamics code LAMMPS [156].

3.5 Closure

Electro-thermal modeling of CNT network/array TFTs is based on Poisson's equation, drift-diffusion equation and Fourier's law. Poisson's equation is solved using finite difference method and method of moments approach for network and arrays,

respectively for computational efficiency. The model provides current, potential and temperature distribution inside the device as a function of device parameters which can be varied to study their exclusive effects on device performance. Dissipative Particle Dynamics method is used to study the dynamics of liquid crystal-CNT composites under AC and DC electric fields.

CHAPTER 4: ROLE OF CONTACT RESISTANCE AND JUNCTION TOPOLOGY IN HIGH FIELD BREAKDOWN OF CN-TFT

This chapter presents an analysis on power dissipation and network breakdown in CN-TFTs (schematic shown in Figure 1). The results are obtained using an electro-thermal model of the CNT network, molecular dynamics simulations of the junctions, and experimental measurement of power dissipation and temperature. Comparison of the measured CN-TFT power vs. source-to-drain voltage (P-V_{SD}) and temperature profiles with the corresponding numerical results (Figure 2) allows us to extract thermal boundary conductances (TBCs) at both CNT junctions and CNT-substrate interface simultaneously. Both TBCs are varied in a wide range in order to explore their relative impact on network breakdown behavior and to find optimum range of these parameters to achieve greater heat dissipation. The effects of network morphology parameters such as network density and junction topology on network breakdown are investigated. The model provides useful insights about the role of the TBCs in power dissipation and electrical breakdown of CN-TFT devices.

4.1 Modeling Parameters and Experimental Conditions

The computational domain of the CN-TFT (Figure 4.1) has been selected based on the experimental devices [34]. Experiments were conducted in the collaboration with Prof. Eric Pop's group at University of Illinois at Urbana Champaign. The details of the device fabrication and CNT-network morphology can be found in the previous studies

[34, 54]. Briefly, the CNT network is grown by chemical vapor deposition on SiO_2 (t_{ox} = 90 nm) supported by a highly n-doped Si substrate (t_{Si} = 500 µm). The device is patterned by photolithography, and the contacts (Ti/Pd = 1/40 nm) are deposited by electron beam evaporation. The Si substrate acts as a back-gate and the gate-to-source voltage is set (V_{GS} ≤ -15 V) such that both metallic and semiconducting tubes in the network are in the "On" state while V_{SD} is increased until network breakdown. Infrared (IR) thermal imaging of the device is performed with the bottom of Si substrate kept at a constant T_0 = 70 ^{o}C and the top surface is exposed to air to facilitate IR imaging and electrical breakdown due to oxidation. The CNT diameter distribution is obtained by atomic force microscopy (AFM), with an average diameter ~2 nm [46, 157].

Carbon nanotubes synthesized by arc discharge method are used as starting materials for all the samples. The diluted solution containing SWCNTs and surfactant is vacuum filtered through a mixed cellulose ester membrane to form CNT network. After the filtration through the membrane the films are washed with copious amount of water to remove residual surfactants. The network is then transferred to supporting substrates of SiO_2 (t_{ox} = 300 nm) on highly n-doped Si wafers (t_{Si} = 500 µm) with predefined electrical contacts and then the filter is dissolved [56]. After the film transfer to the substrate, it is soaked in acetone overnight to remove residual cellulose and is further cleaned by annealing at 230 °C for 1 h in ambient. The device channels are patterned by photolithography and/or electron beam lithography (for submicron width dimensions).

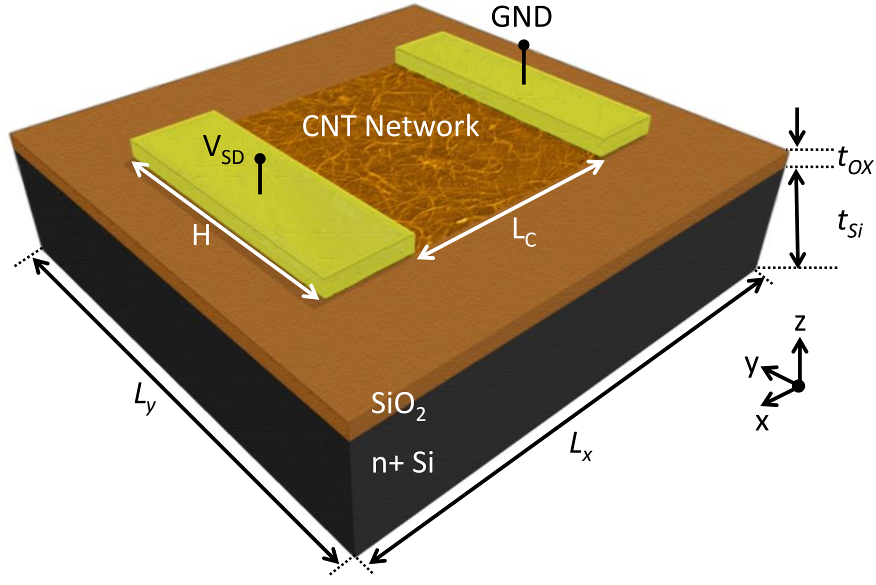

Figure 4.1 Schematic/Computational domain of a carbon nanotube network thin-film transistor (CN-TFT) device. L_x = 500 μm, L_y = 500 μm, L_C = 10 μm, H = 50 μm, t_{Si} = 500 μm, t_{OX} = 90 nm.

Under high field conditions, Joule heating leads to oxidation of the CNTs in air if the temperature exceeds the breakdown temperature $T_{BD} \approx 600$ °C, resulting in the breakdown of the devices [34, 35, 158]. Thus, during this electrical breakdown process, the power dissipation in the device reaches a maximum value near T_{BD}, and then drops quickly to zero as the current paths within the network reform and oxidize CNTs, reaching catastrophic device failure. Back-gated device configuration has been selected for the experiments as it facilitates experimental measurements [34, 56]. All simulation results presented in this work are averaged over a large number of devices ($n \approx 100$) unless specified otherwise. Both mean as well as standard deviation of the breakdown

characteristics are presented to understand the variability in the breakdown behavior for different device geometry and network morphology parameters.

The important dimensional parameters of the CN-TFT are channel length (L_c), channel width (H), average tube length (L_t) and CNT diameter (d) of 10 µm, 50 µm, 4 µm and 2 nm, respectively (Figure 4.1). In real applications, CNT-TFTs can be top-gated and the substrates may be plastics or glass, which may lead to different CNT-substrate TBC and junction morphology. The present analysis considers a range of TBCs which will include the possible TBC values at CNT junctions with different substrates. The device geometry, conductive properties of the substrate and boundary conditions can be easily modified in the present model to consider the different applications of CN-TFTs.

The structure of CNT junctions in a CNT network can significantly affect the thermal transport between CNTs and between a CNT and the supporting substrate. Molecular dynamics (MD) simulations are used to identify the junction structure and estimate the length (L_B) of the buckled segment of the top CNT which is not in direct contact with the SiO_2 substrate (Figure 4.2). The adaptive intermolecular reactive empirical bond order potential (AIREBO) is used to describe C-C interactions in CNTs [159], the Munetoh parameterization of the Tersoff potential to describe the Si-Si, O-O, and Si-O interactions [160], and the Lennard-Jones potential to model the van der Waals interaction between CNT and SiO_2 atoms at the interface [43, 161]. The CNT-SiO_2 system is equilibrated using the canonical ensemble at 375 K for 300 ps, and then sample the positions of each atom for 50 ps. In order to anchor the top CNT with the SiO_2 substrate, a very small force (0.02 Nm^{-1}) towards the substrate is applied on the top CNT during the first 100 ps simulation in NVT (constant volume and temperature ensemble)

and then this force is removed. L_B ~ 30 nm is noted in the final structure (Figure 4.2). In most of the following electro-thermal transport analysis of the CN-TFT network, it is considered that a 30 nm section of all top CNTs at the location of their junctions with other CNTs is not exchanging heat with the substrate directly (i.e., $Bi_S = 0$ is considered for top CNT at the junction for length L_B).

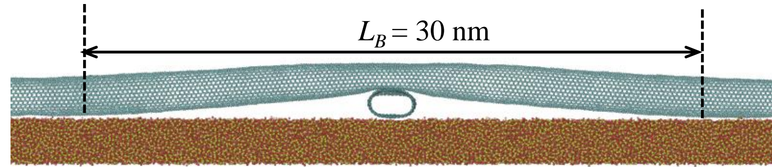

Figure 4.2 Equilibrated structure of the junction between two CNTs supported on SiO_2 substrate, obtained from molecular dynamics (MD) simulations. Using CNT diameter d = 2 nm it is found that L_B ~ 30 nm, which is the approximate length over which the top CNT loses thermal contact with the substrate.

4.1 Model Validation and Estimation of Interfacial Conductances

In order to establish the validity of the computational model, numerical results have been compared with the experimental data. The simulation results are found to be in close agreement with experiments for both power (current) and temperature (Figure 4.3) at $g = 0.16$ $Wm^{-1}K^{-1}$ ($Bi_S = 2 \times 10^{-4}$) and $G_C = 2.4$ pWK^{-1} ($Bi_C = 10^{-7}$). These values of thermal boundary conductances (TBCs) are very close to the typically observed experimental and theoretical values in the literature [34, 42, 43, 46, 48, 162]. Both g and G_C are found simultaneously by comparing the numerically estimated power dissipation and temperature profile in CN-TFTs against the experimental measurements. The power dissipation and thereby the temperature within the CNT network increases with increasing V_{SD} such that it eventually reaches the breakdown temperature of CNTs in air [46, 158] (~600 ^oC). Some CNTs in the channel are likely to have higher current and

power dissipation compared to the rest in the network, and therefore they experience earlier burnout due to excessive self-heating. As a result, percolation pathways change dynamically in the network as V_{SD} is increased further. This burnout process eventually results in a complete breakdown of the network along a random pattern between source and drain (Figure 4.3a). In simulations, the temperature profile of the CNT network is calculated at each voltage step. Those CNTs whose temperature exceeds 600 C, are removed from the network and current and temperature profile is calculated again for the remaining percolating network. This process is repeated at each voltage step. The numerical simulations explain the experimental observations [34] of the breakdown process well. 50 random networks are considered to obtain the statistical average results of current, power (dashed lines in Figure 4.3b) and temperature distribution in a CN-TFT. The statistical averaged numerical results are in good agreement with the experimental measurement of power dissipation with increasing V_{SD} (Figure 4.3b) and the temperature profile at the SiO_2-Si interface obtained from infrared microscopy[34] (Figure 4.3c and 4.3d).

The experimental results based on IR measurements [34] revealed that the average temperature (~105 ^{o}C) in the channel region of CN-TFT near breakdown, was well below the breakdown temperature [158] (~600 ^{o}C in air) of CNTs. Hand calculations [34] suggest that such a limited increase in temperature in the channel region could be attributed to highly localized nanometer-scale hot-spots at the CNT junctions, which cannot be captured by the IR microscopy with a resolution of ~2 μm.

Detailed simulations are performed to investigate the role of both CNT junction and CNT-substrate thermal conductances in the breakdown behavior and next, the effects of network density and junction topology on the network breakdown are explored.

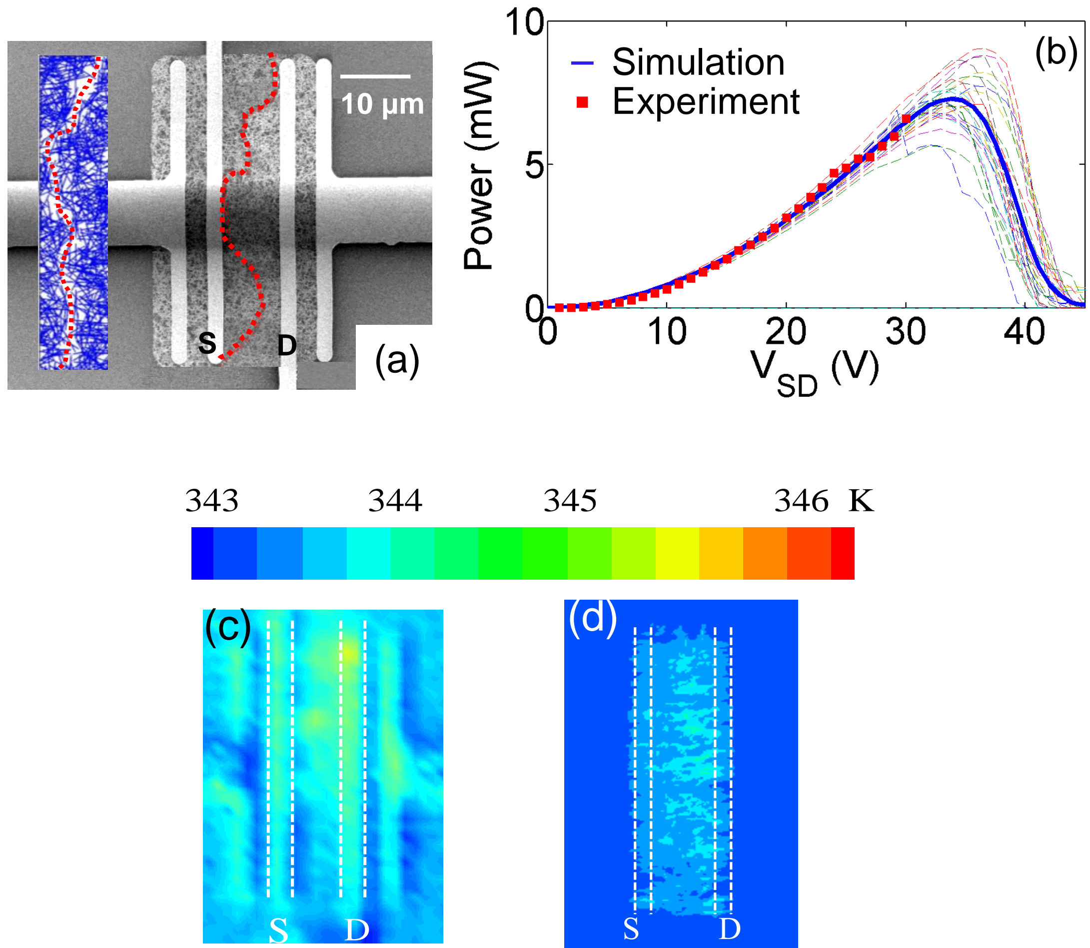

Figure 4.3(a) Comparison of random CNT network from simulations (left inset, channel region) to scanning electron microscopy (SEM) image of the CN-TFT used in experiments after the breakdown, respectively. The red dotted line shows the breakdown pattern of the network. (b) Comparison of computational results to experimental measurements of dissipated power vs. source-drain voltage (V_{SD}); the dark blue curve shows the statistical average of 50 random networks (dashed curves) obtained from the simulations. The power dissipation first increases with V_{SD}, then eventually drops to zero due to burning of CNTs which lead to complete network breakdown. (c-d) Temperature profile at the SiO_2-Si interface obtained from infrared microscopy [34] and numerical simulation respectively for the device shown in (a).

4.2 Role of CNT-Substrate and CNT-CNT Interfacial Thermal Conductance

CNT synthesis and TFT fabrication process can lead to variations of interfacial properties of CNTs such as thermal boundary conductances corresponding to CNT junctions and CNT-substrate interfaces. In order to analyze the impact of varied TBCs on power dissipation and device breakdown, simulations are carried out. Simulations reveal a very interesting feature about the role of junctions in heat dissipation which also supports the experimental observations. Results suggest that the typical junction TBC ($Bi_C = 10^{-7}$) is extremely low and a further decrease in Bi_C does not lead to any change in power and temperature distribution in the network. In other words, it is found that for the typical value of the TBC at CNT junctions, the CNTs can be considered to be thermally non-interacting at their junctions. This particular result is consistent with the assumption that percolative thermal conduction in the network is typically absent [163-165]. Moreover, simulation results clearly show that even if the junction conductance is improved by two orders of magnitude ($Bi_C = 10^{-5}$, which may be practically improbable), it does not change the breakdown behavior of the CNT network significantly (Figure 4.4a). This extremely weak dependence of breakdown behavior on Bi_C can be attributed to very small junction area and the weak nature of thermal interaction at crossed CNT junctions.

Next, the effect of CNT-substrate thermal coupling (non-dimensional parameter Bi_S) on the power dissipation and the breakdown behavior of CN-TFTs is examined. In order to study this dependence, the breakdown behavior of the network is analyzed for Bi_C in the range of 10^{-7} - 10^{-3} at different Bi_S values (10^{-6} - 10^{-3}). The range selected here represents very poor to very good thermal contacts at CNT interfaces. The breakdown

voltage increases significantly when Bi_S is increased (Figure 4.4a). The Figure 4.4a inset shows the power variation in CN-TFT with V_{SD} at low Bi_S (~10^{-6}) and results suggest that the device fails before 10 V for all values of Bi_C in the range specified above. On the other hand, device reaches peak power dissipation at V_{SD} > 24V at Bi_S (~10^{-4}). It can be noted here that simply one order of magnitude increase in Bi_S can bring more positive impact on breakdown behavior than four orders of magnitude increase in Bi_C. These results clearly indicate that CNT junction TBC (Bi_C) plays only a secondary role to CNT-substrate TBC (Bi_S). Thus, the key to enhance the power density capability and device reliability lies in the improvement of CNT-substrate TBC. The two important characteristics of network breakdown, peak power (PP) and V_{SD} at peak power, both strongly depend on Bi_S and follow a power law relation with respect to Bi_S (Figure 4.4b).

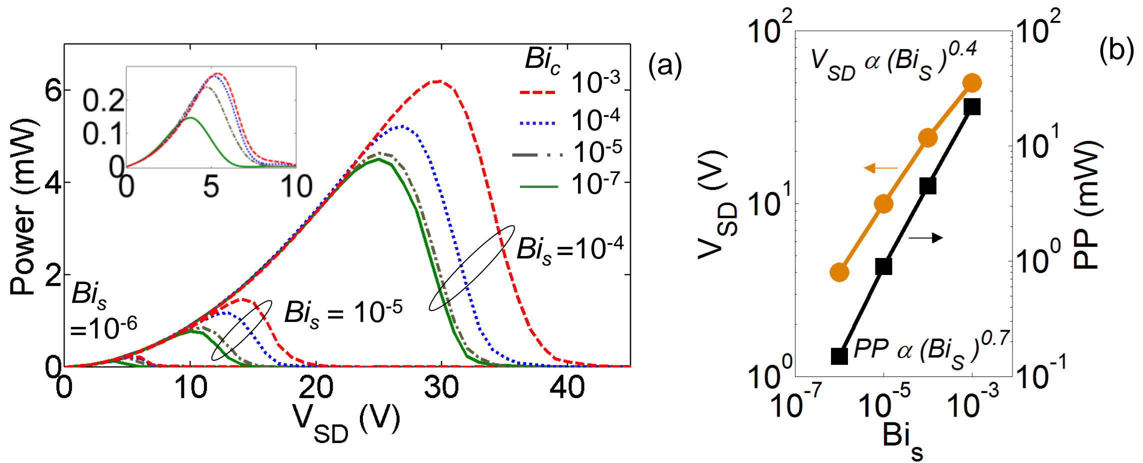

Figure 4.4 (a) Variation of power dissipation in the CN-TFT vs. V_{SD} for different values of normalized thermal conductance at CNT junctions (Bi_C) and CNT-substrate interface (Bi_S); inset plot shows power vs. V_{SD} at Bi_S = 10^{-6} for different values of Bi_C = 10^{-7} to 10^{-3}. (b) Variation of peak power (PP, right axis) and VSD (left axis) corresponding to peak power vs. Bi_S at Bi_C = 10^{-7}.

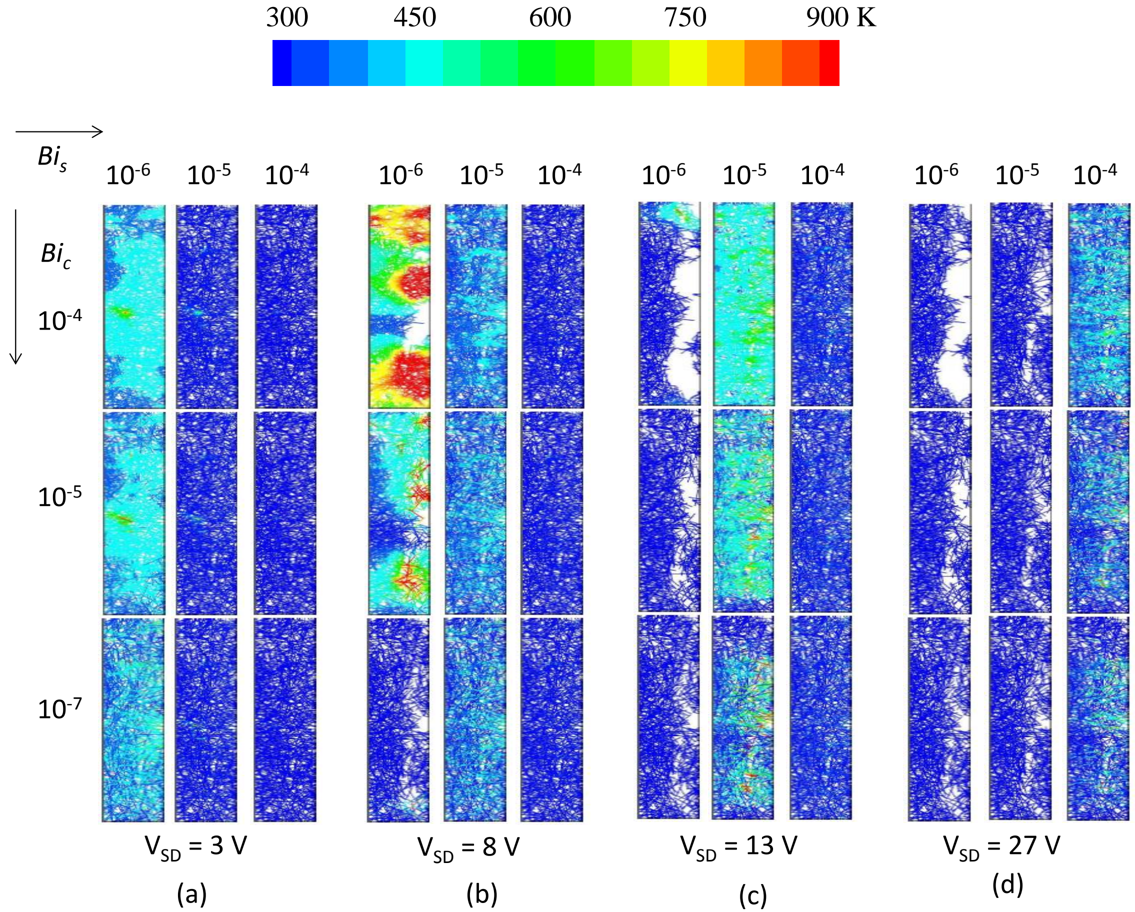

Figure 4.5 Temperature profile in CNT networks for different values of Bi_C and Bi_S at (a) V_{SD} = 3 V, (b) V_{SD} = 8 V, (c) V_{SD} = 13 V, (d) V_{SD} = 27 V. Network density ρ = 3.5 CNTs/μm^2. In each case the current flows from left to right (source to drain) of the panels, respectively.

The thermal profiles in a CNT network for different values of Bi_S and Bi_C at four different voltages (V_{SD}) are shown in Figure 4.5. It should be noted that the CNTs at high temperature are better able to transfer heat to other CNTs in the network at high Bi_C (~10^{-4}). This leads to more uniform spreading of heat across the network, which in turn lowers the peak and average temperature of the network. At the same time, in case of low Bi_S (~10^{-6}), the thermal interaction of CNTs with the substrate is very weak and the

temperature rises steeply with V_{SD} across the network. Subsequently, the temperature of a large cluster of CNTs in the network reaches the breakdown temperature simultaneously leading to big holes in the network (see left-top in Figure 4.5b-d). In case of low Bi_S (~10^{-6}) and lower Bi_C (<10^{-4}), the network breaks down at V_{SD} < 10V along a curvy and random line because only fewer CNTs which form crucial percolative pathways burn due to excessive self-heating as they are not able to spread dissipated power to other CNTs or to substrate. On the other hand, if CNT-substrate TBC is higher ($Bi_S \geq 10^{-5}$), the average temperature of the network is lowered due to increased heat dissipation across the CNT-SiO_2 interface. This also translates into lower temperature at the junctions because heat can efficiently flow along the CNT-axis and then into the substrate at the locations where the CNT is in direct contact with the substrate. As a result, breakdown occurs at higher V_{SD} (>15V) along a curvy and random breakdown pattern (see middle column in Figure 4.5d).

4.3 Effect of Variation in Network Density

As noted in the previous section, the TBC at CNT junction may not have a large impact on CN-TFT device reliability for the typical value of CNT-substrate TBC observed in the experiments and discussed here, but these junctions are extremely important for charge transport across the channel. As the network density increases, the number of junctions and the percolation pathways for the electrical transport in the network also increases. This suggests that the network density directly affects the current and power dissipation in the channel and the breakdown of network depends on the density. To analyze the impact of density variation on the breakdown process, the

developed model is used to consider four different densities (ρ) for the same device geometry/configuration. TBCs are kept constant ($Bi_C = 10^{-7}$, $Bi_S = 10^{-4}$).

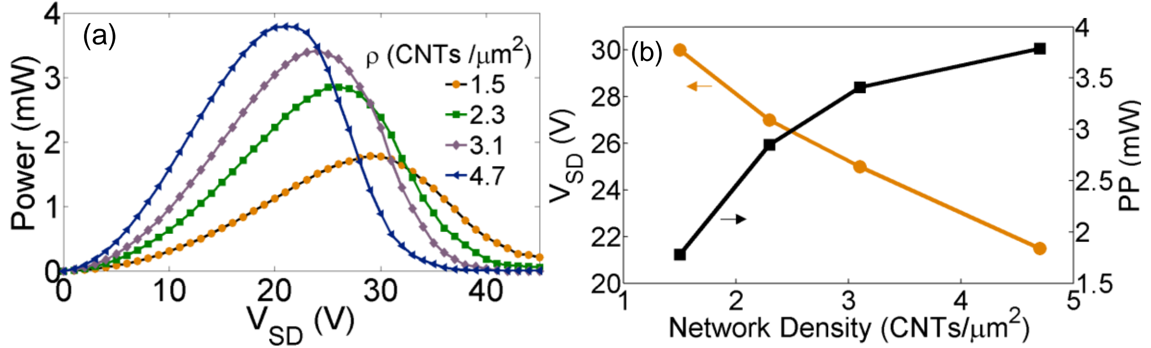

Figure 4.6 (a) Power variation with V_{SD} for different network densities, until complete network breakdown is reached. Statistical average of 50 random networks has been considered for each density. (b) Peak power (*PP*, right axis) and V_{SD} (left axis) corresponding to peak power vs. network density.

The results indicate that higher network density leads to higher power density in the network and consequently the breakdown occurs at lower V_{SD} (Figure 4.6a). For ρ = 1.5 CNTs/μm², power reaches a maximum of 1.7 mW at 30 V. For ρ = 2.3, 3.1 and 4.7 CNTs/μm², peak power *PP* = 2.8 mW, 3.4 mW and 3.75 mW and corresponding V_{SD} = 27, 25, and 21 V. Figure 4.6b shows that there is a clear trade-off between higher current and lower breakdown voltage with increasing network density. An optimum density of network should be chosen to get sufficiently high current without the possibility of early breakdown under high bias operation.

4.4 Impact of CNT buckling at Junctions

Some studies have shown that the fabrication process of CNT networks can affect the CNT network morphology, which will in turn influence the CN-TFT performance. For example, Timmermans *et al*.[54] show changes in the CNT network alignment and CNT junction area, for similar network densities, would significantly affect the mobility, On/Off ratio, and 1/f noise in CN-TFTs. Other studies have shown how the network conductivity can be tuned by controlling the network density and metallic-to-semiconducting CNT ratio.[166, 167] Our model provides new insight into how network morphology influences device reliability by carefully considering the buckling length L_B (Figure 4.2), which can vary with network density due to increased CNT junction density. For some CNTs, the distance between two junctions along a CNT may be $< L_B = 30$ nm as the network density increases. Consequently, at high densities, a large section of a single CNT within the network may not make direct contact with the substrate and is instead supported only by other CNTs. The non-contacting length of the top CNT depends on the diameter of top and bottom CNTs in addition to the distance between junctions, and layout of lower CNTs.

Results from MD simulations of a system shown in Figure 4.7a reveal that the total length of the buckled structure of top CNT is 63 nm when two CNT junctions are separated by 25 nm. The non-contacting length increases with increasing CNT diameter. The large diameter CNTs flatten due to a stronger vdW interaction with the surface [46] which will also have significant effect on the junction structure and non-contacting length. These sections of CNTs are likely locations of hot spots in the network which will strongly affect the breakdown characteristics.

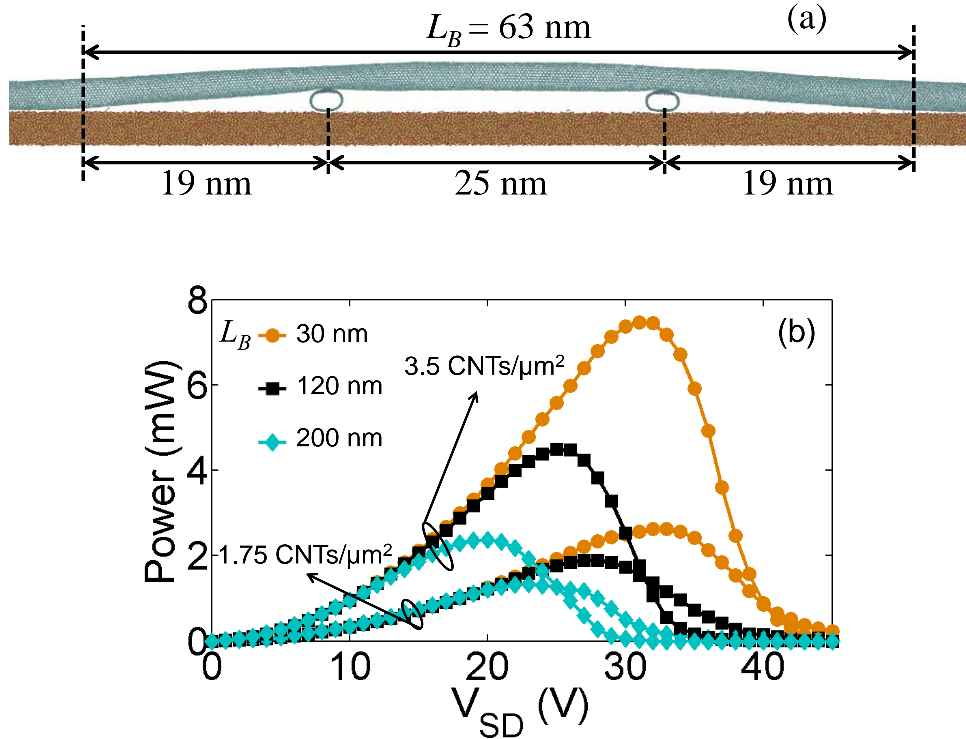

Figure 4.7 (a) MD simulation result of a top CNT supported by two bottom CNTs spaced by 25 nm, leading to an apparently buckled structure of length $L_B \sim$ 63 nm; CNT diameter = 2 nm, (b) Power vs. V_{SD} for two different network densities and different buckling lengths (L_B) at the junction for TBCs $Bi_C = 10^{-7}$ and $Bi_S = 2\text{x}10^{-4}$. The effect of increased buckling length is larger for higher density.

The effect of non-contacting length at CNT junctions are explored by considering two network densities, ρ = 1.75 CNTs/µm^2 and 3.5 CNTs/µm^2, and three cases of buckling length: L_B = 30 nm, 120 nm and 200 nm. The average length of the CNTs in the network is L_t = 4 µm. The peak power dissipation in the network decreases by 50% and 70% corresponding to ρ = 1.75 and 3.5 CNTs/µm^2, respectively (Figure 4.7b), when the length of buckled sections is increased from L_B = 30 nm to 200 nm. V_{SD} corresponding to the peak power decreases by more than 33% when L_B is increased from 30 nm to 200 nm for both densities. The temperature of 10% of junctions increases by more than 150 ^{o}C at

V_{SD} = 15 V as L_B increases from 30 nm to 200 nm for ρ = 1.75 CNTs/µm^2 (see Supplement). The effect of L_B is even greater for denser networks, as for ρ = 3.5 CNTs/µm^2 the temperature of at least 10% of junctions increases by more than 300 ^{o}C at the same V_{SD} = 15 V as L_B increases from 30 nm to 200 nm. This behavior is expected since a larger fraction of CNTs remain buckled due to the increased number of junctions per CNT. This result suggests that the network density ρ could be appropriately selected such that the distance between the junctions on a CNT is higher than the typical value of L_B to avoid early breakdown and enhanced reliability.

4.5 Closure

In summary, power dissipation and network breakdown behavior in CN-TFTs are examined using computational approach. Model is validated with experiments. It is noted that the breakdown characteristics remain invariant even if the TBC at junctions increases by two orders of magnitude from its typical value (~ 2.4 pWK^{-1}). It is also found that one order of magnitude increase in the CNT-substrate TBC from its typical value (~ 0.16 Wm^{-1}K^{-1}) will double the breakdown voltage and quadruple maximum power density capability of network. This analysis provides a useful insight into the role of CNT junctions in power dissipation. It implies that the CNT junctions are the likely locations of the hot spots not because of poor CNT-CNT thermal conductance but rather due to the absence of direct contact of buckled part of CNTs with the substrate at crossed CNT junctions. The denser network may adversely affect the device reliability as the higher percentage of CNTs may not be in direct contact with the substrate. Our analysis suggests

that the CN-TFT performance can be greatly improved by engineering the CNT-substrate interactions and optimizing the network morphology.

CHAPTER 5: ROLE OF CHANNEL DIMENSIONS AND CNT NETWORK MORPHOLOGY IN HEAT DISSIPATION AND THERMAL RELIABILITY

In this chapter, the breakdown characteristics such as peak power (or breakdown power, P_{BD}) and the corresponding source-to-drain voltage referred to as the breakdown voltage (V_{BD}) of CN-TFTs (Figure 5.1) are studied to find their relation with the channel geometry and network morphology. The breakdown characteristics and their standard deviations are analyzed for smaller and larger channel width (W_C) at various channel lengths (L_C) for random networks with constant CNT length, L_t. Next, the alignment of CNTs is systematically varied in the network for a given L_C, W_C and L_t to study the effect of network alignment on the breakdown behavior. Subsequently, a general case is considered employing different log-normal distributions of L_t in conjunction with several alignment distributions for a given L_C and W_C. The analysis presented here, provides new insight into optimizing the device parameters in order to engineer thermal reliability and uniformity in CN-TFT performance characteristics.

5.1 Channel Length and Width Dependence

As mentioned earlier, breakdown behavior and thermal reliability of CN-TFTs is dependent on channel dimensions. In order to quantify and understand the breakdown behavior as a function of channel dimensions, the effect of L_C and W_C on the breakdown characteristics have been examined here. From the perspective of the device breakdown, the two important metrics are P_{BD} and V_{BD}.

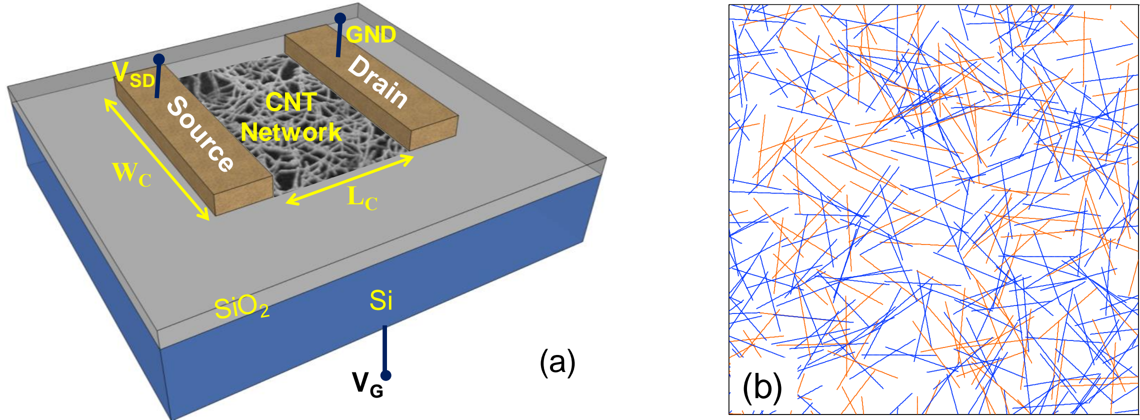

Figure 5.1 Schematic of (a) back-gated CN-TFT device with channel length (Lc) and channel width (W_C) similar to the devices experimentally tested. (b) A sample of simulated random network of CNTs; blue color is used for semiconducting and red for metallic CNTs.

Figure 5.2(a) shows the power dissipation in the device as a function of V_{SD} for three different cases of L_C = 5, 10, 15 μm at a network density of ρ = 15 CNTs/μm^2, W_C = 100 μm, and L_t = 2 μm. A very close agreement of the simulation results with the experiments has been found. It should be noted here that the simulation curves shown in Figure 5.2(a) have been specifically selected out of 100 sample simulations. CN-TFTs with smaller L_C show lesser electrical resistance which in turn leads to higher current (*i.e.*, higher power dissipation) at a given V_{SD} [20, 53]. This causes the device of smaller L_C to break earlier (*i.e.*, at a lower V_{SD}). It is noted that both V_{BD} and P_{BD} linearly scale with L_C [Figure 5.2(b) and 5.2(c)]. The error bars in these figures indicate the variation in breakdown characteristic of the random networks. The size of the error bar represents a 95 percent confidence interval for V_{BD} (or P_{BD}). The experimental values for both V_{BD} and P_{BD} fall well within the range of error bars estimated from the simulations. For a given network density, the number of percolating pathways decreases as L_C increases. As

previously reported, [53] ON current shows greater variations when network density is decreased. Lowering the density is equivalent to reducing the number of percolating pathways, which also occurs when L_C is increased, and therefore the error bars increase as L_C increases. These results suggest that the variability in the breakdown for a given device geometry and network density can be substantial and require due consideration while predicting the device reliability [56].

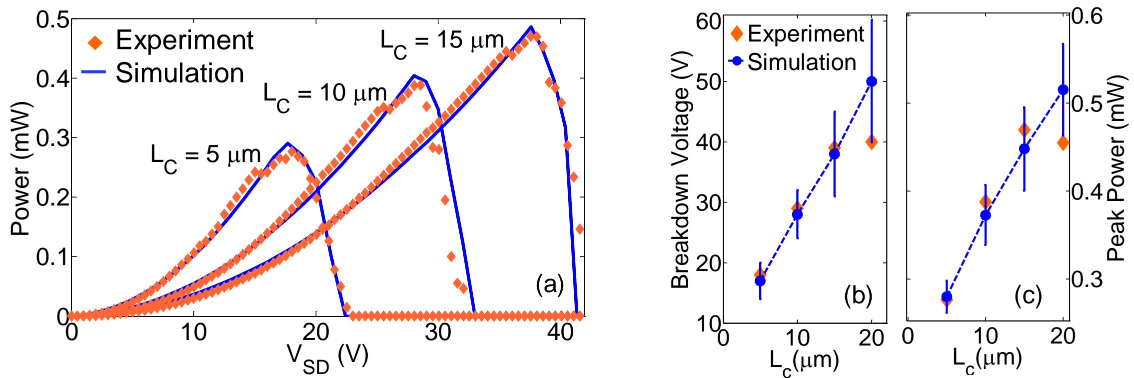

Figure 5.2 (a) Measured and simulated power dissipation in a CNT network versus source-to-drain voltage (V_{SD}) for three different channel lengths (L_C = 5, 10, 15 µm). Simulation results are presented for individual devices here. For a given L_C, power reaches a peak value and then drops quickly to zero as the CNT network breaks down due to the excessive Joule heating and CNT oxidation in air. The value of V_{SD} corresponding to the peak power (P_{BD}) is referred to as the breakdown voltage, V_{BD}. (b) V_{BD} versus L_C, and (c) P_{BD} versus L_C. The error bar represents a 95 percent confidence interval. The device is in the ON state at gate voltage V_{GS} = -40V. Device width W_C = 100 µm; CNT length L_t = 2 µm, network density ρ = 15 CNTs/µm^2. (b) and (c) contain simulation results which are averaged over 100 devices.

Figure 5.3(a) shows the breakdown behavior of CN-TFTs for W_C = 4, 10, 20, 30, and 40 µm at L_C = 10 µm, L_t = 2 µm and ρ = 15 CNTs/µm^2. The curves in Figure 5.3(a) resemble a 'bell' shape due to the statistical averaging. It can be observed that the V_{BD} does not change with W_C. Further, it is found that P_{BD} to be directly proportional to width

when $W_C/L_t > 2$ [Figure 5.3(b)]. It is also noted that the normalized standard deviation (σ_{norm}) of V_{BD} [Figure 5.3(c)] and P_{BD} [Figure 5.3(d)] increases when L_C is increased or W_C is decreased. For $W_C/L_t \leq 2$, relatively large σ_{norm} is observed due to significant incremental change in the number of percolating pathways [168]. It is noted that for ρ = 15 CNTs/μm^2, L_C = 10 μm and $W_C/L_t = 2$, less than 30% of the random networks out of 100 samples have a percolating path between source and drain. The probability of forming a percolating path further decreases as L_C is increased for $W_C/L_t \leq 2$. Therefore, a denser network is employed to study the breakdown behavior for $W_C/L_t \leq 2$.

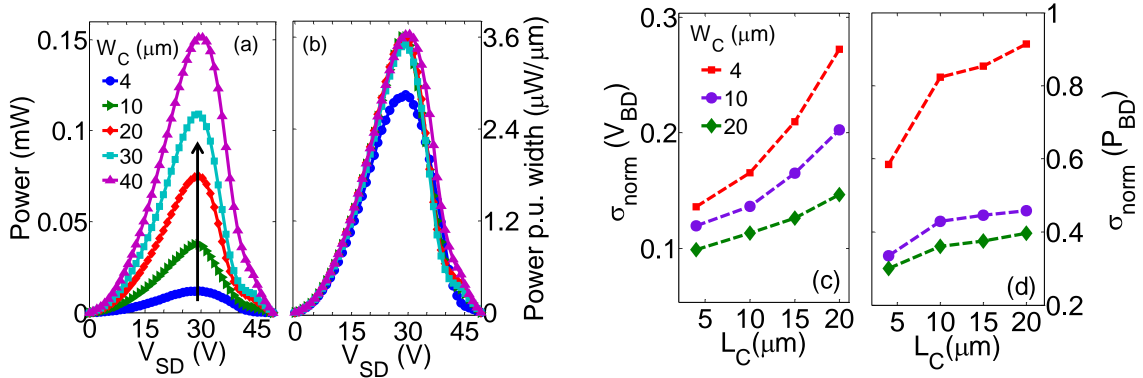

Figure 5.3 Numerical results for (a) power vs. V_{SD} (arrow indicates the increasing channel width), (b) power per unit width vs. V_{SD} for several channel widths (W_C = 4, 10, 20, 30, 40 μm); channel length, L_C = 10 μm, and network density, ρ = 30 CNTs/μm^2. Note that power per unit width becomes invariant with respect to W_C for sufficiently high W_C. (c) σ_{norm} of breakdown voltage (V_{BD}) vs. L_C, and (d) σ_{norm} of peak power (P_{BD}) vs. L_C. Here σ_{norm} = standard deviation / mean.

Figure 5.4 shows the dependence of breakdown behavior on L_C for narrow width devices (W_C/L_t = 0.75, 1, 1.5, 2) at ρ = 30 CNTs/μm^2. It is found that V_{BD} is nearly invariant of the W_C for $W_C/L_t \geq 1$ [Figure 5.4(a)]. P_{BD} follows width-dependent scaling

with L_C such that higher width leads to greater change in P_{BD} per unit change in L_C [Figure 5.4(b)]. A similar trend is observed in the experiments. It is noted that σ_{norm} of V_{BD} [Figure 5.4(c)] and P_{BD} [Figure 5.4(d)] remain nearly invariant of L_C for $W_C/L_t \geq 1$ and σ_{norm} decreases as W_C increases at a given L_C. Overall, it is noted that larger values of L_C and W_C correspond to better device reliability as they lead to larger V_{BD}, greater P_{BD}, and better uniformity in device characteristics.

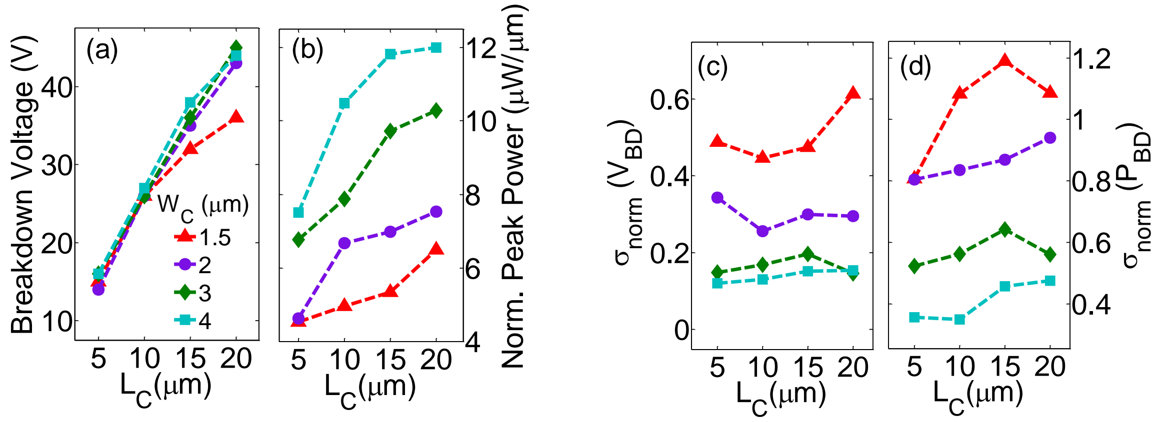

Figure 5.4 Numerical results for (a) breakdown voltage (V_{BD}) and (b) normalized peak power (with respect to W_C) in the CNT network vs. channel length (L_C) for smaller channel widths (W_C). (c) σ_{norm} of V_{BD}, (d) Peak power (PP) vs. L_C. Here, network density $\rho = 30$ CNTs/μm^2.

Previous studies [34-36, 56] on the CN-TFT breakdown show that the network breaks along a zigzag pattern across the channel when W_C is much greater than L_t. In the current study, this breakdown pattern is examined in CN-TFTs when W_C is comparable to L_t. Scanning electron microscopy (SEM) images from the experiments show that the breakdown pattern remains zigzag when L_C is small (few microns) for different values of

W_C, as shown in Figure 5.5 (a, d, g). Also, the length (L_{BD}) of the breakdown gap region [shown in Figure 5.5(g)] is observed to be less than the average L_t which indicates a highly localized burning of CNTs. Further, L_{BD} increases as L_C is increased for a given W_C but does not change much with respect to W_C for a given L_C (Figure 5.5). This trend underlines the role of temperature profile before the breakdown and electrostatic effects of the broken CNTs during the breakdown process.

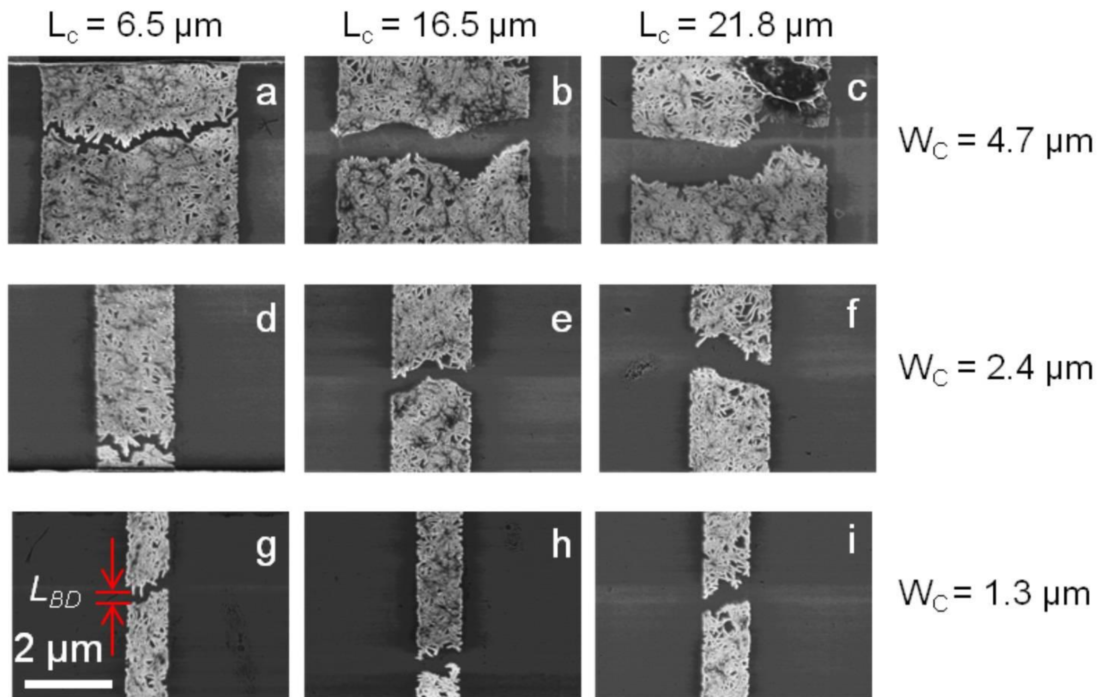

Figure 5.5 Scanning electron microscopy (SEM) images of CN-TFTs after complete breakdown for different channel lengths (L_C = 6.5 μm, 16.5 μm, 21.8 μm) and widths (W_C = 1.3 μm, 2.4 μm, 4.7 μm). The breakdown gap length (L_{BD}) in the CN-TFT increases as the L_C is increased; however L_{BD} does not show much variation when the width is changed.

For devices with larger L_C, the temperature profile is more flat away from the contacts, which leads to larger L_{BD}. In addition, higher electrostatic effect from the

broken tubes amounts to greater induced electric field in the unbroken neighboring CNTs. This electrostatic effect is proportional to the applied voltage between source and drain at the breakdown (*i.e.,* V_{BD}) [36]. As V_{BD} linearly increases with L_C, the breakdown gap also follows nearly the same trend.

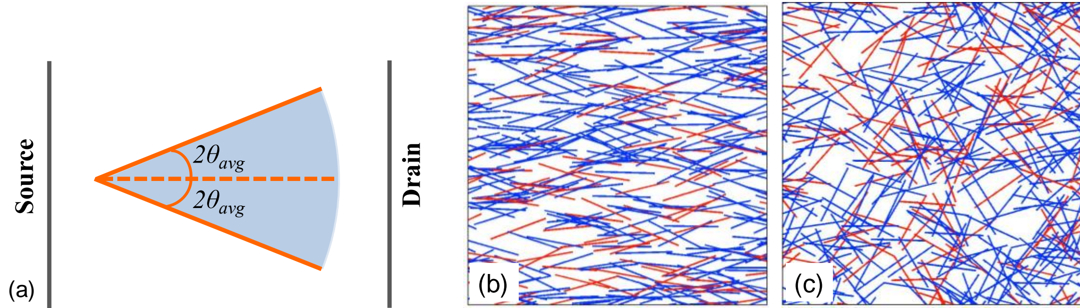

Figure 5.6 (a) The schematic illustrates the alignment of a CNT. The average alignment (θ_{avg}) of the CNT network is defined such that for a specific value of θ_{avg}, a CNT in the network is allowed to make any angle between -2θ_{avg}avg and 2θ_{avg} with equal probability. Hence, by this definition, θ_{avg} = 45° corresponds to a random network, and θ_{avg} = 0° means perfectly aligned CNTs. An example of heterogeneous CNT network with (b) θ_{avg} = 13°; (c) θ_{avg} = 36°. Metallic (M) CNTs in brown, semiconducting (S) CNTs in blue; M:S network density ratio is 1:2.

5.2 Network Morphology

5.2.1 Variable Alignment Angle with Constant CNT Length

In order to investigate the effects of network morphology in terms of CNT alignment on breakdown behavior, several alignment distributions of CNTs in the network are considered. Average alignment (θ_{avg}) is defined such that for a specific value of θ_{avg}, a CNT in the network is allowed to make any angle between -2θ_{avg} and 2θ_{avg} with equal probability, as shown in Figure 5.6.

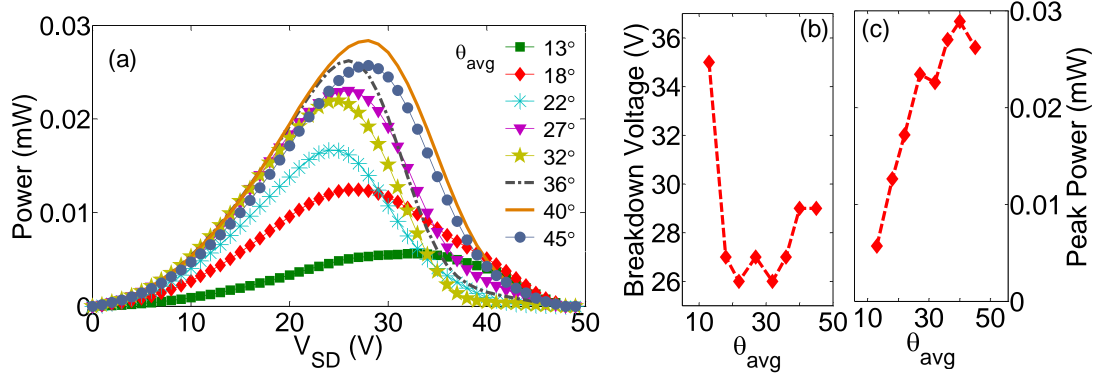

Figure 5.7 (a) Power dissipation vs. source-to-drain voltage (VSD) for different alignments (θ_{avg}) of CNTs in the network. (b, c) V_{BD} and P_{BD} vs. θ_{avg} respectively. Here, Lt = 2 μm, LC = 10 μm, W_C = 10 μm, ρ = 15 CNTs/μm^2. Metallic to semiconducting CNT ratio in the network is 1:2 and their electrical conductivity ratio is 5:1. It should be noted that very few (< 10%) devices have connected pathways at very low angle (θ_{avg} < 10°). However, this number improves (e.g. >70% for θ_{avg} = 13°) significantly for higher θavg.

Figure 5.7(a) shows a plot of power dissipation versus V_{SD} for different network alignments (from θ_{avg} = 9°- 45°). It is observed that for a highly aligned network (θ_{avg} < 10°), devices show negligible current due to the reduced number of percolating pathways bridging the source and drain contacts. However, as θ_{avg} is increased the current increases due to the increasing number of percolating pathways. Previous studies [52] have also suggested that the ON current depends on the alignment and it reaches a maximum at θ_{avg} ~ 30° which is consistent with the results for V_{SD} < 20 V, as shown in Figure 5.7(a). For the breakdown behavior analysis, P_{BD} and V_{BD} dependence on θ_{avg} is investigated. It is found that the V_{BD} first decreases sharply and then shows a zigzag pattern with increasing θ_{avg}. Two local minima are observed at θ_{avg} = 22° and θ_{avg} = 36° [Figure 5.7(b)]. V_{BD} lies in the small range of 26 V to 29 V for θ_{avg} > 10° which suggests a weak dependence of

V_{BD} on alignment. The P_{BD} increases linearly as θ_{avg} increases up to 27° and two 'local' maxima are observed at θ_{avg} = 27° and θ_{avg} = 40° [Figure 5.7(c)].

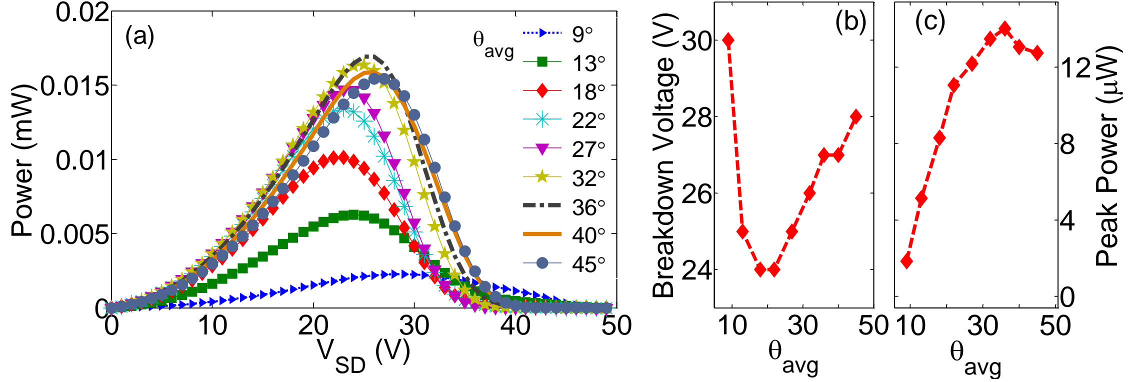

Figure 5.8 (a) Plot of power dissipation in the device vs. source-to-drain voltage (VSD) for different alignments (θavg) of CNTs of purely semiconducting network. (b), (c) breakdown voltage (VBD) and peak power (PBD) are plotted vs. θavg. Here Lt = 2 μm, LC = 10 μm, WC = 10 μm, and ρ = 15 CNTs/μm2.

In order to explore the nature of this dependence, the breakdown pattern of the CNT networks is examined. It should be noted that the network here is considered to be composed of *M* and *S* type CNTs in 1:2 ratio. A Schottky barrier has been assumed to be present between metallic and semiconducting CNTs, and *M-S* junctions are considered to be electrically insulating since *M-M* or *S-S* junction conductance can be 2 orders of magnitude higher than *M-S* junction conductance [45]. It has been shown in previous work [35] that in general heat transfer across the CNT junctions is negligible in comparison to heat transfer across CNT-SiO_2 interface. Therefore the poor thermal contact conductance between CNTs makes crossed-CNT contacts thermally insulating as well [35]. This implies that the network can be considered to be composed of two

independent 'parallel' networks of different densities and conductivities. Therefore the breakdown behavior and characteristics discussed are due to the combined breakdown behavior of pure metallic and semiconducting networks. Figure 5.8(a) shows a plot of power dissipation versus V_{SD} for different θ_{avg} at ρ = 15 CNTs/μm^2 of a homogeneous network (semiconducting CNTs only). It is found that V_{BD} and P_{BD} exhibit only one minima (θ_{avg} = 20°) and maxima (θ_{avg} = 36°) respectively [Figure 5.8(b) and (c)]. A similar trend is observed for pure metallic CNT networks. It should be noted, however, that the density of the metallic and semiconducting networks is in a 1:2 ratio within the combined network, and the location of maxima or minima of the breakdown characteristics depends on ρ [Figure 5.9(a) and (b)]. This is responsible for the existence of the two local optimum points in breakdown characteristics of the heterogeneous network.

5.2.2 Variable alignment angle with log-normal distribution of CNT length

Having discussed the dependence of breakdown behavior on alignment of CNTs where L_t was kept constant, a more general case is considered here. In this section, the breakdown behavior is studied when both CNT length and alignment are varied according to their respective distributions. Figure 5.10 illustrates the log normal distribution of L_t in the network. Here, the device size is $L_C \times W_C = 5 \times 5$ μm, and ρ = 15 CNTs/μm^2.

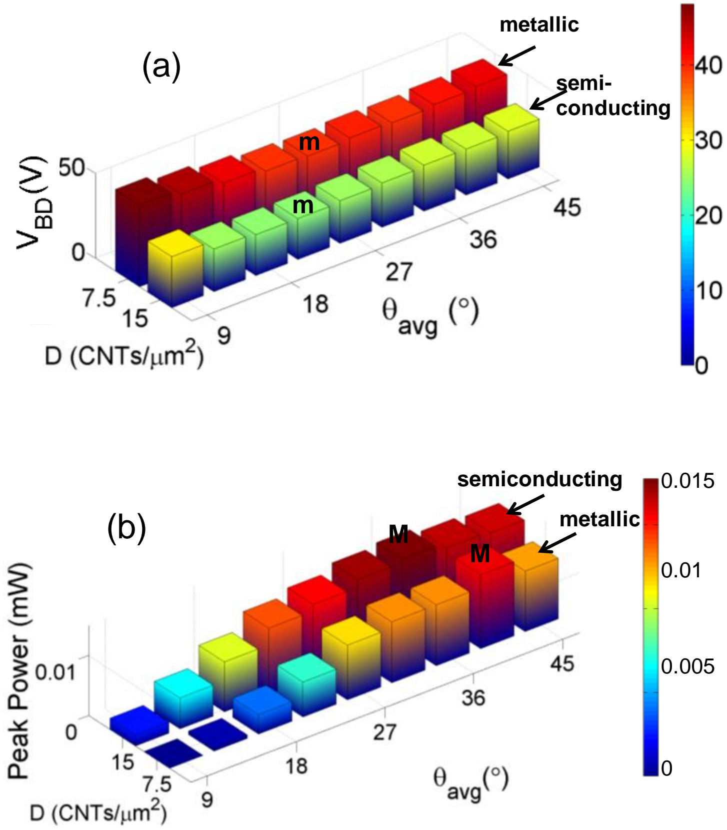

Figure 5.9 A bar plot of (a) breakdown voltage (V_{BD}), (b) peak power dissipation (P_{BD}) versus network alignment (θavg) for metallic (ρ = 7.5 CNTs/μm^2) and semiconducting (ρ = 15 CNTs/μm^2) networks. Letters 'm' and 'M' denote the location of minima and maxima respectively. The metallic to semiconducting CNT density ratio is 1:2 which is same as that in typical unsorted CNT network.

All CNTs are considered to be semiconducting to analyze only the effects of length and alignment distributions. Three different cases of log-normal length distributions (average L_t, $\langle L_t \rangle$ = 1 μm, 1.15 μm and 1.3 μm) and 9 cases of alignment distributions (range of θ_{avg} = 9° (highly aligned network) to 45° (random network)) have been considered. The log-normal distribution is given by following equation:

$$f(L_t,\mu,\sigma)=\frac{1}{L_t\sigma\sqrt{2\pi}}\exp\left[-\frac{(\ln L_t-\mu)^2}{2\sigma^2}\right] \tag{5.1}$$

where f is the probability distribution function, L_t is the CNT length, μ is the mean and σ is the standard deviation of the CNT length. It should be noted that the lognormal distribution of CNT length has a practical significance as this distribution is typically observed in the experiments [56, 169]. The log-normal distribution is expected to affect the reliability and breakdown characteristics of homogenous CNT networks, as a previous study [55] reported that the resistivity of heterogeneous networks varies with the change in the parameters of the log-normal distribution.

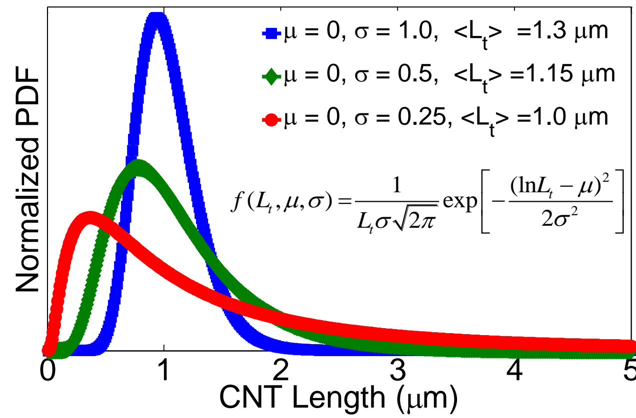

Figure 5.10 Three different log-normal CNT length distributions in the network with average CNT length, <Lt > = 1 μm, 1.15 μm and 1.3 μm.

Results (Figure 5.11) suggest that the effect of the alignment on the breakdown behavior strongly depends on L_t distribution. It is noted that a L_t distribution with higher $\langle L_t \rangle$ provides higher P_{BD}. Also, the θ_{avg} corresponding to the maximum P_{BD} decreases when $\langle L_t \rangle$ is increased. In other words, better thermal reliability can be obtained when $\langle L_t \rangle$ is higher and the network is partially aligned. Interestingly, V_{BD} does not show much

variation despite the fact that P_{BD} changes significantly. The trend of P_{BD} can be explained on the basis of the trade-off associated with the number of percolating paths and resistance of these paths.

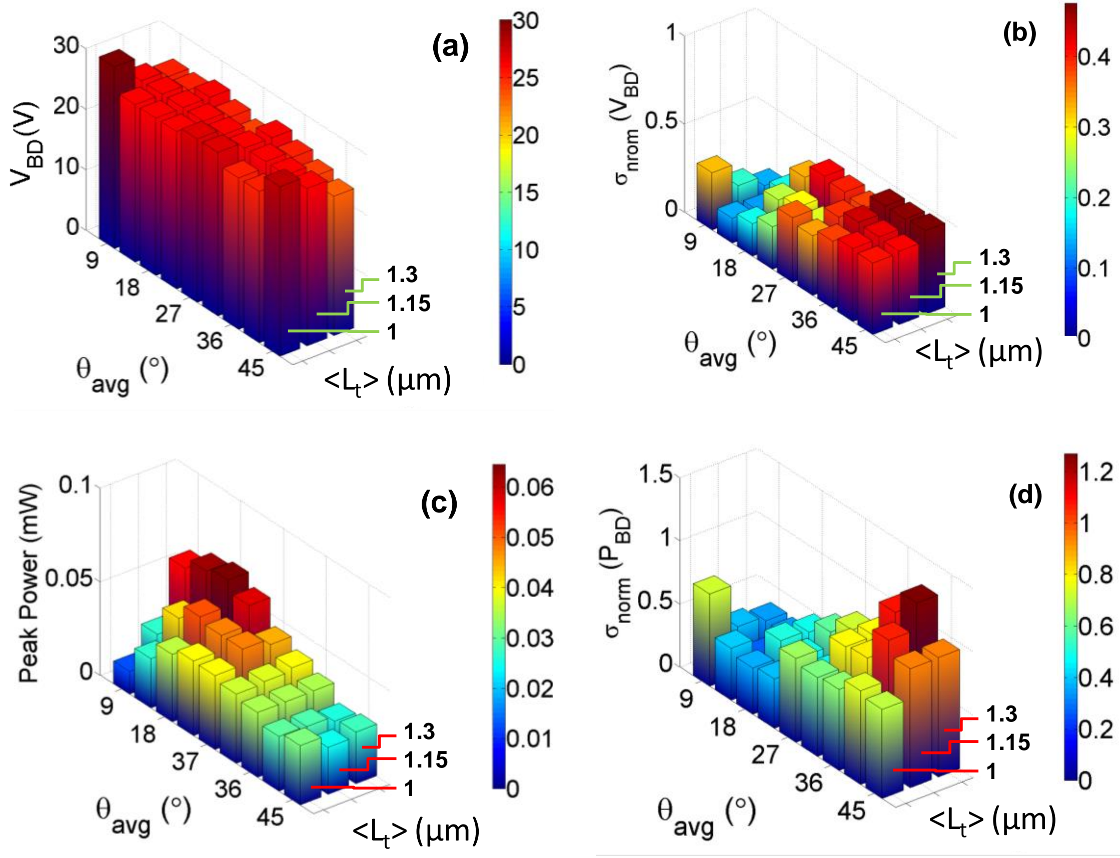

Figure 5.11 A bar plot of (a) breakdown voltage (V_{BD}) (b) Normalized standard deviation (σ_{norm}) of V_{BD}. (c) Peak power (P_{BD}), (d) Normalized standard deviation (σ_{norm}) of P_{BD} for varied alignment and length distributions of the CNT network. The V_{BD} shows little variation as alignment or length distribution is changed, whereas the P_{BD} shows a strong correlation with alignment; this correlation changes significantly as length distribution is changed.

At lower θ_{avg}, the number of percolating paths in the channel will be less, but the resistance of these pathways will be also low due to the lower number of CNT junctions in these pathways. For higher values of θ_{avg}, the network tends toward a random

distribution and the number of connections in the network increases, i.e., the number of effective percolative pathways increases, but the CNT junction density per pathway also increases. Therefore a maximum current (or power) should be achieved for some intermediate θ_{avg} which offers optimal channel resistance. As mentioned earlier, this optimal value of θ_{avg} decreases as $<L_t>$ increases. It is also noted that the standard deviation in V_{BD} and P_{BD} shows little variation with change in $<L_t>$ and θ_{avg}. However, the normalized value of it (σ_{norm}) changes due to the variation in the mean values of the respective variables. More details about power variation with V_{SD} for different lognormal distributions have been included in Figures 5.12 - 5.15. The results in these figures again underline the importance of semi-aligned orientation of CNT networks for longer CNTs and random orientation for shorter CNTs.

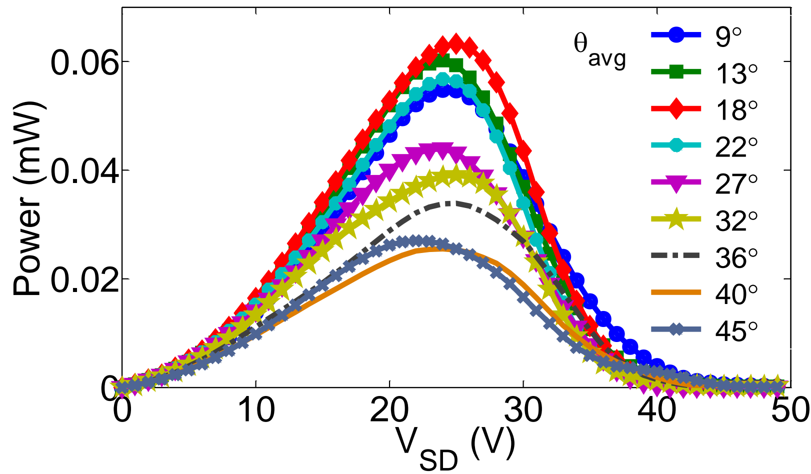

Figure 5.12 Variation in power dissipation with source-to-drain voltage for several alignment cases; CNT length distribution corresponds to $\mu = 0$, $\sigma = 1$ and average CNT length = 1.3 µm. Maximum power dissipation increases with θ_{avg} for $\theta_{avg} = 9°$ to 18°, however it decreases significantly for further increase in θ_{avg}, i.e., the maximum power dissipation is highest for $\theta_{avg} = 18°$. It can be noted that the random network ($\theta_{avg} = 45°$) shows the poorest performance from the point of breakdown behavior and thermal reliability. Interestingly, the voltage corresponding to the peak power does not vary much as θ_{avg} is changed despite the fact that peak power can change up to three times in the range of θ_{avg} considered.

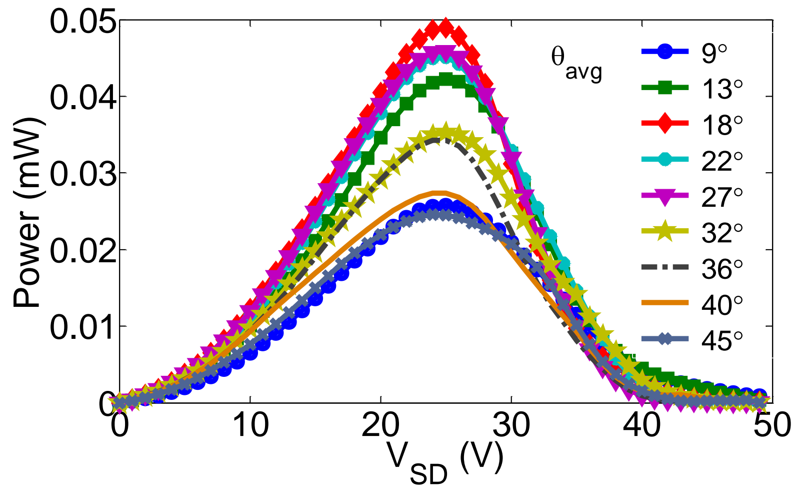

Figure 5.13 Variation in power dissipation with source-to-drain voltage for several alignment cases; CNT length distribution corresponds to $\mu = 0$, $\sigma = 0.5$ and average CNT length = 1.15 μm. Maximum power dissipation is highest for $\theta_{avg} = 18°$. It can be noted here that both highly aligned ($\theta_{avg} = 9°$) and random network ($\theta_{avg} = 45°$) show the poorest performance from the point of breakdown behavior and thermal reliability.

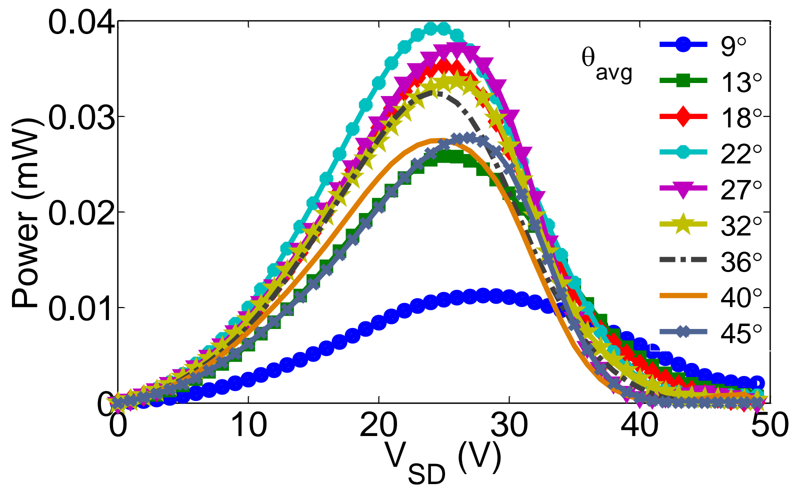

Figure 5.14 Variation in power dissipation with source-to-drain voltage for several alignment cases; CNT length distribution corresponds to $\mu = 0$, $\sigma = 0.25$ and average CNT length = 1 μm. Maximum power dissipation is highest for $\theta_{avg} = 22°$. It can be noted here that the highly aligned network ($\theta_{avg} = 9°$) shows the poorest performance from the point of breakdown behavior and thermal reliability. Also, the difference in the highest maximum power dissipation (at $\theta_{avg} = 22°$) and maximum power dissipation of random network ($\theta_{avg} = 45°$) is significantly less compared to previous two cases. This trend is very similar to that obtained for constant CNT length case since the lognormal CNT length distribution for this case closely resembles to constant CNT length case.

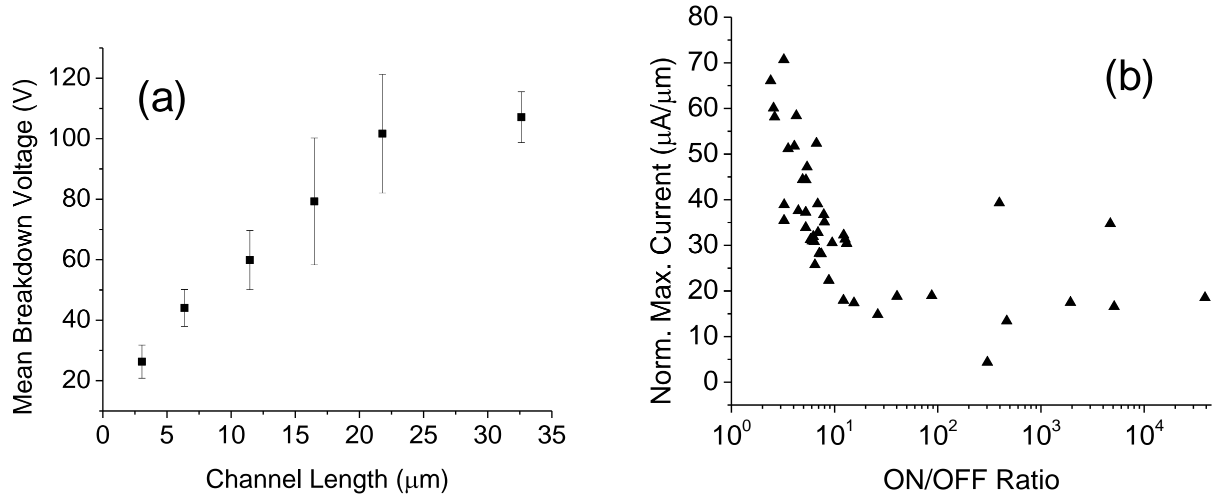

Figure 5.15 Variation of the breakdown voltage V_{BD} versus channel length (L_C). Experimental results are obtained for limited number of devices (total ~30 devices including all the cases). Nevertheless, the general trend agrees well with the simulation results. (b) Variation of normalized maximum current (normalized with respect to W) versus ON/OFF ratio of CN-TFTs. For devices with higher ON/OFF ratio, the maximum current density before breakdown is observed to be lower compared to the devices with lower ON/OFF ratio. It is observed that for semiconducting networks the maximum current is usually lower than the metallic network. Therefore, narrow networks which have more semiconducting paths show lower current capacity. It should be noted that such dependence is observed only when W is less than or comparable to average CNT length and does not exist in case of larger W.

5.3 Closure

In summary, the effects of channel geometry and network morphology on the high field breakdown of carbon nanotube network thin film transistors (CN-TFTs) are investigated. Both experimental and computational techniques are applied to examine the heat dissipation in the device and provide an in-depth analysis of two important characteristics, P_{BD} and V_{BD}, relevant to the breakdown process in CN-TFTs. It is noted that the breakdown characteristics vary significantly with the channel length, but their dependence on the channel width is relatively very small. The results suggest that when

W_C is greater than the average L_t, V_{BD} remains independent of W_C and varies linearly with L_C. The variation in the distribution of alignment and L_t does not significantly affect V_{BD}. However, it is found that P_{BD} increases with both L_C and W_C. In particular, for large W_C, P_{BD} varies linearly with both W_C and L_C. Our results suggest that the thermal reliability of CN-TFTs can be improved by optimizing the CNT length and alignment distribution. In a heterogeneous network, the breakdown characteristics and their relation with the network morphology vary with the ratio of metallic and semiconducting CNTs in the network. The analysis on breakdown behavior of CN-TFT for various log-normal CNT length distribution and several alignment distributions suggests that the heat dissipation and thermal reliability of CN-TFTs can be significantly improved by optimizing the parameters of network morphology.

CHAPTER 6: ELECTRO-THERMAL CROSS-TALK IN ALIGNED CNT TFTs

In this chapter, aligned array CNT TFTs are studied with focus on how electrostatic screening among CNTs affects the overall electrical and thermal performance of these devices. A numerical approach (described in Chapter 2) is utilized to simulate electrical and thermal transport in long channel (micron size) aligned array CNT TFTs. This approach allows us to systematically understand and quantify the role of electrostatic charge screening and thermal cross-talk in electro-thermal transport in CNT TFTs as a function of CNT array density and dielectric oxide thickness.

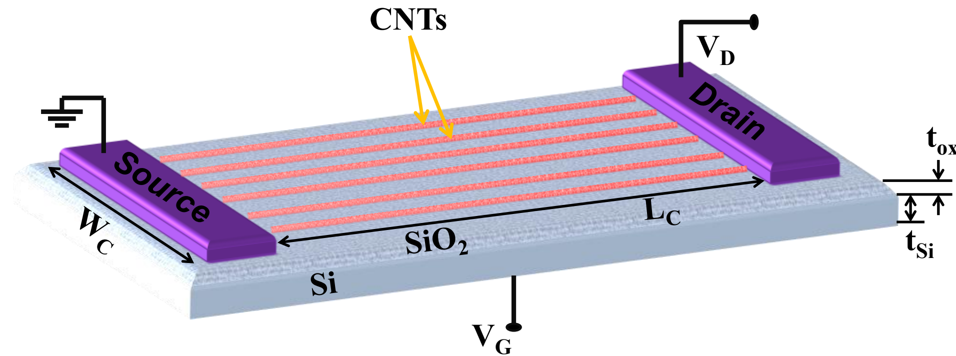

Figure 6.1. Schematic diagram of aligned array carbon nanotube thin-film transistor in back-gate configuration. Channel length (L_C) and width (W_C) are both considered to be 1 µm. Oxide thickness (t_{ox}) is varied from 5 nm to 300 nm. Thickness of p-doped silicon gate (t_{Si}) is 500 µm for all cases. Source and drain are considered to be palladium contacts. All CNTs are semiconducting with diameter, d = 1 nm.

The computational domain for electro-thermal modeling of the CNT-TFT is shown in Figure 6.1 where the channel length (L_c) and width (W_c) are 1 µm each. An

intrinsic semiconducting CNT array with CNT diameter, $d = 1$ nm and band gap, $E_g = 0.8$ eV is used as the channel material. Back-gate geometry (typically used in the experiments) is considered where SiO_2 acts as the gate oxide layer with dielectric constant, $k = 3.9$. The oxide thickness (t_{ox}) has been varied from 10 nm to 300 nm. Si (p++) ($t_{Si} = 500$ μm) acts as the gate electrode. The source/drain are considered to be Palladium (Pd) contacts (metal work function, $\Phi_M = 5.1$ eV). In this work, only p-type CNT array transistors have been studied but the results and analysis can be extended to n-type CNT transistors as well since the operational physical principals remain similar. Ohmic contact is considered between source/drain and the CNTs for hole conduction assuming that the metal Fermi level at contacts is aligned with the valence band edge of CNT. A gate work function ($\Phi_G = \Phi_{CNT}$) is assumed such that CNTs remain intrinsic at gate voltage $V_G = 0$. Density of the CNT arrays has been varied from 5 to 100 CNTs per μm such that the separation distance between neighboring CNTs varies from 200 nm to 10 nm. Oxide thickness (t_{ox}) has been varied from 10 nm to 300 nm.

The bottom surface of the substrate is kept at $T_0 = 300$ K and the top surface is exposed to air with convective boundary condition. In real applications, CNT-TFTs can be top-gated and the substrates may be plastics or glass, which may lead to different CNT-substrate thermal boundary conductance (TBCs). The geometry and material properties of device and boundary conditions can be easily modified in the present model for different applications of CNT-TFTs.

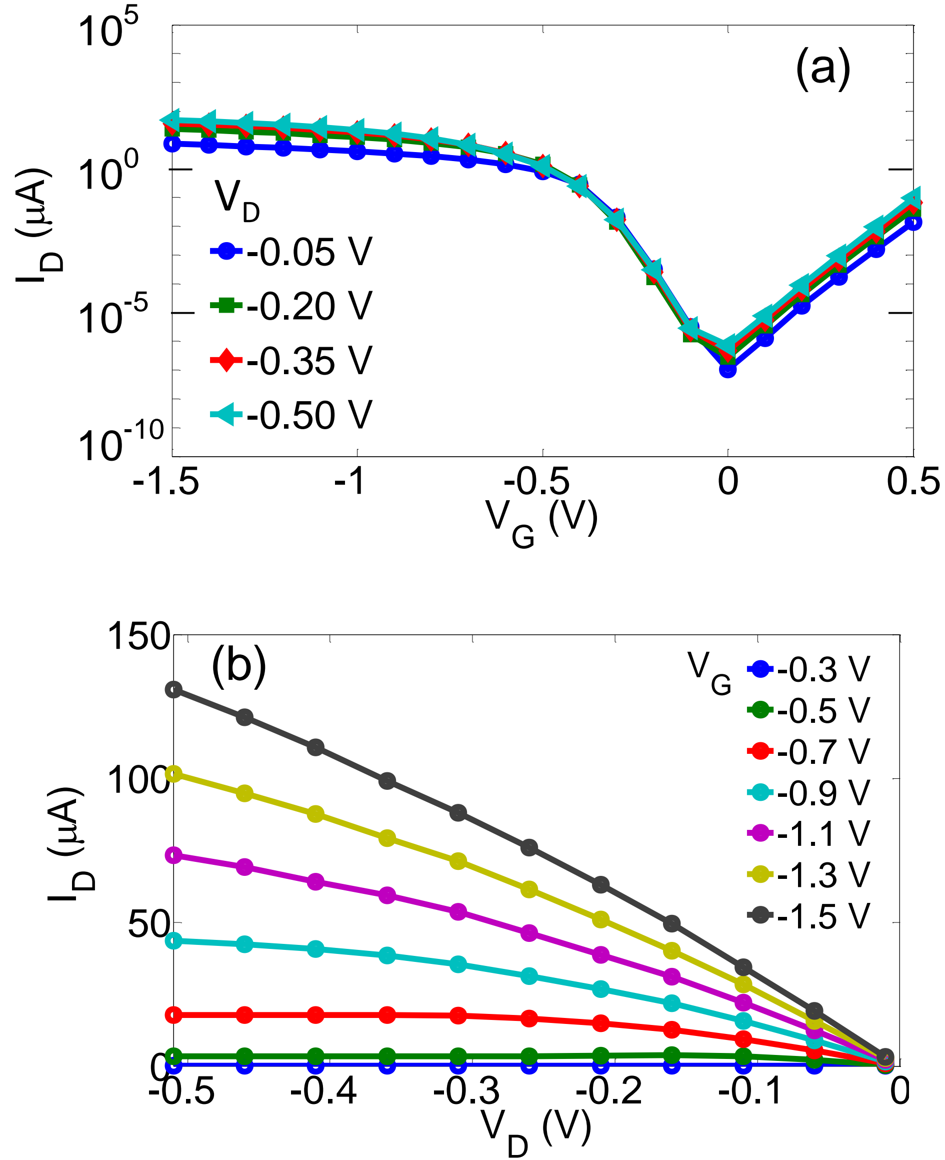

Figure 6.2. (a) Output characteristics (I_D-V_G curves) and (b) Transfer characteristics (I_D-V_D curves) of aligned array CNT-TFT. D = 5 CNTs/μm. L_C and W_C = 1 μm, t_{ox} = 10 nm.

6.1 Transfer and Output Characteristics

With the intent of establishing the validity of computational model for aligned CNT TFTs, the transfer (drain current versus gate voltage) and output (drain current versus source-to-drain voltage) characteristics are plotted as shown in Figure 6.2 (a) and

(b) respectively. On-state channel resistance, obtained from the experiments [62] for aligned array CNT-TFTs, is used to establish the reference for electrical current in the model. Gate voltage is varied between -1.5 V to 0.5 V and source-to-drain voltage is kept between -0.5 V to 0 V. These results are in general agreement (On/Off ratio, ambipolar nature of transfer curves, linear and saturation regions in output curves) with experiments involving diffusive transport in aligned array CNT-TFTs. The exact validation against experimental results has not been attempted as various non-idealities are typically involved in the experiments (*i.e.,* presence of metallic CNTs, surface and bulk trap charges, other imperfections etc.) [57, 62]. The On-state gate voltage in the simulations is considered to be corresponding to V_G = -1 V, where the resistance of semiconducting CNTs is taken as 35 kΩ/μm at CNT array density, D = 5 CNTs/μm. The On-current is ~15 μA and On/Off current ratio ~ 10^7 at V_D = -0.1 V. It should be noted here that the potential across the source/drain contacts reported in the work is the voltage drop across the CNT only, and there will be additional potential drop due to Ohmic resistance across the metal-CNT contacts [170].

6.2 Array Density and Electrostatic Screening

Having established the validity/applicability of the model, the effect of mutual electrostatic screening of CNTs on their charge transport behavior in TFTs is examined. Simulations are performed for moderate to high CNT array densities in the range of 5 - 100 CNTs/μm. Figure 6.3(a) shows the total On- and Off-current variation of the device with respect to CNT array density. On- and Off-current here, are taken at V_G = -1 V and 0 V respectively at V_D = -0.1 V. It is noted that as the array density increases from 5

CNTs/μm to 100 CNTs/μm (*i.e.*, separation distance between the CNTs decreases from 200 nm to 10 nm), the On-current increases sub-linearly by approximately 5 times from 15 μA to 75 μA. The Off-current, however decreases more steeply than On-current as the CNT density is increased. However when the current is calculated on per CNT basis, both On- and Off-currents decrease with increasing array density (Figure 6.4b) underlining the adverse effect of electrostatic screening of charges in CNTs.

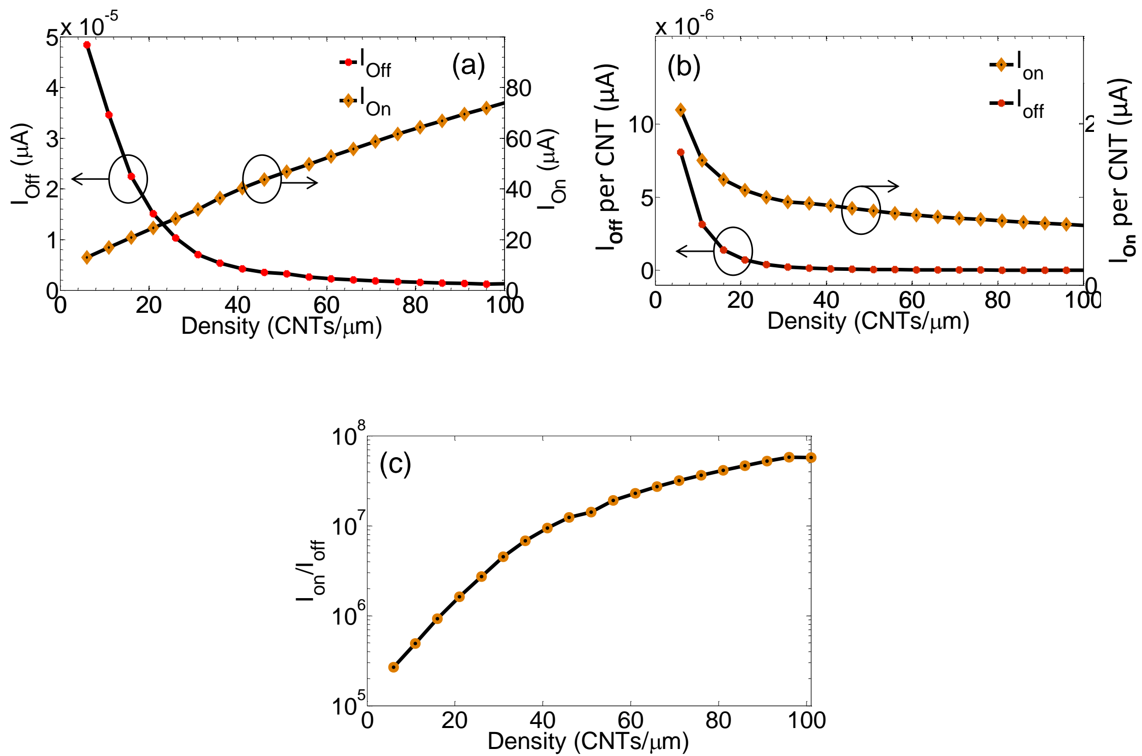

Figure 6.3. Variation of Off-current (left y-axis) and On-current (right y-axis) as a function of density of CNT arrays in the channel. Variation of (a) Total current, (b) current per CNT, (c) On/Off current ratio. $L_C = 1$ μm, $W_C = 1$ μm, $t_{ox} = 300$nm.

It is further noted that the screening effect diminishes Off-current more than the On-current as can be seen in Figure 6.3c where On/Off current ratio is plotted with density. It is found that the On/Off current ratio can increase by more than two orders of

magnitude when the density is increased from 5 CNTs/μm to 100 CNTs/μm. The rise in On/Off current ratio is steep between 5 CNTs/μm to 50 CNTs/μm, after which it starts saturating. These results suggest that although the current per CNT decreases as the CNT density increases due to charge screening, the total On-current and the On/Off ratio can increase substantially, and therefore the denser arrays of CNTs in CNT-TFTs can benefit device performance significantly both for analog and digital applications.

6.3 Gate Coupling and Electrostatic Screening of CNTs

Besides the array density, the electrostatic screening among the CNTs also depends on the gate oxide thickness (t_{ox}) because of the 3-D electrostatics of CNT-TFTs. In order to explore this dependence, simulations are performed for different values of t_{ox}.

Figure 6.4(a) shows the device On-current variation with array density for values of t_{ox} in the range of 10-300 nm. It is noted that the On-current increases with reduced t_{ox} for any given array density. In addition, the rate, at which On-current changes with density, increases with reduced t_{ox}. Figure 6.4b shows the variation of On-current per CNT with density for different values of t_{ox}. Lower t_{ox} leads to higher On-current per CNT as well. The device Off-current however decreases with reduced t_{ox} (Figure 6.4c). Thus, the On/Off ratio increases as t_{ox} is reduced for a given array density (Figure 6.4d). The On/Off ratio increases at faster rate with array density for lower t_{ox}. These results suggest that better gate-coupling due to reduced t_{ox} and denser CNT arrays are beneficial for improved device performance in terms of higher On-current and higher On/Off ratio.

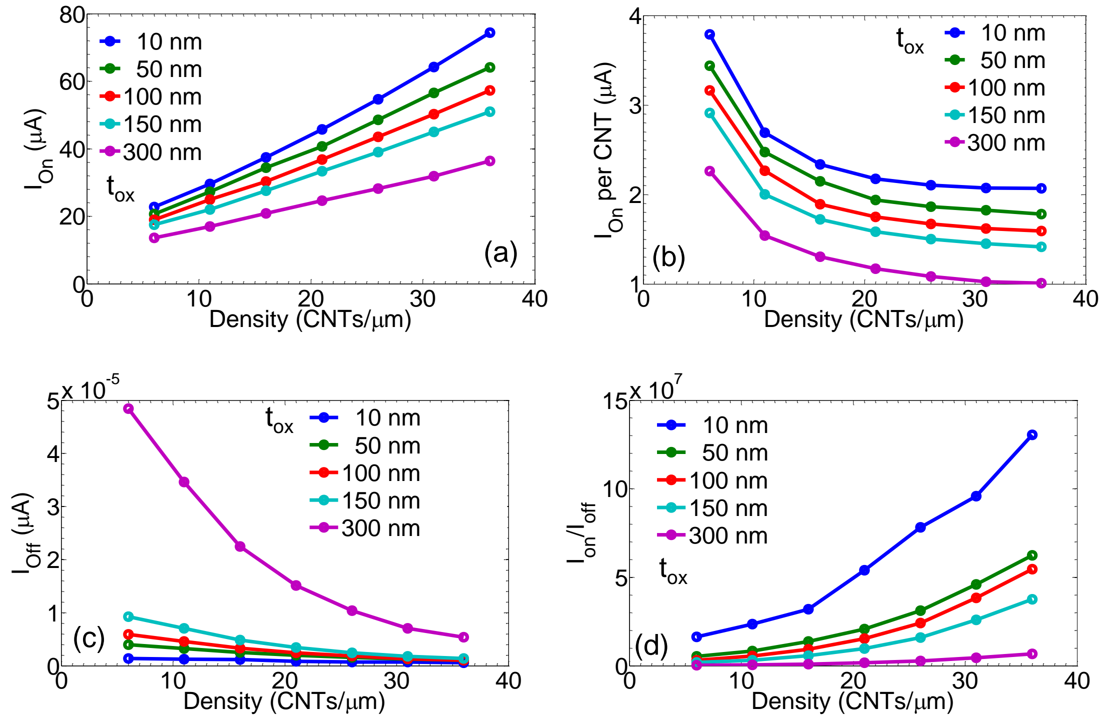

Figure 6.4. Variation of (a) Device On-current, (b) On current per tube, (c) Device Off-current and (d) On/Off current ratio with CNT array density for different oxide thickness. On- and Off-currents values are taken at V_G = -1 V and V_G = 0 V respectively at V_D = -0.1 V. L_C = 1 μm, W_C = 1 μm.

6.4 Power Dissipation and Temperature Profile

As described in previous Section, the denser CNT arrays can be beneficial for improved electrical performance of the CN-TFTs. Denser arrays also result in higher power density (power per unit area) in CNT-TFTs. During the transistor operation, the Joule heating in CNTs leads to rise in temperature of both CNTs and the substrate. If the CNT density is high enough, it is found that there is a thermal cross-talk among the CNTs (via substrate) in addition to electrical cross-talk. The thermal coupling among the CNTs can also play a critical role during the electrical breakdown process which is utilized to remove the metallic CNTs from the CNT arrays [57]. During the electrical breakdown

process, a high source-to-drain bias is applied under 'Off-state' of CNT-TFTs which leads to high Joule heating in metallic CNTs causing them to reach the breakdown temperature (600 ^{o}C in air) and be practically removed from the channel. However, the high temperature of metallic CNTs can also affect the temperature of neighboring semiconducting CNTs and may lead to their breakdown due to thermal coupling via substrate. In order to explore the thermal implications of high density arrays, simulation is performed for thermal transport in CNT-TFTs. Properties such as interfacial thermal conductance of substrate and CNTs are taken from the previous studies of random network CNT-TFTs [171, 172].

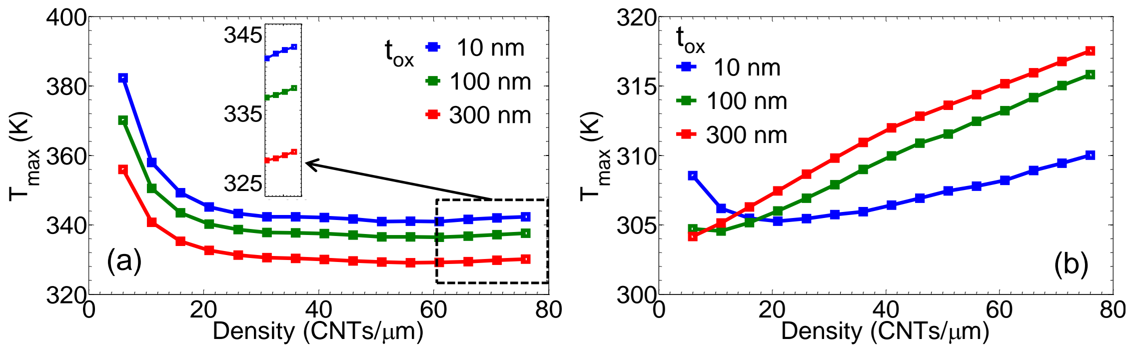

Figure 6.5. Variation of maximum temperature (T_{max}) of (a) CNT array, (b) substrate with CNT array density. V_G = -1 V and V_D = -0.25 V. Inset of figure (a) shows the increasing trend in T_{max} after D = 60 CNTs/μm.

Figure 6.5(a) shows the variation of maximum temperature (T_{max}) of channel (CNTs) with array density for different values of t_{ox} corresponding to V_G = -1 V and V_D = -0.25 V. It is noted that as t_{ox} is reduced, T_{max} increases due to higher current (higher power dissipation) which is a consequence of better gate-channel coupling. It is further found that for a given t_{ox}, the T_{max} decreases as density increases (between 5 - 50

CNTs/μm) as the charge screening among CNTs lower current (lower power dissipation) per CNT with increasing density; a very sharp decline between 5 - 20 CNTs/μm is observed. However, for D > 50 CNTs/μm, despite low current per CNT, there is an increase in the T_{max} of the channel (as shown in Figure 6.5(a) inset) which can be attributed to thermal coupling or cross-talk among CNTs via substrate. The temperature of CNT not only depends on the power dissipation in it, but also on how the heat dissipated in CNTs spreads within the substrate which in turn depends on the array density and the t_{ox}.

The variation in T_{max} of the oxide layer shows slightly more involved behavior (Figure 6.5b). For thin oxide layer (t_{ox} = 10 nm) and for low array density (D < 20 CNTs/μm), there is minimal lateral heat spread and the dissipated heat is directly transferred through the oxide layer to the Si substrate. Therefore, it is noted that for t_{ox} = 10 nm, increase in T_{max} of oxide layer is preceded by a decline when density is increased (blue curve in Figure 6.5b). However, for higher t_{ox}, the lateral heat spreading (responsible for thermal cross-talk of CNTs) become important and the minima in T_{max} shifts to the lower side of density, e.g., for t_{ox} = 100 nm, minima in T_{max} is observed at D ~ 10 CNTs; and for t_{ox} = 300 nm, T_{max} increases monotonically with array density. This involved trend of the variation of T_{max} with array density for different values of t_{ox} shows the interesting overlapping effects of electrostatic and thermal cross-talk of CNTs. These results suggest that when the distance between CNTs is comparable or smaller than t_{ox}, T_{max} of oxide layer increases monotonically where the total power dissipation (rather than power dissipation per CNT) dictates the temperature profile.

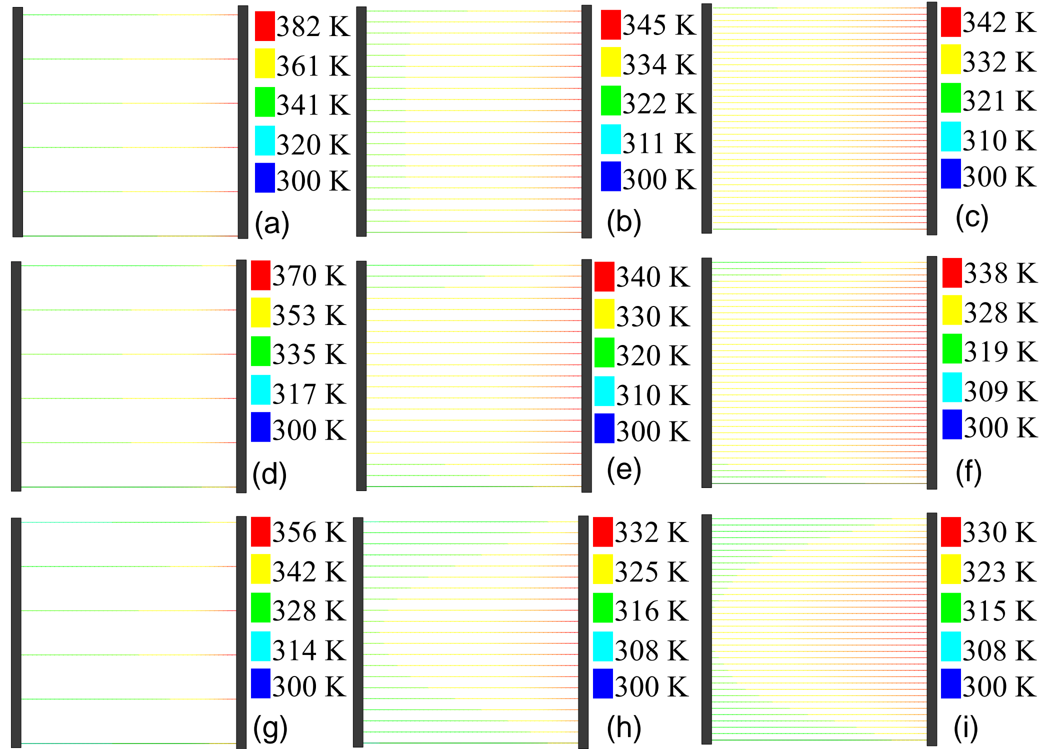

Figure 6.6. Temperature profile of CNTs (a) 5 CNTs/μm, (b) 20 CNTs/μm and, (c) 35 CNTs/μm; t_{ox} = 10 nm, (c) 5 CNTs/μm, (d) 20 CNTs/μm and, (e) 35 CNTs/μm for t_{ox} = 100 nm, and (g) 5 CNTs/μm, (h) 20 CNTs/μm and, (i) 35 CNTs/μm t_{ox} = 300 nm. As the gate oxide thickness increases, power density in the CNTs also decreases resulting in lower temperature.

In order to better understand this behavior, the temperature contour profiles of CNTs and the top surface of oxide layer which is in direct contact with the CNTs are further analyzed. It is noted that the temperature profile changes significantly with both array density and t_{ox} (Figure 6.6). For t_{ox} = 10 nm and a given array density, the temperature variation along the CNT is nearly identical (Figure 6.6a, b, c) for all the 'inner' CNTs with maximum temperature occurring near the drain electrode. The lower temperature for outermost CNTs is due to the electrostatic and thermal edge-effects. For t_{ox} = 100 nm (Figure 6.6d, e, f) and t_{ox} = 300 nm (Figure 6.6g, h, i), it is found that the

spatial variation in the temperature exists not only across the channel length but also across the channel width, e.g., the temperature profile in CNTs located at the middle of the channel is much different than the ones located at the edges. It should also be noted that the temperature gradient (T_{max} - T_{min}) in the channel decreases as array density increased.

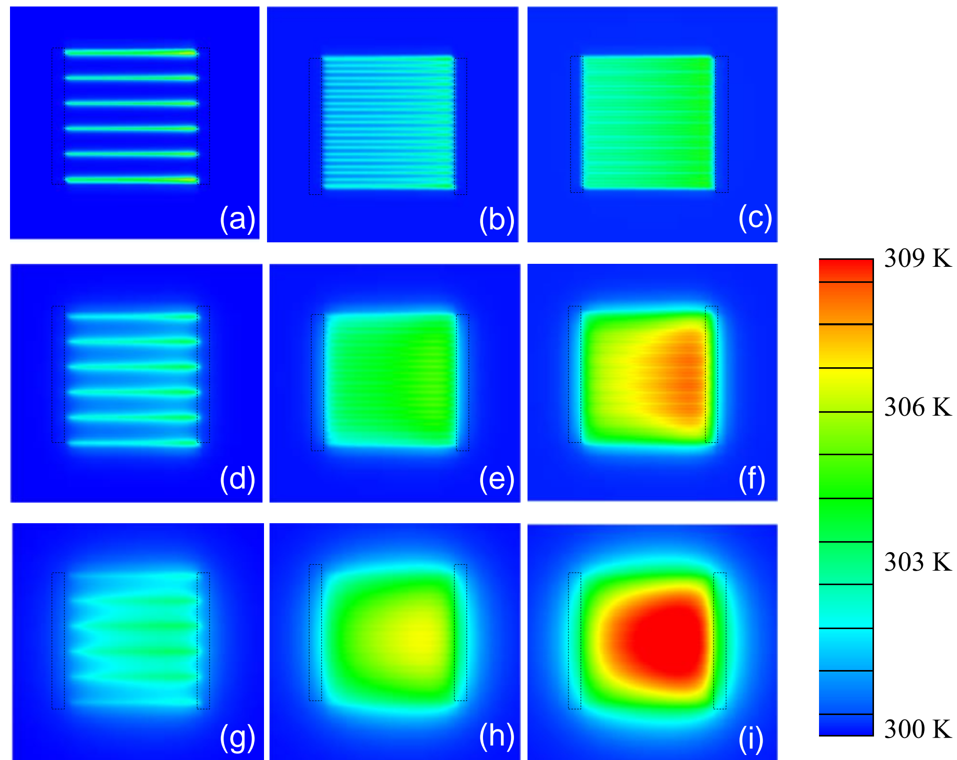

Figure 6.7. Temperature profile of the top surface of oxide layer (a) 5 CNTs/µm, (b) 20 CNTs/µm and, (c) 35 CNTs/µm; t_{ox} = 10 nm, (c) 5 CNTs/µm, (d) 20 CNTs/µm and, (e) 35 CNTs/µm for t_{ox} = 100 nm, and (g) 5 CNTs/µm, (h) 20 CNTs/µm and, (i) 35 CNTs/µm t_{ox} = 300 nm. As the gate oxide thickness increases, greater thermal resistance leads to higher temperature.

Figure 6.7 shows the temperature contour plots of the top surface of the oxide layer which is in direct contact with the CNTs. For t_{ox} = 10 nm (Figure 6.7a, b, c), temperature variation along the CNT 'foot-print' is very small. However, for t_{ox} = 100 nm

(Figure 6.7d, e, f) and t_{ox} = 300 nm (Figure 6.7g, h, i), a substantial spatial temperature variation is observed. For higher array density, the foot-prints of CNTs starts merging (indication of thermal cross-talk) leading to a single large hot-spot with maximum temperature region at the middle of the channel close to the drain electrode. For higher values of t_{ox} (~100, 300 nm), it is clearly noted that maximum temperature increases with increasing density due to higher power density in the channel. It should be noted here that the temperature range shown in the current work are for linear regime (V_G = -1 V and V_D = -0.25 V) of the transistor operation. The temperature rise in the channel will be significantly large for higher values of V_D and in the saturation regime of operation.

6.5 Closure

In summary, electro-thermal transport in aligned array CNT- TFTs is studied using a computational approach. With increasing CNT array density, electrostatic charge-screening among CNTs and the power density in the channel increase which have direct effect on the electrical and thermal performance of CNT-TFTs. The array density and oxide thickness is systematically varied to study the implication of electrostatic screening and thermal coupling on the On-current and temperature profiles of CNT TFTs. The results from this work indicate that: (1) As the CNT array density increases from 5 CNTs/µm to 100 CNTs/µm, charge screening among the CNTs lowers the current per CNT. However, the addition of CNTs benefits the total On-current in the device as it increases by nearly 5 times sub-linearly. (2) The On/Off current ratio increases by more than two orders of magnitude when the CNT density is increased from 5 CNTs/µm to 100 CNTs/µm, where most of the increase occurs below 50 CNTs/ µm as the On/Off ratio

plateaus afterwards. These results suggest that although the current per CNT decreases due to charge screening as the CNT density increases, the device On-current and the On/Off ratio can increase substantially, and therefore the denser arrays of CNTs in CNT-TFTs can benefit device performance significantly particularly for logic devices. (3) For lower CNT array densities (< 50 CNTs/μm), the temperature of CNTs decreases with increased density due to lower current per CNT caused by charge screening among CNTs. For Higher densities (> 60 CNTs/μm), thermal coupling among CNTs becomes significant and the temperature of CNTs starts increasing with increased CNT density. (4) Thinner gate oxide leads to higher On-current in the device which leads to larger power dissipation and higher temperature; therefore oxide thickness need to be optimized along with CNT array density to improve electrical and thermal performance and energy efficiency of the CNT-TFTs. The targeted array density (>100 CNTs/μm) for high performance CNT array based TFTs will present thermal reliability issues emphasizing the importance of design optimization of the device for thermal management of the large scale integrated circuits.

CHAPTER 7: HYSTERESIS IN ALIGNED CNT TFTs

This chapter presents analysis on the mechanism of hysteresis in aligned CNT TFTs with focus on the role of interface trap charges. A modeling approach, described in chapter 3, is applied to analyze the effects of interface trap charges on hysteresis in current-voltage characteristics during forward (positive to negative) and reverse (negative to positive) gate voltage sweep. Variations in the rate (with respect to time) of gate voltage sweep, interface trap charge concentration, oxide thickness and CNT array density are systematically studied. The magnitude of the hysteresis is quantified as the difference between the gate voltages required to obtain average of maximum and minimum currents during forward and reverse sweeps.

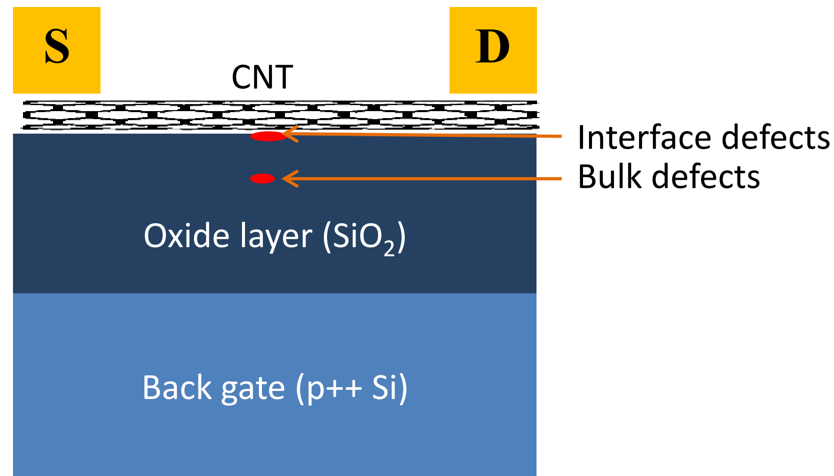

Figure 7.1. Schematic diagram of CNT TFT illustrating the location of trap charge defects responsible for hysteresis.

Hysteresis in CNT TFTs is caused by the charge defects which can be present at the CNT oxide interface and within the oxide layer. Hydroxyl (-OH) group's defects are

generally found at the CNT-substrate interface as an artifact of fabrication techniques of the device. Trapping and detrapping of electrons by these –OH groups, during the forward and reverse sweep of the gate voltage, affects the electrostatic field in CNTs which changes the charge concentration in the channel. At positive gate voltage –OH groups can trap electrons to facilitate hole conduction during the forward sweep (positive to negative gate voltage). At negative gate voltage –OH groups release electrons to attain their neutral state to reduce hole conduction during the reverse sweep (negative to positive gate voltage). This results in different transfer curves (I_D-V_G) for forward and backward sweeps. This temporal instability in I_D-V_G curves leads to hysteresis in transistors.

Bulk defects are generally due to the broken bonds within the amorphous oxide. Bulk defects either act as electron traps (switching between negative and neutral charged states) or hole traps (switching between positive and neutral charged states).

7.1 Impact of Sweep Rate (SR)

Since the time scales of electron trapping and de-trapping process may differ from each other, gate voltage sweep rate may affect the hysteresis. Therefore, here we investigate the effect of change in the gate voltage sweep rate on the hysteresis for interfacial and oxide trap charges separately. Sweep rate of gate voltage have been varied between 0.002 V/s to 20 V/s.

7.1.1 Interface Trap Charges

Figure 7.2 shows the hysteresis in current-voltage characteristics due to interfacial trap charges for different sweep rates (SR) of gate voltage. Trap density (N_T) is here considered to be 5 x 10^{11} /cm^2 and the value of capture coefficient (σ) is taken to be 10^{-16}. It is found that that the change in the sweep rate does not cause any change in the hysteresis for the range of sweep rates (0.002 V/s to 20 V/s) considered here. The results indicate that the interfacial trap charges trapping/de-trapping process is much faster compared to the time scales of the rate of change in gate voltage. These results are consistent with observations made by earlier studies [153].

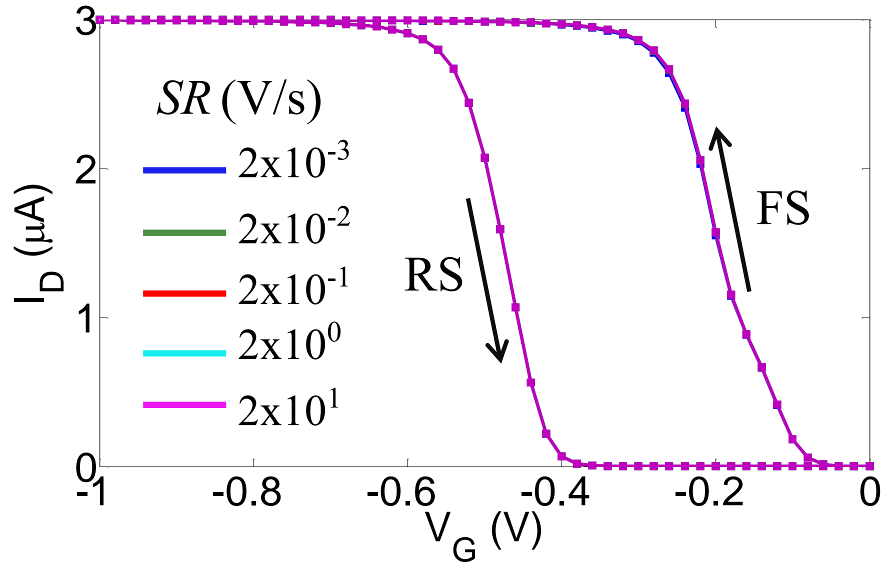

Figure 7.2. Current (I_D) versus gate voltage (V_G) characteristics during forward sweep (FS) and reverse sweep (RS) of gate voltage at different values of sweep rates. Here, trap charges are considered to be present at the CNT-oxide interface.

7.1.2 Bulk Trap Charges

Figure 7.3 shows the hysteresis in current-voltage characteristics due to oxide trap charges present near the CNT for different sweep rates. These oxide traps switch between negative and neutral charged states. Trap density (N_T) is here considered to be 5 x 10^{11} /cm^2 and the value of capture coefficient (σ) is taken to be 10^{-13}. It is noted here that with the increase in the sweep rate in the range considered here, the hysteresis in the device initially increases. However, not much change is observed in the hysteresis after the sweep rate of 0.2 V/s. The trend can be explained as follows. At the beginning of forward sweep, all the electron trap sites are filled. But as the gate voltage is changed during forward sweep, de-trapping process of the trapped electrons also starts. Faster the sweep rate, slower is the process of de-trapping. In addition, above a certain sweep rate (e.g., 0.2 V/s in these simulations), current reaches maximum value before trap sites even begin to release the trapped electrons.

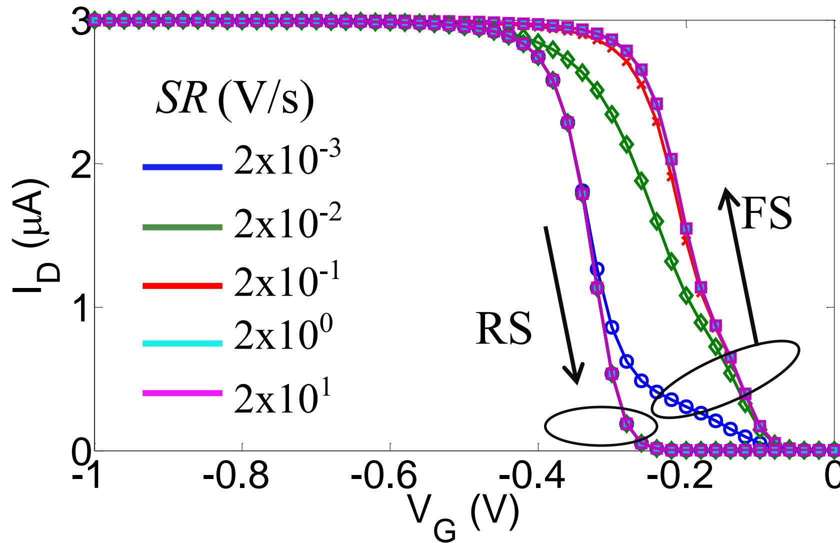

Figure 7.3. Current (I_D) versus gate voltage (V_G) characteristics during forward sweep (FS) and reverse sweep (RS) of gate voltage at different values of sweep rates. Here, the trap charges are considered to be present near the CNT within the oxide layer.

7.2 Impact of Interface Trap Charges Concentration

Defect charge concentration at the interfaces can vary depending upon the process steps involved during the fabrication process. Higher trap charge concentration (N_T) leads to greater hysteresis. To quantify this effect, transfer curves (I_D -V_G) for different values of interfacial N_T are obtained as shown in Figure 7.4. Results indicate that negligible hysteresis is observed below N_T = 5 x 10^9 /cm^2. However for higher values of N_T, the hysteresis increase linearly (Figure 7.5) within the range of N_T considered here. It should be noted here that the x-axis in Figure 7.5 is plotted on log scale and hence the dependence of V_{HYST} on N_T, seems exponential.

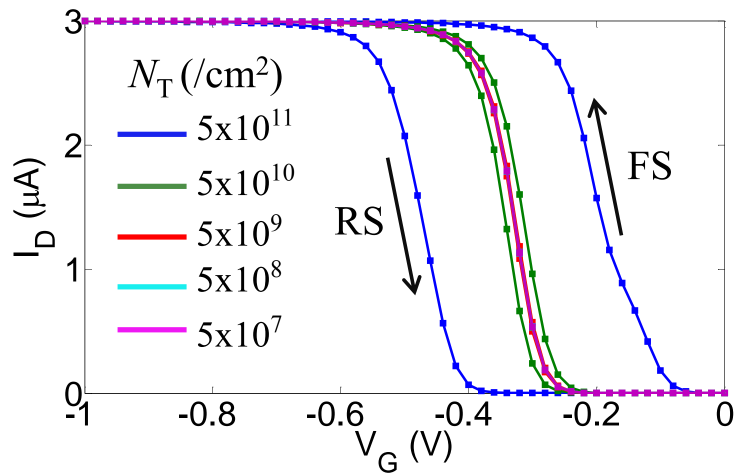

Figure 7.4. Current (I_D) versus gate voltage (V_G) characteristics during forward sweep (FS) and reverse sweep (RS) of gate voltage at different values of interface trap concentration (N_T). Hysteresis increases with the increase in the interface trap density.

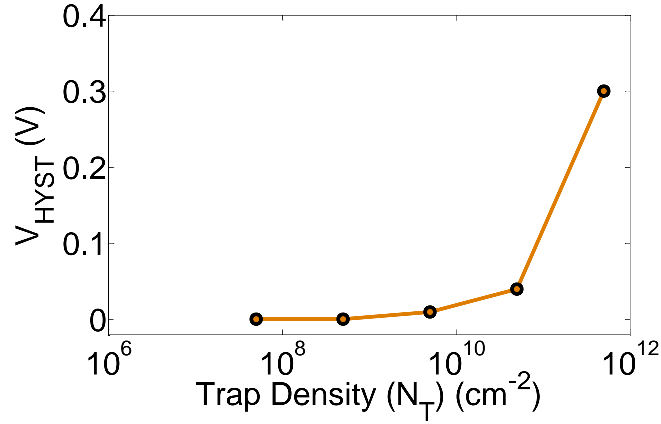

Figure 7.5. Variation of hysteresis (V_{HYST}) voltage with trap density (N_T).

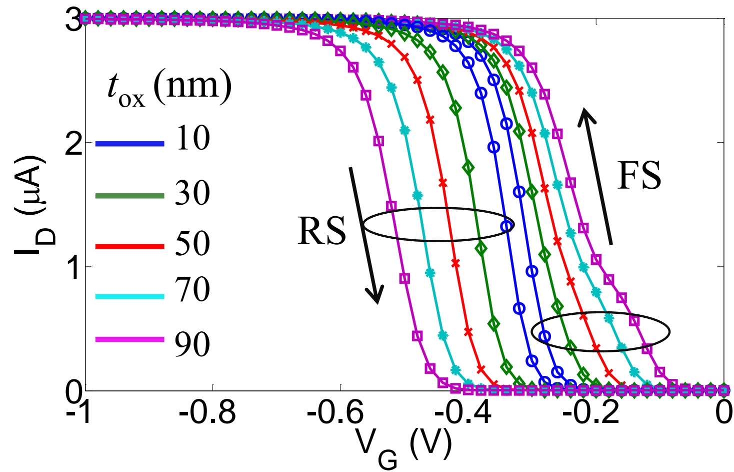

Figure 7.6. Current (I_D) versus gate voltage (V_G) characteristics during forward sweep (FS) and reverse sweep (RS) of gate voltage at different values of oxide layer thickness.

7.3 Impact of Oxide Thickness

The probability of occupation of interfacial trap sites depends on the electron and hole concentration in CNTs which in turn depends on the gate voltage and also on the oxide thickness (t_{ox}). Figure 7.6 shows the hysteresis due to interfacial trap charges for

different values of t_{ox}. It is noted that as t_{ox} increases, hysteresis also increases linearly. For higher values of oxide thickness, the trapping/detrapping process is slower due to lower capacitive coupling between CNTs and gate electrode. This leads to greater hysteresis for thicker oxide layer.

7.4 Impact of CNT Array Density

In aligned array CNT TFTs, electrostatic interaction among the CNTs changes the charge concentration in CNTs as discussed in the previous chapter. Thus, the electrostatic cross-talk among CNT can also affect hysteresis caused by trap charges. Figure 7.7 shows the effect of CNT array density on the hysteresis due to the interfacial trap charges. As the density increases, the total On-current increases but so does the hysteresis. These results underline the importance of the removal of interfacial trap charges for mitigation of hysteresis in dense array CNT TFTs.

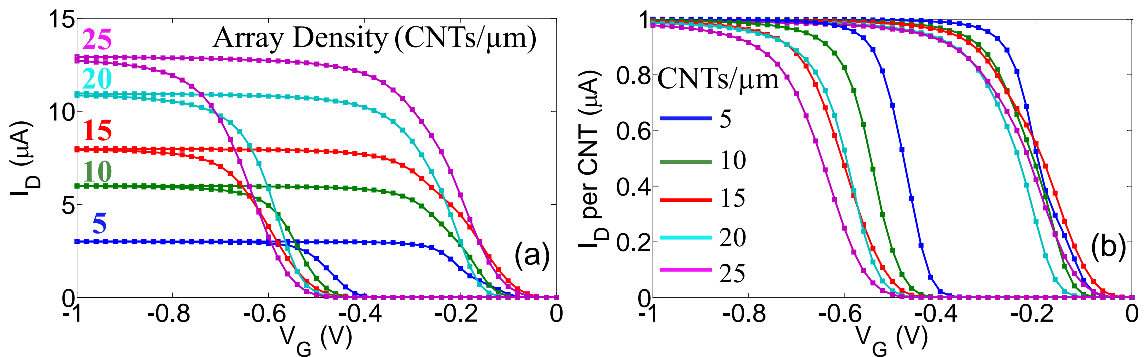

Figure 7.7. Current (I_D) versus gate voltage (V_G) characteristics during forward sweep (FS) and reverse sweep (RS) of gate voltage at different values of CNT array density. (a) total current, (b) current per unit CNT.

7.5 Closure

In summary, hysteresis in aligned CNT-TFTs is investigated using a computational approach. Impact of several parameters such as sweep rate of gate voltage, location and density of trap sites, oxide layer thickness and CNT array density on the hysteresis phenomenon has been investigated by varying these parameters and analyzing corresponding transfer curves for forward and reverse sweeps. It is found that for interfacial trap charges, change in sweep rate does not cause any change in the hysteresis. For bulk oxide charges near the CNT, higher sweep rates cause greater hysteresis. Hysteresis is found to increase with higher oxide thickness and higher CNT array density. The analysis has been presented only for p-type transistors. The hysteresis behavior of n-type transistors may be different because the dynamics (trap filling probability rate) of electron/hole trapping and detrapping process between n-CNT and interface and oxide trap charges may be different.

CHAPTER 8: DISSIPATIVE PARTICLE DYNAMICS STUDY OF CNT-LIQUID CRYSTAL COMPOSITES

This chapter presents an analysis on Liquid Crystals (LC) -CNT composites using DPD simulations. The goal of the present work is to study the scope of this technique in exploring the dynamic behavior of the LC –CNT composites under DC and AC external electric field. A range of DC and AC electric field amplitudes/magnitudes have been applied. CNT concentration has been varied in the composite to systematically analyze the effect of CNTs in LC ensemble on the system anisotropy and associated dynamics.

8.1 Order Parameter and Calculation of Rotational Viscosity

One of the most useful parameter to measure the average orientation of LC system is known as *Order Parameter* (*S*). It quantifies the degree of anisotropy present in the system. It is calculated as the highest eigenvalue of ordering tensor, Q defined as:

$$Q = \frac{1}{2}\left(3\langle \hat{\mathbf{u}}\hat{\mathbf{u}} \rangle - I\right) \tag{8.1}$$

Here, $\hat{\mathbf{u}}$ is unit vector along the axis of LC molecule and I is 3x3 identity matrix. The product in the bracket (< >) is a tensor product of unit vector $\hat{\mathbf{u}}$ with itself. The bracket symbol means average over all the molecules. The eigenvector corresponding to the highest eigenvalue of Q is called director which specifies the unit vector along the direction of average orientation of the system.

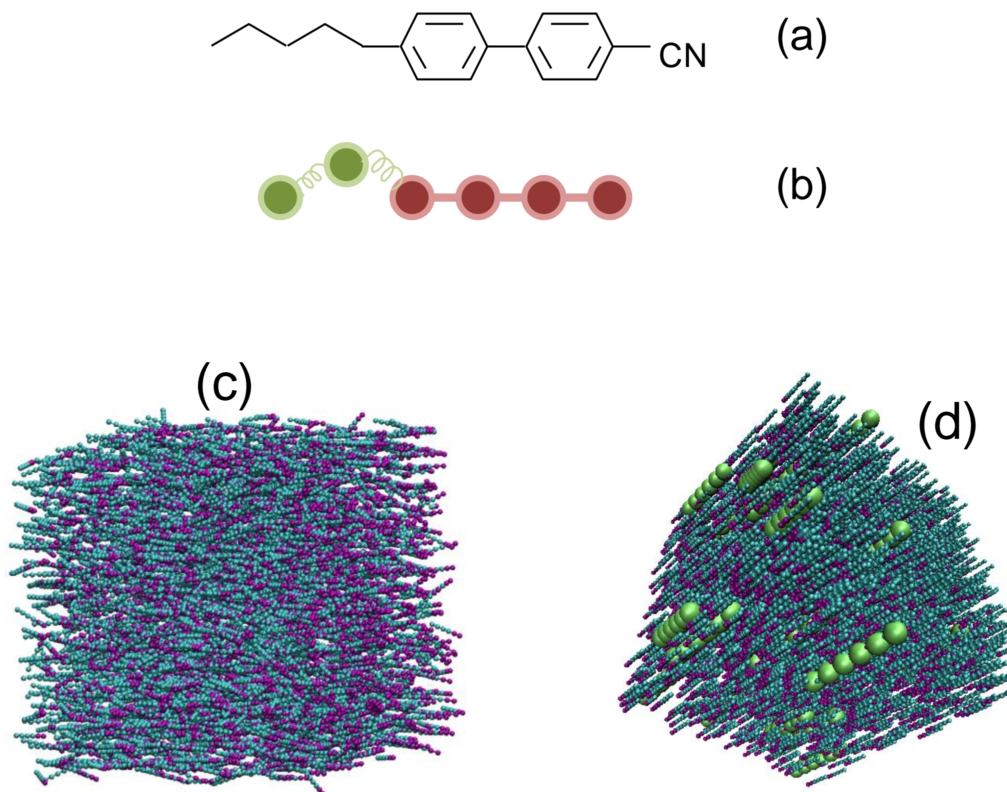

Figure 8.1 (a) Schematic representation of 5-CB molecule, (b) Bead representation of 5-CB where rigid part is modeled as four locked DPD beads which move together in rigid manner and the flexible alkyl groups are modeled as two additional beads connected to one end of the rigid beads which are free to move according to a harmonic potential. (c) Simulation box for ensemble of semi-rigid chain 5-CB molecules. (d) Simulation box for ensemble of semi-rigid chain 5-CB molecules and rigid CNTs.

The zero value of S corresponds to completely random or isotropic phase. The limit, $S = 1$ corresponds to a completely aligned system, *i.e.,* perfect alignment of all molecules in a direction which may not be realized in practice. Typically the value of S is between 0.3 and 0.8 for the nematic phase in which the molecules align on-average along a particular direction but lack the positional order. The experimental value of S for 5-CB is observed to be approximately 0.75 at room temperature [173]. In the simulations, the

system is initialized at $S = 1$ and allow it to equilibrate at room temperature. The DPD parameters are chosen in such a way that the equilibrium value of S for the system matches closely to the experimental value. The validity of choosing these values of DPD parameters is confirmed by calculating the rotational viscosity (γ_1) of 5-CB which closely agrees with experimental values (Figure 8.2) [174]. γ_1 is calculated from the relation given in equation (8.2) where ρ is number density of LC molecules, k is Boltzmann constant, T is temperature and $D_\perp$ is diffusion constant as calculated from equation (8.3). P_2 and P_4 are order parameters of rank two and four respectively as defined in equation (8.4). τ_{00} is a time constant calculated using time variant response of time correlation function (Φ), by fitting exponential decay response from equation (8.6). Φ is calculated with the help of Wigner D-matrix elements (equation 8.5) where m = n =0 and L = 1 for axis symmetric rigid molecules as considered in the present study.

$$\gamma_1 = \frac{\rho kT}{D_\perp}\left(\frac{35\overline{P_2^2}}{16\overline{P_4}+5\overline{P_2}+14}\right) \tag{8.2}$$

$$D_\perp = \left[6\tau_{00}\frac{7+5\overline{P_2}-12\overline{P_4}}{7+10\overline{P_2}+18\overline{P_4}-35\overline{P_2^2}}\right]^{-1} \tag{8.3}$$

$$\overline{P_2} = \frac{\left(3\overline{\cos^2\theta}-1\right)}{2}, \quad \overline{P_4} = \frac{\left(35\overline{\cos^4\theta}-30\overline{\cos^2\theta}+3\right)}{8} \tag{8.4}$$

$\cos\theta = \hat{\mathbf{u}}\cdot\hat{n}$, $\hat{\mathbf{u}}$ is unit vector along molecular axis
and $\hat{n}$ is unit vector along the director of LC ensemble

$$\Phi^L_{mn}(t) = \frac{\left\langle D^{L*}_{mn}(\Omega(t))D^L_{mn}(\Omega(t))\right\rangle}{\left\langle D^{L*}_{mn}(\Omega(0))D^L_{mn}(\Omega(0))\right\rangle} \tag{8.5}$$

$\Omega = (\phi, \theta, \psi)$ is a set of Euler angles.

$$\Phi_{00}^{2}(t)=\Phi_{00}^{2}(\infty)+\left[\Phi_{00}^{2}(0)-\Phi_{00}^{2}(\infty)\right]\exp\left(-\frac{t}{\tau_{00}}\right) \tag{8.6}$$

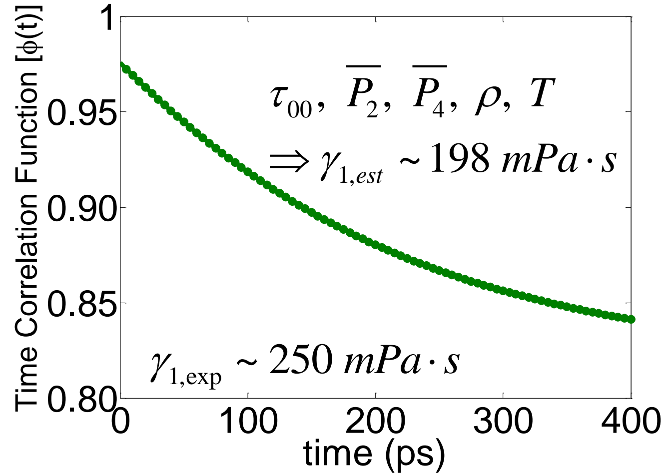

Figure 8.2 Variation of time correlation function with time. Time constant (τ_{00}) obtained from time correlation function is used in calculation of rotational viscosity of LC ensemble.

8.2 Dynamics of CNT-LC Composite under DC Electric Field

In this section, the response of CNT-liquid crystal composites is studied under DC electric field. The equilibrium nematic phase of S = 0.75 and LC director pointed along the x-direction are considered as the initial state of the LC system. DC field of various magnitudes (E^* = 50, 100, 150, 200, 300 in DPD units) is applied along the y-direction to study the effect of externally applied electric field on the reorientation process and to examine associated response time. Figure 8.3 shows the variation of S with time for different values of DC electric field. Figure 8.3a in particular shows the variation of S

with time when there are no CNTs present in the LC ensemble. It is noted that below a certain electric field threshold ($E^* \leq 100$) the order parameter does not change significantly with time. This indicates that the intermolecular pair-wise forces are more dominant than the force exerted by the electric field in this range. At higher E^*, the LC ensemble responds to electric field and loses its anisotropic character gradually as S continues to decreases as time (t) progresses. For $E^* = 300$, the order parameter reaches a minima before it starts rising again as the LC director starts reorienting along the electric field.

Figure 8.3b shows the variation of order parameter S with time for different magnitudes of DC electric field when CNTs are added into LC ensemble with CNTs number concentration of 0.2 %. CNTs are considered to align along the LC director at t = 0. It is found that the threshold electric field magnitude is lowered with the addition of CNTs and LC ensemble responds to electric field much quickly compared to pure LC ensemble case. For E* = 300, the order parameter S even regains its original value at t = 50 nm. The time duration taken by LC ensemble to regain its anisotropy along the electric field direction here is referred to as the response time (τ) of the system. Higher the magnitude of electric field, lower is the response time to regain the original anisotropy. Figure 8.4 shows the schematic of this reorientation process of the system at three different time instants for $E^* = 300$. As mentioned earlier, electric field has to be above critical value to initiate the reorientation of LC system along electric field which is consistent with the experimental observation. [175]

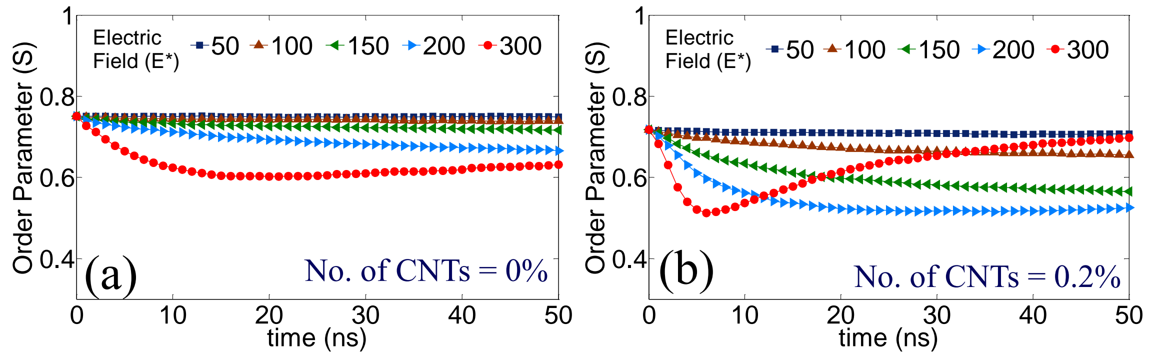

Figure 8.3 Variation of order parameter with time for different magnitudes of DC electric field with CNT concentration of (a) 0 % and (b) 0.2 % in LC ensemble.

Figure 8.5 shows the variation of S with time for varied CNT concentration. Figure 8.5a in particular shows this variation for E* = 50. It is noted that the addition of CNTs in the LC ensemble lowers the equilibrium (*i.e.,* t = 0) value of *S*. By adding 0.8 % CNTs in LC ensemble, the initial value of S is lowered to 0.56 from 0.75 when compared to pure LC ensemble. Figure 8.5a shows the variation of *S* for *E** = 50 which is significantly low electric field. It is noted that addition of CNTs up to 0.4% does not change LC response significantly for *E** = 50. With further increase in CNT concentration causes LC to respond such that order parameter decreases with time which suggests that LC ensemble loses its anisotropic nature. However with increase in electric field (*E** = 300) as shown in Figure 8.5b, the behavior of LC ensemble in the presence of CNTs changes significantly such that the response time decreases swiftly with increasing CNT concentration. For example, LC ensemble not only regains its original value of S but exceeds S = 0.75 within 10 ns at 0.8 % CNT concentration.

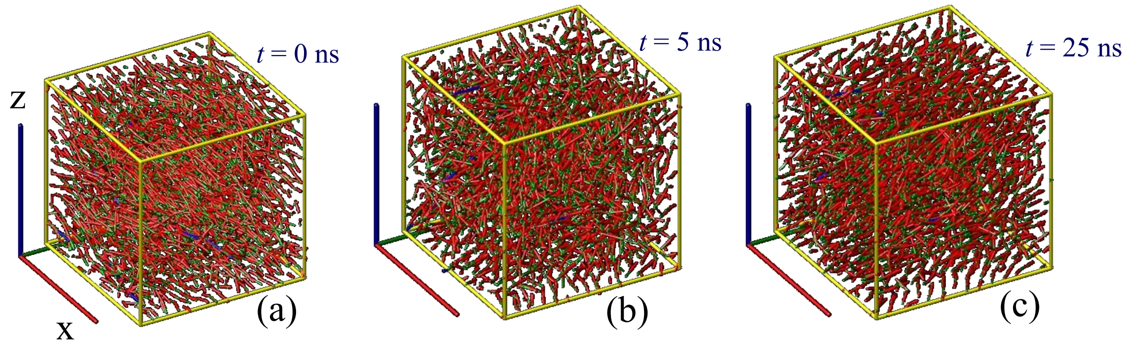

Figure 8.4 Orientation of liquid crystal molecules under electric field (E^* = 300) at different time intervals (a) t = 0, (b) t = 5 ns and, (c) t = 25 ns. Electric field is applied along y-direction.

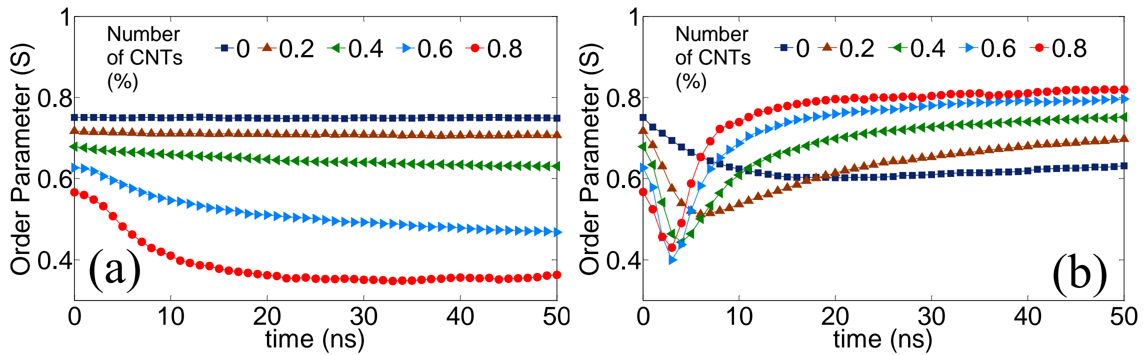

Figure 8.5 Variation of order parameter with time for different concentration of CNTs for DC electric field (a) E* = 50 and (b) E* = 300 applied in y-direction which is perpendicular to the initial LC orientation.

Figure 8.6 shows the distribution of the orientation (cosine of angle between molecular axis and y-direction along which electric field is applied) for E^* = 300 at different time interval with (Figure 8.6a) and without CNT presence (Figure 8.6b). At t = 0, most of the LC molecules are orientated along x-direction. However at t = 25 ns, LC ensemble is almost isotropic when CNTs are not present in the system and it regains its anisotropy at

T = 50 ns when most of the LC molecules are pointing along the electric field direction. With the addition of CNTs (even very minuscule 0.2%) LC ensemble responds much quickly such that system anisotropy is regained at t = 25 ns.

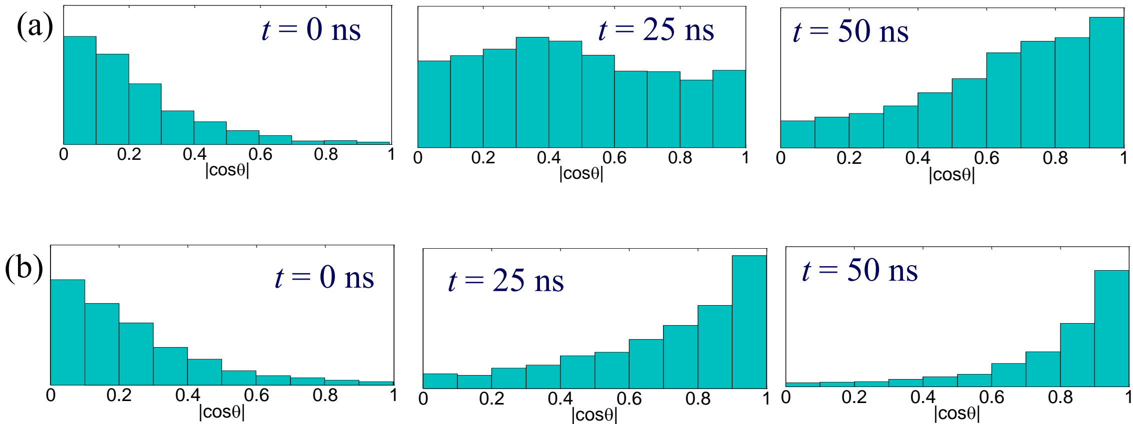

Figure 8.6 Probability distribution of the cosine of angle between liquid crystal molecule's axes and direction of applied external DC electric field (E* = 300) with CNT concentration of (a) 0 % and (b) 0.2 % in LC ensemble.

Figure 8.7a shows that variation of response time with CNT concentration and electric field. It clearly shows that higher CNT concentration in LC ensemble lowers the electric field threshold and accordingly the response time is also lowered. Results show that addition of 0.8% CNTs is equivalent to increasing the electric field 6 folds for equivalent response time of LC ensemble under external DC electric field.

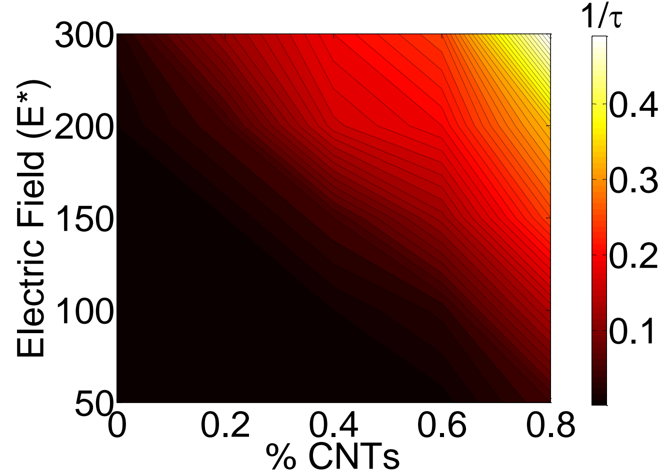

Figure 8.7 Contour plot of response time (τ) of LC ensemble dependence on electric field and CNT concentration. Response time (τ) is defined as the time needed to rotate by 90º to align along the electric field direction.

8.3 Dynamics of CNT-LC Composite under AC Electric Field

Next, the response of LC ensemble under AC field is studied for different amplitudes with varied CNT concentration. The field is specified as $\overrightarrow{E^*} = E_0^* \sin(2\pi t / T)\hat{y}$ where $\hat{y}$ is unit vector along y-axis, E_0^* is the amplitude of electric field, and T is the time period of oscillation. Asterisk (*) symbol indicates that the variables have been normalized with respect to appropriate DPD scales. For the current study, four different amplitudes (E^* = 100, 200, 300, and 400) are employed which are above critical values.

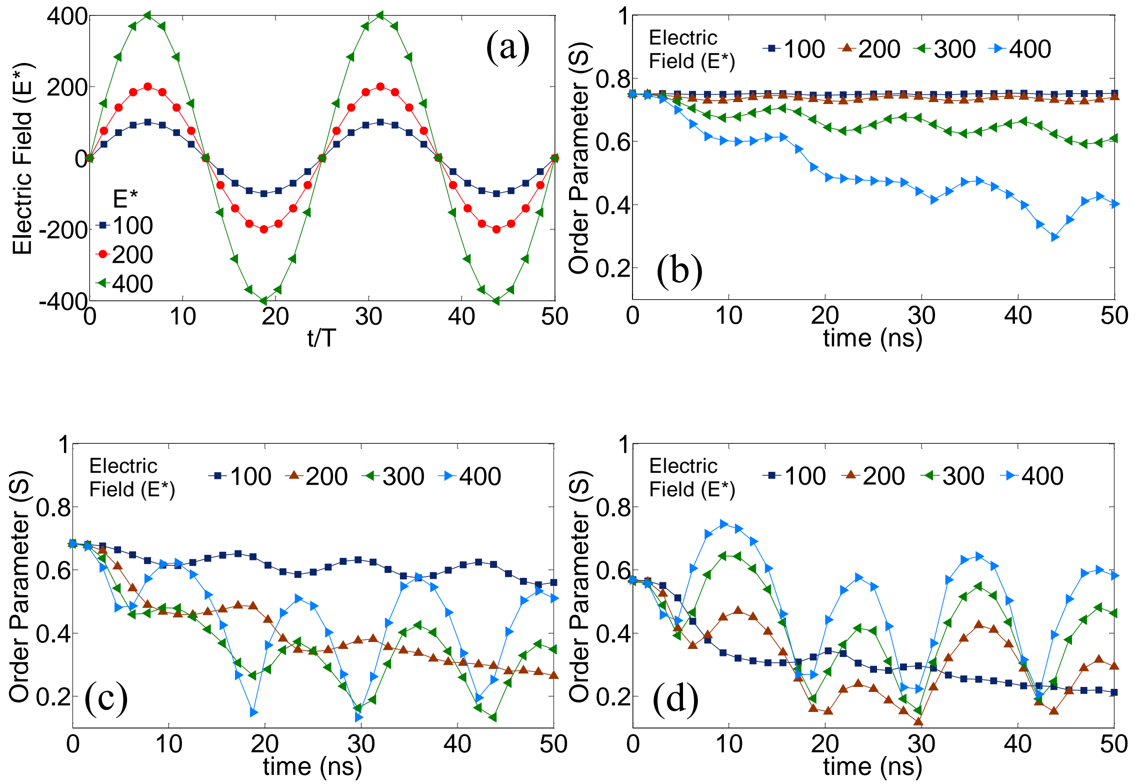

Figure 8.8 (a) Profile of AC electric field with varied amplitude. (b), (c) and (d) show the variation of order parameter with time for varied AC electric field amplitude for CNT concentration of 0%, 0.4% and 0.8% respectively.

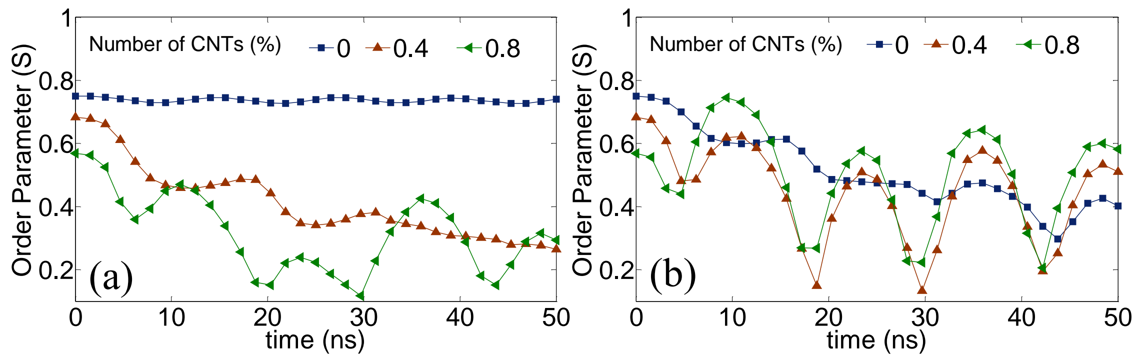

Figure 8.9 Variation of order parameter with time for varied CNT concentration for (a) E* = 200 and (b) E* = 400.

The results for the first two cycles of oscillation of the AC field (Figure 8.8a) are presented with time period of 25 ns. During the cycle electric field varies between +/- E^*, therefore system responds to the field only when field is above the critical value (E^* = 100). Figure 8.8b shows the variation of S with time for varied electric field amplitudes with pure CNT ensemble. For E^* = 100 and 200, there is little change in the value of order parameter S. For E^* = 300 and 400, S oscillates with time as per the AC oscillations of the electric field. However S decreases gradually as time progresses because AC field changes its direction before LC molecules align themselves along the electric field. This contributes to growing isotropy in the system. However the response of the LC ensemble changes when CNTs are added in the system. For example at 0.4 % CNTs concentration (Figure 8.8c), S varies with time in such a way that it follows AC field oscillations with nearly uniform amplitude for initial half a cycle. For lower AC amplitudes, S oscillates but gradually decreases in the amplitude. For 0.8 % CNT concentration (Figure 8.8d) the oscillation amplitudes of S increase with the amplitudes of applied AC field. It should be noted that addition of CNTs (even with small amount) enhances LC response such that lower electric fields are required for a response equivalent to pure LC ensemble response. Figure 8.9, which shows variation of S with time under AC field for varied CNT concentrations, also confirms this observation where addition of CNTs can be seen to assist LC response. Figure 8.9a corresponds to E* = 200 and it is noted that pure LC ensemble hardly responds to the AC field. The addition of CNTs assists the movement of LC molecules but S decreases with time since AC field is not strong enough to sway the molecules along its direction quickly. For E* = 400 (Figure 8.9b), it is noted that simple

addition of 0.4 or 0.8 % CNTs can allow the LC ensemble to follow the electric field with uniform amplitude and the same frequency as the applied field.

8.4 Closure

In summary, a mesoscopic simulation technique, DPD is employed to study the behavior of LC –CNT composites under the application of DC and AC electric fields. DPD being a relatively new technique has not been well explored particularly for studying the dynamic behavior of LC systems and their colloids under electric field. Our analysis suggests that the coarse-grained model of 5-CB can retain most essential features of this LC molecule with rigid backbone and flexible tail. DPD is able to describe relevant physical behavior of LC system both in equilibrium and under electric field. Results are consistent with the experimental observations of rotational viscosity and also for the presence of anisotropic nematic phase at room temperature. This technique is found to be very promising to examine the properties of colloidal liquid crystals however more work is still required to better represent the chemistry between different molecules. For example, in some cases one end of LC molecules may have a greater tendency to get attached to CNT wall due to non-uniform distribution of charges and associated polarity. Such realistic cases need to be taken into account which will also help understand the potential of LC molecules in obtaining highly aligned CNTs.

CHAPTER 9: CONCLUSIONS AND FUTURE WORK

9.1 Summary

In this work, CNT networks and arrays based thin film transistors (TFTs) have been studied using a computational approach. The model is validated against the experimental results. The analysis presented here deals with the issues related to the operational reliability of these devices.

To explore the thermal reliability of CNT network TFTs, power dissipation and CNT network breakdown behavior is examined and correlated with several device parameters. A detailed approach consisting of coupled electro-thermal model of the CN-TFT, molecular dynamics simulations of CNT junctions, and experimental data on power dissipation and temperature contours has been utilized. It is found that the breakdown characteristics remain invariant even if the thermal boundary conductance at CNT junctions increases by two orders of magnitude from its typical value (~ 2.4 pWK^{-1}). On the other hand, one order of magnitude increase in the CNT-substrate thermal boundary conductance from its typical value (~ 0.16 $Wm^{-1}K^{-1}$) can double the breakdown voltage and quadruple maximum power density capability of network. It is noted that the CNT junctions are the likely locations of the hot spots not because of poor CNT-CNT thermal conductance but rather due to the absence of direct contact of buckled part of CNTs with the substrate at crossed CNT junctions. The denser CNT network may adversely affect the device reliability as the higher percentage of CNTs may not be in direct contact with the substrate. The analysis suggests that the CNT network TFT performance can be greatly improved by engineering the CNT-substrate interactions and optimizing the

network density and CNT junctions' topology (e.g., buckling length, structure). It is found that the breakdown characteristics can vary significantly with the channel length, but their dependence on the channel width is relatively very small. The analysis on breakdown behavior of CNT network TFT for various log-normal CNT length distribution and several alignment distributions suggests that the heat dissipation and thermal reliability of CNT network TFTs can be significantly improved by optimizing the network morphology parameters (e.g., semi-aligned longer CNTs).

In case of aligned CNT-TFTs, array density and oxide thickness are varied to study the implication of electrostatic screening and thermal coupling on the current and temperature profiles of CNT TFTs. The results indicate the denser CNT arrays are favorable for both higher On-current and higher On/Off ratio but may also cause serious heat dissipation issues at very high densities. Thinner gate dielectrics increase the On-current in the device but also lead to increase in the temperature due to greater power density. The results provide important guidelines for optimization of gate oxide thickness and array density to improve electrical and thermal performance in aligned array CNT-TFTs. Hysteresis in aligned CNT-TFTs is also studied with focus on the impact of location and density of trap sites, sweep rate of gate voltage, oxide layer thickness and CNT array density. It is found that for interfacial trap charges, change in sweep rate does not cause any change in the hysteresis. However for near interface bulk defects, higher sweep rates leads to larger hysteresis. Also, hysteresis is found to increase with higher oxide thickness and higher CNT array density.

Lastly, a mesoscopic simulation technique, dissipation particle dynamics (DPD), is used to study the behavior of CNT – liquid crystal (LC) colloids under the application of AC and DC electric field. DPD being a relatively new technique has not been well explored particularly for studying the dynamic behavior of LC systems and their colloids under electric field. DPD is able to describe relevant physical behavior of LC system both in equilibrium and under electric field. Results are consistent with the experimental observations of rotational viscosity and also for the presence of anisotropic nematic phase at room temperature. The technique is found to be promising for examining the properties and behavior of CNT - liquid crystal systems under external electric field which can be very useful for many practical applications.

9.2 Future Work

Following are some topics which are open to further research in continuation of the work presented in the current thesis.

9.2.1 Electrical Breakdown in Dense CNT Array TFTs

The as-grown CNTs contain 1:2 ratio of metallic to semiconducting CNTs. Metallic CNTs are detrimental for transistor operation and need to be removed. Electrical breakdown procedure is generally employed in aligned CNT-TFTs to get rid of metallic CNTs. During the electrical breakdown process, high source-to-drain voltage is applied across the channel under Off-state of transistor. Since the electrical conductivity of metallic CNTs is substantially high compared to semiconducting CNTs under Off-state, metallic CNTs carry very high current. High Joule heating in the metallic CNTs causes

them to burn out and be removed effectively from the CNT array. But for high density arrays which are desired for high On-current, selective removal of metallic CNTs will also lead to damage of neighboring semiconducting CNTs. Therefore, the side effects or the collateral damage during the electrical breakdown process on the semiconducting CNTs need to be investigated. A numerical study of the electrical breakdown process can yield useful insights which could be used to minimize the damage of semiconducting CNTs. In nanometer scale transistors where the phonon and electron mean free path is comparable to the channel length, ballistic transport becomes dominant. Therefore, a suitable model for electron- phonon transport in ballistic/quasi-ballistic regime for energy and charge transport needs to be explored and applied.

9.2.2 Modeling of CN-TFTs for Sensor Applications

CNT-TFTs for sensors applications have been explored in various experimental studies. However, very few studies have been focused on the modeling and numerical simulation of these devices. Modeling and simulation can help establish the theoretical framework for the underlying physics during device operations. Insights could further be used to find optimum material properties for fabrication of these devices with improve performance. Governing equations for these devices involves not only charge transport but also the interaction between charges and external perturbation (in the form of either gas molecules or light). Computational approaches are needed to be explored, studied and validated for sensor applications of CN-TFTs.

9.2.3 Analysis of Performance Variation in Aligned CNT-TFTs

In CNT Network TFTs, random network of CNTs are employed which can minimize device to device performance variations as the variations in the electrical properties of individual CNTs and CNT junctions are averaged out in a sufficiently dense percolation network. In case of aligned CNT-TFTs, irregular CNT array pitch, CNT diameters variations (which directly affects the band gap of CNT), impurities at CNT-metal contacts at source/drain (which affect the contact resistance) and a few stray misaligned CNTs in the arrays cause inadvertent performance variations. The performance variations due to each of these factors need to be systematically investigated and examined. This may help identify some of the critical steps during the fabrication process to minimize these variations. Also, efforts are required to devise optimal strategies for designing circuits made of these transistors to deal with these variations.

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