ELECTRO-THERMO-MECHANICAL CHARACTERIZATION OF STRESS DEVELOPMENT IN ALGAN/GAN HEMTS UNDER RF OPERATING CONDITIONS

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CHAPTER 1 INTRODUCTION

1.1 Device Introduction

1.1.1 Device Background and Applications

Gallium nitride (GaN) based high electron mobility transistors (HEMTs) have recently been under intense research and are becoming attractive devices for high-voltage, power, and frequency applications. GaN is a wide band gap (~3.4 eV at room temperature) semiconductor with a high electric breakdown field, good electron mobility, high saturation electron velocity, relatively high thermal conductivity, and is stable at high operating temperatures [1].

Compared to complementary metal-oxide-semiconductors (CMOS) or metal-oxide-semiconductor field-effect transistors (MOSFETs), heterostructure field effect transistors (HFETs) incorporate two materials of different band gaps to create the conduction channel of the device [2, 3] . Due to the high carrier mobility in the channel and the lack of scattering from dopant atoms, these devices are also commonly called high electron mobility transistors (HEMTs). The first HEMT utilized n+AlGaAs and GaAs semiconductors to create the conduction channel of the device. GaN based devices, however, utilize undoped AlGaN and achieve a high critical breakdown field, which is estimated to be 3 MV cm^{-1} [4]; approximately ten times larger than Si and five times that of the GaAs devices, and a high peak electron velocity of 2.7×10^{7} cm s^{-1} [5]. In these devices, implementing either wider or more fingers can increase power density. However, power density doesn't scale linearly due to self-heating and uneven temperature on the fingers [6]. As in all transistors, increasing junction temperature in the HEMT yields a decrease in electron mobility and dissipated power. In addition,

higher junction temperatures are known to cause reliability issues. Under transient operation, however, thermal effects are lessened due to the heating and cooling due to cyclic powering of the device from an ON-state to and OFF-state. Higher saturation currents and transconductance can be achieved in AlGaN/GaN HEMTs under pulsed operation [7]. The device duty cycle, or the percentage a device is in the ON-state in one cycle, will also greatly impact the electrical performance of a device. In their work, Nuttinck demonstrated that reducing the duty cycle from 80% to 1% increased the saturation current from 460 to 580 mA/mm at a bias condition of 40 V_{ds} and 0 V_{gs}. In addition, at the 1% duty cycle, no current "droop" due to device self-heating was observed at 40 V_{ds}.

AlGaN/GaN HEMTs have the potential to greatly impact both the power switch and RF communication applications because of their attractive combination of material properties, especially compared to current state-of-the-art devices (Figure 1).

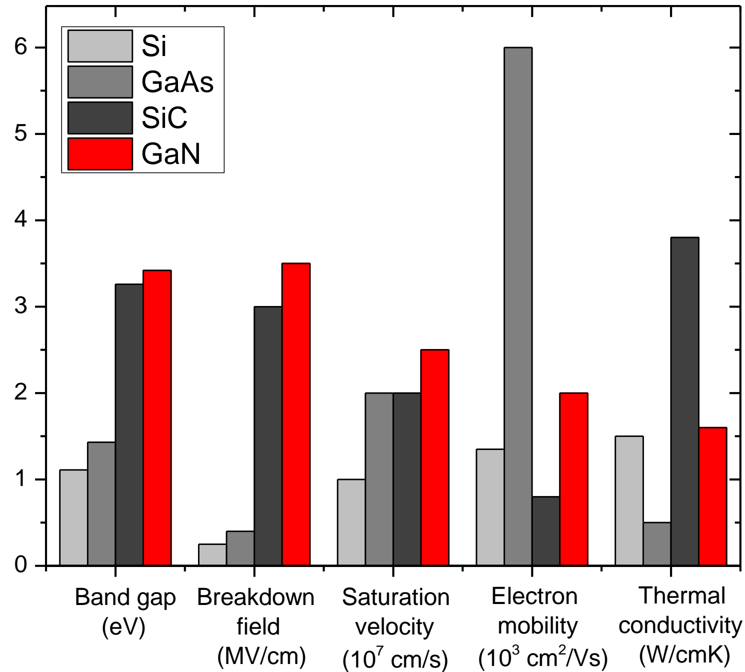

Figure 1. Material properties for existing transistor base materials [8].

Although GaN has a lower maximum electron drift mobility compared to GaAs based devices, GaN has a larger peak electron velocity, larger saturation velocity, higher breakdown voltage, and better thermal stability – all of which contribute to making these devices very suitable for both direct current (DC) and alternating current (AC) power devices [9]. HEMTs have been adopted for many applications that require a transistor with high gate switching frequency or for higher power density applications where high gain and low signal-to-noise are required [10]. Compared to its predecessors, GaN-HEMT technologies exhibit the highest Johnson Figure of Merit (JFoM), which is defined as the product of the cut-off frequency and breakdown voltage as shown in Figure 2 [11]. The JFoM is a measure of the suitability of a semiconductor material for high frequency power transistor applications.

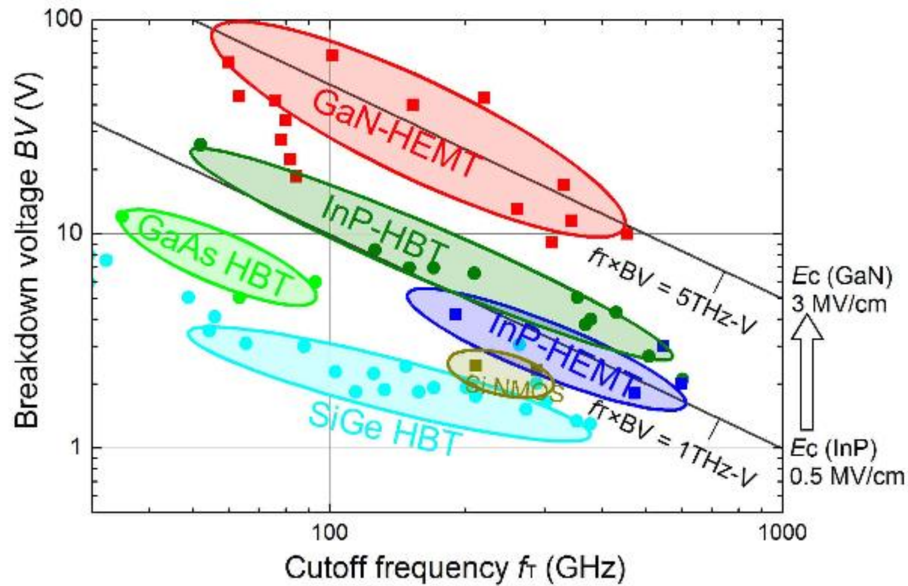

Figure 2. Johnson Figure of Merit (JFoM) of relative HEMT technologies. GaN based devices have a clear advantage in breakdown voltage across a wide range of frequencies [11].

Based on the JFoM in Figure 2, GaN technologies have the potential to be some of the best performing devices for high frequency applications such as advanced radar systems and next generation cellular base towers [12]. Other applications include power

electronic devices to control voltage, current, or frequency characteristics of an electronic circuit. While vertical GaN devices are currently under development, lateral HEMT devices made on low cost Si substrates are poised to impact low voltage applications. In high power applications, SiC substrates are typically utilized due to its high thermal conductivity (~390 $Wm^{-1}K^{-1}$ at 293 K [13]). In addition to power electronics, researchers are also exploring the possibility of utilizing HEMT devices in building DRAM and advanced CPU processors [14].

In all of these applications, the ability to send and receive information is dependent on the power input and efficiency of an RF device. Due to the combination of material properties shown in Figure 1, GaN based devices have the potential to outperform existing technologies in the areas of high power and high frequency applications. Implementing AlGaN/GaN HEMTs in these fields allows for reduction in overall system power consumption and physical size due to their higher efficiency and power density [15].

1.1.2 Device Structure and Fabrication

Figure 3 represents a simplified device structure of an AlGaN/GaN HEMT. Devices are fabricated by first depositing a thin nucleation layer of Aluminum Nitride (AlN) on a substrate layer for epitaxial growth of the subsequent semi-insulating GaN layer. For this thesis, the substrate material used is 6H-SiC, which corresponds to experimental devices. These devices are fabricated using the same process for commercially available devices, but the structure was changed for academic testing and experimentation. SiC offers numerous benefits including high thermal conductivity, and has ~3.5% lattice mismatch with GaN, as shown in Table 1 [16].

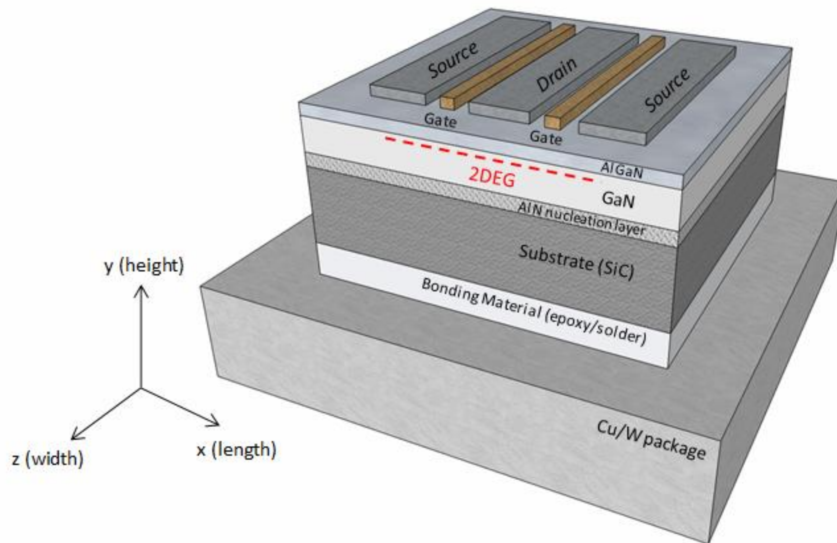

Figure 3. Graphical representation of a 2-Finger AlGaN/GaN HEMT device including substrate and package materials. Packaged devices consist of multiple layer stacks with numerous different length scales.

The AlN nucleation layer provides better adhesion and more uniform, epitaxial growth of the GaN as demonstrated in Figure 4 by Amano *et al.* [17]. The inclusion of the AlN layer ensures a highly uniform, planar film of GaN can be efficiently grown on various substrates, which is crucial for fabricating reliable devices. In addition, the nucleation layer changes the GaN orientation to be Ga- faced, which is important for development of the conducting channel of the device. GaN is typically grown using metalorganic chemical vapor deposition (MOCVD). Flat and dislocation-free layers are important for proper adhesion of other features (such as metal contacts), and prevents interstitial defects, which are known to cause high amounts of thermal resistance in power electronic devices.

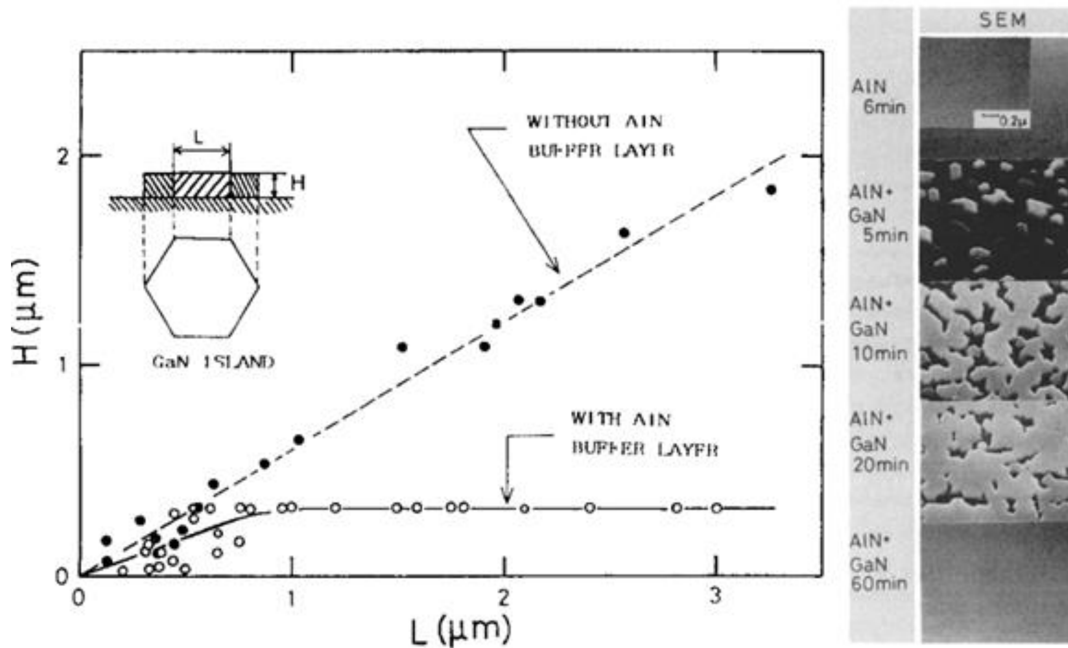

Figure 4. Vertical and Lateral growth of Gallium Nitride islands with and without the inclusion of a nucleation layer. Nucleation layer greatly improves uniform height and lateral growth of the GaN layer [17].

After depositing the GaN layer, a thin layer (usually 20-30 nm) of AlGaN is pseudomorphically grown on top of the GaN layer using either molecular beam epitaxy (MBE) or MOCVD [9, 18]. Unlike preceding AlGaS/GaS HEMTs, AlGaN/GaN heterostructures do not require doping, but rather rely on spontaneous and piezoelectric polarization of the AlGaN and GaN layers to generate free carriers within the device. Various methods of growing the AlGaN and GaN layers exist to control the polarization of the AlGaN and GaN layers and are outlined in Figure 5. Piezoelectric polarization only occurs within a strained layer; spontaneous polarization is an intrinsic property of the material (polarization exists while the material is under zero strain).

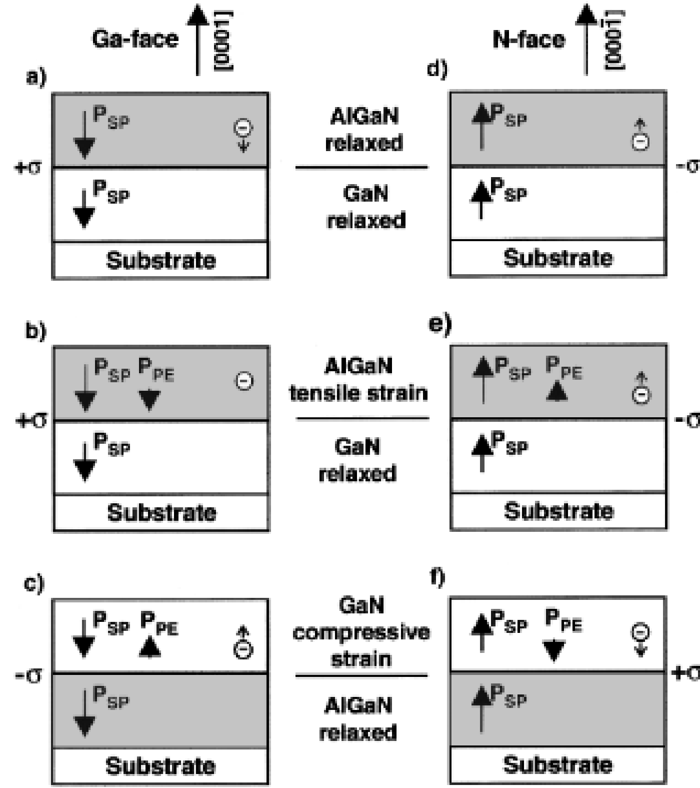

Figure 5. Polarization schemes in AlGaN/GaN HEMTs [9]. Altering growth conditions and substrate material changes the polarization of the AlGaN and GaN layers.

The AlN nucleation layer changes the orientation of the GaN layer, yielding a change to the polar orientation of the AlGaN and GaN. Specifically, the nucleation layer creates a Ga-faced GaN layer with [0001] orientation. In this configuration (which is (b) in Figure 5), AlGaN exhibits both spontaneous and piezoelectric polarization, while the GaN exhibits only spontaneous. For Group III-V materials, which AlGaN and GaN both are, this spontaneous polarization value is very high [9]. The added piezoelectric strain in the AlGaN layer is introduced because of the lattice mismatch between AlGaN and GaN. The pseudomorphic growth of the AlGaN layer stretches the AlGaN lattice constant to that of the GaN layer, inducing large amounts of residual tensile strain. This strain creates the additional piezoelectric polarization and promotes the movement of free carriers to the AlGaN/GaN interface. In fact, this has been demonstrated to be nearly five times larger than the preceding AlGaAs/GaAs devices [9].

Next, the ohmic (source and drain) and Schottky (gate) contacts are deposited. Low-resistance ohmic contacts are crucial to achieve high current densities and high extrinsic gains for thermal stability [19, 20]. Gold (Au) is a common ohmic metal used in microelectronics, but is known to have adhesion and contamination issues in Si fab sites, and can diffuse in III-V based electronic devices [21, 22]. Because of these issues, ohmic contacts are usually made of multiple, thin layer stacks of materials, and then annealed to form a uniform alloy. Ohmic contacts are commonly fabricated with stacks containing Platinum (Pt), Titanium (Ti), copper (Cu), and Gold (Au). Platinum, for example, is a good base material because of its high melting point, which prevents it and other metals from diffusing into the device, and acts as a good adhesion layer for other metals with better electrical properties, such as Au.

Table 1. Lattice structures and constants for GaN and substrate materials.

Material	Crystal structure	Lattice Constant [Å]		Thermal Expansion Coefficient [$10^{-6}K^{-1}$]		Lattice Mismatch [23] [%]	Thermal Conductivity [$Wm^{-1}K^{-1}$]
		a	c	a-axis	c-axis		
GaN	Wurtzite	3.18[24]	5.18[24]	3.9[25]	3.53[25]	0	230
AlN	Wurtzite	3.11[26]	4.98[26]	5.3[27]	4.2[27]	-2.41	285
6H-SiC	Hexagonal	3.08[26]	15.1[26]	4.2[28]	4.6[28]	-3.5	490

Properly designed and fabricated Schottky (gate) structures are crucial for correct electrical device operation. Gate metallizations are commonly deposited in T-gate structures, to reduce the rapidly changing electric field in this region. More information on the device physics and operation of the Schottky contact will be provided in the following section. For this work, the gate is centered between the source and drain ohmic contacts, and the entire device is passivated with Si_3N_4. Although this gate location is not a common configuration, center gate devices have electrical characterization benefits and can be operated in either a forward or reverse bias without a change in performance. Passivating the device protects from moisture and damage, but this layer is also critical

for device performance by greatly reducing dispersion between the large signal AC and DC characteristics of the HEMT device [1, 29, 30].

1.1.3 Device Operating Physics

The electrical current (and thus power) output by a HEMT is a result of the electrical bias conditions placed on the three electrical terminals: source, gate, and drain. Figure 6 outlines the geometry of a device with some representative dimensions labeled [31]. Typically, a voltage is supplied to the drain while the source acts as a ground. The source and drain names come from the fact electrons begin at the source contact, travel through the conducting channel of the device, and exit through the drain [1]. Therefore, directly tying these metallic structures to the conducting channel of the device is critical for proper device operation. Ohmic contacts have a linear current-voltage (I-V) curve in accordance with Ohm's law. Also, current could flow in either direction without current blocking because of rectification or excess power dissipation due to threshold voltages [2].

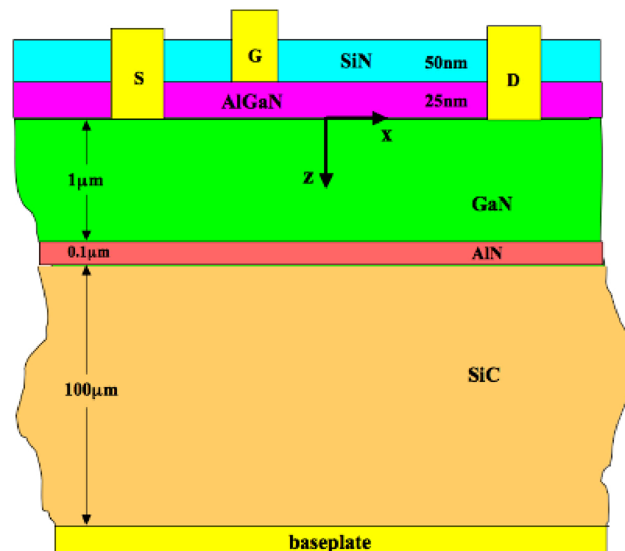

Figure 6. Typical device structure including substrate material (SiC), nucleation layer (AlN), AlGaN/GaN heterostructures layers, metallizations, and SiNx passivation layer [31].

The gate, on the other hand, is a form of non-ohmic contact called a Schottky contact. A Schottky contact is a potential barrier for electrons formed at a metal-semiconductor junction. Like the ohmics, the gate structure is a combination of metals, but is directly deposited on top of the AlGaN layer. The primary characteristic of a Schottky is the height of the potential barrier, Φ_B, and is defined as the difference between the interfacial conduction band E_C and Fermi level E_F. A schematic of the Schottky barrier height is shown in Figure 7. The barrier height reflects the mismatch of the energy position of the majority carrier band edge of the semiconductor and the metal Fermi level across the metal-semiconductor interface [2].

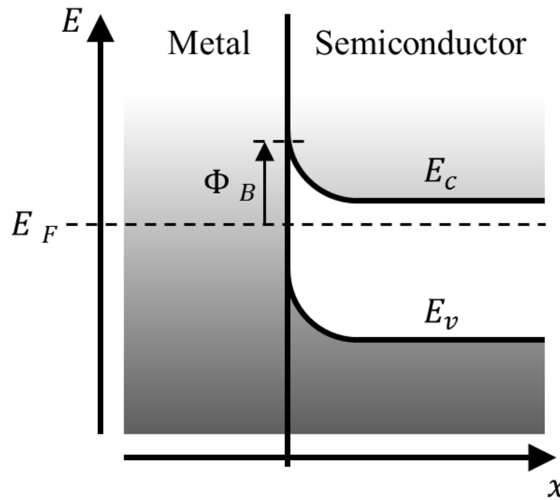

Figure 7. Band diagram and Schottky barrier height representation of a metal-semiconductor interface.

Unlike the ohmics, the gate contact does have rectifying properties, which causes a depletion region of free carriers in the semiconductor around the interface for certain bias conditions. Figure 8 shows the change in the band diagram under reverse (a) and a forward bias (b). Under reverse bias, electrons are blocked from entering the semiconductor because the barrier height is above the Fermi level of the semiconductor. Electrons do not travel up the barrier because of the higher energy state. Similarly, under a forward bias, thermally excited electrons in the semiconductor are able to pass over the

barrier and into the metal. Biasing of the gate contact is important because it controls the conduction channel of the device by modulating the availability of free carriers within the channel. For AlGaN/GaN HEMTs, the gate structure creates depletion regions within the conduction channel to control the amount of power output by the device [2].

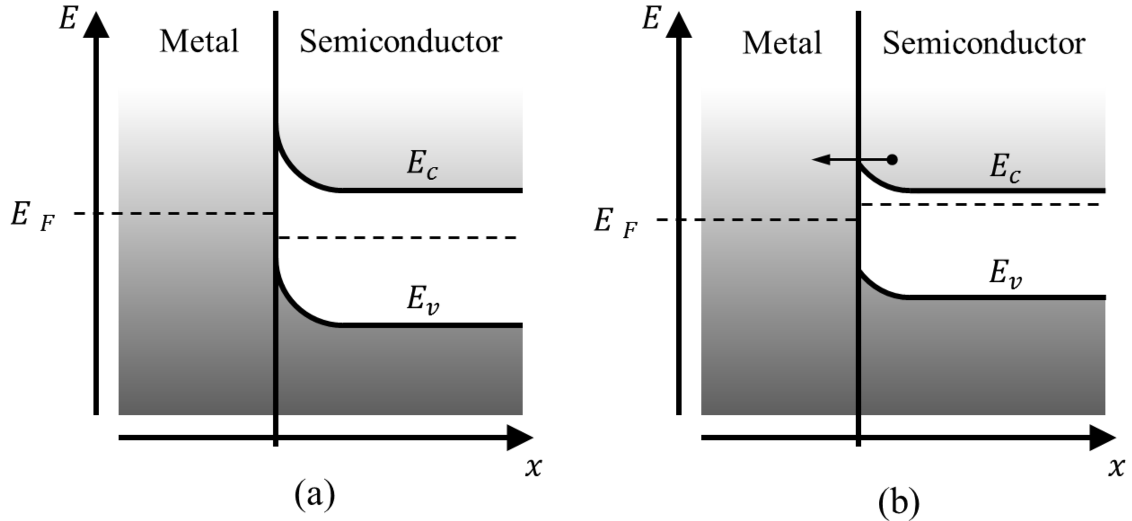

Figure 8. Schottky barrier height shifting under reverse (a) and forward (b) bias.

Quantum physics dictate the exact development and operation of the conducting channel within an AlGaN/GaN HEMT. To compensate for the positive charge, a tightly confined 2 dimensional electron gas (2DEG) develops approximately 80-100 Angstroms (Å) below the AlGaN/GaN interface in the GaN layer, which has a lower bandgap than the AlGaN layer [32]. It has been shown that this phenomenon can cause the 2DEG to have sheet carrier densities in excess of 10^{13} cm^{-2} without intentional doping, which is greatly above traditional Group III-V semiconductors [9]. The conduction of this channel is controlled by the applied drain and gate biases (V_{ds} and V_{gs}, respectively), while the source acts as a ground. When a negative V_{gs} bias is applied, electrons are pushed out of the 2DEG channel and into the buffer (GaN) layer, resulting in the formation of a depletion region and conduction of current within the device is reduced. Further decreasing V_{gs} will completely deplete a section of the 2DEG, yielding a "pinchoff" state

where power is not dissipated by the device. It has been shown that the combination of V_{ds} and V_{gs} greatly impacts the power dissipation, thermal and electrical profiles during operation, and mean time to failure (MTTF) for these devices [33].

1.2 AlGaN/GaN HEMT Reliability Issues

Development and fabrication of AlGaN/GaN HEMTs has significantly advanced in recent years to enable the production of quality military and commercial devices in a wide variety of high power and high frequency applications. To further the development of these devices, however, it is important to investigate the physics associated with the reliability of AlGaN/GaN HEMTs. Several researchers have previously outlined degradation mechanisms within these devices, but the underlying mechanisms for degradation have yet to be fully understood [34-36]. Three factors thought to contribute to the degradation of these devices are the inherent stress/strain due to device fabrication, high thermal gradients under high power operation, and large strain induced by rapidly changing electric fields. Electrical degradation is seen as a rapid increase in the OFF-state gate current at a particular V_{ds}, referred to as the “critical voltage” [37], and through a loss of power added efficiency, change in transconductance, and/or change in gate current noise [37-39]. Above this critical voltage, the onset of degradation is seen in the device. Structural considerations such as the impact of gate length and gate-to-drain spacing have also been demonstrated to influence device degradation [40]. It was found that degradation is largely dependent on the electric field, the critical value for which was calculated to be 1.8 $MVcm^{-1}$. Still further, this degradation effect was demonstrated to have a negative temperature dependence [41]. Under high power operation, both large electric fields and elevated temperatures occur – leading to reduced device reliability and degradation. In addition to the electrical detection of degradation reported in [37],

mechanical degradation has also been observed through AFM and SEM characterization techniques [42]. After stressing beyond the critical voltage, gate structures were removed from devices to reveal cracking around the gate electrode as shown in Figure 9.

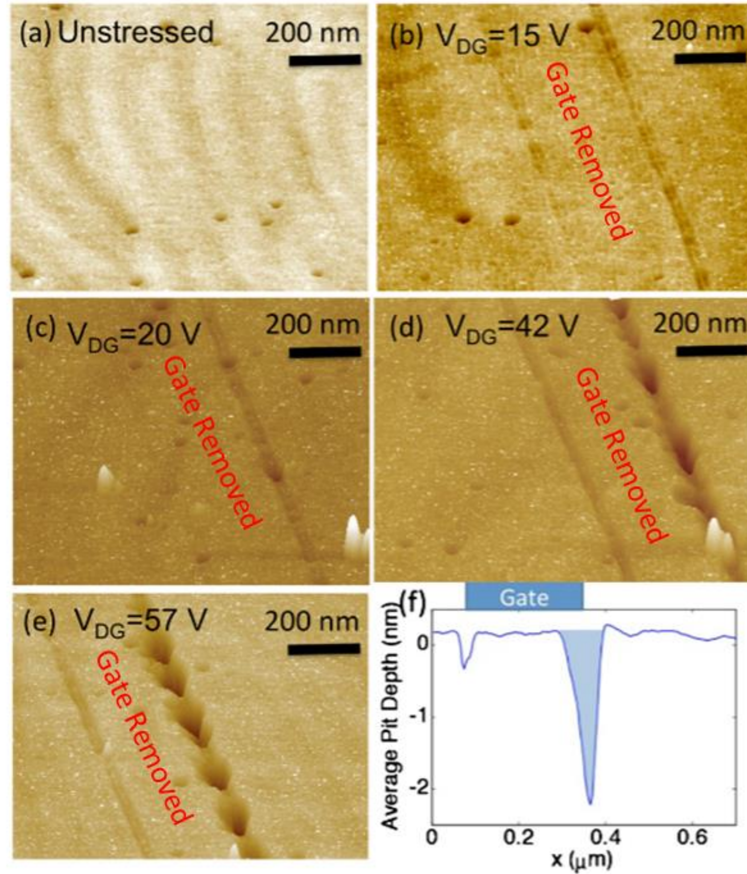

Figure 9. Structural damage observed for devices biased at (a) unstressed, (b) $V_{dg} < V_{crit}$, (c) Vds = V_{crit}, (d) $V_{dg} > V_{crit}$, (e) and $V_{dg} > V_{crit}$, and (f) the average crack profile based on AFM scans [42].

As will be shown in Chapter 3, large amounts of tensile stress develops around the gate footprint on the drain side of the gate. In [42], the device was stressed beyond the critical voltage (V_{crit}) yielding physical, mechanical damage to the device in this area. The authors of [42], however, do not quantify the amount of stress or the heating profile that results from the selected bias conditions. Bias conditions in particular have a large impact on the Joule heating profile, but one researcher reports that it is the total stress, not a single contributor to stress, that can cause degradation [35].

Under transient operation, the combination of electrical bias, frequency, and duty cycle will induce varying amounts of thermal and electrical stress/strain within a device. Moreover, this loading will be applied to devices in a cyclic manner, the details of which have not been studied before for AlGaN/GaN HEMTs. To date, much of the studies of the mechanical effects (stresses) and electric fields in AlGaN/GaN HEMTs published in literature are for devices tested under numerous DC conditions, while the stresses, strains, and temperatures under pulsed or cyclic operation are very different than those seen in previous DC studies. Still further, it is believed that diffusion based electro-chemical effects play an important role in the onset of device degradation [36]. Here, the authors of [36] operated devices under pulsed conditions to determine the filling, emptying, and generation of trap states, especially around the gate edge on the drain side of the device. After pulsing, it was concluded the converse/inverse piezoelectric stress induced by the cyclic loading enhanced the diffusion of oxygen and carbon into the active area of the device, which is known to cause degradation. Exact device degradation physics are unknown and thus properly characterizing the numerous factors that are believed to cause degradation is an important science particularly so in the RF operating regime, where these devices are well suited to operate, but little degradation studies have been performed.

1.2.1 Residual Stress/Strain

Fabrication of GaN based devices requires multiple steps of depositing various materials and annealing to ensure proper adhesion of layer stacks and metallic contacts. Because of this, the devices contain large amounts of intrinsic, or residual, strain due to lattice mismatch and contraction of layers when the device cools from deposition to room temperatures. For example, the pseudomorphic growth induces large amounts of tensile

strain within the AlGaN layer due to lattice mismatch within the GaN layer resulting in stresses in the range of 1-3 GPa in the AlGaN layer [7, 35]. It is because of this strain that the conducting channel of the device has a high current capability, but it also causes reliability issues for these devices. It has also been shown that strain can exists from defects such as dislocations or point defects in a material [43]. Varying process steps greatly impacts the residual strain (or stress) within a fabricated device. GaN in particular is susceptible to deposition conditions and the orientation of the strain is greatly dependent upon the substrate. Davydov et. al. demonstrated that GaN grown on sapphire contains compressive stress [43], while others have shown GaN on 6H-SiC can either be in a compressive or tensile state [44, 45]. Although this same residual strain within the AlGaN layer causes the formation of the 2DEG, and thus creates the majority of free carriers in these devices, device reliability is a concern when additional forms of stress or strain (namely thermoelastic stress due to CTE mismatch and piezoelectric strain due to electric fields) occur during device operation.

1.2.2 Thermoelastic Stress/Strain

High power operation leads to extraordinary operating temperatures for HEMT devices because of high electric fields around or near the conduction channel. Electrons passing through electric fields are accelerated and thus gain energy to become high energy electrons or “hot electrons”. These hot electrons primarily lose energy through the emission longitudinal optical (LO) phonons, which are termed “hot phonons” [46]. Joule heating, however, is primarily carried from an active region by acoustic phonons. LO phonons remain in the active region, until they convert into other vibrations able to transport the Joule heat away (typically into the substrate material). Energy transfer from electrons to acoustic phonons, however, is negligible in a high electric field. It has been

demonstrated that the hot-phonon lifetime (~350 fs) is much longer than LO-phonon emission (~10 fs), leading to an accumulation of hot phonons [47].

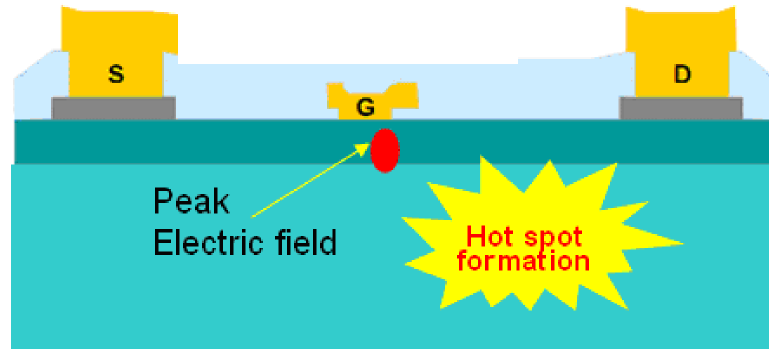

Figure 10. Device schematic with peak electric field location and hotspot formation outlined. Large electric fields create excited or "hot" electrons that cannot effectively dissipate energy to the surrounding lattice [8].

Because the peak electric field is highly localized, LO phonons are generated in a localized area within the device, causing large thermal gradients to develop. Both temperature gradients and CTE mismatch of materials generate thermal stress, which can cause premature device failure. Around the gate structure, where the Joule heating is most prominent, four materials of varying CTE intersect and cause complex stress profiles during device operation. Although researchers have demonstrated power densities in the range of 30 Wmm^{-1} [48], operation in this regime causes high operating temperatures and thus decreased electrical performance and overall reliability. Electrical performance degradation is seen as a drop in output current [49], caused by a reduction in electron mobility and drift velocity due to increase of scattering by thermally excited electrons. Because of these issues, proper thermal management is key for reliable electrical performance and is necessary to increase device mean time to failure (MTTF).

1.2.3 Electrical Stress/Strain

Because AlGaN and GaN are piezoelectric materials, application of an electric field will cause the lattice of both materials to deform. This is known as the inverse piezoelectric effect, or IPE. Under normal operation, large electric field gradients develop between the gate and drain electrodes in AlGaN/GaN HEMTs. More precisely, the peak of this electric field is known to develop at the drain side of the gate footprint. This is because the semiconductor materials' (AlGaN and GaN) electrostatic potential rapidly drops from the applied drain bias to the gate bias in this region. In turn, this generates large amounts of inverse piezoelectric strain due to the large electric field in this region.

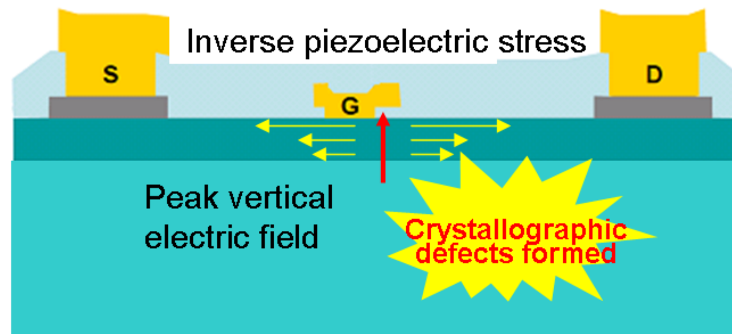

Figure 11. High electric fields yield a large inverse piezoelectric stress effect within AlGaN and GaN leading to the formation of material defects [8].

For low bias conditions (V_{ds} ~ 5 V for the device from [46]), the lateral electric field between the gate and drain is relatively small, with the exception of the large spike under the drain edge of the gate electrode. Under higher voltage bias (V_{ds} ~ 40 V [46]), the relative electric field between the source and gate is unchanged, but the electrostatic potential difference between the gate and drain has significantly increased. Here, the high field region is no longer confined to under the gate, but rather extends in the channel towards the drain. Strains induced by these electric fields can result in device

degradation through the formation of defects known as trap states near the gate in the AlGaN layer [38] (Figure 11). Trap states have been shown to cause the formation of "hot spots" on devices and can trap free carriers, reducing the electrical performance of the device.

Large electric fields and coefficient of thermal expansion (CTE) mismatch of materials can lead to electrical degradation (such as the onset of gate leakage in the device, loss of power added efficiency, current collapse, change in transconductance, and gate current noise) and physical, mechanical degradation (such as cracking or pitting of devices around the edges of the gate contact) [37-39, 50, 51]. Reducing the lateral and vertical spike in electric field is possible through the inclusion of a gate connected field plate (GCFP) as shown in Figure 11, or a source connected field plate (SCFP), which extends from the source over the top of the gate structure. In both cases, the extended metallizations aid in spreading the depletion region of the 2DEG, causing a more gradual change in electric field between the gate and drain contacts.

1.3 AlGaN/GaN HEMT Previous Modeling Review

1.3.1 Existing Modeling Techniques, Results, and Limitations

Vast amounts of numerical and experimental research has already been performed on AlGaN/GaN HEMTs. Early modeling techniques considered only the thermal aspects of large, multi-finger devices with assumed heat generation shapes and locations [52]. Although the authors assumed a heat generation area directly under the gate, their work demonstrates the extremely localized heating as you approach the gate fingers, leading to large temperature gradients from finger-to-finger, in addition to the peak temperature based upon finger location. In addition, gate fingers at the edge of the device, compared

to central locations, experience lower peak temperatures. Their developed model was capable of varying the source-to-drain spacing to create more uniform temperature distribution across a device, but this is not necessarily practical to manufacture. In doing so, however, a 17 ºC reduction in gate temperature was calculated.

Because of these findings, additional thermal research was performed to investigate the effectiveness of active cooling techniques applied to AlGaN/GaN HEMTs [51]. Specifically, μ-channel cooling was incorporated to determine the effectiveness of removing heat, and thus lower the peak temperatures seen around the gate electrode. Various combinations of μ-channel configurations and substrate materials are considered. This work also incorporates the thermal stress effects, since including μ-channels can greatly impact the operating stress due to (respectively) fabrication and large temperature gradients during powering of the device. From their work, one can determine the impact of input power and substrate/channel configuration to minimize either residual or operating stresses, or peak temperature. They find the lowest residual stress to occur when an AlN μ-channel is used. This is because of the good lattice match between the GaN and AlN layers, but higher operating stresses rise due to the lower thermal conductivity of AlN. The best thermal performance was achieved using diamond heat spreaders with silicon μ-channels, but large tensile stresses within the SiC die substrate, and the feasibility of this design is a concern because of the complex fabrication steps.

Although these works present detailed studies of the operating temperatures and resulting stresses within AlGaN/GaN HEMTs, their work is solely based on the thermal response of the devices. Thermal gradients are crucial for electronic device reliability, but the electrical stress failure mechanisms can also lead to device degradation [39, 51]. As previously mentioned, the electrical stress due to the inverse piezoelectric effect can cause the formation of crystallographic-defects. Dr. Jesús del Alamo demonstrated a critical voltage (based on the drain-to-gate voltage), beyond which device degradation is seen and is thought to be independent of thermal effects within AlGaN/GaN HEMTs.

From a modeling standpoint, then, incorporating the electrical effects is critical to be able to confidently predict stress profiles (or failure mechanisms) within these devices. Researchers have demonstrated the electro-thermal coupling and device structure can greatly impact device operating temperatures [33, 53, 54]. In particular, the heating within the device is directly dependent upon the applied bias conditions (V_{ds} and V_{gs}). Neither of these works, however, incorporated the resulting stress profiles as a function of this electro-thermal coupling. It has been demonstrated to be of great importance by researchers [31] and [35] to properly account for the electro-thermal and mechanical response of these devices. In their work, these researchers demonstrate a fully coupled continuum model capable of determining the electrical and thermal profiles within a device and the resulting stresses. Their work demonstrates the capabilities of a fully coupled model, including the electrical performance (such as electron mobility) as being negatively dependent on the operating temperature. This work is of great significance, since previous studies were limited by only electrical or thermal characterization, whereas now the two are coupled and directly impact the stress profiles within the device, particularly in critical regions such as the gate-edge.

Although temperature, stress, and strain profiles have been extensively studied using numerical multi-physics coupled simulations [31, 35, 53] and experimentally during DC electrical testing [38, 49], few have studied the transient stress development or the impact of transient operating conditions even though these devices have numerous applications in the RF regime [55]. This is an extremely important field of study, since these devices are well suited for high frequency operation. Of those who have studied transient analysis for AlGaN/GaN HEMTs, most have only focused on the thermal aspects [56], neglecting the electrical and mechanical response of the devices. Although the operating temperature is important to characterize, it is just a single part of the overall contribution to device degradation. Similarly, detailed studies have been presented that focus on the transient electrical properties and resulting thermal resistances of these

devices [57]. Still other transient studies were developed to give insight to complex device physics such as the formation of surface and bulk trap states [58]. None of these works, however, have a single, combined multi-physical model to correlate the impact of bias conditions, duty cycle, and operating frequency to the resulting stress/strain within the device, nor to the impact on device reliability.

1.3.2 Current Work Motivation and Objective

Understanding the failure modes under transient operation of devices requires a detailed study of the transient stress profiles within an AlGaN/GaN HEMT. Thus, it is important to determine the development of stress during cyclic operation from a powered ON-state where heating occurs, and an OFF-state where no power is dissipated and the device cools. In addition, because of the wide operation range of for these devices, the impact bias condition, frequency, and duty cycle will have on the stress states within the device must also be studied. Therefore, the primary motivation of this work is to detail the development of stress under RF operating conditions. This will include a detailed analysis of how stress changes at various locations including the "critical region" which is localized around the gate footprint on the drain side, as well as areas that can be probed experimentally which is outside of the gate connected field plate (GCFP) on the drain side. Once this is accomplished, a further parametric study on the impact bias condition, duty cycle, and frequency will have on the overall stress profiles. It will be shown that the combination of the three will greatly change the stress profiles within a device, the results of which could be used as guidelines to improve device MTTF.

In this work, Chapter 2 will outline the modeling technique and highlight a few of the previous research initiatives that this work builds upon. First, a small-scale electro-thermal model using Synopsys' Sentaurus Device is presented to characterize the

localized coupling between the electrical and thermal aspects of the device. Due to the computational intensity associated with semiconductor device physics only the channel of the device and a small portion (~10 μm) of the substrate is included. This model will be validated through the quantitative comparison of electrical data (I-V curves) to actual device values. In addition, a qualitative comparison to research available in the literature will be presented as further validation. The resulting heat generation and electrostatic potential data will then be coupled to a large-scale COMSOL Multiphysics structural mechanics model. This model will include full device geometry, including the often neglected AlGaN layer and a full 100 μm substrate of 6H-SiC. This approach to modeling allows for the decoupling of the thermal and piezoelectric stress and strain profiles as demonstrated in [35]. In doing so, the magnitude and distribution of stress present in a device while under cyclic bias conditions is revealed. This method allows transient components (from near gate edge thermo-elastic, inverse piezoelectric) to be convincingly separated from and measured independently of the steady-state contributions (from steady-state temperature rise and temperature gradients, pseudomorphic growth, and built-in process stress).

Once the modeling technique has been described, the transient development of stress will be determined in Chapter 3. This will show how the stress state in a device develops when the device is operated from an OFF-state, where no power is dissipated by the device, to an ON-state, where the applied drain and gate voltages generate complex transient stress profiles. In particular, the peak stress due to the IPE (caused by electric fields) location shifts rapidly during the transition from OFF- to ON-state and *remains constant* throughout the ON-state, while the contribution due to thermal stress (caused by CTE mismatch and large temperature gradients) builds throughout the ON-state. Various positions within the device will be highlighted to show the large stress gradients that develop around critical regions of the device, while other areas undergo stress relaxation

due to an offset of tensile stress due to the IPE and compressive stress states due to thermal effects – resulting in a lower stress state.

From here, a detailed parametric study of the impact bias condition, frequency, and duty cycle will be presented in Chapter 4. This information is important to determine the stress at the same critical regions detailed in Chapter 3, but over a broad range of possible operating conditions. It will be shown how bias condition impacts both the IPE and thermal stress values, while frequency and duty cycle affect only the thermal component of stress. Understanding how these three components affect the overall stress state will allow the selection of appropriate operating conditions to improve device reliability, and will aid in the understanding of how and why devices fail under transient operations.

Next, Chapter 5 will present a comparison between the transient mechanics model and experimental measurements performed by Matthew Rosenberger and Dr. William King from the University of Illinois at Urbana-Champaign. Their work involves characterizing the vertical displacement of devices running under sinusoidal RF inputs using Atomic Force Microscopy (AFM) measurements. This goal is to highlight localized defects on a device, or possibly detect the onset of mechanical degradation within a device through the measurement of vertical displacement. The developed model can aid in understanding the various contributions to the vertical displacement profiles, including bias condition and frequency that experimental techniques along cannot distinguish. In addition, this additional comparison to experimental measurements gives confidence to the developed models accuracy, and further proves its use as a design tool for AlGaN/GaN HEMTs.

CHAPTER 2 COMBINED ELECTRO-THERMO-MECHANICAL MODELING TECHNIQUE

2.1 Electro-Thermal Modeling

With many competing stress effects in an AlGaN/GaN HEMT, it is critical to be able to separate and distinguish the various contributions to stress, so as to be able to understand the physics of failure within the device. In order to properly account for the device physics including bias dependent mobility and Joule heating profiles, a small-scale electro-thermal model is needed to account for the near-gate electric field and resulting heat generation profiles. Great care was taken to match the geometry of actual devices including ohmic contact lengths and heights, spacing between the source, gate, and drain metal contacts, and (perhaps most importantly) the cross-sectional shape of the Schottky (or gate) contact itself.

2.1.1 Sentaurus Device Introduction and Background

A complete finite element model of AlGaN/GaN HEMTs requires accounting for the electrical, thermal, and mechanical characteristics of the device. Heller *et al.* presented a self-consistent electro-thermo-mechanical model capable of accounting for the impact bias conditions have on the self-heating within the device (Figure 12) [33, 54, 59]. Here, several bias conditions of equal total power dissipation (10 W) are compared to demonstrate the impact on the self-heating within the device. In their work, the model dimensions were built around TEM cross-sectional images of an actual device for experimental comparison. In addition, temperature-dependent thermal conductivities and

heat capacities were used for material properties wherever possible. To properly account for the impact of self-heating on the mobility of electrons and holes in the device, temperature- and mole-fraction-dependent semiconductor band gaps and ohmic contact resistances, dielectric constants, effective masses of electrons and holes, and hot electron relaxation times were employed [54].

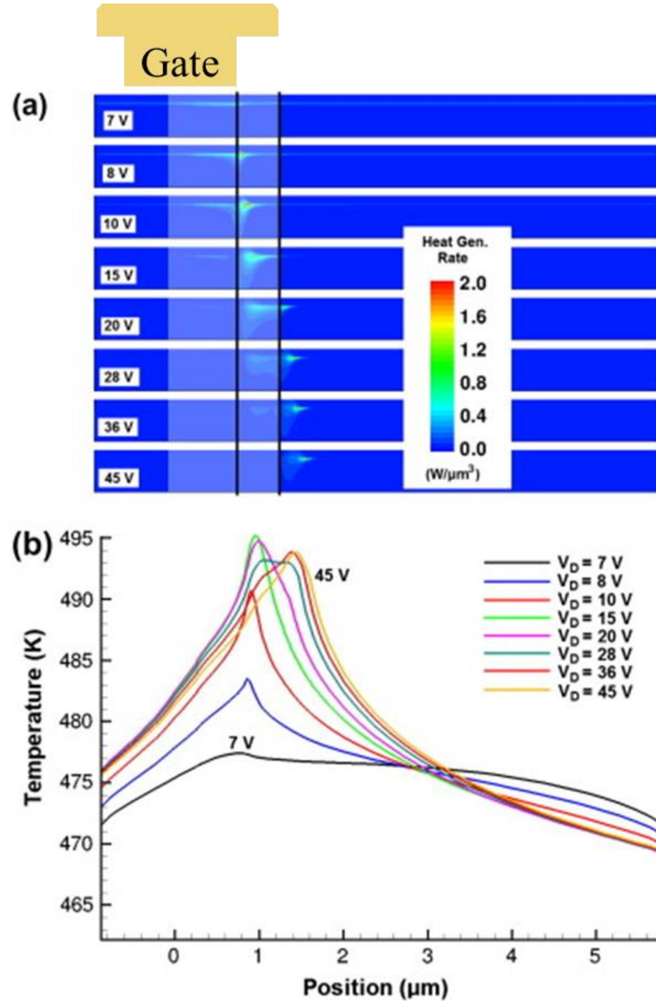

Figure 12. Bias dependence of the Joule heating profile (a) and the resulting temperature profile along the AlGaN/GaN interface (b) [33].

In Figure 12a, the left vertical black line represents the position of the gate footprint point (GFP), and the right line denotes the position of the gate connected field plate (GCFP) edge (a representative gate geometry is added to the top of the Figure for clarity). With

reference to this image, the drain electrode is located to the right hand side of both of these lines. Although it is known that the “hot-spot” is generated near the gate footprint on the drain side, as the drain bias (V_{ds}) is increased the majority of the heat generation region (and thus peak temperature) shifts towards the drain ohmic contact. This is because the majority of the voltage drop (highest changing electric field) occurs in this location between the gate and drain. At high drain bias (45 V_{ds} was the largest drain bias for this work), the heat generation is outside the GCFP, and the bulk of which is located in the channel. Based on these results accounting for the heat generation, as a function of the combined gate and drain bias conditions is key for properly characterizing the stress due to the thermal profile, since the heating profile can greatly change based on the applied electrical bias. Properly accounting for the bias condition also impacts the electrical stress. Since AlGaN and GaN are piezoelectric materials, higher electric fields due to larger applied bias will induce more strain in piezoelectric materials due to the inverse piezoelectric effect (IPE).

In this thesis, Sentaurus Device by Synopsys was used to study the impact of various bias conditions on the electrical and thermal characteristics of AlGaN/GaN HEMTs on silicon carbide (6H-SiC) substrates. This is a commercially available software capable of coupling the electron and hole transport equations with the thermodynamic model for the current densities and lattice temperature within a semiconductor device. In doing so, one can accurately model the electrical distribution and heating profile within a device for different bias conditions (combination of V_{ds}, V_{gs} and V_s). The drift diffusion model for carrier transport invoked by Sentaurus Device [60] for the electron and hole densities are given by

$$\overrightarrow{J_n} = \mu_n(n\nabla E_C - 1.5nkT\nabla \ln m_n) + D_n(\nabla n - n\nabla \ln\gamma_n) \quad (1)$$

$$\overrightarrow{J_p} = \mu_p\left(p\nabla E_V - 1.5pkT\nabla \ln m_p\right) + D_p(\nabla p - p\nabla \ln\gamma_p) \quad (2)$$

Where μ is the mobility, n and p are the electron and hole densities, E_C and E_V are the conduction and valence band energies, k is Boltzmann's constant, T is lattice temperature, m is the density-of-states mass, D is the diffusivity, and γ is a degeneracy factor for modeling. In this equation, the first term accounts for the contribution due to the spatial variations of the electrostatic potential, the electron affinity, and the band gap. The remaining terms take into account the contribution due to the gradient of concentration, and the spatial variation of the effective masses m_n and m_p. Further, the lattice temperature of the device is calculated through

$$\frac{\partial}{\partial t} c_L T - \nabla \cdot k = -\nabla \cdot \left[(P_n T + \Phi_n)\overrightarrow{J_n} + \left(P_p T + \Phi_p\right)\overrightarrow{J_p} \right] - \left(E_C + \frac{3}{2}kT\right)\nabla \cdot \overrightarrow{J_n} - \left(E_V + \frac{3}{2}kT\right)\nabla \cdot \overrightarrow{J_p} + qR_{net}(E_C - E_V + 3kT) + h\omega G^{opt} \quad (3)$$

Where k is the thermal conductivity, c_L is the lattice heat capacity, E_C and E_V are the conduction and valence band energies, respectively, G^{opt} is the optical generation rate from photons with frequency ω, R_{net} is the recombination rate, P is the thermoelectric power, and Φ is the Fermi potential. Compared to traditional modeling techniques that characterize only the Fourier-based diffusion of heat transfer in a device, this method of modeling semiconductor devices calculates more accurate temperature and electrical profiles, which is especially crucial around the gate where large electrical and temperature gradients are seen. The ability to couple the electrical and thermal aspects of an AlGaN/GaN HEMT allows one to accurately model semiconductor devices to improve overall design through the understanding of the thermal and electrical response to different bias conditions.

2.1.2 Small Scale Electro-Thermal Model Structure

Care was taken to construct an accurate model representation of an actual device including overall device dimensions and metallization structure. Figure 13 shows an optical image of a test device for characterization.

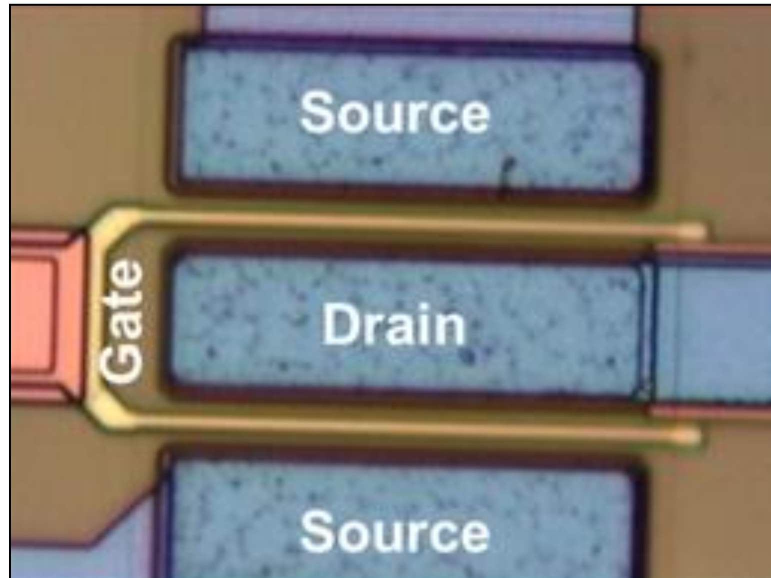

Figure 13. Experimental device consisting of two-finger centered gates. Developed electro-thermal and electro-thermo-mechanical model was built around this device geometry.

These devices contain two-finger gates that are centered between the source and drain contacts. The devices are mounted on a SiC substrate and are passivated with Si_3N_4. Scanning electron microscope images (SEM) were also provided of the source, gate, and drain structure and dimensions, which were used to build the representative model geometry.

A two-dimensional model was constructed using Sentaurus Device to simulate the electrical and thermal characteristics of an $Al_xGa_{1-x}N$/GaN HEMT. From reviewing literature, the mole fraction of aluminum is assumed to be $x = 0.26$ [9]. The AlGaN and GaN heights are taken to be 20 nm and 1.8 µm, respectively, [52, 61]. The overall shape of the model is adapted from that described in [54] and includes 20 µm wide AlGaN and

GaN layers. Darwish demonstrated heat radiating from the localized "hot spot" region forms isothermal contours that are nearly circular [62]. Because of this, the SiC substrate is modeled as the bottom half of an irregular, multifaced polygon centered on the gate electrode, which is consistent with [54]. This layer extends radially from the base of the GaN layer by ~10 μm, which is considerably larger than the heat generation region of the device. An irregular polygon is chosen for the SiC instead of a half-circle for meshing purposes. That is, meshing straight lines and corners with obtuse angles yields a higher quality mesh and gains in computational efficiency over a semi-circular domain while being a good approximation for the entire system. Special attention was given to the channel dimensions: drain-to-source (L_{DS}), source-to-gate (L_{SG}), and drain-to-gate (L_{DG}) lateral spacing. These dimensions were extracted from the optical images of the device shown in Figure 13. The gate length (L_G) is taken to be 0.5 μm [35]. Figure 14 graphically represents the channel spacing for the device.

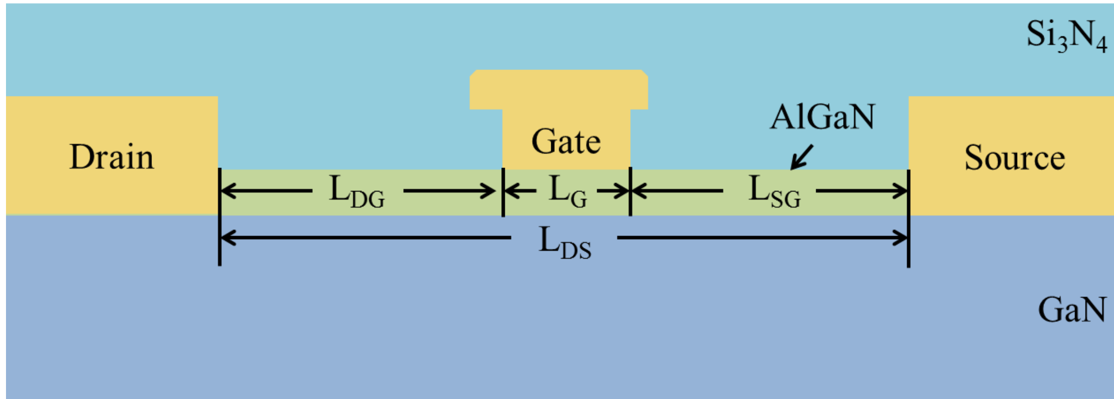

Figure 14. Channel geometry for the experimental devices shown in Figure 13. Dimensions and metallization structures are adapted from SEM images of experimental devices (not shown).

Electrical boundary conditions (or electrical contacts) are defined on the perimeter of the source, gate, and drain regions to simulate the electrical contact points for the device. The material within these regions is modeled as gold [54], except for the 20 nm inclusion of nickel below the gate structure. In addition, a thermal boundary condition of 300 K was imposed on the bottom edges of the SiC substrate layer. Such a condition is

not physically realistic, but because of the intense computational requirements for the simulation, just the area of interest (i.e. the device channel) is modeled fully. To better account for the full structure, a surface thermal resistance term of 0.002 cm^2KW^{-1} was added to the temperature boundary on these edges. In doing this, the heating effects on electrical properties can be accounted for without modeling the entire device structure. This parameter was determined through fitting of DC I_{ds}-V_{ds} curves (Figure 22), where this value was adjusted to aid in matching the current "droop" due to Joule heating within the device. In addition, mobility values for AlGaN and GaN layers were provided from Low-Field Hall measurements, described in [54].

As previously mentioned, the 2DEG of an actual device develops ~80-100 Angstroms (Å) below the AlGaN/GaN interface [32]. However, this model follows other simulations from literature where the 2DEG is modeled as a fixed, uniformly-distributed, and electric-field-independent surface charge density at the AlGaN/GaN interface [33, 54, 63]. This value represents the combined spontaneous and piezoelectric polarization induced charge at the AlGaN/GaN heterojunction interface, and is calculated using the assumed mole fraction from an interpolation of results from Ambacher *et al.* to be 2.0 x 10^{-6} C/cm^2 [9]. Model parameters such as Al- mole fraction, layer thickness, and inclusion of impurities directly affects this value, but it will be shown that good agreement in electrical behavior of the modeled and experimental device was achieved, giving confidence to the 2DEG assumption, model parameters, and imposed boundary conditions.

2.2 Combined Electro-Thermo-Mechanical Model

2.2.1 COMSOL Multiphysics Introduction and Background

Although the constructed Sentaurus Device model can accurately model the electrical and thermal characteristics of the device, the developed model does not have the ability to determine the mechanical response of the device, i.e. stress and strain profiles. Ancona *et al.* demonstrates the importance of accounting for the various stress profiles in a multidimensional continuum thermo-electro-mechanical model and discusses possible degradation mechanisms in the device including electron injection, IPE, thermal stress, intrinsic (residual) stress within the device, and the impact of device geometry [31]. Similar to Heller, their model incorporates multi-physics coupling between the drift-diffusion of electrons and holes, with the device operating temperature and electrical performance. Their results show an extremely focused area around the drain side of the gate edge for stress, as shown in Figure 15. In addition to demonstrating a peak in stress around the gate electrode, these results also demonstrate the complex stress profile of a HEMT device during operation. Away from the gate, for example, stresses are largely compressive in the GaN layer, instead of tensile. Using the developed model, the authors are able to determine design improvements for AlGaN/GaN HEMTs such as changing the gate shape and material composition to study the change in stress profiles, and thus the reliability of the device.

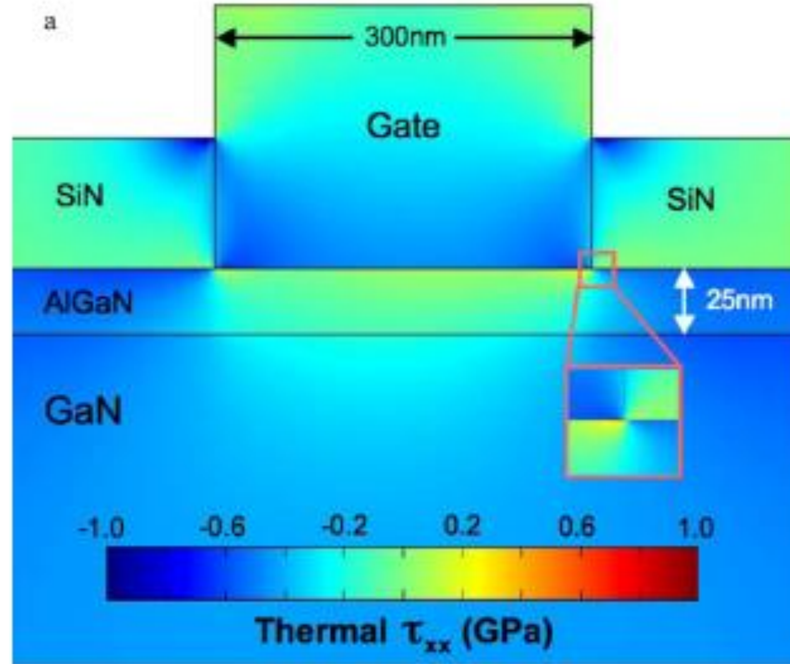

Figure 15. Thermal stress due to temperature gradients and CTE mismatch. At the highlighted point, three materials of varying CTE intersect, causing a localized stress point with high stress gradients [31].

Based on these results, it is clear a properly formulated mechanics model is critical to understanding AlGaN/GaN HEMTs under transient operation. Therefore, COMSOL Multiphysics is used to analyze the mechanical response of a device subjected to the spatial heat generation and electrostatic potential values calculated by the Sentaurus Device model. Within COMSOL, the thermal and electrical physics can be decoupled to determine the impact each have on stress and strain within the device, or superimposed to determine the combined stress profile. In COMSOL, the lattice temperature is determined by:

$$\rho C_p \frac{\partial T}{\partial t} + \rho C_p \boldsymbol{u} \cdot \nabla T = \nabla \cdot (k \nabla T) + Q \tag{4}$$

Where ρ is the density, $C_p$is the heat capacity, T is lattice temperature, and k is the thermal conductivity. The final term Q is the heat generation value, and is the parameter

taken from the Sentaurs model as input to the thermal mechanics model. The second term, $\rho C_p \boldsymbol{u} \cdot \nabla T$, accounts for a moving heat source where $\boldsymbol{u}$ is a velocity field. In this simulation, the lattice temperature is directly determined by the heat generation calculated within the Sentaurus Device model. A flow of the modeling technique is shown in Figure 16.

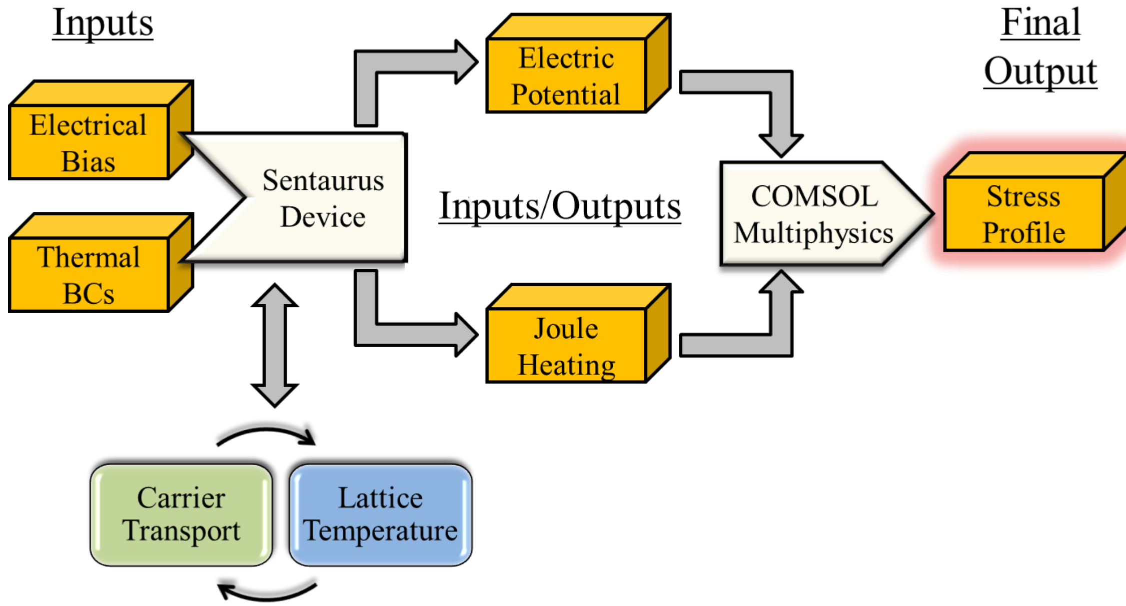

Figure 16. Coupled Sentaurus Device and COMSOL Multiphysics modeling technique.

For the thermal effects, the Thermal Stress module is invoked to accept the heat generation term Q as an input parameter to calculate the temperature gradient within the device. The lattice temperature is then used to directly calculate the internal thermal strain caused by CTE mismatch and temperature gradients through:

$$\varepsilon_{th} = \alpha(T - T_{ref}) \tag{5}$$

Here, ε_{th} is the thermal strain, α is the coefficient of thermal expansion (CTE), T is the lattice temperature, and T_{ref} is a reference strain temperature. In all simulations, T_{ref} is assumed to be 300 K.

The strain induced by the inverse piezoelectric effect (IPE) is accounted for through COMSOL's Piezoelectric Devices module, which combines piezoelectricity with solid mechanics and electrostatics for modeling of piezoelectric devices. The strain induced by an electric field is calculated through

$$\boldsymbol{S} = s_E \boldsymbol{T} + d^T \boldsymbol{E} \tag{6}$$

$$\boldsymbol{D} = d\boldsymbol{T} + \varepsilon_T \boldsymbol{E} \tag{7}$$

where $\boldsymbol{S}$ is the strain, $\boldsymbol{T}$ is the stress, $\boldsymbol{E}$ is the electric field, and $\boldsymbol{D}$ is the electric strain field. The material parameters s_E, d, and ε_T, correspond to the material compliance, the coupling properties, and the permittivity. COMSOL has the capacity to simultaneously account for piezoelectric and linear strain. That is, the simulation calculates the stress and strain within the piezoelectric materials (AlGaN and GaN layers) due to the electric field, as well as the stress and strain this induces on the other non-piezoelectric materials such as the substrate, electrodes, and passivating layer.

The residual stress/strain is not included within the simulation, but has been previously demonstrated in similar devices by [35]. The residual strain in the device is directly dependent upon the growth conditions, quality, and processing steps for making the devices. The devices from [35] have similar characteristics including epilayer thicknesses and matching substrate materials, and should therefore be a good approximation of the residual stress within the device.

2.2.2 Large-Scale Combined Physics Model

Since simulating the mechanical response of the device is "less" computationally intensive, a larger domain can be modeled to better account for the mechanical response

of a full device. Channel dimensions and layer thicknesses used in the large-scale mechanics model are identical to the small-scale electro-thermal model, but a larger substrate domain is used to better mimmic a full device structure. The AlGaN layer is modeled on top of the GaN and extends between the drain and source electrodes as demonstrated in Figure 14. The gate is located in the center of the channel, with the GCFP slightly offset towards the drain contact. Care was taken to align the geometries between the two models, since this could lead to error in the stress/strain calculations due to improperly matched geometries. In addition, similar meshing schemes were employed for the same reason. It should be noted that the overall width and height dimension of 100 μm for the substrate was determined from [54] and by minimizing the model domain without impacting the overall transient response – both thermally, electrically, and mechanically. That is, the domain was decreased (for reduced computational time) until a change was calculated for the temperature, electrical, and stress profiles were noticed. Less than a 1% difference in peak temperature is seen when the domain was enlarged to 300 x 300 μm. Finally, a conformal Si_3N_4 passivation layer is added to encapsulate the top of the geometry. The topography of this material was determined using an atomic force microscopy trace (AFM) of the device shown in Figure 13. Properly modeling the layer thicknesses and electrical contact dimensions are important for properly modeling both the electro-thermal and mechanical response of the devices. In particular, the conformal Si_3N_4 layer is crucial for proper stress/strain profiles, because of this extremely stiff, low CTE material.

2.3 Model Parameters

2.3.1 *Material Properties*

Proper handling of material parameters is crucial for determining the mechanical response of an AlGaN/GaN HEMT because of their complex structure, anisotropic material properties, and varying thicknesses. There is much research into the overall material properties of thin films, and numerous works have shown that crystal structure and direction can greatly impact the material properties [64]. Table 2 and Table 3 show the material properties for the Thermal Stress module.

Table 2. Structural Properties of Materials.

MATERIAL	STIFFNESS MATRIX (GPA)					YOUNG'S MODULUS (GPA)	POISSON'S RATIO
	C_{11}	C_{12}	C_{44}	C_{13}	C_{33}		
GaN [65]	390	145	105	106	398	-	-
6H-SiC [65]	501	111	163	52	553	-	-
Si_3N_4 [66]	-	-	-	-	-	195	0.25
Au [67]	-	-	-	-	-	97	0.42
AlGaN [35]	393	143	126	105	395	-	-

Wherever possible, anisotropic properties were used for the thermal conductivity and coefficient of thermal expansion. A wide range of material properties exists for thin film materials. Unlike bulk material properties, thin films, specifically the GaN layer, are more difficult to determine and a wide range of values exists for the elastic modulus, thermal expansion coefficient, and Poisson ratio [65, 68]. Such a large range of values can have a significant effect on the overall simulation, and therefore material properties must be chosen with care. For this thesis, material properties were chosen from literature based upon values that have been previously verified through numerical simulations and experimental results [35, 61].

Table 3. Thermal Properties of Materials.[1,2]

MATERIAL	COEFFICIENT OF THERMAL EXPANSION ($\times 10^{-6}$ K^{-1})	THERMAL CONDUCTIVITY ($WM^{-1}K^{-1}$)
GaN [25, 69]	$\alpha_a = -1.44\times10^{-5}\,T^2 + 1.7\times10^{-2}\,T + 0.553$ $\alpha_c = -1.39\times10^{-5}\,T^2 + 1.64\times10^{-2}\,T + 0.216$	$150\times(T/300)^{-1.4}$ [70]
6H-SiC [13, 71]	$\alpha_a = -1.36\times10^{-6}\,T^2 + 3.99\times10^{-3}\,T + 2.28$ $\alpha_c = -8.51\times10^{-7}\,T^2 + 2.94\times10^{-3}\,T + 2.44$	$387\times(T/293)^{-1.49}$
Si_3N_4 [72]	3.3	4.5
Au	14.2	317
AlGaN [35]	4.34	30

[1]Temperatures in Kelvin
[2]All temperature dependent properties valid from 300-550K

It is important to mention that wherever possible anisotropic temperature dependent thermal and structural properties were used to accurate describe the true mechanical response of the device. The construction of the stiffness matrix used in the structural simulations assumes transverse-isotropic elastic symmetry and takes the form shown in Equation 8.

$$[C_{ij}] = \begin{bmatrix} C_{11} & C_{12} & C_{13} & 0 & 0 & 0 \\ C_{12} & C_{11} & C_{13} & 0 & 0 & 0 \\ C_{13} & C_{13} & C_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & C_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & C_{66}^{*} \end{bmatrix} \tag{8}$$

*Where $C_{66} = (C_{11}-C_{12})/2$

For the Piezoelectric Devices module, Table 4 shows the electrical constants for GaN and AlGaN including permittivity matrix and piezoelectric coefficients.

Table 4. Electrical Properties for AlGaN and GaN.

Material	Permittivity matrix		Piezoelectric coefficients (Cm^{-1})		
	ε_{11}	ε_{33}	e_{15}	e_{31}	e_{33}
GaN [73]	8.6	10.5	- 0.41	- 0.47	- 0.84
AlGaN [73, 74]	8.71	10.23	- 0.386	- 0.505	0.975

In addition to these values, temperature- and mole-fraction dependent semiconductor band gaps and mobility values have been taken [54] and [61].

2.3.2 Model Boundary Conditions

All model boundary conditions are taken from previous modeling efforts [33, 35, 52, 54, 61, 62, 75, 76] and are shown in Figure 17 (not drawn to scale). For the large-scale mechanics model, a thermal boundary condition of 300 K was applied to the bottom of the SiC substrate and adiabatic boundary conditions are placed around all other surfaces. Similar to the small-scale model, symmetry about the drain electrode allows for just a single gate finger to be modeled. Natural convection (1-15 $Wm^{-2}K^{-1}$) boundary conditions were included in initial modeling efforts, but they were found to not greatly impact the peak temperature and are neglected as a "worst case" scenario for peak temperature and therefore stress. This is due to the peak temperature occurring below the surface of the device, under the low thermal conductivity and thick layer of Si_3N_4.

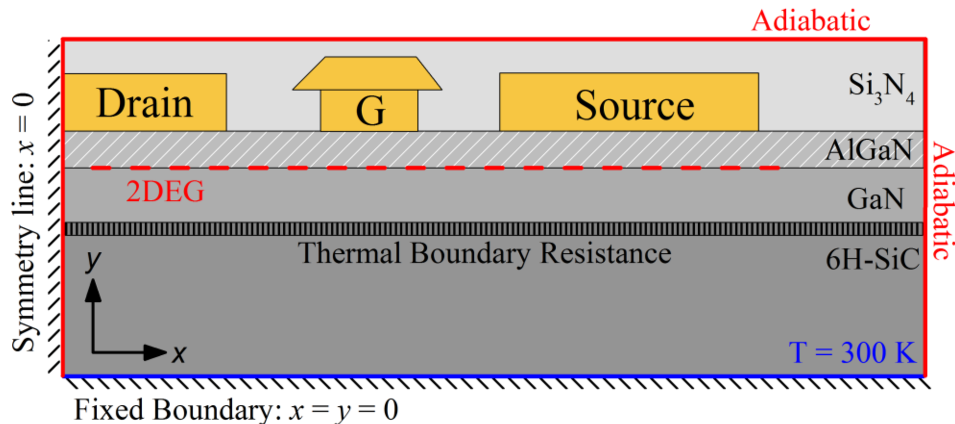

Figure 17. Representative model geometry with boundary conditions labeled (not drawn to scale). Due to symmetry, only half of the actual device is modeled. All boundary conditions are taken from information available in the literature.

Because of the varying length scales associated with semiconductor devices, the AlN nucleation layer is physically omitted, but is modeled as a Thin-Thermally Resistive Layer within COMSOL, or also called a thermal boundary resistance (TBR). The value of which, however, has been shown to vary greatly depending on substrate material and growth process [77-83]. For this thesis, a value of 60 m^2KGW^{-1} [80] is imposed at the GaN/SiC interface to account for the AlN layer itself, in addition to the thermal resistance associated with the GaN/AlN and AlN/SiC interface. A more detailed study of this assumed value will be performed in Chapter 5, when experimental vertical displacement measurements are compared to the model's predictions and the impact of this TBR is shown.

For the Piezoelectric Devices modeling, electrostatic potential (EP) lines are defined throughout the AlGaN and GaN layers, as highlighted in Figure 18. These lines assist in the interpolation between the small-scale EP results to the large-scale model.

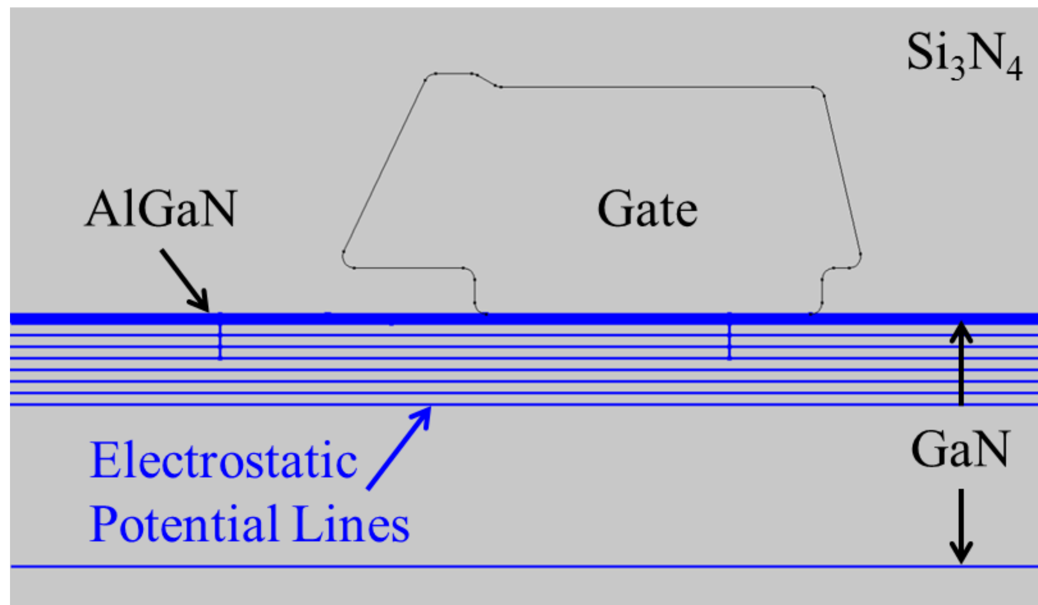

Figure 18. Demonstration of selected electrostatic potential lines. These values are taken from the small-scale electro-thermal model and input as boundary conditions within the AlGaN and GaN layers.

Lines are densely populated within the AlGaN (directly under gate) and are less frequent deeper into the GaN layer, where the EP changes less rapidly in the vertical direction. These lines also have the added benefit for assisted meshing. The COMSOL meshing scheme will be explained further in the next section, but these EP lines prevent the mesh element size from increasing rapidly, and allow for very fine meshing schemes to be placed in these critical areas.

Mechanically, the entire geometry is held fixed on the bottom of the SiC substrate. This constraint is to mimic a packaged device where the substrate is bonded to another holder material. In addition, the symmetry line through the drain electrode is held fixed to prevent moving in the x-direction while all other surfaces are left to deform freely. These mechanical boundary conditions are adopted from [61].

2.3.3 Mesh Sensitivity and Convergence Study

To verify the reported solution has converged, a mesh independence study has been performed. For this model, there is a large combination of irregular shapes (such as the conformal Si_3N_4 layer, ohmic and Schottky contacts). In these areas, a triangular mesh is required to properly capture small radius areas, especially at changing material boundaries. A triangular mesh is also used within the AlGaN layer and the top of the GaN, to better connect to the Si_3N_4 and metallizations mesh. Deeper into the GaN, however, a rectangular mesh is utilized to be more computationally efficient. Farther from the critical region of the device, temperature gradients and electric field gradients are smaller, leading to the ability to use a coarser mesh.

The mesh refinement technique implemented here involves local refinement and/or coarsening of a mesh (known as an h-refinement). This method is extremely common [84-88] because it can drastically increase the accuracy of the model without greatly

impacting the convergence rate. In fact, in some cases this method can increase the convergence rate of the model [87]. Within the critical regions, the mesh is refined until the resulting peak temperature has converged. Figure 19 represents locally increasing the mesh from ~6500 elements to more than 90,000 elements.

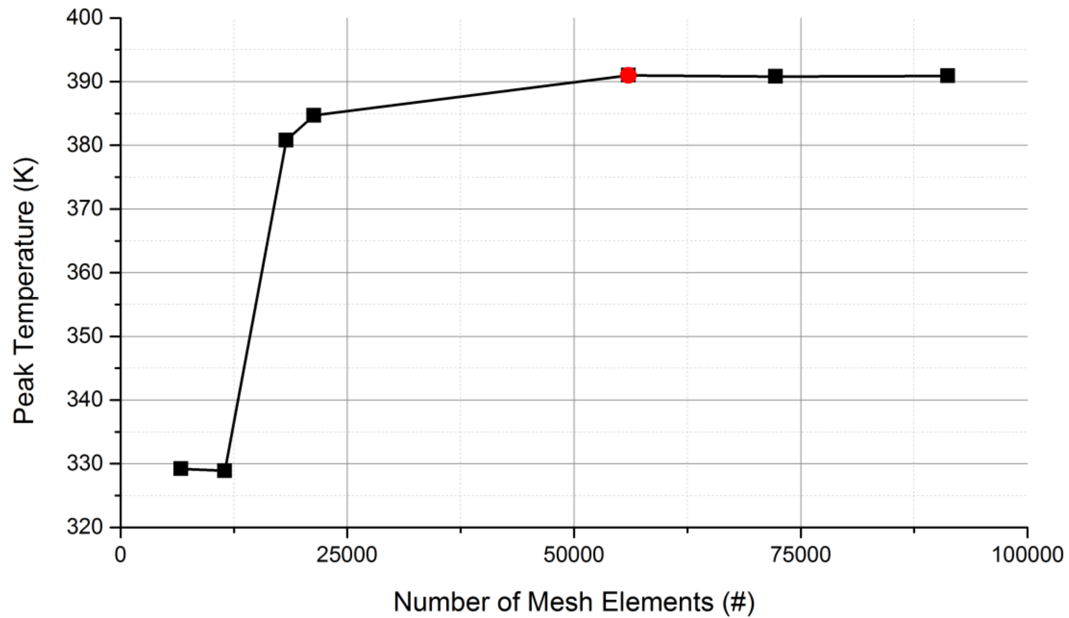

Figure 19. Mesh refinement study using peak temperature and local mesh refinement techniques.

A large increase in the peak temperature is seen between ~11,000 elements to ~21,000 elements. Due to the extreme confinement of the heat generation region, a coarse mesh leads to an under prediction in peak operating temperature. After ~55,000 elements (marked in red), no significant increase in temperature is seen. Therefore, it is safe to assume the model has converged, and further meshing does not increase the accuracy of the model. Figure 20 represents the final meshing scheme for the model corresponding to ~55,000 elements.

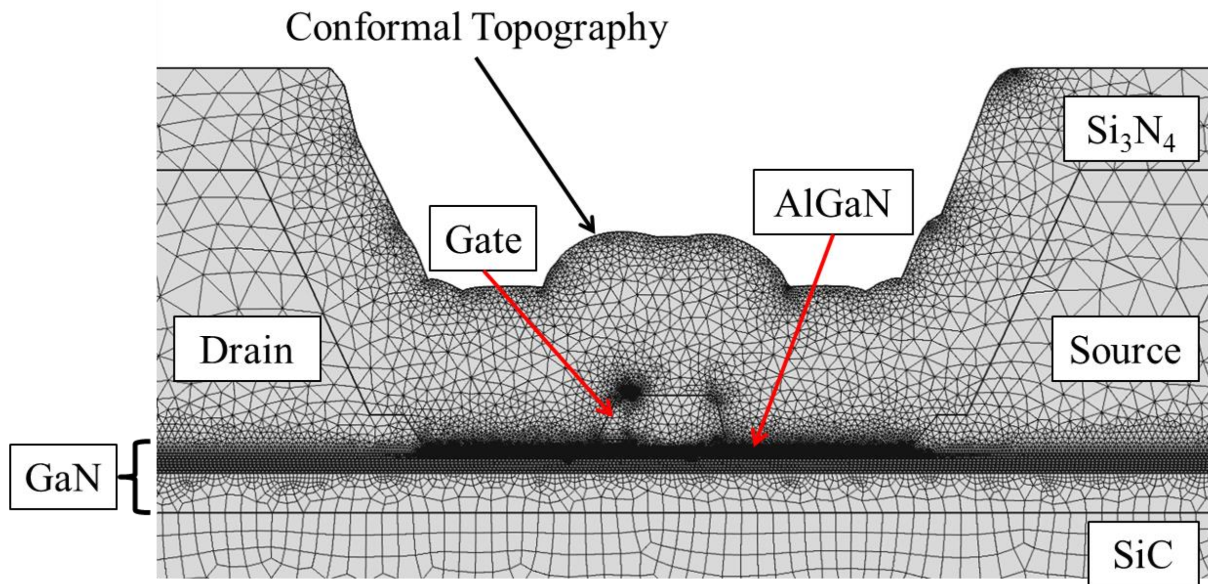

Figure 20. Final meshing scheme for the combined electro-thermo-mechanical model. The mesh is densely populated around the gate structure, where high thermal gradients and electric fields are present.

Although the mesh has converged, the model could still be susceptible to localized stress concentrations at sharp corners or changing material properties. Because of this, the reported stress profiles for the following sections will be taken from small, box averages located at the gate footprint (GFP) and the gate connected field plate (GCFP), where experimental probing is possible using optical techniques. The boxes are 5 nm x 1 nm and their locations are highlighted in Figure 21. Location 1 represents the GFP and Location 2 corresponds to the GCFP points for stress reporting.

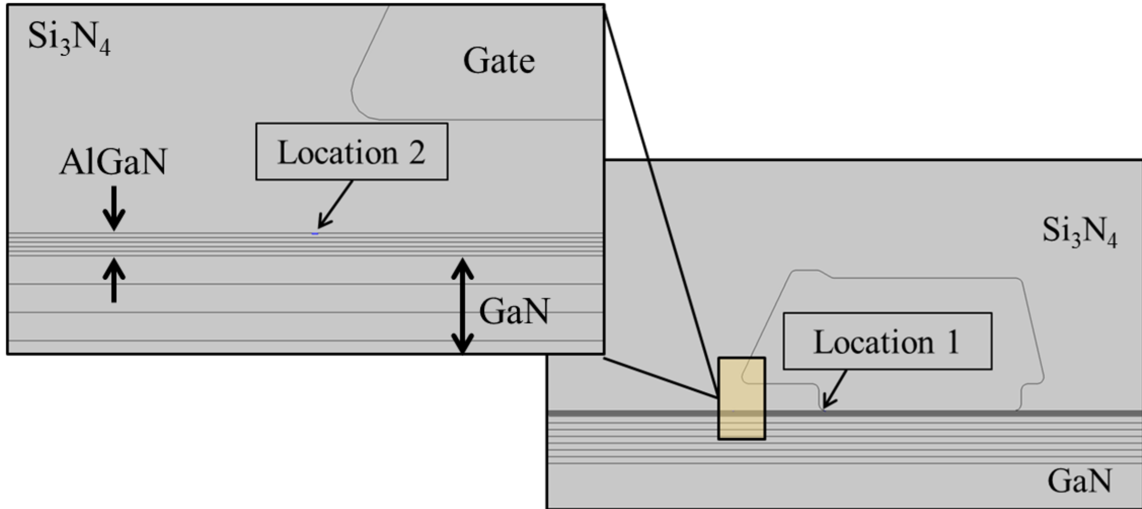

Figure 21. Location points of the small box average stress points. This allows for a conservative stress value to be reported.

Although these locations are relatively close to one another, it will be shown in Chapter 3 that this small spatial separation will highlight the drastic stress profiles that develop under transient operation.

2.3.4 Model Limitations

Finite Element Modeling (FEM) offers numerous benefits to aid in research, design, and manufacturing of systems. Most notably, even the most practical engineering problems can have irregular or complicated domains or nonlinearities associated with the governing physics that limit the ability to use analytical solutions. In addition, large parametric studies can be performed using FEM concurrently, which saves time and money when designing engineering systems. Although numerous researchers have shown its validity, there are several assumptions and limitations to applying this method to AlGaN/GaN HEMTs. Sentaurus Device, for instance, has been shown to be a powerful tool for modeling semiconductor technologies. One researcher [54] highlights the limitations of this modeling program. Although the developed electro-thermal model

is computationally efficient and yields realistic, physics based results, they believe actual channel temperatures will be higher than simulated due to sub-continuum effects. First, the model does account for the transport of energetic electrons and the release of energy gained in high electric fields to the crystal lattice, but it does not account for the full band structure of GaN, which may be a limiting factor in extreme electric fields. Another phenomenon known as "hot phonon bottleneck" [89] is not modeled. Researchers from [54] believe this effect alone will raise the peak temperature within the channel, and increase the bias dependence of this temperature by localizing the Joule heating even further.

Another limitation of the combined electro-thermo-mechanical simulation is the coupling between the physics. Specifically, these simulations are one-way coupled between the electro-thermal, electro-mechanical, and thermo-mechanical modules. In an actual piezoelectric device, strain is induced by crystal expansion/contraction *and* thermal expansion. In return, this strain would cause further generation of charge to develop, possibly leading to a higher 2DEG concentration. Put another way, secondary strain-induced changes would occur in the electric characteristics (piezoelectric polarization field) of the device is not considered. Although this effect may be small, a complete model would directly couple all of these physics, instead of one-way coupling. Even without this, however, good agreement between the experimental device and the electro-thermo-mechanical model is seen.

The final modeling limitation is the use of material properties. In particular, there is a large discrepancy between the thermal conductivity of AlGaN and GaN. Material properties such as thermal conductivity, heat capacity, and elasticity are directly dependent on layer thickness and quality of the crystal structure. Equally important, is the discrepancy of the thermal boundary resistance (TBR) [77] that is modeled at the GaN-SiC interface. Inclusion of this feature physically accounts for any dislocations or

surface defects that occur during the GaN growth process, but has been shown to have a wide range of values and can greatly impact resulting temperature profiles.

Despite these limitations, it will be shown that good electro-thermal agreement between the developed simulation and actual devices has been achieved in Chapter 3. Comparing developed models to actual devices gives confidence in the modeling technique; material properties used, and imposed boundary conditions. In addition, model results are compared to previously presented research in an effort to further validate the model. Once a comprehensive comparison is presented, the model is then applied to demonstrating the transient development of stress due to the inverse piezoelectric stress effect and thermoelastic stress due to CTE mismatch. To the knowledge of the author, no researchers have presented as detailed of a transient characterization of the mechanical response for AlGaN/GaN HEMTs. Therefore, this work could aid in the selection of operating conditions for these devices operating within the RF regime such as bias conditions, frequency, and duty cycle.

CHAPTER 3 TRANSIENT DEVELOPMENT OF STRESS WITHIN ALGAN/GAN HEMTS

3.1 Simulating Electro-Thermal Behavior

The transient formation of stress profiles in AlGaN/GaN HEMTs must be determined before transient failure mechanisms can be fully understood. In this Chapter, the electro-thermal response of a device under DC operation is simulated and compared to experimental devices. This includes the electrical I_{ds}-V_{ds} curves as well as a qualitative comparison to the previously demonstrated bias dependent Joule heating profiles (Figure 12). Next, the formation of stress profiles along the AlGaN/GaN interface is presented to show the peak stress location shifts during pulsed operation. Large stress gradients develop due to the complex electric fields around the gate metallization and thermoelastic stress associated with large temperature gradients and CTE mismatch of materials. In addition, the inverse piezoelectric stress effect remains constant during the ON-state while the thermoelastic stress builds rapidly. When the device is switched to the OFF-state, the IPE stress is relaxed nearly instantaneously, while the thermoelastic stress relaxes slower as the device cools.

3.1.1 DC Comparison: I_{ds}-V_{ds} Electrical Curves

Prior to determining the transient stress profiles, it is important to demonstrate the capabilities of the modeling technique and validate the model based on comparison to experimental test devices and to similar modeling techniques produced in literature. As previously mentioned, the model structure is based upon experimental test structures that

are fabricated using the same techniques as commercially available devices, but have slightly different structure (namely a centered gate electrode) for experimental testing.

To prove the electro-thermal coupling, a comparison plot between experimental and numerical model electrical curves is shown in Figure 22. Experimental devices were bonded to carrier packages using commercially available silver epoxy for testing.

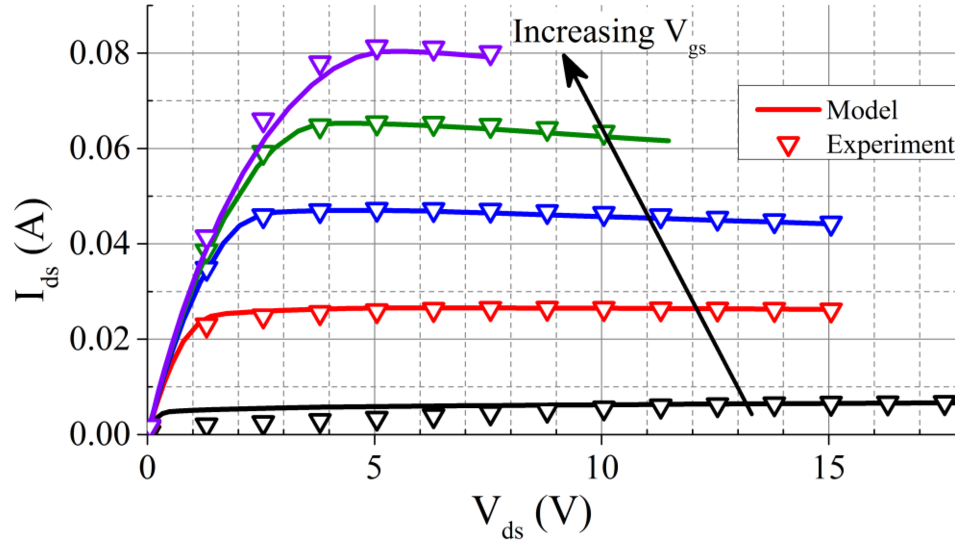

Figure 22. Numerical model comparison of I_{ds}-V_{ds} electrical curves to experimental test structures. Good agreement is seen across a wide range of bias conditions.

For each curve, the V_{gs} is set to a specific value and the V_{ds} is increased while the drain current (I_{ds}) is measured. V_{gs} is varied from -3 V (black curve) to +1 V (magenta curve) in increments of 1 V. The majority of the results in this thesis lie in the -2.5 to 0 V V_{gs} range, which shows excellent agreement between the numerical model and the experimental devices. Another important factor is the model's ability to predict current "droop" due to self-heating within the device. This is seen as a drop in the saturated I_{ds} and is more prominent at higher V_{ds} values (as evident from the Figure). Some disparity, however, is seen in the -3 V and + 1 V case. This is likely due to the nonlinear behavior in the device, the excess generation of hot phonons at varying V_{gs} values, or could be a result of assumed boundary conditions on the model. Electro-thermal coupling is a key part in understanding device physics and understanding the varying stress profiles that

develop under transient operation. Chapter 4 will highlight in detail the impact bias conditions, frequency, and duty cycle have on the cyclic stress profiles.

3.1.2 DC Comparison: Bias Dependent Heating

In addition to the electrical response shown in the previous section, it is important to demonstrate the bias dependence heating within the device. This will aid in future sections, where the transient stress profiles are shown to be largely bias dependent. The three comparison V_{ds} values (10, 28, and 48 V) were chosen based on commercially available devices. For each case, V_{gs} is adjusted to yield the same dissipated power of 6 Wmm^{-1} and the resulting values are -0.1976 V, -2.072 V, and -2.539 V, respectively. Although equal power is dissipated across the three cases, Heller demonstrated (Figure 12) the very different heating profiles will occur within the devices. This information is used as a qualitative comparison to the developed model. Only a qualitative comparison can be made, since Joule heating and electrical data is directly dependent upon device structure include source-to-gate and gate-to-drain dimensions, total number of gate fingers, gate finger width, and substrate material. Figure 23 represents the electric field (top row) and resulting Joule heating profile (bottom row) for the 10, 28 and 48 V_{ds} conditions. Although equal power is dissipated, the change in drain bias causes drastically different electrical and thermal profiles.

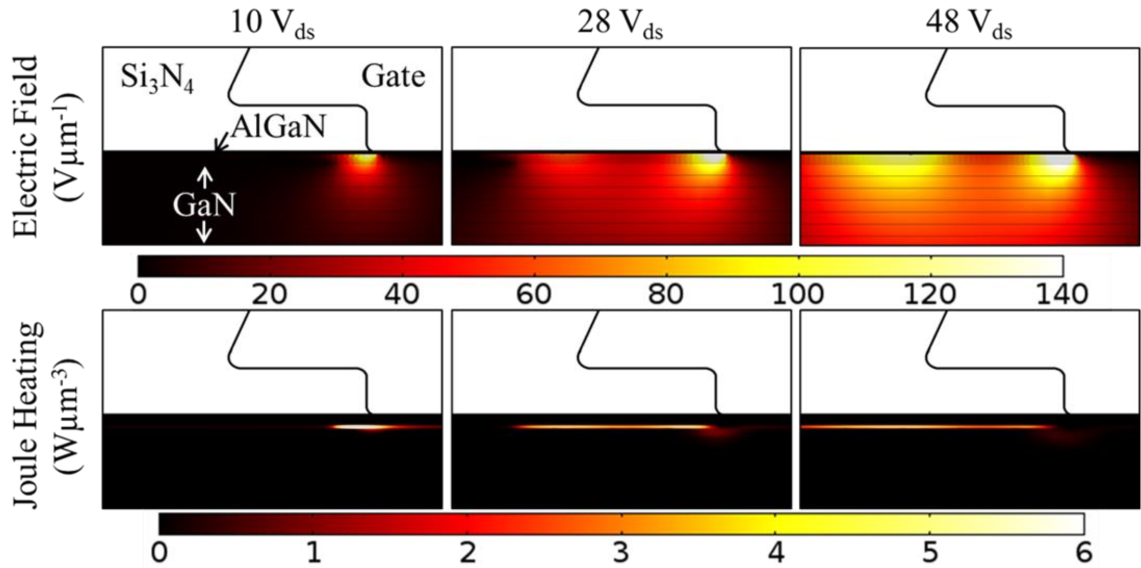

Figure 23. Simulated electric field (top row) and resulting Joule heating profiles (bottom row) for V_{ds} = 10, 28, and 48 V. V_{gs} is adjusted to dissipate an equivalent 6 Wmm^{-1}.

Qualitatively, these results are in good agreement with those previously presented, and are a direct result of the structural characteristics of the device. By varying the V_{ds} and V_{gs} bias conditions, the electric field around the gate structure is altered, resulting in a change in the Joule heating profile within the device. Increasing the V_{ds} from 10 V to 48 V yields a larger electric field under the GCFP, causing an elongation in the Joule heating profile towards the drain (located to the left of the gate structure in Figure 23). Figure 24 represents the temperature profile along the AlGaN/GaN interface for the three power conditions. Similar to Heller, the vertical lines correspond to the gate connected field plate (left vertical line) and the gate footprint (right vertical line) positions. As the drain bias is increased, the higher electric field around the gate connected field plate (GCFP) shifts the Joule heating and thus the localized hotspot towards the drain contact by ~200 nm, which is on the order of the GCFP dimension.

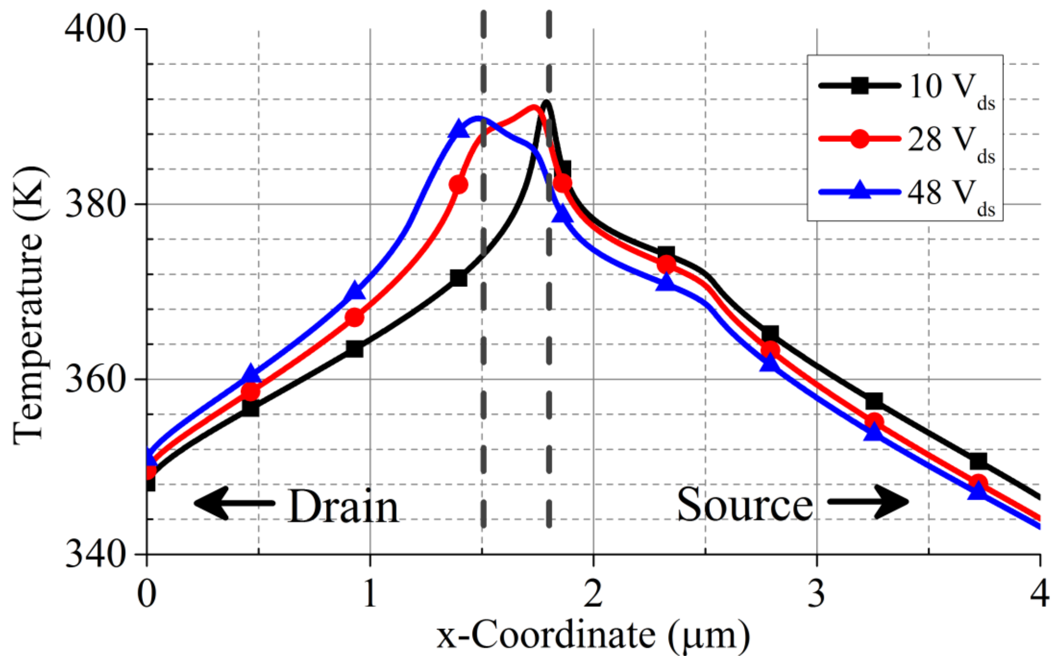

Figure 24. Temperature profile comparison for three different bias conditions with equal total dissipated power. Higher electric fields around the GCFP shift the heat generation towards the drain contact.

The model's ability to accurately account for the electrical characteristics of the device is crucial to predict the resulting electrical and thermal profiles in the device. It will be shown the complex stress profiles that develop under transient operation are directly dependent upon the bias conditions chosen, and properly accounting for the bias dependent electrical and thermal profiles is key to understanding transient device operation. Demonstrating the model's capabilities in addition to comparing to previously published research gives confidence in the model's capacity to effectively determine the development of transient stress within the device under various RF operating conditions.

3.2 Transient Stress Characterization

3.2.1 Transient Stress along the AlGaN/GaN Interface

The response of the AlGaN/GaN HEMTs to pulse conditions was determined. The simulated device was pulsed at 28 V_{ds} at a constant gate bias of -2.072 V_{gs} and duty cycle of 50% at 100 kHz frequency from a starting temperature of 300 K to characterize the development of stress in the device. A duty cycle of 50% is chosen because this condition yields the largest temperature difference between the ON- and OFF-states, which will be demonstrated in a following section, and an operating frequency of 100 kHz is a good representative frequency for a typical operating condition of high frequency and power conditions. The assumed 2DEG location causes the Joule heating to develop along the AlGaN/GaN interface, and thus probing along this interface gives insight to the electrical and thermal stresses that develop under transient operation. The model utilizes a transition period length of 100 ns from OFF-state, where V_{ds} = 0 V and V_{gs} = -2.072 V, to ON-state, where V_{ds} = 28 V and V_{gs} = -2.072 V. This creates a rapid shift in voltage to simulate actual operating conditions. These bias conditions were chosen based upon representative operating conditions for the device, and dissipate 6 Wmm^{-1} under DC operation. The applied V_{ds} value changes rapidly compared to the thermal response of the device. Because of this, the bulk of the piezoelectric portion of stress is expected to develop almost instantaneously because of the sudden voltage potential rise, while the thermal contribution to stress will increase throughout the ON-state portion due to the Joule heating in the device. Because of the electro-thermal coupling, it is expected for both the electrical and thermal profiles to change slightly throughout the ON-state portion of the pulse, since increasing temperatures decreased device mobility.

Figure 25 represents the waveform signal for the applied drain bias (V_{ds}), the resulting dissipated power (P_{ds}), and peak temperature (T_{max}) during transient operation of the device.

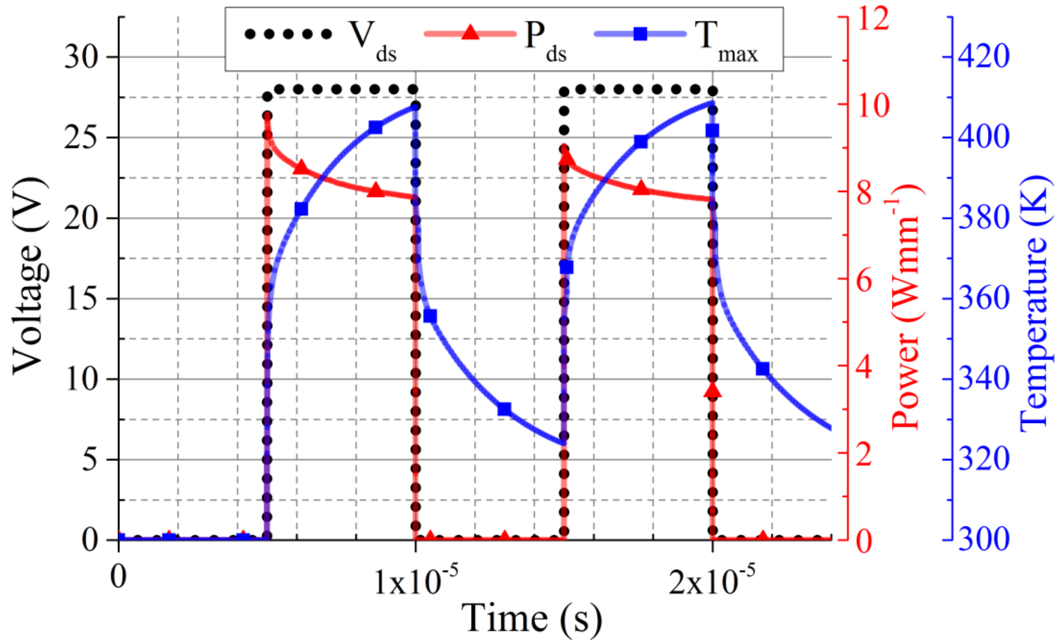

Figure 25. Applied bias conditions for drain and gate electrodes and dissipated power. Device power increases rapidly with applied drain bias and Joule heating occurs. Because of the temperature dependent mobility, dissipated power decreases as the lattice temperature increases.

Under transient operation, a larger power can be dissipated because the Joule heating is less impactful on electron mobility within the device. With the same bias conditions, only 6 Wmm^{-1} is dissipated by the device, while 8-9W/mm is dissipated at 100 kHz and 50% duty cycle. Joule heating still impacts the device under transient operation and is seen as a drop in P_{ds} during the applied V_{ds}. The peak temperature rises quickly with applied V_{ds}, since formation of the Joule heating occurs the instant the V_{ds} is applied. Although not shown, the V_{gs} is held constant during device pulsing.

Next, it is important to determine the individual and combined impact IPE and thermoelastic stress have on the device along the AlGaN/GaN interface. At this interface, large electric fields develop due to the proximity to the gate structure and large temperature gradients occur because the bulk of Joule heating develops at this interface.

Figure 26 represents the vertical component of electric field along the same interface and for the same corresponding times. Similar to Figure 12, vertical lines represent the GFP position (right vertical line) and the GCFP position (left vertical line).

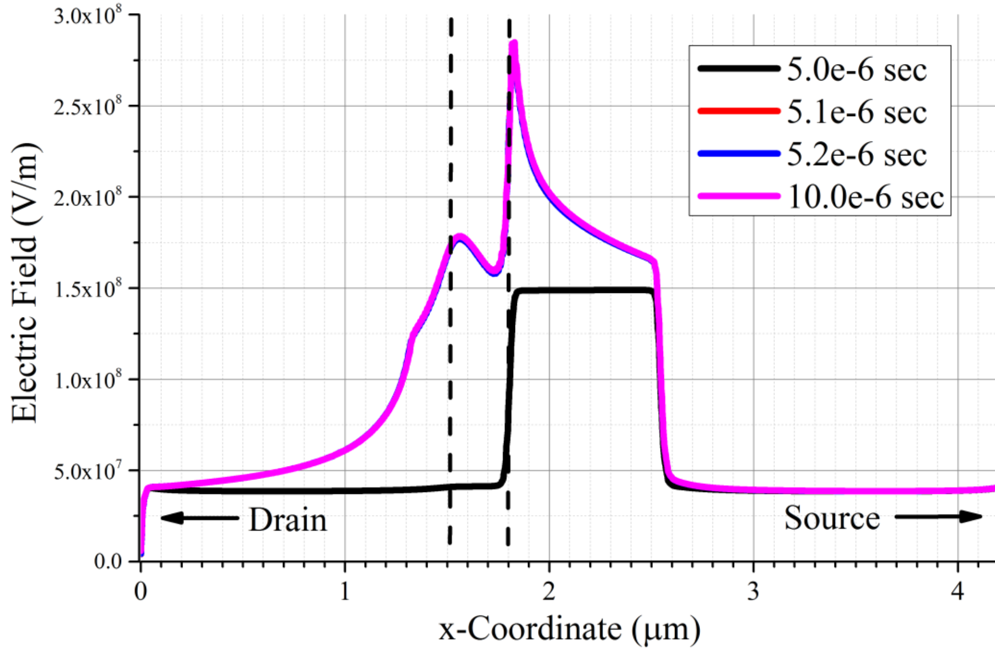

Figure 26. y-Component of the electric field around the gate structure. A local maximum is seen at the gate connected field plate (left dashed black line) and a global maximum is seen at the gate footprint position (right dashed black line).

The electric field develops rapidly with applied drain bias (V_{ds}) and is constant throughout the ON-state portion of device operation. Similarly, the peaks shown in Figure 26 correspond to the gate connected field plate (left vertical line) and the gate footprint (right vertical line). Due to the piezoelectric behavior of AlGaN and GaN, large stress gradients are expected as a direct result of the large electric field gradients – especially at the gate footprint edge.

Figure 27 shows the in-plane stress (x-component) of piezoelectric stress along the AlGaN/GaN interface from just before the ON-state V_{ds} pulse (time = 5.0e-6 seconds), to just before the end of the ON-state (time = 10.0e-6 seconds).

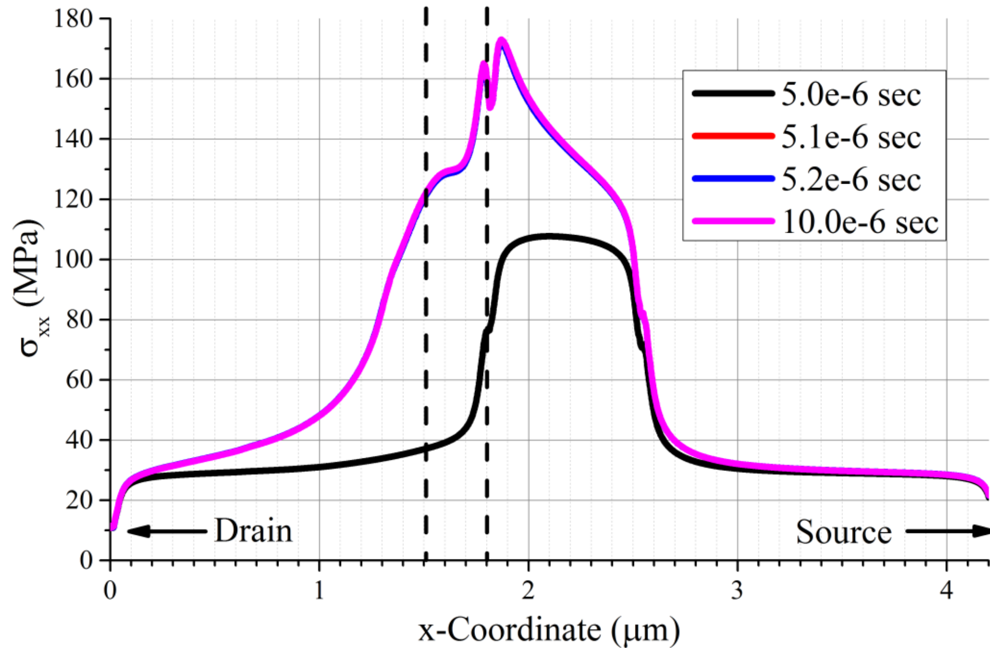

Figure 27. x-Component of piezoelectric stress along the AlGaN/GaN interface just before the ON-state (corresponding to 5.0e-6 sec) to just before the OFF-state (corresponding to 10.0e-6 sec).

Again, the right, vertical dashed line corresponds to the gate footprint edge on the drain side while the left vertical, dashed line represents the gate connected field plate location. During the OFF-state and prior to the V_{ds} pulse (corresponding to 5.0e-6 seconds), stress is nearly symmetrical around the gate. At this time, electrical potentials on both the drain (left of the gate) and source (right of the gate) are 0 V, leading to an equivalent electrostatic potential on either side of the gate structure. This profile is not exactly symmetrical, however, because the gate structure itself is not symmetrical. As the drain bias rapidly increases (as shown in Figure 25), the peak stress along this interface shifts towards the drain side of the gate structure. The peak location corresponds to under the gate footprint, near the peak electric field located at the AlGaN/GaN. At this location, the electrostatic potential within the AlGaN (and GaN) layer rapidly changes from the applied 28 V_{ds} to a value influenced by the -2.072 V_{gs}. It should also be noted that little change is seen in Figure 27 between the 5.01e-6 sec time (which corresponds to right after the 28 V_{ds} is reached) and the 10.0e-6 time (which corresponds to nearly the end of

the pulse). This is caused by the sharp increase in electric potential of the device in response to the sudden increase in V_{ds}. From the OFF-state to the ON-state, over 40 MPa increase in stress state at the AlGaN/GaN interface is seen. In addition, the peak location of the maximum stress state shifts towards the drain ohmic contact by 0.275 μm – which is on the order of the gate connected field plate length. This is not the maximum amount of piezoelectric stress induced in the device, but rather the in-plane stress at the AlGaN/GaN interface. The peak in-plane stress in the device occurs within the AlGaN layer where the electric field is highest – directly underneath the gate footprint on the drain side. In the OFF- state, the peak x-component of stress is found to be at the gate footprint edge on the drain side with a value of 121 MPa, and increases to 282 MPa by the end of the ON-state. The OFF-state stress is attributed to the negative applied gate voltage, which is held constant during V_{ds} pulses.

Characterizing how both the electric field and the resulting stress change along the AlGaN/GaN during cyclic operation is critical for understanding the impact transient reliability issues associated with these devices. Transient electrical characterization is just one component of the total stress along this interface. A complete finite model must account for the Joule heating within the device that is coupled with the electrical profiles. The thermal response due to the Joule can also induce large stress values due to CTE mismatch. Figure 28 represents the temperature profile for the AlGaN/GaN interface for the same time values.

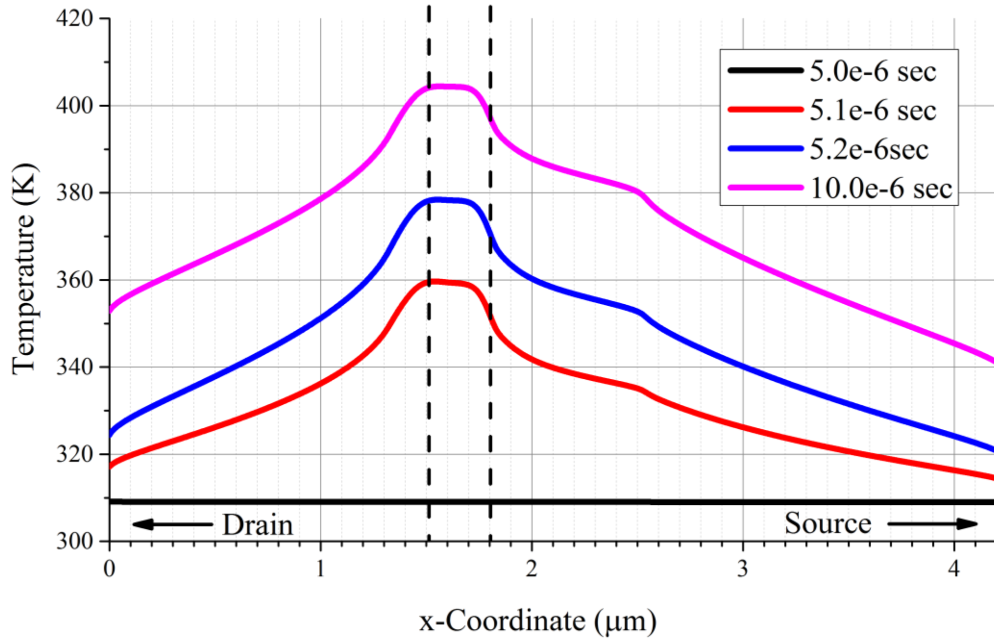

Figure 28. Temperature profile along the AlGaN/GaN interface. Temperature rises rapidly with applied drain bias (V_{ds}), but continues to build throughout the entire ON-state.

As evident from comparing Figure 26 to Figure 28, Joule heating lags behind the piezoelectric effect. The electrical field (and thus IPE stress) develops nearly instantaneously, while the thermal stress effects build throughout the ON-state. This is shown as a temperature rise (Figure 28) and through the thermoelastic stress plot shown in Figure 29. In addition, the thermoelastic stress is largely compressive, especially in areas away from the gate structure and in the channel of the device towards the drain contact. In fact, along this interface, the peak compressive stress exists outside the gate connected field plate.

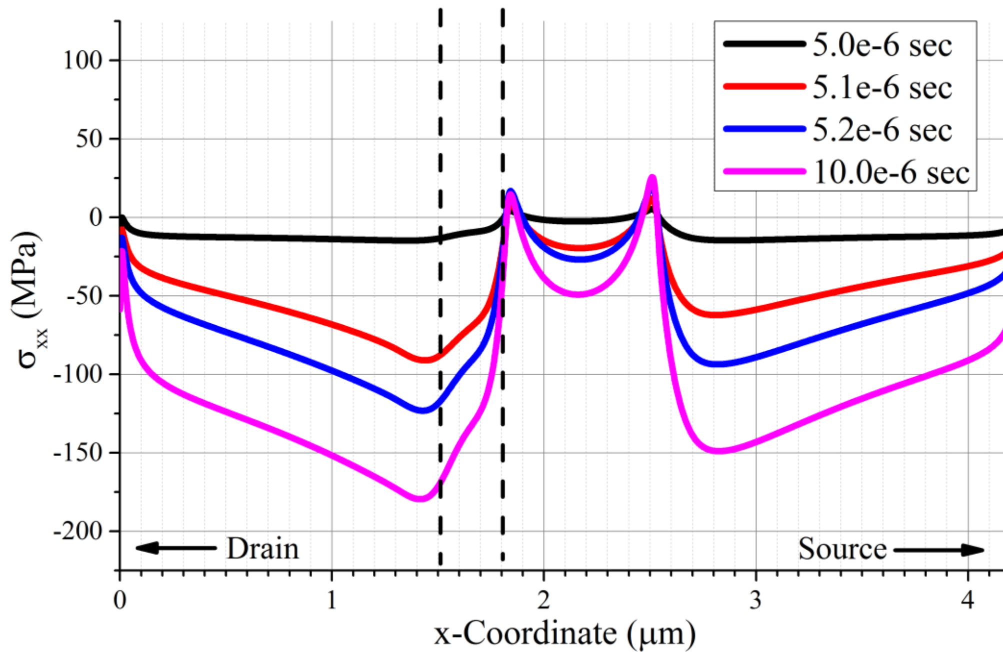

Figure 29. x-Component of thermoelastic stress along the AlGaN/GaN interface. Thermoelastic stress builids throughout the ON-state due to the increase in temperature along this interface.

As with the piezoelectric stress, these values do not represent the maximum amount of thermoelastic stress in the device. The maximum (tensile) and minimum (compressive) x-component of thermoelastic stress is found to be 226 MPa and -136 MPa, respectively. The piezoelectric portion of stress is present immediately after the 28 V_{ds} value is reached, while the magnitude of thermoelastic stress increases during the entire ON-state. Similar to the piezoelectric stress, the peak temperature and stress points shift toward the drain ohmic contact during the ON-state pulse.

These results indicate the stress along this interface is not only under cyclic loading due to the OFF- and ON- states, but also the maximum point location of stress is changing throughout the duration of the ON-state. The thermoelastic stress, however, is compressive whereas the piezoelectric stress is tensile along this interface. Because of this, portions of AlGaN/GaN interface relax during the ON-state because of the Joule heating. Using superposition, the overall resulting combination of IPE + thermoelastic stress can be determined (Figure 30).

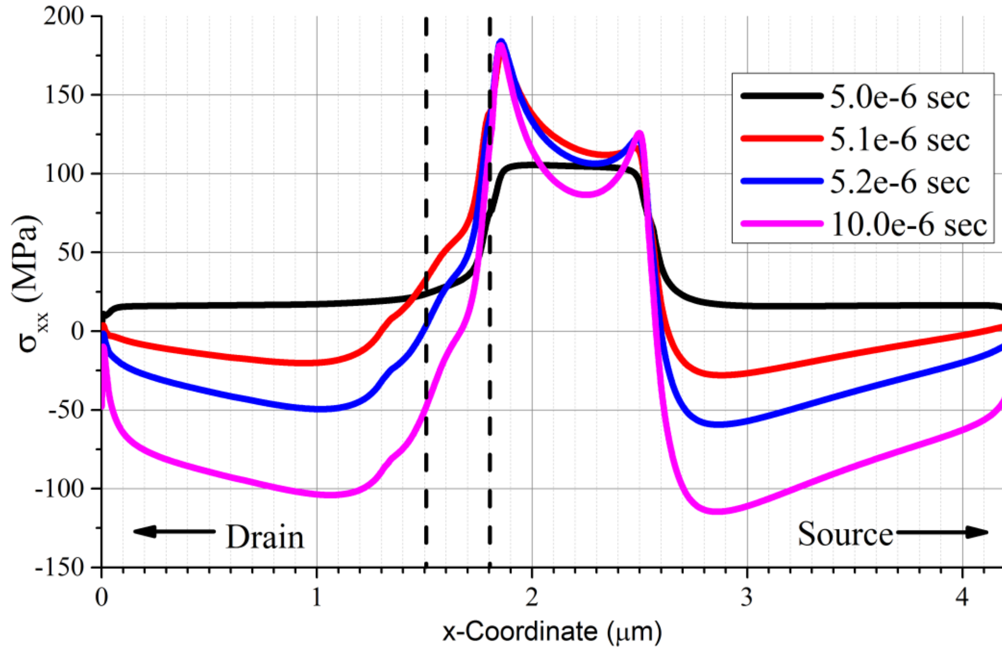

Figure 30. x-Component of the combined stress profile (Thermoelastic + Electric) along the interface. Large stress gradients develop between the channel and gate footprint locations, which could lead to device degradation.

Outside of the gate structure, the thermoelastic stress dominates and the resulting stress is largely compressive, although some relaxation due to the tensile IPE stress does occur. Around the gate footprint, however, the IPE stress dominates making the resulting stress tensile in this area. Between these areas, however, the stress gradient is extremely high. This is seen by the conversion from the highly compressive stresses outside the gate structure to the tensile stresses around the gate footprint. Over the span of less than 0.5 μm, the stress value along this interface changes from -175 MPa to approximately 75 MPa – leading to a complex stress profile that is constantly changing due to the cyclic loading and unloading of the device. It is possible that this stress gradient combined with the cyclic loading and moving peak stress location could lead to different forms of device degradation for AlGaN/GaN HEMTs when compared to DC operation mode.

3.2.2 *Location Dependent Transient Stress*

To further characterize the transient development of stress within AlGaN/GaN HEMTs, two point locations were chosen to show how stress varies during cyclic operation. In particular, the two main areas of interest are the gate footprint (or "critical region"), since large amounts of tensile stress is known to develop here, and just outside the gate connected field plate (GCFP), since this area can be probed relatively easily using optical techniques. In addition to the interfacial stresses shown in the previous section, point locations can show how stress changes in various areas within the device, especially within the AlGaN layer, where residual stresses can be in the excess of 3 GPa [35] for devices on SiC substrates. Figure 31 graphically shows the two regions of interest.

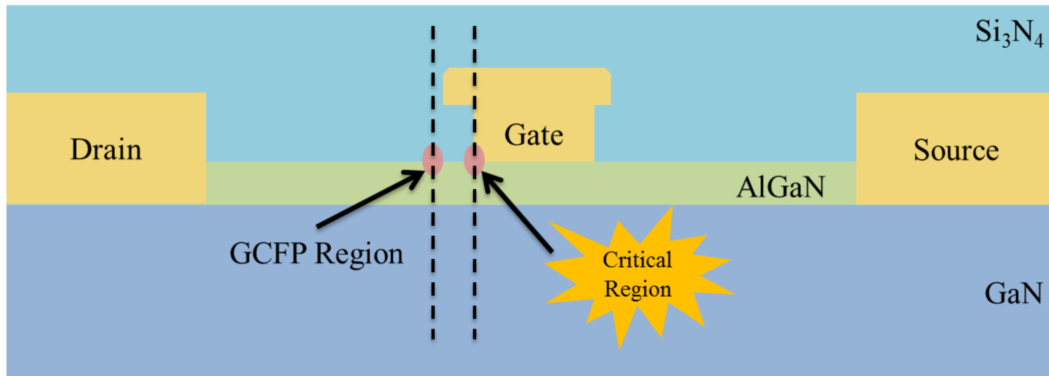

Figure 31. Critical region (located at the gate footprint on the drain side of the device) within the device where highly tensile thermoelastic and electrical stresses develop. Gate connected field plate region (GCFP) is marked as the second point of interest for optical probing of devices.

In both locations, large electric fields develop during the ON-state because of the applied V_{ds} and V_{gs} voltages. Electric fields, represented with units of [Vm^{-1}], are modulated by either changing voltage [V] or distance [m]. Therefore, electric fields at the AlGaN/GaN interface are higher around the "critical region" (or gate footprint) because of its proximity to the gate structure compared to the area under the GCFP. Figure 23 reveals a second electric field peak develops at the GCFP for as drain bias increases, but is less in

magnitude because it is farther from the probed interface. These two points are chosen because of the high electric fields and large temperature gradients. In addition, the critical region is thought to be the location where mechanical degradation occurs most in devices, and the GCFP region is the area often probed experimentally, since the critical region is covered by the GCFP.

Figure 32 shows the stress at the critical region within the device as a function of time. As before, this does not account for additional residual stress within the devices as a result of fabrication processes and lattice mismatch.

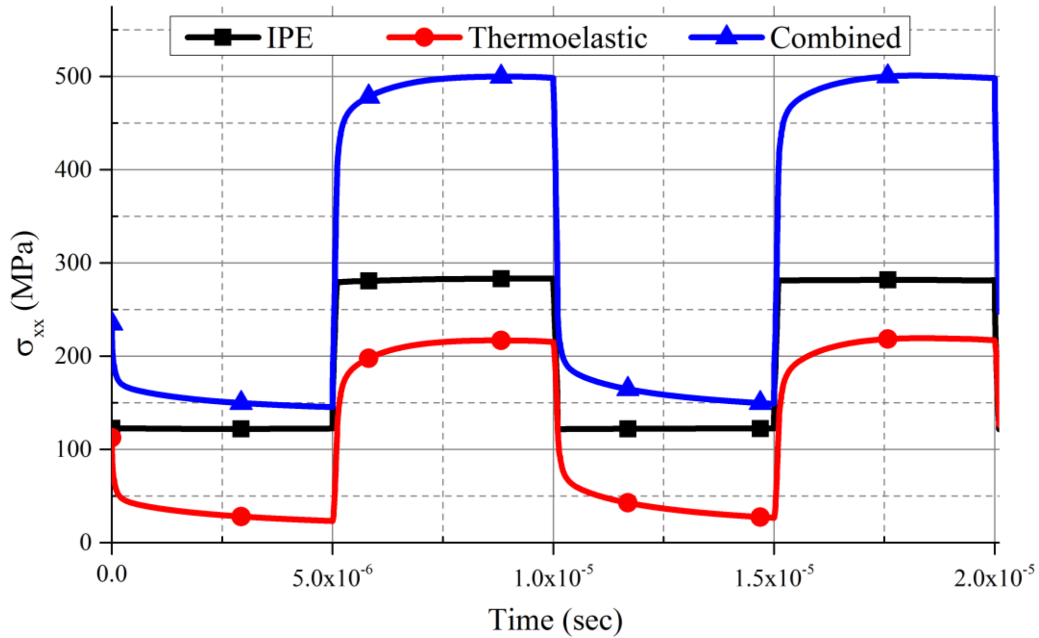

Figure 32. Gate footprint (GFP) stress profile. Both IPE and thermoelastic stresses are highly tensile, leading to a large and rapid development of stress in this location.

Prior to the first pulse (device is in the OFF-state at a time corresponding to 5.0 x 10^{-6} sec), electrical stress exists within the device due to the gate bias and some thermoelastic stress exists because of the previous pulse. Nearly immediately after the ON-state, further tensile stress is induced because of the inverse piezoelectric stress effect of the AlGaN and GaN materials caused by the applied bias condition. Simultaneously, the device begins to rapidly heat, yielding an even higher tensile stress. At this critical

region location, the Joule heating profile is extremely close and results in rapid heating of devices. In addition, the CTE mismatch of the gate metal (Au), AlGaN, and SiN_x yield highly tensile stresses. During the ON-state, tensile stress builds continuously as the device heats until the OFF-state (10.0 x 10^{-6} sec). Throughout the OFF-state, the device cools, returning to the initial internal stress state from the previous pulse. For Figure 32, the critical region point corresponds to nearly the hottest point within the device, which is why the rapid transition in thermoelastic stress is seen. The GCFP point, however, is farther from the device "hot spot" and does not develop tensile stresses due to the high CTE gate electrode (Figure 33).

Compared to the critical region (Figure 32) the overall combined stress is not only compressive, but is much lower in magnitude. This point is still relatively close to the "hot spot" which is why the compressive stress develops relatively quickly, but some lag is seen between the compressive and tensile stresses. This is seen visually on Figure 33 as a rapid upshot in combined stress (due to IPE), and then drops quickly as the larger magnitude thermoelastic stress begins to develop. The amount of relaxation due to the thermoelastic stress is directly dependent on the duty cycle and frequency.

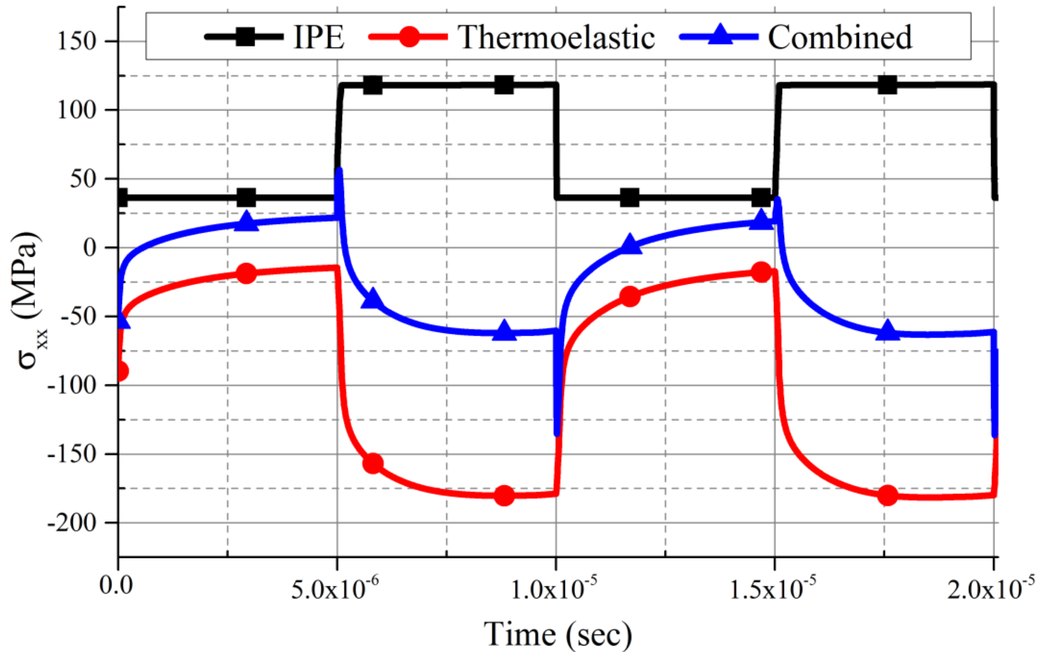

Figure 33. Transient stress corresponding to a location just outside of the GFP. Thermoelastic stress develops after the IPE stress, and is compressive. The highly tensile IPE stress counteracts the thermoelastic stress, yielding an overall reduce stress state.

As previously mentioned, the results presented are for 50% duty cycle. If, for instance, a duty cycle of 5% or less was chosen, or the frequency was increased, the majority of cyclic stress would be due to just the inverse piezoelectric effect, and little relaxation would occur. It is important to understand that the piezoelectric stress is heavily bias dependent, and is always present for a given set of bias conditions, regardless of frequency and duty cycle.

The stress gradient between these two points (the critical region and the GCFP region) is quite large. At the critical region, a peak combined stress value of 500 MPa is calculated, while the GCFP has a combined stress state of approximately -75 MPa. This yields a nearly 575 MPa stress change over the 0.300 μm distance between these points. As evident from Figure 30, discrete points within this region around the gate structure will undergo varying levels of cyclic stress due to the inverse piezoelectric and thermoelastic stress occurring. The thermoelastic stress is largely dependent upon the

location within the device (whether it is tensile or compressive) and the frequency and duty cycle (both of which impact the duration of the ON-state).

Figure 33 represents the combined inverse piezoelectric and thermoelastic stress in the device at the time corresponding to 10.0 x 10^{-6} seconds (last instance the device is powered in the ON-state). Here, the maximum x-component of stress in the device exists at the corner of the gate footprint on the drain side and is found to be around 570 MPa.

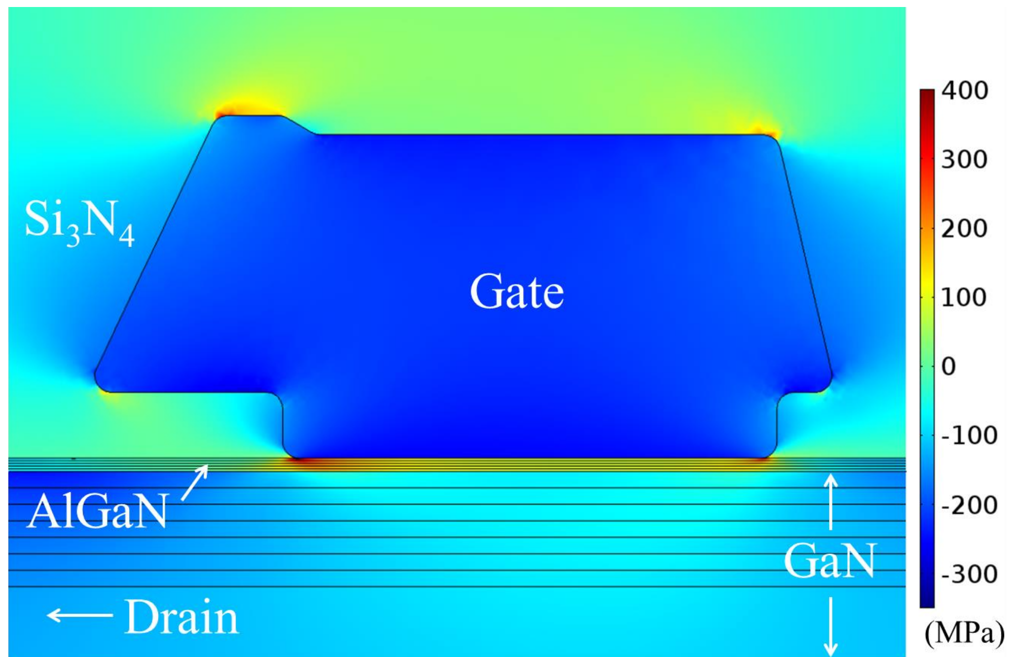

Figure 34. Stress distribution due to thermal and piezoelectric effects at the end of the first ON-state pulse. High amounts of stress exist underneath the gate footprint as a result of high electric field and CTE mismatch of AlGaN, GaN, Au, and Si3N4 layers.

This is due to the large electric fields and coefficient of thermal expansion mismatch of the Si_3N_4, AlGaN, and Au materials around this point. It has been previously shown that the intrinsic stress plays a large role in the onset of degradation within the device [35] and increasing the tensile load within the AlGaN makes this layer vulnerable to mechanical failure [90]. Reference [35] calculated the intrinsic stress within AlGaN layer in the region of the gate edge to be around 3 GPa for AlGaN/GaN HEMTs on SiC substrates with degradation expected around a combined intrinsic, inverse piezoelectric, and

thermoelastic stress of 3.75 GPa. It should be noted that the degradation point will be different between varying device structures, but bias conditions and cyclic loading of the device will contribute to degradation of the device if the combination of intrinsic, inverse piezoelectric, and thermoelastic stress exceeds the expected degradation point for the device. The stresses at the beginning of each pulse in the device occur from residual + inverse piezoelectric stresses in the AlGaN layer. However, these stresses are relaxed in some areas within the device upon Joule heating, but the CTE mismatch between the gate metal and the AlGaN layer induces an additional stress. Thus, for devices which are cycled at a low duty cycle versus high duty cycle, differences in failure rates may occur not simply due to heating, but due to the peak in stress states, where they occur in the device, and duration of applied stresses.

It was found that during the ON-state of a device under pulsed conditions, tensile stress between the AlGaN/GaN layers quickly rises and shifts towards the drain side of the gate edge due to the inverse piezoelectric effect. This is attributed to the sharp rise in drain bias and change in electrostatic potential within the device from the applied V_{ds} to V_{gs}. During the ON-state, this stress is relaxed by the compressive thermoelastic stress outside of the GCFP, which builds during the ON-state due to Joule heating, but the opposite affect is seen in the critical region of the device where IPE and thermoelastic stresses are both tensile. It was shown that the peak from the inverse piezoelectric stress effect and thermoelastic stress changes in magnitude and position between localized areas under the gate structure to the gate foot print during pulsed operations which may lead to duty cycle dependent degradation rates in AlGaN/GaN HEMTs.

Complex stress profiles develop within AlGaN/GaN HEMTs under transient operating conditions. The electrical stress develops rapidly with applied bias, while the thermoelastic stress builds during the ON-state of a device. Areas of interest including at the GFP and outside of the GCFP undergo vastly different transient stresses due to the electrical and thermal profiles. At the GFP, the electrical and thermoelastic stresses are

tensile, resulting in an extremely localized concentration of tensile stress that is suspected to cause reliability issues for these devices. At the GCFP, however, the electrical stress is tensile while the thermoelastic is compressive, leading to an overall relaxed stress state in this area of the device. Even though these locations are close in proximity, high stress gradients develop between these points. Under transient operation, these points undergo heavy amounts of cyclic loading, which could induce failure mechanisms not seen under DC operating conditions, where most of the reliability studies have been performed.

CHAPTER 4 IMPACT OF FREQUENCY, DUTY CYCLE, AND BIAS CONDITION ON THE STRESS WITHIN AlGaN/GaN HEMTs

4.1 Operating Conditions

In addition to understanding the transient stress profiles in important regions of the device (i.e. the critical region at gate footprint and GCFP regions in the AlGaN layer), it is necessary to study the impact various RF operating conditions have on the stress values within AlGaN/GaN HEMTs. Vast combinations of frequency, duty cycle, and bias conditions are possible for these devices due to their high power and high frequency capabilities. Because of this, it is important to outline how the stress within these devices changes in response to altering the operating conditions. The goal of this chapter is to outline the impact each operating condition (frequency, duty cycle, and bias condition) have on the stress in the critical region of the device. It will be shown how the frequency and duty cycle impact only the thermoelastic stress values, while altering the electrical bias conditions drastically changes both the stress contributions by IPE and thermal effects.

4.1.1 Frequency Dependence

Frequencies within the range of 3 kHz to 300 GHz fall within the RF regime where GaN based devices are likely to dominate over preceding GaAs and InP technologies. Prior to wide spread integration, however, it is important to look into the impact frequency has on the operating stresses within these devices. Figure 35 outlines the thermoelastic, IPE, and total combined stress as well as the peak operating temperature as

a function of frequency. Here, the same 28 V_{ds} and -2.072 V_{gs} bias condition and 50% duty cycle from Chapter 3 are kept, while the frequency is increased from 1 kHz to 1 MHz. The stress values correspond to the critical region at the GFP position outlined in Chapter 3 (see Figure 31).

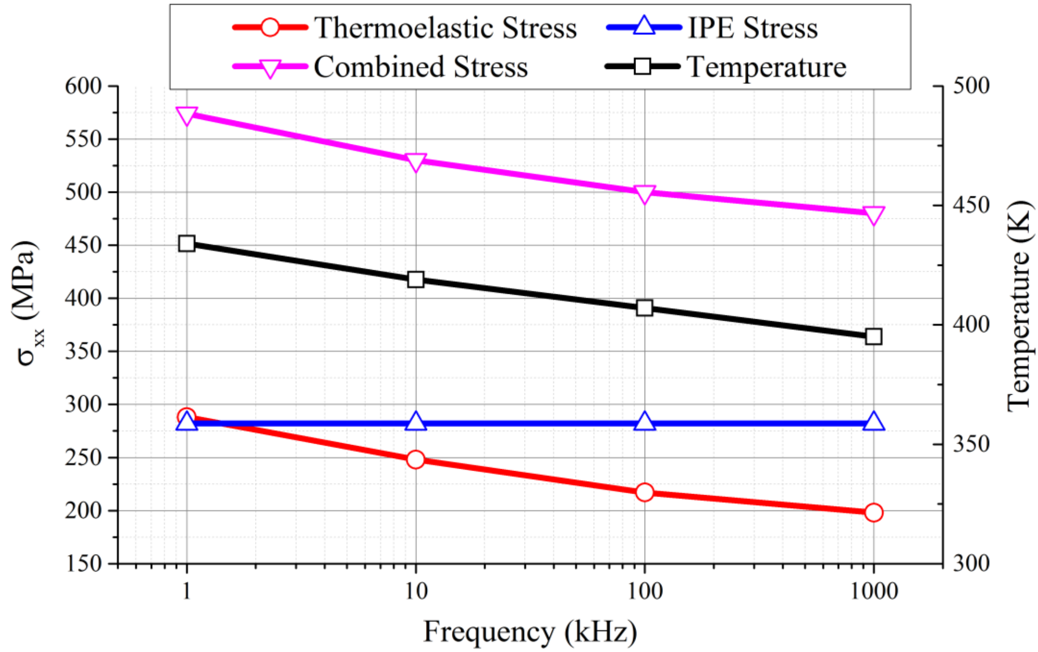

Figure 35. IPE, Thermoelastic, and Combined stress within the critical region of the device for various frequencies. Peak temperature decreases rapidly with increasing frequency.

Across the frequencies studied, a large drop (~40 K) in peak temperature is seen, which is directly dependent upon the pulse length where the device is powered in the ON-state. In response, the lower peak temperature induces less thermoelastic stress. From 1 kHz to 1 MHz, a 31% decrease (90 MPa) is seen in the thermoelastic stress around the critical region in the device. The stress induced by the inverse piezoelectric effect, however, remains constant and is independent of pulsing frequency. This is due to having the same bias conditions (and thus electrostatic potential within the piezoelectric materials) across any frequency range. Regardless of the pulsing frequency, the IPE stress will remain constant for fixed values of V_{ds} and V_{gs}, while the thermoelastic (and thus the total combined stress state) will decrease as the device is pulsed at higher rates.

Understanding stress profiles in addition to peak stress values across a wide range of frequencies is also important to understand transient failure mechanisms. Figure 36 represents the thermoelastic stress profile around the gate structure for (a) 1 kHz and (b) 1 MHz pulsing frequency at the end of the ON-state.

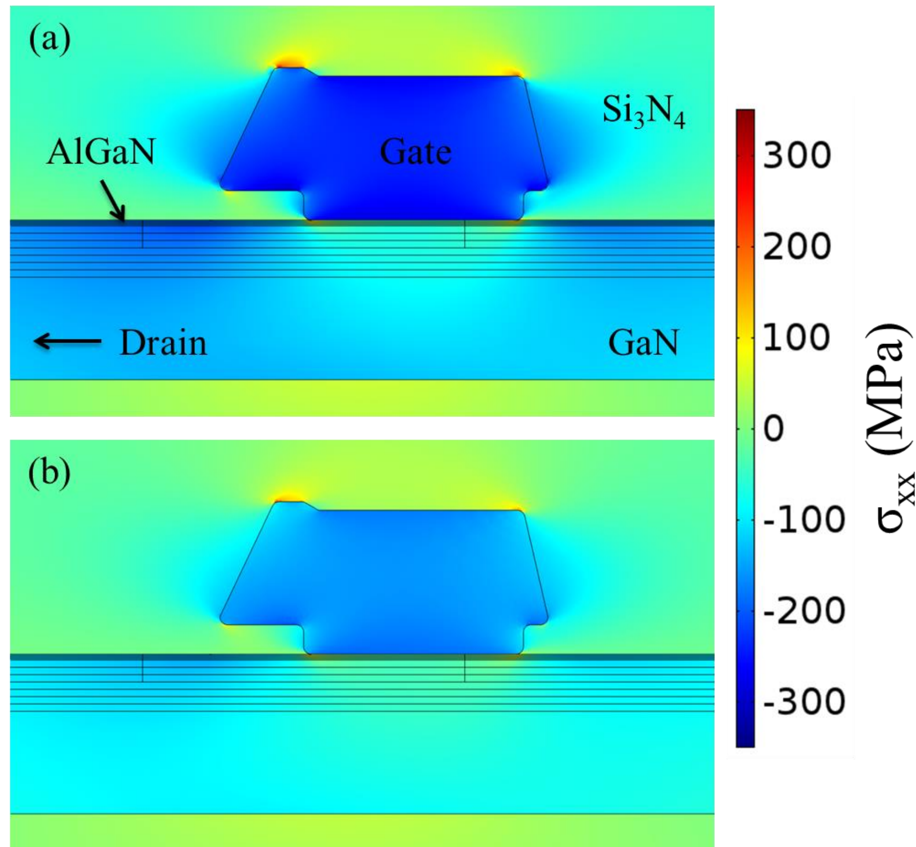

Figure 36. Thermal stress profile around the gate structure for (a) 1 kHz and (b) 1 MHz pulsing. The time corresponds to the end of the ON-state, where peak operating temperature is achieved.

Within the critical region, the same IPE stress develops (not shown) because of the equivalent bias conditions. For the thermoelastic stress, higher tensile stresses are seen in (a) around the gate footprint, while larger compressive stresses are seen in (a) within the AlGaN and GaN layers in the channel on the drain side of the gate, leading to a larger in-plane stress gradient between the drain and gate contacts (left side of the gate with reference to Figure 36). This is directly due to the different ON-state time for the longer pulsing frequency of 1 kHz and could play an important role in the onset of degradation

during transient operation, since the increased stress state is held at a longer period of time for slow frequencies.

4.1.2 Duty Cycle

Microelectronic devices in transient operation are also subjected to various duty cycles. Previous transient studies on insulated-gate bipolar transistors (IGBTs) have shown duty cycles can vary greatly depending upon the application, and the thermal effects due to varying duty cycle impacts the lifetime of the device [91]. IGBTs are three-terminal power semiconductor devices that are capable of fast switching operation similar to HEMTs. The authors of [91] contribute the failure and thus reduction in the power cycling lifetime of IGBTs to the peak operating temperature and thermal cycling (defined as a $\Delta T = T_{max} - T_{min}$ during cycling) induced by the various duty cycles studied. Similar studies, however, have not been performed to the knowledge of the author at the time of this work on GaN based HEMTs. Therefore, characterizing the stresses across a wide range of duty cycle conditions is important to understanding transient failure modes and to aid in understanding the amount of cyclic induced stress. Similar to Figure 35, Figure 37 represents the various contributions to stress within a GaN HEMT subjected to duty cycles between 1-50%. For consistency, the same 28 V_{ds}, -2.072 V_{gs}, and 100 kHz pulsing frequency operating conditions are used.

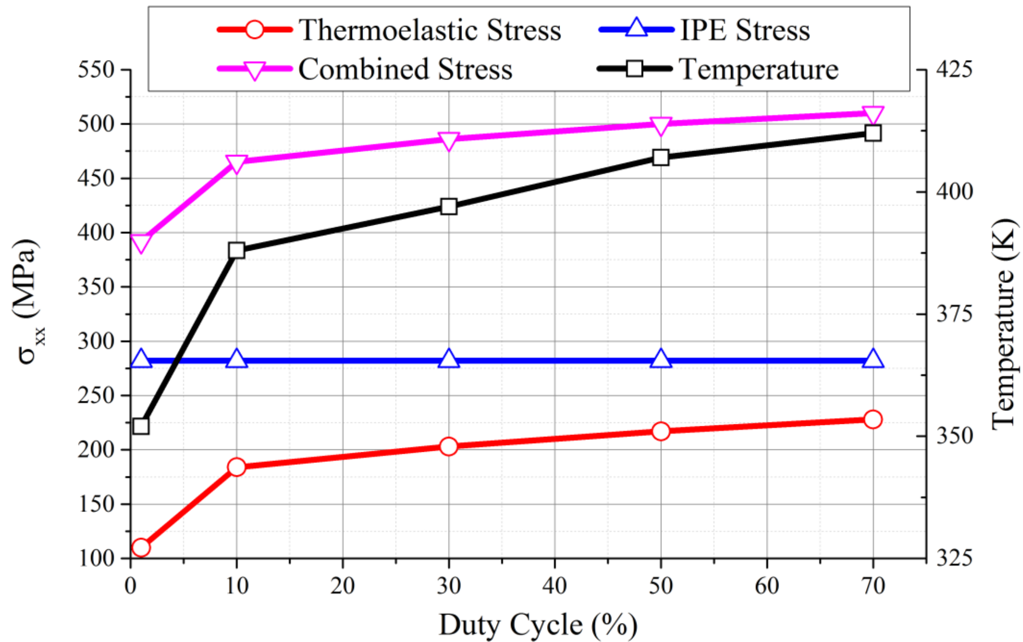

Figure 37. Impact of duty cycle on the IPE, thermoelastic, and combined stress values within the critical region of the device. Peak operating temperature is included to show the correlation between thermoelastic stress and temperature rise.

Similar to increasing frequency, longer duty cycles lead to larger peak operating temperatures and larger thermoelastic stress values, while the IPE stress contribution remains constant. IPE stress is directly dependent upon the applied bias conditions, which will be shown in the next section to greatly change across the standard operating voltages of V_{ds} = 10, 28, and 48 V for these devices. Increasing the duty cycle from 1 to 50% increases the thermoelastic stress value by 49% (~100 MPa) and increases the peak operating temperature by 55 K.

In addition to the peak values, the authors from [91] comment on the impact ΔT (temperature "swing") during cycling. Figure 38 shows the ΔT and the change in thermoelastic stress as a function of duty cycle.

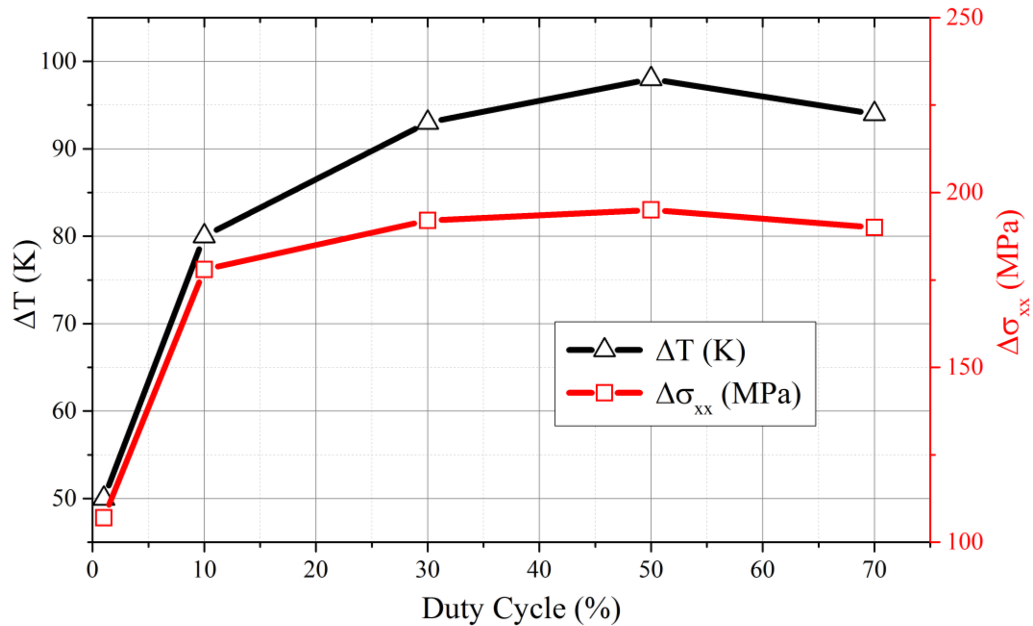

Figure 38. Temperature based upon duty cycle. The largest temperature swing occurs at 50%, where the heating and cooling cycles are have equivalent duration.

The largest ΔT is seen when a device is operated using a 50% duty cycle. This is because the ratio to ON-state to OFF-state is 1, leading to an equivalent amount of heating and cooling, thus causing the largest ΔT. Selection of an operating duty cycle is most likely application dependent, but it is important to understand the impact on stress within the device as the duty cycle is varied. In doing so, one gains an understanding to failure mechanisms within a device (i.e. thermal versus electrical degradation effects) if different failure mechanisms were seen across varying duty cycles.

4.1.3 Bias Dependence

The final transient condition studied is the bias dependence during cyclic operation. Because of their high power capabilities, GaN HEMTs are able to operate across a wide range of bias conditions. Specifically, GaN's high electric breakdown field allows for stable operation in excess of 48 V_{ds}. Depending on application and device size/structure,

this value can vary greatly. In addition, the bias dependent electrical response of devices across a wide range of V_{ds} values is often reported to determine the power added efficiency (PAE) of a power amplifier device [92]. Because of this, it is necessary to determine the stress values across a wide range of bias conditions within the transient regime. Figure 39 represents the transient stress values for DC power condition described in section 3.1.2 and in Figure 23 where an equivalent DC power of 6 Wmm^{-1} is dissipated. Again, the frequency and duty cycle are set to 100 kHz and 50%, respectively.

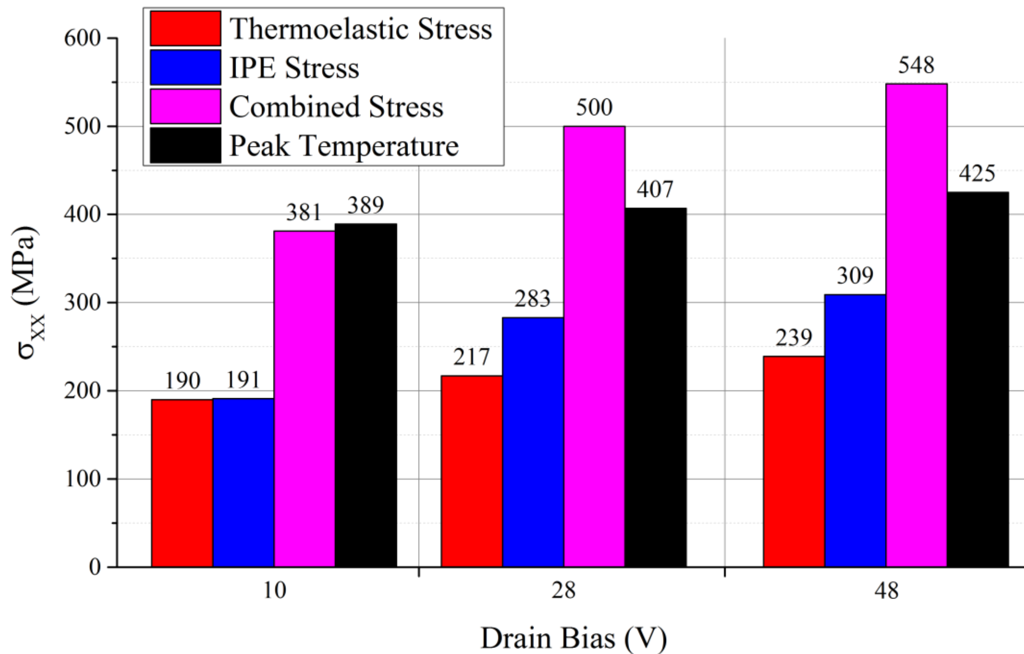

Figure 39. Bias dependence on the transient stress values for equal DC power dissipation. Altering applied bias changes both electrical and thermal stress profiles.

For the low drain bias case of 10 V_{ds}, the stress contributions due to the IPE and temperature gradient are nearly equivalent at ~190 MPa. As the drain bias is increased to 48 V, however, the IPE and thermoelastic stress increase steadily. This is because both the electrostatic potential due to the applied V_{ds} and V_{gs} combination is changing in addition to the Joule heating profile, causing higher temperature operation and larger IPE and thermoelastic stresses. For the 28 V_{ds}, the IPE stress is 30% greater than the

respective thermoelastic stress, and is 48% larger than the preceding 10 V_{ds} case. Also, the thermoelastic stress has increased by 14% over the 10 V_{ds} condition. When a 48 V_{ds} is applied, the IPE and thermoelastic stress states increase again, yielding a combined stress state that is 44% higher than the initial 10 V_{ds} case. Although operating GaN based HEMTs at these high bias conditions is possible, the reliability under transient operation may become an issue due to this increase in the overall stress state within the critical region of the device.

It should be mentioned the peak temperature for these conditions under transient operation is found to be higher than same bias conditions under DC operation. Under DC operation, V_{ds} = 10/28/48 V corresponds to a peak temperature of 391, 390, and 389 K, respectively, while the corresponding peak temperatures under transient operation are found to be 389, 407, and 425 K. For the 10 V_{ds}, the peak temperature under DC is approximately equal to the transient response. This is believed to be due to the extremely localized heating as a result of the rapidly changing electric field within the critical region (gate footprint) of the device (see Figure 23). As this heat generation region spreads with increasing V_{ds}, however, the heating is less localized. Under transient operation, the mobility of the 2DEG is higher than under DC operation because the thermal gradient along the 2DEG is lower, thus less current "droop" due to self-heating arises. Higher peak temperatures occur, but this is due to a higher possible P_{ds} under transient operation. Although the parameters are set to equal the DC dissipation, Figure 40 shows the transient drain power dissipation (P_{ds}) for the presented bias conditions at 100 kHz and 50% duty cycle are higher than the previous 6 Wmm^{-1}.

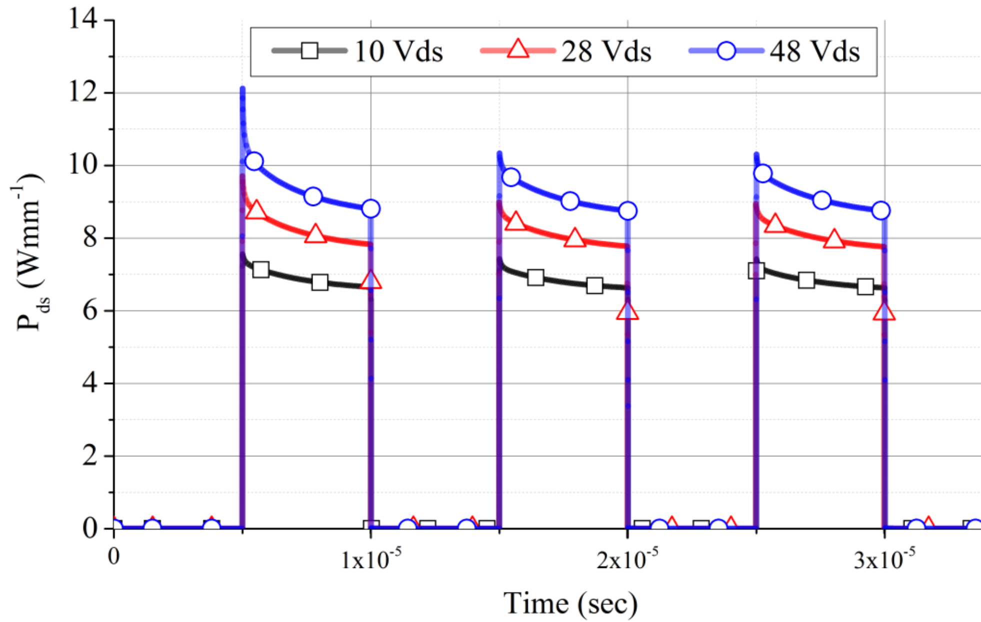

Figure 40. Transient power dissipation for different bias conditions. Because of the cooling during OFF-sate, higher Pds is achieved compared to DC operation.

Higher drain currents are achieved because of the cyclic heating and cooling. This, in turn, yields larger P_{ds} by the device. In fact, the same bias conditions presented in section 3.2.1 yield much higher P_{ds} because of the higher 2DEG mobility. This has been demonstrated experimentally in [7], where the DC versus transient operation and the impact of duty cycle on device performance was studied. Because of the Joule heating during the ON-state, the 2DEG mobility decreases which corresponds to a power "droop" in Figure 40 from the beginning to the ON-state to just before the start of the OFF-state.

In this parametric study, the impact of altering frequency, duty cycle, and bias conditions was studied across a wide range of values to reveal how stress changes within a device. Increasing frequency from 1 kHz to 1 MHz resulted in a 29% reduction in thermoelastic stress, but the IPE stress remained constant. Similar results were seen for various duty cycles. Increasing the duty cycle from 1 to 50% results in a > 70% increase in thermoelastic stress, while the IPE contribution remains constant. In both studies, the

IPE contribution to stress develops nearly instantaneously with applied bias and does not change with either frequency or duty cycle, but is rather a function of applied bias.

More complex changes occur when the bias conditions are varied. Changing the drain bias between 10 and 48 V was shown to have a large impact on the electrical profile (and thus Joule heating profile) within a device around the GCFP and GFP. As the V_{ds} is increased, the electric field around the GCFP is increased and has a large impact on the Joule heating profile. Combined, these changes result in an increased stress state for both the IPE and thermoelastic contributions to stress. The 10 V_{ds} case results in the lowest IPE (190 MPa) and thermoelastic (191 MPa) stress around the GFP. At 28 V_{ds} (48 V_{ds}), the IPE and thermoelastic increase to 283 and 217 MP (390 and 239 MPa), respectively. Based on these results, the operating conditions associated with an AlGaN/GaN HEMT greatly impacts the transient stress profiles. Therefore, it is necessary to characterize and understand the transient stresses in order to understand real-world application failure mechanisms.

CHAPTER 5 MODELING VERTICAL DISPLACEMENT UNDER TRANSIENT OPERATION

5.1 Experimental Test Explanation

One application of the developed modeling technique is to simulate the transient vertical deflection of a device under sinusoidal electrical bias inputs and compare the results to experimental measurements of deflection using an atomic force microscope (AFM) conducted at the University of Illinois at Urbana-Champaign. The developed experimental technique utilizes scanning Joule expansion microscopy (SJEM) to capture the vertical deflection of a 2-Finger AlGaN/GaN HEMT. SJEM is a form of scanning probe microscopy that is performed on an atomic force microscope platform. Figure 41 demonstrates the experimental setup for a SJEM system.

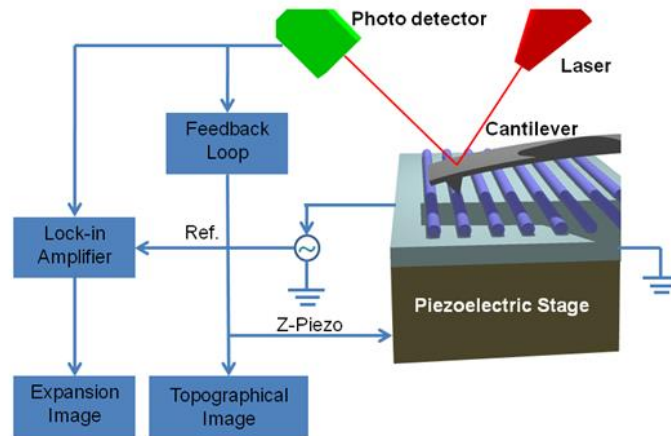

Figure 41. Demonstration of SJEM experimental setup. An AFM cantilever cantilever passes over a surface and the surface topography is captured via the photo detector [93].

During SJEM, an AFM cantilever scans over a surface and returns the topography via the photo detector. In these experiments, the device is operated at a constant V_{gs} value, while

the drain bias is run under a sinusoidal input. The cantilever is held at a fixed position during device operation, and records the deflection of the tip as the device deforms due to inverse piezoelectric (IPE) and thermal expansion effects. By characterizing multiple points within the channel of a device, one can determine localized heating, peak electric field concentrations, or highlight device defects.

Sinusoidal operating parameters for the device must be defined for clarity (a graphical representation is shown in Figure 42). In previous chapters, the device was operated under pulsing between an OFF-state, where V_{ds} was set to 0 V, and then rapidly switched to an ON-state, where the V_{ds} was rapidly transitioned to either 10, 28, or 48 V.

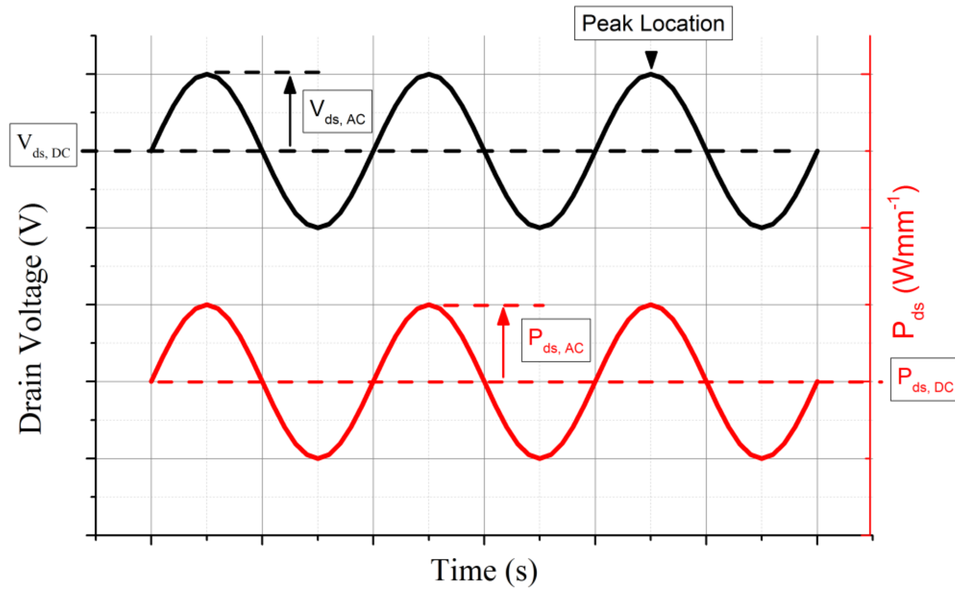

Figure 42. Sinusoidal drain input and power dissipation response.

Under sinusoidal input, the drain bias contains a DC offset, denoted $V_{ds,\ DC}$, and transient amplitude, denoted $V_{ds,\ AC}$. In response to the drain bias, the power dissipated by the device also contains a DC and AC component, denoted as $P_{ds,\ DC}$ and $P_{ds,\ AC}$, respectively. To be consistent with previous modeling efforts of Chapter 3 and Chapter 4, the gate bias was held constant to achieve the desired DC and AC power. In addition, the stress values

reported are consistent with the GFP location as shown in Figure 31, and are taken at the peak power dissipation during the transient cycle.

5.2 Gate Height and Thermal Boundary Resistance Sensitivity Analysis

Prior to a direct comparison of numerical simulation to experimental results, the sensitivity of the vertical displacement based on the gate height and the TBR at the GaN/SiC interface must be determined. Figure 43 depicts a representative device with the GCFP height labeled, and the TBR location is depicted in Figure 17. Both of these values can vary greatly depending upon device structure and manufacturing techniques and is therefore important to characterize their impact on vertical displacement.

5.2.1 Gate Height Dependence

The addition of a GCFP (also called a T-gate structure) is known to improve reliability within AlGaN/GaN devices by changing the distribution of the electric field and reduce the peak electric field seen at the GFP [8].

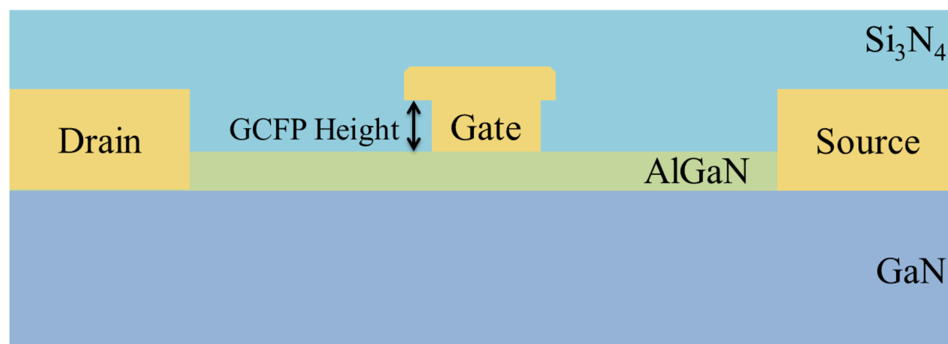

Figure 43. Graphical representation of the GCFP height. This value is varied from 0.10 to 0.06 µm to determine the impact of this gate height on the vertical displacement when a device is operated under a sinusoidal V_{ds}.

Although the simulations presented in this thesis are based upon SEM images of actual devices, resolutions on the order of nanometers are difficult to discern using this imaging technique, and this issue is compounded by the multiple layers of materials within the area of interest (i.e. the gate metallization stacks and thin AlGaN layer are difficult to discern). Therefore, it is important to characterize the impact the height of the GCFP will have on the temperature and stress profiles, in addition to the overall vertical displacement profile while undergoing sinusoidal drain biases.

Three heights of GCFPs are chosen to determine sensitivity: 0.06, 0.08, and 0.10 μm. Although these heights only vary by tens of nanometers, the relative proximity to the 2DEG and small feature sizes associated with semiconductor devices will alter the electric field around the gate structure, resulting in varying electric and thermoelastic stress profiles. For a proper comparison to previous simulations, the gate bias is held constant at -2.072 V and the drain is run under a sinusoidal input with the $V_{ds, DC}$ set 28 V, and $V_{ds, AC}$ +/- 2.60 V. These values are chosen to dissipate a DC component of 6 Wmm^{-1}, with an AC component of +/- 0.5 Wmm^{-1}. It should be noted that although the GCFP heights are changing, an insignificant amount of power dissipation difference is seen across these three cases for varying GCFP heights (< 1%). Figure 45 represents the (a) resulting vertical component of electric field profile along the AlGaN/GaN interface and the (b) spatial distribution of the horizontal component of electric field for the three selected gate heights. Similar to the bias dependence shown in Figure 23, lowering the gate height impacts the electric field within the AlGaN and GaN layers around both the GFP and GCFP.

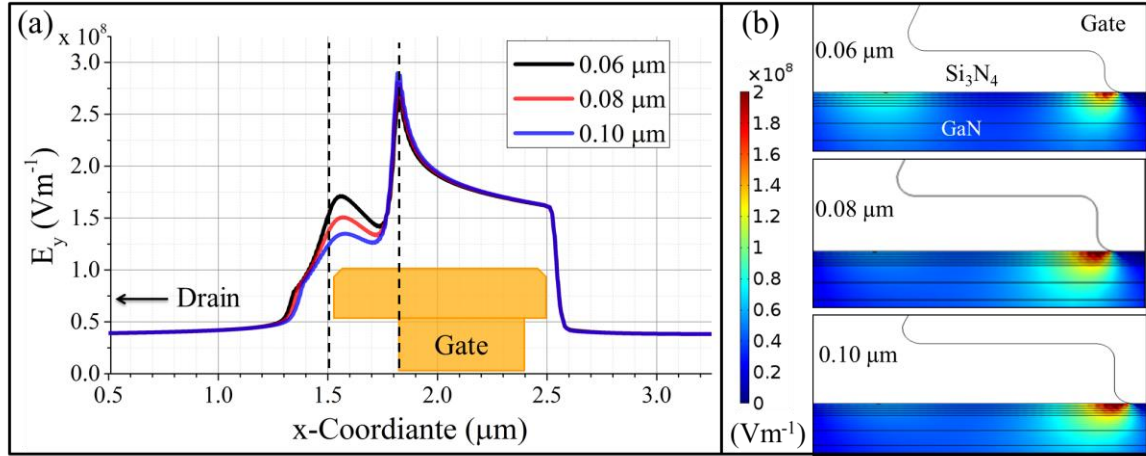

Figure 44. Gate height impact on the electric field distribution where (a) represents the distribution along the AlGaN/GaN interface and (b) is the spatial distribution on the drain side of the gate structure.

At the GCFP region, the local maximum in electric field decreases from 1.71 x 10^{-8} Vm^{-1} to 1.35 x 10^{-8} Vm^{-1} (a 21% reduction) when the height of the field plate is increased from 0.06 µm to 0.10 µm. Conversely, however, the global peak electric field increases from 2.68 x 10^{-8} Vm^{-1} to 2.89 x 10^{-8} Vm^{-1} (an 8% increase) when the field plate height is decreased from 0.10 µm to 0.06 µm. Electric field is reported in units of Vm^{-1}. For the previous bias dependence study (Figure 23), the voltage was increased to increase the electric field around the GCFP. Here, however, the distance is decreased to cause a similar change in electric field around the gate structure. As the electric field around the GCFP increases, less of a 2DEG concentration is seen at the GFP, resulting in a lower electric field in this area.

Altering the electric field around the gate structure directly impacts the Joule heating profiles. Figure 45 represents the (a) temperature distribution along the AlGaN/GaN interface and the (b) spatial distribution of the Joule heating profiles for the three GCFP heights. As the GCFP height is decreased, the local rise in electric field around the GCFP yields an increase in temperature at this location and changes the global maximum in temperature to a point located within the channel of the device between the gate and drain electrodes.

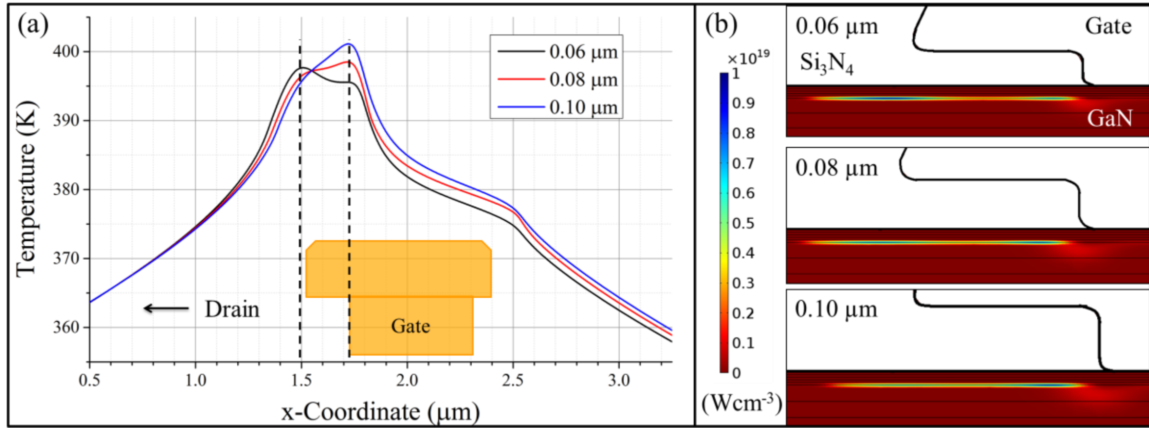

Figure 45. Resulting (a) temperature along the AlGaN/GaN interface and (b) Joule heating profiles. Differences in temperature and heat generation profiles are a direct result to changing electric fields for each gate height.

At the tallest GCFP height of 0.10 µm, the global peak temperature is seen near the GFP, where the electric field spike is highest. Lowering the GCFP from 0.10 to 0.06 µm causes the peak temperature to shift towards the drain by ~ 200 nm and reduces the global peak in temperature by ~ 19 K.

Because of the dissimilar electric and thermal profiles associated with the three GCFP heights, the stress values associated for each gate height varies (Figure 46). The 0.06 µm GCFP height yields the lowest IPE stress (267 MPa) due to a reduced global maximum in electric field around the GFP. This value increases by 5% (to 281 MPa) for the 0.08 µm GCFP height and 10% for the 0.10 µm (to 293 MPa) GCFP height.

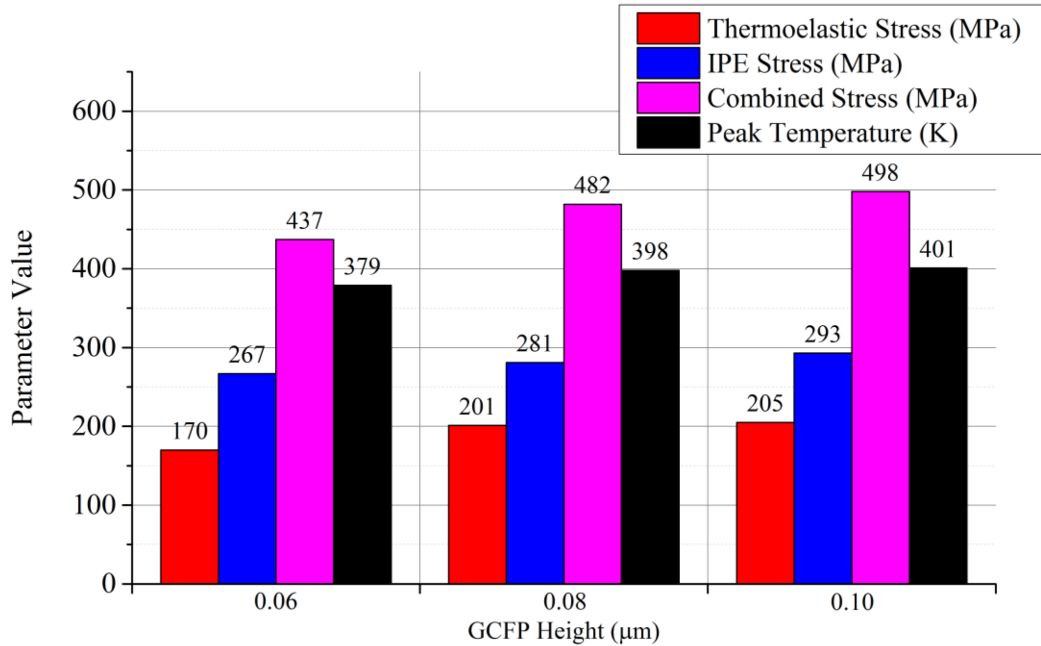

Figure 46. Peak stress values around the GFP for three GCFP heights. Both electrical and thermal stresses change with GCFP height.

Similar results are seen for the thermoelastic contribution of stress. The reduced peak temperature accompanying the 0.06 μm GCFP yields the smallest thermoelastic stress (170 MPa). The temperature increase associated with the 0.08 μm height yields an 18% increase in thermoelastic stress (201 MPa) seen at the GFP. The model calculates a nearly identical peak temperature value for the 0.08 and 0.10 μm GCFP heights (only a 3 K temperature difference), and thus the thermoelastic stress values are nearly identical (201 and 205 MPa, respectively). The major thermal difference between the three heights is the location of the peak temperature. At the tallest gate height, the peak temperature location is near the GFP and underneath the GCFP. At this region, multiple materials of different CTE values intersect, causing a sharp rise in thermoelastic stress when the peak temperature location is within close proximity to this area. Pushing the peak temperature away from this point (as is done with the 0.06 μm height) greatly reduces the stress concentration. Based on these results, reducing the GCFP height from 0.10 μm to 0.06 μm results in an overall reduction of 12% in the combined IPE +

thermoelastic stress state at the GFP. This is an important consideration and could be used as a design tool to manufacture more reliable devices.

The different electrical and thermal profiles also impact the vertical displacement of the device operating under transient conditions. Vertical displacement is taken as the average displacement the device undergoes during sinusoidal operation and is calculated through Equation (9) at individual points along the topography (Figure 20).

$$\frac{(S_{max} - S_{min})}{2} \tag{9}$$

This equation is used instead of maximum or minimum displacement values because the experimental data corresponds to this formulation for vertical displacement, which is important for proper comparison in a following section. Figure 47 represents the vertical displacement of the channel of the device for each GCFP height. The conformal topography and representative gate geometry are added for reference.

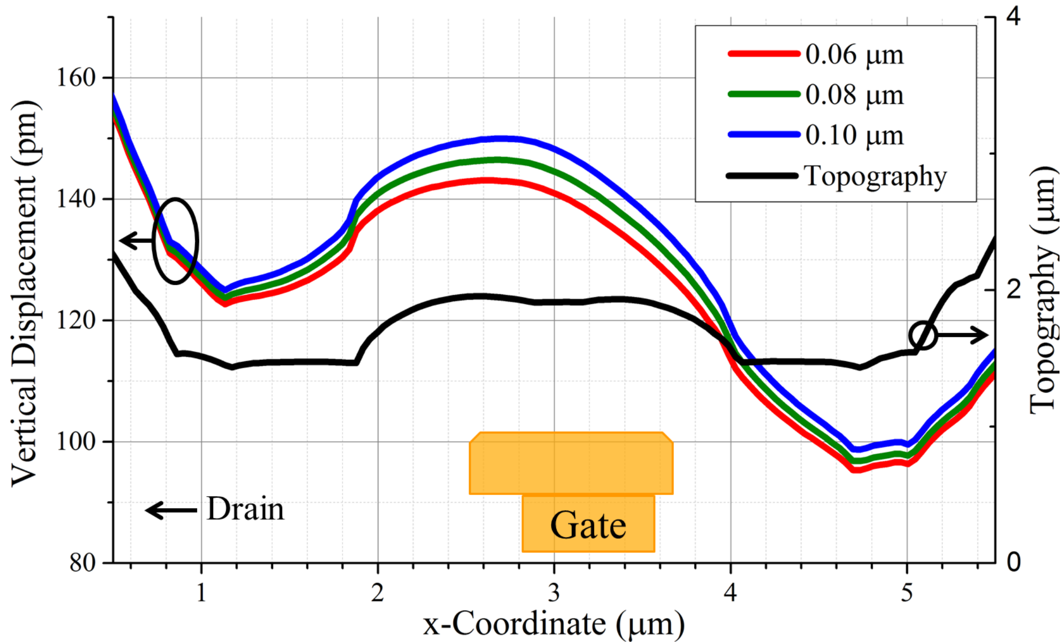

Figure 47. Vertical displacement for the three GCFP heights. Higher displacements are seen for taller gate structures.

The most vertical displacement is seen for the 0.10 μm height and decreases with decreasing GCFP height. Since the gate material has a high CTE, the peak vertical displacement is seen above the gate structure. The peak value of vertical displacement for the 0.06, 0.08, and 0.10 μm GCFP heights correspond to 143, 146, and 150 pm, respectively. Altering the GCFP height slightly changes the peak location of vertical displacement. The peak vertical displacement location shifts towards the drain with decreasing GCFP height (peak locations occur at 2.58, 2.66, and 2.70 μm for the 0.06, 0.08, and 0.10 μm heights, respectively). This is attributed to both the change in electric field and Joule heating profiles, which shift towards the drain with decreased GCFP height. Lowering the GCFP from 0.10 to 0.06 μm (40% reduction) yields < 5% drop in peak vertical displacement. Based on these results, it is clear the GCFP height impacts the vertical displacement, but only marginally for these operating conditions.

There are three factors to consider when modeling the vertical displacement of a device containing varying GCFP heights. First, the electrical profile changes in response to changing gate structure and thus the IPE response of the AlGaN and GaN layers are altered. Under higher electric fields, these materials will undergo more deflection, yielding a change in the vertical displacement simulated by the model. Second, the changing thermal profiles and varying CTE of materials will alter the vertical displacement. Where possible, the mechanics model utilizes temperature dependent CTE values (Table 3) and thus the changing thermal profiles will impact the vertical displacement directly. Finally, a GCFP height of 0.10 μm contains more gold than the other two modeled heights. This effect alone will change the vertical displacement profile because of the inclusion of additional high CTE material (gold). The developed model automatically accounts for all of these factors through the electro-thermal coupling Sentaurus Model, and within the COMSOL mechanics model to determine the transient vertical displacement. Based on the results from this and the next sections, device

parameters can be determined to accurately determine the vertical displacement of an actual device.

5.2.2 Thermal Boundary Resistance Dependence

The TBR imposed at the GaN/SiC has a range of reported values between 4 and 60 m^2KGW^{-1} [77, 78, 80, 82, 94]. Heller *et al.* [33] reports a temperature dependent average of results from [80] and a constant value of low resistance from [94] of 1.2 m^2KGW^{-1}. This parameter can greatly impact the peak temperature and thus the vertical displacement a device undergoes during transient operation. Four TBR values are chosen to study the impact this value has on the model. Three values of 0, 30, and 60 m^2KGW^{-1} are chosen to represent a range of conductive interfaces from high to a low conductivity layers. The fourth value is the temperature dependent TBR taken from [33] and is represented through Equation (10).

$$TBR\ [\mathrm{m^2KGW^{-1}}] = 15 + \frac{(T-273)}{10} \tag{10}$$

where T is the lattice temperature at the GaN/SiC interface in Kelvin. As before, the same 28 V_{ds}, -2.072 V_{gs}, and 100 kHz pulsing frequency under a sinusoidal input are used as the operating conditions. Because of the electro-thermal coupling, the gate voltage was changed slightly for each case to dissipate equivalent power across the four TBR values tested, but this change was not seen to alter the IPE stress greatly (Figure 48).

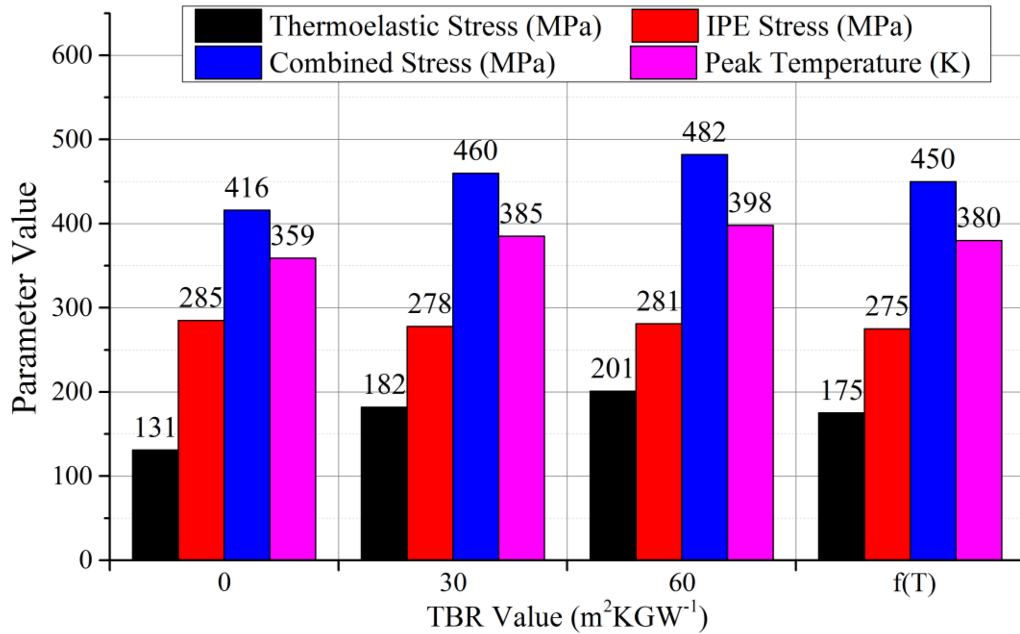

Figure 48. Stress values and peak operating temperature as a function of imposed TBR value. Altering TBR changes the peak operating temperature.

Because of similar temperatures for the 30 m^2KGW^{-1} and temperature dependent TBR from [33], these conditions contain nearly identical stress and peak temperature values. Comparing the other two cases, the peak operating temperature, thermoelastic stress, and overall combined stress within the device change greatly when the TBR increases from 0 to the low-conductivity 60 m^2KGW^{-1}. The 60 m^2KGW^{-1} increases the peak operating temperature by nearly 40 K compared to the perfect interface where no TBR value is imposed. Figure 49 shows the temperature distribution underneath the gate and within the device channel for the (a) 0 and (b) 60 m^2KGW^{-1} TBR simulations.

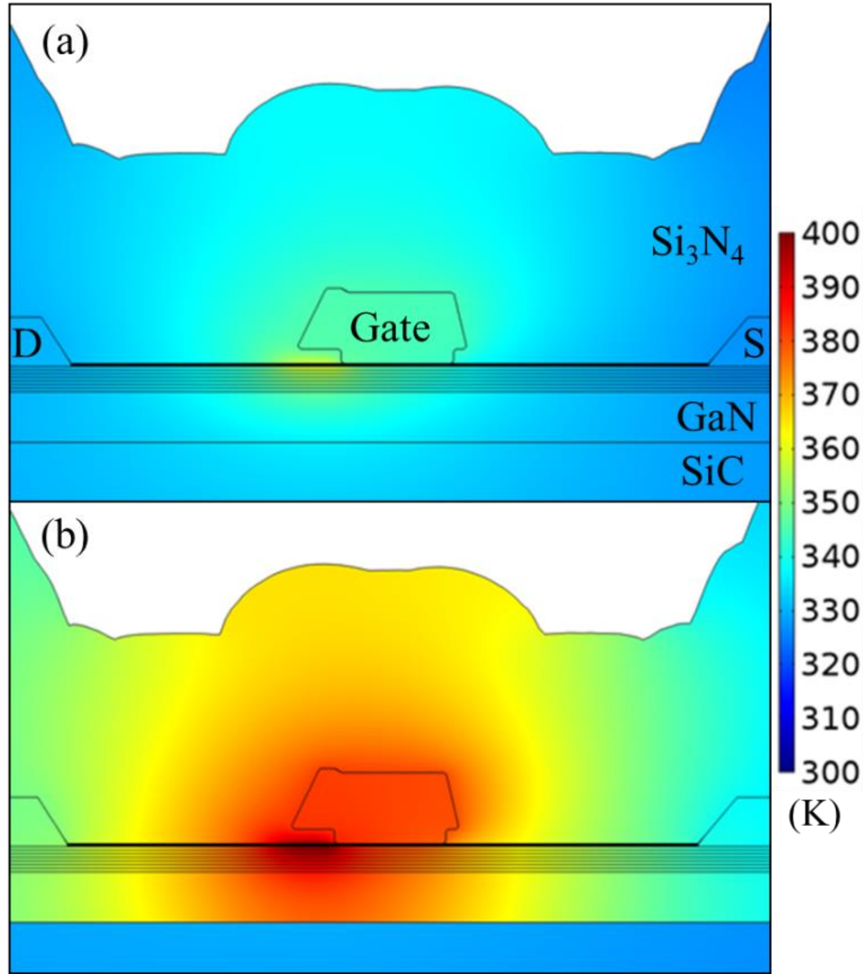

Figure 49. Spatial temperature distribution for the (a) 0 and (b) 60 m^2KGW^{-1} TBR values at the GaN/SiC interface. High value of TBR causes larger peak operating temperatures and more lateral heat spreading.

The imposed TBR causes a high resistance for heat to spread downwards into the SiC substrate and instead must spread laterally through the lower *k*-value GaN. Because of thermal expansion effects, the higher operating temperature associated with the 60 m^2KGW^{-1} TBR yields much higher vertical displacements (Figure 50), especially compared to the 0 TBR case.

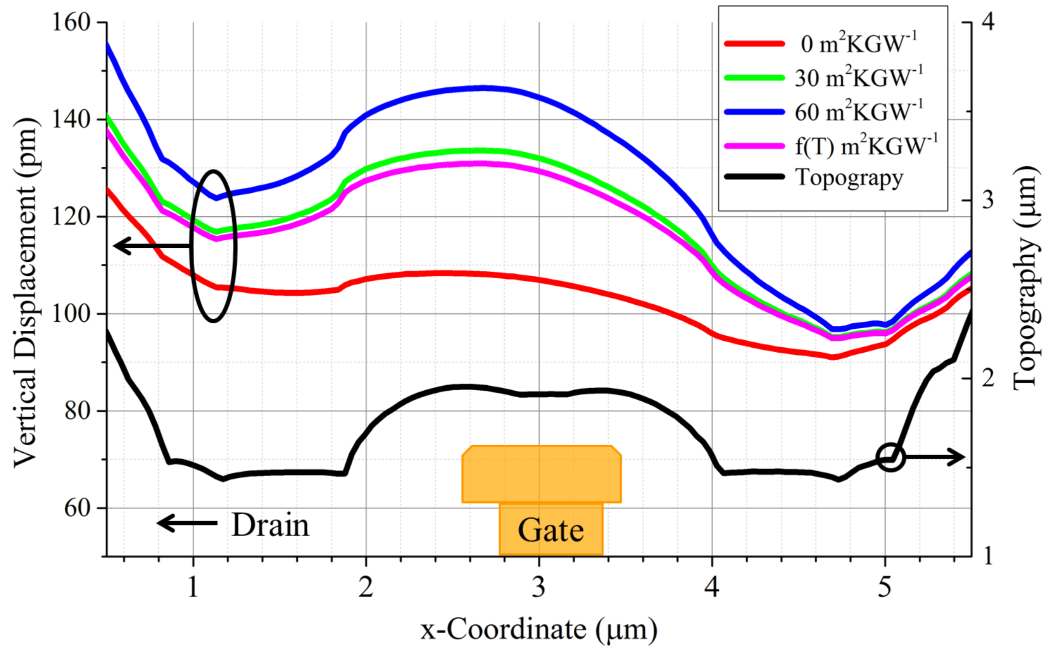

Figure 50. Vertical displacement of the device due to varying the TBR imposed at the GaN/SiC interface. TBR has a large impact in overall displacement due to higher operating temperatures.

Unlike the changing the GCFP height, the TBR greatly influences the vertical displacement profile around the gate structure. Due to similar temperatures and stresses, the 30 m^2KGW^{-1} TBR and the temperature dependent TBR cases are nearly identical. Between the 0 and 60 TBR cases, however, the vertical displacement increases by 35% from 108 pm to 146 pm. This large change in displacement between the reported TBR values creates a need to match this parameter to experimental results prior to direct comparison.

Understanding the thermal and mechanical impact of the interface resistance is critical for designing more reliable devices. If, for example, a perfect interface could be made between the GaN and SiC substrate, one would expect better performance and reliability due to the reduced stress state at the GFP and lower junction temperature within the device as demonstrated by Figure 48. In addition to a lower peak temperature, the temperature gradient around the gate structure greatly changes with a reduce TBR,

leading to higher electron mobility throughout the device channel, and thus better electrical performance.

5.3 Impact of Operating Condition on Vertical Displacement

Understanding the gate height and TBR impact on vertical displacement, the model can be adjusted to better match experimental data for vertical displacement profiles. Based on the results from the previous sections, a GCFP height of 0.08 μm and a TBR of 10 m^2KGW^{-1} are used to compare to experimental results. Chapters 3 and 4 have already demonstrated the impact bias conditions and operating frequency have on electrical and Joule heating profiles, and this chapter will demonstrate their impact on the vertical displacement of a device. A comparison to experimental vertical displacement measurements is performed to further demonstrate the versatility and provide verification of the developed electro-thermo-mechanical model.

5.3.1 Bias Dependence

Figure 23 showed the bias dependent electrical and Joule heating profiles under DC operation, and Figure 39 showed how these bias-dependent effects alter the stress profiles associated with a device. Here, the vertical displacement is simulated and compared to experimental results for three bias conditions. Table 5 summarizes the bias conditions used for the experimental/numerical comparison. These conditions are selected to dissipate a DC component of 5.5 Wmm^{-1} with a transient +/- 0.5 Wmm^{-1}. The slight differences in power are accounted for by normalizing the vertical displacement values around the $P_{ds,\,DC}$ value.

Table 5. Transient operation conditions for model comparison.

$V_{ds, DC}$ [V]	$V_{ds, AC}$ +/- [V]	V_{gs} [V]	$P_{ds, DC}$ [Wmm^{-1}]	$P_{ds, AC}$ +/- [Wmm^{-1}]	Frequency [kHz]
10.0	0.87	-0.38	5.58	0.510	210
28.0	1.95	-2.20	5.63	0.515	210
48.0	2.62	-2.63	5.64	0.535	210

For comparison, the model is set to dissipate the equivalent DC and AC component of power for the V_{ds} and V_{gs} combinations values listed in Table 5. Figure 51 shows the simulated and experimental vertical displacement values for points along the channel of the device.

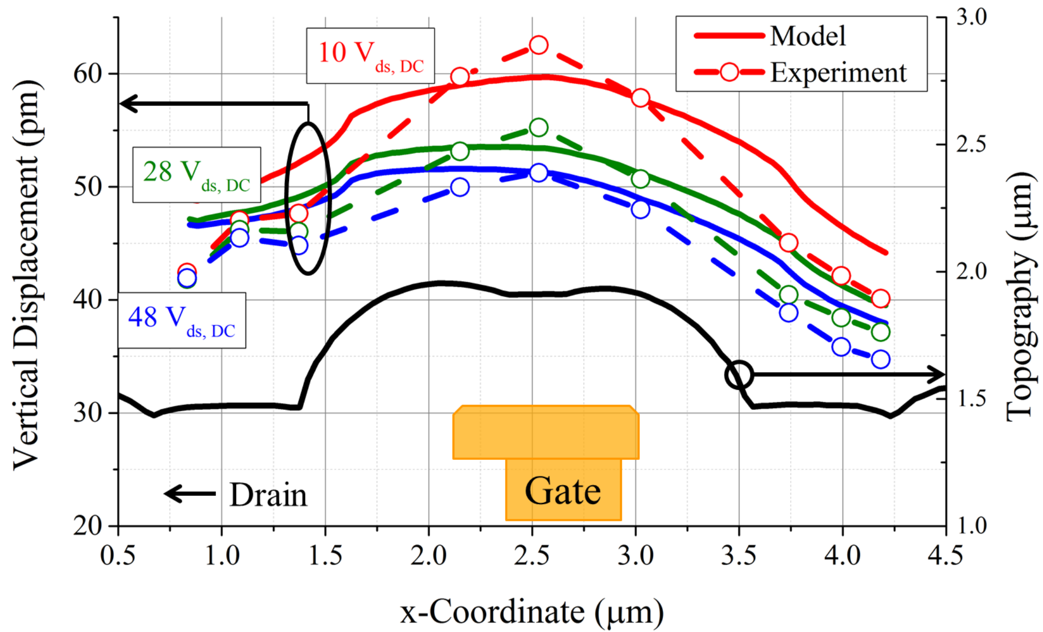

Figure 51. Bias dependence on the vertical displacement of a device. Altering bias conditions changes the electrical and thermal profiles, resulting in a change in vertical displacement.

Lines are added between experiment points for clarity. Relatively good agreement is seen between the developed model and experiments (< %5 difference) across these bias conditions. The largest displacement is seen for the 10 $V_{ds, DC}$ case and decreases with increasing drain bias. In addition to good overall agreement, the relative change between bias conditions is consistent between the simulations and experiments. A ~ 11%

reduction in vertical displacement is seen in both the experiments and simulations when the $V_{ds,\,DC}$ increases from 10 to 28 V. An even larger drop in vertical displacement is seen for the 48 $V_{ds,\,DC}$ condition (~18% experimentally, 14% numerically). This is due to the localized heating associated with this low drain bias condition, and heat spreading as the $V_{ds,\,DC}$ is increased (see Figure 23).

In addition to the thermal effects, the electrical profiles are also changing between each bias condition. Each condition has a different $V_{ds,\,DC}$ offset *and* periodic voltage to dissipate the same transient power. As $V_{ds,\,DC}$ increases, $V_{gs,\,DC}$ is decreased to dissipate an equivalent power, and in this more pinched-off state a larger $V_{ds,\,AC}$ is required to dissipate the same amount of transient power. It was found that the electrical profiles have a small impact on the vertical displacement compared to the thermal effects, and thus fitting the model to the imposed TBR value allows for good agreement across a wide range of bias conditions.

5.3.2 Frequency dependence

Figure 35 from Chapter 4 revealed changing frequency impacted the overall thermoelastic stress within the system, while the electrical contribution to stress remained constant. A similar response is seen for the vertical displacement characterization under sinusoidal inputs, as the vertical displacement is predominantly characterized by thermal effects. Because of this, it is important to characterize the impact frequency will have on vertical displacement. The IPE displacement will remain constant with fixed bias conditions across a range of frequencies (55 to 400 kHz for this comparison), while the changing thermal profiles will manifest as a change in vertical displacement. Figure 52 shows the simulated and experimental vertical displacement measurements for various

frequencies. Here, the 28 $V_{ds, DC}$ bias conditions and TBR value of 10 m^2KGW^{-1} are held constant while the frequency is set to 55, 110, 210, and 400 kHz.

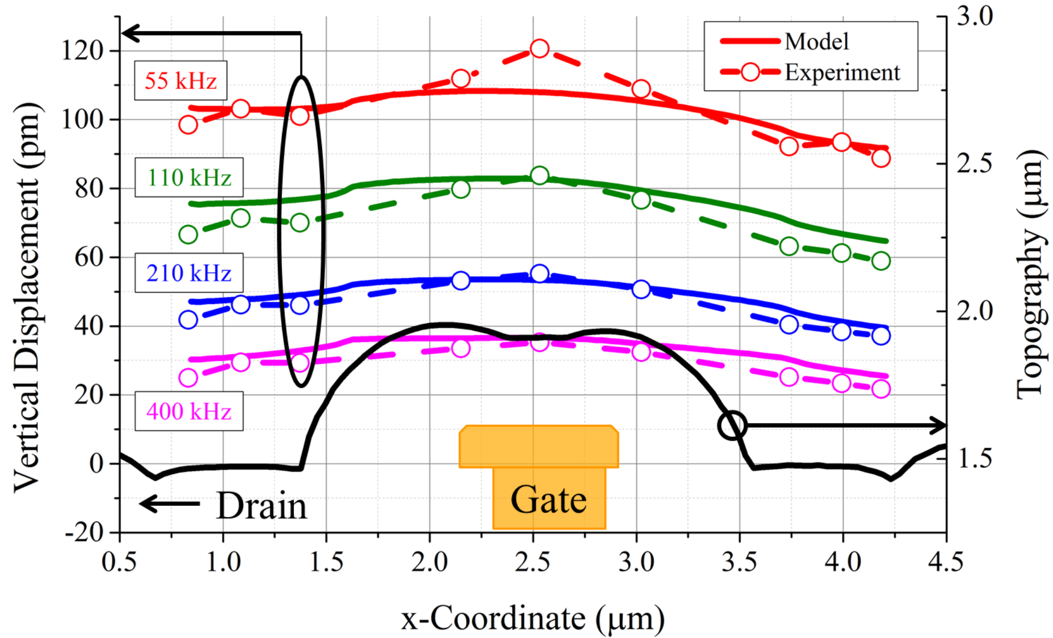

Figure 52. Frequency impact on vertical displacement. A large reduction in vertical displacement is seen as frequency increases from 55 to 400 kHz.

Increasing the operating frequency from 55 to 400 kHz results in a 68% reduction in peak vertical displacement. Here, increasing the frequency decreases the amount of heat spreading, leading to lower transient vertical displacement. In fact, at the 400 kHz case, the profile around the gate structure is nearly flat throughout the channel, indicating uniform vertical displacement during device operation. As frequency decreases to 55 kHz, the peak amplitude location (corresponding to directly over the gate structure) begins to see much higher deflections, and the model begins to under predict the peak deflection seen at this point. Across these frequencies, however, a good agreement is seen between the developed model and experiments, giving confidence to the model's ability to effectively account for the various possible operating conditions for a device.

The simulated and experimental results are the first demonstration of the vertical displacement a device undergoes during transient operation. Both GCFP height and the

imposed TBR were found to impact the vertical displacement, and are therefore important design considerations for AlGaN/GaN HEMTs. The GCFP height marginally affects the vertical displacement, while the TBR value greatly changes the vertical displacement. It was shown a GCFP height of 0.08 μm and a TBR value of 10 m^2KGW^{-1} yield excellent simulation/experimental matching across a wide range of bias conditions and frequencies, giving confidence to the developed model's ability to effectively determine the combined electro-thermo-mechanical response of a device. Further investigation into device deformation could aid in understanding transient failure mechanisms and detail how they vary from failure mechanisms seen under DC power.

CHAPTER 6 CONCLUSION AND FUTURE WORK

6.1 Summary of Results

The presented finite element model is a comprehensive and versatile tool capable of characterizing AlGaN/GaN HEMTs under DC and AC operation. Previous modeling efforts fall short by either neglecting electrical effects, make unrealistic Joule heating profile assumptions, or do not incorporate sufficient structural detail such as a conformal Si_3N_4 layer or accurate gate structure to properly characterize a device's response to various inputs. This model was used to determine the combined electro-thermo-mechanical response of a device subjected to various DC and RF conditions including bias condition, duty cycle, and frequency using the commercially available COMSOL Multiphysics. It was shown the developed model can achieve high accuracy compared to experimental electrical and mechanical data across a broad range of operating conditions and is therefore a useful instrument to understanding devices powered using both DC and AC power schemes.

Previous AlGaN/GaN HEMT simulations have focused primarily on either average stress within the GaN layer or reported peak stress values around the gate structure while operated under DC power. Here, it was demonstrated more complex stress profiles develop within AlGaN/GaN HEMTs under transient operating conditions. First, under OFF- to ON-state pulsing, the electrical stress develops rapidly with applied bias, while the thermoelastic stress builds during the ON-state of a device. Areas of interest including at the GFP and near GCFP within the device channel undergo vastly different transient stresses due to the electrical and thermal profiles. At the GFP, the electrical and thermoelastic stresses are tensile, resulting in an extremely localized concentration of tensile stress that is suspected to cause reliability issues for these devices. At the GCFP,

however, the electrical stress is tensile while the thermoelastic is compressive, leading to an overall relaxed stress state in this area of the device. Even though these locations are close in proximity, high stress gradients develop between these points. Under transient operation, these points undergo heavy amounts of cyclic loading, which could induce failure mechanisms not seen under DC operating conditions, where most of the reliability studies have been performed.

Once the transient stress characteristics were detailed, a parametric study of frequency, duty cycle, and bias condition was performed across a wide range of values to reveal how stress changes with operating condition. Increasing frequency from 1 kHz to 1 MHz resulted in a 29% reduction in thermoelastic stress, but the IPE stress remained constant. This is due to each frequency having the same electrical bias, but increasing frequency reduces overall temperature and heat spreading, resulting in a lower thermoelastic stress around the GFP. Similar results were seen for varying device duty cycle. Increasing the duty cycle from 1 to 50% results in a > 70% increase in thermoelastic stress, while the IPE contribution to stress remains constant. Here, the IPE develops nearly instantaneously with applied bias and does not change with either frequency or duty cycle, but is entirely a function of applied bias.

Altering bias conditions impact both electrical and thermal profiles, resulting in a change in electrical and thermoelastic stress around the GCFP and GFP when the drain bias is varied between 10 and 48 V. As the V_{ds} increases, the electric field around the GCFP rises and has a large impact on the Joule heating profile. Combined, these changes result in an overall increase in stress state for both the IPE and thermoelastic contributions to stress. The 10 V_{ds} case results in the lowest IPE (190 MPa) and thermoelastic (191 MPa) stress states around the GFP. At 48 V_{ds}, the IPE and thermoelastic increase to 390 (+ 105%) and 239 (+ 25%) MPa, respectively.

After characterizing the device's electro-thermo-mechanical response to various operating conditions, a direct comparison to experimental vertical displacement

measurements was performed. This work is the first attempt to characterize the transient vertical displacement of an AlGaN/GaN device under a wide range of possible operating conditions. It was found bias conditions have a large impact on the overall vertical displacement of the device operating with a sinusoidal drain bias. At equal transient power dissipation, a 10 $V_{ds, DC}$ case induces large vertical displacements due to highly localized heating, while increasing the drain bias to 28 V (48 V) yields an 11% (14%) reduction in vertical displacement. This is largely due to thermal effects, since the Joule heating profile is less concentrated around the GFP area with increasing drain bias. Frequency was also shown to greatly impact vertical displacement. From the modeling, increasing the frequency from 55 kHz to 400 kHz lowered the peak vertical displacement by 68%. Good qualitative and quantitative matching is seen between the developed model and experiments, giving confidence to the model's ability to effectively mimic an actual device.

In this work, a detail study of the transient operation of AlGaN/GaN HEMTs has been performed. It is critical to understanding operating characteristics such as electrical and thermal profiles and their impact on the overall stress states within a device. Understanding transient stress profiles is necessary to illustrate and understand transient failure mechanisms.

6.2 Future Work

Finite element modeling is a powerful tool to detail the behavior of an AlGaN/GaN HEMT. One limitation of the presented method, however, is the level of accuracy requires dense meshing strategies, which greatly increase the computational power and time required to perform transient analysis. Because of this, future modeling attempts should be built around developing a faster and more efficient modeling strategy through

either incorporating compact modeling or development of analytical solutions for a reduction in computation time. In doing so, one could quickly generate large parametric studies involving operating conditions or structural changes to a representative device. Another aspect of the developed model that could be improved upon is the coupling between Sentaurus Device and COMSOL Multiphysics. Currently, data is output from Sentaurus Device and is transferred to COMSOL. To eliminate this, a single, all inclusive model should be developed that fully incorporates the mechanical response directly, instead of needing a second modeling program. If done properly, the direct coupling between the mechanical response and the electrical characteristics of a piezoelectric material could also be included. Meaning, as the device heats and expands (or contracts), the change in residual stress or the 2DEG charge could be accounted for to provide better modeling accuracy. A final modeling element that should be included is the ability to account for transient degradation due to cyclic loading of the device. It was demonstrated large amounts of cyclic stress develop under typical transient conditions, which may induce failure mechanisms that vary from previous DC reliability studies.

In addition to enhancing the model's capabilities, a large amount of additional experimental work is needed to properly understand transient failure mechanisms. It was shown complex transient stress profiles occur and are largely influenced by electrical bias, frequency of operation, and duty cycle. Therefore, an important future step for this work is to validate the simulated stress results experimentally through optical probing techniques such as Raman spectroscopy. Future experimental studies could reveal new failure mechanisms in addition to those currently detailed in literature under DC operation, leading to improved device design and overall reliability. The vertical displacement experimentation could also be expanded upon to characterize device degradation. For example, a device could be characterized using SJEM and then degraded using DC stress tests. If mechanical degradation has occurred, then the SJEM results would show different vertical displacements.

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