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Bi-Directional Vector Variable Gain Amplifier for an X-Band Phased Array Radar Application

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BI-DIRECTIONAL VECTOR VARIABLE GAIN AMPLIFIER FOR AN X-BAND PHASED ARRAY RADAR APPLICATION

A Thesis Presented

by

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ABSTRACT

BI-DIRECTIONAL VECTOR VARIABLE GAIN AMPLIFIER FOR AN X-BAND PHASED ARRAY RADAR APPLICATION

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Directed by: Professor Robert Jackson

This thesis presents the design, layout, and measurements of a bi-directional amplifier with variable vector (in-phase / quadrature) gain control that will be part of an electronically steered phased array system. The electronically steered phased array has many advantages over the conventional mechanically steered antennas including rapid scanning of the beam and adaptively creating nulls in desired locations. The 10-bit bi-directional Vector Variable Gain Amplifier (VVGA) is part of the transmit and receive module of each antenna element where transmit and receive functionality is determined through a simple switch. The VVGA performs amplification of the IF IQ pair by an adjustable complex coefficient. At receive, the VVGA functions as a Vector Variable Gain Current Amplifier (VVGCA) and at transmit, the VVGA functions as a Vector Variable Gain Transadmittance Amplifier (VVGTA). Design procedure, layout entry, schematic and parasitic extracted simulation results, and measurements are presented in this thesis.

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LIST OF ABBREVIATIONS

VGA	----------	Variable Gain Amplifier
VGCA	----------	Variable Gain Current Amplifier
VGTA	----------	Variable Gain Transadmittance Amplifier
VVGA	----------	Vector Variable Gain Amplifier
VVGCA	----------	Vector Variable Gain Current Amplifier
VVGTA	----------	Vector Variable Gain Transadmittance Amplifier
CG	----------	Common Gate
CS	----------	Common Source
CMFB	----------	Common Mode Feedback
NF	----------	Noise Figure

CHAPTER 1

INTRODUCTION

1.1 Motivation and System Overview

The aim of this project is to design a bi-directional amplifier with variable vector (in-phase / quadrature) gain control that will be part of an electronically steered phased array system. The electronically steered phased array has many advantages over the conventional mechanically steered antennas including rapid scanning of the beam and adaptively creating nulls in desired locations. Elimination of mechanical steering resolves the problem of inertia and reduces system weight and power consumption. Moreover, presence of numerous antenna elements yields better system reliability as failure of a few elements will not result in complete system failure but merely degrades system performance [1].

An application of the electronically steered phased array antenna could be replacement of the Doppler weather radar network, or Next Generation Radar (NEXRAD), currently deployed in several locations across the United States and operated by the National Weather Service to detect precipitation and atmospheric movement. [2] The high power, long-range Doppler radars have limited ability to observe the lower part of the atmosphere due to earth's curvature. With current technology, one in five tornados goes undetected and 80% of all tornado warnings turn out to be false alarms. The NSF Engineering Research Center (ERC) for Collaborative Adaptive Sensing of the Atmosphere (CASA) is researching a new weather hazard

forecasting and warning technology based on low-cost, dense networks of short-ranged radars that adjust sensing strategy in response to evolving weather and to changing end-user needs. The proposed CASA networks are physically smaller than currently deployed radars, making them easier to install. The densely populated network allows for a more comprehensive mapping of weather fluctuations and eliminates range limitations of the current NEXRAD network. [2]

An example architecture for an electronically steered phased array system is suggested in [1]. Figure 1 depicts a row-column planar array where radiating elements are spaced uniformly in the x and y directions.

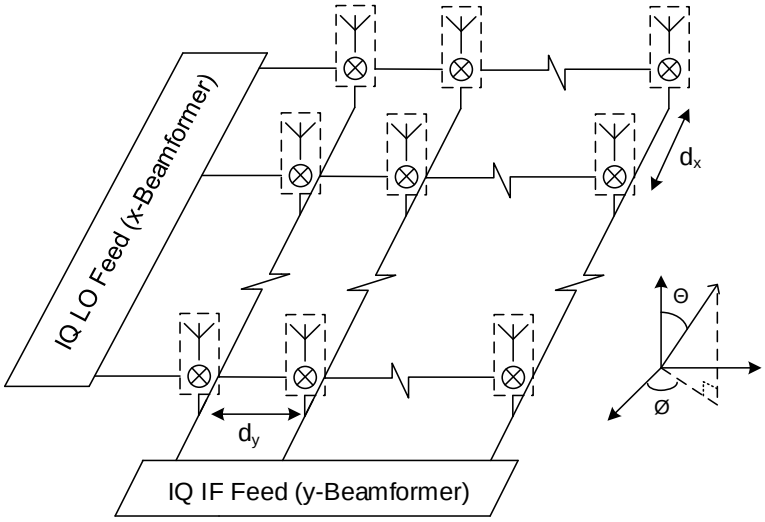

Figure 1. Series fed row-column planar array geometry

For a sufficiently large number of elements, it can be shown that the progressive phase shifts between rows x and columns y necessary and sufficient to steer the main beam in the direction $\theta = \theta_0$ and $\emptyset = \emptyset_0$ is [1]:

$$\beta_x = -kd_x \sin\theta_0 \cos\emptyset_0 \qquad \text{(Eq. 1.1)}$$

$$\beta_y = -kd_y \sin\theta_0 \sin\emptyset_0 \ ^1 \qquad \text{(Eq. 1.2)}$$

In Figure 1, the rows are fed with signals from a local oscillator (LO), the columns are fed with Intermediate Frequency (IF) signals, and the row-column product is obtained thru the use of mixers at each antenna element. The advantage of distributing IF and LO signals is the elimination of impacts such as signal loss and manufacturer tolerances associated with distribution of high frequency signals throughout the array.

The proposed Vector Variable Gain Amplifier (VVGA) introduced in this thesis provides phase shift at each element, as well as compensation for random phase and magnitude errors at each individual array element. Figure 2 depicts the transceiver block diagram containing the VVGA that corresponds to each single array element in Figure 1:

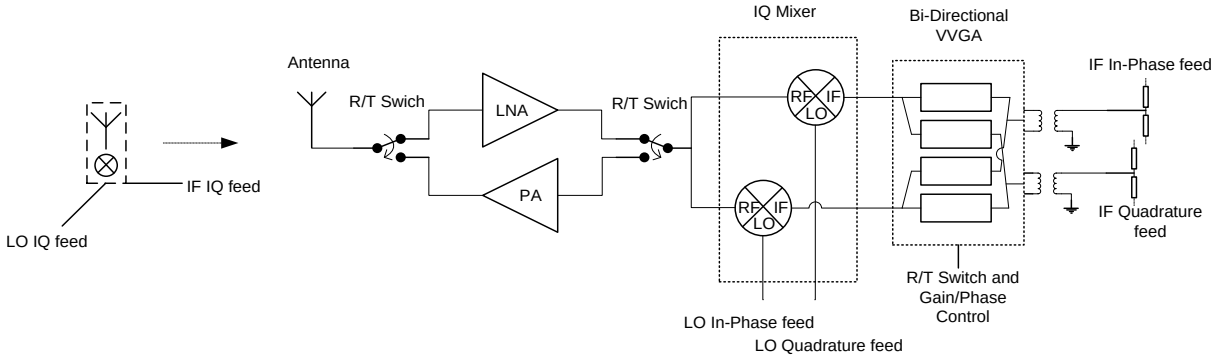

Figure 2: Transceiver block diagram

[1] Value of constant k is dependent on radiation wavelength λ

The basic building block of any electronically steered phased array is the receive and transmit module for each antenna element. The module typically contains a low noise receiver, power amplifier, and digitally controlled phase and gain elements. Distribution of LO and IF signals, requires addition of mixers and on-chip LO signal generators to the transceiver module. The objective of this project is to design a bi-directional VVGA where phase shift and phase and gain adjustments of the IQ IF signal is achieved, and where transmit and receive functionality are determined through a simple R/T switch. The system block diagram is presented in Figure 2. On receive, the RF signal is received by the antenna element and amplified by the LNA. The RF signal is then down-converted by two mixers whose LO signals are in quadrature. This is similar to the Hartley architecture where the signal of interest is down-converted by two quadrature mixers, low pass filtered, phase delayed by 90^o and summed to produce an image free Intermediate Frequency (IF) signal. In the system presented in Figure 2, both mixers contain RC networks for low pass filtering. Quadrature signal summation is performed off chip. The quadrature LO signals driving the mixers are generated on chip and are fed to the antenna modules by the IQ LO. The VVGA performs signal amplification at IF and allows for possible phase mismatch compensation at the LO and IF feeds. On transmit, the signal path is reversed and the LNA is replaced by the PA.

1.2 Vector Variable Gain Amplifier (VVGA)

The scope of this thesis is the design of the bi-directional VVGA. The VVGA performs an amplification of the IF IQ pair by an adjustable complex coefficient. The VVGA is to be integrated within the transceiver system of Figure 2.

In receive mode, the IQ signal flows from the mixer to the VVGA, which then drives an IQ IF feed network. In receive mode, therefore, the VVGA requires low input impedance to maximize mixer current gain. High output impedance is required to inject current into the IF feed. Thus, at receive, the VVGA functions as a Vector Variable Gain Current Amplifier (VVGCA.)

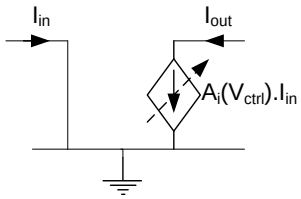

Figure 3: Ideal model of a VGCA

The signal flow is reversed on transmit mode. At transmit, the VVGA requires large input impedance to draw minimum current from the transmission line. High output impedance is required to drive the mixer IF port with maximum current. Thus, at transmit, the VVGA functions as a Vector Variable Gain Transadmittance Amplifier (VVGTA.)

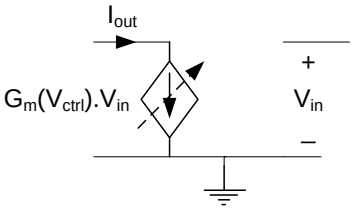

Figure 4: Ideal model of a VGTA

The VVGA consists of four interconnected Variable Gain Amplifier (VGA) blocks as shown in Figure 5:

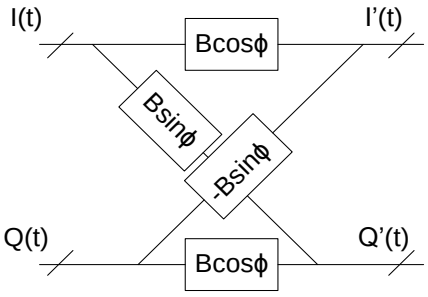

Figure 5: Block diagram of VVGA

By adjusting the gain of each block appropriately as shown, the IQ signal pair is amplified in magnitude by B and phase shifted by ϕ in both receive and transmit directions. The input and output relationship on receive and transmit are:

$$\mathrm{I}(t) = \frac{A}{2}\cos(\omega_I t + \theta) \xrightarrow{\text{Receive}} I'(t) = \frac{AB}{2}\cos(\omega_I t + \theta + \phi) \quad \text{(Eq. 1.3)}$$

$$\mathrm{Q}(t) = \frac{A}{2}\sin(\omega_I t + \theta) \xrightarrow{\text{Receive}} Q'(t) = \frac{AB}{2}\sin(\omega_I t + \theta + \phi) \quad \text{(Eq. 1.4)}$$

$$\mathrm{I}'(t) = \frac{A}{2}\cos(\omega_I t + \theta) \xrightarrow{\text{Transmit}} \mathrm{I}(t) = \frac{AB}{2}\cos(\omega_I t + \theta - \phi) \quad \text{(Eq. 1.5)}$$

$$\mathrm{Q}'(t) = \frac{A}{2}\sin(\omega_I t + \theta) \xrightarrow{\text{Transmit}} \mathrm{Q}(t) = \frac{AB}{2}\sin(\omega_I t + \theta - \phi) \quad \text{(Eq. 1.6)}$$

The direction of signal flow in the VVGA is set by a DC control voltage, V_{ctrl}, common to all four blocks. The gain of each VGA block is set by a five bit digital word. Each block is therefore capable of operating at 2^5 different gain states, referred to hereafter by "s," during receive and transmit. Due to the differential nature of each block, the gain states "s" and "$\bar{s}$" (bitwise NOT value of state "s") are equal in magnitude and 180^o out of phase.

The interconnected VGA blocks are identical. The two sine blocks and the two cosine blocks are differentiated by controlling them with two different five bit digital

words. The negative gain of the $-Bsin(\phi)$ block relative to that of the $Bsin(\phi)$ block is achieved by using the bitwise NOT value of the $Bsin(\phi)$ block control word as the control word for the $-Bsin(\phi)$ block (or vice versa).

The four-block system, therefore, requires ten control bits to adjust the gain. Five control bits adjust the gain for the two $Bcos(\phi)$ blocks, and five control bits adjust the gain for $Bsin(\phi)$ and $-Bsin(\phi)$ blocks, creating, overall, 2^{10} possible gain states. This is depicted in Figure 6 below :

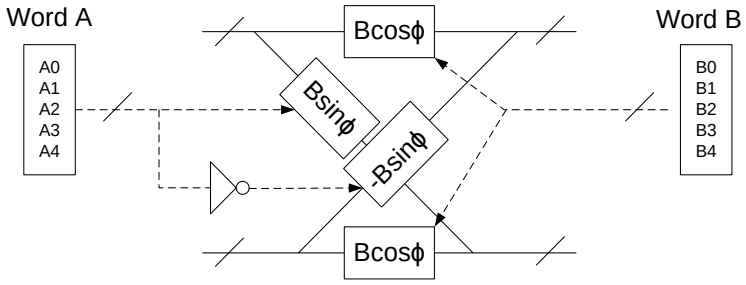

Figure 6: Gain control for VVGA

As each gain state corresponds to a gain in amplitude and shift in phase of the input signal, the 10 bits of available gain states create a discrete plot of amplitude gain versus phase shift in both receive and transmit directions. The gain vs. phase shift plot at each mode, as will be shown later in the thesis, will depict the available gain values, their corresponding phase shift values, and the gain and phase resolutions for any desired gain and phase margin.

To achieve bi-directionality, each VGA block consists of a CG and a CS amplifier. The CG Amplifier is "ON" during the receive mode of operation and the CS amplifier is "ON" during transmit mode of operation. Figure 7 depicts the $Bcos\phi$ block

configuration for receive and transmit. The remainder blocks have an identical configuration:

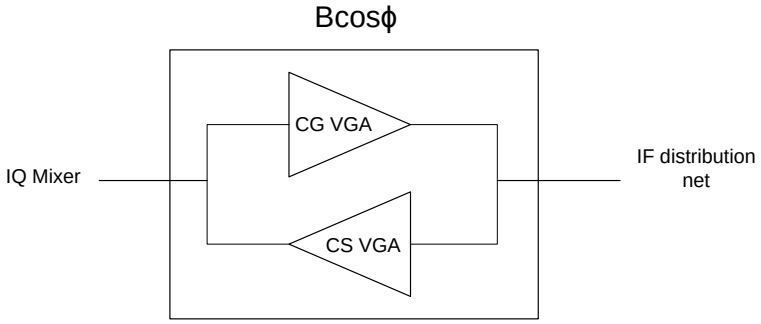

Figure 7: VGA block configuration

1.3 Literature Review

The principle of operation of the VGA blocks described above is to produce an output signal with variable proportionality to the input signal. The variable gain of the CG and CS VGA is achieved through variable transconductance of the MOS devices in the saturation region. The topology of the CG and CS VGA blocks can therefore be compared to various CMOS transconductance multiplier architectures that have been reported in the literature. Multipliers can be thought of as programmable transconductance circuits that are used to create products of two input signals, x and y, to yield a proportional output signal $y = Kxy$, while cancelling the undesired higher order (non-linear) terms. Multipliers employing CMOS technology can be grouped in different categories. Based on the range of input signals x and y, a multiplier is categorized either as a single-quadrant (x and y are both unipolar), two-quadrant (x or y are bipolar) or four-quadrant (x and y are bipolar) multiplier. Based on the regions of operation of the

MOS devices, multipliers are further grouped as Linear or Saturation type architectures. Multipliers can further be grouped based on the signal injection method. [3]

1.3.1 Linear Region Multipliers

A programmable transconductor cell utilizing linear region of operation is used in [4]. A basic configuration of this transconductance cell is shown in Figure 8 below:

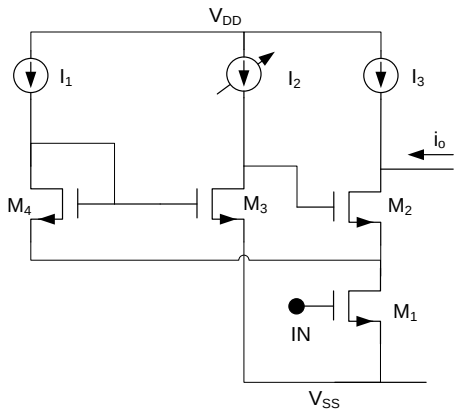

Figure 8: Basic configuration of the programmable transconductance cell as proposed in [4]

The programmable transconductance core are transistors M_1 and M_2. Transistor M_1's V_{ds} is the difference between the over drive voltages of M_4 and M_3, which must be low enough to keep M_1 in the linear region. M_4, M_3 and M_2 form a negative feedback loop to keep M_1 V_{ds} constant across a desired range of M_1 input gate voltages. The output current is then a function of M_1 transconductance, which varies linearly with its V_{ds}, which in turn is varied by DC current I_2. The output current is:

$$i_o = v_{in} K_1 \sqrt{\frac{2}{K_{3,4}}} \left(\sqrt{I_2} - \sqrt{I_1}\right) \qquad \text{(Eq. 1.7)}$$

Assuming $\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4$, the proper functionality of the multiplier above is maintained for $I_2 > I_1$, making this a two-quadrant multiplier (v_{in} is bipolar, $\left(\sqrt{I_2} - \sqrt{I_1}\right)$ is unipolar.) The linearity of this architecture is also poor, as it is a strong function of matching between currents I_3 and the difference between the quiescent current of M_1 and I_1.

A four-quadrant multiplier based on switched capacitor technology is proposed in [5]. The multiplier is realized by combining two programmable transconductance cells as part of a signal processing IC. For simplicity, the switched-capacitor portion is omitted in this review both to emphasize the principle of operation of the multiplier and simplicity. The figure below is the simplified schematic of the four-quadrant linear multiplier proposed in [5]:

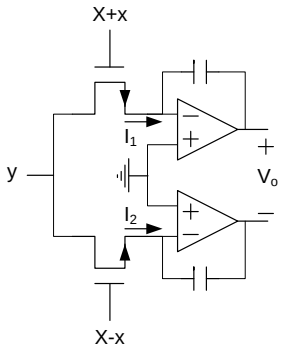

Figure 9: A four-quadrant analog multiplier as proposed in [5]

$$I_1 = K(X + x - VT - y/2)y \qquad \text{(Eq. 1.8)}$$

$$I_2 = K(X - x - VT - y/2)y \quad \text{(Eq. 1.9)}$$

$$I_o = I_1 - I_2 = 2Kxy \quad \text{(Eq. 1.10)}$$

A fully differential four-quadrant multiplier architecture improves the linearity of the multiplier. A fully differential multiplier-divider architecture based on operation in the linear region is proposed in [6]. This architecture can easily be modified to yield a four-quadrant multiplier as shown in the figure below:

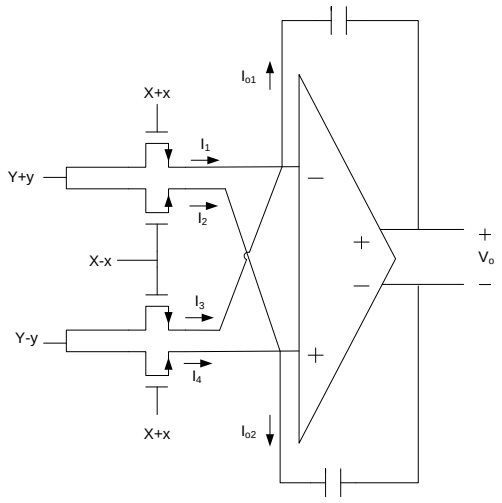

Figure 10: A Fully differential four-quadrant multiplier operating in the linear region obtained by modifying the analog multiplier/divider design concept as proposed in [6]

The output current of this four-quadrant multiplier can be shown to be:

$$I_o = I_{o1} - I_{o2} = 4Kxy \quad \text{(Eq. 1.11)}$$

1.3.2 Saturation Region Multipliers

A main disadvantage of MOS operation in the linear region is low transconductance and low speed. As fully differential architectures offer better non-

linearity cancelation, the fully differential MOS multiplier architectures operating in the saturation region are reviewed next.

One of the most used multiplier architectures is the cross coupled multiplier with source and gate signal injection that is based on the square-law characteristics of MOS transistors operating in the saturation region. This architecture was first proposed by Wang in [7]. The proposed multiplier consists of two cross-coupled variable gain cells with monotonically increasing transconductance with a tunable voltage, as shown in Figure 11 below:

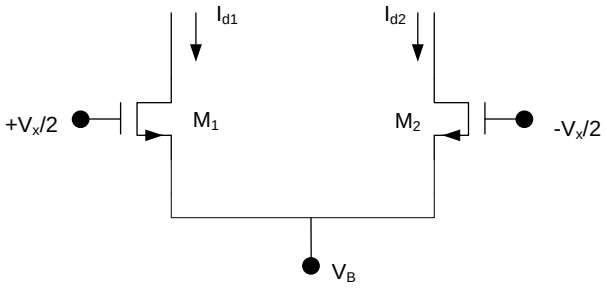

Figure 11: Two-quadrant analog multiplier cell used as building block for Wang's four-quadrant analog multiplier as proposed in [7]

Using the square-law model, the difference between the device currents can be shown to be:

$$I_o = I_{d1} - I_{d2} = -K(V_B + V_T)V_X \quad \text{(Eq. 1.12)}$$

Where K is the MOS transconductance parameter. This is called a two-quadrant multiplier because the input signal V_X could be both positive and negative, while the other input signal, V_B can only have positive values. A four-quadrant multiplier can be obtained by cross-coupling two identical two-quadrant multipliers as shown below [7]:

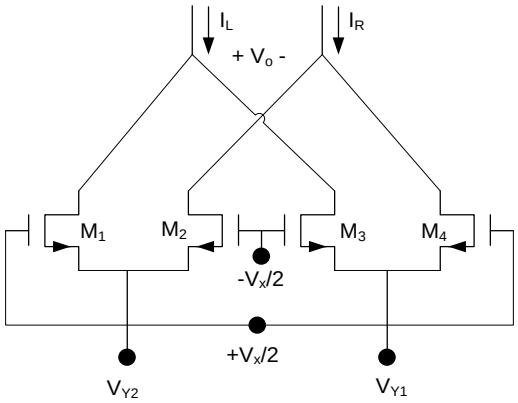

Figure 12: Four-quadrant cross-coupled analog multiplier operating in the saturation region as proposed in [7]

Using the same principles as the two-quadrant multiplier, it can be shown that:

$$I_o = I_L - I_R = KV_X V_Y \qquad \text{(Eq. 1.13)}$$

Where $V_Y = V_{Y1} - V_{Y2}$.

Different signal injection methods at the source of the four-quadrant cross-coupled multiplier above are reported in the literature. Wang's measurement setup employs off-chip op-amps to produce both the gate and source signals [7]. Song and Kim propose use of a source-follower stage to produce sum-squaring and difference-squaring circuits and subtracting them in [8].

1.3.3 Summary

In this thesis, a modified version of the fully differential, four-quadrant multiplier operating in the saturation region is offered as building block of the complex variable gain amplifier in receive and transmit modes of operation. In receive, a four transistor cross-coupled pair operating in saturation is used, and is referred to as VGCA. An AC-coupled differential input signal is injected at the source but no small signal injected at

the gates. The effective transconductance of the VGCA is varied by a change in the effective widths of the gate coupled transistor pairs. With V_y constant in Figure 12, for example, an input signal of zero amplitude at the gates would result in zero output current. In the variable width scheme introduced in this thesis, this is achieved without the need for an input signal at the gates by keeping the widths of transistors M_2 and M_3 equal to transistors M_1 and M_4. As another example, the effect of a large positive differential signal at the gates is replicated in our scheme by lowering the effective widths of transistor pair M_2 and M_3 to almost zero, while simultaneously increasing the effective widths of transistor pair M_1 and M_2 to a maximum. A simplified circuit diagram of the VGCA is shown in Figure 13:

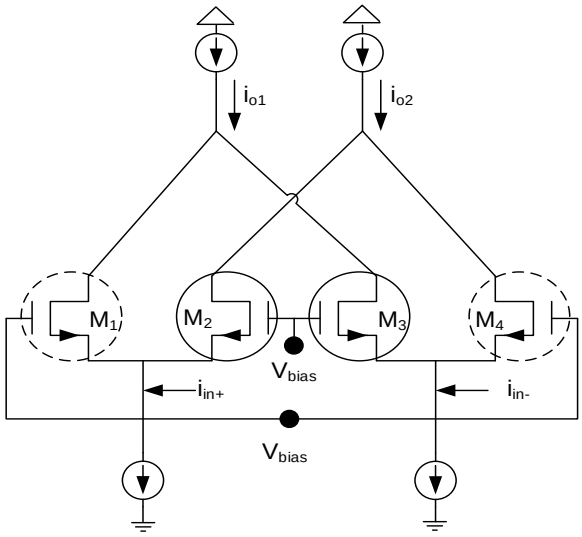

Figure 13: Modified version of the four-quadrant cross-coupled multiplier where effective transconductance is changed by varying the widths of transistors M_1 and M_4 (encircled with dashed lines) relative to widths of transistors M_2 and M_3 (encircled with solid lines) with small signal injection at source terminals

In transmit mode, a PMOS version of the cross coupled FET multiplier with source and gate signal injection is introduced in this thesis. While the variation in transconductance is achieved by adding or removing parallel transistors in the VGCA, therefore eliminating the signal injection at the coupled gate terminals, in transmit mode, or VGTA, the need for small signal injection at the coupled source terminals is eliminated by use of an incremental and symmetric increase or decrease in the DC bias currents of the source-coupled transistors. A simplified circuit diagram of the VGTA is shown in Figure 14:

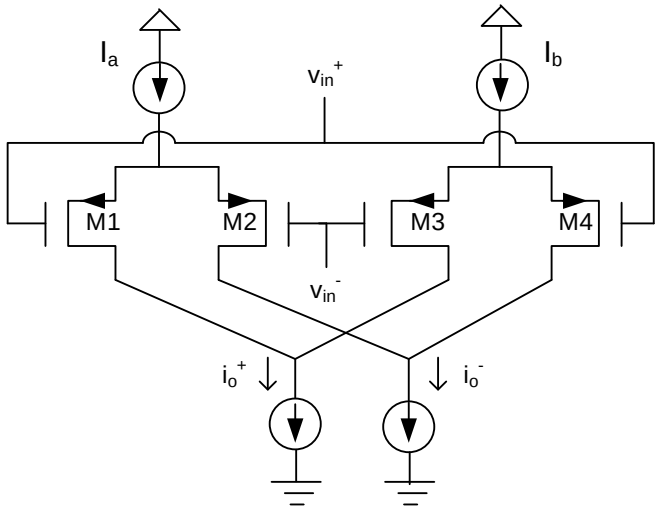

Figure 14: Modified PMOS version of the four-quadrant cross-coupled multiplier where effective transconductnace is changed by varying the bias currents of transistors M_1 and M_2 (I_a) relative to bias currents of transistors M_3 and M_4 (I_b) with small signal injection at gate terminals

Elimination of one continuous small signal input for both the VGTA and VGCA compared to the traditional, cross-coupled multiplier with two input signals allows for discrete transconductance gain states. The complex variable gain amplifier, then, can be

characterized by a look-up map that includes the magnitude and phase response at each discrete gain state at the frequency of interest within the linear input signal range of the amplifier.

1.4 Thesis Structure

In Chapter 2 the building blocks of the VGA are described. The VGCA, which corresponds to the VGA operating in receive mode, and the VGTA, corresponding to transmit mode VGA, are presented in standalone structures. The theory of operation, along with some details in the block design process are offered, and a selection of DC and IF frequency simulation results are presented.

Chapter 3 describes the process of combining the VGCA and VGTA to achieve a bi-directional block that will become the building block of the VVGA. Selected simulation results are shown to demonstrate the bi-directional VGA performance, both as VGCA (receive) and VGTA (transmit).

Chapter 4 describes the construction of a bi directional VVGA from the bi-directional VGA blocks that were described in the previous chapter. Selected simulation results show VVGA performance in VVGCA (receive) and VVGTA (transmit) modes of operation.

Chapter 5 describes the layout and presents post layout simulation results of the VGA and VVGA. Post-layout simulation results are compared to schematic simulation results.

In Chapter 6, measurement results are presented. Measurement setups for VGA and VVGA measurements are shown, and post-layout simulation results corresponding to the measurements are offered for comparison.

Chapters 2, 3, and 4 present designs that are slightly modified from what was laid out and fabricated to improve robustness of the original design. The main modifications of the new design are summarized in Appendix A and schematics are presented in Appendix G.

CHAPTER 2

VARIABLE GAIN AMPLIFIER

2.1 System Block Diagram

The VVGA consists of four interconnected VGA blocks as shown in Figure 15:

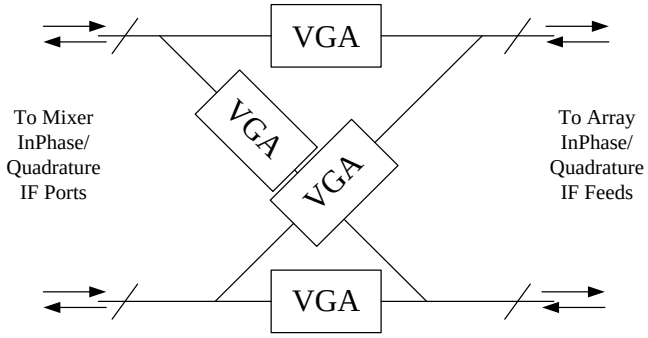

Figure 15: VVGA block diagram

The arrows indicate direction of signal flow during receive (right) and transmit (left). At receive, signal (current) is input from the IQ mixer and is output (current) to the IQ array feeds. At receive, therefore, the VVGA is referred to as VVGCA, and each VGA block is referred to as VGCA. At transmit, signal (voltage) is input from the IQ array feeds and is output (current) to the IQ mixer. At transmit, therefore, VVGA is referred to as VVGTA and each VGA block is referred to as VGTA.

2.2 VGCA

The VGCA is in a differential CG configuration where variation in gain is achieved through adjustment of the amplifier's transconductance parameter. With a constant overdrive voltage applied to amplifying transistors, $V_{od} \equiv V_{gs} - V_{th}$, the amplifier's

transconductance will vary proportionally to the transistor W/L ratio. Implementation of this scheme is presented here. The simplified schematic of the VGCA is shown below:

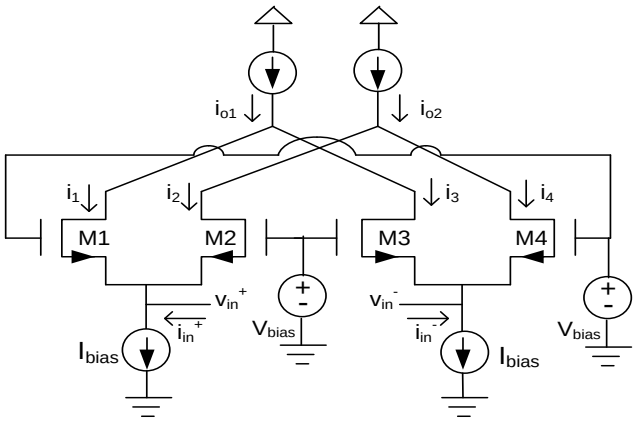

Figure 16: VGCA simplified circuit diagram

The gain of the amplifier is adjusted by adjusting the widths of transistors M_1thru M_4 as follows: for transistors M_1thru M_4, the drain currents are calculated using the square-law relationship as follows[2]:

$$I_1 = \frac{K'}{L} W_1 \left(V_{GS} - \frac{v_{in}}{2} - V_T\right)^2 = \frac{K'}{L} W_1 \left[(V_{GS} - V_T)^2 + \left(\frac{v_{in}}{2}\right)^2 - v_{in}(V_{GS} - V_T)\right] \quad \text{(Eq. 2.1)}$$

The transistors currents are:

$$I_1 = I_{D1} - g_{m1}\frac{v_{in}}{2} + \frac{K'}{L} W_1 \left(\frac{v_{in}}{2}\right)^2 \quad \text{(Eq. 2.2)}$$

[2] It is assumed that all transistors are biased in saturation region with strong inversion. Channel length modulation and other short channel effects are ignored for sake of simplicity.

$$I_2 = I_{D2} - g_{m2}\frac{v_{in}}{2} + \frac{K'}{L}W_2\left(\frac{v_{in}}{2}\right)^2 \quad \text{(Eq. 2.3)}$$

$$I_3 = I_{D3} + g_{m3}\frac{v_{in}}{2} + \frac{K'}{L}W_3\left(\frac{v_{in}}{2}\right)^2 \quad \text{(Eq. 2.4)}$$

$$I_4 = I_{D4} + g_{m4}\frac{v_{in}}{2} + \frac{K'}{L}W_4\left(\frac{v_{in}}{2}\right)^2 \quad \text{(Eq. 2.5)}$$

Where $v_{in}{}^{+} = v_{in}/2 = -v_{in}{}^{-}$ and V_{GS} is the DC value of the gate to source voltage. Using the definition of output current and noting that:

$$W_1 = W_4, W_2 = W_3 \quad \text{(Eq. 2.6)}$$

The output current is then calculated as follows:

$$I_{o1} = I_1 + I_3 = I_{D1} + I_{D3} + (g_{m3} - g_{m1})\frac{v_{in}}{2} + \frac{K'}{L}(W_1 + W_3)\left(\frac{v_{in}}{2}\right)^2 \quad \text{(Eq. 2.7)}$$

$$I_{o2} = I_2 + I_4 = I_{D2} + I_{D4} + (g_{m4} - g_{m2})\frac{v_{in}}{2} + \frac{K'}{L}(W_2 + W_4)\left(\frac{v_{in}}{2}\right)^2 \quad \text{(Eq. 2.8)}$$

$$I_{o-sc} = I_{o1} - I_{o2} = -v_{in}(g_{m1} - g_{m2}) = -v_{in}(g_{m4} - g_{m3}) \quad \text{(Eq. 2.9)}$$

Where, for a constant DC over drive voltage, $g_{m1}$and $g_{m2}$are functions of transistors' effective widths, $W_1$and W_2, respectively. By keeping $W_1 = W_4$, $W_2 = W_3$, and sum of W_1 and W_2 constant, input and output impedances of the CG amplifier stay constant as the effective widths of transistors M_1 thru M_4 are varied to adjust gain. It is evident from the above relationship that this topology achieves adjustable amplification and cancels out all common mode and even order harmonics at the output. Due to its low input impedance, high output impedance, and adjustable gain, the CG amplifier of Figure 16 is referred to as VGCA.

2.2.1 Digital Control of Current Gain

To achieve variable effective width for the CG transistors, the following scheme has been employed.

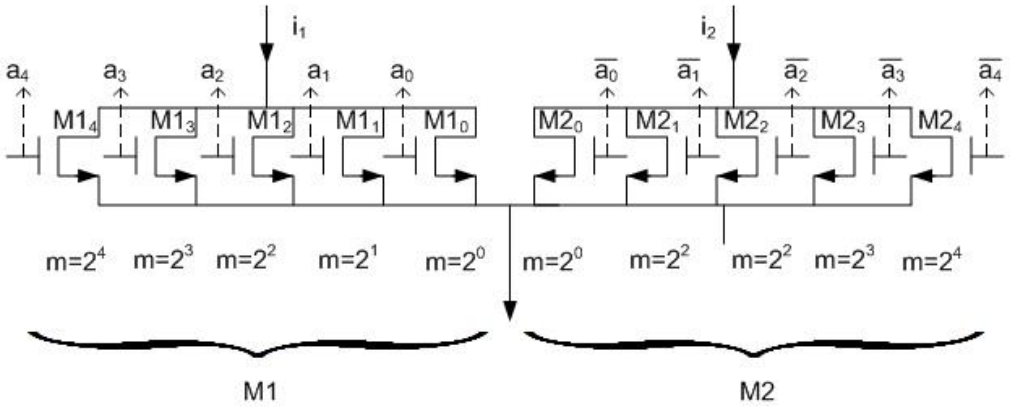

Figure 17: VGCA variable effective gain circuit diagram

The scheme for adjusting the widths of transistors $M1$ and $M2$ is shown in Figure 17 above and the notation is described below. Transistors $M3$ and $M4$ are identical to and set up as mirror images of transistors $M1$ and $M2$.

Transistors $M1$ and $M2$ are each comprised of five parallel NMOS enhancement mode FETs $(M1_0 - M1_4)$ and $(M2_0 - M2_4)$, as indicated in Figure 17. These transistors are connected at drain and source, with their gate voltages connected to binary switches (High or Low) that can turn them ON (saturation region) or OFF (cut-off region)[3]. The switch values are represented as a five bit control word, $A =$

[3] Each digital bit drives an inverter whose rail voltage is set to the appropriate bias voltage using a resistive divider. Each inverter output then drives the gate terminal of NMOS devices as shown in Figure 17

$[a4, a3, a2, a1, a0]$ for transistor $M1$ and as the bitwise NOT value of control word A, $\bar{A}$, for transistor $M2$, where each bit represents a High or Low value.

Transistors $M1_0 - M1_4$ and $M2_0 - M2_4$ are in turn comprised of parallel transistors with channel width equal to W_o. The number of parallel transistors comprising each transistor is indicated as a multiplication factor, m, in Figure 17. As an example, $M1_0$ has a width equal to W_o and $M1_4$ has a width equal to $2^4 \times W_o$.

The effective widths of transistors $M1 - M4$ are therefore equal to:

$$\mathrm{W_1} = \mathrm{W_o} \sum_{i=0}^{4} 2^i a_i \qquad \text{(Eq. 2.10)}$$

$$W_3 = W_2, W_4 = W_1$$

The output current, as described earlier, is a function of transistor effective widths:

$$g_{m1} - g_{m2} = \underbrace{\left[\frac{K_n{}'}{L}(V_{GS} - V_{TN})\right]}_{constant}(W_1 - W_2) \qquad \text{(Eq. 2.11)}$$

From above configuration, $W_1 - W_2$ is determined as follows:

$$W_1 - W_2 = W_o \sum_{i=0}^{4} 2^i (a_\mathrm{i} - \bar{a}_\mathrm{i}) \qquad \text{(Eq. 2.12)}$$

VGCA's transfer function is therefore equal to:

$$Y_f \equiv \frac{I_{o-sc}}{v_{in}} = -\frac{K_n{}' W_o}{L}(V_{GS} - V_{TN}) \sum_{i=0}^{4} 2^i (a_\mathrm{i} - \bar{a}_\mathrm{i}) \qquad \text{(Eq. 2.13)}$$

Where I_{o-sc}/v_{in} is defined as the VGCA's forward transadmittance parameter, Y_f.

2.2.2 Input Impedance

The input impedance can be calculated using the simplified schematic of the VGCA shown in Figure 18 below:

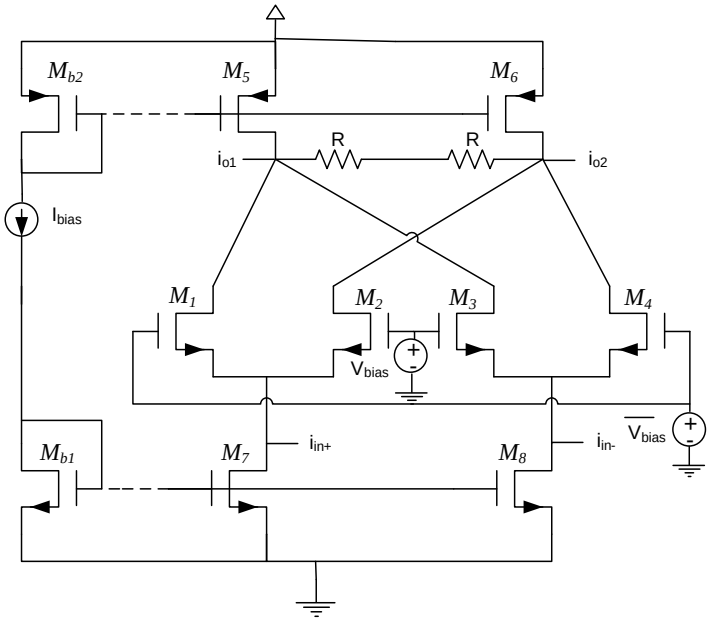

Figure 18: Simplified VGCA schematic

$$R_{in} = \frac{1}{g_{m1}} || \frac{1}{g_{m2}} = \frac{1}{g_{m1} + g_{m2}} = \frac{1}{g_{m3} + g_{m4}} = \frac{1}{g_{m,max}} \quad \text{(Eq. 2.14)}$$

Where $g_{m,max}$ refers to:

$$g_{m,max} = \frac{K_n{}'}{L}(V_{GS} - V_{TN})(W_1 + W_2) \quad \text{(Eq. 2.15)}$$

And:

$$W_1 + W_2 = \mathrm{W_o} \sum_{i=0}^{4} 2^i (a_\mathrm{i} + \bar{a}_\mathrm{i}) = \mathrm{W_o}(2^5 - 1) \quad \text{(Eq. 2.16)}$$

Substituting (Eq. 2.16) and (Eq. 2.15) in (Eq. 2.14) yields:

$$R_{in} = \frac{1}{\frac{K_n{}'}{L}(V_{GS} - V_{TN})\mathrm{W_o}(2^5 - 1)} \qquad \text{(Eq. 2.17)}$$

A more precise calculation of input resistance that takes into account effects of device output resistances and loading at VGCA output, as offered in Appendix B, reveals that the input resistance is also a function of amplifier load at the output. These results are summarized in Table 3 of Appendix B and are repeated here for convenience:

Gain Setting	R_L	R_{in}
$Maximum\ (0,31)$	$Short$	$1/g_{m,max}$
$Minimum\ (15{,}16)$	$Short$	$1/g_{m,max}$
$Maximum\ (0,31)$	$Open$	$2/g_{m,max}$
$Minimum\ (15,16)$	$Open$	$4/3g_{m,max}$

Table 1: VGCA input resistance versus gain settings and load

Due to the expected small impedance seen at the VGCA load[4], however, the load impedance is more accurately modeled as a short than an open. The expected VGCA input resistance, then, is $1/g_{m,max}$.

[4] The expected differential impedance seen at the VGCA load is equal to the impedance looking into the IF in-phase and quadrature feeds of Figure 2 on page 3, which is expected to be approximately 50Ω. The load impedance, therefore, is more accurately modeled as a short than an open.

2.2.3 Output Impedance

The VGCA output resistance is[5]:

$$R_o = r_{o1} \parallel r_{o3} \parallel r_{o5} = r_{o2} \parallel r_{o4} \parallel r_{o6} \quad \text{(Eq. 2.18)}$$

Because:

$$I_{D5} = I_{D1} + I_{D3} \; and \; I_{D6} = I_{D2} + I_{D4} \quad \text{(Eq. 2.19)}$$

The output resistance becomes:

$$R_o = \frac{1}{\lambda_N (I_{D1} + I_{D3})} || \frac{1}{\lambda_P (I_{D1} + I_{D3})} \quad \text{(Eq. 2.20)}$$

Assuming that the n-channel and p-channel MOS devices have approximately equal channel length modulation parameters, the output resistance will be approximated as:

$$R_o \approx \frac{1}{2\lambda (I_{D1} + I_{D3})} = \frac{1}{2\lambda (I_{D2} + I_{D4})} \quad \text{(Eq. 2.21)}$$

$$R_o = \frac{1}{2\lambda (1/2)(V_{GS} - V_{TN})(g_{m1} + g_{m3})} \quad \text{(Eq. 2.22)}$$

$$R_o = \frac{1}{\lambda (V_{GS} - V_{TN}) g_{m,max}} \quad \text{(Eq. 2.23)}$$

With $g_{m,max}$ previously defined in (Eq. 2.15).

The output resistance, as shown in Appendix C, is also a function of source resistance and gain state of the VGCA. The results are repeated here for convenience:

---

[5] It is assumed that the common mode sense resistors ($10k\Omega$) add negligible loading

$$R_{o,\underset{gain}{\max}} = r_{o5} || \, R_{o1} = r_{o1,\underset{gain}{\max}} \left(g_{m,max} \frac{R_s}{2} + 1 \right) || r_{o5} \quad \text{(Eq. 2.24)}$$

$$R_{o,\underset{gain}{\min}} = r_{o1,\max\_gain} \left(\frac{g_{m,max}}{2} \frac{R_s}{2} + 1 \right) || r_{o5} \quad \text{(Eq. 2.25)}$$

Based on the expected R_s value of 160Ω[6], the above expressions are modified as follows:

$$R_{o,\underset{gain}{\max}} = r_{o5} || \, R_{o1} = r_{o1,\max\_gain} (80 g_{m,max} + 1) || r_{o5} \quad \text{(Eq. 2.26)}$$

$$R_{o,\underset{gain}{\min}} = r_{o1,\max\_gain} (40 g_{m,max} + 1) || r_{o5} \quad \text{(Eq. 2.27)}$$

2.2.4 Equivalent Circuit

For high source impedances (relative to multiplier input impedance) and low load impedances (relative to multiplier output impedance), the VGCA can be modeled closely as a current amplifier with variable transfer current ratio:

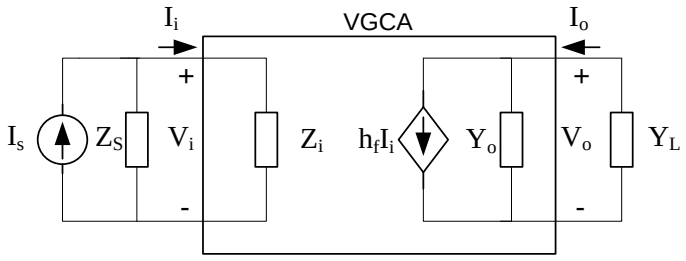

Figure 19: VGCA h-parameter equivalent circuit

[6] Mixer output impedance shown on Figure 2 on page 3 is approximately 160Ω

Here it is assumed that VGCA is perfectly unilateral[7], therefore eliminating the open circuit inverse transfer voltage ratio, h_r. Z_i is the input impedance, h_f is the short circuit transfer current ratio, and Y_o is the open circuit output admittance. Z_s and Y_L correspond to source impedance and load admittance, respectively.

The expression for the transfer current relationship is determined as follows:

$$V_i = Z_i I_i \quad \text{(Eq. 2.28)}$$

$$I_o = h_f I_i + Y_o V_o \quad \text{(Eq. 2.29)}$$

$$\frac{I_o}{I_i} = h_f \frac{Y_L}{Y_o + Y_L} \quad \text{(Eq. 2.30)}$$

$$\frac{I_o}{I_s} = h_f \frac{Y_L}{Y_o + Y_L} \frac{Z_s}{Z_s + Z_i} \quad \text{(Eq. 2.31)}$$

It is evident that large input impedance limits the amplifier input current and large output admittance reduces the current gain of the amplifier (defined as I_o/I_i) . Appropriate values of source and load impedances will maximize current transfer ratio:

$$\frac{Z_s}{Z_s + Z_i} \approx 1 \; when \; Z_i \ll Z_s \quad \text{(Eq. 2.32)}$$

$$\frac{Y_L}{Y_o + Y_L} \approx 1 \; when \; Y_o \ll Y_L \quad \text{(Eq. 2.33)}$$

Then:

---

[7] As explained earlier, the effect of the typical output load resistance ($R_L \approx 50\Omega$) on the input resistance of the VGCA is negligible (Table 1 on page 24) The effect of typical source resistance ($R_S \approx 160\Omega$) on the output resistance is to increase it slightly ((Eq. 2.24) and (Eq. 2.25) on page 26), consistent with the assumption that $Y_L/(Y_o + Y_L) \approx 1 \; for \; Y_o \ll Y_L$. It is therefore reasonable to assume a unilateral system for calculation of current gain.

$$\frac{I_o}{I_i} = \frac{I_o}{I_s} \approx h_f \qquad \text{(Eq. 2.34)}$$

The amplifier's current gain is now evaluated in terms of forward transfer admittance value, Y_f previously calculated in (Eq. 2.13) on page 22:

$$Y_f = \frac{I_{o-sc}}{V_i} = \frac{h_f}{Z_i} \qquad \text{(Eq. 2.35)}$$

$$\frac{I_o}{I_i} = Y_f Z_i \frac{Y_L}{Y_o + Y_L} \qquad \text{(Eq. 2.36)}$$

Assuming negligible input impedance variations with gain settings, substituting (Eq. 2.17) on page 24 into (Eq. 2.36) above yields:

$$\frac{I_o}{I_i} = -\frac{Y_L}{Y_o + Y_L} \frac{\sum_{i=0}^{4} 2^i (a_i - \bar{a}_i)}{2^5 - 1} \qquad \text{(Eq. 2.37)}$$

The plot of short circuit current gain of the VGCA for the 2^5 gain states is shown below:

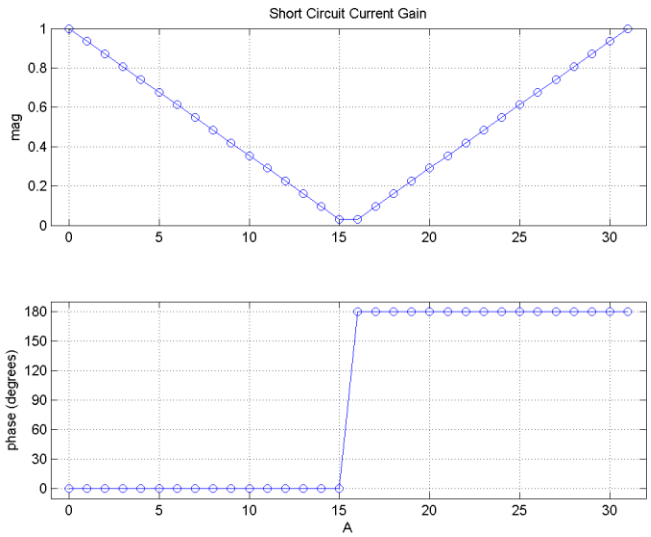

Figure 20: VGCA current gain – ideal

It is noted that for high values of load admittance (relative to output admittance), the amplifier acts as a current buffer at gain setting of $A = 2^5 - 1$ and as an inverting current buffer at gain setting of $A = 0$.

2.2.5 CMFB

To achieve high output impedance for the VGCA, an active PMOS load is used. Consequently, as depicted in Figure 21 below, the DC bias currents in VGCA are set by a PMOS and an NMOS current source, M_{b1} and M_{b2}, respectively. In Figure 21, $I_5 = I_6, I_7 = I_8$, and $I_5 + I_6 = I_7 + I_8$, which implies that all four currents are equal. Slight mismatches between the PMOS and NMOS current mirror transistors, or current mismatches between current mirror transistors $M_{5,6}, M_{7,8}$ and the corresponding diode connected transistors M_{b2}, M_{b1} due to drain source voltage mismatch, however, causes a mismatch between currents $I_{5,6}$ and $I_{7,8}$. The difference in current, $I_{5,6} - I_{7,8}$, must flow through the intrinsic output resistance of the VGCA, $r_{o5} || r_{o1} || r_{o3}$ (and $r_{o6} || r_{o2} || r_{o4}$), possibly creating a large voltage error that cannot be produced by the circuit. For $I_{5,6} < I_{7,8}$, then, transistors $M_{7,8}$ have to enter the triode region so that their drain currents fall to $I_{5,6}$. Similarly for $I_{5,6} > I_{7,8}$, transistors $M_{5,6}$ enter the triode region so that their drain currents fall to $I_{7,8}$.

To maintain constant DC output voltages and currents, a feedback network is implemented. Figure 21 shows the conceptual topology of CMFB implementation in VGCA:

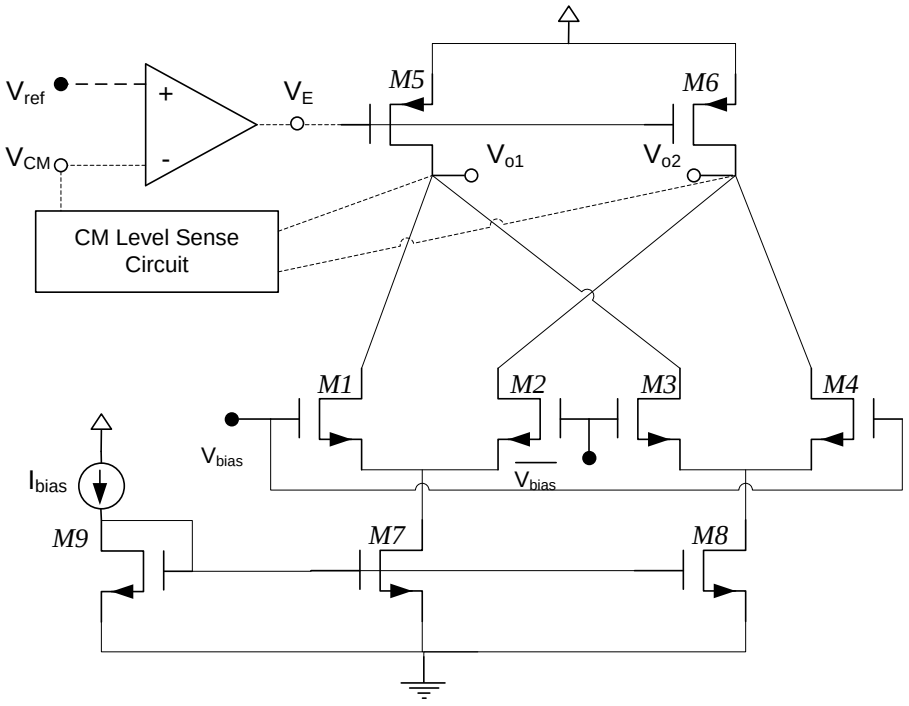

Figure 21: VGCA CMFB conceptual topology

Figure 21 depicts the three mechanisms necessary for CMFB to properly maintain the common mode level: a mechanism to sense the common mode voltage, one to compare the common mode voltage to a reference voltage, V_{ref}, to produce an error signal, and one to apply the error, V_E, to the VGCA bias network (either the PMOS or NMOS current source pair, here the PMOS current source pair is used) for bias current correction. Figure 22 shows the implementation of CMFB circuit in the VGCA:

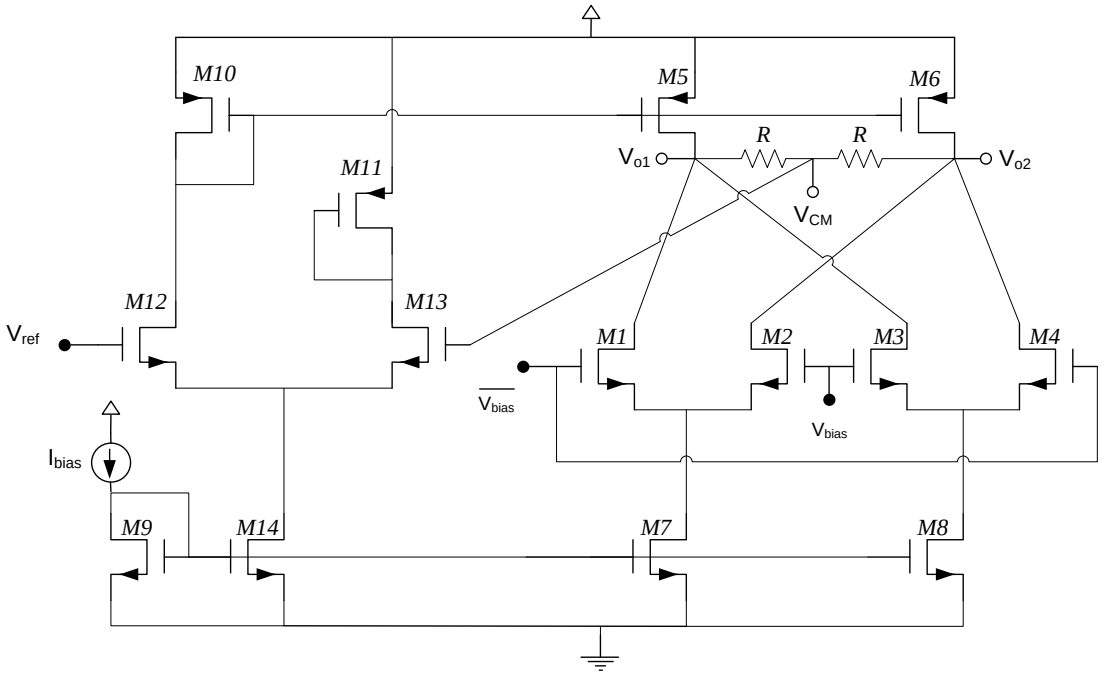

Figure 22: VGCA CMFB implementation

The two resistor network, with each resistor indicated as R, senses the common mode voltage, V_{CM}. For large R (to avoid resistive loading of the output stage):

$$V_{CM} = (V_{o1} + V_{o2})/2 \qquad \text{(Eq. 2.38)}$$

It is important to note that the feedback network compares the average value of the differential output voltage to the reference voltage, ignoring any differential change in the output. The common mode voltage, V_{CM}, is next compared to the reference voltage, V_{ref}, through use of a differential CS configuration: V_{CM} and V_{ref} are converted to currents by applying them to the gates of the input transistor pair, M_{12} and M_{13}. The voltages are then compared through M_{12} and M_{13} current subtraction and the resulting current is applied to VGCA's current source transistor pair through mirroring action of the diode connected load of the differential CS amplifier. The negative nature of the feedback is

evident by inspection: an increase (decrease) in V_{CM} increases (decreases) the drain-source current in M_{13}. This increase (decrease) in current causes a decrease (increase) in source-drain current of M_{10}, which in turn causes a decrease (increase) in M_5 and M_6 source-drain currents, lowering (increasing) the output voltage thus the V_{CM}.

The loop gain, can be calculated by inspection. It is assumed that $g_{m12} = g_{m13}, g_{m10} = g_{m11},$ and $g_{m5} = g_{m6}$:

$$-\frac{v_f}{v_t} = \frac{g_{m5}g_{m12}R_o}{g_{m10}} \quad \text{(Eq. 2.39)}$$

Due to large size of transistors M_1 thru M_4 and M_5 and M_6, and the large output resistance at the output node, the dominant pole is at:

$$p_1 = -\frac{1}{R_o C_p} \quad \text{(Eq. 2.40)}$$

Where C_p is the parasitic capacitance at the output node of the VGCA. Because the resistive CM level sensing network has a gain of 1, the feedback factor, β, is equal to one and for a large enough loop gain:

$$\frac{V_{CM}}{V_{ref}} \approx \frac{1}{\beta}\left(1 - \frac{1}{\beta A}\right) = 1 - \frac{1}{\beta A} \approx 1 \quad \text{(Eq. 2.41)}$$

Further CMFB simulation results and analysis are presented in Appendix F.

2.2.6 DC Biasing[8]

The minimum device width per finger allowed in our technology and the minimum number of fingers set the minimum channel width of the amplifying NMOS device. To obtain 5 bits of variable gain resolution thru the method discussed in previous sections, the minimum device channel width becomes:

$$W_{min} = (2^5 - 1) \times nf_{min} \times fw_{min} \quad \text{(Eq. 2.42)}$$

$$W_{min} = (2^5 - 1) \times nf_{min} \times fw_{min} = (2^5 - 1) \times 2 \times 880nm = 54.56um \quad \text{(Eq. 2.43)}$$

Where nf_{min} is the minimum number of fingers allowed and fw_{min} is the minimum finger width. The biasing voltage requirements for the VGCA are determined next. Referring to Figure 23 below:

---

[8] Almost all transistors in this design are minimum length devices. Some consequences of using minimum length devices are higher current gain error due to channel length modulation, higher device mismatch, and lower intrinsic gain (causes lower DC gain in CMFB error amplifier, reducing closed loop accuracy at low frequencies).

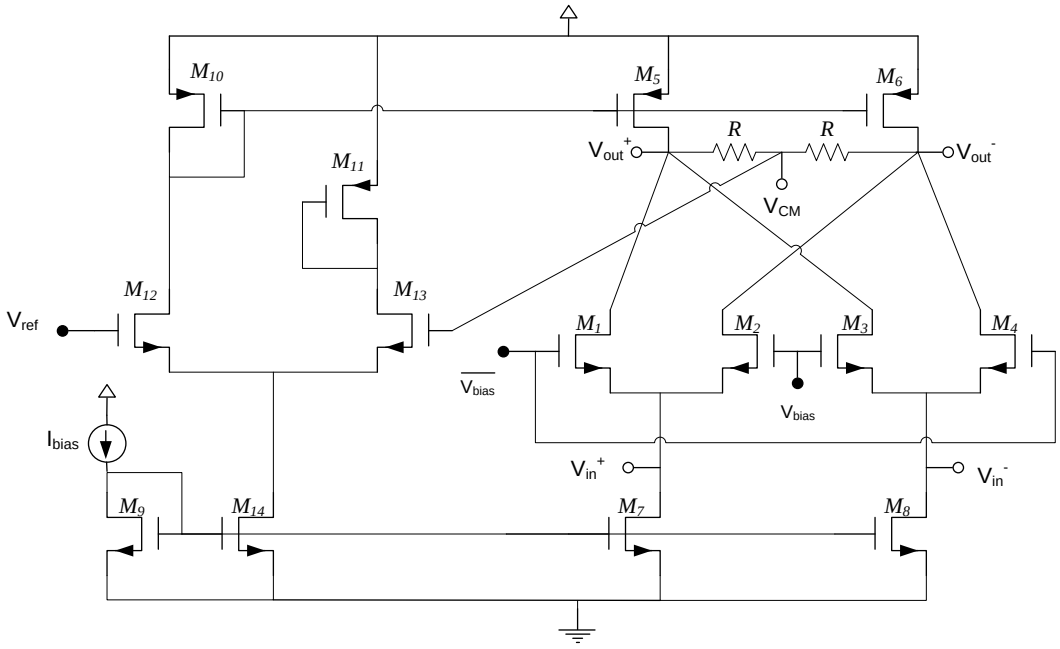

Figure 23: VGCA DC biasing

The gate bias voltage range of transistors $M_{1,2,3,4}$ is:

$$V_{GS1} + V_{OD7} \leq V_{bias} \leq V_{DD} - V_{OD5} + V_{TN} \quad \text{(Eq. 2.44)}$$

$$700mV \leq V_{bias} \leq 1.76V \quad \text{(Eq. 2.45)}$$

Where $V_{GS1-4} = 600mV, V_{OD7} = 100mV, V_{DD} = 1.8V, V_{OD5} = 240m$ and $V_{TN} \approx 500mV$. The bias voltage, V_{bias}, is picked to be $1.12V$. The bias value at the input is set by the necessary gate to source voltage of transistors M_1 thru M_4 to maintain the DC bias current:

$$Vcm_{in} = V_{bias} - V_{TH} - V_{od1} \approx 510mV \quad \text{(Eq. 2.46)}$$

The output common mode range is:

$$V_{bias} - V_{TH} < VCM_{out} < V_{DD} - V_{od5} \quad \text{(Eq. 2.47)}$$

$$612mV < Vcm_{out} < 1.56 \quad \text{(Eq. 2.48)}$$

With the output common mode voltage set to $900mV$ by the CMFB circuit, the output swing is then:

$$-290mV < V_{out} < 290mV \quad \text{(Eq. 2.49)}$$

DC bias currents of transistors M_{1-4} versus the gain states are depicted in Figure 24 below:

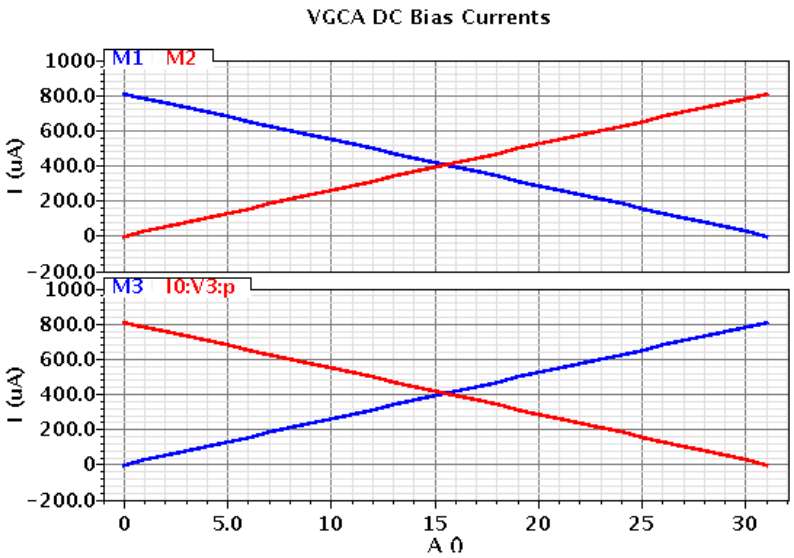

Figure 24: VGCA DC currents versus gain states– schematic simulation result

2.2.7 NMOS Second Order Effects

The body effect affects all NMOS transistors whose source terminal is at a potential higher than their substrate. A positive V_{SB} increases the threshold voltage of the NMOS transistors above the zero-substrate-bias value of the threshold voltage:

$$V_{TN} = V_{TO} + \gamma\left(\sqrt{V_{SB} + 2\phi_F} - \sqrt{2\phi_F}\right) \quad \text{(Eq. 2.50)}$$

Where

$$V_{TO} = zero - substrate - bias\ value\ for\ V_{TP}\ (V)$$

$$\gamma = body - effect\ parameter\ (\sqrt{V})$$

$$2\phi_F = surface\ potential\ parameter\ (V)$$

Figure below is an attempt to understand the body effect in our technology. The drain-source current of an NMOS transistor is plotted against the drain-source voltage for various gate source potentials.

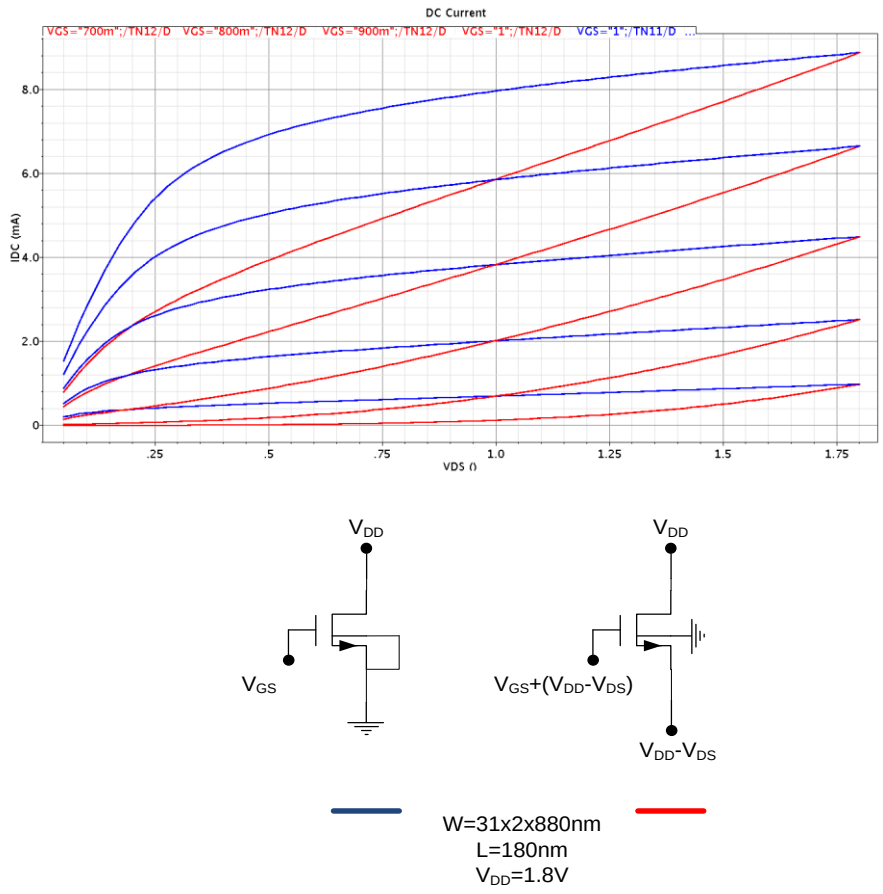

Figure 25: NMOS I_{DS} vs. V_{DS} curves illustrating body effect and channel length modulation – schematic simulation result

From figure above it is clear that the body effect has a significant effect on the device performance. As the potential between the source and body increases, the threshold voltage increases, resulting in a drop in overdrive voltage, the drain-source

current, and the device transconductance. The body effect on all NMOS devices used in the VGCA is similar and proportional to the plot shown above. To eliminate this effect, the NMOS source terminals are tied to their body terminal (isolated P-well process.)

2.3 VGCA Schematic Simulation Results

2.3.1 Input Impedance

Input impedance of the VGCA is next simulated. The testbench is shown in Figure 26 below:

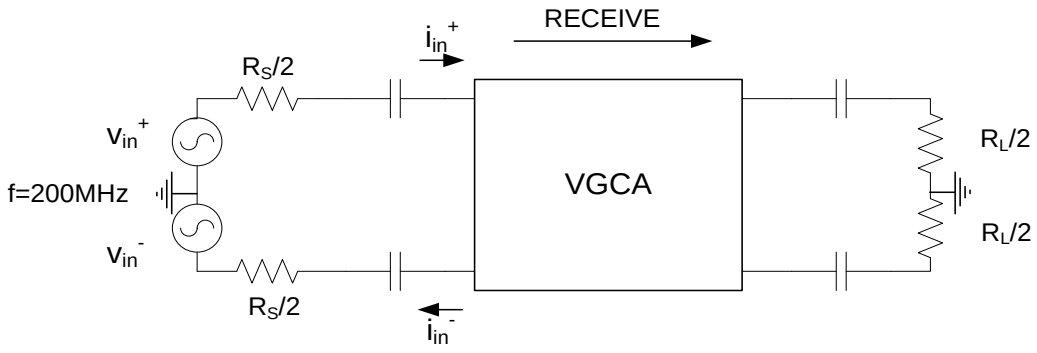

Figure 26: VGCA differential input impedance simulation setup

Where differential input impedance is defined as:

$$Z_{in\_diff} = \frac{v_{in}^+ - v_{in}^-}{i_{in}^+ - i_{in}^-} \quad \text{(Eq. 2.51)}$$

Input impedance simulation results with default terminations[9] is shown in Figure 27 below:

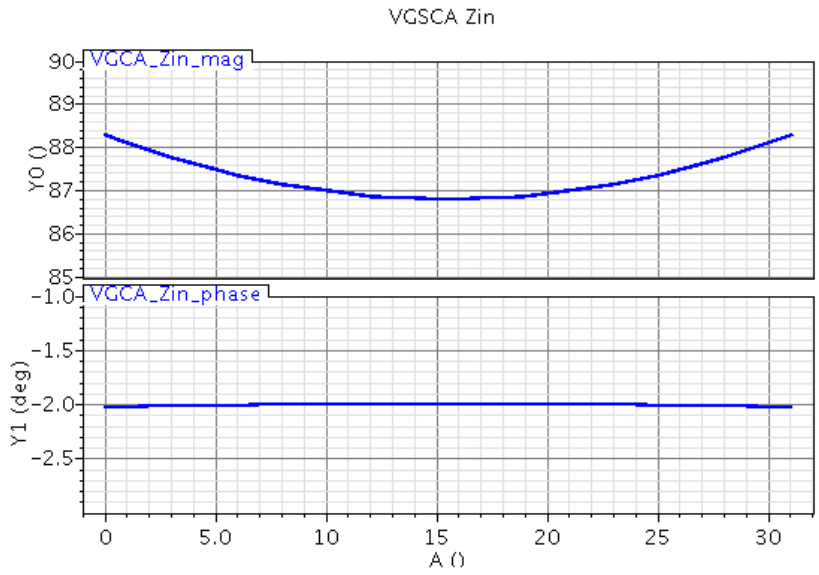

Figure 27: VGCA input impedance – default terminations – schematic simulation result

$$R_{in,50\Omega(\text{simulation})} = 88\Omega \quad \text{(Eq. 2.52)}$$

Simulation results of input resistance for a short output termination, as expected, indicate a resistance of 87Ω with no variation across gain states. For a 50Ω differential output termination, as shown in Figure 27 above, the variation in impedance across gain states is smaller than 2Ω, suggesting that the output termination is similar to a short

[9] Throughout the thesis it is assumed that the typical (default) differential impedance seen by VGCA at the input and output is approximately 160Ω and 50Ω, corresponding to the IQ Mixer differential output impedance and IF feedline differential characteristic impedance, respectively.

termination. The expected input resistance based on short circuit analysis is 97Ω, which is within 10% of the simulation results (87Ω):

$$R_{in,short} = \frac{1}{g_{m,max}}\Bigg|_{g_{m,max}=330.5uS\times(2^5-1)} = 97\Omega \qquad \text{(Eq. 2.53)}$$

With an open output termination, the simulation results indicate that the variation in input impedance (almost entirely resistive) becomes significant across gain states. At minimum gain settings, the input resistance obtained from simulation results is at its minimum and equal to the short circuit input resistance, while at maximum gain settings the resistance increases. This is consistent with the open load input impedance analysis summarized in Table 1 on page 24, repeated here for convenience:

$$R_{in,open,\max gain} = \frac{2}{g_{m,max}} = 2R_{in,short} \qquad \text{(Eq. 2.54)}$$

2.3.2 Output Impedance

The output impedance is simulated as shown in Figure 28 below:

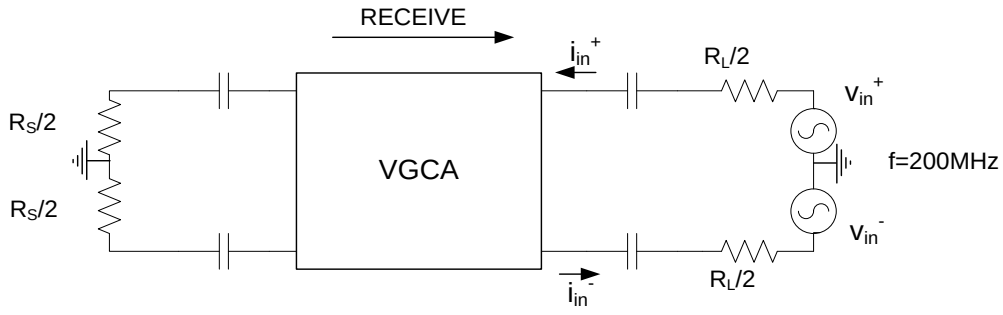

Figure 28: VGCA differential output impedance simulation setup

Where differential output impedance is defined as:

$$Z_{out\_diff} = \frac{v_{in}^{+} - v_{in}^{-}}{i_{in}^{+} - i_{in}^{-}} \qquad \text{(Eq. 2.55)}$$

Figure below shows the output impedance simulation results at $200MHz$:

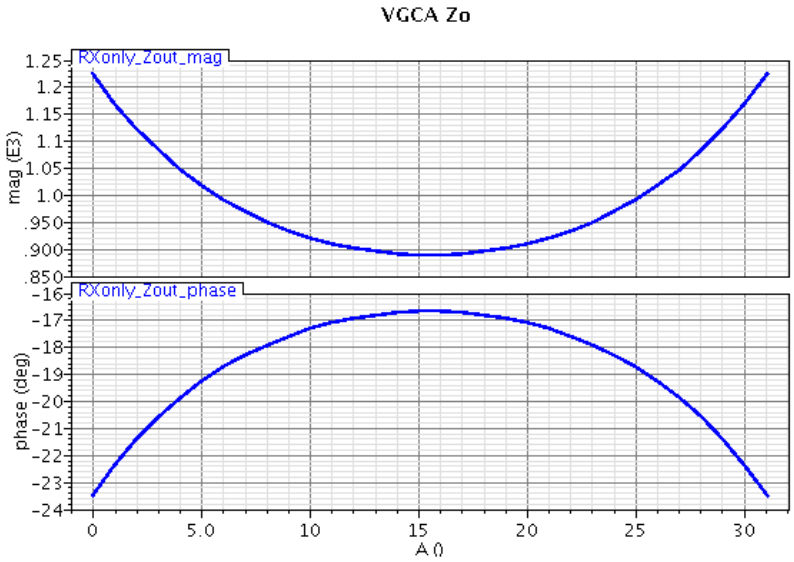

Figure 29: VGCA output impedance vs. gain states – default terminations – schematic simulation result

To find an estimate value for the output resistance and capacitance, the output impedance is plotted across frequency at maximum gain setting:

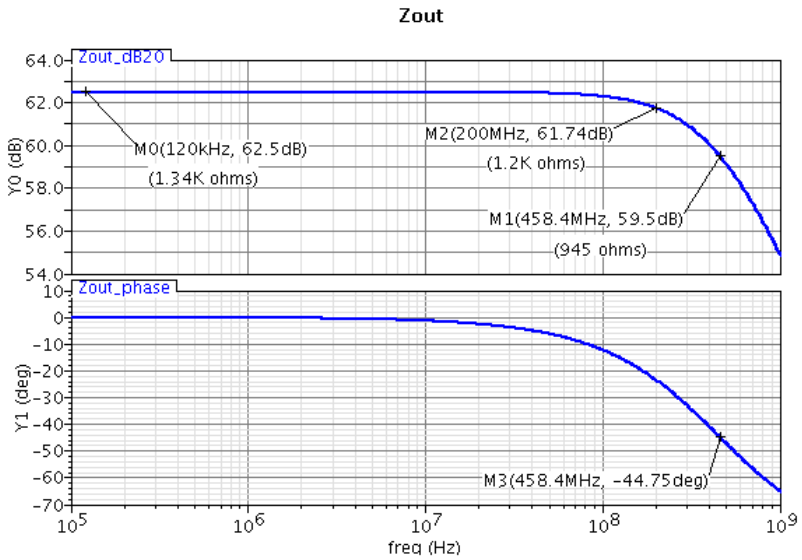

Figure 30: VGCA output impedance vs. frequency at maximum gain setting – default terminations – schematic simulation result

At 3-dB frequency:

$$\left|\frac{R}{1+\frac{s}{1/RC}}\right| = -3dB \qquad \text{(Eq. 2.56)}$$

$$\measuredangle\frac{R}{1+\frac{s}{1/RC}} = -45^{o} \qquad \text{(Eq. 2.57)}$$

Where, from Figure 30 above:

$$R_{o\_sim} = 1.34K\Omega\ (\text{DC}), s = j2\pi(458.4MHz) \xrightarrow{yields} C_{o\_sim} = 260fF \qquad \text{(Eq. 2.58)}$$

At maximum gain setting, hand calculations predict an 8% larger output resistance:

$$R_o = r_{o1,\max\_gain}\left(g_{m,max}\frac{R_s}{2}+1\right)||r_{o5} \approx 1.45K\Omega \qquad \text{(Eq. 2.59)}$$

Where $g_{m,max} \approx 10mS, r_{o1,\max_{gain}} \approx 1.3K, r_{o5} \approx 3.9K\Omega$, and $R_s = 160\Omega$.

At minimum gain setting, simulation results indicate no change in output capacitance, as expected:

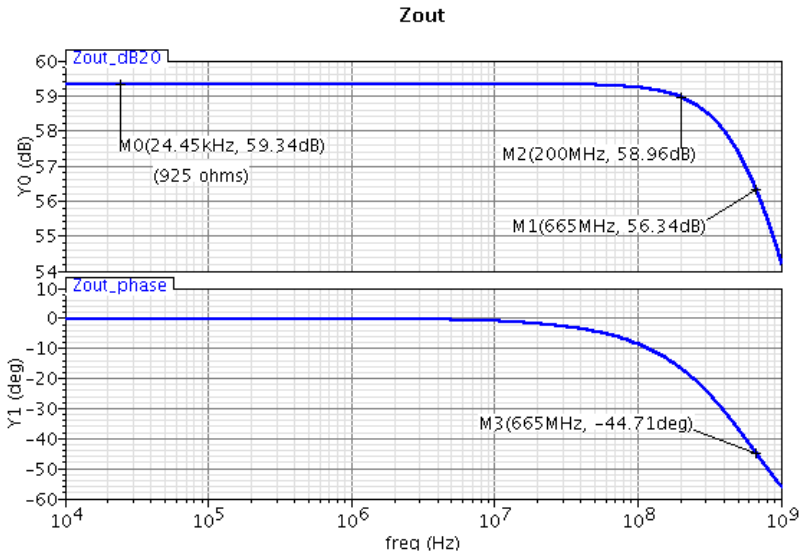

Figure 31: VGCA output impedance vs. frequency at minimum gain setting – default terminations – schematic simulation result

$$R = 925\Omega\ (\text{DC}), s = j2\pi(665MHz) \xrightarrow{yields} C = 260fF \qquad \text{(Eq. 2.60)}$$

The hand calculations predict a 23% larger output resistance:

$$R_{o,\min_{gain}} = r_{o1,\max\_gain}\left(\frac{g_{m,max}}{2}\frac{R_s}{2} + 1\right)||r_{o5} \approx 1.24K\Omega \qquad \text{(Eq. 2.61)}$$

For a shorted source resistance, the output impedance is constant and at its lowest value across all gain states, as expected. The simulation results obtained at $200MHz$ are shown in figure below:

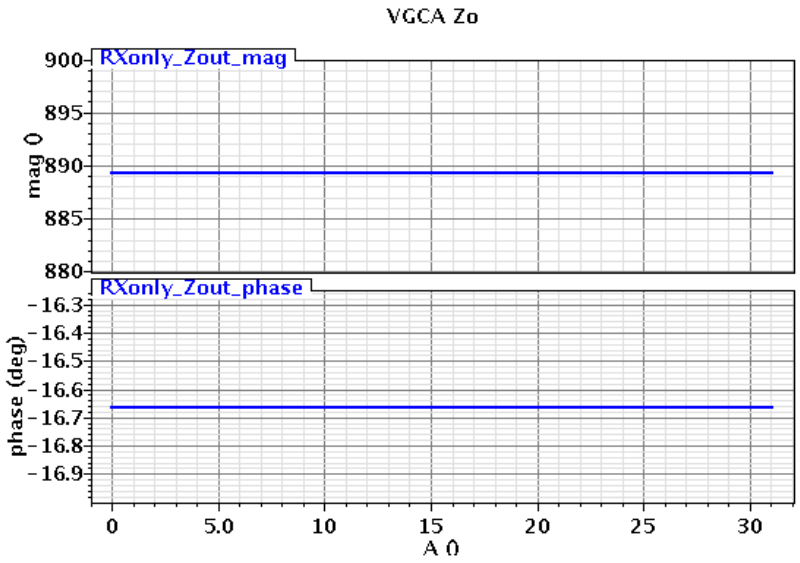

Figure 32: VGCA output impedance vs. gain state – $Rs = 0$ – schematic simulation result

2.3.3 Current Gain

Current gain is next simulated for the typical terminations at $200MHz$. Based on output resistance simulations, the deviation of current gain from ideal unity gain is 5%:

$$\left.\frac{I_o}{I_i}\right|_{\max\_gain} = \mp\frac{Y_L}{Y_o + Y_L}\frac{\sum_{i=0}^{4} 2^i}{2^5 - 1} \approx \mp 0.95 \qquad \text{(Eq. 2.62)}$$

Where $Y_L = 1/Z_L \approx 20m\Omega^{-1}$ and $Y_o = 1/Z_o = 1m\Omega^{-1}$.

Simulation results confirm the expected behavior. Figure 33 below indicates that simulation results across all gain states are within 1% of the expected results obtained by hand calculations.

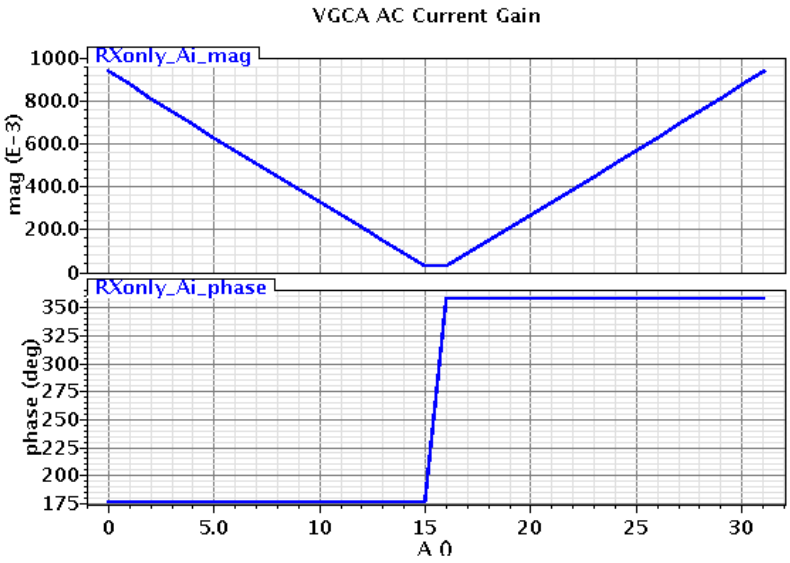

Figure 33: VGCA current gain – default terminations – schematic simulation result

2.3.4 NF

VGCA NF is next simulated. NF increases with decreasing gain. This is expected because the drop in gain is due to drop in transconductance, and the input referred noise increases with decreasing transconductance.

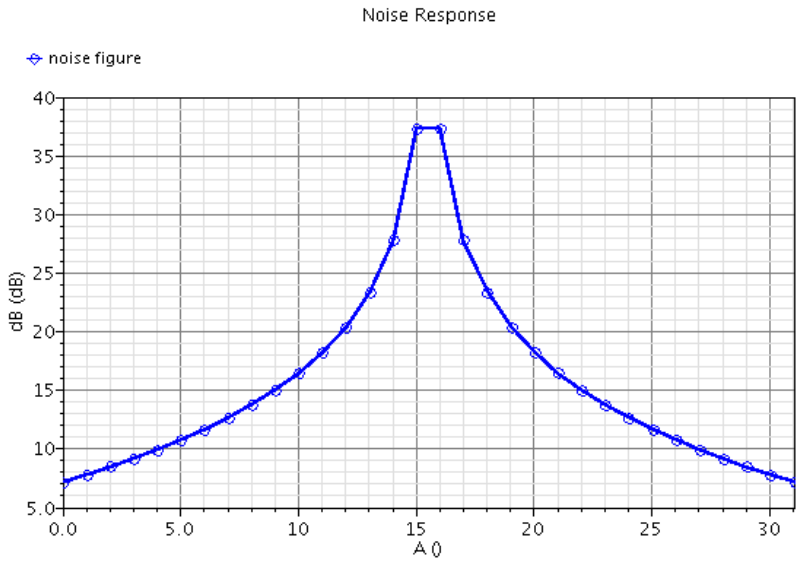

Figure 34: VGCA stand-alone NF at $200MHz$ – 50Ω differential terminations – schematic simulation result

2.4 VGTA

The CS amplifier topology that is the building block of the VGTA is depicted in Figure 35:

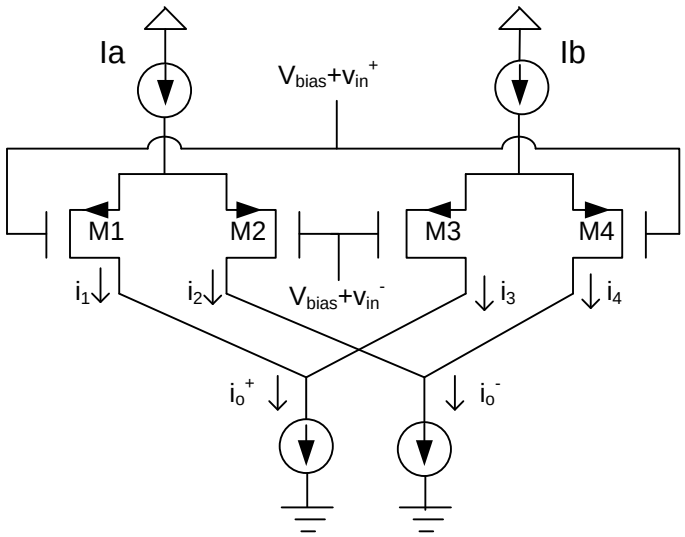

Figure 35: VGTA simplified circuit diagram

This is a current steering circuit consisting of two PMOS differential pairs operating in saturation region. The input signal is injected differentially at the gates of transistors $M_{1,4}$ and $M_{2,3}$, and variable transconductance gain is achieved by varying the bias currents I_a and I_b.

Using a similar approach as the VGCA, the relationship between input voltage and short circuit output current can be determined. Using the square-law model, currents through transistors $M_{1,4}$ are calculated as follows

$$I_1 = \frac{K}{2}\left(V_{SG} - \frac{v_{in}}{2} + V_{TP}\right)^2 = \frac{K}{2}\left[(V_{SG} + V_{TP})^2 + \left(\frac{v_{in}}{2}\right)^2 - v_{in}(V_{SG} + V_{TP})\right] \quad \text{(Eq. 2.63)}$$

$$I_1 = \frac{I_a}{2} - \sqrt{KI_a}\frac{v_{in}}{2} + \frac{K}{2}\left(\frac{v_{in}}{2}\right)^2 \quad \text{(Eq. 2.64)}$$

$$I_2 = \frac{I_a}{2} + \sqrt{KI_a}\frac{v_{in}}{2} + \frac{K}{2}\left(\frac{v_{in}}{2}\right)^2 \quad \text{(Eq. 2.65)}$$

$$I_3 = \frac{I_b}{2} + \sqrt{KI_b}\frac{v_{in}}{2} + \frac{K}{2}\left(\frac{v_{in}}{2}\right)^2 \quad \text{(Eq. 2.66)}$$

$$I_4 = \frac{I_b}{2} - \sqrt{KI_b}\frac{v_{in}}{2} + \frac{K}{2}\left(\frac{v_{in}}{2}\right)^2 \quad \text{(Eq. 2.67)}$$

Where ${v_{in}}^+ = v_{in}/2 = -{v_{in}}^-$.

Using the definition of short circuit output current, $I_{o-sc} = I_{o1} - I_{o2}$, and the fact that $I_{o1} = I_1 + I_3$ and $I_{o2} = I_2 + I_4$, the short circuit output current is determined as:

$$I_{o-sc} = v_{in}\sqrt{K}\left(\sqrt{I_a} - \sqrt{I_b}\right) \quad \text{(Eq. 2.68)}$$

Short circuit forward transfer admittance, as shown in (Eq. 2.68) above, is variable and a function of input bias currents I_a and I_b. The CS topology ensures high input and output impedances. The CS Amplifier of Figure 35 is referred to as VGTA.

2.4.1 Digital Control of Transadmittance

To achieve discrete transconductance gain states by means of bias current steering, a binary-weighted DAC has been implemented and shown in Figure 36:

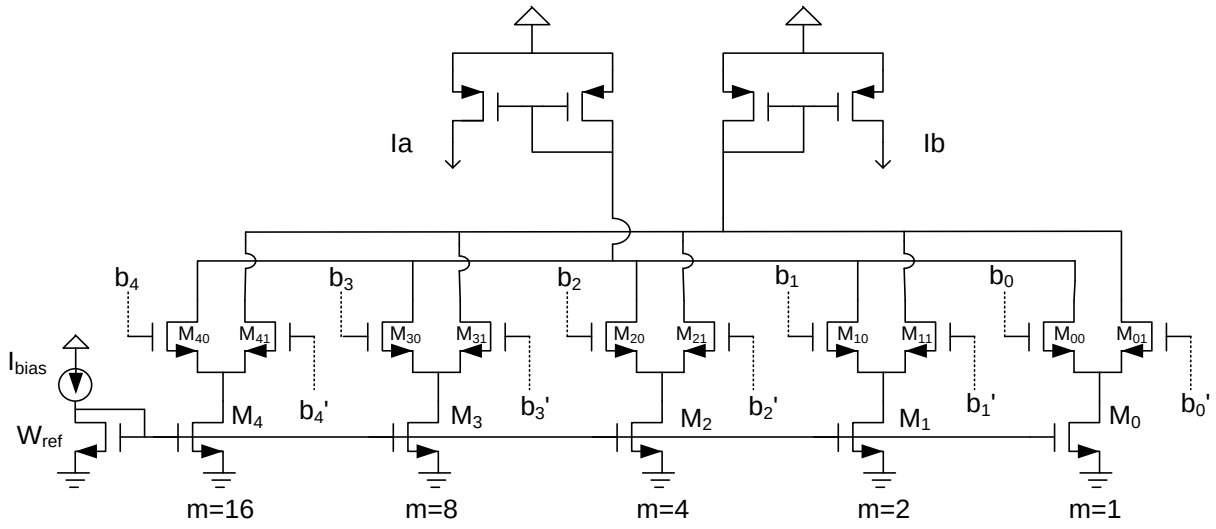

Figure 36: VGTA variable bias current circuit diagram

Figure 36 depicts the current steering DAC (Digital voltage to Analog current) that supplies the binary weighted analog bias currents I_a and I_b to the VGTA using the five bit control word B. NMOS transistors M_j $(j = 0, 1, 2, 3, 4)$ constitute current mirror transistors whose drain currents are proportional to the reference current I_{bias}. The multiplication factor, m, corresponds to the number of parallel NMOS transistors with constant transconductance K_o that constitute M_j transistors. The drain current of each transistor, M_j , therefore, is proportional to its multiplication factor, m. Each transistor M_j , is in turn connected at drain to the source terminals of two NMOS transistors above it, M_{j0}, M_{j1} . The gate voltages of M_{j0} transistors are controlled by the five bit control

word $B = [b_4, b_3, b_2, b_1, b_0]$. The bitwise NOT values of control word B, $\bar{B}$, controls the gate voltages of transistors M_{j1}. Each bit represents a logical high or low value that turns the transistor ON (conducting) or OFF (non-conducting), respectively. The bitwise NOT operation ensures that only one of the adjacent transistors is conducting the drain current of transistors M_j for any value of control word B. Finally, the drain currents of M_{j0} transistors are mirrored through use of a PMOS current mirror, producing the bias supply current I_a. Bias supply current I_b is produced similarly from drain currents of transistors M_{j1}. Currents I_a. and I_b are therefore determined as follows:

$$I_a = I_{bias}\frac{W_o}{W_{ref}}\sum_{i=0}^{4} 2^i b_i \qquad \text{(Eq. 2.69)}$$

$$I_b = I_{bias}\frac{W_o}{W_{ref}}\sum_{i=0}^{4} 2^i \overline{b_i} \qquad \text{(Eq. 2.70)}$$

$$\sqrt{I_a} - \sqrt{I_b} = \sqrt{I_{bias}\frac{W_o}{W_{ref}}}\left(\sqrt{\sum_{i=0}^{4} 2^i b_i} - \sqrt{\sum_{i=0}^{4} 2^i \overline{b_i}}\right) \qquad \text{(Eq. 2.71)}$$

The overall transfer function of the VGTA is obtained by substituting (Eq. 2.26) on page 26 in (Eq. 2.68) on page 46:

$$Y_f \equiv \frac{I_{o-sc}}{v_{in}} = \sqrt{K}\sqrt{I_{bias}\frac{W_o}{W_{ref}}}\left(\sqrt{\sum_{i=0}^{4} 2^i b_i} - \sqrt{\sum_{i=0}^{4} 2^i \overline{b_i}}\right) \qquad \text{(Eq. 2.72)}$$

Where I_{o-sc}/v_{in} is the short circuit forward transfer admittance parameter of the VGTA, Y_f. Figure 37 is a plot of Y_f vs. control word B normalized to $\sqrt{K}\sqrt{I_{bias}\frac{W_o}{W_{ref}}}$.

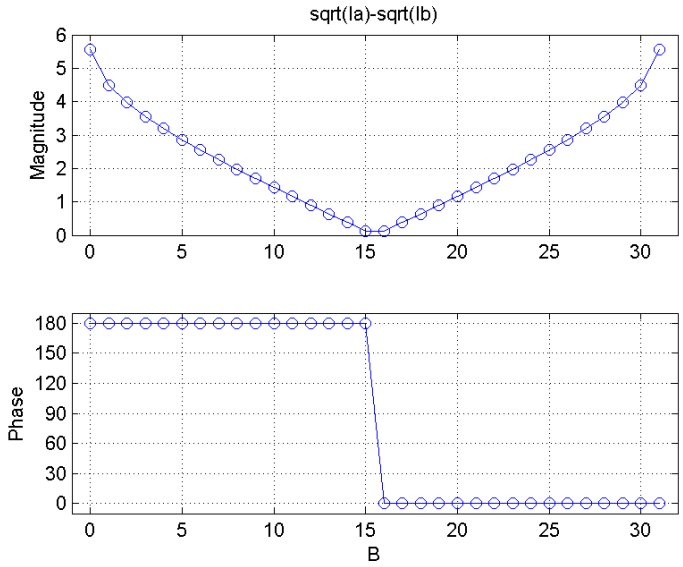

Figure 37: VGTA transconductance – ideal – normalized

As will be observed in section 2.5.3:*Transadmittance* , CLM effects on multiplying NMOS transistors can noticeably degrade the proposed current-steering DAC's differential and integral nonlinearity errors (DNL and INL errors). To alleviate this issue, cascading of the current mirroring devices to increase output resistance and/or adjustment of the aspect ratio of NMOS switches for constant overdrive voltage therefore achieving constant V_{DS} is suggested as future design improvements. Measurement results that will be presented in Chapter 6 indicate the effects of mismatch on worsening of the INL and DNL. Further improvements in matching and reduction of area may be achieved as design and experimental results of Gupta and Saxena suggest using a slightly modified version of the current-steering DAC presented in this thesis. The architecture, which uses a W-2W MOSFET sizing scheme (similar to the well-known R-2R ladder) is originally introduced in [9] and experimental results were presented by Gupta and Saxena

in [10]. Following figure is the slightly modified version of W-2W current steering DAC:

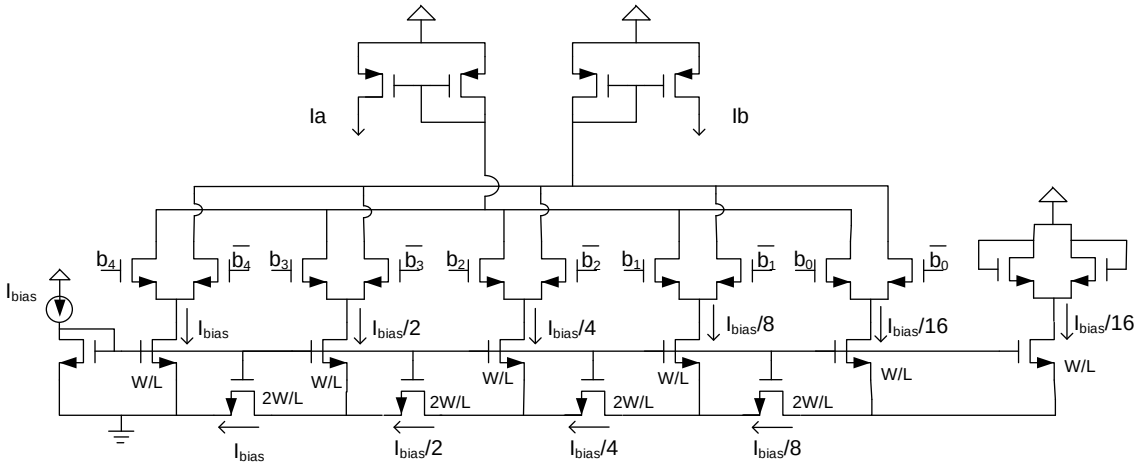

Figure 38: Binary-weighted DAC with W-2W implementation

The main advantage of the W-2W architecture is the reduction in area, and improved matching due to use of MOSFETs with equal aspect ratios.

2.4.2 Input Impedance

The input impedance of VGTA and its variations with load resistance is calculated in Appendix D and results are repeated here for convenience. Referring to Figure 39 below:

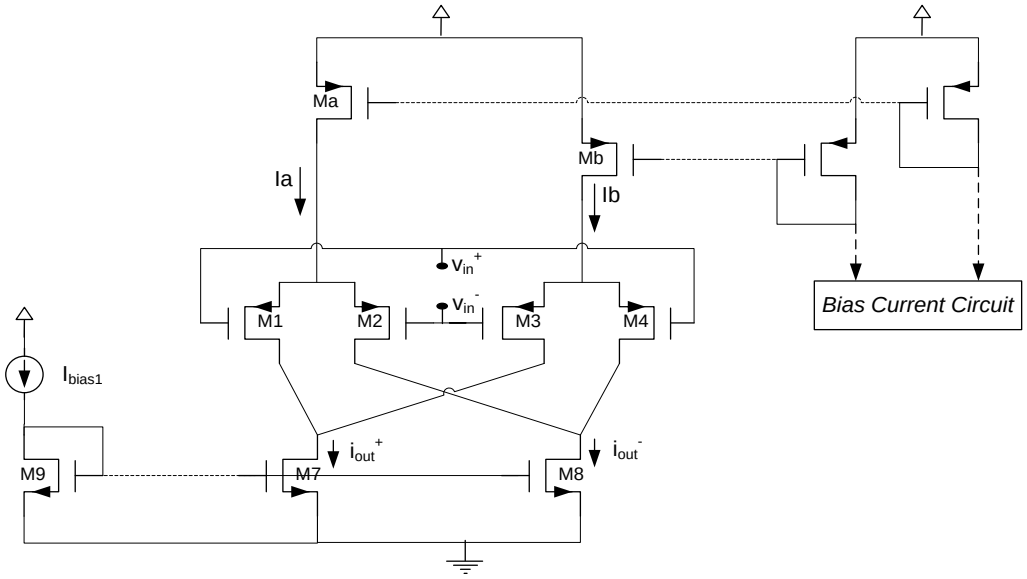

Figure 39: VGTA simplified circuit diagram

$$Z_{in,maxgain} \approx \frac{1}{\left[C_{gs1} + 3C_{ol} + \frac{R_L}{2}\left(g_{m1,max}C_{ol}\right)\right]s} \quad \text{(Eq. 2.73)}$$

$$Z_{in,\min gain} \approx \frac{1}{\left[2C_{gs1} + 2C_{ol} + \frac{R_L}{2}\left(\sqrt{2}g_{m1,max}C_{ol}\right)\right]s} \quad \text{(Eq. 2.74)}$$

Where C_{ol} refers to the gate-diffusion overlap capacitance.

2.4.3 Output Impedance

The output resistance of the VGTA is the parallel combination of output resistance of transistors M_7, M_1, and M_3:

$$R_{out} = r_{o7} || r_{o1} || r_{o3} = r_{o8} || r_{o2} || r_{o4} \quad \text{(Eq. 2.75)}$$

$$R_{out} = \frac{2}{\lambda_N(I_a + I_b)} || \left(\frac{2}{\lambda_p I_a} || \frac{2}{\lambda_p I_b}\right) = \frac{2}{\lambda_N(I_a + I_b)} || \frac{2}{\lambda_P(I_a + I_b)} \quad \text{(Eq. 2.76)}$$

If we assume the n-channel and p-channel MOS devices have equal channel modulation parameters, the output resistance will reduce approximately to:

$$R_{out} \approx \frac{1}{\lambda(I_a + I_b)} \quad \text{(Eq. 2.77)}$$

Substituting (Eq. 2.69) and (Eq. 2.70) on page 48 into this equation yields:

$$R_{out} \approx \frac{W_{ref}}{(2^5 - 1)\lambda I_{bias} W_o} \quad \text{(Eq. 2.78)}$$

The effect of varying gain on the output resistance is studied in Appendix E and the results are repeated here for convenience:

$$R_{o,maxgain} = \frac{6}{I_{a,max}(3\lambda_n + \lambda_p)} \quad \text{(Eq. 2.79)}$$

$$R_{o,mingain=} = \frac{14}{I_{a,max}(7\lambda_n + 3\lambda_p)} \quad \text{(Eq. 2.80)}$$

Assuming $\lambda_n \approx \lambda_p$,:

$$R_{o,maxgain} \approx \frac{15}{14} R_{o,mingain} \quad \text{(Eq. 2.81)}$$

2.4.4 Equivalent Circuit

The VGTA is represented with its Y parameter equivalent circuit in figure below:

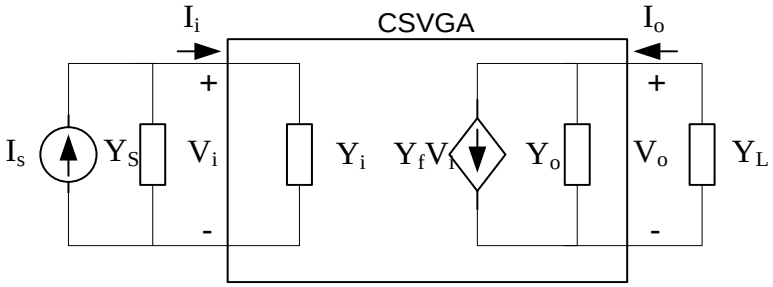

Figure 40: VGTA y-parameter equivalent circuit

Here, Y_i, Y_o , and Y_f are the short circuit input, output, and forward transfer admittances, respectively. Y_S and Y_L are the source and load admittances. The amplifier

is assumed to be completely unilateral, thus omitting the short circuit reverse transfer admittance parameter, Y_r .

The VGTA's transfer transadmittance is determined as follows:

$$I_i = Y_i V_i \quad \text{(Eq. 2.82)}$$

$$I_o = Y_f V_i + Y_o V_o \quad \text{(Eq. 2.83)}$$

$$\frac{I_o}{V_i} = Y_f \frac{Y_L}{Y_o + Y_L} \quad \text{(Eq. 2.84)}$$

(Eq. 2.84) implies that for output admittance much smaller than load admittance, the transfer transadmittance value is almost independent of load admittance and is equal to the short circuit transfer admittance:

$$\frac{I_o}{V_i} = Y_f \frac{Y_L}{Y_o + Y_L} \approx Y_f, for\ Y_o \ll Y_L \quad \text{(Eq. 2.85)}$$

2.4.5 CMFB

The CMFB configuration used to bias the output common mode voltage of the VGTA is similar in architecture and theory of operation to the CMFB circuit used to control the common mode voltage at the output of the VGCA. The configuration is shown in the figure below.

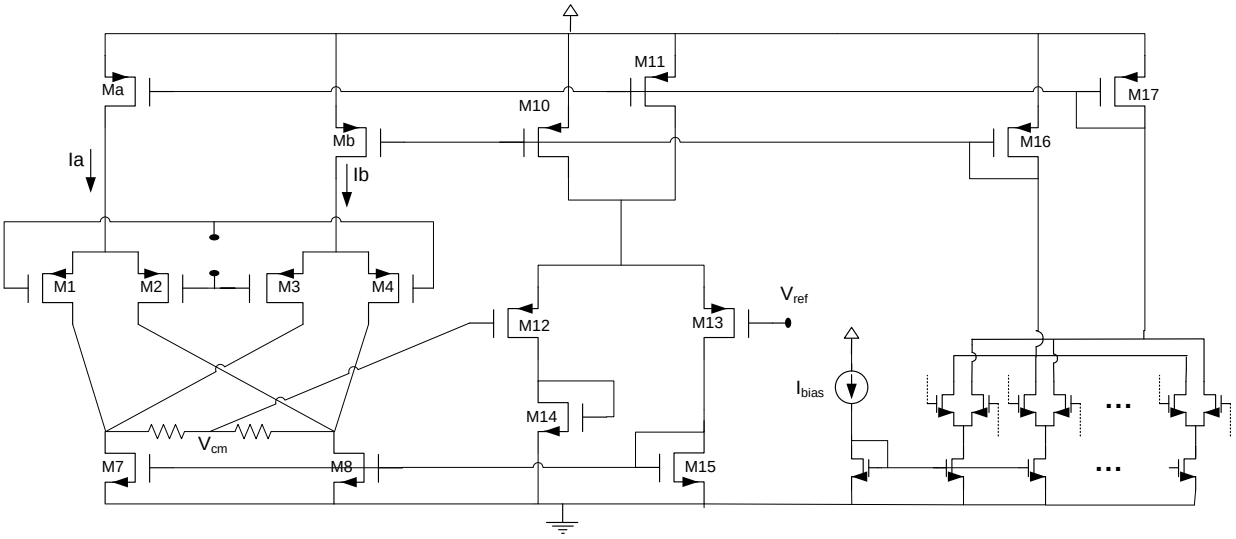

Figure 41: VGTA circuit diagram with CMFB

The operation of the CMFB can be summarized as follows: Current sourcing transistors M_{10} and M_{11} are biased using the same diode connected PMOS transistors used to set the currents in M_a and M_b. This ensures that the CMFB network draws a DC current proportional to $I_a + I_b$. As long as the network is biased properly, this current is then divided equally between each leg of the CMFB network. Diode connected NMOS transistor, M_{15}, then mirrors this current, proportional to $(I_a + I_b)/2$, onto the current sinking transistors M_7 and M_8. Setting M_{15} width to be half that of M_{10} and M_{11}, ensures that the sum of sink currents in M_7 and M_8 is equal to the sum of source currents in M_a and M_b and equal to $I_a + I_b$.

The negative feedback nature of the network is evident by inspection. Similar to the VGCA, the output common mode voltage of the VGTA is sensed using a resistive sensing network. An increase (decrease) in common mode voltage decreases (increases) the current in M_{12}, subsequently increasing (decreasing) the current in M_{13}. This

increase (decrease) in current causes an increase (decrease) in the gate voltages of transistors M_{15}, M_7, and M_8, therefore decreasing (increasing) the output common mode voltage.

The loop gain is next calculated in a similar fashion to the VGCA CMFB. The feedback loop is opened in an appropriate point and a test signal is injected in the direction of feedback. Figure below shows the setup:

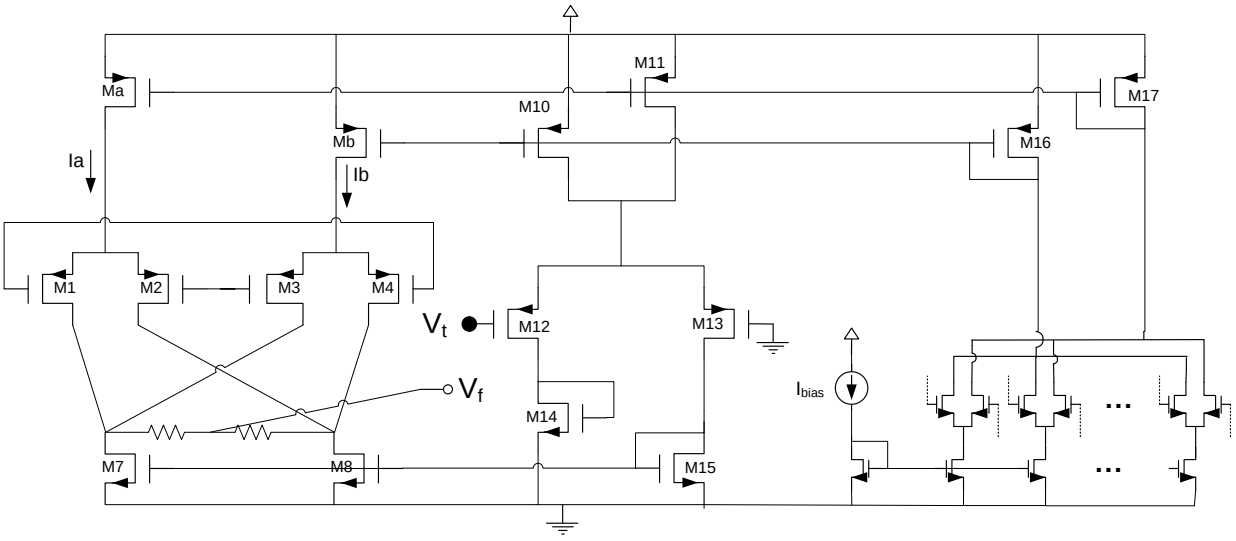

Figure 42: VGTA CMFB loop gain analysis

The loop gain, can be calculated by inspection. It is assumed that $g_{m12} = g_{m13}$, $g_{m14} = g_{m15}$, and $g_{m7} = g_{m8}$:

$$-\frac{v_f}{v_t} = \frac{g_{m7} g_{m12} R_o}{g_{m15}} \qquad \text{(Eq. 2.86)}$$

The dominant pole is at:

$$p_1 = -\frac{1}{R_o C_p} \quad \text{(Eq. 2.87)}$$

Where C_p is the parasitic capacitance at the output node of the VGTA. Further CMFB simulation results and analysis are presented in Appendix F.

2.4.6 DC Biasing

The DC characteristics of the VGTA is studied next. Assuming a maximum gain state, where transistors M_a, M_1, M_2 and M_7 carry maximum DC current, the gate bias voltage range of transistors M_{1-4} is:

$$V_{od7} - |V_{TP}| < V_{bias} < V_{DD} - V_{od,Ma} - V_{SG,M1,M2} \quad \text{(Eq. 2.88)}$$

$$-330mV < V_{bias} < 1.04V \quad \text{(Eq. 2.89)}$$

Where $V_{od7} \approx 70mV, |V_{TP}| \approx 400mV, V_{DD} = 1.8V, V_{od,Ma} \approx 200mV$, and $V_{SG,M1,M2} \approx 560mV$.

The input and output common mode range is then:

$$-V_{bias} - 330mV < v_{in} < 1.04 - V_{bias} \quad \text{(Eq. 2.90)}$$

$$-800mV < v_{in} < 400mV \quad \text{(Eq. 2.91)}$$

$$V_{od7,8} < v_{out} < V_{bias} + |V_{TP}| \quad \text{(Eq. 2.92)}$$

$$70mV < v_{out} < 1V \quad \text{(Eq. 2.93)}$$

Where $V_{bias} \approx 600mV$. With the output common mode voltage set to 550mV, the input and output differential voltage swing is therefore:

$$-400mV < v_{in} < 400mV \quad \text{(Eq. 2.94)}$$

$$-450mV < v_{out} < 450mV \quad \text{(Eq. 2.95)}$$

DC Bias currents and output common mode voltage for all gain settings is shown below:

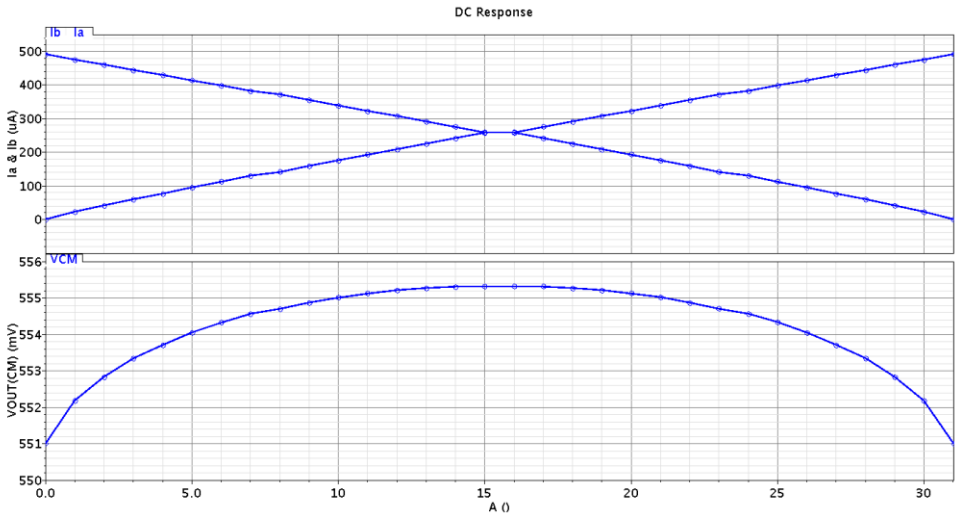

Figure 43: VGTA DC currents and output common mode voltage vs. gain states – schematic simulation result

2.4.7 PMOS Second Order Effects

The body effect affects all PMOS transistors whose source terminal is at a potential lower than their substrate. A positive VBS increases the threshold voltage of the PMOS transistors above the zero-substrate-bias value of the threshold voltage:

$$|V_{TP}| = V_{TO} + \gamma\left(\sqrt{V_{BS} + 2\phi_F} - \sqrt{2\phi_F}\right) \quad \text{(Eq. 2.96)}$$

Where:

$$V_{TO} = zero - substrate - bias\ value\ for V_{TP}\ (V)$$

$$\gamma = body - effect\ parameter\ \left(\sqrt{V}\right)$$

$$2\phi_F = surface\ potential\ parameter\ (V)$$

A reduction of the threshold voltage, on the other hand, is introduced by the secondary effect of Drain Induced Barrier Lowering, or DIBL. As the PMOS source potential increases, the depletion region of the p-n junction between the source and body increases in size and extends under the gate, requiring a smaller gate potential to invert the channel, thus reducing the threshold voltage. This effect is more amplified at smaller channel lengths. DIBL results in an increase in drain current at a given gate potential.

Figure below is an attempt to understand the above effects in our technology.

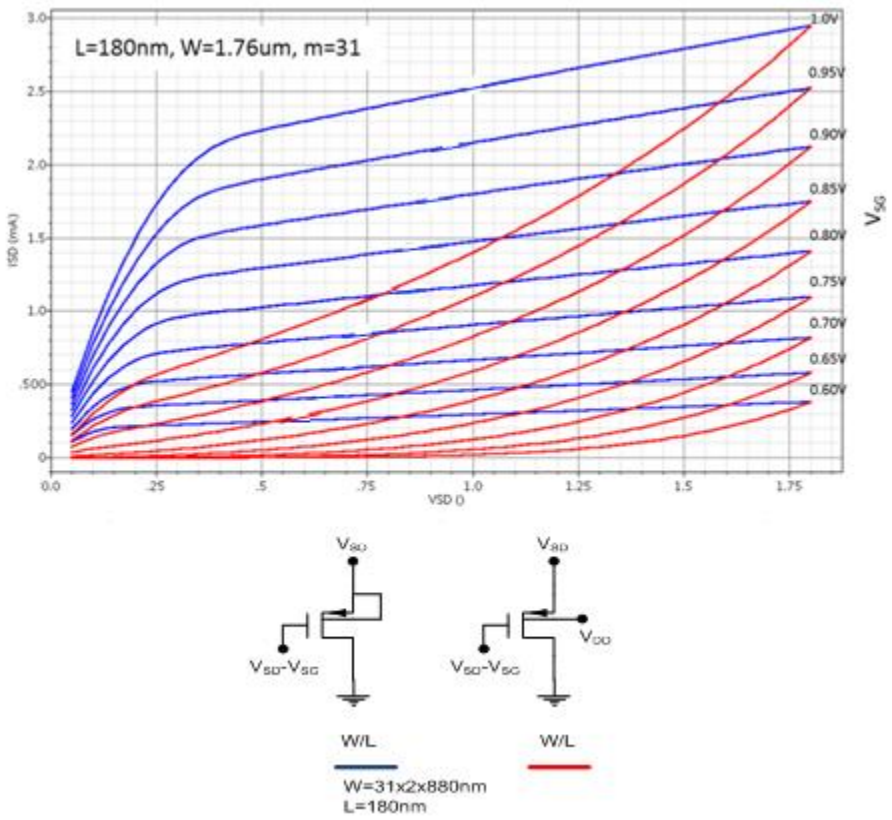

Figure 44: PMOS I_{SD} vs. V_{SD} curves illustrating body effect and channel length modulation – schematic simulation result

From figure above it is clear that the body effect has a significant effect on the device performance. As the potential between the body and source increases, the threshold voltage increases, resulting in a drop in overdrive voltage, the drain-source current, and the device transconductance. The body effect on all PMOS devices used in VGTA is similar and proportional to the plot shown above. To eliminate this effect, all PMOS bodies are tied to their source terminals (Hot NWELLs).

2.5 VGTA Schematic Simulation Results

2.5.1 Input Impedance

VGTA input impedance is simulated for all gain settings and typical loads. The setup is shown in Figure 45:

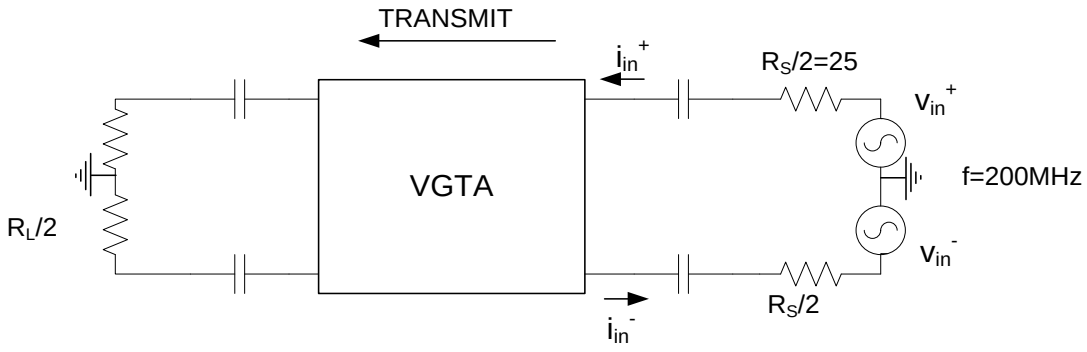

Figure 45: VGTA input impedance simulation setup

The input impedance is shown below. It is noted that the input impedance is almost entirely capacitive, as expected.

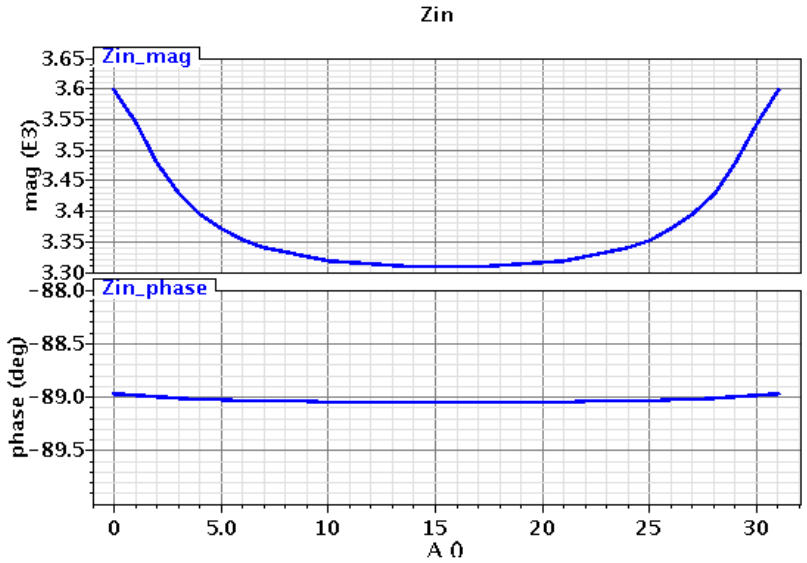

Figure 46: VGTA input impedance – default terminations – schematic simulation result

Comparison of the calculated versus simulated input impedance is shown below. The hand-calculated input impedance for maximum and minimum gain settings as calculated in Appendix D are:

$$Z_{in,maxgain} \approx \frac{1}{\left[C_{gs1} + 3C_{ol} + \frac{R_L}{2}\left(g_{m1,max}C_{ol}\right)\right]s} \quad \text{(Eq. 2.97)}$$

$$\left|Z_{in,maxgain}\right|_{f=200MHz} \approx 3.47k\Omega \quad \text{(Eq. 2.98)}$$

$$Z_{in,\min gain} \approx \frac{1}{\left[2C_{gs1} + 2C_{ol} + \frac{R_L}{2}\left(\sqrt{2}g_{m1,max}C_{ol}\right)\right]s} \quad \text{(Eq. 2.99)}$$

$$\left|Z_{in,mingain}\right|_{f=200MHz} \approx 2.7k\Omega \quad \text{(Eq. 2.100)}$$

Where

$$g_{m1,max} = 2.86mS, R_L = 160\Omega, C_{gs1} \approx 100fF, and\ C_{ol} \approx C_{gs}\big|_{cutoff} \approx 40f$$

Hand calculated impedance is about 4% lower than simulation results at maximum gain settings ($3.47k\Omega$ vs. $3.6k\Omega$) and about 18% lower at minimum gain settings ($2.7k\Omega$ vs. $3.3k\Omega$).

2.5.2 Output Impedance

The simulation setup for output impedance is shown below:

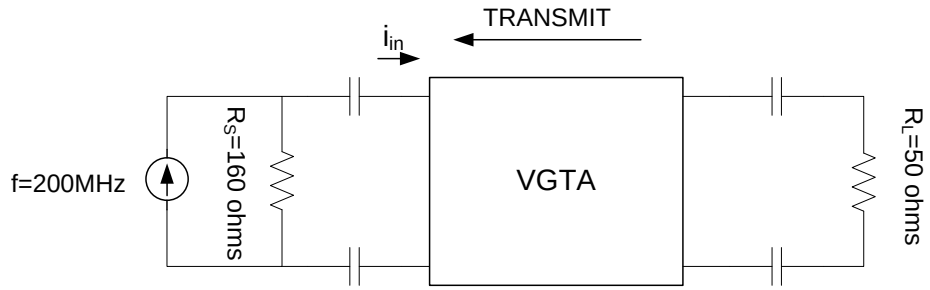

Figure 47: VGTA output impedance simulation setup

Simulation results of the output impedance at all gain settings is shown below:

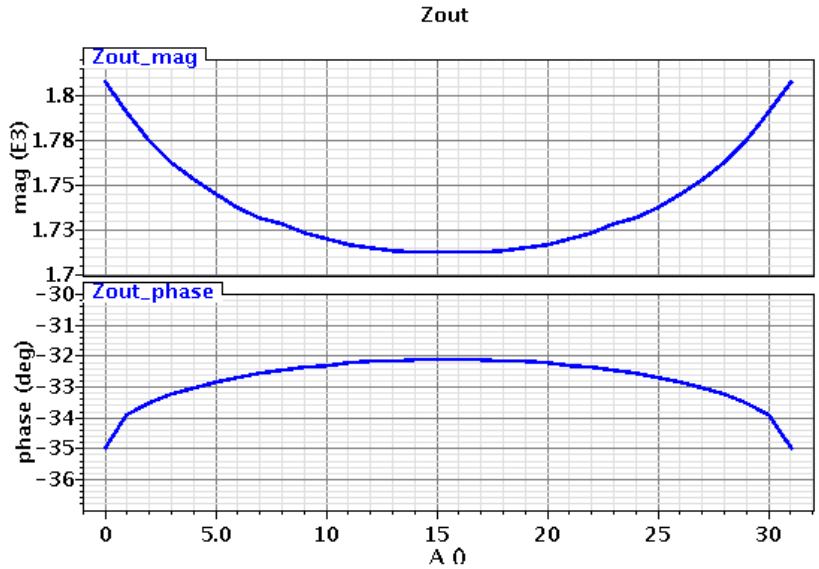

Figure 48: VGTA output impedance vs. gain states – default terminations – schematic simulation result

The output resistance, as expected, is slightly higher at maximum gain setting compared to the minimum. This confirms the relationship between the output resistance at maximum and minimum gain settings that was computed in Appendix D and is repeated here.

$$\frac{R_{o,maxgain}}{R_{o,mingain}} \approx \frac{15}{14} \qquad \text{(Eq. 2.101)}$$

To verify the above relationship, the simulated output resistance at maximum and minimum gain settings can be estimated by plotting the simulated output impedance versus frequency at both the minimum and maximum gain settings:

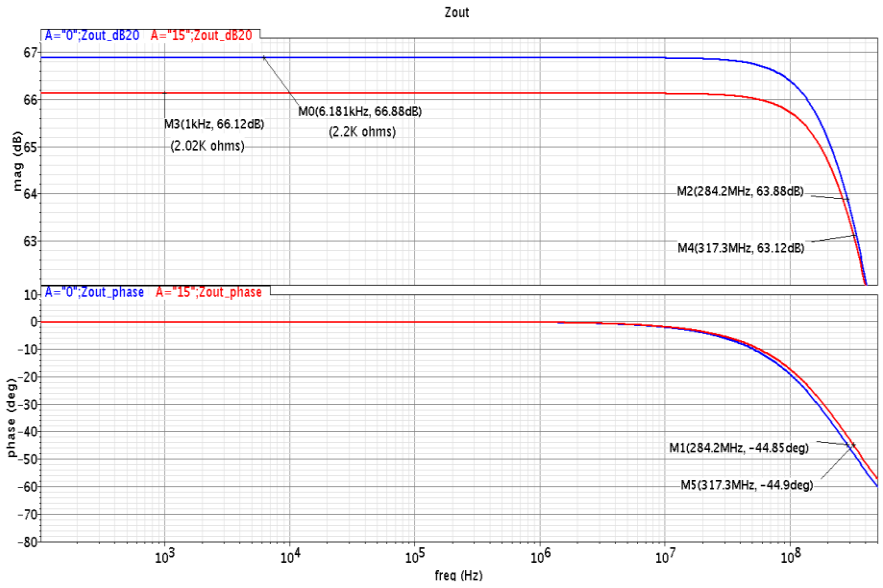

Figure 49: VGTA output impedance at maximum and minimum gain settings vs. frequency – default terminations – schematic simulation result

Simulated output impedance at maximum and minimum gain settings, from figure above, are:

$$R_{o,maxgain} = 2.2k\Omega, C_{out,maxgain} \approx 250\text{fF} \qquad \text{(Eq. 2.102)}$$

$$R_{o,mingain} = 2.02k\Omega, C_{out,mingain} \approx C_{out,maxgain} \quad \text{(Eq. 2.103)}$$

Simulation results confirm this relationship:

$$\frac{R_{o,maxgain}}{R_{o,mingain}} = \frac{2.2K\Omega}{2.02K\Omega} = \frac{15.25}{14} \quad \text{(Eq. 2.104)}$$

The expression for the output resistance at minimum and maximum gain settings is calculated in Appendix E and can be evaluated for comparison. The expression for output resistance is repeated here for convenience:

$$R_{o1} = g_{m1} r_{o1} R_{s,M2} + r_{o1} + R_{s,M2} \quad \text{(Eq. 2.105)}$$

$$R_{o3} = g_{m3} r_{o3} R_{s,M2} + r_{o3} + R_{s,M2} \quad \text{(Eq. 2.106)}$$

$$R_o = r_{o7} || R_{o1} || R_{o3} || 10k\Omega \text{ [10]} \quad \text{(Eq. 2.107)}$$

Table 2 shows the output resistance calculation results using the equation above. The values of parameters in greyed out cells are obtained using DC operating point simulation results at appropriate gain settings

Gain Setting / Device Parameter	Min	Max
g_{m1}	$2.86mS$	$1.9mS$
g_{m2}	$2.86mS$	$1.9mS$
r_{o1}	$8.26k\Omega$	$13.3k\Omega$
r_{o3}	$110M\Omega$	$13.3k\Omega$
r_{o7}	$4.29k\Omega$	$4.08k\Omega$

[10] The $10k\Omega$ resistance is the common mode sense resistor that appears in parallel with the VGTA output resistance. This resistor was omitted from calculations in the appendix for simplicity

$R_{s,M2}$	$\frac{2}{g_{m2}}$	$\frac{4}{3g_{m2}}$
R_{o1}	$25.4k\Omega$	$40.9k\Omega$
R_{o3}	$\approx \infty$	$40.9k\Omega$
$\boldsymbol{R_o}$	$\mathbf{2.68k\Omega}$	$\mathbf{2.54k\Omega}$

Table 2: VGTA output resistance calculation results. Greyed out parameters are obtained using DC operating point information at appropriate gain settings

Hand calculated output resistance is 20% higher than simulation results suggest at minimum gain setting ($2.68k\Omega$ hand calculation, $2.2k\Omega$ simulation result) and 25% higher in maximum gain setting ($2.54k\Omega$ hand calculation, $2.02k\Omega$ simulation result).

2.5.3 Transadmittance

VGTA Transadmittance is next simulated for various gain settings and typical terminations at $200MHz$:

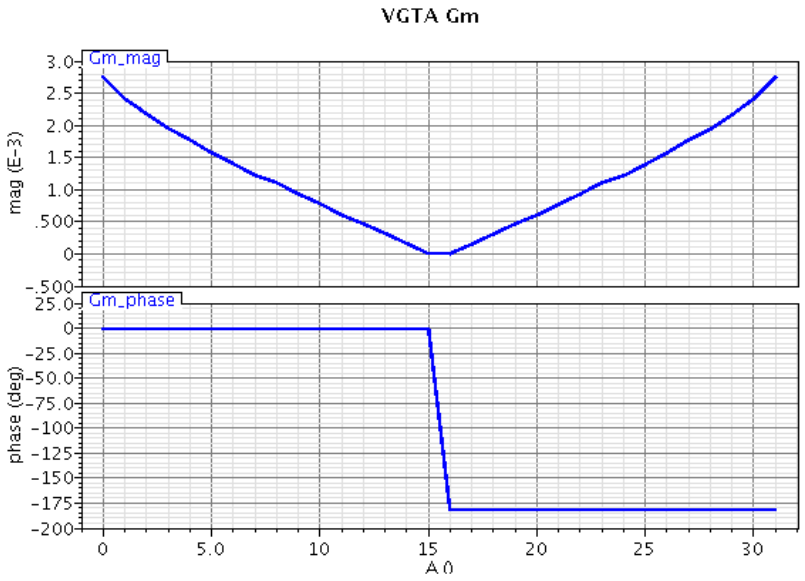

Figure 50: VGTA transadmittance– default terminations – schematic simulation result

The simulated transadmittance is next compared to the value obtained by substituting the VGTA forward short circuit transadmittance parameter (Eq. 2.72) on page 48) into (Eq. 2.84) on page 53:

$$Y_f = \frac{Y_L}{Y_o + Y_L}\sqrt{K}\sqrt{I_{bias}\frac{W_o}{W_{ref}}}\left(\sqrt{\sum_{i=0}^{4} 2^i b_i} - \sqrt{\sum_{i=0}^{4} 2^i \overline{b_i}}\right) \qquad \text{(Eq. 2.108)}$$

Where:

$$Y_L = \frac{1}{160}\Omega^{-1}, Y_o \approx 1.8K\measuredangle(-35^o), K' \approx 66.6\frac{uA}{V^2}[11], W_{m1} = 54.56um, L_{m1} = 180nm, I_{bias}$$

$$= 580uA, W_o = 1.76um, and\ W_{ref} = 54.56um$$

Figure 51 shows the comparison between the VGTA transconductance obtained using hand-calculations and simulation results:

---

[11] Value provided by MOSIS from lot average results obtained from measurements of MOSIS test structures on wafers of a fabrication lot.

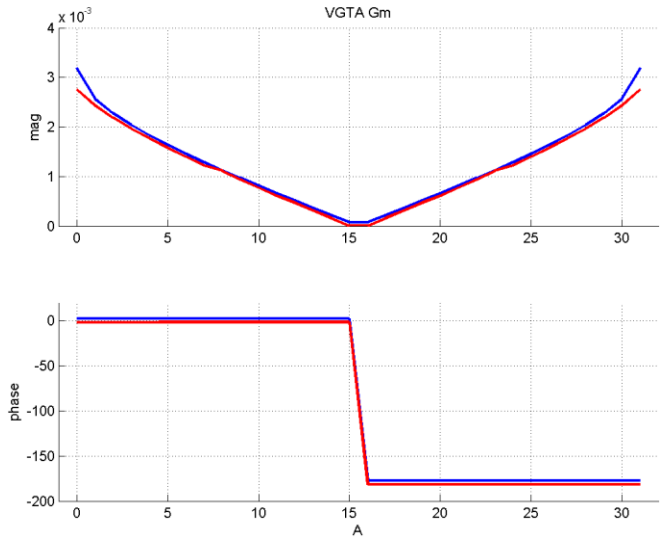

Figure 51: VGTA transadmittance – default terminations – ideal (Blue) vs. schematic simulation result (Red)

To understand the differences between the simulation results and hand calculations, the zoomed in version of the magnitude of plot above is shown below:

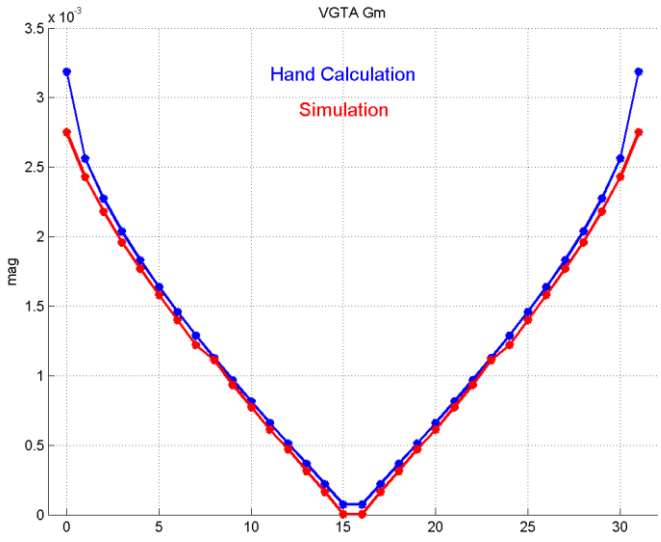

Figure 52: VGTA transadmittance magnitude – default termination – ideal (Blue) vs. schematic simulation result (Red)

The slight constant offset observed between the two traces is due to a one-bit integral nonlinearity (INL) error of the current-steering DAC of the VGTA. Due to channel length modulation effect, the current mirroring transistor associated with bit 1 of the control word generates a slightly higher DC current than half of that generated by current mirror transistor associated with bit2, and this trend continues in a cumulative fashion up to the MSB transistor. The current generated in the MSB current mirroring transistor, in fact, is one LSB current (DC current mirrored by the smallest transistor, associated with bit zero, or LSB) smaller than the ideal, and for this reason, at maximum gain setting the difference between the ideal and simulated transconductance is maximum.

Another deviation created by this error can be seen from the step-like behavior of the simulated Transconductance from gain states seven to eight (and 23 to 24). This is because the sum of currents in transistors associated with bits zero to two is less than one LSB of current smaller than the current in transistor associated with bit three. This creates a non-linearity at transitions between these states. This is a smaller error, as can be seen from the plot, than the step from gain states zero to one (and 30 to 31).

2.5.4 NF

VGTA NF is next simulated at $200MHz$ across all gain states. It is noted that NF increases as gain decreases. This is expected because the drop in gain is due to drop in transconductance, and the input referred noise increases with decreasing transconductance.

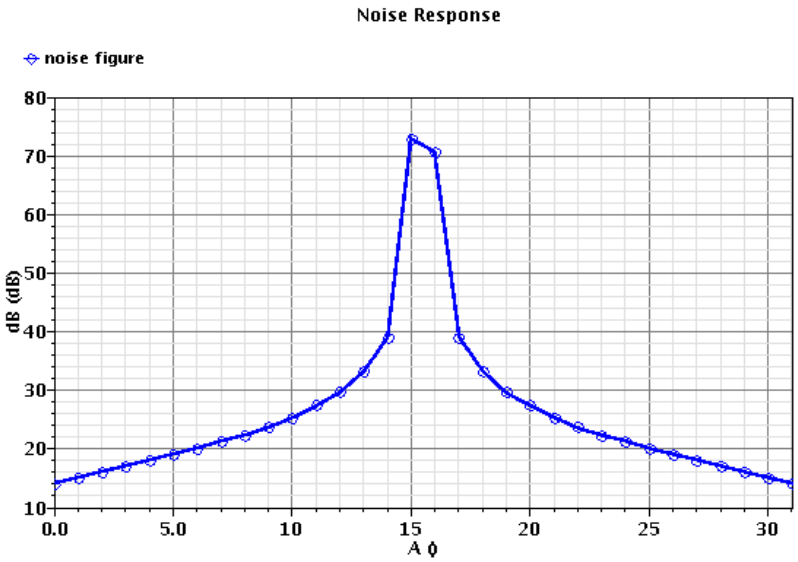

Figure 53: VGTA stand-alone NF at $200MHz$ – 50Ω differential terminations – schematic simulation result

CHAPTER 3

BI-DIRECTIONAL VGA

3.1 System Block Diagram

To achieve bi-directionality for the VGA, the previously discussed VGTA and VGCA are interconnected, as shown conceptually in Figure 54:

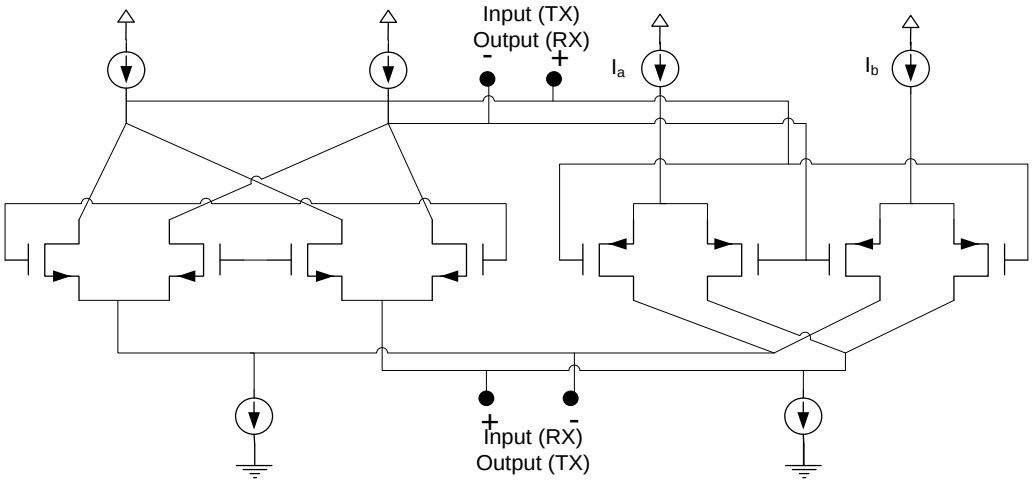

Figure 54: Bi-directional VGA conceptual topology

As shown above, the differential input terminals of the VGCA are connected to the output terminals of the VGTA, and the output terminals of the VGCA are connected to the input terminals of the VGTA, to construct the bi-directional VGA. The following, more detailed schematic shows the interconnections between the two VGA blocks:

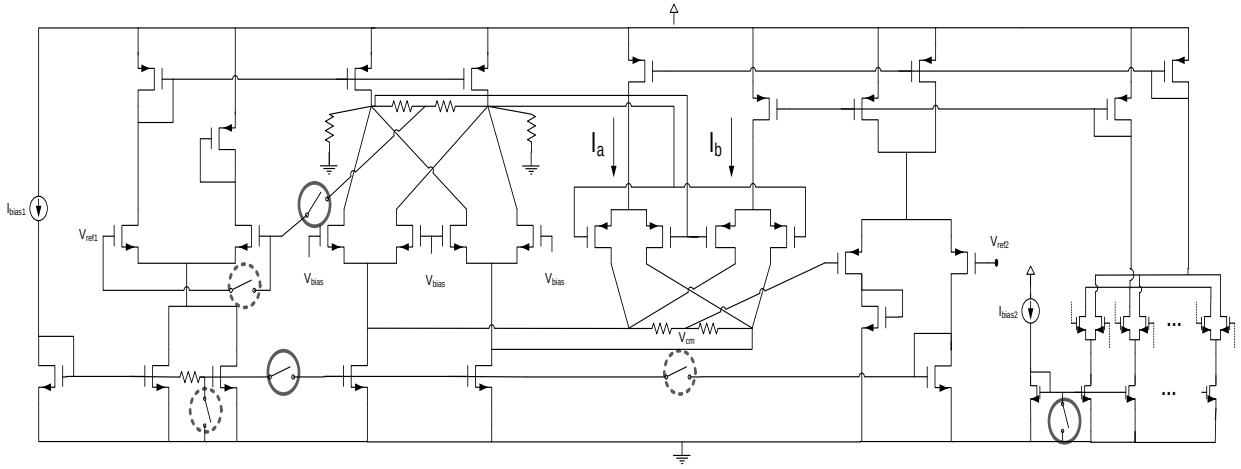

Figure 55: Bi-directional VGA circuit diagram

The switches depicted in Figure 55 are controlled by the DC control voltage V_{ctrl}, and are to ensure proper operation during receive and transmit modes of operation. Switches encircled by solid lines are closed during receive mode of operation, and are open during transmit mode. Similarly, switches encircled by dashed lines are closed during transmit mode of operation, and are open during receive mode of operation. This allows for only the VGCA to be ON during receive mode of operation and only the VGTA to be ON during transmit mode of operation.

3.2 Bi-directional VGA: VGCA

On receive mode, disabling the VGTA is done by reducing the supply bias currents of the PMOS transistors, I_a and I_b, to zero. This is done by disabling the VGTA's 5-bit digital voltage to analog current converter through pulling down the gate voltage of its diode connected biasing NMOS transistor. The VGCA current sink transistor gates need

to be disconnected from the diode connected transistor in VGTA CMFB block as well. The schematic with switches at appropriate positions for receive is shown below:

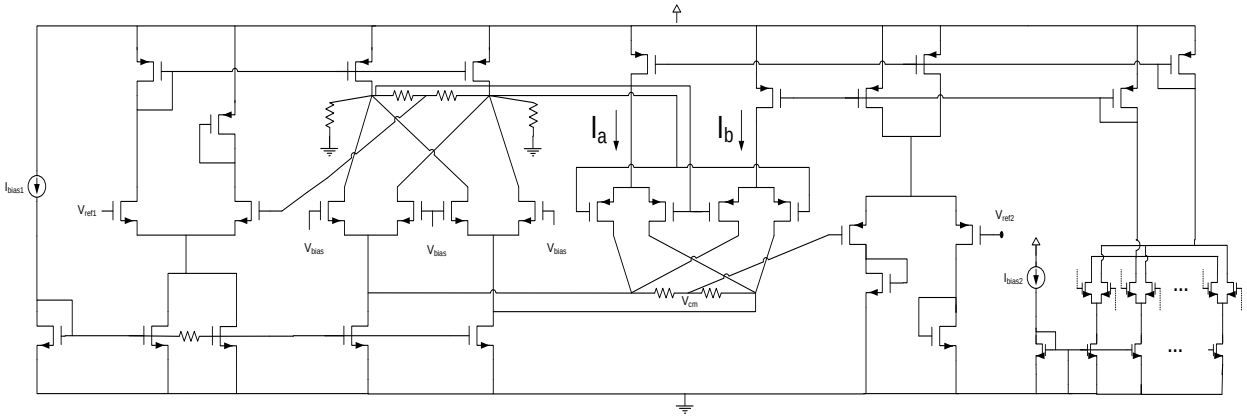

Figure 56: Bi-directional VGA configured as VGCA

To operate as the bi-directional VGCA, the Bi-Directional VGA V_{ctrl} signal is set to low, enabling receive mode of operation, and a suite of simulations are performed.

3.3 Bi-directional VGA: VGCA Schematic Simulation Results

3.3.1 DC

The common mode voltages of the bi-directional VGCA for all gain settings at input and output are identical to the common mode voltages of the stand-alone VGCA, namely:

$$Vcm_{in}{}^{+} = Vcm_{in}{}^{-} = 510mV \quad \text{(Eq. 3.1)}$$

$$Vcm_{out}{}^{+} = Vcm_{out}{}^{-} = 900mV \quad \text{(Eq. 3.2)}$$

3.3.2 Input Impedance

The input impedance simulation is done similar to the input impedance simulations of the VGCA. The results are depicted in Figure 57. Input impedance simulation results are almost identical to what was simulated with the stand-alone VGCA input impedance, the stand-alone results are presented in red.

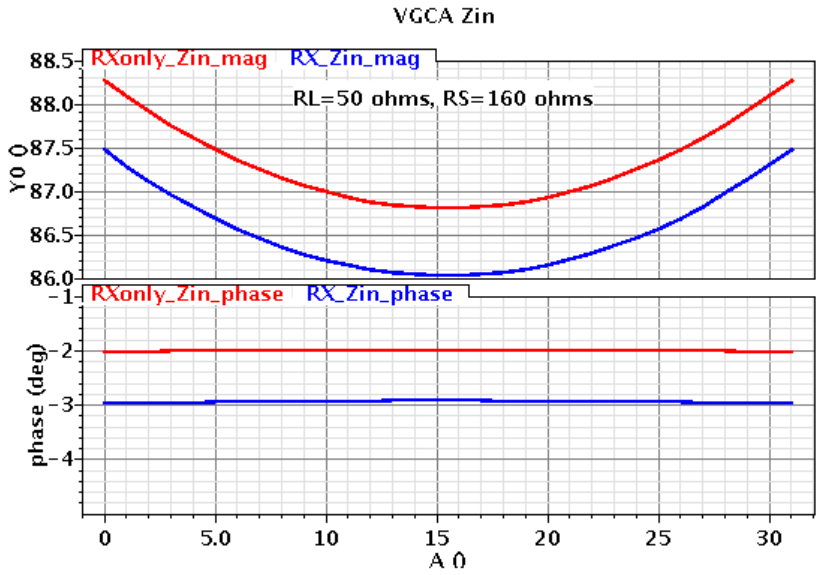

Figure 57: VGCA input impedance – default terminations – schematic simulation result – bi-directional (Blue) vs. stand-alone (Red)

3.3.3 Output Impedance

The output impedance of the bi-directional VGCA is similarly plotted below:

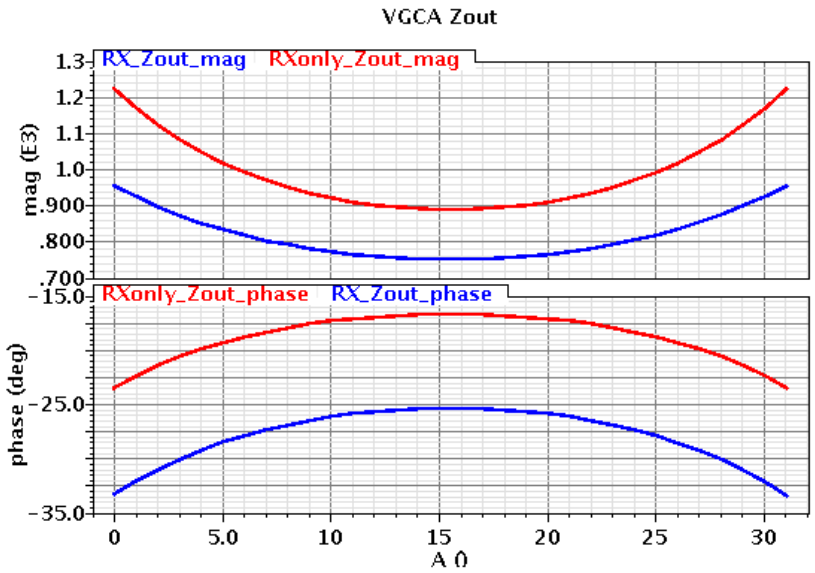

Figure 58: VGCA output impedance – default terminations – schematic simulation result – bi-directional (Blue) vs. stand-alone (Red)

The smaller output impedance of the bi-directional VGCA compared to the stand-alone VGCA's output impedance is almost entirely due to the addition of the $10k\Omega$ resistors to ground at the output of the VGCA. These resistors are used to bias the gate terminals of the VGTA PMOS devices during transmit mode of operation.

3.3.4 Current Gain

Current gain simulation result for typical terminations at $200MHz$ is shown below. The results for bi-directional and stand-alone VGCA are identical.

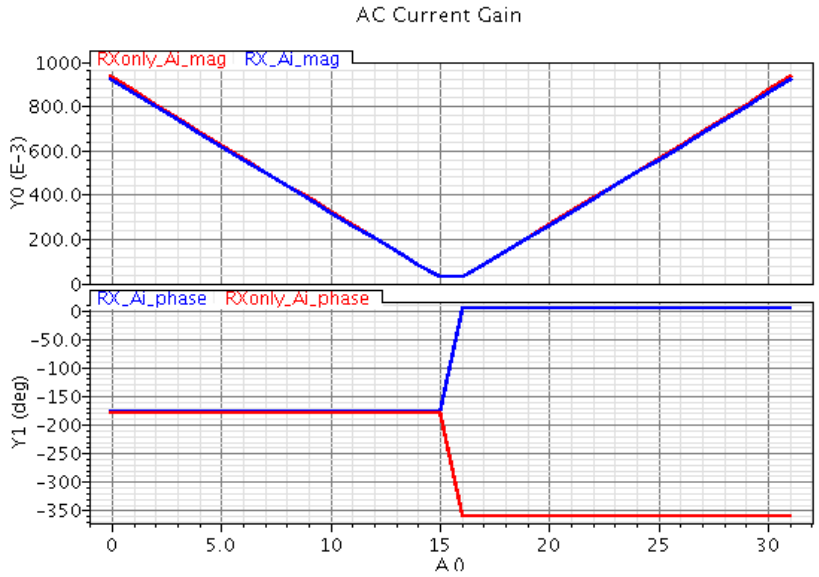

Figure 59: VGCA current gain – default terminations – schematic simulation result – bi-directional (Blue) vs. stand-alone (Red)

3.3.5 Linearity

The $1-dB$ compression point, defined as input signal available power at which the amplifier's transducer gain drops by $1-dB$ is next obtained through simulation. The VGCA is terminated with a 50Ω load, and driven by a 50Ω power source. The x-axis on Figure 60 indicates the available power from the 50Ω source, and the y-axis indicates the delivered power to the 50Ω load.

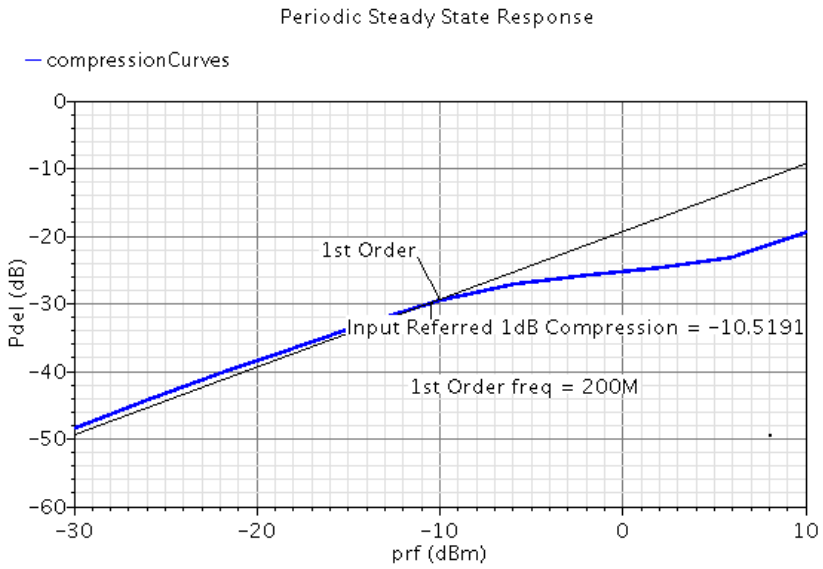

Figure 60: VGCA $1dB$ compression point – 50Ω differential terminations – schematic simulation result

The black trace corresponds to the first order, linear interpolation of the VGCA delivered power, offset by negative one decibel, while the blue trace is the power delivered to the load. The $1-dB$ compression point is the intersection of the two traces. As indicated on the plot, the $1-dB$ compression point occurs at approximately-$10.5dBm$.

3.3.6 NF

To understand the signal degradation caused by the VGCA on the over-all receive path, the NF of the VGCA is measured in simulation for all gain states. At $200MHz$, and with 50Ω source and load terminations, the NF is simulated and plotted in Figure 61. The results are nearly identical to the stand-alone VGCA NF (refer to Figure 34 on page 45).

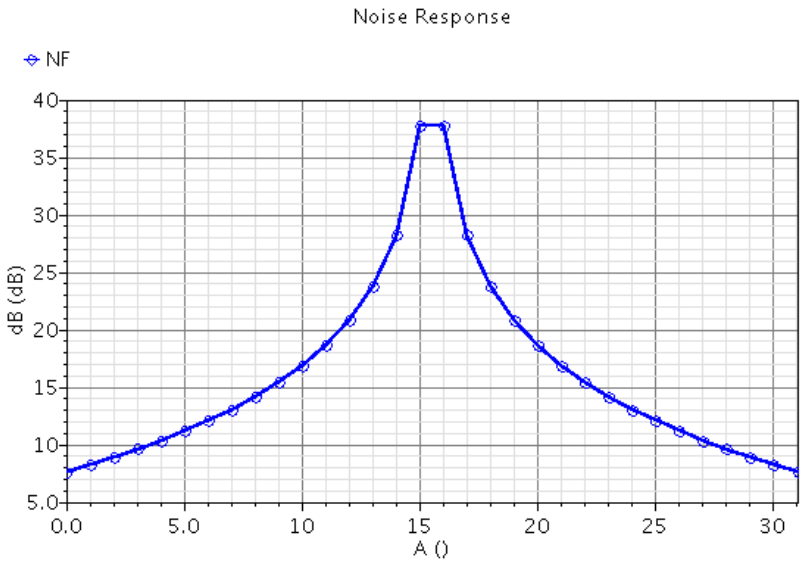

Figure 61: VGCA NF at $200MHz$ – 50Ω differential terminations – schematic simulation result

At maximum gain setting, the NF swept over frequency is depicted below:

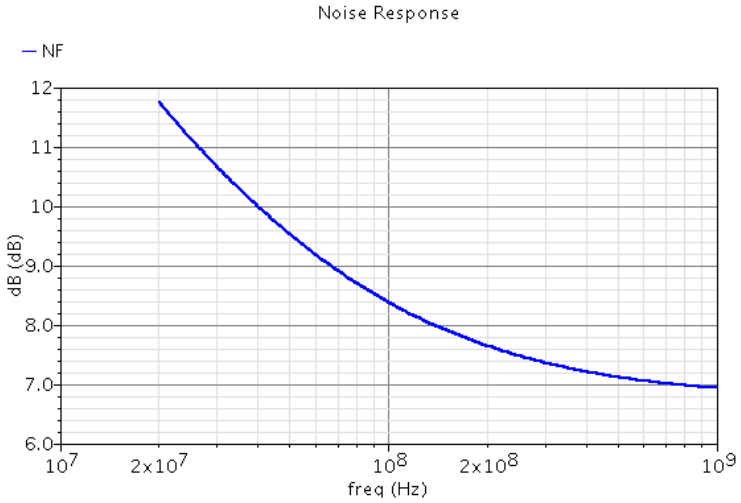

Figure 62: VGCA NF vs. Frequency – 50Ω differential terminations – schematic simulation result

The decrease in NF with increasing frequency can be explained as follows. At low frequencies, noise currents of VGCA NMOS current source devices contribute to the

input referred noise voltage. As the frequency increases, the gate-source capacitance of the amplifying NMOS devices lowers the input impedance, reducing the input referred noise voltage and the NF. [11][12]

3.4 Bi-directional VGA: VGTA

On transmit mode, the VGCA is OFF. This is done by reducing the gate voltages of the NMOS transistors to zero, thus forcing the transistors into the cutoff region. The NMOS current sinks during transmit are biased by the diode connected transistor in the VGTA's CMFB block and so need to be disconnected from the diode connected transistor biasing the VGCA. The CMFB block of the VGCA circuit is disabled by disconnecting the CMFB current sinking transistors from the VGTA current sinking transistors and tying the gate voltages of the CMFB amplifying transistors together to form a common mode amplifier with diode connected loads. To reduce the bias current of this differential circuit to preserve power consumption a switch is used to pull down the gate voltage of one of the two current sinking transistors to ground. By choosing the proper value of the width of the ON current sinking transistor, the bias currents in the two large resistors at the input of the VGTA are controlled to attain desirable bias voltage. The schematic of the VGA during transmit mode of operation with switches at appropriate positions (as depicted in Figure 55 on page 70) is shown below:

---

[12] Due to roll off in frequency response magnitude of the VGCA at higher frequencies, NF will reach a minimum and starts to increase with further increase in frequency

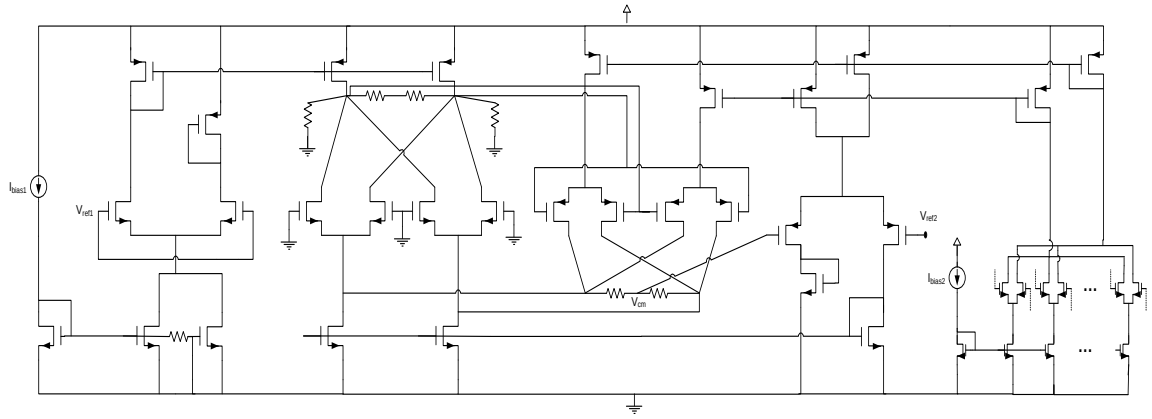

Figure 63: Bi-directional VGA configured as VGTA[13]

To operate as the bi-directional VGTA, the Bi-Directional VGA V_{ctrl} signal is set to high, enabling transmit mode of operation, and a sweep of simulations are performed.

3.5 Bi-Directional VGA: VGTA Schematic Simulation Results

3.5.1 DC

The common mode voltages of the bi-directional VGTA for all gain settings at input and output are shown below. The results are identical to the stand-alone VGTA common mode voltages.

---

[13] Dashed lines at the gates of 5 NMOS devices (3 shown) of the VGTA's binary-weighted current steering DAC indicate biasing network that is omitted in this figure.

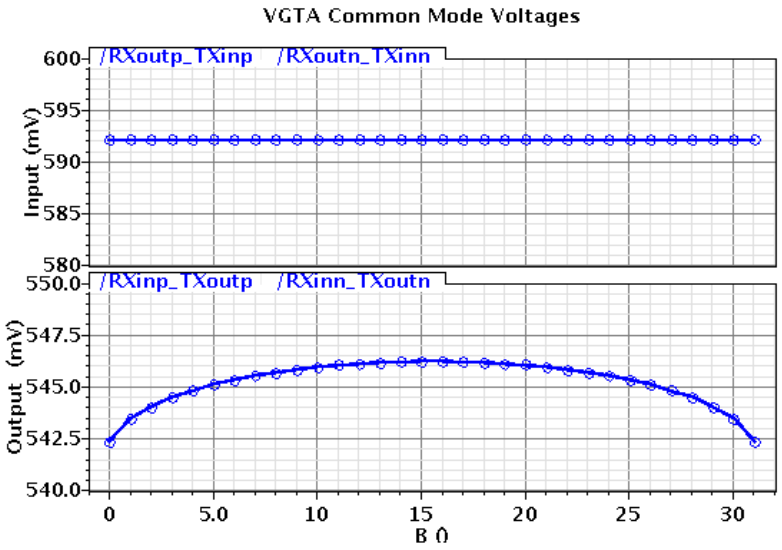

Figure 64[14]: VGTA common mode voltages – default terminations – schematic simulation result

3.5.2 Input Impedance

It is noted that the Bi-Directional VGTA input impedance is significantly lower than that of the stand-alone VGTA. This is explained here: differential input CS stage of the VGTA is parallel with a $10K\Omega$ resistor in parallel with the output resistance of the VGCA PMOS current sinking transistors and in parallel with turned off VGCA NMOS transistors. The PMOS current source device of the VGCA (OFF), is slightly turned on to provide the bias current necessary to bias the input pairs PMOS devices of the VGTA, and it's operating in the weak inversion. This device, therefore, provides a finite output resistance. In addition to this, the large VGCA NMOS devices, although in cutoff region

[14] RXoutp/n_TXinp/n correspond to positive/negative VGTA input terminals and RXinp/n_TXoutp/n correspond to positive/negative VGTA output terminals

of operation, introduce some capacitance from drain to ground, dominated by the drain poly to diffusion overlap capacitance and drain junction to body capacitance. This combination of resistive and capacitive loading, introduced by the connection to the VGCA, drops the input impedance significantly at higher frequencies.

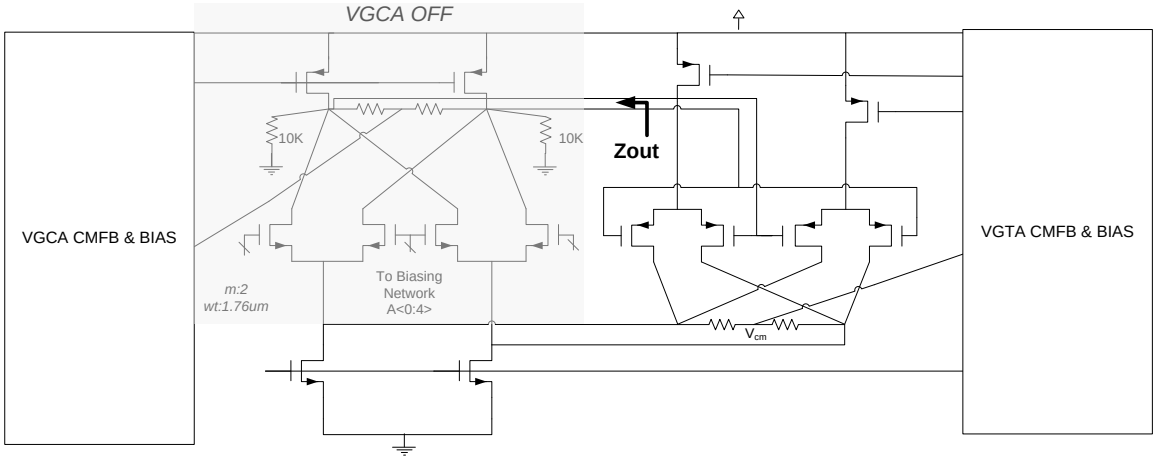

Figure 65: VGTA input impedance – contribution from VGCA – schematic simulation result

Plot below shows the output impedance seen looking into the VGCA network (in OFF mode) from input of the VGTA, as depicted in figure above:

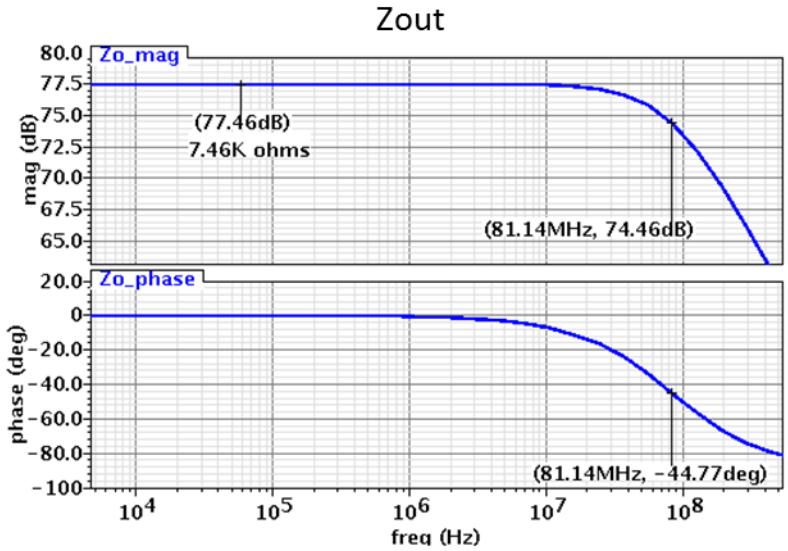

Figure 66: VGTA input impedance – contribution from VGCA– schematic simulation result

The stand-alone VGTA input impedance, obtained from the stand-alone VGTA simulation results of Chapter 2 (Figure 45 on page 59), is:

$$Z_{in,txonly}\big|_{f=200MHz} = -j3.5K\Omega \quad \text{(Eq. 3.3)}$$

$$C_{in,txonly} = \frac{1}{3.5K\Omega \times 2\pi(200MHz)} = 227fF \quad \text{(Eq. 3.4)}$$

The output impedance, looking into the VGCA from VGTA input, from the above figure is:

$$Z_{out} = \frac{R_{out}}{1 + j\omega R_{out}\left(C_{in,txonly} + C_{out}\right)} \quad \text{(Eq. 3.5)}$$

$$\left|Z_{in,tx}\right|_{f=200MHz} = \left|\frac{R_{out}}{1 + j\omega R_{out}\left(C_{in,txonly} + C_{out}\right)}\right| = 1.6K\Omega \quad \text{(Eq. 3.6)}$$

$$\measuredangle Z_{in,tx}\big|_{f=200MHz} = \measuredangle \frac{R_{out}}{1 + j\omega R_{out}\left(C_{in,txonly} + C_{out}\right)} = -77^{o} \quad \text{(Eq. 3.7)}$$

Where

$$R_{out} = 7.46K\Omega, \omega_{3-dB} = 2\pi(81.14\text{MHz}), C_{out} = \frac{1}{\omega_{3-dB} R_{out}} = 260fF$$

Besides a few degrees of discrepancy in the phase of the input impedance from calculated above and simulated, the input impedance drop in the bi-directional VGTA is as expected.

3.5.3 Output Impedance

VGTA output impedance at $200MHz$ is depicted below. It is noted that the output impedance of the stand-alone VGTA is quite higher than that of the VGA.

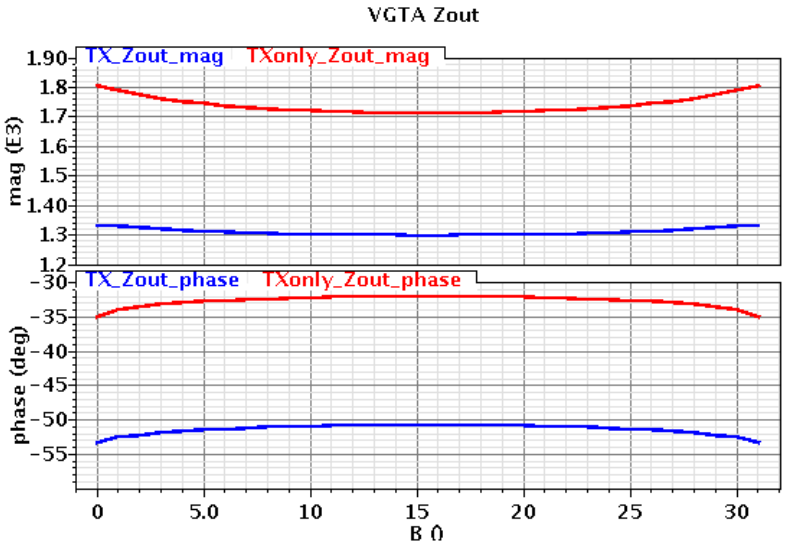

Figure 67: VGTA output impedance – default terminations – schematic simulation result – bi-directional (Blue) vs. stand-alone (Red)

The difference between the two impedances is due to the presence of VGCA NMOS transistors at the output of the VGA during transmit mode of operation. Gate to source capacitance (diffusion to poly overlap), and source to body junction capacitances

of these large devices, in the order of a few hundred femto Farads will have a significant effect on the output impedance at $200MHz$, as observed on the plots. Figure below is the measured impedance looking out from the output of the VGTA into the VGCA (OFF) input:

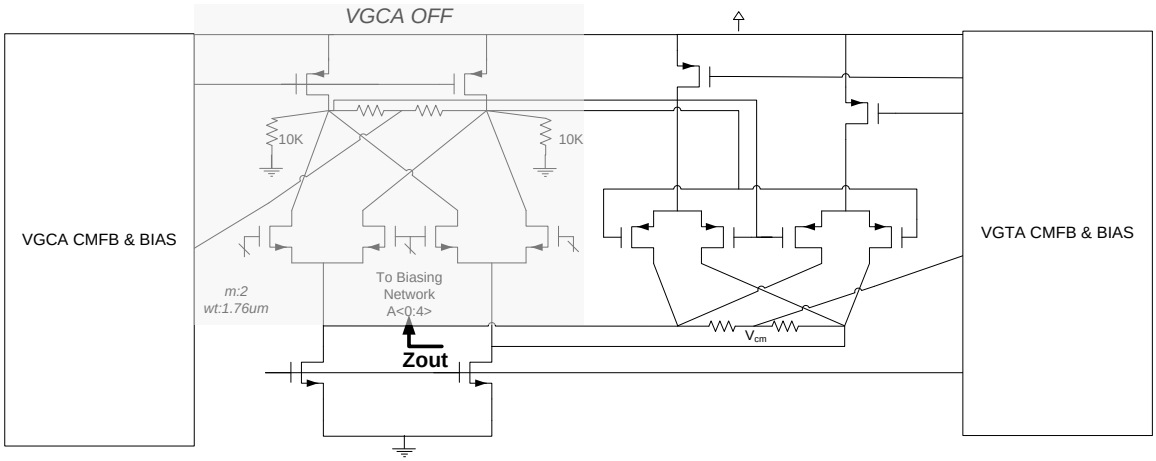

Figure 68: VGTA output impedance – contribution from VGCA

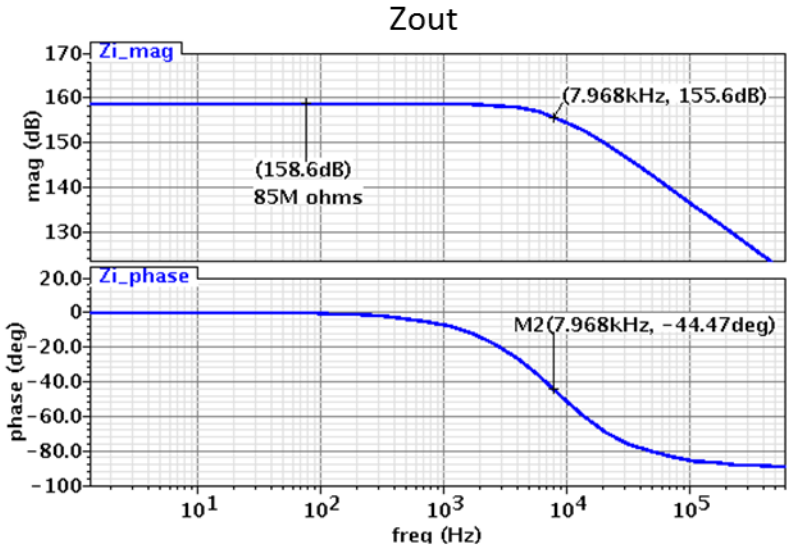

Figure 69: VGTA output impedance - Contribution from VGCA– schematic simulation result

From figure above:

$$R_{out} = 85M\Omega, \omega_{3-dB} = 2\pi(7.97\text{KHz}), C_{out} = \frac{1}{\omega_{3-dB}R_{out}} = 230fF \quad \text{(Eq. 3.8)}$$

The equivalent output capacitance and resistance of the stand-alone VGTA for maximum gain setting was previously calculated in Chapter 2 ((Eq. 2.103), page 63) and the results are repeated here:

$$R_{out,txonly} = 2.2K\Omega, C_{out,txonly} \approx 250\text{fF}$$

The combined output impedance, or equivalently the bi-directional VGTA's output impedance, is then calculated for the maximum gain setting:

$$Z_{out} = \frac{R_{out,txonly}}{1 + j\omega R_{out,txonly}\left(C_{out,txonly} + C_{out}\right)} \quad \text{(Eq. 3.9)}$$

$$\left|Z_{out,tx}\right|_{f=200MHz} = \left|\frac{R_{out,txonly}}{1 + j\omega R_{out,txonly}\left(C_{out,txonly} + C_{out}\right)}\right| = 1.3K\Omega \quad \text{(Eq. 3.10)}$$

$$\measuredangle Z_{out,tx}\Big|_{f=200MHz} = \measuredangle \frac{R_{o,txonly}}{1 + j\omega R_{o,txonly}\left(C_{out,txonly} + C_{o}\right)} = -53^{o} \quad \text{(Eq. 3.11)}$$

The calculated output impedance confirms the drop in output impedance of the bi-directional VGTA due to the capacitive loading of the VGCA NMOS devices.

3.5.4 Transadmittance

The Transadmittance of the VGTA is plotted below. The results are identical to the stand-alone VGTA Transadmittance.

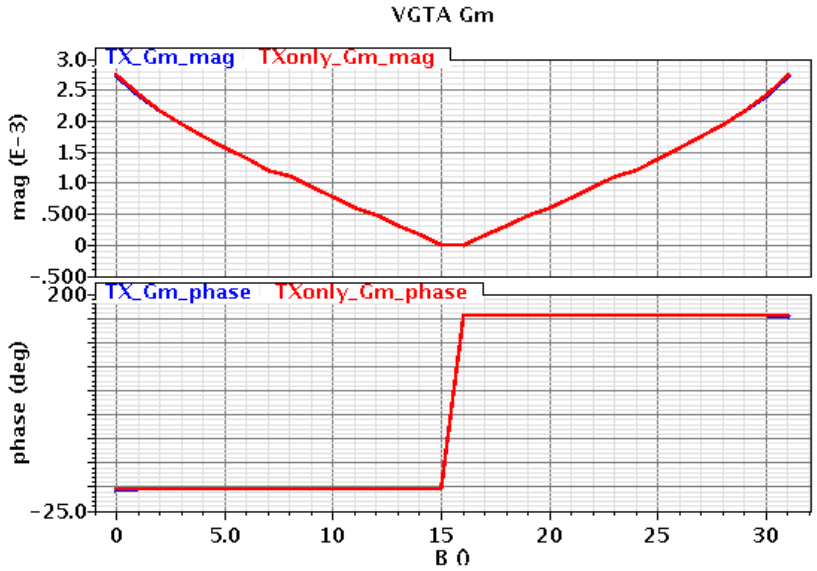

Figure 70: VGTA transadmittance – default terminations – schematic simulation result – bi-directional (Blue) vs. stand-alone (Red)

3.5.5 Linearity

Figure below is the plot of $1dB$ compression point of the VGTA at $200MHz$ at 160Ω load termination:

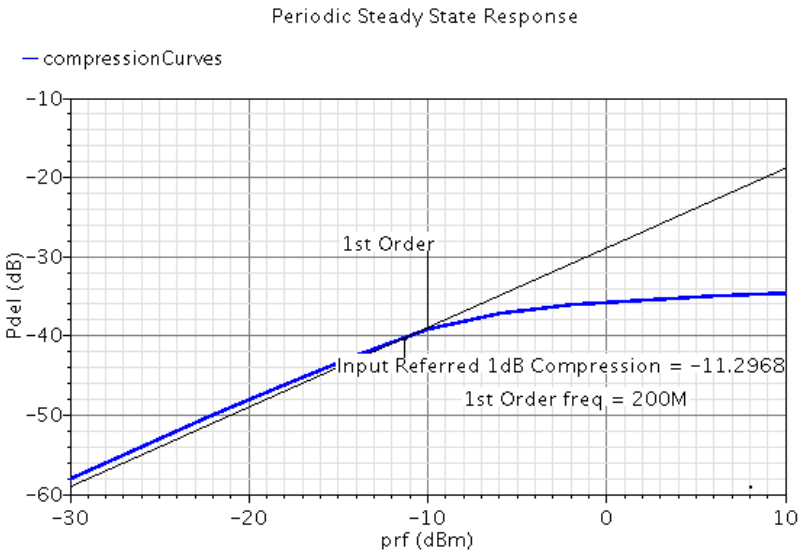

Figure 71: VGTA $1dB$ compression point – 50Ω differential terminations – schematic simulation result

3.5.6 NF

Plot below is the simulation results depicting NF at $200MHz$ for various gain states at 50Ω load termination. The results are nearly identical to the NF simulated for the stand-alone VGTA (refer to Figure 53 on page 68).

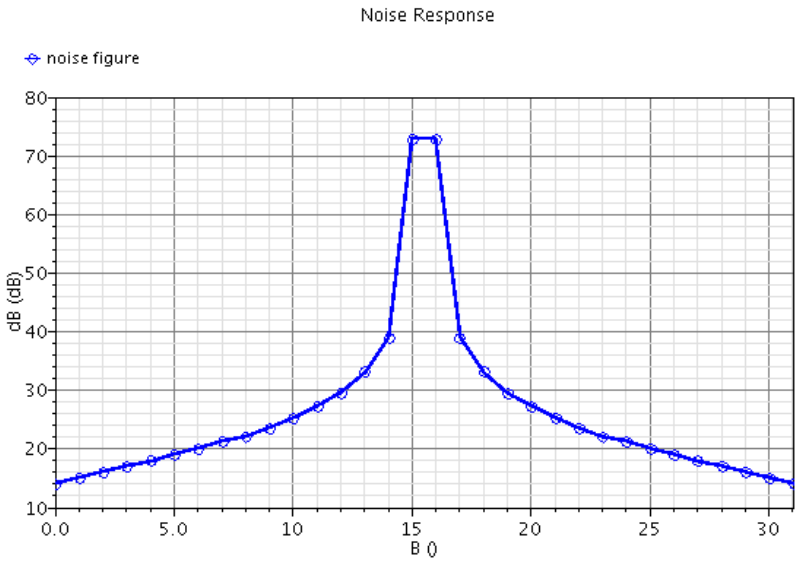

Figure 72: VGTA NF simulation results at $200MHz$ – 50Ω differential terminations – schematic simulation result

At maximum gain setting, the NF swept over frequency is depicted below:

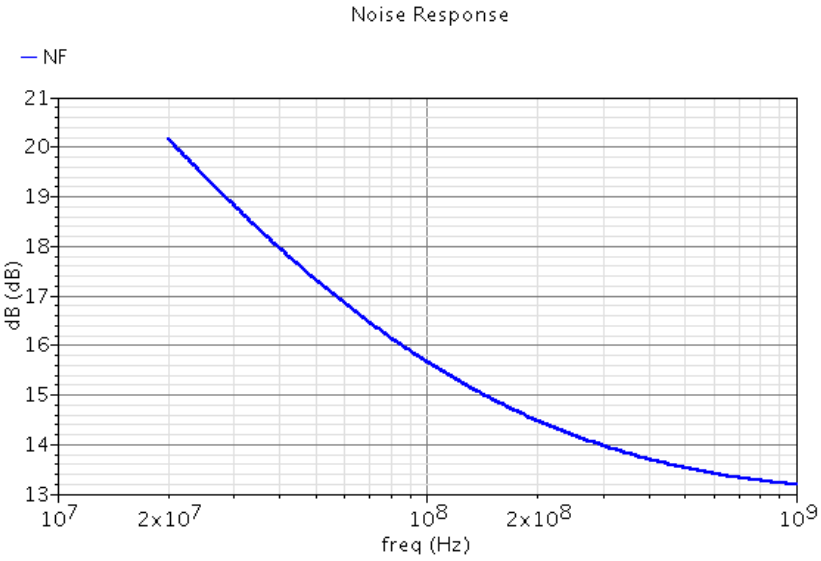

Figure 73: VGTA NF vs. frequency – 50Ω differential terminations – schematic simulation result

CHAPTER 4

BI-DIRECTIONAL VVGA

The VVGA, as shown in Figure 74 below, is constructed using the bi-directional VGAs as its building blocks. Each block represents the bi-directional configuration of Figure 7 on page 8. At receive mode of operation, the blocks represent the VGCA, and on transmit mode they represent the VGTA. The VVGA, thus, acts as a VVGTA during the transmit mode of operation, and as a VVGCA during receive mode of operation. Figure below shows this topology.

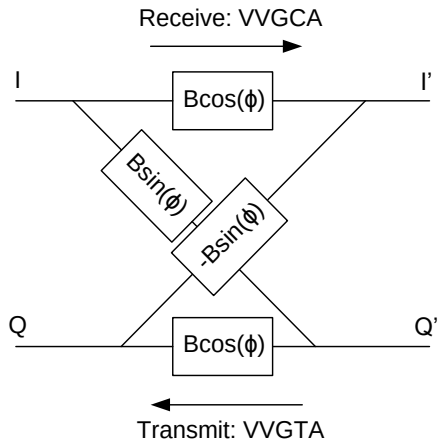

Figure 74: VVGA block diagram: VVGCA (receive) and VVGTA (transmit)

Here, $B\cos\phi$, $B\sin\phi$ and $-B\sin\phi$ values represent the gain of each block during receive or transmit. This configuration, as stated earlier, enables amplification (B) and phase shift (ϕ) of an IQ signal pair in both directions, receive and transmit.

4.1 VGA Configuration at Receive and Transmit Modes

As discussed previously, the output common mode voltage of the individual VGAs is controlled using a CMFB network at the output node. As illustrated earlier, each VGA contains two CMFB blocks, one in direction of receive, VGCA, and one in transmit, VGTA. Because the VVGCA and VVGTA configurations require connecting two output nodes together, it is necessary to ensure only one CMFB circuit is controlling each output common mode voltage at any time to avoid contention at the output and to achieve proper stabilization of the common mode voltage. Because the CMFB circuit, in addition to providing a stable common mode output voltage, also biases the VGCA and VGTA, it is not possible to remove any of the CMFB blocks from the individual VGAs in the VVGA, but it is ensured that only one CMFB loop is active during each mode of operation.[15]

Figure 75 below depicts the VVGA configured as the VVGCA during receive mode of operation and as VVGTA during transmit mode of operation.

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[15] The CMFB setup in the fabricated VVGA design suffers from this design flaw. The details of this issue is discussed in Appendix A. The fix to this problem that has been implemented in the modified design is also present in the same section.

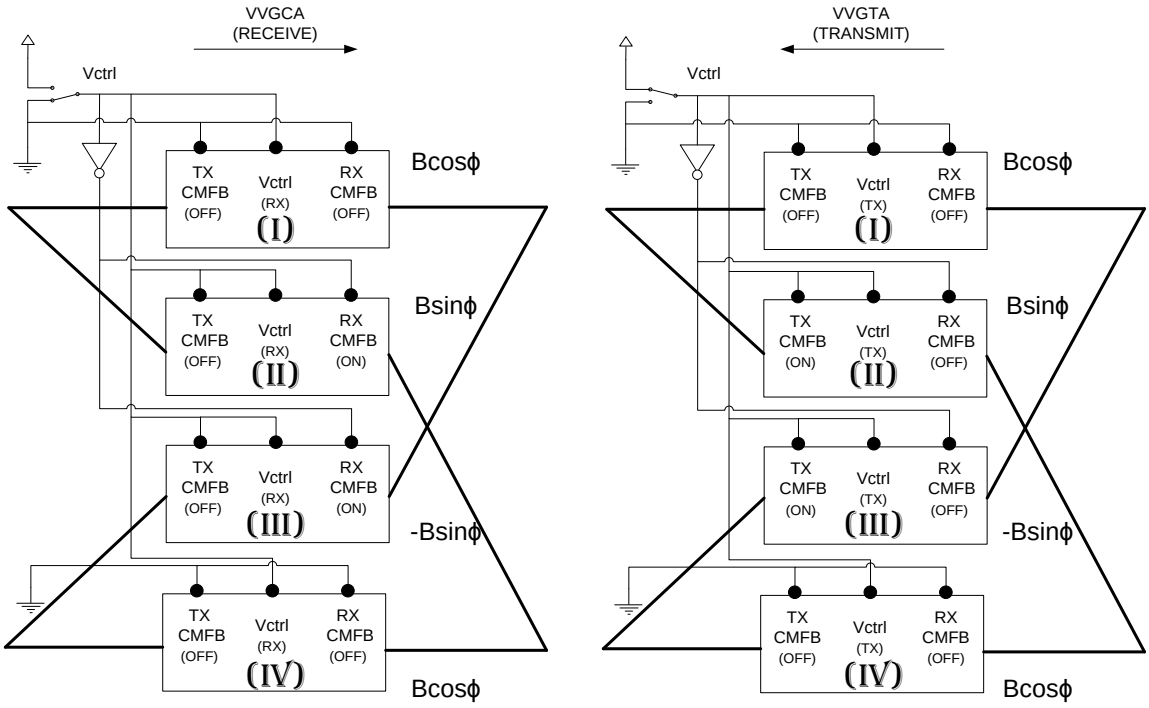

Figure 75: VVGA control signal positions in VVGCA and VVGTA configurations

In Figure 75, each individual block is a VGA, and the V_{ctrl} switch is used to place the bi-directional VGAs in either the receive or transmit modes of operation. To ensure that only one output CMFB loop is active during each VVGA mode of operation, two additional control input signals, "RX CMFB" and "TX CMFB", are introduced. A high (low) "RX CMFB" signal activates (disables) the CMFB loop of the VGA in receive mode, and similarly, a high (low) "TX CMFB" signal activates (disables) the CMFB loop of the VGA in transmit mode. To ensure proper functionality of the VVGA, it is necessary to ensure that the VGA remains properly biased in absence of the CMFB loop, as the CMFB circuit is used to bias the VGA blocks in receive and transmit modes.

VGA blocks, labeled *I* and *IV* on VVGA blocks shown on Figure 75, have their "RX CMFB" and "TX CMFB" switches tied to ground, therefore disabling the CMFB loops at

both receive and transmit modes for these VGA blocks. To ensure output common mode stability at receive and transmit, then, at receive it is necessary to enable the RX CMFB loops of VGA blocks labeled II and III while disabling TX CMFB loops for all VGAs. Similarly, at transmit it is necessary to enable the TX CMFB loops of VGA blocks labeled II and III while disabling the RX CMFB loops of all VGA blocks. This is achieved by connecting the "TX CMFB" switches of VGA blocks II and III directly to V_{ctrl} , and connecting their "RX CMFB" switches to the inverted V_{ctrl}. At receive (VVGCA on Figure 75), then, V_{ctrl} is set to low, which disables VGA II and III TX CMFB loops and enables their RX CMFB loops. At transmit (VVGTA on Figure 75), V_{ctrl} is set to high, thus enabling the TX CMFB loops of VGA blocks II and III and disabling their RX CMFB loops. .

The figure below is the detailed schematic of the VGA that depicts the placement and positions of CMFB switches during receive and transmit modes of operation:

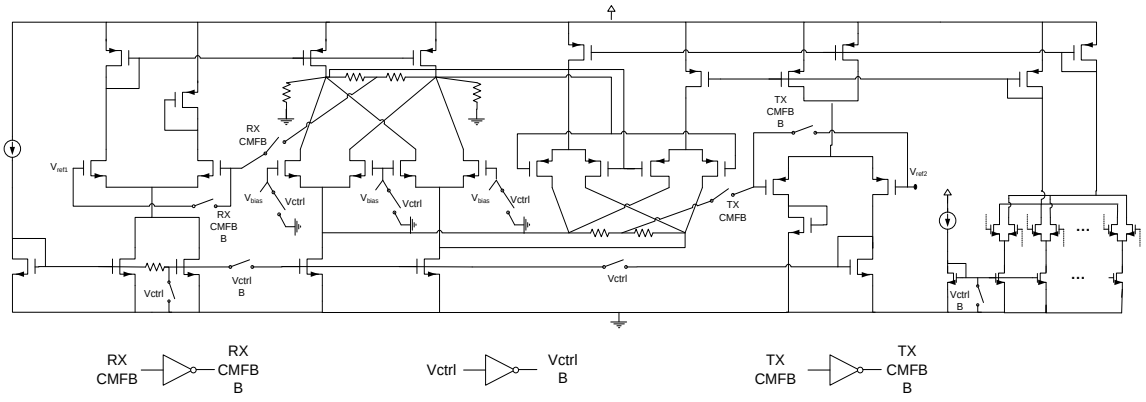

Figure 76: Bi-directional VGA – control switch implementation

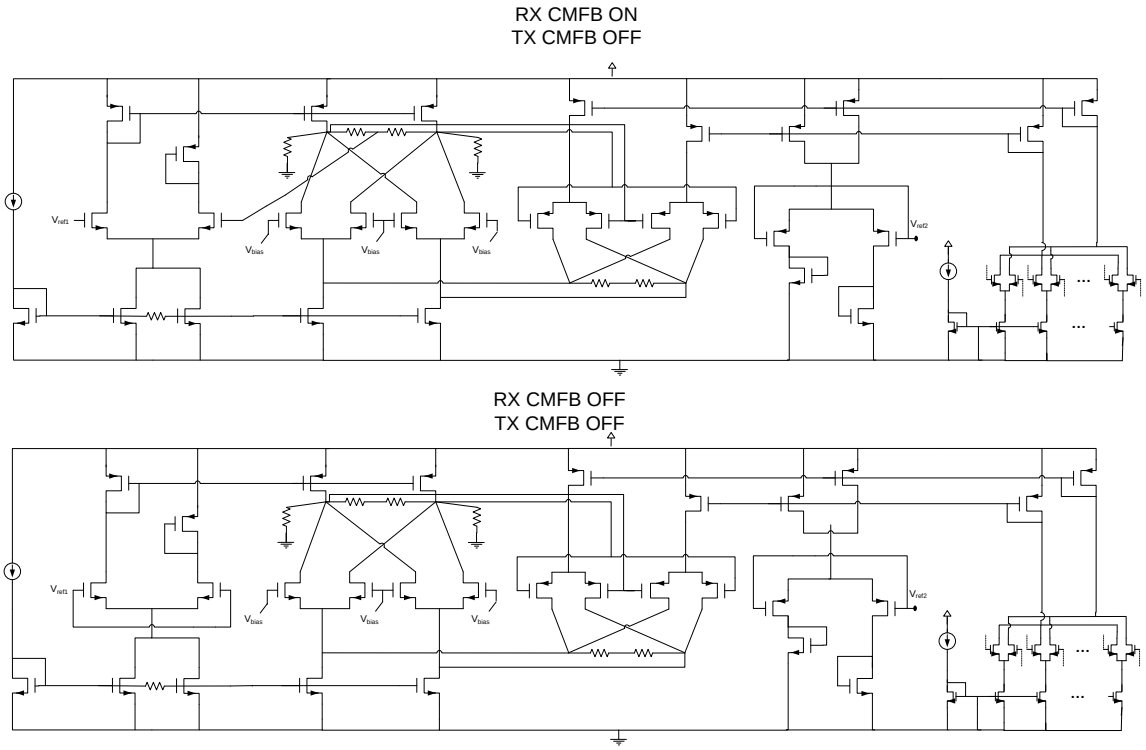

Figure 77: Bi-directional VGA – control switch positions for VGCA configuration (receive mode)

The V_{ctrl} switch is in high position during transmit mode of operation, turning off all RX CMFB switches and leaving on only two TX CMFB circuits, each controlling the common mode voltage at one output node. The two VGTA configurations are shown in Figure 78 below:

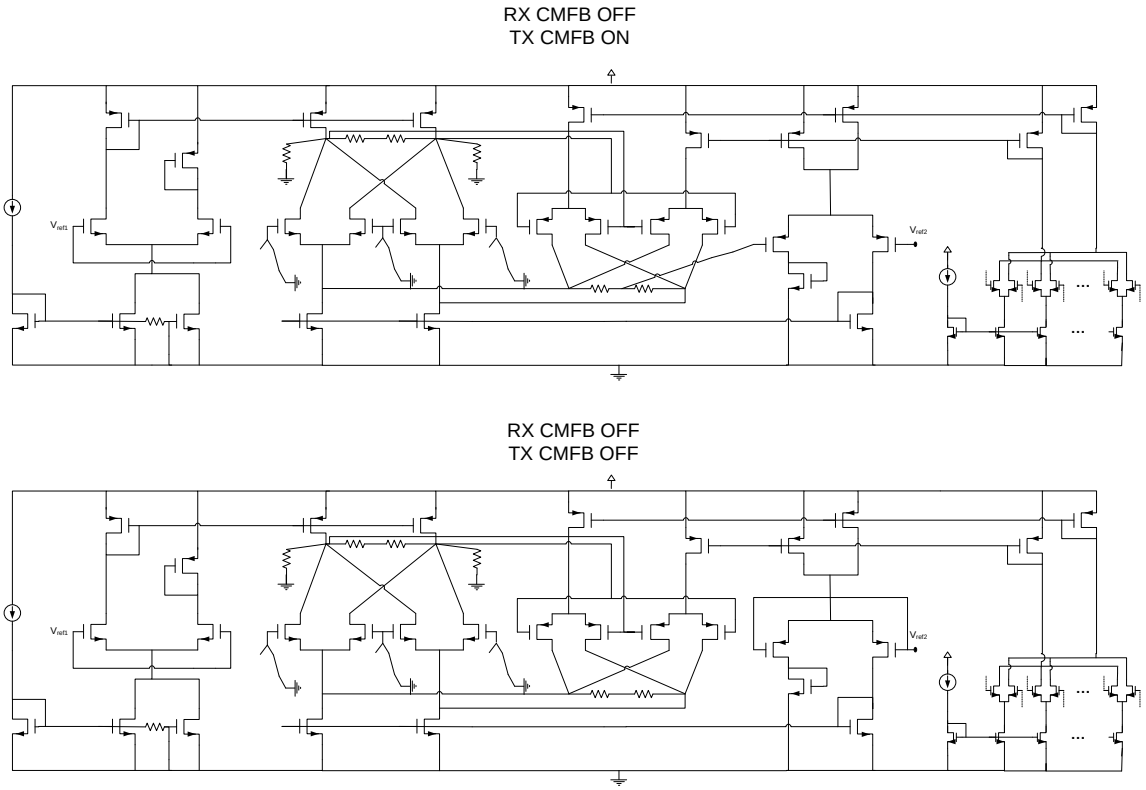

Figure 78: Bi-directional VGA – control switch positions for VGTA configuration (transmit mode)

The aforementioned VGA and VVGA architecture is a modified version of the design that was fabricated on chip, and will be presented in the next two chapters. In the fabricated VVGA architecture, all eight CMFB loops remain active during both receive and transmit modes of operation. In addition to this architecture error, the CMFB architecture, as fabricated, does not provide proper loop stabilization at VGA level. This will also be illustrated in the following chapters. For a quick comparison, the simplified schematic of the VGA, as fabricated, is presented here.

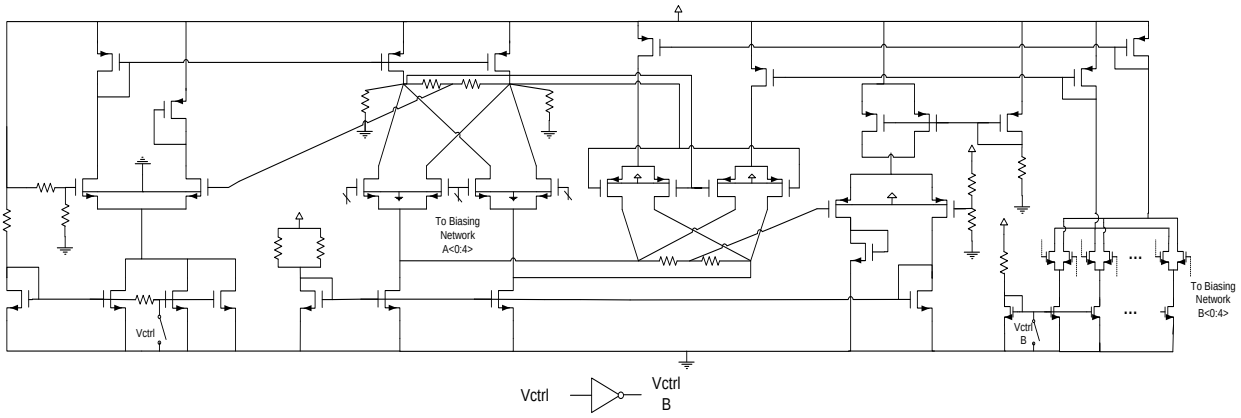

Figure 79: Bi-directional VGA control switch implementation as fabricated

As seen on the above figure, the only two switches present in the fabricated version of the VGA are to decrease (VGCA mode) or eliminate (VGTA mode) the bias current of the off portion of the circuit in each mode of operation, and no mechanism is present to eliminate contention between CMFB loops when the VGAs are connected to form the VVGA.

4.2 VVGCA

The gain of each individual VGA, as discussed earlier, is determined by a five bit control word, thus creating 2^5 possible gain states for each VGA. On each mode of operation, the gain of VGA blocks $B\ cos\ \phi$ are controlled by control word B and that of VGA blocks $B\ sin\ \phi$ and $-B\ sin\ \phi$ are controlled by control word A. This implies that there are 2^{10} possible gain states for the VVGA on both receive and transmit modes of operation.

To find the VVGA's transfer characteristics for all 2^{10} complex gain states, the individual VGA gains are represented as polar values depicted in Figure 80 below. This

eliminates the dependency between gain states associated with gain values $B\ cos\ \phi$ and $B \sin \phi$ of Figure 74 on page 88. An IQ signal pair, $Ae^{j\theta}$ and $Ae^{(j(\theta-\pi/2))}$, (phasor notations) is applied as input at both receive and transmit modes and the output is evaluated:

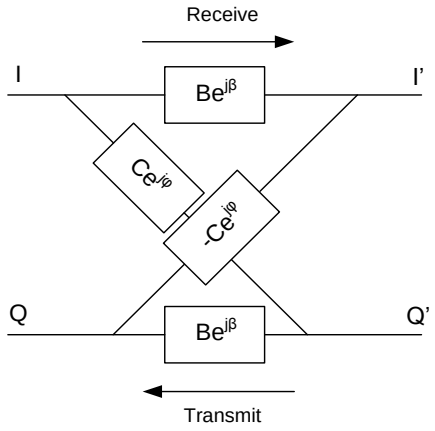

Figure 80: VVGA block diagram

At receive, the input and output relationships are:

$$I' = ABe^{j(\theta+\beta)} - ACe^{j\left(\theta+\varphi-\frac{\pi}{2}\right)} \quad \text{(Eq. 4.1)}$$

$$Q' = ACe^{j(\theta+\varphi)} + ABe^{j\left(\theta+\beta-\frac{\pi}{2}\right)} \quad \text{(Eq. 4.2)}$$

$$\left|I'\right| = A\sqrt{\left(Bcos(\theta+\beta) - Csin(\theta+\varphi)\right)^2 + \left(Bsin(\theta+\beta) + Ccos(\theta+\varphi)\right)^2} \quad \text{(Eq. 4.3)}$$

$$\measuredangle I' = \text{atan2}\left[Bsin(\theta+\beta) + Ccos(\theta+\varphi), Bcos(\theta+\beta) - Csin(\theta+\varphi)\right] \quad \text{(Eq. 4.4)}$$

$$\left|Q'\right| = A\sqrt{\left(Ccos(\theta+\varphi) + Bsin(\theta+\beta)\right)^2 + \left(Csin(\theta+\varphi) - Bcos(\theta+\beta)\right)^2} \quad \text{(Eq. 4.5)}$$

$$\measuredangle Q' = \text{atan2}\left[Csin(\theta+\varphi) - Bcos(\theta+\beta), Ccos(\theta+\varphi) + Bsin(\theta+\beta)\right] \quad \text{(Eq. 4.6)}$$

From above equations it is evident that for any combination of B, C, β and φ, the signals at the output are in quadrature and equal in magnitude for IQ input signals of equal magnitude.

4.2.1 Complex Current Gain

Combining Figure 19: *VGCA h-parameter equivalent circuit* on page 26 with Figure 80 above results in the circuit diagram depicted below.

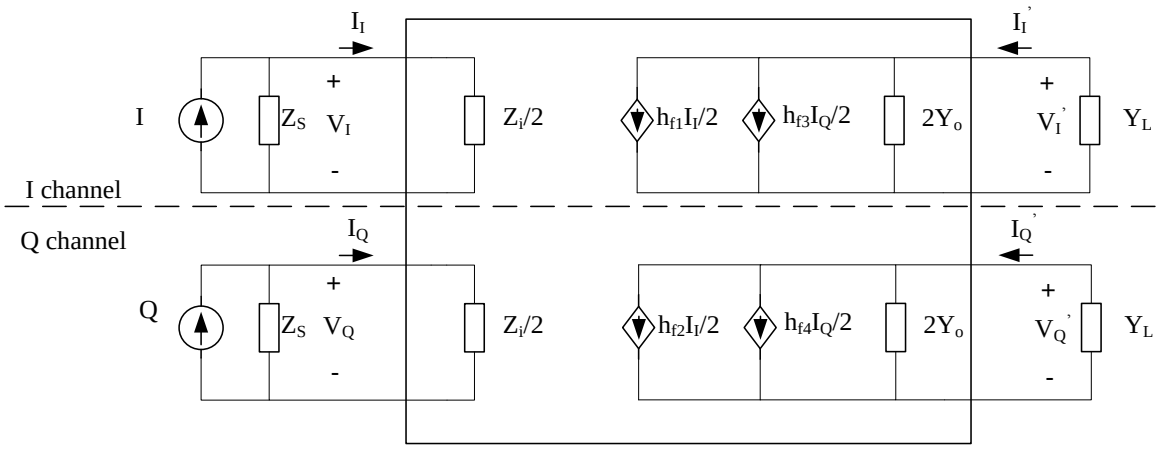

Figure 81: VVGCA h-parameter equivalent circuit

h_{f1} thru h_{f4} correspond to individual VGCA's short circuit forward transfer current ratios and were evaluated earlier as a function of the VGCA's five bit control word in (Eq. 2.31) on page 27. Replacing control word A with control word B yields:

$$h_{f1} = -\frac{\sum_{i=0}^{4} 2^i \left(b_{\mathrm{i}} - \overline{b_{\mathrm{i}}}\right)}{2^5 - 1} \qquad \text{(Eq. 4.7)}$$

Where $\lim_{Y_o \to 0} [Y_L/(Y_o + Y_L)] = 1$.

h_{f2} thru h_{f4} are defined similarly as a function of corresponding control word for each VGCA. The complex current gain of the VVGCA, $(I_I' + jI_Q')/(I_I + jI_Q)$ can be defined in terms of the previously calculated parameter h_f. Referring to Figure 81 above, complex output current is evaluated as:

$$I_I' + jI_Q' = \frac{Y_L}{2(Y_L + 2Y_o)}\left[\left(h_{f1}I_I + h_{f3}I_Q\right) + j\left(h_{f2}I_I + h_{f4}I_Q\right)\right] \quad \text{(Eq. 4.8)}$$

Because $h_{f1} = h_{f4}$, and $h_{f2} = -h_{f3}$, the complex current gain of the VVGCA becomes:

$$\frac{I_I' + jI_Q'}{I_I + jI_Q} = \frac{Y_L}{2(Y_L + 2Y_o)}\left(h_{f1} - jh_{f3}\right) = \frac{Y_L}{2(Y_L + 2Y_o)}\left(h_{f4} + jh_{f2}\right) \quad \text{(Eq. 4.9)}$$

$$\left|\frac{I_I' + jI_Q'}{I_I + jI_Q}\right| = \frac{\mathrm{Y_L}}{2(Y_L + 2Y_o)}\sqrt{{h_{f1}}^2 + {h_{f3}}^2} = \frac{\mathrm{Y_L}}{2(Y_L + 2Y_o)}\sqrt{{h_{f4}}^2 + {h_{f2}}^2} \quad \text{(Eq. 4.10)}$$

$$\measuredangle\frac{I_I' + jI_Q'}{I_I + jI_Q} = atan2\left(-h_{f3}, h_{f1}\right) = atan2\left(h_{f2}, h_{f4}\right) \quad \text{(Eq. 4.11)}$$

Where it's assumed:

$$\measuredangle\frac{\mathrm{Y_L}}{2(Y_L + 2Y_o)} \cong 0^{\mathrm{o}}$$

The values of the four h parameters are:

$$h_{f1} = -\frac{\sum_{i=0}^{4} 2^i\left(b_{\mathrm{i}} - \overline{b_{\mathrm{i}}}\right)}{2^5 - 1} \quad \text{(Eq. 4.12)}$$

$$h_{f4} = h_{f1} \quad \text{(Eq. 4.13)}$$

$$h_{f3} = -\frac{\sum_{i=0}^{4} 2^i(a_{\mathrm{i}} - \overline{a_{\mathrm{i}}})}{2^5 - 1} \quad \text{(Eq. 4.14)}$$

$$h_{f2} = -h_{f3} \quad \text{(Eq. 4.15)}$$

The short circuit, complex current gain of the VVGCA for all possible gain states can be obtained by plotting complex current gain magnitude versus the phase calculated above for all gain states. For ideal, zero output admittance, the short circuit complex current gain is obtained:

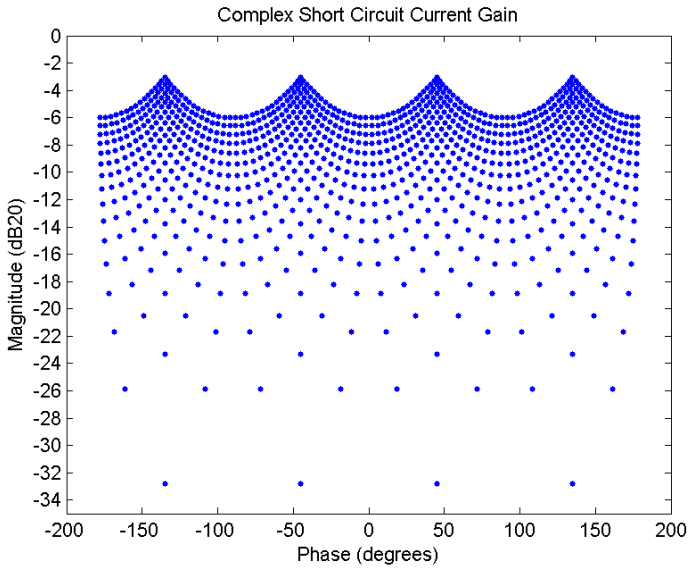

Figure 82: VVGCA complex current gain – ideal

The complex current gain obtained through schematic simulations with a 50Ω load termination is shown below.

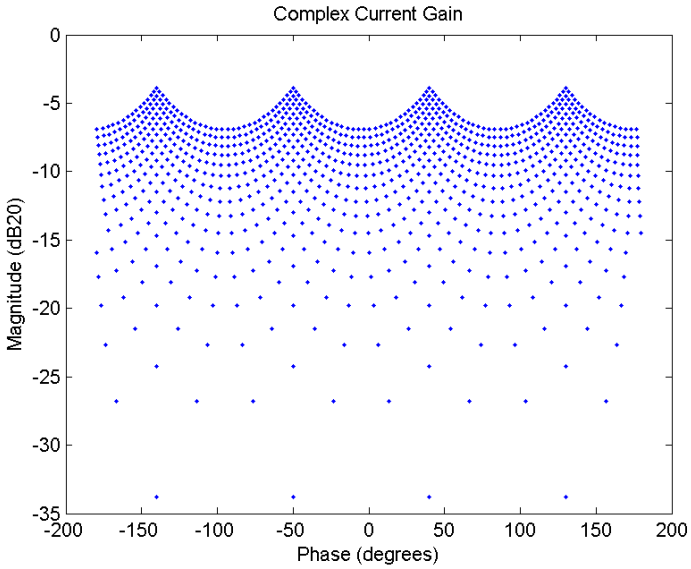

Figure 83: VVGCA complex current gain – default terminations – schematic simulation result

Finite output impedance of the VGCA and non-ideal VGCA current gain results in a complex current gain VVGCA plot that deviates slightly from the ideal, short circuit complex current gain depicted in the plot above. The figure below shows the effect of each non-ideality separately.

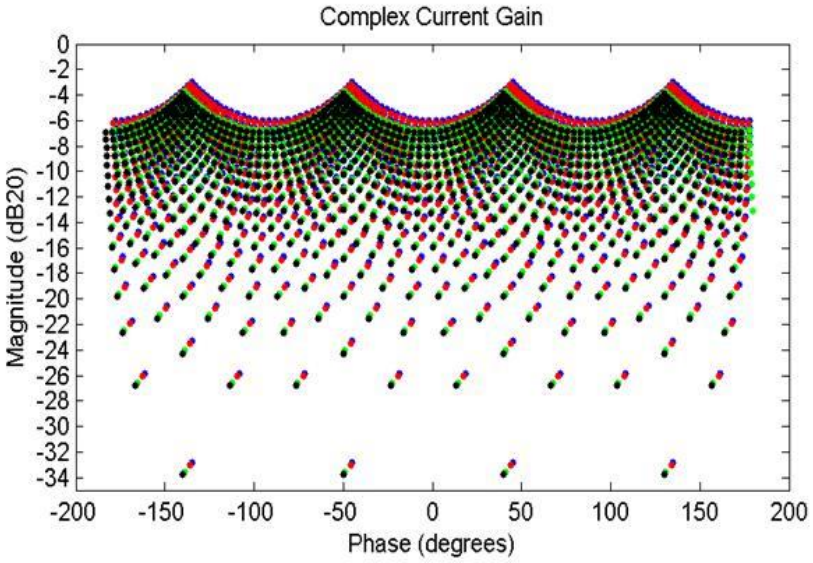

Figure 84: VVGCA complex current gain – Mathematical modeling of non-idealities vs. schematic simulation result: Blue: ideal model – Red: ideal model including effect of source and load terminations in presence of non-finite output impedance and non-zero input impedance – Green: effect of VGCA non-ideal current gain – Black: schematic simulation result

The blue dots correspond to the ideal, short circuit complex current gain shown in Figure 82 on page 98. Red data points depict the effect of adding the VGCA's output impedance and the load resistance to the complex current gain equation. Green data points are generated by replacing the ideal VGCA h parameters with that obtained through simulation. Finally, the black data points correspond to the complex current gain obtained through schematic simulation results.

It is noted that the deviation of the complex current gain from the ideal due to finite output impedance of the VGCAs is insignificant, implying that the VGCA's output impedance is high enough not to disturb the ideal behavior.

The small deviation of VGCA's current gain from the expected ideal, linear current gain creates a noticeable magnitude drop and phase shift. Figure below depicts this more clearly:

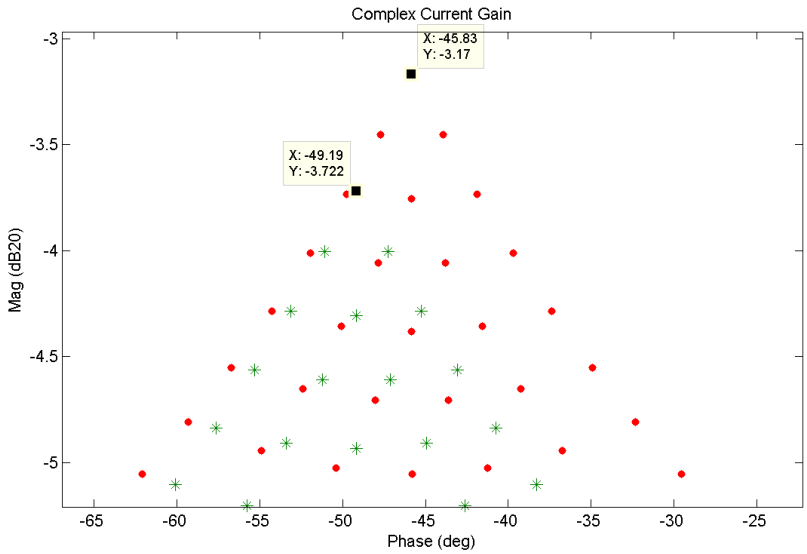

Figure 85: VVGCA complex current gain – Effect of non-ideal VGCA complex current gain

The figure below is the plot of VGCA short circuit current gain, repeated for convenience:

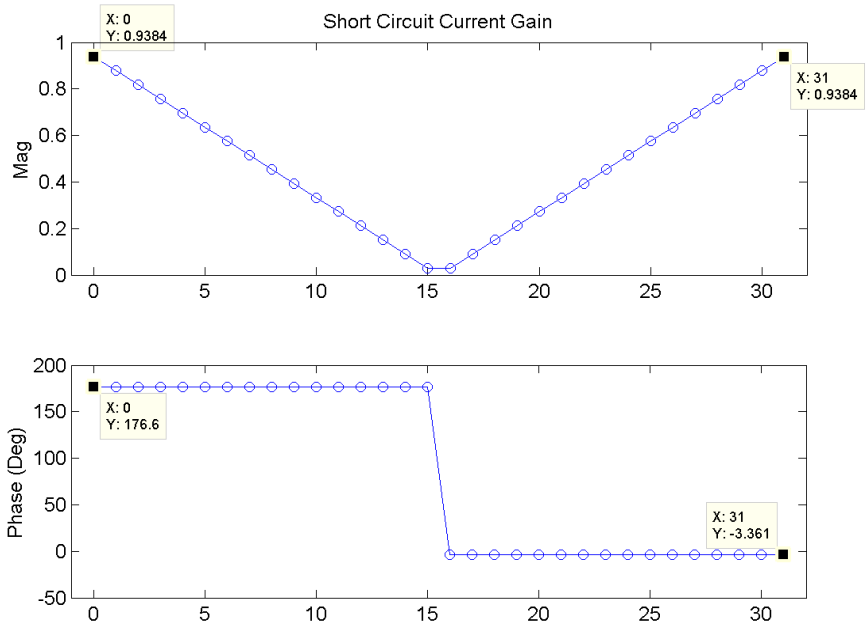

Figure 86: VGCA current gain – short output termination – schematic simulation result

The small drop in short circuit current gain of the VGCA, as observed, is to be expected. At higher frequencies ($200MHz$), any parasitic gate to source capacitance of the NMOS CG devices will provide a finite impedance path to ground. This current dividing effect created by gate to source capacitance of the NMOS and its output resistance, therefore, decreases the output short circuit current gain.

A 6% drop in magnitude of the VGCA maximum ideal current gain of one results in a 6% drop in the VVGCA maximum complex current gain magnitude from that of the ideal ($\approx 0.54\ dB20$ drop). A 3^o positive phase shift of the VGCA current gain from the ideal ($-177^o, +3^o$ as opposed to $-180^o, 0^o$) results in the complex current gain shifting 3^o to the left, as seen on Figure 85 above and confirmed below:

Repeating the complex current gain equation here for convenience:

$$\left|\frac{I_I{}' + jI_Q{}'}{I_I + jI_Q}\right| = \frac{1}{2}\sqrt{h_{f1}{}^2 + h_{f3}{}^2} \quad \text{(Eq. 4.16)}$$

$$\measuredangle \frac{I_I{}' + jI_Q{}'}{I_I + jI_Q} = \measuredangle\left(h_{f1} - jh_{f3}\right) \quad \text{(Eq. 4.17)}$$

For ideal VGCA, $h_{f1} = h_{f3} = 1$ for state 31. The VVGCA complex current gain at the maximum gain setting of $A = B = 31$ is:

$$\frac{1}{2}\sqrt{h_{f1}{}^2 + h_{f3}{}^2} = \frac{\sqrt{2}}{2} = -3dB20 \quad \text{(Eq. 4.18)}$$

$$\measuredangle\left(h_{f1} - jh_{f3}\right) = \measuredangle(1 - j1) = -45^o \quad \text{(Eq. 4.19)}$$

With the actual VGCA (simulation result), $h_{f1} = h_{f3} = 0.94 - 0.05j$, and the VVGCA complex current gain at maximum gain setting is:

$$\frac{1}{2}\sqrt{h_{f1}{}^2 + h_{f3}{}^2} = \frac{1}{2}\sqrt{2 \times 0.94^2} = -3.54dB20 \quad \text{(Eq. 4.20)}$$

$$\measuredangle\left(h_{f1} - jh_{f3}\right) = \measuredangle(0.94 - 0.05j - j(0.94 - 0.05j)) = -48^o \quad \text{(Eq. 4.21)}$$

This difference is observed in Figure 85.

4.2.2 Phase Resolution

Given any gain range, the phase resolution is defined as the largest phase difference between two adjacent gain states within that range. Allowing a larger variation in gain around a given gain results in better phase resolution. The figure below is the plot of system phase resolution at receive for one decibel gain intervals, chosen arbitrarily:

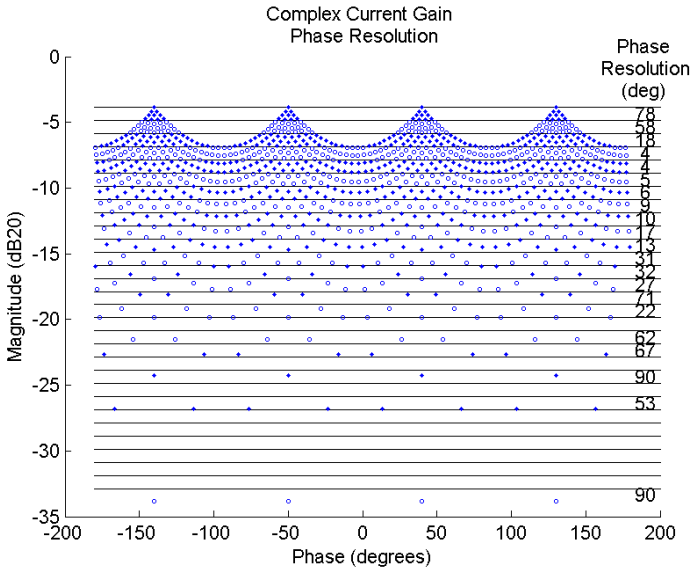

Figure 87: VVGCA complex current gain phase resolution – default terminations – schematic simulation result

4.2.3 Gain Resolution

Gain Resolution could be similarly defined as the largest gain difference between two adjacent gain states for a given phase shift range. Gain resolution can be similarly plotted. Figures below show the complex gain states separated vertically at 10^o increments. The un-shaded areas in Figure 88 and Figure 89 are the gain states within each 10^o phase slot where the maximum separation between adjacent states does not exceed $2dB$ and $1dB$ (chosen arbitrary), respectively.

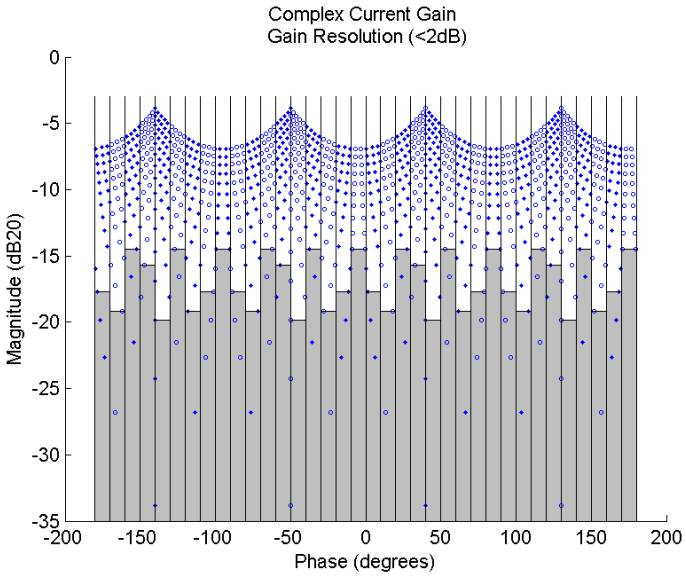

Figure 88: VVGCA complex current gain $2dB$ gain resolution – default terminations – schematic simulation result

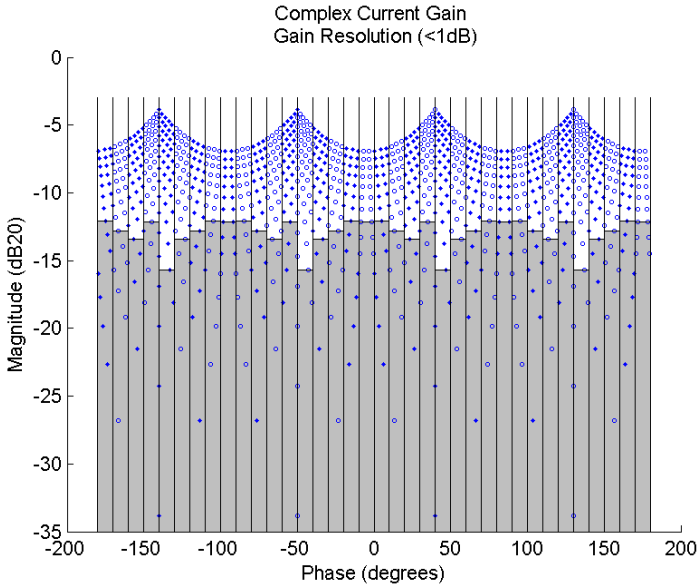

Figure 89: VVGCA complex current gain $1dB$ gain resolution – default terminations – schematic simulation result

4.2.4 Linearity

Linearity of the VVGCA is simulated using the configuration shown in Figure 90 below. The input power is supplied by only one, 50Ω port. The effect of In-phase/Quadrature input sources are captured by manually shifting the output of the Quadrature channel by 90^o and adding it to the In-phase output. This is done by passing the output Quadrature channel through an ideal 90^o phase shifter before summing it with the In-phase signal. Ideal baluns are used for differential to single ended conversion.

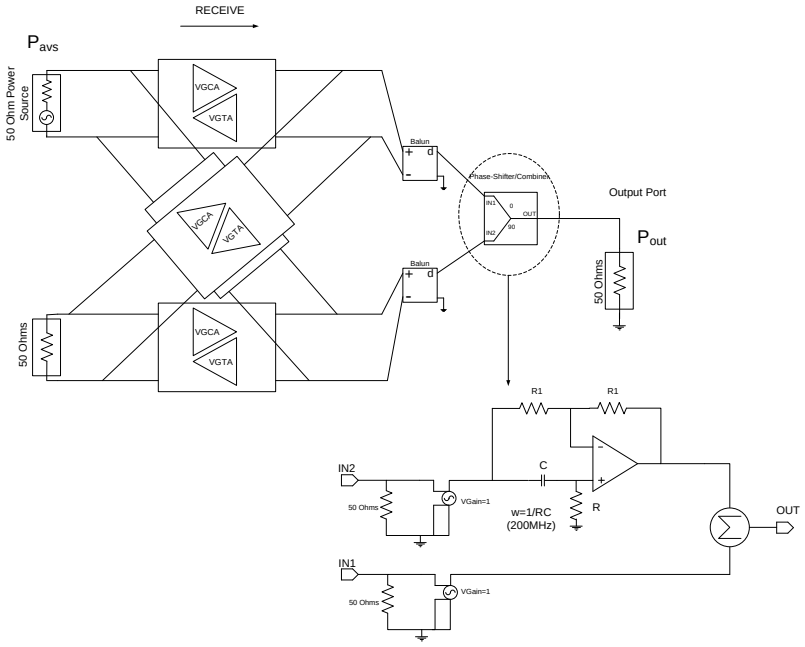

Figure 90: VVGCA linearity simulation testbench setup

Following plot shows the $1dB$ compression point of the VVGCA.[16] The available source power from the 50Ω input port is swept and the power delivered to the 50Ω output port is measured. The transducer gain is defined as:

$$G_T = (P_{del} - P_{avs})dB \qquad \text{(Eq. 4.22)}$$

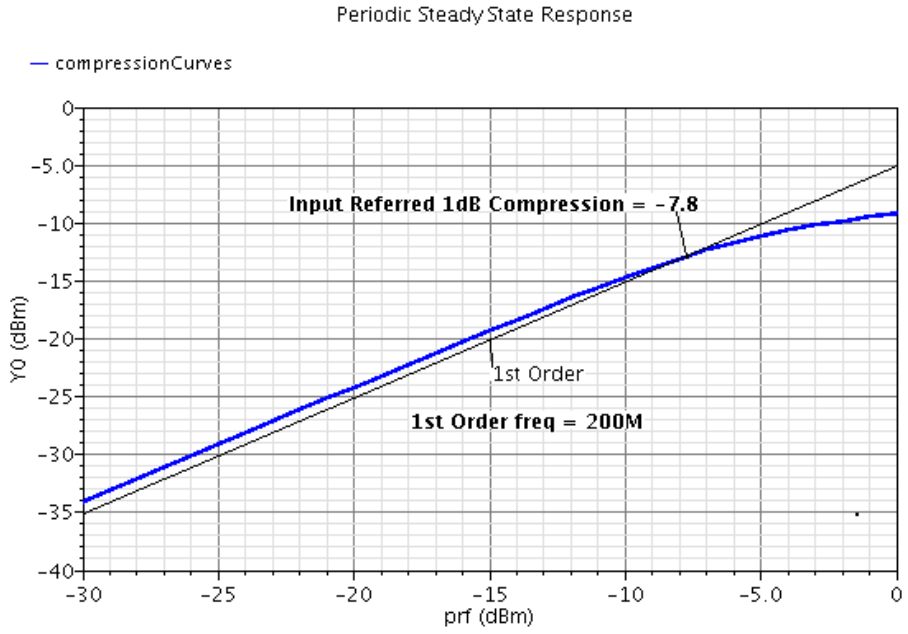

Figure 91: VVGCA $1dB$ compression point – 50Ω differential terminations – schematic simulation result

4.2.5 NF

NF simulations of the VVGCA are performed using the same setup as shown on Figure 90, with the 50Ω power source replaced by a 50Ω noise source. The baluns are

---

[16] Spectre RF Periodic Steady State (PSS) "shooting method" is used to estimate the 1-dB compression point. "Shooting Method" technique is a time domain method that operates by finding an initial condition that results in steady state.

ideal and the Phase-shifter/Adder block is comprised of ideal, noiseless components. Plot below shows the one-sided NF simulation results, with the inner two VGA's gain set to maximum ($B = 0$) and minimum ($B = 15$).

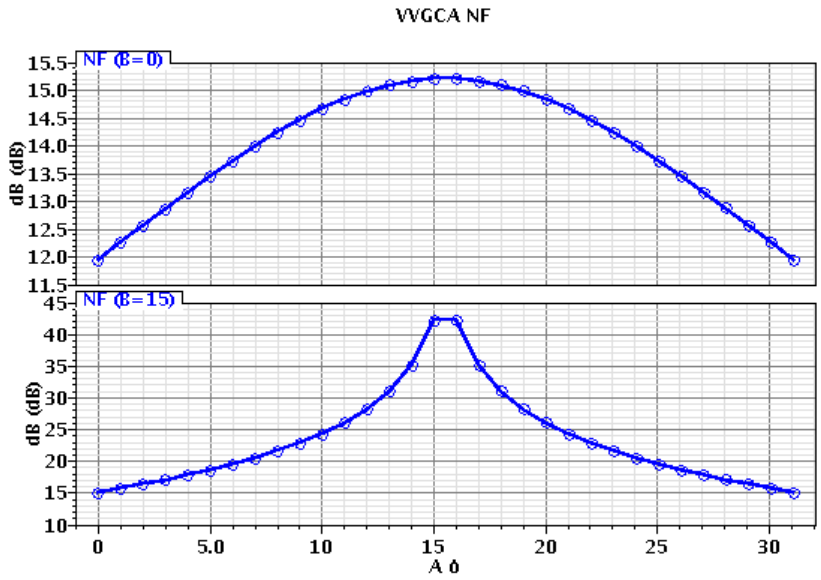

Figure 92: VVGCA NF at $200MHz$ – 50Ω differential terminations – schematic simulation result

4.3 VVGTA

Referring again to Figure 80 on page 95, for the input signal pair $Ae^{j\theta}$ and $Ae^{j\left(\theta-\frac{\pi}{2}\right)}$, the input and output signal relationships at transmit mode of operation are:

$$I = ABe^{j(\theta+\beta)} + ACe^{j\left(\theta+\varphi-\frac{\pi}{2}\right)} \quad \text{(Eq. 4.23)}$$

$$Q = ACe^{j\left(\theta+\varphi-\frac{\pi}{2}\right)} - ACe^{j(\theta+\varphi)} \quad \text{(Eq. 4.24)}$$

$$|I| = A\sqrt{\left(Bcos(\theta+\beta) + Csin(\theta+\varphi)\right)^2 + \left(Bsin(\theta+\beta) - Ccos(\theta+\varphi)\right)^2} \quad \text{(Eq. 4.25)}$$

$$\measuredangle I = \text{atan2}\left(Bsin(\theta+\beta) - Ccos(\theta+\varphi), Bcos(\theta+\beta) + Csin(\theta+\varphi)\right) \quad \text{(Eq. 4.26)}$$

$$|Q| = A\sqrt{\left(-Ccos(\theta+\varphi)+Bsin(\theta+\beta)\right)^2+\left(Csin(\theta+\varphi)+Bcos(\theta+\beta)\right)^2} \quad \text{(Eq. 4.27)}$$

$$\measuredangle Q = \text{atan2}\left(-Csin(\theta+\varphi)-Bcos(\theta+\beta), -Ccos(\theta+\varphi)+Bsin(\theta+\beta)\right) \quad \text{(Eq. 4.28)}$$

As in receive mode, for any combination of B, C, β, and φ, the signals at the output are always in-phase/Quadrature and are equal in magnitude for I'Q' input signals that are equal magnitude and in quadrature.

4.3.1 Complex Transadmittance

To examine the VVGTA, the Y-parameter equivalent circuit of VVGTA is depicted in Figure 93.

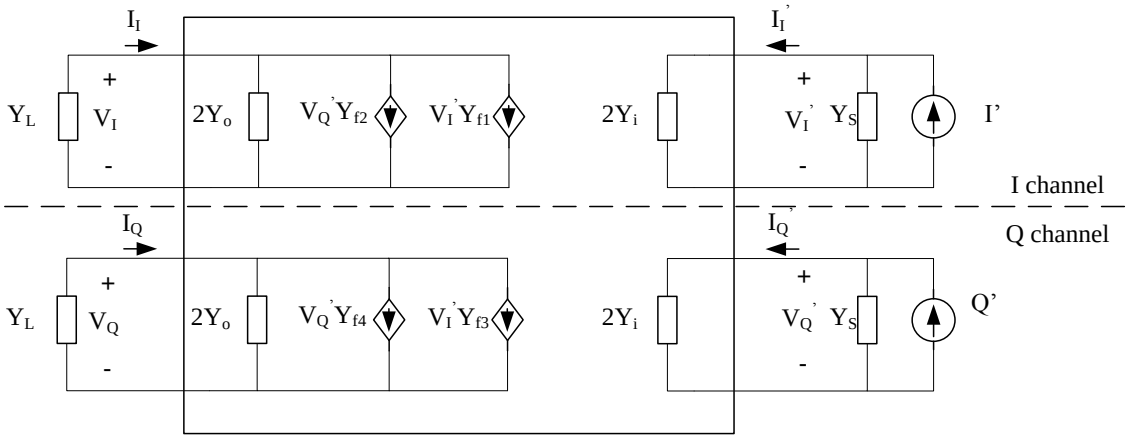

Figure 93: VVGTA y-parameter equivalent circuit

Y_{f1}thru Y_{f4} correspond to individual VGA's short circuit transfer admittance and were evaluated for each VGTA as a function of its five bit control word B in (Eq. 2.72) on page 48, repeated here for convenience:

$$Y_{f1} = \sqrt{K}\sqrt{I_{bias}\frac{W_o}{W_{ref}}}\left(\sqrt{\sum_{i=0}^{4} 2^i b_i} - \sqrt{\sum_{i=0}^{4} 2^i \overline{b_i}}\right) \quad \text{(Eq. 4.29)}$$

Y_{f2}thru Y_{f4} are defined similarly as a function of corresponding control word for each VGTA.

Following a similar procedure to that of VVGCA, complex transfer admittance of the VVGTA, $(I_I + jI_Q)/(V_I{}' + jV_Q{}')$ can be defined in terms of the previously calculated transadmittance parameters Y_f. From Figure 93 above, complex output current is evaluated as:

$$I_I + jI_Q = \frac{Y_L}{Y_L + 2Y_o}\left[V_Q{}'Y_{f2} + V_I{}'Y_{f1} + \mathrm{j}\left(V_Q{}'Y_{f4} + V_I{}'Y_{f3}\right)\right] \quad \text{(Eq. 4.30)}$$

Because $Y_{f1} = Y_{f4}$ and $Y_{f2} = -Y_{f3}$, the complex transfer admittance of the VVGTA becomes:

$$\frac{I_I + jI_Q}{V_I{}' + jV_Q{}'} = \frac{Y_L}{Y_L + 2Y_o}\left(Y_{f1} - jY_{f2}\right) = \frac{Y_L}{Y_L + 2Y_o}\left(Y_{f4} + jY_{f3}\right) \quad \text{(Eq. 4.31)}$$

$$\left|\frac{I_I + jI_Q}{V_I{}' + jV_Q{}'}\right| = \frac{Y_L}{Y_L + 2Y_o}\sqrt{{Y_{f1}}^2 + {Y_{f2}}^2} = \frac{Y_L}{Y_L + 2Y_o}\sqrt{{Y_{f3}}^2 + {Y_{f4}}^2} \quad \text{(Eq. 4.32)}$$

$$\measuredangle\frac{I_I + jI_Q}{V_I{}' + jV_Q{}'} = atan2\left(-Y_{f2}, Y_{f1}\right) = atan2\left(Y_{f3}, Y_{f4}\right) \quad \text{(Eq. 4.33)}$$

Where it's assumed:

$$\measuredangle\frac{Y_L}{Y_L + 2Y_o} \cong 0^{\mathrm{o}}$$

The values of the four transadmittance parameters are:

$$Y_{f1} = \sqrt{K}\sqrt{I_{bias}\frac{W_o}{W_{ref}}}\left(\sqrt{\sum_{i=0}^{4} 2^i b_i} - \sqrt{\sum_{i=0}^{4} 2^i \overline{b_i}}\right) \quad \text{(Eq. 4.34)}$$

$$Y_{f4} = Y_{f1} \quad \text{(Eq. 4.35)}$$

$$Y_{f3} = \sqrt{K}\sqrt{I_{bias}\frac{W_o}{W_{ref}}}\left(\sqrt{\sum_{i=0}^{4} 2^i a_i} - \sqrt{\sum_{i=0}^{4} 2^i \overline{a_i}}\right) \quad \text{(Eq. 4.36)}$$

$$Y_{f2} = -Y_{f3} \quad \text{(Eq. 4.37)}$$

Where:

$$K = K'\frac{W_{m1}}{L_{m1}}, K' \approx 66.6\frac{uA}{V^2}^{17}, W_{m1} = 54.56um, L_{m1} = 180nm, I_{bias} = 580uA,$$

$$W_o = 1.76um, and\ W_{ref} = 54.56um$$

The complex transadmittance magnitude versus phase of the VVGTA are plotted for 2^{10} different gain states in following plot:

[17] Value provided by MOSIS from lot average results obtained from measurements of MOSIS test structures on wafers of a fabrication lot.

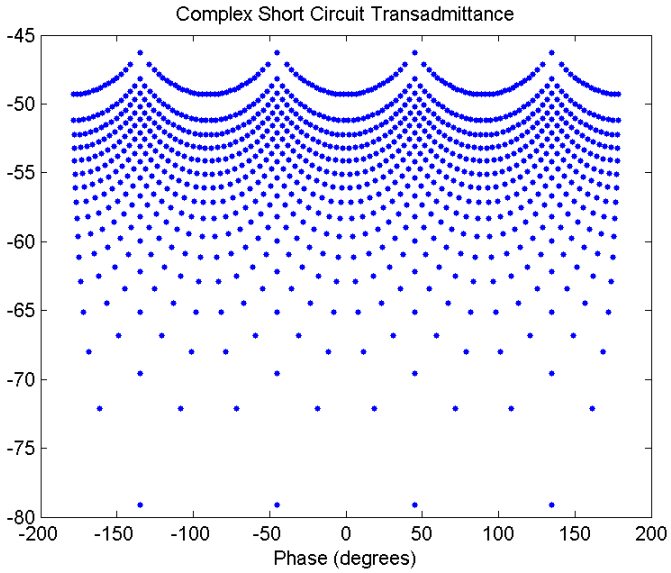

Figure 94: VVGTA complex transadmittance (relative to one siemen) – ideal

Figure 95 below is the VVGTA complex Transadmittance obtained from schematic simulation results:

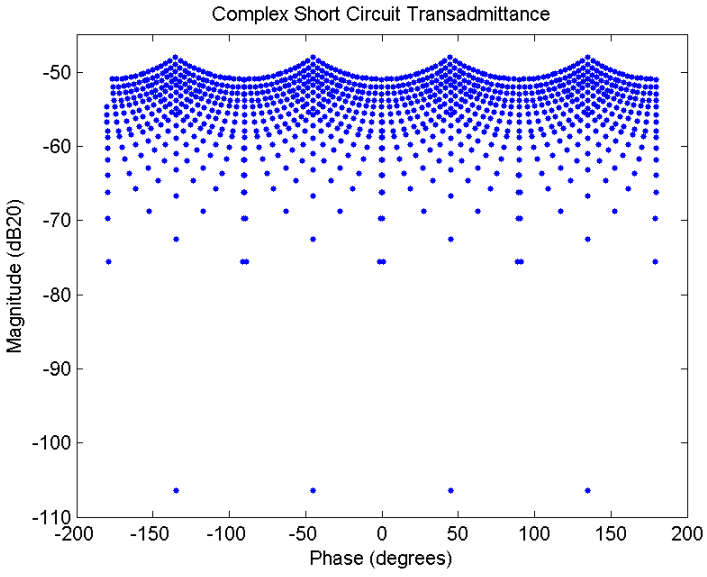

Figure 95: VVGTA complex transadmittance (relative to one siemen) – short output termination – schematic simulation result

The ideal, complex short circuit transconductance, and that obtained through schematic simulation results are plotted in figure below:

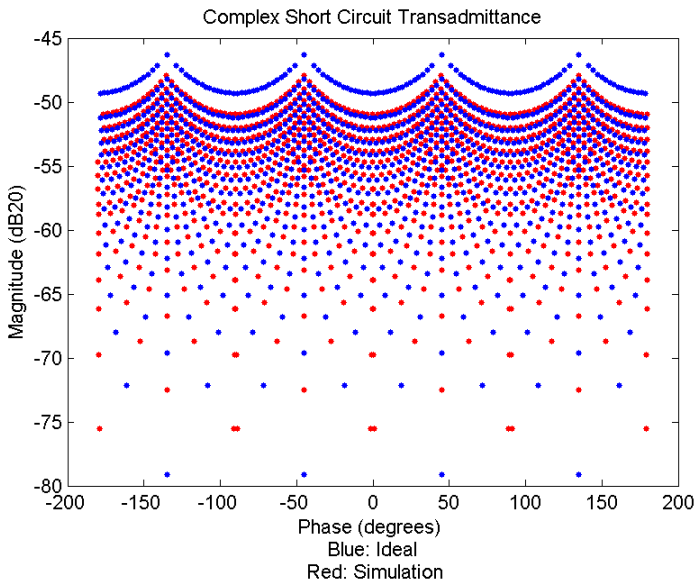

Figure 96: VVGTA complex transadmittance **(**relative to one siemen) – short output termination – ideal (Blue) vs. schematic simulation result (Red)

As depicted in Figure 96 above66 and explained on page 66, the minimum gain states, $A = 15$ and $A = 16$, exhibit a smaller than ideal transadmittance magnitude. This lower than expected gain magnitudes of the VGTA at low gain states affects the VVGTA complex transadmittance as follows: Due to lower gain at states $A\ and\ B = 15{,}16$, Gain state pairs (A, B)[18] that include the minimum gain settings, for example $(A = 15, B = 0{,}1{,}2 \ldots 15)$ and $(A = 16, B = 0{,}1{,}2 \ldots 15)$, exhibit smaller phase offset from one

[18] A and B correspond to the two independent 5-bit control words used for VVGA gain control. See Figure 6: *Gain control for VVGA* on page 19.

another compared to the ideal phase offset. This becomes more apparent for gain state pairs that include a high and a low gain state, for example states $s1 = (A = 15, B = 0)$ and $s2 = (A = 16, B = 0)$. At these gain states, the phase shift contribution of gain states 15 and 16 is much smaller than ideal and almost negligible, causing the complex transadmittance of states $s1$ and $s2$, in the above example, to exhibit almost zero phase offset from one another. Figure below is the ideal and simulation result comparison of transadmittance states $(A = 15, B = 0,1,2 \ldots 15)$ and $(A = 16, B = 0,1,2 \ldots 15])$.

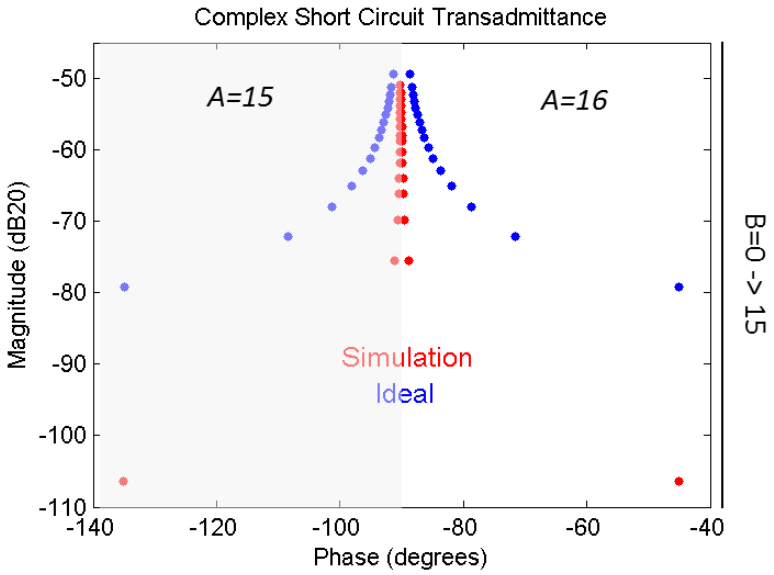

Figure 97: VVGTA complex transadmittance (relative to one siemen) – short output termination – effect of lower VGTA transconductance magnitude than ideal at minimum gain states

As observed in the simulation results in Figure 97, as B decreases, the phase shift between the two adjacent states, $(A = 15, B = 0,1,2 \ldots 15)$ and $(A = 16, B = 0,1,2 \ldots 15)$, reduces and becomes almost zero at states $(A = 15, B = 0)$ and $(A = 16, B = 0)$. .

The magnitude mismatch between the simulated and ideal VGTA transadmittance at maximum gain states ($A = 0\ and\ A = 31$), as depicted on Figure 52 on page 66, results in a mismatch between the ideal and simulated complex transadmittance magnitude of state pairs that include the highest gain states. As evident from Figure 96, simulation results indicate a lower complex gain magnitude than that of ideal at state pairs ($A = 0{,}31, B = 0{,}1{,}2 \ldots 31$) and ($A = 0{,}1{,}2 \ldots 31, B = [0{,}31]$). To demonstrate this effect more clearly, Figure 98 below is the VVGTA Complex Transadmittance for state pairs that only include maximum gain states:

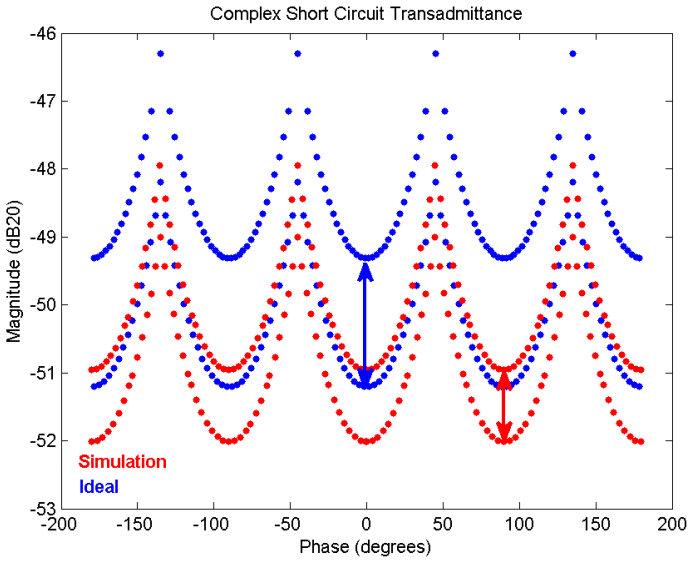

Figure 98: VVGTA complex transadmittance (relative to one siemen) – short output termination – effect of lower VGTA transconductance magnitude than ideal at maximum gain states

Lastly, the much smaller values of complex transadmittance at minimum gain settings, as observed on Figure 96, is also a direct consequence of smaller simulated VGTA transconductance compared to the ideal, normalized transconductance.

Figure 99 below shows the VVGTA complex Transadmittance for a 160Ω output resistance, compared to the expected complex transadmittance calculated.

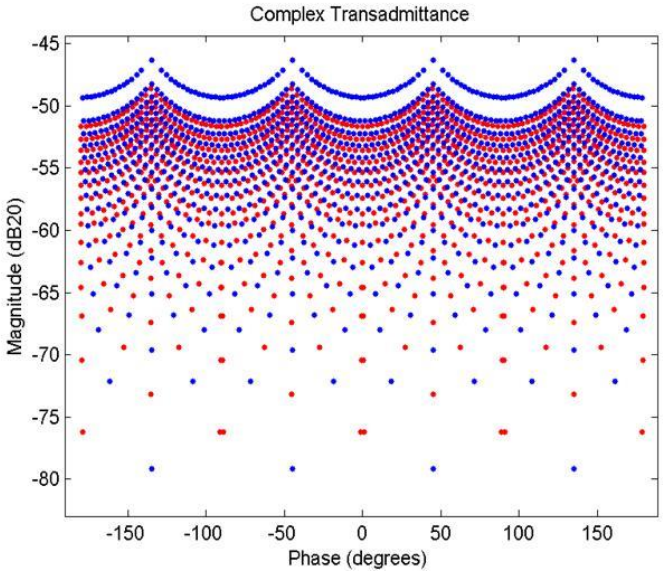

Figure 99: VVGTA complex transadmittance (relative to one siemen) – default terminations – ideal (Blue) vs. schematic simulation result (Red)

4.3.2 Phase Resolution

Figure below is a plot of system phase resolution at transmit for one decibel gain intervals, chosen arbitrarily. The lower plot is the zoomed in version of the Phase Resolution plot.

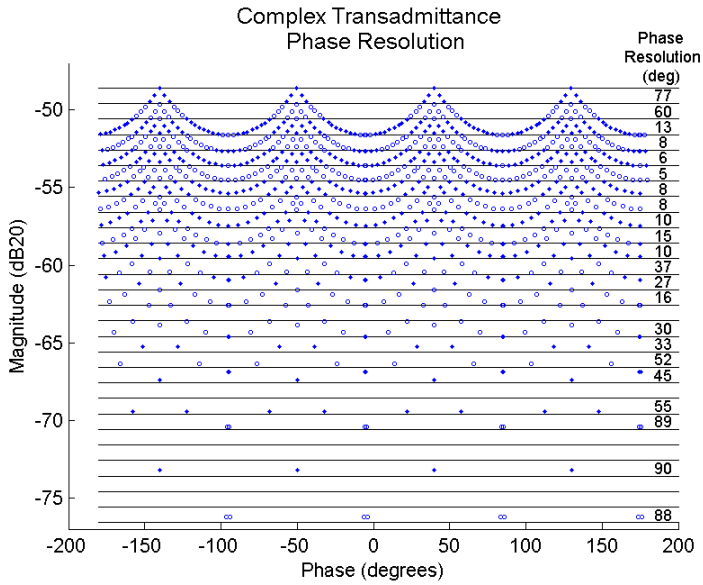

Figure 100: VVGTA complex transadmittance (relative to one siemen) phase resolution – default terminations – schematic simulation result

4.3.3 Gain Resolution

Gain resolution can be similarly plotted. Figures below show the complex gain states separated vertically at 10^o increments. The un-shaded areas on the following plots are the gain states within each 10^o phase slot where the maximum separation between adjacent states does not exceed $2dB$ and $1dB$, respectively.

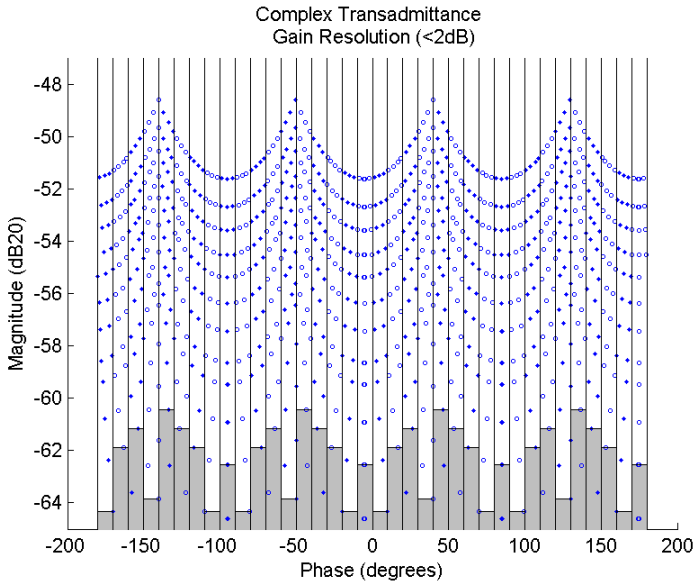

Figure 101: VVGTA complex transadmittance (relative to one siemen) $2dB$ gain resolution – default terminations – schematic simulation result

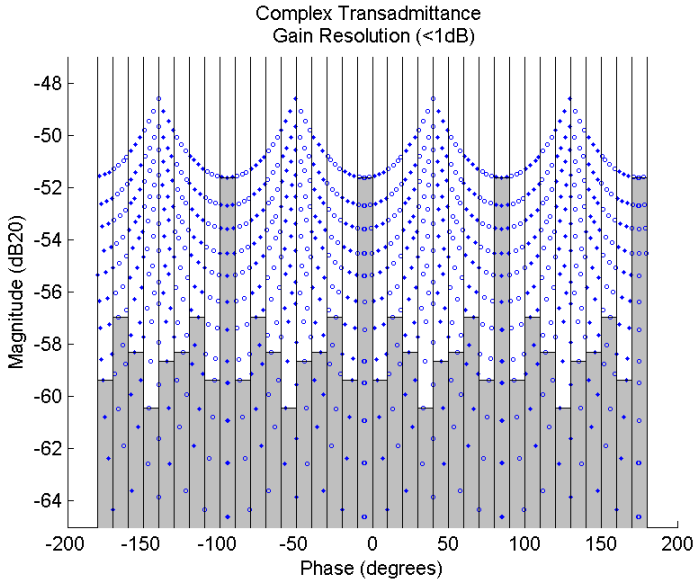

Figure 102: VVGTA complex transadmittance (relative to one siemen) $1dB$ gain resolution – default terminations – schematic simulation result

4.3.4 Linearity

Linearity of the VVGTA is simulated using the same setup as shown on Figure 90 on page 106, with direction of signal flow changed to transmit.

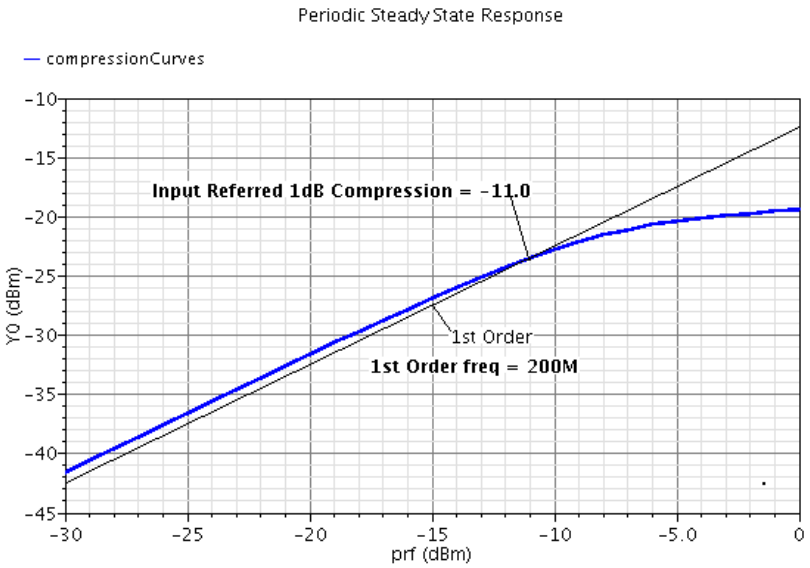

Figure 103: VVGTA $1dB$ compression point – 50Ω differential terminations – schematic simulation result

4.3.5 NF

NF simulations of the VVGTA are performed using the same setup as shown on Figure 90 on page 106, with the 50Ω power source replaced by a 50Ω noise source and the direction of signal flow switched to transmit mode of operation. The baluns are ideal and the Phase-shifter/Adder block is comprised of ideal, noiseless components. Plot below shows the simulation results for the system NF, with the inner two VGA's gain set to maximum ($B = 0$) and minimum ($B = 15$) while sweeping the outer two VGA's gain states.

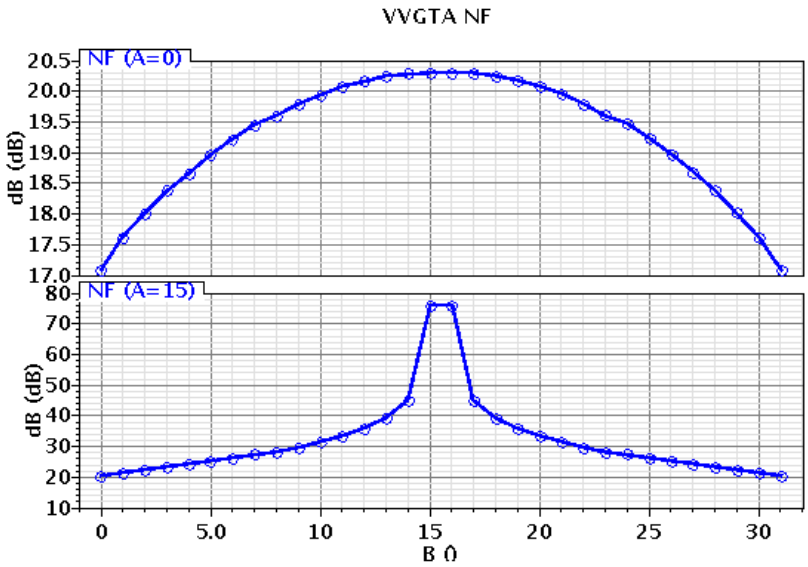

Figure 104: VVGTA NF at $200MHz$ – 50Ω differential terminations – schematic simulation result

CHAPTER 5

PHYSICAL LAYOUT AND POST-LAYOUT SIMULATIONS

In this and proceeding chapters, the layouts, post-layout simulation results, and post-fabrication measurement results correspond to the original VGA and VVGA designs that differ from what has so far been presented in this thesis. The original designs exhibit flaws that were corrected in this thesis and presented results so far have corresponded to the fixed designs. A detailed explanation of the design flaws and corrective actions taken are explained in Appendix A. Because the corrected actions are not reflected in layout nor were fabricated, current and proceeding chapters correspond to layout, post-layout simulation results, and post-fabrication measurement results of the original design.

$180nm$ IBM CMR7SF technology was used for layout with six available metal masks. Standard cell, 1.8V CMOS devices with $3.5nm$ oxide thickness were used for all layouts, using NFET_RF and PFET_RF standard cells as depicted in Figure 105 and Figure 106 of this section.

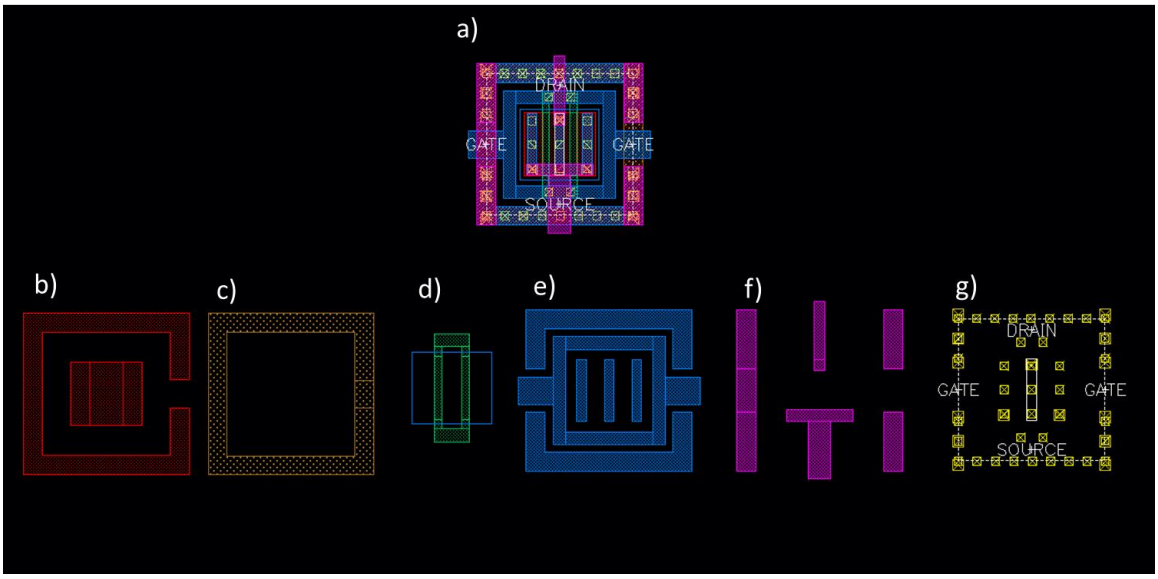

Figure 105: IBM cmrf7sf NFET_RF mask levels a) complete layout. Mask Levels: b) RX c) BP d) PC and DG e) metal 1 f) metal 2 g) stud contacts and wiring level vias

Figure 105 is the layout view of the cmrf7sf nfet_rf cell along with its comprising masks. The NMOS shown is a 2 finger ($1.6um$ per finger), $180nm$ device[19]. The RX mask corresponds to n+ diffused regions making the source and drain tubs. The BP mask level areas are blocked from n+ source drain implants and are used for body contact implantation. The PC mask is the Polysilicon line mask, which, over DG mask (blue square in (d)) receives a thicker gate oxide. The inner metal one square in (e) is connected to the polysilicon by use of PC to M1 contacts, and the outer half rectangles are connected to RX by use of RX to M1 vias for body connection. Metal two is used for source and drain connection and also as an extra metal layer for body connection. The

[19] Dimensions correspond to the building block NMOS ($M1_0$and $M2_0$) shown on Figure 17 on page 32.

three metal one lines in (e) connect metal two to RX for drain and source connections. Stud contacts (connecting either RX or PC to M1) and V1 vias (M1 to M2) are shown in (g). [12]

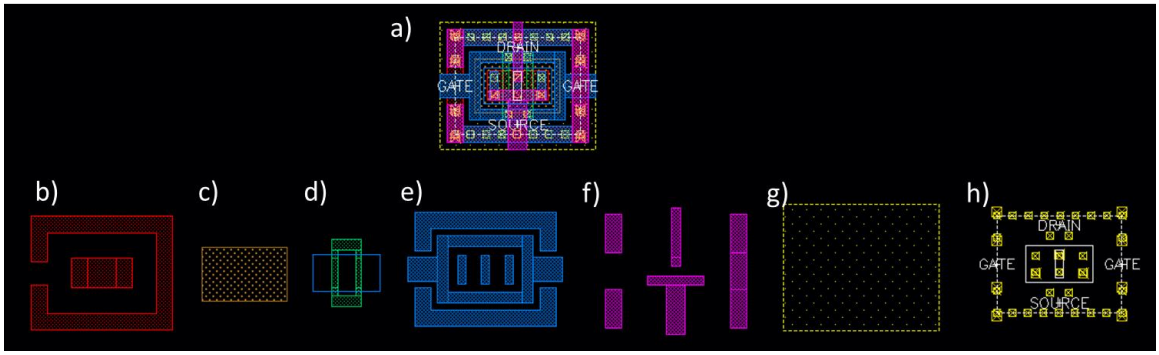

Figure 106: IBM cmrf7sf PFET_RF mask levels a) complete layout. Mask Levels: b) RX c) BP d) PC and DG e) metal 1 f) metal 2 g) NWELL h) stud contacts and wiring level vias

The inner RX mask level corresponds to p+ diffused regions and the outer corresponds to n+ diffused region used for substrate contact. The BP mask level masks the p+ diffused areas (inner part of RX mask) from the n+ implant.

5.1 VGA Layout

The digital implementation of gain control for the VGCA thru adjustable transistor widths requires $4 \times (2\text{^}5 - 1) = 124$ NMOS transistors to be laid out for each VGA (Figure 105). The layout view of transistors M_1 thru M_4 depicted on Figure 17: *VGCA variable effective gain circuit diagram* on page 21 is shown below:

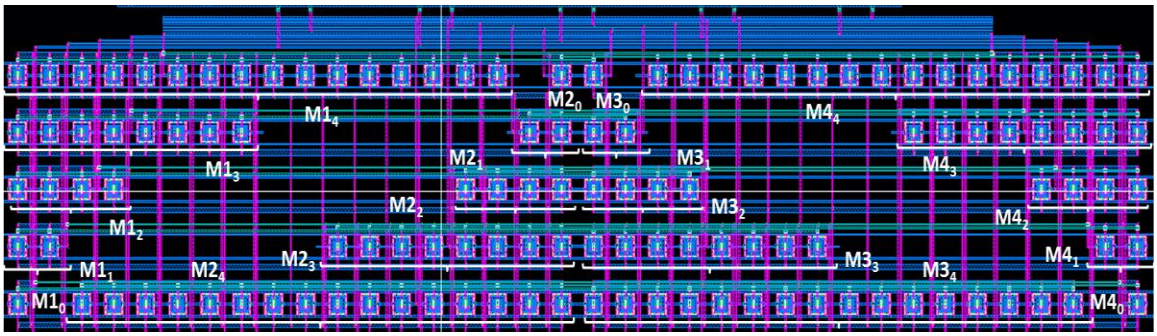

Figure 107: VGA NMOS transistor layout

Transistor names on Figure 107 correspond to the naming convention used on Figure 17 on page 21. The blue traces are metal one layer, laid out from inverter outputs to charge the gates of appropriate transistors for gain control. Transistors comprising M_1 have their drain and source terminals connected by use of metal two wire traces that are drawn vertically, as seen in red on Figure 107. Transistors M_1 and M_2 have their drain and source terminals connected, again using metal two traces. This arrangement repeats for transistor pair M_3 and M_4. The gates of transistors M_2 and M_3 are connected with metal layer one, and the connection between gates of transistors M_1 and M_4 is achieve using metal three layer.

Figure 108 shows the completed layout of the VGA:

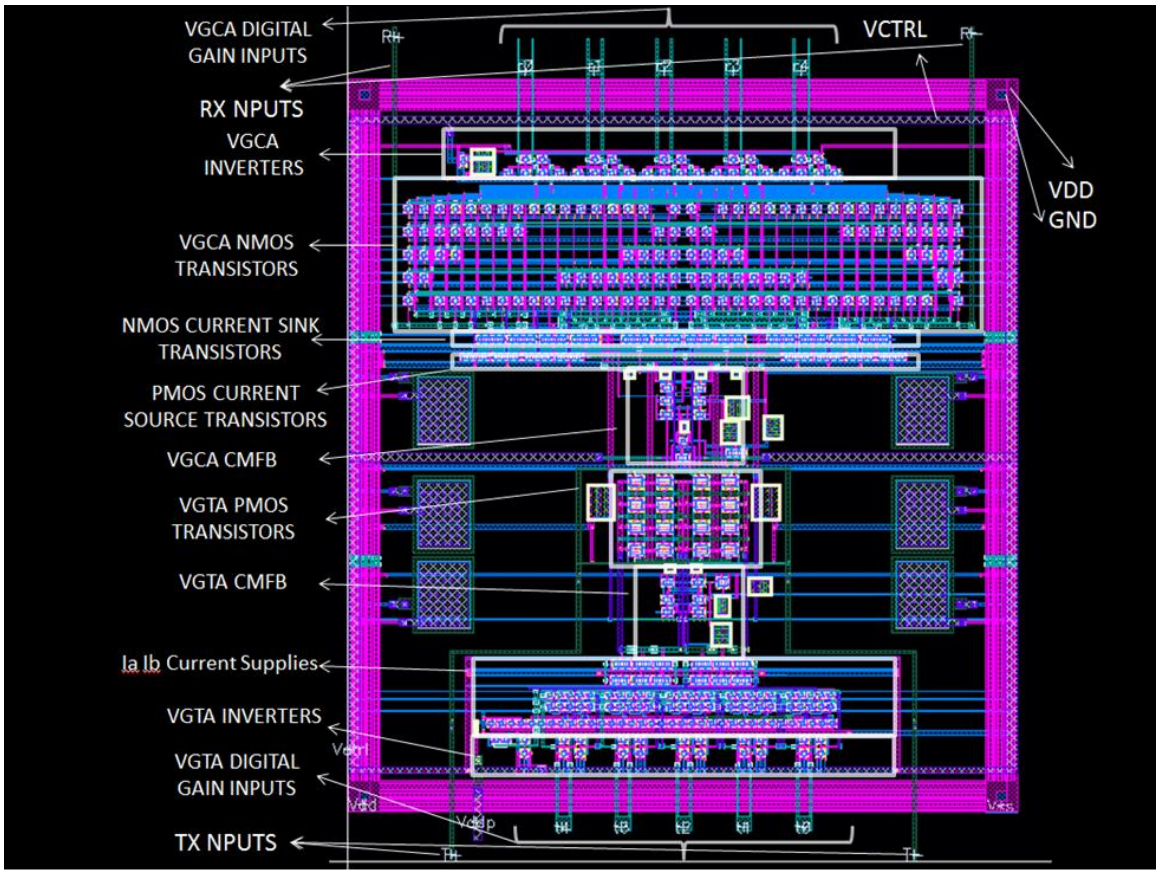

Figure 108: VGA layout

1.5pF metal to metal (MIM) capacitors ($31um\ x\ 24um$) are used as bypass capacitors between power and ground lines. Metal two and one are used for supply voltage and ground, respectively, and are routed around the VGA. All resistors are

$260\ \Omega/\square$ P+ polysilicon. High sheet resistance, low absolute resistance and mis-match sensitivity motivated this choice. [20]

Bond pads are $114um \times 114um$ in dimension and are taken directly from the *cmrf7sf* library. Adding the bond pad models results in the finalized VGA layout depicted in Figure 109 below:

---

[20] According to [10], of the OP resistors, P+ polysilicon resistors have the lowest mismatch after the N+ S/D resistor (72Ω of sheet resistance), and the best Absolute Resistance Sensitivity after OP RP (165Ω of sheet resistance) and K1 BEOL (61Ω of sheet resistance).

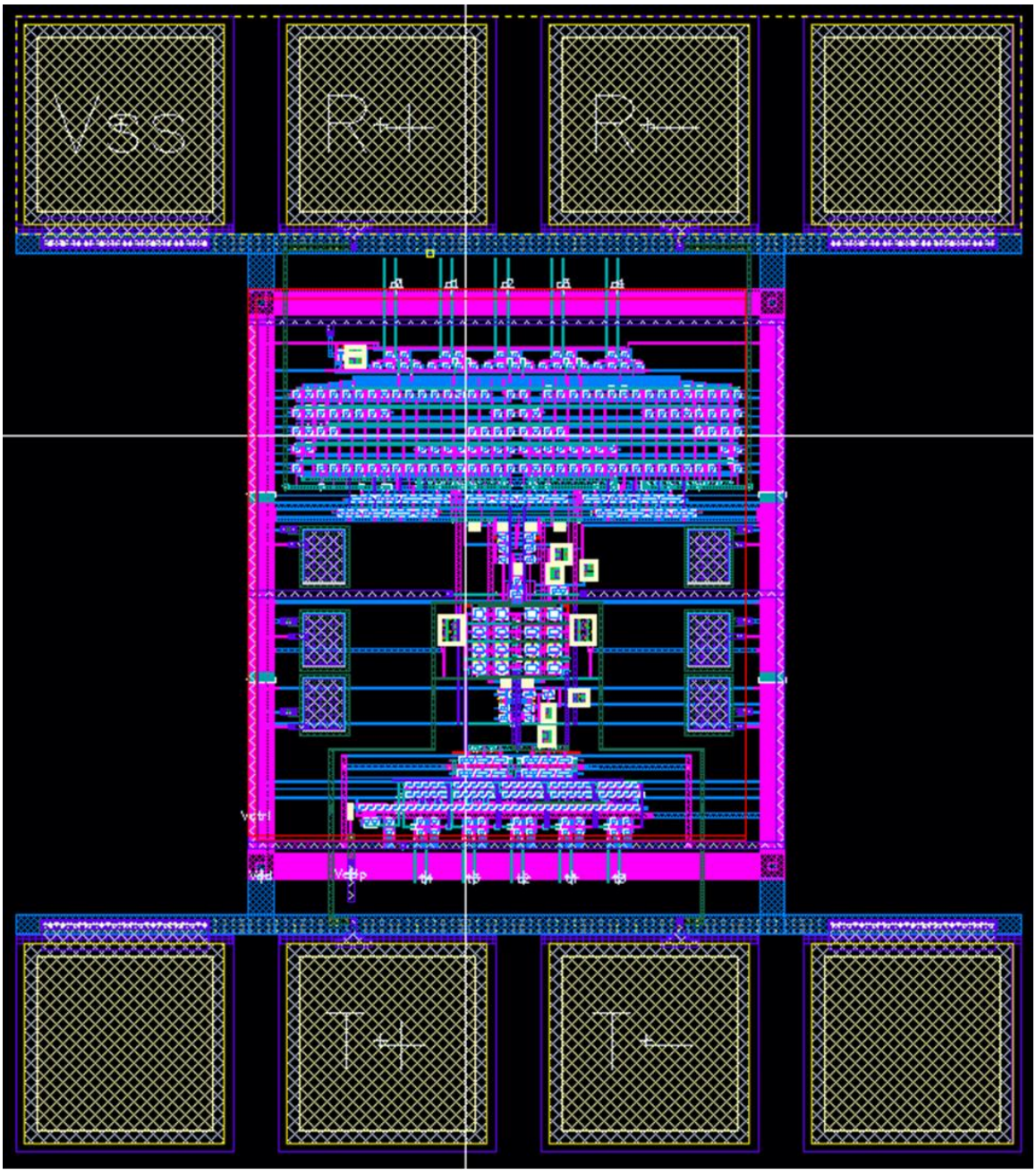

Figure 109: VGA layout including bond pads

5.2 VVGA Layout

To layout the VVGA, the individual VGAs are connected together as shown conceptually in Figure 74 on page 88. Figure 110 below is the layout view of the VVGA:

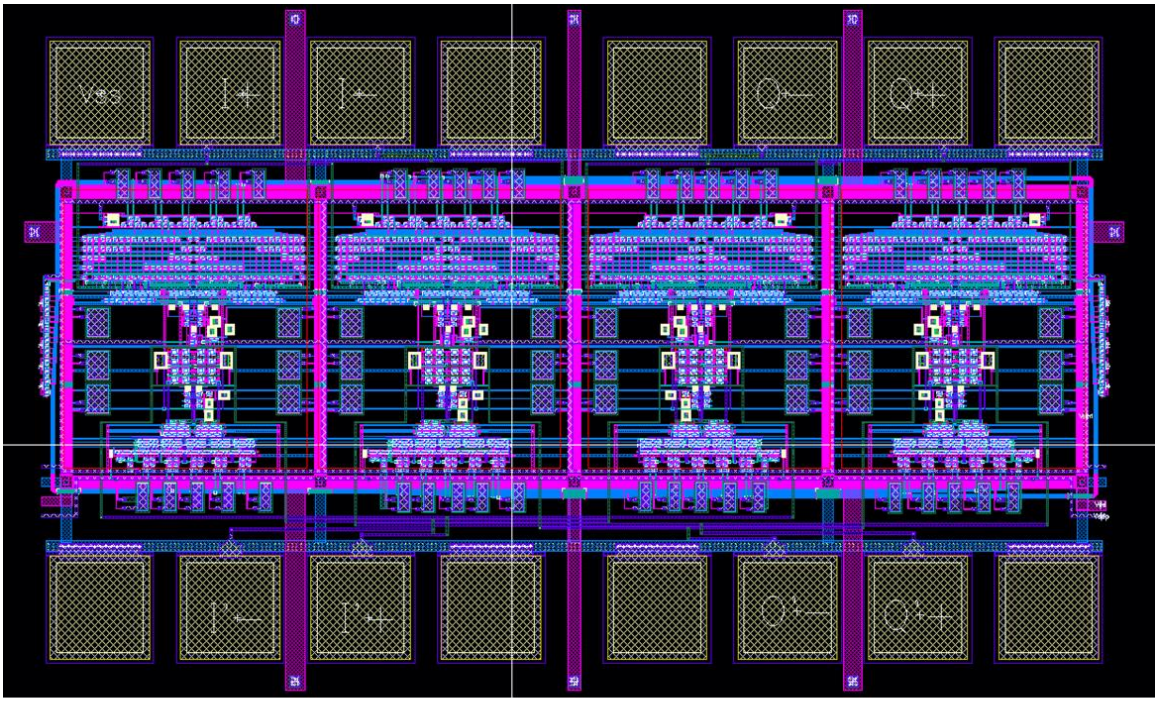

Figure 110: VVGA layout

DC control signals for the VGCA are routed thru metal one at the top of the figure, and the control voltages for the VGTA are routed on the bottom. The inner two VGAs' DC control voltages are supplied by their control word that is fed to a $5\ to\ 10$ de-mux on the right side of the block. The purpose of this de-mux is to route the control word signals to either the VVGCA or the VVGTA, based on the value of control signal switch, V_{ctrl}. The outer two VGAs' DC control signals are supplied similarly by a de-mux on shown on the left side of the layout view on Figure 110. The weakness of this design is

the long metal one lines routing the DC signals to the VGA inverters. As an example, the LSB of control word A, supplied by the de-mux on the left, is routed over $1.3mm$ before it is connected to the input of the VGA inverter on the right. It is noted that the RC drop is not a concern for these lines.

To dampen any high frequency noise coupling onto the DC control lines, MIM bypass capacitors are used at the input of each VGA inverter series. The capacitors are $31um \times 12um$ in dimension, and are approximately $750fF$ in value. Figure 111 shows these capacitors:

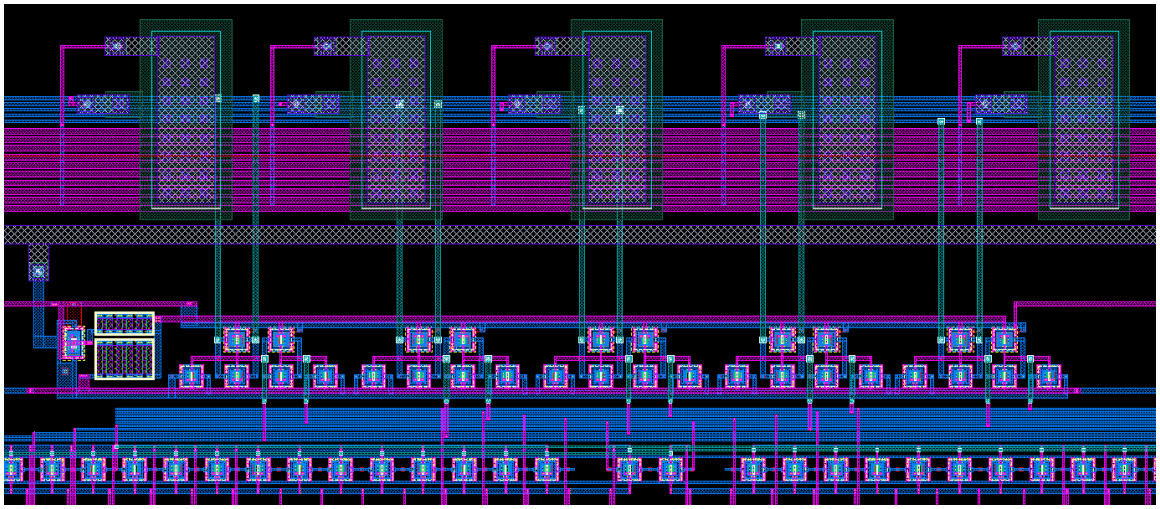

Figure 111: DC control signals' bypass capacitors

The blue lines correspond to metal one wires that are connected at one end to the output of the appropriate de-mux, and at the other end (shown in figure) to the input of the inverter series. The red traces underneath the MIM capacitors correspond to the supply voltage, and blue traces underneath them (not visible in figure) are the ground metal one traces.

5.3 Full Chip Layout

Figure 112 below is the layout view of the entire chip. Chip dimensions are $5mm \times 5mm$, and it contains instances of VGA, VGCA, VGTA, VVGA, and the IQ Mixer.

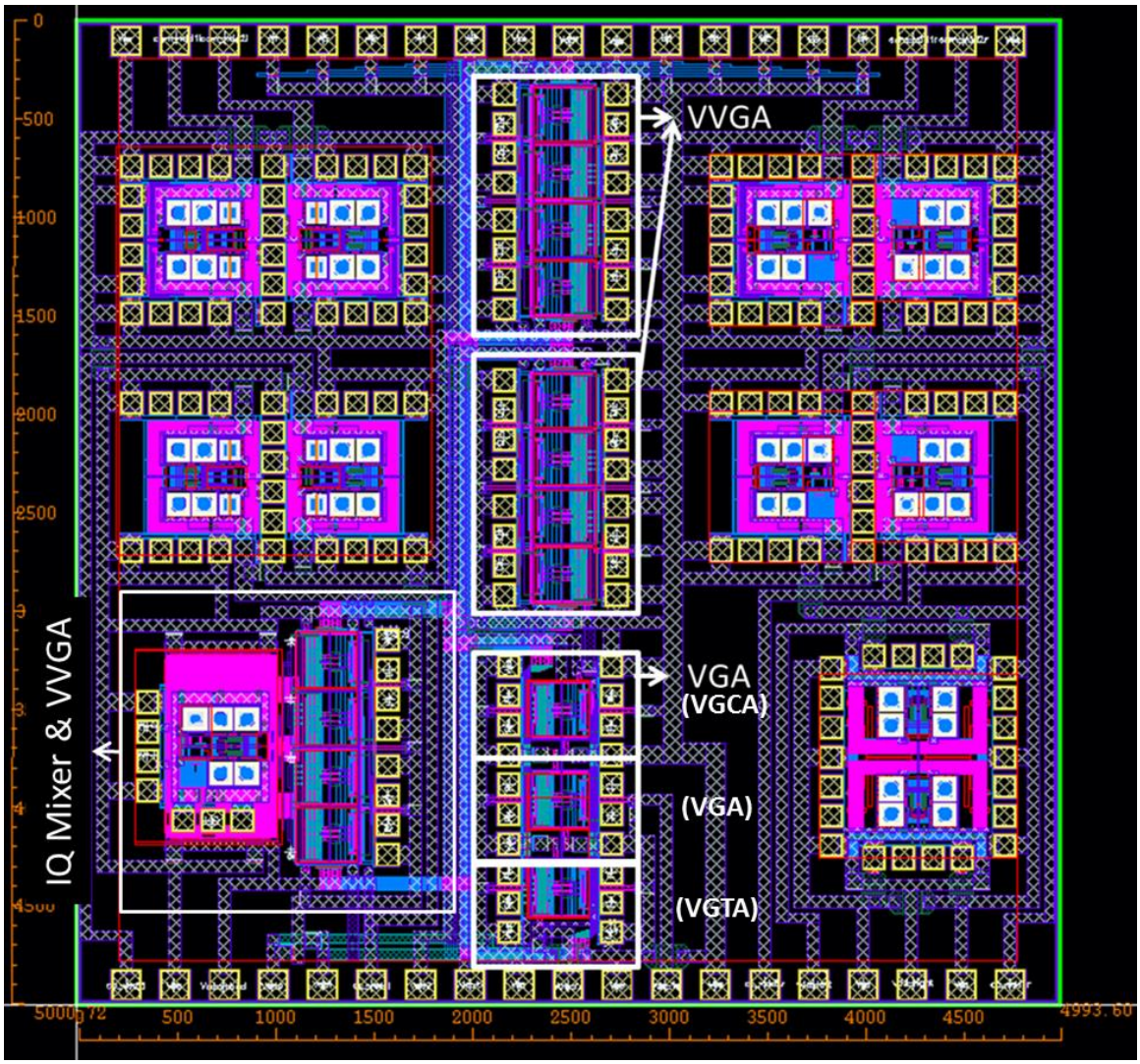

Figure 112: Full chip layout

5.4 Schematic vs. Parasitic Extracted Simulation Results

Assura® Physical Verification Tool Suite was used to enable post-layout simulations. Post layout simulations were done using the parasitic capacitance and parasitic resistance extracted netlists of VGAs and VVGAs. Assura® DRC (Design Rule Checking) was used to check the layout against geometric spacing, width, and other rules and eliminate any design rule violations. Assura® LVS (Layout Versus Schematic) comparison was used to extract devices from the layout and create a layout netlist to compare to schematic netlist to ensure no mismatches are present. Assura® RCX (Resistance, Capacitance, and Inductance Extraction) was then used to create a netlist including extracted parasitic resistances and capacitances from the layout for post-layout simulations.

5.4.1 VGCA

DC

Figure 113 depicts the DC common mode voltage obtained from the layout extracted netlist compared to that of schematic. The dotted line indicates the DC voltage of the positive input node.

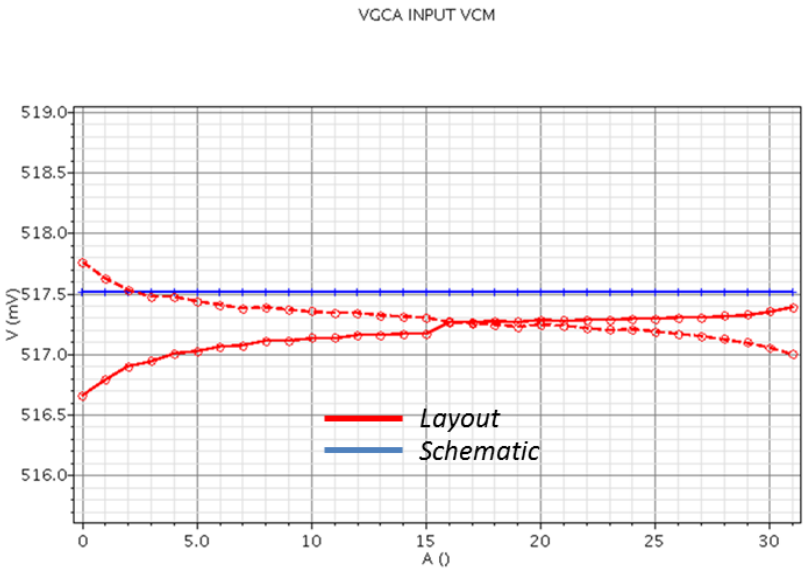

Figure 113: VGCA input common mode voltages – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

The output common mode is similarly plotted:

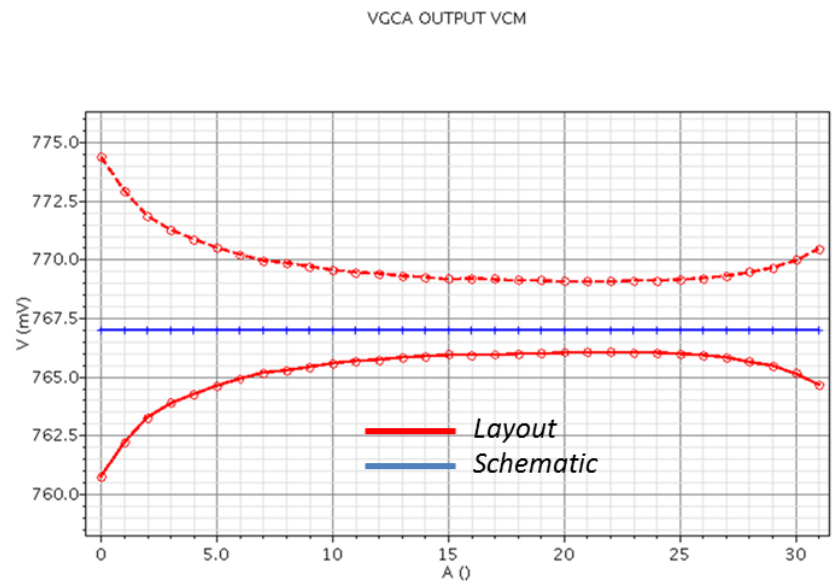

Figure 114: VGCA output common mode voltages – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

Input Impedance

Parasitic extracted and schematic netlist short circuit input impedance of the VGCA is compared next.

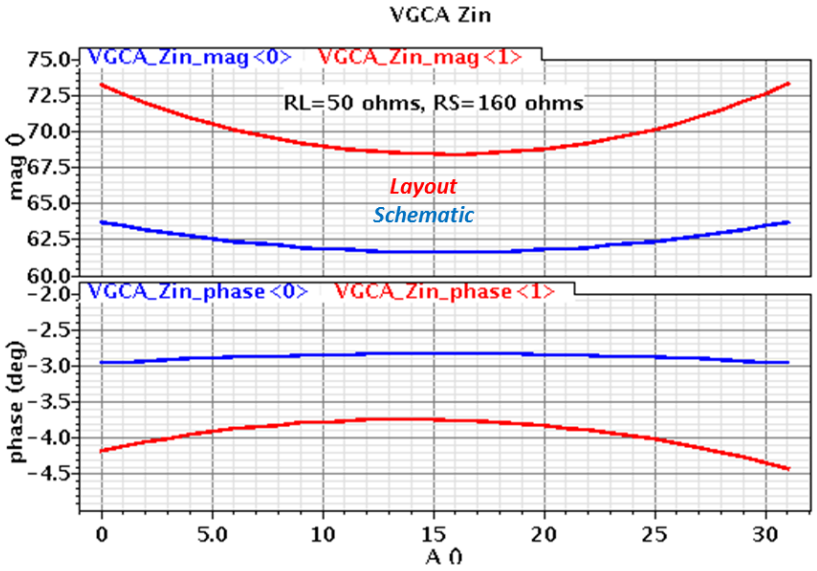

Figure 115: VGCA input impedance – default terminations – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

The parasitic extracted impedance result shows a 10Ω magnitude (mostly resistive) increase compared to the schematic level simulation results. This increase in resistance can be explained as due to the sheet resistance of the metal wires. At almost seven ohms,

the most significant contribution to this increase is the resistance added to the input path from the top level metal route at the input.[21]

Output Impedance

The output impedance post-layout simulation results along with the schematic results are shown in figure below:

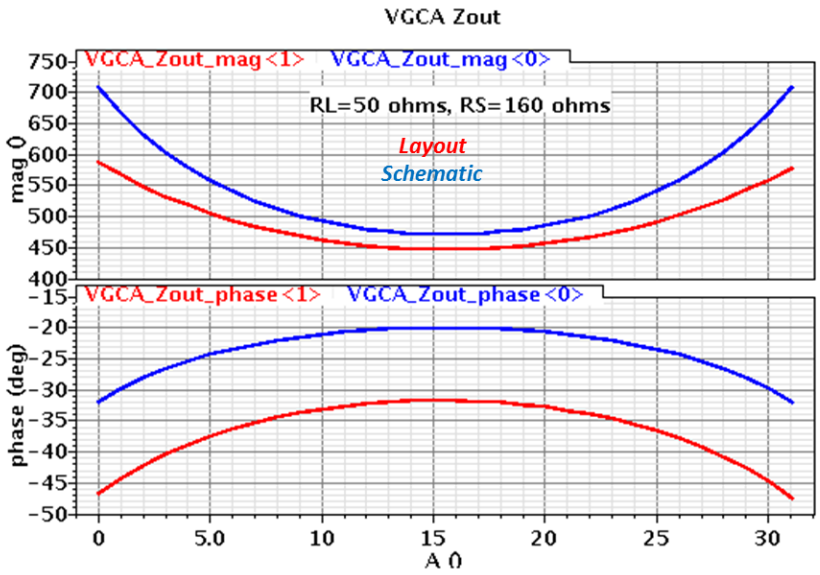

Figure 116: VGCA output impedance – default terminations – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

VGCA output impedance versus frequency at maximum gain setting is plotted below:

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[21] 2um wide, 140um long MT metal layer at $R_s = 0.089\ \Omega/\square$ [10]

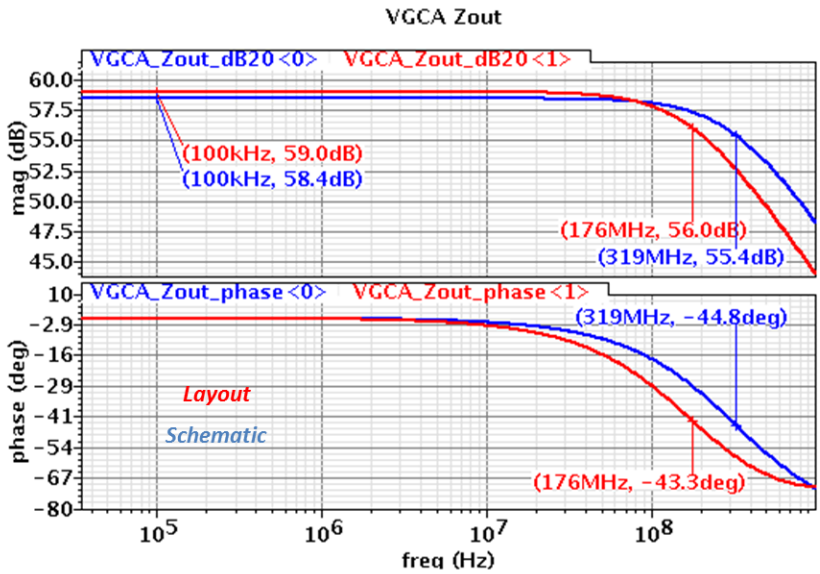

Figure 117: VGCA output impedance ($s = 0$) vs. frequency – default terminations – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

From figure above:

$$R_{o,sch} = 832\Omega, \omega_{3-dB} = 2\pi(319\text{MHz}), C_{o,sch} = \frac{1}{\omega_{3-dB} R_{o,sch}} = 600fF \quad \text{(Eq. 5.1)}$$

$$R_{o,ext} = 891\Omega, \omega_{3-dB} = 2\pi(176\text{MHz}), C_{o,ext} = \frac{1}{\omega_{3-dB} R_{o,ext}} = 1pF \quad \text{(Eq. 5.2)}$$

The small increase in resistance from schematic to layout is mostly due to metal routing at the output of the VGCA. The increase in output capacitance, although not confirmed, is most likely attributed to addition of metal to metal and metal to substrate capacitance in the extracted netlist.

Current Gain

The current gain of the VGCA, with 50Ω differential termination, is shown in Figure 118. The post layout and schematic simulation results are almost identical.

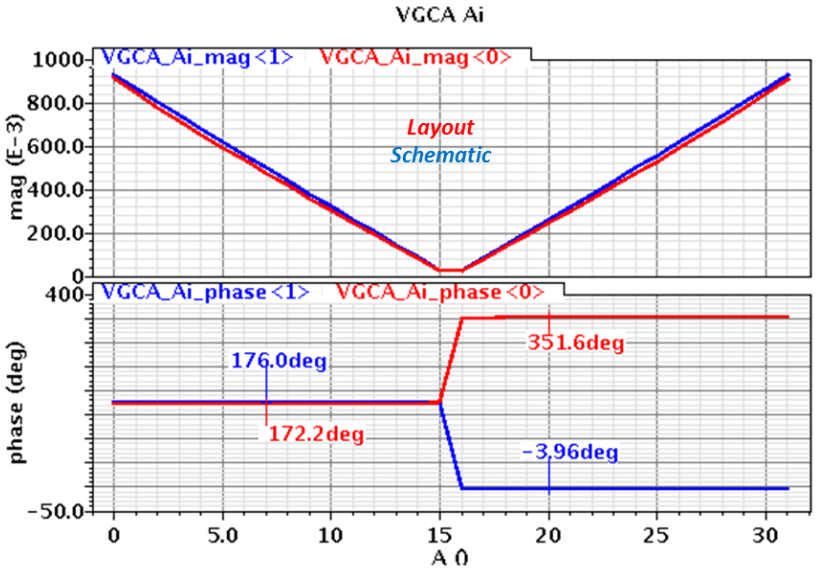

Figure 118: VGCA current gain – default terminations – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

NF

The NF simulation results show a $1dB$ degradation in post layout simulations:

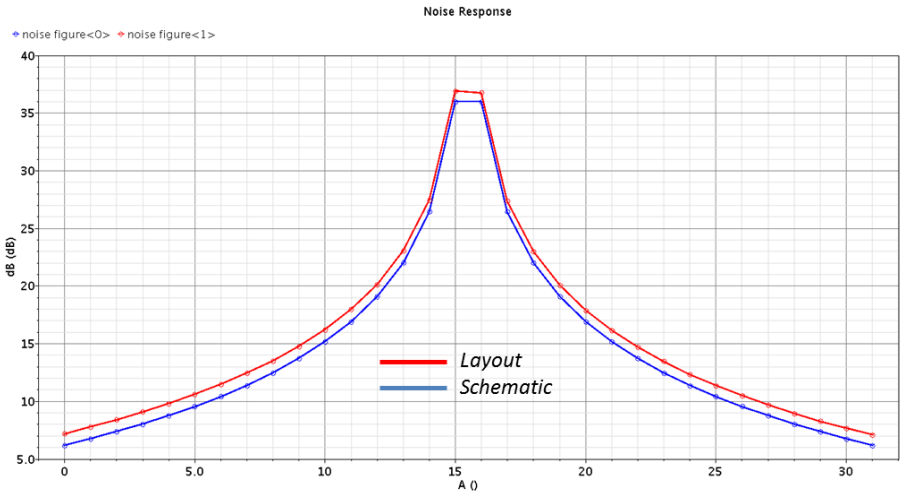

Figure 119: VGCA NF at $200MHz$ – 50Ω differential terminations – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

The degradation in NF in post-layout simulations is not due to an increase in the equivalent output noise power of the VGCA after extraction. Figure below corresponds to VGCA output spectral noise density. Output noise power is nearly identical at $200MHz$ for extracted and schematic simulation results.

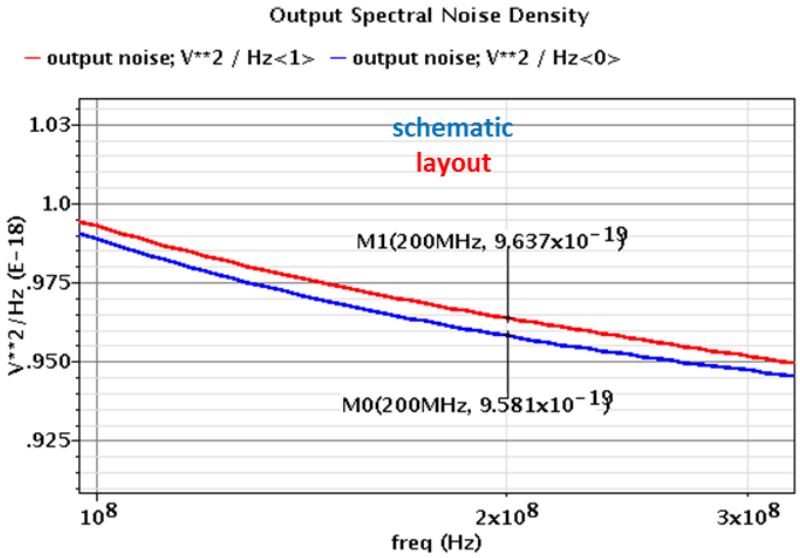

Figure 120: VGCA output spectral noise density at $200MHz$ at highest gain state – 50Ω differential terminations – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

With nearly identical equivalent output noise, the degradation in NF in post-layout simulation is caused by a drop in extracted VGCA voltage gain compared to that of the schematic. Figure 121 below is the plot of VGCA differential voltage gain across frequency:

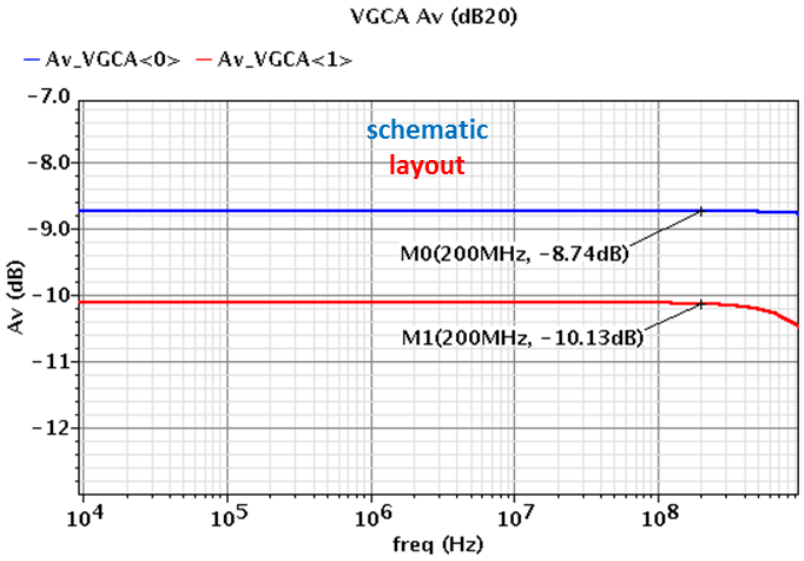

Figure 121: VGCA voltage gain at highest gain state vs. frequency – default terminations – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

Although VGCA output impedance at $200MHz$ reduces by around $1-dB$ in post-layout simulation, this drop does not affect the voltage gain noticeably as this impedance appears in parallel with the 50Ω differential load at the output. The drop in voltage gain, therefore, can only be explained by a drop in the extracted VGCA short circuit transconductance:

$$A_v = G_m(Z_o||50\Omega) \quad \text{(Eq. 5.3)}$$

Figure 122 below is the plot of VGCA differential short circuit transconductance, obtained by injecting an AC-signal using an ideal ac-coupled differential voltage source at the input and measuring the incrementally shorted output current.

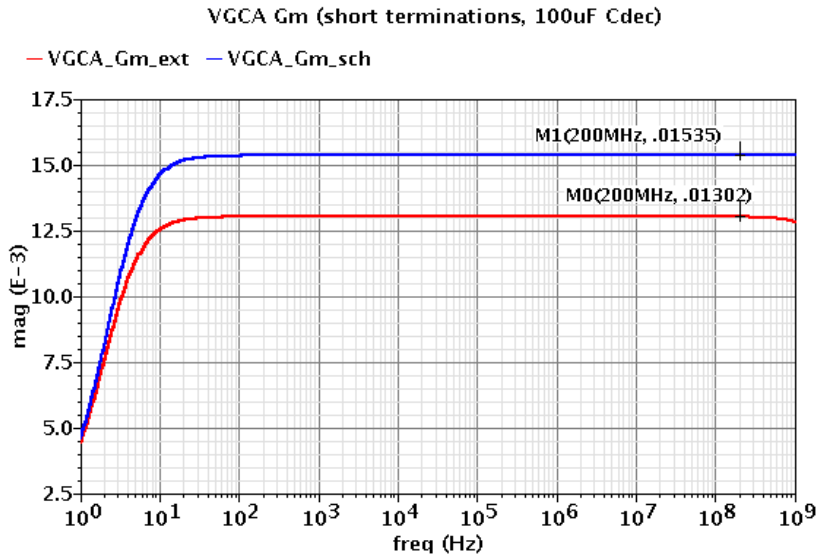

Figure 122: VGCA transconductance at highest gain state vs. frequency – short output termination – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

Figure 122 indicates that the extracted netlist exhibits a $1.4dB$ lower transconductance than that of schematic netlist, which results in the same drop in voltage gain ($-8.74dB$ vs. $-10.13dB$, refer to Figure 121).

The drop in short circuit transconductance can be explained by the 10Ω increase in input resistance of the extracted netlist compared to that of the schematic (refer to Figure 115 on page 133). Assuming the entire resistance increase is due to routing resistance at the source of VGCA NMOS devices, the drop in short circuit transconductance (and voltage gain) can be estimated. VGCA short circuit transconductance is:

$$G_m = \frac{i_{o\_sc}}{v_i} = \frac{g_{m,max}}{1 + g_{m,max}R_s} \qquad \text{(Eq. 5.4)}$$

Assuming $Rs = 0$ for the schematic netlist, and assuming identical device DC bias points before and after extraction (confirmed through DC analysis), the drop in extracted netlist short circuit transconductance is as expected (refer to Figure 122 above):

$$G_{m,sch} = g_{m,max,sch} = g_{m,max,ext} = 0.0153\ S \quad \text{(Eq. 5.5)}$$

$$G_{m,ext} = \frac{0.0153}{1 + 10 \times 0.0153} = 0.0133\ S \quad \text{(Eq. 5.6)}$$

Conclusions

The input and output common mode voltages, simulated at schematic level and post-layout parasitic extracted level are within 1%. The VGCA's input impedance has increased by about 10% after layout, a mostly resistive increase due to metal routing. The output resistance has increased by about 60Ω after layout (a 7% increase), while the output capacitance has increased from $600fF$ to about $1pF$, a 65% increase, possibly due to addition of metal to metal and metal to substrate capacitance after extraction. The current gain of the VGCA is in good agreement before and after extraction, with smaller than 5^o of constant phase shift offset from input to output introduced from post-layout parasitic extraction. NF simulation results show almost $1dB$ of increase in post-layout simulations across all gain settings, due to the increase in input resistance that leads to a drop in effective transconductance of the VGCA.

5.4.2 VGTA

DC

Figure 123 and Figure 124 below are the schematic and post-layout simulation results of the common mode input and output voltages of the VGTA.

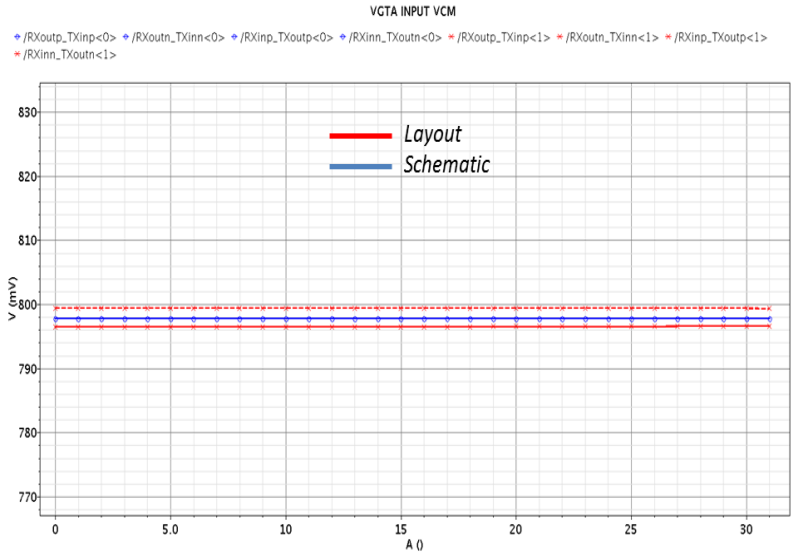

Figure 123: VGTA input common mode voltages – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

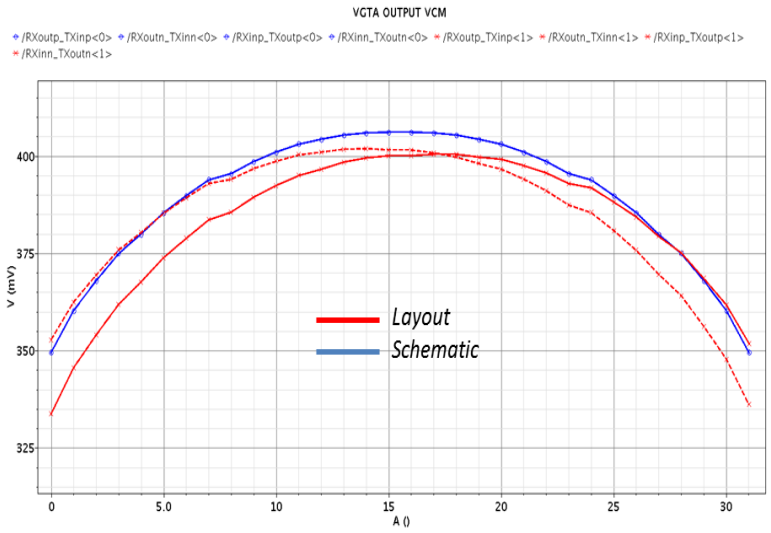

Figure 124: VGTA output common mode voltages – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

Input Impedance

The VGTA input impedance simulation results at post and pre-layout are presented in Figure 125 below:

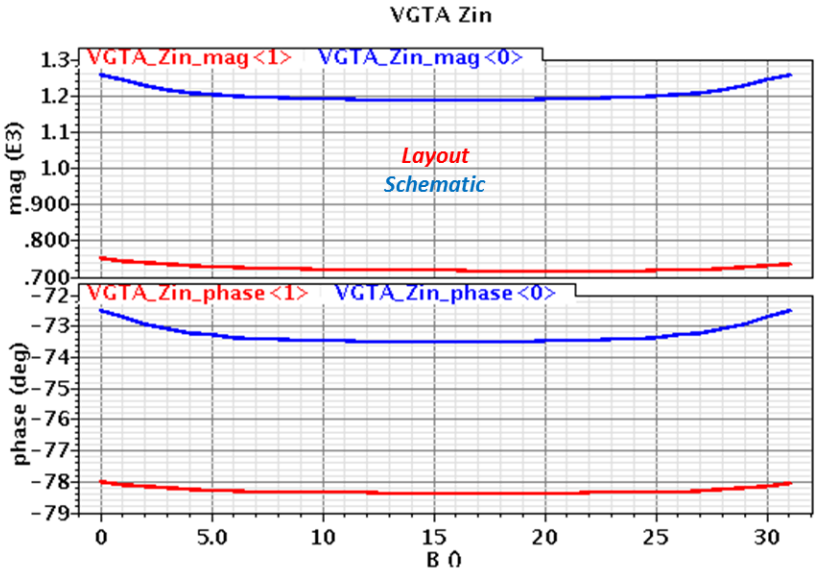

Figure 125: VGTA input impedance – default terminations – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

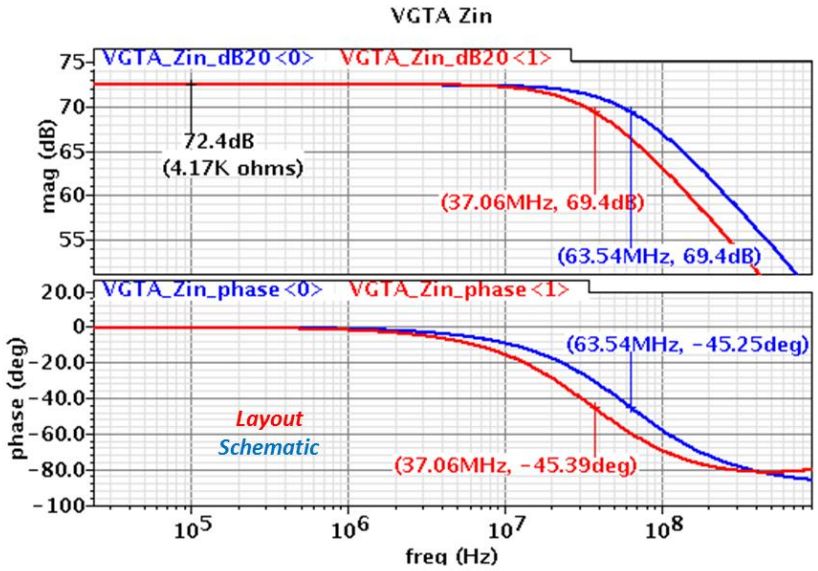

Figure 126: VGTA input impedance ($s = 0$) vs. frequency – default terminations – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

From Figure 126 above, at gain state zero, the difference can be roughly estimated:

$$R_{in_{sch}} = R_{in_{ext}} = R_{in} = 4.17K\Omega \quad \text{(Eq. 5.7)}$$

$$\omega_{3-dB,sch} = 2\pi(63.54\text{MHz}), C_{in,sch} = \frac{1}{\omega_{3-dB,sch} R_{in}} = 600fF \quad \text{(Eq. 5.8)}$$

$$\omega_{3-dB,ext} = 2\pi(37.06\text{MHz}), C_{in,ext} = \frac{1}{\omega_{3-dB,ext} R_{in}} = 1pF \quad \text{(Eq. 5.9)}$$

$$C_{ext} - C_{sch} = 400fF \quad \text{(Eq. 5.10)}$$

The increase in input capacitance can be attributed to addition of metal to metal and metal to substrate capacitance in the extracted netlist.

Output Impedance

Figure 124 is the VGTA output impedance simulations comparing the post layout results to the schematic netlist results.

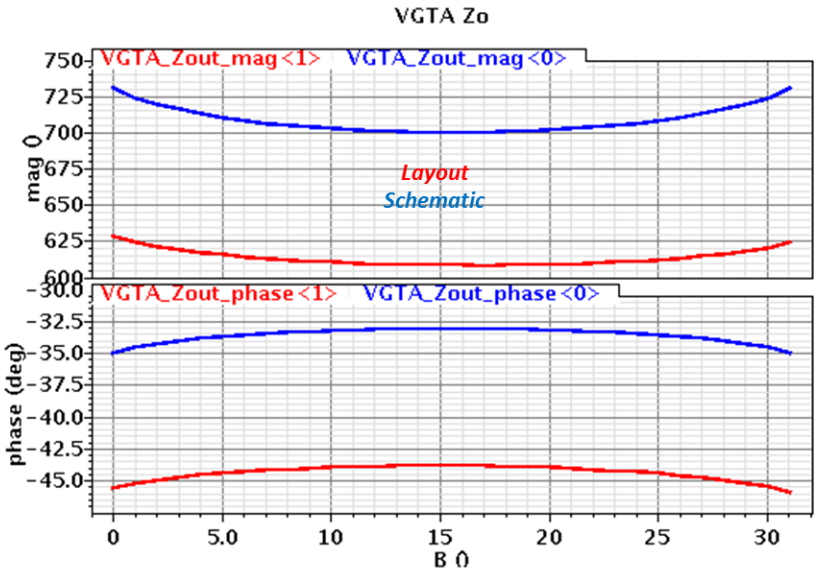

Figure 127: VGTA output impedance – default terminations – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

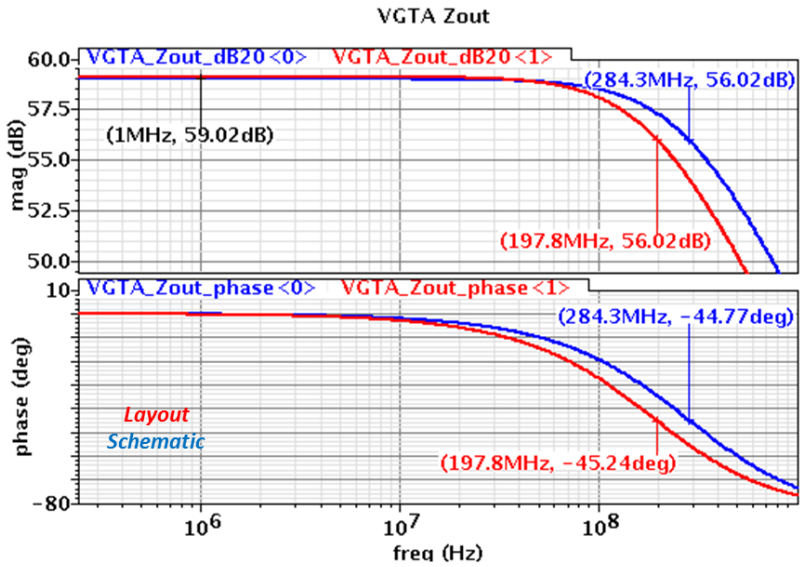

Figure 128: VGTA output impedance ($s = 0$) vs. frequency – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

For gain state zero, the difference between the parasitic extracted and schematic netlist can be roughly estimated:

$$R_{out\_sch} = R_{out\_ext} = R_{out} = 893\Omega \quad \text{(Eq. 5.11)}$$

$$\omega_{3-dB,sch} = 2\pi(284.3\text{MHz}), C_{out,sch} = \frac{1}{\omega_{3-dB,sch} R_{out}} = 625fF \quad \text{(Eq. 5.12)}$$

$$\omega_{3-dB,ext} = 2\pi(197.8\text{MHz}), C_{out,ext} = \frac{1}{\omega_{3-dB,ext} R_{out}} = 900fF \quad \text{(Eq. 5.13)}$$

$$C_{ext} - C_{sch} = 275f \quad \text{(Eq. 5.14)}$$

The increase in output capacitance can be attributed to addition of metal to metal and metal to substrate capacitance in the extracted netlist.

Transadmittance

The post layout VGTA Transadmittance is nearly identical to the schematic simulation results in magnitude. The phase, however, is significantly different at gain states 15 and 16, the smallest positive and negative states, respectively:

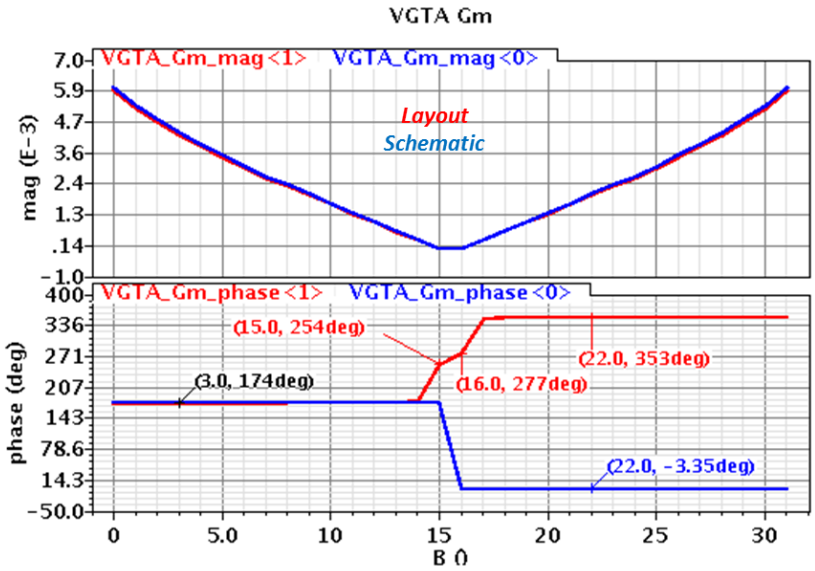

Figure 129: VGTA transadmittance – default terminations – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

One possible explanation of the phase offset is offered here. Referring to Figure 35 on page 45, we can write[22]:

$$i_1 = -\left(g_{m1} - C_{gd1}s\right) v_{in}/2 \qquad \text{(Eq. 5.15)}$$

[22] Short circuit, high frequency current of each PMOS device in Figure 35 is approximately $i = -\left(\frac{C_{big}}{C_{big}+C_{gd}} g_m - \frac{C_{big}C_{gd}}{C_{big}+C_{gd}} s\right) v_{in}/2$, where C_{big} refers to the differential AC-coupling capacitor at the VGTA output to ground. For $C_{big} \gg C_{gd}$, this expression reduces to that of (Eq. 5.15) thru (Eq. 5.18).

$$i_2 = \left(g_{m2} - C_{gd2}s\right) v_{in}/2 \quad \text{(Eq. 5.16)}$$

$$i_3 = \left(g_{m3} - C_{gd3}s\right) v_{in}/2 \quad \text{(Eq. 5.17)}$$

$$i_4 = -\left(g_{m4} - C_{gd4}s\right) v_{in}/2 \quad \text{(Eq. 5.18)}$$

$$i_{o-sc} = (i_1 + i_3) - (i_2 + i_4) \quad \text{(Eq. 5.19)}$$

Assuming: $g_{m1} = g_{m2}$ and $g_{m3} = g_{m4}$, the output short circuit current becomes:

$$i_{o-sc} = 2(g_{m3} - g_{m1}) + \left(C_{gd1} + C_{gd2} - C_{gd3} - C_{gd4}\right)j\omega \quad \text{(Eq. 5.20)}$$

At gain states 15 and 16, the real part of equation above, $2(g_{m3} - g_{m1})$, becomes small as $I_a \approx I_b$, consequently $g_{m3} \approx g_{m1}$. Now, even small mismatches between the C_{gd} of amplifying PMOS transistor pairs (M_1, M_3), (M_2, M_4) due to layout asymmetries will show up as phase offsets. Due to small magnitude of this current, system performance degradation (of VVGTA) will be minimal.

Figure 130 is the short circuit Transadmittance phase of states $14, 15, 16$ and 17 evaluated at different frequencies. It is evident that at higher frequencies and small gain states the phase deviation from the expected (ideal) values increases.

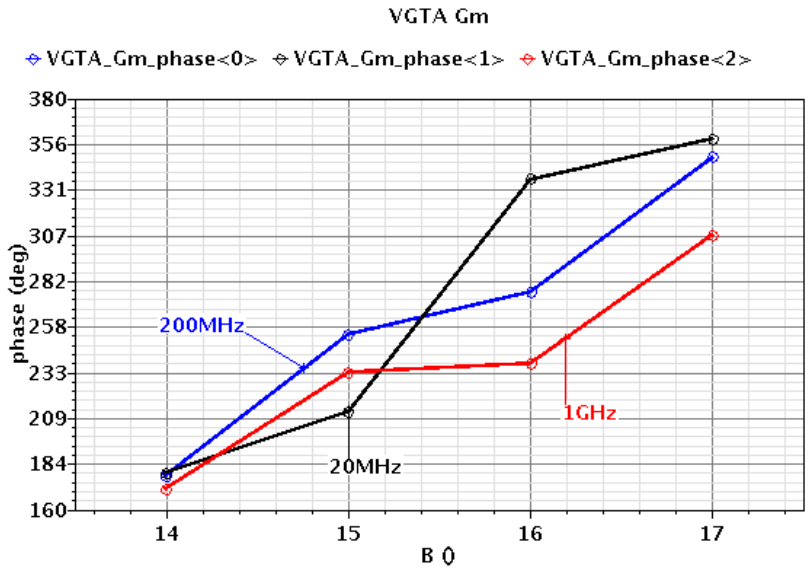

Figure 130: VGTA transadmittance phase vs. frequency for gain states 14, 15, 16, and 17

NF

Post layout NF is almost identical to the schematic level simulation results. Figure 128 is the NF simulation results comparing the post layout simulation to the schematic level simulation.

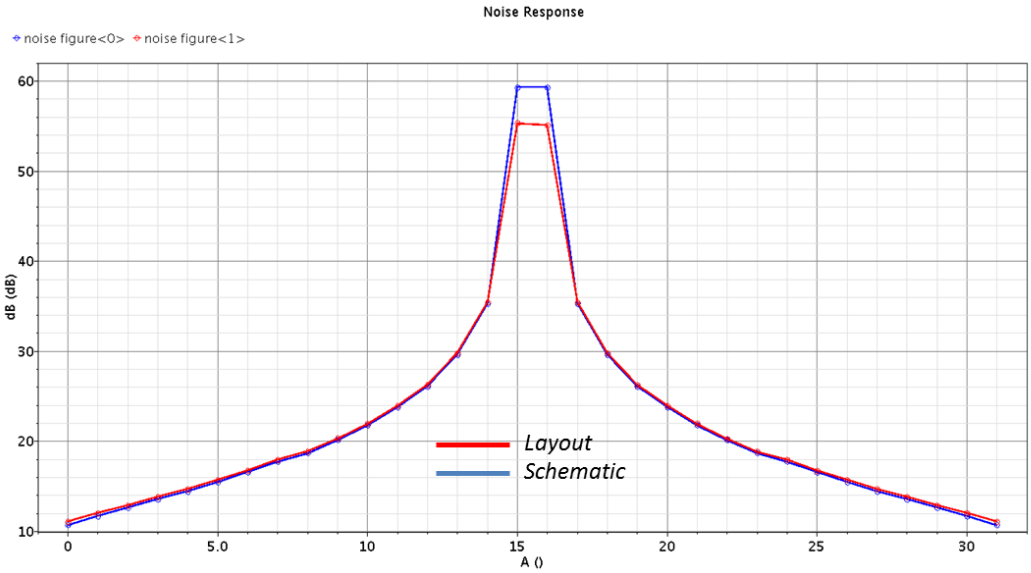

Figure 131: VGTA NF at $200MHz$ – 50Ω differential terminations – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

Conclusions

The error in the input common mode voltages in post-layout extracted simulation compared to the schematic simulation results are negligible ($< 1\%$) while the maximum error in the output common mode voltages is slightly higher at about 5%. Input resistance does not deviate from the schematic results, but the input capacitance increases by almost $400fF$, a 67% increase, in post-layout simulations likely due to addition of metal to metal and metal to substrate capacitance after extraction. Similarly, output resistance in post-layout simulations stays unchanged, while the output capacitance increases by approximately $275fF$, a 44% increase, again due to addition of coupling capacitors after schematic extraction. VGTA transadmittance magnitude is identical in post-layout and schematic simulation results, while the phase of the two minimum gain states ($s = 15,16$) in post-layout simulations deviates from the schematic simulation

results significantly ($\approx \pi / 2$) due to parasitic capacitances introduced in the parasitic extracted netlist . NF measurements are identical in post and pre-layout simulations.

5.4.3 VVGCA

VVGCA schematic versus parasitic extracted simulations are performed to identify the layout parasitic effects. Due to an schematic entry error in connecting the digital gain signals to one of the VGA blocks (greyed out VGA block in Figure 132 below), the testbench to run the post-layout versus schematic simulations of the VVGCA has been modified as shown in Figure 132.[23] The modified testbench eliminated the effect of incorrect gain of the greyed out VGA block by terminating the Quadrature input port of the VVGCA with a 50Ω source and injecting the In-phase input port with a 50Ω signal source. At the output, the differential In-phase and Quadrature ports are converted to single ended signals by use of ideal baluns. The single-ended In-phase output is then fed to an ideal, 50Ω Adder, implemented as a simple voltage controlled voltage source, while the single ended Quadrature output signal is passed through an ideal all-pass filter with a 90^o phase shift at the frequency of interest, $200MHz$, before being added to the In-phase output. The all-pass filter is implemented by an ideal op-amp in a negative feedback configuration as shown.

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[23] As complete system level schematic simulations with various gain states were not run before the design was sent for fabrication, this error was not discovered prior to fabrication. The simulation testbenches that are presented in this section are an attempt to simulate what is measured on the die.

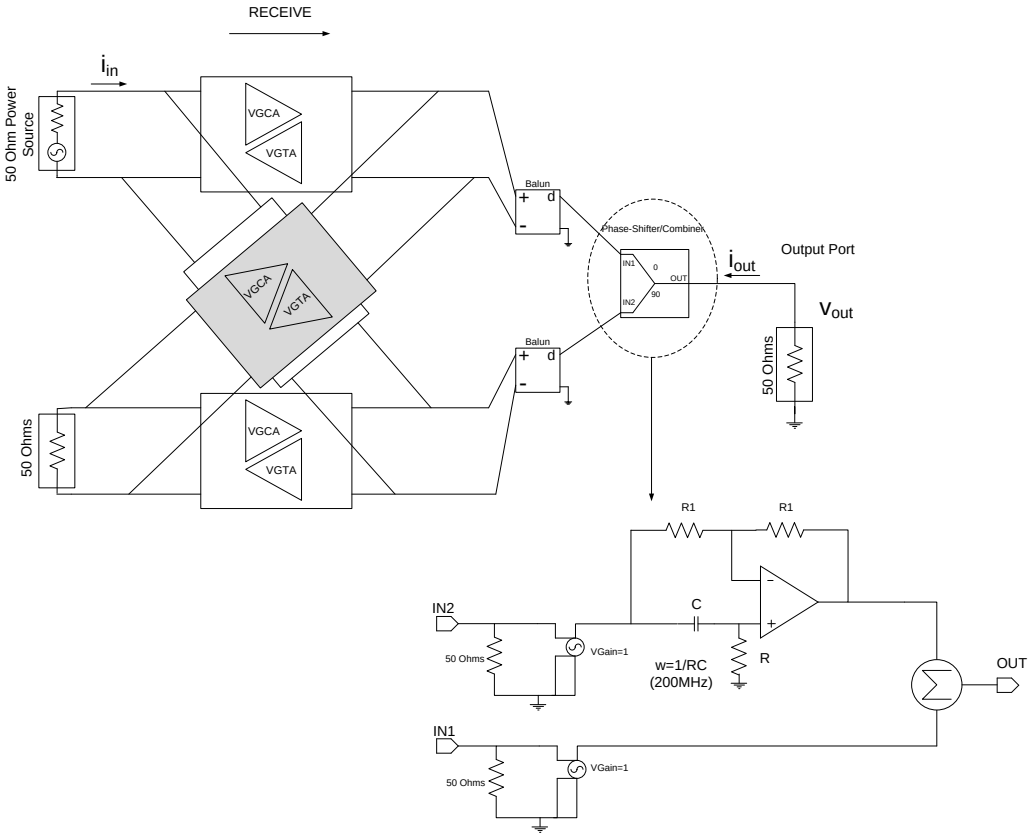

Figure 132: VVGCA simulation testbench for layout parasitic extracted vs. schematic comparison

Complex Current Gain

The complex current gain of the VVGCA with 50Ω termination obtained from the parasitic extracted netlist has a slight shift ($\cong 7°$) and magnitude drop ($\cong 0.3dB20$) at highest gain settings compared to the simulation results obtained from the schematic netlist.

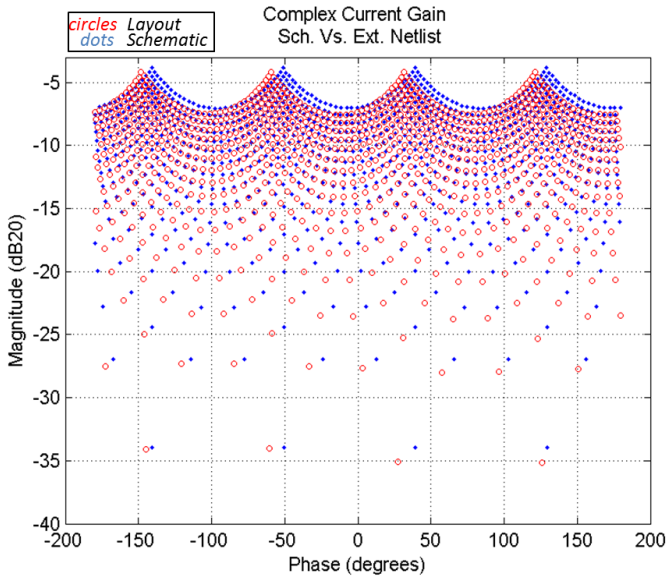

Figure 133: VVGCA complex current gain – default terminations – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

The maximum error vector between the schematic and parasitic extracted complex current gain simulation results is obtained from figure above as follows:

$$\left(\left|A_{i,ext}(A,B)\right| - \left|A_{i,sch}(A,B)\right|\right)\Big|_{worst\ case} = -1.2dB \quad \text{(Eq. 5.21)}$$

$$\left(\measuredangle A_{i,ext}(A,B) - \measuredangle A_{i,sch}(A,B)\right)_{worst\ case} = -11.8^{o} \quad \text{(Eq. 5.22)}$$

Where $A_{i,ext}(A,B)$ and $A_{i,sch}(A,B)$ refer to the post-layout and schematic simulated complex current gain at state pair (A,B). Using the magnitude and phase information obtained at each gain state, shown on plot above, the average complex current gain magnitude and phase offset between the schematic and simulation results are defined as:

$$\overline{|A_{i,error}|} \equiv \frac{1}{2^{10}} \sum_{\substack{0\le A\le 31 \\ 0\le B\le 31}} \left\{ |A_{i,ext}(A,B)|_{dB20} - |A_{i,sch}(A,B)|_{dB20} \right\} \quad \text{(Eq. 5.23)}$$

$$= -0.6dB$$

$$\overline{\measuredangle A_{i,error}} \equiv \frac{1}{2^{10}} \sum_{\substack{0\le A\le 31 \\ 0\le B\le 31}} \left\{ \measuredangle A_{i,ext}(A,B) - \measuredangle A_{i,sch}(A,B) \right\} = -1.5^{o} \quad \text{(Eq. 5.24)}$$

Where $\measuredangle A_{i,ext}(A,B)$ and $\measuredangle A_{i,sch}(A,B)$ refer to the post-layout and schematic simulated complex current gain phase at gain state (A,B), respectively. The error compensated complex current gain plot is then obtained by applying the mean error vector, obtained above, to the layout extracted complex current gain states. Figure below is the plot of the error compensated complex current gain compared to schematic simulated complex current gain.

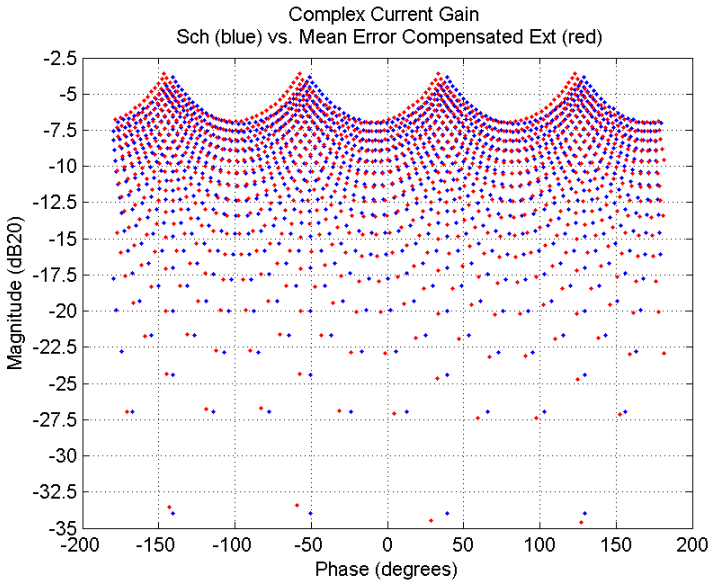

Figure 134: VVGCA complex current gain – default terminations – mean error compensated layout parasitic extracted (Red) vs. schematic (Blue) simulation results

Figure 134 is the plot of VVGCA complex current gain obtained from schematic simulation results compared to the mean error compensated extracted simulation results. Maximum magnitude and phase error between the schematic simulation results and the error compensated extracted results are:

$$\left(\left|A_{i,comp}(A,B)\right|_{dB20} - \left|A_{i,sch}(A,B)\right|_{dB20}\right)\Big|_{worst\ case} = -0.6dB \quad \text{(Eq. 5.25)}$$

$$\left(\measuredangle A_{i,comp}(A,B) - \measuredangle A_{i,sch}(A,B)\right)\Big|_{worst\ case} = -10^{o} \quad \text{(Eq. 5.26)}$$

Where

$$A_{i,comp}(A,B) \equiv A_{i,ext}(A,B) - \overline{A_{i,error}} \quad \text{(Eq. 5.27)}$$

Phase Resolution

Plots below show the comparison in phase resolution for a $1dB$ allowable gain variation between the schematic and layout extracted views:

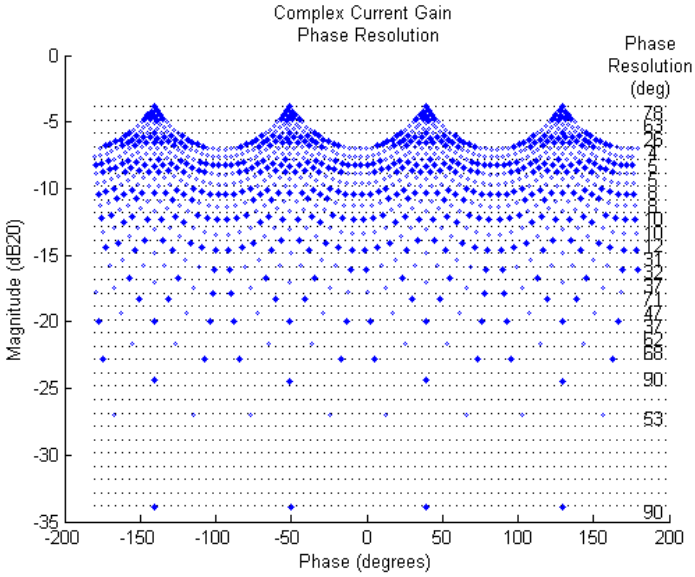

Figure 135: VVGCA complex current gain phase resolution – default terminations – schematic simulation result

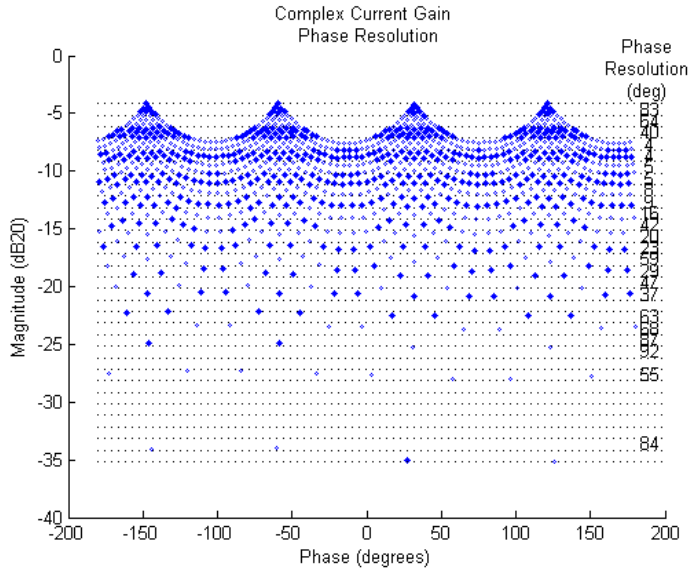

Figure 136: VVGCA complex current gain phase resolution – default terminations – layout extracted simulation result

NF

The NF is measured for two different extreme gain cases. For one case, the inner two blocks' gain is set to a maximum ($s = 0$) while the outer two blocks' gain are swept. At the other extreme the inner two blocks' gain state is changed to a minimum ($s = 15$) and the sweep is repeated. The layout extracted simulation shows a worst case $1.5dB$ error out of a $14dB$ NF.

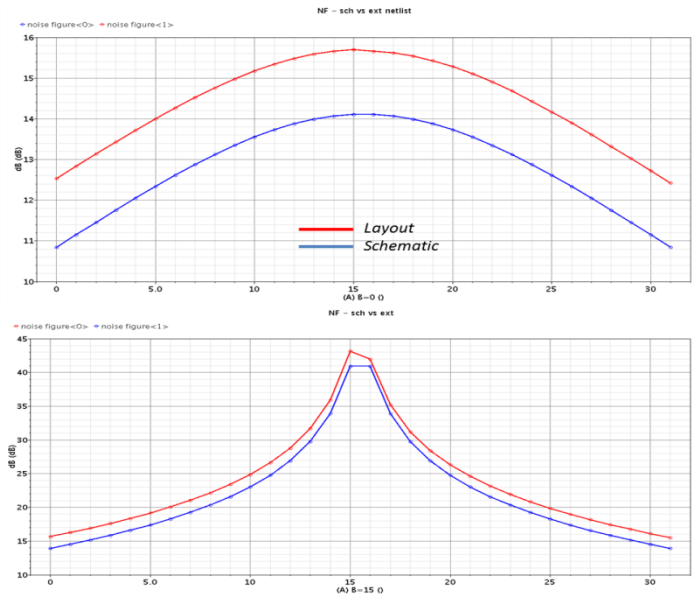

Figure 137: VVGCA NF at $200MHz$ – 50Ω differential terminations – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

Conclusions

A slight phase shift is apparent in the complex current gain versus phase plot of the VGCA is contributed to the phase shift measured in the VGCA current gain. The magnitude of the complex current gain states are close in post layout and pre-layout

simulations. The NF has increased by about $1.5dB$ in post layout simulations, which is also expected based on the post-layout NF simulation results of the VGCA.

5.4.4 VVGTA

Complex Transadmittance

The complex Transadmittance plot is presented below to compare the layout extracted and schematic simulation results. The results are nearly identical in magnitude for higher gain state combinations, with small phase offset.

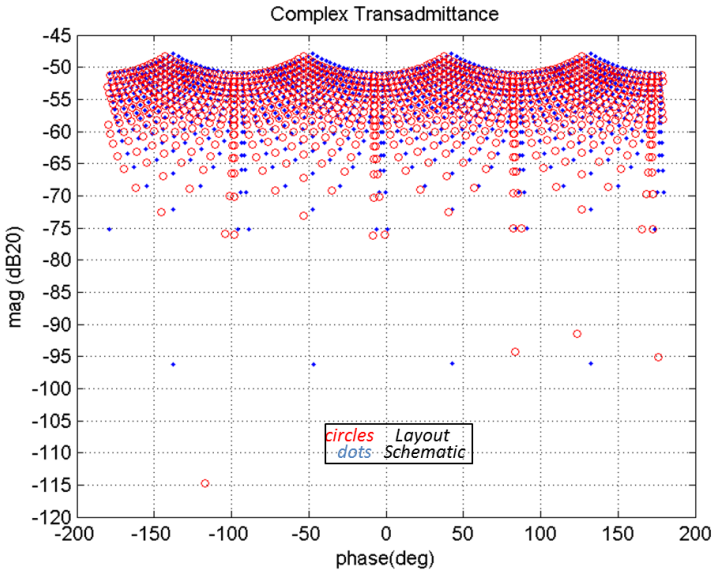

Figure 138: VVGTA complex transadmittance (relative to one siemen) – default terminations – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

Figure below offers a zoomed in view of higher gain states of Figure 138 above:

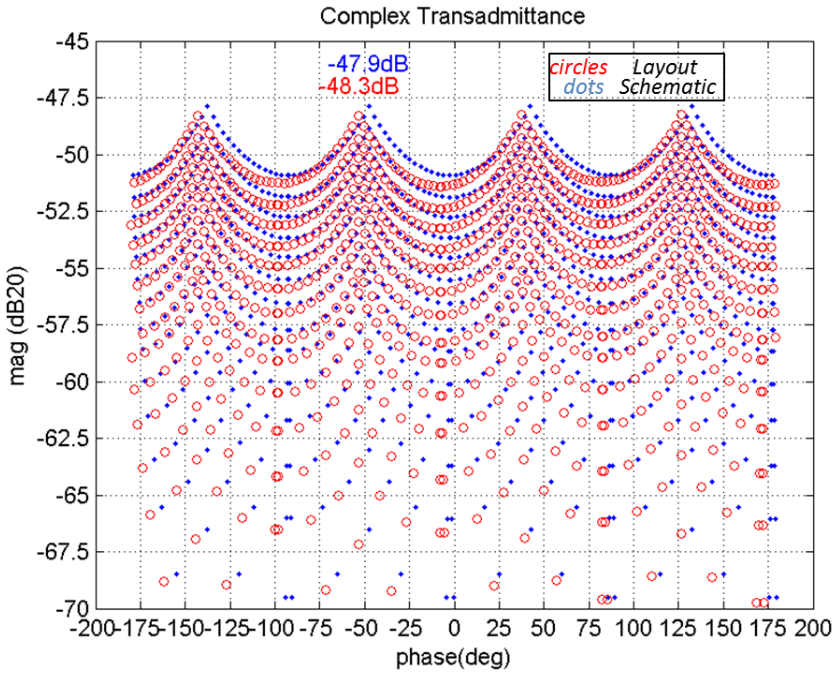

Figure 139: VVGTA complex transadmittance (relative to one siemen) – zoomed in – default terminations – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

The maximum error vector between the schematic and parasitic extracted Y_f simulation results is obtained to be:

$$\left(|Y_{f,ext}(A,B)| - |Y_{f,sch}(A,B)|\right)\Big|_{worst\ case} = -1dB \quad \text{(Eq. 5.28)}$$

$$\left(\measuredangle Y_{f,ext}(A,B) - \measuredangle Y_{f,sch}(A,B)\right)_{worst\ case} = -9.3^o \quad \text{(Eq. 5.29)}$$

Similar to the complex constant correction that was applied to the VVGCA complex current gain, an average complex transadmittance error can be computed and applied to the extracted simulation results to obtain a mean error magnitude and phase. Ignoring the smallest magnitude transadmittance states, $\left(|Y_f| < -90dB20\right)$, the average complex transadmittance error is defined and calculated:

$$\overline{|Y_{f,error}|} \equiv \frac{1}{2^{10}} \sum_{\substack{0\le A\le 31\\ 0\le B\le 31}} \left\{ |Y_{f,ext}(A,B)|_{dB20} - |Y_{f,sch}(A,B)|_{dB20} \right\} = -0.4dB \quad \text{(Eq. 5.30)}$$

$$\overline{\measuredangle Y_{f,error}} \equiv \frac{1}{2^{10}} \sum_{\substack{0\le A\le 31\\ 0\le B\le 31}} \left\{ \measuredangle Y_{f,ext}(A,B) - \measuredangle Y_{f,sch}(A,B) \right\} = -1.6^o \quad \text{(Eq. 5.31)}$$

Figure below is the plot of the error compensated complex transadmittance compared to schematic simulated complex transadmittance.

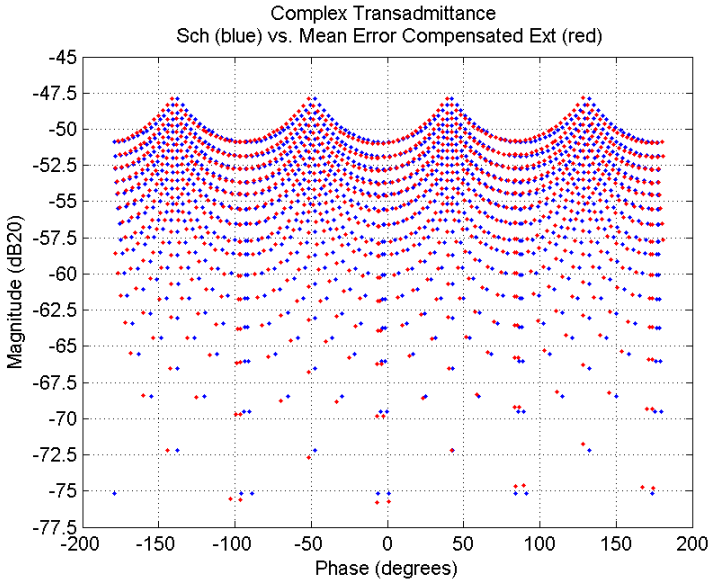

Figure 140: VVGTA complex transadmittance (relative to one siemen) – default terminations – mean error compensated layout parasitic extracted (Red) vs. schematic (Blue) simulation results

Maximum magnitude and phase error between the schematic simulation results and the error compensated extracted results are:

$$\left(|Y_{f,comp}(A,B)|_{dB20} - |Y_{f,sch}(A,B)|_{dB20} \right)\Big|_{worst\ case} = -0.6dB \quad \text{(Eq. 5.32)}$$

$$\left(\measuredangle Y_{f,comp}(A,B) - \measuredangle Y_{f,sch}(A,B) \right)_{worst\ case} = -7.7^o \quad \text{(Eq. 5.33)}$$

Where

$$Y_{f,comp}(A,B) \equiv Y_{f,ext}(A,B) - \overline{Y_{f,error}} \qquad \text{(Eq. 5.34)}$$

Phase Resolution

Plots below show the comparison in phase resolution for a $1dB$ allowable gain variation between the schematic and layout extracted views:

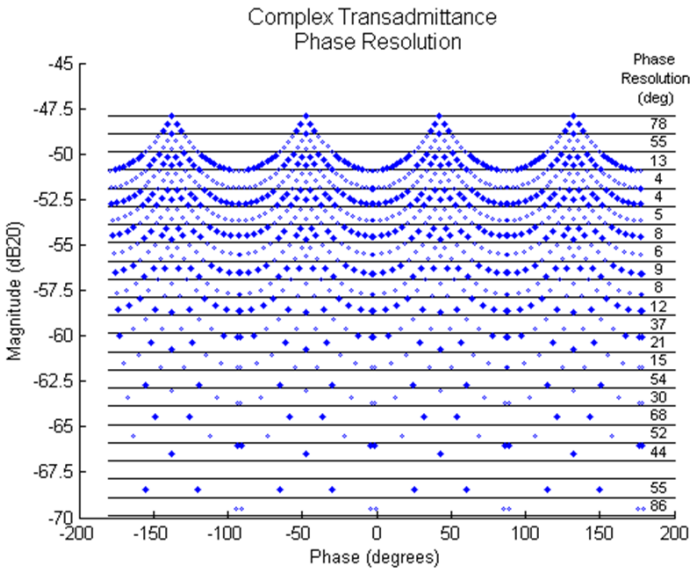

Figure 141: VVGTA complex transadmittance (relative to one siemen) phase resolution – default terminations – schematic simulation result

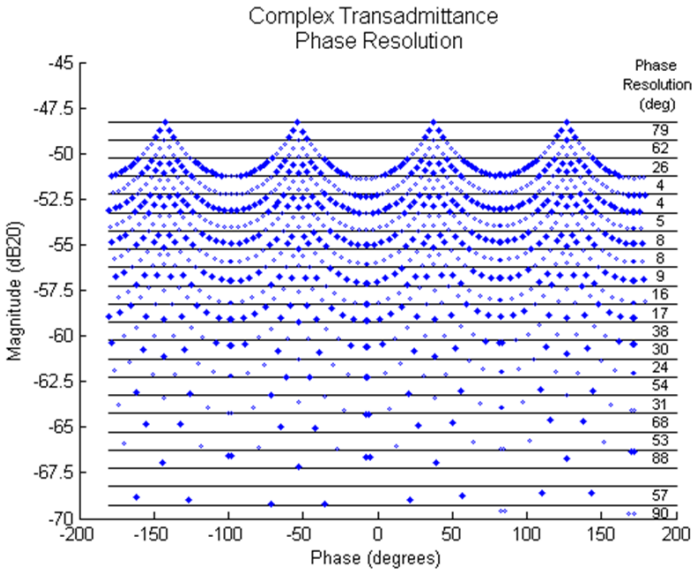

Figure 142: VVGTA complex transadmittance phase resolution – default terminations – layout parasitic extracted simulation result

NF

The VVGTA NF simulation results comparing parasitic extracted with schematic netlist is presented in Figure 143 below. The parasitic extracted simulation shows about $1dB$ of NF degradation. There is also an asymmetry in NF at the smallest gain setting pair ($B = 14$ and 15 when $A = 0$), due most likely to the combination of layout mismatches and small signal levels at the output for these states that amplifies the mismatch effect in NF measurement. It is noted that the extremely small signal level at the output implies that the VVGTA, for all practical purposes, will not be operated at these gain states.

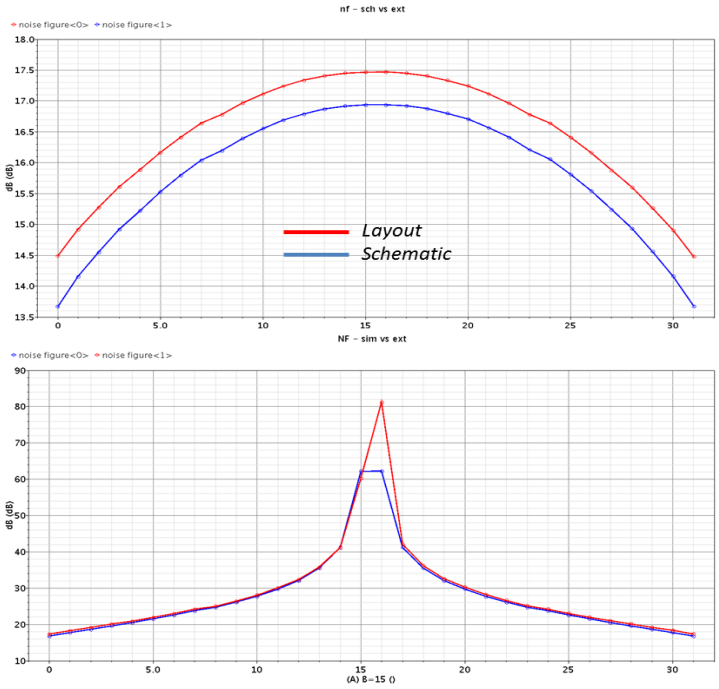

Figure 143: VVGTA NF – 50Ω differential terminations – layout parasitic extracted (Red) vs. schematic (Blue) simulation results

Conclusions

Complex Transadmittance results of post-layout and schematic simulation are in close agreement. The NF increases slightly, by less than $1dB$, in post-layout simulations.

CHAPTER 6

POST-FABRICATION MEASUREMENTS

Post fabrication measurements were done on bare dies. High frequency signals were probed using customized $40GHz$ GSSG and GSSG-GSSG probes on the $115um$ by $115um$ internal bond pads with $150um$ pitch as shown on Figure 109 on page 127. The bond pads along the edges of the die used for wire-bonding are $150um$ by $150um$ with $250um$ pitch. All bond pads are aluminum. Figure 144 below shows the probe station setup:

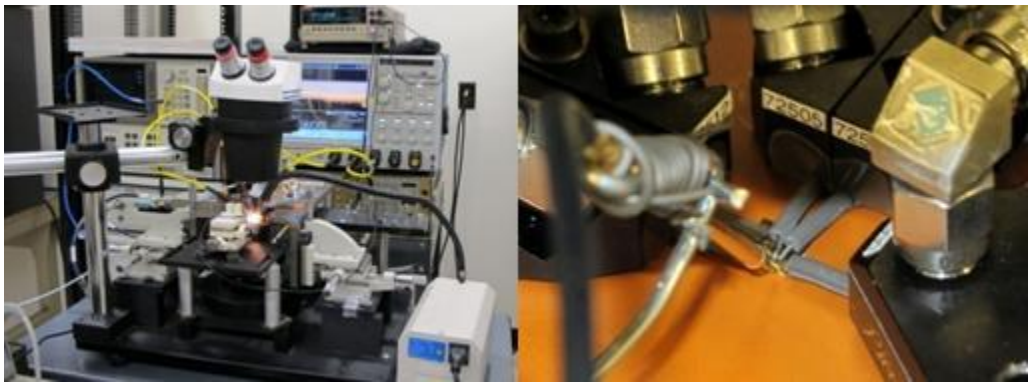

Figure 144: Lammda Lab probe station [13]

DC power supplies, power supply by-pass capacitors, and DC gain control switches are implemented on a PCB. The die was soldered to the board and on-chip DC bond pads were wire bonded to the appropriate pins on the PCB. The PCB image is provided below:

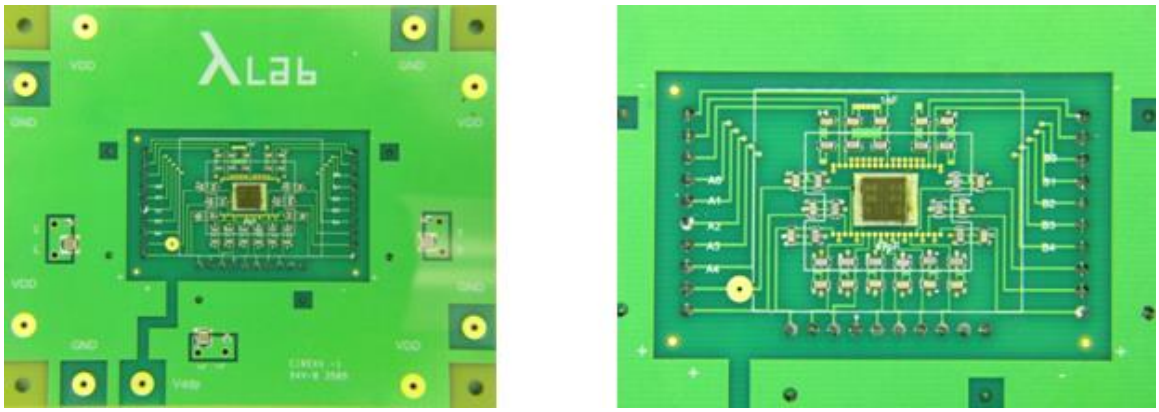

Figure 145: PCB used for post-fabrication measurements [13]

Figure 146 below shows the microscopic view of the entire die. [13] Block one and two are the VVGAs, block three consists of three versions of VGA: receive only VGA block (VGCA), bi-directional VGA, and transmit only VGA block (VGTA). Items four and five are the $115um^2$ high frequency probe bond pads and $150um^2$ bond pads used for wire bonds, respectively.

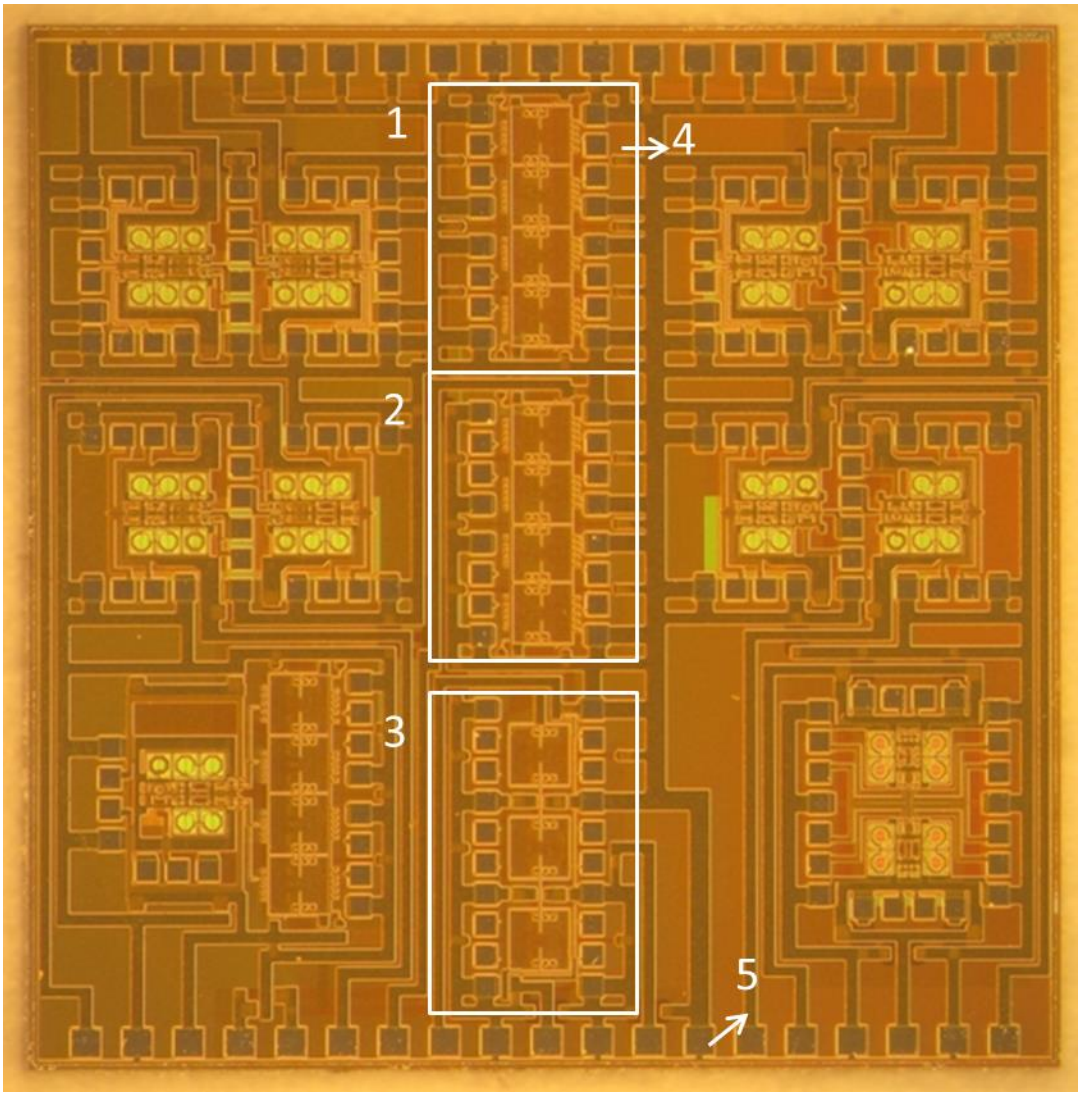

Figure 146: Full Die View: 1,2-VVGA 3-VGA (RX only), VGA, VGA(TX Only) 4- $115um \times 115um$ bond pads with $150um$ pitch 5- $150um \times 150um$ bond pads with $150um$ pitch [13]

Post-fabrication measurements were performed on the VGCA, VGTA, VVGCA, and VVGTA and are presented in the following sections. The IF frequency of interest, as it has appeared in the simulation results so far in the thesis, is $200MHz$. Measurements at

$200MHz$, however, showed significant signal attenuation[24]. This forced the measurements to be taken at $20MHz$ instead. The reason for this attenuation was not revealed despite extensive post-layout simulations. The reason for choosing $20MHz$ for measurements was that at this frequency the measurement results corresponded closely to simulation results. All VGAs experienced this attenuation. The measurement results and corresponding simulation results depicted in this chapter all correspond to signal frequency of $20MHz$.

6.1 VGA: Measurements and Setup

VGA measurement setup is shown in Figure 147 below. Signal generator generates a 50Ω, $20MHz$ signal. The signal is then fed to a $3dB$ power splitter with its one output connected to the primary coil input of a surface mount RF transformer[25] for single ended to differential conversion, and the other to the oscilloscope to monitor the input signal phase relative to the output.

---

[24] Near noise floor

[25] The insertion loss of the RF transformer is $0.65dB$ at $15.5MHz$ for typical performance according to its datasheet. This value was used in baluns for all layout parasitic extracted simulation results that are compared to post-fabrication measurement results.

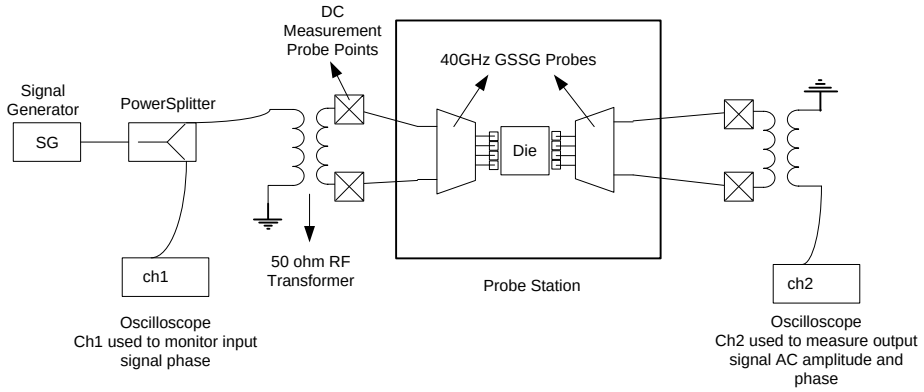

Figure 147: VGA measurement setup for DC common mode and AC signal amplitude and phase measurements

GSSG probes are used to probe the input and output differential signals. At the output, the RF transformer is again used for differential to single ended conversion.

The DC common mode voltages are probed directly on the transformer for all different gain states, as shown on the figure above. The average peak to peak value of the $20MHz$ output voltage is measured on the oscilloscope, along with the phase difference between the input signal (power splitter output) and the output signal. This phase difference is reported as the phase in the proceeding sections.

NF measurement setup is shown in Figure 148 below. Same transformer and GSSG probes are used and the signal generator is replaced by a noise source. A NF Meter is used to measure system NF.

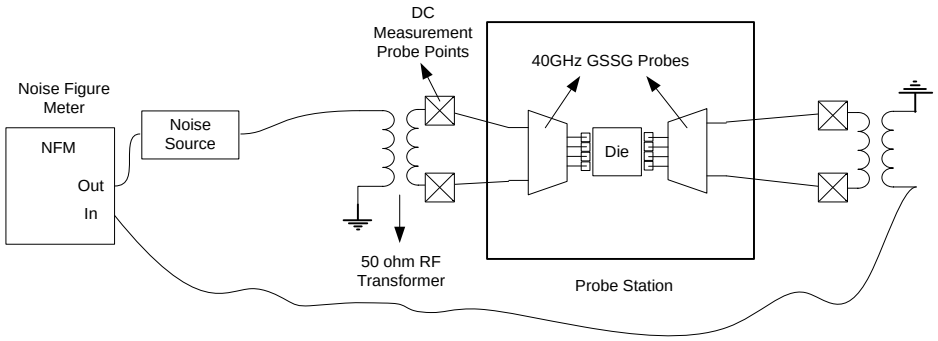

Figure 148: VGA measurement setup for NF measurements

6.2 VGCA Measurements Results

6.2.1 DC

Figure 149 below shows the input and output common mode voltages of the VGA at receive mode of operation for all gain states and the comparison to the layout parasitic extracted simulation results.

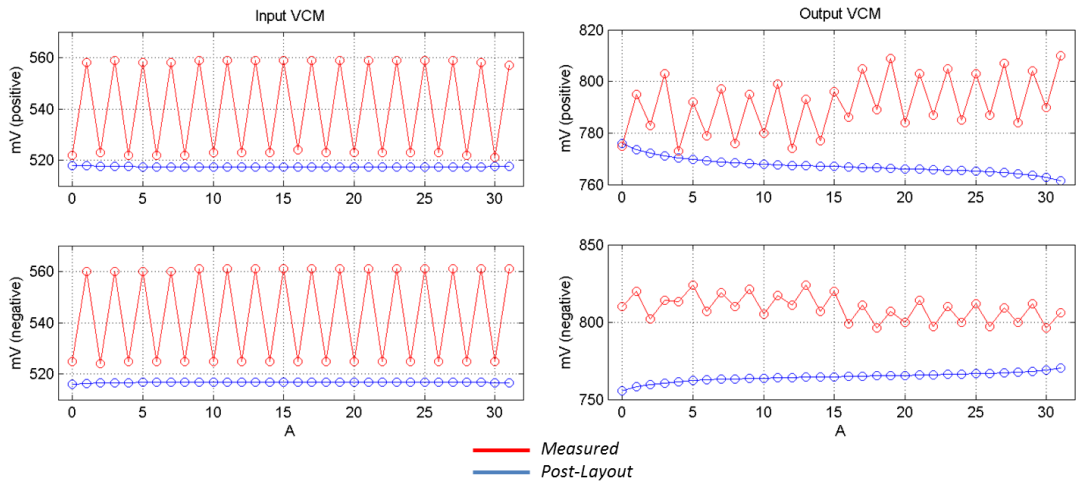

Figure 149: VGCA common mode voltages – post-fabrication measurement results (Red) vs. layout parasitic extracted simulation results (Blue)

It is noted that the input common mode voltage varies by about $40mV$ at every LSB change, and the output common mode voltage also exhibits oscillations at every LSB. Input common mode variations with LSB are not reproducible in simulations and a root cause is not yet determined. However, part to part input common mode variations due to process and mismatch variations, and output common mode oscillations due to ineffective common mode regulation may be expected and explained here:

Process and mismatch dependent variation in the input common mode voltage across process corners and temperature is expected. Relevant portion of the VGA, pertaining to input common mode, is repeated here for convenience:

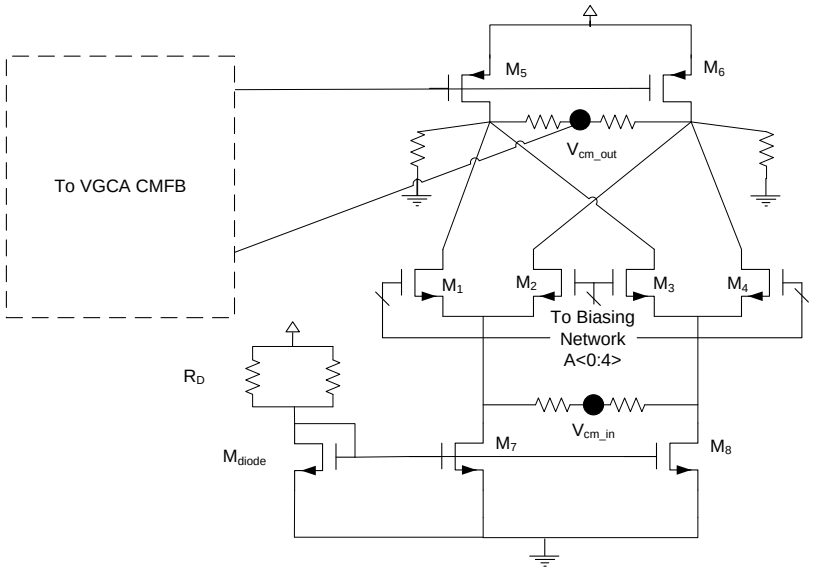

Figure 150: VGCA simplified circuit diagram

The input common mode voltage, V_{cm_in}, as apparent from figure above, is set by the gate to source voltage drop that is required to support the drain currents of transistors M_1 thru M_4. V_{cm_in},, therefore, will vary with transistor threshold voltage variations, absolute value of the drain current of current mirroring transistor, M_{diode} (dependent on

transistor threshold voltage value and absolute value of R_D), and current gain offset between M_{diode} and current sink transistors M_7 and M_8 due to device mismatches. Figure below shows the input common mode voltage variations of the schematic view of the VGCA across the two extreme process corners, FF and SS, and temperature corners, -40° and 125°.

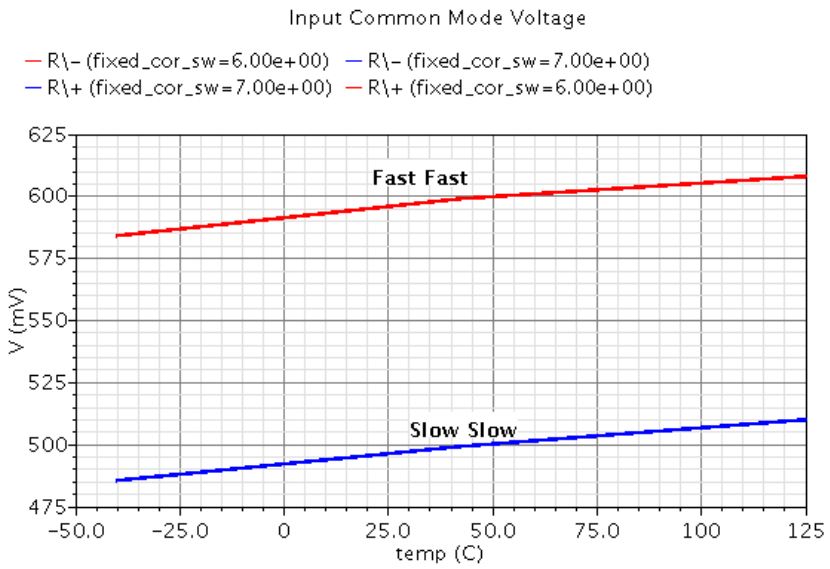

Figure 151: VGCA input common mode voltage variation across extreme device and temperature corners: slow-slow-cold, slow-slow-hot, fast-fast-cold, fast-fast-hot – schematic simulation result

As seen on the figure, process and temperature variations can cause significant deviation of the input common mode voltage from its nominal value of $550mV$. Monte-Carlo simulations including the process and mismatch variations show a standard deviation of almost $15mV$ for the input and output common mode voltages. However, variations of the common mode voltage due to change in LSB are not reproducible in

simulations. Figures below shows the results of the input and output common mode voltages, respectively, for 100 statistical runs with process and mismatch variations.

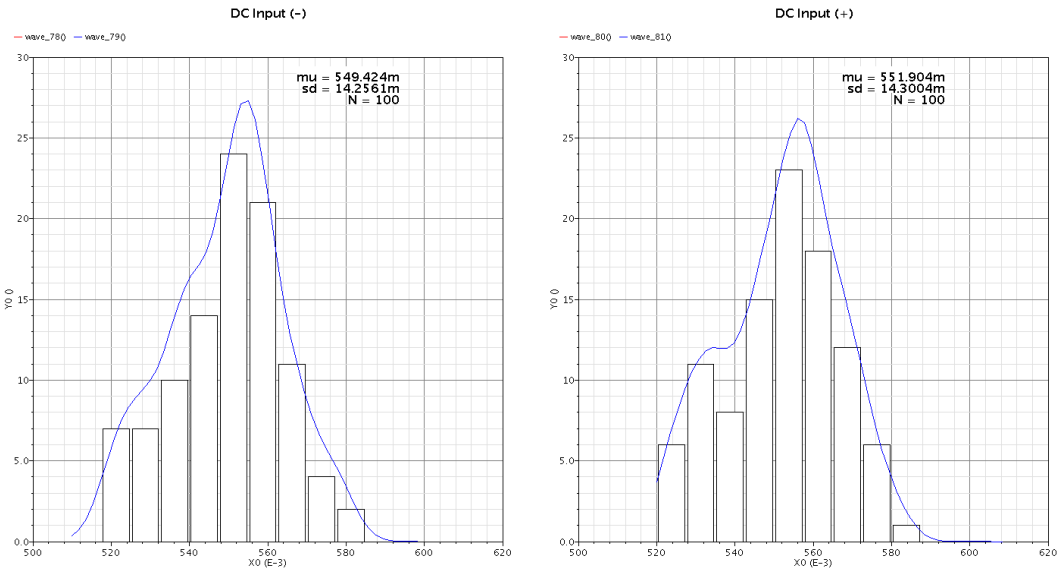

Figure 152: VGCA input common mode voltage variation with mismatch and process corners– schematic simulation result

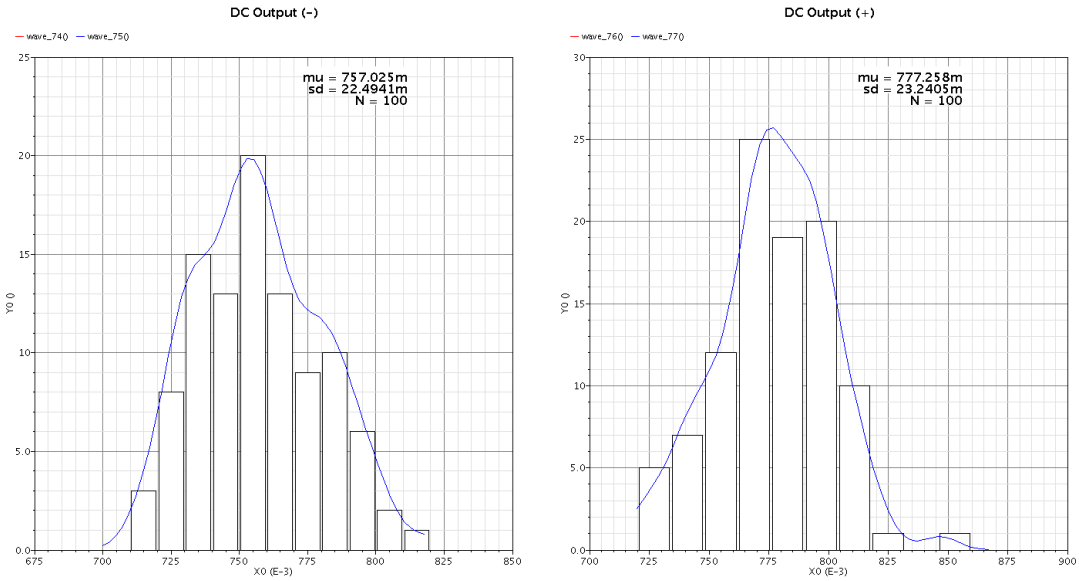

Figure 153: VGCA output common mode voltage variation with mismatch and process corners – schematic simulation result

Monte Carlo simulations, however, do not suggest any correlation between the input common mode voltage and VGCA gain states. Figure below depicts the input common mode voltage values for 10 Monte Carlo runs that include mismatch and process variations for the first five gain states ($A = 0,1,2,3$ and 4). No dependence between the LSB value and value of common mode input voltage is observed.

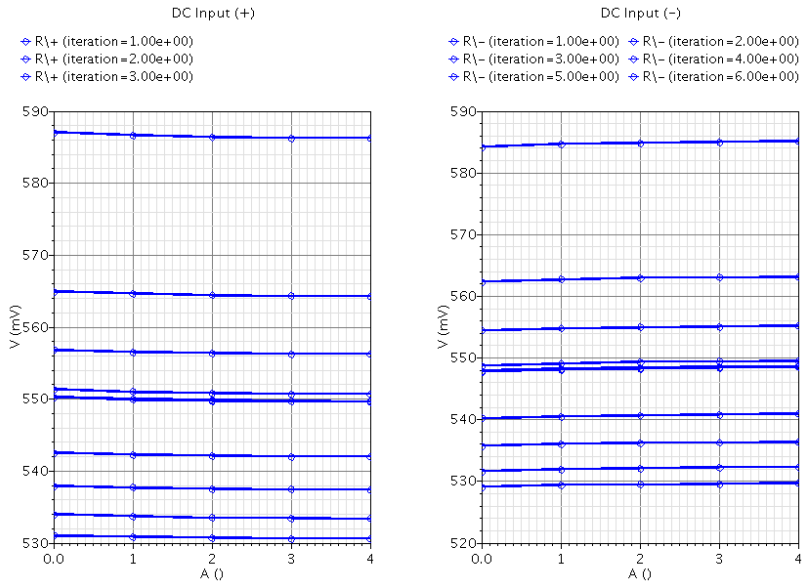

Figure 154: VGCA input common mode voltage variation with mismatch and process corners at gain states $0,1,2,3$ and 4 – schematic simulation result

Conclusion

Input common mode voltage measurements indicate a $40mV$ variation at each LSB. This phenomenon, as stated earlier, is not reproducible in simulations and a root cause was not determined. Simulation results, however, indicate that variation in input common mode over process and temperature corners can be as high as $120mV$, even though simulation results do not suggest any dependence of the input common mode

voltage on gain states, specifically any dependence on every LSB change in the gain control word. Output common mode voltage of the VGCA also exhibits some variation on every LSB change of the control word, however this change is limited to less than $20mV$ (2.5%).

6.2.2 AC

Figure 155 below shows the peak to peak amplitude and phase of the output voltage of the VGCA measured as with the testbench shown on Figure 147 on page 167[26].

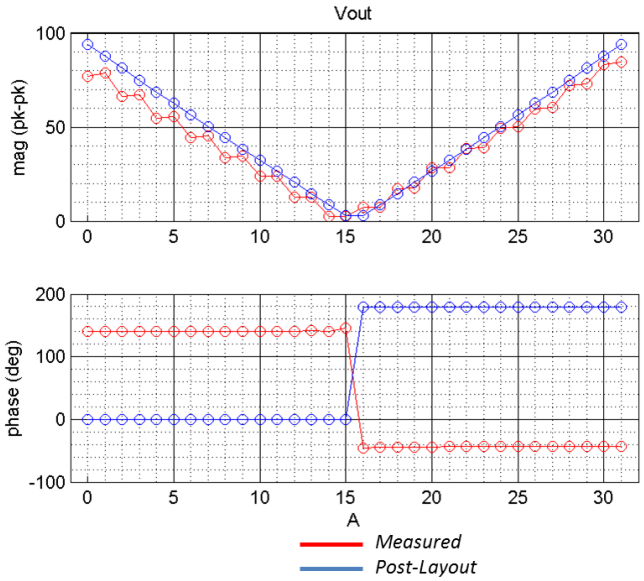

Figure 155: VGCA output voltage amplitude and phase – post-fabrication measurement results (Red) vs. layout parasitic extracted simulation results (Blue)

[26] The insertion loss of the RF Transformer, $0.65dB$ as stated in its datasheet, has been included in the simulation results.

The phase offset between the measured and simulated results is a testbench artifact. The phase is measured by comparing the phase offset between oscilloscope $ch1$ and $ch2$ (see Figure 147 on page 167). $Ch2$ signal at the output, includes some phase shift introduced by the Balun, and the signal at Channel 1 includes some phase shift introduced by the power splitter, together amounting to about 150^o. The 180^o phase shift between the positive and negative gain states, however, is expected and apparent from the measurement results.

The step-like behavior of the measured output signal magnitude suggests a 4-bit resolution of the gain range, indicating that the LSB controlling the gain is not functioning as expected. This behavior can be explained if the LSB bit were always ON:

At gain states between 0 and 15, an always ON LSB will reduce the output voltage magnitude of even states to those of the odd states therefore creating a step-like behavior in output voltage magnitude plot where the magnitudes of even states correspond to that of odd states and are lower than expected (for example, voltage magnitude at state 0 will equal the magnitude at state 1, and voltage magnitude at state 2 will equal that of state 3, therefore voltage magnitudes at states 0 and 2 are smaller than expected). For states 16 thru 31, an always ON LSB will increase the output voltage magnitude of the even states to those of the odd states, therefore creating a step-like behavior in the output voltage magnitude plot where the output voltage magnitudes of even states correspond to that of odd states and are greater than expected (for example, voltage magnitude at state 16 will equal the magnitude at state 17, and voltage magnitude at state 18 will equal that of state 19, therefore voltage magnitudes at states 16 and 18 are greater than expected). This

behavior is observed in Figure 155 above. To confirm this hypothesis, schematic simulation results with the LSB bit set to ON for all gain states is presented in figure below in comparison with the default behavior.

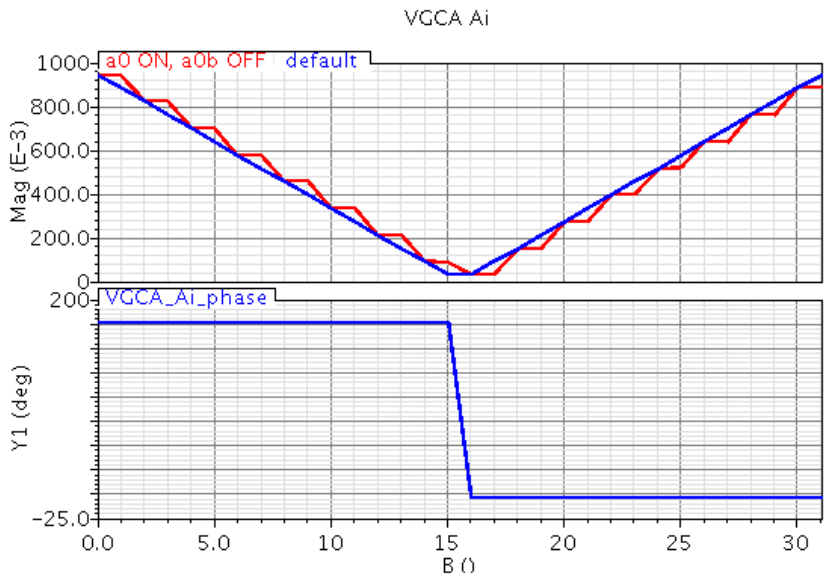

Figure 156: VGCA current gain with LSB set to high for all gain states (Red) vs. the default case (Blue). Odd negative gain states (here states 0 to 15) have higher than expected A_i and odd positive gain states (here states 16 to 31) experience a drop in A_i[27] - default terminations – schematic simulation result

Figure below is the VGCA output peak to peak voltage for all 32 gain states for 10 Monte Carlo simulations with mismatch and process variations. As seen from this plot,

[27] In the text it was explained that even states from 0 to 15 experience a drop, and even states from 16 to 31 experience a rise in A_i. This is not contradictory to the results shown on this figure, as the polarity of the states in this figure are reversed.

slight variations in slope and amplitude are expected from part to part, but the non-linear small signal behavior measured in the lab is not reproduced.

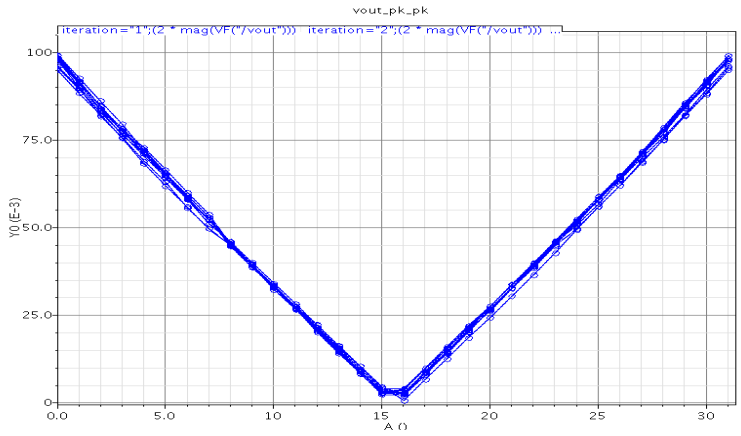

Figure 157: VGCA output voltage magnitude vs. gain states with process and corner variations – schematic simulation result

Monte Carlo simulations show a $15mV$ standard deviation of the common mode voltages from part to part based on modeled mismatches and process corners, but the results of Monte Carlo simulations do not predict the non-linear small signal behavior observed in measurements.

Conclusion

AC voltage measurements at VGCA output indicate that the LSB bit is not functioning as expected. AC simulation results match measurement patterns with the LSB bit set to ON at all gain states. Although the AC behavior is somehow reproducible with this hypothesis, it is unlikely that the LSB bit is completely ineffective, as DC variations at the input were observed at every LSB change. Consequently, the hypothesis

for the LSB dependent VGCA small signal behavior is not confirmed with a high degree of confidence.

6.2.3 Linearity

The linearity of the system was measured in lab by increasing the input source available power and observing the $1dB$ compression point. The measurement was taken at the highest gain setting and the measurement setup was identical to Figure 147 on page 167. Power gain was calculated as follows:

$$P_{delin} = P_{ch1} \quad \text{(Eq. 6.1)}$$

$$P_{delin-dBm} = 10log10\left(\frac{\left({}^{1}/_{2}\right)\left(v_{ch1-pkpk}/2\right)^{2}}{(50\Omega)(1mW)}\right) \quad \text{(Eq. 6.2)}$$

$$P_{delL-dBm} = 10log10\left(\frac{\left({}^{1}/_{2}\right)\left(v_{out-pkpk}/2\right)^{2}}{(50\Omega)(1mW)}\right) \quad \text{(Eq. 6.3)}$$

$$G_P = (P_{delL-dBm} - P_{delin-dBm})dB \quad \text{(Eq. 6.4)}$$

Figure 158 shows the VGCA's $1dB$ compression point.

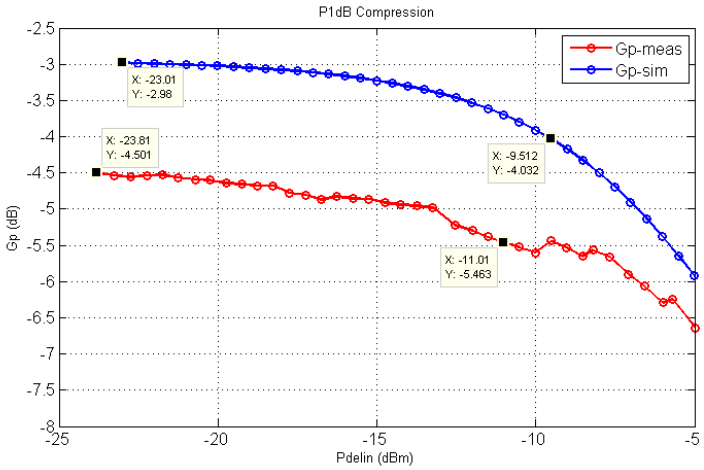

Figure 158: VGCA $1dB$ compression point – post-fabrication measurement results (Red) vs. layout parasitic extracted simulation results (Blue)

The measured and simulated results of $1dB$ compression point are close. The decrease in transducer gain in measurements is largely due to the smaller gain than expected at gain state 0, where a mal-functioning of LSB is hypothesized and explained in the previous section. Estimating the difference between peak to peak voltages of the measured and extracted VGCA from Figure 155 yields in a similar difference in output power observed in figure above ($1.5dB$ measured):

$$20log10\left(\frac{v_{out\_ext-pkpk}}{v_{out\_meas-pkpk}}\right) \cong 20log10\left(\frac{100mV}{80mV}\right) = 1.9dB \qquad \text{(Eq. 6.5)}$$

6.2.4 NF

NF measurements along with the parasitic extracted simulation results are shown in Figure 159 below:

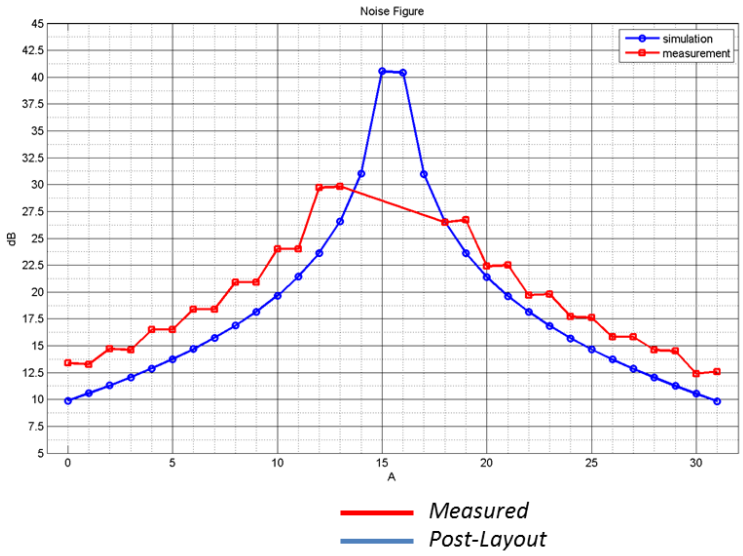

Figure 159: VGCA NF at $200MHz$ – post-fabrication measurement results (Red) vs. layout parasitic extracted simulation results (Blue)

The measured NF is about $2.5dB$ larger than the parasitic extracted simulation shows. The NF pattern is consistent with the peak to peak output voltage measurements, where the LSB did not seem to affect the AC signal power. At lower gain settings, due to small output signal, the NF meter did not produce accurate results.

The increase in NF can be explained if the slope decrease in the post-fabricated output voltage compared to post-layout simulations is contributed entirely by a decrease in the effective transconductance of the NMOS input stage. The effective transconductance of the CG stage is a strong function of the parasitic input resistance seen at the source, as was the case in schematic versus post-layout extracted simulation results that resulted in degradation of NF by $1dB$ (section 5.4.1, page 136). An increase in R_s due to cable resistance, for example, compared to post-layout resistance, can cause a 20% drop in effective transconductance of the VGCA. This is explained below:

Assuming large output resistance relative to the 50Ω channel resistance of the oscilloscope, the maximum output voltage is:

$$v_{out} = -v_{in} g_{m,\max} 50 \qquad \text{(Eq. 6.6)}$$

Where:

$$g_{m,\max} = g_{m1} - g_{m2} \; when \; g_{m2} = 0$$

The maximum peak to peak output voltage of the VGCA at post-layout simulation and post-fabricated measurement, as depicted in Figure 155, is:

$$v_{out,pk-pk,sim} \approx 100mV$$

$$v_{out,pk-pk,meas} \approx 80mV$$

7% of this drop in effective transconductance can be accounted for by the mal-functioning of the LSB. Referring to (Eq. 2.13) on page 22, transconductance degradation due to the LSB bit being ON at state 0 is:

$$1 - \frac{\sum_{i=0}^{4} 2^i (a_i - \bar{a_i})\big|_{s=0,default}}{\sum_{i=0}^{4} 2^i (a_i - \bar{a_i})\big|_{s=0,LSB=ON}} = 1 - \frac{29}{31} \cong 7\% \qquad \text{(Eq. 6.7)}$$

The remainder 13% increase can be explained as due to an increase in source resistance, similar to the degradation in NF that was observed in layout extracted simulations of the VGCA compared to the schematic results. According to Figure 122 on page 139, the effective transconductance of the extracted VGCA at maximum gain state of 0 is:

$$g_{m\_extracted} = 13mS$$

According to (Eq. 5.4) on page 139, an approximately 10Ω increase in source resistance in measurements in addition to the malfunctioning of the LSB can account for the 20% drop in the measured transconductance. Assuming a 20% drop in transconductance, the expected increase in NF can be approximated:

$$\overline{V_{n,in}^2} = 8kT\frac{2}{3}\frac{g_{m,\max} + g_{m,\mathrm{M5,M6}}}{{g_{m,\max}}^2}\ ^{28} \qquad \text{(Eq. 6.8)}$$

Where $g_{m,\mathrm{M5,M6}} \approx 7mS$[29] is the transconductance of the PMOS current source devices at the output of the VGCA. The difference between the input referred noise of the post-layout and fabricated measurements is then equal to:

$$\frac{\overline{V_{n,in,sim}^2}}{\overline{V_{n,in,meas}^2}}dB = 10\log\left(\frac{\frac{g_{m,\max,\mathrm{sim}} + g_{m,\mathrm{M5,M6}}}{{g_{m,\max,\mathrm{sim}}}^2}}{\frac{\frac{4}{5}g_{m,\max,\mathrm{sim}} + g_{m,\mathrm{M5,M6}}}{\left(\frac{4}{5}g_{m,\max,\mathrm{sim}}\right)^2}}\right) \approx -1.8dB \qquad \text{(Eq. 6.9)}$$

This increase in input referred noise power can account for the majority of the increase in NF observed in measurement.

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[28] It is assumed that the input referred noise voltage of the VGCA is approximately $\sqrt{2}$ times a single-stage CG amplifier.

[29] Estimated value obtained from schematic simulation results

6.3 VGTA Measurement Results

The VGTA measurement results along with parasitic extracted simulation results for comparison purposes are presented in this section. The measurement setup is shown on Figure 147 on page 167.

6.3.1 DC

Figure below is the plot of measured and simulated common mode voltages of the VGA in transmit mode of operation.

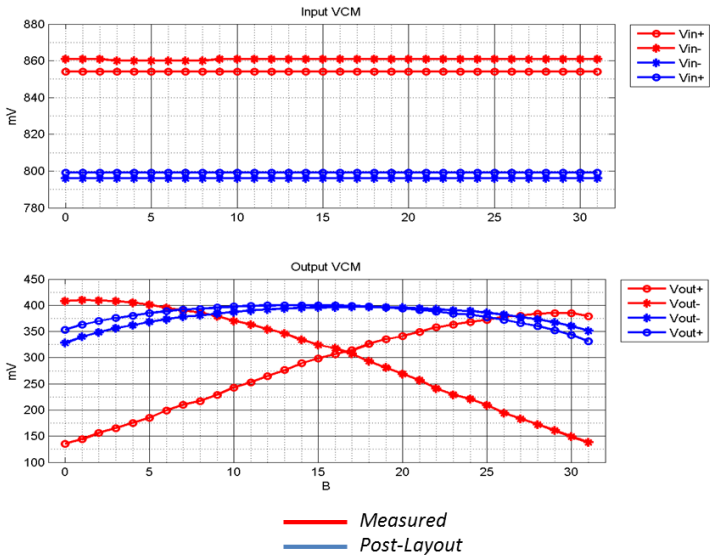

Figure 160: VGTA input and output common mode voltages – post-fabrication measurement results (Red) vs. layout parasitic extracted simulation results (Blue)

Measured input VCM is about 60mV larger than the simulation results. Any mismatch, however, between the current mirroring devices can cause an absolute error in the dc current through the common mode resistors, therefore directly changing the input

common mode voltage. To demonstrate this effect, Monte Carlo simulations with process and mismatch variations were run at schematic level.

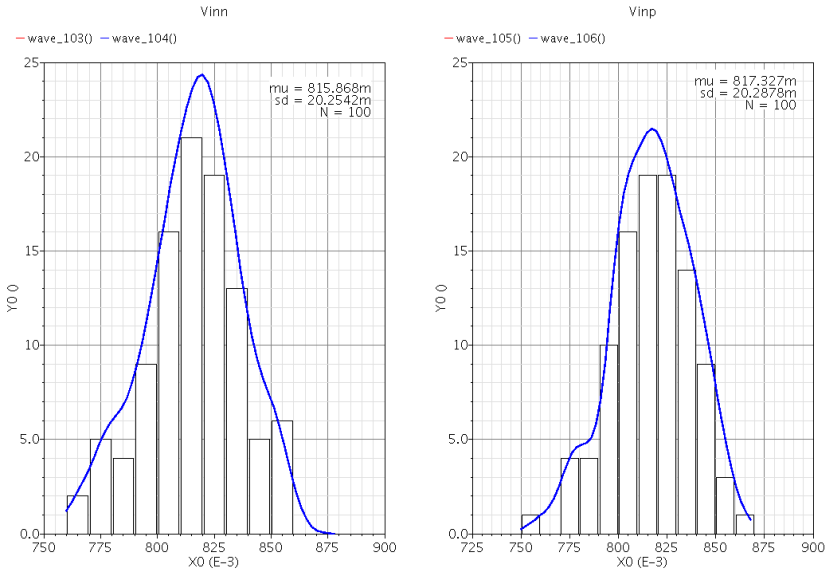

Figure 161: VGTA input common mode voltage variation with process and mismatch – schematic simulation results

The results of 100 Monte Carlo runs indicate a standard deviation of $20mV$ at the input common mode voltage, with worst case values as high as $870mV$ and as low as $750mV$.

At the output, measured common mode voltage varies significantly from $400mV$ to $150mV$ throughout the gain range. The VGTA CMFB circuit is not functioning properly based on measurement results. It is quite likely that, due to incorrect setup of the VGTA CMFB, the CMFB circuit is unable to control the common mode voltage, therefore practically floating the high resistance common mode voltage node of the VGTA. This high resistance node, then, can easily experience great voltage swings with any small

change in the current due to device mismatch. The CMFB circuit, as fabricated, is studied here.

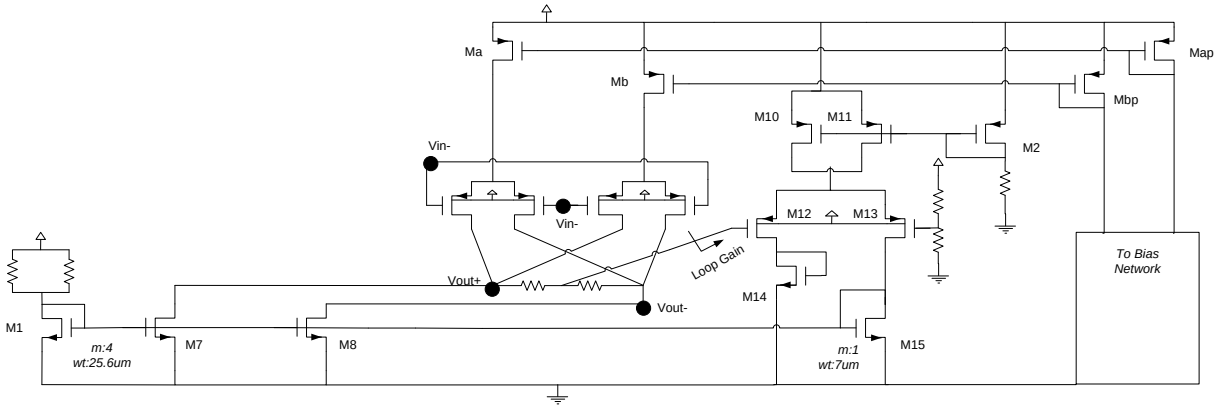

Figure 162: VGTA CMFB loop gain

The CMFB was intended to operate as follows: an increase in the common mode voltage would result in a decrease in the current of M_{12}, therefore increasing the current in diode connected M_{15}. This increase in current is mirrored by M_7 and M_8, therefore reducing the common mode voltage. As setup, however, the diode connected transistor, M_{15}, is connected to another, much larger diode connected transistor, M_1. An increase in current of M_{15} (due to increase in common mode voltage, for example), then would translate to a much smaller gate to source voltage increase on M_{15} (because M_{15} and M_1 are in parallel, M_{15} and M_1 have a much bigger effective width than the M_{15} transistor alone). This small change in the gate source voltage of M_7 and M_8, then, would translate into only a small loop gain, making the CMFB circuit ineffective. Loop gain and phase simulation results confirm this hypothesis, and are presented in Appendix F.

Monte-Carlo simulations with process and mismatch variations show a significant variation in the output common mode voltage from part to part. Figure below is the schematic simulation results of the output common mode voltage obtained from 100 Monte Carlo DC runs.

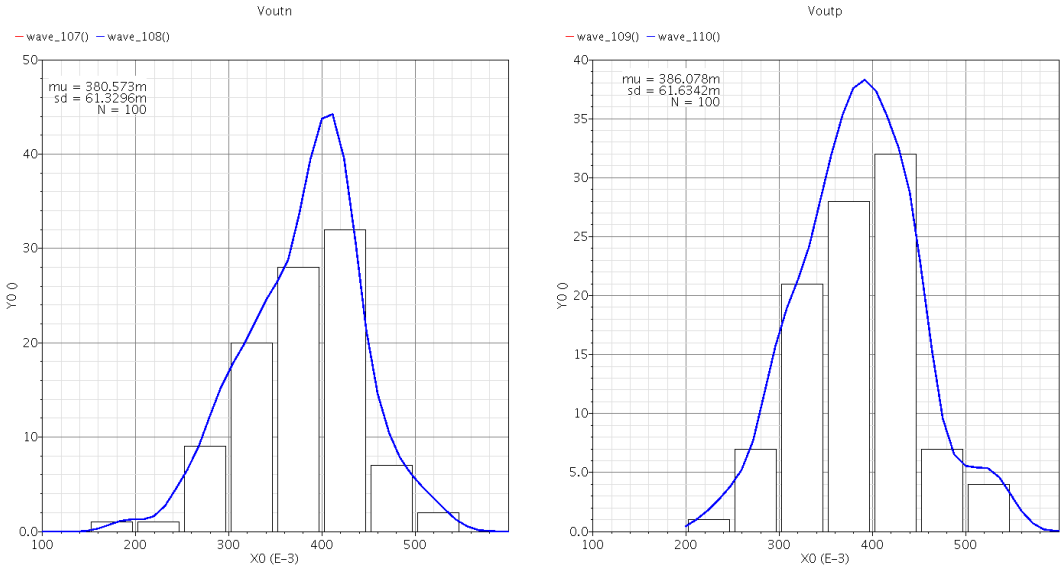

Figure 163: VGTA output common mode voltage variation with mismatch and process variation – schematic simulation results

6.3.2 AC

Figure 164 below is the peak to peak voltage and phase measurements at the output, with setup shown on Figure 147 on page 167.

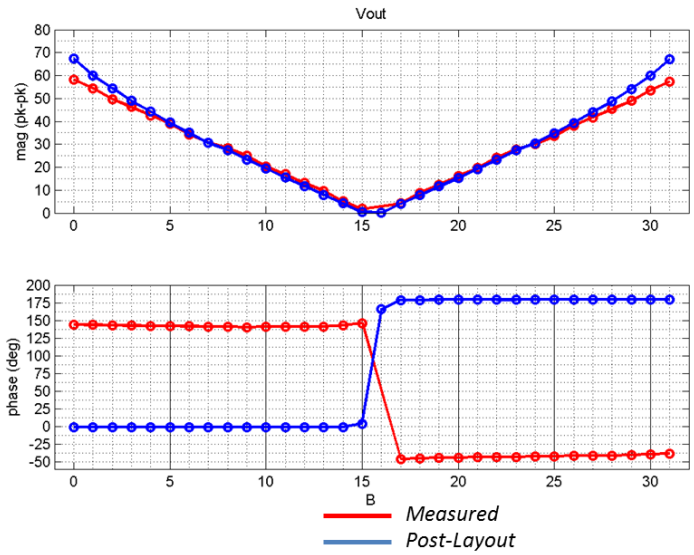

Figure 164: VGTA output voltage magnitude and phase – post-fabrication measurement results (Red) vs. layout parasitic extracted simulation results (Blue)

The 150^o phase offset between the measured and simulated results is again a testbench artifact and was explained in the previous section.

6.3.3 Linearity

$1dB$ compression point of the VGTA is measured and shown in Figure 165 below:

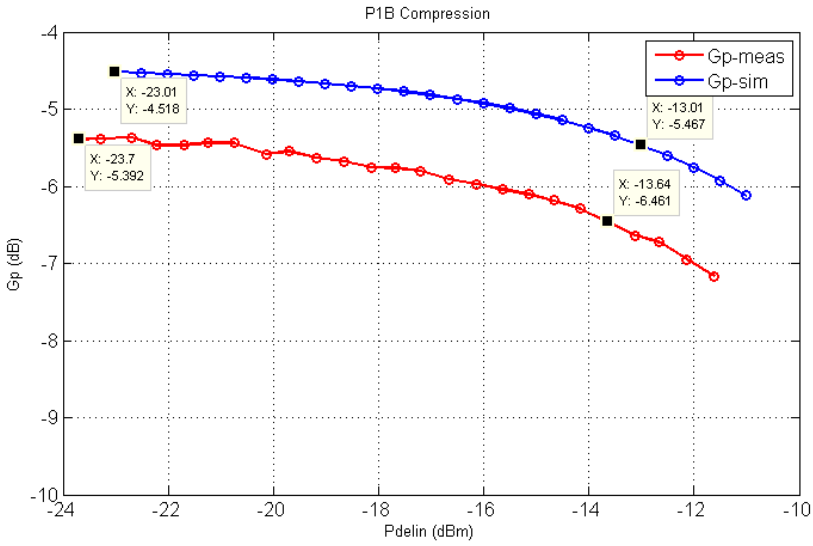

Figure 165: VGTA $1dB$ compression point – post-fabrication measurement results (Red) vs. layout parasitic extracted simulation results (Blue)

Measured $1dB$ compression point appears to be close to the simulation results.

6.3.4 NF

NF measurements closely match the layout parasitic extracted simulation results.

Figure 166 below shows the measurement and simulation results.

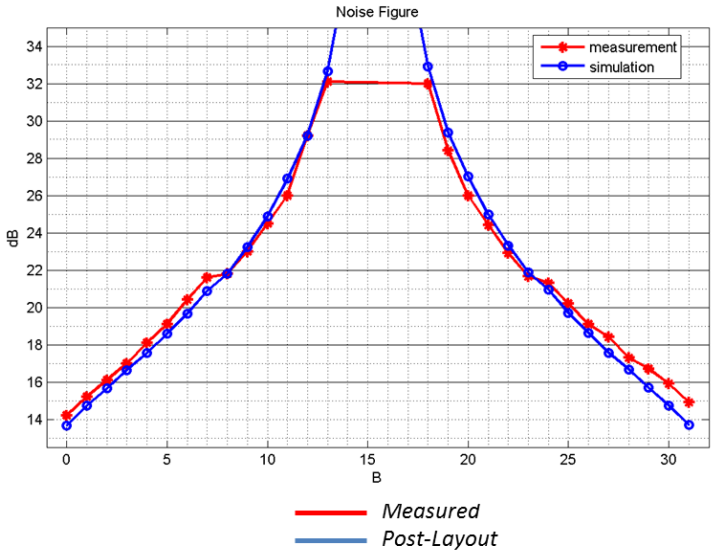

Figure 166: VGTA NF at $200MHz$ – post-fabrication measurement results (Red) vs. layout parasitic extracted simulation results (Blue)

For smaller gain values, corresponding to states 15 and 16, the NF meter did not produce reliable results.

6.4 VVGCA Measurements and Setup

The VVGCA's common mode voltages at the input and output appeared unstable in measurements. As stated earlier, the CMFB circuit controlling the output common mode voltage of the VGCA was not setup properly. Study of loop gain of the CMFB circuit of the VVGCA reveals that the output common mode voltage, as expected from inspection, is ineffective as setup. The figure below is the result of the stability simulation on the CMFB circuit of the schematic view of the VVGCA, performed on the In-phase channel. CMFB loop analysis of the fabricated VVGCA is offered in Appendix F.

To be able to still measure circuit's AC performance, DC voltage sources were used in the lab to force the common mode voltages to known, stable values. The VVGCA measurement setup is shown in Figure 167 below:

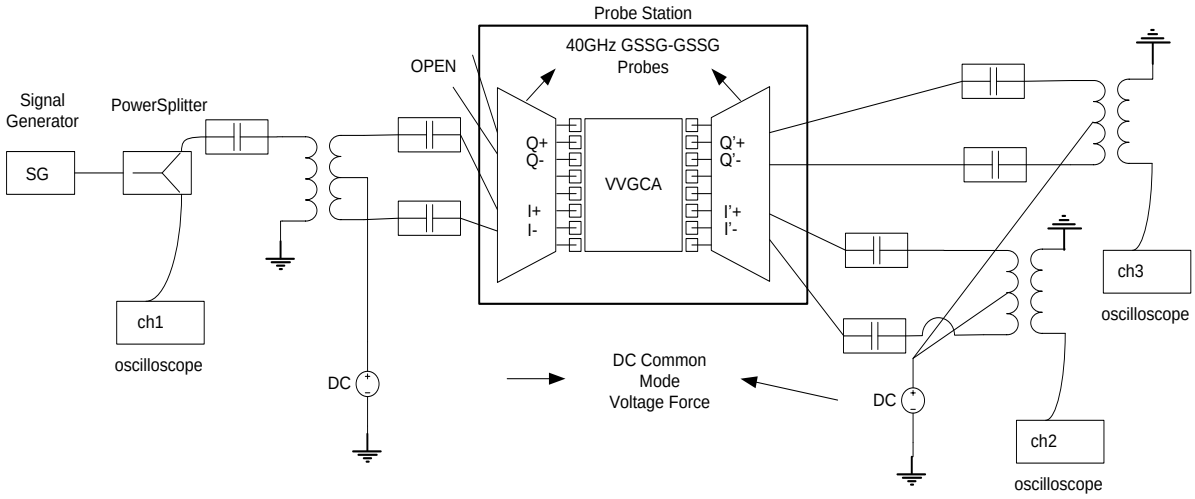

Figure 167: VVGCA measurement setup – forcing DC common mode voltages at input and output

To eliminate the effect of incorrect DC gain control connections to one of the inner two VGA blocks of the VVGCA (as stated earlier), the input signal was only supplied at the In-phase port of the VVGCA, as shown in the figure above. The output voltage was then measured at the in-phase and quadrature outputs of the VVGCA, and was compared to the simulation results.

6.4.1 AC

For a $-8dBm$ of available input power source at $20MHz$ from the signal generator, output AC voltages were obtained at In-phase and Quadrature outputs of the VVGCA. Figure 162 is the peak to peak voltage at the in-phase output of the VVGCA.

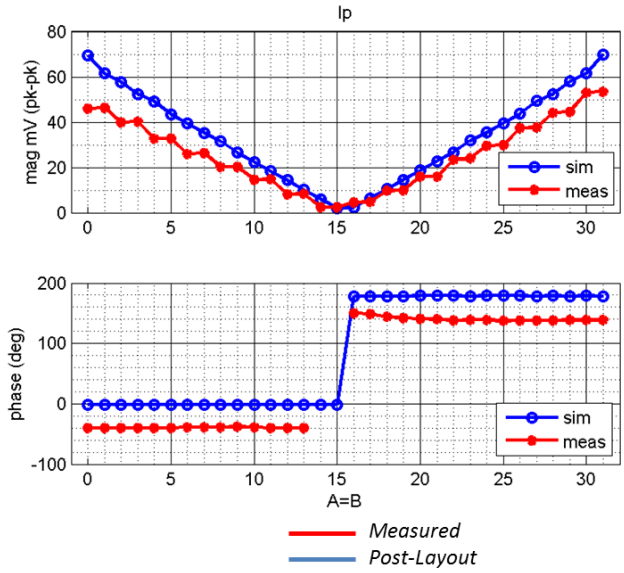

Figure 168: VVGCA output voltage of in-phase channel - magnitude vs. phase – post-fabrication measurement results (Red) vs. layout parasitic extracted simulation results (Blue)

The LSB non-functionality that was observed in the VGCA is again seen here. The magnitude plot exhibits a slightly lower slope than that of measured for VGCA (about 10%). The most likely reason for this drop could be a combination of mismatch between the VGCA main NMOS current mirroring transistors (likely because the devices are not common-centroid nor interdigitated) and the resistance tolerance variation of the resistors used to bias the diode connected NMOS (variation in absolute value of these resistors will directly alter the NMOS operating point). A drop in DC current of the individual

VGCAs due to such effects will reduce the effective transconductance similar to what is observed here.

Voltages at the Quadrature output of the VVGCA deviate significantly from expected values. Figure 169 below shows the results:

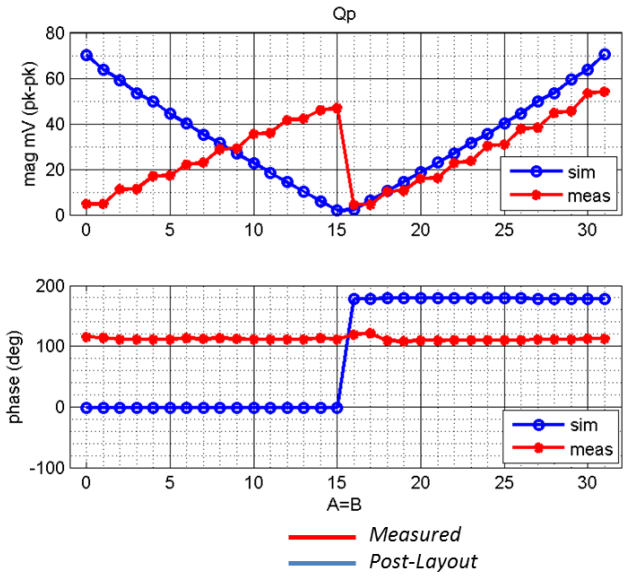

Figure 169: VVGCA output voltage of quadrature channel - magnitude vs. phase – post-fabrication measurement results (Red) vs. layout parasitic extracted simulation results (Blue)

Although not confirmed, the observed behavior of the measured output voltage amplitude and phase in Figure 169 would be explained if the MSB of the control word controlling the inner VGCA gain were shorted to the power supply. The following schematic simulation result shows the similar effect this short would have on the magnitude and phase of the quadrature output signal.

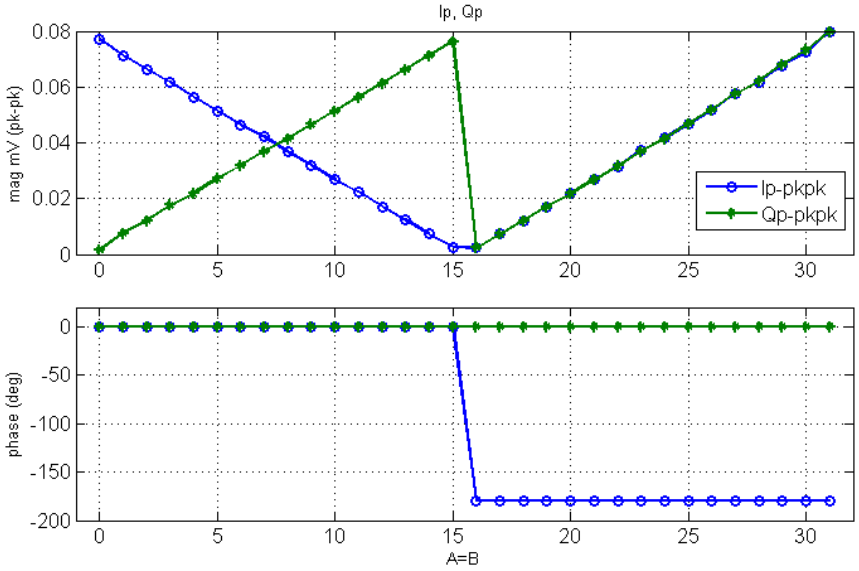

Figure 170: VVGCA: effect of a MSB NMOS gate short to power supply on output voltage – schematic simulation result

6.5 VVGTA Measurements and Setup

Measurement setup for the VVGTA is shown in Figure 171 below. The input signal is fed to the Quadrature input of the VVGTA and the In-phase input is left open.

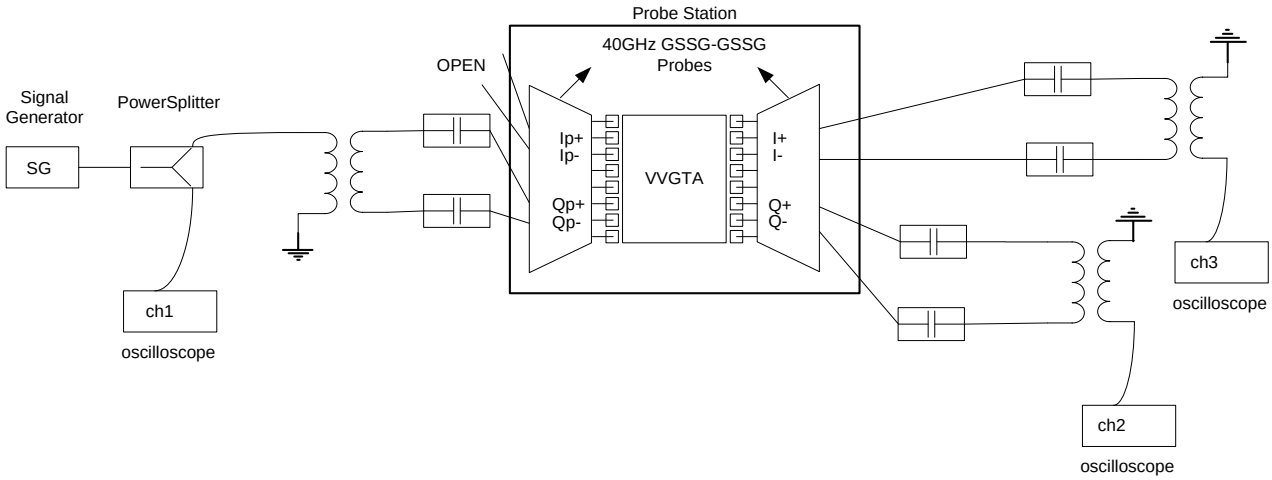

Figure 171: VVGTA measurement setup

6.5.1 DC

Figure 172 below shows the DC measurements at the input of the VVGTA and the parasitic extracted simulation results for comparison.

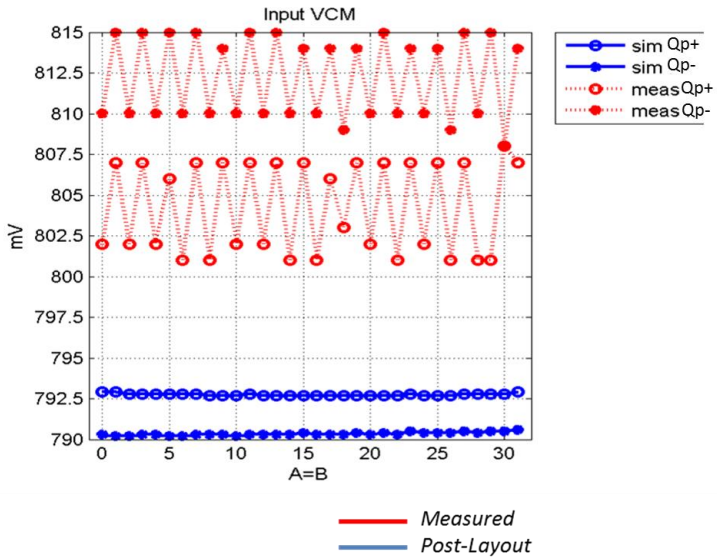

Figure 172: VVGTA input common mode voltages – post-fabrication measurement results (Red) vs. layout parasitic extracted simulation results (Blue)

The slight offset (less than 1%) between the measured positive and negative input common mode voltages are most likely due to random mismatches between the $10k\Omega$ resistors from gates of PMOS CS amplifying transistors to ground that set the common mode voltage. The difference between the extracted simulation results and that of measurement can also be due to random variations in the absolute value of p-poly resistors used ($\sim$2.5% increase).

Output common mode voltages deviate significantly from the simulation results. Figure 173 below shows the DC voltages at the In-phase and Quadrature output of the VVGTA.

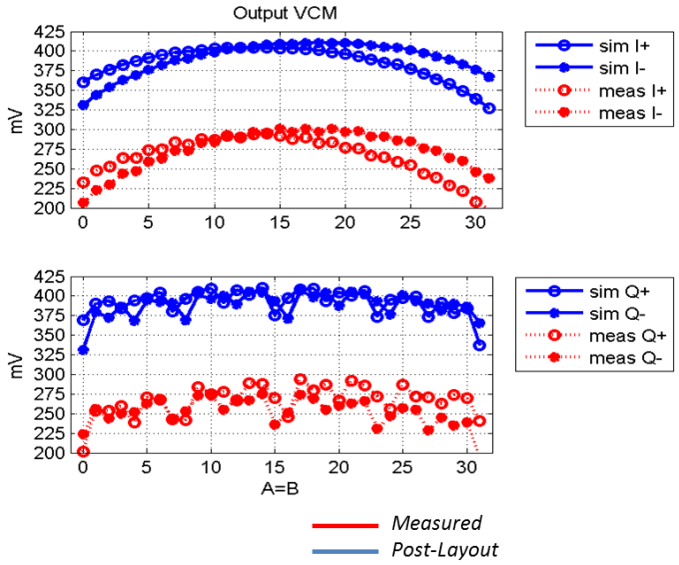

Figure 173: VVGTA output common mode voltages – post-fabrication measurement results (Red) vs. layout parasitic extracted simulation results (Blue)

The large deviation from simulation results to that of measurements can be explained as follows: The differential output nodes of the VVGTA are high impedance nodes whose DC values are set by the CMFB loop. The I-Channel loop gain of the VVGTA CMFB is presented in Appendix F. The VVGTA CMFB loop gain is at almost minus twenty decibels at low frequencies, indicating no common mode regulation at the output. Process corner and mismatch simulation results indicate that a great variation in DC voltage levels at the output is expected:

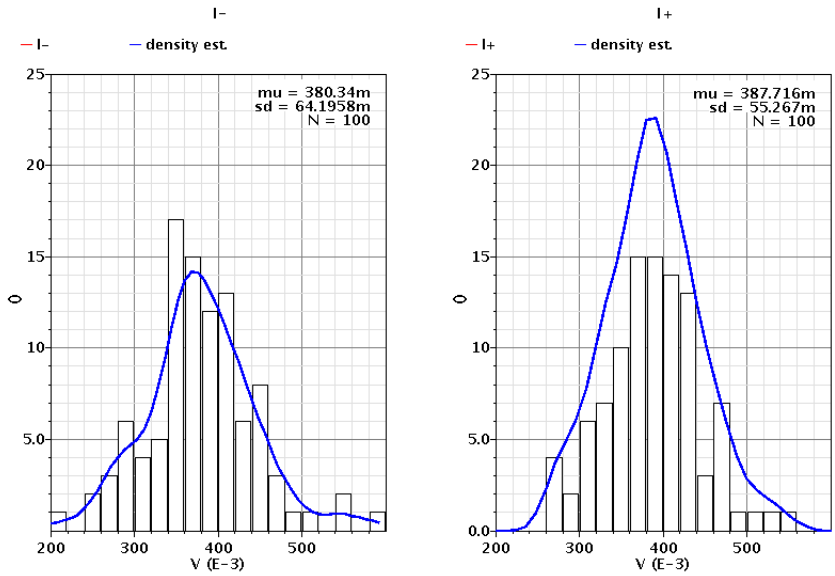

Figure 174: VVGTA output common mode voltage - monte-carlo simulation results – schematic simulation result

Although the CMFB loop is ineffective in regulating the output common mode voltage, no oscillation was observed in the output common mode voltage.

6.5.2 AC

Figure 175 below shows the measurement peak to peak and phase of the output in-phase and quadrature voltages.

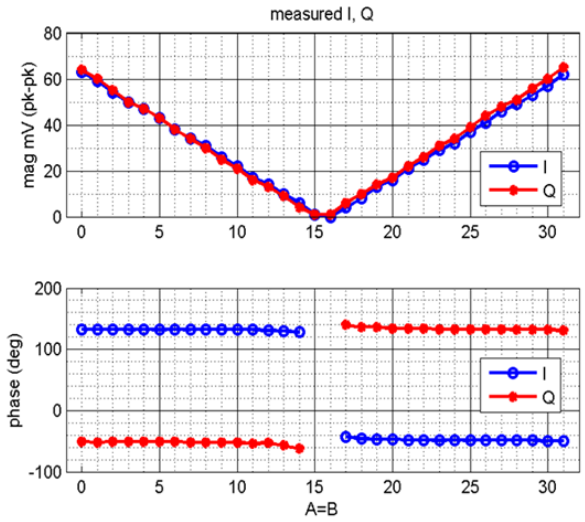

Figure 175: VVGTA in-phase, quadrature output voltages - post-fabrication measurement results

The in-phase and quadrature output voltages of the VVGTA, as measurement results of Figure 175 indicate, are symmetric and the expected 180^o phase offset between the positive and negative gain states is observed.

Figure 176 below shows the In-phase and Quadrature outputs compared to the parasitic extracted simulation results:

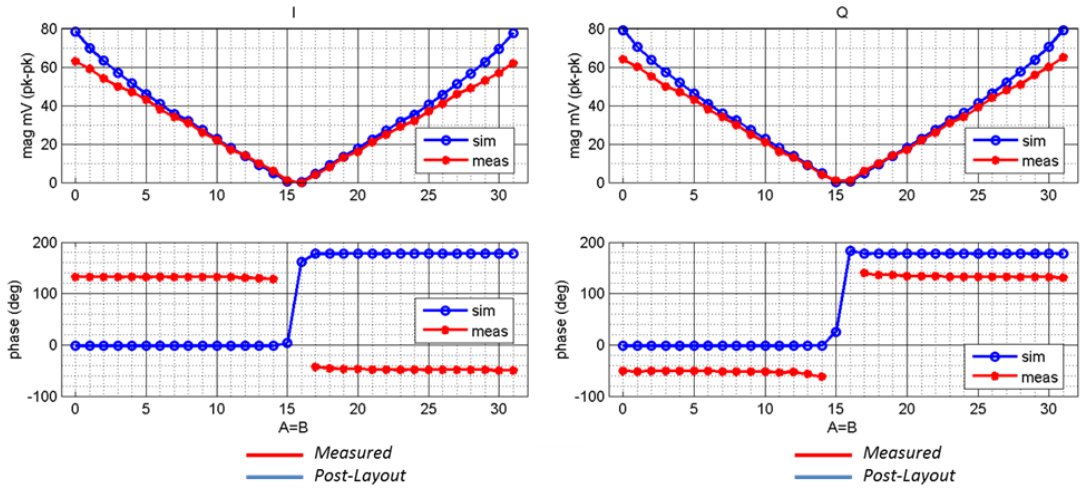

Figure 176: VVGTA in-phase (Left) and quadrature (Right) output voltage magnitude and phase – post-fabrication measurement results (Red) vs. layout parasitic extracted simulation results (Blue)

At lower magnitude gain states $\cong (5 < s < 25)$, the measured and simulated output voltages are in close agreement. At higher gain states $\cong (0 < s < 5, 25 < s < 31)$, however, voltage magnitudes deviate from the expected square root behavior, exhibiting a more linear behavior. A similar trend was observed when studying the difference between the schematic simulation results of VGTA transconductance and that of calculated (Figure 51 on page 66), where the linear behavior of simulated transconductance at higher gain states was attributed to current mismatch in VGTA's digital control word to analog current converter (D/A) transistors due to channel length modulation effect. Although this behavior did not seem to exacerbate when comparing layout extracted simulation results to that of the schematic, it is noted that the layout extracted netlist did not include any transistor mismatch. VGTA D/A transistors are laid out along an approximately $200um$ long x-axis gradient, exposing them to threshold mismatch effects. It can therefore be hypothesized that the mismatch between the

measured in-phase and quadrature voltages of the VVGTA and that of layout extracted simulation results is due to mismatch between the D/A transistors. It is noted that a similar mismatch between the measured and simulated output voltages was observed when comparing VGTA measurements with post-layout simulation results (Figure 164 on page 186).

The complex voltage at the output of the VVGTA, $I + jQ$, can be deduced by using the voltage measurements at the In-phase and Quadrature outputs of the VVGTA above. Figure 177 below is the complex voltage at the output of VVGTA, obtained by complex addition of the measured voltage and phase values at the In-phase and Quadrature outputs of the VVGTA. This value is compared to the complex voltage obtained in the same manner using the In-phase, Quadrature voltage values from the parasitic extracted layout.

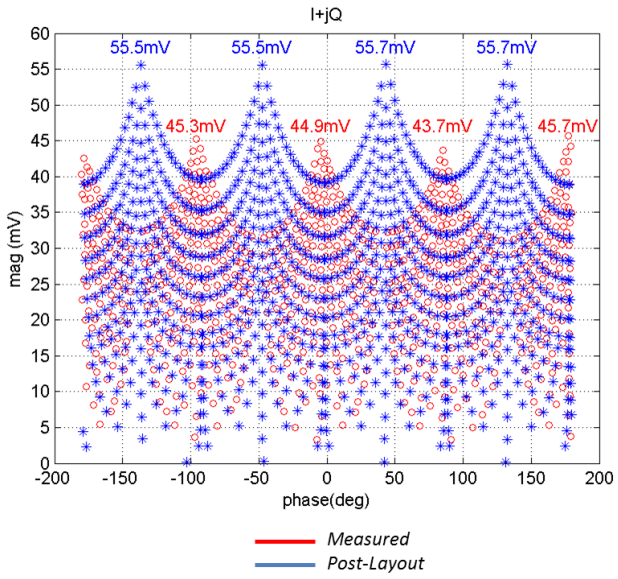

Figure 177: VVGTA complex output voltage – post-fabrication measurement results (Red) vs. layout parasitic extracted simulation results (Blue)

The apparent phase shift between the measured and simulated gain states is a testbench artifact. A 50^{o} phase offset between measured and post-layout simulation results of the I and Q channels, as observed in Figure 176 is due to the fact that the phase measurements only reliably measure the phase offset between the differential signals, ignoring any offset introduced by the power splitter and baluns. Adding this offset to all phase measurements produces results that are in phase with the simulated values. The figure below shows the gain states versus magnitude and phase of the output complex signal with this offset value applied:

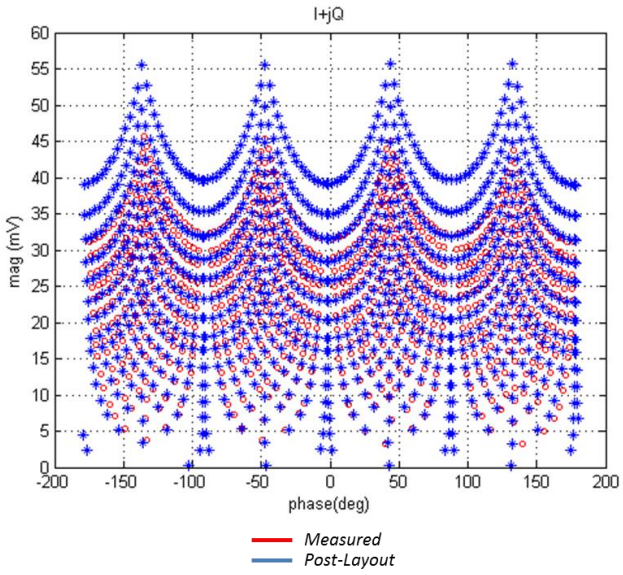

Figure 178: VVGTA complex output voltage – post-fabrication measurement results with phase offset correction (Red) vs. layout parasitic extracted simulation results (Blue)

The maximum error vector between the parasitic extracted and measured complex voltage results is obtained to be:

$$(|V_{meas}(A,B)| - |V_{ext}(A,B)|)|_{worst\ case} = -2dB \qquad \text{(Eq. 6.10)}$$

$$(\measuredangle V_{meas}(A,B) - \measuredangle V_{ext}(A,B))_{worst\ case} = -5.5^{o} \quad \text{(Eq. 6.11)}$$

Similar to the complex constant correction that was applied to the VVGTA complex current gain extracted simulation results relative to the schematic simulation results, an average complex voltage gain error can be computed and applied to the measured complex voltage results and a mean error vector is calculated.

$$\overline{|V_{error}|} \equiv \frac{1}{2^{10}} \sum_{\substack{0\le A\le 31 \\ 0\le B\le 31}} \{|V_{meas}(A,B)|_{dB20} - |V_{ext}(A,B)|_{dB20}\} = -0.9dB \quad \text{(Eq. 6.12)}$$

$$\overline{\measuredangle V_{error}} \equiv \frac{1}{2^{10}} \sum_{\substack{0\le A\le 31 \\ 0\le B\le 31}} \{\measuredangle V_{meas}(A,B) - \measuredangle V_{ext}(A,B)\} = -0.4^{o} \quad \text{(Eq. 6.13)}$$

The figure below is the plot of the error compensated measured complex voltage compared to parasitic extracted simulation results.

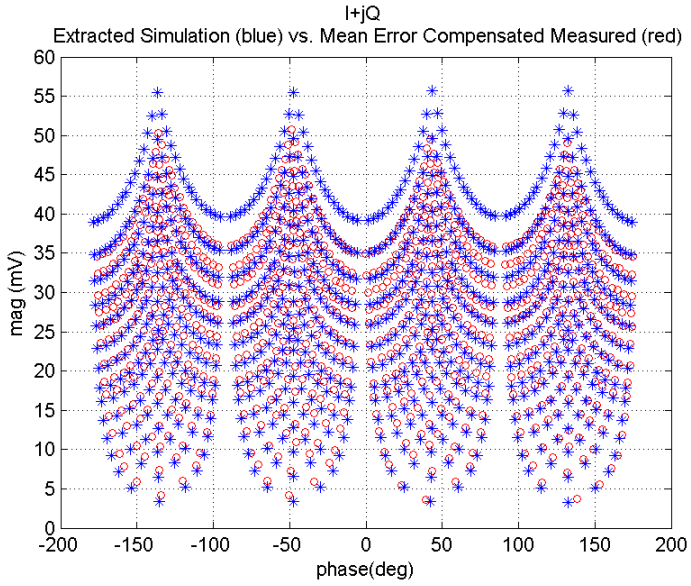

Figure 179: VVGTA complex output voltage – mean error compensated post-fabrication measurement results (Red) vs. layout parasitic extracted simulation results (Blue)

Maximum magnitude and phase error between the extracted simulation results and the error compensated measurement results are:

$$\left(\left|V_{comp}(A,B)\right|_{dB20} - \left|V_{ext}(A,B)\right|_{dB20}\right)\Big|_{worst\ case} = -1.16dB \quad \text{(Eq. 6.14)}$$

$$\left(\measuredangle V_{comp}(A,B) - \measuredangle V_{ext}(A,B)\right)_{worst\ case} = 1^{o} \quad \text{(Eq. 6.15)}$$

Where:

$$V_{comp}(A,B) \equiv V_{ext}(A,B) - \overline{V_{error}} \quad \text{(Eq. 6.16)}$$

CHAPTER 7

CONCLUSIONS

The scope of this thesis was to introduce the concept, design procedure, layout, and post-fabrication measurements for the bi-directional VVGA that is used in the transceiver module of each antenna element of the electronically-steered phased array system, as shown in Figure 2 on page 3. The bi-directionality of the VVGA, discrete gain control of the VVGCA and VVGTA, DC Biasing and CMFB, and layout sizing and floor planning were some of the more challenging parts of this project.

Discrete gain control through changing the effective transistor size requires, as stated earlier, implementation of 124 NMOS devices. Designing a floor plan while keeping the layout area to a minimum and ensuring symmetry of the differential amplifiers were of most challenge during the layout process.

Appropriate interconnection of VGAs to form the VVGA was another challenge faced during design. A design flaw in implementation of CMFB for VVGA that led to a non-robust DC biasing and voltage common mode control may have been costly as post-fabrication measurements indicated large DC deviations at input and output, along with signs of instability at the output. This design weakness was not caught in schematic and parasitic extracted simulations, as device mismatch and Monte Carlo simulations were not run prior to fabrication to observe large variance at the output. Most importantly, CMFB loop gain simulations were not run prior to chip submission for fabrication, which would have unveiled the ineffectiveness of the CMFB loop in regulating the common

mode. As seen in Appendix F, CMFB loop gain results of the fabricated design indicate the non-functionality of the loop. In this thesis, a modified design was presented in an attempt to demonstrate possible future design improvements.

A major setback in the post-fabrication measurements was the large attenuation at the output for $200MHz$ signals. This attenuation was not repeatable in post-layout simulation results. The post-fabrication measurements were performed for $20MHz$ input signals. At this frequency, AC measurement results correlated to the simulation results, with deviations that are explained in the text.

Another setback in the post-layout and post-fabrication of the VVGA was the error in connecting the DC gain control of one of the four VGAs (corresponding to block $-Bsin\emptyset$ on Figure 5 on page 6). This was not caught in a timely manner because the full VVGA simulations were not run prior to chip submission for fabrication. To test functionality, alternative simulation and measurement techniques were offered in chapters five and six. Other issues common to all parts in post-fabrication measurements indicated that the LSB of the gain control word did not properly change the transconductance of the VVGCA, and that MSB of the gain control word during transmit mode of operation was ineffective. Possible root-causes of these effects are provided in Chapter six, but a definite root-cause was not discovered due to lack of debug tools, such as additional on-chip probe pads.

Aside from aforementioned issues, bi-directionality and discrete gain control concepts for the VVGA proved functional. Complex gain magnitude vs. phase look up tables in both receive and transmit directions, as shown in Figure 82*: VVGCA complex current*

gain on page 98 and Figure 94*: VVGTA complex transadmittance* on page 112, may be used to provide phase shift at each antenna element and compensate for random phase and magnitude errors in the transceiver module of the electronically steered phased array architecture, as mentioned in the introduction to this thesis.

To sum up, the phase resolution plots of the VVGCA and VVGTA complex gain are offered here. Because of the problem encountered during measurement of the Quadrature channel of the VVGTA, where no phase change was observed across gain states (Figure 169 on page 191), complex current gain and complex transadmittance gain phase resolution plots of the VVGCA and VVGTA obtained from extracted simulation results are offered here for comparison.

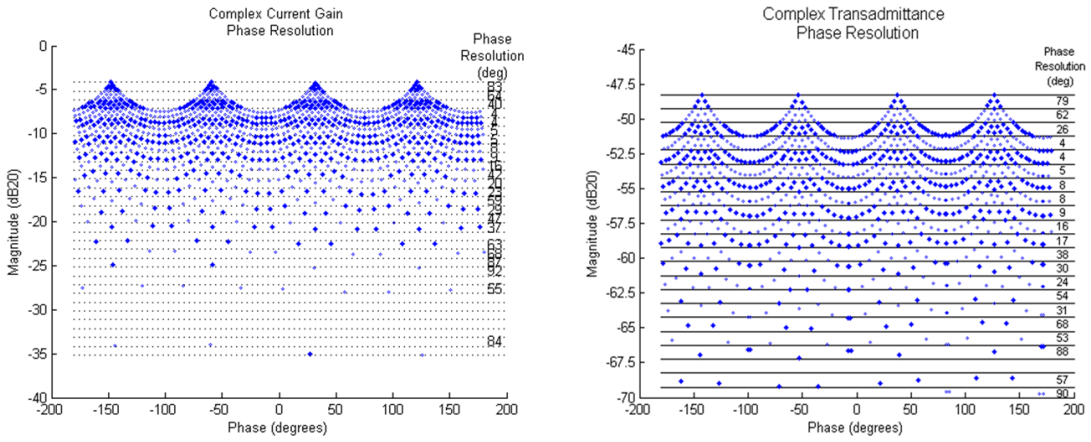

Figure 180: VVGCA complex current gain phase resolution (Left) and VVGTA complex transadmittance (relative to one siemens) phase resolution – layout parasitic extracted simulation results

For the VVGCA complex current gain, the best phase resolution is 4^o and it is at gain intervals of $[-7dB, -8dB]$ and $[-8dB, -9dB]$. For the VVGTA, the best phase resolution is again 4^o at gain intervals of $[-51dB, -52dB]$ and $[-52dB, -53dB]$. This

implies that at the above gain intervals, a 360^o phase shift with 4^o of phase resolution is achievable in both receive and transmit VVGAs.

APPENDICES

APPENDIX A

DESIGN MODIFICATIONS

Chapters two, three, and four offer modified design versions of the fabricated chip in order to correct for some design flaws originally present. These changes are highlighted in this section.

A.1 Bi-Directional VGA Design Issues and Modifications

Design Issues:

The main design issues in the original bi-directional VGA are listed here, with the implemented solutions presented afterward:

1. VGCA CMFB error amplifier is biased independent of the VGCA tail bias currents. This creates additional mismatch between VGCA tail bias currents and the CMFB tail bias current and is undesirable because proper CMFB operation requires a precise current ratio between VGCA NMOS current sink devices and the CMFB diode connected PMOS device that controls the VGCA PMOS load currents.
2. The NMOS load current sources in transmit mode are controlled independently of the transmit CMFB circuit due to large size of the main current mirroring diode connected NMOS transistor compared to the small transmit CMFB NMOS current mirroring diode connected transistor. Variations in gate voltage of the VGTA CMFB NMOS diode connected device due to variations in common mode

output voltage, then, are reduced significantly as this device appears in parallel with the large, independently biased diode connected NMOS device, reducing the CMFB loop gain significantly.

3. VGTA CMFB error amplifier is biased independent of the VGTA bias currents I_a and I_b . This creates additional mismatch between I_a and I_b currents and the CMFB tail bias current and is undesirable because proper CMFB operation requires a precise current ratio between $(I_a + I_b)$ and the CMFB diode connected NMOS device that controls the VGTA NMOS load currents.

The following figure depicts the original Bi-Directional VGA schematic:

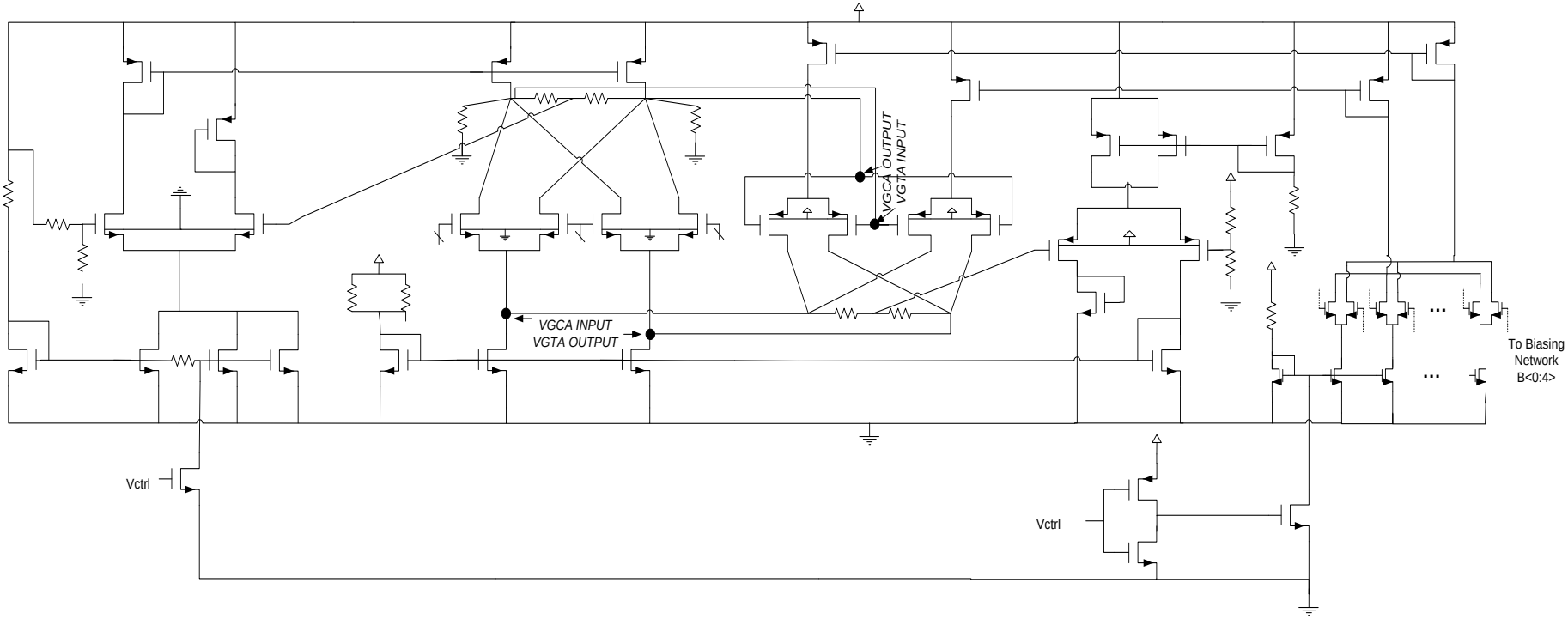

Figure 181: Schematic of bi-directional VGA – fabricated design

Design Modifications:

Following improvements have been implemented in the new design of the bi-directional VGA:

1. VGCA CMFB and current mirroring NMOS devices are controlled by one diode connected NMOS device. During receive, the VGTA CMFB connection to the VGCA is cut off. The VGCA NMOS current sources along with the CMFB circuit current source are biased using one diode connected NMOS that in the original design biased the CMFB circuit. The PMOS current sources of the VGCA are then biased using a diode connected PMOS transistor in the feedback loop that ensures a correct ratio of the current is mirrored onto the VGCA PMOS current sources to maintain the appropriate output common mode voltage.
2. During transmit, the VGCA CMFB connection to VGTA is cut off, and the NMOS current mirroring devices are only controlled by the current in the diode connected NMOS of the VGTA CMFB circuit. In addition, the PMOS current sources of the VGTA and the CMFB circuit are biased using the same two diode connected transistors (VGTA D/A PMOS devices that set the variable bias currents (I_a, I_b) of the VGTA). This architecture ensures that the correct bias is applied to the VGTA NMOS current sources to maintain the desired common mode output voltage level.

The following figure depicts the modified Bi-Directional VGA schematic:

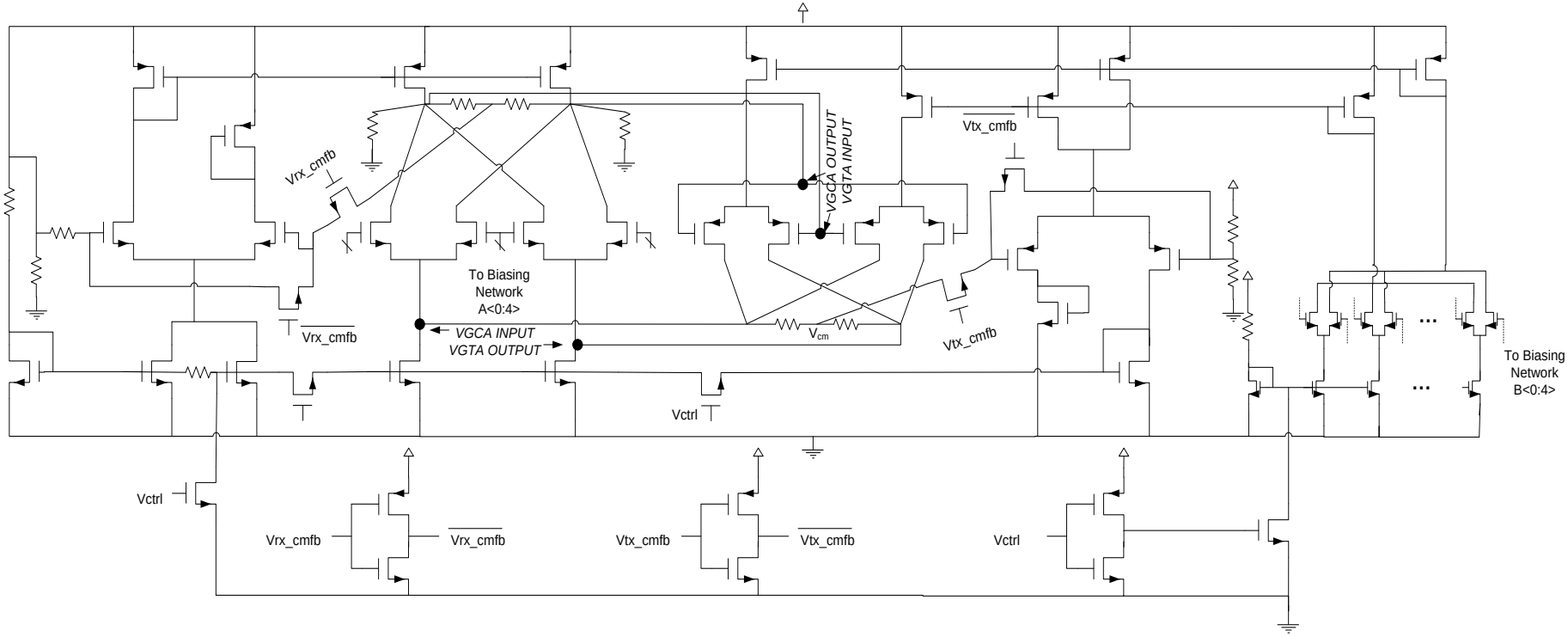

Figure 182: Schematic of bi-directional VGA – modified design

A.2 VVGA Design Issues and Modifications

Besides the error introduced in the fabricated design by incorrect connection of the gain states, the main error in connecting the VGA blocks to create the VVGA was presence of two CMFB loops for each of the two output nodes (In-phase and Quadrature) of the VGA. To correct for this issue, it was necessary to add to the VGA the feature to disable the CMFB of one VGTA and one VGCA in both receive and transmit modes. In the figure below, highlighted switches were added to implement this change:

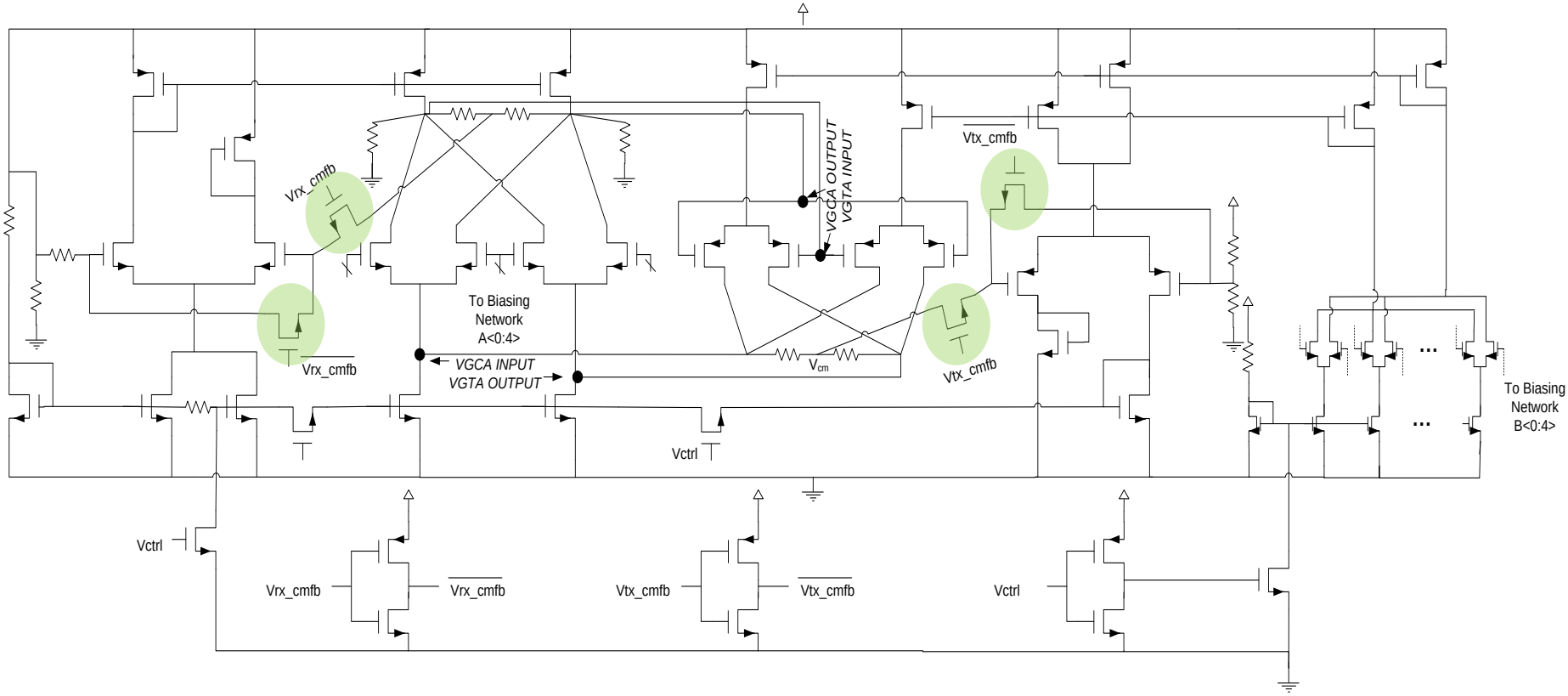

Figure 183: Schematic of bi-directional VGA with VGCA and VGTA CMFB loop ON and OFF programmability switches highlighted – modified design

To turn off the VGTA CMFB during receive, the VGTA output node is disconnected from the CMFB error amplifier, and the input pair transistors of the VGTA CMFB amplifier are connected together using the TX CMFB switch. The VGCA CMFB is turned off similarly during transmit mode of operation using the RX CMFB switch. This architecture, then, allows for the VVGA to have one CMFB loop active for each output node, as shown in Figure 75 on page 90 and repeated here for convenience:

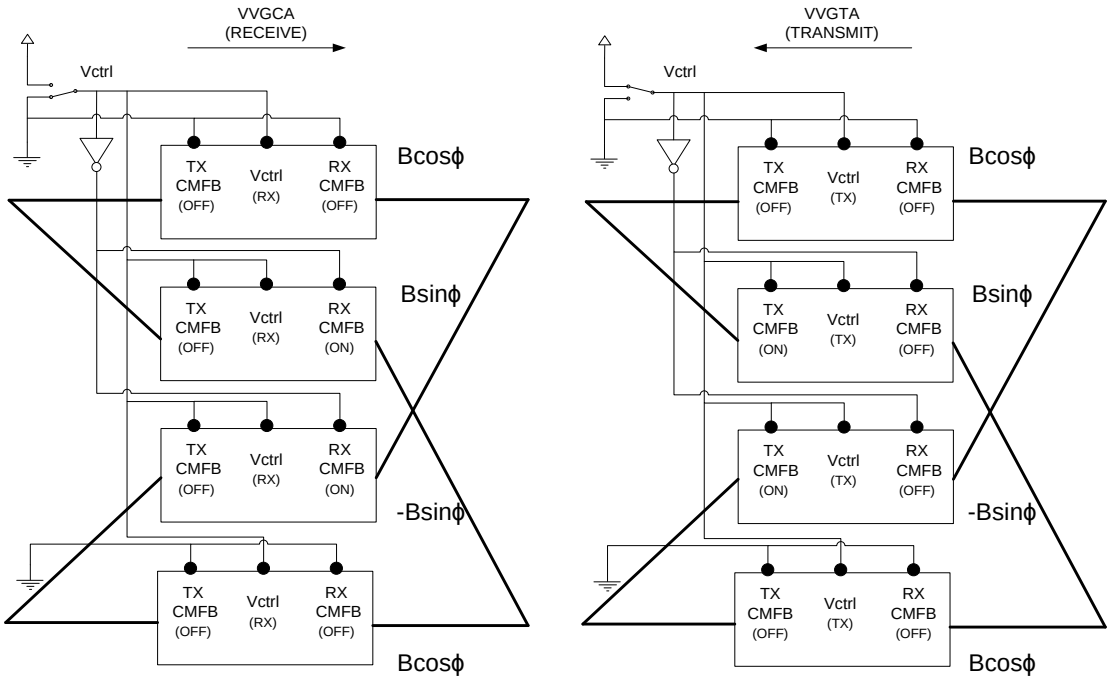

Figure 184: VVGA control signal positions in VVGCA and VVGTA configurations – modified design

APPENDIX B

VGCA INPUT RESISTANCE VARIATION WITH GAIN STATE AND LOAD RESISTANCE

Referring to Figure 23 on page 34, the VGCA input resistance looking at the source of CS transistors M_1 and M_2 is shown in Figure 185 below:

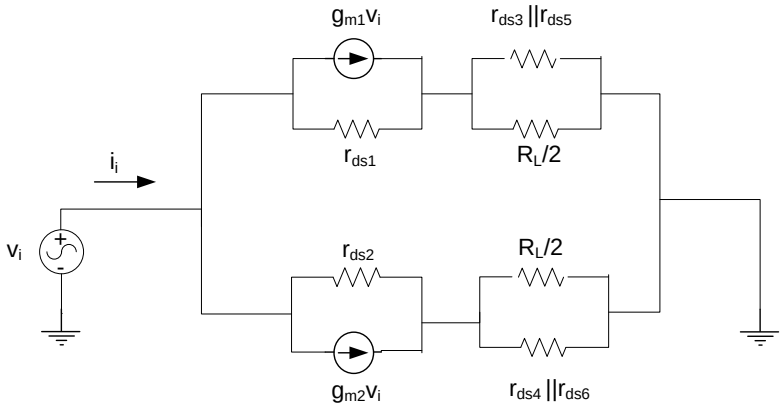

Figure 185: VGCA small signal model for input resistance calculations

Simple nodal analysis of the above schematic with the load resistance equal to R_L results in:

$$R_{in} = \frac{r_{ds1} + (r_{ds3}||r_{ds5}||\,R_L/2)}{1 + g_{m1}r_{ds1}} || \frac{r_{ds2} + (r_{ds4}||r_{ds6}||\,R_L/2)}{1 + g_{m2}r_{ds2}} \qquad \text{(Eq. B.1)}$$

For an open load resistance, the input resistance simplifies to:

$$R_{in,open} = \frac{r_{ds1} + (r_{ds3}||r_{ds5})}{g_{m1}r_{ds1}} || \frac{r_{ds2} + (r_{ds4}||r_{ds6})}{g_{m2}r_{ds2}} \qquad \text{(Eq. B.2)}$$

Assuming comparable values of channel length modulation parameter for n-channel and p-channel transistors, the resistance seen at the drain of amplifying transistors creates

a slight deviation from the input resistance previously calculated in (Eq. 2.14) on page 23.

The input resistance can be evaluated at different gain settings. At maximum gain setting, the input resistance will be:

$$R_{in,open,max\,gain} = \left(\frac{1}{g_{m1}} + \frac{1/\lambda(I_{ds3} + I_{ds5})}{g_{m1}/\lambda I_{ds1}}\right) || \left(\frac{1}{g_{m2}} + \frac{1/\lambda(I_{ds4} + I_{ds6})}{g_{m2}/\lambda I_{ds2}}\right) \quad \text{(Eq. B.3)}$$

Because at maximum gain setting:

$$I_{ds1} = I_{ds5} = I_{ds4} = I_{ds6}$$

$$I_{ds2} = I_{ds3} \approx 0 \rightarrow g_{m2} \approx 0$$

The open terminated input resistance at maximum gain setting becomes:

$$R_{in,open,\max gain} = \frac{2}{g_{m,max}} \quad \text{(Eq. B.4)}$$

Where $g_{m,max}$ is the transconductance of transistor M_1 when $I_{ds1} = I_{ds5}$.

At minimum gain setting, because

$$I_{ds1} = I_{ds2} = I_{ds3} = I_{ds4} = \frac{I_{ds5}}{2} = \frac{I_{ds6}}{2}$$

$$g_{m1} = g_{m2} \approx \frac{g_{m,max}}{2}$$

The open input resistance becomes:

$$R_{in,open,\min gain} = \frac{1}{2}\left(\frac{2}{g_{m,max}} + \frac{1/3\lambda I_{ds1}}{g_{m,max}/2\lambda I_{ds1}}\right) \quad \text{(Eq. B.5)}$$

$$R_{in,open,\min gain} = \frac{4}{3g_{m,max}} \quad \text{(Eq. B.6)}$$

Input resistance for a shorted output and minimum and maximum gain settings is calculated next. The shorted output input resistance becomes:

$$R_{in,short} = \frac{r_{ds1}}{1 + g_{m1}r_{ds1}} || \frac{r_{ds2}}{1 + g_{m2}r_{ds2}} \quad \text{(Eq. B.7)}$$

At maximum gain setting, because $g_{m2} \approx 0$ and $g_{m1}r_{ds1} \gg 1$:

$$R_{in,short,max\,gain} \approx \frac{1}{g_{m,max}} \quad \text{(Eq. B.8)}$$

At minimum gain setting, $g_{m1} = g_{m2} \approx g_{m,max}/2$, and $g_{m1}r_{ds1} \approx g_{m2}r_{ds2} \gg 1$, therefore:

$$R_{in,short,min\,gain} \approx \frac{1}{g_{m,max}} \quad \text{(Eq. B.9)}$$

The effect of load resistance on the input resistance for typical values of differential resistance ($R_L \approx 50\Omega$) seen at the IF feed line is small enough to be treated as short:

$$R_{in,R_L=50\Omega} \approx \frac{1}{g_{m1} + g_{m2}} = \frac{1}{g_{m,max}} \quad \text{(Eq. B.10)}$$

Table below is the summary of VGCA input resistance calculations offered in this section:

Gain Setting	R_L	R_{in}
$Maximum\ (0,31)$	$Short$	$1/g_{m,max}$
$Minimum\ (15,16)$	$Short$	$1/g_{m,max}$
$Maximum\ (0,31)$	$Open$	$2/g_{m,max}$
$Minimum\ (15,16)$	$Open$	$4/3g_{m,max}$

Table 3: VGCA input resistance versus gain settings and load

APPENDIX C

VGCA OUTPUT RESISTANCE VARIATION WITH GAIN STATE AND LOAD RESISTANCE

The input source resistance can cause VGCA output resistance to deviate from the parallel combination of r_{o5}, r_{o1}, and r_{o2}, as shown in below:

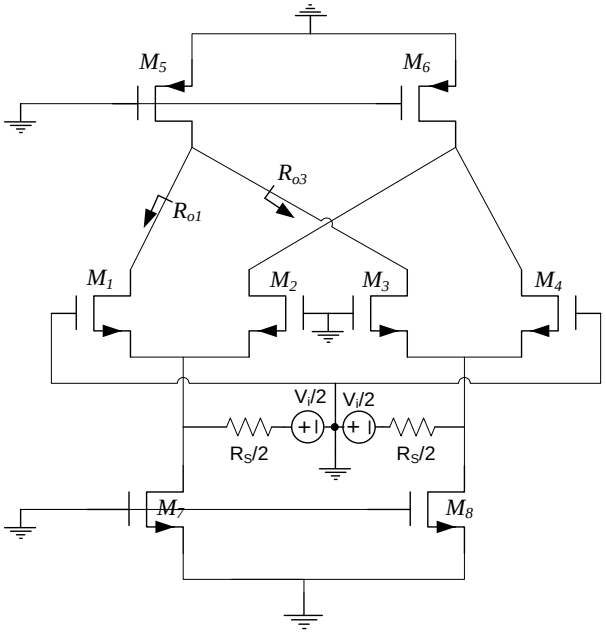

Figure 186: VGCA output resistance – effect of source resistance

Presence of R_s increases VGCA output resistance. Referring to figure above:

$$R_{o1} = g_{m1} r_{o1} \frac{R_s}{2} + r_{o1} + \frac{R_s}{2} \approx r_{o1}\left(g_{m1}\frac{R_s}{2} + 1\right) \quad \text{(Eq. C.1)}$$

$$R_{o3} = g_{m3} r_{o3} \frac{R_s}{2} + r_{o3} + \frac{R_s}{2} \approx r_{o3}\left(g_{m3}\frac{R_s}{2} + 1\right) \quad \text{(Eq. C.2)}$$

$$R_o = r_{o5} || R_{o1} || R_{o3} > r_{o5} || r_{o1} || r_{o3} \quad \text{(Eq. C.3)}$$

With presence of a source resistance, R_s, the output resistance becomes a function of gain setting:

$$r_{o1,\max\_gain} = \frac{1}{2} r_{o1,\min\_gain} \quad \text{(Eq. C.4)}$$

$$r_{o3,\max\_gain} = \frac{1}{2} r_{o3,\min\_gain} \quad \text{(Eq. C.5)}$$

At maximum gain setting, the output resistance is:

$$R_{o1} = r_{o1,\max\_gain}\left(g_{m,max}\frac{R_s}{2} + 1\right) \quad \text{(Eq. C.6)}$$

$$R_{o3} \cong \infty \quad \text{(Eq. C.7)}$$

$$R_{o,\max_{gain}} = r_{o5} || \, R_{o1} = r_{o1,\max_{gain}}\left(g_{m,max}\frac{R_s}{2} + 1\right) || r_{o5} \quad \text{(Eq. C.8)}$$

At minimum gain setting, the output resistance becomes:

$$R_{o1} = 2r_{o1,\max\_gain}\left(\frac{g_{m,max}}{2}\frac{R_s}{2} + 1\right) \quad \text{(Eq. C.9)}$$

$$R_{o3} = R_{o1} \quad \text{(Eq. C.10)}$$

$$R_{o,\min_{gain}} = r_{o1,\max\_gain}\left(\frac{g_{m,max}}{2}\frac{R_s}{2} + 1\right) || r_{o5} \quad \text{(Eq. C.11)}$$

Table below is the summary of VGCA output resistance calculations offered in this section:

Gain Setting	$\boldsymbol{R_{OUT}}$
$Maximum\ (0,31)$	$r_{o1,\max_{gain}}\left(g_{m,max}\frac{R_s}{2} + 1\right) \| \| r_{o5}$
$Minimum\ (15,16)$	$r_{o1,\max\_gain}\left(\frac{g_{m,max}}{2}\frac{R_s}{2} + 1\right) \| \| r_{o5}$

Table 4: VGCA output resistance versus gain settings with presence of source resistance

APPENDIX D

VGTA INPUT IMPEDANCE VARIATION WITH GAIN STATE AND LOAD RESISTANCE

The simplified schematic of the VGTA is repeated here for convenience:

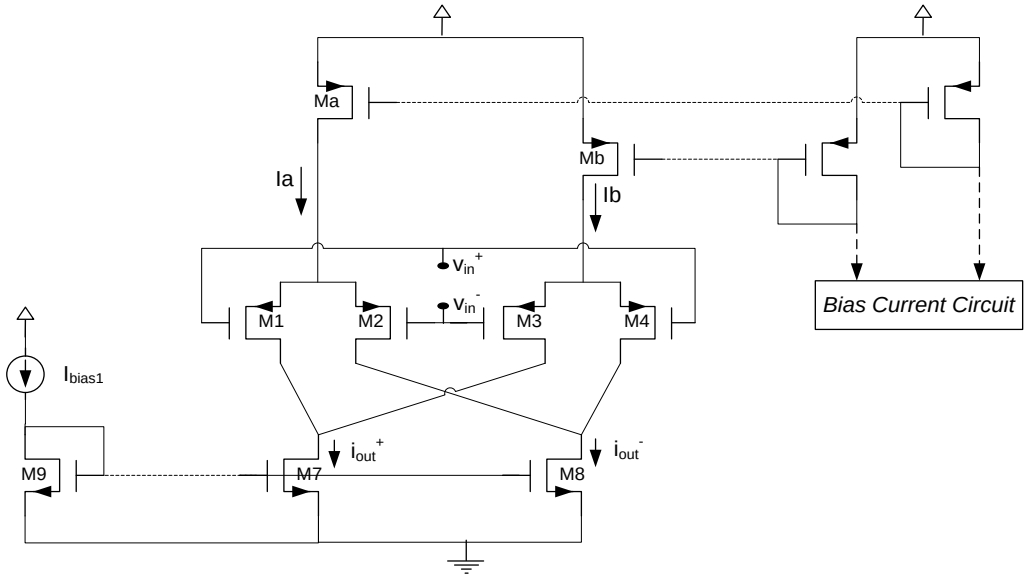

Figure 187: VGTA simplified circuit diagram

The CS configuration of the transconductance amplifier results in a high input impedance. The input impedance of the CS architecture is estimated using the small signal model shown below:

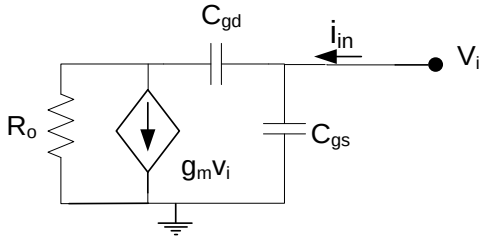

Figure 188: VGTA small signal model for input impedance calculation

$$Z_{in} \approx \frac{1}{[C_{gs} + (1 + g_m R_o) C_{gd}]s} \quad \text{(Eq. D.1)}$$

Input impedance of the VGTA is then approximated as follows:

$$Z_{in} \approx \frac{1}{\left[C_{gs1} + \left(1 + g_{m1}\frac{R_L}{2}\right) C_{gd1}\right]s} \| \frac{1}{\left[C_{gs4} + \left(1 + g_{m4}\frac{R_L}{2}\right) C_{gd4}\right]s} \quad \text{(Eq. D.2)}$$

$$Z_{in} \approx \frac{1}{\left[C_{gs1} + C_{gs4} + C_{gd1} + C_{gd4} + \frac{R_L}{2}\left(g_{m1} C_{gd1} + g_{m4} C_{gd4}\right)\right]s} \quad \text{(Eq. D.3)}$$

At maximum gain setting, with $I_b = 0$, transistors M_3 and M_4 are in cutoff, therefore $C_{gs4} \approx C_{gd4} \approx C_{ol}$ and $g_{m4} = 0$.[30] Transistors M_1 and M_2 are in saturation, which results in:

$$C_{gd1} \approx C_{ol}\,, g_{m1} = \sqrt{K I_{a,max}} = g_{m1,max} \quad \text{(Eq. D.4)}$$

$$Z_{in,maxgain} \approx \frac{1}{\left[C_{gs1} + 3C_{ol} + \frac{R_L}{2}\left(g_{m1,max} C_{ol}\right)\right]s} \quad \text{(Eq. D.5)}$$

At minimum gain setting, where all transistors are in saturation:

$$C_{gs1} \approx C_{gs4}, C_{gd1} \approx C_{gd4} \approx C_{ol} \quad \text{(Eq. D.6)}$$

$$g_{m1} = g_{m4} = \sqrt{K \frac{I_{a,max}}{2}} = \frac{g_{m1,max}}{\sqrt{2}} \quad \text{(Eq. D.7)}$$

Input impedance, then, for minimum gain settings becomes:

$$Z_{in,\min gain} \approx \frac{1}{\left[2C_{gs1} + 2C_{ol} + \frac{R_L}{2}\left(\sqrt{2} g_{m1,max} C_{ol}\right)\right]s} \quad \text{(Eq. D.8)}$$

[30] C_{ol} refers to the gate-diffusion overlap capacitance

APPENDIX E

VGTA OUTPUT RESISTANCE VARIATION WITH GAIN STATE

Referring to Figure 189 below:

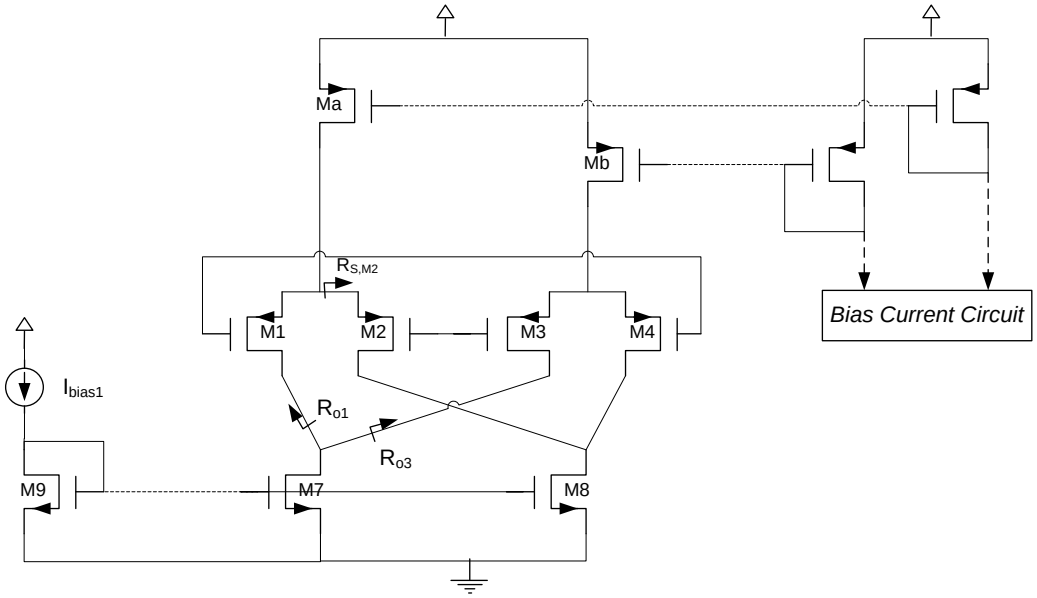

Figure 189: VGTA output resistance – effect of variable gain

$$R_{o1} = g_{m1} r_{o1} R_{s,M2} + r_{o1} + R_{s,M2} \approx r_{o1}\left(g_{m1} R_{s,M2} + 1\right) \quad \text{(Eq. E.1)}$$

$$R_{o3} = g_{m3} r_{o3} R_{s,M2} + r_{o3} + R_{s,M2} \approx r_{o3}\left(g_{m3} R_{s,M2} + 1\right) \quad \text{(Eq. E.2)}$$

$$R_o = r_{o7} || \, R_{o1} \, || R_{o3} \quad \text{(Eq. E.3)}$$

At maximum gain setting, assuming $r_{o2} = r_{o8}$, and $r_{o4} \approx \infty$:

$$R_{o1} = \frac{2}{\lambda_p I_{a,max}} \left(g_{m1} \frac{2}{g_{m2}} + 1 \right) \quad \text{(Eq. E.4)}$$

$$R_{o3} \approx \infty, g_{m1} = g_{m2} \quad \text{(Eq. E.5)}$$

$$R_{o,maxgain} = r_{o7} || \, R_{o1} = \frac{2}{\lambda_n I_{a,max}} || \frac{6}{\lambda_p I_{a,max}} \quad \text{(Eq. E.6)}$$

$$R_{o,maxgain} = \frac{6}{I_{a,max}(3\lambda_n + \lambda_p)} \quad \text{(Eq. E.7)}$$

At minimum gain setting, assuming $r_{o2} = r_{o4} = 2r_{o8}$:

$$R_{o1} = \frac{4}{\lambda_p I_{a,max}}\left(g_{m1}\frac{4}{3g_{m2}} + 1\right) \quad \text{(Eq. E.8)}$$

$$R_{o1} = R_{o3}, g_{m1} = g_{m2} \quad \text{(Eq. E.9)}$$

$$R_{o,mingain=} r_{o7} || R_{o1} || R_{o3} = \frac{2}{\lambda_n I_{a,max}} || \frac{14}{3\lambda_p I_{a,max}} \quad \text{(Eq. E.10)}$$

$$R_{o,mingain=} = \frac{14}{I_{a,max}(7\lambda_n + 3\lambda_p)} \quad \text{(Eq. E.11)}$$

Assuming $\lambda_n \approx \lambda_p$:

$$R_{o,maxgain} \approx \frac{15}{14} R_{o,mingain} \quad \text{(Eq. E.12)}$$

APPENDIX F

CALCULATION AND SIMULATION OF CMFB LOOP GAIN

F.1 Loop Gain Simulation Method

The CMFB circuits in VGAs and VVGAs are studied in this section. A feedback system is characterized by the forward integrator gain, A, and the feedback factor β as shown in figure below:

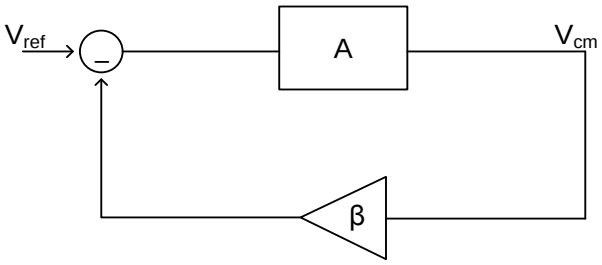

Figure 190: Simplified block diagram of CMFB circuits

It can be shown that the CMFB circuit's transfer function, or closed loop gain, is equal to:

$$\frac{v_{CM}}{v_{ref}} = \frac{\mathrm{A}}{1+\beta A} \qquad \text{(Eq. F.1)}$$

Where A is the open loop gain and βA is the loop gain of the CMFB. For large values of loop gain, the closed loop gain can be approximated as:

$$\frac{V_{CM}}{V_{ref}} = \frac{1}{\beta}\left(\frac{1}{1+\frac{1}{\beta A}}\right) \cong \frac{1}{\beta} \qquad \text{(Eq. F.2)}$$

(Eq. F.2) implies that a high loop gain results in a more precise closed loop gain of the feedback circuit and desensitizes the closed loop gain to variations in open loop gain.

To calculate the loop gain, the loop is broken at a high impedance node and a test source, v_t is placed in the direction of CMFB circuit's signal flow while the input source is shorted. The loop gain is then defined as the ratio of the returned signal to the test signal:

$$\beta A = -\frac{v_f}{v_t} \qquad \text{(Eq. F.3)}$$

An issue arises when attempting to simulate the loop gain by opening up the loop. Because the circuit is linearized around its DC operating point, opening up the loop could result in an offset in DC bias points of the circuit, thus producing skewed results. Inserting a voltage source in the signal path and breaking the loop, also, assumes that the resistance seen by the voltage source is much greater[31] than the impedance seen looking back into the network at the point of termination, otherwise producing an inaccurate loop gain estimate. One way to obtain an accurate loop gain measurement is to keep the loop closed while injecting two separate current and voltage test signals and obtaining the true loop gain using the independently measured current and voltage loop gains. [14] The figure below depicts the measurement setup to implement this method. The loop is opened in its feedback path and the appropriate test signals are injected as depicted in Figure 191 below:

---

[31] The impedance seen at the gate of M_{13} (Figure 22 on page 30) at low frequencies is much higher than the output resistance of the VGCA. At higher frequencies and for a large device, however, the impedance may become low enough to jeopardize accuracy of the stability analysis using a simple voltage source. The method offered here eliminates such inaccuracies, and is similar to the method used by Spectre simulator stability analysis tool to analyze stability of feedback loops. This argument also applies to CMFB circuits of VGTA and VVGAs.

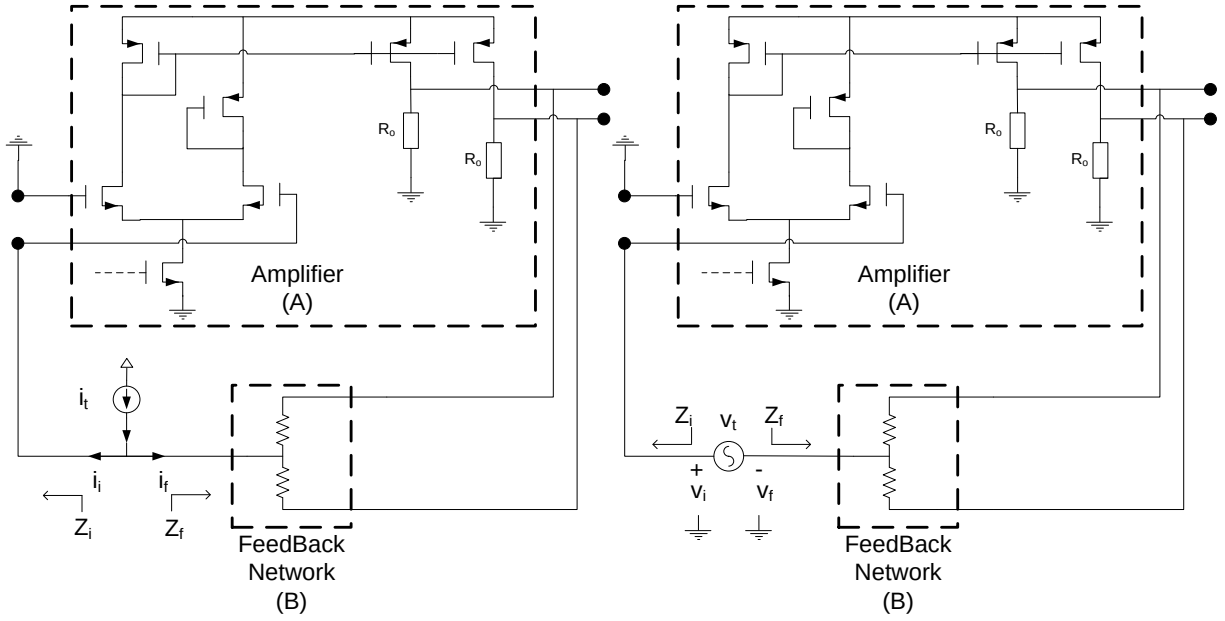

Figure 191: Calculation of VGCA CMFB loop gain using independent AC test current (Left) and voltage (Right) sources

On the left side figure, an AC test current source, i_t, is injected in the signal path. This current is split into a feedback i_f, and input i_i current. The current loop gain is then defined as:

$$T_i \equiv \frac{i_f}{i_i}(i/i) \qquad \text{(Eq. F.4)}$$

On the right side figure, an AC voltage source is inserted in the signal path and the voltage loop gain is defined as:

$$T_v \equiv -\frac{v_f}{v_i}(v/v) \qquad \text{(Eq. F.5)}$$

Loop gain, then, can be obtained as follows:

$$T = \frac{T_v T_i - 1}{2 + T_v + T_i} \approx T_v || T_i \qquad \text{(Eq. F.6)}$$

The current and voltage loop gain relation to the impedance seen looking into the input and feedback path is:

$$\frac{Z_f}{Z_i} = \frac{1 + T_v}{1 + T_i} \qquad \text{(Eq. F.7)}$$

The stability analysis of the spectre circuit simulator, which uses a slightly more advanced method to calculate the loop gain than presented here, is used to obtain the loop gain simulation results that are present in this thesis. [15]

F.2 VGCA CMFB Loop Gain Simulation Results – Comparison of Fabricated and Modified Designs

CMFB loop gain simulation results of the VGCA are compared here between the fabricated design and the modified design. The open and default load VGCA CMFB loop gain simulation results as fabricated are presented in Figure 192 below:

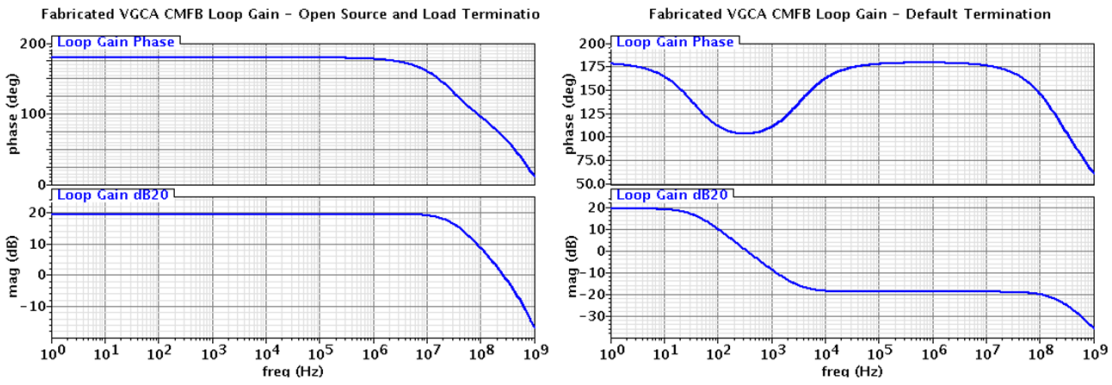

Figure 192: Fabricated VGCA CMFB loop gain with open source and load terminations (Left) and with AC coupled (2uF capacitor) and default source and load terminations (Right)

An additional low frequency pole and zero pair are introduced in the ac-coupled CMFB loop gain. The pole and zero locations are at:

$$p = \frac{1}{2\pi C_{dec}\left(R_o + (R_L/2)\right)} \quad \text{(Eq. F.8)}$$

$$z = \frac{1}{2\pi C_{dec}(R_L/2)} \quad \text{(Eq. F.9)}$$

Where R_o is the VGCA output resistance and R_L is the 50Ω estimated IF feed-line resistance. Referring to the output resistance schematic simulation results of Figure 117 on page 135, the approximate locations of the pole and zero are:

$$p = 93Hz, z = 3.1KHz \quad \text{(Eq. F.10)}$$

From the above figures it is evident that AC-coupled loading does not modify the DC-response of the loop, but reduces the high frequency CMFB loop gain. Common mode control, therefore, at DC is unaffected. This is true for all CMFB loop response plots that follow in this section.

The open and default load VGCA CMFB loop gain simulation results obtained from the new design are presented in Figure 193 below. CMFB loop gains of the modified and fabricated VGCA designs are almost identical:

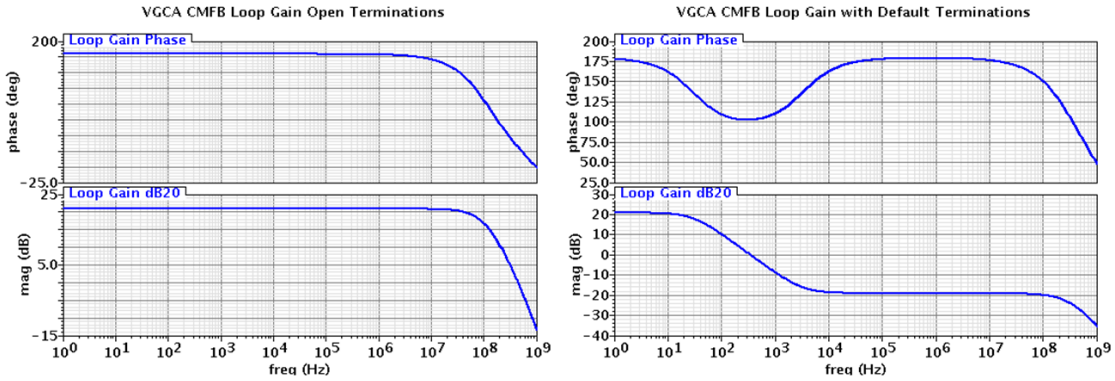

Figure 193: Modified VGCA CMFB loop gain with open source and load terminations (Left) and with AC coupled (2uF capacitor) and default source and load terminations (Right)

F.3 VGTA CMFB Loop Gain Simulation Results – Comparison of Fabricated and Modified Designs

Similarly to the VGCA, the CMFB Loop Gain of the VGTA for fabricated and new designs are compared here.

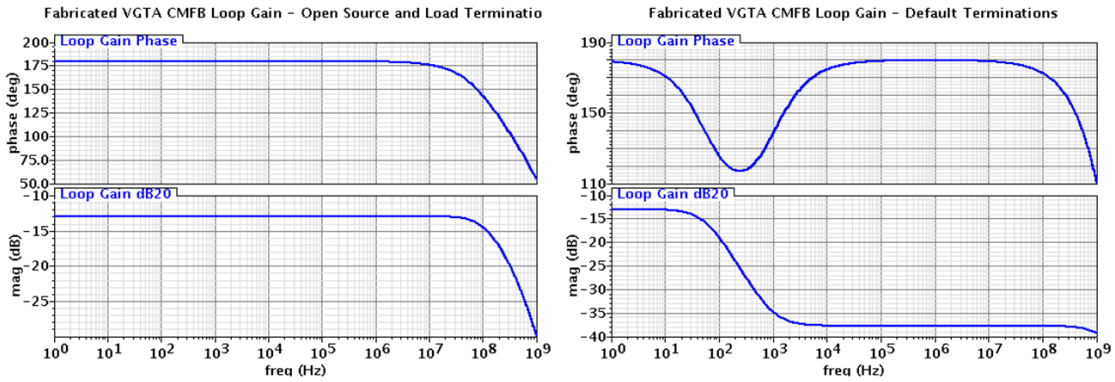

Figure 194 Fabricated VGTA CMFB loop gain with open source and load terminations (Left) and with AC coupled (2uF capacitor) and default source and load terminations (Right)

The VGTA CMFB Loop Gain, as fabricated, exhibits a large negative (in dB) gain at DC, therefore it is not able to effectively stabilize variations in common mode levels at the output. This problem is addressed in Appendix A and the modified design is

presented. The modified design offers $15dB$ of CMFB loop gain at low frequencies. Figure below shows the new CMFB Loop response:

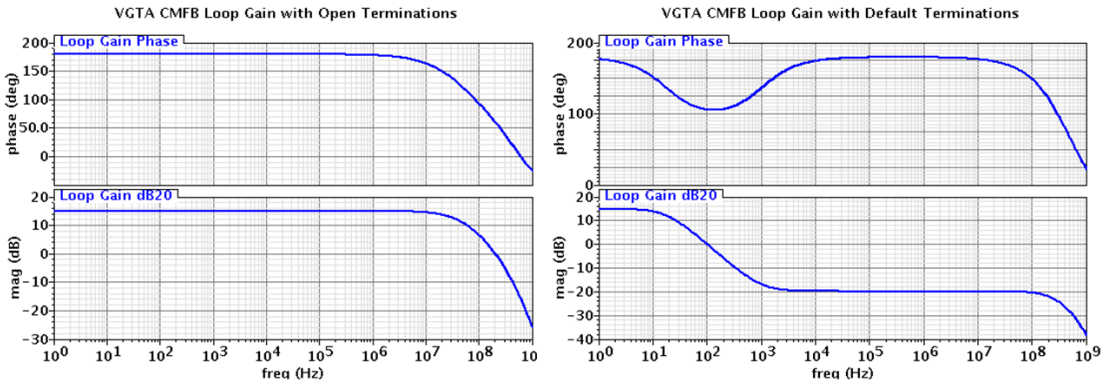

Figure 195: Modified VGTA CMFB loop gain with open source and load terminations (Left) and with AC coupled (2uF capacitor) and default source and load terminations (Right)

F.4 VVGCA CMFB Loop Gain Simulation Results – Comparison of Fabricated and Modified Designs

The VVGCA CMFB loop, as fabricated, exhibits a negative (in dB) loop gain due to presence of a design flaw. This issue is addressed in Appendix A and the modified design is presented. The figure below shows the VVGCA CMFB Loop Gain simulation results, as fabricated.

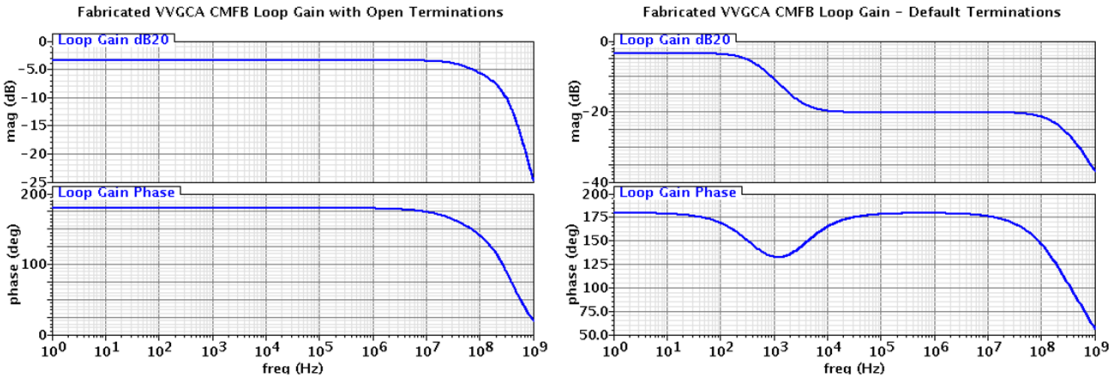

Figure 196: Fabricated VVGCA CMFB loop gain with open source and load terminations (Left) and with AC coupled (2uF capacitor) and default source and load terminations (Right)

In the modified design, the CMFB loop gain increases by $10dB$. The figure below depicts the new CMFB loop response:

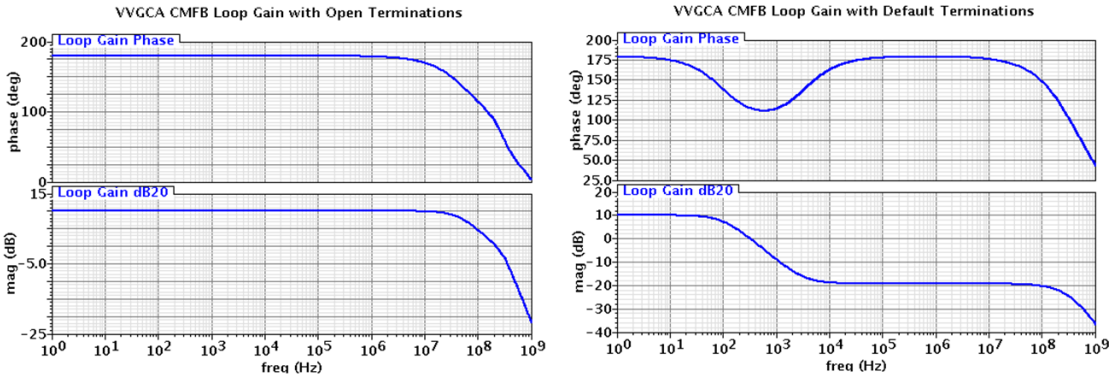

Figure 197: Modified VVGCA CMFB loop gain with open source and load terminations (Left) and with AC coupled (2uF capacitor) and default source and load terminations (Right)

F.5 VVGTA CMFB Loop Gain Simulation Results – Comparison of Fabricated and Modified Designs

Lastly, the CMFB loop gain of the VVGTA is compared between the fabricated and new design. Similar to the fabricated VVGCA, the fabricated VVGTA exhibits a

negative (in dB) CMFB loop gain at DC, implying no common mode signal regulation capability. This issue has been addressed in Appendix A and the modified design is presented. Figure below depicts the CMFB loop response of the fabricated VVGTA:

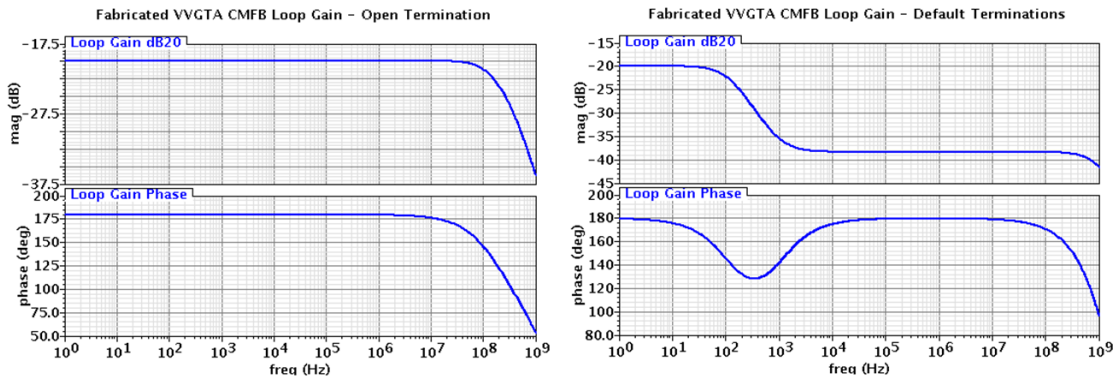

Figure 198: Fabricated VVGTA CMFB loop gain with open source and load terminations (Left) and with AC coupled (2uF capacitor) and default source and load terminations (Right)

The modified VVGTA exhibits a $10dB$ loop gain at DC. Figure 199 below depicts the CMFB loop response of the modified VVGTA:

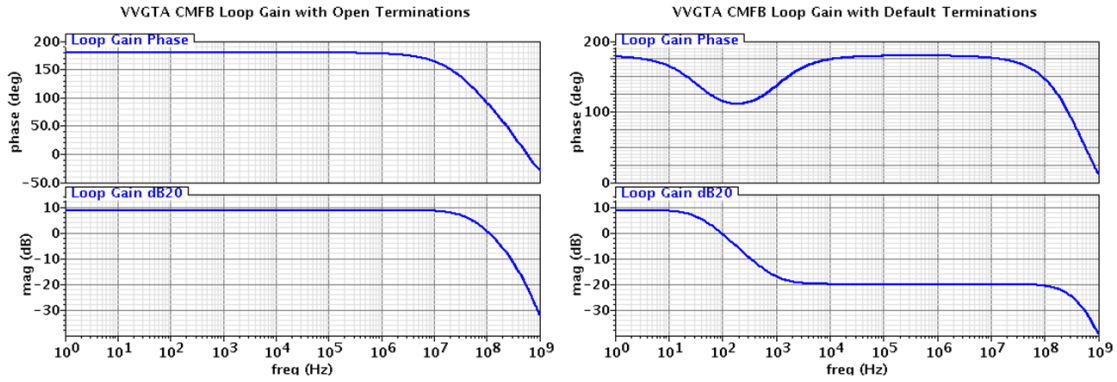

Figure 199: Modified VVGTA CMFB loop gain with open source and load terminations (Left) and with AC coupled (2uF capacitor) and default source and load terminations (Right)

APPENDIX G

CIRCUIT SCHEMATICS

Schematics of modified VGCA, VGTA, Bi-directional VGA, and VVGA as well as schematics of fabricated Bi-directional VGA and VVGA are presented in this appendix.

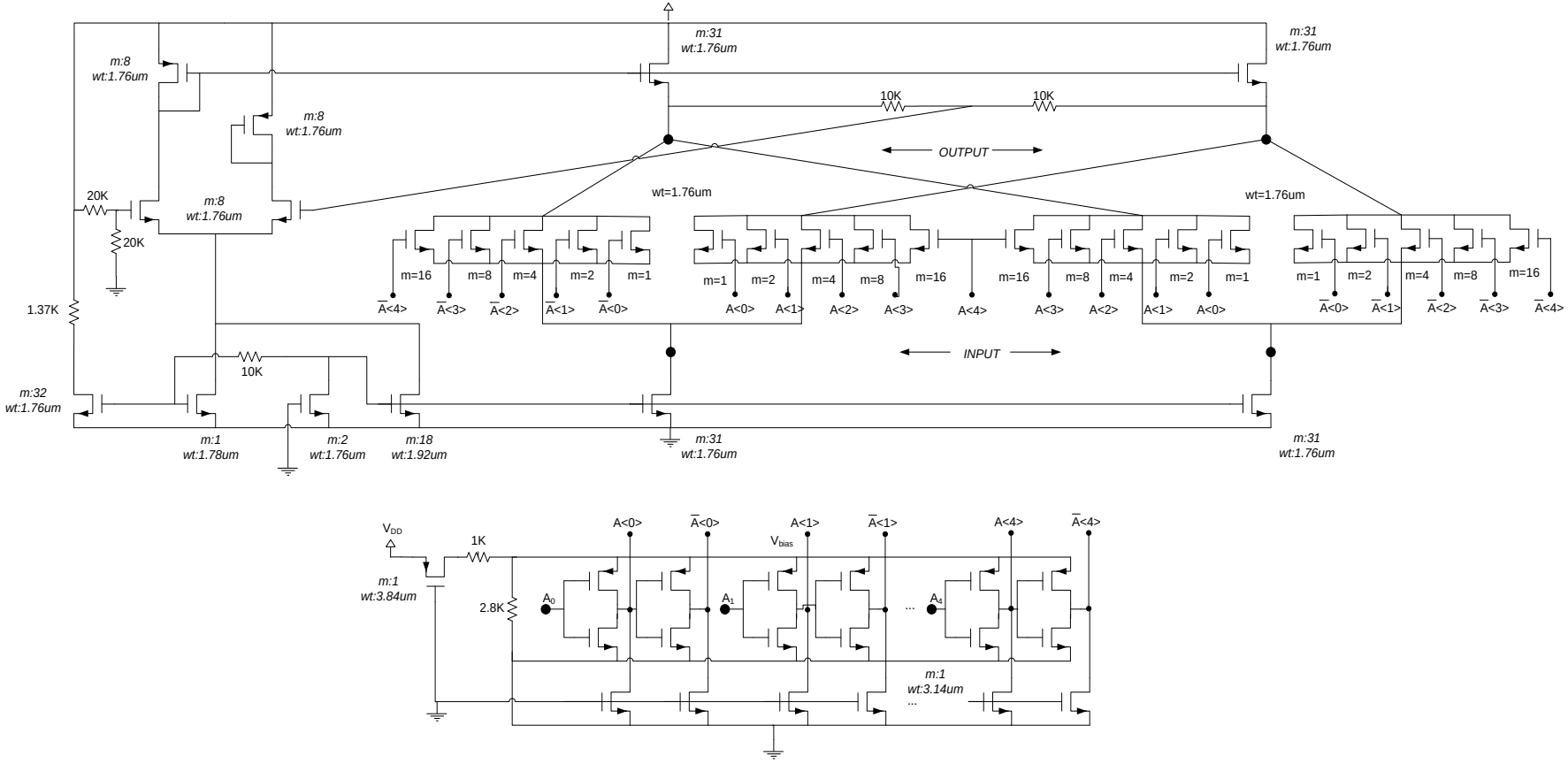

Figure 200: Modified VGCA schematic (not fabricated). Simulation results for this design are presented in Chapter 2.

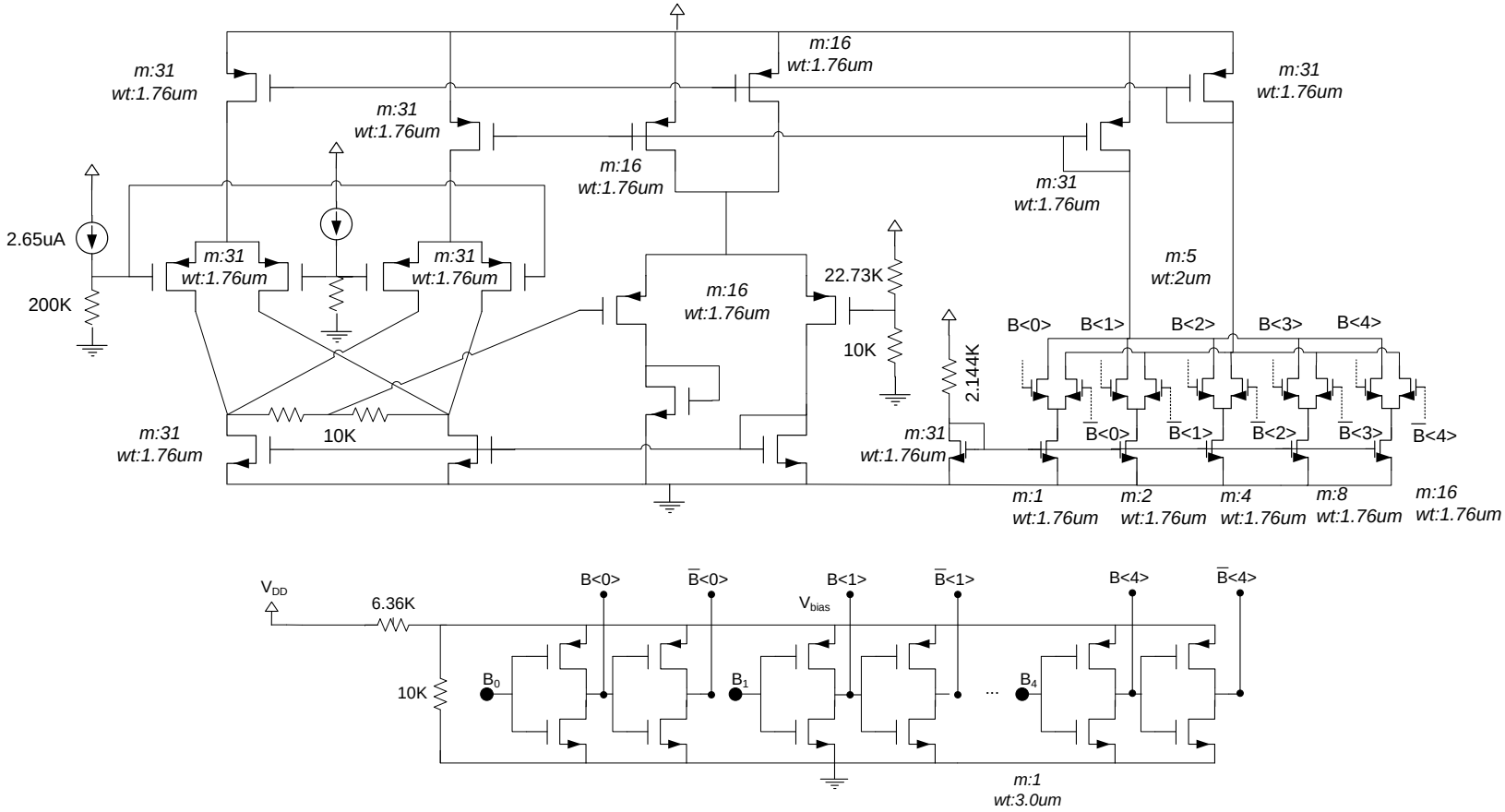

Figure 201: Modified VGTA schematic (not fabricated). Simulation results for this design are presented in Chapter 2.

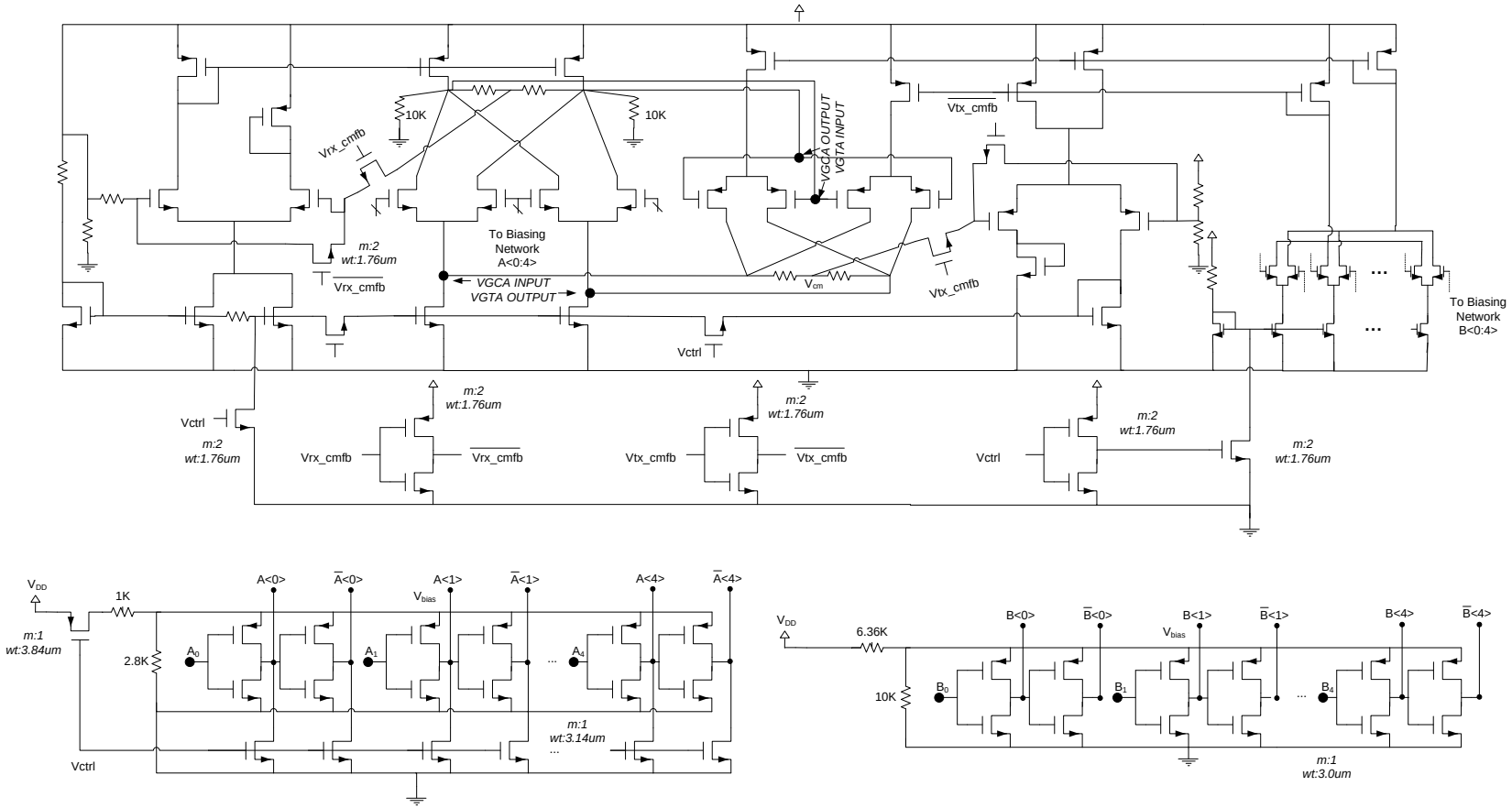

Figure 202: Modified VGA schematic (not fabricated). Simulation results for this design are presented in Chapter 3.

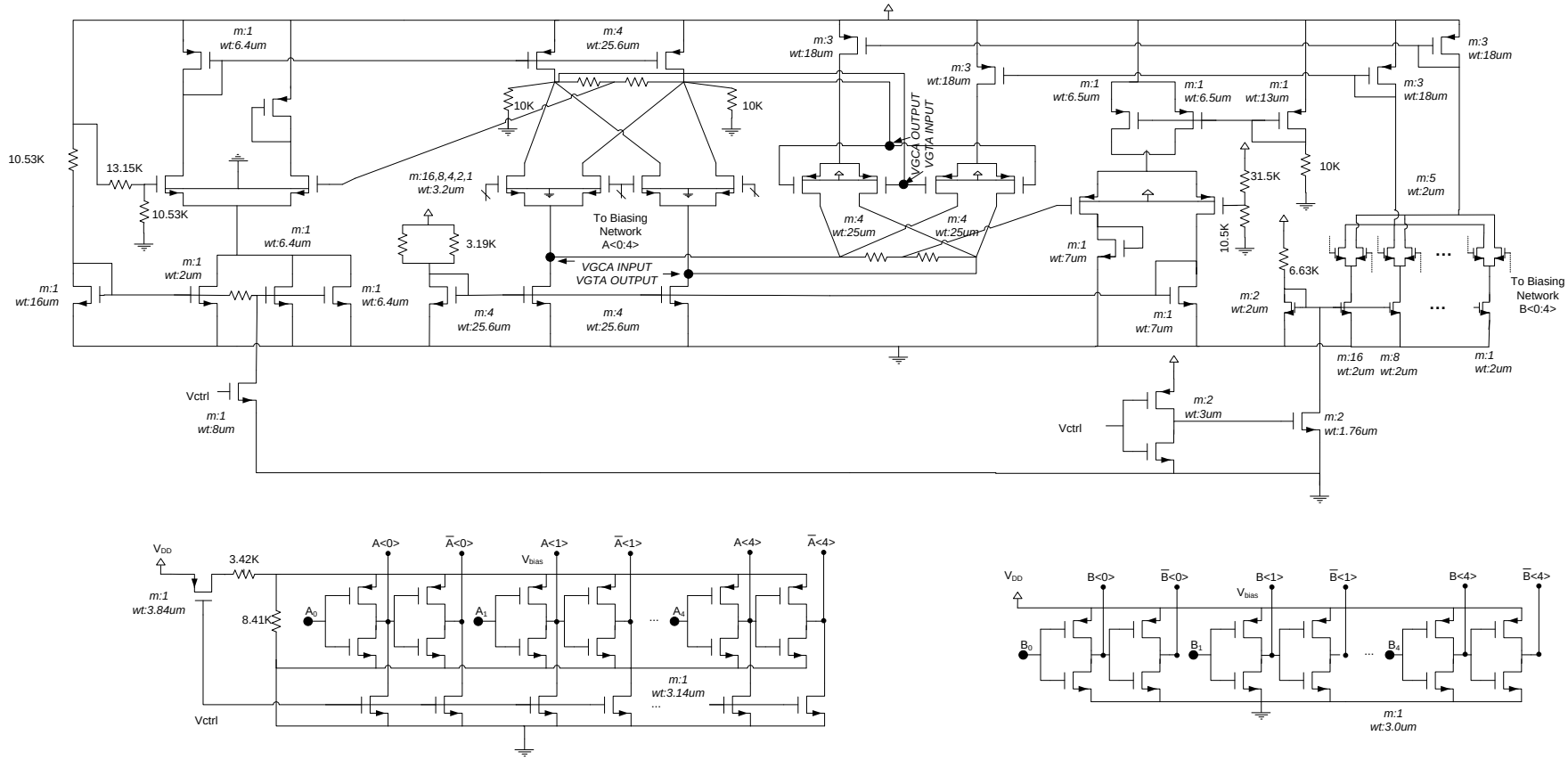

Figure 203: VGA original design (fabricated). Simulation results for this design are presented in Chapters 5 and 6.

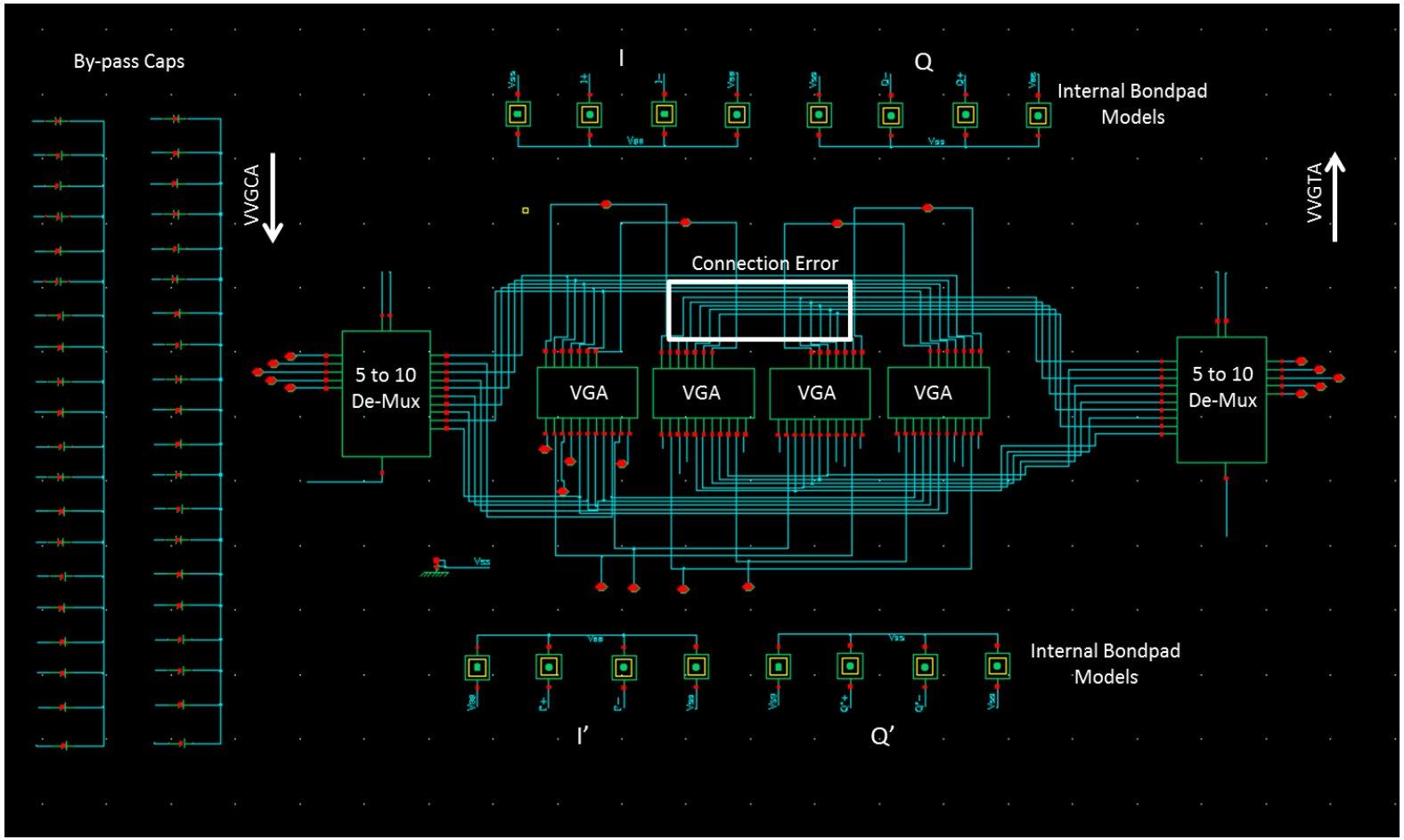

Figure 204: VVGA original design (fabricated). Simulation results for this design are presented in Chapters 5 and 6.

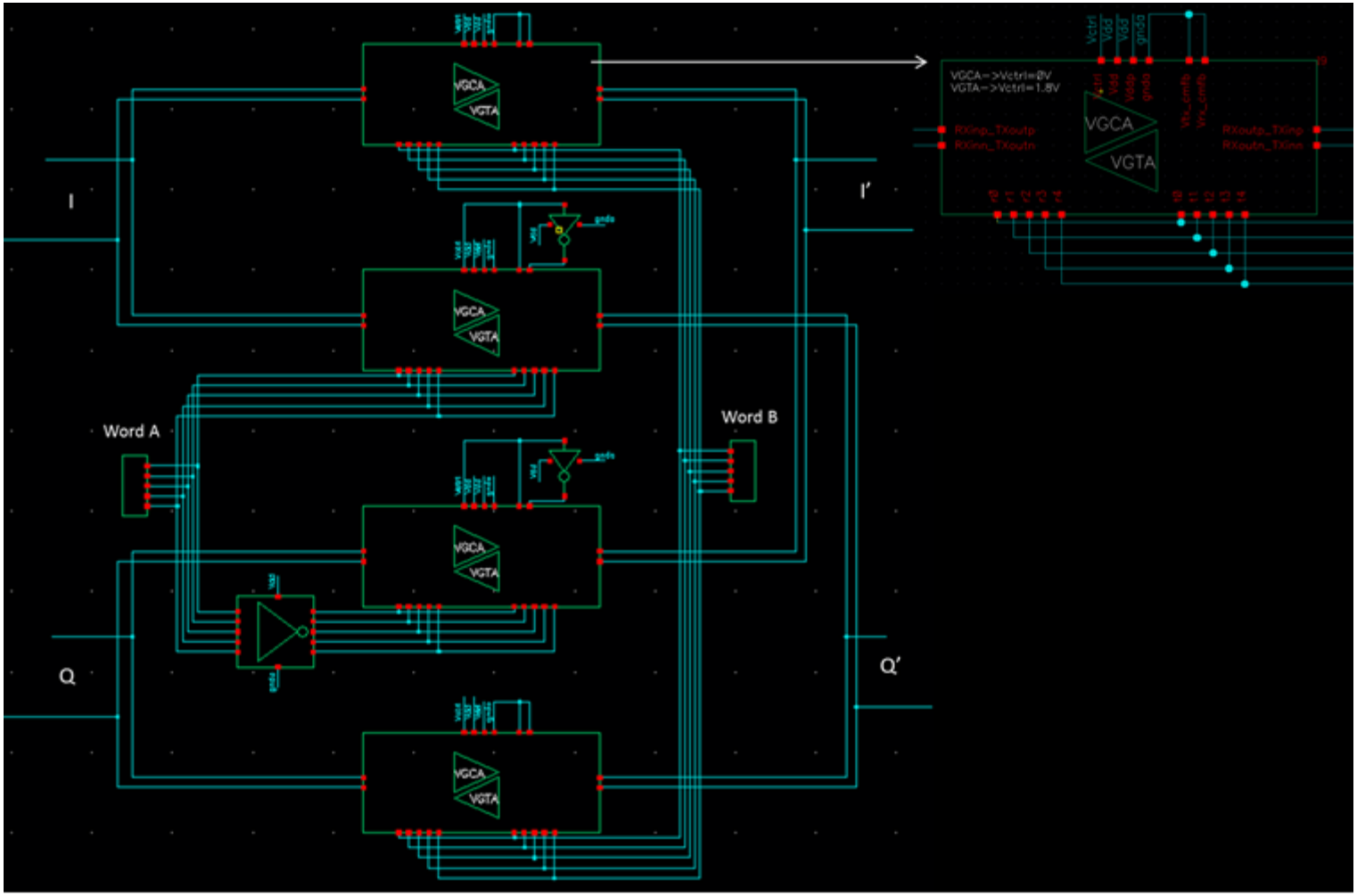

Figure 205: Modified VVGA schematic (not fabricated). Simulation results for this design are presented in Chapter 4.

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