# HIGH PERFORMANCE SILVER DIFFUSIVE MEMRISTORS FOR FUTURE COMPUTING 

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# High Performance Silver Diffusive Memristors For Future Computing 

A Thesis Presented
by

RIVU MIDYA

Submitted to the Graduate School of the University of Massachusetts Amherst in partial
fulfillment of the requirements for the degree of MASTER OF SCIENCE IN ELECTRICAL AND COMPUTER ENGINEERING

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Electrical and Computer Engineering
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# High Performance Silver Diffusive Memristors For Future Computing 

## A Thesis Presented

By

## RIVU MIDYA

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## DEDICATION

To my parents

## ACKNOWLEDGEMENTS

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# ABSTRACT <br> HIGH PERFORMANCE SILVER DIFFUSIVE MEMRISTORS FOR FUTURE COMPUTING 

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Sneak path current is a significant remaining obstacle to the utilization of large crossbar arrays for non-volatile memories and other applications of memristors. A two-terminal selector device with an extremely large current-voltage nonlinearity and low leakage current could solve this problem. We present here a Ag/oxide-based threshold switching (TS) device with attractive features such as high current-voltage nonlinearity $\left(\sim 10^{10}\right)$, steep turn-on slope (less than 1 $\mathrm{mV} / \mathrm{dec}$ ), low OFF-state leakage current ( $\sim 10^{-14} \mathrm{~A}$ ), fast turn ON/OFF speeds ( $<75 / 250 \mathrm{~ns}$ ), and good endurance ( $>10^{8}$ cycles). The feasibility of using this selector with a typical memristor has been demonstrated by physically integrating them into a multilayered 1S1R cell. Structural analysis of the nanoscale crosspoint device suggests that elongation of a Ag nanoparticle under voltage bias followed by spontaneous reformation of a more spherical shape after power off is responsible for the observed threshold switching of the device. Such mechanism has been quantitatively verified by the Ag nanoparticle dynamics simulation based on thermal diffusion assisted by bipolar electrode effect and interfacial energy minimization.

Keywords: threshold switching, resistive switching, memristor, selector, transmission electron microscopy

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## CHAPTER I

# HIGH PERFORMANCE SILVER DIFFUSIVE MEMRISTORS FOR FUTURE COMPUTING 

## A. Introduction

Memristors are promising candidates for both neuromorphic computing and next generation non-volatile memory applications ${ }^{1-7}$ because of their scalability ${ }^{3,8}$, 3D stacking potential $^{9-11}$, and a close resemblance to the operating characteristics of synapses ${ }^{1,4,7,12,13}$. These applications typically require a large crossbar array of memristors, in which sneak path currents from neighboring cells during a write or read of a target cell can severely impede the proper operation of the array. Numerous access devices coupled with a memristor at each crosspoint of the array have been introduced to tackle this critical issue ${ }^{14-16}$. Among those devices, a twoterminal thin-film-based selector may address the issue without compromising the scalability and 3D stacking capability of the memristor. A low OFF-current and a high selectivity of the selector are crucial to enable large crossbar arrays.

Examples of conventional two-terminal thin-film based selectors include Schottky diodes ${ }^{17}$, tunneling junctions ${ }^{18,19}$, ovonic threshold switches (OTS) ${ }^{20-23}$ and metal-insulator transitions (MIT) ${ }^{24-28}$. Kim et al. has demonstrated $32 \times 32$ crossbar array composed of a stacked Schottky diode and a unipolar memristor. ${ }^{17}$ We also have recently demonstrated a highly repeatable selector based on a crested tunnel barrier with essentially unlimited endurance, ${ }^{19}$ but the $10^{5}$ nonlinearity obtained in these tunneling selectors may still not be sufficient for applications where ultra-large arrays are needed. Other selectors, such as mixed-ionic-electronic conduction (MIEC) ${ }^{29-31}$ and $\mathrm{FAST}^{29,30}$ have been reported with attractive performance but undisclosed materials. The concept of using engineered materials by doping fast diffusive species
into dielectrics has recently been introduced ${ }^{32}$ and demonstrated with improved nonlinearity and transition slope ${ }^{33-37}$. However, high operating current (e.g. $>100 \mu \mathrm{~A}$ ) and fast OFF-switching speed (e.g. < 500 ns ) of this type of selectors have not yet been unambiguously demonstrated. Moreover, the operation mechanism, especially the RESET process in which devices relax back from their ON state to the OFF state under zero voltage bias, remains unclear. Although hypotheses based on Rayleigh instability, electronic tunneling, and opposing chemical/mechanical force has been proposed for Ag and Cu based systems to explain the underlying RESET transition, a detailed experimental study of the microstructure and composition of the conducting channel responsible for the volatile switching is still lacking. ${ }^{33,38,}$ 39

We report here a new symmetric bidirectional threshold switching selector device with features including high selectivity of $10^{10}$, steep turn on slope of $<1 \mathrm{mV} / \mathrm{dec}$, high endurance beyond $10^{8}$ cycles and fast ON/OFF switch speed within $75 / 250 \mathrm{~ns}$. The selector has been experimentally stacked on top of a $\mathrm{Pd} / \mathrm{Ta}_{2} \mathrm{O}_{5} / \mathrm{TaO}_{x} / \mathrm{Pd}$ memristor to form an integrated 1 S 1 R cell.

Microscopic analysis of a nanoscale device reveals discontinuous Ag nanostructures in a device after switching along with noticeable structural deformation and nanocrystalline $m-\mathrm{HfO}_{2}$. A numerical switching model based on the thermal diffusion aided with bipolar electrode effects and Gibbs-Thomson effect or minimization of interfacial energy has been developed to quantitatively interpret the observed switching difference between asymmetric $\mathrm{Pd} / \mathrm{HfO}_{\mathrm{x}} / \mathrm{Ag}$ and symmetric $\mathrm{Pd} / \mathrm{Ag}^{2} / \mathrm{HfO}_{x} / \mathrm{Ag} / \mathrm{Pd}$ threshold devices.

## B. Thesis Statement

The objective of my thesis is to explore a new material system and evaluate the feasibility of it being used in solving real world problems preventing memristors from replacing conventional memory.

## C. Approach/Methods

Two different structures are to be studied. The first one is $\mathrm{Pd} / \mathrm{HfOx} / \mathrm{Ag}$ while the second one is $\mathrm{Pd} / \mathrm{HfOx} / \mathrm{Ag} / \mathrm{Pd}$. After fabrication, electrical characterization has been performed. The maximum current during operation was externally controlled using the B1500 Semiconductor Parameter Analyzer. The yield of the devices was calculated.

The switching dynamics of the devices were investigated then by applying fast pulses using the B1530 Waveform Generator. A statistical study was done of the devices by noticing their turn on(delay) times as well as their turn off(relaxation) times. In addition to this, the endurance of the devices was measured in order to determine the number of successful pulse switching over time.

A vertically integrated device was then fabricated using a $\mathrm{Pd} / \mathrm{HfOx} / \mathrm{Ag} / \mathrm{Pd}$ selector and a $\mathrm{Pd} / \mathrm{Ta} 2 \mathrm{O} 5 / \mathrm{TaOx} / \mathrm{Pd}$ memristor with the Pd electrode as a common middle electrode. The 1S1R cell was investigated and electrically characterized.

To get a deeper insight into the mechanism involved in switching of the devices, a High Resolution Transmission Electron Microscope(HRTEM) image was captured. In addition, a Electron Dispersive Spectroscopy(EDS) was performed on the sample to generate an elemental map.

These experiments went a long way in evaluating the feasibility of using these selectors for memory-related applications.

## D. Results and Discussion

The $\mathrm{Pd} / \mathrm{HfOx} / \mathrm{Ag}$ devices were prepared and were electrically characterized. The asprepared $\mathrm{Pd} / \mathrm{HfO}_{\mathrm{x}} / \mathrm{Ag}$ MIM junctions were in their high resistance state (HRS) or OFF-state. The OFF resistance of the as-prepared device was about $10^{13}$ ohms at 0.1 V . The device needed to be electroformed at 1.8 V and a $1 \mu \mathrm{~A}$ compliance current had to applied in order to make it operational. The current of the device increased abruptly, but then returned to the HRS while sweeping the voltage back to zero. In the next positive sweep after electroforming process, the device switched ON at a much lower voltage ( 0.4 V ). Fig. 1(b) presents 100 consecutive cycles of such Threshold Switching(TS) behavior. The device could conduct surprisingly high current levels of 1 mA while still retaining volatile behavior. The HRS notch around 0.06 V in Figure 1 (b) corresponds to a negative current that can be attributed to the nano-battery effect ${ }^{40}$. By setting the read voltage $\left(\mathrm{V}_{\text {read }}\right)$ to 0.2 V and the half-read voltage $\left(\mathrm{V}_{\text {read }} / 2\right)$ to 0.1 V , the 100 switching cycles in Figure 1 (b) yield a selectivity of $\sim 10^{10}$ in terms of the median currents at the two voltages and a maximum selectivity of $6 \times 10^{11}$, which is one of the highest reported in any type of selector so far ${ }^{29,30}$. The turn-ON slope was $<1 \mathrm{mV} /$ decade, which is also the sharpest reported so far ${ }^{34}$. Symmetrical bi-directional volatile switching was observed in a structurally symmetric $\mathrm{Pd} / \mathrm{Ag} / \mathrm{HfO}_{\mathrm{x}} / \mathrm{Ag} / \mathrm{Pd}$ stack, as shown in Fig. 1(c) where devices show no noticeable deterioration after 100 cycles. Both devices feature a low OFF current of $10^{-14} \mathrm{~A}$ (at 0.1 V ), which is also the lowest reported so far. ${ }^{33}$ All devices have shown repeatable threshold switching with mean
threshold voltages spanning from -0.5 V to -0.3 V and 0.4 V to 0.7 V , for negative and positive polarities respectively. (Fig. 2(a-c))


Figure $1 \mathrm{HfO}_{\mathrm{x}}$ based TS devices showing threshold switching with a large ON/OFF ratio and a steep slope. (a) Schematics of the asymmetric and symmetric device structures. The inset shows an SEM image of the crosspoint device. (b) The DC I-V characteristic of the $\mathrm{Pd} / \mathrm{HfO}_{\mathrm{x}} / \mathrm{Ag}$ selector yields a selectivity of $10^{11}$. (c) Consecutive 50 cycles of DC voltage sweep with positive biasing followed by 50 cycles of DC sweep with negative biasing on $\mathrm{Pd} / \mathrm{Ag} / \mathrm{HfO}_{x} / \mathrm{Ag} / \mathrm{Pd}$
showing bipolar threshold switching behavior with an ON/OFF ratio of $10^{8}$ (d) Device shows an ON switching slope of $\sim 1 \mathrm{mV} /$ decade.


Figure 2 (a) 50 DC I-V sweeps on either positive and negative biasing polarities of ten randomly chosen $\mathrm{Pd} / \mathrm{Ag} / \mathrm{HfO}_{\mathrm{x}} / \mathrm{Ag} / \mathrm{Pd}$ selectors on the same wafer. (b) (c) Threshold voltage ( $\mathrm{V}_{\text {th }}$ ) distributions of the ten devices in (a). The threshold voltage is defined as the voltage at which differential conductance is maximum.

The fastest switching observed in these devices exhibited a transition from high resistance state (HRS) to a low resistance state (LRS) within 75 ns when a 2 V pulse was applied, which is comparable to that of a typical memristor, ${ }^{10}$ and relaxation back to the HRS within 250 ns after the bias was removed, as indicated by Fig. 3(a). Note that the turn-ON time could be shorter than 75 ns with a pulse of a higher magnitude, given that the turn-ON time is inversely proportional to the exponential of the amplitude of the driving voltage pulse as reported for

CBRAM ${ }^{41}$. The device exhibited an endurance over a hundred million cycles. Fig. 3(b) shows the endurance testing result that was acquired using $10 \mu \mathrm{~s} / 4 \mathrm{~V}$ programming pulses and 75 $\mu \mathrm{s} / 0.1 \mathrm{~V}$ read pulses, with a $25 \mu \mathrm{~s}$ wait time in between each write and read event (see the inset of Fig. 3(b)). The delay time follows a distribution at a given voltage and hence an elongated pulse was employed for the endurance test to minimize the unsuccessful switching events. (Fig. 4(a)). In addition, relaxation time typically maintains a linear relationship with the pulse width. (Fig. 4(b)). The threshold switching at an elevated temperature displays an increased OFF state current due to thermal facilitated transport. ${ }^{30,42,43}$ (Fig. 5(a-b)) The relaxation time (or equivalently the retention time) of the $\mathrm{Pd} / \mathrm{Ag} / \mathrm{HfO}_{x} / \mathrm{Ag} / \mathrm{Pd}$ selectors follows a typical exponential relationship with the reciprocal temperature (Fig. 5(c)), yielding a fitted Ag hopping barrier of 0.21 eV , which is close to that in a Ag doped silicon oxynitride. ${ }^{44}$

We fabricated a vertically integrated cell consisting of a $\mathrm{Pd} / \mathrm{Ag} / \mathrm{HfO}_{x} / \mathrm{Ag} / \mathrm{Pd}$ threshold switch on top of a $\mathrm{Pd} / \mathrm{Ta}_{2} \mathrm{O}_{5} / \mathrm{TaO}_{x} / \mathrm{Pd}$ memristor with a Pd layer as a shared middle electrode (ME), as shown in a scanning electron micrograph for a top view and a transmission electron micrograph for a focused ion beam cut cross-section (Fig. 6(a)). We also performed a EDS(Energy Dispersive Spectroscopy)(Fig. 6(b)) to confirm the chemical composition of the focused ion beam cut cross section. It is to be noted that the TA peak of Pd and Pt overlap. The dedicated middle electrode allowed us to access the characteristics of the selector, the memristor and the 1S1R cell, separately. Electrical DC voltage sweeps had been applied to the individual $\mathrm{Pd} / \mathrm{Ag}^{2} / \mathrm{HfO}_{\mathrm{x}} / \mathrm{Ag} / \mathrm{Pd}$ threshold selector, as shown in Figure 6(c). The selector showed repeatable threshold switching with both biasing polarities. Repeatable bipolar memristive switching of the individual $\mathrm{Pd} / \mathrm{Ta}_{2} \mathrm{O}_{5} / \mathrm{TaO}_{x} / \mathrm{Pd}$ memristor is illustrated in Figure 6(d). Figure 6(e) shows the DC voltage sweep response of the integrated 1 S 1 R . The $\mathrm{Pd} / \mathrm{Ag} / \mathrm{HfO}_{\mathrm{x}} / \mathrm{Ag} / \mathrm{Pd}$ threshold switch acted
as a select device in this case, with the capability of greatly suppressing sneak current in large arrays.


Figure 3 Switching speed and endurance performance of the bipolar $\mathrm{Pd} / \mathrm{Ag} / \mathrm{HfO}_{\mathrm{x}} / \mathrm{Ag} / \mathrm{Pd}$ selectors. (a) The device is turned on within 75 ns and relaxes back to HRS within 250 ns. (b) Endurance of the selector with over $10^{8}$ cycles. The inset shows the waveform employed in endurance measurement which consists of a $10 \mu \mathrm{~s}$ pulse with an amplitude of 4 V for ON
switching followed by a 0.1 V read pulse. The time interval between switching pulses is $100 \mu \mathrm{~s}$ ( $25 \mu$ s waiting time plus $75 \mu$ s read time).


Figure 4 (a) Typical histogram plot of the relaxation time of the $\mathrm{Pd} / \mathrm{Ag} / \mathrm{HfO}_{\mathrm{x}} / \mathrm{Ag} / \mathrm{Pd}$ selector extracted from 50 measurements. The applied pulse width and voltage in each independent measurement were $50 \mu$ s and 4 V , respectively (b) The general trend in the variation of relaxation time as a function of pulse width. The amplitude of the pulse and reading pulse are 1.5 V and 0.1 V , respectively.

With increasing voltage, the selector first turned on at $\sim 0.5 \mathrm{~V}$ followed by the SET transition of the $\mathrm{Pd} / \mathrm{Ta}_{2} \mathrm{O}_{5} / \mathrm{TaO}_{x} / \mathrm{Pd}$ memristor at $\sim 1.2 \mathrm{~V}$. The subsequent reading sweep with the same single sweep (purple curve) verified the LRS of the memristor. During the negative voltage sweep, the threshold selector turned on at $\sim-0.4 \mathrm{~V}$ followed by a gradual RESET transition of the $\mathrm{Pd} / \mathrm{Ta}_{2} \mathrm{O}_{5} / \mathrm{TaO}_{\mathrm{x}} / \mathrm{Pd}$ memristor in the interval from $\sim-0.8 \mathrm{~V}$ to $\sim-1.4 \mathrm{~V}$. (See the blue curve) The following reading sweep (magenta curve) again verified the HRS of the memristor. Similar electrical performances had also been demonstrated on wire-joined 1S1R system consisting of discrete $\mathrm{Pd} / \mathrm{Ag} / \mathrm{HfO}_{x} / \mathrm{Ag} / \mathrm{Pd}$ threshold selector and the same kind of $\mathrm{Pd} / \mathrm{Ta}_{2} \mathrm{O}_{5} / \mathrm{TaO}_{\mathrm{x}} / \mathrm{Pd}$
memristors. It should also be noted that the threshold voltage to turn on a $\mathrm{Pd} / \mathrm{Ag} / \mathrm{HfO}_{\mathrm{x}} / \mathrm{Ag} / \mathrm{Pd}$ threshold switch with a given voltage pulse is a function of the pulse width.


Figure 5 Repeatable DC threshold switching I-V characteristics of the $\mathrm{Pd} / \mathrm{Ag} / \mathrm{HfO}_{\mathrm{x}} / \mathrm{Ag} / \mathrm{Pd}$ device at elevated temperature of (a) $85^{\circ} \mathrm{C}$ (b) $145^{\circ} \mathrm{C}$. (c) Relaxation or retention time dependence on the reciprocal temperature. The activation energy for the material system is calculated to be 0.21 eV .

The shorter the pulse width used, the larger the switching voltage needed. (See for example, Figure 2) Thus, the threshold voltages for the selectors using fast pulses are higher than those above values obtained from the quasi-DC switching sweeps. Pulse switching followed by DC sweep reading of the memristor states has also been carried out. As shown in Fig. 7(a), the
integrated 1S1R was switched by applying a $500 \mu$ s pulse with 2 V amplitude. Subsequent DC reading sweeps in Fig. 7(b) with up to 0.5 V amplitude


Figure 6 Electrical performance of an integrated 1S-1R device consisting of a
$\mathrm{Pd} / \mathrm{Ta}_{2} \mathrm{O}_{5} / \mathrm{TaO}_{\mathrm{x}} / \mathrm{Pd}$ memristor and a $\mathrm{Pd} / \mathrm{Ag}^{2} / \mathrm{HfO}_{\mathrm{x}} / \mathrm{Ag} / \mathrm{Pd}$ selector. (a) Scanning electron micrograph top view of the vertically integrated selector and memristor (left) and transmission electron micrograph of the cross-section prepared by focused ion beam cutting. (b) Elemental mapping of the sample done using EDS (c) Repeatable bipolar threshold switching of the individual $\mathrm{Pd} / \mathrm{Ag} / \mathrm{HfOx} / \mathrm{Ag} / \mathrm{Pd}$ selector. (d) Repeatable bipolar memristive switching of the individual $\mathrm{Pd} / \mathrm{Ta}_{2} \mathrm{O}_{5} / \mathrm{TaO}_{\mathrm{x}} / \mathrm{Pd}$ memristor. (e) DC I-V characteristics of the vertically integrated selector and memristor. The selector turned on at $\sim 0.5 \mathrm{~V}$ (blue curve), followed by the SET of the memristor at $\sim 1.2 \mathrm{~V}$. The LRS of memristor was verified by the subsequent sweep (purple curve). On the negative voltage, the selector turned on at $\sim-0.4 \mathrm{~V}$ (red curve) before the memristor

RESET in the interval from $\sim-0.8 \mathrm{~V}$ to $\sim-1.2 \mathrm{~V}$. The followed sweep verified the HRS of the memristor (magenta curve).
didn't turn ON the selector. The 0.7 V reading sweep turned the selector ON and yielded a current $\sim 150 \mu \mathrm{~A}$ at 0.7 V. In Fig. 7(c), a $500 \mu \mathrm{~s}$ pulse with -2 V amplitude was applied to the integrated 1S1R cell, showing an abrupt current drop due to memristor RESET. The subsequent reading sweeps with up to -0.6 V amplitudes didn't turn the selector ON . The -0.8 V sweep turned the selector ON and yielded a current of $\sim 10 \mu \mathrm{~A}$, which suggests that the memristor was in its OFF state.


Figure 7 Validation of the memristor resistance after pulse switching (a) A $500 \mu$ s pulse with 2 V amplitude was applied to SET the memristor. (b) The subsequent reading sweeps didn't turn the selector ON until the 0.7 V sweep which showed $\sim 150 \mu \mathrm{~A}$ current at 0.7 V biasing indicating the ON state of the memristor. (c) A $500 \mu$ s pulse with -2 V amplitude was applied to RESET the
memristor. (d) The subsequent reading sweeps didn’t turn the selector ON until the -0.8 V sweep which showed current $\sim 10 \mu \mathrm{~A}$ at -0.8 V indicating the OFF state of the memristor.

To unravel the underlying mechanism of the volatile switching, nanoscale crosspoint junctions with an electrode width of 100 nm were fabricated for high resolution transmission electron microscopy (HRTEM) analysis (Fig. 8). The TEM sample was prepared to cover the entire nanodevice to minimize the possibility of missing important features responsible for the switching behavior. The nanoscale $\mathrm{Pd} / \mathrm{Ag}_{\mathrm{g}} / \mathrm{HfO}_{\mathrm{x}} / \mathrm{Ag} / \mathrm{Pd}$ crosspoint device demonstrated similar threshold switching characteristics to the microdevices prepared by photolithography, and withstand an ON-state current of $100 \mu \mathrm{~A}$ (Figure 9). In order to observe the evolution of the microstructures, Figure 8(c) and (d) show two cross-sections of nanoscale junctions of an asdeposited device and an electrically operated device that exhibited repeated volatile switching as shown in Figure 8(b). The metal/dielectric interface in the operated device was rougher than that of the as-deposited device, a possible result of grain growth in the electrodes induced by Joule heating. ${ }^{45}$ In addition, the Energy Dispersive Spectroscopy (EDS) elemental map revealed that Ag layers at both the top and bottom electrodes in the operated device (Figure 8(d)) were less continuous, compared to the Ag layers in Figure 8(c) of the as-deposited device, which is likely caused by Ag migration into both the dielectric and electrode layers during electrical cycling ${ }^{46}$. As highlighted by the two white arrows, the Ag profile of the EDS maps in the operated device revealed two detectable Ag protrusions with a cone-like shape, one residing in the top electrode pointing downwards while the other standing on the bottom electrode pointing upwards. Being a poor Ag ion conductor and unable to dissolve Ag chemically, $\mathrm{HfO}_{\mathrm{x}}$ makes $\mathrm{Ag}^{+}$easy to be chemically reduced within the dielectrics due to low ion mobility and low redox reaction rate, yielding the observed cone shaped Ag filament which grows from the Ag source rather than
having Ag deposition on the opposite anode. ${ }^{47,48}$ However, neither of the protrusions completely
bridged the dielectric between the top and bottom electrodes, which is different from the




Figure 8 Anatomy of nanodevices revealing morphology, composition and structural information around filament remains. (a) SEM micrograph of 100 nm crosspoint junctions of $\mathrm{Pd} / \mathrm{Ag} / \mathrm{HfO}_{x} / \mathrm{Ag} / \mathrm{Pd}$ selectors. (b) DC I-V characteristics of the junction on the right side of (a) showing repeatable threshold switching. (c) TEM cross-sectional image of a pristine device. The inset shows an EDS map of Ag element of the solid white box region. (d) TEM cross-sectional image of the measured device with IV shown in (b). The inset shows an EDS map of Ag element of the solid white box region. Two Ag protrusions are highlighted by the white arrows which are likely the remains of filaments. (e) EDS line profile of Ag along the dashed white lines in (c) and (d). The measured device features a narrow Ag gap as a result of the occurrence of Ag protrusion. (f) HRTEM of the dashed white box region in (d) which shows a narrowed Ag gap. The FFT (Fast Fourier Transfer) corresponding to the left white box shows the presence of nanocrystalline Ag while that of the right box shows the existence of crystalline $\mathrm{HfO}_{2}$ [011] facets.


Figure 9 (a) SEM micrograph of 100 nm crosspoint junctions of $\mathrm{Pd} / \mathrm{Ag} / \mathrm{HfOx} / \mathrm{Ag} / \mathrm{Pd}$ selectors. (b)DC I-V characteristics of a $\mathrm{Pd} / \mathrm{Ag} / \mathrm{HfOx} / \mathrm{Ag} / \mathrm{Pd} 100 \times 100 \mathrm{~nm} 2$ crossline device which is capable of withstanding same current level (i.e. $100 \mu \mathrm{~A}$ ) as those microscale devices.
behavior typically observed in CBRAM ${ }^{46,48,49}$. The incomplete bridging was further verified by EDS line scans of the Ag peak along the white dashed lines shown in Figure 8(e), which also showed a clear narrowing of the dielectric layer thickness. This agrees with the experimental observation that those devices relax back to the HRS after the switching voltage is removed. In addition, the nanocrystalline monoclinic phase of $\mathrm{HfO}_{2}$ was observed adjacent to the broken bridge (see Figure 8(f)), a common aftereffect of Joule heating during the operation of the device ${ }^{50}$.

## E. Implications of Research

The present results seem to offer promise for a selector for memory applications. The selectors exhibit very high on-off ratio and hence are promising candidates for solving the sneak path current issue currently plaguing the memristor crossbar arrays from achieving full potential in replacing conventional flash based memory. If memristors can replace flash based memory, then computing space can be drastically decreased because memristors can be stacked three dimensionally.

Table 1 : Comparison with other technologies

| Technology | OTS ${ }^{22,23}$ | Mott MIT ${ }^{\text {26 }}$ | MIEC ${ }^{51}$ | FAST <br> (Electronic) ${ }^{29}$ | Unknown ${ }^{52}$ | Cu filament rupture ${ }^{33}$ | Our Device ${ }^{53}$ |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| Structure | TiN/AsTeGe SiN/TiN | $\begin{aligned} & \mathrm{TiN} / \mathrm{NbO}_{x} / \\ & \mathrm{W} \end{aligned}$ | Cu doped <br> $\mathrm{TE} / \mathrm{Cu}_{8} \mathrm{GeSe}_{6} / \mathrm{C}$ <br> u doped BE | N. A. | Te/Doped Chalcogenide/Be | $\begin{aligned} & \mathrm{Pt} / \mathrm{HfO}_{2} / \mathrm{HfO}_{2}: \\ & \mathrm{Cu} / \mathrm{Cu} \end{aligned}$ | Pt/Ag/HfO2/Ag/Pt |
| TEM |  |  | MIEC <br> BEC <br> 100 mm |  | TE <br> Begred-chatregenitit |  |  |
| Size | $\begin{aligned} & 30 \mathrm{~nm} \times 30 \\ & \mathrm{~nm} \end{aligned}$ | 10 nm x Length | 20 nm diameter | $\begin{aligned} & 15 \mathrm{~nm} \times 100 \\ & \mathrm{~nm} \end{aligned}$ | 200nm diameter | 300 nm diameter | $5 \mu \times 5 \mu$ and 100 nm $\times 100 \mathrm{~nm}$ |
| $\mathrm{V}_{\text {turestold }}$ | $\sim 3 \mathrm{~V}$ | $\sim 1.3 \mathrm{~V}$ | Gradual | $1 \mathrm{~V}(\sim 10 \mathrm{~nm})$ | 1.5 V | 0.5 V | 0.3-0.7V |
| $\mathbf{V}_{\text {hold }}$ | $\sim 1.6 \mathrm{~V}$ | $\sim 1.3$ | Gradual | Same with $\mathrm{V}_{\text {th }}$ | 0.2 V | $<0.1$ V | 0-0.2V |
| $\mathrm{I}_{\mathrm{oN}} / \mathrm{I}_{\text {OFF }}$ | $\sim 2.5 \times 10^{3}$ | >50 | $\sim 3 \times 10^{4}$ | $>10^{7}$ | $10^{7}$ | $10^{7}$ | $10^{10}$ |
| Time to turn ON | 4ns | N. A. | $<100$ ns | <50 ns | $<10$ ns | $<50 \mathrm{~ns}$ (No Fig) | <75ns |
| Time to OFF | Not verified | N. A. | Not verified | <50 ns | Not verified | $\begin{aligned} & <100 \mathrm{~ns} \text { (No } \\ & \text { Fig) } \end{aligned}$ | <250ns |
| Endurance | $10^{8}$ | $10^{6}$ | $10^{8}$ | $10^{8}$ | $10^{9}$ | $10^{10}$ | $10^{8}$ |
| On Current Density(J ${ }_{\text {ON }}$ ) (MA/cm2) | 11 | 10 | 50 | 5 | 1.6 | >1 | >1 |

## REFERENCES

1. Waser, R.; Aono, M. Nat. Mater. 2007, 6, (11), 833-840.
2. Waser, R.; Dittmann, R.; Staikov, G.; Szot, K. Adv. Mater. 2009, 21, (25-26), 2632-2663.
3. Kwon, D.-H.; Kim, K. M.; Jang, J. H.; Jeon, J. M.; Lee, M. H.; Kim, G. H.; Li, X.-S.; Park, G.-S.; Lee, B.; Han, S.; Kim, M.; Hwang, C. S. Nat. Nanotechnol. 2010, 5, (2), 148-153.
4. Ohno, T.; Hasegawa, T.; Tsuruoka, T.; Terabe, K.; Gimzewski, J. K.; Aono, M. Nat. Mater. 2011, 10, (8), 591-5.
5. Chen, A. B.; Kim, S. G.; Wang, Y.; Tung, W. S.; Chen, I. W. Nat. Nanotechnol. 2011, 6, (4), 237-41.
6. Choi, B. J.; Chen, A. B.; Yang, X.; Chen, I. W. Adv. Mater. 2011, 23, (33), 3847-52.
7. Yang, J. J.; Strukov, D. B.; Stewart, D. R. Nat. Nanotechnol. 2013, 8, (1), 13-24.
8. Terabe, K.; Hasegawa, T.; Nakayama, T.; Aono, M. Nature 2005, 433, (7021), 47-50.
9. $\quad$ Strukov, D. B.; Williams, R. S. Proc Natl Acad Sci U S A 2009, 106, (48), 20155-8.
10. Yu, S.; Chen, H.-Y.; Gao, B.; Kang, J.; Wong, H. S. P. ACS Nano 2013, 7, (3), 2320-2325.
11. Seok, J. Y.; Song, S. J.; Yoon, J. H.; Yoon, K. J.; Park, T. H.; Kwon, D. E.; Lim, H.; Kim, G. H.; Jeong, D. S.; Hwang, C. S. Adv. Funct. Mater. 2014, 24, (34), 5316-5339.
12. Lim, H.; Kim, I.; Kim, J. S.; Hwang, C. S.; Jeong, D. S. Nanotechnology 2013, 24, (38), 384005.
13. Mahalanabis, D.; Barnaby, H. J.; Gonzalez-Velo, Y.; Kozicki, M. N.; Vrudhula, S.; Dandamudi, P. Solid•State Electron. 2014, 100, 39-44.
14. Kim, S.; Zhou, J.; Lu, W. D. IEEE Trans. Electron Devices 2014, 61, (8), 2820-2826.
15. Zhou, J.; Kim, K. H.; Lu, W. IEEE Trans. Electron Devices 2014, 61, (5), 1369-1376.
16. Burr, G. W.; Shenoy, R. S.; Hwang, H., Select Device Concepts for Crossbar Arrays. In Resistive Switching, Wiley-VCH Verlag GmbH \& Co. KGaA: 2016; pp 623-660.
17. Kim, G. H.; Lee, J. H.; Ahn, Y.; Jeon, W.; Song, S. J.; Seok, J. Y.; Yoon, J. H.; Yoon, K. J.; Park, T. J.; Hwang, C. S. Adv. Funct. Mater. 2013, 23, (11), 1440-1449.
18. Kawahara, A.; Azuma, R.; Ikeda, Y.; Kawai, K.; Katoh, Y.; Hayakawa, Y.; Tsuji, K.; Yoneda, S.; Himeno, A.; Shimakawa, K.; Takagi, T.; Mikawa, T.; Aono, K. IEEE Journal of Solid-State Circuits 2013, 48, (1), 178-185.
19. Choi, B. J.; Zhang, J.; Norris, K.; Gibson, G.; Kim, K. M.; Jackson, W.; Zhang, M. X.; Li, Z.; Yang, J. J.; Williams, R. S. Adv. Mater. 2016, 28, (2), 356-62.
20. Anbarasu, M.; Wimmer, M.; Bruns, G.; Salinga, M.; Wuttig, M. Appl. Phys. Lett. 2012, 100, (14), 143505.
21. Lee, M. J.; Lee, D.; Kim, H.; Choi, H. S.; Park, J. B.; Kim, H. G.; Cha, Y. K.; Chung, U. I.; Yoo, I. K.; Kim, K. In Highly-scalable threshold switching select device based on chaclogenide glasses for 3D nanoscaled memory arrays, Electron Devices Meeting (IEDM), 2012 IEEE International, 10-13 Dec. 2012, 2012; pp 2.6.1-2.6.3.
22. Kim, S.; Kim, Y. B.; Kim, K. M.; Kim, S. J.; Lee, S. R.; Chang, M.; Cho, E.; Lee, M. J.; Lee, D.; Kim, C. J.; Chung, U. I.; Yoo, I. K. In Performance of threshold switching in chalcogenide glass for 3D stackable selector, 2013 Symposium on VLSI Technology, 1113 June 2013, 2013; pp T240-T241.
23. Lee, M. J.; Lee, D.; Kim, H.; Choi, H. S.; Park, J. B.; Kim, H. G.; Cha, Y. K.; Chung, U. I.; Yoo, I. K.; Kim, K. In Highly-scalable threshold switching select device based on chaclogenide glasses for 3D nanoscaled memory arrays, 2012 International Electron Devices Meeting, 10-13 Dec. 2012, 2012; pp 2.6.1-2.6.3.
24. Son, M.; Lee, J.; Park, J.; Shin, J.; Choi, G.; Jung, S.; Lee, W.; Kim, S.; Park, S.; Hwang, H. IEEE Electron Device Letters 2011, 32, (11), 1579-1581.
25. Kim, S.; Liu, X.; Park, J.; Jung, S.; Lee, W.; Woo, J.; Shin, J.; Choi, G.; Cho, C.; Park, S.; Lee, D.; Cha, E. j.; Lee, B. H.; Lee, H. D.; Kim, S. G.; Chung, S.; Hwang, H. In Ultrathin (<10nm) $\mathrm{Nb}_{2} \mathrm{O}_{5} / \mathrm{NbO}_{2}$ hybrid memory with both memory and selector characteristics for
high density 3D vertically stackable RRAM applications, VLSI Technology (VLSIT), 2012 Symposium on, 12-14 June 2012, 2012; pp 155-156.
26. Cha, E.; Woo, J.; Lee, D.; Lee, S.; Song, J.; Koo, Y.; Lee, J.; Park, C. G.; Yang, M. Y.; Kamiya, K.; Shiraishi, K.; Magyari-Köpe, B.; Nishi, Y.; Hwang, H. In Nanoscale ( $\sim 10 \mathrm{~nm}$ ) 3D vertical ReRAM and $\mathrm{NbO}_{2}$ threshold selector with TiN electrode, 2013 IEEE International Electron Devices Meeting, 9-11 Dec. 2013, 2013; pp 10.5.1-10.5.4.
27. Lee, D.; Park, J.; Park, S.; Woo, J.; Moon, K.; Cha, E.; Lee, S.; Song, J.; Koo, Y.; Hwang, H., BEOL compatible ( $300^{\circ} \mathrm{C}$ ) TiN/TiO ${ }_{x} / \mathrm{Ta} / \mathrm{TiN} 3 \mathrm{D}$ nanoscale ( $\sim 10 \mathrm{~nm}$ ) IMT selector. In 2013 IEEE International Electron Devices Meeting, 2013; pp 10.7.1-10.7.4.
28. Gibson, G. A.; Musunuru, S.; Zhang, J.; Vandenberghe, K.; Lee, J.; Hsieh, C.-C.; Jackson, W.; Jeon, Y.; Henze, D.; Li, Z.; Stanley Williams, R. Appl. Phys. Lett. 2016, 108, (2), 023505.
29. Sung Hyun, J.; Kumar, T.; Narayanan, S.; Lu, W. D.; Nazarian, H. In 3D-stackable crossbar resistive memory based on Field Assisted Superlinear Threshold (FAST) selector, Electron Devices Meeting (IEDM), 2014 IEEE International, 15-17 Dec. 2014, 2014; pp 6.7.1-6.7.4.
30. Sung Hyun, J.; Kumar, T.; Narayanan, S.; Nazarian, H. IEEE Trans. Electron Dev. 2015, 62, (11), 3477-3481.
31. Narayanan, P.; Burr, G. W.; Shenoy, R. S.; Stephens, S.; Virwani, K.; Padilla, A.; Kurdi, B. N.; Gopalakrishnan, K. IEEE J. Electron Devices Soc. 2015, 3, (5), 423-434.
32. Yang, J.; Wu, W.; Xia, Q. Switchable two-terminal devices with diffusion/drift species. 8,879,300, 2014.
33. Luo, Q.; Xu, X.; Liu, H.; Lv, H.; Lu, N.; Gong, T.; Long, S.; Liu, Q.; Sun, H.; Banerjee, W.; Liu, M., Cu BEOL Compatible Selector with High Selectivity ( $>10^{7}$ ), Extremely Low Off-current ( $\sim \mathrm{pA}$ ) and High Endurance ( $>10^{10}$ ). In Electron Devices Meeting (IEDM), 2015 IEEE International, 2015.
34. Jeonghwan, S.; Jiyong, W.; Prakash, A.; Daeseok, L.; Hyunsang, H. IEEE Electron Device Lett. 2015, 36, (7), 681-683.
35. Song, J.; Prakash, A.; Lee, D.; Woo, J.; Cha, E.; Lee, S.; Hwang, H. Appl. Phys. Lett. 2015, 107, (11), 113504.
36. Chen, W.; Barnaby, H. J.; Kozicki, M. N. IEEE Electron Device Letters 2016, 37, (5), 580-583.
37. Song, J.; Woo, J.; Lee, S.; Prakash, A.; Yoo, J.; Moon, K.; Hwang, H. IEEE Electron Device Letters 2016, PP, (99), 1-1.
38. Hsiung, C.-P.; Liao, H.-W.; Gan, J.-Y.; Wu, T.-B.; Hwang, J.-C.; Chen, F.; Tsai, M.-J. ACS Nano 2010, 4, (9), 5414-5420.
39. Sun, H.; Liu, Q.; Li, C.; Long, S.; Lv, H.; Bi, C.; Huo, Z.; Li, L.; Liu, M. Adv. Funct. Mater. 2014, 24, (36), 5679-5686.
40. Valov, I.; Linn, E.; Tappertzhofen, S.; Schmelzer, S.; van den Hurk, J.; Lentz, F.; Waser, R. Nat. Commun. 2013, 4, 1771.
41. Yu, S.; Wong, H. S. P. IEEE Trans. Electron Devices 2011, 58, (5), 1352-1360.
42. Wang, Z.; Yu, H.; Tran, X. A.; Fang, Z.; Wang, J.; Su, H. Phys. Rev. B 2012, 85, (19).
43. Wang, Z.; Yu, H.; Su, H. Sci. Rep. 2013, 3, 3246.
44. Wang, Z.; Joshi, S.; Saveliev, S. E.; Jiang, H.; Midya, R.; Lin, P.; Hu, M.; Ge, N.; Strachan, J. P.; Li, Z.; Wu, Q.; Barnell, M.; Li, G.-L.; Xin, H. L.; Williams, R. S.; Xia, Q.; Yang, J. J. Nat. Mater. 2016.
45. Günther, B.; Kumpmann, A.; Kunze, H. D. Scr. Metall. Mater. 1992, 27, (7), 833-838.
46. Yang, Y. C.; Pan, F.; Liu, Q.; Liu, M.; Zeng, F. Nano Lett. 2009, 9, (4), 1636-1643.
47. Yang, Y.; Gao, P.; Li, L.; Pan, X.; Tappertzhofen, S.; Choi, S.; Waser, R.; Valov, I.; Lu, W. D. Nat Commun 2014, 5, 4232.
48. Yang, Y.; Gao, P.; Gaba, S.; Chang, T.; Pan, X.; Lu, W. Nat Commun 2012, 3, 732.
49. Tian, X.; Yang, S.; Zeng, M.; Wang, L.; Wei, J.; Xu, Z.; Wang, W.; Bai, X. Adv. Mater. 2014, 26, (22), 3649-54.
50. Miao, F.; Strachan, J. P.; Yang, J. J.; Zhang, M. X.; Goldfarb, I.; Torrezan, A. C.; Eschbach, P.; Kelley, R. D.; Medeiros-Ribeiro, G.; Williams, R. S. Adv. Mater. 2011, 23, (47), 5633-40.
51. Virwani, K.; Burr, G. W.; Shenoy, R. S.; Rettner, C. T.; Padilla, A.; Topuria, T.; Rice, P. M.; Ho, G.; King, R. S.; Nguyen, K.; Bowers, A. N.; Jurich, M.; BrightSky, M.; Joseph, E. A.; Kellock, A. J.; Arellano, N.; Kurdi, B. N.; Gopalakrishnan, K. In Sub-30nm scaling and high-speed operation of fully-confined Access-Devices for 3D crosspoint memory based on mixed-ionic-electronic-conduction (MIEC) materials, 2012 International Electron Devices Meeting, 10-13 Dec. 2012, 2012; pp 2.7.1-2.7.4.
52. Yang, H.; Li, M.; He, W.; Jiang, Y.; Lim, K. G.; Song, W.; Zhuo, V. Y. Q.; Tan, C. C.; Chua, E. K.; Wang, W.; Yang, Y.; Ji, R. In Novel selector for high density non-volatile memory with ultra-low holding voltage and $10<$ sup>7</sup> on/off ratio, 2015 Symposium on VLSI Technology (VLSI Technology), 16-18 June 2015, 2015; pp T130T131.
53. Midya, R.; Wang, Z.; Zhang, J.; Savel'ev, S. E.; Li, C.; Rao, M.; Jang, M. H.; Joshi, S.; Jiang, H.; Lin, P.; Norris, K.; Ge, N.; Wu, Q.; Barnell, M.; Li, Z.; Xin, H. L.; Williams, R. S.; Xia, Q.; Yang, J. J. Advanced materials 2017.
