ON-CHIP DIELECTRIC COHESIVE FRACTURE CHARACTERIZATION AND MITIGATION INVESTIGATION THROUGH OFF-CHIP CARBON NANOTUBE INTERCONNECTS

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ON-CHIP DIELECTRIC COHESIVE FRACTURE CHARACTERIZATION AND MITIGATION INVESTIGATION THROUGH OFF-CHIP CARBON NANOTUBE INTERCONNECTS

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To my wife, parents, and sisters.

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SUMMARY

The cohesive fracture of thin films is a concern for the reliability of many devices in microelectronics, MEMS, photovoltaics, and other applications. In microelectronic packaging the cohesive fracture toughness has become a concern with new low-k dielectric materials currently being used. To obtain the low-k values needed to meet electrical performance goals, the mechanical strength of the material has decreased. This has resulted in cohesive cracks occurring in the Back End of Line (BEoL) dielectric layers of the microelectronic packages. These cracks lead to electronic failures and occur after thermal loading (due to CTE mismatch of materials) and mechanical loading. To prevent these cohesive cracks, it is necessary to measure the cohesive fracture resistance of these thin films to implement during the design and analysis process. Many of the current tests to measure the cohesive fracture resistance of thin films are based on methods developed for larger scale specimens. These methods can be difficult to apply to thin films due to their size and require mechanical fixturing, physical contact near the crack tip, and complicated stress fields. Therefore, a fixtureless cohesive fracture resistance measurement technique has been developed that utilizes photolithography fabrication processes. This technique uses a superlayer thin film with a high intrinsic stress deposited on top of the desired test material to drive cohesive fracture through the thickness of test material. In addition to developing a technique to measure the fracture resistance of dielectric thin films, the use of carbon nanotube (CNT) forests as off-chip interconnects is investigated as a potential method to mitigate the fracture of these materials. The compressive and tensile modulus of CNT forests is characterized, and it is

seen that the modulus is several orders of magnitude less than that of a single straight CNT. The low-modulus CNT forest will help mechanically decouple the chip from the board and reduce stress occurring in the dielectric layers as compared to the current technology of solder ball interconnects and therefore improve reliability. The mechanical performance of these CNT interconnects is investigated by creating a finite-element model of a flip chip electronic package utilizing CNT interconnects and comparing the chip stresses to a traditional solder ball interconnect scenario. Additionally, flip chips are fabricated with CNT forest interconnects, assembled to an FR4 substrate, and subjected to accelerated thermomechanical testing to experimentally investigate their performance.

CHAPTER 1

INTRODUCTION AND LITERATURE REVIEW

1.1 Introduction

In recent years, copper interconnects and low-k dielectrics have emerged as a key enabling technology for device performance to overcome RC delay in microelectronic packaging. After the adoption of copper as the primary conductor in devices, significant amount of research has been conducted on reducing wire capacitance by utilizing dielectrics with lower dielectric constants than traditional oxides (Figure 1).

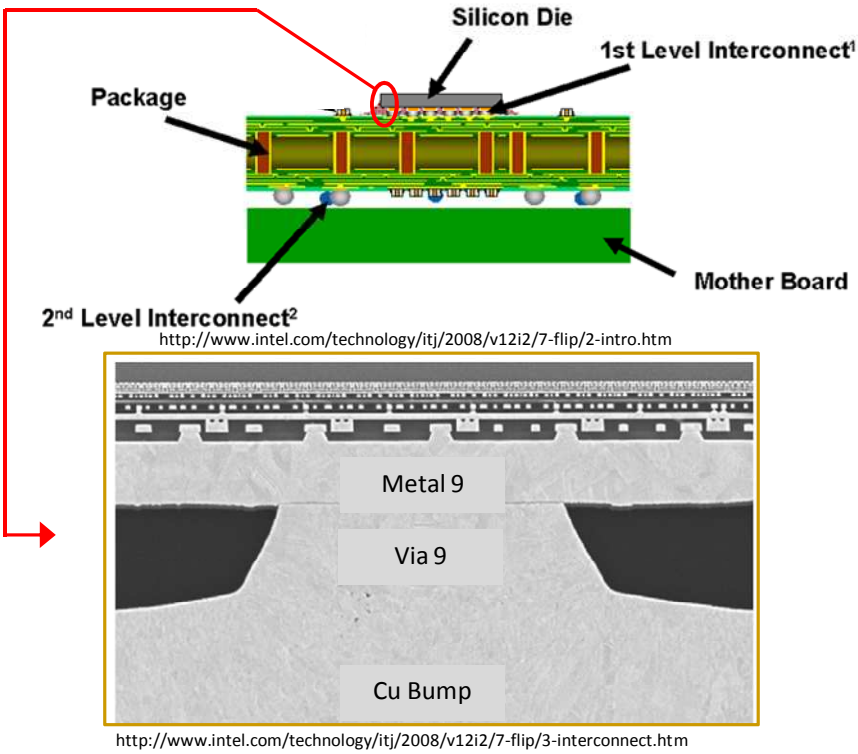


Figure 1: (top) Schematic of flip chip ball grid array package, illustrating the various levels of interconnects to attach the silicon die to the board substrate [1]. (bottom) SEM cross-section image of various metallization layers and surround dielectric material in the vicinity of a bump interconnect [2].

To achieve these low dielectric constants, the materials have become more porous and also incorporation of air gaps into the layers is being investigated in order to reduce the overall effective dielectric constant of the material. Unfortunately, the pace of implementing these low-k material technologies has been slowing down as stated by earlier ITRS projections because of difficulties in fabrication, cost, and reliability. These difficulties are mainly due to the fact that the tactics used to reduce the dielectric constant, such as increasing porosity, also reduces the mechanical strength of the material [3-5]. These poor mechanical properties coupled with a general decrease in layer thickness, make the material more susceptible to cohesive and interfacial cracking during chemical mechanical polishing (CMP) at early stages of fabrication and also during assembly, packaging, and later during reliability testing (Figure 2) [6].

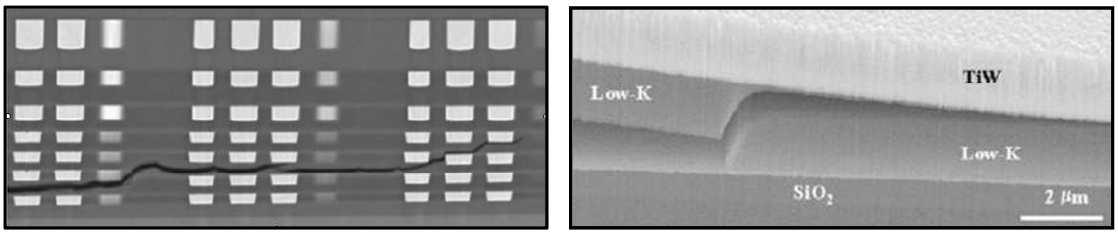


Figure 2: Examples of cohesive and interfacial fracture of dielectric layers in electronic packaging [6].

Such manufacturing and reliability issues will continue to be a concern with future technologies of increasingly smaller interconnect lines, spaces, and mechanically weaker low-k interlayer dielectrics. This is why the ITRS roadmap has labeled the manufacturing, implementation, reliability, and characterization of low-k dielectrics as one of the grand challenges to overcome for the future of microelectronics [7]. Also, thin films are of importance in other industries besides microelectronics such as micro-electrical-mechanical systems (MEMS), photovoltaics, and coatings where cohesive fracture can also be a concern. Therefore it is extremely important to pursue further

research to understand the mechanical properties of thin film materials to better implement them. In addition to measuring the mechanical properties of such thin films, it is also important to explore methods to prevent cohesive failure in dielectric layers.

One such possible solution to aide in preventing cohesive failure of these thin film layers is through the use of compliant electrical interconnects to connect the silicon die to the printed circuit board. Compliant interconnects allow for the silicon die and the printed circuit board or chip carrier to be electronically connected, but mechanically decoupled. This allows the die and the board to mechanically deform independently from any external mechanical loads or from thermal loads that cause these materials with different coefficients of thermal expansion (CTE) to deform independently. Therefore compliant interconnects reduce the stresses in the thin films and help prevent cohesive fracture compared to traditional rigid solder ball electrical interconnects. In recent years, carbon nanotubes have garnered great interest in many research fields due to their excellent mechanical, electrical, and thermal properties. Additionally, it has been shown that while individual CNTs have a high elastic modulus [8] and strength [9], CNT forests have a very low effective modulus [10]. If bundles of CNT are used as electrical interconnects, the low effective modulus will create a compliant interconnect and still have high mechanical strength and desirable electrical resistance. Therefore electronic interconnects consisting of CNT forest bundles offer the potential to mitigate the cohesive fracture of thin films used in microelectronic packaging.

1.2 Literature Review

In this section, a review of literature relevant to thin film cohesive fracture is presented along with the application of CNTs as off-chip interconnects and the

mechanical characterization of carbon nanotubes. Furthermore after each of these sections a discussion of the fundamental gaps that motivated this research will be presented.

1.2.1 Thin Film Cohesive Fracture Testing

Measuring the fracture toughness of a material provides very important information for the design, analysis, and implementation of materials. For bulk materials this measurement has become a common practice, for which standard procedures have been developed and are readily accessible (i.e. compact specimen, single edge notched tension panel, edge cracked plate subjected to pure bending tests) [11]. With the increased use of thin films and coatings in recent years, there is a need for similar cohesive fracture toughness data for thin films of materials. The properties of the bulk material may not be applicable to their respective thin films due to: 1) surface interface effects that are more pronounced at small scales, 2) limited number of grains in a given volume, 3) the materials may only be available in thin film form and not in bulk 4) and the effect of manufacturing processes used [12]. These manufacturing process include the method and parameters used during the deposition process and procedures used to remove material or pattern it. For a given material, there may be several deposition processes that can be used to create the film such as sputtering, evaporation, or chemical vapor deposition. Each of these processes can result in different microstructure and grains, and therefore affect the mechanical properties of the thin film. Additionally, for each of these processes there are a wide set of deposition parameters such as deposition rate, chamber pressure, and temperature that can have similar effects. Also during the material removal and patterning, either dry etching or wet etching may be used which

lead to differences in surface roughness of the film. It is for these reasons why new test methods are being developed to measure the fracture toughness of thin films. Many new tests have been developed over the years to measure the cohesive fracture toughness of thin films. These tests can be grouped into two general categories:

1. Nanoindentation (radial cracks, circumferential, channel cracking)
2. Microtensile testing (membrane deflection, inchworm actuation, tension by residual stress, bulge testing)

Nanoindentation Based Measurement Techniques

The key component of nanoindentation based measurements techniques is that they use a nanoindentation system. This system uses a micron scale tip of standard shape (ex. Berkovich, Vickers, cube-corner, flat-punch, sphere, etc.), that then comes into contact with the test material surface and then a force is applied by a capacitive transducer and the resulting displacement is recorded to create a force versus displacement curve. The system allows for nanoscale measurement of both the force and displacement. Three general approaches have been used to measure the fracture toughness of thin films using a nanoindenter system which are defined by the type of crack created.

Radial cracking occurs when a sharp edged tip such as a Berkovich or Vickers tip is used as shown in Figure 3. The fracture toughness is then measured using the length of the resulting radial cracks, the peak load, and geometry constants [13]. One specific difficulty of this technique is producing a crack of the desired shape, such as a half penny, that can only be allowed to penetrate a depth of less than 10% of the film thickness [14].

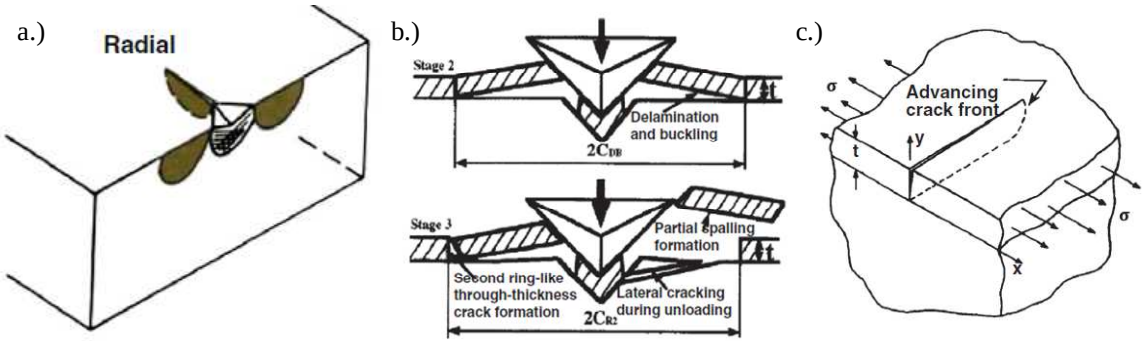


Figure 3: Three different types of cracking created using nanoindentation to measure fracture toughness of thin films. a.) radial crack [15], b.) circumferential crack [16], c.) channel crack [17].

Circumferential Cracking and spallation occurs during nanoindentation when there is both cohesive cracking and delamination of the thin film. This indentation process is separated into three stages where Stage 1 is defined by circumferential through thickness cracks forming under the nanoindenter tip. Stage 2 occurs when delamination and buckling of the thin film occur around the contact area due to lateral pressure and Stage 3 is defined by a second circumferential through thickness crack forming. During Stage 3 there is a sudden increase in the displacement without a large increase in load, which results in a step in the load versus displacement curve [13]. The fracture toughness can then be calculated with the fracture energy expended during the sudden displacement increase and from the radius of the second circumferential crack. A point of controversy is determining the value of this fracture energy for irreversible work, which is convoluted due to effect of the substrate and plastic vs. elastic energy dissipation [18].

Channel cracking fracture testing is defined by cracks occurring through the total thickness of a thin film. These types of testing techniques can be done with nanoindentation [19] or with other approaches such as multi-strain flexure tests [20] that utilize four point bend configurations. The analysis approach used for channel cracking measurements is similar to circumferential cracking and radial cracking, but with a

different crack geometry and substrate constraining effects [13]. The main difficulties of this approach are locating the first through thickness channel crack that occurs in the specimen and having a large enough difference in hardness between the substrate and the film [21].

Microtensile Testing Measurement Techniques

There has been significant development in different microtensile testing measurement techniques resulting in many different approaches. The following sections summarize the methods of membrane deflection, nanoscale actuation, tension by residual stress, and bulge testing (Figure 4).

Membrane/beam deflection [12, 22] – This method is executed by using microfabrication techniques and photolithography to define either freestanding membranes or beams on a substrate. Then a load is applied to the center of the free standing membrane/beam with a nanoindenter until fracture. The load is measured with the nanoindenter and the displacement can either be measured with the nanoindenter as well, or some other system such as an interferometer can be used. This technique attempts to improve on the other nanoindenter based techniques by eliminating the complexity introduced by the underlying substrate, but still requires major equipment such as the nanoindenter.

Nanoscale actuation [23, 24] – Similar to membrane/beam deflection this test uses micro-fabrication techniques and photolithography to define freestanding micro-scale beams on a substrate. One end of the beam is fixed to the substrate, and the other end is free to allow for a nanoscale actuator to be attached. After the actuator is attached to the free end, the actuator is used to apply a load and measure the resulting displacement. Challenges arise when attaching the actuator to the free end of the test sample, which

requires great care not to damage the sample. Additionally this technique requires use of customized and specialty equipment.

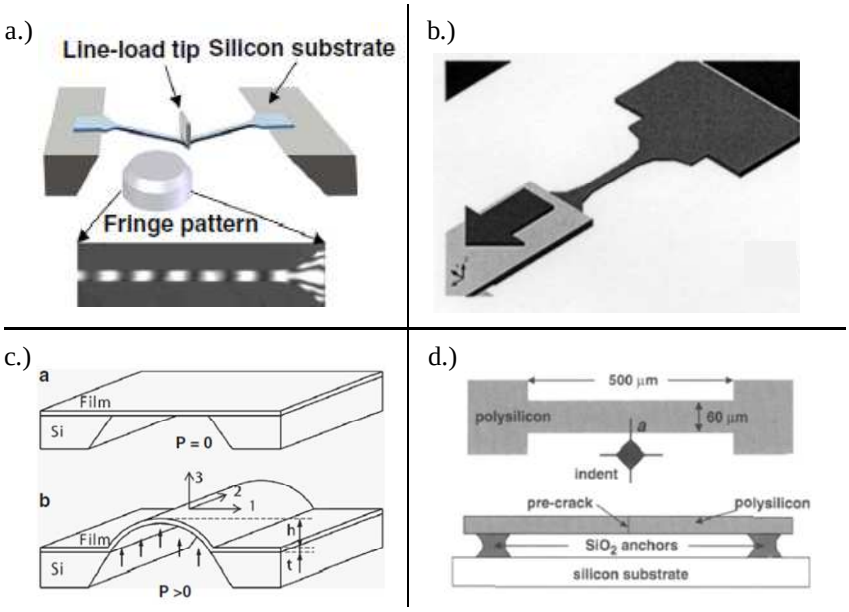


Figure 4: Examples of microtensile tests: a.) membrane/beam deflection[22], b.) Nanoscale actuation [24], c.) bulge test [25], d.) tension by residual stress [26].

Bulge testing [25, 27, 28] – In this test technique after the thin film of interest is deposited on a silicon substrate, the back of the silicon wafer is patterned and etched to create a freestanding membrane of the thin film. Then in the center of the freestanding membrane, a focused ion beam is used to create a small precrack through the film. Either water or air is then used on the backside of the freestanding membrane to apply a pressure on the film, causing it to bulge. The membrane and precrack is monitored while the pressure is increased to determine the critical pressure.

Tension by residual stress [26, 29] - In this method the residual stress in the film is used to drive crack propagation in freestanding thin film beams fixed at both ends. The origin of the residual stresses in these reports is due to thermal stresses that developed during the high temperature deposition of the thin films. Before the beams are released from the

substrate, a micro indenter is used to indent the substrate near the center of the beam to create a pre-crack. Then after the pre-crack is created, and the beam released from the substrate, depending on the amount of residual stress present, the crack will grow. This test method requires several fabrication runs in order to create beams with different residual stress levels to measure the fracture toughness. While the use of the residual stress to drive fracture has its advantages, this method requires the test material to have the ability to deposit it with a high and wide range of stresses. This therefore limits the number of thin films available to use with this test.

Gaps in Existing Thin Film Fracture Test Methods

As presented in the previous sections of this chapter, the most common general types of thin film fracture test methods are those that are based on the use of a nanoindenter system and other methods that eliminate the use of a nanoindenter by utilizing micro-fabrication processes. The main advantage of the nanoindenter based approaches is that these are fairly standard commercial systems, and therefore potentially available to researchers. But if not, these systems can be extremely expensive, and therefore cost prohibitive. Another referenced advantage of this method is simple test sample preparation, consisting of just a thin film of the target test material deposited on a rigid substrate. With these advantages, there are also several disadvantages including:

- The nanoindenter tip creates complex stress fields when contacting the test material and therefore makes the analytical solutions for the fracture toughness difficult.
- The measurement of the mechanical properties of the thin film can be affected by the hardness and modulus of the substrate it is deposited on,

therefore creating possible limits of materials applicable to the method [13, 21].

- Creating the desired crack type for the respective nanoindenter test sub categories is not straightforward (i.e. circumferential vs. radial cracking), and then subsequently locating and measuring the resulting cracks can also be difficult and add uncertainty [13].

These disadvantages of the nanoindenter based measurement methods have lead to the development of the second major category of thin film fracture test. This second category are the microtensile test methods that attempt to overcome some of the disadvantages of the nanoindenter based methods related to the unwanted effects of the substrate on the target test film's mechanical property measurement by using freestanding beams or membranes. Additionally, in order to reduce cost, these microtensile test methods do not require the use of nanoindenter systems. But in the process of creating these different approaches to measure the fracture toughness of thin films, customized and complicated mechanism are devised to apply the force that drives fracture in the test material or to measure its displacement or the resulting crack lengths. Additionally, these mechanisms may require fixturing and attaching to the fragile micro/nano scale material specimens which can result in unwanted stress concentrations and premature failure. Therefore, this thesis presents a new test method to measure the cohesive fracture resistance of thin films that improves on some of these disadvantages of the nanoindenter based and microtensile tester methods by:

- Eliminating the possible undesirable effects of the substrate by using freestanding films

- Not requiring fixturing, clamping, or attachment for the application external forces or to measure resulting displacements.
- Use fabrication processes that create representative thin films of the target application for the material
- Does not require expensive, complicated, or custom measurement equipment

1.2.2 General Fracture Mechanics

There are two broad approaches in mechanical engineering to guide the design of a structural component against failure. The first approach utilizes the traditional strength of materials concepts and focuses on calculating the stress that the component experiences during loading and then compares the calculated stress to a mechanical property of the material such as yield strength to determine the adequacy of the component's design. A second approach is the fracture mechanics approach, and involves three parameters, as compared to two of the strength of materials approach. The fracture mechanics approach is similarly concerned with the applied stress to the component, but also adds the size of a potential flaw/crack and uses the mechanical property of fracture toughness. The study of fracture mechanics seeks to quantify the combination of these three parameters to guide the design of structural components.

This field of research on modern fracture mechanics began to be formally developed early in the twentieth century. Within fracture mechanics there are generally two different analysis approaches, 1) the stress intensity factor approach and 2) the energy criterion approach. In a plate composed of a perfect linear elastic material without cracks with an applied in-plane stress of σ, the resulting stress throughout the

plate is a constant value of σ also. But if a crack is introduced to the plate, a stress field is created around the crack tip. In the stress intensity factor approach the stress field created by a crack within a material due to an applied stress is proportional to K_I, the stress concentration factor. For the case of a through thickness crack with a width of *2a* in an infinite plate with a thickness *B* and an applied in-plane uniform stress of σ as depicted in Figure 5 the stress intensity factor is given by:

$$K_I = \sigma\sqrt{\pi a} \tag{1}$$

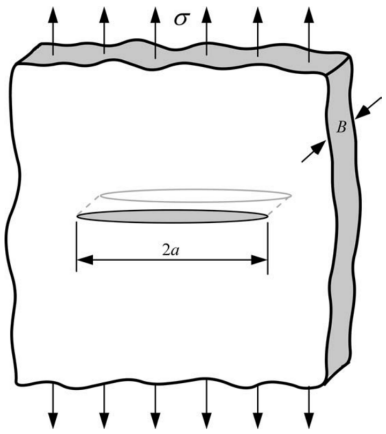


Figure 5: Schematic of infinite plate with through thickness crack with uniform tensile load applied [30].

From observing Equation 1, the value of K_I is a function of σ and crack size *a*, with fracture occurring when a critical value of K_I is reached. This critical value is referred to as K_{IC} and is a measure of the fracture resistance of the material and is a material property. Additionally the stress intensity factor allows for the stress field around the crack tip to be calculated. The components of the stress for the situation illustrated in Figure 6 are given by the following equations using a polar coordinate system:

$$\sigma_{xx} = \frac{K_I}{\sqrt{2\pi r}}\cos\left(\frac{\theta}{2}\right)\left[1 - \sin\left(\frac{\theta}{2}\right)\sin\left(\frac{3\theta}{2}\right)\right] \tag{2}$$

$$\sigma_{yy} = \frac{K_I}{\sqrt{2\pi r}}\cos\left(\frac{\theta}{2}\right)\left[1 + \sin\left(\frac{\theta}{2}\right)\sin\left(\frac{3\theta}{2}\right)\right] \quad (3)$$

$$\tau_{xy} = \frac{K_I}{\sqrt{2\pi r}}\cos\left(\frac{\theta}{2}\right)\sin\left(\frac{\theta}{2}\right)\cos\left(\frac{3\theta}{2}\right) \quad (4)$$

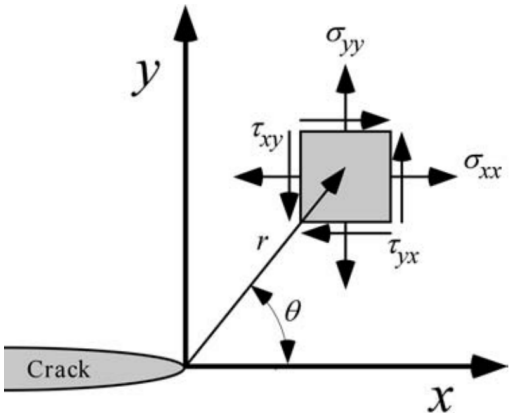


Figure 6: Schematic of stress fields near crack tip [30].

There exist many different variations of Equation 1 depending on the loading, crack geometry, and crack location.

The energy approach of fracture mechanics allows some of the analysis issues concerning the stress fields near the crack tip of the stress concentration approach to be avoided and offers a more convenient form to solve engineering problems [30]. A common model utilized by the energy approach is the strain energy release rate (*G*). This is the energy dissipated during fracture per unit of new crack surfaces created, or simply a measure of the energy available for an increment of crack extension, and is given by:

$$G = -\frac{d\Pi}{dA} \quad (5)$$

Where, *Π* is the potential energy supplied by internal strain energy and external forces, and *A* is the crack face area. Specifically, the potential energy of the elastic body is

composed of the strain energy stored in the body, *U*, and the work done by external forces, *F*, given by:

$$\Pi = U - F \tag{6}$$

Another common name used for the energy release rate is the crack driving force. Using this relationship, the energy release rate can be theoretically calculated for any crack length in a material. For the situation in Figure 1 of the through crack in an infinitely large plate with a uniform tensile stress, the energy release rate is given by:

$$G = \frac{\pi\sigma^2 a}{E} \tag{7}$$

For all materials, there exists a specific value of energy release rate at which fracture occurs called the critical energy release rate (G_c). Similar to the critical stress concentration value, the critical energy release rate is a material property and is a measure of the material's fracture resistance [30]. Where the relationship between the critical energy release rate and the critical stress intensity factor for the case of plane stress is given by:

$$G = \frac{K_I^2}{E} \tag{8}$$

This relationship for the critical values of the energy release rate and the stress intensity factor is also valid for none critical cases. Additional discussion is given in Section 4.4 and 5.2.8 on the use of the energy release rate for the fracture measurement method developed in this thesis and specifically its application in finite-element analysis.

1.2.3 CNT Based Off-Chip Interconnect Implementation

Single wall carbon nanotubes consist of single sheets of carbon atoms bonded in hexagonal arrangements rolled into a tubular form. It is also possible to create

multiwalled carbon nanotubes consisting of more than one sheet rolled together. The possible dimensions of carbon nanotubes are extraordinary, with diameters of less than 5 nm [31] and lengths in the range of centimeters [32] having been demonstrated in literature. Carbon nanotubes are created in a high temperature growth processes utilizing a carbon containing precursor gas that decomposes and dissolves into a metal catalyst film present. Growth occurs when the solubility limit of the carbon in the catalyst is reached and the carbon atoms are precipitated from the catalyst. Several synthesis methods have been used to grow CNTs in literature such as arc discharge, laser ablation, thermal CVD, and PECVD [33]. Further detail on the CNT growth process is given later in Section 8.4 and discussed in context to the application of this thesis.

Effective Mechanical Property Characterization of CNTs

Since the discovery of carbon nanotubes (CNTs), there have been many proposals for their potential use due to their extraordinary mechanical, electrical, and thermal properties. Some of these applications call for use of individual carbon nanotubes, while others utilize forests or turfs of carbon nanotubes. In the latter case, the forests consist of many vertically aligned carbon nanotubes (VACNTs) grown together, resembling an entangled forest of vertically aligned carbon nanotubes. In addition to vertically aligned CNTs though, the growth process to create CNTs can result in various levels of alignment, size distribution, and density as illustrated in Figure 7.

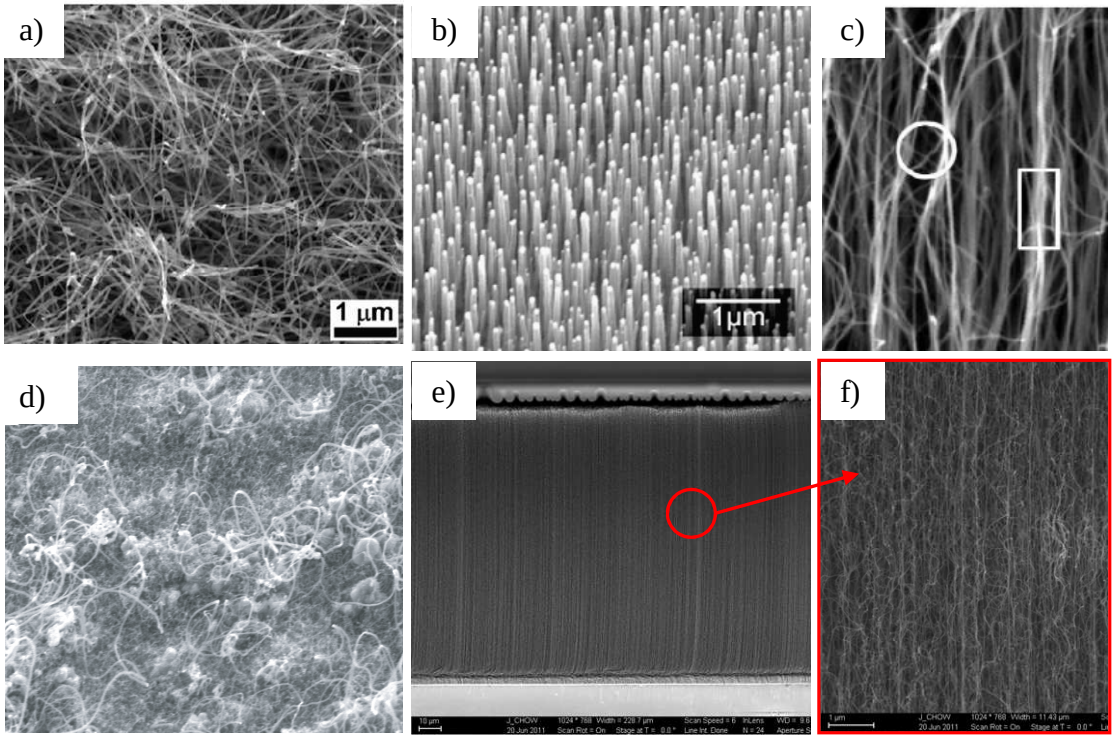


Figure 7: SEM images of different CNTs. a) CNT sponge with poor alignment, b) vertically aligned CNTs with low density and height, c) high magnification SEM image of vertically aligned CNT forest, d) CNT mat with poor alignment and poor size distribution, e) vertically aligned CNT forest with consistent diameter, f) zoomed-in image of e) showing good vertical alignment.

Some of the proposed applications for such CNT forests include nano/micro springs [34, 35], electrical interconnects [36-38], thermal interface materials [39, 40] to cool devices, or structural applications such as those proposed for a space elevator cable [41, 42]. To explore new potential applications and to create better and more reliable designs that utilize such CNTs, it is necessary to characterize the mechanical properties of CNT forests. Current research shows that while individual CNTs have reported values of tensile modulus in the ~100 GPa [43] – 4.15 TPa [8] range, the effective compressive modulus can be orders of magnitude lower, in the 0.1-1.0 MPa range. These measurements illustrate that CNTs are extremely compliant structures that could be used in other new applications where this characteristic is desired, such as compliant electrical off-chip interconnects for electronic packages.

Table 1: Measurements of the modulus of CNT forests performed with various methods.

Reported Modulus Values	Experimental Details
Nonlinear response: 1 MPa modulus for strains of 0.0-0.57, and 20.8 MPa for strains >0.57 [44]	Uniform compression test using an Instron® 5843 of 1000 µm tall CNT block between parallel plates. (Strain range ~0.0-0.65)
Reduced modulus of 10-20 MPa [45]	Nanoindenter with CSM and a 100 µm diameter flat punch tip on free ends of vertically aligned CNTs. CNT heights ranged from 35-1200 µm. (Strain range ~0.0-0.7)
Nonlinear response: 0.3 MPa for strains 0.0-0.05, 1.6 MPa for strain 0.05-0.20, and 0.25 MPa for strains >0.20 [46]	Uniform compression test using MTS Nano Bionix® of 280 µm tall CNT block.
Reduced modulus of 12.7 MPa (strain range ~0.0-0.002) [47]	Nanoindenter with a 5 µm radius tip on free ends of vertically aligned CNTs with a height of 1200 µm transferred to a substrate.
Reduced modulus between 50-60 MPa with nonlinear behavior [48]	Nanoindenter with a Berkovich tip on vertically aligned CNT forests with bundle diameter of 200 µm and heights of 20-100 µm. Indent depths were <1 µm.

Given that CNTs are a relatively new material, there are no standard techniques to measure their mechanical properties. Previous publications that report on their mechanical properties have used a range of techniques, some modifying and extending more traditional methods to perform the measurements. Several studies utilize nanoindentation to measure the mechanical properties of CNT forests/turfs [10, 45, 49], others use universal testing machines in compression [44, 46], while some have used unique/nontraditional techniques based on micro cantilevers/resonators [50]. With these different measurement techniques and with the wide range of variables affecting the fabrication of the CNTs, there is also a wide range of reported CNT effective modulus values as shown in Table 1.

Currently the most common approach to measure the mechanical properties of CNT forests utilizes a nanoindenter system. With this approach several different nanoindenter tips such as Berkovich, flat punch, or spherical geometries may be used to contact and compress the CNT forests. From these nanoindenter tests, force vs. displacement is measured during loading and subsequent unloading. This data is then used to calculate the stress vs. strain response of the CNT forest during loading and unloading. The stress calculation while using nanoindentation of the CNT forests possesses challenges and issues related to the tip geometry and the nature of the CNT forest structure. The CNT forests contain intertwined CNTs that act as a "foam block" and deform in unison with each other. When a nanoindenter system is used to measure the force vs. displacement of such CNT forests, the nanoindenter tip makes direct contact with the tips of the CNTs, which creates three specific issues that need consideration. 1) As the nanoindenter tip, such as a Berkovich tip, makes contact with the CNT tips, the contact area will increase with the depth of indentation, which has an effect on the contact area function [48, 51, 52]. 2) During compression, CNTs directly beneath the nanoindenter tip will de-tangle and detach from the surrounding CNTs. 3) Also during compression of the CNTs, they will be constrained by surrounding CNTs, and therefore affect potential buckling and/or outward bulging of the CNTs. Such outward bulging of CNTs during compression was observed by Qui et al [48]. Of these considerations, the first makes the calculation of the stress vs. strain difficult, while the second and third can potentially yield stiffer mechanical response values for the CNTs. Alternatively, a flat punch nanoindenter tip can be used to address the first issue by allowing the contact area between the nanoindenter tip and the CNTs to remain constant, but the issues of the

effects of the surrounding CNTs still remain. Therefore there is a need for new tests to measure the effective compressive modulus of CNT forests/turfs to address these concerns.

CNT Forest Off-Chip Interconnects

The field of electronic packaging deals with connecting integrated circuits (IC's) with other components into a complex system to create electronic products. Electronic packaging plays a critical role in creating electrical and physical interconnections, cooling, and protecting the electronic components and has a large impact on their performance, cost, reliability, size, and efficiency [53]. While advances in the continued reduction in the size of IC's to keep up with Moore's Law garners much attention, advances in electronic packaging is becoming the major technological hurdle to overcome [54, 55]. Therefore, great amounts of research and finances are being focused on packaging related challenges.

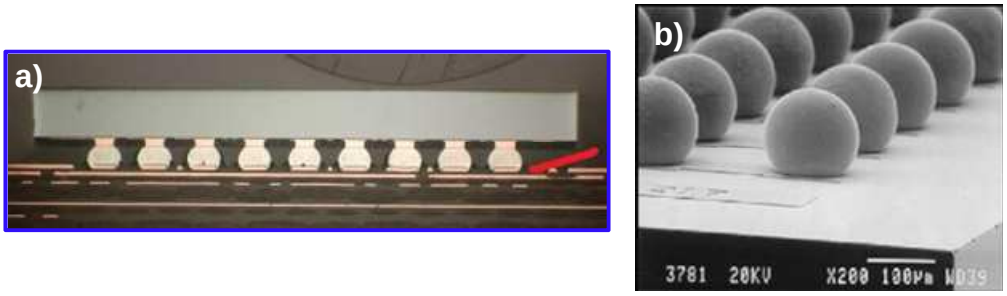


Figure 8: a) Cross-sectional view of assembled flip chip with solder balls [56]. b) SEM image of unassembled solder balls [57].

One of the major technology areas in electronic packaging requiring advancement are interconnects, which consists of on-chip and off-chip interconnects. On-chip interconnects are included in creating the transistors of IC's and also electrically connecting the various layers on the device. Whereas, off-chip interconnects are

comparably larger in size and are used to connect chips to other chips that may be stacked vertically (i.e. vias) or to connect chips to substrates such as printed circuit boards or chip carriers (i.e. flip chips) (Figure 8 and Figure 9). The technical responsibilities of interconnects include providing electrical connection, mechanical connection, and heat dissipation, all of which become more important and challenging as device integration is increased, size decreased, and materials with greater dissimilarities are employed. It is reported that interconnects are the location of 90% of all electrical and mechanical failures in electronic products [54] and therefore are a technology in constant pursuit of advancement.

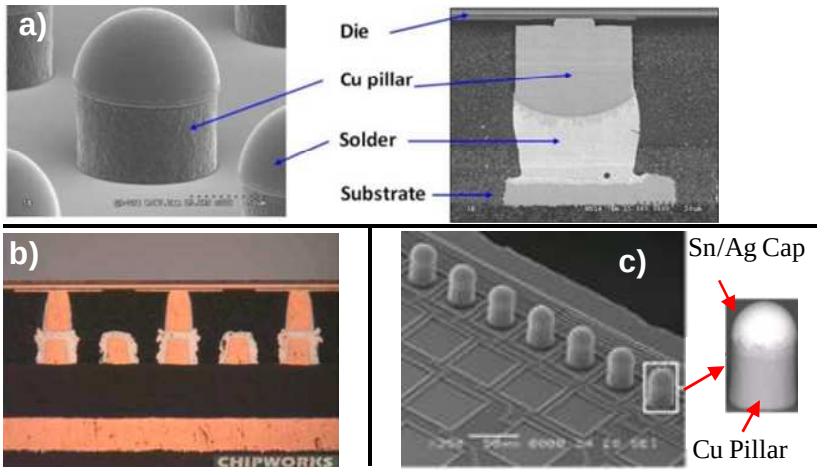


Figure 9: a) SEM image of Cu pillar with solder cap and a cross-sectional view of it assembled [58]. b) Cross-sectional optical image of several assembled Cu pillars [59]. c) SEM image of several unassembled Cu pillars with solder caps [60].

Two common materials used in the different types of off-chip interconnects are copper and solder (Figure 8 and Figure 9). Currently, solder interconnects are being successfully implemented at 150 µm, but there exist large process, electrical performance, and reliability limitations for sub 100 µm pitches that are expected for the next generation of electronic packages [61]. For example, a reliability and process concern for solder interconnects is that at these fine pitches, the majority of the

interconnect is composed of intermetallic alloys due to bonding the solder to metal pads of the chip. The presence of the intermetallic make the interconnects more susceptible to fracture and fatigue cracks. Therefore new sets of interconnect technologies are needed to overcome these challenges and successfully achieve fine pitches. The general requirements needed in new off-chip interconnects include [61]:

1. Electrical properties - high current density capabilities, low electromigration, resistance, inductance, and capacitance
2. Mechanical properties - high strength, with good compliance, and fatigue resistance
3. Process compatibility with existing fabrication and materials

Due to the extraordinary mechanical, electrical, and thermal properties reported for CNTs in recent years, they are a good candidate for potential off-chip interconnects to meet these requirements (Figure 10) [62, 63]. Using modeling, it has been shown by Chiariello et al. that interconnects consisting of MWCNT bundles can have lower electrical resistance than those made up of Cu and SWCNTs even with low site densities for the MWCNTs [64]. Additionally at fine pitches the interconnects need to be able to withstand large current densities to prevent electromigration. The maximum current densities for Cu and solder are ~106 A/cm^2 and ~104 A/cm^2 respectively, while CNTs are 1000 times that [65, 66]. To verify this, it has been shown experimentally that single CNTs don't fail in a continuous accelerating manner that is typical of electromigration failures [67]. The high thermal conductivity of CNT forests [39, 68] has also been investigated for use as a thermal interface material to dissipate heat generated within chips. CNT interconnects therefore could also contribute to lowering the overall device

temperature and improve device performance while improving the thermomechanical reliability due to smaller changes in temperature experienced. Another concern related to temperature is that the typical temperature used to grow CNTs is ~700-800^{o}C. This is not compatible with back-end fabrication processes that require temperatures less than 400-500^{o}C [69]. Two approaches are being developed to overcome this obstacle. The first approach is to determine a method to grow high quality CNT forests at lower temperatures. The second approach is to grow the CNTs on a separate substrate, and then transfer them either onto the chip or carrier substrate.

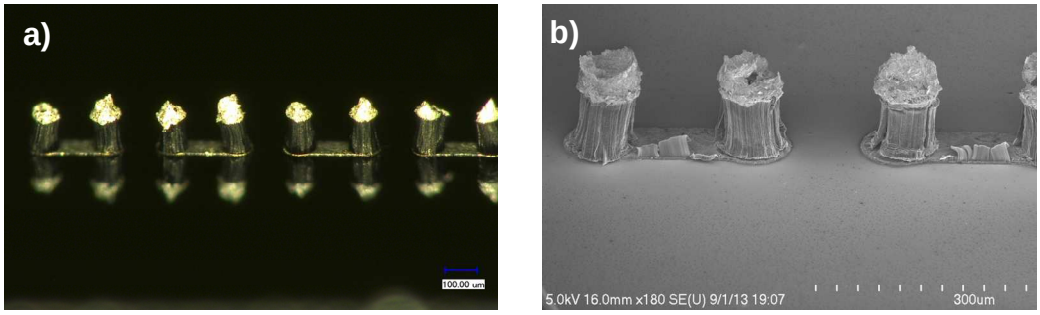


Figure 10: Optical image (a) and SEM image (b) of CNT forests grown on Cu daisy chains with electrically conductive adhesive patterned on the top surface.

The high strength of individual CNTs is well known, with reported values ranging from 11-150 GPa [9, 70] which would create an interconnect that is resistant to mechanical failure. In addition to this high strength, CNT forests have been measured to have a low effective modulus allowing the forests to be deformed greatly. This type of property will create a compliant interconnect and help reduce stresses that occur in the dielectric layers on the chip which originate from the CTE mismatch between the substrate and chip. New low-k dielectric layers are very weak and prone to cohesive and interfacial failure and therefore require new technologies to mitigate the stresses. This benefit has been mentioned in studies demonstrating CNTs as off-chip interconnects, but has not been the focus of any investigation or the mechanical benefit quantified.

There have been several reports that demonstrate CNT forests used as electrical off-chip interconnects with differences in the fabrication and assembly process and dimensions used [36, 63, 66, 69, 71, 72]. One of the earlier demonstrations of CNT forests as off-chip interconnects was presented by Soga et al. (Figure 11) where they grew a blanket layer of CNTs with a height of 100 μm using thermal chemical vapor deposition (CVD) and hot filament CVD at a temperature of 600-800^{o}C [71]. Then a chip was created with a conducting material patterned to form a grid array of connected daisy chains, and conductive adhesive was patterned on the ends of the daisy chains with a pad size of 170 μm and a pitch of ~300 μm. This chip was then pressed into the CNT blanket layer and the adhesive was allowed to cure at 180^{o}C. After curing, the chip was removed from the CNT blanket, allowing the CNTs to be transferred to the chip only where the adhesive was present. The chip with CNTs was assembled to a substrate with a complimentary daisy chain pattern with similar conductive adhesive. In some cases CNTs tips were coated with a conductive metal before assembly to the second substrate in order to improve resistance, which was measured to be as low as 2.3 Ω for a single interconnect. An alternative transfer process has also been demonstrated by Kumar et al. where low temperature solder alloys were used to transfer the CNTs instead of a conductive adhesive [69]. This study showed that the CNT forests can have good wetting with solder and create electrical contacts.

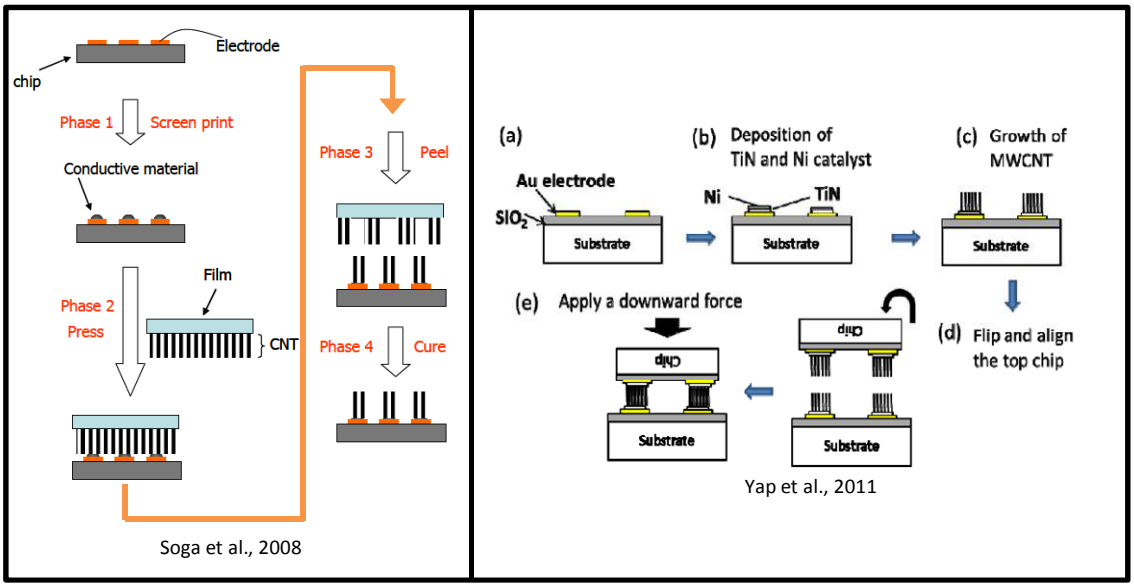


Figure 11: (left) Illustration of CNT transfer process to create CNT interconnects [71]. (right) Illustration of process to assemble CNT interconnects by making CNT-CNT contact [72].

A different approach to create CNT off-chip interconnects is one that does not use solder or adhesives and has been demonstrated by multiple groups. In this general approach (Figure 11) CNT forests are grown on both the chip and the substrate, then the chip is flipped onto the substrate, aligned, and then pressed together so that the two CNT forests penetrate each other [36, 63, 72]. This approach has been investigated in an attempt to utilize reports that CNT to CNT contact resistance is an order of magnitude less than that of CNT tip to metal [73]. Also, these reports are not concerned with process compatibility and avoiding the high CNT growth temperatures. The reports using this alternative method have only obtained values similar to those using CNTs with conducting adhesives, but they have shown that the interconnects are very reworkable due to the ability to attach, detach, and reattach the CNTs [36].

The resistance values presented in most of the studies using different techniques for the CNT off-chip interconnects are high compared to current technologies [36, 63, 66, 69, 71, 72], while one report did demonstrate better values than a conductive adhesive

[36]. To consistently meet the electrical performance requirements it is possible to increase the CNT density, improve the CNT quality, and improve the contact/attachment of CNTs to electrodes all of which are being widely investigated [74]. For example, it has been shown that capillary densification of CNT forest bundles can reduce the measured electrical resistance (including contact resistance) by 400 times, or 2300 times if the change in cross sectional area is included in the calculation [75]. CNT forests still have great potential as a future off-chip interconnect and therefore the mechanical performance and methods on how to incorporate them into finite-element models of electronic packages need to be pursued.

Gaps in Existing CNT Research

While there has been a focus on demonstrating the possible assembly processes of CNT off-chip interconnects and improving the electrical performance, almost no research has been performed on the mechanical performance. In most CNT off-chip interconnect studies, it is commonly stated that CNTs could increase thermomechanical reliability, but there is no quantitative study presenting this. For example, it has been qualitatively shown that chips assembled to substrates using CNT interconnects can be compressed; causing the CNTs to undergo compressive deformation with most of the initial height being recovered after the load is removed [71]. In a different study, 5x5 mm silicon chips and substrates were connected with CNT interconnects with a height of 1.0-5.5 µm and a diameter of 25 µm [76]. These samples were then thermal cycled and showed very little change in resistance after 2000 cycles. It should be noted that there was no CTE mismatch between the chip and substrate in this study and does not offer much insight into the thermomechanical reliability of CNT off-chip interconnects. Therefore there are

gaps in existing research concerning their mechanical performance which should be investigated in order to implement CNT forests as off-chip interconnects.

In addition to these gaps regarding CNT implementation there are also gaps in the measurement of the effective mechanical properties of CNT forests. The issues in current CNT forest effective property measurements were discussed in this Introduction chapter. The measurement of these mechanical properties are needed in order to create accurate finite-element models of the CNT off-chip interconnects that are important for studying and designing next generation electronic packages. These models will demonstrate the mechanical performance and any benefits that CNT interconnects may have on overall mechanical reliability of electronic packages and supplement the other research on the electrical performance of CNT interconnects. Therefore the gaps in existing research to measure the effective properties of CNT forests and implement them as off-chip interconnects include:

- Development of a method to measure the effective modulus of CNT forests that eliminates the consideration of nanoindenter tip geometry and effect of surrounding CNTs while allowing for easy data extraction.
- Investigation of mechanical benefits of CNT forest off-chip interconnects and the incorporation of CNT effective properties in a flip-chip on board analysis.

CHAPTER 2

OVERVIEW AND OBJECTIVES

2.1 General Problem Statement

In the field of microelectronics and electronic packaging the cohesive cracking of thin films, such as low-k dielectrics, is a major reliability concern for current and future devices (Figure 12). This thesis aims to address this issue of cohesive cracking that can occur in dielectric thin films by 1) developing a new test method to measure the cohesive fracture resistance of these thin films to help understand the problem and 2) by investigating the use of CNTs for off-chip interconnects to then mitigate the issue (Figure 13). A fixtureless cohesive fracture measurement technique that uses a material with high intrinsic stress, called the "superlayer", to drive cohesive fracture will be designed and implemented for silicon dioxide dielectric thin films. CNT forests will be investigated as electrical off-chip interconnects, which will include experimental characterization of their effective mechanical properties to implement in finite-element models of chip-to-board microelectronic packages followed by experimental assembly of such packages and accelerated thermomechanical reliability testing to demonstrate the mechanical performance of the CNT interconnects.

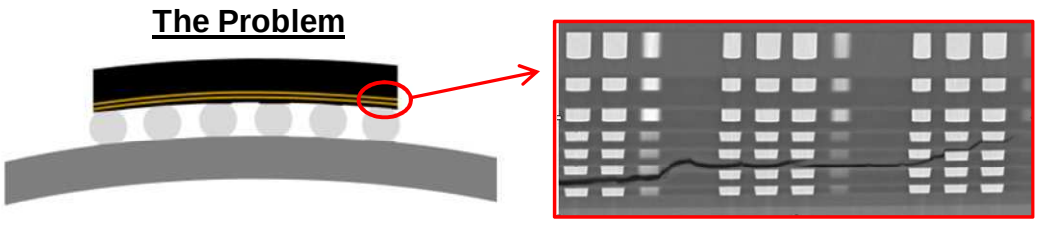


Figure 12: (left) Mechanically coupled chip to substrate with solder balls inducing high stress levels and cracking of dielectric layers (right).

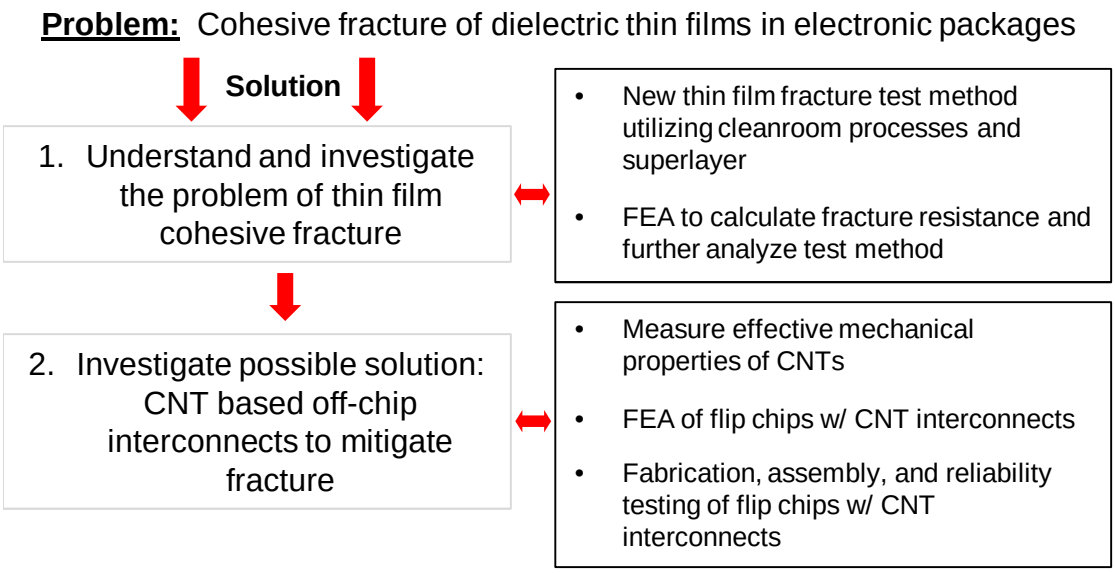


Figure 13: Flow chart of objectives and components of this thesis.

2.2 Thin Film Cohesive Fracture Test

2.2.1 Development and Demonstration of New Thin Film Cohesive Fracture Test

The first objective of this thesis addresses investigating and understanding the fracture of the dielectric films, and will be accomplished by developing a new test method to measure the cohesive fracture resistance of such thin films (Figure 14). This new cohesive fracture test method possesses the following advantages for testing thin films as compared to more traditional approaches:

- Eliminates the possible undesirable effects of the substrate by using freestanding films.
- Does not require fixturing, clamping, or attachment for the application external forces or to measure resulting displacements.
- Uses fabrication processes that create representative thin films of the target application for the material.

- Does not require expensive, complicated, or custom measurement equipment.

The majority of these advantages of this new test method is due to the test's utilization of cleanroom fabrication processes and a highly-stressed superlayer material to drive fracture in the free-hanging test material and avoids the need for fixturing and the application of external loads. Therefore, the early sections of this thesis focus on the design of this new cohesive fracture test method with respect to the geometric design of the test structures and creating the overall cleanroom fabrication process. Then the test will be demonstrated by measuring the cohesive fracture resistance of several silicon dioxide films with thicknesses ranging from ~100 to ~400 nm. The measured cohesive fracture resistance value will then be compared to values for silicon dioxide obtained in literature.

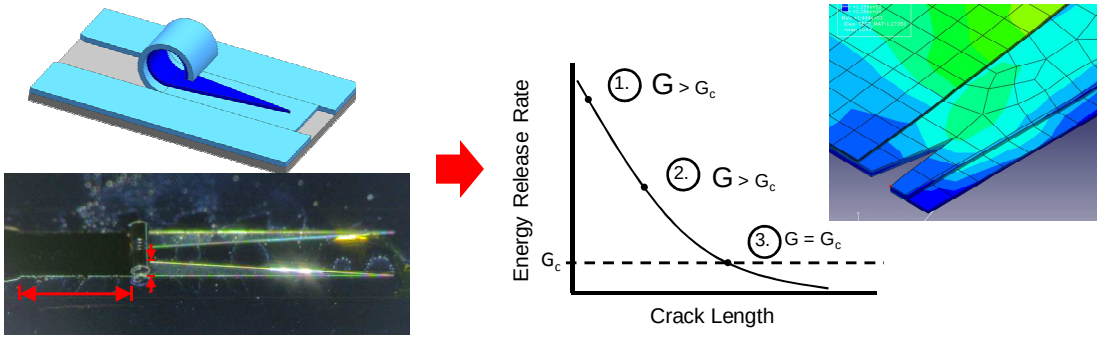


Figure 14: (left) Fabrication of cohesive fracture test. (right) Finite-element analysis of fracture test.

2.2.2 Finite-Element Analysis of Cohesive Fracture Test

Another main component of this cohesive fracture test method is the use of finite-element analysis of the experimental results of the test specimens. Finite-element analysis will be used to demonstrate the basic fracture mechanics concept of the new test method and how the shape and stress of the superlayer provide a measurement of the cohesive fracture resistance. Additionally an investigation will be done using finite-

element analysis to understand the effects of some of the main parameters on the test, such as film thickness, superlayer thickness, superlayer stress, and test sample geometry. Lastly, the material properties of the test material in the model will be varied in order to investigate the possibility of utilizing this new test method to measure the fracture resistance of materials other than silicon dioxide that are used in a wide range of applications.

2.3 CNT Based Off-Chip Interconnects

After the cohesive fracture test method has been developed to investigate the fracture resistance of thin films, the second objective of this thesis is to investigate the use of CNT off-chip interconnects to mitigate this issue of cohesive fracture of dielectric layers in electronic packages (Figure 15). In electronic packages, one of the main causes of cohesive cracking of the dielectric layers is thermomechanical stresses that arise from the mismatch between the values of the CTE's of the silicon chip and the substrate that they are attached to by off-chip interconnects. Traditional off-chip interconnects, such as solder balls, rigidly connect the silicon chip to the substrate and mechanically couple them. This creates the high level of thermomechanical stresses in the chip that cause cracking of the dielectric layers. CNTs have been proposed in literature as possible off-chip interconnects due to their electrical conductivity, high strength, and low effective modulus. Interconnects with a low effective modulus would allow the silicon chip to be mechanically decoupled from the substrate, allowing them to deform independently when subjected to external temperatures or loads, and therefore reduce the stresses in the dielectric layers and mitigate cohesive fracture.

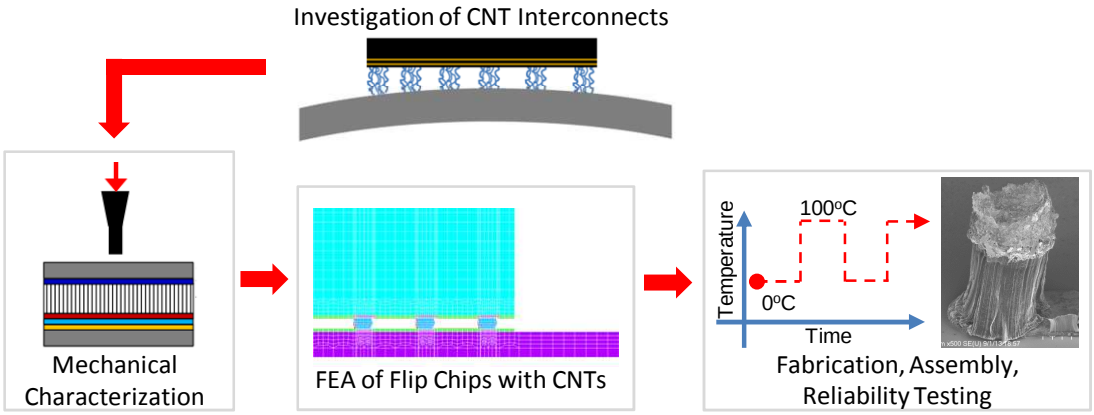


Figure 15: Components of the investigation of CNTs as off-chip interconnects.

2.3.1 Mechanical Characterization of CNTs for Off-Chip Interconnects

The goal of the second component of the thesis is to investigate the mechanical performance of CNT off-chip interconnects. Such a quantitative investigation is absent in current literature as discussed in Section 1.2.3 (Gaps in Existing CNT Research). To accomplish this goal it is first necessary to characterize the mechanical properties of CNT forests to demonstrate their low effective modulus compared to the high reported values for a single CNT in tension. This characterization will be executed by utilizing three different test methods including nanoindentation, small scale tensile testing, and an SEM with load-cell compression fixture. These test methods will provide effective modulus measurement values in compression, tension, and allow for semi-insitu observation of the nature of deformation of the CNTs.

2.3.2 Finite-Element Analysis of Electronic Packages with CNT Interconnects

The effective modulus measurements for the CNT forests will then form the basis for the mechanical material property model for the CNT interconnects in a finite-element analysis of a silicon chip assembled to a FR4 substrate. The results of this finite-element

analysis will then be compared to the same electronic package utilizing traditional solder balls. This will demonstrate the mechanical decoupling of the silicon chip from the FR4 substrate for the case of CNT interconnects, and therefore a reduction of chip stress and mitigation of dielectric cracking. Additionally, mechanical performance investigations will be conducted with these finite-element models such as CNT height and material model aspects (i.e. isotropic vs. transversely isotropic) provide insight for potential future use of CNT based off-chip interconnects.

2.3.3 Fabrication, Assembly, and Thermomechanical Reliability Testing of CNT Interconnects

The final aspect of the investigation of the mechanical performance of CNT based off-chip interconnects is experimentally testing their thermomechanical reliability. Therefore, CNT interconnects with a diameter of ~120 μm and a height of ~100 μm will be grown on copper daisy chains, and then assembled and attached to FR4 substrates with electrically conductive adhesive. The assembled packages will then be subjected to cyclic thermal shock testing to obtain a measurement of their thermomechanical performance by monitoring the electrical resistance of the daisy chained CNT interconnects. This will then be compared to similar flip chip packages utilizing solder balls without underfill and other new nontraditional interconnects and provide a quantitative basis of the mechanical performance of CNT off-chip interconnects.

2.4 Summary of Objectives

Below is a list of the objectives that will be addressed in the following chapters of this thesis.

- To develop a new fixtureless experimental test technique for measurement of thin film cohesive fracture resistance using a stressed superlayer and generation of cohesive fracture data for SiO_2 thin film.
- To develop finite-element models for calculation of cohesive fracture resistance of thin films and understanding the effect of key test parameters.
- To develop two test techniques to measure effective modulus of CNT forests and generate data for values of CNT forest effective modulus.
- To develop a methodology to mechanically model CNT based electrical off-chip interconnects in finite-element analysis of flip chip electronic package and to demonstrate the mechanical benefits CNT interconnects.
- To fabricate, assemble, and thermo-mechanically test flip chips that utilize CNT based off-chip interconnects to quantitatively demonstrate their mechanical performance.

CHAPTER 3

METHOD TO MEASURE TENSILE STRENGTH OF LOW MODULUS THIN FILMS USING STRESSED SUPERLAYER

3.1 Introduction

This chapter presents and discusses early research conducted for this thesis that led to the development of the new cohesive fracture test presented in Chapter 4. While the cohesive fracture test discussed later in Chapter 4 is one of the two main topics of this thesis, this chapter focuses on a new method to measure the tensile strength of low modulus thin films. This chapter serves to present and demonstrate this new tensile strength measurement technique, while also providing insight and appreciation for the genesis of the thin film cohesive fracture test of Chapter 4. This test method to measure the tensile strength of thin films is similar to the cohesive fracture test since they both 1) use a highly-stressed film to drive deformation of the test material and 2) both use photolithography and clean room processes to fabricate and perform the tests. These two characteristics of the two different test methods allow them to possess similar advantages when applied to the mechanical testing of thin films.

One of the advantages for this tensile strength measurement technique is associated with fixturing of the test material and with the material test samples themselves. To conduct most standard mechanical testing techniques, first a material specimen is created, such as a dog-bone sample for uniaxial tensile testing to measure the tensile strength or a compact specimen for fracture toughness measurement. This specimen is then held in place with mechanical grips or other fixturing devices allowing external loads to be applied to the specimen to cause deformation and subsequent failure.

The geometric dimensions of thin films and their low strength make the measurement of their mechanical properties inherently difficult using traditional methods such as this. In general, thin films of any type of material (metals, polymers, oxides, etc.) with thicknesses in the micro and nanometer range are extremely fragile, difficult to handle, difficult to hold in place and fixture, and the application of externally applied loads can cause unwanted local stress effects [77]. It is therefore desired to utilize a test method for thin films that does not require such fixturing or externally applied loads when measuring their mechanical properties. The tensile strength test technique presented in this chapter is applicable for measuring the tensile strength of a wide range of nano and micro-scale, thin, low strength materials that cannot otherwise be measured accurately through conventional fixture-based load application techniques. A material that possesses such characteristics is parylene-C, and was therefore chosen to demonstrate the proposed tensile strength test technique. This polymer has a wide range of thin film applications such as a moisture barrier coating, electrical insulation in microelectronic devices, and as structural components in MEMS devices [78-80]. In these applications, design for reliability is an issue due to the exposure to external loads that can result in material failure. It is therefore desired to measure mechanical properties such as the tensile strength for thin film parylene-C, but little research has been conducted on measuring it.

3.2 Test Concept

The proposed test method to measure the tensile strength of thin films avoids the previously mentioned issues by using basic lithography processes to mechanically test materials without traditional fixturing or the application of external loads. The main concept behind this method is to cause failure of the thin film by depositing a material

with high intrinsic tensile stress on top of it. A similar concept has also been used to measure the interfacial fracture strength of copper thin films on glass by Bagchi et al. [81] and is also used in the cohesive fracture test method that is a major component of this thesis and discussed in Chapter 4. In this thesis, the highly-stressed material is called the "superlayer". Before discussing the concept of the proposed tensile test technique it is important to understand the concept of the superlayer and how it can be used to cause cracking in parylene films without external fixturing or loads.

In general, all thin films have some sort of stress state. The total stress is composed of an extrinsic component from external loading after material deposition and a thermal component which arises from differences in the coefficient of thermal expansion between the film and substrate, and an intrinsic component. The test techniques presented in this thesis utilize only the intrinsic stress component. This intrinsic stress is caused by the grain structure that develops in the thin film as it is deposited. Using a magnetron sputtering of chromium thin films it is possible to control the grain structure by altering the argon gas pressure that is present to sustain the plasma used to sputter the chromium. In this investigation, a Unifilm® magnetron sputter machine was used with argon pressures ranging from 2-6 mTorr, which produced film stress values from +1.5 GPa to +1.0 GPa. A detailed discussion and explanation on thin film intrinsic stress is given in Section 4.2 and should be used as a reference for this investigation.

The stress that this superlayer possesses is the key component to this test technique to measure the tensile strength of thin films. This high stress in the superlayer induces elevated magnitudes of stress in the test material that has been deposited below

the superlayer. Stress in the test material that exceeds its tensile strength causes failure and is visually signified by cracking of the material. Different magnitudes of stress in the test material can be induced by different magnitudes of stress in the superlayer and different superlayer thicknesses. During the test process to determine the upper and lower boundaries of the tensile strength, first a superlayer with specific stress and thickness is used. Then, if cracking does not occur with this superlayer, the test is repeated with a superlayer of greater thickness or stress magnitude (illustrated in Figure 16). Then if cracking occurs, the test can be repeated with a lower stress magnitude or thickness. With this iterative process the material's tensile strength can be determined, and in this study it is demonstrated with parylene-C.

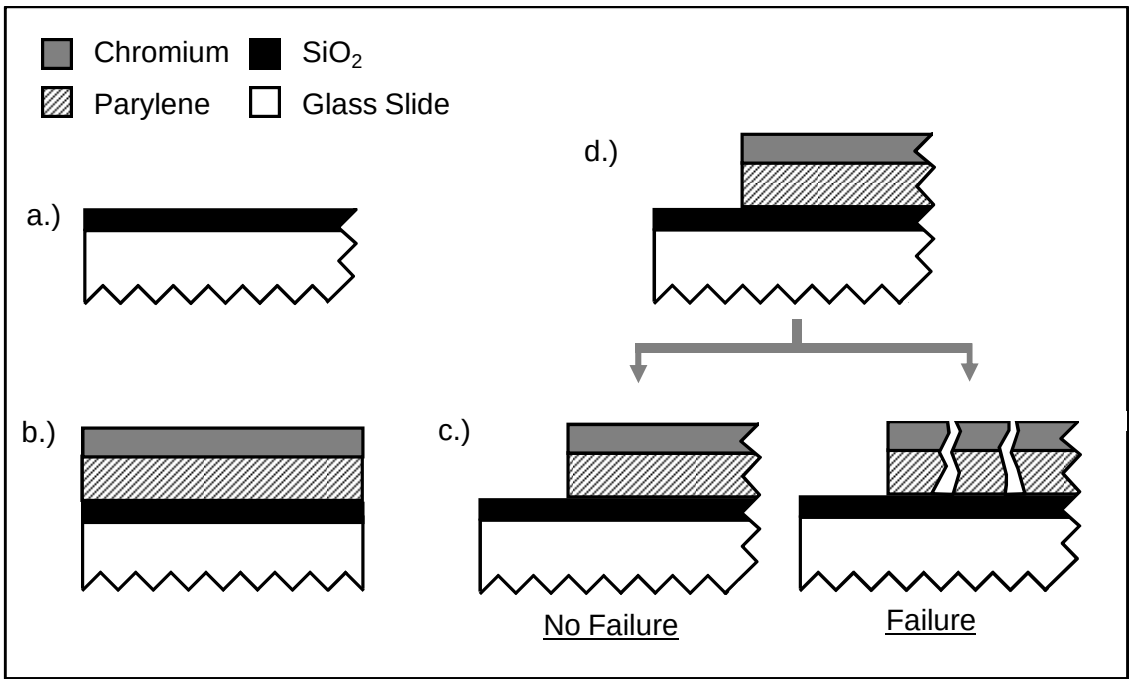


Figure 16: Side view of test samples during the fabrication process. Step c) shows the possible outcomes of No Failure with no cracking of the material occurring, or failure occurring which is signified by cracking of the materials.

3.3 Test Fabrication

The fabrication of this process is outlined in Figure 16 and begins on a glass slide with 100 nm of SiO_2 deposited on it with a Uniaxis® PECVD. A Lapcoater® 2PDS 2010 was then used to deposit 1 μm or 3.46 μm of parylene-C. Next a blanket layer of chromium was deposited on top of the parylene with a Unifilm® PVD Sputterer. The chamber pressure was adjusted to induce high levels of tensile intrinsic stress in the chromium. Stress magnitudes ranging from 1-1.4 GPa were utilized in this study. The chromium was then patterned into strips approximately 200 μm x 2000 μm with Shipley® 1813 photoresist. This chromium pattern was then used as the masking layer to pattern the parylene. A Plasma-Therm® RIE with O_2 plasma was used to etch the parylene. Once the strips were defined, they were observed for cracking to signify if the stress created by the chromium superlayer in the parylene was above the tensile strength. This process was then continued with four different chromium thicknesses and/or intrinsic stresses to determine the tensile strength of parylene-C. The characteristics and dimensions of the samples that were fabricated are summarized in Table 2.

Table 2: Dimensions and characteristics of the fabricated experimental test samples and dimensions used for the different FEA.

Sample #	Parylene Thickness (nm)	Chromium Thickness (nm)	Nominal Chromium Stress (MPa)
1	1000	250	1300
2	1000	25	1300
3	3460	25	1000
4	1000	50	1000

3.4 Test Finite-Element Analysis of Experimental Test Specimens

In this study, finite-element analysis (FEA) was used to determine the stress in the parylene-C film caused by the stressed superlayer and extract the tensile strength of parylene-C from the experimental data. A 2-dimensional ABAQUS® model for each of the test samples was created using CPE4R plane strain elements. The models consisted of layers of SiO_2, parylene-C, and chromium as shown in Figure 16 and Figure 17. The linear elastic material properties used for each of the materials included: SiO_2 (Poisson's ratio, ν=0.25, Modulus of Elasticity, E=64 GPa [82]), parylene-C (ν=0.4, E=4.75 GPa [83]), and chromium superlayer (ν= 0.31, E=260 GPa [84]). To constrain the model, the bottom of the SiO_2 layer was fixed in all degrees of freedom (Figure 17) because the actual test specimens are fabricated on a glass substrate of much greater thickness (~1000 μm) than the films included in this FEA model. For loading conditions, the chromium layer was modeled with the nominal tensile intrinsic stress that is given in Table 2 for each test sample. Additionally an intrinsic stress of 25 MPa [85, 86] was included in the parylene-C layer due to stresses developed during the deposition process.

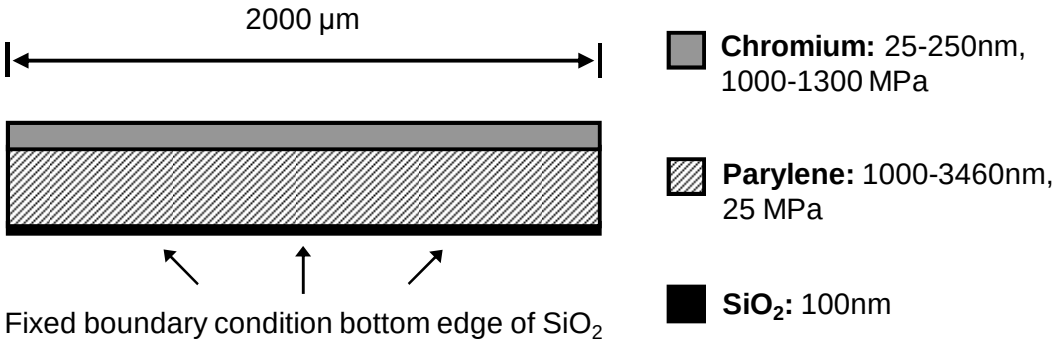


Figure 17: Side view of 2-dimensional finite-element model of entire test strip. Bottom edge of SiO_2 has all degrees of freedom fixed as a boundary condition.

3.5 Results and Discussion

In each of these models, the highest stress values (von Mises, principal, and Tresca) were found to be in the region near the ends of the test strips as in Figure 18 and Figure 19. Experimentally, such stress levels would cause propagation of cracking in the entire sample if this high stress is above the tensile strength, and therefore result in cracking of the entire strip. This mode of failure of cracking along the entire strip was expected and observed during experimentation and signified failure. The maximum von Mises, principal, and Tresca stress was determined through finite-element analysis for each of the samples and is given in Table 3. In general these results demonstrate that the stress in the parylene is increased by either increasing the intrinsic stress or thickness of the superlayer.

The experimental results showed that the tensile strength is exceeded when the test sample shows cracking. During the testing, cracking was observed with samples 1, 2, and 4 and no cracking with sample 3. Figure 20 (left) shows the cracked sample 1, where the cracking of parylene-C also results in the cracking of the superlayer, and Figure 20 (right) shows sample 3 with no cracking present. The stress that the parylene is experiencing is determined from the FEA results discussed in Section 3.4 and above in Section 3.5. Using both the FEA and the experimental results of samples 2 and 3 it is seen that the tensile strength of parylene-C is in the range of 57 MPa considering the von Mises stress. This result is similar to measured bulk values of 55 MPa and measured thin film values of 59 MPa [83]. The FEA results also show that parylene failure occurs at higher stress values if principal stress (maximum: 72.5 MPa) or maximum Tresca stress (maximum: 62.3 MPa) is used as the failure criteria.

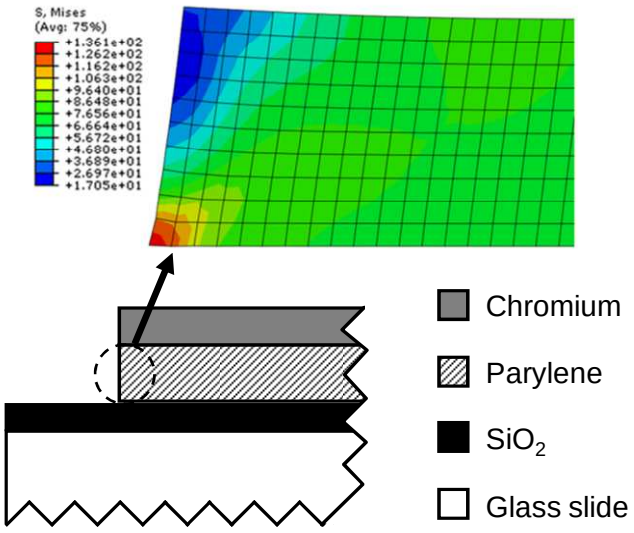


Figure 18: Zoomed-in contours of von Mises stress in parylene-C from a finite-element model for test sample #1 (Unit for stress is MPa).

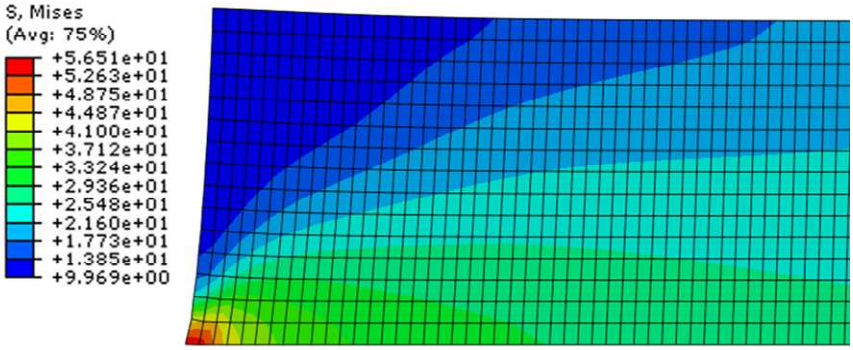


Figure 19: Zoomed-in contours of von Mises stress in parylene-C from a finite-element model for test sample #3 (Unit for stress is MPa).

Table 3: FEA and experimental results.

Sample #	Maximum Total von Mises Stress in Parylene (MPa)	Maximum Total Principal Stress in Parylene (MPa)	Maximum Total Tresca Stress in Parylene (MPa)	Experimental Result
1	136.1	177.5	153.2	Crack
2	57.0	72.5	62.3	Crack
3	56.5	70.7	61.9	No Crack
4	60.6	77.1	66.5	Crack

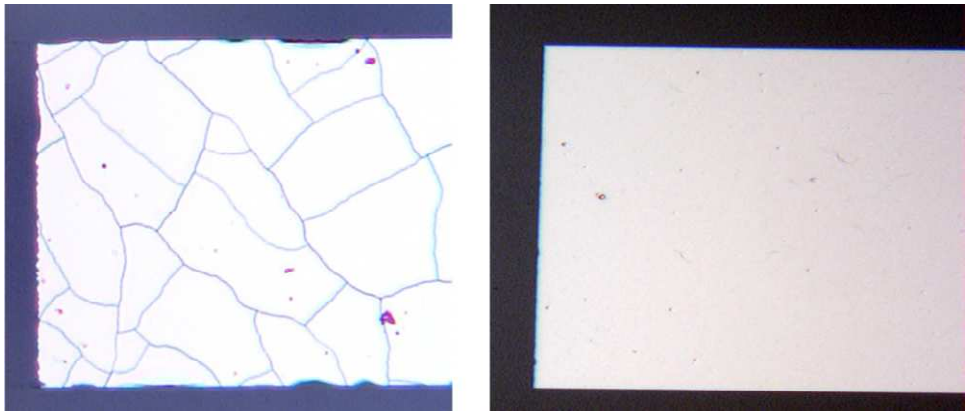


Figure 20: Left optical image is a top-view of cracking observed in sample #1 and right image is a top view of sample #3 with no cracking present.

3.6 Conclusion

In this chapter, a new testing technique to determine the tensile strength of low strength thin films was demonstrated by measuring the tensile strength of the polymer parylene-C. The technique presented avoids the issues associated with testing thin films by utilizing simple photolithography based sample preparation, not requiring fixturing of thin films, and is driven by the high intrinsic stress of the superlayer film. Additionally, this technique uses finite-element analysis to extract the tensile strength from the experimental data. It was found that von Mises stress failure criteria produced values for tensile strength close to reported bulk and thin film values, while principal stress and Tresca stress failure criterion values were greater. The results presented in this study show that this test method is viable for determining the tensile strength of similar thin film materials with low tensile strength. Lastly, this chapter demonstrates a second new test technique contained within this thesis that uses a highly-stressed superlayer to measure the mechanical properties of thin films. This method to measure the tensile strength of low strength thin films by utilizing a superlayer serves as a precursor for the

superlayer based method to measure the cohesive fracture resistance of thin films that is a major topic of this thesis and presented subsequently in Chapter 4.

CHAPTER 4

COHESIVE FRACTURE TEST FABRICATION AND EXPERIMENTAL RESULTS

4.1 Introduction

Thin films of materials are currently being used in a wide range of applications in fields such as microelectronics, NEMS/MEMS, solar powered devices, and medical devices. In these applications, the thin films can be used as a coating on a thicker material or several layers of different thin films can be used to create a specific device. In both of these general types of applications it is common for mechanical failures to occur due to thermal or mechanical loads that the devices experience during their fabrication or lifetime (Figure 21). These mechanical failures can either be interfacial fracture, which is cracking occurring at the interface of the thin films, or cohesive cracking, which is cracking that extends through the thickness of the thin film. In microelectronic devices that are composed of many layers of thin films, interfacial and cohesive cracking is a major reliability issue. Specifically, the microelectronic industry has been encountering a major technological hurdle with such cracking occurring in dielectric thin films and has devoted a great amount of energy and resources to understand the interfacial and cohesive fracture strengths of thin films. This is due to there being no standard techniques to measure the cohesive or interfacial fracture toughness of thin films (as discussed in Section 1.2.1). While there are many standard tests to measure the cohesive fracture toughness of bulk materials, these measurements may not be applicable to their respective thin films due to: 1) surface interface effects that are more pronounced at small scales, 2) limited number of grains in a given volume,

3) the materials may only be available in thin film form and not in bulk and 4) the effect of manufacturing processes used.

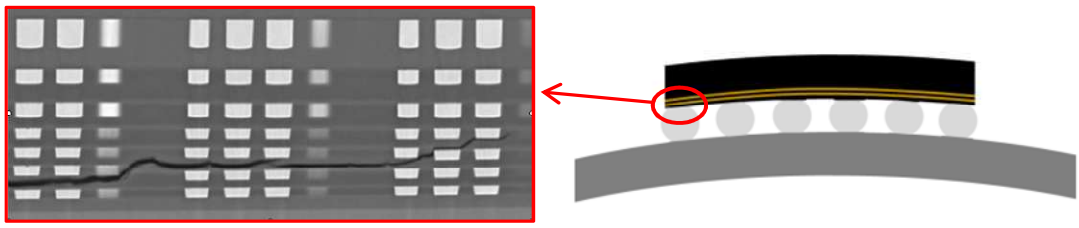


Figure 21: Left SEM image shows cross section of Back End Of Line (BEOL) dielectric layers with metallization lines [6]. Image shows cohesive and interfacial cracking occurring in the dielectric layers caused by mechanical or thermal CTE mismatch loading on the flip chip connected to a substrate by rigid solder ball interconnects (right image).

It is for these reasons, and those discussed in more detail in Section 1.2.1, that new tests have been developed to specifically measure the cohesive fracture toughness of thin films. Recent thin film test methods include those that are based on the use of a nanoindenter system and other microtensile test methods that employ micro-fabrication techniques to eliminate the use of a nanoindenter. The nanoindenter based techniques have the advantages of using a commercial system, but they are very expensive. Additionally while the sample preparation of these techniques can be very simple, and consist of just the thin film deposited on a substrate, there are still several disadvantages including:

1. The stiffness and hardness of the substrate can affect the measurements with the nanoindenter [13, 21].
2. Complex stress fields occur at the indenter tip and make the analytical solutions used to determine the toughness difficult and rigorous [87, 88].
3. Determining and creating the desired crack geometry, and then locating and measuring the crack can be difficult and add uncertainty to the results [13].
4. This method requires access to nanoindenter, which is an expensive system.

It is because of these challenges and disadvantages of such nanoindenter based methods, that other microtensile test methods have been developed. These methods typically try to eliminate the effect that the substrate has on the thin film's properties by using free-hanging/standing beams or membranes. It is also desired to eliminate the need for the nanoindenter system to reduce cost, which some of the microtensile methods achieve. But in the process of designing a test method that does not utilize a nanoindenter system, complicated and customized mechanisms are created to either apply the force to drive fracture or measure displacements/crack lengths. Additionally some of these methods require fragile fixturing and attaching of the test specimens, which is a difficult task when dealing with micro/nano thick films. Therefore, this chapter presents a new test method to measure thin film cohesive fracture toughness that: 1.) does not require complicated/expensive equipment, 2.) does not require external fixturing or application of forces or clamps, 3.) uses freestanding films to eliminate the effect of the substrate material, 4.) and uses standard fabrication processes that create representative film compositions occurring in the target application.

In addition to these desired test characteristics mentioned, the presented cohesive fracture test method has additional advantages. One of these advantages is that during the fabrication of this test technique, the photolithography fabrication process allows for many test samples to be fabricated and tested at the same time due to the parallel nature of photolithography fabrication. Therefore, each wafer results in many critical energy release rate data points of the target test material.

Also, the next generation of low-k dielectric materials is achieving their low dielectric constants from increased levels of porosity [3-6]. Testing such films using

more traditional thin film fracture test methods such as nanoindentation becomes difficult, especially while the thickness of these films is also decreasing. Generally when using nanoindentation, it is desirable to keep the indentation depth to be less than $1/10^{th}$ of the thin film thickness so that the substrate properties do not influence the test results [89-92]. With increasingly thin materials used in microelectronic applications, it is difficult to extract fracture properties by keeping the $1/10^{th}$ indentation depth guideline. Also, the increased porosity of new low-k dielectric thin films creates an issue in determining the "actual" area of contact of the porous material with the nanoindenter tip. Such an "actual" area of contact is important to for the nanoindentation analysis [91]. Therefore there is a need to for new thin film fracture tests to be applicable to advances in future semiconductor and thin film technologies.

The main concept behind this new test method is to cause cohesive failure of the thin film by depositing a material with high intrinsic tensile stress on top of it. This thin film with a high tensile intrinsic stress is also the aspect of the test method responsible for many of the test's unique characteristics and advantages. In this study the highly-stressed material is called the "superlayer". Before discussing the concept of the proposed cohesive fracture test technique it is important to understand the concept of the superlayer and how it can be used to initiate and propagate cracking in thin films without external fixturing or loads.

4.2 Engineered Thin Film Stress: Superlayer Concept

All thin films have some sort of stress state. The total stress is composed of an extrinsic component from external loading after deposition and a thermal component which arises from differences in the coefficient of thermal expansion between the film

and substrate, and an intrinsic component. The test technique presented in this thesis utilizes only the intrinsic stress component. Two common models to explain intrinsic stress in deposited metal films are the Grain Boundary Relaxation model and the Shot Peening model [93-96]. These models can be used to explain the general relationship between the intrinsic stress and the sputter deposition parameter of argon gas pressure that is shown in Figure 22 [96]. During the sputter deposition process, the argon gas is used to create the plasma in the deposition chamber allowing material to be sputtered from the source material target onto the substrate. When the argon pressure in the sputter chamber is low, the target metal atoms will collide less with the argon ions in the chamber. Less scattering of the target atoms will occur and therefore result in a dense pattern of target material on the substrate. The interatomic distance of such a deposited film is less than the equilibrium spacing, which creates a compressive intrinsic stress in the deposited film as shown in region 1 of Figure 22. If the argon pressure in the sputter chamber is increased, the target atoms will collide more with the argon ions present, resulting in a coarser and less dense deposited film. The interatomic distance will be larger than equilibrium spacing in this case and create a tensile intrinsic stress in the deposited film (region 2 in Figure 22). If the argon pressure is increased further, the tensile stress will reach a maximum value and then decrease as the argon pressure is increased (region 3 in Figure 22). This is due to increased voids in the film microstructure and thus decreased density that cannot sustain continued increases of stress. Therefore, in region 3, the stress decreases with increased sputter chamber pressure [93]. This phenomenon allows for a wide range of stress levels by using various argon pressures and sputtering material. For example, in this study chromium

superlayers were deposited using a Unifilm^{TM} PVD Sputterer with sputter chamber pressures ranging from 2-6 mTorr. The stresses produced ranged from +1.51 GPa to +1.02 GPa and are shown in Figure 22. The range of argon pressures used in this study for chromium was only in the tensile stress region and is consistent with the pattern described in region 3 of Figure 22. Others have demonstrated similar results using various materials over a wider range of pressures [94, 97].

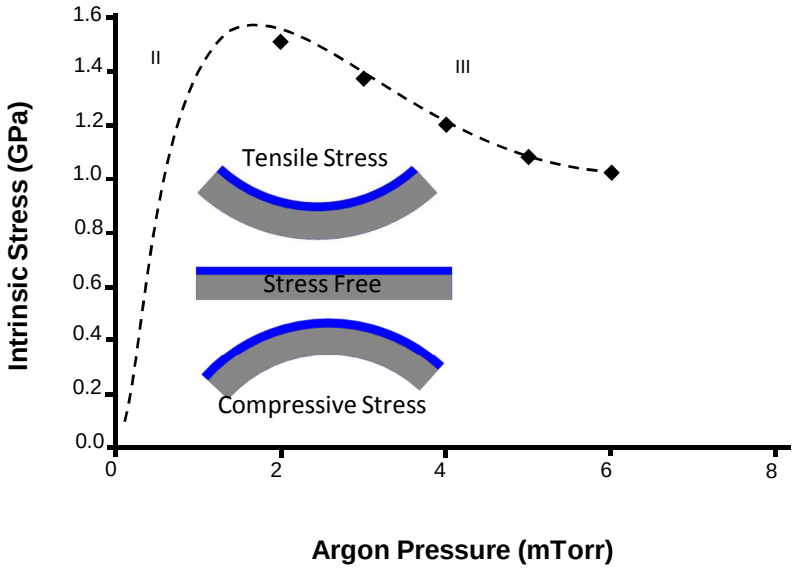


Figure 22: Illustrates general relationship between argon gas pressure and intrinsic stress in thin films for regions two and three. Region one is not shown, which would include a continuation from region two down to a compressive stress region. Additionally, actual data for argon sputter pressure vs. measured intrinsic stress of chromium using magnetron DC sputtering has been overlaid on the general relationship.

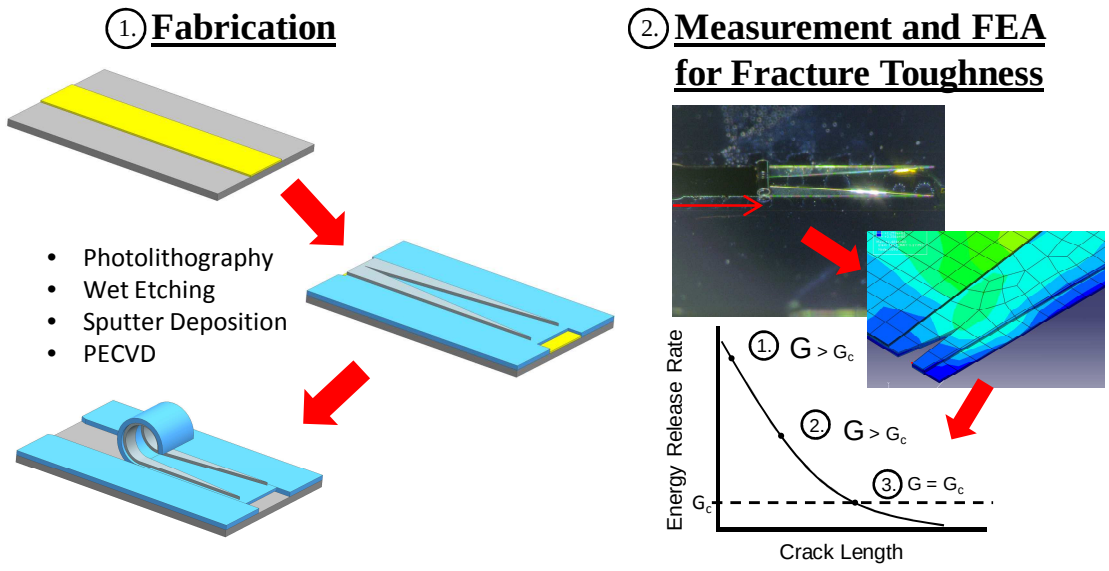


Figure 23: Illustration depicts the two main components of the superlayer fracture toughness test. First, the fabrication of the test and then second, the measuring of fractured samples and the FEA of the results to determine the test materials fracture toughness.

4.3 Superlayer Test Method to Measure Thin Film Fracture Resistance

To measure the cohesive fracture toughness of thin films a new test method has been developed and is presented in this section. To create a test method that overcomes the issues mentioned in Section 1.2.1 (Gaps In Existing Thin Film Fracture Test Methods), photolithography methods are used to pattern and create rectangular free-hanging thin film specimens that are attached at two opposite edges to a rigid silicon substrate, and then a highly-stressed superlayer material is deposited and patterned into a triangular shape on top of the free-hanging test material. Once this super layer is patterned, and the test material is released, the stress from the superlayer initiates and drives crack propagation through the test material. This crack length is then measured and the experimental specimen is modeled in FEA with the same geometries, crack length, and stress states to calculate the fracture toughness of the test material. The following subsections (as illustrated in Figure 23) will go into detail on: 1.) The

fabrication process to create the test samples with the superlayer 2.) The experimental results of several test runs and the FEA of these experimental results to calculate the fracture toughness of the test material.

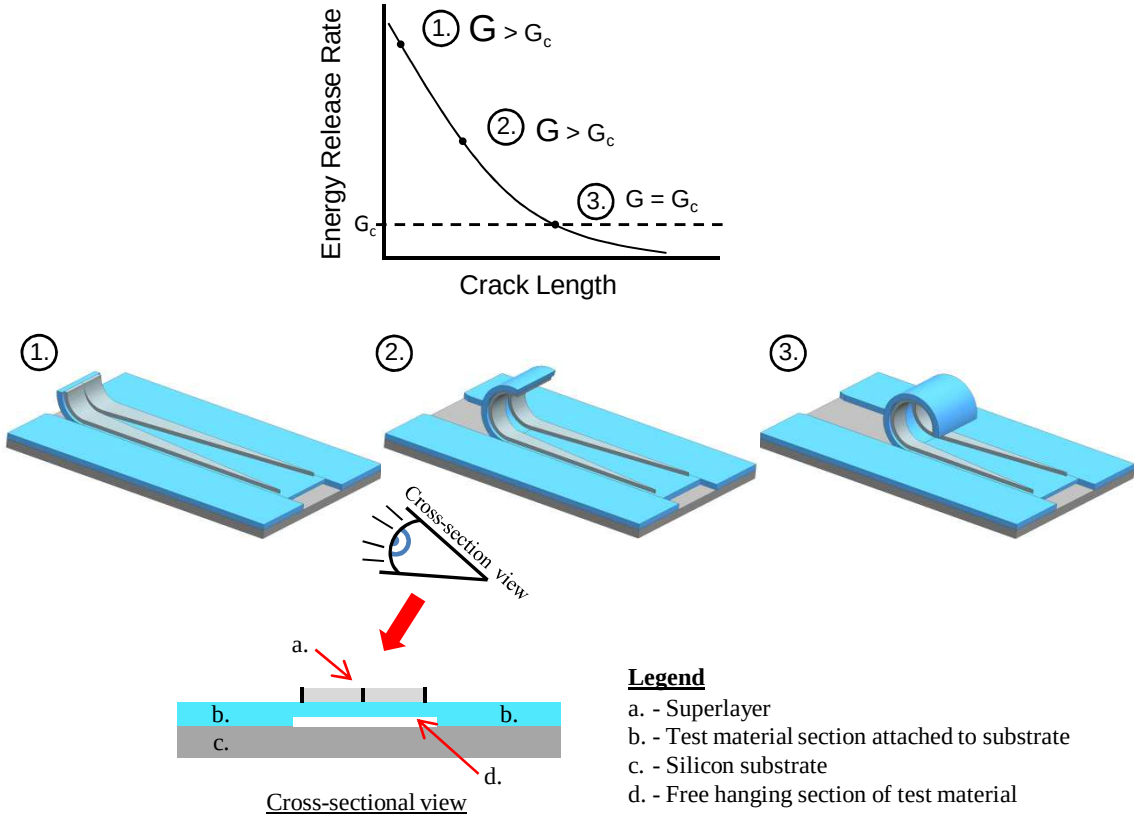


Figure 24: Illustration of main test concept of decreasing energy for fracture as the crack propagates. The decreasing energy is due to the triangular shape of the superlayer. Also, shows the general geometry of the test samples with a section of the test material that is free-hanging with the triangular superlayer on top.

4.4 Cohesive Fracture Test Concept

This outlined test method measures the cohesive fracture toughness of the target test material (i.e. silicon dioxide) by using the highly-stressed superlayer deposited on top of the test material. The energy of the highly-stressed superlayer is used to generate fracture and drive crack propagation through the thickness of the free-hanging test material. The amount of energy supplied by the superlayer is dependent on the intrinsic

stress, thickness, and width of the superlayer material. Therefore the geometry of the superlayer can be used to help determine the critical fracture energy of the test material. For example, Figure 24 and Figure 27 (STEP IV and V) shows a triangular shaped superlayer of constant thickness deposited on top of a freestanding test material film fixed at the edges to a substrate beneath it. At the crack initiation locations at the base of the superlayer triangle, if the energy supplied by the superlayer is greater than the critical fracture energy of the test material, cohesive cracking will occur and propagate. As the crack propagates, the width of the superlayer decreases due to its triangular shape, and therefore the energy supplied by the superlayer also decreases. The cohesive crack will then continue to propagate as long as the energy supplied by the superlayer at the crack tip is greater than the critical fracture energy of the test material. Crack propagation will cease when the energy supplied by the superlayer is equal to the critical fracture energy of the test material, and therefore provide a measurement of the fracture toughness of the test material. This is further illustrated in Figure 24 and some example test specimens that have cracked are shown in Figure 25. The energy approach to fracture mechanics states that fracture occurs when the energy available for crack growth is sufficient to overcome the resistance of the material [30]. This criterion for cohesive fracture to occur and propagate is:

$$G > G_c \tag{9}$$

Where G is the available energy release rate (ERR) and G_c is the critical energy release rate, which is a measure of the fracture toughness of the material. The energy release rate can also be defined as:

$$G = -\frac{dU}{dA} \tag{10}$$

Where *dU* is the change in strain energy for a change in crack face area *dA*, as the crack is grown. In this proposed test method, the strain energy decreases as the crack grows due to the decreasing width of the superlayer. Therefore the *dU* value decreases as the crack grows until it reaches a value that causes $G=G_c$ and provides a value for the fracture toughness of the film (Figure 24).

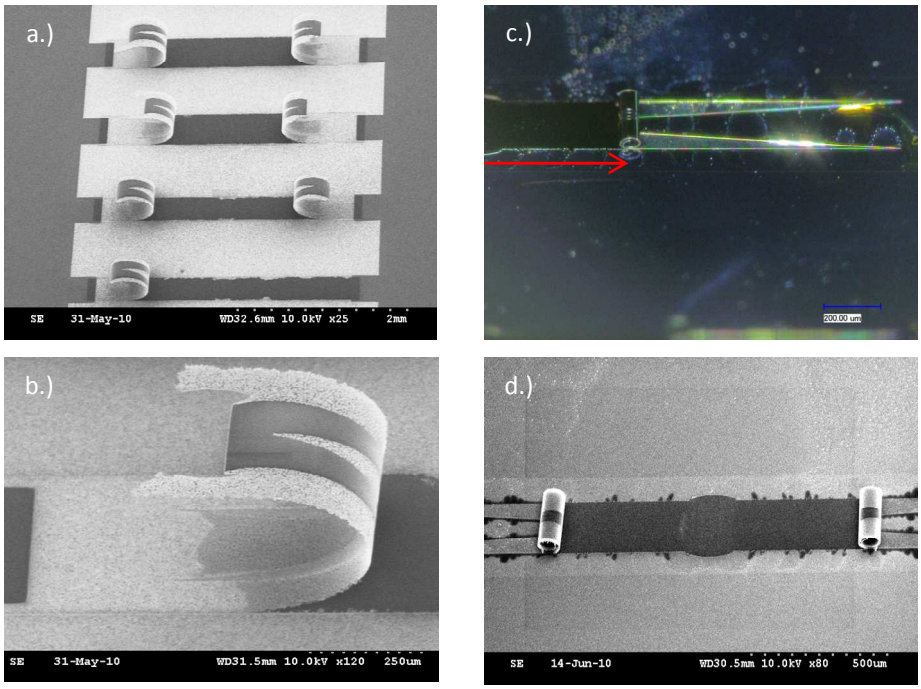


Figure 25: Fabricated test specimens after they have been released and allowed to cohesively crack. a-b.) 1200 nm of SiO_2, 200 nm of Cr with an intrinsic stress of 1.2 GPa. c-d.) 315 nm of SiO_2, 120nm with an intrinsic stress of 1.2 GPa.

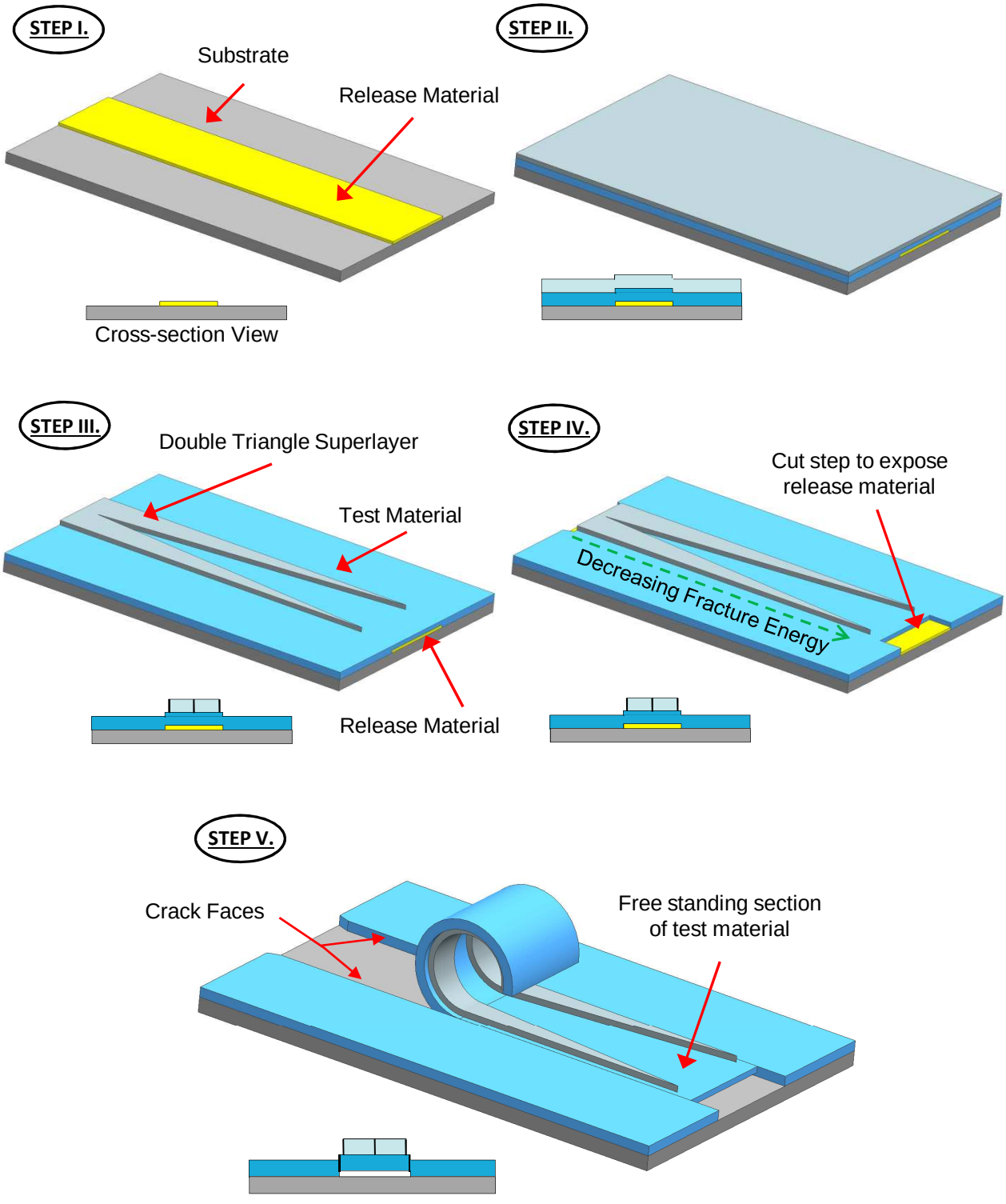


Figure 26: Fabrication process for the cohesive fracture test technique.

4.5 Test Sample Fabrication Process

The fabrication process of this test method utilizes standard lithography and material deposition processes to create the test specimens. This ensures that the materials being tested are representative of those of interest in industry and also compatible with their standard processes. Silicon dioxide was chosen as the test material to demonstrate this method since it has been commonly used as a dielectric material in electronic packaging, but currently it is being replaced by new propriety materials with lower dielectric constants. These new lower dielectric constant materials have better electrical characteristics, but at the cost of weaker mechanical properties (as discussed in Section 1.1 as one of the driving reason for new cohesive fracture tests). But, compared to these newer dielectric materials, silicon dioxide can be easily deposited and the values for its fracture toughness are readily available in literature to allow for validation of the results of this new cohesive fracture test method. Therefore there is a need for new tests such as the one presented here, to characterize and better understand the cohesive fracture resistance of new thin film dielectric materials. The fabrication procedure is described in the following paragraphs and is illustrated in Figure 26.

The first main step of fabrication of this cohesive fracture test method is to pattern rectangular strips of the sacrificial material on a silicon substrate (Figure 26, STEP I). In this thesis ~20 nm of gold was used as the sacrificial material. Gold was chosen since it is an inert metal, can be etched with high selectively to allow full release of the test material from the substrate and test material, and does not bond to materials well, and therefore makes the release step easier. It should be noted that this poor adhesion of gold sometimes requires the use of an adhesion layer below it to prevent premature

delamination during subsequent wet processing and handling. In this study, a ~5 nm thick chromium film was used. Both of these blanket film layers (chromium and gold) were deposited on a 4" silicon wafer using a Unifilm® magnetron sputter machine.

After depositing the gold film, it is then necessary to pattern the sacrificial material into strips with photoresist and etching processes (Figure 26, STEP I). To create the rectangular gold sacrificial strips, the first photolithography mask was used to pattern Shipley Microposit® SC1827 photoresist with a thickness of ~2.7 μm (details of the SC1827 recipe are contained in Appendix A.1.1). After exposing and developing the SC1827 photoresist, the gold sacrificial layer was patterned by etching with Transene® GE-8148 gold etchant. Once the gold etching was completed, the photoresist was removed with Shipley Microposit® 1165 photoresist remover and subsequently subjected to an oxygen descum process using a Plasma-Therm® RIE machine to further clean any residual photoresist off the patterned gold rectangular strips and silicon wafer surface (details of oxygen descum process are contained in Appendix A.1.3).

Next a blanket layer of the test material of interest is deposited over the sacrificial layer. For the demonstration of this new test method, the test material chosen was silicon dioxide. The silicon dioxide layer was deposited using a Unaxis® PECVD machine (Figure 26, STEP II). The deposition was completed using precursor gases of 400 sccm of SiH_4 and 900 sccm of N_2O, at a temperature of 250^oC, a pressure of 900 mtorr, and a plasma power of 25 watts. The resulting deposition rate using these parameters was ~50 nm/min and was used to deposit the silicon dioxide film of the desired thickness for the test.

Before the silicon dioxide test material is patterned, a blanket layer of the superlayer material is deposited on top of it. During the fabrication of these test samples, chromium was chosen as the superlayer material to blanket the silicon dioxide (Figure 26, STEP II). The chromium film was deposited using a Unifilm® magnetron sputter machine which allows the argon pressure to be controlled during sputter deposition, and therefore allows control over the superlayer stress as mentioned in Section 4.2. The typical range of argon pressures used to create a superlayer with a stress of 1-2 GPa was 2-5 mtorr. To obtain an accurate measure of the stress in the superlayer film, a dummy silicon wafer was also coated with chromium prior to the deposition run of the test sample with the same deposition parameters. The stress in the chromium film on this dummy sample was then measured using a Bowoptic® Stress Measurement system and recorded for later use in the calculation of the cohesive fracture resistance of the test material. In this system, the curvature of silicon wafer after the deposition of Cr layer is used to determine the stress in Cr layer.

Next the deposited superlayer material is patterned into triangles with photoresist and etching processes (Figure 26, STEP III). This pattern is created by using the second photolithography mask and Shipley Microposit® SC1827 photoresist. After exposing and developing the SC1827 photoresist, the chromium superlayer was patterned by etching with Cyantek® CR-7 chromium etchant. Once the chromium etching was completed, the photoresist was removed with Shipley Microposit® 1165 photoresist remover and subsequently subjected to an oxygen descum process using a Plasma-Therm® RIE machine to further clean any residual photoresist.

After the superlayer material is patterned into triangles, the test material is patterned with shapes as illustrated in STEP IV of Figure 26 and additional etches are performed to expose sections of the sacrificial material below it. This patterning of the silicon dioxide was completed by utilizing the third photolithography mask and Shipley Microposit® SC1827 photoresist. The pattern of the silicon dioxide test material creates crack initiation notches, creates access to the gold sacrificial layer beneath the silicon dioxide, and creates a cut step to help initiate the action of the superlayer (Figure 27). After exposing and developing the SC1827 photoresist, the cut step was begun by etching the small exposed area of the chromium superlayer with Cyantek® CR-7 chromium etchant. Then the cut step was completed by etching the silicon dioxide patterned using buffered oxide etchant (BOE).

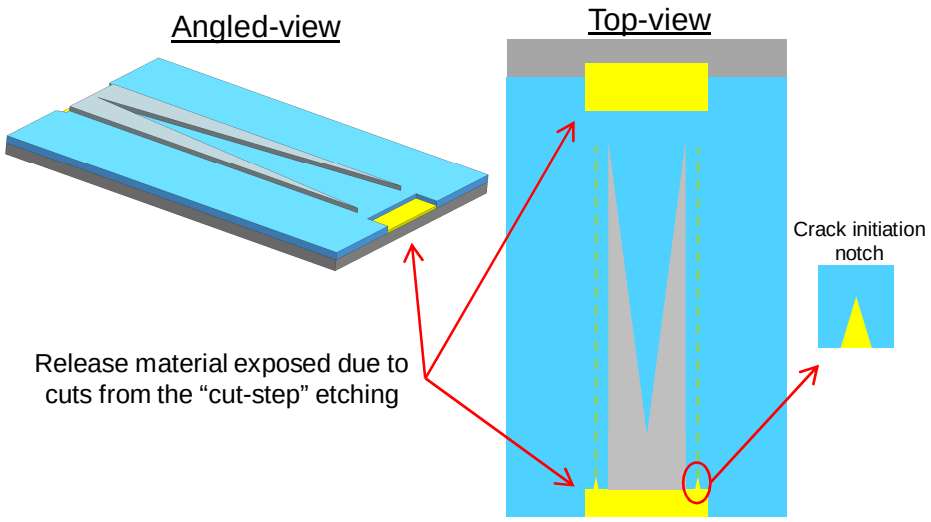


Figure 27: Detailed view of fabrication process STEP IV of Figure 26 showing the cut step to etch SiO_2 to expose the release material below it and create crack initiation notches.

With the gold sacrificial layer exposed from the patterning and etching using the third photolithography mask, the exposed gold sacrificial layer was then etched with Transene® GE-8148 gold etchant. Since this gold etchant has to laterally etch beneath the silicon dioxide test material, it requires an etch time of several hours. Once the entire

gold sacrificial layer was removed, the SC1827 photoresist was removed with Shipley Microposit® 1165 photoresist remover. With the sacrificial material and photoresist removed, the test material is no longer fully secured to the substrate or being held down and therefore the superlayer can now cause cohesive crack initiation and propagation (Figure 26, STEP V). The length of the crack is then measured and allows for the cohesive fracture strength to be determined using finite-element analysis of a model of the specific test using the same geometries, crack length, and superlayer stress.

4.6 Photolithography Mask Design and Test Sample Geometry

To fabricate the cohesive fracture test discussed in Section 4.5 it is necessary to use photolithography cleanroom processes. This photolithography fabrication process utilizes three photolithography masks. The masks used for this test were four inch square soda lime with chromium material as the pattern and were created by Photo Sciences Incorporated®. The general layout of these three masks is illustrated in Figure 28 which shows screen captures of the mechanical drawings used to fabricate each of the separate masks. Also, Figure 29 shows the patterning results produced by each of the masks, where Mask *A* patterns the release material on the silicon substrate, Mask *B* defines the geometry of the triangular superlayer, and lastly Mask *C* patterns the blanket layer of the test material into the test strip geometry and creates access to the release material below it. It should be noted that the optical images of Figure 29 shows two test strips that are created by the "cut" located at the middle of the sample. This cut creates two test strips with the individual strip's cracks propagating in opposite directions, therefore one patterned strip creates two separate test strips when the test is completed.

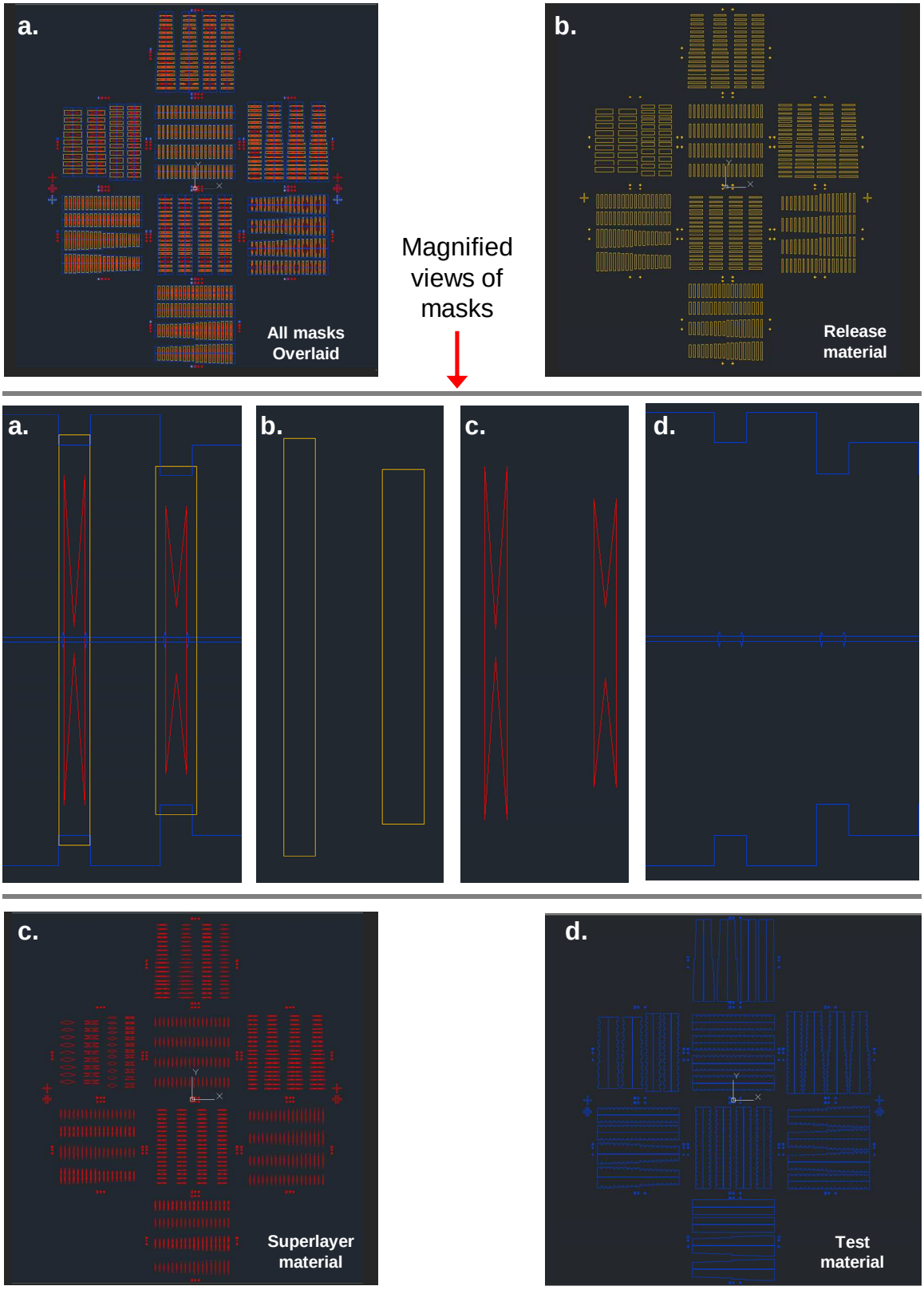


Figure 28: Mechanical drawings of each of the three individual photolithography masks (each 4x4 inch) and one image of all three masks overlaid. Additionally, a magnified view of a section of two test sample for each respective mask (magnified view is signified by matching letter labels).

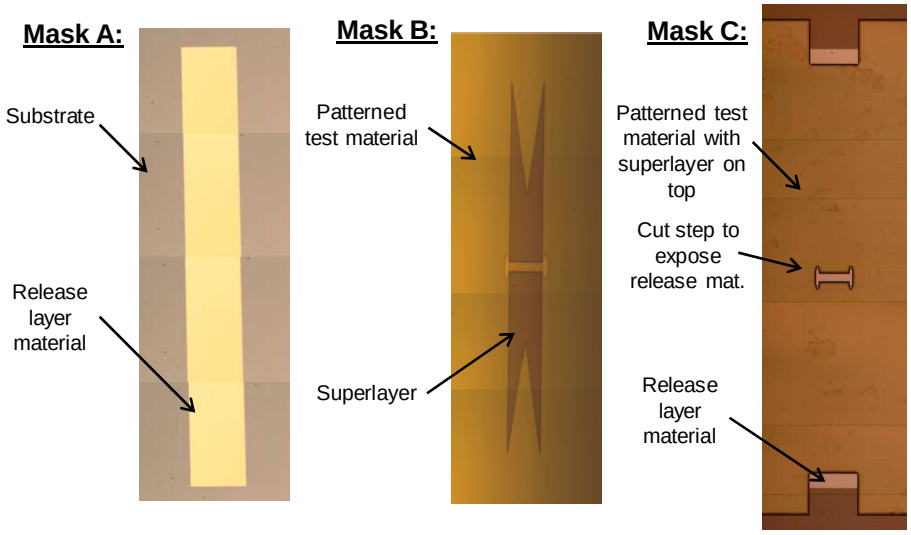


Figure 29: Optical images of the results of each mask during fabrication. Mask *A* defines the rectangular shape of the release material, Mask *B* defines the superlayer triangles, and Mask *C* patterns the test material blanket layers into the shape of the test specimen and creates windows to give access to the release material below it. The image for Mask *C* still possesses the photoresist mask, therefore obscuring the patterned superlayer below it.

The entire mask contains many different overall cohesive test strip designs with different dimensions and geometries. In general, the mask contains test strips where the widths of the release material strips range from ~300-540 µm (which defines the width of the free-hanging section of the test material), the total length of the superlayer range from 1100-1800 µm, the length of the triangular section of the superlayer range from 700-1500, and the width of the superlayer is 200 µm. The general dimensions of this cohesive fracture test are based off of those used in Zheng's [97] interfacial fracture toughness test, but dimensions and geometries were varied here to investigate and eliminate any potential effects on the cohesive fracture results. Figure 30 and Table 4 illustrates the ranges of the important dimensions tested in the mask design.

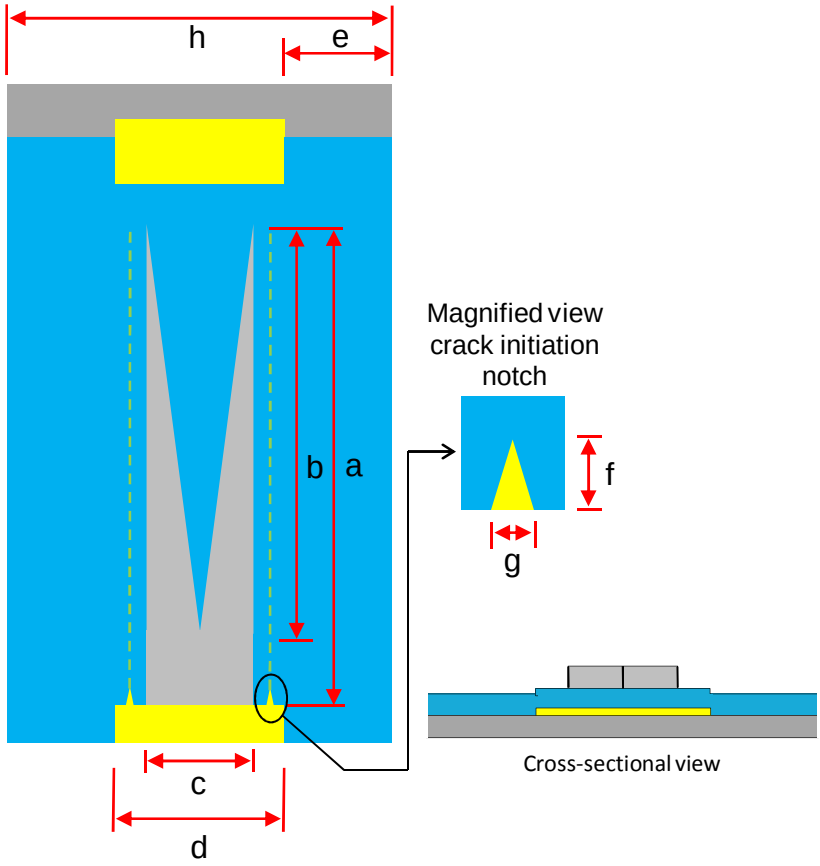


Figure 30: Illustration of the top-down view of a single test specimen showing the key dimensions of the superlayer triangle, test material, release material, and crack initiation notch. Also for clarity, a cross-sectional view is given.

Table 4: List of ranges for the values of the dimensions in Figure 30 that were included in the photolithography mask design.

Label	Dimension Name	Range of Values (μm)	Label	Dimension Name	Range of Values (μm)
a	Total superlayer length	1100, 1200, 1300, 1600, 1700, 1800	e	Test material width attached to Si substrate	230, 280, 300, 350
b	Superlayer triangle section length	700, 800, 900, 1000, 1500	f	Crack initiation notch height	25, 50, 80
c	Superlayer width	200 (600, 800 for large samples)	g	Crack initiation notch width	20
d	Release material width	300, 400, 440, 540 (980 and 1140 for large samples)	h	Test strip width	1000 (1200, 1400, 1720, 1740 for larger samples)

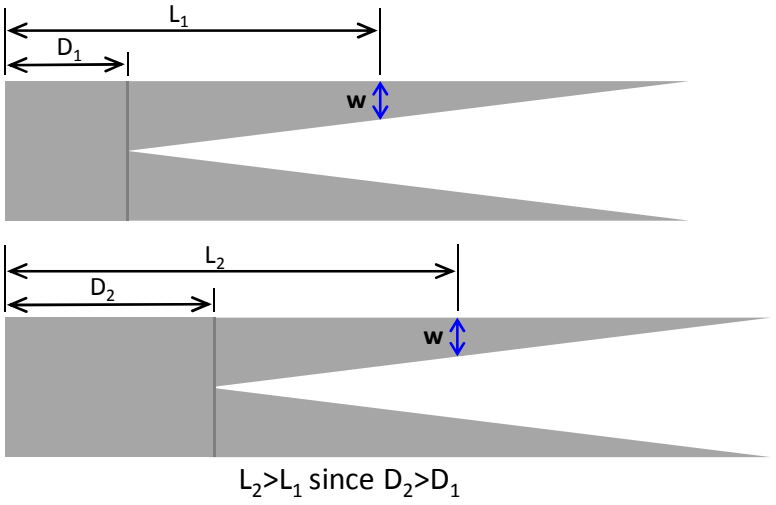


Figure 31: Illustration of the composition of the total length of the triangular superlayer to investigate effect of amount of curling.

One of the major geometry variables tested in this mask design concerns the combination of the total superlayer length (*a* in Figure 30) and the superlayer triangle section length (*b* in Figure 30). Different combinations of these two dimensions allows for the investigation of the effect of the crack length and the amount of curling on the fracture measurements. This is because the total superlayer length is composed of the superlayer triangle length and a rectangular section of constant width at the base of the superlayer strip (as illustrated in Figure 31). This rectangular section adds length to the propagating crack and therefore requires the strip to curl more compared to a superlayer with a shorter rectangular section. For example, in Figure 31, superlayers 1 and 2 have the same total length, but superlayer 1 has a longer superlayer triangle and a short rectangular section compared to superlayer 2 (i.e. $D_2 > D_1$). When a cohesive crack propagates, it ceases at some length where the width of the superlayer, *w*, at the location of the crack tip relates to the cohesive fracture resistance of the test material. But in the case of the two test strips here, since $D_2 > D_1$, in order to reach the same *w* the crack

length and amount of curling of sample 2 must be greater than sample 1 (i.e.$L_2 > L_1$). It is in this manner that the mask design takes crack length and curling into account by having different superlayer triangle lengths.

Another important geometry that was tested in the photolithography mask design was the shape of the superlayer triangle. Two general triangles were included in the mask design, a single triangle and a double forked triangle as illustrated in Figure 32. During fabrication, it was found that the double forked triangles were more successful than the single triangles. It is thought that the double triangle design provides a more constant direction of the crack tip as it propagates and therefore it cracks in a straight line. With the double triangle, the distance between the edge of the superlayer film and the crack is a constant distance. The single triangle design does not provide this, and therefore cracking commonly occurs along the edge of the superlayer. Examples of unsuccessful strips of a single triangle design are shown in Figure 32.

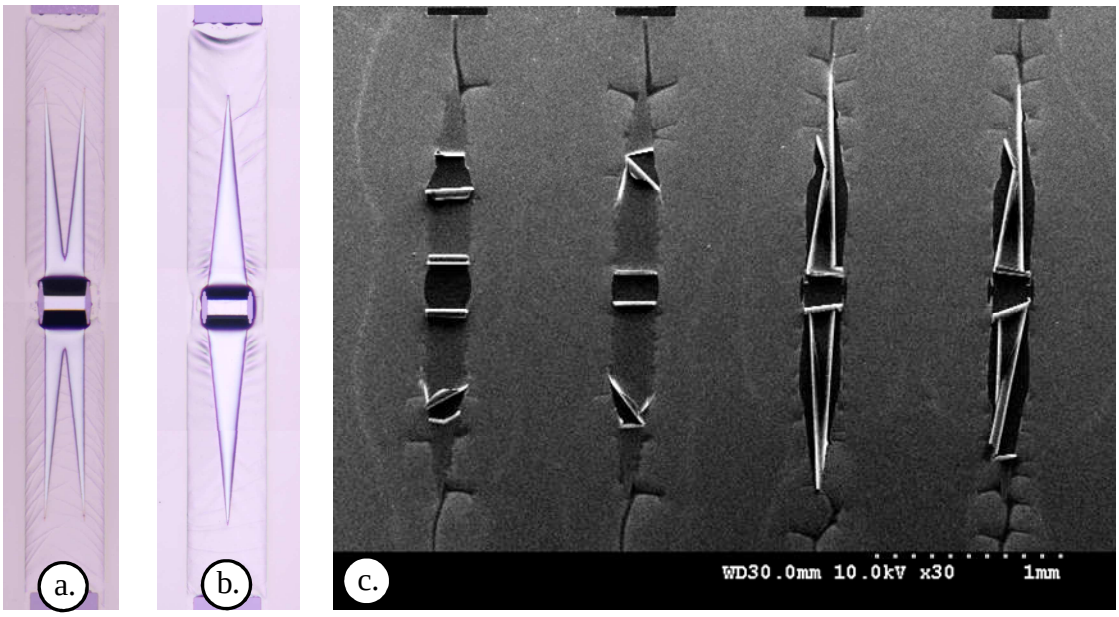


Figure 32: Top-down optical images of test strips with different superlayer shapes. Image a. shows a double forked triangular superlayer and b. shows a single triangle superlayer. Image c. shows a top-down SEM view of several improperly failed samples with single triangle superlayers.

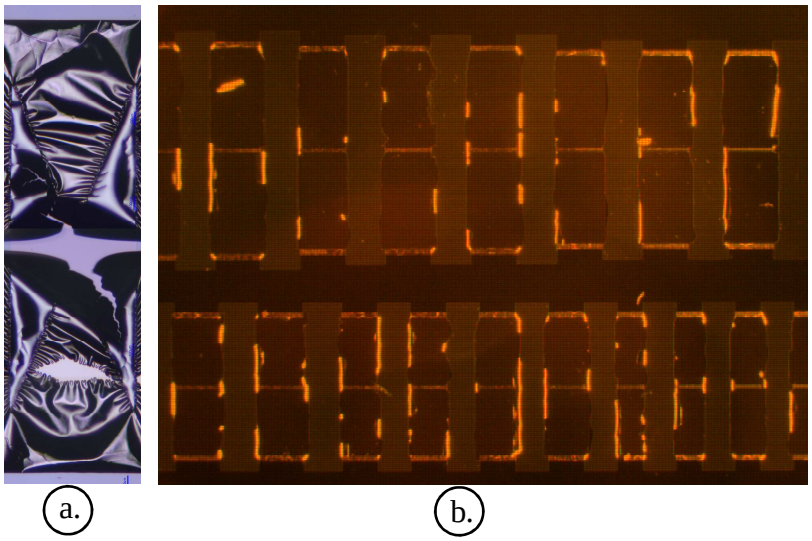


Figure 33: a.) Shows optical image of top-down view of a single improperly failed large planar area superlayer test strip with a superlayer width of 800 µm. Image b.) shows one row of large planar area test strips with superlayer widths of 600 µm and another row with superlayers with widths of 800 µm. All of the strips in these rows prematurely failed during fabrication.

In addition to the general superlayer shape, wide planar geometries of the triangular superlayers were investigated in the photolithography mask design. Large superlayer widths of 600 µm and 800 µm with total superlayer lengths of 1100 µm and 1800 µm were included in the design. When fabricated, these test samples did not survive till completion of the process. It is thought that this occurred because such large superlayer widths provide too much energy for fracture, causing the test strips to destroy themselves. The large width of the superlayer also causes the width of the free-hanging section of the test material to also be very wide and at these sub-micron film thicknesses the free-hanging film is extremely fragile. These fragile thin films and large widths are very susceptible to premature cracking and tearing during wet processing (as shown in Figure 33). Also, when the width of the superlayer is approximately equal to its length, plate bending occurs instead of cylindrical bending [98]. It is desired to create a situation of cylindrical bending to allow for curling of the test strips as they cohesively crack.

Therefore the best results were obtained with test strips with smaller planar geometries of widths of 300-400 µm for the given superlayer lengths.

The last feature geometry that was included in the photolithography mask was the crack initiation notch size. These notches on the test strips had a base width of 20 µm and had lengths of 25, 50, and 80 µm. The notches were varied in size and sharpness due to the uncertainty of the development of the photoresist for such sharp triangle tips since the limit of standard photolithography is ~ 3um. From the fabrication of the test strips with all the notch sizes, it was observed that they all were fabricated successfully and performed properly despite the chosen dimensions.

4.7 Cohesive Test Fabrication Results

To demonstrate the cohesive fracture test described in this chapter, five different test wafers were fabricated and the resulting crack lengths measured. Since this test was initially developed to measure the fracture toughness of increasingly fragile new low-k dielectric films that are being used in Back End Of Line microelectronic packaging, it was decided to use silicon dioxide as the test material. This is because, silicon dioxide is a traditional dielectric material that has been mechanically characterized in literature, and therefore allows for this new test method to be investigated while offering a comparison to existing measurement values. Additionally, to better demonstrate this new test method each of the test wafers fabricated possessed different values for the test material thickness, superlayer thickness, and superlayer stress. These different film thicknesses and superlayer stress values were used to show that this new test method yields fracture resistance values of silicon dioxide that are within the range of those reported in literature. The specific thicknesses and superlayer stress for each of these five samples

are listed in Table 5. All of the films contained in this group of tests are in the range of a few hundred nanometers thick, with the thickness of the superlayer ranging from 43-203 nm measured by either a Dektak® or Tencor® KLA profilometer and the thickness of the silicon dioxide ranging from 110–408 nm measured with a Nanospec® Reflectometer.

Table 5: List of material thicknesses and superlayer stresses for the five different experimental test samples fabricated.

Sample	Test Material Thick. (nm)	Superlayer Thick. (nm)	Superlayer Stress (MPa)
#1	193	43	1944
#2	193	105	1640
#3	110	130	1296
#4	315	120	1205
#5	408	203	1100

After each of the samples listed in Table 5 were fabricated and allowed to crack, all of the crack lengths for each test sample contained on the wafer were measured using a Hitachi® S-4700 FE-SEM, Zeiss® Ultra60 FE-SEM, or a Keyence® VHX-600 digital microscope. The fundamental dimension of interest that relates to the critical energy release rate is the width of the triangular superlayer at the crack tip. But, for experimental purposes, the crack length of each cracked test strip was measured, and then using simple geometry, the width of the superlayer at the crack tip was calculated. Examples of these cracked samples are shown in Figure 34 to Figure 39 and additional images are shown in Appendix A.2.

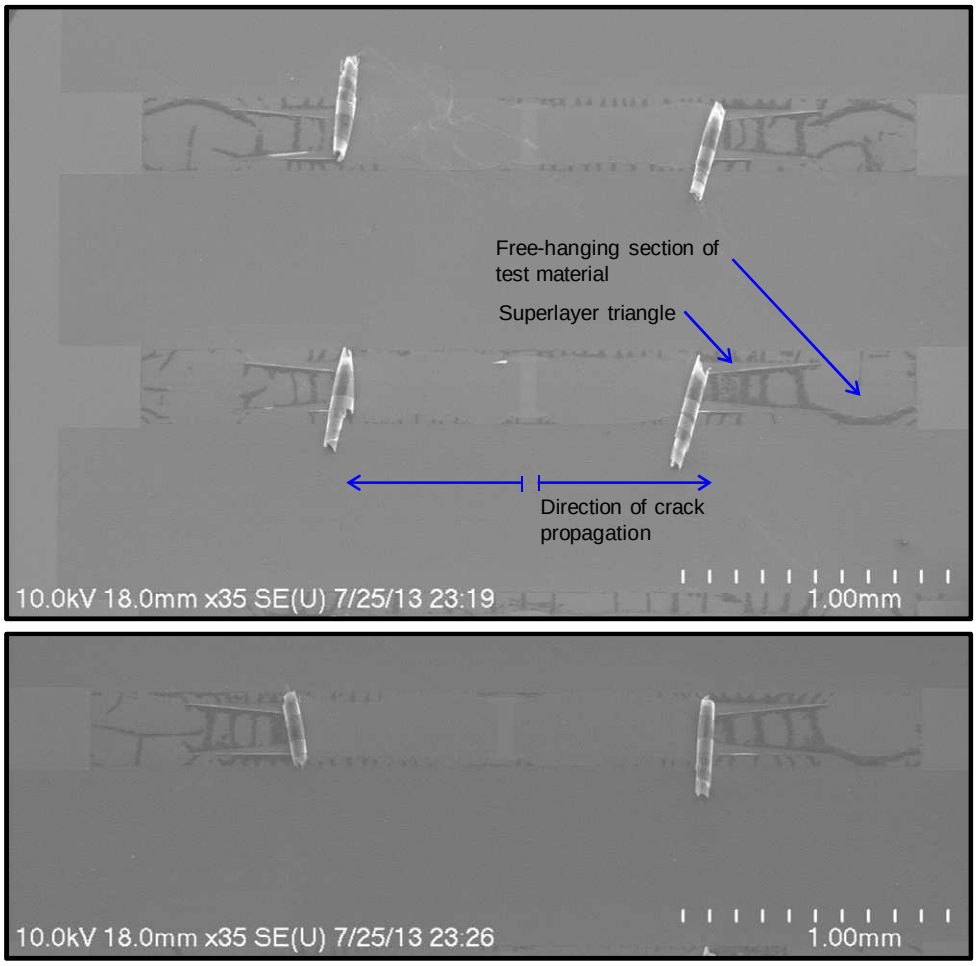


Figure 34: SEM images of top down view of finished test strips of Sample #1. Image shows three separate test strips, giving a total of six test samples, where each strip consists of two test samples with cracks propagating in opposite directions.

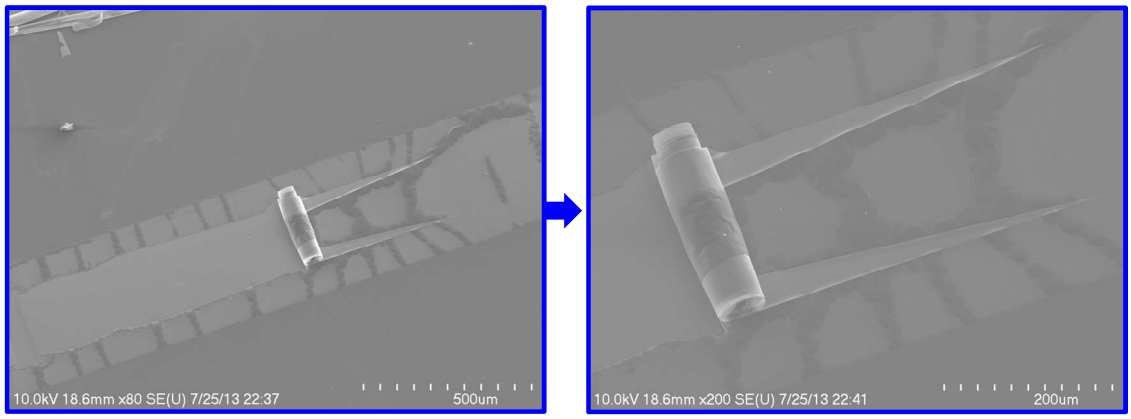


Figure 35: SEM images of various magnifications of a single test sample of Sample #1. Left image shows entire crack length of the test sample and left image shows the un-cracked portion including the curled superlayer and test material.

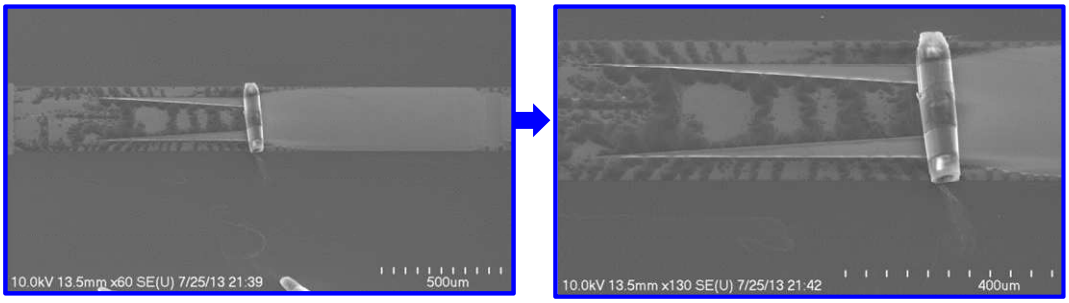


Figure 36: SEM images of various magnifications of a single test sample of Sample #1. Left image shows entire crack length of the test sample and left image shows the un-cracked portion including the curled superlayer and test material.

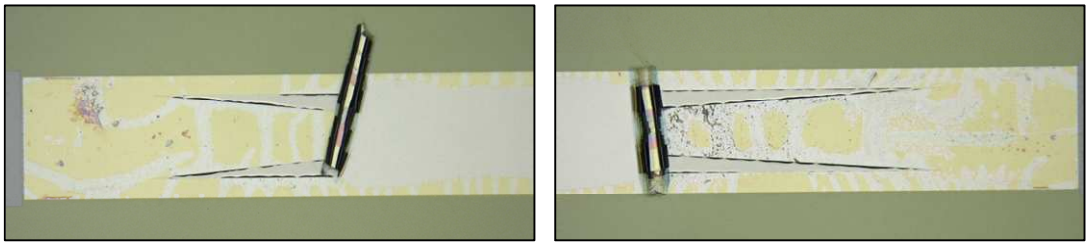


Figure 37: Optical images of two different test samples of Sample #1. The bare Si substrate is seen where the free-hanging test material has cracked and curled.

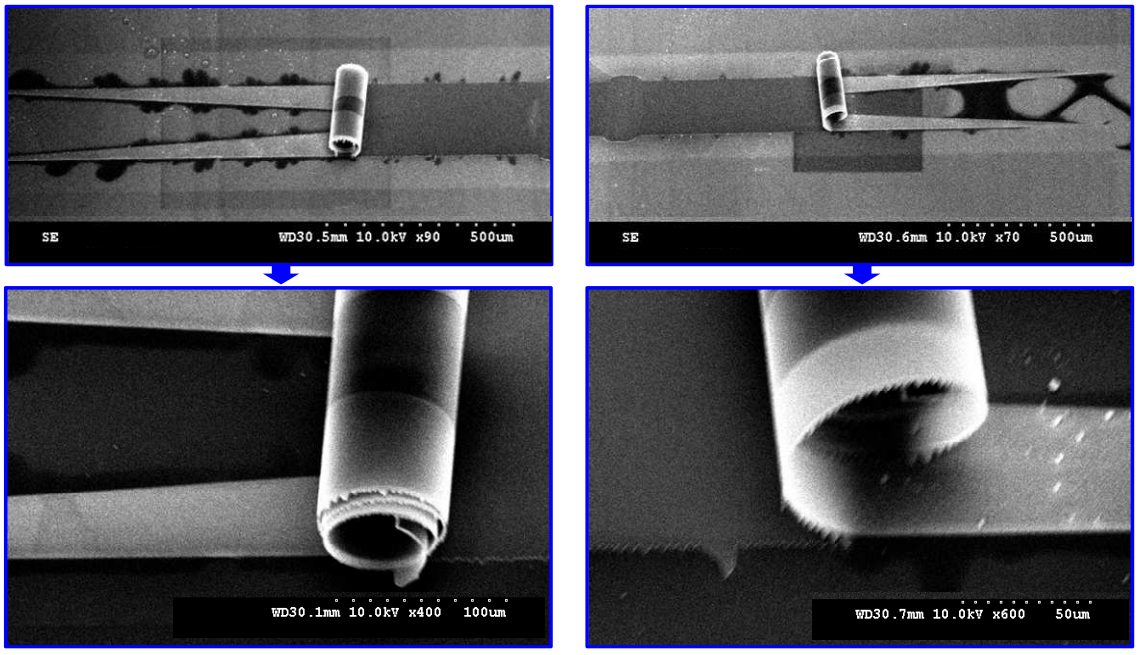


Figure 38: SEM Images of two different test samples of Sample #4. Top two images show the entire lengths of the test samples with the cracked and un-cracked portions. Bottom images show increased magnification views of the respective test samples of the curled test material.

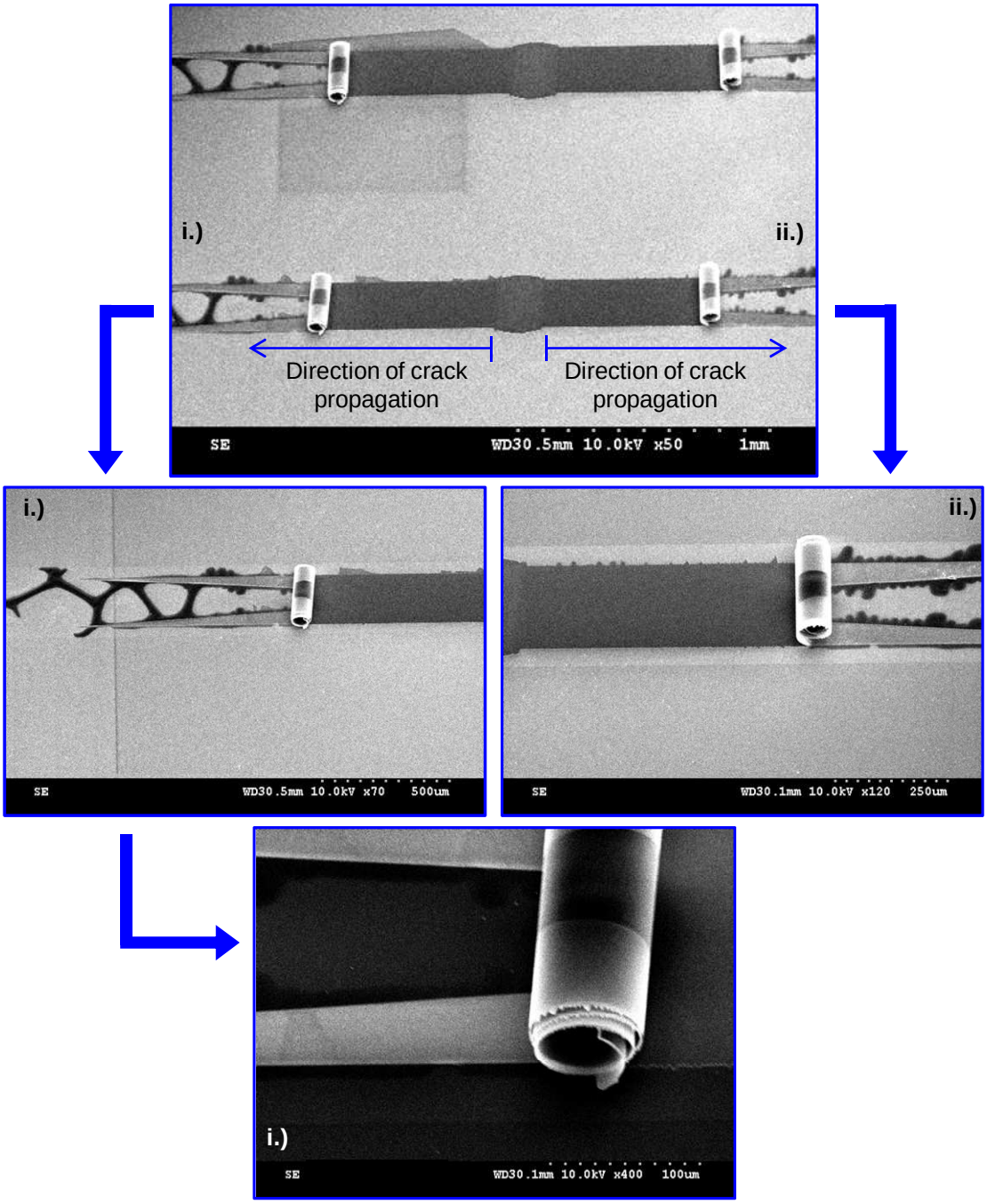


Figure 39: SEM images of top down view of finished test strips of Sample #4. Top image shows two separate test strips, giving a total of four test samples, where each strip consists of two test samples with cracks propagating in opposite directions. Images of increased magnifications of the test samples labeled i.) and ii.) in the top image are show in three bottom images.

In all of these figures of the cracked test samples, the general concept of this test method is demonstrated. It is observed from these images that:

- The cracks initiated at the end of the test sample where the triangular superlayer is widest and propagated in the direction of decreasing superlayer width.
- Cohesive cracks propagated on both sides of the forked triangular superlayer, parallel to each other, and through the thickness of only the free-hanging section of the silicon dioxide test material.
- The test material and the superlayer neatly curled together on themselves as the crack propagated through the test material.
- The cohesive crack in the test material ceased at some distance at a location with some specific width of the superlayer triangle associated with it.

In addition to demonstrating these basic test method concepts, these pictures allowed the crack length for each of the individual test samples on each wafer to be measured. Also, using these crack lengths and the geometric concept of similar triangles, the width of the superlayer at the crack tip was calculated for each individual test sample. The average measurements from all of the individual test samples on the five different wafers along with the range of values are listed in Table 6. This table lists average widths of the superlayer triangle at the crack tip and the average crack lengths from all of the experimental results for each wafer along with the deviations of these values to provide information on the test result's error/uncertainty (~20 individual test samples from each wafer). It should be noted that the crack lengths listed in Table 6 are equivalent crack

lengths based on a double forked triangular superlayer with triangle length of 1000 µm and width of 100 µm for the width of the base of a single triangle of the double forked superlayer geometry. This equivalent crack length is listed in the table since many different superlayer dimensions/shapes were utilized in the test to create different crack lengths to reach the same superlayer width at the crack tip to investigate the effect of the amount of material curling (concept demonstrated in Figure 31). As mentioned earlier, the crack lengths and superlayer widths at the crack tip listed in Table 6 are related to each other through similar triangles. These experimental measurements will next be used in finite-element analysis of each specific experimental scenario to calculate the fracture resistance of the silicon dioxide test material.

Table 6: List of measured crack lengths (equivalent crack length based on a superlayer double forked triangle with triangle length of 1000 µm and width of 100 µm for the width of the base of a single triangle of the forked double superlayer geometry) and widths of the superlayer at the crack tip for the five different test samples fabricated. Also the deviation of the superlayer width and crack length are listed.

Sample	Test Mat./Superlayer Thick. (nm)	Superlayer Stress (MPa)	Crack Length (µm)	Superlayer width at crack tip (µm) (calculated from crack length using similar triangles)
#1	193/43	1944	548.5 (±60.2)	45.15 (±6.02)
#2	193/105	1640	605.0 (±40.6)	39.53 (±4.06)
#3	110/130	1296	741.1 (±44.4)	25.89 (±4.44)
#4	315/120	1205	405.3 (±79.4)	59.47 (±7.94)
#5	408/203	1100	535.0 (±141.9)	46.50 (±14.19)

4.8 Finite-Element Analysis of Experimental Results to Calculate Fracture Resistance

To measure the cohesive fracture resistance of the desired test material, it is necessary to perform the two main steps illustrated earlier in Figure 23, where the first step is the fabrication of the test samples and then the second is the measurement of the resulting crack lengths and the use of finite-element analysis to calculate the cohesive fracture resistance. In the previous section of this chapter (Section 4.7), the average widths of the superlayer at the crack tip for the five different sets of samples were measured and reported. In order to calculate the cohesive fracture resistance of the silicon dioxide test material it is necessary to perform a finite-element analysis of these specific experimental test specimens. Therefore five different finite-element models were created with the measured values of test material thickness, superlayer thickness, and superlayer stress listed in Table 5 of the experimental test samples. For each of these models the respective experimentally measured crack length (and therefore, the corresponding superlayer width at the crack tip of Table 6) was used in the models. Additionally, the Young's modulus values for the silicon dioxide test material and the chromium superlayer were measured using nanoindentation to create a more accurate finite-element analysis. These films were prepared on silicon wafers with the same deposition process as the films used in the cohesive fracture test to provide representative films. The details of these nanoindentation measurements for the Young's modulus values are presented in Appendix A.3. The Young's modulus value used for the silicon dioxide (E_{SiO2}) was 86.2 GPa and the Young's modulus value for the chromium (E_{Cr}) was 149.54 GPa. Using these geometric parameters, experimental crack lengths, and material

properties of the test samples then allowed the energy release rate of the crack to be calculated using both the virtual crack closure technique (VCCT) and the J-integral method in the finite-element models. The energy release rate calculated using these two methods range from 0.3%-0.9% from each other and therefore this similarity of two different approaches provides validity to the calculations. Since these two calculations are in agreement, only the energy release rate calculated by VCCT is presented in Table 7. The energy release rate reported here is the total energy release rate (G_{total}), which includes all the components G_I, G_{II}, and G_{III}, and is calculated for the node located at the middle of the line defining the crack tip through the thickness of the test material. In addition to reporting the values of G_{total}, this value has been converted to the critical stress intensity factor K_{IC}, where $G = K_{IC}^{\ 2} / E$, since the silicon dioxide test material is brittle and exhibits linear elastic fracture mechanics. The specifics of these methods and finite-element model are fully discussed in Chapter 5, and should be used as a reference for this current discussion.

Table 7: List of calculated fracture parameters using the measured experimental crack lengths and FEA. Also the deviation of these values resulting from the range of experimentally measured lengths has been included.

Sample	Critical Total Energy Release Rate (J/m^2)	Total Stress Intensity Factor (MPa$\sqrt{m}$)
#1	9.82 (±3.58)	0.908 (±0.151)
#2	13.99 (±3.23)	1.09 (±0.126)
#3	8.89 (±2.74)	0.865 (±0.139)
#4	13.20 (±3.21)	1.06 (±0.116)
#5	10.64 (±5.53)	0.919 (±0.277)

In addition to solving the finite-element models of the five different experimental test samples with their respective measured crack lengths, each model was solved for several other possible crack lengths. In these simulations, the crack was grown along the entire length of the test strip to provide the relationship between crack length and energy release rate. The relationship for each sample is presented in the plots of Figure 40 and Figure 41. Also, polynomials have been fit to these plots to allow calculation of the energy release rate for any crack for these samples and are listed on the plots.

The values for the critical total energy release rate and the critical stress intensity factor calculated for the five different experimental test samples are listed in Table 7. The values for the average critical total energy release rate ranged from 8.89-13.99 J/m^2 with an average value for the five test samples being 11.3 J/m^2. Additionally, the values for the critical stress intensity factor ranged from 0.865-1.09 MPa$\sqrt{m}$ with an average value for the five test samples being 0.968 MPa$\sqrt{m}$. These critical stress intensity factors obtained are very near/within the range of 0.77-1.0 MPa$\sqrt{m}$ [29, 99-101] of reported values for thin silicon dioxide films in literature. Additionally, these critical stress intensity factors from literature can be converted to the critical energy release rate using the measured Young's modulus of 86.2 GPa for silicon dioxide to yield a range of 6.88-11.6 J/m^2. The measured values for the critical total energy release rate are also very near/within this reported range. These measured values for the fracture resistance of silicon dioxide demonstrate the ability of this new test method, which uses a stressed film superlayer and photolithography fabrication processes, to accurately measure the fracture resistance of thin films. Also, Table 7 lists the deviation of the average critical energy release rate values for each sample number to show that there is some error/uncertainty

associated with the test results. This error/uncertainty arises from the range of crack lengths and corresponding width of the superlayer at the crack tip measured for each sample number listed in Table 6. Even with this error/uncertainty, the majority of the ranges of the fracture parameters in Table 7 still fall within the range of silicon dioxide fracture parameters found in literature.

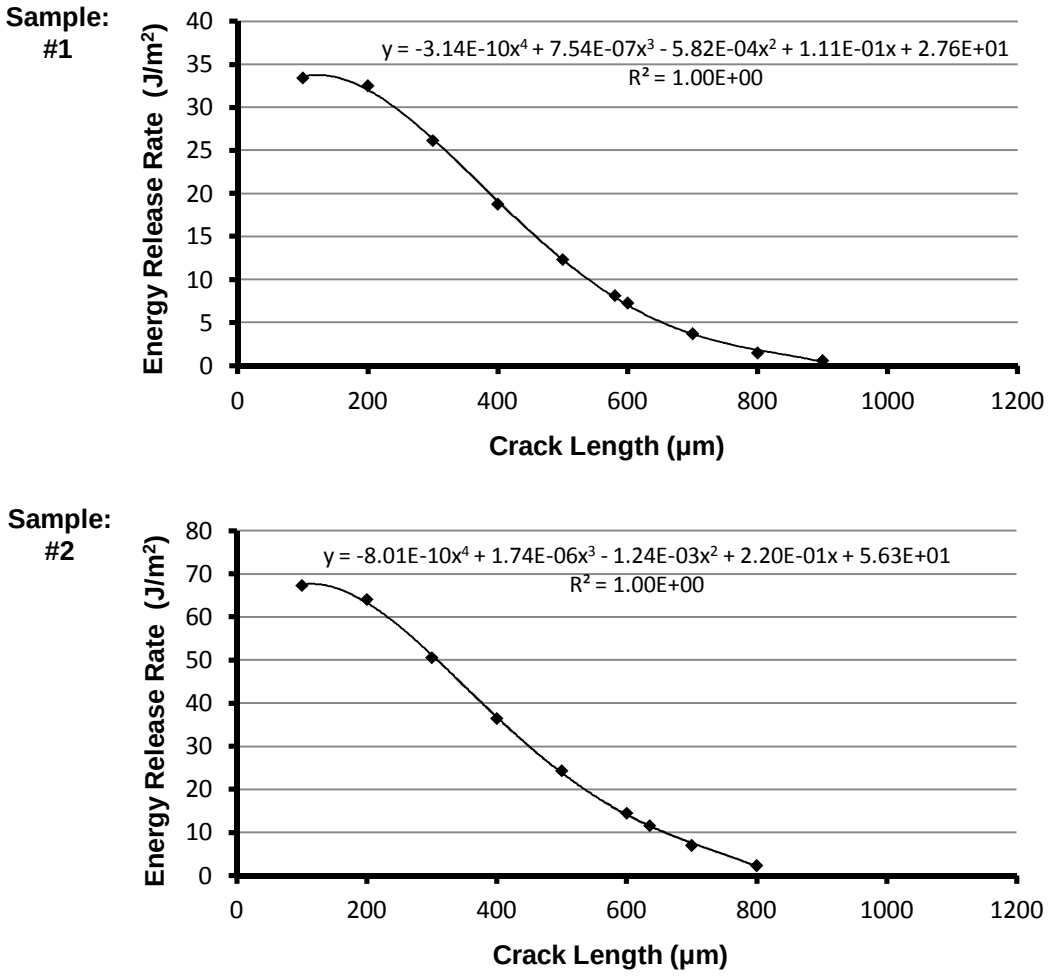


Figure 40: Graphs of the crack length vs. energy release rate calculated using FEA for Samples #1, and #2 that were fabricated. Additionally each graph includes a polynomial fitted to the FEA results to calculate the energy release rate for any potential crack length.

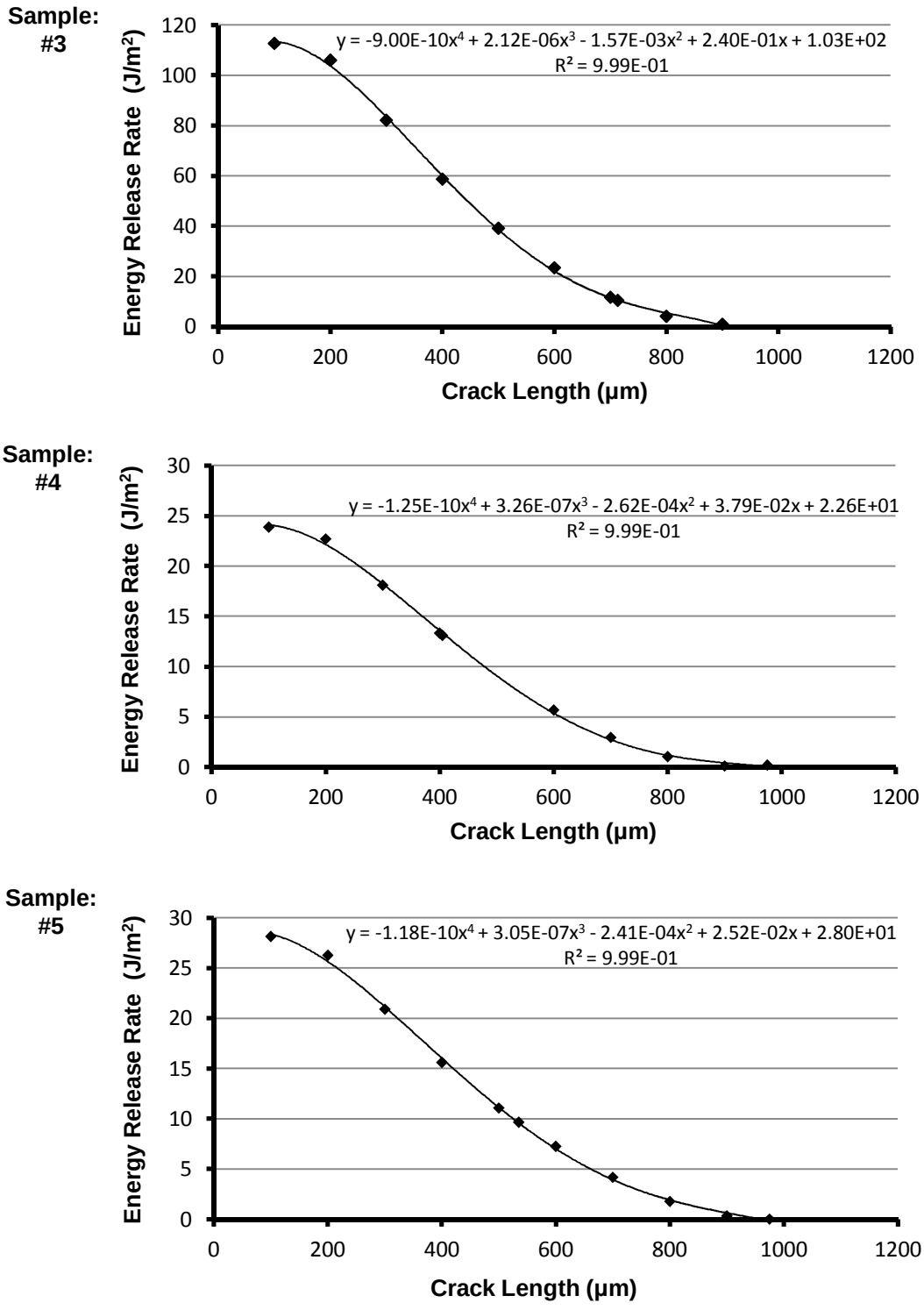


Figure 41: Graphs of the crack length vs. energy release rate calculated using FEA for Samples #3, #4 and #5 that were fabricated. Additionally each graph includes a polynomial fitted to the FEA results to calculate the energy release rate for any potential crack length.

4.9 Conclusion

In this chapter a new method to measure the cohesive fracture resistance of thin films was discussed and demonstrated. The test method possesses advantages and improves upon existing test methods by utilizing a highly-stressed superlayer film to initiate and drive fracture in the test material. This allows the test method to not require external mechanisms to attach to the test sample and fracture it, and by using photolithography and clean room fabrication processes, the need to hold and fixture the film is eliminated. These are desirable characteristics for test methods aimed toward fragile thin films such as new dielectric materials being pursued for electronic packaging. Since this test method utilizes clean room processes to achieve some of these characteristics, the three mask photolithography process to fabricate the test samples was presented and discussed in detail. This includes the mask pattern geometries, material deposition processes, and material patterning/etching processes.

To demonstrate the cohesive fracture test method, silicon dioxide was chosen as the test material with chromium as the stressed superlayer material. Five different test wafers were fabricated using these materials, and with each wafer consisting of different test sample parameters such as test material thickness, superlayer thickness, and superlayer stress. All five wafers/samples produced many successful test samples showing cohesive cracking, material curling, and eventual crack halting at a specific superlayer triangle width. The finite-element analysis of each of these five different test sample scenarios with different measured crack lengths (widths of superlayer at the crack tip) yielded an energy release rate of 8.89-13.99 J/m^2 with an average value for the five test samples being 11.3 J/m^2 and a critical stress intensity factor of 0.865-1.09 $MPa\sqrt{m}$

with an average value for the five test samples being 0.968 MPa√m. All of these values are very close/within reported literature values for thin film silicon dioxide of 6.88-11.6 J/m^2 for the energy release rate, and 0.77-1.0 MPa√m for the stress intensity factor [29, 99-101]. These experimental results demonstrate the validity of this new test method since five different test wafers were fabricated with different test material thickness, superlayer thickness, and superlayer stress and all five wafers produced cohesive fracture values for silicon dioxide within the expected range. Therefore, this new test can successfully measure the cohesive fracture resistance of new fragile low-κ dielectric films used in electronic packaging and aid in designing future electronic packages to prevent cohesive fracture of these fragile films and increase reliability.

CHAPTER 5

FINITE-ELEMENT MODELING OF SUPERLAYER BASED COHESIVE FRACTURE TEST TECHNIQUE

5.1 Introduction

In this chapter, extraction of the critical energy release rate from the cohesive fracture test using finite-element modeling is presented and discussed. As discussed in the previous chapter, at the completion of the release step of the fabrication process, the test material cohesively cracks due to the high stress level possessed by the superlayer material. Subsequently, the length of the cohesive crack, or the width of the triangular superlayer at the crack tip, is measured. It is then necessary to correlate this experimentally measured length to a value of the cohesive fracture resistance of the film. Therefore, this chapter focuses on the second component of the cohesive fracture test illustrated in Figure 42, which includes developing and understanding the finite-element model to calculate the cohesive fracture resistance of the thin film from the experimental results.

The beginning sections of this chapter focus on the creation of the finite-element model, specifically the geometry and dimensions necessary to represent the scenarios of the different experimental results and for different possible test configurations to be investigated. These sections also discuss the modeling techniques utilized to simulate the overall deformation and behavior of the model, such as the geometric symmetry that is present, the necessary boundary conditions, and the utilization of a global-local modeling approach to accurately capture the mechanics in the crack tip region. Furthermore, a crucial aspect of this new cohesive fracture test is the use of the superlayer film

possessing a high level of intrinsic stress. Therefore the method to create this initial stress state in the superlayer film will be presented and validated. The final topic detailing the creation of the finite-element model includes the calculation of the fracture resistance of the test material. Therefore the fracture mechanics concepts of the virtual crack closure technique (VCCT) and the J-integral that were chosen for this investigation will be explained in general and with respect to the current finite-element analysis.

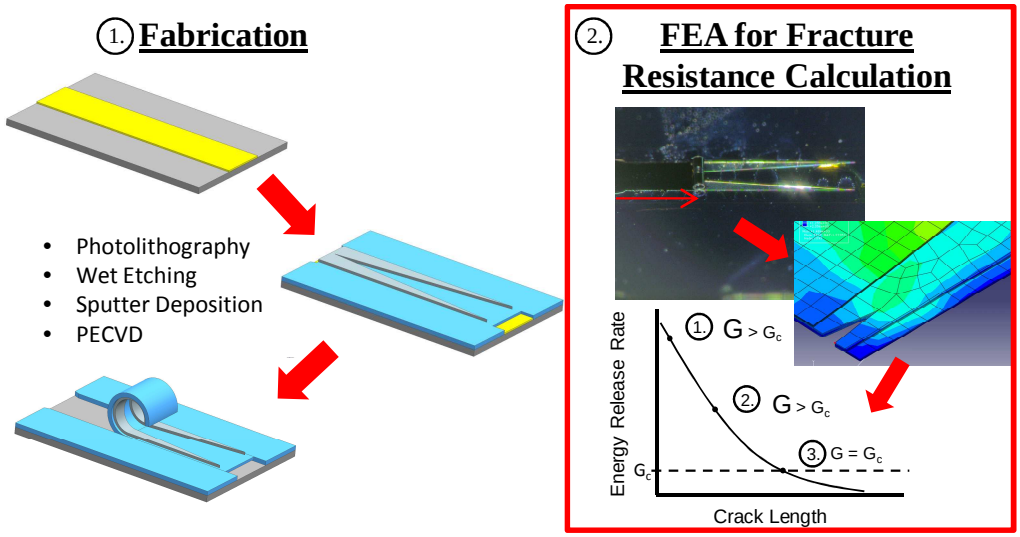


Figure 42: Schematic illustrating the two main components of the cohesive fracture test technique. Step 1 is the fabrication of test samples and Step 2 includes the use of FEA to calculate the fracture resistance from the experimental crack lengths.

After the discussion of the approach to create the finite-element model in the first section, the subsequent sections will use the model to investigate the effects of key parameters on the fracture calculations. This will include studies on the effect of the test material thickness, superlayer thickness, superlayer stress, test material modulus, and the width of the free-hanging section of the test material. The effect that these parameters have on the calculated energy release rate will be determined through independent investigations of each of these parameters. The investigation of these parameters is intended to provide a better understanding of the mechanics behind this test method to

allow for its future application to measure the cohesive fracture resistance of other materials.

5.2 Development of Finite-Element Model of Cohesive Fracture Test Technique

The following subsections of this chapter focus on the discussion of the approaches used to create the finite-element model of the cohesive fracture test technique. This includes the methods to parameterize the geometry of the cohesive fracture test samples, geometric symmetry, boundary conditions employed, and the use of global-local modeling. Additionally, the techniques used to simulate the intrinsic stress of the superlayer and the fundamental fracture mechanics to calculate the fracture resistance within the finite-element software will be explained.

5.2.1 General Finite-Element Model Information

The finite-element model of the cohesive fracture test was created using ANSYS® software. When first creating a finite-element model of a specific component, object, or device it is necessary to determine how to best simplify the model to minimize computation time and the output file size while retaining the accuracy of the model. The geometry of the cohesive fracture test and the nature of its out-of-plane deformation makes the modeling challenging (Figure 43). Thus it is necessary to model the cohesive fracture test as a 3D model due to the nature of the test's geometry and the deformation. The triangular shape of the superlayer in the *X*-*Y* plane and the location of the crack tip of the model, does not allow for the model to be represented in a simplified 2D model of the geometry contained within the *X*-*Z* plane (as shown in Figure 43). Modeling only the geometry in the *X*-*Z* plane would not capture the changing width of the triangular superlayer as the crack grows, which is a key concept of this test technique. Also, a 2D

model of the *X*-*Y* plane cannot be used since the deformation caused by the stressed superlayer is in the *Z*-direction, which is out of the plane of the test strip. Specifically, the 3D elements used in this work were SOLID185, which are 8-node structural elements.

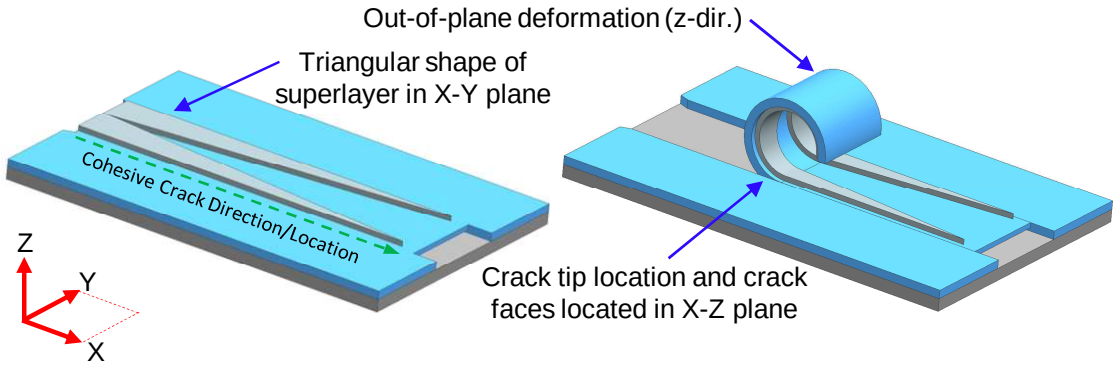


Figure 43: Illustrations of full geometry of cohesive fracture specimens with respect to the coordinate system used in discussion. Left image is un-deformed before cracking, right image shows out-of-plane deformation after cracking.

Since a 3D model with 3D elements is being used, the total number of elements is very large due to the dimensions of the cohesive fracture test samples. This is because the planar dimensions of the test strip geometry is approximately 1000 μm long and 300 μm wide, while the thicknesses of the test material (e.g. SiO_2) and the superlayer (e.g. Cr) are only a few hundred nanometers. To mesh this geometry with such a difference between the material thickness and planar dimensions with 3D elements, while maintaining a proper length-to-width aspect ratio of the elements, the element size must be in the tens of nanometers scale resulting in extremely high number of elements and thus prohibitive computational time and resources.

5.2.2 Global-Local Modeling Technique

In order to create a model with the desired mesh for this relatively large and challenging model, a global-local analysis was utilized. This type of analysis is possible

here since all the desired final analyses are concerned with what occurs at the crack tip, and not the rest of the geometry. In a global-local analysis, two sequential analyses are performed as illustrated in Figure 44. First the entire model is meshed with a large element size and solved. Then a second model of just the geometry in the vicinity of the location of interest is created and meshed with a smaller element size. Next, the displacements of the nodes of the global model are retrieved from the global solution, and the displacement values for the nodes on the "cut" boundaries of the new local model, that were obtained from the global model, are applied to the corresponding nodes of the local model. The local model is then solved, and final fracture analysis calculations are conducted with the results of the local model. With this type of global-local approach, it is possible to decrease the amount of elements needed while maintaining accuracy, by using one analysis of the entire global model with a larger element size, followed by a second analysis of only the local geometry of interest with a smaller element size. In the global-local analysis of the cohesive fracture test, the global model utilized 2 elements through the thickness of the test material (i.e. SiO_2) and 5 elements through the thickness of the superlayer (i.e. Cr), which resulted in a total of ~2.6 million elements. Similarly, the local model used 10 elements through the thickness of the test material and 5 elements through the thickness of the superlayer and resulted in ~1.6 million elements.

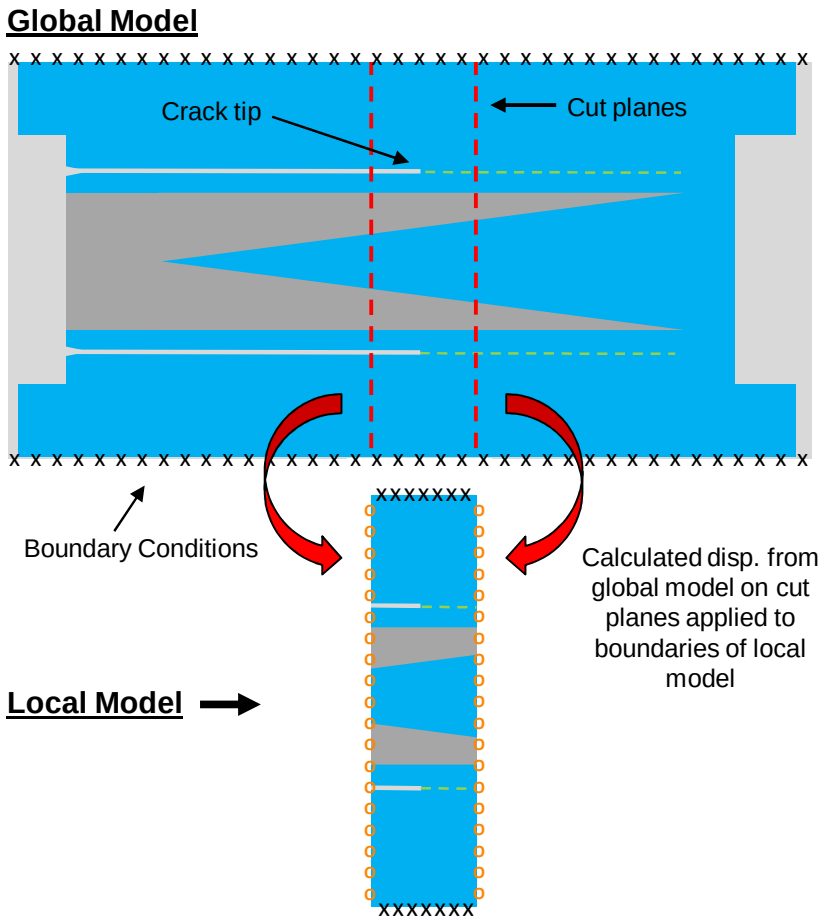


Figure 44: Top-down view of the global-local modeling approach applied to full geometry (no symmetry used) of the cohesive test. Two separate simulations are solved. First the global model is solved, and the displacements of the nodes located on the cut planes are applied to the labeled boundaries of the local model, of just a portion of the global model. This local model is then solved separately.

5.2.3 Finite-Element Model - Boundary Conditions

In addition to utilizing a global-local approach in the analysis of the cohesive fracture test, geometric symmetry was also employed. By examining Figure 45 it is apparent that the cohesive fracture test exhibits half-symmetry in the *X*-*Z* plane. Therefore it is only necessary to model half of the test strip, consisting of only one of the triangles of the double triangle superlayer and only one of the cohesive cracks. To create the half symmetry behavior, symmetry boundary conditions were applied to faces of symmetry of the model as shown in Figure 45. These boundary conditions included zero

displacement in the *y*-direction and zero rotation in the *x*-direction and *z*-direction. By using half symmetry, the number of elements within the model is halved while providing the same results as a full model. Also, to complete the boundary conditions for both the global and local models, the nodes on the outer edge of the test material at the location with the largest *y*-values, had the nodal displacements fixed in all directions. This boundary condition is to simulate the edge of free-hanging test material where it is rigidly attached to the silicon wafer substrate. Since the silicon wafer is much thicker with high rigidity, the silicon substrate platform was not modeled in the analysis.

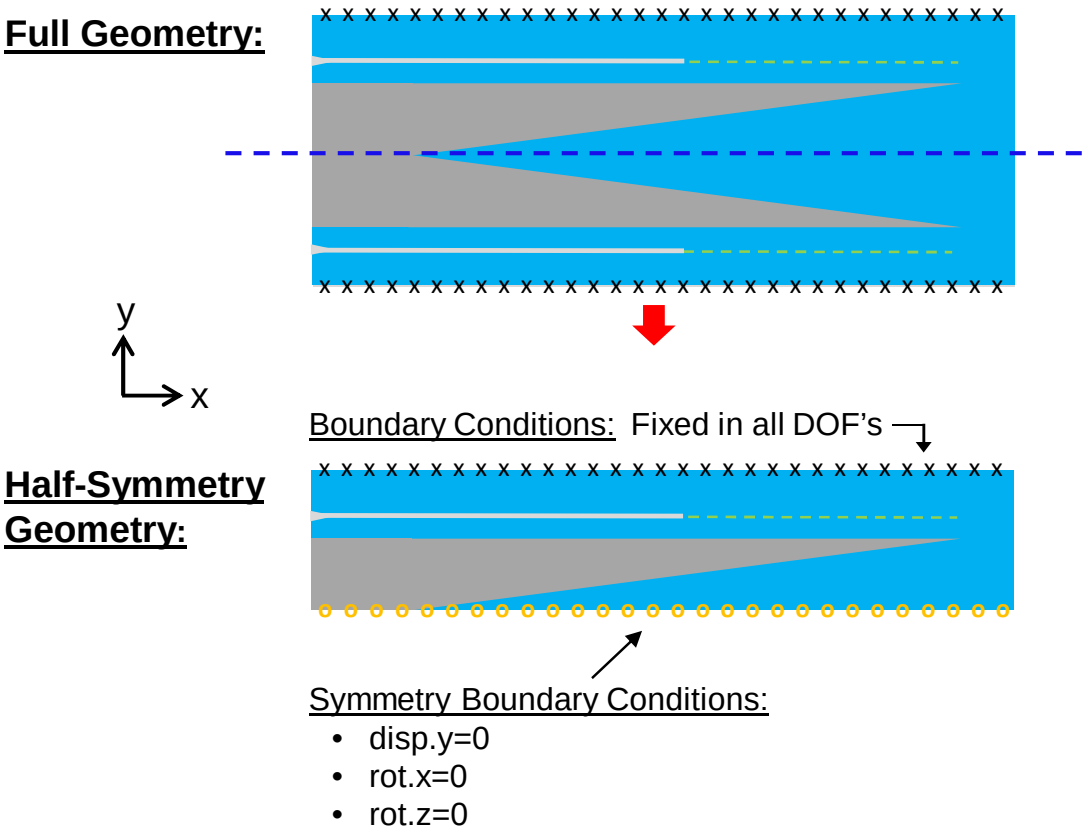


Figure 45: Illustration the half symmetry used for the finite-element model of the cohesive fracture test and the boundary conditions used.

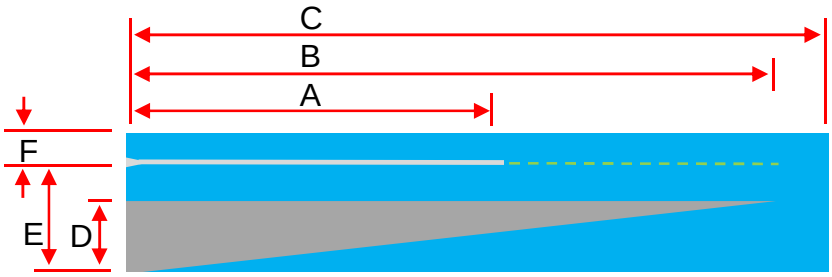


Figure 46: Illustration of top-view of finite-element model of cohesive fracture test with half symmetry labeling the main dimensions for the model.

Table 8: List of values for the labeled dimensions illustrated in Figure 46 and used in the finite-element model.

Label	Dimension Name	Range of Values (μm)	Label	Dimension Name	Range of Values (μm)
A	Crack length	100-975	D	Superlayer half-width	100
B	Superlayer length	1000	E	Free-hanging test material width	300, 350
C	Test material length	1050	F	Fixed test material width	11

5.2.4 Finite-Element Model - Geometry

When creating the model geometry for the finite-element analysis of the cohesive fracture test, the geometry was parameterized in the ANSYS® APDL code to allow for different combinations of values to be tested. This permits different crack lengths, material thicknesses, and planar dimensions to be analyzed in addition to the other non-geometric parameters such as superlayer stress and test material properties. The key parameters of the cohesive fracture finite-element model are shown in Figure 46 and Table 8. In general, for the geometry of the finite-element model, the superlayer length

used was 1000 μm, the superlayer half-triangle width was 100 μm, test material width of free-hanging section was 300 or 350 μm, the free-hanging section of the test material attached to the substrate was 11 μm, the entire test material length was 1050 μm, and the crack length varied from 100-975 μm. Then for the local model, all of these dimensions are the same, except the model only contains a cut section of the global model. The width of this cut is 1.25 μm. This width was the chosen since it contains the stress gradient created by the crack tip of the cohesive crack of the test material.

5.2.5 Finite-Element Model – Crack Geometry

The crack in the cohesive fracture test is modeled as two separate coincident faces that join at one end as shown in Figure 47. Once a load is applied to the system, the coincident faces can separate. In this finite-element analysis containing fracture calculations such as VCCT and J-integral, the mesh at, and surrounding, the crack tip are important. To manage this, the majority of all of the elements of the global and local models are map meshes to control their size. Specifically, in front of the crack tip, and behind the crack tip, the element length is 0.5 μm for the global model and 0.015 μm for the local model. Additionally, a refined map mesh is created in the vicinity of the crack tip in the local model.

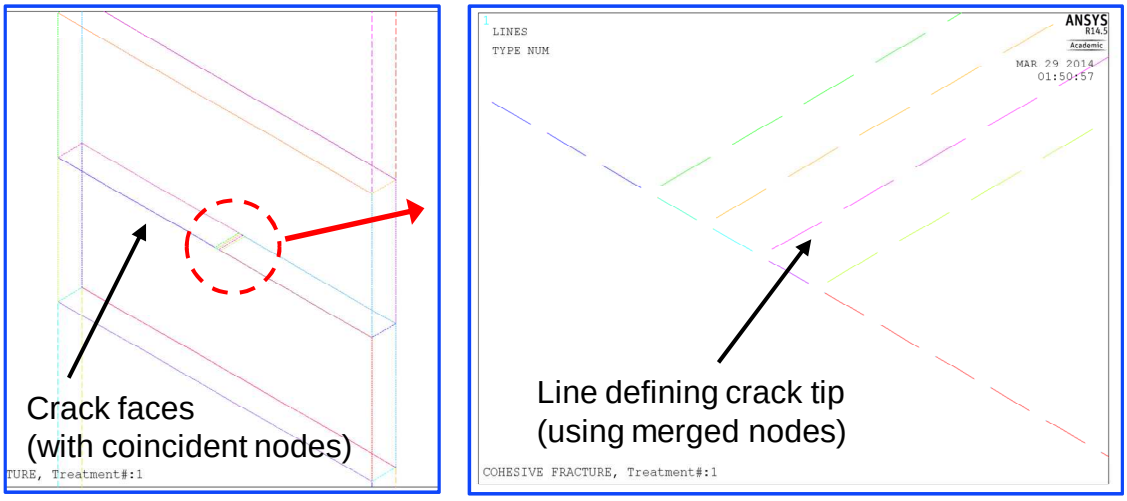


Figure 47: Images of lines of finite-element local model of cohesive fracture test. Left image shows zoomed-in image of entire width of the local model strip including the cracked region. Right image shows just the region near the crack tip and the line defining it the crack tip through the material thickness.

5.2.6 Finite-Element Model – Material Properties

The mechanical properties of the test material and the superlayer are an important component of the finite-element model. To provide accurate results for the scenario of the SiO_2 test material and chromium superlayer, the Young's modulus values for SiO_2 and chromium were measured using nanoindentation. Separate samples of each of these films were prepared on silicon wafers using the same deposition processes as the films used in the cohesive fracture test to provide representative films. The details of these nanoindentation measurements for the Young's modulus values are presented in Appendix A.3. The Young's modulus and Poisson's ratio values measured and used for silicon dioxide (E_{SiO2}) were 86.2 GPa and 0.17 [77, 102-104] respectively, and for chromium (E_{Cr}) the values were 149.54 GPa and 0.21 [105, 106] respectively. These properties were modeled with linear elastic behavior in the finite-element analysis. Additionally, for any given analysis in this investigation, if not stated, these values for the mechanical properties should be assumed. In a later section of this chapter, the modulus

of the test material will be varied in several finite-element analyses to investigate the application of this cohesive fracture test on other materials besides silicon dioxide.

5.2.7 Finite-Element Model – Modeling Superlayer Intrinsic Stress

One of the most important components behind the concept of this cohesive fracture test is the intrinsic stress of the superlayer film. It is this high level of tensile stress in the superlayer that drives the cohesive fracture in the test material to allow for measurement of the cohesive fracture toughness. Therefore, it is extremely important to accurately model the superlayer film stress in the finite-element analysis. It was first attempted to use the ANSYS® built-in command, INISTATE, to create the initial stress in the superlayer. It was found that this command accurately models the film stress and resulting forces and displacements, but not the strain energy and the command is also not available for all element types. The ANSYS® calculated strain energy values for the stressed film resulted in negative values using this command. These negative strain energy values yield incorrect values if the finite crack extension approach is used to calculate the strain energy release rate. This approach requires the change in strain energy of the system to be calculated, between two different models if a crack is grown an incremental distance, Δa. Therefore, a different approach was used to model the superlayer stress. It was decided to create the stress in the superlayer with an equivalent thermal stress.

With this equivalent thermal stress approach, a coefficient of thermal expansion is assumed for the superlayer material, while the test material is given a coefficient of thermal expansion of zero. This is done to only create an initial stress in the superlayer and not the test material when a temperature is applied. To create a desired equivalent

biaxial thermal stress in the superlayer, a temperature is calculated using Hooke's law (Equation 11) and the equation for thermal mechanical strain (Equation 12) [105] given below. Then the temperature that should be used to create the desired initial stress, σ_i, in the ANSYS® model is given by Equation 13. In the finite-elements analysis of the cohesive fracture test, a tensile stress in the superlayer was desired; therefore Equation 13 yielded a negative change in temperature to be applied to the finite-element model.

$$\varepsilon_x = \frac{1}{E_{film}}\left(\sigma_x - \upsilon_{film}\left(\sigma_y + \sigma_z\right)\right) \tag{11}$$

$$\varepsilon = \left(\alpha_s - \alpha_f\right)\Delta T \tag{12}$$

$$\Delta T = \frac{\left(\frac{1}{E_{film}}\right)\left(\sigma_x - \nu_{film}\sigma_y\right)}{-\alpha_{film}} \tag{13}$$

This equivalent thermal stress method was validated by comparing results obtained with a finite-element analysis that utilized such an equivalent thermal biaxial stress with an analytical calculation for this specific scenario [105, 107]. The comparison was done using a 3D circular disk with a radius of 50 μm composed of a 5 μm thick substrate of one material and with a film of another material on top of it with a thickness of 0.4 μm. The comparison between these two models produced a difference in curvature and substrate strain energy less than 0.5%, while the film strain energy difference was less than 4%. Therefore, it was determined that the equivalent thermal stress approach results in correct deformation and strain energy values, and thus, is viable for finite-element analysis of this cohesive fracture test. Also, when applying this stress in the ANSYS® model, the equivalent thermal stress was applied in both the global and local models with the stresses σ_x and σ_y possessing the same values for both directions.

5.2.8 Finite-Element Model – Fracture Mechanics

To calculate the cohesive fracture resistance using the test method of this thesis, it is necessary to calculate the strain energy release rate for a specific crack length of the test strip. The term, strain energy release rate (G), is the energy dissipated during fracture per unit of new crack surfaces created, or simply a measure of the energy available for an increment of crack extension, and is given by (Equation 14) [30]:

$$G = -\frac{d\Pi}{dA} \tag{14}$$

In this relationship, Π is the potential energy supplied by internal strain energy and external forces, and A is the crack face area. Using this relationship, the energy release rate (ERR) can be theoretically calculated for any crack length in a material. For all materials, there exists a specific value of energy release rate called the critical energy release rate (G_c), which is a material property and a measure of the material's fracture toughness [30]. If the calculated energy release rate for a specific crack is lower than the critical energy release rate ($G < G_c$) the crack will not propagate. Conversely, if the calculated energy release rate for the crack is greater than the critical energy release rate ($G > G_c$), the crack will propagate. At the location where the crack ceases to propagate, the energy available for crack propagation is equal to the critical energy release rate ($G = G_c$). This is also directly related to the main concept behind this cohesive fracture test and the triangular shaped superlayer. At the initial crack notch of the test specimen, the width of the triangular superlayer is very large, and thus providing a large amount of potential energy, Π, which causes $G > G_c$ and therefore propagation of the cohesive crack. As the crack propagates, the width of the triangular superlayer at the crack tip decreases, and therefore so does the potential energy and the resulting strain energy

release rate since the incremental change in the crack face area remains constant. As the crack propagates through the test material, along the length of the triangular superlayer, eventually a specific crack length and corresponding superlayer width is reached where $G = G_c$. Therefore, allowing a measurement of the critical energy release rate of the material and a measurement of the cohesive fracture resistance.

Two methods commonly utilized in finite-element analyses to calculate the energy release rate are: 1) the virtual crack closure technique (VCCT) and 2) the J-integral. Both of these methods will be used in this analysis to calculate the energy release rate in the finite-element models of the cohesive fracture test samples. One benefit of these two methods is that they are capable of calculating the energy release rate for a specific crack length with only one simulation, which greatly reduces the calculation time and the results file size. This is unlike the finite crack extension method that requires two separate simulations to determine the actual difference in strain energy calculated from two separate models with incrementally different crack lengths. Another benefit of these two methods is that they do not require special elements to perform the fracture calculations. Other fracture methods employed in finite-element analysis require special singular elements that have mid-side nodes moved one-quarter the distance from the original midpoint position. The crack tip is then placed at this modified mid-side node to allow for the crack tip singularity to be captured in this approach. Therefore, the VCCT and the J-integral possess desirable characteristic for the fracture calculations of the cohesive fracture test.

To calculate the energy release rate using the VCCT and a single simulation, the energy needed to incrementally close the crack must be calculated. This is illustrated by

the nodes and elements of one half of a crack face depicted in Figure 48. To calculate the closing energy, it is assumed that the force required to close the crack at node j is equal to the force on the adjacent node i (the crack tip). This force is found by selecting node i and only the elements of one side of the crack face geometry. The three directional components of this force are then multiplied by the respective displacements of node j. This multiplication of approximated forces at node j that were obtained from node i, and the calculated displacements at node j, yields values for the energy to close the crack. These values are then divided by the crack face area, which is calculated from the geometric terms Δl and b that are defined by the size (length and thickness) of the elements behind and ahead of the crack tip as given in Figure 48. In the finite-element analysis for this investigation, the crack tip region mesh details (values of Δl and b) are given in Sections 5.2.2 and 5.2.5. All these elements were of equal size and map meshed to control their size and shape. Using all these discussed terms then allows for the three different directional components of the energy release rate as defined in Equation 15 - 18 to be calculated as shown below:

$$G_I = -\frac{1}{2\Delta lb} F_{iy} * \Delta v_j \tag{15}$$

$$G_{II} = -\frac{1}{2\Delta lb} F_{ix} * \Delta u_j \tag{16}$$

$$G_{III} = -\frac{1}{2\Delta lb} F_{iz} * \Delta w_j \tag{17}$$

$$G_T = G_I + G_{II} + G_{III} \tag{18}$$

In this analysis, the reported values for the energy release rates will be the total energy release rate G_T calculated from the node located at the middle of the thickness of the test material along the line defining the crack tip if not stated otherwise.

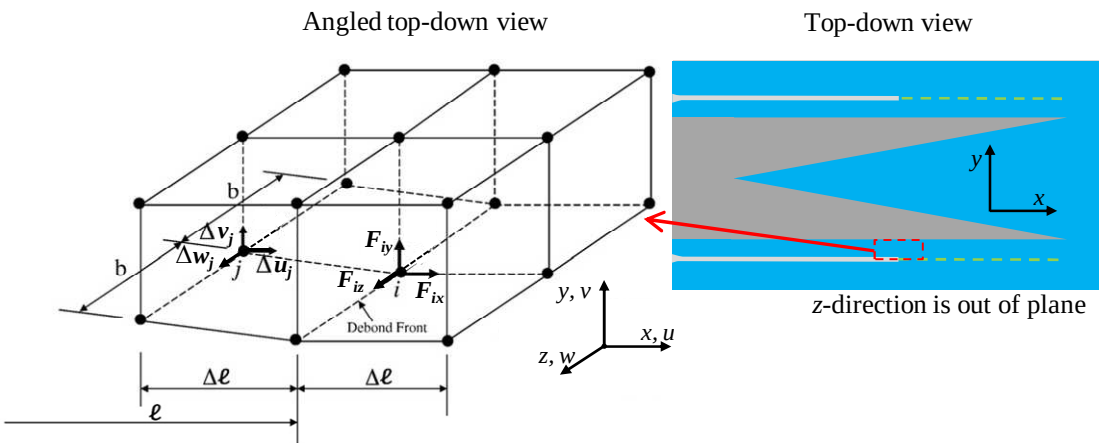


Figure 48: Illustrates the calculation of the energy release rate using VCCT within a finite-element analysis. The elements represent one of the faces of the cohesive crack and show the crack tip node used to determine the forces and the node in front of the crack tip to determine the crack displacements [108].

The second method that will be used to calculate the energy release rate is the J-integral. The J-integral is a widely accepted method to calculate the energy release rate in fracture and is valid for both linear and non-linear material behavior scenarios [30]. This calculation is performed with the following contour integral (for a 2D case) starting at one of the crack faces and traveling around the crack tip to the adjacent crack face (Figure 49). For a 2D case, area integration is used, while in a 3D case, volume integration is used. In the integral below, W is the strain energy density, T is the kinematic energy density, σ represents the stress, u is the displacement vector, and Γ us the contour over which the integration is carried out [109]:

$$J = \lim_{\Gamma \to 0} \int_{\Gamma_0} \left[(W + T)\delta_{1i} - \sigma_{ij} \frac{\partial u_j}{\partial x_1} \right] n_i d\Gamma \qquad (19)$$

The calculation of the J-integral using ANSYS® finite-element analysis is executed using the CINT command. For every simulation of the cohesive fracture test strips, the energy release rate was calculated with both the VCCT and the J-integral using the same mesh for the model and the crack tip. These two methods calculate the energy

release rate by two very different approaches and therefore provide a form of verification of the calculated values. The energy release rate calculated using these two methods generally differed less than ~4% from each other and therefore this similarity between the two different approaches provides validity to the calculations.

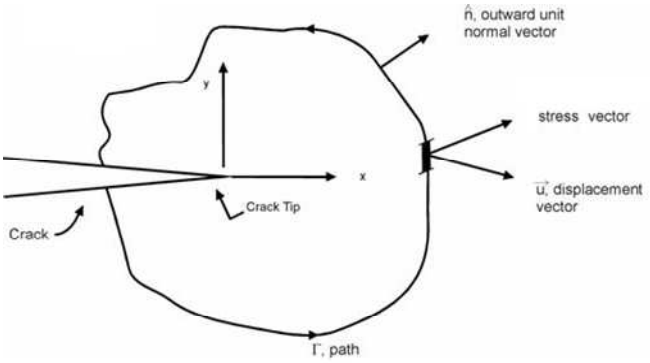


Figure 49: Illustration of calculation of the J-integral to calculate the energy release rate for a 2D case. The figure shows the crack and the path of the area integration used in a 2D calculation [109].

5.3 Finite-Element Analysis Results

5.3.1 Test Material Thickness

The first variable of the cohesive fracture test that was investigated with the finite-element model discussed in this chapter was the effect of the test material thickness. To investigate the effect of this parameter, the thickness of the test material was varied from 0.05 μm to 1.0 μm in seven different finite-element analyses. These are typical thin film thicknesses that are used in clean room fabrication processes at Georgia Institute of Technology, and therefore formed the range studied here. For this investigation, silicon dioxide was used as the test material, with material properties of E = 86.2 GPa and ν = 0.17 [77, 102-104], while using a chromium superlayer with a stress of 1.54 GPa and material properties of E = 149.54 GPa and ν = 0.21 [105, 106]. For all of the simulations in this investigation, the superlayer possessed a thickness of 0.2 μm and

the width of the free-hanging test material was 250 μm, while all other parameters were the same as used in previous finite-element analyses of this thesis.

The results for a cohesive crack growing from 100 μm to 900 μm for each of these seven simulations of different test material thicknesses are shown in Figure 50. These results demonstrate that the energy release rate for a given crack length decreases when the thickness of the test material is increased while keeping the superlayer parameters constant. This observation is expected, since for example, if a cohesive fracture test sample is fabricated with a test material thickness of 0.05 μm, and the measured crack length is 700 μm, according to the Figure 50, the critical total energy release rate is then ~68 J/m^2. But if another sample is fabricated with a test material thickness of 1.0 μm and the same crack length is measured, then the critical total energy release rate is ~4 J/m^2. If the same crack length is measured for two scenarios of different test material thicknesses, then the thinner material must have a greater critical energy release rate due to its great resistance to fracture.

Additionally, the comparison of the total energy release rate between the different scenarios for successive crack lengths was determined to be fairly consistent. For example, the total energy release rate for the scenario with test material thickness of 0.05 μm was ~170-190% greater than the total energy release rate for the scenario with a test material thickness of 1.0 μm for each respective crack length. This shows that the effect of the test material thickness is predictable for the design of future tests.

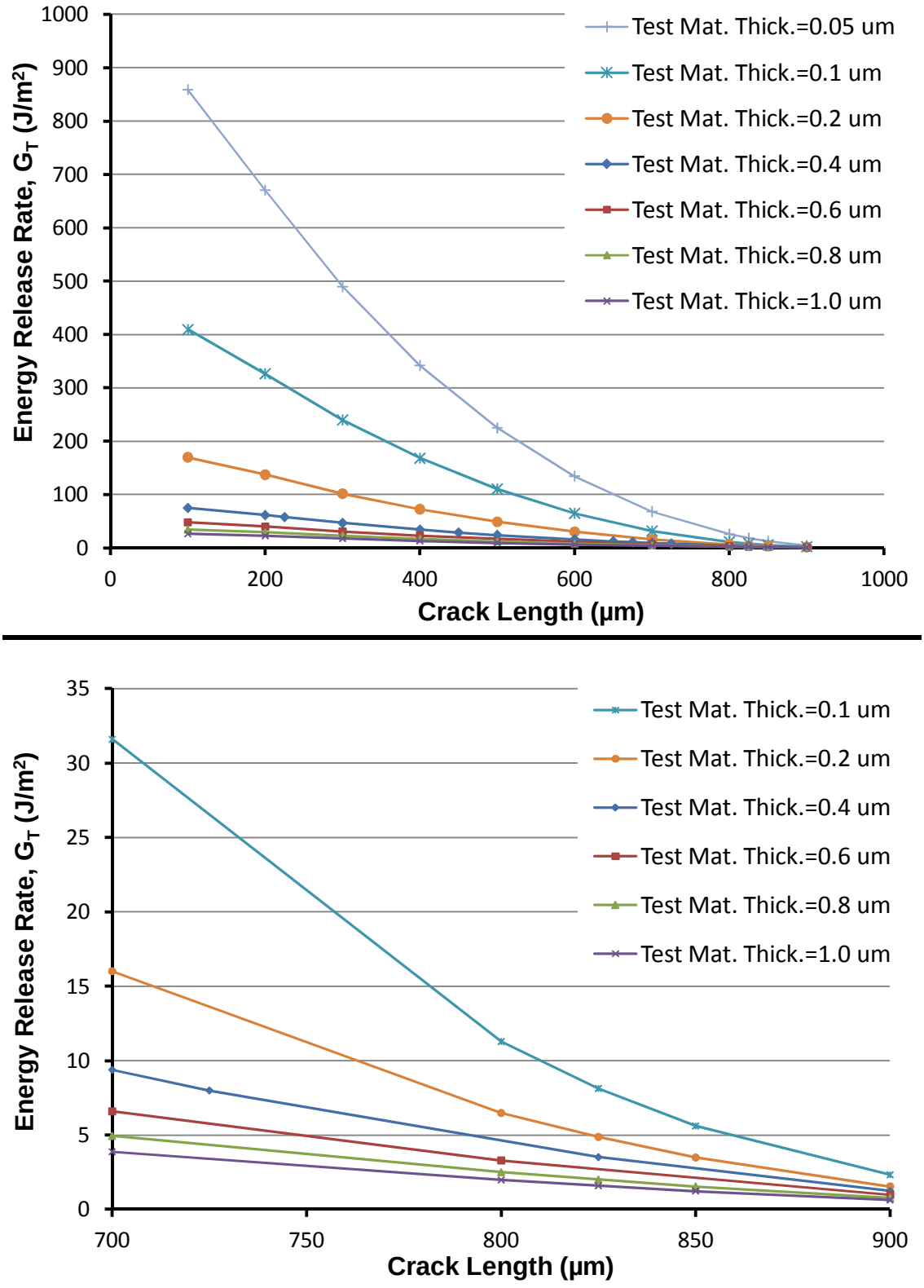


Figure 50: Plots of energy release rate vs. crack length for different test material thicknesses. Top plot is for cracks of 100-900 μm, and bottom plot is zoomed in on 700-900 μm.

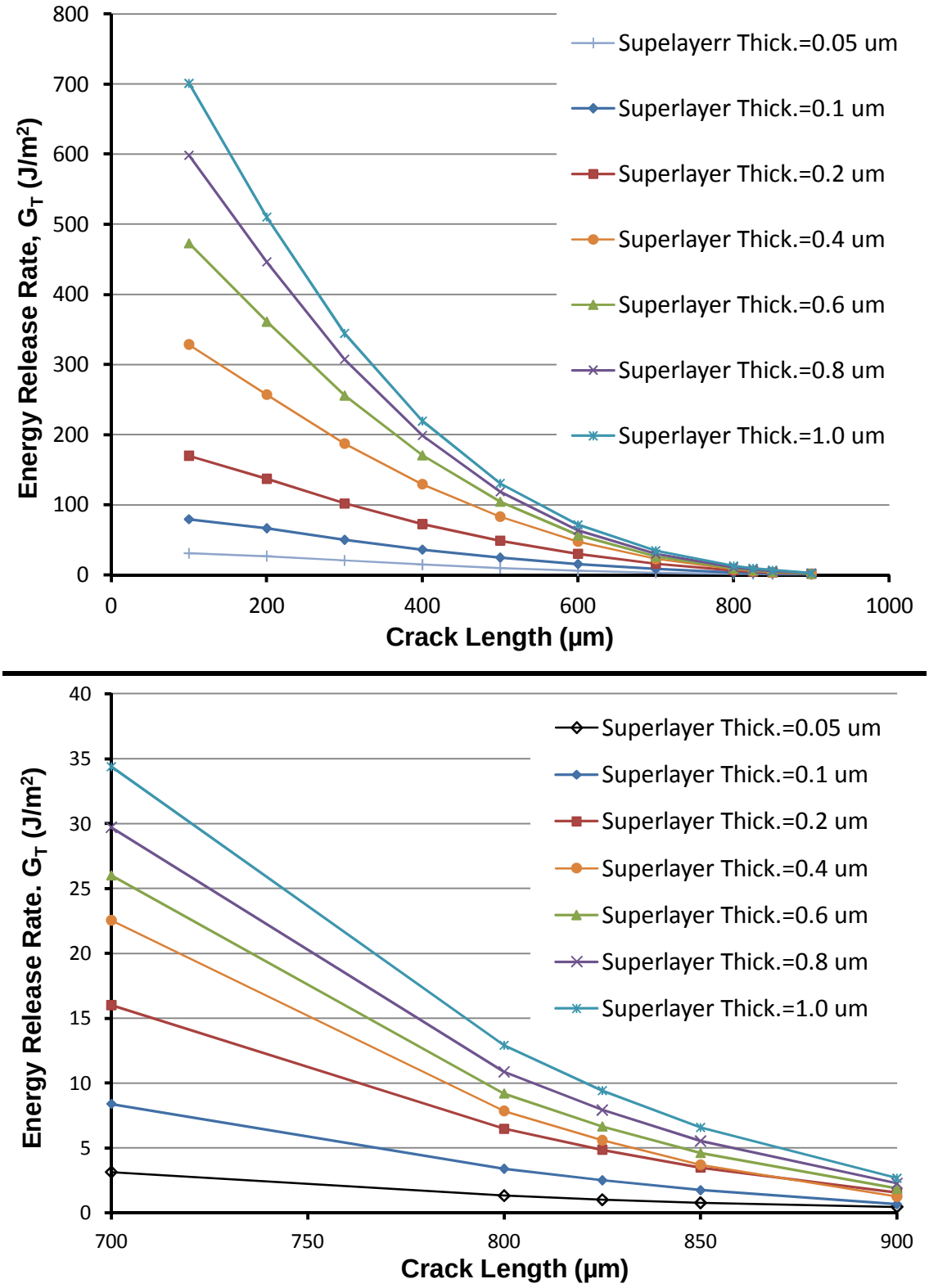


Figure 51: Plots of energy release rate vs. crack length for different superlayer thicknesses. Top plot is for cracks of 100-900 μm, and bottom plot is zoomed in on 700-900 μm.

5.3.2 Superlayer Thickness

Another major variable that was studied using this finite-element model was the effect of the superlayer thickness. To investigate the effect of this parameter, the thickness of the superlayer was varied from 0.05 μm to 1.0 μm in seven separate finite-element analyses. In this study, silicon dioxide was used as the test material, with material properties of E = 86.2 GPa and ν = 0.17 [77, 102-104], while using a chromium superlayer with a stress of 1.54 GPa and material properties of E = 149.54 GP and ν = 0.21 [105, 106]. For all of the simulations in this investigation, the test material possessed a thickness of 0.2 μm and the width of the free-hanging test material was 250 μm, while all other parameters were the same as used in previous finite-element analyses of this thesis.

The results for a cohesive crack growing from 100 μm to 900 μm for each of these seven simulations of different superlayer thicknesses are shown in Figure 51 and an enlarged view of the portion for crack lengths of 700 μm to 900 μm is also shown in Figure 51. The trends of these plots are opposite to those previously discussed in the test material thickness study. Specifically, this investigation demonstrates that the energy release rate increases with increasing superlayer thickness for a given crack length while keeping all other test parameters constant. To illustrate this trend, consider a test specimen fabricated with a superlayer thickness of 1.0 μm that has a measured crack length of 700 μm, and therefore according to Figure 51, has a critical total energy release rate of ~34 J/m^2. But, if a different sample is fabricated with a superlayer thickness of 0.2 μm and has the same measured crack length of 700 μm, the critical total energy release rate is then 16 J/m^2. The greater energy release rate for thicker superlayer

thicknesses at a given crack length occurs due to there being more energy for fracture possessed by the superlayer having a greater volume of stressed material as compared to thinner superlayers. The scenario with the thicker superlayer would have to provide a greater energy release rate and therefore be more crack resistance compared to a scenario with a thinner superlayer thickness. Thus these thicker superlayers have more driving force for fracture and therefore should provide a larger energy release rate. Additionally, the results of Figure 51 show that the results for the different scenarios of varying superlayer thickness are more evenly spaced than Figure 50 for the investigation of test material thickness. This demonstrates a stronger effect of the test material thickness than the superlayer thickness.

5.3.3 Superlayer Stress Value

Similar to the previous study on the effect of the superlayer thickness, the effect of the magnitude of the superlayer stress was also investigated. In this study, three different cohesive fracture test scenarios of superlayers with stresses of 0.5, 1.0, and 2.0 GPa were modeled using finite-element analysis. These stress levels are similar to those that are capable by using various materials and deposition processes. In these finite-element models the superlayer stress was varied while keeping all other parameters the same, with silicon dioxide ($E = 86.21$ GPa, $\nu = 0.17$ [77, 102-104]) material properties used for the test material, and chromium ($E = 149.54$ GPa, $\nu = 0.21$ [105, 106]) material properties for the superlayer. Also, the test material thickness utilized was 0.2 μm and the superlayer thickness was 0.1 μm, while the width of the free-hanging section of the test material was 300 μm. The results of the total energy release rate for these three different superlayer stress scenarios for crack lengths from 100 μm to 900 μm are

presented in Figure 52. These results demonstrate a similar trend to what was determined from the study on superlayer thickness. Specifically, that the energy release rate for a given crack length increases with increasing levels of stress possessed by the superlayer. The energy release rate increases due to the higher stress levels creating more driving force and fracture energy.

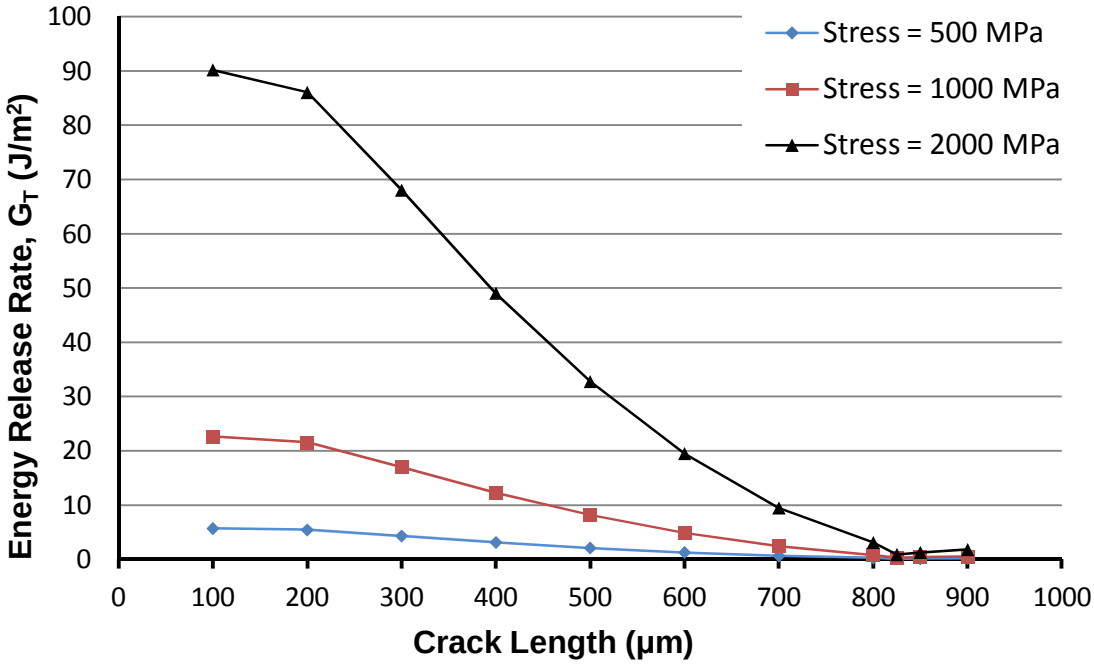


Figure 52: Plot of energy release rate vs. crack length for different superlayer stress values for crack lengths of 100-900 μm.

5.3.4 Test Material Modulus

Another parameter of interest of the finite-element model for this cohesive fracture test is the test material's Young's modulus. By varying the value for the Young's modulus used in the finite-element analysis, it is possible to investigate the resulting energy release rates if this test method was utilized to measure the fracture resistance of other thin films besides silicon dioxide. Therefore, Young's modulus values of 10, 50, 100, 200, and 300 GPa were used in the finite-element model to investigate a

wide range of potential test materials. For example, potential materials of interest that are common in MEMS and microelectronic fabrication that are within this range of values include aluminum oxide [110, 111], hafnium oxide [112], silicon nitride [113, 114], titanium oxide [115, 116], carbon doped silicon oxide (SiCO:H) [117, 118], and hydrogenated nitrogen silicon carbide (SiCN:H) [117]. In the finite-element model for this study, the thickness of the test material was 0.2 μm and the thickness of the superlayer was 0.1 μm with material properties of chromium ($E = 149.54$ GPa, $\nu = 0.21$ [105, 106]). Also, the intrinsic stress of the superlayer was 1.64 GPa and the width of the free-hanging section of the test material was 300 μm.

The results for a cohesive crack growing from 100 μm to 900 μm for each of these simulations with different test material moduli are shown in Figure 53. The trends that are demonstrated with these plots are similar to those found from the study on the test material thickness. In the investigation here, a decrease in the test material modulus, cause an increase in the total energy release rate for a given crack length. A material with a low Young's modulus will result in a greater deformation for a specific load compared to a material with a larger Young's modulus. Therefore if two materials with different modulus are tested with this cohesive fracture method and result in the same crack length, then the material with the lower modulus must have a greater resistance to fracture, and thus a larger critical total energy release rate. Additionally, Figure 53 provides insight on how to utilize this cohesive fracture test when using it to test other materials, with respect to choosing material thicknesses and superlayer stresses. For example, to test a material with a low modulus, it may be necessary to chose a thick test material thickness, thin

superlayer thickness, and lower superlayer stress so that the energy for fracture is not too great for the film.

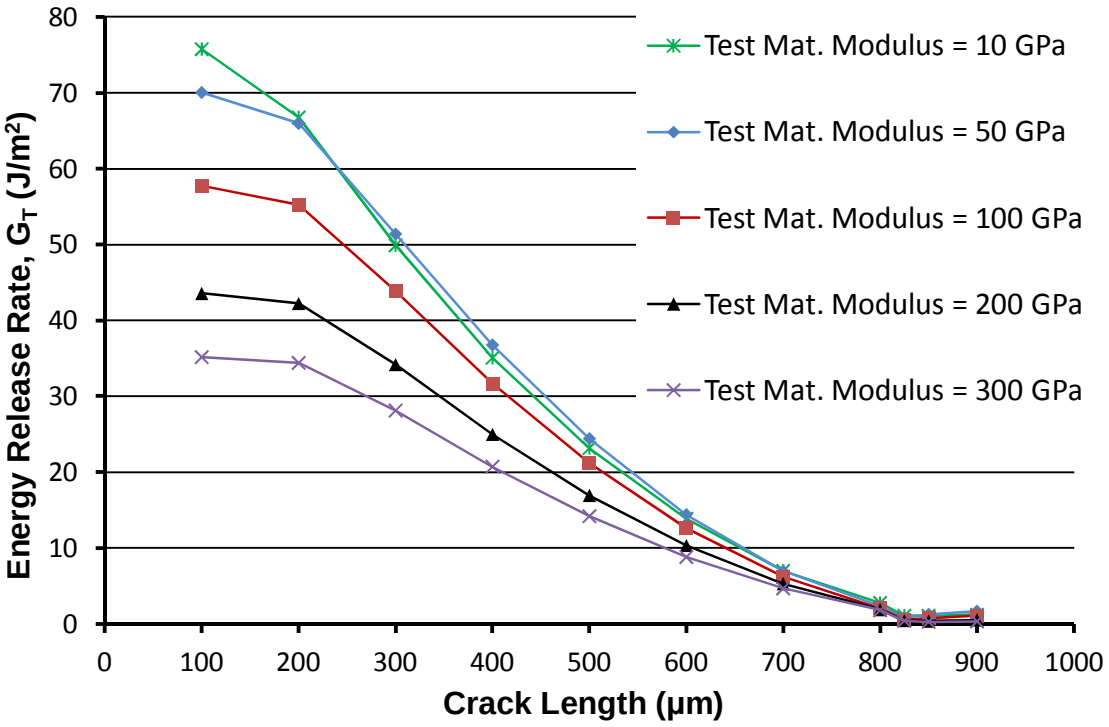


Figure 53: Plot of energy release rate vs. crack length for different Young's modulus values for the test material for crack lengths of 100-900 μm.

5.3.5 Width of Free-hanging Section of Test Material

The last parameter of the cohesive fracture test that was investigated using finite-element analysis was the width of the free-hanging section of the test material (as labeled in Figure 46). This was investigated, since when designing the cohesive fracture test strips, a width for this free-hanging section must be chosen. While the minimum width of the free-hanging section in the current test configuration is limited by the width of the superlayer triangle, there is no limit to the maximum. Therefore to study any effect, different widths of 250, 300, and 350 μm were used in three different finite-element analyses of the cohesive fracture test. In this investigation the test material used was

silicon dioxide (E = 86.21 GPa, ν = 0.17) with a thickness of 0.193 μm and the superlayer used was chromium (E = 149.54 GPa, ν = 0.21) with a thickness of 0.105 μm and an intrinsic stress of 1.64 GPa. All other parameters were the same as in previous analysis in this chapter.

The results for a cohesive crack growing from 100 μm to 900 μm for each of these simulations with different test material widths for the free-hanging section are shown in Figure 54. One trend that is illustrated by these three plots is that the shape of the plots changes slightly depending on the width. Specifically, as the width of the test material decreases, the curve of total energy release rate vs. crack length exhibits a greater linear behavior in the section of the curve at short crack lengths. This is because as the superlayer attempts to curl at these short crack lengths for the scenario where the free-hanging section of the test material width is large compared to the width of the superlayer, then the free-hanging section is less rigid and less constrained with more free play, as compared to a scenario of smaller test material width. Similarly, the plots of Figure 54 demonstrate that as the width of the free-hanging section of the test material decreases, the total energy release rate increases for a given crack length. This occurs because the smaller widths of the free-hanging section of the test material allow more energy to drive fracture as opposed to bending the free-hanging section of the test material. In, general the width of the free-hanging section of the test material compared to the width of the superlayer has an effect on the energy release rate of the cohesive fracture test. This offers another parameter to vary when designing a test for a new test material to achieve the desired range of energy release rates to subject the material to.

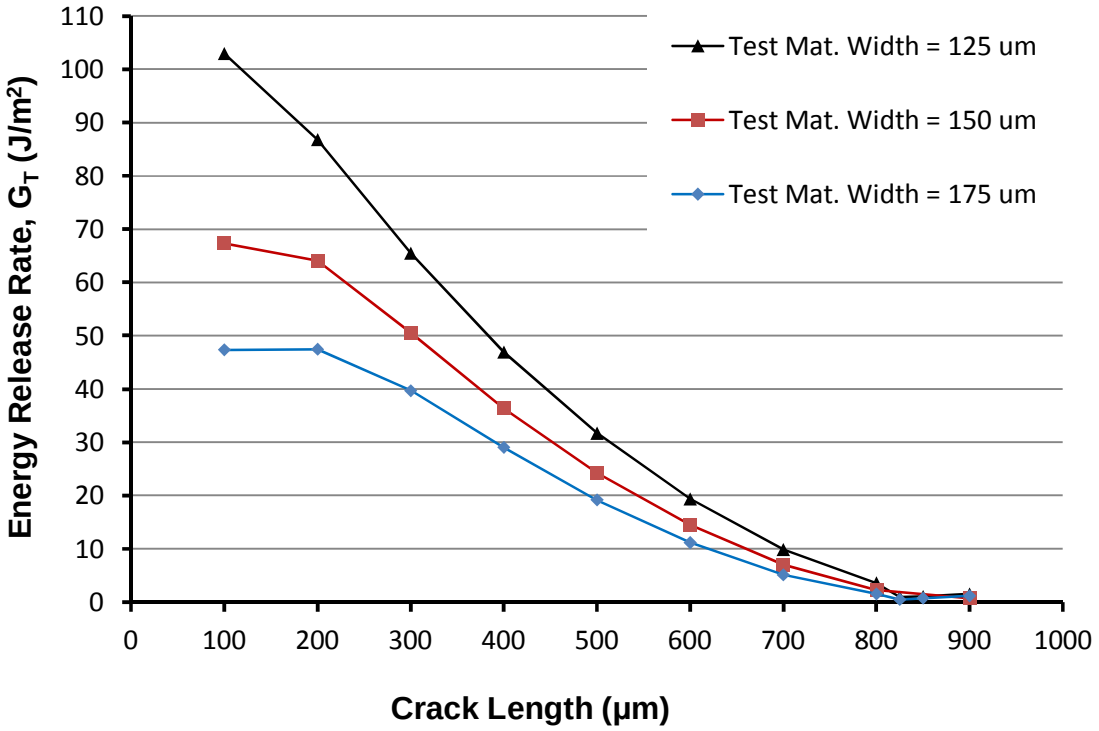


Figure 54: Plot of energy release rate vs. crack length for different test material width (free-hanging section) values for crack lengths of 100-900 μm.

5.4 Conclusion

In this chapter the finite-element analysis of the cohesive fracture test, which is a main component of this thesis, was presented and discussed. The finite-element analysis of the cohesive fracture test is important because the experimental results of the cohesive fracture samples produce a measurement of the critical cohesive crack length, or width of the superlayer at the crack tip, that then needs to be correlated to the critical total energy release rate. Therefore in this chapter, the development of the finite-element analysis of the cohesive fracture test was discussed in detail, including the choice to utilize 3D modeling, the use of half-symmetry, and the boundary conditions employed to accurately represent the cohesive fracture test samples. Additionally, due to the contrast in large planar dimensions compared to micro/nano film thicknesses, it was necessary to use a

global-local modeling approach to perform the calculation of the energy release rate at the crack tip. The specifics of this global-local model were presented.

Another extremely important aspect of this cohesive fracture test is the use of the superlayer with high intrinsic stress to drive cohesive fracture in the test material without using external loads and eliminating the need for traditional fixturing. To model the biaxial intrinsic stress in the finite-element model, an equivalent thermal stress was determined and used. Additionally, the validity of this equivalent thermal stress was demonstrated with respect to the resulting curvature and strain energies for a situation with a known analytical solution.

To provide a measurement of the test material's resistance to fracture, the total energy release rate was calculated using the VCCT. Additionally, these values obtained using VCCT were supported by calculating the J-integral, which produced fracture resistance values within 5% of the VCCT calculations and thus providing corroboration. Also, the finite-element analysis of the cohesive fracture test strip was performed while increasing the crack length for successive simulations to demonstrate the fundamental concept of the test, to show that the energy release rate decreases as the crack is grown. This is due to the triangular shape of the superlayer, where the planar width of the superlayer at the location of the crack tip decreases as the crack is grown. All of the analyses performed of the different test sample scenarios demonstrated this fundamental concept.

During the design of this cohesive fracture test, key parameters were identified that were of interest to investigate the effects of and to potentially improve future test designs. These parameters include the effect of the test material thickness, superlayer

thickness, superlayer stress, test material modulus, and the width of free-hanging section of the test material. Each of these parameters was investigated in separate studies, where the parameter of interest was varied while keeping all the others constant. It was found that the effect of each of these parameters agreed with initial hypotheses. For example, as the test material thickness or the test material modulus is decreased, the total energy release rate for a given crack length increases. Conversely, as the superlayer thickness or the superlayer stress level is decreased, the energy release rate for a given crack length increases. The combination of all of these parameters and their trends enable the cohesive fracture test to be varied in order to accommodate a wide range of potential test materials besides silicon dioxide. This is necessary since such potential test materials will have various combinations of Young's modulus and cohesive fracture resistance. The fracture test applied to them must simultaneously provide enough energy to initiate fracture, while also allowing the critical total energy release rate to be within the main section of the energy release rate vs. crack length relationship. In summary, the finite-element model of the cohesive fracture test was created and discussed in detail in this chapter to allow for the calculation of the critical energy release rate from the experimentally measured crack lengths. Additionally, the trends and relationships of the key parameters were presented and show that the mechanics behind this fracture test are predictable, and therefore allow for future application on different materials.

CHAPTER 6

MECHANICAL CHARACTERIZATION OF CARBON NANOTUBES FOR OFF-CHIP INTERCONNECTS

6.1 Introduction

The purpose of the mechanical characterization of the CNT forests is to measure their effective modulus and better understand their behavior. These measurements form the basis for the material properties used in a finite-element analysis of an electronic package using CNT forests as electrical off-chip interconnects later in Chapter 7. The measurement techniques developed and discussed in this chapter are used as an improvement to approaches and an extension to already reported studies/values in literature that were discussed in Section 1.2.3 (Effective Mechanical Property Characterization of CNTs). The techniques in this chapter focus on measuring the effective modulus. This is because in the target application of off-chip interconnects, forests of CNTs will be used, and the CNTs in the forests act in unison as a single material due to Van der Waals forces and CNT entanglement [75, 119, 120]. Several different measurement techniques were developed in this thesis to provide insight on the nature of CNT forest deformation and include:

1.) Nanoindenter based measurement technique

2.) Nanoindenter based technique with preloaded test specimens

3.) Semi-insitu SEM based technique

4.) Tensile tester based measurement

These techniques and the results will be discussed in this chapter and show that while individual CNTs have reported values of tensile modulus in the ~100 GPa [43] – 4.15 TPa [8] range, the effective modulus can be orders of magnitude lower, in the 0.1-1.0 MPa range. These measurements show that CNTs are extremely compliant structures that could be used in other new applications such as off-chip electrical interconnects.

6.2 Nanoindenter Based Measurement Technique

To explore new potential applications and to create better and more reliable designs that utilize such CNT forests, it is necessary to characterize the mechanical properties of CNT forests. The test technique presented in this section utilizes nanoindentation of parallel plates of silicon with CNT forests sandwiched between them to measure the CNT compressive modulus. The presented approach addresses the challenges associated with extracting the effective compressive modulus of CNTs using a flat or Berkovich tip, as discussed later in Section 6.2.2.

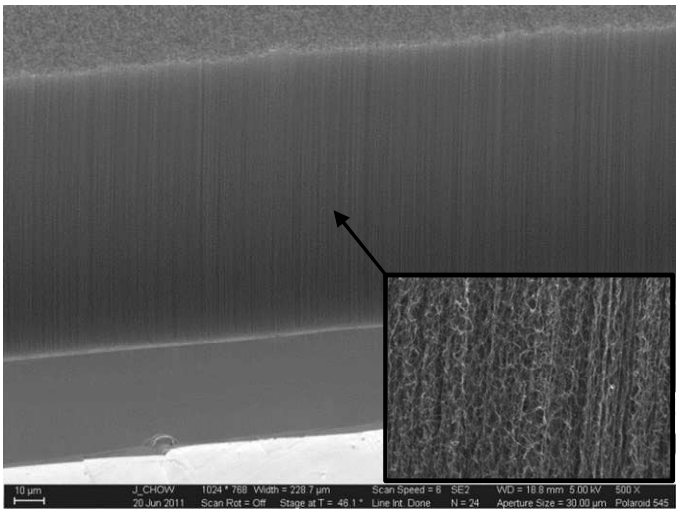


Figure 55: SEM image of VACNTS grown on silicon substrate. Image shows side of VACNT forest/turf and free tips. Inset shows higher magnification image of the "waviness" of VACNTS.

6.2.1 CNT Test Sample Fabrication

To measure the effective compressive modulus of vertically aligned carbon nanotube forests, sandwiched CNT samples were first fabricated. VACNT forests were grown on silicon pieces with dimensions of ~1 cm^2 with 300 nm thick thermal SiO_2, a 15 nm thick Al_2O_3 support layer via atomic layer deposition (ALD), and 2.2 nm of Fe catalyst via e-beam evaporation. Then the VACNTs were grown (Figure 55) using thermal chemical vapor deposition, as outlined in [121]. The heights of the CNTs grown for different test samples were 61, 315, and 683 µm with a CNT density of <9%, with little variation in density to have significant effect on the measured effective modulus. After each of these samples was grown, another piece of silicon was placed on the top of the CNTs to create a sandwich structure, and the sandwich was then tested with nanoindentation. After this nanoindentation testing, the second piece of silicon was removed, coated with SU8® epoxy based photoresist, and placed on the top of the CNTs, creating a sandwich structure as shown in Figure 56. This adhesive-bonded sample was then retested with nanoindentation to investigate the effect of the CNT end condition on the measured modulus.

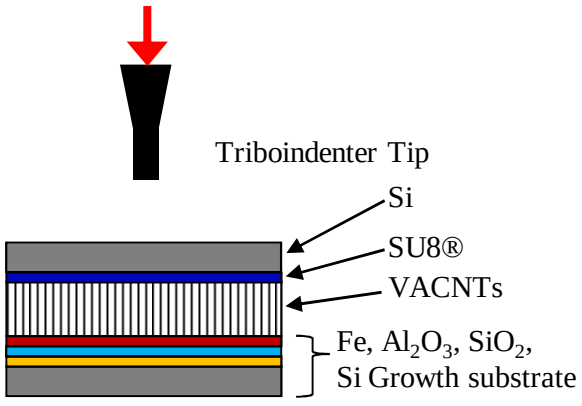


Figure 56: Si/CNT/Si sandwich sample construction used during testing. Schematic is not to scale.

6.2.2 Parallel-Plate CNT Sandwich Specimen with Nanoindentation

To perform these nanoindenter based measurements a Hysitron Triboindenter® maintained by the Georgia Tech IEN was used. The Hysitron was equipped with a high force transducer head and Berkovich tip allowing a maximum force of 1.5 N with a maximum displacement of 96 µm. The triboindenter tip was used to apply a force to the top piece of silicon of the Si/CNT/Si structure and uniformly compress the forest of CNTs as shown in Figure 56. During this test, the force and the corresponding change in height were measured by the triboindenter during compressive loading of the CNTs as well as during unloading. The tests were conducted using displacement control at a loading and unloading rate of 700 nm/s. During the test, all of the CNTs were compressed in unison between the silicon substrates, essentially like a single "foam-like" material [75, 119, 120]; therefore this entire area was used to calculate the effective properties. During these measurements the Berkovich tip of the triboindenter did not create any markings on the top silicon piece and the measured effective modulus of the CNTs was much less than that of silicon. Therefore the displacements measured by the triboindenter are due solely to the change in height of the CNTs, and not the deformation of the silicon.

This measurement method utilizing rigid parallel plates of silicon to compress the CNTs in unison allows the nanoindenter force to be distributed over the entire area of the CNT turf. On the other hand, if one were to use a Berkovich nanoindenter tip or a flat punch in direct contact with the tips of the CNTs (without a rigid substrate across the tips) to make similar force vs. displacement measurements, there are certain important issues that need to be considered. First, as reported elsewhere [48, 51, 52], the contact

area of the Berkovich tip will continue to increase with the depth of indentation and affects the area function. Second, unlike traditional solid materials, the tip regions of the compressed CNTs will have to detach or de-entangle from the surrounding CNTs to facilitate compression. Third, as the CNTs are compressed, the potential buckling and/or outward bulging of the CNTs will be constrained by the surrounding CNTs. Bulging of CNT turfs was observed by Qiu et al. during compression tests [48]. Out of these, the first aspect makes the stress data extraction difficult, while the second and the third aspect can potentially artificially increase the stiffness of the CNTs directly under the Berkovich tip. Alternatively, one can use a flat punch with the nanoindenter to address some of these issues. With the flat punch, the contact area remains the same with compression, and the stress data extraction is easier. However, the effect of surrounding CNTs on the column of CNTs that is being compressed will still be present with the flat punch experiments. The current set of experiments with parallel plates, effectively addresses three of the above issues with the Berkovich tip and/or the flat punch.

6.2.3 Nanoindentation Based Measurement Method: Results and Discussion

Compliance Curves During Compressive Loading and Unloading

In this study two general force vs. displacement curve shapes were observed during uniform compression of the CNT forests of heights 61, 315, and 683 µm by nanoindentation (Figure 57 and Figure 58). One of these curve shapes was a single upward curve similar to the response of many linear elastic materials during nanoindentation, and the other shape observed was a nonlinear curve with two distinct regions. A wide range of force vs. displacement shapes have been previously reported

for CNT turfs/forests [10, 44-49, 51, 52, 122-124]. In these reports there have been different CNT geometries, growth parameters, tested strain ranges, measurement methods such as uniform compression using parallel plates [44, 46, 47] or nanoindentation [10, 45, 47-49, 51, 52, 122, 123], different tip geometries for nanoindentation (Berkovich [48, 51, 52], flat punch [10, 45, 51, 52, 123], spherical [47], etc.), and different CNT end conditions (free, fixed, etc). The curves with only a single region obtained with nanoindentation of the 61 µm tall CNTs (Figure 57 and Figure 58) for example, is a similar response to tests of comparable strain ranges but with different nanoindenter tips used to contact the free tips of CNT forests [47, 52]. All of the curves for the different CNT samples in Figure 57 and Figure 58 exhibit mostly elastic behavior for the indentation depths tested. The 683 µm tall sample provided a curve with two distinct regions when no adhesive was used for attachment to the second silicon substrate (Figure 57). The two regions of the curve for this sample are attributed to the unevenness in the top surface of the CNT forest. Without adhesive on the second substrate, it is possible that it takes a few micrometers of displacement before all the CNT tips are engaged. This explanation is supported by subsequently obtaining a compliance curve with a single section for the 683 µm tall CNTs by using an adhesive to attach the second substrate.

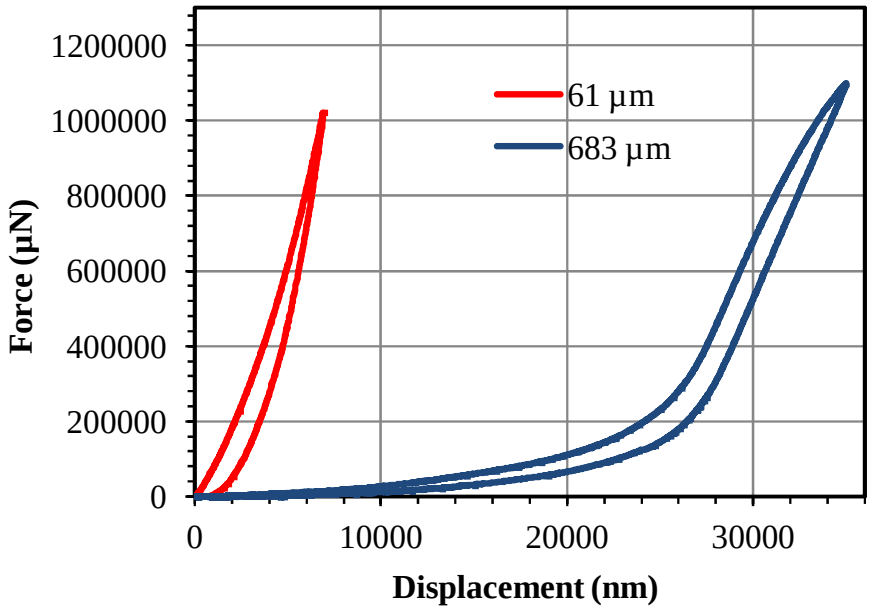


Figure 57: Compliance curves of CNTs of 61 µm and 683 µm with no adhesive connecting second Si substrate to CNT tips.

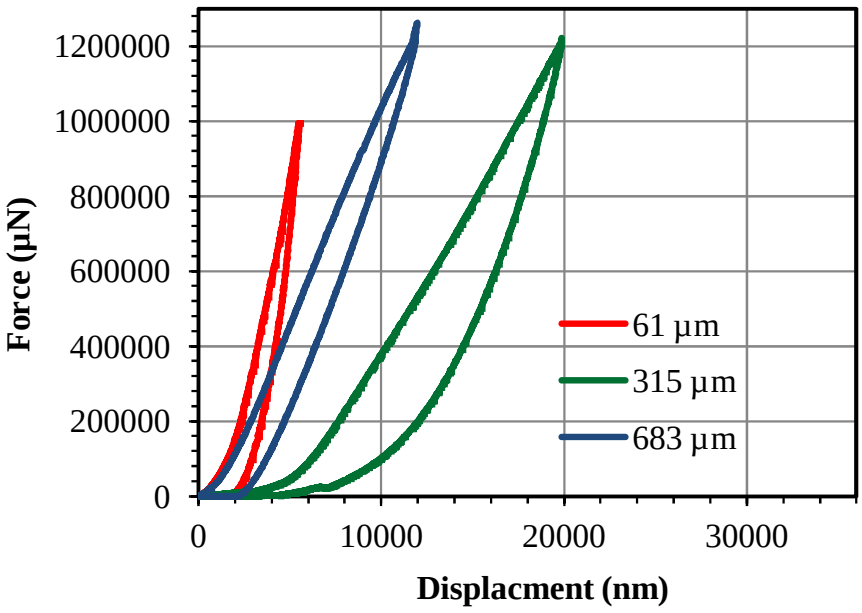


Figure 58: Compliance curves of CNTs of 61 µm, 315 µm, and 683 µm with adhesive connecting second Si substrate to CNT tips.

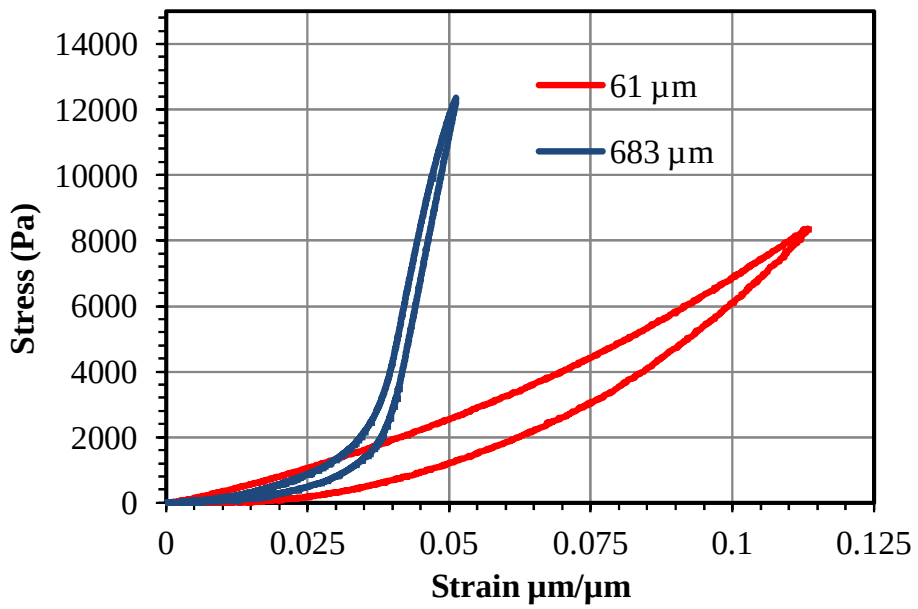


Figure 59: Stress vs. strain curves of CNTs of 61µm and 683 µm with no adhesive connecting second Si substrate to CNTs.

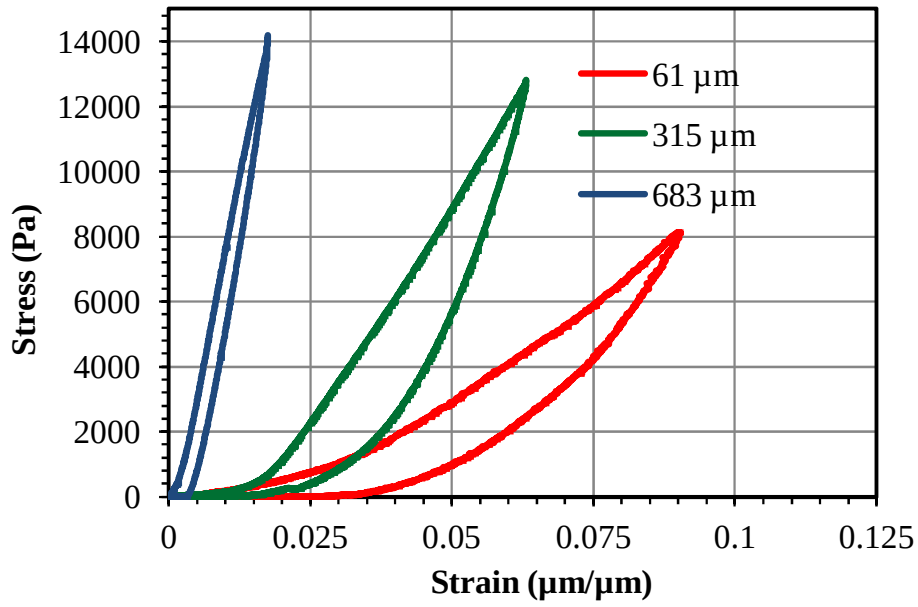


Figure 60: Stress vs. strain curves of CNTs of 61µm, 315 µm, and 683 µm with adhesive connecting second Si substrate to CNTs. The magnitude of stress and strain are shown, as both stress and strain are compressive.

Stress/Strain and Effective Modulus Data Extraction from Load vs. Displacement Curves

The main objective of this study investigating the mechanical properties of CNT forests was to obtain the modulus in the normal direction for the given CNT forests. A plot of the stress vs. strain was calculated from the force vs. displacement data by assuming that the forest acts like a foam and the force is applied normal to the CNTs during loading and unloading of the CNT sandwich structure with the nanoindenter. Prior to placing or adhering the second silicon substrate on the CNT forest to create the test samples as shown in Figure 56, the forest was imaged with an optical microscope to measure the entire area of the CNT forest normal to the applied load. For the samples tested, this area was ~1 cm^2. The normal stress was then calculated by dividing the force measured by the nanoindenter by this area of the CNT forest. Similarly, the displacement measured by the nanoindenter was divided by the initial uncompressed height of the CNT forest to obtain the corresponding strain. The stress vs. strain data during loading and subsequent unloading was plotted for each CNT height and CNT tip constraint scenarios such as CNT tips not secured with adhesive to second substrate and CNT tips secured to second substrate with adhesive (Figure 59 and Figure 60). Overall, the value of the effective compressive modulus of CNT turfs with heights 61, 315, and 683 µm and different end constraints ranged from 0.12-1.20 MPa. These values were calculated using the slope of the top 40% of the loading section and the top 40% of the unloading section of the stress vs. strain curves of Figure 59 and Figure 60 [10, 125]. All of these values are orders of magnitude less than reported values for individual CNTs [8, 126] and even of bulk graphite in tension [127]. These low measured values for the CNT forests/turfs compared to these different forms of the material could be attributed to the low density,

wavy geometry of the CNTs (as shown in Figure 55), and the folding nature of the deformation of the CNTs. This local bending/folding nature will be discussed and supported with SEM images later in this chapter (Section 6.4). While the effective compressive modulus measured here is low, it is comparable to measurements of CNT turfs/forest by selected others as shown in Table 9.

Additionally, it was observed that there was a slight dependence of the measured effective compressive modulus on the height of the CNT forest. For the heights tested in this study, the effective compressive modulus increased with increasing height. Available literature does not provide any conclusive information regarding the effect of CNT forest height on its effective modulus. This is most likely due to the differences in CNT density, alignment, and entanglement morphology and evolution during growth in various studies. For example, Tong et al. [128] found that the CNT forests with heights ranging from 15-500 µm had a compressive modulus of ~0.25 MPa that was independent for the heights tested. This independence was explained by the periodic wavy structure of the CNTs, with the more important factor being the wavelength of the evenly distributed periodic structure. Conversely, Maschman et al. [45] report that the mechanical response of CNT forests is dependent on the CNT height. The measured effective modulus for CNT forests with heights of 35, 190, 300, 650, and 1200 µm ranged from ~10-20 MPa. This paper does not specifically discuss the cause of the variation in effective modulus, but discusses how the CNT forest height and CNT alignment influence the buckling that is observed. Vertical alignment and entanglement depend on the growth conditions, and thus influence the measured compressive modulus.

Therefore, there appears to be no consensus in the published literature on the effect of height on CNT effective modulus.

Table 9: Comparison of measured CNT forest modulus values in literature using various methods

Reported Modulus Values	Experimental Details
Reduced modulus of 10-20 MPa [45]	Nanoindenter with CSM and a 100 µm diameter flat punch tip on free ends of vertically aligned CNTs. CNT heights ranged from 35-1200 µm. (Strain range ~0.0-0.7)
Reduced modulus of 2.6-3.3 MPa [10]	Nanoindenter with a 100 µm diameter flat punch tip on free ends of vertically aligned CNTs with a height of 600 µm. (Strain range ~0.0-0.22)
Nonlinear response: 1 MPa modulus for strains of 0.0-0.57, and 20.8 MPa for strains >0.57 [44]	Uniform compression test using an Instron® 5843 of 1000 µm tall CNT block between parallel plates. (Strain range ~0.0-0.65)
Nonlinear response: 0.3 MPa for strains 0.0-0.05, 1.6 MPa for strain 0.05-0.20, and 0.25 MPa for strains >0.20 [46]	Uniform compression test using MTS Nano Bionix® of 280 µm tall CNT block.
Reduced modulus of 14.7 MPa +/- 5.7 [52]	Nanoindenter with tip of 1 µm radius on free ends of vertically aligned CNTs.
Reduced modulus between 50-60 MPa with nonlinear behavior [48]	Nanoindenter with a Berkovich tip on vertically aligned CNT forests with bundle diameter of 200 µm and heights of 20-100 µm. Indent depths were <1 µm.
Reduced modulus of 12.7 MPa (strain range ~0.0-0.002) [47]	Nanoindenter with a 5 µm radius tip on free ends of vertically aligned CNTs with a height of 1200 µm transferred to a substrate.

Stress/Strain Loading Modulus vs. Unloading Modulus

Since the mechanical characterization of CNT turfs is a relatively new field, both the loading and unloading sections of the stress vs. strain curves were used to calculate

the effective compressive modulus for completeness. Traditional nanoindentation utilizes the unloading section of the compliance curve since it relies on the assumption of elastic-plastic loading and elastic unloading [126]. It is seen for all the cases of different CNT heights and end constraints that the modulus obtained from unloading curves was approximately 41.83% greater than the modulus obtained from the loading curves (Table 10). For example, the 61 µm tall CNTs using an adhesive to connect the CNT tips to the second substrate, the loading modulus was found to be 0.14 MPa while the unloading modulus was 0.23 MPa. This increase of modulus is explained by the shape of the stress vs. strain curves of Figure 59 and Figure 60. It is possible that during the loading process, the CNTs elastically compress and become more entangled. Then during the unloading of this displacement controlled test, the CNTs do not completely recover their initial height due to some unrecoverable and/or delayed recoverable deformation from entanglement of the CNTs. Therefore, the magnitude of the range of strain during unloading is lower than during loading and results in a greater elastic modulus. Additionally, subsequent indentations on the same sample provide similar stress vs. strain curves, and therefore it is possible that the recovery of CNT deformation at these strain ranges is time dependent to an extent.

Table 10: List of CNT forest effective modulus measure in this study for different CNT heights, with/without adhesive on the top substrate, and calculated from the loading or unloading section of the stress/strain curve.

	Average Effective Modulus (MPa)			
CNT Height (µm)	**No Adhesive & Loading**	**No Adhesive & Unloading**	**Adhesive & Loading**	**Adhesive & Unloading**
61	0.12	0.17	0.14	0.23
315	-	-	0.35	0.62
683	0.73	0.94	0.80	1.2

Effect of CNT End Constraint on Modulus

The stress vs. strain data collected during this study also allowed for the effect of the CNT tip constraint on the effective modulus to be analyzed. Uniform compression tests with the nanoindenter were performed with the 61 µm and 683 µm tall CNT turfs first without using an adhesive to attach the second substrate to the CNT tips (data listed in Table 10). Then CNTs of the same height were tested, but the substrate was coated with a SU8® (an epoxy based photoresist) to adhere the tips of the CNT turf to the substrate. It was seen that the end constraints affect the computed elastic modulus. In general, when an adhesive is used on the second substrate, the modulus of CNTs is 10-30% greater than the modulus of the CNTs without an adhesive on the second substrate. This increase in modulus is due to the fixed constraint of the CNTs when an adhesive is used on the tips compared to the sliding and/or rotating constrain of the CNTs when an adhesive is not used on the tips.

6.3 Nanoindenter Based Technique with Preloaded Test Specimens

The measured values for the effective modulus of the CNT forests obtained in the previous sections of this chapter were found to be relatively low, in the range of ~0.12-1.2 MPa. Due to these low values compared to a single CNT (~100 GPa [43] - ~4.15 TPa [8]), it was desired to investigate the effective modulus further to aid in exploring CNTs as off-chip interconnects. In literature, it has been observed that the effective modulus of CNT forests can increase as they are compressed [44, 46]. This is due to the low density of CNT forests (typically <10%) and their low stiffness, which allows them to easily compress and deform, and therefore leading to densification of the CNT forest. This densification, occurring at some strain value during compression, causes the forest to

stiffen due to the greater instantaneous density of the forest and increases the measured effective modulus. For this study it was desired to investigate if the effective modulus increases greatly at higher loads and strains for the CNT forest sandwich samples. But, the previous nanoindenter based methods of Section 6.2 are limited to a maximum load of ~1.5 N with the Hysitron high force head. Therefore to use the same size CNT sandwich sample of Section 6.2 it is necessary to develop a new technique to test the CNT forest at higher forces with the available equipment.

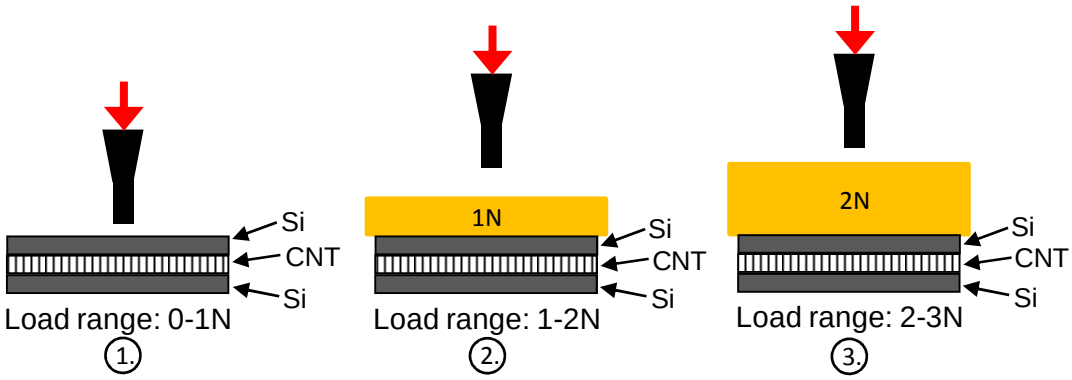


Figure 61: Illustration of three successive nanoindentation measurements using preloaded samples. Test 1 subjects the CNT forest to forces 0-1 N, Test 2 subjects CNTs to 1-2 N, and Test 3 subjects CNTs to 2-3 N.

In the nanoindenter tests of Section 6.2, the maximum strain the CNTs achieved during testing is limited by the maximum load that the Hysitron high force head is capable of (~1.5 N) applying. In order to test the mechanical response of the CNT forests at higher strains, the test samples were preloaded with small weights in stages to allow for greater total forces to be applied to the sandwiched test samples as illustrated in Figure 61. The samples used here, were of the same CNT sandwich construction as in Section 6.2 with adhesive attaching the top silicon substrate to the CNT tips. The CNTs used were 145 μm tall and were grown in an Aixtron Black Magic® thermal CVD system using a recipe similar to that presented later in Section 8.5.

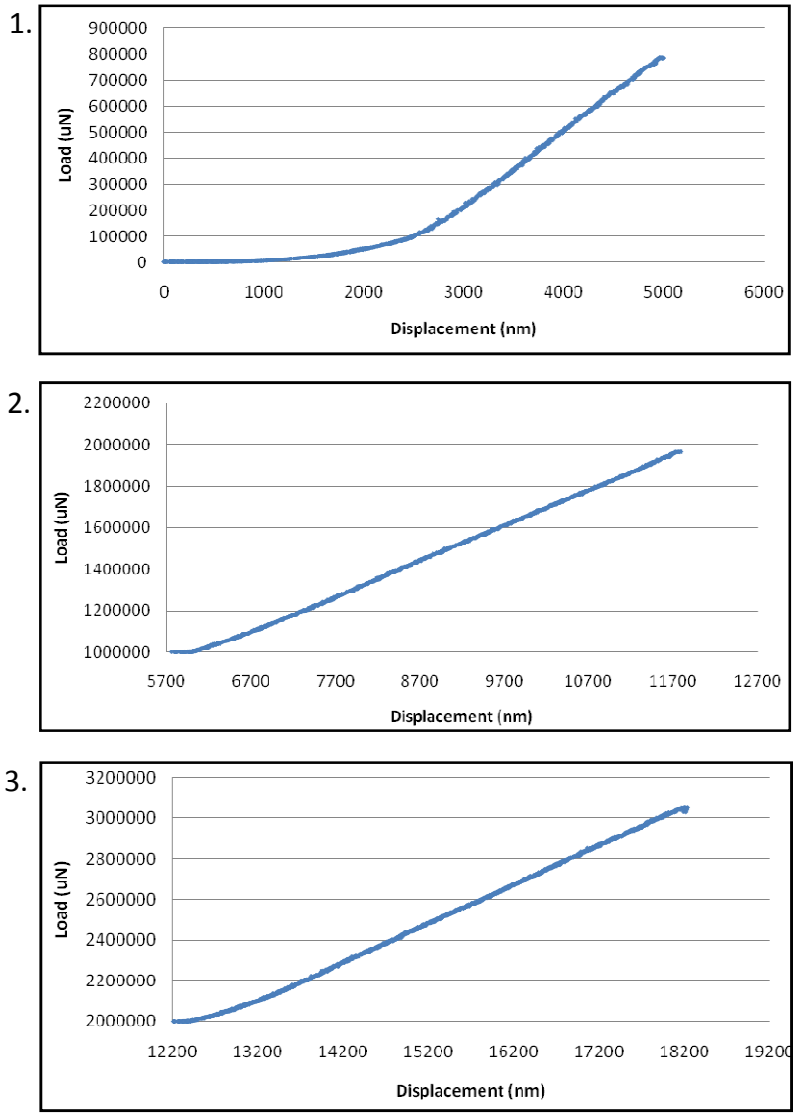


Figure 62: Compliance curves for three successive indentation measurements on CNT forests using 1.) forces of 0-1 N, 2.) forces of 1-2 N, and 3.) forces of 2-3 N.

To carry out these preloaded measurements illustrated in Figure 61, nanoindentation was first performed on the CNT sandwich sample without any preloads and with a loading and unloading rate of 700 nm/s. This measurement subjected the CNT forest to a force range of 0-1 N due solely to the nanoindenter force head. The resulting compliance curve of force vs. displacement for the loading section of the curve is shown in Graph 1 of Figure 62. Using the same methods as Section 6.2.3, the effective modulus

for this test was 0.39 MPa. Next, as illustrated in Figure 61, a small, flat, 1 N brass weight was fabricated and carefully placed on the CNT sandwich sample. Then the same nanoindentation process was performed on the sample. Contacting the nanoindenter tip with the top surface of the brass weight on the CNT sample effectively subjects the CNT forest to a higher force range of 1-2 N. The resulting compliance curve for this tested force range of 1-2 N is shown in Graph 2 of Figure 62, which yielded an effective modulus of 0.27 MPa. Finally, a third and final test was performed in the same manner as the second test, except a brass weight of 2 N was utilized. This third nanoindentation test subjected the CNT forest to a force range of 2-3 N. The force vs. displacement curve for this third test is shown in Graph 3 of Figure 62 and yielded a modulus of 0.31 MPa. From the results of these three tests of increasing forces and strains, it is seen that the effective modulus of the CNT forests is consistent, ranging from 0.27-0.39 MPa while being strained to a maximum of ~0.13. Also, during these tests the CNT forest did not stiffen as the forest was subjected to greater forces in this strain range, and the forest maintained a linear mechanical response during all three measurements. If the test was continued to even greater strains, the forest may become densified as in Figure 65 and result in a larger measured effective modulus. Though, for the forests here and for strains less than ~0.13, the modulus is consistent.

6.4 Semi-insitu SEM Based Technique

To support the findings obtained with the triboindenter based measurement techniques and to provide information on the nature of the deformation of the CNTs, a semi in-situ measurement method was developed using a scanning electron microscope. It was desired to confirm that in fact that the effective compressive modulus of the CNT

forests was on the order of 1 MPa since reported values for single CNTs are so much greater. This method is illustrated in Figure 63 and includes a compression fixture with a force load cell measuring device.

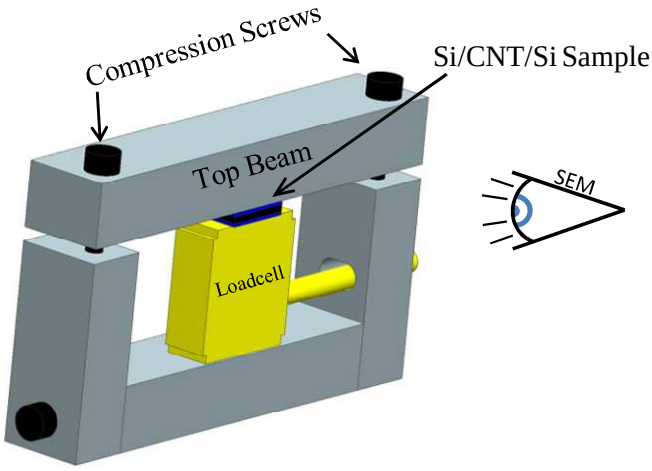


Figure 63: Drawing of the compression fixture used to apply compressive force to Si/CNT/Si sample to measure the effective compressive modulus. The fixture allowed a force to be applied to the sample, which would compress it, and then an SEM was used to measure the resulting change in height of the CNT forest.

The load cell used was a Futek® JR S-beam LSB200 with a max load of 10 pounds coupled with a Futek® USB210 data acquisition system. Additionally, engineering drawing of the custom compression fixture can be found in Appendix A.4.1. A similar Si/CNT/Si sandwich sample with no adhesive as was used in Section 6.2.1 was used with this measurement approach, and placed in between the load cell and the top beam of the fixture. The compression screws on the top beam were tightened to apply, and hold, a compressive force to the CNTs. To measure the effective compressive modulus using this technique, the procedure outlined below was followed:

1. Use SEM to measure the initial height of CNTs with no load applied.
2. Outside of SEM chamber, insert CNT sandwich sample into the compression fixture, apply load by tightening compression screws, record force from load cell.

3. Electrically disconnect load cell from data acquisition and place in SEM chamber.
4. Use SEM to measure new compressed height of CNTs.
5. Remove compression fixture with CNT sample from SEM.
6. Connect load cell to data acquisition system, use compression screws to increase force on CNTs, and repeat the procedure to measure CNT height using SEM.
7. Repeat this process for several more steps with increasing force to obtain relationship of force vs. displacement and thus, effective stress vs. strain.

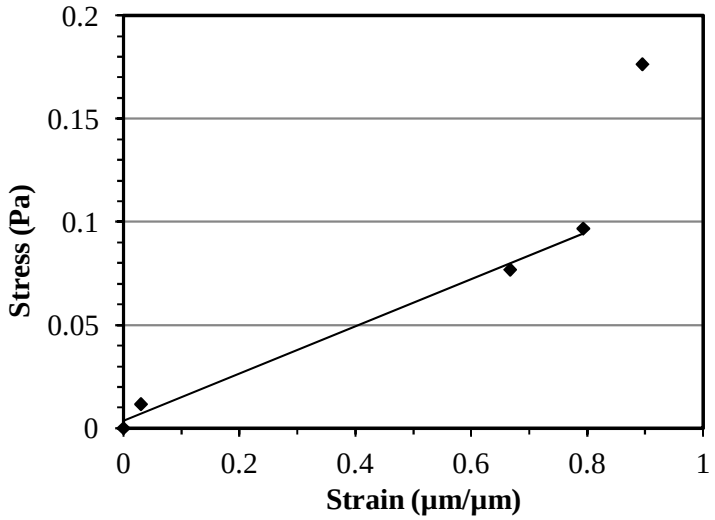


Figure 64: Stress vs. strain data of CNT sample with initial height of ~133µm obtained using Si/CNT/Si sandwich in compression fixture with SEM. The effective compressive modulus for this height of CNTs was measured to be 0.11 MPa using this measurement method.

6.4.1 Effective Compressive Modulus by SEM with Compressive Fixture: Results and Discussion

Each of the measurements at a specific force and resulting change in height of the CNTs with the SEM compressive fixture allowed for similar calculations of effective stress and strain as performed with the triboindenter-based measurements of Section 6.2.3. This test method was performed with a CNT forest 133 µm in height and the resulting effective stress vs. strain plot is shown in Figure 64 and shows the measured

effective compressive modulus to be 0.11 MPa. Additionally, the resulting SEM images of the CNT forest at each distinct load step during the experimental procedure are presented in Figure 65. This effective compressive modulus measured with the SEM-based method is comparable to the modulus values obtained with the triboindenter-based methods and therefore provides support for those measurements. Additionally, the stress vs. strain curve shows a steep increase for the last load step at a strain of ~0.8. This is most likely due to densification of the CNTs after they have completely collapsed. This densified structure was captured with the SEM and shown in Figure 65E. Similar large increases in stiffness have been reported at large strains by Maschmann et al. [10, 45], Suhr et al. [44] and Hutchens et al. [123]. Also this densification and increase in modulus occurs at a larger strain than tested with the preloaded samples of Section 6.3, and therefore support the measurements of that section of this chapter.

In addition to stress vs. strain data, the SEM images of the CNTs under compressive loading provide insight on the nature of the CNT forest deformation. First, it is seen that the folding initially occurs near the growth surface of the silicon substrate (Figure 65B). This is believed to occur because the CNTs are more constrained at that location since they are attached to the growth substrate. The tips of the CNTs are in contact with the top silicon substrate, but have the ability to slide and rotate since no adhesive was used in this SEM based experimental approach. Additionally, others have reported that buckling initially occurs near the growth substrate since CNT density and alignment are lower at this location [10, 52, 123]. Agreement on the location of subsequent buckling is not as clear and appears to be dependent on the CNT samples and test method. Zbib et al. and Hutchens et al. used a flat punch tip on CNT turf columns of

smaller diameter than the punch tip and observed all buckling to occur near the roots [52, 123]. Conversely, Maschmann et al. used a flat punch on a CNT turf much larger than the tip and observed initial buckling at the root and subsequent buckling near the tips [10, 45]. While Qiu et al. observed buckling both on the root side and tip side depending on the CNT turf configuration/attachment with the rigid substrate during uniform compression [48]. Although the initial folding occurred near the growth substrate, the subsequent folding was not distinctively at the top or bottom region of the CNT turf. Also, the SEM images of the CNTs in the compression fixture show that there is a large amount of unrecovered strain of the CNT turf after the load is removed from the final load step. Figure 65F shows the CNT turf after the test with no load and a final height of ~20.7 µm, which results in ~84.4% unrecovered strain. The presence of unrecovered strain during this SEM-based method provides some support for the explanation given for the differences in the loading and unloading sections of the stress vs. strain curves obtained with the nanoindentation-based method in Section 6.2.3. Additionally, it should be noted that from these SEM images, the deformation of the CNTs is not distributed throughout the total length of the CNTs, like what would happen with a traditional spring in compression. The CNTs demonstrate a deformation that is similar to local folding in nature, as shown by Figure 65C. This type of folding provides the large deformations under compressive loads, which then results in the low effective compressive modulus of the CNT forests. Also, the low modulus of CNT forests under compression has been attributed to buckling [10, 52, 123], bending [129, 130], low volume density [131, 132], CNT defects [133], etc. and in addition to these, the low modulus can be attributed to the inherent waviness of the CNT structures [130].

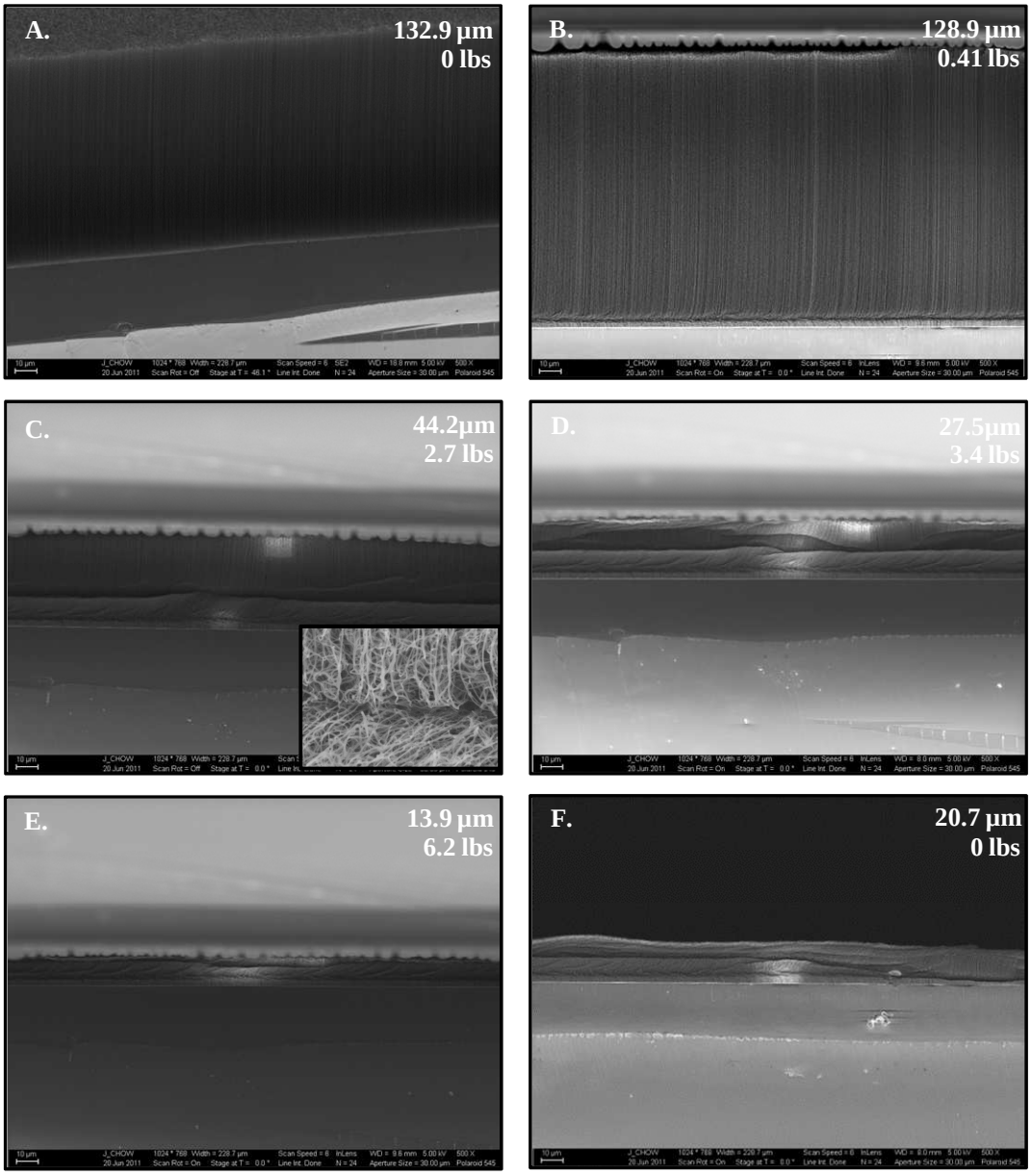


Figure 65: (A.-E.) SEM image of entire height of CNT forest while being compressed with Si substrate at the top and Si growth substrate at the bottom. Folding of the CNT structure is observed near the bottom growth substrate. Image (B.) shows initial folding occurring near growth substrate. Higher magnification SEM image of CNT folding shown in inset of (C.). Unrecovered strain of CNT turf is shown in (F.) with load removed.

6.5 Tensile Tester Based Measurement

The fourth experimental measurement of the effective mechanical properties of the CNT forest was based on more traditional tensile testing methods using a Test Resources® 100P225 Tensile Tester. This used similar sandwiched CNT forests as in the

previous sections in this chapter between silicon substrates and is illustrated in Figure 66 along with tensile data of a CNT forest with a height of ~695 µm and sample area of 108 mm^2. This yielded an effective modulus of ~0.84 MPa which is comparable to the nanoindenter based values and also 4-6 orders of magnitude less than reported values for an individual CNT. The stress vs. strain curve in Figure 66 shows a linear response through the entire tensile test, and this indicates that there is no debonding of the interfaces during the test. Also, by dispensing an adequate amount of adhesive evenly on the silicon substrate, it was ensured that all of the CNTs were attached to the top substrate. Furthermore, the modulus of the adhesive is 2 GPa [134] and that of the silicon substrate is ~169 GPa [135] which are several orders of magnitude higher than that of the CNT forest, and thus, the observed deformation is that of the CNTs.

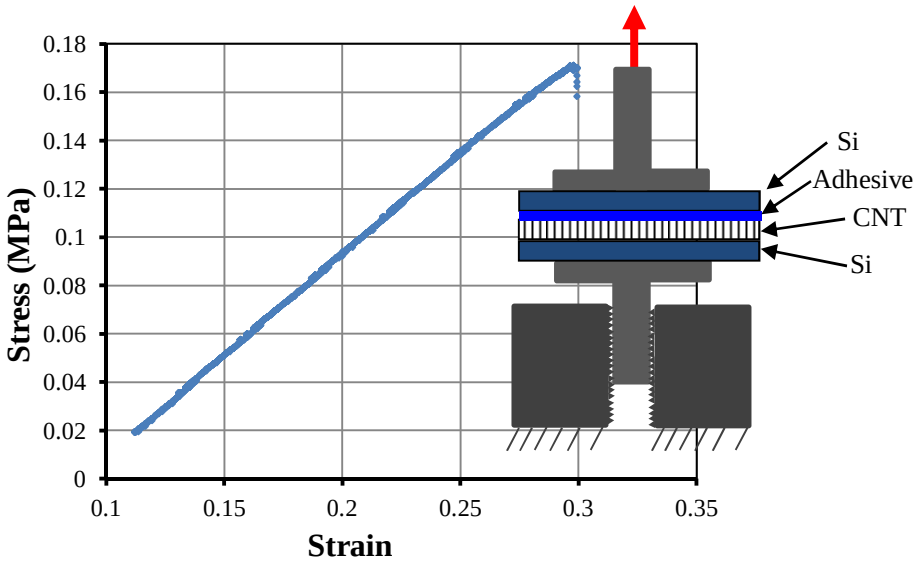


Figure 66: Illustration of configuration of Si/CNT/Si sandwich test sample used in tensile test and also stress vs. strain data of tensile test for a sample with a CNT height of 695 µm.

6.6 Conclusion/Summary

In this chapter the effective mechanical properties of carbon nanotubes were experimentally measured using four different methods. These four methods were used to

measure the effective modulus of CNT forests, where all the vertically aligned CNTs deformed in unison acting as a single foam-like material. The four measurement techniques developed and utilized here included 1) a nanoindenter based method, 2) a nanoindenter based method using preloaded samples, 3) a semi-insitu method coupled with an SEM, 4) and a tensile tester based measurement. All the measurements obtained using these different techniques were relatively close and ranged from ~0.11-1.2 MPa, depending on the CNT forest height, CNT tip constraint condition, strain range, and direction of applied force. The nanoindentation based method developed in this chapter, compressed the CNT forest between two rigid silicon substrates by using the nanoindenter to contact and apply a force to the top rigid substrate. This is the first investigation using a nanoindenter with a sample between rigid substrates to avoid issues concerning the contact area function between CNT forest tips and the indenter tip. This is an improvement on past methods focused on the using a nanoindenter to measure the effective properties for CNT forest as a whole.

Furthermore, to use this nanoindenter based method with sandwiched CNT samples to test higher strain ranges, a method using preloaded samples was also developed. This technique placed weights on the top rigid substrate of the CNT sandwich. The nanoindenter tip was then used to contact the top surface of the weight and compress the CNT forest. This approach allowed the CNT forest to be subjected to, and tested over a larger range of forces and strains than just the standard nanoindenter is capable of. The nanoindenter measurements with preloaded CNT sandwich samples showed that these CNT samples exhibit a linear mechanical response up to the maximum strain tested (~0.13) with these nanoindenter based methods. Additionally, the CNT

forests were tested using more traditional methods such as a microscale tensile tester. Similar samples of a CNT forest between rigid substrates was pulled in tension and yielded a similar modulus of ~0.84 MPa. To support these low modulus and highly compliant mechanical property measurements from these three different methods, a semi-insitu SEM based technique was developed. This allowed for force vs. displacement measurements of the CNT forests while observing the nature of the deformation with an SEM. This method yielded a similar low modulus of ~0.11 MPa for the CNT forest and also demonstrated a large increase in modulus at high strains due to CNT forest densification. The local buckling and folding of the CNT forest as it was compressed was also observed with the SEM to confirm and validate these effective modulus values being several orders of magnitude less than that of a single CNT in tension.

In summary, several measurement techniques were developed and used in this chapter to measure the effective modulus of CNT forests. The values measured for the effective modulus were in the range of 0.11-1.2 MPa and are several orders of magnitudes less than that of a single CNT in tension. These measurements show that CNT forests possess a very low effective modulus and therefore offer potential mechanical performance benefits as CNT based off-chip interconnects. Lastly, the measurements obtained in this chapter add to and extend the existing body of data in literature and will serve as the basis of the material property model for CNT based off-chip interconnects in finite-element analysis conducted on electronic packages utilizing CNT based interconnects that are presented in a later chapter of this thesis.

CHAPTER 7

FINITE-ELEMENT MODELING OF ELECTRONIC PACKAGE WITH CNT OFF-CHIP INTERCONNECTS

7.1 Introduction

Chapter 6 of this thesis measured effective mechanical properties of CNT forests, and showed that the measured values of effective modulus are in the range of 0.12-1.2 MPa. These values are very low compared to a single CNT and also to traditional interconnect materials such as solder (34 GPa for SAC305 solder [136]) or even less commonly used electrically conductive adhesives (~250-3500 MPa [137, 138]). In this chapter, the values of effective modulus that were measured previously in this thesis will be used in finite-element models of electronic packages to demonstrate the mechanical performance benefits of CNT based off-chip interconnects and its potential to help mitigate fracture of low-k dielectric layers. This will be demonstrated with 3D finite-element models of dummy silicon flip chip packages attached to FR4 substrates with a peripheral interconnect configuration. This package will be modeled along with a traditional package utilizing solder ball interconnects and underfill to provide a comparison of the mechanical performance of the CNT interconnect scenario. In these comparisons, stresses in the silicon chip, stresses in the interconnects, and warpage will be discussed. In addition to general mechanical performance comparisons with traditional packages, variables such as the modulus, orthotropic vs. isotropic properties CNT properties, and interconnect height will be varied to investigate their effect on the mechanical performance of the electronic package utilizing CNT off-chip interconnects to provide guidance and a better understanding for their future potential use.

7.2 3D Finite-Element Model

In this section a 3D model of a silicon die attached to a FR4 substrate was modeled. This was done using ANSYS® V14 and was represented with quarter symmetry of the full model geometry in order to reduce the total amount of elements while providing all of the desired results. The main goal of this analysis was to demonstrate that lower die stresses of an assembled flip chip package can be achieved by utilizing CNT based interconnects compared to traditional solder ball interconnects. The lower die stresses would imply that on-chip low-k dielectric material will experience lower stresses, and thus, will not crack or delaminate.

7.2.1 3D Model Geometry

The geometry of the finite-element model is based on the commercially available mechanical dummy flip chip of model number PB08-400x400-DC-LF2 obtained from Practical Components Inc. This chip was chosen since it has dimensions relevant to current commercially available microelectronic devices. The modeled chip has pad diameters of 105 µm, a pitch of 203 µm, and an overall full geometry size of 8.12 x 8.12 mm, with a total of 40 interconnects per side in a peripheral arrangement. The remaining geometric dimensions of the model are listed in Table 11 and illustrated in Figure 67 and Figure 68.

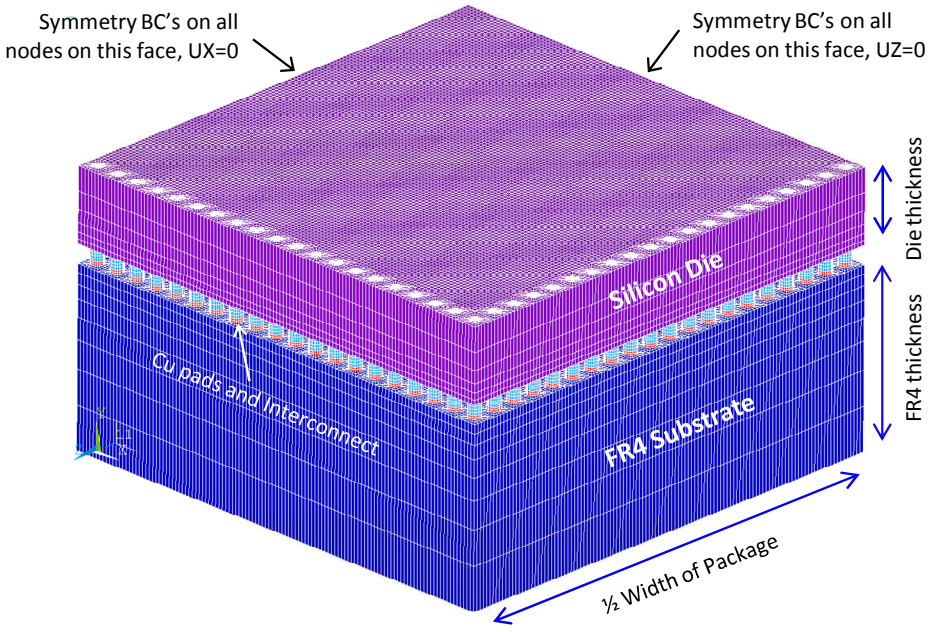


Figure 67: Illustration of finite-element model of flip chip on FR4 substrate connected with interconnects. Only a quarter of the model is shown, due to quarter symmetry of the model. The illustration is from the Ansys® model and includes labels of the various materials.

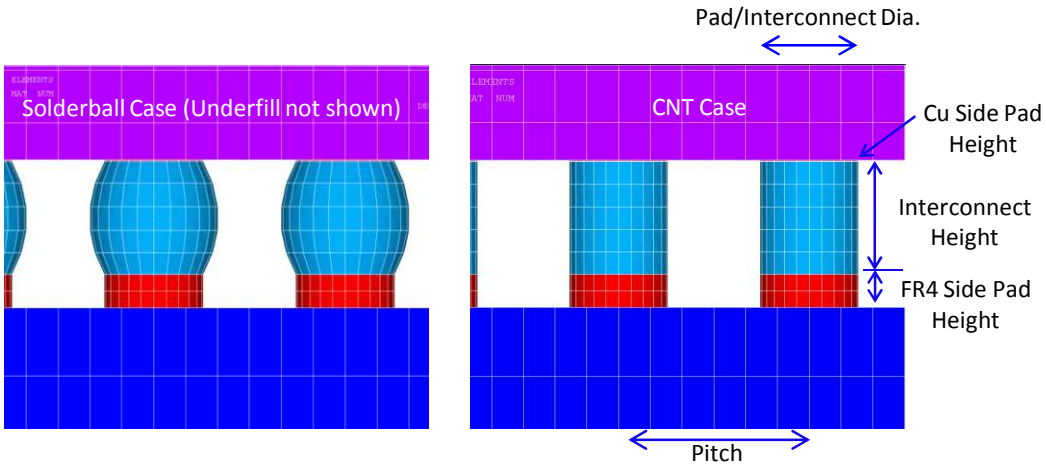


Figure 68: Zoomed in side view of Figure 67 showing the copper pads on the FR4 board side and thinner die-side copper pads. The left illustration depicts the traditional solder ball case and the right illustration depicts the CNT case. Additionally, important geometric parameters are labeled.

Table 11: Dimensions used for finite-element model of electronic package in Section 7.2.1

Geometric Parameter	Dimension (μm)
Pitch	203
Pad Diameter	105
FR4 Thickness	1500
Die Thickness	625
Interconnect Height	120
FR4 side Cu Thickness	35
Die side Cu Thickness	1.7

7.2.2 3D Model Material Properties

Material properties used in this analysis were traditional properties used in literature of finite-element simulations of electronic packages. The FR4 substrate was modeled as orthotropic temperature dependent (Table 12) [139], silicon as temperature independent isotropic (Table 13) [139], copper as temperature independent isotropic (Table 14) [140], underfill as temperature dependent isotropic (only used for the solder ball case) (Table 15) [136], SAC305 lead free solder as a temperature dependent viscoplastic isotropic material (Table 17) [136], and the CNT interconnect as a temperature independent isotropic material (Table 18). For the solder, the Anand's viscoplastic model was chosen with coefficients as listed in Table 17 [136]. Also, since a thermomechanical analysis is being performed, it is crucial to define the stress free state of the materials. The stress free state of the solder is assumed to be its reflow (melting) temperature of 220^{o}C, while for the rest of the materials in the model the transition temperature of the underfill (160^{o}C) was used. These stress free temperatures are similar to those found in literature performing similar analyses of traditional electronic packages

[136]. Additionally, the material properties for the CNTs for this first analysis are isotropic with and elastic modulus of 1 MPa and listed in Table 18, which is within the range measured in this thesis in Section 6.2.3. In a later section of this chapter, the value for the CNT modulus in the finite-element model will be varied and a transversely isotropic material model will be utilized to investigate the effect on the die stresses. Additionally, the value for the Poisson's ratio used, if not stated otherwise, is 0.35 as measured by Maschmann et al [141].

Table 12: Temperature dependent orthotropic mechanical properties for FR4 substrate used in finite-element model [139]

	Temperature (^{o}C)					
Property	**30**	**95**	**110**	**125**	**150**	**270**
E_{xx} (MPa)	22400	20680	19970	19300	17920	16000
E_{yy} (MPa)	1600	1200	1100	1000	600	450
E_{zz} (MPa)	22400	20680	19970	19300	17920	16000
G_{xz} (MPa)	630	600	550	500	450	441
G_{xy} (MPa)	199	189	173	157	142	139.3
G_{yz} (MPa)	199	189	173	157	142	139.3
ν_{xz}	0.136	0.136	0.136	0.136	0.136	0.136
ν_{xy}	0.1425	0.1425	0.1425	0.1425	0.1425	0.1425
ν_{yz}	0.136	0.136	0.136	0.136	0.136	0.136
CTE_{xx}	20e-6	20e-6	20e-6	20e-6	20e-6	20e-6
CTE_{yy}	86.5e-6	86.5e-6	243e-6	400e-6	400e-6	400e-6
CTE_{zz}	20e-6	20e-6	20e-6	20e-6	20e-6	20e-6

Table 13: Temperature independent isotropic properties of silicon die [139]

Property	Value
E (MPa)	160000
ν	0.34
CTE	2.6e-6

Table 14: Temperature independent isotropic properties of copper [140]

Property	Value
E (MPa)	121000
ν	0.3
CTE	17.3e-6

Table 15: Temperature dependent isotropic properties of underfill [136]

Property	Value
E (MPa)	7600
ν	0.3
CTE	28e-6 (Temp. $\leq 150^{o}$C) 104e-6 (Temp. $\geq 170^{o}$C)

Table 16: Temperature dependent isotropic properties of SAC305 solder [136]

Property	Value
E (MPa)	**387000-176*T**
ν	**0.35**
CTE	**25e-6**

Table 17: Anand model constants for SAC305 [136]

Symbol	Value	Units
A	17.994	1/s
Q/R	9970	K
ξ	0.35	-
m	0.153	-
s	2.536	MPa
n	0.028	-
h_0	1525.98	MPa
α	1.69	-
S_0	2.15	MPa

Table 18: Isotropic properties for CNTs used in finite-element simulations of electronic package

Property	Value
E (MPa)	1 MPa
ν	0.35 [141]
CTE	--

7.2.3 3D Finite-Element Model Analysis

In order to determine the stresses in the silicon die due to CTE mismatch, it was decided to perform a single cool down step from 160^{o}C to 25^{o}C (room temperature). This temperature was chosen since it is the last thermal assembly step for a flip chip with a solder ball and underfill configuration. The temperature of 160^{o}C is the cure temperature for a typical underfill [136]. This same analysis was performed for the CNT interconnect scenario even though the model does not include underfill. This same

temperature of 160°C was used to provide a more direct comparison of mechanical performance for the two interconnect scenarios.

7.2.4 Finite-Element Analysis Results – CNT Interconnect vs. Solder Ball

The first scenario solved in this investigation was the flip chip with CNT interconnects utilizing an isotropic modulus of 1 MPa and a Poisson's ratio of 0.35 (Table 18) cooled from 160°C to 25°C (room temp). This was compared to the scenario with traditional solder interconnects and underfill undergoing the same finite-element analysis. The stresses in only the silicon die were determined and are presented in Table 19. It can be seen that all of the stresses are greatly reduced in the case of the flip chip with CNT off-chip interconnects, with the percent changes ranging from ~94-71% for all the stresses. Two important stress components of this analysis are σ_{xx}, which is a major cause of cohesive failure, and σ_{yy}, which is a major cause for interfacial fracture in BEOL low-k layers. In addition to greatly reducing the stress magnitudes in the silicon die, the regions of the silicon die that are experiencing elevated stress levels are also decreased by the use of CNT interconnects. For example, the maximum σ_{xx} stress for the solder ball scenario occurs in most of the planar area of the chip, as shown by the large amount of red contours in Figure 69a and Figure 69b. Compare this to the CNT interconnect scenario, Figure 69c and Figure 69d, which only has the elevated σ_{xx} stresses occurring in regions near the interconnects and copper pads. Therefore, the CNT off-chip interconnects not only reduce stresses in the chip greatly, but also these elevated stress values occur in much less of a volume of the chip.

Additionally, an analysis was performed on a stand-alone silicon chip with copper pads and then cooled similarly from 160^{o}C to 25^{o}C. This silicon chip showed similar die stresses as the scenario of the silicon chip assembled to the FR4 substrate with CNT interconnects (listed in Table 19). This means that the stresses for the CNT interconnect scenario are due mostly to the CTE mismatch between the silicon die and the copper pads, and not due to the CTE mismatch from the FR4 substrate. Therefore the CNT interconnects are able to completely decouple the silicon die from the board, resulting in no additional assembly-induced stresses.

Table 19: Comparing finite-element analysis of die stresses for solder ball vs. CNT interconnect scenarios.

	Stress Type (MPa)			
Interconnect Scenario	σ_{xx}	σ_{yy}	σ_{xz}	σ_{yz}
a) Solder balls with underfill	58.118	36.979	18.157	78.469
b) CNT interconnect	9.3482	2.3979	5.2836	5.2836
c) Stand-alone chip with Cu pads	9.3582	2.3920	4.3919	5.2694
Percent change between scenarios a) and b)	83.92%	93.52%	70.90%	93.27%

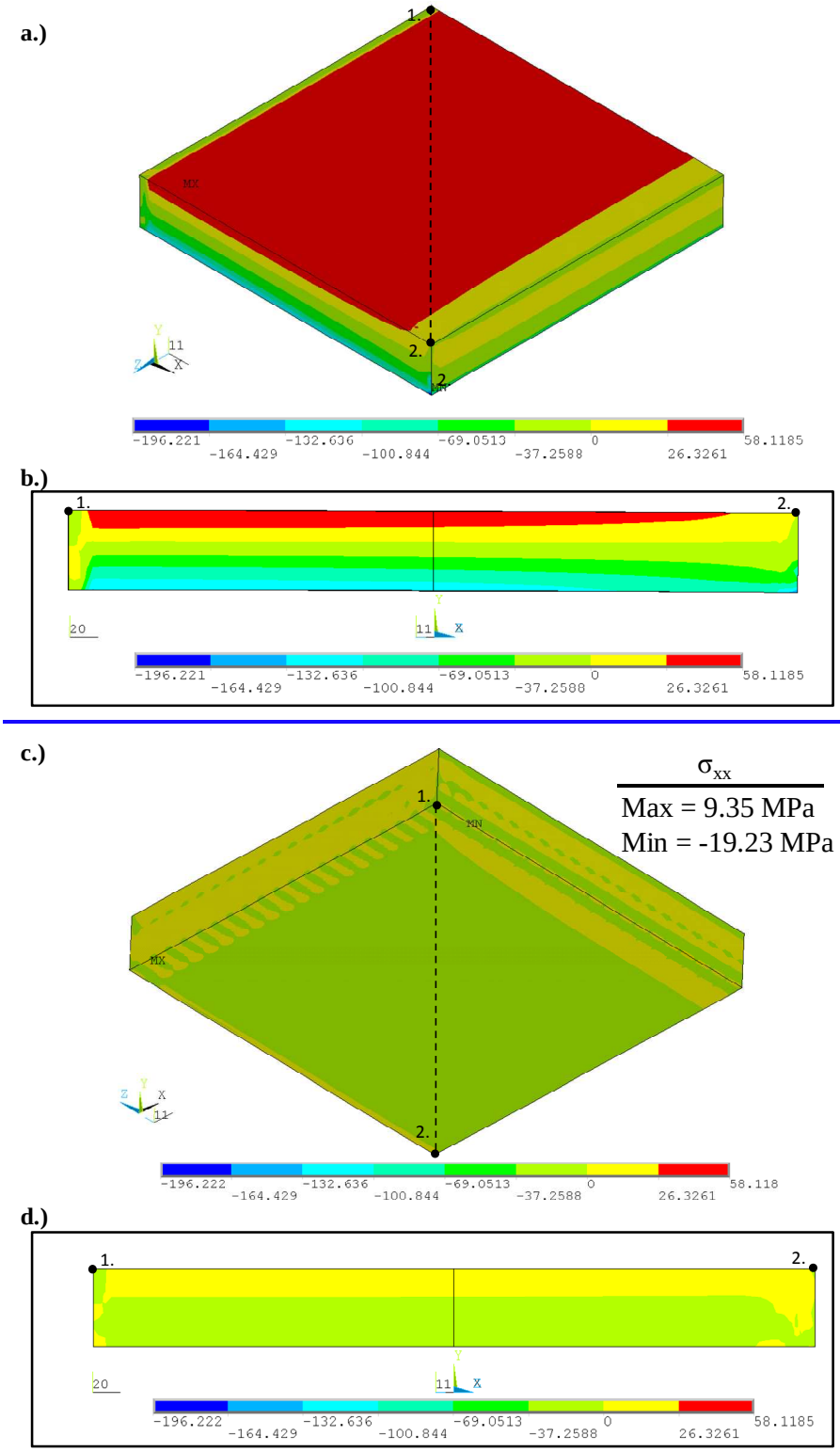
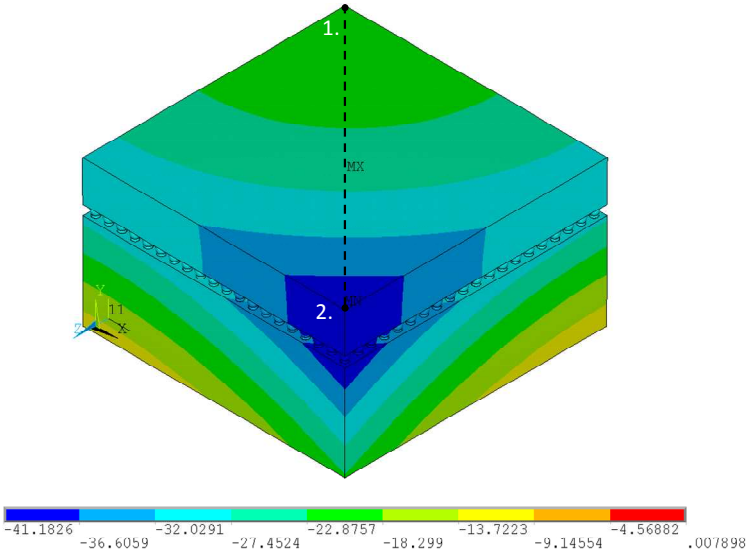


Figure 69: Contour plot of σ_{xx} stress (MPa) in only silicon die of two scenarios a.) Solder ball and underfill case from angled top view. b.) Internal view of stress contour at cross section of silicon die marked by line 1-2 in a) of this figure. c.) CNT interconnect case from angled bottom view. d.) Internal view of stress contour at cross section of silicon die marked by line 1-2 in c) of this figure.

To further illustrate that the CNT interconnects mechanically decouple the silicon die from the FR4 substrate, the warpage of the silicon die is investigated for the two different scenarios. Here, the warpage is calculated from the difference in out of plane displacement (y-direction of Figure 70 and Figure 71) between points 1 and 2. Since all of the materials in the model deform in the y-direction due to both warpage and the component of CTE in the y-direction, it is necessary to use the difference between diagonal corners of the die to quantify the warping/bending shape of the die when cooled. An internal cross sectional view of the displacement contours along the diagonal plane of the silicon die of Figure 69 is given in figure 70. Table 20 lists the warpage of the two different interconnect scenarios calculated from these figures. For the traditional solder ball scenario the warpage of the die is 21.82 μm and then by utilizing the CNT interconnects, the warpage is essentially eliminated with a warpage of 0.008 μm. To further visually illustrate that the use of CNT interconnects mechanically decouples the silicon die from the substrate, the y-displacement contours of the total model is shown in Figure 70 for both of the interconnect scenarios. In the solder interconnects scenario, the displacements of the die and board are similar, as shown by the similar displacement contours of the die and board of Figure 70a. Conversely, in the scenario of the CNT interconnect in Figure 70b, the displacement contours of the substrate and the die are different and therefore deforming independently and mechanically decoupled.

a.)



b.)

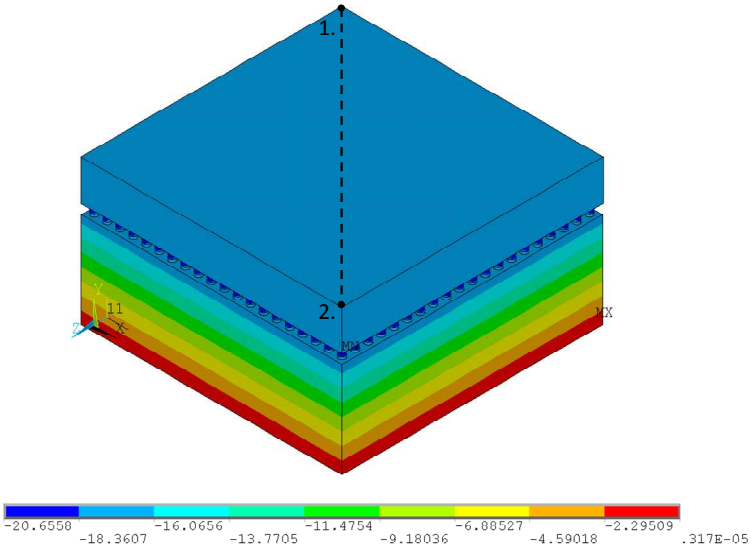


Figure 70: Contour plot of y-displacement of entire finite-element models of two scenarios a.) Solder ball and underfill case (underfill not shown) b.) CNT interconnect case.

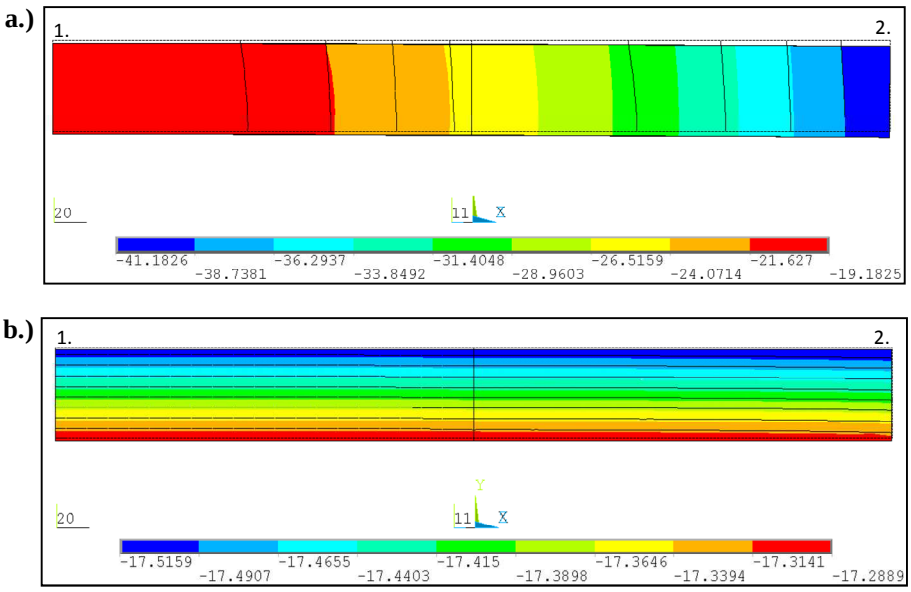


Figure 71: a.) Plot of y-displacement of only chip, internal view of diagonal plane of line 1-2 for solder ball case of Figure 70a. b.) Plot of y-displacement of only chip, internal view of diagonal plane of line 1-2 for CNT case of Figure 70b.

Table 20: Silicon die warpage for two interconnect type scenarios

Interconnect Scenario	Silicon Die Warpage (μm)
Solder balls with Underfill	21.82
CNT interconnect	0.008

7.2.5 Finite-Element Analysis Results – CNT Modulus

The effective modulus of CNT forests used in this thesis was measured to have a modulus ranging from 0.12-1.2 MPa, but literature contains studies with measured values as large as 275 MPa [141]. These differing values of effective modulus are a subject of ongoing research in literature and have been shown to be effected by differences in parameters such as CNT waviness, density, and diameter [130, 132] . Since a wide range of modulus values for CNT forests is possible, it was desired to investigate the effect that this has on the die stresses if used in an electronic package to provide insight for future implementation. In this study the same analysis as in Section 7.2.4 was performed where

the package was cooled from 160°C to 25°C, and the modulus was varied from 0.1 MPa to 500 MPa with a constant Poisson's ratio of 0.35. The die stresses from these scenarios of different modulus values are shown in Table 21. These values show that for CNT interconnects with a Young's modulus within the range of 0.1-100 MPa, that there is very little effect on all of the components of stress in the die. However, the greatest CNT modulus of 500 MPa creates an increase in die stresses when compared to the lower modulus values. But, even though the chip stresses increase by using the greater CNT modulus of 500 MPa, all the values are still much less than the traditional solder ball and underfill scenario. Specifically, this CNT interconnect scenario with a Young's modulus of 500 MPa has σ_{xx} and σ_{yy} stress values that are 80.14% and 61.49% less than the solder ball scenario respectively. This illustrates that during implementation of CNTs of off-chip interconnects, it is not critical to control the CNT modulus during synthesis to achieve large improvements in mechanical reliability.

Table 21: Comparing finite-element analysis of die stresses for CNT interconnect scenarios of various modulus

	Stress Type (MPa)			
CNT Interconnect Modulus (MPa)	**σ_{xx}**	**σ_{yy}**	**σ_{xz}**	**σ_{yz}**
0.1	9.3572	2.3926	4.383	5.2708
1.0	9.3482	2.39793	4.3925	5.28364
10	9.3097	2.4509	4.4871	5.4157
100	9.7326	3.4454	5.3769	6.7193
500	11.544	14.242	8.3958	12.521

Table 22: Comparing finite-element analysis of interconnect stresses for CNT interconnect scenarios of various moduli

	Stress Type (MPa)		
CNT Interconnect Modulus (MPa)	σ_{xx}	σ_{yy}	σ_{xz}
0.1	0.0024510	2.3926	0.00074136
1.0	0.0245	0.0093884	0.0074060
10	0.24456	0.093863	0.073269
100	2.3865	0.93654	0.66351
500	10.552	40.523	2.7372
Solder ball interconnect with Underfill	80.575	58.611	2.4423

In addition to investigating die stresses resulting from varying the CNT modulus, the stress in the CNT material was also calculated (Table 22). It was found that stresses increase significantly as the CNT modulus is increased, but like the die stresses, they are still relatively low with values of 10.56 MPa for σ_{xx} and 40.52 MPa for σ_{yy} for the worst scenario tested of a CNT modulus of 500 MPa. These are low stresses for CNTs, which have been shown to have strengths of 11-150 GPa [9, 70] and therefore should not be a great concern.

7.2.6 Finite-Element Analysis Results – CNT Height

Another variable of interest when investigating CNT forests as off-chip interconnects is the height of the forest. In this section, the effect of the CNT height on the die stresses was studied by using CNT heights of 30, 60, 120, and 240 µm in a similar analysis as in previous sections of this chapter. In this analysis a modulus of 1 MPa and a Poisson's ratio of 0.35 was used and the package was cooled from 160°C to 25°C. From

this, it was found that the value of CNT height within the tested height range and with a modulus of 1 MPa had virtually no effect on the die stresses. The values for the components of die stresses calculate from these simulations are listed in Table 23. There was an effect though on the CNT interconnect stress as illustrated in Figure 72 where the σ_{xx} and σ_{yy} stresses decrease with increasing CNT interconnect height. Still, in all of the heights simulated, the stresses in the interconnects are extremely low compared to the stresses in a traditional solder ball of similar height.

Table 23: Comparing finite-element analysis of die stresses for CNT interconnect scenarios of various heights

	Stress Type (MPa)			
CNT Interconnect Height (µm)	**σ_{xx}**	**σ_{yy}**	**σ_{xz}**	**σ_{yz}**
20	9.3194	2.4158	9.2996	4.4419
60	9.3364	2.4043	9.3065	4.4085
120	9.3482	2.3979	9.3139	4.3925
240	9.3549	2.3942	9.3190	4.3847

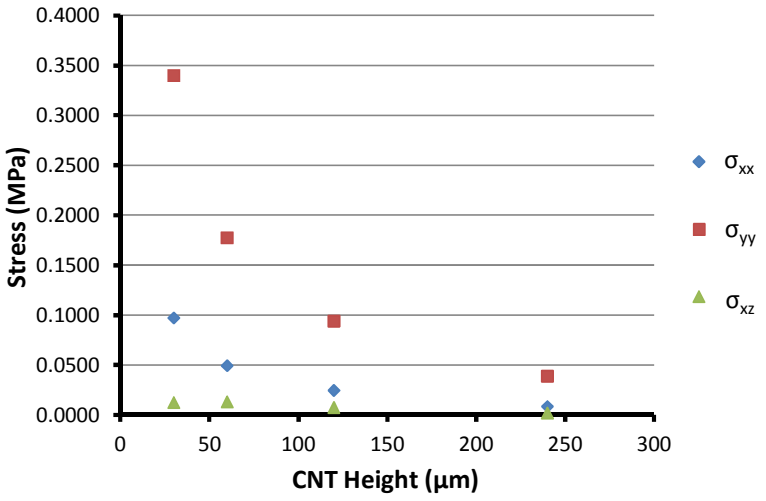


Figure 72: Interconnect stress values of σ_{xx}, σ_{yy}, and σ_{xz} as a function of CNT height.

7.2.7 Finite-Element Analysis Results – Transversely Isotropic Material Model

In the previous sections of this chapter the finite-element analysis of a flip chip package utilizing CNT forests as off-chip interconnects was studied. In these analyses, the CNT forest was modeled as a fully isotropic material using the modulus measured by nanoindenting the CNTs in the direction of growth as the modulus for all directions. But it is known that the structure of the CNT forest varies with direction. The material structure resembles that of a transversely isotropic material, which is a special case of orthotropy and is defined by a material having the same properties in one plane and different properties in the direction normal to that plane. For this study, the CNT forest has the same properties in the X-Z plane of Figure 73, and therefore $E_x=E_z$, but with different properties in the direction of the CNT growth (Y-direction) and therefore, E_y. To fully define this material model, five independent elastic constants are needed, which are E_y, $E_x=E_z$, ν_{yx}, ν_{xz}, and $G_{xy}= G_{yz}$. The properties that are in the X-Z plane of isotropy are $E_x=E_z$ and $\nu_{xz}= \nu_{zx}$. While the properties that are out of plane of isotropy are E_y and ν_{yx}. The other properties, G_{xz} and ν_{xy}, that are needed to implement this as an orthotropic property in Ansys® can then be calculated from the previous five independent constants and using the following relationships for a transversely isotropic material:

$$G_{xz} = \frac{E_x}{2(1+\nu_{xz})} \tag{20}$$

$$\frac{\nu_{yx}}{E_y} = \frac{\nu_{xy}}{E_x} \tag{21}$$

$$E_x = E_z \tag{22}$$

In addition to these three relationships (Equations 20 - 22), this discussion regarding the CNT material model is completed in detail in Appendix A.5 to aid in the calculations of the property components in the following paragraphs.

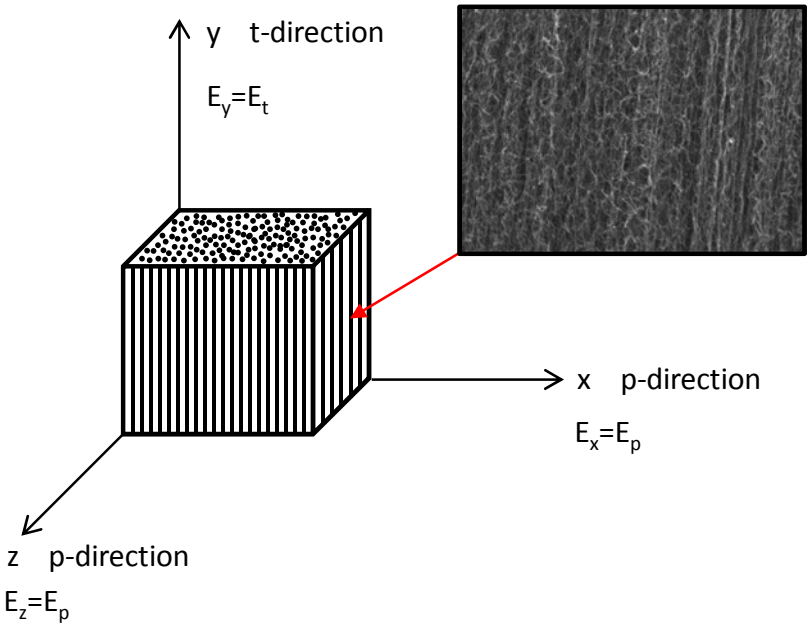


Figure 73: Diagram of orientation of CNT forest for off-chip interconnects for the transversely isotropic material model implemented in finite-element analysis. CNT growth direction is in the Y-direction.

In this section it will be studied whether using this transversely isotropic model for the CNTs will have an effect on the finite-element analysis of the flip chip package compared to the isotropic material model. It will be determined if it is necessary to measure all five of the independent variables to implement the CNT material as a transversely isotropic material or if it is sufficient to model the CNT interconnect as a fully isotropic material for purposes of mechanical reliability studies. To investigate this, first a case using all of the transversely isotropic properties obtained by Maschmann et al [141] will be implemented in the finite-element model, and then a second case will be

tested based Maschmann et al's values while incorporating the modulus in the direction of CNT growth that was measured in this thesis in Section 6.2.3.

In the first case of transversely isotropic CNT properties, all of the properties were obtained from Maschmann et al [141] and by using Equations 20 - 22 and Equations 27 - 31 (Appendix A.5), with specifically calculating G_{xz} from Equation 20 and ν_{xy} from Equation 21. These values are listed in Table 24 and were implemented in Ansys® as an orthotropic material. Along with this initial case, a second case using a Young's modulus value of $E_y = 1$ MPa that is within the range of the values measured from this thesis was used along with the same values for the three different Poisson's ratios determined by Maschmann et al. By using a modulus value of $E_y = 1$ MPa with the Poisson's ratios of Maschmann et al, then allows for values of E_x, E_z, and G_{xz} to be calculated. Using this approach, these calculated values of E_x, E_z, and G_{xz} will be different than Maschmann et al's, but the material model will behave in a similar manner since the same Poisson's ratios are used. Specifically, the Young's modulus values are calculated from Hooke's law for an orthotropic material given by Equation 21 and 22 and the shear modulus by using those values and Equation 20. The values for the mechanical properties for this second case of transversely isotropic material model are listed in Table 24. In order to obtain values for G_{xy} and G_{yz}, it is needed to assume they are the same as G_{xz} for this case. This assumption is based off the observation that the three components of shear moduli are very similar to each other in Maschmann et al's model. This relationship of shear moduli values is extended in this second case so that G_{xy} and G_{yz} are the same as G_{xz}. Therefore all of the mechanical material constants are defined for the second case for a transversely isotropic CNT material and listed in Table 24.

Table 24: Transversely isotropic properties for CNT off-chip interconnect for two cases of material models

Property	Case 1: Using values from Maschmann et al [141]	Case 2: Using modulus values from this thesis and from [141]
E_x (MPa)	2.5	0.0119
E_y (MPa)	210	1
E_z (MPa)	2.5	0.0119
ν_{xz}	0.12	0.12
ν_{xy}	0.004167	0.004167
ν_{yz}	0.35	0.35
G_{xz}	1.12	0.005
G_{xy}	1.10	0.005
G_{yz}	1.10	0.005

Table 25: Die stresses calculated using two different cases of transversely isotropic material models for CNT interconnects and two cases of similar fully isotropic material models

CNT Material Model Case	σ_{xx} (MPa)	σ_{yy} (MPa)	σ_{xz} (MPa)	σ_{yz} (MPa)
Case 1: Transversely iso. model from [141]	9.3070	2.4191	4.4210	5.3148
Fully iso. with E = 210 MPa	10.308	6.1822	6.3403	8.4659
Case 2: Transversely iso. model using modulus values from this thesis and from [141]	9.3582	2.3920	4.3819	5.2694
Fully iso. with E = 1.0 MPa	9.3482	2.3979	4.3925	5.2836

Finite-element models that are the same as in Section 7.2.1-7.2.3 were used for this section, but while utilizing the two different cases of transversely isotropic material models of Table 24. In comparing the values of properties of the two material models it can be seen that the values of the respective Young's moduli are approximately two orders of magnitude different from each other. The die stresses from the finite-element analysis of these two cases are listed in Table 25. This table shows that the stress values are very similar for Case 1 and 2 even though there is almost two orders of magnitude difference in the moduli values between the cases. This is due to a similar observation from the study investigated in Section 7.2.5 where the effect of the magnitude of the isotropic modulus was conducted. In that study when the isotropic modulus was very low, further reduction of the modulus had little effect on the die stresses since the silicon die and substrate were effectively already mechanically decoupled. In Case 1, of the transversely isotropic property study, even though E_y has a value of 210 MPa, the die stresses are very low and similar to the values of Case 2 where E_y=1 MPa. This is because while E_y is greater in Case 1, the values of E_x and E_z are still very small (~2 orders of magnitude less than Case 1) and therefore dominate the thermomechanical stress results. These relatively low values of E_x and E_z then cause very little change in the die stresses even though E_y=210 MPa is at a relatively large value for a CNT forest. This observation is further illustrated by comparing these transversely isotropic models to cases of fully isotropic material models that use E_y and ν_{yx} of each of the respective transversely isotropic models. The values for these cases are also listed and compared in Table 25. This table shows that Case 1 compared to the fully isotropic model with E_y=210 MPa has slightly lower die stresses than the already low stresses of the fully

isotropic case. Therefore, the fully isotropic model is a conservative assumption for the die stresses. But for Case 2 compared to the fully isotropic model using the same E_y = 1 MPa, all of the die stress values are extremely similar, with very little difference. Therefore for this situation where the largest modulus value in the transversely isotropic material is relatively low, the simplified fully isotropic material model is a valid assumption to study the thermomechanical die stresses of the flip chip.

In summary, the use of a transversely isotropic material model for CNT interconnects has an effect on the die stresses while performing a thermomechanical analysis. The effect that the transversely isotropic model has on the die stresses is dependent on the severity of the difference in the material properties for the different directions and also on the magnitude of the moduli. This effect was found to be very small or almost zero in this study due to the large moduli difference and low value of the lowest Young's modulus in the material models. In the models tested, there was a difference of two orders of magnitude between E_y and E_x=E_z, with the value of $E_x \leq$ 2.5 MPa. If a different material model was used instead, with the three moduli closer in value or with a larger value for the lowest moduli, then the die stresses would increase and approach that of the results using a fully isotropic model with the same modulus. Even with this scenario, the stresses in the silicon die would be very low. Therefore the fully isotropic model is a conservative assumption, while still demonstrating very low die stresses when compared to traditional solder ball interconnects. If a different analysis scenario is performed though, it may beneficial to revisit this question since multiple factors are involved. For the thermomechanical analysis conducted in this study, a fully isotropic material model is sufficient.

7.3 Summary – Finite-Element Modeling of CNT Off-Chip Interconnect

In this chapter the issue of mitigating the fracture of weak low-k dielectric layers caused by high stresses in silicon dies was investigated. This was completed by using finite-element analysis to model a flip chip attached to a FR4 substrate with CNT forest interconnects with a relatively low effective modulus. It was shown with finite-element analysis that the CNT interconnects effectively mechanically decoupled the FR4 substrate from the flip chip and eliminate/greatly reduce the thermal mechanical stresses due to CTE mismatch between the two. It was show that these CNT interconnects can reduce die stresses by 94-71% compared to traditional lead free solders with underfill. Also, not only are the stresses in the die reduced greatly, but the amount of the chip that experiences elevated stress levels is much smaller than occurring when solder balls and under fill is used. This would further help mitigate the occurrence of fracture in low-k layers. It was also demonstrated that the flip chip and FR4 substrate are mechanically decoupled by showing that chip warpage is reduced/eliminated by using the CNT interconnects.

After addressing the main question of this chapter regarding the use of CNT interconnects to reduce die stresses, the finite-element models were used to better understand the effect of key parameters relevant to the implementation of CNT forests as off-chip interconnects. Since a wide range of values have been measured for the modulus values of CNT forests, it was desired to understand the effect of varying this on flip chip stresses. It was found that there a small degree of dependence on the flip chip stresses when the modulus values are high within the range of reported values. But, even these cases of elevated chip stresses provide large decreases in die stresses compared to cases

using solder balls and underfill. Therefore it was determined that it is not crucial to attempt to control the CNT effective modulus value during the fabrication process to achieve these thermomechanical reliability benefits.

Another packaging design variable that was studied with finite-element models was the CNT height. This is important since there is an open range of heights possible for packaging engineers to choose from when growing the CNTs. It was found that CNT height has very little effect on die stresses (using a Young's modulus of 1 MPa obtained in this thesis) since the die stresses are already very low for the simulated CNT modulus value. But for cases with CNTs of different modulus values that would result in higher die stresses, increasing the interconnect height could allow a method to reduce the die and interconnect stresses if needed.

Lastly the effect of the type of material model for the CNT interconnect, fully isotropic vs. transversely isotropic, to be used in the finite-element analysis was investigated. It was found that there is very little difference between the die stresses between the two material model types when the axial modulus of the transversely isotropic model is used for the fully isotropic material model. The difference between the material models increases as the axial modulus used is increased (while the moduli within the plane of isotropy remain constant) but the die stresses still remain low in both material model cases. Therefore it was determined that the fully isotropic model is a conservative material model assumption and sufficient for these thermomechanical reliability studies.

In summary, this chapter shows that CNT off-chip interconnects reduce die stresses greatly and will aid in mitigating low-k dielectric cracking. Additionally, this

chapter provided insight on the effect of important design variables relevant to electronic packaging such as CNT modulus, height, and material model type to aid future pursuits of this packaging technology.

CHAPTER 8

CNT OFF-CHIP INTERCONNECT FABRICATION, ASSEMBLY AND MECHANICAL RELIABILITY TESTING

8.1 Introduction

In this chapter the fabrication, assembly, and reliability testing of the electrical off-chip interconnects composed of vertically aligned CNT forests is presented and discussed. The electronic packages that are created and tested for thermomechanical reliability are composed of a dummy silicon chip with copper daisy chain traces with CNT forests grown on the circular pads of the daisy chains that form the off-chip interconnects. These CNT interconnects are attached with electrically conductive adhesive (ECA) to an FR4 substrate with a complementary daisy chain pattern. This assembled package was then thermal shock tested to experimentally demonstrate the mechanical reliability benefits that low modulus CNT forest interconnects offer. These experimental results help support and provide validation of the finite-element analysis that was performed on these electronic packages presented in Chapter 7. The reliability benefit that is observed is due to the CNT's low modulus that allows the silicon chip and FR4 substrate to be mechanically decoupled from each other. This decoupling reduces the thermomechanical stresses that occur due to the difference in the CTE's of the silicon and FR4 materials. Currently in literature, there have been studies and reports of the fabrication of CNT based off-chip interconnects with the focus of these studies being the fabrication and characterization of their electrical performance [36, 63, 66, 69, 71, 72]. These studies mention a potential mechanical benefit, but none demonstrates the mechanical reliability benefits that CNT off-chip interconnects can provide. Therefore

the fabrication of electronic packages with CNT based off-chip interconnects for thermomechanical reliability testing presented in this chapter is the first such study and provides a bases for future endeavors in CNT interconnect research.

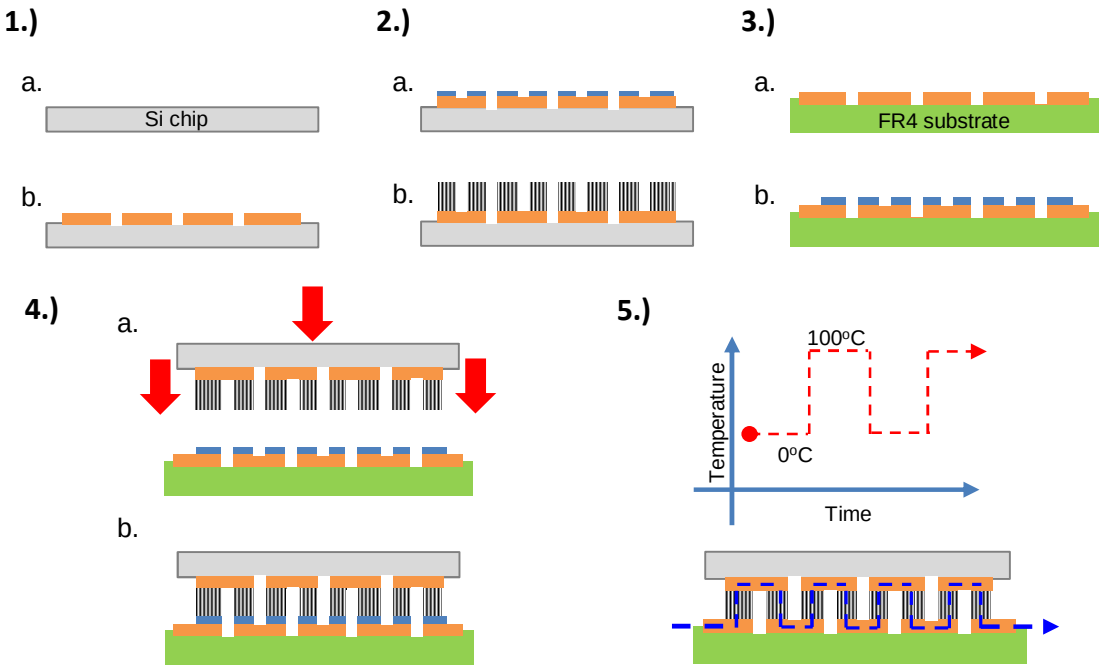


Figure 74: Overall/general presentation of the steps necessary to first fabricate the Si chip with CNT interconnects, creating FR4 substrate with stencil patterned conductive adhesive, assembly and attachment of the Si chip to the FR4 substrate, and finally thermomechanical testing.

8.2 Overview/General Package Fabrication

To achieve the final goal of performing thermal cycle testing to demonstrate that the silicon die and FR4 substrate are mechanically decoupled from each other, and that the CNT interconnects provide thermomechanical reliability benefits, it is first necessary to fabricate and assemble the test vehicle samples as shown in Figure 74. To fabricate these samples, the overall necessary steps include:

1. Create dummy silicon chips with photolithography patterned peripheral copper daisy chains on a blank silicon wafer.

2. Use photolithography to pattern CNT support structure material and CNT catalyst on the circular pads of the copper daisy chains, and then grow the CNT forests for the off-chip interconnects on the silicon chip.
3. Create custom FR4 substrate with complimentary daisy chain pattern and then stencil electrically conductive adhesive onto the copper pads of the FR4 substrate.
4. Assemble the silicon dummy chip with CNT interconnects to the FR4 substrate with stenciled adhesive using a modified rework/alignment assembly tool. Then cure the adhesive to mechanically and electrically connect the silicon chip with CNT interconnects to the FR4 substrate, and thus completing the daisy chain style electrical circuit.
5. Test the thermomechanical reliability by subjecting test vehicles to accelerated thermal shock tests while insitu monitoring the electrical resistance of several of the interconnects.

Each of the following sections of this chapter will focus on and go into detail on each of these steps and the processes used to fabricate and test these samples.

8.3 Chip-Side Daisy Chain Fabrication

The electronic package utilizing CNT interconnects fabricated and assembled in this chapter is the same as was analyzed with finite-element analysis in Chapter 7. The package geometries and dimensions are based on commercially available electronic packages and specifically the dummy mechanical chip PB08-400x400-DC-LF2 available from Practical Components Inc. The dimensions used here to fabricate the chips are illustrated in Figure 75, where the diameter of the daisy chain pads are 120 μm, with a

pitch of 203 µm, and copper trace width of 105 µm. Also, the thickness of the copper composing the daisy chains is 1.7 µm.

The fabrication process for the silicon chip with copper daisy chain pattern is illustrated in Figure 76 and starts with a blank silicon wafer of a thickness of ~550 µm (Figure 76, Step 1). Then a Unifilm® magnetron sputter machine is used to deposit a 1.7 µm thick copper film (Step 2). Next, the copper was patterned into a daisy chain pattern using photolithography and Shipley Microposit® SC1827 photoresist with a thickness of ~2.7 µm (Steps 3-4). Using Transene® Aluminum Etchant A, the copper was then etched into the daisy chain pattern on top of the silicon (Step 5). The photoresist was then removed with Shipley Microposit® 1165 photoresist remover and subsequently subjected to an oxygen descum process using a Plasma-Therm® RIE machine to further clean any residual photoresist off the copper (Step 6). The result of these fabrication processes is the copper daisy chains shown in Figure 77, and on which the CNT forests will be grown and presented in the next section.

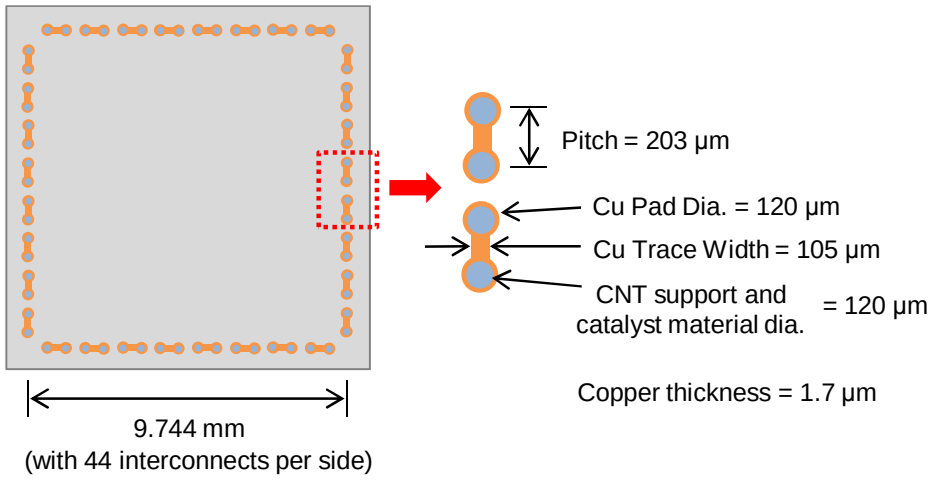


Figure 75: Dimensions of the fabricated Si chip with Cu daisy chain and growth materials for CNT interconnects.

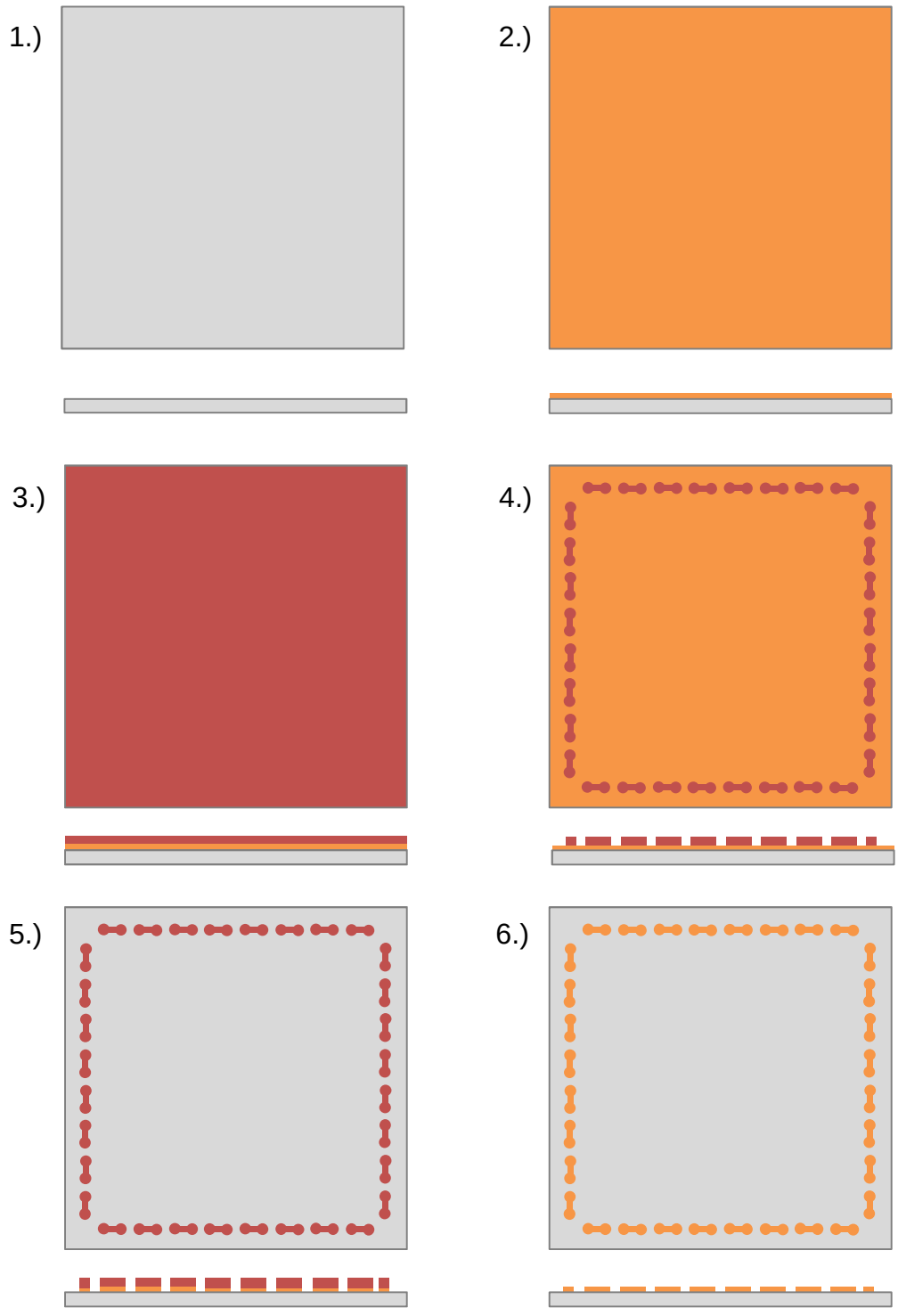


Figure 76: Illustration of photolithography fabrication process to create peripheral Cu daisy chain pattern on Si chip.

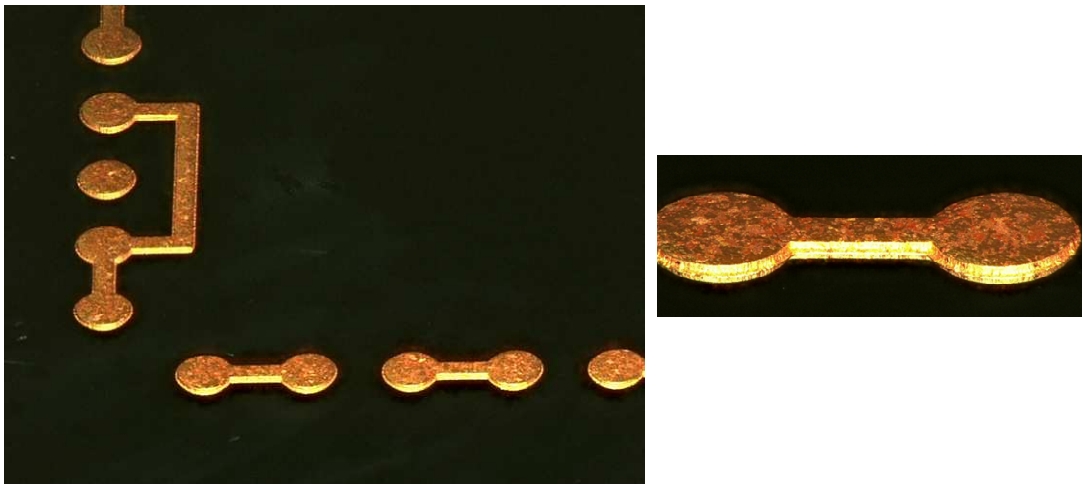


Figure 77: (left) Optical images of example of Cu daisy chains located at the corner of a peripheral pattern on a Si chip. (right) Magnified optical image of single Cu daisy chain.

8.4 Patterning CNT Growth Materials

After creating the copper daisy chain pattern discussed in the previous section, it was necessary to grow vertically aligned CNT forests selectively on the circular areas of the daisy chain in Figure 77 to create the CNT interconnects. The process to grow CNTs in this thesis utilizes thermal CVD, a metallic catalyst film, and a support material film. Several synthesis methods have been used to grow CNTs in literature such as arc discharge, laser ablation, thermal CVD, and PECVD [33]. But, thermal CVD was chosen here for this study since it possesses many desirable characteristics of the electronic packaging and semiconductor industry such as, high production yield, low setup cost , scalability [142], and most importantly it is very conducive to growing CNTs selectively on specific patterned areas. Currently, there is no definitive CNT growth model or mechanism, but there is a widely accepted general process for CNT growth described by Kumar and Ando [142], and is presented in the preceding paragraph.

To grow CNTs, a hydrocarbon precursor gas such as acetylene [143-146], ethylene [147, 148], methane [149-151], xylene [152, 153], or carbon monoxide [154] is

passed over a test sample at an elevated temperature in the range of ~550-1200^{o}C [155]. The sample must contain a thin metal catalyst at the location of desired CNT growth. The most common catalyst materials are transition metals including Fe, Co, Mo, and Ni because of their high solubility of carbon at high temperatures [142]. Additionally, these thin catalyst films are deposited on top of a thin support layer such as quartz, silicon, silica, or aluminum. This support layer and the thin nature of the catalyst/support layer, combined with the high process temperature, allow the catalyst film to break up into small nanoparticles on the surface which act as reactive sites. Generally, the size of these nanoparticles has a strong influence on the CNT diameter and on whether SWCNTs or MWCNTs are created [156]. Later, as the hydrocarbon precursor gas enters the thermal chamber, it then travels and hits these hot catalytic nanoparticles which cause the gas to decompose into carbon and hydrogen species. The carbon species then dissolves into the catalyst particle due to the metal's carbon solubility, while the hydrogen species floats away. Once the catalyst nanoparticle reaches its carbon solubility limit for the given metal and temperature, the dissolved carbon precipitates out of the particle. This commences the actual CNT tube growth as it precipitates out and crystallizes the carbon atoms into the form of a cylindrical structure. This structure is characterized by possessing no dangling bonds, causing it to be energetically stable. Finally, the CNT growth ceases when the precursor gas flow is stopped or when the catalyst nanoparticle becomes coated with amorphous carbon buildup (sometimes referred to as poisoning) and thus preventing further adsorption of carbon species.

In the following synthesis of CNTs for off-chip interconnects, acetylene was chosen as the precursor gas since it possesses linear hydrocarbons, which generally

produce straight CNTs due to their decomposition into atomic carbons or linear dimers/trimers [157, 158]. Additionally, literature has been shown that acetylene when used in conjunction with the common catalyst of Fe and Al support film can synthesis tall vertically aligned CNT forest on copper films. Therefore, the use of an acetylene precursor, Fe catalyst, and Al support film was used in this study to synthesize CNTs with the desired characteristics for the off-chip interconnects.

In order to create CNT interconnects, it is necessary to selectively grow forests of CNTs on the copper pads of the daisy chains. To accomplish this, the catalyst and support materials must be patterned on the circular copper pads using a photolithography lift-off process that is illustrated in Figure 78 and described in the following. First, negative photoresist (Futurrex® NR9-1500PY) was used to coat the silicon wafer containing the previously created copper daisy chain pattern on the surface (Figure 78, Step 2). Then a photomask with a circular peripheral pattern was used with a mask aligner to create holes in the negative photoresist layer (Figure 78, Step 3). It should be noted that the exposure time for the negative photoresist was four times the calculated theoretical exposure time based on the photoresist thickness and mask aligner lamp intensity due to the reflectivity of the copper daisy chain. After the resist was exposed, patterned, and developed, a short descum process in a Plasma-Therm® RIE was performed in order to remove any residual resist or other organic material remaining on the opened circles on the copper pads of the photoresist.

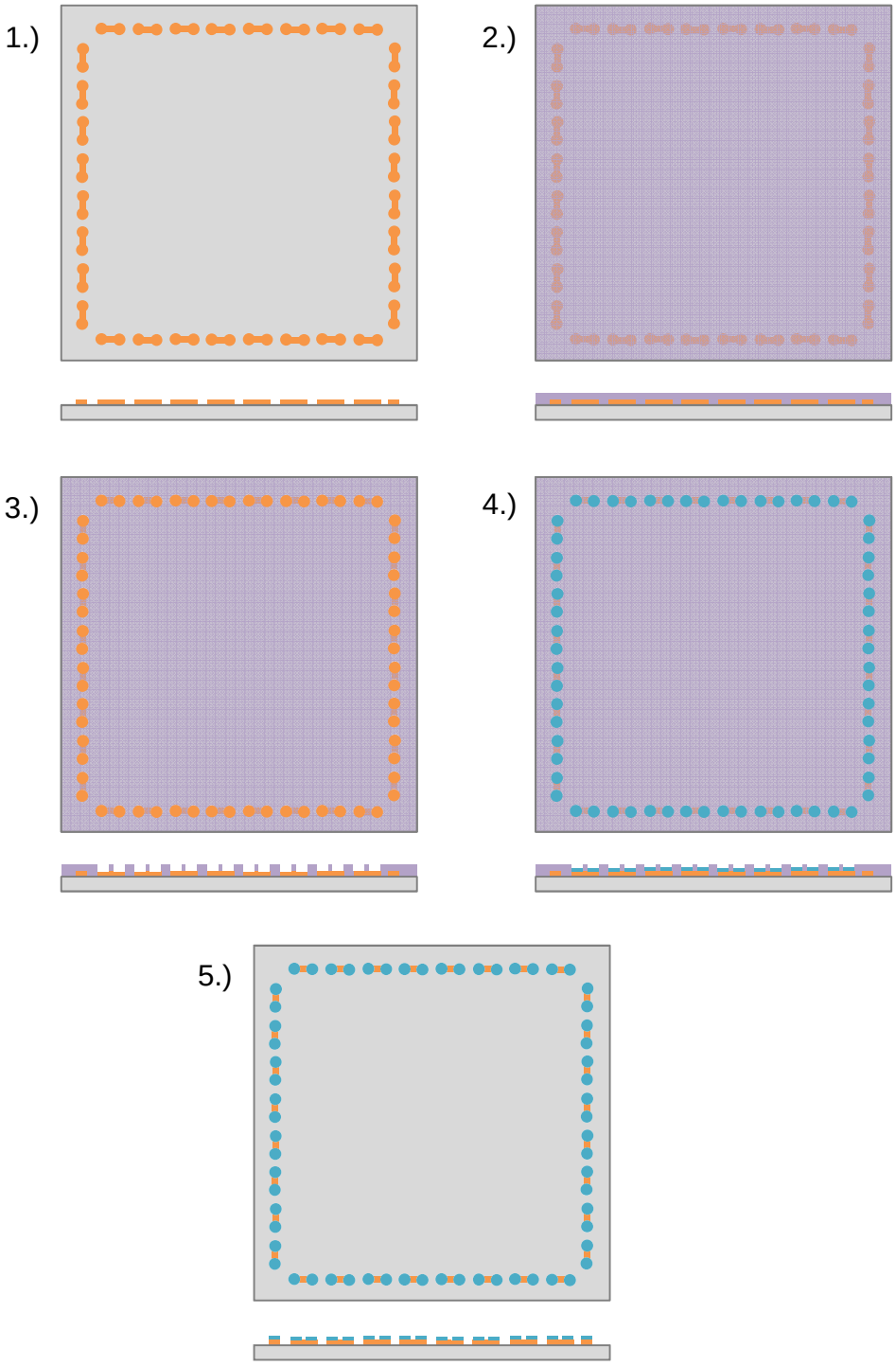


Figure 78: Photolithography lift-off process steps to define the catalyst and support material for CNT growth on the already patterned copper daisy chain on a silicon die.

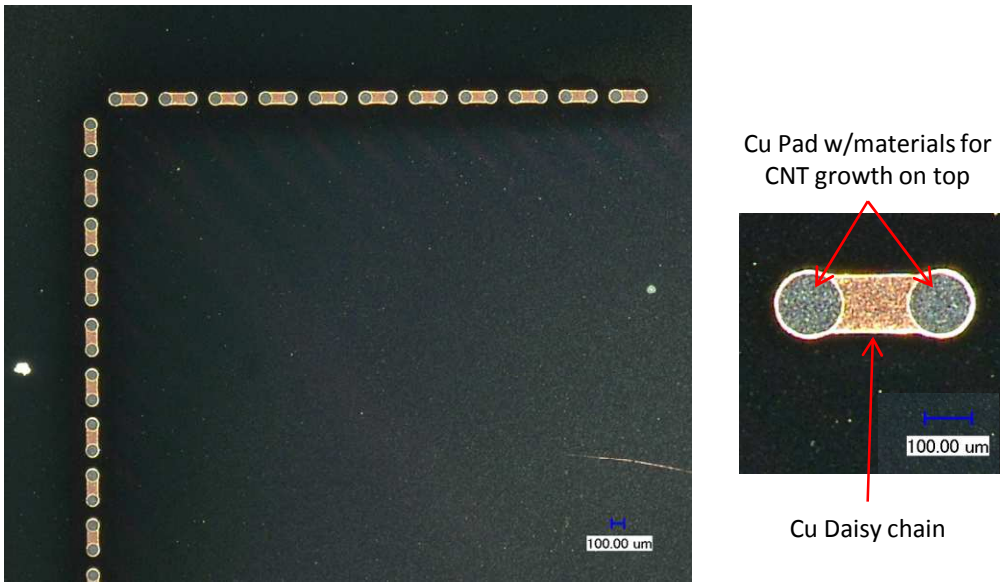


Figure 79: (left) Optical image of a corner of the peripheral patterned copper daisy chains with the catalyst and support material defined. (right) Zoomed in optical image of a single daisy chain with catalyst and support material patterned on circular the circular copper pads.

It is very important that the copper pads are clean to avoid any contamination of the support layer and catalyst layer that will subsequently be deposited on top of these areas. The importance of avoiding contamination by organic materials prior to and during CNT growth is related to the topic of amorphous carbon buildup on the catalyst particles mentioned earlier in this section. This "bad" amorphous carbon prevents the growth of the "good" crystalline carbon of the growing CNT tube [146, 159]. Therefore, it is necessary to clean the exposed area of the copper pad, but while not removing the remaining photoresist. Once this preparation and cleaning is completed, a CVC® E-beam evaporator is used to first deposit 10 nm of aluminum at a rate of 0.2 Å/s as a support layer followed by 2.2 nm of iron catalyst at a rate of 0.1 Å/s (Figure 78, Step 4). After the Al and Fe are deposited, it is necessary to complete the lift-off process by removing the negative resist (Figure 78, Step 5). The resist was removed by placing the samples in an acetone solvent bath in an ultrasonic sonicator for 1 minute. While removing the

photoresist during this process, it is essential to not over sonicate. Over sonication can potentially remove the thin support and catalyst films in the process of removing the negative photoresist. After the negative photoresist is removed, the sample is descumed in the Plasma-Therm® RIE for 5 minutes to remove any excess organic material on the surface or catalyst film. At this stage of the fabrication, the support/catalyst layer has been patterned on the circular pads of the copper daisy chain as shown in Figure 79.

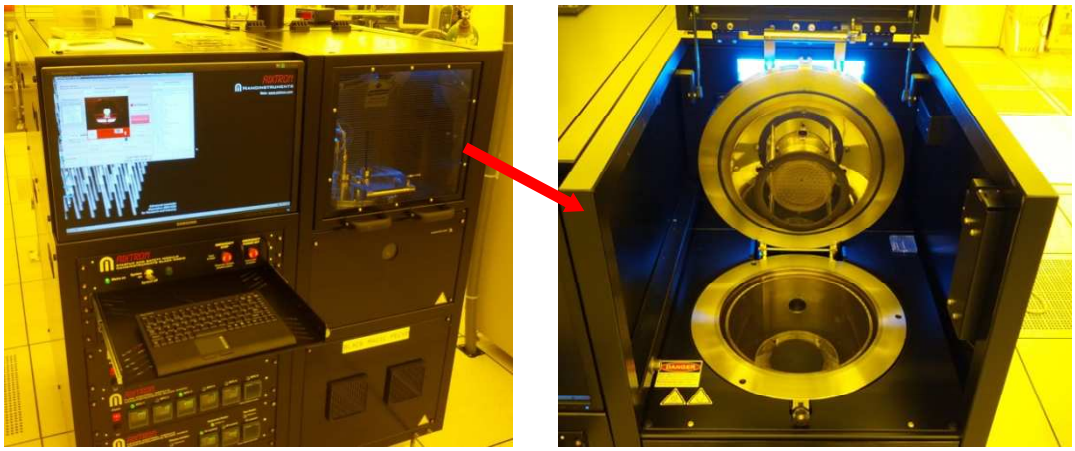


Figure 80: (left) Aixtron® Black Magic CVD system. (right) Close up of CVD chamber showing the sample plate and Quartz shower head on the chamber lid.

8.5 Growing CNTs on Copper Daisy Chains

The most common substrate for growing CNTs is silicon. Recently there has been a great amount of research pursuing growing high quality vertically aligned CNTs on other materials such as metal [39, 124, 160-166]. This is due to the great interest in using CNTs as electric of thermal conductors, and therefore making metal an obviously desirable growth substrate to attach CNTs to devices. For the application in this thesis, the CNT forests are being used as off-chip electrical interconnects grown on the copper pads of a daisy chain substrate to create an electrical circuit. Since the substrate in this case is the copper daisy chain pad (Figure 79), it is necessary to use a CNT recipe that grows vertically aligned CNTs on copper. Even though copper is a transition metal, it

has been shown to either promote or inhibit CNT growth. Therefore, the CNT growth recipe, support layer material, and catalyst are important for successful CNT synthesis on copper. The CNT recipe used here was based on several found in current literature [167-170]. Additionally the CNTs used in this section were grown in an Aixtron® Black Magic CVD system (Shown in Figure 80) maintained at Georgia Tech in the Institute for Electronics and Nanotechnology (IEN). The synthesis recipe is a low pressure process with the following steps:

1. Anneal the catalyst using 700 sccm of H_2 with 200 sccm of N_2 carrier gas, while ramping the temperature to 740^{o}C at 300^{o}C/min.
2. Once 740^{o}C is reached, anneal for 3 minutes. With these parameters, the catalyst anneal step is carried out at 22.4 mbar.
3. After the anneal step, ramp temperature to 850^{o}C at 300^{o}C/min.
4. Once 850^{o}C is reached, flow 100 sccm C_2H_2 (acetylene) along with 700 sccm of H_2 and 200 sccm of N_2 carrier gas. With these parameters, CNT growth is carried out at 8.44 mbar. Flow gasses for desired CNT growth time.
5. To terminate growth, turn off flow of C_2H_2 and H_2 and wait till temperature cools to 650^{o}C.
6. Once 650^{o}C is reached, increase flow of N_2 to 1000 sccm. Then at 600^{o}C, increase N_2 flow to 8000 sccm. N_2 gas flow is turned off once the temperature reaches 200^{o}C and the sample can be unloaded.

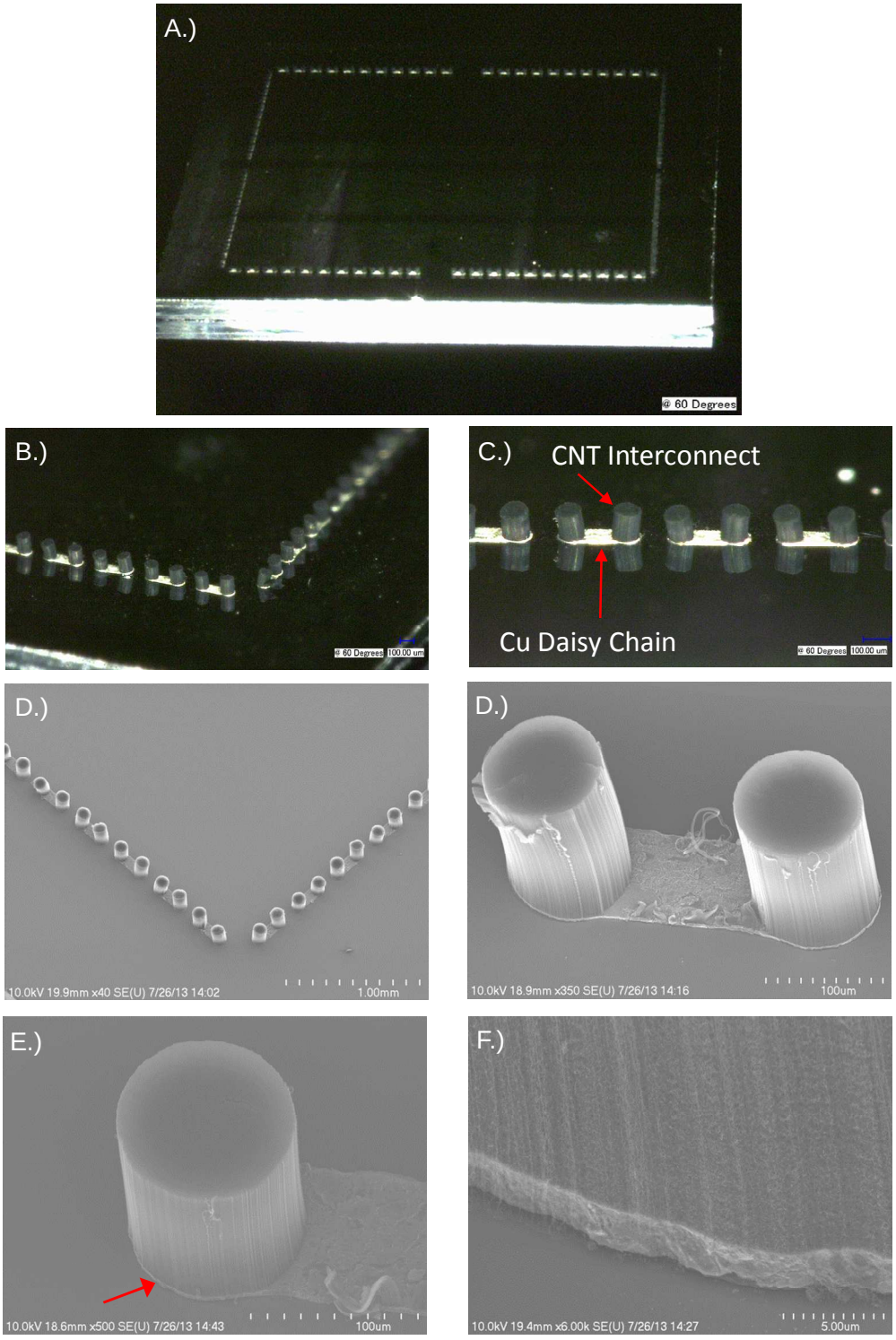


Figure 81: A.) Optical image of entire Si chip with Cu daisy chains with CNT bundles. B-C.) Zoomed in optical images of Cu daisy chains with CNTs grown on them showing even height between interconnects. D.-E.) SEM images of various magnifications showing CNTs on Cu daisy chains with good evenness and alignment F.) SEM image showing Cu film with CNT roots bonded to it and having a slightly wavy CNT geometry.

The length of time that the acetylene precursor gas is allowed to run is a major determining factor on the height of the CNT forests for the interconnects. During synthesis it was found that the growth rate was not always consistent. This was attributed to the fact that the Aixtron® Black Magic system is a shared machine with several users, and therefore contamination is an issue. As mentioned previously, the nature of CNT growth involves the competing pathways of the accumulation of "good" graphitic carbon and "bad" amorphous carbon [146, 159]. The latter of these can be increased by outside organic contamination from many possible sources. Additionally, The CVC® E-beam evaporator used to deposit the support and catalyst material is also a shared machine and therefore has possible variances that are difficult to control. The growth of CNTs has very little tolerance to such variations and therefore the CNT growth results vary, but growth times were typically between 8-20 minutes.

The target height for the interconnects was 75-150 μm. This is a relatively tall height for CNT forests with a bundle diameter of ~120 μm, but it is still possible for the bundles to have consistent height from bundle-to-bundle with minimal bundle bending. This type of bundle height/alignment is necessary for CNT alignment/attachment to the FR4 substrate in the subsequent assembly processes. Several optical and SEM images of the CNT interconnects grown for this study are shown in Figure 81. These images in Figure 81 show that the CNTs are within the desired height range, have good bundle alignment, are vertically aligned with a wavy local structure to provide good compliance, and are grown on and attached to the underlying copper daisy chain to allow electrical conduction. Also, it should be added that the FEA models discussed in the previous chapter have used the fabricated CNT height, discussed in this chapter.

8.6 Stenciling Electrically Conductive Adhesive

In order to attach the CNTs grown on the copper daisy chain pads of the silicon chip created in Section 8.5 to the complementary daisy chain pattern on the FR4 substrate, electrically conductive adhesive was used. Conductive adhesive is a common material in electronic packaging and has gained interest due to its lead-free nature, and can be applied to repair interconnects, bridge electrical traces, or act as the interconnect itself [137]. The use of adhesive in this study allows the CNT off-chip interconnects to be connected to the FR4 substrate both electrically and mechanically. Electrically conductive adhesives have been used with CNTs in other studies [171, 172], but slightly differently, in this investigation the adhesive is being used to connect the already grown and defined CNT bundles to the copper daisy chain of the FR4 substrate. This attachment of the silicon chip and FR4 substrate completes the daisy chain circuitry (Figure 74, Step 5) that will be monitored during the thermal shock testing to determine the mechanical reliability of a package using CNT forests as off-chip interconnects.

Specifically, it was decided to use Epotek-H20-PFC® electrically conductive adhesive (Specification literature in Appendix A.6). This adhesive has a proper viscosity to allow for stencil printing down to opening sizes of 101.6 μm (according to the specification literature, but 40 μm according to experience of Epotek engineering support), low electrical resistance (0.0004 ohm-cm vs. 0.000015 ohm-cm for Sn/Pb solder [137]), a wide range of cure temperatures (21^{o}C - 175^{o}C), and consists of a two part epoxy that contains silver flakes to create electrical conductivity in the epoxy.

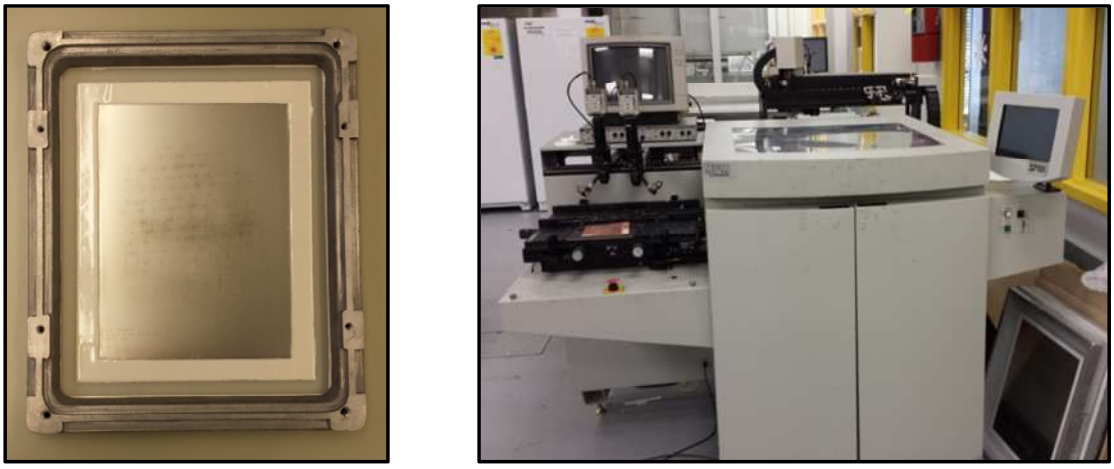


Figure 82: (left) Framed metal foil stencil that was used in the SPM machine (right) to pattern the electrically conductive adhesive on FR4 substrates.

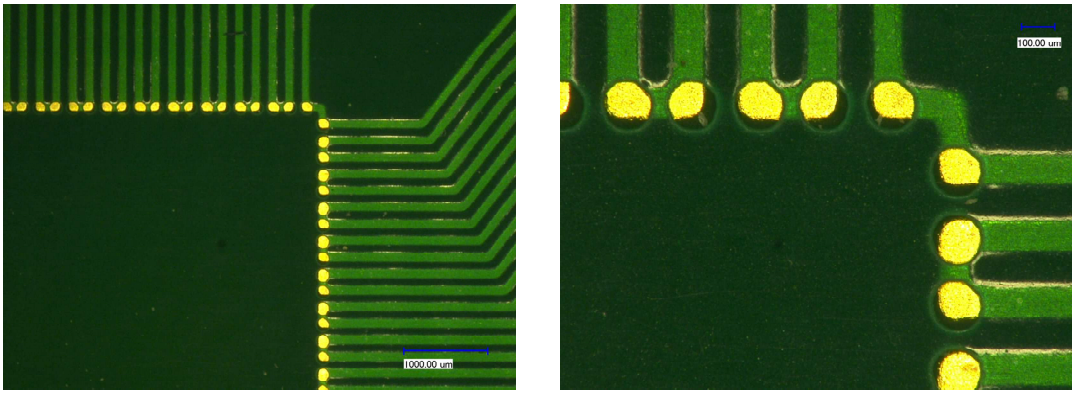


Figure 83: Optical images of custom fabricated FR4 substrates of various magnifications. Shows corner of peripheral copper daisy chain pattern covered by green soldermask. Circular soldermask openings to be filled with electrically conductive adhesive.

In order to pattern the adhesive on the FR4 substrate, an 8”x10” framed SMT metal stencil was designed and fabricated (Figure 82). The stencil matches the geometry of the CNT interconnects, consisting of peripheral circular openings with a pitch of 203 μm, and stencil openings of an 80 μm diameter. The FR4 substrate that the adhesive will be patterned on also has a copper daisy chain pattern on the surface. On top of this copper daisy chain there is a patterned solder mask layer with openings exposing only the circular pads of the daisy chains (Figure 83). The thickness of this solder mask (~23 μm) helps contain the adhesive when the stencil is in contact with the surface and the adhesive

is squeegeed into the openings, and therefore filling them up. Also, in order to prevent any additional bleeding/bridging of the adhesive when patterned, it was necessary for the stencil openings to be smaller than the ~100 μm diameter solder mask openings.

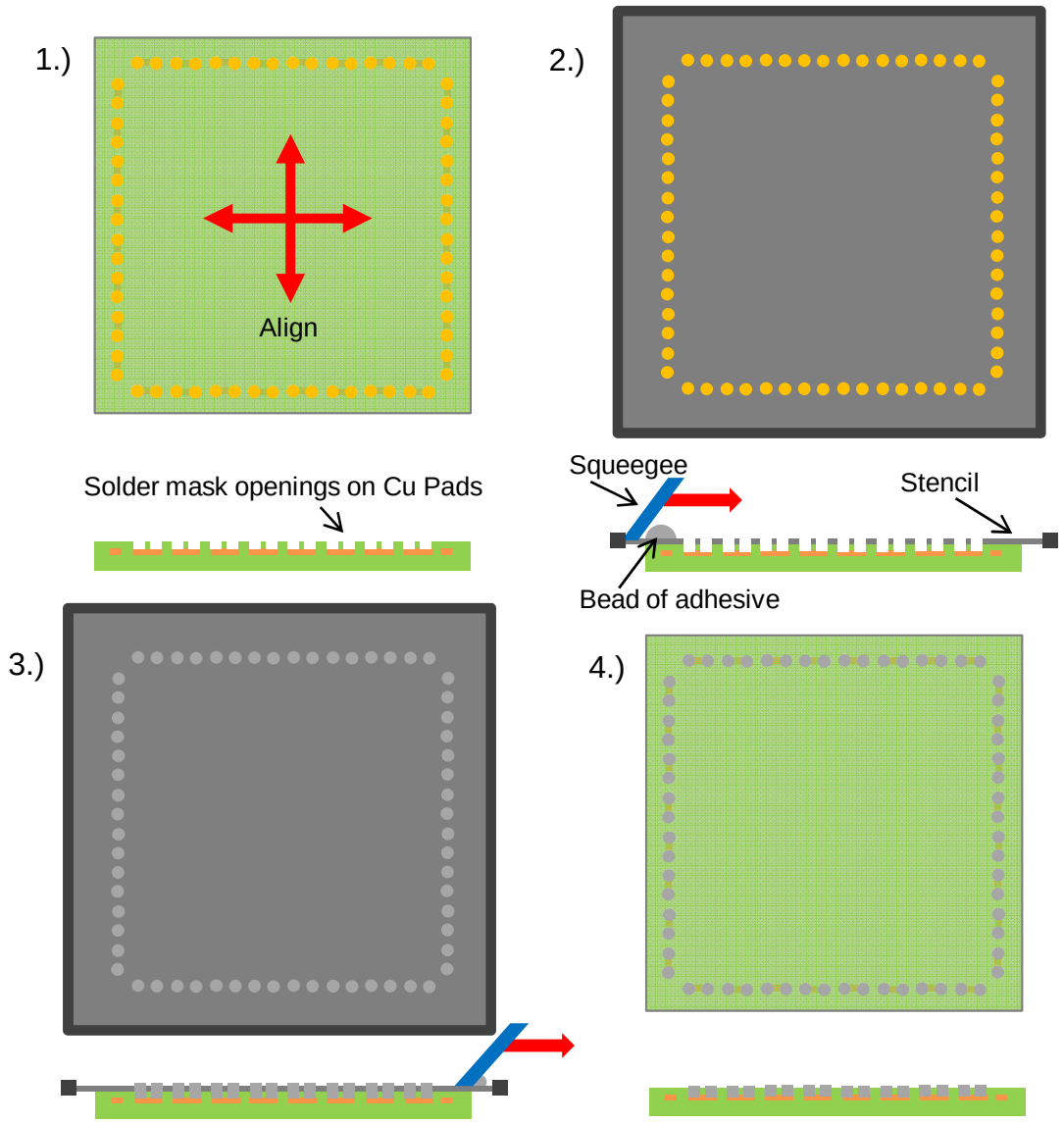


Figure 84: Illustration of process used to pattern the electrically conductive adhesive on the circular copper pads of the FR4 substrate using a stencil and stenciling machine.

To perform the stenciling of the electrically conductive adhesive onto the FR4 substrate, a SPM machine manufactured by MPM Corporation was used. This machine is shown in Figure 82 and is maintained by the Georgia Tech Packaging Research Center

(PRC). The general process of stenciling the adhesive using this machine is illustrated in Figure 84 and outlined below:

1. Process begins with aligning the solder mask openings on the FR4 substrate with the openings in the stencil (Figure 84, Step 1).
2. Once aligned, the user applies a line of excessive adhesive to the stencil along the outside of the pattern edge. The machine then presses the stencil against the board with a specified distance as shown in Figure 84 Step 2, then the machine brings the squeegee into contact with the surface of the stencil with the specified squeegee force (Appendix A.1.4), and then squeegees the adhesive across the stencil at the specified speed.
3. The squeegee is then withdrawn from the stencil showing that the adhesive has filled the openings of the stencil and is adhering to the copper daisy chain pads (Figure 84, Step 3).
4. Then the stencil is withdrawn from the FR4 substrate, leaving the adhesive only on the copper pads of the daisy chain (Figure 84, Step 4).

Examples of successfully patterned electrically conductive adhesive are shown in Figure 85. These optical images of various magnifications show that the adhesive is contained in the solder mask openings of the FR4 substrate for the entire peripheral daisy chain pattern of the test sample with no bleeding or bridging of the adhesive. Therefore, at this point the FR4 substrate with adhesive is ready for assembly with the dummy silicon chip with the CNT interconnects grown on it.

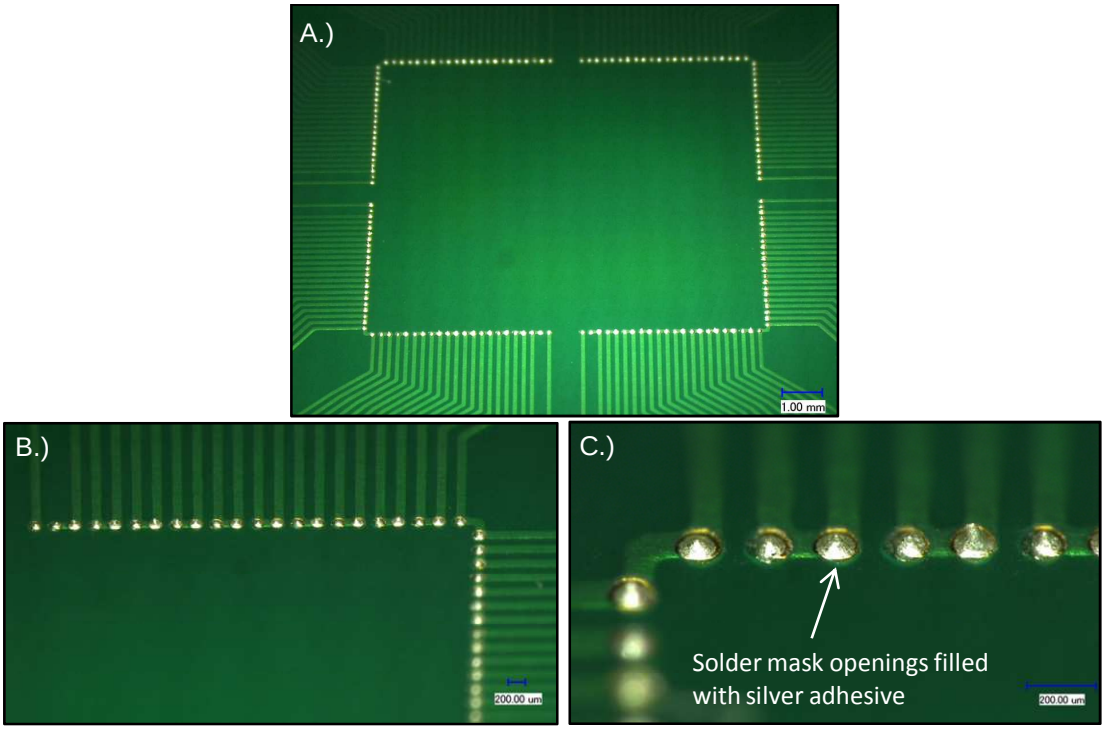


Figure 85: A.) Angled optical image of entire peripheral daisy chain pattern for a single Si chip on the FR4 substrate with patterned electrically conductive adhesive. B.)-C.) Show higher magnification optical images of the patterned adhesive filling the solder mask openings and covering the copper daisy chain pads.

8.7 Assembly of Silicon Chip with CNT Off-chip Interconnects to FR4 Substrate

With the CNT interconnects grown on the copper daisy chains of the silicon chip and the electrically conductive adhesive patterned on the complementary daisy chain pattern of the FR4 substrate, it is necessary to next assemble the two components. The assembly process used here is similar to that of traditional solder ball interconnects, while possessing some different requirements. Since the CNT interconnects have a low effective modulus to mechanically decouple the deformation of the silicon chip and FR4 substrate, the vertical (*Z*-axis) placement of the chip with CNT interconnects requires great precision. Such precision is not offered by typical flip chip alignment/bonding tools, therefore custom modifications and fixtures were added to a common flip chip alignment/bonding tool (Figure 86). The alignment/bonding tool (Figure 86) allows for

manual alignment of the silicon chip and FR4 substrate using micro-stages in the horizontal plane (*XY*-plane), but there is little control on the vertical displacement or on the resulting force during the placement of the chip on the substrate after the alignment. In order to accommodate these requirements for assembly of the CNT interconnects, the custom fixture shown in Figure 87 was fabricated and added to the alignment tool. This fixture includes a *Z*-axis stage that utilizes pico-motors to provide very precise control of displacement of the FR4 substrate when contacting the CNT interconnects. The stage also has a force load cell incorporated into it to provide observation and control of the amount of force used during assembly. This custom fixture was fabricated in the Georgia Tech mechanical engineering machine shop.

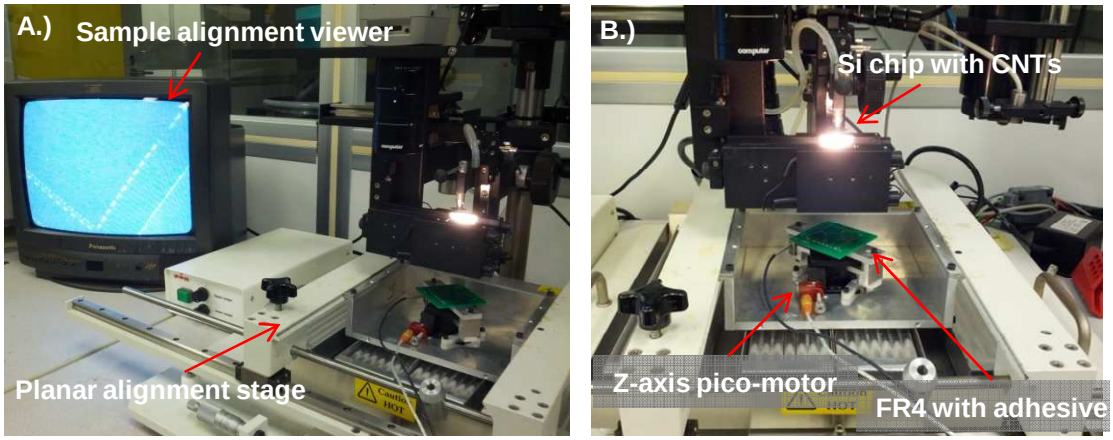


Figure 86: A.) View of monitor showing superimposed view of Si chip on FR4 substrate and the aligner/bonder tool on the right. B.) Zoomed in image of aligner/bonding tool showing the custom fixture on the *XY* stage, with the *Z*-axis pico-motor, FR4 substrate resting on it, dual view microscope above it, and the Si chip on the vacuum chuck above that.

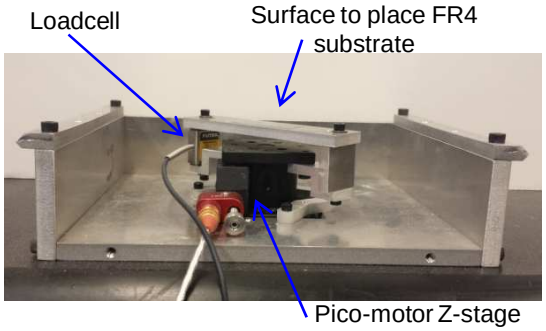


Figure 87: Custom fixture for alignment tool with black pico-motor used to bring the FR4 substrate into contact with CNT interconnects. Also shows aluminum beam where FR4 substrate rests and force load cell for monitoring bonding force.

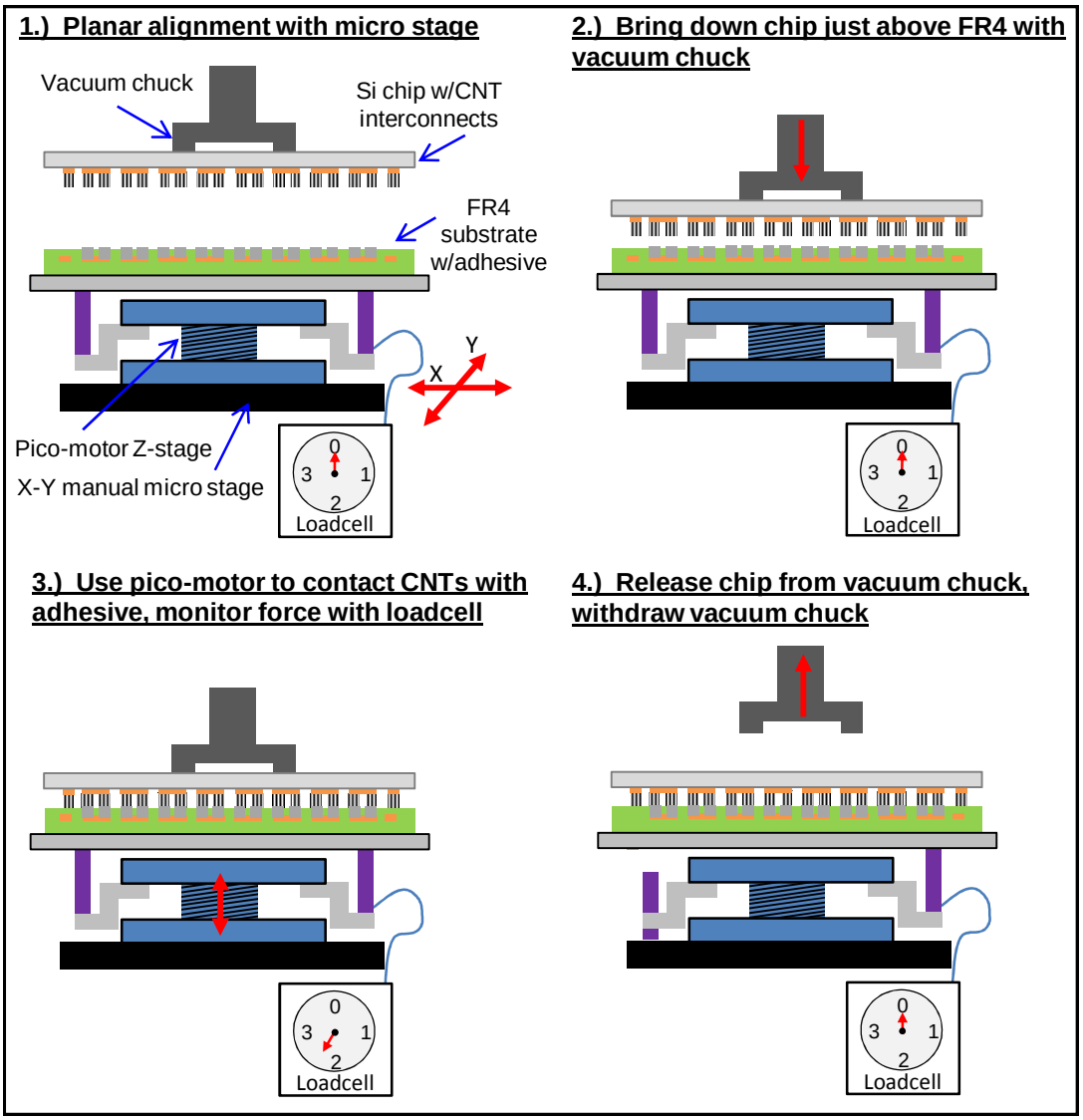


Figure 88: Assembly process with custom fixture to attach silicon die with CNT interconnects to FR4 substrate with electrically conductive adhesive.

The general process to use this alignment/bonding tool with the custom *Z*-axis pico-motors is illustrated in Figure 88 and outlined below.

1. Place silicon chip on the vacuum chuck and place the FR4 substrate with stenciled adhesive on the custom stage with double sided tape. Use the alignment/bonding tool to align the CNT interconnects of the silicon chip with the copper pads and adhesive of the FR4 substrate in the in the *XY*-plane.
2. Once aligned, use the alignment/bonding tool's *Z*-axis approach lever to bring the silicon chip just out of contact with the FR4 substrate. With the chip close to the FR4 substrate, use the custom *Z*-axis pico-motors to slowly bring the CNT interconnects into contact with the adhesive.
3. While using the pico-motors, monitor the stage force load cell. Once the total force reaches ~1 N, stop the pico-motors, turn off the vacuum chuck on the chip, and retract the vacuum chuck.
4. Remove the assembled package carefully from the double sided adhesive on the *Z*-stage and cure the adhesive in oven at the desired temperature to finalize the attachment of the CNT interconnects to the copper pads of the FR4 substrate.

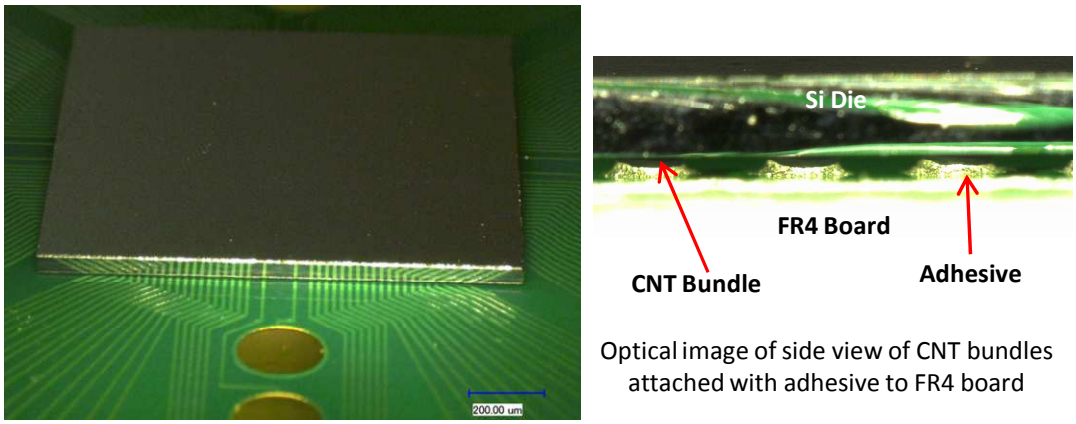


Figure 89: (left) Optical image of angled view of entire Si chip assembled to FR4 substrate. (right) Magnified optical image of example individual CNT interconnects attached to FR4 substrate with electrically conductive adhesive.

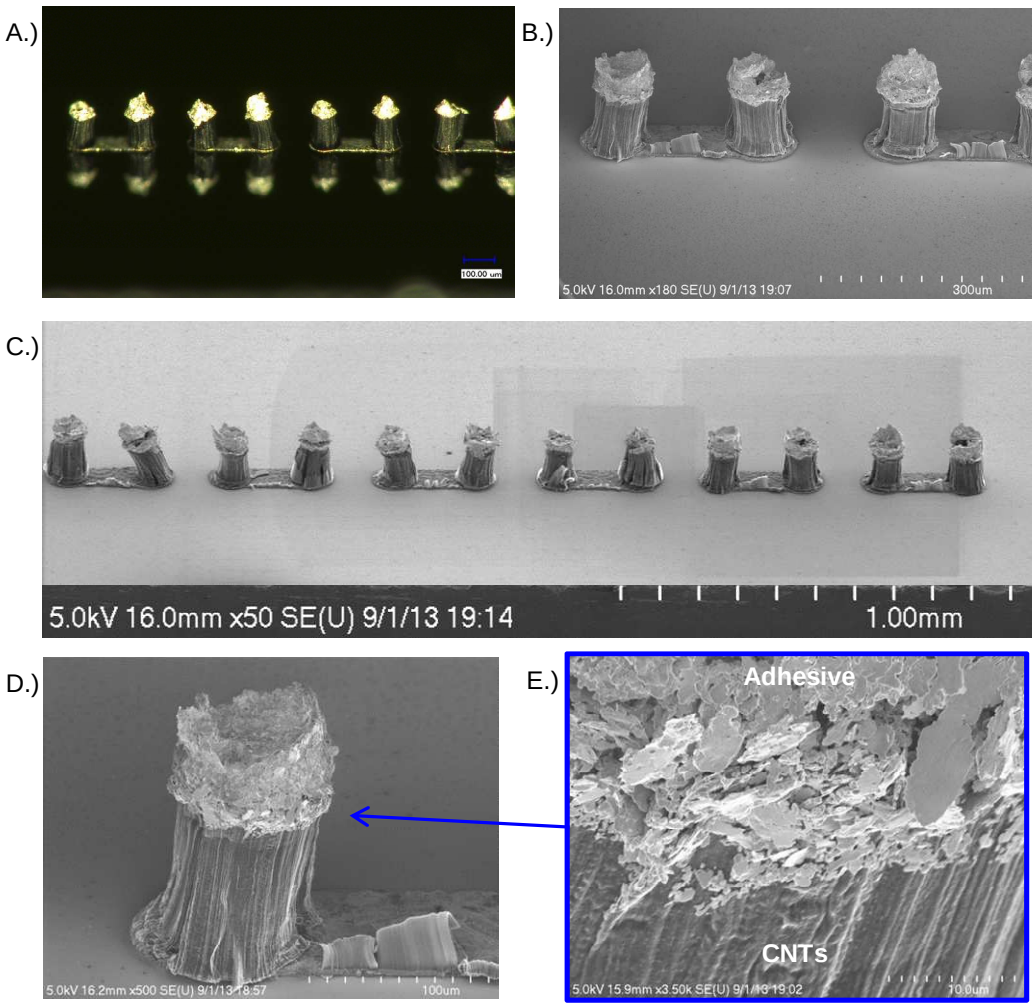


Figure 90: A.) Angled optical image of CNT interconnects grown on Cu daisy chains with CNT bundle tips coated with electrically conductive adhesive. B.)-E.) SEM images of various magnifications of similar CNT interconnects with adhesive coated tips. E.) Zoomed SEM image of electrically conductive adhesive, showing the Ag flakes and wicking of adhesive into the CNT forest.

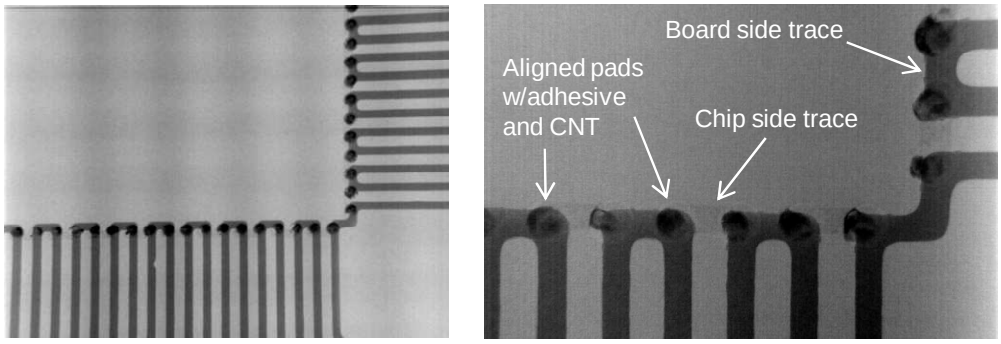


Figure 91: X-ray images of Si chip with Cu daisy chain and CNT interconnects aligned/assembled on FR4 with daisy chain pattern and adhesive. Dark Cu traces are substrate side, and light traces are chip side.

Several samples were assembled using this custom alignment/bonding tool and are shown in Figure 89. Additionally, the ability of the CNT interconnects to wet and wick the electrically conductive adhesive was investigated. The custom alignment/bonding tool was used to contact the tips of the CNT interconnect onto a flat surface coated with the electrically conductive adhesive, and then the sample with the CNT interconnects was retracted from the surface. These CNTs are shown under magnification in Figure 90, and show that the adhesive attached to and was wicked by the CNT interconnects. Also, to show that the packages have been assembled and aligned properly, x-ray imaging was performed. These x-ray images are shown in Figure 91 and are top-down magnified views illustrating that the daisy chain pads on the silicon chip are aligned with the copper pads of the FR4 substrate. This demonstrates proper alignment and assembly of the packages utilizing CNT interconnects that can next be thermal shocked for reliability tests.

8.8 Electrical Resistance Measurement of CNT Interconnects

The primary purpose of off-chip interconnects is to electrically connect devices and components of electronic systems to provide signaling and power for operation. Therefore, the electrical characteristics such as the inductance and resistance are a major design concern when investigating new electronic interconnects along with the mechanical reliability performance discussed in this thesis. The combination of electrical performance, mechanical performance, and manufacturability of traditional solder balls has allowed them to become the industry standard for this application. But, as mentioned in the Introduction Section 1.2.3 (CNT Forest Off-Chip Interconnects) of this thesis, some of these characteristics of lead-free solder balls are becoming difficult to maintain

as they are scaled down for newer packaging technologies. Ideally, new off-chip interconnect technologies aim to achieve the same electrical performance of solder balls, while improving reliability and scalability to smaller dimensions. For reference, the electrical resistance of lead-free solder balls is very low, with a DC resistance of ~0.7 mΩ, and for an example of another traditional alternative interconnect, there are also wire bond interconnects that have resistances of ~93 mΩ for a 0.8 mil thick wire [173]. The resistances for these interconnects are very low, and demonstrate why industry has gone to great lengths to continue their use in future applications.

To date, there have been several initial and first round investigations focusing on the experimental measurement of the electrical resistance of CNT forests for off-chip interconnects, and also for the similar structures of electrical vias, both with an extremely large range of reported values [63, 71, 72, 74, 76, 143, 172, 174-178]. Of these initial studies focusing on the electrical performance, the lowest reported resistance for a CNT forest interconnect is 2.2 Ω [76] and the highest is 300 kΩ [176], with more commonly reported resistances in the 10 Ω - 10 kΩ range. The specifics of these studies such as CNT growth parameters, CNT height, attachment method/type, and bonding force differed in these studies, but several studies demonstrated the importance of bonding force. Where an increase in force resulted in lowered interconnect resistance in the studies reporting the lowest resistances (~2 Ω) [63, 72]. The main goal of the investigation of CNT off-chip interconnects in this thesis was their mechanical reliability performance, and not improving their electrical resistance. The only electrical requirement for this study was that the CNT interconnects provided an electrical resistance measurement for the daisy chain circuit (Figure 74) in order to monitor their

reliability during thermal mechanical shock tests. With that stated, the lowest resistance measured in this study of a single daisy chain from the two successfully assembled flip chip packages with CNT interconnects, was 25.6 Ω measured from Sample A. This daisy chain resistance of 25.6 Ω consists of two separate CNT forest interconnects, and therefore an approximation for the resistance of a single CNT interconnect would be half of this measurement, and thus ~12.8 Ω. Additionally, the average resistance measured for the 80 daisy chains of Sample A was 103.2 Ω (~51.6 Ω for a single interconnect), and the lowest single daisy chain resistance of Sample B was 84.4 Ω, with an average of 184.2 Ω (~92.1 Ω for a single interconnect) for this test sample (electrical resistance measurements for the two flip chip packages are summarized and presented in Table 26). Therefore, the CNT off-chip interconnects fabricated and assembled with electrically conductive adhesive in this thesis are similar to those in electrical performance studies in current literature.

Table 26: Summary of initial electrical resistance values for the flip chips fabricated with CNT interconnects for thermomechanical reliability testing.

	Resistance (Ω)			
Sample	**Min. single daisy chain**	**Min. single interconnect**	**Avg. single daisy chain**	**Avg. single interconnect**
A	25.6	12.8	103.2	51.6
B	84.4	42.2	184.2	92.1

Additionally as a quick check, the electrical resistance of an assembled interconnect consisting of one CNT forest was calculated using the published values of electrical resistivity's for CNTs and conductive adhesive. An estimate of the theoretical electrical resistance for these CNT off-chip interconnects with electrically conductive

adhesive can be calculated using the fundamental relationship between electrical resistance, electrical resistivity, and the interconnect geometry. For a CNT bundle with a diameter of 100 µm, a height of 100 µm, and a CNT areal density of 5%, the CNT bundle resistance ranges from 0.25478 to 0.01274 Ω using a CNT electrical resistivity ranging from 1 Ω·µm [179] to 0.05 Ω·µm [180], respectively. Similarly, of the total electrical resistance of the interconnect attributed to the electrically conductive adhesive that has a diameter of 100 µm and a thickness of 12 µm is then 0.0612 Ω using an electrical resistivity of 0.05 Ω·µm of the Epotek H20E-PFC electrically conductive adhesive. Therefore the total theoretical resistance of the interconnect ranges from 0.316 - 0.074 Ω. This computed resistance is much less than the lowest measured resistance value of 12.8 Ω for the CNT based off-chip interconnects. The higher measured electrical resistance is due to various interfacial resistances such as the CNT/adhesive interface, adhesive/copper pad interface, and CNT/Cu-Al support layer interface. Therefore, there is scope for a significant amount of improvement in the fabrication and assembly to reduce the interfacial resistances, and thus, the overall interconnect resistance. For example, it would be possible to increase the bonding force during assembly since only ~1 N was used here compared to 40 N used in the literature that resulted in 2.2 Ω [76], and thus the overall resistance can be reduced. This assembly force provides room for further improvement of this investigation, but additionally work is required in the field of chemistry and material science focusing on how to attach these CNT forests to conducting metal traces to fully harness their phenomenal material properties, while maintaining the thermomechanical reliability benefits.

8.9 Thermomechanical Testing of Assembled Packages with CNT Off-Chip Interconnects

After the silicon chip with CNT off-chip interconnects was assembled with electrically conductive adhesive to an FR4 substrate, they were next subjected to cyclic thermal shock testing. The purpose of this test is to demonstrate the thermomechanical reliability benefits of the CNT off-chip interconnects. The reliability of an electronic device is defined as the probability that the device will be functional within an acceptable limit or quantity of time [181]. During this cyclic thermal shock testing, the reliability of the package with CNT interconnects will be tested by cycling the packages between thermal chambers with temperatures of 0°C and 100°C at a rate of three cycles per hour (Figure 92).

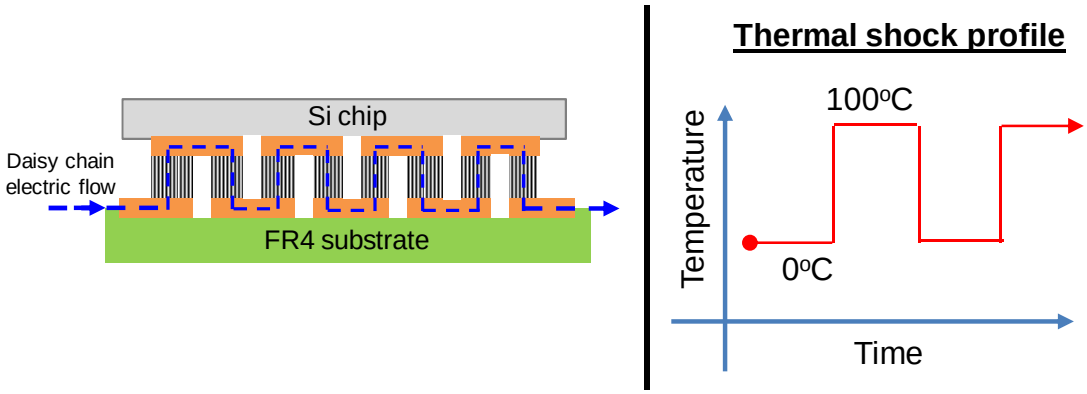


Figure 92: (left) Illustration demonstrating the daisy chain circuitry of the CNT interconnects that allow the interconnect integrity to be monitored during thermal shock testing. (right) Cyclic thermal shock testing that the test vehicle is subjected.

These conditions are based on those set by the Joint Electron Devices Engineering Council (JEDEC) in the JESD22-A104-B reliability test standard using a J thermal profile. Exposing the assembled package to these cyclic temperatures causes the silicon chip and the FR4 substrate to expand and contract different amounts due to the different CTE's of the materials (i.e. 3 ppm/°C for silicon and 11-17 ppm/°C for the substrate).

This difference causes thermomechanical stresses in the silicon die and interconnects leading to fracture or fatigue failures in flip chips during such thermal shock testing.

Table 27: Reliability results of thermal shock testing of electronic packages with CNT off-chip interconnects.

Test Sample	Daisy Chain #	Start Resistance (Ω) (cycle 0)		End Resistance (Ω) (cycle ~1660)	
		0^oC	100^oC	0^oC	100^oC
A	1	27.0	22.5	$9.9x10^{37}$	40k
	2	113.9	90.3	13k	160
	3	121.1	100.6	13k	290
	4	71.2	61.4	96	86
B	5	112.5	90.0	308	260
	6	11993.8	243.5	$9.9x10^{37}$	$9.9x10^{37}$
	7	197.5	146.3	$9.9x10^{37}$	$9.9x10^{37}$
	8	203.8	144.5	$9.9x10^{37}$	$2x10^6$

In this test, two assembled packages (Sample *A* and *B*) using CNT interconnects as described in Sections 8.2 to 8.5 were subjected to the thermal shock conditions. During the test, the electrical resistance of eight separate daisy chains (16 interconnects) was monitored insitu (as in Figure 92). The resistance measured for each of these daisy chains of the two test samples in the 0^oC chamber and 100^oC chamber during the first cycle, and then also during the last cycle of 1660 is listed in Table 27. During thermal shock testing, resistances consistently exceeding $1x10^{20}$ Ω were taken to be open circuits or complete failures of the individual daisy chains. As the daisy chains consist of CNTs attached with conductive adhesive, any measurable resistance shows that the daisy chain is not broken. Taking this as the failure criteria, it is seen that all four of the insitu monitored daisy chains of Sample *A* and two of the daisy chains of Sample *B*, have

successfully passed the thermal cycling test over 1600 cycles. The best performing interconnect during testing was #4 of Sample *A* that started with resistances of 71.2 Ω / 61.4 Ω and an ending resistances of 96 Ω / 86 Ω, and therefore very little change after the 1660 cycles. This interconnect, and the rest of Sample *A*, is a proof-of-concept that these CNT interconnects can survive many cycles once the assembly issues are improved. Comparatively, if these flip chips were assembled with traditional lead-free solder balls without underfill, they would not be able to survive as many cycles since the CTE mismatch between the silicon and FR4 substrate is too large. This is because the use of underfill was one of the main enabling technologies for flip chips with traditional solder ball at this scale [182]. Also, during reliability testing of flip chips using traditional solder balls and underfill, failures usually occur in the silicon and interconnects at locations where the underfill delaminates, thus illustrating the importance of underfill for reliability of traditional solder balls. Additionally, other reliability studies investigating new compliant interconnects such as the promising Flex Connect, completely failed at less than 143 thermal shock cycles of 0^{o}C-100^{o}C during initial tests [183]. Further research and investigations are necessary for this technology, but the survival of six out of eight of the insitu monitored daisy chains for the flip chips using CNT off-chip interconnects during these initial reliability tests shows promise for future pursuits using this technology.

To supplement these insitu results, resistance measurements were conducted by hand of all the 80 separate daisy chains for each of the two test samples at several intervals during the reliability test. The earlier insitu measurements of the interconnect resistance was limited since it only allowed 8 daisy chains to be monitored during

thermal shock testing. These additional hand measurements of all the daisy chains provide an overall impression of the CNT interconnect reliability for each of the samples to support the smaller sample size of the insitu measurements of Table 27, and the results are summarized in Table 28. The Table 28 shows that initially Sample *A* has 100% of the 80 daisy chains working (i.e. resistance less than $1x10^{20}$ Ω) and Sample *B* has 92.5%. Then near the completion of the thermomechanical testing at 1247 cycles, Sample *A* has 77.5% and Sample *B* has 30% of the daisy chains working. Therefore, the majority of failures occurs during the early stages of thermal cycles, and remains relatively consistent at higher cycles. As mentioned earlier, these early failures are most likely due to assembly issues that can be addressed in subsequent studies to improve results.

Table 28: Thermomechanical reliability test results. Lists percentage of working interconnects out of all the interconnects of Samples A and B at various stages of testing.

	Cycle: 0	**Cycle: 478**	**Cycle: 1247**
Sample	**% of Interconnects Working**	**% of Interconnects Working**	**% of Interconnects Working**
A	100	86.25	77.50
B	92.5	35	30

These results of Table 28 support the insitu results of Table 27 by increasing the amount of daisy chain resistances measured during thermal cycling and therefore aid in the proof-of-concept of utilizing CNT interconnects to improve the thermomechanical reliability of flip chips without underfill. With increased experience with CNT fabrication, conductive adhesive dispensing, and assembly process development, more samples need to be prepared and validated before additional definitive conclusions can be drawn on CNT interconnect thermomechanical reliability.

8.10 Conclusion

In this chapter the fabrication, assembly, and thermomechanical reliability testing of electronic packages utilizing CNT off-chip interconnects was demonstrated and discussed. First the fabrication details were presented to create the silicon test chips with copper daisy chains patterned on the silicon's surface. Also, the CNT growth recipe was developed, showing how to grow vertically aligned CNT forests on the copper daisy chains with bundle diameters of ~100 μm and pitches of ~200 μm. Interconnects with these dimensions were chosen due to their relevance to current industry pursuits in electronic packaging. Next, the equipment and procedures required to stencil electrically conductive adhesive on custom designed FR4 substrates, along with custom fixtures to accurately assemble and align the flip chip with CNT interconnects onto the FR4 substrate was created. This assembled flip chip test vehicle allowed for accelerated thermal shock tests to demonstrate the thermomechanical reliability benefits of CNT interconnects. The tests showed that 6 of the 8 insitu monitored daisy chains with CNT interconnects survived ~1660 thermal shock cycles. These values are much higher than what is achievable for similar flip chip packages utilizing lead free solder balls without underfill, and therefore the CNT interconnects demonstrate future potential mechanical benefits from this initial proof-of-concept study. Additionally, while this chapter focused on the mechanical performance of the CNT interconnects, measurements were conducted on the electrical resistance of the CNT off-chip interconnects created for these tests. These resistance measurements obtained for the CNT interconnects were relatively low for CNTs and similar to other studies conducted in literature focusing on characterizing the electrical performance of CNT interconnects. In summary, this chapter presented

some of the first quantitative results of the thermomechanical reliability benefits that CNT interconnects offer, and provides a proof-of-concept since further research is needed to improve results. These results also support the FEA studies performed on similar electronic packages presented in Chapter 7. It is the hope that this research on the fabrication, assembly, and experimental reliability of CNT off-chip interconnects extends current research and supports future endeavors in research to develop CNTs for interconnect applications.

CHAPTER 9

RESEARCH CONTRIBUTIONS, SUMMARY, AND FUTURE WORK

9.1 Research Contributions

This thesis has made a number of research contributions, as outlined below. This work has:

- Developed a new test method to measure the tensile strength of low modulus thin films. This method utilizes a highly-stressed superlayer material to cause failure of the target test material. This work has demonstrated this test method by measuring the tensile strength of parylene-C polymer.
- Developed a new fixtureless experimental test technique for measurement of thin film cohesive fracture resistance using a stressed superlayer. The test development included designing three photolithography masks and creating the cleanroom fabrication instructions detailing the material deposition, photoresist patterning, thin film etching, and thin film release process.
- Generated cohesive fracture resistance data for SiO_2 thin films using the new cohesive fracture test method. Utilized the test method to measure the cohesive fracture resistance of five different silicon dioxide test material thicknesses ranging from ~100 nm to ~400 nm. Fracture data obtained in this study was in agreement with reported values in literature.
- Developed a finite-element model to mimic the innovative aspects of the test technique including the varying superlayer width due to the triangular shape of

the superlayer as well as the 3D nature of stress fields around the tearing crack propagation.

- Developed a nanoindenter based test method to measure the effective modulus of CNT forests. Demonstrated the test method by measuring the effective modulus of CNT forests of three different heights.
- Developed a test method to measure the effective modulus of CNT forests using a SEM with custom compression fixture and loadcell. The test method allowed semi-insitu observation of the deformation of the CNT forests under compressive loading. The test method was utilized to generate data for values of CNT forest effective modulus and images of CNT forest deformation at various levels of compression.
- Generated test data for effective modulus of CNT forests in tension with the use of tensile load frame method.
- Developed an assembly process for flip chips on organic substrates with CNT-based interconnects and has shown that such flip chips will have low stress, low warpage, and will last several hundred thermal cycles without the need for an underfill material. To facilitate CNT interconnect assembly, this work designed and fabricated pico-motor controlled z-axis alignment stage with loadcell.

9.2 Research Findings and Summary

This work has shown that stress-engineered superlayer can be successfully used to measure fracture strength of polymer and oxide materials. In particular, this work has:

- Shown that the tensile strength of parylene-C thin film is 57 MPa using a new test technique, and that this value is within the range reported in literature.
- Shown that critical energy release rate of thin film SiO_2 is 8.89 J/m^2 – 13.99 J/m^2 (with an average value of 11.3 J/m^2), and this value is within the range measured by conventional techniques. The advantage of the proposed technique is that it does not use fixtures, and thus, can be used for nano-scale SiO_2 where fixturing and load application can be a challenge.
- Shown that by decreasing available energy release rate by suitably patterning the superlayer, crack propagation can be arrested, and thus, critical energy release rate can be obtained.
- Shown that the modulus of CNT forests under compression as well as tension is in the range of 0.11 to 1.2 MPa through various test techniques, and has shown that this value is several orders of magnitude lower than the modulus of individual straight CNT.
- Developed a finite-element model that accounts for the orthotropic nature of the CNT interconnects, and has shown that CNT off-chip interconnects greatly reduce the stresses (~94-71%) in the silicon chip compared to traditional solder ball interconnects. Additionally it was found in the CNT interconnect scenario, that the volume of the silicon chip subjected to elevated thermomechanical stress levels is greatly reduced compared to the scenario utilizing solder balls, and further mitigating possible cohesive cracking of dielectric layers.

- Shown that it is possible to grow well-aligned vertical CNT forests on copper thin film daisy chains where CNT interconnects had a diameter of ~120 μm, height of 75-150 μm, and a pitch of ~200 μm.
- Shown that it is possible to align and assemble silicon chips with CNT daisy chains onto FR4 substrates with a complimentary daisy chain pattern. Electrically conductive adhesive was patterned on FR4 substrate to adhere CNT interconnects to the daisy chain of the FR4 substrate.
- Shown that the electrical resistance of assembled CNT daisy chain is ~12.8 Ω for a single CNT interconnect. This value is similar to those reported in literature focusing on the electrical characteristics of CNT interconnects.
- Subjected assembled flip chips with CNT interconnected to accelerated thermal shock testing while monitoring interconnect daisy chain resistance to obtain a quantitative measure of the mechanical performance of an electronic package with CNT interconnects. Thermal shock reliability testing of flip chips with CNT interconnects showed that 6 of the 8 monitored daisy chains with CNT interconnects survived 1660 thermal shock cycles. These values are much higher than what is achievable for similar flip chip packages utilizing lead free solder balls without underfill, and therefore the CNT interconnects demonstrate future potential mechanical benefits.

9.3 Future Work

- Utilize cohesive fracture test to measure fracture resistance of different materials such as aluminum oxide, silicon nitride, carbon doped silicon dioxide, hafnium oxide, or titanium oxide.

- Investigate different superlayer planar geometries besides a triangular shape, such as curved tapered geometries.
- Investigate measuring the elastic modulus of a thin film using a similar structure of a free hanging test material film with a stressed superlayer film deposited on top of it by measuring the resulting radius of curvature of the test structure. Either the elastic modulus of the test material or the elastic modulus of the superlayer film may be measured with this method.
- Perform different thermomechanical tests on flip chip packages utilizing CNT interconnects. Such as four-point bend testing with strain gauges attached to the silicon chips or digital image correlation of the edge of the silicon chip to observe the chip strains in-situ.
- Perform additional nanoindentation measurements of effective mechanical properties of CNT forests in directions perpendicular to the growth direction and effective shear modulus values.

APPENDIX A

APPENDIX

A.1 Clean Room Processes

A.1.1 Shipley® 1827 Photoresist Recipe

1. Using photoresist spin coater (ex. SCS G3 Spin Coater or CEE100CB Spinner) coat substrate with photoresist using the following spin parameters:
    a. Maximum spin speed - 3000 rpm
    b. Ramp rate - 1000 rpm/s
    c. Spin time - 35 seconds.
2. Soft-bake photoresist on hotplate:
    a. Temperature – 115^{o}C
    b. Time – 3.5 minutes
3. Using mask aligner (ex. Karl Suss MA6) expose photoresist using the following parameters:
    a. Wavelength – 405 nm (channel 2 on MA6)
    b. Exposure time – 16 seconds (calculated time was 11 seconds based on a dose of 220 mJ/cm^2 and lamp intensity, but mask absorption causes the need for longer exposure times)
4. Develop photoresist using MF-354 for ~35 seconds, the development process can be observed while the sample is in the developer liquid. (MF-354 can be created from MF-351 by diluting with water at a ratio 3.5:1). Rinse wafer and developed photoresist in DI water.

5. Hard-bake photoresist on hotplate:
    a. Temperature – 115^{o}C
    b. Time – ~3.5 - 5.0 minutes (baking time depends on the harshness of the subsequent etchant that will be used, more severe etchants may require longer times at the risk of being more difficult to remove later)
6. If performing a wet etching process, run a short ~20 second oxygen plasma descum process with the Plasma Therm RIE. Cleaning with a descum process helps create more consistent etch times and even wet etches.
7. Expected photoresist thickness is about 2.7 μm.

A.1.2 Futurrex® NR9-1500PY Photoresist Recipe

1. Using photoresist spin coater (ex. SCS G3 Spin Coater or CEE100CB Spinner) coat substrate with photoresist using the following spin parameters:
    a. Maximum spin speed - 3000 rpm
    b. Ramp rate - 1000 rpm/s
    c. Spin time - 40 seconds.
2. Soft-bake photoresist on hotplate:
    a. Temperature – 150^{o}C
    b. Time – 1.0 minutes
3. Using mask aligner (ex. Karl Suss MA6 TSA) expose photoresist using the following parameters:
    a. Wavelength – 365 nm (channel 1 on TSA)
    b. Exposure time – 4.5 minutes for copper and 1 minute for other materials (calculated time was 28 seconds based on a sensitivity of 190 mJ/cm^2 per

1 μm of thickness and a lamp intensity of 10 mW/cm^2, but mask absorption and the case of patterning on copper, the reflectivity of copper causes the need for much longer exposure times)

4. Hard-bake photoresist on hotplate:
    a. Temperature – 100^{o}C
    b. Time – ~1.0 minutes
5. Develop photoresist using RD6 for ~12-20 seconds, the development process can be observed while the sample is in the developer liquid. Rinse wafer and developed photoresist in DI water.
6. Since this is a negative resist, it is necessary to clean off the areas that do not have photoresist on them since material will be deposited here for a lift-off process. Therefore, run a short ~30 second oxygen plasma descum process with the Plasma Therm RIE.
7. Expected photoresist thickness is about 1.2-1.4 μm

A.1.3 Plasma Therm RIE Descum Process Parameters

Table 29: Plasma Therm RIE Descum Process Parameters

Parameter	Value
Chamber Pressure	204 mTorr
Process Gas – O_2	35 sccm
Plasma Power	200 Watts

A.1.4 Stencil Squeegee Parameters

Table 30: Stencil Squeegee Parameters

Parameter	Value
Print Force	8.1 kg (tested range of 4-20 kg)
Squeegee Speed	10 mm/s
Stencil Disp.	1.57 mm

A.2 Supplementary Cohesive Fracture Images

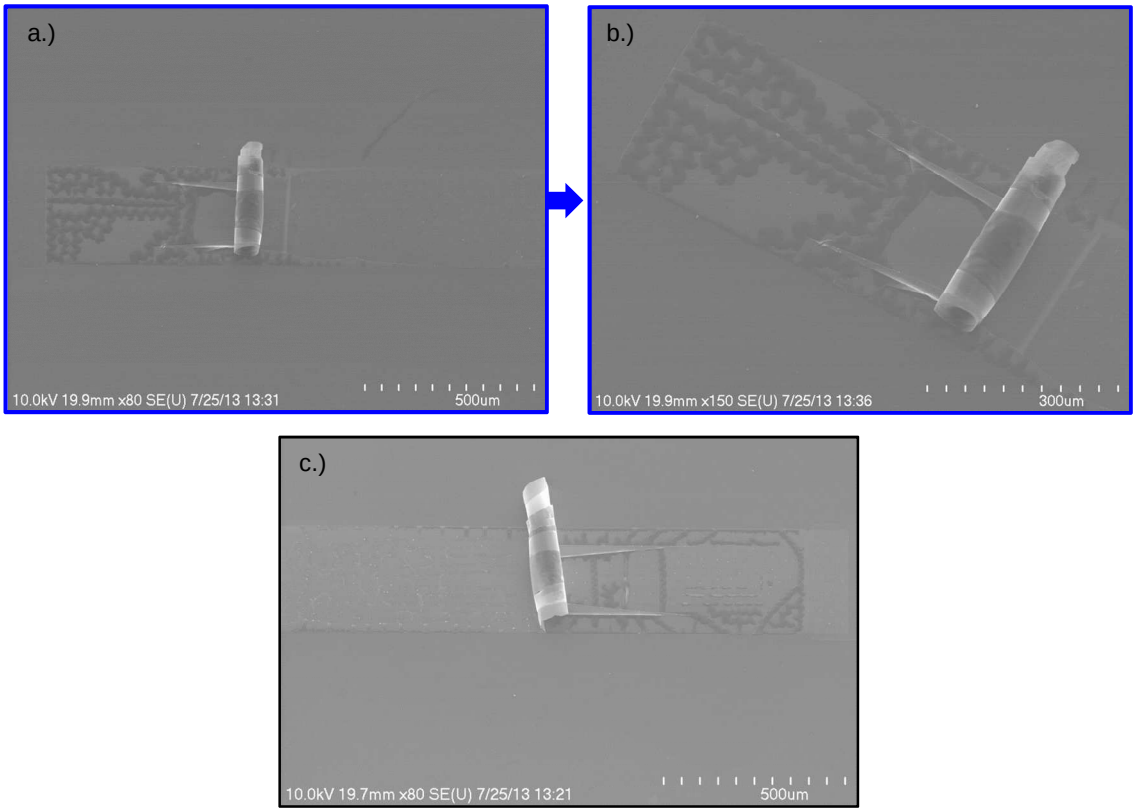


Figure 93: SEM images of Sample #2. Top two images are of the same test sample at different magnifications. Bottom image is of a different test sample.

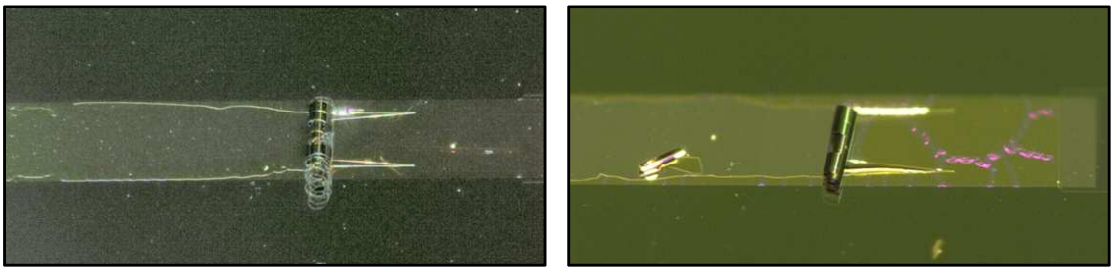


Figure 94: Optical images of two different test samples from Sample #2.

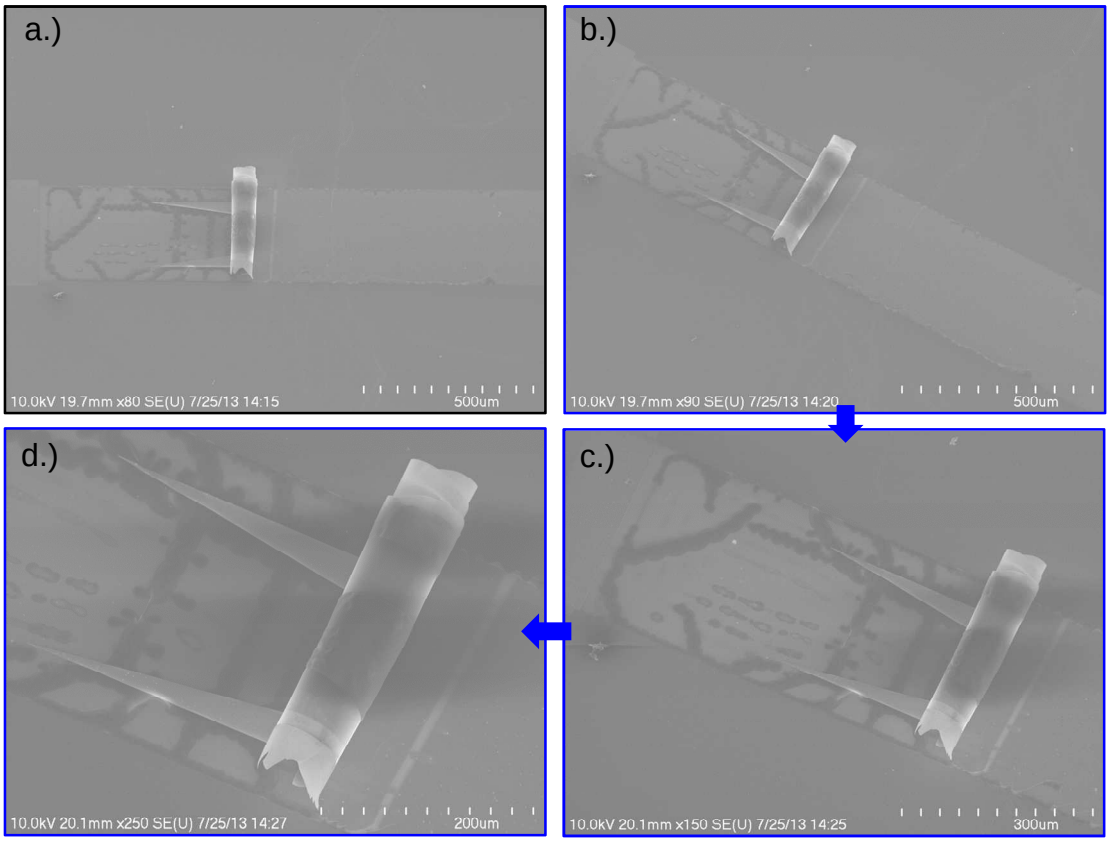


Figure 95: SEM images of various magnifications of the same test sample of Sample #2. Images a.) and b.) show the full test sample with the cracked and un-cracked sections. Where the cracked section shows the bare silicon, and the un-cracked section shows the remaining free-hanging silicon dioxide test material. Images c.) and d.) show increased magnification views of the curled test material and un-cracked sections of the test material.

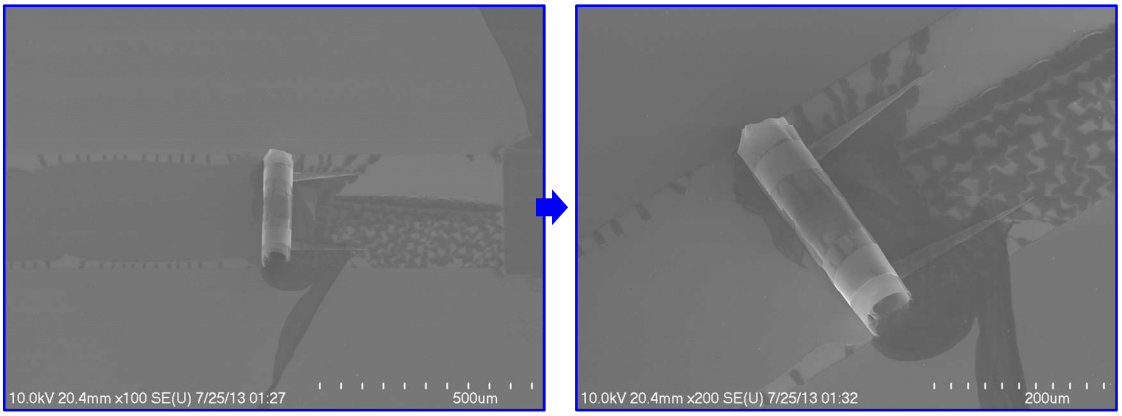


Figure 96: SEM images of a single test sample of Sample #3 of various magnifications.

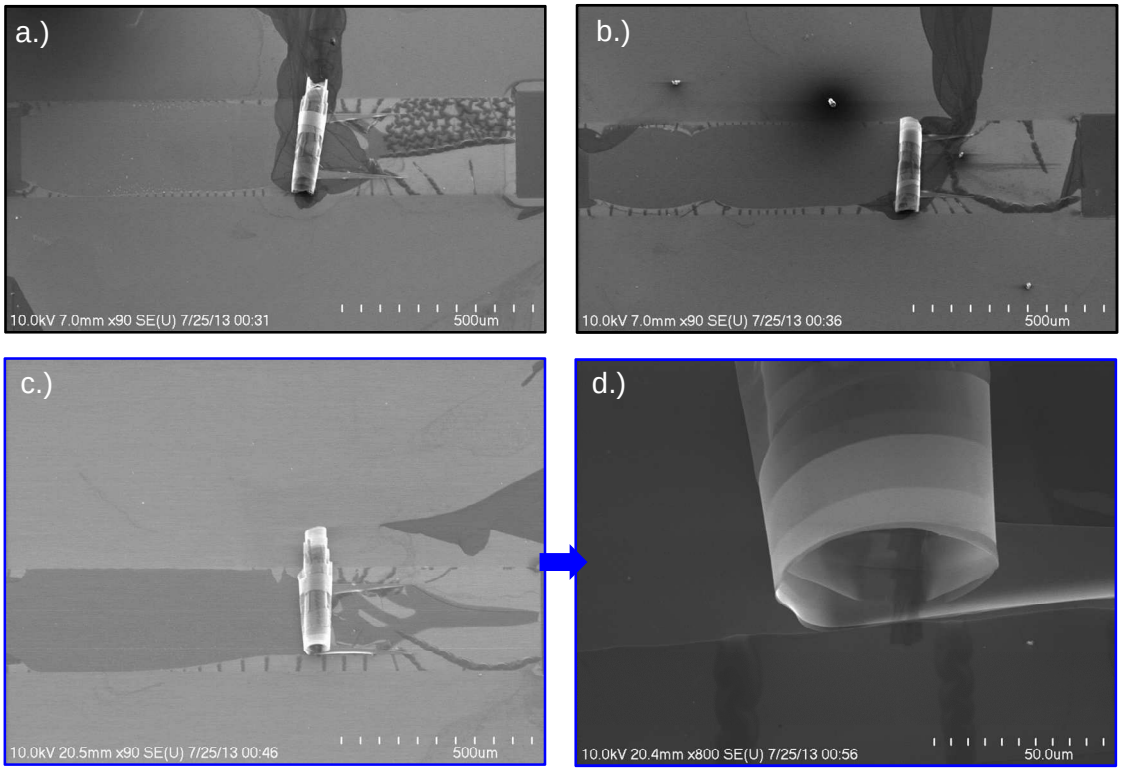


Figure 97: SEM images of three different test samples from Sample #3. Images c.) and d.) are of the same test sample at different magnifications.

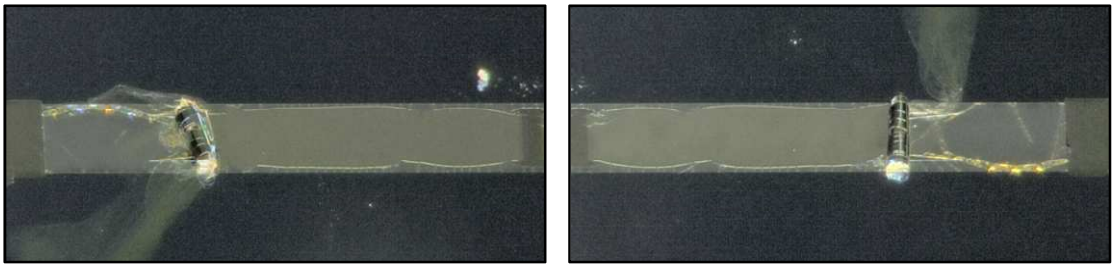


Figure 98: Optical microscope images of two different test samples from Sample #3. Images show the full test sample including the cracked portions and un-cracked portions of the test material.

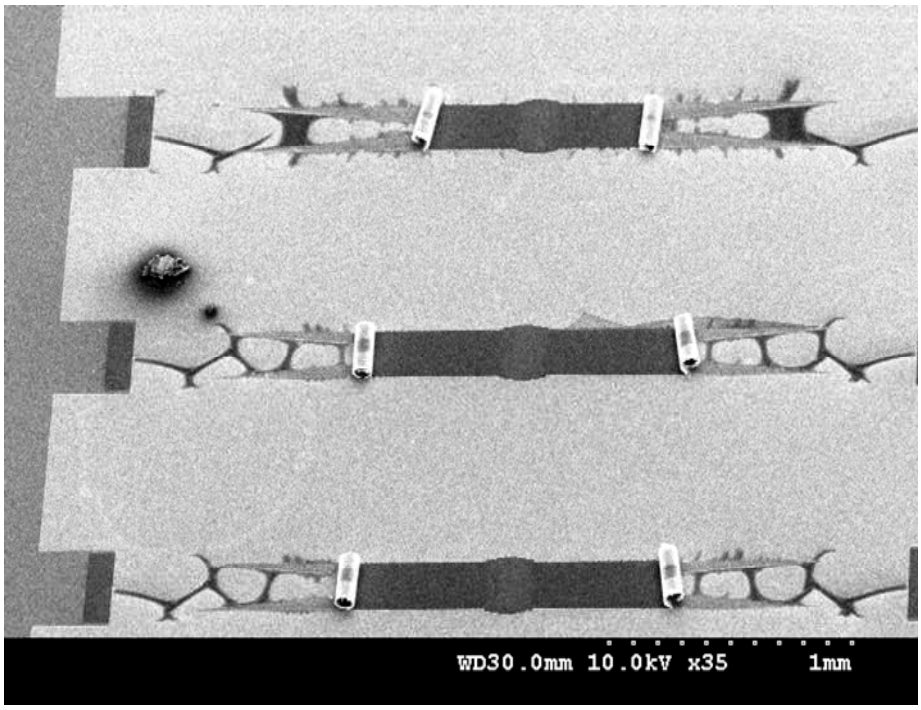


Figure 99: SEM images of top down view of finished test strips of Sample #4. Image shows three separate test strips, giving a total of six test samples, where each strip consists of two test samples with cracks propagating in opposite directions. Dark rectangular areas are the bare silicon substrate that was covered with free-hanging silicon dioxide test material before crack initiation and curling.

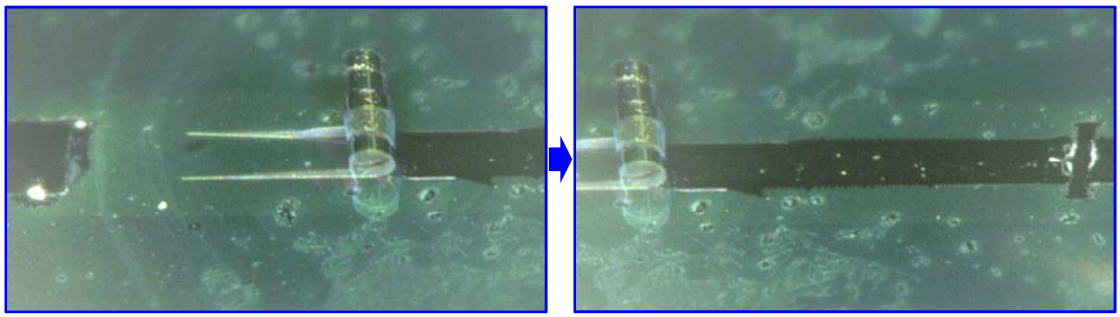


Figure 100: Optical microscope images of a single test sample of Sample #5. The left image shows the un-cracked portion, the test material and superlayer curl, and some of the cracked portion. The right image shows the entire cracked portion and the test material and superlayer curl.

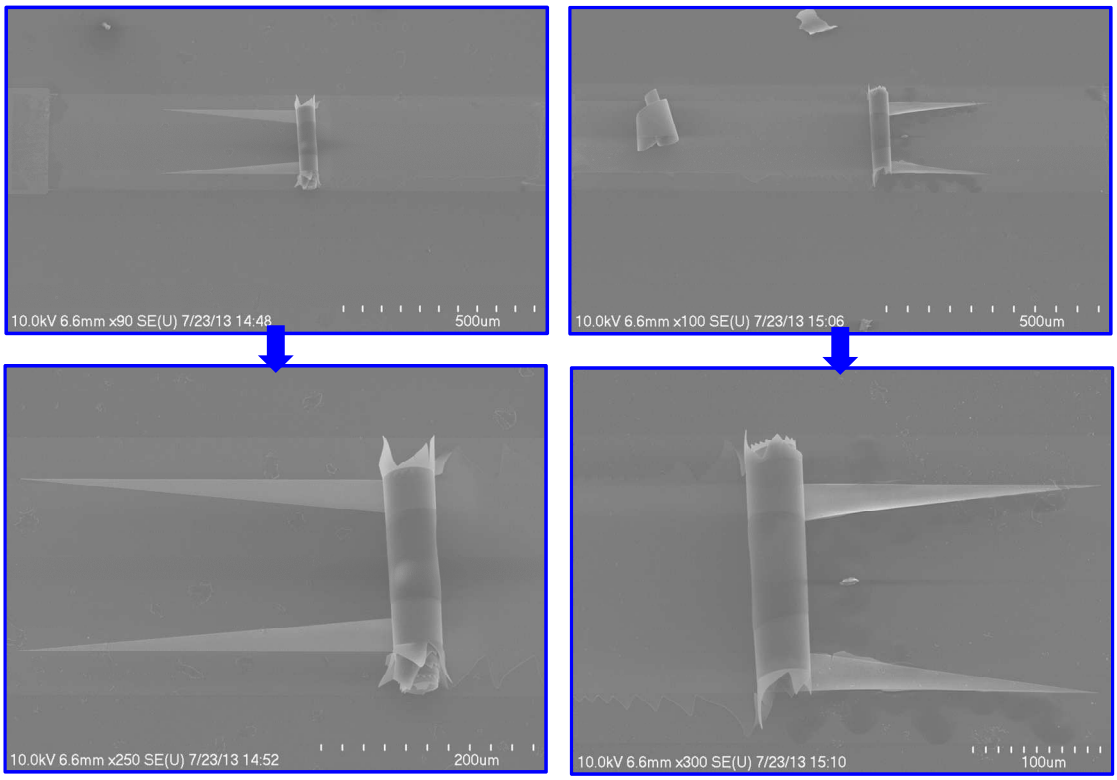


Figure 101: The top two images show SEM images of two different test samples of Sample #5. The two lower images are higher magnification images of the respective test samples.

A.3 Nanoindentation of Silicon Dioxide and Chromium Films

A.3.1 Introduction: Young's Modulus Measurement

After the experimental aspect of this new cohesive fracture measurement technique has been completed, it is necessary to perform finite-element analysis of the experimental situation in order to calculate the fracture resistance of the test material. To create the most accurate finite-element analysis of the experimental fracture results and to demonstrate this technique, the Young's modulus of the test material and of the superlayer need to be measured for use in the finite-element analysis. The Young's modulus of the test material and of the superlayer was therefore measured by utilizing a nanoindenter system. The Young's modulus of thin films can be easily measured with a nanoindenter, and therefore one was utilized here.

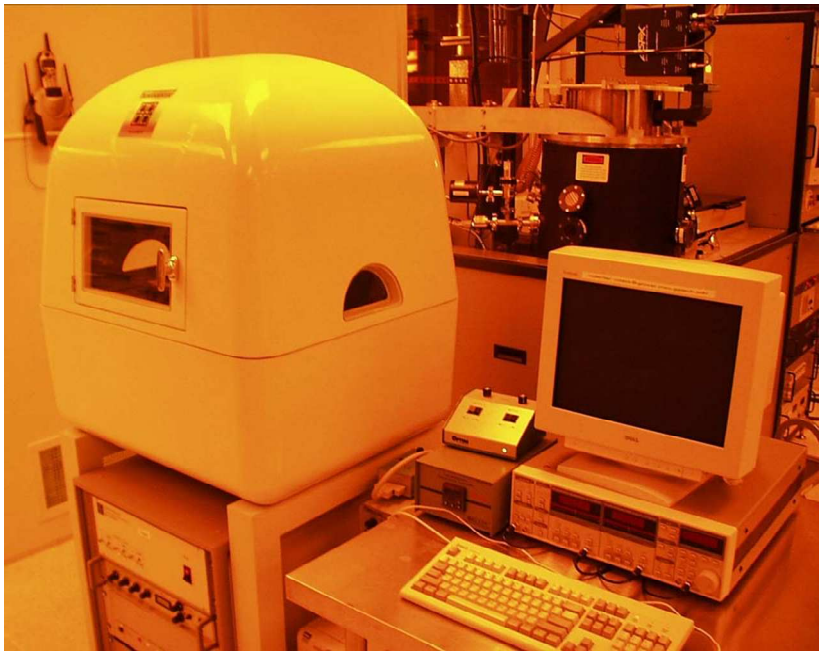


Figure 102: Hysitron nano indentation system owned and maintained at Georgia Tech IEN.

A.3.2 Nanoindenter Sample Preparation

Thin film samples of both the test material and the superlayer were prepared on separate silicon wafers of a thickness of ~500 µm. The test material used was silicon dioxide and was deposited using a Unaxis® PECVD and the deposition parameters used are listed in Table 31. Similarly, the material used as the superlayer is a thin film of chromium deposited using a Unifilm® magnetron sputtering system and the sputter deposition parameters include a deposition rate of 500 Å/m with a pressure of 5 mTorr. The deposition parameters used for these test specimens were the same as those used in the fracture toughness technique in order to provide a representative material to obtain the young's modulus from. Three samples were created with thicknesses of 100, 200, and 500 nm for each material and all were measured with the nanoindenter. This was done to capture any differences in the nanoindenter measurement due to material thickness and/or substrate interaction.

Table 31: Unaxis® PECVD Parameters

Temperature (^{o}C)	250
Pressure (mTorr)	900
SiH_4 Flow Rate (sccm)	400
N_2O Flow Rate (sccm)	900
Power (watts)	25

A.3.3 Nanoindenter Results: Silicon Dioxide and Chromium

The nanoindenter system used for these measurements was a Hysitron® system maintained by the Georgia Tech IEN with a Berkovich tip. The data collected by the Hysitron® system is also analyzed by the Hysitron® analysis software that calculates

material hardness and modulus based on the theories of Doerrer and Nix & Oliver & Pharr [184]. For each sample of a certain thickness, nine separate indents were performed on the thin film with increasing peak loads for each sample. This then allowed the entire sample set to cover a specified peak force range (different for each sample material and thickness), and consequently a resulting indent depth range as well. Then an area function was applied to these series of indents in order to calculate the reduced modulus for each indent. The coefficients for this area function were determined by a similar series of indents of a standard quartz calibration specimen. Using this area function to calculate the reduced modulus of quartz yielded 66.3 GPa, compared to the expected value of 69.6 GPa. Figure 103 and Figure 105 show the force verse displacement results for one of the silicon dioxide and chromium samples respectively. Additionally, Figure 104 and Figure 106 show the calculated reduced modulus vs. peak depth for the nine different indentations performed for each of these samples. The remaining data for the other silicon dioxide and chromium samples are located in Table 32 and Table 33. Using all of the measured values from each sample, the average reduced modulus for the PECVD silicon dioxide is 82.39 GPa. The Young's modulus of the film is then calculated using the below equation and the mechanical properties of the diamond Berkovich tip (E_{tip} = 1140 GPa, ν_{tip} = 0.07) [184]:

$$\frac{1}{E_r} = \left(\frac{1-\nu^2}{E}\right)_{speciman} + \left(\frac{1-\nu^2}{E}\right)_{tip} \quad (23)$$

Using $\nu_{specimen}$ = 0.17 [77], the measured Young's modulus of the PECVD SiO_2 is then 86.21 GPa. This is very similar to reported values that range from ~69-83 GPa depending on deposition method and parameters [77, 102, 103, 105, 185]. Similarly the

average reduced modulus of the magnetron sputtered chromium is 137.64 GPa, and using $\nu_{specimen}$ = 0.21 [105] the Young's modulus is then 149.54 GPa and is within reported values. These reported values for Cr vary greatly depending on deposition techniques and deposition parameters, ranging from ~107-280 GPa [105, 186-192]. This large range of values highlights the need to measure the Young's modulus of the specific Cr films used in this fracture technique.

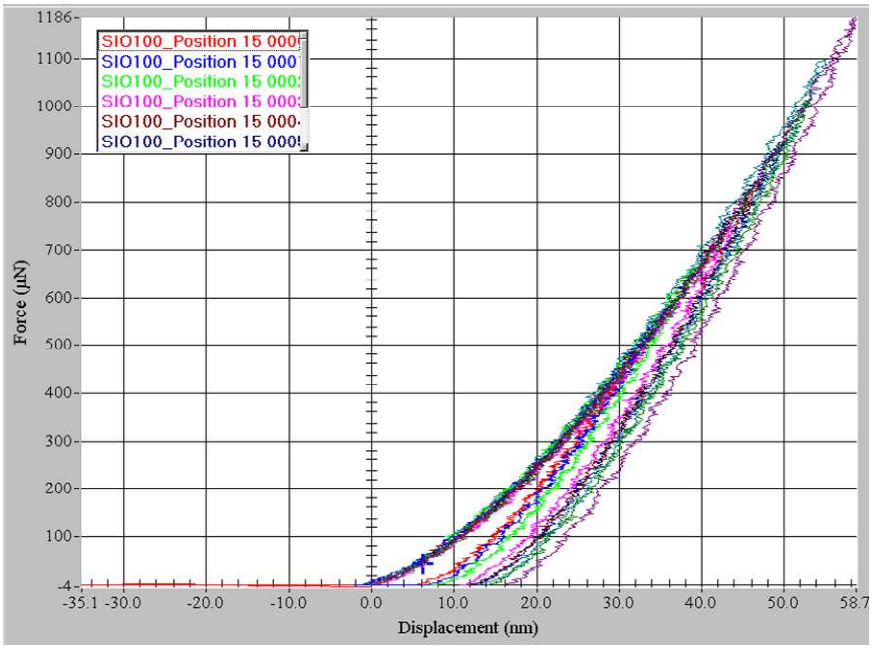


Figure 103: Force vs. Displacement data for 100 nm SiO_2 showing nine different indents each with increasing maximum peak loads and maximum peak indent depths.

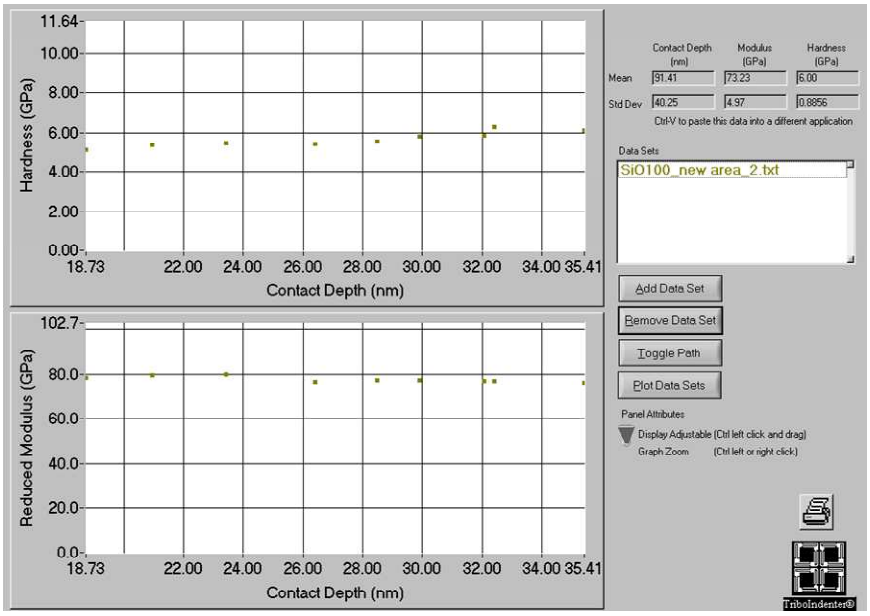


Figure 104: Calculated hardness and reduced modulus from the force vs. displacement data for 100 nm thick SiO_2. Graph shows the reduced modulus calculated from each of the nine different indents, each with a greater peak indent depth than the previous.

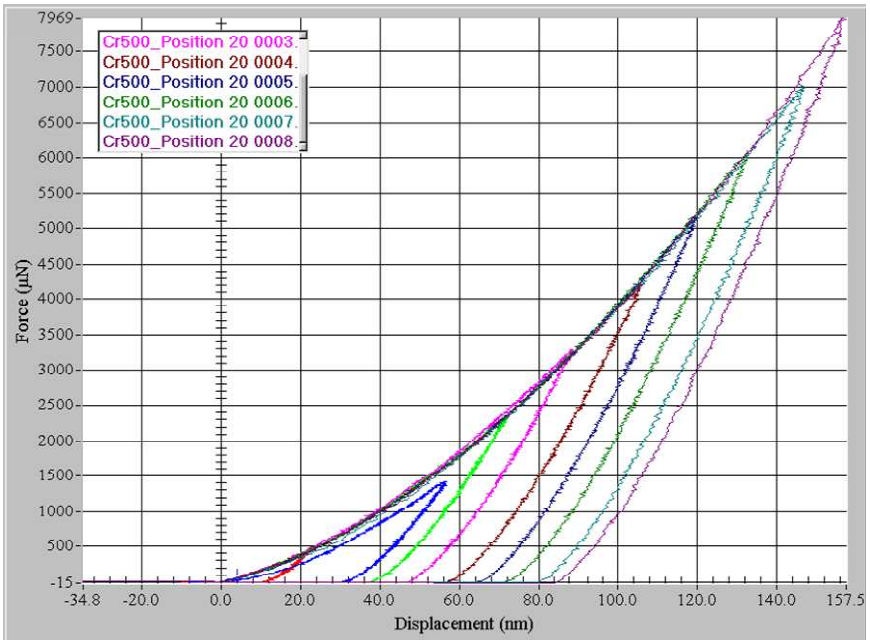


Figure 105: Force vs. Displacement data for 100 nm Cr showing nine different indents each with increasing maximum peak loads and maximum peak indent depths.

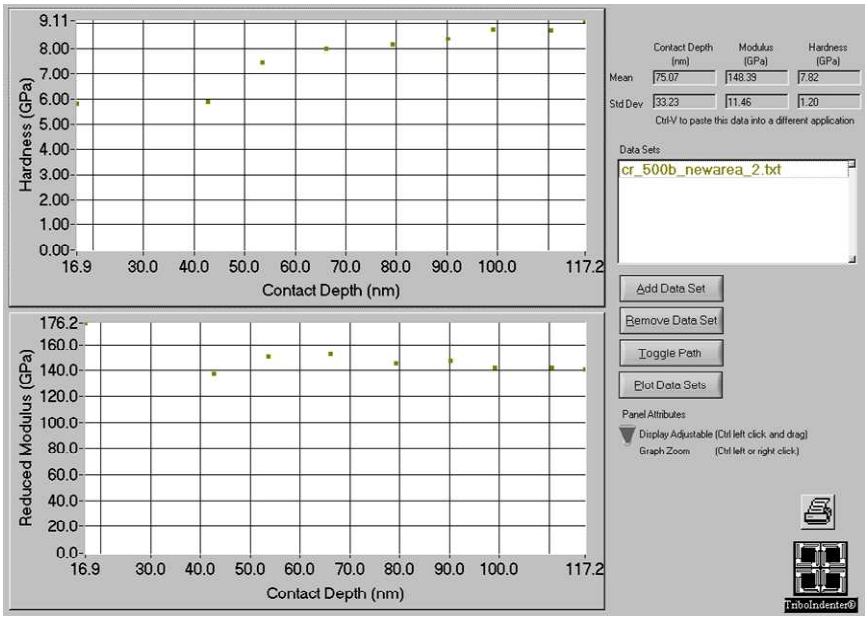


Figure 106: Calculated hardness and reduced modulus from the force vs. displacement data for 100 nm thick Cr. Graph shows the reduced modulus calculated from each of the nine different indents, each with a greater peak indent depth than the previous.

Table 32: Nanoindenter data for SiO_2 samples

Film Thick. (nm)	# Indents	Indent Depth Range (nm)	Indent Force Range (μN)	Red. Modulus Range (GPa)	Avg. Young's Modulus (GPa)
100	9	18.8-25.4	486-1184	76.29-79.89	80.92
200	9	18.9-68.9	483-2972	82.93-108.07	102.03
500	9	22.8-142.5	484-7952	62.24-77.81	75.97
Tot. Avg.					**86.21**

Table 33: Nanoindenter data for Cr samples

Film Thick. (nm)	# Indents	Indent Depth Range (nm)	Indent Force Range (μN)	Red. Modulus Range (GPa)	Avg. Young's Modulus (GPa)
100	9	12.95-37.58	489-1984	109.10-134.06	126.85
100	9	12.71-36.74	492-1984	109.86-135.26	125.24
200	9	15.44-78.53	490-4973	134.18-147.05	153.82
200	9	14.49-74.34	490-4972	145.73-154.13	161.74
500	9	17.99-119.11	491-7969	143.65-154.35	168.07
500	9	16.89-117.23	492-7969	141.19-176.19	162.95
Tot. Avg.					**149.54**

A.4 Engineering Drawings

A.4.1 SEM Compression Fixture

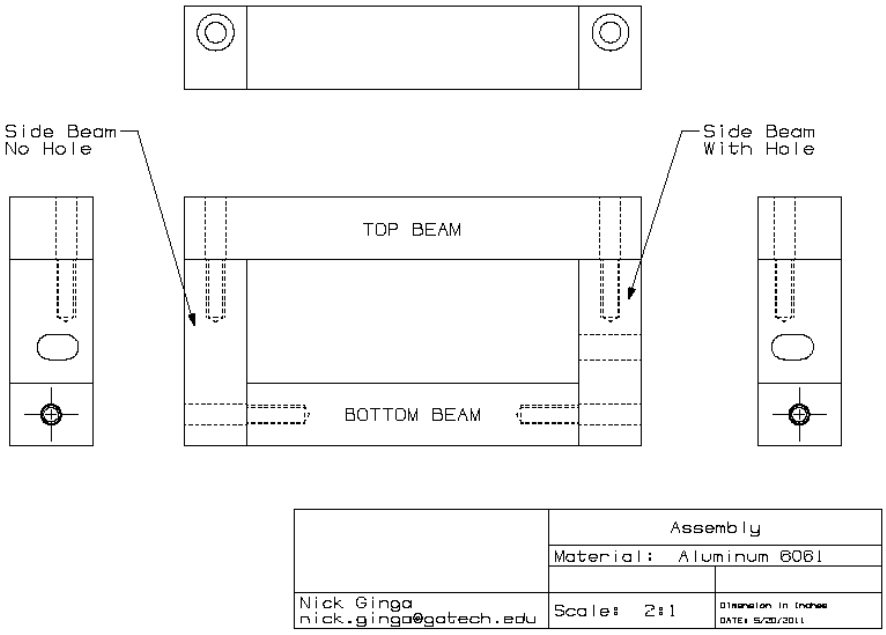


Figure 107: SEM Compression Fixture: Assembled

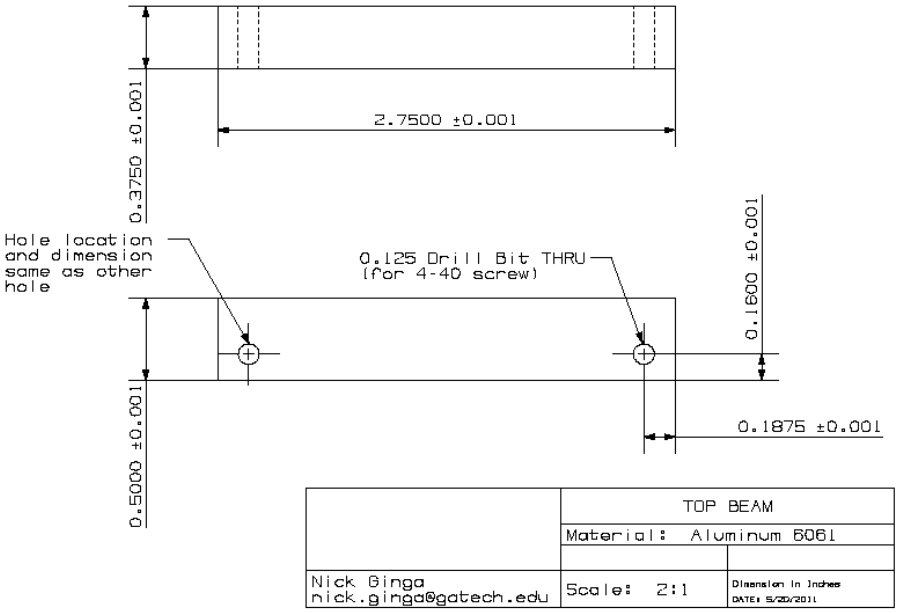


Figure 108: SEM Compression Fixture: Top Beam

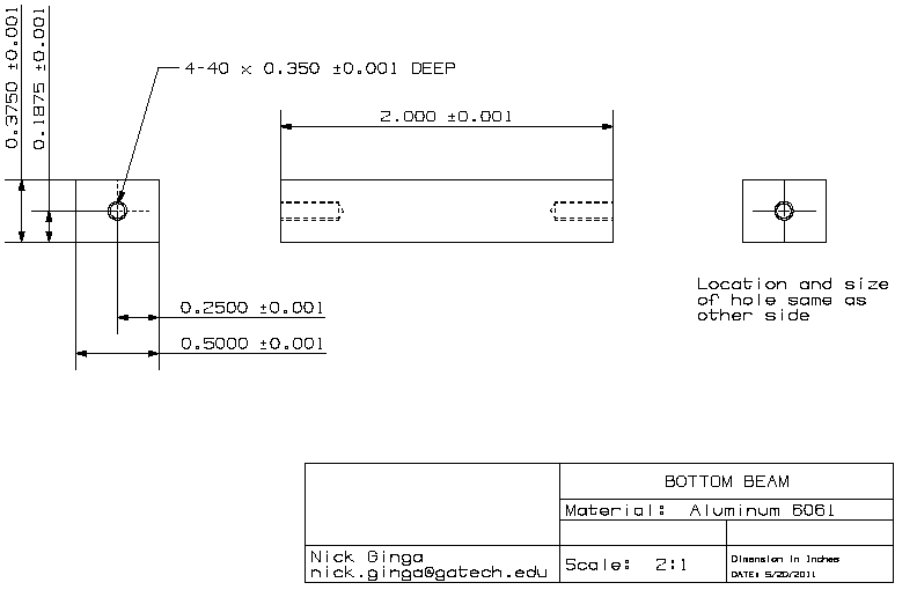


Figure 109: SEM Compression Fixture: Bottom Beam

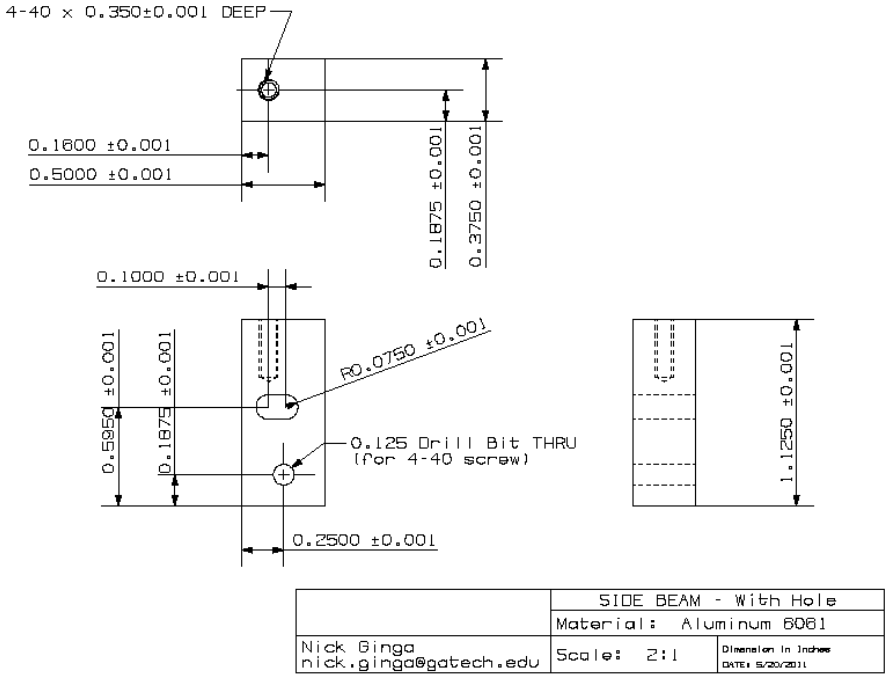


Figure 110: SEM Compression Fixture: Bottom Beam Hole

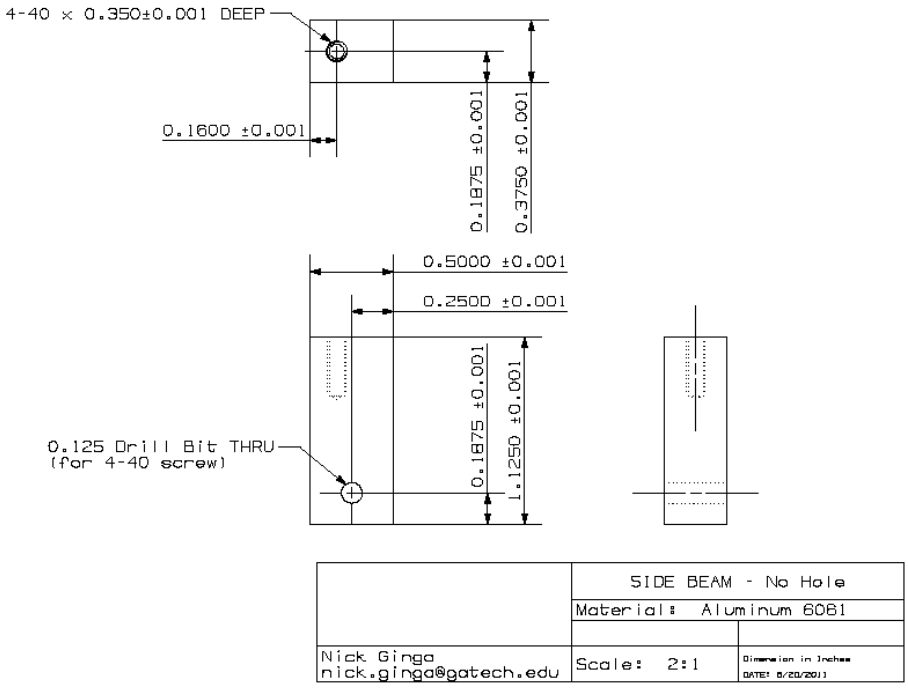


Figure 111: SEM Compression Fixture: Bottom Beam No Hole

A.4.2 CNT Assembly Fixture

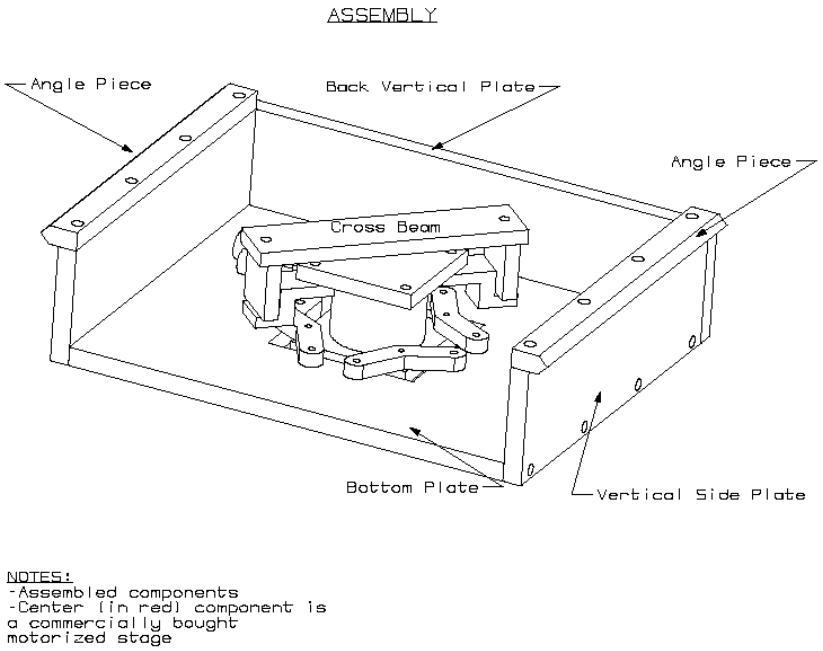


Figure 112: CNT Assembly Fixture: Assembly

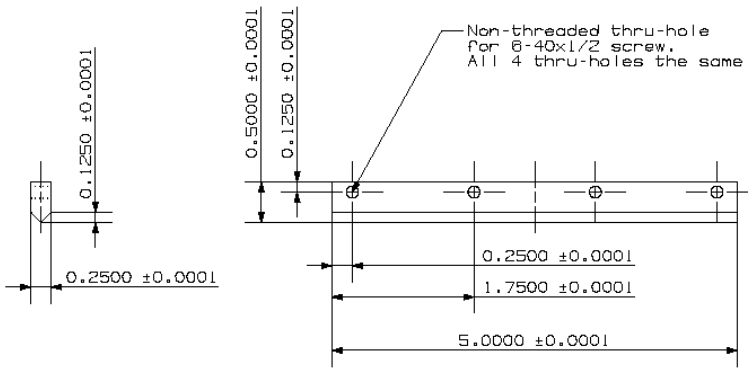


Figure 113: CNT Assembly Fixture: Angle Piece

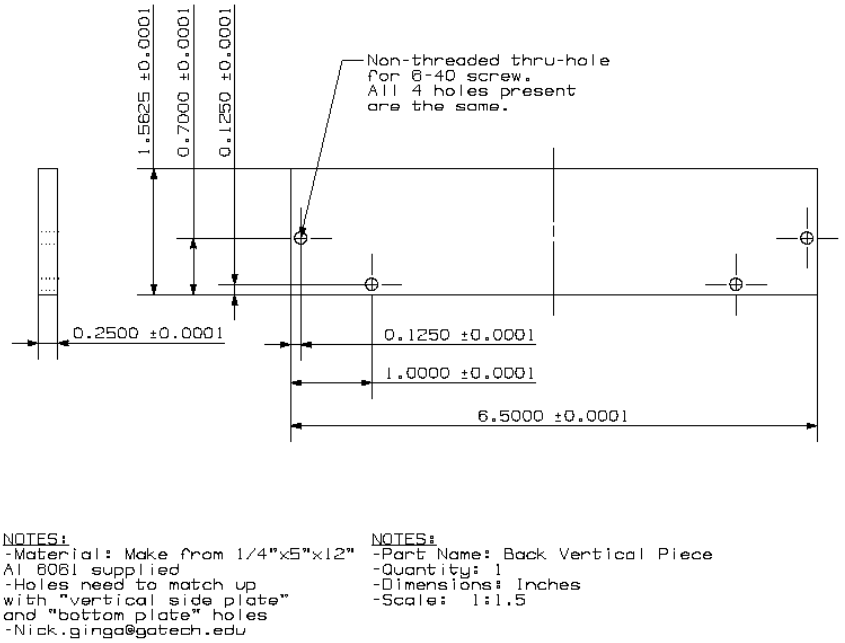


Figure 114: CNT Assembly Fixture: Back Vertical Plate

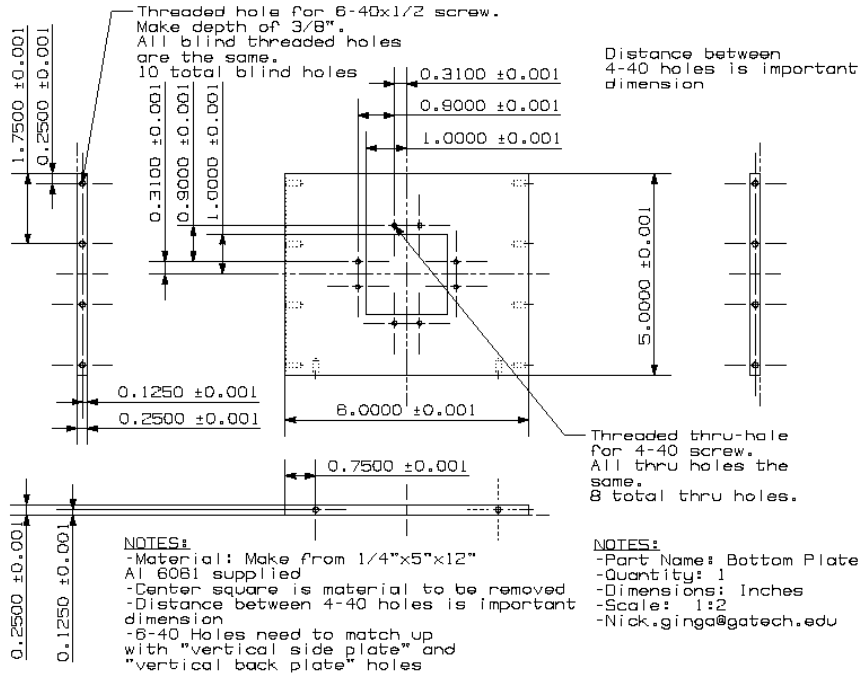


Figure 115: CNT Assembly Fixture: Bottom Plate

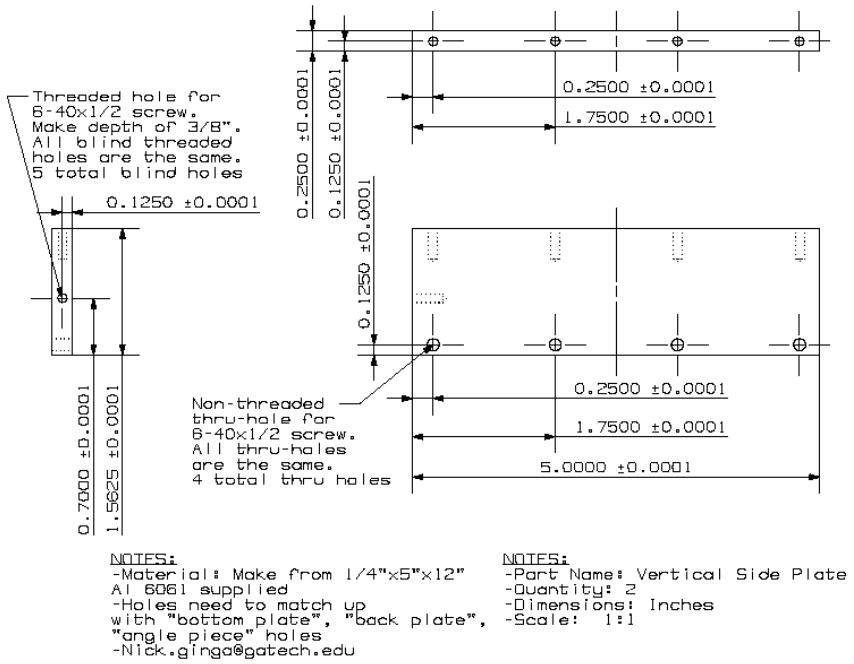


Figure 116: CNT Assembly Fixture: Vertical Side Plate

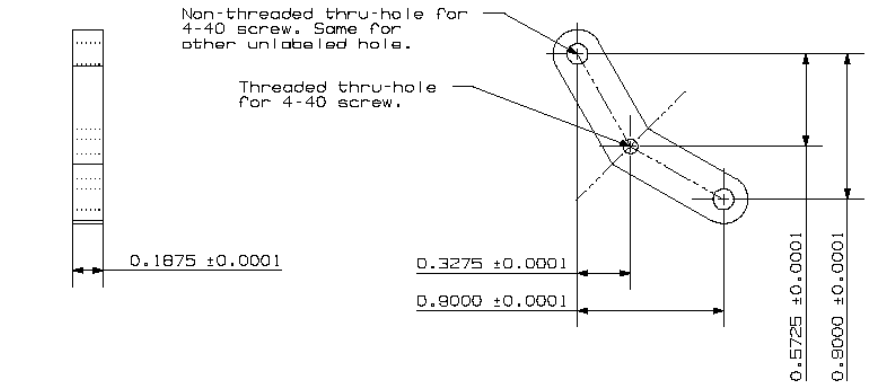


Figure 117: CNT Assembly Fixture: Plate

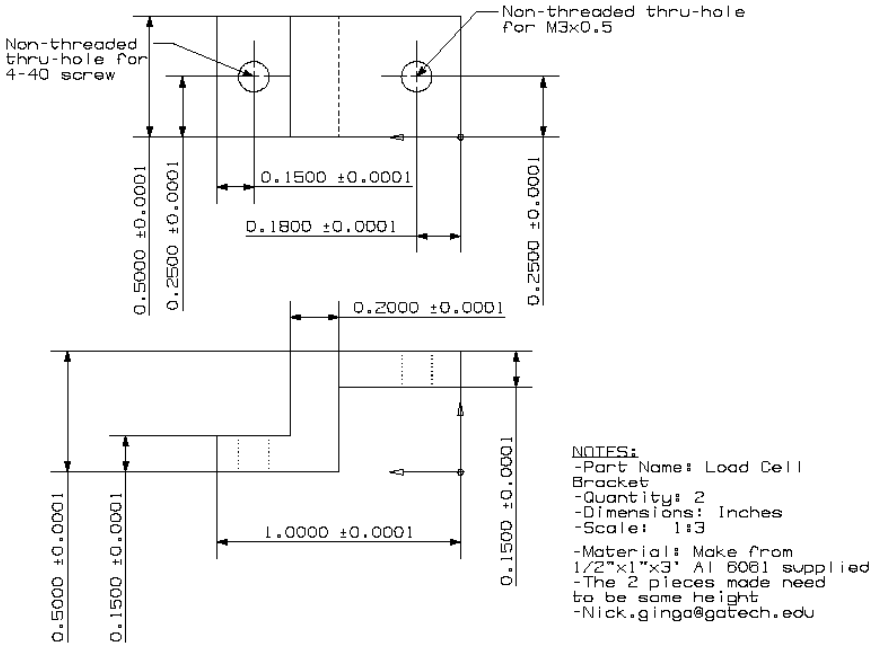


Figure 118: CNT Assembly Fixture: Loadcell Bracket

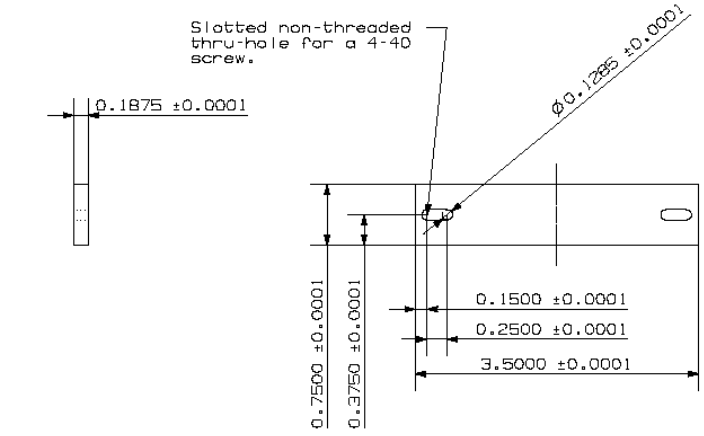


Figure 119: CNT Assembly Fixture: Crossbeam

A.5 Orthotropic and Transversely Isotropic Material Models

Compliance matrix for an orthotropic material is defined by:

$$\begin{bmatrix} \frac{1}{E_x} & -\frac{\nu_{yx}}{E_y} & -\frac{\nu_{zx}}{E_z} & 0 & 0 & 0 \\ -\frac{\nu_{xy}}{E_x} & \frac{1}{E_y} & -\frac{\nu_{zy}}{E_z} & 0 & 0 & 0 \\ -\frac{\nu_{xz}}{E_x} & -\frac{\nu_{yz}}{E_y} & \frac{1}{E_z} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{2G_{yz}} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{2G_{zx}} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{2G_{xy}} \end{bmatrix} \tag{24}$$

Where:

- ν_{ij} - defines the Poisson's ratio where *i* is the direction of extension and *j* is the direction of corresponding contraction.
- G_{ij} –defines the shear modulus in the direction *j* on the plane whose normal vector is in direction *i*.
- For the case of orthotropic materials the following relationships are true:

$$\frac{\nu_{yx}}{E_y} = \frac{\nu_{xy}}{E_x}, \quad \frac{\nu_{zx}}{E_z} = \frac{\nu_{xz}}{E_x}, \quad \frac{\nu_{yz}}{E_y} = \frac{\nu_{zy}}{E_z} \tag{25}$$

For a CNT forest, the material structure resembles that of a transversely isotropic material, which is a special case of orthotropy and is defined by a material having the same properties in one plane and different properties in the direction normal to that plane. For this study, the CNT forest has the same properties in the *X-Z* plane of Figure 73, and therefore $E_x=E_z$, but with different properties in the direction of the CNT growth (*Y*-direction) and therefore, E_y. To fully define this material model, five independent elastic constants are needed, which are E_y, $E_x=E_z$, ν_{yx}, ν_{xz}, and $G_{xy}= G_{yz}$. The properties that are in the *X-Z* plane of isotropy are $E_x=E_z$ and $\nu_{xz}= \nu_{zx}$, which can also be referred to as E_p and ν_p. While the properties that are out of plane of isotropy are E_y and ν_{yx}, and can be referred to as E_t and ν_{tp}. The other properties, G_{xz} and ν_{xy}, that are needed to implement this as an orthotropic property in Ansys®, can then be calculated from the previous five independent constants and using the following relationships for a transversely isotropic material. The compliance matrix for transversely isotropic material for orientation of CNT forests in this study is defined by:

$$\begin{bmatrix} \frac{1}{E_p} & -\frac{\nu_{tp}}{E_t} & -\frac{\nu_p}{E_p} & 0 & 0 & 0 \\ -\frac{\nu_{pt}}{E_p} & \frac{1}{E_t} & -\frac{\nu_{pt}}{E_p} & 0 & 0 & 0 \\ -\frac{\nu_p}{E_p} & -\frac{\nu_{tp}}{E_t} & \frac{1}{E_p} & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{2G_p} & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{2G_t} & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{2G_p} \end{bmatrix} \quad (26)$$

For the case of a transversely isotropic material, the following relationships also hold true due to the isotropy occurring in plane *X*-*Z* of the CNT forest:

$$\begin{aligned} E_x &= E_z = E_p \\ E_y &= E_t \end{aligned} \tag{27}$$

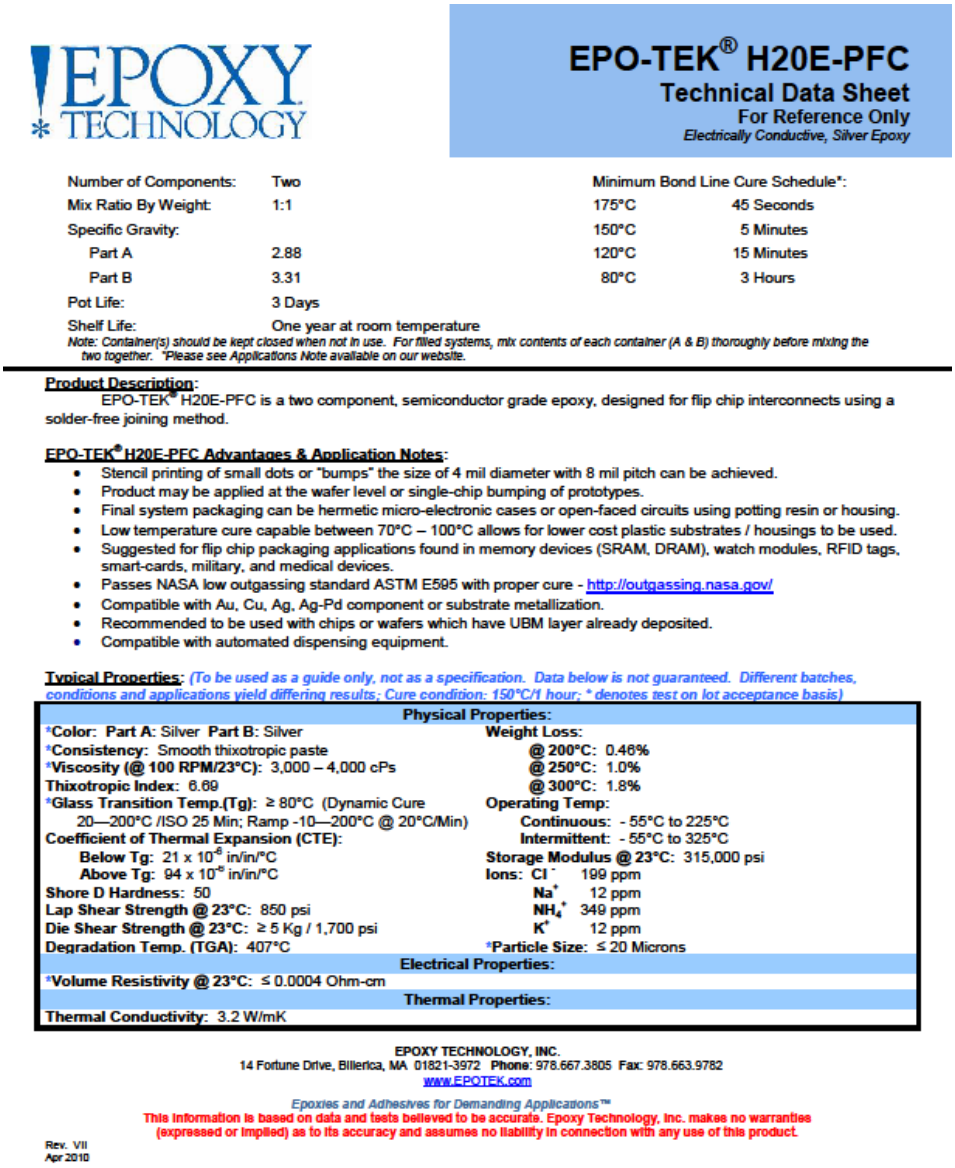
$$\begin{aligned} \nu_{yx} &= \nu_{yz} = \nu_{tp} \\ \nu_{xy} &= \nu_{zy} = \nu_{pt} \\ \nu_{xz} &= \nu_{zx} = \nu_p \end{aligned} \tag{28}$$

$$\begin{aligned} G_{yz} &= G_{xy} = G_p \\ G_{zx} &= G_t \end{aligned} \tag{29}$$

$$\frac{\nu_{yx}}{E_y} = \frac{\nu_{xy}}{E_x} \Leftrightarrow \frac{\nu_{tp}}{E_t} = \frac{\nu_{pt}}{E_p} \tag{30}$$

$$G_{xz} = \frac{E_x}{2\left(1+\nu_{xz}\right)} \Leftrightarrow G_p = \frac{E_p}{2\left(1+\nu_p\right)} \tag{31}$$

A.6 Electrically Conductive Adhesive Spec. Sheet



EPOXY TECHNOLOGY

EPO-TEK® H20E-PFC
Technical Data Sheet
For Reference Only
Electrically Conductive, Silver Epoxy

Number of Components:	Two
Mix Ratio By Weight:	1:1
Specific Gravity:	
Part A	2.88
Part B	3.31
Pot Life:	3 Days
Shelf Life:	One year at room temperature

Minimum Bond Line Cure Schedule*:

175°C	45 Seconds
150°C	5 Minutes
120°C	15 Minutes
80°C	3 Hours

*Note: Container(s) should be kept closed when not in use. For filled systems, mix contents of each container (A & B) thoroughly before mixing the two together. *Please see Applications Note available on our website.*

Product Description:
EPO-TEK® H20E-PFC is a two component, semiconductor grade epoxy, designed for flip chip interconnects using a solder-free joining method.

EPO-TEK® H20E-PFC Advantages & Application Notes:
- Stencil printing of small dots or "bumps" the size of 4 mil diameter with 8 mil pitch can be achieved.
- Product may be applied at the wafer level or single-chip bumping of prototypes.
- Final system packaging can be hermetic micro-electronic cases or open-faced circuits using potting resin or housing.
- Low temperature cure capable between 70°C – 100°C allows for lower cost plastic substrates / housings to be used.
- Suggested for flip chip packaging applications found in memory devices (SRAM, DRAM), watch modules, RFID tags, smart-cards, military, and medical devices.
- Passes NASA low outgassing standard ASTM E595 with proper cure - http://outgassing.nasa.gov/
- Compatible with Au, Cu, Ag, Ag-Pd component or substrate metallization.
- Recommended to be used with chips or wafers which have UBM layer already deposited.
- Compatible with automated dispensing equipment.

Typical Properties: *(To be used as a guide only, not as a specification. Data below is not guaranteed. Different batches, conditions and applications yield differing results; Cure condition: 150°C/1 hour; * denotes test on lot acceptance basis)*

Physical Properties:	
*Color: Part A: Silver Part B: Silver	Weight Loss:
*Consistency: Smooth thixotropic paste	@ 200°C: 0.46%
*Viscosity (@ 100 RPM/23°C): 3,000 – 4,000 cPs	@ 250°C: 1.0%
Thixotropic Index: 6.69	@ 300°C: 1.8%
*Glass Transition Temp.(Tg): ≥ 80°C (Dynamic Cure 20—200°C /ISO 25 Min; Ramp -10—200°C @ 20°C/Min)	Operating Temp:
	Continuous: - 55°C to 225°C
Coefficient of Thermal Expansion (CTE):	Intermittent: - 55°C to 325°C
Below Tg: 21 x 10^{-6} in/in/°C	Storage Modulus @ 23°C: 315,000 psi
Above Tg: 94 x 10^{-6} in/in/°C	Ions: Cl^- 199 ppm
Shore D Hardness: 50	Na^+ 12 ppm
Lap Shear Strength @ 23°C: 850 psi	NH_4^+ 349 ppm
Die Shear Strength @ 23°C: ≥ 5 Kg / 1,700 psi	K^+ 12 ppm
Degradation Temp. (TGA): 407°C	*Particle Size: ≤ 20 Microns
Electrical Properties:	
*Volume Resistivity @ 23°C: ≤ 0.0004 Ohm-cm	
Thermal Properties:	
Thermal Conductivity: 3.2 W/mK	

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14 Fortune Drive, Billerica, MA 01821-3972 Phone: 978.667.3805 Fax: 978.663.9782
www.EPOTEK.com

Rev. VII
Apr 2010

Figure 120: Electrically Conductive Adhesive Spec. Sheet

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