EMBEDDED ACTIVE AND PASSIVE METHODS TO REDUCE THE JUNCTION TEMPERATURE OF POWER AND RF ELECTRONICS

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EMBEDDED ACTIVE AND PASSIVE METHODS TO REDUCE THE JUNCTION TEMPERATURE OF POWER AND RF ELECTRONICS

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SUMMARY

AlGaN/GaN high electron mobility transistors (HEMTs) have been widely used for high power and high frequency RF communications due to their fast switching and large current handling capabilities. The reliability of such devices is strongly affected by the junction temperature where the highest magnitude occurs in a local region on the drain side edge of the gate called the hotspot. Thus, thermal management of these devices remains a major concern in the design and reliability of systems employing AlGaN/GaN HEMTs. Due to the large power densities induced in these devices locally near the drain side edge of the gate, it is clear that moving thermal management solutions closer to the heat generation region is critical in order to reduce the overall junction temperature of the device. In this work, we explore the use of embedded microchannel cooling in the substrate of AlGaN/GaN HEMTs made on Si and SiC substrates and compare them to passive cooling techniques using Si, SiC, and diamond substrates. In addition, the impact of cooling fluids and harsh environmental conditions were considered. The study was performed using a combination of CFD and finite volume analysis on packaged AlGaN/GaN HEMTs. Active cooling using embedded microchannels were shown to have a significant impact on the heat dissipation over the passive cooling methods, approaching or exceeding that of diamond cooled devices. For vertical power devices (IGBT), embedded microchannels in the power electronics substrates were explored. In both the power devices and lateral AlGaN/GaN HEMTs, the use of embedded microchannels with nonlinear channel geometries was shown to be the most effective in terms of reducing the device junction temperature while minimizing the pumping power required.

CHAPTER 1 INTRODUCTION

1.1 Background for AlGaN/GaN HEMT

The principle of a high electron mobility transistor (HEMT) is based on a heterojunction between different semiconductor materials with different bandgaps. The idea of a HEMT came in 1979 when n-type AlGaAs with undoped GaAs was used as the material combination [1]. Electrons from the AlGaAs layers moved to the GaAs potential wells (the potential well was formed because AlGaAs and GaAs have different bandgaps), and then the electrons can move quickly without colliding with any impurities because the GaAs is undoped. Therefore the electrons experience less from ionized donor scattering and achieve higher mobility compared to GaAs MOSFETs [1]. Since then, various material combinations have been explored and used depending on the applications (e.g. InAlAs/InGaAs and AlGaAs/InGaAs). The incorporation of Indium in the GaAs was found to help in improving the high frequency performances [2].

In recent years, AlGaN/GaN HEMTs have grown in popularity as GaN-based devices show significant advantages over their AlGaAs/GaAs HEMT counterparts, as shown in Table 1.1. GaN has a significantly higher bandgap than GaAs based materials. This wide bandgap makes GaN an excellent candidate for device operation in high temperature and harsh environments [3]. GaN-based devices also process a very high electron density (on the order of 10^{13} cm^{-2}) in the region of its 2-dimensonal electronic gas (2DEG) which is almost an order of magnitude higher than GaAs based device. The formation of the 2DEG is schematically shown in Figure 1.1. Both GaN and AlGaN layers are polar and exhibit spontaneous polarization. Spontaneous polarization is an inherit property of the materials that exists under zero strain condition. During the growth

of AlGaN, the positive side of the crystal atoms of AlGaN is aligned towards the GaN layer and the negative side is towards the growth direction [4], as shown in Figure 1.1. Since the thin AlGaN layer (~20 nm) is pseudomorphically grown on the relatively thick (~2 μm) GaN layer, the in-plane crystallography of AlGaN matches with that of GaN. However, AlGaN and GaN are two different materials with different crystal and thermal properties. This "forced" match of crystal lattice to that of GaN layer results in an elastic strain in the layers. Since the lattice constant of AlGaN is smaller than that of GaN, the pseudomorphically grown AlGaN is under tensile strain with respect to GaN [5]. Since the AlGaN is piezoelectric, the elastic strain causes a very high electric field (~10^6 V/cm) [4], which is high enough to ionize electrons and cause them to drift towards the heterointerface. This process is called piezoelectric polarization. The spontaneous and piezoelectric polarization of GaN and AlGaN together can generate enough sheet charge at the AlGaN/GaN interface to draw 1 to $2\text{x}10^{13}$ cm^{-2} electrons to the GaN side of the interface, forming a 2DEG. This large number of carriers in the 2DEG transfers to high current capability of the AlGaN/GaN HEMT.

Table 1.1 Basic properties of semiconductor materials for microwave power transistors [6].

Properties	Si	AlGaAs /InGaAs	SiC	AlGaN /GaN
Bandgap (E_g), eV	1.1	1.4	3.2	3.4
Electron mobility (μ_n), $cm^2 V^{-1} s^{-1}$	1350	8500	700	1200-2000
Saturation field electron velocity (υ_{sat}), $*10^7$ cm/s	1.0	2.0	2.0	2.5
2D sheet electron density (n_s), cm^{-2}	--	$3 * 10^{12}$	--	$(1\text{-}2) * 10^{13}$
Critical breakdown field (E_c), MV/cm	0.3	0.4	2.0	3.3
Thermal conductivity (K), $Wcm^{-1}K^{-1}$	1.5	0.5	4.5	1.3

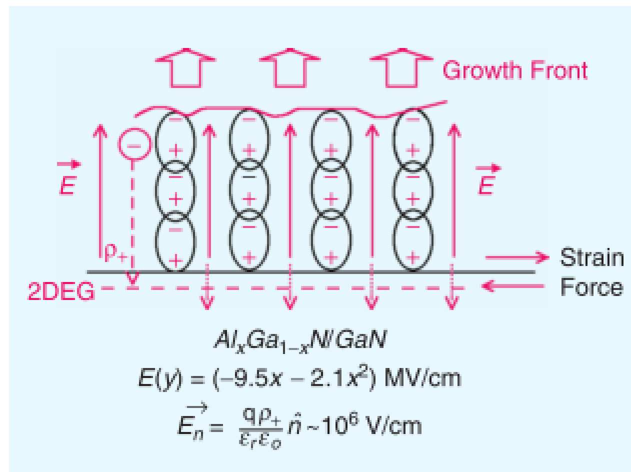

Figure 1.1 Schematic model showing the formation of a 2DEG at the AlGaN/GaN heterointerface [4].

AlGaN/GaN HEMTs also have a high critical breakdown field (~7 times higher than GaAs based HEMT), permitting high voltage operations. This high voltage application reduces the need for voltage conversion (low voltage devices need to have the operating voltage step down to the required voltage). Along with its high current capability as discussed above, the high current high voltage leads to high power applications of the AlGaN/GaN HEMT. AlGaN/GaN HEMTs have demonstrated one order of magnitude higher power density (power per unit width)

than GaAs based HEMTs. The high power density transfers into smaller devices resulting in higher impedance and lower chip cost as well as reduced system costs by reducing power combining [7]. A schematic comparison of AlGaN/GaN HEMT and AlGaAs/GaAs HEMT is shown in Figure 1.2.

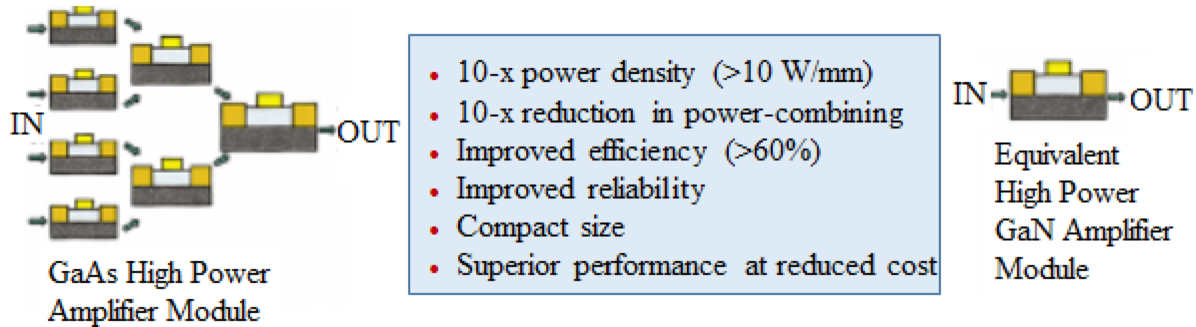

Figure 1.2 A schematic illustrating advantages of GaN over existing technology [7].

The fabrication of a typical AlGaN/GaN HEMT starts with the epitaxial growth of the GaN layer (channel layer). Up to very recently, wafers of single crystal GaN were not commercially available. So alternative substrates such as sapphire (Al_2O_3), Silicon carbide (SiC) or Silicon (Si) have been used. Among all these, SiC is the most attractive substrate because of its small lattice mismatch to GaN and high thermal conductivity, as shown in Table 1.2. However, SiC substrates are costly. Si and sapphire substrates are less costly than SiC substrates. But sapphire has relatively big lattice mismatch with GaN and low thermal conductivity (~50 W/mK), making it a poor choice in thermal management. Si (111) has a closer lattice constant to GaN than Si (100), and thus is a preferred choice. Recently diamond has been explored and used as the substrate because of its ultra-high thermal conductivity (~1200 W/mK) [8][9][10]. However, GaN on diamond substrate is expected to be limited to specific applications because of

its high cost. Therefore, Si is becoming attractive thanks to its low cost, availability in large wafer size, but suffers from its relatively poor thermal conductivity when compared to SiC.

The lattice mismatch between the GaN and its heteroepitaxial growth substrate introduces a large number of dislocations in the GaN layer as well as inherent stress due to difference in lattice constant and coefficient of thermal expansion differences between the two materials [11]. Thus a nucleation layer (typically consists of Aluminum nitride AlN because AlN and GaN both have the wurtzite structure and their lattice constants are close to each other) is needed. This thin AlN layer is typically deposited on the substrate before the growth of GaN layer. Studies have found that the AlN nucleation layer helps to reduce dislocations in the GaN layer and a smoother surface could be achieved [12] [13].

Table 1.2 Material properties of substrate and nucleation layers for GaN epitaxy [14] [15] [16].

Materials	Lattice parameter (Å)		Thermal conductivity (W/m-K)	Coefficient of thermal expansion (/K)		Crystal structure
	a	c		a	c	
GaN	3.189	5.185	150	5.59e-6	7.75e-6	Wurtzite
AlN	3.112	4.982	170	4.15e-6	5.27e-6	Wurtzite
Si (100)	5.431		150	2.6		Diamond
Si (111)	3.366		150	3.6		Diamond
6H-SiC	3.08	15.12	490	4.2e-6	4.68e-6	Hexagonal
Sapphire	4.758	12.99	50	7.5e-6	8.5e-6	rhombohedral

Following the deposition of the AlN nucleation layer, GaN films are grown by epitaxial techniques such as metal-organic chemical vapor deposition (MOCVD) or molecular beam epitaxy (MBE). The MBE method must be carried out at high vacuum condition and has a very low growth rate but it provides the highest purity of GaN film [17]. MOCVD is a more commonly used method with a higher growth rate but also has more defects. Upon the completion of the growth of the GaN layer, AlGaN layer is grown on the GaN layer with either

MBE or MOCVD [18] [19]. Since MOCVD has a higher growth temperature than MBE, a higher tensile strain in AlGaN layer is found by using MOCVD, resulting in a higher piezoelectric polarization, which is desirable for a high 2DEG carrier concentration at the AlGaN/GaN interface. Finally, ohmic contact deposition, gate metallization and passive layer deposition are needed to complete the device fabrication.

1.1.1 Reliability Issue for AlGaN/GaN HEMT

Figure 1.3 shows a front view of an AlGaN/GaN HEMT device in a conventional cooling structure. The red arrow shows all the layers that heat has to go through from heat source to be dissipated at the heat sink. Some of these layers have high thermal resistance, for example, the CuW package which is relatively thick, and the thermal grease layer which has low thermal conductivity. It must be noted that AlGaN/GaN HEMTs have high power density capability, resulting in a high heat flux/heat generation over the active region of the device. For example, a 10 W/mm power density in the channel with a gate length of 0.5 μm (as a first approximation) creates a heat flux of 1x 10^{10} W/m^2 if all of the heat is being dissipated over an area twice as wide as the device gates. This high heat flux has to spread and pass through all the layers in the device and package structure which imposes severe requirements for thermal management since failure time of the device is strongly dependent on the junction temperature [20], as shown in Figure 1.4. A temperature change from 200 °C to 227 °C would result in an order of magnitude lower mean time to failure in some cases.

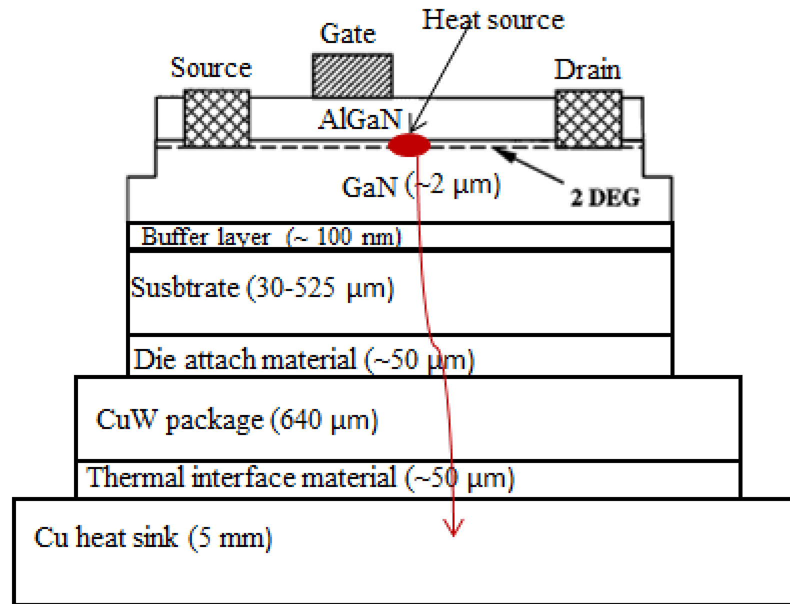

Figure 1.3 Front view of an AlGaN/GaN HEMT device showing all the layers between the heat source and the heat sink.

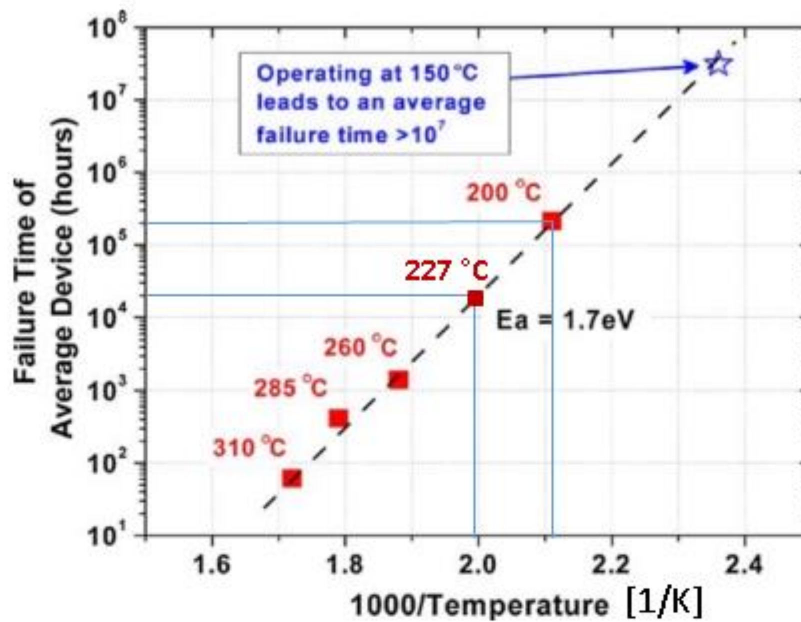

Figure 1.4 Plot showing exponential relationship between device temperature and failure time [20].

The high junction temperature can also negatively affect electrical performance of the device and accelerate device degradation. Some studies found that as temperature increases, the parasitic resistances increase linearly while the effective electron mobility decreases exponentially [21]. Studies have shown that the current saturation in measured I-V characteristics was found at an electric field that is much lower than that for the saturation of electron drift velocity due to self-heating of the devices. And also there is a significant difference in saturated current between GaN on SiC, GaN on Si and GaN on sapphire substrates, as shown in Figure 1.5. This difference in saturated current is believed to directly related to self-heating levels of the structures with different substrates and the self-heat levels are determined by the biased conditions and thermal properties of the substrate materials. The much bigger reduction in current density found in AlGaN/GaN grown on sapphire material is due to its much higher lattice temperature than the others as a consequence of the low thermal conductivity of sapphire [22][23].

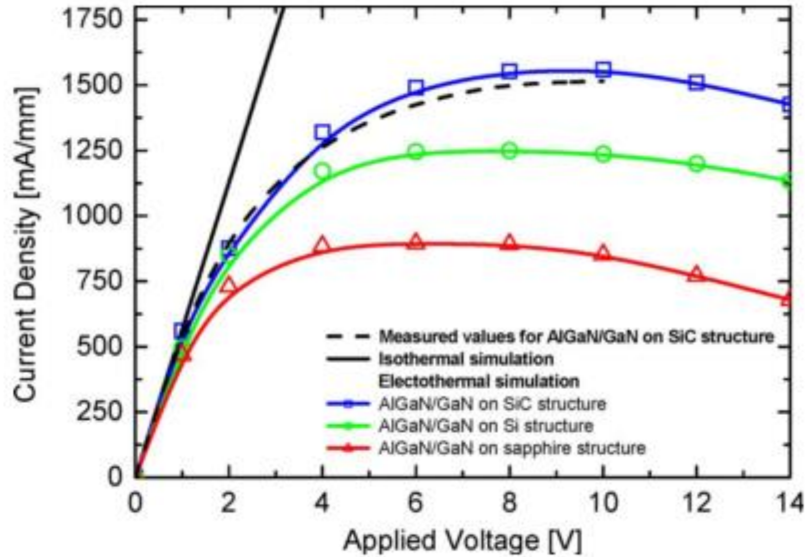

Figure 1.5 I-V characteristics as a function of the applied voltage. The isothermal simulation (solid line) and measured values (dashed line) are for the AlGaN/GaN on SiC structure [23].

1.2 Background of IGBT

The insulated gate bipolar transistor (IGBT) is a three-terminal power semiconductor device primary used as an electronic switch with fast switching and high voltage capabilities. Since an IGBT cell, as shown in Figure 1.6, is constructed similarly to an n-channel vertical MOSFET while containing a PNP bipolar junction, as shown in Figure 1.7, it is worth to first take a look at the MOSFET and bipolar junction transistor (BJT). In the MOSFET, when the gate is forward biased, the free hole carriers in the P^+ -epitaxial layer under the gate area are repelled away and thus a channel is created for electrons to flow from source to the drain [24]. The electrons are thus the majority carriers. The MOSFETs are voltage controlled. The electrons can start flowing as soon as the electrical bias is applied to the gate and stop as soon as the gate bias is removed, resulting in a fast switching speed [24]. Unlike MOSFET, BJTs are current controlled and rely on the minority carriers injected in the base. When the transistor needs to be switched off, a large amount of minority carriers are still in the base and needs to be removed—a

stored charge problem. This problem limits the switching speed of BJTs. Generally BJTs have low overall efficiency and are practically limited to less than 10 kHz in application. Therefore, MOSFETs are advantageous over BJT with their high switching speed and high frequency capabilities [25].

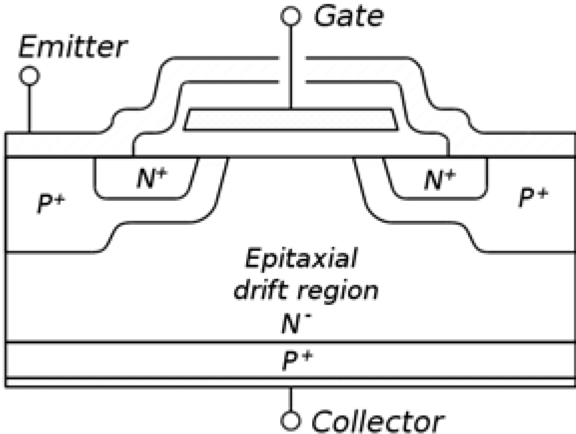

Figure 1.6 Simplified cross-section of an IGBT.

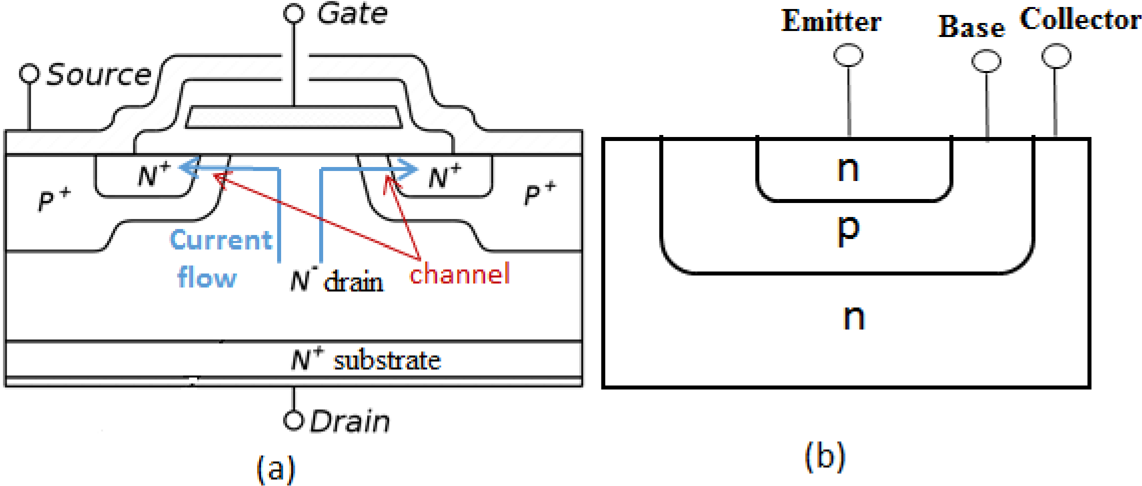

Figure 1.7 Simplified cross section of (a) a vertical MOSFET and (b) bipolar junction transistor.

However, in high voltage applications, MOSFETs exhibit lower efficiency due to their increased conduction loss as a consequence of increased on-resistance (the resistance between the drain and the source) [26]. The advantage of IGBT now comes to light: it combines the high switching speed of MOSFET with the low conduction loss of a BJT. Today, IGBTs have replaced power BJT and MOSFET in the medium voltage (600-2500 V), medium power (10 kW), and medium frequency range up to 20 kHz. IGBTs are also used in high power or megawatt-power sector such as motor drives for heavy motors [27]. The device structural material is Silicon and typically direct bond copper (DBC) is the substrate for IGBT.

IGBTs are getting more popular in hybrid electric vehicles (HEV) by providing traction motor control. The growing market of HEVs strongly relies on the reliability of the IGBTs. It has been found that the high junction temperature and temperature gradient among the power module directly affects the reliability of IGBT devices. Power cycling in IGBTs cause mechanical stress in the solder attach layer resulting in delamination. It can also cause increase in threshold voltage, indicating a degradation of the gate oxide [28]. Another study shows that the wire bonds and metallization of the IGBT exhibit high sensitivity to high-temperature power cycling. Heel fractures, liftoff, and metallurgical damage were observed at high temperatures (up to 170 °C) [29]. Since IGBTs are for high voltage high power applications, the junction temperature could be high enough to severely affect the reliability of the devices.

1.3 Research Motivation and Thesis Outline

As discussed above, the reliability of AlGaN/GaN HEMT strongly depends on its junction temperature. In order to improve the reliability, the junction temperature has to be maintained at a low value (under 200 °C in order to have an average lifetime of $2x10^5$ hours based on Figure

1.4). With a highly localized heat source, it is crucial to spread out the heat as much as possible for efficient heat removal at the heat sink. Therefore, substrates with high thermal conductivity are desirable. Sapphire is the traditional substrate for GaN, but it has a low thermal conductivity (~50 W/mK). Silicon carbide SiC is also a very common substrate and has good thermal conductivity (~490 W/mK at room temperature), but SiC substrates are costly. Silicon (Si) is an attractive substrate material because it is less costly than SiC and has a reasonable thermal conductivity (~150 W/mK at room temperature). Diamond has the highest thermal conductivity (>1200 W/mK) and is expected to be an excellent heat spreader under the GaN layer. However, unlike GaN on SiC or Si substrate, the technology of using diamond as a substrate material for HEMT devices is far from mature and is very costly. Therefore, an opportunity exists to explore an alternative way to cool the devices. By moving the heat sink or cold plate as close as possible to the heat source, the thermal resistance will be minimized and allow for the use of AlGaN/GaN HEMTs on lower thermal conductivity substrates. Although it is not possible to embed a heat sink inside the GaN layer as GaN is an active layer (channel layer) for the device, embedding a heat sink inside the SiC or Si substrate by use of microchannels is possible. Since Si is undoped, it can act as an electrically insulated layer. Liquid coolants can flow through the microchannels embedded inside the substrate to greatly reduce the thermal resistance between the heat source and the coolant. Additionally, we will explore different microchannel features inside heat sink for enhanced thermal performance. Through the use of computational fluid dynamics (CFD) model, we propose to be the first to investigate the use of embedded non-linear microchannel cold plate in the substrate of AlGaN/GaN HEMTs.

The concept of bringing the heat sink closer to the heat source for a reduced thermal resistance can be applied to IGBT devices. Although it is not feasible to embed the microchannel

heat sink inside the silicon chip because current flows inside the chip, the heat sink can be embedded inside the DBC substrate. Similar to the study of HEMT, we will explore different microchannel features inside heat sink for enhanced thermal performance.

An outline from chapter 2 to chapter 5 is shown below:

Chapter 2 presents a literature review on different cooling techniques for AlGaN/GaN HEMT devices and IGBT devices studied so far.

Chapter 3 presents computational results for AlGaN/GaN HEMT devices. Both passive and active liquid cooling using Si, SiC and diamond substrates are studied and compared. Specifically, active liquid cooling using SiC and and Si substrates are compared to passive cooling using high thermal conductivity diamond substrate. The maximum power density for different substrate and cooling method is obtained with a junction temperature of 200 °C. Additionally, the impact of ambient temperature on the choice of cooling fluid and power density requirement is investigated.

Chapter 4 presents simulation results for active liquid cooling of IGBTs. Single-sided cooling with linear and pin fin microchannels is studied and is compared to double-sided cooling with pin fin microchannels.

Chapter 5 states the final conclusions and proposes future work for further investigation of embedded microchannel liquid cooling inside a substrate and validations with experiment.

CHAPTER 2 BACKGROUND

2.1 Introduction

The purpose of this chapter is to have an overview of some previous works on thermal management of AlGaN/GaN HEMTs and IGBTs. For AlGaN/GaN HEMTs, standard cooling method and advanced heat spreading cooling methods with solid state and microchannel liquid cooling will be discussed. For IGBT devices, single-sided cooling with different packaging structures and double-sided microchannel liquid cooling will be presented. Thermal resistance, power dissipation, flow rate and pressure drop in each cooling method are also discussed.

2.2 Thermal Management for AlGaN/GaN HEMT

2.2.1 Standard Cooling method

The standard cooling method for AlGaN/GaN HEMT devices is shown in Figure 2.1. GaN on Si or SiC substrate (die) is soldered to a CuW package for electrical connection. The CuW is placed on a big copper heat sink, in which high volume of water flows through to maintain a certain temperature inside the copper cold plate. Since the coefficient of thermal expansion (CTE) is very different between substrate materials and copper, the CuW layer can also help to reduce thermal stress. CuW has a CTE of $7x10^{-6}$ /°C [30]. SiC and Si have CTE of 3.2 to $3.8x10^{-6}$ /°C [31] and 2.6 to $3.5x10^{-6}$ /°C [32] from 20 °C to 200 °C, respectively while copper has a CTE of 16.5 /°C [33]. In order to have a good physical connection between the CuW package and the copper heat sink, a thin layer (less than 100 μm) of thermal grease or epoxy is needed.

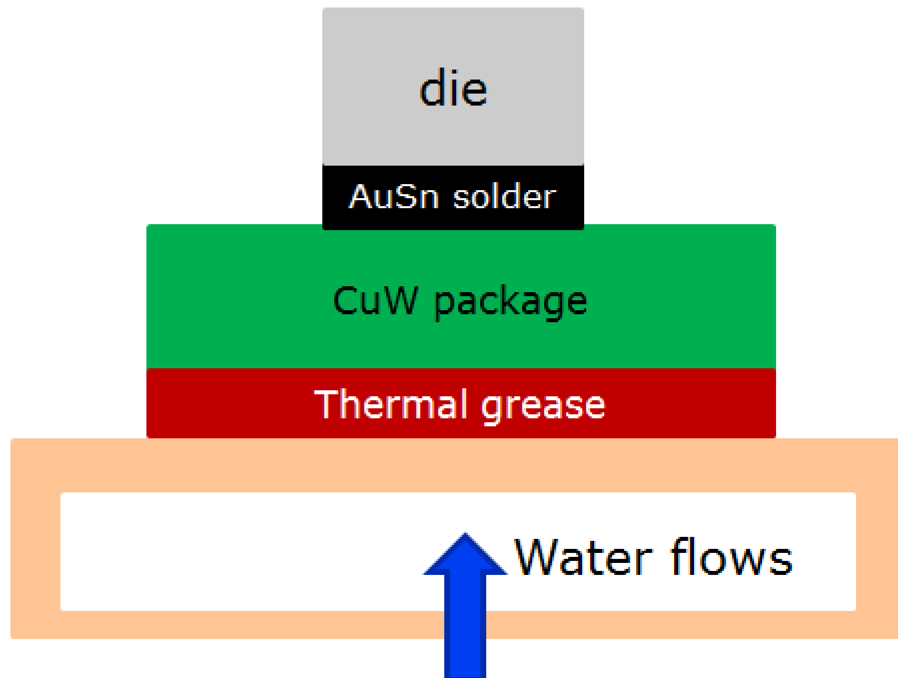

Figure 2.1 Stardard cooling structure for AlGaN/GaN HEMT.

2.2.2 Advanced heat spreading techniques

1) Phase change heat spreader

Improvements in heat spreading in AlGaN/GaN HEMTs can be used to reduce the overall package resistance and reduce the junction temperature of the devices. One technology that has been recently developed is the use of phase change heat spreaders which provide an effective thermal conductivity equal to or greater than diamond within the DARPA Thermal Ground Plane Program. With a thermal conductivity that is comparable to polycrystalline diamond, these phase change heat spreaders require low cost materials and fabrication techniques. One study used Carbon Nanotube (CNT) enhanced sintered Cu powder wick structure or Cu foam structure in the Thermal Ground Plane (TGP) [34] . With the CNT, wicks can operate in the boiling regime at lower heat inputs and temperatures. And with the Cu foam structure, the evaporative resistance can be greatly reduced. Another study investigated an all

titanium thermal ground plane which was light, strong and compatible with water [35]. The groove wick was coated by nanoporous titania, as shown in Figure 2.2, which could increase wicking velocity by 70% [36], resulting in a higher flow rate. The effective thermal conductivity was found to be ~8000 W/mK [35].

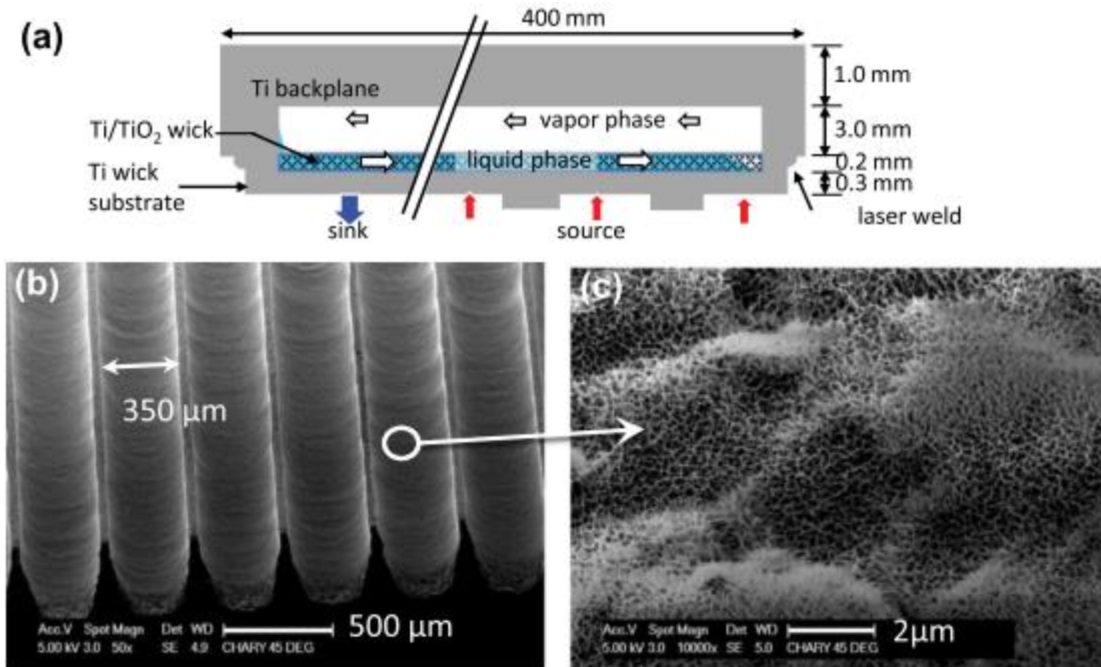

Figure 2.2 (a) cross sectional diagram of Titanium thermal ground plane; (b) Etched grooves in titanium substrate with a depth of 250 µm and a width of 350 µm and (c) the titanium is oxidized to produce the Nano-Structrued-Titania structure [35].

2) Diamond substrate

A solid state method of heat spreading can be approached by introducing high thermal conductivity materials in the AlGaN/GaN device stack. The majority of AlGaN/GaN HEMTs are grown on SiC substrates due to its high thermal conductivity (~400 W/mK), which is approximately 2.5 times that of GaN. However, the use of SiC is not always sufficient for

devices operating at high power densities. Diamond substrates have a factor of 3-4 higher thermal conductivity than SiC and are of interest for thermal management in AlGaN/GaN HEMTs. Compared to GaN on 370 µm SiC, GaN on 25 µm CVD diamond demonstrated only half of the thermal resistance from experimental results [37]. The advantage in thermal management in using CVD diamond as the substrate is shown in Figure 2.3. There is a significant reduction in temperature especially at high power density while using diamond substrate. But GaN on diamond does not have as good electrical performance as GaN on SiC. It is found that GaN epitaxy layer on diamond has a higher turn on voltage and higher sheet resistivity leading to lower current and power in a device [38]. Along with high cost of diamond, the success of this approach is limited as of today.

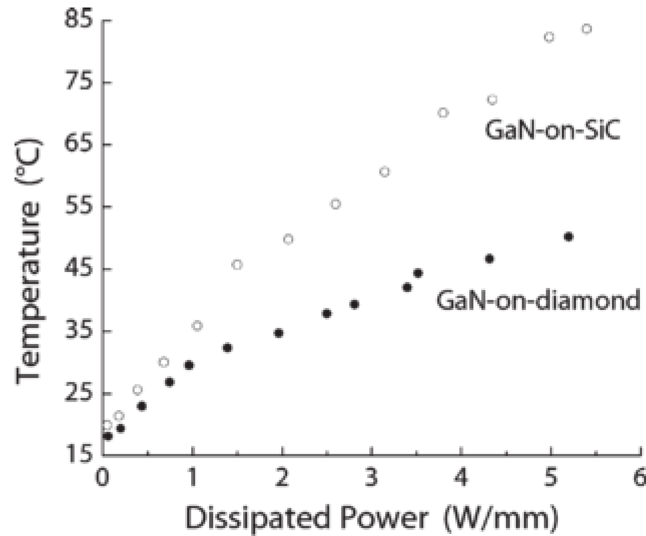

Figure 2.3 Operating temperature of single-finger GaN-on-diamond and GaN-on-SiC HEMTs [37].

To integrate AlGaN/GaN on diamond, the AlGaN/GaN epitaxial layers were first grown by metal organic chemical vapor deposition (MOCVD) on Si (111) substrates. This AlGaN/GaN/Si wafer was then front-side-mounted to a mechanical substrate so that the Si substrate could be removed from the backside to reveal the GaN buffer layer. Finally this AlGaN/GaN structure was attached to a flat poly-crystalline CVD diamond substrate, as demonstrated in [10] [39]. Another study reported growing GaN on (111) single crystal diamond substrate by molecular beam epitaxy (MBE) [8]. In either one of these growth method, a transition layer based on AlN is needed to reduce the lattice mismatch between the GaN layer and the substrate and to promote the growth of high quality GaN layer. But this transition layer increases the overall thermal resistance by increasing the thermal boundary resistance (TBR) between the GaN layer and the diamond substrate. This TBR arises from GaN-transition and transition-substrate interface resistances as well as the intrinsic thermal resistance of the transition layer. This interface resistance is controlled by grain boundary scattering, defect scattering, and acoustic impedance mismatch [40]. This TBR could diminish the benefits of using diamond substrate. As discussed in [9], the first generation of GaN-on-diamond which consists of 1200 nm thick transition layer (600 nm $Al_{0.5}Ga_{0.5}N$ and 600 nm AlN) has a TBR of 108 m^2K/GW, and this resistance was reduced to 36 m^2K/GW in their second generation of GaN-on-diamond with reduced thickness of transition layer. However, this reduced TBR still can slow down heat dissipation from the heat source to the diamond heat sink.

Another challenge in using diamond substrate is to grow high quality diamond with sufficiently high thermal conductivity. Most of the CVD diamond layers are reported to have a thermal conductivity of near 1200 W/m-K [41] although intrinsic thermal conductivity of diamond at room temperature is 2000 W/m-K. The thermal properties of CVD diamond is

strongly dependent on its microstructure, which is affected by its growing parameters especially the ratio of methane to hydrogen concentration used during the deposition process [42]. The CVD grown diamond also exhibits columnar growth, as shown in Figure 2.4. The thermal conductivity of the CVD diamond has be found to be anisotropic, nonhomogeneous and thickness dependent [43] [44]. All these add to the complications of using sufficiently high thermal conductivity diamond substrate, in addition to the challenges in scaling up the process because of the accumulated stresses due to CTE that can lead to wafer breakage and thus severely limiting the maximum achievable wafer diameter [45]. This increased complexity in fabrication along with high cost limits the widespread use of diamond.

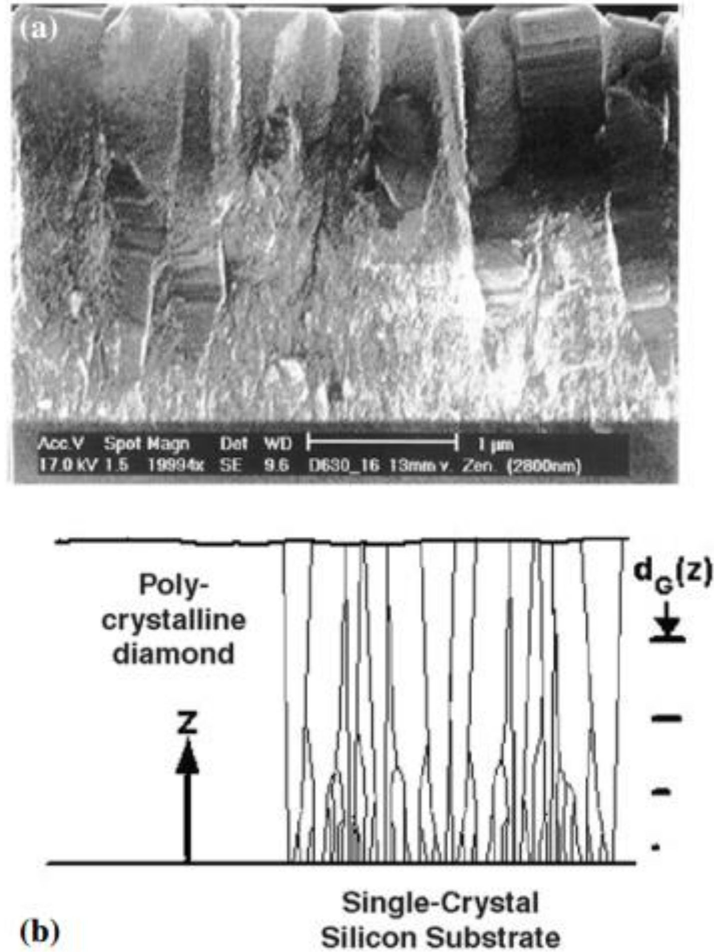

Figure 2.4 (a) Cross-sectional electron micrograph of a diamond layer deposited at 800 °C and nucleated using a bias voltage; (b) schematic of the grain structure in a micro-scale diamond layer deposited on silicon. [42] [46]

Another use of high thermal conductivity diamond in the thermal management of HEMT is to selectively grow diamond in thermal vias, as demonstrated in [47]. Backside vias were etched in the back of GaN on SiC substrates where diamond was selectively grown subsequently. There was a 60 °C difference between GaN on SiC with and without diamond thermal vias, as shown in Figure 2.5.

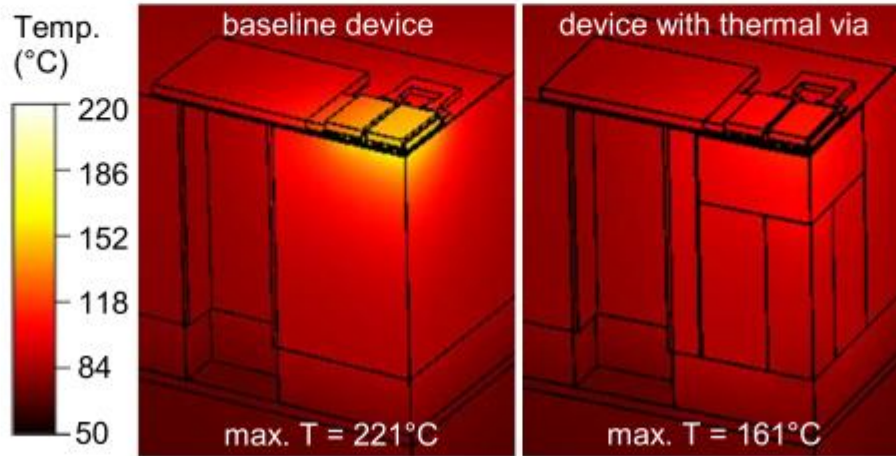

Figure 2.5 GaN HEMT self-heating simulated for 3.5 W power dissipation (7 W/mm) [47].

3) Use of Microchannel Heat Sinks

Another method to introduce advance heat spreading in devices is to use convection as opposed to conduction to remove the heat from the device. This has been reported in a previous study through the use of a direct-die-attached copper microchannel heat sink [48]. The geometry of the Cu heat sink is shown in Figure 2.6. The GaN-on-Si die is mounted on top of the microchannel with 50 µm AuSn interfacial material. The heat sink features 21 linear fins and is water cooled. This Cu heat sink also serves as a ground plane for the device. A printed circuit board (PCB) with a square cut at the middle is attached onto the heat sink so that the package can be wire-bonded to connect the chip to power supply. Compared to conventional cooling, this use of direct-die-attached heat sink eliminates the thermal resistance due to the CuW layer and the low thermal conductivity epoxy, and brings the heat sink closer to the heat source. However, the CTE mismatch between the Si substrate and Cu heat sink can be problematic.

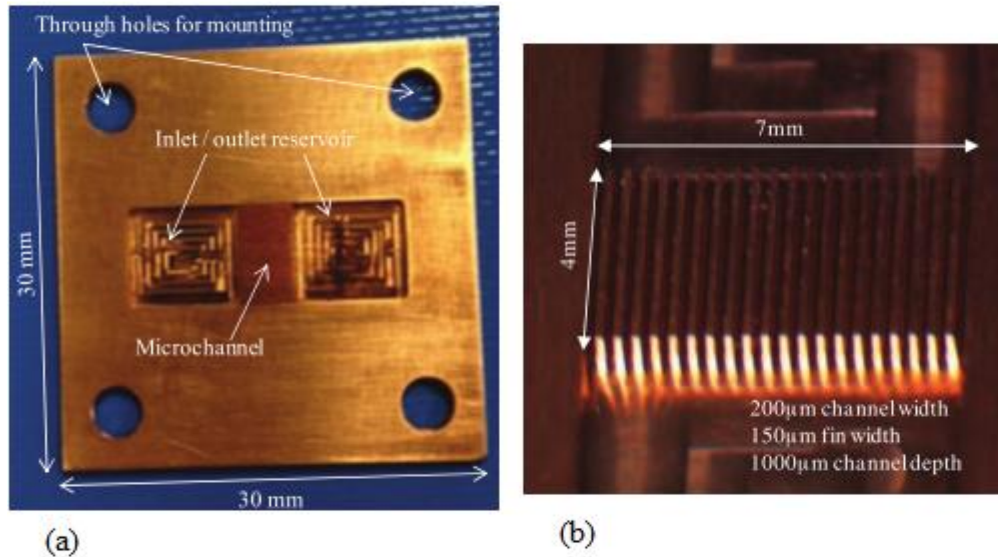

Figure 2.6 (a) Fabricated copper microchannel heat sink and (b) Zoomed-in view of microchannel [48].

The use of direct-die-attached microchannel coolers for the thermal management of GaN-on-SiC HEMT was first explored by Dr. Calame from Naval Research Laboratory. [49] [50] Both metallic and non-metallic coolers were studied, as shown in Figure 2.7 and Figure 2.8. They found that a hybrid microchannel consists of CVD diamond on SiC exhibits the best cooling performance. However, the exact power density of the HEMT that the microchannel cooler could handle cannot be evaluated because a spatially-averaged heat flux on the entire active area was used in both their computational and experimental methods.

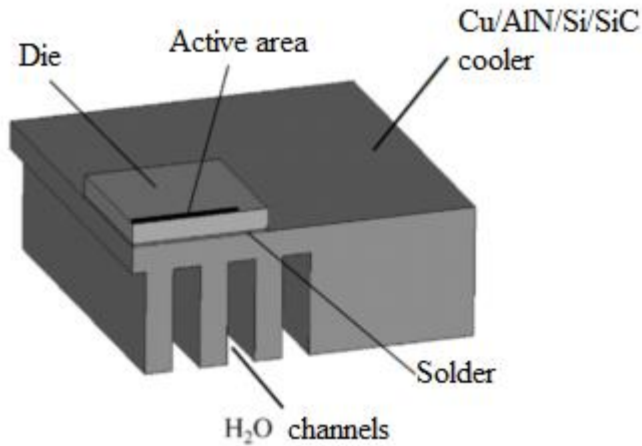

Figure 2.7 Test geometry for the SiC die on a Cu/AlN/Si/SiC microchannel cooler configuration. Only ¼ of the problem is shown due to symmetry. [49] [50]

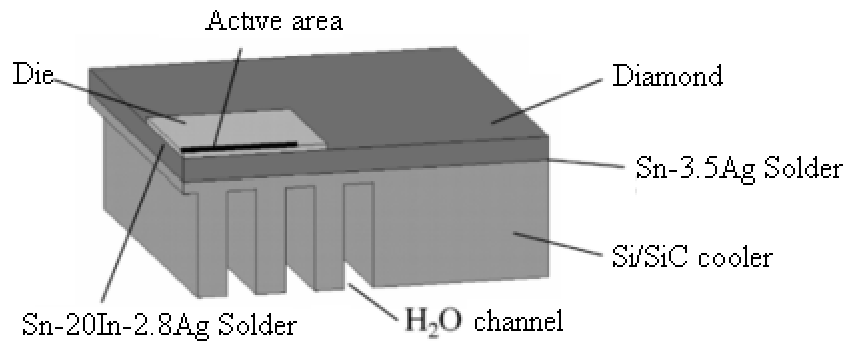

Figure 2.8 Geometry of a complex package consisting of a thinned SiC die, a diamond heat spreader, and a Si/SiC microchannel cooler, bonded together with two types of solder. Only ¼ of the problem is shown due to symmetry. [49] [50]

The idea of forming tree-branch microchannels in SiC for direct cooling of high power electronics was proposed by a group in Penn State University. [51] The microchannels were laser machined into 11.5 mm x 16 mm x 1.5 mm thick SiC pieces, as shown in Figure 2.9. Since the microchannels are 10 mm long, the pressure drop for their best designed tree-branch microcachannel was almost 400 kPa at the flow rate of 200 ml/min. Such a high pressure drop

will not only require high pumping power, but decrease reliability of using microchannel liquid cooling. Furthermore, the cooling performance of this SiC microchannel heat sink has not been evaluated on any real devices.

Figure 2.9 Image of single crystal SiC heat sink with tree-branch structure. [51]

Although there are very limited studies on microchannel liquid cooling for HEMT devices, numerous of studies have reported use of microchannel liquid cooling for high power electronic devices. Tuckerman and Pease were the first ones who studied forced liquid cooling for planar integrated circuits in 1981 [52]. Linear microchannels were etched in a silicon wafer and wafer was fed through the microchannels. At a flow rate of about 2.4 L/min, the thermal resistance reached 0.1 K/W. A lot of work has been focused on improving heat transfer performance of the microchannel heat sink by adding features inside the heat sink to increase the turbulence intensity of the fluid flow. Wang studied offset branching network features in a cold plate and found that this offset in leaf-like branching network can reduce pressure drop significantly [53]. Rubio-Jimenez compared the online and offset micro pin fin heat sinks with variable fin density and found that the offset micro pin fin heat sink show better thermal performance than online pin fin heat sink. Pin fin heat sink had a 1.5% and 7.5% reduction in the overall bottom wall temperature compared to the online microchannel heat sink and linear microchannel heat sink.

Pin fin micro heat sink could also improve the temperature uniformity. But the pressure drop increased significantly while using pin fin heat sink [54]. Lawson studied the thermal performance of multiple low arrays of low aspect ratio pin fins and found that the smaller the streamwise spacing the bigger the array-averaged Nusselt number. This effect of streamwise spacing is more obvious than that of spanwise spacing on heat transfer performance. But pressure loss is more dependent on spanwise spacing than on streamwise spacing [55]. Khan investigated and compared thermal/fluid performance of different fin geometries including rectangular plate fins, square, circular and elliptical pin fins. The square pin fin was found to have the worst thermal performance while the circular pin fins had the best performance [56].

Another way to improve heat transfer performance of the microchannel heat sink is to use high thermal conductivity material for the heat sink. Fabian Pease et al. proposed using diamond microchannel to improve heat sinking for laser diode arrays [57]. The calculated resistance between heat source and the coolant using CVD diamond microchannel heat sink was found to be 75% less than that for silicon microchannel heat sink. Raytheon Company has demonstrated that it was feasible to fabricate a diamond microchannel heat sink and integrate into practical systems for superior thermal performance [58].

2.3 Thermal Management for IGBT

With the increasing demand on high power, high efficiency and high reliability of power electronics, traditional air cooling methods can no longer provide sufficient cooling capability. Liquid cooling with microchannel heat sinks has been used as an alternative solution for thermal management for devices with high heat flux.

2.3.1 Wire Bonding With Single Sided Cooling

A conventional packaged structure of a semiconductor device consists of a DBC (Cu/AlN/Cu or Cu/Al_2O_3/Cu) substrate, a base plate, a thin layer of thermal grease and air or water cooled heat sink, as shown in Figure 2.10. The low thermal conductivity of thermal grease (usually < 1 W/mK) contributes to a large thermal resistance in the conventional package. When Cu/Al_2O_3/Cu DBC was used, the thermal resistance was 0.312 K/W with a water cooled heat sink. This resistance was reduced to 0.245 K/W if AlN ceramic was used instead of Al_2O_3 [59]. Thermal resistance for an air-cooled package was found to be 0.35 K/W [60]. For a maximum chip temperature rise of 55 °C, the maximum chip power dissipation is limited to 157 W.

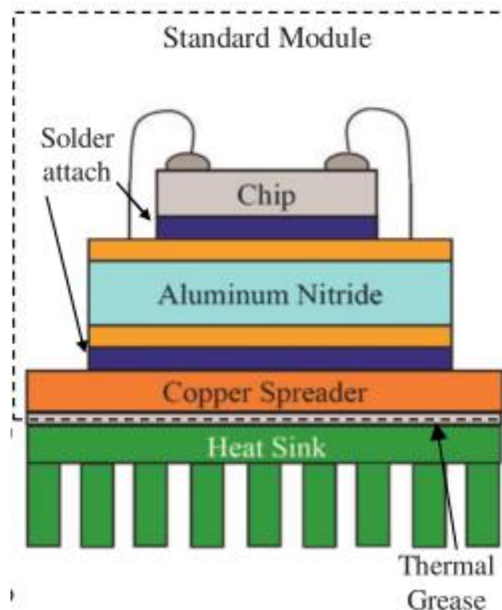

Figure 2.10 Cross section of a conventional packaging structure of a semiconductor power device [61].

To further shorten the heat transfer path from heat source to coolant, microchannels can be made into the ceramic layer (AlN in this case) of a DBC, as shown in Figure 2.11 (b). Recent

progress in AlN processing enables the realization of the AlN-based microchannel heat sink. The U.S. army research lab first proposed and fabricated such AlN based heat sink [61]. While minimizing heat path by moving the heat sink from below DBC in conventional cooling (as shown in Figure 2.11 (a)) up to inside the DBC (as shown in Figure 2.11 (b)), a 15% and 80% reduction were achieved compared to conventional cooling with AuSn solder and thermal interface material (TIM) between DBC and heat sink, respectively. The total thermal resistance of the AlN-based microchannel heat sink was 0.128 K/W at a pressure drop of 66.6 kPa [62].

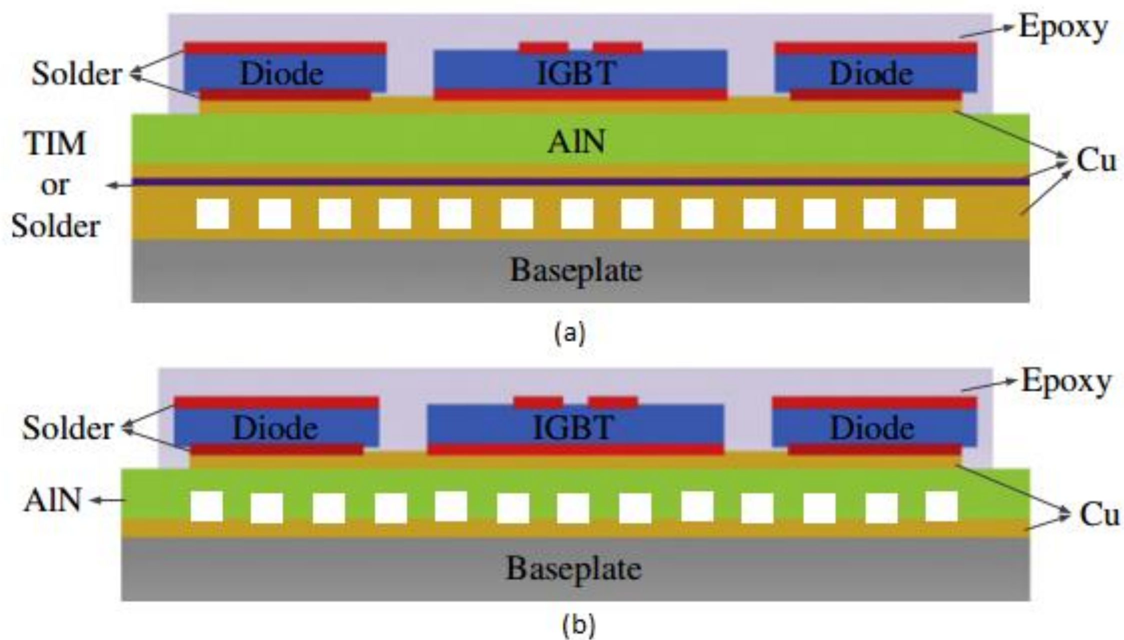

Figure 2.11 (a) conventional cooling structure and (b) cooling structure with a shorter heat source to coolant path [62].

An advanced liquid cooled base plate using pins inside the plate has shown good thermal management performance [63]. The base plate was made of metal matrix composites (MMC). The MMC consisted of aluminum alloy and porous silicon carbide. It has a thermal conductivity of about 180 W/mK. IGBT dies were mounted on both sides of the base plate, as shown in

Figure 2.12. This cooling scheme not only reduced temperature rise of the junction but also increased temperature uniformity among IGBT dies. A total power of 1200 W from 12 IGBT dies was achieved while maintaining a maximum junction temperature of 100 °C. The temperature variation among junction temperatures of dies was within 1 °C. An average junction to case thermal resistance of 0.047 K/W was found at a flow rate of 7.57 liter/min. This thermal resistance was calculated by the temperature difference between the average junction temperature and case temperature (the average temperature in the MMC baseplate right above the channel) divided by the total power dissipation from one side. The pressure drop was 39 mbar.

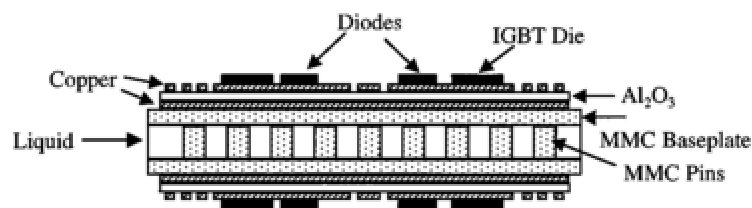

Figure 2.12 Cross sectional view of a IGBT module with liquid cooling [63].

A more aggressive scheme employed the use of direct water spray-cooling over a three-phase motor drive system [60], as demonstrated in Figure 2.13. A 25 μm parylene coating was used to electrically insulate the exposed devices and interconnections. This method greatly reduced the chip to "case" thermal resistance (the "case" referred to the impinging water) for each IGBT in the power module. A thermal resistance of about 0.05 K/W was obtained under a mass flow rate of 1.02 liter/min. The power loss for the whole system consisting of 6 IGBTs was 670 W.

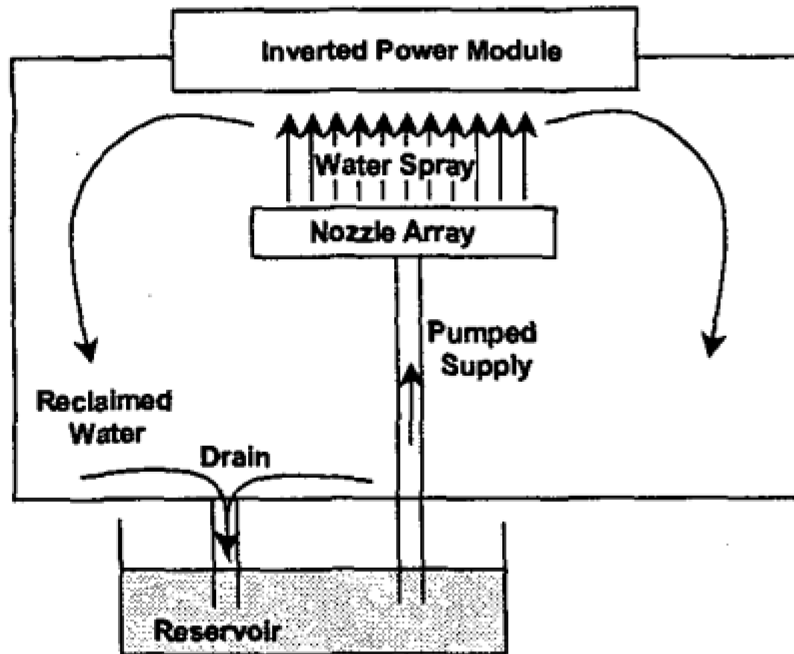

Figure 2.13 Schematic of the water-spray facility [60].

Previous researchers investigated single and two-phase cooling in a micro-scale copper heat sink onto which an IGBT die was directly brazed [64]. Although it was unclear what was in between the IGBT die and the copper heat sink to electrically insulate the interconnection, a comparison between single phase and two-phase can be made. For single phase cooling, a thermal resistance of 0.101 K/W was realized with a flow rate of 2 liter/min and a pressure drop of 3.1 kPa. A similar thermal resistance was obtained in the two-phase cooling with a significantly reduced flow rate (0.030 liter/min) and pressure drop (0.27 kPa). Therefore, a much lower pumping power was needed in two-phase cooling, although there are more challenges in realizing two-phase than single phase flow, for instance, to prevent flow instability and local dry-out.

2.3.2 Flip Chip Bonding With Double Sided Cooling

In wire-bonded devices with single sided cooling, heat dissipation via conduction through one side of the die and then via convection at the heat sink was the only path as natural convection on the other side of the die was negligible. But if the wire-bonded connection is replaced by flip chip bonding, the chip can be cooled on both sides. Gillot [65] proposed this double-sided cooling scheme for high power IGBT modules in which the IGBT chip and diodes were sandwiched between the two DBCs, as shown in Figure 2.14. Microchannel heat sinks made of copper were brazed onto the top and bottom DBC using a Pb/Sn solder (with a thermal conductivity of 50 W/mK). The IGBT chips and diodes were brazed onto the top and bottom DBCs with a Sn/Pb/Ag solder (with a thermal conductivity of 23 W/mK) using flip chip solder bump technology. For a temperature rise of 45 °C, the module with double sided cooling could handle 340 W/cm^2 of power dissipation, leading to an increase of 76% compared to 195 W/cm^2 in single sided cooling. Under the same power dissipation, the maximum chip temperature decreased from 63 °C in single-sided cooling to 44 °C in double-sided cooling, suggesting a temperature reduction of 30%. The thermal resistance for double-sided cooling was 0.09 to 0.12 K/W for a flow rate range of 1 to 8 liter/min. This thermal resistance was calculated by the temperature difference between the junction temperature of the chip and inlet fluid temperature divided by power dissipated in the chip.

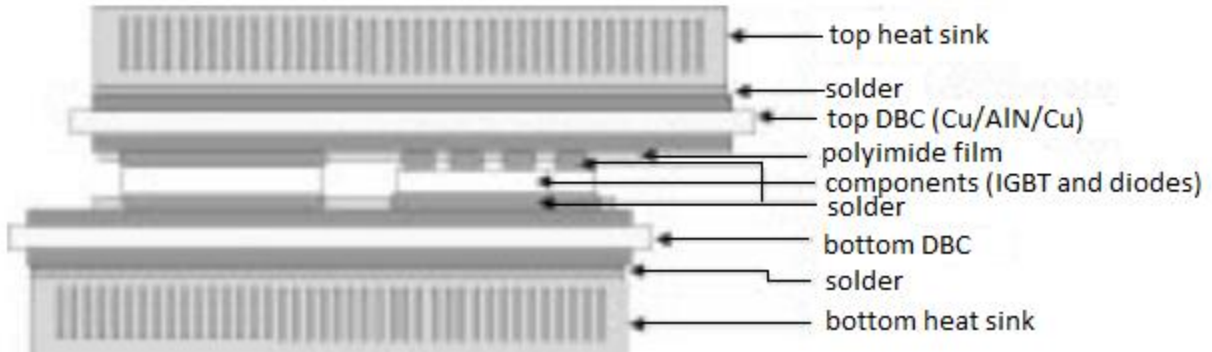

Figure 2.14 Module with double sided cooling. Heat sinks were brazed to top and bottom heat sinks [65].

Mei also conducted a study on double-sided cooling of IGBT with the chip sandwiched between the top and bottom DBC [66]. The main focus of the study was to investigate the mechanical and thermal performance of nanosilver paste as an alternative lead-free die-attach material. Nanosilver has a thermal conductivity of 220 W/mK, which is much higher than regular solders. However, low thermal conductivity Al_2O_3 (k = 26 W/mK) was chosen as the dielectric layer in DBC in this study, which caused a high junction to case thermal resistance. The thermal resistances were 0.46 and 0.26 W/mK for the single-sided and double-sided cooling, respectively. Similar to [65], a 30% reduction in chip junction temperature was seen from adding the second cooling path.

Low temperature joining technique was another method used to connect power semiconductor chips to DBC and enable double-sided cooling [59]. Materials to be bonded with this method have to have a well adhered and oxide-free metal surface such as silver or gold [67]. Since the studied IGBT in [59] had a gold layer on its contact pads and the diode had a silver layer on cathode and anode contacts, the chips were able to be joined to the DBC by the low temperature joining technique, and thus there was no solder layer in between the chips and DBC.

As shown in Figure 2.15, each microchannel heat sink was formed in between two DBCs and was made by joining copper plates with short bridges. This packaging design gave a thermal resistance of 0.087 K/W at a flow rate of 6 liter/min and a pressure drop of about 350 kPa.

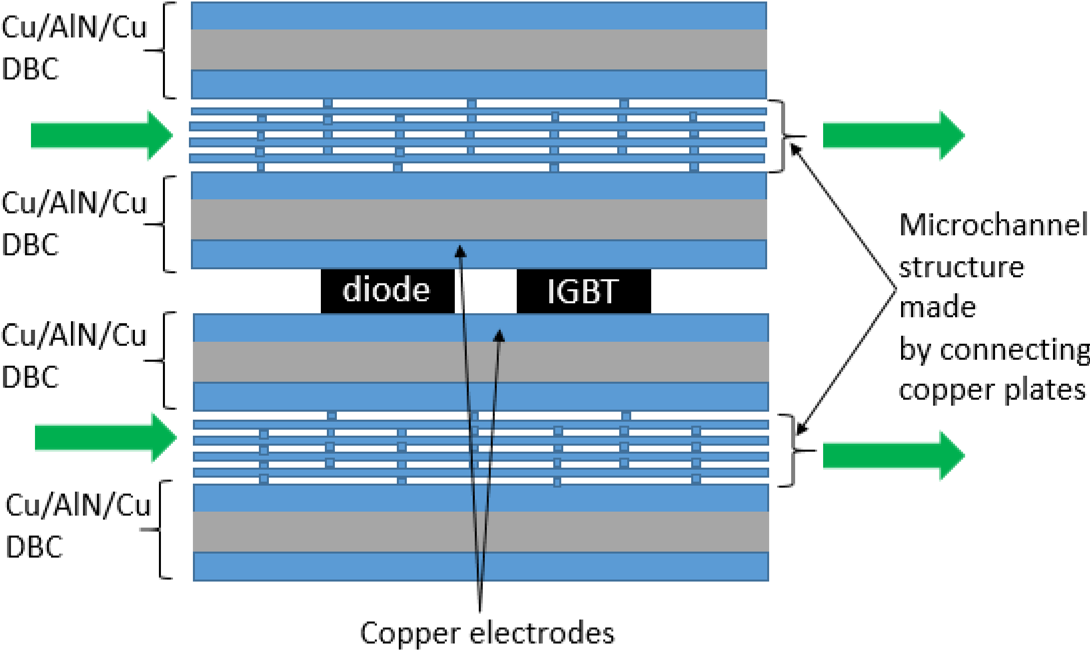

Figure 2.15 Cross section of power semiconductors connected to DBCs using low temperature joining techniques. Contact pads are not shown in this figure.

In order to shorten heat dissipation path between heat source and coolant in double-sided cooling, a new packaging design with microchannel heat sinks integrated into top and bottom DBC substrates was investigated recently [68], as shown in Figure 2.16. Linear fins were featured in the heat sinks. A thermal resistance of 0.11 K/W was found for the double-sided cooling, which was about 35% lower than the single-sided cooling with the same microchannel heat sink geometry.

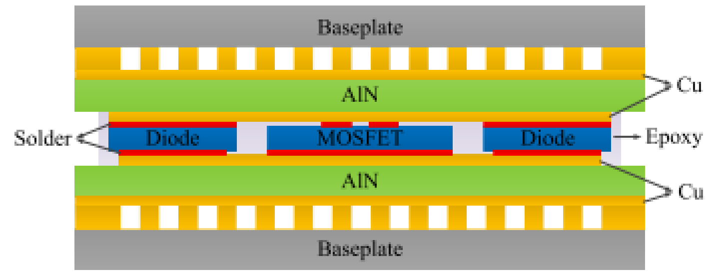

Figure 2.16 Cross sections of a packaging structure with heat sinks integrated into DBC substrates in double-sided cooling [68].

CHAPTER 3
THERMAL-FLUID MODELING OF ALGAN/GAN HEMT

3.1 Introduction

The purpose of this chapter is to report a comparison of the use of passive cooling methods via conduction through the device substrate and active cooling on the thermal performance of AlGaN/GaN HEMTs. Different substrate materials (Si, SiC and diamond) were tried in both passive and active cooling through the integration of microfluidic channels. In addition, the impact of harsh environmental conditions and cooling fluids were also considered. Transient simulations for pulsed conditions were used to show the additional power that could be dissipated under transient operating conditions. The method employed a computational fluid dynamics model to capture the fluid flow, pressure drop, and thermal distribution in the packaged devices. The objective is to determine if active cooling combined with low thermal conductivity substrates can match or outperform passively cooled devices on high thermal conductivity substrates. In addition, the maximum performance expected from single phase integrated active cooling on the performance of AlGaN/GaN is provided.

3.2 Chip Definition, Device Geometry and System Layout

3.2.1 Baseline Passively Cooled Devices

In this study, the junction temperatures in AlGaN/GaN HEMTs on Si, SiC, and diamond substrates were investigated. Si was considered for AlGaN/GaN HEMT due to its low cost (ten times cheaper than SiC) which may lower the overall cost of devices such as power electronics.

SiC is a more commonly used material due to its high thermal conductivity and is primarily used in applications involving high power densities and has been under development for the past 30 years. Finally, diamond has the highest thermal conductivity (~1200 W/mK) but also the highest cost and is relatively new in terms of the development of AlGaN/GaN HEMTs. The structure of the devices considered involve AlGaN/GaN HEMTs with 30 fingers (gates), which can be found in some commercially available power amplifier devices. While devices with as many as 120 fingers can be found and will require additional demands on the thermal management scheme, 30 finger devices were chosen as they are relevant commercially, but also balance the need for computational time with increasing number of elements required to capture the device thermal response. A gate width of 150 μm was chosen as this width is consistent with Monolithic Microwave Integrated Circuits (MMIC) [69]. A multi-finger interdigitated HEMT structure is shown in Figure 3.1.

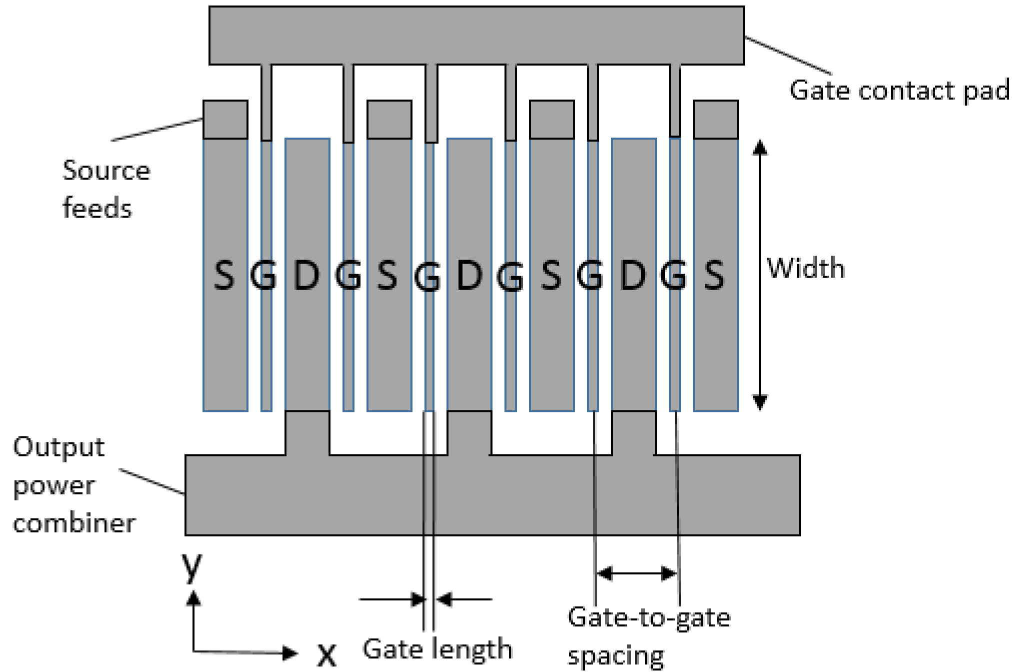

Figure 3.1 Close-up of a 6-finger interdigitated HEMT structure showing source (S), gate (G) and drain (D) electrodes.

It has been found in numerous studies that the localized heating occurs on the drain side edge of the gate, as shown in Figure 3.2, as a result of the combination of electric field spike, complex phonon interaction and ballistic transport effects [5]. In order to estimate this heat source under each gate electrode, a linear heat flux area with 0.5 μm in length (x-direction) and 150 μm in width (y-direction) was used on top of the thermal model while neglecting the details of the electrode contacts.

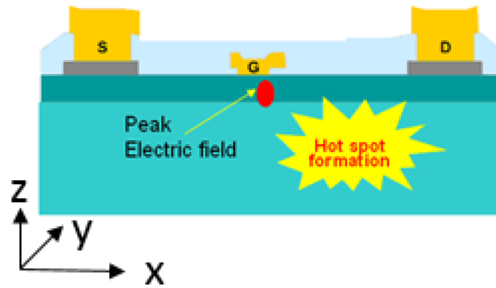

Figure 3.2 Location of hotspot formation in operational AlGaN/GaN HEMT [5].

The dimensions of the die were 2 mm long and 1 mm wide and was attached to a commercially available CuW microwave Lead Amplifier Package (product number: LAP580274 from Stratedge), as shown in Figure 3.3, with a 50 µm thick AuSn solder die attach layer. Then, the CuW package was mounted on a heat sink (a copper cold plate) using 50 µm thick thermal epoxy. The copper plate, which was liquid cooled (at 300K), was a lot larger than the CuW package. It was set to be 4 cm long by 2 cm wide in the model. The detailed model of the die with a package on the cold plate is shown in Figure 3.4. The thermal properties of each material and the thickness of each layer are listed in Table 3.1 and Table 3.2. These material properties are experimental results from different sources.

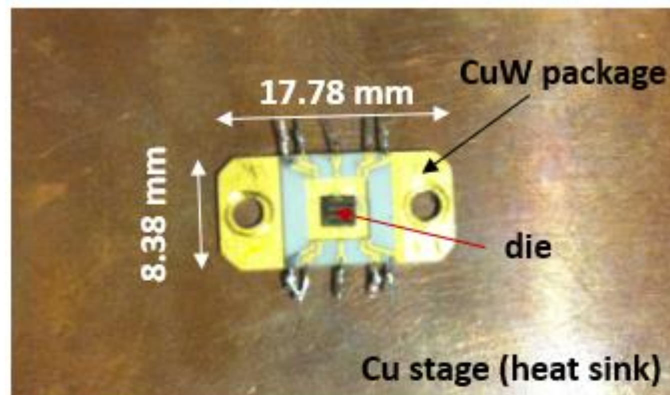

Figure 3.3 A die on a CuW Lead Amplifier Package, which was placed on a Cu heat sink.

Figure 3.4 also shows additional details in the structure of the device. AlGaN/GaN HEMTs are heterostructured devices that involve the growth of a thin layer of AlGaN (~20 nm) on top of a GaN layer that can be as thick as 2 μm. Due to the lattice mismatch with the substrate, a buffer layer between the GaN layer and the substrate is included that introduces a thermal boundary resistance. This buffer layer can be as large as 100 nm. Finally, the various substrates (Si, SiC, and diamond) can range between 30-200 μm. Simplifications to the structure for modeling purposes will be discussed in section 3.3.

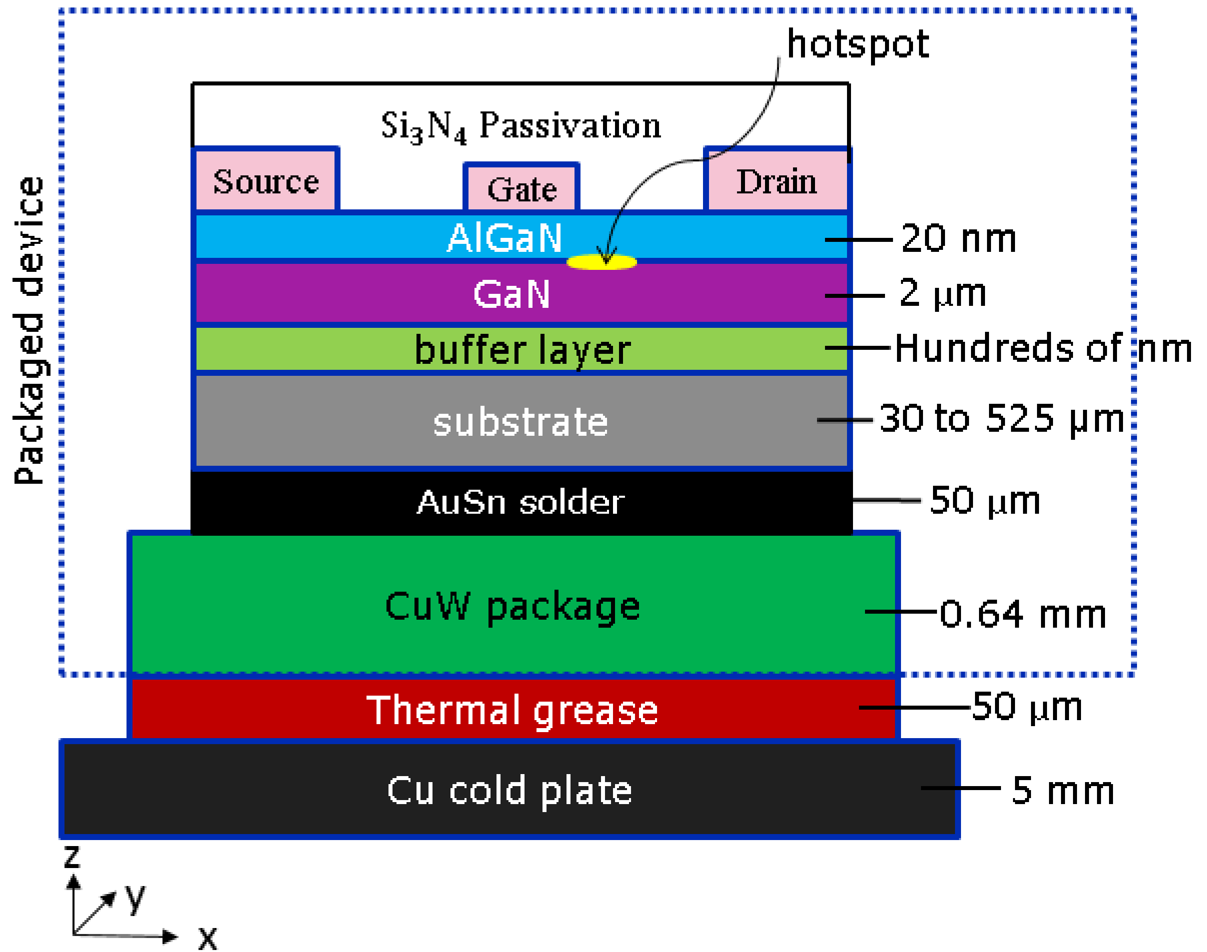

Figure 3.4 Schematic of a cross-section of a packaged AlGaN/GaN HEMT device on a Cu heat sink. Figure not drawn to scale.

Table 3.1 . Thermal conductivity [70] [71] for all substrates and the thermal boundary resistance (tbr) [9] [72] between the substrate and the GaN layer. tbr for both the 1st and 2nd generation GaN-on-diamond devices [9] are shown. * is in plane and ** is out of plane.

Substrate	Thermal conductivity [W/m-K]	Thermal Boundary Resistance [x 10^{-8} $W^{-1}m^2K$]
SiC	$387 \times [\frac{T}{293}]^{-1.49}$	3.3
Si	$148 \times [\frac{T}{300}]^{-1.3}$	3.3
Diamond	$0.003 \times T^2 - 4.238 \times T + 2478$ * $0.0024 \times T^2 - 3.397 \times T + 1983$ **	108 (1st), 3.6 (2nd)

Table 3.2 Thickness and thermal conductivity [70] of the materials used in simulations.

Material	Thickness [μm]	Thermal Conductivity [W/m-K]
GaN	2	$150 \times [\frac{\mathrm{T}}{300}]^{-1.4}$
AuSn/Solder	50	57
CuW	640	$204 - 0.0251 \times \mathrm{T} - 0.0000762 \times \mathrm{T}^2$
Epoxy	50	2.5
Cu	5000	387

3.3 Model Definition

In passive cooling of these devices as shown in Figure 3.5, heat dissipates through substrate from heat sources to the copper cold plate which has a fixed temperature. To model this cooling set up, a constant temperature of 300 K was used at the bottom of the copper plate which represents the center of the cold plate where fluid is flowing. In this passive cooling case, HEMT devices on Si, SiC, and diamond substrates with different substrate thickness and gate to gate spacings of 30 μm, 40 μm and 50 μm were analyzed. In all the cases, thermal simulations were performed for the entire system, accounting for multiple length scales in one model. The 20 nm AlGaN barrier layer, as shown in Figure 3.4, was ignored in the thermal modeling assuming that it would not contribute greatly to the total thermal resistance. The buffer/transition layer between GaN and the substrate was replaced by a Thermal Boundary Resistance (TBR) in the thermal model. The values of TBR for difference substrates are shown in Table 3.1, are taken from experimental measurements in the literature [9][72]. The Joule heating in the channel was approximated by a surface heat flux on top of the GaN layer with an area of 150 μm wide by 0.5 μm long, as shown in Figure 3.6.

3.3.1 Finite Volume Model of Passive Cooling

A 3D model accounting for the aforementioned simplifications was created for the passive cooling of the AlGaN/GaN HEMTs which is shown in Figure 3.5. The material properties used for these simulations are given in Table 3.1 and Table 3.2. All surfaces, except the heat flux regions and the bottom surface of the copper plate were set as adiabatic. The bottom surface of the copper plate was set to a constant temperature T=300K. Due to the symmetric nature of the problem, only a quarter of the system was simulated.

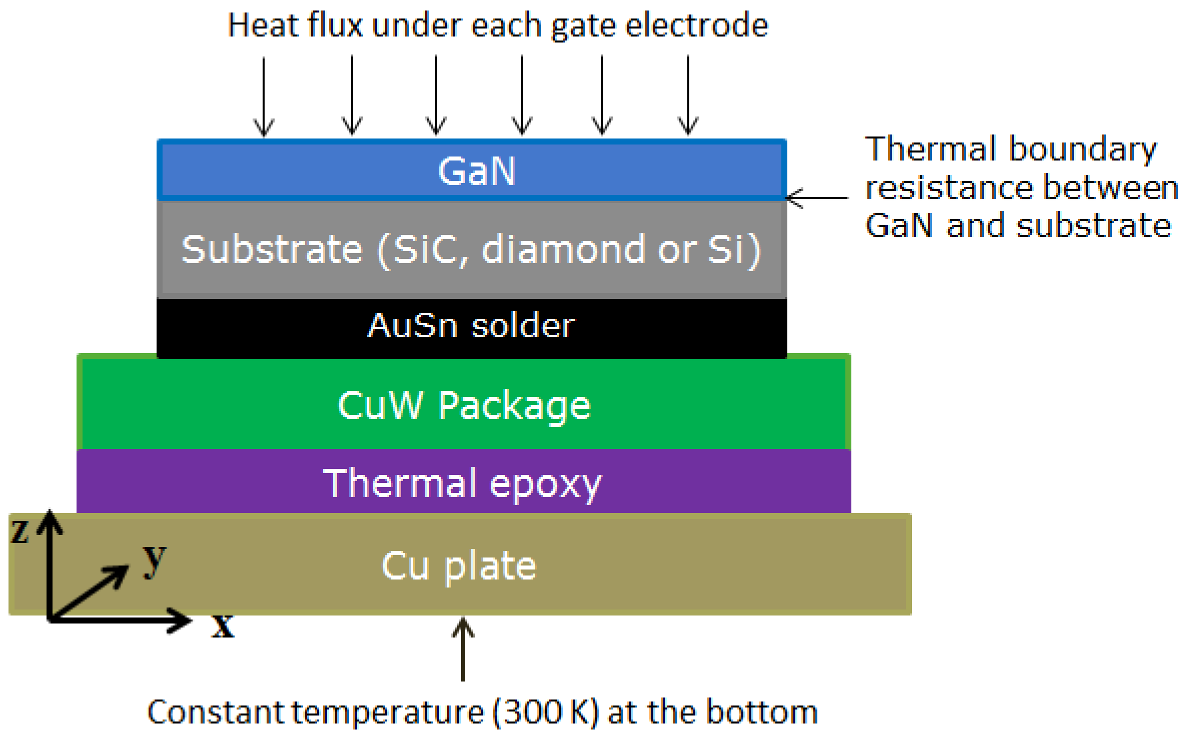

Figure 3.5 Side view of a 3-D model for passive cooling. A constant temperature of 300 K is applied at the bottom of the Cu plate. Heat flux is applied on top of GaN layer as shown in Figure 3.6.

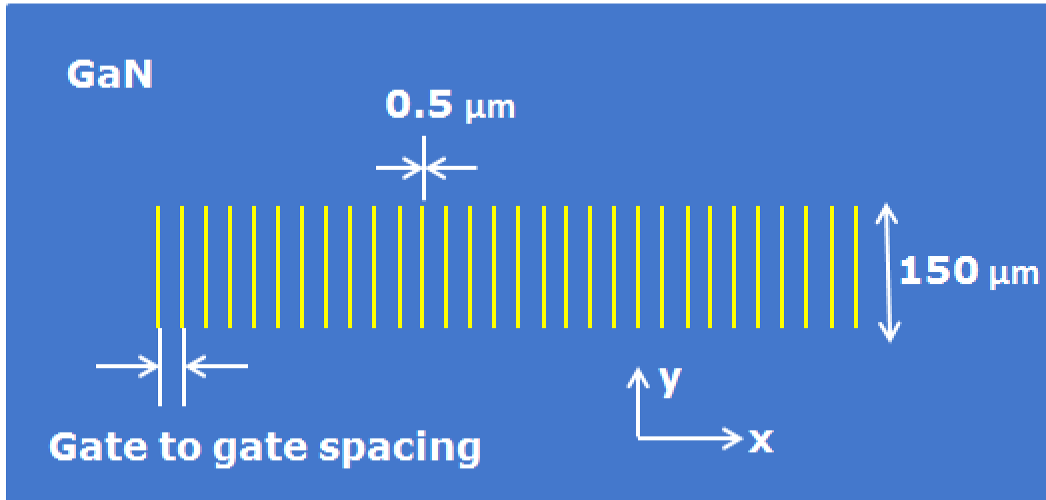

Figure 3.6 A top view of a 3-D thermal model with 30 identical heat flux areas (for 30-finger device) on top of GaN layer. Dimensions of the heat flux area are labeled.

One of the approaches to reduce the overall thermal resistance of the package in the passive cooling approach is to minimize the thermal resistance of the substrate which provides heat spreading and a 1-D resistance to heat flow. In this study, the effect of the substrate thickness on the peak temperature was investigated. The optimum thickness for each substrate material was found as a function of gate-to-gate spacing of 30 μm, 40 μm and 50 μm. The optimal thickness was then used in subsequent geometries modeled in this study.

In another approach to passive cooling, the introduction of high thermal conductivity diamond vias as a heat spreading method was investigated. This can be achieved by locally etching the relatively low thermal conductivity silicon substrate under the heat source and filling it with high thermal conductivity CVD diamond [47], as shown in Figure 3.7. The diamond thermal vias is expected to spread the heat under the active area.

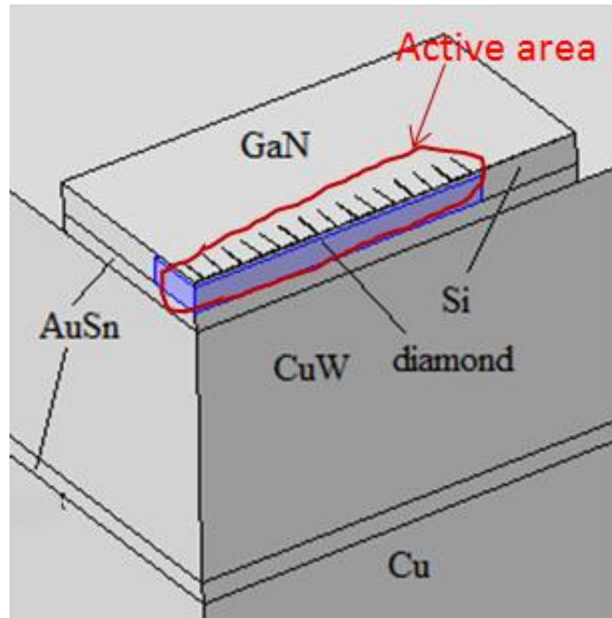

Figure 3.7 Diamond filled thermal vias inside Si substrate. Only a quarter of the model is shown.

3.3.2 Active Cooling Using Integrated Microchannels

Another method to effectively remove heat and reduce the junction temperature is to integrate liquid cooling as close to the junction as possible. This can be done by integrating a microchannel cooler directly under the die as shown in Figure 3.8. The microchannels can be formed in a separate substrate and attached to the rear side of the die since it is not practical to form microchannels directly on the die with active devices [73].

Thermal-fluid simulations for the whole system were performed using ANSYS Fluent software. Due to the symmetric nature of the problem, only half of the system was modeled. Both GaN-on-Si and GaN-on-SiC with integrated microchannel coolers were analyzed with linear fin and pin fin microchannels.

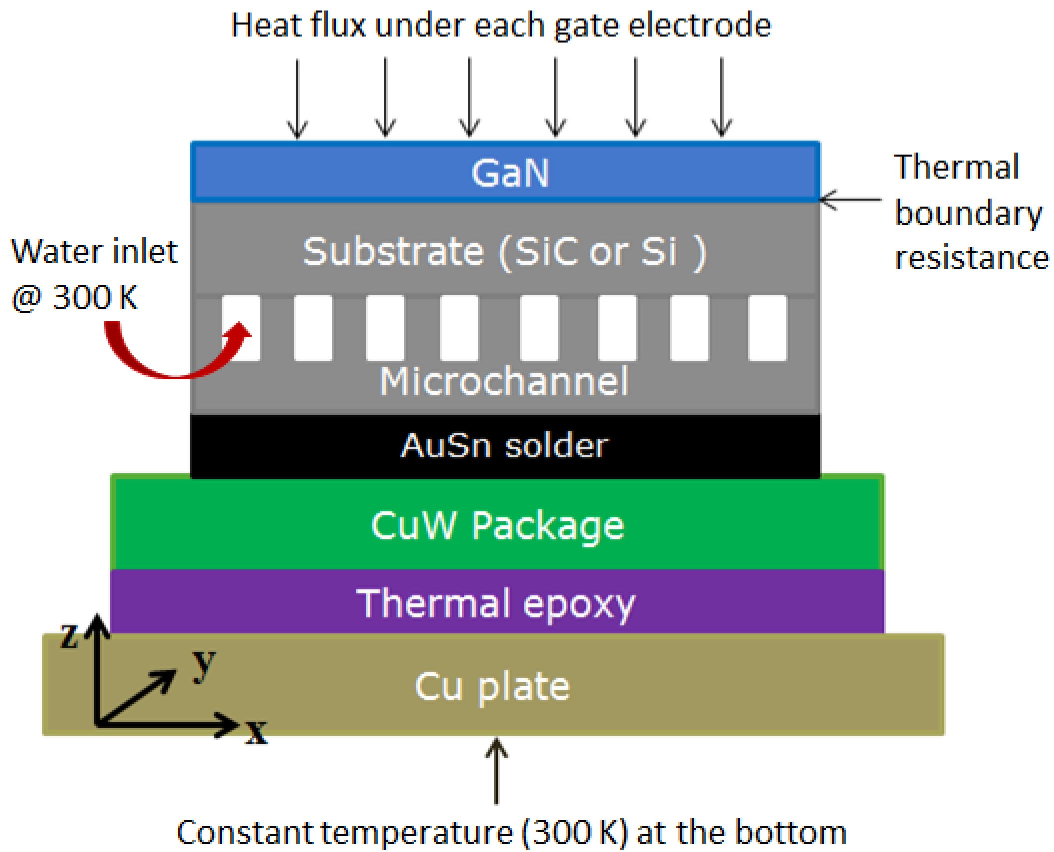

Figure 3.8 Side view of a 3-D model for microchannel cooling with microchannels built on a Si or SiC wafer and attached to the Si or SiC substrate. A constant temperature of 300 K is applied to the bottom of the Cu plate. Heat flux is applied on top of GaN layer as shown in Figure 3.6

3.3.2.1 (a) Microchannel Cooler with Linear Channels

The first microchannel cooler considered contained an array of linear fins as shown in Figure 3.9 (a). Practical dimensions for the cooler were taken from previous studies [73] where Si microchannels were successfully fabricated and used in experiments. The Si microchannels attached to the backside of the substrate has a height H_c of 250 μm and a width W_c of 35 μm. The wall thickness W_t is 25 μm. There are 32 channels in total, as shown in Figure 3.9 (a). In order to have a fair comparison in thermal performance between the Si microchannels and the

SiC microchannels, the same microchannel dimensions were used for the SiC microchannel cooler. The high aspect ratio of the SiC etching used here has been studied and shown to be feasible [74] [75]. Water was used as the coolant with an inlet temperature of 300 K and a flow rate varied from 8.4 mL/min to 230 mL/min. At 230 mL/min, the pressure drop reached 200 kPa, which was the upper limit for pressure drop set in this study. All surfaces except the heat flux area under each gate electrode, the fluid-solid interface, and the bottom surface of the copper plate, were set as adiabatic boundary conditions. As with the passive cooling case, a constant temperature of T=300 K was applied to the bottom surface of the copper plate. The Cu cold plate was kept here because some amount of heat is expected to flow via conduction to the cold plate which depends on the fluid flow rate. The amount dissipated through the cold plate is expected to increase as fluid flow rate in the microchannel decreases. For each flow rate, simulations were repeated as a function of power density (or heat flux) until the junction temperature reached 200 °C. This thermal limit along with the maximum pressure drop of 200 kPa were used to define the maximum power density that could be dissipated in the devices.

3.3.2.2 (b) Pin Fin Microchannel

As an alternative to the linear fin microchannel, a pin fin microchannel cooler was investigated. Pin fin microchannels have been actively studied as they can increase the turbulence intensity or mixing of the fluid flow and thereby exhibit a higher convective heat transfer coefficient and more effective heat removal by the heat transfer fluid [76][55][54][56]. Therefore, a pin fin microchannel cooler was considered to determine its potential benefits for single phase liquid cooling.

In this study, staggered pin fins with different diameters (D), longitudinal spacing (S_L) and transverse spacing (S_T), as shown in Figure 3.9 (b) and (d), were studied. Identical to the

linear fin microchannel, the height of the pin fins are also 250 μm. Water at an inlet temperature of 300 K was used as the coolant. A maximum pressure drop of 200 kPa was used as a pressure drop limit while the maximum power density was found by limiting the maximum junction temperature to 200 °C. Different pin fin diameter and spacing, as shown in Table 3.3, were studied and compared.

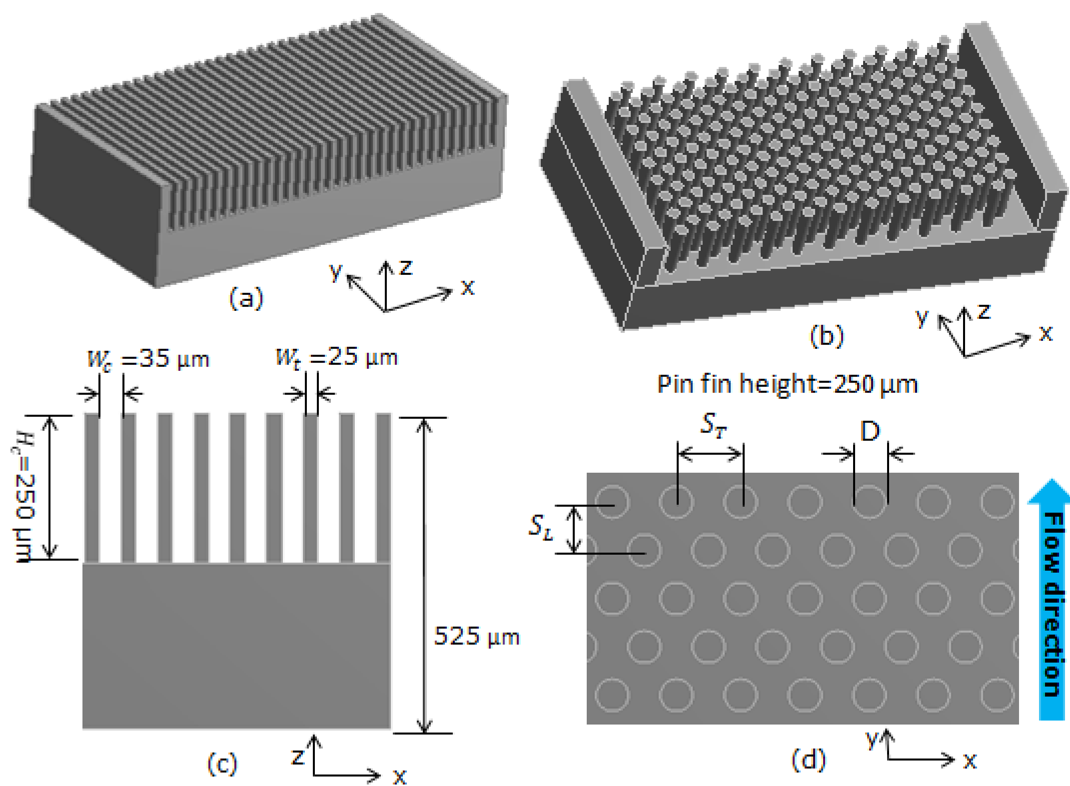

Figure 3.9 (a) Linear fin microchannel cooler and (b) pin fin microchannel cooler that can be attached to the substrate. (c) A side view of the linear microchannel cooler with dimensions of the channels and (d) a side view of the pin fin microchannel cooler.

Table 3.3 Pin fin diameters and spacings for pin fin microchannels. S_L represents longitudinal spacing and S_T represents transverse spacing.

Symbol	Diameter [μm]	S_L [μm]	S_T [μm]
PF1	50	100	100
PF2	50	75	100
PF3	50	50	100
PF4	60	60	90
PF5	50	50	75
PF6	40	40	60

3.4 Numerical Analysis

3.4.1 Numerical Assumptions

The following assumptions were made for all simulations:

1) The fluid remained single phase and flow remained laminar.

The Reynolds numbers were calculated using the following equations:

$$Re \equiv \frac{\rho u_{avg} D_h}{\mu} \tag{3-1}$$

$$for\ linear\ fin,\ \ D_h \equiv \frac{4A}{P} = \frac{2H_c W_c}{W_c + H_c} \tag{3-2}$$

$$for\ pin\ fin,\ \ D_h \equiv \frac{4A}{P} = \frac{2H_c (S_T - D)}{(S_T - D) + H_c} \tag{3-3}$$

where ρ is density, u_{avg} is the mass average of velocity, H_c is channel height, W_c is channel width. D is diameter, and S_T is transverse spacing for pin fins.

2) The system operates in steady state.

3) The water has constant properties except viscosity. The temperature dependent viscosity of water is given by [54]:

$$\mu = 2.414 \times 10^{-5} \times 10^{\left(\frac{247.8}{T-140}\right)} \tag{3-4}$$

where μ is viscosity and T is temperature in Kelvin. The justification to the assumption of using constant density, heat capacity and thermal conductivity of water can be found in [77] and [78].

4) Solid materials including Cu, AuSn solder, and thermal epoxy have constant thermal conductivities.
5) Radiation and natural convection were negligible.
6) The thermal effect of AlGaN layer was negligible because of its small thickness (~20 nm).
7) The thermal effect of the buffer layer between GaN and substrate can be simplified and modeled with an added thermal boundary resistance.
8) Only constant Joule heating is considered (no coupled electrical effects).
9) The bottom of the Cu plate can be maintained at a constant temperature (ambient temperature).

3.4.2 Mesh Generation

A mesh sensitivity analysis was done to ensure that the junction temperature does not change more than 1% when the number of elements increased by 0.5 million, as shown in Figure 3.10. The mesh of the whole system consisted of around 2-million tetrahedral elements for the passive cooling model and more than 5-million tetrahedral/quadrilateral elements in the active cooling model. Figure 3.11 shows the meshing of the whole modeling system in liquid cooling (only half of the system was modeled due to the symmetric nature of the problem). From the Cu plate at the bottom up to the device at the top, the element size decreases to account for the larger

gradients in temperature in the device. The dark region at the top in this figure is where the die located. Figure 3.12 (a) is a zoom-in view of the die, which consists of the GaN layer, the substrate, and the embedded microchannel on the CuW package. Figure 3.12 (b) is a zoom-in view of the top surface of GaN layer with heat flux regions. Element sizes are much smaller in the heat flux regions. Figure 3.13 shows a top-view of pin fins with water surrounding the fins. An inflation feature with a smooth transition option was applied at the lateral surfaces of pin fins with 5 layers.

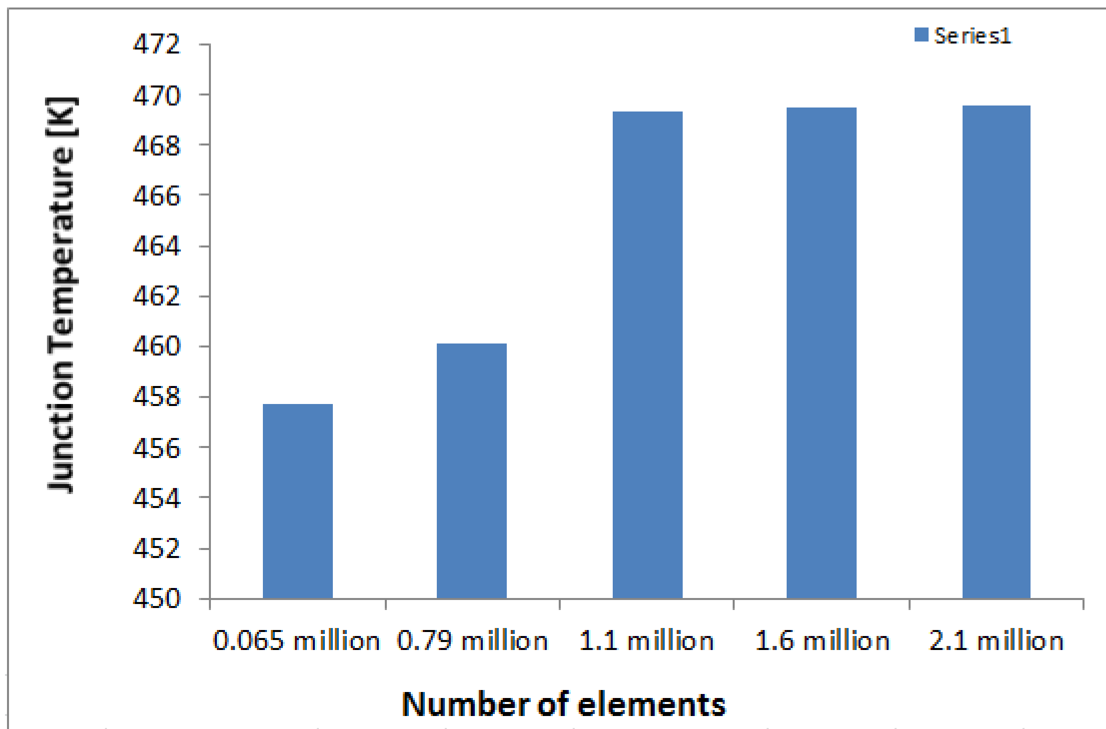

Figure 3.10 Element size sensitivity analysis for passively cooled GaN on Si.

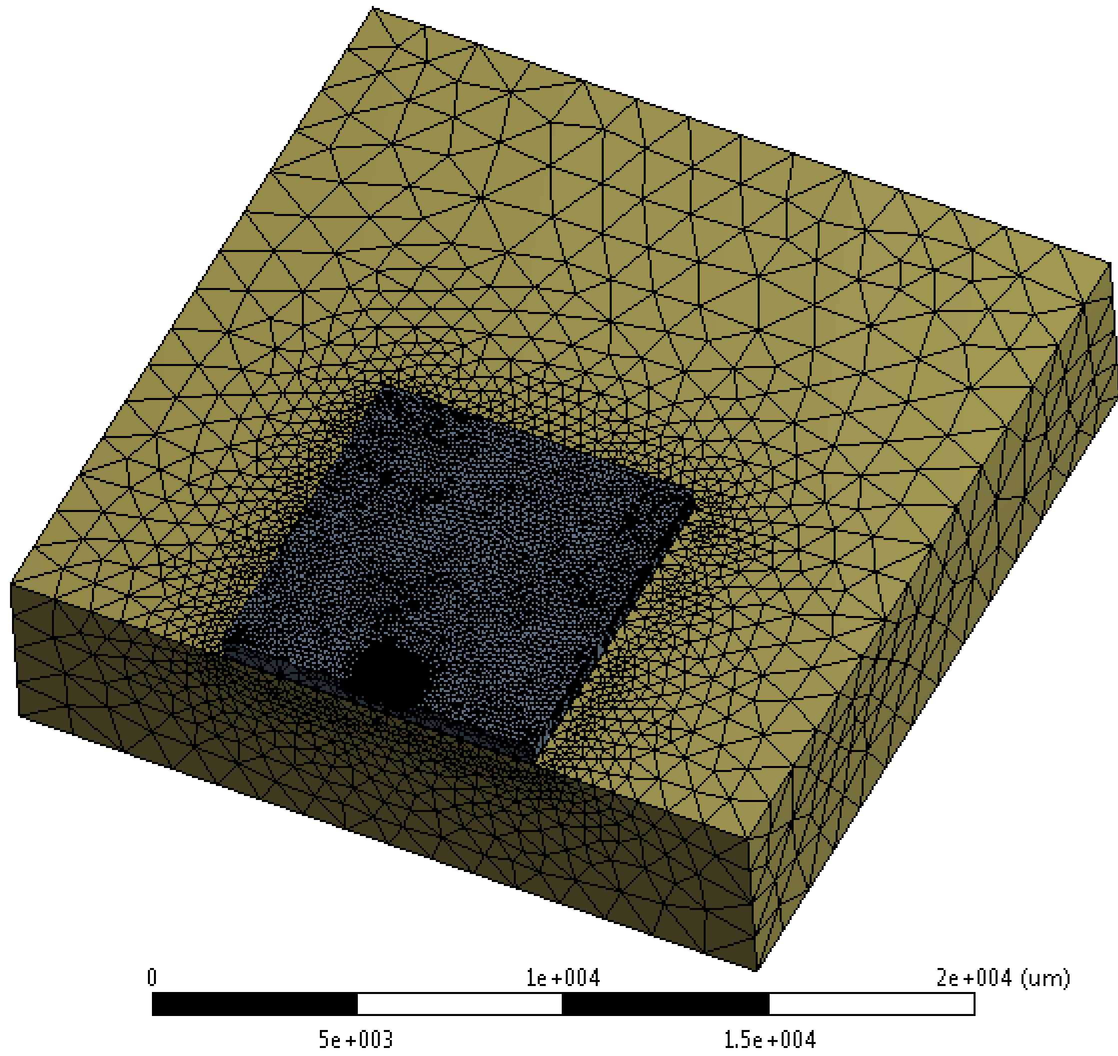

Figure 3.11 Meshing in the system. Due to the symmetric nature, only half of the whole system is shown here.

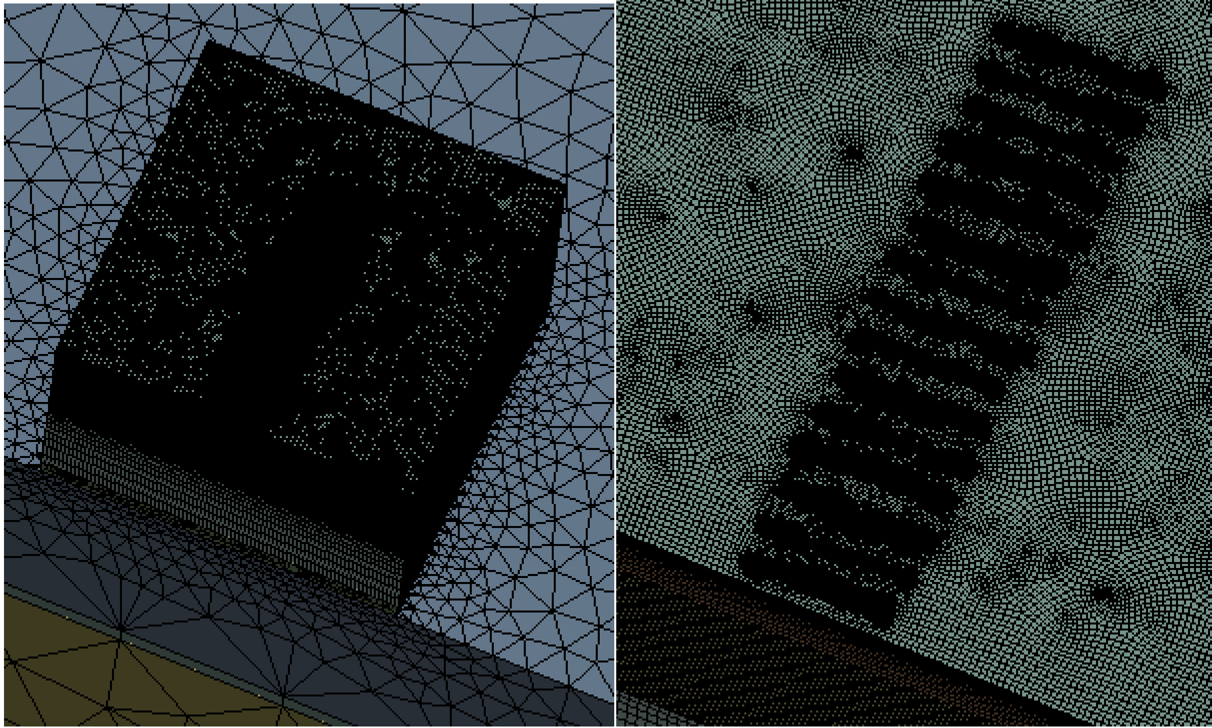

Figure 3.12 Zoom in view of the meshing of (a) device with integrated microchannels and (b) heat flux areas on top of GaN layer.

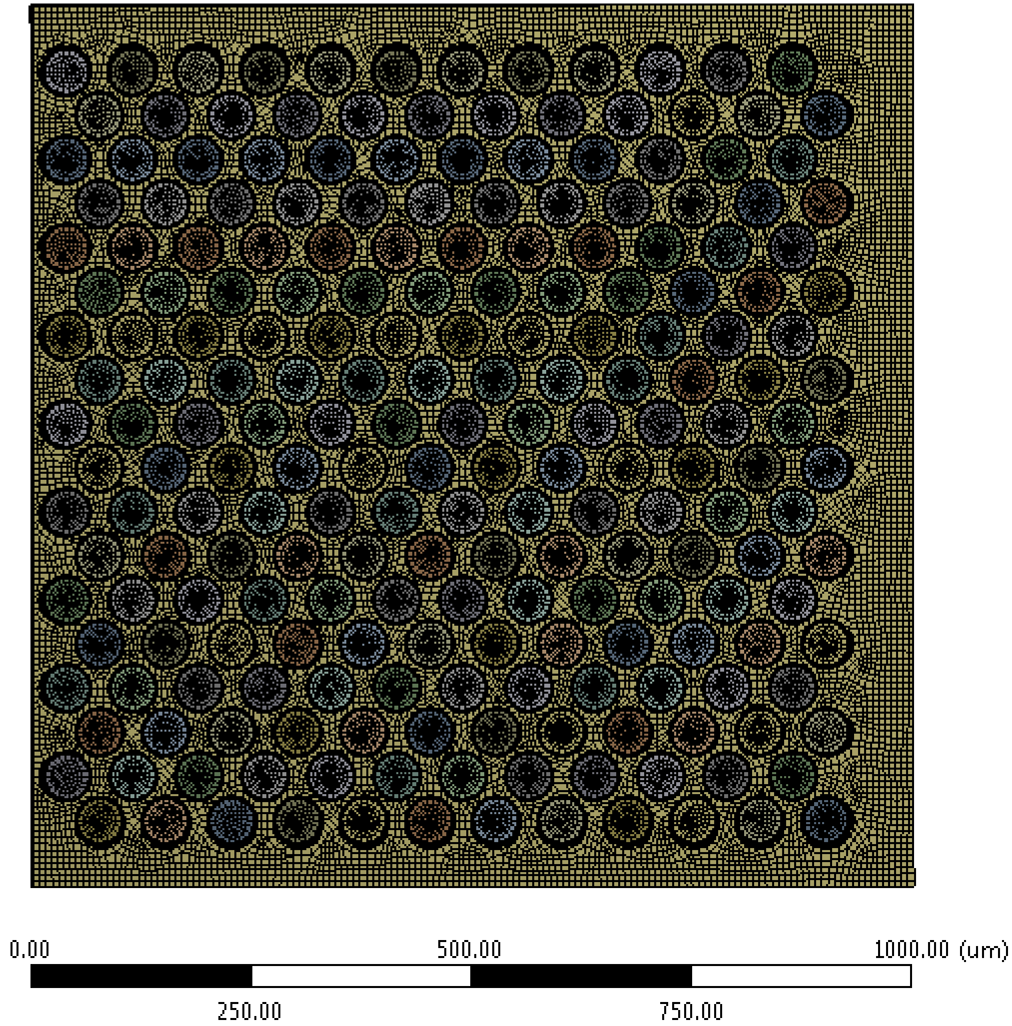

Figure 3.13 Meshing of pin fins with water surrounded by. The dark circles around the pin fins are the inflation layers.

3.4.3 Numerical Model

The SIMPLE algorithm was used for the Pressure-Velocity Coupling and the second order upwind scheme was used for discretization of both momentum and energy. The governing equations for continuity, momentum and energy can be expressed in the flowing equations:

$$\nabla U = 0 \tag{3-5}$$

$$\rho(\vec{U} \cdot \nabla\vec{U}) + \Delta P - \emptyset = 0 \tag{3-6}$$

$$\rho c_p(\vec{U} \cdot \nabla T) - k_f(\nabla^2 T) = 0 \tag{3-7}$$

where ρ is density, U is velocity, P is pressure, c_p is heat capacity, T is temperature, and k_f is thermal conductivity. These are properties of the fluid. $\emptyset$ involves the viscous effects generated in the system due to the relative velocity of the fluid through the channels [54]. The residual for energy was set to 1E-6. The residuals for velocity and continuity were set to 1E-4.

3.5 Results for Steady Heat Flux at Room Temperature

3.5.1 Comparison between analytical solution and computational solution in passive cooling

An analytical method to estimate the overall thermal resistance for GaN on SiC was employed by using the following equations:

$$\theta_1 = \frac{1}{\pi W_g k_{GaN}} \ln\left(\frac{4t_1}{\pi L_g}\right) + \frac{1}{\pi W_g k_{Sub}} \ln\left(\frac{f_1}{f_2}\right) + \frac{1}{\pi s k_{Sub}} \ln\left(\frac{h_1}{h_2}\right) = 98.3\ °C/W \tag{3-8}$$

where $f_1 = \frac{\sqrt{x_{f1}+1}+\sqrt{x_{f1}-1}}{\sqrt{x_{f1}+1}-\sqrt{x_{f1}-1}}$, $f_2 = \frac{\sqrt{x_{f2}+1}+\sqrt{x_{f2}-1}}{\sqrt{x_{f2}+1}-\sqrt{x_{f2}-1}}$, $h_1 = \sqrt{\frac{\sqrt{x_{h1}+1}+1}{\sqrt{x_{h1}+1}-1}}$, $h_2 = \sqrt{\frac{\sqrt{x_{h2}+1}+1}{\sqrt{x_{h2}+1}-1}}$, k is thermal conductivity, w_g is gate width, s is gate-to-gate spacing, L_g is gate length, t_1 is thickness of GaN, and t_2 is thickness of substrate. $x_{f1} = \frac{W_g}{2\rho t_1}$, $x_{f2} = \sqrt{1 + \left(\frac{W_g}{\sqrt{2}s}\right)^2 - \left(\rho\frac{t_1}{\sqrt{2}s}\right)^2}$, $x_{h1} = \left(\frac{W_g}{\pi t_2}\right)^2 - 4\left(\frac{\rho t_1}{\pi t_2}\right)^2$, $x_{h2} = \left(\frac{W_g}{\sqrt{2}s}\right)^2 - 4\left(\frac{\rho t_1}{\sqrt{2}s}\right)^2$.

$$\theta_2 = \frac{t_{solder}}{A_{solder}k_{solder}} = 0.44\ °C/W \tag{3-9}$$

$$\theta_3 = \frac{t_{CuW}}{A_{CuW}k_{CuW}} = 0.02\ °C/W \tag{3-10}$$

$$\theta_4 = \frac{t_{epoxy}}{A_{epoxy}k_{epoxy}} = 0.13\ °C/W \tag{3-11}$$

$$\theta_5 = \frac{t_{Cu}}{A_{Cu}k_{Cu}} = 0.016\ °C/W \tag{3-12}$$

$$\theta_{tot} = \theta_1 + \theta_2 + \theta_3 + \theta_4 + \theta_5 = 99\ °C/W \tag{3-13}$$

where L is the thickness and A is cross-sectional area. θ_1 to θ_5 correspond to thermal resistance in different sections of the model as shown in Figure 3.14. The thermal conductivities of GaN and SiC used in the analytical solution are 119 W/m-°C (at 81 °C) and 297 W/m-K (at 77 °C), respectively. These thermal conductivities are based on average temperatures of the GaN and SiC substrate in simulation.

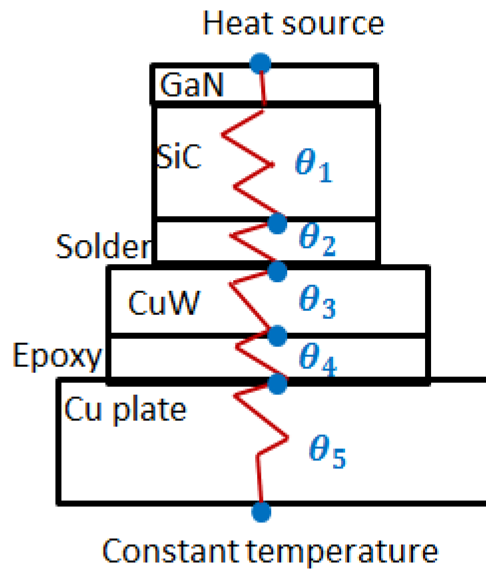

Figure 3.14 Thermal resistance network of passively cooled GaN on SiC.

The equation for calculating the thermal resistance of GaN and substrate (θ_1) is taken from [79] with assumptions including constant thermal conductivity of all the materials and isothermal surface at the bottom of the substrate. Also, this analytical solution does not take the number of fingers or the size of the die into consideration. For GaN on 200 µm thick SiC substrate, the total thermal resistance is found to be 99 °C/W based on the analytical solution,

while it is 206 °C/W (with $\theta_{computational} = \frac{T_{j_avg} - T_{amb}}{P}$ $where$ T_{j_avg} is the average temperature in heat flux areas, and T_{amb} is the ambient temperature, P is the power of one finger) from computational solution with 30 fingers in total. The difference in thermal resistance between the analytical method and computational method is directly related to the effect of multiple heat sources (the number of fingers), which was not taken into account in the analytical solution.

When the device has only one finger, the overall thermal resistance was found to be 91 °C/W base on computational solution, which is very close that (80 °C/W) calculated from the analytical solution. Thermal conductivities of GaN and SiC used in the analytical solution are 147 W/m-°C (at 31 °C) and 368 W/m-K (at 30 °C), respectively. These thermal conductivities are based on average temperatures of the GaN and SiC substrate in simulation. In this case, the analytical solution has a lower value for thermal resistance because the spreading resistances in the AuSn solder, the CuW, the epoxy and the Cu cold plate layers were ignored in the analytical solution.

3.5.2 Passive Cooling

Since both 1-D conduction and heat spreading in the substrate layer contribute to the thermal resistance across the substrate layer, there exists an optimum substrate thickness at which the combined resistance from both mechanisms is the lowest. By varying the substrate thickness from 25 μm to 525 μm and comparing the maximum device temperature under the same power density, we can find the optimum thickness for each substrate material and gate-to-gate spacing (G2G). The results are shown in Figure 3.15 for a power density of 4.1 W/mm. For both SiC and Si substrates, the smaller the gate-to-gate spacing, the higher the peak temperature

is under the same substrate thickness and power density (4.1 W/mm) conditions. This is because although they have the same linear power density (4.1 W/mm), devices with smaller gate-to-gate spacing would have a higher aerial power density in the active area. For SiC, the maximum temperature decreases and then increases as thickness increases, as shown in Figure 3.15 (b). The transition occurs between 200 μm and 300 μm and the optimum thicknesses was observed at 200 μm, 225 μm and 275 μm for 50, 40, and 30 μm gate-to-gate spacing, respectively. For GaN on Si substrate, the optimum thickness occurs at a much smaller thickness. It was found to be 75 μm, 50 μm and 25 μm for 50, 40, and 30 μm gate-to-gate spacing, respectively, as shown in Figure 3.15 (a). The dependency of the peak temperature on substrate thickness can be explained by the combined effect of spreading resistance and 1-D thermal resistance. When the substrate is very thin, the spreading resistance dominates the thermal response. When the substrate is very thick, a 1-D thermal resistance dominates. Si has a smaller optimum thickness than SiC due to the fact that Si has much lower thermal conductivity than SiC. While increasing the substrate thickness helps to decrease the spreading resistance in both SiC and Si substrates, the 1-D thermal resistance increases more rapidly in Si than in the SiC substrate. Therefore, the trade-off in thickness for Si is much smaller than for SiC substrate.

The optimum thickness for each case shown in Figure 3.15 indicates a linear trend between gate-to-gate spacing and optimum thickness. For the SiC substrate, the optimum thickness increases as gate-to-gate spacing decreases while Si substrate has the opposite trend.

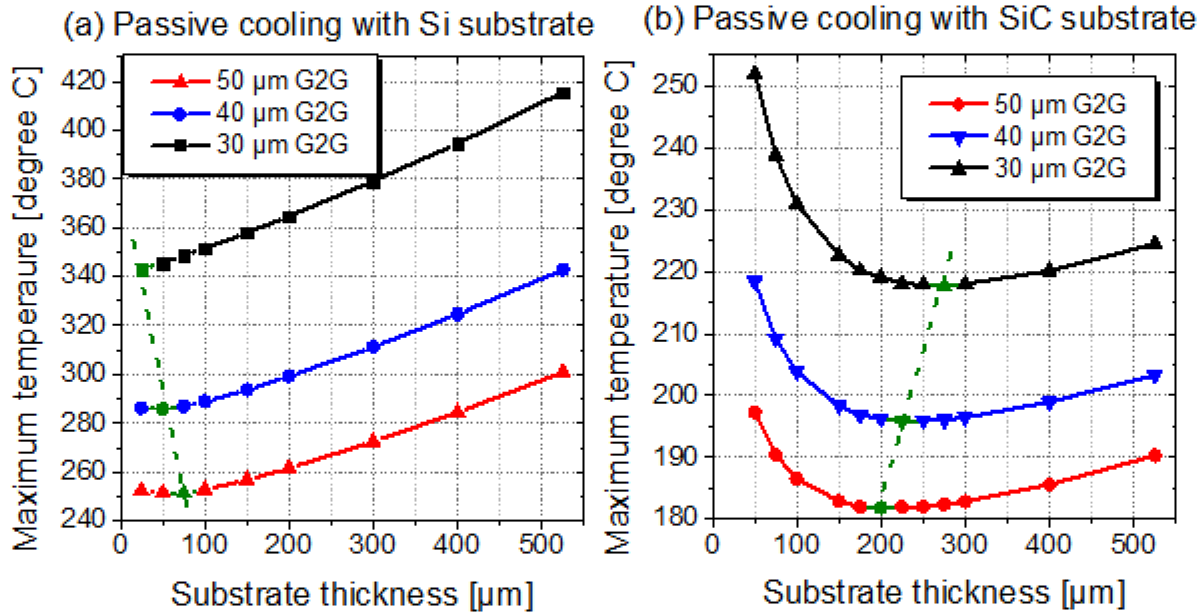

Figure 3.15 Effect of substrate thickness on peak temperature for Si and SiC substrates with different gate-to-gate spacing and a power density of 4.1 W/mm. The green dots represent the optimum thickness for each case.

The thermal resistances for different substrates and gate-to-gate spacing are shown in Figure 3.16. Diamond with thickness of 30 µm, 50 µm, 100 µm and 200 µm are also shown in the figure. GaN on 200 µm diamond has a thermal resistance that is 21% and 45% lower than GaN on SiC and GaN on Si at their optimum thicknesses, respectively. Thermal resistance for GaN on diamond decreases as diamond thickness increases. From 100 µm to 200 µm diamond, there is 3.4% decrease in thermal resistance. The power density for GaN on 200 µm diamond is 5.8 W/mm with a maximum device temperature of 200 °C.

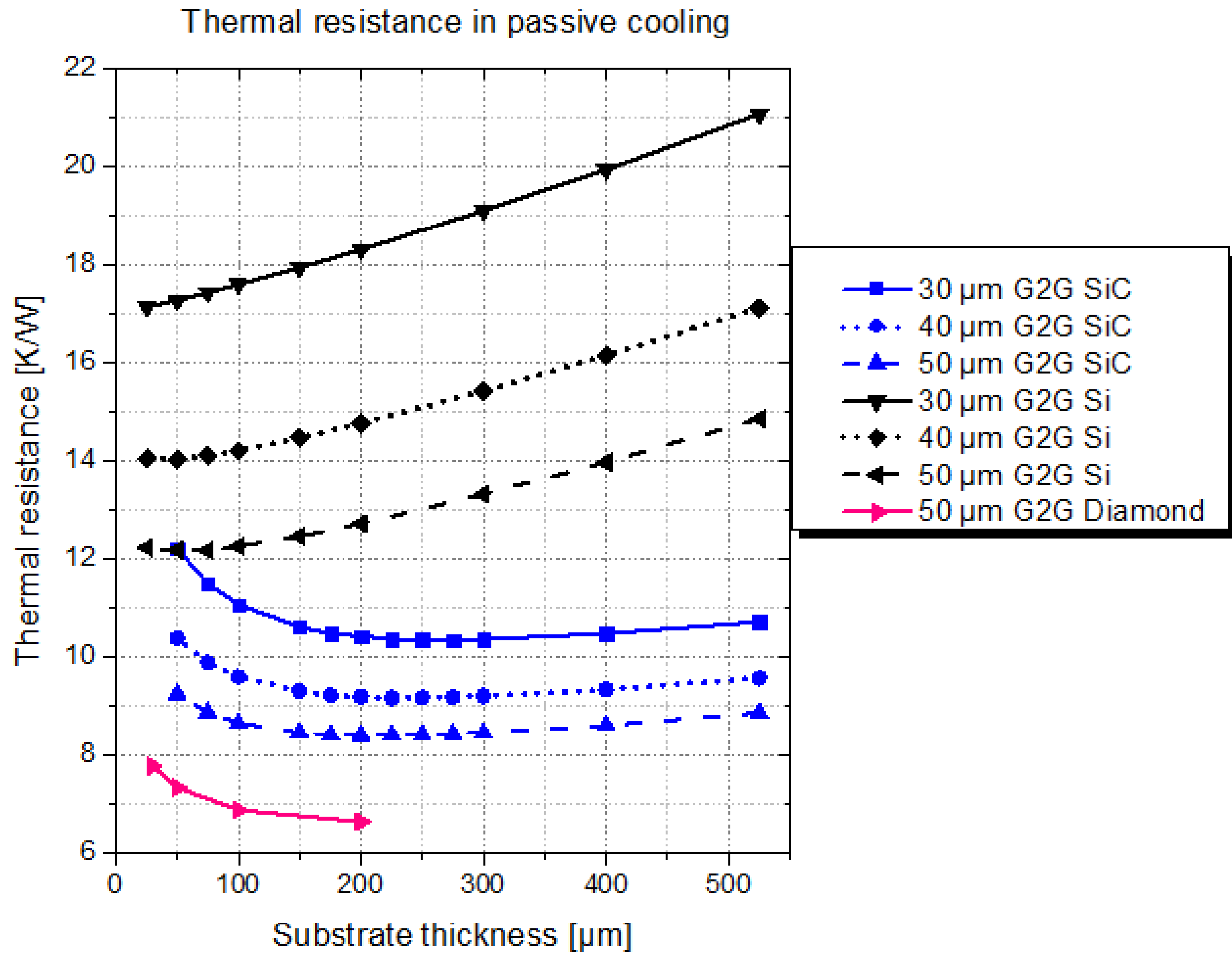

Figure 3.16 Thermal resistances for substrates with different thickness and gate-to-gate (G2G) spacing.

Temperature contours for GaN on optimum and non-optimum thicknesses with 50 µm gate-to-gate spacing are shown in Figure 3.17 and Figure 3.18. For GaN on SiC, the temperature distribution in the 200 µm substrate is much more uniform than in the 50 µm substrate. Therefore, increasing the substrate thickness from 50 µm to 200 µm would allow heat to spread out and reduce the spreading resistance resulting in a low junction temperature. For GaN on Si, temperature distribution in the 525 µm substrate does not show more uniformity than in the 75

μm. Since Si has low thermal conductivity, increasing substrate thickness would rapidly increases the 1-D resistance resulting in a much higher junction temperature.

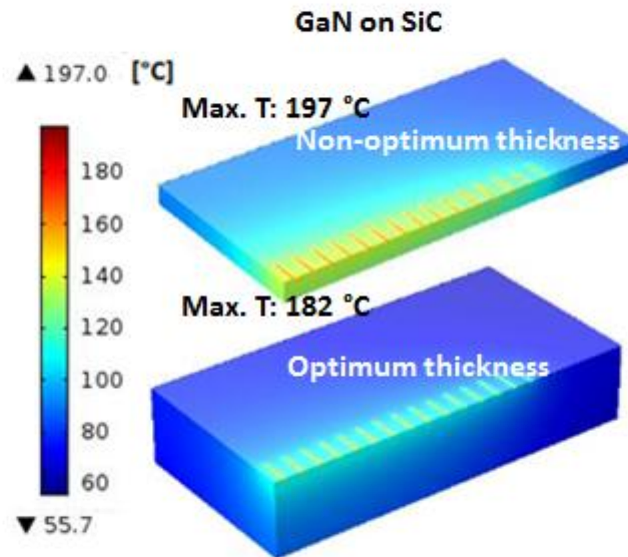

Figure 3.17 Temperature contour for GaN on 50 μm SiC (top) and GaN on 200 μm SiC (bottom) in passive cooling. Gate-to-gate spacing is 50 μm and power density is 4.1 W/mm.

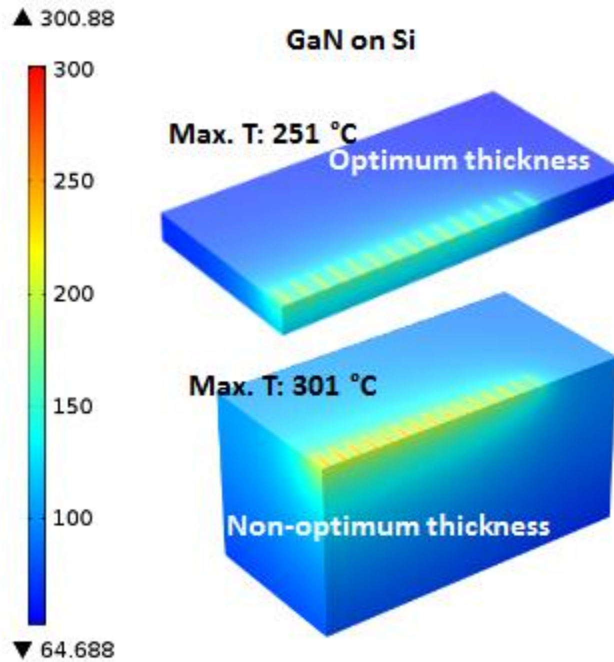

Figure 3.18 Temperature contour for GaN on 75 µm Si (top) and GaN on 525 µm Si (bottom) in passive cooling. Gate-to-gate spacing is 50 µm and power density is 4.1 W/mm.

A more detailed investigation of the active region can be done by plotting the temperature distribution across the gate fingers at the center of the channel, as shown in Figure 3.19 and Figure 3.20. These plots are for 50 µm gate-to-gate spacing. The peaks in these figures represent the junction temperatures of the device channels. The plots show how flat the maximum temperature profile is for the device. Since failure rates are temperature dependent, it is desirable to have a flat temperature profile across a device with a large number of channels to reduce the rate of degradation across the device fingers. It is seen that the temperature difference between the inner-most finger and the outer-most finger is 38 °C for the 50 µm thick SiC substrate and 25 °C for the 200 µm thick SiC substrate. In Figure 3.19, it is clear that the peak temperatures are more uniform with the 200 µm SiC substrate than with the 50 µm substrate. However, this difference is not noticeable for Si, as shown in Figure 3.20. The temperature

difference between the inner-most finger and the outer-most finger is 36 °C for both 525 µm and 75 µm Si substrates. Based on this results and results shown in Figure 3.15, a 200 µm thick SiC substrate and 75 µm thick Si substrate will be used for the analysis of the microchannel cooling in active cooling.

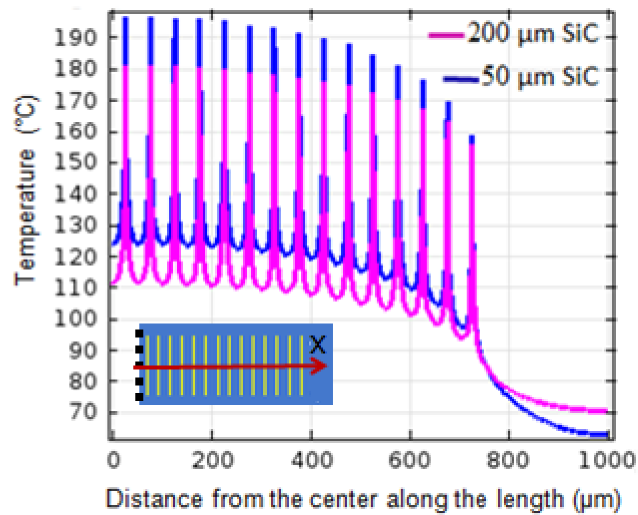

Figure 3.19 The temperature profile across the center of each finger (the center of the width) on the top surface of GaN for GaN on 50 µm SiC substrate (blue) and GaN on 200 µm SiC substrate (pink) with 50 µm gate-to-gate spacing and power density of 4.1 W/mm in passive cooling.

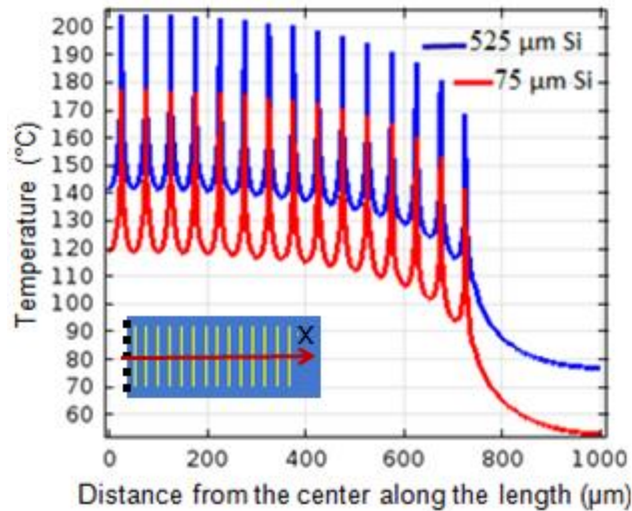

Figure 3.20 The temperature profile along center of each finger (the center of the width) on the top surface of GaN for GaN on 75 μm Si substrate (red) and GaN on 525 μm Si substrate (blue) with 50 μm gate-to-gate spacing and power density of 3 W/mm in passive cooling.

The use of diamond filled thermal vias increased the power density for GaN on Si from 3.3 W/mm to 4.3 W/mm (under the 200 °C maximum temperature condition), which is close to the use of SiC substrate in passive cooling, but less than the use of 30 μm thick diamond substrate (4.95 W/mm). Under the same power density (at 4.1 W/mm), the use of diamond filled thermal vias in Si substrate reduced the peak temperature by 63 °C in passive cooling, as shown in Figure 3.21. In addition, the diamond thermal vias helped to increase temperature uniformity among all the fingers, as shown in Figure 3.22. The difference in peak temperature between the inner-most finger and the out-most finger in the case with thermal vias (18 °C) is much smaller than the case without thermal vias (56 °C).

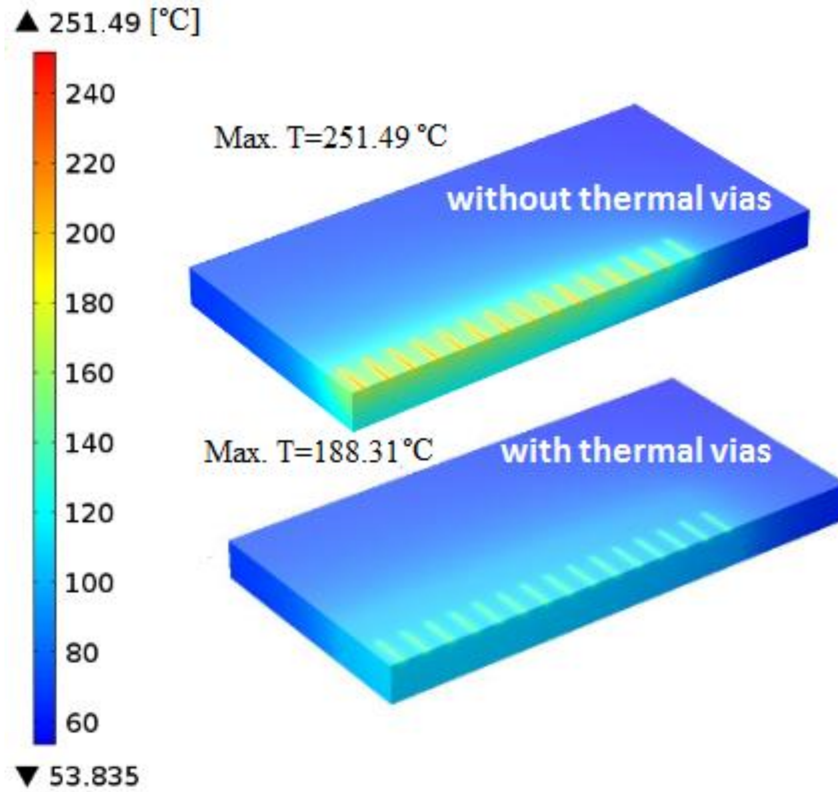

Figure 3.21 Temperature distribution on (a) GaN on 75 μm Si substrate and (b) GaN on 75 μm Si substrate with diamond thermal vias. The power density was 4.1 W/mm. Only a quarter of the whole geometry is shown due to the symmetry nature of the problem.

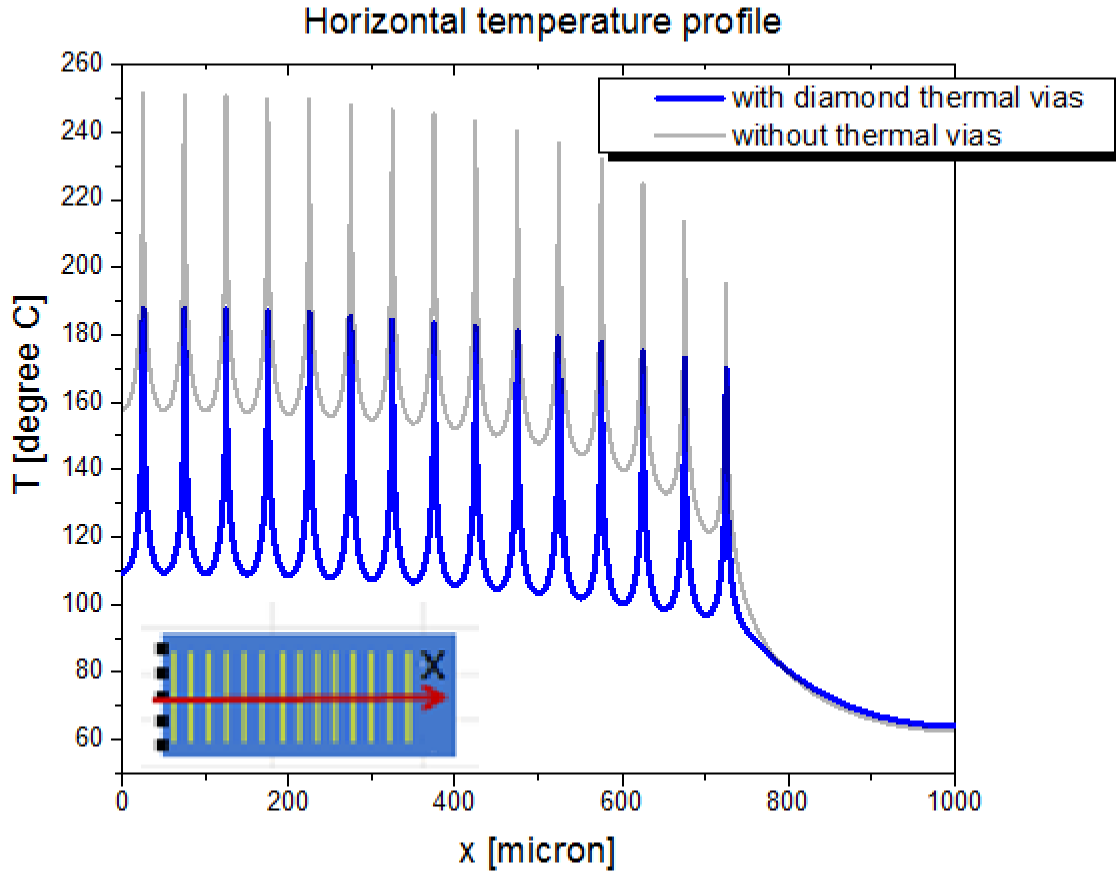

Figure 3.22 The temperature profile along center of each finger on the top surface of GaN for GaN on 75 μm Si substrate with and without diamond thermal vias. Both cases have 50 μm gate-to-gate spacing and power density of 4.1 W/mm.

3.5.3 Microchannel Liquid Cooling

The Reynolds number was found to be between 30.55 and 733.2 for linear microchannels and was between 162.6 and 514.1 for pin fin microchannels using equations (1) to (3). Therefore, the laminar flow model was valid for all simulations. Also the maximum fluid temperature was below its boiling temperature, so the single-phase flow model for all simulations was valid as well.

3.5.3.1 Linear Fin Microchannel Liquid Cooling

With a linear fin array, the maximum power density increases as the volumetric flow rate increases for both GaN on SiC and GaN on Si under a maximum device temperature of 200 °C condition, as shown in Figure 3.23. We found that at low flow rates (<50 ml/min), the power density is very sensitive to flow rate, but as flow rate increases the slop decreases. When the flow rate is low, the hydrodynamic entry length $x_{fd,h}$ is short and the fluid flow becomes fully developed inside the microchannel. The entry length $x_{fd,h}$ for different flow rate is shown in Figure 3.24. At a flow rate of about 70 ml/min, $x_{fd,h}$ reaches 1000 µm, which is the length of the linear microchannel. Therefore, fully developed flow occurs inside the microchannel when the flow rate is less than 70 ml/min. In the fully developed region, the local Nusselt number becomes constant and thus the heat transfer coefficient becomes constant [80]. At this point, increasing flow rate will increase the entry length and decrease the fully developed region inside the microchannel. This phenomenon accounts for the high sensibility of power density to flow rate at low flow rates. When further increasing the velocity, the bulk fluid temperature rise decreases but at a decreasing rate, although the power dissipation is increasing, as shown in Figure 3.25. At a flow rate of about 200 ml/min, the bulk fluid temperature rise is near constant. So the junction temperature becomes less sensitive to the velocity. Devices with smaller gate-to-gate spacing have to operate at a lower power density than devices with greater gate-to-gate spacing under the same flow rate and maximum device temperature conditions, as shown in Figure 3.23. At a flow rate of 230 mL/min, the pressure drop reaches 200 kPa, which was the upper limit for pressure drop in this study.

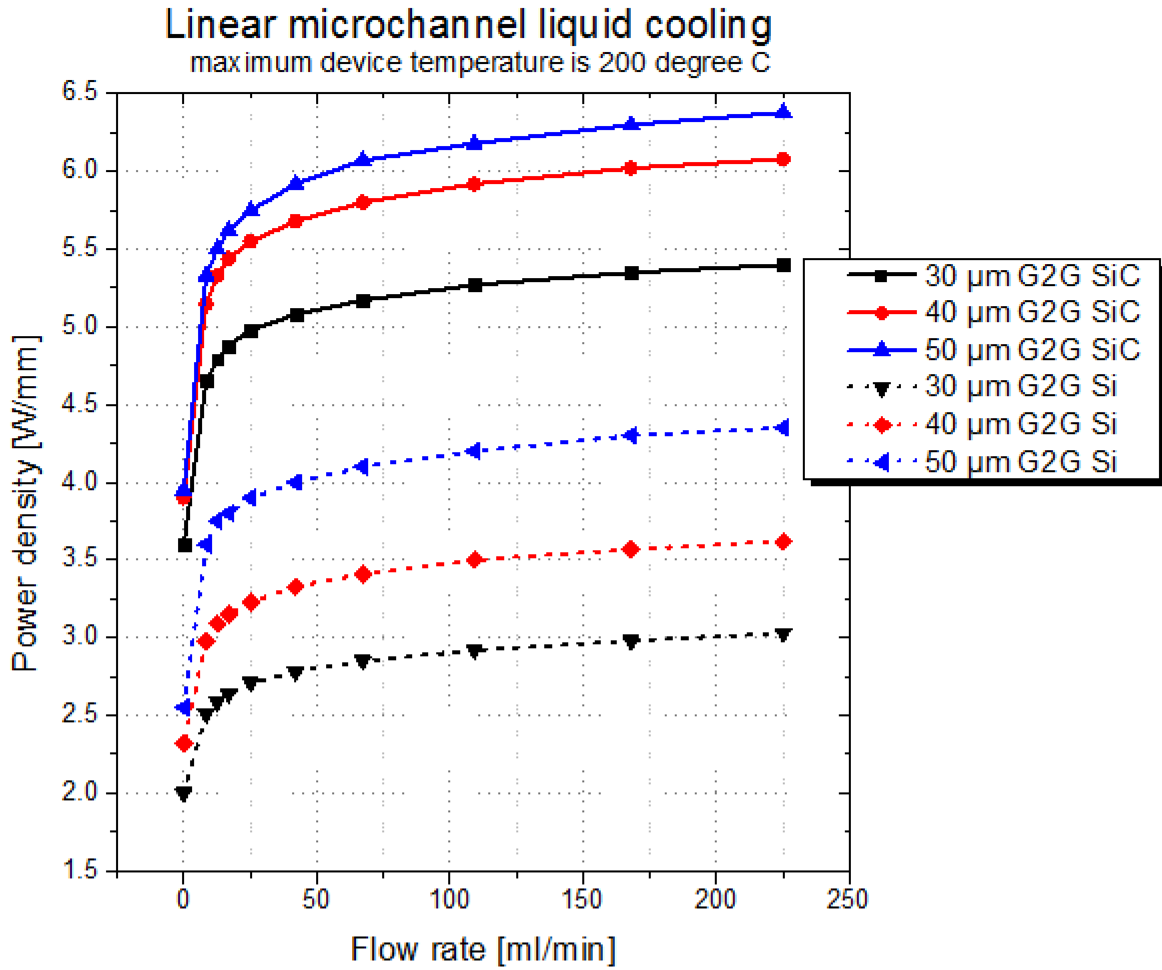

Figure 3.23 Power density vs. volumetric flow rate for different gate-to-gate spacing "G2G" and substrate materials. The power density corresponds to the maximum power density in the device to have a junction temperature no higher than 200 °C. Optimum thicknesses were used for the substrates.

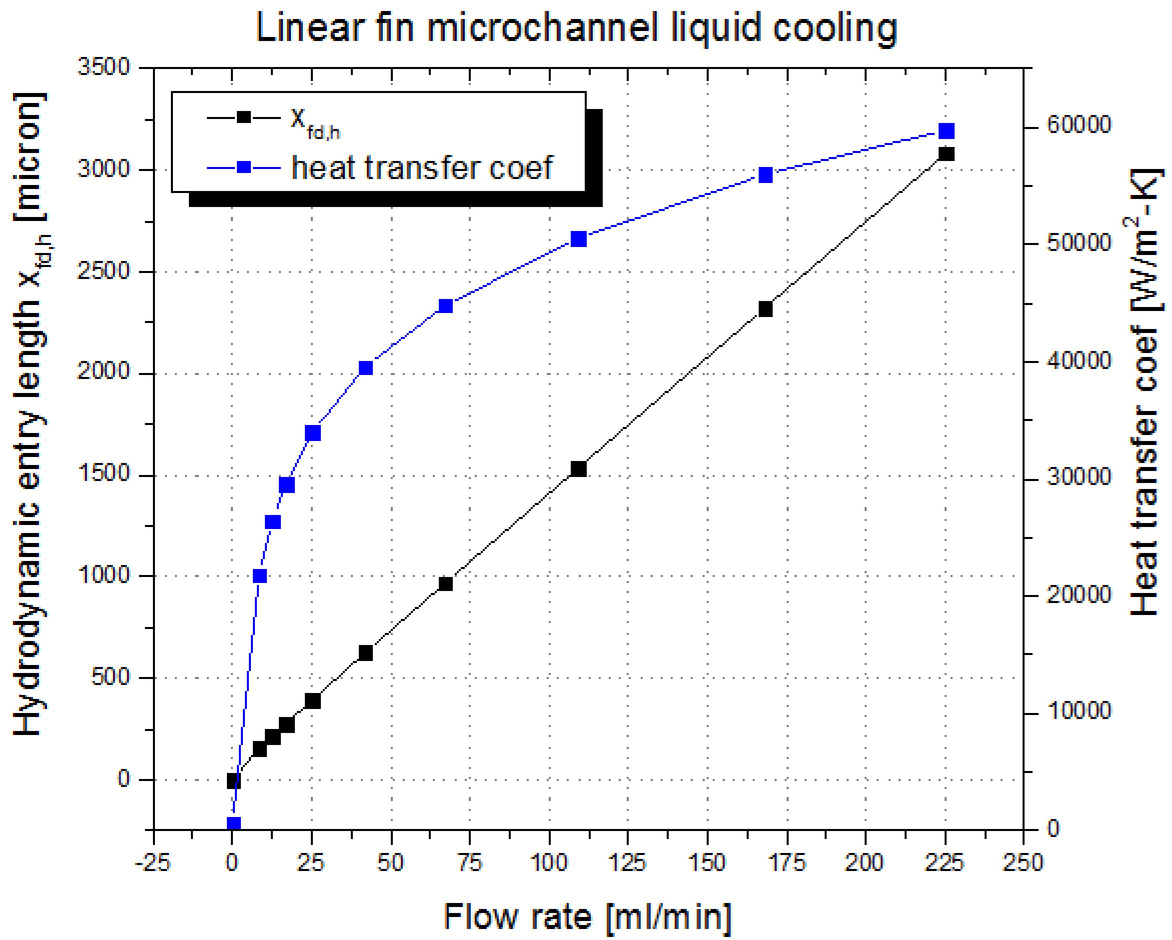

Figure 3.24 Hydrodynamic entry length and average heat transfer coefficient in linear microchannal as a function of water flow rate.

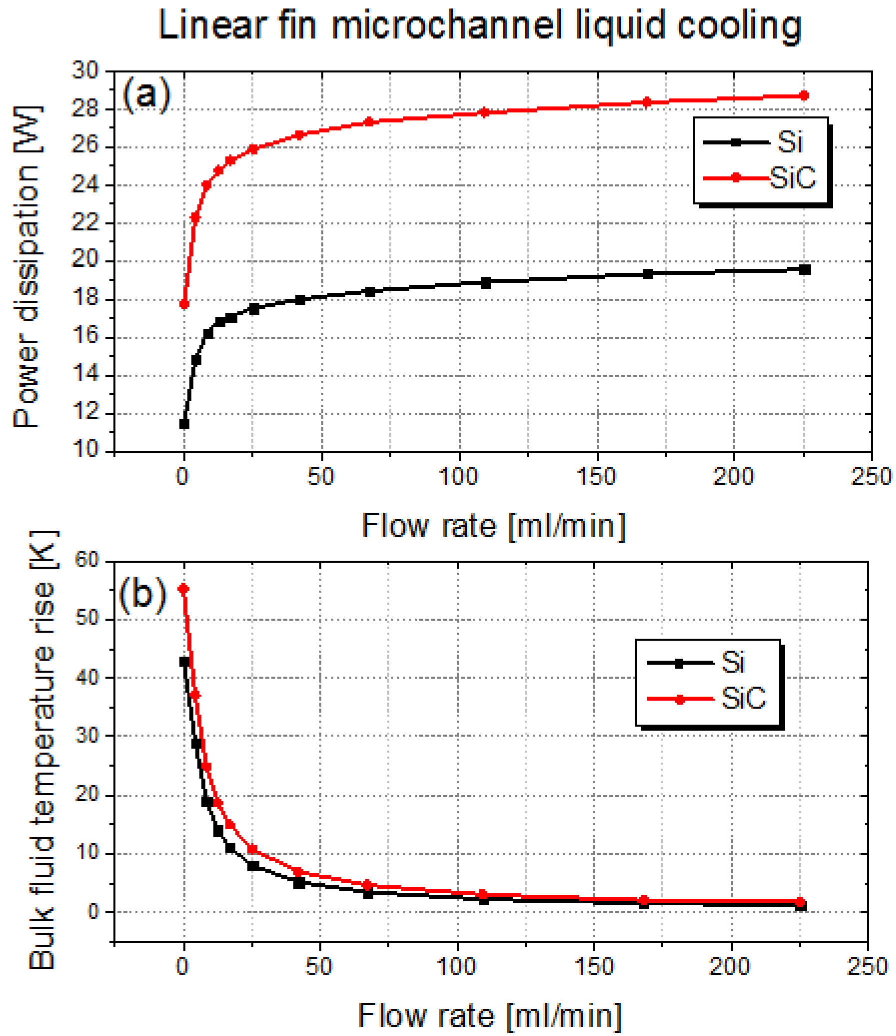

Figure 3.25 (a) Maximum power dissipation (for a maximum temperature of 200 °C) as a function of flow rate and (b) bulk fluid temperature rise as a function of flow rate with a corresponding power dissipation shown in (a) for GaN on Si and GaN on SiC with linear microchannels and 50 µm gate to gate spacing.

Thermal resistances for different substrate material and gate-to-gate (G2G) spacing were calculated with the following equation and is plotted in Figure 3.26:

$$R_{tot} = \frac{\Delta T}{P} = \frac{T_{max} - T_{ambient}}{P} \quad (3\text{-}14)$$

where T_{max} is the maximum device temperature, which occurs in the center of the inner-most finger as shown in Figure 3.27. P is the total power dissipation.

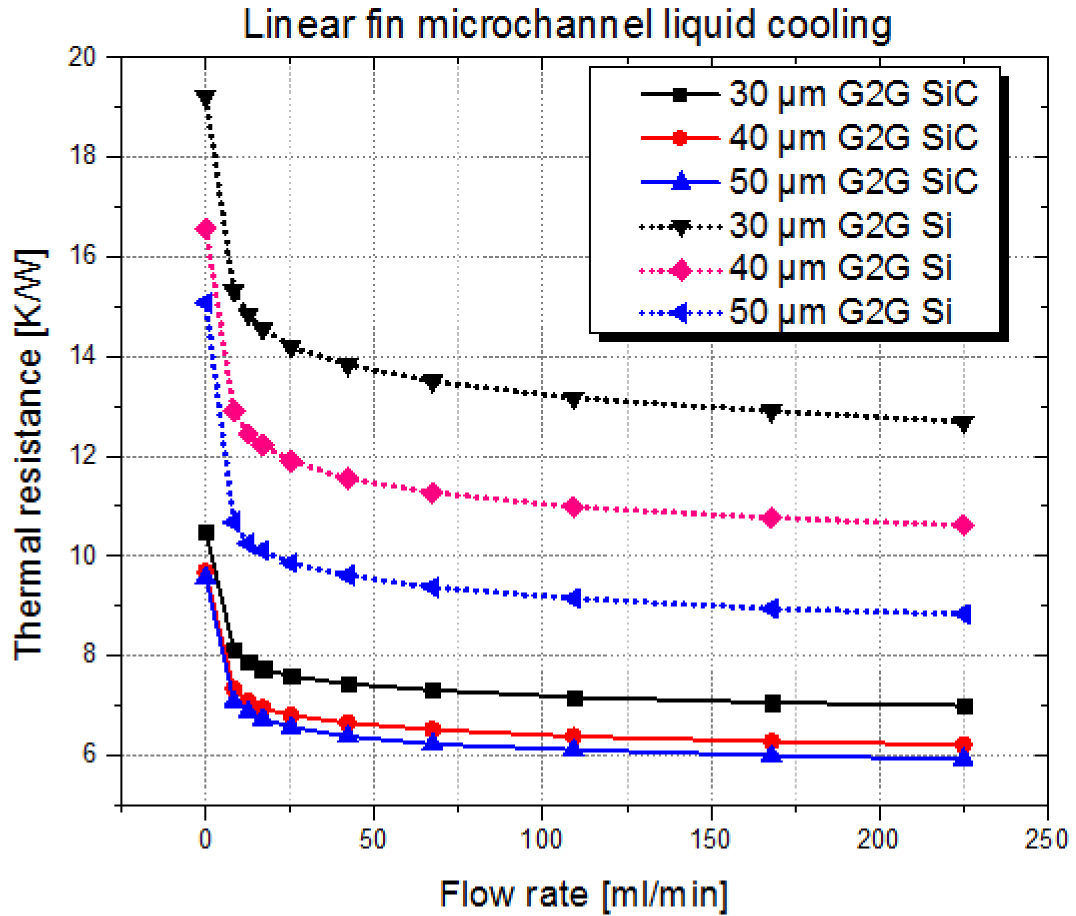

Figure 3.26 Thermal resistance for GaN on Si and GaN on SiC substrates with linear fin microchannel and different gate-to-gate spacing.

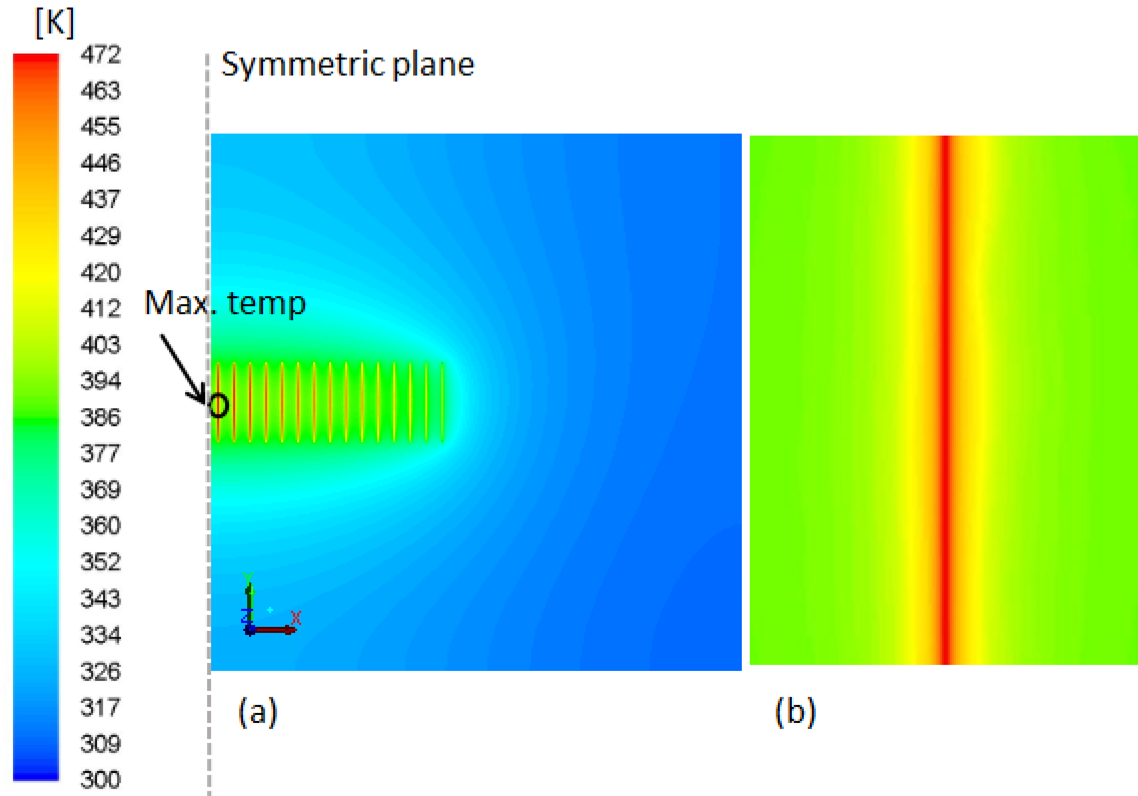

Figure 3.27 (a) is the top view of the temperature distribution on the GaN layer and (b) is the zoom-in view of the middle part of the inner-most finger (circled area in (a)).

Although microchannel liquid cooling was used, a certain amount of heat could still be transferred through the CuW package and dissipated through the copper cold plate. Therefore, not a hundred percent of heat is always taken away by the water in the microchannels, as shown in Figure 3.28. The lower the flow rate, the higher percentage of heat dissipates through the bottom Cu plate. If the water stops flowing, a hundred percentage of heat would have to dissipate through the bottom Cu plate. At an extremely low flow rate (in the case of microchannel clogging) of 0.0168 ml/min (1 mm/s in velocity), the device can handle 3.95 W/mm with SiC substrate and 2.55 W/mm with Si substrate with greater than 99.5% of the heat dissipated through the bottom Cu plate, as indicated in Figure 3.28. Under the same flow rate condition,

GaN on SiC had a higher percentage of its heat transfer through the Cu plate than GaN on Si. This can be due to the fact that the Si is more thermally resistive than the SiC. The percentage of heat dissipated by water is calculated as below:

$$\text{heat dissipated by water } (\%) = \frac{c_p \times \dot{m} \times (T_o - T_i)}{30 \times P \times 0.15} \times 100 \tag{3-15}$$

where c_p is heat capacity of water, $\dot{m}$ is mass flow rate, T_o is the mass-average water temperature at outlet, T_i is water temperature at inlet, which is 300 K, P is the power density in W/mm, 30 represents the number of fingers in total and 0.15 is the finger width in millimeter.

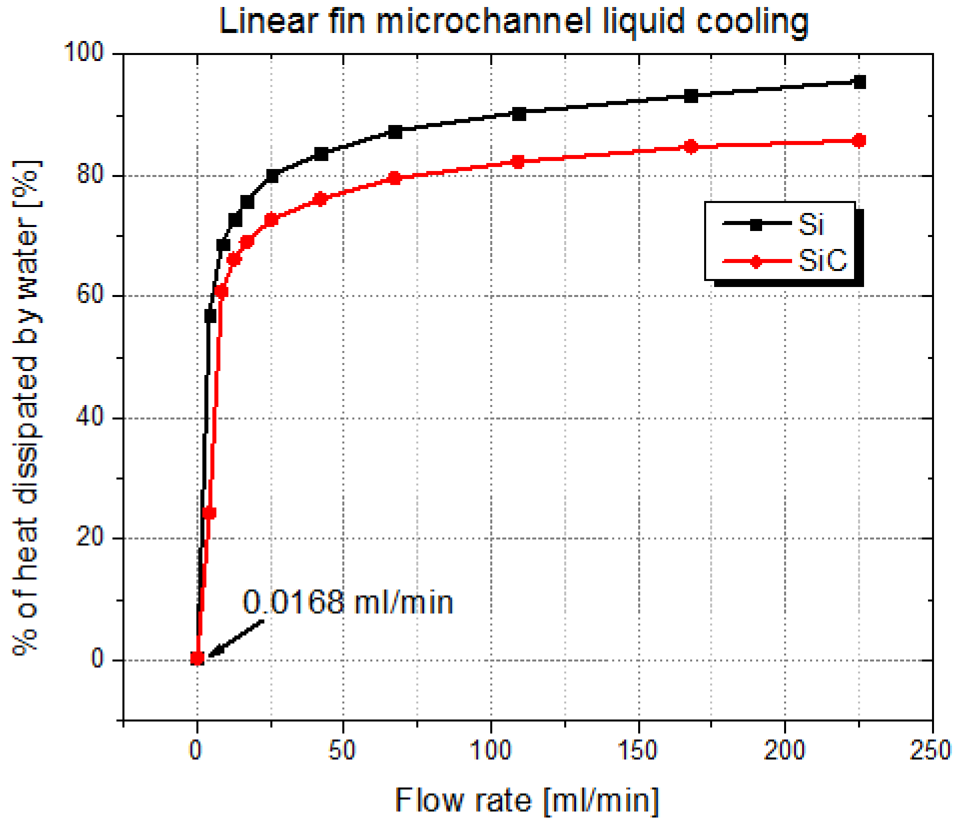

Figure 3.28 Percentage of heat dissipated by water vs. flow rate with uses of SiC and Si linear microchannels with 50 µm gate-to-gate spacing.

3.5.3.2 Pin Fin Microchannel Liquid Cooling

The maximum power densities for GaN-on-SiC and GaN-on-Si with pin fin microchannels are shown in Figure 3.29. All pin fin geometries are listed in Table 3.3 under the same pressure drop of 200 kPa and maximum junction temperature of 200 °C, pin fin 5 with diameter of 50 μm, longitudinal spacing of 50 μm and transverse spacing of 75 μm has the highest power density for both GaN-on-Si and GaN-on-SiC.

Figure 3.29 also shows the performance of linear fin microchannels labeled "LC" with 200 kPa pressure drop and a maximum 200 °C junction temperature conditions for comparison. Although the performance of linear microchannels are close to that of pin fin microchannel in terms of maximum power density, the volumetric flow rate for the pin fin microchannels was much less than that for the linear microchannels, as shown in Figure 3.30 (a). Since pumping power is related to the pressure drop and flow rate, the pumping power required for the pin fin microchannels is thus much less than that required by linear microchannels, as shown in Figure 3.30 (b).

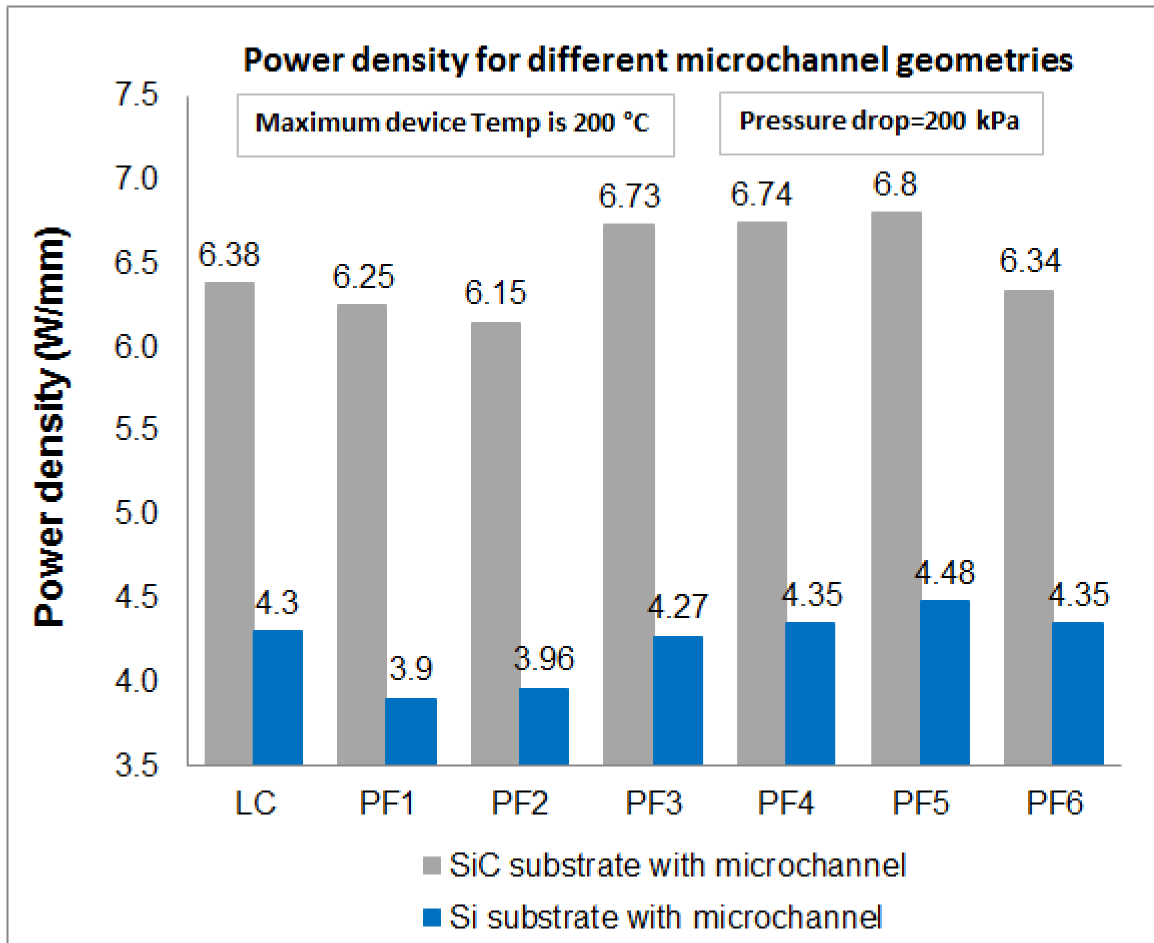

Figure 3.29 Comparison of power density between different microchannel designs under the 200 °C maximum temperature and 200 kPa pressure drop conditions. "LC" is linear channel. "PF" is pin fin channel. Pin fin 5 has the highest power density for both SiC and Si materials. 50 μm gate-to-gate spacing considered for all cases.

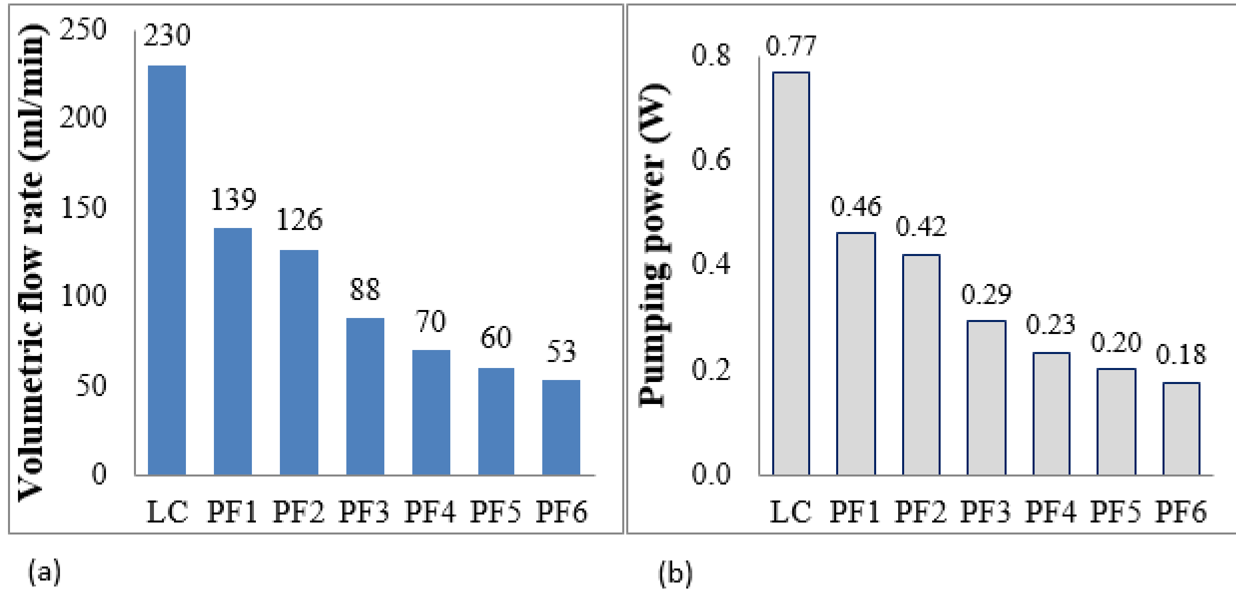

Figure 3.30 (a) Comparison of volumetric flow rate for different microchannel designs under the same 200 kPa pressure drop condition. (b) Comparison of pumping power for different microchannel designs under the same 200 kPa pressure drop condition.

With a thermal conductivity of more than twice of Si, SiC heat sink provides a power density of more than 50% higher than Si heat sink does in pin fin microchannel cooling. We are interested to see how much diamond heat sink can provide in terms of power density while maintaining a device peak temperature at or below 200 °C. Although not widely used, Diamond microchannel heat sink has been fabricated and investigated for its superior heat transfer capability for wide bandgap semiconductors [58].

The diamond pin fin microchannel has the same geometry as the Si/SiC pin fin microchannel (see PF5 in Table 3.3). GaN on 100 μm diamond substrate increases the power density from 5.6 W/mm in passive cooling to 9.6 W/mm in pin fin microchannel liquid cooling, while GaN on 200 μm diamond increases from 5.8 W/mm to 10.9 W/mm. It was found that in

GaN on 200 μm diamond, the thermal resistance from the 2 μm GaN layer and the thermal boundary resistance between the GaN and the diamond substrate contributed 70.2% of the total thermal resistance (compared to 30.5% for GaN on Si and 46.3% for GaN on SiC in active cooling) using the simplified 1D thermal resistance calculation as shown below:

$$R_{tot} = \frac{T_{\max_device} - T_{inlet}}{q} = 3.49\ K/W \tag{3-16}$$

$$R_{GaN+TBR} = \frac{T_{\max_device} - T_{\max_subs}}{q} = 2.45\ K/W \tag{3-17}$$

Where $T_{\max_device}$is the maximum temperature on top of GaN layer (it is also the maximum temperature of the heat flux areas). T_{inlet} is the fluid inlet temperature of 300 K. $T_{\max_subs}$ is the maximum temperature at the top surface of the substrate. q is the total power in watt.

Figure 3.31 shows a comparison of the maximum power density that can be dissipated by active and passive cooling approaches discussed so far. Any power density exceeding this maximum power density would cause a maximum device temperature greater than 200 °C resulting in serious device reliability issues. The data show that active microchannel cooling in Si substrates is nearly the same as passive cooling in SiC substrates in terms of power density. However, embedding pin fin microchannels in SiC substrates has a great impact, dramatically outperforming 200 μm thick passively cooled diamond substrates. These data show benefits of combining microchannel cooling with SiC to extend the performance past that of passive cooling with high thermal conductivity diamond substrates.

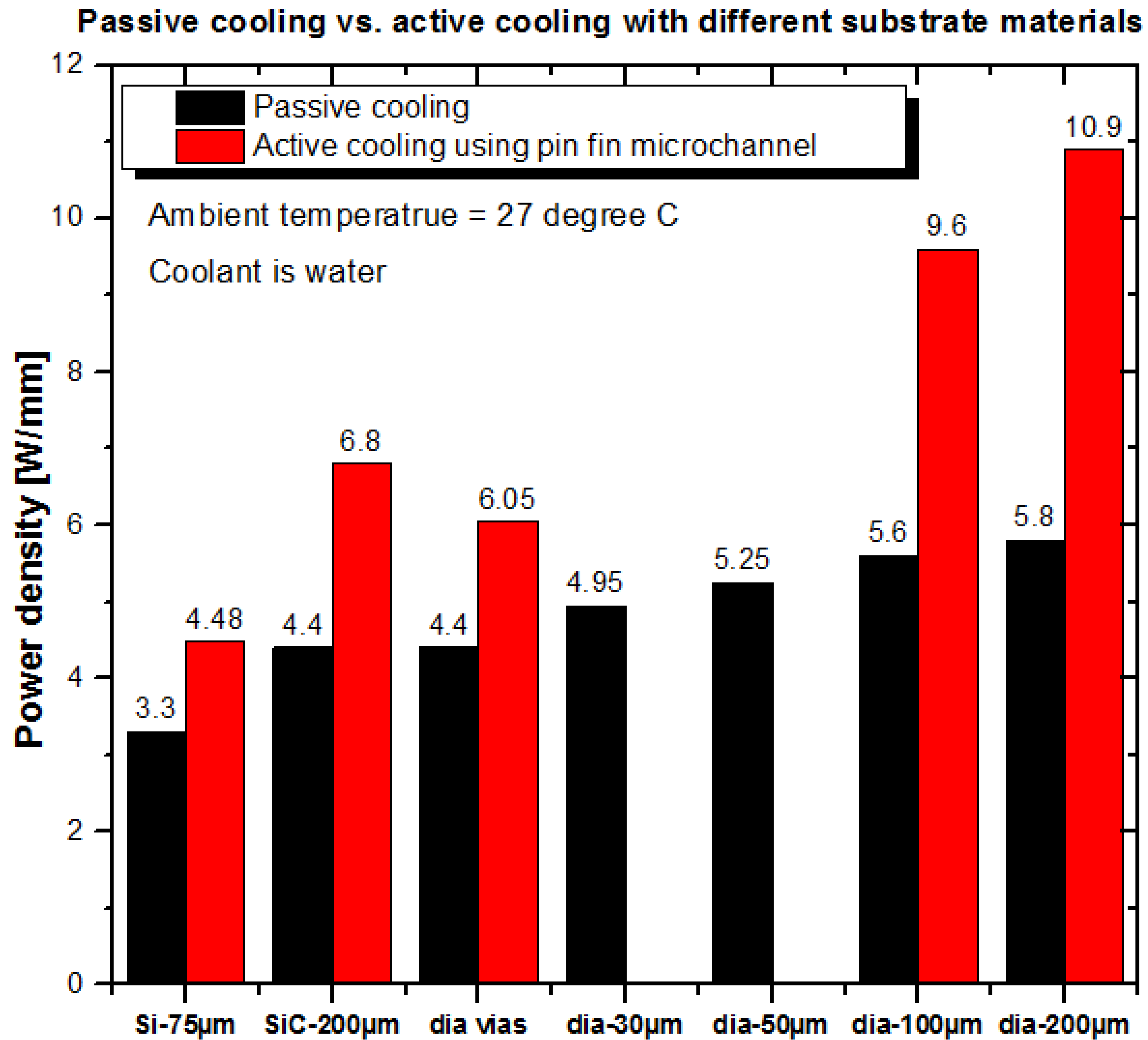

Figure 3.31 Comparison of power density between passive cooling and active cooling with microchannel. Diamond substrates with thicknesses of 30 µm, 50 µm, 100 µm and 200 µm are chosen for comparison. Pin fin 5 microchannel cooler is chosen to represent microchannel cooling. All cases are under the 200 °C maximum device temperature condition. Cases with microchannel coolings have 200 kPa pressure drop. 50 µm gate-to-gate spacing for all cases.

Based on the calculations above, we can conclude that the best single phase liquid cooling can allow 10.9 W/mm in power density (for a 30-finger device) with the constant heat

flux assumption. However, when HEMT devices operate in a pulsed condition, the maximum power density is expected to be higher because the heat flux would be zero when the device is at OFF state (more discussion in section 3.7). For GaN on 200 μm diamond, the power density almost doubles from passive cooling to active cooling. Analysis shows that in passive cooling, further increasing the thickness of diamond will not offer any significant increase in power density.

3.6 Simulation Results for Steady Heat Flux at Harsh Environments

Previous calculations were done based on a 300 K ambient temperature with the constraint of single phase flow. But the environmental condition may change significantly depending on the application of the HEMT devices. It can be tens of degrees below 0 Celsius or above 100 Celsius. Thus, water cannot be used as the coolant anymore under these harsh environmental conditions and new coolant fluid needs to be investigated. In this section, we will discuss how the harsh environment affect the choice of cooling fluids and explore whether active cooling using embedded microchannals remains most effective in reducing the junction temperature under different ambient temperatures.

Two common methods used in selecting the best heat transfer fluid are to calculate the Mouromtseff number and the Figure of Merit [81] [82]. The Mouromtseff number is a measurement of solely heat transfer performance while the Figure of Merit (FOM) is a measurement of both the heat transfer and required pumping power. Therefore, FOM $\propto \frac{c_p k}{\mu}$ for single phase laminar flow, where c_p is heat capacity, k is fluid thermal conductivity and μ is viscosity. [83] Based on Figure 3.32, liquid metal outperforms water, but its highly corrosive

property hinders its wide application. Salt based solutions like potassium formate/water and dynalene HC-30 have heat transfer properties that are as good as water and have reasonable pumping power requirements, but they are very corrosive and long term protection is not possible even with corrosive inhibitors. [84] Methanol/water and Ethanol/water are the next best candidates based on Figure 3.32, but they have low flash point (The lowest temperature at which it can vaporize to form an ignitable mixture in air). Methanol/water has a flash point of 29 °C and Ethylene Glycol/water has a flash point of 27 °C. [85] Thus Ethylene Glycol/water becomes the best candidate as it has effective freeze protection and relatively efficient heat transfer. It is non-corrosive if proper corrosive inhibitor is used, non-flammable, readily biodegradable and relatively low cost. [84] Ethylene Glycol/water (50% in weight) has a freezing point of -37 °C and a boiling point of about 107 °C. [86]

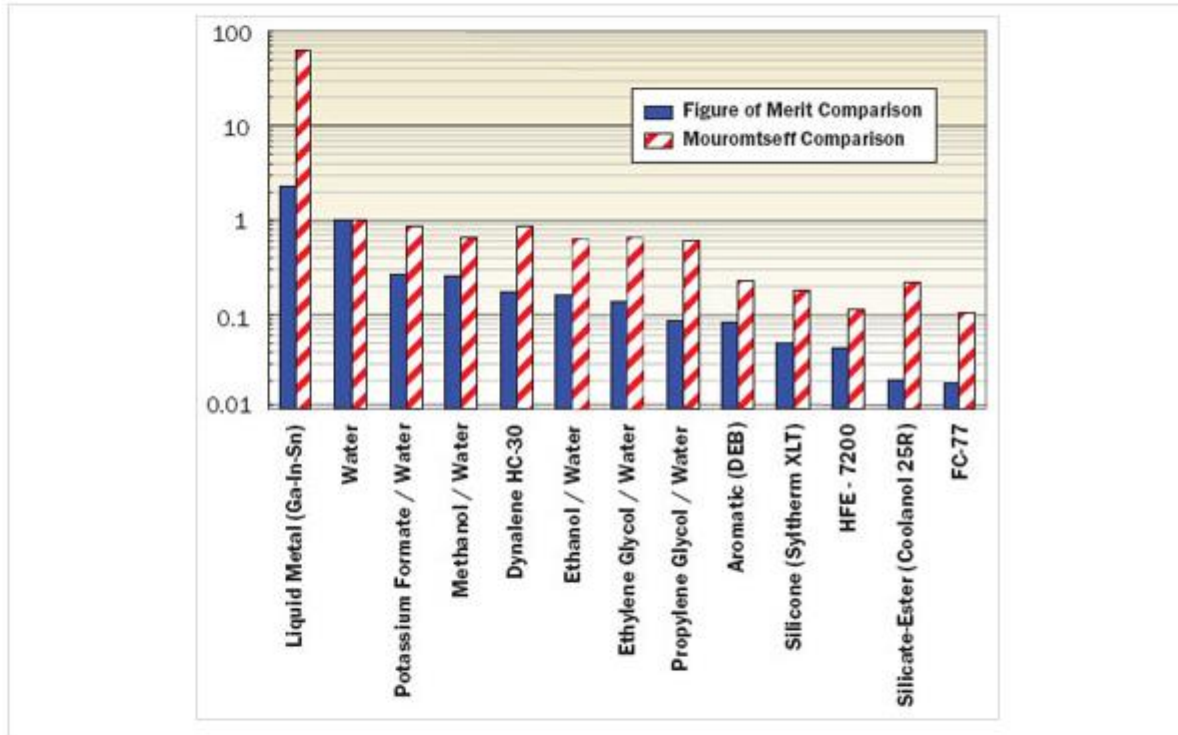

Figure 3.32 Comparison in thermal and hydraulic perspectives of different heat transfer fluids. Figure obtained from [83].

The viscosity of Ethylene Glycol (EG) solution is very temperature dependent. The relationship between viscosity and temperature from [86] was expressed as equations at specific temperature points, however, it was necessary to have equations that would be valid for certain temperature ranges as the temperature rise of the cooling fluid could be up to tens of degrees. Therefore, data points from this source were used to build relationships between temperature and viscosity at different temperature ranges, as shown in Appendix I. Except fluid inlet temperature and the fixed temperature at the bottom of the Cu plate, all other boundary conditions were the same as previously defined, as shown in Figure 3.8.

At ambient temperatures of -30 °C, 27 °C and 80 °C, active cooling with EG solution using pin fin microchannels for GaN on SiC has slightly better thermal performance (less than 10% in power density) than passive cooling using even 200 µm diamond substrate, as shown in Figure 3.33, Figure 3.34 and Figure 3.35. But active cooling using Si substrate offers less than passive cooling using SiC substrate. The advantages of using active cooling are less prominent at -30 °C than at 27 °C while comparing active cooling to passive cooling. At -30 °C ambient temperature, there was a 35% increase in power density for GaN on SiC and 12% increase for GaN on Si when changing from passive cooling to active cooling, compared to 41% increase for GaN on SiC and 21% increase for GaN on Si at 27 °C. This can be due to the fact that viscosity of EG solution significantly increases as temperature goes down. At a fixed pressure drop of 200 kPa, the increased viscosity results in less flow rate, and thus higher fluid temperature rise and worse heat transfer performance. For example, at 27 °C ambient temperature, the volumetric flow rate for GaN on SiC was 23.32 ml/min. This flow rate reduced to 7.58 ml/min at -30 °C ambient temperature.

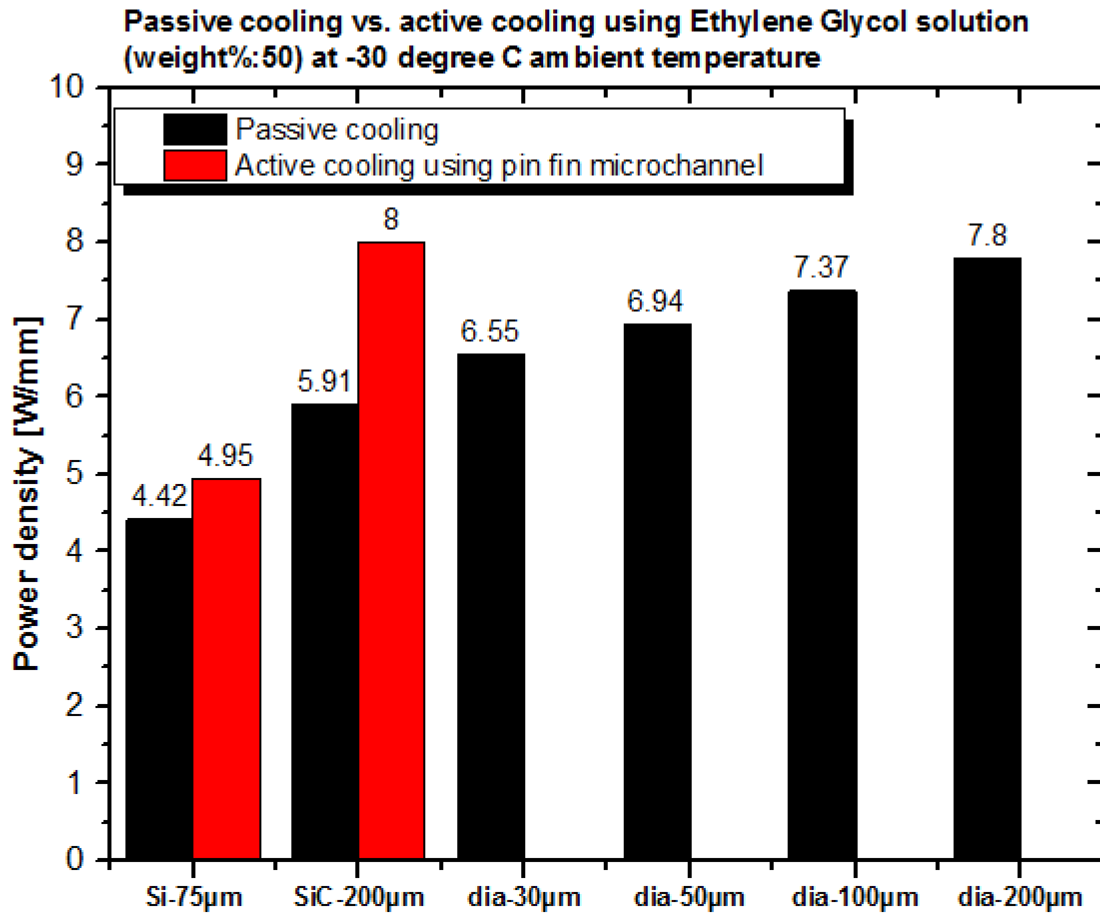

Figure 3.33 Comparison between passive cooling and active cooling at -30 °C ambient temperature. The pressure drop was 200 kPa for active liquid cooling. The maximum device temperature was 200 °C for all cases.

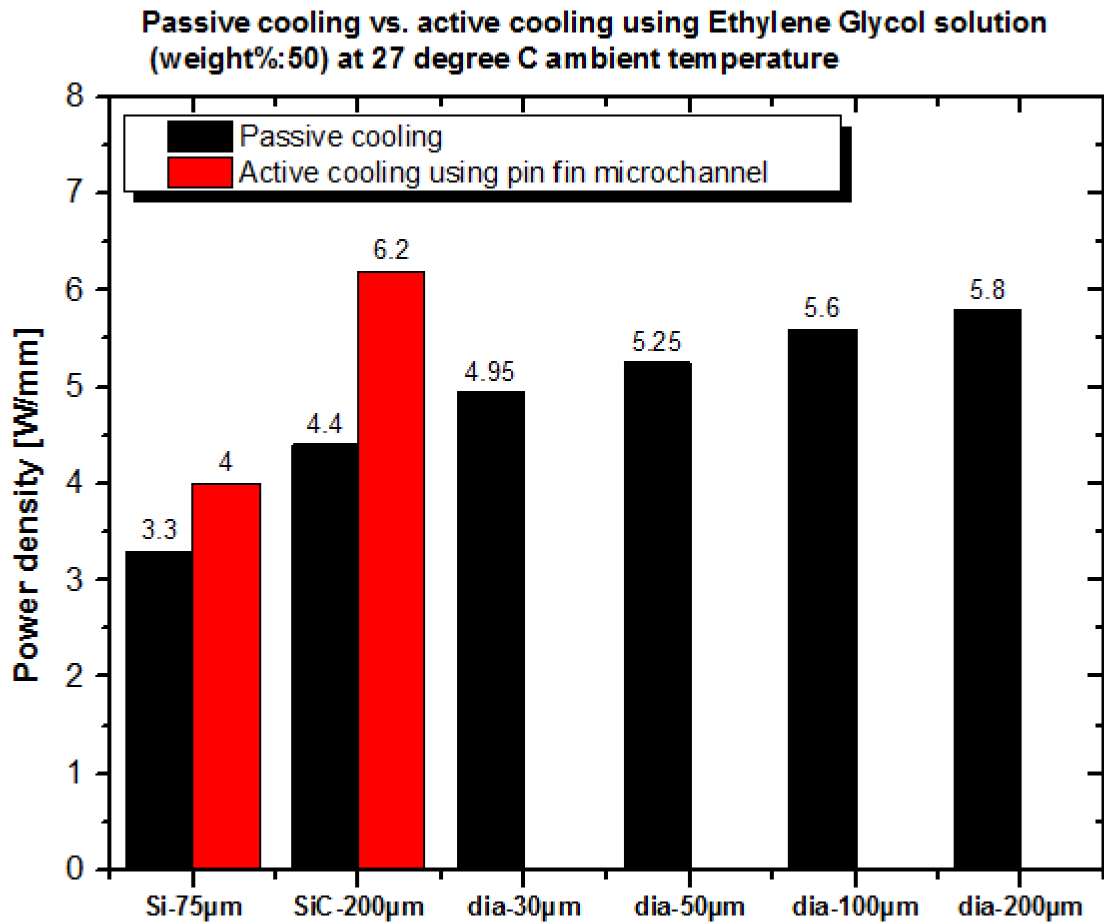

Figure 3.34 Comparison between passive cooling and active cooling at 27 °C ambient temperature. The pressure drop was 200 kPa for active liquid cooling. The maximum device temperature was 200 °C for all cases.

At 80 °C ambient temperature, although the viscosity of EG solution decreased and volumetric flow rate increased to 31.18 ml/min from 23.32 ml/min at 27 °C, the temperature rise of the cooling fluid limited the power density as we were only focus in simulating single phase cooling. At a power density of 1.6 W/mm for GaN on Si using active cooling, as shown in Figure 3.35, the maximum temperature of the cooling fluid was 105.23 °C, which was only about 2 °C below its boiling point. Therefore, the power density could not go higher although the maximum

device temperature was only 142.03 °C. However, GaN on SiC could handle much higher power density (166% higher than GaN on Si) while keeping the maximum temperature of cooling fluid below its boiling point. This could be due to the fact that the much higher thermal conductivity of SiC could help to spread out thermal energy resulting in a more uniform temperature in the cooling fluid. 23.34% of heat was dissipated through the bottom Cu plate in GaN on SiC while it was 16.97% in GaN on Si. At the power density of 4.25 W/mm, the maximum device temperature in GaN on SiC was 200 °C and the maximum temperature of the cooling fluid was 105 °C.

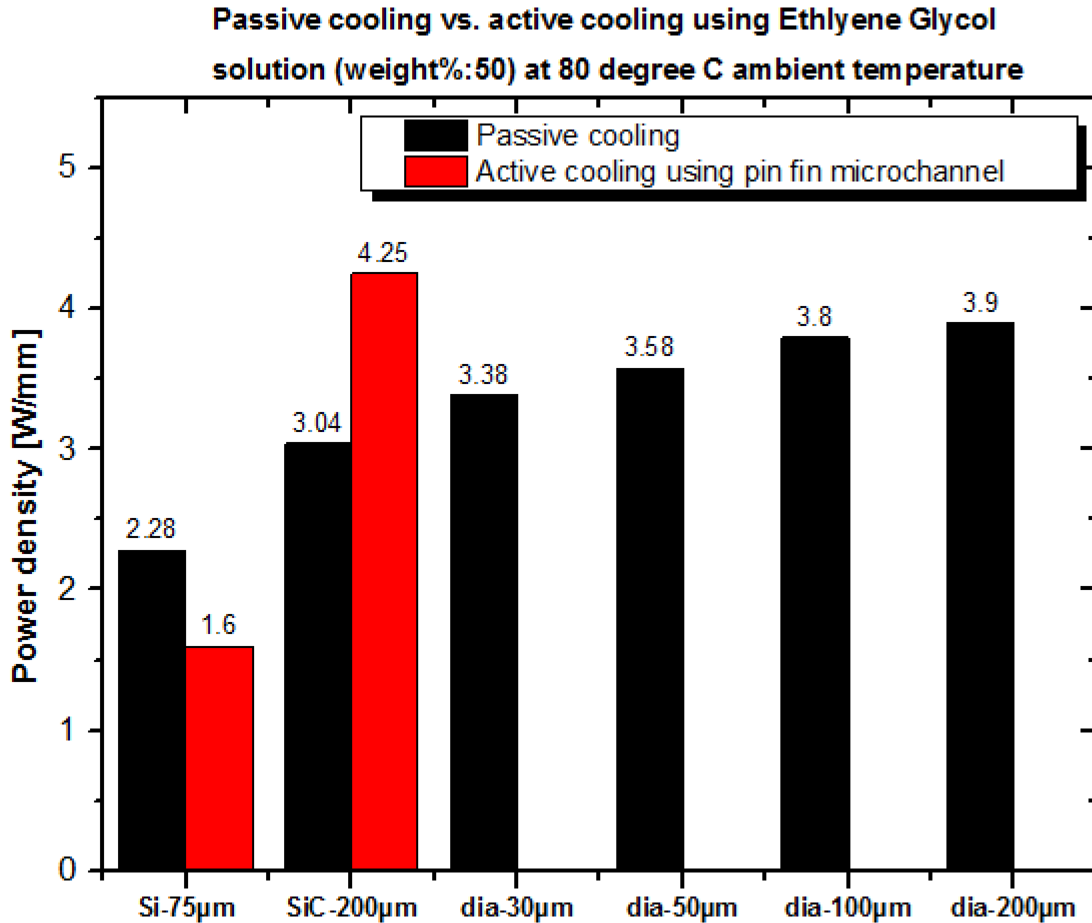

Figure 3.35 Comparison between passive cooling and active cooling at 80 °C ambient temperature. The pressure drop was 200 kPa for active liquid cooling. The maximum device temperature was 200 °C except GaN on Si with active cooling.

3.7 Simulation Results for Unsteady Heat Flux at Room Temperature

The previous results show the operation of GaN devices under DC operation, but they may also operate under RF or pulsed conditions. The time dependent heat source (heat flux in this study) is a square wave periodic waveform. In order to capture this phenomenon, a square wave function, as shown in Figure 3.36, was used in generating the time dependent heat flux in ANSYS Fluent. Although it was not possible to have infinite number of Fourier sine terms as an

input function in ANSYS, 50 Fourier sine terms were used and that was enough to generate a square wave-like function, as shown in Figure 3.36. The user input function of the heat flux in the simulation was written in C language as shown in Appendix I, along with temperature dependent thermal conductivities of other materials as well as temperature dependent viscosities of the coolants.

In this transient simulation, the model geometry and materials are identical to the static simulation as described in sections 3.2 to 3.4. Water at an inlet temperature of 300 K was used as the coolant. The heat flux started cycling as soon as water started flowing. 500 kHz was used as the pulsed frequency. Although this is not the radio frequency, the goal was to find out how much higher liquid cooling can achieve in terms of power density when the device is in pulsed condition. It was important to have enough time steps so that there were enough data points to construct the exact square wave. However, the more time steps each cycle would inevitably cause the calculations more computationally expensive. Therefore, there was a trade-off between accuracy and computational time. In this simulation, each cycle consisted of 20 time steps, which has been shown to be good enough to construct a square wave heat flux, as shown in Figure 3.37. With 20 times steps each cycle, spikes in each corner, as shown in Figure 3.36, could be avoided. The highest heat flux value in Figure 3.37 was 1.3402E10 W/m^2 while the desired/input value was 1.34E10 W/m^2. And the lowest heat flux value in Figure 3.37 was 0.025 W/m^2 while the desired/input value was 0. Therefore, 20 time steps per cycle was good enough to capture the desired highest and lowest heat flux values.

$$q_{square}(t) = \frac{4}{\pi}\sum_{k=1}^{\infty}\frac{\sin(2\pi(2k-1)ft)}{(2k-1)} \tag{3-18}$$

where q is heat flux, f is frequency in Hz and t is time in seconds.

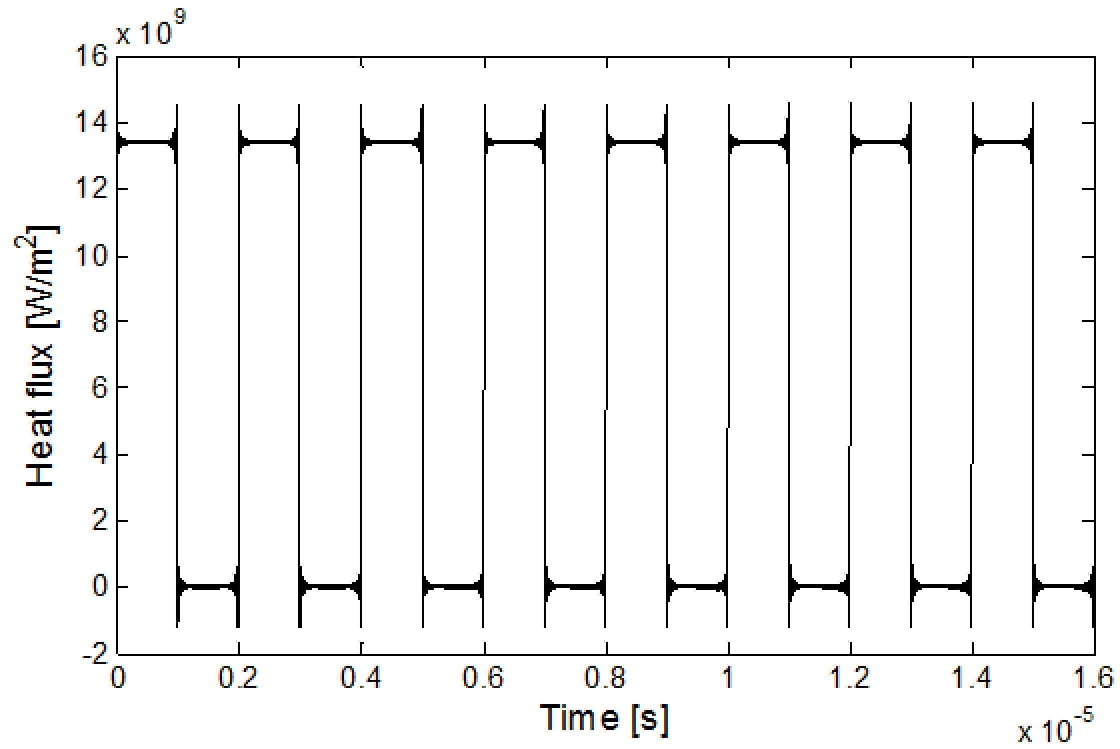

Figure 3.36 Square wave function with 50 terms and a frequency of 500 kHz. There were 200 time steps in a cycle. Figure generated in Matlab.

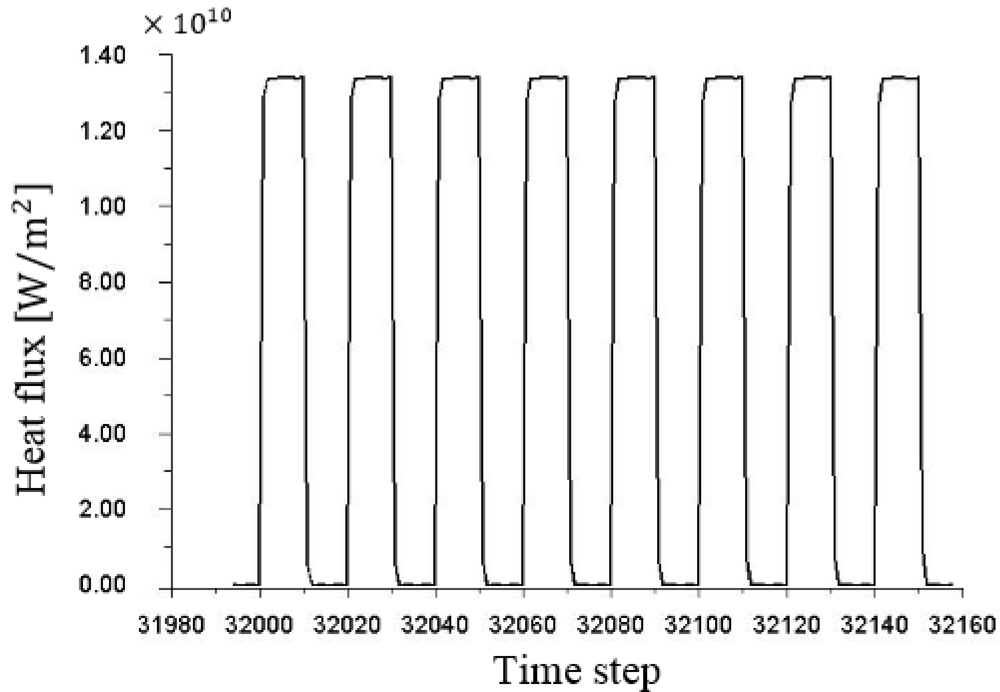

Figure 3.37 Square wave function of heat flux. Figure generated from ANSYS Fluent.

For GaN on Si with embedded pin fin microchannels, as flow time (from the time fluid started flowing, note that fluid started flowing as soon as heat flux started cycling) reached 0.0031838 s, the system reached quasi-steady state. The maximum power density was 6.7 W/mm and the maximum device temperature was around 465 K (or 192 °C) as shown in Figure 3.38. There is an about 50% increase in power density (4.48 W/mm for constant heat flux as shown in section 3.5) when the heat flux changes from constant to time dependent in a square wave manner and a frequency of 500 kHz. This simulation took approximately 5 days.

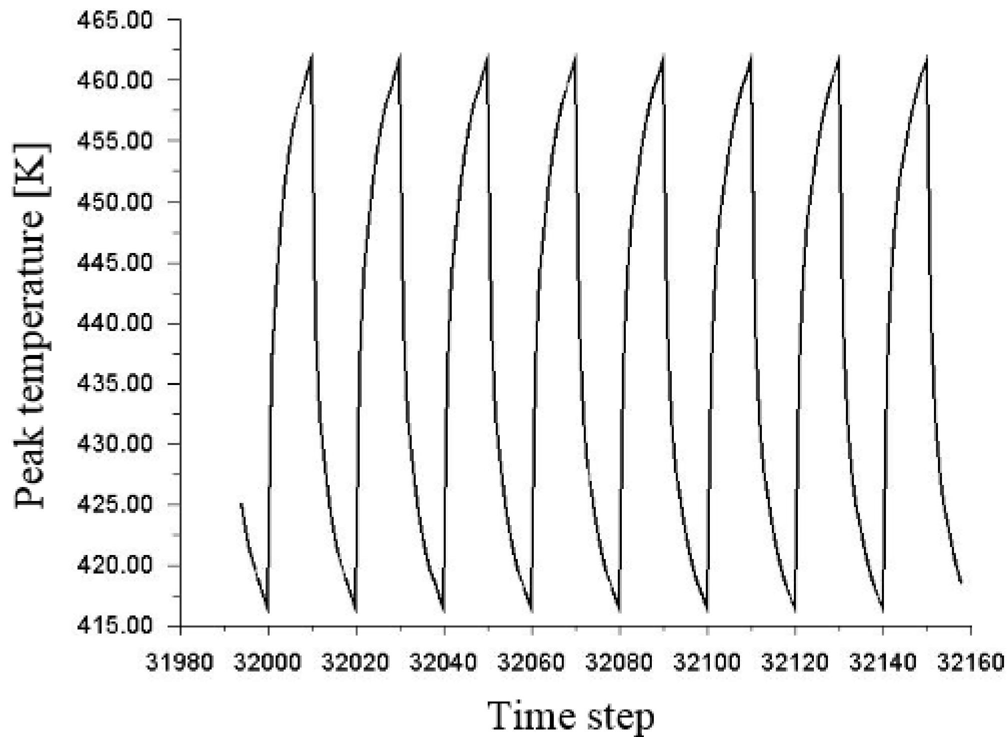

Figure 3.38 Quasi-steady state for GaN on Si with embedded pin fin microchannels under transit simulation. Power density at On-state was 6.7 W/mm.

For GaN on SiC with embedded pin fin microchannels, as flow time reached 0.0085 s, the system reached quasi-steady state. The maximum power density was 10.05 W/mm and the maximum device temperature was around 469 K (or 196 °C). There was a 48% increase in power density (6.8 W/mm for constant heat flux as shown in section 3.5) when the heat flux changes from constant to time dependent in a square wave manner with a frequency of 500 kHz. This simulation took approximately 7 days.

3.8 Conclusion

The use of active cooling through the incorporation of embedded microchannels in AlGaN/GaN HEMTs is an alternative to using passive cooling methods involving high thermal

conductivity substrates. It was found that the use of pin fin microchannel geometries provides additional benefits over that seen for linear microchannels, namely a reduction in the required pumping power for a similar maximum power density. While microchannels in SiC substrates show benefits when comparing devices to passively cooled diamond substrates, the reliability of such microchannel pumped systems will need to be proven. Thus, passive cooling methods may still be preferred in some cases where reliability is paramount. Also, the use of embedded microchannels in Si substrates show a similar performance as that seen in passively cooled SiC, but much less than diamond substrates. Thus, the biggest benefit seen through this study is the use of embedded channels in SiC. In comparing embedded channels in SiC and Si, devices on SiC can handle power densities that are 50% larger. Thus, single phase liquid cooling in these devices is attractive since it improves the power handling capabilities while leveraging the larger industrial base that has been developed in growing reliable AlGaN/GaN HEMTs on SiC substrates.

CHAPTER 4 Active Cooling of IGBT Modules

4.1 Introduction

The purpose of this chapter is to investigate the introduction of single phase microchannel cooling close to the junction of Insulated Gate Bipolar Transistor (IGBT) with single-sided and double-sided liquid cooling. Due to the vertical geometry of the device, the liquid cooling is placed in the bottom side of the Direct Bonded Copper (DBC) power electronics substrate. The goal is to find out what is the maximum power dissipation a single chip can have while maintaining the maximum chip temperature to be less than 85 °C under different cooling methods. Power dissipation, pressure drop, required pumping power and thermal resistance of each cooling method are analyzed and compared. A wire-bonded IGBT chip on DBC substrate in conventional cooling will serve as a baseline and is shown in Figure 4.1.

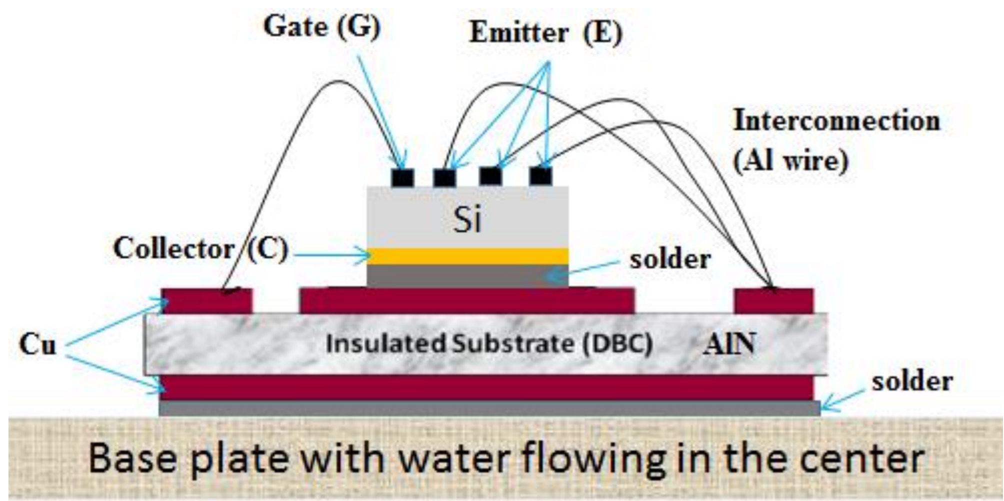

Figure 4.1 Front view of an IGBT chip on DBC substrate with conventional cooling (a baseline).

4.2 System Layout and Modeling Definition

3-D thermal-fluid modeling was performed for the whole packaged IGBT system using ANSYS Fluent. Water was used as the coolant fluid with an inlet temperature of 300 K. The chip is made of silicon and is 100 μm thick with a 1 cm by 1 cm cross section. Direct Bonded Copper (DBC) was used as the device substrate for electric connection and mechanical support. The DBC substrate is 2 cm by 2 cm and consists of two 300 μm Cu layers and a 500 μm AlN layer in between the Cu layers. The following assumptions were made in all simulations:

1) Fluid remained single phase and flow remained laminar.

2) The system operates in steady state.

3) Water had constant properties except viscosity. The temperature dependent viscosity is expressed in the following equation [54]:

$$\mu = 2.414 \times 10^{-5} \times 10^{\left(\frac{247.8}{T-140}\right)} \quad (4\text{-}1)$$

4) Radiation and natural convection were ignored.

5) Uniform heat generation within the chip.

6) Emitter and gate contact pads cover 70% of the chip’s top surface (for double-sided cooling).

7) The emitter, base and collector contact pads do not affect thermal transport as they are less than 100 nm thick.

8) No heat exchange at the bottom of the microchannel cold plate.

9) Except thermal conductivity of Si and viscosity of the coolant fluid, all other materials had constant properties, as shown in Table 4.1 and Table 4.2.

Table 4.1 Properties of all solid materials used in simulations [71][65].

Material	Thickness [μm]	Thermal Conductivity [W/m-K]
Si	100	$148 \times [\frac{T}{300}]^{-1.4}$
AuSn/Solder	50	57
AlN	500	170
Cu	300	387

Table 4.2 Fluid properties used in simulations [54].

Fluid	Density [kg/m^3]	Specific heat [J/kg-K]	Thermal conductivity [W/m-K]	Viscosity [kg/m-K]
Water	998.2	4182	0.6	$2.414 \times 10^{-5} \times 10^{\left(\frac{247.8}{T-140}\right)}$

4.2.1 Single Sided Cooling

In single sided cooling, the silicon chip is attached to the DBC heat sink using 50 μm thick AuSn solder. With the assumption that contact pads do not affect thermal transfer, the collector layer was not included in the model, as shown in Figure 4.2. The top side of the Si chip and the bottom side of the microchannel cover were assumed to be in an adiabatic condition, as discussed in [64]. In order to shorten the distance between the heat source and the cold plate, fin geometries are made into the Cu layer of the DBC substrate to allow coolant fluids flow through. Both linear fins and pin fins, as shown in Figure 4.3, were analyzed. The linear fin microchannel cold plate features 26 fins with a length of 1 cm, a height of 250 μm and width of 200 μm. Each channel width is also 200 μm. According to [52], equating the channel width to the wall (fin)

width can minimize the convective thermal resistance. Although further reducing the aspect ratio of the fins can lead to smaller convective thermal resistance, it increases complexity in making a low-cost microchannel embedded cold plate. 200 μm was chosen here as the fin width as it has been shown that this size of linear fins can be made by directly machining into the bottom Cu layer of the substrate via laser ablation which has been done in GE [87]. This is a much cheaper and efficient process than doing the microfabrication in a clean room.

Three different pin fin microchannel cold plates with different pin fin spacings were evaluated. These pin fins also have a height of 250 μm. Since there is uniform heat generation in the chip, the highest temperatures of the chip and the coolant fluid would be in the fluid outlet side due to heating of the fluid as it absorbs energy passing through the heat exchanger. Therefore, it is important to minimize the temperature rise of the coolant fluid at the outlet by increasing its mass flow rate. At a fixed pressure drop, the "denser" the pin fin arrays, especially in the stream-wise direction, the smaller the fluid flow rate would be. However, the higher the number of pin fins, the greater the convection area and thus the smaller the convective thermal resistance. Therefore, there is a tradeoff between minimizing the thermal resistance due to heating of coolant fluid and minimizing the thermal resistance due to convection under a certain pressure drop.

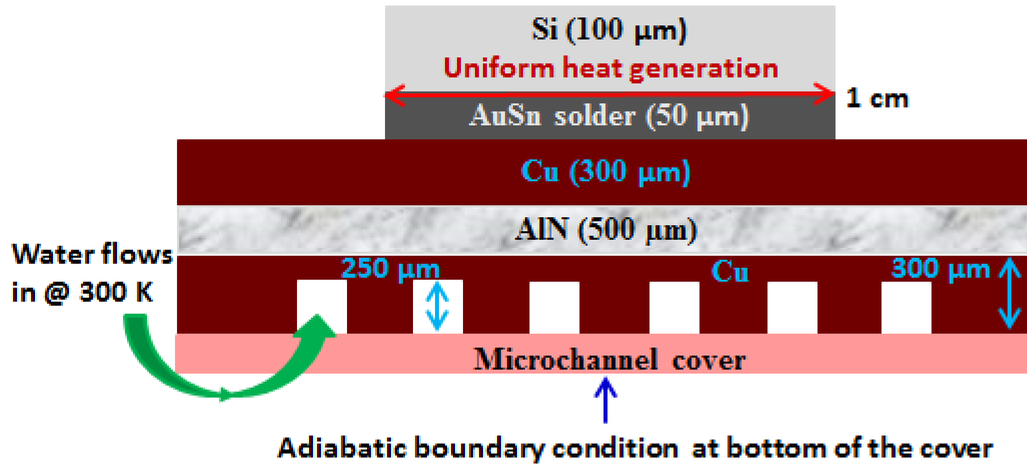

Figure 4.2 Side view of a modeling structure for an IGBT with single sided cooling.

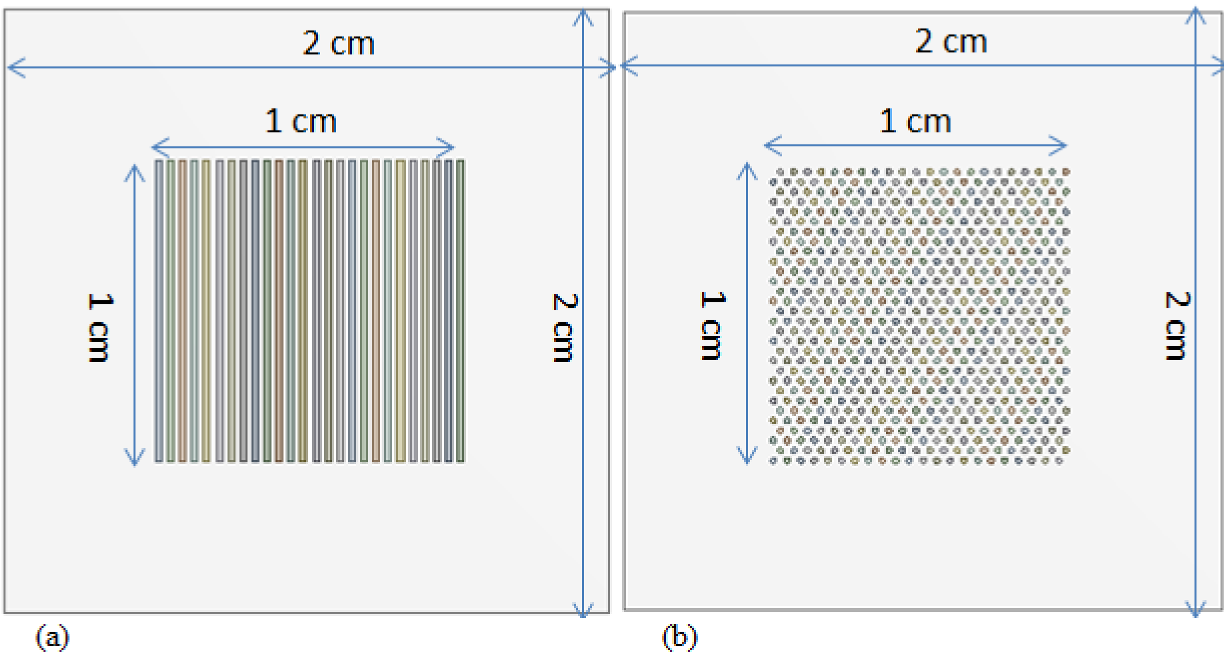

Figure 4.3 Top view of embedded microchannels in a Cu substrate layer in DBC with (a) linear fins and (b) pin fins.

4.2.2 Double Sided Cooling

In single sided cooling, there is negligible heat dissipation via natural air cooling at the top of the Si chip so that almost all the heat has to go to the bottom DBC heat sink. However, the cooling performance can be improved if we can extend the cooling area by adding another DBC heat sink on top of the chip, given that 70% (Based on data provided by Oak Ridge National Lab) of the chip's top surface is covered by the emitter and base metal contact pads. Based on this reason, double sided cooling is proposed as shown in Figure 4.4. The geometries of each DBC heat sink are identical to those used in single sided cooling. The top AuSn solder covers 70% of the chip's top surface. Only pin fin microchannels are studied.

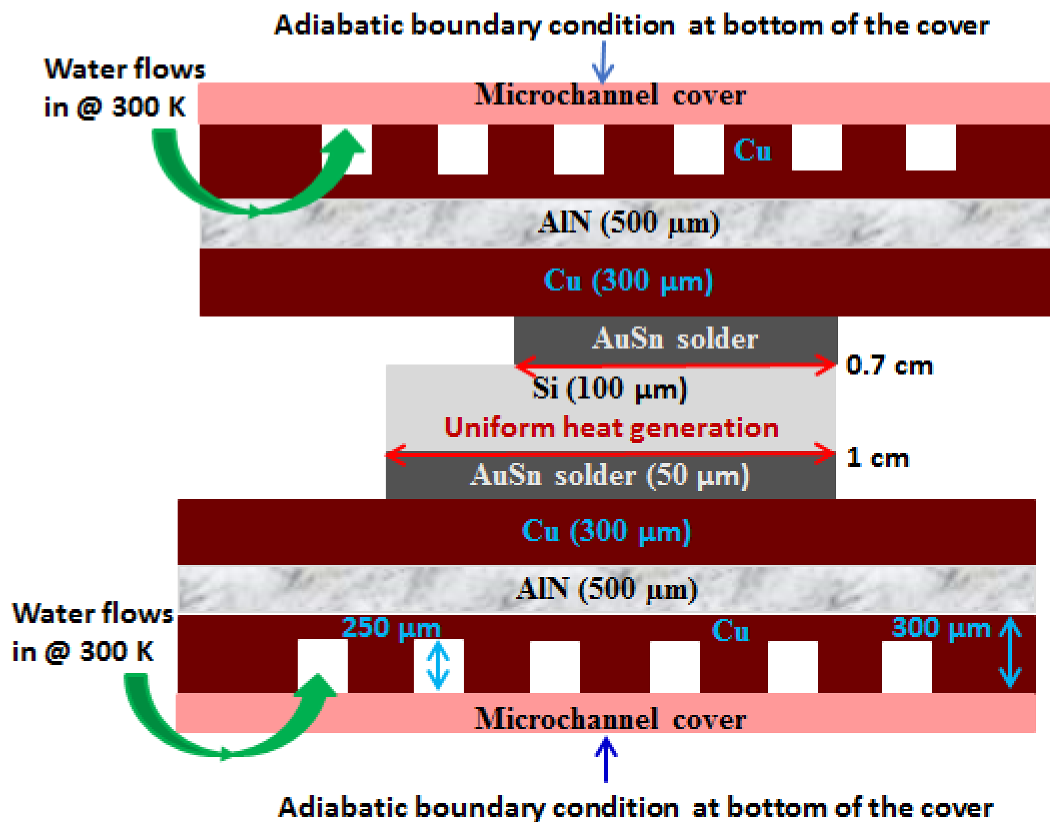

Figure 4.4 Side view of a modeling structure for an IGBT with double sided cooling.

4.3 Simulation Results

For every simulation, energy balance was checked and less than 1% error was found for every cases based on equation (13).

$$q = \dot{m}c_p\Delta T \tag{4-2}$$

where $\dot{m}$ is mass flow rate, c_p is heat capacity of water and ΔT is the temperature difference between inlet temperature and mass-averaged outlet temperature of water.

4.3.1 Comparing Different Staggered Pin Fin Spacings

Pin fins microchannels with different longitudinal (S_L) and transverse (S_T) spacings as listed in Table 4.3 show different cooling performances. A pin fin diameter (D) of 200 μm was used in all cases. The smaller the S_L and S_T, the "denser" the fin arrangement was and the higher the number of pin fins in each cold plate. Prototype 1 had the most pin fins and thus the greatest convection area while Prototype 3 has the fewest fin fins and smallest convection area. All cases were under the same power and pressure drop. Prototype 1 has a much higher chip temperature than the other two. It also has the highest maximum coolant fluid temperature, or maximum fluid temperature rise. The maximum fluid temperature at the outlet led to the high maximum chip temperature at the outlet side. This high maximum fluid temperature is due to its low mass flow rate (Prototype 1 has the least mass flow rate as shown in Table 4.3). Under the same pressure drop, less fluid can flow through a microchannel with higher number of pin fins due to impingement of fluid on the fins. Prototype 3 has a slightly higher maximum chip temperature than prototype 2, which could be due to an increase in convention thermal resistance since it has

a lower contact area with fewer pin fins, although it has a higher mass flow rate and lower maximum fluid temperature than Prototype 2.

Although the mass flow rate in Prototype 2 was only 5% less than that in Prototype 1, the actual water passed through the pin fins in Prototype 2 could be much more than 5% than that in Prototype 1. This is because the majority of the water bypassed the pin fin area.

Table 4.3 Comparison in heat transfer performance of different staggered pin fin spacings in a microchannels cold plate. Coolant fluid was 300 K at inlet for all cases.

	D (μm)	S_L (μm)	S_T (μm)	# of pin fins	Power (W)	ΔP (kPa)	$\dot{m}$ (g/s)	Max. fluid temp (K)	Max. chip temp (K)
Prototype 1	200	250	400	1000	370	200	37.54	349.41	380.96
Prototype 2	200	333	454	660	370	200	39.47	338.68	354.40
Prototype 3	200	400	500	520	370	200	40.60	335.48	356.08

Based on simulation results from Table 4.3, Prototype 2 was chosen for the rest of simulations.

4.3.2 Comparing Double Sided Cooling With Single Sided Cooling

For single sided cooling, the use of pin fins leads to significant higher cooling capability than the use of linear fins at a pressure drop equal to or greater than 50 kPa (26% higher in terms of power dissipation at 50 kPa pressure drop), as shown in Figure 4.5. Also, the use of double sided cooling using pin fins can increase the power by at least 36.5% from singled sided cooling. This increase gets higher at a lower pressure drop, for instance, 68% increase at a pressure drop of 5 kPa. All three trends in Figure 4.5 get flatter as pressure drop increases, indicating a lower coefficient of performance (COP) at a higher pressure drop. The advantages of using pin fins can also be seen in Figure 4.6, where a microchannel cold plate with pin fins was more sensitive to

increase in flow rate than that with linear fins. This could be due to the fact that fluid temperature rise in linear fin microchannel got less sensitive to flow rate as flow rate increased, as discussed in chapter 3.

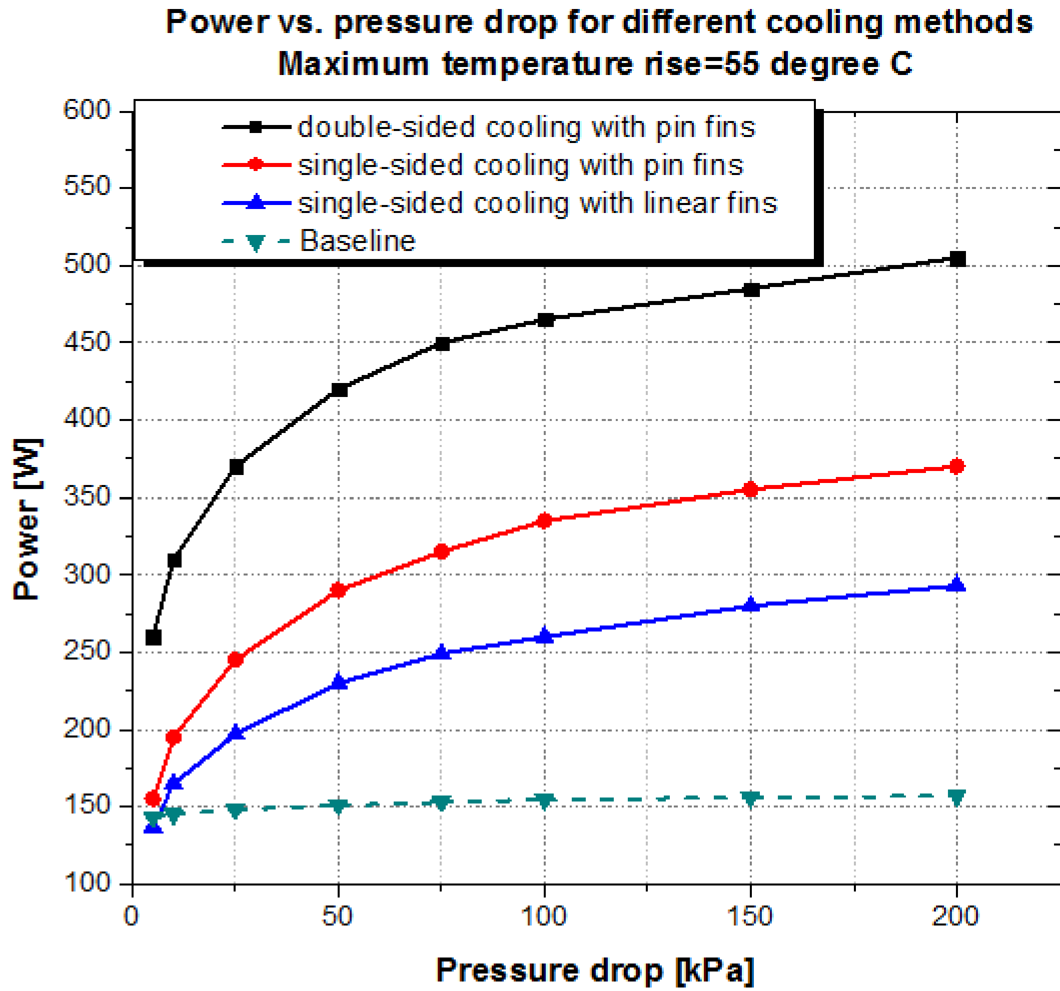

Figure 4.5 Power dissipation in a chip verses pressure drop in microchannel for different cooling methods. The maximum temperature rise in the chip is 55 °C for all cases. Baseline is the convetional cooling method with a structure shown in Figure 4.1.

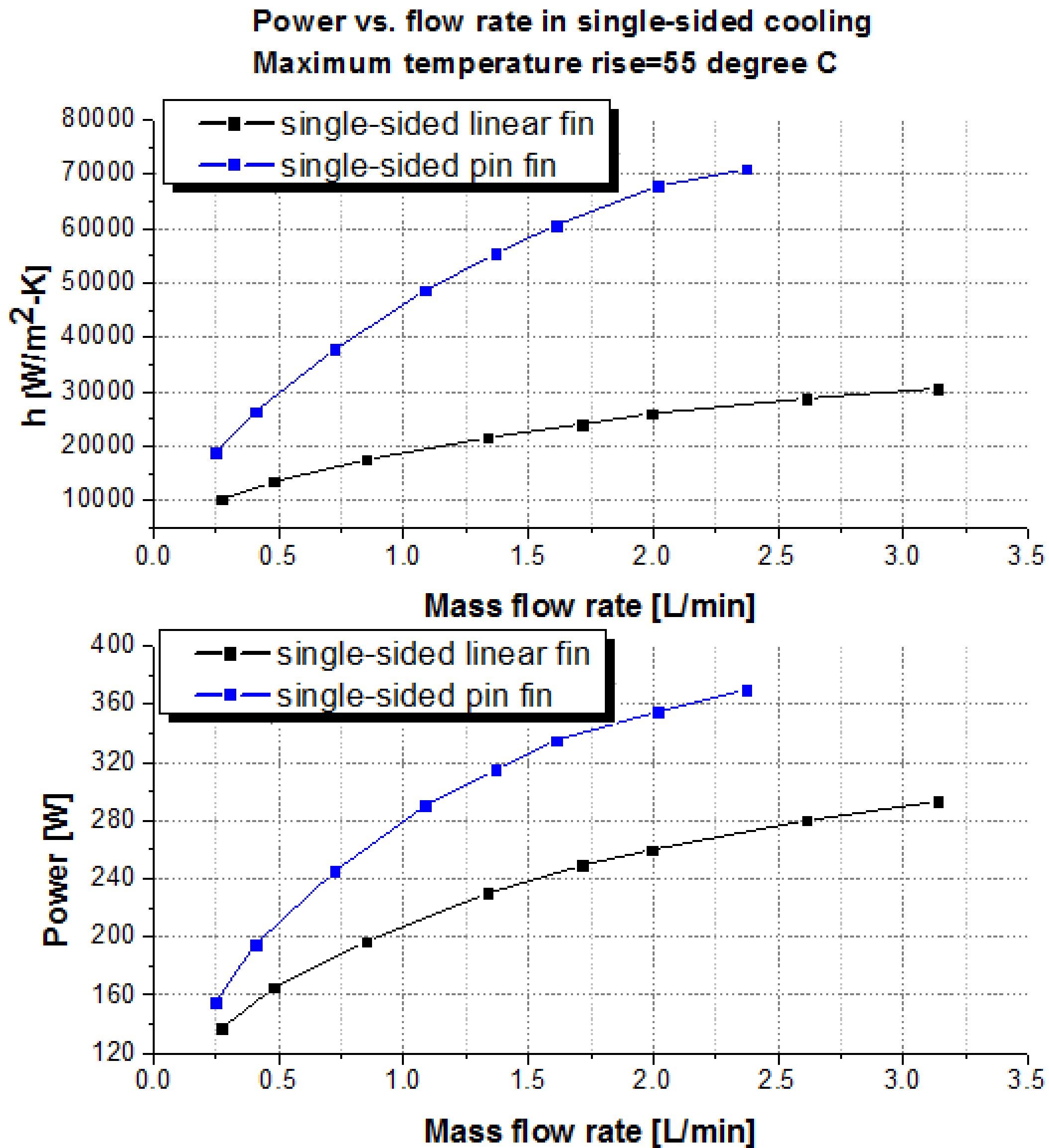

Figure 4.6 Power dissipation and average heat transfer coefficient in a chip verses fluid flow rate in microchannel for single sided cooling with linear fins and pin fins. The maximum temperature rise in the chip is 55 °C for all cases.

The thermal resistances for single sided cooling were calculated as the temperature difference between the average temperature at the top surface of the Si chip and the average temperature of the coolant fluid divided by the power dissipation. In double sided cooling, the

average temperature of the chip was used in calculating the overall thermal resistance. The relationships between thermal resistance and pressure drop over a microchannel cold plate for all cooling methods are shown in Figure 4.7. Thermal resistance decreases significantly as pressure drop increases while the pressure drop is less than 50 kPa. But once pressure drop reaches 100 kPa, further increasing the pressure drop only results in a very small decrease in thermal resistance (7.3%, 7.5% and 9.0% decreases in thermal resistance while increasing pressure drop from 100 kPa to 200 kPa for single sided cooling with linear fins, single sided cooling with pin fins and double sided cooling with pin fins).

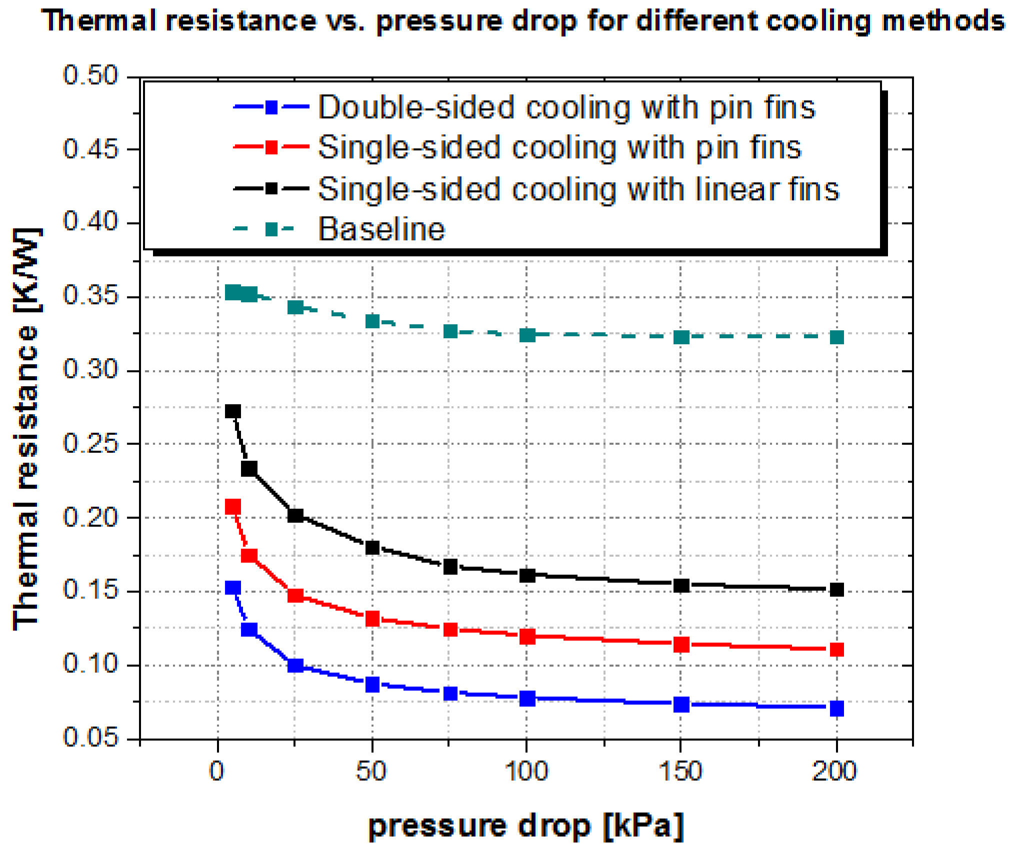

Figure 4.7 Overall thermal resistance verses pressure drop in microchannel for different cooling methods.

In single sided cooling, since the coolant fluid temperature increases from inlet to outlet, the highest chip temperature is near the outlet, as shown in Figure 4.8 and Figure 4.9. But for double sided cooling, the highest temperature of the chip was in the 30% of the chip portion where no AuSn solder contact was on top, as shown in Figure 4.10. In this region, the heat could only dissipate through the bottom DBC, while in the other region (the 70% region) heat could dissipate through both top and bottom DBCs. Since the coolant fluid flows in the top and bottom microchannel cold plates are in opposite direction, there is no significant difference in temperature between inlet and outlet sides of the chip, as shown in Figure 4.11.

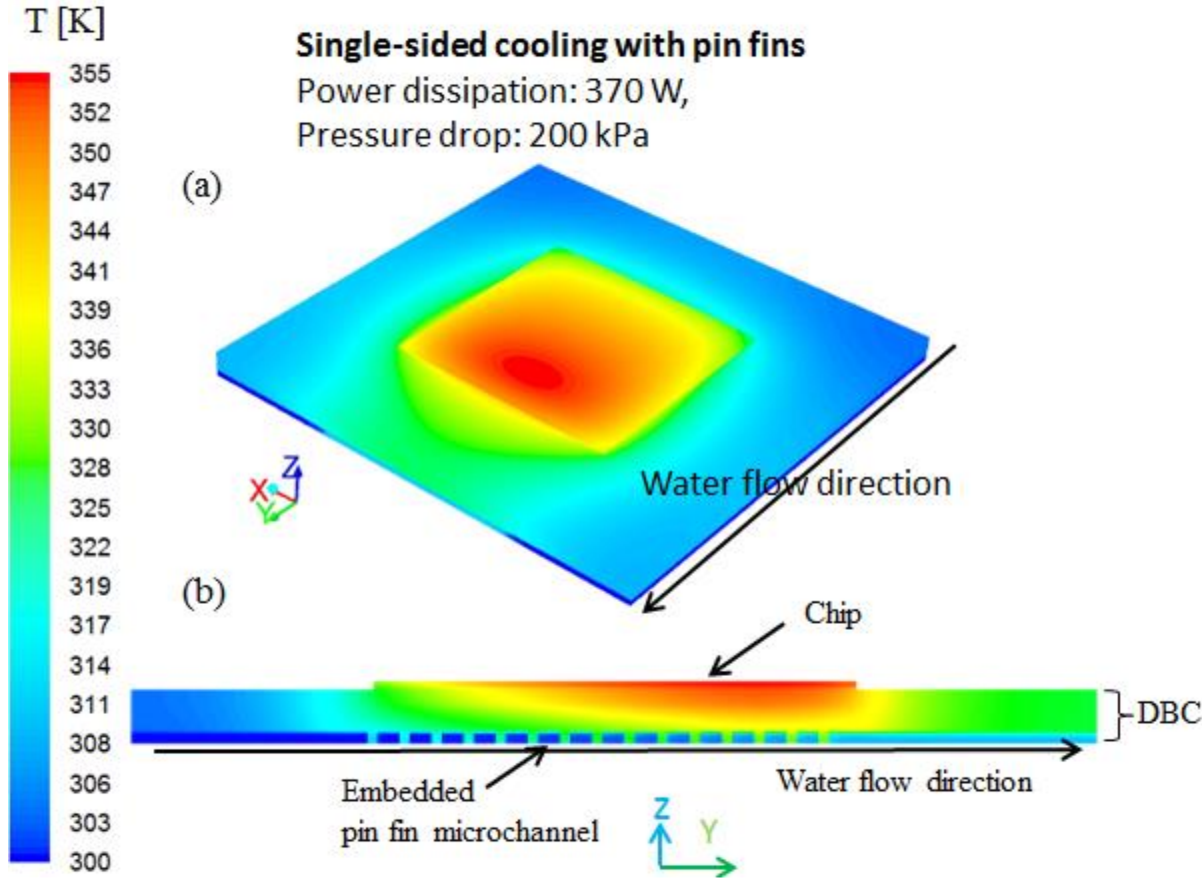

Figure 4.8 (a) Isometric view and (b) side view of temperature distribution in a single-side cooled IGBT.

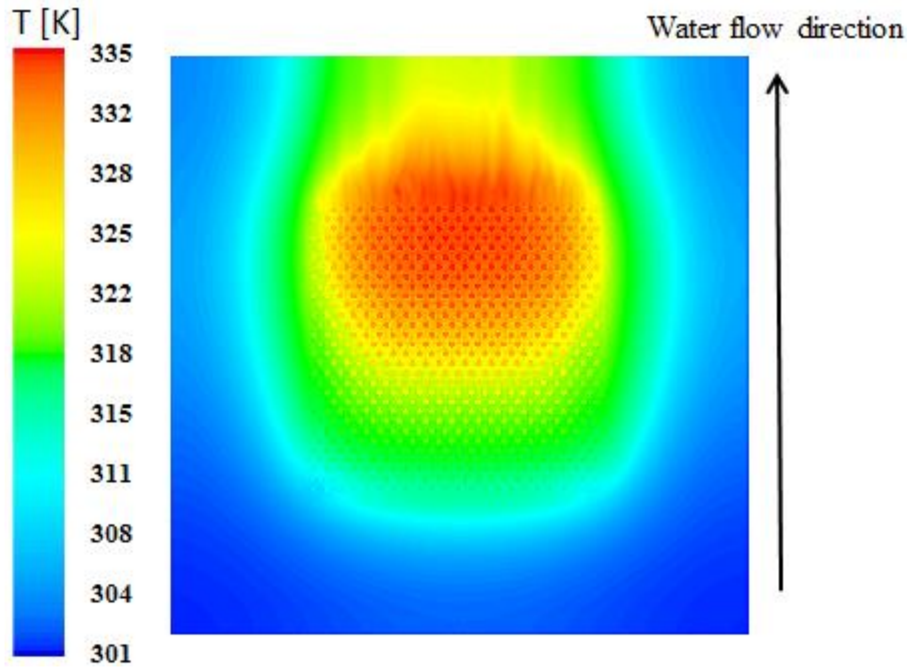

Figure 4.9 Bottom view of temperature distribution in a DBC with embedded pin fin microchannel.

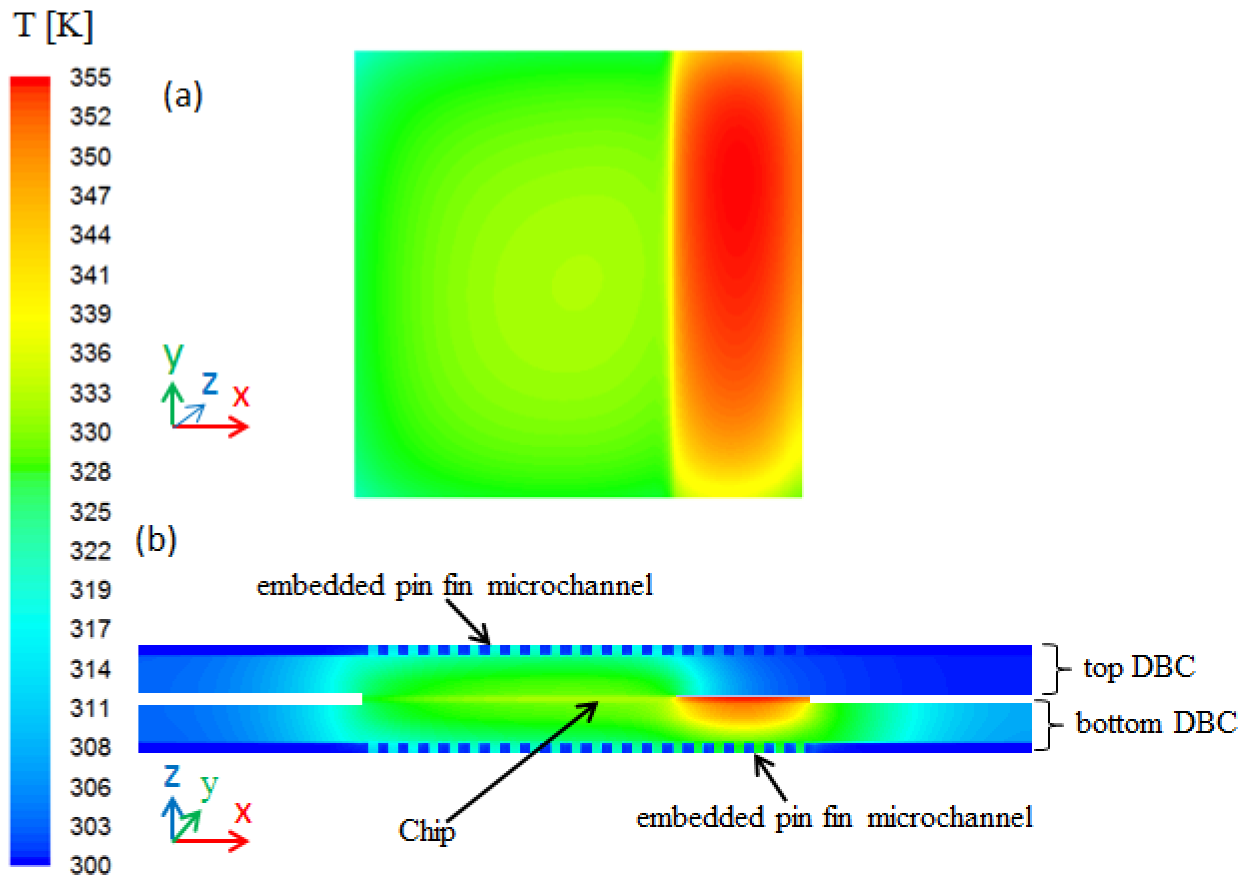

Figure 4.10 Temperature distribution in (a) Top view of the Si chip and (b) side view of the packaged IGBT in a double sided cooling. Water flows in y-direction.

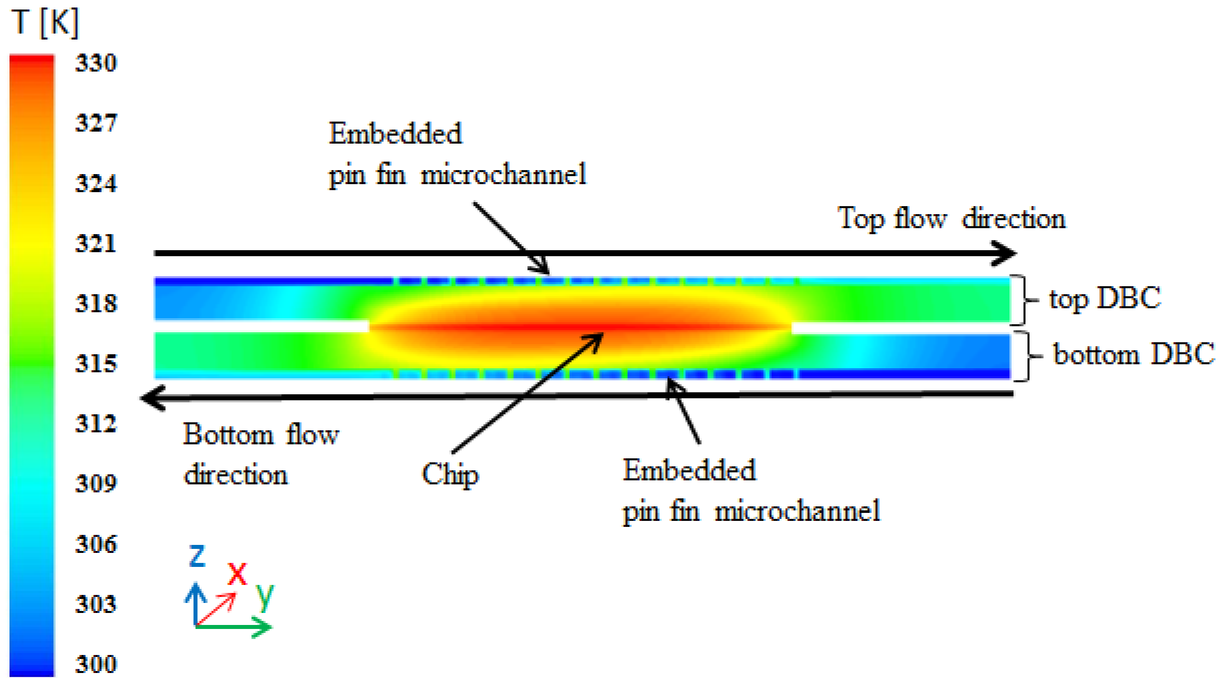

Figure 4.11 Side view of temperature distribution in a double-side cooled IGBT.

The relationships between power dissipation and required pumping power for all three cooling methods are shown in Figure 4.12. The pumping power for double sided cooling shown is the total pumping power from both top and bottom microchannels. It is clear that double sided cooling is advantageous over single sided cooling in terms of the amount of heat removed per unit of power input.

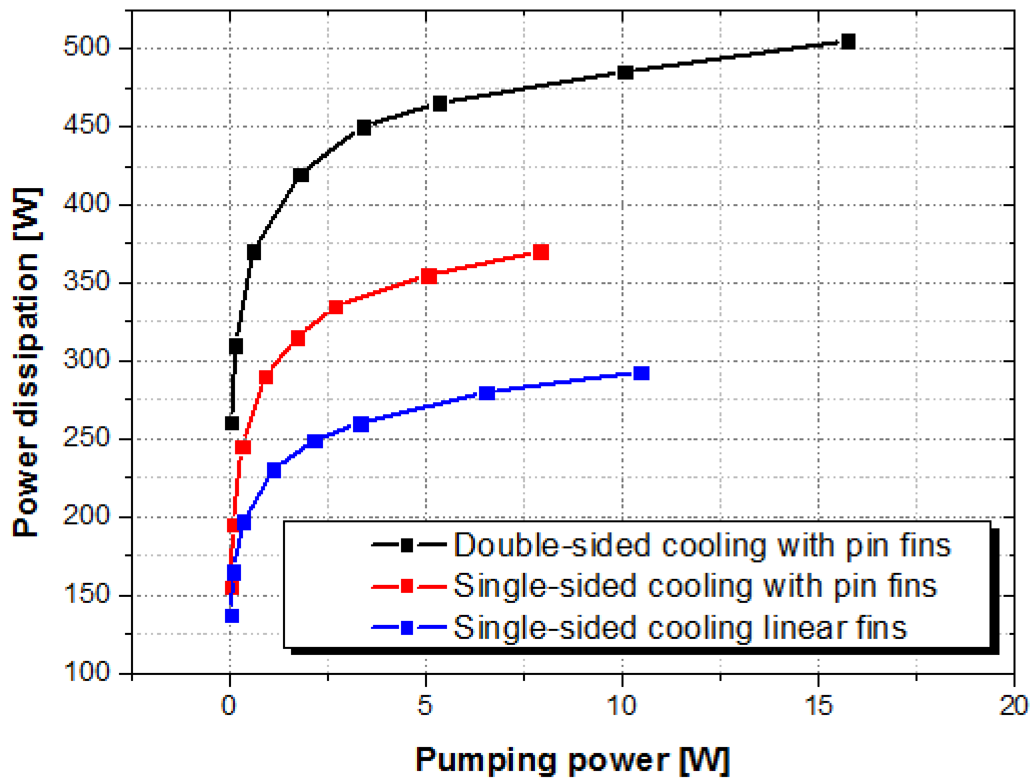

Figure 4.12 Power dissipation in the chip verses. pumping power for different cooling methods. The maximum pressure drop for each microchannel cold plate is 200 kPa. And the maximum temperature rise in the chip is 55 °C. The pumping power for the double sided cooling is the total power required by both top and bottom microchannel cold plates.

4.4 Conclusion

Under the same pumping power condition, double sided cooling with embedded pin fin microchannels into the Cu layer of the DBC provides the best cooling performance based on simulation results presented above. Double sided cooling can increase power by 31.5% and 77% from single sided cooling with pin fins and single sided cooling with linear fins at a pumping power of 5 W. For a given number of chip(s), this reduced thermal resistance using double sided

cooling can increase the power range, operating frequency of the converters or the lifetime of the devices. For a giving current rating, this reduced thermal resistance can help to reduce the number of chips and thus reduce the volume and cost.

CHAPTER 5 CONCLUSION AND FUTURE WORK

The motivation of this work was to decrease the junction temperature of both AlGaN/GaN HEMT and IGBT devices by reducing the thermal resistance between the junction and the coolant. We proposed that by placing the heat sink closer to the heat source, this thermal resistance would be reduced. To validate this proposed idea, numerical studies using ANSYS Fluent were performed.

For the AlGaN/GaN HEMT devices, while using the same substrate material, embedded microchannel liquid cooling show a significant reduction (>35%) in thermal resistance compared to conventional cooling. The greatest benefit we found from embedding microchannels into device substrate for liquid cooling was that using low cost low thermal conductivity silicon substrates employing liquid cooling have a similar thermal performance to using high cost high thermal conductivity silicon carbide substrates in conventional cooling. And the use of silicon carbide in embedded microchannel liquid cooling outperforms the use of extremely expensive CVD diamond in conventional cooling. The calculated required pumping power for forced liquid cooling was 0.2 W to dissipate 30.6 W and 20.16 W of joule heat from GaN on SiC and GaN on Si, respectively. The use of pin fins greatly reduced the required pumping power compared to linear fins in microchannel heat sinks while also providing a slightly higher power density under the same maximum device temperature condition. Under extreme ambient temperatures (-30 °C and 80 °C ambient temperatures), microchannel liquid cooling using ethylene glycol for GaN on silicon carbide still outperforms conventional cooling using CVD diamond substrate. However, liquid cooling using silicon substrates did not work as well as conventional cooling using silicon carbide under these extreme conditions. Embedded diamond microchannel liquid cooling with

200 μm diamond substrate gave the highest power density (10.9 W/mm) among all the cases studied in this work.

For IGBT devices, in single-sided cooling, the thermal resistance for the case with pin fin microchannel was 27% less than that with linear fin microchannel under the same pressure drop condition. Pin fin microchannel heat sinks also had a lower required flow rate than linear microchannels under the same pressure drop. Thus, a significant reduction in pumping power was seen by using pin fin microchannels. Double-sided cooling with fin pins further reduced the thermal resistance by 35% and 52% compared to single-sided cooling with pin fins and with linear fins, respectively. The thermal resistance of double-sided cooling with pin fins was only 22% of the thermal resistance of the baseline.

Future Work

As computational results show that embedded microchannel liquid cooling with silicon carbide substrate show promising thermal management performance for AlGaN/GaN HEMTs, it is encouraging to continue the work by extending this work to experiments. In order to conduct experiments to validate these simulation results, fabrication of such pin fin microchannel heat sink is needed. For both HEMT and IGBT devices, it is worth studying microchannels with different features, for instance, manifolds or jet impingement, which can induce stronger turbulence intensity in the flowing fluid inside the heat sink, and/or cause smaller pressure drop than pin fin microchannels studied so far. In addition, new pin fin geometries other than those studied here should be considered. It is possible to make airfoil-like structures which provide less flow resistance than pin fin structures and could provide additional benefit in thermal performance. The arrangement of these structures do not have to be uniformly placed and should

be studied by CFD analysis. Finally, methods to manufacture the integrated cooling in DBC substrates can be considered using 3D printing or micro-precision machining to enhance the practicality of making complex structures for microchannel cooling.

APPENDIX I

```
#include "udf.h"

DEFINE_PROPERTY(kGaN, cell, thread)

{

float temp, ktc;

temp=C_T(cell, thread);


ktc=150*pow((temp/300),(-1.4));

return ktc;

}


DEFINE_PROPERTY(kSi, cell, thread)

{

float temp, ktc;

temp=C_T(cell, thread);


ktc=148*pow((temp/300),(-1.3));

return ktc;

}

DEFINE_PROPERTY(kSiC, cell, thread)

{

 float temp, ktc;

temp=C_T(cell, thread);


ktc=387*pow((temp/293),(-1.49));

return ktc;

}

DEFINE_PROPERTY(kcuw, cell, thread)

{

float temp, ktc;

temp=C_T(cell, thread);
```

```
ktc=204-0.0251*temp-0.0000762*pow(temp,2);

return ktc;

}

DEFINE_PROPERTY(muWater, cell, thread)

{

 float temp, ktc;

temp=C_T(cell, thread);


ktc=2.414*0.00001*pow(10,(247.8/(temp-140)));

return ktc;

}

DEFINE_PROPERTY(muEGlowT, cell, thread)

{

 float temp, ktc;

temp=C_T(cell, thread);


ktc=4.887e8*exp(-0.09636*temp)+6.64*exp(-0.02558*temp);

return ktc;

}

DEFINE_PROPERTY(muEGhighT, cell, thread)

{

 float temp, ktc;

temp=C_T(cell, thread);


ktc=4.6656934*pow(10,-4)*pow((temp/100),2)-4.3262731491*pow(10,-
3)*(temp/100)+0.0103252511;

return ktc;

}

DEFINE_PROPERTY(muEGroomT, cell, thread)

{

 float temp, ktc;
```

```
temp=C_T(cell, thread);


ktc=7.4813*pow(10,-3)*pow((temp/100),4)-
0.108321748*pow((temp/100),3)+0.58887746442*pow((temp/100),2)-
1.4259595*(temp/100)+1.299716962;

return ktc;

}

DEFINE_PROPERTY(muEGmedianT, cell, thread)

{

 float temp, ktc;

temp=C_T(cell, thread);


ktc=104.1*exp(-0.03621*temp)+0.009481*exp(-0.007735*temp);

return ktc;

}

DEFINE_PROPERTY(kdiamond, cell, thread)

{

 float temp, ktc;

temp=C_T(cell, thread);


ktc=0.0024*temp*temp-3.3967*temp+1983.4;

return ktc;

}

DEFINE_PROFILE(heatflux_profile,t,i)
{

 face_t f;

 begin_f_loop(f,t)

 {


F_PROFILE(f,t,i)=(((sin(1*6.283*CURRENT_TIME/0.000002)/1+sin(3*6.283*CURRENT_TIME/0.00000
2)/3+sin(5*6.283*CURRENT_TIME/0.000002)/5+sin(7*6.283*CURRENT_TIME/0.000002)/7+sin(9*6.28
3*CURRENT_TIME/0.000002)/9+sin(11*6.283*CURRENT_TIME/0.000002)/11+sin(13*6.283*CURRENT_TI
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0.000002)/95+sin(97*6.283*CURRENT_TIME/0.000002)/97+sin(99*6.283*CURRENT_TIME/0.000002)/9
9)*4/3.14159+1)/2)*pow(10,10)*1.34;

 }

 end_f_loop(f,t)

}
```

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