EXPERIMENTAL AND THEORETICAL ASSESSMENT OF THIN GLASS PANELS AS INTERPOSERS FOR MICROELECTRONIC PACKAGES

A Thesis
Presented to
The Academic Faculty

by

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In Partial Fulfillment
of the Requirements for the Degree
Master's of Science in the
School of Mechanical Engineering

Georgia Institute of Technology
May 2014

EXPERIMENTAL AND THEORETICAL ASSESSMENT OF THIN GLASS PANELS AS INTERPOSERS FOR MICROELECTRONIC PACKAGES

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ACKNOWLEDGEMENTS

There are many people that I need to thank for their time, energy, and support for not only this work, but for helping to get me here.

I would like to thank my advisor, Prof. Suresh Sitaraman, who provided incredible support and guidance throughout my time at Georgia Tech. I would also like to thank Prof. Rao Tummala and Prof. Yogendra Joshi for their valuable time and feedback as committee members.

In addition to being a committee member, I would like to thank Prof. Tummala as the Director of 3D Microsystems Research Center (Packaging Research Center), which provided the industry based motivation for my work. I am in debt to many other members of PRC, including: Makoto Kobayashi, Anne Matting, Vanessa Smet, and Anna Stumpf for assembly work and discussions; Florian Nebe, Ichiro Sato, Yutaka Takagi, and Tao Wang as well as Jason Bishop and Chris White for cleanroom assistance; and Patricia Allen, Karen May, and Brian McGlade for administrative support.

I would like to thank the members of Computer-Aided Simulation of Packaging Reliability (CASPaR) Lab who offer valuable discussion and support every day, including Wei Chen, Justin Chow, Xi Liu, Raphael Okereke, and Christine Taylor. In particular, I would like to thank Sathya Raghavan for modeling support and experimental guidance.

I would like to thank my parents who have provided incredible love, support, guidance, and friendship throughout my life, and without whom, I would not be where I am or who I am today. I would like thank my sister, Katherine, as well as my extended family.

Lastly, I would like to thank God for the many opportunities and strength He provides me on a daily basis.

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LIST OF SYMBOLS

α – coefficient of thermal expansion

$\Delta\varepsilon_P$ – Plastic strain range

N_f – Fatigue life

ε_{acc}^{in} – Inelastic accumulated strain

ε_{ij} - Component ij of the strain tensor

$\dot{\varepsilon}^{pl}$ – Inelastic strain rate tensor

$\dot{\bar{\varepsilon}}^{pl}$ – Rate of accumulated equivalent plastic strain

S_{ij} – Deviatoric stress

$\bar{\sigma}$ – Equivalent stress

A, ξ, m, h_0, a – Material constants for Anand's model

Q – Activation energy for Anand's model

R – Universal gas constant

s – Internal state variable

s* - Deformation resistance

LIST OF ABBREVIATIONS

T_g – Glass transition temperature

BGA – Ball Grid Array

CTE – Coefficient of Thermal Expansion

FE(M) – Finite Element (Method)

I/O – Input/Output

IC – Integrated Circuit

ECTC – Electronic Components and Technology Conference

CPMT – Components, Packaging, and Manufacturing Technology

SUMMARY

As the microelectronic industry moves toward stacking of dies to achieve greater performance and smaller footprint, there are several reliability concerns when assembling the stacked dies on current organic substrates. These concerns include excessive warpage, interconnect cracking, die cracking, and others. Silicon interposers are being developed to assemble the stacked dies, and then the silicon interposers are assembled on organic substrates. Although such an approach could address stacked-die to interposer reliability concerns, there are still reliability concerns between the silicon interposer and the organic substrate. This work examines the use of diced glass panel as an interposer, as glass provides intermediate coefficient of thermal expansion between silicon and organics, good mechanical rigidity, large-area panel processing for low cost, planarity, and better electrical properties. However, glass is brittle and low in thermal conductivity, and there is very little work in existing literature to examine glass as a potential interposer material.

Starting with a 150 x 150 mm glass panel with a thickness of 100 μm, this work has built alternating layers of dielectric and copper on both sides of the panel. The panels have gone through typical cleanroom processes such as lithography, electroplating, etc. Upon fabrication, the panels are diced into individual substrates of 25 x 25 mm and a 10 x 10 mm flip chip with a solder bump pitch of 75 um is then reflow attached to the glass substrate followed by underfill dispensing and curing. The warpage of the flip-chip assembly is measured. In parallel to the experiments, numerical models have been developed. These models account for viscoplastic behavior of the solder. The models

also mimic material addition and etching through element “birth-and-death” approach. The warpage from the models has been compared against experimental measurements for glass substrates with flip chip assembly. It is seen that the glass substrates provide significantly lower warpage compared to organic substrates, and thus could be a potential candidate for future 3D systems.

CHAPTER 1

INTRODUCTION

As integrated circuits (ICs) have scaled according to Moore's Law [1], microelectronic packages have also continued to scale over the last several decades with higher interconnect density. As the technologies available have ranged from 2D wire-bonded packages through area-array flip-chip and, more recently, 2.5D and 3D, the capabilities of packaging have exponentially increased to provide more I/Os. In doing so, the interconnect pitch has decreased proportionally.

Packaging today is commonly done with an organic substrate such as FR4, which has been the case since transitioning from ceramics in the 1990s. As packaging continues to scale, the limits of organic substrates are being approached. The demand for thinner packages, primarily from a mobile perspective, reduces the mechanical support and rigidity an organic substrate can provide. As size increases, organic packages have limited dimensional stability. Also, with organic substrates, there are limits in terms of line widths and spaces. This is due to fact that the organic substrates are not as planar and smooth as silicon, glass, or ceramic substrates. Furthermore, the higher coefficient of thermal expansion (CTE) of the organic substrate creates assembly yield issues due to the differential lateral displacement between the substrate and the die. Also, the large CTE mismatch creates die-to-substrate reliability concerns as well. On the other hand, although ceramics can address most of these issues associated with organic substrates, cost is a major impediment.

Glass has the potential to combine some of the benefits of ceramics and organics. For example, glass is rigid. The CTE of the glass can be tailored to meet silicon or

organic CTE. In other words, glass can function as an interposer with an intermediate CTE between silicon and organic board. Glass is smooth and planar, and therefore, amenable to fabricating fine lines and spaces. Glass is available in large panels, and therefore, will facilitate large-area processing. Glass is inexpensive compared to ceramic. However, glass has other challenges that need to be addressed and studied. Fabrication and assembly processes have been well established for silicon, ceramic, and organic materials, while process development for glass is still in its infancy. For example, metallization of glass, lamination on glass, fine via drilling and metallization, and other processes need to be extensively studied and characterized. The thermal, mechanical, and electrical properties and performance of glass have not been adequately studied in literature for microelectronic packaging applications. The objective of this work is to study the processing of glass substrates through numerical models and experiments, and to compare the results against organic and silicon substrates. In particular, this thesis focuses on warpage induced in glass substrates during thin-film processing as well as during die assembly. This work employs finite-element birth-and-death approach to simulate thin-film processing as well as die assembly process. The simulation includes the thermal history associated with such processes as well as material and geometry parameters at various stages of the processes. This work compares the predicted warpage results against experimental data. Also, this work compares the warpage behavior of glass substrate against silicon and organic substrates, and develops design guidelines for glass substrates to minimize warpage.

In this work, the terms interposer and substrate are used interchangeably and refer to one item between a silicon die and the system printed circuit board.

CHAPTER 2

LITERATURE REVIEW

This chapter provides background on warpage during substrate fabrication, warpage during assembly. It also provides historical background and a discussion of current substrate materials.

As per the JEDEC Standard for Package Warpage Measurement of Surface-Mount Integrated Circuits at Elevated Temperatures [2], warpage is defined as the distance between the contact and reference planes. In general, a dome shape is defined as convex warpage, while a bowl shape is defined as concave warpage. Convex warpage, known as positive warpage, is when the corners of the package are closer to the contact plane than the center of the bottom surface. Concave warpage, known as negative warpage, is when the corners of the package are further from the contact plane than the center of the bottom surface.

2.1 Substrate Warpage: Causes and Problems

Substrate warpage is warpage during substrate fabrication. A substrate contains materials including the core material, polymer or dielectric, copper, solder resist, nickel, gold, etc. An example cross-section of a ball grid array package (BGA) is illustrated in Figure 2.1. Copper traces throughout the substrate route electrical signals, while vias connect between layers and across the entire substrate. The fabrication for a substrate utilizes a series of processes to deposit, laminate, etch, etc., each of which uses an optimized process for a set amount of time at a specific temperature. This subsequent series of processes can create stress. If the stress is uneven, the substrate warps [3] [4].

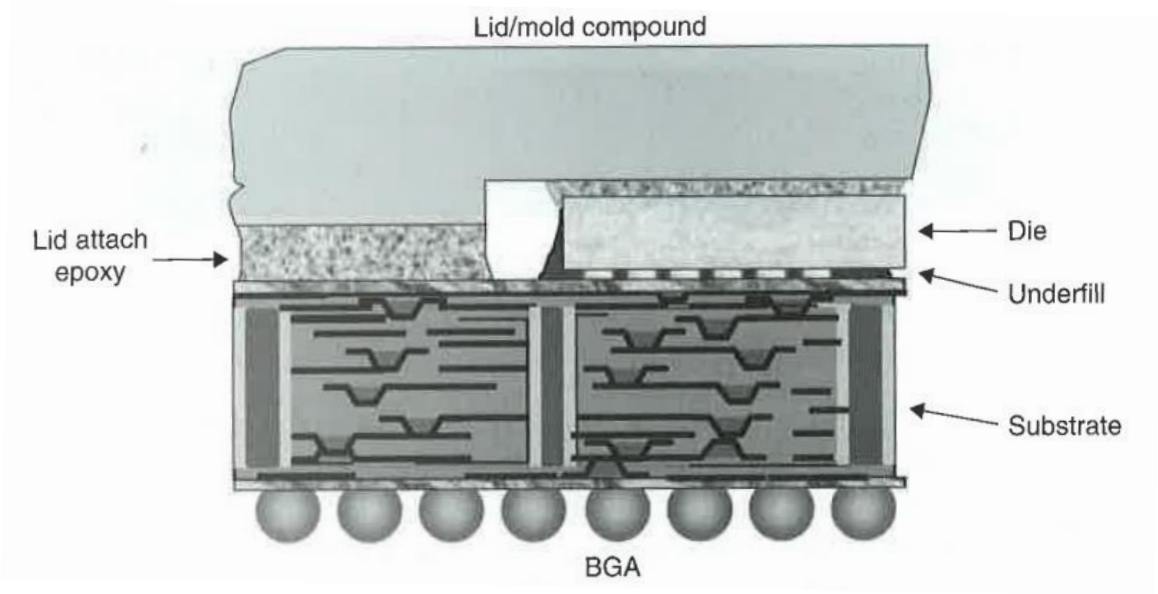


Figure 2.1: Cross-section of ball grid array package (credit: [5]).

To study the warpage of a fabricated substrate, laminate theory can be applied. This theory takes into account the dimensions and properties of each layer and can be applied to anisotropic elastic materials. Laminate theory for steady-state without in-plane forces can be simplified to the equations,

$$\frac{\partial N_x}{\partial x} + \frac{\partial N_{xy}}{\partial y} = 0 \qquad \textbf{(2.1)}$$

$$\frac{\partial N_{xy}}{\partial x} + \frac{\partial N_y}{\partial y} = 0 \qquad \textbf{(2.2)}$$

$$\frac{\partial^2 M_{xx}}{\partial x^2} + 2\frac{\partial^2 M_{xy}}{\partial x \partial y} + \frac{\partial^2 M_{yy}}{\partial y^2} + q + \bar{N}_x \frac{\partial^2 w_0}{\partial x^2} + 2\bar{N}_{xy}\frac{\partial^2 w_0}{\partial x \partial y} + \bar{N}_y \frac{\partial^2 w_0}{\partial y^2} = 0 \qquad \textbf{(2.3)}$$

where q is the transverse force, $\bar{N}_x$, $\bar{N}_y$, and $\bar{N}_{xy}$ are the in-plane applied forces, M_x, M_x, and M_{xy} are the moments, and for a rectangular laminate that is simply support at $x = 0$ and $y = 0$, the solution for the warpage, w_0 has the form

$$w_0 = \sum_{m=1}^{\infty} W_m(x)\sin(\beta y) \quad \textbf{(2.4)}$$ [6].

However, such laminate theories have several approximations and assumptions. Different stress-free temperatures for different materials are difficult to include in laminate theory models. Linear-elastic material behavior is easily captured in laminate theory models; however, elastic-plastic or viscoplastic behavior is not captured in such models. Most of the laminate models assume that the layers are of equal size. In reality, with substrate fabrication and die assembly, the layers are of different planar dimensions. Laminate theory models usually assume that each layer is made of one material with appropriate material properties. However, in flip-chip assemblies on substrates, different layers have combination of materials in the same layer. For example, the gap between the die and substrate contains both viscoplastic solder as well as viscoelastic underfill material. For such composite layers, the properties have to be approximated using some smearing before laminate plate theory can be used.

The finite element method (FEM) is a numerical approach [7] [8] that is often applied to microelectronic package warpage problems, e.g. [3] [9]. This is because numerical models can account for direction-, time-, and temperature-dependent material properties. Also, they can account for different layers having different dimensions and features. They can model individual geometry entities within a given layer without using smeared properties. Work by Tan and Ume have compared laminate theory and FEM approaches during surface mounting, in addition to comparing with closed form equations of the differential equations of thermo-mechanics. The results from the FEA were found to closely agree with experimental validation [6].

Substrate fabrication includes a wide temperature range. Annealing copper traces above the glass transition temperature of the polymer can cause or change the

deformation of the structure. Studies have been done on the viscoelastic material properties of polymers [10] as well as the effects of cooling process and rate effects on residual warpage [11].

The thickness of each material is critical as well for a multilayered substrate. Layers that were once very thin in comparison with the substrate core, such as copper traces, are becoming more important as substrates and dies become thinner [4] [12].

2.2 Assembly Warpage: Causes and Problems

Assembly joins the silicon chip onto organic substrate, where the silicon has a CTE of 2.6 ppm/ºC [13] and the organic has a CTE of about 20 ppm/ºC [14]. Die to substrate assembly requires reflowing solder, which requires temperatures of 230 ºC to 260 ºC for lead-free solders. The reliability thermal cycling range of microelectronics packages is between -55 to 125 ºC [15]. This is an accelerated thermal cycling range, although most packages do not experience these extreme temperature conditions. Thus, the temperature change between reflow temperature to room temperature and to further thermal cycling temperature extremes, in combination with the CTE mismatch, creates warpage.

Warpage of substrate creates several fabrication and reliability issues. For example, during sequential fabrication, mask alignment and exposure will be affected when the substrate has warpage. Particularly, this has significant effect on fine features. When the package substrate warps, assembly of flip-chip on the substrate is a challenge, especially for large packages. The chip solder bumps do not properly align with the substrate pads under excessive warpage, and thus, will affect assembly yield. Furthermore, the standoff height of the bumps from the die center to edge will be

different with the substrate warpage leading to solder opens. Once the chip is assembled on to organic substrate, the entire package will have more warpage than a stand-alone substrate. Therefore, assembly of the second-level solder bumps will also be a challenge.

In addition to board assembly challenges, warpage can have an impact on thermal performance. High performance applications require active cooling, often in the form of a heat sink attach to the die with thermal paste to improve heat conduction. When the die and substrate assembly warps, the gap between the die and the heat spreader or heat sink is non-uniform, and therefore, it could lead to excessive thickness of the thermal interface material [16] and/or debonding of the thermal interface material under thermal excursions [17] [18].

In addition to warpage, the difference in CTE between different materials will cause solder strain under thermal excursions, and will affect solder fatigue life, e.g. [19] [20]. According to JEDEC standards, thermal cycling is the standard way to test fatigue life [15]. To model thermal cycling and predict fatigue life, FEM with viscoplastic material models for solder has been used [21] [22]. To model solder as a viscoplastic material, Anand's model is a commonly-used implementation within FEM, e.g. [23].

2.3 Warpage Measurement Techniques

As the microelectronic world continues to shrink, more advanced techniques to measure warpage are required. Old methods, such as a gauge indicator shim, are inadequate. Contact profilometry requires a probe to move across the surface, making it a very slow method of data collection.

Noncontact options include optical interferometry, digital image correlation, and moiré methods. Optical interferometry uses interference of two or more light waves for distance measurements. The classical interferometry technique, Twyman-Green, is full-field and high resolution but requires a complex and expensive setup [24]. Digital image correlation is a full-field technique to measure strain or displacement, however, the optical system has difficulty dealing with silicon surface. Moiré methods are a subset of interferometry that use overlapping periodic grating lines and takes advantage of moiré fringes. Moiré methods include shadow moiré, projection moiré, and digital fringe projection. Of these, shadow moiré has the highest resolution, fastest data acquisition, and fastest computation time. The downside is that it requires a master glass grating that may affect the thermal behavior of the sample [24]. Shadow moiré is often viewed as the best option for warpage measurements and is widely used [20] [25] [6].

2.4 Approaches to Reduce Warpage

Warpage is an unavoidable problem: it is impossible to fabricate a substrate and assemble it and not have it warp. Thus, ways to control and reduce warpage are sought out. In industry, warpage is approached as a size limitation; larger packages have more warpage [26]. Thus, by limiting the size of the package, the warpage is constrained.

To reduce warpage during substrate fabrication, processes can be done to both sides symmetrically or mirrored as closely as possible. Depositing layers of polymer on both sides at once and designing masks with similar amounts of copper in each region will reduce or eliminate warpage.

As packages continue to get thinner, warpage gets worse. The core that provides mechanical rigidity to the package is reduced, providing less support to the package [27].

Since warpage is a function of CTE mismatch, changing the materials can reduce the warpage. Underfills and polymers have high CTEs. However, it is not simple or straight forward to modify the CTE of these materials without influencing other properties. For example, filler particles are used with epoxy underfills which reduces the underfill CTE. However, the filler particles increase the modulus of the underfill and thus tightly couple the die to the substrate. Altering the polymer chemistry could influence the dielectric, thermal, and other properties of these materials, and could also affect their cure regimes and adhesion to different materials. Low CTE materials have been investigated to achieve lower warpage, e.g. [28] [29]. This work uses glass as a substrate material in part because of the low CTE.

2.5 Status on Substrate Materials

Historically, the packaging of integrated circuits (ICs) has changed each decade: leadframes in the 1970s, ceramics in the 1980s, and organics or wafer level packing (WLP) in the 1990s. Organics and WLP have continued to be widely used today. The continued demand for smaller, higher performing, more functional devices has pushed packaging to evolve. The limitations of organics are being pushed today, as the mobile space demands thinner packages and the high performance space requires less signal loss [5].

As a potential replacement to organic substrates, silicon and glass are under consideration. Silicon has the benefit of an already existing infrastructure of the semiconductor industry with vast knowledge on processes and handling, but is expensive. On the other hand, glass has little existing infrastructure, but is inexpensive, has high electrical resistance, has low loss, has high strength, has high modulus, and is resistance

to process chemicals [30]. The Packaging Research Center at Georgia Tech is investigating glass as a packaging material through several ongoing efforts. One such effort is focusing on laser drilling holes in glass interposers [31]. Another effort is focusing on plating and metallization of through package vias in glass [32]. Thermal performance of glass interposer is under investigation by Cho and Joshi [33]. Beyond using glass panels as interposer materials, the potential applications of glass are far reaching, including 3D glass photonics [34] and more [30].

CHAPTER 3

OBJECTIVES AND SCOPE OF RESEARCH

Although glass has been used in a wide range of applications, the use of glass as an interposer material is in research stages, far from practical implementation. Most of the ongoing research, however, focuses on the electrical and material aspects of glass. As such, there is a need for an assessment of the thermo-mechanical aspects of glass. Also, it is appropriate to compare and contrast the existing packaging materials compared to glass. Thus, the objectives of this research are to determine flip chip on glass package warpage through models and experiments, and to compare the warpage against other substrate/interposer materials.

To accomplish these objectives, this thesis will employ the following approach:

1. Fabricate glass interposers with polymer and metal layers and assemble silicon flip chip devices with underfill employing standard cleanroom and assembly processes
2. Measure the warpage of such flip chip on glass package through temperatures associated with the fabrication process
3. Develop physics-based numerical model to mimic the fabrication and assembly processes taking into consideration material addition at various temperatures
4. Determine through such models the warpage of flip chip on glass package and validate the modeling results against experimental data
5. Employ the models to study other substrate materials and other dimensions to develop design guidelines for minimizing package warpage

CHAPTER 4

GLASS INTERPOSER FABRICATION AND FLIP CHIP ASSEMBLY

This chapter provides details on sequential fabrication of polymer and metal layers on a glass panel in Section 4.1 and details on flip-chip assembly on glass in Section 4.2.

4.1 Two Metal Layer Glass Interposer Fabrication

Fabrication began with a bare thin glass panel. The panel was a low-CTE EN-A1 glass from Asahi Glass Co. Ltd., measuring 150 x 150 mm and would produce a five by five array of 25 x 25 mm interposers with dicing paths between the interposers. Although the processing was carried out on a panel, for the sake of clarity, the process steps are described using one interposer, as illustrated in Figure 4.1. Figure 4.1a depicts the cross section of a 25 x 25 mm interposer.

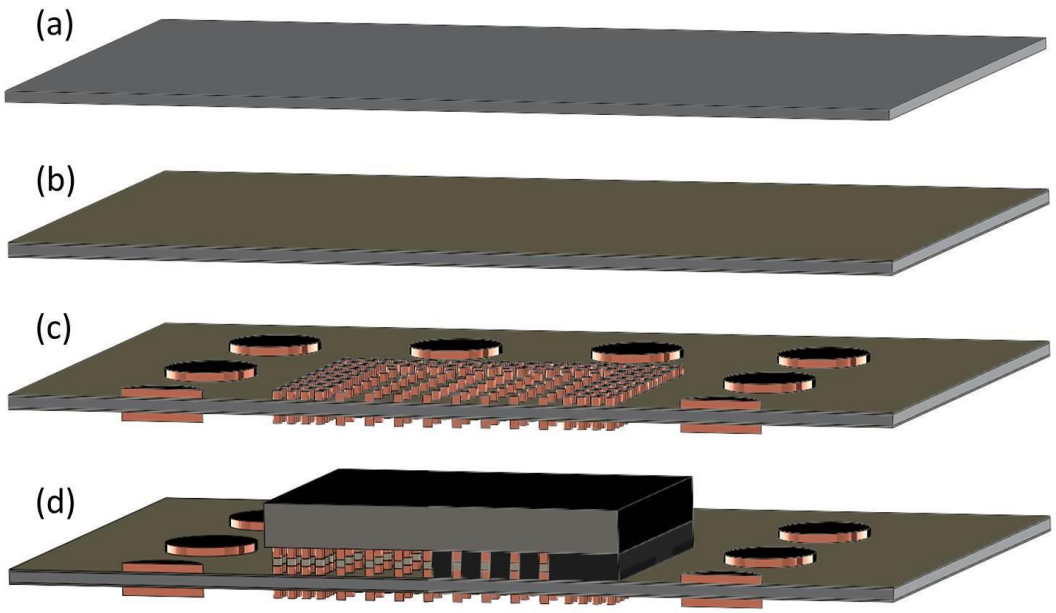


Figure 4.1: Cross section schematic of fabrication process steps. From the top, (a) bare glass; (b) polymer laminated glass; (c) interposer with trace pattern; (d) after die assembly (with partially hidden underfill).

First, the panel was cleaned using acetone and isopropyl alcohol. The panel was rinsed in distilled water and placed in an oven to dry. A surface treatment to enhance the adhesion between glass and polymer was applied to both sides. Then, 17.5 µm polymer layer of ZEONIF^{TM} ZS-100 was vacuum laminated on both sides of the glass panel. The panel was hot pressed at 115 ºC with 1.5 tons of force, and cured at 180 ºC for one hour, as represented in Figure 4.1b and as shown in Figure 4.2.

A semi-additive process ("SAP") was used to create the copper traces. The polymer laminated panel was cleaned using a desmear process. A copper seed layer was then deposited using an electroless bath. Palladium is used as an adherent prior to electroless copper plating, and therefore, palladium residue is usually present on the substrate surface. After electroless copper process, a dry photoresist film that is 15 µm thick, was laminated. The photoresist was exposed using the mask in Figure 4.3 and

developed. A photolithography optimization was performed to arrive at desired dimensions.

Figure 4.3 shows the mask on the substrate, which is a daisy chain pattern with test pads around the outside. The mask has five peripheral rows at 50 µm pitch in an in-line configuration, and a central area array at 150 µm pitch for a total of 7169 I/Os. The two insets, labeled (1) and (2), show detailed regions of the mask. The daisy chains are separated to isolate the critical areas, corners, and edges. At the end of assembly, the daisy chains were four-point probed to ensure assembly yield.

Copper was electroplated to 10 µm thick, as seen in Figure 4.4, which shows copper and photoresist on a glass panel. The photoresist was stripped, the copper seed layer is etched, and the palladium residue is etched. The palladium residue, which was left over from the electroless copper bath, was removed with Pallastrip^{TM} from Atotech Inc., which also etches copper. As this process was done in a beaker, the resulting traces were not of uniform height, varying from 5 to 10 µm. The result was a trace pattern of copper, shown as a cross section in Figure 4.1c and seen in Figure 4.5. The top view in Figure 4.5 is a five by five array of interposers on a 150 mm x 150 mm panel.

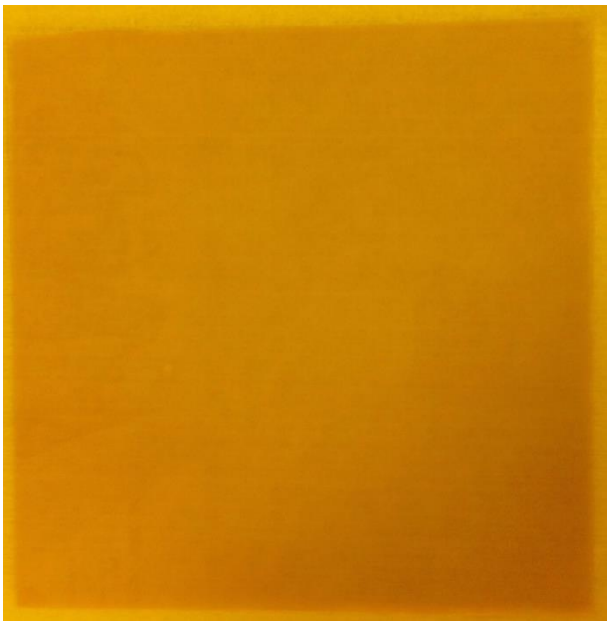


Figure 4.2: Glass panel during fabrication: after ZS-100 lamination, hot press, and curing.

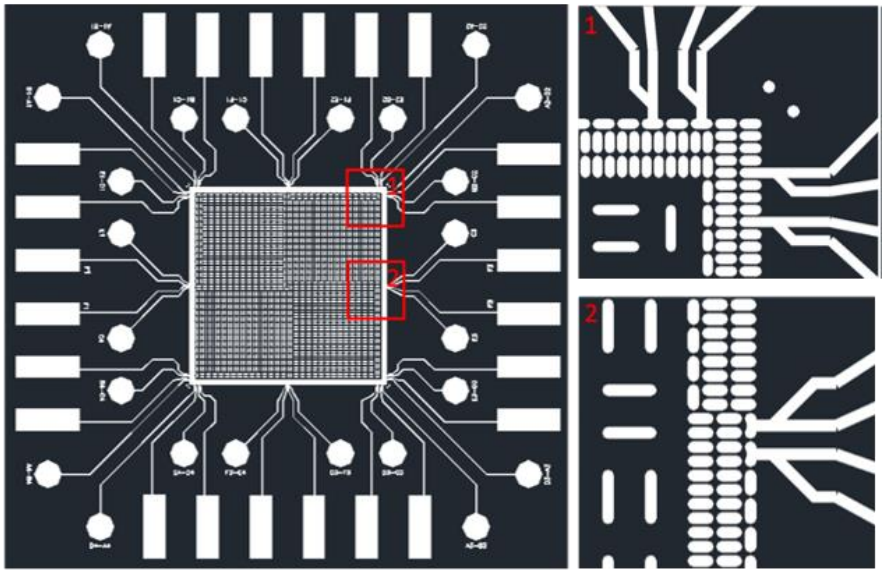


Figure 4.3: Mask used for interposer fabrication. Top image is full interposer layout with die region in center. Regions 1 and 2 are expanded below. The large pads surrounding the die are for test purposes.

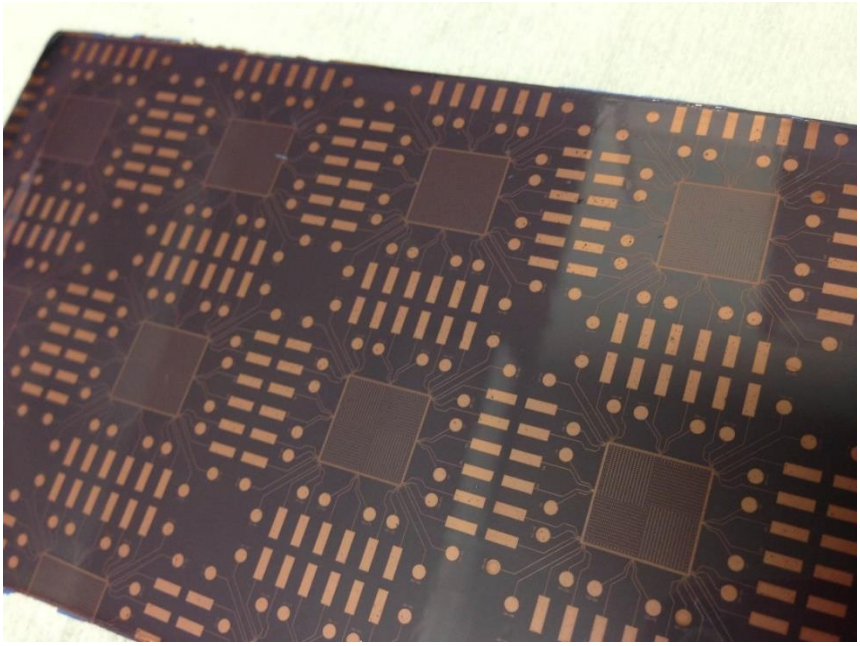


Figure 4.4: Glass panel during fabrication: after electroplating copper, before stripping photoresist.

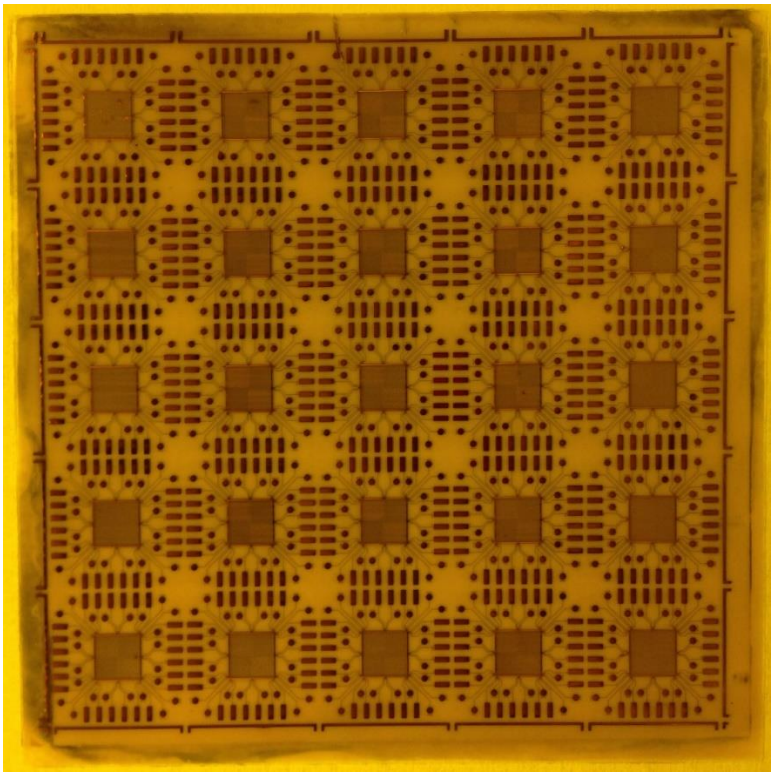


Figure 4.5: Glass panel during fabrication: after etching, before surface finish.

A palladium finish was applied using an electroless bath to prevent oxidation to the copper traces. The resulting panel with palladium color traces and pads are shown in Figure 4.6.

Although two metal layers are present on top and bottom of the glass interposer, no through-glass vias were fabricated in this work. Via fabrication through glass interposers is being pursued by other researchers within the Packaging Research Center at Georgia Tech.

4.2 Die Assembly with Glass Interposer

Before the die is assembled to the glass interposer, the panel was diced. The dicing was mechanical dicing with a Disco dicing tool at a speed of 1 mm/sec for 100, 150, and 300 μm glass.

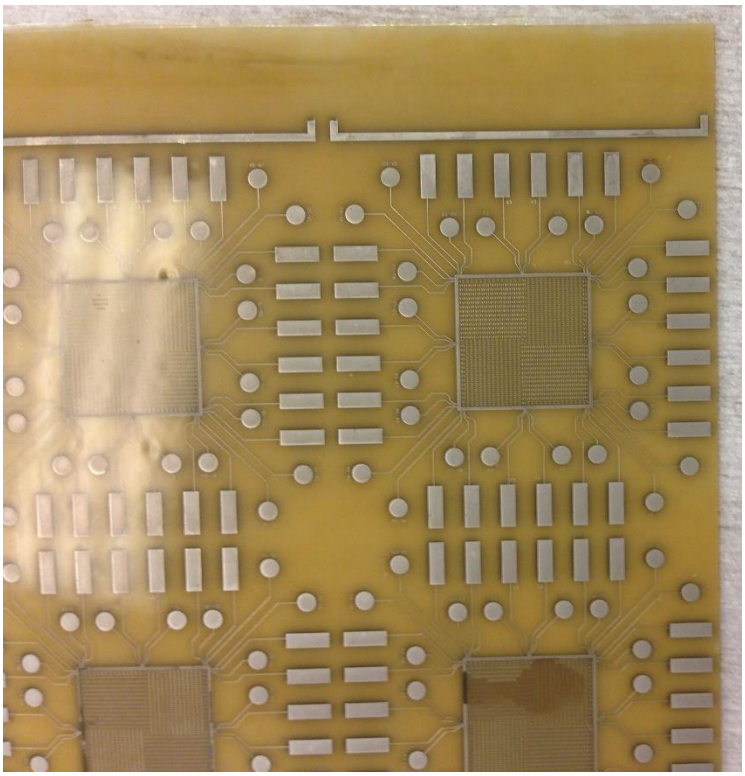


Figure 4.6: Partially diced glass interposer panel, prior to assembly.

A 10 x 10 mm silicon die was assembled to the glass interposer, as shown in Figure 4.1d. A 1-2 µm thick copper dogbone redistribution layer was laid out by electrolytic plating from a thin sputtered Ti/Cu seed layer. Copper micro-bumps with solder caps were plated on top of the RDL layer, 30 µm in diameter, with a 5 µm Cu height and a 10 µm co-plated Sn-3.5Ag height. Two dies of thickness 200 µm and 400 µm were used in this study. The assembly was carried out by the Interconnection and Assembly Team of the Package Research Center. To assemble the die to the interposer, a flux was first applied to the interposer. The silicon die was assembled on the glass interposer by flip-chip thermo-compression bonding with a peak temperature of 250 ºC for five seconds and a 1.5 MPa pressure for five seconds. No-clean tacky flux specific for lead-free applications was dispensed on the bonding area on the glass interposer prior to assembly.

Figure 4.7 shows the temperature profile used during the thermo-compression bonding, where the first plateau corresponds to the flux activation phase, while the second plateau corresponds to the solder reflow phase. The interposers were rinsed with acetone after assembly to remove any flux residue and baked at 150 ºC for 30 minutes before underfilling. Next, a capillary underfill was dispensed in an L-shape, at two edges of the die. The fillet was completed for the remaining edges of the die after capillary action. Then, the assembly was cured at 165 ºC for 90 minutes.

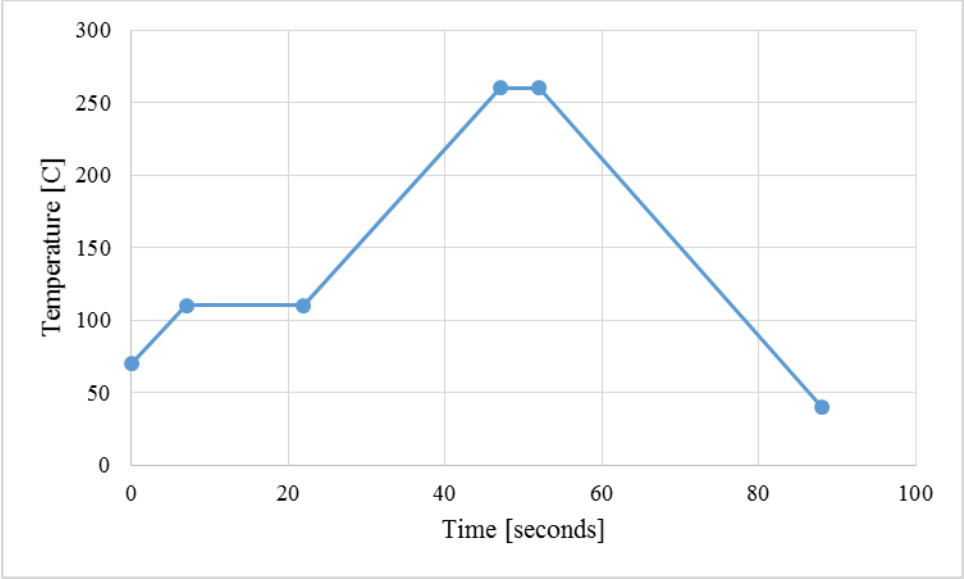


Figure 4.7: Temperature profile of thermo-compression bonding.

A 25 mm x 25 mm x 100 µm glass interposer with 10 mm x 10 mm x 400 µm die is shown in Figure 4.8 and a 25 mm x 25 mm x 300 µm glass interposer with 10 mm x 10 mm x 400 µm die is shown in Figure 4.9.

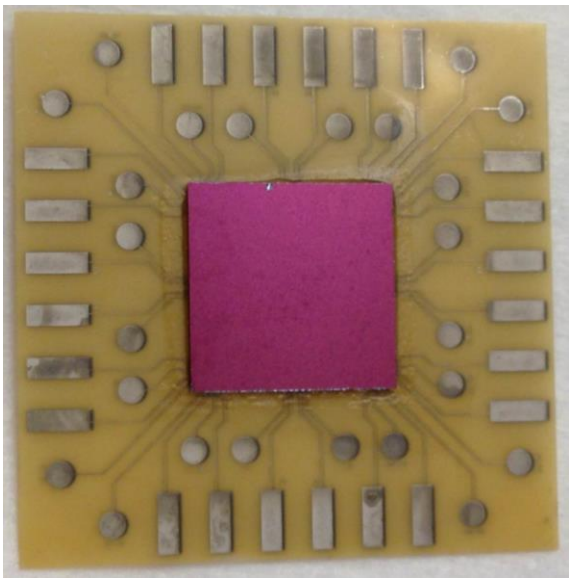


Figure 4.8: Assembled 25 mm x 25 mm x 100 µm glass interposer with 10 mm x 10 mm x 400 µm die (sample #1).

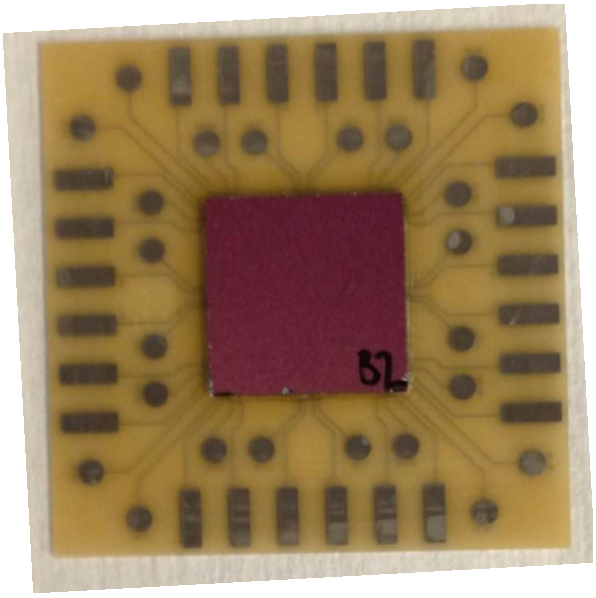


Figure 4.9: Assembled 25 mm x 25 mm x 300 µm glass interposer with 10 mm x 10 mm x 400 µm die (sample #2).

CHAPTER 5

SHADOW MOIRÉ WARPAGE MEASUREMENTS

This chapter provides details on full-field shadow moiré warpage results for three flip chip on glass samples at various temperatures. Shadow moiré uses phase stepping of moiré fringe images to create a high resolution, full-field measurement over a range of temperatures.

This work focuses on three glass interposer packages. The first, referred to as "sample #1" was a 25 mm x 25 mm x 100 µm glass interposer with a 10 mm x 10 mm x 400 µm silicon die. "Sample #2" was a 25 mm x 25 mm x 300 µm glass interposer with a 10 mm x 10 mm x 400 µm silicon die, only differing from sample #1 in the thickness of glass. "Sample #3" was a 18.4 mm x 18.4 mm x 150 µm glass interposer with a 10 mm x 10 mm x 200 µm silicon die. These samples were used for experimentally measuring warpage, and the warpage results were then used to validate the results from the predictive models.

5.1 Warpage Evolution During Interposer Fabrication

Using the fabrication and assembly process outlined in Chapter 4, glass interposer structures were fabricated and assembled. All interposers were built symmetrically, therefore, the panel was identical on top and bottom at almost all times. The variation in substrate height, if one were to run a profilometer, is due to surface roughness of the interposer or due to various trace and pad heights, rather than due to any warpage. Thus, the warpage during fabrication was negligible and could be viewed as zero.

The first material added was a uniform layer of a homogenous polymer material, ZEONIF^{TM} ZS-100. Steps used to deposit this layer were silane treatment, vacuum lamination, hot press, and curing. During silane treatment, the two sides of the glass were not identical, but silane solution does not produce any warpage. The polymer was added at the same time to both sides during vacuum lamination, and therefore, no warpage resulted due to vacuum lamination. However, the removal of the first protective plastic sheet from the polymer caused the warpage until the second protective plastic sheet was removed as well. When both sheets were removed, the resulting warpage was negligible. The fabrication proceeded identically on both sides during hot press. While the polymer was curing, the panel was vertical.

The desmear and electroless plating processes all used submersion baths. The glass panels were placed in a frame, which held the panels with light pressure normal to the surface around the edge. After the seed layer was deposited, the panels were identical on both sides, and the panels remained flat.

When photoresist dry film was laminated, it was laminated on one side of the panel, and then the other. As with the previous processes, no warpage was observed when one side of the panel was laminated and the other side was yet to be laminated. Exposure was performed on both sides of the panel prior to development. During development, solution was sprayed from both sides uniformly while the panel was placed horizontally.

The effects of the photolithography process depend on the mask(s) chosen. If the same mask was used on both sides of the panel, the warpage would be negligible upon thermal excursions. This was because the result is the same amount of copper in an

identical distribution on both sides. With different masks, the copper traces could create warpage with sufficient temperature change. In this work, all panels used the same mask for both sides, and thus, no warpage was observed from copper traces. Therefore, the panels did not have any apparent warpage prior to die assembly.

5.2 Shadow Moiré Tool

Shadow moiré measurements were taken with akrometrix's TherMoiré PS400^{TM} , shown in Figure 5.1 by Namics Corporation in Japan. Details on Shadow Moiré can be found in several publications [6] [35] [36]. For the sake of continuity and readability, a brief overview of the procedure is presented here. The tool is capable of measuring warpage with a sample size up to 400 x 400 mm to an accuracy of 2.5 µm. The samples were placed in a temperature chamber, capable of heating and cooling at 1 ºC per second up to 250 ºC and down to 50ºC. The machine could heat and cool beyond these changes but at a slower rate. Measurement with the TherMoiré PS400^{TM} requires painting the sample for data acquisition, which was done before measurement began. Higher resolution grating and paint could improve the accuracy of measurement at the cost of field of view height.

Shadow moiré fringe projection images were taken from the substrate side for samples #1 and #2 and taken from the die side for sample #3. This is visualized in Figure 5.2. Fringe projection images were captured at the prescribed temperatures of 30, 60, 80, 140, 200, 220, 240, and 260 ºC. The temperature ramp for data collection took 20 minutes after set up. The shadow moiré images were then analyzed using akrometrix

software to determine warpage magnitude at different locations of the sample, giving the results presented in Figure 5.10 and Figure 5.20.

Figure 5.1: TherMoiré PS400™ by akrometrix.

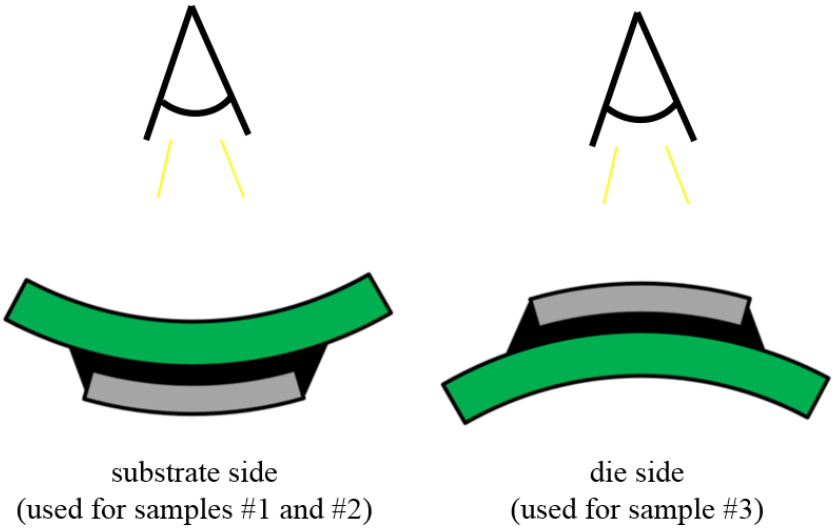


Figure 5.2: Viewing angle: die side and substrate side.

5.3 Shadow Moiré Data

5.3.1 Shadow Moiré Data for 25mm, 100µm Glass with 10mm, 400µm Die (Sample #1)

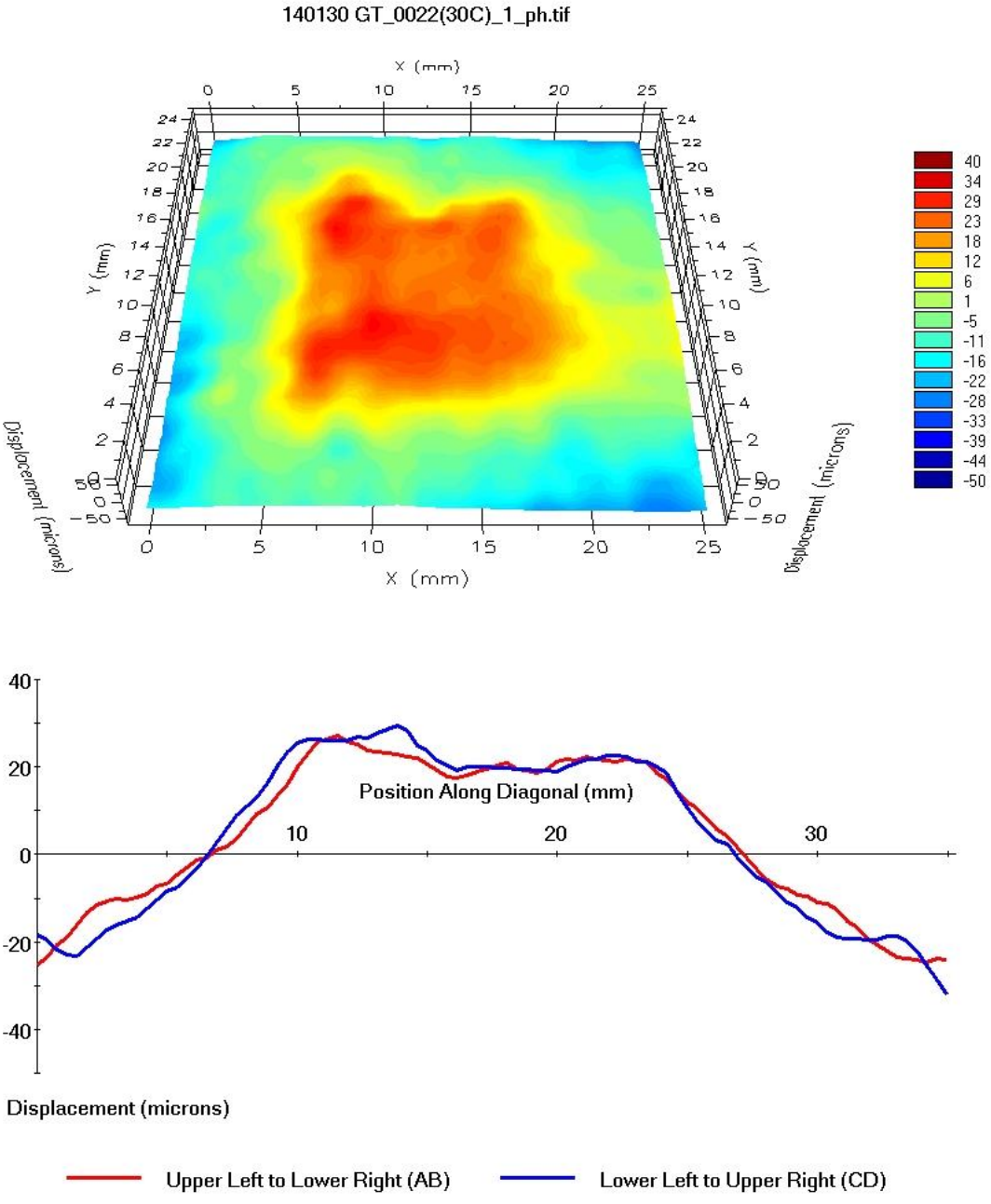


Figure 5.3: Shadow moiré data for 25 mm x 25 mm x 100µm glass with 10 mm x 10 mm x 400µm die (sample #1) at 30 ºC.

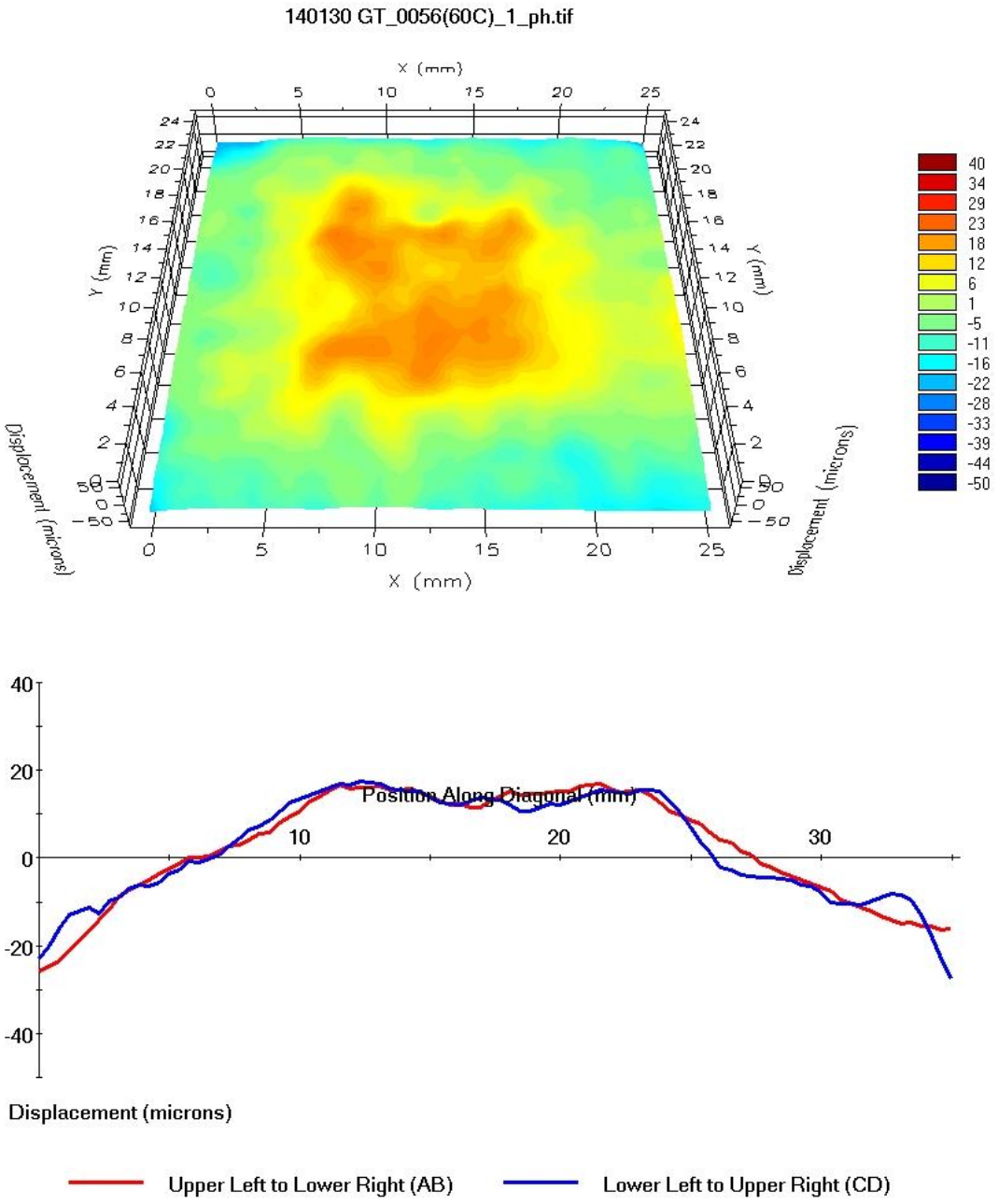


Figure 5.4: Shadow moiré data for 25 mm x 25 mm x 100µm glass with 10 mm x 10 mm x 400µm die (sample #1) at 60 ºC.

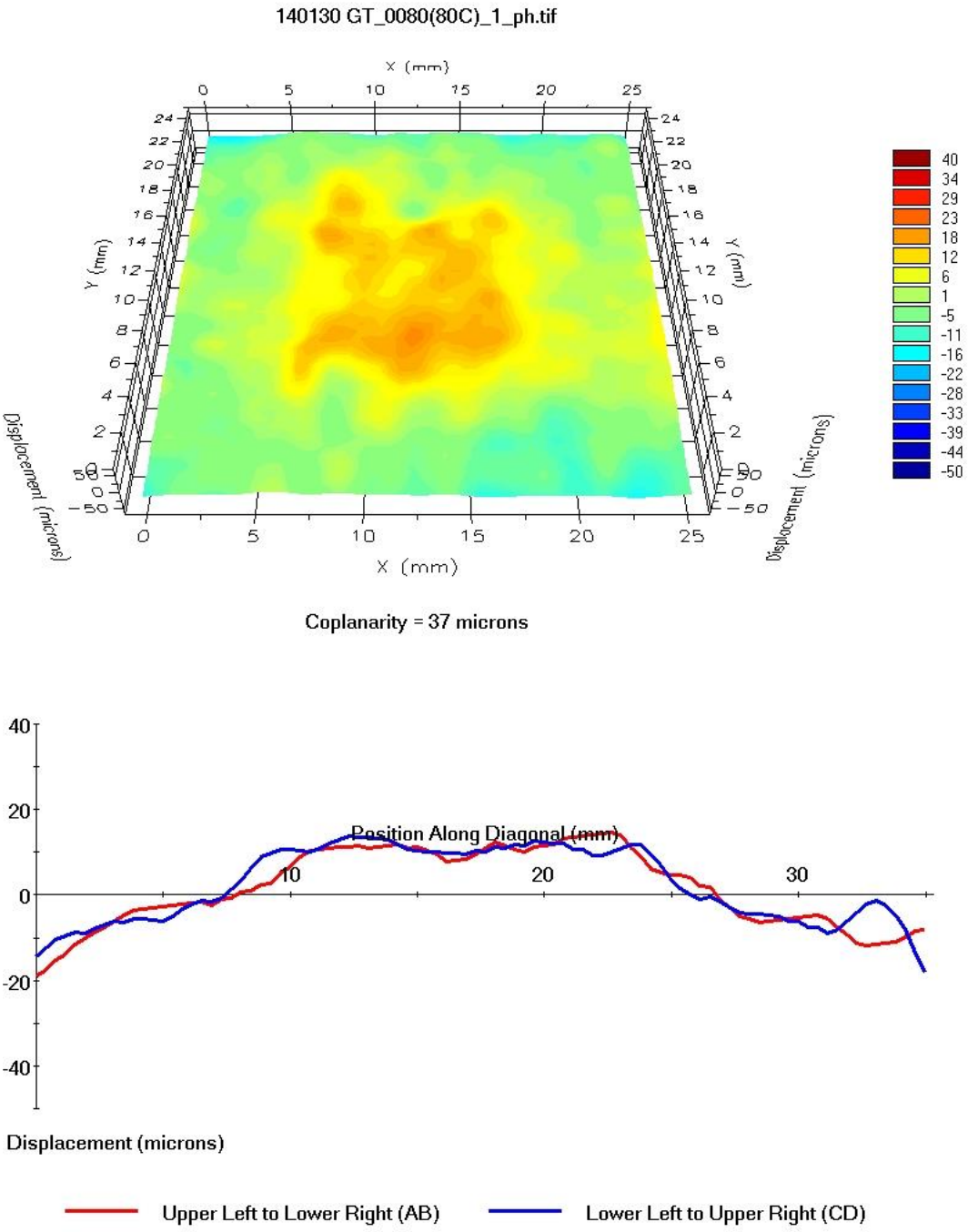


Figure 5.5: Shadow moiré data for 25 mm x 25 mm x 100µm glass with 10 mm x 10 mm x 400µm die (sample #1) at 80 ºC.

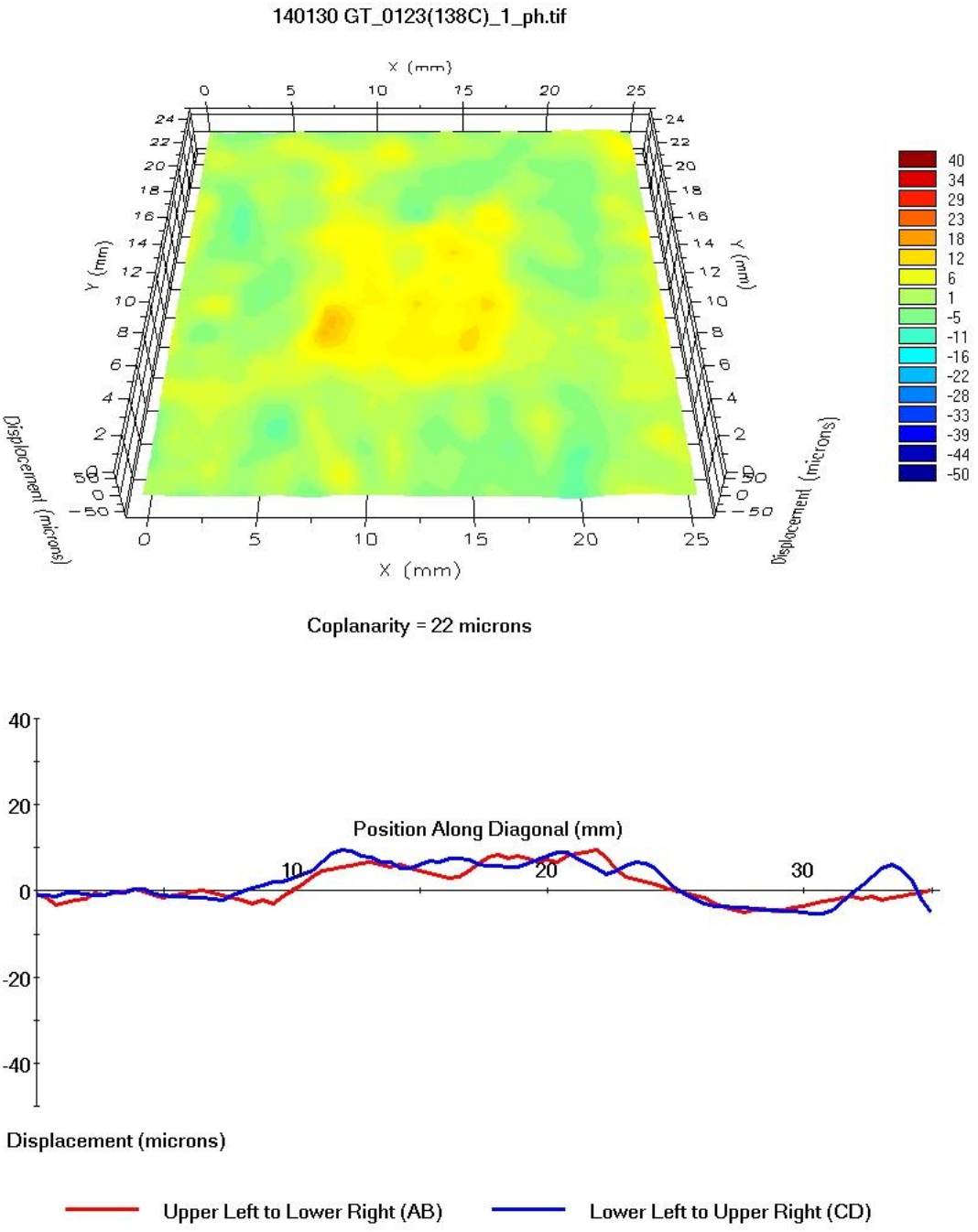


Figure 5.6: Shadow moiré data for 25 mm x 25 mm x 100µm glass with 10 mm x 10 mm x 400µm die (sample #1) at 138 ºC.

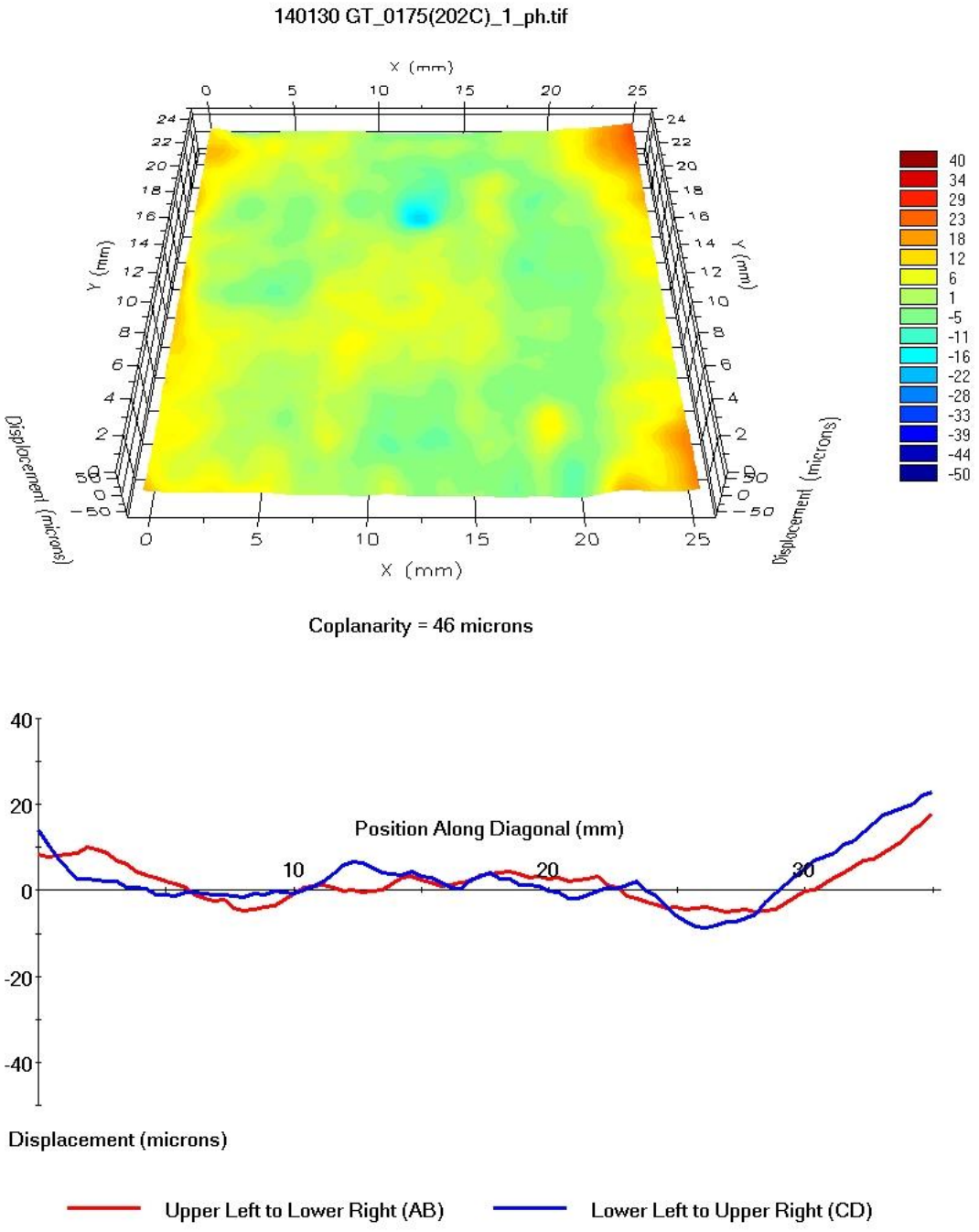


Figure 5.7: Shadow moiré data for 25 mm x 25 mm x 100µm glass with 10 mm x 10 mm x 400µm die (sample #1) at 202 ºC.

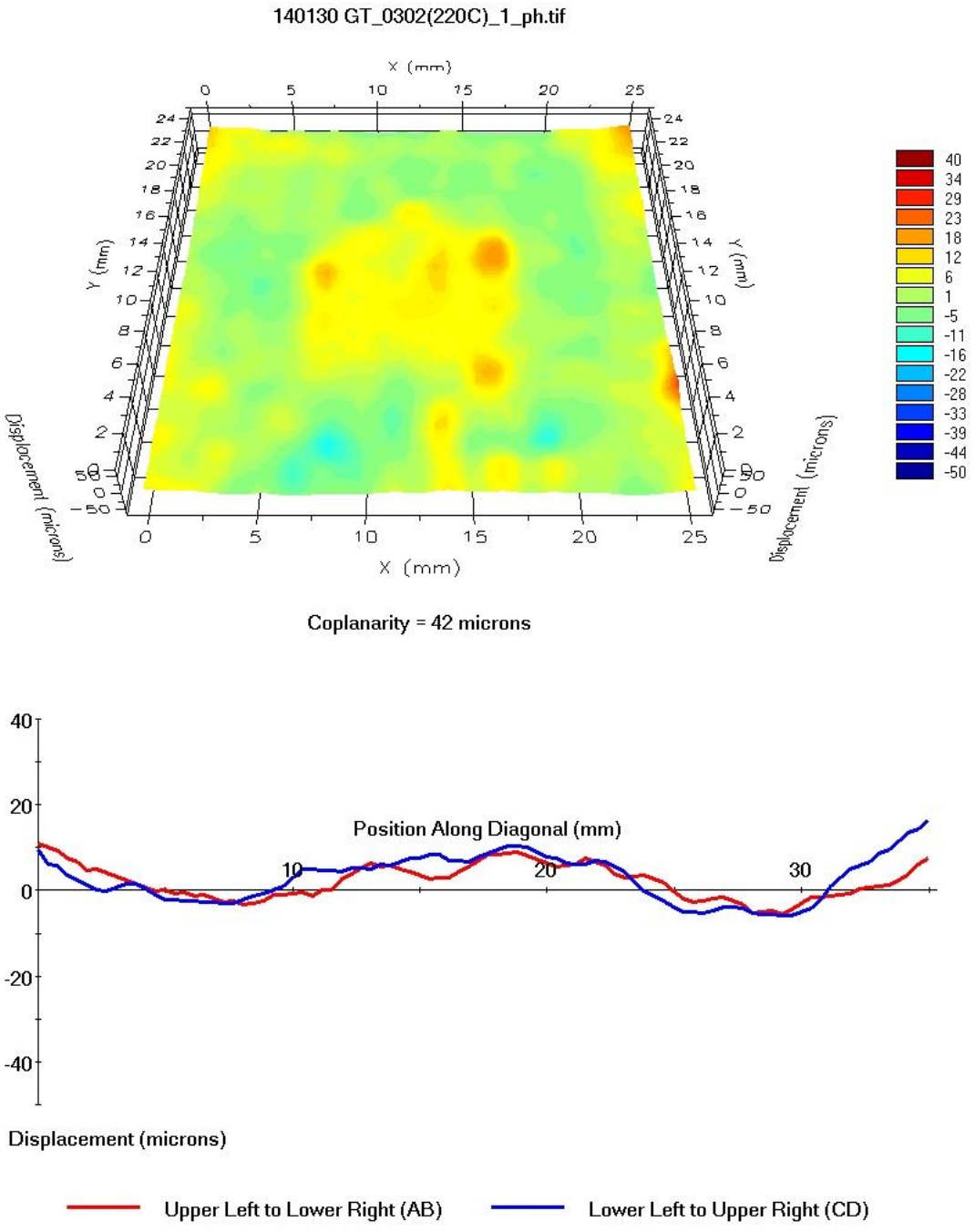


Figure 5.8: Shadow moiré data for 25 mm x 25 mm x 100µm glass with 10 mm x 10 mm x 400µm die (sample #1) at 220 ºC.

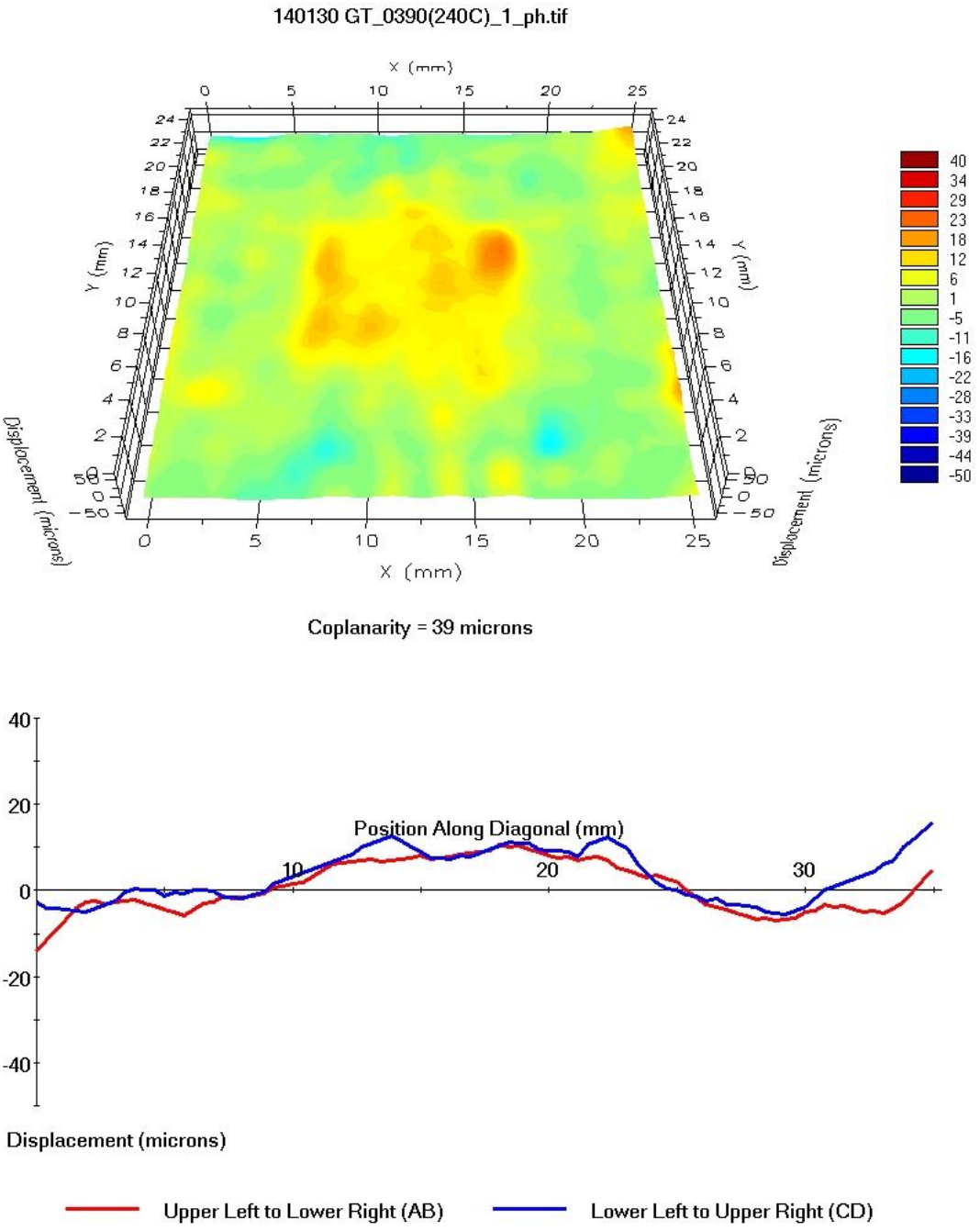


Figure 5.9: Shadow moiré data for 25 mm x 25 mm x 100µm glass with 10 mm x 10 mm x 400µm die (sample #1) at 240 ºC.

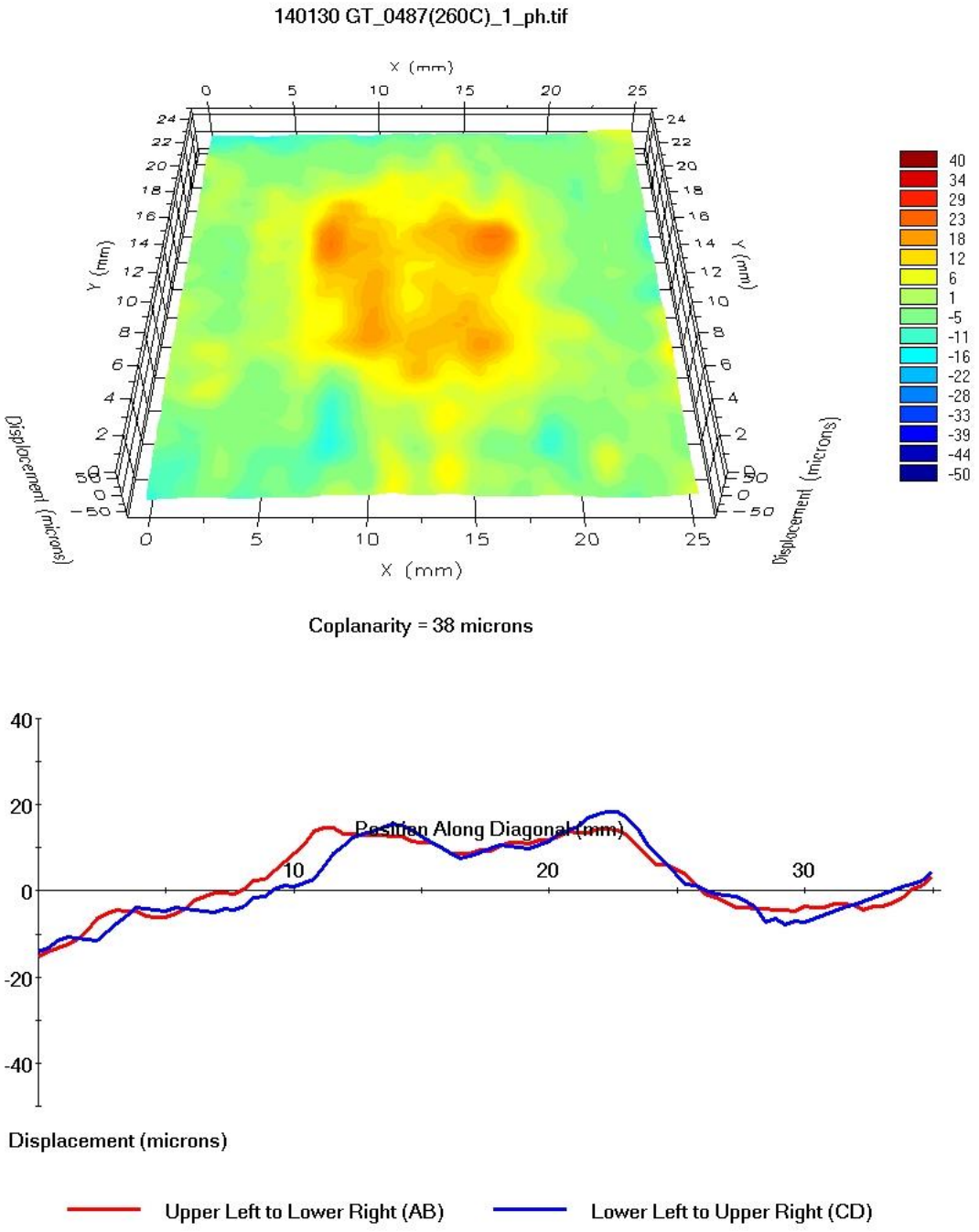


Figure 5.10: Shadow moiré data for 25 mm x 25 mm x 100µm glass with 10 mm x 10 mm x 400µm die at 260 ºC.

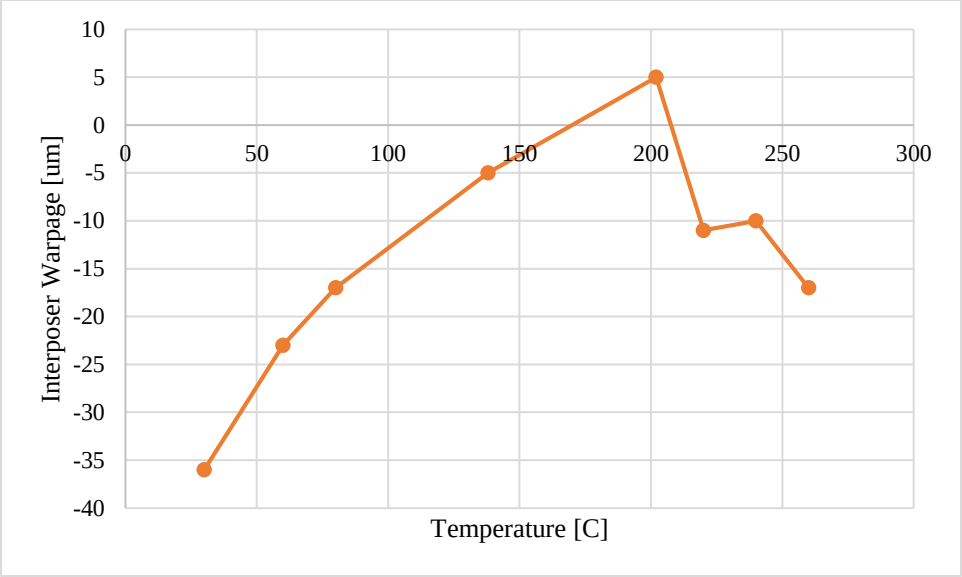


Figure 5.11: Package warpage of 25mm, 100µm glass with 10mm, 400µm die (sample #1) from shadow moiré.

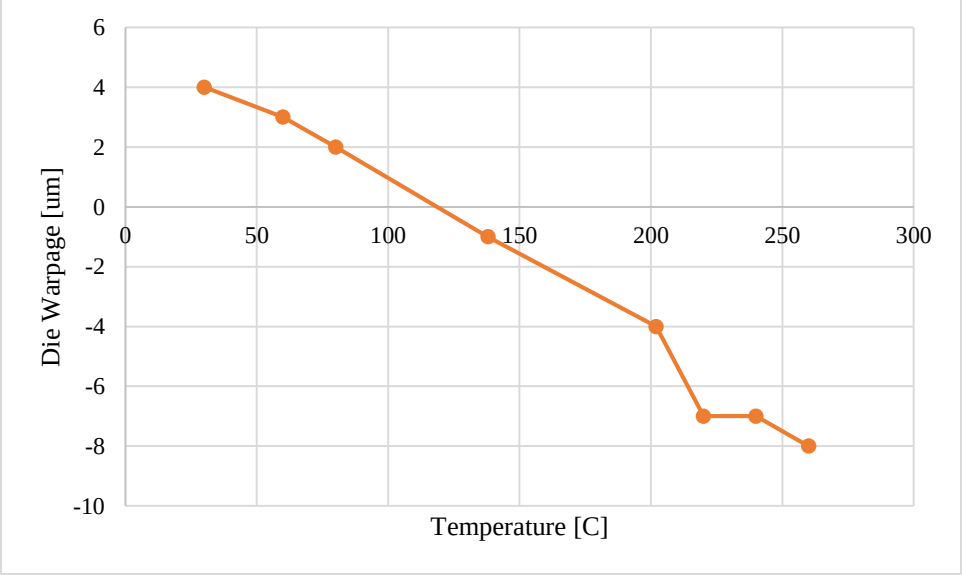


Figure 5.12: Die warpage of 25mm, 100µm glass with 10mm, 400µm die (sample #1) from shadow moiré.

Figure 5.10 shows the shadow moiré images and heights along the two diagonals at 30, 60, 80, 140, 200, 220, 240, and 260 ºC for a 25 mm x 25 mm x 100µm glass with 10 mm x 10 mm x 400µm die (sample #1). This data is aggregated and used to create

Figure 5.11, which shows the package warpage as a function of temperature, and Figure 5.12, which shows the die warpage as a function of temperature. Both of these results are extracted from the same shadow moiré measurement, presented in Figure 5.10; interposer warpage is the difference between the center and the edges of the interposer and die warpage data is the difference between the center and the edges of the die. As seen in the figures, the package has a maximum warpage at room temperature, and this warpage continues to decrease as the temperature is increased toward the stress-free temperature. As discussed in the fabrication section, the stress-free temperature for the lamination process was 160 ºC, the solder assembly was 220 ºC, and for underfill cure was 160 ºC. Therefore, the package, in general, has less warpage at higher temperature than at room temperature. However, it should be pointed out that the exact shape of the package substrate is influenced by various process parameters such as underfill fillet height around the chip, underfill voids and uniformity of underfill in the gap between the die and the interposer, the microbump dimensions and shape after assembly, etc., and thus, variations in the measured warpage behavior can be explained. Also, at temperatures above 220 ºC, the solder is likely to be in molten state, and thus, will not provide rigid coupling between the die and the interposer.

Comparing Figure 5.11 and Figure 5.12, the die and interposer warp in different directions below the stress free temperature. This is because of the underfill fillet. As the underfill has a very large CTE, it shrinks more than the surrounding material, exerting a force that causes the interposer to bend. Chapter 7 provides additional insight into the role of underfill fillet on interposer warpage.

5.3.2 Shadow Moiré Data for 25mm, 300µm Glass with 10mm, 400µm Die (Sample #2)

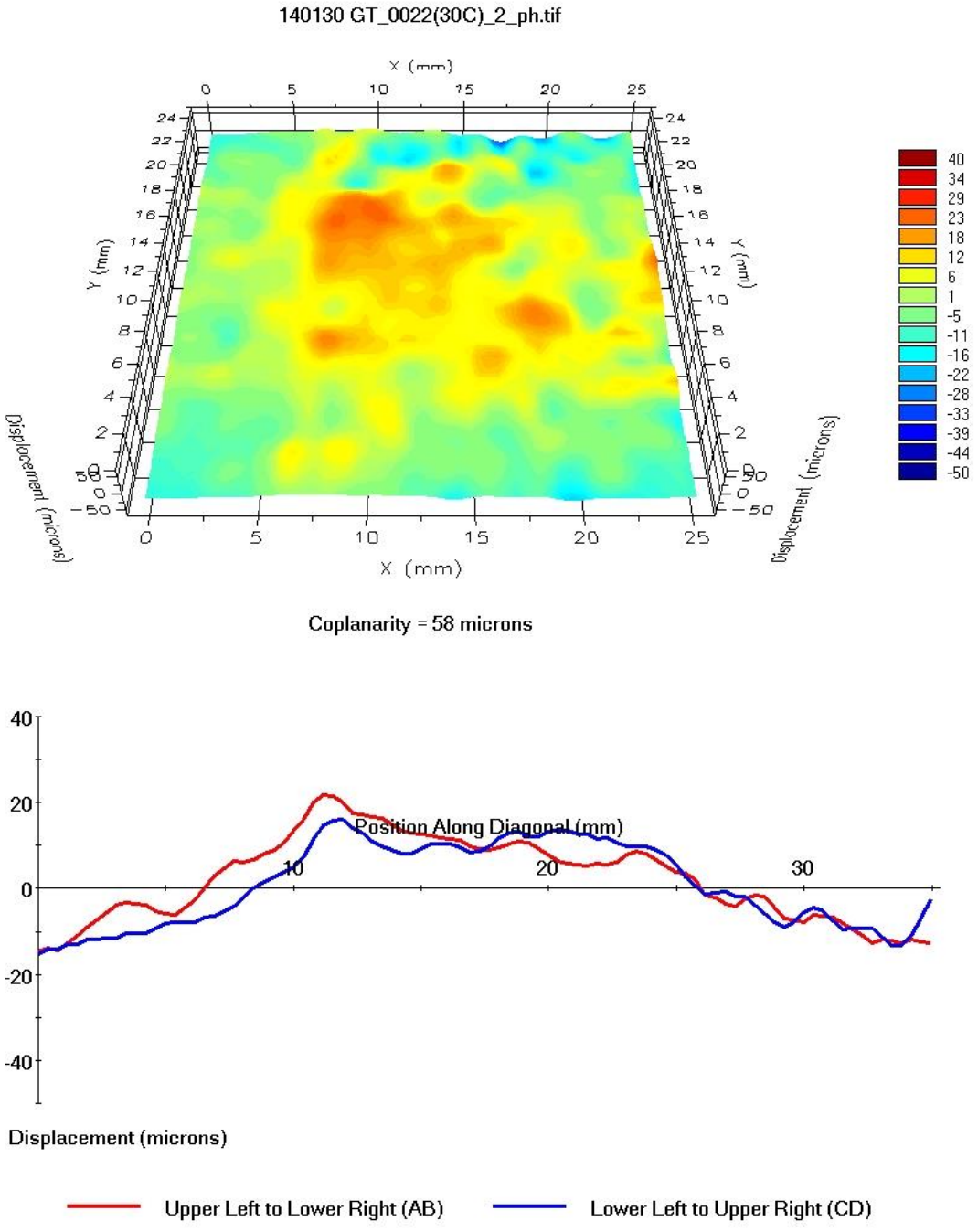


Figure 5.13: Shadow moiré data for 25 mm x 25 mm x 300µm glass with 10 mm x 10 mm x 400µm die (sample #2) at 30 ºC.

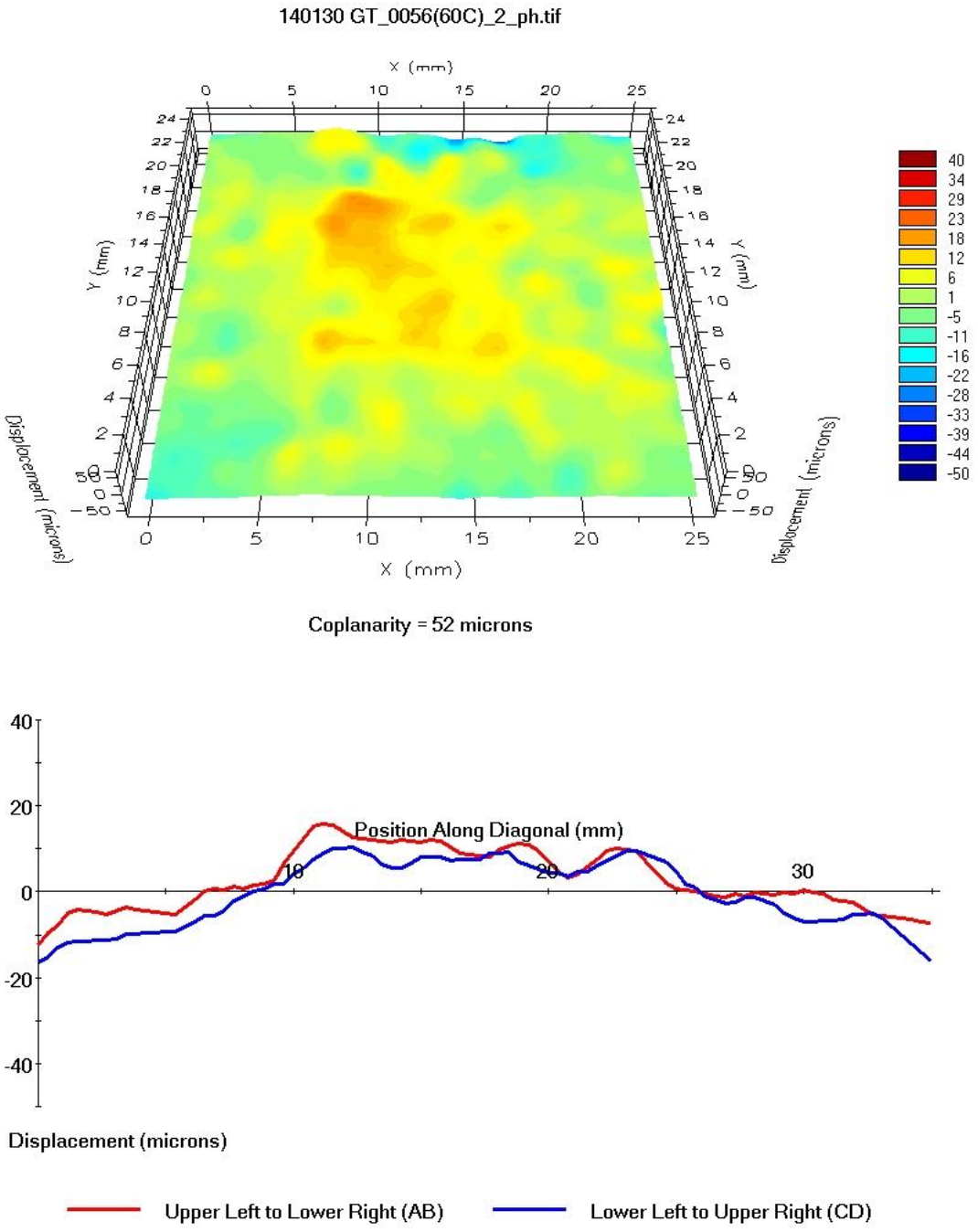


Figure 5.14: Shadow moiré data for 25 mm x 25 mm x 300µm glass with 10 mm x 10 mm x 400µm die (sample #2) at 60 ºC.

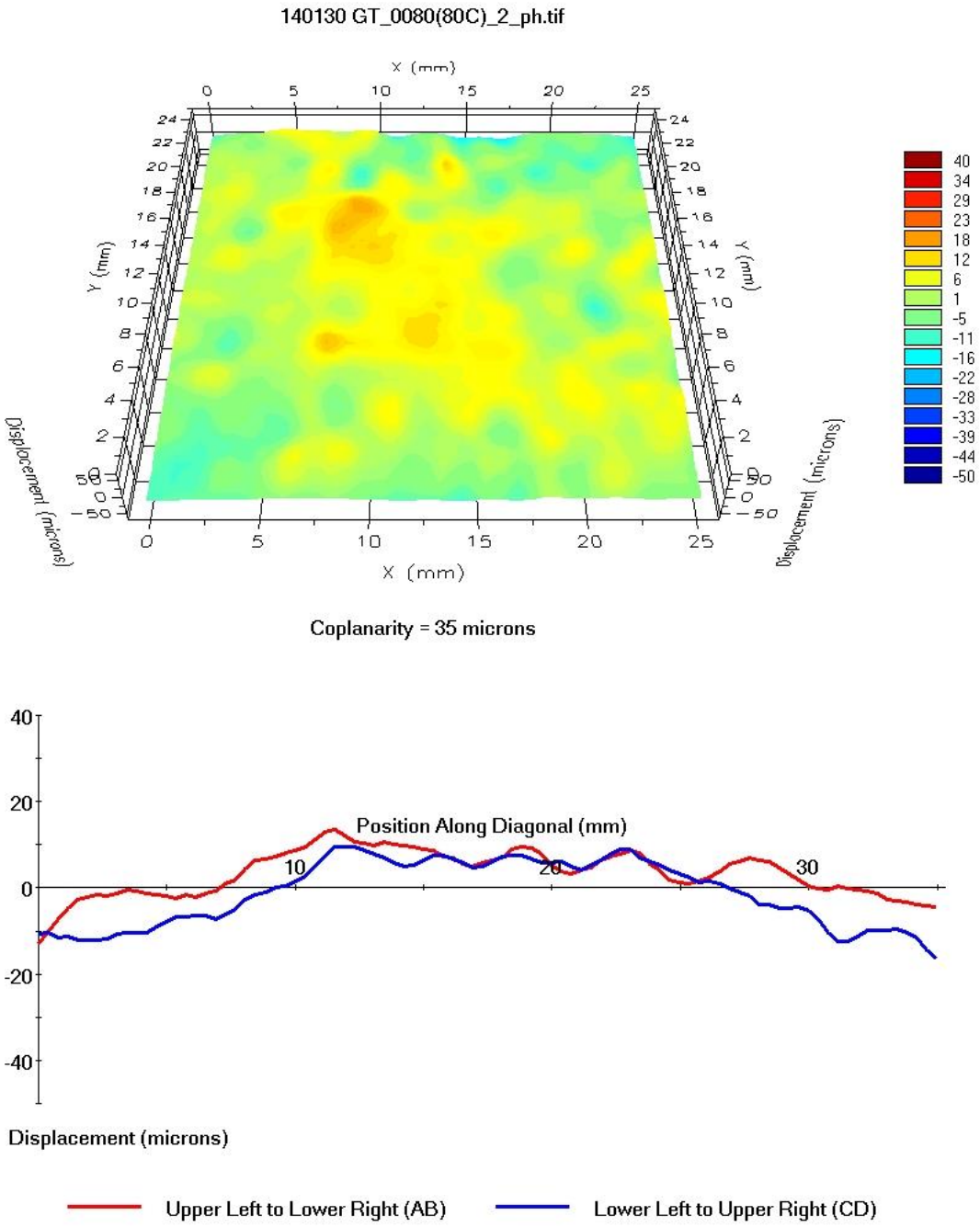


Figure 5.15: Shadow moiré data for 25 mm x 25 mm x 300µm glass with 10 mm x 10 mm x 400µm die (sample #2) at 80 ºC.

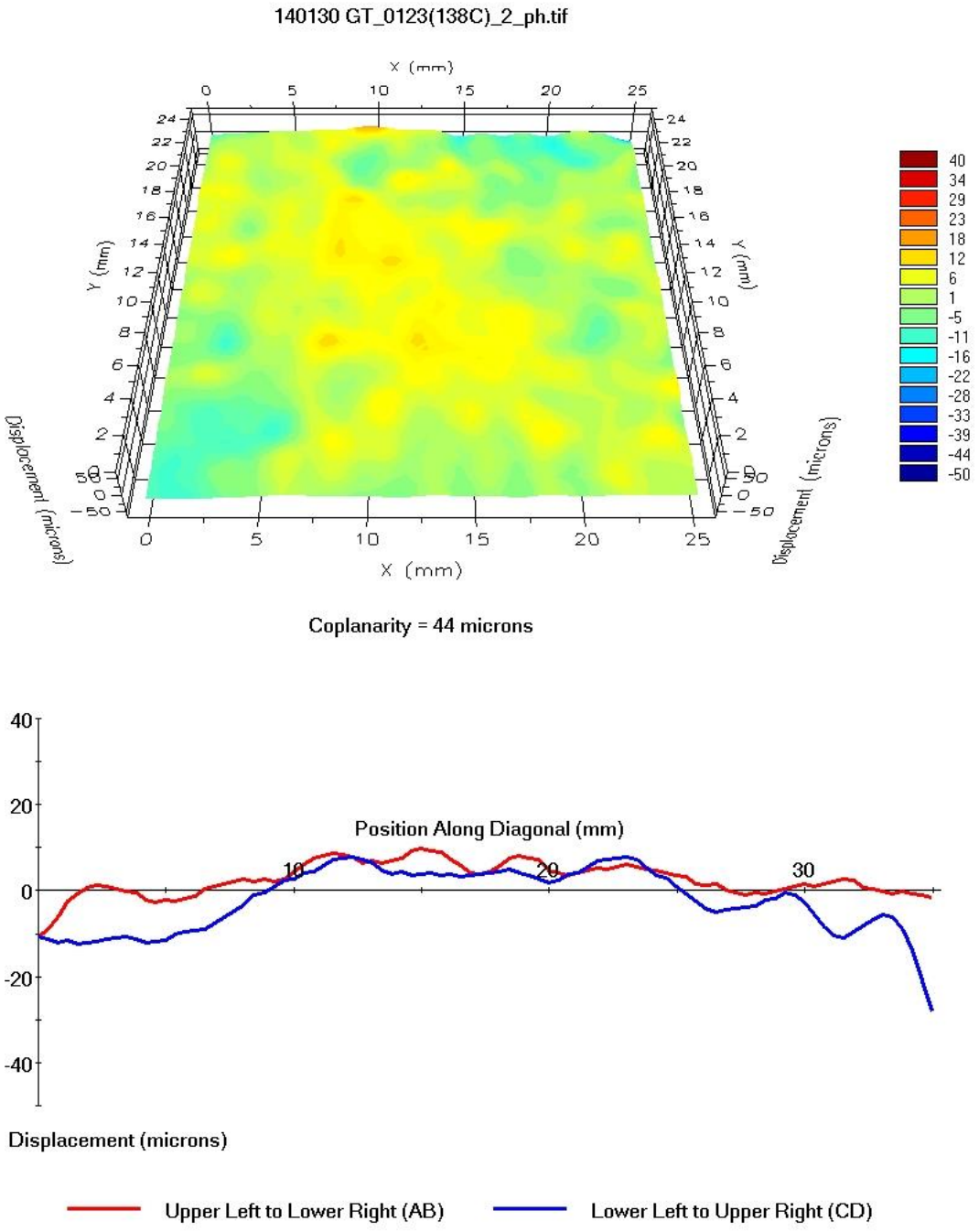


Figure 5.16: Shadow moiré data for 25 mm x 25 mm x 300µm glass with 10 mm x 10 mm x 400µm die (sample #2) at 138 ºC.

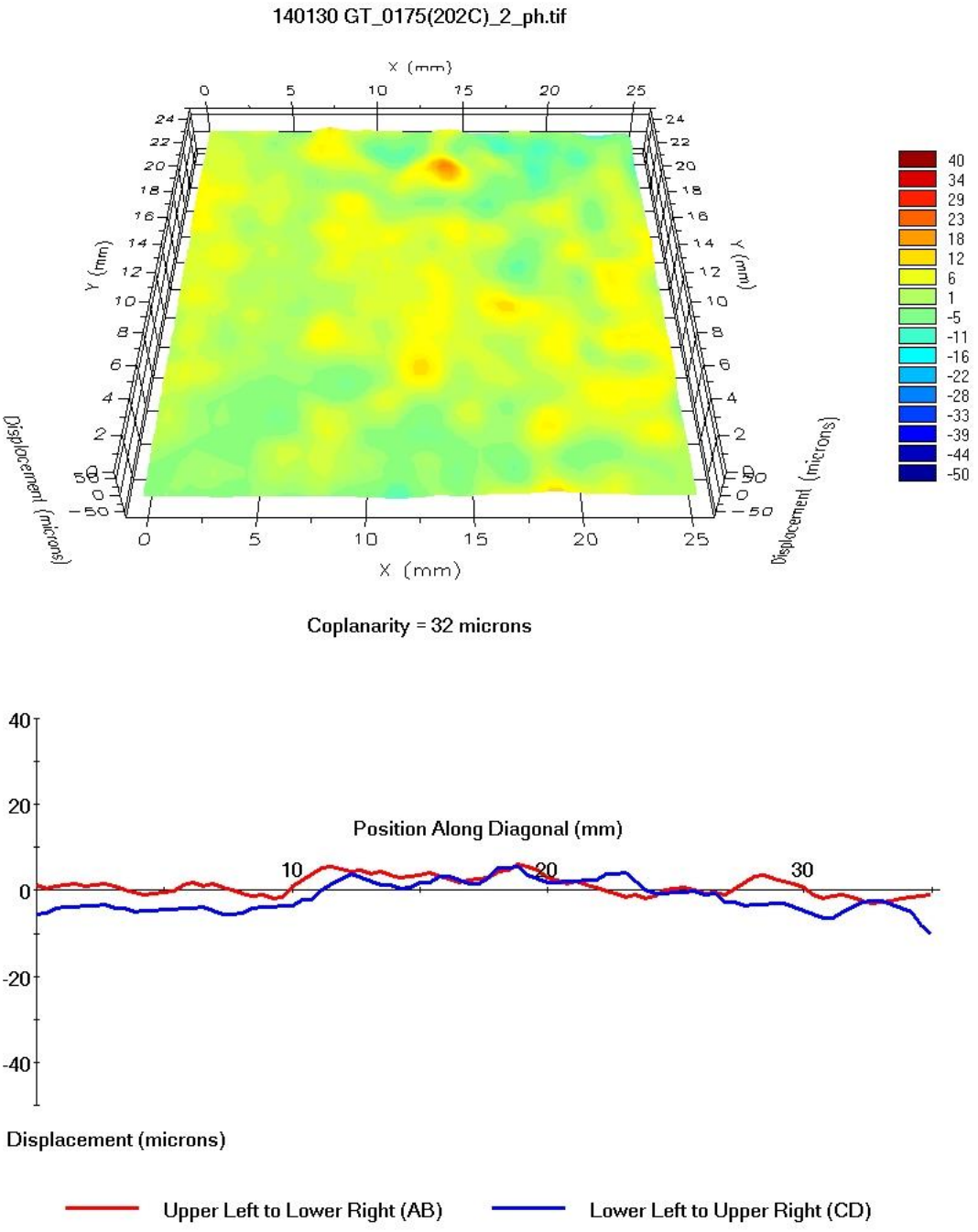


Figure 5.17: Shadow moiré data for 25 mm x 25 mm x 300µm glass with 10 mm x 10 mm x 400µm die (sample #2) at 202 ºC.

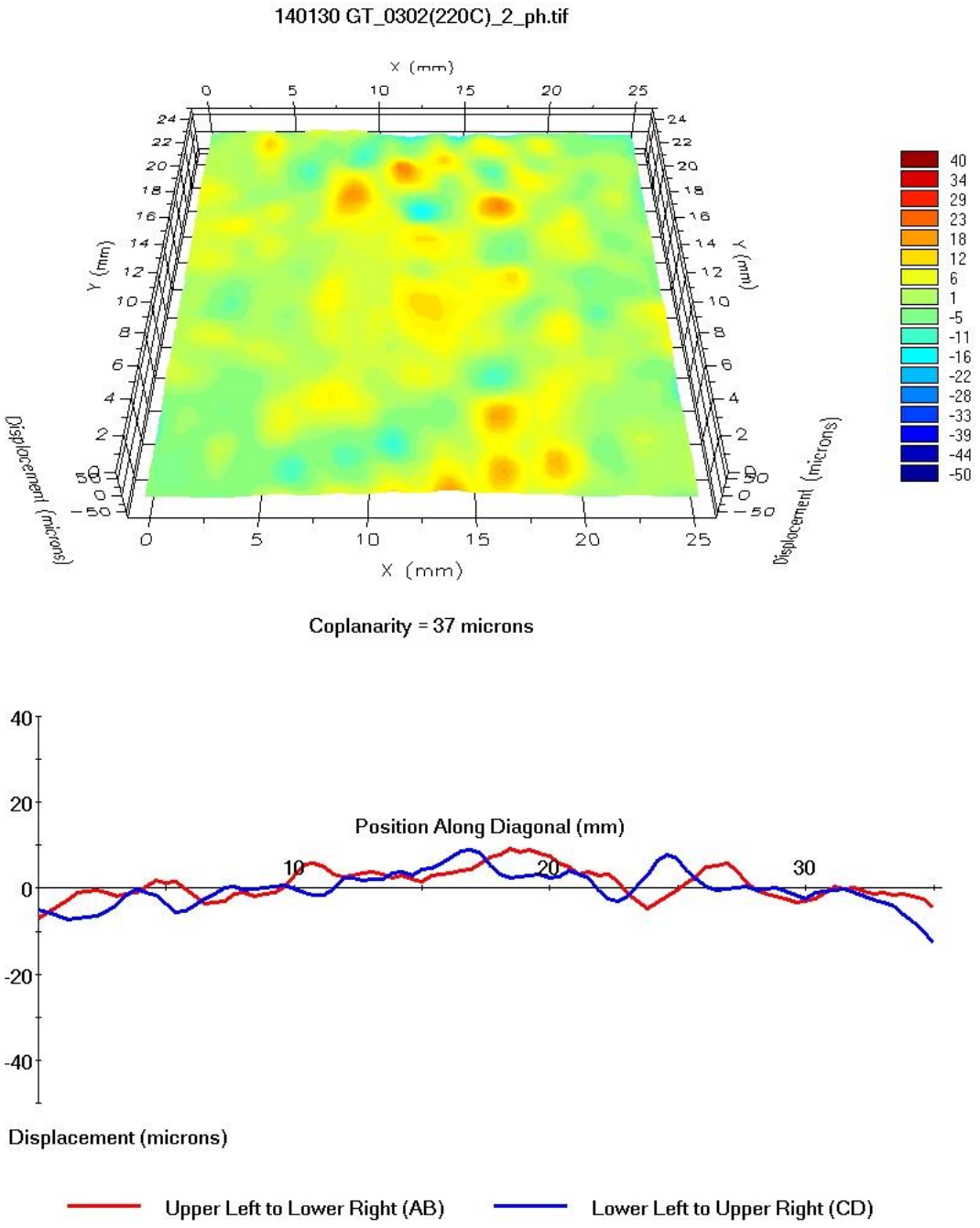


Figure 5.18: Shadow moiré data for 25 mm x 25 mm x 300µm glass with 10 mm x 10 mm x 400µm die (sample #2) at 220 ºC.

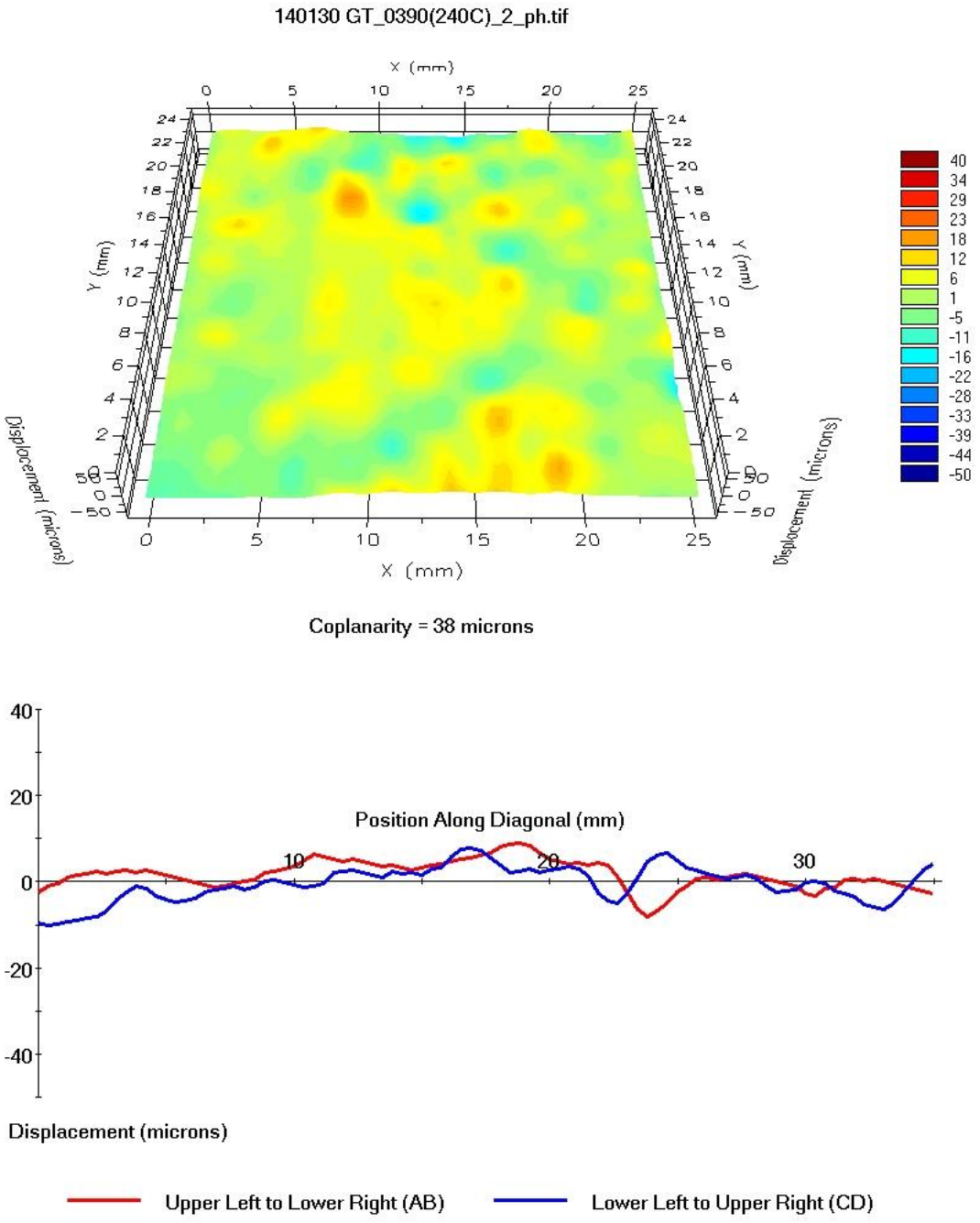


Figure 5.19: Shadow moiré data for 25 mm x 25 mm x 300µm glass with 10 mm x 10 mm x 400µm die (sample #2) at 240 ºC.

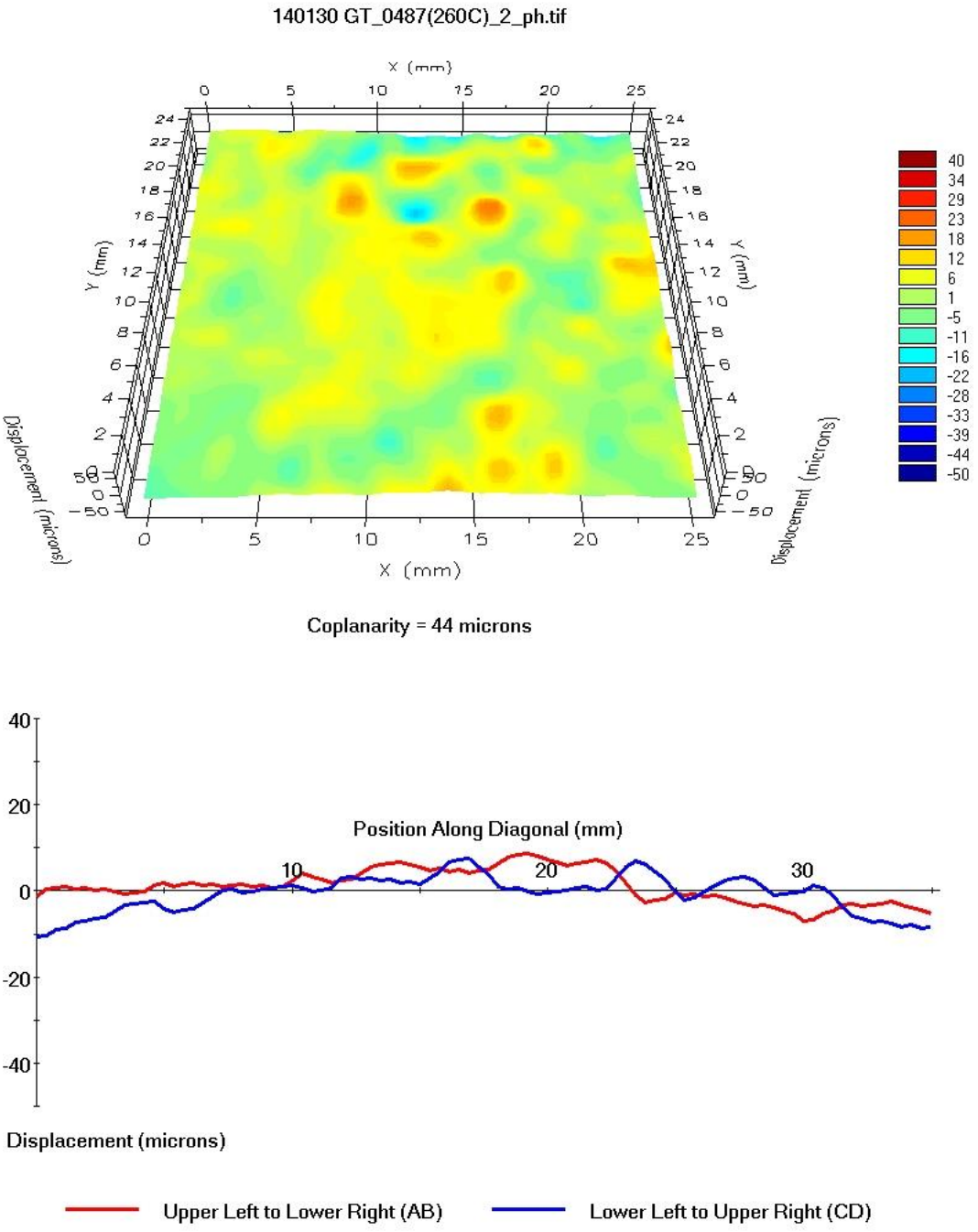


Figure 5.20: Shadow moiré data for 25 mm x 25 mm x 300µm glass with 10 mm x 10 mm x 400µm die (sample #2) at 260 ºC.

Figure 5.21 shows the die warpage as a function of temperature for a 25 mm x 25 mm x 300 µm low CTE glass with a 10 mm x 10 mm x 400 µm die (sample #2). Similar

to the 100 µm glass result presented in Figure 5.12, the warpage started dome like at 30 ºC and decreased with increasing temperature. Near the stress-free temperature of the underfill cure, the warpage is nearly zero. When the temperature was further increased beyond the underfill cure temperature, the die/substrate assembly warped like a bowl with the die being on the top. This was to be expected because upon heating, the glass interposer expands more than the die, and therefore, the assembly takes a bowl shape where the die is present. However, further increase in temperature, especially above 220 °C shows that the structure has a reduced warpage. This could be because of two reasons: first, solder would melt above 220 °C, and therefore, would not offer any stiffness across the standoff height and second, the underfill modulus would be significantly lower because the temperature is much above the glass transition temperature.

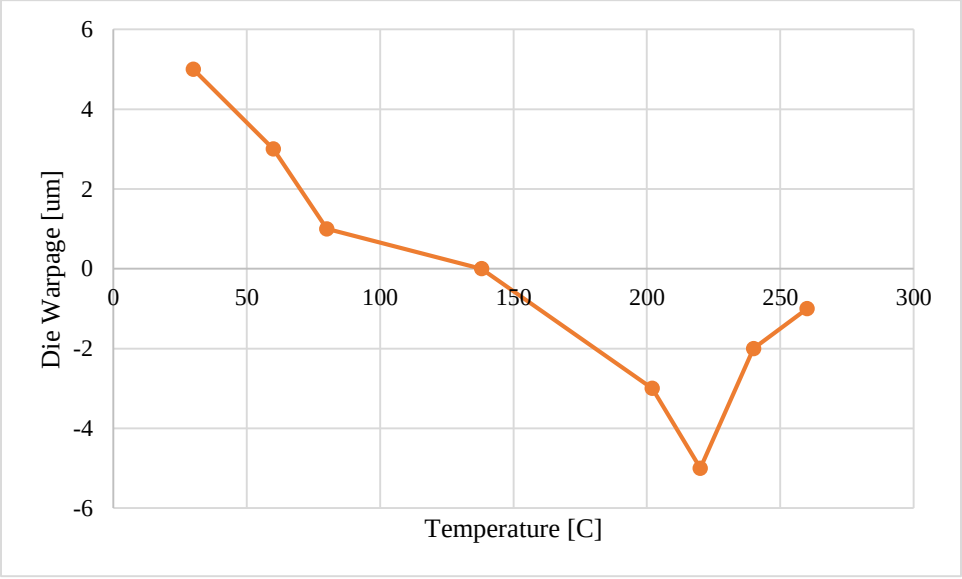


Figure 5.21: Die warpage of 25mm, 300µm glass with 10mm, 400µm die (sample #2) from shadow moiré.

5.3.3 Shadow Moiré Data for 18.4mm, 150µm Glass with 10mm, 200µm Die (Sample #3)

Figure 5.22 illustrates the warpage as a function of temperature for a 10 mm x 10 mm x 200 µm silicon die on 25 mm x 25 mm x 100 µm low CTE glass (sample #3). As with the 100 µm and 300 µm glass with 400 µm die, the 150 µm glass with 200 µm die has the most warpage at 30 ºC and decreases with increasing temperature as the temperature approaches a stress free temperature around 150 ºC. Again, the rate of warpage change as a function of temperature decreases for high temperature.

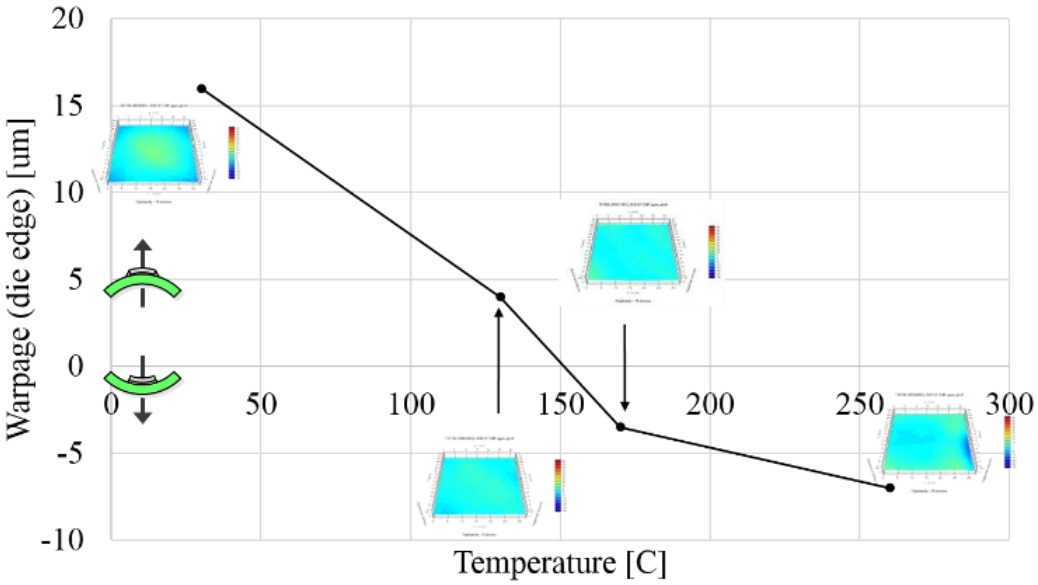


Figure 5.22: Warpage from shadow moiré for 10 mm x 10 mm x 200 µm silicon die on 25 mm x 25 mm x 150 µm glass interposer (sample #3).

CHAPTER 6

PREDICTIVE MODEL FOR GLASS INTERPOSER AND ASSEMBLY WARPAGE

6.1 Geometric Model

In parallel to experiments, finite-element models were created to understand the role of substrate properties and assembly processes on warpage. The modeling was done parametrically in ANSYS™, using plane-strain approximation and with 2.5D strip models.

6.1.4 2D Plane-Strain Model

Although 2.5D or 3D models are desirable to account for property and geometry variations in the third dimension, 2D models are appropriate for comparison between different cases. Figure 6.1a shows a schematic of the plane-strain model for an interposer; the model captures the glass substrate, the polymer layers, copper redistribution layers, solder interconnects, underfill, and silicon die. The *x* direction is used as the in-plane direction and the *y* direction is used as the out-of-plane direction. The model is half symmetric, with symmetry boundary conditions at the left side. One node at left bottom is fixed in *y* direction to prevent rigid body motion. The fixed node is within the glass, as the glass is present from the beginning of fabrication, which is important for process modeling.

The primary concerns when meshing are the solder strain and the number of vertical elements in a material layer. First, the solder mesh is important to capture strain and make accurate fatigue life predictions. Compared to the size of the solder joint, the

package is up to 3000 times larger, mandating a sufficient number of elements in the in plane direction. Second, for linear quadrilateral and triangular plane-strain elements, three elements are required in the out of plane direction to accurately model the displacements. Further away from critical regions, such as in the silicon and glass, the mesh is less fine. The element count used for most 2D models is about 230,000.

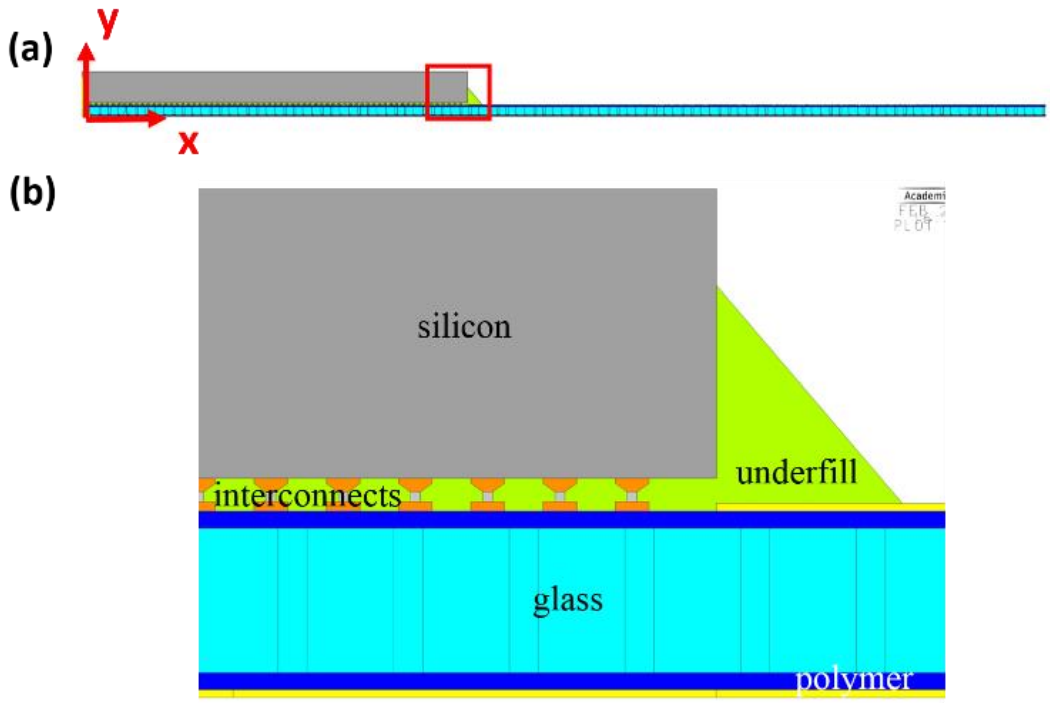


Figure 6.1: (a) Plane-strain model showing all modeled components; (b) zoomed-in image of boxed area from (a).

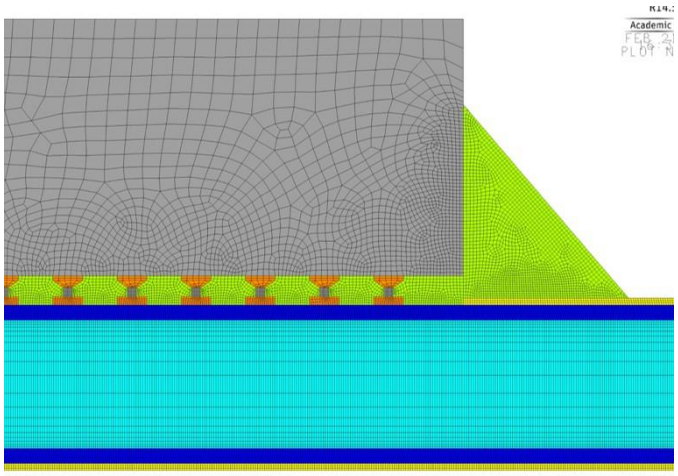


Figure 6.2: Mesh of plane-strain model from Figure 6.1(b).

6.1.5 2.5D Model

In addition to the plane-strain models, 2.5D models are created, as illustrated in Figure 6.3. Consistent with the plane-strain model, *x* is in-plane and *y* is out-of-plane, while *z* has been added in-plane. The model captures all elements present in the plane-strain model, namely, the glass substrate, the polymer layers, copper redistribution layers, solder interconnects, underfill, and silicon die. A zoomed-in image of the mesh for the 2.5D model is shown in Figure 6.4; underfill is not shown in the figure so the interconnects can be seen. The 2.5D model is one pitch wide, allowing it to capture properties and geometry variations in the third dimension. Unlike a full 3D model, a 2.5D model takes less computational time. Similar to the plane-strain model, half symmetry is employed, and symmetry boundary conditions are applied on the left. Again, one node is constrained in *y* direction to prevent rigid body motion. All nodes on the front and the rear face (as seen in Figure 6.4) are coupled in *z* direction so that the *z* displacements are uniform for all nodes on those faces. Compared to the 2D model which has about 230,000 linear plane elements and two degrees of freedom per node, the 2.5D model has about 1.1 million linear solid elements and three degrees of freedom per node.

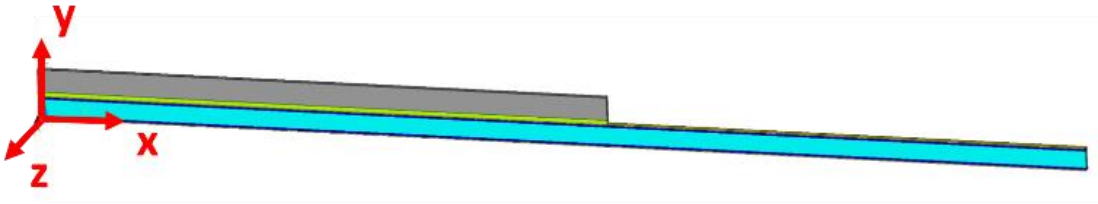


Figure 6.3: 2.5D model.

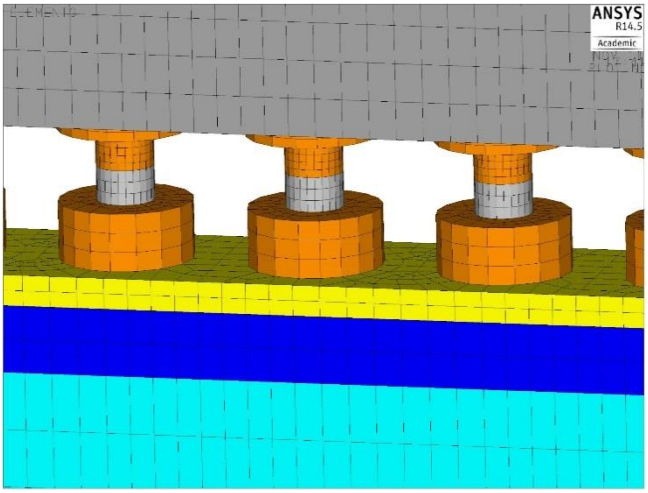


Figure 6.4: Example mesh from 2.5D model.

The meshes shown in Figure 6.2 and Figure 6.4 are example meshes, and multiple mesh densities were used to ensure that the results converged.

6.2 Material Model and Stress-Free Temperatures

The fabrication and assembly process includes many temperatures over various lengths of time. To model these, it is important to understand the mechanics of the materials and how the materials are modeled.

Material properties used in the models are given in Table 6.1, Table 6.2, and Table 6.3. Table 6.1 shows the thermo-mechanical material properties and includes the stress-free temperature for various materials, based on fabrication process steps.

Materials are given a stress-free temperature based on when they are added to the package during fabrication, as discussed in 6.3 Process Modeling: Material Birth and Death.

Silicon is directionally dependent based on crystal orientation and standard processing, with the in-plane modulus being higher than the out-of-plane modulus or [100] direction [13]. The stress free temperature for silicon is different based on the application; the silicon die is viewed as stress free during the solder reflow, while the silicon interposer is stress free during dielectric build-up. Underfill CTE varies from 25 to 65 for different compounds. Properties for the polymer, ZEONIF^{TM} ZS-100, were obtained from the manufacturer, Zeon Corporation. The values for an organic substrate represent a homogenized material [14].

The properties shown in Table 6.1 for low CTE glass represent the published properties for Asahi Glass Co., Ltd.'s EN-A1 glass, which was throughout this work. When measured with a three point bend, a modulus of 96 GPa was obtained. While this value is 25 percent larger than the published value, the effect on the warpage results changes by less than two percent. This work uses the published value for consistency.

Table 6.2 shows the temperature-dependent material properties for electroplated copper, which has a lower modulus than bulk copper [37]. These values are lower than for bulk copper and decrease with increasing temperature.

A viscoplastic model of solder is required to accurately model the change in deformation and to later predict fatigue life. The flow equation for inelastic strain is

$$\dot{\varepsilon}^{pl} = \dot{\bar{\varepsilon}}^{pl}\left(\frac{3}{2}\frac{S_{ij}}{\bar{\sigma}}\right) \qquad \textbf{(6.1)}$$

where $\dot{\varepsilon}^{pl}$ is the rate of equivalent plastic strain accumulation, S_{ij} is the deviatoric stress, and $\bar{\sigma}$ is the equivalent stress. The rate of accumulated equivalent plastic strain is defined as

$$\dot{\varepsilon}^{pl} = \sqrt{\frac{2}{3}\dot{\varepsilon}^{pl}\dot{\varepsilon}^{pl}} \qquad \textbf{(6.2)}$$

Using the Anand model, the equivalent plastic strain rate can also be written

$$\dot{\varepsilon}^{pl} = Aexp\left(-\frac{Q}{RT}\right)\left\{sinh\left(\xi\frac{\bar{\sigma}}{s}\right)\right\}^{\frac{1}{m}} \qquad \textbf{(6.3)}$$

where Q is activation energy, R is the universal gas constant, T is absolute temperature, s is an internal state variable, and A, ξ, and m are material constants. The rate of evolution is controlled by

$$\dot{s} = \oplus h_0\left|1 - \frac{s}{s^*}\right|^a \dot{\varepsilon}^{pl} \qquad \textbf{(6.4)}$$

where $\oplus$ is +1 if s is less than or equal to s* or -1 if s is greater than s* and s*, the deformation resistance saturation, is defined as

$$s^* = \hat{s}\left\{\frac{\dot{\varepsilon}^{pl}}{A}\exp(\frac{Q}{RT})\right\}^n \qquad \textbf{(6.5)}$$

where ŝ and n are material constants [22]. Based on [23], Anand's model for 96.5-tin 3.5-silver solder uses the properties found in Table 6.1 and Table 6.3, which presents Anand's viscoplastic model parameters for 96.5 Sn-3.5 Ag solder.

Table 6.1: Isotropic, temperature-independent material properties.

Material	E [GPa]	CTE [ppm/ºC]	N	Stress Free Temp. [C]
Silicon chip	$E_{x,z}$ = 169 E_y = 130	2.6	0.28	220
96.5Sn-3.5Ag Solder	58	24	0.4	220
Underfill	3	50	0.4	160
Low CTE Glass	77	3.8	0.22	160
Copper	--	17	0.33	40
Polymer	6.9	31	0.3	160
Organic Substrate	20	20	0.14	160
Silicon Interposer	$E_{x,z}$ = 169 E_y = 130	2.6	0.28	160

Table 6.2: Temperature dependence of copper modulus [37].

Temperature [ºC]	0	100	140	150	160	170	180	220	260
E [GPa]	80	72	68.8	68	67.2	66.4	65.6	62.4	59.2

Table 6.3: Coefficients for Anand's viscoplastic model of tin silver solder [23].

Coefficient	Value
A [s^{-1}]	$2.23(10^6)$
Q/R [K]	8900
ξ	6
m	0.182
$\hat{s}$ [MPa]	73.81
n	0.018
h_0 [MPa]	3321.15
a	1.82
s_0 [MPa]	39.09

6.3 Process Modeling: Material Birth and Death

To mimic the actual fabrication process, element "birth" and "death" are used in the simulation model. At the beginning of process simulation, only the glass interposer is present, as shown in Figure 4.1. Therefore, the simulation starts with "birthing" the glass panel, and "killing" all other layers or materials. Such a "killing" or death means that the material layers are actually present in the model, however, with a modulus of

elasticity that is several orders of magnitude less than other "birthed" materials. In the simulation, the killed elements have a modulus of elasticity reduced by a factor of 10^6.

The dry polymer film is laminated on both sides of the glass interposer and cured at 160 ºC. Thus, the process model activates or births the polymer film at 160 ºC, and the current modulus of the polymer film is the actual modulus of the film at 160 ºC. The entire model is then simulated to be cooled down to room temperature. The model warpage is minimal, as the polymer is laminated on both sides.

Subsequently, copper is electroplated on both sides of the interposer at 40 °C and then patterned to create the pads and traces. Therefore, copper elements in the model are activated at 40 °C. The palladium surface finish is not simulated. This is because the palladium is 300 nm thick that is several orders of magnitude less than copper pads as well as the substrate in thickness. Thus, the presence of palladium is not likely to influence the warpage results.

The interposer is then heated for reflow assembly of the flip chip, and the chip, solder, and chip pads are "birthed" at the solder melting temperature of 220 °C, and the entire assembly is cooled to 160 °C at which the underfill is "birthed," and then the entire assembly is cooled to room temperature. Although in reality, the assembly is cooled to room temperature followed by heating to underfill dispensing and cure, the models do not include such a cooling and heating step. This is because literature [38] shows that the results are nearly the same between the two modeling approaches, except that the approach used here is computationally less time consuming.

Figure 6.5 illustrates this concept, that the temperature is raised and lowered through fabrication and assembly; full details are shown in Table 6.4. If a material model

does not include time dependent properties, then a single time step solution is identical to several time steps. In the process modeling, no alive materials have time dependent properties until solder is birthed. Thus, all solution steps prior to assembly are given a time step of 1.

Table 6.4: Sequential fabrication process temperatures.

Description	Material(s) Added	Temperature [ºC]
Start	Glass	RT
Add ZIF	ZIF	160
Cool	--	RT
Deposit copper	Copper	40
Cool	--	RT
Assembly	Solder and Silicon Die	220

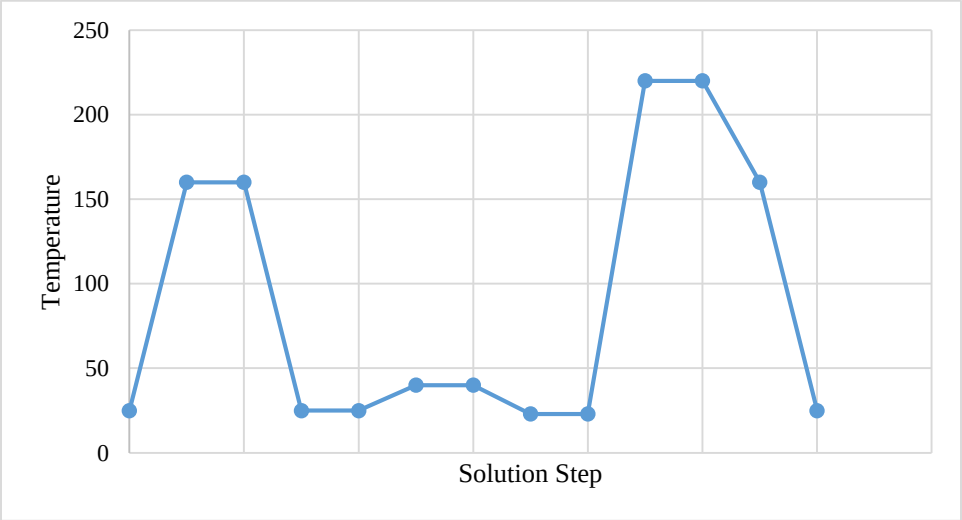


Figure 6.5: Example of fabrication and assembly process temperatures.

6.4 Predicted Warpage and Validation

All warpage modeling results are shown for die edge center, as illustrated with the red highlight in Figure 6.6. Consequently, all validation is from edge data. The warpage is influenced significantly by underfill fillet, and along a die edge, there is a continuous fillet that influences the interposer warpage. This fillet can be adequately captured

through plane-strain approximation. On the other hand, the corner warpage is influenced by the fillets on both edges of the corner as well as the corner fillet itself, and therefore, it is difficult to capture through one cross-section model. Thus, warpage along the edge are simulated and compared against experimental data.

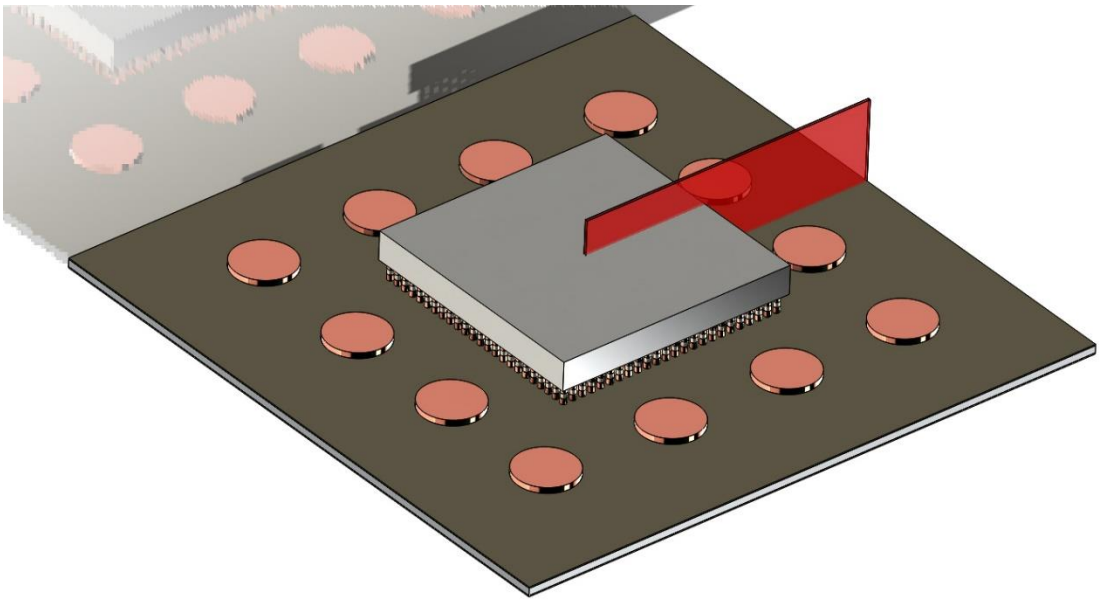


Figure 6.6: "Edge" cross section of package used for warpage modeling.

The finite element models build are validated with the glass interposers fabricated. Examples of this validation depicted in Figure 7.1, Figure 6.7, Figure 6.8, and Figure 6.9, which shows temperature model comparison with the shadow moiré data.

Figure 6.7 compares the predictive model and the experimental results for a 25 mm x 25 mm x 100 µm glass interposer with 10 mm x 10 mm x 100 µm die. As seen, the simulated results track the experimental data. Both experimental results show similar warpage near 25 ºC. The model captures the decrease in warpage as a function of temperature. The slope of the line corresponds to the CTE mismatch for a given

geometry. The stress free temperature, where the package is flat, is near the underfill cure temperature.

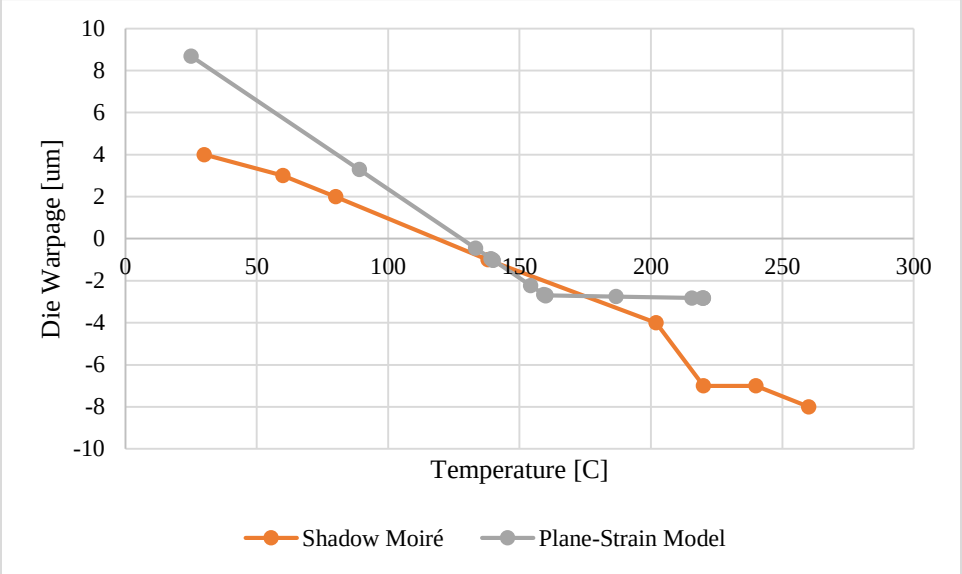


Figure 6.7: Predictive model validation (die) for 25mm, 100µm glass with 10mm, 400µm die (sample #1).

Figure 6.8 compares the predictive model and the experimental results for a 25 mm x 25 mm x 300 µm glass interposer with 10 mm x 10 mm x 100 µm die. The shadow moiré experimental data are the green squares, and the plane-strain model predictions are red triangles.

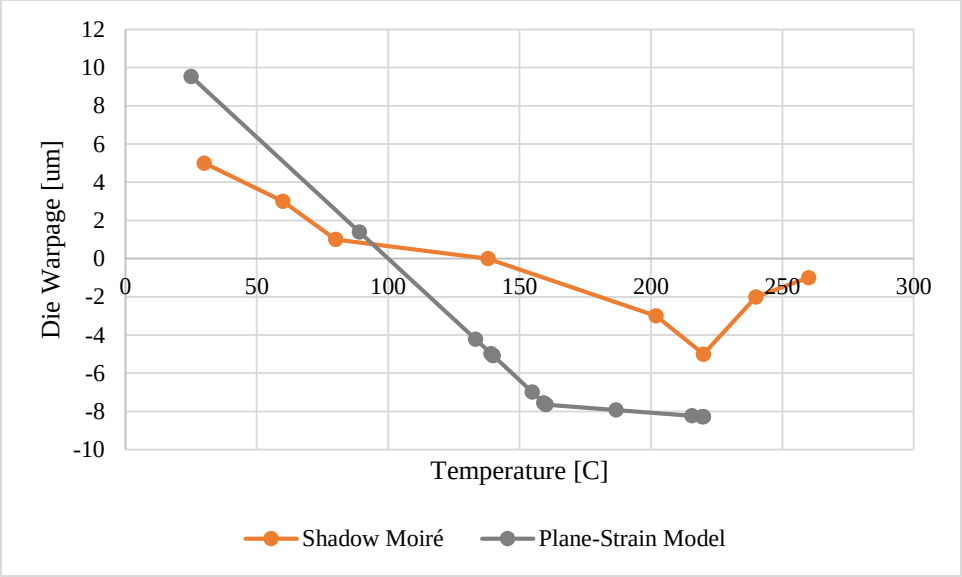


Figure 6.8: Predictive model validation for 25mm, 300µm glass with 10mm, 400µm die (sample #2).

In Figure 6.9, die warpage at the middle of the edge is compared for a 25 mm x 25 mm x 150 µm low CTE glass interposer with 10 mm x 10 mm x 200 µm die. This plot compares the 2D as well as 2.5D results against experimental data. The shadow moiré data is plotted in black, the plane-strain model is plotted in gray, and the 2.5D model is plotted in orange. Both models capture the 30 ºC warpage well. The models capture the decrease in warpage as a function of temperature well, though the 2.5D model captures it better until approximately 160 ºC. Beyond this temperature, both models are offset from the experimental results by approximately two microns. Neither model goes above 220 ºC because the solder changes states, which is only represented as a softening in the material model.

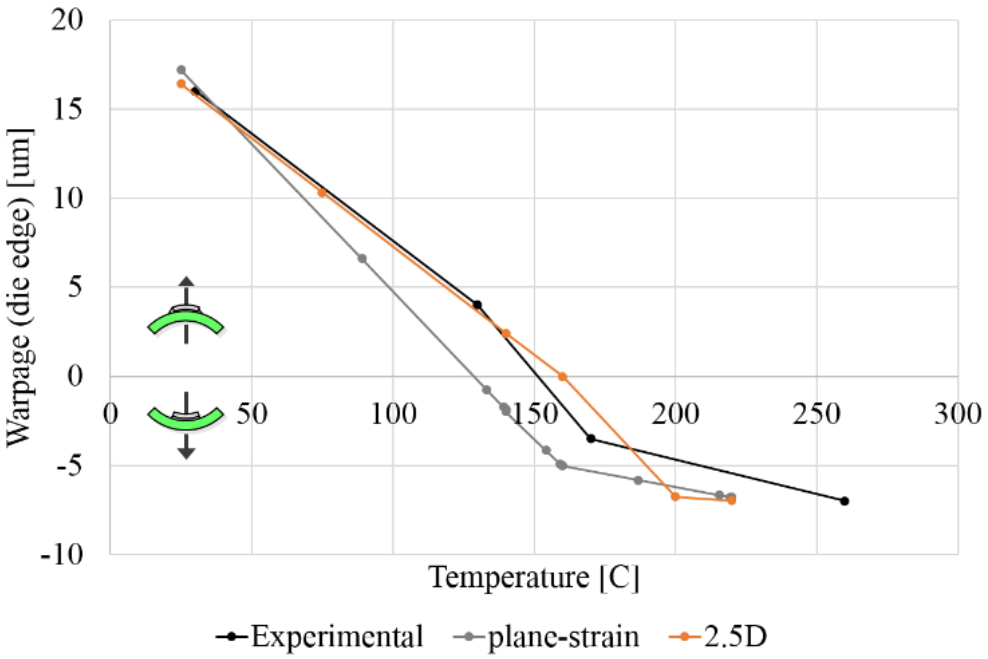


Figure 6.9: Predictive model validation for 18.4mm, 150µm glass with 10mm, 200µm die (sample #3).

CHAPTER 7

ROLE OF UNDERFILL FILLET ON INTERPOSER WARPAGE

This chapter investigates the effect of underfill fillet on warpage for glass interposer package over a range of temperatures. During underfill dispensing, underfill fillet is controlled by the amount of underfill dispensed, the viscosity and surface tension of the underfill, the thickness and size of the die, the standoff height, and other parameters. Therefore, the control of underfill fillet size is usually achieved through several trials. In addition to underfill fillet, complete flow of the underfill under the die without any void is another important item that is considered during underfill dispensing. In this chapter, only the effect of underfill fillet on interposer warpage is considered.

7.1 Interposer Warpage Prediction and Validation

Figure 7.1 shows the interposer warpage as a function of temperature for a 25 mm x 25 mm x 100 µm glass interposer with a 10 mm x 10 mm x 400 µm die (sample #1). At 25 ºC, the model predicts a shape that is dome-like where the die is and bowl-like beyond the die region.

As seen, the simulations show a monotonic trend in the warpage of the substrate with temperature. The warpage is minimum near the underfill cure temperature. This is to be expected because the large structures in the assembly, namely the die and the substrate, are tightly bonded together by the underfill at the underfill cure temperature, and thus the underfill cure temperature is near the stress-free temperature for the assembly.

At temperatures above 200 °C, the experimental results show that the warpage changes the monotonic trend. This is due to potential decoupling of the die from the interposer due to extreme softening of underfill and dielectric polymer as well as softening and potential melting of solder. Such trends are not adequately captured in the model due to lack of material data at these high temperatures.

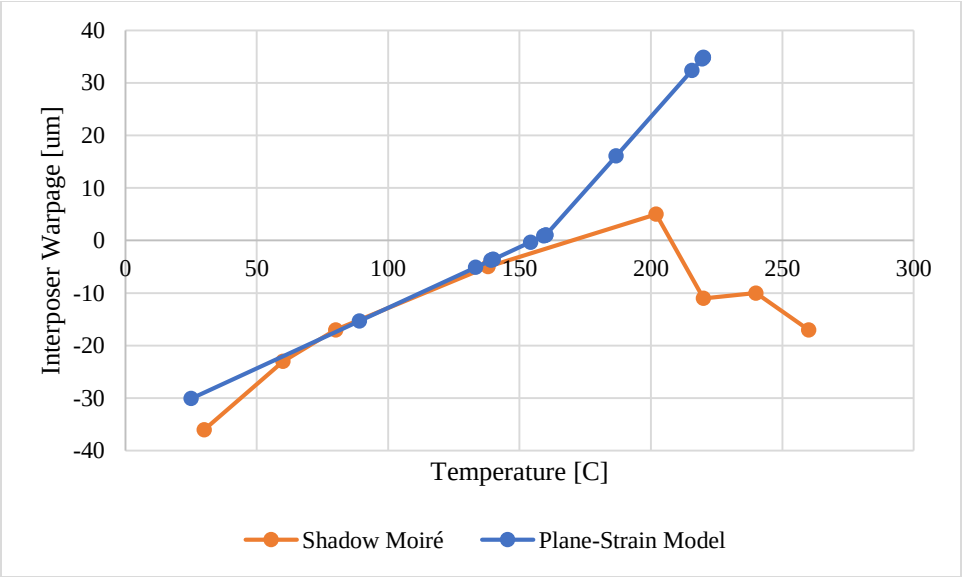


Figure 7.1: Predictive model validation (interposer) for 25mm, 100µm glass with 10mm, 400µm die (sample #1).

This observation is visualized in Figure 7.2, where the package makes a "W" shape at room temperature shown in (a). As the temperature increases to stress free temperature, the package becomes flat, shown in (b).

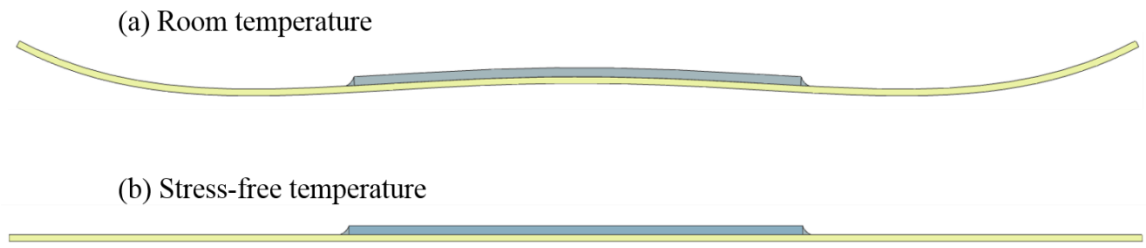


Figure 7.2: Warpage trend observed in glass interposer packages.

The bowl shape of the substrate is a result of the underfill fillet. The underfill is cured at 165 ºC and has a glass transition temperature of 140 ºC. At 25 ºC, the underfill shrinks a large amount. This exerts a force on the interposer, causing it to warp up. On the other hand, at 160 ºC, the underfill cure temperature, the warpage is nearly zero.

7.2 The Effect of Underfill Fillet on Interposer Warpage

The simulation result shown in Figure 7.1 assumes that the underfill fillet touches the top edge of the die. For a fillet that is 400 µm tall and 400 µm long and touches the top edge of the die, the deformed assembly images are shown at 25 ºC in Figure 7.3 and at 160 ºC in Figure 7.4. As seen, at room temperature, the assembly has a dome and bowl shape as illustrated in Figure 7.2a, while the assembly is nearly flat at 160 °C, the stress-free temperature.

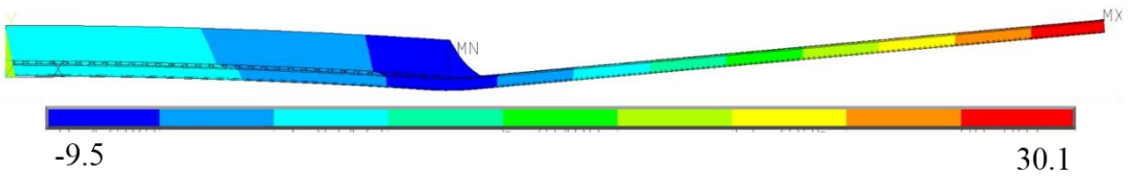


Figure 7.3: Warpage contour plot (at 20x scale) of package with full fillet at 25 ºC.

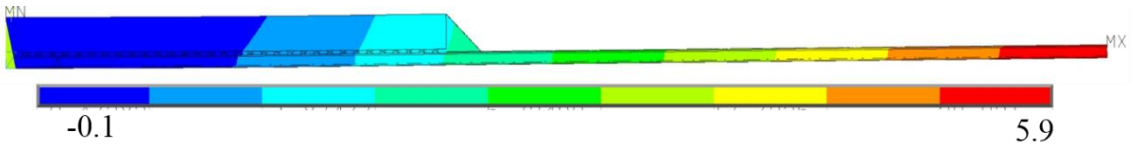


Figure 7.4: Warpage contour plot (at 20x scale) of package with full fillet at 160 ºC.

To understand the role of the underfill fillet size, different sizes of fillets were simulated. In all of the simulations, the stress-free temperatures, the geometry, and the mesh were kept identical to be able to compare different cases. The warped geometry, as simulated, with a fillet that is 200 µm tall and 200 µm long is shown in Figure 7.5 at 25 ºC and in Figure 7.6 at 160 ºC. As seen, at 25 ºC, the interposer is nearly flat, in contrast to the warpage shown in Figure 7.3 for a larger fillet. In both cases, the die warpage is nearly identical, and this is because the fillet has minimal effect on the warpage of the die. Also, the warpage at 160 ºC for both cases is minimal, as this is the stress-free temperature for both assemblies.

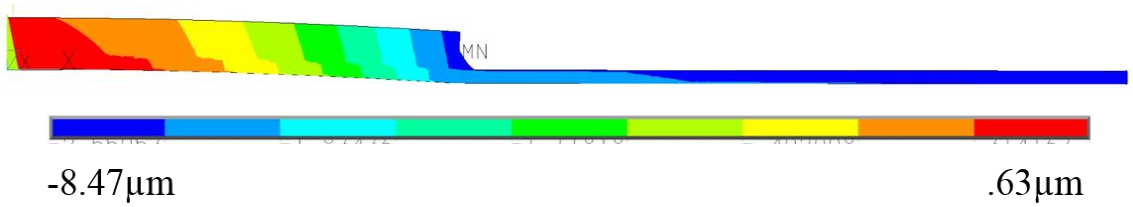


Figure 7.5: Warpage contour plot (at 20x scale) of package with half fillet at 25 ºC.

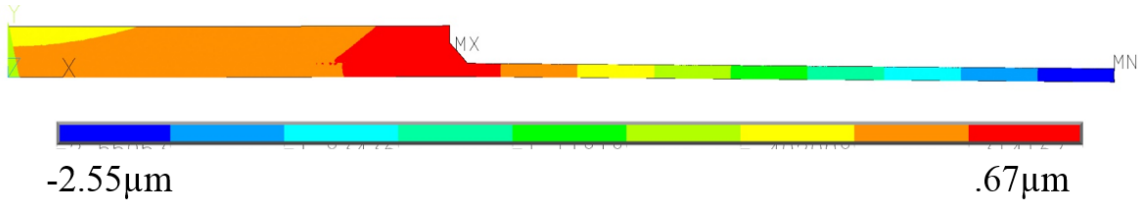


Figure 7.6: Warpage contour plot (at 20x scale) of package with half fillet at 160 ºC.

In addition to the two fillets, a third case was simulated in which there was no underfill fillet. Although such cases extremely rare in actual applications, it is possible due to incomplete or unoptimized underfill volume, one or more sides of the assembly may not have an underfill fillet, and thus, it is reasonable to examine the role of no fillet on the assembly warpage. Without an underfill fillet, the interposer warpage at room temperature is dome-shaped at 25 ºC, as illustrated in Figure 7.7. One of the important differences between Figure 7.3 and Figure 7.7 is that the assembly has a uniform dome shape in Figure 7.7, while it has a dome and bowl shape in Figure 7.3. Also, as the structure is uniformly dome-like in Figure 7.7, the overall warpage is much greater without any fillet. Figure 7.8 shows the warpage at 160 ºC for a no-fillet case, and as before for other cases, the assembly has minimal warpage near the stress-free temperature.

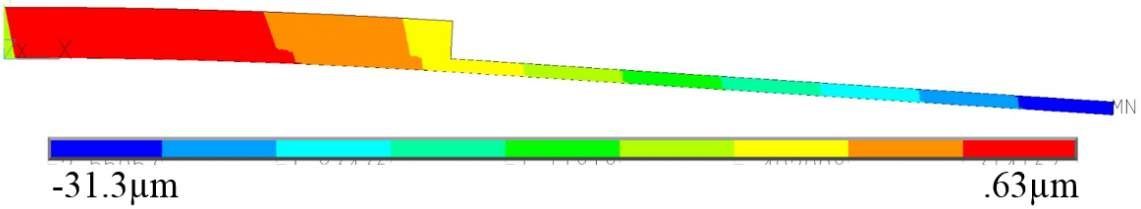


Figure 7.7: Warpage contour plot (at 20x scale) of package with no fillet at 25 ºC.

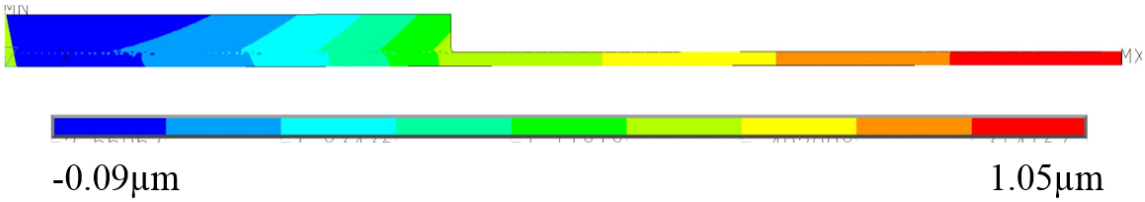


Figure 7.8: Warpage contour plot (at 20x scale) of package with no fillet at 160 ºC.

The interposer warpage is relevant in package to board assembly, and the planarity of the package determines whether assembly is feasible. Also, the CTE and

modulus of the underfill impact the interposer warpage. Changing the material properties of the underfill would alter the effects of the fillet on interposer warpage.

The importance of the size of the fillet on interposer warpage may explain the variability in the experimental warpage results, presented in Figure 5.13 though Figure 5.20. The variation in the size of the fillet produces noticeable warpage differences. If the fillet from a package was not uniform around the die, the package would warp unevenly.

The impact of underfill fillet size observed in glass should be true for other materials as well. The degree to which the trend is observed should correlate to the CTE mismatch because the monotonic warpage state is continued or changed by the size of the underfill fillet.

CHAPTER 8

PREDICTIVE MODEL FOR FIRST-LEVEL INTERCONNECT THERMAL-CYCLING RELIABILITY

This chapter provides details on the thermal-cycling reliability of first-level interconnects taking into consideration the thermal profile associated with substrate processing and flip-chip assembly.

In contrast to the warpage measurements, modeling, and validation which are performed at the edge of the interposer, all strain measurements come from the corner of the die, as illustrated in Figure 8.1. This is done because the corner of the die will have the worst case scenario.

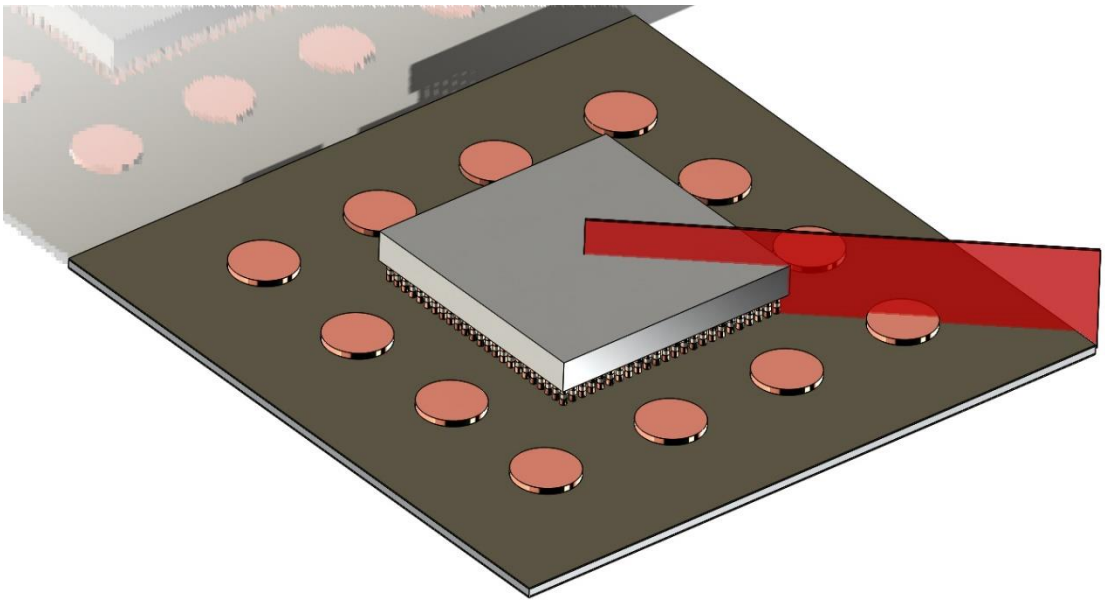


Figure 8.1: "Corner" cross section of package used for reliability modeling.

8.1 Thermal Profile for Process and Thermal Cycling

Table 8.1 details the full fabrication and assembly process modeled in addition to the thermal cycling conditions. As mentioned in the previous chapter, during fabrication,

the model begins with a bare glass panel at room temperature. The panel is heated to 160 ºC and ZIF is birthed to mimic the curing temperature. After cooling, copper is deposited at 40 ºC. The panel is cooled and heated to 220 ºC, when the die, solder, and die pads are birthed. The assembly is cooled to room temperature over 300 seconds.

After flip chip assembly, the flip chip on glass structure is simulated to be thermal cycled as outlined in the thermal profile in Table 8.1. The minimum and maximum temperatures of -55 and 125 ºC, according to JEDEC [15]. As seen, simulated thermal cycling uses five minute dwells and five minute heating and cooling periods. The thermal cycling is included with the fabrication, assembly, and thermal cycling for the full temperature profile in Figure 8.2.

Table 8.1: Thermal cycling conditions.

Description	Temperature [ºC]	Time [seconds]
Thermal Cycling	Ramp to -55	300
	-55 dwell	300
	Ramp to 125	300
	125 dwell	300

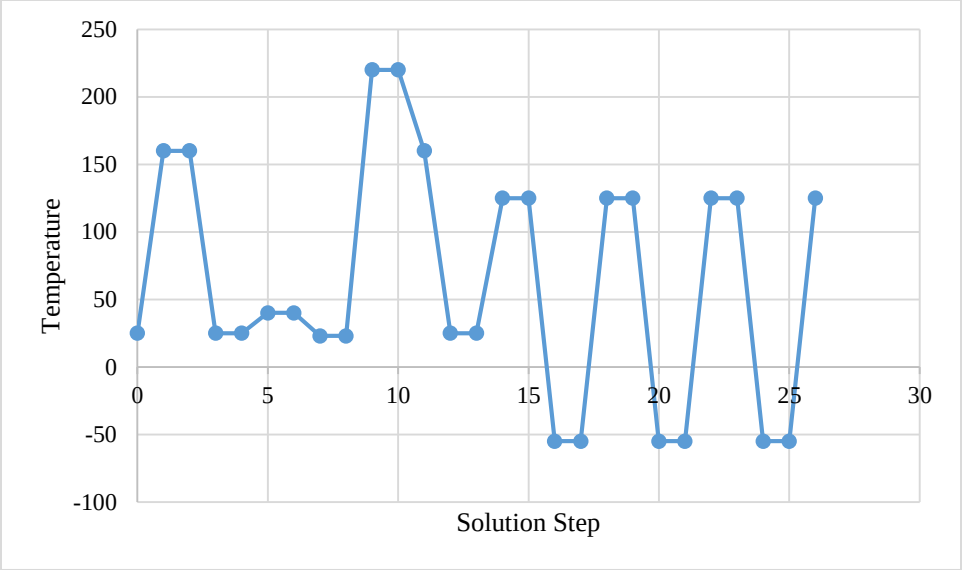


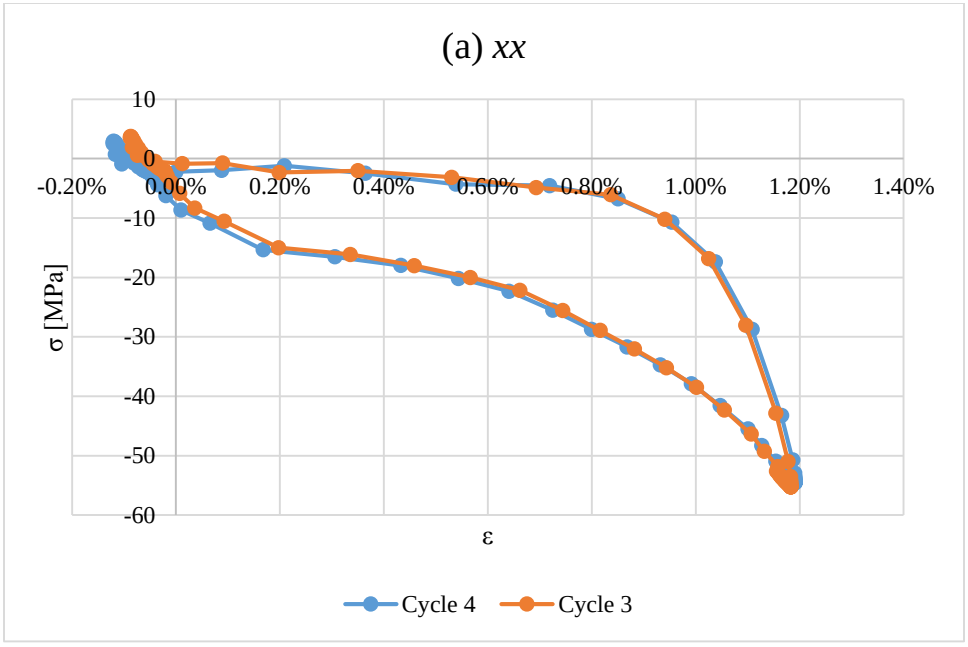
Figure 8.2: Full temperature model for fabrication, assembly, and thermal cycling.

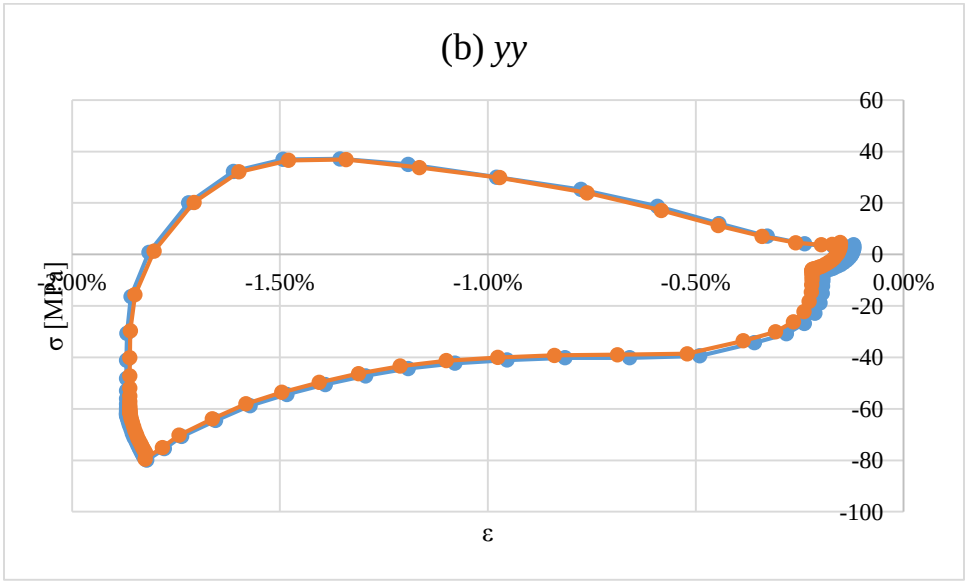
8.2 Solder Strain Contours

To evaluate the fatigue life of the solder during thermal cycling, inelastic strain range per thermal cycle is used. As solder joint fatigue is low-cycle fatigue, strain-based prediction is appropriate [39]. As the solder undergoes multi-axial strain, the equivalent strain over one thermal is used for fatigue life calculation. The inelastic strain increment through a given temperature cycle is summed to get inelastic strain accumulated per cycle, and this value is then divided by 2 to get inelastic strain range per cycle.

To acquire cumulative inelastic strain range from the predictive models, three thermal cycles are run. The third cycle is used as the thermal cycle for which the strain tensors are acquired for cumulative strain calculation. This is because the stress-strain hysteresis loop almost stabilizes by the third cycle. To validate this, the components of stress and strain of fourth thermal cycle were compared to the third thermal cycle, shown in Figure 8.3. As seen in Figure 8.3a, the stress-strain components in normal *x* direction are small in magnitude. However, the normal *y* direction components as well as shear

components have sizeable magnitude. The normal *y* direction components are influenced by warpage as well as underfill expansion/contraction during thermal cycling, while the shear components are influenced by global differential displacement of the silicon die compared to the glass interposer as well as local differential displacement.





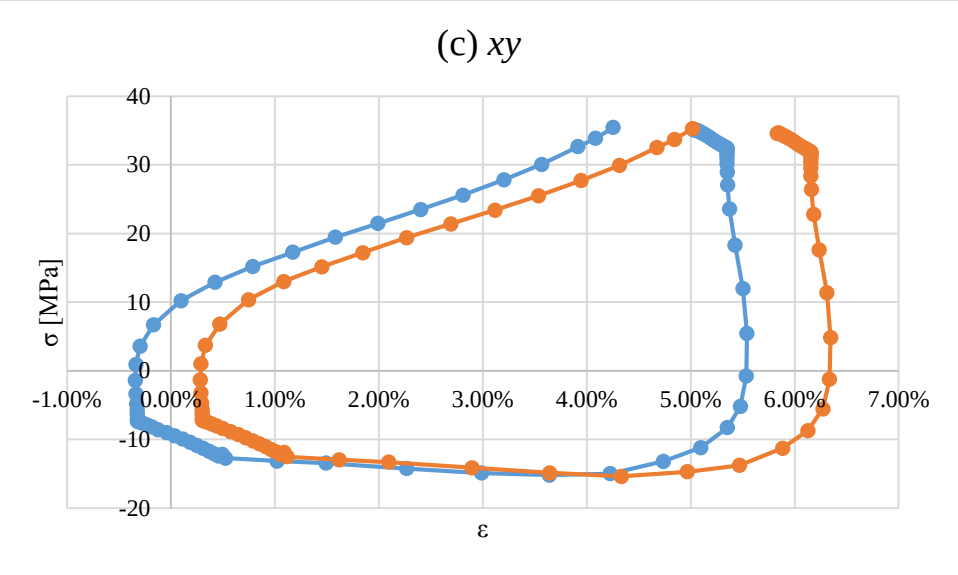


Figure 8.3: Strain hysteresis loop for (a) *xx*, (b) *yy*, and (c) *xy* components of plane-strain model.

Figure 8.5 shows the inelastic strain range contours for solder joints from a 25 mm x 25 mm x 150 µm glass interposer with 10 mm x 10 mm x 200 µm die. The contours come from the solder three joints furthest from the neutral point, as shown in Figure 8.4. The solder images are rectangular shaped because of the copper pillar interconnect technology. Since fatigue life is a function of inelastic strain range, the contour plots of accumulated strain depict where the solder should fail.

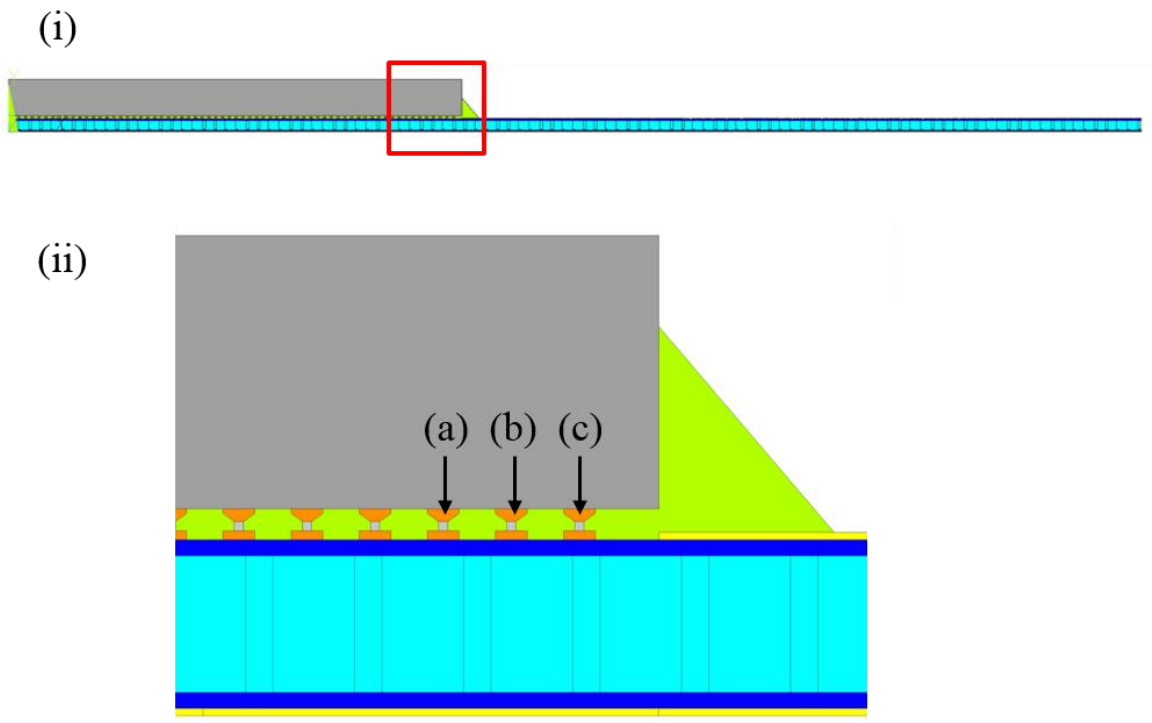


Figure 8.4: Solder joint location schematic for solder strain contours.

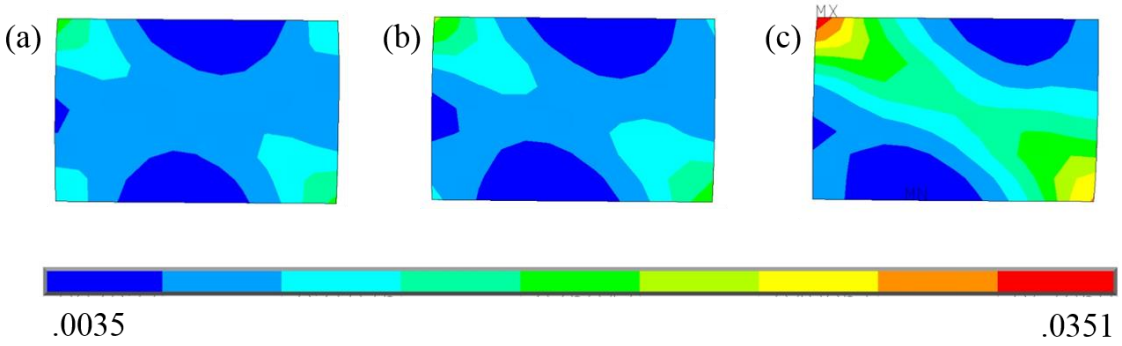


Figure 8.5: Inelastic strain range contours for glass interposer.

As seen in Figure 8.5, there is not much variation in solder strains for the last three solder joints. This is because the underfill is able to mechanically couple the die to the interposer and reduces the solder strains. Also, as seen, the solder strains are the greatest at the top left corner of the solder joint.

8.3 Thermal Cycling Fatigue Life

Based on the Based on the accumulated strain values, the fatigue life is calculated using the Coffin-Manson equation,

$$\Delta\varepsilon_P N_f^{\alpha} = C \quad \textbf{(8.1)}$$

where $\Delta\varepsilon_P$ is the plastic strain range, N_f is the fatigue life, α is the fatigue ductility exponent, and C is the fatigue ductility coefficient. Volume averaging has been suggested to predict fatigue life [22]. This work uses elements with a total area of 12.5 μm^2 (4.2 percent of the solder joint area) close to the critical location to compute the volume-averaged plastic strain range. The Coffin-Manson-type equation is an empirical fit, as most low-cycle fatigue life models are. The values used for tin silver solder in (8.1) are presented in Table 8.2.

Table 8.2: Coffin-Manson coefficient values.

Model	α	C	$\Delta\varepsilon_P$	N_f
Kanchanomai, *et al.* [40]	0.93	21.9	.0271	1336
Andersson, *et al.* [41]	0.6978	3.921	.0271	1245

Based on these values, the solder strain life is calculated to be 861 with the Andersson, et al., coefficients and 1013 with the Kanchanomai, et al., coefficients.

CHAPTER 9

MATERIAL AND GEOMETRY GUIDELINES FOR WARPAGE

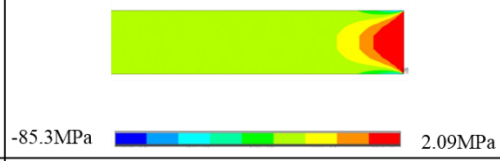
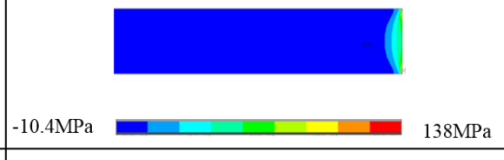
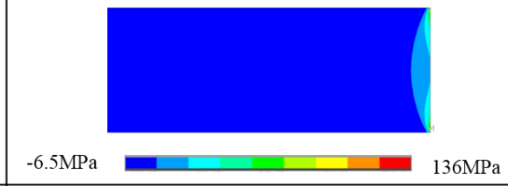
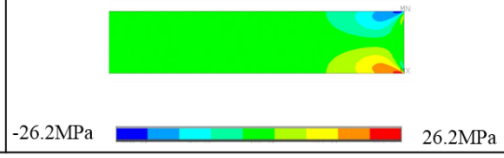
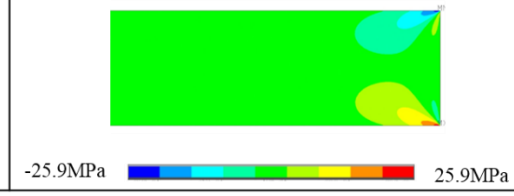
This chapter employs the validated finite-element models to compare warpage for organic and silicon packages against glass packages. Also, this chapter examines the role of geometry parameters on flip chip on glass package warpage.

9.1 Process-Induced Stresses

During fabrication, the sequential fabrication processes create internal stresses within the microelectronics package. Table 9.1 shows the components of stress at the end of glass interposer fabrication for two glass thicknesses, 100 µm and 300 µm. Each stress component is plotted on the same scale for both thicknesses.

The thinner glass experiences greater stress in the *x*, *y*, and *xy* directions. As seen, the axial stresses (σ_{xx}) are mostly compressive in the body of the glass. This is because the glass has a lower CTE compared to the polymer, and therefore, under cooling, experiences compressive axial stress. The peel stress (σ_{yy}) is mostly zero most of the interface, except near the edges. Similarly, the shear stress (σ_{xy}) is mostly zero most of the interface, except near the edges. The edge effect is present through a length that is of the same order of magnitude as the thickness of the substrate.

Table 9.1: Stress during fabrication as function of glass thickness.

	100µm Glass	300µm Glass
σ_{xx}		
σ_{yy}		
σ_{xy}		

An alternative approach to varying the thickness of glass is to vary the thickness of the build-up layers relative to the glass while keeping the glass thickness constant. Similar trends will be observed.

9.2 Warpage Comparison for Organics, Glass, and Silicon

One objective of this work is to evaluate the use of glass interposers against existing technology. Thus, Figure 9.1 compares the simulated die warpage on glass interposers with organic substrates and silicon interposers. As discussed earlier, the same modeling method was used to predict the warpage for organic and silicon substrates with similar process modeling and similar mesh density. In these simulations, the silicon substrate was assumed to be isotropic, while the organic substrate was assumed to be orthotropic with temperature-dependent properties. The material properties for these substrates are given in Table 6.1.

As seen in Figure 9.1, the organic substrate has the highest warpage of 97.4 µm compared to the warpage of 17.5 µm for the low CTE glass interposer and 6.12 µm of Si interposer. This is because the organic substrate has the largest CTE mismatch compared to the silicon die, followed by low-CTE glass substrate and silicon substrate, in that order.

Although Si substrate has a matched CTE compared to the die, the assembly still has some warpage, albeit small. This is because of the presence of polymer and copper materials that are present on the silicon substrate and thus, would increase its effective CTE compared to the Si die. Although the silicon substrate has the least warpage, the board level assembly as well as the second-level interconnect reliability will pose greater challenges for a silicon interposer. This is because the CTE mismatch between a silicon interposer and an organic printed circuit board will be high. Glass provides an intermediate CTE between a silicon die and an organic system board, and therefore, can function as an appropriate interposer between the die and the board.

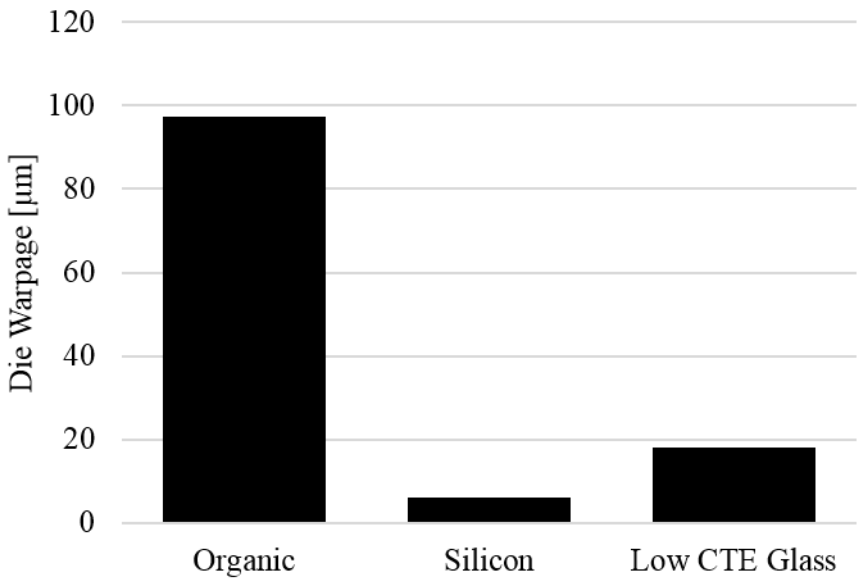


Figure 9.1: Die warpage for a 10 mm, 200 µm-thick die on an 18.4 mm, 150 µm-thick substrate as function of substrate core material.

9.3 Warpage Comparison for Different Die and Substrate Thicknesses

The warpage depends on both the die and substrate thickness as seen in Figure 9.2, in which data for a 400 µm die is plotted in red and a 200 µm die is plotted in black. Die warpage is plotted as a normalized value for each die thickness to highlight the importance of the ratio of die thickness to substrate thickness. From this plot for a glass package, the worst ratio is when the die is 1.2 to 1.5 times as thick as the glass core. This ratio will vary based on substrate materials and build-up, but the idea will still apply. For example, with more metal layers, the ratio is expected to increase as the overall interposer will be larger in relation to the glass core. Moving away from this critical ratio, making either the die or substrate be thicker or thinner, will reduce the overall warpage.

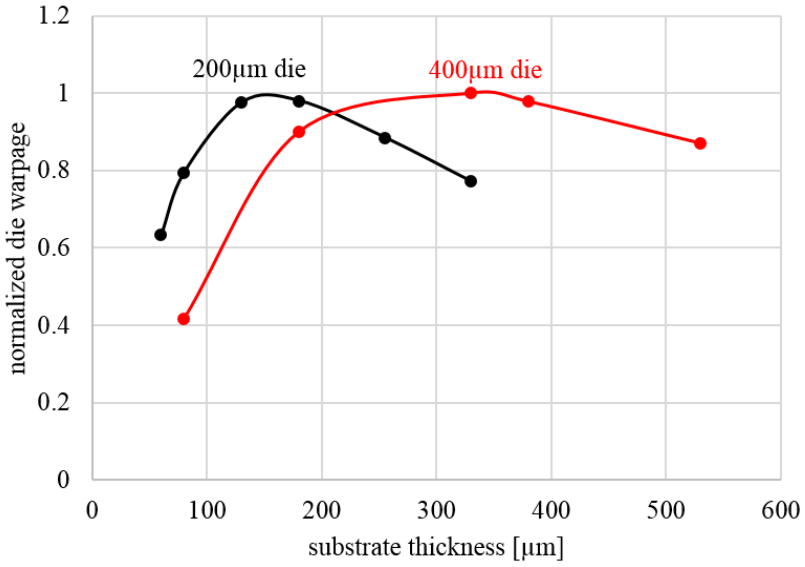


Figure 9.2: Normalized warpage as a function of substrate thickness for a glass package.

9.4 Fatigue Life Comparison for Organics, Glass, and Silicon

Similar to glass, the fatigue life for organic and silicon are calculated using the inelastic strain range from the third thermal cycle. The inelastic strain range contours for the three solder joints furthest from the center of the package are illustrated for organic substrate in Figure 9.3 and for silicon interposer in Figure 9.4. For reference, the inelastic strain range contours for glass interposer is shown in Figure 8.5.

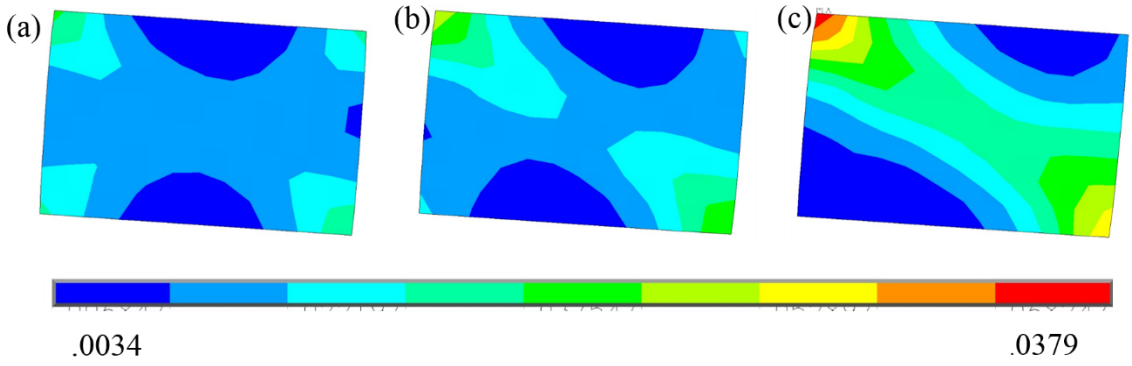


Figure 9.3: Inelastic strain range contours for organic substrate.

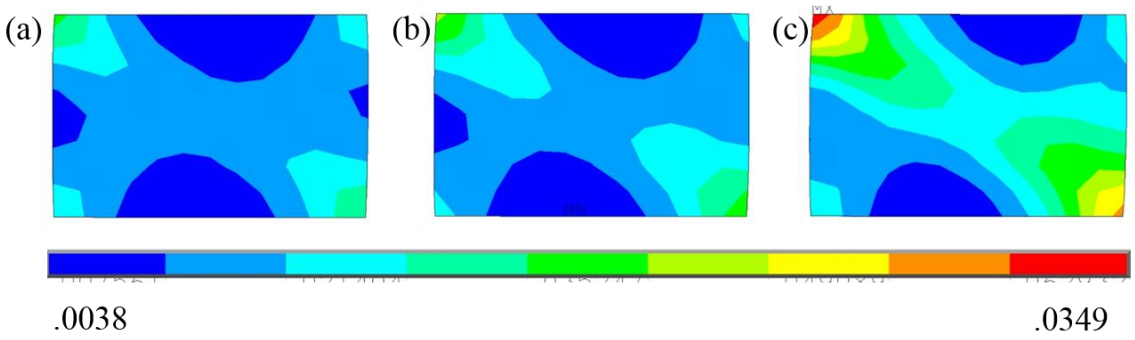


Figure 9.4: Inelastic strain range contours for silicon interposer.

As seen, of the three substrates, the silicon substrate has the least inelastic strain. This is followed by glass interposer and organic substrate, in that order. The presence of underfill makes the solder strains almost the same for the three cases. Otherwise, it is likely that solder in organic substrate will have the greatest strain and is likely to fail through fatigue much sooner. The solder strains, in general, are high compared, and this is because of small standoff height and small diameter microbumps used in this study.

Using the predictive model thermal cycling described in *8.3 Thermal Cycling Fatigue Life*, the fatigue life for a 25 mm x 25 mm x 150 µm core interposer with 10 mm x 10 mm x 200 µm die are presented in Table 9.2. Organic has the worst fatigue life and silicon has the best fatigue life, with glass being in the middle.

Table 9.2: Fatigue life for 25mm, 150µm core with 10mm, 200µm die (with underfill).

Material	Organic	Glass	Silicon
Fatigue Life [41]	1100	1245	1255
Fatigue Life [40]	1217	1336	1344

It is important to note that fatigue life predictions show large changes with small changes in inelastic strain range. This is because the Coffin-Manson equation is very sensitive to minor changes in the inelastic strain range. Also, in this comparison, the

inelastic plastic strain range is obtained from one critical element in the model. It is also a common practice to select several neighboring elements to determine volume-averaged strain for fatigue life calculations. As the purpose of this section is to compare different cases, it is appropriate to use the same technique for the comparison.

9.5 Design Guidelines

Based on the experimental findings and predictive model developed, this work offers design guidelines to minimize the impact of warpage and improve fatigue life.

Glass was considered as an interposer material in part because of good mechanical material properties, with high modulus material and CTE close to silicon. This is evident in experimental data, as no warpage observed was greater than 17 µm for a 10 mm x 10 mm die. This expanded to a maximum warpage of 40 µm at the package level for a 25 mm x 25 mm interposer. This is significantly below the JEDEC standard, at 203 µm (8 mil) that would be the maximum tolerance based on package size. This large difference between measured warpage for glass and the JEDEC standard is because the JEDEC standard are based on organic substrates, which have much higher warpage than glass. In comparison to glass and organic, a silicon interposer will have less die warpage than a glass interposer after die assembly, but has a large CTE mismatch with the system board.

To minimize fabrication warpage for a glass package, build-up symmetry can be utilized. Laminating polymer layers on both sides at the same time reduces internal stress. Designing metal layers with similar amounts of copper in each area reduces warpage. During annealing and curing processes, it is important to uniformly support the glass panel, rather than letting it sag.

To minimize assembly warpage for a glass package, the die size can be reduced, the thickness ratio of the die to glass interposer can be move away from 1.2-1.5, and underfill choice. As the interposer is only coupled to the die in the die region, interposer size is irrelevant to die warpage. However, interposer size is still important to warpage during second level assembly. The assembly warpage of a silicon die on a glass interposer is worst when the silicon is 1.2 to 1.5 times as thick as the glass panel. Choosing die or interposer thicknesses that are outside this range will produce less warpage. While not studied in this work, lowering the reflow temperature is expected to reduce warpage because there will be a smaller temperature change to the operating temperature range.

The underfill fillet greatly influences the shape of the interposer warpage after assembly at room temperature. Larger fillets warp the interposer upward around the die while smaller fillets have less impact on the interposer warpage.

CHAPTER 10

CONCLUSIONS, CONTRIBUTIONS, AND FUTURE WORK

10.1 Conclusions

This work has experimentally fabricated glass interposers and assembled flip chip devices. Also warpage measurements have been carried out using shadow moiré technique. Physics-based finite-element models have been developed to mimic fabrication and assembly processes and to compare predicted warpage values against experimental data.

Based on the experimental and theoretical work carried out in this thesis, it is seen that thin glass interposer is a viable alternative to organic or other substrates for reducing warpage. This work has shown that the warpage can be as small as 19% compared to organic substrates for dies with a thickness of 200 um on a 150 um thick substrate. This work has also shown that the solder joint fatigue life for glass interposers can exceed 1000 thermal cycles.

With glass interposers, the die warpage is worst when the die is 1.2 to 1.5 times as thick as the interposer (including build-up layers), and thus, a suitable die to substrate thickness ratio needs to be selected for reducing the package warpage. Glass substrates, due to their intermediate CTE, can effectively serve as interposers between a silicon die and an organic printed circuit board. Thus, glass interposers will be appropriate for enhancing the reliability of first as well as second-level interconnects.

10.2 Contributions

This work explores the mechanical reliability of glass as an interposer material, with a focus on warpage. The contributions of this work include:

- Fabrication of glass interposer packages with varying interposer size and thicknesses and dies of varying thicknesses. While following a process of record for consistency in fabrication in assembly, this allows systematic study of design parameters.
- Warpage measurement of glass packages, obtaining critical data for the development of glass as an interposer material.
- Development of predictive models for glass warpage, including the fabrication and assembly process steps, to better understand the mechanical reliability aspects relating to glass interposers.
- Validation of models with shadow moiré data, to improve and give credence to the models.
- Investigation of the role of underfill fillet on warpage for glass interposers.
- Thermal cycle modeling to compare the fatigue life of glass to other substrate materials.
- Creating design guidelines to minimize warpage and increase fatigue life of glass interposer packages.

10.3 Future Work

There are several potential paths for this work to continue. The work may be expanded to include a wider range of glass interposers, including 4ML. The impact of vias for glass interposers, both on warpage and mechanical reliability, is a topic not yet

explored and will be required for glass interposers to become a commercial product. Ultra thin glass panels are another potential area of interest, as mobile demand pushes for even thinner packages.

There is additional scope for improvement in the models developed in this work including a full 3D model, viscoelastic properties of underfill and polymer, and inclusion of thermo-mechanical properties of various materials, especially at higher temperatures, through experimental characterization.

This work compared glass interposers to organic substrates and silicon interposers. The organic substrate was modeled as FR-4. Low CTE organic substrates, made of up to 80 percent glass, are under development as well. While these organic substrates have CTEs as low as the glass presented in this work, they may still experience more warpage after assembly. This is because the organic substrate has a glass transition temperature that is below the reflow temperature, and it is still likely to experience higher warpage. However, a glass interposer has stable material properties in the temperature regime under consideration for electronic packaging assembly and testing.

This work leaves out package to board assembly and its impacts, which would also be required for commercialization. Reliability results from modeling should be validated with experimental work to give more credence to fatigue life predictions.

This work has not considered power cycling issues where the die is expected to be at a higher temperature compared to the interposer. Such power cycling experiments, warpage measurements, and simulations can be potentially carried out in the future. However, it may be pointed out that under power cycling, the higher temperature of the

silicon die will compensate for the lower CTE of silicon, and thus, likely to result in less warpage compared to uniform temperatures studied in this work.

Glass cracking is another concern which is related to mechanical reliability which future work needs to consider. However, glass cracking is a board and complex topic, which may better be served as an independent study, separate of warpage.

Additional studies may be done on alternative fabrication or assembly methods. While it is expected that a lower reflow temperature would decrease warpage, the effects on reliability are unknown. As glass package evolves, the processes used will change. In fabrication, the best examples of this include direct metallization of glass; in assembly, examples include new methods such as direct copper to copper bonding. Thus, there is enormous scope for further research and study in the area of glass interposers.

REFERENCES

[1] G. E. Moore, "Cramming More Components onto Integrated Circuits," *Proc. IEEE,* vol. 86, no. 1, pp. 82-85, 1998.

[2] JEDEC Standard, "Package Warpage Measurement of Surface-Mount Integrated Circuits at Elevated Temperatures: JESD22-B112A," 2009.

[3] R. C. Dunne and S. K. Sitaraman, "Warpage and Interfacial Stress Distribution in a Single-Level Integrated Module (SLIM)," *J. Electronic Packaging, ASME,* vol. 119, no. 3, pp. 197-203, 1997.

[4] J. Kim, S. Lee, J. Lee, S. Jung and C. Ryu, "Warpage Issues and Assembly Challenges Using Coreless Package Substrate," in *IPC APEX Expo*.

[5] R. R. Tummala and M. Swaminathan, Introduction to System-On-Package (SOP), McGraw-Hill, 2008.

[6] W. Tan and I. C. Ume, "Application of Lamination Theory to Study Warpage Across PWB and PWBA During Convective Reflow Process," *IEEE Trans. CPMT,* vol. 2, no. 2, pp. 217-223, 2012.

[7] J. N. Reddy, An Introduction to the Finite Element Method, Tata McGraw-Hill, 2005.

[8] S. D. Rajan, Introduction to Structural Analysis & Design, Wiley, 2000.

[9] S. Raghavan, K. Klein, S. Yoon, J.-D. Kim, K.-S. Moon, C. P. Wong and S. K. Sitaraman, "Methodology to Predict Substrate Warpage and Different Techniques to Achieve Substrate Warpage Targets," *CPMT*, vol. 1, no. 7, pp. 1064-1073, 2011.

[10] S. Raghavan, R. I. Okereke and S. K. Sitaraman, "An Efficient Implementation of Polymer Viscoelastic Behavior Through a Pseudo Visoelastic Model," *J. Microelectronics and Electronic Packaging,* vol. 8, no. 2, pp. 84-87, 2011.

[11] S. Nakamura, R. Miyaoka and A. Kondo, "Effect of Cooling Conditions to Residual Warpage of Laminated Structure Consisting of Epoxy Resin and Various Substrates," *J. Japan Institute of Electronics Packaging,* vol. 16, no. 3, pp. 221-226, 2013.

[12] Z. W. Zhong, P. Arulvanan and C. K. Goh, "Effects of Key Process Conditions on Warpage and Via Protrusion of LTCC Substrate," *Materials and Manufacturing Processes,* vol. 23, pp. 183-188, 2008.

[13] M. A. Hopcroft, W. D. Nix and T. W. Kenny, "What is the Young's Modulus of Silicon?," *J. Microelectromechanical Systems,* vol. 19, no. 2, pp. 229-238, 2010.

[14] H. Guojun, G. K. Yong, L. Jing-en, L. W. Chin and X. Baraton, "Thermoelastic Properties of Printed Circuit Boards: Effect of Copper Traces," in *EMPC*, 2009.

[15] JEDEC, "JESD22-A104-C Temperature Cycling," JEDEC, 2005.

[16] Y. Liu, Y. Liu, Z. Yuan, T. Chen, K. Lee and S. Belani, "Warpage Analysis and Improvement for a Power Module," in *ECTC*, 2013.

[17] X. Liu, J. Zheng and S. K. Sitaraman, "Hygro-Thermo-Mechanical Reliability Assessment o a Thermal Interface Material for a Ball Grid Array Package Assembly," *J. Electronic Packaging*, vol. 2, no. 10, pp. 41-48, 2010.

[18] S. S. Too, J. Hayward, R. Master, T.-S. Tan and K.-H. Keok, "Effects of Organic Package Warpage on Microprocessor Thermal Performance," in *ECTC,* 2007.

[19] T. Lee, J. Lee and I. Jung, "Finite Element Analysis for Solder Ball Fatigue Failures in Chip Scale Package," *Microelectronics Reliability*, vol. 38, pp. 1941-1947, 1998.

[20] X. Liu, Q. Chen, V. Sundaram, M. Simmons-Matthews, K. P. Wachtler, R. R. Tummala and S. K. Sitaraman, "Reliability Assesment of Through-Silicon Vias in Multi-Die Stack Packages," *IEEE Trans. Device and Materials Reliability*, vol. 12, no. 2, pp. 263-271, 2012.

[21] L. O. McCaslin, S. Yoon, H. Kim and S. K. Sitaraman, "Methodology for Modeling Substrate Warpage Using Copper Trace Pattern Implementation," *IEEE Trans. Adv. Packaging*, vol. 32, no. 4, pp. 740-745, 2009.

[22] R. Darveaux, "Effect of Simulation Methodology on Solder Joint Crack Growth Correlation," in *ECTC*, 2000.

[23] N. Bai, X. Chen and H. Gao, "Simulation of Uniaxial Tensile Properties for Lead-free Solders with Modified Anand Model," *Materials and Design*, vol. 30, pp. 122-128, 2009.

[24] S. Kang and I. C. Ume, "Techniques for Measuing Warpage of Chip Packages, PWBs, and PWB Assemblies," *CPMT*, vol. 3, no. 9, pp. 1533-1544, 2013.

[25] K. M. Jansen and B. Öztürk, "Warpage Estimation of a Multilayer Package Including Cure Shrinkage Effects," *IEEE Trans. CPMT*, vol. 3, no. 3, pp. 459-466, 2013.

[26] W. Zhang, F. Zhu, H. Liao, S. Song, H. Zhang and S. Liu, "Warpage Measurement of Silicon Wafers of Various Bonding Areas," in *Int'l Conference on Electronic Pacakaging Technology & High Density Packaging*, 2012.

[27] W. Lin, S. Wen, A. Yoshida and J. Shin, "Evaluation of Raw Substrate Variation from Different Suppliers and Processes and their Impact on Package Warpage," in *ECTC*, 2012.

[28] W. Lin and M. W. Lee, "PoP/CSP Warpage Evaluation and Viscoelastic Modeling," in *ECTC*, 2000.

[29] X. Qin, S. Gottschall, N. Kumbhat, R. M. Raj, S. Kim, V. Sundaram and R. Tummala, "Large Silicon, Glass, and Low CTE Organic Interposers to Printed Wiring Board SMT Interconnections Using Copper Microwire Arrays," in *ECTC*, 2013.

[30] V. Sundaram, "Glass is More Than an Interposer," in *Global Interposer Technology Conference*, 2013.

[31] W. Thomas, "Manufacturing Readiness of Glass Interposers," in *Global Interposer Technology Conference*, 2013.

[32] K. Demir, K. Ramachandran, Y. Sato, Q. Chen, V. Sukumaran, R. Rucha, V. Sundaram and R. R. Tummala, "Thermomechanical and Electrochemical Reliability of Fine-Pitch Through-Package-Copper Vias (TPV) in Thin Glass Interposers and Packages," in *ECTC*, 2013.

[33] S. Cho, Y. Joshi, V. Sundaram, Y. Sato and R. R. Tummala, "Comparison of Thermal Performance between Glass and Silicon Interposers," in *ECTC*, 2013.

[34] B. C. Chou, Y. Sato, V. Sukumaran, J. Sun, V. Sundaram, G.-K. Chang and R. R. Tummala, "Modeling, Design, and Fabrication of Ultra-high Bandwidth 3D Glass Photonics (3DGP) in Glass Interposers," in *ECTC*, 2013.

[35] P. S. Theocaris, "Moiré Topography of Curved Surfaces," *Experimental Mechanics,* vol. 7, no. 7, pp. 289-296, 1967.

[36] H. Ding, R. E. Powell, C. R. Hanna and I. C. Ume, "Warpage Measurement Comparison Using Shadow Moiré and Projection Moiré Methods," *IEEE Trans. Comp. & Packaging Tech.*, vol. 24, no. 4, pp. 714-721, 2002.

[37] R. S. Li and J. Jiao, "The Effects of Temperature and Aging on Young's Moduli of Polymeric Based Flexible Substrates," *Int. J. Microcircuits & Electronic Packaging,* vol. 23, no. 4, pp. 456-461, 2000.

[38] S. Manjula and S. K. Sitaraman, "Effect of Out-of-Plane Material Behavior on In-Plane Modeling," in *InterSociety Conference on Thermal Phenomena*, 1998.

[39] R. W. Smith, M. H. Hirschberg and S. S. Manson, "Behavior of Materials Under Conditions of Thermal Stress," NACA, 1954.

[40] C. Kanchanomai, Y. Miyashita and Y. Mutoh, "Low-Cycle Fatigue Behavior of Sn-Ag, Sn-Ag-Cu, and Sn-Ag-Cu-Bi Lead-Free Solders," *J. Electronic Materials,* vol. 31, no. 5, pp. 456-465, 2002.

[41] C. Andersson, Z. Lai, H. Jiang and Y. Yu, "Comparison of isothermal mechanical fatigue properties of lead-free solder joints and bulk solders," *J. Material Science and Engineering A,* vol. 394, pp. 20-27, 2005.