ADDRESSING THERMAL AND ENVIRONMENTAL RELIABILITY IN GAN BASED HIGH ELECTRON MOBILITY TRANSISTORS

A Thesis
Presented to
The Academic Faculty

by

Samuel H. Kim

In Partial Fulfillment
of the Requirements for the Degree
Master of Science in the
School of Mechanical Engineering

Georgia Institute of Technology

August, 2014

Copyright © Samuel H. Kim 2014

ADDRESSING THERMAL AND ENVIRONMENTAL RELIABILITY IN GAN BASED HIGH ELECTRON MOBILITY TRANSISTORS

Approved by:

Dr. Samuel Graham, Advisor
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Baratunde A. Cola
School of Mechanical Engineering
Georgia Institute of Technology

Dr. Shyh-Chiang Shen
School of Electrical and Computer Engineering
Georgia Institute of Technology

Date Approved: 04/07/2014

To my family and God

ACKNOWLEDGEMENTS

First of all, I would like to express my sincere gratitude to my advisor, Dr. Samuel Graham, for the continuous support of my MS study and research, for his patience, motivation, enthusiasm, and immense knowledge. His guidance helped me in all the time of research and writing of this thesis. I could not have imagined having a better advisor and mentor for my study.

Besides my advisor, I would like to thank the rest of my thesis committee: Dr. Baratunde Cola and Dr. Shyh-Chiang Shen for taking their time to be on my committee. Their encouragement and insightful comments are very much appreciated.

I am grateful to Raytheon, RFMD, and the Air Force Research Laboratory for their financial support, providing devices, and providing critical feedbacks on the measurements. I truly wish many thanks to Dr. Sukwon Choi for his sincere instruction and training of device physics and the operating principle of Raman spectroscopy. He has never refused to help me when I had a hard time during experiments and my personnel issues.

I would like to thank my fellow graduate students, past and present, for their support and scientific collaborations in Electronics Manufacturing and Reliability Laboratory Group: In no particular order, thanks are deserved to Dr. Nazli Donmezer, Dr. Yongjin Kim, Dr. Anuradha Bulusu, Dr. Hossein Sojudi, Dr. Parisa Shahid, Hyungchul Kim, Minseok Ha, Shweta Natarajan, Yishak Habtemichael, Anne Mallow, Jason Jones, Xiuping Chen, Luke Yates, Georges Pavlidis, David Samet, John Taphouse, Adewale Odukomaiya, Mahiro Kato, and Ankit Singh.

I also want to mention some friends outside of our group, who have made the life more pleasant and less painful: Sangbeom Cho, Thomas Yun, Jeomoh Kim, Steven Isaacs, Vikneshan Sundaralingam, Martin Cacan, Theresa Wilks, Stephen Leadenham, Wayne Maxwell Jr., and many more. I wish to also acknowledge people met through the GTKSA, the Yonsei Alumni,

and the New Church of Atlanta who were a huge part of my journey as well. Lastly, I would like to thank my parents for always believing in me, for their continuous love and their support in my decisions. Without whom I could not have made it here.

TABLE OF CONTENTS

ACKNOWLEDGEMENTS iii
LIST OF TABLES vii
LIST OF FIGURES viii
SUMMARY viii
CHAPTER 1: INTRODUCTION 1
1.1 Gallium Nitride HEMTs 1
1.2 Operating Principles of AlGaN/GaN HEMTs 4
1.3 Reliability 8
1.3.1 Thermal Reliability 10
1.3.2 Environmental Reliability 13
1.4 Research overview 16
CHAPTER 2: BACKGROUNDS TO IMPROVE THE THERMAL REILABILITY OF ALGAN/GAN HEMTS 19
2.1 Utilizing High Thermal Conductive Substrates 19
2.1.1 Integration of GaN on Diamond 24
2.2 Utilizing Thermal Packaging 34
CHAPTER 3: EXPERIMENTAL METHODOLOGY OF TEMPERATURE MEASUREMENTS 37
3.1 Introduction 37
3.2 Micro-Raman Spectroscopy 39
3.2.1 Theory 39
3.2.2 Raman Thermometry 41
3.2.3 Peak Position Method 42
3.2.4 Linewidth Method 43
3.2.5 2-peak-fit Method 44
3.2.6 Calibration and Uncertainty 45
3.3 Experimental Set-up 49
3.4 Results and Discussion 55
3.5 Uncertainty Analysis 60
3.6 Summary and Conclusions 62

CHAPTER 4: FINITE ELEMENT MODELING 63
4.1 Introduction 63
4.2 GaN HEMTs Modeling 64
4.2.1 Thermal Modeling 64
4.2.2 Thermo-Structural Mechanics Coupled Modeling 67
4.3 Temperature Results 70
4.3.1 Effect of Substrate and Thickness 71
4.3.2 Effect of Gate-to-gate Spacing 72
4.3.3 Effect of Gate Width 76
4.3.4 Effect of Interfacial Layers 77
4.4 Operational Thermo-Elastic Stresses 80
4.5 Summary and Conclusions 85
CHAPTER 5: ENVIRONMENTAL RELIABILITY IN ALGAN/GAN HEMTS 87
5.1 Introduction 87
5.2 Experimental Set-up 90
5.3 Results and Discussion 95
5.3.1 Step-Stress-test 95
5.3.2 Time Dependent Degradation Study 97
5.4 Summary and Conclusions 102
CHAPTER 6: CONCLUSION AND FUTURE WORK 104
REFERENCES 108

LIST OF TABLES

Table 1: Comparison of the physical properties of important semiconductors for high voltage power devices [8, 9]..2
Table 2: Properties of key substrate materials, AlN buffer layer, and GaN layer [8, 56, 57].......22
Table 3: Thermal boundary resistances between GaN and substrates..34
Table 4: Linear coefficients for 2-peak fit method by [98]..47
Table 5: Physical origin of temperature dependence and limitation in Raman thermometry.......48
Table 6: Property of Instec C300W industrial chiller..51
Table 7: Thermal conductivity of material used in experiments [62]..53
Table 8: Total uncertainty (all in °C) is decomposed into each uncertainty to confirm the main drivers of total uncertainty, which are Term (5) and (6) that are resulted from the uncertainty of elastic constants of GaN. 61
Table 9: Temperature dependent thermal properties [62, 104-106] 66
Table 10: Assuming the transverse-isotropic elastic symmetry, the elastic constant matrix of the thin films take the form, and the values are following [106-108]:......................69
Table 11: Total thermal resistances for different gate-to-gate spacing for SiC and Diamond as substrates. 74
Table 12: Thermal resistances between GaN on Diamond and SiC [59, 65] (in m^2-K/GW) 78
Table 13: CTE of various material at 300 K [57] 81

LIST OF FIGURES

Figure 1: AlGaN/GaN HEMT applications: Satellite communication system, radar system, epitaxial GaN layer, and GaN electronics in hybrid electric vehicles [10-13]............3

Figure 2: Main characteristics of GaN: high electron mobility, large band gap, and low parasitic capacity, which make GaN-devices advantageous in power and RF circuits [14]..3

Figure 3: Formation of a 2DEG at the AlGaN/GaN heterointerface due to spontaneous and piezoelectric polarization effects..6

Figure 4: Illustration of pseudomorphic growth of AlGaN on top of GaN resulting in tensile strain due to the lattice mismatch between AlGaN and GaN 6

Figure 5: 2-dimensional electron sheet density induced by piezoelectric effect in $Al_xGa_{1-x}N$/GaN heterostructures with different Al mole fraction and various AlGaN barrier layer thickness: 1–30 nm; 2–20 nm; 3–10 nm; 4–5 nm. Thick solid line shows the sheet electron density corresponding to a corresponding critical thickness of AlGaN for fully strained heterostructures as a function of aluminum molar fraction [18]. 7

Figure 6: Decrease in the drain current (I_D) and the output power (P_{out}) during the time-dependent operation test [31] 9

Figure 7: Change in device characteristics before (Fresh; blue line) and after stress experiment (Degraded; red line) [24]. From upper-left corner (clockwise): I-V output characteristics, transfer characteristics, and gate current characteristics, where I_D = drain current, V_{DS} = drain-source voltage, I_G = gate current, V_{GS} = gate-source voltage, g_m = transconductance...9

Figure 8: Phonon dispersion curves for GaN showing the decay of LO phonons into lower energy modes [36] 11

Figure 9: Cross section image of a GaN HEMT with the location of the hotspot in red dot [37] 11

Figure 10: Decreases in transfer characteristic (g_m) as temperature increases [38] 12

Figure 11: Arrhenius plot showing a Mean Time to Failure (Left) and the extrapolation data demonstrating 20-year drift with 50 ℃ difference (Right) [39]........................13

Figure 12: Gate metal was etched to characterize the exposed surface using AFM. The electrical degradation is closely related to structural damage at the gate edge of the device [40]. 14

Figure 13: Normalized I_{Dmax}, R_D, R_S, $I_{Gstress}$, and I_{Goff} as a function of stress voltage in a step-stress experiment in the V_{DS} = 0 V state ($V_{DG} = V_{DS} – V_{GS}$ = 10 – 50 V in 1V steps) [49]. After the critical voltage, I_{Dmax} decreases, R_D, R_S, $I_{Gstress}$, and I_{Goff} increase due to degradation. 15

Figure 14: Results of the time-resolved Electroluminescence (EL) measurements carried out during stress at V_G = – 30 V, V_{DS} = 0 V [46]. EL demonstrates that the increase in gate leakage current is correlated with the creation of discrete and very localized hot spots [50]. This figure shows, for sufficiently long stress times, degradation occurs even below the critical voltage (here, $V_{critical}$ = – 35 V). 15

Figure 15: Schematic devcie structure with a diagram of thermal path through substrate, where thermal boundary resistances (TBRs) exist between GaN/buffer layer and buffer/substrate. Thermal conductivity of substrate and TBR play an important role to spread the heat out. 19

Figure 16: Due to mismatch of coefficient of thermal expansion (CTE) between layers, tensile strain is applied in GaN layer during cooling process on diamond substrates. [53] 20

Figure 17: Cross sectional transmission electron microscopies (TEMs) of GaN-Si and GaN-SiC with AlN buffer layer, and GaN-Diamond with an adhesion layer, which adds thermal boundary resistances [59, 60] 23

Figure 18: GaN, AlN, and AlGaN have wurzite crystal structures, whereas diamond has a cubic crystal structure 25

Figure 19: Grain structure in CVD diamond layers with a grain size that is initially very small and increases with film [69]. 25

Figure 20: Scanning electron microscope of CVD diamond sample. The columnar growth and increasing grain size from bottom to top are evident. Micrographs of the top sufaces of three samples are shown on the right [70]. 26

Figure 21: (a) Thermal conductivities of perpendicular and parallel to the plane of the film. (b) The lengths of the bars are proportional to the local conductivity in the schematic [70] 27

Figure 22: Thermal boundary resistance as a function of nucleation density [68].......................28

Figure 23: The process for forming a GaN HEMT epi-on-diamond composite wafer [63].........30

Figure 24: Cross sectional schematic drawings of GaN-on-diamond substrates with TEMs [65] a) utilizes an AlN nucleation layer to facilitate the growth of AlGaN/GaN on the diamond substrate while b) uses a diamond seed layer to grow a thick layer of diamond on the back side of the AlGaN/GaN layer. 30

Figure 25: Schematics of the AlGaN/GaN heterostructures (a) without and (b) with the AlN/GaN multi-buffer layer during growth (1200 °C) and during the cooling process [53] 31

Figure 26: (Top) Structure of AlGaN/GaN device with a heater source. (Bottom) Temperature rise in GaN and substrates, (a) GaN/SiC and (b)GaN/Sapphire with boundary due to self-heating that was measured by Raman spectroscopy (points) and determined from finite element modeling (lines). ΔT denotes the temperature discontinuity at the interface, and ΔT_{exp}, the experimental value [73]. 33

Figure 27: Cross sectional schematic for TDTR measurements of GaN-on-Diamond [62] 33

Figure 28: Two flip-chip designs: (Left) bumps are placed on the source, drain, and gate contact pad, (Right) additional bumps are placed directly on the source and drain ohmic contacts. In this way, there is direct thermal and electrical contact between the ohmic contacts and the metal pads on the AlN carrier [75]. 35

Figure 29: Schematic of heat flow through the cold plate. Usually water or other coolant flows through the cold plate. 35

Figure 30: Schematic of the die on a copper microchannel cooler that water can flow directly through the microchannels [77] 36

Figure 31: Energy level diagram for Rayleigh and Raman scattering processes 40

Figure 32: A schematic of a typical Raman spectrum of GaN showing with peak positions (ω) of two phonon modes (E_2(High) mode of strain-free GaN : ~568 cm^{-1} and

A_1(LO) mode of it: ~ 732 cm^{-1}), and the line-width, or full width at half maximum (FWHM, Γ). 42

Figure 33: Temperature calibration from the change in temperature to change in peak positions of the E2(High) and A1(LO) mode, and in linewidth of E2(High) mode of GaN. 46

Figure 34: Raman shifts vs. residual stresses obtained by XRD measurements. The slope of each curve is represented in Table 4 as K coefficients. [98]................................47

Figure 35: Schematic of experimental apparatus including spectrometer and peripherals used for characterizing AlGaN/GaN HEMTs: Renishaw Raman 50

Figure 36: Temperature of water used as a coolant, and that of the heating stage as a function of a power. Flow rate had to be increased to cool down the heat dissipating from the high power HEMTs. 51

Figure 37: (Left) Schematic of GaN on SiC / GaN on Diamond device [62] (Right) Experimental set-up: Thermal grease (Silicone-based zinc oxide filled polysiloxane) was applied in (1), between the heating stage and the copper mount, Silver-based thermal compound was applied in (2), between the copper mount and the package, where the thermal conductivity of it is 6 W/m-K. Also, bolts were screwed between the package and the copper mount, and between the copper and the heating stage to immobilize the device during the micro-Raman process..52

Figure 38: (Top left) 30 μm gate-to-gate spacing GaN on SiC; only edge of gate was accessible to measure, (Top right) 10 μm gate-to-gate spacing GaN on Diamond; edge of gate and center of gate were accessible, (Bottom left) Schematic of measured locations (Bottom right) 10 × 125 μm GaN HEMTs on CuMo bar on Cu plate. 55

Figure 39: Temperature calibration from the change in temperature to change in peak positions of the E_2(High) and A_1(LO) mode frequencies for GaN on SiC and GaN on Diamond devices. Both shows good linear relation between the temperature difference and Raman shifts for two different modes. 56

Figure 40: (Top) Temperature rise and (Bottom) thermoelastic stress of the center of channel at various power dissipation utilizing Raman thermometry techniques

of GaN on Diamond device compared with modeling results. Due to thermoelastic stress, the E_2(High) peak position underestimates the temperature obtained by 2-peak-fit method. The difference in temperatures indicates the amount of thermoelastic stresses, which was also obtained by 2-peak-fit method. 57

Figure 41: Measured (from A_1(LO) peak shifts method) and modeled operational temperatures of GaN on SiC and Diamond, where the modeling results are taken from [62]. 59

Figure 42: Schematic of 60 fingers AlGaN/GaN HEMT package for the thermal modeling: (Top) Quarter of whole package including copper mount, Cu/W package, solder, substrate, and GaN layer. (Bottom) Dimensions of a cross-section of a packaged device on a Cu heat sink (not to scale). Since the model is quarter, 30 heat sources were applied. Instead of dividing HEMT layer, AlGaN, GaN, and buffer layers were modeled as one layer. 65

Figure 43: The schematic of the simulated 3D structure with quarter symmetry. Various thickness of substrate will firstly investigated, gate-to-gate spacing, gate width, and then interfacial resistance, which includes thermal resistances of AlN buffer, adhesion layer between GaN and Diamond, and thermal boundary resistances will be studied lastly. 67

Figure 44: (a) Schmatic of cross-sectional of the device with ohmic contacts and SiN layer on top of the GaN layer (not to scale). Other package information is same as thermal modeling. (b) Boundary conditions of GaN HEMTs with a quarter symmetry: Heat source is given as an area and symmetry walls are considered as adiabatic and prescribed. (c) Unlike thermal modeling, 0.6 μm gold metal as source, gate, and drain are added and SiN passivation layer is added to consider the stress effects on GaN. Stresses were averaged through the probe in modeling to compare with the experiments, ...68

Figure 45: Maximum power density according to the commercilized device, (50 μm gate-to-gate spacing with 350 μm thick substrate), when limiting the maximum temperature to 500 K. 70

Figure 46: Maximum channel temperatures for various substrate thickness at 4 W/mm for 50 μm gate-to-gate spacing 71

Figure 47: Schematic of two different gate-to-gate spacing device with 200 μm thickeness substrate at 4 W/mm. The active area features sixty 2.5 μm long heating fingers; these fingers represent the device area where power dissipation is concentrated......72

Figure 48: Highest channel temperatures of different power density showing linear relation for various gate-to-gate spaicng with 200 μm thickness of diamond. 50 μm gate-to-gate spacing shows lower thermal resistance (39.7 mm-K/W) compared to 10 μm gate-to-gate spacing (28.6 mm-K/W) 73

Figure 49: 10 μm gate-to-gate spacing GaN on Diamond device shows lower temperature than 50 μm gate-to-gate spacing GaN on SiC, where both substrates are 200 μm thick...73

Figure 50: Temprature calculation for various gate-to-gate spacing to find the optimized thickness of diamond with the mimum temperature rise at 4 W/mm. Below its optimized thickness, the temperature rise rapidly, but ~200-300 μm thick, there is only <5 ℃ differences with the temperature of each optimized thickness. 75

Figure 51: Channel temperature of different gate widths for GaN on SiC and GaN on Diamond. 76

Figure 52: Peak and averaged channel temperature for different thermal resistances between GaN and Diamond, where the 50 μm gate-to-gate spacing device with 370 μm gate widths, and a 200 μm substrate thickness was used at 4 W/mm. 78

Figure 53: Temperature distribution through the thickness of GaN and its substrate. 79

Figure 54: Schematic of effects of CTE mismatch for epitaxial layers: (Top) If epitaxial layer is grown on higher CTE layer, the layer with lower CTE will experience tensile strain during heating, (Bottom) Vice versa..80

Figure 55: Operational thermo-elastic stress from the experiments; 10 μm gate-to-gate spacing GaN on Diamond and 30 μm gate-to-gate spacing GaN on SiC, and from the modeling; both 10 μm gate-to-gate spacing that SiC shows much higher stress since it has higher temperature rise than GaN on Diamond.................82

Figure 56: Differences in stresses when the same temperature rise is applied. Since the CTE mismatch of GaN and SiC is lower than that of GaN and Diamond, GaN on SiC has lower thermal stress. 82

Figure 57: (Top) Red spot indicates the underneath of the gate edge, where the stresses are calculated, (Bottom) Metallization adds tensile strain that total stresses are lower than Figure 55: ~50 MPa at 120 K and ~90 MPa at 180 K for both GaN on Diamond and GaN on SiC. 84

Figure 58: Stresses of x and y components are evaluated to confirm the bi-axial stress state in GaN layer to verify the 2-peak-fit method, where g2g stands for gate-to-gate spacing. z = 0 m is at the surface of SiN and GaN, and z = 2.171 m is at the surface of GaN and its substrate. 85

Figure 59: Schematic of the cyclic process of atomic layer depostion process on top of SiN passivation layer of AlGaN/GaN HEMTs. TMA is used as a pulsing precursor, then H_2O takes the methyl producing CH_4. Finally Al_2O_3 is formed on SiN layer on AlGaN/GaN HEMT. 89

Figure 60: (a) Two finger source-connected-field-plated (SCFP) AlGaN/GaN HEMT before ALD coating (b) After ALD coating (c) The thickness of the coated layer on top of the device. 91

Figure 61: Cambridge Fiji Plasma ALD system (Left), Cincinnati Subzero Micro Climate Humidity Chamber at 50 ℃ and 85 % RH (Right)..92

Figure 62: Schematic of experimental apparatus including spectrometer and peripherals used for measuring residual stresses of AlGaN/GaN HEMTs 93

Figure 63: (Left) PL is the phenomenon of light emission from a matter after the absorption of photons, (Right) PL spectra of GaN epifilms unde tensile and compressive stress [125]. 94

Figure 64: Schematic of depth of laser into AlGaN/GaN HEMTs showing that only visible laser penetrates GaN layer since the laser energy is lower than GaN Band-gap [125] 95

Figure 65: Devices were stressed from 10V_{DG} to 140V_{DG} in 2V increments for 60 s each step, where $V_{DG} = V_{DS} - V_{GS}$ at V_{DS} = 0V. (a) I_{Goff} vs. V_{DG}, where I_{Goff} is gate current after each stress at V_{GS} = -5 V, V_{DS} = 0.1 V, (b) $I_{Gstress}$ vs. V_{DG}, where

$I_{Gstress}$ is gate stress current during stressing, (c) $I_D/I_{D(0)}$ vs. V_{DG}, where I_D is drain current at V_{GS} = 2 V, V_{DS} = 5 V and $I_{D(0)}$ is drain current before stressing. 96

Figure 66: Transconductance (g_m) vs. V_{GS} (V) for time-dependent study in the humid condition: (a) Uncoated device, (b) ALD-coated device (Uncoated and coated devicces in laboratory air conditions are not shown here since both showed similar characteristics that have no changes as (b) shows, (c) maximum transconductance and threshold voltage (V_{TH}) extracted from (a)....................99

Figure 67: I_{DS} vs. V_{DS} curve comparing between fresh devices and stressed devices after 8500 s. (a) Uncoated device in the laboratory air condition, (b) ALD-coated device in the laboratory air condition, (c) Uncoated device in the humid condition, and (d) ALD-coated device in the humid condition....................100

Figure 68: Residual stresses of tested devices before stressing; each numbers corresponds to the tested devices; 13~16 are ALD-coated devices. The averaged value of all devices is ~500 MPa....................101

Figure 69: Decrease in residual stress as defects are formed, or lattice relaxation occurs. After a certain time, device blew up showing the lowest residual stress. 102

SUMMARY

AlGaN/GaN high electron mobility transistors (HEMTs) have appeared as attractive candidates for high power, high frequency, and high temperature operation at microwave frequencies. In particular, these devices are being considered for use in the area of high RF power for microwave and millimeter wave communications transmitter applications at frequencies greater than 100 GHz and at temperatures greater than about 150 °C. However, there are concerns regarding the reliability of AlGaN/GaN HEMTs. First of all, thermal reliability is the chief concern since high channel temperatures significantly affect the lifetime of the devices. Therefore, it is necessary to find the solutions to decrease the temperature of AlGaN/GaN HEMTs. In this study, we explored the methods to reduce the channel temperature via high thermal conductivity diamond as substrates of GaN. Experimental verification of AlGaN/GaN HEMTs on diamond substrates was performed using micro-Raman spectroscopy, and investigation of the design space for devices was conducted using finite element analysis as well. In addition to the thermal impact on reliability, environmental effects can also play a role in device degradation. Using high density and pinhole free films deposited using atomic layer deposition, we also explore the use of ultra-thin barrier films for the protection of AlGaN/GaN HEMTs in high humidity and high temperature environments. The results show that it is possible to protect the devices from the effects of moisture under high negative gate bias stress testing, whereas devices, which were unprotected, failed under the same bias stress conditions. Thus, the use of the atomic layer deposition (ALD) coatings may provide added benefits in the protection and packaging of AlGaN/GaN HEMTs.

CHAPTER 1: INTRODUCTION

1.1 Gallium Nitride HEMTs

The development of advanced RF-communication systems, such as satellite communications and radar systems as shown in Figure 1, are directly linked to the increased capability of the electronics used to transmit and receive data. In this space, the desire to increase both output power and operational frequency is limited, in part, by the semiconductor technology utilized [1, 2]. Increasing the capability of RF electronics requires materials with a high electron mobility, wide band gap, and large breakdown field, all of which can be found in gallium nitride (GaN)-based high electron mobility transistors (HEMTs) [3]. As shown in Table 1, GaN is advantageous in power/RF circuits with a large band gap of 3.4eV, which leads to a high breakdown field of 3.3 MV/cm allowing GaN-based devices to operate at high voltages, which is 10 times higher than that of Si or GaAs [4]. The high electric field saturation speed and the low parasitic capacitance of GaN allow high maximum operational frequency, which is advantageous in RF circuits. In addition, with high electron mobility, saturation drift velocity, and high maximum current allows high power to be achieved even though the electron mobility of Si or GaAs is higher than that of GaN as shown in Figure 2.

The high carrier concentrations and mobilities of AlGaN/GaN HEMTs are realized without the need for intentional doping unlike Si or GaAs. This is accomplished through the deposition of a thin layer of AlGaN on top of the GaN layer. A two dimensional electron gas forms due to the spontaneous and piezoelectric polarization, which attracts electrons to the GaN side of the interface between AlGaN and GaN. While these charges are confined near the interface, they can move laterally with high mobility which gives rise to the development of heterojunction field

effect transistors (HFETs). The hetero-structure of AlGaN/GaN features high voltage and high current, resulting in high power densities (>40 W/mm in RF, >7 W/mm in DC), high switching speeds (>160 GHz), and the ability of devices to operate at high temperatures greater than about 200 °C [5, 6]. Therefore, GaN-based semiconductors offer the promise of producing microwave electronic devices with RF power capability an order of magnitude greater than that available from comparable devices fabricated from other materials such as Si and GaAs [7].

Table 1: Comparison of the physical properties of important semiconductors for high voltage power devices [8, 9]

Material	Bandgap (eV)	Electron Mobility (cm^2/V-s)	Breakdown Field (MV/cm)	Saturation Drift Velocity ($\times 10^7$ cm/s)	Thermal Conductivity (W/cm-K)
Si	1.12	1350	0.3	1.0	1.5
GaAs	1.43	8500	0.4	1.2	0.5
GaN	3.39	900	3.3	2.5	1.3
AlN	6.10	1100	11.7	1.8	2.9

Figure 1: AlGaN/GaN HEMT applications: Satellite communication system, radar system, epitaxial GaN layer, and GaN electronics in hybrid electric vehicles [10-13]

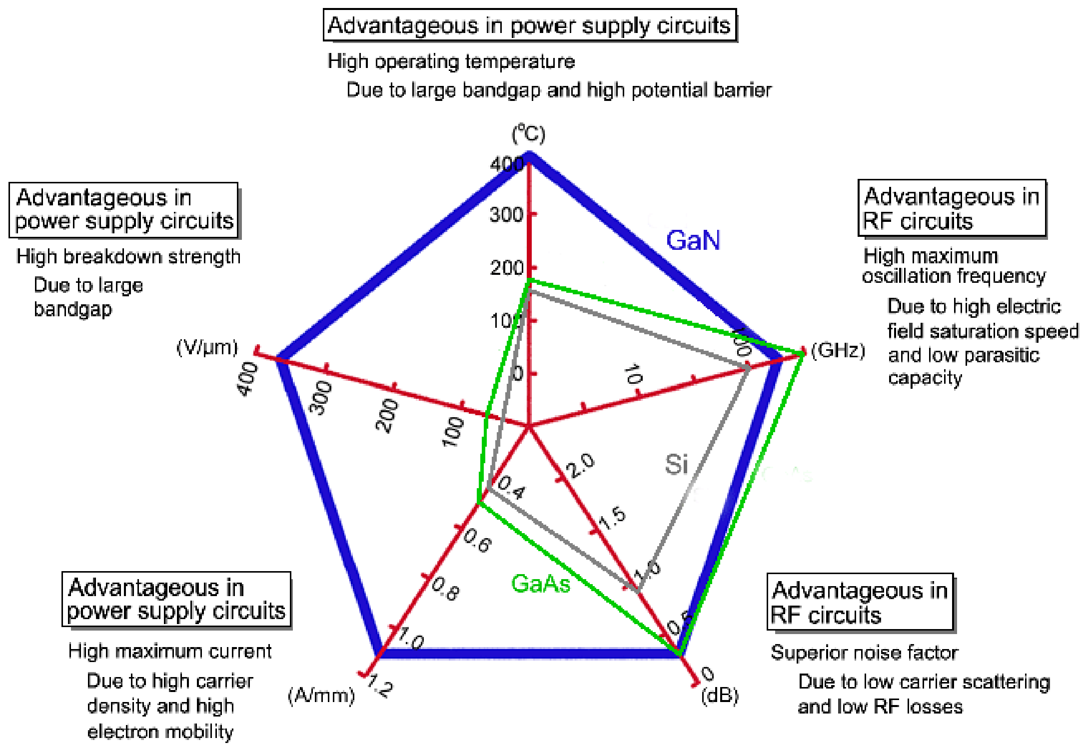


Figure 2: Main characteristics of GaN: high electron mobility, large band gap, and low parasitic capacity, which make GaN-devices advantageous in power and RF circuits [14]

1.2 Operating Principles of AlGaN/GaN HEMTs

HEMT or HFET devices have conductive channels formed by a conducting layer of free electrons at the heterointerface of a doped large bandgap semiconductor (e.g., AlGaAs) and an undoped smaller bandgap semiconductor (e.g., GaAs). Electrons from the edge region of the doped AlGaAs transfer into the lower bandgap semiconductor and gather in the quantum well that forms in the GaAs at the interface between the two materials. The electrons are confined in the quantum well, which has a thickness on the order of 20–30 Å. The distribution of the electrons in the quantum well is two-dimensional because the dimensions of the channel length and width are very large and the thickness of the quantum well is very small. Therefore, the charge density is termed a two-dimensional electron gas (2DEG) and is characterized as a sheet charge density with units of cm^{-2}. The sheet charge density for the AlGaAs/GaAs heterointerface is on the order of 2×10^{12} cm^{-2} [15]. The advantage of the 2DEG is that there are essentially no impurity atoms in the undoped GaAs and the quantum well, and the electrons in the conducting channel do not experience significant impurity scattering, permitting them to move with very high mobility, generally much greater than can be obtained in a bulk semiconductor material. In AlGaN/GaN, the carrier mobility is high, and the conducting channel resistance is very low, permitting HEMTs to produce high-frequency and low-noise performance.

The first AlGaN/GaN heterostructures were fabricated by growing thin AlGaN layers on thicker GaN material with neither the AlGaN nor GaN layers being doped [7]. Despite the lack of electrons from intentional doping, a 2DEG was formed at the heterointerface. The 2DEG has very high electron mobility (1,500 cm^2/V-s), high saturation velocity ($\sim 2 \times 10^7$ cm/s), and very high sheet charge density, on the order of $10^{13} \sim 10^{14}$ cm^{-2}, which is factor of five greater than produced in the AlGaAs/GaAs system [16]. Unlike AlGaAs/GaAs system, there is no

intentionally doped impurity to supply electrons that we need to know the source of the electrons that form the 2DEG.

The electrons that form the 2DEG result from the growth process. Since the AlGaN and GaN layer are both polar and piezoelectric material [17], the atoms in the AlGaN line up so that the positive side of the atomic layer lines up towards the GaN layer. As the layer thickness increases during the growth, the atomic layers continue to align, creating an electric field internal to the AlGaN layer, with the positive side of the dipole facing the GaN and the negative side of the dipole facing the growth surface that is called spontaneous polarization (Figure 3). In addition to the spontaneous polarization effect, during the pseudomorphic growth of thin AlGaN layer, the layer is forced to grow on top of the lattice-mismatched GaN layer as shown in Figure 4, where AlGaN has smaller lattice constant than GaN. The lattice constant of GaN is a = 3.189 Å and c = 5.185 Å, and that of AlN is a = 3.112 Å and c = 4.982 Å [17]. Therefore the AlGaN layer is under tensile strain to accommodate the lattice structure resulting in high piezoelectric polarization. Therefore, due to these spontaneous and piezoelectric polarizations, the magnitude of the electric field is very high, and is sufficient to ionize some of the covalent bonds by removing electrons as well as any impurities in the material. This high electric field will cause electrons to drift towards the heterointerface of AlGaN and GaN, where they fall into the quantum well, thereby creating the 2DEG. As the electrons move from the AlGaN into the GaN, the magnitude of the electric field is reduced, thereby acting as a feedback mechanism to quench the electron transfer process until no further electrons are transferred into the quantum well.

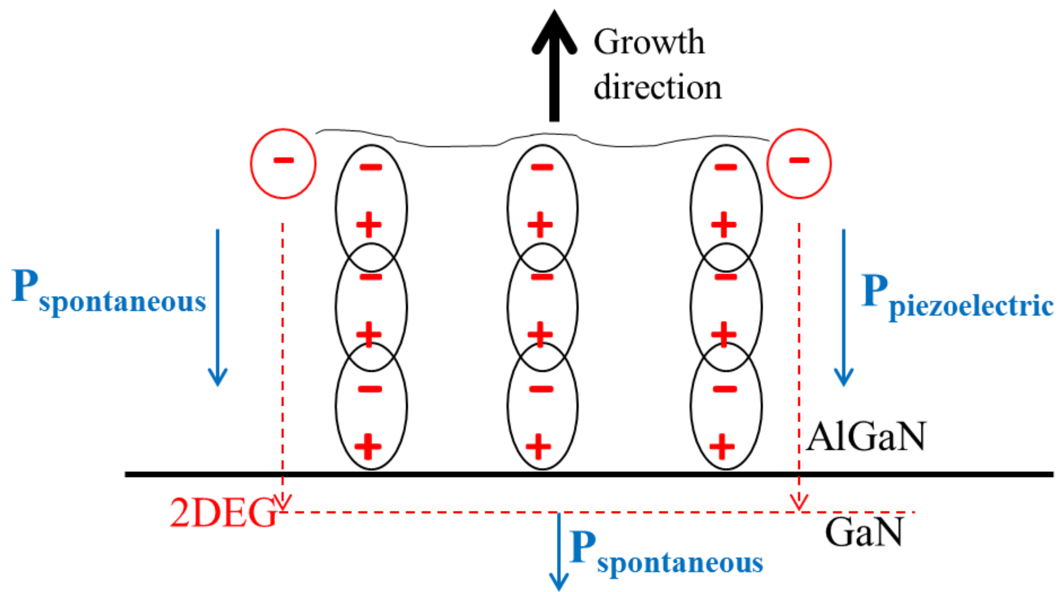


Figure 3: Formation of a 2DEG at the AlGaN/GaN heterointerface due to spontaneous and piezoelectric polarization effects

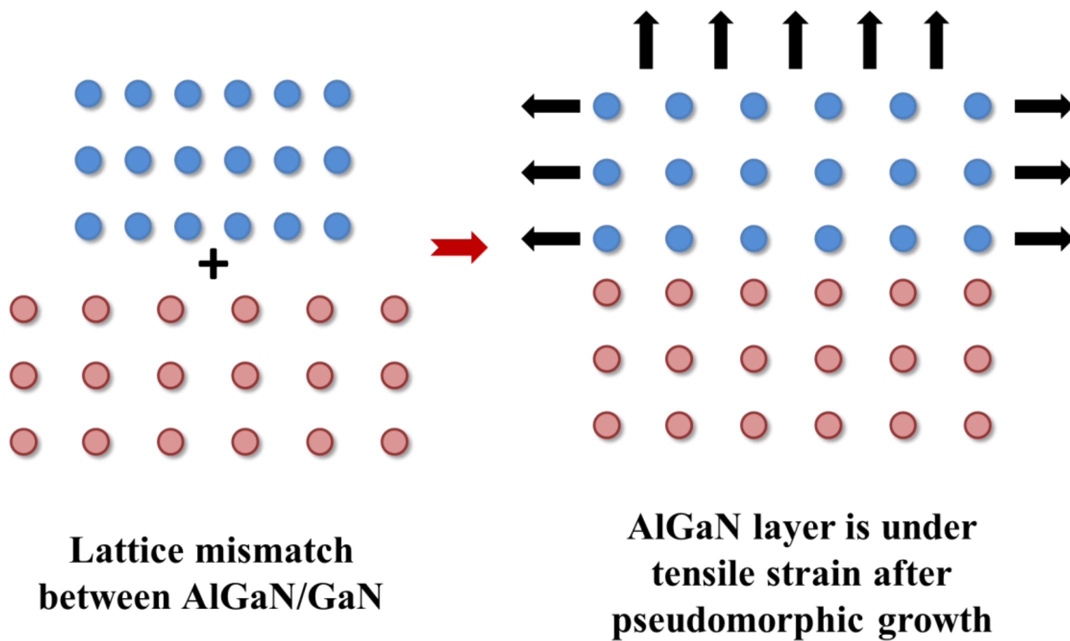


Figure 4: Illustration of pseudomorphic growth of AlGaN on top of GaN resulting in tensile strain due to the lattice mismatch between AlGaN and GaN

If the strain accommodation in AlGaN layer is not possible, then dislocation defects at the interface may form leading to relaxed film or the original lattice structure. Therefore, controlling the barrier film thickness of AlGaN and the Al concentration in the AlGaN has been used to control the density of the 2DEG [18]. If the $Al_xGa_{1-x}N$ barrier layer remains fully strained, where the Al concentration and the barrier layer thickness increase, the electron sheet concentration increases as well produced by the piezoelectric effect as shown in Figure 5. When the strained film (AlGaN layer) becomes thicker, the strain energy increases. Eventually, at one point, misfit dislocations form to reduce strain energy, i.e., lattice relaxation, at the expense of dislocation energy, so called the critical thickness. Once the barrier layer thickness exceeds the critical thickness, the elastic strain will decrease [19-23].

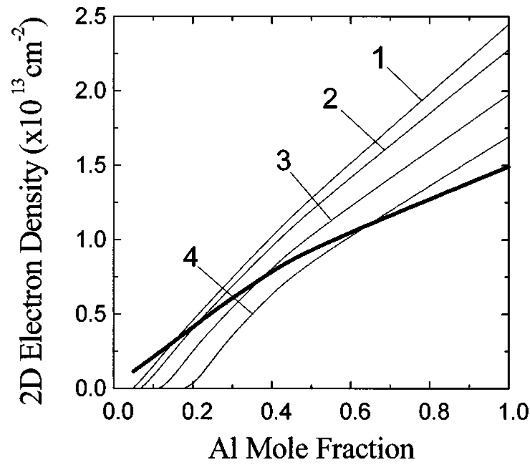


Figure 5: 2-dimensional electron sheet density induced by piezoelectric effect in $Al_xGa_{1-x}N/GaN$ heterostructures with different Al mole fraction and various AlGaN barrier layer thickness: 1–30 nm; 2–20 nm; 3–10 nm; 4–5 nm. Thick solid line shows the sheet electron density corresponding to a corresponding critical thickness of AlGaN for fully strained heterostructures as a function of aluminum molar fraction [18].

1.3 Reliability

Despite these benefits, GaN HEMTs have not been utilized widely in high-power applications because of concerns with their reliability. Since the performance of a device is limited only by the number of carriers and their ability to be transported, the high concentration and large polarization causing their formation are central to the capability of the device. However, even under typical device operating conditions, the output power as well as the drain current (I_D) decreases, and the device electrical characteristics can degrade as shown in Figure 6. The general electrical characteristics of AlGaN/GaN HEMTs are: output characteristics determined by I_D vs. drain-source voltage (V_{DS}), transfer characteristics by I_D vs. gate-source voltage (V_{GS}), which includes the information of threshold voltage (V_{Th}, the value of V_{GS} that allow I_D start to flow) and transconductance (g_m, the reciprocal of resistance or the ratio of the change in I_D to the change in V_{GS}), and gate current characteristics by the gate current (I_G) vs. V_{GS} showing the leakage current. Figure 7 shows these electrical characteristics for fresh and degraded condition. Obviously, after degradation, the performance of HEMTs, output and transfer characteristics, will decrease; I_D will drop, g_m will decrease, V_{Th} will increase, and leakage current will increase after degradation. Since GaN HEMTs are targeted to be operated at high power, high reliability is not only demanding but challenging. Therefore, appropriate designs are needed to maximize their reliability. While great studies have been made in the last ten years to understand degradation mechanisms in AlGaN/GaN HEMTs, a full understanding of this process has still not been obtained [24-30].

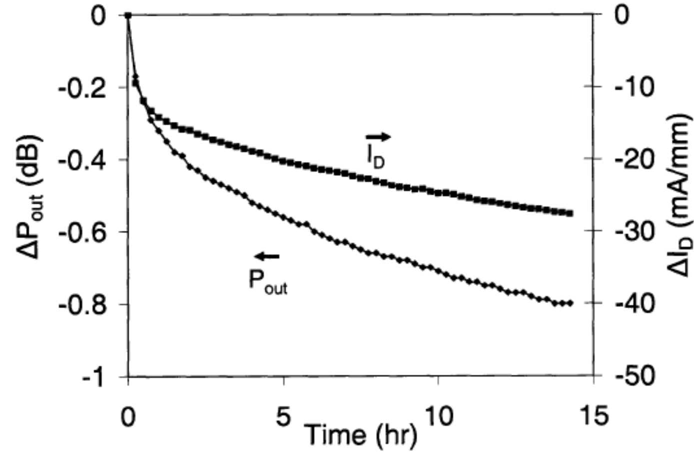


Figure 6: Decrease in the drain current (I_D) and the output power (P_{out}) during the time-dependent operation test [31]

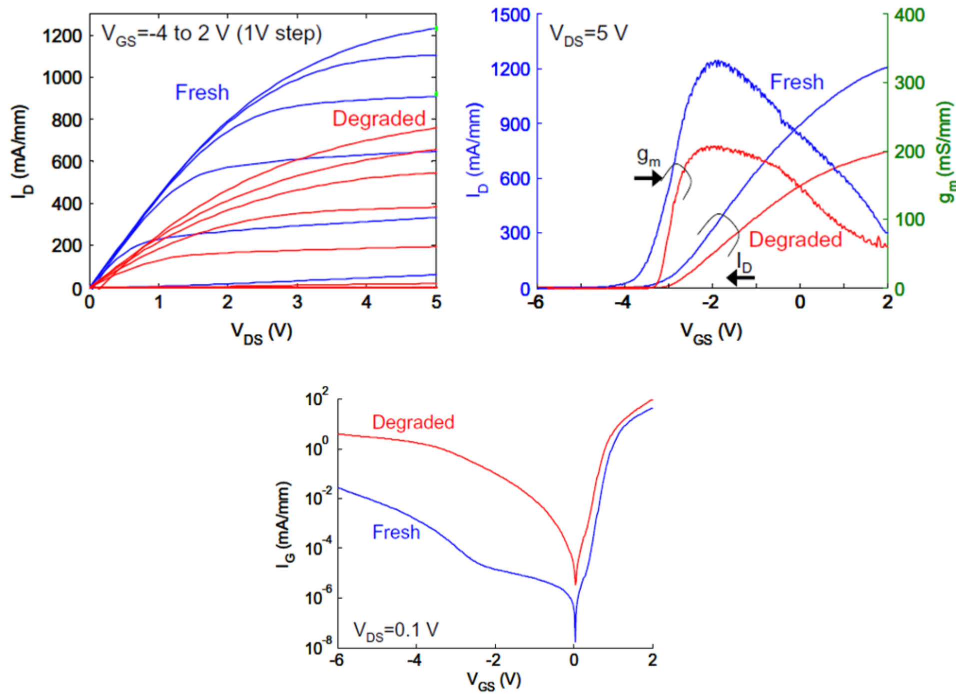


Figure 7: Change in device characteristics before (Fresh; blue line) and after stress experiment (Degraded; red line) [24]. From upper-left corner (clockwise): I-V output characteristics, transfer characteristics, and gate current characteristics, where I_D = drain current, V_{DS} = drain-source voltage, I_G = gate current, V_{GS} = gate-source voltage, g_m = transconductance.

1.3.1 Thermal Reliability

During the operation of AlGaN/GaN devices, electrons are accelerated down a potential gradient in the channel of the transistor and scatter with and emit phonons in the lattice. While this impacts the saturation velocity and mobility in the device, it releases thermal energy into the lattice of the AlGaN and GaN causing the temperature to rise. To be specific, most of the heat is dissipated by high speed electrons interacting with the GaN crystal lattice which causes the generation of high energy longitudinal optical (LO) phonons via Fröhlich interaction, which is a Coulomb interaction between electrons and the longitudinal electric field produced by the LO phonons [32], because of the strong ionic nature of GaN [33]. While the generation LO phonons is the primary energy loss mechanism of the electrons to the GaN lattice, the LO phonons have a low velocity which results in the thermal energy going into a phonon mode which contribute very little to the lattice thermal conductivity. These phonons must decay into lower frequency, fast moving phonons acoustic phonons, which contribute greatly to the thermal conductivity. Since there is a large difference in the mass of the Ga and N atoms, a large phononic bandgap exists which make the decay of LO phonons into LA and TA acoustic phonons more complex. The decay time of LO (~350 fs) is considerably longer than the time for electrons to generate them (~10 fs), thus, the emitted LO phonons remain in the channel until they either are reabsorbed by electrons or decay into other modes as shown in Figure 8 [34]. This phenomenon results in the phonon bottleneck in heat transport in GaN devices and is severe at the drain side edge of the gate, where the electric field is highest, and so called self-heating effect. This results in the localized accumulation of non-equilibrium LO phonons, or so-called hot phonons, which generates an intense hotspot in the channel of AlGaN/GaN HEMTs as shown in Figure 9 with cross sectional image. Understanding the complex phenomena of the nanoscale electrothermal

interactions in AlGaN/GaN HEMTs is still under investigation, but results from the combination of the electric field spike at the edge of the gate, complex phonon interactions, and ballistic-diffusive phonon transport effects [35].

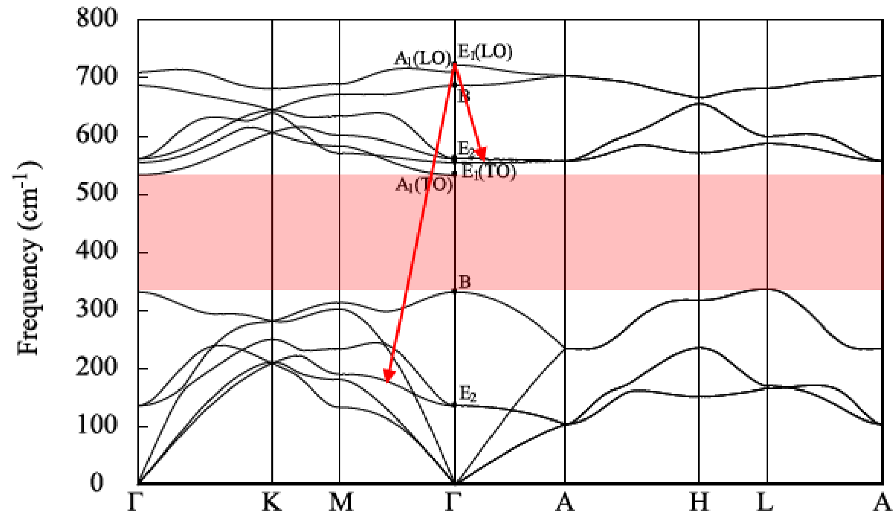


Figure 8: Phonon dispersion curves for GaN showing the decay of LO phonons into lower energy modes [36]

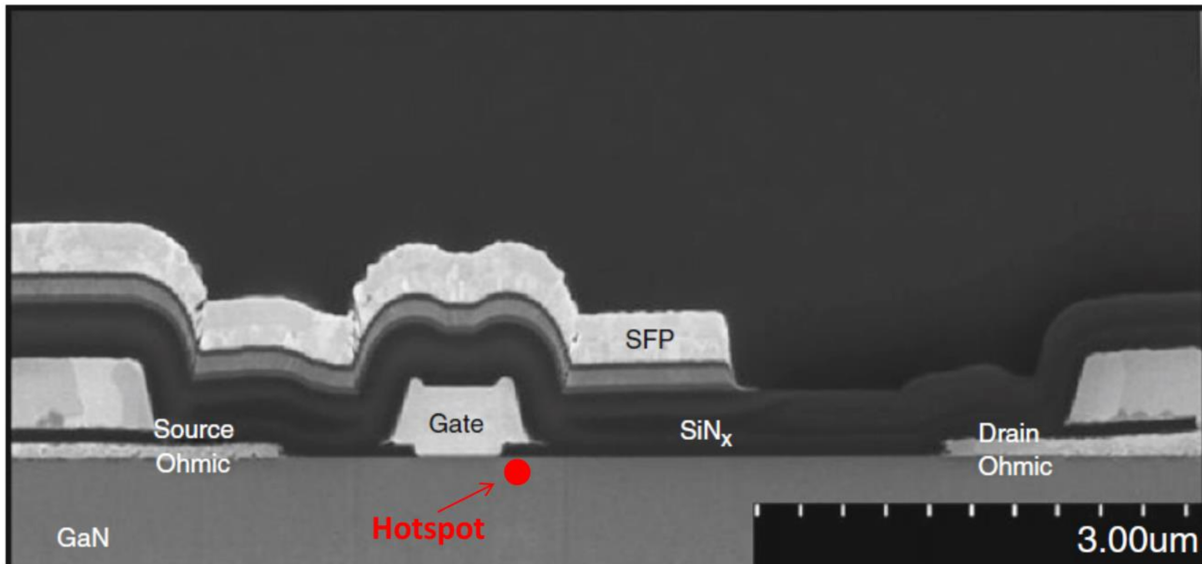


Figure 9: Cross section image of a GaN HEMT with the location of the hotspot in red dot [37]

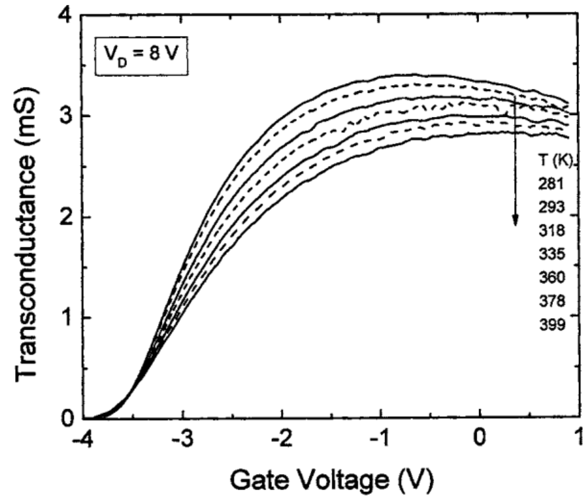


Figure 10: Decreases in transfer characteristic (g_m) as temperature increases [38]

The self-heating effect is also observable in the I-V characteristics, i.e., decreases in I_{DS} at large V_{DS} conditions or decrease in the transfer characteristics (g_m) as shown in Figure 10. Excessively high temperatures have the potential to degrade the stability of the gate (Schottky) and ohmic (source/drain) contacts of the transistor as well as form material defects, thus causing device failure or reliability problems. In its most simplistic expression, the failure rate of AlGaN/GaN HEMTs has been seen to follow an Arrhenius relationship, thus having the strong temperature dependence as shown in Figure 11. While degradation and failure of devices can occur under the application of large electric fields without any current flow (no heating), it is generally accepted that the introduction of elevated temperature can accelerate the failure of AlGaN/GaN HEMTs. Thus, control of the junction temperature is critical to improving the overall reliability of AlGaN/GaN HEMTs. While devices are projected to operate at temperature as high as 200°C, the high local heat fluxes (>1 kW/cm^2) and the high power densities desired for these devices (>7 W/mm under DC operation) means that the challenges of thermal management will remain a key instrument in improving the reliability of this technology.

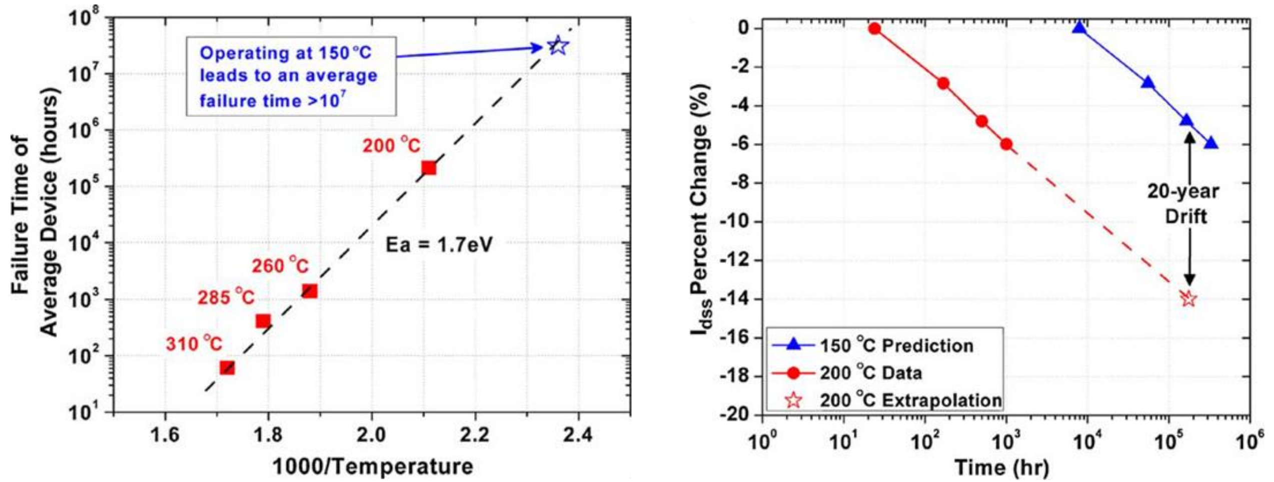


Figure 11: Arrhenius plot showing a Mean Time to Failure (Left) and the extrapolation data demonstrating 20-year drift with 50 ℃ difference (Right) [39]

To improve the reliability of AlGaN/GaN HEMTs, methods to reduce the junction temperature of these devices are necessary. The thermal management of AlGaN/GaN HEMTs can be conducted with the choice of substrates or the designing of the packages, which can dissipate heat well. In this study, utilizing high thermal conductive material, especially diamond, will be the main part that more detail about the methods to improve the thermal reliability will be discussed in Chapter 2.

1.3.2 Environmental Reliability

In addition to the temperature impact on reliability, environmental effects can also play a role in device degradation. It has been observed that during OFF-state voltage stress tests that pits and grooves in the vicinity of the gate can form which has been linked to trap generation, current collapse, and increased leakage current [24, 40, 41]. The current collapse is the result of electrons from the gate being trapped at the AlGaN surface states and acting as a virtual gate to deplete the 2DEG to make charge neutral [42, 43]. Although SiN_x passivation is widely used to prevent current collapse, the exact mechanism by which SiN_x passivation works is still unclear.

A lot of experimental studies have investigated the evolution of structural damage or defect formation mechanism due to the inverse piezoelectric effect because of the high vertical electric at the drain edge of the gate [24, 40, 44, 45]. In addition to the tensile strain due to the lattice mismatch between AlGaN barrier and GaN layer, the mechanical strain produced by the electric field increases the elastic energy in the AlGaN barrier. If this elastic energy exceeds a critical value, crystallographic defects are formed which become trapping sites for electrons as shown in Figure 12. To verify this critical value, step-stress-tests (Figure 13) have been performed in various studies such as high drain voltage (forward bias), high negative gate voltage (reverse bias), and time-dependent (Figure 14) stress tests [27, 44, 46-49]. As stress voltage increases, not only the lattice damage will occur after elastic energy reaches its critical value, but electrical degradation will also occur. The voltage where electrical degradation occurs is called the critical voltage [49]. After exceeding this critical voltage, Figure 13 shows a decrease in I_{Dmax}, drain current at V_{DS} = 5 V, V_{GS} = 2 V, increase in $I_{Gstress}$ = gate current during stress, I_{Goff} = gate current at V_{DS} = 0.1 V, V_{GS} = -5 V, and resistances of drain and source (R_D and R_S), which agrees with Figure 7 [49].

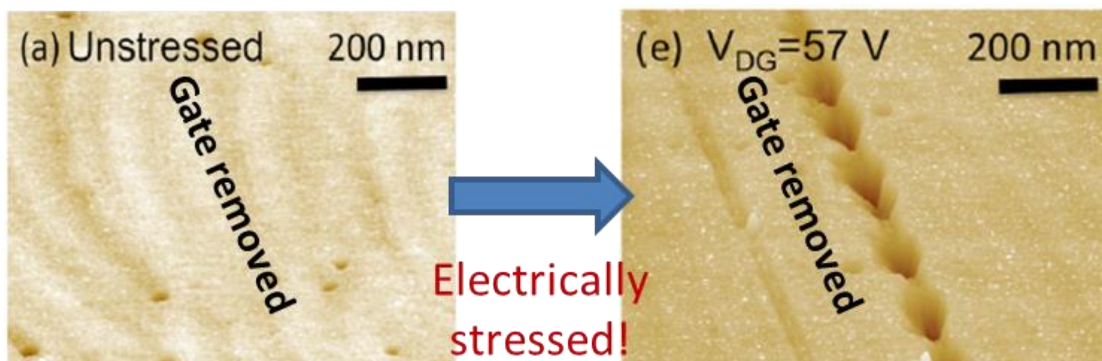


Figure 12: Gate metal was etched to characterize the exposed surface using AFM. The electrical degradation is closely related to structural damage at the gate edge of the device [40].

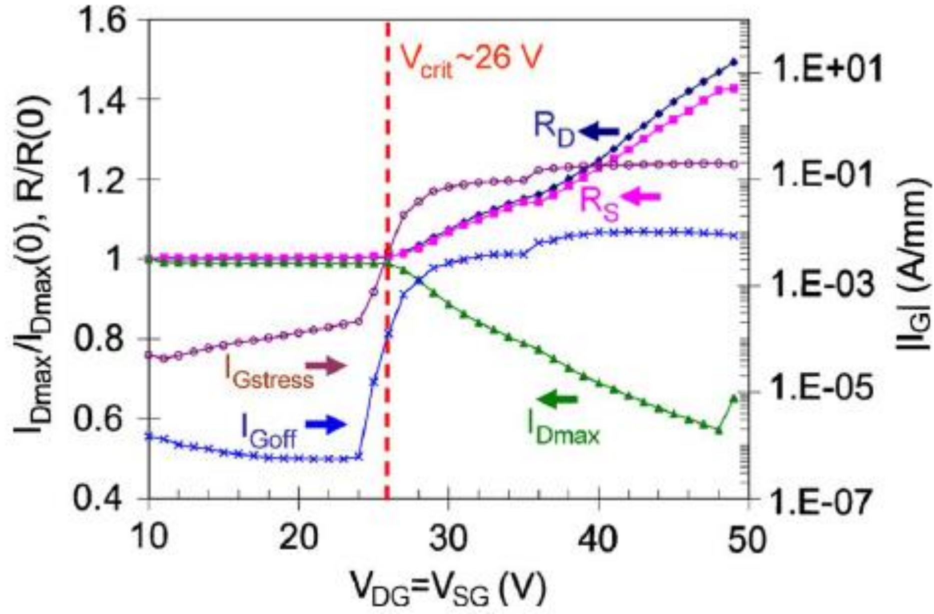


Figure 13: Normalized I_{Dmax}, R_D, R_S, $I_{Gstress}$, and I_{Goff} as a function of stress voltage in a step-stress experiment in the $V_{DS} = 0$ V state ($V_{DG} = V_{DS} - V_{GS} = 10 - 50$ V in 1V steps) [49]. After the critical voltage, I_{Dmax} decreases, R_D, R_S, $I_{Gstress}$, and I_{Goff} increase due to degradation.

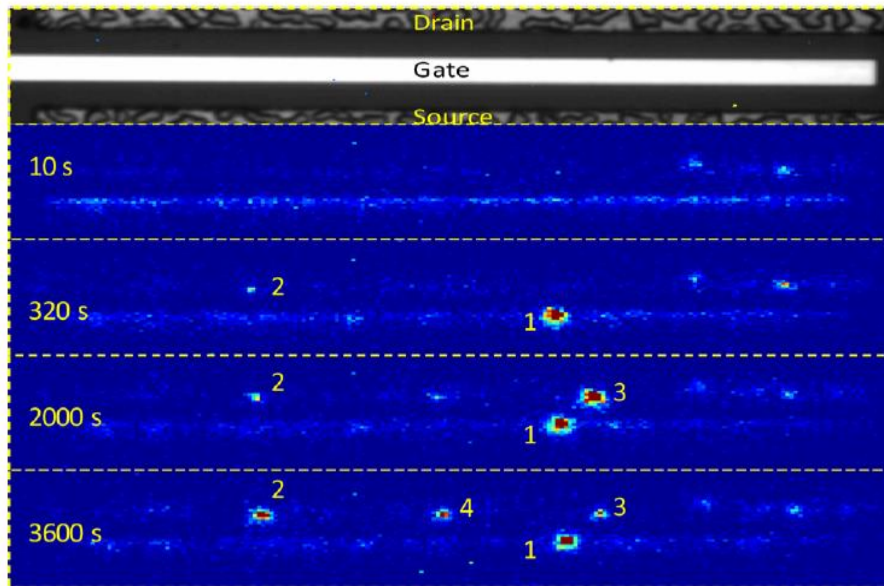


Figure 14: Results of the time-resolved Electroluminescence (EL) measurements carried out during stress at $V_G = -30$ V, $V_{DS} = 0$ V [46]. EL demonstrates that the increase in gate leakage current is correlated with the creation of discrete and very localized hot spots [50]. This figure shows, for sufficiently long stress times, degradation occurs even below the critical voltage (here, $V_{critical} = -35$ V).

It has been found that moisture or residual water molecules play a significant role in the DC-to-RF performance degradation of GaN-based HEMTs and the rate of degradation seen in step stress testing [30]. Previous data clearly show that the rate of degradation for HEMTs is different in air than other inert environments. An air ionization model was proposed to explain the suppression of current collapse in vacuum. The evidence of the strong role of oxygen diffusion and field-driven oxidation in the OFF-state degradation of GaN transistors has been found in other studies [29]. Other reports have also discussed the origin of the native gate oxide on the GaN surface and how oxygen-related traps can increase the gate leakage current [39, 51, 52]. In addition, a hydrophobic material was used to suppress the current collapse of AlGaN/GaN HEMTs [30], however, there was no discussion for the step-stress-test in the presence of water vapor.

These studies substantiate that one cannot emphasize too much the importance of an electronic packaging for environmental effects. The electronic packaging means the envelope of protection from surrounding such as oxygen and water vapor that affects the reliability. As achieving cost efficiency and high productivity is one of the key objectives of electronics, there are significant demands for small sized, hermetic cavity packaging technologies. Protection of devices from environmental exposure would help to improve device lifetime and reduce the demand on the package architecture and reduce the cost of devices.

1.4 Research overview

As discussed in Section 1.3, there are concerns regarding the reliability of AlGaN/GaN HEMTs in terms of the high junction temperatures that can be induced in the devices as well as their exposure to water vapor in the air from the environment. First of all, thermal reliability is the main concern that the hot spot with their high heat flux (>1 kW/cm^2) will degrade the device

as shown in Figure 11. Therefore, it is desirable to find the solution to decrease the temperature of AlGaN/GaN HEMTs in order to improve device lifetimes. This can be done through effective heat spreading near the active junction of the device where the hotspot forms and the heat is initially generated. In this study, we explored the methods to reduce the channel temperature in AlGaN/GaN HEMTs through building the devices on high thermal conductivity diamond substrates. As a base line study, GaN on SiC devices were used to compare with GaN on diamond device to elucidate the merit of using high thermal conductive material. Both experimental verification using micro-Raman thermometry as well as finite element modeling were used to explore the thermal design of AlGaN/GaN HEMTs on diamond substrates.

In addition to the thermal design, the effects of the environmental exposure of AlGaN/GaN HEMTs to water vapor can lead to shortened lifetimes and requires hermetic packaging. However, this can be relaxed upon the appropriate coating of the devices, allow for less stringent requirements on the sealing of the packages for AlGaN/GaN HEMTs. In this work, we explore the impact of environmental barrier films on the reliability of AlGaN/GaN HEMTs in humid environments. The incorporation of environmental barriers to improve device reliability is done through depositing conformal coatings using atomic layer deposition on devices and measuring their performance under large negative gate bias electrical stressing. These reliability studies propose the importance of packaging to protect from the environmental effects.

An outline from chapter 2 to chapter 6 is shown below:

Chapter 2 provides the methods to improve the thermal reliability of AlGaN/GaN HEMTs, and especially, the challenge of utilizing of diamond as GaN substrates is investigated. Chapter 3 overviews the experimental methodology of temperature measurements and the technique of Raman spectroscopy used in this study. It also presents the experimental set-up and the results of

the junction temperature of devices, made on high thermal conductivity substrates made from CVD diamond, which are compared to those made on SiC substrate. Then, Chapter 4 focuses on numerical modeling to show the impact of using high thermal conductivity diamond as a method to reduce the junction temperature, providing structural modification for better thermal design. Chapter 5 presents the use of ultra-thin coatings by atomic layer deposition (ALD) on AlGaN/GaN HEMTs as a method to reduce their susceptibility to degradation from water vapor in the environment. Electrical step stress testing was performed to measure the degradation in electrical characteristics and photoluminescence was performed to show changes in lattice relaxation. Chapter 6 states the final conclusions and proposes future work to further the development of the reliability of GaN HEMTs.

CHAPTER 2: BACKGROUNDS TO IMPROVE THE THERMAL REILABILITY OF ALGAN/GAN HEMTS

2.1 Utilizing High Thermal Conductive Substrates

As discussed in Chapter 1, the high heat flux in the device channel will degrade AlGaN/GaN HEMTs such that appropriate thermal management techniques are necessary to limit their temperature rise. Since the hot spot is generated below the gate edge at the drain side as shown in Figure 9, the thermal management of AlGaN/GaN HEMTs starts with the choice of substrate for the growth of the devices since the growth substrate is near the device channel and provides a mechanism for heat spreading as shown in Figure 15.

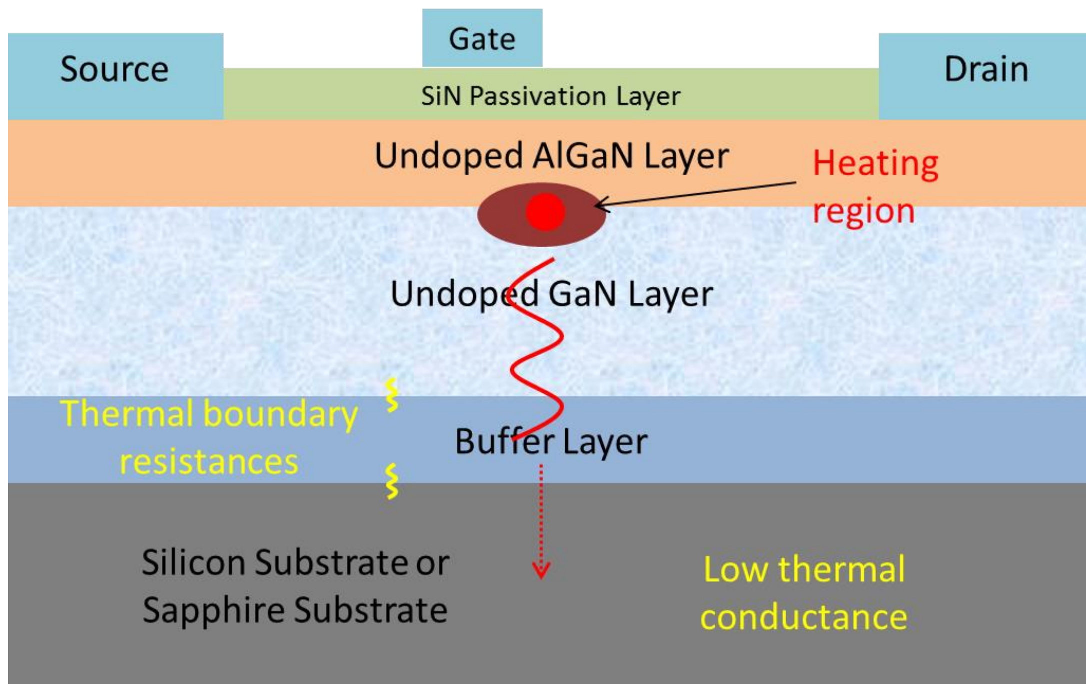


Figure 15: Schematic devcie structure with a diagram of thermal path through substrate, where thermal boundary resistances (TBRs) exist between GaN/buffer layer and buffer/substrate. Thermal conductivity of substrate and TBR play an important role to spread the heat out.

The choice of substrate material and the device design process should include properties such as lattice constants, coefficient of thermal expansion (CTE), thermal conductivity, thermal boundary resistance, electrical resistivity, and cost. If there is a lattice mismatch, which was explained in Figure 4, or CTE mismatch (Figure 16, Table 2) between GaN and the substrate, there is a possibility to form crystallographic defects. To decrease those mismatches, a buffer layer is grown between GaN and the substrate which gives rise to a thermal boundary resistance that is also important to heat dissipation. Having a higher thermal conductivity allows heat to spread out more easily, and a lower electrical resistivity is necessary to insulate from the active region of AlGaN/GaN HEMTs. Lastly, cost and availability are always a concern for the commercialization of the device.

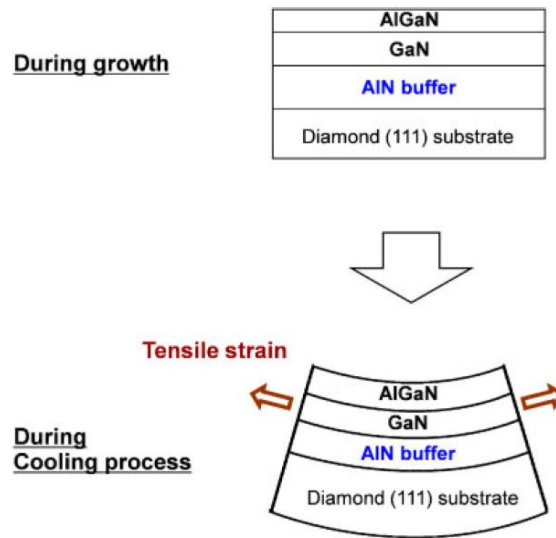


Figure 16: Due to mismatch of coefficient of thermal expansion (CTE) between layers, tensile strain is applied in GaN layer during cooling process on diamond substrates. [53]

Much of the early GaN HEMT research utilized sapphire (Al_2O_3) substrates, since the development and the production of sapphire as a substrate material has motivated the industry to develop GaN optoelectronic such as LEDs since 1993 [54]. However, the low thermal conductivity of the material (35 W/m-K) has largely relegated its use to GaN research today. Even during I–V sweeps, the self-heating will result in a reduced current at a high voltage, larger when compared to other competing substrate materials. More recently, cost-effective Si has emerged rapidly as well as high performance SiC as alternative substrates, leaving only a little viable interest in HEMTs built on sapphire substrates.

The long history of the development and modification of silicon has enabled the control of GaN-on-Si heteroepitaxy with low cost and considerable size. Applications for GaN-on-Si HEMTs have employed substrates across a wide range of resistivity. For example, p-type Si for power switching and intrinsic (float-zone, highly resistive) silicon for RF power amplifiers have utilized Si substrates [55]. Silicon has a reasonable thermal conductivity (149 W/m-K) that is similar to a thermal conductivity of bulk crystalline GaN, but inferior to a thermal conductivity of the chief competing substrate material, which is silicon carbide (6H-SiC: 490 W/m-K, 4H-SiC: 370 W/m-K). Furthermore, the lattice and coefficient of thermal expansion mismatches create a challenge to grow epitaxial GaN as shown in Figure 17. In general, none of the substrates used in AlGaN/GaN HEMT production are latticed matched with GaN. Therefore, buffer layers have been introduced to decrease the residual stress and the dislocation density from CTE mismatch and lattice mismatch. AlN is a common buffer material since it is also wurtzite in crystal structure similar to GaN and SiC, with a lattice constant closer to GaN. The thermal properties and lattice constants of key materials are summarized in Table 2, with the percentage of mismatches between materials and GaN.

Table 2: Properties of key substrate materials, AlN buffer layer, and GaN layer [8, 56, 57]

	Al_2O_3	Si	6H-SiC	Diamond	AlN	GaN
Thermal conductivity (W/m-K)	35	149	490	>1000	290	130
Lattice constant (a, Å)	4.758	5.431	3.080	3.567	3.112	3.189
Coefficient of thermal expansion (10^{-6}/K @ 300K)	6.66	2.60	4.30	1.50	4.15	5.59
Lattice (mismatch, %)	33	41	3.5	11	2.5	-
CTE (mismatch, %)	-20	53	23	73	26	-

With the higher thermal conductivity of SiC and wurtzite crystal structure similar to GaN, it is easier to nucleate and grow high-quality GaN-on-SiC with an Al buffer layer than on any other non-GaN substrate shown in Table 2. When AlN buffer layer is utilized between SiC and GaN, there is less than a 1% lattice mismatch between SiC and AlN. Therefore, misfit dislocations at the interface are separated by more than 30 nm, but are still in the range of $10^6 – 10^8$ /cm^2. This is due to the fact that the AlN/GaN interface mismatch of 2.5 % corresponds to a critical thickness for misfit dislocation generation of about 4 nm as shown in Figure 17 [58]. At this point, with its high thermal conductivity, SiC substrates are the most effective for suppressing the temperature rise in AlGaN/GaN HEMTs during high-power operation. However, the thermal

performance of SiC substrates is still limiting and more aggressive thermal management procedures are needed to full realize the potential of AlGaN/GaN HEMTs while limiting the junction temperature to less than 200℃.

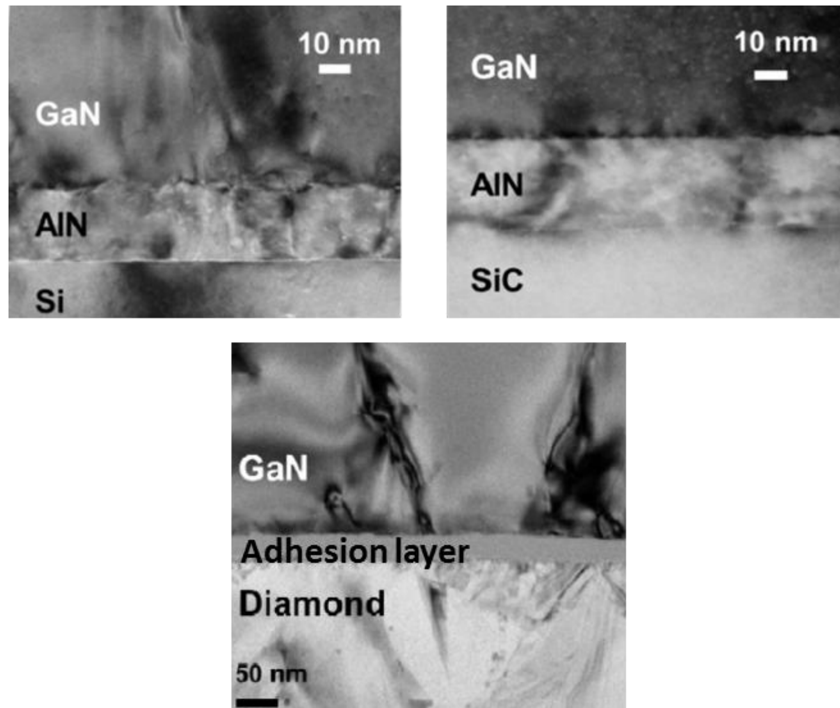


Figure 17: Cross sectional transmission electron microscopies (TEMs) of GaN-Si and GaN-SiC with AlN buffer layer, and GaN-Diamond with an adhesion layer, which adds thermal boundary resistances [59, 60].

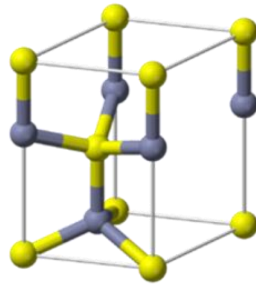
In contrast to SiC, nature's most thermally conductive material, diamond, provides a thermal conductivity that is approximately 3.5 times higher than that of SiC, making it an attractive option for thermal management. Therefore, several studies have investigated the use high thermal conductivity diamond substrates with a thermal conductivity ranging from up to 1800 W/m-K to provide solid state heat spreading in AlGaN/GaN HEMTs [61-65]. If AlGaN/GaN HEMTs on diamond are achieved, they will operate with the device temperatures

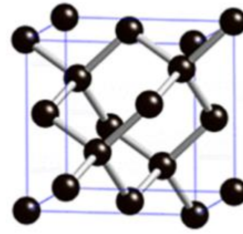
lower than SiC devices under similar power conditions or allow a reduction in the size of the devices while maintaining the same temperature. These improvements will ultimately improve the ability to increase the maximum output power as well as the thermal reliability of the devices. In addition, the substrate is right underneath the hotspot in the channel that moves a critical aspect of the thermal management solution (heat spreading) closer to the active region of the device.

In spite of its superior thermal performance, diamond has a different crystal structure, lattice mismatch, and CTE mismatch with GaN that make it difficult to grow GaN layers on top of diamond, even with the use of buffer layers. In addition to the use of buffer layers, the GaN layer can be transferred onto diamond films using an adhesion layer as opposed to growth as shown in Figure 17. The challenges of utilizing diamond will be discussed in the following section.

2.1.1 Integration of GaN on Diamond

The challenge remains in the integration of AlGaN/GaN devices with diamond. Unlike SiC in which the growth of AlGaN/GaN has occurred over the past 30 years, the integration of diamond with these devices is rather nascent in its development. In addition, because of the lattice mismatch and the CTE mismatch between GaN and diamond, it is difficult to grow GaN directly on top of diamond substrates. While SiC, Si, and sapphire are single crystal substrates, CVD diamond is polycrystalline and the lattice mismatch varies over the surface of the diamond, where GaN is wurtzite in structure as shown in Figure 18 that makes AlGaN/GaN heterostructure growth on diamond surface has been extremely difficult [66].





Wurzite Structure **Diamond Cubic Structure**

Figure 18: GaN, AlN, and AlGaN have wurzite crystal structures, whereas diamond has a cubic crystal structure

The deposition of diamond on non-diamond substrates that can be used to produce layers for AlGaN/GaN HEMTs produces a highly imperfect structure near the interface. The microstructural disorder yields a thermal resistance that can strongly impede passive cooling. Therefore, thermophysical property analysis is required to investigate not only the effect of grain size and nucleation density of diamond on its thermal properties, but also the thermal boundary resistance, which will be discussed later in this section [67-69]. The microstructure of a typical CVD film is shown in Figure 19 and Figure **20**.

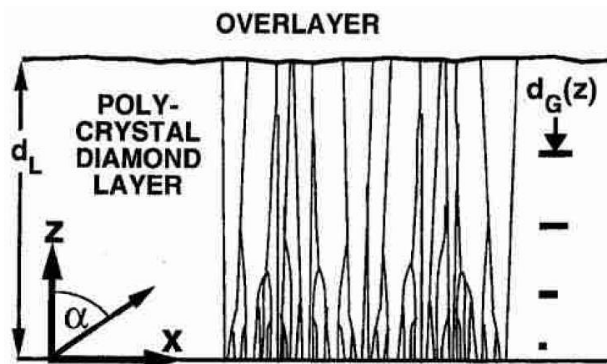


Figure 19: Grain structure in CVD diamond layers with a grain size that is initially very small and increases with film [69].

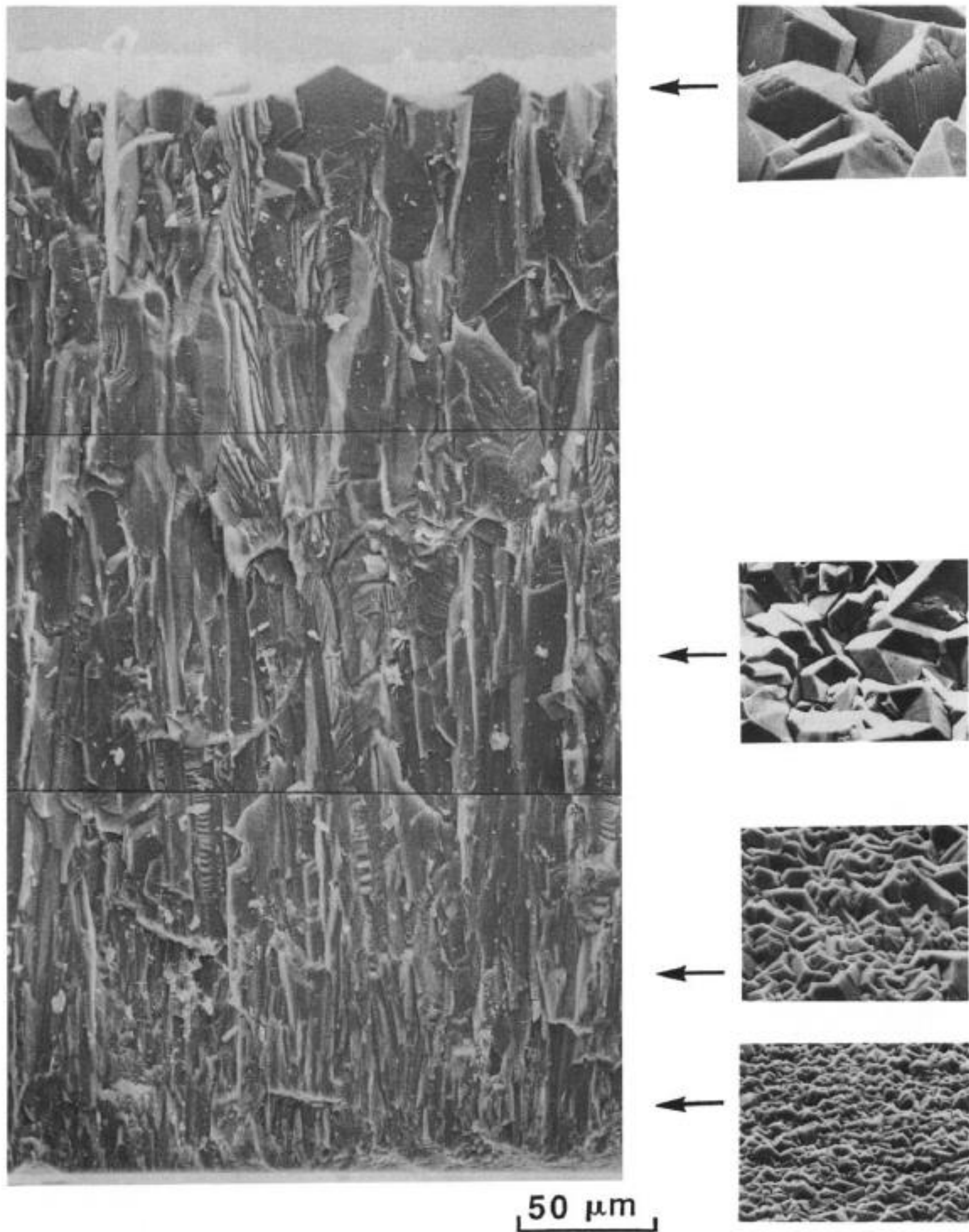


Figure 20: Scanning electron microscope of CVD diamond sample. The columnar growth and increasing grain size from bottom to top are evident. Micrographs of the top sufaces of three samples are shown on the right [70].

CVD diamond grows in a columnar structure with a grain size that is initially very small and increases with film that is shown in Figure 19 and Figure **20**. Because of the large anisotropy of the grain structure as well as the dependence of grain size on the height above the substrate, it may be expected that the thermal conductivity will be non-uniform vertically within the sample. We can explain the anisotropy by assuming that the impurities/defects tend to be located near grain boundaries. This would result in a significantly higher probability that a phonon incident on a grain boundary will be reflected rather than scattered isotropically. Thermal conductivities perpendicular and parallel to the CVD grain vs. height z from the bottom were calculated as shown in Figure 21. According to Figure 21, such decreased transmission through grain boundaries would impede parallel thermal transport more than perpendicular, providing a natural explanation for the anisotropy, showing 50 % lower thermal conductivity when the distance from the surface is lower than 100 μm [70]. It may be expected that a locally defined conductivity will depend on the position z as well as the direction of heat flow. After certain distance from the surface with sufficient size of diamond, for this case 300 μm, there was no effect of anisotropy.

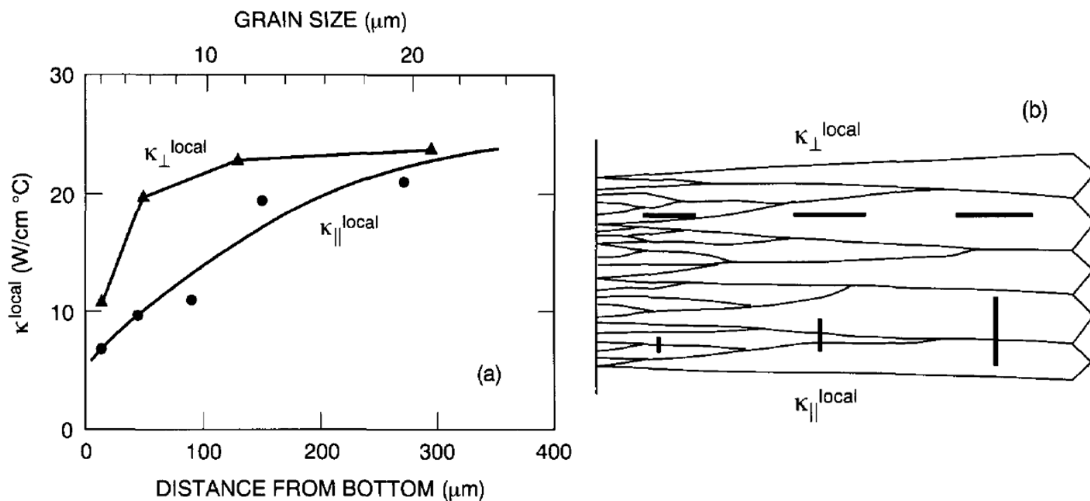


Figure 21: (a) Thermal conductivities of perpendicular and parallel to the plane of the film. (b) The lengths of the bars are proportional to the local conductivity in the schematic [70]

Figure 22 validates the importance of achieving the largest possible growth of grain dimension relative to the separation from the boundary. The large spatial lateral grain-size gradient results not only in a lower value of thermal boundary resistance (TBR), but also in an extension of the range of nucleation densities for which resistance is minimized [68]. It can be prove by Figure 22, at nucleation density of 10^{10} cm^{-2}, the spatial grain-size gradient with $\gamma = 0.4$ has 50 % lower TBR than $\gamma = 0.1$, whereas at nucleation density of 10^{12} cm^{-2}, the spatial grain-size gradient with $\gamma = 0.4$ has 75 % lower TBR than $\gamma = 0.1$.

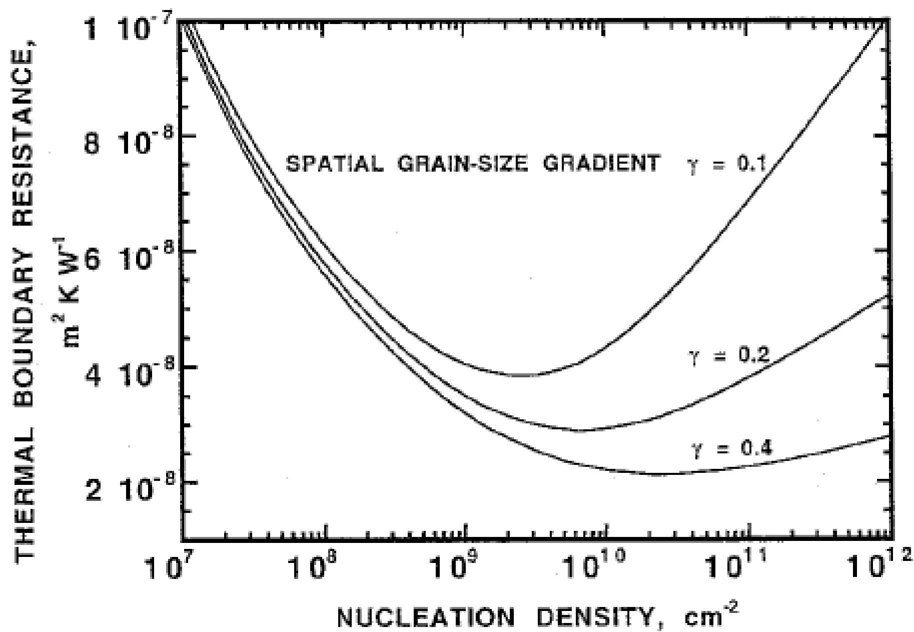


Figure 22: Thermal boundary resistance as a function of nucleation density [68]

Advancements in the development of the processing GaN on diamond devices have been achieved, which includes removing GaN from its growth substrate, usually Si (111), and bonding to GaN or use a multi-buffer layer to have fewer defects on GaN [53, 63, 66, 71]. In general, these methods provide a substrate with high thermal conductivity, but also thermal resistance at the interface between the GaN and the diamond. In addition, recent progresses shows the direct growth of GaN on a single crystal diamond (111) substrate with low thermal resistance [64]. Also, because of the high thermal conductivity of diamond, nanocrystalline diamond has been capped on top of AlGaN/GaN HEMTs to spread the heat [72]. Understanding how to design devices on these diamond substrates will take the advantage of high thermal conductivity of diamond, and realize the thermal resistance at the interface between GaN and diamond is lacking at this point and limits the effectiveness of this approach.

To build the wafer, previous studies started with GaN HEMT epitaxial layers (typically 2 μm thick) grown on SiC/Sapphire/Si substrate [63]. In order to preserve the orientation of the epilayers, which is required to fabricate HEMTs on this structure, they performed an epilayer transfer twice. They bonded the GaN-epilayer structure to another silicon wafer, which formed a SiC/Sapphire/Si-GaN-silicon wafer stack. The silicon wafer served as a sacrificial carrier for the GaN epilayers and allows them to be removed. The growth wafer is subsequently removed using a combination of grinding and selective dry etching, and then a CVD diamond wafer is attached to the flipped GaN epilayers using a 50 nm adhesion layer which is commercially proprietary. In the resulting structure, a thin GaN epilayer structure containing is deposited on a highly thermally-conductive diamond substrate, separated only by a thin dielectric adhesive layer [63]. The whole process is illustrated in Figure 23. Investigation of the adhesive layer as a thermally resistive layer will be conducted in Chapter 3. A photograph of a GaN wafer attached using an

AlN buffer layer similar to GaN on SiC growth as well as the use of a diamond seed layer on the backside of GaN are shown in Figure 24.

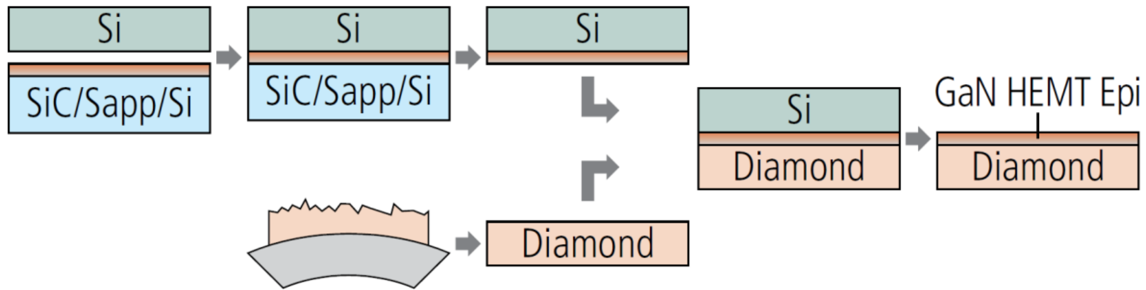


Figure 23: The process for forming a GaN HEMT epi-on-diamond composite wafer [63]

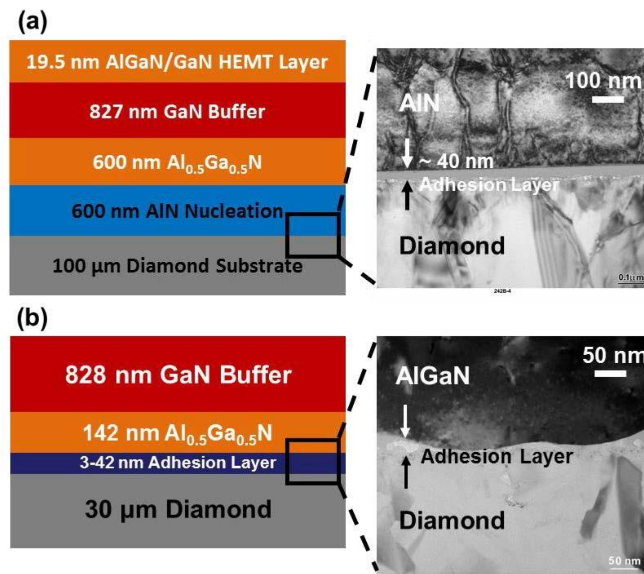


Figure 24: Cross sectional schematic drawings of GaN-on-diamond substrates with TEMs [65] a) utilizes an AlN nucleation layer to facilitate the growth of AlGaN/GaN on the diamond substrate while b) uses a diamond seed layer to grow a thick layer of diamond on the back side of the AlGaN/GaN layer.

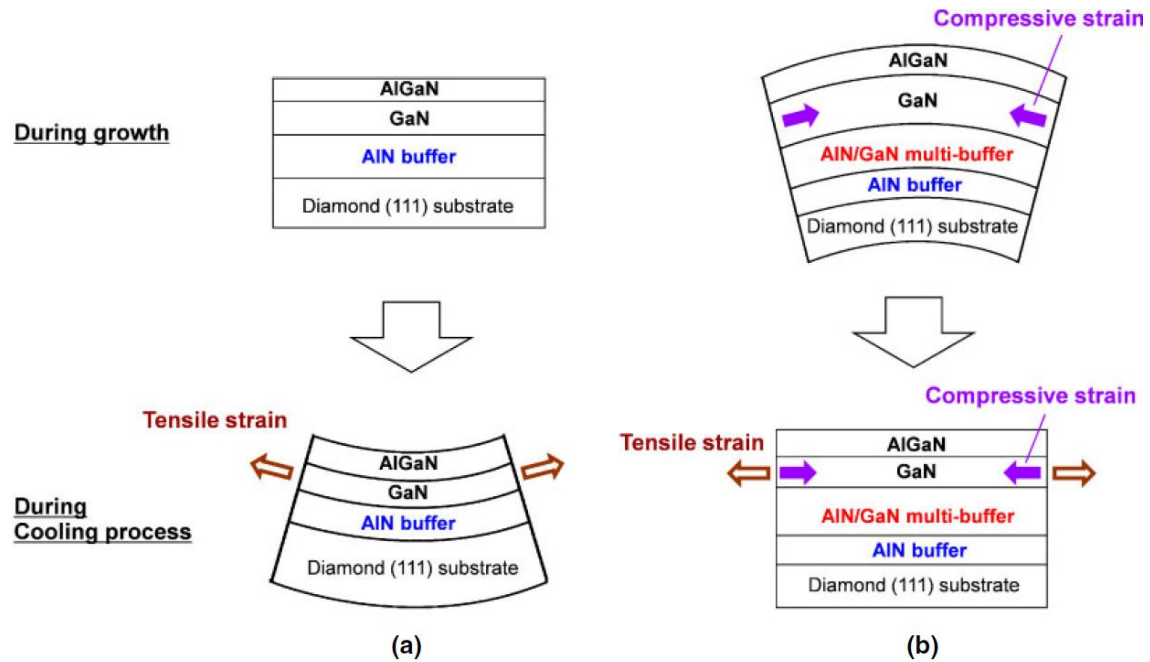


Figure 25: Schematics of the AlGaN/GaN heterostructures (a) without and (b) with the AlN/GaN multi-buffer layer during growth (1200 ℃) and during the cooling process [53]

In other studies, AlN/GaN buffer layers were used to prevent the crack formation in GaN layer. Because of not only the differences in lattice constants between GaN (a = 3.189 Å) and AlN (a = 3.112 Å), but the coefficient of thermal expansion (CTE) mismatch of GaN (3.2×10^{-6} K^{-1}) and diamond (1.5×10^{-6} K^{-1}), the averaged lattice constant of AlN/GaN buffer layer (a = 3.174 Å) will reduce the crack formation during the cooling process. Without the buffer layer, strong tensile strain is induced in the GaN layer during the cooling process and there is a high possibility of forming cracks to relax the strong tensile strain. In the AlN/GaN buffer layer, compressive strain is induced in the GaN layer by the AlN/GaN buffer layer during growth, then the compressive strain compensates for the tensile strain induced during the cooling process, and the AlGaN/GaN heterostructures with low crack densities are obtained on the diamond substrate as shown in Figure 25 [53].

Although there are a lot of techniques to grow or transfer GaN on diamond as discussed above, it is important to understand the effect of thermal boundary resistance (TBR) the GaN and diamond. In the presence of the heat flux across the boundary, this interface thermal resistance results in temperature discontinuity as shown in Figure 26. This difference results from the interface between the epitaxial films and their growth substrate that contains buffer layers and areas with a high concentration of defects and impurities [73]. Therefore, many studies have investigated to determine the TBR accurately using theoretical calculations and experimental methods [59, 62, 65, 73, 74]. There are two main metrologies to obtain thermal boundary resistances: Raman spectroscopy [73] and time-domain thermal reflectance (TDTR) [60, 62]. Raman spectroscopy extracts TBR from vertical temperature field in device as shown in Figure 26. The investigated devices have a 30 nm thick buffer layer with ~300 μm substrate (SiC and Sapphire) thickness [73]. The thermal conductivity of substrate is determined by temperature-depth measurements inside substrate. However, there are uncertainty contributions because of temperature averaging and assumptions of GaN thermal conductivity [73]. Nonetheless, the results of experiments were matched with the simulation, which TBR values were 33 and 120 m^2K/GW for GaN/SiC and GaN/Sapphire, respectively. The theory of Raman spectroscopy will be discussed more in Chapter 3. In picosecond TDTR, spatial and temporal distributions of optical heating pulses are well characterized as shown in Figure 27. To obtain the TBR, precise knowledge of material thickness and substrate thermal properties are required since temporal decay of surface temperature is governed by sub-surface properties. These samples have 828 nm GaN layer with ~28 nm buffer layers on 30 μm diamond, and a 50 nm aluminum transducer was applied on the top of the GaN, having TBR of 5 and 36 m^2K/GW for GaN/SiC and GaN/Diamond, respectively [65].The values of TBRs are summarized in Table 3.

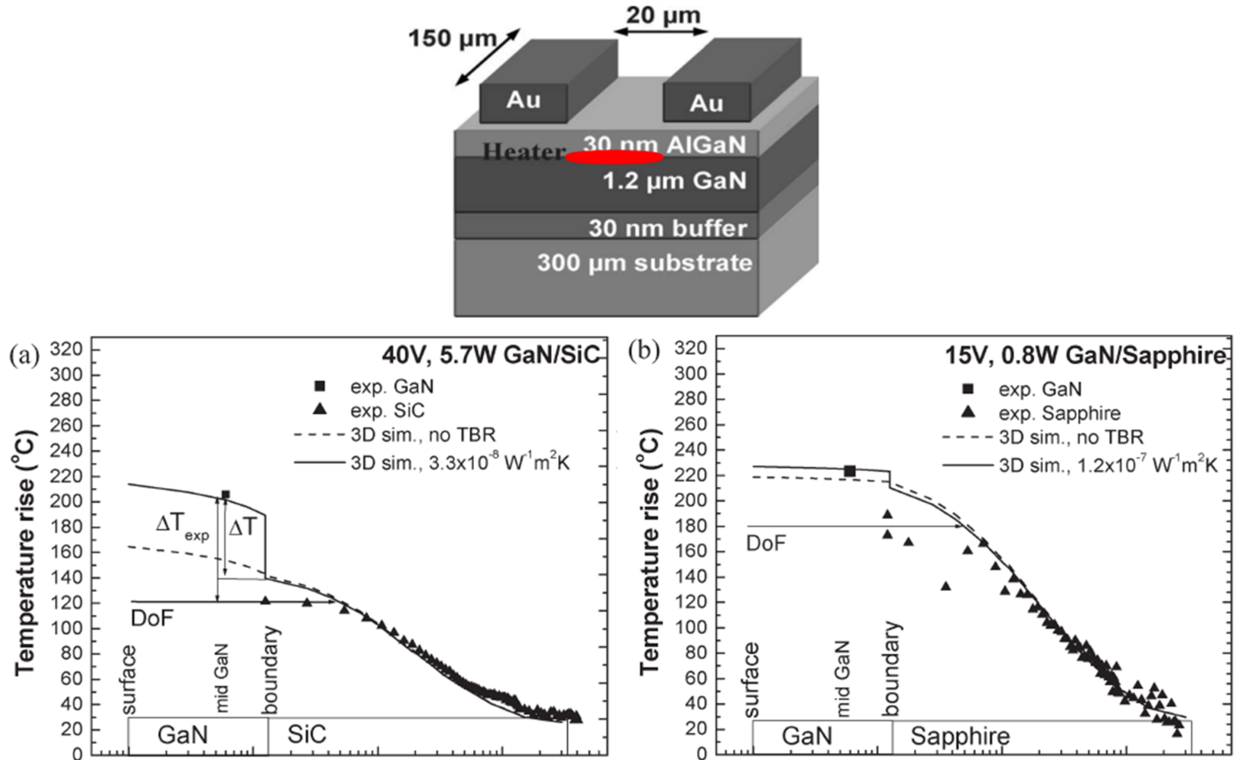


Figure 26: (Top) Structure of AlGaN/GaN device with a heater source. (Bottom) Temperature rise in GaN and substrates, (a) GaN/SiC and (b)GaN/Sapphire with boundary due to self-heating that was measured by Raman spectroscopy (points) and determined from finite element modeling (lines). ΔT denotes the temperature discontinuity at the interface, and ΔT_{exp}, the experimental value [73].

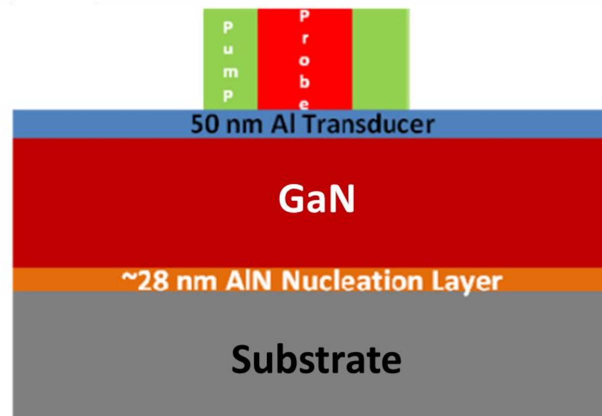


Figure 27: Cross sectional schematic for TDTR measurements of GaN-on-Diamond [62]

Table 3: Thermal boundary resistances between GaN and substrates

	Sapphire	Si	4H-SiC	Diamond
Thermal Boundary Resistance (m^2K/GW)	120 [73]	33 [73]	33[73] 4-5 [60]	48 [62] 36 [65]

2.2 Utilizing Thermal Packaging

Because of the low thermal conductance of conventional Si/Sapphire substrates, several methods have been investigated to lower the device temperature when utilizing these materials. Researchers have integrated the HEMTs onto an AlN carrier substrate with using flip chip bonding to dissipate the heat as shown in Figure 28 [75]. The AlN here is the preferred carrier substrate because of its high thermal conductivity (180 W/m-K at 300K). However, the contact area of the solder bumps that have a thermal conductivity as high as 50 W/m-K, limits the heat flow path and still provides significant thermal resistance to the thermal management technique.

Using a package, the chip is bonded substrate down onto a Cu/W frame using epoxy or solder attachment (e.g., AuSn), and cooled from the substrate side with a coolant through a cold plate as shown in Figure 29. Depending on the package attachment and other materials that may exist between the package and cold plate, additional thermal resistance in the heat flow path may be encountered. Overall, the thermal resistance of the commercial package has reported to be on the order of 60 K/W [76], but again is highly dependent on device and package design. For most high powered AlGaN/GaN devices, this is the standard methodology for their thermal management.

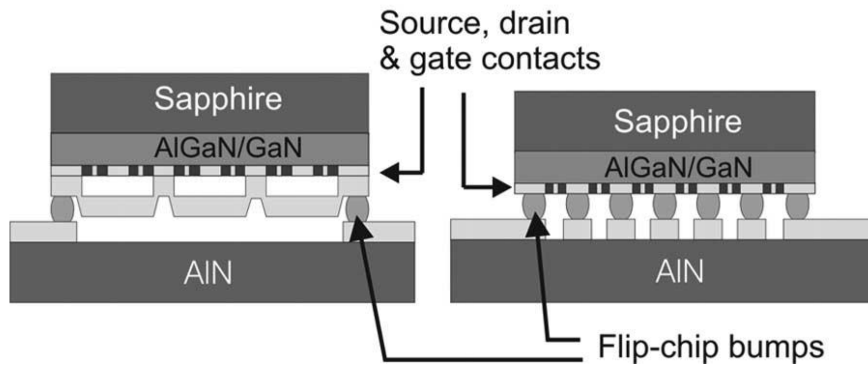


Figure 28: Two flip-chip designs: (Left) bumps are placed on the source, drain, and gate contact pad, (Right) additional bumps are placed directly on the source and drain ohmic contacts. In this way, there is direct thermal and electrical contact between the ohmic contacts and the metal pads on the AlN carrier [75].

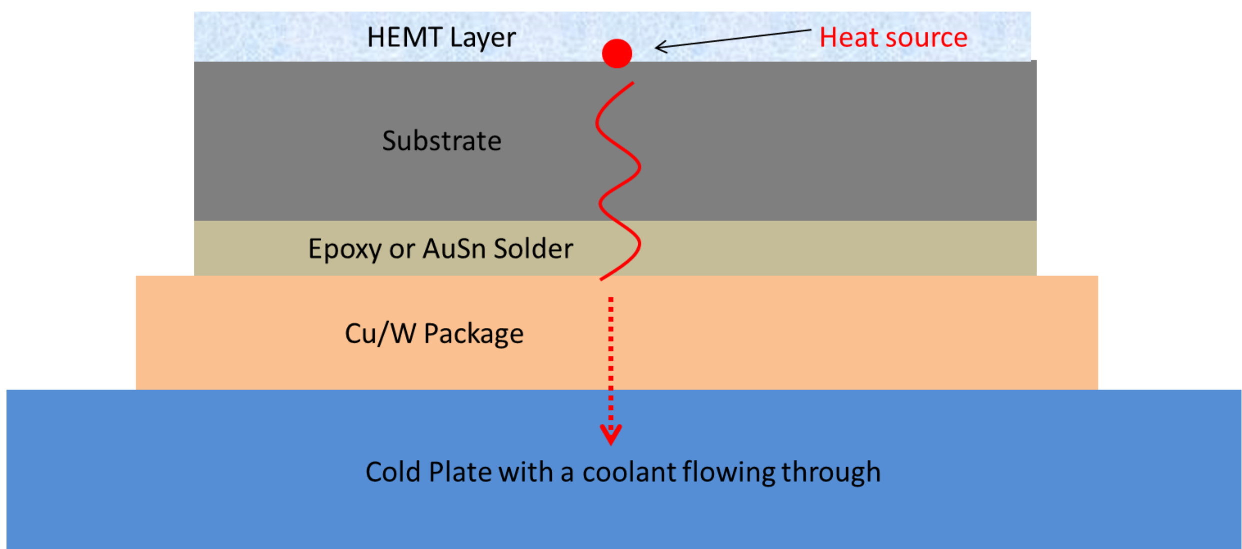


Figure 29: Schematic of heat flow through the cold plate. Usually water or other coolant flows through the cold plate.

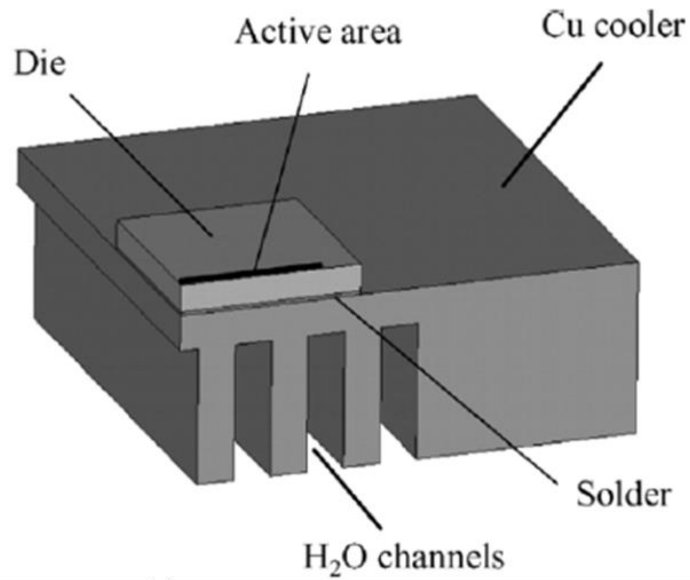


Figure 30: Schematic of the die on a copper microchannel cooler that water can flow directly through the microchannels [77]

Direct heat transfer from the chip surface using which is direct liquid cooling has been studied as well. Direct immersion cooling of a silicon substrate using Freon-12 was investigated [78]. For the GaN devices, ethanol was selected as the suitable volatile working fluid since its insulation properties and superior corrosion resistance, even though ethanol has a poor merit compared with water [76]. However, the size of the container is 15 mm in diameter and the lengths were 500 mm that will not fit to the appropriate micro-system and will be difficult to handle the coolant. Several means of increasing the critical heat flux of pool boiling with di-electric coolant such as FC-72 as the working fluid were investigated, as well as evaporative spray cooling, jet impingement cooling methods, two-phase flow in micro-channel heat sink, and various material was used for the micro-channel as shown in Figure 30 [77, 79-83]. Unlike the cold plate, micro-channel has more contact area with water, and thus more cooling power.

CHAPTER 3: EXPERIMENTAL METHODOLOGY OF TEMPERATURE MEASUREMENTS

3.1 Introduction

Accurate temperature measurement with high spatial resolution when applied to AlGaN/GaN HEMTs is a challenging research topic. Measurements down to the submicron regime are desired in order to capture both lateral and vertical thermal gradients (static and transient) in the transistor channels, where conventional methods are not able to make measurements. The development of a nanoscale thermometer is not only a matter of controlling the spatial resolution of the measurement technique, but also the development and improvement in the application of techniques and understanding their limitations. There are several application of techniques used to measure AlGaN/GaN HEMTs: time-domain thermo reflectance (TDTR) / thermo reflectance imaging, IR thermometry, DC characterization methods, scanning thermal microscope (SThM), and Raman thermometry.

TDTR is a method by which the thermal properties of a material can be measured such as thermal conductivity, which can be applied most remarkably to thin film materials (up to hundreds of nanometers thick), which have properties that vary drastically when compared to the same materials in bulk. The basic concept of this technique is to examine the change in the reflectance of the surface of a material while it is heated up that can be used to derive the thermal properties [59, 74]. Similarly, thermo reflectance imaging measures the reflected visible wavelength illumination to provide the surface temperature distribution with submicron spatial resolution, whereas IR thermometry has ~ 10 µm resolution. It was shown that IR thermometry underestimates the channel temperature of AlGaN/GaN HEMTs for several reasons [84]. Low resolution (~10 µm) limited by the wavelength of the radiation from the device surface,

emissivity calibration issues related with background radiation, and IR radiation is transparent to wide band gap materials, which limits the accuracy of IR thermometry [85]. DC characterization method can be utilized to measure the channel temperature of AlGaN/GaN HEMTs [86], which is a noninvasive and fast technique. However, it probes an electrical average temperature over a whole domain of the devices, thus the average temperature values from this method are significantly lower than the peak temperature of AlGaN/GaN HEMTs [87]. A scanning thermal microscope (SThM) operates by taking a sharp temperature sensing tip to near sample surface, which is utilized by the combination of an atomic force microscope (AFM) and a thermal probe. Then, the temperature of the tip is changed by localized heat transfer between the tip and the surface of the sample [88].

Raman spectroscopy provides non-contact and fast means to locally analyze micro-scale devices such as AlGaN/GaN HEMTs with sufficient high spatial resolutions of ~1 μm [89]. For micro and nano-scale semiconductor devices, sensors, and actuators, the goal is to measure temperature distributions resulting from electrical heating, e.g. self-heating effect in AlGaN/GaN HEMTs, with simultaneously high spatial and temporal resolution. In contrast to the scanning probe methods, most optical thermometry methods directly probe the micro device without requiring heat diffusion into a solid sensor, which eliminates the associated delay. Raman spectroscopy measures phonon frequency of semiconductor materials, which makes possible to measure both stress and temperature [90]. Therefore, Raman spectroscopy can serve as an effective tool for examining operating devices since interference to the electrical performance of the device by photon irradiation can be minimized by utilizing a sub-band gap visible laser. For these reasons, to compare the temperature between GaN on SiC and GaN on diamond HEMTs for the thermal reliability study, micro-Raman Spectroscopy is utilized for this study.

3.2 Micro-Raman Spectroscopy

3.2.1 Theory

Raman spectroscopy is a spectroscopic technique based on the inelastic scattering of monochromatic light with a material, usually from a laser source. In this method, photons are scattered by the sample elastically (Rayleigh scattering) or inelastically (Raman scattering) which results in a frequency shift in photons. The Raman scattering is based on molecular deformations in an electric field determined by the material's molecular polarizability. The photons can be considered as an oscillating electromagnetic wave with electrical vector. Upon interaction with the sample, it induces electric dipole moment, which interacts with the molecular vibrations.

Monochromatic laser light with frequency υ_0 excites molecules and transforms them into oscillating dipoles. Such oscillating dipoles emit light of three different frequencies (Figure 31) when:

1. A molecule with no Raman-active modes absorbs a photon with the frequency υ_0. The excited molecule returns back to the same basic vibrational state and emits light with the same frequency υ_0 as an excitation source. This type if interaction is called an elastic Rayleigh scattering.
2. A photon with frequency υ_0 is absorbed by Raman-active molecule which at the time of interaction is in the basic vibrational state. Part of the photon's energy is transferred to the Raman-active mode with frequency υ_m and the resulting frequency of scattered light is reduced to υ_0 - υ_m. This Raman frequency is called Stokes frequency, or Stokes scattering.
3. A photon with frequency υ_0 is absorbed by a Raman-active molecule, which, at the time of interaction, is already in the excited vibrational state. Excessive energy of excited Raman

active mode is released, molecule returns to the basic vibrational state and the resulting frequency of scattered light goes up to $\upsilon_0 + \upsilon_m$ This Raman frequency is called Anti Stokes frequency, or just Anti-Stokes scattering.

Since the energy loss or gained by the photons is directly related to the energy loss or gained by the phonon vibrational modes, this technique allows for the direct measurement of the vibrational energies of the zone centered phonons in the material.

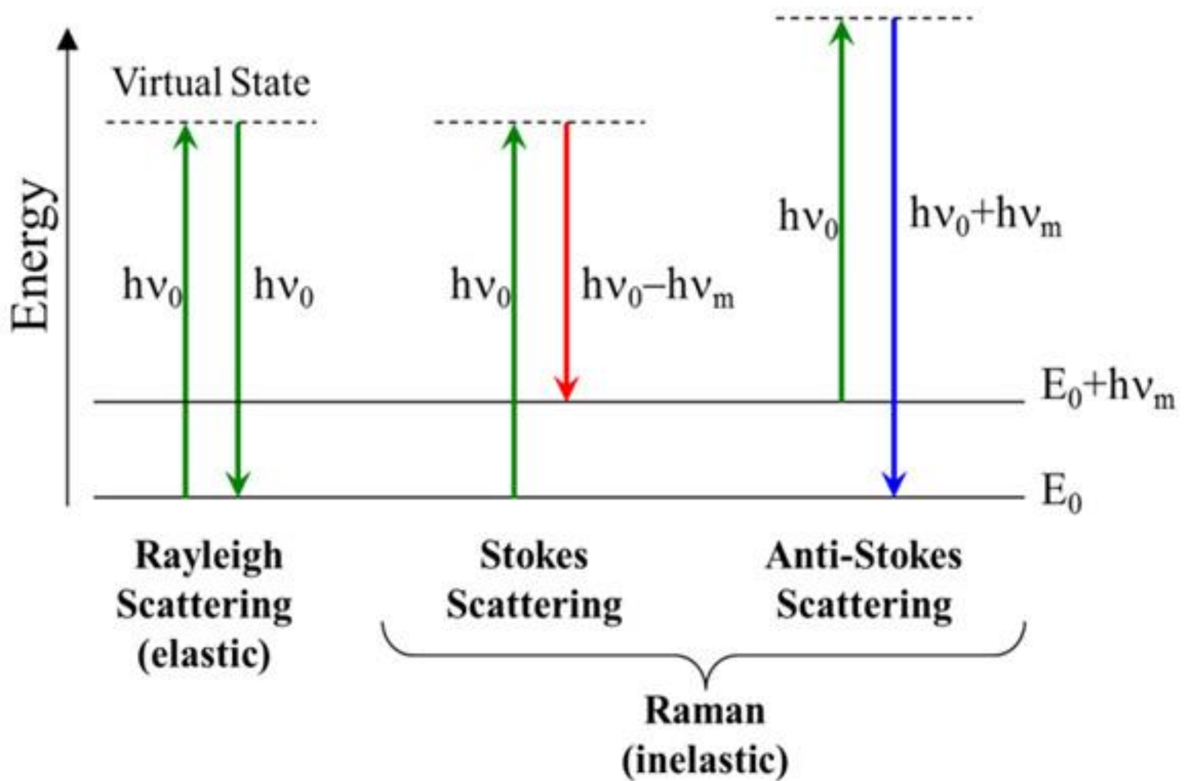


Figure 31: Energy level diagram for Rayleigh and Raman scattering processes

About 99.999% of all incident photons in spontaneous Raman undergo elastic Rayleigh scattering. Only about 0.001% of the incident light produces inelastic Raman signal with frequencies $\upsilon_0 \pm \upsilon_m$. Therefore, lasers are used as a light source that is capable of irradiation on a sample with very high photon density. Spontaneous Raman scattering is very weak and special measures must be taken to distinguish it from the predominant Rayleigh scattering. Instruments such as notch filters, tunable filters, laser stop apertures, double and triple spectrometric systems are used to reduce Rayleigh scattering and obtain high-quality Raman spectra.

3.2.2 Raman Thermometry

Temperature rise in the channel of AlGaN/GaN HEMTs can be obtained by the analysis of the changes in the vibrational characters (phonons). Therefore, any characteristics of the phonons, which vary with temperature, can be used to measure the thermal state of the system. For example, the change in Raman frequencies represents the change in temperature/stress states, and the change in line width of the peak, or full-width-half-maximum (FWHM), represents the change in temperature or quality of the crystal. Following Figure 32 shows the typical Raman spectrum of GaN, when it is heated or under tensile strain, the peaks show red-shifts, otherwise blue-shifts. For 180° back scattering geometry, GaN has E_2(High) and A_1(LO) Raman active modes.

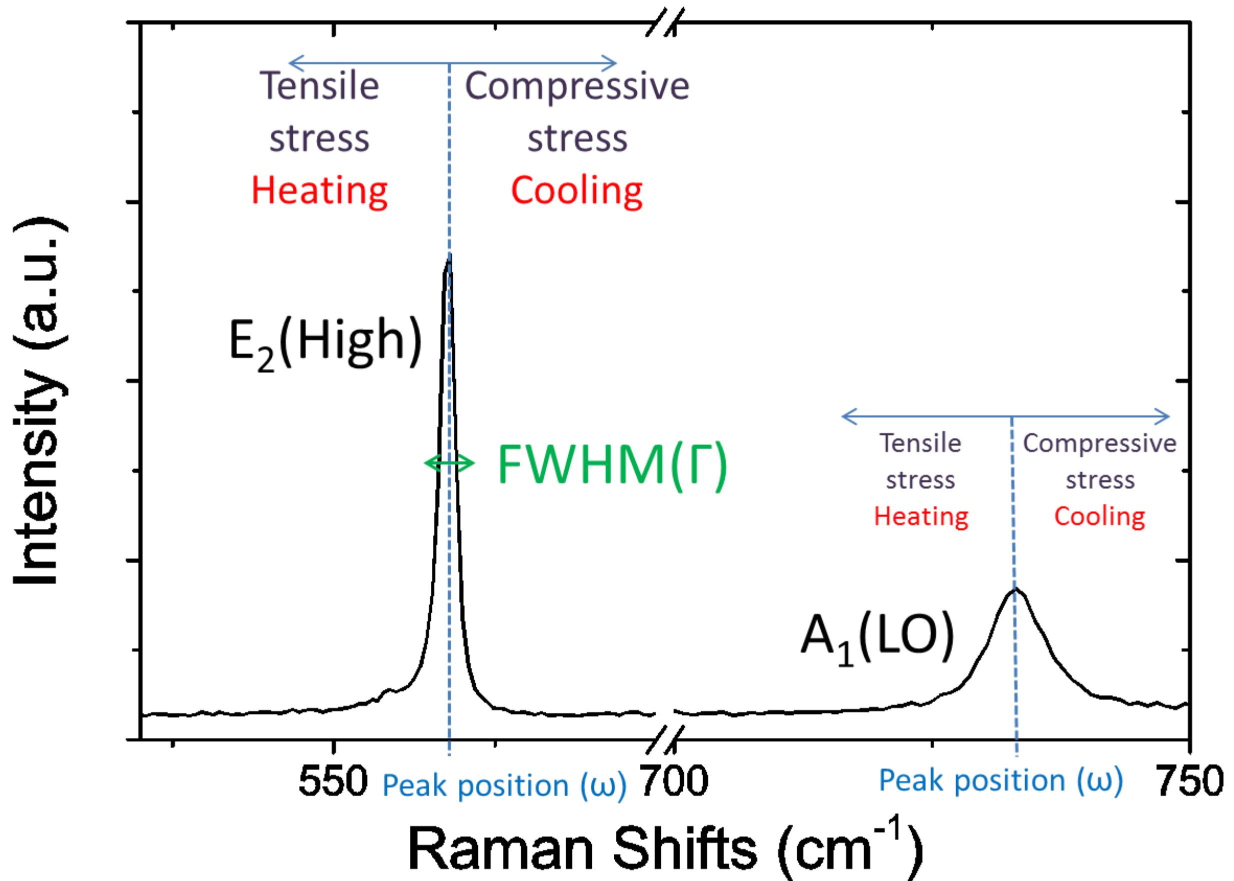


Figure 32: A schematic of a typical Raman spectrum of GaN showing with peak positions (ω) of two phonon modes (E_2(High) mode of strain-free GaN : ~568 cm^{-1} and A_1(LO) mode of it: ~ 732 cm^{-1}), and the line-width, or full width at half maximum (FWHM, Γ).

3.2.3 Peak Position Method

As the lattice is heated or cooled, the equilibrium positions of the atoms are displaced, resulting in a volumetric expansion or contraction of the lattice and a change in interatomic forces as a result of the anharmonicity of the bonds [91]. These changes in the interatomic forces modify the phonon vibrational frequencies that results in the change of the Raman peak position. Typically, the temperature dependent E_2(High) phonon frequency shift of Stokes Raman of AlGaN/GaN HEMTs is utilized [92].

However, temperature is not the only one that affects the peak position. As the volumetric changes, which contribute to peak shifts, result from the change of distances between the atoms, the peak position is sensitive to the lattice strain as well. During the operation of AlGaN/GaN HEMTs, thermo-elastic stress that comes from self-heating effect and inverse piezoelectric stress that is related with the magnitude of the vertical component of the electric field in GaN layer are developed.

Therefore, the shifts in phonon frequency include both temperature and stress effects. Utilizing peak shift method to obtain the operating temperature of AlGaN/GaN HEMTs underestimates it that it is necessary to consider not only the thermal effects but the other factors that could affect the Raman spectra.

3.2.4 Linewidth Method

The linewidth of a Raman peak results from the lifetime of the phonon. The lifetime of the phonons can be determined from the Heisenberg uncertainty principle which states that the energy of the phonon can be measured only for a finite amount of time. The dominant contribution comes from the thermal expansion that the increase in interaction among optical phonons at high temperature causing increased phonon scattering and decreased phonon lifetime. The linewidth of the phonon, Γ (cm^{-1}), is related with the phonon lifetime, τ, which can be described mathematically according to the energy-time uncertainty relationship:

$$\Gamma \sim \Delta E = \hbar / \tau \qquad (1)$$

where $\hbar$ = 5.3×10-12 $cm^{-1}s$ [93]. Therefore rise in temperature accompanies phonon peak broadening since life time is decreased. Scattering of the phonon is dependent on a variety features such as defects, material boundaries, and other phonons. Phonon-phonon scattering is a dominant factor in broadening of line-width since the phonon population increases with elevation

of lattice temperature, whereas other factors such as defects and grains are temperature independent. This increment in population reduces the phonon lifetime, and thus increasing the linewidth allowing temperature to be measured.

In AlGaN/GaN HEMTs, a pinch-off reference condition was used, in which the device is biased for peak position and linewidth method. At the pinch-off state, the current flow barely since the channel region near the drain is closed. Large internal electric fields occur during operation, and since piezoelectric materials are involved, piezoelectric effects in the polar direction of the crystal induce changes in the line-width [94]. Therefore, to minimize this electrical effect, which induce changes in the peak position and linewidth, the pinch-off state was employed as a reference state instead of an unbiased state to obtain the operational temperature [95].

3.2.5 2-peak-fit Method

While the peak shift method has lower measurement uncertainties than the linewidth method, the peak shift method is susceptible to the presence of thermoelastic stresses, which develop in the channel of the AlGaN/GaN HEMTs. For 180° backscattered Raman measurements on the c-plane of GaN, it is possible to see both the E_2 (High) and A_1(LO) modes as shown in Figure 32. Recently, researchers have utilized the shift in both peaks to measure the temperature rise in AlGaN/GaN HEMTs, which are corrected for thermoelastic stresses and which provide lower measurement uncertainty than the linewidth method [96, 97]. This method can be utilized by following equations:

$$\Delta\omega_{E2(High)} = A_{E2(High)}\Delta T + K_{E2(High)}\Delta\sigma$$

$$\Delta\omega_{A1(LO)} = A_{A1(LO)}\Delta T + K_{A1(LO)}\Delta\sigma \qquad (2)$$

where $K_{E2(High)}$ and $K_{A1(LO)}$, are linear coefficients for the stress-phonon frequency relations, are

obtained by X-ray diffraction and Raman measurements on high-quality GaN templates. And, $A_{2(High)}$ and $A_{A1(LO)}$ describe the linear temperature-phonon frequency relations, derived by performing Raman measurements on a high-quality HVPE GaN sample subject to known temperatures from room temperature up to 400 ℃ [98].

3.2.6 Calibration and Uncertainty

Raman thermometry starts with a calibration of Raman signal to the range of interested temperature. Each technique requires precise, accurate, and repeatable measurements that 20 measurements were conducted for each condition. To calibrate the device Raman response to temperature rise, peak shifts and linewidth broadens of Raman Stokes signals were collected. There was no power applied, and the temperature was uniformly increased to 25, 40, 50, 60, 70, and 80 ℃ using a temperature controlled stage with a temperature stability of ± 1 ℃. Then, the changes in the spectrum are fitted with Voigt function, which is a convolution of Lorentzian and Gaussian form, resulting in Figure 33. It shows the red shift of the E_2(High) and A_1(LO) modes of GaN in response to elevated device temperature. A linear fit was used to describe shifts in phonon frequencies with respect to change in temperatures. A second order polynomial did suffice to represent the relation between change in linewidths and change in temperatures from the reference condition, 25 ℃.

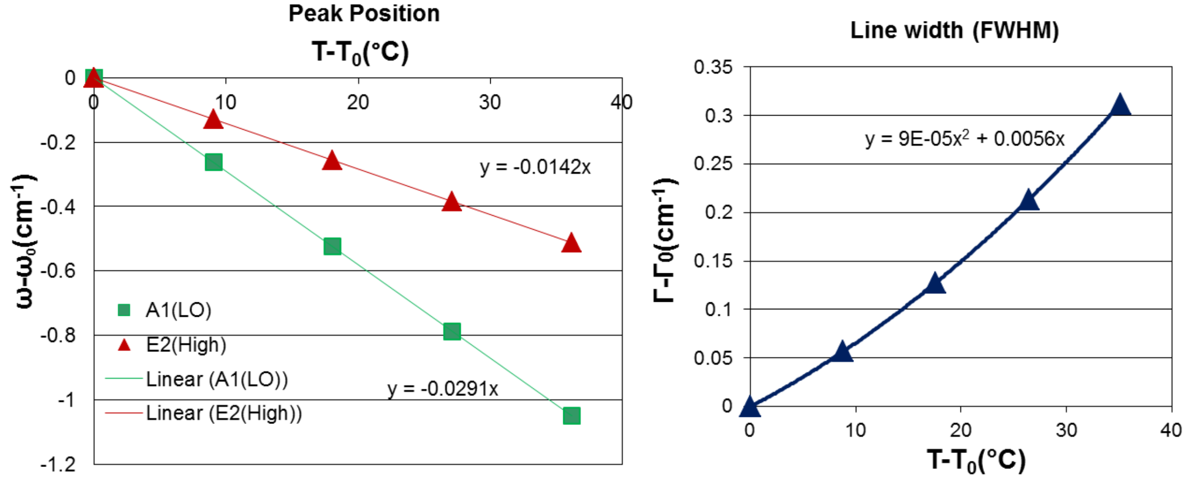


Figure 33: Temperature calibration from the change in temperature to change in peak positions of the E2(High) and A1(LO) mode, and in linewidth of E2(High) mode of GaN.

Through fitting these graphs, the slopes of shifts in peak position and temperature rise will be used as a constant for a single peak shift method, and second order polynomial fitting constant can be expressed as:

$$\omega - \omega_0 = A(T - T_0)$$

$$\Gamma - \Gamma_0 = B(T - T_0)^2 + C(T - T_0) \tag{3}$$

where, ω and Γ are the measured peak position and line-width at temperature T while ω_0 and Γ_0 are the reference peak position and line-width measured at the reference temperature of T_0, 25 °C. A, B, and C are calibration constants, which are given alongside their 95% confidence intervals, which can be found from Figure 33.

For the 2-peak-fit method, however, these calibration processes are not needed since the method relies on the intrinsic character of the material: response of phonon frequency from temperature increment or applied stress. Therefore, to utilize this method, relations between temperature/stress and the frequency shifts of the E_2(High) and A_1(LO) phonon modes of GaN need to be determined.

The linear coefficients for the stress–phonon frequency relations in equation (2) were obtained by conducting X-ray diffraction (XRD) and Raman measurements on diverse high-quality UID GaN templates. The linear temperature-phonon frequency relations were derived by performing Raman measurements on a high-quality HVPE GaN sample subject to known temperatures within the range of room temperature up to 400 ℃ [97]. From these measurements, following Figure 34 was obtained, and then the slope was obtained for the coefficients as shown in Table 4.

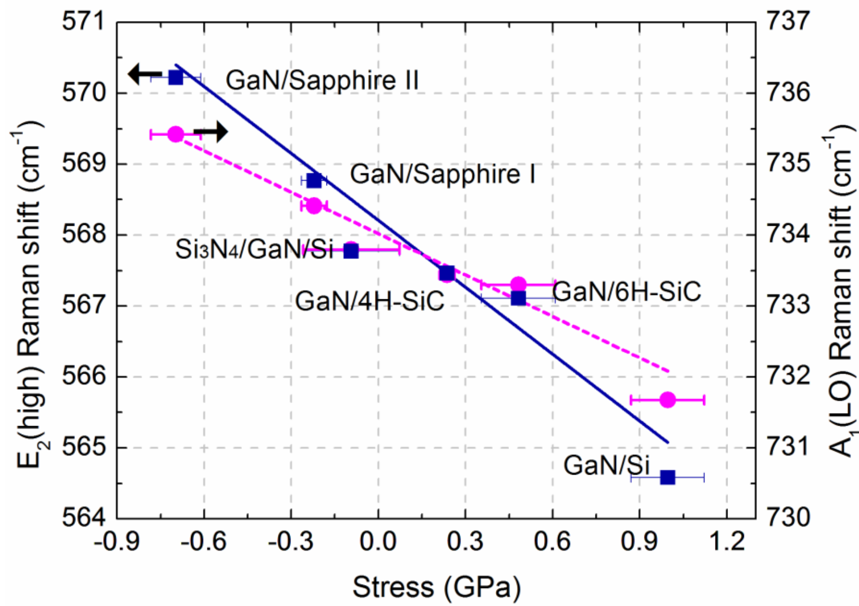


Figure 34: Raman shifts vs. residual stresses obtained by XRD measurements. The slope of each curve is represented in Table 4 as K coefficients. [98]

Table 4: Linear coefficients for 2-peak fit method by [98]

Coefficient	Units	Best estimate	95% confidence interval
$K_{E2(High)}$	cm^{-1}/GPa	-3.09	±0.41
$K_{A1(LO)}$	cm^{-1}/GPa	-2.14	±0.28
$A_{E2(High)}$	cm^{-1}/°C	-0.015	±0.0001
$A_{A1(LO)}$	cm^{-1}/°C	-0.0281	±0.0001

After obtaining all these calibrations, the temperature measurements can be performed. Uncertainty will be followed as well, where the sources of error come from variation in the 95 % confidence interval of the temperature, calibration constants, and fitted Raman spectra at the operated and pinch-off states, respectively. For example, the equation (3) from the linewidth method can be taken into uncertainty analysis. Individual uncertainties can be summed through a vector process as follows:

$$\delta\Delta T = \left[\left(\frac{\partial\Delta T}{\partial\Delta\Gamma}\delta\Delta\Gamma\right)^2 + \left(\frac{\partial\Delta T}{\partial \mathrm{B}}\delta\mathrm{B}\right)^2 + \left(\frac{\partial\Delta T}{\partial C}\delta C\right)^2\right]^{1/2} \tag{4}$$

In equation (4), reference temperature, T_0 from $\Delta T = T - T_0$, remains constant. Similarly, from the equation (2), uncertainty of 2-peak-fit method can be obtained that will be discussed in section 3.5. Then, with the uncertainty, the temperature rise from reference state can be obtained. Following Table 5 summarizes the spectral features that have been discussed.

Table 5: Physical origin of temperature dependence and limitation in Raman thermometry

Spectral Feature	Physical Origin	Physical Limitations	Error Possibility	Uncertainty
Peak position	Change in interatomic force	Convoluted stress	High	Low
Linewidth	Phonon scattering	Change in phonon-phonon scattering	Low	High
2-peak-fit	Change in interatomic force	Applicable only in bi-axial stress state	Moderate	Moderate

3.3 Experimental Set-up

The thermal response of AlGaN/GaN HEMTs on SiC and CVD diamond substrates where measured using micro-Raman spectroscopy with visible light excitation. For comparing GaN on Diamond and GaN on SiC devices, micro-Raman experiments were conducted using a Renishaw InVia Raman microscope with a 488 nm line of an Ar_+ laser and 3000 l/mm diffraction grating, with a laser beam diameter ~1 μm. Sub-band gap laser wavelengths were used for Raman measurements to prevent localized heating of GaN by laser light absorption. The collected Raman signals were imaged on a solid state cooled front side illuminated CCD. Experiments were carried out with the laser light perpendicular to the basal plane of GaN in a 180° backscattering configuration and un-polarized detection with a 50× lens.

All power sourcing and electrical measurements were conducted with a Keithley 2400 SMU for biasing gate-source and 2425 and 2651 SMUs for biasing drain-source, where high current and high voltage are needed, in 4 wire configurations. Both the calibration and measurement steps for micro-Raman thermal metrology were done at 25 °C on high spatial uniformity Instec heating stages with temperature controllers for 20 measurements for best estimates and uncertainties (95 % confidence intervals). The resulting Raman spectrum was analyzed with a Gaussian-Lorentzian (Voigt) fit to find peak parameters of the Stokes peaks of GaN. The Renishaw InVia microscope is seen in Figure 35, and the setup of the device, showing the GaN on SiC with a Cu mount affixed to on a heating stage for thermal control of the bottom of the mount.

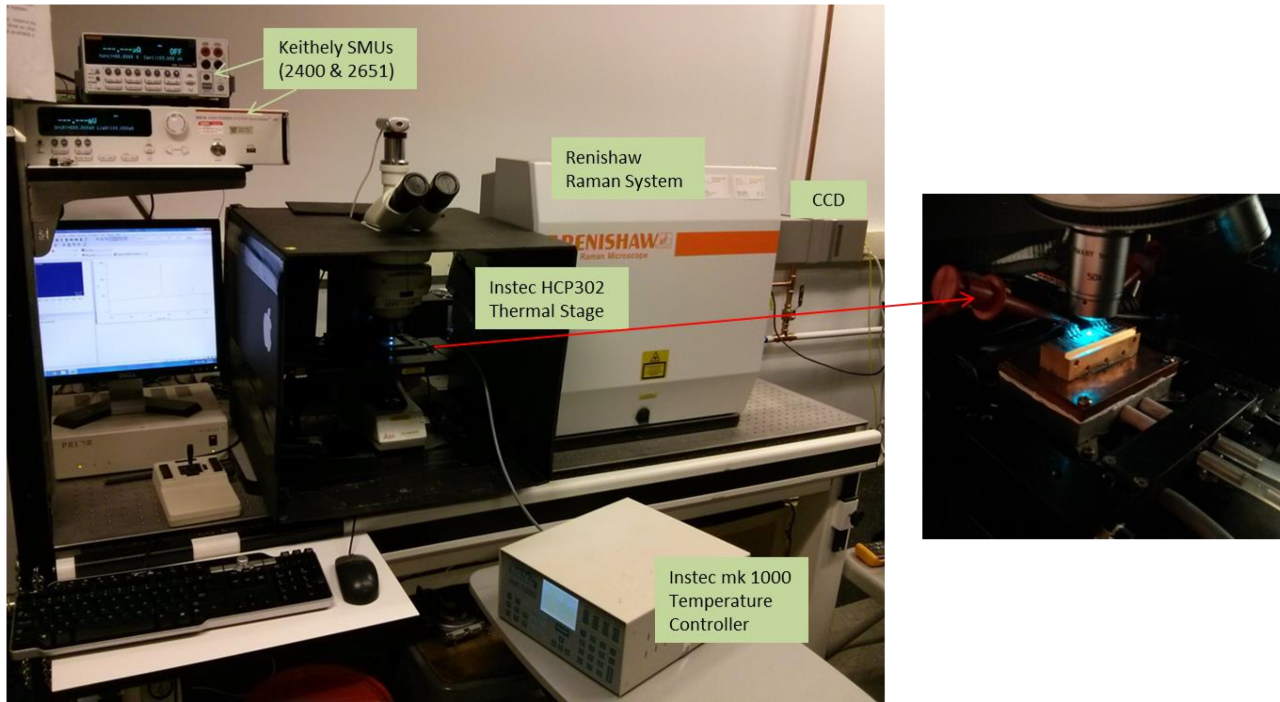


Figure 35: Schematic of experimental apparatus including spectrometer and peripherals used for characterizing AlGaN/GaN HEMTs: Renishaw Raman

Since HEMTs dissipate high power, liquid cooling was required to stabilize the base temperature of the heating stage. Without the cooling system, the thermal stage did not stabilize at high base temperature (95 ℃) for even low power density (1 W/mm for our devices). An INSTEC C300W industrial chiller was used for the cooling system. The flow rate of water controlled to maintain the temperature of the plate for different heat dissipation power levels. As the power dissipation increased, the minimum stabilization temperature increased for our setup as shown in Figure 36. Therefore, the flow rate of the water should be increased up to 16 GPH (~ 1 L/min) for a 5 W/mm power dissipation to maintain a minimum baseplate temperature of 27 ℃. Table 6 exhibits the properties of the chiller used in experiments.

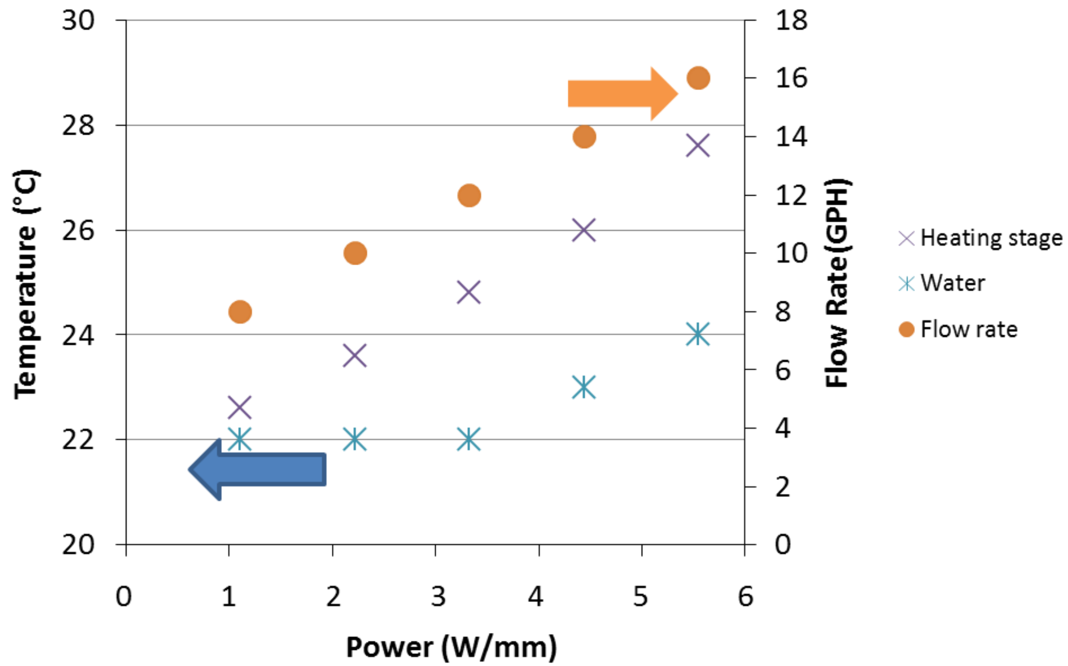


Figure 36: Temperature of water used as a coolant, and that of the heating stage as a function of a power. Flow rate had to be increased to cool down the heat dissipating from the high power HEMTs.

Table 6: Property of Instec C300W industrial chiller

Specifications	Values
Input Voltage	AC 100~110 V
Frequency	60 Hz
Current	4.5 ~ 6.5 A
Cooling Capacity	5186 Btu/h ~ 1520 W
Coolant Tank Capacity	6 L
Coolant Inlet/Outlet	10 mm OD connector
Max Lift	10 m
Weight	30 kg
Chiller Dimensions	60 X 30 X 49 cm

Devices were affixed onto the hotplate using a 6.35 mm thick thermally ultra-conductive oxygen-free (Cu 101) cooper mount, using a thin layer of silicone-based thermal grease between the heating stage and the copper mount, and a silver-based thermal compound was applied between the copper mount and the device as shown in Figure 37. The mounting procedure ensured that the device was immobilized during the micro-Raman process. The device package was attached to a 0.015" thick Mo tab using AuSn solder attach. The Mo spreader was attached using a thermal epoxy to a CuMo center bar. The center bar was attached to an aluminum plate bolted to a temperature controlled stage as shown in Figure 37 as well.

Figure 37: (Left) Schematic of GaN on SiC / GaN on Diamond device [62] (Right) Experimental set-up: Thermal grease (Silicone-based zinc oxide filled polysiloxane) was applied in (1), between the heating stage and the copper mount, Silver-based thermal compound was applied in (2), between the copper mount and the package, where the thermal conductivity of it is 6 W/m-K. Also, bolts were screwed between the package and the copper mount, and between the copper and the heating stage to immobilize the device during the micro-Raman process

Table 7: Thermal conductivity of material used in experiments [62]

Materials		Thermal Conductivity (W/m-K)
GaN		$490560*T^{-1.41}$
Diamond	In plane	$27287*T^{-0.55}$
	Through plane	$34109*T^{-0.55}$
CuMo		167
6061 Aluminum alloy (Heating Stage)		170
101 Copper Alloy (Copper plate)		380
Silicon-based thermal grease between the heating stage and the copper mount		N/A, but usually low (0.7 - 3)
Silver-based thermal grease between the copper mount and the device package		6

The thermal conductivities of materials used in the experiments are shown in Table 7. The thermal conductivities of GaN, diamond, and CuMo are obtained from [62]. [62] used a combination of Time-Domain Thermo-Reflectance (TDTR) and one-dimensional steady-state (1DSS) measurements to obtain the thermal properties of GaN on Diamond substrates. TDTR measurements focused on GaN epitaxial layer, the adhesion layer, heterogeneous interface resistances, and near-interface conductivity gradients in the CVD diamond film (through plane). The GaN conductivity obtained in the data fit was compared to and exhibited reasonable agreement with data reported in [60]. 1DSS measurements were performed to obtain in-plane thermal conductivity of the CVD diamond at Element Six [62]. Samples were prepared through CVD growth of 50µm thick ~10 × 45 mm free-standing diamond films. A miniature film heater, air-cooled heat sink and precisely located Type-K thermocouples were employed to heat and

cool the sample within an enclosure suppressing convective and radiative losses. Temperature measurements were conducted with known heating conditions and linear regression was performed to extract in-plane CVD diamond conductivity [62]. The temperature dependence of $T^{-0.55}$ was assumed for the conductivity of CVD diamond, and as mentioned in Chapter 2, there was an anisotropy, of which was assumed as 20 % based upon results reported by [99, 100]. Thermal properties employed for packaging layers were obtained via laser flash measurements and using resistance thermometry methods at Raytheon [62].

Both GaN on SiC and GaN on Diamond HEMT devices consisted of 10 fingers with 125 μm width. The GaN on Diamond devices were fabricated on a ~94 μm CVD diamond substrate with 10 μm gate-to-gate spacing, whereas GaN on SiC were fabricated on ~500 μm SiC substrate 30 μm gate-to-gate spacing, where the gate-to-gate spacing is defined in Figure 38 [62]. The effect of decreasing size by third is shown in the pictures of devices in Figure 38 that were taken with 5× lens using the Renishaw system. Measurements were taken directly adjacent to the source connected field plate (SCFP) between the gate and the drain. Since there were air-bridges on top of the devices, only edges of the gate were able to measure for GaN on SiC device as shown in the schematic in Figure 38. There was a slight opening for GaN on Diamond device at the center that center of the gate was measured additionally to the edge of the gate. The red dots in Figure 38 correspond to the position of the laser spots during the measurements.

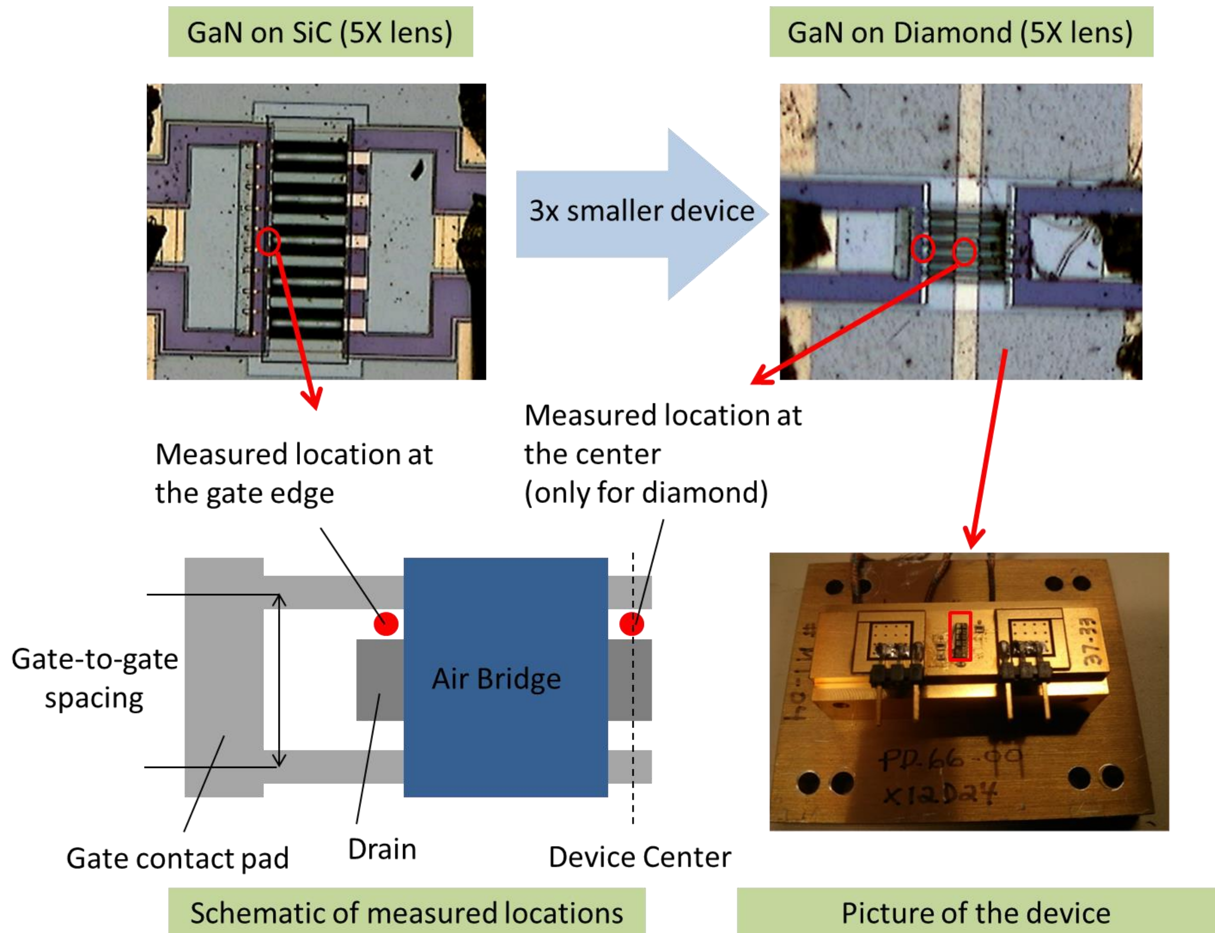


Figure 38: (Top left) 30 μm gate-to-gate spacing GaN on SiC; only edge of gate was accessible to measure, (Top right) 10 μm gate-to-gate spacing GaN on Diamond; edge of gate and center of gate were accessible, (Bottom left) Schematic of measured locations (Bottom right) 10 × 125 μm GaN HEMTs on CuMo bar on Cu plate.

3.4 Results and Discussion

Micro Raman measurements were performed to compare operational temperature at open locations in GaN on SiC and GaN on Diamond HEMTs during DC-bias operation. The operational temperature of GaN on Diamond device, at the center of gate between air-bridge, was measured with increment in power densities. And temperature of 5 of 10 channels at the

edge of the gate for two different power densities, 4.2 and 6.9 W/mm, were measured and compared between GaN on SiC and GaN on Diamond HEMTs. The reference measurements were taken before and after operation at the pinch-off state instead of no-bias condition to exclude the piezoelectric effect as discussed in section 3.2. Even though the first attempt to obtain the temperature was employing 2-peak-fit method, there were slight disagreements with the modeling as shown in Figure 40. Since the 2-peak-fit method can be applied when the operational thermo-elastic stress is in bi-axial-stress state, we had to confirm this assumption held by simulation, which will be discussed in Chapter 4. Therefore, as shown in Figure 39, calibration steps were needed for the E_2(High) and A_1(LO) modes to obtain the peak position based temperature, and compare with the modeling results.

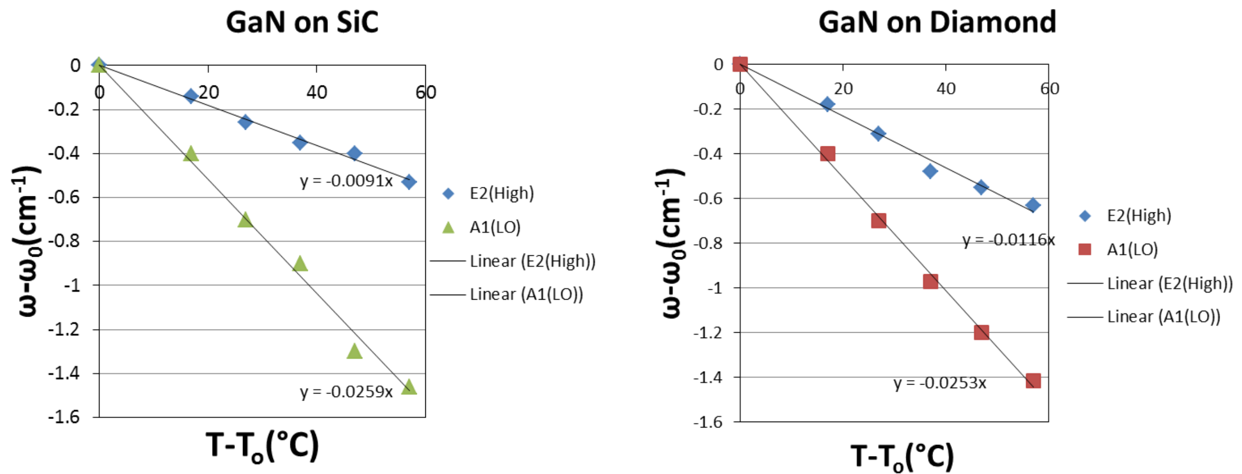


Figure 39: Temperature calibration from the change in temperature to change in peak positions of the E_2(High) and A_1(LO) mode frequencies for GaN on SiC and GaN on Diamond devices. Both shows good linear relation between the temperature difference and Raman shifts for two different modes.

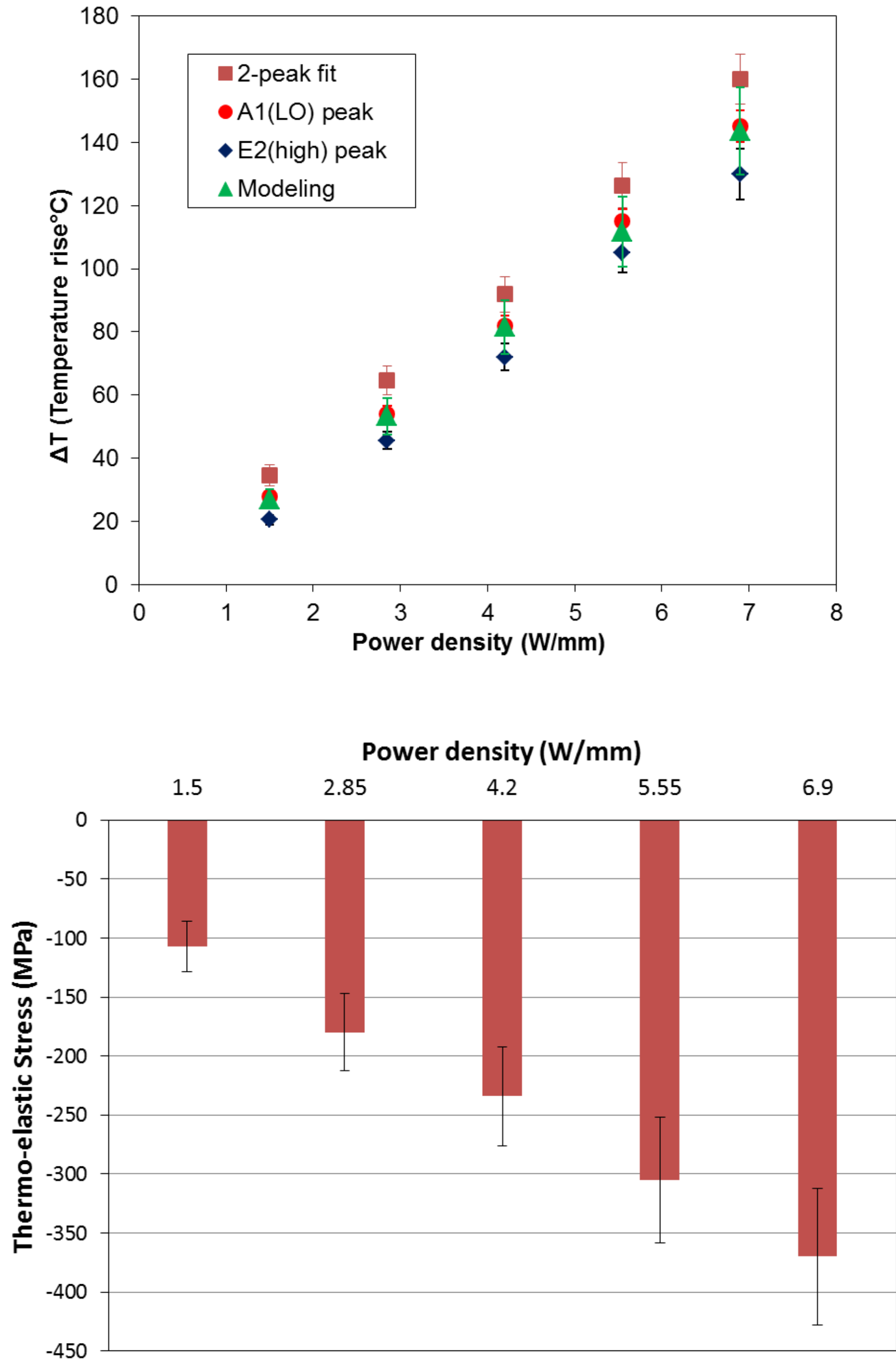


Figure 40: (Top) Temperature rise and (Bottom) thermoelastic stress of the center of channel at various power dissipation utilizing Raman thermometry techniques of GaN on Diamond device compared with modeling results. Due to thermoelastic stress, the E_2(High) peak position underestimates the temperature obtained by 2-peak-fit method. The difference in temperatures indicates the amount of thermoelastic stresses, which was also obtained by 2-peak-fit method.

From Figure 40, the modeling results agree well with the temperature by A_1(LO) peak position method, which is the first success to measure and match the GaN on Diamond HEMTs with modeling and experiments. Modeling was performed in [62] since the design parameters were proprietary data that cannot be done without knowing the structure parameters. The thermal properties were discussed in section 3.3. The 2-peak fit method showed a bit higher than the modeling results, whereas the E_2(High) peak position method underestimated the value because of the operational thermo-elastic stress. The reason for the lower temperature of E_2(High) mode than A_1(LO) mode is that A_1(LO) mode-peak position-based temperature is less sensitive to c-plane biaxial stress than E_2(High) mode-peak position-based temperature is. This can be confirmed by the coefficients from temperature-phonon frequency relations ($K_{E2(High)}$ = -3.09 cm^{-1}/GPa > $K_{A1(LO)}$ = -2.14 cm^{-1}/GPa). A_1(LO) phonon mode corresponds to atomic oscillations along the c-axis, whereas the E_2(High) mode of GaN corresponds to the atomic oscillation in the c-plane, which has a nonpolar character. Therefore, the E_2(High) peak position method is more sensitive to the lattice strain in the c-plane that underestimates the operational temperature, while A_1(LO) mode-based temperature agrees well with the modeling results.

Formerly, to calculate the operational thermoelastic stress, it was required to calibrate the device and use the temperature obtained by line-width method [101]. Utilizing 2-peak-fit method, however, which does not necessitate the calibration step, we can calculate the stress from equation (2). It was shown in previous studies that the operational thermoelastic stress in the GaN layer under the conductive channel is compressive, because local thermal expansion is hindered by the colder regions [102]. Indeed, the stresses were under compressive as shown in Figure 40. In addition, as power dissipation increases, the operational thermo-elastic stress increases. And thus, the temperature difference between the temperatures obtained by the

modeling and by the E_2(High) peak position method increases as the power increases as shown in Figure 40.

The operational temperatures at the edge of the gate fingers were used to compare the GaN on SiC to the GaN on Diamond devices as shown in Figure 41. As discussed above, strong agreements were obtained between the experimental data and the modeling data. With the reduced size of the device by a factor of 3 in terms of the gate to gate spacing for the GaN on Diamond versus GaN on SiC, Figure 41 shows a 20 % increase in the gate edge temperature. However, in [62], the strong correlation enabled the use of the model to confidently predict peak junction temperature in GaN on SiC and GaN on Diamond HEMTs. The GaN on Diamond device with 10 μm gate-to-gate spacing was determined to exhibit a peak junction temperature of 113.8 °C, 6.3 °C (6 %) higher than the 30 μm gate-to-gate spacing GaN on SiC at 3× the areal dissipation density (420 vs. 120 W/mm^2) [62]. Thus, these experimental results show a superior performance of the GaN on diamond device from the thermal perspective.

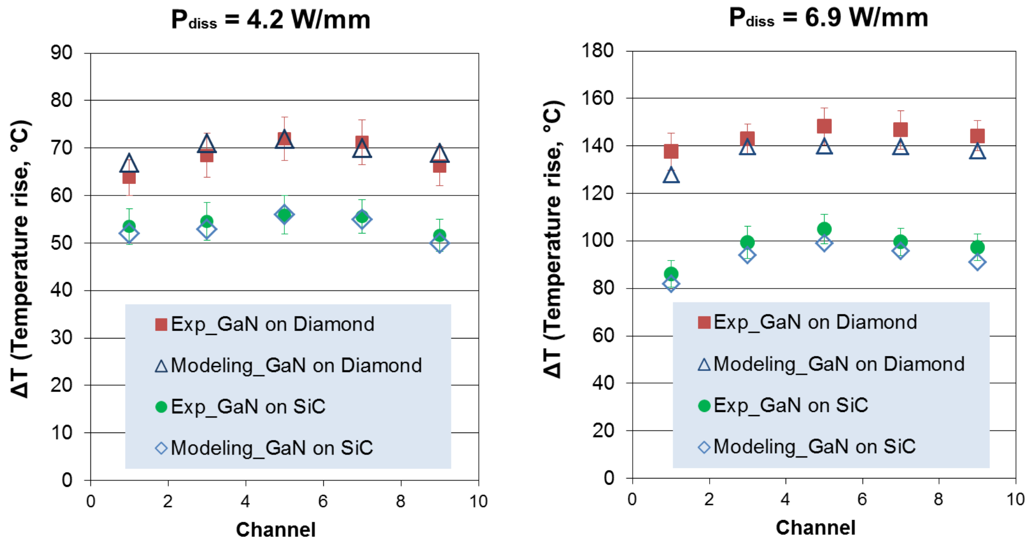


Figure 41: Measured (from A_1(LO) peak shifts method) and modeled operational temperatures of GaN on SiC and Diamond, where the modeling results are taken from [62].

Although GaN on SiC devices with 10 μm gate-to-gate spacing were not fabricated, and therefore were not measured, simulations showed that the temperature would increase more than 50 ℃ relative to the 30 μm gate-to-gate device [62]. Therefore this elucidates the importance of the high conductivity diamond substrate at a high HEMT areal power density. The potential of GaN on Diamond as a means to increase HEMT power density will enable smaller, higher power density devices. Perhaps equally importantly, we have successfully related these performance advantages to underlying material characteristics, building confidence in results, and informing follow-on development and future GaN on Diamond RF device design efforts.

3.5 Uncertainty Analysis

Since all the measurements repeated 20 times at each location and each power condition, an uncertainty analysis was performed. For the best estimates, 95 % confidence intervals were used, and the process of calculating the uncertainty of the 2-peak-fit method will be derived. The typical uncertainty of the 2-peak fit method is about 4 ~ 10 ℃, where the uncertainty in δK_{E2} and δK_{A1} (stress coefficients) is partially due to the uncertainty in knowing the elastic constants for GaN, which are the main drivers as shown in Table 8. Typical uncertainties of phonon frequencies are ~ 0.003 cm^{-1} for $\delta\Delta\omega_{E2}$, ~0.03 cm^{-1} for $\delta\Delta\omega_{A1}$. About 75~80 % of the uncertainty comes from the uncertainty of linear coefficients for the stress-phonon frequency relations, δK_{E2} and δK_{A1} (0.41 and 0.28 cm^{-1}/GPa) from Table 4. The rest comes from measurement uncertainty. From equation (2), the temperature rise can be obtained as equation (5), and the uncertainty is derived in equation (6):

$$\Delta T = \frac{\Delta\omega_{E2} \times K_{A1} - \Delta\omega_{A1} \times K_{E2}}{A_{E2} \times K_{A1} - A_{A1} \times K_{E2}} \quad (5)$$

$$\delta\Delta T = \left[\left(\frac{\partial\Delta T}{\partial\Delta\omega_{E2}}\delta\Delta\omega_{E2}\right)^2 + \left(\frac{\partial\Delta T}{\partial\Delta\omega_{A1}}\delta\Delta\omega_{A1}\right)^2 + \left(\frac{\partial\Delta T}{\partial A_{E2}}\delta A_{E2}\right)^2 + \left(\frac{\partial\Delta T}{\partial A_{A1}}\delta A_{A1}\right)^2 + \left(\frac{\partial\Delta T}{\partial K_{E2}}\delta K_{E2}\right)^2 + \left(\frac{\partial\Delta T}{\partial K_{A1}}\delta K_{A1}\right)^2\right]^{1/2} \quad (6)$$

Table 8: Total uncertainty (all in ℃) is decomposed into each uncertainty to confirm the main drivers of total uncertainty, which are Term (5) and (6) that are resulted from the uncertainty of elastic constants of GaN.

Contribution of Uncertainty	Ch. 1 @ 4.2W/mm	Ch. 5 @ 4.2W/mm	Ch. 1 @ 6.9W/mm	Ch. 5 @ 6.9W/mm
TERM (1)	0.16	0.18	0.14	0.13
TERM (2)	2.78	2.71	1.43	1.73
TERM (3)	0.07	0.07	0.07	0.07
TERM (4)	0.10	0.10	0.10	0.10
TERM (5)	1.90	2.24	2.79	4.26
TERM (6)	1.93	2.27	2.83	4.32
Total Uncertainty (°C)	**3.88**	**4.19**	**4.23**	**6.31**

As shown in Table 8, where Term (1) corresponds to the first term in equation (6) and Term (6) corresponds to the last term in the equation, total uncertainty increases with increase in temperature as a result of changes in peak shape and intensity and contributions from magnitude of the peak shift on the stress uncertainty. Thus the middle channel of the device, which has higher temperature, can have higher uncertainty versus fingers at the edge. The uncertainty in

K_{A1} and K_{E2} (Term 5 and 6) increase as $\Delta\omega$ increases, or temperature increases. Higher uncertainty exists in the measurement of the A_1(LO) mode (Term 2), since its peak height is lower than the E_2(High) mode and the peak is broader.

3.6 Summary and Conclusions

In Chapter 3, thermometry techniques were reviewed, and micro-Raman Spectroscopy was utilized to measure the operational temperature of HEMTs. The Peak position method, line-width method, and 2-peak-fit method were explained, and utilized to obtain the operational temperature and operational thermo-elastic stress. The difference between the temperature from peak position method of E_2(High) mode and that from 2-peak-fit method increased, as power dissipation increased indicating the increment in operational thermo-elastic stress. Since peak position is also affected by the strain, it underestimates the temperature.

The data taken on GaN on diamond devices showed superior performance to devices on SiC, which were strongly agreed between experiments and modeling. By shrinking the size of the GaN on diamond device by a factor of 3 in terms of gate to gate spacing versus GaN on SiC, the experimental data at the gate of the edge showed ~20 % temperature rise, whereas modeling showed only 6 % rise at the peak junction temperature. Thus, the use of diamond substrates is an effective method to reduce to overall device temperature or reduce the size of the devices. These effects include nontrivial thermal interface resistances between the GaN and diamond layers which should be further minimized to potentially reduce the impact on the device performance. These effects will be further explored in Chapter 4.

CHAPTER 4: FINITE ELEMENT MODELING

4.1 Introduction

As shown from previous chapter, non-contact optical experiments can be performed to characterize the thermal response of GaN-on-diamond devices. However, it is impractical to fabricate and test a large number of variations in the structure of the device to know whether or not this is true for all geometries. Thus, the use of numerical modeling provides a method to explore the design space of GaN-on-diamond devices to elucidate the parameters that impact the thermal performance the most, limiting the benefits of the diamond substrates.

Coupled electro-thermal simulation of AlGaN/GaN HEMTs, however, is a challenging task. To model these devices, there are several physical conditions to be considered. First, the piezoelectric and polar nature of AlGaN/GaN materials as well as surface defects must be considered. These defects are not well controlled and characterized. In addition, electro-thermal simulation of HEMTs requires very fine meshing at the active area, where the 2DEG is located. On the other hand, in pure thermal simulations, the active heat generation area is substituted by a uniform heat source, losing the electrical information. Instead, the effort is concentrated on the simulation of heat flow patterns extending to realistic package dimensions, hundreds of micrometers or milimeters in three-dimensions. To be specific, these pure thermal simulations allow for more realistic calculation of the self-heating that accounts for far field boundary conditions and larger regions around the active area of the device.

In this chapter, AlGaN/GaN HEMTs differing by geometry (gate-to-gate spacing, gate-width, and substrate thickness), substrate material, and thermal boundary resistances are simulated and compared in order to give meaningful results for proper thermal management. In

addition, operational thermo-elastic stresses are modeled to confirm the bi-axial stress state from Chapter 3.

4.2 GaN HEMTs Modeling

4.2.1 Thermal Modeling

For the base line device for this study, 60 fingers (gates) AlGaN/GaN HEMTs are investigated that are commercially available, which requires the thermal management. Figure 42 illustrates the schematic of AlGaN/GaN HEMT package. This includes the copper mount for the heating stage, Cu/W package (based on the 13-439 stratedge packages [103]), AuSn solder, substrate, and active HEMT layer. Instead of dividing HEMT layer, AlGaN, GaN, and buffer layers were modeled as one layer with total thickness of 2.171 μm HEMT layer, including the AlGaN layer (21 nm) and AlN buffer layer (100 nm). The heat sources sat on this HEMT layer with 0.8 by 1 μm thick; the thickness of substrates was initially 350 μm thick; the thickness of solder was 50 μm; the thickness of Cu/W package was 1 mm; and the width of the gate was initially 185 μm, which is half of the commercial HEMTs width, 370 μm. Other pertinent dimensions are given in Figure 42, while the thickness of substrate and gate-width will be changed afterwards. Initially, the thin thermal resistive layer of AlN was added between the HEMT layer and the substrate with the value of 60 m^2-K/GW, which will be changed as well. Two adiabatic symmetric planes were used such that only a quarter of the whole package was modeled, where the bottom plane was fixed at 300 K. The top surface is cooled by natural convection with h = 1 W/m^2-K. We used the following temperature-dependent thermal properties (T in Kelvin), which was also discussed in Chapter 3, as shown in Table 9. The coefficients of thermal expansion will be used in Section 4.2.2, Thermo-elastic stress modeling. The thermal simulations using COMSOL Multiphysics™ had approximately 550,000 elements.

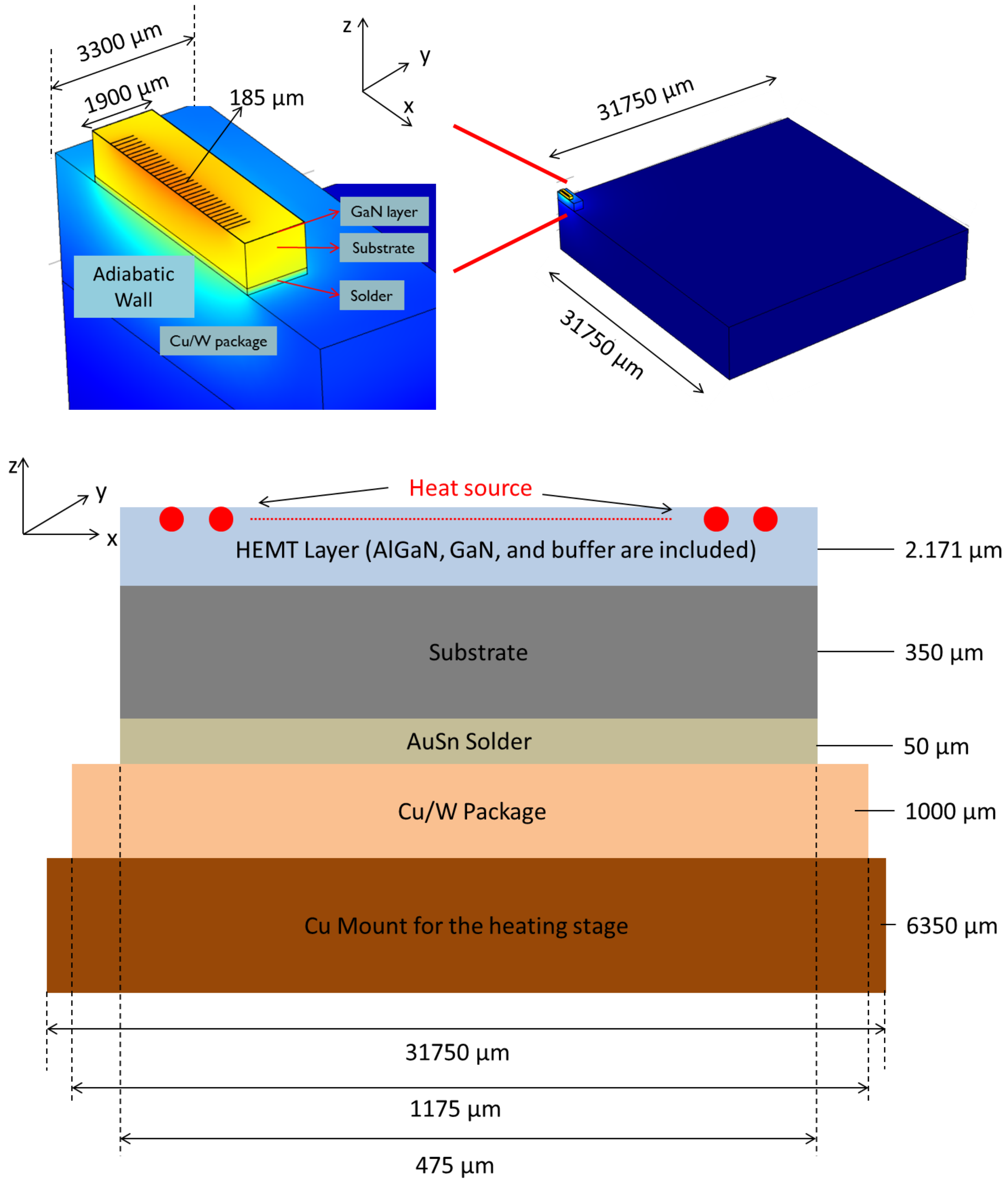


Figure 42: Schematic of 60 fingers AlGaN/GaN HEMT package for the thermal modeling: (Top) Quarter of whole package including copper mount, Cu/W package, solder, substrate, and GaN layer. (Bottom) Dimensions of a cross-section of a packaged device on a Cu heat sink (not to scale). Since the model is quarter, 30 heat sources were applied. Instead of dividing HEMT layer, AlGaN, GaN, and buffer layers were modeled as one layer.

Table 9: Temperature dependent thermal properties [62, 104-106]

Material	Thermal Conductivity (W/m-K)	Coefficient of Thermal Expansion (10^{-6}/K)
Diamond	In plane (a) = $27287 \times T^{-0.55}$ Through plane (c) = $34109 \times T^{-0.55}$	1.5
6H-SiC	$387 \times (T/293)^{-1.49}$	$\alpha_a = -1.36 \times 10^{-6} T^2 + 3.99 \times 10^{-3} T + 2.28$ $\alpha_c = -8.51 \times 10^{-7} T^2 + 2.94 \times 10^{-3} T + 2.44$
GaN	$150 \times (T/300)^{-1.4}$	$\alpha_a = -1.44 \times 10^{-5} T^2 + 1.7 \times 10^{-2} T + 0.553$ $\alpha_c = -1.39 \times 10^{-5} T^2 + 1.64 \times 10^{-2} T + 0.216$
Si_3N_4	1	1.5
Au	317	14.2
Cu/W	$-7.62 \times 10^{-5} T^2 - 2.51 \times 10^{-2} T + 204$	7
Sn-Au Solder	57	24

The section 4.3, thermal modeling, will investigate the effect of the substrate depth, the gate-to-gate spacing, the gate width, and interfacial resistance according to the material, which includes thermal resistances of AlN buffer / adhesion layer / thermal boundary resistances as shown in Figure 43. Especially, GaN on diamond versus GaN on SiC devices were compared since both substrates have been investigated from Chapter 3.

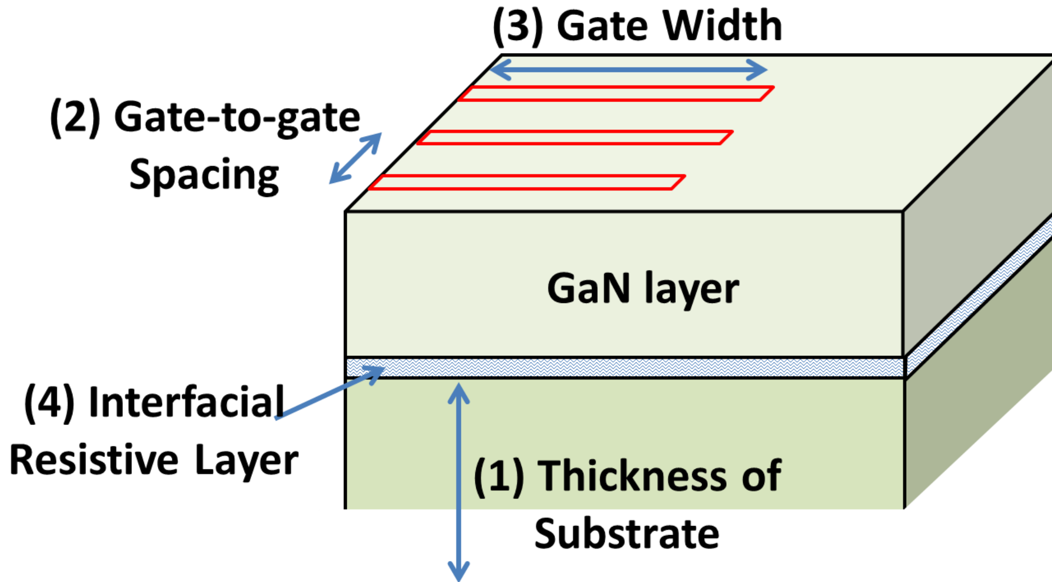


Figure 43: The schematic of the simulated 3D structure with quarter symmetry. Various thickness of substrate will firstly investigated, gate-to-gate spacing, gate width, and then interfacial resistance, which includes thermal resistances of AlN buffer, adhesion layer between GaN and Diamond, and thermal boundary resistances will be studied lastly.

4.2.2 Thermo-Structural Mechanics Coupled Modeling

Unlike pure thermal modeling, ohmic contacts (gate, drain, and source), and SiN passivation layer were added on top of GaN layer to predict the stress distributions in operational AlGaN/GaN HEMTs, since metallization will affect the stress between the ohmic contacts and the GaN layer as shown in Figure 44. A 0.6 μm thick gold metal layer was placed on top of the GaN, and therefore, the number of finite elements increased from 550,000 to 1,600,000 elements. Thus, instead of modeling 60 fingers devices, 10 fingers devices were modeled which are similar to the experimental devices in Chapter 3. HEMT devices consisted of 10 fingers with 125 μm widths, and the lengths of ohmic contacts and the spacing with each other are given in Figure 44. All other geometries and boundary conditions of packages are same as thermal modeling.

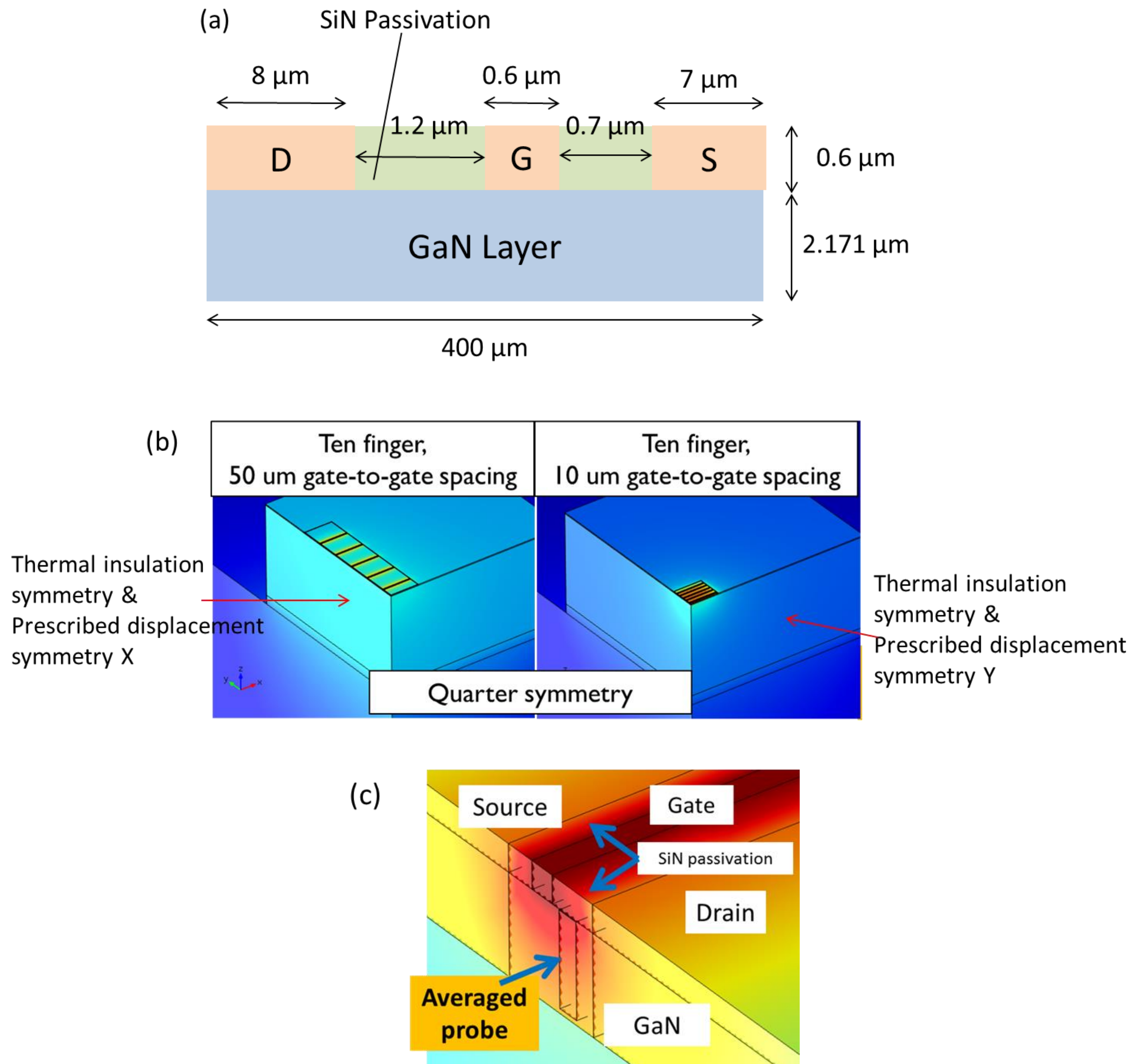


Figure 44: (a) Schmatic of cross-sectional of the device with ohmic contacts and SiN layer on top of the GaN layer (not to scale). Other package information is same as thermal modeling. (b) Boundary conditions of GaN HEMTs with a quarter symmetry: Heat source is given as an area and symmetry walls are considered as adiabatic and prescribed. (c) Unlike thermal modeling, 0.6 µm gold metal as source, gate, and drain are added and SiN passivation layer is added to consider the stress effects on GaN. Stresses were averaged through the probe in modeling to compare with the experiments,

Similar to thermal modeling, by replacing the symmetry planes with adiabatic and prescribed sidewalls, modeling can be restricted to one quarter of the whole structure with no loss of information as shown in Figure 44. Since the experimental data collected by Raman spectroscopy was averaged through the GaN layer thickness, comparisons to calculations were made over a volume that was similar to the volume probed by the Raman laser as shown in Figure 44. The transverse-isotropic elastic symmetry was assumed for the elastic constants that are shown in Table 10. The coefficient of thermal expansion was given in Table 9.

Table 10: Assuming the transverse-isotropic elastic symmetry, the elastic constant matrix of the thin films take the form, and the values are following [106-108]:

$$[C_{ij}] = \begin{bmatrix} C_{11} & C_{12} & C_{13} & 0 & 0 & 0 \\ C_{12} & C_{11} & C_{13} & 0 & 0 & 0 \\ C_{13} & C_{13} & C_{33} & 0 & 0 & 0 \\ 0 & 0 & 0 & C_{44} & 0 & 0 \\ 0 & 0 & 0 & 0 & C_{44} & 0 \\ 0 & 0 & 0 & 0 & 0 & C_{66} \end{bmatrix}$$

where $C_{66} = (C_{11} - C_{12})/2$.

[GPa]	Diamond	6H-SiC	GaN
C11	1143	501	390
C12	82.6	111	145
C13	82.6	52	106
C33	1143	553	398
C44	530.2	163	105

4.3 Temperature Results

As shown in Figure 11, the lifetime of the HEMTs will exponentially decrease beyond 200 °C or 493 K (or ~500 K). Therefore, the maximum temperature of the channel was limited to 500 K for this study, where the maximum temperature occurs at the middle channel of the central finger in our geometry. As mentioned in section 4.2.1, the dimension of the base line devices are: a 50 µm gate-to-gate spacing, 370 µm long gate-width with 350 µm thick substrate having 60 m^2-K/GW thermal boundary resistance, the maximum power density was calculated for both substrates: SiC and Diamond. As shown in Figure 45, GaN on Diamond device show a 50% increase in power density than GaN on SiC before reaching the maximum temperature of 500K. However, we can design the device showing much higher thermal performance.

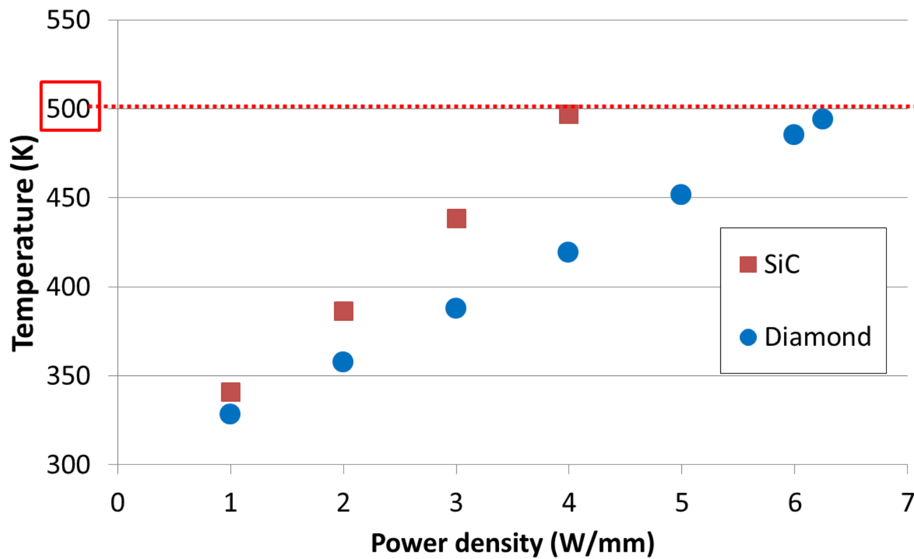


Figure 45: Maximum power density according to the commercilized device, (50 µm gate-to-gate spacing with 350 µm thick substrate), when limiting the maximum temperature to 500 K.

4.3.1 Effect of Substrate and Thickness

First of all, we investigated the effect of thickness of substrate for SiC and Diamond on their thermal performance. Since SiC showed a temperature of 500 K at 4 W/mm, we applied 4 W/mm for various thicknesses for both materials. As shown in Figure 46, the maximum channel temperature for SiC obtains a minimum at a thickness of 150 µm, and that of Diamond occurs at 200 µm. As the thickness is increased beyond these optimal values, a 1D resistance begins to dominate the thermal response while for thicknesses smaller than the optimal value, spreading resistance dominates. Since the thermal conductivity of SiC is much lower than that of GaN on Diamond, the channel temperature of GaN on SiC tends to increase much faster than that of GaN on Diamond as the substrate thickness is increased. Thus, having samples with substrates, which are much thicker than their optimal values, will show a larger benefit of GaN on diamond as opposed to GaN on SiC.

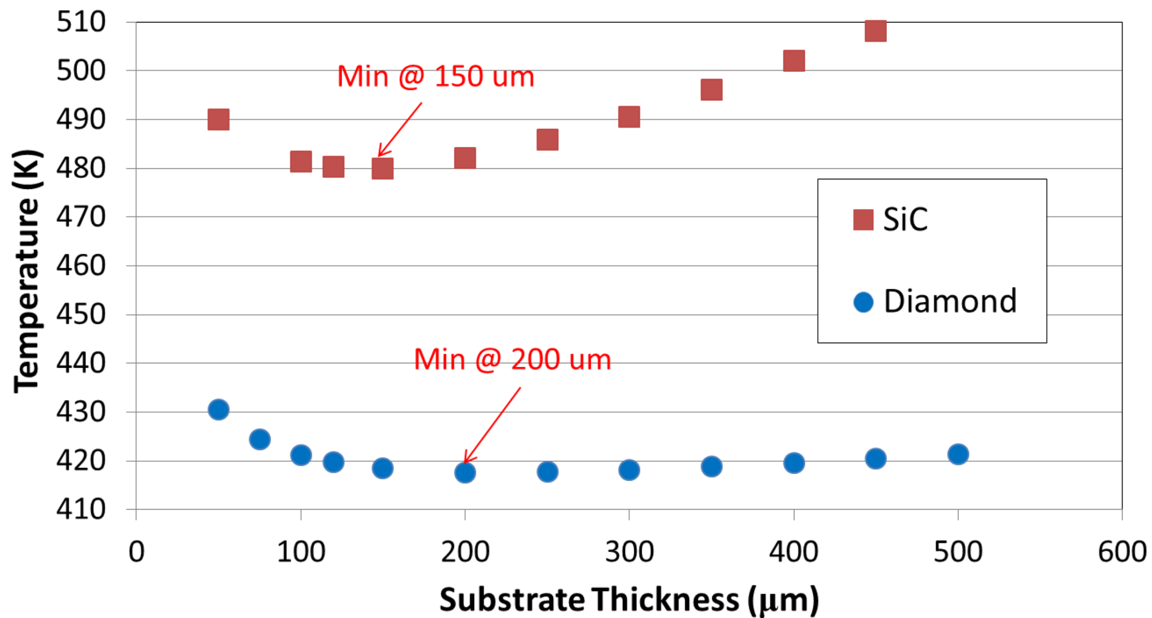


Figure 46: Maximum channel temperatures for various substrate thickness at 4 W/mm for 50 µm gate-to-gate spacing

4.3.2 Effect of Gate-to-gate Spacing

Since there was only 1 degree Celsius difference between 150 and 200 µm thick SiC as shown in Figure 46, the thickness of substrate as 200 µm for both SiC and Diamond was selected. Then, temperatures were calculated for different gate-to-gate spacing: from 10 to 50 µm at the constant power dissipation, 4 W/mm. Figure 47 illustrates two different gate-to-gate spacings for 60 finger HEMT devices. Obviously, as the gate-to-gate spacing gets smaller, the temperature rise increases linearly as power dissipation increases as shown in Figure 48. The slopes of the Figure 48 are the total thermal resistance (R_{th}, mm-K/W) of the packaged stack as the slope can be expressed as:

$$\Delta T = R_{th} \times P_{dissipation} \tag{6}$$

where ΔT is the temperature rise from reference temperature, 300K. The resistances are obtained from Figure 48 summarized in Table 11. From Figure 48, the slope of 50 µm gate-to-gate spacing is the lowest with the value of 28.6 mm-K/W showing the lowest temperature rise, whereas that of 10 µm gate-to-gate spacing is 39.7 mm-K/W.

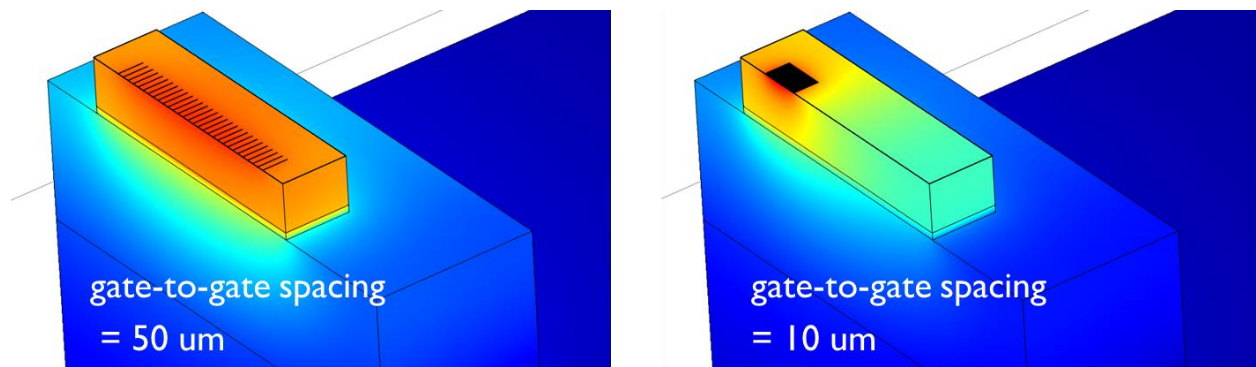


Figure 47: Schematic of two different gate-to-gate spacing device with 200 µm thickeness substrate at 4 W/mm. The active area features sixty 2.5 µm long heating fingers; these fingers represent the device area where power dissipation is concentrated.

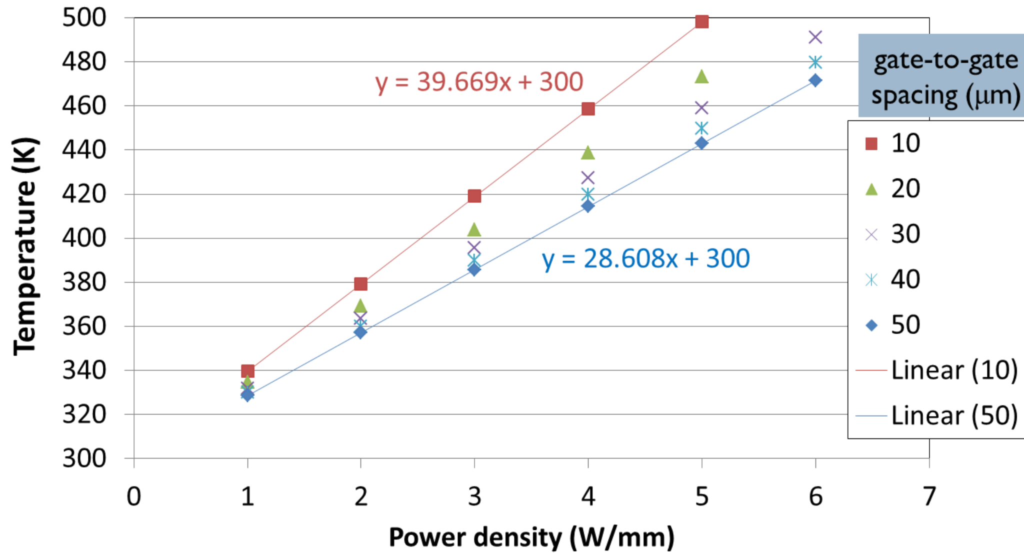


Figure 48: Highest channel temperatures of different power density showing linear relation for various gate-to-gate spaicng with 200 µm thickness of diamond. 50 µm gate-to-gate spacing shows lower thermal resistance (39.7 mm-K/W) compared to 10 µm gate-to-gate spacing (28.6 mm-K/W)

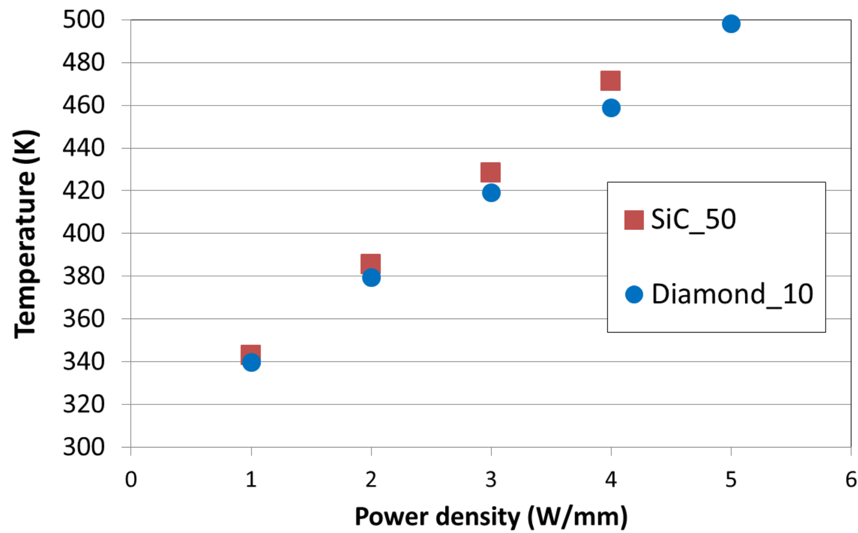


Figure 49: 10 µm gate-to-gate spacing GaN on Diamond device shows lower temperature than 50 µm gate-to-gate spacing GaN on SiC, where both substrates are 200 µm thick.

Table 11: Total thermal resistances for different gate-to-gate spacing for SiC and Diamond as substrates.

Substrate	**SiC**	**Diamond**				
Gate-to-gate spacing (µm)	**50**	**10**	**20**	**30**	**40**	**50**
Thermal Resistance (mm-K/W)	42.8	39.7	34.6	31.8	29.9	28.6

As shown in Figure 49, 10 µm gate-to-gate spacing GaN on Diamond has a lower temperature rise with the resistance of 39.7 mm-K/W than 50 µm gate-to-gate spacing GaN on SiC device with the resistance of 42.8 mm-K/W for a substrate thickness of 200 µm as summarized in Table 11. These results show that GaN on Diamond device can potentially reach much higher power densities with smaller gate-to-gate spacings than GaN on SiC as shown experimentally in Chapter 3. It should be noted that the optimized diamond layer thickness is used here in this study and much larger devices having 60 gate fingers, whereas the HEMTs used in experiments had 10 fingers. Thus, an overall improvement is observed as the device structure becomes larger. Finally, it should be noted that the 200 µm diamond thickness was optimized for a 50 µm gate-to-gate spacing for the device. As the gate pitch is further reduced, additional considerations may be needed to further improve the device performance. Figure 50 shows the results of the optimized diamond thickness for different gate-to-gate spacing. As the gate pitch reduces, the optimized thickness of diamond increases. However, we have to consider not only the cost of growing or transferring CVD diamond, but also the thermal conductivity of diamond as thickness and nucleation density matters as discussed in Figure 21 in Chapter 2. For example, 500 µm thick diamonds for 10 µm gate-to-gate spacing device is unrealistic in terms of cost and

growth technique that common diamond thickness for GaN is ~100 μm. Therefore, we don't have to push ourselves too hard to match the optimized thickness if it costs too much. There is only <5 ℃ differences between the temperature of 200-300 μm thick and that of the optimized thickness for each gate-to-gate spacing. Thus, having ~200-300 μm thick of diamond, where the anisotropic behavior of the diamond thermal conductivity diminishes according to Figure 21, will be reasonable for all gate-to-gate spacing.

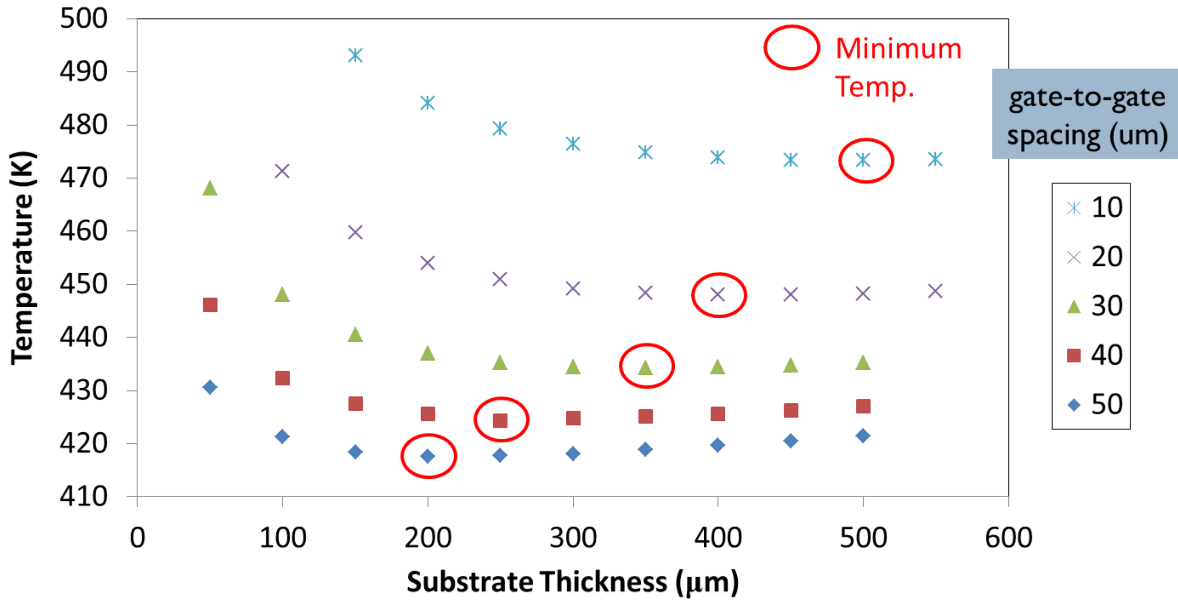


Figure 50: Temprature calculation for various gate-to-gate spacing to find the optimized thickness of diamond with the mimum temperature rise at 4 W/mm. Below its optimized thickness, the temperature rise rapidly, but ~200-300 μm thick, there is only <5 ℃ differences with the temperature of each optimized thickness.

4.3.3 Effect of Gate Width

Not only does the gate-to-gate spacing affect the temperature, but also the width of the gate or device channel. In the current simulations, the device channel width was fixed at a value of 370 µm. For studying the impact of channel width, the 50 µm gate-to-gate spacing with a 200 µm substrate thickness was used at 4 W/mm power dissipation for both diamond and SiC. As the gate width increases from 100 to 400 µm, the results of temperatures are shown in Figure 51. The data show that as the gate width increases, the temperature increases linearly for both diamond and SiC. With the superior thermal conductivity of diamond compared to SiC, the width of gate of GaN on Diamond can be increased up to 650 µm, whereas that of GaN on SiC can be increased up to 400 µm, when we limit the maximum temperature to 500 K. This result also agrees with the result from Figure 45, which showed the maximum power density for SiC and Diamond. Increasing the gate width can be described as increasing the power density that makes two different results in strong agreement.

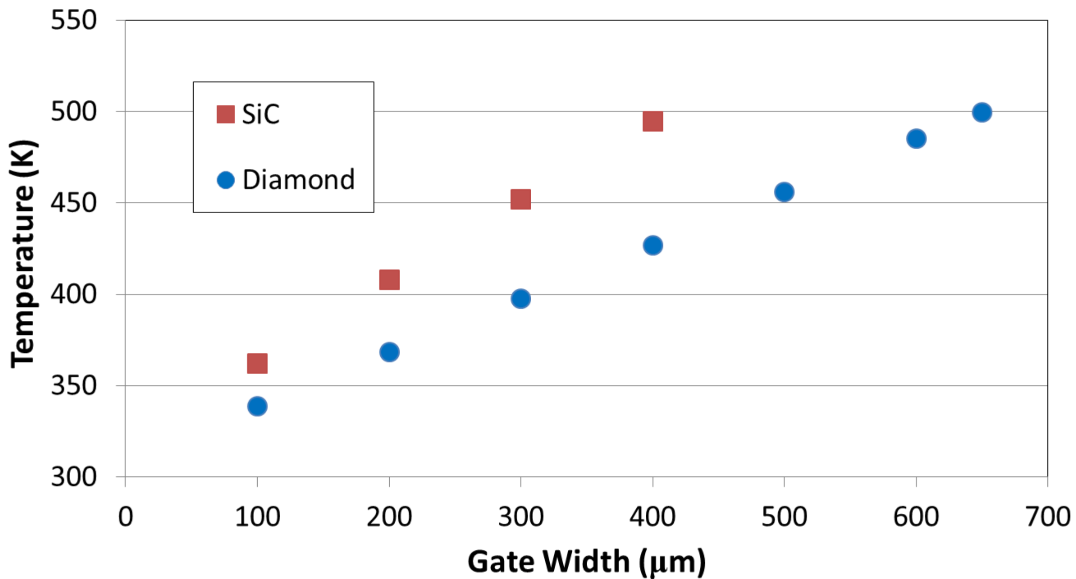


Figure 51: Channel temperature of different gate widths for GaN on SiC and GaN on Diamond.

4.3.4 Effect of Interfacial Layers

Lastly, we cannot ignore the effect of the interfacial layers that has thermal boundary resistances as it has been emphasized in [60, 62, 65, 74]. Since the model in this study only includes the GaN layer and substrate layer on top of the package, variations in the interfacial layer must be included. For studying the impact of interfacial layers, the 50 μm gate-to-gate spacing device with 370 μm gate widths, and a 200 μm substrate thickness was used at 4 W/mm power dissipation for both diamond and SiC. Until now, the interfacial thermal resistance was fixed with the value of 60 m^2-K/GW. However, the resistances can be varied, which is dependent on how the GaN layer is grown, or transferred on the substrates, as discussed in Chapter 2 and summarized in Table 12. Apparently, the thermal resistance of direct growth of GaN on diamond is lower than that of transferred GaN on diamond with adhesion layer. In addition, since the growth techniques of GaN on SiC have been well established, and they are well lattice matched, adhesion layer is unnecessary. However, the interfacial resistance between the buffer or adhesion layer and substrate varies that can be resulted from the thickness of layers. Therefore, after considering all these issues, we can have various total thermal resistances, $\mathbf{R_{Total}}$, summing all the thermal resistances existing between the layers as summarized in Table 12. The total thermal resistances of GaN on Diamond vary from 20 to 120 m^2-K/GW, while that of GaN on SiC differ from 20 to 75 m^2-K/GW. Therefore, the maximum channel temperatures were calculated for different thermal resistance values from 0 to 100 m^2-K/GW as shown in Figure 52. When we assume that we can obtain 0 resistances, which is somewhat unrealistic, it results in 16 °C or 13.8 % decrease in the averaged channel temperature than 100 m^2-K/GW total resistances. If direct growth of GaN on Diamond is available having the resistances between 20 and 60 m^2-K/GW, there will be only 6 °C or 4.7 % between those two values for the 50 μm gate-to-gate

spacing device with 370 μm gate widths, and a 200 μm substrate thickness was used at 4 W/mm. In addition, there is a 10 ℃ differences in peak temperature as shown in Figure 52. Even though 5-10 ℃ differences in temperature can be comparable with the uncertainty from the measurements, the efforts to reduce the thermal resistances must make steady progress.

Table 12: Thermal resistances between GaN on Diamond and SiC [59, 65] (in m^2-K/GW)

Material	$R_{AlGaN\text{-}GaN}$	$R_{GaN\text{-}Adhesion}$	$R_{Adhesion\text{-}AlN}$	$R_{AlN\text{-}Substrate}$	R_{Total}
Diamond, w/o adhesion	5	10		(5, 20, 50)	20 - 65
Diamond, w/ adhesion	15	30	20	(5, 20, 50)	70 - 120
SiC	5	10		(1, 30, 60)	20 - 75

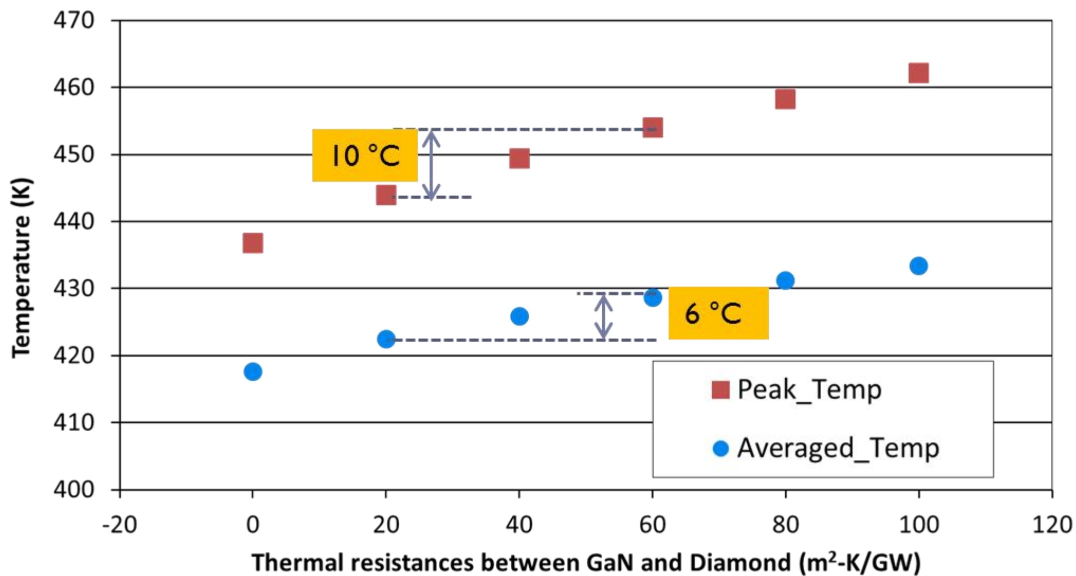


Figure 52: Peak and averaged channel temperature for different thermal resistances between GaN and Diamond, where the 50 μm gate-to-gate spacing device with 370 μm gate widths, and a 200 μm substrate thickness was used at 4 W/mm.

Moreover, we can see the effect of thermal boundary resistances (TBR) through the thickness of GaN and its substrate. As shown in Figure 53, TBR adds temperature rise in GaN layer for both GaN on Diamond and GaN on SiC. The temperature differences of GaN in GaN on Diamond are ~25 K and 46 K, for TBR = 0 and 100 m^2-K/GW, respectively. And, for the temperature rises of GaN on SiC, there are only 5~6 K differences with GaN on Diamond that there is no effect of thermal conductivity of substrate, but effect of thermal boundary resistance.

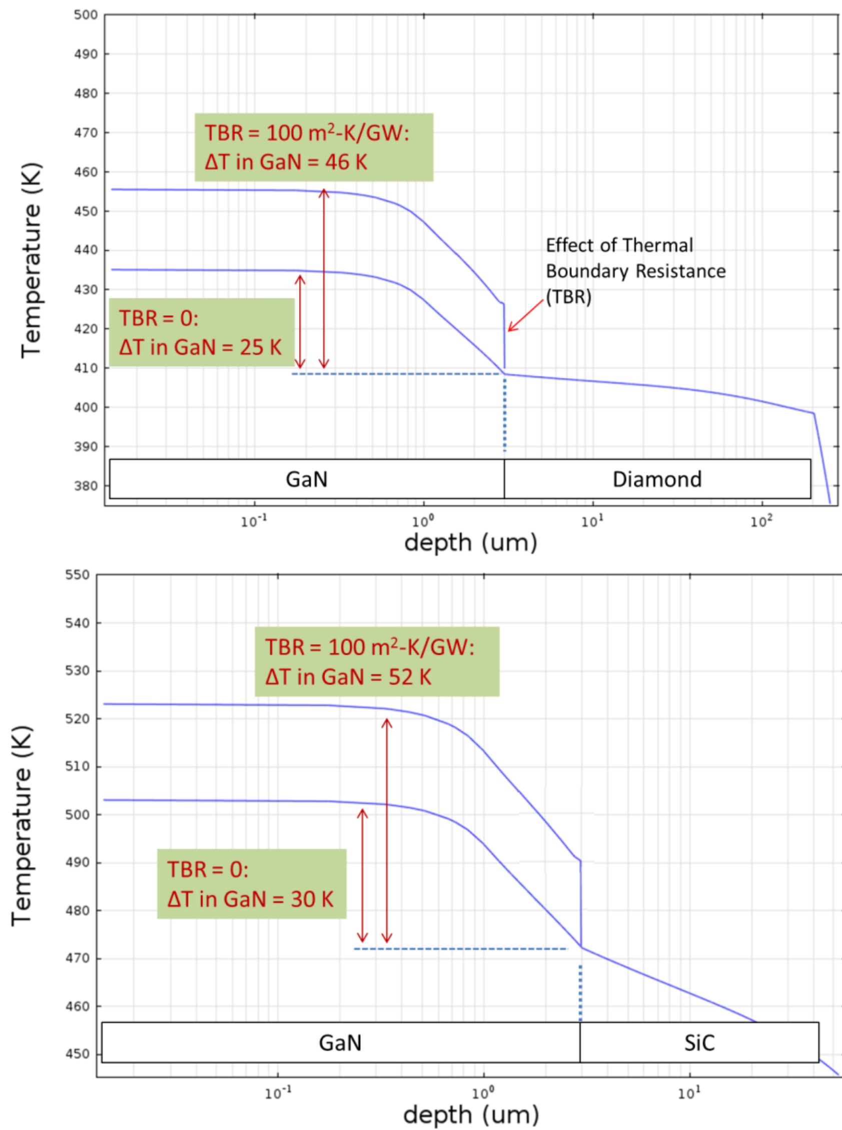


Figure 53: Temperature distribution through the thickness of GaN and its substrate.

4.4 Operational Thermo-Elastic Stresses

The objective of this study is to analyze each layers, ohmic contacts, SiN passivation layer, GaN layer, and substrate from the stress effects. In addition, to support the 2-peak-fit used in Chapter 3, we will investigate the stress components in x and y direction to examine if GaN layer is under bi-axial stress condition or not. From Figure 40 in Chapter 3, the averaged operational thermo-elastic stresses of GaN were obtained by Equation (2), utilizing the 2-peak-fit method with Raman spectroscopy. Extracting the stresses from the results, the experimental stresses can be compared with modeling data. Prior to getting through the modeling results, Figure 54 shows the basic idea of how coefficient of thermal expansion (CTE) mismatch will cause the strain in layers. When the epitaxial layer, which is thinner than the substrate, is grown on top of the layer having higher CTE, the epitaxial layer will experience tensile strain during heating.

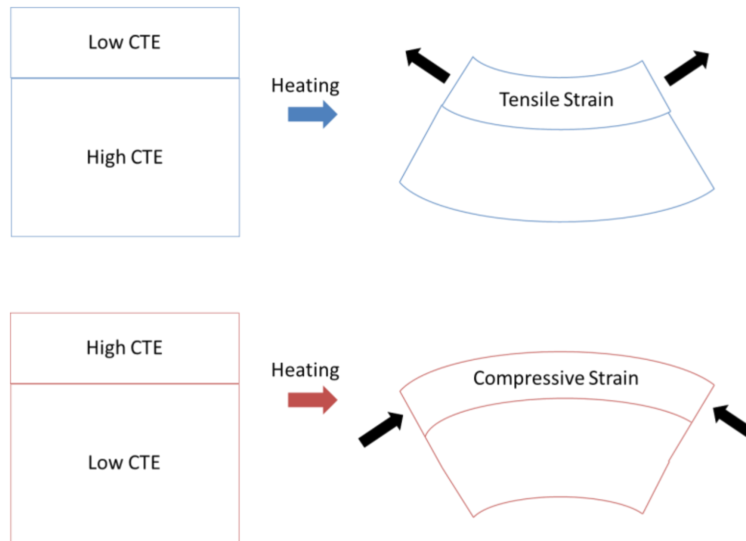


Figure 54: Schematic of effects of CTE mismatch for epitaxial layers: (Top) If epitaxial layer is grown on higher CTE layer, the layer with lower CTE will experience tensile strain during heating, (Bottom) Vice versa.

Table 13: CTE of various material at 300 K [57]

Material	GaN	SiC	Diamond	Au	SiN
Coefficient of Thermal Expansion (10^{-6}/K)	5.6	4.3	1.5	14.2	1.5

The values of CTE are summarized in Table 13 showing the differences between each other layers. Knowing all the geometries and structural/thermal properties from previous sections, we can obtain the stress values from modeling to compare with the experimental results. As shown in Figure 41 from Chapter 3, GaN on SiC showed a lower temperature rise than GaN on Diamond and thus, the thermal stresses from experiments are also lower as shown in Figure 55 that all stresses are under compressive since GaN has higher CTE, 5.6×10^{-6}/K, than SiC and Diamond, 4.3 and 1.5×10^{-6}/K. However, this comparison is for two different gate-to-gate spacing devices, 30 µm gate-to-gate spacing GaN on SiC device and 10 µm gate-to-gate spacing GaN on Diamond device. Therefore, we have to compare the same gate pitch (10 µm) with same power density. As a result, GaN on SiC shows higher compressive stress than GaN on Diamond as shown in Figure 55. This is because temperature rise of GaN on SiC is higher than GaN on Diamond for the same gate-to-gate spacing as discussed in section 4.3, even though CTE mismatch of GaN and Diamond (73 %) is larger than that of GaN and SiC (23 %). Therefore, more investigation is required to understand the effect of CTE mismatch.

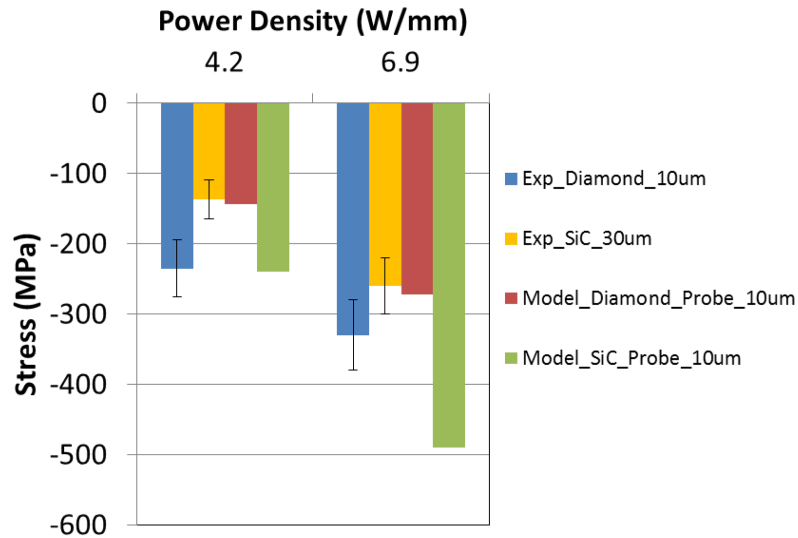


Figure 55: Operational thermo-elastic stress from the experiments; 10 µm gate-to-gate spacing GaN on Diamond and 30 µm gate-to-gate spacing GaN on SiC, and from the modeling; both 10 µm gate-to-gate spacing that SiC shows much higher stress since it has higher temperature rise than GaN on Diamond.

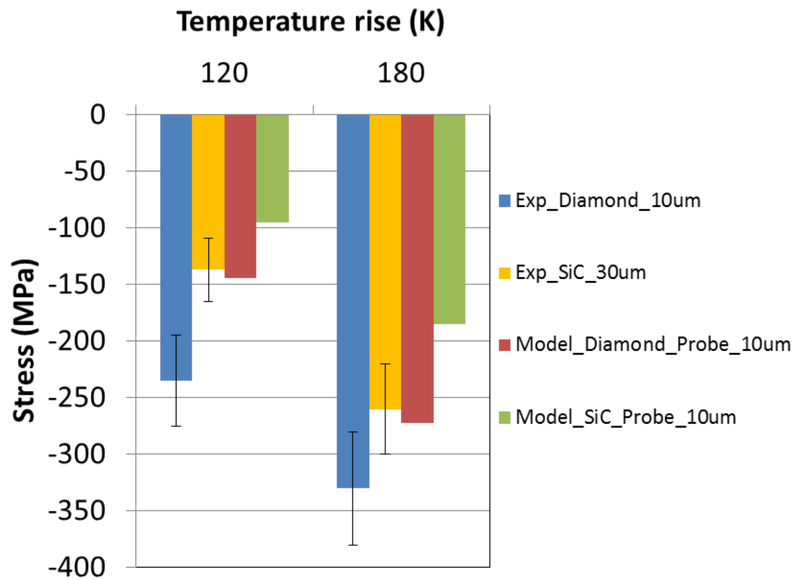
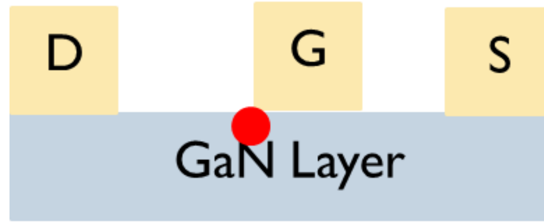


Figure 56: Differences in stresses when the same temperature rise is applied. Since the CTE mismatch of GaN and SiC is lower than that of GaN and Diamond, GaN on SiC has lower thermal stress.

To verify if the effect of the CTE mismatch exists or not, the temperature rise for both GaN on SiC and GaN on Diamond must be same. Thus, the thermal properties of the substrate are not changed, which still have the same temperature rise, but the structural properties are changed to have same elastic constants and CTEs for both SiC and Diamond that is an imaginary material. Obviously, GaN on SiC shows lower thermal stress than GaN on Diamond because of lower CTE mismatch as shown in Figure 56. Therefore, the model used in this study can be verified by reasonable calculations. We can learn from Figure 55 and Figure **56** that even though the CTE mismatch of GaN and SiC (23 %) is about a third of GaN and Diamond (73 %), the highest thermal conductivity of Diamond superiorly reduces the temperature at the active region. This consequences in lowering thermal stresses in GaN on Diamond than GaN on SiC, which shows the promise of utilizing Diamond as AlGaN/GaN HEMTs.

In addition, we investigate the effect of metallization caused by the ohmic contacts and the effect of SiN passivation layer. To study these effects, right underneath the gate edge at the drain side is investigated as shown in Figure 57. Since gold is used as ohmic contacts that has the highest CTE among the HEMT layers, ohmic contacts experience compressive stress while GaN layer experiences tensile stress because of the principal of action and reaction. Therefore, as shown in Figure 57, the tensile stress added in GaN layer will lower the total stresses than previous results (Figure 56). For both GaN on SiC and GaN on Diamond, ~50 MPa is added at 120 K (corresponds to temperature rise of GaN on Diamond at 4.2 W/mm) and ~90 MPa is added at 180 K (6.9 W/mm).



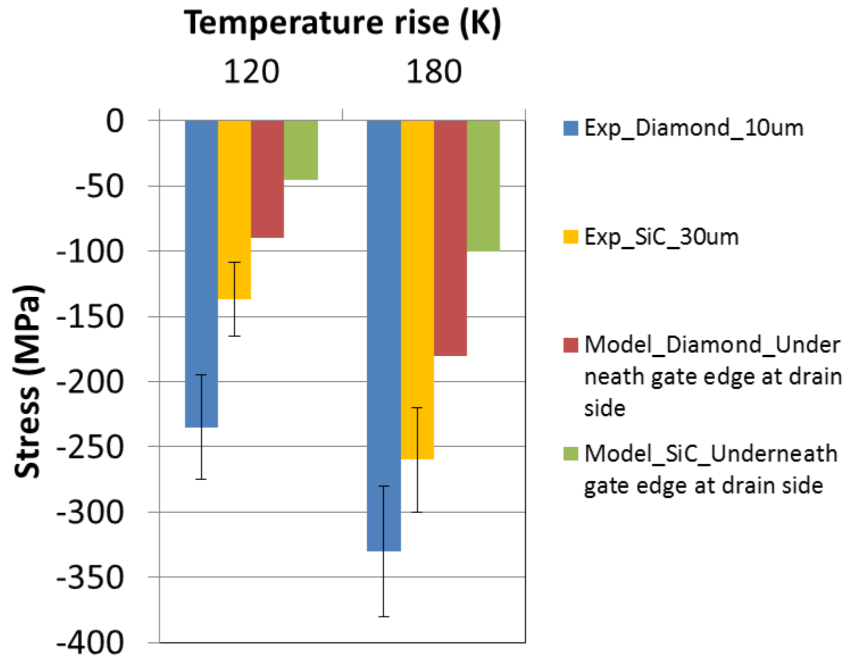


Figure 57: (Top) Red spot indicates the underneath of the gate edge, where the stresses are calculated, (Bottom) Metallization adds tensile strain that total stresses are lower than Figure 56: ~50 MPa at 120 K and ~90 MPa at 180 K for both GaN on Diamond and GaN on SiC.

Lastly, since the 2-peak-fit method, utilized in Chapter 3, is only acceptable when the stress state is bi-axial, stresses of x and y components in GaN layer are calculated while the all stresses were x-components so far. As shown in Figure 58, both components agree well with each other that confirms the bi-axial stress state in GaN layer.

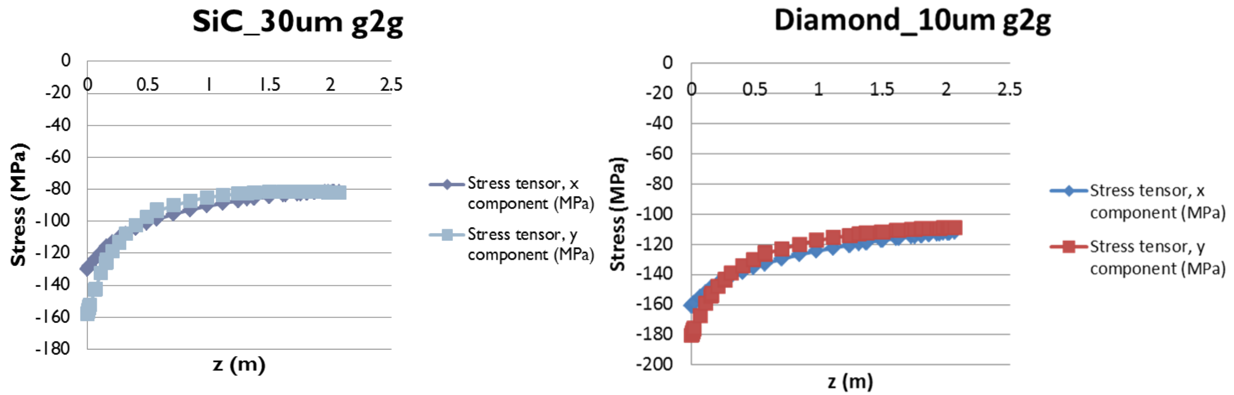


Figure 58: Stresses of x and y components are evaluated to confirm the bi-axial stress state in GaN layer to verify the 2-peak-fit method, where g2g stands for gate-to-gate spacing. z = 0 m is at the surface of SiN and GaN, and z = 2.171 m is at the surface of GaN and its substrate.

4.5 Summary and Conclusions

This chapter showed and discussed temperature and stress results of a three-dimensional finite-element thermal simulation of GaN-based HEMT structures. Most of the material had the temperature dependent properties. Several factors affecting the device self-heating have been taken into account and discussed including substrate material, substrate thickness, gate-to-gate spacing, gate width, and the interfacial resistances. Thermal stresses, which result from self-heating, are also modeled, and compared with each other. The main results can be summarized as follows.

(1) As the substrate thickness is increased, the channel temperature of GaN on SiC tends to increase much faster than that of GaN on Diamond since the thermal conductivity of SiC is much lower than that of GaN on Diamond.

(2) Temperature rise of 10 μm gate-to-gate spacing GaN on Diamond device, with 39.7 mm-K/W total resistance, is lower than that of 50 μm gate-to-gate spacing GaN on

SiC device, with 42.8 mm-K/W, for the same power dissipation and the same substrate thickness showing the promise of decreasing size by 5, whereas experiments showed 3× decreases in size.

(3) As the gate width gets shorter, channel temperature gets lower. And the gate width of GaN on Diamond device can be increased up to 650 μm, while that of GaN on SiC to 400 μm.

(4) Effect of the interfacial resistance layer is investigated that if direct growth of GaN on Diamond is obtainable, having the resistances between 20 and 60 m^2-K/GW, there will be only ~5 % difference in temperature.

(5) Although the CTE mismatch of GaN and SiC (23 %) is about a third of GaN and Diamond (73 %), the highest thermal conductivity of Diamond superiorly reduce the temperature at the active region. This consequences in lowering thermal stresses in GaN on Diamond than GaN on SiC, which shows the promise of utilizing Diamond as AlGaN/GaN HEMTs.

(6) Metallization from ohmic contacts adds tensile strain in GaN layer ~50 MPa at 4.2 W/mm and ~90 MPa at 6.9 W/mm.

(7) Bi-axial stress state is also confirmed for GaN on SiC and GaN on Diamond, which confirms the experimental results from Chapter 3.

(8) To improve the thermal reliability of GaN HEMTs, devices should be designed with shorter gate-width and larger gate-to-gate spacing with higher thermal conductive material such as diamond, which must have a lower interfacial resistance with GaN and other buffer/adhesive layers. Even though high CTE mismatch exists, high thermal conductive material will reduce the thermal stresses.

CHAPTER 5: ENVIRONMENTAL RELIABILITY OF ALGAN/GAN HEMTs

5.1 Introduction

Wide bandgap semiconductors made from group III-Nitrides comprise a critical technology for the advancement of both power electronics and high power wireless communications. Devices made from heterojunctions of AlGaN and GaN possess traits such as high electron mobility, breakdown fields that are 10× that of Si, high temperature stability, and fast switching speeds, which make them attractive for replacements to GaAs in wireless devices and Si in power electronic modules [7, 16, 17]. While much promise has been shown in the development of AlGaN/GaN technology, a physical understanding of the mechanisms governing the reliability of these devices remains to a subject of intense investigation. Several studies have recently identified the degradation mechanisms with regard to inverse piezoelectric effects, trap generation effects, ohmic and gate metal degradation, and charge trapping at the HEMT surface causing current collapse [24, 26, 27, 29, 30, 40, 41, 44, 46, 48, 49, 109]. Also, recent studies suggest that the degradation in these devices not only depends on temperature, but also exposure to environmental oxidants such as water vapor [29, 30, 110]. Thus, packaging and device architectural issues will play an important role in the long term reliability of these devices.

In recent years, the development of environmental barrier coatings has been used widely to improve the lifetimes of other devices such as organic electronics when exposed to atmospheric conditions. These coatings aim to achieve very low diffusion rates of oxygen and water vapor into the packaged devices, with effective water vapor transmission rates (WVTRs) less than 10^{-5} g/m^2/day. This can be achieved through vacuum deposited multilayer organic-inorganic coatings [111-115], ultra-low defect atomic layer deposition (ALD) coatings [116-119], and hybrid

coatings containing plasma enhanced CVD (PECVD) coatings that are capped with ALD coatings in order to seal the defects from PECVD and provide ultralow water vapor transmission rates [120]. Since the PECVD films have defects, which provide permeation pathways for water vapor and oxygen, the passivation layer by PECVD SiN_x on AlGaN/GaN HEMTs will be threatened by water vapor and oxygen. Therefore, there is a possibility to borrow from the technology used in packaging organic electronics, and apply an ALD film, which is smooth, conformal, and pinhole-free, on top of the devices to provide protection from moisture.

To investigate the effect of water vapor and the use of barrier layers to protect the AlGaN/GaN HEMTs, we coated HEMTs with thin layers of Al_2O_3 and HfO_2 using atomic layer deposition (ALD). ALD is based on sequential and self-limiting surface reactions [121]. For example, the Al_2O_3 layer can be deposited using tri-methyl-aluminum (TMA, $Al(CH_3)_3$) and H_2O as shown in Figure 59. With the sequential 130 cycles of these reactions, it yields around 13 nm thick Al_2O_3 layer. This unique growth technique can provide atomic layer control and allow conformal films to be deposited on very high aspect ratio structures. The choice of HfO_2/Al_2O_3 layers arises from the ease of growth of alumina on the SiNx layer followed by the chemical stability of the HfO_2 layer in the presence of water [122]. Thus, the hafnia layer is solely to cap the alumina layer and prevent chemical reaction with this layer and to preserve the barrier performance. To test the efficacy of the ALD coated layer from the water vapor, we electrically stressed the uncoated and coated devices in a controlled humid condition at 85 % RH, and at an elevated temperature of 50 ℃ not only to solely investigate the effect of moisture, but to accelerate the degradation of the uncoated devices in the presence of moisture.

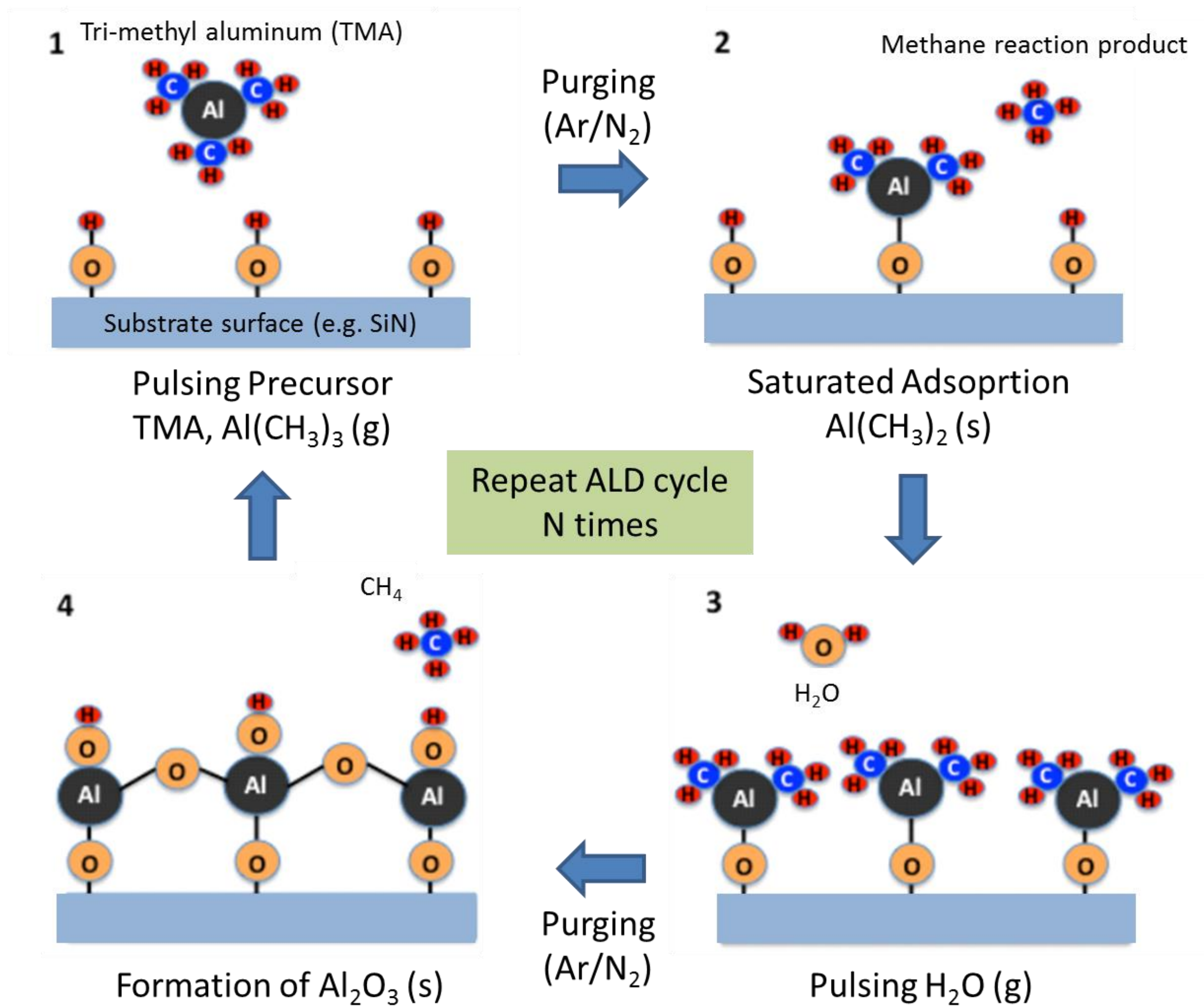


Figure 59: Schematic of the cyclic process of atomic layer depostion process on top of SiN passivation layer of AlGaN/GaN HEMTs. TMA is used as a pulsing precursor, then H_2O takes the methyl producing CH_4. Finally Al_2O_3 is formed on SiN layer on AlGaN/GaN HEMT.

In this study, we used the negative gate bias stress-induced degradation of AlGaN/GaN HEMTs. Namely, the negative gate bias stress applies the negative voltage between the gate and source to verify the critical voltage for degradation. As the electrical voltage stress increases, not it is possible to damage the lattice after the elastic energy reaches its critical value, but electrical degradation will also occur. The voltage where electrical degradation occurs is called the critical

voltage [49]. In the first set of conditions, the gate-source bias, V_{GS}, was decreased up to the critical voltage, where the degradation of devices started, at a fixed drain-source bias, V_{DS}, of 0V to exclude hot-electron effects on the channel [48, 49]. After reaching the critical voltage, we stressed devices for sufficiently long time, near the critical voltage to investigate the increase in defect concentration with photoluminescence [46]. Previously, other researchers showed that a hydrophobic material could be used to suppress the current collapse of AlGaN/GaN HEMTs [30]. However, these coatings are thick while ALD can provide excellent protection with nanometer scale coatings. While this previous study utilized ALD alumina coatings that failed, it was due to the instability of the alumina layer in humid environments, which is already known in the area of barrier films for organic electronics. The hafnia coated alumina layer is expected to provide improved stability. In addition, there was no discussion for the impact of these coatings in protecting the AlGaN/GaN HEMTs under the negative gate bias testing in the presence of water vapor. Thus, this study will help us understand how ALD coatings can perform in the environmental protection of these devices.

5.2 Experimental Set-up

The two-finger source-connected-field-plated (SCFP) AlGaN/GaN HEMTs were examined for these experiments. The gate width and gate to drain channel spacing were 50 μm and 1.5 μm, respectively. The thickness of the GaN buffer was ~2 μm, and semi-insulating 6H-SiC was used as the substrate material. The devices were attached to Cu/W packages with the silver-based epoxy at 150 °C for 20 minutes. Since the ALD coating is a conformal coating that coats the entire exposed system, we wire bonded the devices prior to the coating. The wire-bonded devices are shown in Figure 60 comparing between uncoated and coated devices. AlGaN/GaN HEMTs were coated using a Cambridge NanoTech Plasma ALD. During the deposition, the temperature

of the chuck was 100 °C to allow for low temperature deposition. The Al_2O_3 layer was deposited for 130 cycles, yielding around 13 nm, and then it was capped with HfO_2 for 20 cycles (about 2 nm) as shown in Figure 60. $HfCl_4$ was used as the precursor for the hafnia with H_2O as the oxidant. The reason why HfO_2 is used is because it is chemically resistant to reactions with water, as previously stated. In addition, the dielectric constant of HfO_2 is 25, whereas the dielectric constant of Al_2O_3, SiO_2, and Si_3N_4 are 9, 3.9, and 7.5 [103, 123]. Therefore, unlike other barrier films, HfO_2 has a strong dielectric behavior that can protect from water vapor or other contaminants causing electrical degradation.

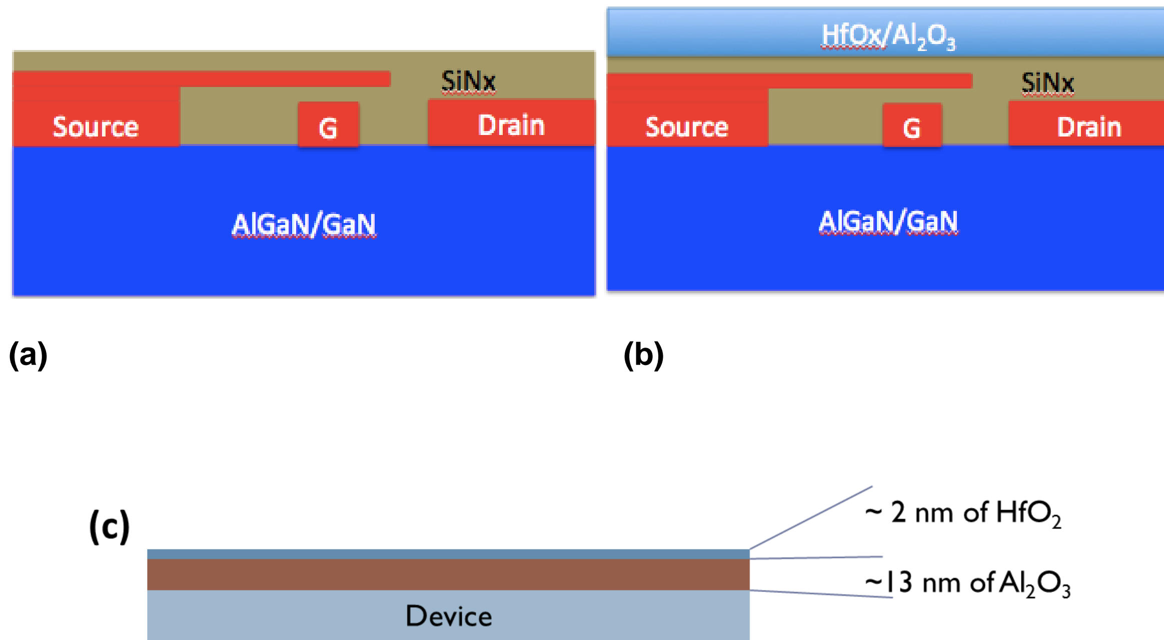


Figure 60: (a) Two finger source-connected-field-plated (SCFP) AlGaN/GaN HEMT before ALD coating (b) After ALD coating (c) The thickness of the coated layer on top of the device.

In order to investigate the effect of the barrier film, coated and uncoated devices were placed in a Cincinnati Subzero Micro Climate Humidity Chamber for testing under controlled humidity and the temperature conditions as shown in Figure 61. The temperature of the chamber was maintained at 50 °C and the humidity of 85 % relative humidity. Additional samples were tested

on a thermal stage held at 50 ℃ with the relative humidity of the laboratory air being about 30 %. Thus, we could isolate the impact of humidity on device performance by testing at similar temperatures.

Figure 61: Cambridge Fiji Plasma ALD system (Left), Cincinnati Subzero Micro Climate Humidity Chamber at 50 ℃ and 85 % RH (Right)

To investigate negative gate bias stress-induced degradation of AlGaN/GaN HEMTs, the HEMTs were step stressed with a Keithely 2400 series from $10V_{DG}$ to $140V_{DG}$ in 2V increments for 60 s each step, where $V_{DG} = V_{DS} – V_{GS}$. In the first set of conditions, the gate-source bias, V_{GS}, was increased up to the critical voltage, where the degradation of devices started, at a fixed drain-source bias, V_{DS}, of 0V to exclude hot-electron effects on the channel [48, 49]. The next step, after finding the critical voltage, we stressed devices for a sufficiently long time to investigate the increases in defect concentration for a lower voltage than the critical voltage [46]. As previous studies characterized stressed devices with time-resolved electroluminescence (EL) to investigate the increases in defect with increasing stress time qualitatively [46], we measured

the change in residual stress with photoluminescence (PL) quantitatively. A Horiba Jobin Yvon LabRAM HR800 was used for micro-Photoluminescence experiments, where a 325 nm He-Cd laser was used as the excitation source. The spectrometer had a focal length of 800 mm, and was equipped with a liquid N_2 cooled backside illuminated charged-coupled device (CCD) detector. A 1800 groove/mm diffraction grating was used and the confocal hole size was adjusted to 100 µm with a 39X UV lens as shown in Figure 62.

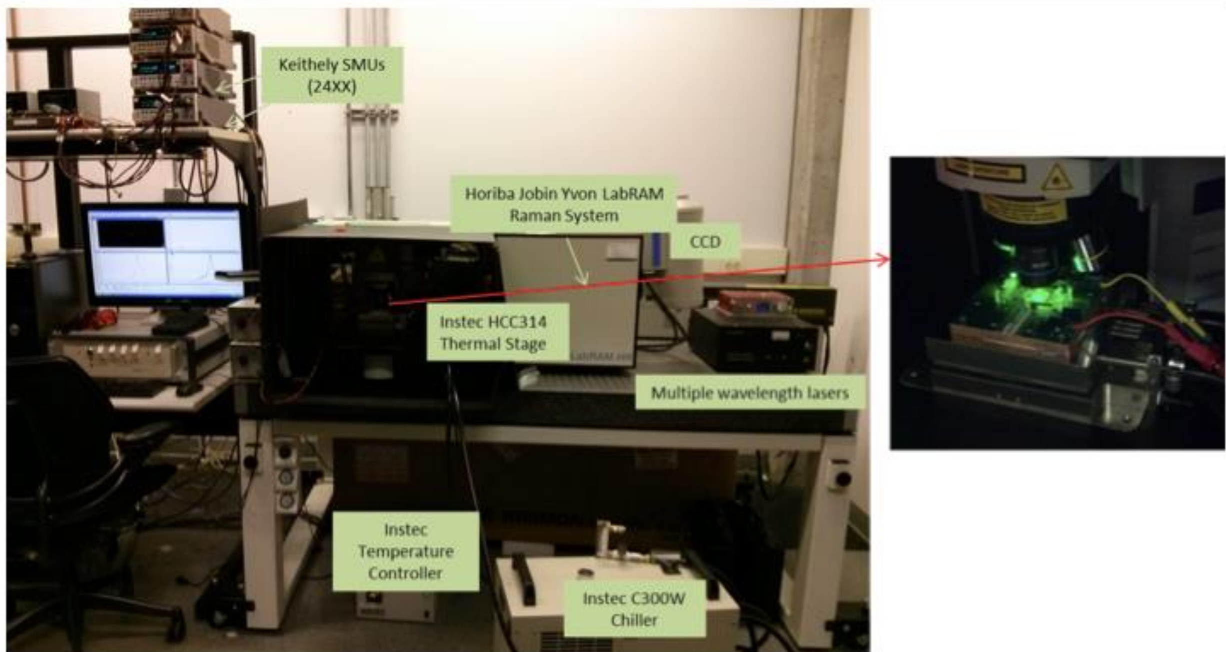


Figure 62: Schematic of experimental apparatus including spectrometer and peripherals used for measuring residual stresses of AlGaN/GaN HEMTs

Similar to Raman spectroscopy, PL spectroscopy is a non-contact, nondestructive method of probing the electronic structure of materials. Basically, light is directed onto a sample, where it is absorbed and photoexcitation can occur. As shown in Figure 63, the photoexcitation causes electrons to move to a higher energy state (green arrow), and upon relaxation, energy is released

in the form of photons with an energy related to the bandgap (red arrow). Usually, in semiconductors, these transitions occur between states in the conduction and valence bands, where the energy of interband transition is known as the bandgap energy (E_g). Therefore, PL spectroscopy gives a direct measure of the bandgap of semiconductors. Even though micro-Raman spectroscopy can measure the stress, visible lasers (488/532 nm) average the GaN layer since it has lower energy than the bandgap of GaN as shown in Figure 64. Therefore, 325 nm UV laser was used for PL with since its energy (3.8 eV) is higher than the bandgap of GaN (3.4 eV). Since the bandgap is sensitive to the state of the strain, and change in stress will indicate degradation. If defects are generated in the active area, lattice relaxation can occur resulting in the initially strained AlGaN/GaN layer to relax [124].

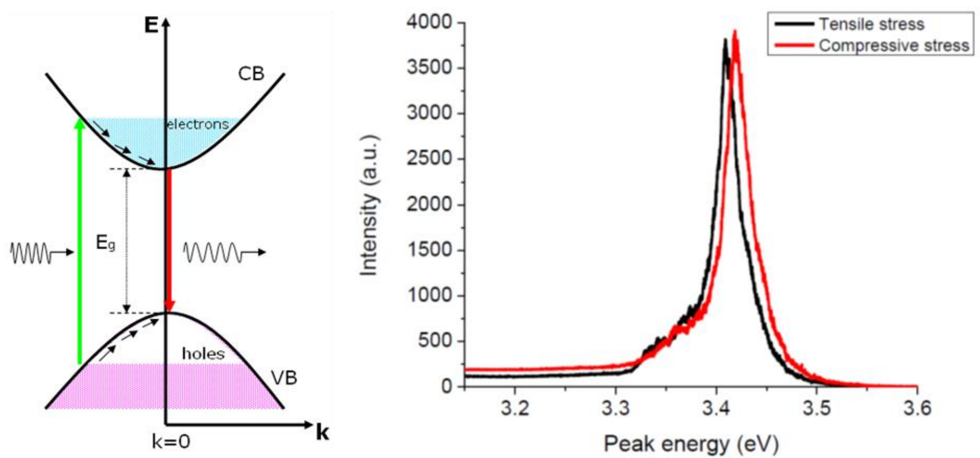


Figure 63: (Left) PL is the phenomenon of light emission from a matter after the absorption of photons, (Right) PL spectra of GaN epifilms unde tensile and compressive stress [125].

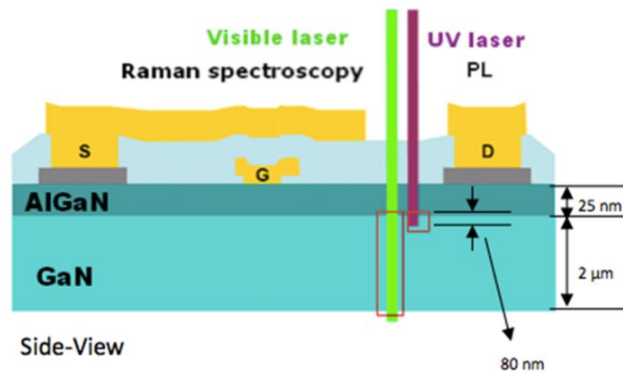


Figure 64: Schematic of depth of laser into AlGaN/GaN HEMTs showing that only visible laser penetrates GaN layer since the laser energy is lower than GaN Band-gap [125]

5.3 Results and Discussion

5.3.1 Step-Stress-test

Before testing the function of the barrier film on AlGaN/GaN HEMTs inside the humidity chamber for the environmental study, the behavior of the devices were investigated in laboratory air (30% RH) as a baseline. The sample temperature was elevated by testing them on a thermal stage held at 50 ℃. In this study, four different devices were tested as shown in Figure 65: two uncoated devices and two ALD-coated devices were tested in laboratory air (50 ℃, 30 % RH) and in the environmental chamber condition (50 ℃, 85 % RH). V_{DS} was stepped in 1 V increments from 10 to 140 V, or V_{GS} was stepped from −10 to −140 V, while the source and drain were grounded in order to stress both sides of the gate finger simultaneously (V_{DS} = 0 V) to avoid self-heating, and the devices were stressed for 60 s at each voltage step followed by an I-V sweep to check for degradation.

Figure 65 shows the results of IV sweep: the gate current at nearly off state (V_{GS} = -5 V, V_{DS} = 0.1 V), the gate current during stressing the device, and the drain current at mostly open state (V_{GS} = 2 V, V_{DS} = 5 V) versus stress voltage at V_{DS} = 0 V (source and drain grounded). When

the gate current begins to rise or the drain current begins to drop, it is indicating the degradation of the device. After a certain point, the stress current ($I_{Gstress}$) increases with stress voltage and increases by about one order of magnitude, which is similar to all other step-stressing reliability studies [24, 27, 46, 109]. For the devices tested in this study, the increment in the gate current or drop in the drain current occur around 130 V_{DG}, which is considered as the critical voltage for this type of devices. The critical voltage of 130 V was observed for devices tested in the laboratory air conditions and for devices with the ALD coating for both laboratory air and the humidity chamber.

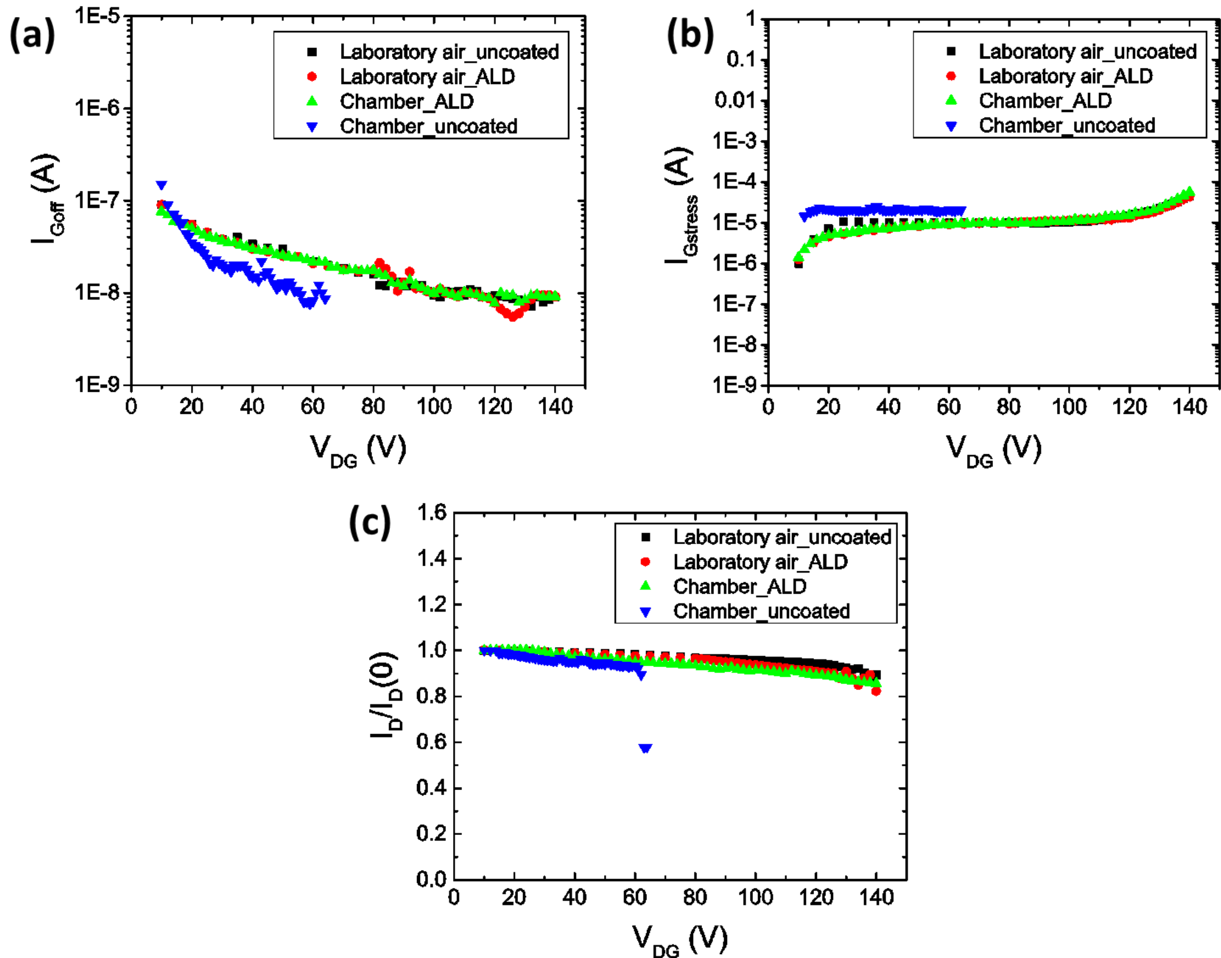


Figure 65: Devices were stressed from 10V_{DG} to 140V_{DG} in 2V increments for 60 s each step, where $V_{DG} = V_{DS} - V_{GS}$ at V_{DS} = 0V. (a) I_{Goff} vs. V_{DG}, where I_{Goff} is gate current after each stress

at V_{GS} = -5 V, V_{DS} = 0.1 V, (b) $I_{Gstress}$ vs. V_{DG}, where $I_{Gstress}$ is gate stress current during stressing, (c) $I_D/I_{D(0)}$ vs. V_{DG}, where I_D is drain current at V_{GS} = 2 V, V_{DS} = 5 V and $I_{D(0)}$ is drain current before stressing.

When uncoated devices were stressed in the humid condition, there were sudden changes in all electrical characteristics around 65 V_{DG}, having very high gate current leakage, or large drop in drain current, which shows that the critical voltage in the humidity chamber was lower by a factor of 2 when placed in air at 85%. Therefore, the effect of the ALD barrier film shows some improvement in the protection of the devices, since they behave as the baseline device in laboratory air, in spite of being placed in the humidity chamber. Moreover, early degradation of the uncoated device at the humid condition indicates that the water vapor affects the reliability of the AlGaN/GaN HEMTs. To investigate further this effect of the ALD barrier films in the humidity chamber, devices were tested at a voltage lower than the critical voltage to look at time dependent effects as seen in previous studies [46].

5.3.2 Time Dependent Degradation Study

In this section, changes in the IV characteristics and residual stresses are shown for the time-dependent degradation study of coated and uncoated devices. First, to characterize I-V of AlGaN/GaN HEMTs, the stress voltage was applied at 60 V_{DG}, which is lower than the critical voltage of normal condition device (~130 V_{DG}), but close to the critical voltage of the uncoated device in the humidity chamber as shown in previous section. The stress was applied for a sufficiently long time for several steps (300, 3000, and 8500 s are included in results) for the uncoated device to degrade in the humidity chamber. After stressing the devices, an I-V sweep was performed showing the change in IV characteristics as response to time as shown in Figure 66. Figure 66 (a) shows the change in transconductance (g_m), which is the reciprocal of

resistance, or the ratio of the drain current change to the gate voltage change. Therefore, decrease in maximum transconductance ($g_{m, max}$) means the degradation in the transfer characteristics. The transconductance decreased from 24 mS to 21 mS (where mS = mA/V), showing a decrease of about 12.5 % from the fresh condition as shown in Figure 66 (c). In addition to the reduction of g_m of uncoated device in the humid condition, the threshold voltage increased from −3.2 V_{GS} to −2.8 V_{GS}. The increment of threshold voltage signifies that a larger gate–source voltage due to increasing channel resistance needs to be applied to allow the drain current to flow, thus meaning the degradation of the device as shown in Figure 66 (c).

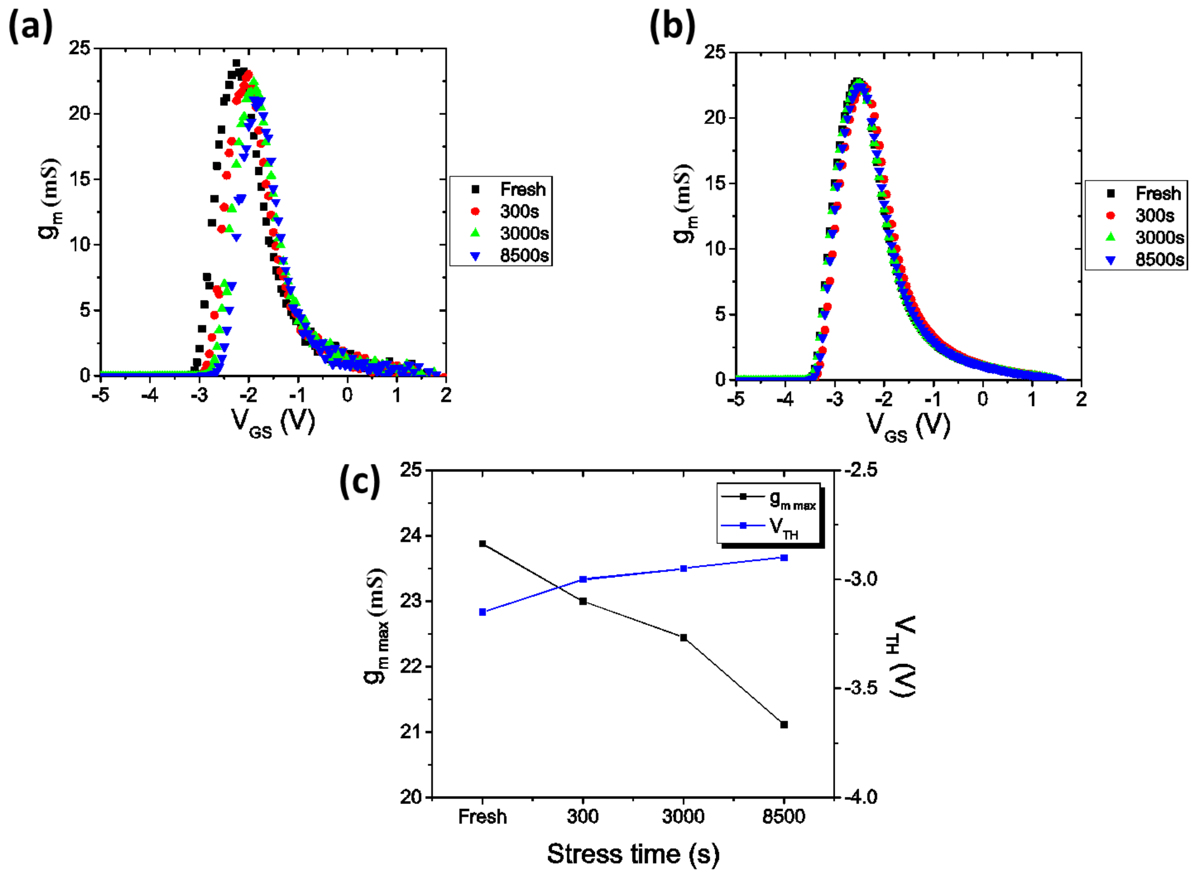


Figure 66: Transconductance (g_m) vs. V_{GS} (V) for time-dependent study in the humid condition: (a) Uncoated device, (b) ALD-coated device (Uncoated and coated devicces in laboratory air conditions are not shown here since both showed similar characteristics that have no changes as (b) shows, (c) maximum transconductance and threshold voltage (V_{TH}) extracted from (a)

Figure 67 shows the drain current vs. the drain voltage for different devices, comparing between their fresh condition and the stressed condition after 8500 s at V_{DG} = 60 V. Only the uncoated devices in the humid condition showed the degradation showing the effect of the water vapor during stressing. At the fully opened condition, V_{GS} = 2 V & V_{DS} = 10 V, the saturated drain current dropped from ~100 mA to ~60 mA showing 40 % decrease, which is significant. However, the coated device showed no signs of degradation over this same period of time for both laboratory air and humidity chamber testing.

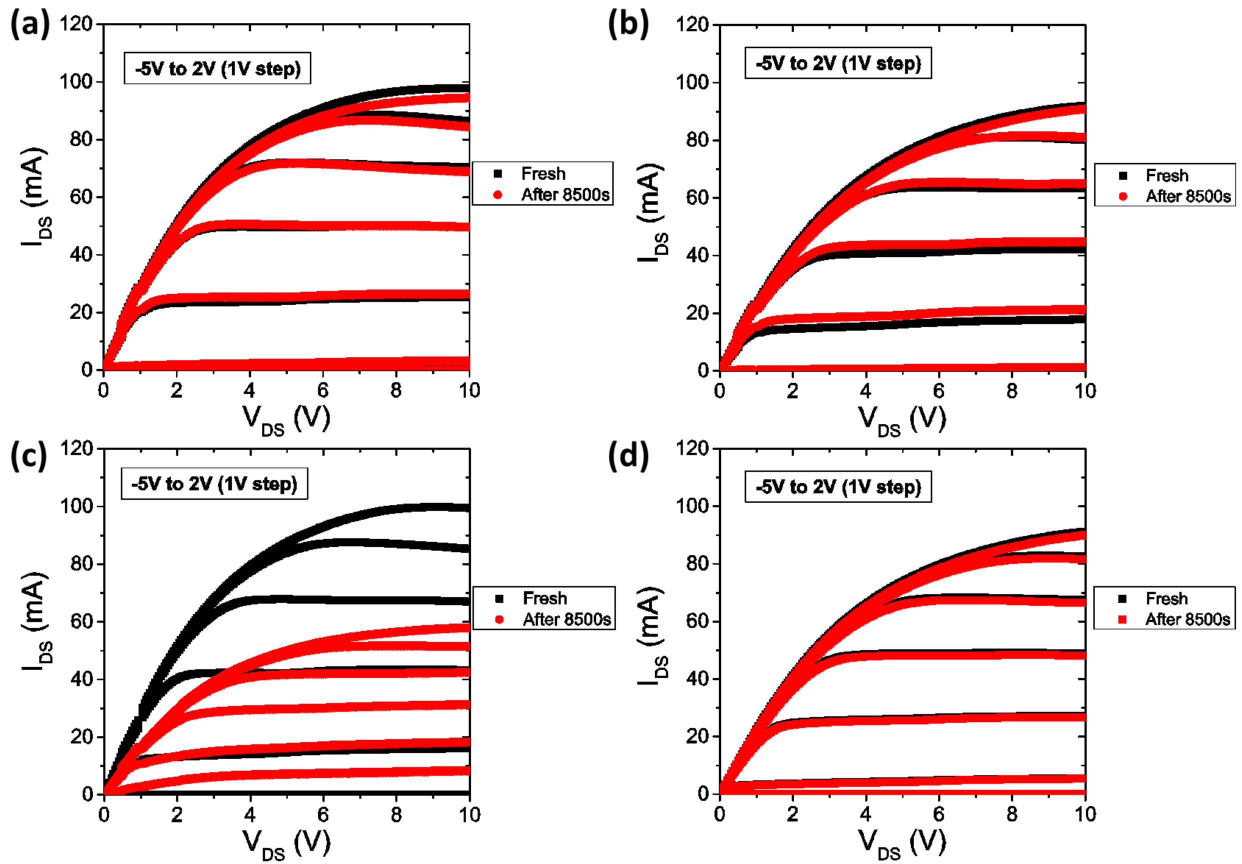


Figure 67: I_{DS} vs. V_{DS} curve comparing between fresh devices and stressed devices after 8500 s. (a) Uncoated device in the laboratory air condition, (b) ALD-coated device in the laboratory air condition, (c) Uncoated device in the humid condition, and (d) ALD-coated device in the humid condition

Finally, utilizing PL, residual stress in the channel was measured to determine if stress relaxation occurred during stressing. Before stressing the devices, the initial state of the residual stress was measured. All of the tested devices showed a similar level of the initial residual stress, ~500 MPa as shown in Figure 68, before the step-stress-test / time-dependent degradation study. The huge uncertainty (~ ±50 MPa) comes from the calibration constants and the uncertainty in elastic constants for bare GaN samples [126].

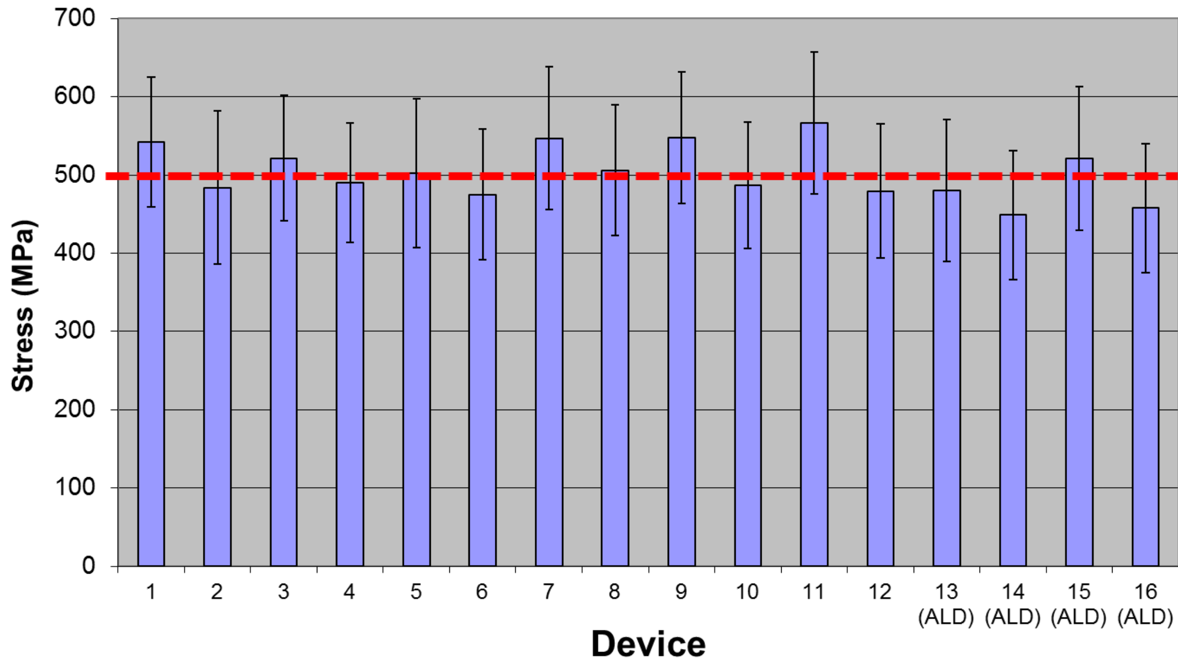


Figure 68: Residual stresses of tested devices before stressing; each numbers corresponds to the tested devices; 13~16 are ALD-coated devices. The averaged value of all devices is ~500 MPa.

When the defects are generated in channels because of the degradation, lattice relaxation may occur, which will cause a reduction in residual stress. The results of this study are shown in Figure 69. For this relaxation study, the uncoated devices were tested near its critical voltage, 130 V_{DG}, in laboratory air. As the stress time increases, a slight decrease in stress is observed until device failure occurs where a large drop in stress is seen. Initially, the residual stress of the device in Figure 69 was ~490 MPa, and after stressing it for 3000 s, it reduced to ~430 MPa showing 12 % decrease. Then, after permanent degradation, which occurred after ~6000 s, the residual stress close to the damaged location after device failure ~350 MPa showing 30 % decrease. While these data do not clearly identify the mechanism for the slight stress decrease, it is believed to be due to damage forming in the device channel which was detected by PL.

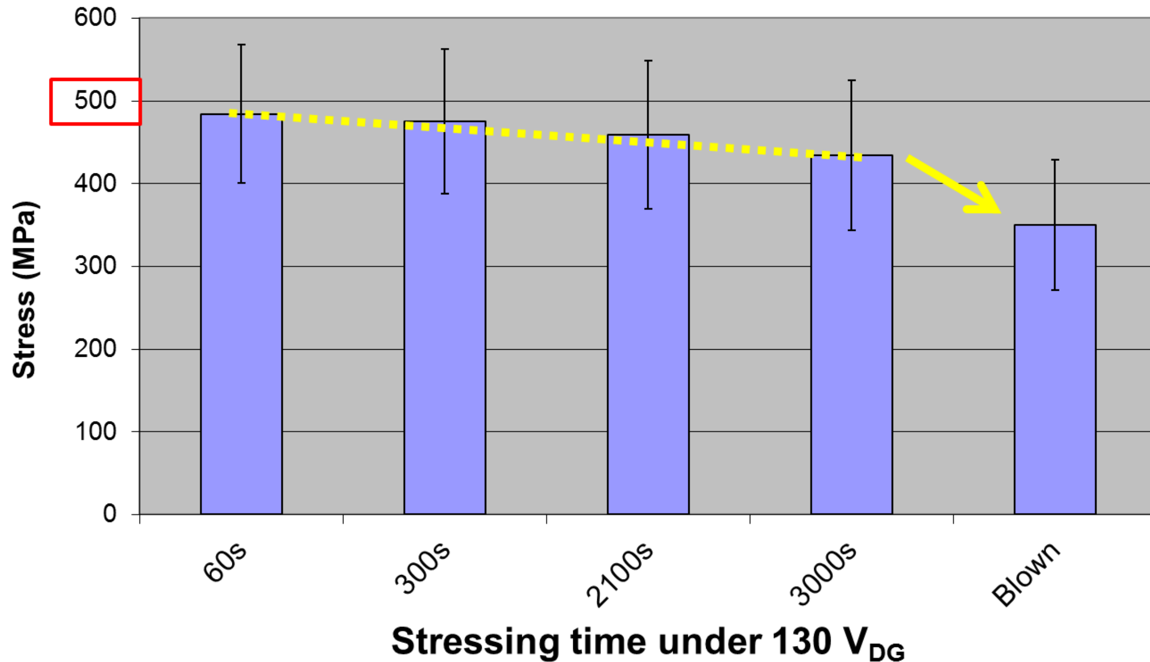


Figure 69: Decrease in residual stress as defects are formed, or lattice relaxation occurs. After a certain time, device blew up showing the lowest residual stress.

5.4 Summary and Conclusions

This chapter showed the effect of water vapor on device reliability and the effectiveness of ALD barrier films deposited using Al_2O_3 and HfO_2 on protecting devices in this environment. The reliability studies were performed under the negative-gate-bias step-stress-tests with the time dependent experiments. The degradation of HEMTs and the efficiency of ALD-coated layers were verified using IV characterization and PL measurements. The main results can be summarized as follows.

(1) The critical voltages of the uncoated device and the ALD-coated device in laboratory air, but elevated conditions (50 ℃ and 30 % RH) and the coated device in the humid condition (50 ℃ and 85 % RH) were 130 V_{DG} at V_{DS} = 0 V, whereas the critical voltage

of the uncoated device in the humid condition was 65 V_{DG} showing. This result demonstrates the ability to protect the devices using the ALD barrier.

(2) The time dependent study, at voltages lower than the critical voltage (60 V_{DG}), was conducted to support the merit of the ALD-coated barrier film. The uncoated device in the humid condition degraded with time, while the ALD-coated device did not degrade in the same condition.

(3) PL measurements were executed to measure the residual stresses of the devices. Decrease in the stress means the formation of defects, which results from the lattice relaxation after the degradation from high reverse bias stress (130 V_{DG}).

(4) It was confirmed that the ALD barrier film not only improved the environmental reliability, protecting from water vapor, but that the coating can lead to a more robust method of storage and using the devices in addition to hermetic sealing.

CHAPTER 6: CONCLUSION AND FUTURE WORK

AlGaN/GaN high electron mobility transistors (HEMTs) are very promising semiconductor devices for high power, high frequency, and high temperature applications such as radar and communications. The unique combination of large bandgap, high saturated drift velocity, large polarization field, and high breakdown field of AlGaN and GaN make them excellent materials for HEMT devices. These HEMTs handle more than one order of magnitude higher power densities than any other semiconductor such as GaAs or Si based devices. However, in spite of the excellent performance demonstrated by these devices, their markets are still limited by their reliability. The localized self-heating limits the peak power density and degrades device reliability. Also, behind electrical reliability, there have been recent studies to understand the fundamental failure mechanisms, but they are still not clearly understood yet including the environmental effects on the devices.

The purpose of this thesis was to address the thermal and the environmental reliability of AlGaN/GaN HEMTs. To improve the thermal reliability of these devices, CVD diamond substrates were utilized instead of SiC substrates. Even though there have been some difficulties in integration of GaN on diamond because of lattice mismatch and CTE mismatch with high cost, recent efforts have used chemical-vapor-deposited (CVD) diamond substrates for AlGaN/GaN HEMTs. Integration of diamond substrates within a few micrometers of the hot region can be a fascinating materials solution for thermal management because CVD diamond can have a thermal conductivity greater than1500 W/m-K, which is much higher than those of SiC substrate (~490 W/m-K) used for commercialized AlGaN/GaN HEMTs.

The benefits of using a CVD diamond substrate was demonstrated experimentally by comparing the thermal performance of devices made on SiC to those made on CVD diamond.

The results showed that it was possible to reduce the size of the GaN on diamond device by a factor of three when compared to the GaN on SiC at the same power level while coming within 10% of the same device temperature. The temperatures of both devices were measured via micro-Raman thermometry showing that there was only 6 % increase in peak junction temperature for the GaN on diamond HEMT. Therefore, this elucidates the importance of the high conductivity diamond substrate at high HEMT areal power dissipation density (420 vs. 120 W/mm^2, GaN on diamond and GaN on SiC, respectively). The potential of GaN on diamond as a means to increase HEMT power density will enable smaller, higher power density integrated circuits in micro-sizes.

In addition, finite element modeling was performed to modify the structure of AlGaN/GaN HEMTs for better thermal management. Even though it was shown in experiments that diamond as a substrate dominates other substrate materials, the growth technique of GaN on diamond is nascent compared to that of GaN on Si or SiC, interfacial resistances in GaN/AlN buffer (adhesion layer)/diamond vary a lot. Also, the geometric structure of HEMTs affects the heat propagation. Therefore, parametric studies with different substrate material, substrate thickness, gate-to-gate spacing, gate width, and the interfacial resistances were performed. As a result, larger gate-to-gate spacing, shorter gate width, and smaller interfacial resistances showed lower temperature rise. Nonetheless, it was shown by modeling that actually a factor of 5 size reduction may be possible with GaN on diamond when compared to GaN on SiC.

On top of the electric field driven degradation, to enhance the environmental reliability of AlGaN/GaN HEMTs, barrier films were deposited by atomic layer deposition (ALD) to protect these devices from the water vapor. Al_2O_3 and HfO_2 were used for the barrier film, which were deposited only for 15 nm. First of all, the critical voltages of devices were measured by negative

gate bias step stress tests for both humid and laboratory air conditions. To verify the effect of these barrier films, uncoated devices and ALD-coated devices were tested in the humidity chamber for sufficiently long time at 60 V_{DG}, which is near the critical voltage of uncoated device in humidity chamber, whereas the critical voltage of other devices was ~130 V_{DG}. By measuring transfer characteristics: transconductance and threshold voltage, and output characteristics: I_{DS} vs. V_{DS} of coated and uncoated devices, before and after stressing the device, the effect of ALD coating was confirmed. PL measurements were also performed to measure the residual stresses of the devices that decrement in the stress indicated the lattice relaxation after the degradation from high reverse bias stress, 130 V_{DG}. Therefore, the barrier film by ALD coatings improved the environmental reliability, protecting from the oxidants, water vapor, and contaminants, and decrease the size of packaging as well.

Future Work

Continued research in AlGaN/GaN HEMTs regarding their reliability issues is important. As finite element modeling showed the low thermal resistance between the interfacial layer of GaN and diamond affects heat spreading, improvements of growth of diamond and its integration with GaN needs to be investigated for better thermal reliability. The role of stress in the device performance is not clear and should be studied since diamond is a much stiffer substrate than SiC with a larger CTE mismatch with GaN. Also, the issue of device reliability is of concern during electrical stressing. Since this is a newer technique for making AlGaN/GaN HEMTs, it is clear that studies must be performed to understand the device reliability implications are for this new system. While enhanced thermal performance was shown, it is not merited if the electrical

performance is compromised. Furthermore, higher power densities and higher electric fields will be seen in the devices which can have reliability implications.

For the barrier film effect study to improve the environmental reliability, changing the thickness of barrier layer with various materials should be performed. In addition, changing the step-stress-condition from negative-bias-condition to forward-bias-condition which are more realistic in terms of device operation needs to be performed. For degraded devices, post processing to determine the failure mechanisms is required to shed more light onto this topic. In addition to PL stress measurements, TEM/SEM analysis of devices will be helpful to understand the crystallographic defects in degraded devices. Also, surface analytical techniques such as Auger electron spectroscopy, which shows the particles on top of the device surface, will support the effect of ALD-coating that the presence of water will accelerate the degradation.

REFERENCES

[1] J. Shealy, J. Smart, M. Poulton, R. Sadler, D. Grider, S. Gibb*, et al.*, "Gallium nitride (GaN) HEMT's: progress and potential for commercial applications," in *Technical digest-IEEE Gallium Arsenide Integrated Circuit Symposium*, 2002, pp. 243-246.

[2] K. Gurnett and T. Adams, "Considerations for GaN-powered base stations," *III-Vs Review,* vol. 19, pp. 20-22, 2006.

[3] S. Elhamri, A. Saxler, W. Mitchel, R. Berney, C. Elsass, Y. Smorchkova*, et al.*, "Study of deleterious aging effects in GaN/AlGaN heterostructures," *Journal of applied physics,* vol. 93, pp. 1079-1082, 2002.

[4] Y. F. Wu, B. Keller, S. Keller, D. Kapolnek, P. Kozodoy, S. Denbaars*, et al.*, "Very high breakdown voltage and large transconductance realized on GaN heterojunction field effect transistors," *Applied physics letters,* vol. 69, pp. 1438-1440, 1996.

[5] S. Saygi, H. Fatima, X. He, S. Rai, A. Koudymov, V. Adivarahan*, et al.*, "Performance stability of high-power III-nitride metal-oxide semiconductor-heterostructure field-effect transistors," *physica status solidi (c),* vol. 2, pp. 2651-2654, 2005.

[6] Y. F. Wu, M. Moore, A. Saxler, T. Wisleder, and P. Parikh, "40-W/mm Double Field-plated GaN HEMTs," in *Device Research Conference, 2006 64th*, 2006, pp. 151-152.

[7] U. K. Mishra, P. Parikh, and W. Yi-Feng, "AlGaN/GaN HEMTs-an overview of device operation and applications," *Proceedings of the IEEE,* vol. 90, pp. 1022-1031, 2002.

[8] M. Bhatnagar and B. J. Baliga, "Comparison of 6H-SiC, 3C-SiC, and Si for power devices," *Electron Devices, IEEE Transactions on,* vol. 40, pp. 645-655, 1993.

[9] T. Chow, V. Khemka, J. Fedison, N. Ramungul, K. Matocha, Y. Tang*, et al.*, "SiC and GaN bipolar power devices," *Solid-State Electronics,* vol. 44, pp. 277-301, 2000.

[10] *Radar System*. Available: http://www.offshore.no/international/news/article.aspx?id=16493

[11] *Satellite*. Available: http://www.lockheedmartin.com/us/news/press-releases/2013/september/0912-ss-aehf.html

[12] *epiGaN*. Available: http://www.powerguru.org/gan-on-si-materials-optimised-for-high-power-electronics/

[13] "Power Electronics in Hybrid Electric Vehicles."

[14] *GaN diagram*. Available: http://www.gansystems.com/why_gallium_nitride.php

[15] H. Sakaki, G. Yusa, T. Someya, Y. Ohno, T. Noda, H. Akiyama*, et al.*, "Transport properties of two-dimensional electron gas in AlGaAs/GaAs selectively doped heterojunctions with embedded InAs quantum dots," *Applied physics letters,* vol. 67, pp. 3444-3446, 1995.

[16] O. Ambacher, B. Foutz, J. Smart, J. R. Shealy, N. G. Weimann, K. Chu*, et al.*, "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaN/GaN heterostructures," *Journal of Applied Physics,* vol. 87, pp. 334-344, 01/01/ 2000.

[17] F. Bernardini, V. Fiorentini, and D. Vanderbilt, "Spontaneous polarization and piezoelectric constants of III-V nitrides," *Physical Review B,* vol. 56, pp. R10024-R10027, 10/15/ 1997.

[18] A. Bykhovski, R. Gaska, and M. Shur, "Piezoelectric doping and elastic strain relaxation in AlGaN–GaN heterostructure field effect transistors," *Applied physics letters,* vol. 73, pp. 3577-3579, 1998.

[19] O. Ambacher, J. Smart, J. Shealy, N. Weimann, K. Chu, M. Murphy, *et al.*, "Two-dimensional electron gases induced by spontaneous and piezoelectric polarization charges in N-and Ga-face AlGaN/GaN heterostructures," *Journal of Applied Physics,* vol. 85, pp. 3222-3233, 1999.

[20] L. F. Eastman, V. Tilak, J. Smart, B. M. Green, E. M. Chumbes, R. Dimitrov, *et al.*, "Undoped AlGaN/GaN HEMTs for microwave power amplification," *Electron Devices, IEEE Transactions on,* vol. 48, pp. 479-485, 2001.

[21] P. Asbeck, E. Yu, S. Lau, G. Sullivan, J. Van Hove, and J. Redwing, "Piezoelectric charge densities in AlGaN/GaN HFETs," *Electronics letters,* vol. 33, pp. 1230-1231, 1997.

[22] E. Yu, G. Sullivan, P. Asbeck, C. Wang, D. Qiao, and S. Lau, "Measurement of piezoelectrically induced charge in GaN/AlGaN heterostructure field-effect transistors," *Applied physics letters,* vol. 71, pp. 2794-2796, 1997.

[23] S. Jain, A. Harker, and R. Cowley, "Misfit strain and misfit dislocations in lattice mismatched epitaxial layers and other systems," *Philosophical Magazine A,* vol. 75, pp. 1461-1515, 1997.

[24] J. A. del Alamo and J. Joh, "GaN HEMT reliability," *Microelectronics reliability,* vol. 49, pp. 1200-1206, 2009.

[25] E. Heller, S. Choi, D. Dorsey, R. Vetury, and S. Graham, "Electrical and structural dependence of operating temperature of AlGaN/GaN HEMTs," *Microelectronics Reliability,* vol. 53, pp. 872-877, 2013.

[26] M. Kuball, M. Ťapajna, R. J. Simms, M. Faqir, and U. K. Mishra, "AlGaN/GaN HEMT device reliability and degradation evolution: Importance of diffusion processes," *Microelectronics Reliability,* vol. 51, pp. 195-200, 2011.

[27] G. Meneghesso, G. Verzellesi, F. Danesin, F. Rampazzo, F. Zanon, A. Tazzoli, *et al.*, "Reliability of GaN high-electron-mobility transistors: state of the art and perspectives," *Device and Materials Reliability, IEEE Transactions on,* vol. 8, pp. 332-343, 2008.

[28] S. DasGupta, L. B. Biedermann, M. Sun, R. Kaplar, M. Marinella, K. R. Zavadil, *et al.*, "Role of barrier structure in current collapse of AlGaN/GaN high electron mobility transistors," *Applied Physics Letters,* vol. 101, pp. 243506-243506-4, 2012.

[29] F. Gao, B. Lu, L. Li, S. Kaun, J. S. Speck, C. Thompson, *et al.*, "Role of oxygen in the OFF-state degradation of AlGaN/GaN high electron mobility transistors," *Applied Physics Letters,* vol. 99, pp. 223506-223506-3, 2011.

[30] F. Gao, D. Chen, B. Lu, H. L. Tuller, C. V. Thompson, S. Keller, *et al.*, "Impact of Moisture and Fluorocarbon Passivation on the Current Collapse of AlGaN/GaN HEMTs," 2012.

[31] K. Boutros, P. Rowell, and B. Brar, "A study of output power stability of GaN HEMTs on SiC substrates," in *Reliability Physics Symposium Proceedings, 2004. 42nd Annual. 2004 IEEE International*, 2004, pp. 577-578.

[32] X. B. Zhang, T. Taliercio, S. Kolliakos, and P. Lefebvre, "Influence of electron-phonon interaction on the optical properties of III nitride semiconductors," *Journal of Physics-Condensed Matter,* vol. 13, pp. 7053-7074, Aug 13 2001.

[33] S. Sridharan, A. Venkatachalam, and P. Yoder, "Electrothermal analysis of AlGaN/GaN high electron mobility transistors," *Journal of Computational Electronics,* vol. 7, pp. 236-239, 2008.

[34] A. Matulionis, "Hot phonons in GaN channels for HEMTs," *Physica Status Solidi a-Applications and Materials Science,* vol. 203, pp. 2313-2325, Aug 2006.

[35] A. Christensen and S. Graham, "Multiscale Modeling of Hot Spots in Gan High Electron Mobility Transistors," *Ipack 2009: Proceedings of the Asme Inter Pack Conference 2009, Vol 1,* pp. 535-541, 2010.

[36] H. Siegle, G. Kaczmarczyk, L. Filippidis, A. Litvinchuk, A. Hoffmann, and C. Thomsen, "Zone-boundary phonons in hexagonal and cubic GaN," *Physical Review B,* vol. 55, p. 7000, 1997.

[37] P. Burgaud, L. Constancias, G. Martel, C. Savina, and D. Mesnager, "Preliminary reliability assessment and failure physical analysis on AlGaN/GaN HEMTs COTS," *Microelectronics Reliability,* vol. 47, pp. 1653-1657, 2007.

[38] S. P. McAlister, J. A. Bardwell, S. Haffouz, and H. Tang, "Self-heating and the temperature dependence of the dc characteristics of GaN heterostructure field effect transistors," *Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films,* vol. 24, p. 624, 2006.

[39] S. Singhal, T. Li, A. Chaudhari, A. Hanson, R. Therrien, J. Johnson*, et al.*, "Reliability of large periphery GaN-on-Si HFETs," *Microelectronics Reliability,* vol. 46, pp. 1247-1253, 2006.

[40] P. Makaram, J. Joh, J. A. del Alamo, T. Palacios, and C. V. Thompson, "Evolution of structural defects associated with electrical degradation in AlGaN/GaN high electron mobility transistors," *Applied Physics Letters,* vol. 96, pp. 233509-3, 06/07/ 2010.

[41] G. Meneghesso, F. Rampazzo, P. Kordos, G. Verzellesi, and E. Zanoni, "Current collapse and high-electric-field reliability of unpassivated GaN/AlGaN/GaN HEMTs," *Electron Devices, IEEE Transactions on,* vol. 53, pp. 2932-2941, 2006.

[42] G. Meneghesso, G. Verzellesi, R. Pierobon, F. Rampazzo, A. Chini, U. K. Mishra*, et al.*, "Surface-related drain current dispersion effects in AlGaN-GaN HEMTs," *Electron Devices, IEEE Transactions on,* vol. 51, pp. 1554-1561, 2004.

[43] R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, "The impact of surface states on the DC and RF characteristics of AlGaN/GaN HFETs," *Electron Devices, IEEE Transactions on,* vol. 48, pp. 560-566, 2001.

[44] J. Joh, J. A. d. Alamo, K. Langworthy, S. Xie, and T. Zheleva, "Role of stress voltage on structural degradation of GaN high-electron-mobility transistors," *Microelectronics Reliability,* vol. 51, pp. 201-206, 2011.

[45] J. Jungwoo and J. A. del Alamo, "Critical Voltage for Electrical Degradation of GaN High-Electron Mobility Transistors," *IEEE Electron Device Letters,* vol. 29, pp. 287-289, 2008.

[46] M. Meneghini, A. Stocco, M. Bertin, D. Marcon, A. Chini, G. Meneghesso*, et al.*, "Time-dependent degradation of AlGaN/GaN high electron mobility transistors under reverse bias," *Applied Physics Letters,* vol. 100, pp. 033505-033505-3, 2012.

[47] S. Y. Park, C. Floresca, U. Chowdhury, J. L. Jimenez, C. Lee, E. Beam*, et al.*, "Physical degradation of GaN HEMT devices under high drain bias reliability testing," *Microelectronics Reliability,* vol. 49, pp. 478-483, 2009.

[48] A. Sozza, C. Dua, E. Morvan, M. diForte-Poisson, S. Delage, F. Rampazzo*, et al.*, "Evidence of traps creation in GaN/AlGaN/GaN HEMTs after a 3000 hour on-state and off-state hot-electron stress," in *Electron Devices Meeting, 2005. IEDM Technical Digest. IEEE International*, 2005, pp. 4 pp.-593.

[49] J. Joh and J. A. Del Alamo, "Critical voltage for electrical degradation of GaN high-electron mobility transistors," *Electron Device Letters, IEEE,* vol. 29, pp. 287-289, 2008.

[50] E. Zanoni, F. Danesin, M. Meneghini, A. Cetronio, C. Lanzieri, M. Peroni*, et al.*, "Localized damage in AlGaN/GaN HEMTs induced by reverse-bias testing," *Electron Device Letters, IEEE,* vol. 30, pp. 427-429, 2009.

[51] M. Tajima, J. Kotani, and T. Hashizume, "Effects of surface oxidation of AlGaN on DC characteristics of AlGaN/GaN high-electron-mobility transistors," *Japanese Journal of Applied Physics,* vol. 48, p. 0203, 2009.

[52] X. Cao, S. Pearton, A. Zhang, G. Dang, F. Ren, R. Shul*, et al.*, "Electrical effects of plasma damage in< equation> p-< font face='verdana'> GaN</equation>," *Applied physics letters,* vol. 75, pp. 2569-2571, 1999.

[53] K. Hirama, M. Kasu, and Y. Taniyasu, "Growth and Device Properties of AlGaN/GaN High-Electron Mobility Transistors on a Diamond Substrate," *Japanese Journal of Applied Physics,* vol. 51, p. 01AG09, 2012.

[54] S. P. S. Nakamura, G. Fasol, "The blue laser diode: the complete story," *Springer,* 2000 2000.

[55] J. W. Johnson, E. L. Piner, A. Vescan, R. Therrien, P. Rajagopal, J. C. Roberts*, et al.*, "12 W/mm AlGaN-GaN HFETs on silicon substrates," *Electron Device Letters, IEEE,* vol. 25, pp. 459-461, 2004.

[56] M. Leszczynski, H. Teisseyre, T. Suski, I. Grzegory, M. Bockowski, J. Jun*, et al.*, "Lattice parameters of gallium nitride," *Applied Physics Letters,* vol. 69, p. 73, 1996.

[57] *Properties*. Available: http://www.ioffe.ru/SVA/NSM/Semicond/

[58] F. Ponce, B. Krusor, J. Major Jr, W. Plano, and D. Welch, "Microstructure of GaN epitaxy on SiC using AlN buffer layers," *Applied physics letters,* vol. 67, pp. 410-412, 1995.

[59] J. Cho, E. Bozorg-Grayeli, D. H. Altman, M. Asheghi, and K. E. Goodson, "Low thermal resistances at GaN–SiC interfaces for HEMT technology," *Electron Device Letters, IEEE,* vol. 33, pp. 378-380, 2012.

[60] J. Cho, Y. Li, D. Altman, W. Hoke, M. Asheghi, and K. Goodson, "Temperature Dependent Thermal Resistances at GaN-substrate Interfaces in GaN Composite Substrates," in *Compound Semiconductor Integrated Circuit Symposium (CSICS), 2012 IEEE*, 2012, pp. 1-4.

[61] M. Alomari, A. Dussaigne, D. Martin, N. Grandjean, C. Gaquière, and E. Kohn, "AlGaN/GaN HEMT on (111) single crystalline diamond," *Electronics Letters,* vol. 46, p. 299, 2010.

[62] M. T. David Altman, James McClymonds, Samuel Kim, Samuel Graham, Jungwan Cho, Kenneth Goodson, Daniel Francis, Firooz Fail, Felix Ejeckam, and Steven Bernstein, "Analysis and Characterization of Thermal Transport in GaN HEMTs on Diamond Substrates," presented at the ITHERM 2014, Orlando, FL USA, 2014.

[63] D. Francis, F. Faili, D. Babić, F. Ejeckam, A. Nurmikko, and H. Maris, "Formation and characterization of 4-inch GaN-on-diamond substrates," *Diamond and Related Materials,* vol. 19, pp. 229-233, 2010.

[64] K. Hirama, Y. Taniyasu, and M. Kasu, "AlGaN/GaN high-electron mobility transistors with low thermal resistance grown on single-crystal diamond (111) substrates by metalorganic vapor-phase epitaxy," *Applied Physics Letters,* vol. 98, p. 162112, 2011.

[65] J. Cho, Z. Li, E. Bozorg-Grayeli, T. Kodama, D. Francis, F. Ejeckam, *et al.*, "Improved Thermal Interfaces of GaN–Diamond Composite Substrates for HEMT Applications," *Components, Packaging and Manufacturing Technology, IEEE Transactions on,* vol. 3, pp. 79-85, 2013.
[66] K. Hirama, Y. Taniyasu, and M. Kasu, "Heterostructure growth of a single-crystal hexagonal AlN (0001) layer on cubic diamond (111) surface," *Journal of Applied Physics,* vol. 108, p. 013528, 2010.
[67] K. Goodson, O. Käding, M. Rösler, and R. Zachai, "Experimental investigation of thermal conduction normal to diamond-silicon boundaries," *Journal of Applied Physics,* vol. 77, pp. 1385-1392, 1995.
[68] M. Touzelbaev and K. Goodson, "Impact of nucleation density on thermal resistance near diamond-substrate boundaries," *Journal of thermophysics and heat transfer,* vol. 11, pp. 506-512, 1997.
[69] K. E. Goodson, "Thermal conduction in nonhomogeneous CVD diamond layers in electronic microstructures," *Journal of Heat Transfer,* vol. 118, pp. 279-286, 1996.
[70] J. Graebner, S. Jin, G. Kammlott, Y.-H. Wong, J. Herb, and C. Gardinier, "Thermal conductivity and the microstructure of state-of-the-art chemical-vapor-deposited (CVD) diamond," *Diamond and Related materials,* vol. 2, pp. 1059-1063, 1993.
[71] J. Kuzmik, S. Bychikhin, D. Pogany, E. Pichonat, O. Lancry, C. Gaquière, *et al.*, "Thermal characterization of MBE-grown GaN/AlGaN/GaN device on single crystalline diamond," *Journal of Applied Physics,* vol. 109, p. 086106, 2011.
[72] V. Goyal, A. V. Sumant, D. Teweldebrhan, and A. A. Balandin, "Direct Low-Temperature Integration of Nanocrystalline Diamond with GaN Substrates for Improved Thermal Management of High-Power Electronics," *Advanced Functional Materials,* vol. 22, pp. 1525-1530, 2012.
[73] A. Sarua, H. Ji, K. Hilton, D. Wallis, M. J. Uren, T. Martin, *et al.*, "Thermal boundary resistance between GaN and substrate in AlGaN/GaN electronic devices," *Electron Devices, IEEE Transactions on,* vol. 54, pp. 3152-3158, 2007.
[74] J. P. Reifenberg, K.-W. Chang, M. A. Panzer, S. Kim, J. A. Rowlette, M. Asheghi, *et al.*, "Thermal boundary resistance measurements for phase-change memory devices," *Electron Device Letters, IEEE,* vol. 31, pp. 56-58, 2010.
[75] J. Das, H. Oprins, H. Ji, A. Sarua, W. Ruythooren, J. Derluyn, *et al.*, "Improved thermal performance of AlGaN/GaN HEMTs by an optimized flip-chip design," *Electron Devices, IEEE Transactions on,* vol. 53, pp. 2696-2702, 2006.
[76] N. Otsuka, S. Nagai, M. Yanagihara, Y. Uemoto, and D. Ueda, "Low-Pressure Direct-Liquid-Cooling Technology for GaN Power Transistors," *Japanese Journal of Applied Physics,* vol. 50, p. 04DF07, 2011.
[77] J. P. Calame, R. E. Myers, F. N. Wood, and S. C. Binari, "Simulations of direct-die-attached microchannel coolers for the thermal management of GaN-on-SiC microwave amplifiers," *Components and Packaging Technologies, IEEE Transactions on,* vol. 28, pp. 797-809, 2005.
[78] R. C. Jaeger, J. Goodling, M. Baginski, C. Ellis, N. Williamson, and R. O'Barr, "High heat flux cooling for silicon hybrid multichip packaging," *Components, Hybrids, and Manufacturing Technology, IEEE Transactions on,* vol. 12, pp. 772-779, 1989.

[79] J. Lee and I. Mudawar, "Two-phase flow in high-heat-flux micro-channel heat sink for refrigeration cooling applications: Part II—heat transfer characteristics," *International Journal of Heat and Mass Transfer,* vol. 48, pp. 941-955, 2005.

[80] M. Visaria and I. Mudawar, "Theoretical and experimental study of the effects of spray inclination on two-phase spray cooling and critical heat flux," *International Journal of Heat and Mass Transfer,* vol. 51, pp. 2398-2410, 2008.

[81] D. C. Wadsworth and I. Mudawar, "Enhancement of single-phase heat transfer and critical heat flux from an ultra-high-flux simulated microelectronic heat source to a rectangular impinging jet of dielectric liquid," *Journal of heat transfer,* vol. 114, pp. 764-768, 1992.

[82] I. Mudawar, "Direct-immersion cooling for high power electronic chips," in *Thermal Phenomena in Electronic Systems, 1992. I-THERM III, InterSociety Conference on*, 1992, pp. 74-84.

[83] J. Calame, R. Myers, S. Binari, F. Wood, and M. Garven, "Experimental investigation of microchannel coolers for the high heat flux thermal management of GaN-on-SiC semiconductor devices," *International Journal of Heat and Mass Transfer,* vol. 50, pp. 4767-4779, 2007.

[84] A. Sarua, H. F. Ji, M. Kuball, M. J. Uren, T. Martin, K. P. Hilton*, et al.*, "Integrated micro-Raman/Infrared thermography probe for monitoring of self-heating in AlGaN/GaN transistor structures," *Ieee Transactions on Electron Devices,* vol. 53, pp. 2438-2447, Oct 2006.

[85] K. Maize, E. Heller, D. Dorsey, and A. Shakouri, "Thermoreflectance CCD imaging of self heating in AlGaN/GaN high electron mobility power transistors at high drain voltage," in *Semiconductor Thermal Measurement and Management Symposium (SEMI-THERM), 2012 28th Annual IEEE*, 2012, pp. 173-181.

[86] J. Kuzmik, P. Javorka, A. Alam, M. Marso, M. Heuken, and P. Kordos, "Determination of channel temperature in AlGaN/GaN HEMTs grown on sapphire and silicon substrates using DC characterization method," *Ieee Transactions on Electron Devices,* vol. 49, pp. 1496-1498, Aug 2002.

[87] N. Killat, M. Kuball, T. M. Chou, U. Chowdhury, and J. Jimenez, "Temperature Assessment of AlGaN/GaN HEMTs: A Comparative study by Raman, Electrical and IR Thermography," *2010 International Reliability Physics Symposium,* pp. 528-531, 2010.

[88] R. Aubry, J.-C. Jacquet, J. Weaver, O. Durand, P. Dobson, G. Mills*, et al.*, "SThM temperature mapping and nonlinear thermal resistance evolution with bias on AlGaN/GaN HEMT devices," *Electron Devices, IEEE Transactions on,* vol. 54, pp. 385-390, 2007.

[89] T. Batten, A. Manoi, M. J. Uren, T. Martin, and M. Kuball, "Temperature analysis of AlGaN/GaN based devices using photoluminescence spectroscopy: Challenges and comparison to Raman thermography," *Journal of Applied Physics,* vol. 107, Apr 1 2010.

[90] T. Beechem III, "Metrology of gan electronics using micro-raman spectroscopy," 2008.

[91] G. Lucazeau, "Effect of pressure and temperature on Raman spectra of solids: anharmonicity," *Journal of Raman Spectroscopy,* vol. 34, pp. 478-496, 2003.

[92] M. Kuball, J. M. Hayes, M. J. Uren, T. Martin, J. C. H. Birbeck, R. S. Balmer*, et al.*, "Measurement of temperature in active high-power AlGaN/GaN HFETs using Raman spectroscopy," *Ieee Electron Device Letters,* vol. 23, pp. 7-9, Jan 2002.

[93] M. Kuball, J. M. Hayes, Y. Shi, and J. H. Edgar, "Phonon lifetimes in bulk AlN and their temperature dependence," *Applied Physics Letters,* vol. 77, pp. 1958-1960, Sep 25 2000.
[94] T. Beechem, A. Christensen, S. Graham, and D. Green, "Micro-Raman thermometry in the presence of complex stresses in GaN devices," *Journal of Applied Physics,* vol. 103, p. 124501, 2008.
[95] T. Beechem, A. Christensen, S. Graham, and D. Green, "Micro-Raman thermometry in the presence of complex stresses in GaN devices," *Journal of Applied Physics,* vol. 103, Jun 15 2008.
[96] T. Batten, J. W. Pomeroy, M. J. Uren, T. Martin, and M. Kuball, "Simultaneous measurement of temperature and thermal stress in AlGaN/GaN high electron mobility transistors using Raman scattering spectroscopy," *Journal of Applied Physics,* vol. 106, Nov 1 2009.
[97] S. Choi, E. R. Heller, D. Dorsey, R. Vetury, and S. Graham, "The Impact of Bias Conditions on Self-Heating in AlGaN/GaN HEMTs," *Electron Devices, IEEE Transactions on,* vol. 60, pp. 159-162, 2013.
[98] S. Choi, S. Graham, E. Heller, and D. Dorsey, "The Analysis of Wide Band Gap Semiconductors Using Raman Spectroscopy," pp. 545-582, 2013.
[99] A. V. Sukhadolau, E. V. Ivakin, V. G. Ralchenko, A. V. Khomich, A. V. Vlasov, and A. F. Popovich, "Thermal conductivity of CVD diamond at elevated temperatures," *Diamond and Related Materials,* vol. 14, pp. 589-593, 2005.
[100] S. Coe and R. Sussmann, "Optical, thermal and mechanical properties of CVD diamond," *Diamond and Related Materials,* vol. 9, pp. 1726-1729, 2000.
[101] T. Beechem, S. Graham, S. P. Kearney, L. M. Phinney, and J. R. Serrano, "Invited Article: Simultaneous mapping of temperature and stress in microdevices using micro-Raman spectroscopy," *Rev Sci Instrum,* vol. 78, p. 061301, Jun 2007.
[102] T. Beechem, A. Christensen, D. Green, and S. Graham, "Assessment of stress contributions in GaN high electron mobility transistors of differing substrates using Raman spectroscopy," *Journal of Applied Physics,* vol. 106, pp. 114509-114509-9, 2009.
[103] Available: http://www.stratedge.com/
[104] C. Roder, S. Einfeldt, S. Figge, and D. Hommel, "Temperature dependence of the thermal expansion of GaN," *Physical Review B,* vol. 72, p. 085218, 2005.
[105] S. H. Lee, S. Y. Kwon, and H. J. Ham, "Thermal conductivity of tungsten–copper composites," *Thermochimica Acta,* vol. 542, pp. 2-5, 2012.
[106] Z. Li and R. Bradt, "Thermal expansion of the hexagonal (6H) polytype of silicon carbide," *Journal of the American Ceramic Society,* vol. 69, pp. 863-866, 1986.
[107] N. Nakamura, H. Ogi, and M. Hirao, "Elastic constants of chemical-vapor-deposition diamond thin films: resonance ultrasound spectroscopy with laser-Doppler interferometry," *Acta Materialia,* vol. 52, pp. 765-771, 2004.
[108] A. Polian, M. Grimsditch, and I. Grzegory, "Elastic constants of gallium nitride," *Journal of Applied Physics,* vol. 79, p. 3343, 1996.
[109] J. Jungwoo and J. A. del Alamo, "Time evolution of electrical degradation under high-voltage stress in GaN high electron mobility transistors," in *Reliability Physics Symposium (IRPS), 2011 IEEE International*, 2011, pp. 4E.3.1-4E.3.4.
[110] E. Douglas, C. Chang, B. Gila, M. Holzworth, K. Jones, L. Liu*, et al.*, "Investigation of the effect of temperature during off-state degradation of AlGaN/GaN High Electron Mobility Transistors," *Microelectronics Reliability,* vol. 52, pp. 23-28, 2012.

[111] P. E. Burrows, V. Bulovic, S. R. Forrest, L. S. Sapochak, D. M. Mccarty, and M. E. Thompson, "Reliability and Degradation of Organic Light-Emitting Devices," *Applied Physics Letters,* vol. 65, pp. 2922-2924, Dec 5 1994.

[112] P. E. Burrows, G. L. Graff, M. E. Gross, P. M. Martin, M. K. Shi, M. Hall*, et al.*, "Ultra barrier flexible substrates for flat panel displays," *Displays,* vol. 22, pp. 65-69, May 2001.

[113] G. L. Graff, R. E. Williford, and P. E. Burrows, "Mechanisms of vapor permeation through multilayer barrier films: Lag time versus equilibrium permeation," *Journal of Applied Physics,* vol. 96, pp. 1840-1849, Aug 15 2004.

[114] M. S. Weaver, L. A. Michalski, K. Rajan, M. A. Rothman, J. A. Silvernail, J. J. Brown*, et al.*, "Organic light-emitting devices with extended operating lifetimes on plastic substrates," *Applied Physics Letters,* vol. 81, pp. 2929-2931, Oct 14 2002.

[115] P. Mandlik, J. Gartside, L. Han, I. C. Cheng, S. Wagner, J. A. Silvernail*, et al.*, "A single-layer permeation barrier for organic light-emitting displays," *Applied Physics Letters,* vol. 92, Mar 10 2008.

[116] P. F. Carcia, R. S. McLean, M. H. Reilly, M. D. Groner, and S. M. George, "Ca test of Al2O3 gas diffusion barriers grown by atomic layer deposition on polymers," *Applied Physics Letters,* vol. 89, p. 3, Jul 2006.

[117] A. A. Dameron, S. D. Davidson, B. B. Burton, P. F. Carcia, R. S. McLean, and S. M. George, "Gas diffusion barriers on polymers using multilayers fabricated by Al2O3 and rapid SiO2 atomic layer deposition," *Journal of Physical Chemistry C,* vol. 112, pp. 4573-4580, Mar 27 2008.

[118] S. M. George, "Atomic Layer Deposition: An Overview," *Chemical Reviews,* vol. 110, pp. 111-131, Jan 2010.

[119] M. D. Groner, S. M. George, R. S. McLean, and P. F. Carcia, "Gas diffusion barriers on polymers using Al2O3 atomic layer deposition," *Applied Physics Letters,* vol. 88, Jan 30 2006.

[120] N. Kim, W. J. Potscavage, B. Domercq, B. Kippelen, and S. Graham, "A hybrid encapsulation method for organic electronics," *Applied Physics Letters,* vol. 94, pp. -, Apr 20 2009.

[121] *ALD*. Available: http://en.wikipedia.org/wiki/Atomic_layer_deposition

[122] A. Bulusu, H. Kim, D. Samet, and S. Graham Jr, "Improving the stability of atomic layer deposited alumina films in aqueous environments with metal oxide capping layers," *Journal of Physics D: Applied Physics,* vol. 46, 2013.

[123] M.-H. Cho, Y. Roh, C. Whang, K. Jeong, H. Choi, S. Nam*, et al.*, "Dielectric characteristics of Al2O3–HfO2 nanolaminates on Si (100)," *Applied physics letters,* vol. 81, pp. 1071-1073, 2002.

[124] J. Kuzmik, G. Pozzovivo, C. Ostermaier, G. Strasser, D. Pogany, E. Gornik*, et al.*, "Analysis of degradation mechanisms in lattice-matched InAlN/GaN high-electron-mobility transistors," *Journal of Applied Physics,* vol. 106, pp. 124503-124503-7, 2009.

[125] S. Choi, E. Heller, D. Dorsey, and S. Graham, "The Analysis of Wide Band Gap Semiconductors Using Raman Spectroscopy," in *Materials and Reliability Handbook for Semiconductor Optical and Electron Devices*, O. Ueda and S. J. Pearton, Eds., ed: Springer New York, 2013, pp. 545-582.

[126] S. Choi, E. Heller, D. Dorsey, R. Vetury, and S. Graham, "Analysis of the residual stress distribution in AlGaN/GaN high electron mobility transistors," *Journal of Applied Physics,* vol. 113, p. 093510, 2013.